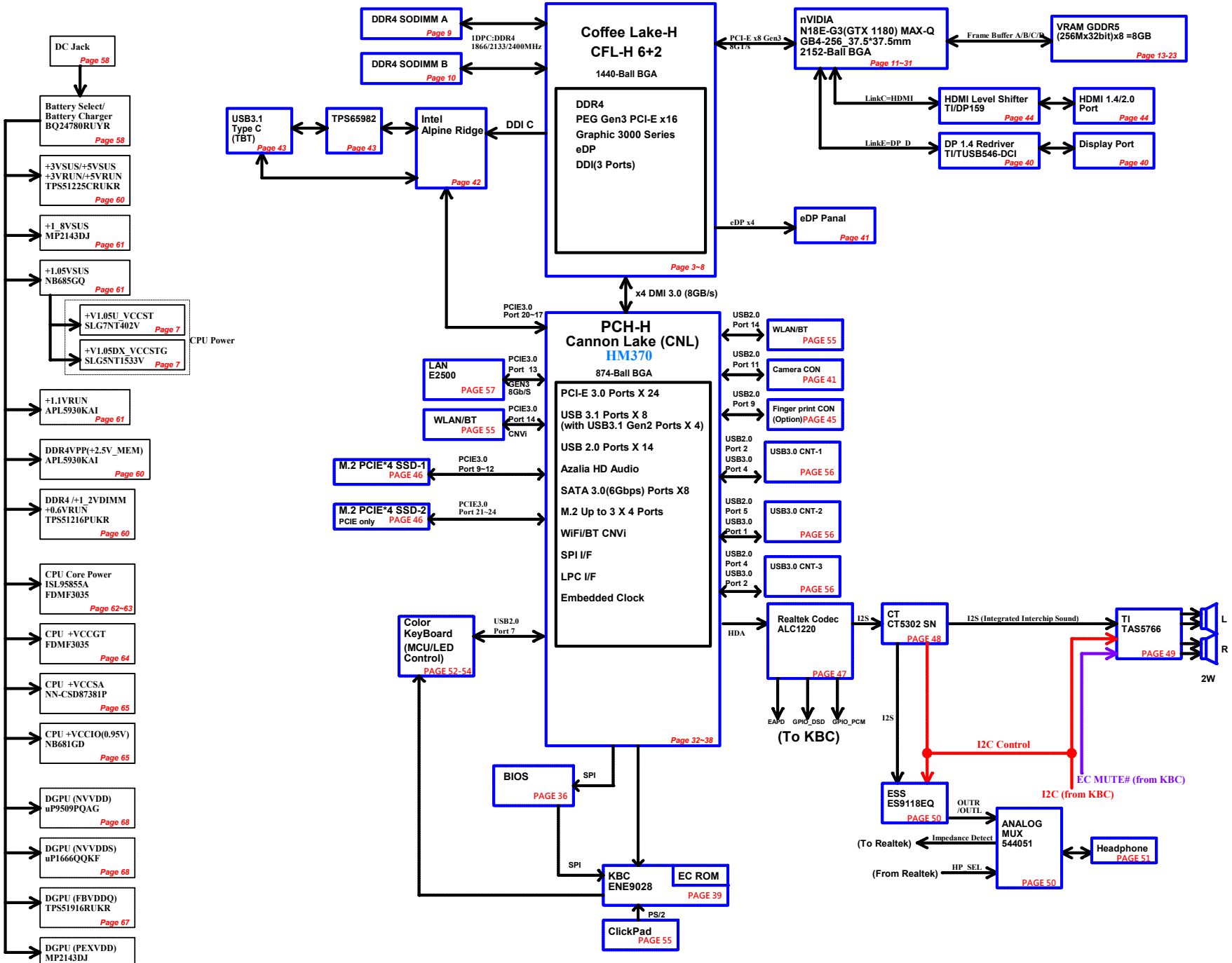
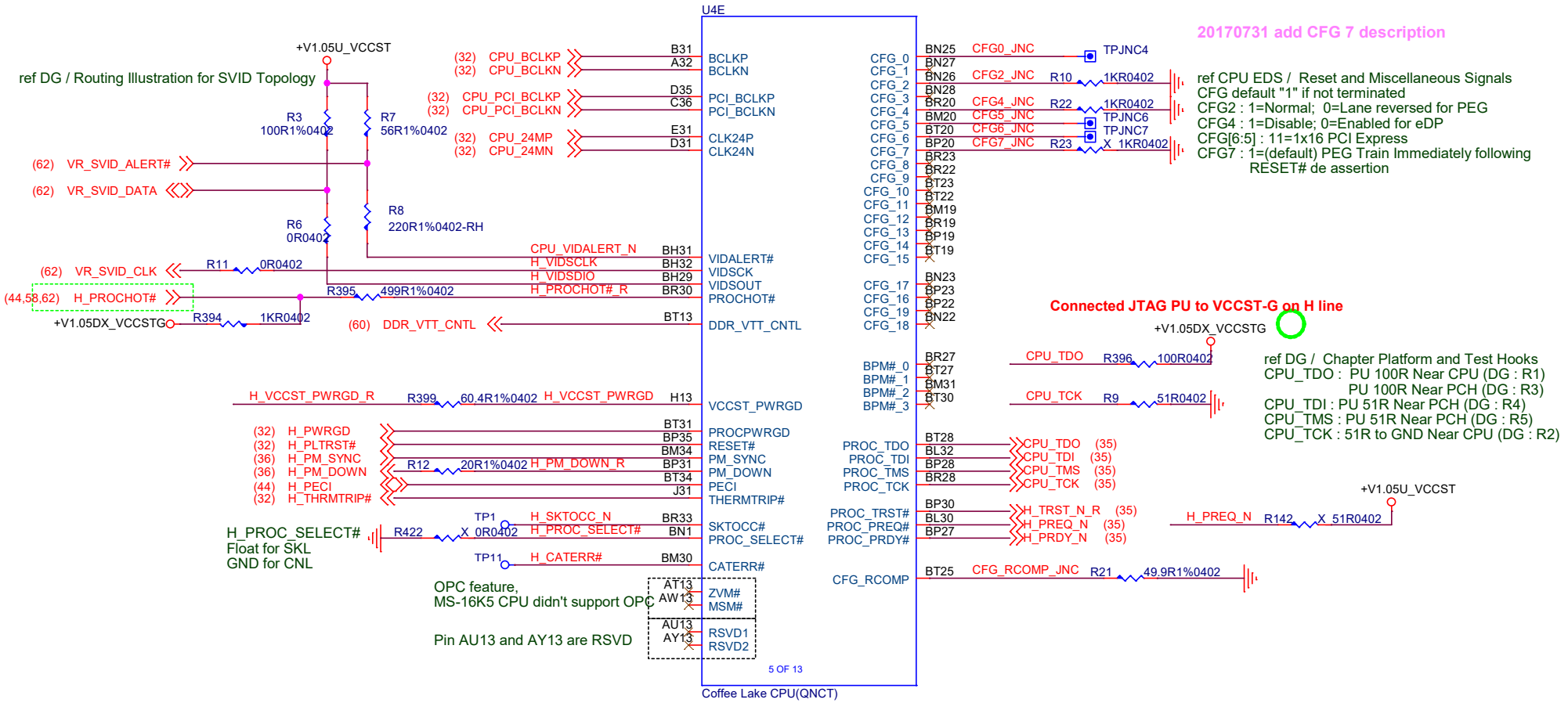
MS-16Q4 Ver : 10

Intel Coffee Lake-H

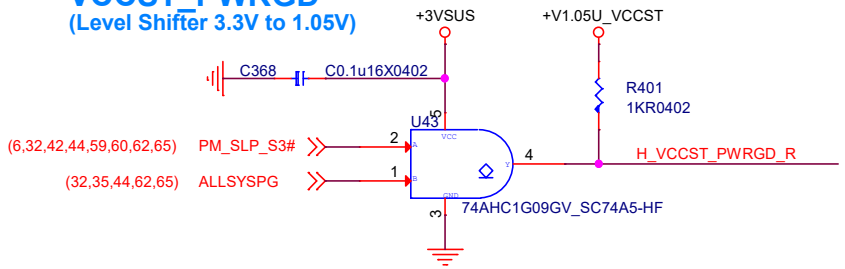


msi	MICRO-STAR INT'L CO.,LTD.
Title	Block Diagram
Size	Document Number: MS-16Q4
Rev	10
Date:	Sheet 1 of 75

CFL-H (HOST)



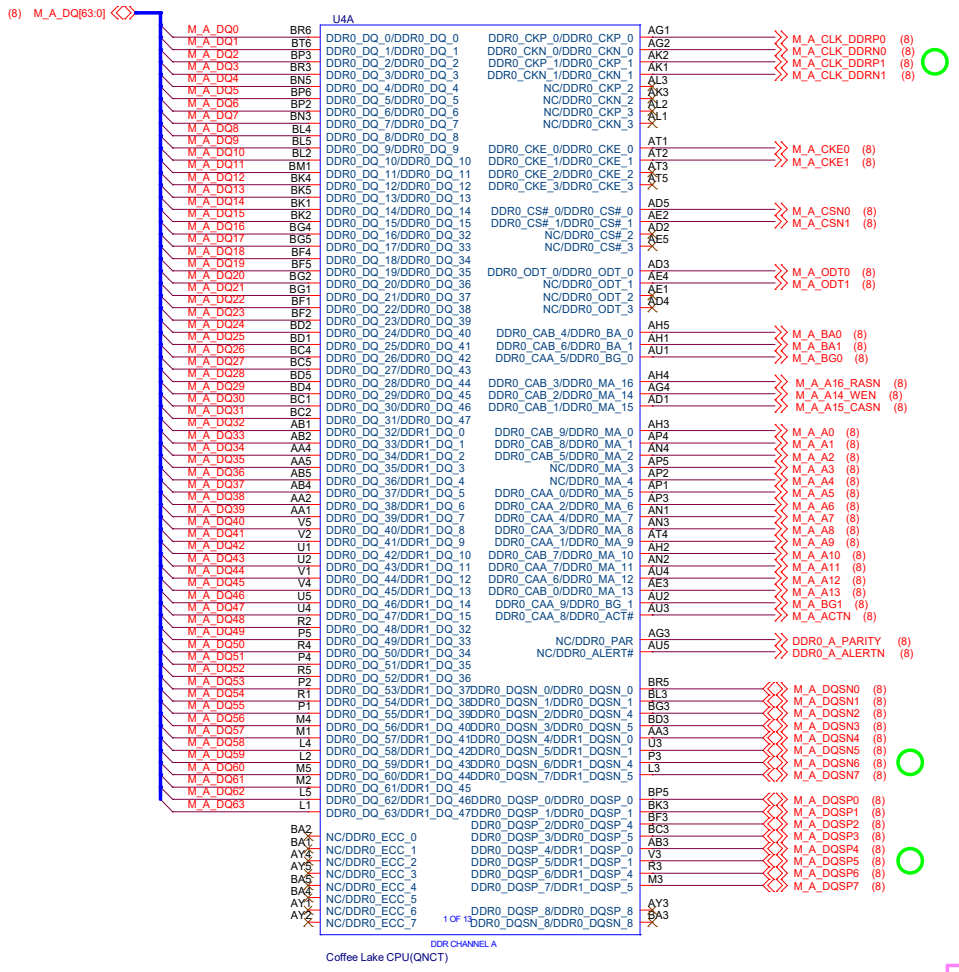
VCCST_PWRGD
(Level Shifter 3.3V to 1.05V)



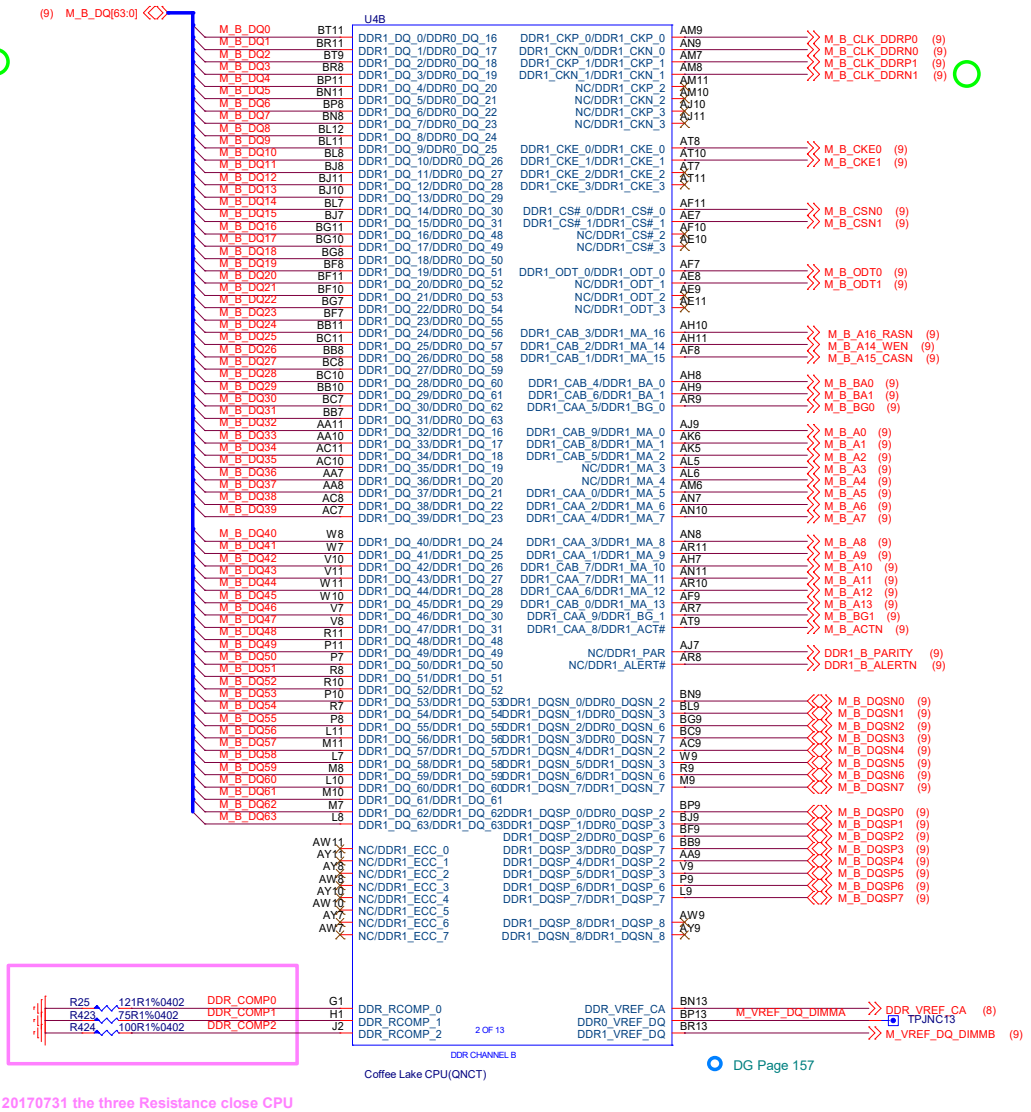
74AHC1G09GV is AND Gate with open drain output

MICRO-STAR INT'L CO.,LTD.		
Title: CFL-H(HOST)		
Size: Custom	Document Number: MS-16Q4	Rev: 10
Date: Monday, December 24, 2018	Sheet 2 of 75	

DDR Channel A



DDR Channel B



DG Page 157

20170731 the three Resistance close CPU

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Title: CFL-H(DDR4)			
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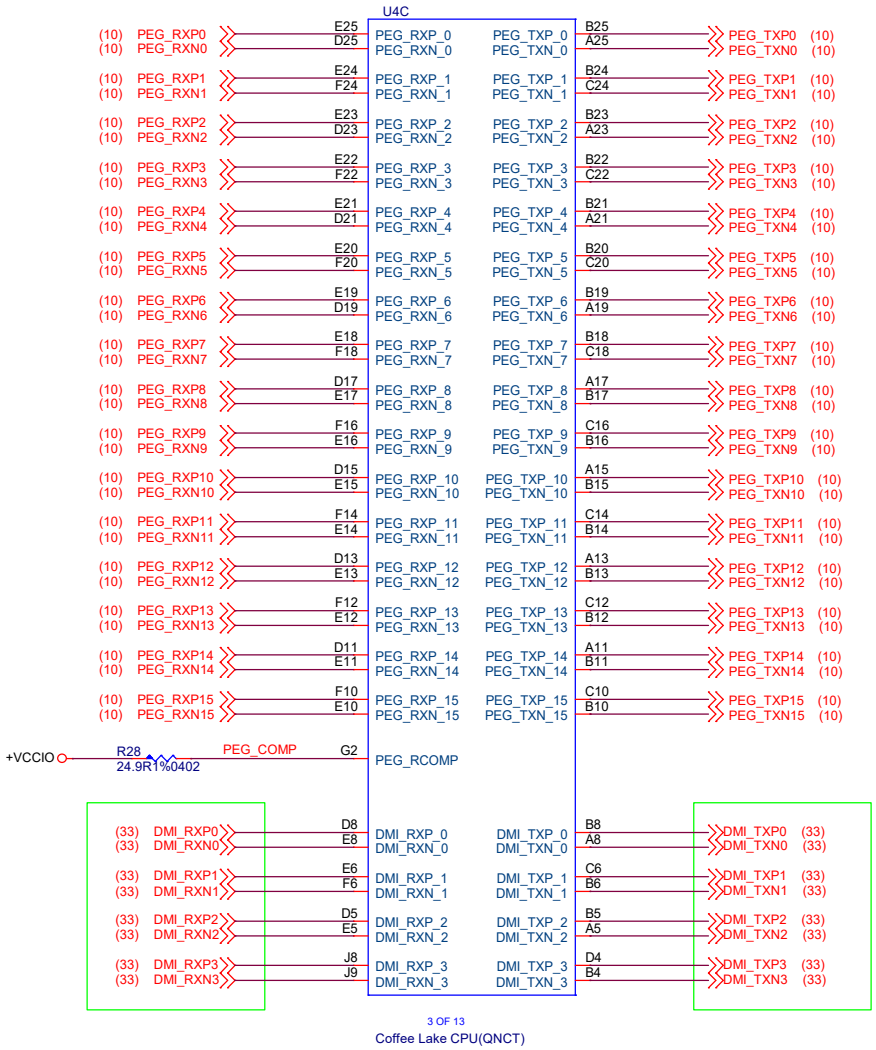
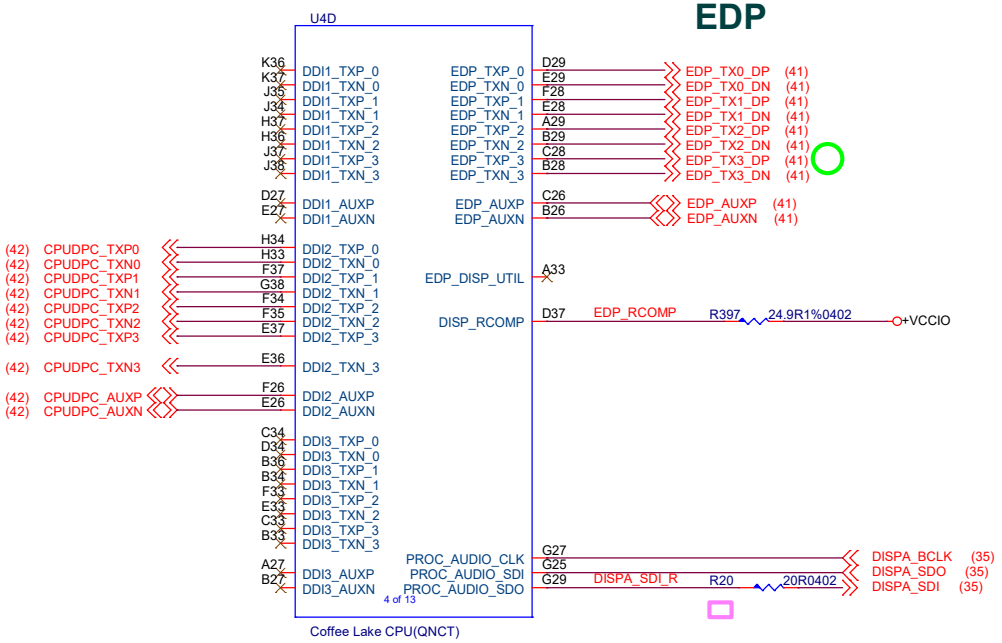


DDI C
DP to AR



EDP

20170731 change R2351 to 20R to follow DG

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	CFL-H(DMI/Display)	
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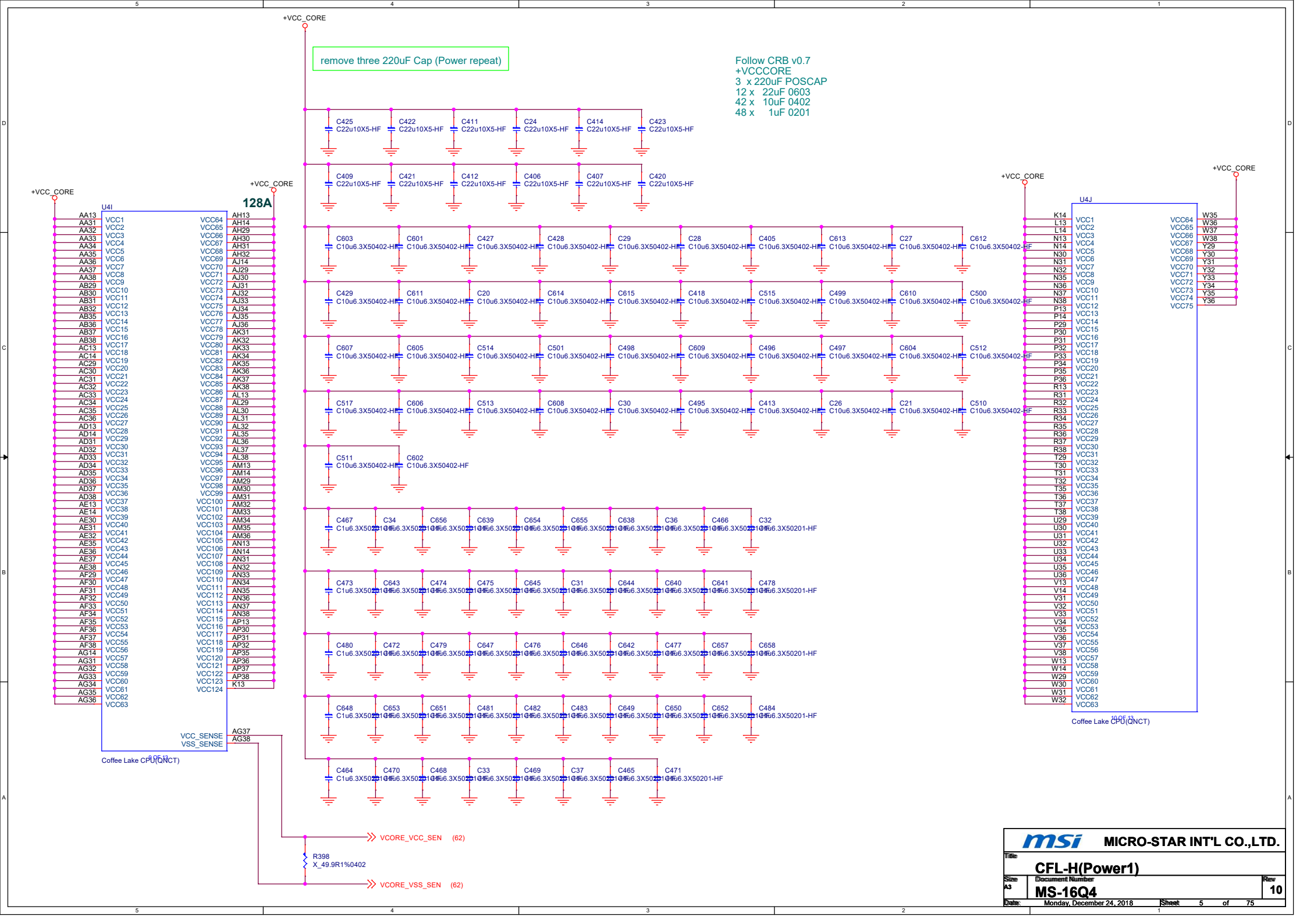
+VCC_CORE
remove three 220uF Cap (Power repeat)
Follow CRB v0.7
+VCCCORE
3 x 220uF POSCAP
12 x 22uF 0603
42 x 10uF 0402
48 x 1uF 0201
128A
U4I
Coffee Lake CPU(QNCT)
U4J
Coffee Lake CPU(QNCT)
VCC_SENSE
VSS_SENSE
VCORE_VCC_SEN (62)
VCORE_VSS_SEN (62)
R398
X_49.9R1%0402
MICRO-STAR INT'L CO.,LTD.
CFL-H(Power1)
MS-16Q4
Monday, December 24, 2018

Follow CRB v0.7
+VCCDU (+1_2VDIMM)
4 x 22uF 0603
12 x 10uF 0402

11.1A

+VCCSA

U4L

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8 VCCSA9 VCCSA10 VCCSA11 VCCSA12 VCCSA13 VCCSA14 VCCSA15 VCCSA16 VCCSA17 VCCSA18 VCCSA19 VCCSA20 VCCSA21 VCCSA22

3.3A

+1_2VDIMM

C805 C796 C814 C806 C22u10X5-HF

C804 C797 C803 C673 C793 C1034 C679 C792 C675 C676 C699 C10u6.3X50402-HF

Close CPU Y23 pin

C677 C10u6.3X50402-HF

6.4A

+VCCIO

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21

0.13A

+VCCSFR_OC

VCCPLL_OC1 VCCPLL_OC2 VCCPLL_OC3

0.06A

+V1.05U_VCCST

VCCST

0.02A

+V1.05DX_VCCSTG

VCCSTG2 VCCSTG1

0.15A

+V1.05U_VCCPLL

VCCPLL1 VCCPLL2

VCCSA_SENSE VSSSA_SENSE

VCCSA_VCC_SENSE (62)
VCCSA_VSS_SENSE (62)

VCCIO_SENSE VSSIO_SENSE

+VCCIO

12 OF 13
Coffee Lake CPU(QNCT)

Remove +VCCVDDQ_CLK, it combine with VDDQ.
Pin number : Y12

+VCCSFR_OC R417 0R0402 +1_2VDIMM

+V1.05U_VCCPLL R408 0R0402 +V1.05U_VCCST

+V1.05U_VCCPLL C489 C1u10X50402-HF

Close CPU H28 and J28 pin

recommend external test point on CRBv0.7.

TPJNC14 TPEV_PEG_VIEW_2

U4M

RSVD_TP5 IST_TRIG RSVD_TP4 RSVD_TP3 RSVD_TP1 RSVD_TP2 RSVD15 RSVD28 RSVD27 RSVD14 RSVD13 RSVD30 RSVD31 RSVD2 RSVD1 RSVD5 RSVD4 VSS_A36 VSS_A37 PROC_TRIGIN PROC_TRIGOUT RSVD24 RSVD23 RSVD7 RSVD21 RSVD26 RSVD29 RSVD19 RSVD18 RSVD9 RSVD11 RSVD10 RSVD12 RSVD3 RSVD25 RSVD22 RSVD20 RSVD17 RSVD16 RSVD8 RSVD6

(35) PCH_2_CPU_TRIGGER_R
(35) CPU_2_PCH_TRIGGER_R
R409 30R0402 CPU_2_PCH_TRIGGER

13 OF 13
Coffee Lake CPU(QNCT)

Follow CRB v0.7
+VCCSA
5 x 47uF 0805
4 x 22uF 0603
7 x 10uF 0402
1 x 1uF 0201

+VCCSA 20180221

C395 C386 C410 C16 C408 C18 C23 C419 C424 C22u4X60603

20181001 C401 C400 C397 C398 C399 C394 C19 C10u4X6S0402-HF
20181001
20181001

C35 C1u6.3X50201-HF

+VCCIO

C600 C660 C519 C10u6.3X50402-HF

Follow CRB v0.7
+VCCIO
3 x 22uF 0603

+V1.05DX_VCCSTG

Cap side of CRB and PDG are 0201

C41 C1u6.3X60402

+VCCSFR_OC

Cap side of CRB and PDG are 0201

C674 C633 C1u10X50402-HF

+V1.05U_VCCST

Cap side of CRB and PDG are 0201

C446 C1u6.3X60402

Close CPU H30 pin

+V1.05DX_VCCSTG

+V1.05DX_VCCSTG +3VSUS

U2 VDD S D CAP GND ON SLG5NT1533V_STDFN8-HF

C43 C0.1u50X0402-HF
+1.05VSUS
C440 C10u4X6S0402-HF
VCCSTG_EN R18 0R0402

C42 C470p50X0402

+3VSUS

U3 X_M74VHC1GT08DFT2G_SC705-RH

R17 100KR0402

PM_SLP_S3# (2,32,42,44,59,60,62,65)
1.8V Level
CPU_C10_GATE# (36,65)

PN : T3E-1GT0800-O05
MC74VHC1GT08
AND Gate Level Shifter

	VCC	Min	Max
VIH	3V	1.4V	
VIL	3V		0.53V

(1)Ref DG Section 51.1.3
VCCSTG should be gated by
{SLP_S3#} AND {CPU_C10_GATE#}
(2)Power Sequence spec tCPU26 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us

20170913 add R604 to follow DG

20170731 change C45 to 0.1uF

+V1.05U_VCCST

+V1.05U_VCCST +3VSUS

U44 VDD S D CAP GND ON SLG5NT1533V_STDFN8-HF

C45 C0.1u50X0402-HF
+1.05VSUS
C44 C10u4X6S0402-HF
PM_SLP_S4# (32,44,60)

C450 C220p50N0402

R404 100KR0402

Discharge R Max 300 Ohm

Ref DG Table 51-1
VCCST gated by SLP_S4#

20170731 change C45 to 0.1uF
20170804 change U39 to SLG5NT1533V to correct power sequence control by PM_SLP_S4#
C404 change from 2200pF to 220pF

MICRO-STAR INT'L CO.,LTD.

Title: CFL-H(Power2)

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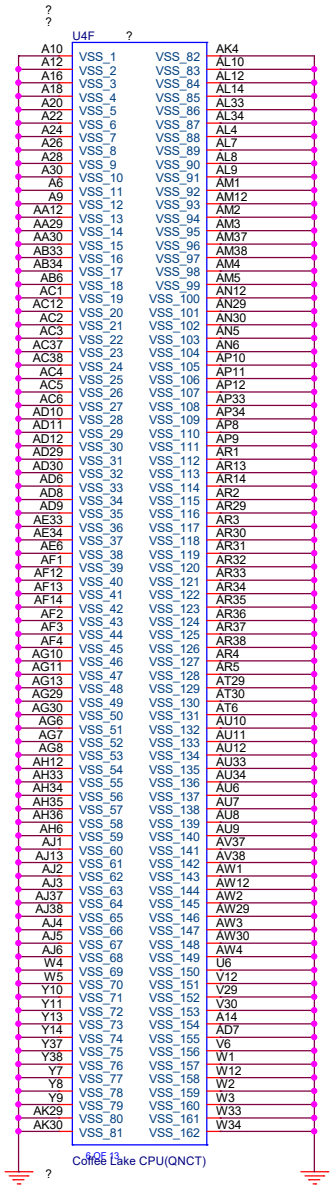

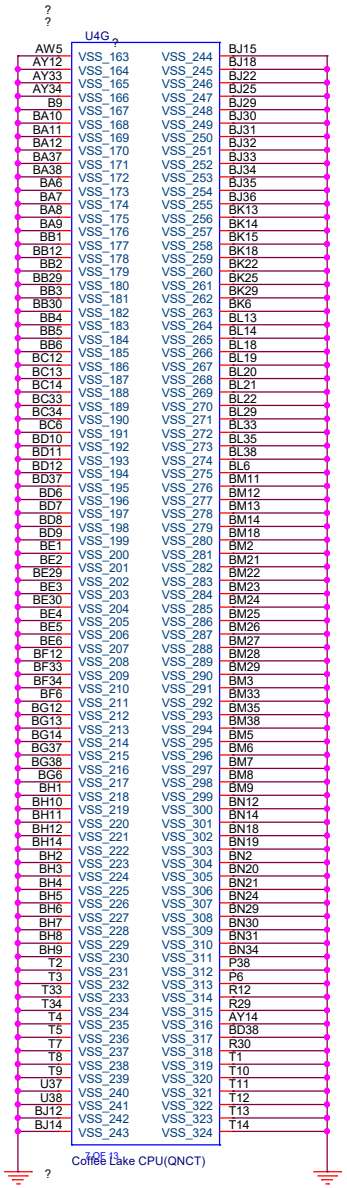

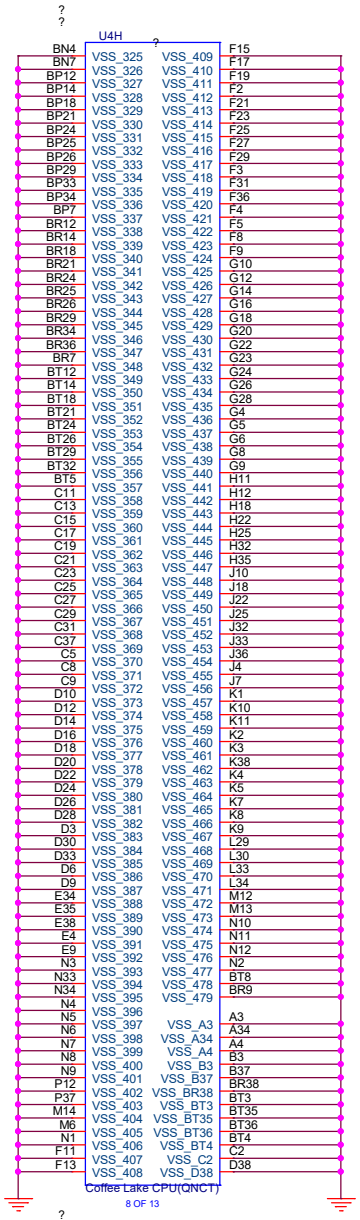

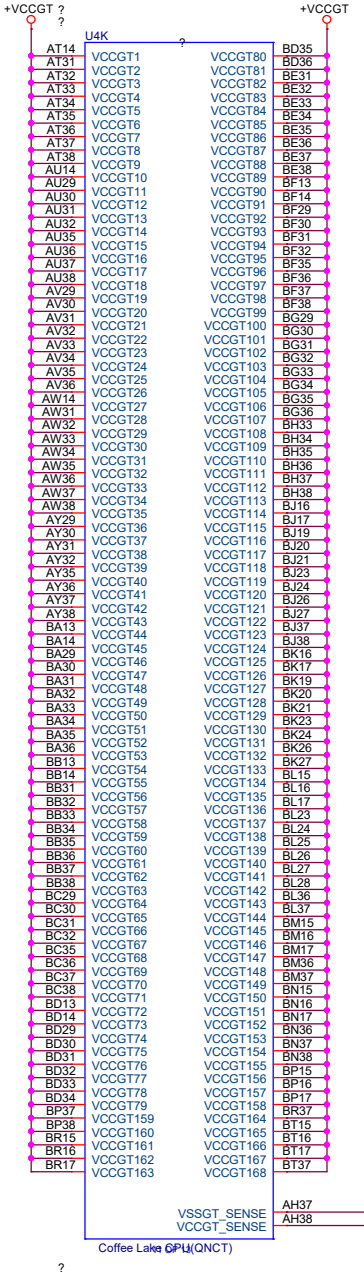

32A

+VCCGT

C40 C557 C525 C415 C449 C503 C434 — C47u6.3X50805-HF
C448 C458 C447 C416 C25 C444 C435 — C22u10X5-HF
C555 C634 C659 C635 C579 C518 C492 C494 C493 C487 — C10u6.3X50402-HF
C460 C505 C486 C485 C637 C463 C529 C504 C636 C462 C461 C618 — C1u6.3X50201-HF

VCCGT_VSS_SEN (62)
VCCGT_VCC_SEN (62)

remove two 220uF Cap for +VCCGT
(Power repeat)

Follow CRB v0.7
+VCCGT
2 x 220uF POSCAP
7 x 47uF 0805
7 x 22uF 0603
10x 10uF 0402
12x 1uF 0201

MICRO-STAR INT'L CO.,LTD.

Title: CFL-H(Power3)

Size: A3 | Document Number: MS-16Q4 | Rev: 10

Date: Monday, December 24, 2018 | Sheet 7 of 75

SODIMM_A0 (TOP-Reverse)

SOCKET1A

(3) M_A_DQ[63:0]

M_A_DQ5 8
M_A_DQ0 7
M_A_DQ2 20
M_A_DQ3 21
M_A_DQ1 4
M_A_DQ4 3
M_A_DQ6 16
M_A_DQ7 17
M_A_DQ8 28
M_A_DQ12 29
M_A_DQ14 41
M_A_DQ11 42
M_A_DQ9 24
M_A_DQ13 25
M_A_DQ10 38
M_A_DQ15 37
M_A_DQ17 50
M_A_DQ20 49
M_A_DQ23 62
M_A_DQ18 63
M_A_DQ16 46
M_A_DQ21 45
M_A_DQ19 58
M_A_DQ22 59
M_A_DQ25 70
M_A_DQ28 71
M_A_DQ30 83
M_A_DQ31 84
M_A_DQ24 66
M_A_DQ29 67
M_A_DQ27 79
M_A_DQ26 80
M_A_DQ32 174
M_A_DQ37 173
M_A_DQ39 187
M_A_DQ34 186
M_A_DQ36 170
M_A_DQ33 169
M_A_DQ38 183
M_A_DQ35 182
M_A_DQ41 195
M_A_DQ45 194
M_A_DQ46 207
M_A_DQ42 208
M_A_DQ44 191
M_A_DQ40 190
M_A_DQ43 203
M_A_DQ47 204
M_A_DQ49 216
M_A_DQ52 215
M_A_DQ55 228
M_A_DQ51 229
M_A_DQ50 211
M_A_DQ48 212
M_A_DQ53 224
M_A_DQ54 225
M_A_DQ61 237
M_A_DQ60 236
M_A_DQ58 249
M_A_DQ63 250
M_A_DQ56 232
M_A_DQ57 233
M_A_DQ62 245
M_A_DQ59 246

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

(3) M_A_BG0 115
(3) M_A_BG1 113
BG0 BG1

A0 144 — M_A_A0 (3)
A1 132 — M_A_A1 (3)
A2 131 — M_A_A2 (3)
A3 128 — M_A_A3 (3)
A4 126 — M_A_A4 (3)
A5 127 — M_A_A5 (3)
A6 122 — M_A_A6 (3)
A7 125 — M_A_A7 (3)
A8 121 — M_A_A8 (3)
A9 146 — M_A_A9 (3)
A10/AP 120 — M_A_A10 (3)
A11 119 — M_A_A11 (3)
A12 158 — M_A_A12 (3)
A13 151 — M_A_A13 (3)
A14/WE# 156 — M_A_A14_WEN (3)
A15/CAS# 152 — M_A_A15_CASN (3)
A16/RAS# — M_A_A16_RASN (3)

BA0 150 — M_A_BA0 (3)
BA1 145 — M_A_BA1 (3)
CS0# 149 — M_A_CSN0 (3)
CS1# 157 — M_A_CSN1 (3)
CK0 137 — M_A_CLK_DDRP0 (3)
CK0# 139 — M_A_CLK_DDRN0 (3)
CK1 138 — M_A_CLK_DDRP1 (3)
CK1# 140 — M_A_CLK_DDRN1 (3)
CKE0 109 — M_A_CKE0 (3)
CKE1 110 — M_A_CKE1 (3)
SCL 253 — SMB_CLK_DIMM (9,35,55)
SDA 254 — SMB_DATA_DIMM (9,35,55)
ODT0 155 — M_A_ODT0 (3)
ODT1 161 — M_A_ODT1 (3)

DM0#/DBIO# 12 — +1_2VDIMM
DM1#/DBI1# 33
DM2#/DBI2# 54
DM3#/DBI3# 75
DM4#/DBI4# 178
DM5#/DBI5# 199
DM6#/DBI6# 220
DM7#/DBI7# 241
DBI8# 96

DQS0 13 — M_A_DQSP0 (3)
DQS1 34 — M_A_DQSP1 (3)
DQS2 55 — M_A_DQSP2 (3)
DQS3 76 — M_A_DQSP3 (3)
DQS4 179 — M_A_DQSP4 (3)
DQS5 200 — M_A_DQSP5 (3)
DQS6 221 — M_A_DQSP6 (3)
DQS7 242 — M_A_DQSP7 (3)
DQS8 97
DQS0# 11 — M_A_DQSN0 (3)
DQS1# 32 — M_A_DQSN1 (3)
DQS2# 53 — M_A_DQSN2 (3)
DQS3# 74 — M_A_DQSN3 (3)
DQS4# 177 — M_A_DQSN4 (3)
DQS5# 198 — M_A_DQSN5 (3)
DQS6# 219 — M_A_DQSN6 (3)
DQS7# 240 — M_A_DQSN7 (3)
DQS8# 95

SA0 256 — SA0_DIMA0_0_0 JNC2 1 2 X_0402
SA1 260 — SA1_DIMA0_0_0 JNC4 1 2 X_0402
RFU 166 — SA2_DIMA0_0_0 JNC3 1 2 X_0402

A0 (0 0 0)

DDR4SODIMM-260PS_BLACK-HF-20
DDR4_SODIMM260P_H4_5
N13-2600220-L41

20170912 C922 change to C71-33102AE-P01
ref DG/ Section 4.14.1
CFL-H DDR4 SDDIMM Power Plane Decoupling

+1_2VDIMM
C1008 1 2 C330u2SO-HF

+1_2VDIMM
C900 C10u6.3X50402-HF
C872 C10u6.3X50402-HF
C891 C10u6.3X50402-HF
C889 C10u6.3X50402-HF
C868 C10u6.3X50402-HF
C920 C10u6.3X50402-HF
C879 C10u6.3X50402-HF
C941 C10u6.3X50402-HF
C873 C10u6.3X50402-HF
C935 C10u6.3X50402-HF
C880 C10u6.3X50402-HF
C953 C10u6.3X50402-HF
C904 C10u6.3X50402-HF
C923 C10u6.3X50402-HF
C945 C10u6.3X50402-HF
C942 C10u6.3X50402-HF

+1_2VDIMM
C871 C1u10X50402-HF
C927 C1u10X50402-HF
C870 C1u10X50402-HF
C869 C1u10X50402-HF
C874 C1u10X50402-HF
C926 C1u10X50402-HF
C924 C1u10X50402-HF
C938 C1u10X50402-HF
C898 C1u10X50402-HF
C865 C1u10X50402-HF
C922 C1u10X50402-HF
C914 C1u10X50402-HF
C890 C1u10X50402-HF
C864 C1u10X50402-HF
C925 C1u10X50402-HF
C921 C1u10X50402-HF

+1_2VDIMM
R516 1KR1%0402
M_VREF_CA_DIMM
R527 2R1%0402 — DDR_VREF_CA (3)
R519 1KR1%0402
C1039 C0.1u16X0402
C1041 C0.022u25X0402
R528 24.9R1%0402

+1_2VDIMM
2A
C858 C1u6.3X60402
C961 C10u4X6S0402-HF
C892 C1u6.3X60402
C885 C10u4X6S0402-HF
1A

+2.5V_MEM
M_VREF_CA_DIMM
C946 C10u6.3X50402-HF
C937 C0.1u16X0402

VDDQ_VTT
750mA
C1033 C10u6.3X50402-HF
C997 C1u10X50402-HF
C1031 C1u10X50402-HF

SOCKET1B

+3VRUN
C844 C0.1u16X0402
C852 C2.2u6.3X60402-HF

+1_2VDIMM
R526 470R1%0402
R522 0R0402 — PCH_DRAMRST# (32)
C1037 X_C0.1u16X0402

111 VDD-1
112 VDD-2
117 VDD-3
118 VDD-4
123 VDD-5
124 VDD-6
129 VDD-7
130 VDD-8
135 VDD-9
136 VDD-10
141 VDD-11
142 VDD-12
147 VDD-13
148 VDD-14
153 VDD-15
154 VDD-16
159 VDD-17
160 VDD-18
163 VDD-19

257 VPP-1
259 VPP-2

164 VREF_CA
258 VTT

167 VSS-53
168 VSS-54
171 VSS-55
172 VSS-56
175 VSS-57
176 VSS-58
180 VSS-59
181 VSS-60
184 VSS-61
185 VSS-62
188 VSS-63
189 VSS-64
192 VSS-65
193 VSS-66
196 VSS-67
197 VSS-68
201 VSS-69
202 VSS-70
205 VSS-71
206 VSS-72
209 VSS-73
210 VSS-74
213 VSS-75
214 VSS-76
217 VSS-77
218 VSS-78
222 VSS-79
223 VSS-80
226 VSS-81
227 VSS-82
230 VSS-83
231 VSS-84
234 VSS-85
235 VSS-86
238 VSS-87
239 VSS-88
243 VSS-89
244 VSS-90
247 VSS-91
248 VSS-92
251 VSS-93
252 VSS-94

261 261
262 262

MEC2 MEC2
MEC1 MEC1

VDDSPD 255

CB0/NC4 92
CB1/NC3 91
CB2/NC6 101
CB3/NC8 105
CB4/NC2 88
CB5/NC1 87
CB6/NC5 100
CB7/NC7 104

C0/CS2#/NC9 162
C1/CS3#/NC10 165

RESET# 108 — DDR4_DRAMRST# (9)

ACT# 114 — M_A_ACTN (3)
ALERT# 116 — DDR0_A_ALERTN (3)
EVENT# 134

Parity 143 — DDR0_A_PARITY (3)

VSS-1 1
VSS-2 2
VSS-3 5
VSS-4 6
VSS-5 9
VSS-6 10
VSS-7 14
VSS-8 15
VSS-9 18
VSS-10 19
VSS-11 22
VSS-12 23
VSS-13 26
VSS-14 27
VSS-15 30
VSS-16 31
VSS-17 35
VSS-18 36
VSS-19 39
VSS-20 40
VSS-21 43
VSS-22 44
VSS-23 47
VSS-24 48
VSS-25 51
VSS-26 52
VSS-27 56
VSS-28 57
VSS-29 60
VSS-30 61
VSS-31 64
VSS-32 65
VSS-33 68
VSS-34 69
VSS-35 72
VSS-36 73
VSS-37 77
VSS-38 78
VSS-39 81
VSS-40 82
VSS-41 85
VSS-42 86
VSS-43 89
VSS-44 90
VSS-45 93
VSS-46 94
VSS-47 98
VSS-48 99
VSS-49 102
VSS-50 103
VSS-51 106
VSS-52 107

DDR4SODIMM-260PS_BLACK-HF-20
DDR4_SODIMM260P_H4_5
N13-2600220-L41

MICRO-STAR INT'L CO.,LTD.

Title: DDR4_SODIMM_A0
Size: Custom
Document Number: MS-16Q4
Rev: 10
Date: Monday, December 24, 2018
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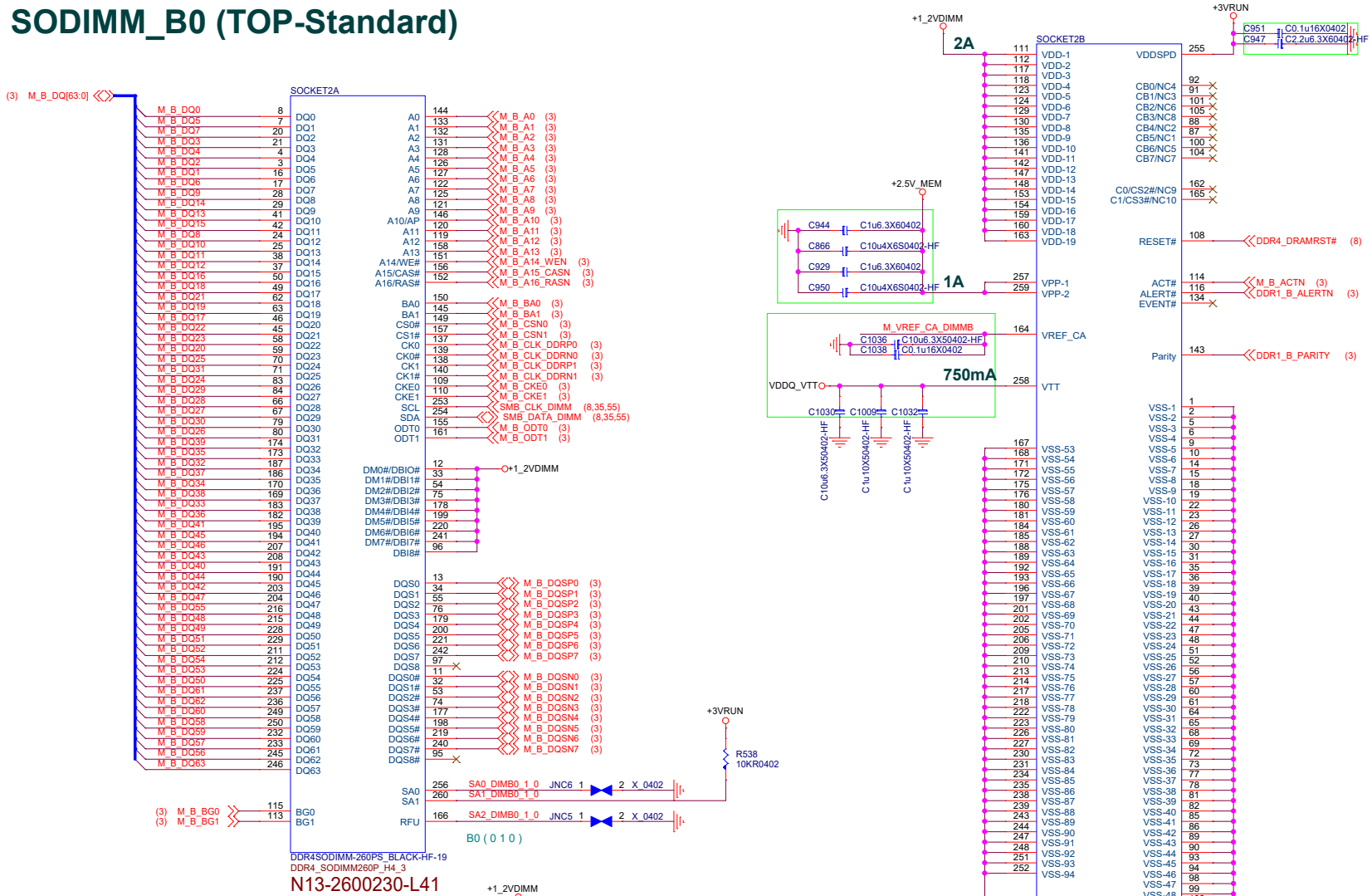
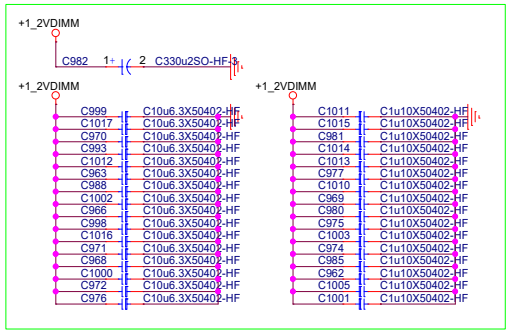
SODIMM_B0 (TOP-Standard)



20170912 C872 change to C71-33102AE-P01

ref DG/ Section 4.14.1

CFL-H DDR4 SDDIMM Power Plane Decoupling



MICRO-STAR INT'L CO.,LTD.

Title	DDR4_SODIMM_B0	
Size: Custom	Document Number: MS-16Q4	Rev: 10
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20181025

G100 G101

X_N18E-G2-A1 B03-TU10655-N08

X_N18E-G1-KD-A1 B03-TU10645-N08

3V3_NV

20180713 Follow design question

R383 10KR1%0402

G1A

BGA2228 COMMON

1/22 PCI_EXPRESS

(27,32) PEX_RST#

R438 100KR0402

GND

20180712

1V8_AON

R407 10KR0402

PEX_CLKREQ#

GC6_GPU_WAKE#

(32) GFX_REFCLK

(32) GFX_REFCLK#

PEX_WAKE BK44
PEX_RST BK26
PEX_CLKREQ BL26
PEX_REFCLK BM26
PEX_REFCLK BM27

(4) PEG_RXP15	C758 C0.22u16X0402-HF	PEG_C_TXP15_JNC	BG26	PEX_TX0
(4) PEG_RXN15	C755 C0.22u16X0402-HF	PEG_C_TXN15_JNC	BH26	PEX_TX0
(4) PEG_TXP15	C79 C0.22u16X0402-HF	PEG_C_RXP15_JNC	BL27	PEX_RX0
(4) PEG_TXN15	C78 C0.22u16X0402-HF	PEG_C_RXN15_JNC	BK27	PEX_RX0
(4) PEG_RXP14	C738 C0.22u16X0402-HF	PEG_C_TXP14_JNC	BF26	PEX_TX1
(4) PEG_RXN14	C725 C0.22u16X0402-HF	PEG_C_TXN14_JNC	BE26	PEX_TX1
(4) PEG_TXP14	C76 C0.22u16X0402-HF	PEG_C_RXP14_JNC	BG29	PEX_RX1
(4) PEG_TXN14	C77 C0.22u16X0402-HF	PEG_C_RXN14_JNC	BL29	PEX_RX1
(4) PEG_RXP13	C725 C0.22u16X0402-HF	PEG_C_TXP13_JNC	BF27	PEX_TX2
(4) PEG_RXN13	C716 C0.22u16X0402-HF	PEG_C_TXN13_JNC	BG27	PEX_TX2
(4) PEG_TXP13	C75 C0.22u16X0402-HF	PEG_C_RXP13_JNC	BM29	PEX_RX2
(4) PEG_TXN13	C74 C0.22u16X0402-HF	PEG_C_RXN13_JNC	BM30	PEX_RX2
(4) PEG_RXP12	C631 C0.22u16X0402-HF	PEG_C_TXP12_JNC	BG29	PEX_TX3
(4) PEG_RXN12	C620 C0.22u16X0402-HF	PEG_C_TXN12_JNC	BH29	PEX_TX3
(4) PEG_TXP12	C73 C0.22u16X0402-HF	PEG_C_RXP12_JNC	BL30	PEX_RX3
(4) PEG_TXN12	C72 C0.22u16X0402-HF	PEG_C_RXN12_JNC	BK30	PEX_RX3
(4) PEG_RXP11	C632 C0.22u16X0402-HF	PEG_C_TXP11_JNC	BF29	PEX_TX4
(4) PEG_RXN11	C619 C0.22u16X0402-HF	PEG_C_TXN11_JNC	BE29	PEX_TX4
(4) PEG_TXP11	C70 C0.22u16X0402-HF	PEG_C_RXP11_JNC	BK32	PEX_RX4
(4) PEG_TXN11	C71 C0.22u16X0402-HF	PEG_C_RXN11_JNC	BL32	PEX_RX4
(4) PEG_RXP10	C596 C0.22u16X0402-HF	PEG_C_TXP10_JNC	BF30	PEX_TX5
(4) PEG_RXN10	C587 C0.22u16X0402-HF	PEG_C_TXN10_JNC	BG30	PEX_TX5
(4) PEG_TXP10	C69 C0.22u16X0402-HF	PEG_C_RXP10_JNC	BM32	PEX_RX5
(4) PEG_TXN10	C68 C0.22u16X0402-HF	PEG_C_RXN10_JNC	BM33	PEX_RX5
(4) PEG_RXP9	C586 C0.22u16X0402-HF	PEG_C_TXP9_JNC	BG32	PEX_TX6
(4) PEG_RXN9	C563 C0.22u16X0402-HF	PEG_C_TXN9_JNC	BH32	PEX_TX6
(4) PEG_TXP9	C67 C0.22u16X0402-HF	PEG_C_RXP9_JNC	BL33	PEX_RX6
(4) PEG_TXN9	C64 C0.22u16X0402-HF	PEG_C_RXN9_JNC	BK33	PEX_RX6
(4) PEG_RXP8	C566 C0.22u16X0402-HF	PEG_C_TXP8_JNC	BF32	PEX_TX7
(4) PEG_RXN8	C561 C0.22u16X0402-HF	PEG_C_TXN8_JNC	BE32	PEX_TX7
(4) PEG_TXP8	C63 C0.22u16X0402-HF	PEG_C_RXP8_JNC	BM35	PEX_RX7
(4) PEG_TXN8	C62 C0.22u16X0402-HF	PEG_C_RXN8_JNC	BL35	PEX_RX7
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(4) PEG_RXN7	C559 C0.22u16X0402-HF	PEG_C_TXN7_JNC	BG33	PEX_TX8
(4) PEG_TXP7	C61 C0.22u16X0402-HF	PEG_C_RXP7_JNC	BM35	PEX_RX8
(4) PEG_TXN7	C60 C0.22u16X0402-HF	PEG_C_RXN7_JNC	BM36	PEX_RX8
(4) PEG_RXP6	C536 C0.22u16X0402-HF	PEG_C_TXP6_JNC	BG35	PEX_TX9
(4) PEG_RXN6	C548 C0.22u16X0402-HF	PEG_C_TXN6_JNC	BH35	PEX_TX9
(4) PEG_TXP6	C58 C0.22u16X0402-HF	PEG_C_RXP6_JNC	BL36	PEX_RX9
(4) PEG_TXN6	C59 C0.22u16X0402-HF	PEG_C_RXN6_JNC	BM36	PEX_RX9
(4) PEG_RXP5	C528 C0.22u16X0402-HF	PEG_C_TXP5_JNC	BF35	PEX_TX10
(4) PEG_RXN5	C531 C0.22u16X0402-HF	PEG_C_TXN5_JNC	BE35	PEX_TX10
(4) PEG_TXP5	C57 C0.22u16X0402-HF	PEG_C_RXP5_JNC	BK38	PEX_RX10
(4) PEG_TXN5	C56 C0.22u16X0402-HF	PEG_C_RXN5_JNC	BL38	PEX_RX10
(4) PEG_RXP4	C523 C0.22u16X0402-HF	PEG_C_TXP4_JNC	BF36	PEX_TX11
(4) PEG_RXN4	C526 C0.22u16X0402-HF	PEG_C_TXN4_JNC	BG36	PEX_TX11
(4) PEG_TXP4	C54 C0.22u16X0402-HF	PEG_C_RXP4_JNC	BM38	PEX_RX11
(4) PEG_TXN4	C55 C0.22u16X0402-HF	PEG_C_RXN4_JNC	BM39	PEX_RX11
(4) PEG_RXP3	C507 C0.22u16X0402-HF	PEG_C_TXP3_JNC	BG38	PEX_TX12
(4) PEG_RXN3	C521 C0.22u16X0402-HF	PEG_C_TXN3_JNC	BH38	PEX_TX12
(4) PEG_TXP3	C53 C0.22u16X0402-HF	PEG_C_RXP3_JNC	BL39	PEX_RX12
(4) PEG_TXN3	C52 C0.22u16X0402-HF	PEG_C_RXN3_JNC	BK39	PEX_RX12
(4) PEG_RXP2	C491 C0.22u16X0402-HF	PEG_C_TXP2_JNC	BF38	PEX_TX13
(4) PEG_RXN2	C506 C0.22u16X0402-HF	PEG_C_TXN2_JNC	BE38	PEX_TX13
(4) PEG_TXP2	C50 C0.22u16X0402-HF	PEG_C_RXP2_JNC	BK41	PEX_RX13
(4) PEG_TXN2	C51 C0.22u16X0402-HF	PEG_C_RXN2_JNC	BL41	PEX_RX13
(4) PEG_RXP1	C459 C0.22u16X0402-HF	PEG_C_TXP1_JNC	BF39	PEX_TX14
(4) PEG_RXN1	C490 C0.22u16X0402-HF	PEG_C_TXN1_JNC	BG39	PEX_TX14
(4) PEG_TXP1	C49 C0.22u16X0402-HF	PEG_C_RXP1_JNC	BM41	PEX_RX14
(4) PEG_TXN1	C48 C0.22u16X0402-HF	PEG_C_RXN1_JNC	BM42	PEX_RX14
(4) PEG_RXP0	C451 C0.22u16X0402-HF	PEG_C_TXP0_JNC	BH41	PEX_TX15
(4) PEG_RXN0	C457 C0.22u16X0402-HF	PEG_C_TXN0_JNC	BG41	PEX_TX15
(4) PEG_TXP0	C46 C0.22u16X0402-HF	PEG_C_RXP0_JNC	BL42	PEX_RX15
(4) PEG_TXN0	C47 C0.22u16X0402-HF	PEG_C_RXN0_JNC	BK42	PEX_RX15

N18E-G3-A1 B03-TU10455-N08

Place under GPU

GPU and PS

PEX_DVDD BB35, BB36, BC35, BC36, BD33, BD36
PEX_CVDD BB33, BC33
PEX_HVDD BB26, BB27, BB29, BB32, BC26, BC27, BC29, BC30, BC32, BD27, BD30
PEX_PLL_HVDD BB30

PEX_VDD

C896 C0.47u4X6S0201-HF, C1057 C0.47u4X6S0201-HF, C916 C0.47u4X6S0201-HF, C801 C0.47u4X6S0201-HF, C146 C4.7u6.3X6S0603, C907 C4.7u6.3X6S0603, C90 C10u4X6S0402-HF, C89 C10u4X6S0402-HF
C943 C0.47u4X6S0201-HF, C878 C0.47u4X6S0201-HF, C827 C0.47u4X6S0201-HF, C857 C0.47u4X6S0201-HF, C839 C4.7u6.3X6S0603, C91 C10u4X6S0402-HF, C719 C22u4X60603, C720 C22u4X60603
C808 C0.47u4X6S0201-HF, C840 C0.47u4X6S0201-HF, C802 C0.47u4X6S0201-HF, C856 C0.47u4X6S0201-HF
C807 C0.47u4X6S0201-HF, C93 C0.47u4X6S0201-HF, C1061 C0.47u4X6S0201-HF, C1044 C0.47u4X6S0201-HF
1V8_MAIN
C1276 C0.47u4X6S0201-HF, C1291 C0.47u4X6S0201-HF, C1318 C0.47u4X6S0201-HF, C1585 C4.7u6.3X6S0603, C1337 C4.7u6.3X6S0603, C1295 C10u4X6S0402-HF, C1589 C22u4X60603, C1590 C22u4X60603
C1278 C0.47u4X6S0201-HF, C1302 C0.47u4X6S0201-HF, C1328 C0.47u4X6S0201-HF, C1594 C4.7u6.3X6S0603, C1261 X_C0.47u4X6S0201-HF, C1573 C10u4X6S0402-HF, C1574 C10u4X6S0402-HF, C1588 X_C22u4X60603
C1340 C0.47u4X6S0201-HF, C1311 C0.47u4X6S0201-HF, C1348 C0.47u4X6S0201-HF
C1250 C0.47u4X6S0201-HF, C1268 C0.47u4X6S0201-HF, C1563 C0.47u4X6S0201-HF
GND

PEX_TERMP BL44 PEX_TERMP R384 2.49KR1%0402 GND

GPU CLK REQ#

GPU_CLKREQ# (32)

1V8_MAINO

Q45 N-BSS138LT1G_SOT23-3-RH

C756 C0.01u50X0402

GND

PEX_CLKREQ#

20160616A Delete Q1,R26
20160826 Modify Q21 gate signal from DGPU_PWRGD to 1V8_MAIN & Add C763 0.01uF

20160905A Change Q21 PN from D03-0341409-A68 to D03-0013829-005

Title	DGPU_PCI-E Host		
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G1B
?
BGA2228
COMMON
2/22 FBA

G1C
?
BGA2228
COMMON
3/22 FBB

FBVDDQ
R379 10KR1%0402
R313 10KR1%0402
FBA_CMD<10>
FBA_CMD<26>
FBA_CMD<2>
FBA_CMD<18>
R24 10KR1%0402
R26 10KR1%0402
GND

FBVDDQ
R392 10KR1%0402
R310 10KR1%0402
FBB_CMD<10>
FBB_CMD<26>
FBB_CMD<2>
FBB_CMD<18>
R27 10KR1%0402
R29 10KR1%0402
GND

NO stuffed
FBVDDQ
R382 X 60.4R1%0402
R381 X 60.4R1%0402
FBA_DEBUG1
20180713
Follow design question

FBVDDQ
R400 X 60.4R1%0402
R385 X 60.4R1%0402
FBB_DEBUG1
20180713
Follow design question

GDDR6 CMD Mapping

	Lower 0..31 DRAM1 CHA-Byte 0,1	x16 Mode Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

W> 12mils
PLACE AT BALLS
W> 16mils, 0.5A
PLACE AT BALLS
Place near GPU
1V8_MAIN
LB1 30L2A-50_0402-RH
C1572 C22u4X60603
C1561 C4.7u6.3X6S0603
C1557 C4.7u6.3X6S0603
C769 C0.47u4X6S0201-HF
C1265 C0.47u4X6S0201-HF
C767 C0.47u4X6S0201-HF
C826 C0.47u4X6S0201-HF

Title	DGPU_MEM IF A/B
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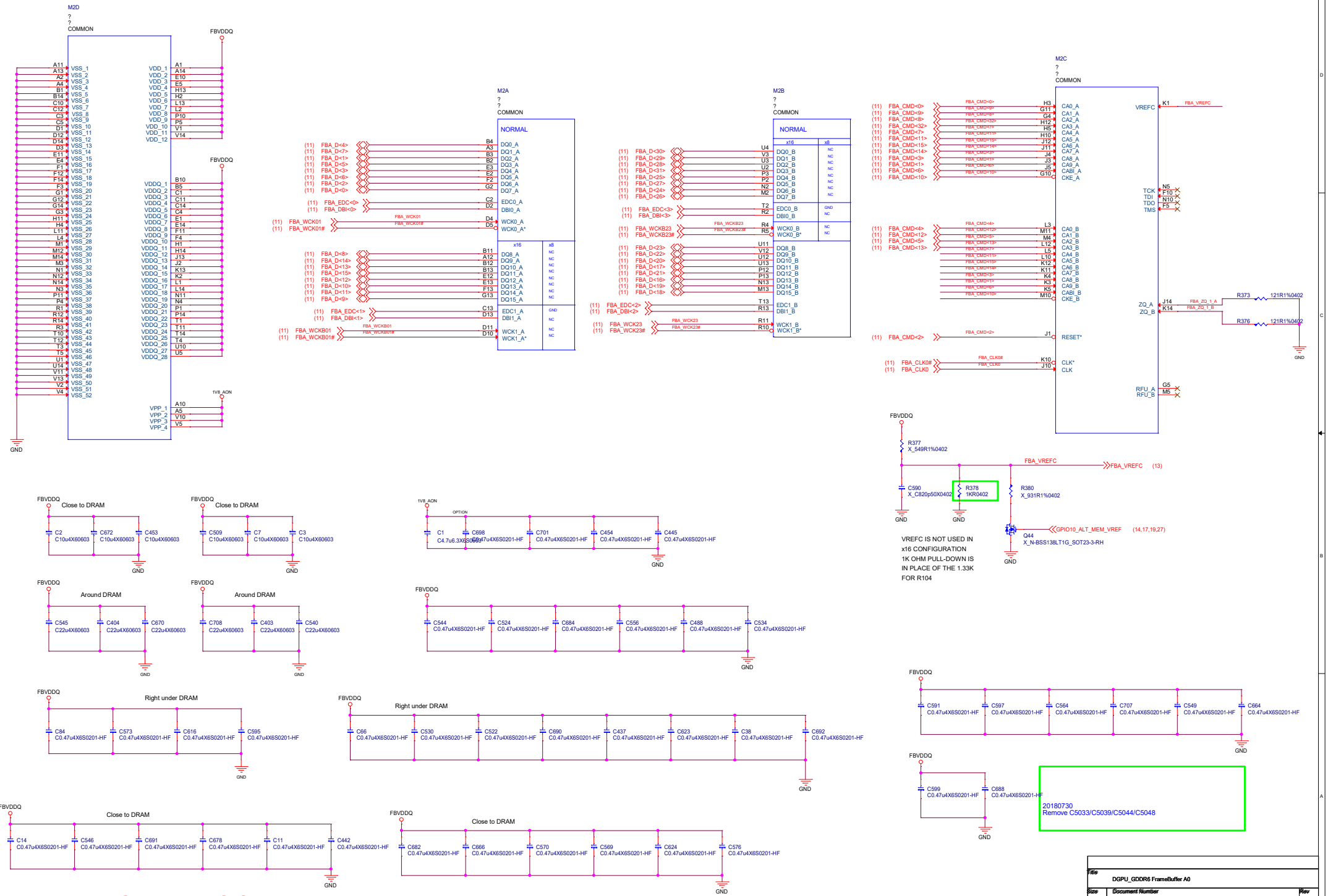

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Size	Document Number	Rev
Custom	MS-16Q4	10
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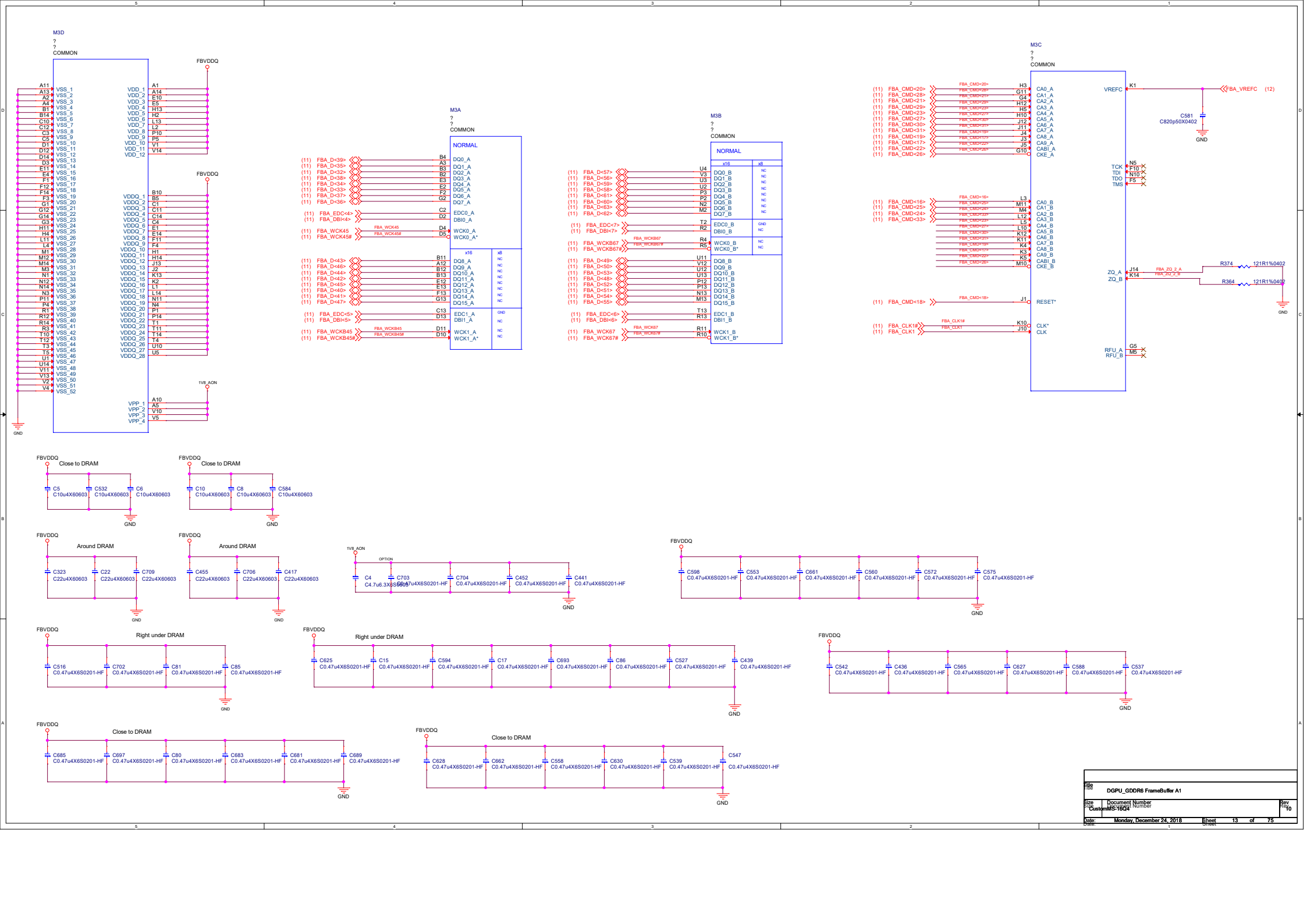
M3D
COMMON
M3A
COMMON
NORMAL
M3B
COMMON
NORMAL
M3C
COMMON
FBVDDQ
1V8_AON
GND
Close to DRAM
Around DRAM
Right under DRAM
Close to DRAM
Right under DRAM
Close to DRAM
C5 C10u4X60603
C532 C10u4X60603
C6 C10u4X60603
C10 C10u4X60603
C8 C10u4X60603
C584 C10u4X60603
C323 C22u4X60603
C22 C22u4X60603
C709 C22u4X60603
C455 C22u4X60603
C706 C22u4X60603
C417 C22u4X60603
C4 C4.7u6.3X5S60603
C703 C0.47u4X6S0201-HF
C704 C0.47u4X6S0201-HF
C452 C0.47u4X6S0201-HF
C441 C0.47u4X6S0201-HF
C598 C0.47u4X6S0201-HF
C553 C0.47u4X6S0201-HF
C661 C0.47u4X6S0201-HF
C560 C0.47u4X6S0201-HF
C572 C0.47u4X6S0201-HF
C575 C0.47u4X6S0201-HF
C516 C0.47u4X6S0201-HF
C702 C0.47u4X6S0201-HF
C81 C0.47u4X6S0201-HF
C85 C0.47u4X6S0201-HF
C625 C0.47u4X6S0201-HF
C15 C0.47u4X6S0201-HF
C594 C0.47u4X6S0201-HF
C17 C0.47u4X6S0201-HF
C693 C0.47u4X6S0201-HF
C86 C0.47u4X6S0201-HF
C527 C0.47u4X6S0201-HF
C439 C0.47u4X6S0201-HF
C542 C0.47u4X6S0201-HF
C436 C0.47u4X6S0201-HF
C565 C0.47u4X6S0201-HF
C627 C0.47u4X6S0201-HF
C588 C0.47u4X6S0201-HF
C537 C0.47u4X6S0201-HF
C685 C0.47u4X6S0201-HF
C697 C0.47u4X6S0201-HF
C80 C0.47u4X6S0201-HF
C683 C0.47u4X6S0201-HF
C681 C0.47u4X6S0201-HF
C689 C0.47u4X6S0201-HF
C628 C0.47u4X6S0201-HF
C662 C0.47u4X6S0201-HF
C558 C0.47u4X6S0201-HF
C630 C0.47u4X6S0201-HF
C539 C0.47u4X6S0201-HF
C547 C0.47u4X6S0201-HF
C581 C820p50X0402
R374 121R1%0402
R364 121R1%0402
FBA_VREFC (12)
Title: DGPU_GDDR6 FrameBuffer A1
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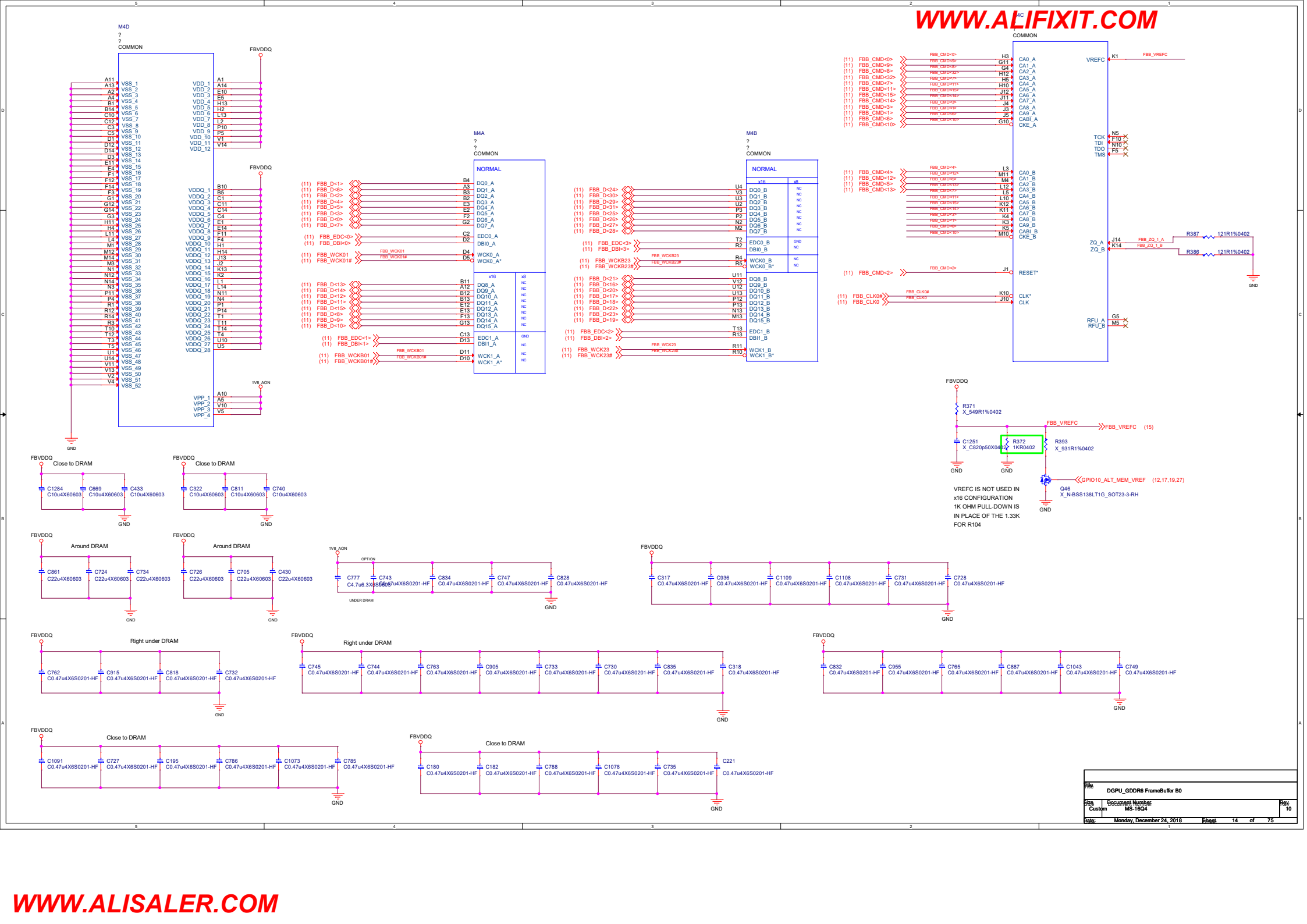

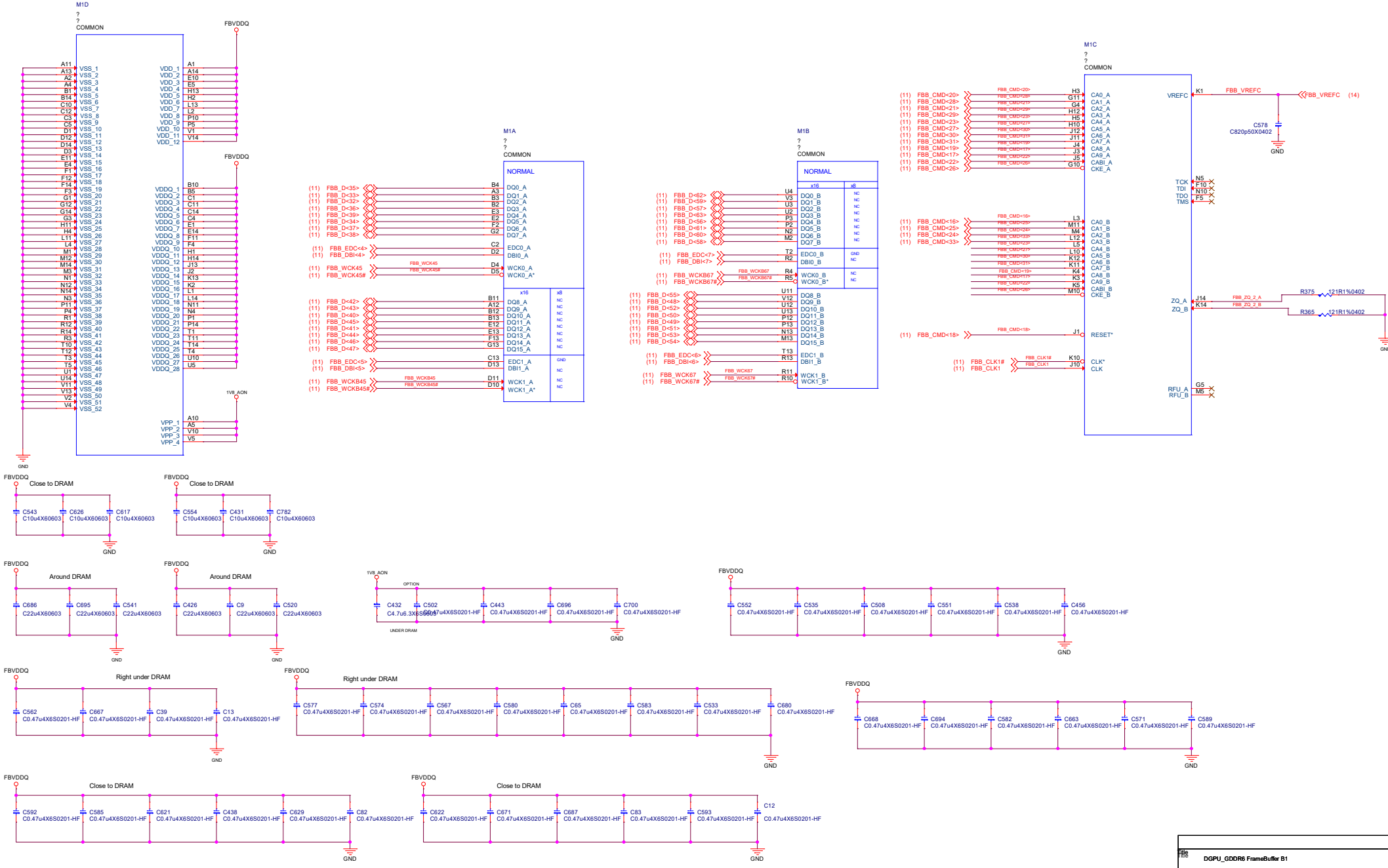
M1D
COMMON
FBVDDQ
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12
VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12 VDDQ_13 VDDQ_14 VDDQ_15 VDDQ_16 VDDQ_17 VDDQ_18 VDDQ_19 VDDQ_20 VDDQ_21 VDDQ_22 VDDQ_23 VDDQ_24 VDDQ_25 VDDQ_26 VDDQ_27 VDDQ_28
1V8_AON
VPP_1 VPP_2 VPP_3 VPP_4
GND
M1A
COMMON
NORMAL
x16 x8
DQ0_A DQ1_A DQ2_A DQ3_A DQ4_A DQ5_A DQ6_A DQ7_A
EDC0_A DBI0_A
WCK0_A WCK0_A*
DQ8_A DQ9_A DQ10_A DQ11_A DQ12_A DQ13_A DQ14_A DQ15_A
EDC1_A DBI1_A
WCK1_A WCK1_A*
M1B
COMMON
NORMAL
DQ0_B DQ1_B DQ2_B DQ3_B DQ4_B DQ5_B DQ6_B DQ7_B
EDC0_B DBI0_B
WCK0_B WCK0_B*
DQ8_B DQ9_B DQ10_B DQ11_B DQ12_B DQ13_B DQ14_B DQ15_B
EDC1_B DBI1_B
WCK1_B WCK1_B*
M1C
COMMON
CA0_A CA1_A CA2_A CA3_A CA4_A CA5_A CA6_A CA7_A CA8_A CA9_A CABI_A CKE_A
CA0_B CA1_B CA2_B CA3_B CA4_B CA5_B CA6_B CA7_B CA8_B CA9_B CABI_B CKE_B
RESET*
CLK* CLK
VREFC
TCK TDI TDO TMS
ZQ_A ZQ_B
RFU_A RFU_B
FBB_VREFC
C578 C820p50X0402
R375 121R1%0402
R365 121R1%0402
Close to DRAM
C543 C626 C617 C554 C431 C782 C10u4X60603
Around DRAM
C686 C695 C541 C426 C9 C520 C22u4X60603
OPTION
UNDER DRAM
C432 C4.7u6.3X6S0603 C502 C443 C696 C700 C552 C535 C508 C551 C538 C456 C0.47u4X6S0201-HF
Right under DRAM
C562 C667 C39 C13 C577 C574 C567 C580 C65 C583 C533 C680 C668 C694 C582 C663 C571 C589
C592 C585 C621 C438 C629 C82 C622 C671 C687 C83 C593 C12
Title
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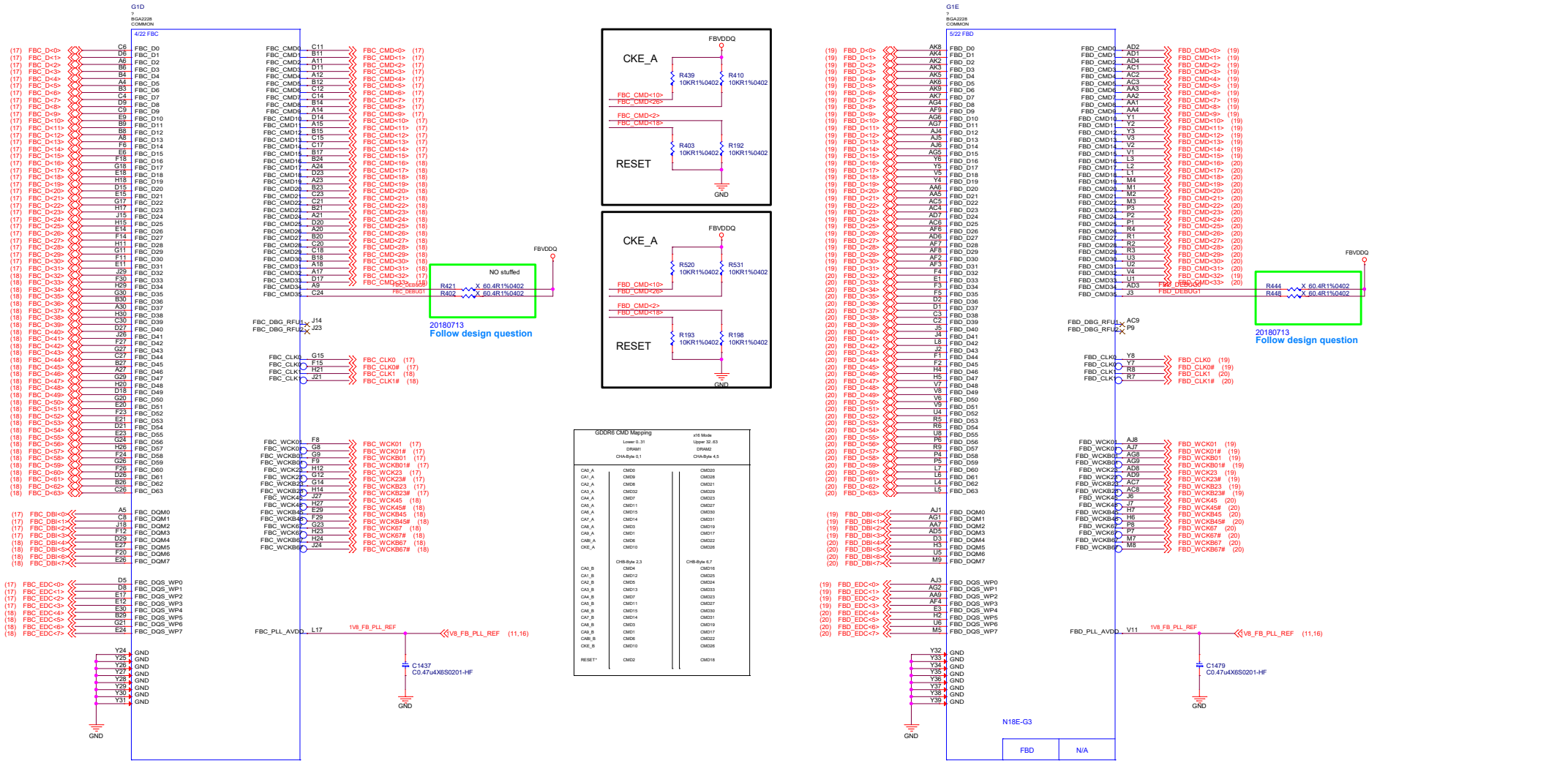

Title	DGPU_MEM IF C/D
Size	CustomMS-16O4
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Date	Monday, December 24, 2018
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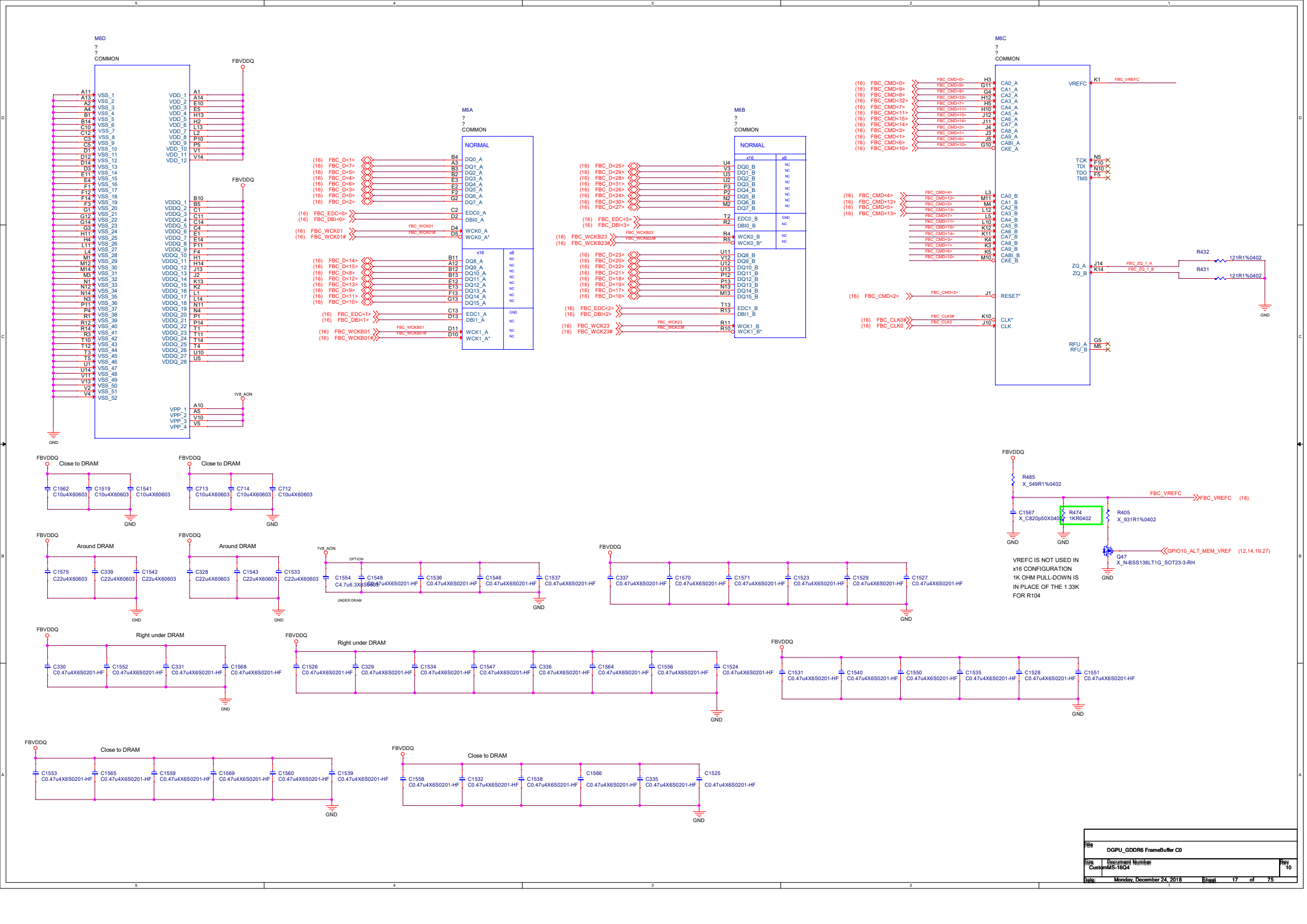
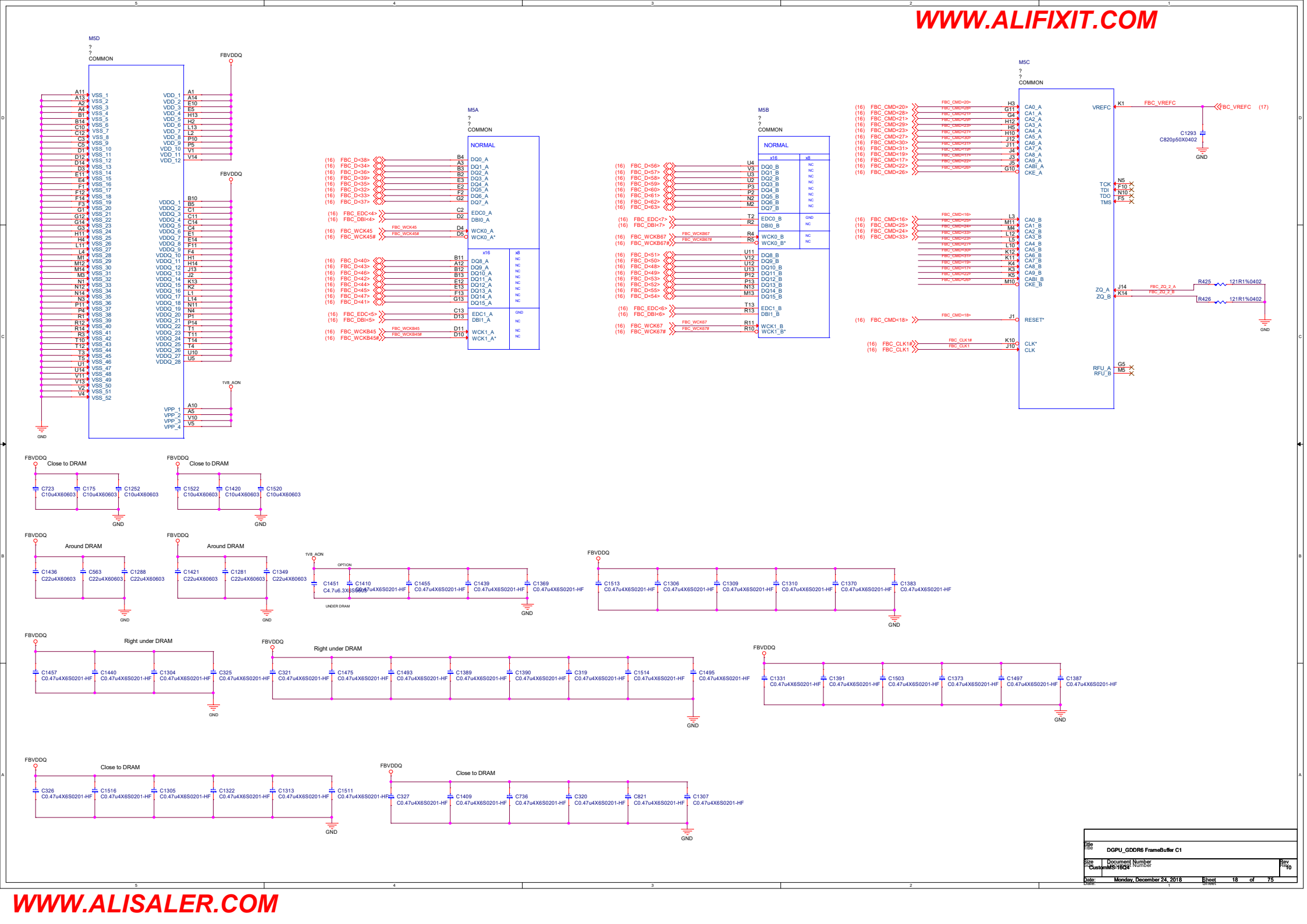
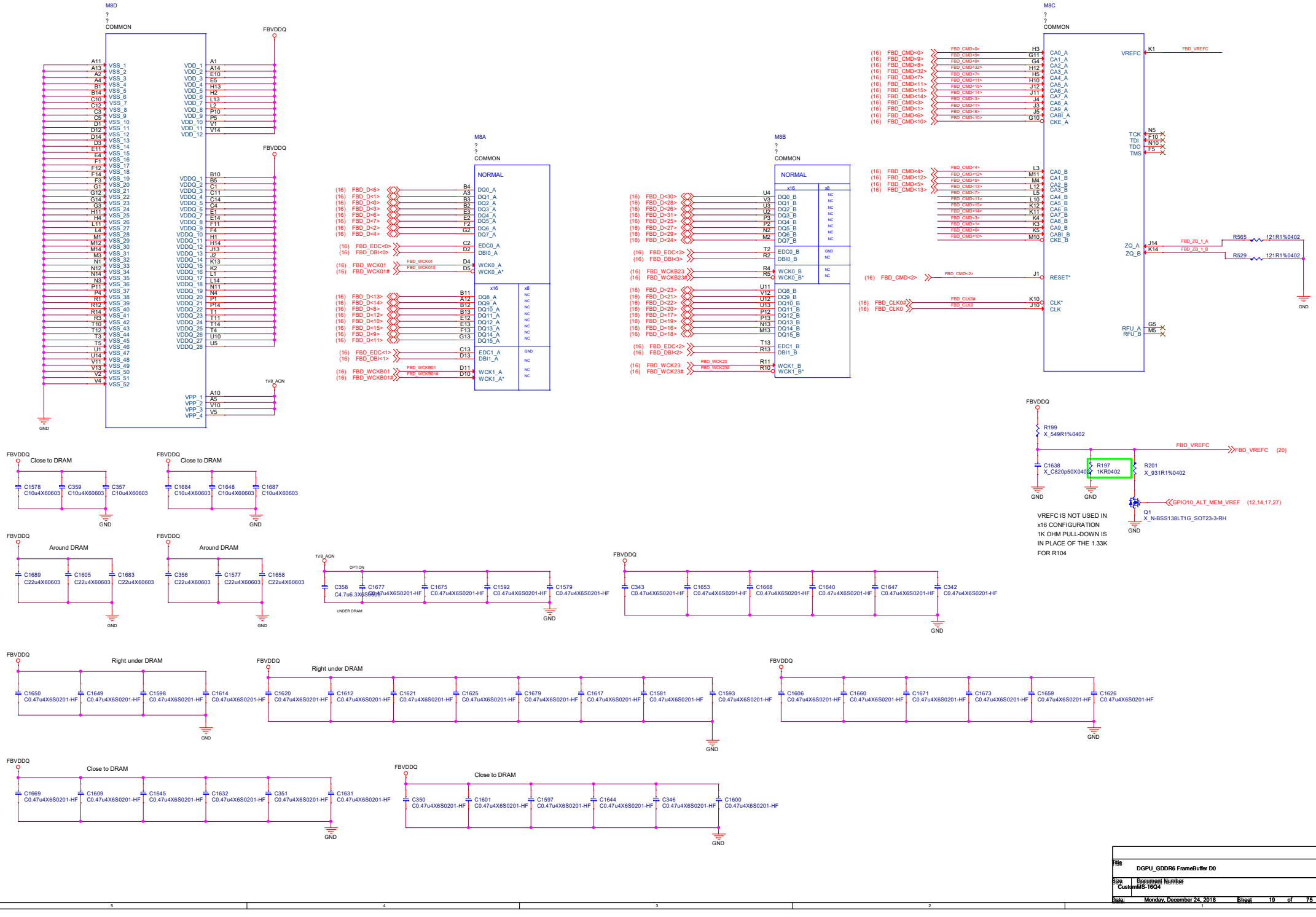

M6D
COMMON
M6A
NORMAL
M6B
NORMAL
M6C
COMMON
FBVDDQ
1V8_AON
GND
Close to DRAM
Around DRAM
Right under DRAM
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104
DGPU_GDDR6 FrameBuffer C0
Monday, December 24, 2018




M8D
COMMON
FBVDDQ
1V8_AON
GND
M8A
NORMAL
M8B
NORMAL
M8C
COMMON
VREFC
FBD_VREFC
TCK
TDI
TDO
TMS
ZQ_A
ZQ_B
R565 121R1%0402
R529 121R1%0402
RESET*
CLK*
RFU_A
RFU_B
R199 X_549R1%0402
R197 1KR0402
R201 X_931R1%0402
C1638 X_C820p50X0402
Q1 X_N-BSS138LT1G_SOT23-3-RH
GPIO10_ALT_MEM_VREF (12,14,17,27)
VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R104
Close to DRAM
Around DRAM
Right under DRAM
OPTION
UNDER DRAM
DGPU_GDDR6 FrameBuffer D0
Custom
MS-16G4
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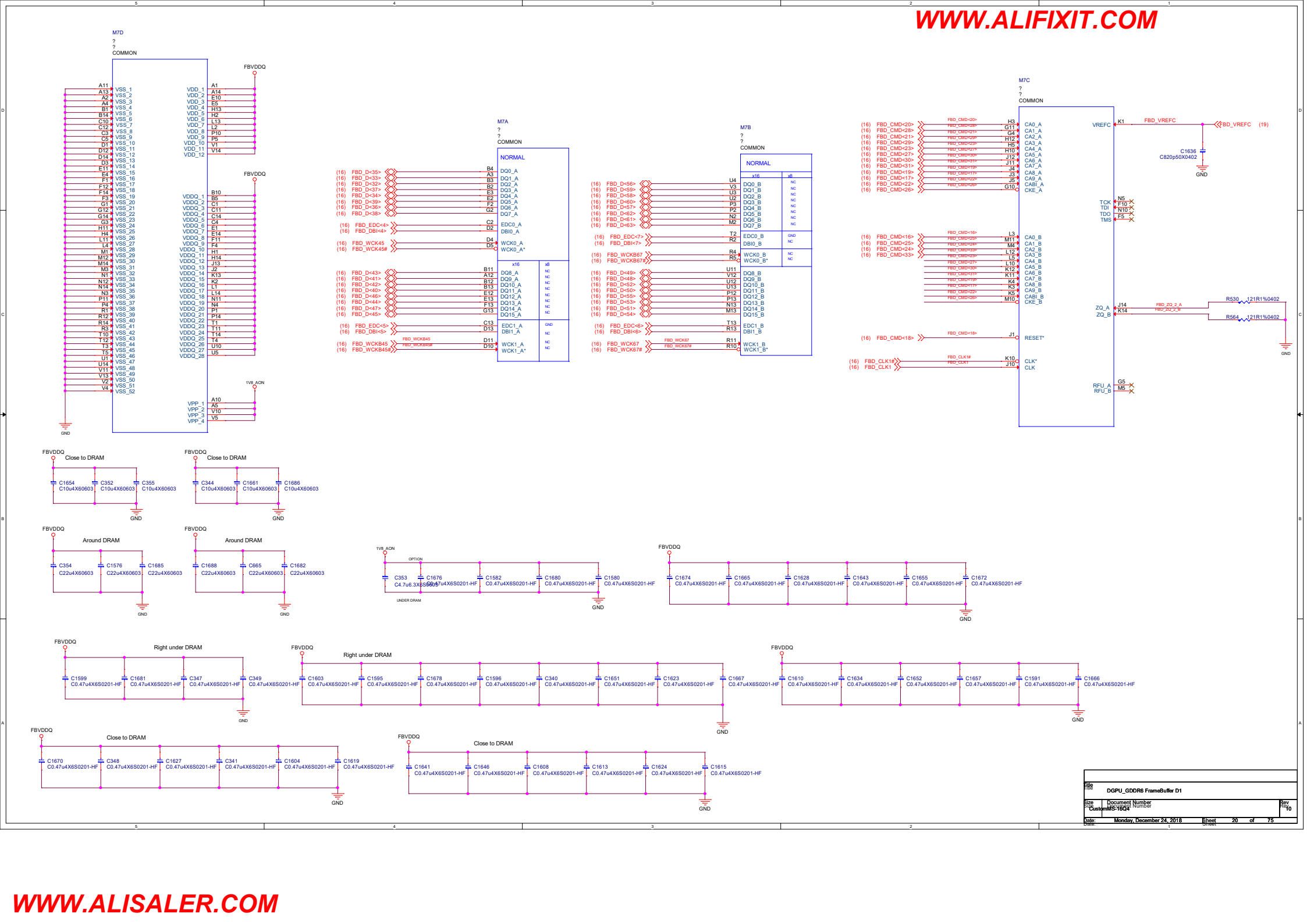

Title	DGPU_GDDR6 FrameBuffer D1
Size	Custom
Document Number	MS-16C4
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Date:	Monday, December 24, 2018
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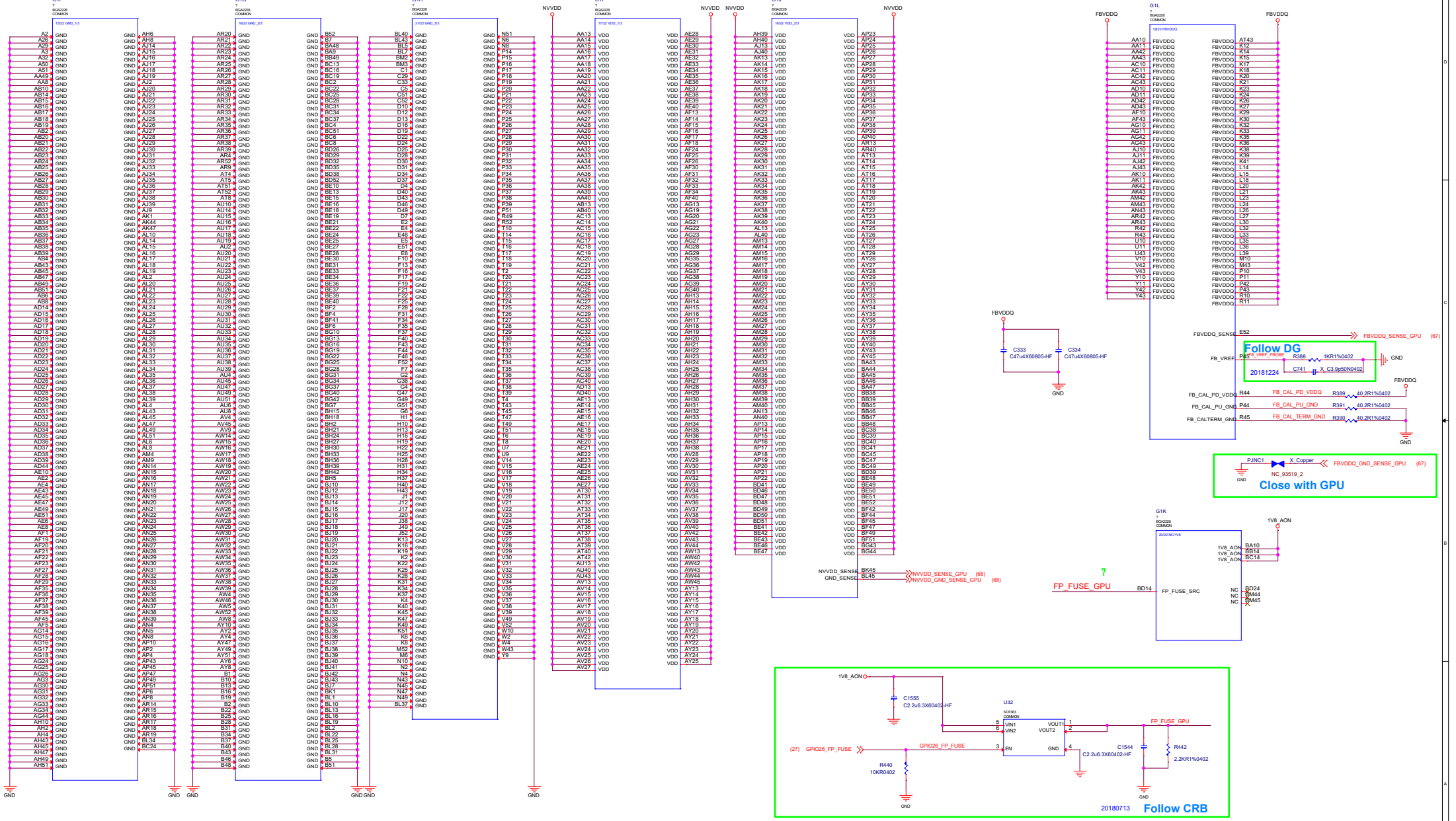
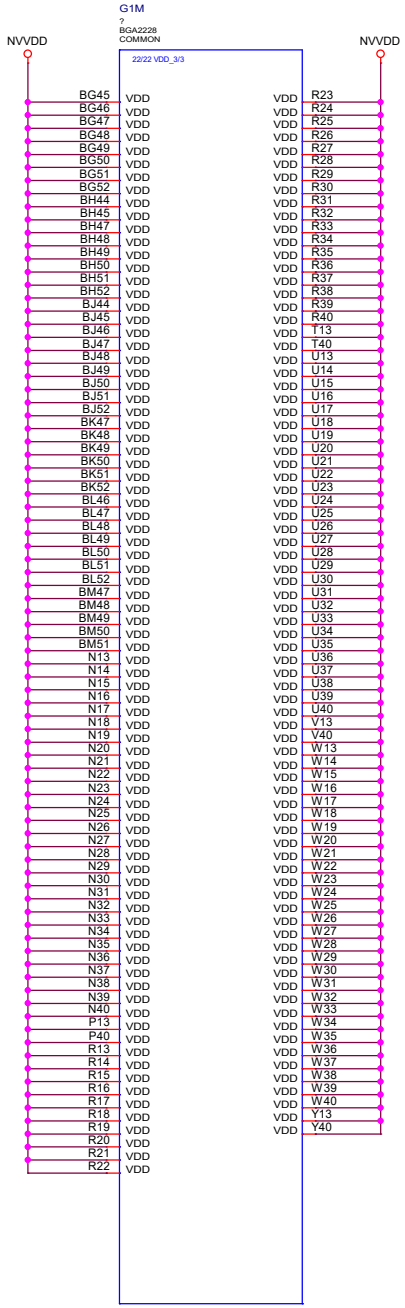

G1F
G1G
G1H
G1I
G1J
G1L
G1K
NVVDD
FBVDDQ
1V8_AON
GND
NVVDD_SENSE_GPU (68)
NVVDD_GND_SENSE_GPU (68)
FBVDDQ_SENSE_GPU (67)
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FBVDDQ_GND_SENSE_GPU (67)
FP_FUSE_GPU
GPIO26_FP_FUSE
Follow DG
20181224
Close with GPU
Follow CRB
20180713
GPU PWR AND GND
Monday, December 24, 2018

GPU PWR GND NCs



Title:	GPU PWR AND GND	
Size: Custom	Document Number: MS-16Q4	Rev: 10
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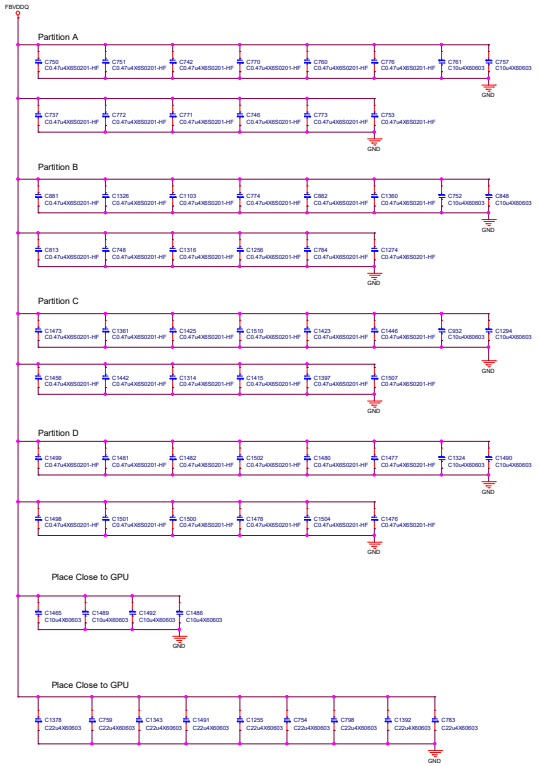
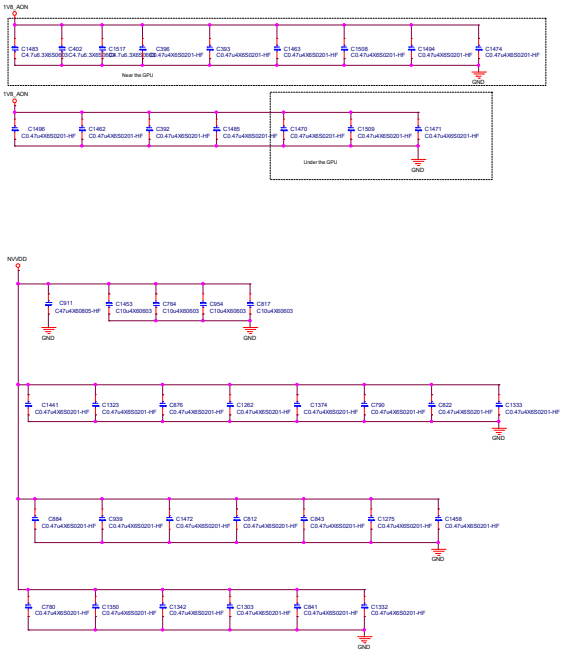
GPU DECOUPLING A

FBVDDQ_GPU



NVVDD

1V8_AON



Title	DGPU_GPU DECOUPLING A
Size	Document Number: MS-16Q4
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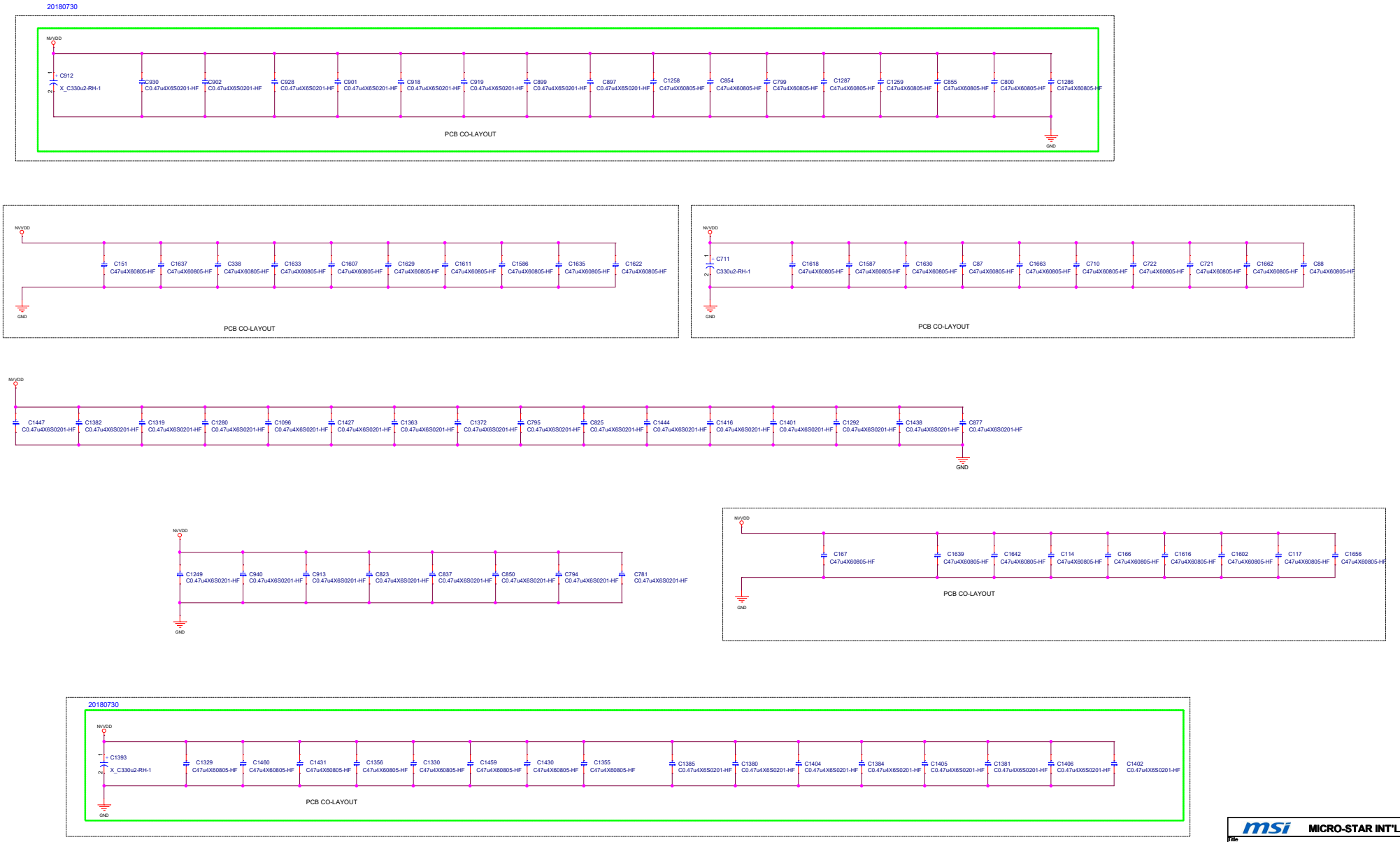
MICRO-STAR INT'L CO.,LTD.

GPU DECOUPLING B

GPU Decoupling



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU GPU DECOUPLING B	
Size: Custom	Document Number: MS-16Q4	Rev: 10
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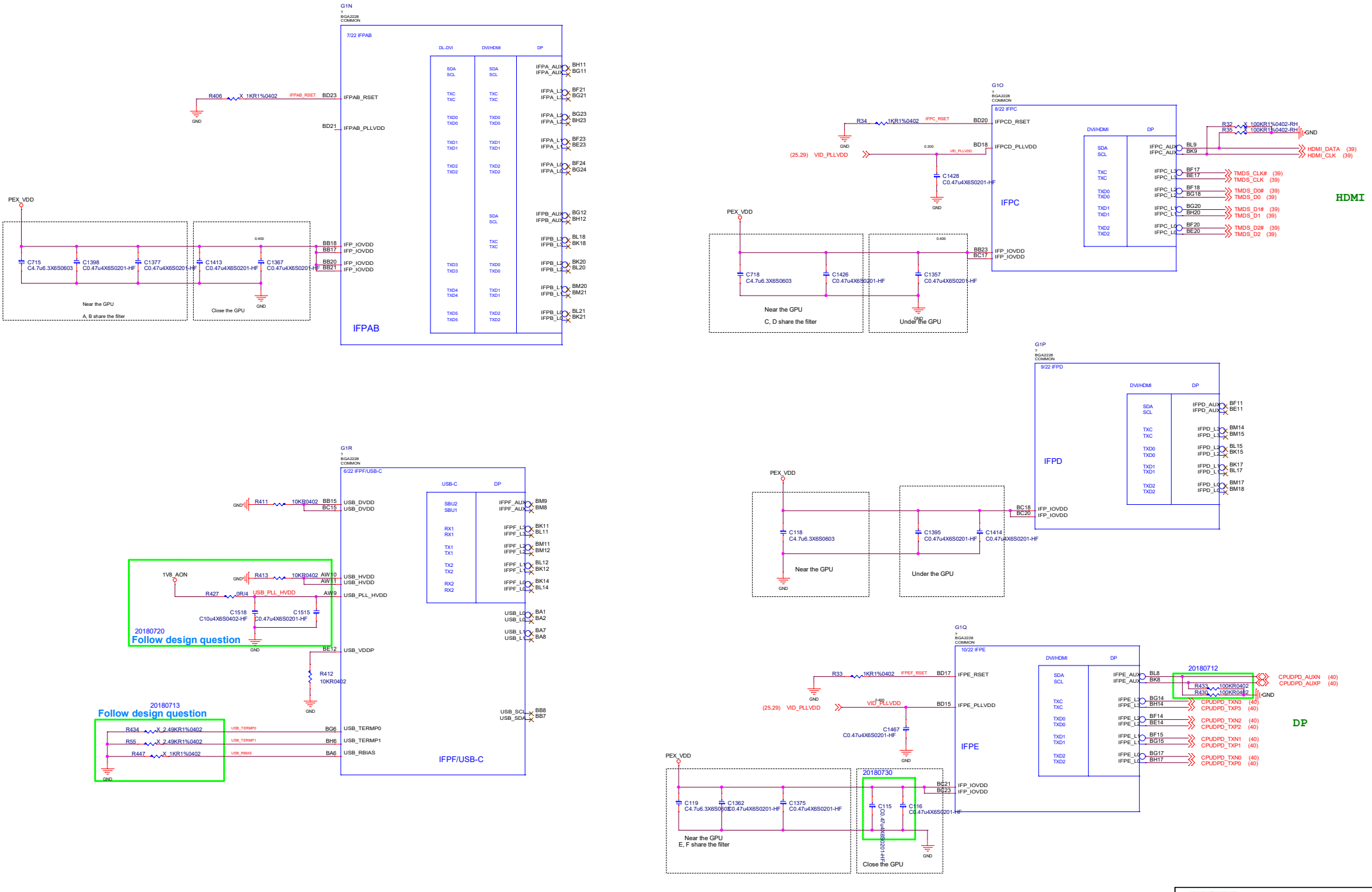
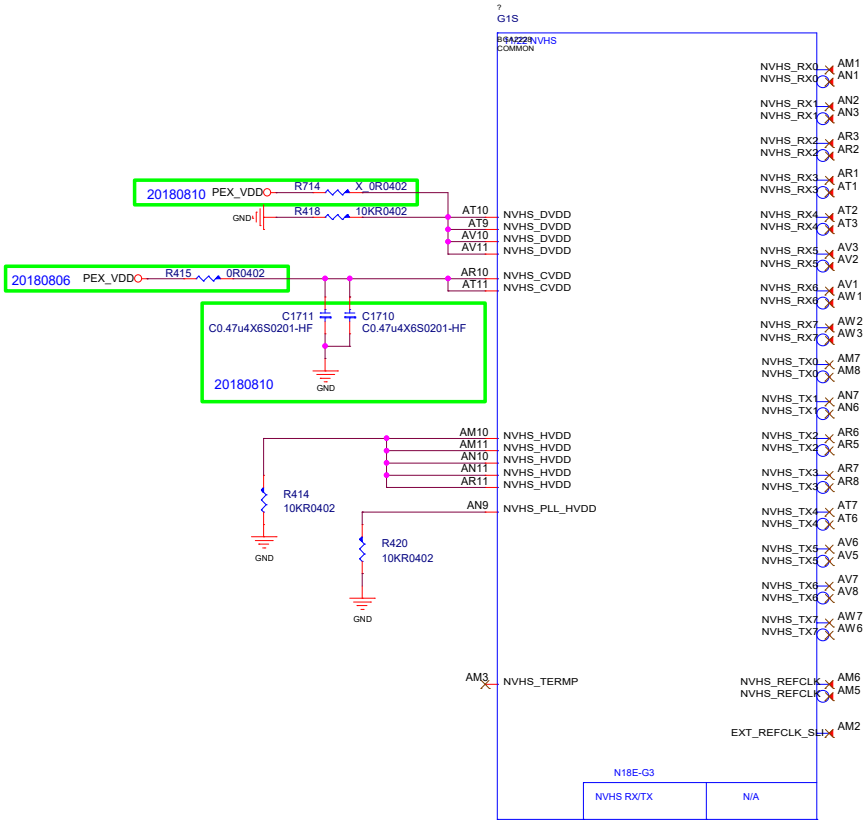
DACA,Display IF



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_DACA,Display IF		
Size A2	Document Number MS-16Q4		Rev 10
Date: Monday, December 24, 2018		Sheet 25 of 75	



Title	GPU_ NVLink & Framelock	
Size: Custom	Document Number: MS-16Q4	Rev: 10
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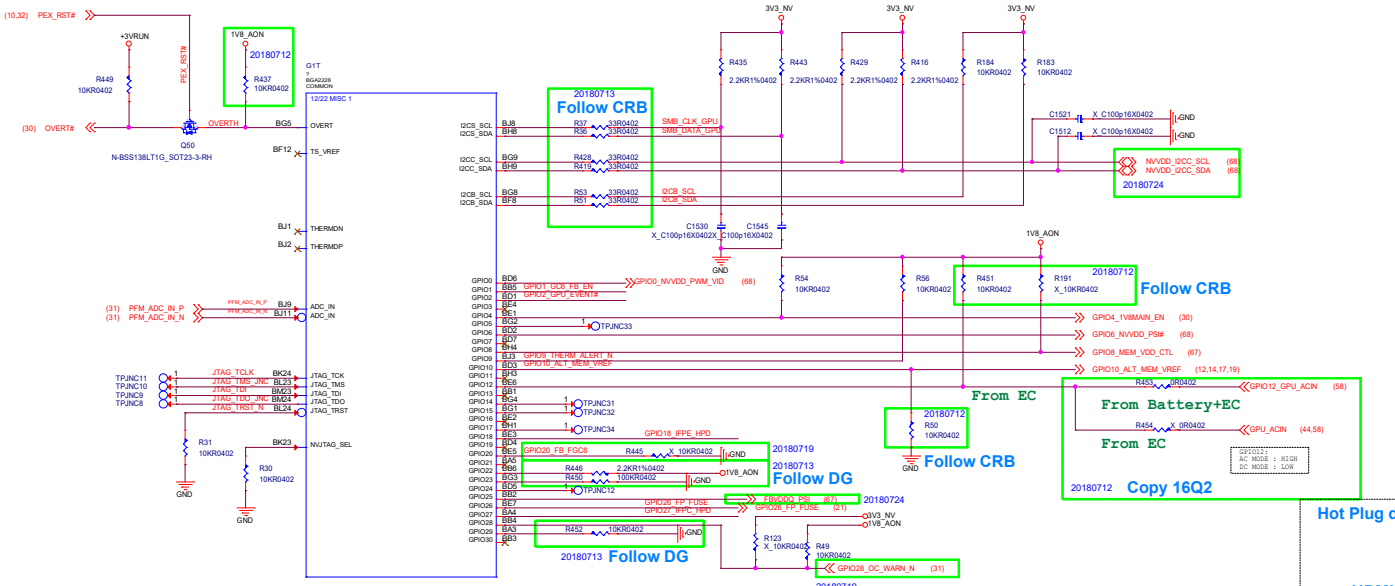

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	**NVDD_PWM_VID**	O	PWM Output to control NVVDD	0 to 1V8 PWM output (No Pull Up or Down)
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	**UNUSED**	O		
GPIO4	**1V8_MAIN_EN**	O	GPU POWER Sequencing for GC6 2.1	10K pull-up to 1V8 _AON
GPIO5	**FRAME_LOCK**	I	Active low Frame Lock	10K pull-up to 1V8 _AON
GPIO6	**NVDD_PSI**	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	O	LCD Panel Backlight PWM	100K pull-down
GPIO8	**MEM_VDD_CTL**	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	10K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	10K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K pull-up to 1V8_AON
GPIO13	**UNUSED**	O		
GPIO14	**HPD_IFPA**	I	Hot Plug Detect for IFPA	10K pull-up to 1V8_AON
GPIO15	**HPD_IFPB**	I	Hot Plug Detect for IFPB	10K pull-up to 1V8_AON
GPIO16	**UNUSED**	O		
GPIO17	**HPD_IFPD**	I	Hot Plug Detect for IFPD	10K pull-up to 1V8_AON
GPIO18	**HPD_IFPE**	I	Hot Plug Detect for IFPE	10K pull-up to 1V8_AON
GPIO19	**Reserved**	O		
GPIO20	**NB_FGC6**			10K pull-down
GPIO21	**LCD_BLEN**		**LCD Panel Backlight Enable**	100K pull-down
GPIO22	**SWAPRDY_IN**			2.2K pull-up to 1V8_AON
GPIO23	**RASTER_SYNC1**			100K pull-down
GPIO24	**HPD_IFPF/USBC_HPD or DONGLE_DET**	I	**Hot Plug Detect for IFPF or USBC**	10K pull-up to 1V8_AON
GPIO25	**FBVDD_PSI**	O		
GPIO26	**FP_FUSE**			10K pull-down
GPIO27	**HPD_IFPC**	I	Hot Plug Detect for IFPC	10K pull-up to 1V8_AON
GPIO28	**INA_HT/ADC_MUX_SEL**			10K pull-up
GPIO29	**IDLE_IN_SW**	I		10K pull-down
GPIO30	**UNUSED**			

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPIO,I2C

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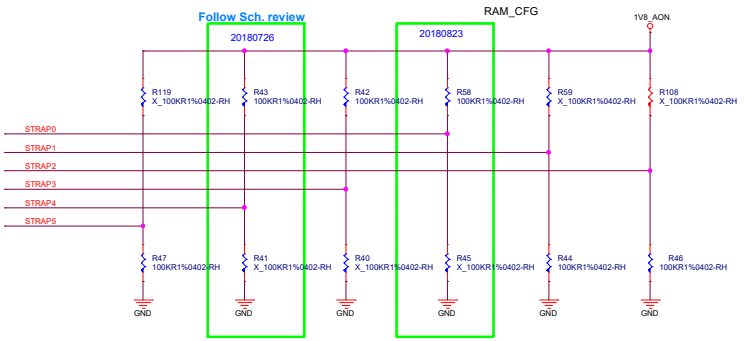
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	DEFAULT
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Hynix
00111	16Gb	256-bit	Samsung
01000	16Gb	256-bit	Micron



ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

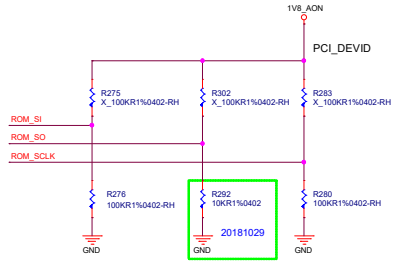
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

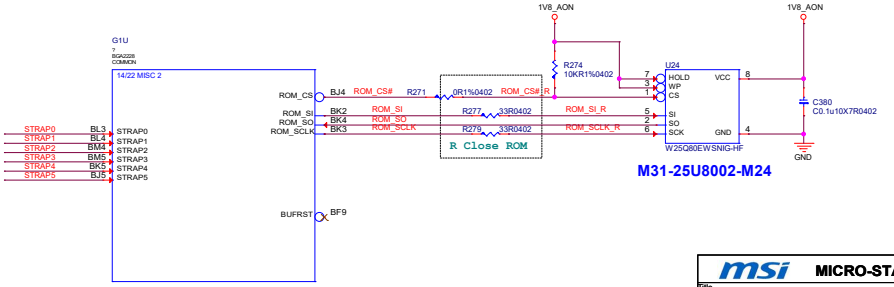
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

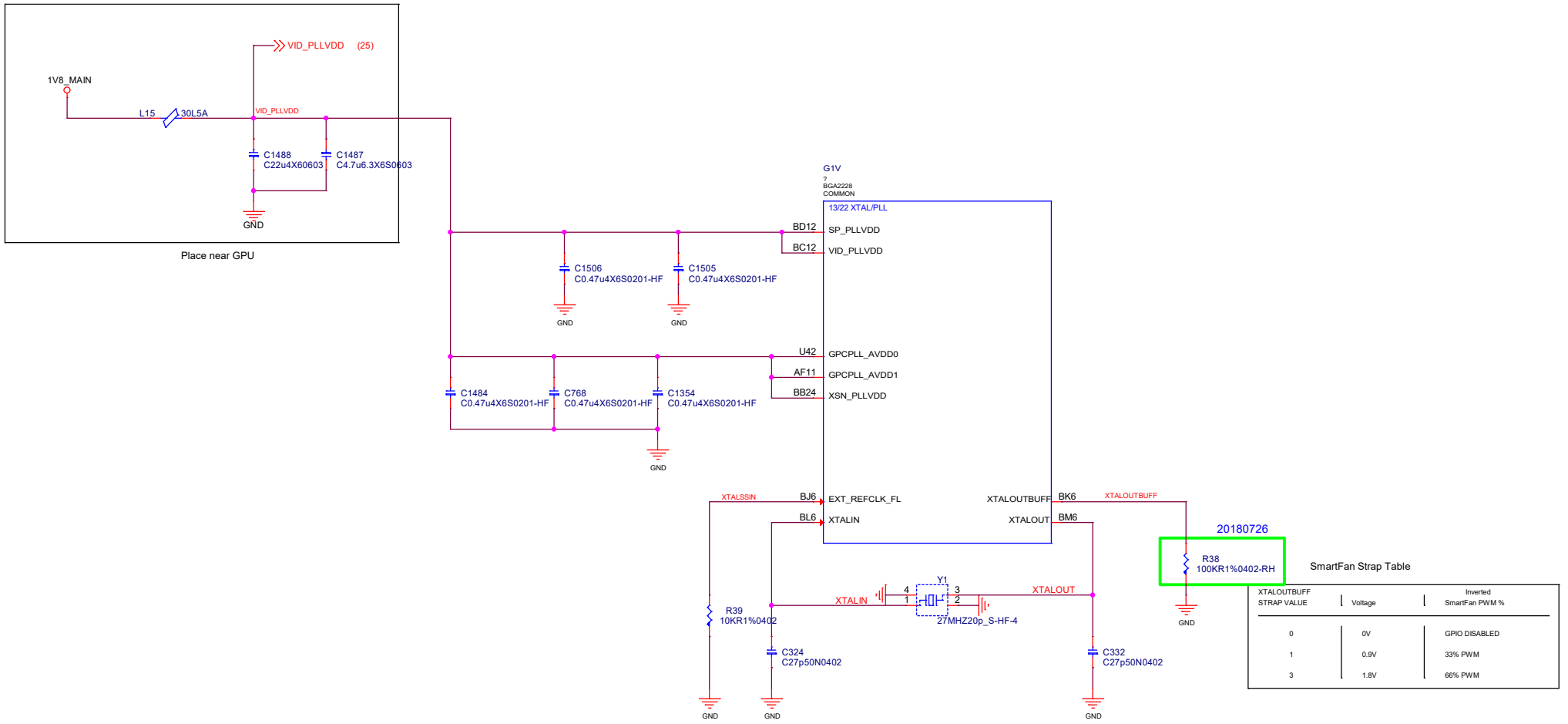




MICRO-STAR INT'L CO.,LTD.

Title: DGPU_ROM,HW Straps		
Size: Custom	Document Number: MS-16Q4	Rev: 10
Date: Monday, December 24, 2018	Sheet 28 of 75	

Check!!!!!!



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU MIO & XTAL		
Size: A3	Document Number: MS-16Q4	Rev: 10
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nVIDIA Power Sequence Control

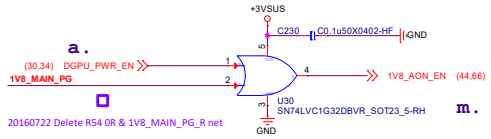
Power on = 1V8_AON ->1V8_MAIN->3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power off= DGPUPWREN->(PEX_VDD->NVVDDQ->3V3_NV)->FBVDDQ->1V8_MAIN->1V8_AON

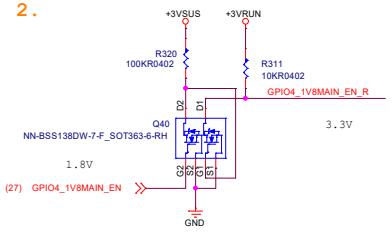
The ramp time for any rail must be more than 40us and is recommended to be less than 2ms

From 1V8_MAIN_EN to PEX_VDD must NOT exceed 4ms

1.



2.



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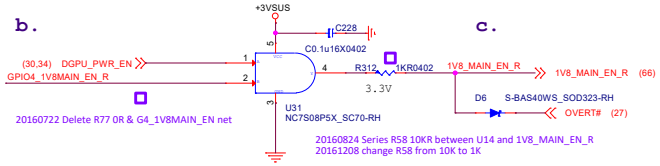
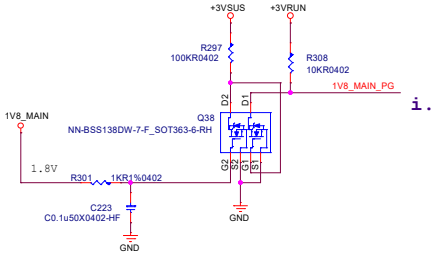
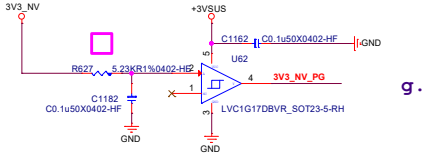


5.



7.



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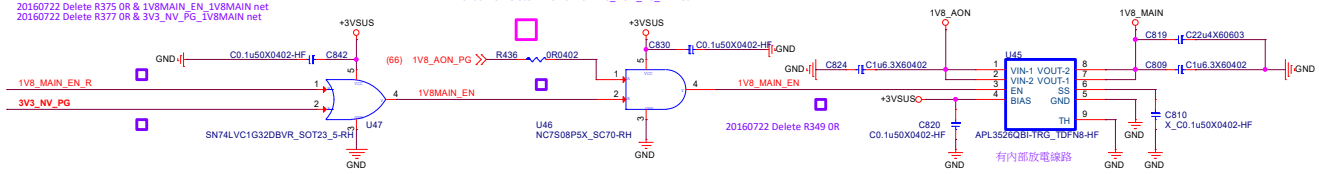

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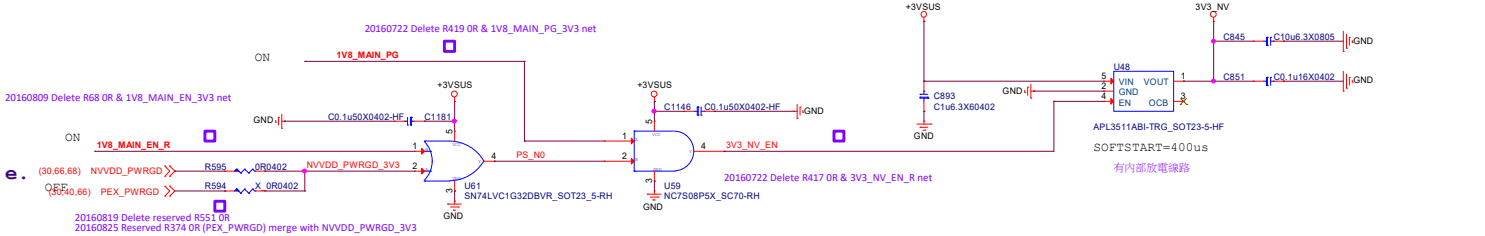
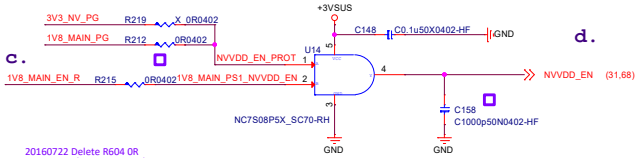


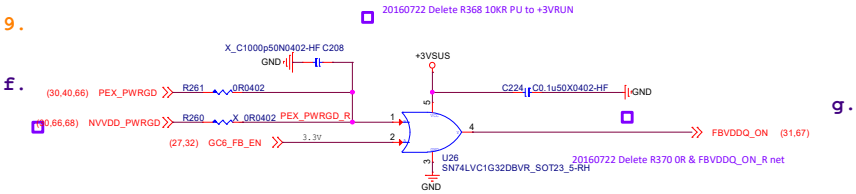
NVVDD Power Enable

The propagation delay between 1V8_MAIN_EN and the NVVDD_EN needs to be less than 300us during both power up and power down

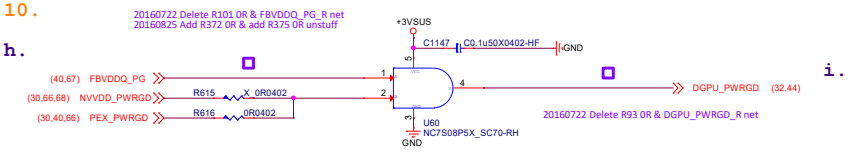
8.



9.



10.



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_Power Sequence

Size: Document Number: MS-16Q4 Rev: 10

Date: Sheet 30 of 75

DGPU_Power Control

20181210

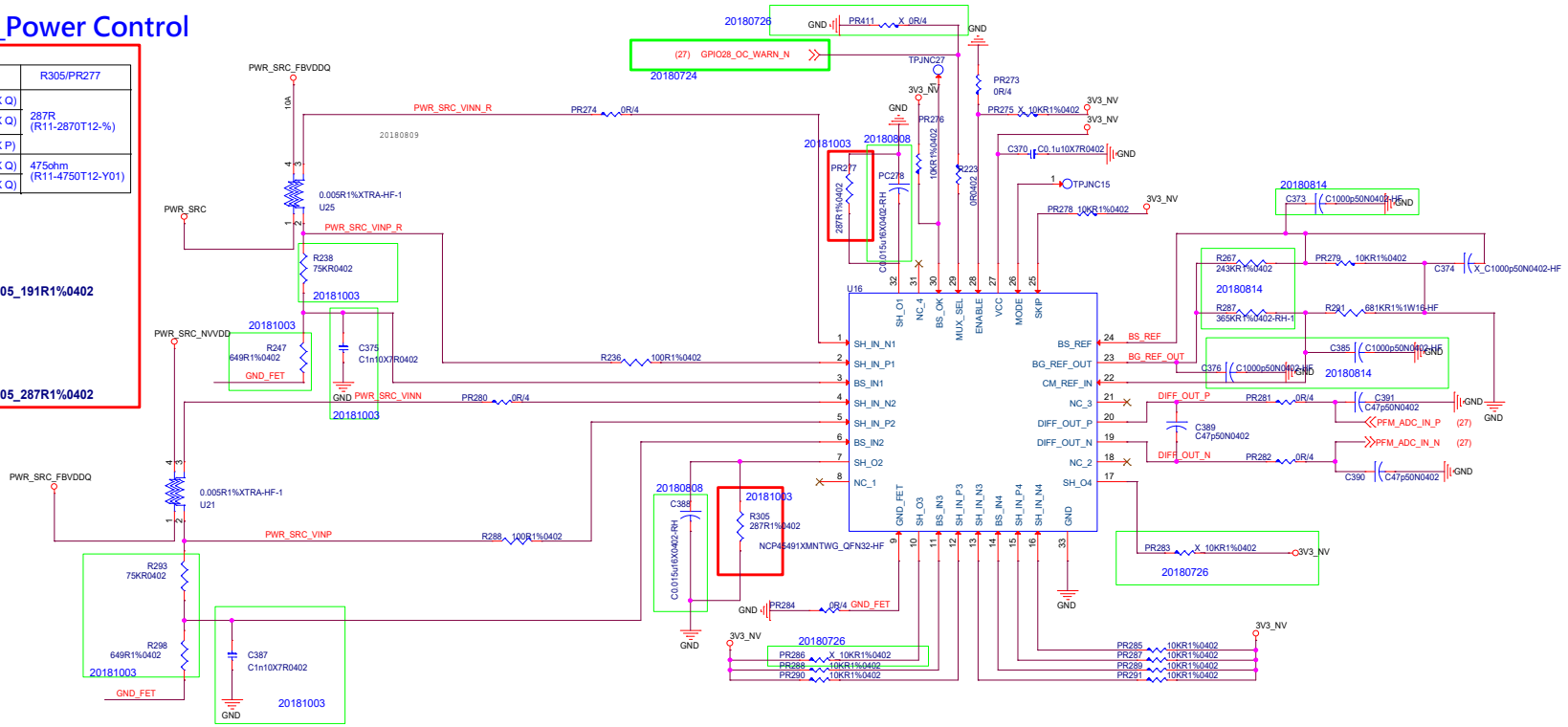
	R305/PR277
N18E-G3(MAX Q)	287R (R11-2870T12-%)
N18E-G2(MAX Q)	
N18E-G1(MAX P)	
N18E-G1(MAX Q)	475ohm (R11-4750T12-Y01)
N18E-G0(MAX Q)	

PU100

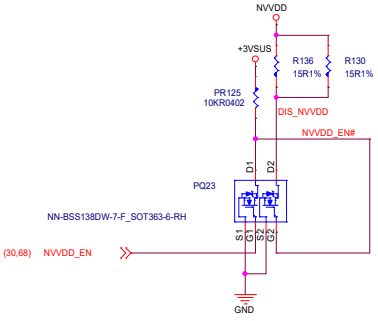
X_PR277_R305_191R1%0402

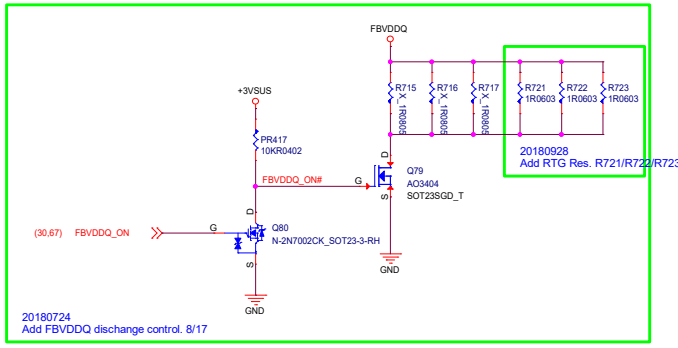
PU101

X_PR277_R305_287R1%0402



Discharge





PEX_VDD 內部放電4ms

3V3_AON內部放電 2ms

1V8AON內部放電2ms

1V8_MAIN內部放電320us

msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_Discharge		
Size: Custom	Document Number: MS-16Q4		Rev: 10
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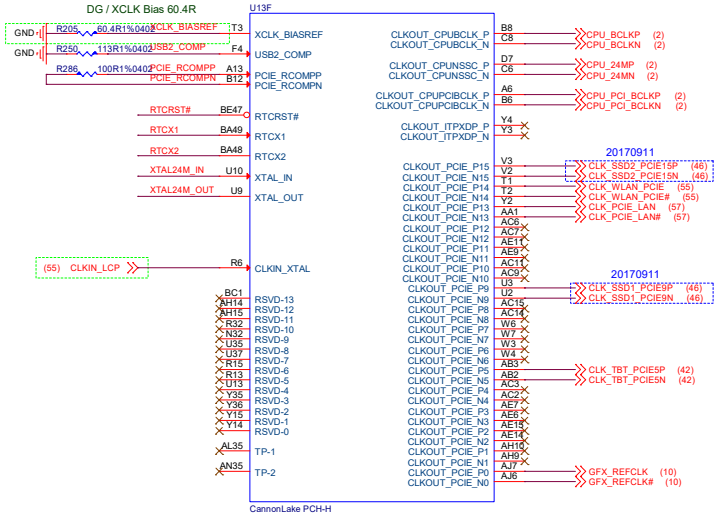
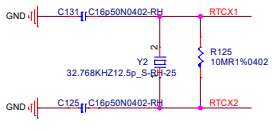
HM370 (RTC/PCIE_Clock/Clock/RSVD)

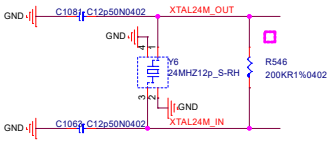


20170828 R2175 change to 200K to follow DG and CRB

RTC Block(Close to PCH)

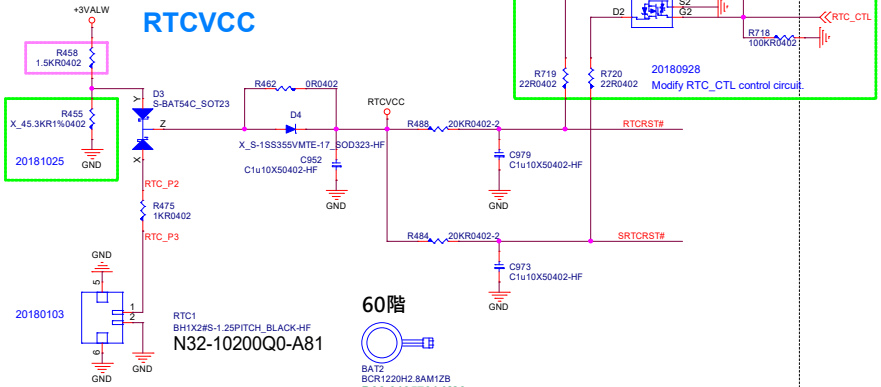


24MHz Clock

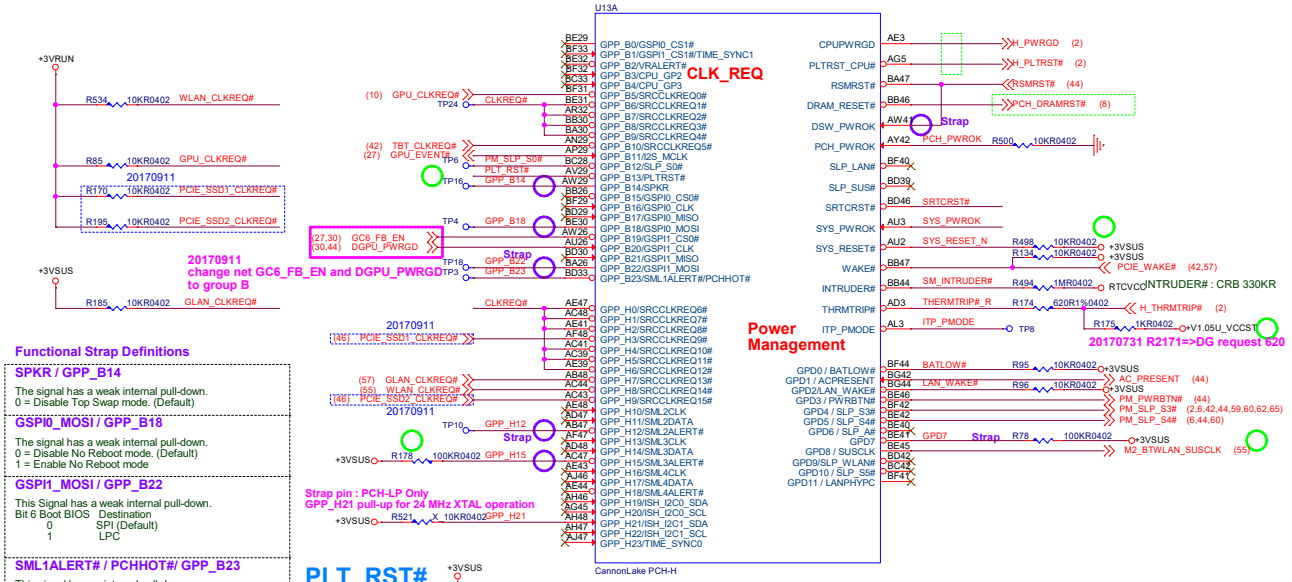


20170731 change R2185 to 1.5K to follow DG

RTCVCC



HM370 (CLKREQ/ACPI)



Functional Strap Definitions

SPKR / GPP_B14

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)

GSPI0_MOSI / GPP_B18

The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

GSPI1_MOSI / GPP_B22

This Signal has a weak internal pull-down.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC

SML1ALERT# / PCHHOT# / GPP_B23

This signal has an internal pull-down.

GPP_H12

This signal has a weak internal pull-down.

GPP_H15

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

GPPD7

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

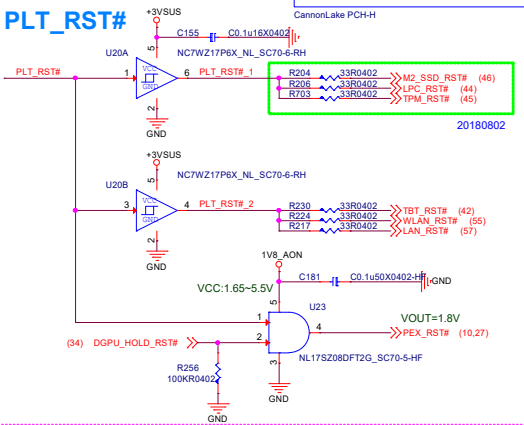
DG/ RTC Well Input Strap

RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

20170911 change net GC6_FB_EN and DGPU_PWRGD to group B

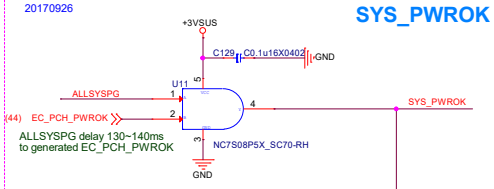
Strap pin : PCH-LP Only
GPP_H21 pull-up for 24 MHz XTAL operation

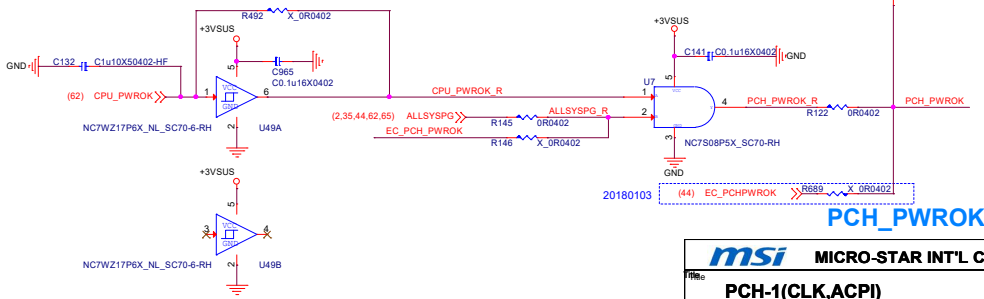
PLT_RST#



20170926

SYS_PWROK

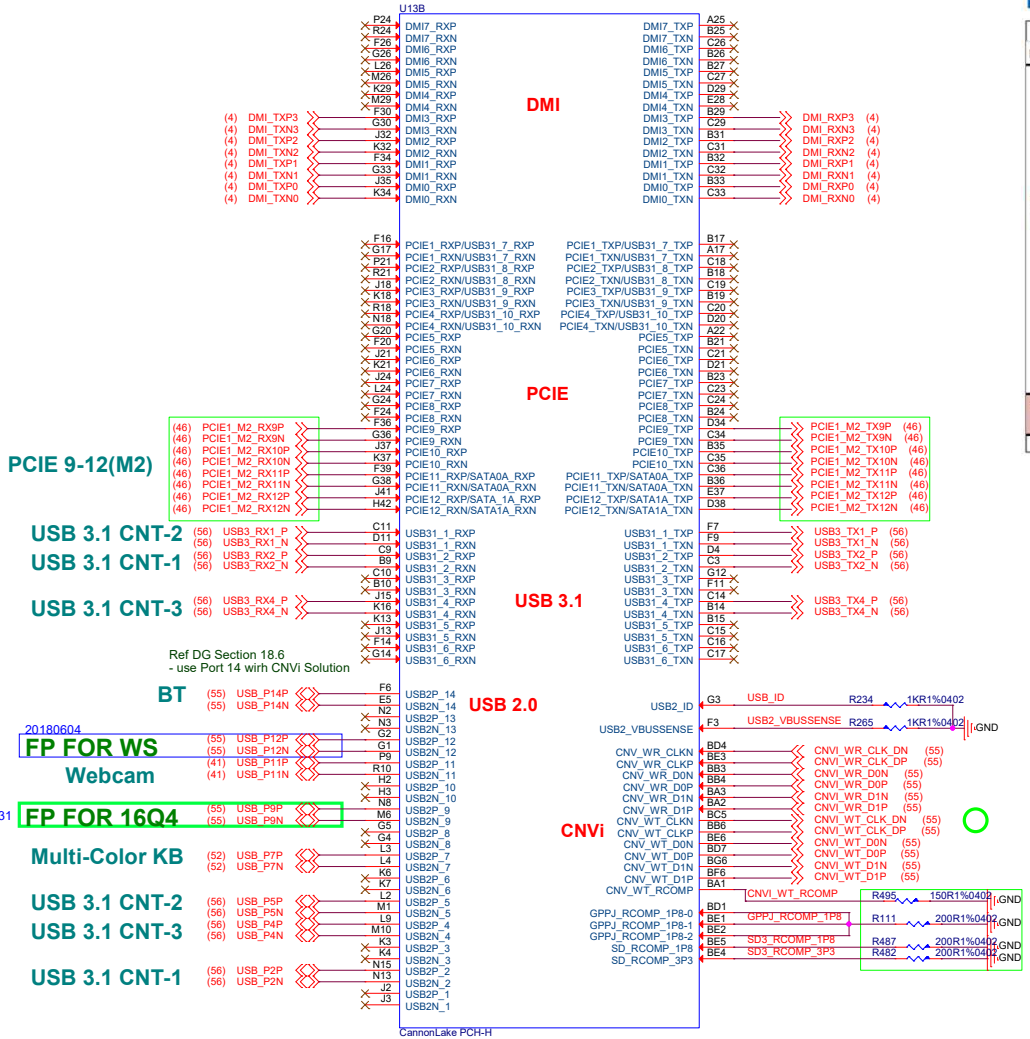


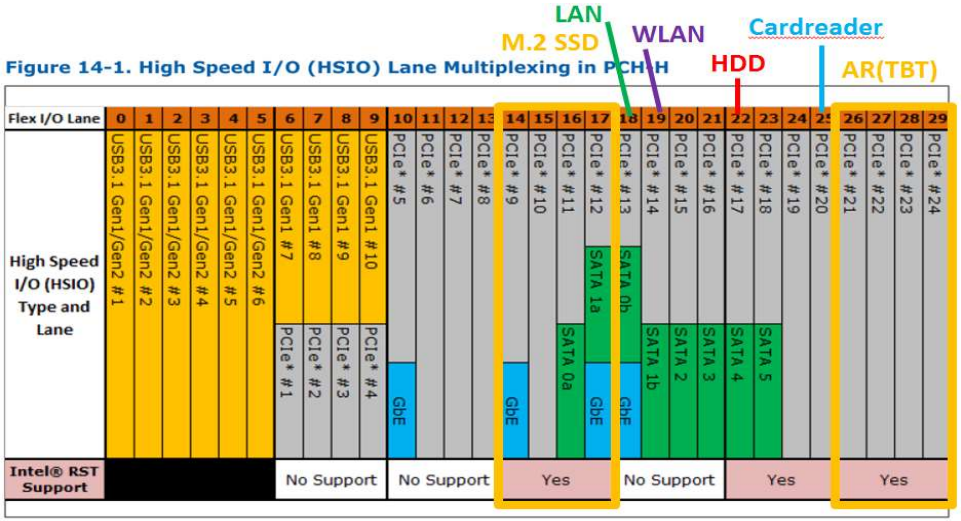


PCH_PWROK

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-1(CLK,ACPI)		
Size: C	Document Number: MS-16Q4	Rev: 10
Date: Monday, December 24, 2018	Sheet: 32 of 75	

HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)





SKU

¹ SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.

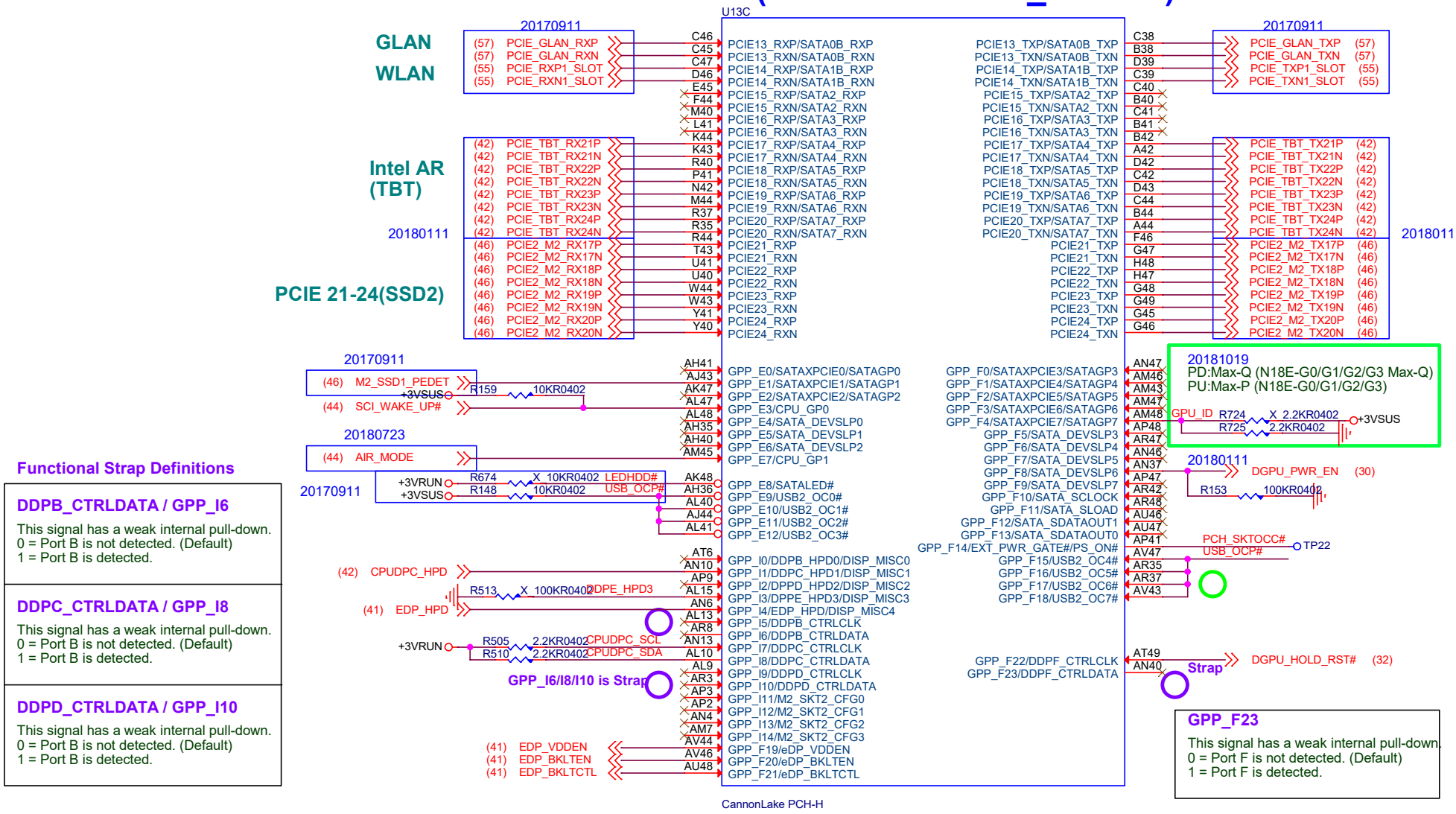
HM370
QM370
CM246

Intel® RST for PCIe Storage port configurable as x2/x4 M.2.

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

msi	MICRO-STAR INT'L CO.,LTD.
Title	PCH-2(DMI/PCIE/USB)
Size	Document Number: MS-16Q4 — Rev: 10
Date:	Monday, December 24, 2018 — Sheet 33 of 75

HM370(SATA/PCIE/USB_OC/DDI)



Functional Strap Definitions

DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_F23

This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.

MICRO-STAR INT'L CO.,LTD.

Title: PCH-3(SATA/PCIE/USB_OC/DDI)

Size: Custom | Document Number: MS-16Q4 | Rev: 10

Date: Monday, December 24, 2018 | Sheet 34 of 75

HM370 (HDA/GPIO/TJAG)

Functional Strap Definitions

SMBALERT# / GPP_C2

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

SML0ALERT# / GPP_C5

This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

HDA_SDO

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)

+3VSUS
R87 2.2KR0402 SUS_SMBCLK
R88 2.2KR0402 SUS_SMBDATA
TP12 GPP_C2
R86 X_499R1%0402 SML0_CLK_R
R89 X_499R1%0402 SML0_DATA_R
GPP_C5
TP5
20170926
Strap
+3VSUS R90 X_10KR0402
1 = eSPI Is selected for EC.

20170801
delete C8613
add C8988,C8989,C8990,C8991,C8992
to follow DG

20170731 change R2352 and R2353 to 30R to follow DG

U13D

SMBUS
GPP_C0/SMBCLK BE26
GPP_C1/SMBDATA BF26
GPP_C2/SMBALERT# BE25
GPP_C3/SML0CLK BF25
GPP_C4/SML0DATA BE24
GPP_C5/SML0ALERT# BF24
GPP_C6/SML1CLK BF27
GPP_C7/SML1DATA BE27
GPP_C8/UART0_RXD BE23
GPP_C9/UART0_TXD BB24
GPP_C10/UART0_RTS# BA24
GPP_C11/UART0_CTS# AP24
GPP_C12/UART1_RXD/ISH_UART1_RXD AU24
GPP_C13/UART1_TXD/ISH_UART1_TXD AP21
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AW24
GPP_C15/UART1_CTS#/ISH_UART1_CTS# BD21
GPP_C16/I2C0_SDA BF23
GPP_C17/I2C0_SCL BC22
GPP_C18/I2C1_SDA BF21
GPP_C19/I2C1_SCL BE21
GPP_C20/UART2_RXD BD20
GPP_C21/UART2_TXD BE20
GPP_C22/UART2_RTS# AW21
GPP_C23/UART2_CTS# AV21

GPIO
GPP_D0/SPI1_CS#/SBK0/BK0 BF19
GPP_D1/SPI1_CLK/SBK1/BK1 BE19
GPP_D2/SPI1_MISO/SBK2/BK2 BE18
GPP_D3/SPI1_MOSI/SBK3/BK3 BF18
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4 BE15
GPP_D5/I2S2_SFRM/CNV_RF_RESET# BE16
GPP_D6/I2S2_TXD/MODEM_CLKREQ BA17
GPP_D7/I2S2_RXD AW18
GPP_D8/I2S2_SCLK AV18
GPP_D9/ISH_SPI_CS#/GSPI2_CS0# BA20
GPP_D10/ISH_SPI_CLK/GSPI2_CLK BB20
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO BB16
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI AN18
GPP_D13/ISH_UART0_RXD/I2C2_SDA BE17
GPP_D14/ISH_UART0_TXD/I2C2_SCL BF17
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN AR18
GPP_D16/ISH_UART0_CTS#/CNV_WCEN BF14
GPP_D17/DMIC_CLK1/SNDW3_CLK AW15
GPP_D18/DMIC_DATA1/SNDW3_DATA AV16
GPP_D19/DMIC_CLK0/SNDW4_CLK BD16
GPP_D20/DMIC_DATA0/SNDW4_DATA BF15
GPP_D21/SPI1_IO2 BD17
GPP_D22/SPI1_IO3 BC17
GPP_D23/ISH_I2C2_SCL/I2C3_SCL BE14

CNVI_RF_RESET (55)
MODEM_CLKREQ (55)

20170911
change net GC6_FB_EN and DGPU_PWRGD to group B

TP_I2C_DATA (55)
TP_I2C_CLK (55)
20180723

+3VSUS
20180724
R207 2.2KR0402 TP_I2C_CLK
R202 2.2KR0402 TP_I2C_DATA

TP15
TP14
TP13
TP20

(47) CODEC_HDA_BITCLK R101 33R0402 C105 C2p50N0402
(47) CODEC_HDA_RST# R106 33R0402 C108 C2p50N0402
HDA_BCLK BD11
HDA_RST_N BE10
C112 C2p50N0402
(47) CODEC_HDA_SDIN0
CODEC_HDA_SDIN0 BF10
C106 C2p50N0402
(47) CODEC_HDA_SDOUT R104 33R0402
(44) FLASH_SECURITY R102 1KR1%0402
(47) CODEC_HDA_SYNC R105 33R0402
C107 C2p50N0402
HDA_SDO BF12
HDA_SYNC BG13
Strap
R138 30R0402 DISPA_BCLK_R
(4) DISPA_BCLK
(4) DISPA_SDI
(4) DISPA_SDO
R140 30R0402 DISPA_SDO_R
AM3
AN3
AM2
BD12
BE12

AUDIO
HDA_BCLK/I2S0_SCLK
HDA_RST#/I2S1_SCLK
HDA_SDI1/I2S1_RXD
HDA_SDI0/I2S0_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDACPU_SCLK
HDACPU_SDI
HDACPU_SDO
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA

AR2 CL_CLK
AT5 CL_DATA
AU4 CL_RST#

TJAG
CPU_TRST# AM4 H_TRST_N_R (2)
PCH_JTAG_TCK AJ3 TP9
PCH_JTAG_TDI AH2 CPU_TDI (2)
PCH_JTAG_TMS AJ4 CPU_TMS (2)
PCH_JTAGX AH4 CPU_TCK (2)
PCH_JTAG_TDO AH3 CPU_TDO (2)
PRDY# AM5 H_PRDY_N (2)
PREQ# AL2 H_PREQ_N (2)
TRIGGER_IN AK2
TRIGGER_OUT AK3 TRIGGER_OUT R147 30R0402 CPU_2_PCH_TRIGGER_R (6) PCH_2_CPU_TRIGGER_R (6)

CannonLake PCH-H

+V1.05DX_VCCSTG
CPU_TDO R152 100R0402
CPU_TDI R155 51R0402
CPU_TMS R151 51R0402
Connected JTAG PU to VCCST-G on H line

ref DG / Chapter Platform and Test Hooks
CPU_TDO : PU 100R Near CPU (DG : R1)
PU 100R Near PCH (DG : R3)
CPU_TDI : PU 51R Near PCH (DG : R4)
CPU_TMS : PU 51R Near PCH (DG : R5)
CPU_TCK : 51R to GND Near CPU (DG : R2)

SMB Isolation

+3VSUS +3VRUN
R278 1KR1%0402 R273 1KR1%0402
Q35 NN-BSS138DW-7-F_SOT363-6-RH
(2,32,44,62,65) ALLSYSPG
GND
PWRGD_PS_SMBUS_ISOLATE
+3VRUN
R248 2.2KR0402 R272 2.2KR0402
NN-BSS138DW-7-F_SOT363-6-RH Q34
SUS_SMBCLK
SUS_SMBDATA
SMB_CLK_DIMM (8,9,55)
SMB_DATA_DIMM (8,9,55)
C187 C210 C206
X_C0.1u16X0402 GND GND X_C0.1u16X0402 GND C0.1u16X0402

MICRO-STAR INT'L CO.,LTD.			
Title: PCH-4(HDA/GPIO/TJAG)			
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20170731 change R2226 unstuff to gollow CRB

CLK_PCI_KBC CI10 X_C10p50N0402 GND

HM370 (UART/I2C/SPI)

U13E

+3VRUN

(44) KBRST# BE39 GPP_A0/RCIN#/ESPI_ALERT1#
(44,45) LAD0 BB39 GPP_A1/LAD0/ESPI_IO0
(44,45) LAD1 AW37 GPP_A2/LAD1/ESPI_IO1
(44,45) LAD2 AV37 GPP_A3/LAD2/ESPI_IO2
(44,45) LAD3 BA38 GPP_A4/LAD3/ESPI_IO3
(44,45) LPC_FRAME# BE38 GPP_A5/LFRAME#/ESPI_CS0#
AW35 GPP_A6/SERIRQ/ESPI_CS1#
EC_PIRQ_PU BA36 GPP_A7/PIRQA#/ESPI_ALERT0#
EC_CLKRUN#_R AV32 GPP_A8/CLKRUN#
CLK_PCI_KBC_R BB36 GPP_A9/CLKOUT_LPC0/ESPI_CLK
CLK_PCI_TPM_R BB34 GPP_A10/CLKOUT_LPC1
PME# BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#
BF36 GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
BC37 GPP_A13/SUSWARN#/SUSPWRDNACK
BF38 GPP_A14/SUS_STAT#/ESPI_RESET#
TP2 GPP_A15 BE35 GPP_A15/SUSACK#
BE33 GPP_A16/CLKOUT_48
BD38 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
BF35 GPP_A18/ISH_GP0
BD34 GPP_A19/ISH_GP1
BE34 GPP_A20/ISH_GP2
BA33 GPP_A21/ISH_GP3
AW32 GPP_A22/ISH_GP4
AV34 GPP_A23/ISH_GP5

LPC

R76 10KR0402 (44,45) INT_SERIRQ R103 10KR1%0402 +3VSUS
R493 22R0402 (44) CLK_PCI_KBC
+3VSUS R84 X_10KR0402
(44) ECESPI_RST#
(55) ATTN#
20180724

+3VSUS
R80 10KR1%0402
EC_CLKRUN#_R R100 0R0402 EC_CLKRUN# (44)
R79 X_10KR0402 GND

N48 GPP_K4
N47 GPP_K5
P47 GPP_K6
R46 GPP_K7
P48 GPP_K8
V47 GPP_K9
V48 GPP_K10
W47 GPP_K11
Y46 GPP_K12/GSXDOUT
Y48 GPP_K13/GSXSLOAD
W46 GPP_K14/GSXDIN
AA45 GPP_K15/GSXSRESET#
Y47 GPP_K16/GSXCLK
R47 GPP_K17/ADR_COMPLETE
T47 GPP_K18/NMI#
T48 GPP_K19/SMI#
T46 GPP_K20
T45 GPP_K21
L48 GPP_K22/IMGCLKOUT0
M45 GPP_K23/IMGCLKOUT1

(42) TBT_CIO_PLUG_EVENT#
(42) TBT_FORCE_PWR_R
(44) KBSCI#

EDS:SCI capabillity is available on all GPIOs

AW13 GPP_G0/SD_CMD
BE9 GPP_G1/SD_D0
BF8 GPP_G2/SD_D1
BF9 GPP_G3/SD_D2
BG8 GPP_G4/SD_D3
BE8 GPP_G5/SD_CD#
BD8 GPP_G6/SD_CLK
AV13 GPP_G7/SD_WP

EDS:GPP_G[7:0] (support SMI# only)

AV6 GPP_J0/CNV_PA_BLANKING
AY3 GPP_J1/CPU_VCCIO_PWR_GATE#
AW3 GPP_J2
AT10 GPP_J3
AV4 GPP_J4/CNV_BRI_DT/UART0_RTS#
AY2 GPP_J5/CNV_BRI_RSP/UART0_RXD
BA4 GPP_J6/CNV_RGI_DT/UART0_TXD
AV3 GPP_J7/CNV_RGI_RSP/UART0_CTS#
AW2 GPP_J8/CNV_MFUART2_RXD
AU9 GPP_J9/CNV_MFUART2_TXD
AV7 GPP_J10
AR13 GPP_J11/A4WP_PRESENT

TP19 CPU_C10_GATE# (6,65)

Strap

CNVI_BRI_DT (55) GPP_J4
CNVI_BRI_RSP (55)
CNVI_RGI_DT (55) GPP_J6
CNVI_RGI_RSP (55)

TP7
TP21

L47 GPP_K0
L46 GPP_K1
U48 GPP_K2
U47 GPP_K3

DG / Single Flash Topology Table 29-3
(1) R use 50 Ohm for 3.3V
(2) SPIO_IO2/IO3 PU 1KR when using quad mode

GND CI1 X_C10p50N0402

AW47 SPI0_CLK PCH_SPI_CLK R143 49.9R1%0402 SPI_CLK
AY47 SPI0_CS0# SPI_CS0#
AW48 SPI0_CS1#
AY48 SPI0_IO2 PCH_SPI_WP# R141 49.9R1%0402 SPI_WP#
BA46 SPI0_IO3 PCH_SPI_HOLD# R139 49.9R1%0402 SPI_HOLD#
BA45 SPI0_MISO PCH_SPI_MISO R499 49.9R1%0402 SPI_MISO
AU41 SPI0_MOSI PCH_SPI_MOSI R497 49.9R1%0402 SPI_MOSI
AT40 SPI0_CS2#

Strap Pin

AE2 PM_DOWN H_PM_DOWN (2)
AF3 PM_SYNC PCH_PM_SYNC R161 30R0402 H_PM_SYNC (2)
AF2 PECI PCH_PECI R160 X_10KR0402 GND

CRB : PCH PECI 10KR NC

20170731 change R2228 to R11-0103012-W08
but no stuff following CRB

CannonLake PCH-H

Functional Strap Definitions

GPP_J4

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

GPP_J6

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

SPI0_IO2

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_IO3

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_MOSI

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

MISO isn't Strap

20180802

(45) CLK_PCI_TPM 22R0402 R704 CLK_PCI_TPM_R
C1549 X_C10p25N0402

SPI FLASH ROM 16MB

+VCCSPI : connect to +3VSUS

+3VSUS +3VSUS +3VSUS +3VSUS +3VSUS

R231 1KR0402
R218 1KR0402
GND C164 C0.1u16X0402
R222 1KR0402
R229 1KR0402
20170926

(44) SPI_CS0#
(44) SPI_MISO
SPI_WP#
SPI_HOLD#
SPI_CLK (44)
SPI_MOSI (44)

U19
1 CS VCC 8
2 DO(IO1) HOLD(IO3) 7
3 WP(IO2) CLK 6
4 GND DI(IO0) 5
GND
MX25L12873FM2I-10G-HF

20170809 U79 change from socket to ROM
P/N：M31-2512832-M24

20170831
add R3535 and R3536 for GCoff

(40,44) DP_HPD R226 0R0402 GPP_K7
(39,44) HDMI_HPD_DET R555 0R0402 GPP_K10

M31-2512893-W03
,M-IC FLASH,128M(16Mx8bit),10ms,SOIC-8pin(208mil),WINBOND/W25Q128JVSIQ,2.7V,3.6V,SPI,,HALOGEN FREE

M31-2512832-M24
,M-IC FLASH,128M(16Mx8bit),40ms,SOP-8pin,MXICMX25L12873FM2I-10G(T),2.7V,3.6V,SPI,,HALOGEN FREE

MICRO-STAR INT'L CO.,LTD.

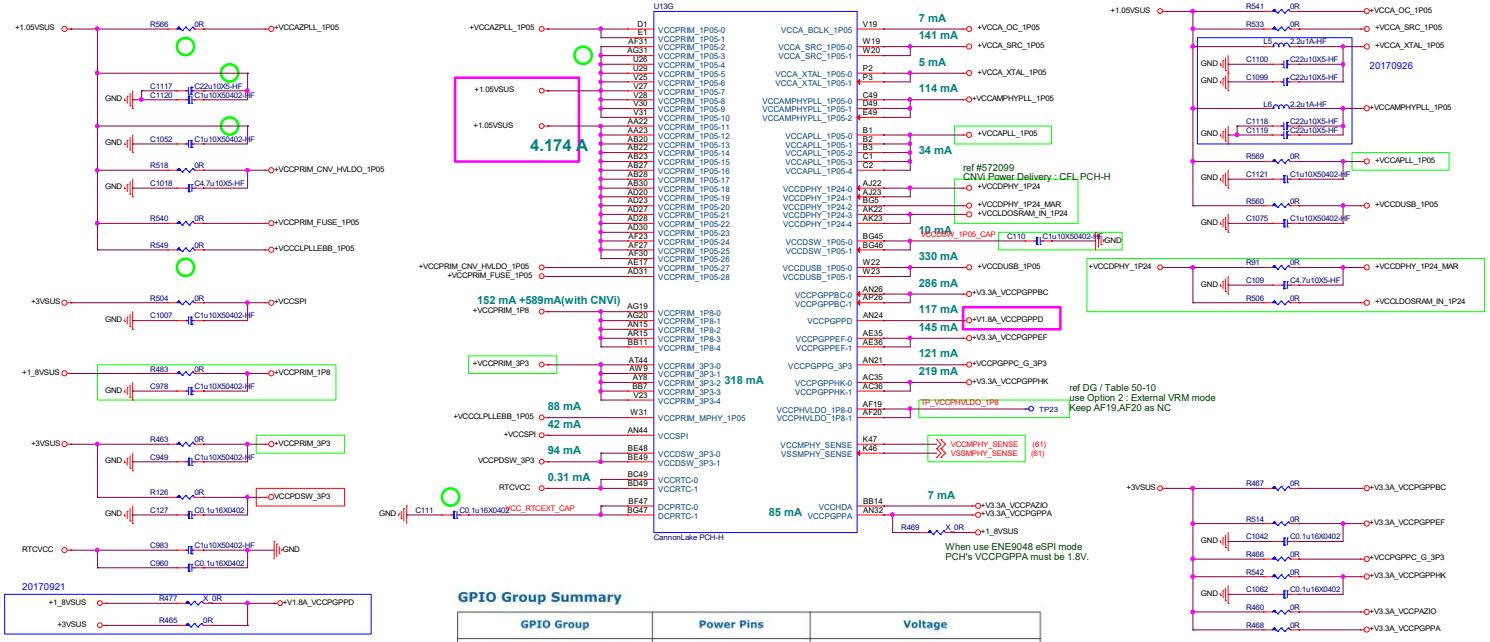
Title: PCH-5(UART/I2C/SPI)

Size | Document Number: MS-16Q4 | Rev: 10

Date: Monday, December 24, 2018 Sheet 36 of 75

HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements



20170911 change VCCPGPPD from 3.3V to 1.8V(SUS)
20170920 add R612 for +3VSUS

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPPBC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

Power Descriptions for PCH in CNL-H

Name	Description
VCCA_BCLK_1P05	**Analog supply for BCLK circuitries**: 1.05V
VCCA_SRC_1P05	**Analog supply for PCIe clock circuitries**: 1.05V
VCCA_XTAL_1P05	**Analog supply for XTAL circuitries**: 1.05V
VCCDUSB_1P05	**Supply for USB digital logic**: 1.05V
VCCAPLL_1P05	**Analog supply for BCLK/DMI/Audio PLLs:** 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P05	**Primary Well**: 1.05V. For PCIe//USB3/SATA MPHY logic, I/O blocks, SRAM, JTAG, CNVi.
VCCDSW_1P05	**Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P05	**Mod PHY Primary**: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB PLL dividers.
VCCAMPHYPLL_1P05	**Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs**: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_1P8	**1.8V Primary Well**.
VCCPRIM_3P3	**3.3V Primary Well**.
VCCSPI	**SPI Primary Well 3.3V or 1.8V**, for SPI interface.
VCCHDA	**HDA Audio Power 3.3V, 1.8V, or 1.5V**, for Intel® High Definition Audio.
VCCDSW_3P3	**3.3V Deep Sx Well**.
VCCRTC	**RTC Well Supply**. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. ***Note:*** VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. ***Note:*** Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
DCPRTC	RTC decoupling capacitor only. This rail should NOT be driven.
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	**1.8V or 3.3V for GPP_A group.**
VCCPGPPBC	**1.8V or 3.3V for GPP_B and GPP_C groups.**
VCCPGPPD	**1.8V or 3.3V for GPP_D group.**
VCCPGPPEF	**1.8V or 3.3V for GPP_E and GPP_F groups.**
VCCPGPPG_3P3	**3.3V for GPP_G group.**
VCCPGPPHK	**1.8V or 3.3V for GPP_H and GPP_K groups.**
VCCMPHY_SENSE	**1.05V Sense Line.**
VSSMPHY_SENSE	**0V (Ground) Sense Line.**
VSS	**Ground.**

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Title: PCH-6(Power)

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PCH-H(GND)

20170731 Add TP22 to follow CRB suggestion
20170911 Del TP22 to follow CRB 0.9

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Title	PCH-7(GND)	
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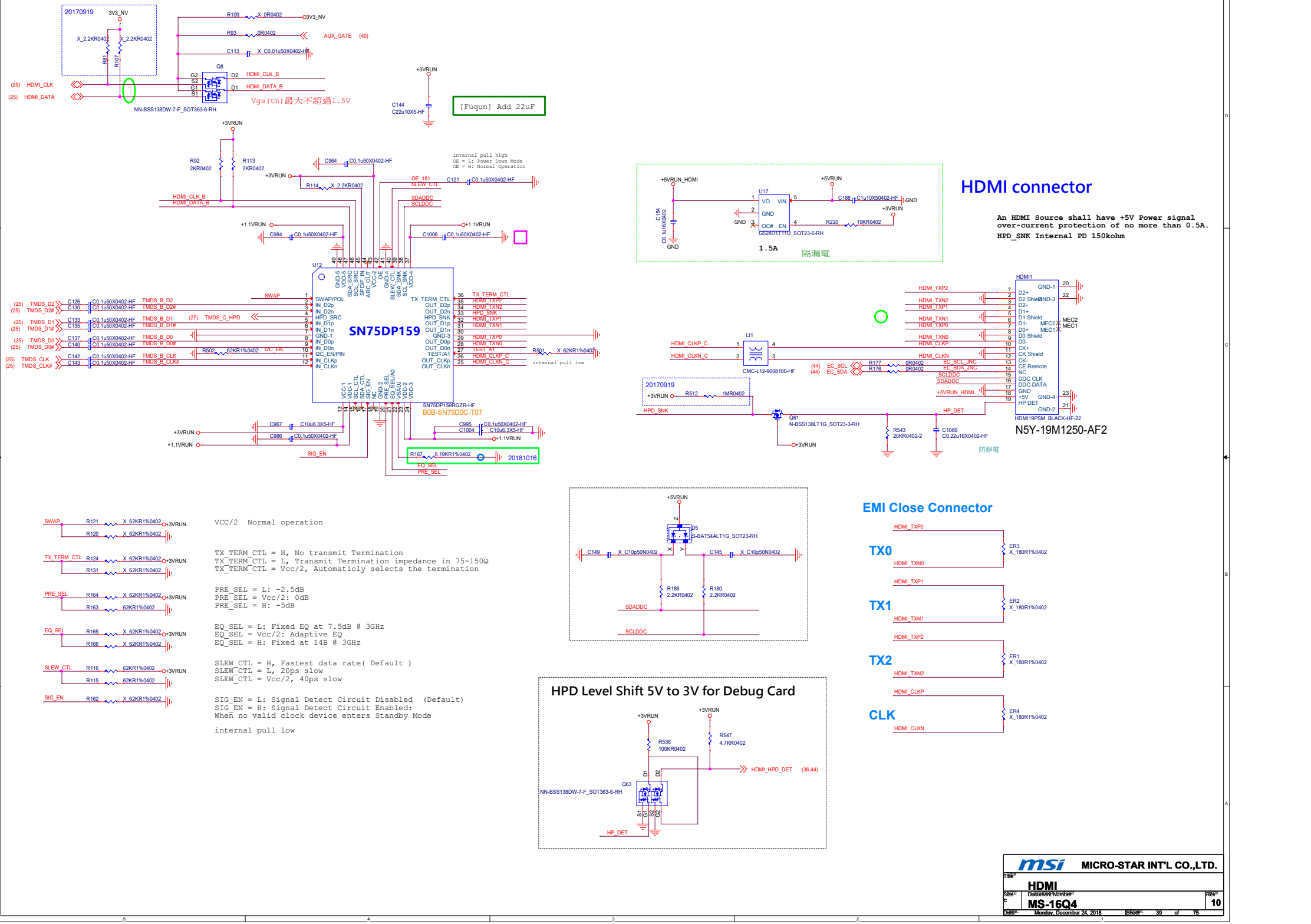
20170919
3V3_NV
X_2.2KR0402
X_2.2KR0402
R84
R107
R109 X 0R0402 3V3_NV
R93 0R0402 AUX_GATE (40)
C113 X C0.01u50X0402-HF
Q8
G2
S2
G1
S1
D2 HDMI_CLK_B
D1 HDMI_DATA_B
(25) HDMI_CLK
(25) HDMI_DATA
NN-BSS138DW-7-F_SOT363-6-RH
Vgs(th)最大不超過1.5V
+3VRUN
C144
C22u10X5-HF
[Fuqun] Add 22uF
R92
2KR0402
R113
2KR0402
C964 C0.1u50X0402-HF
R114 X 2.2KR0402
internal pull high
OE = L: Power Down Mode
OE = H: Normal Operation
OE_181
SLEW_CTL
C121 C0.1u50X0402-HF
SDADDC
SCLDDC
HDMI_CLK_B
HDMI_DATA_B
+1.1VRUN
C984 C0.1u50X0402-HF
C1006 C0.1u50X0402-HF
U12
SN75DP159
SWAP
SWAP/POL
IN_D2p
IN_D2n
HPD_SRC
IN_D1p
IN_D1n
GND-1
IN_D0p
IN_D0n
I2C_EN/PIN
IN_CLKp
IN_CLKn
TX_TERM_CTL
OUT_D2p
OUT_D2n
HPD_SNK
OUT_D1p
OUT_D1n
GND-3
OUT_D0p
OUT_D0n
TEST/A1
OUT_CLKp
OUT_CLKn
SN75DP159RGZR-HF
B0B-SN75D0C-T07
(25) TMDS_D2
(25) TMDS_D2#
(25) TMDS_D1
(25) TMDS_D1#
(25) TMDS_D0
(25) TMDS_D0#
(25) TMDS_CLK
(25) TMDS_CLK#
C126 C0.1u50X0402-HF TMDS_B_D2
C130 C0.1u50X0402-HF TMDS_B_D2#
C133 C0.1u50X0402-HF TMDS_B_D1
C135 C0.1u50X0402-HF TMDS_B_D1#
C137 C0.1u50X0402-HF TMDS_B_D0
C140 C0.1u50X0402-HF TMDS_B_D0#
C142 C0.1u50X0402-HF TMDS_B_CLK
C143 C0.1u50X0402-HF TMDS_B_CLK#
(27) TMDS_C_HPD
R502 62KR1%0402 I2C_EN
TX_TERM_CTL
HDMI_TXP2
HDMI_TXN2
HDMI_TXP1
HDMI_TXN1
HDMI_TXP0
HDMI_TXN0
HDMI_CLKN
HDMI_CLKP
R501 X 62KR1%0402
internal pull low
C967 C10u6.3X5-HF
C986 C0.1u50X0402-HF
C995 C0.1u50X0402-HF
C1004 C10u6.3X5-HF
+3VRUN
+1.1VRUN
SIG_EN
R167 6.19KR1%0402
20181016
EQ_SEL
PRE_SEL
+5VRUN_HDMI
U17
VO
VIN
GND
OC#
EN
G524D1T11U_SOT23-5-RH
C154
C0.1u16X0402
C168 C1u10X50402-HF
R220 10KR0402
1.5A
隔漏電
HDMI connector
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.
HPD_SNK Internal PD 150kohm
HDMI1
HDMI19PSM_BLACK-HF-22
N5Y-19M1250-AF2
LI1
CMC-L12-9008100-HF
HDMI_CLKP_C
HDMI_CLKN_C
(44) EC_SCL
(44) EC_SDA
R177 0R0402 EC_SCL_JNC
R176 0R0402 EC_SDA_JNC
SCLDDC
SDADDC
+5VRUN_HDMI
HP_DET
20170919
R512 1MR0402
HPD_SNK
Q61
N-BSS138LT1G_SOT23-3-RH
R543 20KR0402-2
C1066 C0.22u16X0402-HF
防靜電
SWAP R121 X 62KR1%0402 +3VRUN
R120 X 62KR1%0402
VCC/2 Normal operation
TX_TERM_CTL R124 X 62KR1%0402 +3VRUN
R131 X 62KR1%0402
TX_TERM_CTL = H, No transmit Termination
TX_TERM_CTL = L, Transmit Termination impedance in 75~150Ω
TX_TERM_CTL = Vcc/2, Automaticly selects the termination
PRE_SEL R164 X 62KR1%0402 +3VRUN
R163 62KR1%0402
PRE_SEL = L: -2.5dB
PRE_SEL = Vcc/2: 0dB
PRE_SEL = H: -5dB
EQ_SEL R165 X 62KR1%0402 +3VRUN
R166 X 62KR1%0402
EQ_SEL = L: Fixed EQ at 7.5dB @ 3GHz
EQ_SEL = Vcc/2: Adaptive EQ
EQ_SEL = H: Fixed at 14B @ 3GHz
SLEW_CTL R116 62KR1%0402 +3VRUN
R115 62KR1%0402
SLEW_CTL = H, Fastest data rate(Default)
SLEW_CTL = L, 20ps slow
SLEW_CTL = Vcc/2, 40ps slow
SIG_EN R162 X 62KR1%0402
SIG_EN = L: Signal Detect Circuit Disabled (Default)
SIG_EN = H: Signal Detect Circuit Enabled:
When no valid clock device enters Standby Mode
internal pull low
+5VRUN
D5
S-BAT54ALT1G_SOT23-RH
C149 X C10p50N0402
C145 X C10p50N0402
R186 2.2KR0402
R180 2.2KR0402
SDADDC
SCLDDC
HPD Level Shift 5V to 3V for Debug Card
+3VRUN
R536 100KR0402
R547 4.7KR0402
HDMI_HPD_DET (36,44)
Q63
NN-BSS138DW-7-F_SOT363-6-RH
HP_DET
EMI Close Connector
TX0
TX1
TX2
CLK
HDMI_TXP0
HDMI_TXN0
HDMI_TXP1
HDMI_TXN1
HDMI_TXP2
HDMI_TXN2
HDMI_CLKP
HDMI_CLKN
ER3 X_180R1%0402
ER2 X_180R1%0402
ER1 X_180R1%0402
ER4 X_180R1%0402
MICRO-STAR INT'L CO.,LTD.
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DP 1.4 Retimer (PS8463)

+3VRUN VDD33 L36 330L1.2A-150-RH C1704 C4.7u6.3X6S0603 C1690 C0.1u10X4 C1703 C0.1u10X4 C361 C0.1u10X4 GND Close Chip

+1.2VRUN VDD12 L37 330L1.2A-150-RH C381 C4.7u6.3X6S0603 C362 C0.1u10X4 C379 C0.1u10X4 C378 C0.1u10X4 GND Close Chip

+1.2VRUN VDDTX12 L38 330L1.2A-150-RH C1705 C4.7u6.3X6S0603 C1701 C0.1u10X4 C364 C0.1u10X4 C1702 C0.1u10X4 GND Close Chip

+1.2VRUN VDDRX12 L39 330L1.2A-150-RH C360 C4.7u6.3X6S0603 C367 C0.1u10X4 C372 C0.1u10X4 C365 C0.1u10X4 GND Close Chip

+1.2VRUN VDDA12 L40 330L1.2A-150-RH C371 C4.7u6.3X6S0603 C369 C0.1u10X4 C366 C0.1u10X4 C363 C0.1u10X4 GND Close Chip

+1.2VRUN

+1.2VRUN +3VSUS U18 VDD S D CAP GND ON SLG7NT402V_TDFN8-HF TDFN8 I36-NT4020C-SF9 C382 C1u6.3X50201-HF +1_2VDIMM C377 C10u6.3X50402-HF RUN_ON (44,59,61) C384 C0.01u50X0402

20181002

EQ0 R692 X_4.7KR0402 R693 4.7KR0402 +3VRUN GND
EQ1 R701 X_4.7KR0402 R702 4.7KR0402 +3VRUN GND

[EQ1,EQ0] (internal pull down 150k-ohm)=
LL:Compensate channel loss up to 8 @ HBR3
LM:Compensate channel loss up to 11 @ HBR3
LH:Compensate channel loss up to 14 @ HBR3
ML:Compensate channel loss up to 16 @ HBR3
MM:Compensate channel loss up to 17 @ HBR3
MH:Compensate channel loss up to 18 @ HBR3
HL:Compensate channel loss up to 19 @ HBR3
HM:Compensate channel loss up to 20 @ HBR3
HH:Compensate channel loss up to 21 @ HBR3

I2C_ADDR R225 X_4.7KR0402 R232 4.7KR0402 +3VRUN GND

I2C_ADDR (internal pull down 150k-ohm)=
L:0x10 - 0x2F (Default)
H:0x90 - 0x9F and 0xD0 - 0xDF

U68 PS8463QFN46GTR-A4

VDDRX12 (25) CPUDPD_TXP0 C1102 C0.1u50X7/4 DDID_LANE0_DP (25) CPUDPD_TXN0 C1095 C0.1u50X7/4 DDID_LANE0_DN
(25) CPUDPD_TXP1 C1090 C0.1u50X7/4 DDID_LANE1_DP (25) CPUDPD_TXN1 C1080 C0.1u50X7/4 DDID_LANE1_DN
(25) CPUDPD_TXP2 C1074 C0.1u50X7/4 DDID_LANE2_DP (25) CPUDPD_TXN2 C1069 C0.1u50X7/4 DDID_LANE2_DN
(25) CPUDPD_TXP3 C1060 C0.1u50X7/4 DDID_LANE3_DP (25) CPUDPD_TXN3 C1055 C0.1u50X7/4 DDID_LANE3_DN

TO EC/PCH
TO DGPU
(36,44) DP_HPD R216 33R0402 (27) CPUDPB_HPD

DPC1_LANE0_DP_LC0 C1698 C0.1u50X7/4 DDID_LANE0_DP_C
DPC1_LANE0_DN_LC0 C1697 C0.1u50X7/4 DDID_LANE0_DN_C
DP_CA_DET
DPC1_LANE1_DP_LC1 C1696 C0.1u50X7/4 DDID_LANE1_DP_C
DPC1_LANE1_DN_LC1 C1695 C0.1u50X7/4 DDID_LANE1_DN_C
DP_HPD_SNK
DPC1_LANE2_DP_LC2 C1693 C0.1u50X7/4 DDID_LANE2_DP_C
DPC1_LANE2_DN_LC2 C1694 C0.1u50X7/4 DDID_LANE2_DN_C
DPC1_LANE3_DP_LC3 C1691 C0.1u50X7/4 DDID_LANE3_DP_C
DPC1_LANE3_DN_LC3 C1692 C0.1u50X7/4 DDID_LANE3_DN_C
20181001

VDDA12
VDDTX12_1
EQ1

TPJNC38 TPJNC39 R694 4.99KR1%0402 GND

CFG2 R213 X_4.7KR0402 R214 4.7KR0402 +3VRUN GND

CFG2 (internal pull down 150k-ohm)=
L:PS8463 output is dynamically adjusted based on link training.
M:PS8463 output is fixed to 400mV/0dB.
H:PS8463 output is fixed to 800mV/3.5dB.

CFG1 R700 X_4.7KR0402 +3VRUN

CFG1 (internal pull down 150k-ohm)=
L:Auto EQ enabled, EQ automatically adjusted based on link training
H:Auto EQ disabled.

CFG0 R699 X_4.7KR0402 R697 4.7KR0402 +3VRUN GND

CFG0 (internal pull down 150k-ohm)=
L:Auto jitter cleaning mode (default)
M:Redriving mode
H:Full jitter cleaning mode

PD# R696 4.7KR0402 +3VRUN

PD# (internal pull up 150k-ohm) =
L:Chip power down
H:Normal operation

Avoid DP Leakage

+3VRUN Q41 N-AO3404_SOT23 W>20mils 3V_DP_PWR C236 C4.7u10X5/6 (59) RUND R324 1K/4 C243 C0.1u10X7/4 C254 C4.7u10X5/6 C252 C0.1u10X7/4

Mini Display Port

0.75A

3V_DP_PWR PF1 F-0805L075WR W>20mils DP_PWR MDP1 DP_PWR ML_LANE0P ML_LANE0N ML_LANE1P ML_LANE1N ML_LANE2P ML_LANE2N ML_LANE3P ML_LANE3N AUX_CHP AUX_CHN CONFIG1 CONFIG2 HPD MEC1 MEC2 GND-6 GND-1 GND-2 GND-3 GND-4 GND-5 X1 X2 X3 X4 DISPO20PSM_BLACK-RH-6

DDID_LANE0_DP_C DDID_LANE0_DN_C DDID_LANE1_DP_C DDID_LANE1_DN_C DDID_LANE2_DP_C DDID_LANE2_DN_C DDID_LANE3_DP_C DDID_LANE3_DN_C
CPUDPD_AUXP_CC CPUDPD_AUXN_CC
DP_CA_DET DP_CONFIG2
DP_HPD_SNK
R295 100KR1%0402 R290 100KR1%0402 R299 1MR/4 R294 5.1MR/4 R253 100KR/4 C383 C0.1u10X7/4
D9 BAV99LT1_SOT23

N5W-20M0500-H06

CAD_SNK Have internal Pull down 1Mohm.
HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

AUX Level Shifter

+5VRUN +3VSUS R464 10KR1%/4 R470 10KR1%/4 (39) AUX_GATE Q53 NN-SM1600DSCSC-TRG_SOT363-6-HF
(30,67) FBVDDQ_PG (30,66) PEX_PWRGD R472 X_0R/4 R476 0R/4 20171017 GND
GND C933 C0.01u50X0402 AUX_GATE Q48
(25) CPUDPD_AUXP (25) CPUDPD_AUXN CPUDPD_SCL CPUDPD_SDA
NN-SM1600DSCSC-TRG_SOT363-6-HF
Vgs(th) Max<1.5V

For Dual Mode Switch to DDC

20180726
Follow Sch. review

+3VRUN R211 2KR1%/4 R209 2KR1%/4 R208 4.7KR0402
SCL/SDA PU 2K Ohm
Q39 P-AO3415_SOT23-3-RH Q37 P-AO3415_SOT23-3-RH Q13 N-2N7002CK_SOT23-3-RH
DP_CA_DET
CAD_DECT= "0" =>AUX
CAD_DECT= "1" =>DDC
Q42 NN-SM1600DSCSC-TRG_SOT363-6-HF SDA_SRC SCL_SRC
CPUDPD_SCL CPUDPD_SDA C1700 C0.1u50X7/4 IN_AUXP C1699 C0.1u50X7/4 IN_AUXN

EMI (Close CONN)

DDID_LANE0_DP_C EL1 ER5 X_180R1%/4 X_CMC-L12-9008100-HF DDID_LANE0_DN_C
DDID_LANE1_DP_C EL3 ER6 X_180R1%/4 X_CMC-L12-9008100-HF DDID_LANE1_DN_C
DDID_LANE2_DP_C EL4 ER7 X_180R1%/4 X_CMC-L12-9008100-HF DDID_LANE2_DN_C
DDID_LANE3_DP_C EL11 ER8 X_180R1%/4 X_CMC-L12-9008100-HF DDID_LANE3_DN_C

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Title: DP 1.4 Retimer (PS8463-A4)
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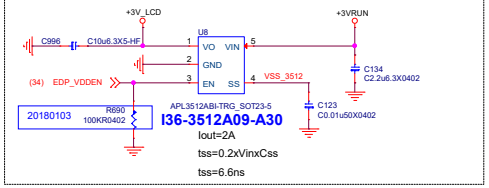
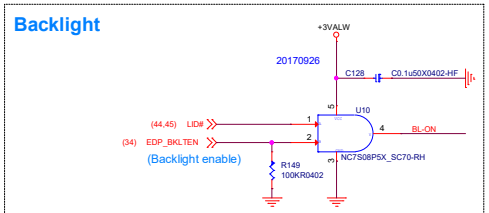
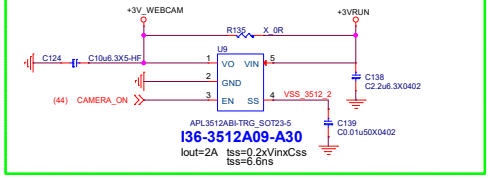
Pannel Device Logic Power



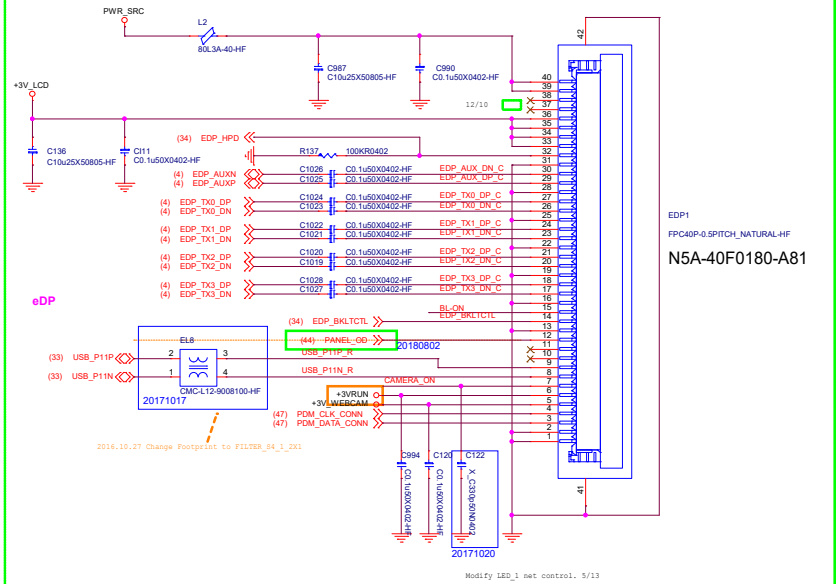
Backlight



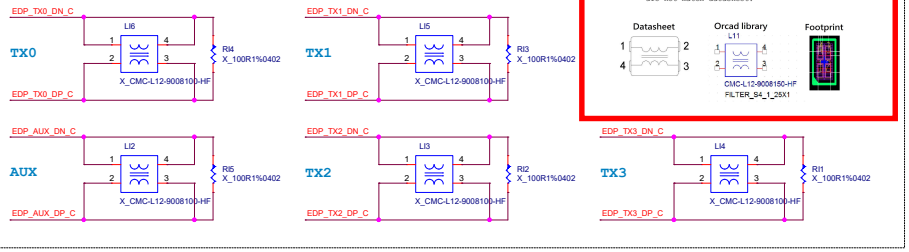
CAMERA Power



eDP Connector

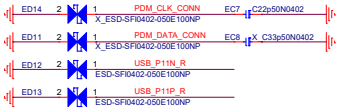


EMI Close Connector



Note: CMC-L12-9008150-HF(P/N : L12-9008150-T19) 's default Orcad library and footprint FILTER_84_1_25X1 are not match datasheet.

ESD



LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufactureer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	
19	VDD	
20	VDD	
21	VDD	
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/0ff
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)

MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector/Camera

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Thunderbolt

20170830
modify for AR b-step, c-step chip and wake function

DDI C
DP++

CIO1

CIO0

B07-L634015-I06

20170830
reserve U3053 and C8999

20170830
R228,R232 change to 2.2K to follow CRB

20170919
R461 change to connect with TBT_CLKREQ#_R

20170830
R262 change to unstuff

GPIO	TERMINATION	Power Rail	
GPIO_0	10K	PU	VCC3V3_LC
GPIO_1	10K	PU	VCC3V3_LC
GPIO_2	100K	PD	
GPIO_3	100K	PD	
GPIO_4	10K	PU	VCC3V3_LC
GPIO_5	10K	PU	VCC3V3_LC
GPIO_6	100K	PD	
GPIO_7	100K	PD	
GPIO_8	100K	PD	
POC_GPIO_0	10K	PU	VCC3V3_TBT_SX
POC_GPIO_1	10K	PU	VCC3V3_TBT_SX
POC_GPIO_2	100K	PD	
POC_GPIO_3	100K	PD	
POC_GPIO_4	10K	PU	VCC3V3_TBT_SX
POC_GPIO_5	10K	PU	VCC3V3_TBT_SX
POC_GPIO_6	100K	PD	

MICRO-STAR INT'L CO.,LTD.

Title: Alpine Ridge(TBT)

Size: | Document Number: MS-16Q4 | Rev: 10

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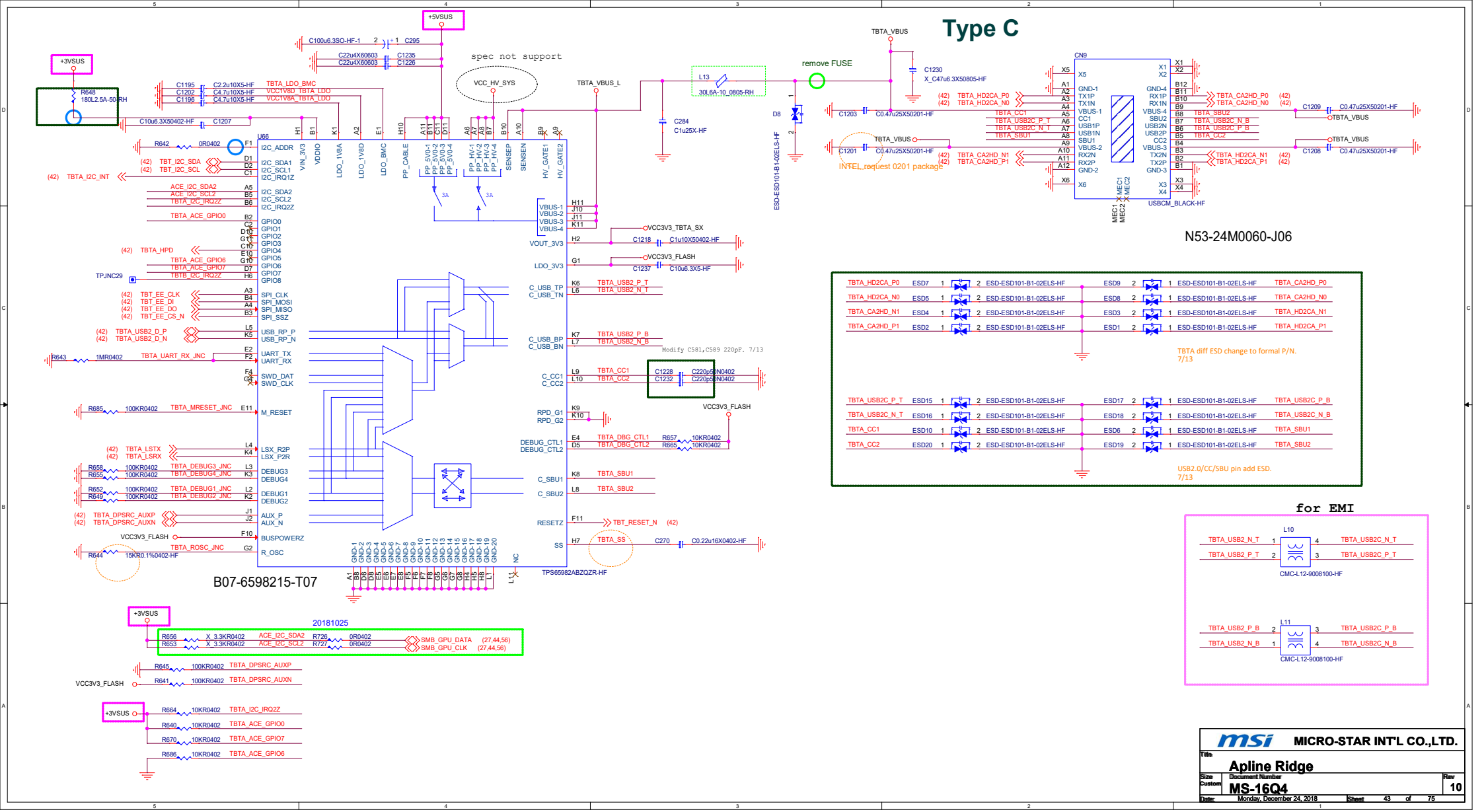
Type C
spec not support
remove FUSE
INTEL request 0201 package
N53-24M0060-J06
B07-6598215-T07
TPS65982ABZQZR-HF
USBCM_BLACK-HF
TBTA diff ESD change to formal P/N.
7/13
USB2.0/CC/SBU pin add ESD.
7/13
for EMI
CMC-L12-9008100-HF
20181025
Modify C581,C589 220pF. 7/13
MICRO-STAR INT'L CO.,LTD.
Apline Ridge
MS-16Q4
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KBC/EC/uP (ENE9028)

ENE9028 & 9048 Power Notes :

pin9 VCCLPC :
3.3V for ENE9028's LPC mode.
1.8V for ENE9048's eSPI mode.

pin111 VCC0 :
3.3V for ENE9028's PLC function
3.3V for ENE9048's eSPI operation with Pre-Driver.

When use ENE9048 eSPI mode
PCH's VCCPGPPA must be 1.8V

Hardware Reset

CN14 SW-TACTB1-6PS-RH-2
N71-0100900-D02
RST_SW# R688 100R1%0402 Close to SW
ECRST# C1244 C0.1u50X0402-HF
GND

PU/PD

R593 10KR0402 RSMRST#
R586 10KR0402 KBRST#
RSMRST# follow DG modify to 10K

+3VSUS
R608 2.2KR0402 EC_SCL3
R602 2.2KR0402 EC_SDA3
20171012

+3VALW
R666 10KR0402 LID#

+3VALW
R619 4.7KR0402 BATCLK_M
R612 4.7KR0402 BATDATA_M

+3VALW
RN3 8P4R-10KR0402 KBIN0 KBIN1 KBIN2 KBIN3
RN4 8P4R-10KR0402 KBIN4 KBIN5 KBIN6 KBIN7

+3VSUS
R577 100KR0402 AC_PRESENT
20170829 add R3528

remove OVERT# (Active Low)

LPC I/F

(36,45) INT_SERIRQ
(36,45) LPC_FRAME#
(36) CLK_PCI_KBC
(36) EC_CLKRUN#
(36,45) LAD0
(36,45) LAD1
(36,45) LAD2
(36,45) LAD3

FAN&PWM

ECRST#
(36) KBRST#
(36) KBSCI#
(38,39) HDMI_HPD_DET
(32) LPC_RST#
LEDKB_EN
20180604
(45) DGPU_FAN_PWM2
(58) AC_CTL
(35) FLASH_SECURITY
(45) CPU_FAN_PWM0
(45) DGPU_FAN_PWM1
(45) CPUFAN_FB0
(45) GPUFAN_FB1

IKB

KBOUT0 KBOUT1 KBOUT2 KBOUT3 KBOUT4 KBOUT5 KBOUT6 KBOUT7 KBOUT16 KBOUT17
(52) EC_IO1
20180802
(41) PANEL_OD
(58) BATT_EN
(58) BAT_IN#
(41,45) LID#
(61) SUSPWROK
LID#
TPJNC25 TPJNC26 EC_SDA EC_SCL
KBOUT8 KBOUT9 KBOUT10 KBOUT11 KBOUT12 KBOUT13 KBOUT14 KBOUT15

ESB

(47) EAPD
(49,50) EC_MUTE#

CIR

KBIN6 KBIN7
20170926
(60) DIMM_ON_2V5
(32) RTC_CTL

SPI FLASH

(36) SPI_MISO
(36) SPI_MOSI
(36) SPI_CLK
(36) SPI_CS0#

PS2 I/F

(55) TP_CLK
(55) TP_DATA
20171012
(48,49,50) AZ_I2C_SCL
(48,49,50) AZ_I2C_SDA
R609 22R0402 EC_SCL3
R603 22R0402 EC_SDA3
(58) BATCLK_M
(58) BATDATA_M

UART

(47) EC_HP_JD
(47) AZ_GPIO3_DSD
(40,59,61) RUN_ON
(32) PM_PWRBTN#
R576 0R0402

POWER/GROUND

VCC_LPC VCC VCC-1 VCC-2 VCC-3 VCC0 VCC_IO2
AVCC AGND GND GND-1 GND-2 GND-3 GND-4
R607 X_0R0402 +1_8VSUS
R611 0R0402 +3VALW
C1150 C0.1u16X0402
C1126 C1197 C1136 C1187 C0.1u16X0402

SMBUS

SDA0/GPIO45 SMB_GPU_DATA (27,43,56)
SCL0/GPIO44 SMB_GPU_CLK (27,43,56)
IEDI_SDA/SDA1/GPIO47 EC_SDA (39)
IEDI_SCL/SCL1/GPIO46 EC_SCL (39)
20170921
SMB_GPU_DATA R631 3.3KR0402
SMB_GPU_CLK R634 3.3KR0402

AD/DA

DA0/GPO3C EC_PCHPWROK (32)
DA1/GPO3D CAMERA_ON (41)
DA2/GPO3E DGPU_PWRGD (30,32)
DA3/GPO3F WLAN_PWRON (55)
20180103
AD0/GPI38 KBIN0
AD1/GPI39 KBIN1
AD2/GPI3A KBIN2
AD3/GPI3B KBIN3
AD4/GPI42 KBIN4
AD5/GPI43 KBIN5

SDI

GPXIOA00/GPIO60/SHICS# EC_SPI_CS (52)
GPXIOA01/GPIO61/SHICLK EC_SPI_CLK (52)
GPXIOA02/GPIO62/SHIDO EC_SPI_DO (52)

ALLSYSPG

POWER_FAIL0/GPIO63/GPXIOA03 SUS_ON (59)
GPIO64/GPXIOA04 GPUFAN_FB2 (45)
GPIO65/GPXIOA05 ADP_ICC (58)
VCOUT1/GPIO66/GPXIOA06 EC_PROCHOT#
VCOUT0/GPIO67/GPXIOA07 ALLSYSPG (2,32,35,62,65)
GPIO68/GPXIOA08 LED_CHARGE
GPIO69/GPXIOA09 LED_BATLOW
GPIO8A/GPXIOA10
GWG/GPIO8B/GPXIOA11 AC_PRESENT (32)
SDIDO/GPIO78/GPXIOD00 EC_SPI_DI (52)
GPIO79/GPXIOD01 AC_OK (58)
EC_EN#/GPIO7A/GPXIOD02 GPU_ACIN (27,58)
GPIO7B/GPXIOD03 PWR_SW# (45)
GPIO7C/GPXIOD04 1V8_AON_EN (30,66)
GPIO7D/GPXIOD05 DP_HPD (36,40)
GPIO7E/GPXIOD06 PECI_9048PWR
GPIO7F/PECI H_PECI_R
R574 43R0402 H_PECI (2)
R506 X_10KR0402 +3VSUS
for ENE9048 ,GPIO7E define PECI Power to VCCST

ESPI

GPIO04 ECESPI_RST#_R
i_clk_8051/GPIO07
PROCHOT#/i_clk_peri/GPIO08
POWER_FAIL1/GPIO18
GPIO50 SCI_WAKE_UP# (34)
GPIO52 EC_PCH_PWROK (32)
WDT_LED#/GPIO54 GPIO_LID (55) USB_ENABLE (56)
GPIO56 PWR_LED#
XCLK32K/GPIO57 RSMRST# (32)
GPIO59 PM_SLP_S3# (2,6,32,42,59,60,62,65)
PM_SLP_S4# (6,32,60)
R618 X_0R0402 ECESPI_RST# (36)
20180723

LED

GPIO1A/NUMLED#
GPIO53/CAPSLED#
GPIO55/SCROLED#
LED_CAP
CAMERA_LED_ON

EC_PCH_PWROK

GPIO18 : ALLSYSPG delay 99ms to generated EC_PCH_PWROK
+3VSUS
R581 10KR0402
R590 10KR0402
PWR_LED# Q65 N-BSS138LT1G_SOT23-3-RH
PWR_LED (45)
20180808

EC_PROCHOT#

+3VSUS
C1094 C0.1u16X0402
R553 10KR0402 EC_PROCHOT#
U56 SN74AUP1G07DCKR_SC70-5-RH
OPEN DRAIN
TO BUFFER OUTPUT
20170814 add net name H_PROCHOT#_BUF
R548 75R1%0402 H_PROCHOT# (2,58,62)
C1084 C47p50N0402-RH

LED Board

+5VALW GND
FPC3
LED_BATLOW
LED_CHARGE
20181016
FPC6P-TB-0.5PITCH_WHITE-HF
N5A-06F0390-A81

Pin1 to Pin1

+5VRUN
(5-2.95) / 68 = 30.1 mA
30.1 X 8 = 241.1 mA
KBLED2
X_FPC6P-TB-0.5PITCH_WHITE-HF
N5A-06F0390-A81
FPC_S6_0_5MM
KB_LED_R#
Q68 X_AO3404
D03-0340409-A68
SOT23SGD_T
LEDKB_EN

FOR WS

(All stuff)
20180604

KB1

FPC30P-TB-0.5PITCH_WHITE-HF
N5A-30F0230-A81
+5VRUN
CAMERA_LED_ON#
LED_CAP#
KBOUT17 KBOUT16 KBIN0 KBIN1 KBIN2 KBIN3 KBIN4 KBIN5 KBIN6 KBIN7 KBOUT15 KBOUT14 KBOUT13 KBOUT12 KBOUT11 KBOUT10 KBOUT9 KBOUT8 KBOUT7 KBOUT6 KBOUT5 KBOUT4 KBOUT3 KBOUT2 KBOUT1 KBOUT0
20170920
Copy 16Q1

For EMI

EC17 KBOUT7 KBOUT6 KBOUT5 KBOUT4
EC16 KBOUT3 KBOUT2 KBOUT1 KBOUT0
EC18 KBOUT11 KBOUT10 KBOUT9 KBOUT8
EC19 KBOUT15 KBOUT14 KBOUT13 KBOUT12
8p4C-100p50N0402-RH
KBOUT16 PC257 C100p16X0402
KBOUT17 PC258 C100p16X0402

VCC : +5 V
LED Vf 2.95~3.45V

	Min(LED Vf : 3.45V)	Max(LED Vf : 2.95V)
LED Current	172 mA	252 mA

Q36

LED_CAP CAMERA_LED_ON
Q36 NN-BSS138DW-7-F_SOT363-6-RH
D2 LED_CAP#_R R281 0R0402 LED_CAP#
D1 CAMERA_LED_ON#_R R254 0R0402 CAMERA_LED_ON#
X_ESD-DIODE ED2 ED1 GND
20170920
Copy 16Q1

Title	KBC/EC/uP (ENE9028)
Size	C
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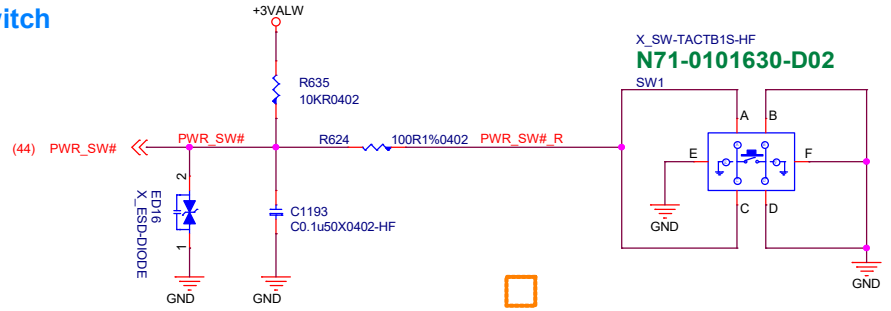
MICRO-STAR INT'L CO.,LTD.

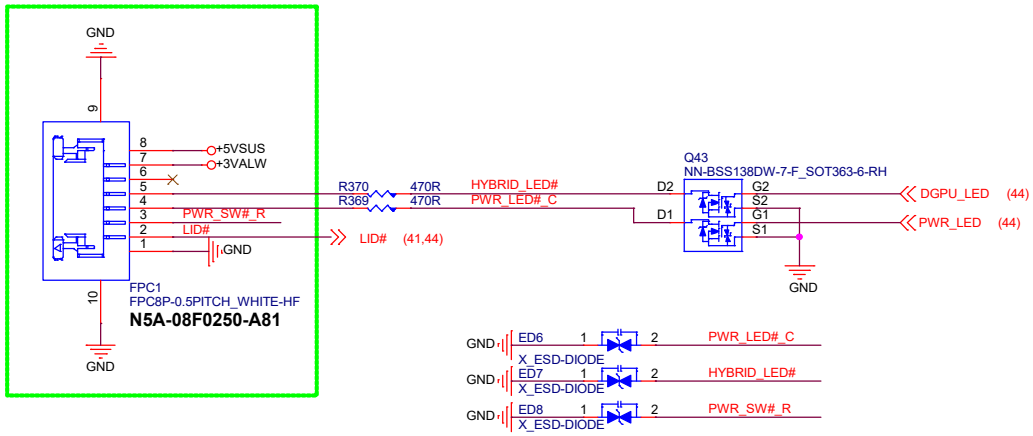
PWR SW/CPU FAN/BTB CONN/ LED CONN

Power Switch



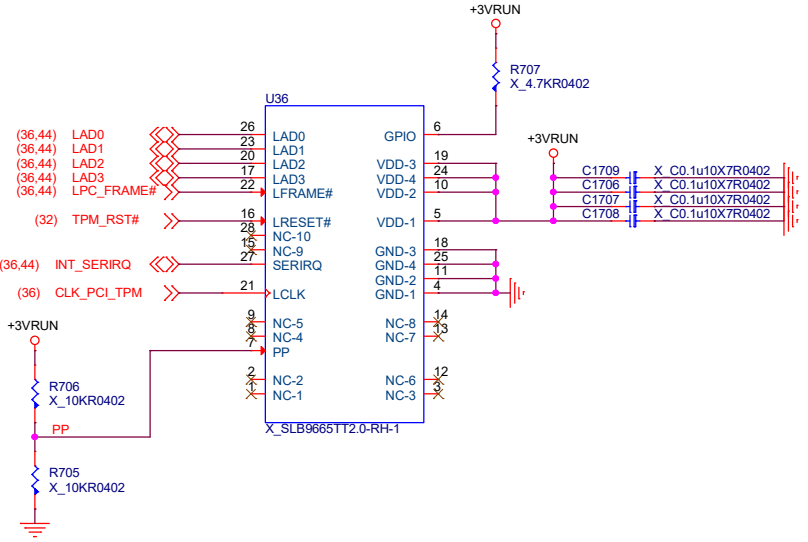
Power LED+SW+FP

20181016

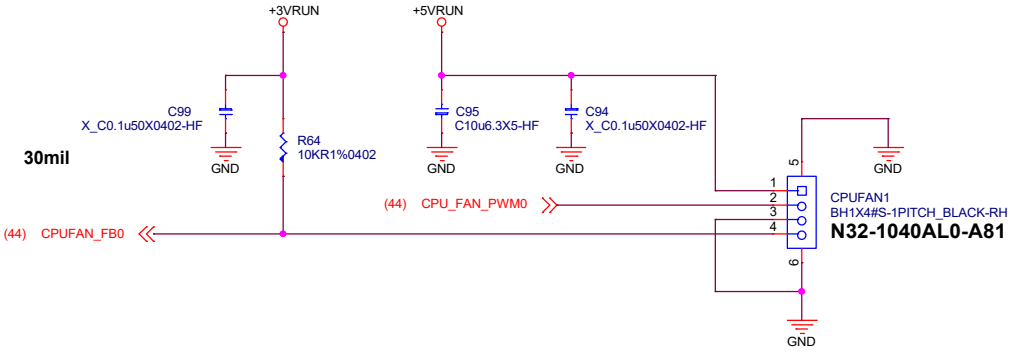


TPM

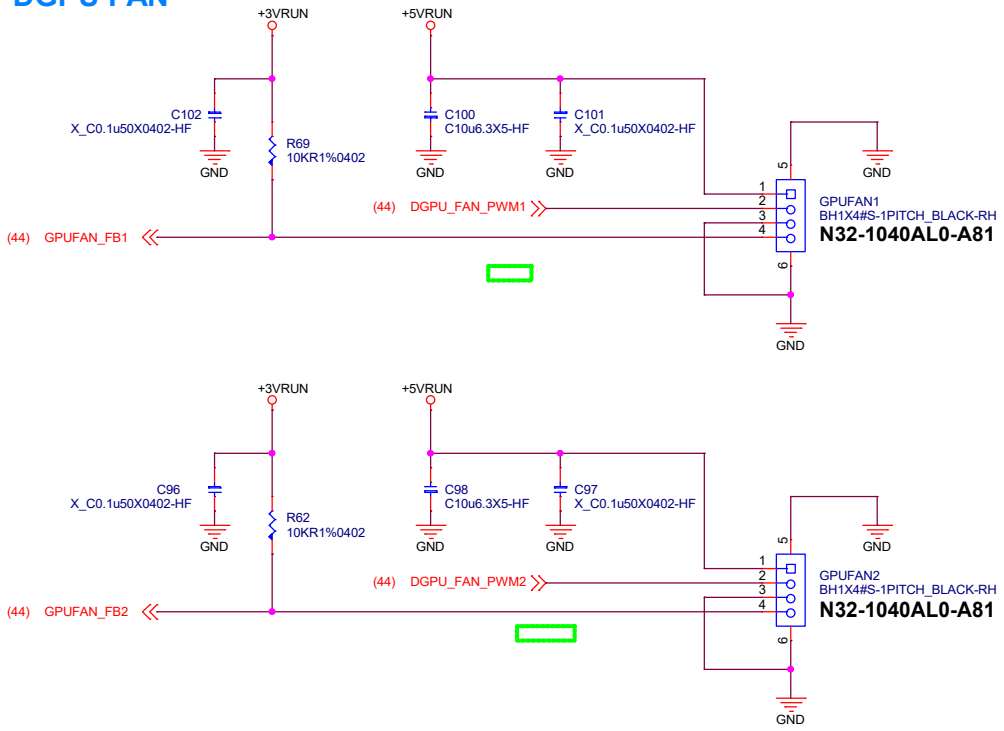
20180802



CPU FAN



DGPU FAN



MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN/LED/PWR SW/TPM

Size	Document Number	Rev
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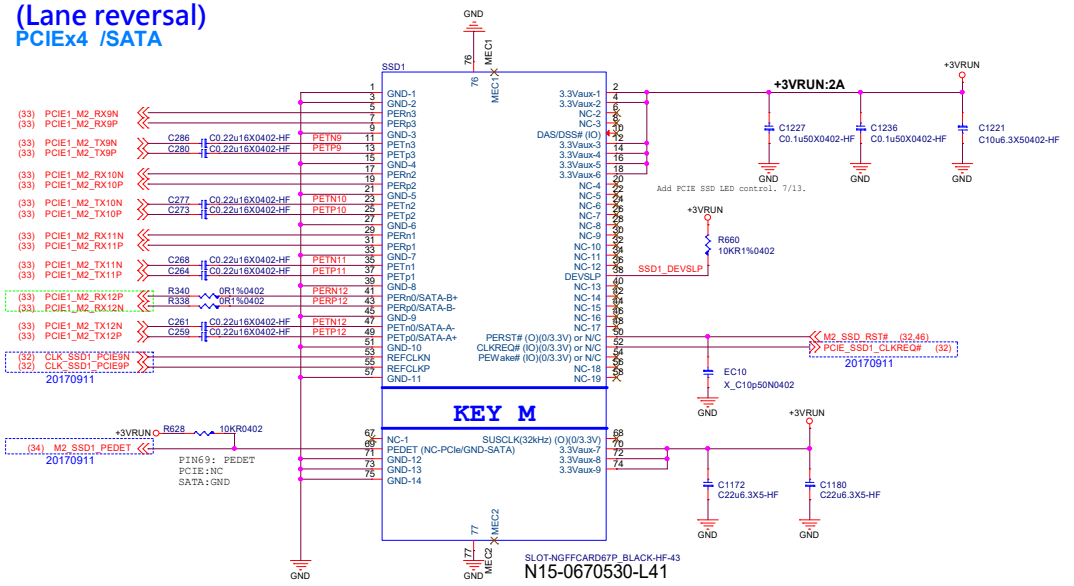
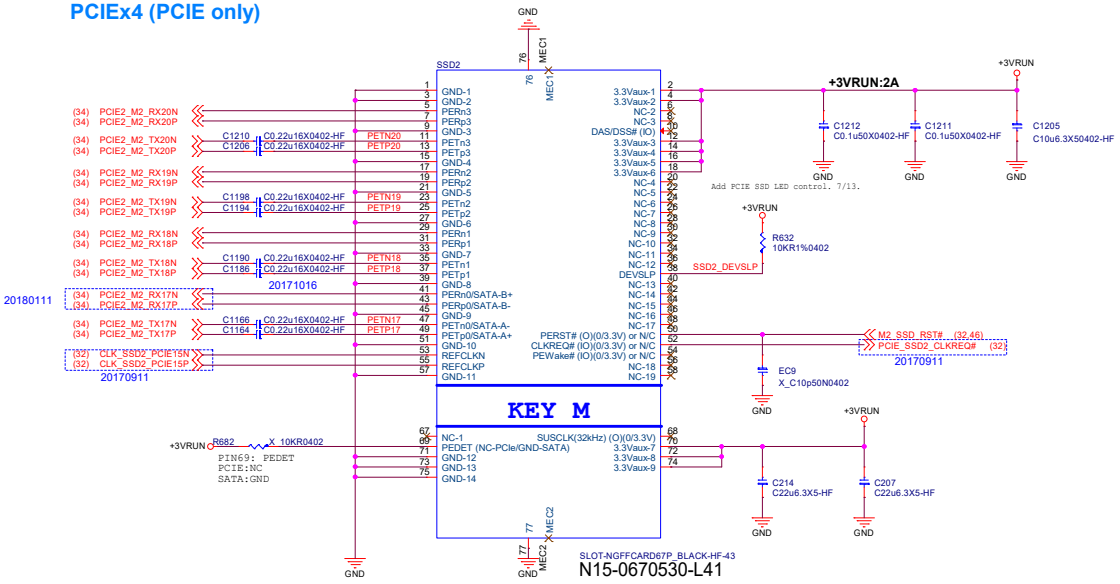
M2 SSD -1
(Lane reversal)
PCIEx4 /SATA



M2 SSD -2
PCIEx4 (PCIE only)



MICRO-STAR INT'L CO.,LTD.	
Title:	M2 SSD/TPM
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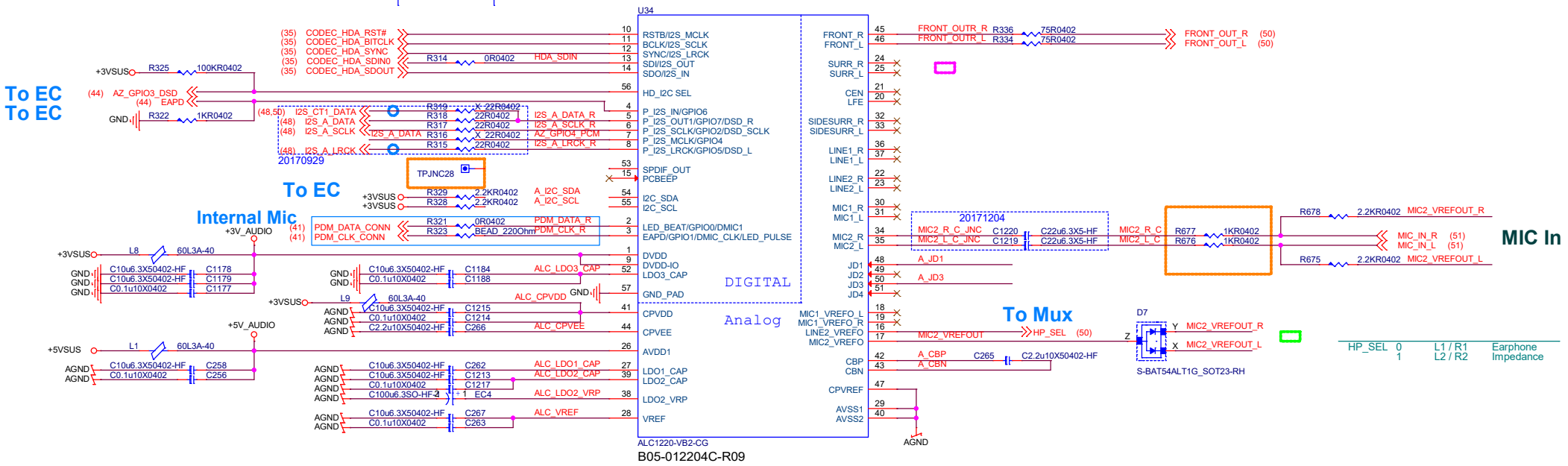
AUDIO(ALC1220)

ALC1220	AZ_GPIO3_DSD
PCM	H
DSD	L



Title	Audio(ALC1220-VB2)
Size	Custom
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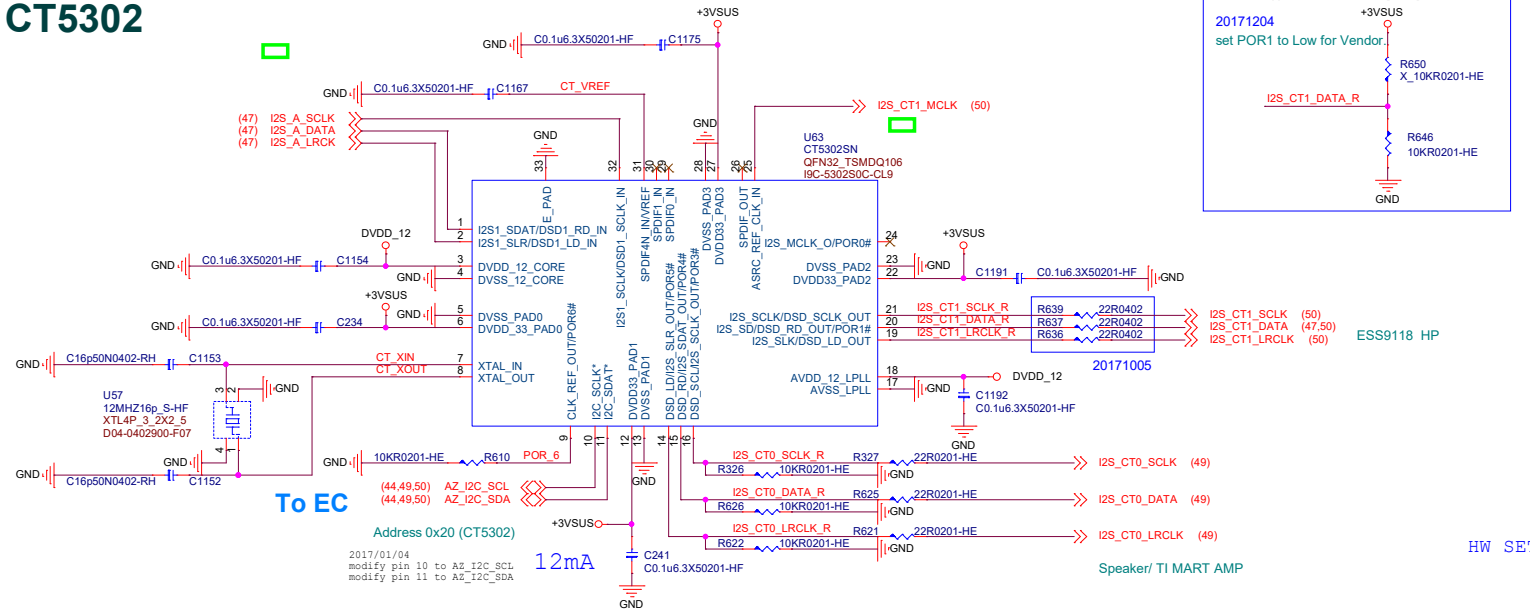
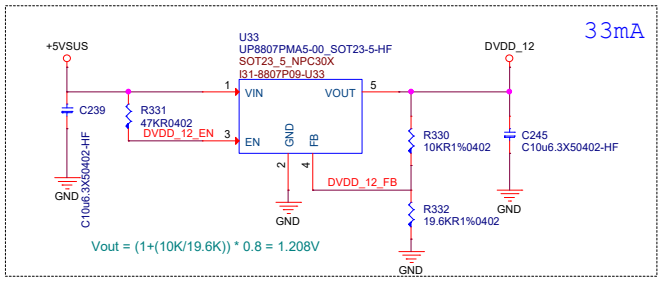
MICRO-STAR INT'L CO.,LTD.

CT5302





Pin Name	Description	Function Table
POR_IN_1	POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	Select I2S1 output port is master or slave mode
POR_IN_3 POR_IN_4	POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	Select Crystal frequency
POR_IN_5 POR_IN_6	POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	I2C serial interface device ID selection

HW SETTING

I2S output slave mode:

Select I2S1 output port

No.	POR1	Definition
0	0	I2S output master mode
1	1	I2S output slave mode

HW SETTING

Hardware Crystal:

Select current external crystal frequency

No	POR4	POR3	Definition
0	0	0	12.0000MHz
1	0	1	11.2896MHz
2	1	0	12.2880MHz
3	1	1	14.3180MHz

HW SETTING

I2C Slave ID

Define chip I2C slave address

No	POR6	POR5	Definition
0	0	0	0x20
1	0	1	0x22
2	1	0	0x24
3	1	1	0x26

MICRO-STAR INT'L CO.,LTD.

Title: CT5302

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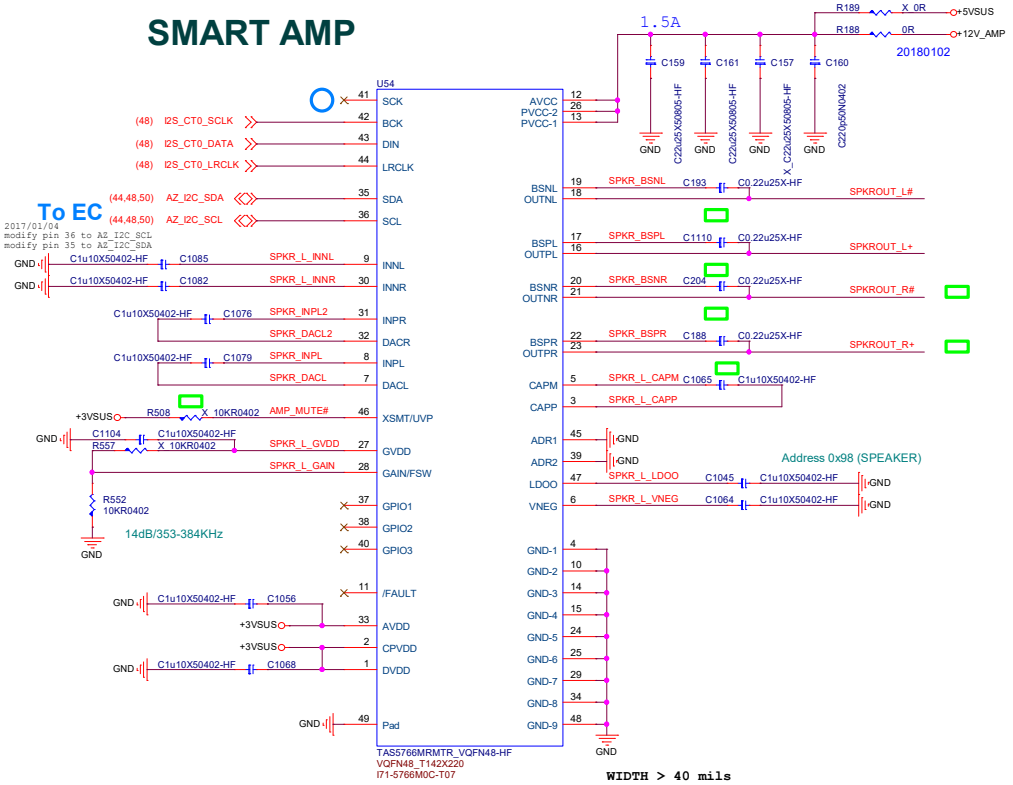
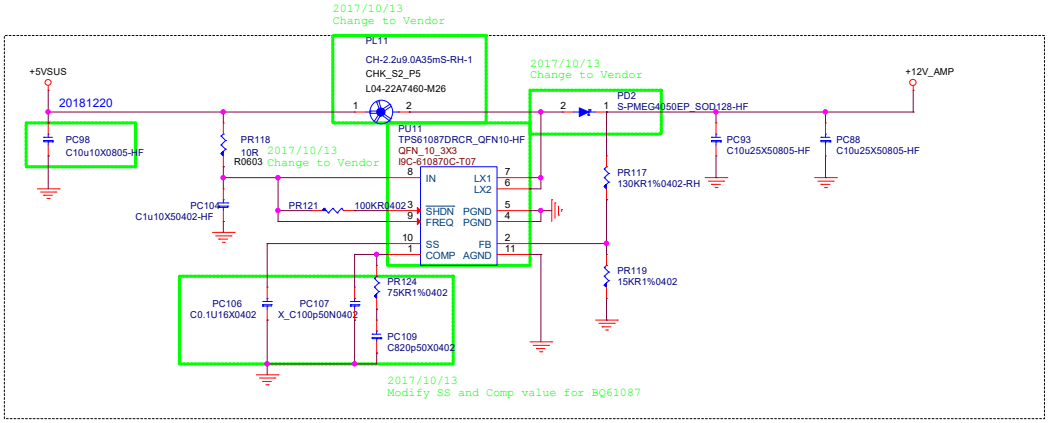
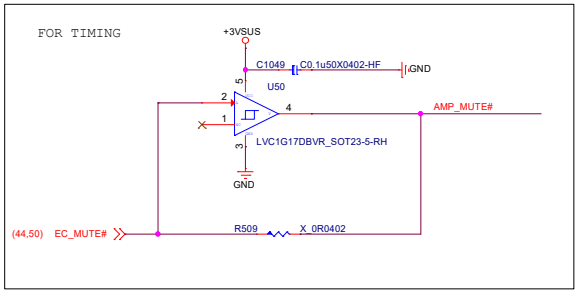
SMART AMP

WIDTH > 40 mils



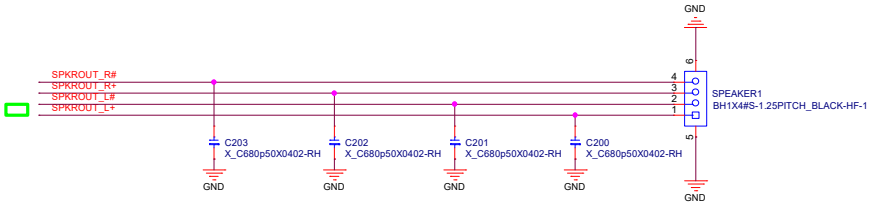
WIDTH > 40 mils





CON TO BE CONFIRM

SPK Conn



MICRO-STAR INT'L CO.,LTD.

Title	SMART AMP	
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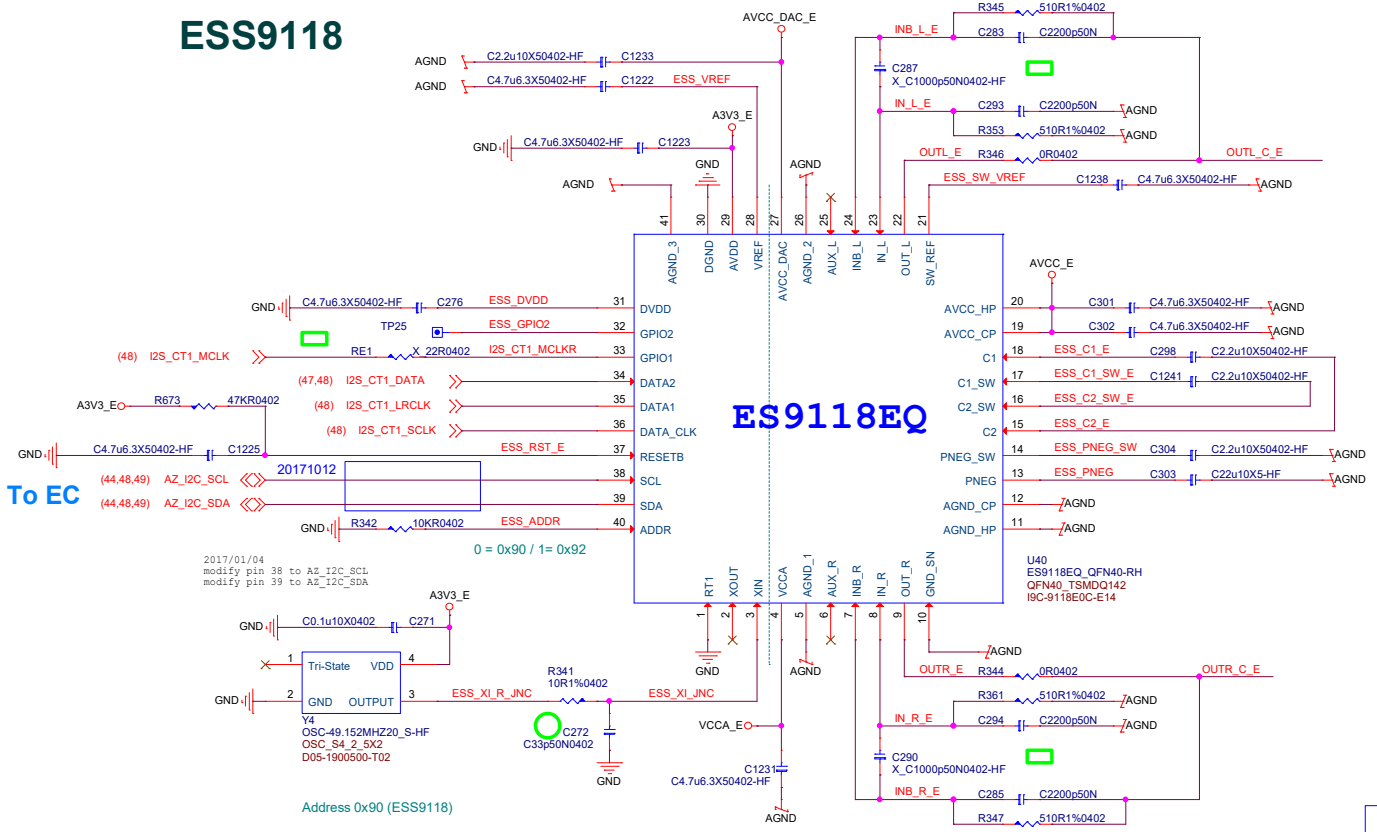
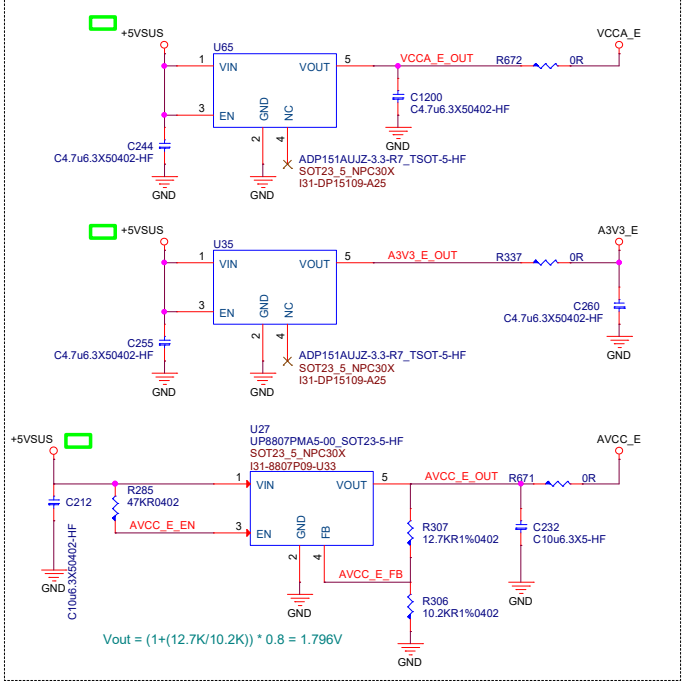
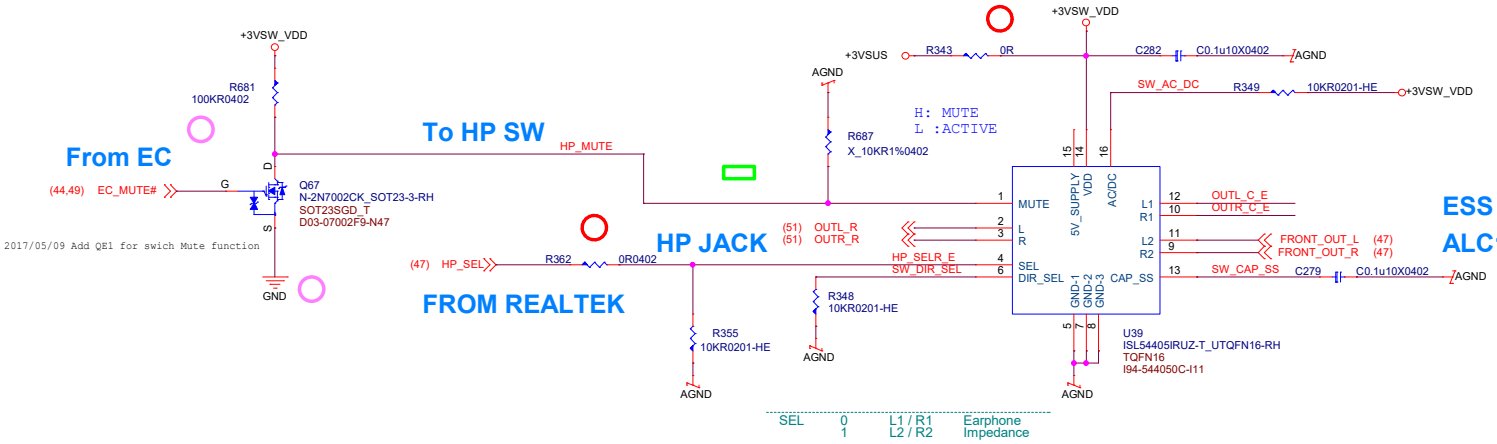
ESS9118



Power



Audio MUX



Truth Table

INPUTS				OUTPUTS				
AC/DC	DIR	MUTE	SEL	L1, R1	L2, R2	COM (L,R) C/P Shunts	L1, R1 C/P Shunts	L2, R2 C/P Shunts
0	X	0	0	ON	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON
1	0	0	1	OFF	ON	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF
1	1	1	X	OFF	OFF	ON	OFF	OFF

NOTE: MUTE, AC/DC, DIR: Logic "0" ≤ 0.5V, Logic "1" ≥ 1.4V or Float with a 3.3V Supply or 5V supply.
SEL: Logic "0" ≤0.5V, Logic "1" ≥ 1.4V with a 3.3V Supply or 5V supply.
X = Don't Care

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Title	ESS Audio (ES9118EQ)
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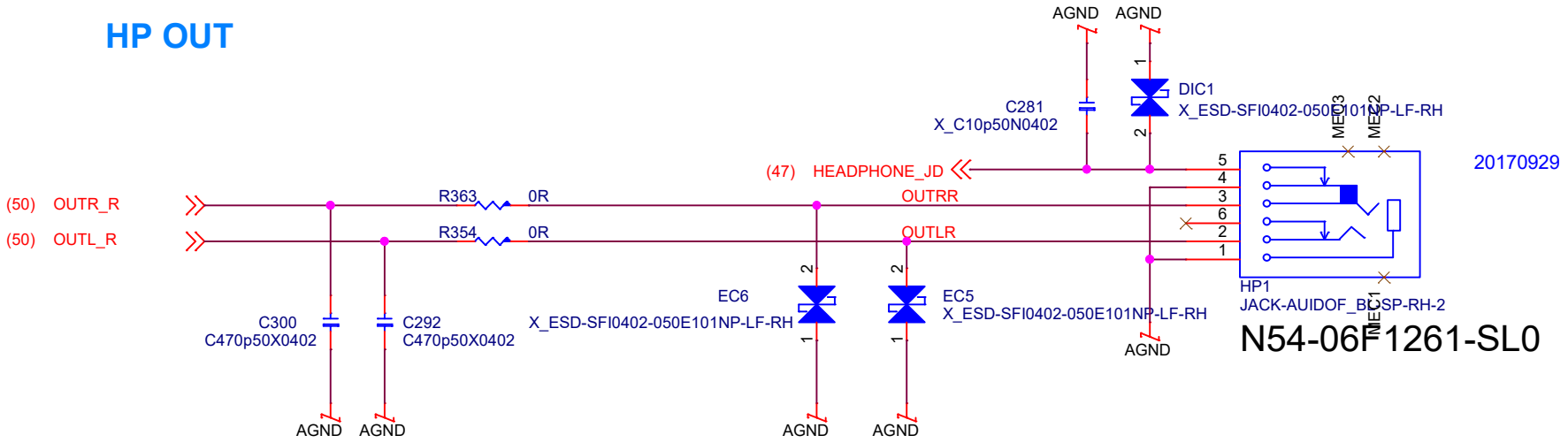
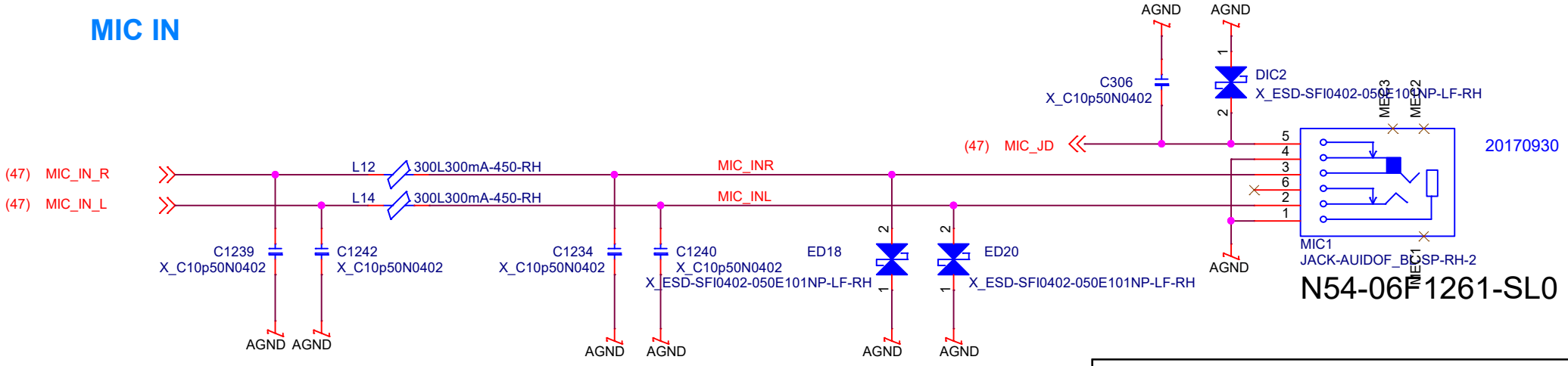
Audio CONN

HP OUT



MIC IN



MICRO-STAR INT'L CO.,LTD.		
Title: Audio Jack		
Size: Custom	Document Number: MS-16Q4	Rev: 10
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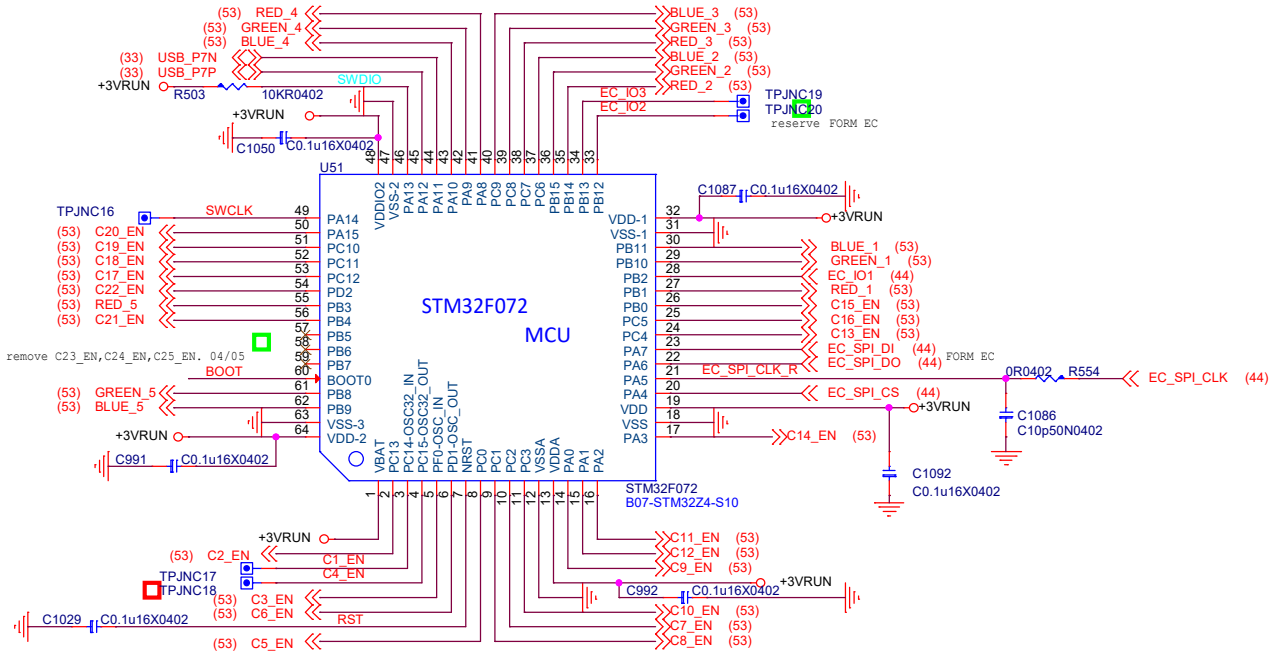
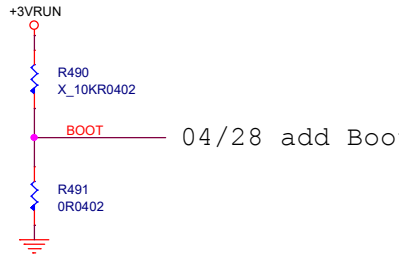
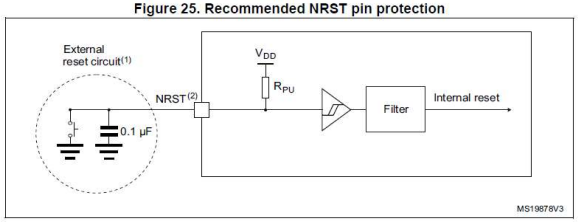




04/28 add Boot net and resistor

Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 56: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

MICRO-STAR INT'L CO.,LTD.

Title: MCU/Matrix

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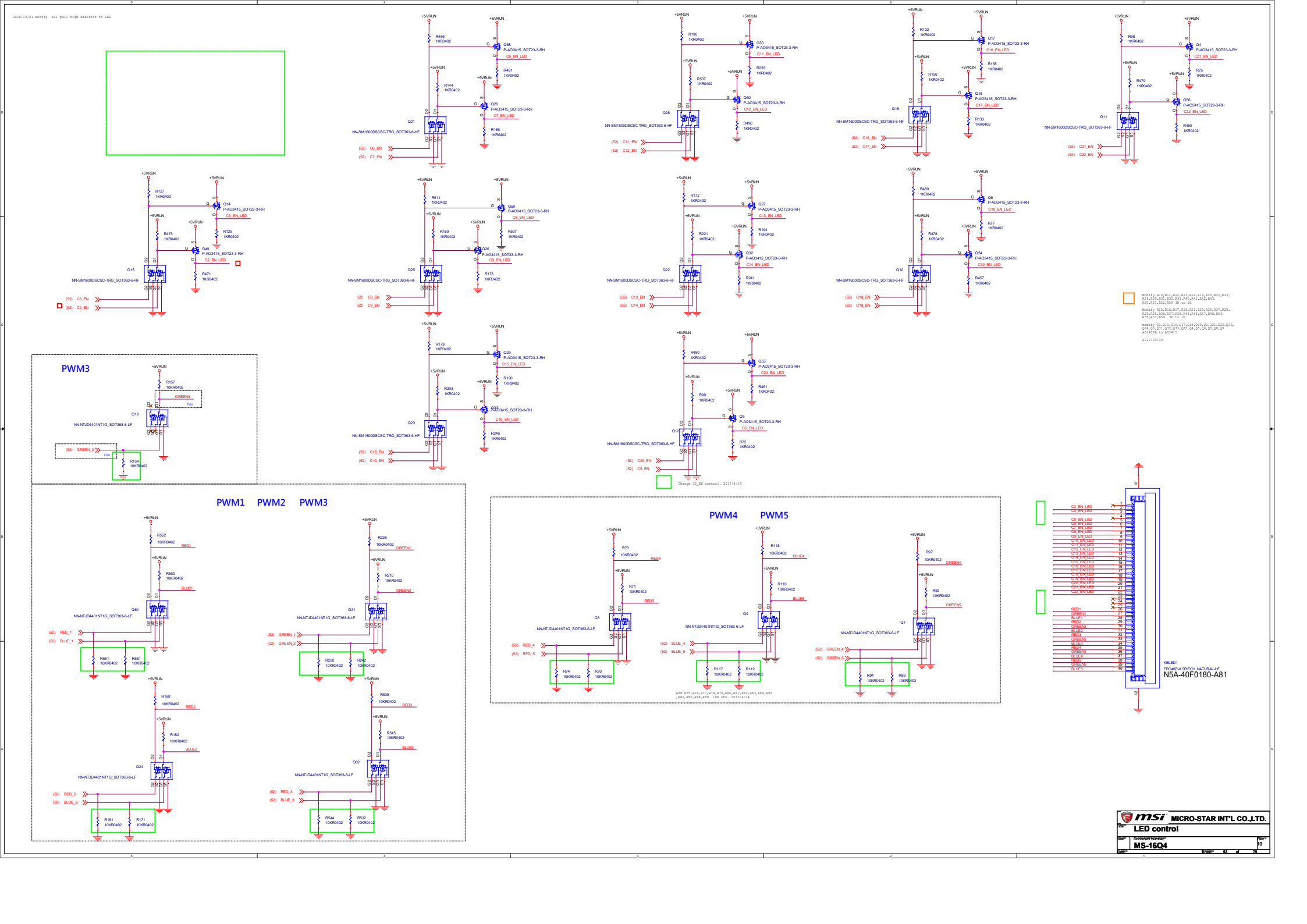

2016/12/01 modify all pull high resistor to 1KR
PWM3
PWM1 PWM2 PWM3
PWM4 PWM5
Change C5_EN control. 2017/4/14
Add R75,R76,R77,R78,R79,R80,R81,R82,R83,R84,R85 ,R86,R87,R88,R89 10K ohm. 2017/4/14
Modify R10,R11,R12,R13,R14,R19,R20,R22,R23, R24,R30,R31,R32,R33,R40,R41,R42,R45, R50,R51,R52,R56 3K to 1K
Modify R15,R16,R17,R18,R21,R25,R26,R27,R28, R29,R34,R35,R36,R37,R38,R43,R44,R46,R47,R48,R54, R55,R57,R58 10K to 1K
modify Q1,Q11,Q14,Q17,Q18,Q19,Q2,Q21,Q22,Q23, Q24,Q3,Q31,Q32,Q33,Q35,Q4,Q5,Q6,Q7,Q8,Q9 AO3407A to AO3415
2017/04/19
K8LED1
FPC40P-0.5PITCH NATURAL-HF
N5A-40F0180-A81
MICRO-STAR INT'L CO.,LTD.
LED control
MS-16Q4
REV 1.0
Sheet 53 of 75

	PWM1	PWM2	PWM3	PWM4	PWM5
MCU_C1_EN					
MCU_C2_EN		P			F3
MCU_C3_EN			PgUp	F4	INS
MCU_C4_EN					
MCU_C5_EN		RIGHT	UP	DOWN	LEFT
MCU_C6_EN		F5	PgDn	F6	DEL
MCU_C7_EN	F8	CAP	A	S	D
MCU_C8_EN	F9	TAB	Q	W	E
MCU_C9_EN	F10	CTRL_L	WIN_L	ALT_L	K131
MCU_C10_EN	F11	SHI_L	|\(K45)	Z	X
MCU_C11_EN	V	B	N	M	<,
MCU_C12_EN	F12	SPACE	3#	K132	C
MCU_C13_EN	>.	/?	K56	SHI_R	ENT
MCU_C14_EN	K133	ALTR	SS(Fn)	2@	CTR_R
MCU_C15_EN	F	G	H	J	K
MCU_C16_EN	L	:;	"'	K42	|\(K29)
MCU_C17_EN	O	F7	{[	}]	BACK
MCU_C18_EN	R	T	Y	U	I
MCU_C19_EN	9(	0)	-_	+=	k14
MCU_C20_EN	4$	5%	6^	7&	8*
MCU_C21_EN	`~	1!	ESC	F1	F2
MCU_C22_EN	PAUSE	SCR	PRT		
MCU_C23_EN					
MCU_C24_EN					
MCU_C25_EN					

Mapping to
KBC's KBIN & KBOUT

KBIN_3,KBOUT_9	KBIN_6,KBOUT_5	KBIN_7,KBOUT_5	KBIN_7,KBOUT_4	KBIN_6,KBOUT_9
KBIN_3,KBOUT_5		KBIN_4,KBOUT_9	KBIN_5,KBOUT_9	
KBIN_1,KBOUT_12	KBIN_2,KBOUT_5	KBIN_6,KBOUT_12	KBIN_4,KBOUT_12	KBIN_2,KBOUT_12
KBIN_2,KBOUT_9	KBIN_4,KBOUT_5	KBIN_5,KBOUT_5	KBIN_5,KBOUT_4	KBIN_7,KBOUT_9
KBIN_6,KBOUT_4	KBIN_4,KBOUT_4	KBIN_1,KBOUT_4	KBIN_2,KBOUT_4	KBIN_0,KBOUT_4
KBIN_3,KBOUT_4		KBIN_7,KBOUT_12	KBIN_5,KBOUT_12	KBIN_3,KBOUT_12
	KBIN_0,KBOUT_13	KBIN_4,KBOUT_0	KBIN_5,KBOUT_0	KBIN_4,KBOUT_1
	KBIN_1,KBOUT_3	KBIN_2,KBOUT_0	KBIN_3,KBOUT_0	KBIN_2,KBOUT_1
	KBIN_3,KBOUT_3	KBIN_7,KBOUT_13	KBIN_4,KBOUT_3	KBIN_2,KBOUT_13
	KBIN_2,KBOUT_3	KBIN_0,KBOUT_9	KBIN_6,KBOUT_0	KBIN_7,KBOUT_0
KBIN_7,KBOUT_1	KBIN_6,KBOUT_2	KBIN_7,KBOUT_2	KBIN_6,KBOUT_6	KBIN_7,KBOUT_6
	KBIN_5,KBOUT_3		KBIN_5,KBOUT_13	KBIN_6,KBOUT_1
KBIN_6,KBOUT_7	KBIN_7,KBOUT_7	KBIN_6,KBOUT_8	KBIN_7,KBOUT_8	KBIN_1,KBOUT_5
KBIN_6,KBOUT_13	KBIN_6,KBOUT_3	KBIN_1,KBOUT_13	KBIN_3,KBOUT_13	KBIN_7,KBOUT_3
KBIN_5,KBOUT_1	KBIN_4,KBOUT_2	KBIN_5,KBOUT_2	KBIN_4,KBOUT_6	KBIN_5,KBOUT_6
KBIN_4,KBOUT_7	KBIN_5,KBOUT_7	KBIN_4,KBOUT_8	KBIN_5,KBOUT_8	KBIN_0,KBOUT_5
KBIN_2,KBOUT_7		KBIN_2,KBOUT_8	KBIN_3,KBOUT_8	KBIN_0,KBOUT_12
KBIN_3,KBOUT_1	KBIN_2,KBOUT_2	KBIN_3,KBOUT_2	KBIN_2,KBOUT_6	KBIN_3,KBOUT_6
KBIN_0,KBOUT_7	KBIN_1,KBOUT_7	KBIN_0,KBOUT_8	KBIN_1,KBOUT_8	KBIN_1,KBOUT_9
KBIN_1,KBOUT_1	KBIN_0,KBOUT_2	KBIN_1,KBOUT_2	KBIN_0,KBOUT_6	KBIN_1,KBOUT_6
		KBIN_0,KBOUT_10	KBIN_1,KBOUT_10	KBIN_2,KBOUT_10
	KBIN_0,KBOUT_3	KBIN_0,KBOUT_0	KBIN_1,KBOUT_0	KBIN_0,KBOUT_1
KBIN_0,KBOUT_11	KBIN_1,KBOUT_11	KBIN_2,KBOUT_11	KBIN_3,KBOUT_11	KBIN_4,KBOUT_11
KBIN_3,KBOUT_10	KBIN_4,KBOUT_10	KBIN_5,KBOUT_10	KBIN_6,KBOUT_10	KBIN_7,KBOUT_10
KBIN_3,KBOUT_7		KBIN_7,KBOUT_11	KBIN_6,KBOUT_11	KBIN_5,KBOUT_11

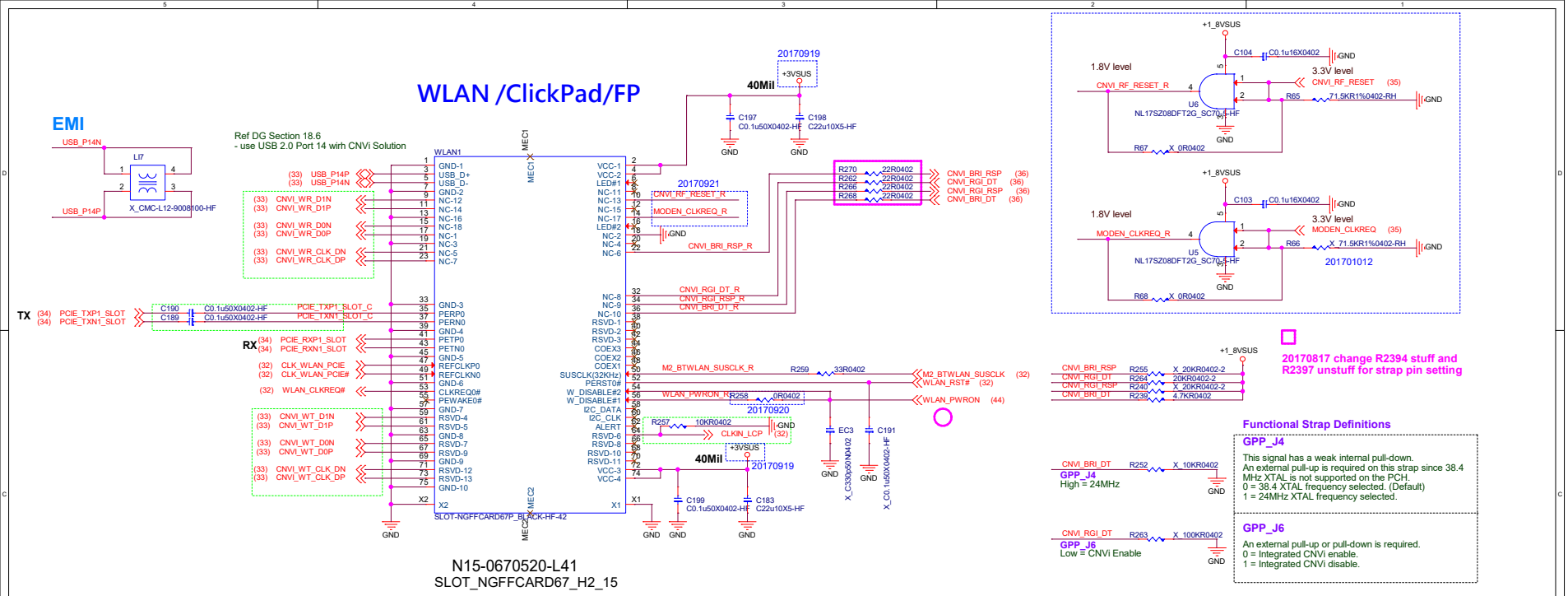
MICRO-STAR INT'L CO.,LTD.

Title: Keyboard Matrix

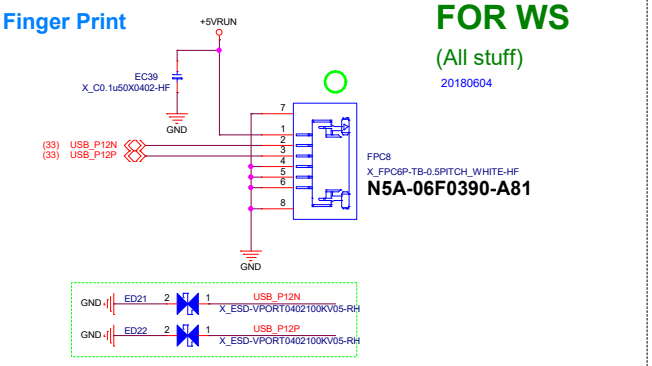
Size | Document Number: MS-16Q4 | Rev: 10

Date: | Sheet 54 of 75

WLAN /ClickPad/FP



Finger Print

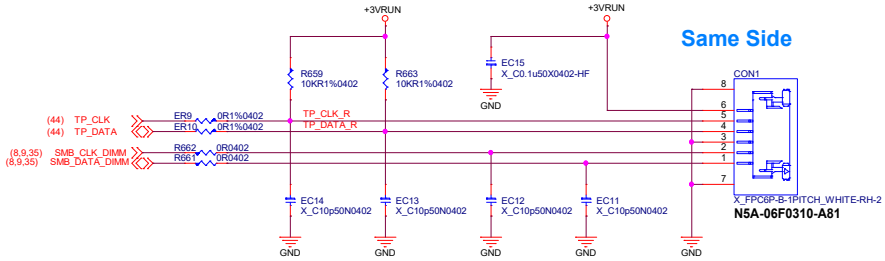


FOR WS

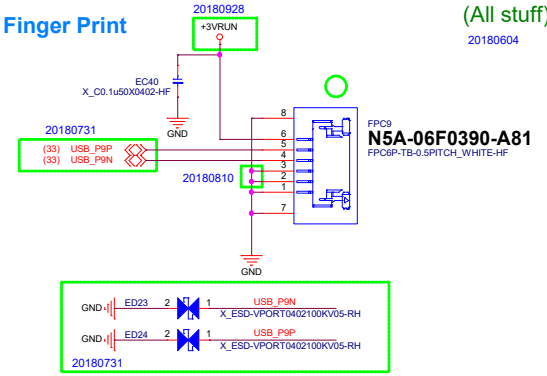
(All stuff)

20180604

Click Pad



Finger Print

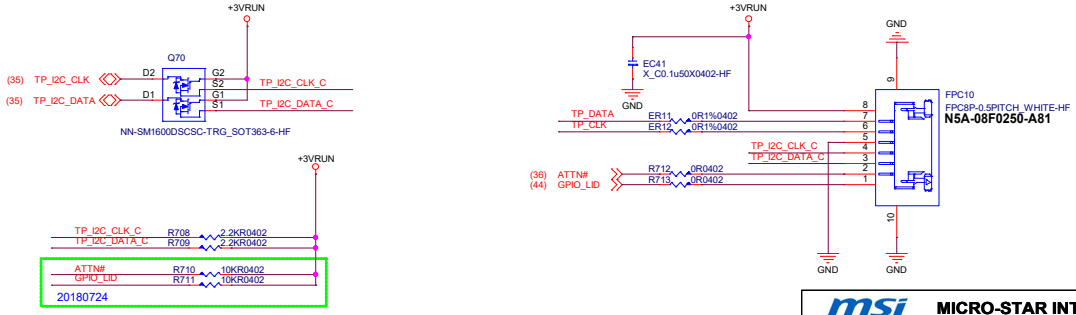


FOR 16Q4

(All stuff)

20180604

FOR 16Q4



msi	MICRO-STAR INT'L CO.,LTD.		
Title	WLAN /ClickPad/FP		
Size: Custom	Document Number: MS-16Q4	Rev: 10	
Date: Monday, December 24, 2018	Sheet 55 of 75		

USB3.0 CNT-1/-2/-3

USB3.1 Gne2 Retimer

I93-M15620C-AD0

EC

Strap

MODE : mode select
H = ATE Test mode
M = Strapping mode
L = I2C mode (v)

SSC_EN : Spread Spectrum
H = SSC enable
L = SSC disable(v)

I2C Mode : I2C Address
EQB = Address 1 ; SWB = Address 2
LL = 78

24MHz Clock

+1_2VSUS

MAX 1A

USB3.0 CNT-3

USB3.0 Port-2
USB2.0 Port-4

N53-09M1071-AF2

Note: CMC-L12-9008100-HF(P/N : L12-9008100-I05) 's Default Orcad library and footprint FILTER_84_1_25X1 are not match datasheet.

Datasheet | Orcad library | Footprint

USB Power Switch

I36-5478102-G07
GMT

ESD

ESD-STSU0504F-HF

EMI

Y01-REMPAS1-000

EMI Check

USB3.0 CNT-2

USB3.0 Port-1
USB2.0 Port-5

N53-09M1071-AF2

USB Power Switch

I36-5478102-G07
GMT

ESD

ESD-STSU0504F-HF

USB3.0 CNT-1

USB3.0 Port-4
USB2.0 Port-2

N53-09M1071-AF2

USB Power Switch

I36-5478102-G07
GMT

ESD

ESD-STSU0504F-HF

MICRO-STAR INT'L CO.,LTD.

Title: USB3.0 CNT-1/-2/-3

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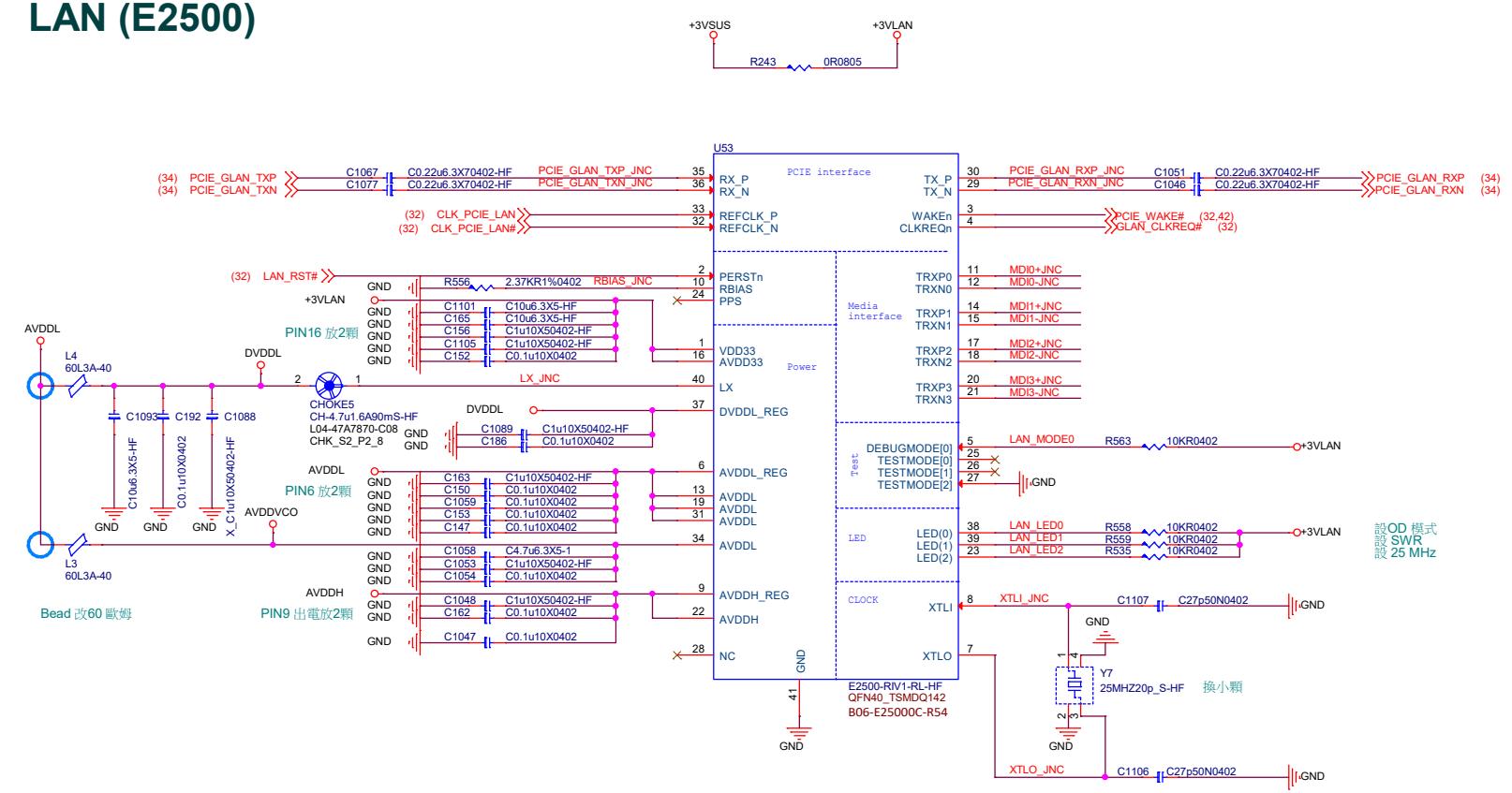
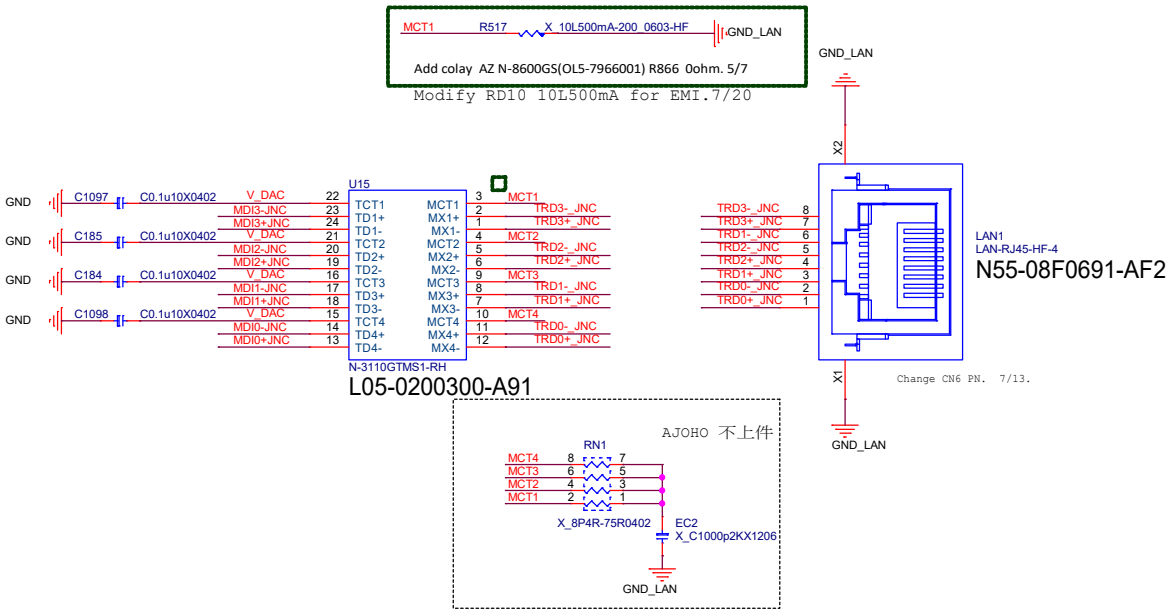
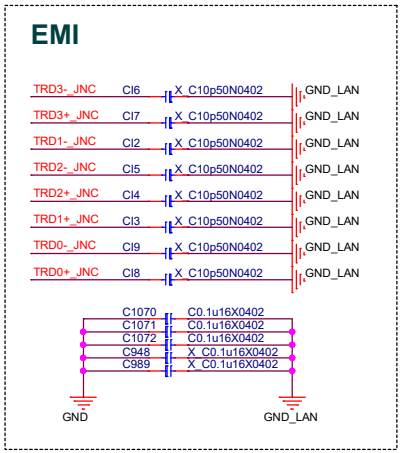
LAN (E2500)







msi	MICRO-STAR INT'L CO.,LTD.		
Title	GIGA_LAN(E2500)		
Size: Custom	Document Number: MS-16Q4	Rev: 10	
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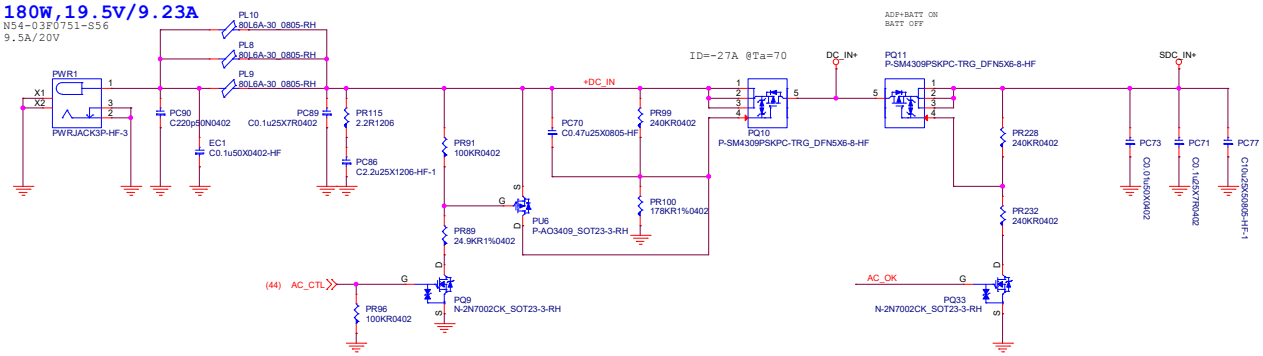
N92-03M0941-SL0

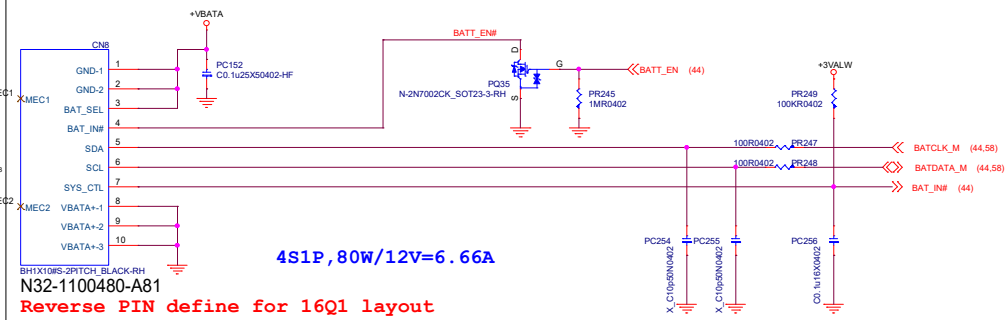
180W,19.5V/9.23A

N54-03F0751-S56

9.5A/20V



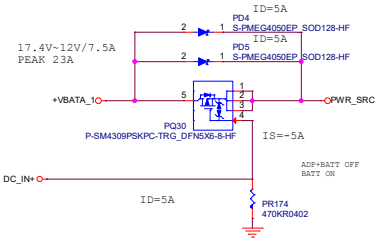
AC_OK#	GPU_ACIN (EC control)	GPIO12_GPU_ACIN
0	0	AC
0	1	AC
1	0	AC
1	1	DC

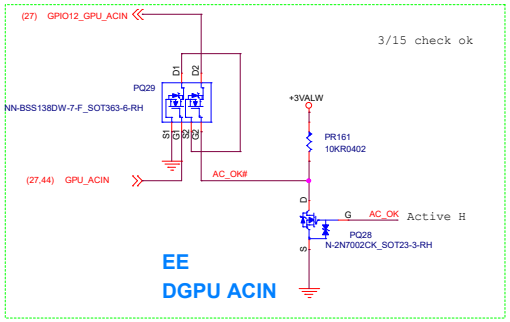


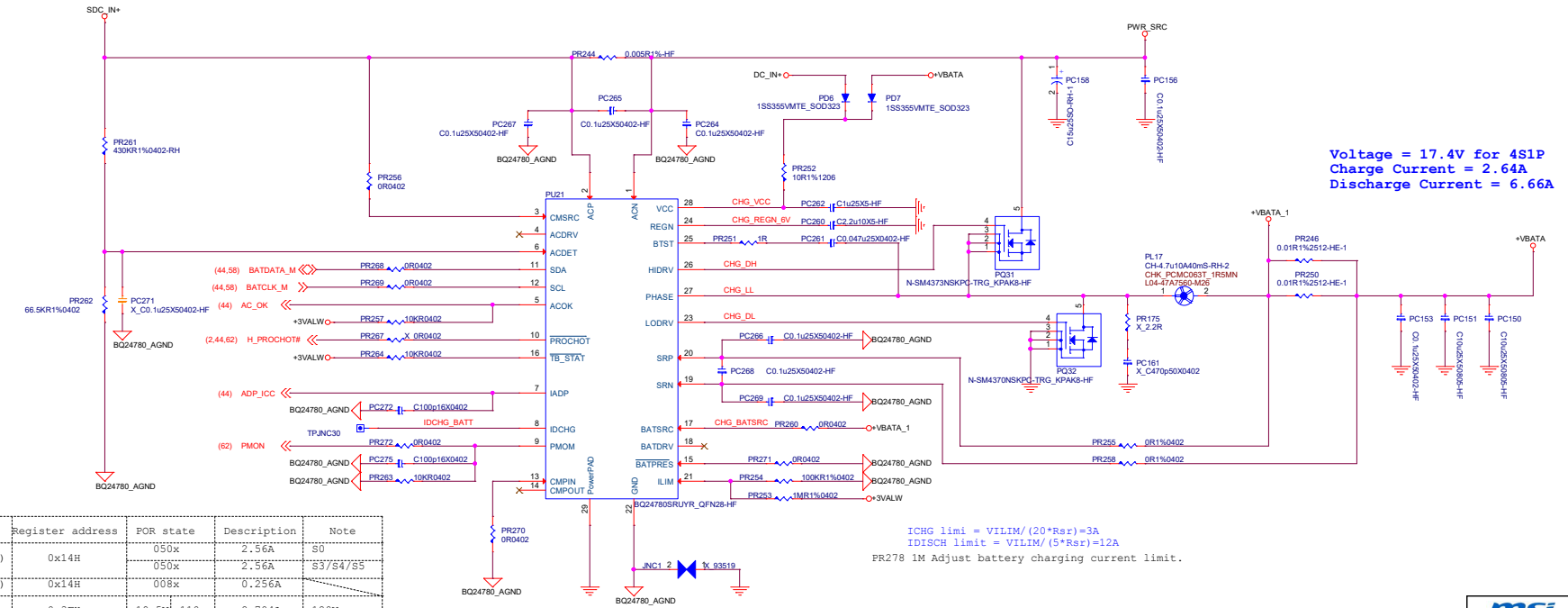
4S1P,80W/12V=6.66A

N32-1100480-A81

Reverse PIN define for 16Q1 layout







Voltage = 17.4V for 4S1P
Charge Current = 2.64A
Discharge Current = 6.66A

ICHG limi = VILIM/(20*Rsr)=3A
IDISCH limit = VILIM/(5*Rsr)=12A
PR278 1M Adjust battery charging current limit.

Register name	Register address	POR state	Description	Note
Charge current(5mR)	0x14H	050x	2.56A	S0
		050x	2.56A	S3/S4/S5
Prepare charge(5mR)	0x14H	008x	0.256A	
Input current(5mR)	0x3FH	19.5V 110x	8.704A	180W
Charge voltage	0x15H	43Fx	17.392V	4S1P
Discharge current(5mR)	0x39H	080x	4.096A	BOOST current

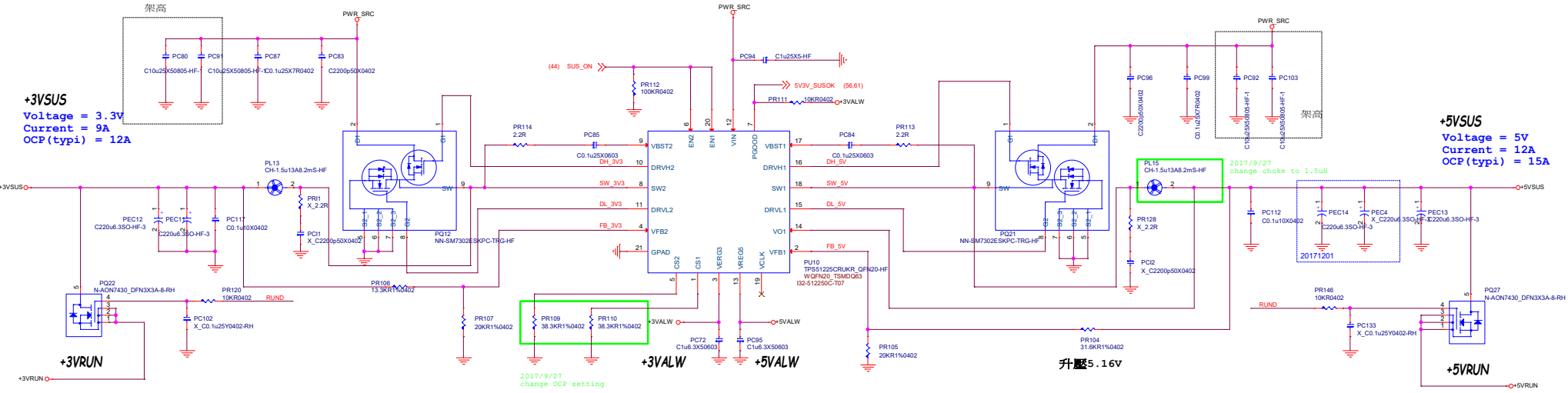
MICRO-STAR INT'L CO.,LTD.

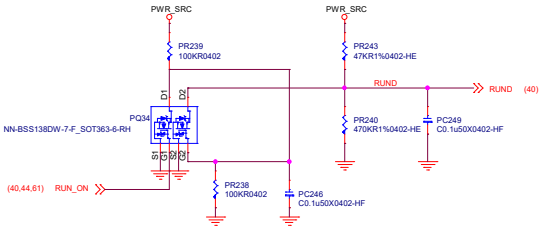
Title: Battery select/Charger

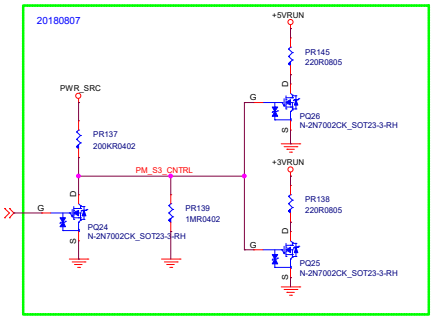
Size: Custom | Document Number: MS-16Q4 | Rev: 10

Date: Monday, December 24, 2018 | Sheet 58 of 75

System Power







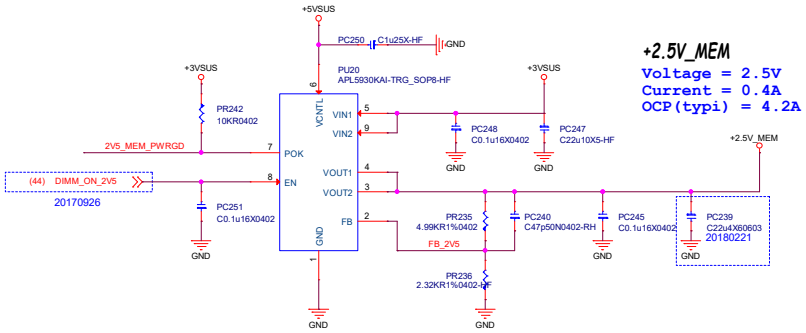
MICRO-STAR INT'L CO.,LTD.

Title: System Power

Size: Custom | Document Number: MS-16Q4 | Rev: 10

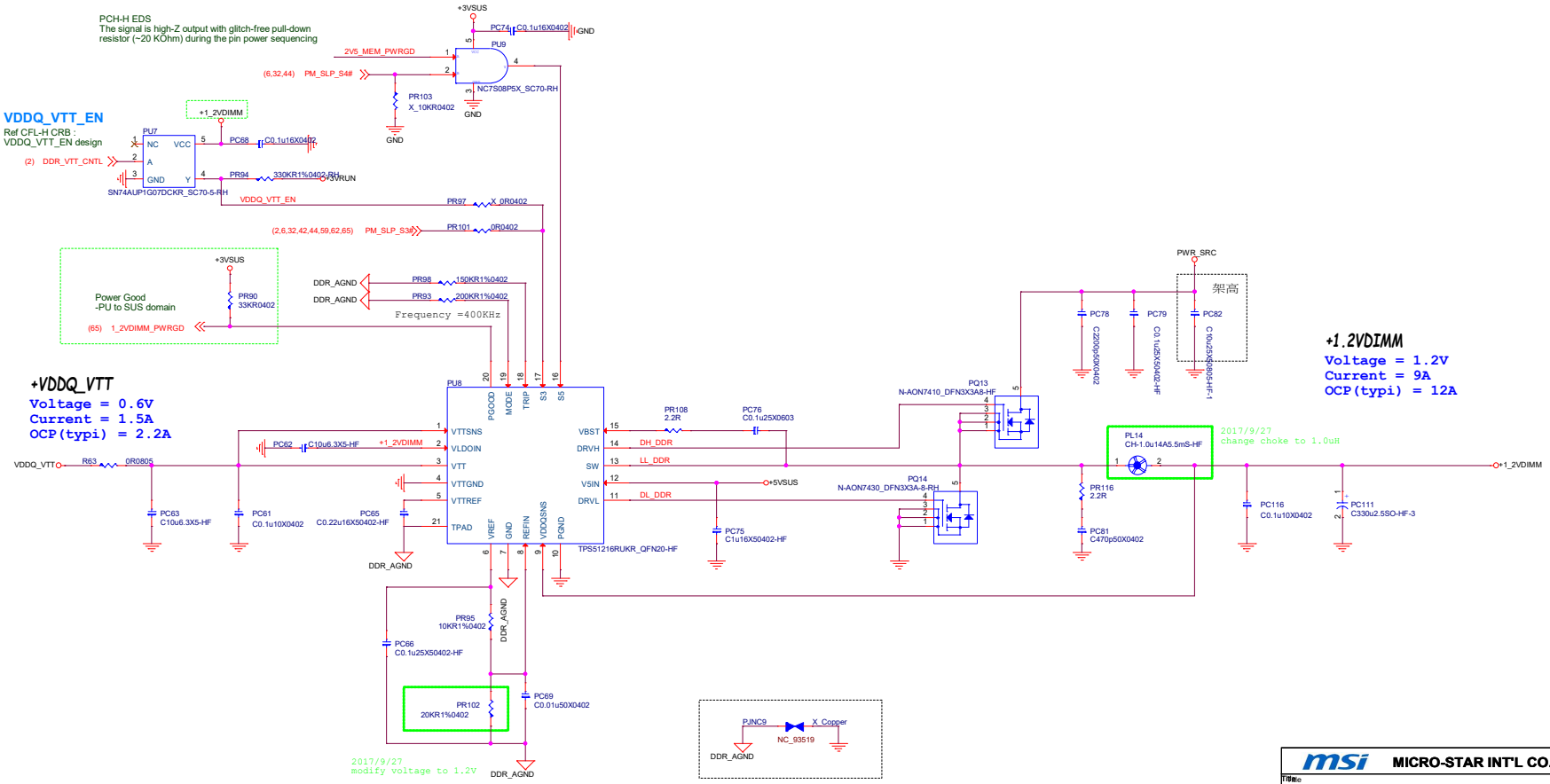
Date: Monday, December 24, 2018 | Sheet 59 of 75

+2.5V_MEM (DDR4/Vpp)



+2.5V_MEM
Voltage = 2.5V
Current = 0.4A
OCP(typi) = 4.2A

+1.2VDIMM / VDDQ_VTT(0.6V)



+VDDQ_VTT
Voltage = 0.6V
Current = 1.5A
OCP(typi) = 2.2A

+1.2VDIMM
Voltage = 1.2V
Current = 9A
OCP(typi) = 12A

Title	+2.5VMEM/+1.2VDIMM/VDDQ_VTT
Size / Custom	Document Number: MS-16Q4
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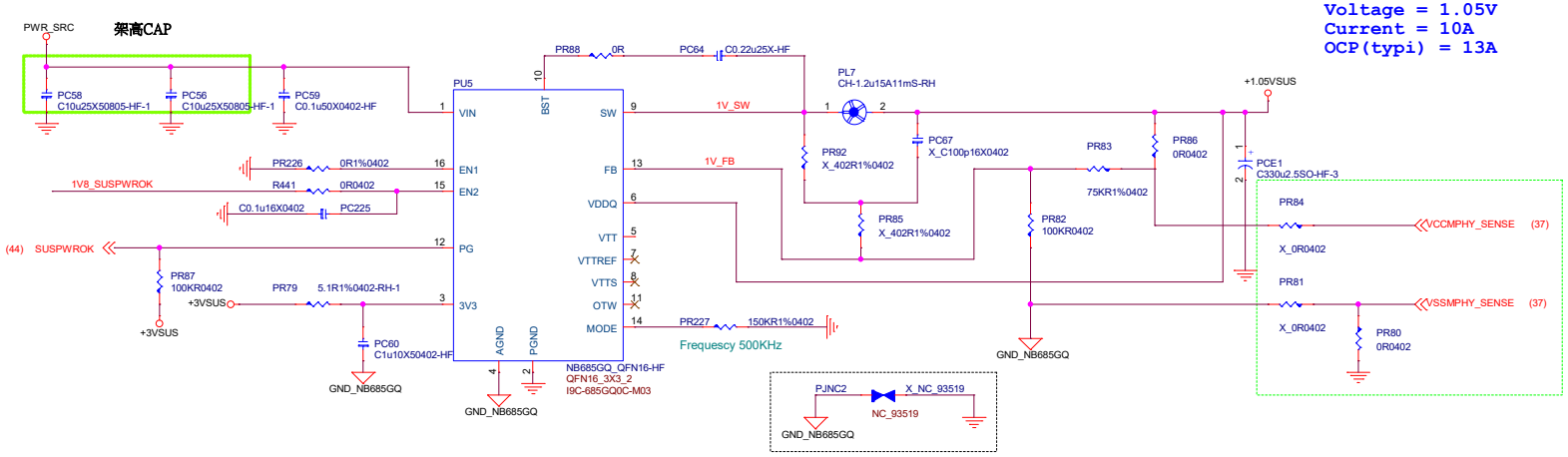
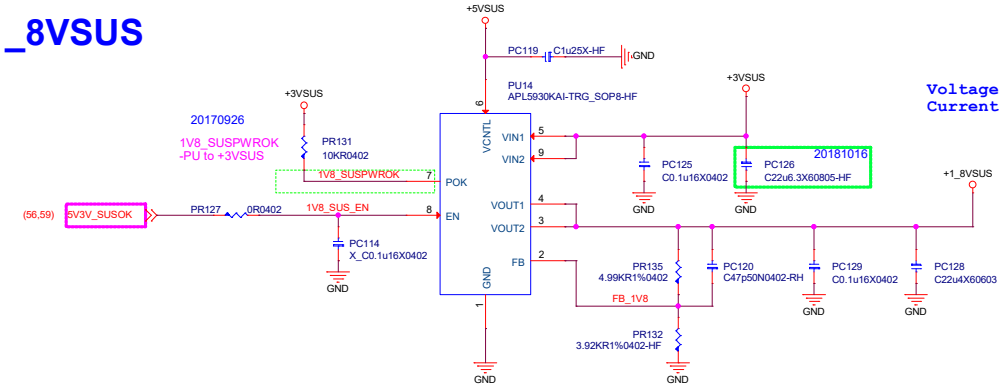
MICRO-STAR INT'L CO.,LTD.

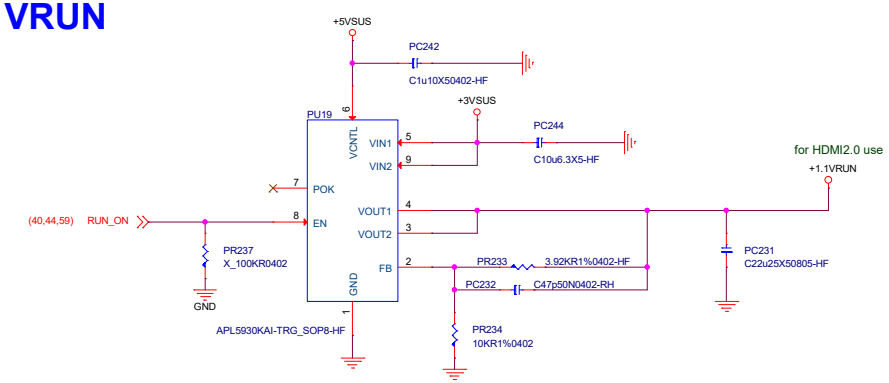
+1.05VSUS



+1_8VSUS

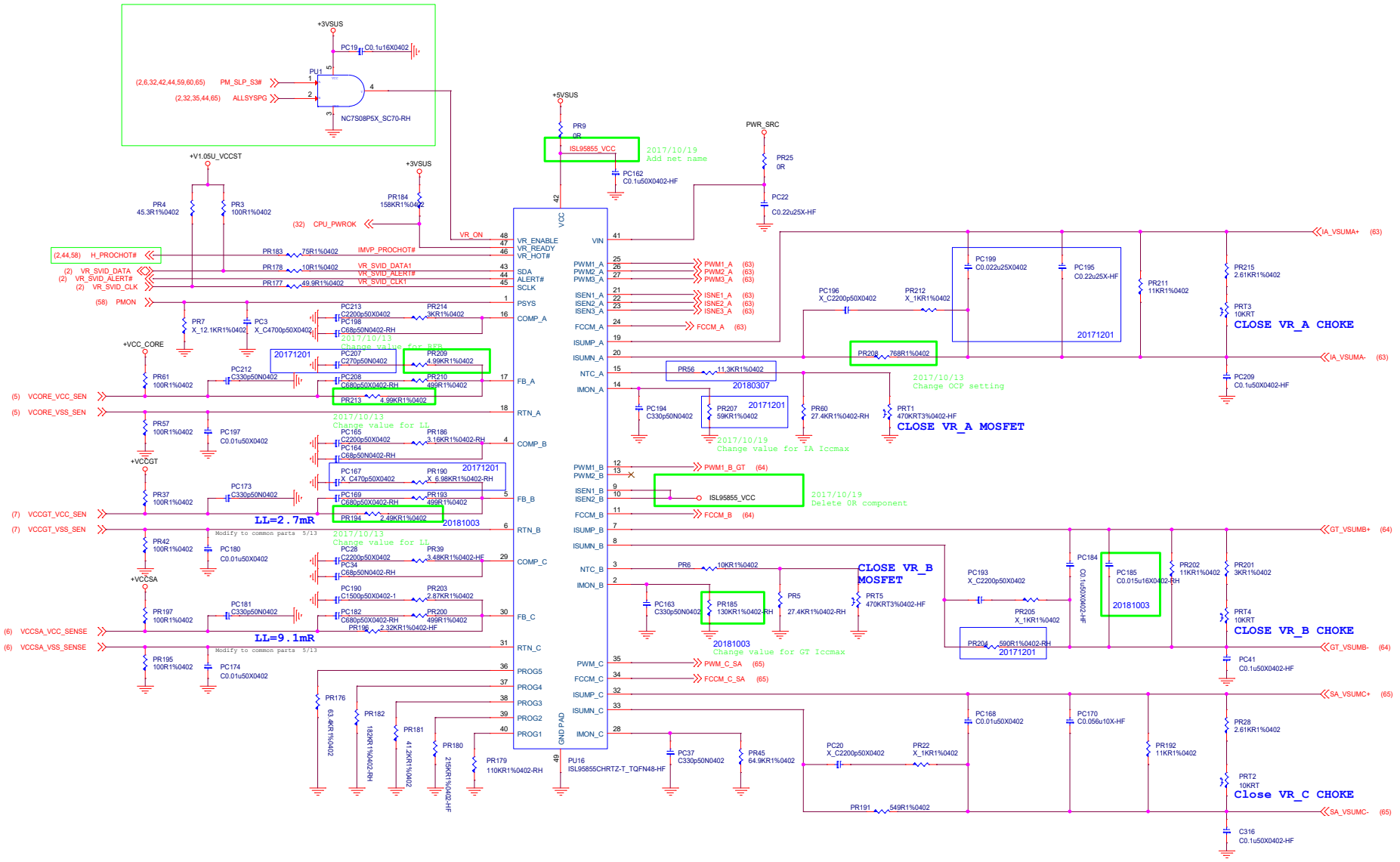


+1.1VRUN



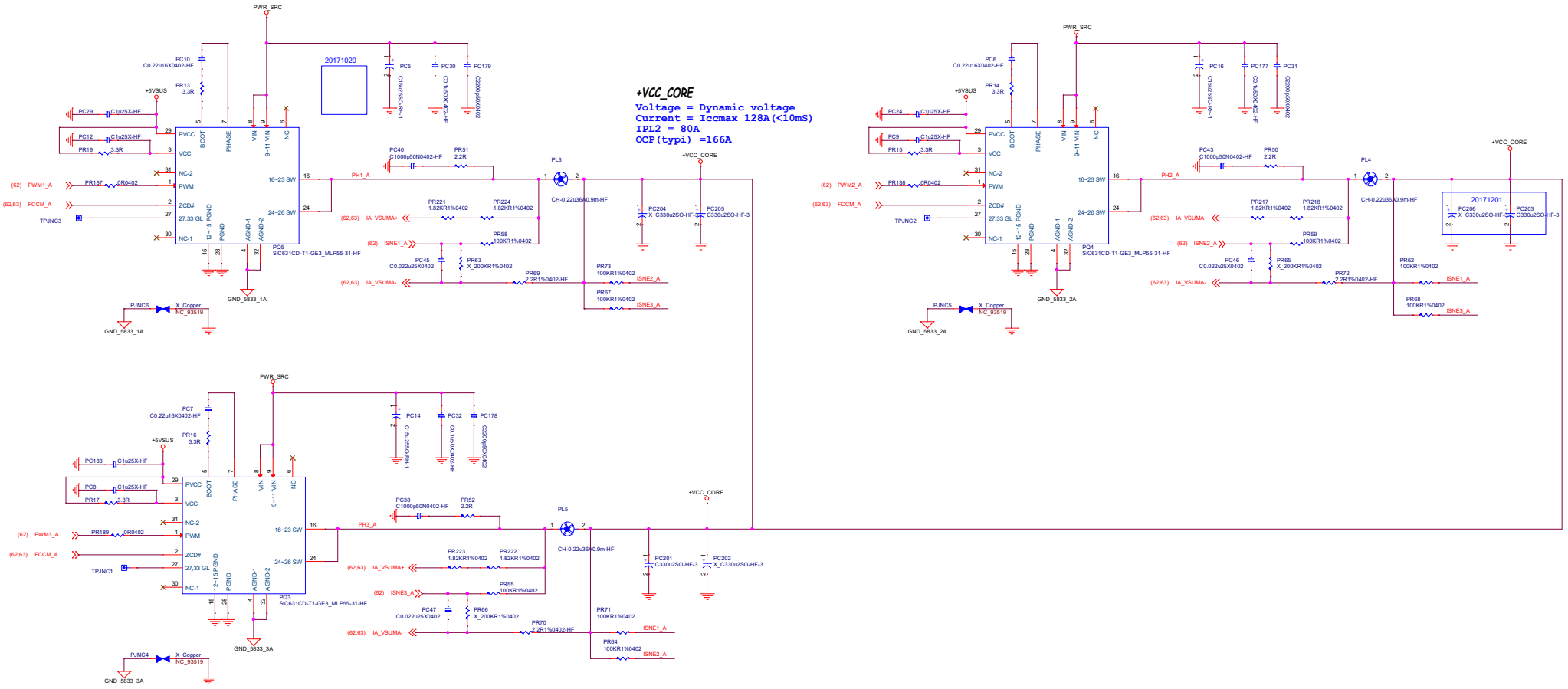
MICRO-STAR INT'L CO.,LTD.		
Title: +1.05VSUS/+1_8VSUS/+1.1VRUN		
Size: Custom	Document Number: MS-16Q4	Rev: 10
Date: Monday, December 24, 2018	Sheet 61 of 75	

Coffee Lake H-line
6+2 45W ISL95855C



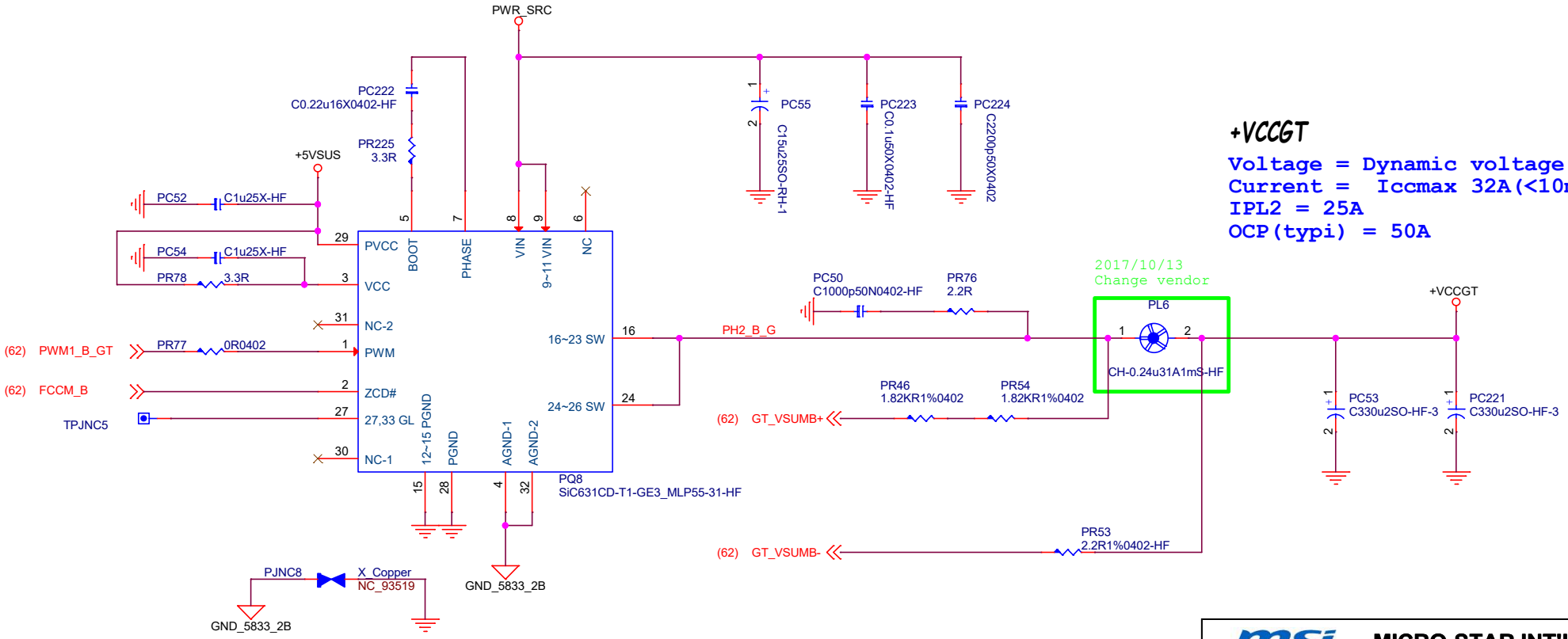
Title	CFL-H 6+2 45W ISL95855A
Size	Custom
Document Number	MS-16Q4
Rev	10
Date	Monday, December 24, 2018
Sheet	62 of 75

MICRO-STAR INT'L CO.,LTD.



MICRO-STAR INT'L CO.,LTD.			
Title: Vcore			
Size: Custom	Document Number: MS-16Q4		Rev: 10
Date: Monday, December 24, 2018		Sheet 63 of 75	

+VCCGT

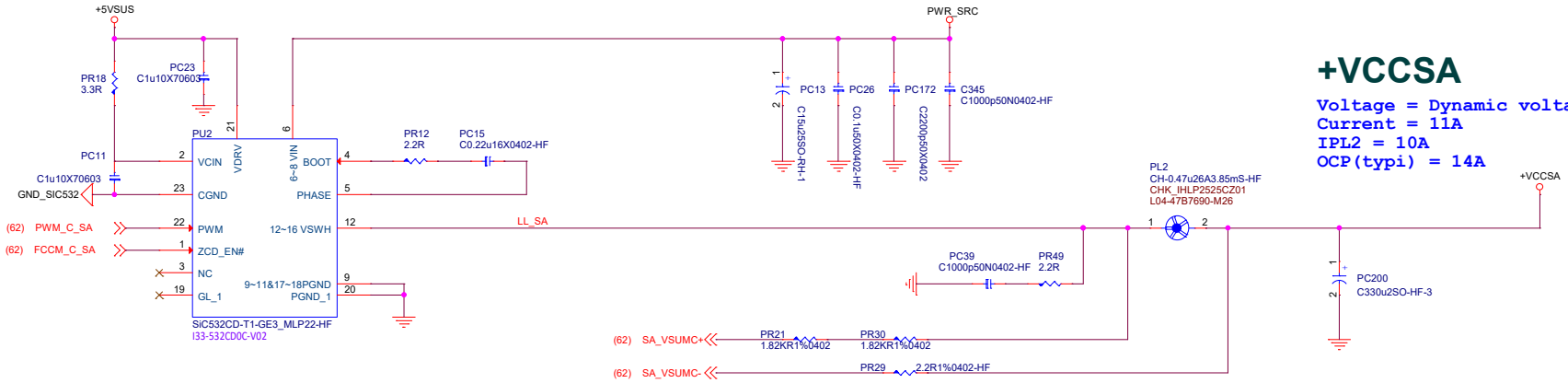


+VCCGT

Voltage = Dynamic voltage
Current = Iccmax 32A(<10mS)
IPL2 = 25A
OCP(typi) = 50A

MICRO-STAR INT'L CO.,LTD.		
Title: VCCGT		
Size: Custom	Document Number: MS-16Q4	Rev: 10
Date: Monday, December 24, 2018	Sheet 64 of 75	

+VCCSA

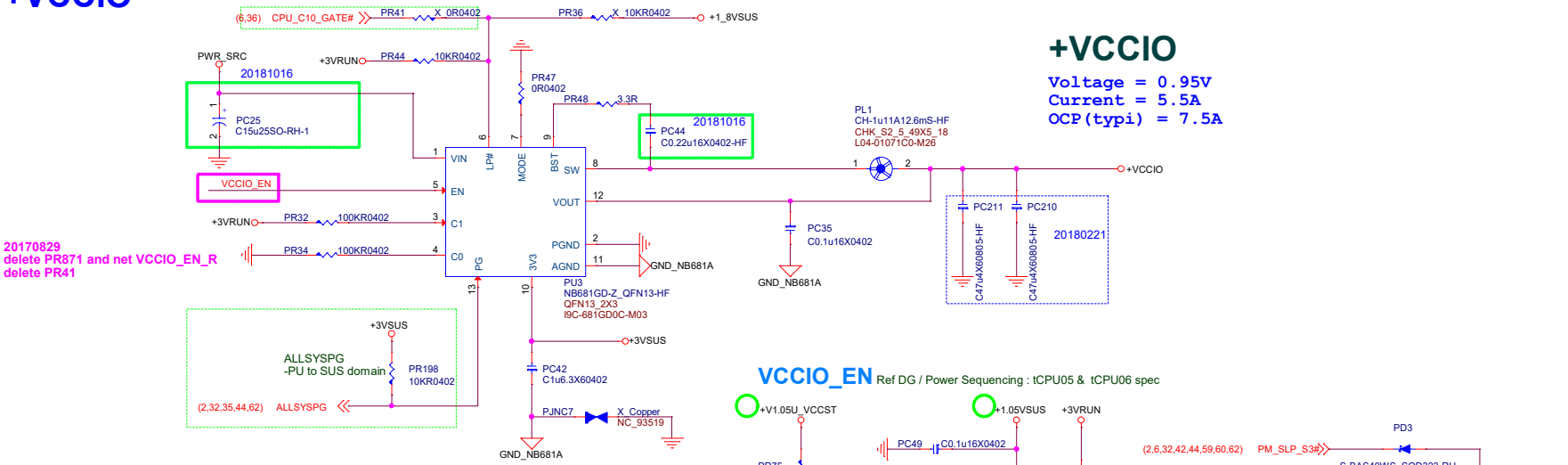


+VCCSA

Voltage = Dynamic voltage
Current = 11A
IPL2 = 10A
OCP(typi) = 14A

+VCCIO

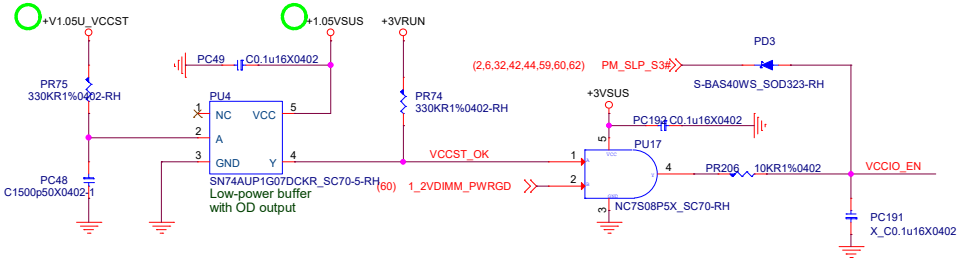
Power Sequence spec tCPU27 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 240 us



+VCCIO

Voltage = 0.95V
Current = 5.5A
OCP(typi) = 7.5A

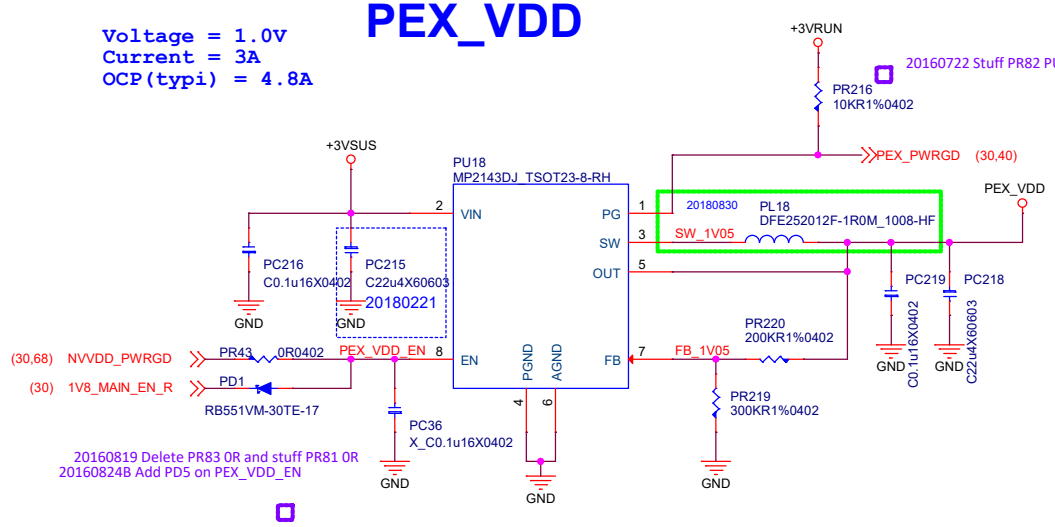
VCCIO_EN Ref DG / Power Sequencing : tCPU05 & tCPU06 spec



msi	MICRO-STAR INT'L CO.,LTD.		
Title: VCCSA/VCCIO			
Size: Custom	Document Number: MS-16Q4		Rev: 10
Date: Monday, December 24, 2018		Sheet 65 of 75	

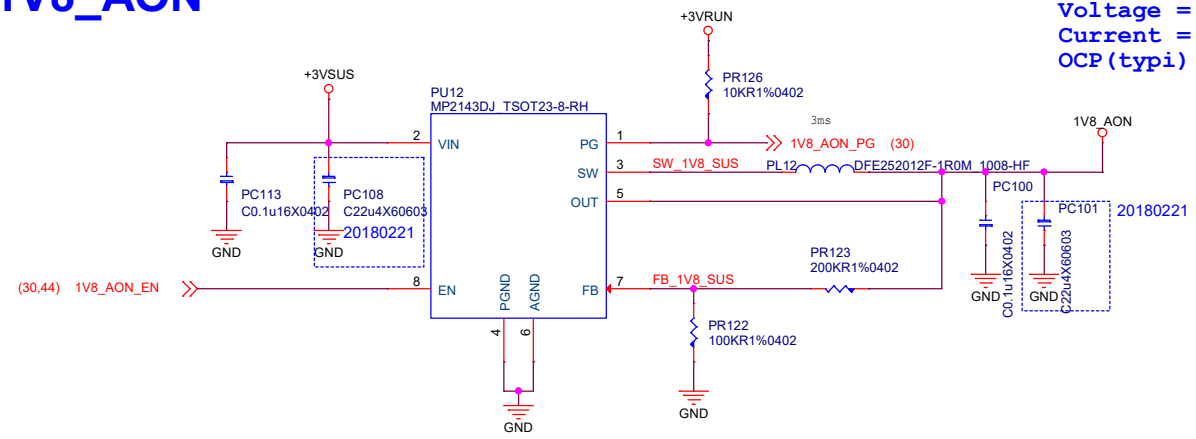
PEX_VDD

Voltage = 1.0V
Current = 3A
OCP(typi) = 4.8A



1V8_AON

1V8_AON
Voltage = 1.8V
Current = 2.26A
OCP(typi) = 4.8A

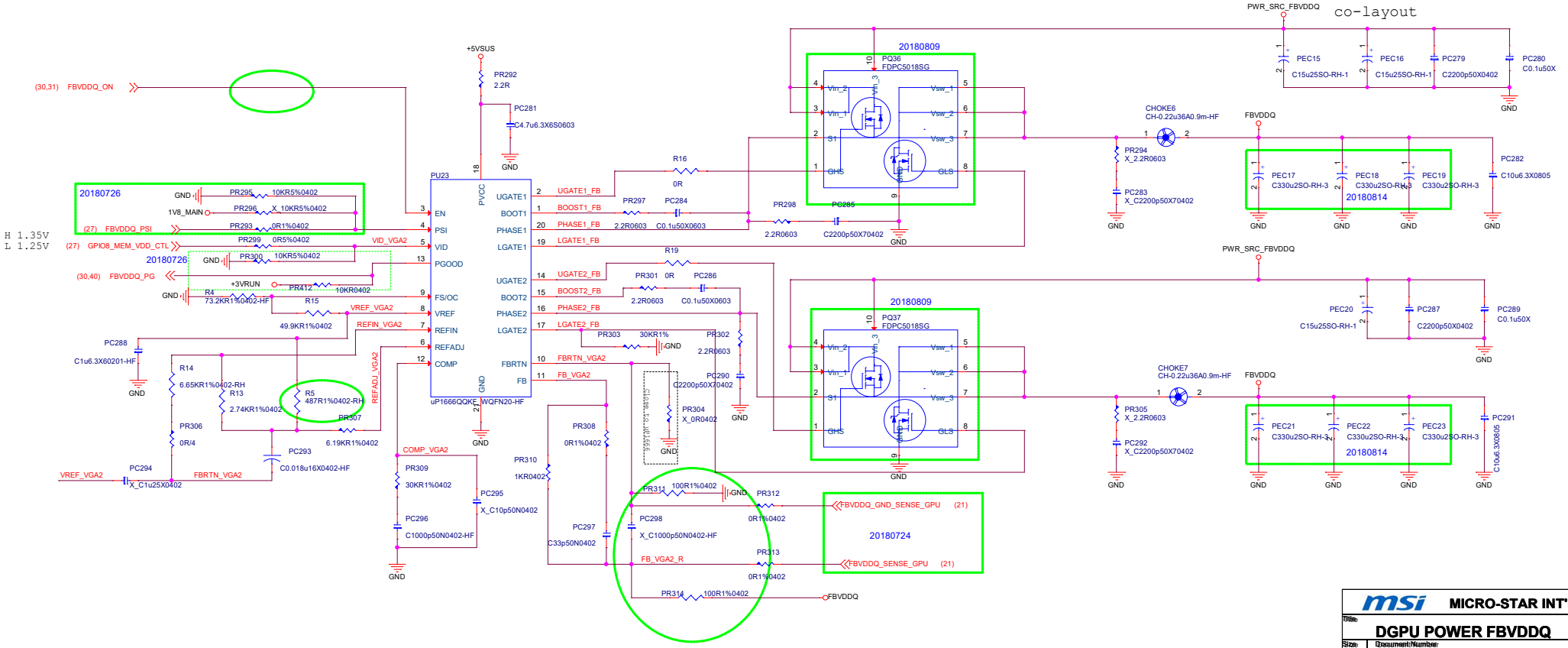


MICRO-STAR INT'L CO.,LTD.		
Title: 1V8_AON/PEX_VDD		
Size: B	Document Number: MS-16Q4	Rev: 10
Date: Monday, December 24, 2018	Sheet 66 of 75	

N18E-G3 FBVDDQ / UP1666P

VBoot:1.35V
Vmin:1.25V / Vmax:1.35V

MAXQ-G3 EDP-Peak 54A
MAXQ-G3 EDP-Con 40A



Title	DGPU POWER FBVDDQ
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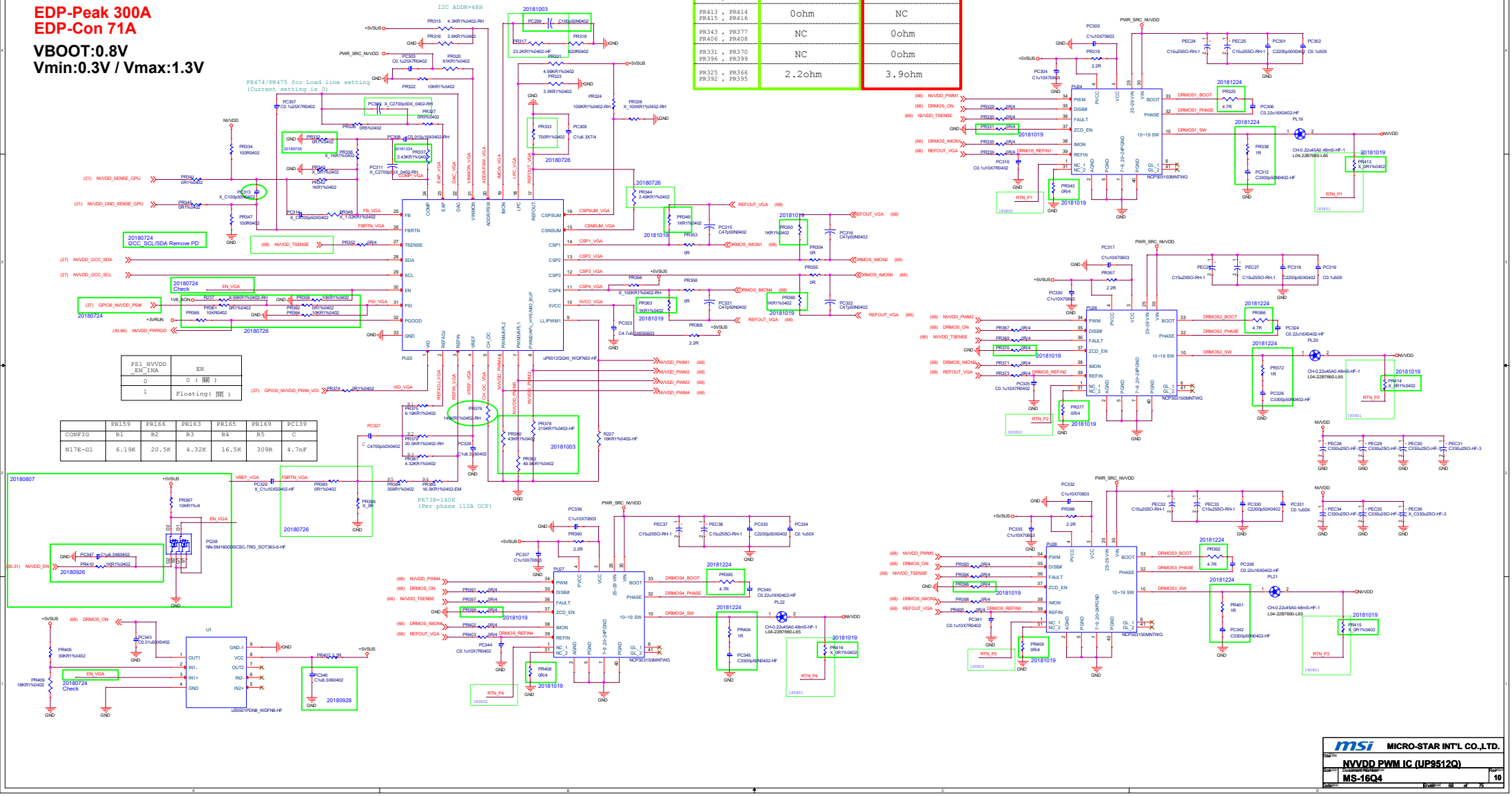
MICRO-STAR INT'L CO.,LTD.

DGPU POWER NVVDD
UP9512Q

EDP-Peak 300A
EDP-Con 71A

VBOOT:0.8V
Vmin:0.3V / Vmax:1.3V

	UPI(N/A)	ON(N18E-G1/G2/G3)
PR349 , PR350 PR360 , PR363	NC	1Kohm
PR413 , PR414 PR415 , PR416	0ohm	NC
PR343 , PR377 PR406 , PR408	NC	0ohm
PR331 , PR370 PR396 , PR399	NC	0ohm
PR325 , PR366 PR392 , PR395	2.2ohm	3.9ohm



PSI_NVVDD_EN_INA	EN
0	0 (關)
1	Floating(開)

	PR159	PR166	PR163	PR165	PR169	PC139
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	4.7nF

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Title: NVVDD PWM IC (UP9512Q)

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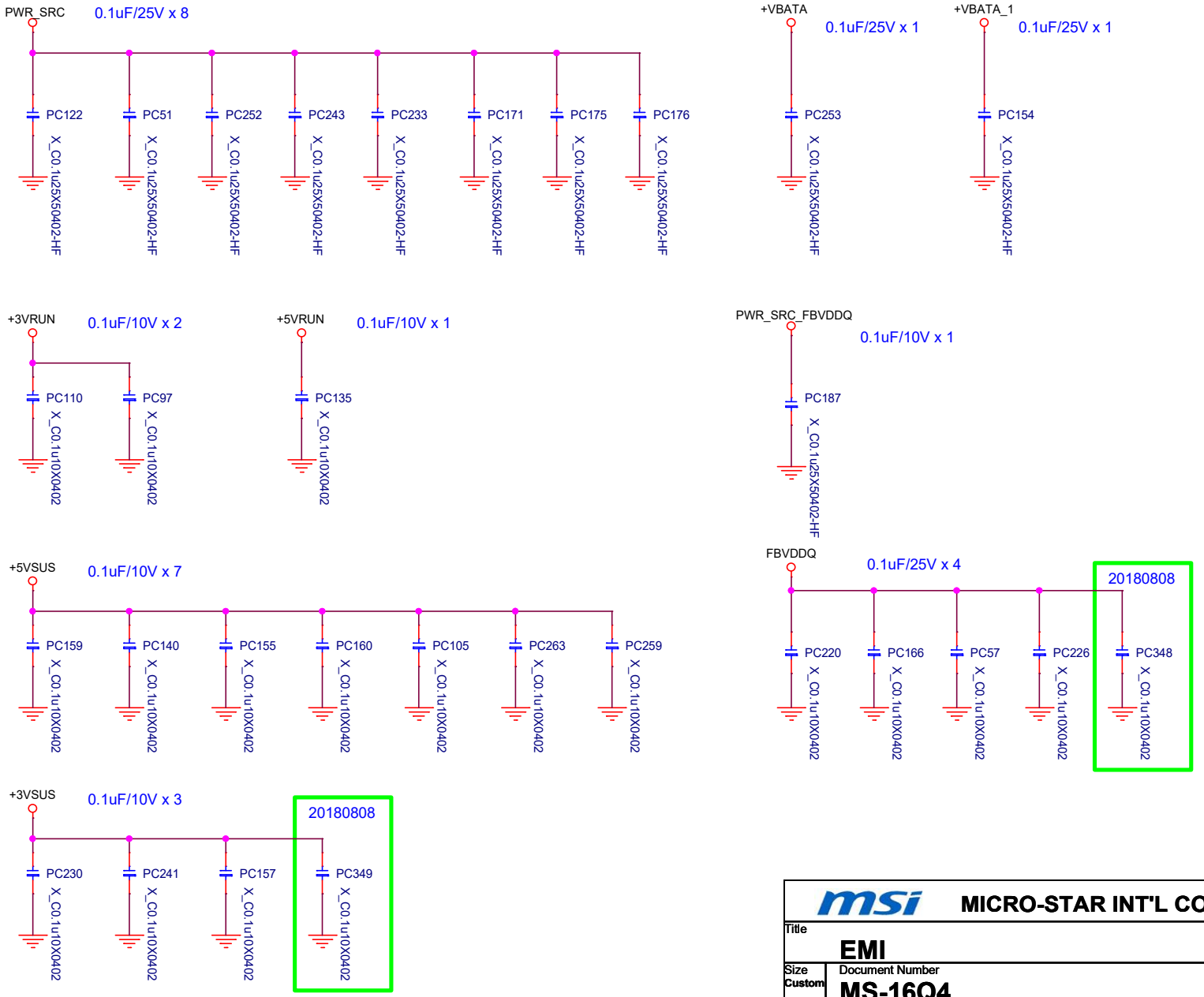
EMI

20171018



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Title: EMI		
Size: Custom	Document Number: MS-16Q4	Rev: 10
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dGPU Holes

MGPU1 H_R185D169BR276_PB_N
MGPU2 H_R185D169BR276_PB_N
GND GND

CPU Holes

MCPU2 H_R276D169_PB_N
MCPU1 H_R276D169_PB_N
MCPU3 H_R276D169_PB_N
GND GND GND

BKT

UME5 CPU BKT
X_CPU BRACKET
307-6Q40111-HG0

MYLAR

UME37 DDR MYLAR
DDR_MYLAR
E2P-0112911-G40

UME36 DDR MYLAR
DDR_MYLAR
E2P-0112911-G40

PCB1
PD0-16Q4110-H73
PD0-16Q4110-H73

FM1 FM15 FM37 FM47 FM12 FM2 FM21 FM51 FM13 FM30 FM36 FM5 FM32 FM6 FM16 FM42 FM28 FM11 FM31 FM41 FM34 FM25 FM10 FM43 FM50 FM9 FM23 FM7 FM20

MH8 X_H_R276D118 H_R276D118_N
MH2 X_H_R276D118 H_R276D118_N
MH1 X_H_R276D118 H_R276D118_N
MH14 X_H_R276D118 H_R276D118_N
MH13 X_H_R276D118 H_R276D118_N
MH5 X_H_R276D118 H_R276D118_N
MH11 X_H_R276D118 H_R276D118_N
GND GND GND GND GND GND GND

MH15 X_H_R276D118 H_R276D118_N
PCB左下角 AGND區

MH12 X_NPTH_98 NPTH_98
MH3 X_NPTH_98 NPTH_98
MH7 X_NPTH_98 NPTH_98
GND GND GND

MH4 X_H_R197D118_PT_N H_R197D118_PT_N
MH6 X_H_R197D118_PT_N H_R197D118_PT_N
GND GND

SSD Stand-off

MH10 E2B-16K1010-RH H_R201D118_PT_N
MH9 E2B-16K1010-RH H_R201D118_PT_N
GND GND
SSD stand-off bottom
SSD stand-off bottom

XX2 X_NPTH118 NPTH118
XX4 X_NPTH118 NPTH118
XX3 X_NPTH118 NPTH118
XX1 X_NPTH118 NPTH118
PCB板外

E1 X_HS-MS1011-RH
E3 X_HS-MS1011-RH
E2 X_HS-MS1011-RH
GND GND GND

UME1 HDMI Lable
HDMI ROYALTY
Y01-RHDMI03-000

UME2 BIOS Lable
UEFI_CODE_BIOS_LABEL
G51-N1CO041-A09

For MP

RUBBER

UME42 RUBBER
RUBBER
E2Y-3A12911-Y40

UME43 RUBBER
RUBBER
E2Y-3A12911-Y40

UME44 RUBBER
RUBBER
E2Y-3A12911-Y40

DDR_RUBBER

UME38 RUBBER
DDR_RUBBER
E2Y-6K21111-Y40

UME39 RUBBER
DDR_RUBBER
E2Y-6K21111-Y40

UME40 RUBBER
DDR_RUBBER
E2Y-6K21111-Y40

UME41 RUBBER
DDR_RUBBER
E2Y-6K21111-Y40

ADHESIVE_TYPE

UME45 ADHESIVE TYPE
ADHESIVE_TYPE
E2Y-8121911-G40

UME46 Mylar
G3 GPU MYLAR
E2P-7G11811-Y42

UME100 Option Mylar
X_G1&G2 GPU MYLAR
E2P-7G12411-Y42

UME101 Option Mylar
X_G0 GPU MYLAR
E2P-7G12511-Y42

UME47 FABRIC 20181220
FABRIC
E2Y-X059611-CA7

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Title: Screw/ME
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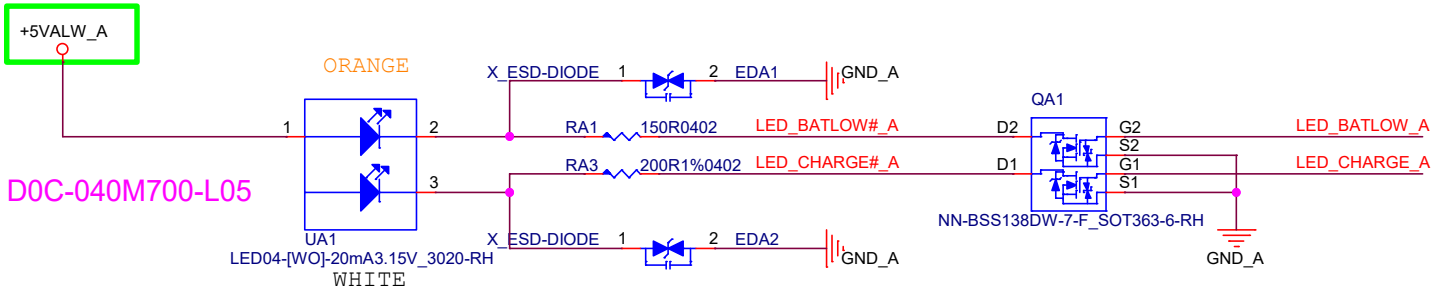
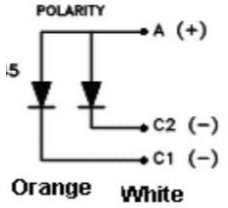
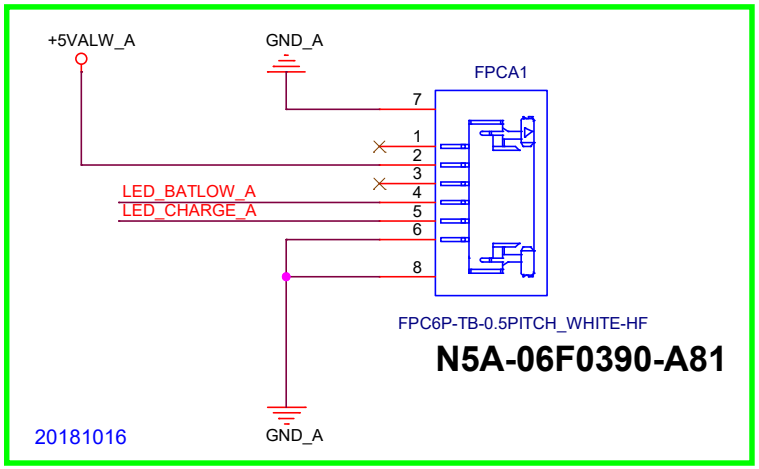
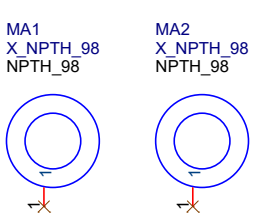
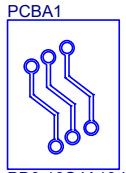




Part No.	Lens	Emitted Color	Pin Assignment
LTW-326DSKF-5A	Yellow	InGaN White	C2
		AlInGaP Orange	C1







PD0-16Q4A10-H73

MICRO-STAR INT'L CO.,LTD.

Title: **LED Board**

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+3VALW_B 20181016

2015.01.06

Hall Switch

UB1
X
Y
VDD
GND
VOUT
Z
GND_B

CB1
C0.1u50X0402-HF
RB1
X_100KR0402
GND_B

APX8132HAI-TRG_SOT23-3-HF
I36-8132H09-A30

CB2
X_C10p50N0402
GND_B

LID#_B

20180808
SWB1
SW-TACTB1S-HF
N71-0101630-D02

PWR_SW#_B
A
B
E
F
C
D
GND_B
GND_B

20180808
+5VSUS_B
LEDB1
ORANGE
2
4
HYBRID_LED#_B
1
3
PWR_LED#_B
WHITE
LED04-WO-20mA3.15V30mA2.4V_1516-RH
D0C-040H800-L05

20180803
MB2
X_H_R347D221_N
H_R347D221_N
GND_B

MB1
X_NPTH_98
NPTH_98

20180813
MB3
X_NPTH_98
NPTH_98

20181016
GND_B
10
+5VSUS_B
+3VALW_B
HYBRID_LED#_B
PWR_LED#_B
PWR_SW#_B
LID#_B
GND_B
1
2
3
4
5
6
7
8
9
GND_B
FPCB1
FPC8P-0.5PITCH_WHITE-HF
N5A-08F0250-A81

PCBB1
PD0-16Q4B10-H73
PD0-16Q4B10-H73

MICRO-STAR INT'L CO.,LTD.

Title: **PWR/Hall Sensor**

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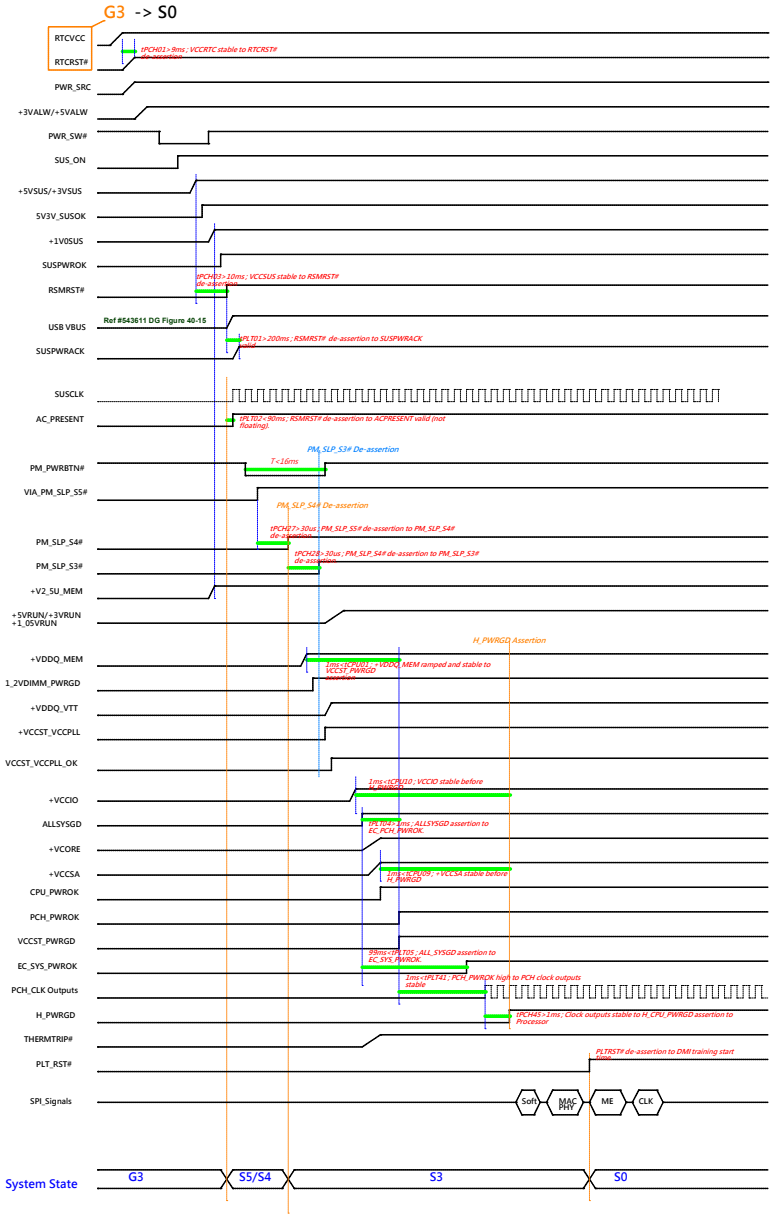
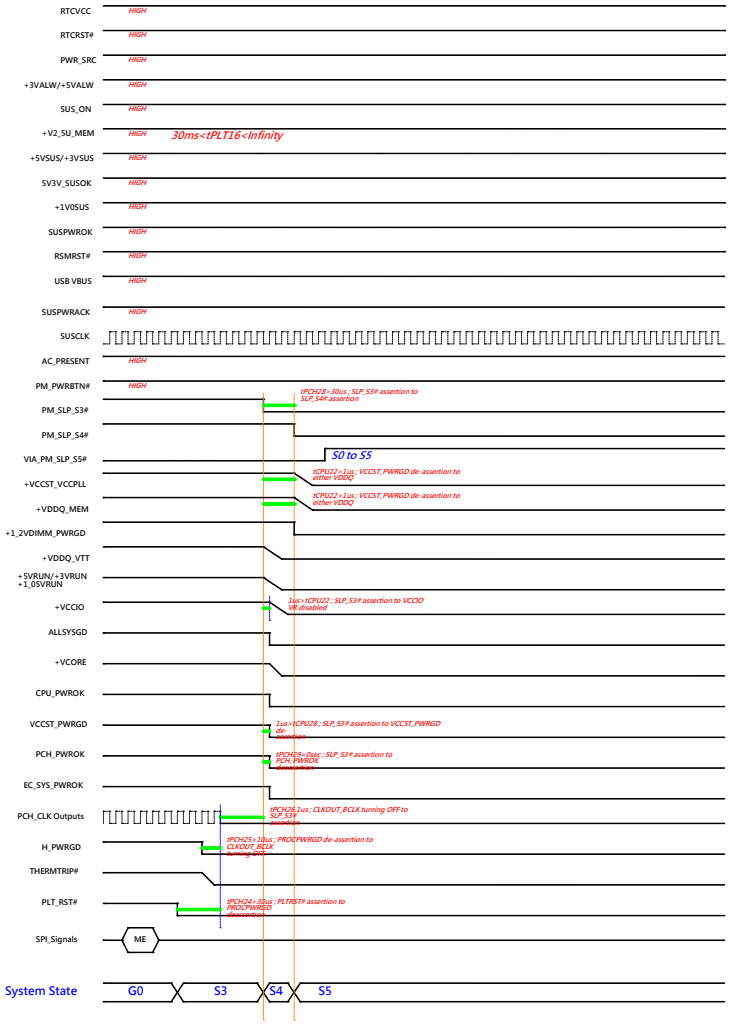
SKL-S DT Power ON Sequence G3 to S0

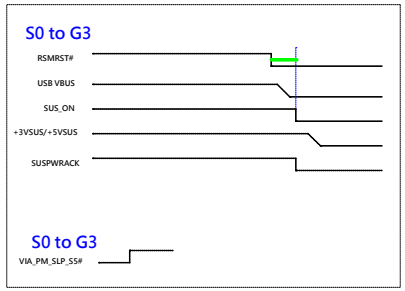
Ref #543611 Chapter40
Figure 40-4, SKL-S Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]
Table 40-5, Platform Sequencing Timing Parameters



MS-1813 : SKL-S DT Power Down Sequence S0 to S5

Ref #543611 Chapter40
Figure 40-6, SKL-S Timing Diagram for S0 to G3 [Non-Deep Sx Platform]
Table 40-5, Platform Sequencing Timing Parameters





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File: Power on Sequence			
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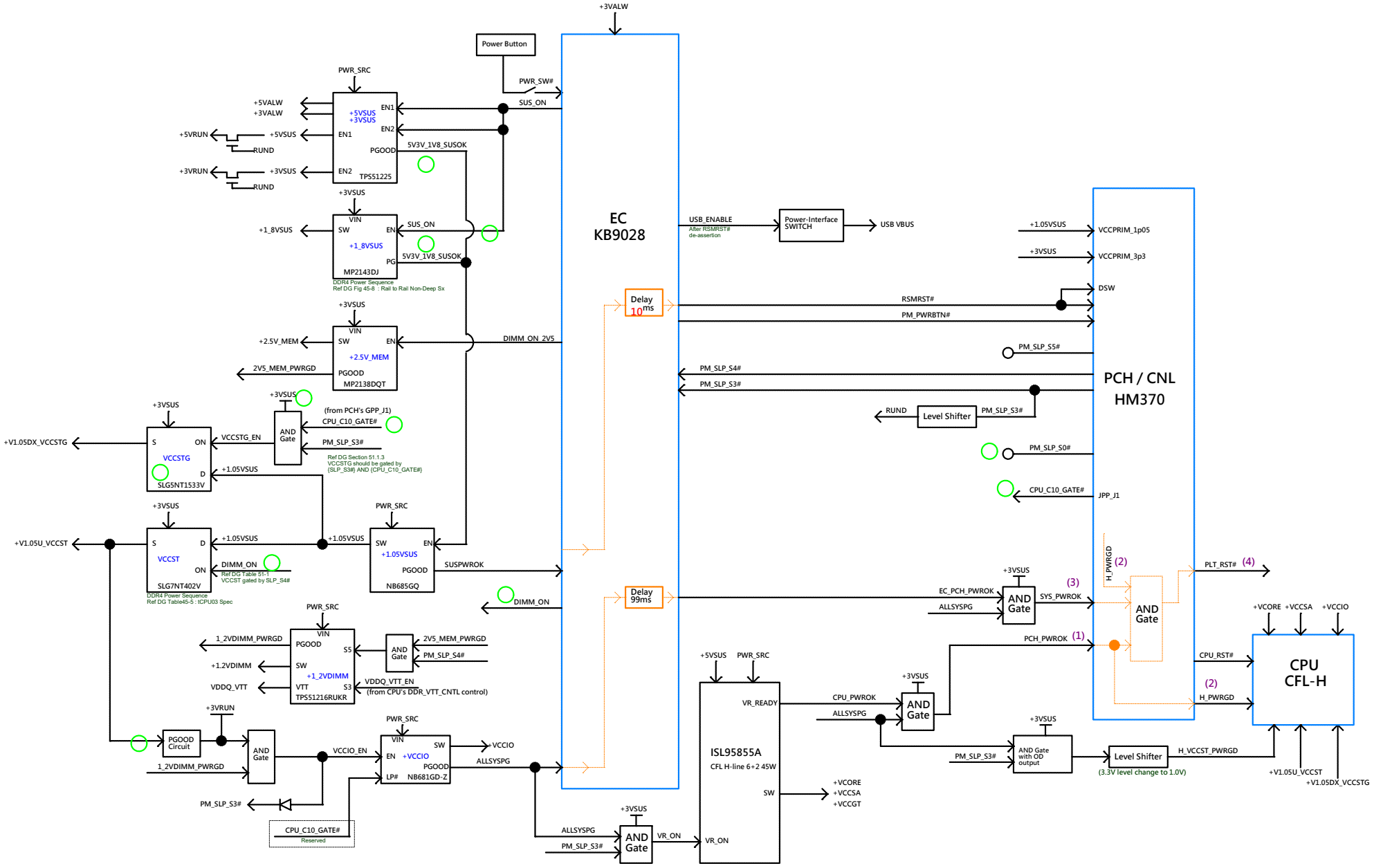
MS-16Q4 : CFL-H Mobile Power on Block Diagram

ref DG Chapter45 Power Sequencing Spec



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Title	Power ON Block Diagram
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History

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DATE	PAGE	DESCRIPTION
2018	ALL	first version from 16Q4
20180918	ALL	Add CFG_5_8750H_N18EG1_E2500_SAMSUNG for New BOM Add CFG_16Q4A Add CFG_16Q4B
	31	Modify R305,PR277 to 287 ohm(R11-1690T12-W08) for N18E-G3 Modify R305,PR277(PU100) to 287 ohm(R11-1910T12-W08) for N18E-G2 Modify R305,PR277(Add PU101) to 287 ohm(R11-2870T12-W08) for N18E-G1
	10	Modify G1(Add G101) to (OB3-16P7002-N08) for N18E-G1
	19,20	Frame Buffer ABC (D NC) for N18E-G1
20180926	70	CPU BRACKET(UME5) > NC
	55	Unstuff CON1
	45	Modify TPM Function to NC Stuff FPC1
	68	Modify PR410 to 1K-ohm for PD sequence
20180926	All	10
	55	Modify FPC9 power from +5VRUN to +3VRUN
	32	Modify RTC_CTL control circuit.
	31	Add RTG Resistor R721/R722/R723 , Unstuff R715/R716/R717
	68	Modify PC346 form 1uF/X6S/0201 to 0402
20181001	31	SWAP DP LAN2 & 3
20181002	31	Stuff R693, unstuff R692 for Parade.
20181003	62	Modify PR185 form 113K to 130K-ohm Modify PR194 form 2K to 2.49K-ohm Modify PC185 form 33nF to 15nF , Stuff it.
	68	Modify PC299 form 220pF to 100pF Modify PR380 form 34.8K to 43K-ohm Modify PR382 form 34.8K to 49.9K-ohm Modify PR378 form 169K to 215K-ohm
	31	Modify R238,R293 form 750K to 75K-ohm Modify R247,R298 form 6.49 to 649-ohm Modify PR277,R305 to 287-ohm for N18E-G1/G2/G3 Modify C375,C387 form 0.1uF to 1nF , Stuff it.
20181016	65	Modify PC18 & PC25 to C71-150251G-S03
	39	Modify R167 to 6.19K-ohm(R11-6191T12-W08)
	44,71	Modify FPCA1,FPC3 pin define
	45,72	Modify FPC1,FPCB1 pin define
	72	Move Hall sensor to PWR board
	65	Remove PC18 Modify PC44 to 0.22uF,16V,X7R(C11-2242512-W08)
	61	Modify PC126 to 22uF,6.3V,X6S(C11-226A314-M09)
20181016	68	Modify PU24,PU26,PU27,PU28 to I33-9619A0C-U47 Modify PR325,PR366,PR392,PR395 to 2.2ohm (R11-022A013-W08) Stuff PR413,PR414,PR415,PR416 Unstuff PR349,PR350,PR360,PR363 Unstuff PR331,PR370,PR396,PR399
	34	Add R724,R725 (GPU_ID) for BIOS
20181025	43	Add R726,R727 for Safety
	10	Modify G1 to OB3-1W1E004-N08 (N18E-G3-A1 PS) Modify U100 to OB3-1W1E003-N08 (N18E-G2-A1 PS) Modify U101 to OB3-16P7003-N08 (N18E-G1-KD-A1 PS)
	32	Unstuff R455
	43	Unstuff R653,R656
20181029	29	Modify R292 to 10K-ohm for NV Spec(ROM_SO).
20181101	70	Modify UME5(CPU BKT) to 307-6Q40111-HG0
20181118	28	Modify U200(VRAM) to M12-80325K5-S0N
20181118	68	PU24,PU26,PU27,PU28 : change to I33-303150C-O05 PR325,PR366,PR392,PR395 : 2.2ohm change to 3.9ohm (R11-039A033-W08) PR349,PR350,PR360,PR363 : NC change to 1Kohm(R11-0102T12-W08) PR331,PR370,PR396,PR399 : NC change to 0ohm(R11-0000012-W08) PR413,PR414,PR415,PR416 : 0ohm change to NC PR343,PR377,PR406,PR408 : NC change to 0ohm(R11-0000012-W08)
20181118	10	Mdoify G1 to B03-TU10455-N08(N18E-G3-A1) Mdoify G100 to B03-TU10655-N08(N18E-G2-A1) Mdoify G101 to B03-TU10645-N08(N18E-G1-KD-A1)
20181220	70	Add UME46/100/101(GPU Mylar) for ME Add UME47(FABRIC) for ME
	49	Modify PC98 to C11-1067620-M09 for Power
20181224	68	PR337 : 8.2K change to 2.43K(R11-2431T12-Y01) PR325/PR366/PR392/PR395 : 3.9R change to 4.7R(R11-047A013-Y01) PR338/PR372/PR401/PR404 : 2.2R change to 1R(R11-0010023-Y01) PC312/PC326/PC342/PC345 : 1000p change to 3300p(C11-3322012-Y01) Unstuff C741 Modify R388 from R11-499AT12-W08(49.9R1%0402) to R11-0102T12-W08(1KR1%0402)

Notice:
VRAM Option:
R45/R58/U200
N18E-G3/G2 > ABCD
N18EG1 > ABC

GPU Option:
G1(G100/G101)
GPU_ID(R724,R725)
R305,PR277(PU100/PU101)

CPU Opton:U4
CPU BRACKET > NC

DATE	PAGE	DESCRIPTION

DATE	PAGE	DESCRIPTION

DATE	PAGE	DESCRIPTION

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