

COMPAL CONFIDENTIAL

X12 South Peak 14 UMA TBT TGL

MODEL NAME :GDF40

PCB NO : LA-K491P

BOM P/N :431ANW31L0x

Tiger Lake U42 UP3

2020-11-30

REV : 2.0 (A01)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESDComponent
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- CONN@ : Connector Component
- MIPI60@ :MIPI Component
- NMIPI60@ :Non MIPI Pop Component
- VPRO@ : vPro Component
- NVPRO@ : Non-vPro Component
- WWAN@ : WWAN Component
- WWANRF@ : WWAN RF Component
- TGSSD@ : Intel Teton Glacier storage Component
- ST@ : ST TPM Component
- NU@ : Nuvoton TPM Component
- CPU@ : CPU
- 5107@ : MEC5107 Component
- 5200@ : MEC5200 Component
- JUMP@ : Jump solder and short
- @JUMP@ : Jump no solder
- CML@ : Comet lake platform Component
- TGL@ : Tiger lake platform Component
- 5107ES@ : MEC5107ES EC Chip
- 5107NES@ : MEC5107NES EC Chip
- 5200B@ : MEC5200B EC Chip

Part Number	Description
DA800102000	PCB 30K LA-K491P REV0 MB 1 S

Layout Dell logo



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REV:A01
PWB:2FM7C

Power CKT : X12 SOUTH PEAK 14UU_TBT_TGL_A00_PWR_20201028
GPIO map : X12_TGL_U GPIO map Rev0.9_20200728
Connector list : South Peak 14 conn List_200609

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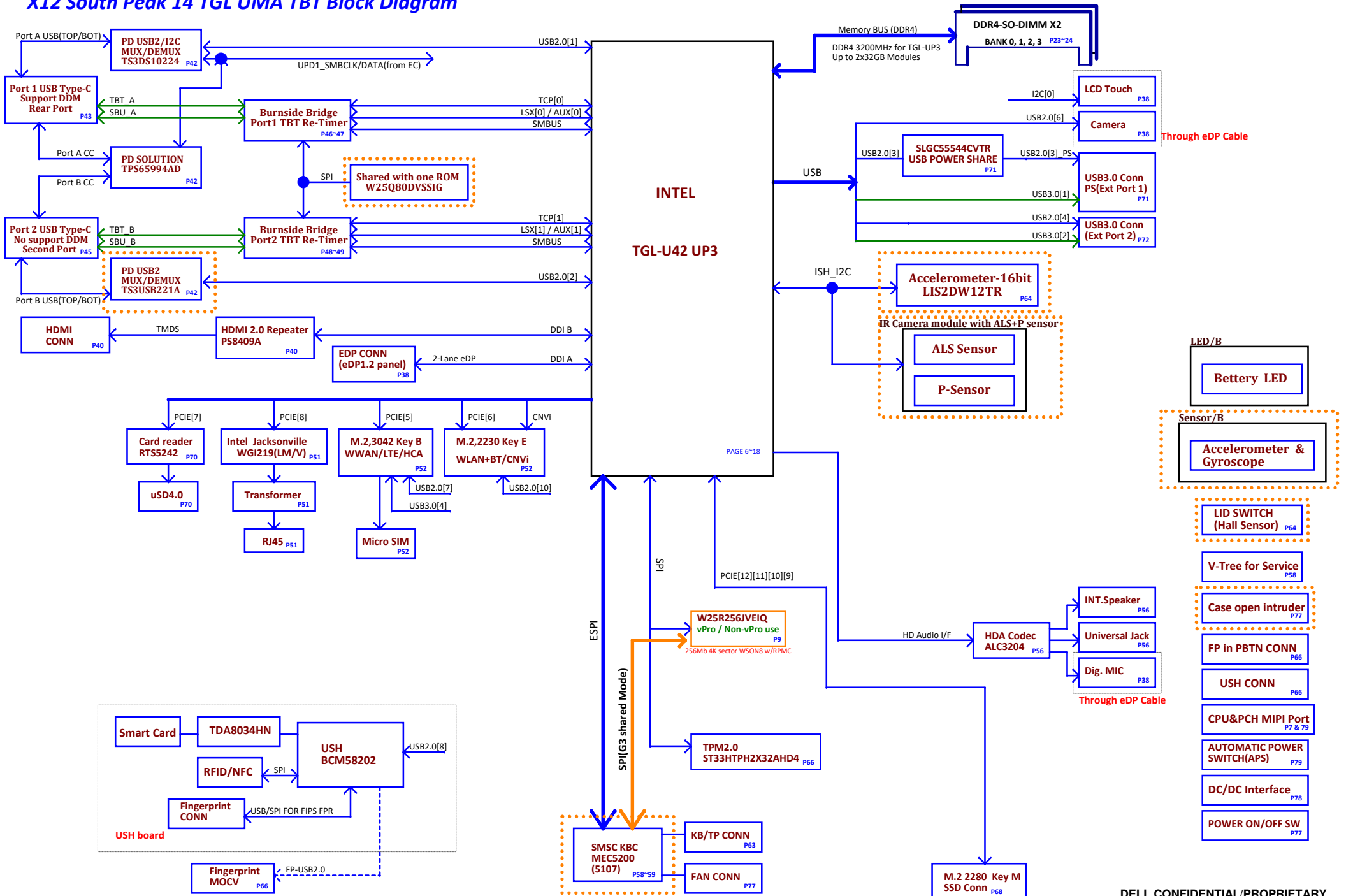
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Size	Document Number	Rev	
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X12 South Peak 14 TGL UMA TBT Block Diagram



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	PRIM PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0ix/Moff	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF
S0ix (Suspend to RAM) / M-OFF	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB3.0	Gbe	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		JUSB1
USB3.0-2		PCIE-2		JUSB2
USB3.0-3		PCIE-3		NA
USB3.0-4		PCIE-4		M.2 3042(WWAN)
		PCIE-5		M.2 3042(LTE)
	V	PCIE-6		M.2 2230(WLAN)
	V	PCIE-7		CARD READER
	V	PCIE-8		LOM
		PCIE-9		M.2 2280 SSD
		PCIE-10		
		PCIE-11	SATA-0	
		PCIE-12	SATA-1	

USB PORT#	DESTINATION
1	Type-C Port 1
2	Type-C Port 2
3	JUSB1(RIGHT)
4	JUSB2(LEFT)
5	NA
6	Camera
7	M.2 3042(WWAN)
8	USH
9	Reserved for FPR in PB
10	M.2 2230(BT)

PM TABLE

State \ power plane	+3.3V_RTC_LDO +5V_ALW +5V_ALW2 +3.3V_ALW2 +3.3V_ALW2 +3.3V_PRIM +1.8V_PRIM +3.3V_ALW_DSW +VCC_VNNEXT_1P05 +VCC_V1P05EXT_1P05	+1.2V_MEM +2.5V_MEM +1.05V_VCCSTG	+1.05V_VCCSTG* +3.3V_RUN +5V_RUN +1.8V_RUN +1.2V_RUN +0.6V_DDR_VTT	+RTC_CELL
S0	ON	ON	ON	ON
S0ix	ON	ON	OFF	ON
S5 S4/AC	ON	OFF	OFF	ON
S5 S4/DC only	OFF	OFF	OFF	ON

*VCCSTG can be turned off when the processor is in C10

Figure 2. Flexible HSIO Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4			GbE	GbE	GbE		SATA 0	SATA 1

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Port assignment

Document Number

LA-K491P

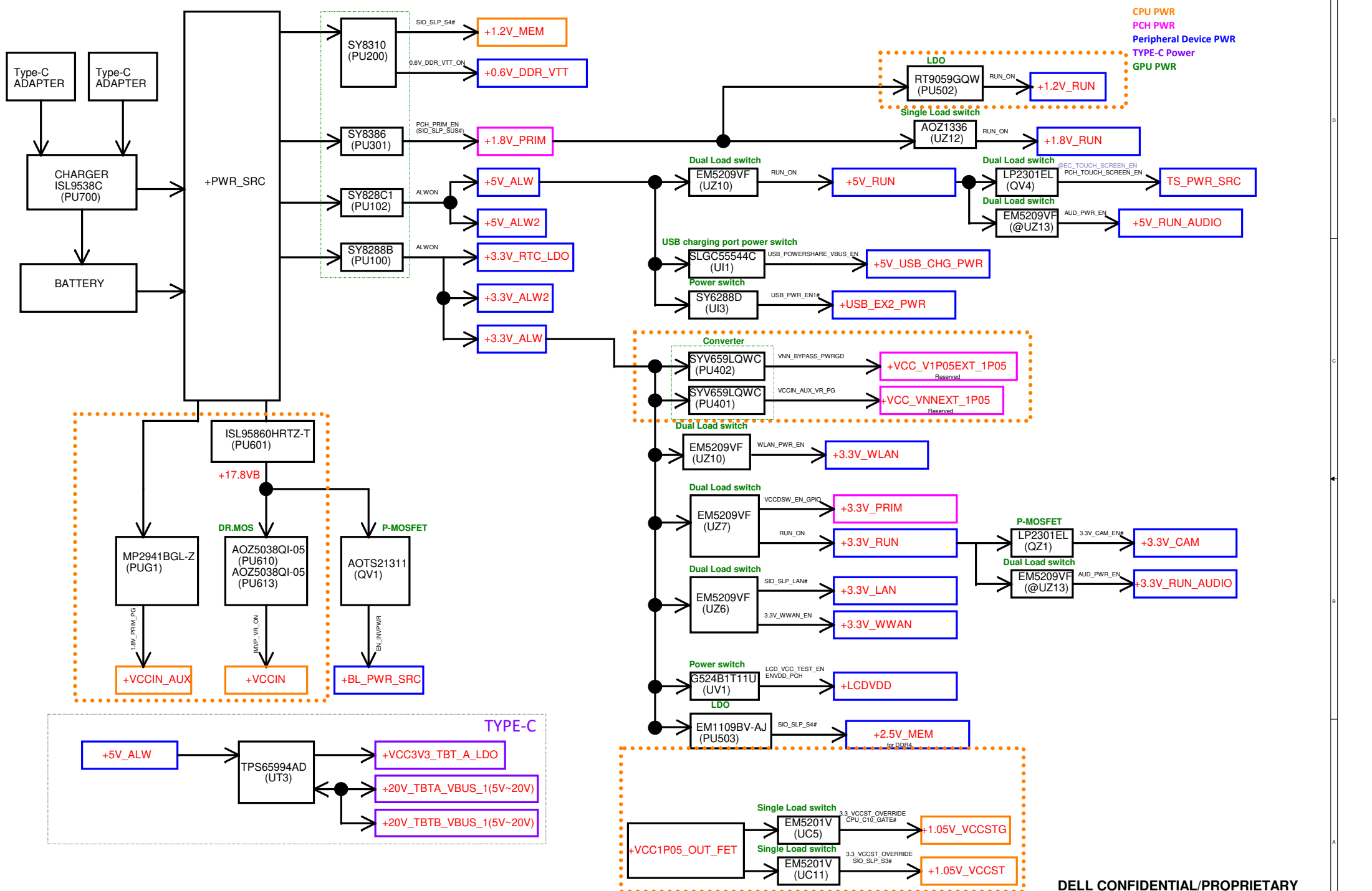
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Rev 2.0



CPU PWR
 PCH PWR
 Peripheral Device PWR
 TYPE-C Power
 GPU PWR

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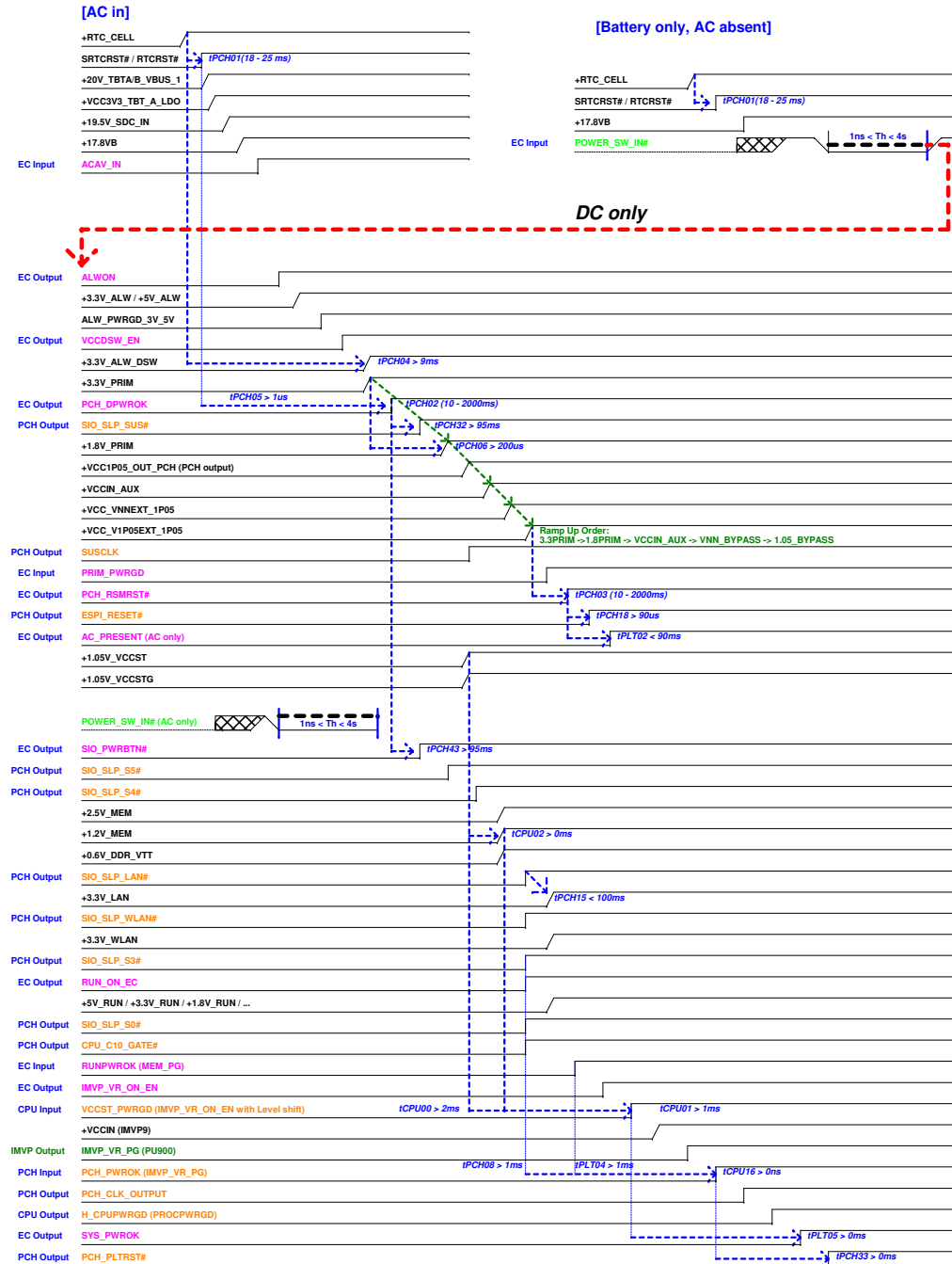
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Power rails

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Power Sequence G3 -> S0 Non deep



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Power Sequence

Document Number LA-K491P

DATE: Tuesday, December 08, 2009

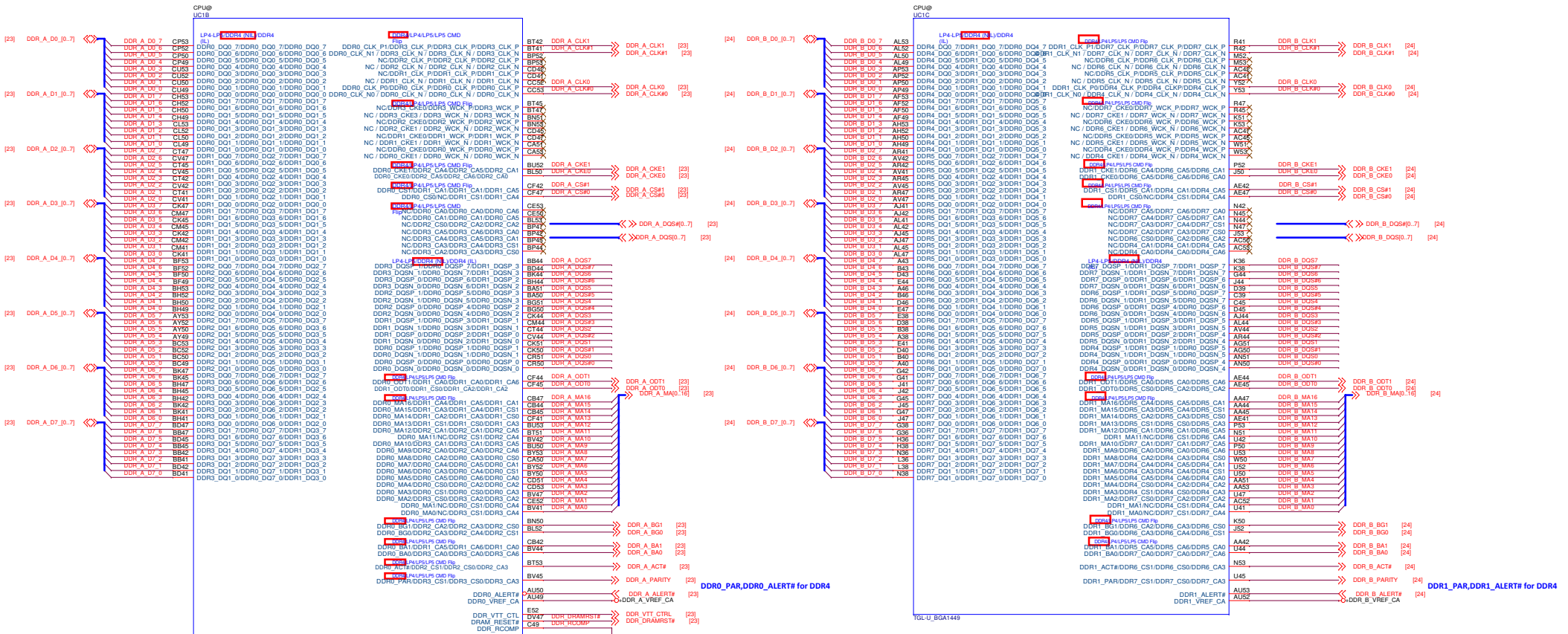
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REV

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DDR4, Ballout for side by side(Non-Interleave)



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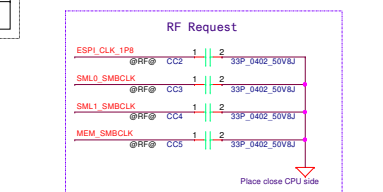
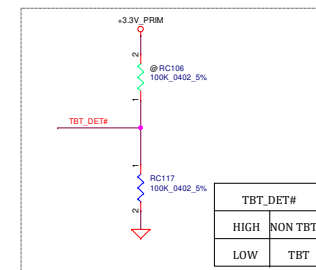
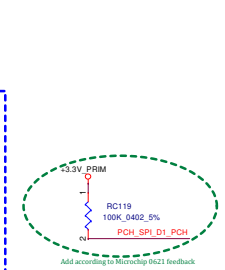
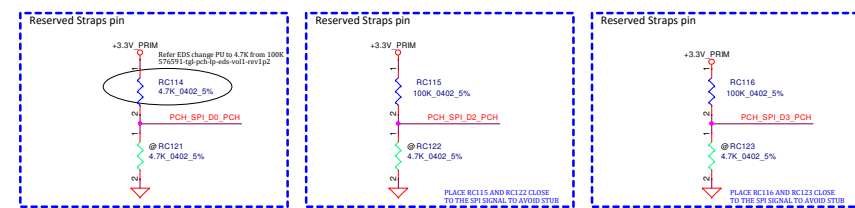
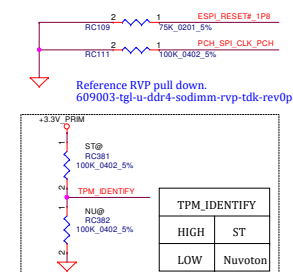
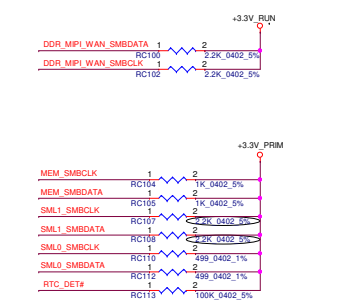
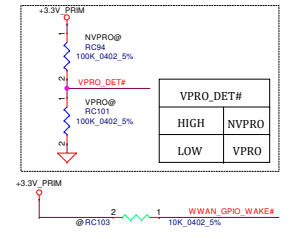
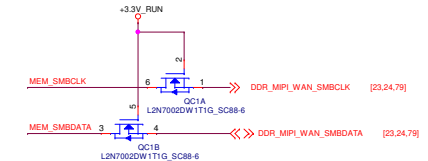
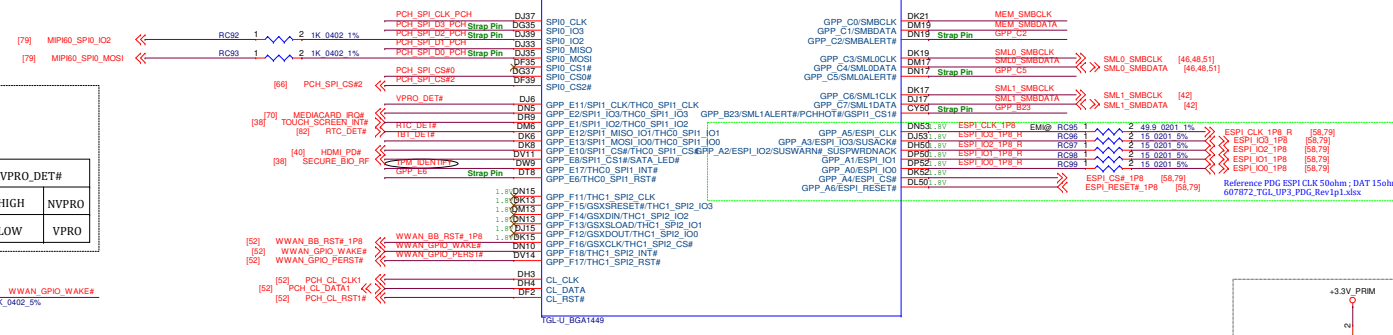
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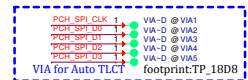
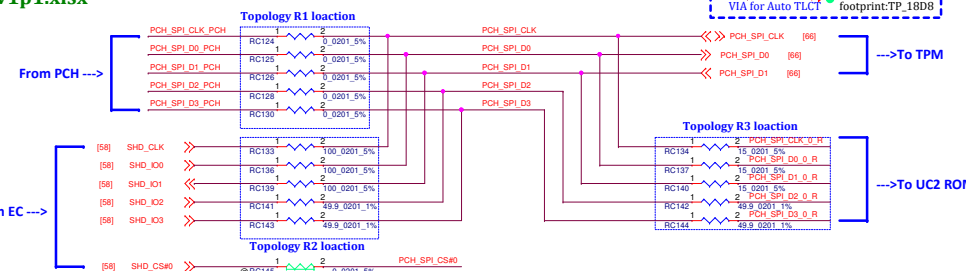
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Quirk 198138
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 SPI_M0S0-SPI_I01
 606576-ctrl-pch-to-edev011-rev1p0.P.262-263



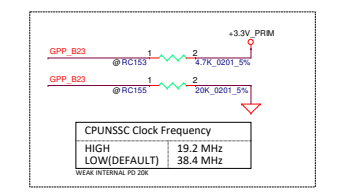
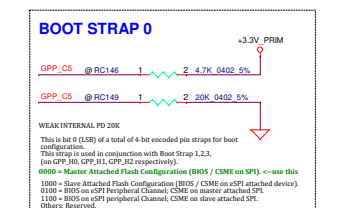
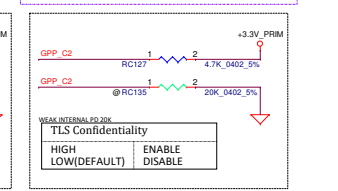
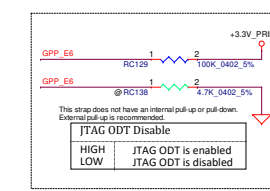
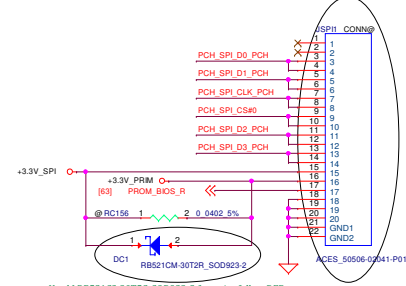
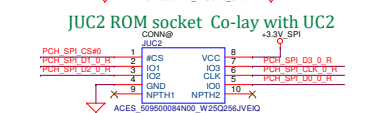
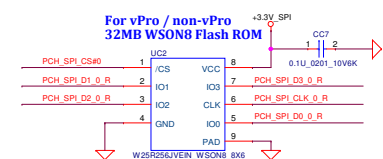
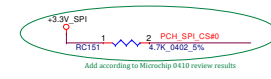
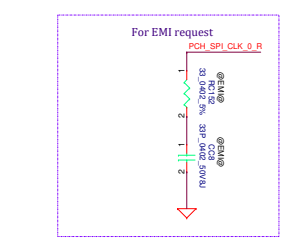
EC G3 SPI Flash Sharing with Wire-OR(1 Flash and 1TPM) Reference 607872_TGL_UP3_PDG_Rev1p1.xlsx SPI0 Flash sheet Non-Vpro / Vpro Topology at P.105



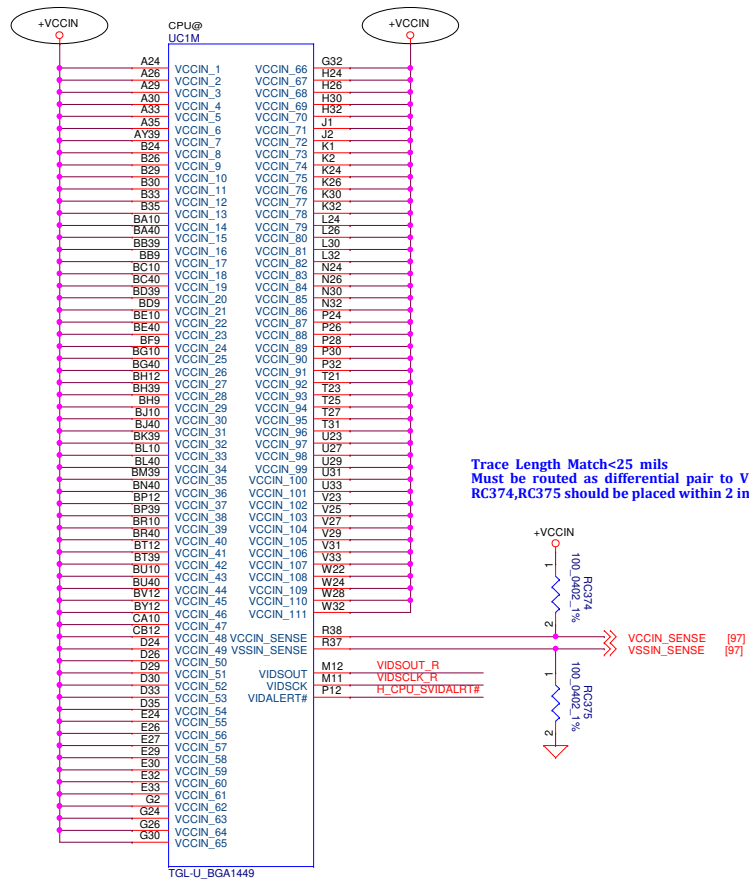
System ROM choice need follow ARD approved list

BIOS ROM	Dell Approved P/Ns: (See Dell ENG0013005 for updates)
	32MB (WSON-8, 8x6mm) (MUST support RPMC)
	Windbond - W25R256V1Q
	Macronix - MX77L25650FZ4142
	GigaDevice - GD25R256DY1GR
	XMC - XM25RH256C1Q1T10Q

System ROM choice need follow ARD approved list 32MB (WSON-8, 8x6mm) (MUST support RPMC) Windbond - W25R256V1Q Macronix - MX77L25650FZ4142 GigaDevice - GD25R256DY1GR

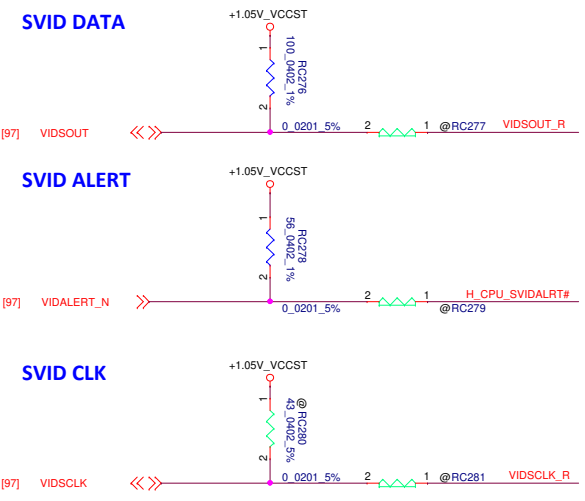


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Trace Length Match < 25 mils
 Must be routed as differential pair to VR
 RC374, RC375 should be placed within 2 inches (50.8 mm) of the CPU.

1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
 2. Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU



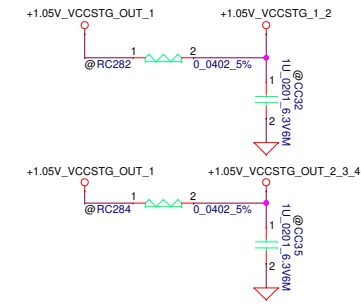
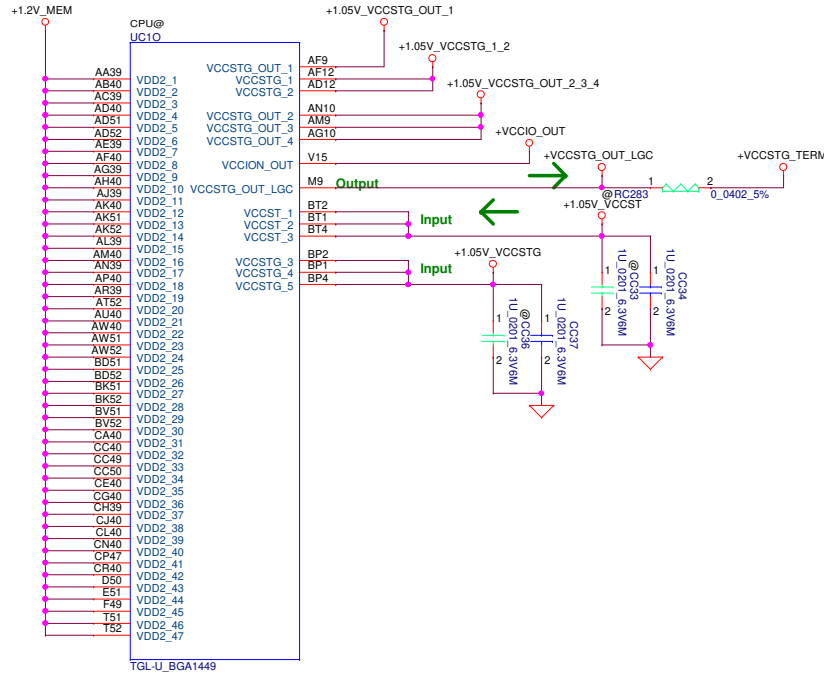
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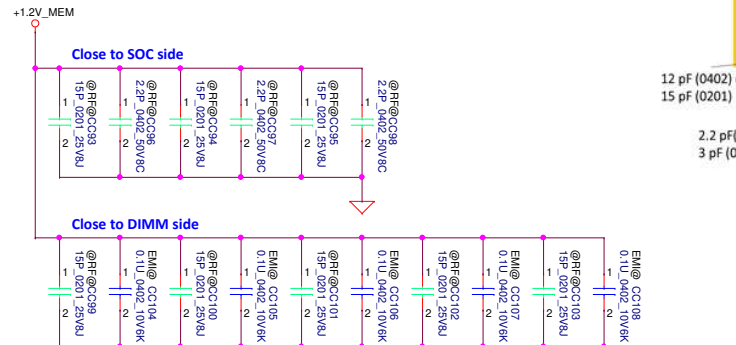
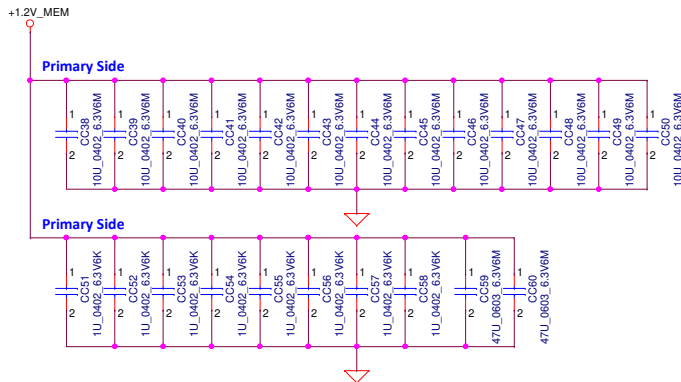
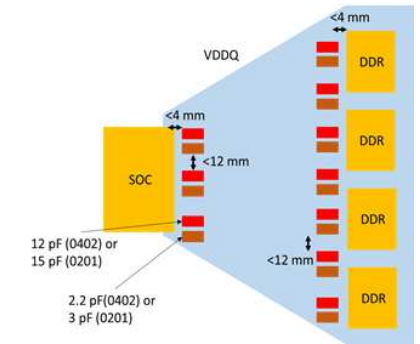
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 TGL-UP3_8L_T3_SS_VDD2 sheet
 VDD2:
 Primary Side cap
 2x 47uF 0603 + 8x 1uF 0402 + 13x 10uF 0402

607872_TGL_UP3_PDG_Rev1p1.xlsx
 EMC DDR RFI Mitigation sheet
 DDR Power Plane RF cap Decoupling
 Caps Qty reference RVP
 609003-tgl-up3-ddr4-sodimm-rvp-tdk-rev1p0
 PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART

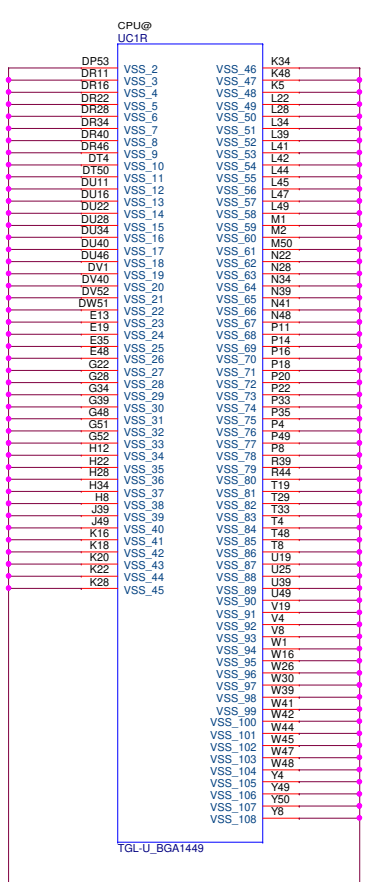
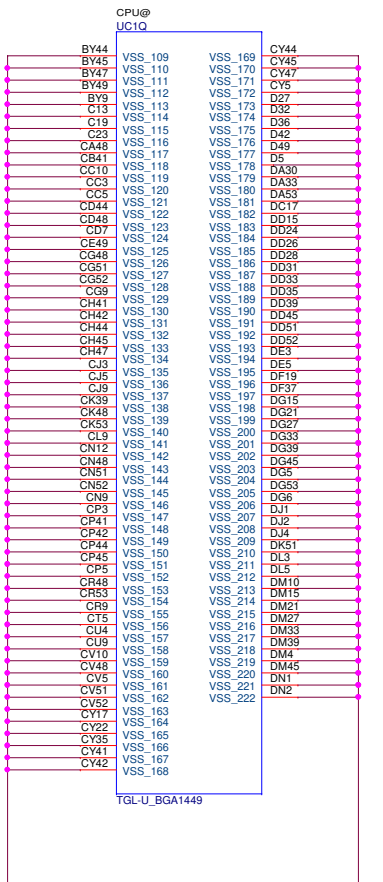
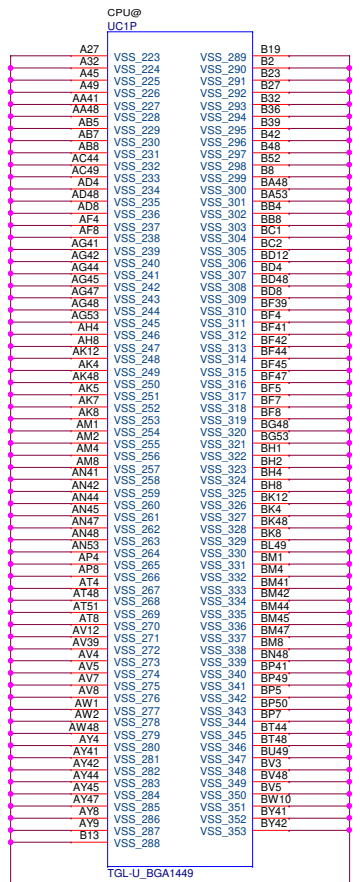


CC104,CC105,CC106,CC107,CC108 based on EMI request ,change to 0.1U_0402_10V6K from 2.2P_0402_50V8C

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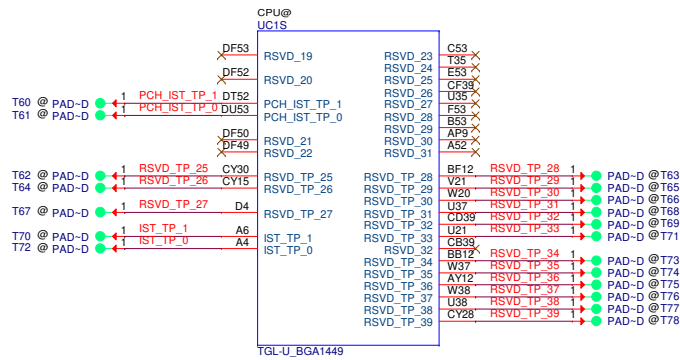
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MCP(12/13)VSS		
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Reserve


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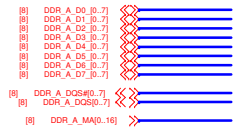
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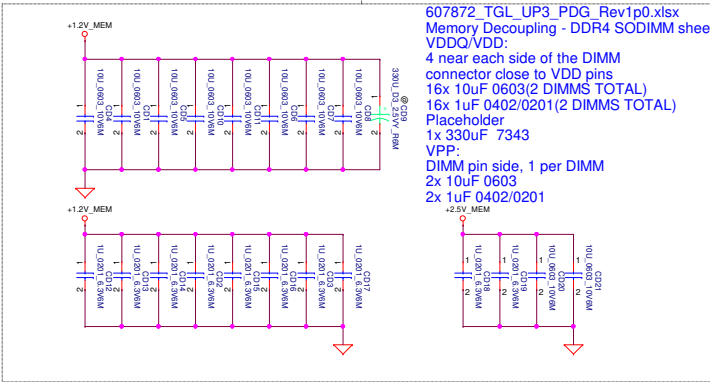
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		Compal Electronics, Inc.	
Title		SOC or PCH / FCH	
Size	Document Number		Rev
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Link LOTES_ADDR0206-P001A02 done 0410

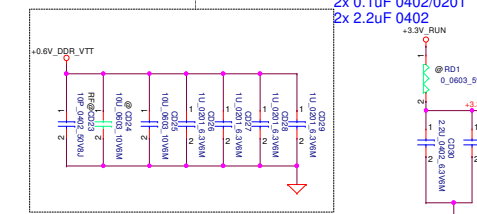


Layout Note:
Place near JDIMM1



607872_TGL_UP3_PDG_Rev1p0.xlsx
Memory Decoupling - DDR4 SODIMM sheet
VDDQ/VDD:
4 near each side of the DIMM
connector close to VDD pins
16x 10uF 0603(2 DIMMS TOTAL)
16x 1uF 0402/0201(2 DIMMS TOTAL)
1x 330uF 7343
VPP:
DIMM pin side, 1 per DIMM
2x 10uF 0603
2x 1uF 0402/0201

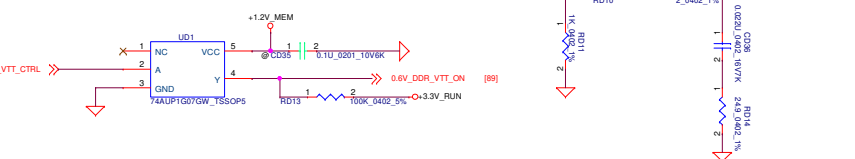
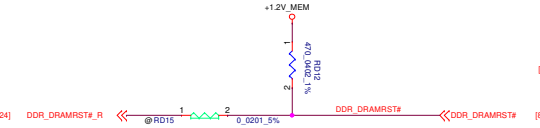
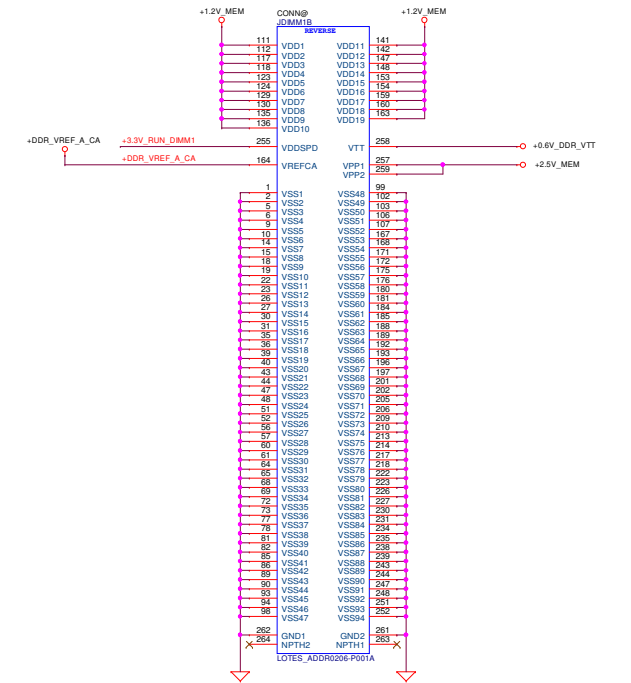
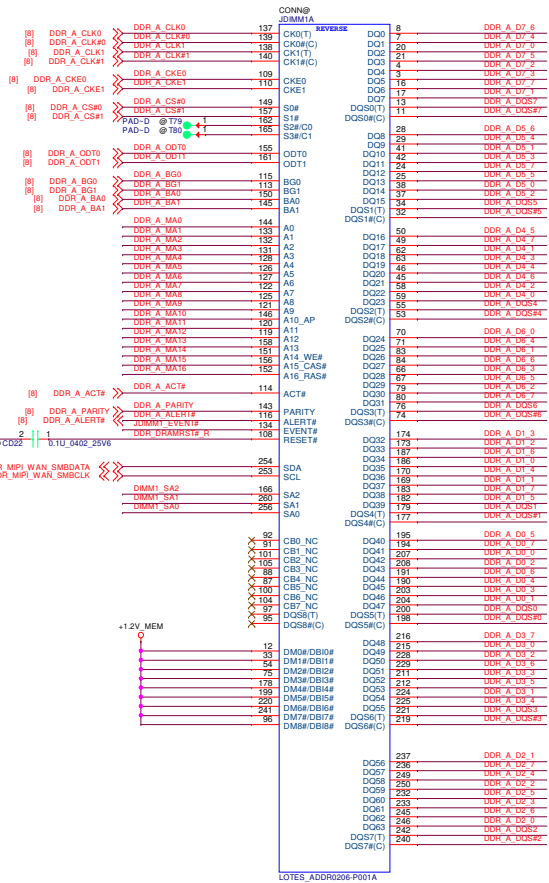
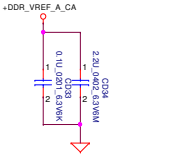
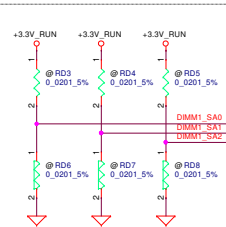
Layout Note:
Place near JDIMM1.258



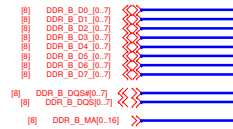
607872_TGL_UP3_PDG_Rev1p0.xlsx
Memory Decoupling - DDR4 SODIMM sheet
VTT:
Place on VTT plane close to SODIMM
2x 10uF 0603(1 cap stuffed, 1 placeholder)
4x 1uF 0402/0201
VDDSPD:
Place close to DIMM
2x 0.1uF 0402/0201
2x 2.2uF 0402

DIMM Select

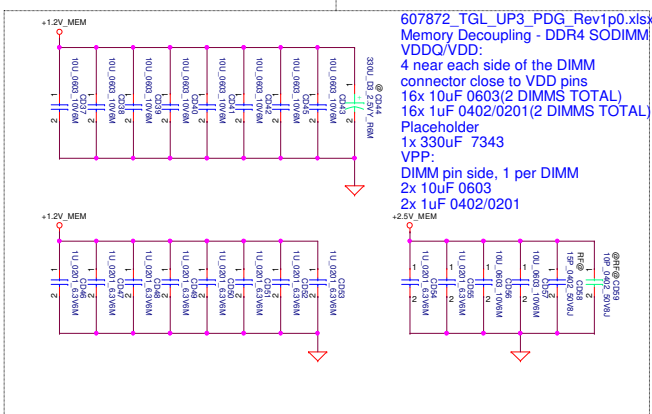
	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



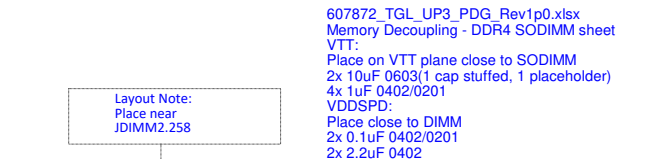
Link LOTES_ADDR0206-P001A02 done 0410



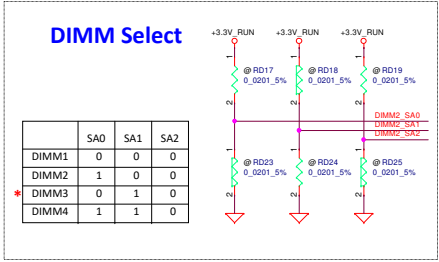
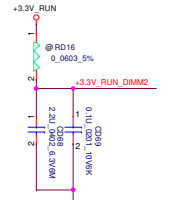
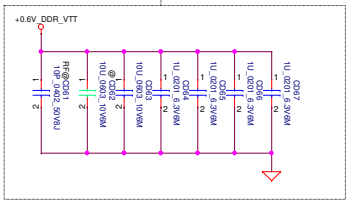
Layout Note:
Place near JDIMM2



607872_TGL_UP3_PDG_Rev1p0.xlsx
Memory Decoupling - DDR4 SODIMM sheet
VDDQ/VDD:
4 near each side of the DIMM connector close to VDD pins
16x 10uF 0603(2 DIMMS TOTAL)
16x 1uF 0402/0201(2 DIMMS TOTAL)
Placeholder
1x 330uF 7343
VPP:
DIMM pin side, 1 per DIMM
2x 10uF 0603
2x 1uF 0402/0201

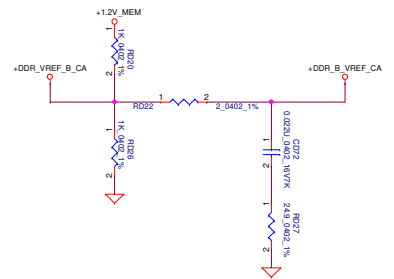
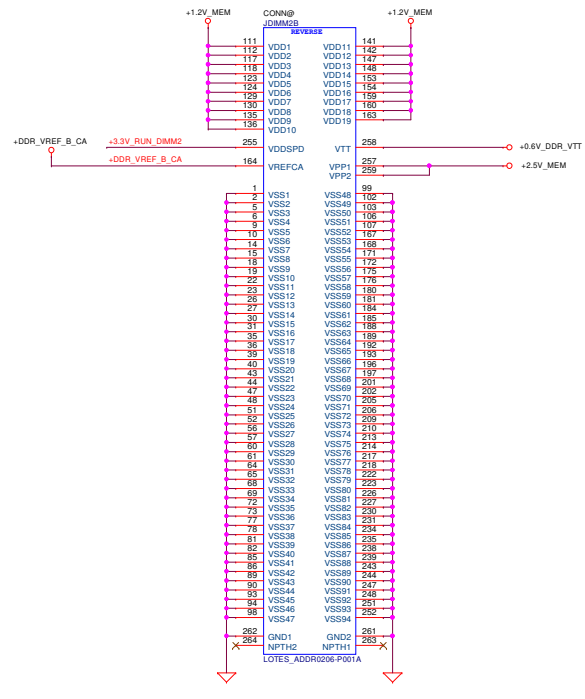
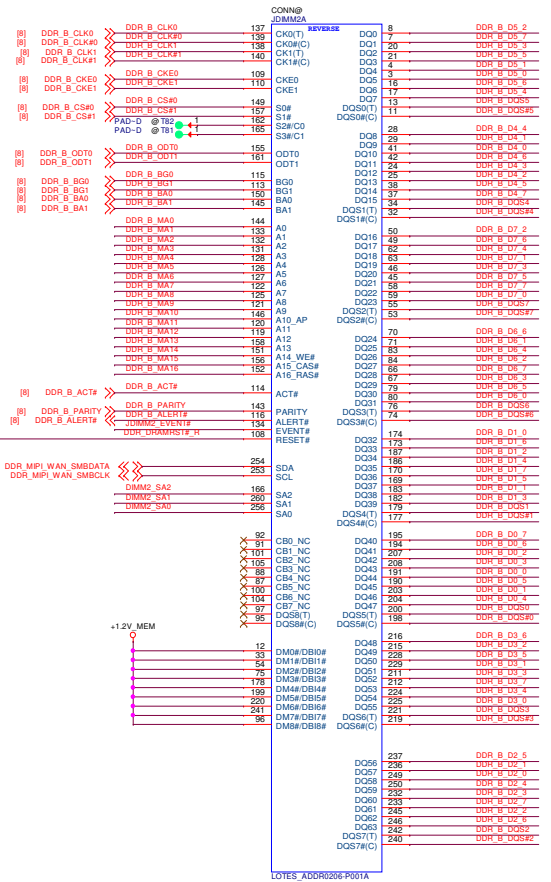


607872_TGL_UP3_PDG_Rev1p0.xlsx
Memory Decoupling - DDR4 SODIMM sheet
VTT:
Place on VTT plane close to SODIMM
4x 1uF 0402/0201
VDDSPD:
Place close to DIMM
2x 0.1uF 0402/0201
2x 2.2uF 0402



DIMM Select


	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



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Title		GPU	
Size	Document Number	Rev	
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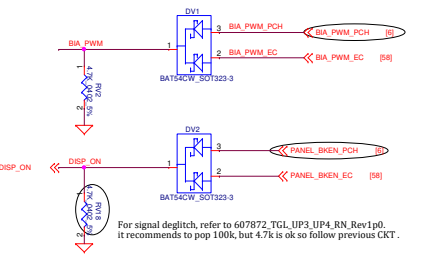
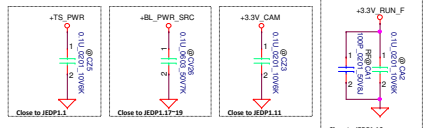
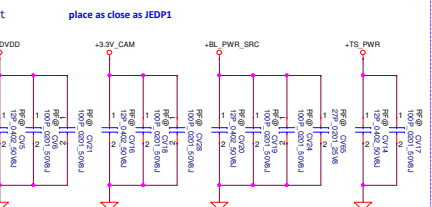
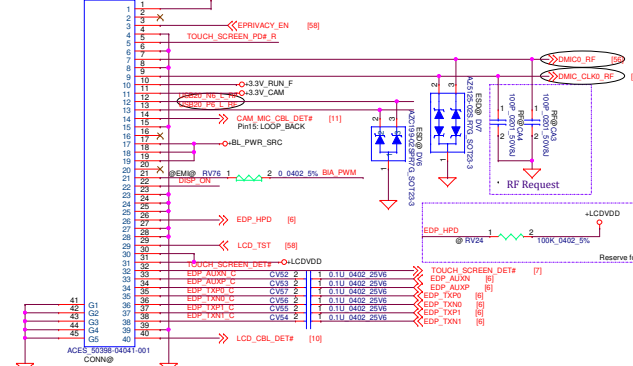


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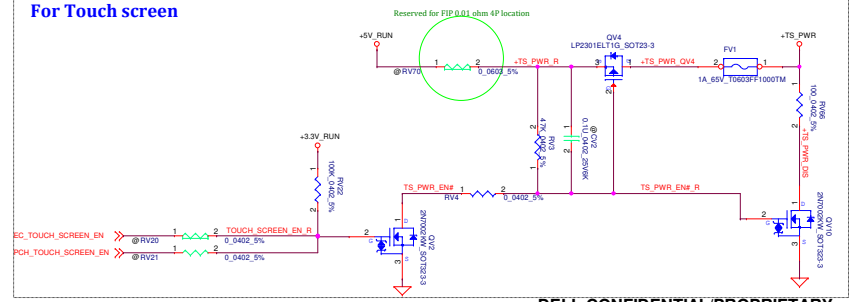
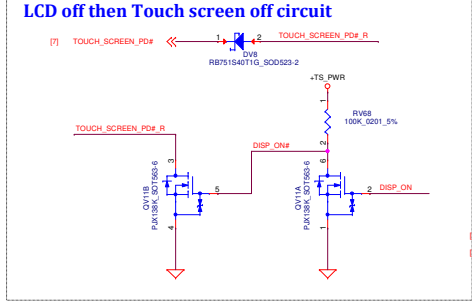
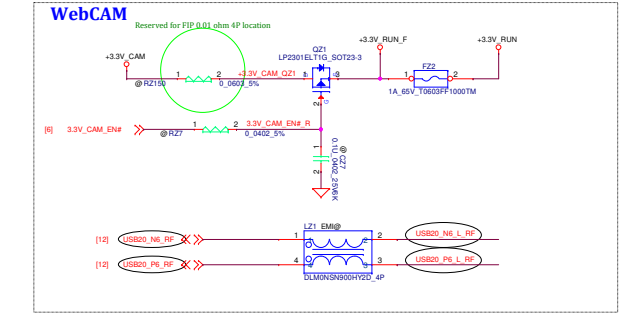
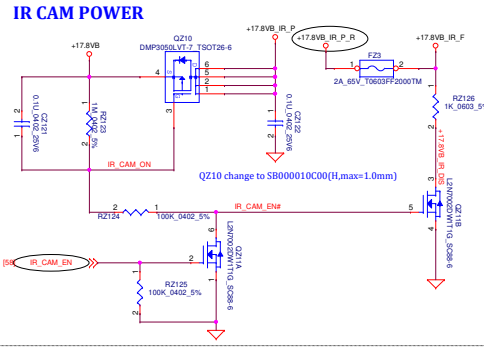
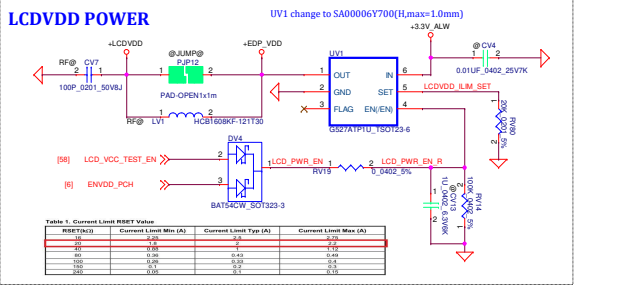
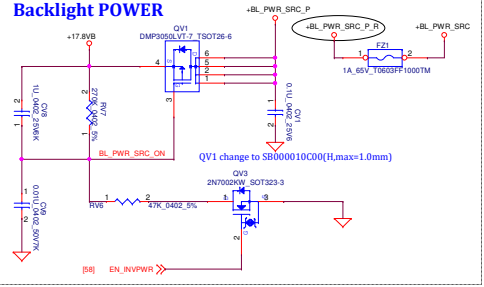
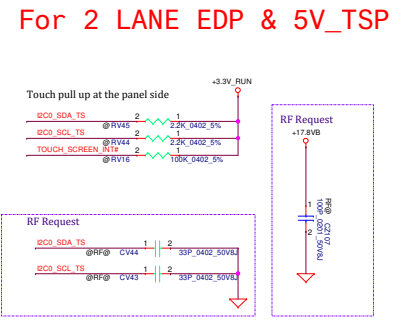
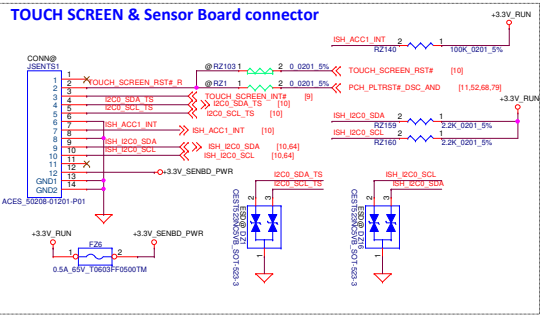
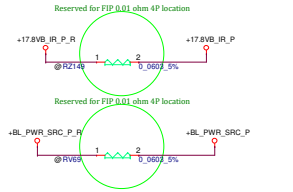
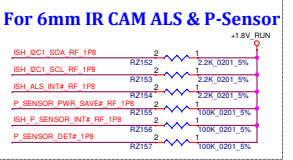
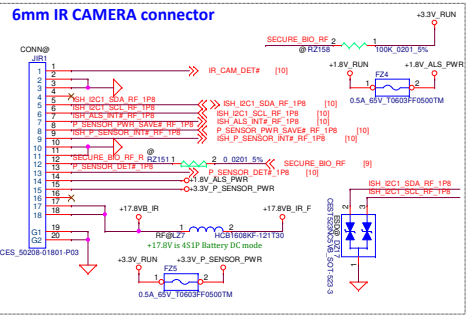
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Title		
GPU DC/DC Interface		
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LINK 50398-04041-001 DONE
Due to SB12/14 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table



Camera Truth table	Mic Only	6mm RGB Camera	6mm IR Camera w/o sensor	6mm IR Camera with sensor
GPP_F19(CAM_MIC_CBL_DET#)	L	L	L	L
GPP_C15(IR_CAM_DET#)	H	H	H	L
GPP_C10(P_SENSOR_DET#_1P8)	H	H	H	L



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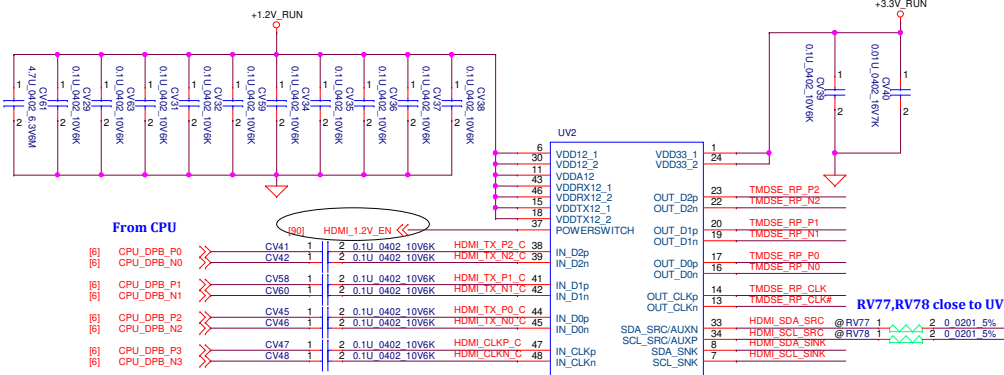
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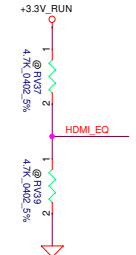
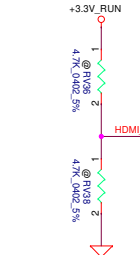
Title		DP	
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From CPU

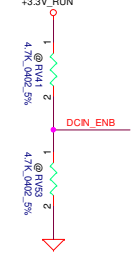
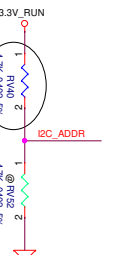
HDMI_RST# internally pulled up at ~150K.

PDB (Chip PWR down)
 HIGH(DEFAULT) Normal operation
 LOW Chip PWR down
 Internal 150K PU



Output pre-emphasis setting. Internally pulled up at ~150K, 3.3V/I/O.
 L: Programmable pre-emphasis to 2.5dB
 H: No pre-emphasis (default)

Receiver equalization setting. Internally pulled up at ~150K, 3.3V/I/O.
 L: Programmable EQ for channel loss up to 15.6dB
 H: Programmable EQ for channel loss up to 17dB (default)
 M: Programmable EQ for channel loss up to 11dB



I2C address selection. Internally pulled down at ~150K.
 L: Slave address 0x10-0x2B (default)
 H: Slave address 0x90-0x9F;0xD0-0xDF

DC coupling enable. Internally pulled up at ~150K.
 L: DC coupling input
 H: AC coupling input (default)

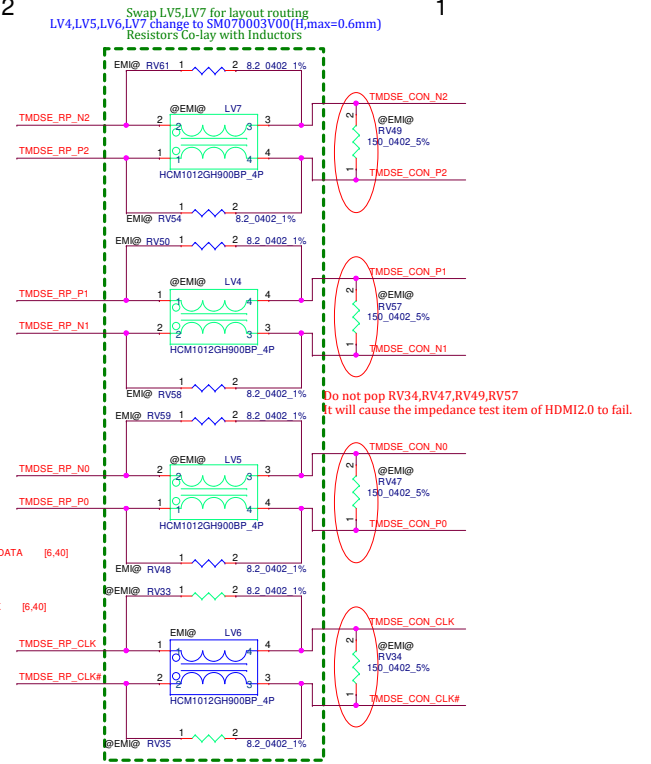
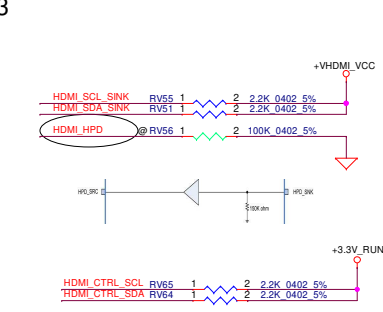
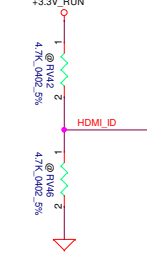
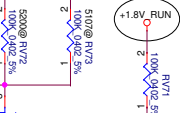
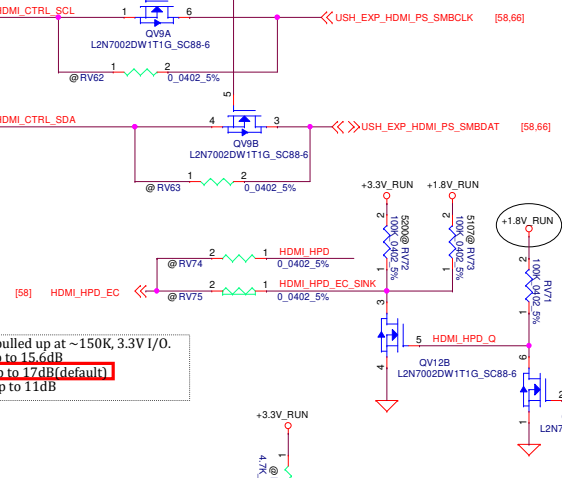
Configuration pin. Internally pulled down at ~150K.
 L: HDMI ID enable (default)
 H: HDMI ID disable

RV77, RV78 close to UV2

HDMI_HPD_SINK internally pulled down at ~100K.

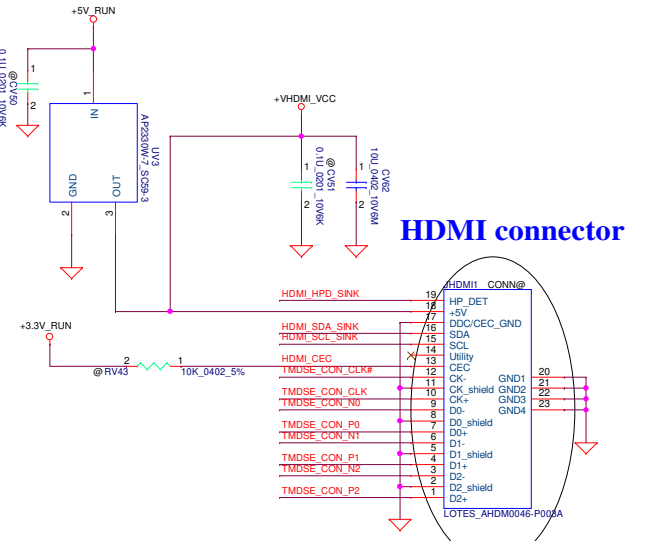
PS8409 DDC bypass circuit
 If used need pop QV13, RC1, RC2, RV53, RV81, RV82;
 need depop RV77, RV78
 QV13, RV81, RV82 close to UV2

Need to use low capacitance MOSFET on DDC_SDA/SCL
 (Total capacitance of signal <=50pF)



Do not pop RV34, RV47, RV49, RV57
 It will cause the impedance test item of HDMI2.0 to fail.

HDMI connector



Link LOTES_AHDM0046-P003A done

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HDMI2.0 CONN
 LA-K491P
 Date: Tuesday, December 08, 2020 Sheet 40 of 128

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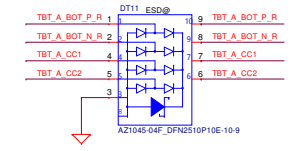
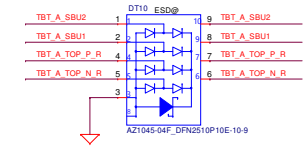
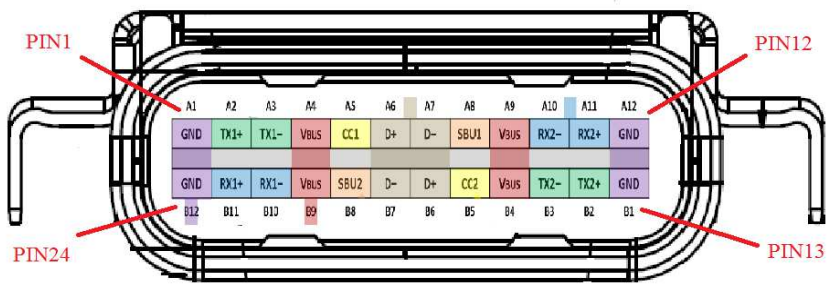
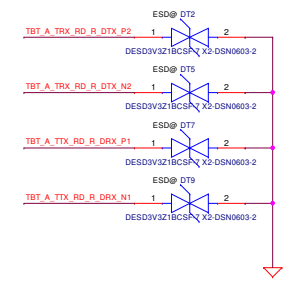
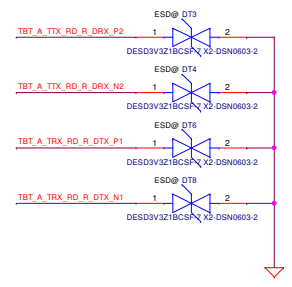
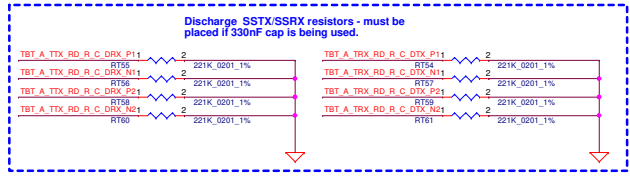
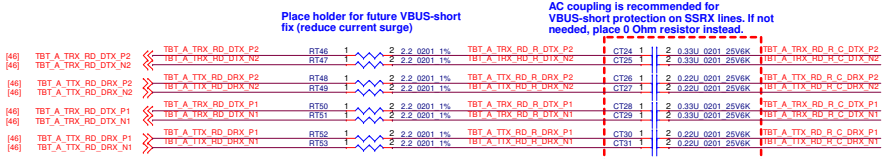
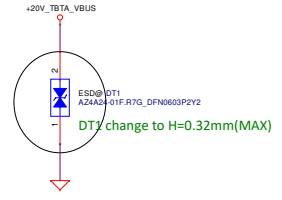
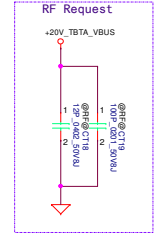
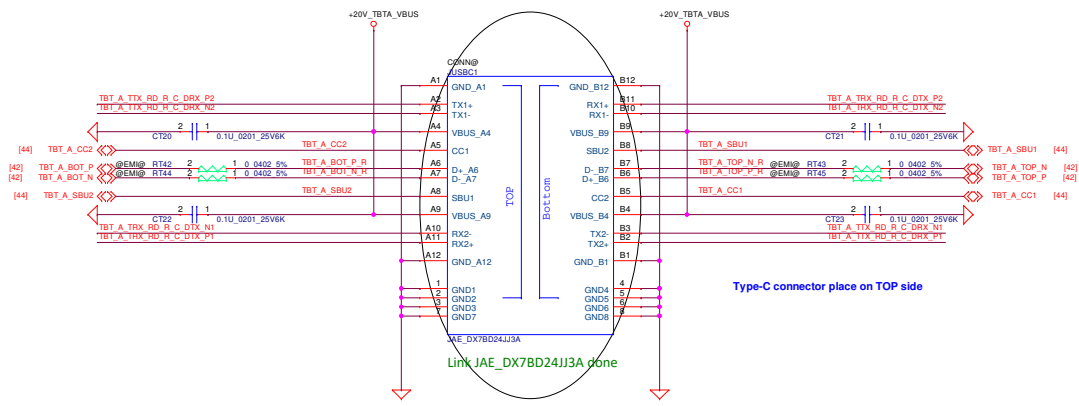


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For Type-C port 1(Support DDM)



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Compal Electronics, Inc.
[TypeC]Connector Port1
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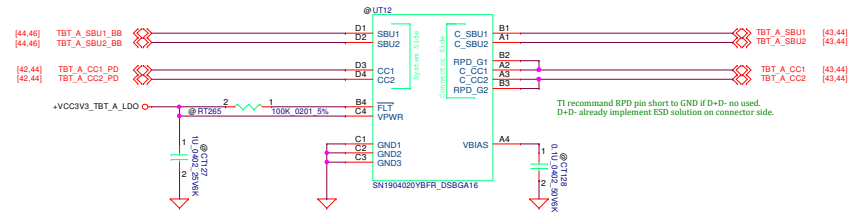
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Type-C Port 1

Bypass



Reserved short-to-VBUS overvoltage and IEC ESD Protection

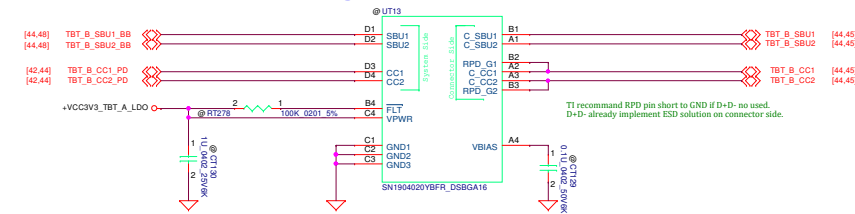


Type-C Port 2

Bypass



Reserved short-to-VBUS overvoltage and IEC ESD Protection



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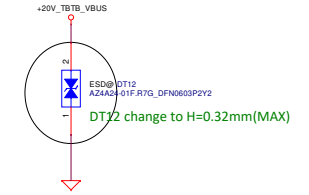
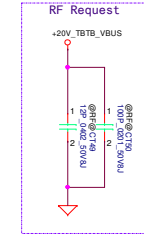
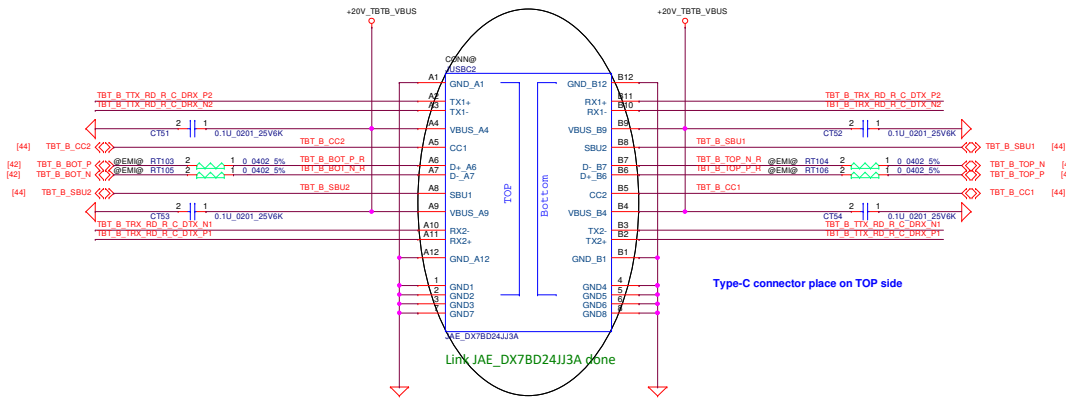


Title: [TypeC]VBUS short protector
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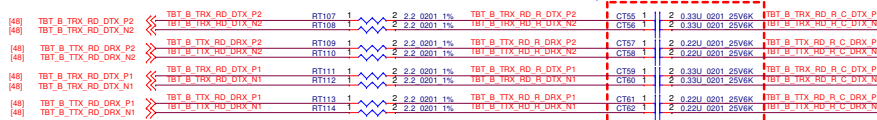
Rev 2.0

JAE X12 DX07BD24J3 with X10 DX07BD24J2 same layout

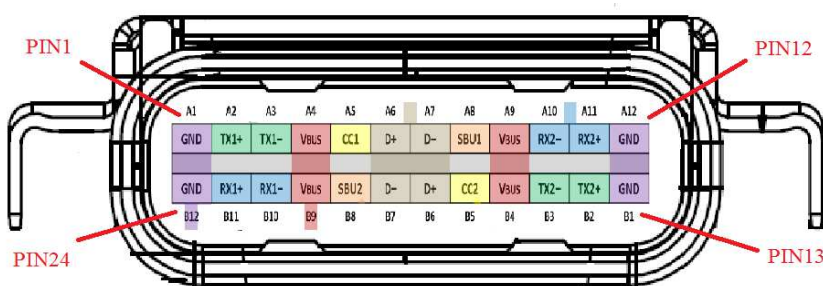
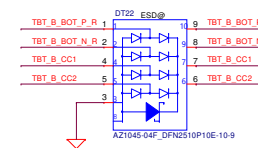
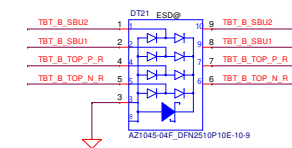
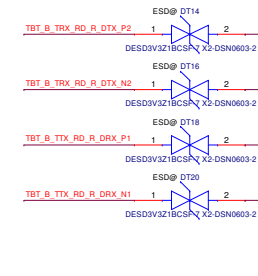
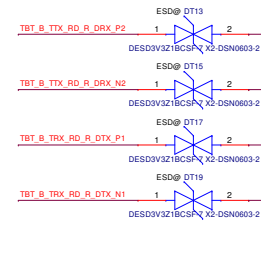
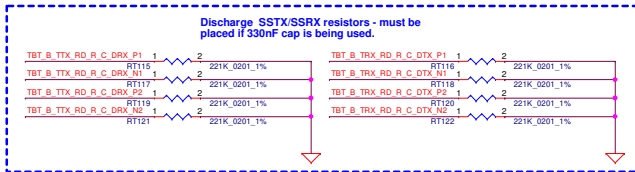


Place holder for future VBUS-short fix (reduce current surge)

AC coupling is recommended for VBUS-short protection on SSRX lines. If not needed, place 0 Ohm resistor instead.



Discharge SSTX/SSRX resistors - must be placed if 330nF cap is being used.



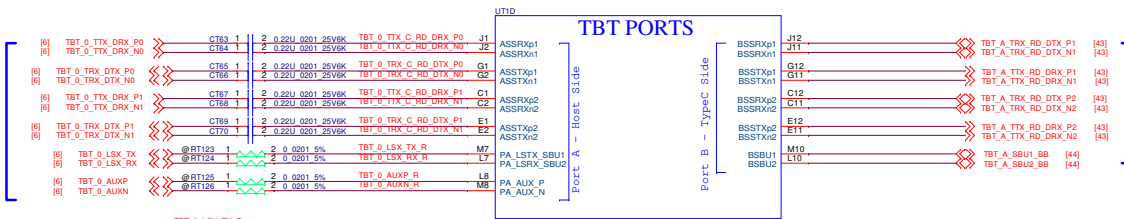
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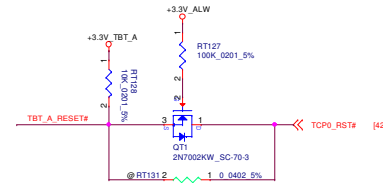
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Size	Document Number	Rev	2.0
LA-K491P			
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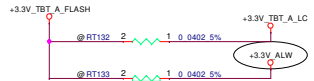
From CPU



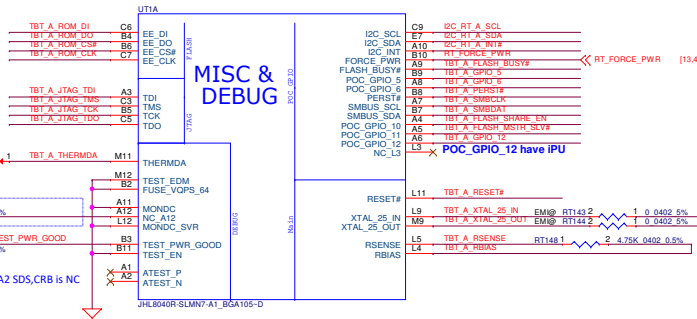
To Type-C Port1 connector



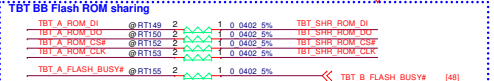
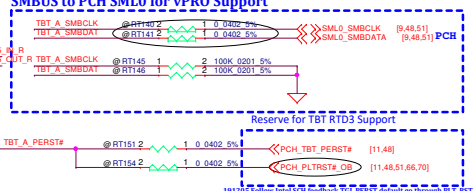
Follow Single Burnside Bridge Host Reference Design Rev 1.8



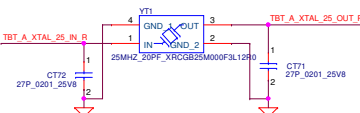
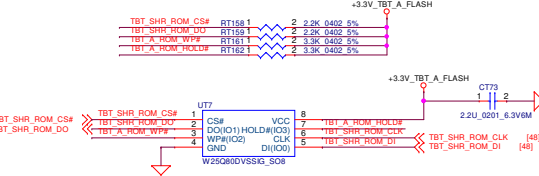
MISC & DEBUG



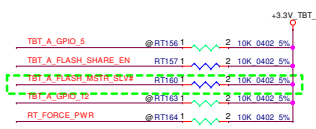
SMBUS to PCH SML0 for vPRO Support



Flash Sharing between 2 Re-timers:
 * SPI signals should be shared (DG_EE_DI, DG_EE_DO, DG_EE_CS#, DG_EE_CLK)
 * DG_FLASH_BUSY# should be shared between BBR#1 and BBR#2 with PU to PW_VCC3X3_SV_SYS
 * DG_FLASH_MSTR_SLV of BBR#1 (set as Master) should be PU and PD for BBR#2 (set as Slave)
 * DG_FLASH_SHARE_EN should be PU.



RT ref p.5 XTAL Recommended FW2000252 by Pericom XRCGB25M00F3L12R0 by Murata
 Suggest adding GND shield across Crystal and 10pF caps for better RF.



(L11) DG_P1_RST#:
 For PD based systems, DG_P1_RST# should be output from PD.
 For TCPC based systems, DG_P1_RST# should be output from SOC/EC.

(B10) FORCE_PWR: Connect to PCH for FW update
 '0' - by default
 '1' - for debug only

(A9) DG_FLASH_BUSY#: connection to PU

(A4) DG_FLASH_SHARE_EN (IPU):
 '0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.
 '1' - Flash is shared between 2 Re-timers.

(A5) DG_FLASH_MSTR_SLV (IPU):
 '0' - Set Re-timer to be Slave on shared flash SPI I/F.
 '1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG_POC_GPIO6:
 '0' - Reserved for debug
 '1' - Indication to S0 state for Re-timer

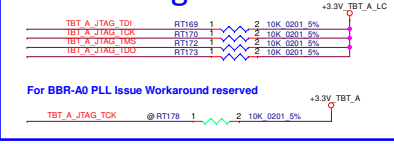
BBR ROM choice need follow Intel approved list

3.1 Flash Types Supported

Table 1.2. Supported Types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
AMIC	A25L080	8.0	3.0-3.6
Spansion	S25FL208K	8.0	2.7-3.6
Winbond	W25Q80DVSNI6	8.0 (8pin SOIC150 mil)	2.7-3.6
Macronix	MX25L8006M11	8.0 (150mil, 8-SOP)	2.7-3.6
Micron	M25PE80-VMM6TP	8.0 (150mil, SOB)	2.7-3.6
Micron	M25PX80-VMM6TP	8.0 (150mil, SOB)	2.3-3.6

JTAG Debug



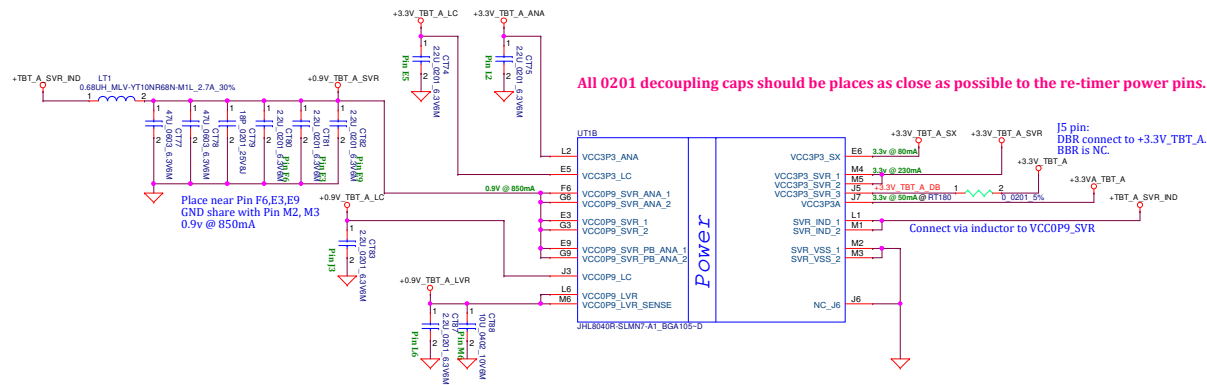
For BBR-A0 PLL Issue Workaround reserved

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TypeC|TBT BB TCSS Port1

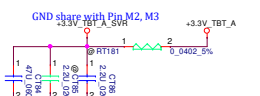
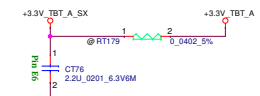
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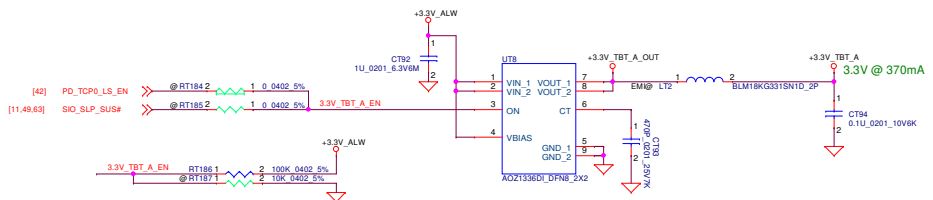
All 0201 decoupling caps should be placed as close as possible to the re-timer power pins.

Place near Pin F6,E3,E9
GND share with Pin M2, M3
0.9v @ 850mA

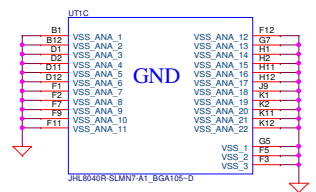
+3.3V_TBT_A_SX Ripple: 40mVp-p
Tolerance (+ 5%/ - 5%)
should be 3.465v maximum and 3.07v minimum for normal operation.



To support vPRO docking +3.3V_TBT_A should be always on even at S5.



BB ref sch p.6 note
DG_P1_PWR_GATE_EN:
For PD based systems, DG_P1_PWR_GATE_EN should be output from PD.
For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.



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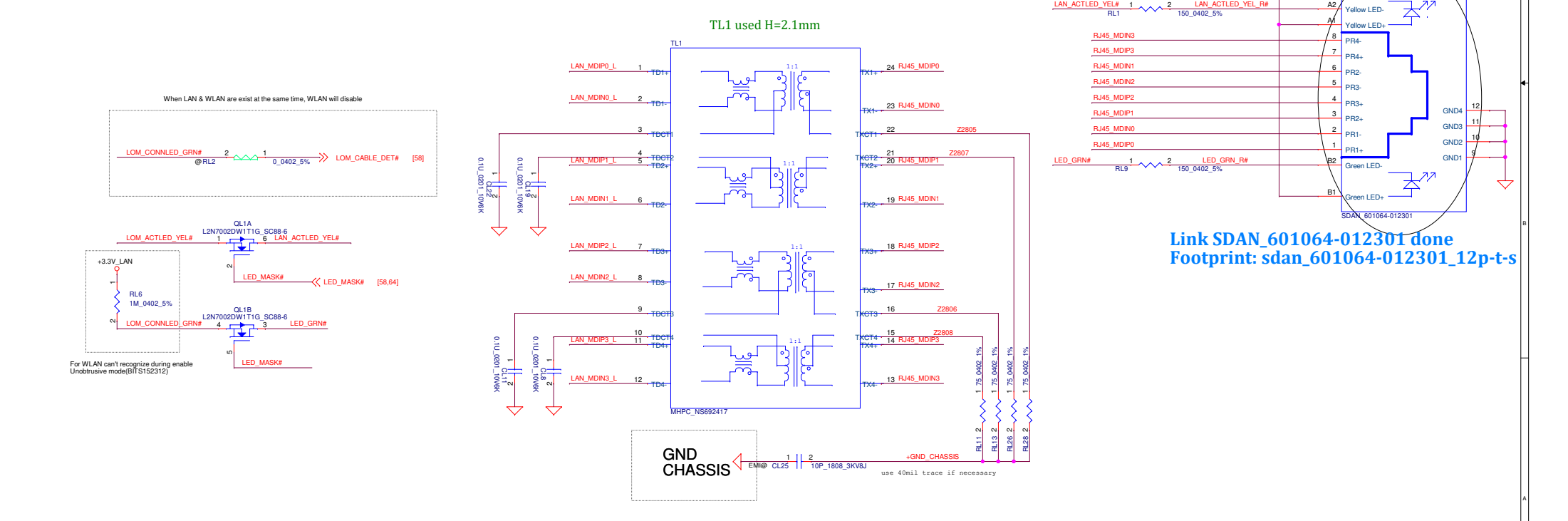
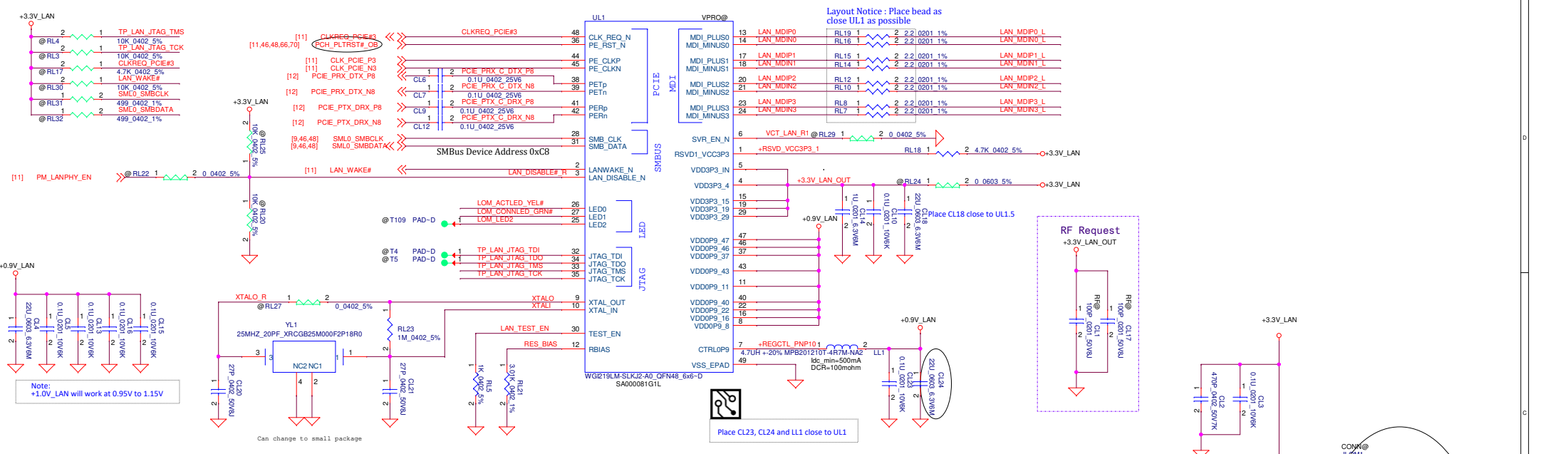
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Title **Reserve [Type C]PD Power**

Size Document Number **LA-K491P** Rev **2.0**

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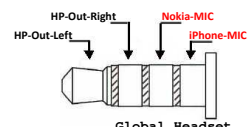
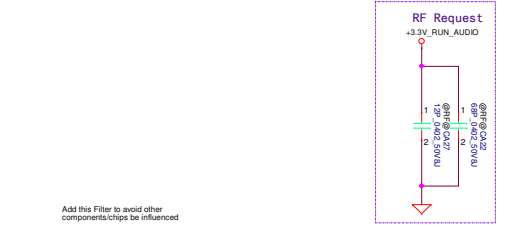
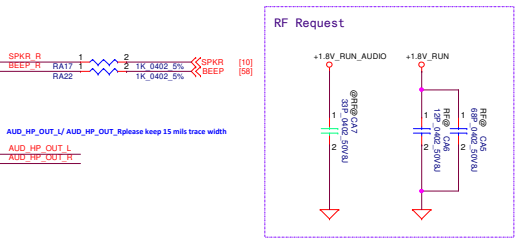
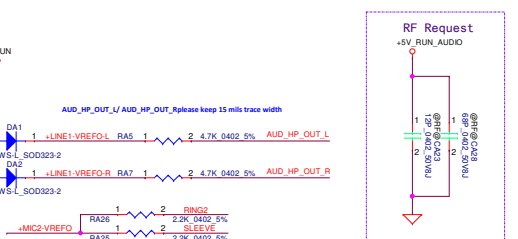
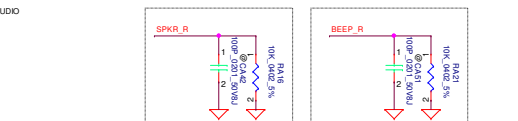
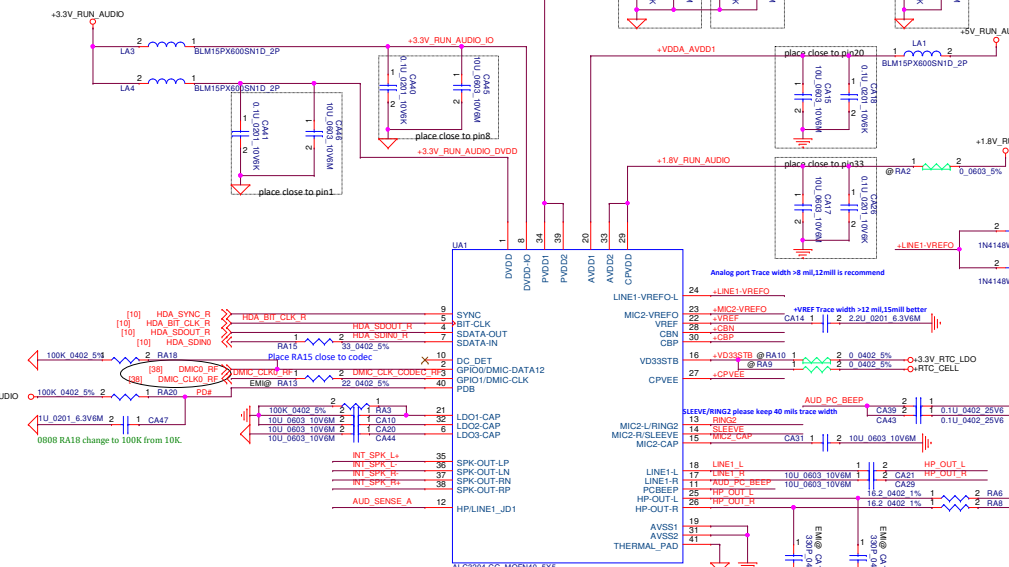
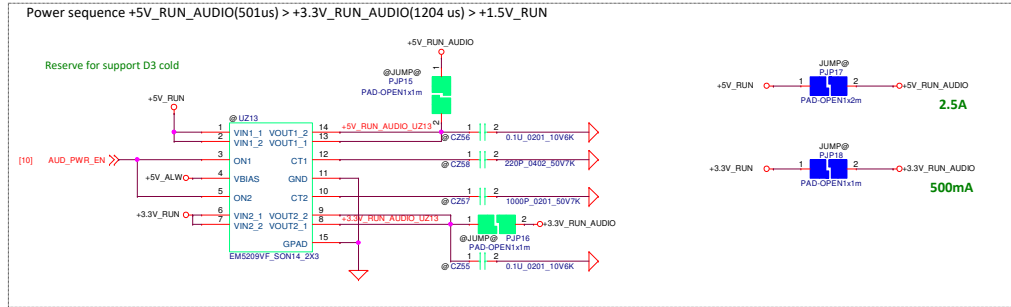
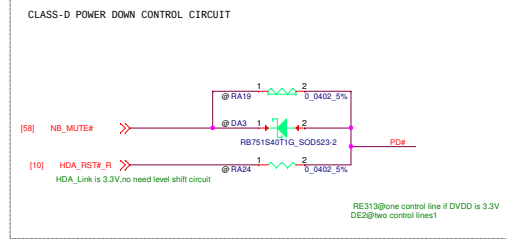
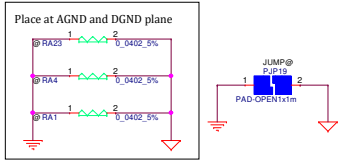
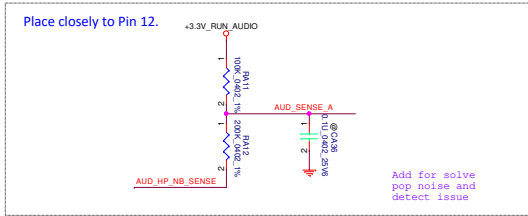
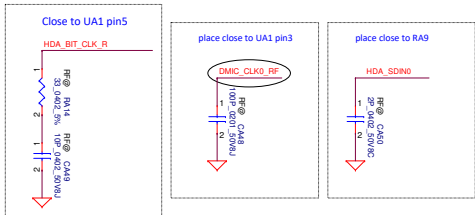
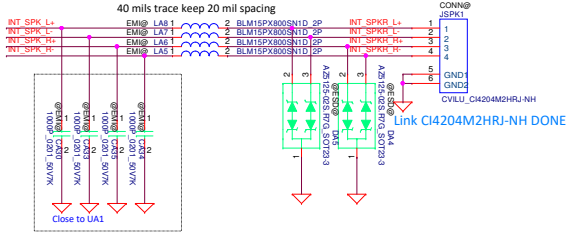
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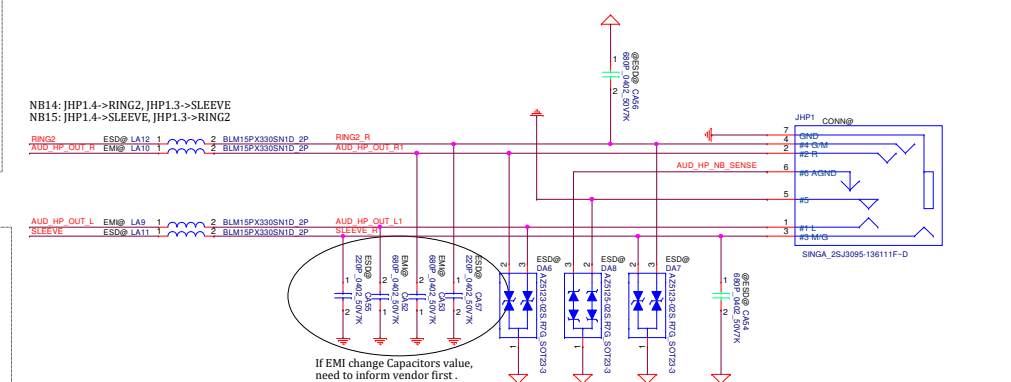
1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

Internal Speakers Header

40 mils trace keep 20 mil spacing



Universal Jack



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Codex ALC3204	
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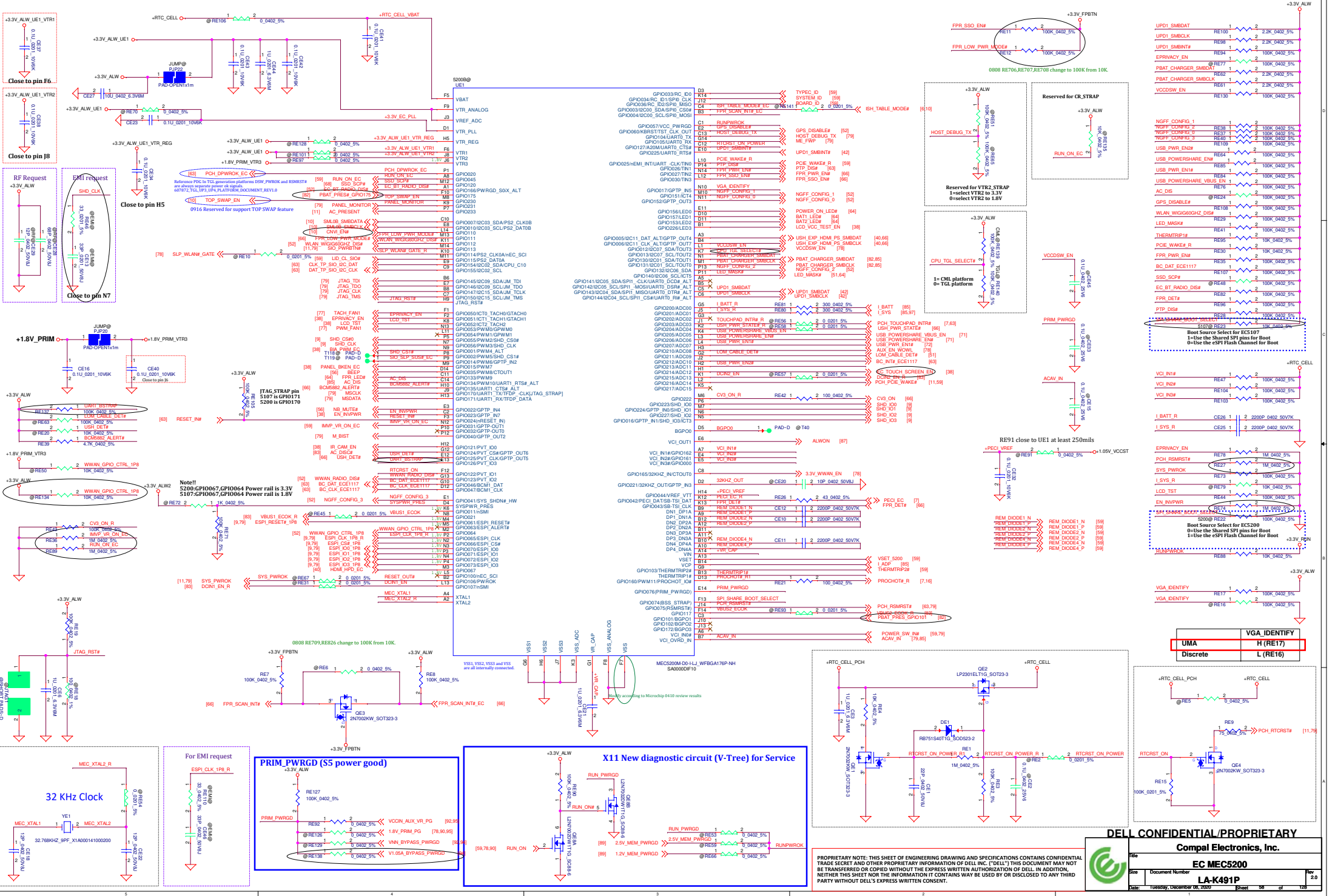
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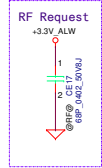
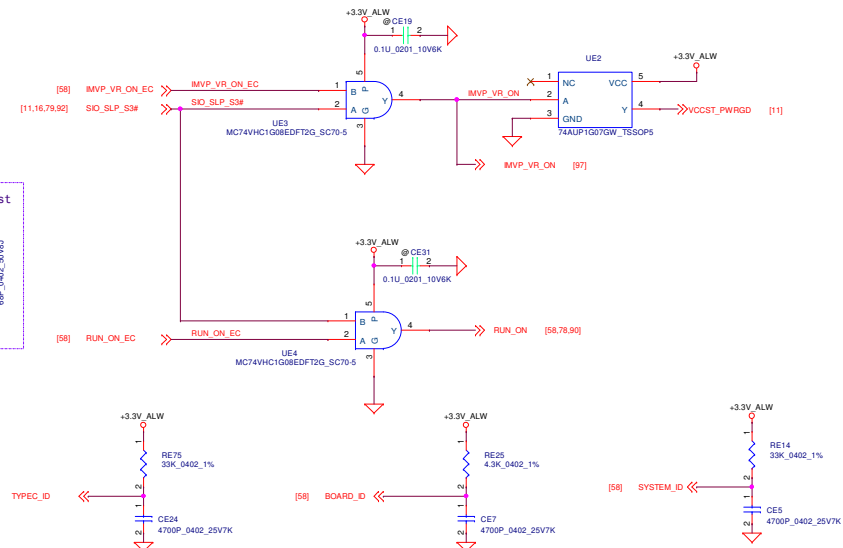
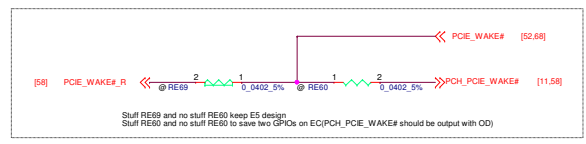
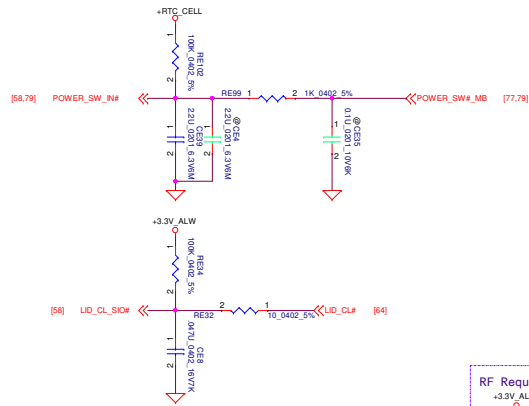
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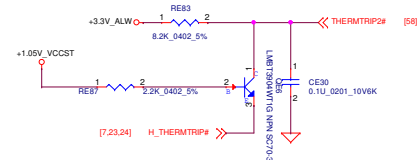
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Size	Document Number	LA-K491P	Rev 2.0
Date:	Tuesday, December 08, 2020	Sheet 57	of 128



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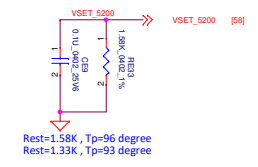
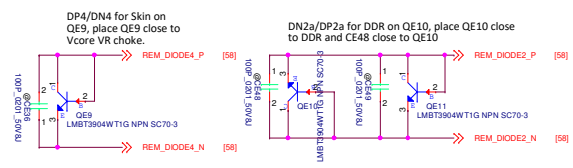
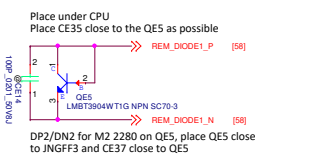
RE343	CE62	REV	RE79	CE40	REV	RE300	CE47	PANEL SIZE
240K	4700p	Single Port ACE w/o TR	240K	4700p	X00	240K	4700p	11"
130K	4700p	Single Port ACE w/TR	130K	4700p	X01	130K	4700p	12"
62K	4700p	Dual Port ACE w/o TR	62K	4700p	X02	62K	4700p	13"
* 33K	4700p	Dual Port ACE w/TR	33K	4700p	X03	* 33K	4700p	14"
8.2K	4700p	Dual Port ACE (w/TR +w/o TR)	8.2K	4700p	reserved	8.2K	4700p	15"
4.3K	4700p		* 4.3K	4700p	A00	4.3K	4700p	17"
2K	4700p		2K	4700p		2K	4700p	15P
1K	4700p		1K	4700p		1K	4700p	



TYPEC_ID rise time is measured from 0%~63.2% BOARD_ID rise time is measured from 0%~63.2% SYSTEM_ID rise time is measured from 0%~63.2%

Thermal diode mapping

5200 Channel	Location
DP1/DN1	CPU (QE5)
DP2/DN2	M2 2280 (QE11)
DN2a/DP2a	DDR (QE10)
DP3/DN3	NA
DP4/DN4	CPU VR (QE9)



Reserve

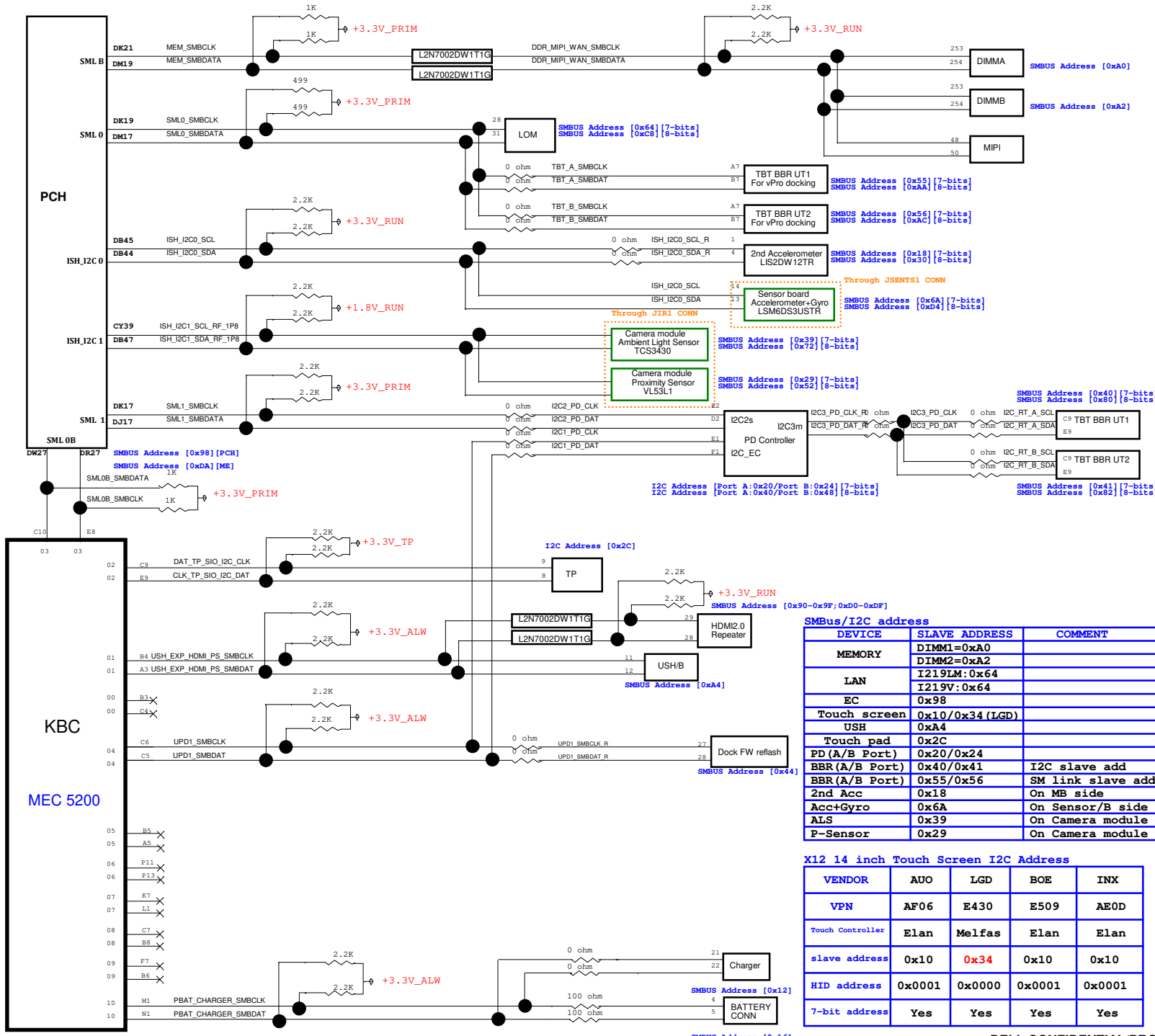
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Title		Secure & Reset IC	
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SMBus/I2C address

DEVICE	SLAVE ADDRESS	COMMENT
MEMORY	DIMM1=0xA0	
	DIMM2=0xA2	
	I219LM:0x64	
LAN	I219V:0x64	
	EC	0x98
Touch screen	0x10/0x34 (LGD)	
USB	0xA4	
Touch pad	0x2C	
PD (A/B Port)	0x20/0x24	
BBR (A/B Port)	0x40/0x41	I2C slave add
BBR (A/B Port)	0x55/0x56	SM link slave add
2nd Acc	0x18	On MB side
Acc+Gyro	0x6A	On Sensor/B side
ALS	0x39	On Camera module
P-Sensor	0x29	On Camera module

X12 14 inch Touch Screen I2C Address

VENDOR	AUO	LGD	BOE	INX
VPN	AF06	E430	E509	AE0D
Touch Controller	Elan	Melfas	Elan	Elan
slave address	0x10	0x34	0x10	0x10
HID address	0x0001	0x0000	0x0001	0x0001
7-bit address	Yes	Yes	Yes	Yes

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File: **SMBus Block Diagram**

Size: Document Number: **LA-K491P**

Date: Tuesday, December 06, 2010 Sheet 61 of 126 Rev: 2.0

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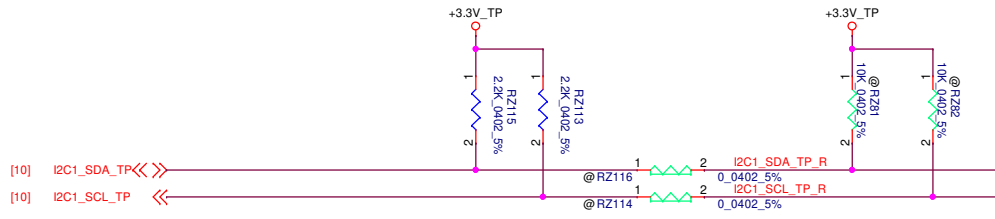
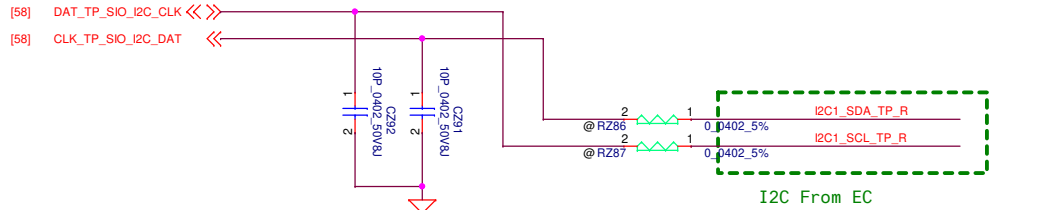


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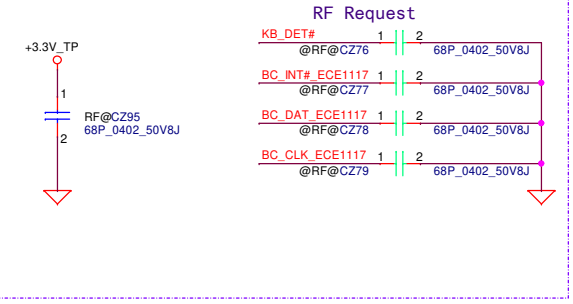
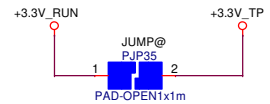
Title		LED (Controller)	
Size	Document Number	LA-K491P	Rev 2.0
Date:	Tuesday, December 08, 2020	Sheet 62	of 128

Touch Pad

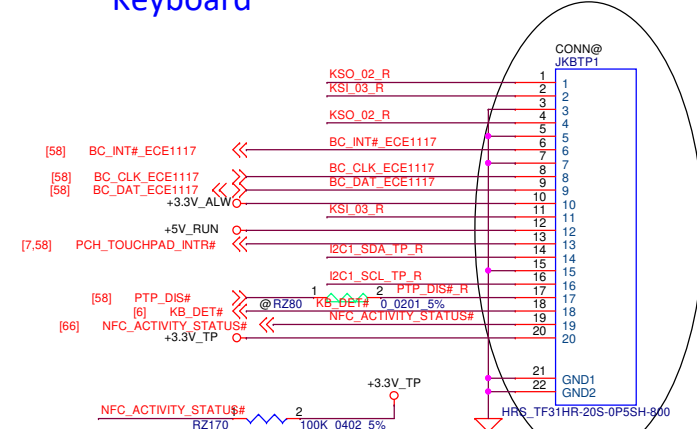


I2C From CPU

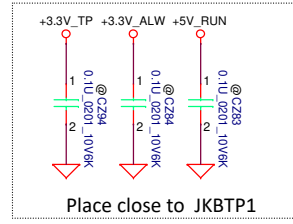
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7). For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows. Route PS2 from EC to the touch pad also for contingency plan if I2C has issues.



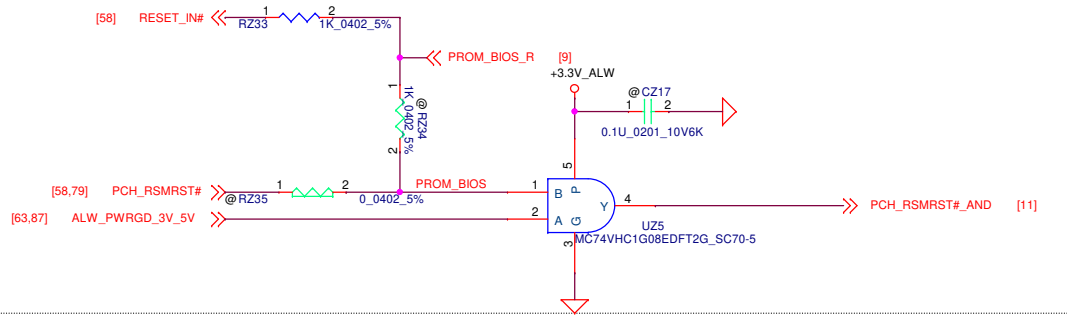
Keyboard



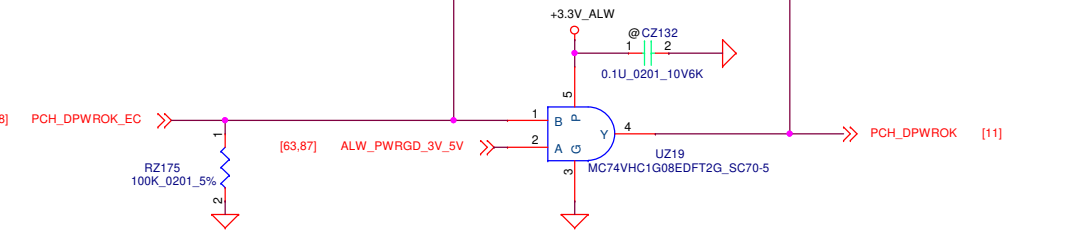
LINK HRS_TF31HR-20S-0P5SH-800 DONE



RSMRST circuit



DSW_PWROK circuit



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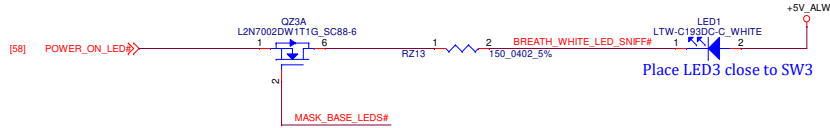
Title		Keyboard	
Size	Document Number	Rev 2.0	
Date: Tuesday, December 08, 2020		Sheet 63	of 128

Battery LED

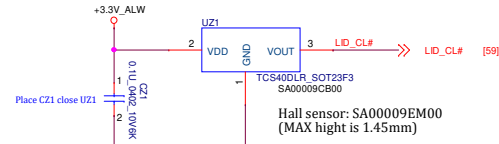


RZ32
NB14 used 470ohm
NB15 used 330ohm

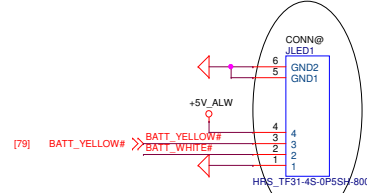
Breath LED



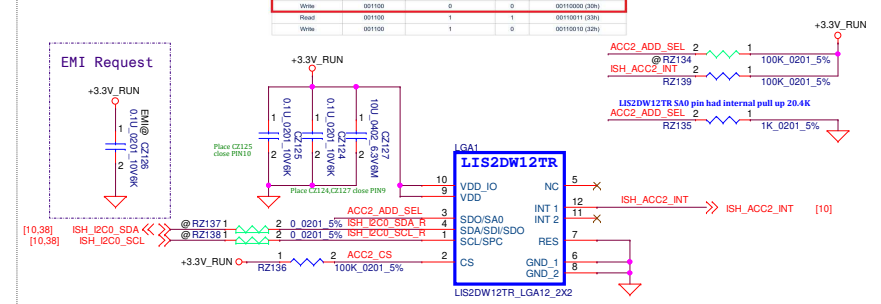
LID SWITCH



LED Board CONN



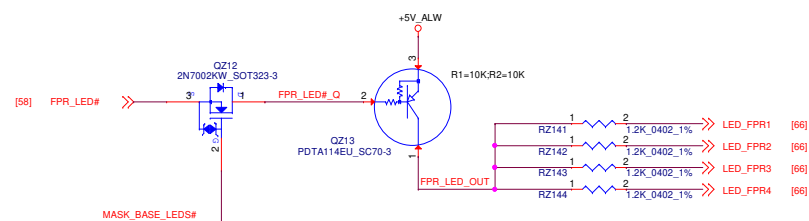
Accelerometer-16bit



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

FPR LED



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		Compal Electronics, Inc.	
		LED/Hall Sensor/ACC sensor	
File	Document Number		Rev
	LA-K491P		2.0
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Compal Electronics, Inc.		
Title		
Reserve for KB/TP/LED/LID		
Size	Document Number	Rev
	LA-K491P	2.0
Date:	Tuesday, December 08, 2020	Sheet 65 of 128

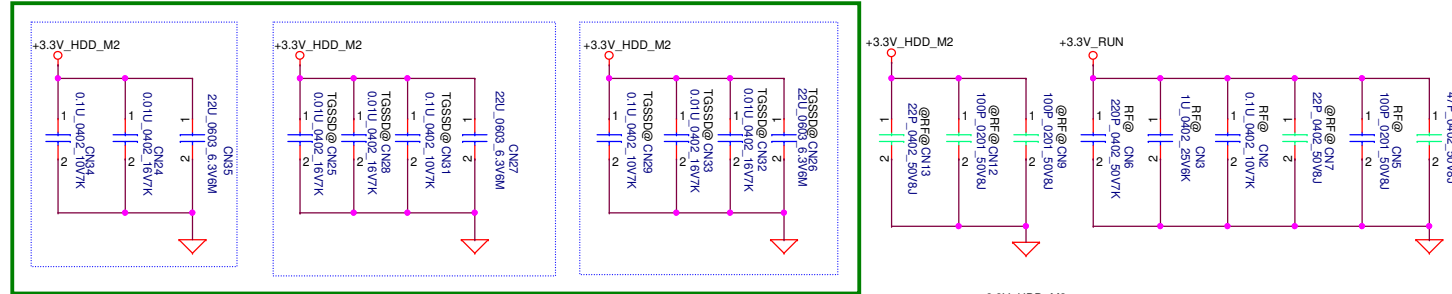
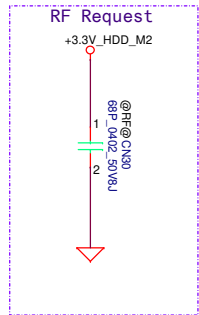
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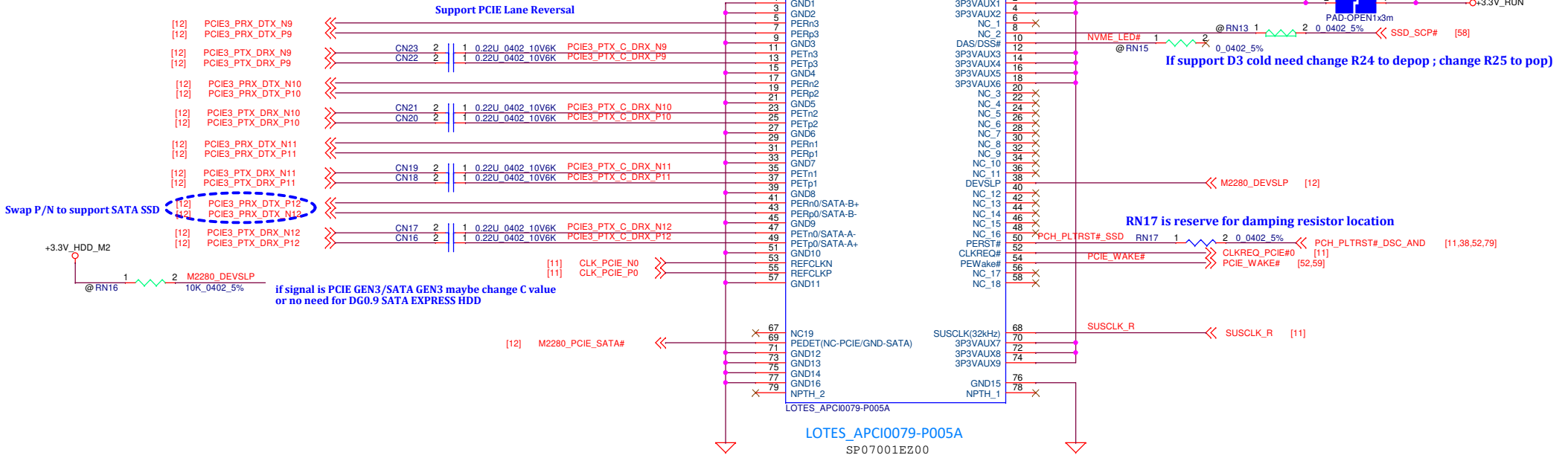
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	Title Reserve HDD/ODD/FFS Conn	
Size	Document Number LA-K491P	Rev 2.0
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Add Power Decoupling for support Intel Teton Glacier



2280 SSD
NGFF slot C Key M



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M2 2280 Socket

Title	M2 2280 Socket		Rev	2.0
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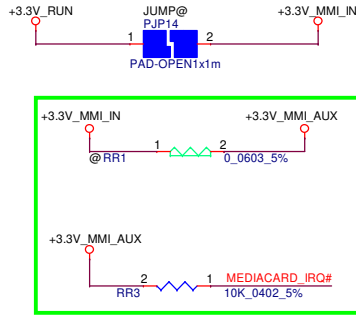
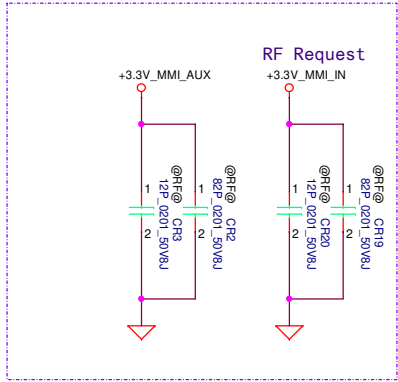


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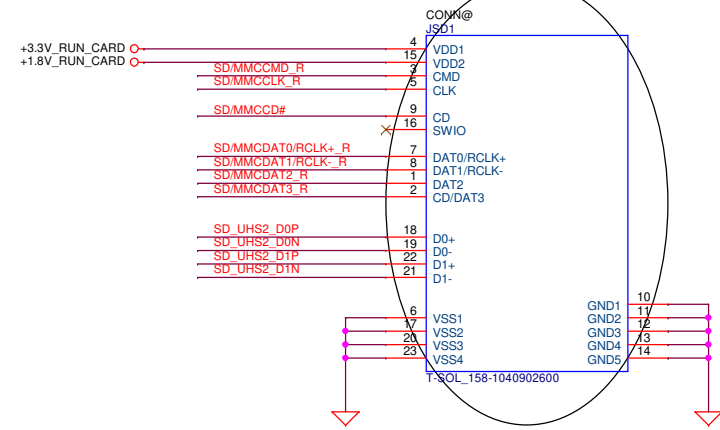
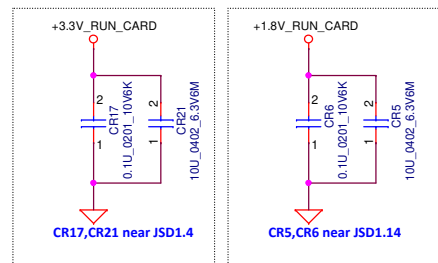
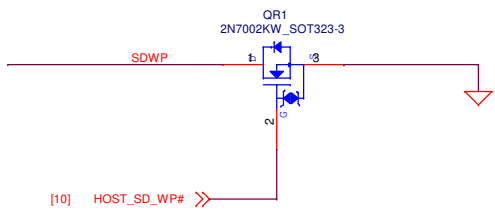
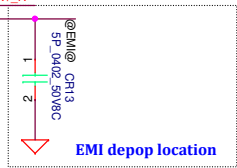
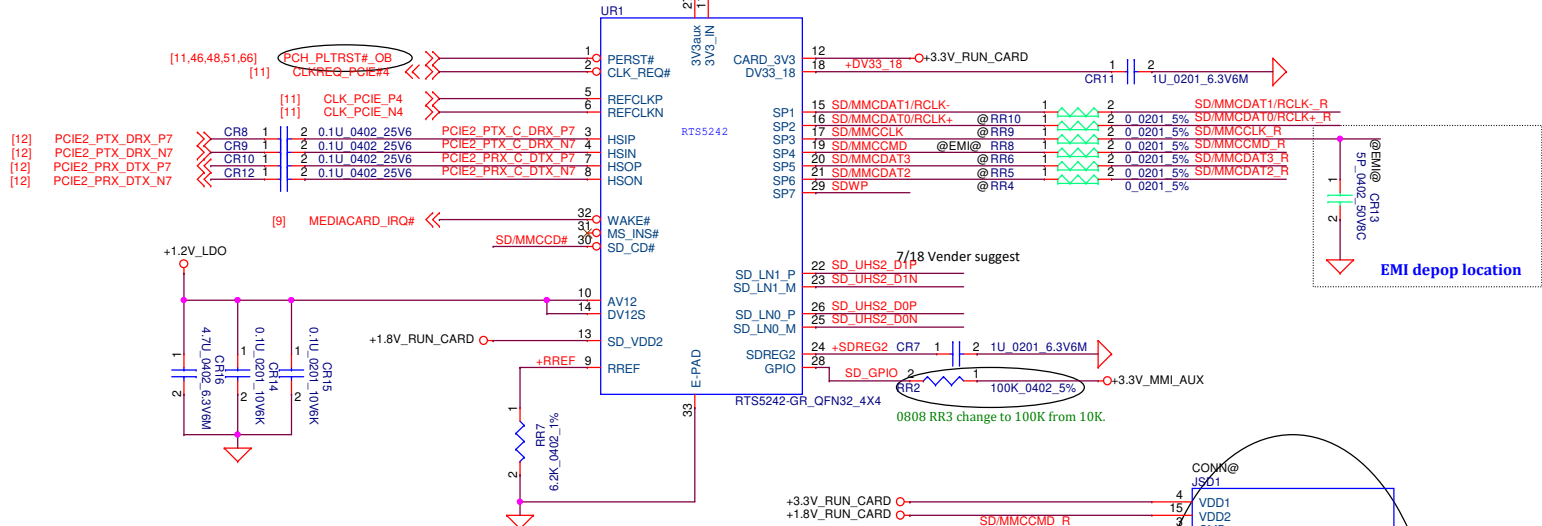
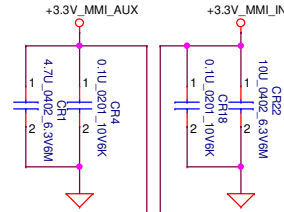
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Title		eMMC/UFS	
Size	Document Number	LA-K491P	Rev 2.0
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For PCIE Interface



Support D3 Hot(if support D3 cold need control PIN11 3V3_MMI_IN on/off)



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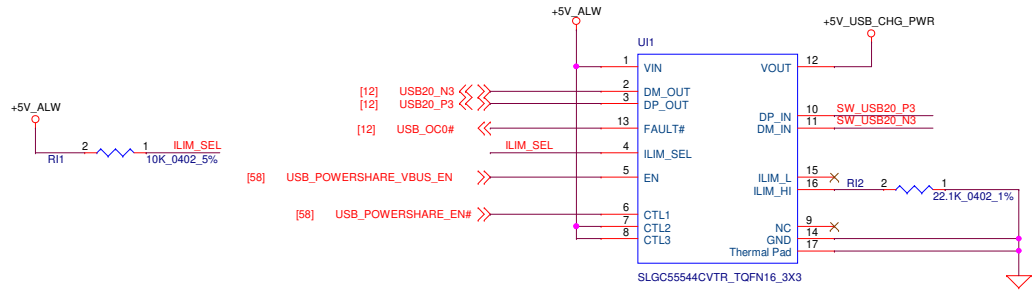
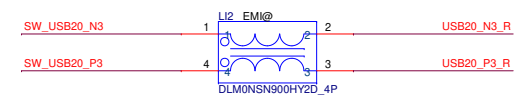
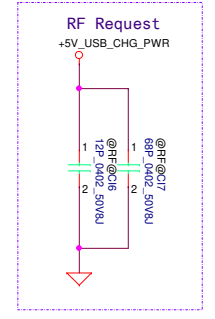
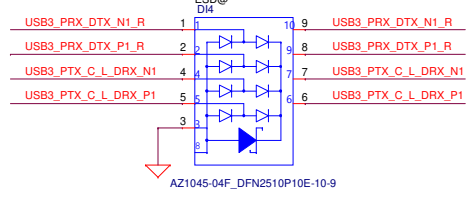
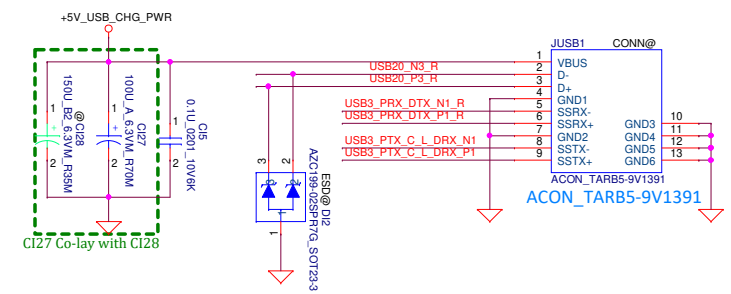
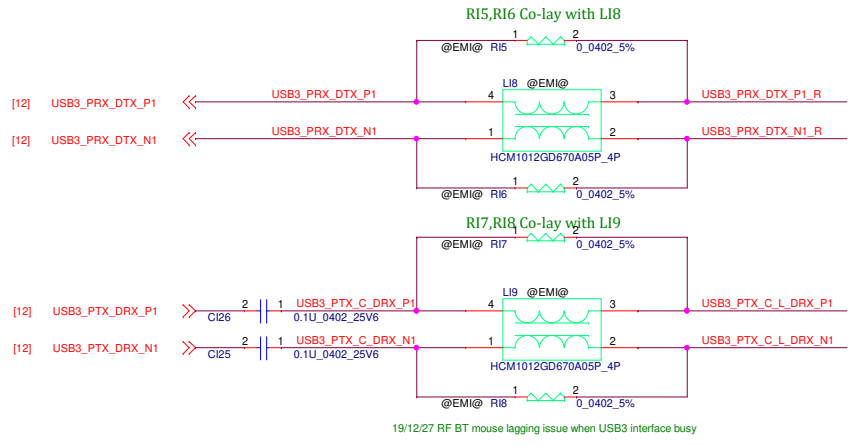
Card Reader RTS5242

LA-K491P

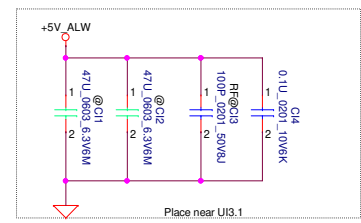
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MAIN: SLGC55544CVTR

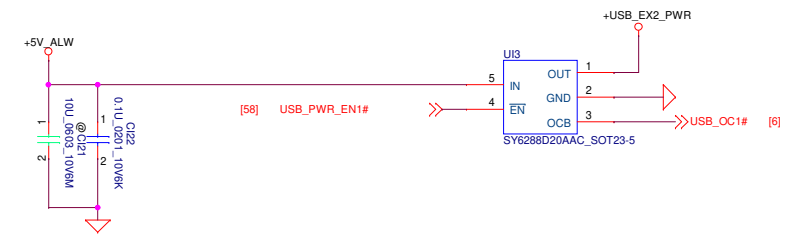
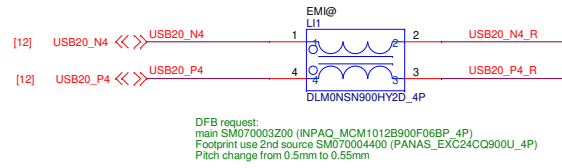
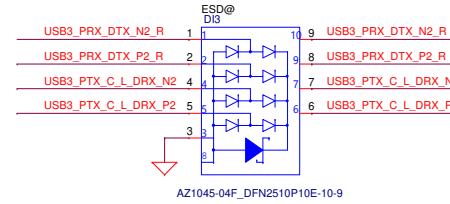
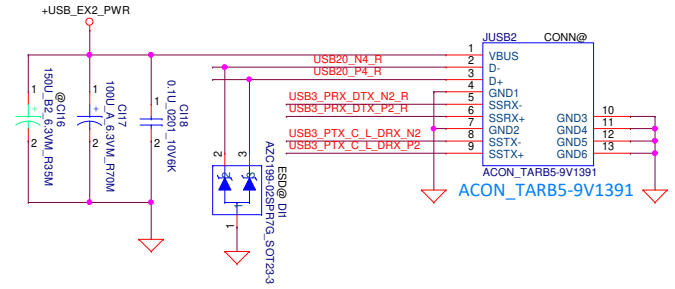
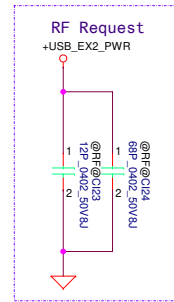
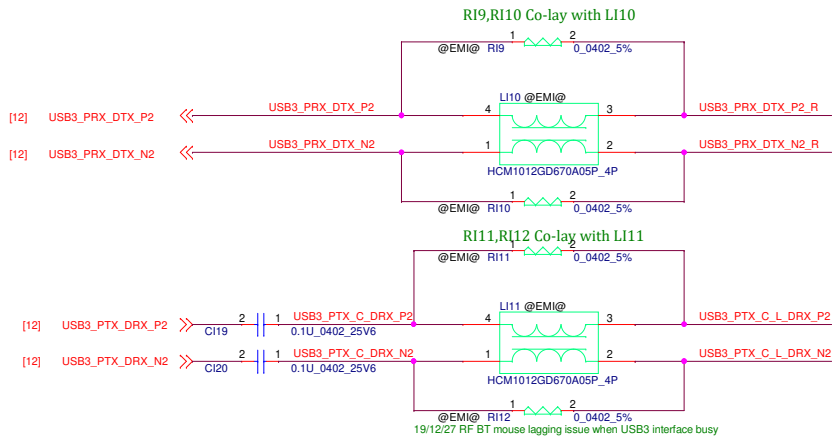


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Title		JUSB1+PS	
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Title: **JUSB2**

Size: Document Number **LA-K491P** Rev: 2.0

Date: Tuesday, December 08, 2020 Sheet 72 of 128

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Title		USB2/USB3 DB	
Size	Document Number	LA-K491P	Rev 2.0
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Reserve

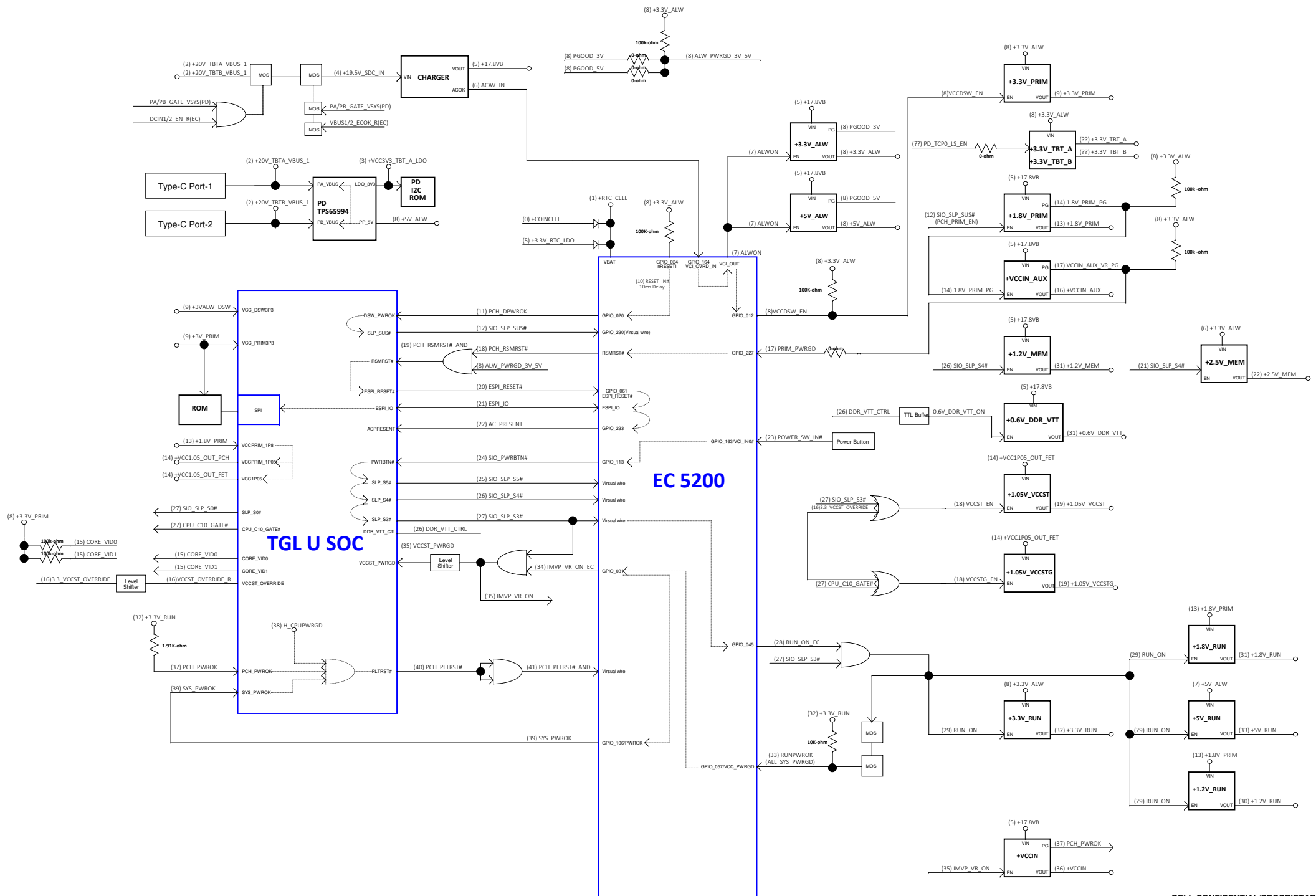
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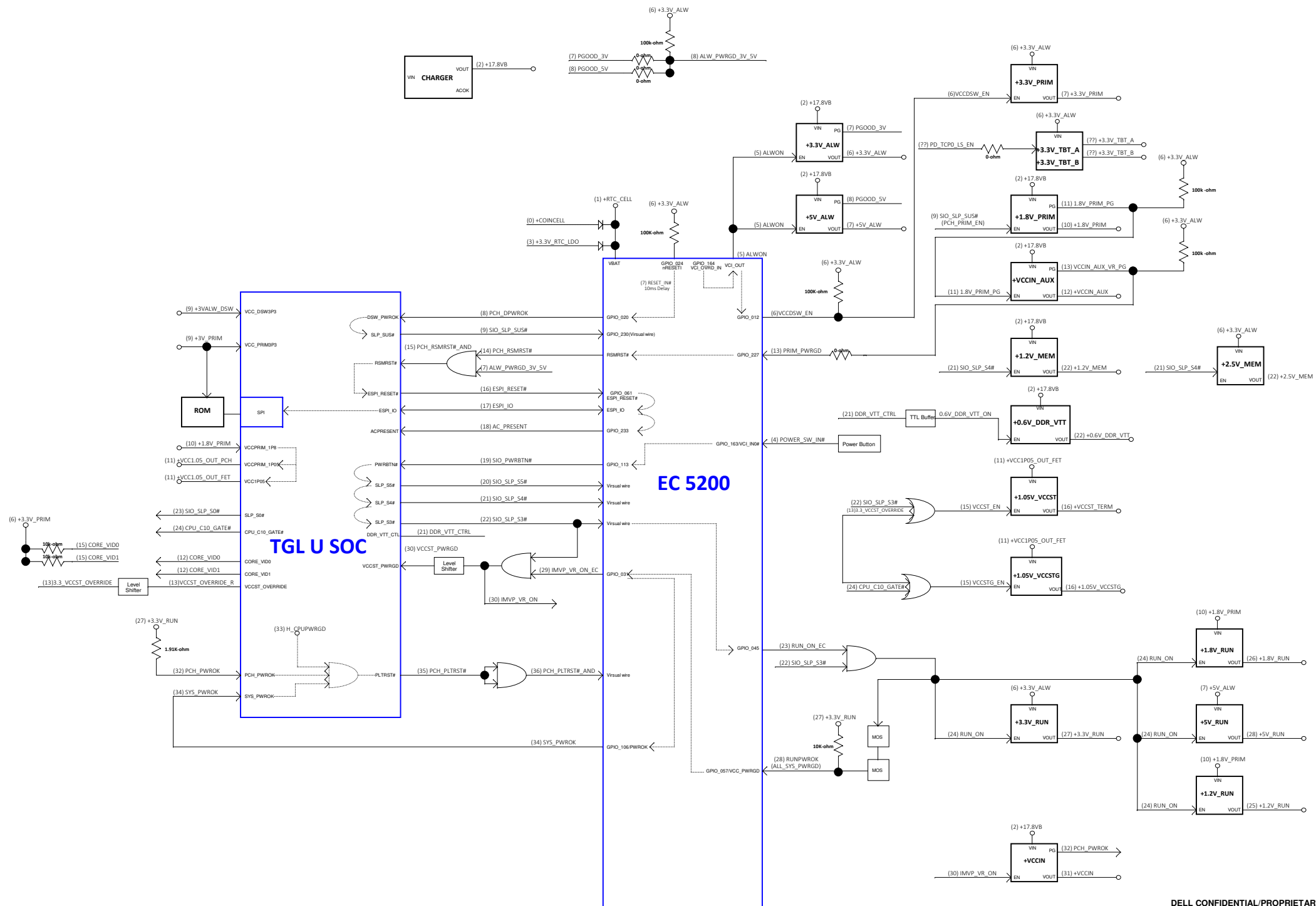
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Size	Document Number	Rev	2.0
Date: Tuesday, December 08, 2020		Sheet	74 of 128



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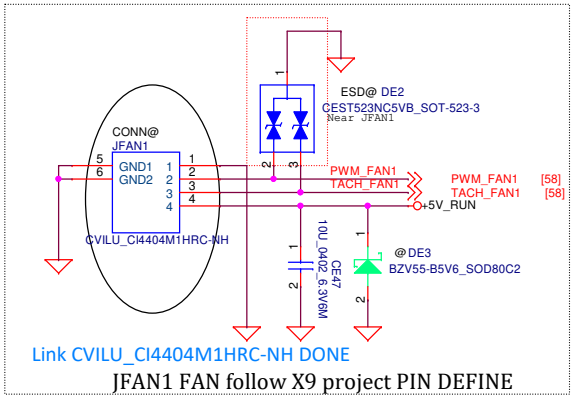
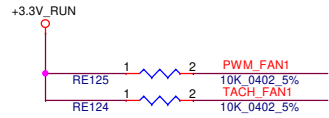
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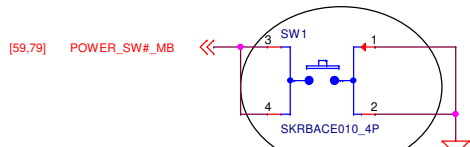
DC Power up Sequence

Document Number: **LA-K491P**

Rev: 1.0

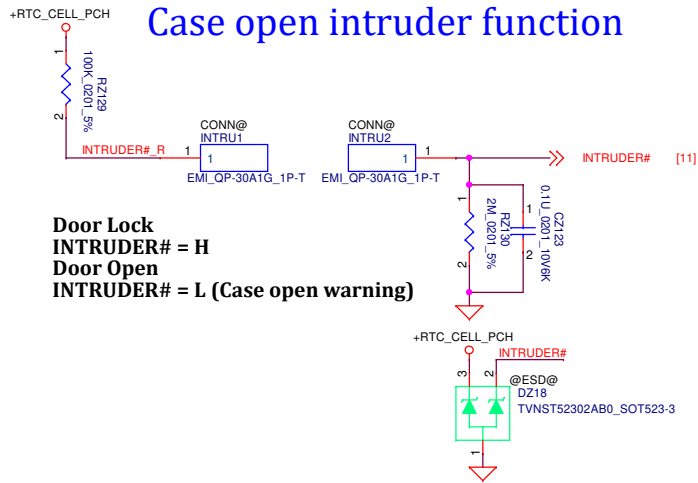


POWER & INSTANT ON SWITCH TOP



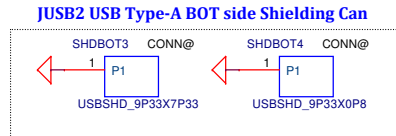
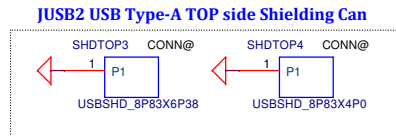
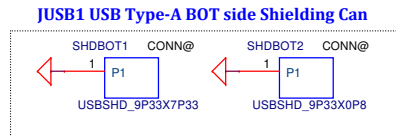
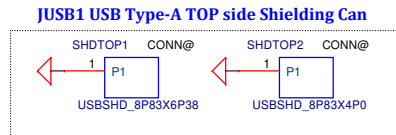
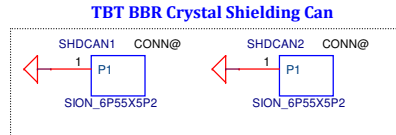
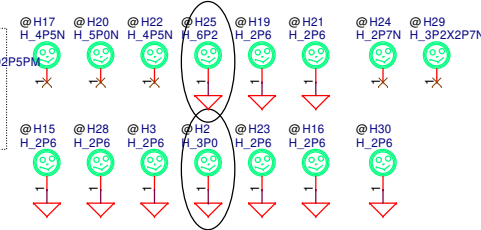
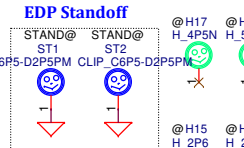
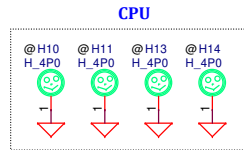
Link SW_SKRBACE010_4P DONE
Footprint: SW_NTC033-XK1G-X200T_4P

Case open intruder function



Fiducial Mark

- ⊗ FD1 FIDUCIAL MARK-D
- ⊗ FD2 FIDUCIAL MARK-D
- ⊗ FD4 FIDUCIAL MARK-D
- ⊗ FD3 FIDUCIAL MARK-D



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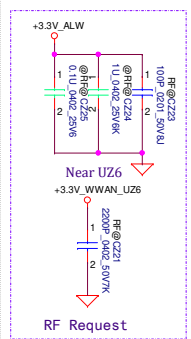
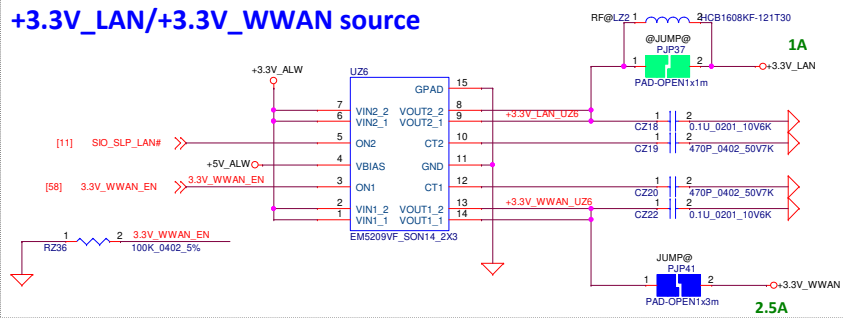
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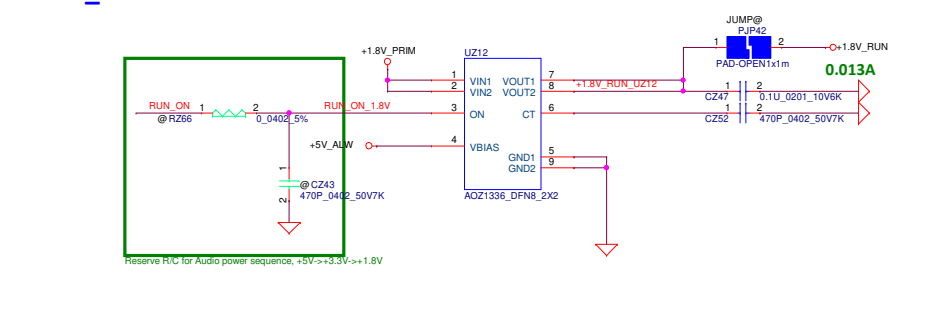
PWRBTN & PAD & ME & FAN

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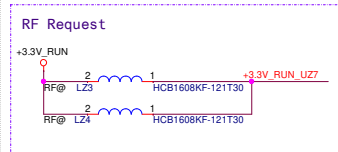
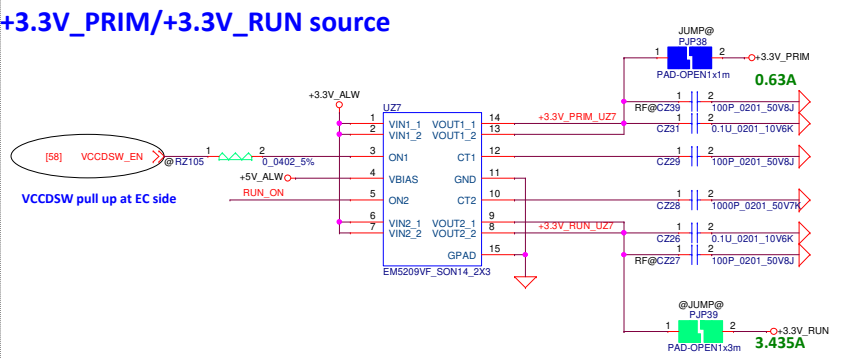
+3.3V_LAN/+3.3V_WWAN source



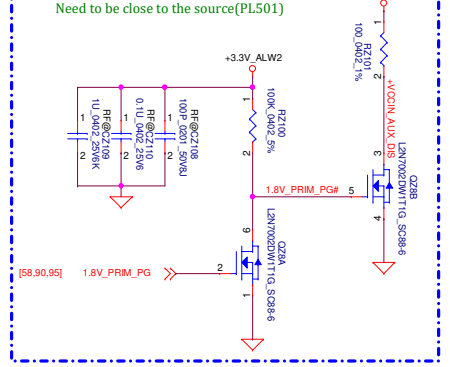
+1.8V_RUN source



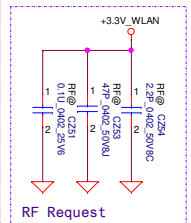
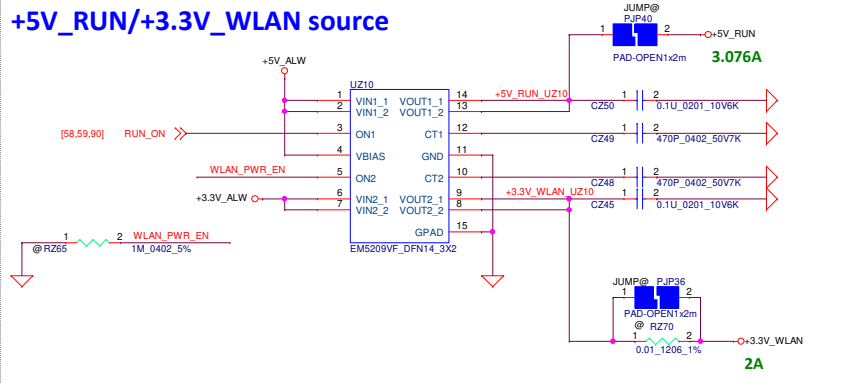
+3.3V_PRIM/+3.3V_RUN source



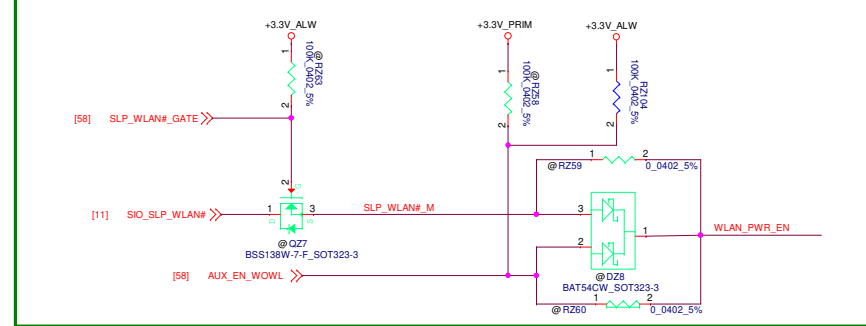
+VCCIN_AUX discharge circuit



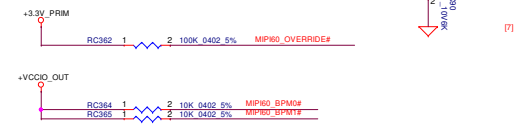
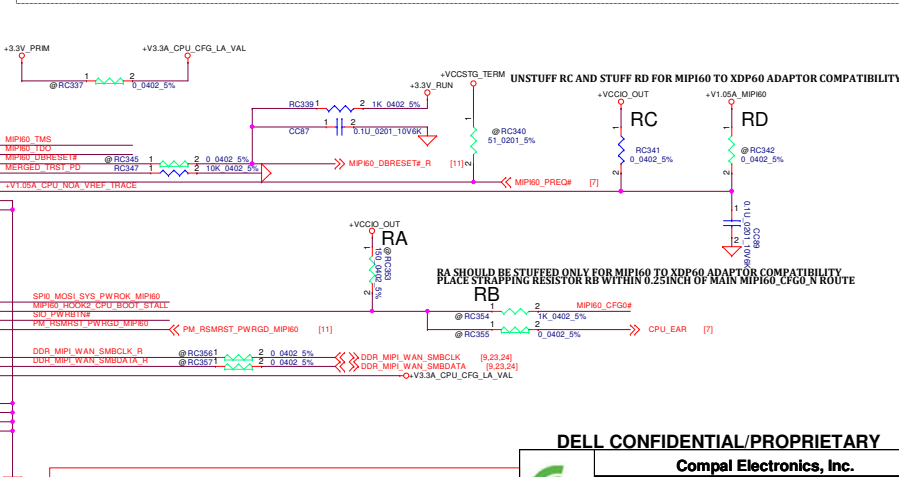
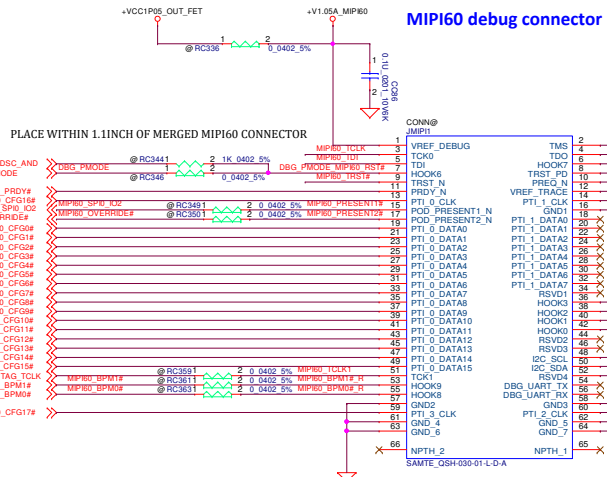
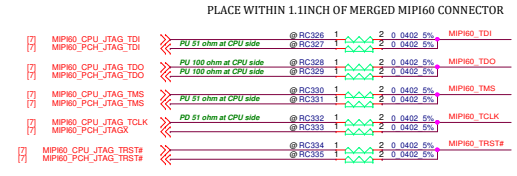
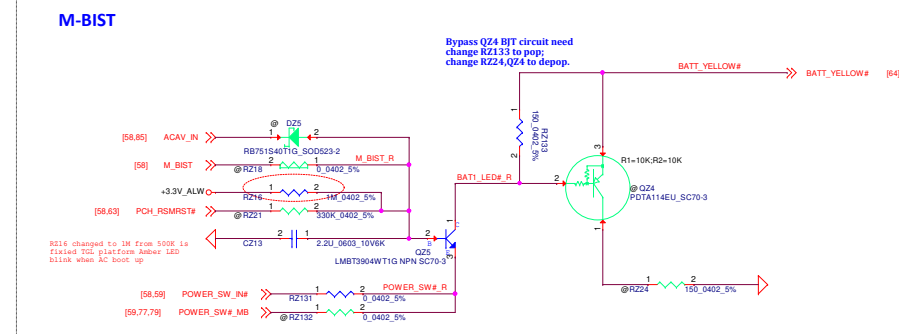
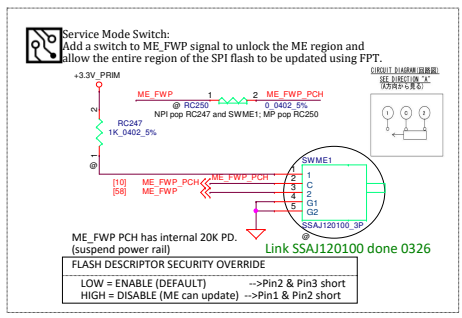
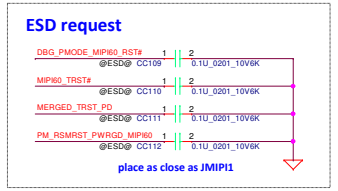
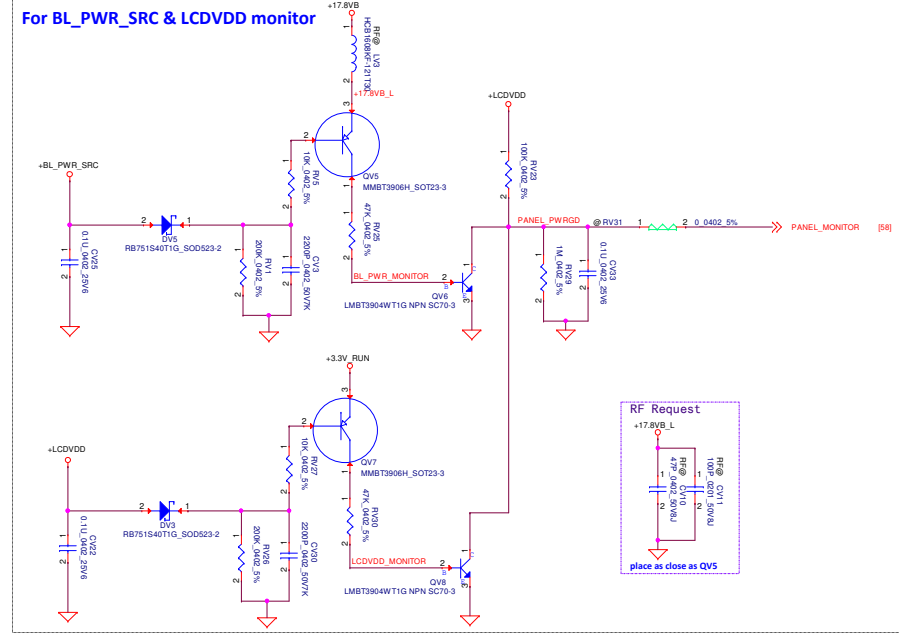
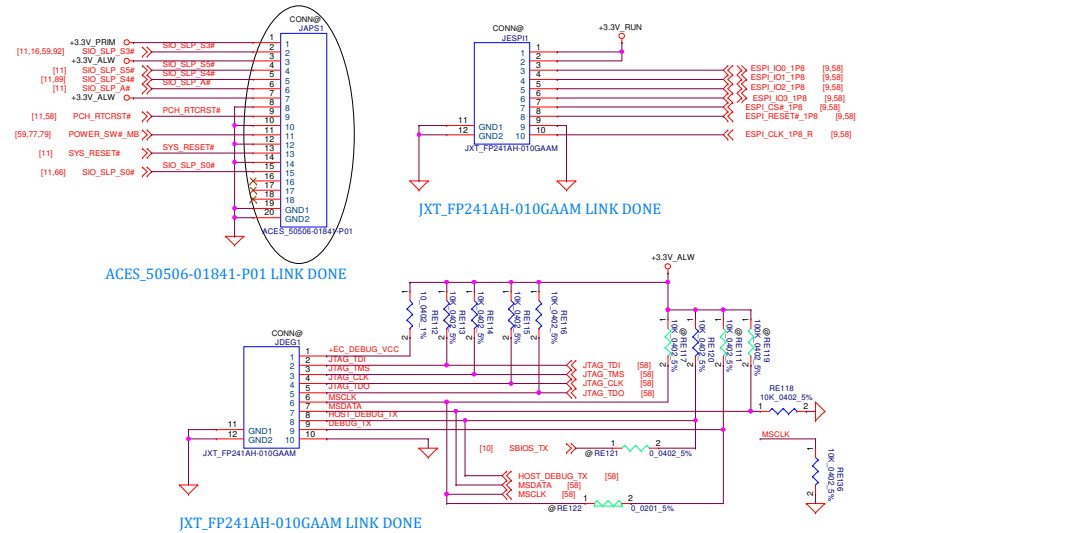
+5V_RUN/+3.3V_WLAN source



EC request to reserve OR gate for WLAN power enable



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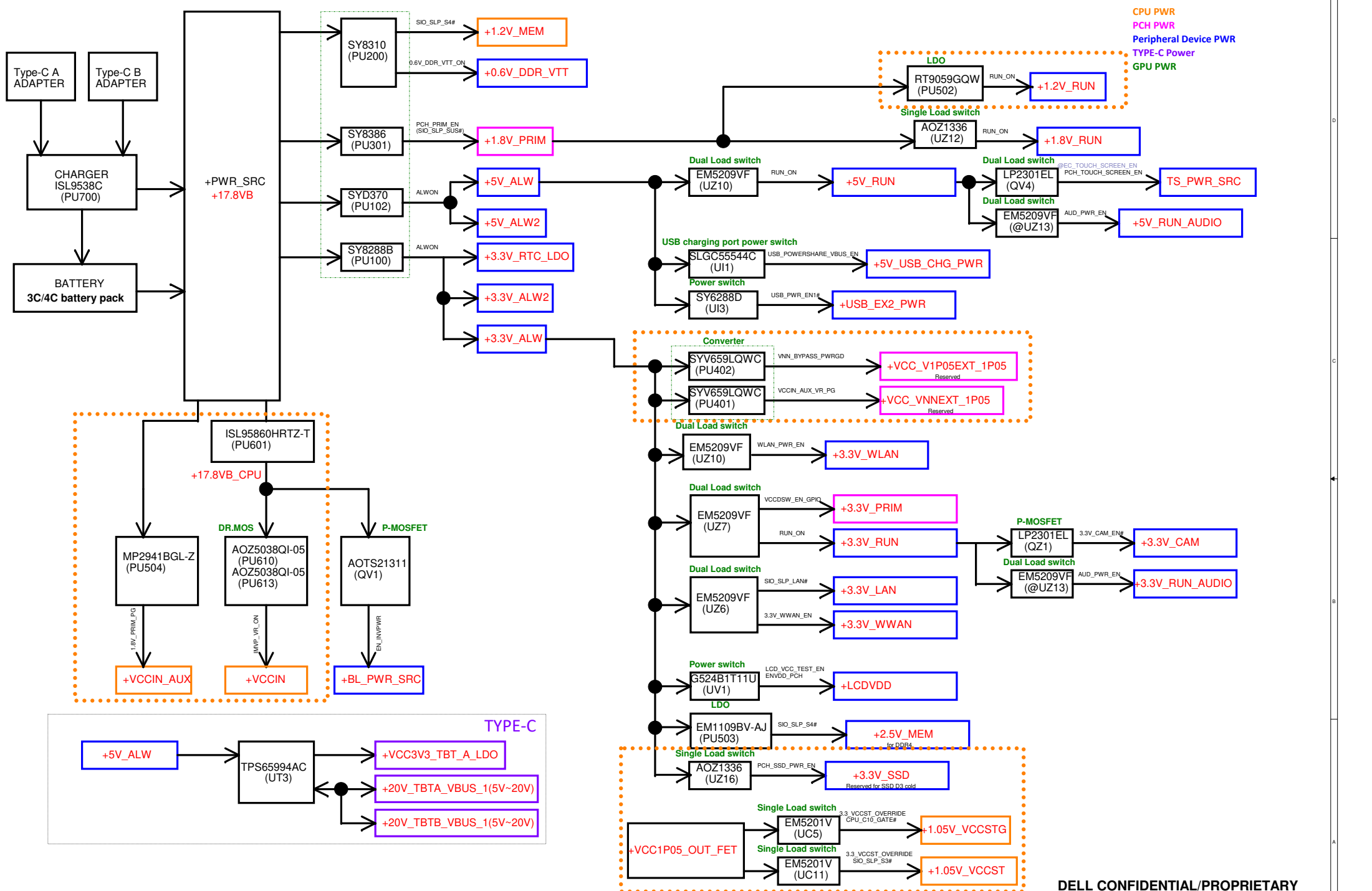
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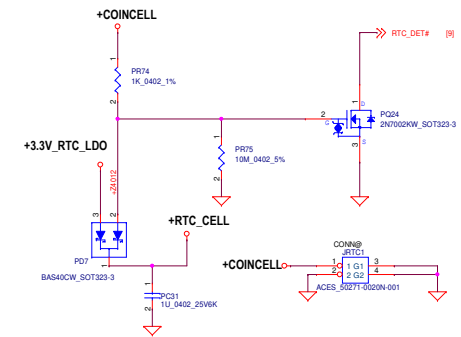
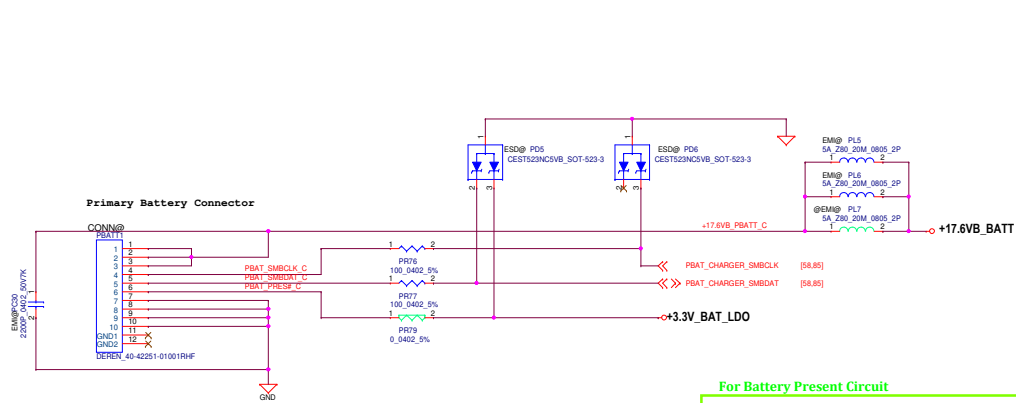
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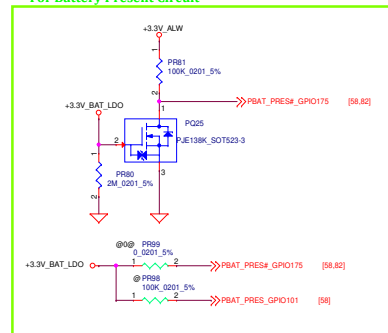
Power rails

LA-K491P

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For Battery Present Circuit

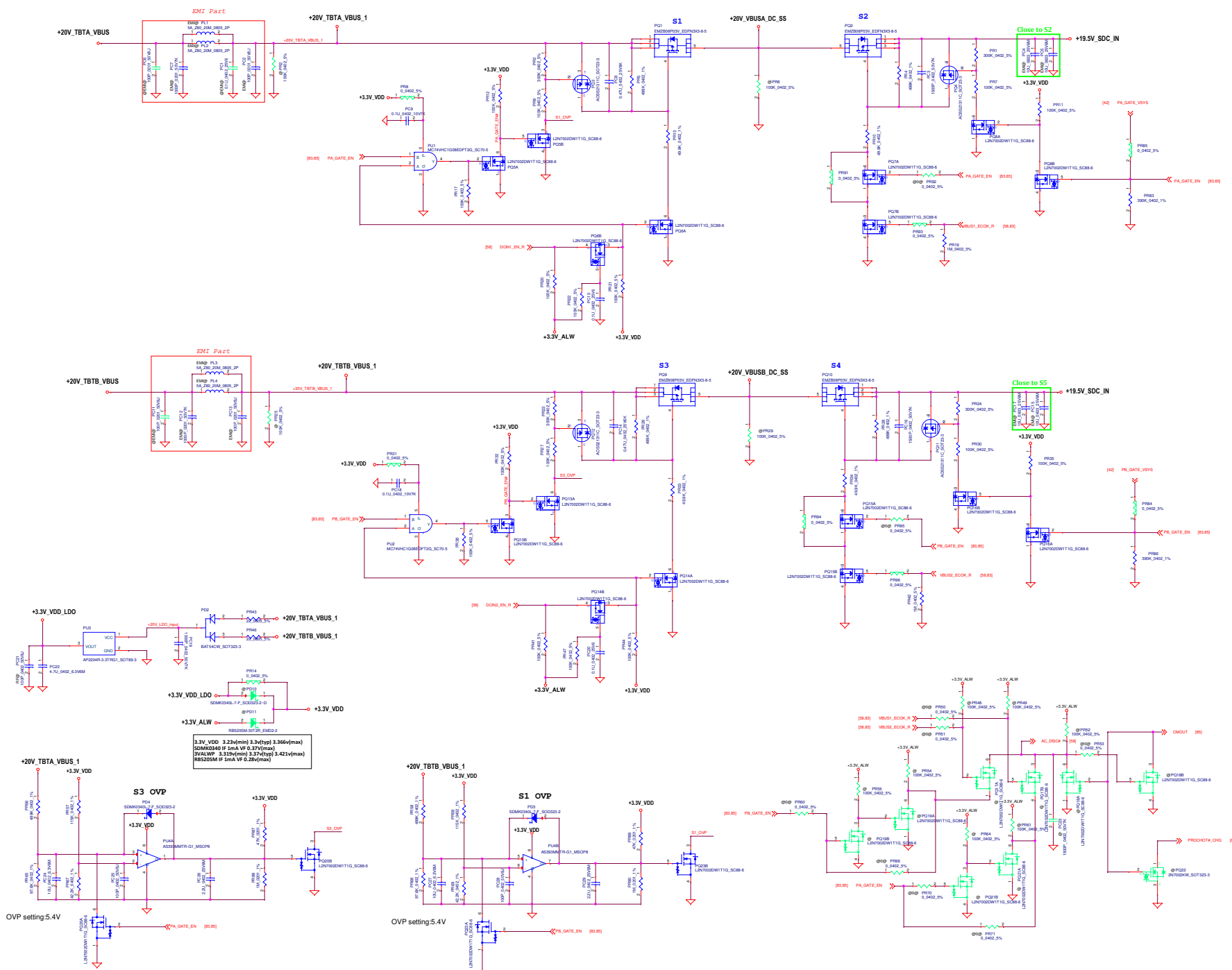


Location	Value	X11 battery (Battery PRES# internal pull down)	X12 battery (Battery PRES# internal LDO) Low voltage action
PR81	100K	V	V
PQ25	PJE138K		V
PR80	2M	V	V
PR99	100	V	

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		Battery Connector/ RTC	
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3.3V_VDD 3.23v(min) 3.3v(typ) 3.366v(max)
 S0M02020 IF 1mA VF 0.37V(max)
 3VALWP 3.315v(min) 3.37v(typ) 3.421v(max)
 RES255M IF 3mA VF 0.28v(max)

OVP setting:5.4V

OVP setting:5.4V

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


Compal Electronics, Inc.
 2TypeC PD Selector
 1A-K-01P

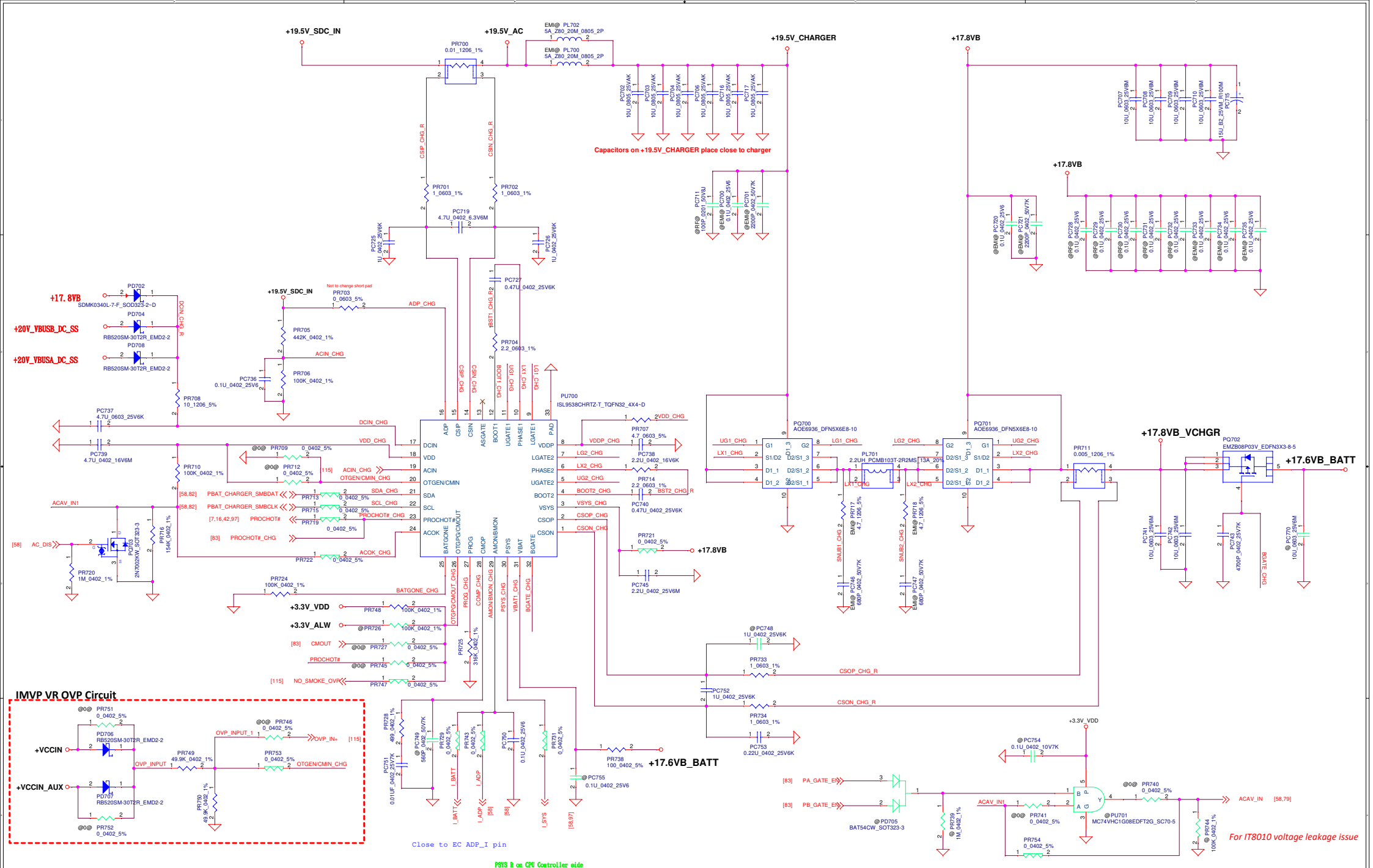
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Compal Electronics, Inc.

Charger


LA-K491P

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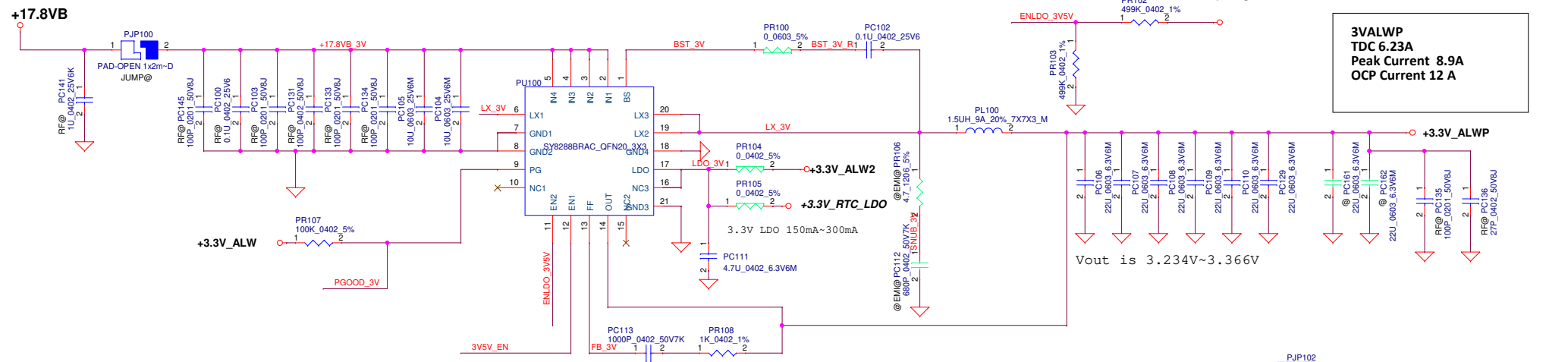
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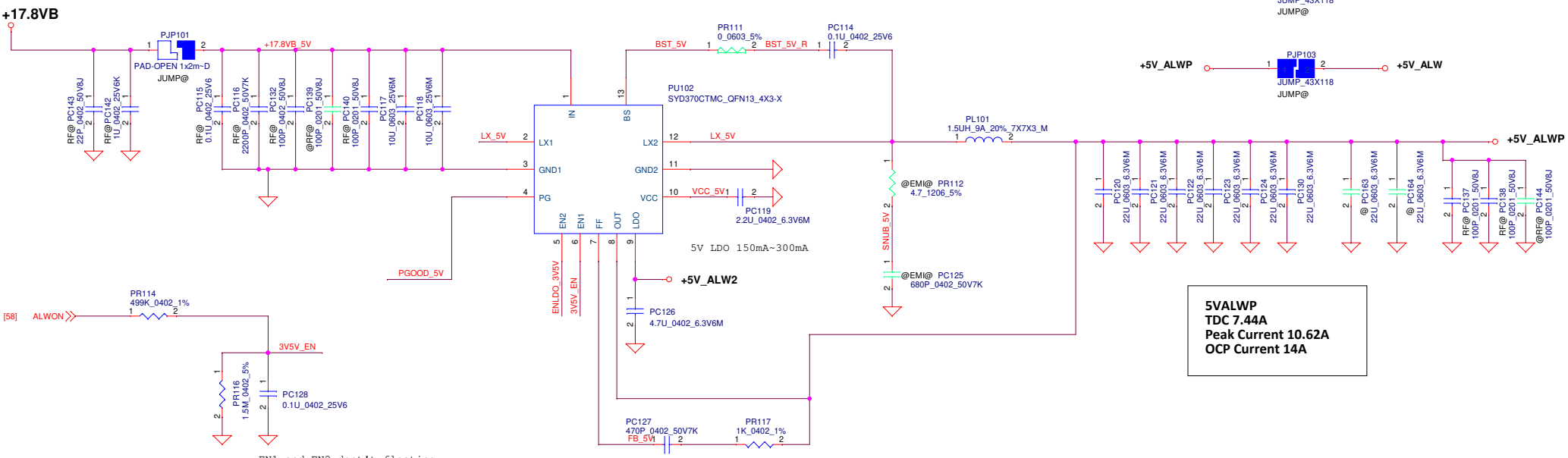
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3VALWP
 TDC 6.23A
 Peak Current 8.9A
 OCP Current 12 A



5VALWP
 TDC 7.44A
 Peak Current 10.62A
 OCP Current 14A

EN1 and EN2 dont't floating


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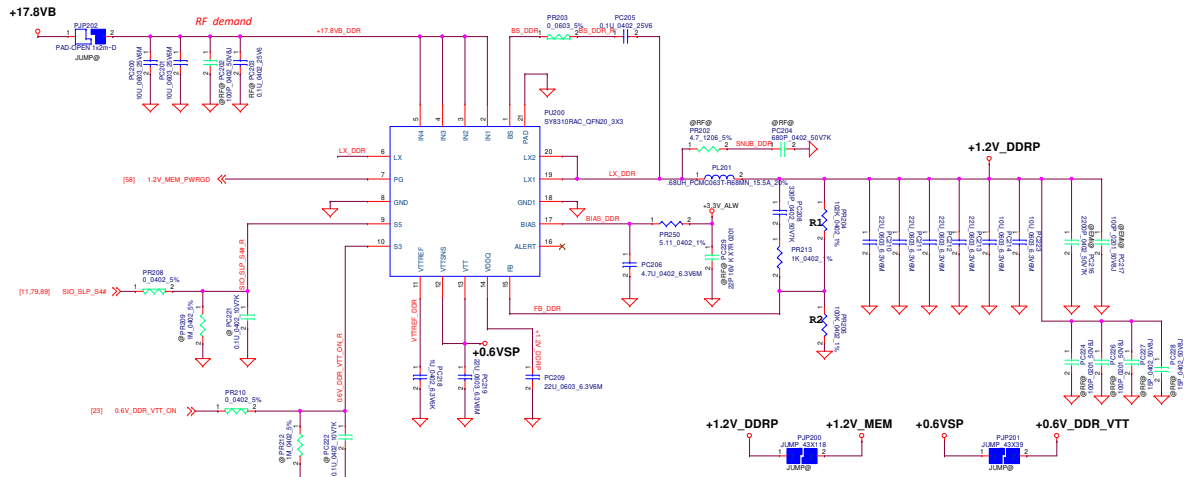
Compal Electronics, Inc.		
+5V ALW/3.3V ALW		
Title		
Size	Document Number	Rev
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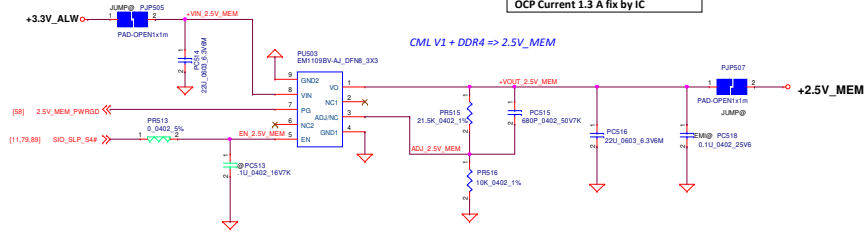
Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Standby	L	H	off	off
Shutdown	L	L	off	off

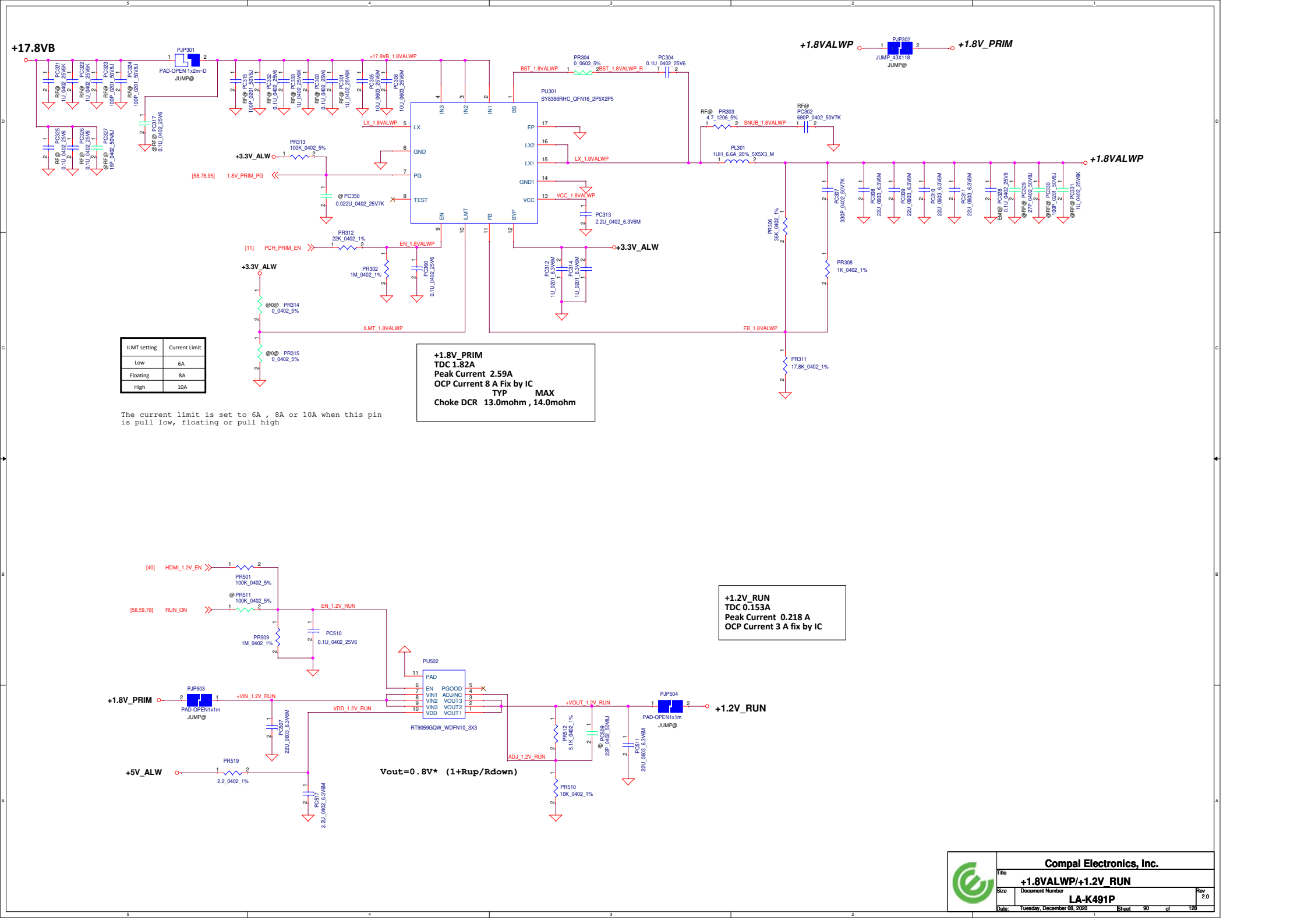
Note: S3 - sleep ; S5 - power off

+1.2V_DDR
 TDC 5.62A
 Peak Current 8.03A
 OCP Current 16A Fix by IC

0.6VSP +/- 5%
 TDC 0.42A
 Peak Current 0.6A
 OCP Current 2A (fix)

2.5V_MEM
 TDC 0.645A by power budget
 EMI1109BV-AJ Pd limit=1.7W
 Peak loading=0.921A
 $Pd=(3.3-2.5) \times 0.921 = 0.7368W < 1.7W$
 OCP Current 1.3 A fix by IC





ILMT setting	Current Limit
Low	6A
Floating	8A
High	10A

The current limit is set to 6A , 8A or 10A when this pin is pull low, floating or pull high


+1.8V PRIM
TDC 1.82A
Peak Current 2.59A
OCP Current 8 A Fix by IC
TYP MAX
Choke DCR 13.0mohm , 14.0mohm

+1.2V RUN
TDC 0.153A
Peak Current 0.218 A
OCP Current 3 A fix by IC

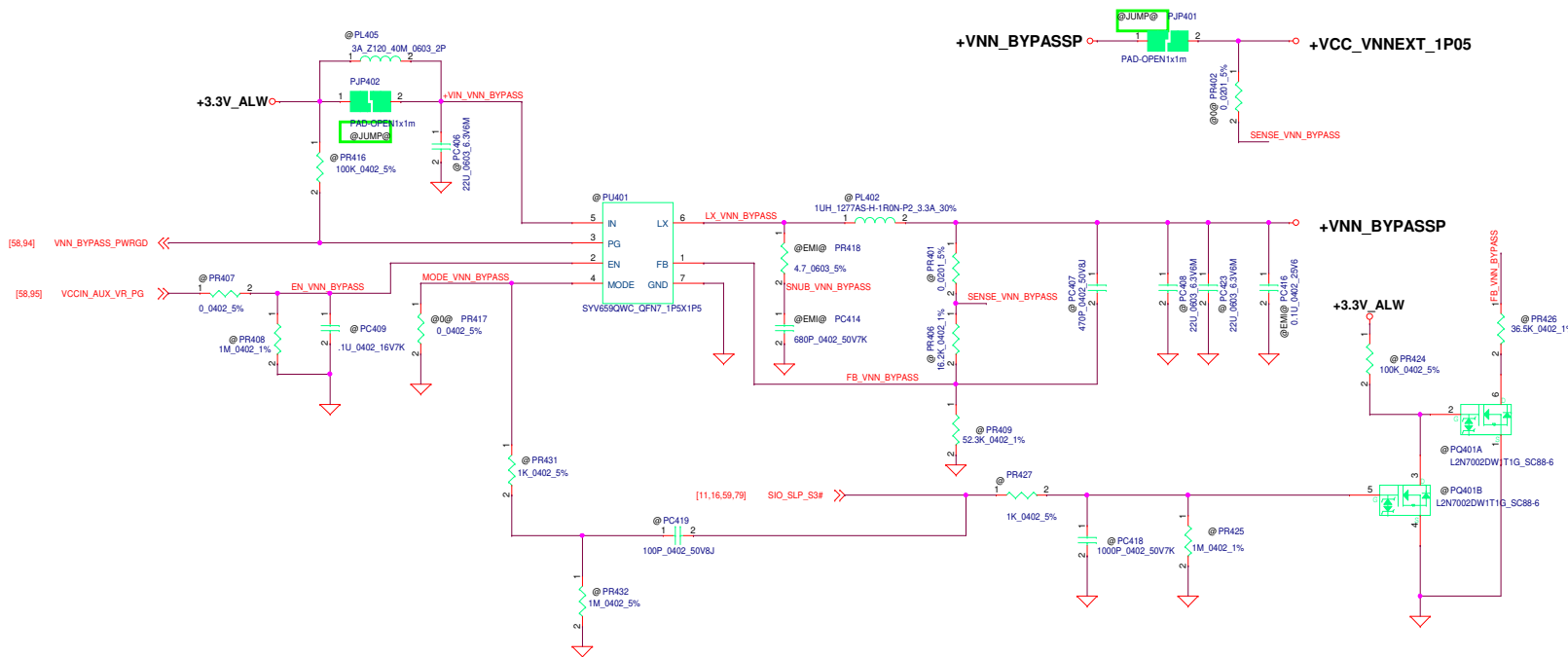
$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

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+VNN_BYPASS
 TDC 0.2A
 Peak Current 0.2A
 OCP Current 3 A


+VNN_BYPASS VR Voltage Configurations
 Follow Intel TGL PDG Rev0.9

SLP_S3# State	Output Voltage
Low	1.05
High	0.78

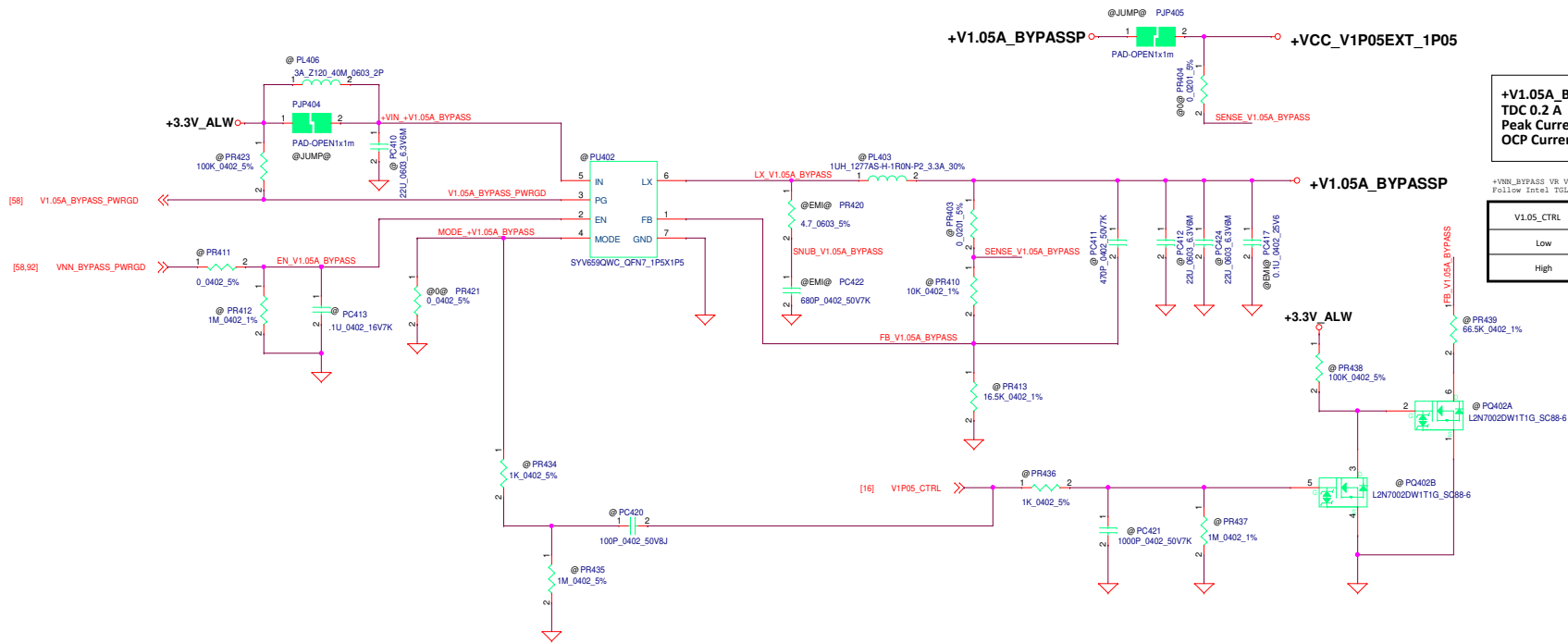
VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two dedicated voltage regulators that save platform power during low power states (Sx/S0ix). Both VCC_V1P05EXT_1P05 and VCC_VNNEXT_1P05 are VIDed rails that operate at two voltage levels each. The VID control for this VR is the SLP_S3# signal.

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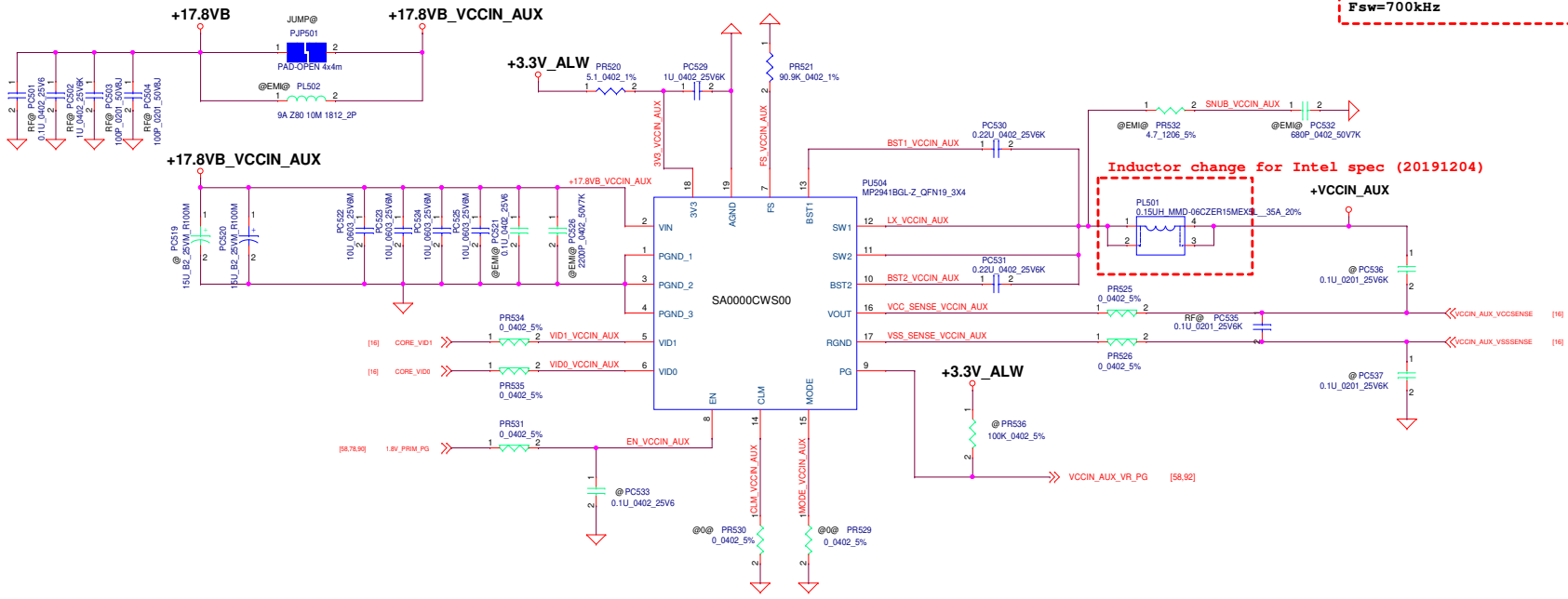
+V1.05A_BYPASS
 TDC 0.2 A
 Peak Current 0.2A
 OCP Current 3 A

+VNN_BYPASS VR Voltage Configurations
 Follow Intel TGL PDD Rev0.9

V1.05_CTRL	Output Voltage
Low	1.05
High	0.96

VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two dedicated voltage regulators that save platform power during low power states (Sx/S0ix). Both VCC_V1P05EXT_1P05 and VCC_VNNEXT_1P05 are VIDed rails that operate at two voltage levels each. The VID control for this VR is the SLP_S3# signal.

+VCCIN_AUX
TDC :14A
Peak Current 27A (ICCmax)
DC Load line :NA
AC Load line :NA
Current limit :32A(min) by IC pin.14 setting (per phase)
Fsw=700kHz



Inductor change for Intel spec (20191204)

Table---1:VID control Bit logics

VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:F9 Select

State	Fs (kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

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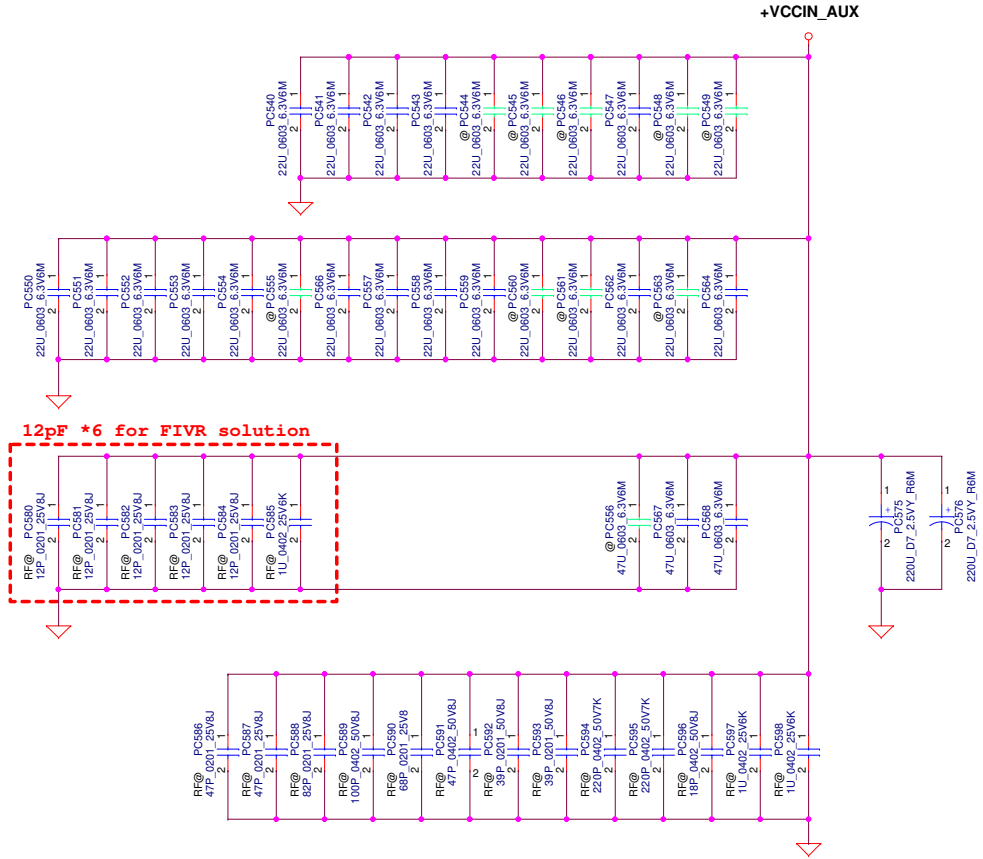
+VCCIN_AUX

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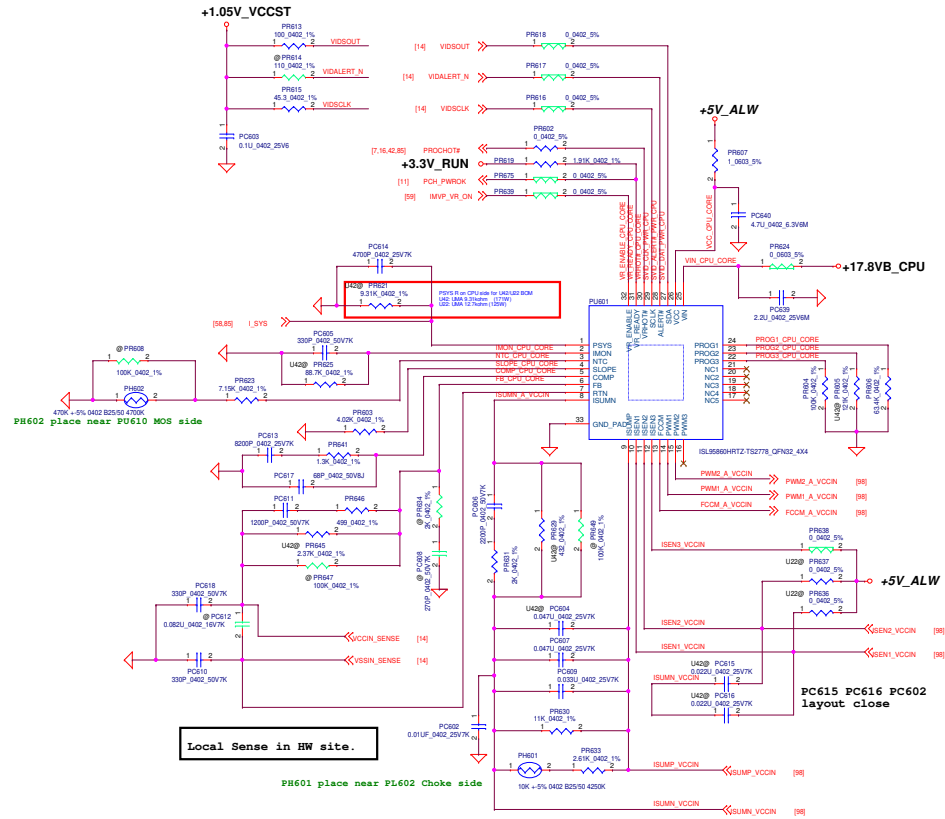


+VCCIN_AUX Output CAP :
 22U_0603 *16 pcs + reserved 9pcs
 47U *2 pcs + reserved 1 pcs
 220U_D7 *2pcs
 12pF *6 (for FIVR solution)

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			CPU Decoupling CAP	
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IMVP9-CPU CORE


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
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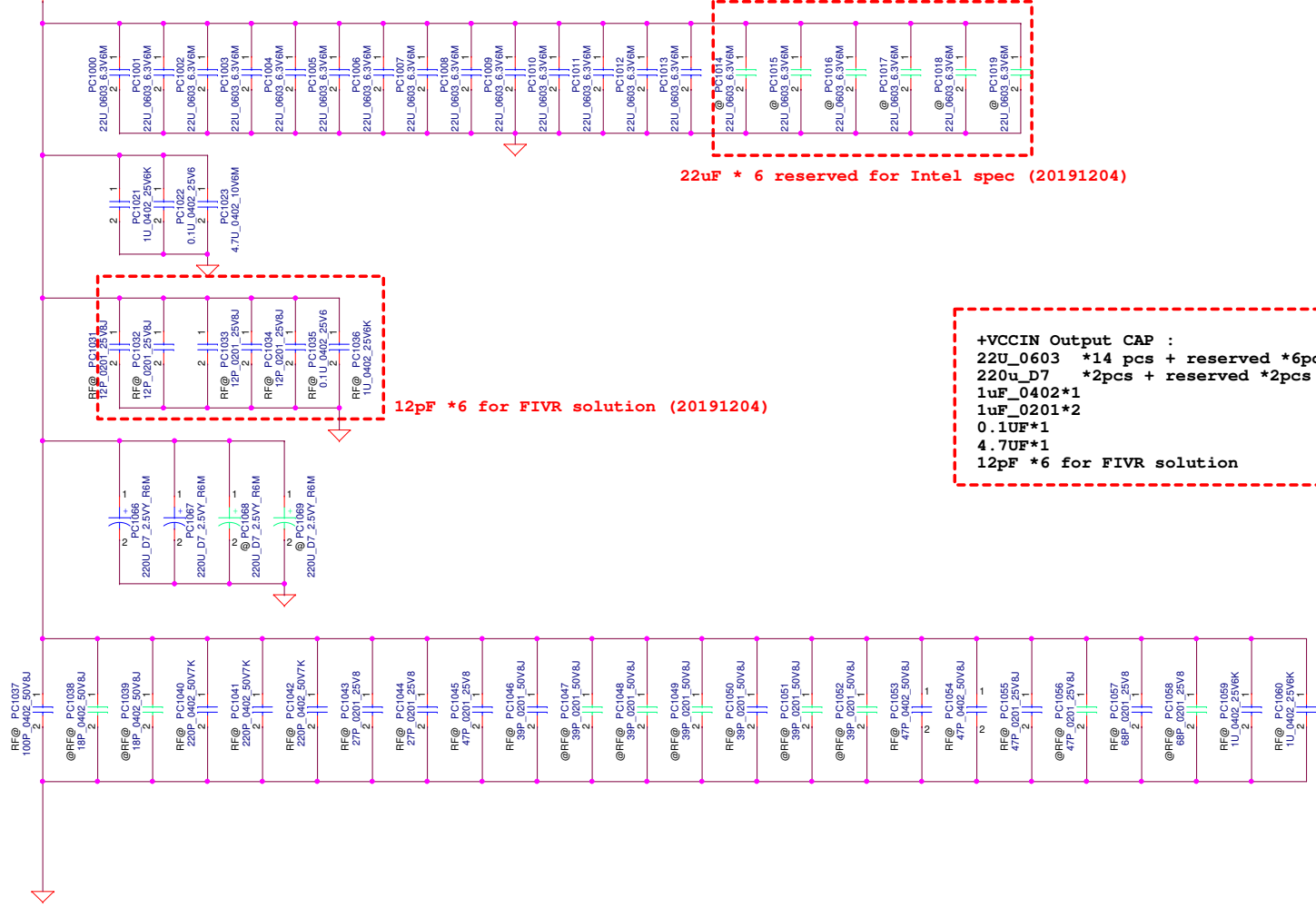
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+VCCIN



22uF * 6 reserved for Intel spec (20191204)

12pF * 6 for FIVR solution (20191204)

+VCCIN Output CAP :
 220u_0603 *14 pcs + reserved *6pcs
 220u_D7 *2pcs + reserved *2pcs
 1uF_0402*1
 1uF_0201*2
 0.1uF*1
 4.7uF*1
 12pF * 6 for FIVR solution

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
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
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
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
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
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
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
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
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
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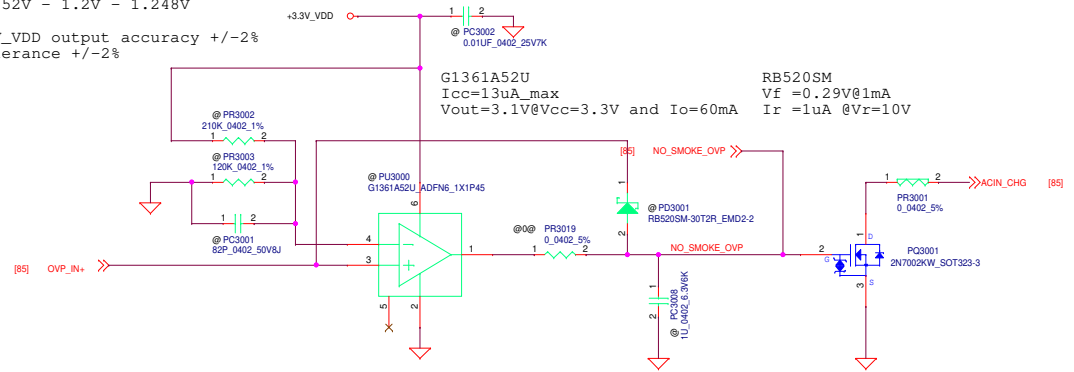
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
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$$V_f = 1.152V - 1.2V - 1.248V$$

1. +3.3V_VDD output accuracy +/-2%
2. R tolerance +/-2%




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
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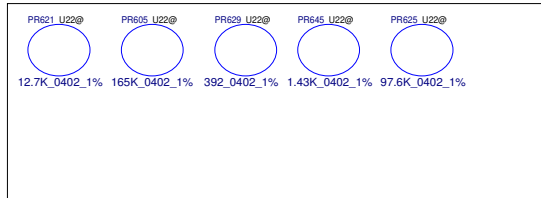
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
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U22



Location	U22	[1phase]	U42	[2phase]	U62	[2phase]
PR621	V	12.7K	V	9.31K	V	9.31K
PR605	V	165K	V	121K	V	121K
PR629	V	392	V	432	V	432
PR645	V	1.43K	V	2.37K	V	2.37K
PR625	V	97.6K	V	88.7K	V	88.7K

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1	P.83	5/13	B2B change to Gen11 solution	1. PC3, PC16 change to pop	X01
2	P.87	5/13	5V IC footprint	1. 5V IC footprint name change to "SYD370CTMC_QFN13_3X4-X"	X01
3	P.98	6/10	EMI request	1. PJP601 change to depop 2. PL601 change to pop	X01
4	P.90 P.95 P.96 P.98 P.101	6/10	RF request	1. PC315, PC501, PC502, PC503, PC504, PC659 change to pop and PC502 change from 18P_0402_50V6 to 1U_0402_25V6K. 2. Add PC332 (0.1U_0402_25V6), PC333 (1U_0402_25V6K) for RF request 3. PC660 change to pop and value change to from 2200P to 220P. 4. Add 13 pcs RF MLCC on +VCCIN_AUX output PC586, PC587 (56P_0201_25V8) PC588 (82P_0201_25V8J) PC589 (100P_0402_50V8J) PC590 (68P_0201_25V8) PC591 (47P_0402_50V8J) PC592, PC593 (39P_0201_50V8J) PC594, PC595 (220P_0402_50V7K) PC596 (18P_0402_50V8J) PC597, PC598 (1U_0402_25V6K) 5. Add 24 pcs RF MLCC on +VCCIN output PC1037 (100P_0402_50V8J) PC1038, PC1039 (18P_0402_50V8J) PC1040, PC1041, PC1042 (220P_0402_50V7K) PC1043, PC1044 (27P_0201_25V8) PC1045 (56P_0201_25V8) PC1046, PC1047, PC1048, PC1049, PC1050, PC1051, PC1052 (39P_0201_50V8J) PC1053, PC1054 (47P_0402_50V8J) PC1055, PC1056 (47P_0201_25V8J) PC1057, PC1058 (68P_0201_25V8) PC1059, PC1060 (1U_0402_25V6K) 6. PC649, PC659, PC660 change to pop	X01
5	P.96	6/10	CPU output decoupling CAP	1. PC556 and PC566 location exchange 2. PC544, PC545, PC546, PC548, PC549, PC555, PC556, PC560, PC561, PC563 change to depop 3. PC576 change to pop	X01
6	P.97	6/10	R/C Tune Value for Intel Validation	For U42 1. PR629 change to 432_0402_1% 2. PC608, PR634, PR649 change to depop 3. PC604 change to 0.047U_0402_25V7K For U22 PC608, PR634 change to depop	X01

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Item	Page#	Date	Issue Description	Solution Description	Rev.
7	P.83	7/22	Un-stuff external PROCHOT# circuit for DTC item	1. Depop PR53, PR54, PR55, PR61, PR64, PQ17, PQ19, PQ21	X02
8	P.115	7/22	Un-stuff external OVP circuit for DTC item	1. Depop PC3002, PR3002, PR3003, PU3000, PD3001	X02
9	P.95 P.98	7/22	Add " -NPM " PCB Footprint to cover green paint for Co-lay depop component	1. PJP601 PCB footprint change from JUMP_43X118 to JUMP_43X118-NPM 2. PL502 PCB footprint change from 9A_Z80_1812_2P to 9A_Z80_1812_2P-NPM	X02
10	All	7/22	0 ohm change to short pad	TGL 0 ohm change to short-PAD : 40 pcs PR8,PR31,PR79,PR91,PR93, PR94,PR96,PR100,PR111,PR104, PR105,PR119,PR120,PR203,PR208, PR210,PR304,PR513,PR525,PR526, PR531,PR534,PR535,PR616,PR617, PR618,PR638,PR639,PR675,PR686, PR687,PR692,PR693,PR624,PR682, PR683,PR713,PR715,PR721,PR722, PR729,PR731,PR743,PR3001	X02
11	P.85	7/30	Increase more margin for Vcore OVP circuit	1. PR749 change from 45.3K_0402_1% to 49.9K_0402_1%	X02
12	P.85	8/14	PD ROM remove charger DCIN_CHG voltage margin cause VBUS keep 5V potential risk	1. PD704 power source change to "+20V_VBUSB_DC_SS" 2. Add PD708 and power source come from "+20V_VBUSB_DC_SS"	X02
13	P.85	8/14	Un-stuff ACAV_IN function un-stuff for DTC item	1. Depop PD705 / PC754 / PU701	X02
14	P.95	8/30	+VCCIN_AUX sense noise from CPU remote sense issue solution	1. Add PC535 100nF_0201_25V	X02
15	P.95 P.98	8/30	Low noise MLCC change to Normal type for DTC item	AUX : PC522 / PC523 / PC524 / PC525 VCCIN : PC624 / PC625 / PC626 / PC627 / PC633 / PC634 / PC635 / PC636 Change from low noise to normal MLCC	X02
16	P.85 P.97	8/31	For PROCHOTcircuit voltage level tuning	1. PR719, PR602 change from 100_0402 to 0_0402_5%	X02
17	P.92 P.94	9/1	+VNN_BYPASS OVP solution (Premium)	1. PU401 / PU402 CPN change from SYV659LQWC to SYV659QWC	X02
18	P.96 P.101	8/31	RF request	1. PC580, change to 1.0uF/0201 2. PC581,PC1031 change to 0.1uF/0201 3. PC582,PC1032 change to 100pF/0201 4. PC585, PC1036 change to 1.0uF/0402 5. PC1035 change to 0.1uF/0402 6. PC1051,PC1052,PC1047 change to depop	X02

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Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.
19	All	10/14	0 ohm change to short pad	TGL 0 ohm change to short-PAD : 11pcs PR208,PR210,PR513,PR531,PR14, PR84,PR85,PR719,PR747,PR754, PR753.	A00
20	P.97	10/20	PU601 CPN to L-end CPN for MP	1. PU601 CPN to L-end (SA0000ASX0L) CPN for MP	A00
21	P.98	10/20	Dr.MOS change to AOZ5038QI-05 for MP	1. PU610, PU613 CPN change to AOZ5038QI-05.	A00
22	P.92 P.94	10/27	VNN_BYPASS & V1.05A_BYPASS power rail change to volume design for Gen12 DTC item	+VNN_BYPASS De-pop PR432,PR416,PR407,PR401,PR425,PL402,PR431,PR408,PR427,PU401, PQ401,PR424,PC418,PC406,PC416,PC408,PR409,PR406,PC407,PR426,PC419 +V1.05A_BYPASS De-pop PL403,PR410,PC410,PR403,PR423,PR436,PR439,PC421,PR411,PR435, PC420,PQ402,PU402,PR434,PR438,PC411,PR412,PC412,PR413,PC417,PR437	A00
23	P.96 P.101	10/28	RF request MLCC optimized	1. PC1039,PC1038,PC1049,PC1048,PC1056,PC1058 all change to De-pop. 2. PC580,PC581,PC582,,PC1031,PC1032 all change to 12pF.	A00


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LAN Clarkville


NVPRO@UL1



WG1219V SLKJ4 A0 QFN
SA00009345L

TPM Chip


NU@ UZ4



NPCT750JADYX
SA0000AQ2C0


X76_TPM

STX76@ ZZZ



ALT. GROUP PARTS TPM TGL STMICRON GDF40
X7691431L01


NUX76@ ZZZ



ALT. GROUP PARTS TPM TGL NUVOTON GDF40
X7691431L02


EC Chip

5107ES@ UE1



MEC5107KD4LJTR_WFBGA176P-NH
SA0000CQ730

5107NES@ UE1



MEC5107KD4LJTR_WFBGA176P-NH
SA0000CQ740

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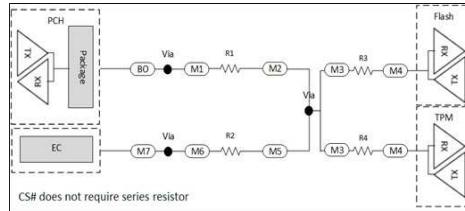
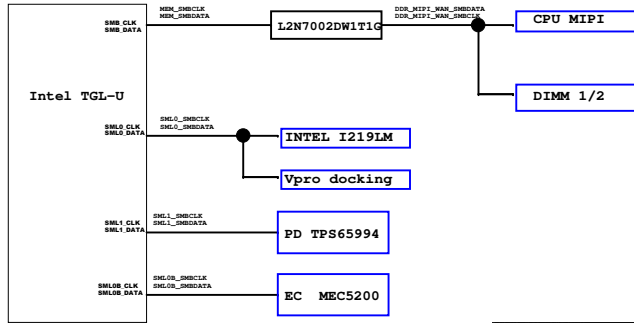
Bom option

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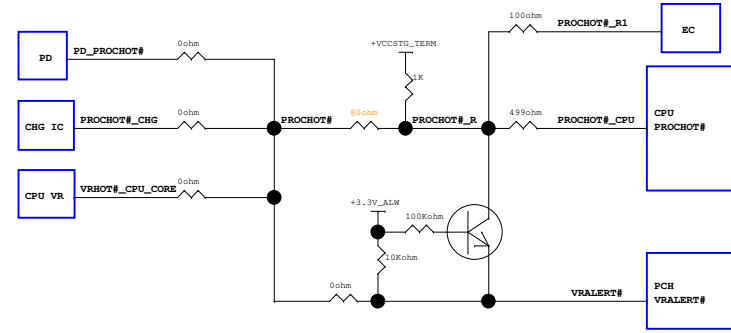
SMBUS Block Diagram



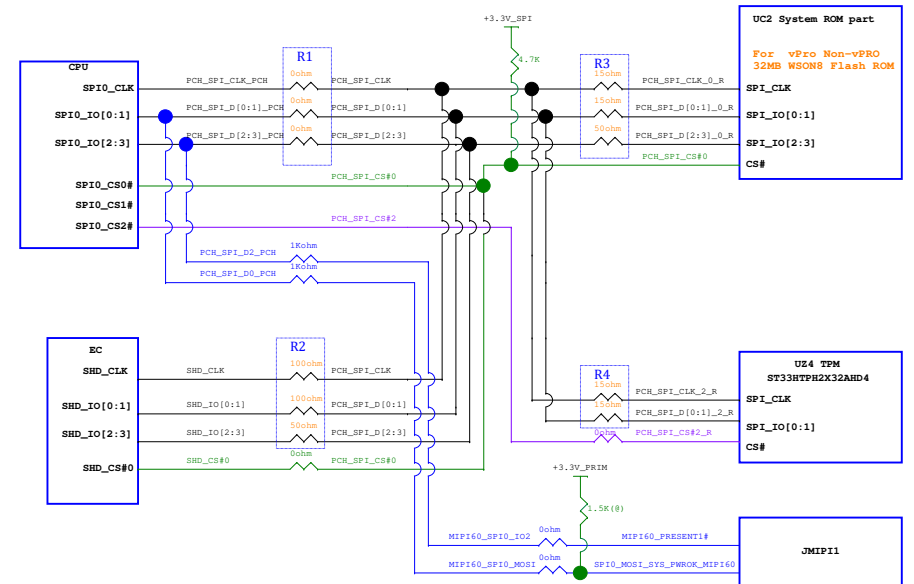
Segment	Time Type	Reference	Via Count	Max Length, Segment (mm)	Max Length, Total (mm)
B0/M7	MS/SL	VSS	1	12.7	165.1
M1/M6	MS/SL/DSL	VSS	1	76.2	
M2/M5	MS	VSS	0	25.4	
M3	MS	VSS	0	25.4	
M4	MS	VSS	0	25.4	
M4	MS	VSS	0	25.4	

Notes	Details
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
EC and PCH branch requirement	Delta between M1-M2 and M5-M6 shall not exceed 25.4mm (1 inch)
R1	100 ohm resistor for 1.8V and 100 ohm for 3.3V. To be placed on SPIO_CLK, SPIO_MISO, SPIO_MOSI, SPIO_IO_2 and SPIO_IO_3
R2	50 ohm for 1.8V and 50 ohm for 3.3V. To be placed on SPIO_CLK, SPIO_MISO and SPIO_MOSI
R3	50 ohm for 1.8V and 50 ohm for 3.3V. To be placed on SPIO_CLK, SPIO_MISO and SPIO_MOSI
R4	50 ohm for 1.8V and 50 ohm for 3.3V. To be placed on SPIO_CLK, SPIO_MISO and SPIO_MOSI
Minimum length	M1, M3, M4 and M6: 12.7mm M2 and M5: 2.54mm
M3 + M4	8X branches of segment M3-M4 need to have length matching of 2.54mm
Length matching between CLK and DATA/CS#	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPIO_CLK SPIO_MOSI_IO_0 SPIO_MISO_IO_1 SPIO_IO_3 SPIO_IO_2 SPIO_FLASH_IO11_CS# SPIO_TPM_CS#

PROCHOT# Topology

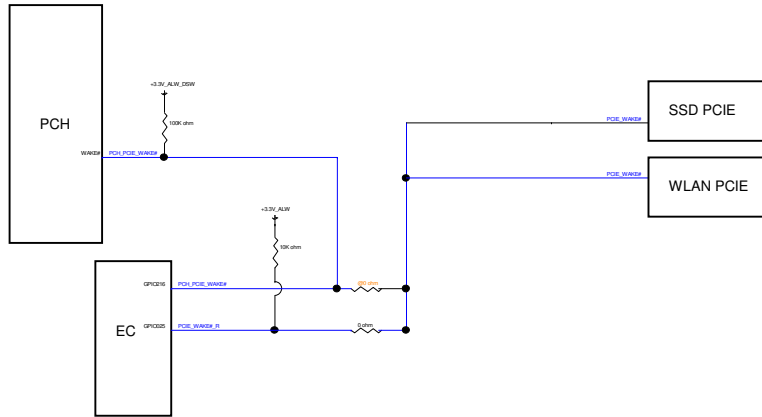


EC G3 SPI Flash Sharing with Wire-OR Non-Vpro / Vpro Topology

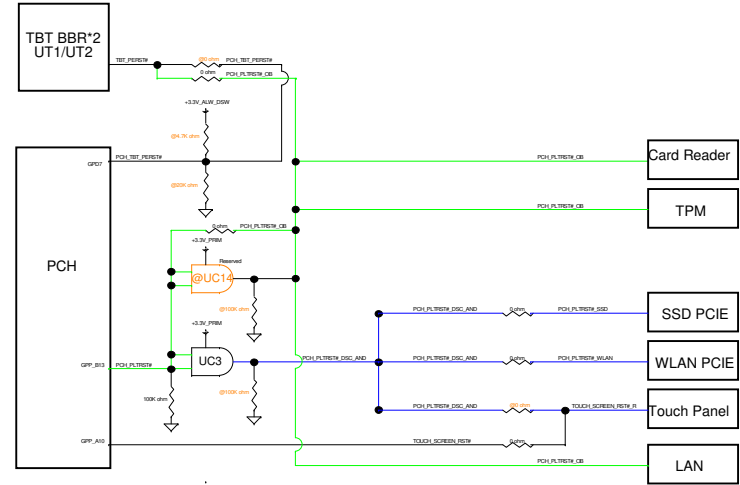


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PCH_PCIE_WAKE# Topology



PCH_PLTRST# Topology



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Other Topology-2

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Version Change List (P. I. R. List)					
Item	Page#	Date	Issue Description	Solution Description	Rev.
1	P.59	6/8	Enter DVT1.0 phase	1. Change location RE25 part to 130K_0402_1% from 240K_0402_1%	X01
2	P.58	6/8	EC needs to distinguish between TGL or CML platform.	1. Add net CPU_TGL_SELECT# on GPIO013 2. Add location RE139(BOM Structure CML@),RE140(BOM Structure TGL@) 100K_0402_5%	X01
3	P.42	6/8	Modified according to ARD define	1. Change location UT3 part to SN1908005 from PTPS65994 2. Change location UT5 to SN10224RUKR from TS3DS10224	X01
4	P.42	6/8	Modified according to ARD define	1. Change location UT11 to depop from pop	X01
8	P.123	6/8	Implement Nuvoton TPM chip to try run on 2nd / 3rd sku	1. Add BOM option location UZ4 SA0000AQ2C0(BOM Structure NU@)	X01
9	P.40	6/10	Modified according to HDMI 2.0 EA test result	1. Change EMI location LV6 to pop from depop 2. Change EMI location RV35,RV36 to depop from pop	X01
5	P.58	6/10	Boot Source Select strap pin define difference on 5170 and 5200 chip	1. Change location RE23 pull up 10K_0402_5% BOM Structure to 5107@ 2. Change location RE22 pull down 100K_0402_5% BOM Structure to 5200@	X01
6	P.64	6/10	Modified according to the brightness test result of FPR LED	1. Change location RZ141,RZ142,RZ143,RZ144 part to 4.99K_0402_1% from 1K_0402_5%	X01
7	P.52	6/15	Modified according to WWAN FIBCOM vendor review feedback	1. Change location CZ111 part to 220U_B2_6.3VM_R35M from 100U_B2_6.3VM_R35M 2. Delete location CZ32 part 22U_0402_6.3V6M 3. Change RF location CZ36 part to 6.8P_0402_50V8C from 100P_0402_50V8J 4. Change RF location CZ30 part to 33P_0402_50V8J from 100P_0402_50V8J 5. Change RF location CZ35 part to 39P_0402_50V8J from 100P_0402_50V8J	X01
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<p style="text-align: center;">EE P.I.R</p>					
<p style="text-align: center;">LA-K491P</p>					
<p style="text-align: center;">Date: Tuesday, December 08, 2020 Sheet 126 of 128</p>					

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Item	Page#	Date	Issue Description	Solution Description	Rev.
1	P.59	8/3	Enter DVT2.0 phase	1. Change location RE25 part to 62K_0402_1% from 130K_0402_1%	X02
2	P.64	8/11	Modified according to LED brightness test result	1. Change location RZ13 part to 150_0402_5% from 1K_0402_5%	X02
3	P.77	8/11	Modified according to power button force test result	1. Change location SW1 part to 260gF from 200gF	X02
4	P.52	8/11	Modified according to the vendor and Intel recommend, if no support SSD can bypass it	1. Change location RZ42, CZ33, RZ46, RZ41, RZ37, UZ8 to un-stuff from stuff. 2. Change location RZ38 to stuff from un-stuff	X02
5	P.123	8/11	EC roll back to 5107 solution	1. Add 5107 MP chip BOM option location UE1	X02
6	P.79	8/24	Due to the different design of platform CPU POWER, it affects the time for EC to receive PRIM power good	1. Change location RZ16 part to 1M_0402_5% from 330K_0402_5%.	X02
7	P.9 P.52	8/24	Modified according to the vendor and Intel recommend, if no support SSD can bypass it	1. Change location UZ9, CZ42, RZ61, RZ55, RC103 to un-stuff from stuff 2. Change location RZ57 to stuff from un-stuff	X02
8	P.64	8/24	Modified according to the brightness test result of FPR LED	1. Change location RZ141,RZ142,RZ143,RZ144 part to 1.2K_0402_1% from 4.99K_0402_1%	X02
9	P.79	8/31	Cost down BJT part	1. Change location QZ4, RZ24 to un-stuff from stuff 2. Change location RZ133 to stuff from un-stuff	X02
10	P.52	9/2	Modified according to the vendor and recommend (Module has diode internal)	1. Change location DZ6, DZ7 part to 0_0603_5%	X02

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Item	Page#	Date	Issue Description	Solution Description	Rev.
1	P.59	10/13	Enter Pilot phase	1. Change location RE25 part to 4.3K_0402_1% from 62K_0402_1%	A00
2	P.42	10/13	Reserve for issue about leakage current from PD	1. Add location RT279 at +VIN_3V3_A_TBT, pull-down resistor 100K_0402_5% for reserved	A00
3	P.77	10/13	Fix RTC battery life issue	1. Change location RZ130 part to 2M_0201_5% from 1M_0201_5%	A00
4	P.63	10/22	According to Intel PDG2.1 about sequence and waveform result	1. Change location RZ171 BOM structure to un-stuff from stuff 2. Change location UZ19 BOM structure to stuff from un-stuff	A00
5	All	10/22	0 ohm change to short pad	1. TGL only 0 ohm change to short-PAD : 67 pcs RA10,RC345,RT12,RZ11,RC160,RC346, RT13,RZ15,RC245,RC349,RT14,RZ20, RC248,RC350,RT133,RZ60,RC250,RC355, RT154,RZ7,RC277,RC356,RT215,RZ84, RC279,RC357,RT246,RZ57,RC281,RC359, RT247,RC301,RC361,RT253,RC326,RC363, RT254,RC327,RC379,RT255,RC328,RE53, RT256,RC329,RE59,RT266,RC330,RE66, RT267,RC331,RE141,RT268,RC332,RT7, RT269,RC333,RT8,RV75,RC334,RT9, RV77,RC335,RT10,RV78,RC343,RT11,RZ103	A00
6	P.63	11/12	Fix hang hot-reset when flash EXE	1. Add location RZ175 at PCH_DPEROK_EC, pull down resistor 100K_0201_5%	A01

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