A34 Schematics

Tiger Lake-UP3

15 SKUD UMA S16G SIT

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Taipei Hsien 221, Taiwan, R.O.C.

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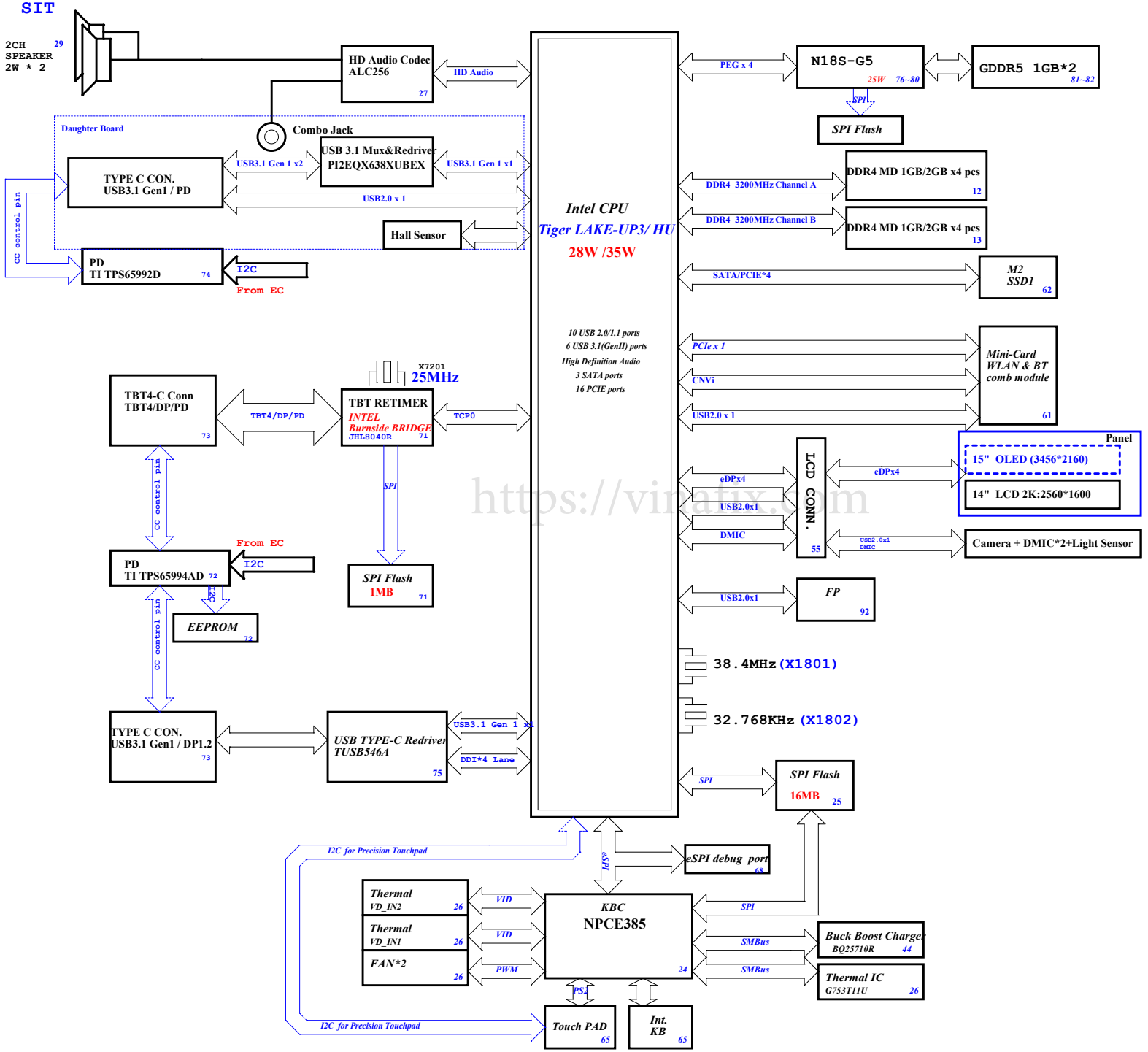
Project Code: 4PD0MW010001(A34)
4PD0MS010001(A35)
PCB No : 203027
Revision : SIT

A34_TGL(14")/A35_TGL(15") Block Diagram



GPU DC/DC RT8813DGQW	85	CHARGER BQ25710	44
	OUTPUTS	INPUTS	OUTPUTS
19V_DCBATOUT	1V_VGACORE_S0	19V_AD+ BT+	19V_DCBATOUT
GPU DC/DC G5335FQZ1U	86	SYSTEM DC/DC SY8288CRAC	45
	OUTPUTS	INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_VGA_S0	19V_DCBATOUT	5V_AUX_S5 5V_S5
GPU DC/DC TPS22976	86	SYSTEM DC/DC SY8288BRAC	45
	OUTPUTS	INPUTS	OUTPUTS
	1D8V_AON_S0	19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5
GPU DC/DC TPS22976	86	CPU DC/DC RT3612EBGQW	46,47
	OUTPUTS	INPUTS	OUTPUTS
	1D8V_VGA_S0	19V_DCBATOUT	1V_CPU_CORE
GPU DC/DC G2822DRC1U	86	CPU DC/DC RT3612EBGQW	46,50
	OUTPUTS	INPUTS	OUTPUTS
	1V_VGA_S0	19V_DCBATOUT	1D8V_VCCIN_AUX
		CPU DC/DC RT3612EBGQW	46,48
		INPUTS	OUTPUTS
		19V_DCBATOUT	1V_VCCSA
		CPU DC/DC G5416QS1U	51
		INPUTS	OUTPUTS
		19V_DCBATOUT	1D2V_S3
		3D3V_S5	2D5V_S5
		SYSTEM DC/DC G5335DQZ1U	53
		INPUTS	OUTPUTS
		3D3V_S5	1D8V_S5
		SYSTEM Load switch G5027CRD1D	40
		INPUTS	OUTPUTS
		1D05V_S5_OUT	1V_VCCST 1V_VCCSTG

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Title: Block Diagram

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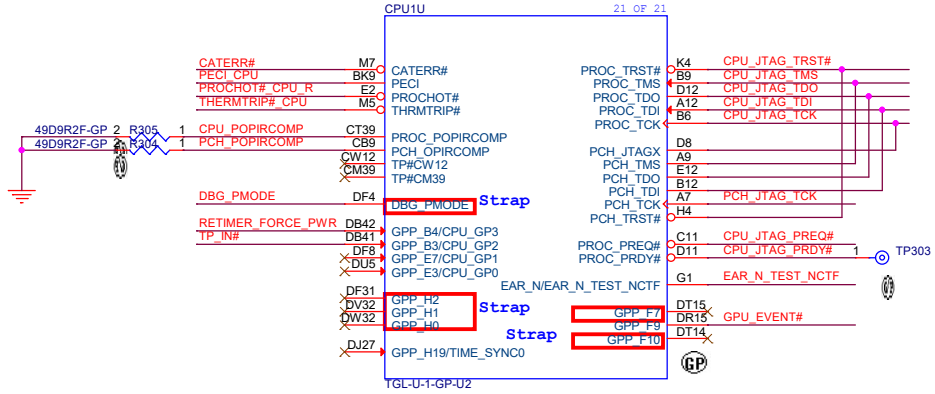
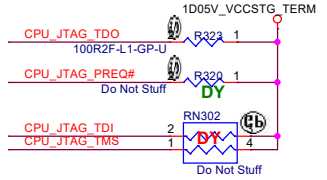
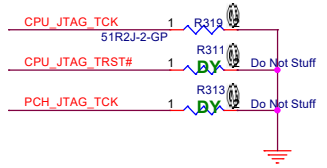
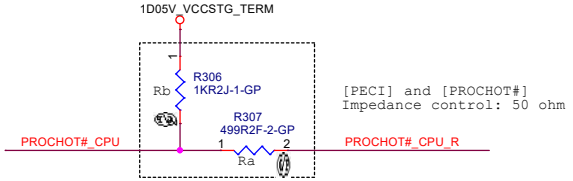
Main Func = CPU

24 PECI_CPU
22,24,44,46 PROCHOT#_CPU
26 THERMTRIP#_CPU
65 TP_IN#
79 GPU_EVENT#
15 DBG_PMODE
71,72 RETIMER_FORCE_PWR









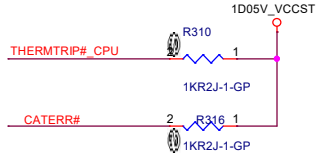
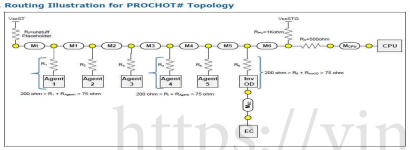
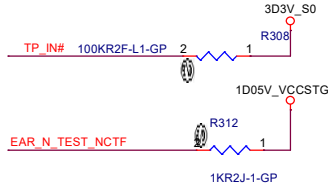


Figure 10-1. Routing Illustration for PROCHOT# Topology





M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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Title: CPU (THML/JTAG)
Size: Custom
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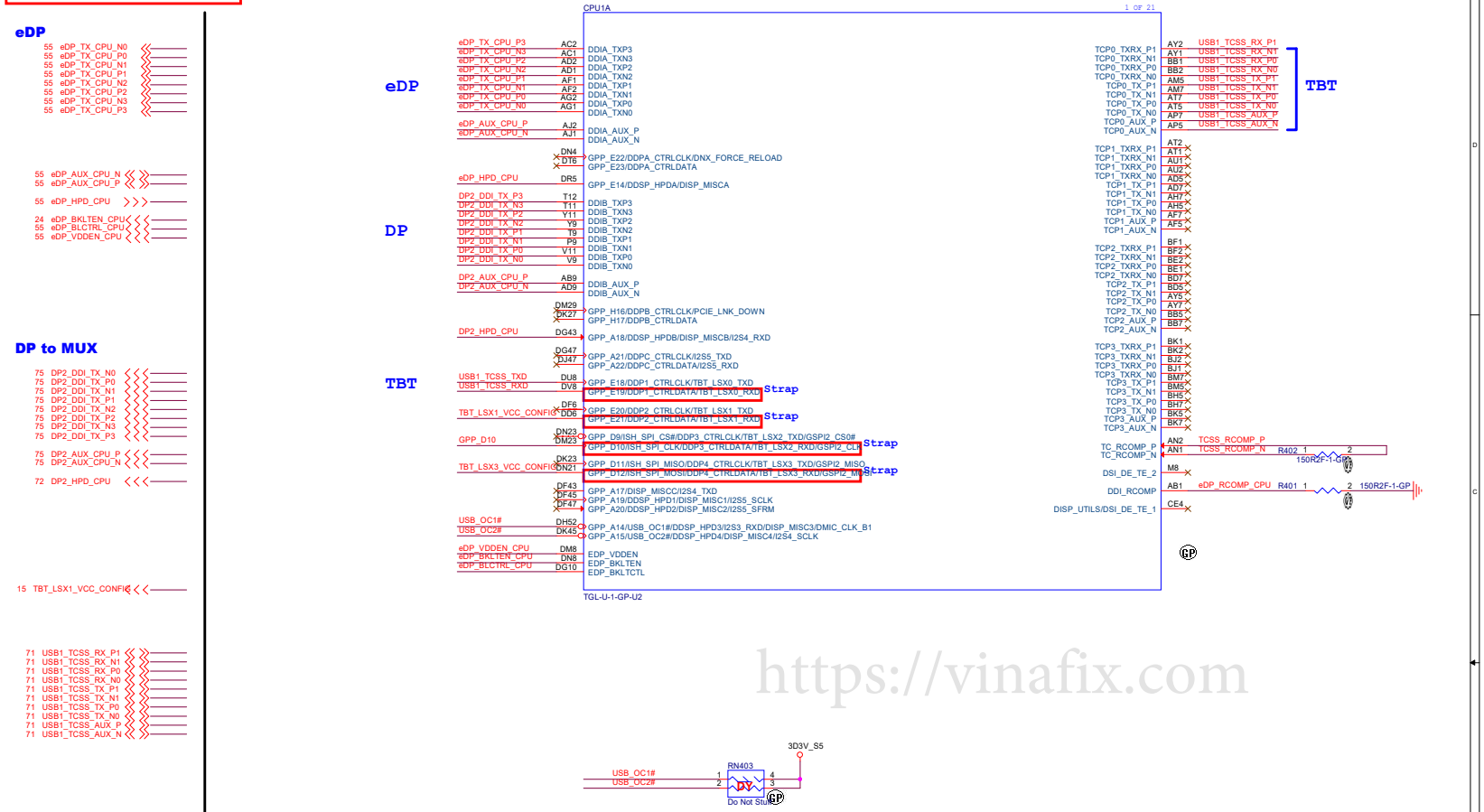
Main Func = CPU



Document Number: 607872 Ver 1.2

Port	Function	DDI Signal Name	DP Signal Name
DDI B	Main Link	DDIB_TXP[0]	DDIB_DP_LANE0_P
		DDIB_TXN[0]	DDIB_DP_LANE0_N
		DDIB_TXP[1]	DDIB_DP_LANE1_P
		DDIB_TXN[1]	DDIB_DP_LANE1_N
		DDIB_TXP[2]	DDIB_DP_LANE2_P
		DDIB_TXN[2]	DDIB_DP_LANE2_N
		DDIB_TXP[3]	DDIB_DP_LANE3_P
		DDIB_TXN[3]	DDIB_DP_LANE3_N
	Aux	DDIB_AUX_P	DDIB_DP_AUX_P
		DDIB_AUX_N	DDIB_DP_AUX_N
	HPD	DDSP_HPDB	DPB_HPD

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Title: CPU (DDI/EDP)

Size: Custom | Document Number: A34_TGL | Rev: SDV

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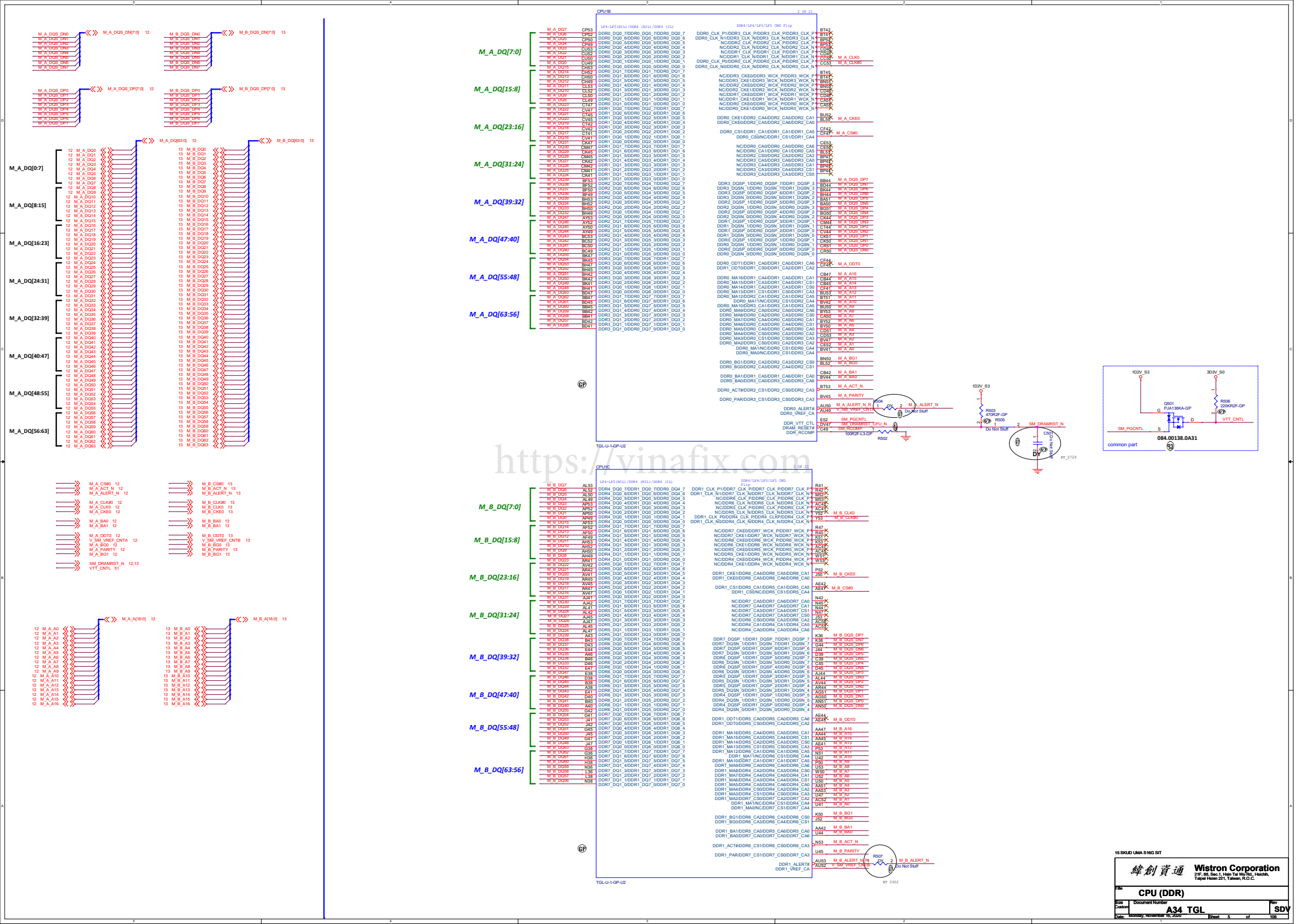

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Title: CPU (DDR)

Size	Document Number	Rev
Custom	A34_TGL	SDV

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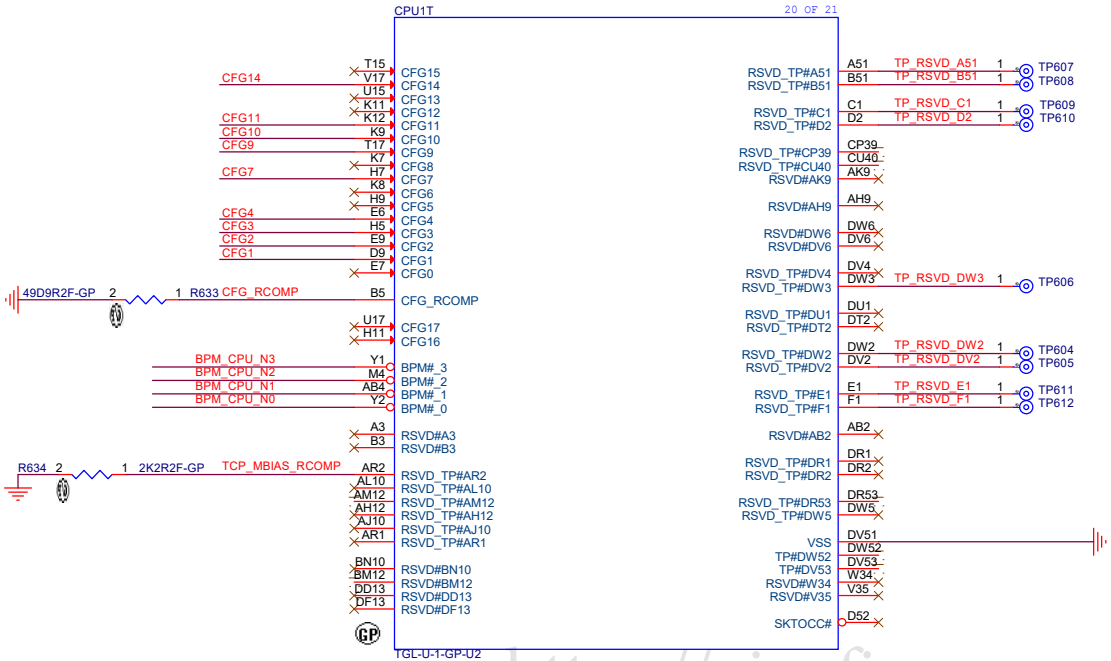
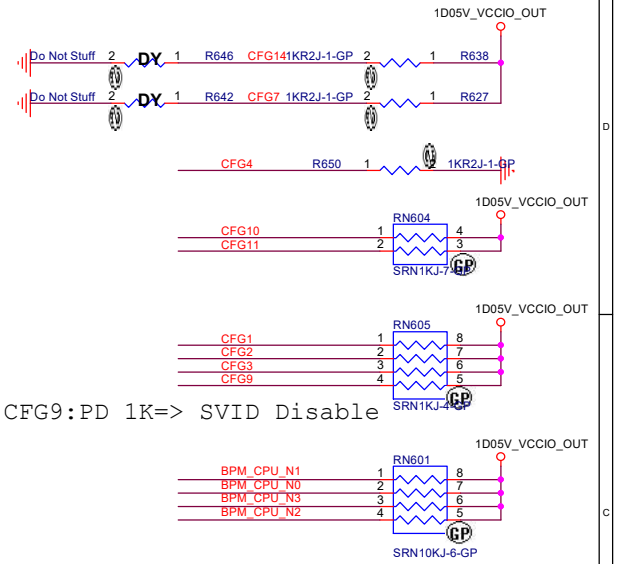
Main Func = CPU





CFG9:PD 1K=> SVID Disable

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

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Title: CPU (CFG/IST)

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Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

CPU1M 13 OF 21

1V_CPU_CORE

VCCIN: A24, A26, A29, A30, A33, A35, AY39, B24, B26, B29, B30, B33, B35, BA10, BA40, BB39, BB9, BC10, BC40, BD39, BD9, BE10, BE40, BF9, BG10, BG40, BH12, BH39, BH9, BJ10, BJ40, BK39, BL10, BL40, BM39, BN40, BP12, BP39, BR10, BR40, BT12, BT39, BU10, BU40, BV12, BY12, CA10, CB12, D24, D26, D29, D30, D33, D35, E24, E26, E27, E29, E30, E32, E33, G2, G24, G26, G30

1V_CPU_CORE

VCCIN: G32, H24, H26, H30, H32, J1, J2, K1, K2, K24, K26, K30, K32, L24, L26, L30, L32, N24, N26, N30, N32, P24, P26, P28, P30, P32, T21, T23, T25, T27, T31, U23, U27, U29, U31, U33, V23, V25, V27, V29, V31, V33, W22, W24, W28, W32

VCCIN_SENSE
VSSIN_SENSE

R38 VCCCORE_SENSE
R37 VSSCORE_SENSE

VIDSOUT
VIDSCK
VIDALERT#

M12 SVID_DATA_CPU
M11 SVID_CLK_CPU
P12 SVID_ALERT#_CPU

TGL-U-1-GP-U2

1D05V_VCCST

R703 1 2 100R2F-L1-GP-U SVID_DATA_CPU
R701 1 2 56R2J-4-GP SVID_ALERT#_CPU
R706 1 2 Do Not Stuff SVID_CLK_CPU

DY

ET_0729

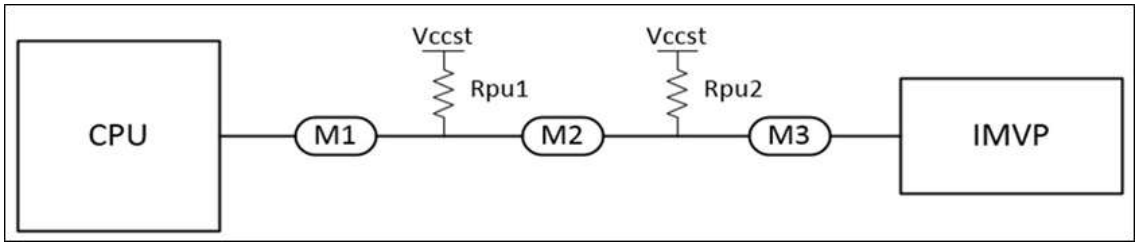
Layout note:
Length matchin 25mil, and close SOC in 2inch "

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

1V_CPU_CORE

R704 1 2 100R2F-L1-GP-U VCCCORE_SENSE
R705 2 100R2F-L1-GP-U VSSCORE_SENSE



Notes	Details
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSCK platform resistors	Rpu1=empty, Rpu2=45Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=empty
Platform resistors tolerances	5%
Route ordering	When routing at minimum spacing route Alert betweeen Data and Clock

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Title: **CPU (VCORE/VID)**

Size: Custom | Document Number: **A34_TGL** | Rev: **SDV**

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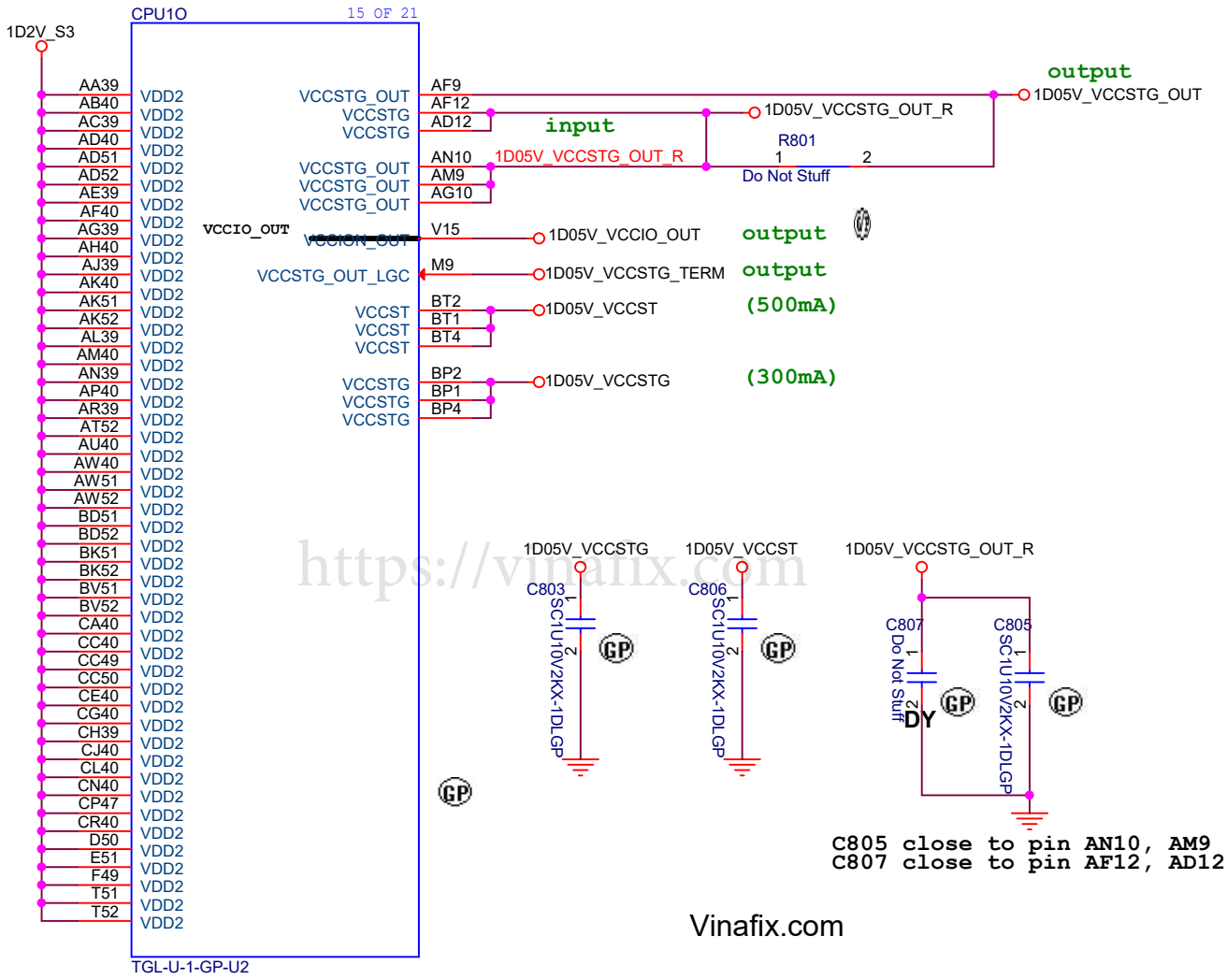
Main Func = CPU



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Title	CPU (VCCGT/VCCIO/VDDQ/VCCSA)	
Size A4	Document Number A34_TGL	Rev SDV
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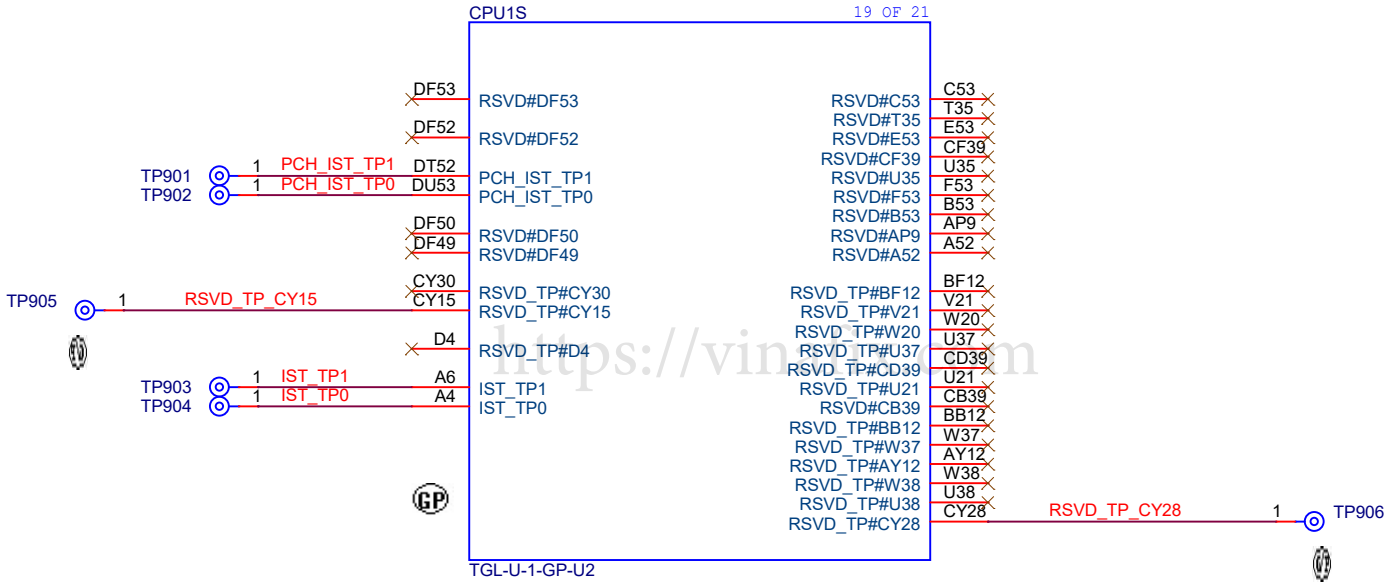
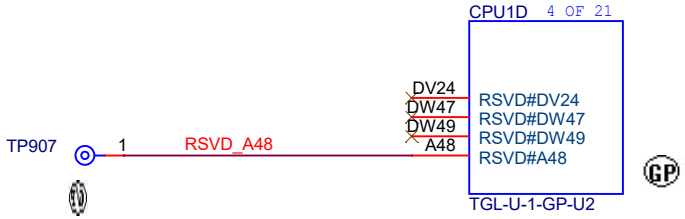


REFER DOC#614056 FOR ES1 WORKAROUND CIRCUIT FOR PINs CY15 and CY28.



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Title	CPU	
Size A4	Document Number A34_TGL	Rev SDV
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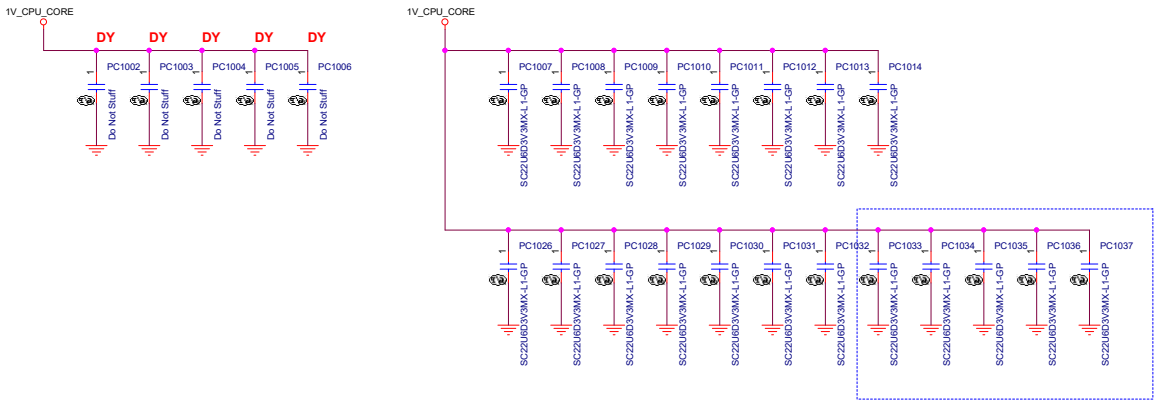
Main Func = CPU

VCORE

TGL_U42

U42
IccMax current-10ms max = 65 A

22uF	PCS	Cap
U42	15+5	330uF*1



TGL-UP3_8L_T3_DS_VCCIN

Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN	Secondary Side	0402	10 uF	12
	Primary Side	7343	220 uF	2
		7343	PH	2
		0603	22 uF	8

TGL-UP3_8L_T3_SS_VCCIN

Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN	Primary Side	7343	220 uF	2
		7343	PH	2
		0603	22 uF	10
		0402	10 uF	12

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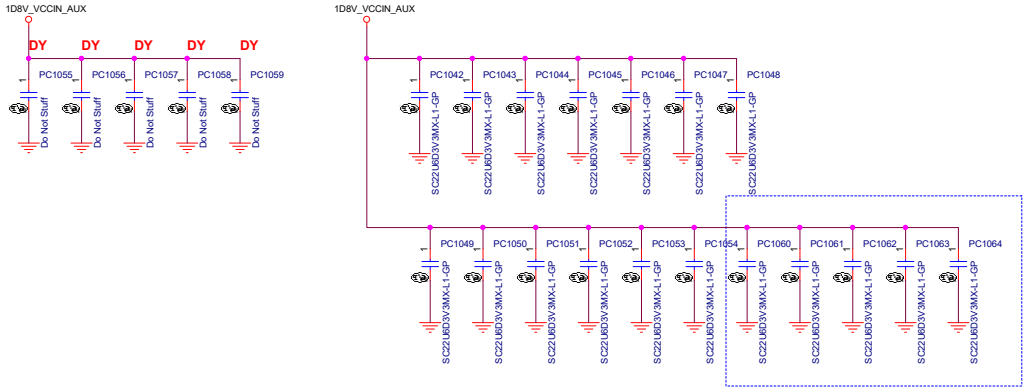
VCCINAUX

RT6543

22uF	PCS	Cap
U42	13+5	330uF*1



TGL-UP3_8L_T3_DS_VCCIN_AUX

Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX	CPU Primary Side	7343	220uF	1
		0805	47uF	3
		0805	Placeholder	3
		0603	22uF	12
		0402	10uF	15
	CPU Secondary side	0402	10uF	10

TGL-UP3_8L_T3_SS_VCCIN_AUX

Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX	CPU Primary Side	7343	220uF	2
		0805	47uF	3
		0805	Placeholder	3
		0603	22uF	12
		0402	10uF	17

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Title: CPU_(Power CAP1)

Size: Custom | Document Number: A34_TGL | Rev: SDV

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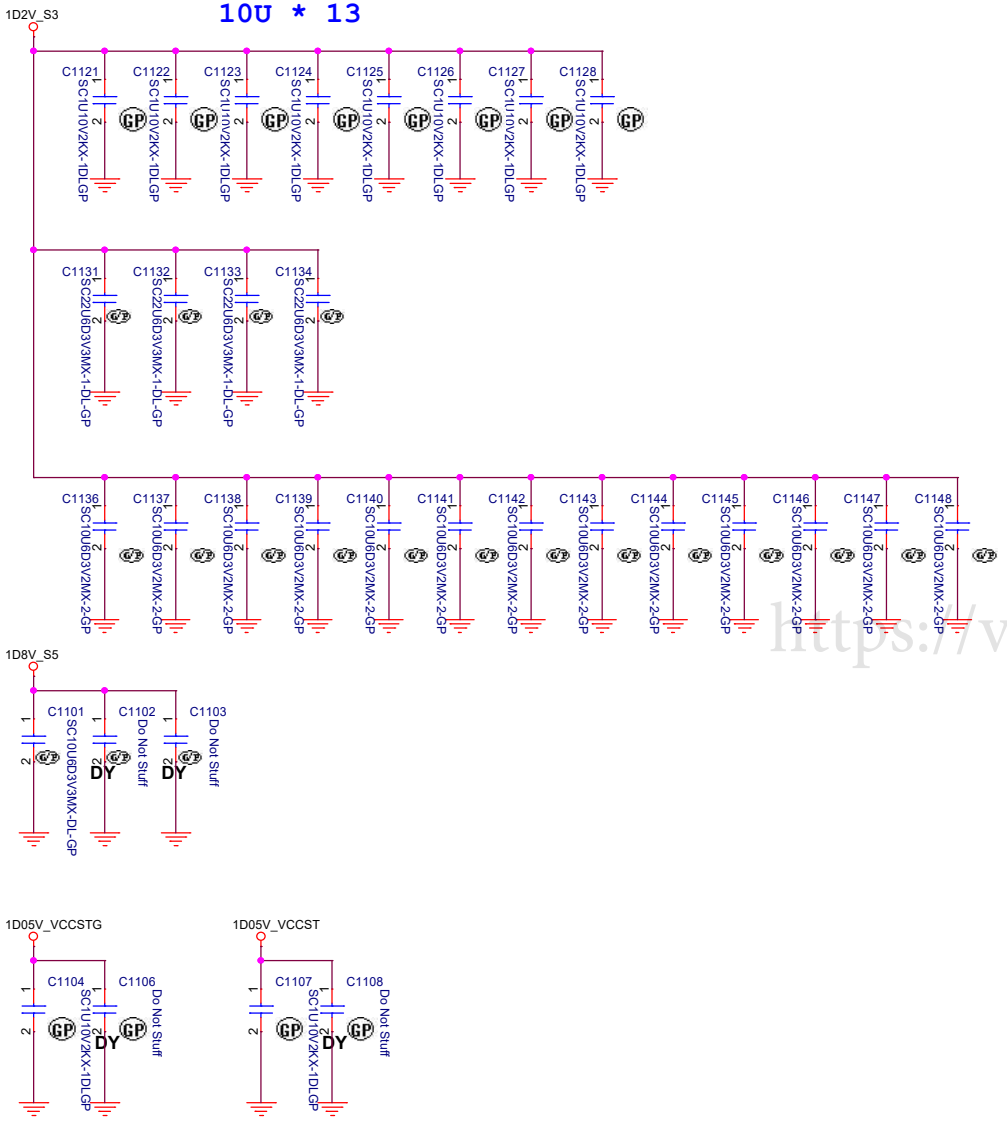
Main Func = CPU

VDDQ

1U * 8
22U * 4
10U * 13



TGL-UP3_8L_T3_DS_VDD2

Power Rail	Decap Placement	Form Factor	Value	Number
VCCDD2	Secondary Side	0402	10uF	8
	Primary Side	0603	47uF	2
		0402	1uF	8

TGL-UP3_8L_T3_SS_VDD2

Power Rail	Decap Placement	Form Factor	Value	Number
VCCDD2	Primary Side	0603	47uF	2
		0402	1uF	8
		0402	10uF	13

TGL-UP3_VCCST

Power Rail	Decap Placement	Form Factor	Value	Number
VCCST	Primary/Secondary Side	0402	1uf	2

TGL-UP3_VCCSTG

Power Rail	Decap Placement	Form Factor	Value	Number
VCCSTG	Primary/Secondary Side	0402	1uf	2

Document Number: 607872 Ver 1.1

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Title: *CPU (Power Cap2)*

Size: Custom | Document Number: A34_TGL | Rev: SDV

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Main Func = DIMM1

SDP & DDP SETTING

R1212~R1215:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

Alt 2

	SDP x16	DDP x16
E9		Re9 0Ω
		Rm9 open
M9		Rm9b 0Ω
A9	VSS	BG1

SDP x16: 0Ω
DDP x16: 240Ω, 0Ω, open

0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

Close to CPU1

VDDQ/VDD 1uF x16

VPP 1uF x8

VTT 1uF x8

VDDQ/VDD 10uF x5

VPP 10uF x2

VTT 10uF x2

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Title: DDR (DDR4-CHA)	
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Main Func = DIMM2

SDP & DDP SETTING

R1331~R1334:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

Alt 2

	SDP x16	DDP x16
E9	VSS	UZQ
M9	VSS	BG1

Controller BG1

	SDP x16	DDP x16
Re9	0Ω	240Ω
Rm9	open	0Ω
Rm9b	0Ω	open

0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

Close to CPU1

VDDQ/VDD 1uF x16

VDDQ/VDD 10uF x5

VPP 1uF x8

VPP 10uF x2

VTT 1uF x8

VTT 10uF x2

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(Blanking)

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Title	DDR (RSVD) (DDR4-CHA1)	
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18 SPI_SI_CPU
18 SPI_WP_CPU
18 SPI_HOLD_CPU
21,61 CNV_RGI_DT
18 GPP_C5/SML0ALERT#
18 GPP_E6
19 HDA_SDOUT_CPU
4,71 USB1_TCSS_RXD
3 DBG_PMODE
4 TBT_LSX1_VCC_CONFIG
18 GPP_E10
18 GPP_E11
4 TBT_LSX3_VCC_CONFIG
4 GPP_D10

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	=20K PD= R1501 DY Do Not Stuff GPP_C5/SML0ALERT# = internal 20K PD=	=NO INTERNAL= R1503 4K7R2J-2-GP SPI_SI_CPU BOOT_HALT Close to U2501 R1511 DY Do Not Stuff	=NO INTERNAL= R1504 100KR2J-1-GP GPP_E6 R1512 DY Do Not Stuff	=20K PD=	=NO INTERNAL= R1506 100KR2J-1-GP SPI_WP_CPU Close to U2501 R1514 DY Do Not Stuff CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	=20K PD= R1509 DY Do Not Stuff HDA_SDOUT_CPU	=NO INTERNAL= CNV_RGI_DT R1516 DY Do Not Stuff = PU 100K on M.2 =
High	ESPI Disable		Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=		Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	SPI0_IO3		GPP_E10	GPP_E11
Schematic	E19 PD 20K R1518 DY Do Not Stuff TBT_LSX1_TCSS_RXD R1521 DY Do Not Stuff	E21 PD 20K R1519 DY Do Not Stuff TBT_LSX1_VCC_CONFIG R1522 DY Do Not Stuff	D10 PD 20K R1520 DY Do Not Stuff GPP_D10 R1523 DY Do Not Stuff	D12 PD 20K R1524 DY Do Not Stuff TBT_LSX3_VCC_CONFIG R1525 DY Do Not Stuff	=NO INTERNAL= R1526 100KR2J-1-GP SPI_HOLD_CPU Close to U2501 DY R1527 Do Not Stuff	=20K PU= R1528 DY Do Not Stuff DBG_PMODE R1529 DY Do Not Stuff	R1531 20KR2J-L-2-GP GPP_E10	R1532 20KR2J-L-2-GP GPP_E11
High	3.3V	3.3V	3.3V	3.3V		DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V		DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	RA RB	RA RB		

Vinafix.com

15 SKUD UMA S16G SIT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: A2 | Document Number: A34_TGL | Rev: SDV

Date: Monday, November 16, 2020 | Sheet 15 of 106

Main Func = PCH

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

USB3 Type C port (MB)
75 USB1_USB30_TX_P
75 USB1_USB30_TX_N
75 USB1_USB30_RX_P
75 USB1_USB30_RX_N

USB3 Type C port (IO)
66 USB2_USB30_TX_P
66 USB2_USB30_TX_N
66 USB2_USB30_RX_P
66 USB2_USB30_RX_N

WLAN
61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_TX_C_N
61 WLAN_PCIE_TX_C_P

M.2 SSD1
63 SSD1_PCIE_TX_P0
63 SSD1_PCIE_TX_N0
63 SSD1_PCIE_RX_P0
63 SSD1_PCIE_RX_N0
63 SSD1_PCIE_TX_P1
63 SSD1_PCIE_TX_N1
63 SSD1_PCIE_RX_P1
63 SSD1_PCIE_RX_N1
63 SSD1_PCIE_TX_P2
63 SSD1_PCIE_TX_N2
63 SSD1_PCIE_RX_P2
63 SSD1_PCIE_RX_N2
63 SSD1_PCIE_TX_P3
63 SSD1_PCIE_TX_N3
63 SSD1_PCIE_RX_P3
63 SSD1_PCIE_RX_N3
65 SATAGP1

TBT Type C port 1(MB)
73 USB1_USB20_N
73 USB1_USB20_P

USB3 Type C port (MB)
73 USB2_USB20_P
73 USB2_USB20_N

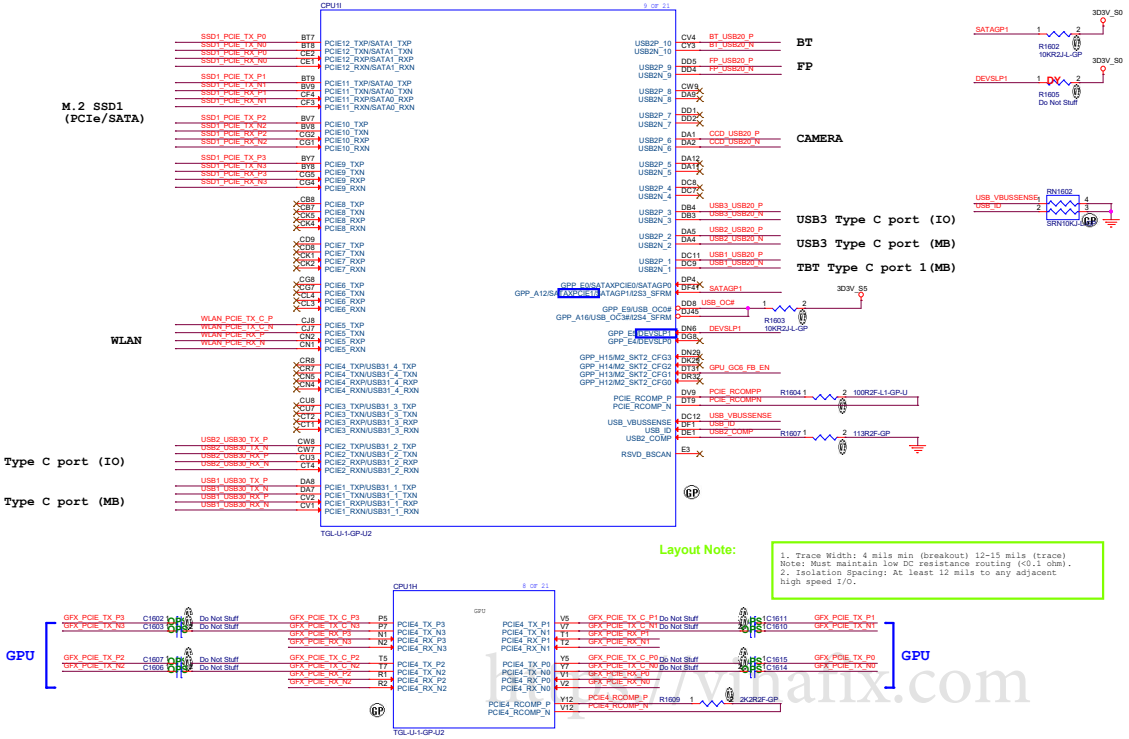
USB3 Type C port (IO)
66 USB3_USB20_P
66 USB3_USB20_N

FP
89,92 FP_USB20_P
89,92 FP_USB20_N

CAMERA
55,89 CCD_USB20_N
55,89 CCD_USB20_P

BT
61,89 BT_USB20_N
61,89 BT_USB20_P

GPU
76 GFX_PCIE_TX_P0
76 GFX_PCIE_TX_N0
76 GFX_PCIE_RX_P0
76 GFX_PCIE_RX_N0
76 GFX_PCIE_TX_P1
76 GFX_PCIE_TX_N1
76 GFX_PCIE_RX_P1
76 GFX_PCIE_RX_N1
76 GFX_PCIE_TX_P2
76 GFX_PCIE_TX_N2
76 GFX_PCIE_RX_P2
76 GFX_PCIE_RX_N2
76 GFX_PCIE_TX_P3
76 GFX_PCIE_TX_N3
76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3
79,86 GPU_GC6_FB_EN
63 DEVSLP1



Features	Premium UP3	Premium UP4
USB 2.0 Ports	10	10
PCIe Gen 3 Lanes	12	10
PCIe Root Ports	6	5
USB 3.2 Gen 2x1 Ports	4	4
SATA Ports (all 6 Gb/s capable)	2	0
AUDIO DSP Core Count	4	4

SKU	0	1	2	3	4	5	6	7	8	9	10	11
Premium UP3	USB 3.2 Gen 2x1/ PCIe 3.0	USB 3.2 Gen 2x1/ PCIe 3.0	USB 3.2 Gen 2x1/ PCIe 3.0	USB 3.2 Gen 2x1/ PCIe 3.0	PCI e 3.0	PCI e 3.0	PCIe 3.0/ GbE	PCI e 3.0 /Gb E	PCI e 3.0 /Gb E	PCIe 3.0	PCIe 3.0/ SATA	PCIe 3.0/ SATA
Premium UP4	USB 3.2 Gen 2x1/ PCIe 3.0	USB 3.2 Gen 2x1/ PCIe 3.0	USB 3.2 Gen 2x1/ PCIe 3.0	USB 3.2 Gen 2x1/ PCIe 3.0	-	-	PCIe 3.0/ GbE	PCI e 3.0 /Gb E	PCI e 3.0 /Gb E	PCIe 3.0	PCIe 3.0	PCIe 3.0

Tiger Lake PCH-LP SKU

CHIPSET SKU	Max. USB 2.0 Nbr of Ports	USB 2.0 P1	USB 2.0 P2	USB 2.0 P3	USB 2.0 P4	USB 2.0 P5	USB 2.0 P6	USB 2.0 P7	USB 2.0 P8	USB 2.0 P9	USB 2.0 P10 (or CNVi BT)	USBr1	USBr2
PREMIUM-UP4	6												
PREMIUM-UP3	10												
MAINSTREAM BASE-UP3	8												

Port Disabled | Port Enabled | Port Enabled for Intel® Wireless-AC only

Integrated Bluetooth* and USB 2.0 Design Considerations

Tiger Lake UP3

For integrated Bluetooth* functionality with the Intel® Wireless-AC (CNVi) solution, Tiger Lake PCH-LP USB 2.0 port # 10 must be used.

If integrated Bluetooth* functionality is not desired, Tiger Lake UP3 USB 2.0 port 10 may be used for USB functionality.

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12
Logical Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1	0	1	0	1
	2x2 LR	1	0	1	0	1	0	1	0	1	0	1	0
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0
	4x1	0	0	0	0	0	0	0	0	0	0	0	0
Assigned Root Ports	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	2x2 LR	RP3		RP1		RP7		RP5		RP11		RP9	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

15 SKUD UMA S16G SIT

Wistron Corporation
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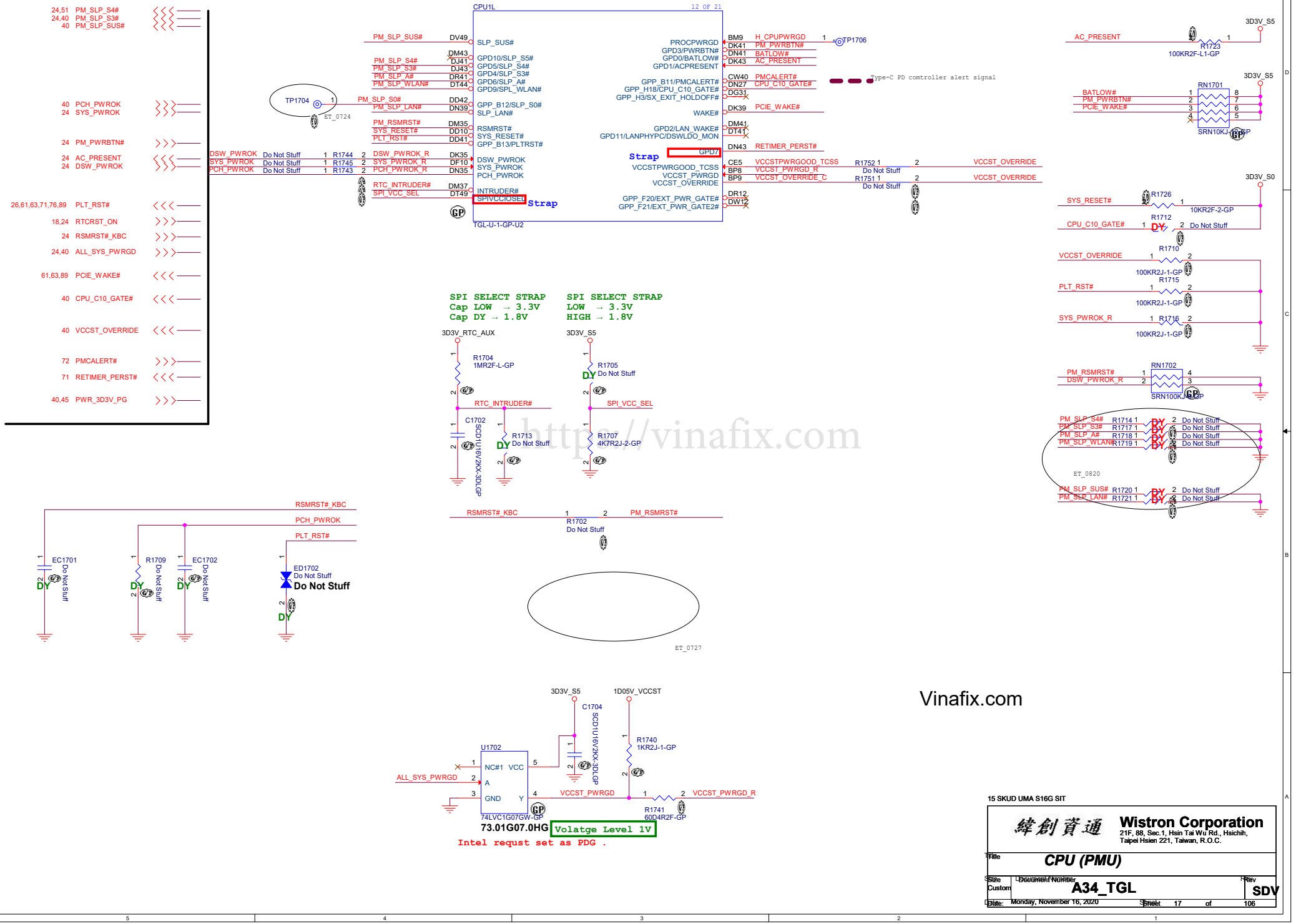
Title: CPU (PCIE/SATA/USB)
Size: Custom | Document Number: A34_TGL | Rev: SDV
Date: Monday, November 16, 2020 | Sheet 16 of 106

Main Func = PCH



15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)

Size: Custom | Document Number: A34_TGL | Rev: SDV

Date: Monday, November 16, 2020 | Sheet 17 of 106

Main Func = PCH

SPI
24,25,89 SPI_CLK_ROM
25,89 SPI_HOLD_ROM
25,89 SPI_WP_ROM
24,25,89 SPI_SO_ROM
24,25,89 SPI_SI_ROM
24,25,89 SPI_CS_CPU_N0
15 SPI_HOLD_CPU
15 SPI_WP_CPU
15 SPI_SI_CPU

WLAN
61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N

15 GPP_E10
15 GPP_E6
15 GPP_E11

SSD1
63 SSD1_CLK_CPU_N
63 SSD1_CLK_CPU_P
63 SSD1_CLKREQ_CPU_N

ESPI
24,68 ESPI_CPU_IO0
24,68 ESPI_CPU_IO1
24,68 ESPI_CPU_IO2
24,68 ESPI_CPU_IO3
24,68 ESPI_CPU_CS#
24,68 ESPI_CPU_RST#
24,68 ESPI_CPU_CLK

OTHER
71 CPU_I2C_SCL_SML0
71 CPU_I2C_SDA_SML0
72 CPU_I2C_SCL_SML1
72 CPU_I2C_SDA_SML1
15 GPP_C5/SML0ALERT#
61 SUS_CLK_CPU

76 GFX_CLK_CPU_P
76 GFX_CLK_CPU_N
76 GFX_CLKREQ_CPU_N

24 RTCRST_ON

CPU1E — 5 OF 21 — TGL-U-1-GP-U2

SPI_CLK_ROM R18101 2 SPI_CLK_CPU
SPI_HOLD_ROM R18111 2 SPI_HOLD_CPU
SPI_WP_ROM R18121 2 SPI_WP_CPU
SPI_SO_ROM R18161 2 SPI_SO_CPU
SPI_SI_ROM R18181 2 SPI_SI_CPU
SPI_CS_CPU_N0

SPI0_CLK DJ37
SPI0_IO3 DG35
SPI0_IO2 DJ39
SPI0_MISO DJ33
SPI0_MOSI DJ35
SPI0_CS1# DF35
SPI0_CS0# DG37
SPI0_CS2# DF39

GPP_E11 GPP_E11/SPI1_CLK/THC0_SPI1_CLK DJ6
GPP_E2/SPI1_IO3/THC0_SPI1_IO3 DN5
GPP_E1/SPI1_IO2/THC0_SPI1_IO2 DR9
GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1 DM6
GPP_E10 GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0 DK6
GPP_E10/SPI1_CS#/THC0_SPI1_CS# DK8
GPP_E6 GPP_E8/SPI1_CS1#/SATA_LED# DV11
GPP_E17/THC0_SPI1_INT# DW9
GPP_E6/THC0_SPI1_RST# DT8

GPP_F11/THC1_SPI2_CLK DN15
GPP_F15/GSXSRESET#/THC1_SPI2_IO3 DK13
GPP_F14/GSXDIN/THC1_SPI2_IO2 DM13
GPP_F13/GSXSLOAD/THC1_SPI2_IO1 DN13
GPP_F12/GSXDOUT/THC1_SPI2_IO0 DJ15
GPP_F16/GSXCLK/THC1_SPI2_CS# DK15
GPP_F18/THC1_SPI2_INT# DN19
GPP_F17/THC1_SPI2_RST# DV13

CL_CLK DH3
CL_DATA DH4
CL_RST# DF2

Strap
Strap

GPP_C0/SMBCLK DK21 CPU_SMB_SCL
GPP_C1/SMBDATA DM19 CPU_SMB_SDA
GPP_C2/SMBALERT# DN19 GPP_C2/SMBALERT#
GPP_C3/SML0CLK DK19 CPU_I2C_SCL_SML0
GPP_C4/SML0DATA DM17 CPU_I2C_SDA_SML0
GPP_C5/SML0ALERT# DN17 GPP_C5/SML0ALERT#
GPP_C6/SML1CLK DJ17 CPU_I2C_SCL_SML1
GPP_C7/SML1DATA CY50 GPP_B23 1
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# DJ17 CPU_I2C_SDA_SML1

vPro support on TBT ports

Slave:PD(65994&65992)

GPP_A5/ESPI_CLK DN53 ESPI_CPU_CLK_R
GPP_A3/ESPI_IO3/SUSACK# DJ53 ESPI_CPU_IO3_R
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK DH50 ESPI_CPU_IO2_R
GPP_A1/ESPI_IO1 DP50 ESPI_CPU_IO1_R
GPP_A0/ESPI_IO0 DP52 ESPI_CPU_IO0_R
GPP_A4/ESPI_CS# DK52 ESPI_CPU_CS#
GPP_A6/ESPI_RESET# DL50 ESPI_CPU_RST#

R18341 49D9R2F-GP ESPI_CPU_CLK
R18501 15R2F-2-GP ESPI_CPU_IO3
R18381 15R2F-2-GP ESPI_CPU_IO2
R18361 15R2F-2-GP ESPI_CPU_IO1
R18351 15R2F-2-GP ESPI_CPU_IO0
R18141 Do Not Stuff
R18131 75KR2J-GP

Intel requst set as PDG .

3D3V_S5
RN1806 CPU_SMB_SCL CPU_SMB_SDA — Do Not Stuff
RN1807 CPU_I2C_SCL_SML0 CPU_I2C_SDA_SML0 — Do Not Stuff
RN1804 CPU_I2C_SCL_SML1 CPU_I2C_SDA_SML1
SRN2K2J-1-GP

GPP_C2/SMBALERT# Do Not Stuff R1802 3D3V_S5

CPU1K — 11 OF 21 — TGL-U-1-GP-U2

CLKOUT_PCIE_P6 BW1
CLKOUT_PCIE_N6 BW2
CLKOUT_PCIE_P5 CB2
CLKOUT_PCIE_N5 CB1
CLKOUT_PCIE_P4 BW4
CLKOUT_PCIE_N4 BW5
CLKOUT_PCIE_P3 CL7
CLKOUT_PCIE_N3 CL8
CLKOUT_PCIE_P2 CB4
CLKOUT_PCIE_N2 CB5
CLKOUT_PCIE_P1 BY4
CLKOUT_PCIE_N1 BY3
CLKOUT_PCIE_P0 CN7
CLKOUT_PCIE_N0 CN8
XCLK_BIASREF DJ5

SSD1_CLK_CPU_P
SSD1_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
GFX_CLK_CPU_P
GFX_CLK_CPU_N
R18262 1 60D4R2F-GP XCLK_BIASREF

GPP_F19/SRCCLKREQ6# DU14
GPP_H11/SRCCLKREQ5# DF23
GPP_H10/SRCCLKREQ4# DG25
GPP_D8/SRCCLKREQ3# DT24
GPP_D7/SRCCLKREQ2# DT30 SSD1_CLKREQ_CPU_N
GPP_D6/SRCCLKREQ1# DV30 WLAN_CLKREQ_CPU_N
GPP_D5/SRCCLKREQ0# DW30 GFX_CLKREQ_CPU_N

XTAL_OUT DM1 XTL_38D4M_X2_CPU
XTAL_IN DL1 XTL_38D4M_X1_CPU
GPD8/SUSCLK DW41 SUS_CLK_CPU
RTCX2 DT47 XTL_32K_X2_CPU
RTCX1 DR47 XTL_32K_X1_CPU
RTCRST# DN37 RTC_RST#
SRTCRST# DK37 SRTC_RST#

WLAN
SSD1 (Gen3)
GPU (Gen4)

3D3V_S0
RN1803 GFX_CLKREQ_CPU_N WLAN_CLKREQ_CPU_N SSD1_CLKREQ_CPU_N
SRN10KJ-6-GP

XTL_38D4M_X1_CPU — C1805 SC12P50V2JN-3GP-U
R1827 200KR2F-L-3-GP
X1803 XTAL-38D4MHZ-38-GP
1st = 082.30040.0251
2nd = 082.30040.0241
3rd = 082.30040.0381
XTL_38D4M_X2_CPU — C1806 SC12P50V2JN-3GP-U

3D3V_RTC_AUX
RN1802 SRN20KJ-1-GP
C1801 SC1U10V2KX-1DLGP
SRTC_RST# RTC_RST#
G1802 Do Not Stuff
C1802 SC1U10V2KX-1DLGP

XTL_32K_X2_CPU
XTL_32K_X1_CPU
R1815 10MR2J-L-GP
X1802 XTAL-32D768KHZ-6GP
1st = 082.30003.0301
C1804 SC12P50V2JN-3GP
C1803 SC12P50V2JN-1GP

RTCRST_ON — Q1802 2N7002K-2-GP-U — RTC_RST#
R1846 100KR2F-L1-GP
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

PCI Express* Signal Groups

Signal Group	Signal Name	Description
Input PCI Express*	PCIE4_RX_P[3-0] PCIE4_RX_N[3-0]	PCI Express* Receive Differential Pair
Output PCI Express*	PCIE4_TX_P[3-0] PCIE4_TX_N[3-0]	PCI Express* Transmit Differential Pair
COMP	PCIE4_RCOMP_P PCIE4_RCOMP_N	PCI Express* Compensation
Note: Customer can use PCH CLKOUT_SRC_P [4, 3, 0] clock out signals for PCIe gen4.		

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/ESPI/SMBS/XTAL/CLK)
Size: Custom | Document Number: A34_TGL | Rev: SDV
Date: Monday, November 16, 2020 | Sheet 18 of 106

Main Func = PCH

27 HDA_SDIN0_CPU
27 HDA_SDOUT_CODEC
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
15 HDA_SDOUT_CPU

24,85 DGPU_PWROK

55 DMIC1_SCL_CPU
55 DMIC1_SDA_CPU

24 ME_UNLOCK

21,61 CNV_RF_RESET#

61,89 BLUETOOTH_EN

76 DGPU_HOLD_RST#

7 OF 21

CPU1G

HDA_BITCLK_CPU — DR38 — GPP_R0/HDA_BCLK/I2S0_SCLK
HDA_SYNC_CPU — DU37 — GPP_R1/HDA_SYNC/I2S0_SFRM
HDA_SDOUT_CPU — DT37 — GPP_R2/HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU — DV37 — GPP_R3/HDA_SDI0/I2S0_RXD

Strap

TP1901

HDA_RST#_CPU — DV41 — GPP_R4/HDA_RST#
DMIC1_SCL_CPU — DL53 — GPP_A7/I2S2_SCLK/DMIC_CLK_A0
DMIC1_SDA_CPU — DG51 — GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
DG50 — GPP_A10/I2S2_RXD/DMIC_DATA1
DL49 — GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
DL52 — GPP_A11/PMC_I2C_SDA/I2S3_SCLK

R1919 200R2F-L-GP
BLUETOOTH_EN — DH49 — GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
SNDW_RCOMP — DF33 — SNDW_RCOMP

GPP_F8/I2S_MCLK2_INOUT — DW15 — DGPU_PWROK
GPP_D19/I2S_MCLK1 — DW24
GPP_A23/I2S1_SCLK — DG41
GPP_R7/I2S1_SFRM — DT38
GPP_R6/I2S1_TXD — DV38
GPP_R5/HDA_SDI1/I2S1_RXD — DW38 — PROJECT_ID1
GPP_S6/SNDW3_CLK/DMIC_CLK_A0 — DN31
GPP_S7/SNDW3_DATA/DMIC_DATA0 — DM31
GPP_S4/SNDW2_CLK/DMIC_CLK_A1 — DK33
GPP_S5/SNDW2_DATA/DMIC_DATA1 — DK31 — DGPU_HOLD_RST#
GPP_S2/SNDW1_CLK/DMIC_CLK_B0 — DW35
GPP_S3/SNDW1_DATA/DMIC_CLK_B1 — DV35
GPP_S0/SNDW0_CLK — DT32
GPP_S1/SNDW0_DATA — DR35

TGL-U-1-GP-U2

RN1901
HDA_SDOUT_CODEC — 1 — 8 — HDA_SDOUT_CPU
HDA_SYNC_CODEC — 2 — 7 — HDA_SYNC_CPU
HDA_BITCLK_CODEC — 3 — 6 — HDA_BITCLK_CPU
4 — 5
SRN33J-7-GP

ME_UNLOCK — R1904 1KR2J-1-GP — HDA_SDOUT_CPU

HDA_BITCLK_CODEC
DY EC1901 Do Not Stuff

3D3V_S5
R1936 UMA 10KR2J-3-GP
PROJECT_ID1
R1937 OPS Do Not Stuff

GPIO S group supports 1.8 V only.
GPIO R group supports per-group voltage configuration (3.3 V or 1.8 V) only.

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緯創資通 Wistron Corporation
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Title: CPU (HDA/I2S/SD/DMIC)

Size: A3 | Document Number: A34_TGL | Rev: SDV

Date: Monday, November 16, 2020 | Sheet 19 of 106

Main Func = PCH

68 CPU_UART2_TXD
68 CPU_UART2_RXD

61,89 WIFI_RF_EN

27 HDA_SPKR

55,89 ISH_I2C0_SCL
55,89 ISH_I2C0_SDA
24 EC_I2C_SCL_LS
24 EC_I2C_SDA_LS

65,89 CPU_I2C_SCL_TP
65,89 CPU_I2C_SDA_TP

55,89 ISH_ALS_INT#

86 DGPU_PWR_EN#
24 EC_SCI#

CPU1F

6 OF 21

HDA_SPKR
WIFI_RF_EN
PSW_CLR#

DC53 GPP_B16/GSPI0_CLK
BA51 GPP_B18/GSPI0_MOSI
DC49 GPP_B17/GSPI0_MISO
DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
DC52 GPP_B13/GSPI0_CS0#
Strap
Strap

CY49 GPP_B20/GSPI1_CLK
CY53 GPP_B22/GSPI1_MOSI
CY52 GPP_B21/GSPI1_MISO
BA50 GPP_B19/GSPI1_CS0#

DV21 GPP_C9/UART0_TXD
DT21 GPP_C8/UART0_RXD
DR21 GPP_C11/UART0_CTS#
DW21 GPP_C10/UART0_RTS#

DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD
DT19 GPP_C12/UART1_RXD/ISH_UART1_RXD
DR18 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#

CPU_UART2_TXD
CPU_UART2_RXD

DJ21 GPP_C21/UART2_TXD
DG23 GPP_C20/UART2_RXD
DJ19 GPP_C23/UART2_CTS#
DF21 GPP_C22/UART2_RTS#

DV18 GPP_C17/I2C0_SCL
DW18 GPP_C16/I2C0_SDA

Touch Pad

CPU_I2C_SCL_TP
CPU_I2C_SDA_TP

DJ23 GPP_C19/I2C1_SCL
DT18 GPP_C18/I2C1_SDA

DJ29 GPP_H5/I2C2_SCL
DJ31 GPP_H4/I2C2_SDA

DF29 GPP_H7/I2C3_SCL
DG29 GPP_H6/I2C3_SDA

DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

TGL-U-1-GP-U2

DR27 GPP_D14/ISH_UART0_TXD
DW22 GPP_D13/ISH_UART0_RXD
DV26 GPP_D16/ISH_UART0_CTS#
DT25 GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5

DGPU_PWR_EN#

DB45 GPP_B6/ISH_I2C0_SCL
DB44 GPP_B5/ISH_I2C0_SDA

ISH_I2C0_SCL
ISH_I2C0_SDA

Light SENSOR

CY39 GPP_B8/ISH_I2C1_SCL
DB41 GPP_B7/ISH_I2C1_SDA

DD47 GPP_B10/I2C5_SCL/ISH_I2C2_SCL
DD48 GPP_B9/I2C5_SDA/ISH_I2C2_SDA

DJ8 GPP_E16/ISH_GP7
DR7 GPP_E15/ISH_GP6
DR24 GPP_D18/ISH_GP5
DU25 GPP_D17/ISH_GP4
DV31 GPP_D3/ISH_GP3/BK3/SBK3
DU31 GPP_D2/ISH_GP2/BK2/SBK2
DT27 GPP_D1/ISH_GP1/BK1/SBK1
DV27 GPP_D0/ISH_GP0/BK0/SBK0

EC_SCI#
EC_SMI#
ISH_ALS_INT#

DR51 GPP_RCOMP

GPP_RCOMP
R2026 1 2 200R2F-L-GP

DN33 GPP_T3/I2C7_SCL
DT33 GPP_T2/I2C7_SDA

DG17 GPP_U5/GSPI3_CLK
DG18 GPP_U4/GSPI3_CS0#

1D8V_S0

ISH_I2C0_SCL
ISH_I2C0_SDA

G2001
NTZD3154N-G-2-GP
75.03154.07C

EC_I2C_SCL_LS
EC_I2C_SDA_LS

SDV 1026

1D8V_S0
ISH_ALS_INT# 10KR2J-3-GP 1 R2030

3D3V_S0
EC_SCI# R2002 1 10KR2J-3-GP
EC_SMI# R2001 1 BY Do Not Stuff

3D3V_S0
ET_0826
For N18S-G5
R2003 1 BY Do Not Stuff
DGPU_PWR_EN# R2027 1 OPS Do Not Stuff

3D3V_S0
PSW_CLR# R2004 1 10KR2J-3-GP

G2001
Do Not Stuff
Password Clear

1D8V_S0
ISH_I2C0_SCL
ISH_I2C0_SDA
RN2004
SRN2K2J-1-GP

3D3V_S0
CPU_I2C_SCL_TP
CPU_I2C_SDA_TP
RN2002
SRN2K2J-1-GP

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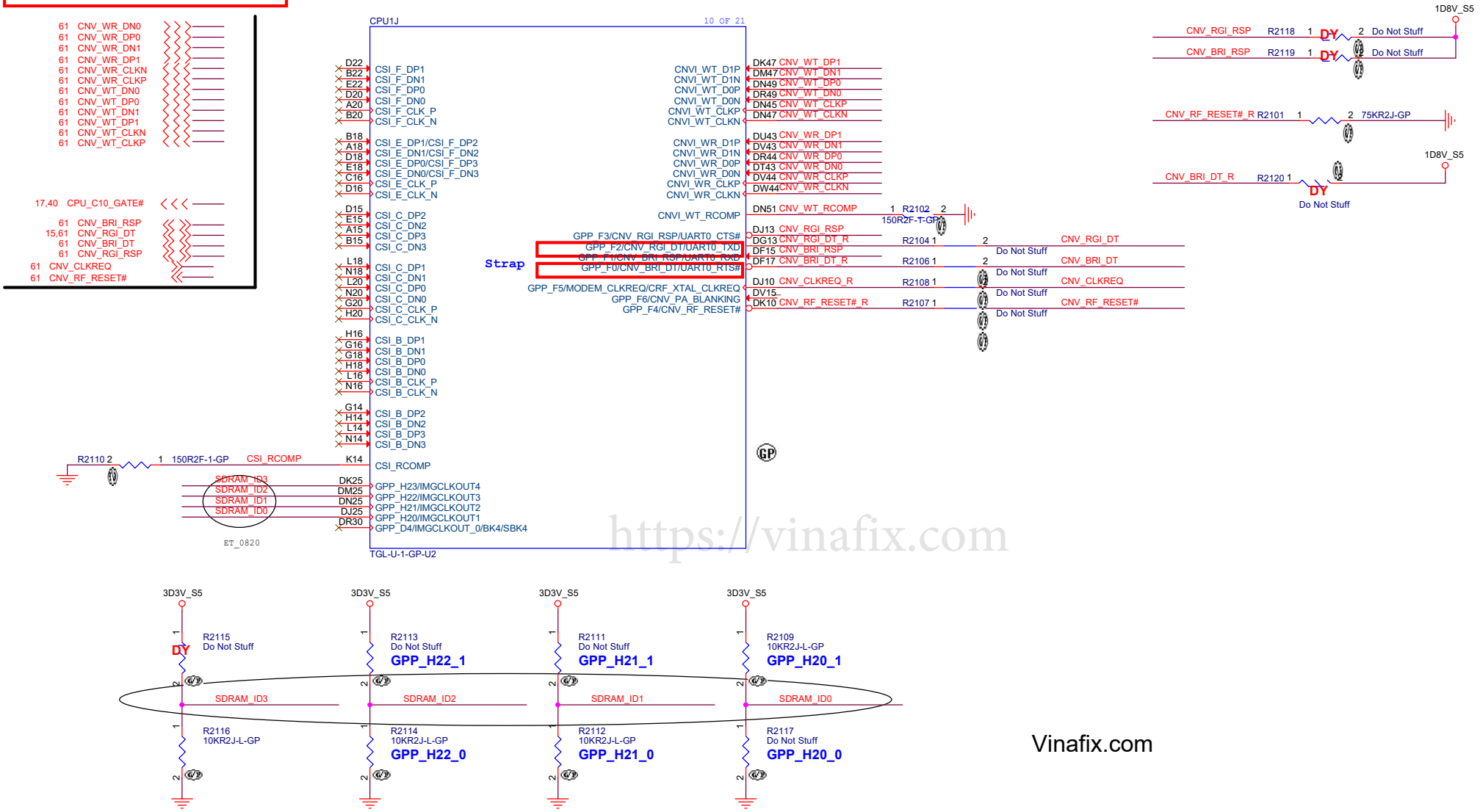
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: Custom | Document Number: A34_TGL | Rev: SDV

Date: Monday, November 16, 2020 | Sheet 20 of 106

Main Func = PCH



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RAM_ID3 / GPP_H23	RAM_ID2 / GPP_H22	RAM_ID1 / GPP_H21	RAM_ID0 / GPP_H20	Vendor	Total Density	Description	Vendor PN	Part No.
0	0	0	0	Micron	16GB	Memory 16Gb 1z SDP DDR4 3200M Micron	MT40A1G16KD-062E:E	MM20000013725
0	0	0	1	Samsung	16GB	Memory 16Gb A-Die DDR4 SDRAM 3200M Sam	K4AAG165WA-BCWE	MM20000077820
0	0	1	0	Micron	8GB	Memory 8Gb 1y DDR4 DRAM 3200M Micron	MT40A512M16TB-062E:J	MM20000013625
0	0	1	1	Samsung	8GB	Memory 8Gb C-Die DDR4 SDRAM 3200M SAM	K4A8G165WC-BCWE	MM20000077720

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Taipei Hsien 221, Taiwan, R.O.C.

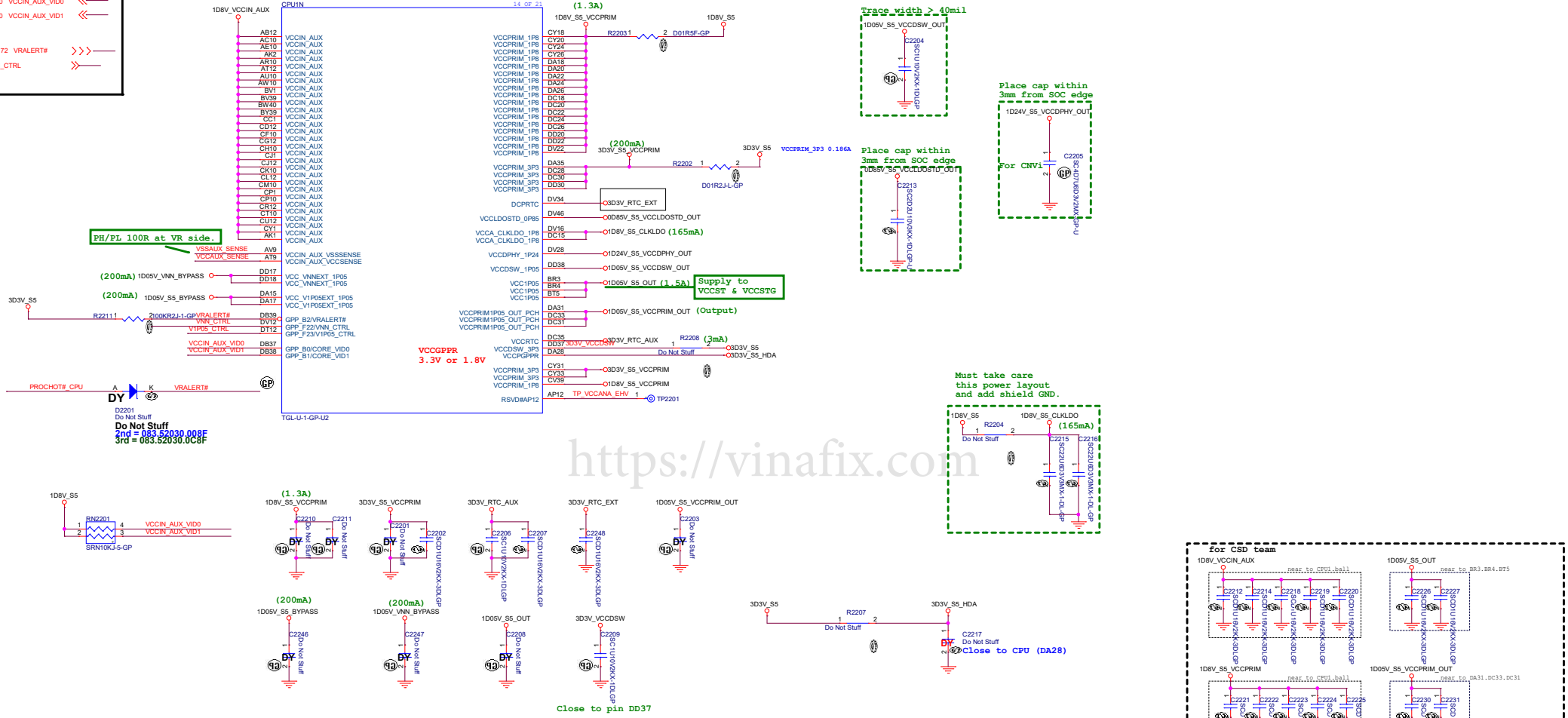
Title: CPU (EMMC/CNVi)

Size: Custom | Document Number: A34_TGL | Rev: SDV

Date: Monday, November 16, 2020 | Sheet 21 of 106

Main Func = PCH

50 VSSAUX_SENSE
50 VCCAUX_SENSE
3,24,44,46 PROCHOT#_CPU
40 V1P05_CTRL
50 VCCIN_AUX_VID0
50 VCCIN_AUX_VID1
72 VRALERT#
40 VNN_CTRL



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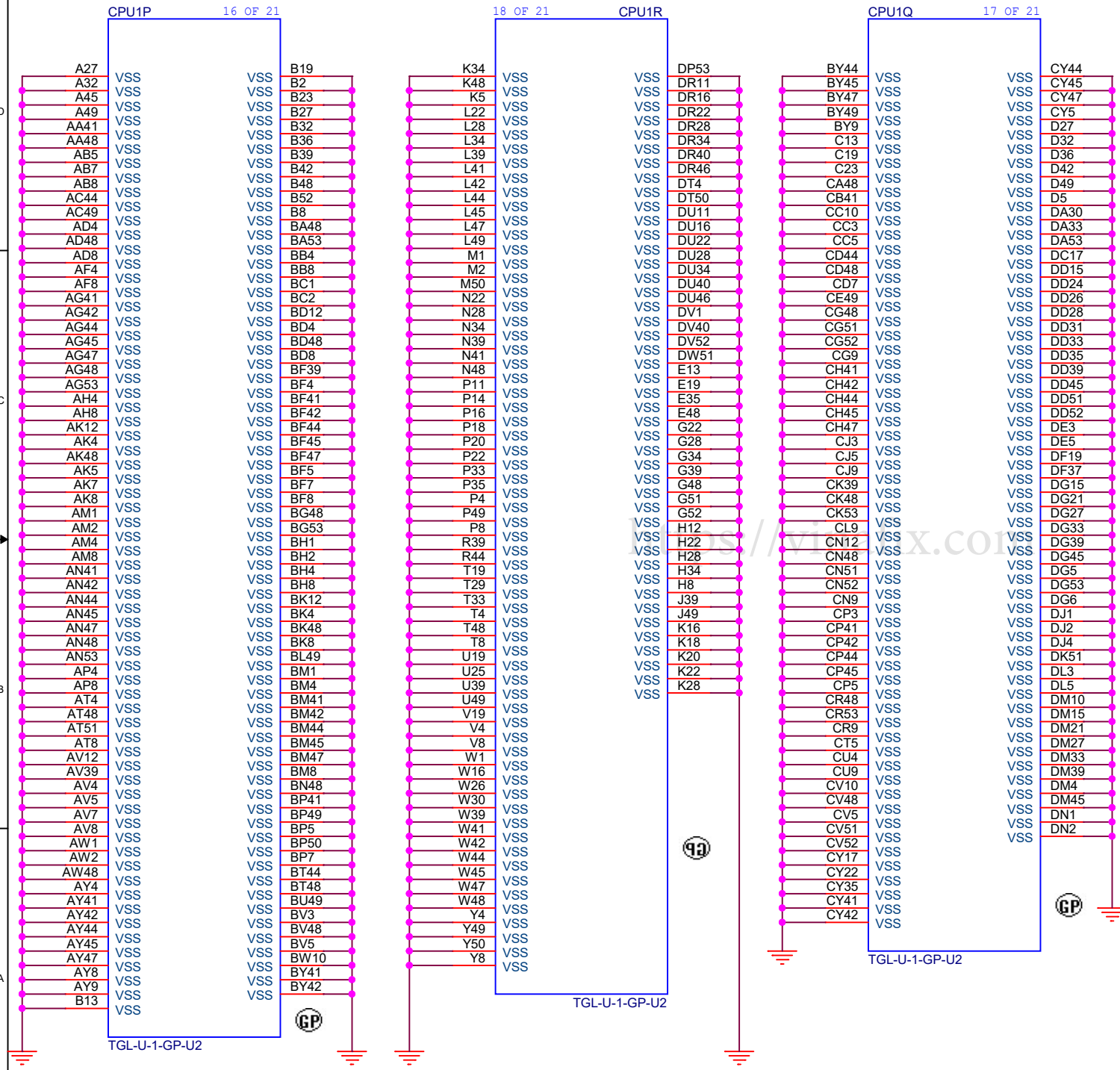
Title: CPU (PCH-LP PWR&Caps)

Size	Document Number	Rev
A2	A34_TGL	SDV

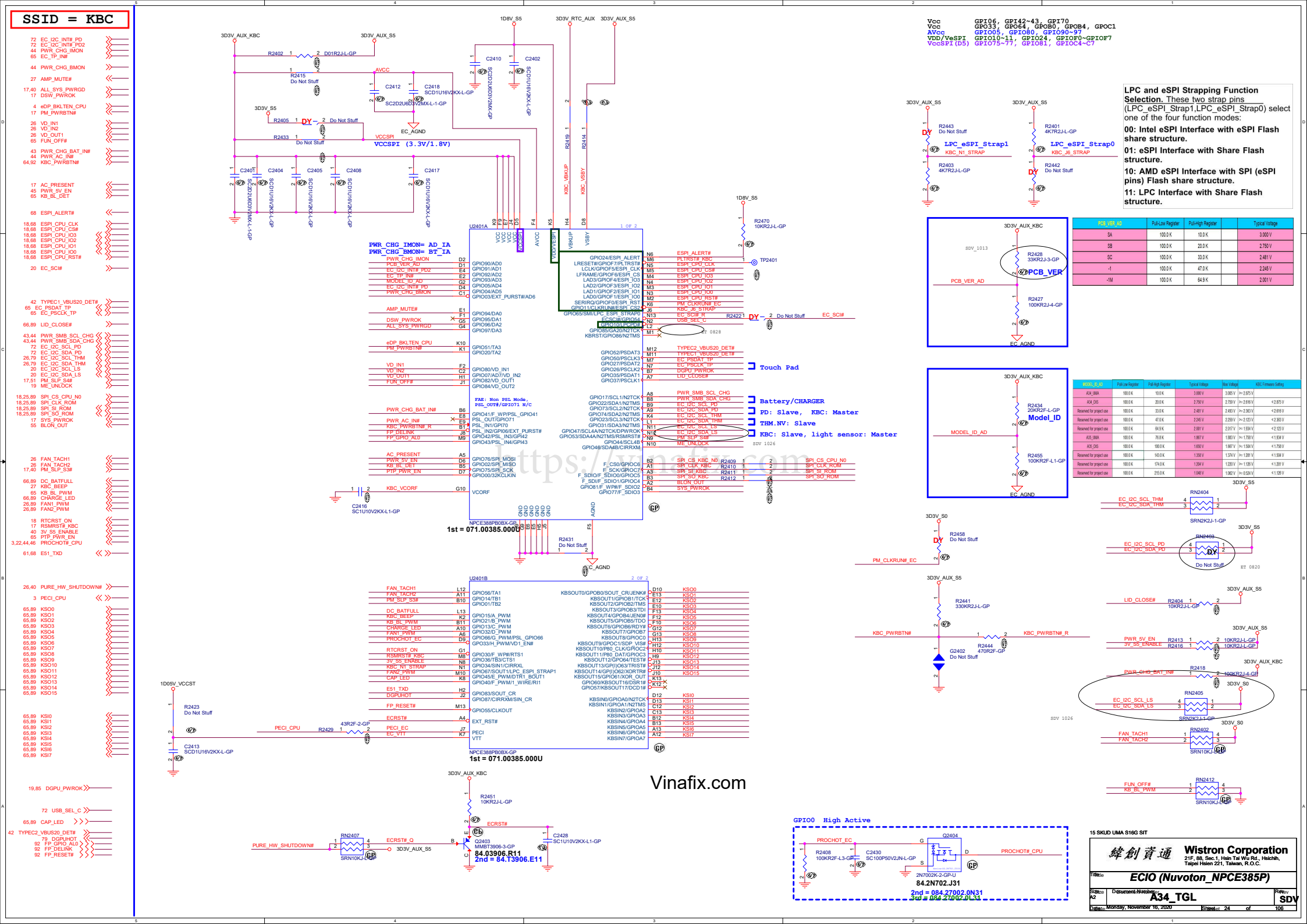
Date: Monday, November 16, 2020 Sheet 22 of 106

Main Func = PCH



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (VSS)***	
Size A4	Document Number **A34_TGL**	Rev **SDV**
Date: Monday, November 16, 2020	Sheet 23 of 106	

SSID = KBC



PCB_VER_AD	Pull-Low Register	Pull-High Register		Typical Voltage
SA	100.0 K	10.0 K		3.000 V
SB	100.0 K	20.0 K		2.750 V
SC	100.0 K	33.0 K		2.481 V
-1	100.0 K	47.0 K		2.245 V
-1M	100.0 K	64.9 K		2.001 V

MODEL_ID_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
A34_UMA	100.0 K	10.0 K	3.000 V	3.085 V	>= 2.975 V
A34_DIS	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.690 V
Reserved for project use	100.0 K	33.0 K	2.481 V	2.483 V	>= 2.383 V
Reserved for project use	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V
A35_UMA	100.0 K	76.8 K	1.807 V	1.883 V	>= 1.758 V
A35_DIS	100.0 K	100.0 K	1.650 V	1.687 V	>= 1.594 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.394 V	>= 1.281 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.139 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.924 V

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Title: ECIO (Nuvoton_NPCE385P)

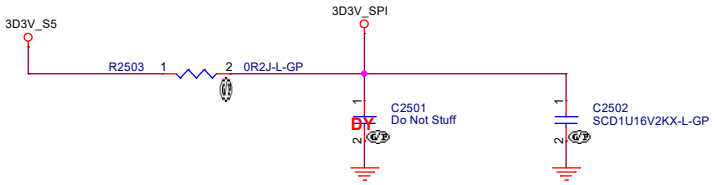
Size: A2 | Document Number: A34_TGL | Rev: SDV

Date: Monday, November 16, 2020 | Sheet 24 of 106

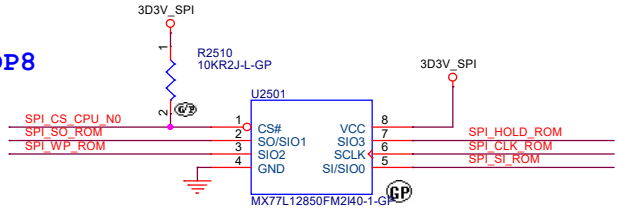
Main Func = BIOS ROM/RTC

SYSTEM SPI ROM

Length Matching between DATA and CLK should be maximum of 500 mils.

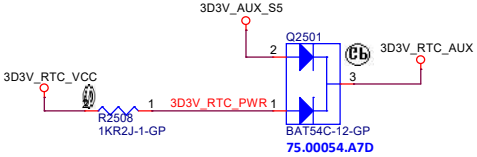


SOP8



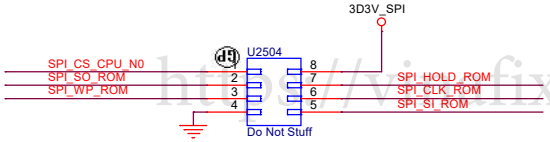
072.12850.0001

2nd = 072.25128.0A81



RPMC (Replay-Protected Monotonic Counter)

072.12850.0001	MXIC	MX77L12850FM2I40
072.25128.0A81	WINBOND	W25R128JVSIQ



Do Not Stuff

LAB

Co-Lay

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Title	*Flash/RTC*	
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SSID = Thermal

24 VD_IN1
24 VD_IN2
24,40 PURE_HW_SHUTDOWN#
24 VD_OUT1
40,46 PWR_VCORE_VR_READY
24,89 FAN1_PWM
24 FAN_TACH1
89 FAN_TACH1_C
24 FAN_TACH2
24,89 FAN2_PWM
89 FAN_TACH2_C
3 THERMTRIP#_CPU
61,63,71,76,89 PLT_RST#

3D3V_AUX_S5 — R2611 16KR2F-GP — VD_IN1
RT2601 NTC-100K-12-GP-U — T8 — 69.60011.221 — 2nd = 69.60013.201
C2607 SCD1U16V2KX-L-GP
C2608 SC100P50V2JN-L-GP

3D3V_AUX_S5 — R2612 16KR2F-GP — VD_IN2
RT2602 NTC-100K-12-GP-U — 1st = 69.60011.221 — 2nd = 69.60013.201
C2610 SCD1U16V2KX-L-GP
C2609 SC100P50V2JN-L-GP

Layou Note :Place Close to CPU1

PLT_RST# — R2609 4K7R2J-2-GP — PLT_RST#_CPU_THERM — Q2604 MMBT2222ALT1G-GP — THERMTRIP#_CPU
R2607 2K2R2J-2-GP
C2611 SCD1U16V2KX-L-GP
PURE_HW_SHUTDOWN#

3D3V_S0 — R2606 2KR2F-L1-GP — VD_OUT1
Q2603 2N7002K-2-GP-U — PWR_VCORE_VR_READY
84.2N702.J31 — 2nd = 084.27002.0N31 — 3rd = 084.27002.0L31

RT2601 close CPU and Vcore choke
VD_IN1 trace 10 mil

24,79 EC_I2C_SCL_THM
24,79 EC_I2C_SDA_THM

3D3V_S0 — RN2602 SRN2K2J-1-GP
EC_I2C_SDA_THM — Q2602 L2N7002SDW1T1G-GP — THM_SML1_DATA
EC_I2C_SCL_THM — THM_SML1_CLK
1st = 75.27002.F7C — 2nd = 075.27002.057C — 3rd = 075.67002.007C

THM261 G753T11U-GP — 074.75311.007F
THM_SML1_DATA — SMBDATA
THM_SML1_CLK — SMBCLK
ALERT# — R2608 7K5R2F-1-GP — 3D3V_S0
C2612 SCD1U16V2KX-L-GP

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2kΩ	75
	7.5kΩ	90
	10.5kΩ	100
	14kΩ	105
	18.7kΩ	110

Layout 15 mil

5V_FAN_S0 — R2643 0R3J-0-GP — 5V_S0
D2601 Do Not Stuff — Do Not Stuff — 2nd = 83.R5003.T8F
C2603 SC4D7U25V5KX-L2-GP
C2602 Do Not Stuff

FAN1_PWM
FAN_TACH1 — D2602 RB551V30-GP — FAN_TACH1_C
5V_FAN_S0
FAN1 — ACES-CON4-29-GP
83.R5003.H8H — 2nd = 83.R5003.T8F
20.F1639.004 — 2nd = 020.F0097.0004

5V_FAN2_S0 — R2644 0R3J-0-GP — 5V_S0
D2604 Do Not Stuff — Do Not Stuff — 2nd = 83.R5003.T8F
C2613 SC4D7U25V5KX-L2-GP
C2614 Do Not Stuff

FAN2_PWM
FAN_TACH2 — D2603 RB551V30-GP — FAN_TACH2_C
5V_FAN2_S0
FAN2 — ACES-CON4-29-GP
83.R5003.H8H — 2nd = 83.R5003.T8F
20.F1639.004 — 2nd = 020.F0097.0004

15 SKUD UMA S16G SIT

Wistron Corporation
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Title: Flash/RTC
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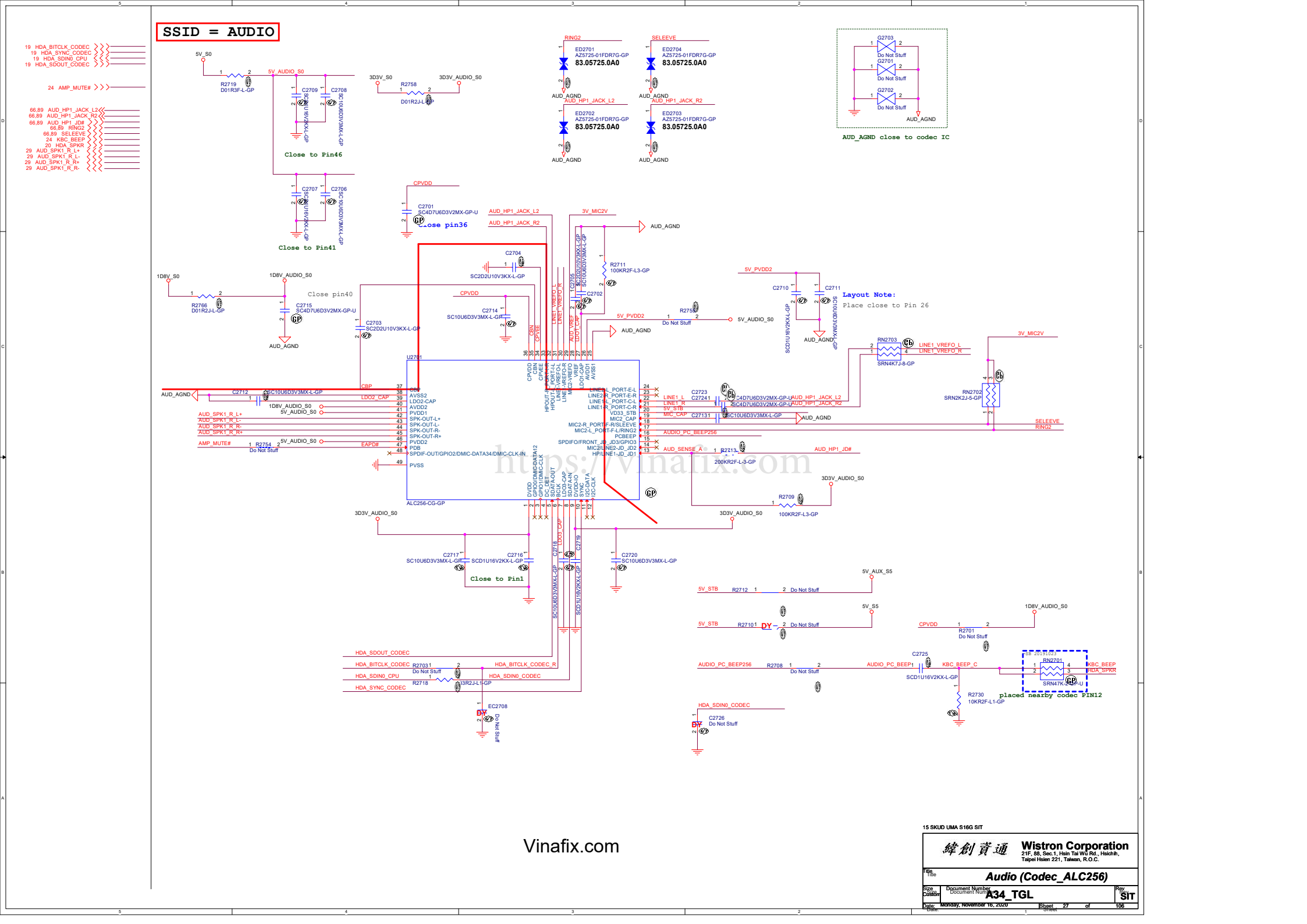
SSID = AUDIO



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Codec_ALC256)

Size: Custom | Document Number: A34_TGL | Rev: SIT

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15 SKUD UMA S16G SIT

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio (RSVD) (Audio AMP)***

Size	Document Number	Rev
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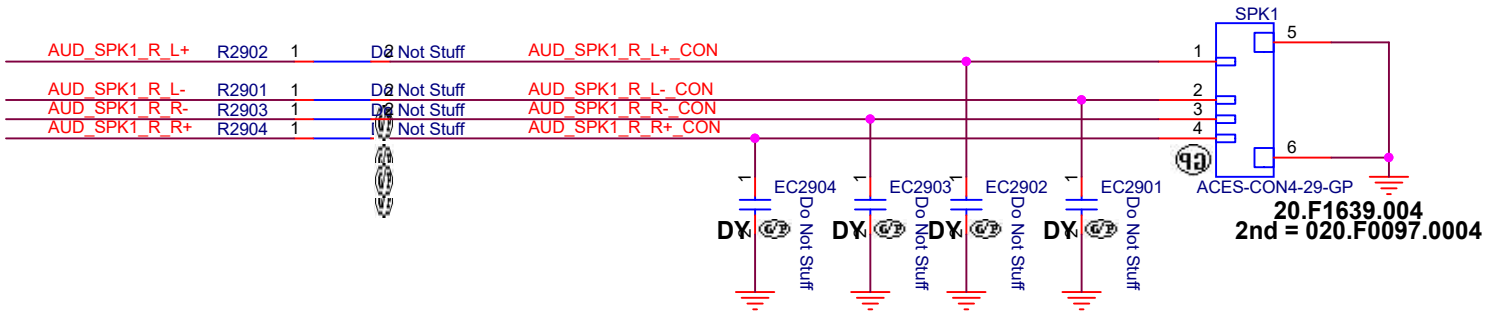
SSID = AUDIO

Speaker

27 AUD_SPK1_R_L-
27 AUD_SPK1_R_L+
27 AUD_SPK1_R_R-
27 AUD_SPK1_R_R+

89 AUD_SPK1_R_L-_CON
89 AUD_SPK1_R_L+_CON
89 AUD_SPK1_R_R-_CON
89 AUD_SPK1_R_R+_CON



20.F1639.004
2nd = 020.F0097.0004

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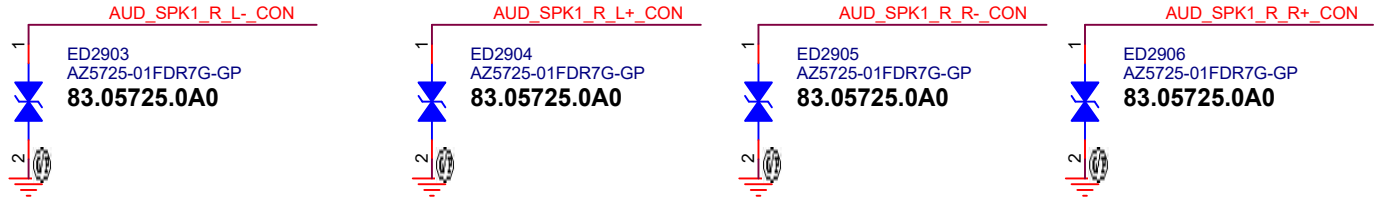

15 SKUD UMA S16G SIT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Audio(Speaker)*	
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Wistron Corporation
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Title: ***RSVD***		
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Title: ***RSVD***		
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Title: ***RSVD***		
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Title: *RSVD*		
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Title: ***RSVD***		
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Title	***RSVD***	
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15 SKUD UMA S16G SIT

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Title: ***RSVD***		
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Title: ***RSVD***		
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15 SKUD UMA S16G SIT

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Title: ***RSVD***		
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Title: ***RSVD***		
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24 3V_S5_ENABLE
24,26 PURE_HW_SHUTDOWN#
45 PWR_3D3V_EN
17,24 PM_SLP_S3#
17 CPU_C10_GATE#
22,50 VCCIN_AUX_VID0
22,50 VCCIN_AUX_VID1
17 VCCST_OVERRIDE
17,24 ALL_SYS_PWRGD
17 PCH_PWROK
51 PWR_VDDQ_PG
46 PWR_VCORE_VR_EN
26,46 PWR_VCORE_VR_READY
40,54 PWR_VNN1D05V_VID1
22 VNN_CTRL
22 V1P05_CTRL
40,54 PWR_VNN1D05V_VID1
54 PWR_VNN1D05V_VID2
50 VCCIN_AUX_PWRGD
54 PWR_VNN_EN
54 PWR_1D05V_EN
17 PM_SLP_SUS#
53 PWR_1D8V_EN
45 PWR_3D3V_PG

3V_S5_ENABLE — R4009 2KR2F-L1-GP — PWR_3D3V_EN
D4002 RB520S30-GP — PURE_HW_SHUTDOWN#
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

PWR_VCORE_VR_READY — R4019 Do Not Stuff — PCH_PWROK
PM_SLP_S3# — D4001 RB520S30-GP — C4001 Do Not Stuff
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

3D3V_S5 — R4017 1KR2J-L2-GP
PM_SLP_S3# — D4005 RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F
PWR_VDDQ_PG — R4001 Do Not Stuff
C4005 Do Not Stuff
ALL_SYS_PWRGD — R4002 Do Not Stuff — PWR_VCORE_VR_EN

3D3V_S0/5V_S0

5V_S5 — U4007 VBIAS
3D3V_S5 — C4018 SC1U10V2KX-L1-GP — IN1#1 IN1#2 IN2#6 IN2#7
5V_S5 — C4014 SC1U10V2KX-L1-GP
PM_SLP_S3# — R4008 Do Not Stuff — 3V_5V_S0_EN — EN1 EN2
CT1 CT2 — SW_3D3V_S0_CT — SW_5V_S0_CT — C4016 Do Not Stuff — C4015 Do Not Stuff
OUT1#13 OUT1#14 OUT2#8 OUT2#9 — 3D3V_S0 — 5V_S0
GND THERMAL_PAD — C4019 SC1U10V2KX-L1-GP — C4020 SC1U10V2KX-L1-GP
C4021 Do Not Stuff
G2898KD1U-GP
074.02898.0093
2nd = 074.05209.0093

5V_S0 — D4006 Do Not Stuff
3D3V_S0 — D4007 Do Not Stuff

3D3V_S5 — R4005 100KR2J-4-GP — VCCST_OVERRIDE_G — Q4001 2N7002K-2-GP-U — R4006 100KR2J-4-GP — VCCST_OVERRIDE_3D3V
VCCST_OVERRIDE — Q4002 LSI1012LT1G-GP
084.01012.0031
VGS(th)= 0.9V(max)
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31
VGS(th)= 2.5V(max)
VGS(th)= 2.0V(max)
VGS(th)= 2.1V(max)

1D8V_S0

Q4004 FJA3413-1-GP
084.03413.0031
2nd = 084.02301.0031
1D8V_S5 — C4044 SCD1U16V2KX-L-GP — R4034 10KR2J-L-GP — C4045 SC1U10V2KX-L1-GP — R4035 20KR2J-L3-GP — 1D8V_EN# — 1D8V_S0
For CODEC 0.2A
C4046 Do Not Stuff
PM_SLP_S3# — Q4003 2N7002K-2-GP-U — 1D8V_EN#
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

Layout Note:
Close to CPU Side

VccST

VccST 0.5A
1D05V_S5_OUT — U4002 — 1D05V_VCCST_R — R4026 D01R3F-L-GP — 1D05V_VCCST
PM_SLP_S3# — D4004 BAT54C-12-GP
VCCST_OVERRIDE_3D3V
5V_S5 — VCCST_EN — R4004 100KR2J-4-GP — C4002 SC1U10V2KX-L-GP
VBIAS ON — GND — C4003 SC1U10V2KX-L1-GP
G5027CRD1D-GP-U
074.05027.0B93
2nd = 074.05201.0A93
6A
Rds(on): 6.5mΩ
TON: 8us
6A
Rds(on): 7.8mΩ (Max)
TON: 25~40us
75.00054.A7D
2nd = 075.00054.0B7D
3rd = 075.00054.T7D

Layout Note:
Close to CPU Side

VccSTG

VccSTG 0.3A
1D05V_S5_OUT — U4005 — 1D05V_VCCSTG_R — R4028 D01R2J-L-GP — 1D05V_VCCSTG
CPU_C10_GATE# — D4003 BAT54C-12-GP
VCCST_OVERRIDE_3D3V
5V_S5 — VCCSTG_EN — R4029 Do Not Stuff — VCCSTG_EN_R — R4015 100KR2J-4-GP — C4009 SC1U10V2KX-L1-GP
VBIAS ON — GND — C4010 SC1U10V2KX-L1-GP
G5027CRD1D-GP-U
074.05027.0B93
2nd = 074.05201.0A93
6A
Rds(on): 6.5mΩ
TON: 8us
6A
Rds(on): 7.8mΩ (Max)
TON: 25~40us
75.00054.A7D
2nd = 075.00054.0B7D
3rd = 075.00054.T7D

PWR_3D3V_PG — R4031 Do Not Stuff — PWR_1D8V_EN
PM_SLP_SUS# — R4030 Do Not Stuff
C4022 Do Not Stuff

BYPASS

VCCIN_AUX_PWRGD — R4010 0R2J-L-GP — PWR_VNN_EN
R4011 10KR2J-L-GP — PWR_1D05V_EN — C4004 SC1U16V2KX-3DX-GP
PM_SLP_S3# — R4012 0R2J-L-GP
VNN_CTRL — R4013 Do Not Stuff — PWR_VNN1D05V_VID1
V1P05_CTRL — R4014 0R2J-L-GP — PWR_VNN1D05V_VID2

Follow CRB
Document Number: 612304 Ver 1.0

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (Power Plane Enable)
Size: A2
Document Number: A34_TGL
Rev: SIT
Date: Monday, November 16, 2020
Sheet 40 of 106

15 SKUD UMA S16G SIT

緯創資通

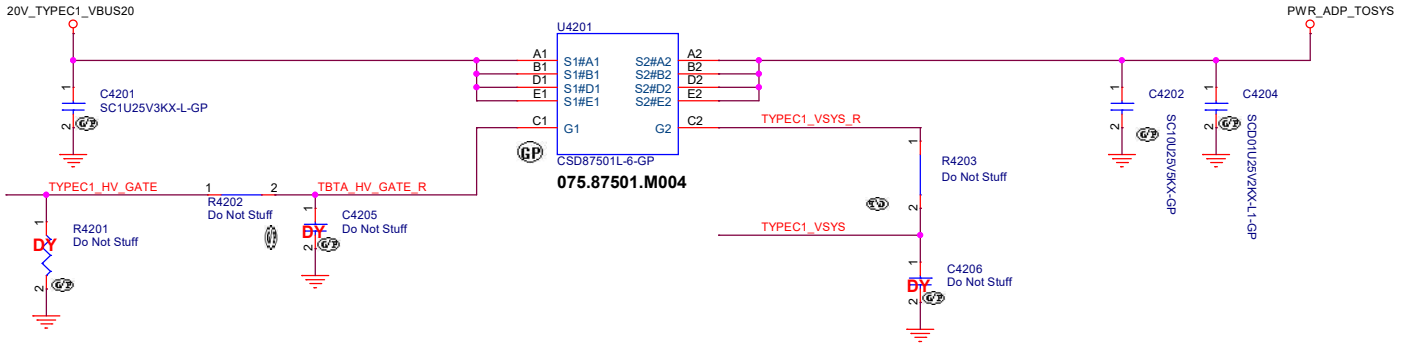
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

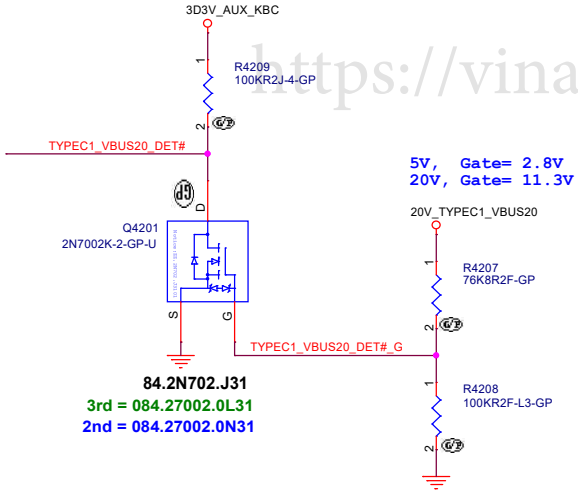
Title: ***RSVD***		
Size: A4	Document Number: **A34_TGL**	Rev: **SIT**
Date: Monday, November 16, 2020	Sheet 41 of 106	

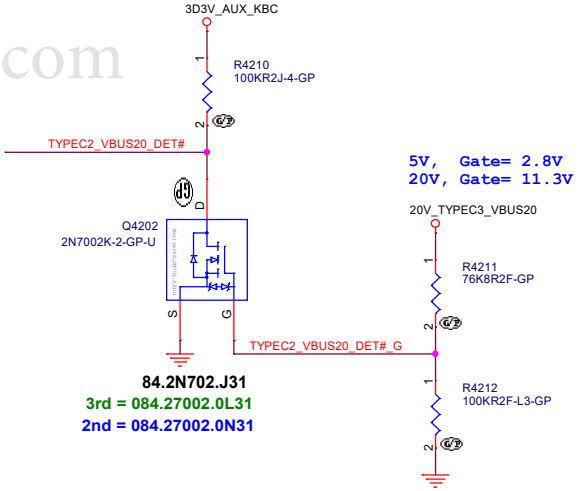
72 TYPEC1_HV_GATE

24 TYPEC1_VBUS20_DET#
24 TYPEC2_VBUS20_DET#

72 TYPEC1_VSYS







15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 042_INT IO (TYPEC DC-DC)

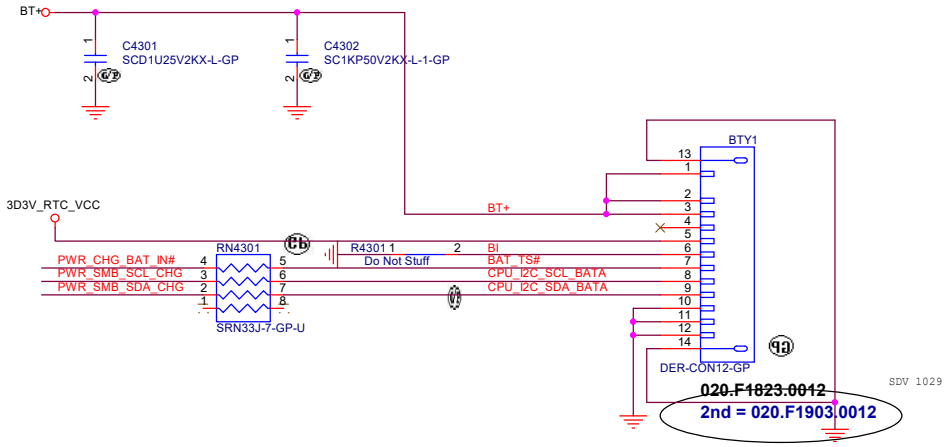
Size: A3 | Document Number: A34_TGL | Rev: SIT

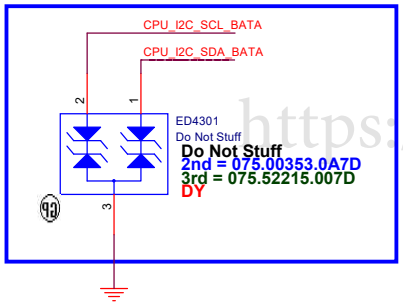
Date: Monday, November 16, 2020 | Sheet 42 of 106

BATTERY CONNECTOR

24,44 PWR_SMB_SCL_CHG
24,44 PWR_SMB_SDA_CHG
24 PWR_CHG_BAT_IN#

89 BI
89 BAT_TS#
89 CPU_I2C_SCL_BATA
89 CPU_I2C_SDA_BATA





15 SKUD UMA S16G SIT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (DC IN/BAT CON)**

Size: Custom | Document Number: **A34_TGL** | Rev: **SIT**

Date: Monday, November 16, 2020 | Sheet 43 of 106

OFFPAGE - PIC - EE

For 95W/135W Adapter : PZ0703EK/AONS21309C

PH on EE Side

PH on EE Side

Device will be transition from normal Buck-Boost operation to PTM operation by:
- Set REG0x21[7] = 0, to disable the EN_EXITILIM.
- Set REG0x20[6] = 1
- Set REG0x28[2:1] = 1
- Ground ILIM_HIZ pin

Device will transition out of PTM mode with host control by:
- Set REG0x28[2:1] = 0
- Pull ILIM_HIZ pin to high
- Device exits PTM into buck-boost operation if tripping VinDPM or IinDPM
- Device exits PTM into buck-boost operation under fault conditions (ACOC, TSHUT, BATOC).

VAT support for BQ25710

	VCLIM	PR423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

Reserve for Power test

1st = 074.25710.M003

84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

0505
buyer: 7"

Reserve for PTM
If it hasn't more GPIO

# of CELL	VCELL_PRE	PR415
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

1st = 76.27002.F7C
2nd = 076.27002.0E7C
3rd = 076.67002.007C

Do Not Stuff
2nd = 084.27002.0N31
3rd = 084.27002.0L31

15 SKILD UMA 516G SIF

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

BQ25710R_Charger

Size: A3 | Document Number: A34_TGL | Rev: SIT

Date: Monday, November 16, 2020 | Sheet 44 of 56

OFFPAGE-Signal

40 PWR_3D3V_EN >> PWR_3D3V_EN

PH on EE Side

40 PWR_3D3V_PG >> PWR_3D3V_PG

24 PWR_5V_EN >>

OFFPAGE-GAP

19V_DCBATOUT PWR_DCBATOUT_3D3V

PG4501 Do Not Stuff 1 2 GP
PG4502 Do Not Stuff 1 2 GP
PG4503 Do Not Stuff 1 2 GP
PG4504 Do Not Stuff 1 2 GP

3D3V_S5 PWR_3D3V

PG4505 Do Not Stuff 2 1 GP
PG4506 Do Not Stuff 2 1 GP
PG4507 Do Not Stuff 2 1 GP
PG4508 Do Not Stuff 2 1 GP
PG4509 Do Not Stuff 2 1 GP
PG4510 Do Not Stuff 2 1 GP
PG4511 Do Not Stuff 2 1 GP
PG4512 Do Not Stuff 2 1 GP

3D3V_AUX_S5 PWR_3D3V_LDO

PG4527 Do Not Stuff 2 1 PWR_3D3V_LDO GP

19V_DCBATOUT PWR_DCBATOUT_5V

PG4552 Do Not Stuff 1 2 GP
PG4553 Do Not Stuff 1 2 GP
PG4555 Do Not Stuff 1 2 GP
PG4557 Do Not Stuff 1 2 GP
PG4559 Do Not Stuff 1 2 GP
PG4561 Do Not Stuff 1 2 GP

5V_S5 PWR_5V

PG4551 Do Not Stuff 2 1 GP
PG4554 Do Not Stuff 2 1 GP
PG4556 Do Not Stuff 2 1 GP
PG4558 Do Not Stuff 2 1 GP
PG4560 Do Not Stuff 2 1 GP
PG4563 Do Not Stuff 2 1 GP
PG4564 Do Not Stuff 2 1 GP
PG4566 Do Not Stuff 2 1 GP

5V_AUX_S5 PWR_5V_LDO

PG4565 Do Not Stuff 2 1 PWR_5V_LDO GP

PWR_DCBATOUT_3D3V

PC4501 DY Do Not Stuff
PC4502 SC10U25V3MX-9-GP DY
PC4503 Do Not Stuff DY

PR4501 Do Not Stuff
PC4506 SCD1U25V2KX-L-GP
PWR_3D3V_BOOT 1 2 PWR_3D3V_BOOT_A 1

PU4501
IN#2 IN#3 IN#4 IN#5
LX#6 LX#19 LX#20
PWR_3D3V_PH
PWR_3D3V_PG
NC#10 NC#15 NC#16
EN1 EN2
PWR_3D3V_EN 12
PWR_3D3V_EN2 11
BS PG FF OUT LDO
PWR_3D3V_BOOT 1
PWR_3D3V_PG 9
PWR_3D3V_FB 13
GND GND GND GND
7 8 18 21
SY8288BRAC-GP
PWR_3D3V_LDO

PL4501 IND-1D5UH-23-GP-U

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

IDC:8A
OCP: 11.51 ~ 15.51A

PWR_3D3V
PC4509 PC4510 PC4511 DY PC4513 DY PC4512 Do Not Stuff
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP

PR4514 1MR2J-1-GP
PR4509 499KR2F-1-GP
PR4508 499KR2F-1-GP
PR4505 100KR2J-1-GP
PC4508 Do Not Stuff DY
PC4507 SC4D7U6D3V3KX-L-GP
PC4521 SC1KP50V2KX-L-1-GP
PR4506 1KR2F-3-GP
PG4528 Do Not Stuff

19V_DCBATOUT
3D3V_AUX_S5
PWR_3D3V_VOUT
PWR_3D3V_FB2

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A

Trace used 10 mil

Place another side , make GND plan bigger

5V_AUX_S5

PR4552 Do Not Stuff DY

Place another side , make GND plan bigger

PWR_DCBATOUT_5V

PC4552 PC4554 PC4555 Do Not Stuff DY
SC10U25V2KX-L-GP

PU4551
IN#2 IN#3 IN#4 IN#5
PG BS LX#6 LX#19 LX#20 OUT FF LDO
PWR_5V_PG 9
PWR_5V_BOOT 1
PWR_5V_PH
PWR_5V_VOUT
PWR_5V_FB 13
PWR_5V_LDO 15
NC#10 NC#16
VCC
EN1 EN2
PWR_5V_VCC 17
PWR_5V_EN 12
PWR_5V_EN2 11
GND GND GND GND
7 8 18 21
SY8288CRAC-GP

PR4554 Do Not Stuff
PC4553 SCD1U25V2KX-L-GP
PL4551 IND-1D5UH-23-GP-U

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

IDC:8A
OCP: 12.05 ~ 16.05A

PWR_5V
DY PC4565 Do Not Stuff
PC4556 PC4557 PC4558 PC4559 PC4560 PC4561
2Cell 2Cell
For 2cell use
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP

PG4562 Do Not Stuff

PC4562 SC2D2U10V3KX-L-GP
PR4556 1MR2J-1-GP
PR4557 499KR2F-1-GP
PR4558 499KR2F-1-GP Do Not Stuff
PC4564 DY
PC4563 SC1KP50V2KX-L-1-GP
PR4555 1KR2F-3-GP
PC4551 SC4D7U6D3V3KX-L-GP

For 2cell use

Trace used 10 mil

1st = 074.08288.0B43
2nd = 074.05068.0043

19V_DCBATOUT
PWR_5V_VOUT
PWR_5V_FB_A
PWR_5V_LDO

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A

Place another side , make GND plan bigger

5V_S5 3D3V_S5 PWR_DCBATOUT_3D3V PWR_DCBATOUT_5V

D4501 DY Do Not Stuff
D4502 DY Do Not Stuff
D4503 DY Do Not Stuff
D4504 DY Do Not Stuff

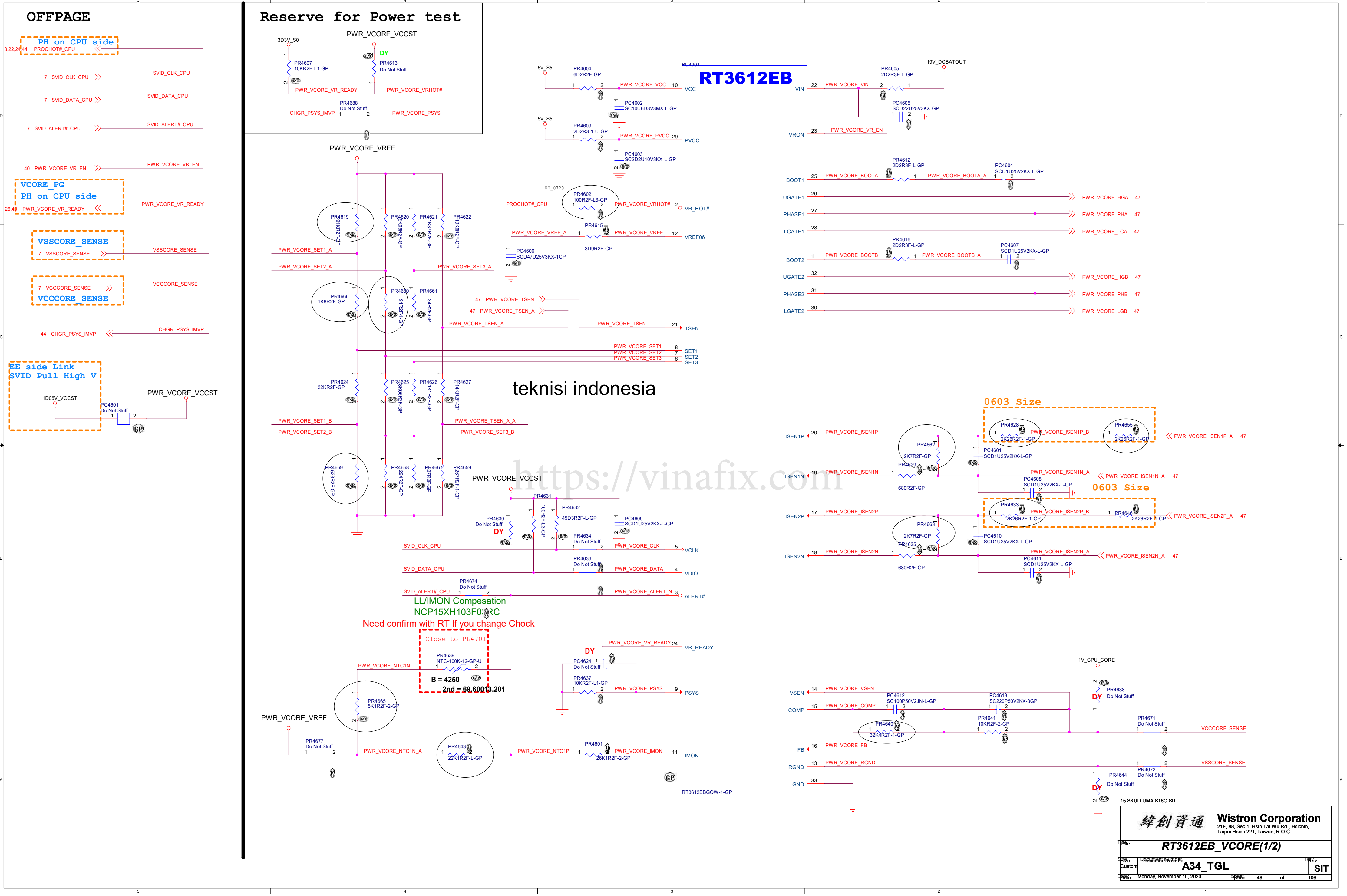
15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8288C&SY8288B_5V3D3V

Size: Custom | Document Number: A34_TGL | Rev: SIT

Date: Monday, November 16, 2020 | Sheet 45 of 106



OFFPAGE
PH on CPU side
PROCHOT#_CPU
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT#_CPU
PWR_VCORE_VR_EN
VCORE_PG
PH on CPU side
PWR_VCORE_VR_READY
VSSCORE_SENSE
VCCCORE_SENSE
CHGR_PSYS_IMVP
EE side Link
SVID Pull High V
1D05V_VCCST
PG4601
Do Not Stuff
PWR_VCORE_VCCST
Reserve for Power test
3D3V_S0
PR4607
10KR2F-L1-GP
PR4613
Do Not Stuff
DY
PWR_VCORE_VRHOT#
PR4688
Do Not Stuff
PWR_VCORE_PSYS
PWR_VCORE_VREF
RT3612EB
PU4601
VCC
PVCC
VR_HOT#
VREF06
TSEN
SET1
SET2
SET3
VCLK
VDIO
ALERT#
VR_READY
PSYS
IMON
VIN
VRON
BOOT1
UGATE1
PHASE1
LGATE1
BOOT2
UGATE2
PHASE2
LGATE2
ISEN1P
ISEN1N
ISEN2P
ISEN2N
VSEN
COMP
FB
RGND
GND
RT3612EBGQW-1-GP
19V_DCBATOUT
5V_S5
PWR_VCORE_HGA
PWR_VCORE_PHA
PWR_VCORE_LGA
PWR_VCORE_HGB
PWR_VCORE_PHB
PWR_VCORE_LGB
0603 Size
PWR_VCORE_ISEN1P_A
PWR_VCORE_ISEN1N_A
PWR_VCORE_ISEN2P_A
PWR_VCORE_ISEN2N_A
teknisi indonesia
LL/IMON Compesation
NCP15XH103F03RC
Need confirm with RT If you change Chock
Close to PL4701
PR4639
NTC-100K-12-GP-U
B = 4250
2nd = 69.60013.201
1V_CPU_CORE
15 SKUD UMA S16G SIT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RT3612EB_VCORE(1/2)
Size
Custom
Document Number
A34_TGL
Rev
SIT
Date: Monday, November 16, 2020
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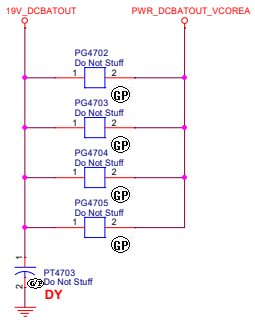
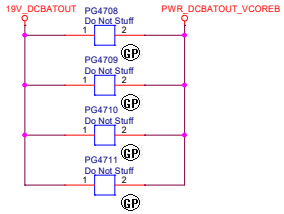
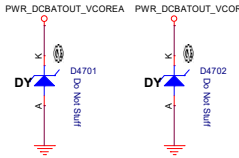
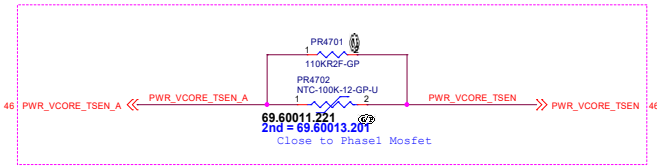
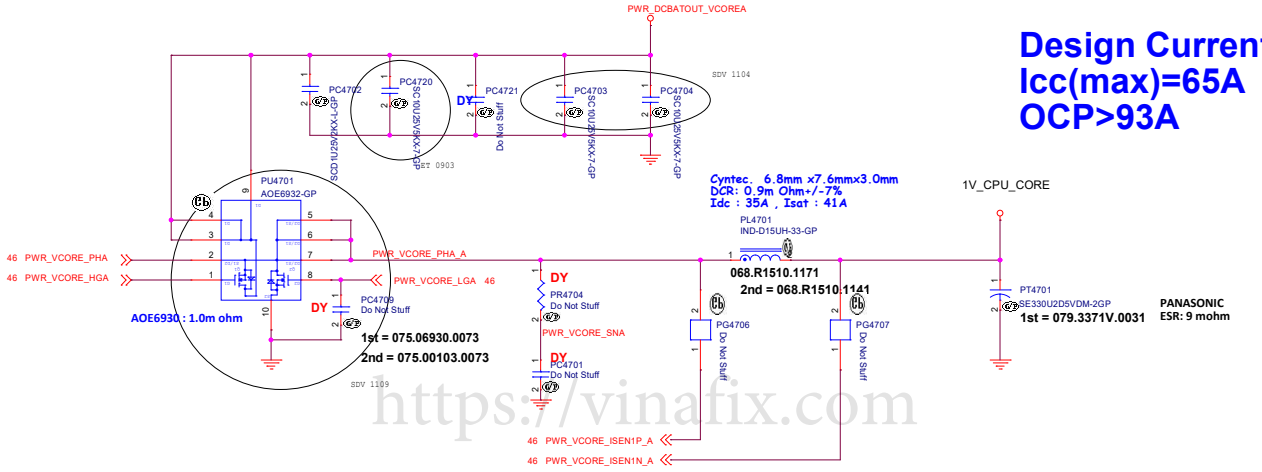
OFFPAGE











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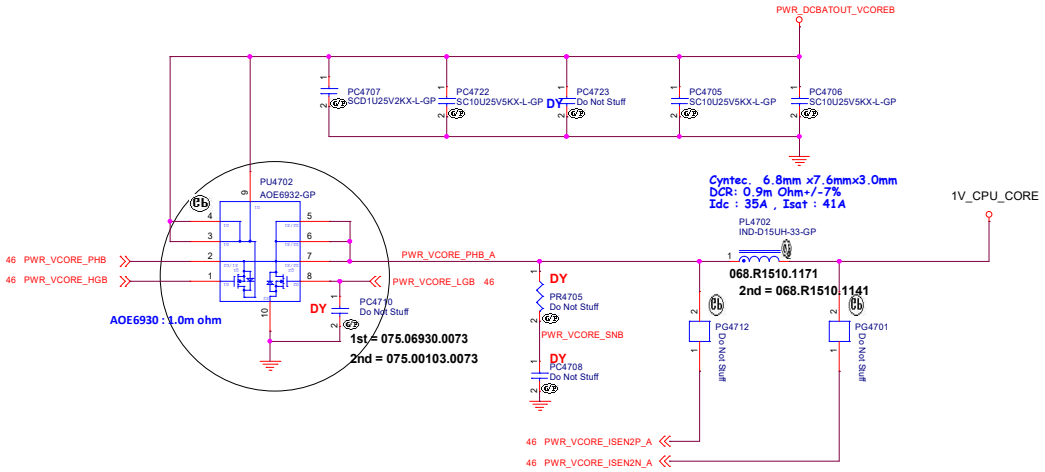
OCP>93A



15 SKUD UMA S16G SIT

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT3612EB_VCORE(2/2)
Size: Custom	Document Number: A34_TGL
Rev: SIT	
Date: Monday, November 16, 2020	Sheet 47 of 106

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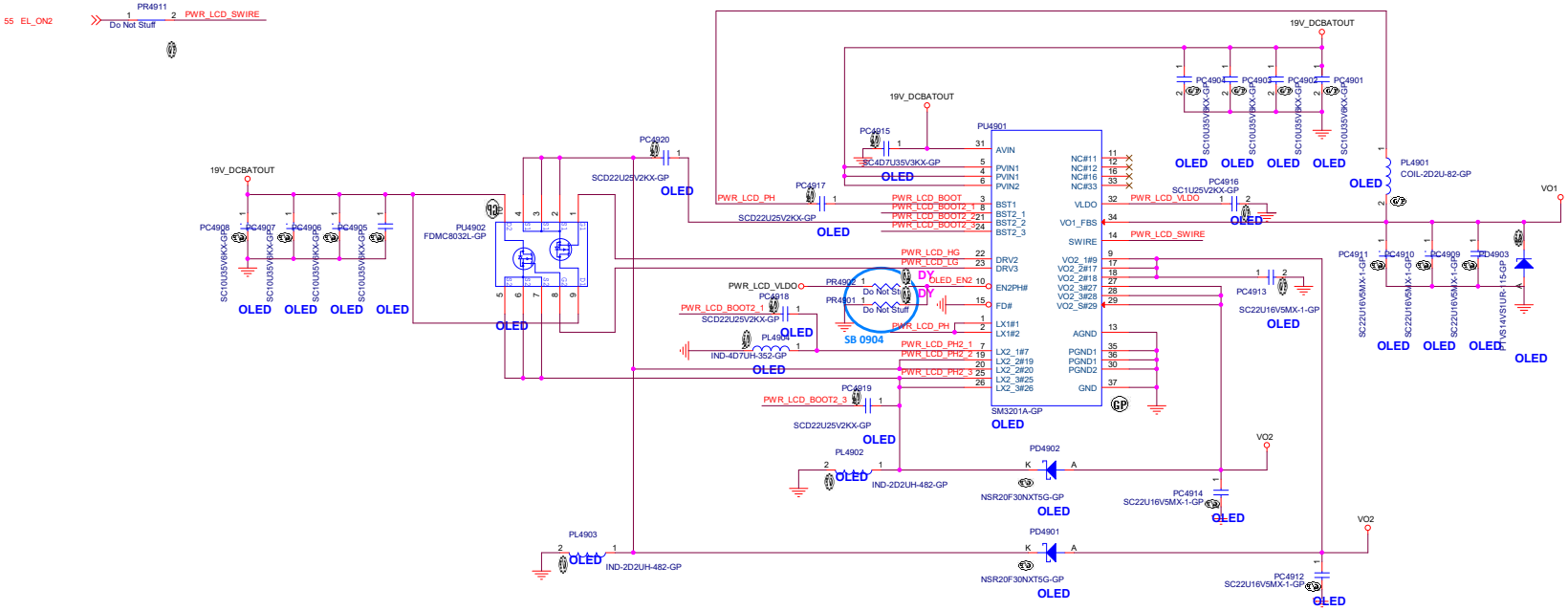
15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER (RSVD)		
Size: A	Document Number: A34_TGL	Rev: SIT
Date: Monday, November 16, 2020	Sheet 48 of 106	



Vinafix.com

15 SKUD UMA S16G SIT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 049_Power (LCD_SM3201A)

Size	Document Number	Rev
A2	A34_TGL	SIT

Date: Monday, November 16, 2020 Sheet 49 of 106

OFFPAGE

PH on EE Side

40 VCCIN_AUX_PWRGD — PRS003 Do Not Stuff — PWR_VCCAUX_PG

PH on CPU side

22 VCCIN_AUX_VID1 — VCCIN_AUX_VID1

22 VCCIN_AUX_VID0 — VCCIN_AUX_VID0

VCCAUX_SENSE

22 VCCAUX_SENSE — VCCAUX_SENSE

22 VSSAUX_SENSE — VSSAUX_SENSE

VSSAUX_SENSE

53 PWR_VCCAUX_EN — PWR_VCCAUX_EN

OFFPAGE_GAP

19V_DCBATOUT — PGS001 Do Not Stuff — PWR_DCBATOUT_VCCAUX

PGS002 Do Not Stuff

PGS003 Do Not Stuff

PGS004 Do Not Stuff

VCCIN_AUX_VID1 — PRS034 Do Not Stuff — PWR_VCCAUX_VID1

VCCIN_AUX_VID0 — PRS035 Do Not Stuff — PWR_VCCAUX_VID0

1D8V_VCCIN_AUX — PRS017 Do Not Stuff

VCCAUX_SENSE

VSSAUX_SENSE — PRS018 Do Not Stuff

PWR_DCBATOUT_VCCAUX — D5001 1N4 SHUT

OCP : 41.6A

PRS004 — 178KR2F-GP — PWR_VCCAUX_CS_DIS

5V_S5 — PRS001 SD1R2J-1-GP — PC5001 SC100U6X0KX-L1-GP

3D3V_S5 — PRS002 Do Not Stuff — PWR_VCCAUX_PVCC

PRS003 100KR2F-L1-GP — PWR_VCCAUX_VCC

PWR_VCCAUX_PG

PWR_VCCAUX_EN

PWR_VCCAUX_VID1

PWR_VCCAUX_VID0

PRS005 Do Not Stuff — DY

PRS006 Do Not Stuff — DY

HI = 800KHz
Flot = 600KHz
Low = 400KHz

PWR_VCCAUX_FSWEL

PUS001 RT6543AGQW-GP

CS_DIS, PVCC, VCC, PG, EN, VID1, VID0, FSWSEL, AGND, BOOT, VSYS, UG, PH, LG, PGND, ISENSEP, ISENSEN, VOUT, COMP, FB, RGND

074.06543.0073

PWR_VCCAUX_BOOT — PRS007 Do Not Stuff — PWR_VCCAUX_BOOTA — PCS003 SCD1U25V2KX-GP

PRS033 DRSJJ-0-GP — PCS004 SCD1U25V2KX-GP — PWR_VCCAUX_VSYS — PWR_DCBATOUT_VCCAUX

PWR_VCCAUX_HG

PWR_VCCAUX_PH

PWR_VCCAUX_LG

PUS002 FDMS3600-G2-R.JK0215-COLAY-GP

1st = 075.00046.0073
2nd = 075.00019.0A73

PWR_VCCAUX_ISENSEP

PWR_VCCAUX_ISENSEN

PWR_VCCAUX_VOUT — PRS012 0R3F-1-GP-U — PWR_VCCAUX_VOUTA

PWR_VCCAUX_COMP — PCS010 SC22P50V2KX-1-GP — PWR_VCCAUX_COMPA — PRS013 10KR2F-2-GP

PCS011 DY — PWR_VCCAUX_COMPB — PRS014 Do Not Stuff

PCS012 SC22P50V2JN-4GP — PRS015 5K62R2F-GP

PWR_VCCAUX_FB

19_08_05 PCS010: 100P50V_0402 -> 2k2P50V_0402
PCS012: 10P50V_0402 -> 22P50V_0402

19_08_05 PRS011: 0R5014 -> DY

19_08_05 PRS015: 13k_0402 -> 5.62k_0402

VSSAUX_SENSE

VCCAUX_SENSE

PRS016 0R2F-1-GP

PCS013 Do Not Stuff — DY

PWR_DCBATOUT_VCCAUX

EZ0903

PCS006 SCD1U25V2KX-GP — PCS007 SCD1U25V2KX-GP — PCS008 SCD1U25V2KX-GP — PCS009 SCD1U25V2KX-GP

68.R2210.10V
6.8mm x 7.3mm x 3.0mm
DCR: 2.5 ~ 2.8 mOhm
Idc : 23A , Isat : 40A

Iccmax= 27A
TDC=14A

PL5001 IND-D22UH-37-GP — 68.R2210.10V
2nd = 068.R2210.1141

1D8V_VCCIN_AUX

PWR_VCCAUX_PH

PCS005 Do Not Stuff

PCS006 — PT5001_PT5002 SCD1U25V2KX-1-GP — DY

PWR_VCCAUX_ISENSEP_A

PRS008 5K36R2F-GP

PCS005 SCD1U25V2KX-GP

PRS009 267R2F-1-GP

PRS010 845R2F-GP

Close to IC

PWR_VCCAUX_NTC

PRS011 NTC-10K-2-GP-U

2nd = 69.60013.131
10KF / B=3370K

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCAUX

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OFFPAGE

S5
17,24 PM_SLP_S4# PR5115 1 2 PWR_VDDQ_EN Do Not Stuff

S3
5 VTT_CNTL PR5114 1 2 PWR_VTT_EN Do Not Stuff

PH on EE Side
40 PWR_VDDQ_PG PWR_VDDQ_PG

OFFPAGE_GAP

19V_DCBATOUT PG5101 Do Not Stuff PWR_DCBATOUT_VDDQ
PG5102 Do Not Stuff
PG5103 Do Not Stuff

1D2V_S3 PG5105 Do Not Stuff PWR_VDDQ
PG5106 Do Not Stuff
PG5107 Do Not Stuff
PG5108 Do Not Stuff
PG5109 Do Not Stuff
PG5110 Do Not Stuff
PG5112 Do Not Stuff
PG5114 Do Not Stuff

1D2V_S3 PG5115 Do Not Stuff PWR_VDDQ_VLDOIN

0D6V_VREF_S0 PG5111 Do Not Stuff PWR_VDDQ_VTT

3D3V_S5 PG5119 Do Not Stuff PWR_VDDQ_V3V

2D5V_S3 PG5118 Do Not Stuff PWR_VDDQ_V2P5

PWR_DCBATOUT_VDDQ
D5101 Do Not Stuff

PC5104因為layout關係所以直接下PGND即可
獨立下地並遠離NOISE

5V_S5 PR5101 Do Not Stuff
PR5108 620KR2F-GP
PWR_VDDQ_PH PWR_VDDQ_TON PWR_VDDQ_VCC
PWR_VDDQ_V3V
PWR_VDDQ_AGND
PC5104 SC1U10V2KX-L1-GP
PC5117 SC1U10V2KX-L1-GP
3D3V_S5
R5104 Do Not Stuff
DY
Do Not Stuff
PC5102
If 5V has droop
Please mount it

PU5101
TON VCC GND V3V BST LX#12 LX#11 LX#10 LX#9 LX#32 V2P5 PGOOD VLODIN VTT VTTGND VTTSNS VTTREF PGND VDDQSNS VDDQSET
G5416QS1U-GP
074.05416.0073

PWR_VTT_EN PWR_VDDQ_EN
PWR_VDDQ_PG
PWR_VDDQ_VLDOIN
PWR_VDDQ_VTT
PWR_VDDQ_VTTSNS
PWR_VDDQ_VTTREF
PC5118 SC10U6D3V3MX-L-GP
PC5111 PC5112 Do Not Stuff SC10U6D3V3MX-L-GP
PC5114 SCD1U16V2KX-L-GP
PG5120 Do Not Stuff
PR5112 Do Not Stuff
PWR_VDDQ_AGND

PWR_DCBATOUT_VDDQ
PC5101 SC100U25V3KX-7-GP
PC5105 SC10U25V5KX-GP
PR5111 Do Not Stuff
PWR_VDDQ_BOOT
PC5110 SCD1U25V2KX-L-GP
Cyntec 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A
PL5101 COIL-1UH-34-GP-U1
TDC : 8A
PWR_VDDQ_PH
PWR_VDDQ_V2P5
PC5116 SC10U6D3V3MX-L-GP
PR5110 Do Not Stuff
PC5115 Do Not Stuff
PR5113 Do Not Stuff
PG5104 Do Not Stuff
PWR_VDDQ_SNS
PC5106 PC5107 PC5109 PC5113
SC22U6D3V3MX-L1-GP
Close to PC5113
PWR_VDDQ_VDDQSET_A
PR5105 6K2R2F-GP
PC5124 Do Not Stuff
R1
R2
PR5106 10K2R2F-GP
PWR_VDDQ_VDDQSNS
PWR_VDDQ_VDDQSET
Vout= 0.75*(1+R1/R2) = 1.2
PWR_VDDQ_AGND

15 SKUD UMA S16G SIT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G5416Q_VDDQ
Size: A2
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15 SKUD UMA S16G SIT

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RSVD)***

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OFFPAGE

40 PWR_1D8V_EN

50 PWR_VCCAUX_EN

PR5307 Do Not Stuff

OFFPAGE_GAP

19V_DCBATOUT PWR_DCBATOUT_1D8V

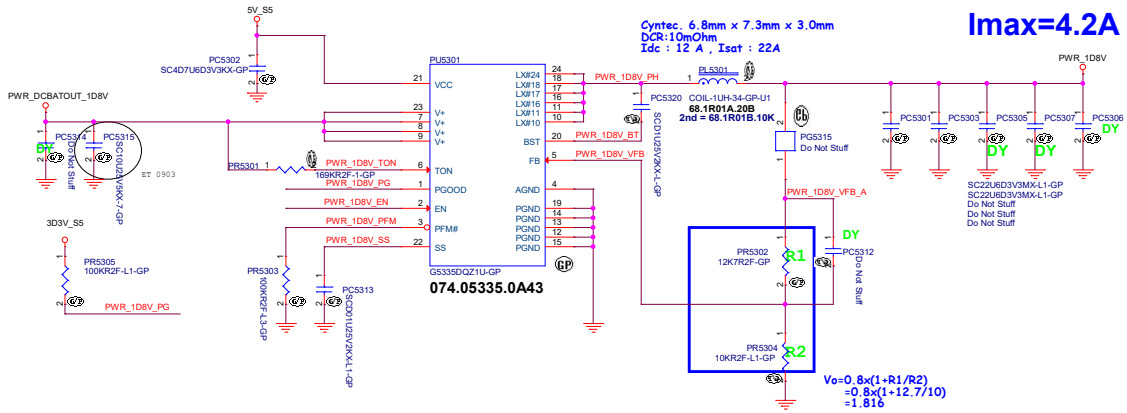
PG5301 Do Not Stuff
PG5302 Do Not Stuff
PG5303 Do Not Stuff

PWR_1D8V 1D8V_S5

PG5304 Do Not Stuff
PG5305 Do Not Stuff
PG5318 Do Not Stuff
PG5320 Do Not Stuff
PG5321 Do Not Stuff

SSID = PWR.Plane.Regulator_1p0v

G5335D for 1D8V



15 SKUD UMA S16G SIT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G5335D_1D8V		
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OFFPAGE

PH on EE Side

VCCIN_AUX_PWRGD
40 PWR_VNN_EN → PWR_VNN_EN

40 PWR_1D05V_EN → PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
40 PWR_VNN1D05V_VID2 → PWR_VNN1D05V_VID2

PM_SLP_S3#
40 PWR_VNN1D05V_VID1 → PWR_VNN1D05V_VID1

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

OFFPAGE-GAP

1D05V_VNN_BYPASS — PG5401 Do Not Stuff 1 2 GP — PWR_VNN

1D05V_S5_BYPASS — PG5402 Do Not Stuff 1 2 GP — PWR_1D05V

3D3V_S5 — R5420 1 2 Do Not Stuff PWR_VNN1D05V_PG — DY

Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A

PL5401 IND-1UH-382-GP BYPASS

PC5411 SC22U6D3V3MX-L1-GP
PC5412 SC22U6D3V3MX-L1-GP

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

PL5402 IND-10UH-330-GP BYPASS

PC5414 Do Not Stuff
PR5408 0R2J-L-GP
PR5407 Do Not Stuff
PC5410 SC22U6D3V3MX-L1-GP
PC5413 SC22U6D3V3MX-L1-GP

PC5401 SC1U10V2KX-L1-GP
PR5413 2D2R2J-GP
5V_S5

PC5402 SC4D7U25V5KX-L2-GP
PR5422 Do Not Stuff
PR5410 Do Not Stuff
19V_DCBATOUT
SC4D7U25V5KX-L2-GP

PC5404 SCD1U25V2KX-L-GP
PC5405 SCD1U25V2KX-L-GP
PWR_VNN1D05V_BOOTA_A
PWR_VNN1D05V_BOOTB_A

PC5406 Do Not Stuff — DY

PR5423 0R2F-1-GP PWR_VNN1D05V_PHB
PR5401 0R2F-1-GP PWR_VNN1D05V_PHA

PU5401 APW8743CQBI-TRG-GP
074.08743.0A73

VCC	8	EN1	15 PWR_VNN_EN
VIN1	11	EN2	6 PWR_1D05V_EN
VIN2	10	LX1	1 PWR_VNN1D05V_PHA
VID1	13	LX2	4 PWR_VNN1D05V_PHB
BOOT1	2	VOUT2	5 PWR_VNN1D05V_FB2
BOOT2	3	VOUT1	16 PWR_VNN1D05V_VOUT1
VID2	14	AGND	17
POK	7	PGND	9
		PGND	12

PWR_VNN1D05V_VCC
PWR_VNN1D05V_VINA
PWR_VNN1D05V_VINB
PWR_VNN1D05V_VID1
PWR_VNN1D05V_BOOTA
PWR_VNN1D05V_BOOTB
PWR_VNN1D05V_VID2
PWR_VNN1D05V_PG

PR5419 — PWR_VNN
PR5430 Do Not Stuff — DY

3D3V_S5 3D3V_S5

PR5426 Do Not Stuff — DY — PWR_VNN1D05V_VID1
PR5427 Do Not Stuff — DY — PWR_VNN1D05V_VID2

PR5433 10KR2F-2-GP
PR5428 10KR2F-2-GP

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
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Title: APW8743_ByPASS
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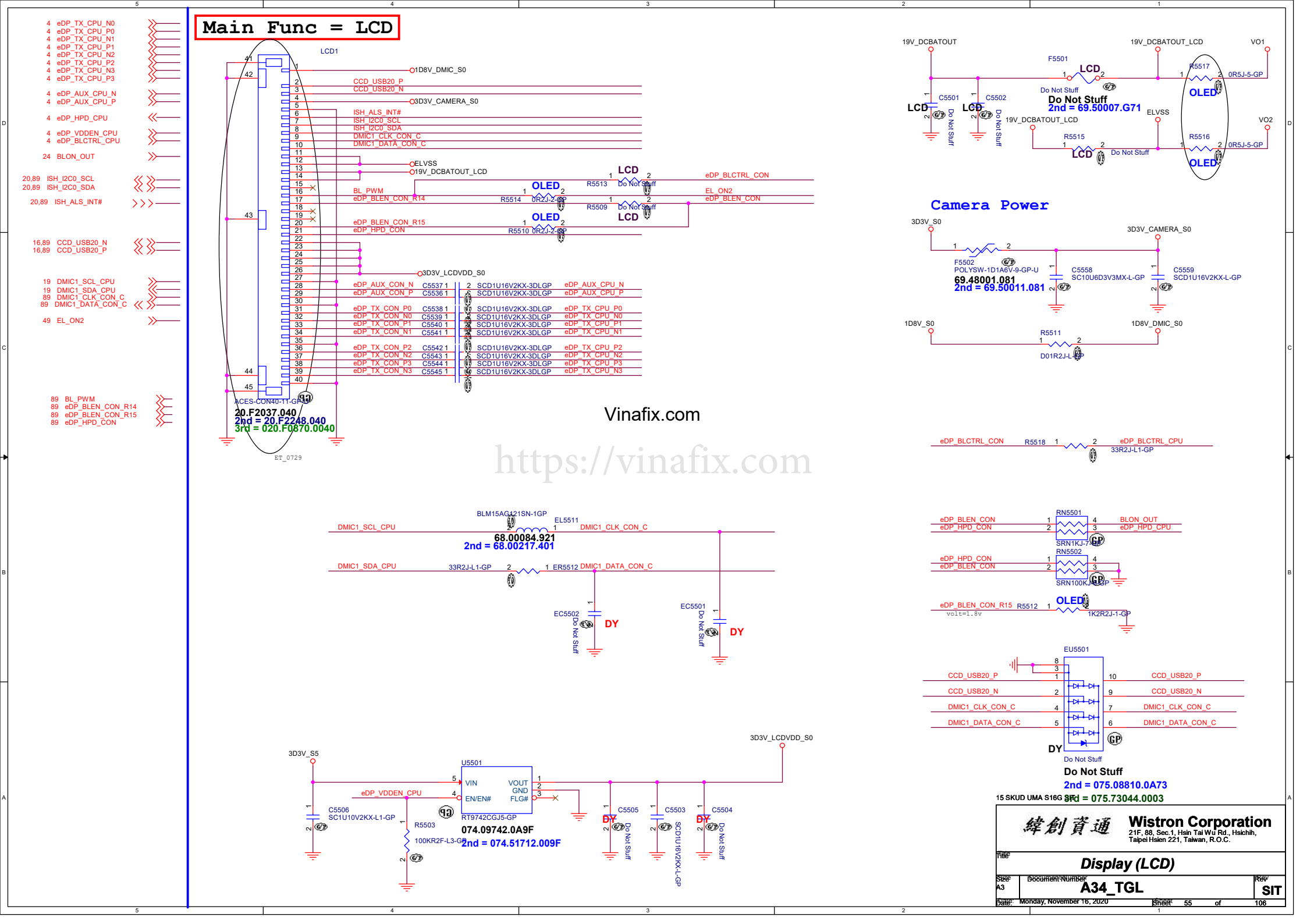
Main Func = LCD



Camera Power

15 SKUD UMA S16G SFF

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (LCD)**

Size	Document Number	Rev
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15 SKUD UMA S16G SIT

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RSVD***		
Size: A3	Document Number: **A34_TGL**	Rev: **SIT**
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15 SKUD UMA S16G SIT

緯創資通

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Title	***RSVD***	
Size A4	Document Number **A34_TGL**	Rev **SIT**
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15 SKUD UMA S16G SIT

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Title: ***RSVD***		
Size: A4	Document Number: **A34_TGL**	Rev: **SIT**
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15 SKUD UMA S16G SIT

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Title: ***RSVD***		
Size: A4	Document Number: **A34_TGL**	Rev: **SIT**
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15 SKUD UMA S16G SIT

緯創資通

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Title: ***RSVD***		
Size: A4	Document Number: **A34_TGL**	Rev: **SIT**
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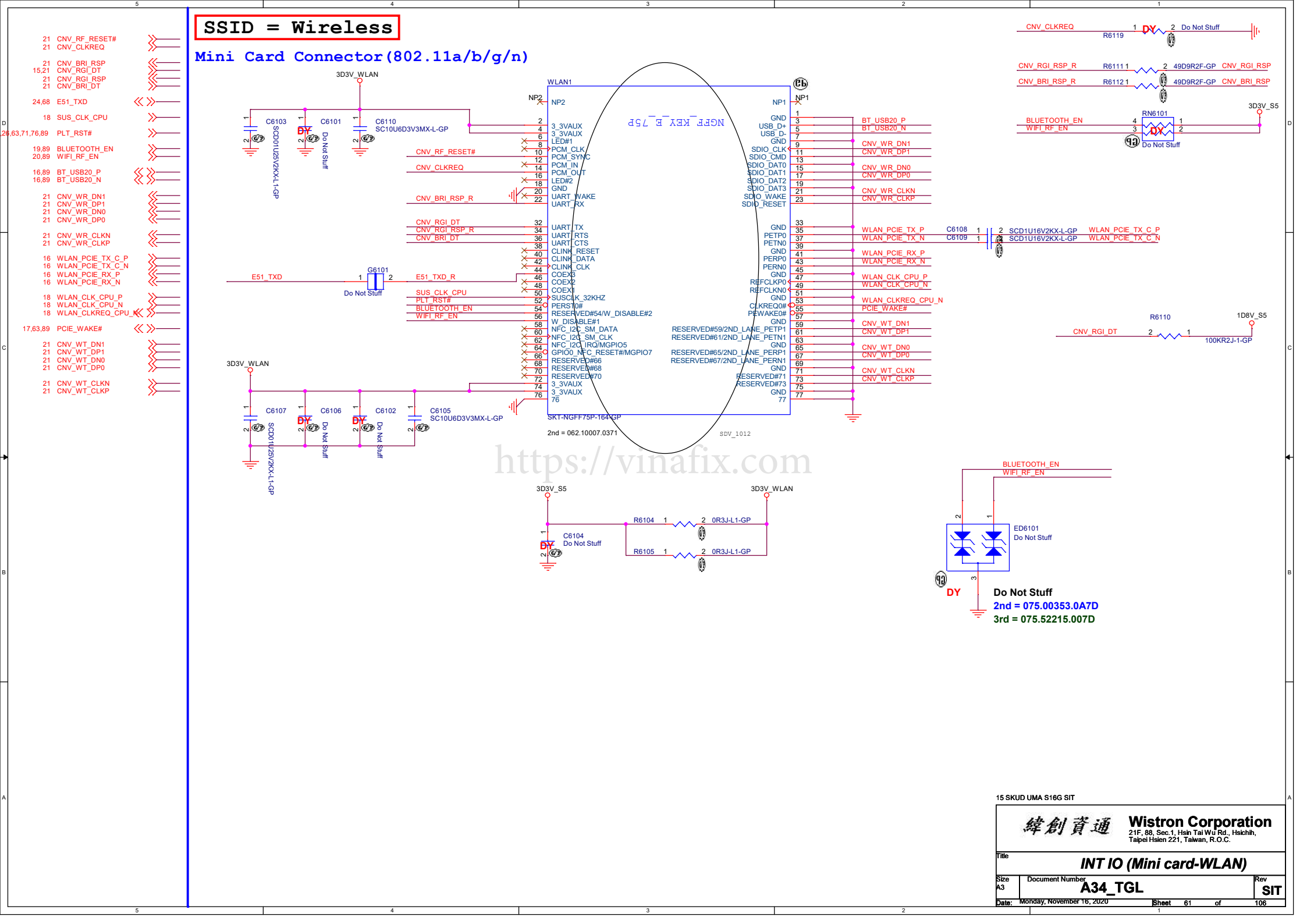
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



15 SKUD UMA S16G SIT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***INT IO (Mini card-WLAN)***
Size A3 / Document Number	**A34_TGL** / Rev **SIT**
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15 SKUD UMA S16G SIT

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***INT IO WWAN***

Size	Document Number	Rev
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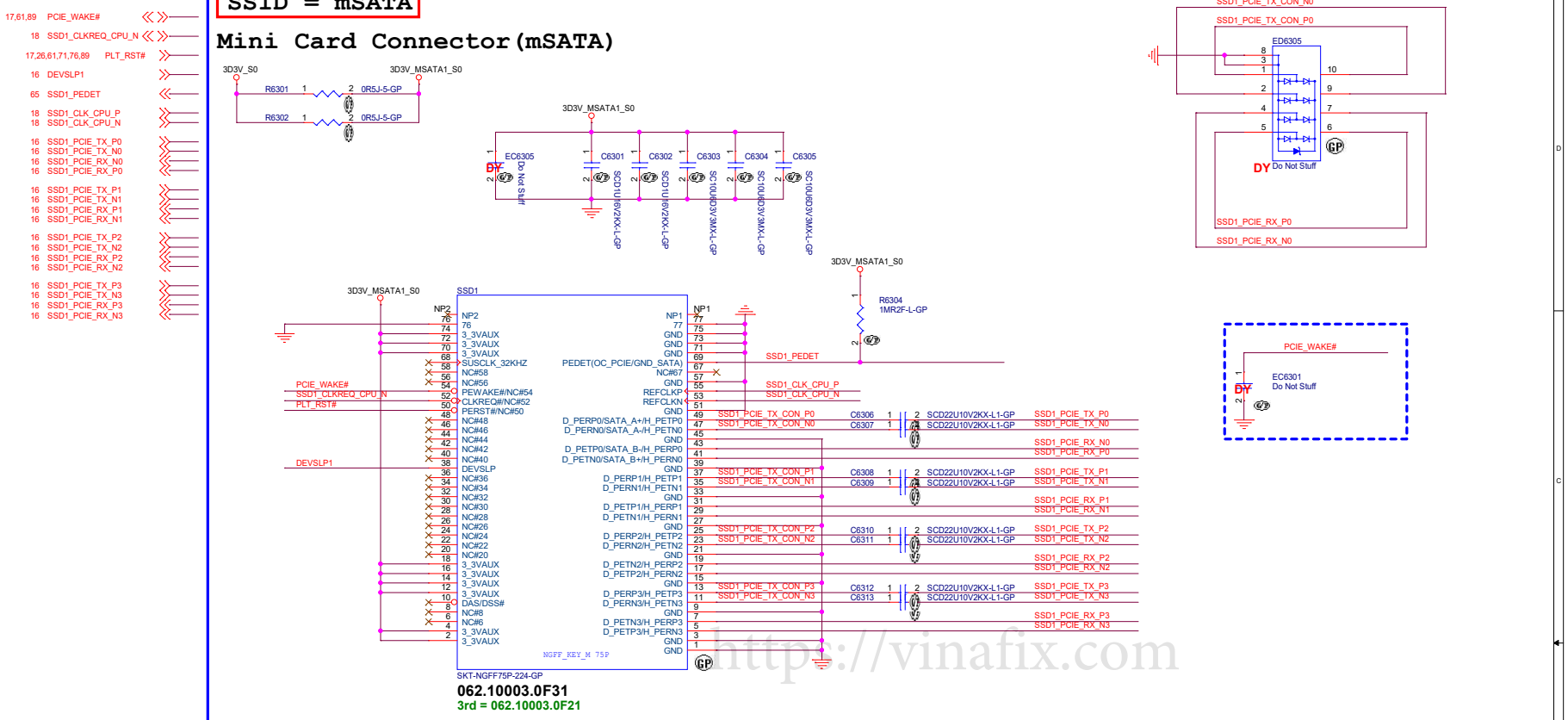
Date: Monday, November 16, 2020 Sheet 62 of 106

SSID = mSATA

Mini Card Connector(mSATA)



062.10003.0F31

3rd = 062.10003.0F21

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Document Number: 575412 Ver 0.9
220 nF nominal capacitors are recommended for Gen 3
100 nF nominal capacitors are recommended for Gen 2

15 SKUD UMA S16G SIT

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title:	INT IO (SSD-NGFF-1)	
Size: Custom	Document Number: A34_TGL	Rev: SIT
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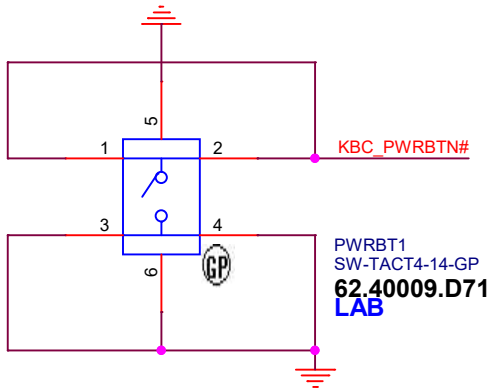
Power Button



24,92 KBC_PWRBTN#

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED / Button / Power Button	
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SSID = KBC

20,89 CPU_I2C_SCL_TP
20,89 CPU_I2C_SDA_TP
3 TP_IN#
24 EC_TP_IN#
24 PTP_PWR_EN
24 FUN_OFF#
24 EC_PSCLK_TP
24 EC_PSDAT_TP
89 CPU_I2C_SDA_TP_CON
89 CPU_I2C_SCL_TP_CON
65,89 EC_TP_IN_R#
63 SSD1_PEDET
16 SATAGP1
89 EC_PSCLK_TP_CON
89 EC_PSDAT_TP_CON
65,89 EC_TP_IN_R#
89 FUN_OFF#_R

3D3V_TP_S3
3D3V_S0
RN6505 SRN2K2J-5-GP
Q6503
L2N7002SDW1T1G-GP
EC6504 Do Not Stuff
EC6505 Do Not Stuff
1st = 75.27002.E7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C

R6502 100KR2F-L3-GP
Q6501
L2N7002SDW3T1G-GP
SATAGP1
SSD1_PEDET
R6503 33R2J-L1-GP
M.2 auto detection
1st = 75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C

RN6503 SRN4K7J-8-GP
R6508 Do Not Stuff
RN6502 SRN33J-5-GP-U
R6507 Do Not Stuff
EC6502 Do Not Stuff
EC6501 Do Not Stuff
EC6503 Do Not Stuff
TP1
HRS-CON12-8-GP
20.K0824.012
2nd = 020.K0339.0012

TOUCH PAD

ED6501 Do Not Stuff
2nd = 075.00353.0A7D
3rd = 075.52215.007D
for TOUCH PAD reserve

3D3V_S5
U6502
RT9742CGJ5-GP
PTP_PWR_EN
C6509 SC1U10V2KX-L1-GP
C6504 SC47U6D3V3MX-GP-U
074.09742.0A9F
2nd = 074.51712.009F

EC6507 Do Not Stuff

CNI	
PIN NO.	PIN DEFINE
1	NC
2	NC
3	GND
4	GND
5	PS/2_CLK
6	PS/2_DATA
7	SCL
8	SDA
9	INT
10	LID_CLOSE
11	VDD_3.3V
12	VDD_3.3V

24,89 KSI[0..7]
24,89 KSO[0..15]
24 KB_BL_PWM
24 KB_BL_DET

Internal KeyBoard Connector

KB1
ACES-CON32-GP
20.K0592.030
CAP_LED_C
5V_S5

Q6505
2N7002K-2-GP-U
24,89 CAP_LED
CAP_LED_C_R
R6505 330R2J-3-GP
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

Internal KeyBoard Connector

KBBL1
ACES-CON4-83-GP
020.K0206.0004
2nd = 020.K0345.0004
KB_BL_DET_R
R6511 100KR2F-L3-GP
KB_BL_DET
KB_LED_PWM_D
R6512 200KR2F-L-3-GP
5V_S0
C6501 Do Not Stuff
Q6504 LSI1012LT1G-GP
KB_BL_PWM
084.01012.0031

A34 K/B

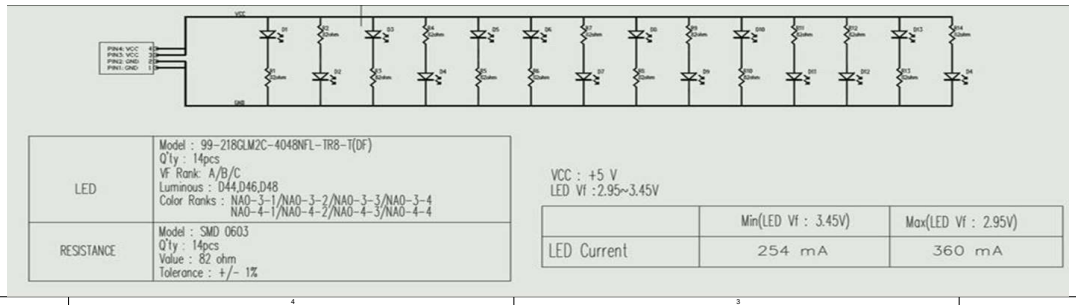
BackLight	
Pin4	P5V0S
Pin3	P5V0S
Pin2	GND
Pin1	GND

Membrane	
Pin1	SCAN_IN<0>
Pin2	SCAN_IN<1>
Pin3	SCAN_IN<2>
Pin4	SCAN_OUT<0>
Pin5	SCAN_OUT<1>
Pin6	SCAN_OUT<2>
Pin7	SCAN_IN<3>
Pin8	SCAN_OUT<3>
Pin9	SCAN_OUT<4>
Pin10	SCAN_OUT<5>
Pin11	SCAN_OUT<6>
Pin12	SCAN_OUT<7>
Pin13	SCAN_OUT<8>
Pin14	SCAN_IN<4>
Pin15	SCAN_OUT<9>
Pin16	SCAN_IN<5>
Pin17	SCAN_IN<6>
Pin18	SCAN_OUT<10>
Pin19	SCAN_OUT<11>
Pin20	SCAN_IN<7>
Pin21	SCAN_OUT<12>
Pin22	SCAN_OUT<13>
Pin23	SCAN_OUT<14>
Pin24	SCAN_OUT<15>
Pin25	N.C.
Pin26	N.C.
Pin27	N.C.
Pin28	CAPS_LED#_3
Pin29	N.C.
Pin30	P5V0S_CAPS

A35 K/B

B/L FPC Pin Define	
PIN4	VCC
PIN3	VCC
PIN2	GND
PIN1	GND

MEM Keyboard Pin Define	
PIN 1	SCAN_IN<0>
PIN 2	SCAN_IN<1>
PIN 3	SCAN_IN<2>
PIN 4	SCAN_OUT<15>
PIN 5	SCAN_OUT<14>
PIN 6	SCAN_OUT<13>
PIN 7	SCAN_IN<3>
PIN 8	SCAN_OUT<12>
PIN 9	SCAN_OUT<11>
PIN 10	SCAN_OUT<10>
PIN 11	SCAN_OUT<9>
PIN 12	SCAN_OUT<8>
PIN 13	SCAN_OUT<7>
PIN 14	SCAN_IN<4>
PIN 15	SCAN_OUT<6>
PIN 16	SCAN_IN<5>
PIN 17	SCAN_IN<6>
PIN 18	SCAN_OUT<5>
PIN 19	SCAN_OUT<4>
PIN 20	SCAN_IN<7>
PIN 21	SCAN_OUT<3>
PIN 22	SCAN_OUT<2>
PIN 23	SCAN_OUT<1>
PIN 24	SCAN_OUT<0>
PIN 25	NC
PIN 26	NC
PIN 27	NC
PIN 28	CAPS_LED#_3
PIN 29	NC
PIN 30	P5V0S_CAPS



LED	Model : 99-218GLM2C-4048NFL-TR8-T(DF) Q'ty : 14pcs VF Rank: A/B/C Luminous : D44,D46,D48 Color Ranks : NA0-3-1/NA0-3-2/NA0-3-3/NA0-3-4 NA0-4-1/NA0-4-2/NA0-4-3/NA0-4-4
RESISTANCE	Model : SMD 0603 Q'ty : 14pcs Value : 82 ohm Tolerance : +/- 1%

VCC : +5 V
LED Vf :2.95~3.45V

	Min(LED Vf : 3.45V)	Max(LED Vf : 2.95V)
LED Current	254 mA	360 mA

15 SKUD UMA S16G SIT

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Title: INT IO (KB/TP)
Size: A2
Document Number: A34_TGL
Rev: SIT
Date: Monday, November 16, 2020
Sheet 65 of 106

SSID = User.Interface

USB

16 USB3_USB20_N
16 USB3_USB20_P

16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P

Audio Jack

27,89 RING2
27,89 AUD_HP1_JACK_L2
27,89 AUD_HP1_JD#
27,89 AUD_HP1_JACK_R2
27,89 SELEEVE

72,89 USB2_PD_CC1
72,89 USB2_PD_CC2

24,89 LID_CLOSE#

24,89 DC_BATFULL
24,89 CHARGE_LED

72,89 USB_SEL

89 USB3_CON_USB20_N
89 USB3_CON_USB20_P

USB3_USB20_N — R6601 1 — 0R2J-2-GP — USB3_CON_USB20_N
USB3_USB20_P — R6602 1 — 0R2J-2-GP — USB3_CON_USB20_P

EU6601 DY

USB2_USB30_TX_P — 8,3,1 — 10 — USB2_USB30_TX_P
USB2_USB30_TX_N — 2 — 9 — USB2_USB30_TX_N
USB2_USB30_RX_P — 4 — 7 — USB2_USB30_RX_P
USB2_USB30_RX_N — 5 — 6 — USB2_USB30_RX_N

Do Not Stuff

Do Not Stuff
2nd = 075.08810.0A73
3rd = 075.73044.0003

EU6602 DY

USB3_CON_USB20_N — 8,3,1 — 10 — USB3_CON_USB20_N
USB3_CON_USB20_P — 2 — 9 — USB3_CON_USB20_P
4 — 7
5 — 6

Do Not Stuff

Do Not Stuff
2nd = 075.08810.0A73
3rd = 075.73044.0003

USB2_PD_CC1 — EU6603 Do Not Stuff — DY
USB2_PD_CC2 — EU6604 Do Not Stuff — DY

IOBD1

3D3V_AUX_S5
LID_CLOSE# — 34
33
32
31
30
AUD_AGND — 29
28
SELEEVE — 27
AUD_HP1_JACK_R2 — 26
AUD_HP1_JD# — 25
AUD_HP1_JACK_L2 — 24
RING2 — 23
22
21
USB2_PD_CC2 — 20
USB2_PD_CC1 — 19
DC_BATFULL — 18
CHARGE_LED — 17
USB_SEL — 16
15
1D8V_S5 — 14
5V_AUX_S5 — 13
12
11
USB2_USB30_RX_N — 10
USB2_USB30_RX_P — 9
8
USB2_USB30_TX_N — 7
USB2_USB30_TX_P — 6
5
4
USB3_CON_USB20_N — 3
USB3_CON_USB20_P — 2
1
36

KYO-CON34-GP

020.K0346.0034
2nd = 020.K0270.0034

20V_TYPEC3_VBUS20

IOBD2

1
2
3
4
5
6
7
8

ACES-CON6-81-GP

020.F1039.0006
2nd = 020.F0283.0006

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Conn (USB/AUDIO)***

Size	Document Number	Rev
Custom	A34_TGL	SIT

Date: Monday, November 16, 2020 Sheet 66 of 106

15 SKUD UMA S16G SIT

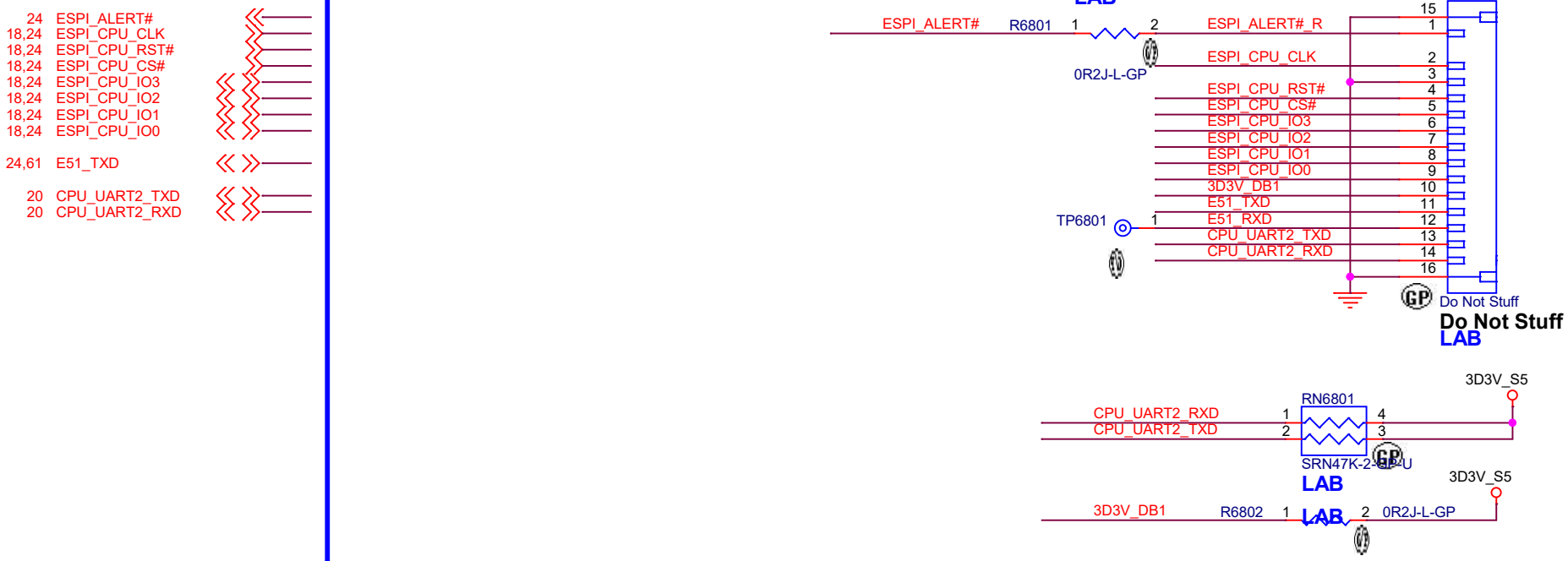
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A	A34_TGL	SIT

Date: Monday, November 16, 2020 Sheet 67 of 106



15 SKUD UMA S16G SIT

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Debug (ESPI Debug)**

Size	Document Number	Rev
A4	A34_TGL	SIT

Date: Monday, November 16, 2020 Sheet 68 of 106

15 SKUD UMA S16G SIT

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Title: ***Reserved***

Size	Document Number	Rev
A4	A34_TGL	SIT

Date: Monday, November 16, 2020 Sheet 69 of 106

15 SKUD UMA S16G SIT

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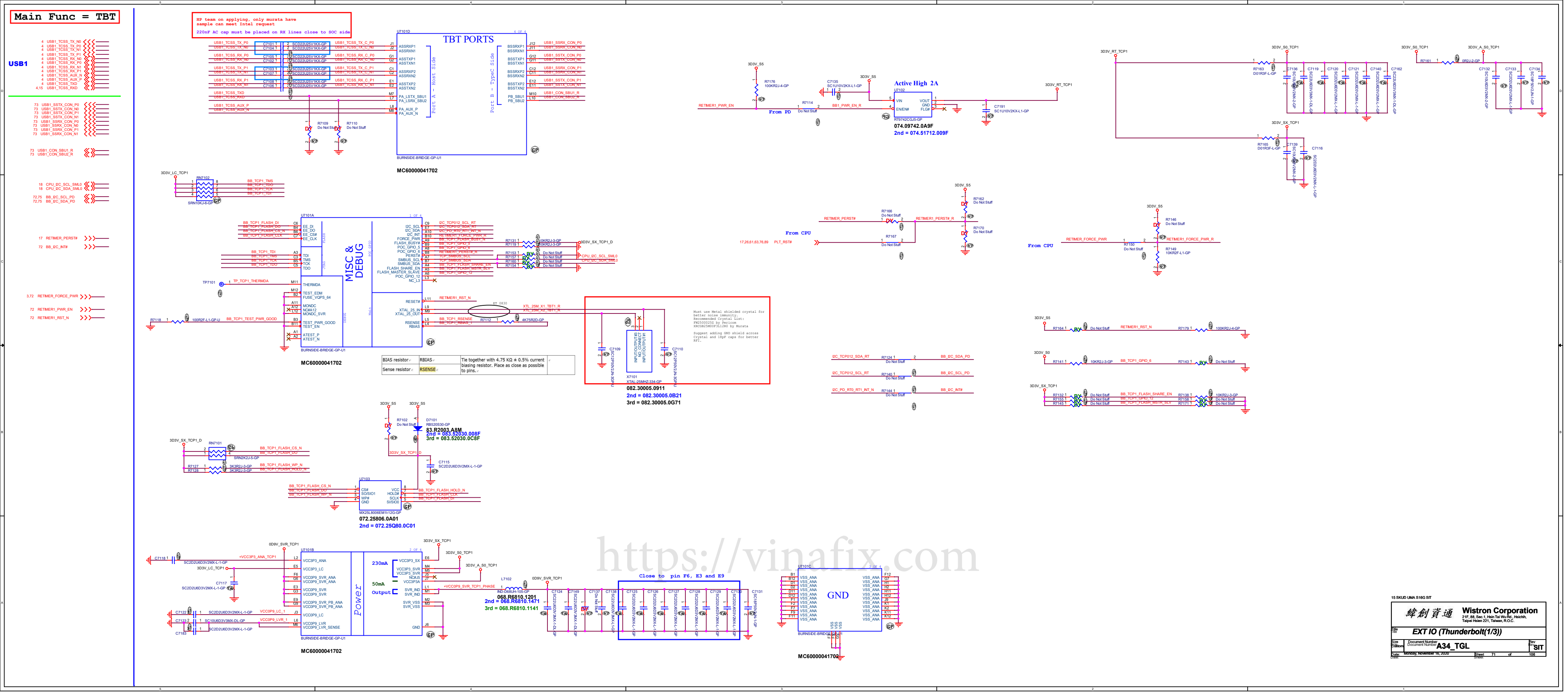
Title: ***Reserved***

Size	Document Number	Rev
A4	A34_TGL	SIT

Date: Monday, November 16, 2020 Sheet 70 of 106

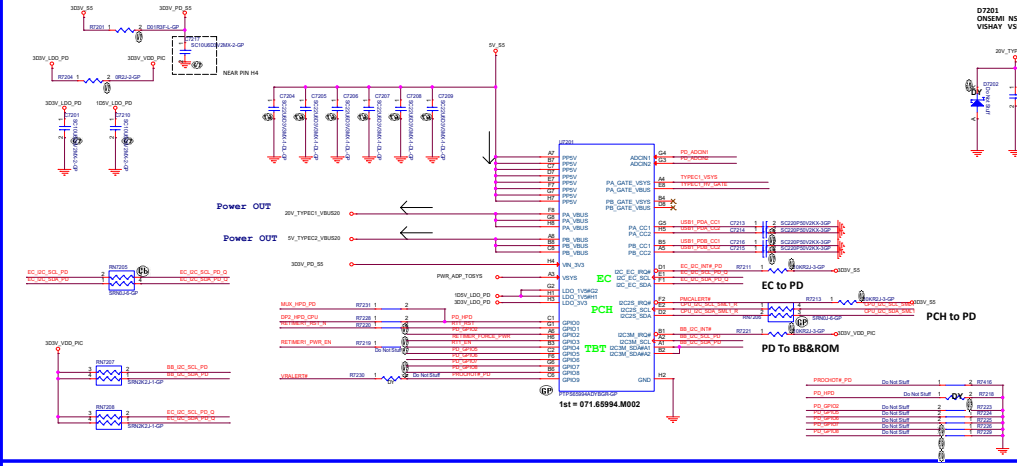


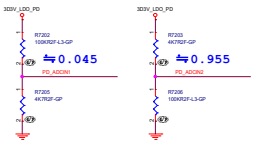
Main Func = TBT
USB1
HP team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side
TBT PORTS
Port A - Host Side
Port B - TypeC Side
BURNSIDE-BRIDGE-GP-U1
MC60000041702
MISC & DEBUG
Power
230mA
50mA Output
GND
Active High 2A
074.09742.0A9F
2nd = 074.51712.009F
From PD
From CPU
Close to pin F6, E3 and E9
BIAS resistor
RBIAS
Sense resistor
RSENSE
Tie together with 4.75 KΩ ± 0.5% current biasing resistor. Place as close as possible to pins.
Must use Metal shielded crystal for better noise immunity.
082.30005.0911
2nd = 082.30005.0B21
3rd = 082.30005.0G71
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F
072.25806.0A01
2nd = 072.25Q80.0C01
068.R6810.1201
2nd = 068.R6810.1471
3rd = 068.R6810.1141
Wistron Corporation
EXT IO (Thunderbolt(1/3))
A34_TGL
SIT

Main Func = TypeC

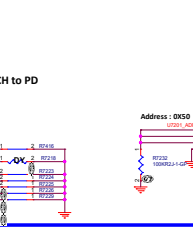
Main Func = TypeC

PD for TYPEC 1 (TBT4)& TYPEC 2





D7201
ONSEMI NSR20F30NXT5G
VISHAY VSKY20301608
PLACE NEAR U7201



I2C Address Selection

I2C1 Master: EC Slave: PD	USB1(TBT4)	0x23	TCP0
	USB2	0x27	
I2C2 Master: CPU Slave: PD	USB1(TBT4)	0x23	TCP0
	USB2	0x27	
I2C3 Master: PD Slave: Retimer	USB1(TBT4)	0x40	TCP0
	USB2	0x44	

Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)(1)	Port	Slave Address Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Available During BOOT
#1	A	0	1	0	0	0	0	0	R/W	Yes
#1	B	0	1	0	0	1	0	0	R/W	No
#2	A	0	1	0	0	0	0	1	R/W	Yes
#2	B	0	1	0	0	1	0	1	R/W	No
#3	A	0	1	0	0	0	1	0	R/W	Yes
#3	B	0	1	0	0	1	1	0	R/W	No
#4	A	0	1	0	0	0	1	1	R/W	Yes
#4	B	0	1	0	0	1	1	1	R/W	No

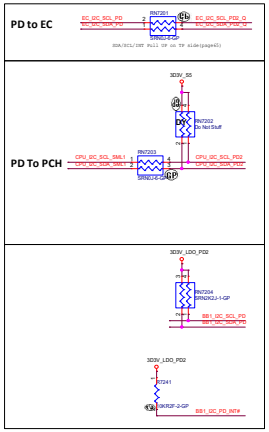
Table 6. Device Configuration using ADCIN1 and ADCIN2

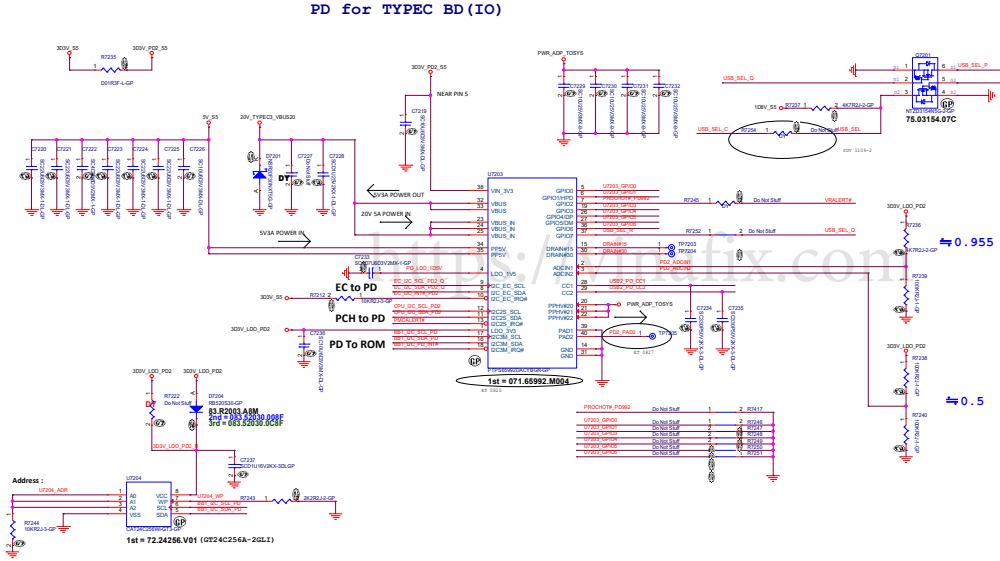
ADCIN1 decoded value (1)	ADCIN2 decoded value (1)	I²C address index (2)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1) MIN	MAX	Without using R_{UP} or R_{DOWN}	ADCINx decoded value
0	0.0228	tie to GND	0
0.0229	0.0722	N/A	1
0.0723	0.1425	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7064	tie to LDO_1V5	5
0.7065	0.9060	N/A	6
0.9061	1.0	tie to LDO_3V3	7

PD for TYPEC BD(IO)





I2C Address Selection

I2C1 Master: EC Slave: PD	USB3(IO)	0x20	
I2C2 Master: CPU Slave: PD	USB3(IO)	0x20	
I2C3 Master: PD Slave: ROM	USB3(IO)	0x50	

Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address Index (decoded from ADCIN1 and ADCIN2)(1)	Port	Slave Address Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Available During BOOT
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

Device Functional Modes (continued)

Table 6. Device Configuration using ADCIN1 and ADCIN2 .

ADCIN1 decoded value (1)	ADCIN2 decoded value (1)	I²C address Index (2)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1) MIN	MAX	Without using R_{UP} or R_{DOWN}	ADCINx decoded value
0	0.0228	tie to GND	0
0.0229	0.0722	N/A	1
0.0723	0.1425	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7064	tie to LDO_1V5	5
0.7065	0.9060	N/A	6
0.9061	1.0	tie to LDO_3V3	7

15 SKUID UMA S WIG SIT

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EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size: Custom | Document Number: A34_TGL | Rev: SIT

Date: Monday, November 16, 2020 | Sheet 72 of 108

Main Func = TypeC

USB1

Type C 2

TBT4-C Conn
TBT4/DP/PD

PIN	SIGNAL_NAME	PIN	SIGNAL_NAME
A1	GND	B12	GND
A2	SSTXp1	B11	SSRXp1
A3	SSTXn1	B10	SSRXn1
A4	VBUS	B9	VBUS
A5	CC1	B8	SBU2
A6	Dp1	B7	Dn2
A7	Dn1	B6	Dp2
A8	SBU1	B5	CC2
A9	VBUS	B4	VBUS
A10	SSRXn2	B3	SSTXn2
A11	SSRXp2	B2	SSTXp2
A12	GND	B1	GND

062.10009.M073

068.09002.2001

075.09904.0A7C
2nd = 075.53456.000C
3rd = 075.54236.007C

1st = 075.08315.0073
2nd = 083.58017.00AF

TYPE C CON.
USB3.1 Gen1 / DP1.2

PIN	SIGNAL_NAME	PIN	SIGNAL_NAME
A1	GND	B12	GND
A2	SSTXp1	B11	SSRXp1
A3	SSTXn1	B10	SSRXn1
A4	VBUS	B9	VBUS
A5	CC1	B8	SBU2
A6	Dp1	B7	Dn2
A7	Dn1	B6	Dp2
A8	SBU1	B5	CC2
A9	VBUS	B4	VBUS
A10	SSRXn2	B3	SSTXn2
A11	SSRXp2	B2	SSTXp2
A12	GND	B1	GND

062.10009.M075

DY
Do Not Stuff

075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003

75.05125.07D
2nd = 075.00353.0A7D
3rd = 075.52215.007D

15 SKUID UMA S16G SIT

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size: Custom | Document Number: A34_TGL | Rev: SIT

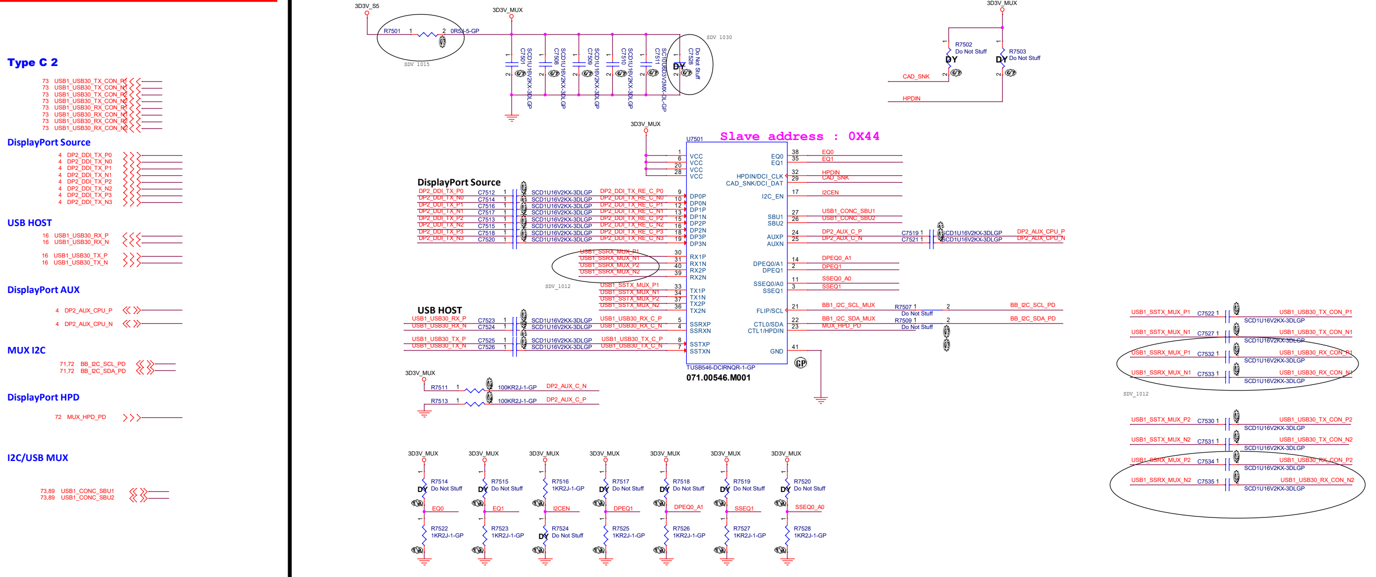
Date: Monday, November 16, 2020 | Sheet 73 of 106

Main Func = TypeC

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RSVD*		
Size: A4	Document Number: A34_TGL	Rev: SIT
Date: Monday, November 16, 2020	Sheet 74 of 106	

Main Func = TYPEC MUX



FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode, Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

15 SKUD UMA S16G SIT

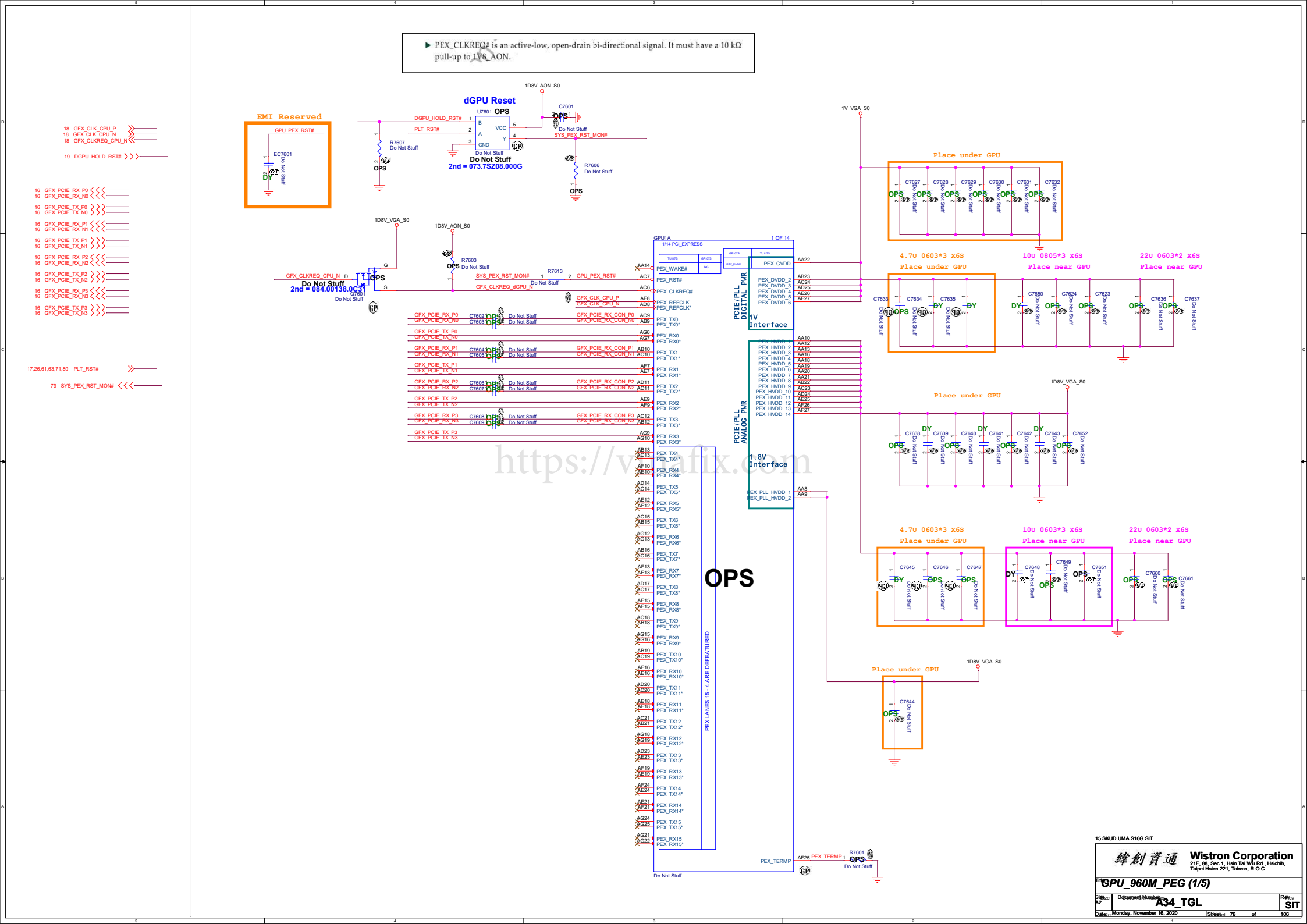
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 075_EXT IO (TypeC driver)

Size: Custom | Document Number: A34_TGL | Rev: SIT

Date: Monday, November 16, 2020 | Sheet 75 of 106

▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.



15 SKUD UMA S16G SIT

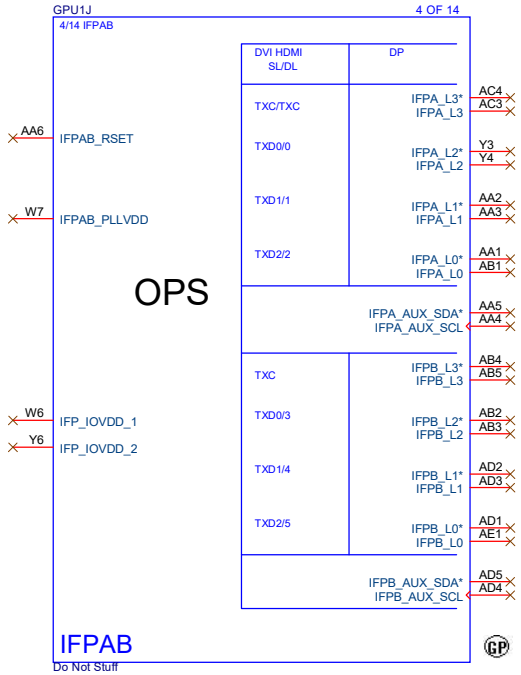
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

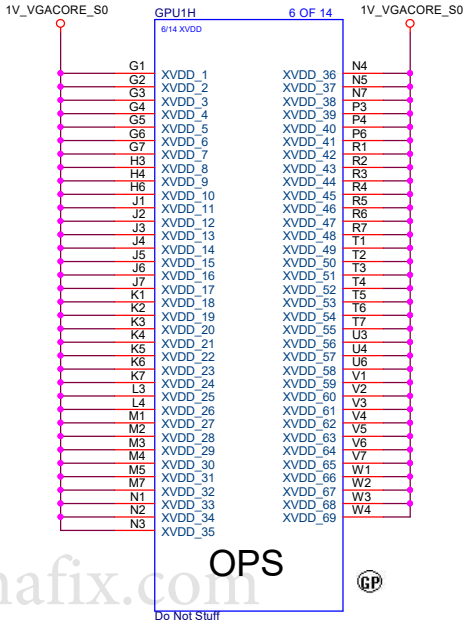
Title: GPU_960M_PEG (1/5)

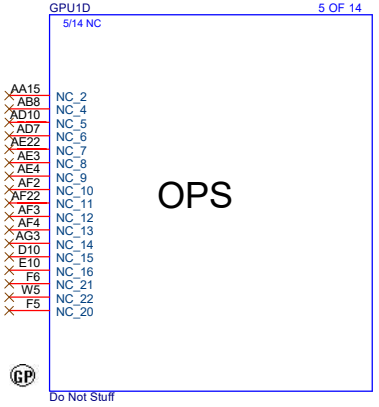
Size: A2 | Document Number: A34_TGL | Rev: SIT

Date: Monday, November 16, 2020 | Sheet 76 of 106

Main Func = dGPU







Vinafix.com

15 SKUD UMA S16G SIT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU_DIGITALOUT (2/5)**

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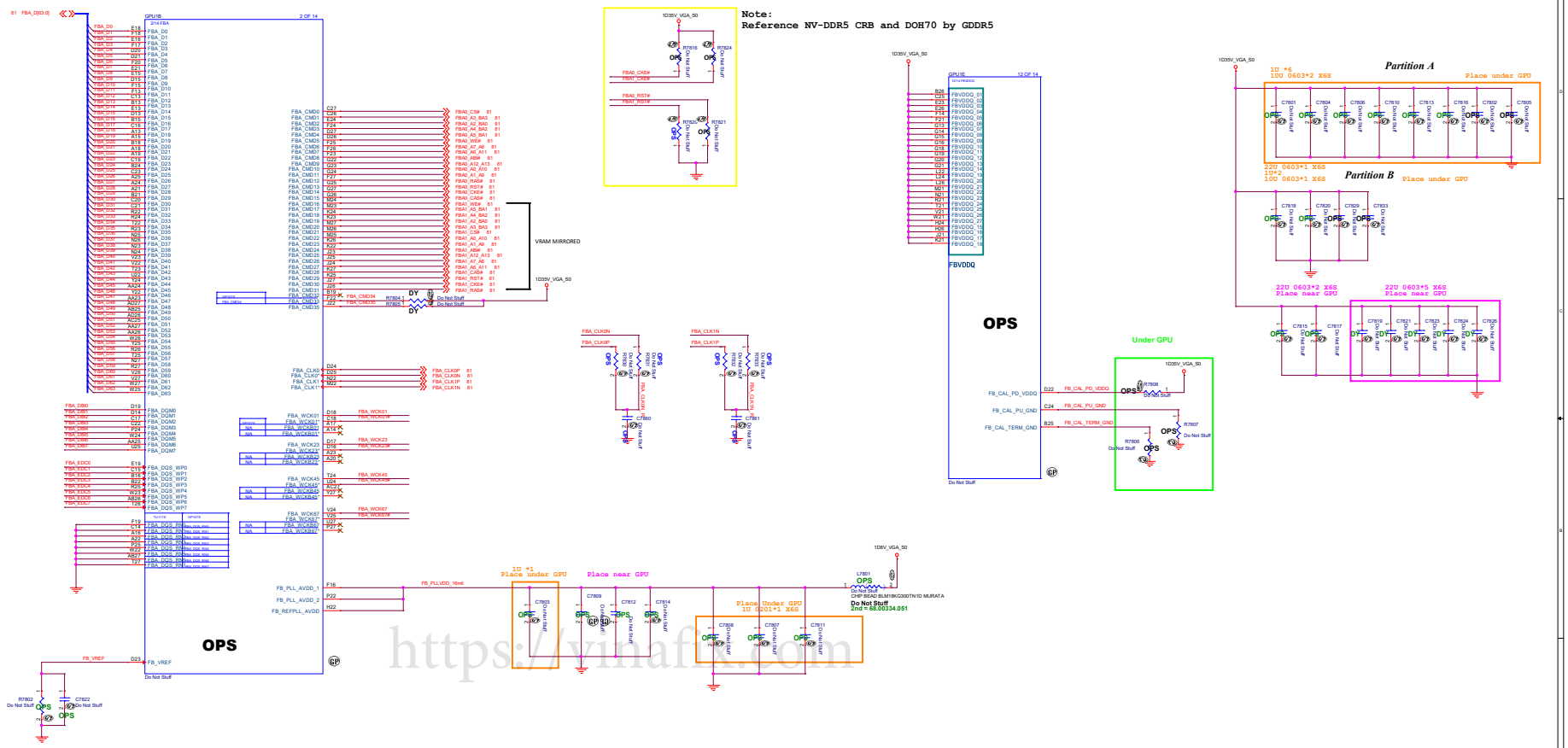
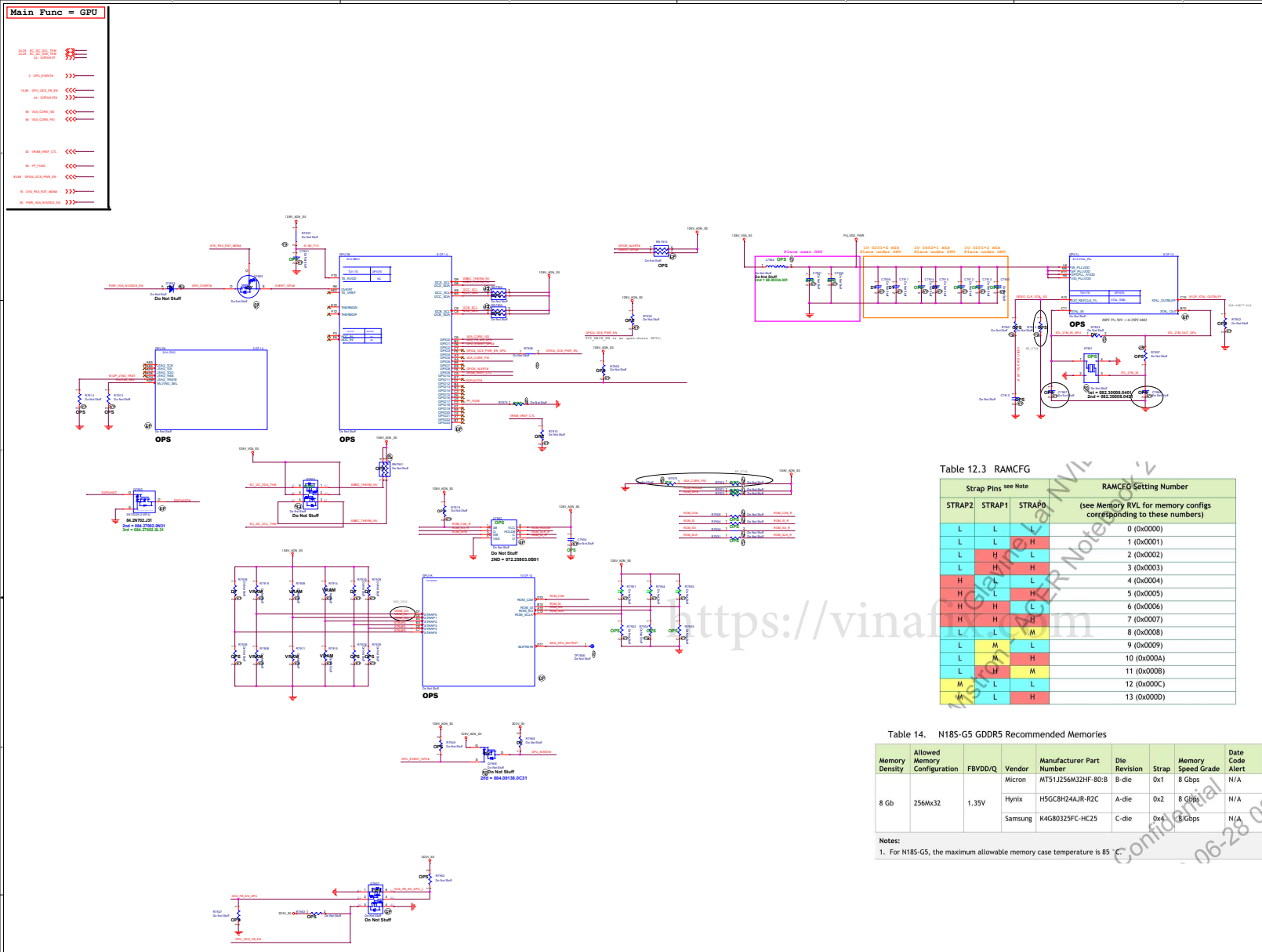
Group A

Group B

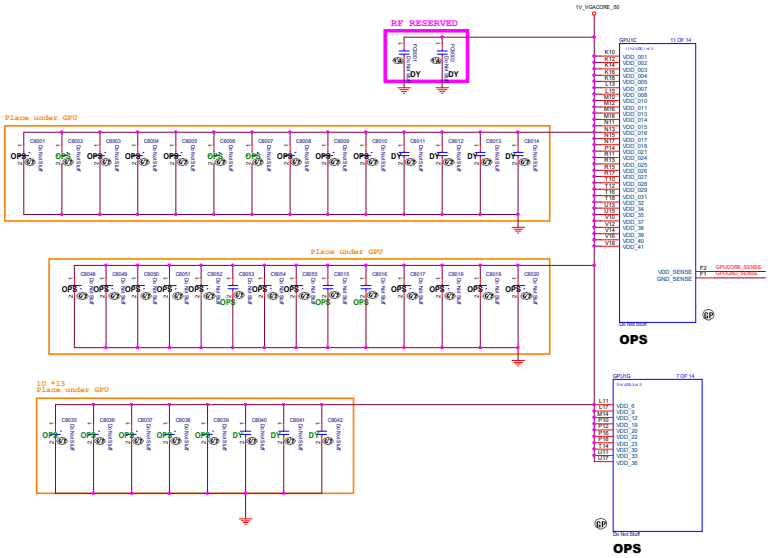


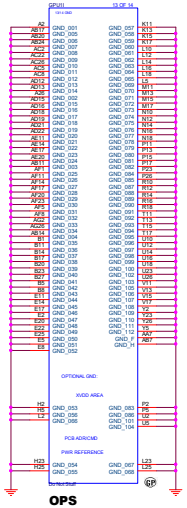
15 SKUID LIMA S16G SIT

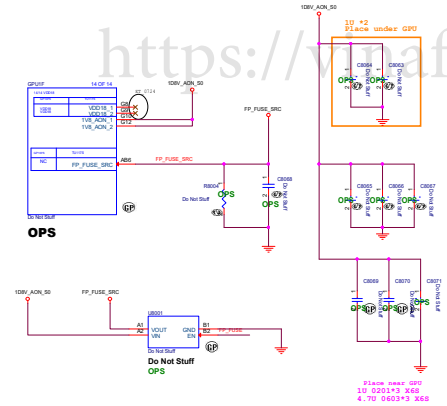
緯創資通	Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU_VRAM I/F (3/5)	
Size: Custom	Document Number: A34_TGL
Rev: SIT	
Date: Monday, November 16, 2020	Sheet 78 of 109


Main Func = GPU
OPS
Do Not Stuff
Place near GPU
10 0201*4 X6S
Place under GPU
10 0402*1 X6S
10 0201*2 X6S
Table 12.3 RAMCFG
Strap Pins see Note
RAMCFG Setting Number
(see Memory RVL for memory configs corresponding to these numbers)
STRAP2 STRAP1 STRAP0
L L L 0 (0x0000)
L L H 1 (0x0001)
L H L 2 (0x0002)
L H H 3 (0x0003)
H L L 4 (0x0004)
H L H 5 (0x0005)
H H L 6 (0x0006)
H H H 7 (0x0007)
L L M 8 (0x0008)
L M L 9 (0x0009)
L M H 10 (0x000A)
L H M 11 (0x000B)
M L L 12 (0x000C)
M L H 13 (0x000D)
Table 14. N18S-G5 GDDR5 Recommended Memories
Memory Density
Allowed Memory Configuration
FBVDD/Q
Vendor
Manufacturer Part Number
Die Revision
Strap
Memory Speed Grade
Date Code Alert
Qual Plan
Status
8 Gb 256Mx32 1.35V
Micron MT51J256M32HF-80:B B-die 0x1 8 Gbps N/A Full Production candidate
Hynix H5GC8H24AJR-R2C A-die 0x2 8 Gbps N/A Full Production candidate
Samsung K4G80325FC-HC25 C-die 0x4 8 Gbps N/A Full Production candidate
Notes:
1. For N18S-G5, the maximum allowable memory case temperature is 85 °C.
Wistron Corporation
GPU_GPIO/STRAP
A34_TGL
SIT

Main Func = GPU







15.SKLD.UMA.S16G.SIT

蜂創資通 Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU_POWER/GND (5/5)

Document Number: A34_TGL

Rev: SIT

Monday, November 16, 2009

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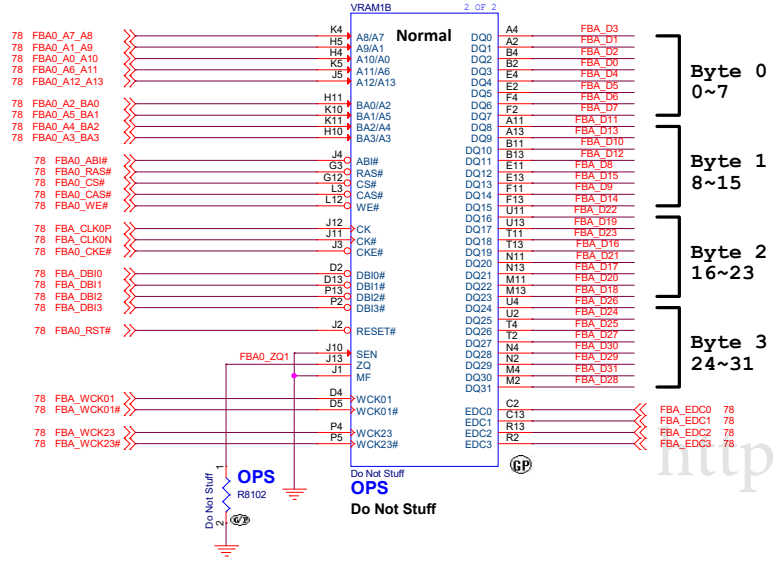
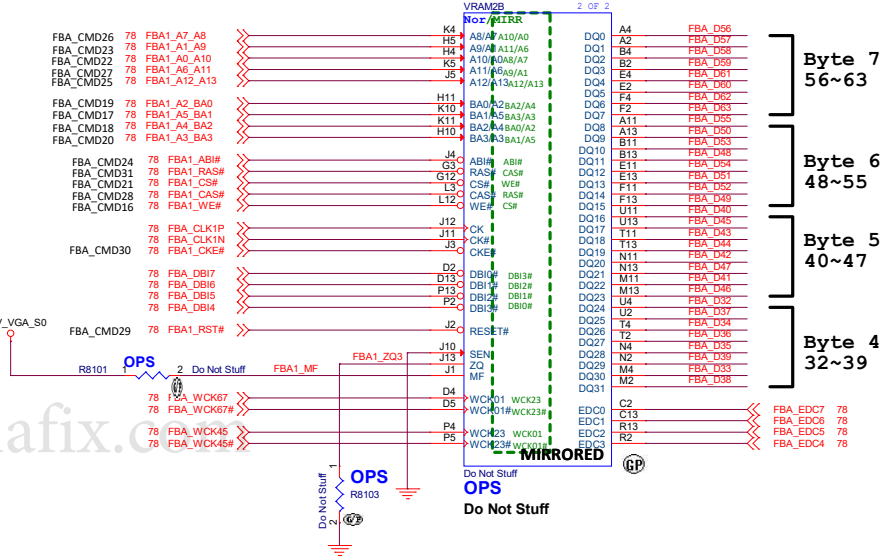
TABLE
GDDR5 VIDEO MEMORY 072.05424.0A0U 072.44132.000U 072.04032.000N

	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1 VRAM2	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BABG-60-F-D





15 SKUD UMA S16G SIT

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (VRAM CH AB)**

Size	Document Number	Rev
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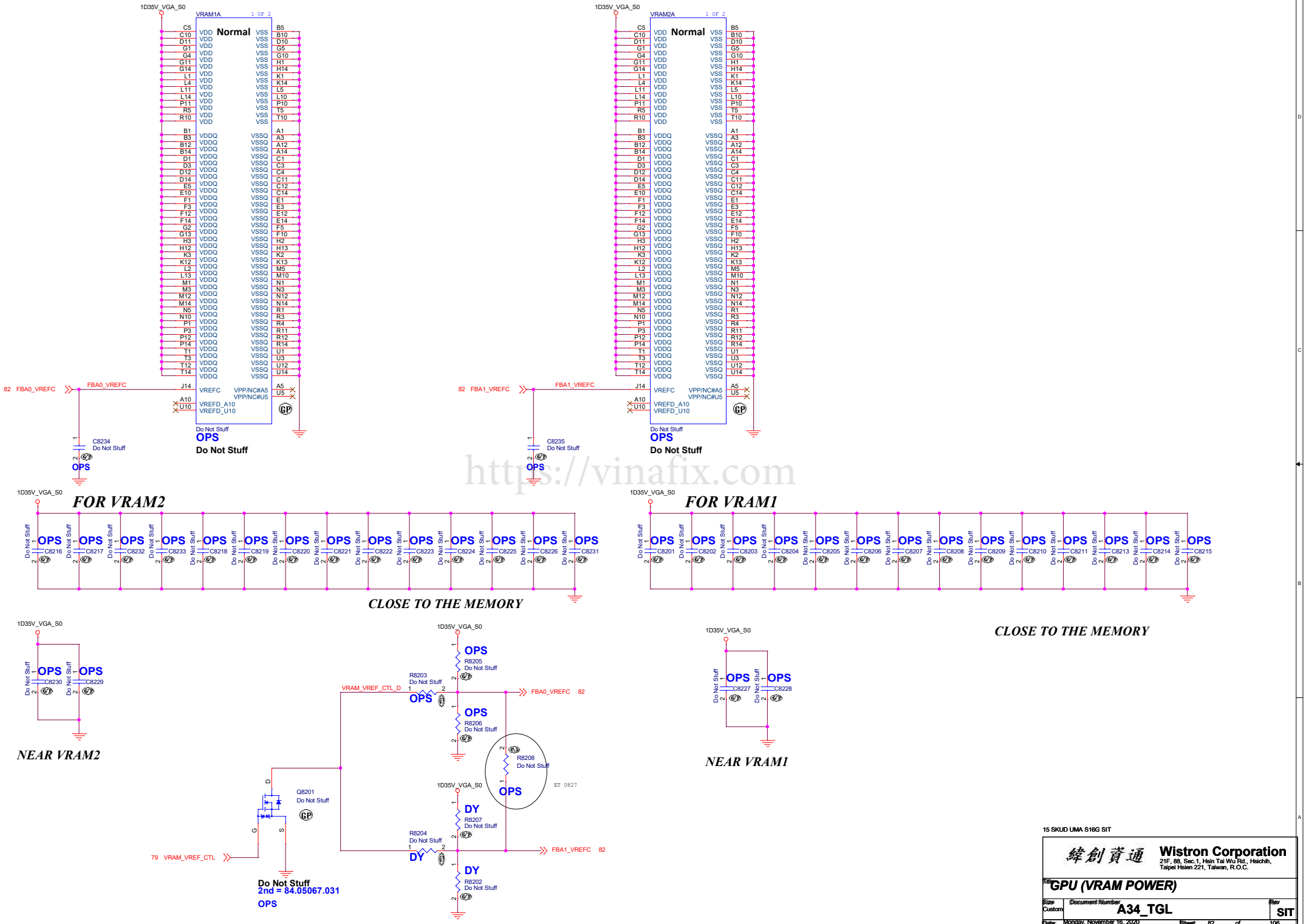

15 SKUD UMA S16G SIT

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM POWER)

Size	Document Number	Rev
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VGA Power A***

Size	Document Number	Rev
A4	A34_TGL	SIT

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Title: ***VGA Power B***

Size	Document Number	Rev
A4	**A34_TGL**	**SIT**

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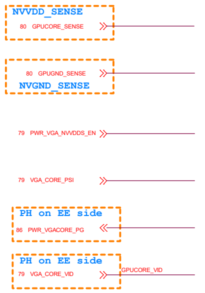

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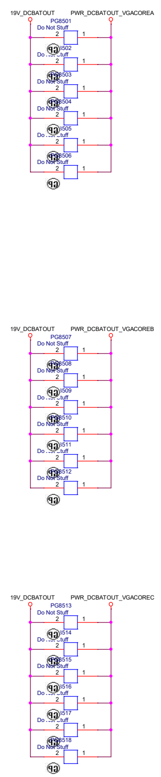


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

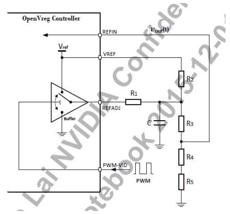
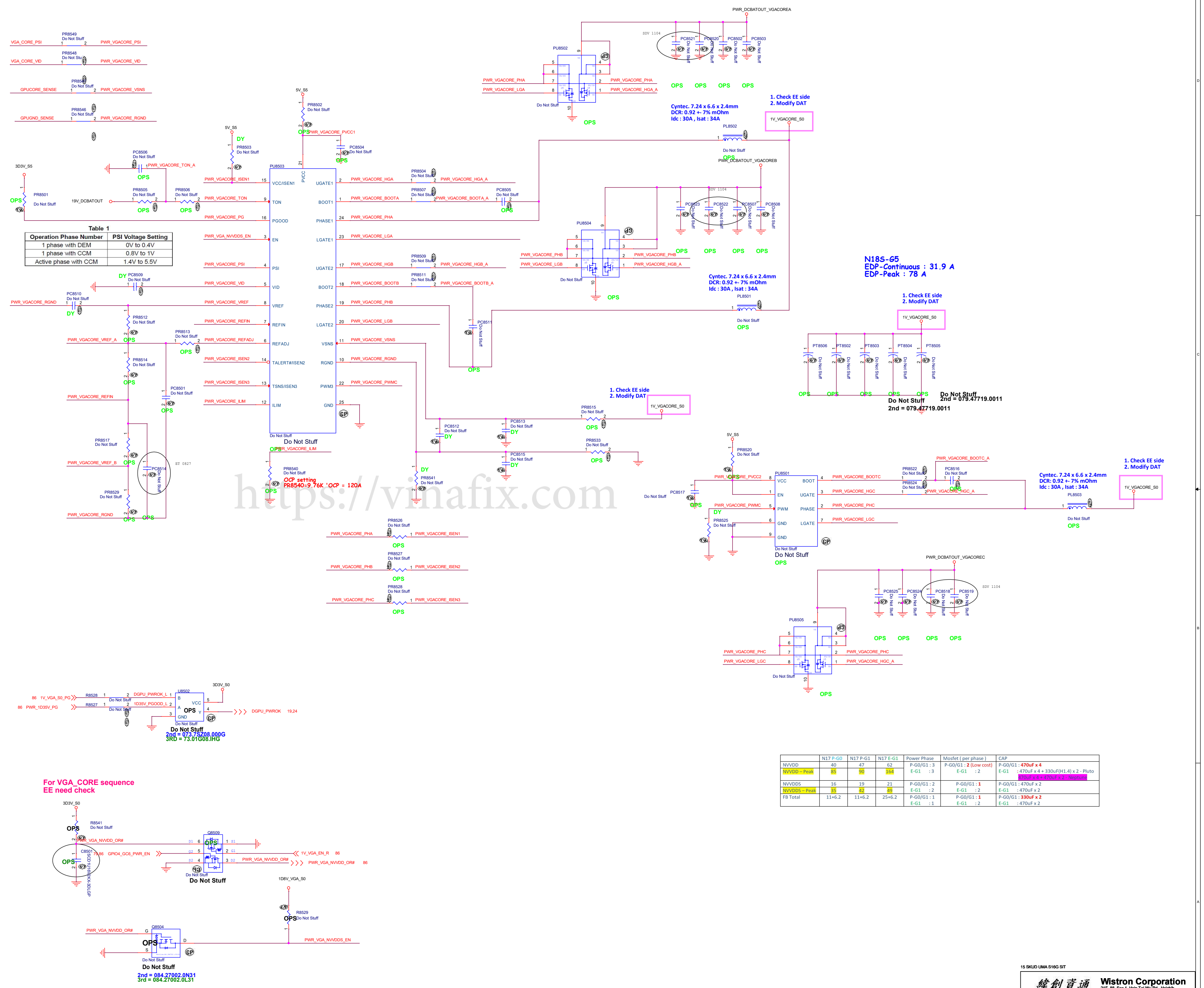


Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	1.5

Table 1

Operation Phase Number	PSI Voltage Setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.8V to 1V
Active phase with CCM	1.4V to 5.5V



	N17 P-G0	N17 P-G1	N17 E-G1	Power Phase	Mosfet (per phase)	CAP
NVVDD	40	47	62	P-G0/G1 : 3 E-G1 : 3	P-G0/G1 : 2 (Low cost) E-G1 : 2	P-G0/G1 : 470uF x 4 E-G1 : 470uF x 4 + 330uF(H1.4) x 2 - Pluto 470uF x 4 + 470uF x 2 - Neptune
NVVDD – Peak	85	90	164			
NVVDDS	16	19	21	P-G0/G1 : 2 E-G1 : 2	P-G0/G1 : 1 E-G1 : 2	P-G0/G1 : 470uF x 2 E-G1 : 470uF x 2
NVVDDS – Peak	35	42	49			
FB Total	11+6.2	11+6.2	25+6.2	P-G0/G1 : 1 E-G1 : 1	P-G0/G1 : 1 E-G1 : 2	P-G0/G1 : 330uF x 2 E-G1 : 470uF x 2

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SSID = PWR.Plane.Regulator_1p35v

G5335F for 1D35V

TDC : 8A
ICCMAX=8A

Table 7. Output EDP-Continuous

	NVVDD	GPU FBIO	FB Total[2]	1.0V Total[1]	1.8V Total[1]
	--	1.35V[4]	1.35V[4]	1.0V[4]	1.8V[4]
Product	(A)	(A)	(A)	(A)	(A)
H175-G1	30.0	3.0	5.6	0.1	0.1
H175-LG	15.4	2.5	5.0	0.1	0.2

Table 8. Output EDP-Peak

	NVVDD	GPU FBIO	FB TOTAL[4]	1.0V Total[1]
	--	1.35V[3]	1.35V[3]	1.0V[3]
Product	(A)	(A)	(A)	(A)
H175-G1	60.1	3.4	6.9	0.2
H175-LG	48.3	2.8	5.8	0.2

G2822 for 1V_VGA_S0

1D8V_AON_S0 to 1D8V_VGA_S0

TDC=1.2A
Imax=1.9A

For tuning VGA_CORE sequence.

Main Func = dGPU

3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D8V_AON_S0

1D8V_VGA_S0

1D8V_VGA_S0

1D35V_VGA_S0

Wistron Corporation

G5335F_1D35V

A34_TGL

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RSVD***

Size	Document Number	Rev
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Title: ***UNUSED PARTS (RSVD)***

Size	Document Number	Rev
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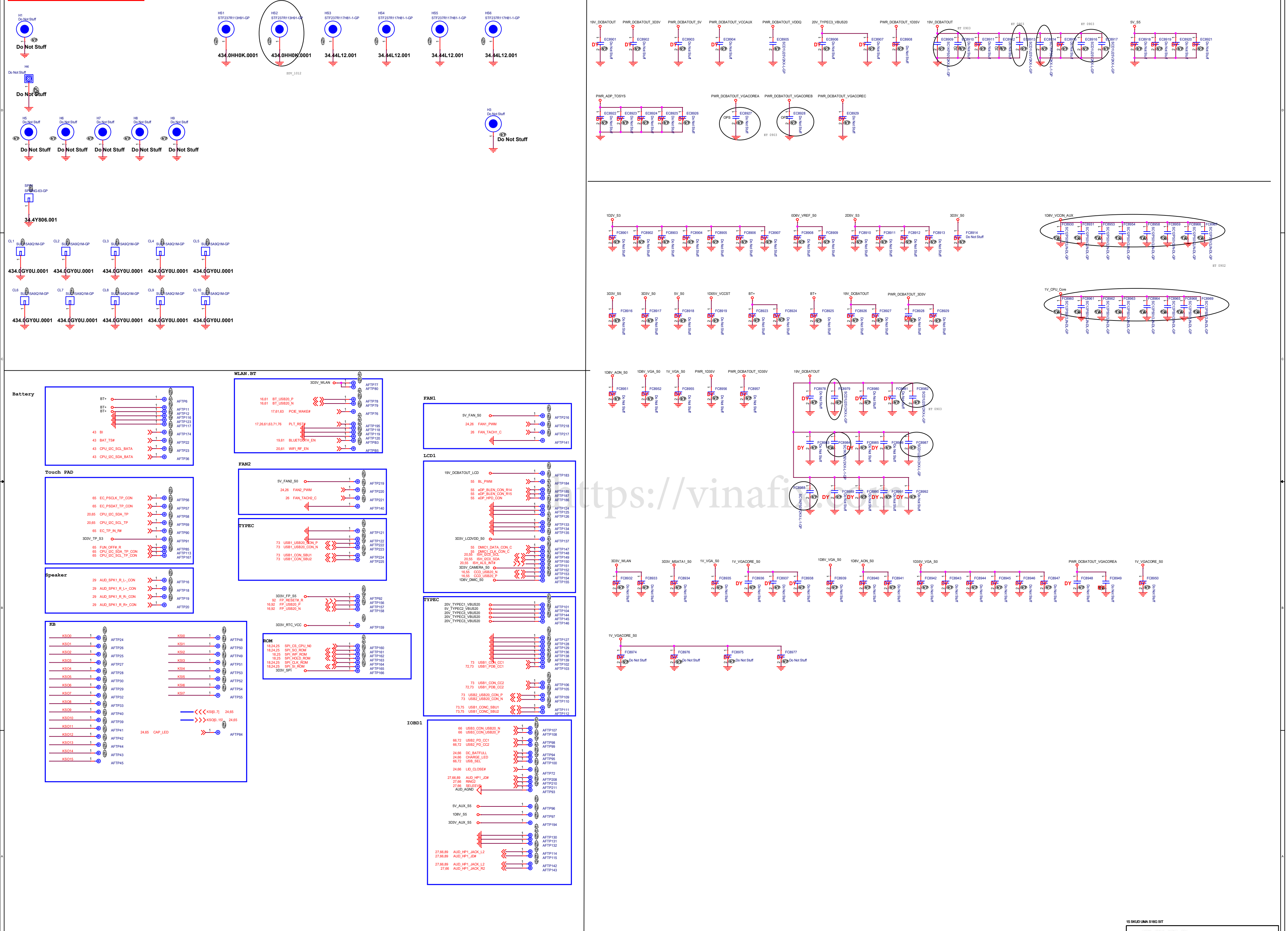
Main Func = EMC/ RF



15 SKUD UMA S16G SIT

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UNUSED PARTS (RF/EMI Capacitors)

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***INT IO (RSVD)***

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緯創資通

Wistron Corporation
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Title: ***INT IO (TPM)***

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Main Func = Finger Printer

16,89 FP_USB20_P
16,89 FP_USB20_N
24,64,92 KBC_PWRBTN#
24 FP_GPIO_AL0
24 FP_DELINK
24,64,92 KBC_PWRBTN#
24 FP_RESET#
89 FP_RESET#_R

FP1
HRS-CONN-GP
020.K0376.0008
2nd = 020.K0328.0008
3rd = 20.K0767.008
3D3V_FP_S5
FP_RESET# R
FP_USB20_CON_N
FP_USB20_CON_P
device internal PU
FP_DELINK_R
FP_GPIO_AL0_R
KBC_PWRBTN#
GPIO2
GPIO3
EC9203
Do Not Stuff
DY

3D3V_S5
3D3V_AUX_S5
R9210
Do Not Stuff
R9211
0R2J-2-GP
DY
3D3V_FP_S5
C9201
SCD1U16V2KX-3GP

3D3V_FP_S5
R9212
Do Not Stuff
DY
FP_DELINK_R
R9213
Do Not Stuff
DY
3D3V_FP_S5
R9214
Do Not Stuff
DY
FP_GPIO_AL0_R
R9215
Do Not Stuff
DY

R9202
0R2J-2-GP
FP_USB20_CON_P
FP_USB20_CON_N
EL9201
DY
Do Not Stuff
FP_USB20_P
FP_USB20_N
Do Not Stuff
R9201
0R2J-2-GP

FP_USB20_CON_P
FP_USB20_CON_N
EU9202
AZ5315-02F-GP
83.05315.0A0

FP_DELINK
R9223
0R2J-2-GP
FP_DELINK_R
FP_GPIO_AL0
R9222
0R2J-2-GP
FP_GPIO_AL0_R
FP_RESET#
R9221
Do Not Stuff
FP_RESET#_R
DY
KBC_PWRBTN#
EU9201
Do Not Stuff
DY
EC9202
Do Not Stuff
DY

SDV 1013
3D3V_FP_S5
R9216
Do Not Stuff
DY
FP_DELINK
Q9201
FP_DELINK_R
3D3V_FP_S5
3D3V_FP_S5
FP_GPIO_AL0
FP_GPIO_AL0_R
R9217
Do Not Stuff
Do Not Stuff
DY
DY
3D3V_FP_S5

3D3V_FP_S5
R9218
Do Not Stuff
DY
Q9202
FP_RESET#
FP_RESET#_R
3D3V_FP_S5
Do Not Stuff
Do Not Stuff
DY

15 SKUD UMA S16G SIT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: INT IO (Finger Printer)		
Size: A3	Document Number: A34_TGL	Rev: SIT
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EXT IO (RSVD) (Express Card/PCIE slot)**

Size	Document Number	Rev
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (RSVD)***

Size	Document Number	Rev
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Wistron Corporation
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Title: ***EXT IO (RSVD)***

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Commercial (RSVD)*

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Title: ***Commercial (RSVD)***

Size	Document Number	Rev
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Commercial (RSVD)***

Size	Document Number	Rev
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Title: ***Debug (XDP debug)***

Size	Document Number	Rev
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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Title: *Change History*

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Bandon /NorthBay Power Up Sequence Diagram (Non_Deep Sx Platform)

Battery BTY1 — BT+ → MOS EMB07P03H → 19V_DCBATOUT

TypeC USB1 — 20V_TYPEC1_VBUS20 → dual MOS CSD87501L → PWR_ADP_TOSYS → Chargrer BQ25710RSNR

TypeC USB3 — 20V_TYPEC3_VBUS20 → MOS TPS65992DAC → PWR_ADP_TOSYS

19V_DCBATOUT → SY8288BRAC (Vin / Vout / EN / PGOOD) → 3D3V_S5, 3D3V_PG

19V_DCBATOUT → SY8288CRAC (Vin / Vout / EN / PGOOD) → 5V_S5, 5V_PG

KBC_NPCE385

GPIO013

b — PWR_3D3V_EN

c — DSW_PWROK

19V_DCBATOUT → G5335DQZ1U (Switching Regulator) → 1D8V_S5, PWR_1D8V_PG (g)

PM_SLP_SUS#

19V_DCBATOUT → RT6543AGQW (Switching Regulator) → 1D8V_VCCIN_AUX, PWR_VCCAUX_PG (h)

CORE_VID1, CORE_VID2

19V_DCBATOUT → APW8743CQBI (Switching Regulator) → PWR_VNN_EN, PWR_1D05V_EN, PWR_VNN1D05V_PG (i)

j — RSMRST#_KBC

1 — KBC_PWRBTN#

2 — PM_PWRBTN#

Virtual Wire — PM_SLP_S3#

TGL U

d — DSW_PWROK → DSW_PWROK

PM_SLP_SUS# → SLP_SUS# (e)

f — CORE_VID1 → GPP_B0/CORE_VID0

CORE_VID2 → GPP_B1/CORE_VID1

k — PM_RSMRST# → RSMRST#

GPD3/PWRBTN#

SLP_S5#

SLP_S4#

PM_SLP_S3# → G2898KD1U (5V_S5, 3D3V_S5 → 5V_S0, 3D3V_S0)

Load SW 1D8V_S5 → PJA3413 → 1D8V_S0

PM_SLP_S5# (3), PM_SLP_S4# (4), VTT_CNTL → G5416QS1U-GP (19V_DCBATOUT, 5V_S5 → 2D5V_S3, 1D2V_S3, 0D6V_S0, PWR_VDDQ_PG)

PWR_VDDQ_PG, PM_SLP_S3# → AND GATE → ALL_SYS_PWRGD → LS → VCCST_PWRGD_R → VCCST_PWRGOOD

10 — VTT_CNTL → DDR_VTT_CTL

CPU_C10_GATE#

PCH_PWROK → PCH_PWROK

11 — SYS_PWROK → SYS_PWROK

SLP_S3#

SLP_S0#

12 — PLT_RST# → PLT_RST#

CPU_C10_GATE# (5), VCCST_OVERRIDE (6) → OR GATE → VCCSTG_EN_R

PM_SLP_S3# → OR GATE (7)

PM_SLP_S0#

Switching Regulator

1D05V_S5_OUT 5V_S5 → G5027CRD1D → 1D05V_VCCSTG

Load SW

1D05V_S55V_S5 → G5027CRD1D → 1D05V_VCCST

Load SW

8 — VR_EN

9 — VR_RDY

VR_ENABLE VR_READY

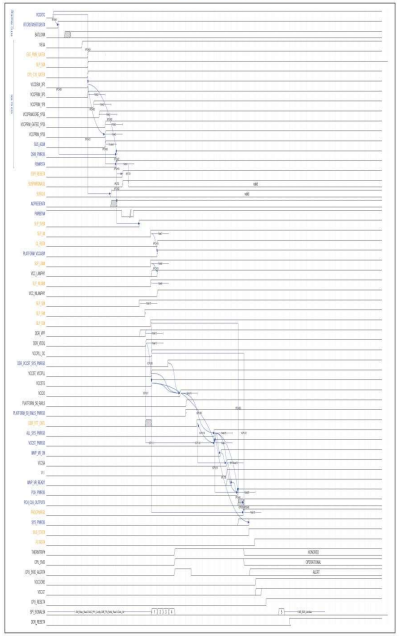
IMVP8 RT3612EBGQW

a b c d e f g h i

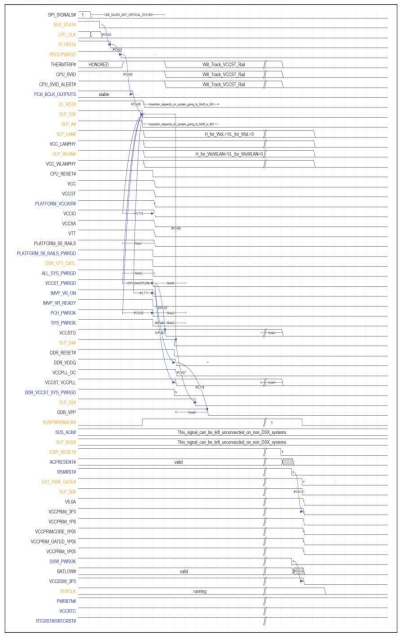
1 2 3 4 5 6 7 8 9 10

11 12

Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]



15 SKUD UMA S16G SIT

Wistron Corporation
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Title: Power Sequence

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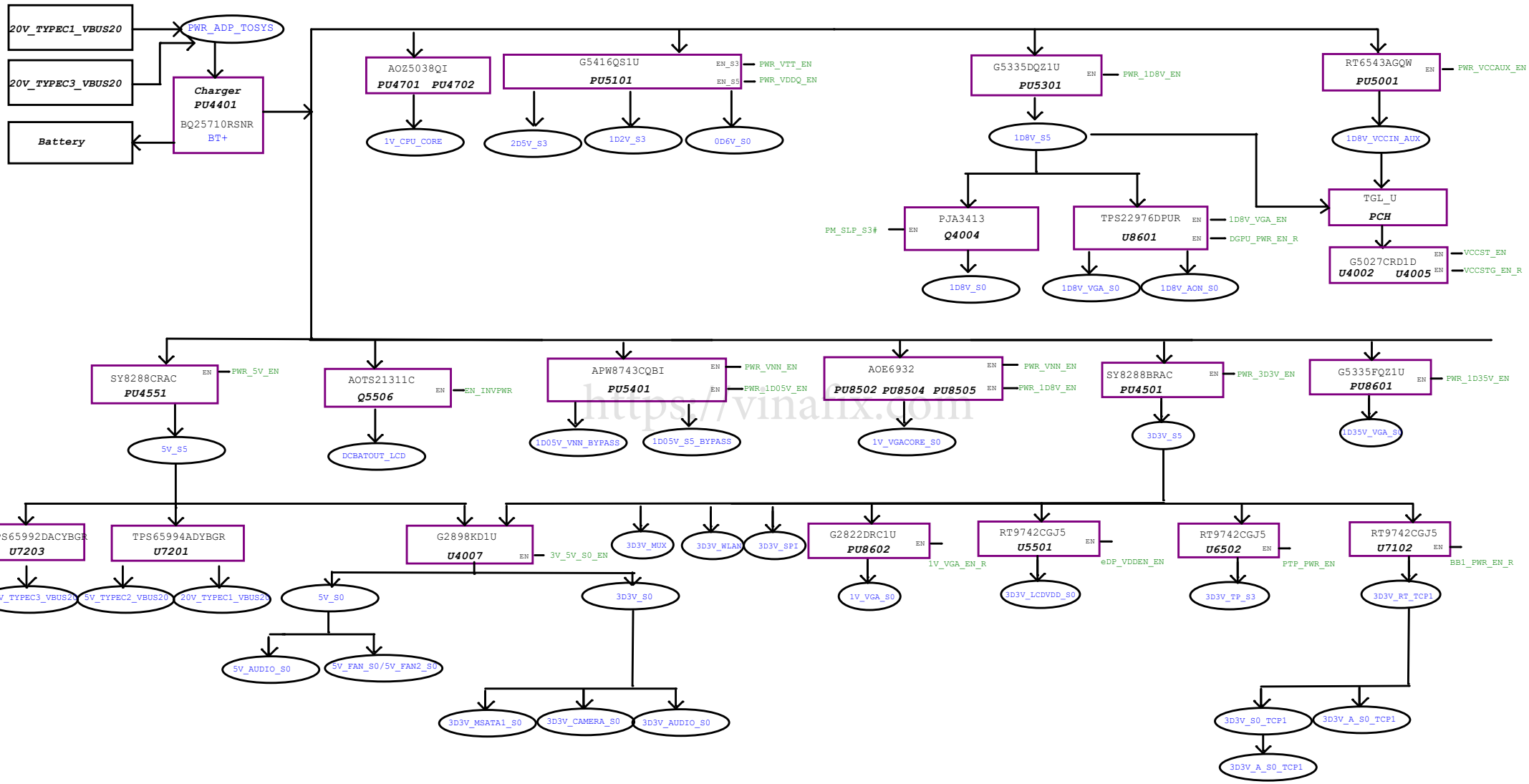

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Title: Power Block Diagram

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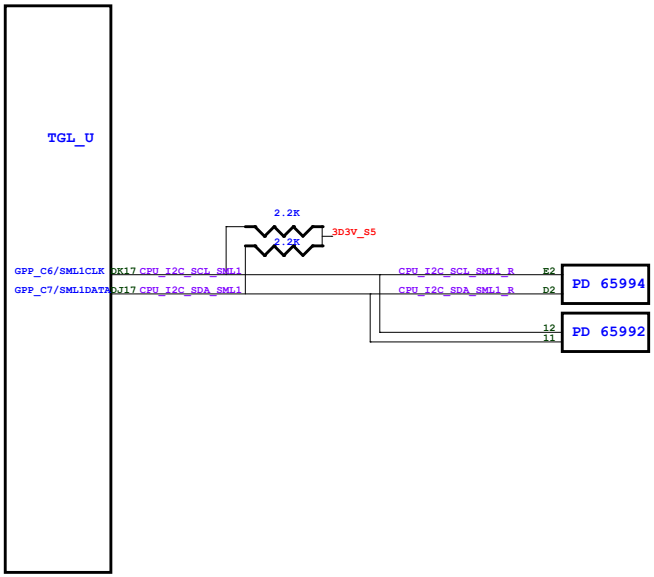
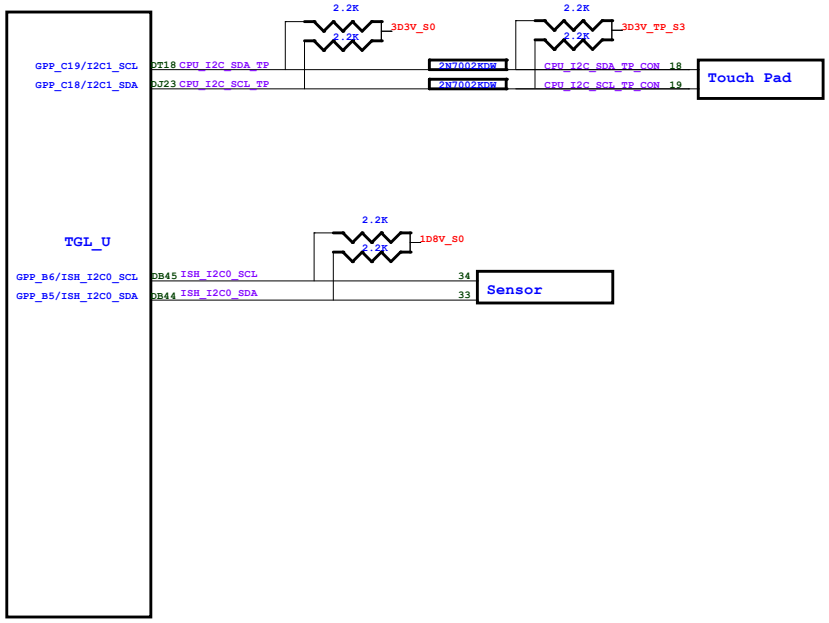
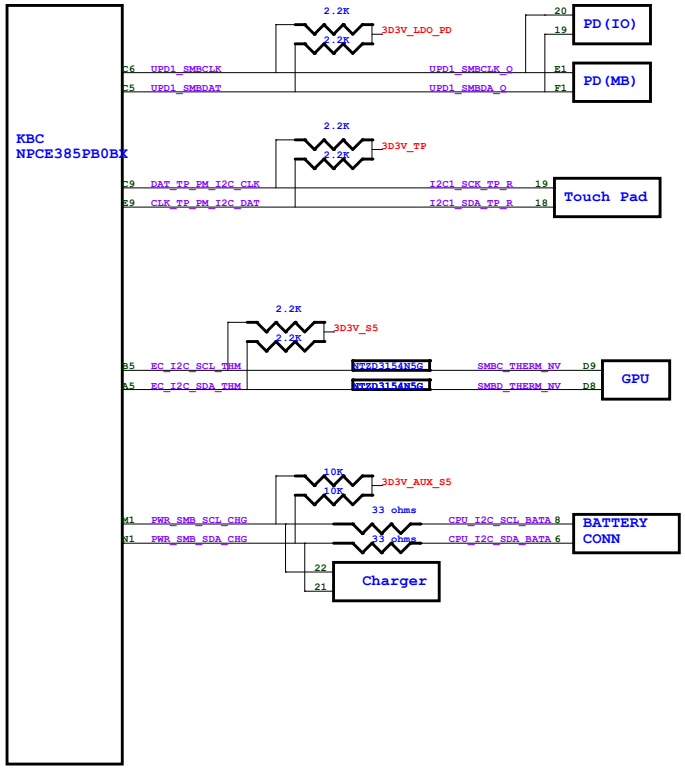
SMbus Block Diagram



I2C Block Diagram





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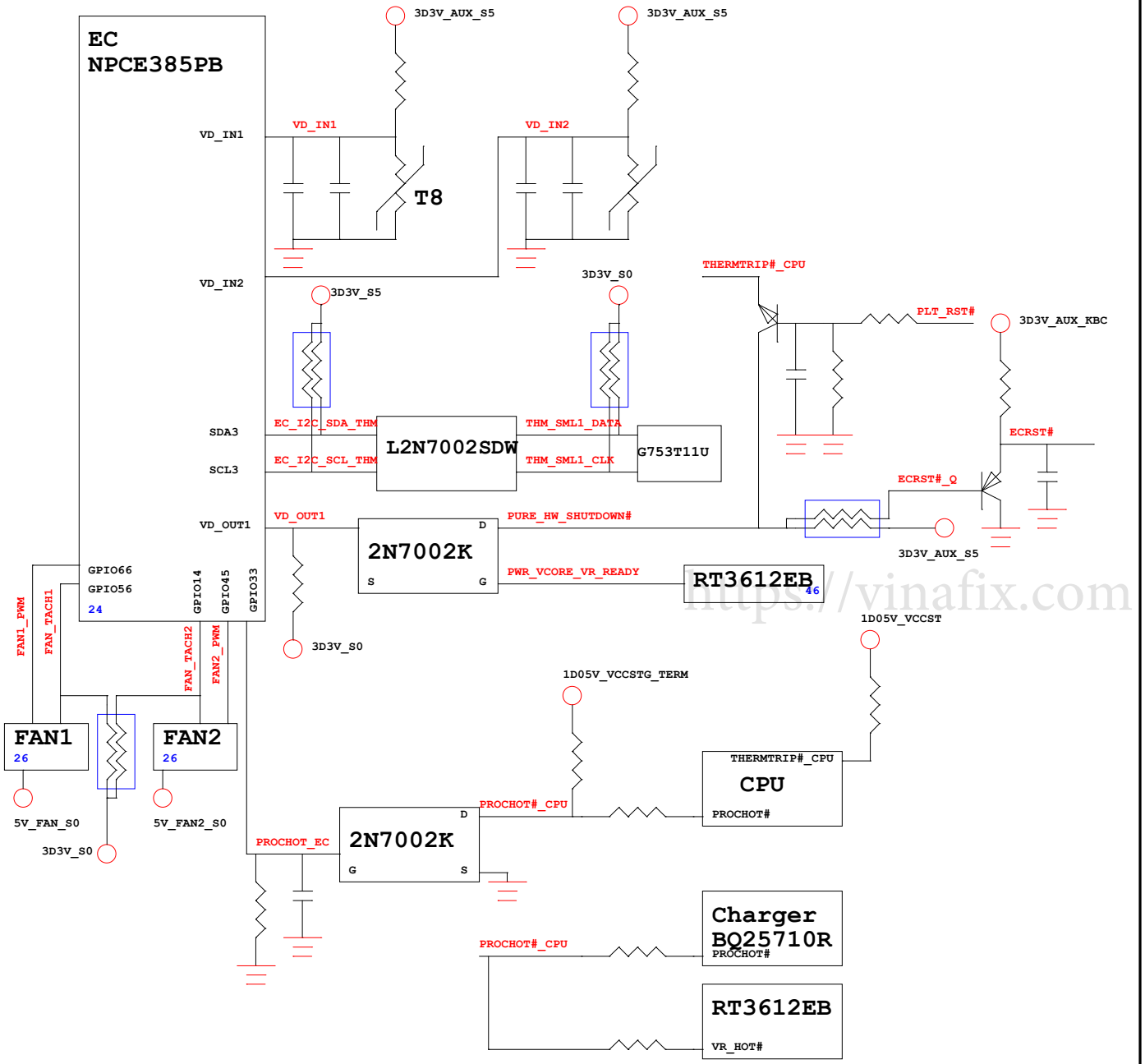
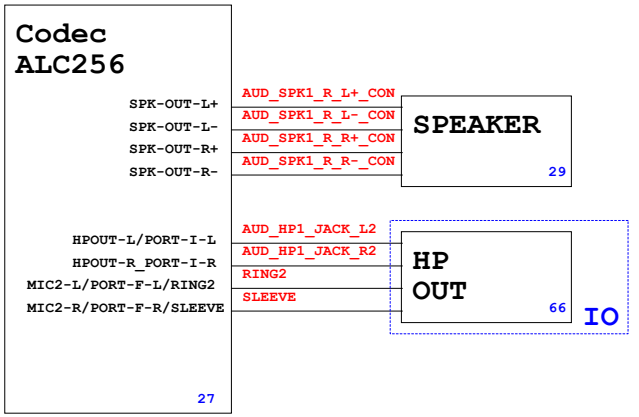
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM		
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