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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

TENJIN

MV BUILD

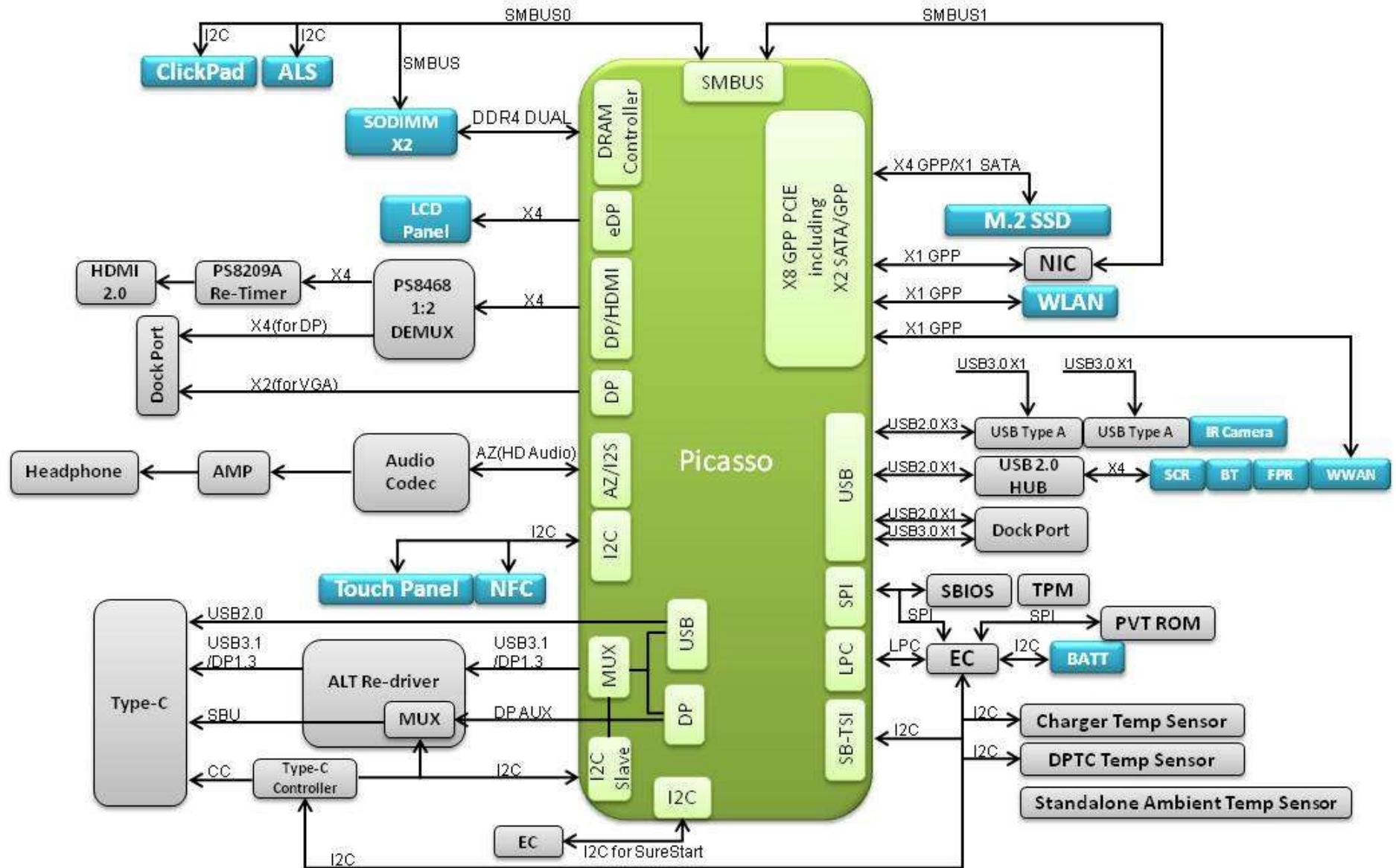
2019.5.17

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN/DRAWER		XXX	DATE		21-OCT-2002	TITLE		MODEL PROJECT,FUNCTION		
CHECK		EVAN SHIH	SIZE		A3	CODE		MAIN BOARD		
APPROVAL		MORRIS CHANG	PCB PIN		XXXXXXXXXX	PCB VER		XXX		
FILE NAME		TENJIN (20190517) (2) (1).dxf	SHEET		1 of 66	DOC NUMBER		1.310XXXXXXXX-0		
REV			REV		X01	SHEET		1 of 66		

INVENTEC

700 System Block Diagram



TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET			REV
1			X01

CHANGE# xxx PCBPN 6Dxxxxxxxxx DATE 21-OCT-2002 PCBVER xxx

TABLE OF CONTENTS

01.PROJECT NAME	30.APU FP5-7	58.POWER BUTTON LED
02.BLOCK DIAGRAM	31.APU FP5-8	59.SMART CARD D/B
03.TABLE OF CONTENTS	32.APU FP5-9	60.SMART CARD LED
04.PROJECT DESIGN INFO.	33.DDR4_SO-DIMM0	61.USB D/B-1
05.BLOCK DIAGRAM_POWER	34.DDR4_SO-DIMM1	62.USB D/B-2
06.SEQUENCE	35.DP DEMUX	63.ALS D/B
07.I2C/SMBUS MAP	36.HDMI CNTR	64.MIC D/B
08.SYSTEM POWER(CHARGER)	37.EDP & WEBCAM	65.SCREW
09.SYSTEM POWER(BARREL/PD SELECTOR)	38.M.2 SSD CNTR	66.EMI & RF SOLUTION
10.SYSTEM POWER(ADP_ID/OCP)	39.USB 2.0 HUB & USB 3.0 RE-DRIVER	
11.SYSTEM POWER(P5V0DS)	40.USB WALK UP0	
12.SYSTEM POWER(P3V3DS)	41.USB-C PD CONTROLLER	
13.SYSTEM POWER(P1V2)	42.USB-C REDRIVER	
14.SYSTEM POWER(P2V5)	43.USB-C CNTR	
15.SYSTEM POWER(P0V9A)	44.FP & PS & NFC CNTR	
16.SYSTEM POWER(P1V8A)	45.BIOS	
17.VCORE CONTROLLER	46.KBC	
18.SYSTEM POWER(VCORE & VCORE_NB)	47.KEYBOARD	
19.NA	48.TPM	
20.DC JACK & BATTERT CNTR.	49.LAN NIC	
21.POWER(SLEEP)	50.TRANSFORMER & RJ45	
22.POWER(SEQUENCE)	51.M.2 WLAN & BT	
23.FAN & THERMAL	52.M.2 WWAN	
24.APU FP5-1	53.DOCK CONNECTOR	
25.APU FP5-2	54.AUDIO CODEC	
26.APU FP5-3	55.SPEAKER & AUDIO JACK	
27.APU FP5-4	56.D/B CNTR & 12S SHUT DOWN	
28.APU FP5-5	57.POWER BUTTON D/B	
29.APU FP5-6		

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TITLE MODEL PROJECT FUNCTION
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIGNAL	VOTAGE	G3	S5	S3	S0	REMARK
P1V5A_RTC	1.5V	O	O	O	O	COIN BATTERY
PVBAT	19V	X	O	O	O	DC-IN ALWAYS
P3V3DS	3.3V	X	O	O	O	DC-IN ALWAYS
P5V0DS	5V	X	O	O	O	DC-IN ALWAYS
P3V3A	3.3V	X	O	O	O	
P1V8A	1.8V	X	O	O	O	
P0V9A	0.9V	X	O	O	O	
P2V5	2.5V	X	X	O	O	
P5V0A_USB	5V	X	X	O	O	
P1V2	1.2V	X	X	O	O	
P5V0S	5V	X	X	X	O	
P3V3S	3.3V	X	X	X	O	
P1V8S	1.8V	X	X	X	O	
P0V9S	0.9V	X	X	X	O	
P0V6S	0.6V	X	X	X	O	
PVCORE_NB	SVC/SVD	X	X	X	O	
PVCORE	SVC/SVD	X	X	X	O	

INTERFACE	PORT ASSIGNMENT
USBC/DP#0	USB TYPE-C
USBC/DP#1	NA
USB3_0#1	WALK UP PORT0
USB3_0#2	WALK UP PORT1
USB3_1#0	DOCK PORT
GPP0	WWAN
GPP1	NIC
GPP2	WLAN
GPP3	NA
GPP4	M.2 SSD
GPP5	M.2 SSD
GPP6	M.2 SSD
GPP7	M.2 SSD
DDI0	EDP
DDI1	HDMI / DOCK PORT
DDI2	DOCK PORT VGA
SATA0	NA
SATA1	M.2 SSD

USB 2.0	PORT ASSIGNMENT
USB2_0#0	USB TYPE-C
USB2_0#1	WALK UP PORT0
USB2_0#2	WALK UP PORT1
USB2_0#3	DOCK PORT
USB2_1#0	USB2.0 HUB
USB2_1#1	CAMERA

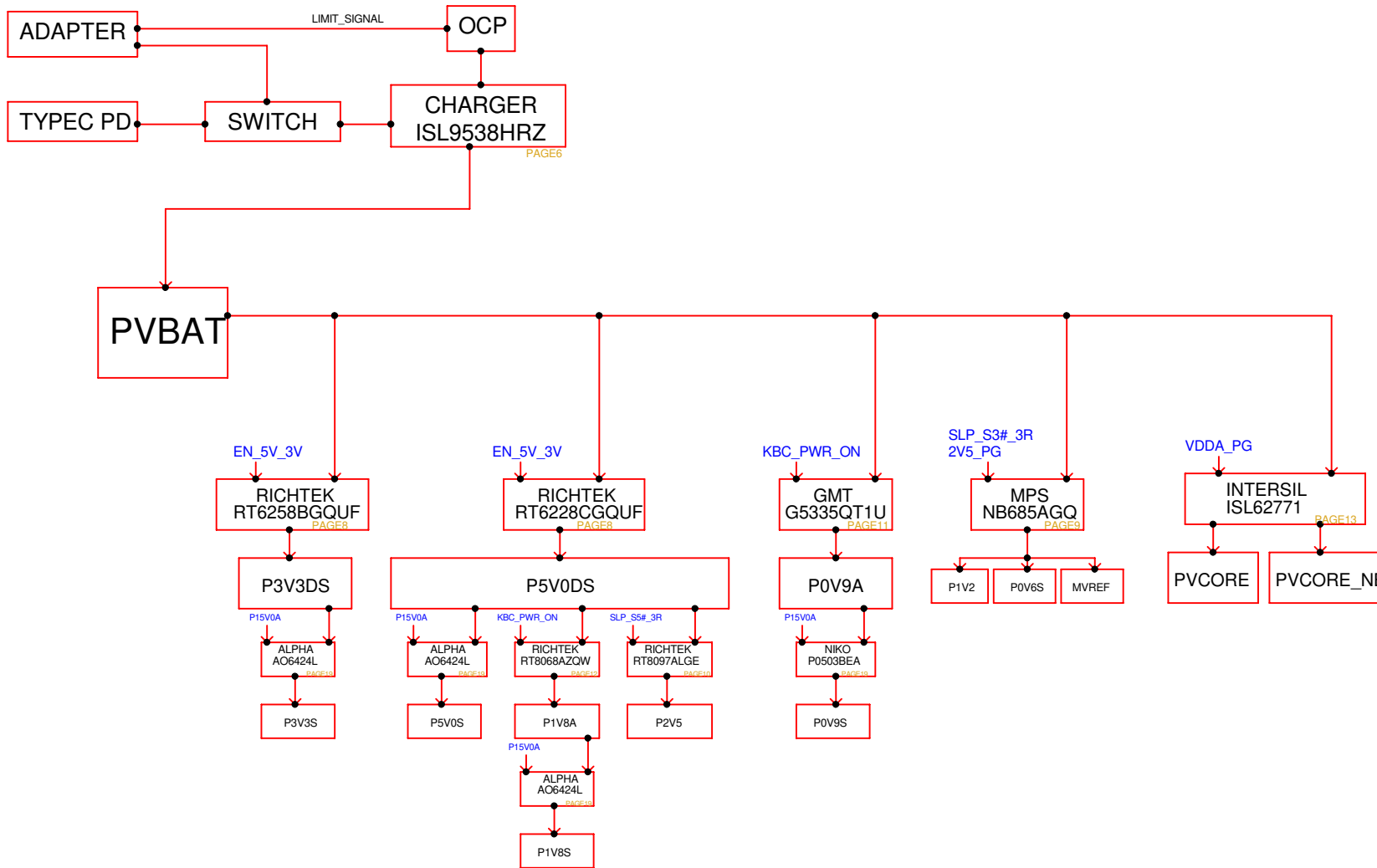
INVENTEC

TITLE: MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxxxx PCB VER: XXX

SHEET 4 of 66

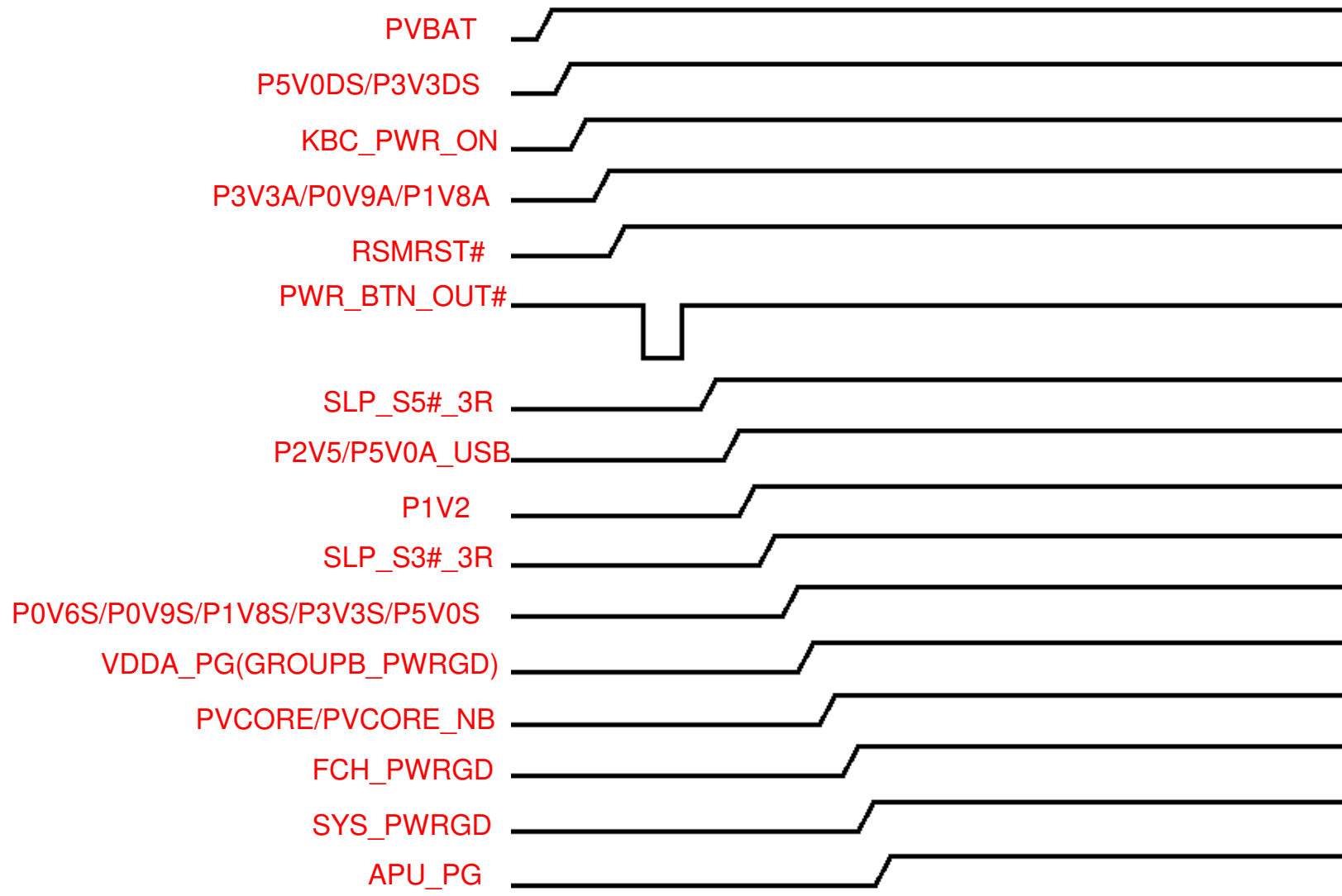


INVENTEC

TITLE			
MODEL PROJECT FUNCTION BLOCK DIAGRAM POWER			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

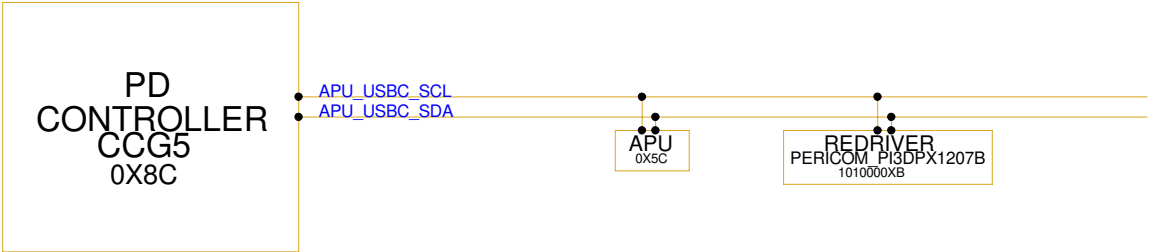
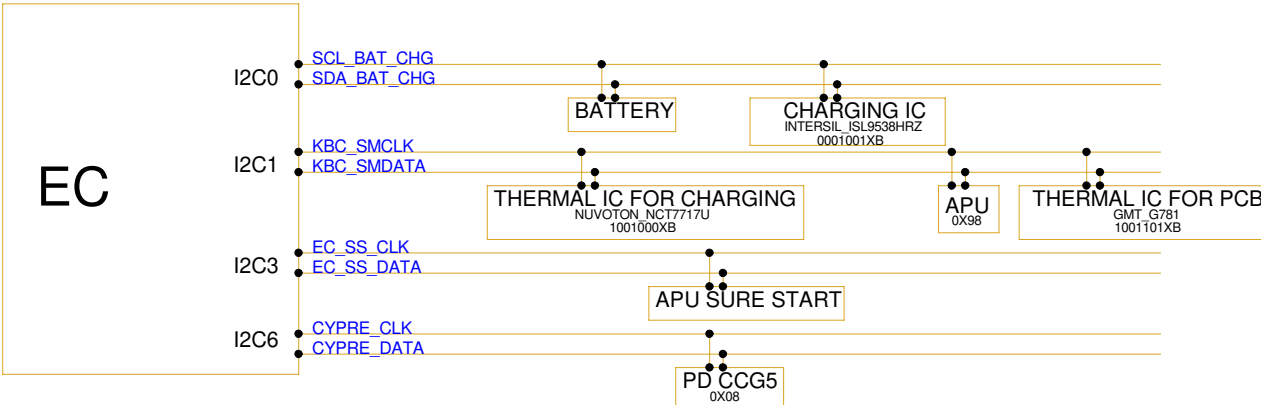
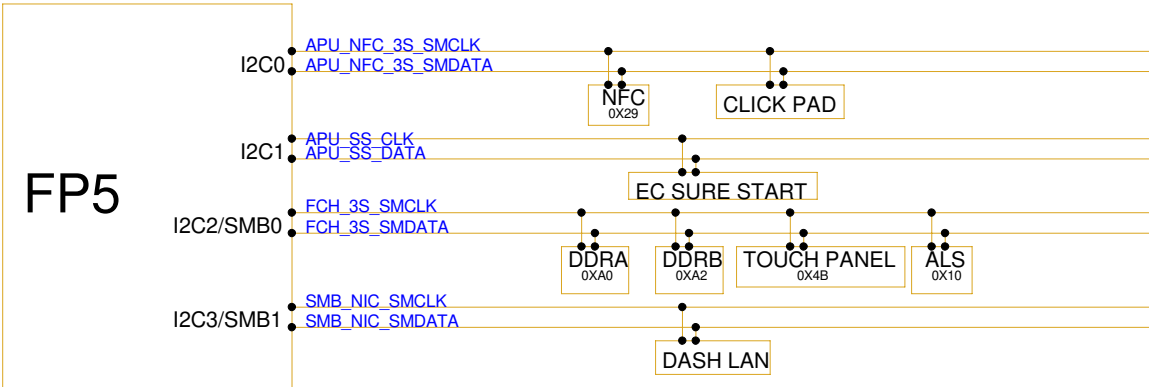
D
C
B
A



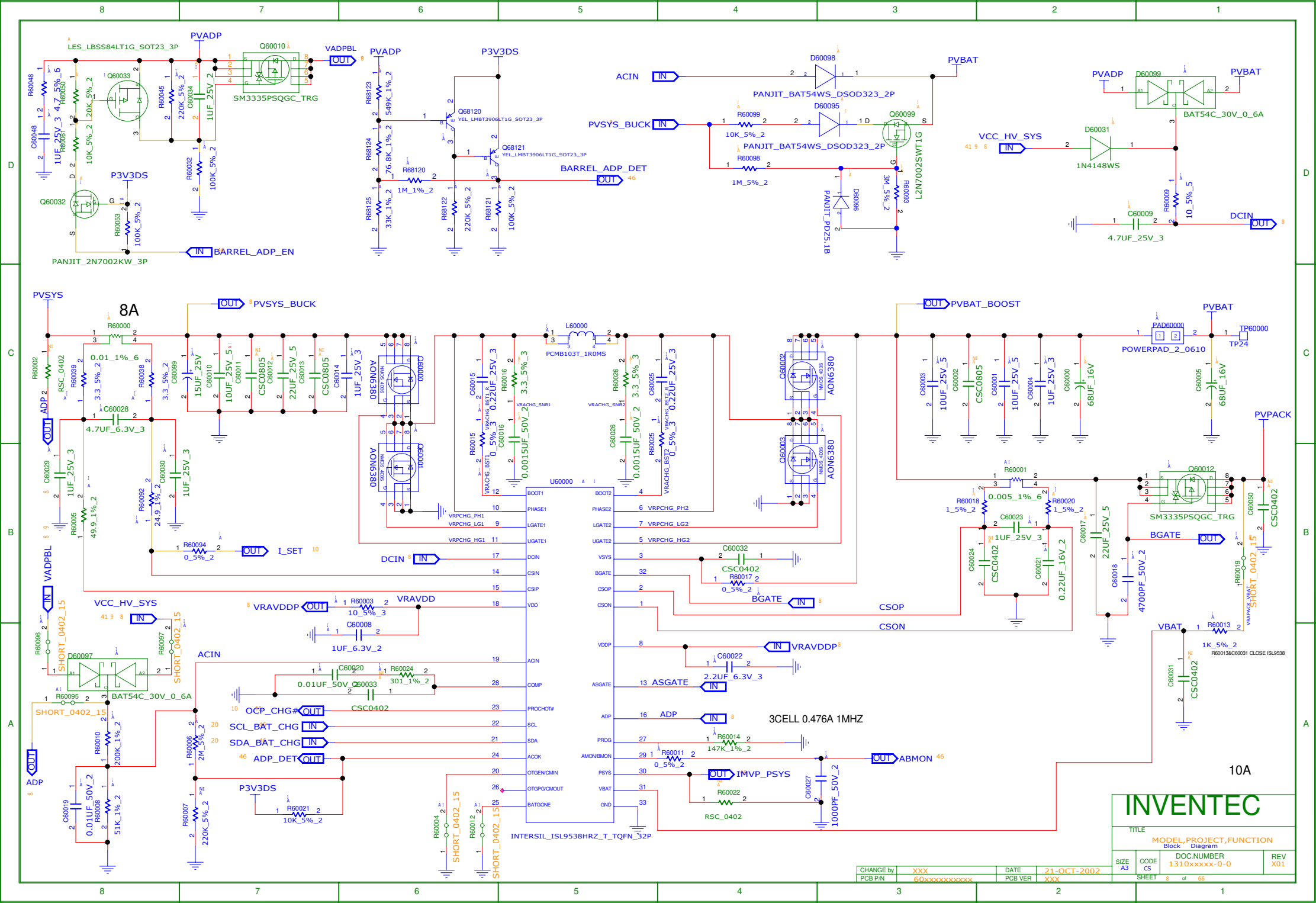
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TITLE			
MODEL,PROJECT,FUNCTION SEQUENCE			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310XXXX-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
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INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

10A

3CELL 0.476A 1MHZ

INTERSIL_ISL9538HRZ_T_TQFN_32P

SM3335PSQGC_TRG

PANJIT_2N7002KW_3P

SM3335PSQGC_TRG

LES_LBSS84LT1G_SOT23_3P

Q60010

Q60032

Q60033

Q60034

Q60035

Q60036

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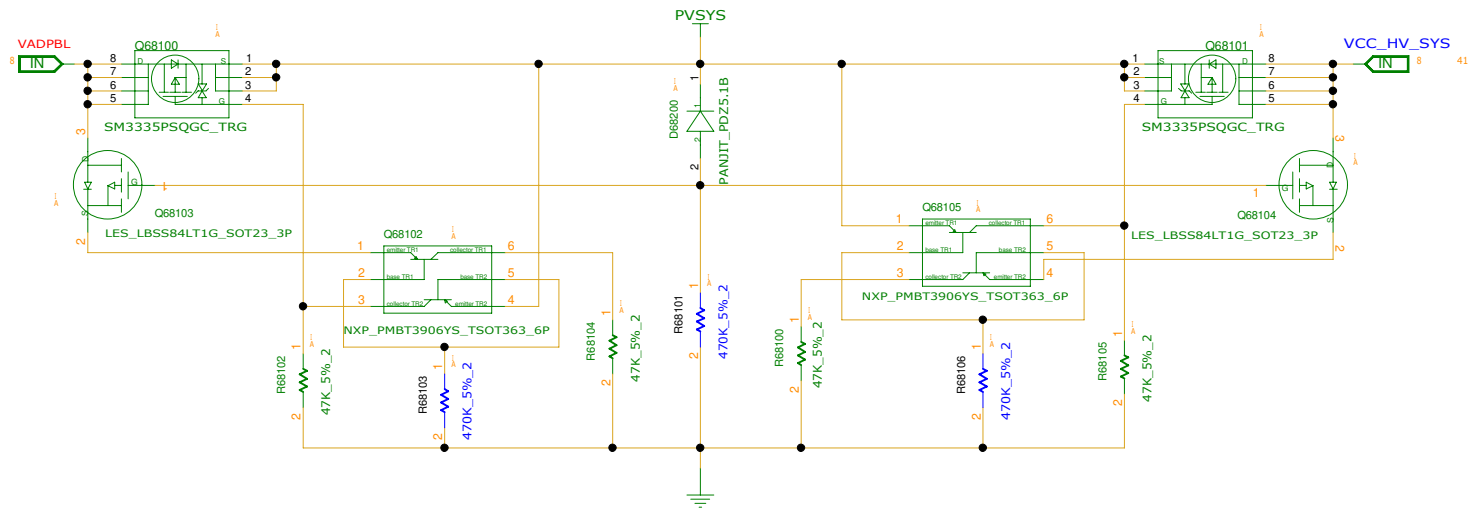
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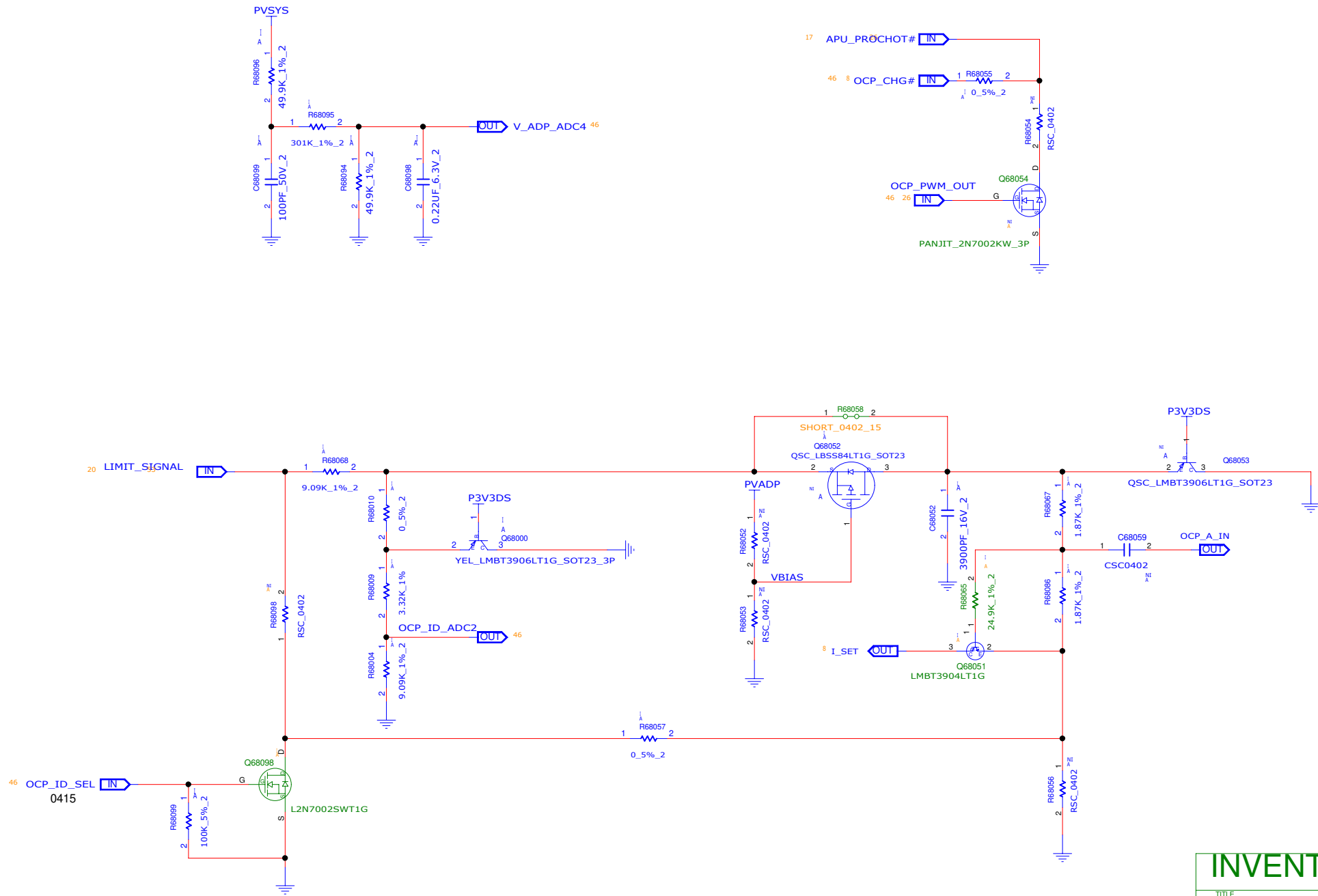
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INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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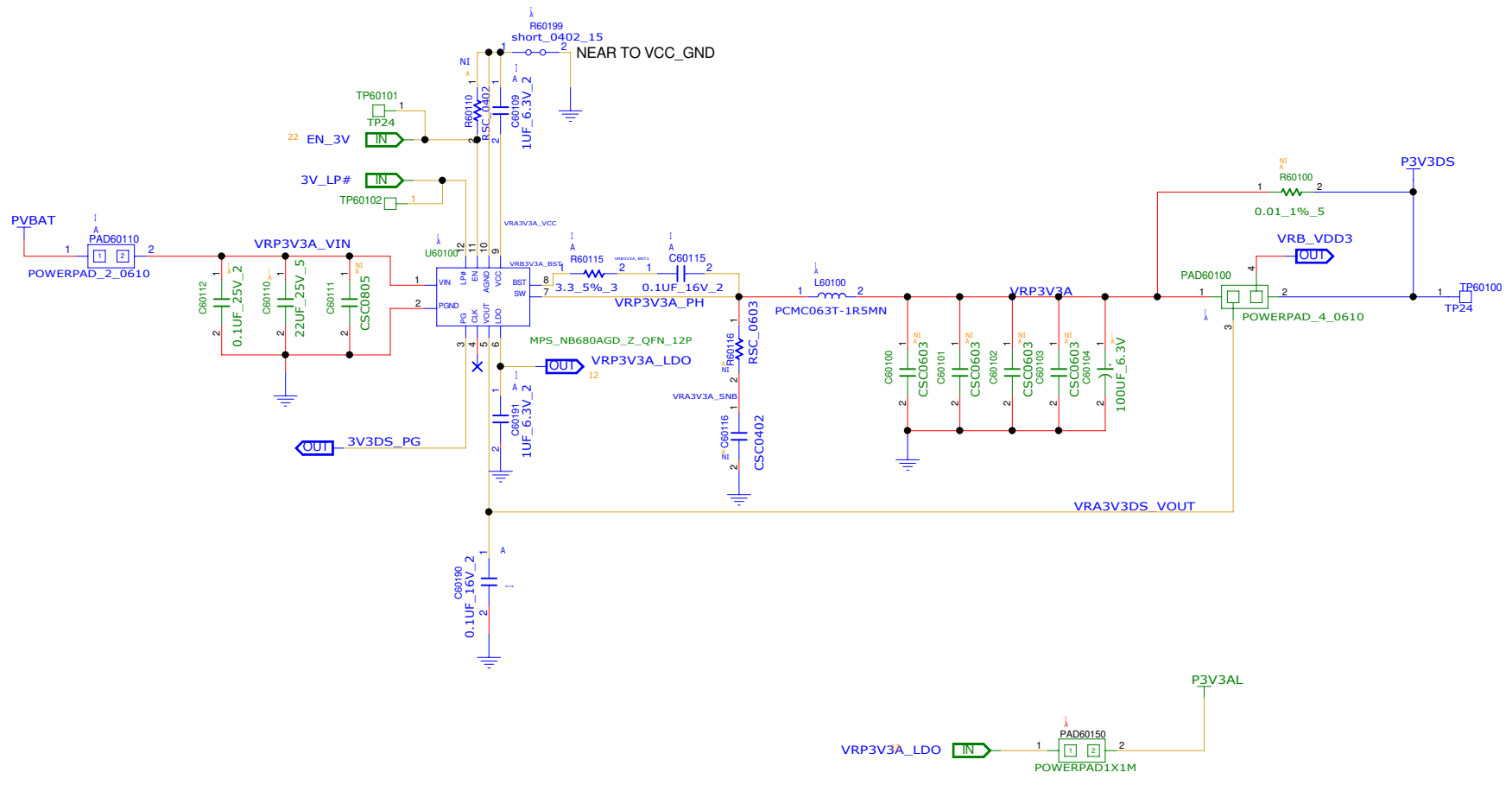
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PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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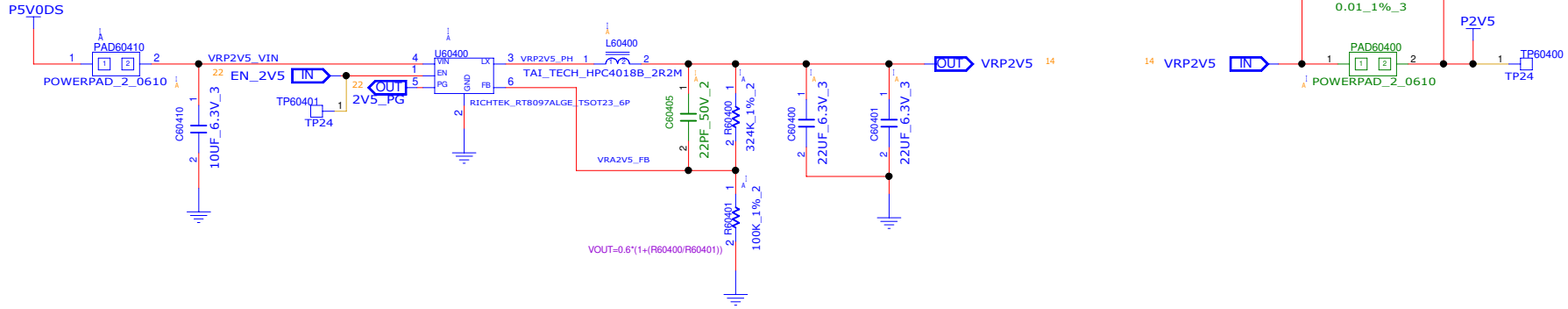
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PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

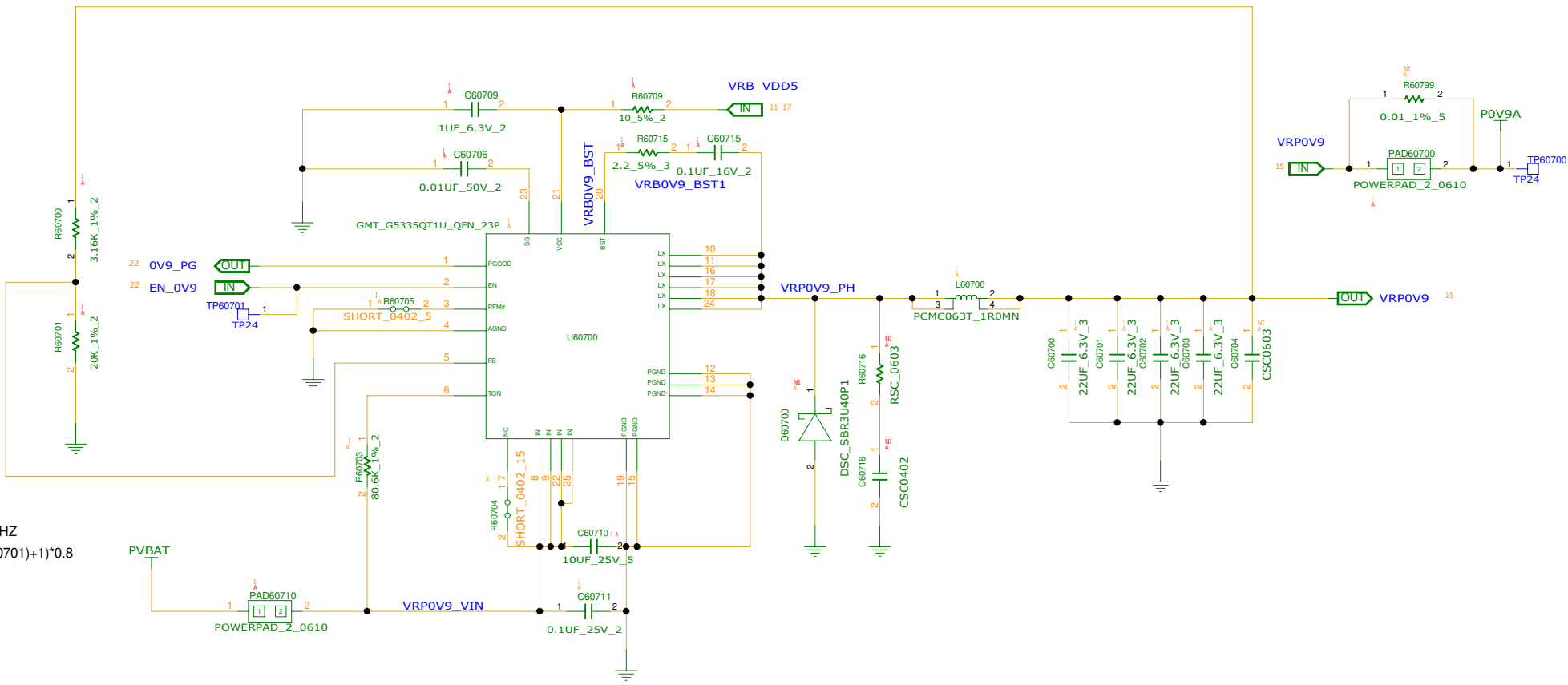


INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

F_{SW}=500KHZ
 $VO = ((R60700/R60701)+1) * 0.8$



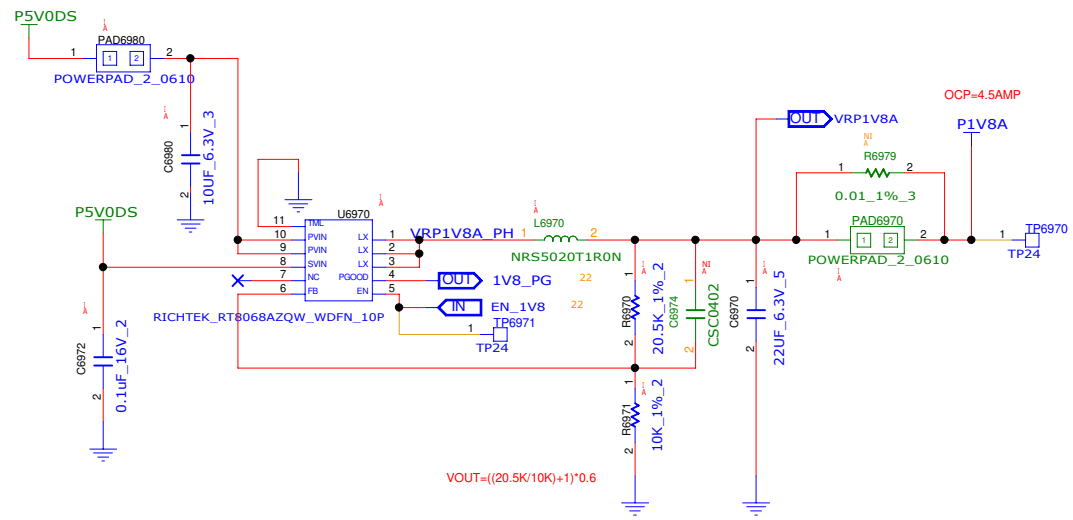
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TITLE: MODEL, PROJECT, FUNCTION
 Block Diagram

DOC NUMBER: 1310xxxx-0-0
 REV: X01

SIZE: A3
 CODE: CS
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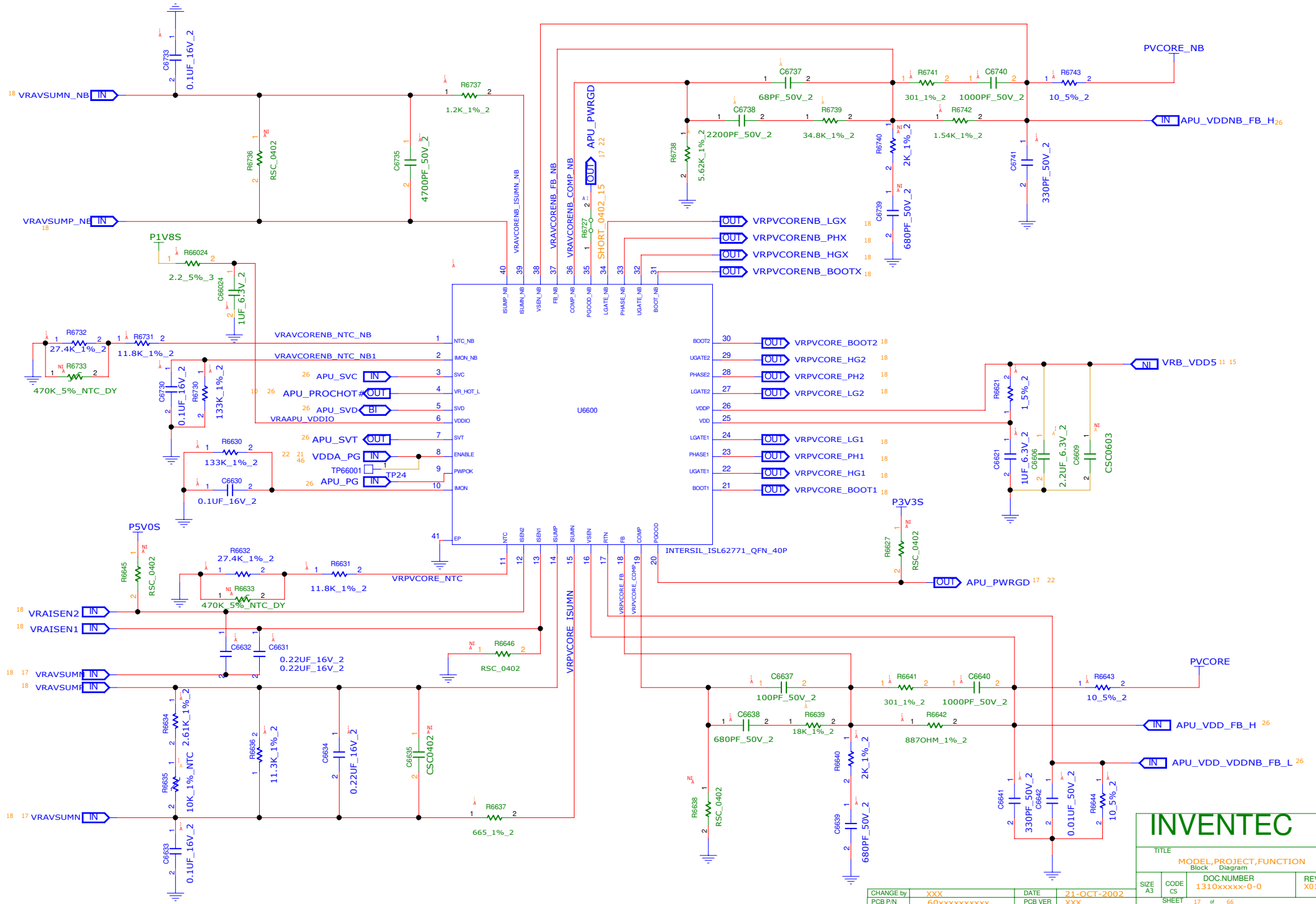
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX



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TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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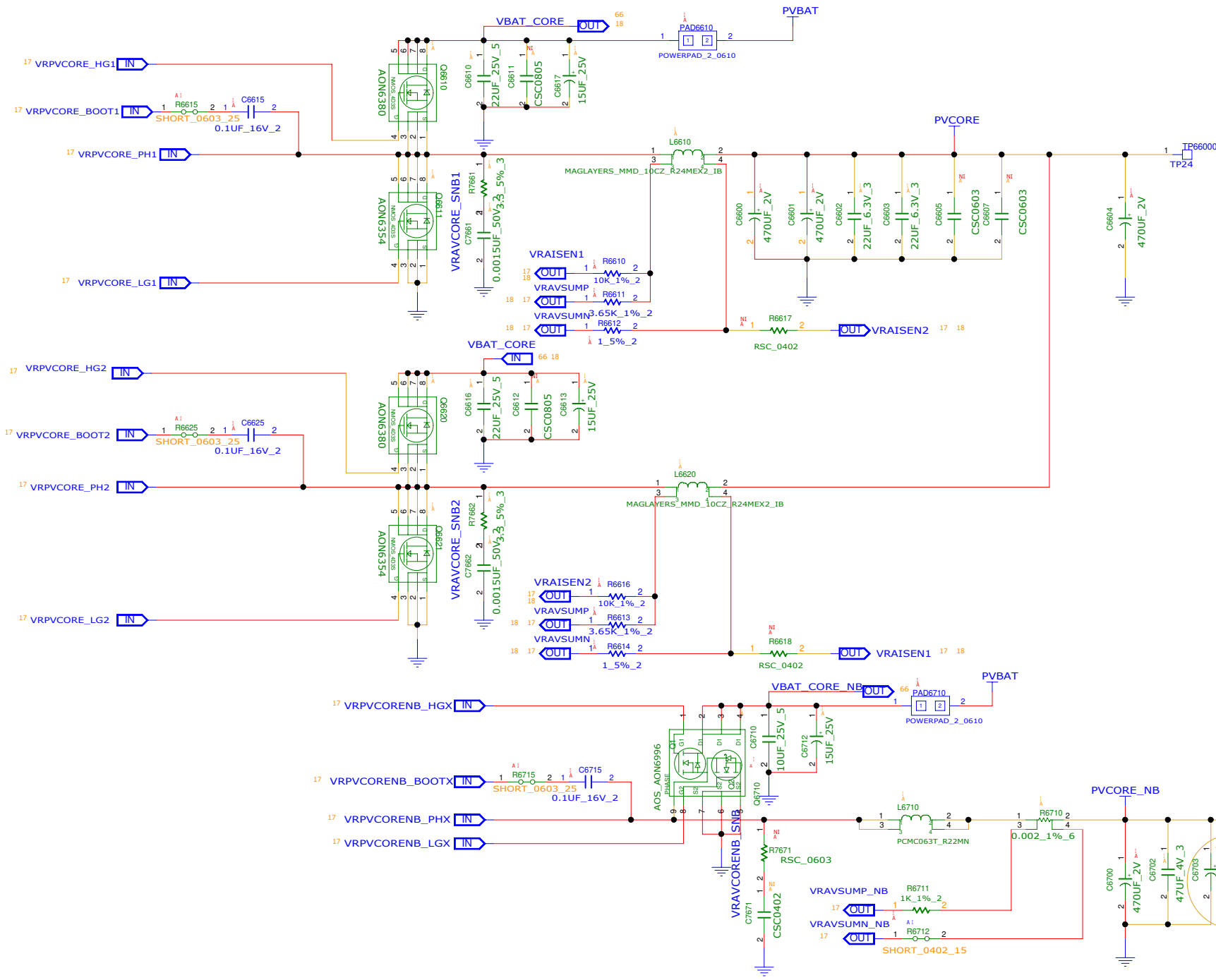
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3		CODE CS	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
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CLOSE TO CPU

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		18 of 66	

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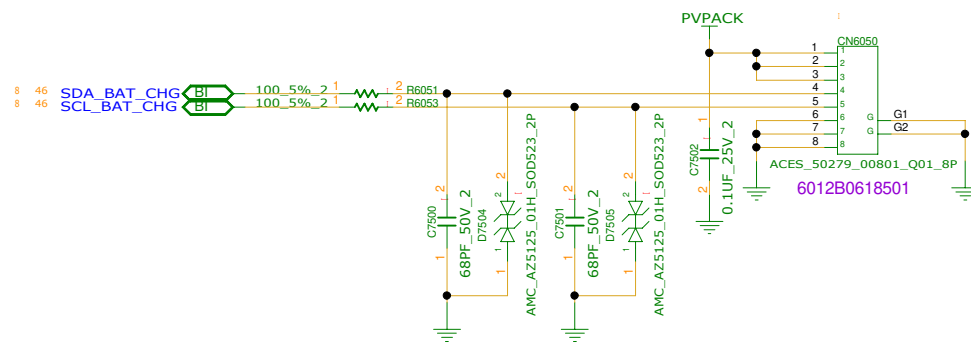
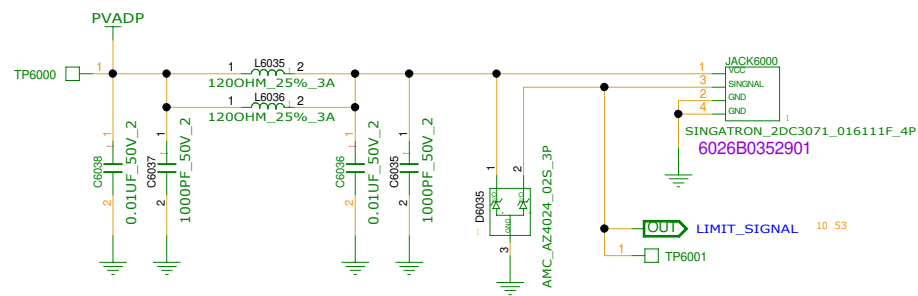
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CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC NUMBER	REV
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	19 of 66	1310xxxxx-0-0	X01

TITLE
MODEL,PROJECT,FUNCTION
NA

SIZE A3
CODE CS
SHEET 19 of 66

DOC NUMBER
1310xxxxx-0-0
REV
X01

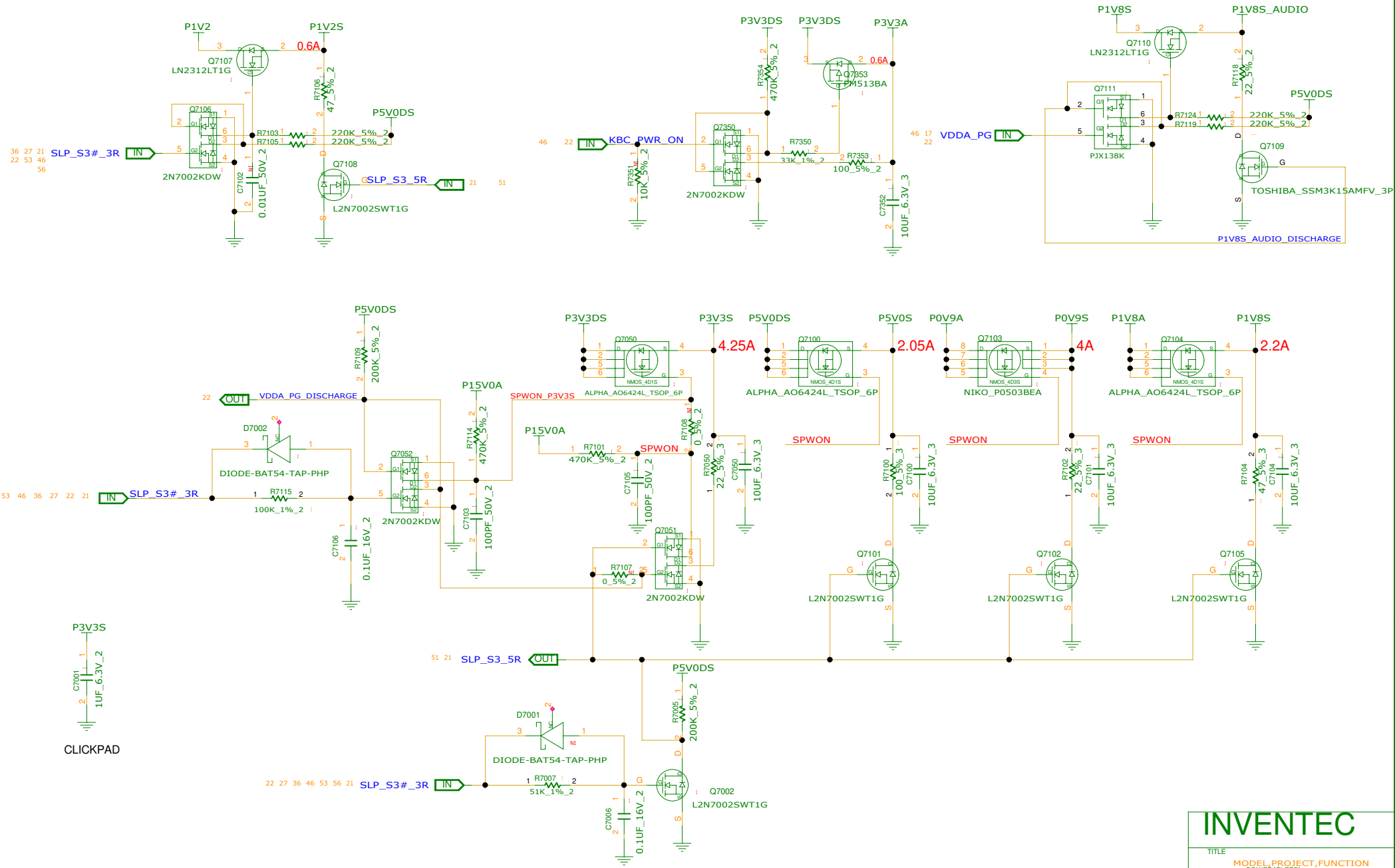


INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
DC JACK & BATTERY CNTR			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

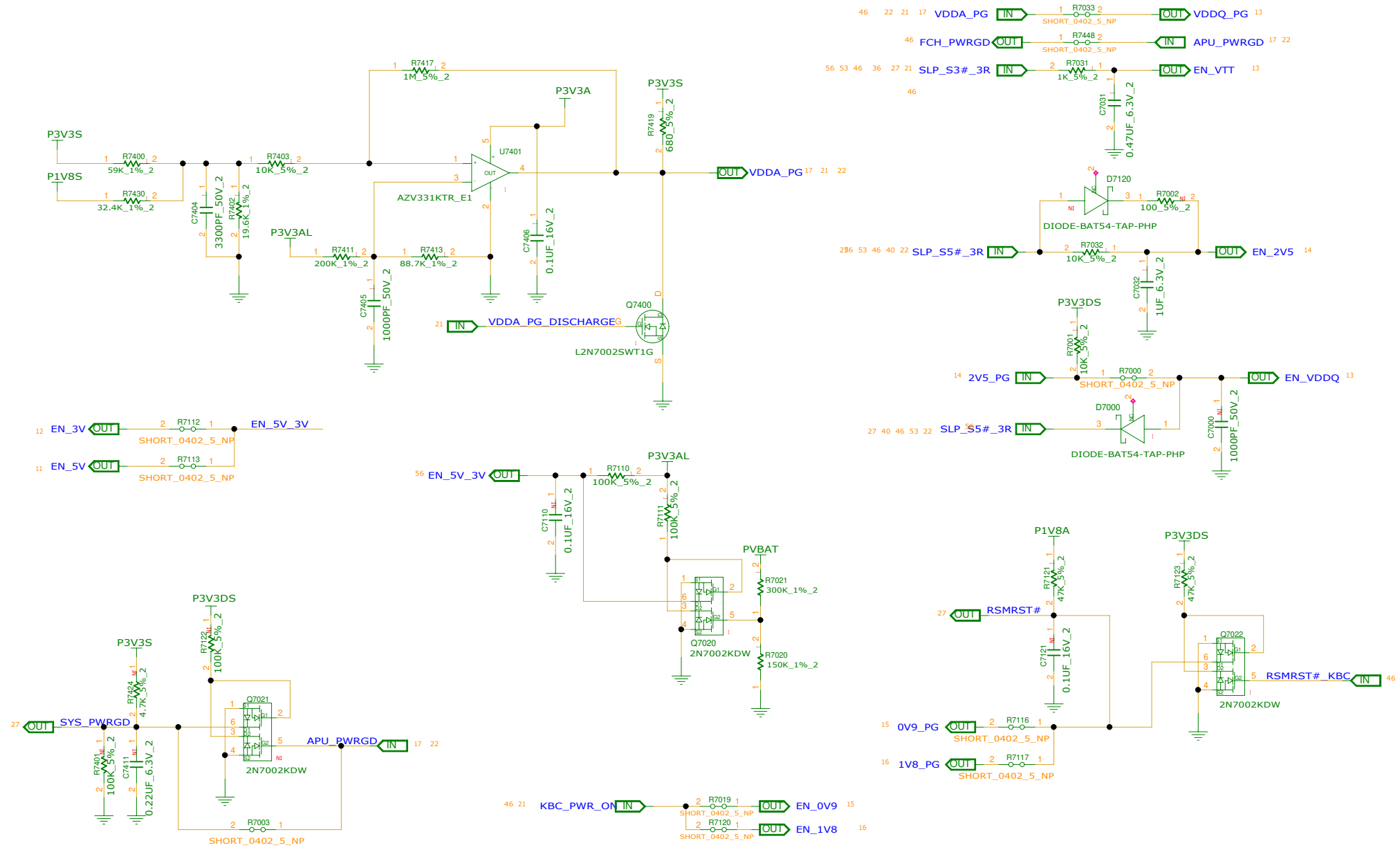
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INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
POWER(SLEEP)			
DOC NUMBER			
1310xxxxx-0-0			
SIZE	CODE	REV	
A3	CS	X01	
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PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

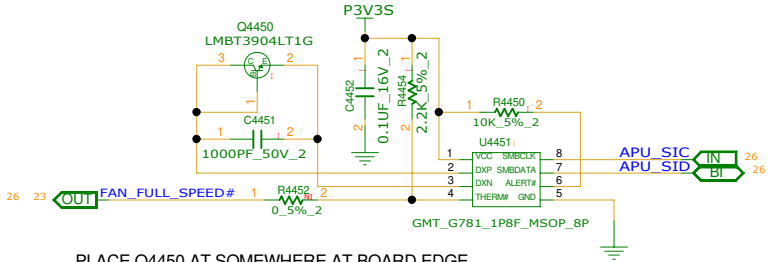
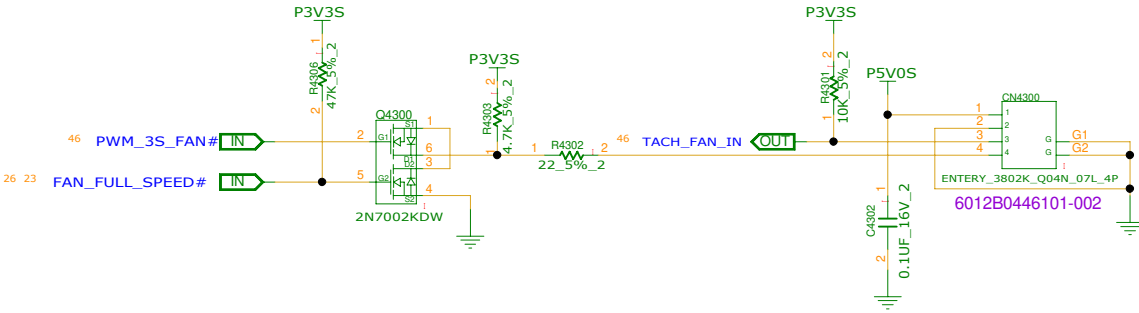


INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
POWER SEQUENCE			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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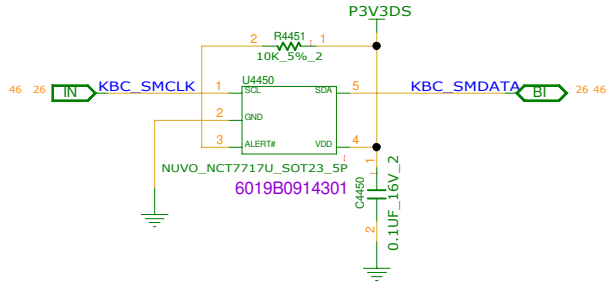
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PLACE Q4450 AT SOMEWHERE AT BOARD EDGE

PLACE U4451 AT BOTTOM SIDE AND CLOSED TO CPU
BUT NOT INTERFERE WITH HIGH SPEED ROUTINGS

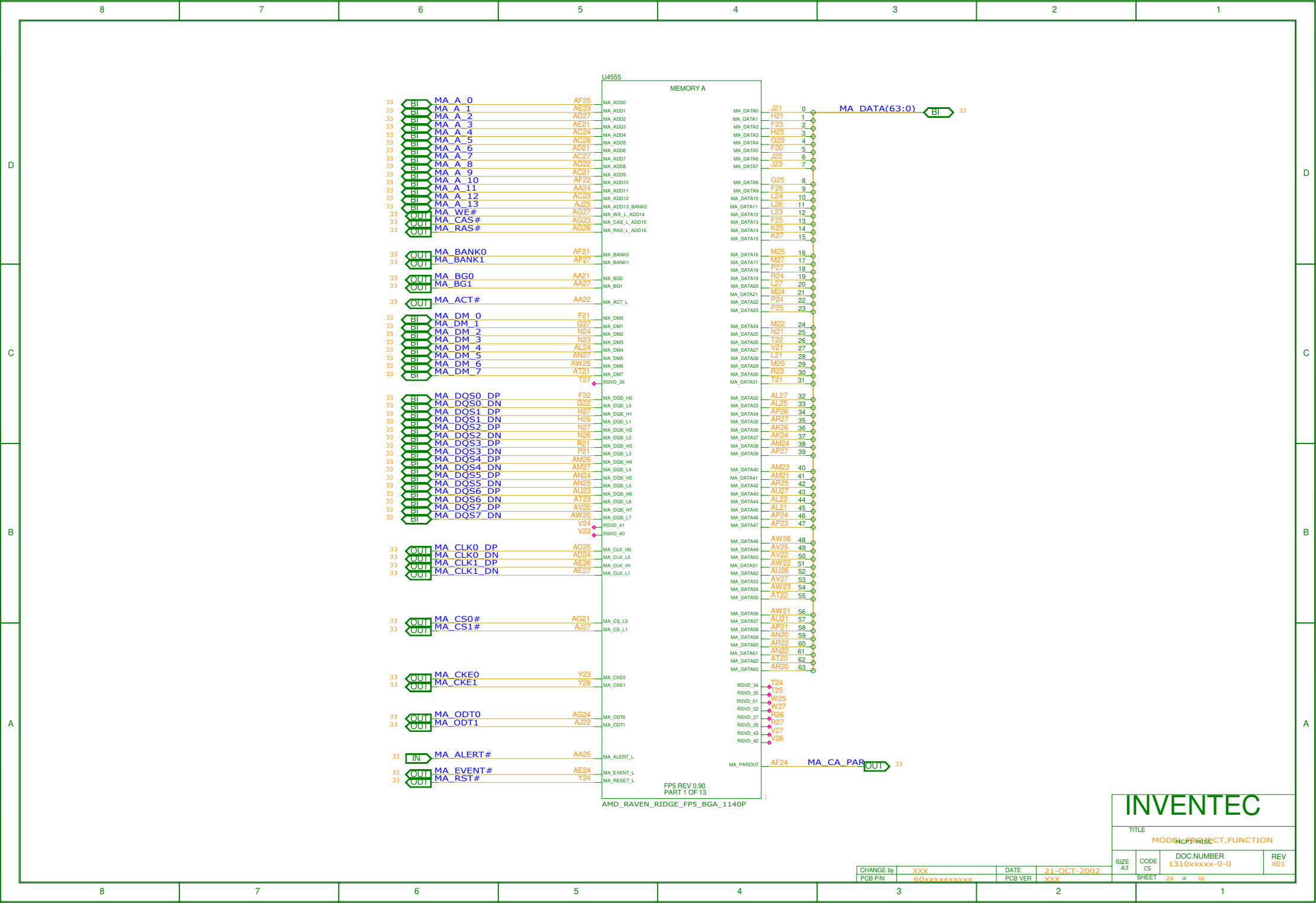
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INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
FAN & THERMAL			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



U4555
MEMORY A

33	BI	MA_A 0	AF25	MA_ADD0	MA_DATA0	J21	0	MA_DATA(63:0)	BI	33
33	BI	MA_A 1	AE23	MA_ADD1	MA_DATA1	H21	1			
33	BI	MA_A 2	AD27	MA_ADD2	MA_DATA2	F23	2			
33	BI	MA_A 3	AE21	MA_ADD3	MA_DATA3	H23	3			
33	BI	MA_A 4	AC24	MA_ADD4	MA_DATA4	G20	4			
33	BI	MA_A 5	AC26	MA_ADD5	MA_DATA5	F20	5			
33	BI	MA_A 6	AD21	MA_ADD6	MA_DATA6	J22	6			
33	BI	MA_A 7	AC27	MA_ADD7	MA_DATA7	J23	7			
33	BI	MA_A 8	AD22	MA_ADD8						
33	BI	MA_A 9	AC21	MA_ADD9						
33	BI	MA_A 10	AF22	MA_ADD10	MA_DATA8	G25	8			
33	BI	MA_A 11	AA24	MA_ADD11	MA_DATA9	F26	9			
33	BI	MA_A 12	AC23	MA_ADD12	MA_DATA10	L24	10			
33	BI	MA_A 13	AJ25	MA_ADD13_BANK2	MA_DATA11	L26	11			
33	OUT	MA_WE#	AG27	MA_WE_L_ADD14	MA_DATA12	L23	12			
33	OUT	MA_CAS#	AG23	MA_CAS_L_ADD15	MA_DATA13	F25	13			
33	OUT	MA_RAS#	AG26	MA_RAS_L_ADD16	MA_DATA14	K25	14			
					MA_DATA15	K27	15			
33	OUT	MA_BANK0	AF21	MA_BANK0	MA_DATA16	M25	16			
33	OUT	MA_BANK1	AF27	MA_BANK1	MA_DATA17	M27	17			
33	OUT	MA_BG0	AA21	MA_BG0	MA_DATA18	P27	18			
33	OUT	MA_BG1	AA27	MA_BG1	MA_DATA19	R24	19			
33	OUT	MA_ACT#	AA22	MA_ACT_L	MA_DATA20	L27	20			
					MA_DATA21	M24	21			
33	BI	MA_DM 0	F21	MA_DM0	MA_DATA22	P24	22			
33	BI	MA_DM 1	G27	MA_DM1	MA_DATA23	F25	23			
33	BI	MA_DM 2	N24	MA_DM2						
33	BI	MA_DM 3	N23	MA_DM3	MA_DATA24	M22	24			
33	BI	MA_DM 4	AL24	MA_DM4	MA_DATA25	N21	25			
33	BI	MA_DM 5	AN27	MA_DM5	MA_DATA26	T22	26			
33	BI	MA_DM 6	AW25	MA_DM6	MA_DATA27	V21	27			
33	BI	MA_DM 7	AT21	MA_DM7	MA_DATA28	L21	28			
			T27	RSVD_36	MA_DATA29	M20	29			
					MA_DATA30	R23	30			
					MA_DATA31	T21	31			
33	BI	MA_DQS0 DP	F23	MA_DQS_H0	MA_DATA32	AL27	32			
33	BI	MA_DQS0 DN	G22	MA_DQS_L0	MA_DATA33	AL25	33			
33	BI	MA_DQS1 DP	H27	MA_DQS_H1	MA_DATA34	AP26	34			
33	BI	MA_DQS1 DN	H26	MA_DQS_L1	MA_DATA35	AR27	35			
33	BI	MA_DQS2 DP	N27	MA_DQS_H2	MA_DATA36	AK26	36			
33	BI	MA_DQS2 DN	N26	MA_DQS_L2	MA_DATA37	AK24	37			
33	BI	MA_DQS3 DP	R21	MA_DQS_H3	MA_DATA38	AM24	38			
33	BI	MA_DQS3 DN	F21	MA_DQS_L3	MA_DATA39	AP27	39			
33	BI	MA_DQS4 DP	AM26	MA_DQS_H4						
33	BI	MA_DQS4 DN	AM27	MA_DQS_L4	MA_DATA40	AM23	40			
33	BI	MA_DQS5 DP	AN24	MA_DQS_H5	MA_DATA41	AM21	41			
33	BI	MA_DQS5 DN	AN25	MA_DQS_L5	MA_DATA42	AR25	42			
33	BI	MA_DQS6 DP	AU23	MA_DQS_H6	MA_DATA43	AU27	43			
33	BI	MA_DQS6 DN	AT23	MA_DQS_L6	MA_DATA44	AL22	44			
33	BI	MA_DQS7 DP	AV20	MA_DQS_H7	MA_DATA45	AL21	45			
33	BI	MA_DQS7 DN	AW20	MA_DQS_L7	MA_DATA46	AP24	46			
			V24	RSVD_41	MA_DATA47	AP23	47			
			V23	RSVD_40						
33	OUT	MA_CLK0 DP	AD25	MA_CLK_H0	MA_DATA48	AW26	48			
33	OUT	MA_CLK0 DN	AD24	MA_CLK_L0	MA_DATA49	AV25	49			
33	OUT	MA_CLK1 DP	AE26	MA_CLK_H1	MA_DATA50	AV22	50			
33	OUT	MA_CLK1 DN	AE27	MA_CLK_L1	MA_DATA51	AW22	51			
					MA_DATA52	AU26	52			
					MA_DATA53	AV27	53			
					MA_DATA54	AW23	54			
					MA_DATA55	AT22	55			
33	OUT	MA_CS0#	AG21	MA_CS_L0	MA_DATA56	AW21	56			
33	OUT	MA_CS1#	AJ27	MA_CS_L1	MA_DATA57	AU21	57			
					MA_DATA58	AP21	58			
					MA_DATA59	AN20	59			
					MA_DATA60	AR22	60			
					MA_DATA61	AN22	61			
					MA_DATA62	AT20	62			
					MA_DATA63	AR20	63			
33	OUT	MA_CKE0	Y23	MA_CKE0	RSVD_34	T24				
33	OUT	MA_CKE1	Y26	MA_CKE1	RSVD_35	T25				
					RSVD_51	W25				
					RSVD_52	W27				
					RSVD_27	R26				
					RSVD_28	R27				
					RSVD_43	V26				
					RSVD_42	V26				
33	IN	MA_ALERT#	AA25	MA_ALERT_L	MA_PAROUT	AF24				
33	OUT	MA_EVENT#	AE24	MA_EVENT_L						
33	OUT	MA_RST#	Y24	MA_RESET_L						

FP5 REV 0.90
PART 1 OF 13

AMD_RAVEN_RIDGE_FP5_BGA_1140P

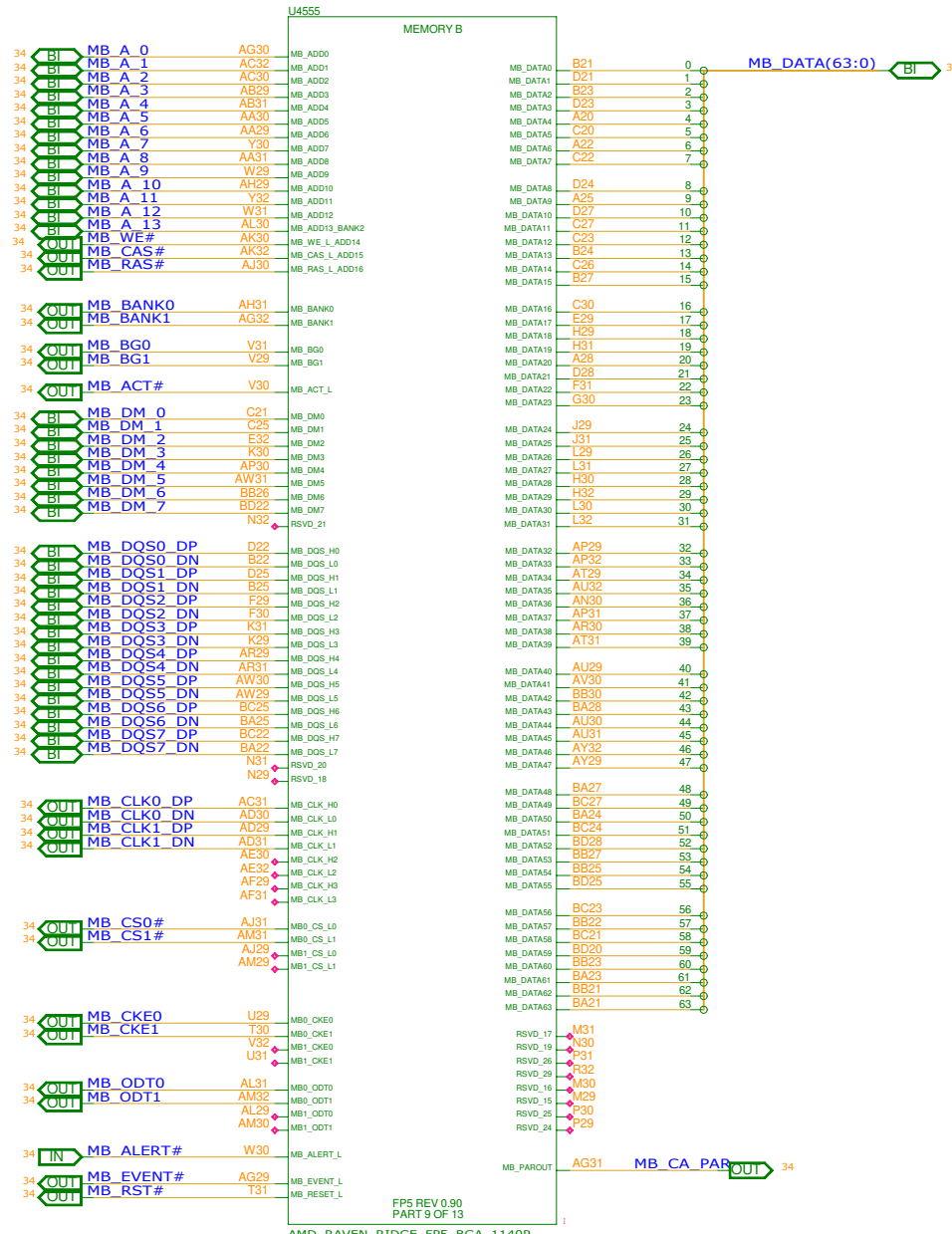
INVENTEC

TITLE: **MODEM PCIE**
MODE: **MODEM PCIE, FUNCTION**

SIZE A3 CODE CS DOC NUMBER 1310XXXX-0-0 REV X01

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60XXXXXXXXXX PCB VER: XXX

SHEET 24 of 66



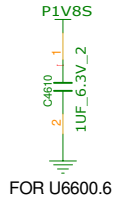
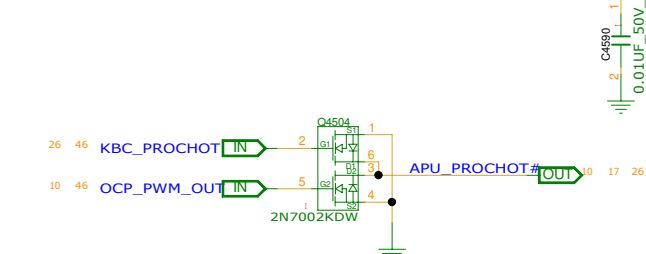
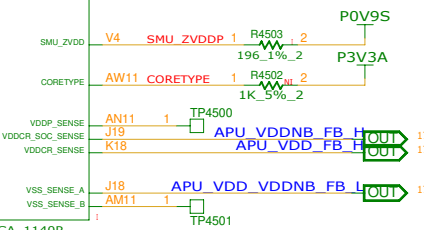
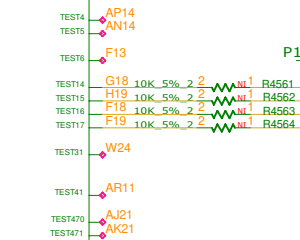
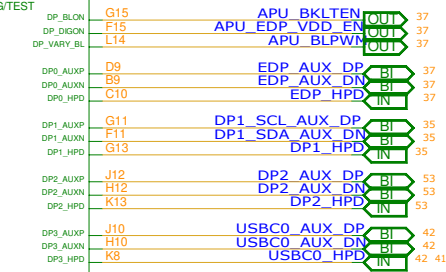
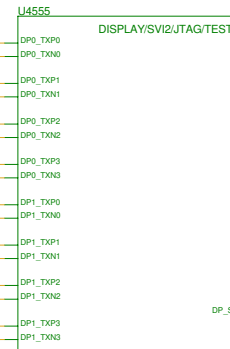
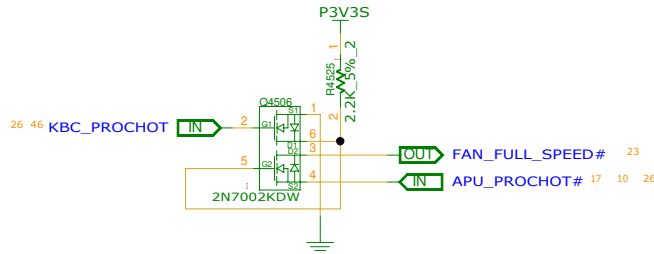
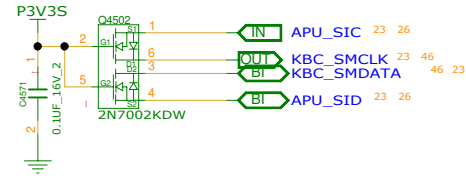
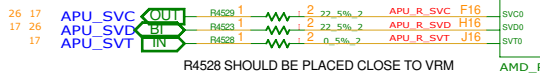
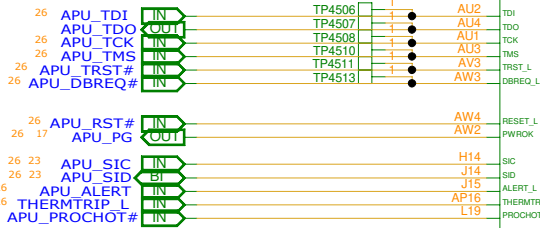
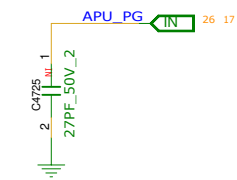
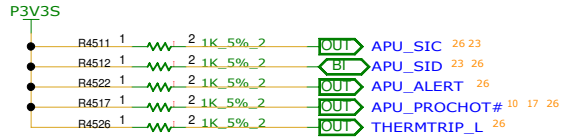
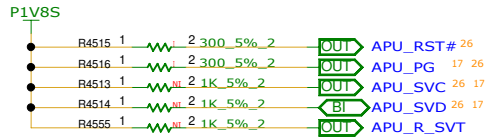
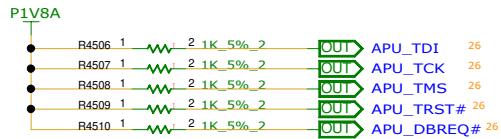
FPS REV 0.90
PART 9 OF 13
AMD_RAVEN_RIDGE_FPS_BGA_1140P

INVENTEC

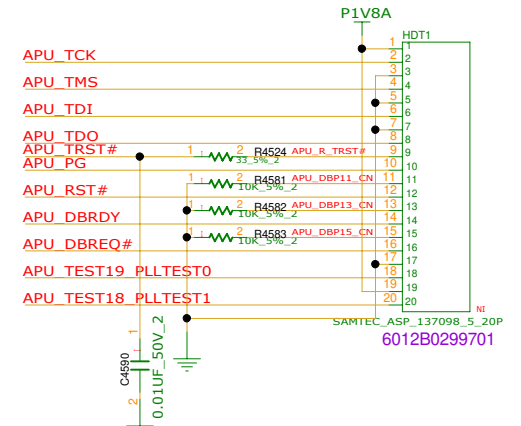
TITLE
MCP2542 USB & SYSTEM SEQUENCE

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01
SHEET 25 of 66

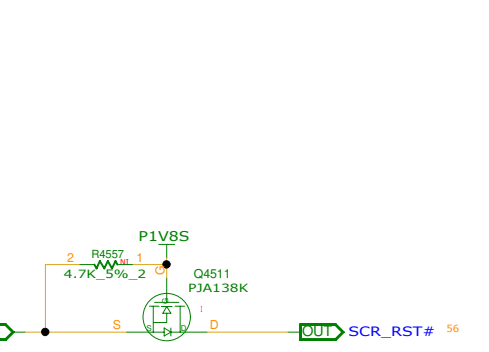
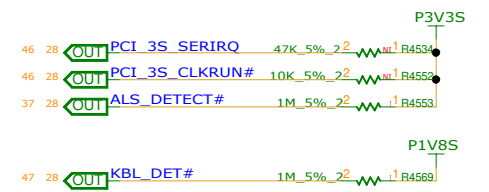
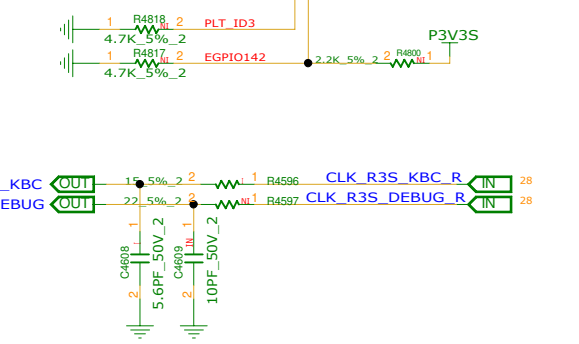
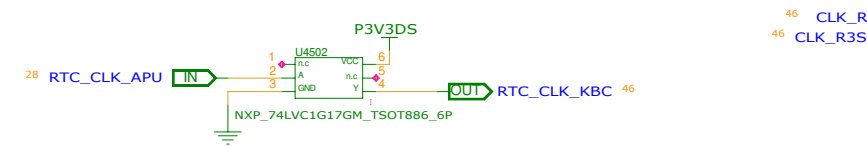
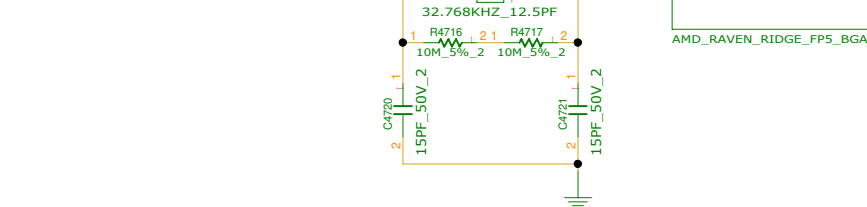
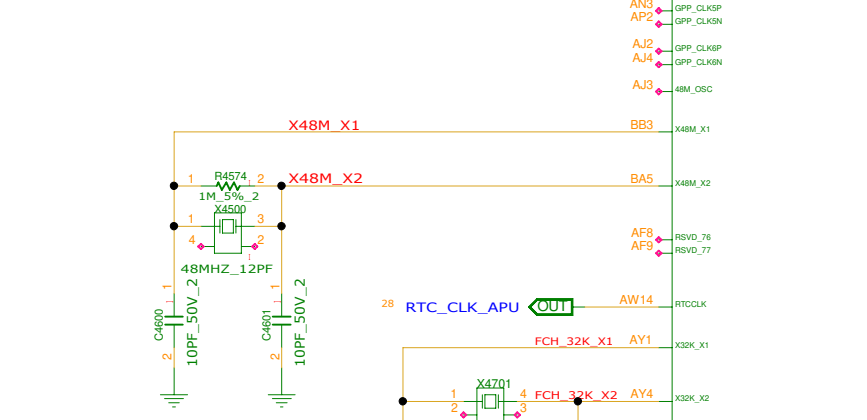
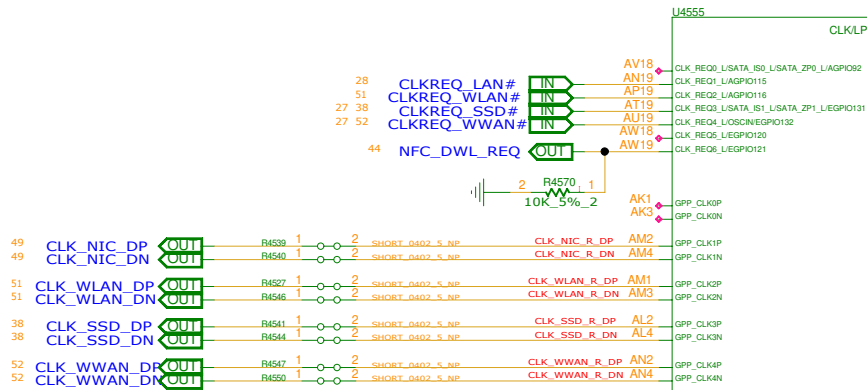
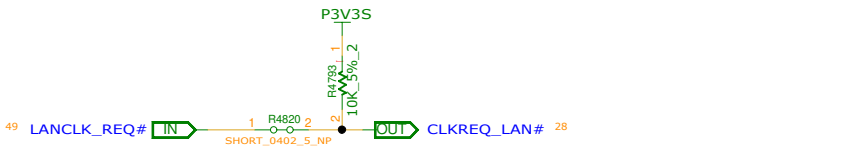
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



PU FOR INTERNAL PD FOR CUSTOMER



INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		26 of 66	



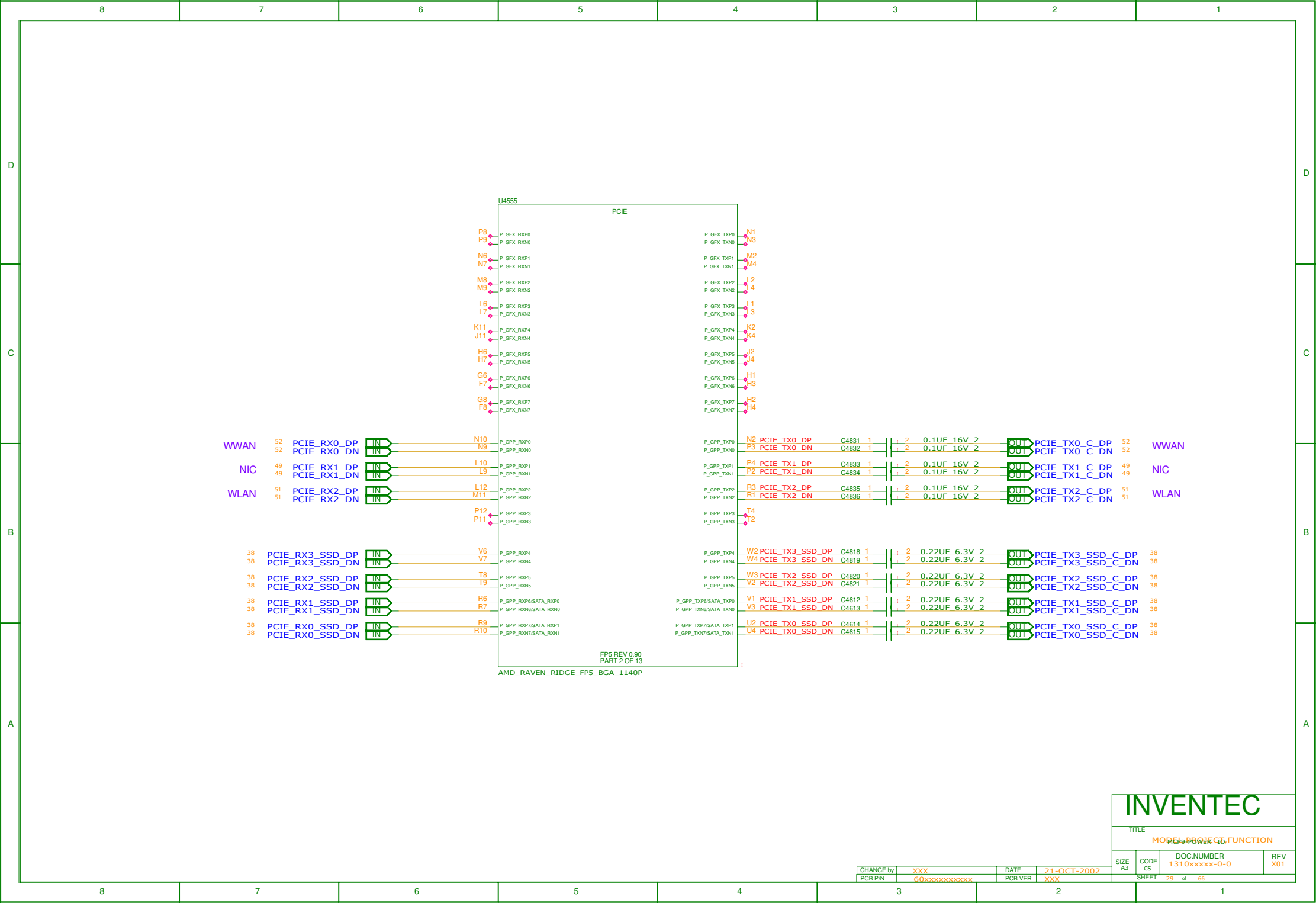
PLATFORM ID	P_ID1 EGPIO141 INTERNAL PD	P_ID2 EGPIO142 INTERNAL PH	P_ID3 EGPIO143 INTERNAL PH
LLARGA13"	0	0	1
TENJIN 14"	0	1	0
TENJIN 15"	0	1	1

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
MCP5-DDR

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 28 of 66			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



Ref	Component	Value	Part	QTY	Value	Vol	Cur	Dir	Ref	Component	Value	Part	QTY	Value	Vol	Cur	Dir	Ref
52	PCIE_RX0_DP	IN	N10	P_GPP_RXP0	P2	PCIE TX0 DP	C4831	1	1	2	0.1UF	16V	2	OUT	PCIE_TX0_C_DP	52	WWAN	
52	PCIE_RX0_DN	IN	N9	P_GPP_RXN0	P3	PCIE TX0 DN	C4832	1	1	2	0.1UF	16V	2	OUT	PCIE_TX0_C_DN	52	WWAN	
49	PCIE_RX1_DP	IN	L10	P_GPP_RXP1	P4	PCIE TX1 DP	C4833	1	1	2	0.1UF	16V	2	OUT	PCIE_TX1_C_DP	49	NIC	
49	PCIE_RX1_DN	IN	L9	P_GPP_RXN1	P2	PCIE TX1 DN	C4834	1	1	2	0.1UF	16V	2	OUT	PCIE_TX1_C_DN	49	NIC	
51	PCIE_RX2_DP	IN	L12	P_GPP_RXP2	R3	PCIE TX2 DP	C4835	1	1	2	0.1UF	16V	2	OUT	PCIE_TX2_C_DP	51	WLAN	
51	PCIE_RX2_DN	IN	M11	P_GPP_RXN2	R1	PCIE TX2 DN	C4836	1	1	2	0.1UF	16V	2	OUT	PCIE_TX2_C_DN	51	WLAN	
38	PCIE_RX3_SSD_DP	IN	V6	P_GPP_RXP4	W2	PCIE TX3 SSD DP	C4818	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX3_SSD_C_DP	38		
38	PCIE_RX3_SSD_DN	IN	V7	P_GPP_RXN4	W4	PCIE TX3 SSD DN	C4819	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX3_SSD_C_DN	38		
38	PCIE_RX2_SSD_DP	IN	T8	P_GPP_RXP5	W3	PCIE TX2 SSD DP	C4820	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX2_SSD_C_DP	38		
38	PCIE_RX2_SSD_DN	IN	T9	P_GPP_RXN5	V2	PCIE TX2 SSD DN	C4821	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX2_SSD_C_DN	38		
38	PCIE_RX1_SSD_DP	IN	R6	P_GPP_RXP6/SATA_RXP0	V1	PCIE TX1 SSD DP	C4612	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX1_SSD_C_DP	38		
38	PCIE_RX1_SSD_DN	IN	H7	P_GPP_RXN6/SATA_RXN0	V3	PCIE TX1 SSD DN	C4613	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX1_SSD_C_DN	38		
38	PCIE_RX0_SSD_DP	IN	R9	P_GPP_RXP7/SATA_RXP1	U2	PCIE TX0 SSD DP	C4614	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX0_SSD_C_DP	38		
38	PCIE_RX0_SSD_DN	IN	R10	P_GPP_RXN7/SATA_RXN1	U4	PCIE TX0 SSD DN	C4615	1	1	2	0.22UF	6.3V	2	OUT	PCIE_TX0_SSD_C_DN	38		

FPS REV 0.90
PART 2 OF 13

AMD_RAVEN_RIDGE_FP5_BGA_1140P

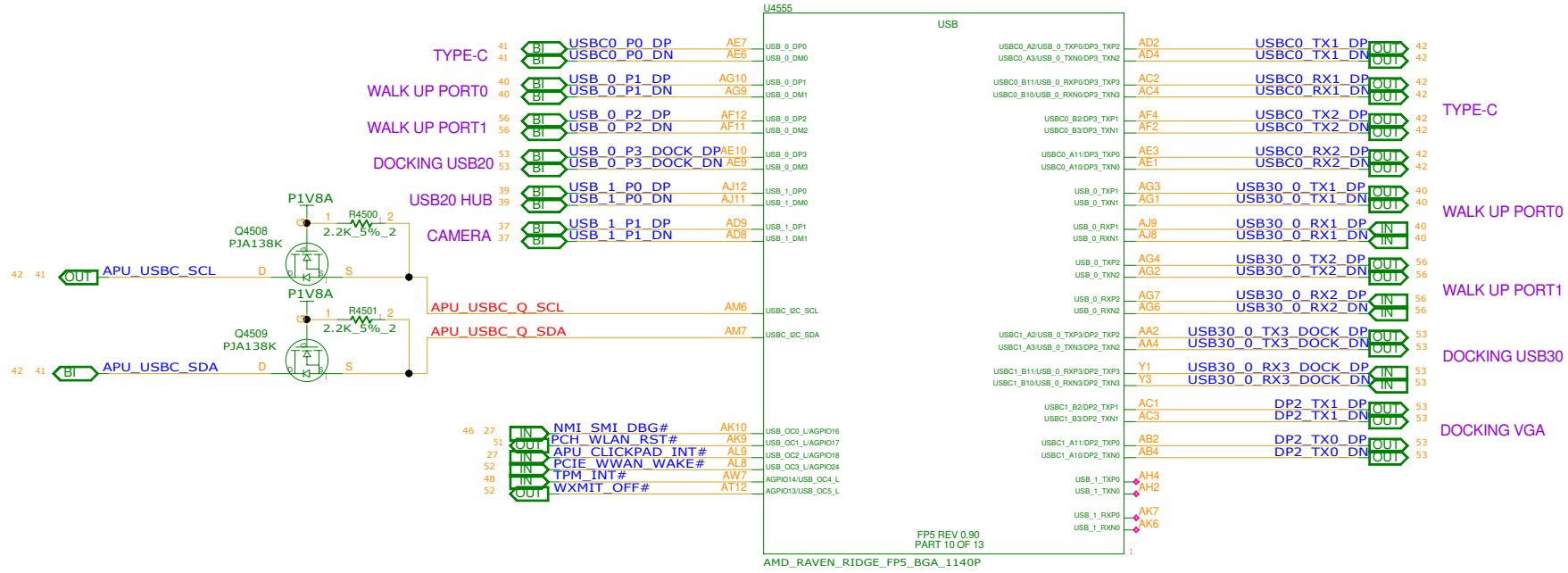
INVENTEC

TITLE: **MOBILE POWER CB FUNCTION**

SIZE A3 CODE CS DOC NUMBER 1310XXXX-0-0 REV X01

SHEET 29 of 66

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX



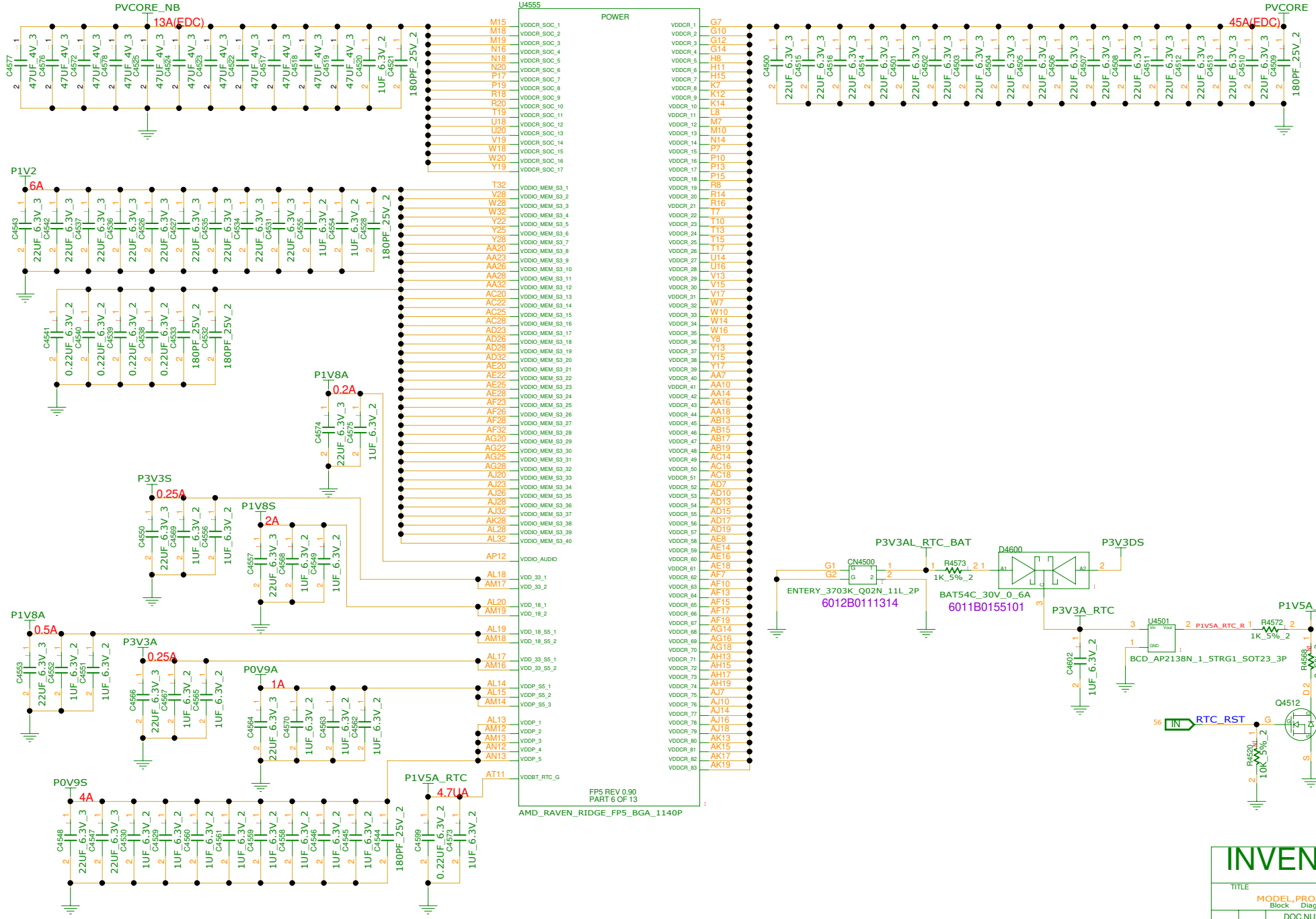
INVENTEC

TITLE: MCHP10 POWER/FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310XXXX-0-0 REV X01

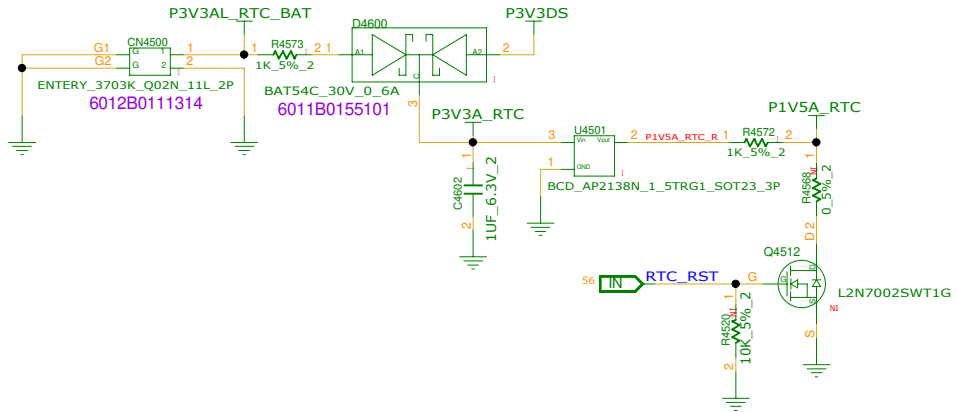
SHEET 30 of 66

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX



- U4555
- M15 VDDCR_SOC_1
 - M18 VDDCR_SOC_2
 - M19 VDDCR_SOC_3
 - N16 VDDCR_SOC_4
 - N18 VDDCR_SOC_5
 - N20 VDDCR_SOC_6
 - P17 VDDCR_SOC_7
 - R18 VDDCR_SOC_8
 - R19 VDDCR_SOC_9
 - R20 VDDCR_SOC_10
 - T19 VDDCR_SOC_11
 - U18 VDDCR_SOC_12
 - U28 VDDCR_SOC_13
 - V16 VDDCR_SOC_14
 - W18 VDDCR_SOC_15
 - W20 VDDCR_SOC_16
 - Y19 VDDCR_SOC_17
 - T32 VDDIO_MEM_S3_1
 - V28 VDDIO_MEM_S3_2
 - W28 VDDIO_MEM_S3_3
 - W32 VDDIO_MEM_S3_4
 - Y23 VDDIO_MEM_S3_5
 - Y25 VDDIO_MEM_S3_6
 - Y28 VDDIO_MEM_S3_7
 - AA20 VDDIO_MEM_S3_8
 - AA23 VDDIO_MEM_S3_9
 - AA26 VDDIO_MEM_S3_10
 - AA28 VDDIO_MEM_S3_11
 - AA32 VDDIO_MEM_S3_12
 - AC30 VDDIO_MEM_S3_13
 - AC33 VDDIO_MEM_S3_14
 - AC25 VDDIO_MEM_S3_15
 - AC28 VDDIO_MEM_S3_16
 - AD23 VDDIO_MEM_S3_17
 - AD26 VDDIO_MEM_S3_18
 - AD29 VDDIO_MEM_S3_19
 - AD33 VDDIO_MEM_S3_20
 - AE20 VDDIO_MEM_S3_21
 - AE22 VDDIO_MEM_S3_22
 - AE25 VDDIO_MEM_S3_23
 - AE28 VDDIO_MEM_S3_24
 - AF23 VDDIO_MEM_S3_25
 - AF26 VDDIO_MEM_S3_26
 - AF28 VDDIO_MEM_S3_27
 - AF32 VDDIO_MEM_S3_28
 - AG20 VDDIO_MEM_S3_29
 - AG22 VDDIO_MEM_S3_30
 - AG25 VDDIO_MEM_S3_31
 - AG28 VDDIO_MEM_S3_32
 - AJ20 VDDIO_MEM_S3_33
 - AJ23 VDDIO_MEM_S3_34
 - AJ26 VDDIO_MEM_S3_35
 - AJ28 VDDIO_MEM_S3_36
 - AJ32 VDDIO_MEM_S3_37
 - AK28 VDDIO_MEM_S3_38
 - AL28 VDDIO_MEM_S3_39
 - AL32 VDDIO_MEM_S3_40
 - AP12 VDDIO_AUDIO
 - AL18 VDDIO_18_1
 - AM17 VDDIO_18_2
 - AL20 VDDIO_18_5S_1
 - AM19 VDDIO_18_5S_2
 - AL19 VDDIO_33_5S_1
 - AM18 VDDIO_33_5S_2
 - AL17 VDDVP_SS_1
 - AM16 VDDVP_SS_2
 - AL14 VDDVP_SS_3
 - AM15 VDDVP_1
 - AM12 VDDVP_2
 - AM13 VDDVP_3
 - AN12 VDDVP_4
 - AM14 VDDVP_5
 - AT11 VDD0BT_RTC_G

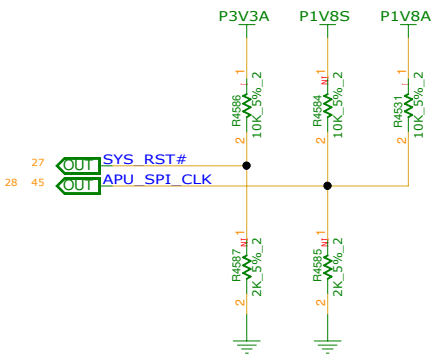
FP5 REV 0.90
PART 6 OF 13
AMD_RAVEN_RIDGE_FP5_BGA_1140P



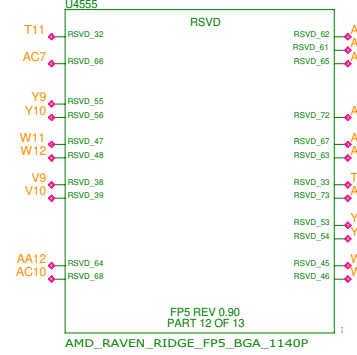
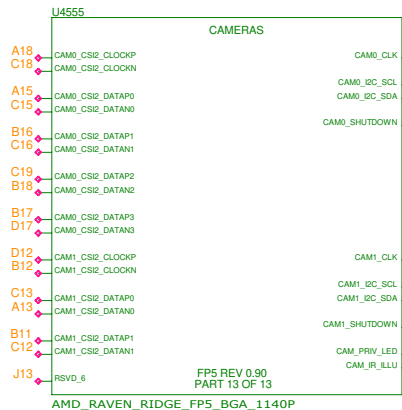
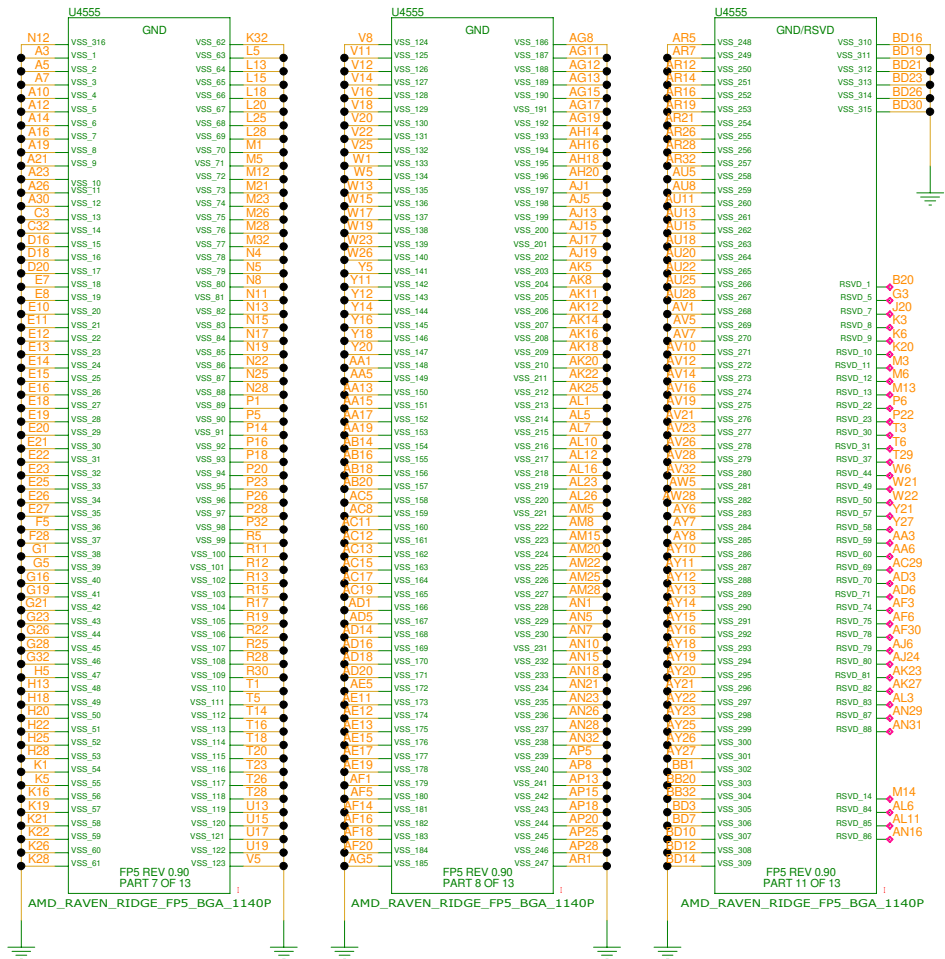
INVENTEC

TITLE				MODEL, PROJECT, FUNCTION	
Block Diagram				DOC NUMBER	
1310xxxx-0-0				REV	
X01				SHEET	
31 of 66					

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



STRAP	DEFINITION
SPL_CLK	1: USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0: USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#	1: NORMAL RESET MODE(DEFAULT) 0: SHORT RESET MODE



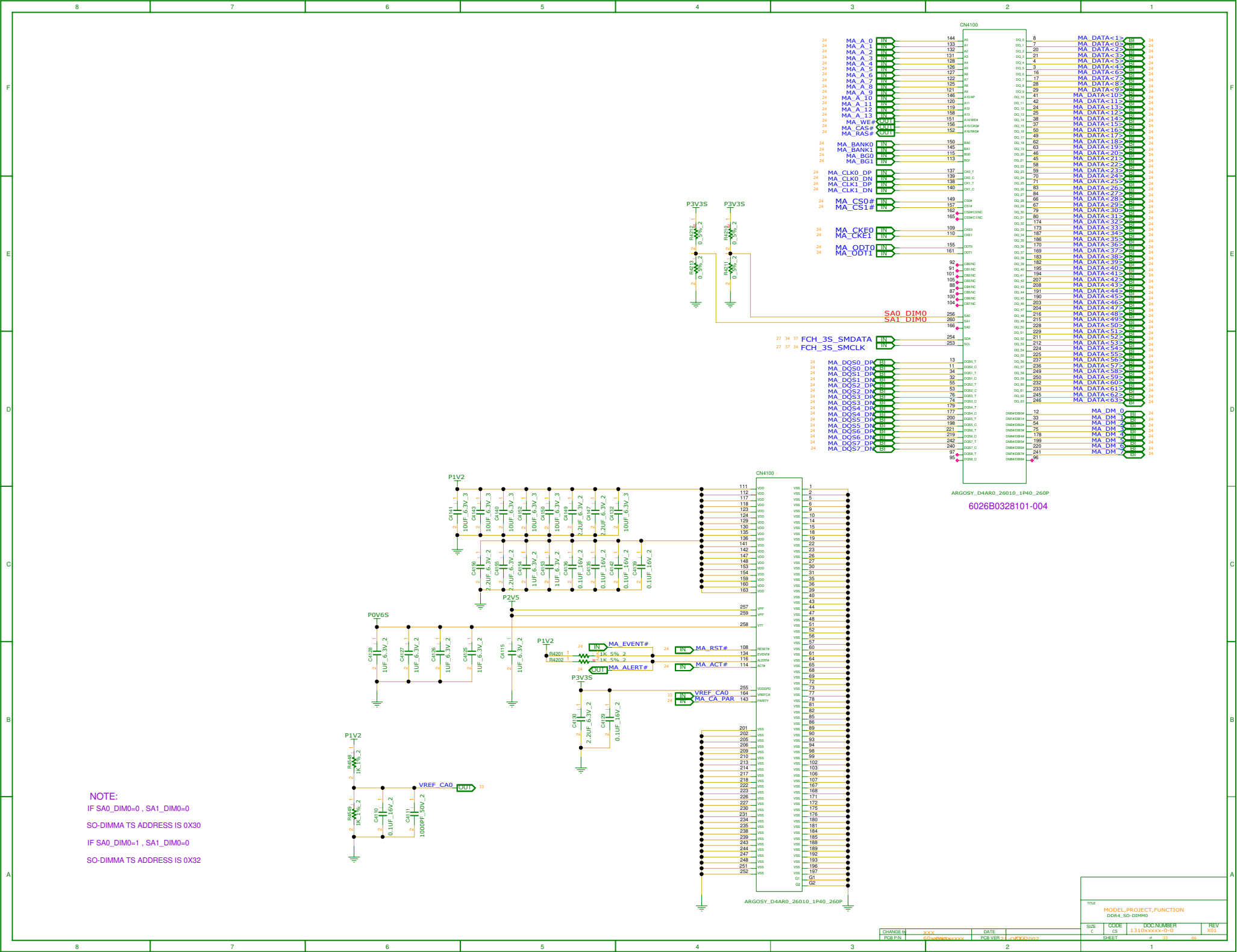
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TITLE: MODEM PCIE CONTROL FUNCTION

SIZE: A3 CODE: CS DOC NUMBER: 1310XXXX-0-0 REV: X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX



Pin	Signal Name	Direction	Internal Pin	Internal Name
24	MA_A_0	IN	144	AP
24	MA_A_1	IN	133	A1
24	MA_A_2	IN	132	A2
24	MA_A_3	IN	131	A3
24	MA_A_4	IN	128	A4
24	MA_A_5	IN	122	A5
24	MA_A_6	IN	127	A6
24	MA_A_7	IN	125	A7
24	MA_A_8	IN	121	A8
24	MA_A_9	IN	121	A9
24	MA_A_10	IN	146	AI0
24	MA_A_11	IN	120	A11
24	MA_A_12	IN	119	A12
24	MA_A_13	IN	158	A13
24	MA_A_14	IN	151	AI14WEF
24	MA_CAS#	IN	156	AI15CAS
24	MA_RAS#	IN	152	AI15RASP
24	MA_BANK0	IN	150	BA0
24	MA_BANK1	IN	145	BA1
24	MA_BG0	IN	115	BD0
24	MA_BG1	IN	113	BD1
24	MA_CLK0_DP	IN	137	CKL_T
24	MA_CLK0_DN	IN	138	CKL_C
24	MA_CLK1_DP	IN	138	CKL_T
24	MA_CLK1_DN	IN	140	CKL_C
24	MA_CS0#	IN	149	CSM
24	MA_CS1#	IN	157	CSM
24	MA_CS2#	IN	162	CSM
24	MA_CS3#	IN	165	CSM
24	MA_CS4#	IN	109	CSM
24	MA_CS5#	IN	110	CSM
24	MA_CS6#	IN	111	CSM
24	MA_CS7#	IN	155	CSM
24	MA_CS8#	IN	151	CSM
24	MA_CS9#	IN	82	CSM
24	MA_CS10#	IN	91	CSM
24	MA_CS11#	IN	101	CSM
24	MA_CS12#	IN	105	CSM
24	MA_CS13#	IN	88	CSM
24	MA_CS14#	IN	87	CSM
24	MA_CS15#	IN	100	CSM
24	MA_CS16#	IN	104	CSM
24	MA_CS17#	IN	94	CSM
24	MA_CS18#	IN	256	SAD
24	MA_CS19#	IN	166	SAD
24	MA_CS20#	IN	254	SAD
24	MA_CS21#	IN	253	SAD
24	MA_CS22#	IN	13	DS0
24	MA_CS23#	IN	11	DS0
24	MA_CS24#	IN	34	DS0
24	MA_CS25#	IN	32	DS0
24	MA_CS26#	IN	53	DS0
24	MA_CS27#	IN	55	DS0
24	MA_CS28#	IN	76	DS0
24	MA_CS29#	IN	74	DS0
24	MA_CS30#	IN	179	DS0
24	MA_CS31#	IN	177	DS0
24	MA_CS32#	IN	200	DS0
24	MA_CS33#	IN	198	DS0
24	MA_CS34#	IN	221	DS0
24	MA_CS35#	IN	219	DS0
24	MA_CS36#	IN	242	DS0
24	MA_CS37#	IN	240	DS0
24	MA_CS38#	IN	97	DS0
24	MA_CS39#	IN	95	DS0
24	MA_CS40#	IN	12	DM0
24	MA_CS41#	IN	33	DM0
24	MA_CS42#	IN	54	DM0
24	MA_CS43#	IN	75	DM0
24	MA_CS44#	IN	178	DM0
24	MA_CS45#	IN	199	DM0
24	MA_CS46#	IN	200	DM0
24	MA_CS47#	IN	241	DM0
24	MA_CS48#	IN	96	DM0

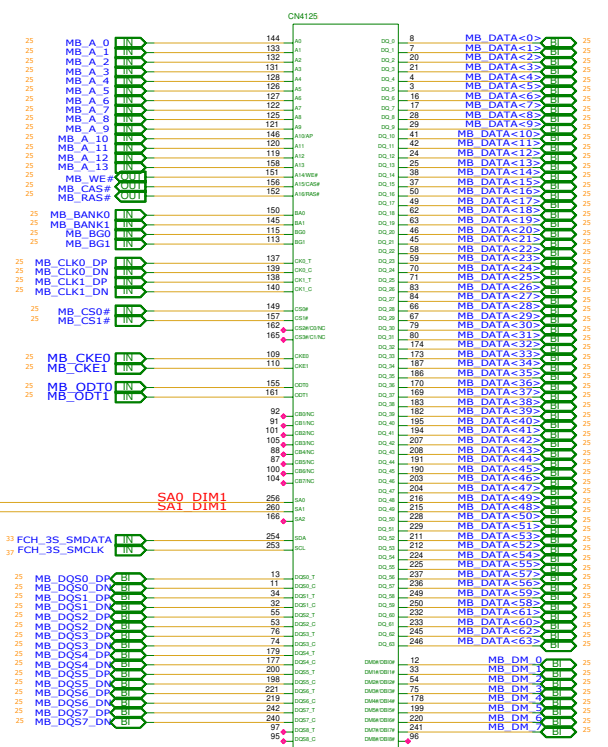
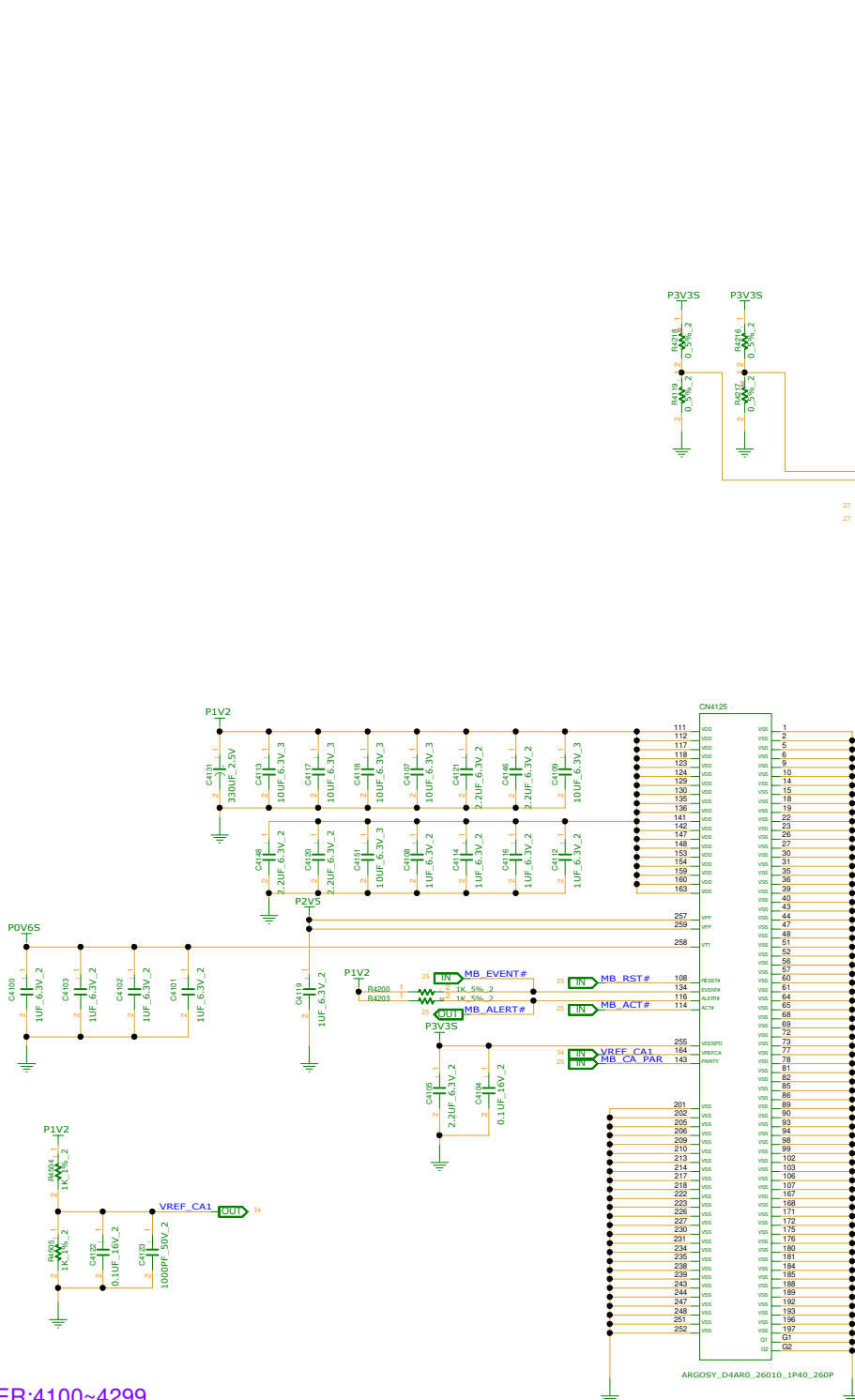
NOTE:
 IF SA0_DIM0=0, SA1_DIM0=0
 SO-DIMMA TS ADDRESS IS 0X30
 IF SA0_DIM0=1, SA1_DIM0=0
 SO-DIMMA TS ADDRESS IS 0X32

ARGOSY_D4AR0_26010_1P40_260P
 6026B0328101-004

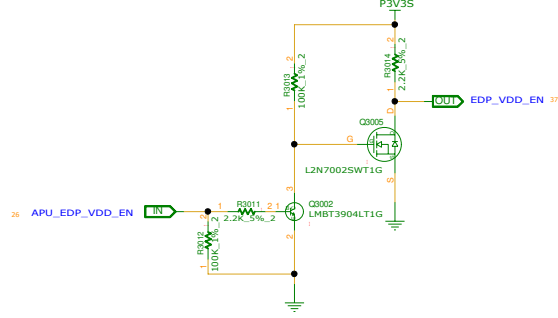
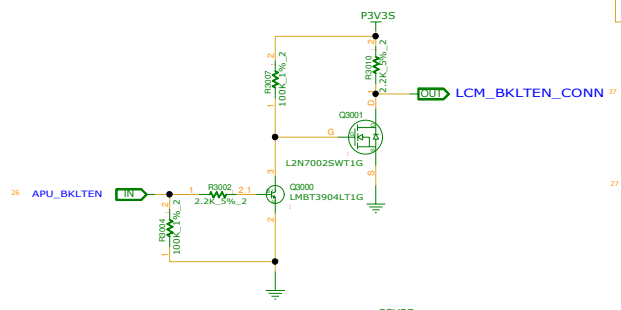
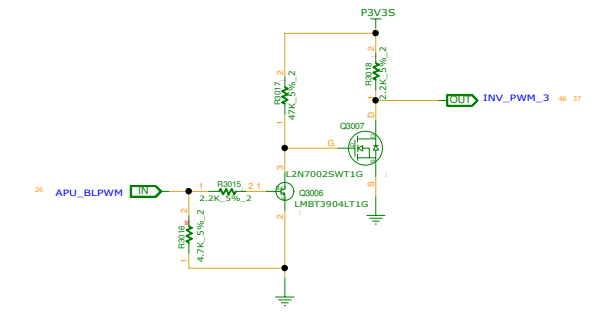
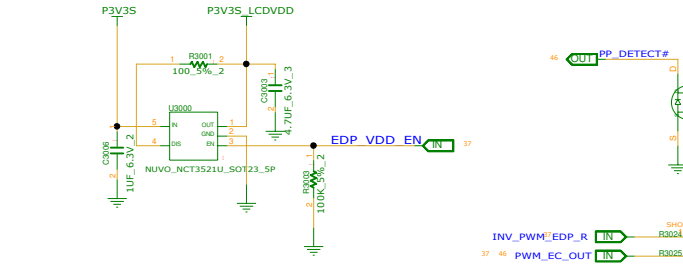
CHANGE#	XXX	DATE	CODE	DOC NUMBER	REV
PCB.P/N	6026B0328101-004	PCB.VER.1	2	1313D000000-010	31
SIZE	C	SHEET	4	31	36

NOTE:
 SO-DIMM SPD ADDRESS IS 0X44
 SO-DIMM TS ADDRESS IS 0X34

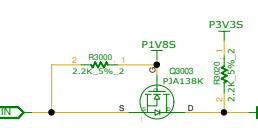
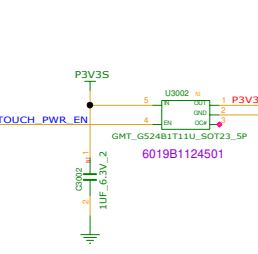
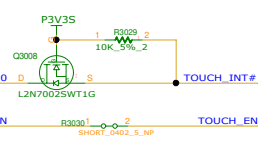
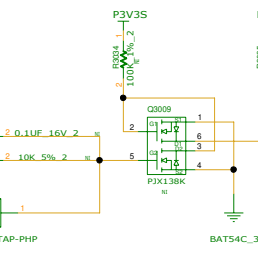
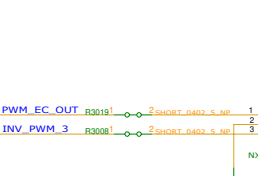
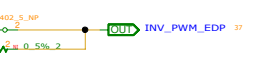
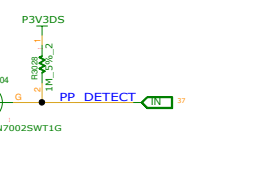
REFERENCE NUMBER:4100~4299



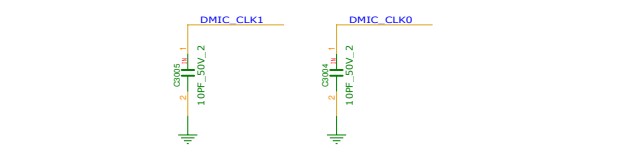
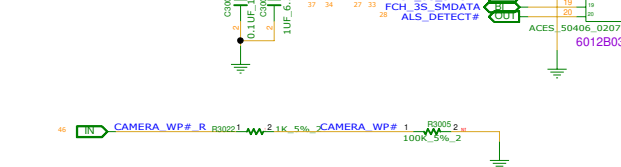
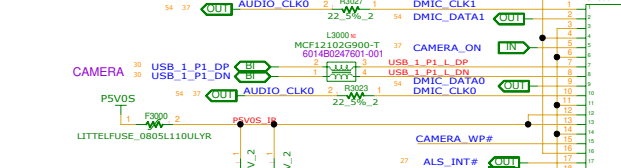
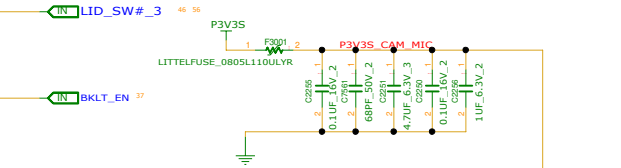
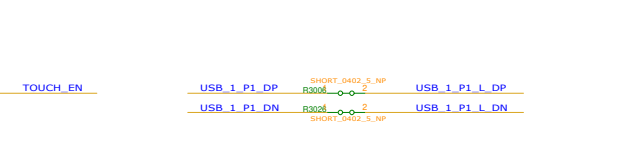
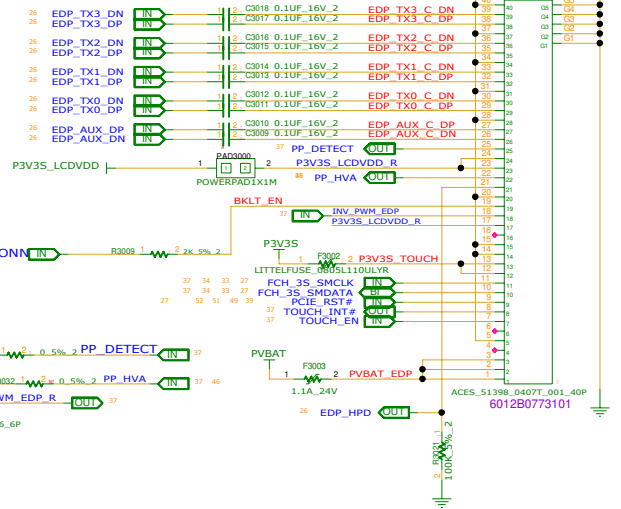
ARGOSY_D4AR0_26010_1P40_260P
 6026B0328101-004



DP TO EDP LEVEL SHIFT

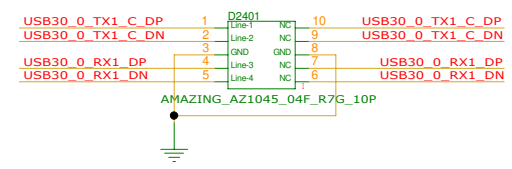
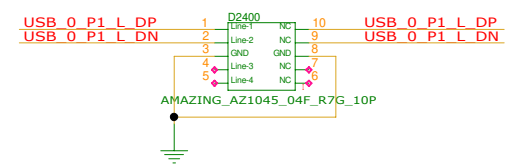
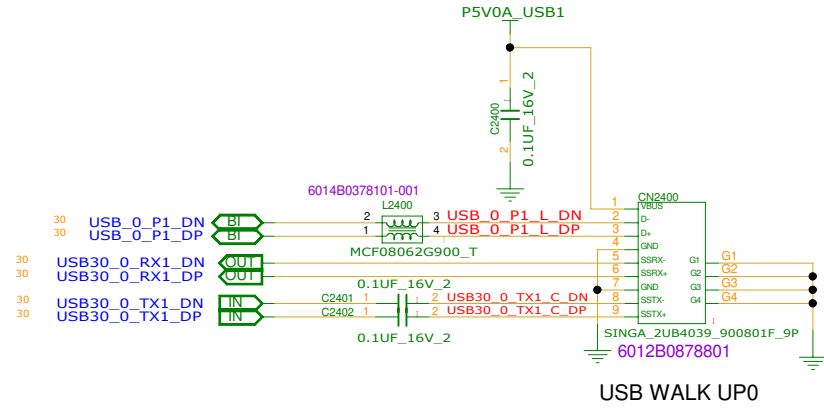
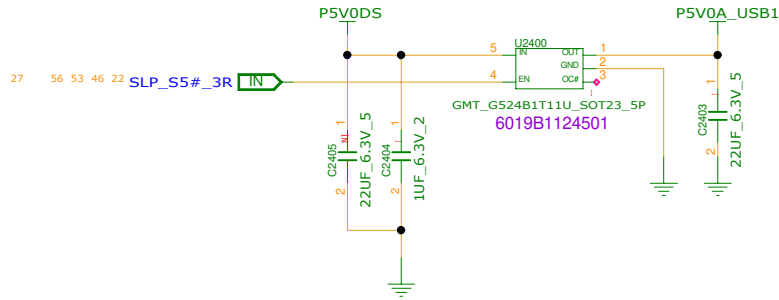


REFERENCE NUMBER:3000~3049



TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOCNUMBER	REV
A5	65	1310XXXX-0-0	X01
SHEET	37	of 66	

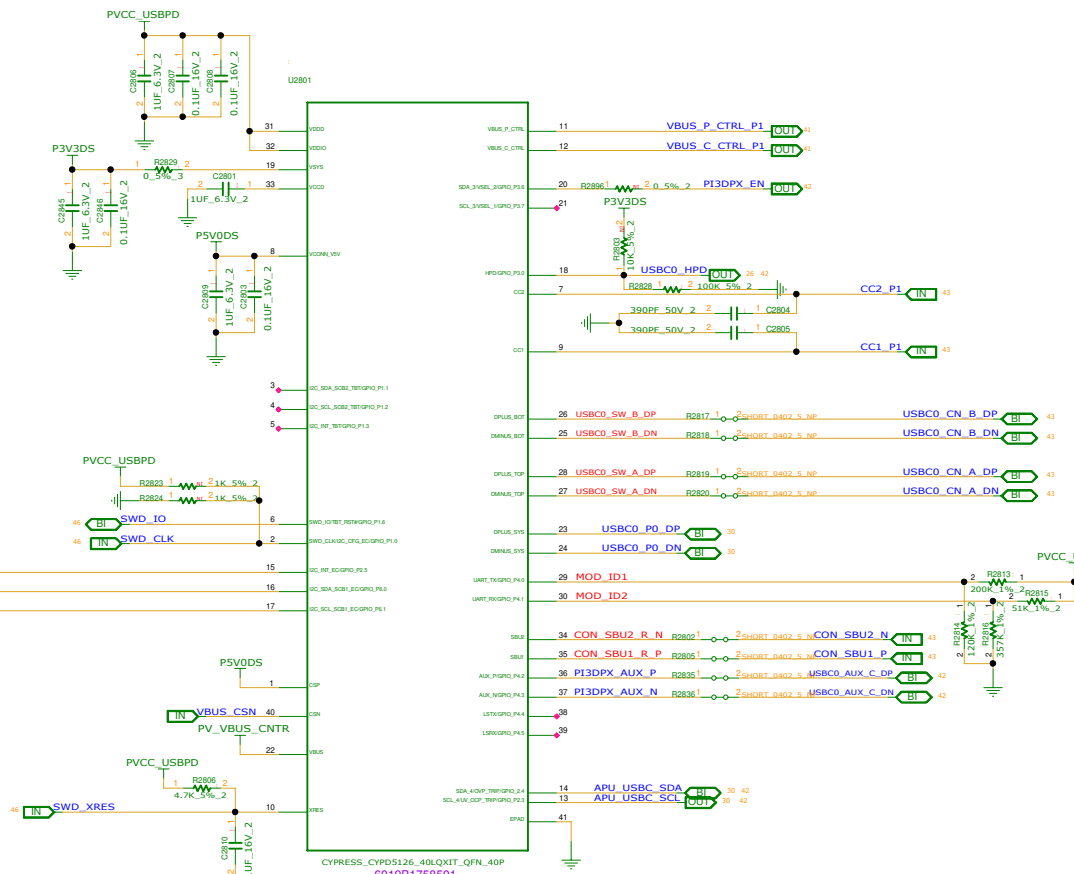
CHANGE#	XXX	DATE	21-OCT-2002
PCB/PIN	6PXXXXXXXXXX	PCB/VER	XXX



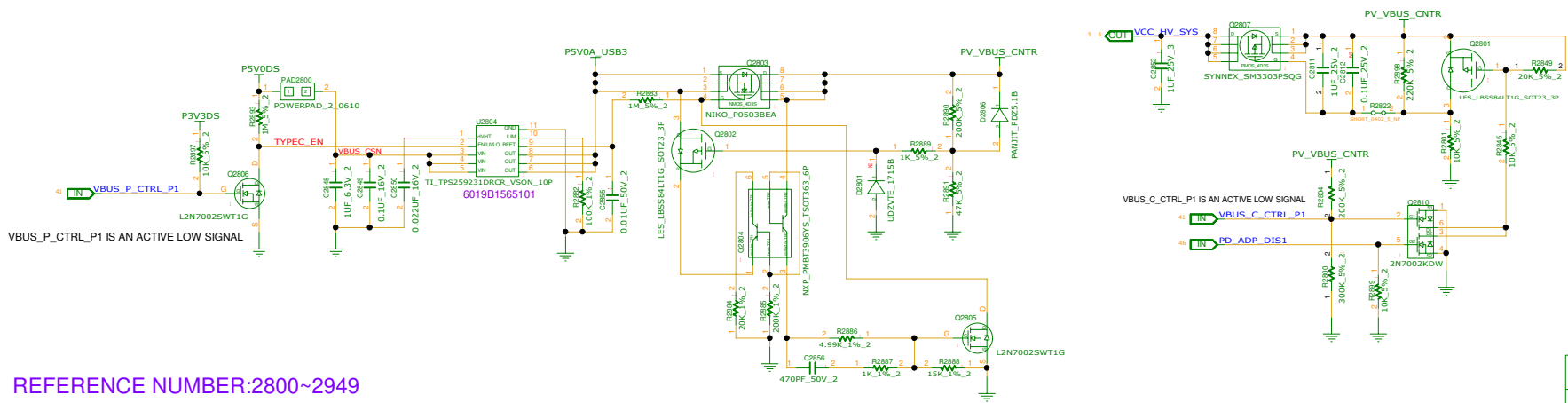
REFERENCE NUMBER:2400~2499

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION USB			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		40 of 66	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

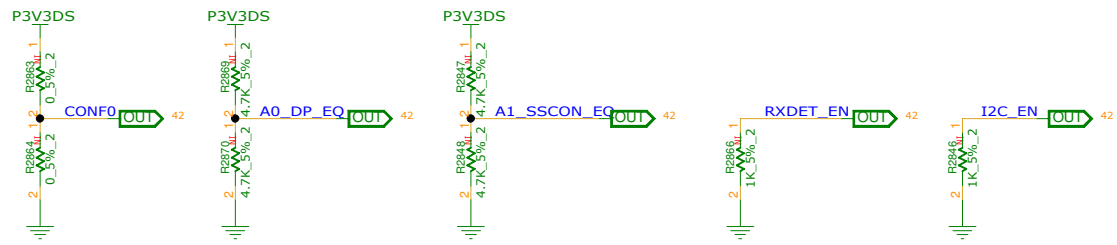
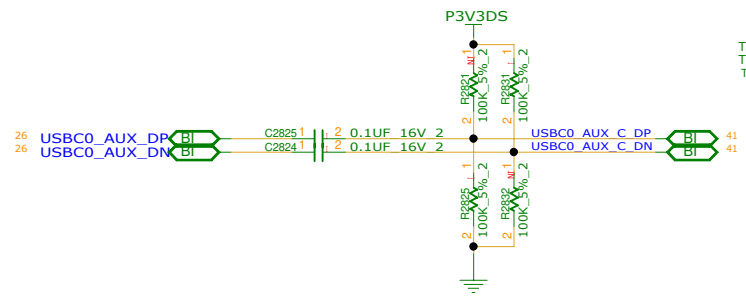
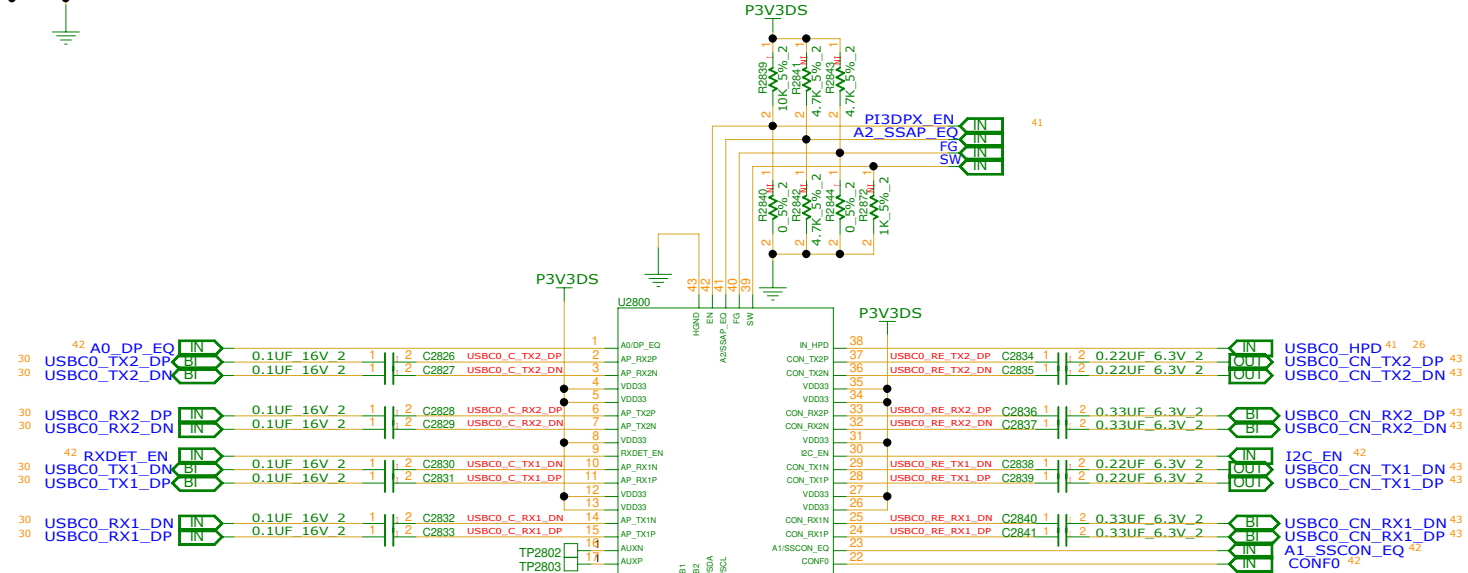
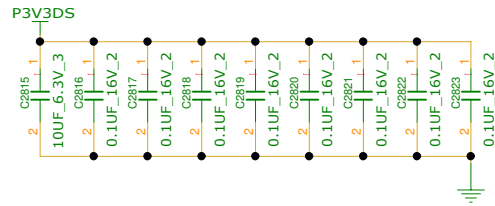


$MOD_ID1 = L3 = 3 \cdot VDD8 / 8 = 1.2375V$
 $MOD_ID2 = L7 = 7 \cdot VDD8 / 8 = 2.8875V$



REFERENCE NUMBER:2800~2949
USB-C PD CONTROLLER

CHANGE#	XXX	DATE	21-OCT-2002	TITLE	MODEL,PROJECT,FUNCTION	SIZE	CODE	DOCNUMBER	REV
PCB PIN	60XXXXXXXXXX	PCB VER	XXX	Block Diagram		AS	1310XXXXXX-2-0		X01
SHEET	41						of 66		



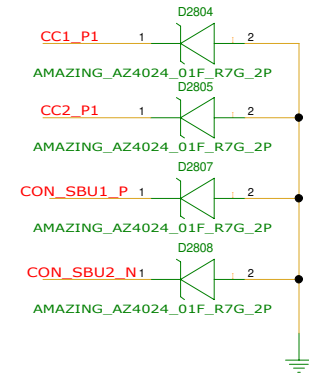
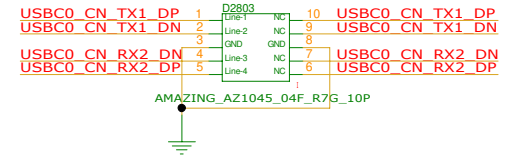
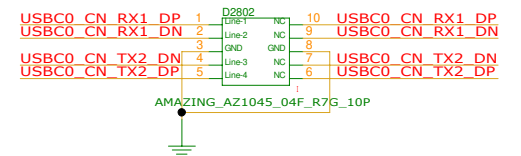
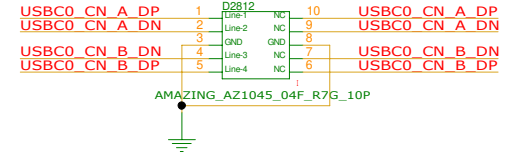
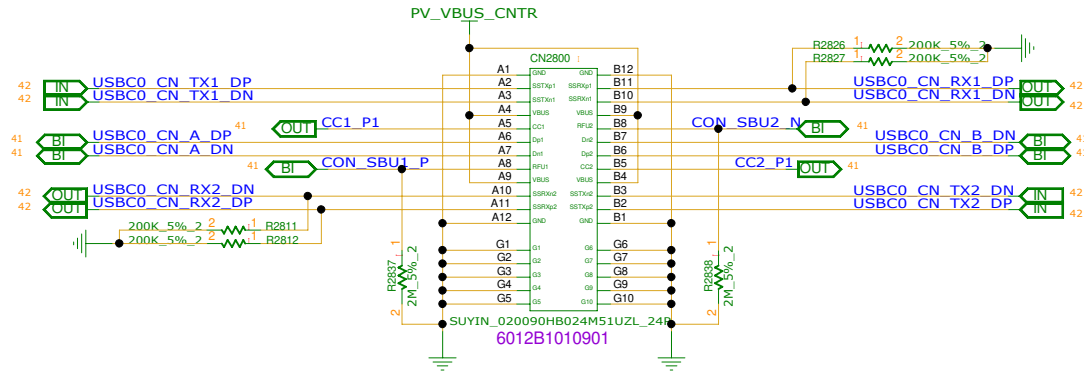
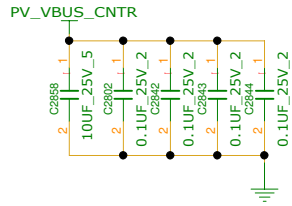
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

SHEET 42 of 66

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

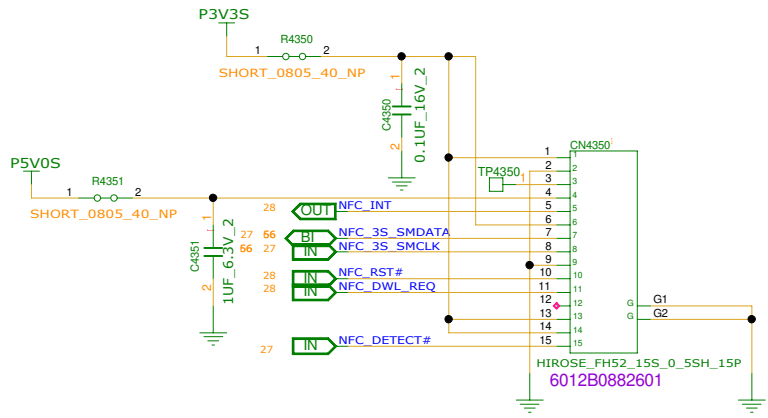


USB TYPE C

REFERENCE NUMBER:2800 ~ 2949

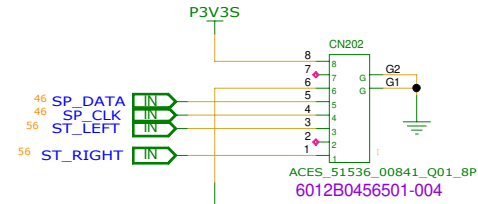
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
USB TYPE-C_CNTR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		43 of 66	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



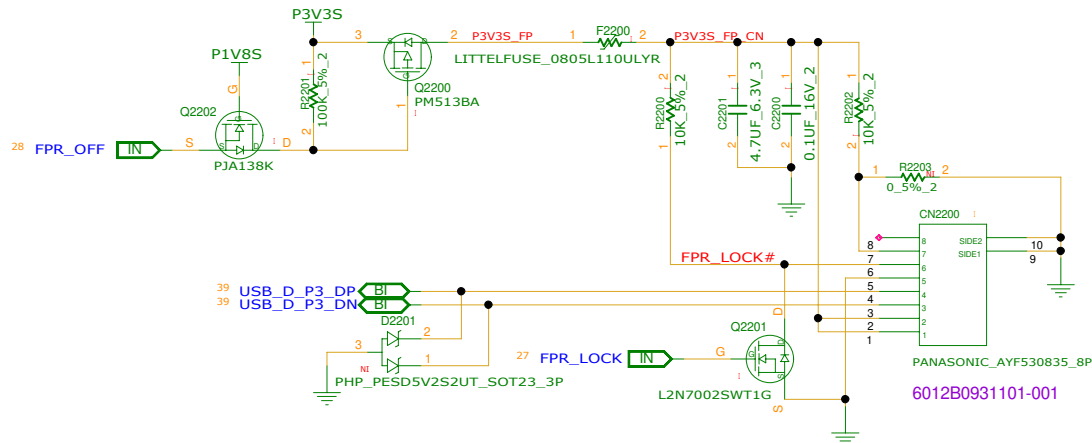
NFC MODULE CNTR

REFERENCE NUMBER : 4350~4399



POINT STICK CNTR

REFERENCE NUMBER : 200~299



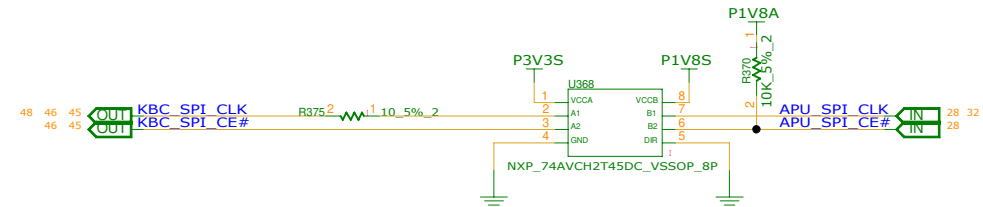
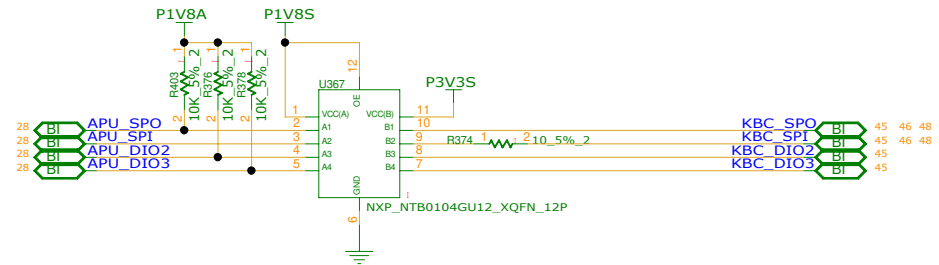
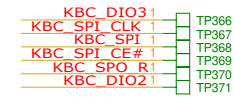
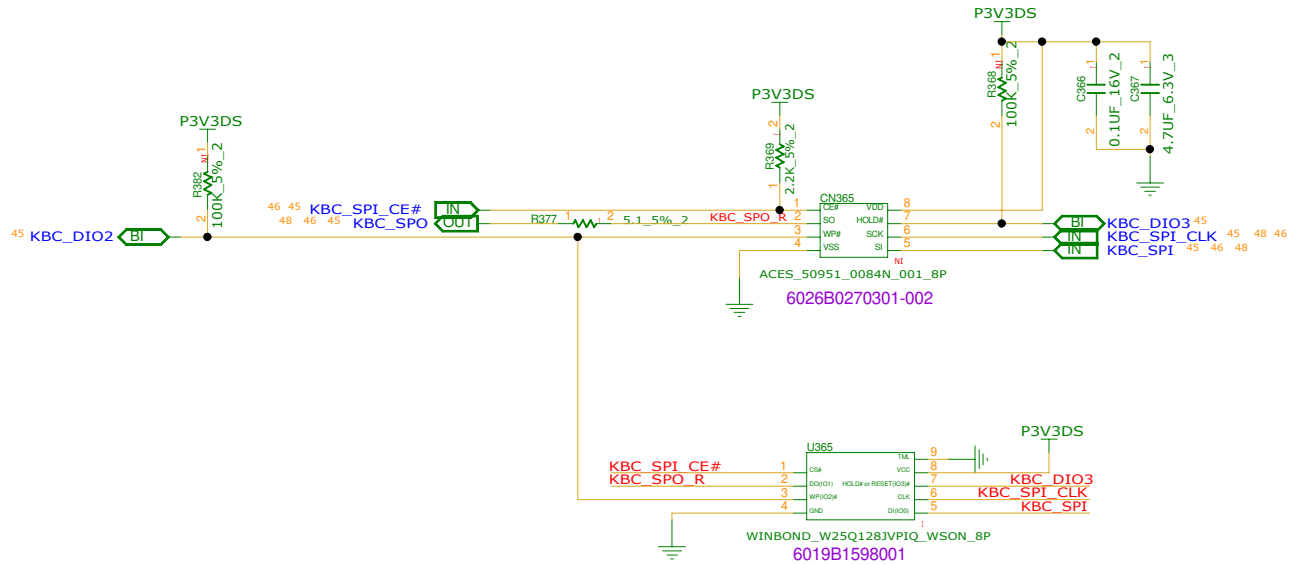
FINGER PRINT CNTR

REFERENCE NUMBER : 2200~2249

INVENTEC			
TITLE MINI PRINTER & NFC FUNCTION			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 44 of 66			

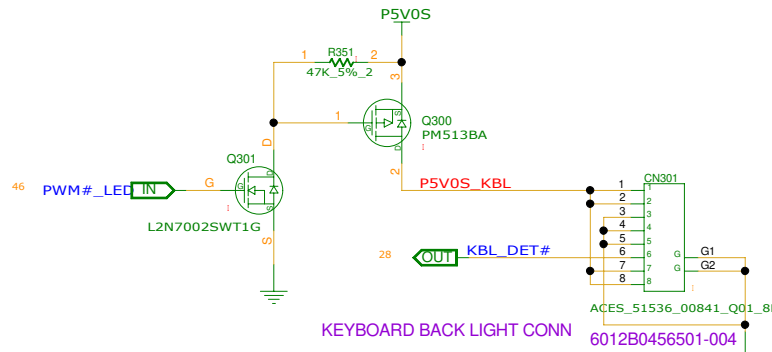
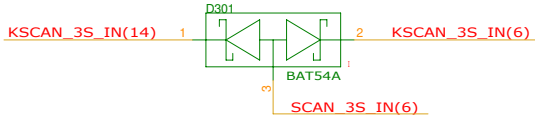
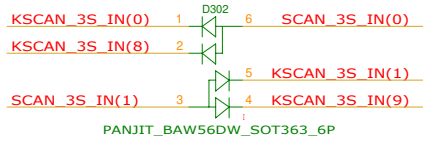
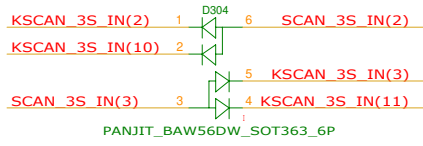
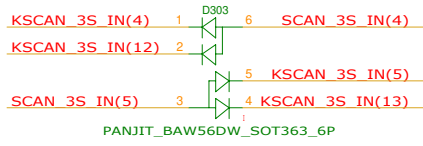
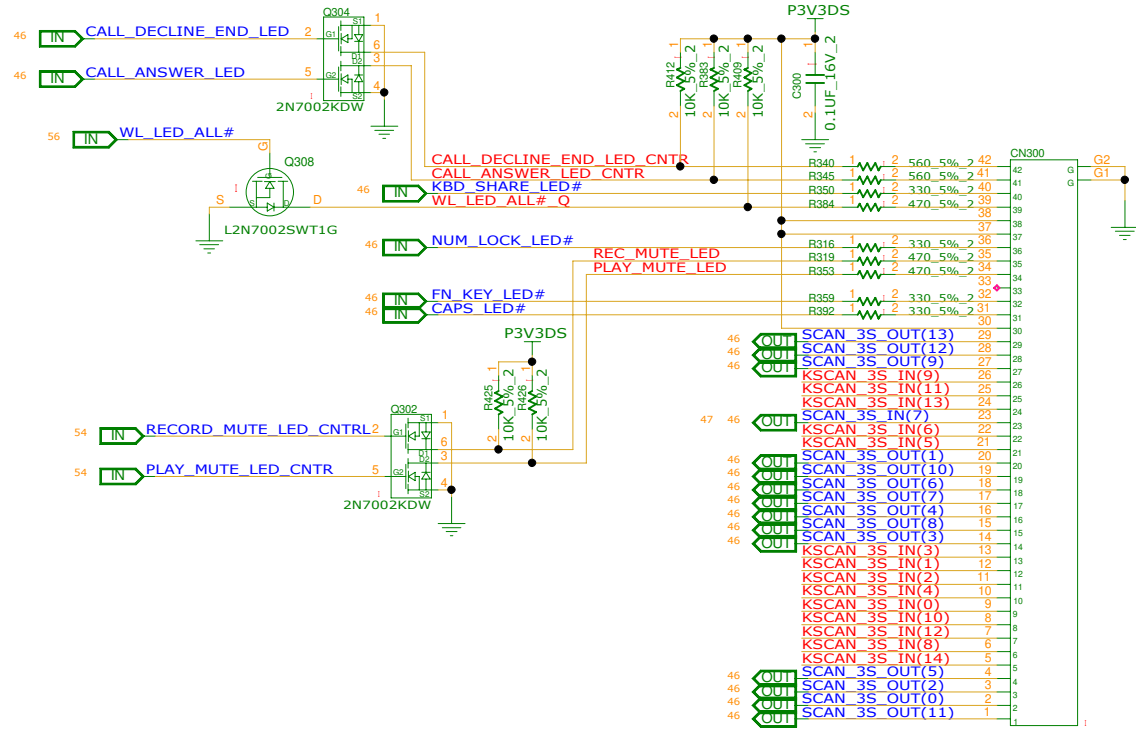
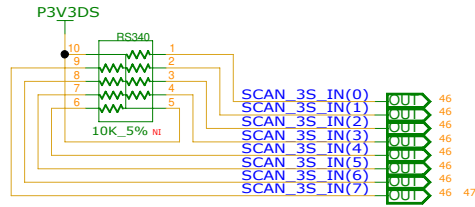
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SPI FLASH



INVENTEC			
TITLE MODEL, PROJECT, FUNCTION			
BIOS			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxxx		PCB VER XXX	
SHEET 45 of 66			

REFERENCE NUMER : 300~399



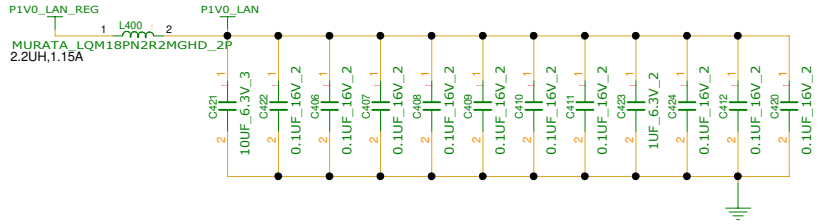
NOTE:
KBL_DET# FOR KEYBOARD LIGHT DETECT

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

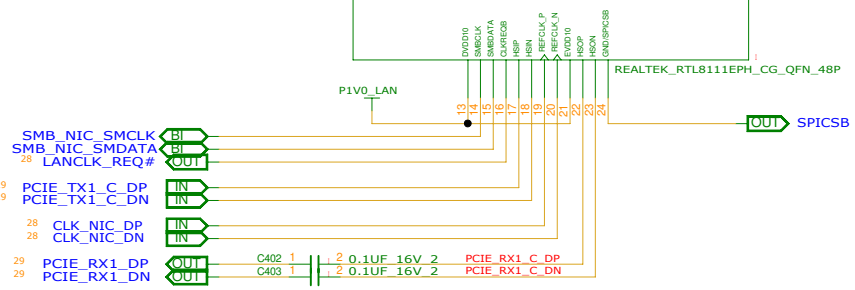
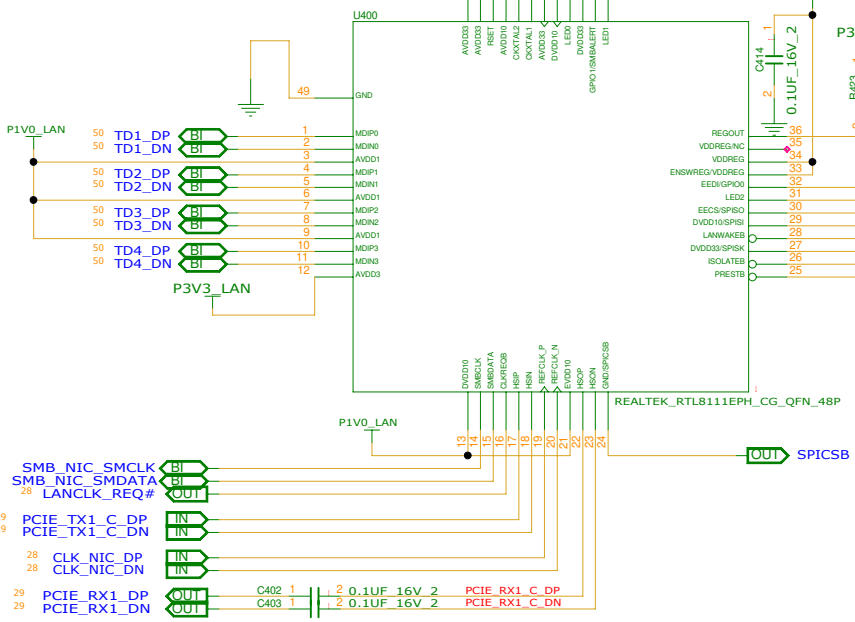
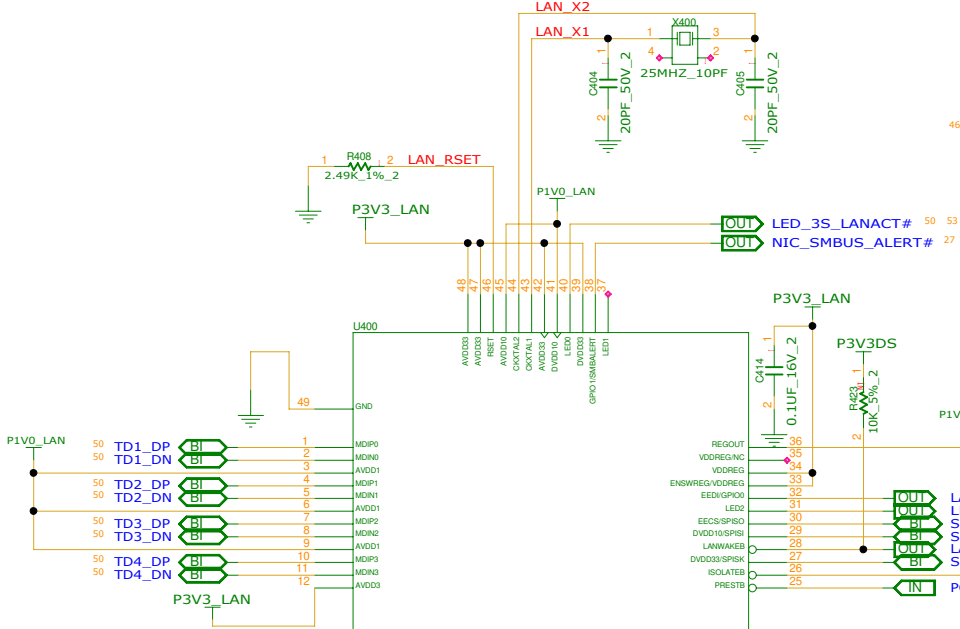
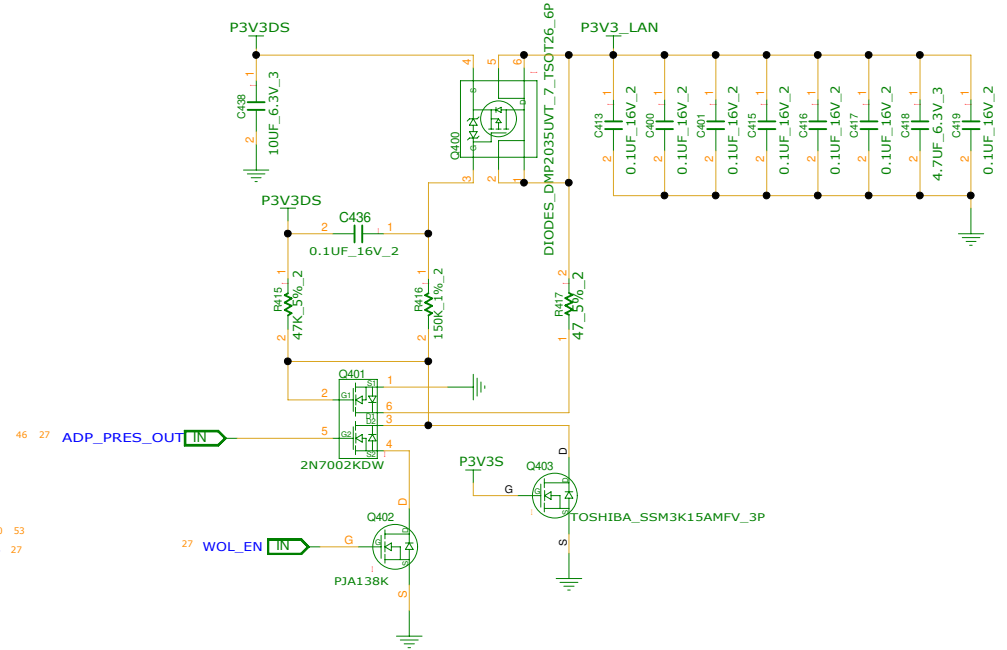
INVENTEC

TITLE: KEYBOARD
 MODIFIED PROJECT, FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01
 SHEET 47 of 66



P3V3_LAN RISING TIME 0.5MS~100MS



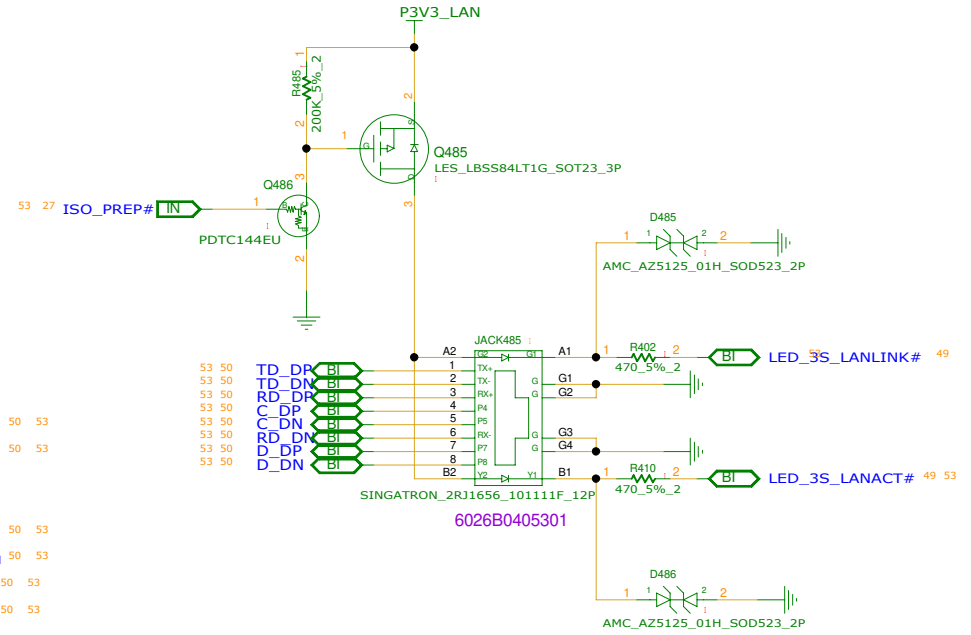
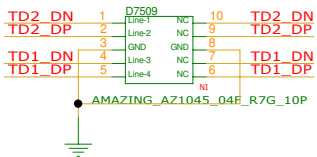
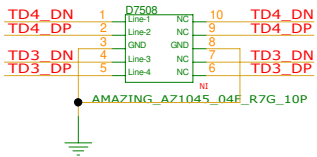
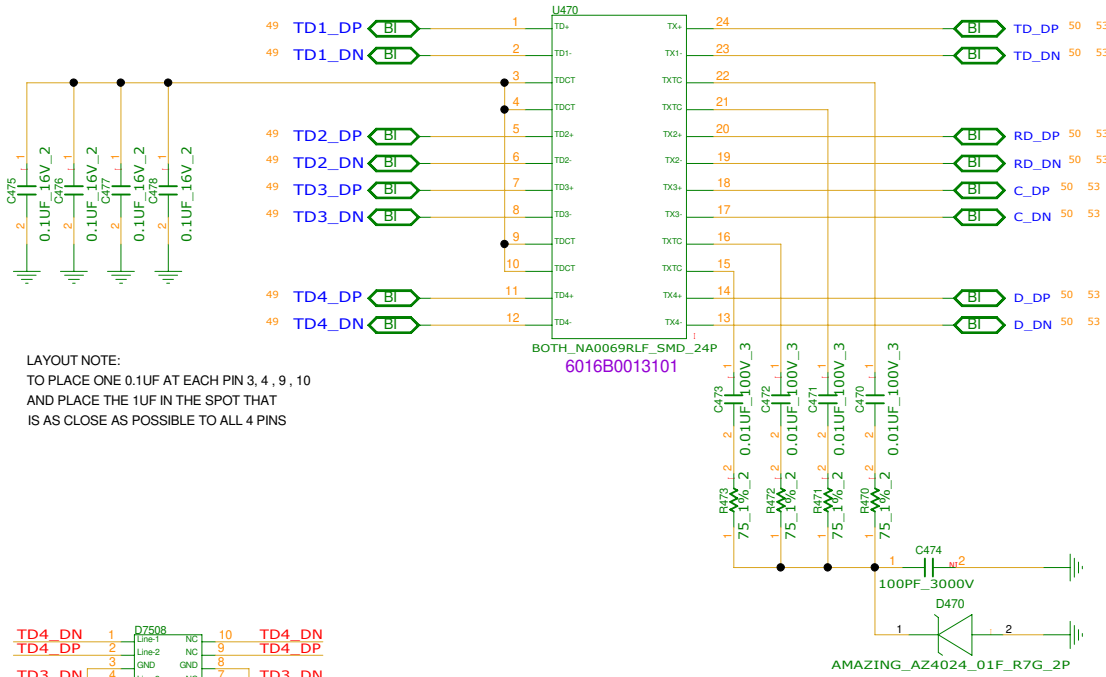
REFERENCE NUMBER : 400~469

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 49 of 66			

CHANGE by	XXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxxx	PCB VER	XXX

TRANSFORMER & RJ45 CONN

REFERENCE NUMER : 470~499



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

INVENTEC			
TITLE MODEL PROJECT FUNCTION TRANSFORMER & RJ45			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		50 of 66	

REFERENCE NUMBER:1400~1499

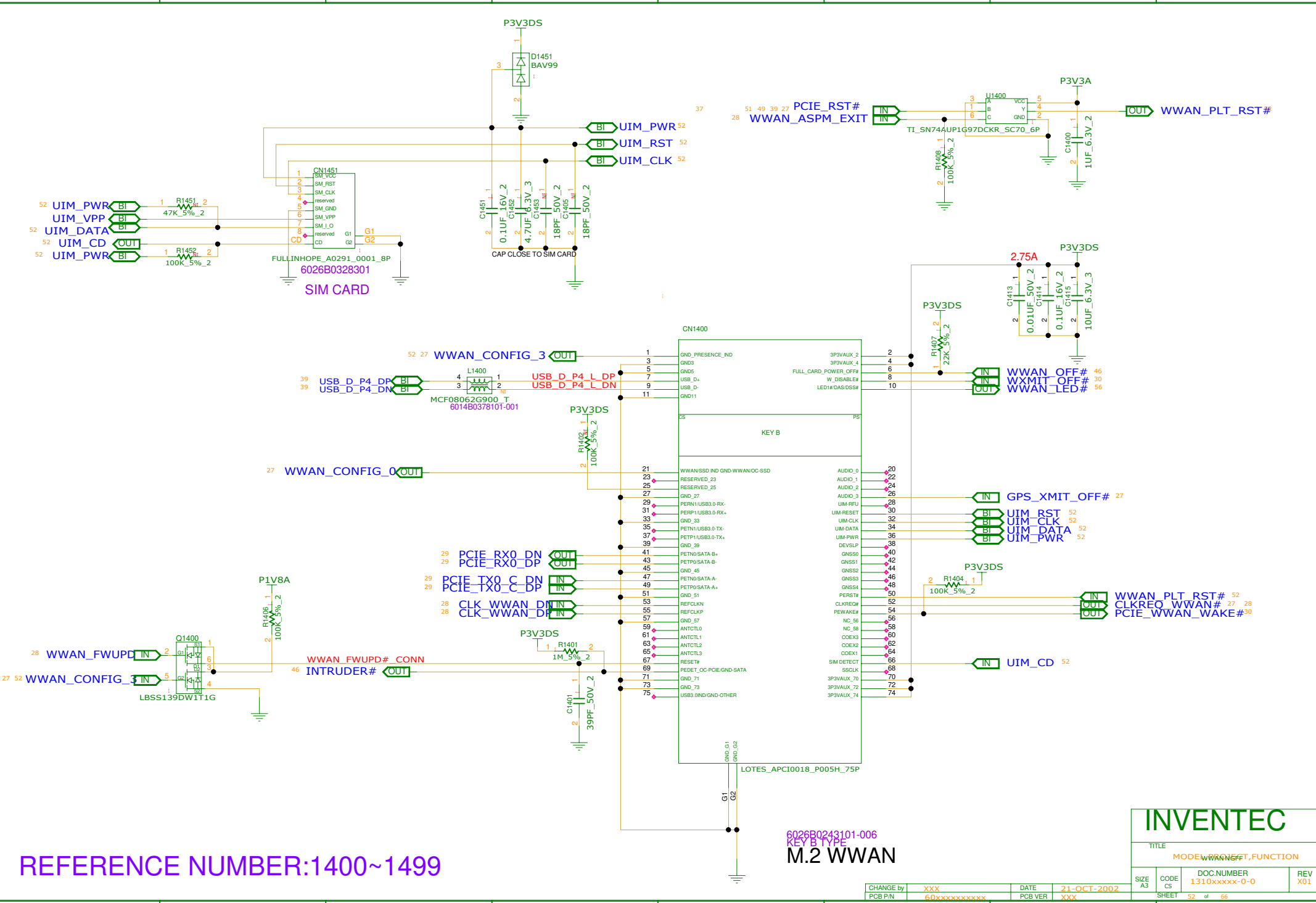
6026B0243101-006
KEY B TYPE
M.2 WWAN

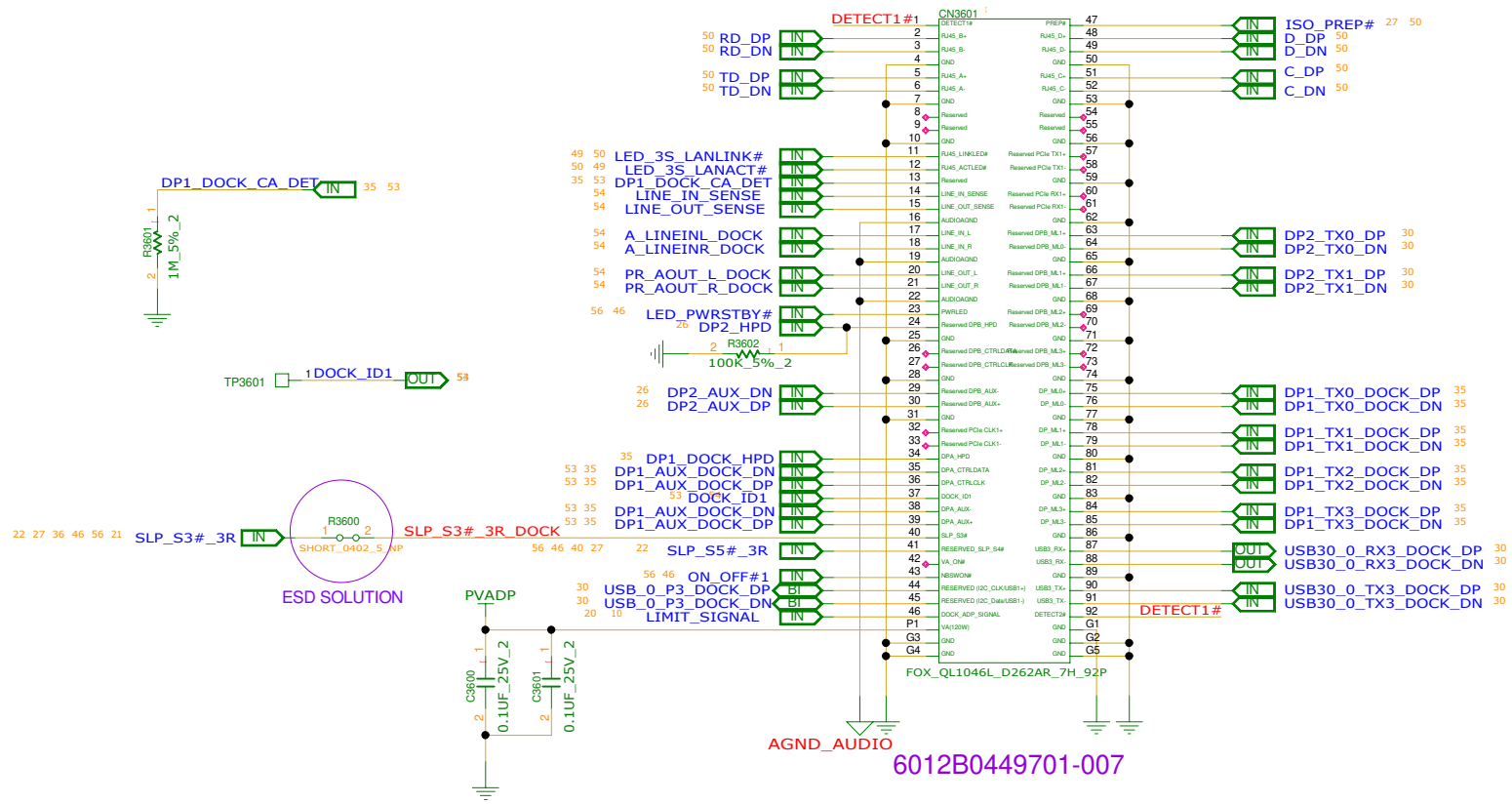
INVENTEC

TITLE
MODEM WWAN KEY B, FUNCTION

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		52 of 66	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX





6012B0449701-007

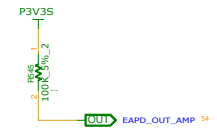
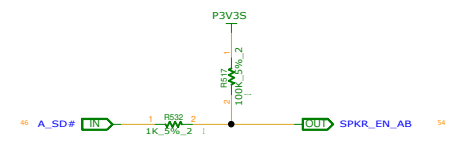
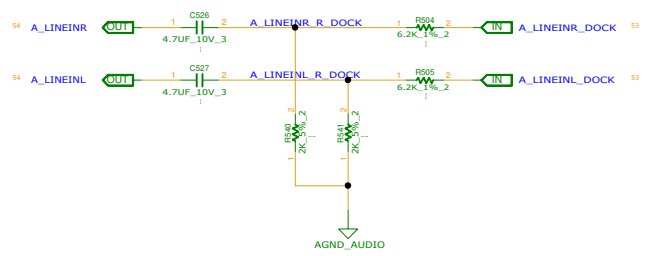
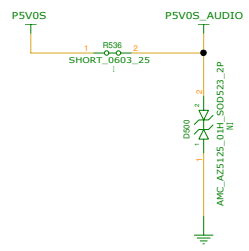
INVENTEC

TITLE: MODEL PROJECT,FUNCTION
DOCKING_CNTR

SIZE A3 CODE CS DOCNUMBER 1310xxxx-0-0 REV X01

SHEET 53 of 66

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

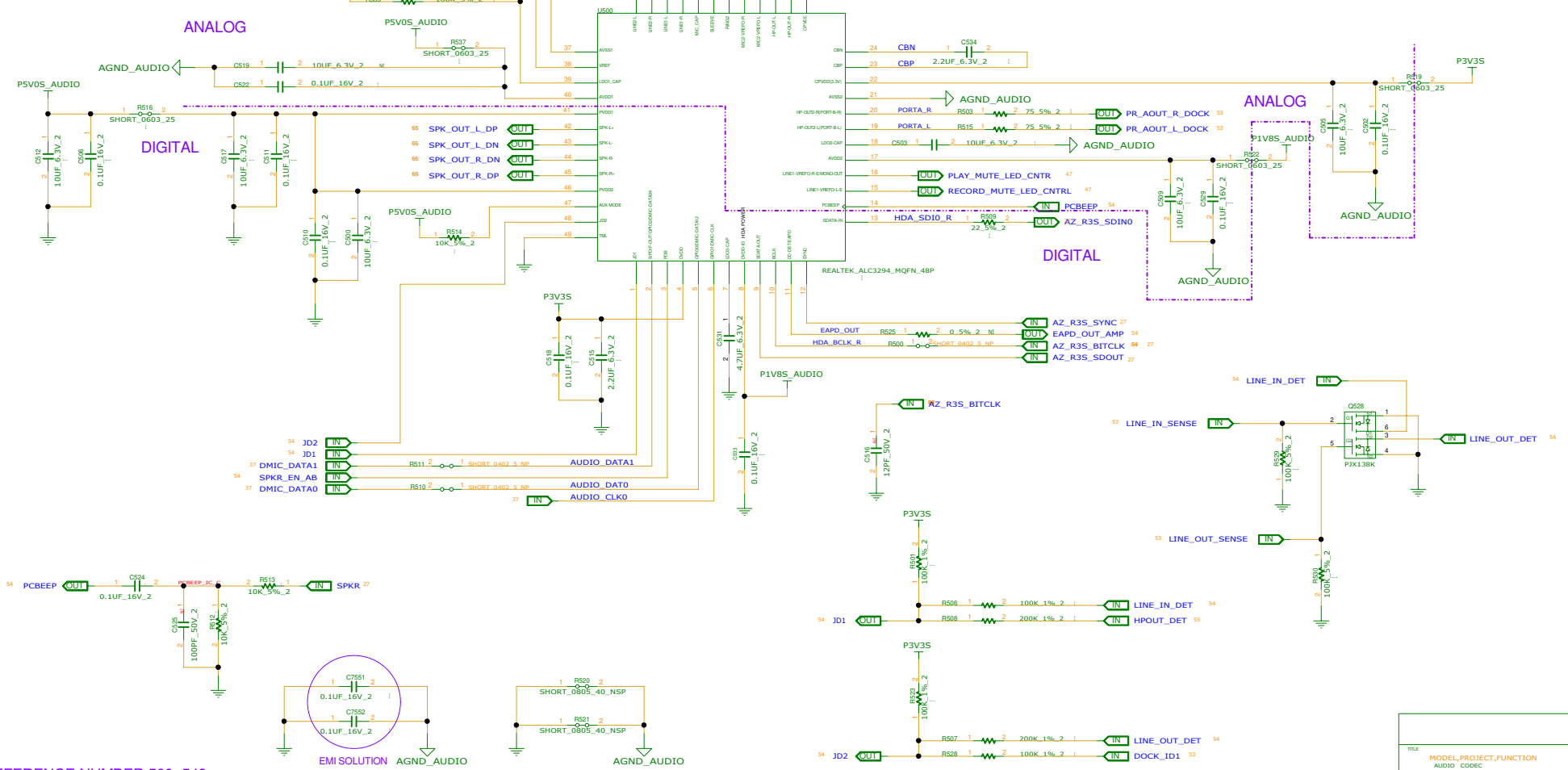


ANALOG

DIGITAL

ANALOG

DIGITAL

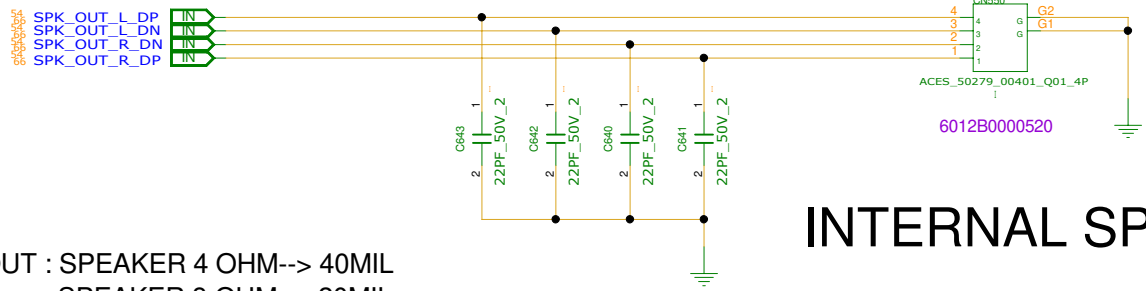


REFERENCE NUMBER:500~549

EMI SOLUTION AGND_AUDIO

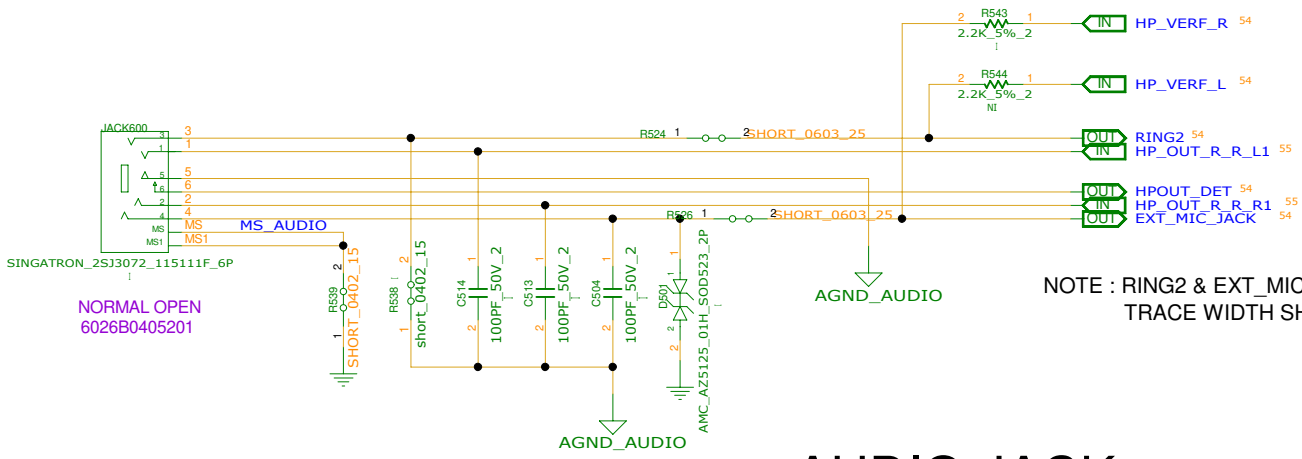
AGND_AUDIO

CHANGE#	XXX	DATE	21-OCT-2002	SIZE	CODE	DOCNUMBER	REV
PCB PIN	6Dxxxxxxxxxx	PCB VER	XXX	A5	63	1310xxxxx-2-0	X01
				SHEET	54	of 66	



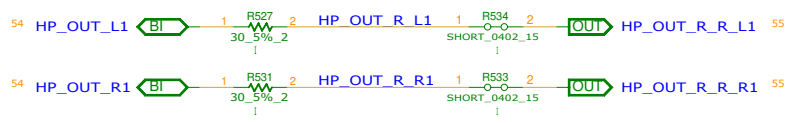
INTERNAL SPEAKER

LAYOUT : SPEAKER 4 OHM--> 40MIL
SPEAKER 8 OHM--> 20MIL



NOTE : RING2 & EXT_MIC_JACK
TRACE WIDTH SHOULD BE 40MIL LEAST

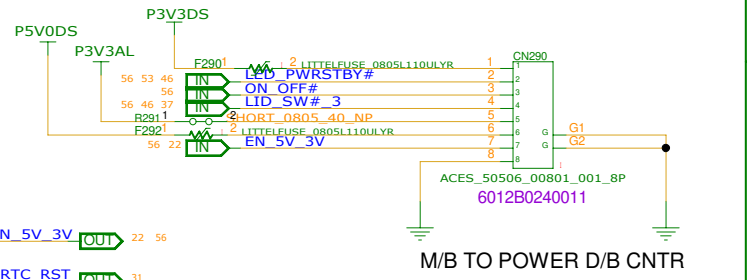
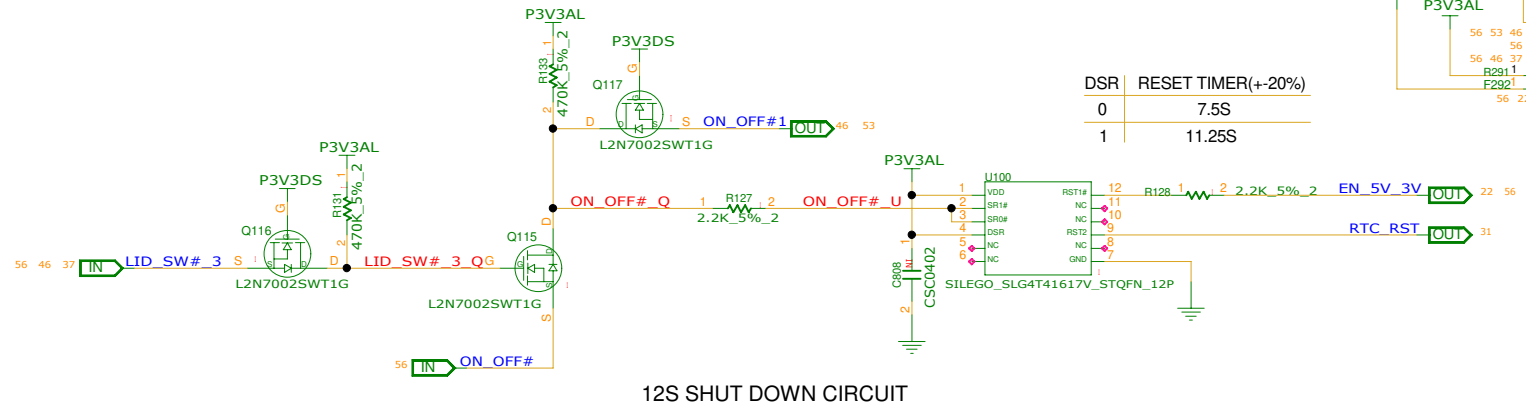
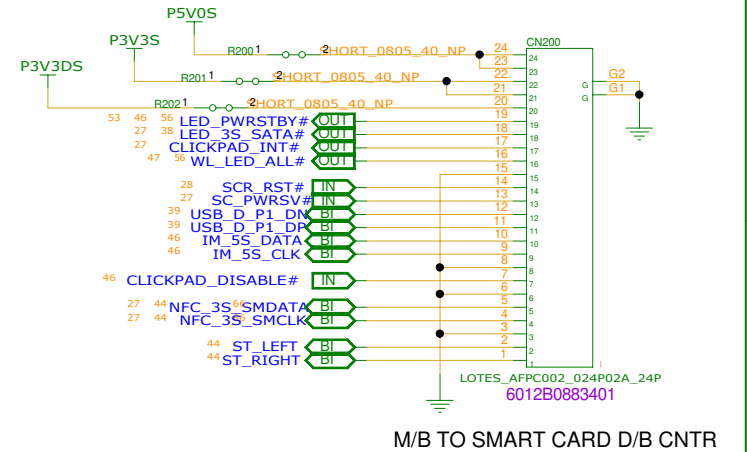
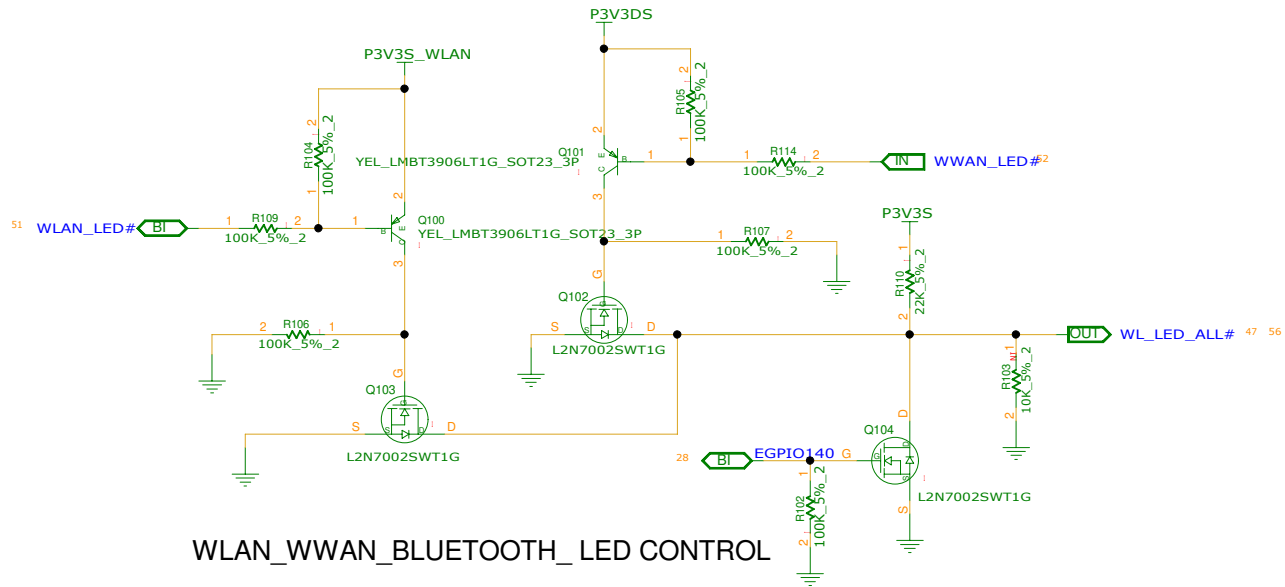
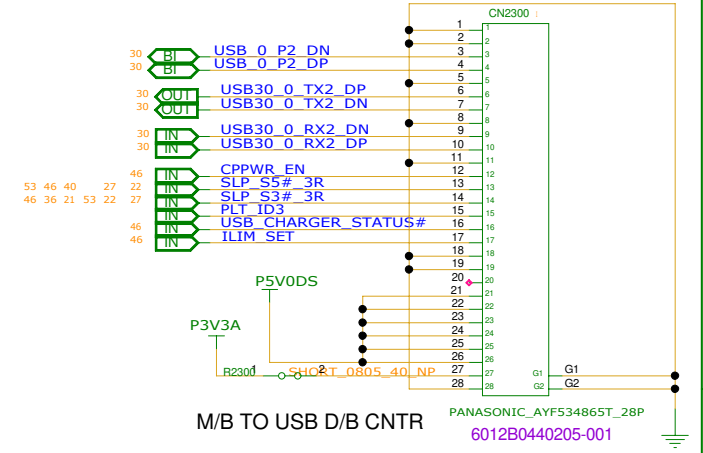
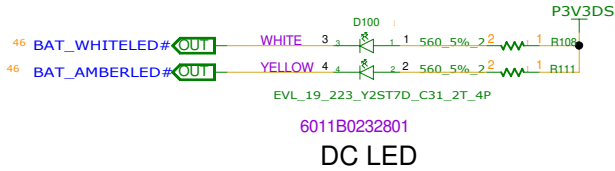
AUDIO JACK



REFERENCE NUMBER:600~649

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION SPEAKER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		55 of 66	

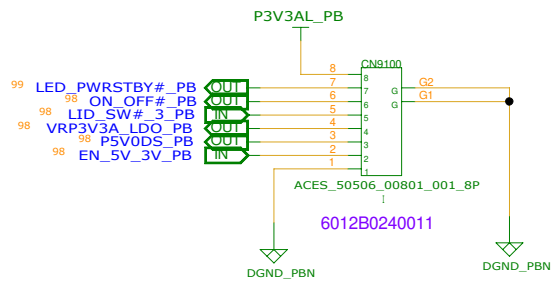
REFERENCE NUMBER:100~199



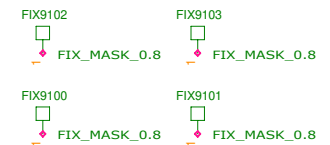
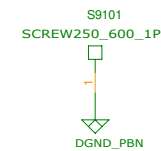
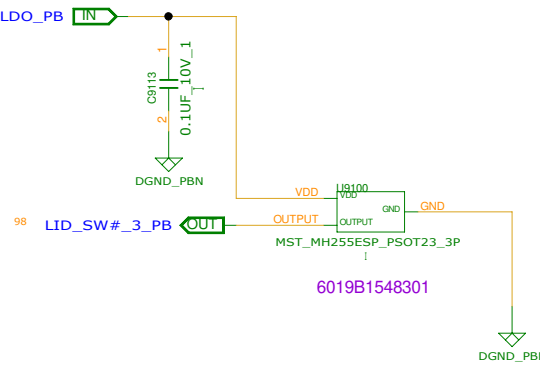
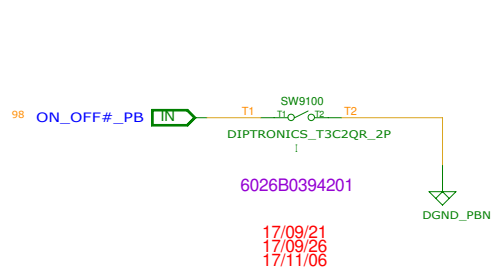
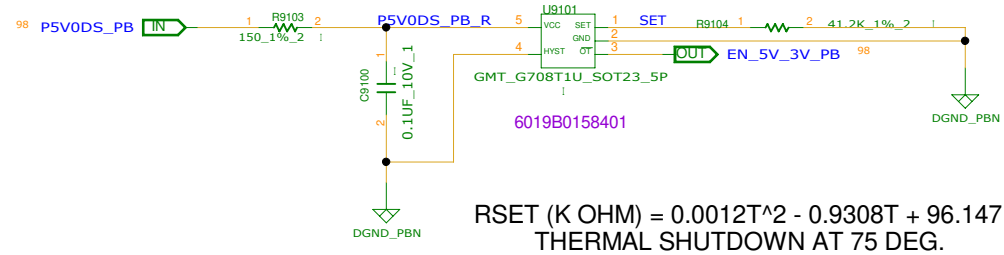
INVENTEC

TITLE			
512R2EL01NPJ&C2B1CNTR10N			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		56 of 66	

CHANGE by	XXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxxx	PCB VER	XXX



AMBIENT TEMP SENSE



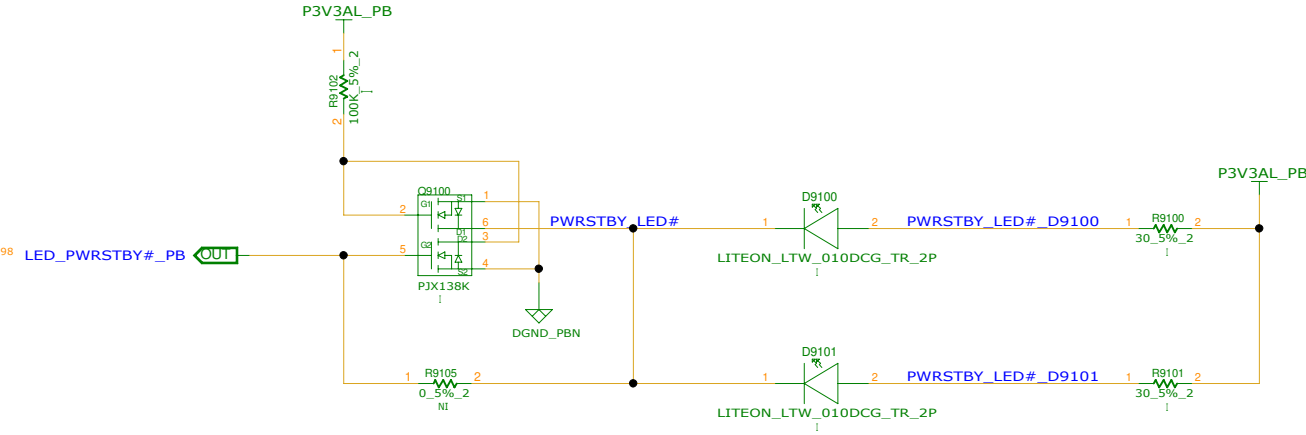
POWER SWITCH DAUGHTER BOARD

LOCATION NUMBER:9000~9099

INVENTEC				
TITLE MODEL PROJECT FUNCTION POWER BUTTON BOARD				
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01	
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX	
SHEET		57 of 66		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

POWER BUTTON BOARD LED

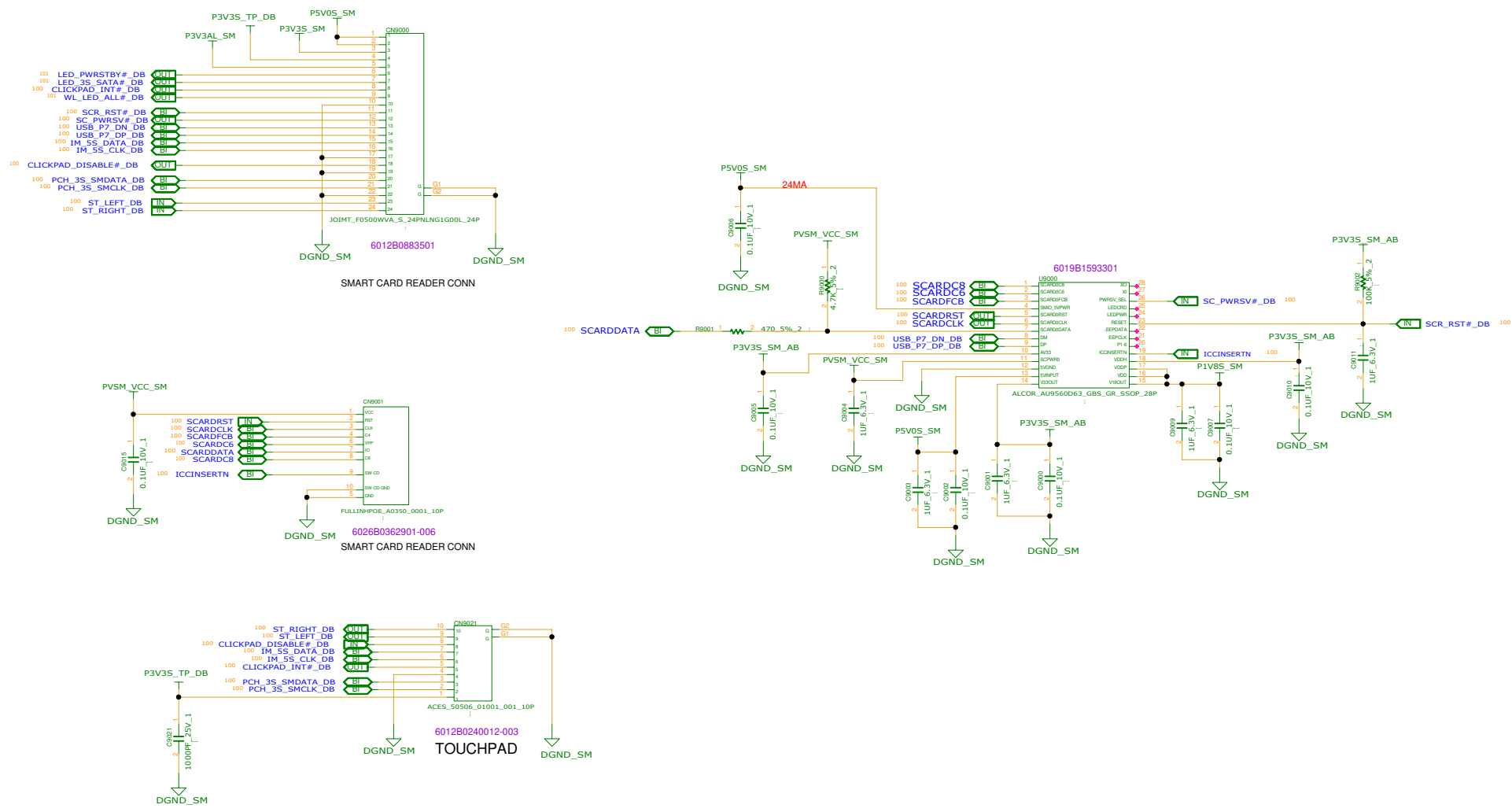


LOCATION NUMBER:9000~9099

INVENTEC

TITLE		MODEL PROJECT FUNCTION		REV
POWER BUTTON BOARD LED		1310xxxx-0-0		X01
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
SHEET		58 of 66		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

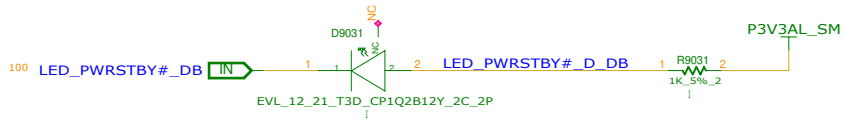


- FIX9000
FIX_MASK_0.8
- FIX9001
FIX_MASK_0.8
- FIX9002
FIX_MASK_0.8
- FIX9003
FIX_MASK_0.8
- FIX9004
FIX_MASK_0.8
- FIX9005
FIX_MASK_0.8

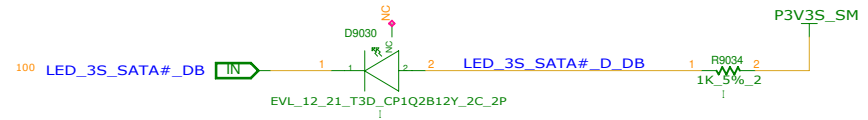
LOCATION NUMBER:9100~9199

INVENTEC			
TITLE MODEL_PROJECT_FUNCTION SMART_CARD_DB			
CHANGE#	XXX	DATE	21-OCT-2002
PCB PIN	60XXXXXXX	PCB VER	XXX
SIZE A1	CS	DOC NUMBER	1310XXXX-2-0
SHEET	01	REV	01

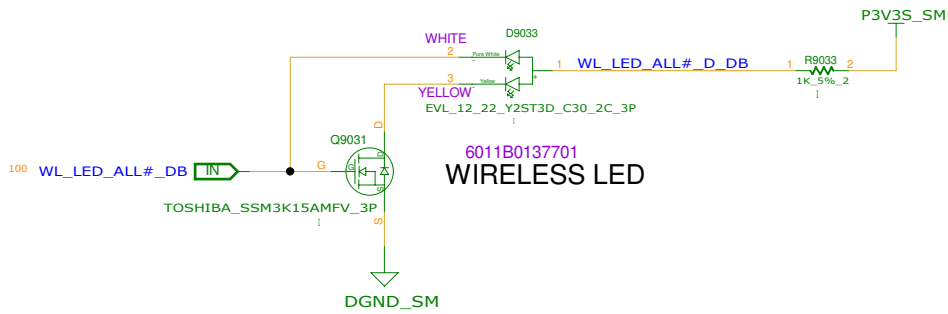
SMART CARD D/B LED



6011B0115101-005
POWER LED



6011B0115101-005
SATA LED

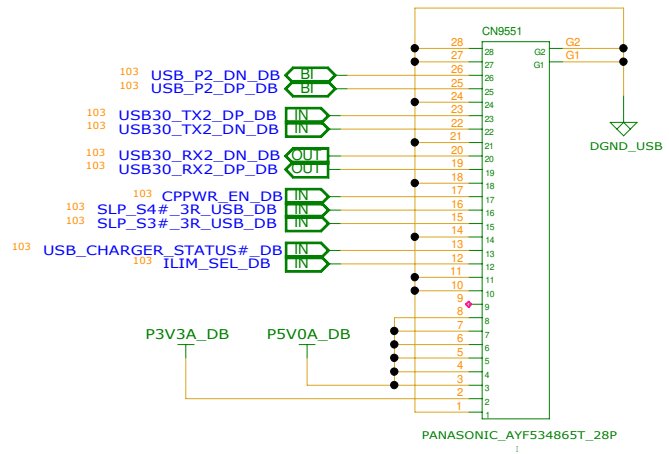


6011B0137701
WIRELESS LED

LOCATION NUMBER:9100~9199

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION SMART CARD D/B LED			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET
XXX 60xxxxxxxxxxx		21-OCT-2002 XXX	60 of 66

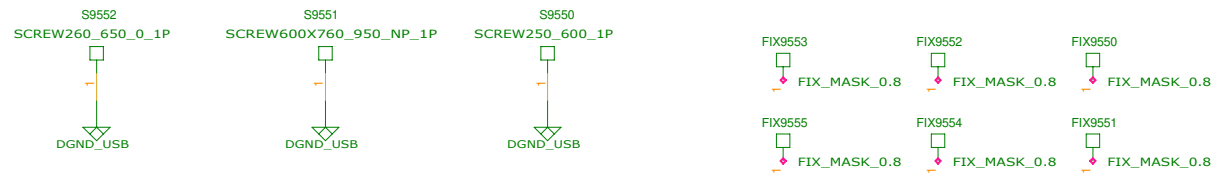
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



6012B0440205-001

NOTE : CN9551.13 IS PLT_ID3, NOT GND

USB DB CNTR

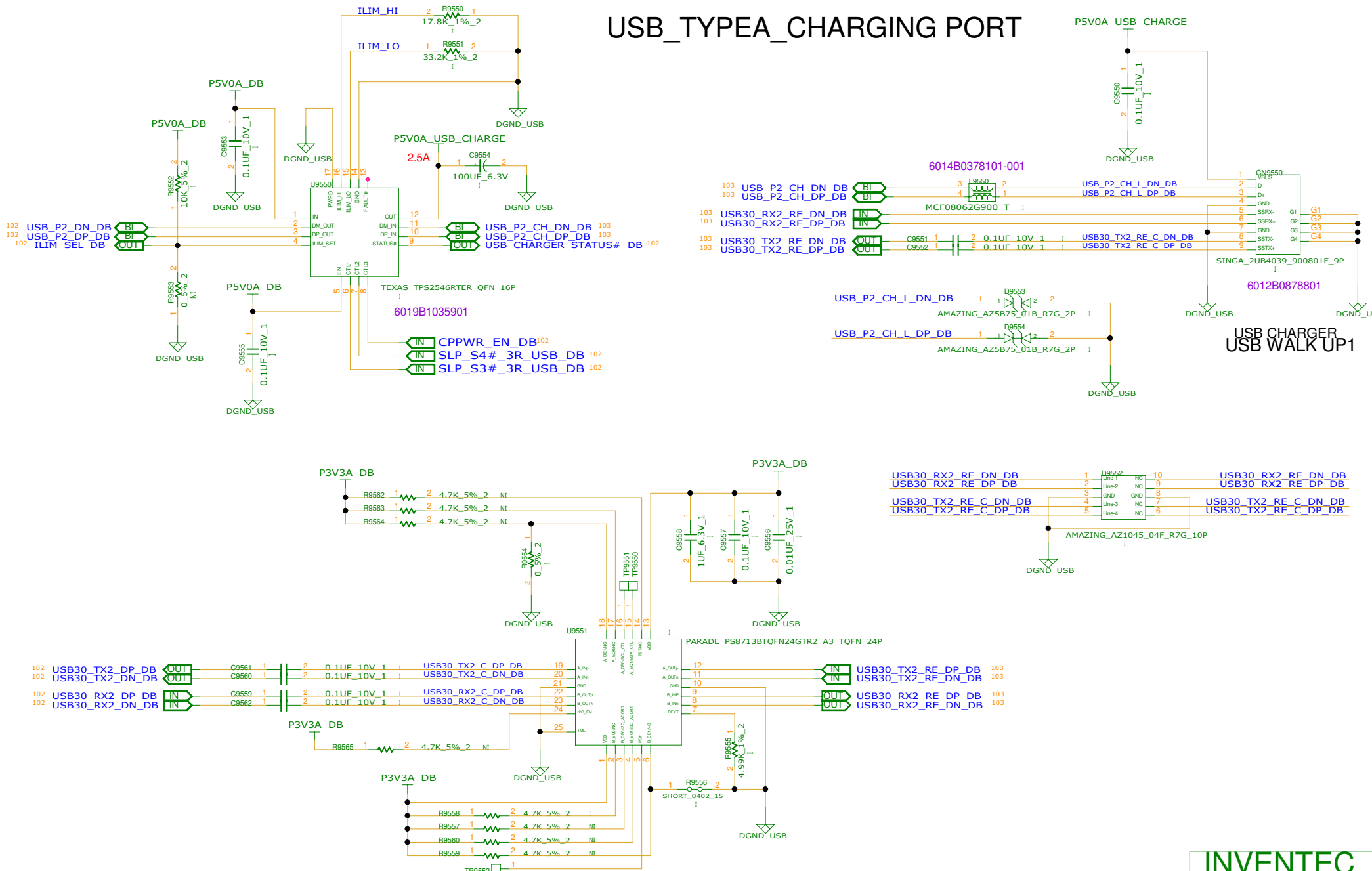


LOCATION NUMBER:9200~9299

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION USB_DB_CNTR			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET
XXX 60xxxxxxxxxx		21-OCT-2002 XXX	61 of 66

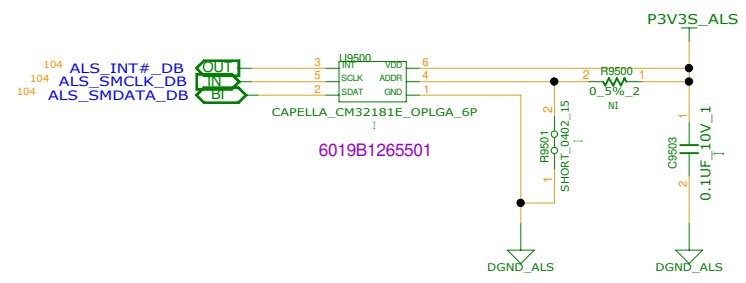
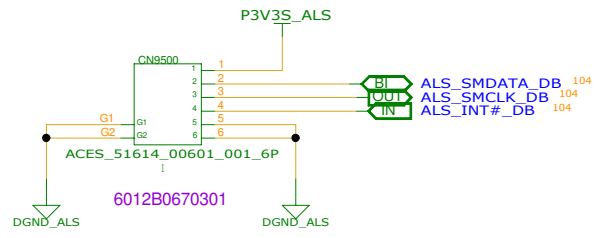
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

USB_TYPEA_CHARGING PORT



LOCATION NUMBER:9200~9299

INVENTEC			
TITLE MODEL PROJECT FUNCTION USB CHARGER PORT			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		62 of 66	



AMBIENT LIGHT SENSOR

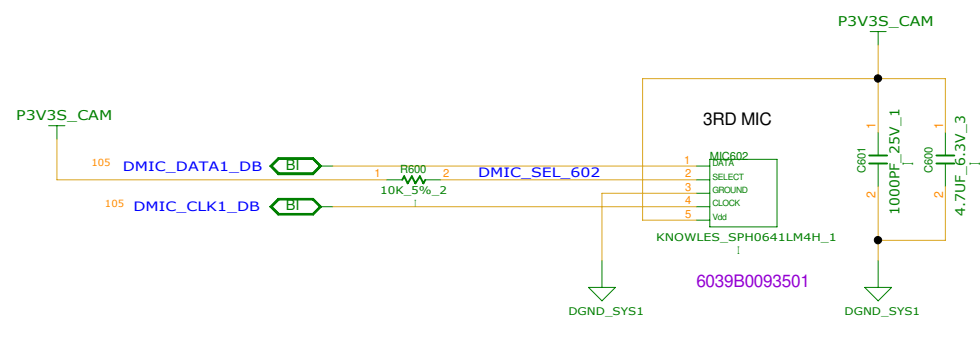
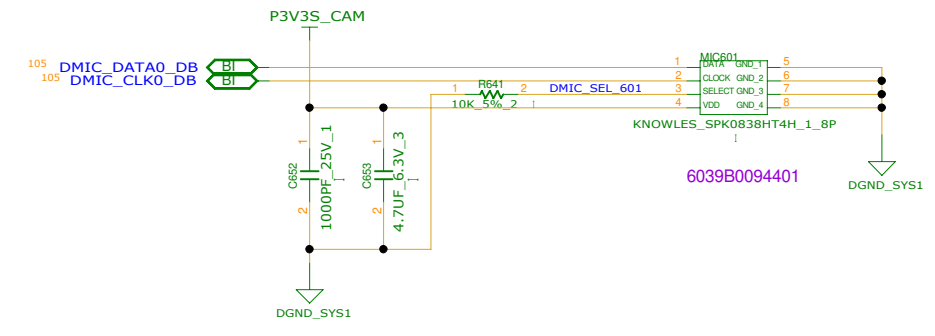
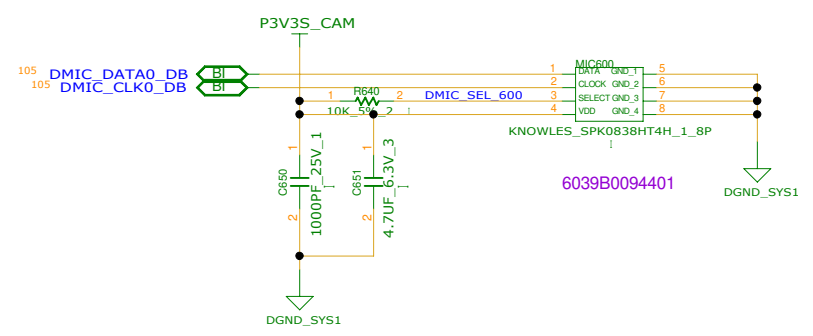
ADDR IS HIGH, SELECT ADDRESS 0X48
 ADDR IS LOW, SELECT ADDRESS 0X10



LOCATION NUMBER:9300~9349

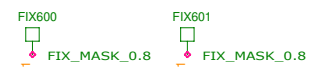
INVENTEC			
TITLE MODEL,PROJECT,FUNCTION ALS_D/B			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
SHEET 63 of 66			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

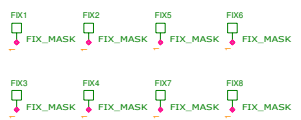
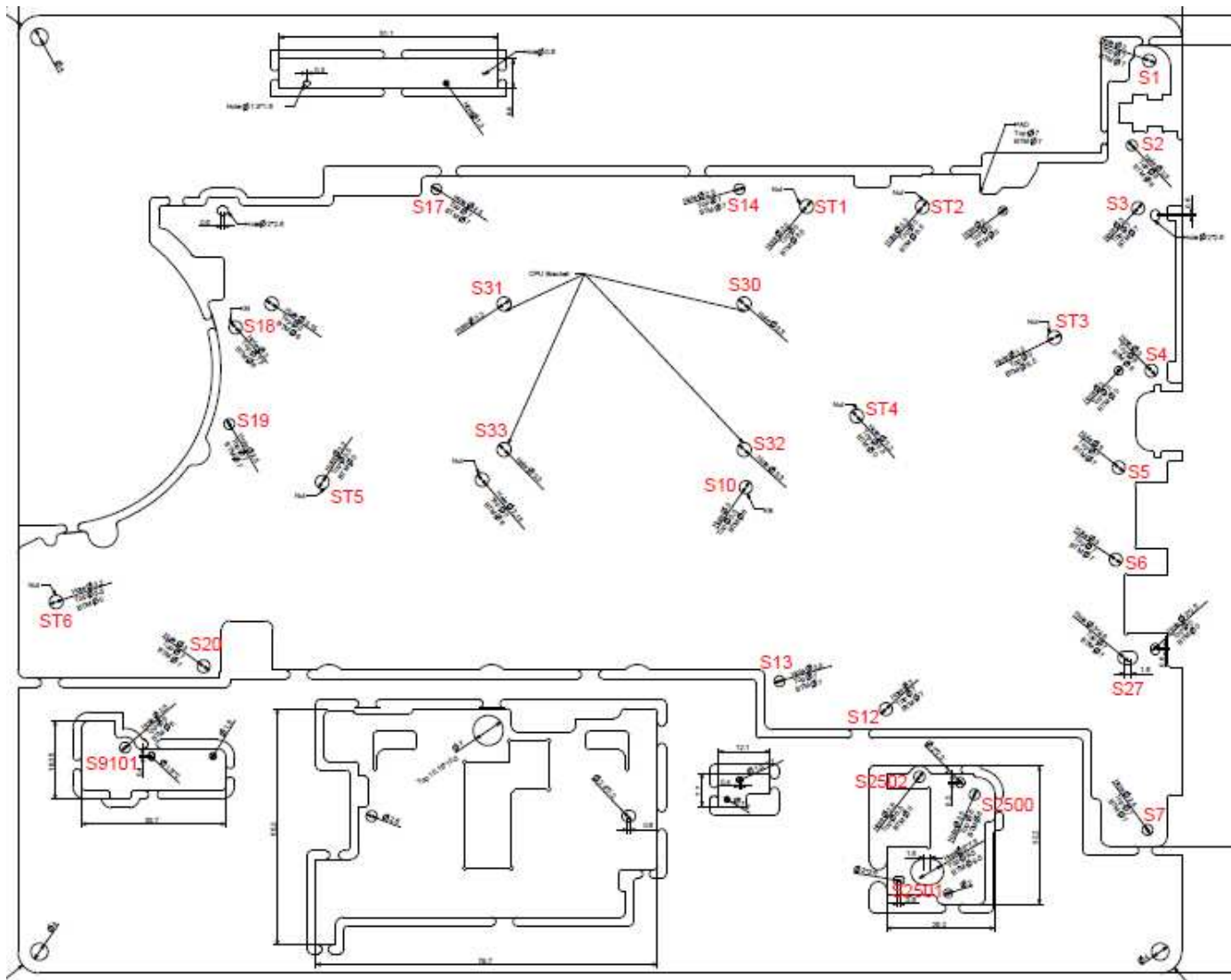
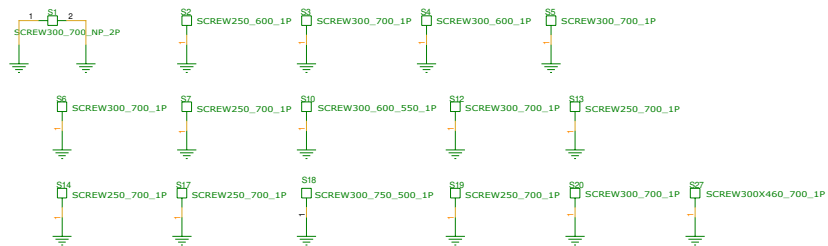
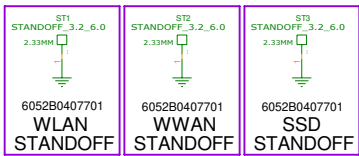
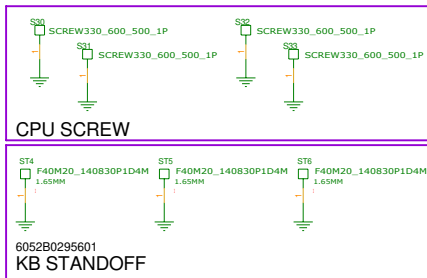


MIC DOUGHTER BOARD

LOCATION NUMBER:9350~9399



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION MIC_BOARD			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		64 of 66	



CHANGE#		xxx	DATE	21-OCT-2002	SIZE	CODE	DOCNUMBER	REV
PCBPN		60xxxxxxxxxx	PCBVER	xxx	A5	CS	1310xxxxx-2-0	X01
SHEET		65			of 65			

TITLE		
MODEL_PROJECT_FUNCTION		
Block Diagram		

