Ares-2 (LAR-2)

AMD CEZANNE Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

DY	*DUMMY*
PCBID	*PCB NO. control for SW*
SKUID	*CPU Type change for SW*
MEM_IDx_x	*Memory ID for SW*
DDR4_CTRL	*SDP DDP setting*
SDP/DDP	*Select single DIE (SDP) Dual DIE(DDP)*
HDT	*Debug Connectors*
EMC	*For EMC test request*
PSL	*KBC PSL model control*
YOGA,YOGA2	*YOGA model setting*
ZZ	*For Test Piont /Hole /ShortPad*
MS	*Modern stand by*
DASH/NON_DASH	*DASH function control*
YOGA/CLAMSHELL	*YOGA/CLAMSHELL control*
dTPM/fTPM	*TPM/NON_TPM control*
WOV/NON_WOV	*WOV control*

LAR2 CZ

緯創資通 **Wistron Corporation**
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Title: ***COVER PAGE***

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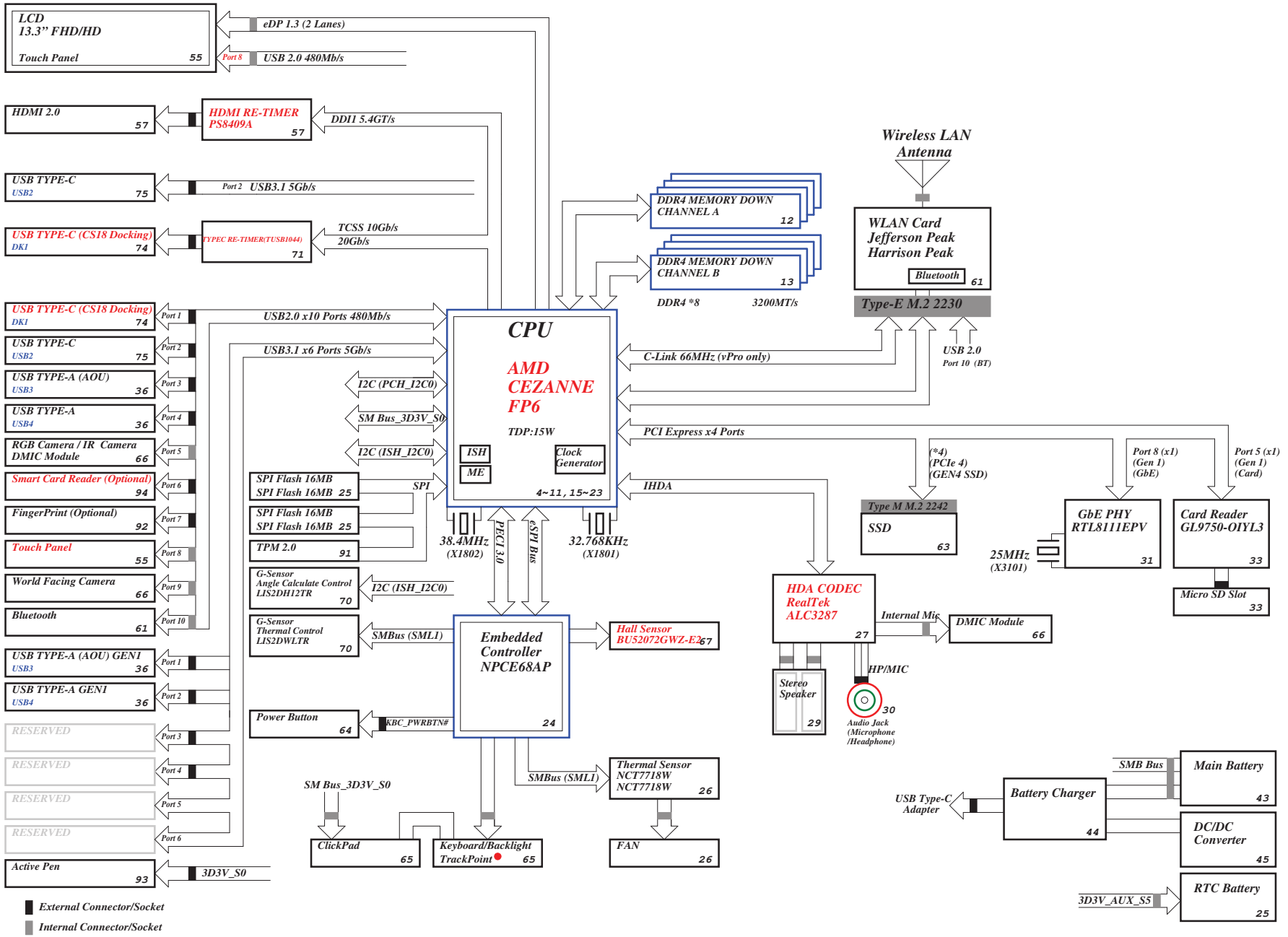
AMD CEZANNE Block Diagram

Project Code: 4PD0P7010001
PCB(Raw Card): 203088-SD



PCB Layer Stackup

10 Layers
L1: Component (TOP)
L2: GND
L3: Signal
L4: GND
L5: Signal
L6: Signal
L7: GND
L8: Signal
L9: GND
L10:Component (BOTTOM)

Battery Charger/Selector BQ25710RSNR 44		
20V_VINT_IN	19V_DCBATOUT BT+	
System DC/DC 5V SY8288CRAC 45		
19V_DCBATOUT	5V_S5 5V_AUX_S5	
System DC/DC 3D3V SY8288BRAC 45		
19V_DCBATOUT	3D3V_S5 3D3V_AUX_S5	
VCORE MP2945GU 46		
VCORE MP86901 47		
19V_DCBATOUT	1V_CPU_CORE	
VDDCR_SOC MP86901 48		
19V_DCBATOUT	1V_VDDCR_SOC	
50		
DC/DC 1D2V_S3 RT8231CGQW 51		
19V_DCBATOUT	1D2V_S3	
DC/DC 0D6V_VREF_S0 RT8231CGQW 51		
1D2V_S3	0D6V_VREF_S0	
DC/DC 2D5V_S5 APL5934 51		
5V_S5	2D5V_S3	
DC/DC 0D75V_S5 RT5753 52		
3D3V_S5	0D75V_S5	
DC/DC 0D75V_S0 RT5753 52		
3D3V_S5	0D75V_S0	
DC/DC 1D8V_S5 SY8386RHC 53		
19V_DCBATOUT	1D8V_S5	

LAR2 CZ

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Title: BLOCK DIAGRAM

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SSID = PCH

SSD1 M.2 (PCIE)

63	SSD_PCIE_RX_P0
63	SSD_PCIE_RX_N0
63	SSD_PCIE_RX_P1
63	SSD_PCIE_RX_N1
63	SSD_PCIE_RX_P2
63	SSD_PCIE_RX_N2
63	SSD_PCIE_RX_P3
63	SSD_PCIE_RX_N3
63	SSD_PCIE_TX_CON_P0
63	SSD_PCIE_TX_CON_N0
63	SSD_PCIE_TX_CON_P1
63	SSD_PCIE_TX_CON_N1
63	SSD_PCIE_TX_CON_P2
63	SSD_PCIE_TX_CON_N2
63	SSD_PCIE_TX_CON_P3
63	SSD_PCIE_TX_CON_N3

SD CARD

33	SD_PCIE_RX_N
33	SD_PCIE_RX_P
33	SD_PCIE_TX_C_N
33	SD_PCIE_TX_C_P

NIC GLAN

31	LAN_PCIE_RX_N
31	LAN_PCIE_RX_P
31	LAN_PCIE_TX_C_P
31	LAN_PCIE_TX_C_N

WLAN

61	WLAN_PCIE_RX_N
61	WLAN_PCIE_RX_P
61	WLAN_PCIE_TX_CON_N
61	WLAN_PCIE_TX_CON_P

IR CAMARA

56	CCD_PCIE_RX_N
56	CCD_PCIE_RX_P
56	CCD_PCIE_TX_C_N
56	CCD_PCIE_TX_C_P

GFX & GPP, 85Ω

APU1B

PCIE

G13	P_GFX_RXP0	P_GFX_TXP0	F4
F13	P_GFX_RXN0	P_GFX_TXN0	F2
J14	P_GFX_RXP1	P_GFX_TXP1	F3
H14	P_GFX_RXN1	P_GFX_TXN1	E4
G15	P_GFX_RXP2	P_GFX_TXP2	E1
F15	P_GFX_RXN2	P_GFX_TXN2	C1
J15	P_GFX_RXP3	P_GFX_TXP3	D5
K15	P_GFX_RXN3	P_GFX_TXN3	E6
H16	P_GFX_RXP4	P_GFX_TXP4	C6
J16	P_GFX_RXN4	P_GFX_TXN4	D6
F18	P_GFX_RXP5	P_GFX_TXP5	B6
G18	P_GFX_RXN5	P_GFX_TXN5	C7
J18	P_GFX_RXP6	P_GFX_TXP6	D8
K18	P_GFX_RXN6	P_GFX_TXN6	B8
H19	P_GFX_RXP7	P_GFX_TXP7	C8
G19	P_GFX_RXN7	P_GFX_TXN7	A8

M.2 SSD1 (PCIE)

SSD_PCIE_RX_P0	G11	P_GPP_RXP0	P_GPP_TXP0	L3	SSD_PCIE_TX_P0	C305 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_P0
SSD_PCIE_RX_N0	F11	P_GPP_RXN0	P_GPP_TXN0	L1	SSD_PCIE_TX_N0	C306 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_N0
SSD_PCIE_RX_P1	J10	P_GPP_RXP1	P_GPP_TXP1	L4	SSD_PCIE_TX_P1	C307 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_P1
SSD_PCIE_RX_N1	H10	P_GPP_RXN1	P_GPP_TXN1	L2	SSD_PCIE_TX_N1	C308 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_N1
SSD_PCIE_RX_P2	G8	P_GPP_RXP2/SATA0_RXP	P_GPP_TXP2/SATA0_TXP	M4	SSD_PCIE_TX_P2	C309 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_P2
SSD_PCIE_RX_N2	F8	P_GPP_RXN2/SATA0_RXN	P_GPP_TXN2/SATA0_TXN	M2	SSD_PCIE_TX_N2	C310 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_N2
SSD_PCIE_RX_P3	G6	P_GPP_RXP3/SATA1_RXP	P_GPP_TXP3/SATA1_TXP	N3	SSD_PCIE_TX_P3	C311 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_P3
SSD_PCIE_RX_N3	F7	P_GPP_RXN3/SATA1_RXN	P_GPP_TXN3/SATA1_TXN	N1	SSD_PCIE_TX_N3	C312 1 2	SCD22U10V2KX-1GP SSD_PCIE_TX_CON_N3

M.2 SSD1 (PCIE)

IR CAMARA

SD CARD

NIC GLAN

WLAN

CCD_PCIE_RX_P	M9	P_GPP_RXP4	P_GPP_TXP4	T2	CCD_PCIE_TX_P	C313 1 2	SCD1U6D3V1KX-GP CCD_PCIE_TX_C_P
CCD_PCIE_RX_N	M8	P_GPP_RXN4	P_GPP_TXN4	T4	CCD_PCIE_TX_N	C314 1 2	SCD1U6D3V1KX-GP CCD_PCIE_TX_C_N
SD_PCIE_RX_P	L7	P_GPP_RXP5	P_GPP_TXP5	R1	SD_PCIE_TX_P	C315 1 2	SCD1U6D3V1KX-GP SD_PCIE_TX_C_P
SD_PCIE_RX_N	L6	P_GPP_RXN5	P_GPP_TXN5	R3	SD_PCIE_TX_N	C316 1 2	SCD1U6D3V1KX-GP SD_PCIE_TX_C_N
LAN_PCIE_RX_P	K7	P_GPP_RXP6	P_GPP_TXP6	P2	LAN_PCIE_TX_P	C317 1 2	SCD1U6D3V1KX-GP LAN_PCIE_TX_C_P
LAN_PCIE_RX_N	K8	P_GPP_RXN6	P_GPP_TXN6	P4	LAN_PCIE_TX_N	C318 1 2	SCD1U6D3V1KX-GP LAN_PCIE_TX_C_N
WLAN_PCIE_RX_P	H6	P_GPP_RXP7	P_GPP_TXP7	N2	WLAN_PCIE_TX_P	C303 1 2	SCD1U16V2KX-3GP WLAN_PCIE_TX_CON_P
WLAN_PCIE_RX_N	H7	P_GPP_RXN7	P_GPP_TXN7	N4	WLAN_PCIE_TX_N	C304 1 2	SCD1U16V2KX-3GP WLAN_PCIE_TX_CON_N

L9	P_GPP_RXP8/SATA2_RXP	P_GPP_TXP8/SATA2_TXP	K2
L10	P_GPP_RXN8/SATA2_RXN	P_GPP_TXN8/SATA2_TXN	K4
K11	P_GPP_RXP9/SATA3_RXP	P_GPP_TXP9/SATA3_TXP	J4
J11	P_GPP_RXN9/SATA3_RXN	P_GPP_TXN9/SATA3_TXN	J2
J12	P_GPP_RXP10	P_GPP_TXP10	H3
H12	P_GPP_RXN10	P_GPP_TXN10	H1
J13	P_GPP_RXP11	P_GPP_TXP11	H4
K13	P_GPP_RXN11	P_GPP_TXN11	H2

FP6 REV 0.92
PART 2 OF 13

RENOIR-FP6-GP

ZZ.00CPU.421

LAR2 CZ

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Title: CPU (PCIE/SATA)

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5 4 3 2 1

D

C

B

A

(Blanking)

LAR2 CZ

緯創資通

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Title

CPU (RSVD)

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

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SSID = CPU

APU Type 2 does not support Channel A

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer

APU1A

MEMORY A

M_A_A0 AK26 MA_ADD0/RSVD
M_A_A1 AG24 MA_ADD1/RSVD
M_A_A2 AG23 MA_ADD2/MAB_CA0
M_A_A3 AG26 MA_ADD3/MAA_CA4
M_A_A4 AG27 MA_ADD4/MAA_CA5
M_A_A5 AF21 MA_ADD5/MAA_CA3
M_A_A6 AF22 MA_ADD6/MAA_CA2
M_A_A7 AF25 MA_ADD7/RSVD
M_A_A8 AF24 MA_ADD8/RSVD
M_A_A9 AE21 MA_ADD9/RSVD
M_A_A10 AL21 MA_ADD10/MAB_CS_L1
M_A_A11 AF27 MA_ADD11/MAA_CKE1
M_A_A12 AE23 MA_ADD12/MAA_CKE0
M_A_A13 AM23 MA_ADD13_BANK2/RSVD
M_A_A14 AM21 MA_WE_L_ADD14/MAB_CKE1
M_A_A15 AL27 MA_CAS_L_ADD15/RSVD
M_A_A16 AL24 MA_RAS_L_ADD16/MAB_CKE0

M_A_BA0 AL22 MA_BANK0/MAB_CS_L0
M_A_BA1 AK27 MA_BANK1/MAB_CA1

M_A_BG0 AE27 MA_BG0/MAA_CS_L1
M_A_BG1 AE26 MA_BG1/MAA_CS_L0

M_A_ACT_N AD22 MA_ACT_L/RSVD

M_A_DM0 L27 MA_DM0/MAA_DM1
M_A_DM1 N23 MA_DM1/MAA_DM0
M_A_DM2 R27 MA_DM2/MAA_DM2
M_A_DM3 Y24 MA_DM3/MAA_DM3
M_A_DM4 AP27 MA_DM4/MAB_DM2
M_A_DM5 AW23 MA_DM5/MAB_DM3
M_A_DM6 AT21 MA_DM6/MAB_DM1
M_A_DM7 AV18 MA_DM7/MAB_DM0
W24 RSVD_52

M_A_DQS_DP0 M25 MA_DQS_H0/MAA_DQS_H1
M_A_DQS_DN0 M24 MA_DQS_L0/MAA_DQS_L1
M_A_DQS_DP1 P22 MA_DQS_H1/MAA_DQS_H0
M_A_DQS_DN1 P21 MA_DQS_L1/MAA_DQS_L0
M_A_DQS_DP2 T24 MA_DQS_H2/MAA_DQS_H2
M_A_DQS_DN2 R24 MA_DQS_L2/MAA_DQS_L2
M_A_DQS_DP3 AA21 MA_DQS_H3/MAA_DQS_H3
M_A_DQS_DN3 Y21 MA_DQS_L3/MAA_DQS_L3
M_A_DQS_DP4 AP23 MA_DQS_H4/MAB_DQS_H2
M_A_DQS_DN4 AP24 MA_DQS_L4/MAB_DQS_L2
M_A_DQS_DP5 AW22 MA_DQS_H5/MAB_DQS_H3
M_A_DQS_DN5 AV22 MA_DQS_L5/MAB_DQS_L3
M_A_DQS_DP6 AT20 MA_DQS_H6/MAB_DQS_H1
M_A_DQS_DN6 AR20 MA_DQS_L6/MAB_DQS_L1
M_A_DQS_DP7 AR18 MA_DQS_H7/MAB_DQS_H0
M_A_DQS_DN7 AT18 MA_DQS_L7/MAB_DQS_L0
Y26 RSVD_58
Y27 RSVD_59

M_A_CLK_P0 AJ25 MA_CLK_H0/MAA_CKT
M_A_CLK_N0 AJ24 MA_CLK_L0/MAA_CKC
AJ22 MA_CLK_H1/MAB_CKT
AJ21 MA_CLK_L1/MAB_CKC

M_A_CS0_N AL25 MA_CS_L0/MAB_CA2
AM26 MA_CS_L1/MAB_CA5

M_A_CKE0 AD24 MA_CKE0/MAA_CA1
AD25 MA_CKE1/MAA_CA0

M_A_ODT0 AM24 MA_ODT0/MAB_CA3
AM27 MA_ODT1/MAB_CA4

M_A_ALERT_N AE24 MA_ALERT_L/TEST31A
M_A_EVENT_N AK23 MA_EVENT_L
SM_DRAMRST_N_A AD27 MA_RESET_L

FP6 REV 0.92
PART 1 OF 13

RENOIR-FP6-GP

ZZ.00CPU.421

MA_DATA0/MAA_DATA8 K27 M_A_DQ0
MA_DATA1/MAA_DATA9 L26 M_A_DQ1
MA_DATA2/MAA_DATA13 N26 M_A_DQ2
MA_DATA3/MAA_DATA12 N27 M_A_DQ3
MA_DATA4/MAA_DATA11 G27 M_A_DQ4
MA_DATA5/MAA_DATA10 H27 M_A_DQ5
MA_DATA6/MAA_DATA15 M27 M_A_DQ6
MA_DATA7/MAA_DATA14 N24 M_A_DQ7

MA_DATA8/MAA_DATA0 L23 M_A_DQ8
MA_DATA9/MAA_DATA1 N21 M_A_DQ9
MA_DATA10/MAA_DATA5 T21 M_A_DQ10
MA_DATA11/MAA_DATA4 T22 M_A_DQ11
MA_DATA12/MAA_DATA7 M22 M_A_DQ12
MA_DATA13/MAA_DATA6 L24 M_A_DQ13
MA_DATA14/MAA_DATA2 R21 M_A_DQ14
MA_DATA15/MAA_DATA3 R23 M_A_DQ15

MA_DATA16/MAA_DATA17 P24 M_A_DQ16
MA_DATA17/MAA_DATA16 R26 M_A_DQ17
MA_DATA18/MAA_DATA21 T27 M_A_DQ18
MA_DATA19/MAA_DATA20 V27 M_A_DQ19
MA_DATA20/MAA_DATA19 P25 M_A_DQ20
MA_DATA21/MAA_DATA18 P27 M_A_DQ21
MA_DATA22/MAA_DATA23 V23 M_A_DQ22
MA_DATA23/MAA_DATA22 T25 M_A_DQ23

MA_DATA24/MAA_DATA30 W22 M_A_DQ24
MA_DATA25/MAA_DATA31 Y23 M_A_DQ25
MA_DATA26/MAA_DATA26 AC24 M_A_DQ26
MA_DATA27/MAA_DATA27 AC23 M_A_DQ27
MA_DATA28/MAA_DATA28 V21 M_A_DQ28
MA_DATA29/MAA_DATA29 W21 M_A_DQ29
MA_DATA30/MAA_DATA24 AA24 M_A_DQ30
MA_DATA31/MAA_DATA25 AA22 M_A_DQ31

MA_DATA32/MAB_DATA17 AP26 M_A_DQ32
MA_DATA33/MAB_DATA16 AN24 M_A_DQ33
MA_DATA34/MAB_DATA21 AR25 M_A_DQ34
MA_DATA35/MAB_DATA20 AU26 M_A_DQ35
MA_DATA36/MAB_DATA19 AN25 M_A_DQ36
MA_DATA37/MAB_DATA18 AN27 M_A_DQ37
MA_DATA38/MAB_DATA23 AR27 M_A_DQ38
MA_DATA39/MAB_DATA22 AU27 M_A_DQ39

MA_DATA40/MAB_DATA30 AV25 M_A_DQ40
MA_DATA41/MAB_DATA31 AW25 M_A_DQ41
MA_DATA42/MAB_DATA26 AV20 M_A_DQ42
MA_DATA43/MAB_DATA27 AW20 M_A_DQ43
MA_DATA44/MAB_DATA28 AV27 M_A_DQ44
MA_DATA45/MAB_DATA29 AW26 M_A_DQ45
MA_DATA46/MAB_DATA24 AU21 M_A_DQ46
MA_DATA47/MAB_DATA25 AW21 M_A_DQ47

MA_DATA48/MAB_DATA11 AT22 M_A_DQ48
MA_DATA49/MAB_DATA10 AP21 M_A_DQ49
MA_DATA50/MAB_DATA14 AN19 M_A_DQ50
MA_DATA51/MAB_DATA15 AN18 M_A_DQ51
MA_DATA52/MAB_DATA12 AU23 M_A_DQ52
MA_DATA53/MAB_DATA13 AR22 M_A_DQ53
MA_DATA54/MAB_DATA9 AN20 M_A_DQ54
MA_DATA55/MAB_DATA8 AP19 M_A_DQ55

MA_DATA56/MAB_DATA6 AT19 M_A_DQ56
MA_DATA57/MAB_DATA7 AW18 M_A_DQ57
MA_DATA58/MAB_DATA2 AU16 M_A_DQ58
MA_DATA59/MAB_DATA3 AW16 M_A_DQ59
MA_DATA60/MAB_DATA4 AW19 M_A_DQ60
MA_DATA61/MAB_DATA5 AU19 M_A_DQ61
MA_DATA62/MAB_DATA1 AP16 M_A_DQ62
MA_DATA63/MAB_DATA0 AT16 M_A_DQ63

RSVD_54 W27
RSVD_53 W25
RSVD_68 AC25
RSVD_69 AC27
RSVD_49 V26
RSVD_48 V24
RSVD_63 AA27
RSVD_62 AA25

MA_PAROUT/RSVD AK24 M_A_PARITY

M_DDR4
M_LPDDR4
AN21
AN22

1D2V_S3

Follow CRB 20190423

1D2V_S3

R501
1KR2J-1-GP

M_A_EVENT_N

12 M_A_A0
12 M_A_A1
12 M_A_A2
12 M_A_A3
12 M_A_A4
12 M_A_A5
12 M_A_A6
12 M_A_A7
12 M_A_A8
12 M_A_A9
12 M_A_A10
12 M_A_A11
12 M_A_A12
12 M_A_A13
12 M_A_A14
12 M_A_A15
12 M_A_A16

12 M_A_BA0
12 M_A_BA1
12 M_A_BG0
12 M_A_BG1
12 M_A_ACT_N

12 M_A_DM0
12 M_A_DM1
12 M_A_DM2
12 M_A_DM3
12 M_A_DM4
12 M_A_DM5
12 M_A_DM6
12 M_A_DM7

12 M_A_CLK_P0
12 M_A_CLK_N0

12 M_A_CS0_N

12 M_A_CKE0

12 M_A_ODT0

12 M_A_ALERT_N

12 SM_DRAMRST_N_A

12 M_A_PARITY

M_A_DQS_DN0
M_A_DQS_DN1
M_A_DQS_DN2
M_A_DQS_DN3
M_A_DQS_DN4
M_A_DQS_DN5
M_A_DQS_DN6
M_A_DQS_DN7
M_A_DQS_DN[7:0] 12

M_A_DQS_DP0
M_A_DQS_DP1
M_A_DQS_DP2
M_A_DQS_DP3
M_A_DQS_DP4
M_A_DQS_DP5
M_A_DQS_DP6
M_A_DQS_DP7
M_A_DQS_DP[7:0] 12

M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ8
M_A_DQ9
M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
M_A_DQ16
M_A_DQ17
M_A_DQ18
M_A_DQ19
M_A_DQ20
M_A_DQ21
M_A_DQ22
M_A_DQ23
M_A_DQ24
M_A_DQ25
M_A_DQ26
M_A_DQ27
M_A_DQ28
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M_A_DQ30
M_A_DQ31
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M_A_A10
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M_A_A[16:0] 12

LAR2 CZ

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Title: **CPU (DDR4_CHA)**

Size: A3 | Document Number: **LAR-2 CZ** | Rev: **-2**

Date: Wednesday, July 28, 2021 | Sheet 5 of 106

SSID = CPU

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer

Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc. M_PAROUT	M_RESET_L	M_EVENT_L	M_ALERT	

APU1I

MEMORY B

RENOIR-FP6-GP

FP6 REV 0.92
PART 9 OF 13

ZZ.00CPU.421

1D2V_S3

R601 1KR2J-1-GP

LAR2 CZ

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Title: CPU (DDR4_CHB)

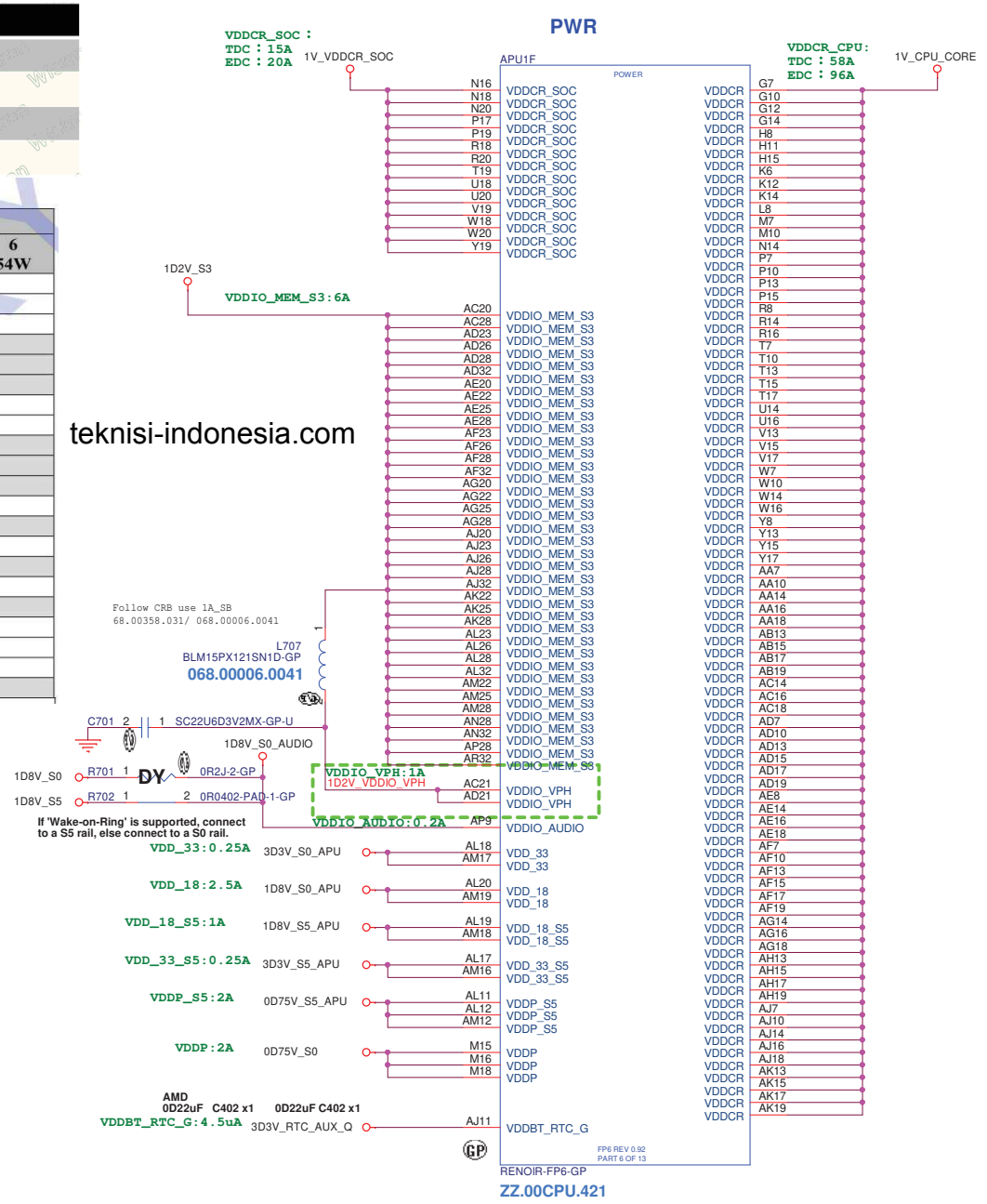
Size: A3 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 6 of 106

SVI	FP4 – Bristol Ridge	FP5 – Raven Ridge
Supply 1	VDDCR_CPU – x86 Cores	VDDCR_VDD – x86 Cores, GPU
Supply 2	VDDCR_NB – Rest Of Chip	VDDCR_SOC – Rest Of Chip
Supply 3	VDDCR_GFX – GPU	N/A
Sum@15W	TDC: 56A, EDC: 87A	TDC: 45A, EDC: 58A

Table 5. FP6 Processor Voltage Supply Currents

Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION 1 10W	2 15W	3 25W	4 35W	5 45W	6 54W
VDDCR_VDD	Variable (0.65–TBD)[5]	TDC [3]	20	33	44	51	58	
		EDC	34	50	70	90	96	
		Max Loadstep [4]	29	43	65	76	84	
VDDCR_SOC	Variable (0.7–TBD)[5]	TDC [3]	10	13			15	
		EDC	13	17			20	
		Max Loadstep [4]						
VDDIO_MEM_S3[6]	1.10	TDC	6.00					
	1.20	TDC	6.00					
VDDIO_VPH[7]	1.10	TDC	1.00					
	1.20	TDC	1.00					
	1.80	TDC	1.00					
VDDP	0.75	TDC	2.00					
VDDP_S5	0.75	TDC	2.00					
VDD_18	1.80	TDC	2.50					
VDD_18_S5	1.80	TDC	1.00					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	3.00	TDC	4.5µA					



15.3.5 VDDIO _ VPH Power Delivery and Decoupling

VDDIO _ VPH is the dedicated supply voltage for DisplayPort 0 and PCIe phys . When DisplayPort 0 is used for eDP , the source of VDDIO _ VPH can be the same source as VDDIO _ MEM _ S 3. This allows lower power and better battery life . When DisplayPort 0 is used for DP or TMDS , the source of VDDIO _ VPH can be the same source as VDD _18.

LAR2 CZ

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Title: **CPU (POWER)**

Size	Document Number	Rev
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Date: Wednesday, July 28, 2021 Sheet 7 of 106

SSID = PCH

DISPLAY/SVI/JTAG/TEST

APU Type I(CZ): 1D8V
APU Type II(CZ-L): 3D3V

APU Type I 1D8V
APU Type II 3D3V

PINOUT	Description
DP_BLON	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

DisplayPort	Device
0	eDP
1	HDMI
2	
3	

eDP

55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
24 PANEL_BLEN
55 EDP_VDD_EN
55 PANEL_BKLTCTL
55 EDP_AUX_CPU_P
55 EDP_AUX_CPU_N
55 EDP_HPD_CPU

HDMI

57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_HPD_CPU

HDT

68 APU_TDI
68 APU_TDO
68 APU_TCK
68 APU_TMS
68 APU_TRST_N
68 APU_DBREQ_N

68,73 RST_CPU_N
46,68 PWR_SVID_PWRGD

24,44,46 PROCHOT_CPU_N

SVID

46 SVID_CLK_CPU
46 SVID_DATA_CPU
46 SVID_ALERT_CPU_N

46 VDDNB_SENSE
46 VCCCORE_SENSE
46 VSSCORE_SENSE
52 VDDP_S5_SENSE
52 VDDP_S0_SENSE
51 VDDIO_MEM_S3_SENSE

24,96 CPU_SMB_SDA_EC
24,96 CPU_SMB_SCL_EC

75 USB2_TCSS_AUX_CPU_P
75 USB2_TCSS_AUX_CPU_N
73 USB2_TPC_HPD
71 TYPEC_AUX_CPU_P
71 TYPEC_AUX_CPU_N
73 TYPEC_TPC_HPD

96 CPU_SMB_SDA
96 CPU_SMB_SCL

1D8V_S5
RN803 1 2 4 3 RST_CPU_N PWR_SVID_PWRGD
SRN4K7J-8-GP

HDT EVT stage要上

1D8V_S5
HDT PIN Pull High Resistor
ASM if HDT CONN is needs of use
RN804 1 2 3 4 8 7 6 5 APU_TDI APU_TCK APU_TRST_N APU_DBREQ_N
SRN1KJ-4-GP
R805 1 APU_TMS
1KR2J-1-GP

3D3V_S0
RN801 1 2 4 3 PROCHOT_CPU_N ALERT_N_CPU
SRN1KJ-7-GP
RN802 1 2 4 3 CPU_SMB_SCL CPU_SMB_SDA
SRN1KJ-7-GP
R803 1 THERMTRIP_N_CPU
1KR2J-1-GP

C821 1 SC27P50V2JN-2-GP RST_CPU_N
C822 1 SC27P50V2JN-2-GP PWR_SVID_PWRGD

1D8V_S0
RN805 2 1 4 CPU_SMB_SCL CPU_SMB_SDA
SRN1KJ-7-GP

RN801 change to 4 pin from 8 pin & add RN802
Add RN803 RSVD SIC/ SID 1D8V_S0 signal
Reserve 1.8v pull up at SIC & SID of CPU (Right now pull up 3.3v)_-1

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

APU1C
DISPLAY/SVI2/JTAG/TEST

eDP
eDP_TX_CPU_P0 D11 DP0_TXP0
eDP_TX_CPU_N0 B11 DP0_TXN0
eDP_TX_CPU_P1 C11 DP0_TXP1
eDP_TX_CPU_N1 A11 DP0_TXN1
D10 DP0_TXP2
B10 DP0_TXN2
D9 DP0_TXP3
B9 DP0_TXN3

HDMI
HDMI_DDI_TX_P0 G23 DP1_TXP0
HDMI_DDI_TX_N0 H23 DP1_TXN0
HDMI_DDI_TX_P1 F22 DP1_TXP1
HDMI_DDI_TX_N1 G22 DP1_TXN1
HDMI_DDI_TX_P2 G21 DP1_TXP2
HDMI_DDI_TX_N2 H21 DP1_TXN2
HDMI_DDI_TX_P3 F20 DP1_TXP3
HDMI_DDI_TX_N3 G20 DP1_TXN3

DP_BLON A22 PANEL_BLEN
DP_DIGON D23 EDP_VDD_EN
DP_VARY_BL C23 PANEL_BKLTCTL
D12 EDP_AUX_CPU_P DP0_AUXP
B12 EDP_AUX_CPU_N DP0_AUXN
C12 EDP_HPD_CPU DP0_HPD
J20 HDMI_SCL_CPU DP1_AUXP
K20 HDMI_SDA_CPU DP1_AUXN
L21 HDMI_HPD_CPU DP1_HPD
L19 TYPEC_AUX_CPU_P DP2_AUXP
M19 TYPEC_AUX_CPU_N DP2_AUXN
M20 TYPEC_TPC_HPD DP2_HPD
M14 USB2_TCSS_AUX_CPU_P DP3_AUXP
L14 USB2_TCSS_AUX_CPU_N DP3_AUXN
L16 USB2_TPC_HPD DP3_HPD
B23 DP_STEREOSYNC_APU DP_STEREOSYNC

eDP
R840 10KR2F-2-GP
R841 10KR2F-2-GP
HDMI
DOCK
TYPEC USB2

3D3V_S0
RN806 SRN2K2J-5-GP
HDMI_SCL_CPU
HDMI_SDA_CPU

TEST4 BB6 TEST4 TP808
TEST5 BD5 TEST5 TP807
TEST6 AG12
TEST14 G25 TEST14_APU TP810
TEST15 K25 TEST15_APU TP811
TEST16 F25 TEST16_APU TP812
TEST17 F26 TEST17_APU TP813
TEST31 H26 TEST31_APU TP802
TEST41 AK9 TEST41 TP809
ANALOGIO_0 AK21
ANALOGIO_1 AG21

HDT
APU_TDI AP3 TDI
APU_TDO AU1 TDO
APU_TCK AR2 TCK
APU_TMS AU3 TMS
APU_TRST_N AR4 TRST_L
APU_DBREQ_N AT2 DBREQ_L

HDT
HDT CONN PIN#12 RST_CPU_N AW3
HDT CONN PIN#10 PWR_SVID_PWRGD AW4 RESET# PWROK

CPU_SMB_SCL B22
CPU_SMB_SDA D22 SIC SID
ALERT_N_CPU C22 ALERT_L
THERMTRIP_N_CPU AN9 THERMTRIP_L
PROCHOT_CPU_N B25 PROCHOT_L
an output signal as overtemperature condition

3D3V

SVID
SVID_CLK_CPU D25 SVC0
SVID_DATA_CPU C25 SVD0
SVID_ALERT_CPU_N A25 SVT0

FP6 REV 0.92
PART 3 OF 13
RENOIR-FP6-GP

SMU_ZVDD P3 SMU_ZVDD
R812 1 2 196R2F-GP
0D75V_S0

VDDP_S5_SENSE AK7 VDDP_S5_SENSE_APU R815 0R402-DB-GP-U VDDP_S5_SENSE
VDDP_SENSE AK12 VDDP_S0_SENSE_APU R816 0R402-DB-GP-U VDDP_S0_SENSE
VDDCR_SOC_SENSE J23 VDDNB_SENSE_APU R806 0R402-DB-GP-U VDDNB_SENSE
VDDCR_SENSE K22 VCCCORE_SENSE_APU R807 0R402-DB-GP-U VCCCORE_SENSE
VDDIO_MEM_S3_SENSE J21 VDDIO_MEM_S3_SENSE TP814
VSS_SENSE_A J22 VSS_SENSE_APU R809 0R402-DB-GP-U VSSCORE_SENSE
VSS_SENSE_B AJ12 VSS_SENSEB TP801

ZZ.00CPU.421

C879 C889 C890 SC27P50V2JN-2-GP
if SI is not ok, suggest that install capacitor.
C890 ASM
for SVID Signal Quality test
Alert noise over spec 200mv_SC

VDDNB_SENSE R801 1V_VDDCR_SOC
VCCCORE_SENSE R802 1V_CPU_CORE
VSSCORE_SENSE R804
VSS_SENSEB R817 0R2J-2-GP
100R2F-L3-GP

1D8V_S0 3D3V_S0
R810 0R2J-2-GP
R811 0R0402-PAD-1-GP
3D3V_S0_SIC_SID
CPU_SMB_SDA Q808 CPU_SMB_SDA_EC
2N7002KDW-1-GP
75.27002.F7C
CPU_SMB_SCL_EC
CPU_SMB_SCL

Check list: PD/CRB:PH

1D8V_S0
R837 1KR2F-L1-GP
DP_STEREOSYNC_APU
R808 1KR2J-1-GP

LAR2 CZ

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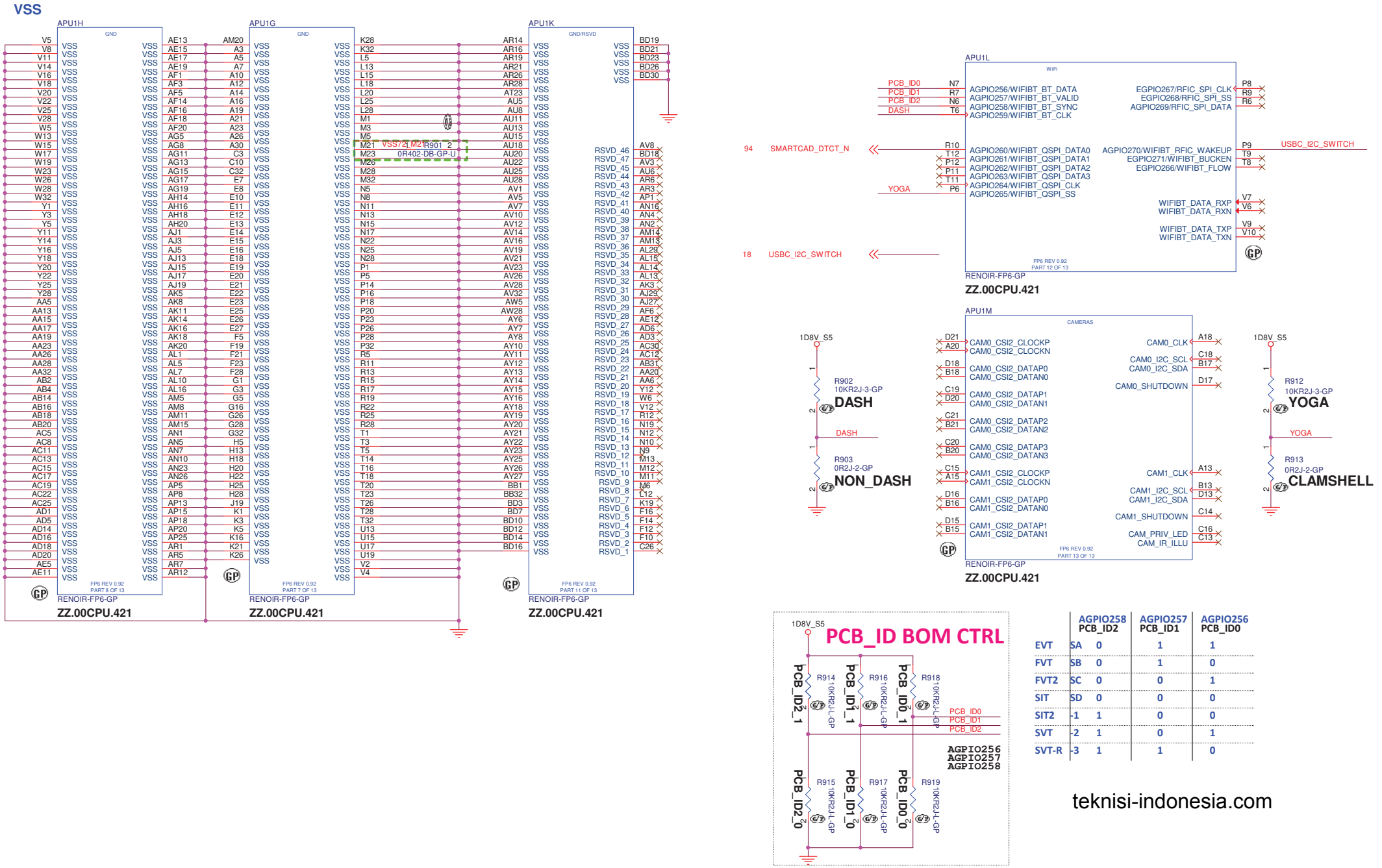
Title: CPU (DP/SVI/JTAG/TEST)
Size: A3
Document Number: LAR-2 CZ
Rev: -2
Date: Wednesday, July 28, 2021
Sheet 8 of 106



	AGPIO258 PCB_ID2		AGPIO257 PCB_ID1	AGPIO256 PCB_ID0
EVT	SA	0	1	1
FVT	SB	0	1	0
FVT2	SC	0	0	1
SIT	SD	0	0	0
SIT2	-1	1	0	0
SVT	-2	1	0	1
SVT-R	-3	1	1	0

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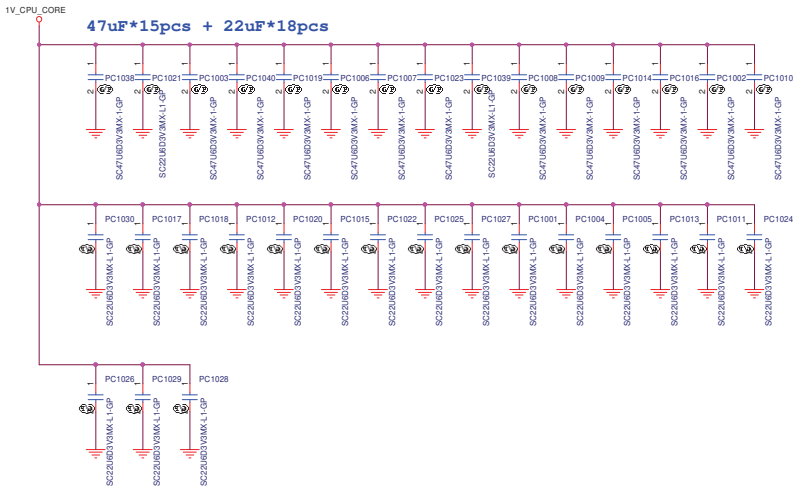
Title: ***CPU (VSS)***

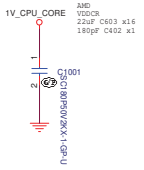
Size: A3 | Document Number: **LAR-2 CZ** | Rev: **-2**

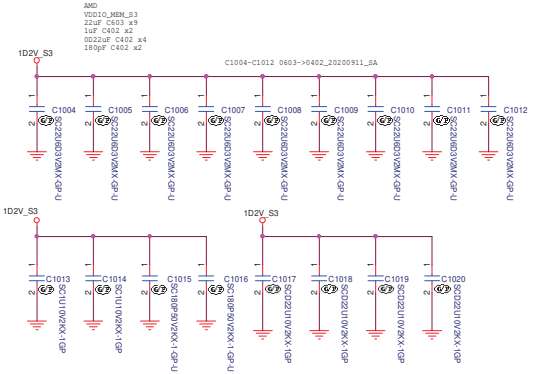
Date: Wednesday, July 28, 2021 | Sheet 9 of 106

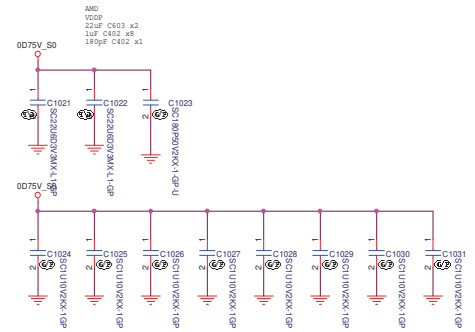
Main Func = CPU

1V_VDDCORE AMD_FP6_25W

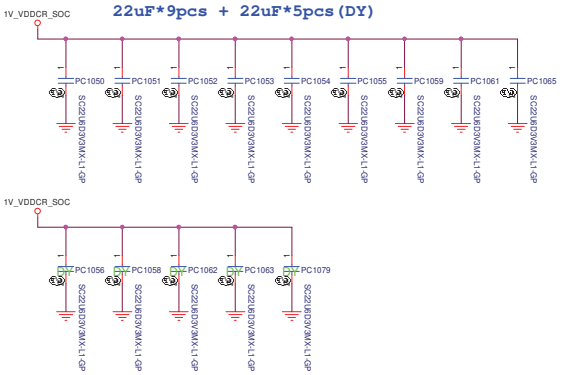


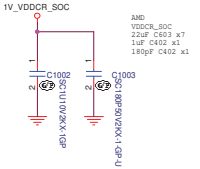






1V_VDDCR_SOC





RED:ASM
YELLOW:DY
GREEN:PC1088 - PC1D04 - PC1056 - PC1057換成 078.22610.05F1 (22uF/0402)
20200629_SC

LAR2 CZ

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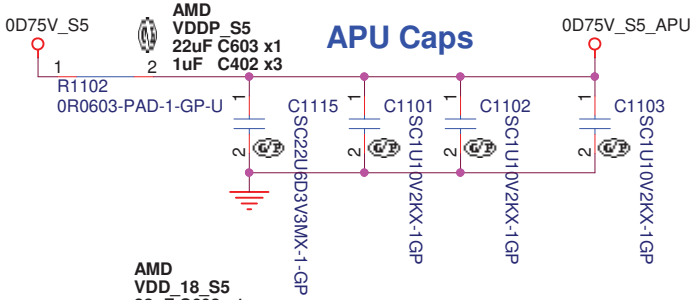
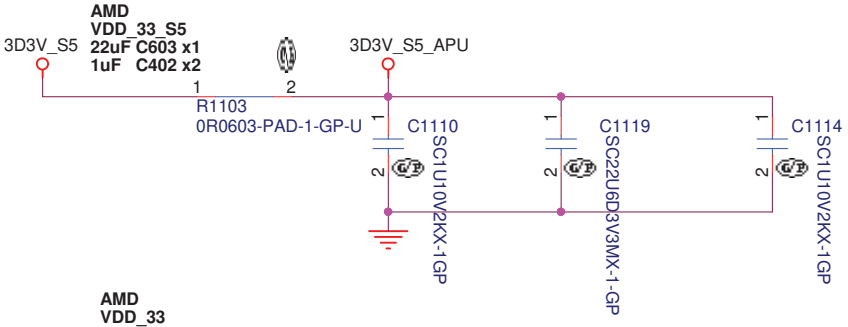
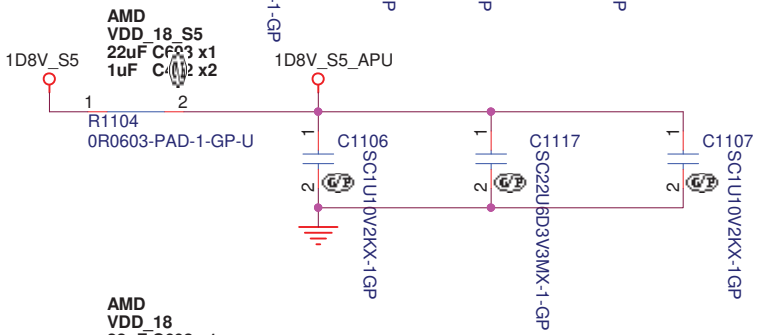
Title: CPU (POWER CAP1)

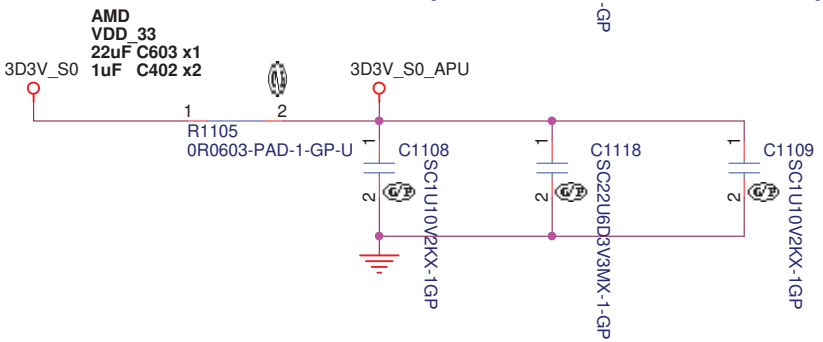
Size	Document Number	Rev
Custom	LAR-2 CZ	-2

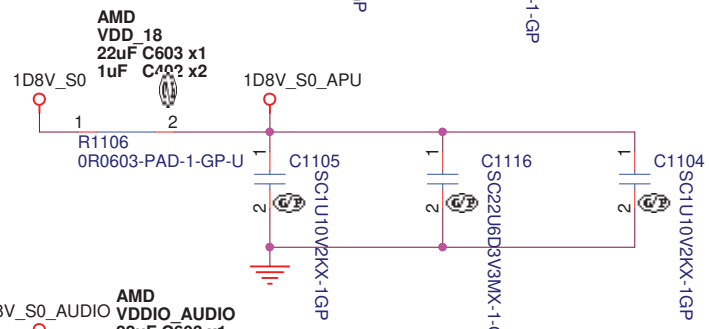
Date: Wednesday, July 28, 2021 Sheet 10 of 106

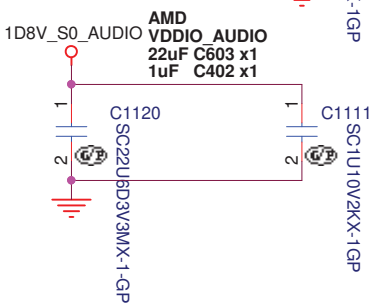












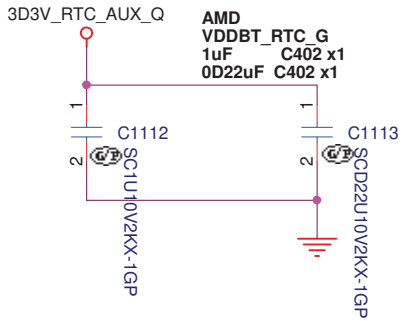


Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3[1, 2]	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 µF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 µF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 µF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

LAR2 CZ

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Title: ***CPU (POWER CAP2)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

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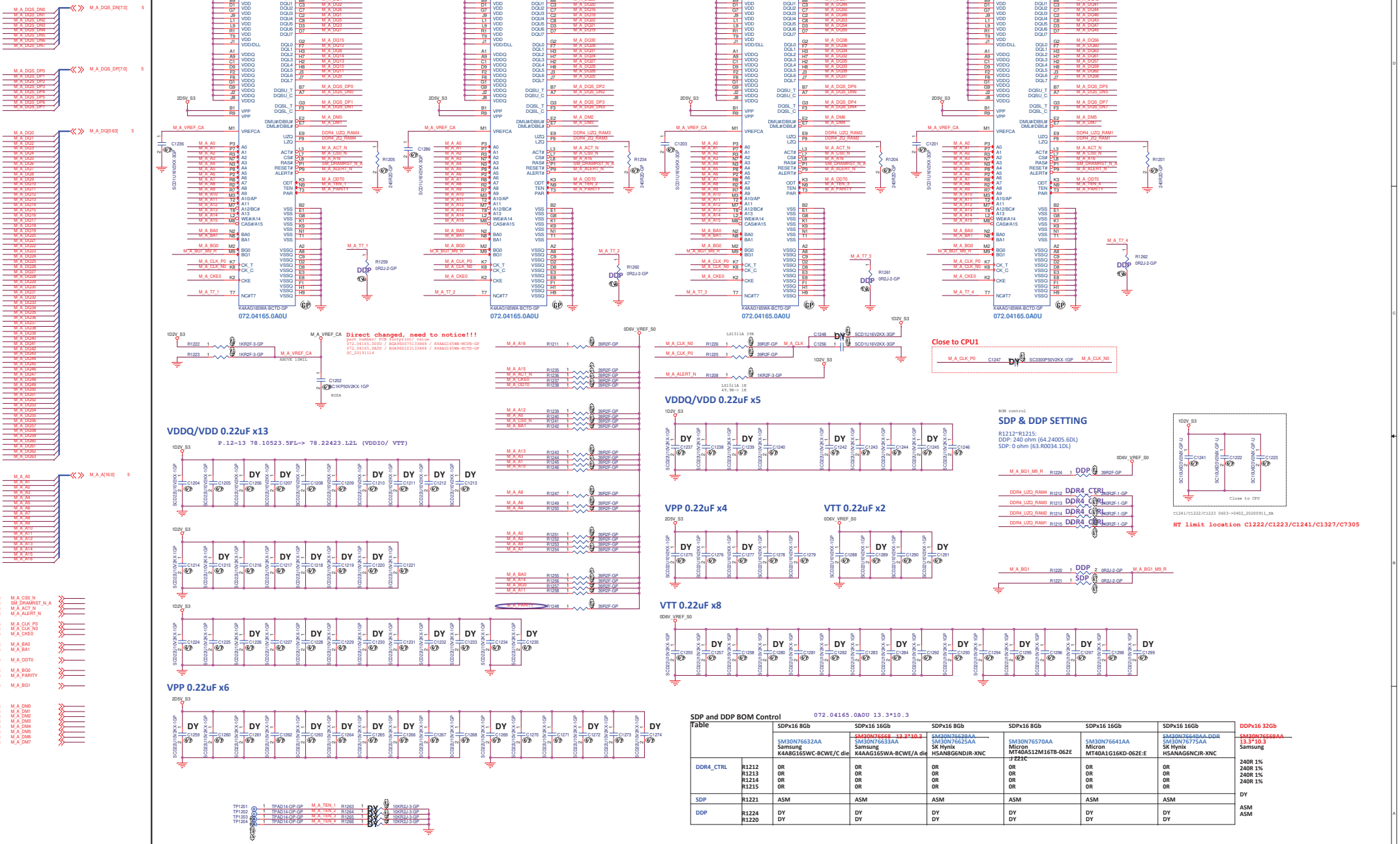
Main Func = DIMM1



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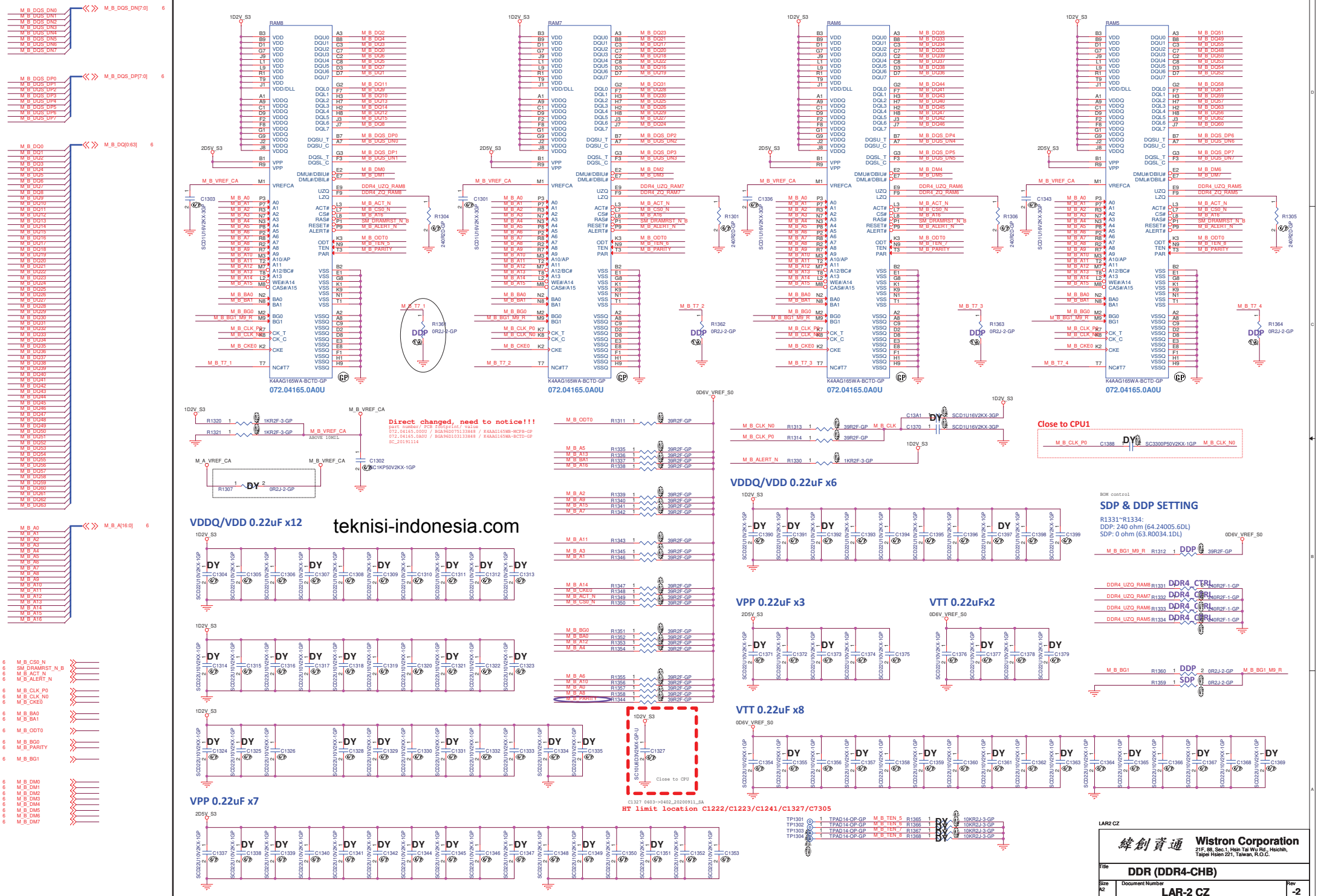

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Title	DDR (DDR4-CHB)
Size	A2
Document Number	LAR-2 CZ
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Date	Wednesday, July 28, 2021
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LAR2 CZ

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Title
DDR (RSVD)

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

Date: Wednesday, July 28, 2021 Sheet 14 of 106

(Blanking)

LAR2 CZ

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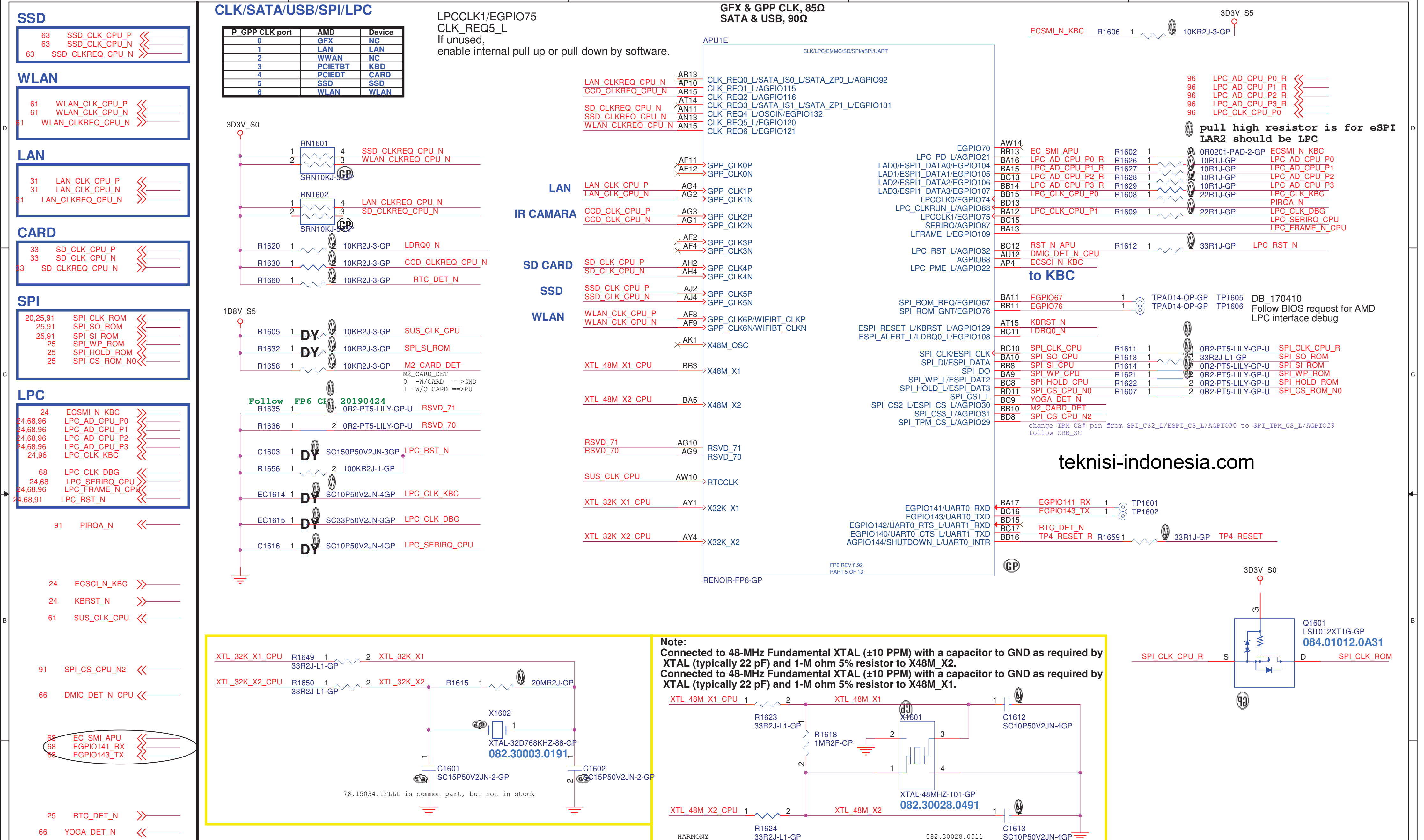
Title: ***FCH (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

Date: Wednesday, July 28, 2021 Sheet 15 of 106



P_GPP CLK port	AMD	Device
0	GFX	NC
1	LAN	LAN
2	WWAN	NC
3	PCIETBT	KBD
4	PCIEDT	CARD
5	SSD	SSD
6	WLAN	WLAN

Note:
Connected to 48-MHz Fundamental XTAL (±10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X2.
Connected to 48-MHz Fundamental XTAL (±10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X1.

X1602	C1601	C1602	4ZA P/N
SEIKO 082.30003.0301	15pF	15pF	4ZA.0M501.0001
EPSON 082.30003.0191	15pF	15pF FVT	4ZA.0M501.0002
NDK 082.30003.0221	15pF	15pF FVT	4ZA.0M501.0003
TXC 082.30003.0231	15pF	15pF FVT	4ZA.0M501.0004
TAITIEN 082.30003.0A11	12pF	12pF	4ZA.0M501.0005

X1601	C1612	C1613	ppm
HARMONY 82.30026.371	10pF	10pF	20ppm
HOSONIC 082.30028.0091			20ppm
HOSONIC 082.30028.0491			10ppm

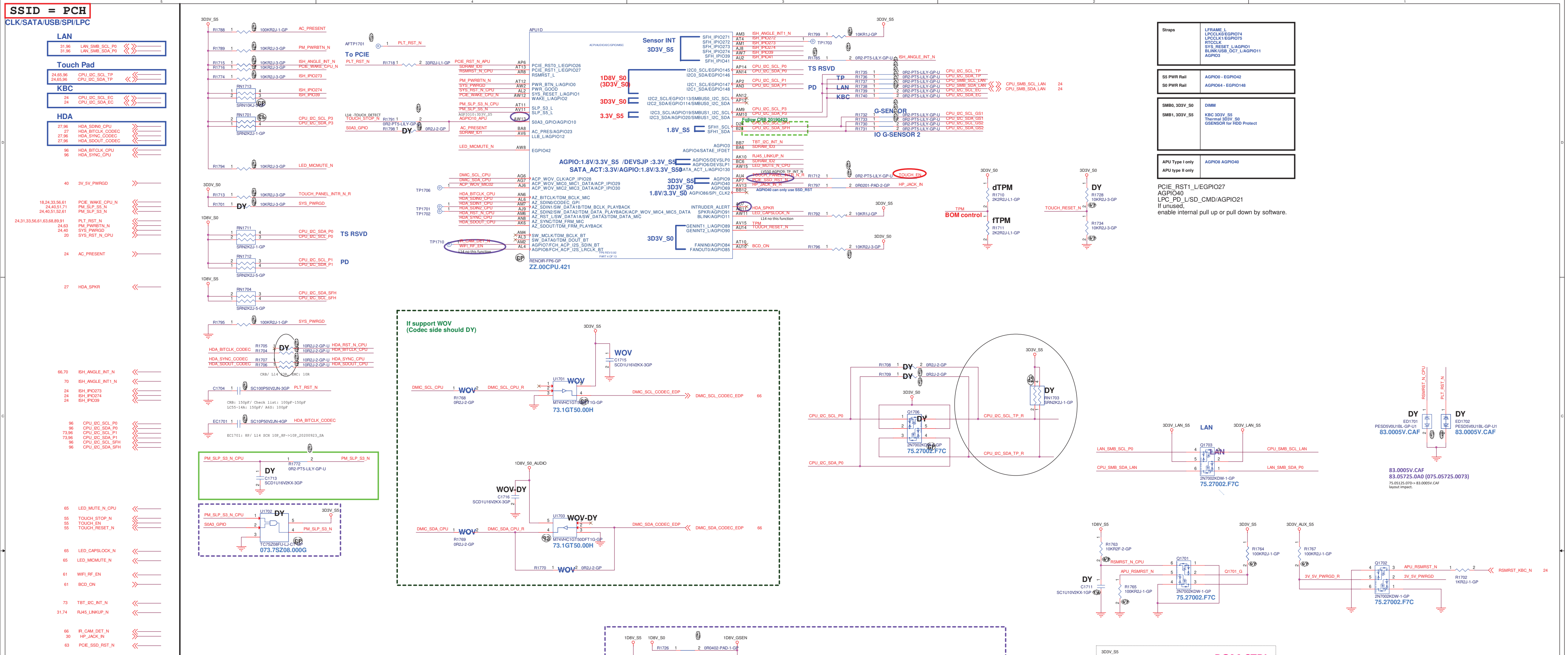
LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (CLK/LPC/SPI/EMMC/SD/UA)

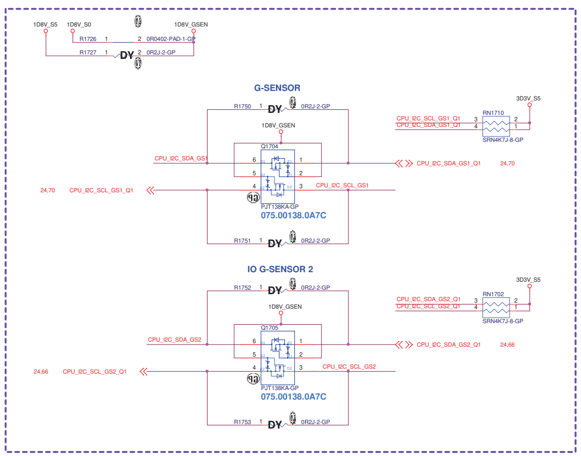
Size: A3 | Document Number: LAR-2 CZ | Rev: -2

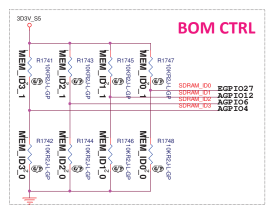
Date: Wednesday, July 28, 2021 | Sheet 16 of 106



INTERNAL DEBUG PURPOSE ONLY

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled





EVT/FVT/SIT/SVT:

Memory Configuration

00: (Reserve)
01: 8GB
10: 16GB
11: 16GB DDP

Memory Supplier

00: Samsung
01: Micron
10: SK Hynix
11: (Reserve)

072.04165.0A0U 13.3*10.3

AGPIO4 SDRAM_ID3	AGPIO6 SDRAM_ID2	AGPIO12 SDRAM_ID1	EGPIO27 SDRAM_ID0	Memory ID	Supplier	Density	PN	DDR4		
0	0	0	0	0	SAMSUNG	4GB	SM30N76632	SDPx16 8Gb	3200	
0	1	0	0	4	SAMSUNG	8GB	SM30N76632AA			
1	0	0	0	8	SAMSUNG	16GB	~~SM30N76568~~	~~SDP~~ SM30N76633AA		13.3*10.3
1	1	0	0	12	~~SAMSUNG~~	~~16GB~~	~~SM30N76569AA~~	~~DDP~~		13.3*10.3
0	0	0	1	1	MICRON	16GB	SM30N76604AA	SDPx16 8Gb	3200	
0	1	0	1	5	MICRON	8GB	SM30N76570AA			
1	0	0	1	9	MICRON	16GB	SM30N76641AA			
1	1	0	1	13	MICRON	8GB	SM30N76836AA			
0	0	1	0	2	SK HYNIX	4GB	SM30N76639	SDPx16 8Gb	3200	
0	1	1	0	6	SK HYNIX	8GB	SM30N76625AA	~~SM30N76639AA~~		
1	0	1	0	10	SK HYNIX	16GB	SM30N76775AA	~~SM30N76640AA DDP~~		
1	0	1	0	14	SK HYNIX					

0=L, 1=H

LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (AZ/I2C/GPIO/RTC/SMBS/M)

Size: A1 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 17 of 106

Main Func = USB

USB3.0 Port3
36 USB3_USB31_RX_N
36 USB3_USB31_RX_P
36 USB3_USB31_TX_N
36 USB3_USB31_TX_P
35 USB3_USB20_N
35 USB3_USB20_P

USB3.0 Port4
36 USB4_USB31_RX_N
36 USB4_USB31_RX_P
36 USB4_USB31_TX_N
36 USB4_USB31_TX_P
36 USB4_USB20_N
36 USB4_USB20_P

BT
61 BT_USB20_N
61 BT_USB20_P

IR Camera
56 CCD_USB20_N
56 CCD_USB20_P

Type-C USB20
74 USB1_USB20_N
74 USB1_USB20_P

Type-C DK1
71 USB1_TCSS_TX_P0
71 USB1_TCSS_TX_N0
71 USB1_TCSS_RX_P0
71 USB1_TCSS_RX_N0
71 USB1_TCSS_TX_P1
71 USB1_TCSS_TX_N1
71 USB1_TCSS_RX_P1
71 USB1_TCSS_RX_N1

Type-C 2 USB20
75 USB2_USB20_N
75 USB2_USB20_P

Type-C 2
75 USB2_TCSS_TX_P0
75 USB2_TCSS_TX_N0
75 USB2_TCSS_RX_P0
75 USB2_TCSS_RX_N0
75 USB2_TCSS_TX_P1
75 USB2_TCSS_TX_N1
75 USB2_TCSS_RX_P1
75 USB2_TCSS_RX_N1

38,73 USB_OC1_N
38,73 USB_OC0_N
24,31 LAN_WAKE_N
17,24,33,56,61 PCIE_WAKE_CPU_N

73 CPU_I2C_SCL_PD
73 CPU_I2C_SDA_PD

HUB(World Facing Camera,SCR,TS)
38 HUB_USB20_P
38 HUB_USB20_N

FP
92 FP_USB20_P
92 FP_USB20_N

9 USBC_I2C_SWITCH
65 PAD_DISABLE
65 PAD_RESET_N

APU1J

DK1 USB2.0 Port1: USB1_USB20_P AC6 / USB1_USB20_N AC7
USB2.0 Port3: USB3_USB20_P AA8 / USB3_USB20_N AA9
Camera (RGB & IR Camera): CCD_USB20_P Y10 / CCD_USB20_N Y9
FP: FP_USB20_P Y7 / FP_USB20_N Y6
Type-C 2 port2: USB2_USB20_P AC9 / USB2_USB20_N AC10
USB2.0 Port4: USB4_USB20_P AA11 / USB4_USB20_N AA12
BT: BT_USB20_P W8 / BT_USB20_N W9
HUB(World Facing Camera,SCR,TS): HUB_USB20_P W11 / HUB_USB20_N W12
World Facing Camera (Yoga only)

CPU_I2C_SCL_TYPEC AL9
CPU_I2C_SDA_TYPEC AL8

USB_OC0_N AE9 AOU
USB_OC1_N AE10 NON_AOU
PAD_DISABLE AE6
PAD_RESET_N AE7

USB
USBC0_DP/USB0_DP
USBC0_DN/USB0_DN
USB1_DP
USB1_DN
USB2_DP
USB2_DN
USB3_DP
USB3_DN
USBC4_DP/USB4_DP
USBC4_DN/USB4_DN
USB5_DP
USB5_DN
USB6_DP
USB6_DN
USB7_DP
USB7_DN
USBC_I2C_SCL
USBC_I2C_SDA
USB_OC0_L/AGPIO16
USB_OC1_L/AGPIO17
USB_OC2_L/AGPIO18
USB_OC3_L/AGPIO24

USBC0_TX1P/USB0_TXP/DP2_TXP2 AA1 USB1_TCSS_TX_P0
USBC0_TX1N/USB0_TXN/DP2_TXN2 AA3 USB1_TCSS_TX_N0
USBC0_RX1P/USB0_RXP/DP2_TXP3 AA2 USB1_TCSS_RX_P0
USBC0_RX1N/USB0_RXN/DP2_TXN3 AA4 USB1_TCSS_RX_N0
USBC0_TX2P/DP2_TXP1 AC2 USB1_TCSS_TX_P1
USBC0_TX2N/DP2_TXN1 AC4 USB1_TCSS_TX_N1
USBC0_RX2P/DP2_TXP0 AC1 USB1_TCSS_RX_P1
USBC0_RX2N/DP2_TXN0 AC3 USB1_TCSS_RX_N1
USB1_TXP AE1 USB3_USB31_TX_P
USB1_TXN AE3 USB3_USB31_TX_N
USB1_RXP AD8 USB3_USB31_RX_P
USB1_RXN AD9 USB3_USB31_RX_N
USBC4_TX1P/USB4_TXP/DP3_TXP2 V3 USB2_TCSS_TX_P0
USBC4_TX1N/USB4_TXN/DP3_TXN2 V1 USB2_TCSS_TX_N0
USBC4_RX1P/USB4_RXP/DP3_TXP3 U4 USB2_TCSS_RX_P0
USBC4_RX1N/USB4_RXN/DP3_TXN3 U2 USB2_TCSS_RX_N0
USBC4_TX2P/DP3_TXP1 W2 USB2_TCSS_TX_P1
USBC4_TX2N/DP3_TXN1 W4 USB2_TCSS_TX_N1
USBC4_RX2P/DP3_TXP0 W1 USB2_TCSS_RX_P1
USBC4_RX2N/DP3_TXN0 W3 USB2_TCSS_RX_N1
USB5_TXP AD2 USB4_USB31_TX_P
USB5_TXN AD4 USB4_USB31_TX_N
USB5_RXP AD12 USB4_USB31_RX_P
USB5_RXN AD11 USB4_USB31_RX_N

FP6 REV 0.92
PART 10 OF 13

RENOIR-FP6-GP
ZZ.00CPU.421

Type C USB3.1 Gen2 + USB2.0 + DP → DK1 USB2.0 Port1
USB3.0 Port3
Type C USB3.1 Gen1 + USB2.0 + DP → Type-C 2 port2
USB3.0 Port4

1.8V_S5

3D3V_S5
R1805 1 DY 2 10KR2J-3-GP PAD_RESET_N
R1806 1 DY 2 10KR2J-3-GP PAD_DISABLE
RN1802 1 4 SRN10KJ-5-GP USB_OC1_N
2 3 USB_OC0_N

LAN_WAKE_N R1801 1 DY 2 0R2J-2-GP PAD_RESET_N
AMD CRB
PCIE_WAKE_CPU_N R1802 1 DY 2 0R2J-2-GP PAD_DISABLE

AGPIO13/USB_OC5_L
If unused,
enable internal pull up or pull down by software.

PAD_DISABLE
R1807 100KR2J-1-GP

1D8V_S5
USBC_I2C_SWITCH
R1803 0R0402-PAD-1-GP
R1804 0R2J-2-GP DY
C1801 SCD1U16V2KX-3GP
1D8V_S5_PD
Q1801
CPU_I2C_SCL_PD → CPU_I2C_SCL_TYPEC
CPU_I2C_SDA_PD → CPU_I2C_SDA_TYPEC
PJT138KA-GP
075.00138.0A7C

1D8V_S5
RN1803
CPU_I2C_SCL_TYPEC
CPU_I2C_SDA_TYPEC
SRN4K7J-8-GP

96 CPU_I2C_SCL_TYPEC
96 CPU_I2C_SDA_TYPEC

LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (USB/Camera/RSVD)
Size: A3 | Document Number: LAR-2 CZ | Rev: -2
Date: Wednesday, July 28, 2021 | Sheet 18 of 106

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LAR2 CZ

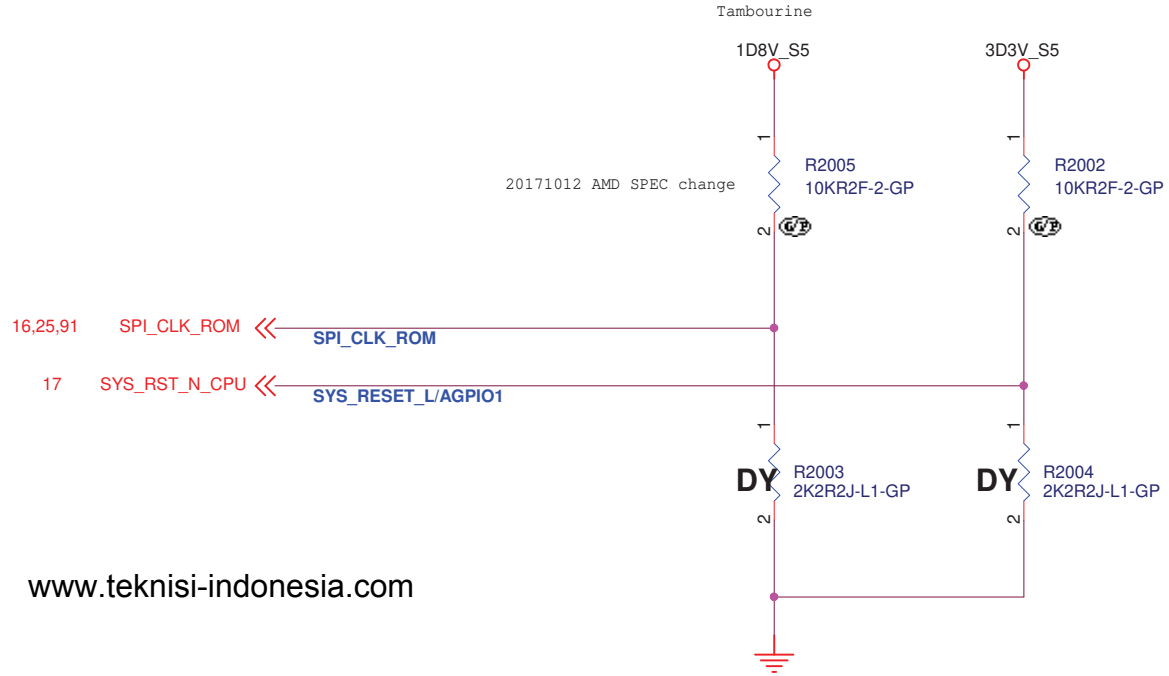
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***FCH (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

Date: Wednesday, July 28, 2021 Sheet 19 of 106

STRAP PINS



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10KΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***FCH (Strap)***

Size	Document Number	Rev
A4	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 20 of 106

(Blanking)

LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
FCH (RSVD)

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

Date: Wednesday, July 28, 2021 Sheet 21 of 106

(Blanking)

LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (RSVD)*

Size	Document Number	Rev
A4	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 22 of 106

(Blanking)

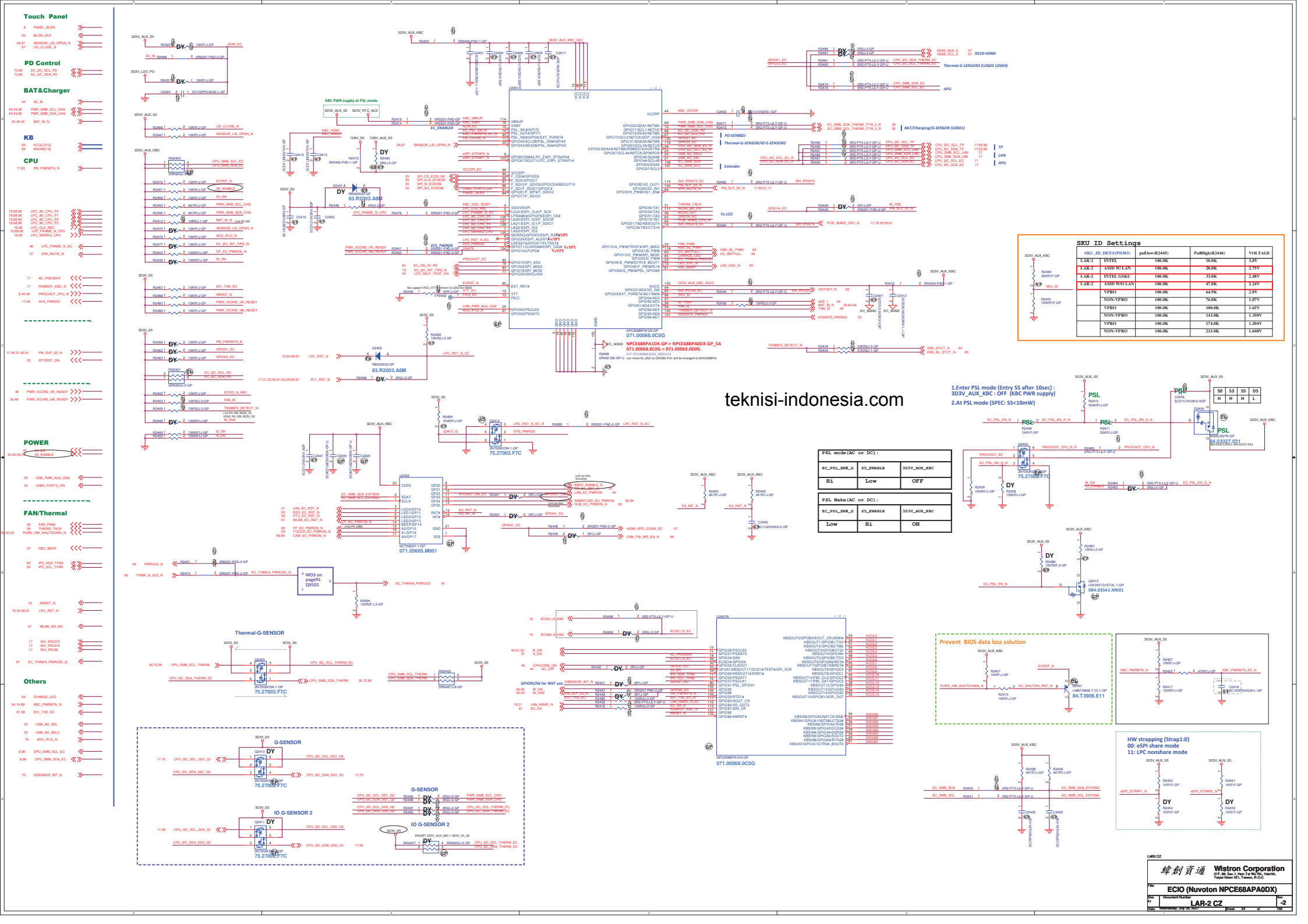
LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

Date: Wednesday, July 28, 2021 Sheet 23 of 106


Touch Panel
PANEL_BLEN
BLON_OUT
SENSOR_LID_OPEN_N
LID_CLOSE_N
PD Control
EC_SCI_SCL_PD
EC_SCI_SDA_PD
BAT&Charger
AC_IN
PWR_SMB_SCL_CHG
PWR_SMB_SDA_CHG
BAT_IN_N
KB
KCOL[15:0]
KROW[7:0]
CPU
PM_PWRBTN_N
LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
LPC_CLK_KBC
LPC_FRAME_N_CPU
LPC_SERIRQ_CPU
LPC_FRAME_N_EC
SPK_MUTE_N
AC_PRESENT
RSMRST_KBC_N
PROCHOT_CPU_N
SYS_PWRGD
PWR_VCORE_VR_READY
PWR_VCORE_NB_READY
POWER
SS_ENABLE
USB_PWR_ACIU_EN2
USB3_PORT2_ON
FAN/Thermal
FAN_PWM
THERM_TACH
PURE_HW_SHUTDOWN_N
KBC_BEEP
IPD_SDA_TPAD
IPD_SCL_TPAD
KBRST_N
LPC_RST_N
WLAN_MS_EN
ISH_IPIO273
ISH_IPIO274
ISH_IPIO39
EC_THINKA_PWRLED_O
Others
CHARGE_LED
KBC_PWRBTN_N
ES1_TXD_EC
USB_AO_SEL
USB_AO_SEL2
ACIU_PLG_N
CPU_SMB_SCL_EC
CPU_SMB_SDA_EC
GSENSOR_INT_N
3D3V_AUX_S5
3D3V_AUX_KBC
3D3V_S0
3D3V_LDO_PD
3D3V_RTC_AUX
KBC PWR supply at PSL mode.
U2401A
NPCE688PA1DX-GP
071.00068.0C0G
NPCE688PA1DX-GP-> NPCE688PA0DX-GP_SA
071.00068.0C0G-> 071.00068.0D0G
teknisi-indonesia.com
SKU ID Settings
SKU_ID_DET(GPIO83)
pull low(R2445)
PullHigh(R2446)
VOLTAGE
LAR-2 INTEL 100.0K 10.0K 3.0V
LAR-2 AMD W/LAN 100.0K 20.0K 2.75V
LAR-2 INTEL GSKU 100.0K 33.0K 2.48V
LAR-2 AMD W/O LAN 100.0K 47.0K 2.24V
VPRO 100.0K 64.9K 2.0V
NON-VPRO 100.0K 76.8K 1.87V
VPRO 100.0K 100.0K 1.65V
NON-VPRO 100.0K 143.0K 1.358V
VPRO 100.0K 174.0K 1.204V
NON-VPRO 100.0K 215.0K 1.048V
1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)
PSL mode(AC or DC) :
EC_PSL_EN#_G SS_ENABLE 3D3V_AUX_KBC
Hi Low OFF
PSL Wake(AC or DC) :
EC_PSL_EN#_G SS_ENABLE 3D3V_AUX_KBC
Low Hi ON
Prevent BIOS data loss solution
HW strapping (Strap1:0)
00: eSPI share mode
11: LPC nonshare mode
Thermal-G-SENSOR
G-SENSOR
IO G-SENSOR 2
Wistron Corporation
ECIO (Nuvoton NPCE68APA0DX)
LAR-2 CZ
-2

Main Func = SPI Flash

SPI FLASH ROM1(32MByte)for BIOS

24 SPI_CLK_ECROM
24 SPI_SI_ECROM
24 SPI_CS_ECIO_N0
24 SPI_SO_ECROM

1D8V_VCCSPI
R25471 10KR2J-3-GP SPI_SO_ROM_R
R25481 10KR2J-3-GP SPI_CS_ROM_N0_R
R25491 10KR2J-3-GP SPI_WP_ROM_R
R25501 10KR2J-3-GP SPI_HOLD_ROM_R

1D8V_VCCSPI
C2516 SC22U6D3V3MX-1-GP
C2517 SCD1U16V2KX-3GP

1D8V_S5
R2516 0R0402-PAD-1-GP

TABLE BIOS1
32MB WSON 8

Vender	Vender P/N	Wistron P/N	
WINBOND	W74M25JWZEIQ	072.07425.0001	RPMC
MACRONIX	MX77U25650FZ4I42	072.77256.0A01	RPMC

SPI_CS_ROM_N0 R2552 10R2F-L-GP SPI_CS_ROM_N0_R
SPI_SO_ROM R2553 0R2-PT5-LILY-GP-U SPI_SO_ROM_R
SPI_WP_ROM R2554 0R2-PT5-LILY-GP-U SPI_WP_ROM_R
SPI_CS_ECIO_N0 R2517 0R2-PT5-LILY-GP-U
SPI_SO_ECROM R2518 0R2-PT5-LILY-GP-U

BIOS1 **32MByte**
S# DQ1 W#/VPP VSS GND VCC HOLD# C DQ0
LILY-BIOS-COLAY-GP-U
ZZ.00PAD.M41
Co-lay symbol: ZZ.00PAD.M41

SPI_HOLD_ROM_R
SPI_CLK_ROM_R
SPI_SI_ROM_R

R2506 0R2-PT5-LILY-GP-U SPI_HOLD_ROM 16
R2502 33R2J-L1-GP SPI_CLK_ROM 16,20,91
R2503 0R2-PT5-LILY-GP-U SPI_SI_ROM 16,91
R2519 0R2-PT5-LILY-GP-U SPI_CLK_ECROM
R2520 0R2-PT5-LILY-GP-U SPI_SI_ECROM

VCC接1.8V
Need BOM control to 072.07425.0001
EVT: DIP
FVT: SMT

For ECRST# issue
U2502 JUST EVT ASM
RSVD

1D8V_AUX_S5 R2546 DY 0R2J-2-GP 1D8V_VCCSPI
15
16,91
15

3D3V_AUX_KBC R2543 DY 0R2J-2-GP
3D3V_AUX_S5 R2544 DY 0R2J-2-GP
3D3V_LDO_VIN
3D3V_EN
U2502 DY
VIN GND EN VOUT SNS/NC#4
3D3V_VOUT
RT9078-18GJ5-GP
074.09078.003F
C2514 DY SC1U10V2KX-1GP

1D8V_AUX_S5 R2545 DY 0R2J-2-GP
C2515 DY SC1U10V2KX-1GP

Main Func = RTC

24 RTCRST_ON
16 RTC_DET_N

3D3V_AUX_S5
3D3V_RTC_AUX
D2502 LBAT54CLT1G-1-GP **075.00054.0B7D**
C2505 SCD47U25V3KX-1-GP-U

RTC CONN
3D3V_RTC_VCC
RTC1 ACES-CON2-20-GP-U **20.F1639.002**
R2507 1KR2J-1-GP
3D3V_RTC_Q
RTC_DET_N
Q2505 PJA7002H-R1-00001-2-GP **084.07002.M010**
R2509 10MR2J-L-GP

Near RTC CONN (RTC1)
3D3V_RTC_VCC
AFTP2501 AFTE14P-GP
AFTP2503 AFTE14P-GP
AFTP2502 AFTE14P-GP

3D3V_RTC_AUX
084.03415.0031->84.03327.031
Q2501 SSM3J327R-GP **84.03327.031**
RTC_AUX_Q
R2511 1KR2F-L1-GP
3D3V_RTC_AUX_Q
C2511 SC1U10V2KX-1GP
C2512 SC1U10V2KX-1GP
C2513 SC1U10V2KX-1GP
G2501 GAP-OPEN
R2512 DY 0R2J-2-GP
RTCRST_ON
Q2511 PJE8408-R1-00001-GP **084.08408.0031**
Q2511_S
R2513 100R2J-L-GP
R2515 10KR2F-2-GP

LAR2 CZ

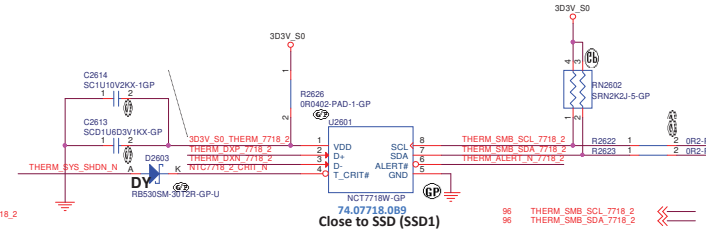
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

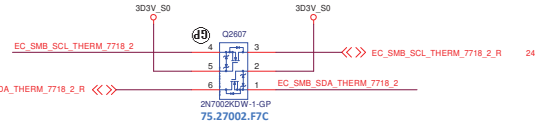
Title **FLASH/RTC**
Size A3 | Document Number **LAR-2 CZ** | Rev **-2**
Date: Wednesday, July 28, 2021 | Sheet 25 of 106

Main Func = Thermal Sensor

Thermal Sensor

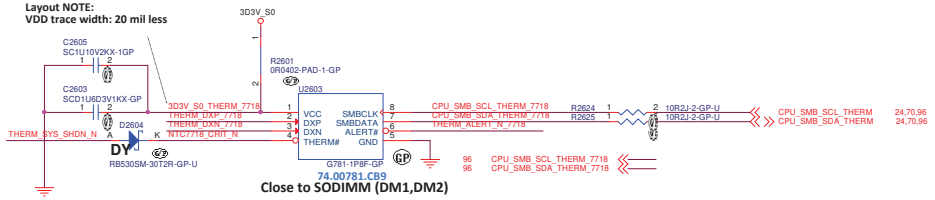
Sensor	Target
U2601	SSD
U2603	DIMM
Q2601	CPU
Q2602	Charger

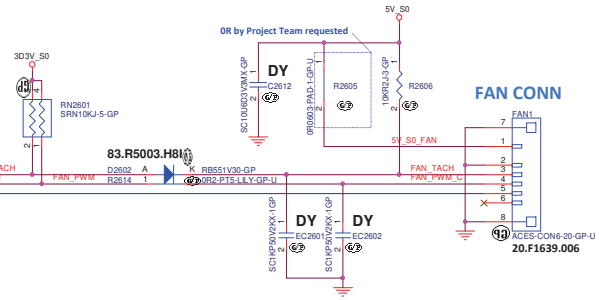


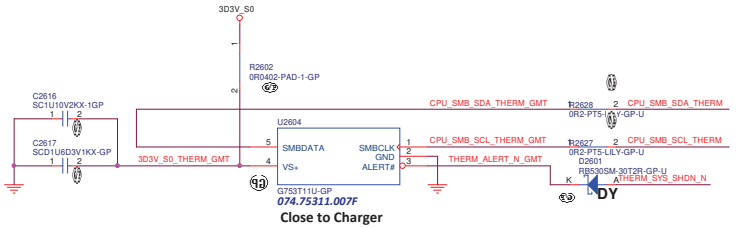


FAN Controller

NCT7718W 's maximum power consumption can be xxx mA (TBD)







CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

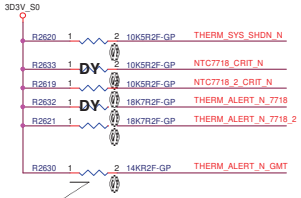
ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

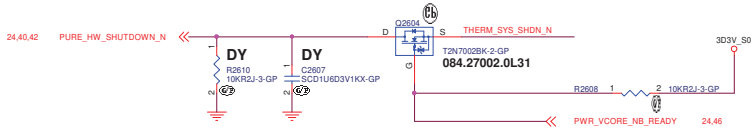
NCT7717U Table:

R2630	
2.0K	75
7.5K	90
10.5K	100
14.0K	105
18.7K	110

NCT7718W Table:

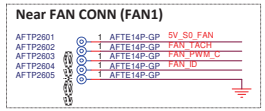
R2619 / R2621 (R1633) (R1632)	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125





PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



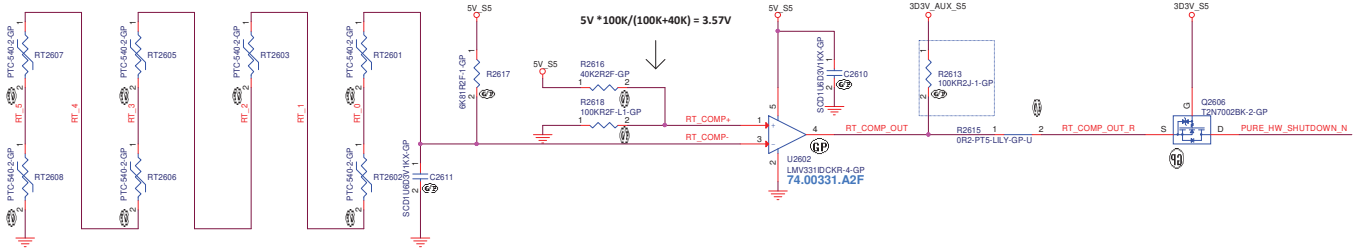
ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2kΩ	75
	7.5kΩ	90
	10.5kΩ	100
	14kΩ	105
	18.7kΩ	110

TABLET

ID	Target	Function
RT2601		
RT2602		
RT2603		
RT2605		
RT2606		
RT2607		
RT2608		



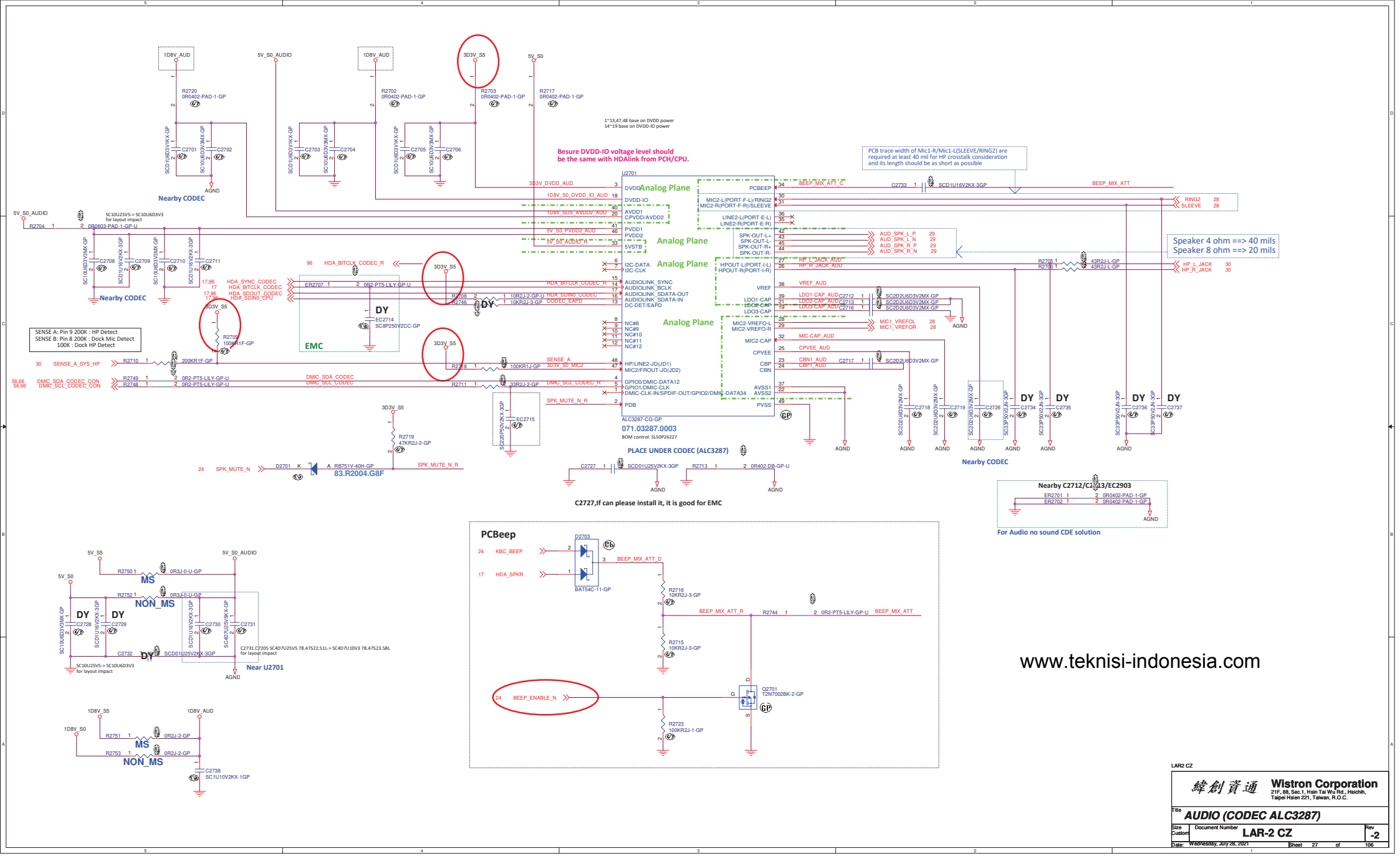
LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

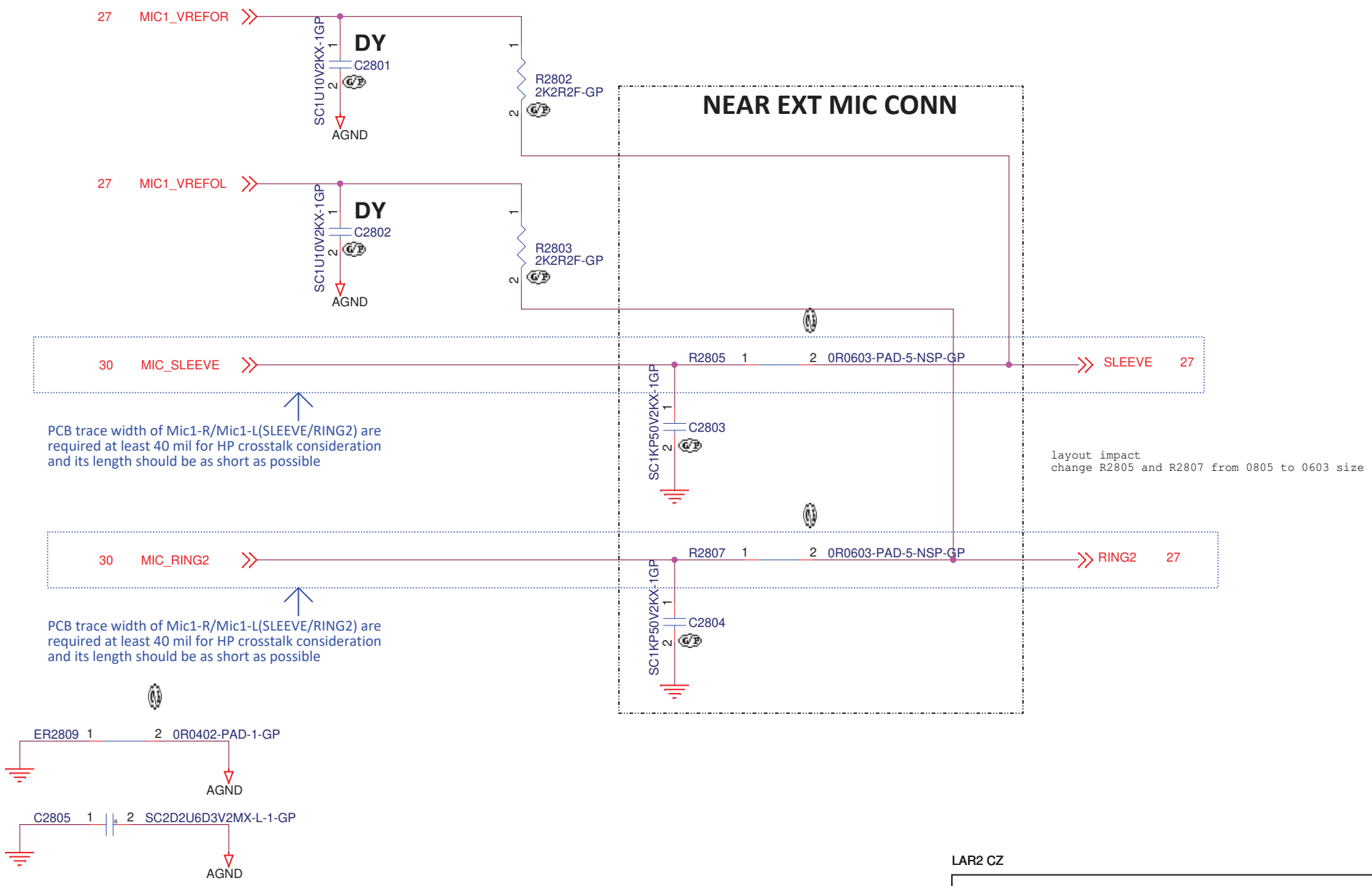
Title: INT IO (THERMAL/FAN)

Size	Document Number	Rev
A2	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 26 of 106



LAR2 CZ	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO (CODEC ALC3287)
Size: Custom	Document Number: LAR-2 CZ
Rev	-2
Date: Wednesday, July 28, 2021	Sheet 27 of 106



LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

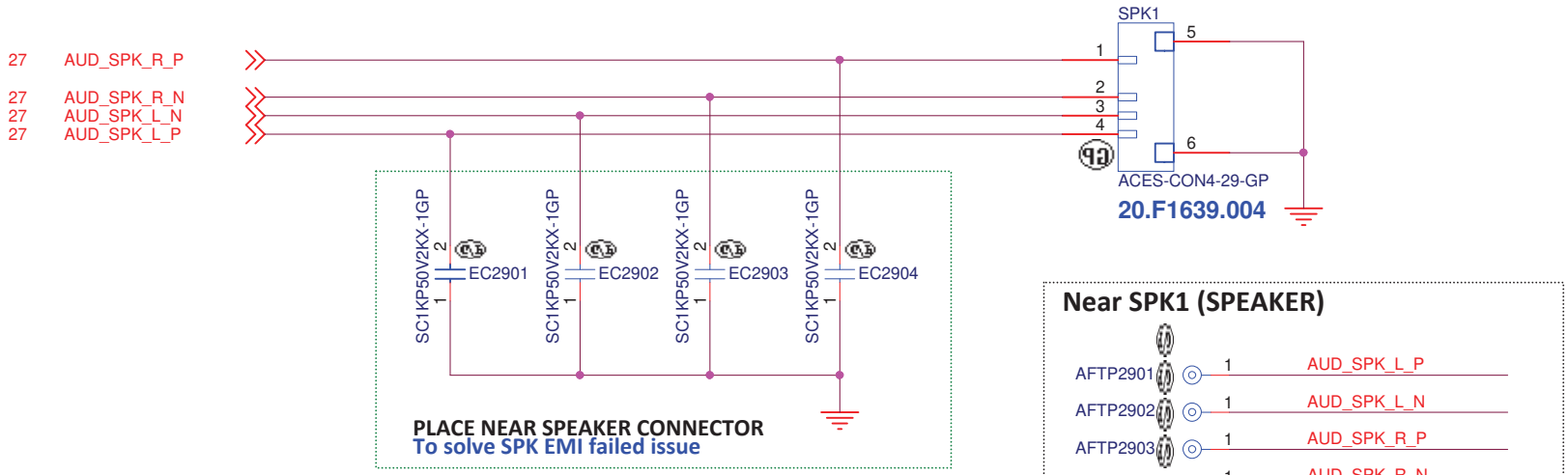
Title: ***AUDIO (MIC I/F)***

Size	Document Number	Rev
A4	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 28 of 106

Main Func = AUDIO

SPEAKER CONN



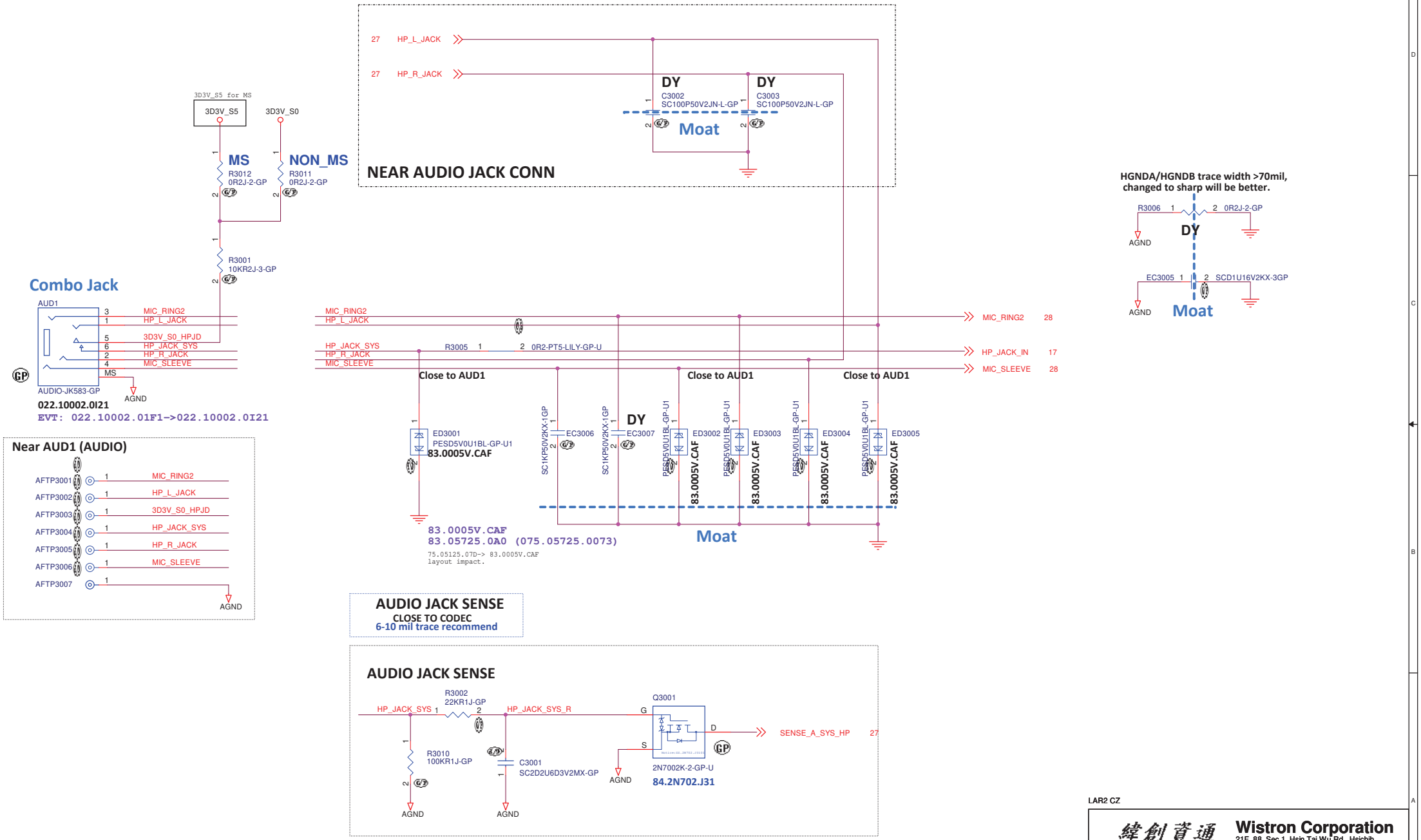
LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (SPEAKER)***

Size	Document Number	Rev
A4	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 29 of 106



LAR2 CZ

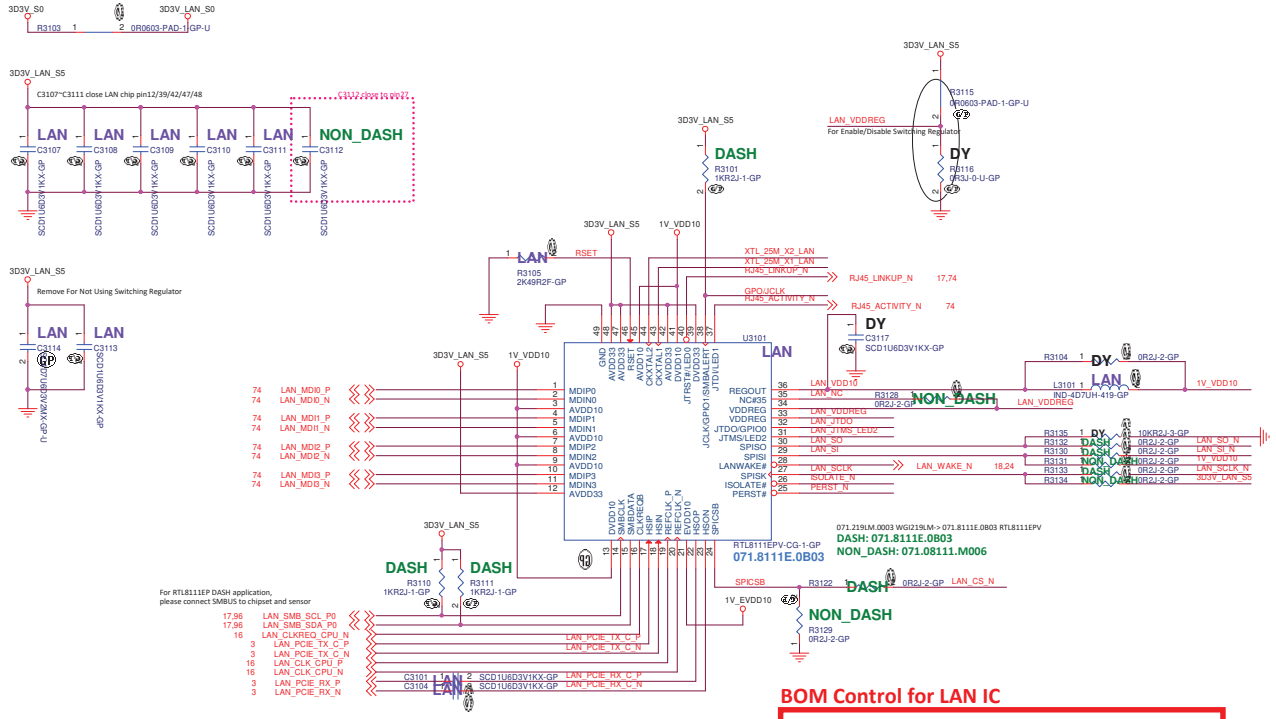
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (AUDIO JACK)***

Size	Document Number	Rev
A3	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 30 of 106

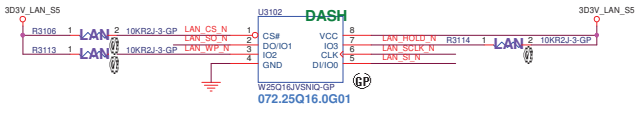
Main Func = LAN

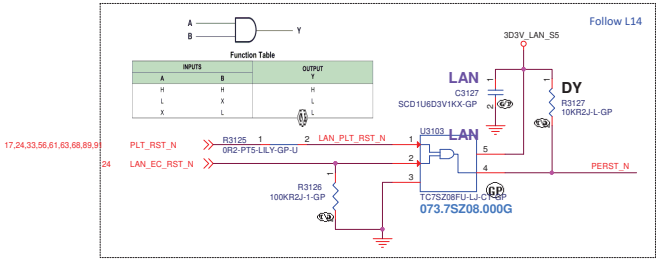


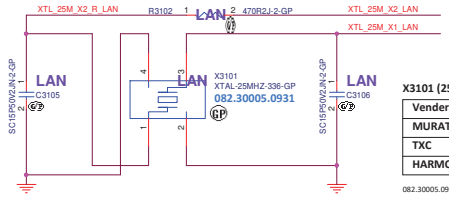
BOM Control for LAN IC

Table of LAN IC Option

	Del "DUMMY" Property for BOM	SKU ID Settings (Page24)
W/ LAN DASH	NON_DASH — LAN IC P/N : 071.8111E.0B03 REALTEK / RTL8111EPV	LAR-2 AMD W/ LAN
W/ LAN NON_DASH	DASH — LAN IC P/N : 071.08111.M006 REALTEK / RTL8113HN	LAR-2 AMD W/ LAN
W/O LAN	LAN,DASH, NON-DASH	LAR-2 AMD W/O LAN



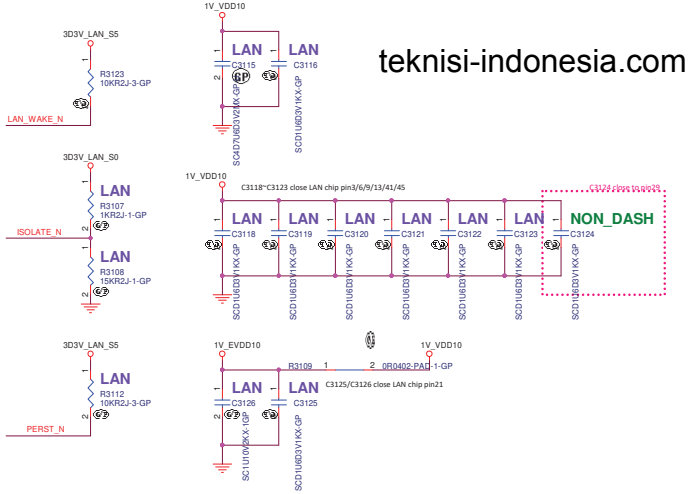


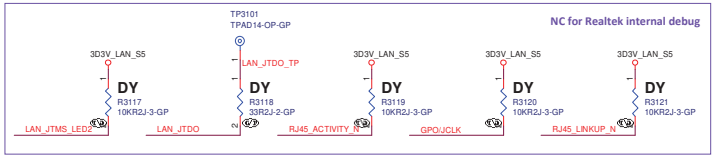


X3101 (25MHz)

Vender	Vender PN	Wistron PN
MURATA	XRCGB25M000F2P40R0	082.30005.0911
TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81

082.30005.0931 BOM control to 082.30005.0911 (COMMON PART)





LAR2 CZ

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RTL8111EPV)

Size: A2 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 31 of 106

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LAR2 CZ

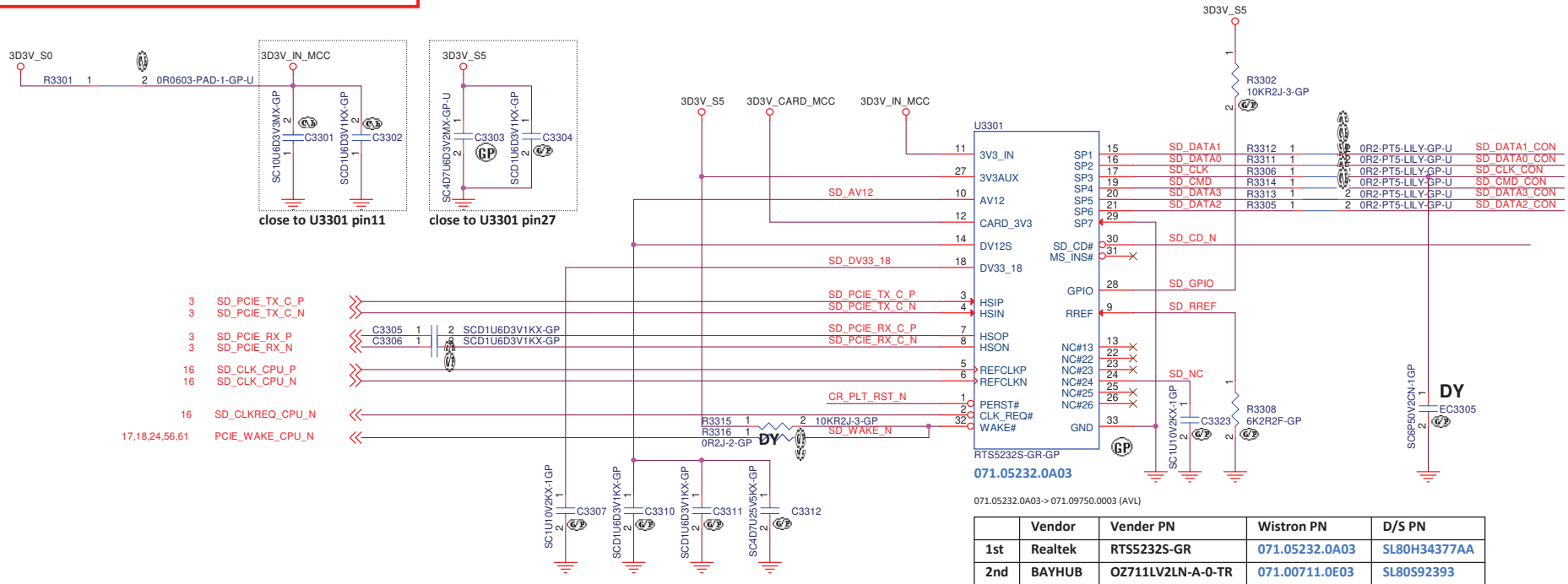
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***LAN (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

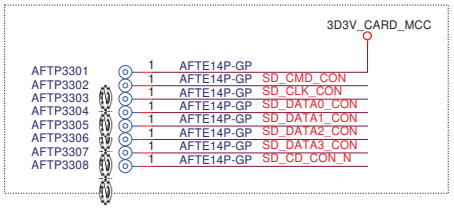
Date: Wednesday, July 28, 2021 Sheet 32 of 106

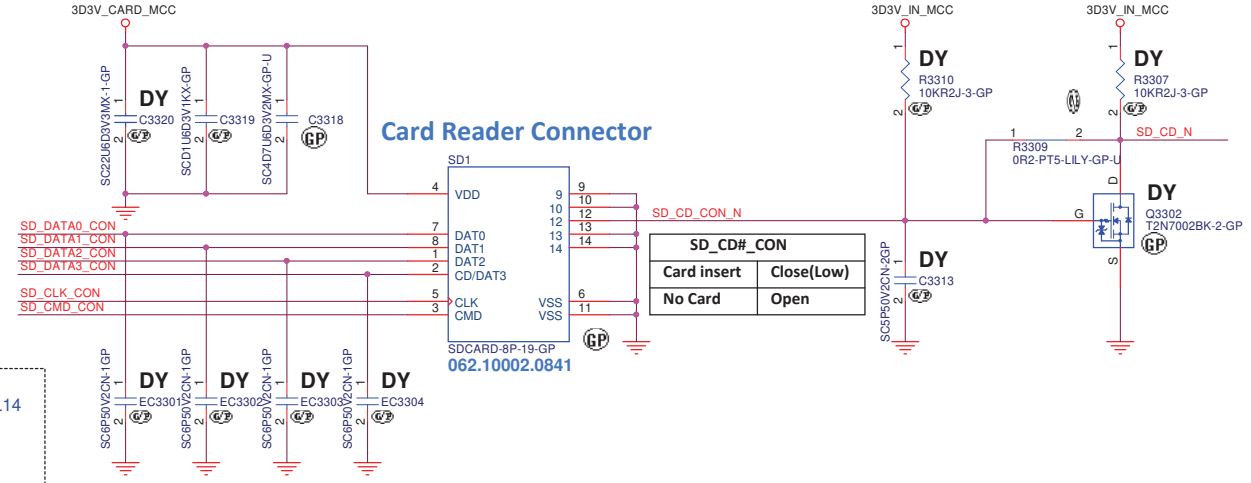
Main Func = Card Reader

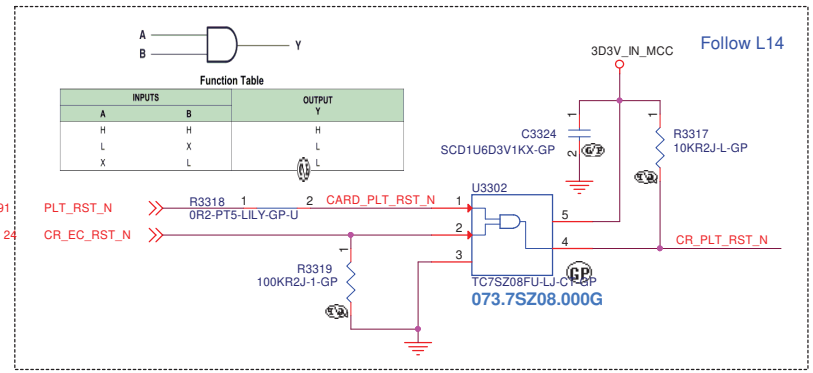


	Vendor	Vender PN	Wistron PN	D/S PN
1st	Realtek	RTS5232S-GR	071.05232.0A03	SL80H34377AA
2nd	BAYHUB	OZ711LV2LN-A-0-TR	071.00711.0E03	SL80S92393
~~2nd~~	~~GENESYS~~	~~GL9750-QIYL3~~	~~071.09750.0003~~	

These test pins trace should be short and close to connector







LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD READER (SDIO/CONN)**

Size	Document Number	Rev
A3	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 33 of 106

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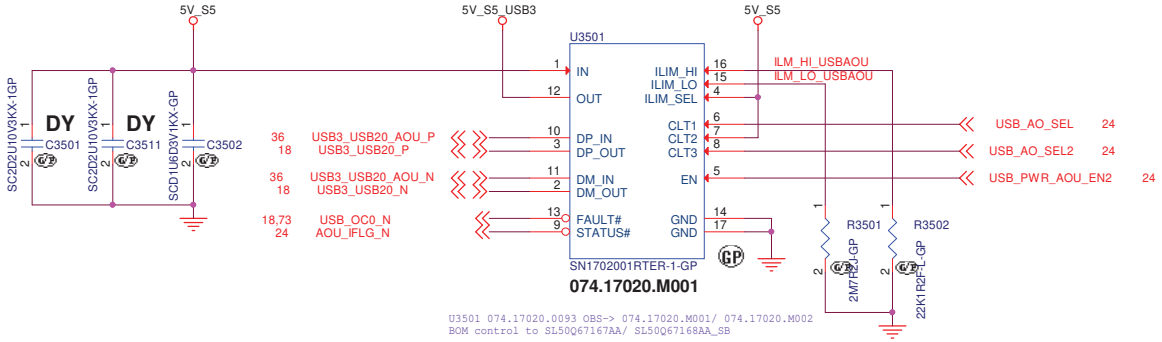
LAR2 CZ

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB (RSVD)***
Size A4	Document Number **LAR-2 CZ**
Rev **-2**	
Date:	Wednesday, July 28, 2021
Sheet	34 of 106

Main Func = USB Charger

For USB3.0 System Port3 (For AOU)



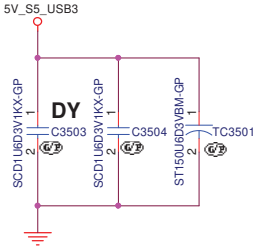
SN1702001RTER is not equivalent device of TPS2546RTER

Current Limit Target : 2.3A (2.1-2.45A)

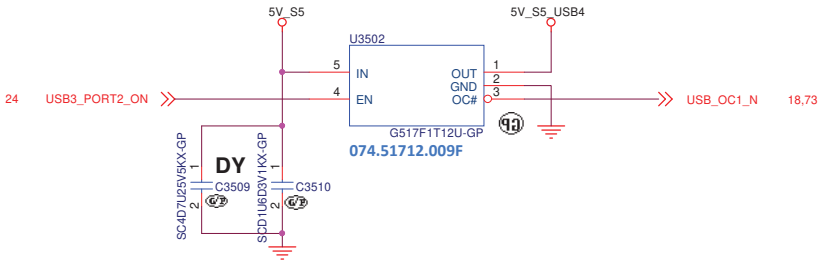
TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N	
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093	SL50Q67167AA
2nd	Pericom	PI5USB2546HZHEX	074.52546.0D73	SL50Q67168AA

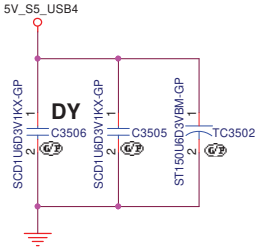
Layout Note: Close USB3.0 Port3



For USB3.0 System Port4



Layout Note: Close USB3.0 Port4



Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N	
1st	GMT	G517F1T12U	074.51712.009F	074.09742.0A9F
2nd	SILERGY	SY6288C20AAC	074.06288.007B	074.51712.009F
				074.06288.007B

Please confirm VIH voltage level of G517F1T12U EN pin, DP_DIGON is 1.8V level.

LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

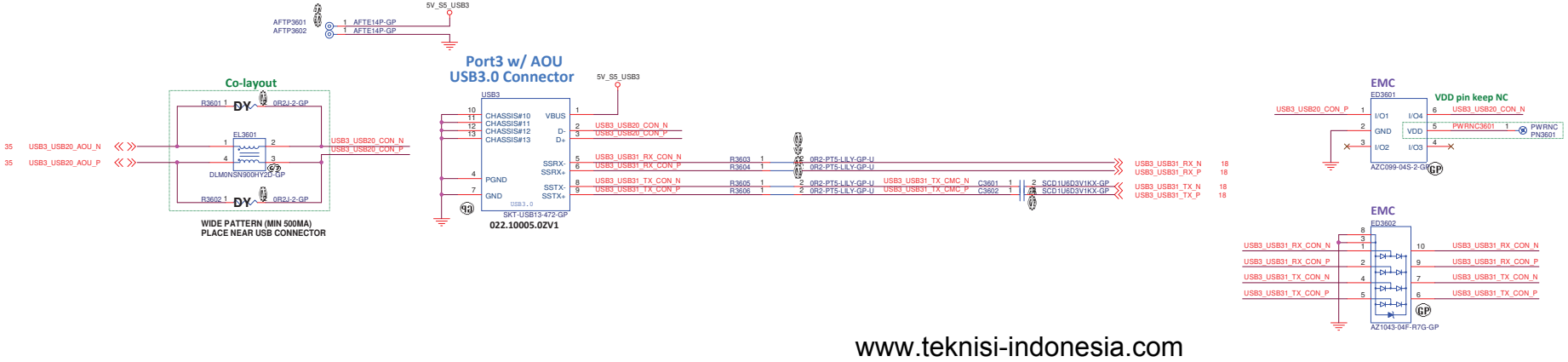
Title: USB (CHARGER/SWITCH)

Size: A3 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 35 of 106

Main Func = USB3.0 Port3 w/ AOU

Main Func = USB3.0 Port4



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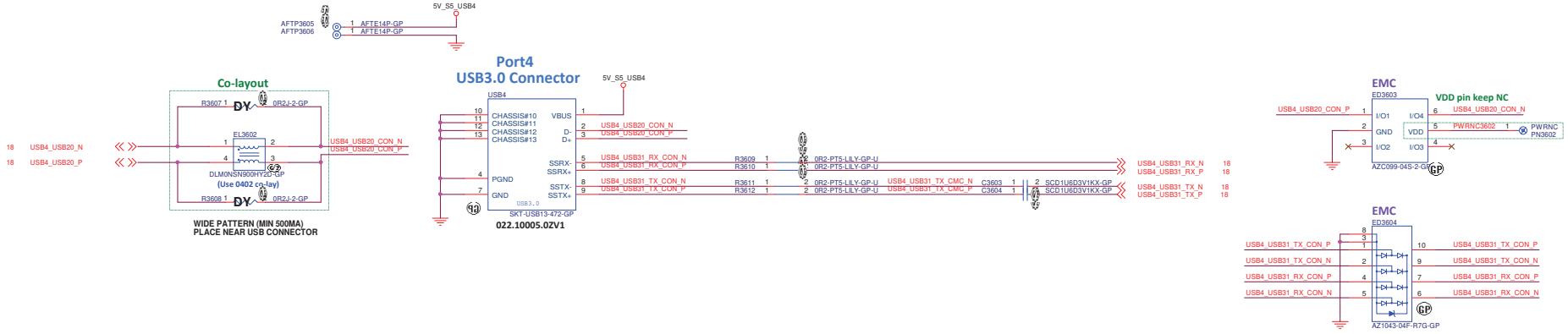

LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB3.0 CONN)

Size: A2 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 36 of 106

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LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

Date: Wednesday, July 28, 2021 Sheet 37 of 106

USB2 HUB

Power

3D3V_S0 — R3821 1 DY D01RL0816F-1-GP — 3D3V_HUB_VDD

3D3V_S5 — R3801 1 DY D01RL0816F-1-GP — 3D3V_HUB_VDD

C3801 SCD1U16V2KX-3GP

Close to pin 28

HUB

USB2.0 | 18 HUB_USB20_P | 18 HUB_USB20_N

World Facing Camera

USB2.0 | 66 WFCAM_USB20_P | 66 WFCAM_USB20_N

Smart card

USB2.0 | 94 SMARTCAD_USB20_P | 94 SMARTCAD_USB20_N

TS

USB2.0 | 55 TS_USB20_P | 55 TS_USB20_N

96 HUB_I2C_SCL

96 HUB_I2C_SDA

3D3V_S5 — R3824 330KR1J-GP

C3814 SCD1U16V2KX-3GP — 3D3V_S5

24 HUB_EC_PWRON_N — R3823 1KR1F-GP — HUB_EC_EN_R_N — R3822 20KR1J-GP — HUB_EC_EN_G_N

Q3801 SSM3J327R-GP

84.03327.031

3D3V_HUB_V33

U3802 DY M24C02RMN6TP-GP

E0 E1 E2 VSS — VCC WC# SCL SDA — HUB_I2C_SCL HUB_I2C_SDA

072.24C02.0001

EVT ASM

U3801 FE1D1S-BQFN24B-GP

071.01124.0003

LED1 LED2 DPU DMU BUSJ DRV OVC# PWR# REXT TEST# VBUSM XRSTJ THERMAL_PAD — VDD5 VD33F DP1 DM1 DP2 DM2 DP3 DM3 DP4 DM4 XIN XOUT

HUB_I2C_SCL HUB_I2C_SDA

HUB_USB20_CMC_P HUB_USB20_CMC_N

3D3V_HUB_BUSJ

HUB_OVCJ

HUB_REXT

3D3V_HUB_VBUSM

3D3V_HUB_XRSTJ

25_THM

From USB3 HUB2

R3804 100KR2J-1-GP

R3805 100KR2J-1-GP

R3806 100KR2J-1-GP

R3814 10KR2J-3-GP

OVCJ pin must be pulled high if not used.

C3812 SCD01U16V2KX-3GP

R3818 2K7R2F-GP +/-1%

PWRNC3801 — PWRNC PN3801

WFCAM_USB20_P WFCAM_USB20_N SMARTCAD_USB20_P SMARTCAD_USB20_N TS_USB20_P TS_USB20_N

World Facing Camera

Smart card

TS

XTL_12M_X1_HUB XTL_12M_X2_HUB

3D3V_HUB_VDD — L3801 MMZ1608Y471BTA00-GP — 3D3V_HUB_V33

068.00017.0141

Bead 100MHz/470R/500mA DCR=350~500mohm

C3810 SC22U16V3MX-GP

X3801 XTAL-12MHZ-114-GP

082.30000.0291

82.30006.491-> 082.30000.0291
TAITIEN 082.30000.0381
HARMONY 082.30000.0301
HOSONIC 082.30000.0291

C3802 DY SC20P50V2JN-1GP

C3803 DY SC20P50V2JN-1GP

Co-Layout

HUB_USB20_P — HUB_USB20_N

R3825 0R2J-2-GP

L3802 DY FILTER-4P-61-GP

69.10171.001

R3826 0R2J-2-GP

HUB_USB20_CMC_P — HUB_USB20_CMC_N

D3801 DY PESD5V0H1BSFYL-GP-U1

D3802 DY PESD5V0H1BSFYL-GP-U1

LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB Redriver/Hub)

Size: A3 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 38 of 106

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LAR2 CZ

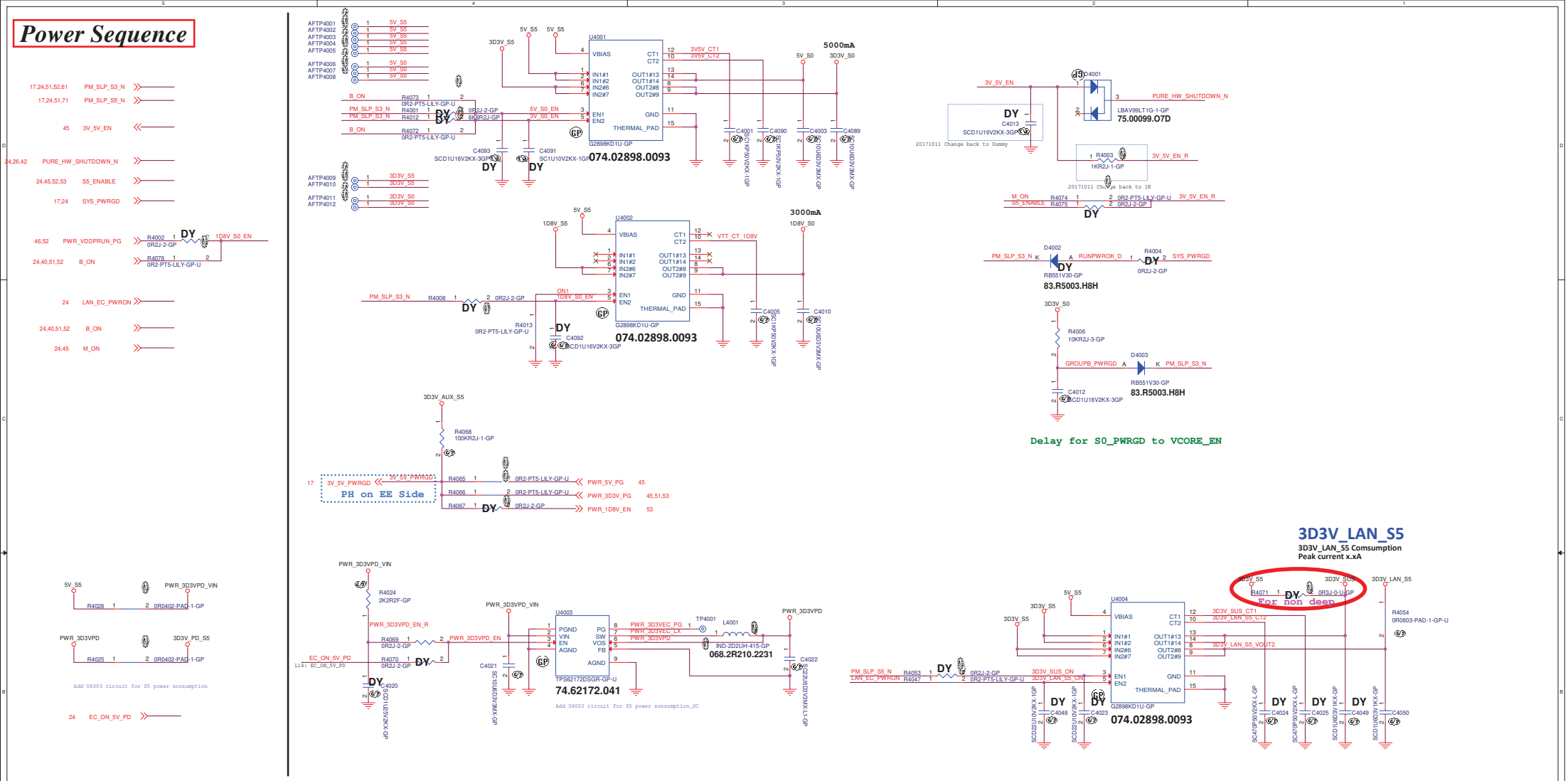
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sequence (RSVD)**

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

Date: Wednesday, July 28, 2021 Sheet 39 of 106

Power Sequence



LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (Power Plane Enable)

Size: A2 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 40 of 106

(Blanking)

LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sequence (RSVD)**

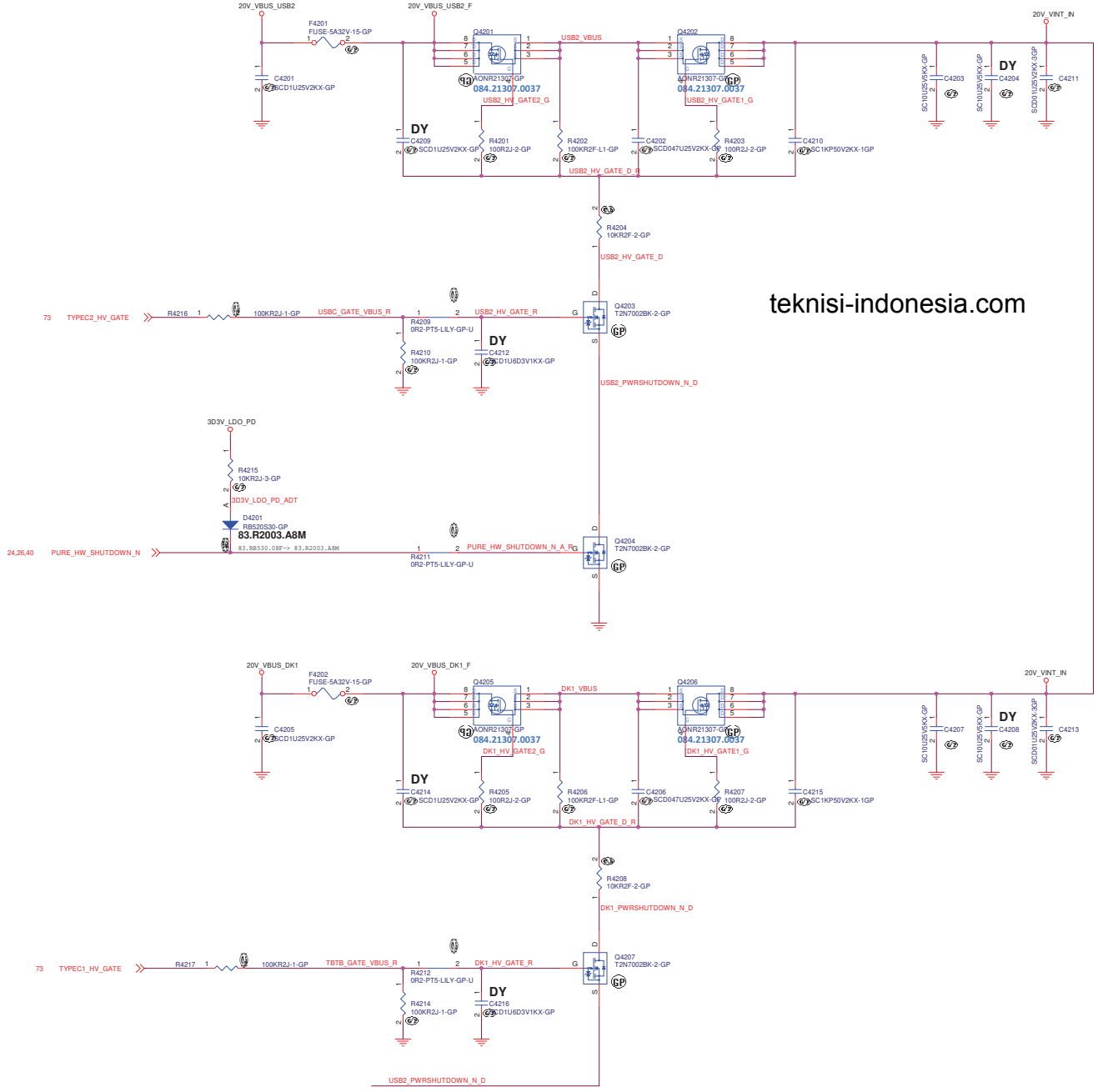
Size	Document Number	Rev
A4	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 41 of 106

Main Func = ADT Input

Q4201, Q4202, Q4205, Q4206

1st	AOS	AONR21307	084.21307.0037



LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

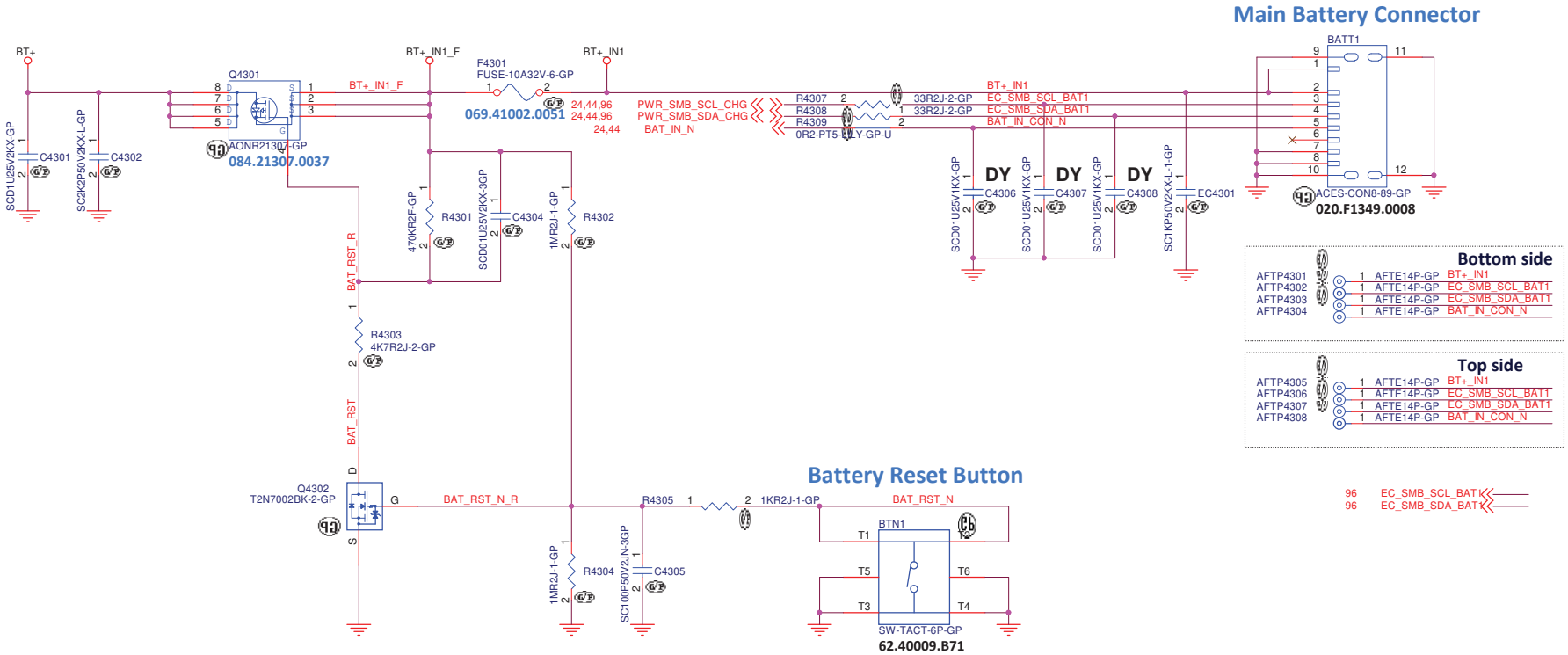
Title: INT IO (TYPEC DC-DC)

Size: A2 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 42 of 106

Main Func = M-BAT Input

Main Func = BAT Reset



LAR2 CZ

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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (ATX/ DC/ BATT Conn)

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Date: Wednesday, July 28, 2021 | Sheet 43 of 106

OFFPAGE – PIC – EE

PH on EE Side

24,42,56	PWR_SMB_SCL_CHG	PWR_SMB_SCL_CHG
24,43,56	PWR_SMB_SDA_CHG	PWR_SMB_SDA_CHG

PH on EE Side

8,24,46	PROCHOT_CPU_N	PROCHOT_CPU_N
24,43	BAT_IN_N	BATT_OUT
24	AC_IN	AC_IN
24	ADP_I	ADP_I
24	AC_OFF	AC_OFF
96	PWR_CHG_SCL	
96	PWR_CHG_SDA	

Device will be transition from normal Buck-Boost operation to PTM operation by:
- Set REGN3 [7] = 0, to disable the EN_EXITILIM.
- Set REGN3[6] = 1.
- Set REGN3[2:1] = 1.
- Ground ILIM_HIZ pin

Device will transition out of PTM mode with host control by:
- Set REGN3[2:1] = 0.
- Pull ILIM_HIZ pin to high.
- Device exits PTM to buck-boost operation if tripping VINDPM or IINDPM.
- Device exits PTM to buck-boost operation under fault conditions (VCOC, TSHUT, BATOC).

For Adapter IN
Confirm with EE

20V_VNT_IN

064.R010L.L005

084.00636.0037

084.00636.0A37

2.2uH,
DCR=16~20mohm,
Idc=8A, Isat=14A
6.8*6.4*3mm

IND-3D2UH-46-GP-U1

074.25710.M001

84.2N702.J31

083.52030.008F

For cost

Reserve for Power test

Reserve for PTM
If it hasn't more GPIO

500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

# of CELL	VCELL_PROG	PR8418
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

0505
buyer: 7"

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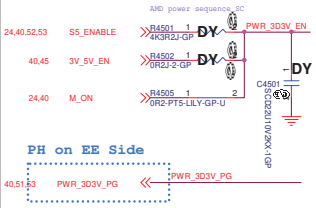
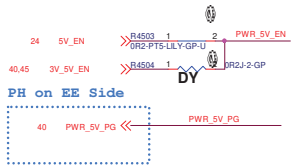
POWER (CHARGER_BQ25710R)

Size: Custom | Document Number: LAR-2 CZ | Rev: -2

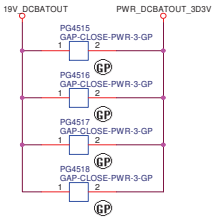
Date: Wednesday, July 08, 2009 | Sheet 44 of 106

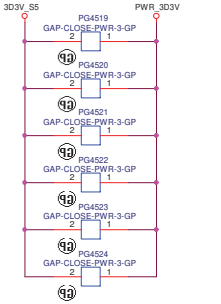
OFFPAGE-Signal

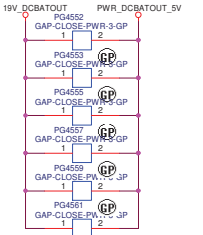


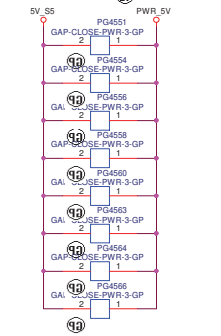


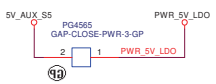
OFFPAGE-GAP

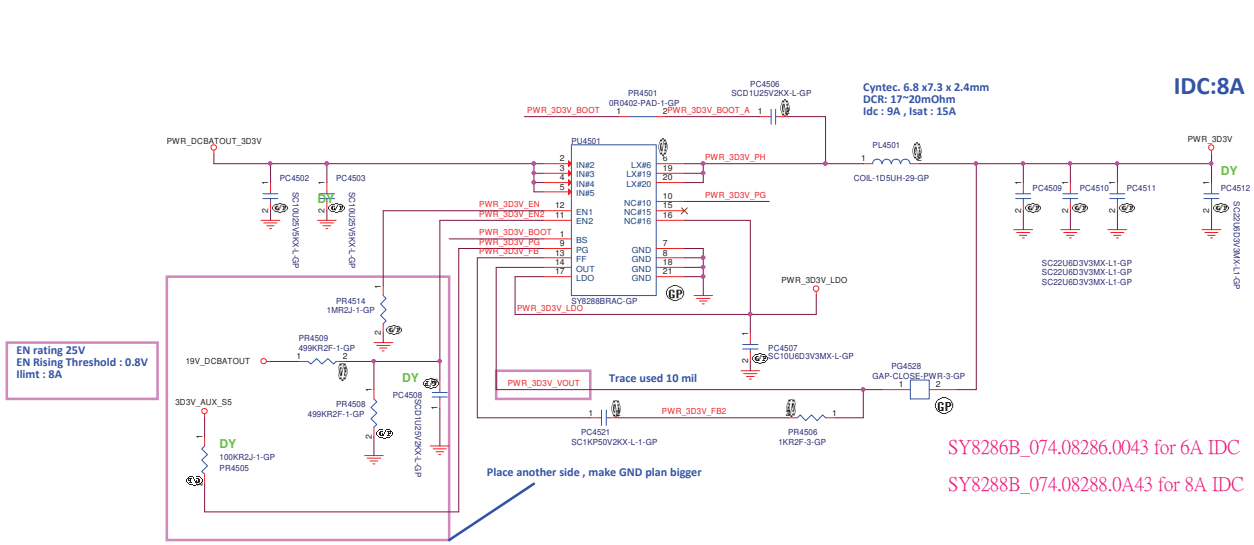


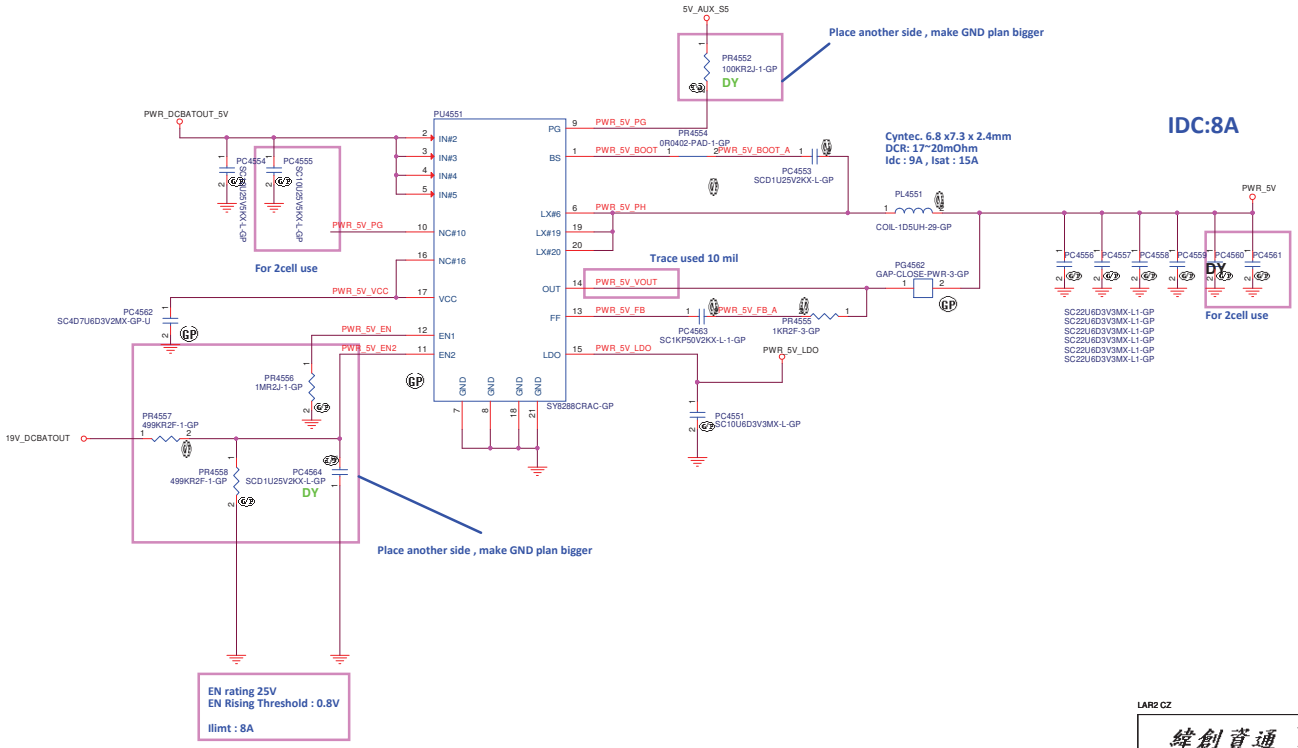












LAR2 CZ

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Title: POWER(SY8288B&SY8288C_3D3V/5V)

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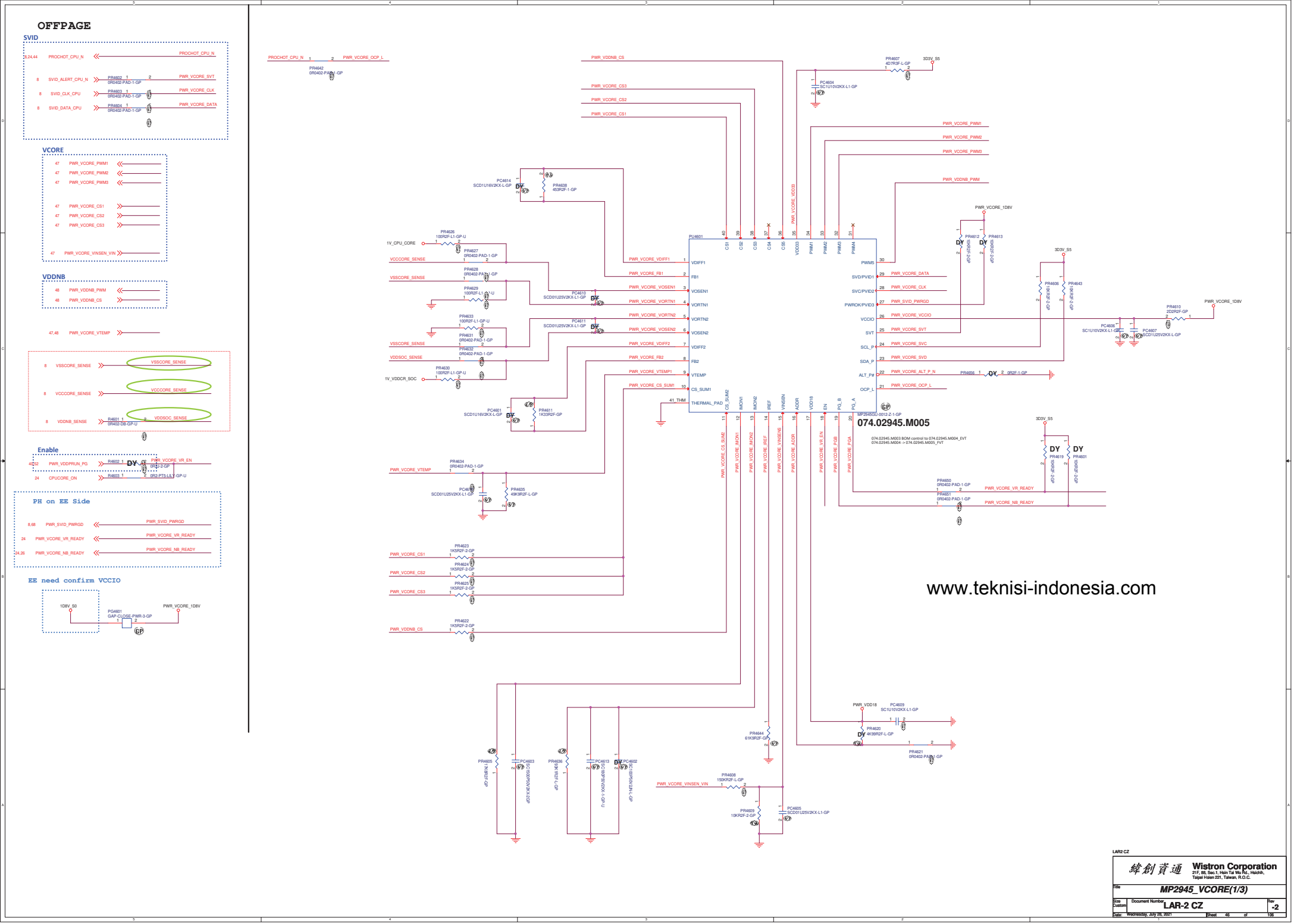
OFFPAGE
SVID
VCORE
VDDNB
Enable
PH on EE Side
EE need confirm VCCIO
PU4601
MP2945GU-0012-Z-1-GP
074.02945.M005
074.02945.M003 BOM control to 074.02945.M004_EVT
074.02945.M004 -> 074.02945.M005_FVT
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MP2945_VCORE(1/3)
LAR-2 CZ
Wednesday, July 28, 2021

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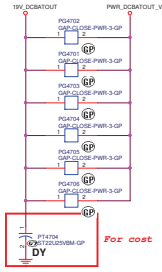
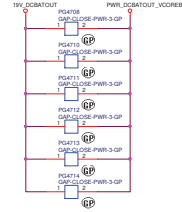
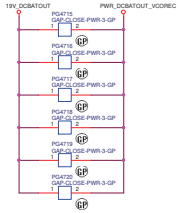




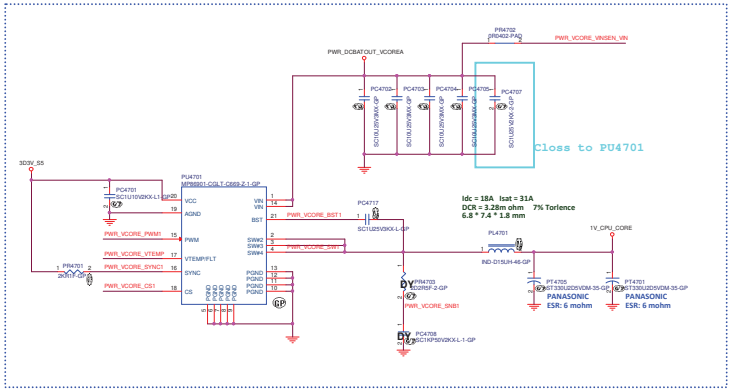


46 PWR_VCORE_PWM1
46 PWR_VCORE_PWM2
46 PWR_VCORE_PWM3

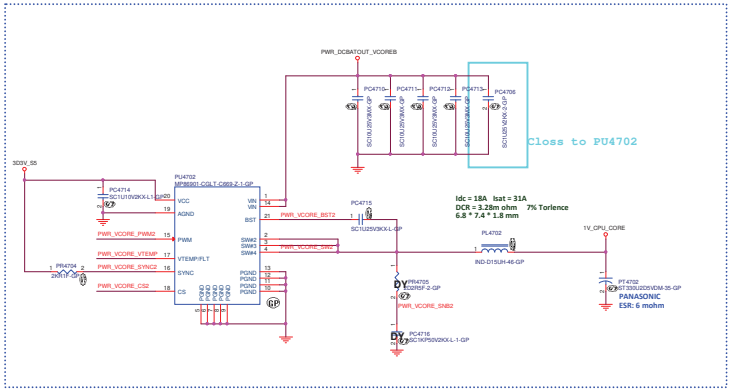
46 PWR_VCORE_CS1
46 PWR_VCORE_CS2
46 PWR_VCORE_CS3

46,48 PWR_VCORE_VTEMP
46 PWR_VCORE_VINSEN_VIN

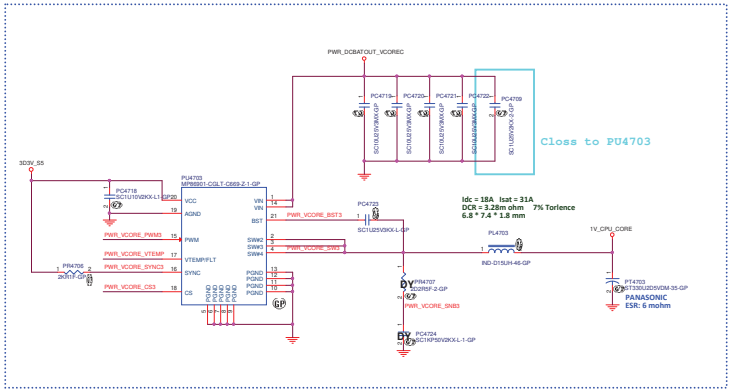
PHASE1



PHASE2



PHASE3



FP6 15W
CPU_CORE
TDC : 33A
Iccmax : 90A
OCP < 112.5A

Table 8. FP6 Processor Voltage Supply Currents for AMD Family 19h Models 50h-5Fh Processors

Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION					
			1 10 W	2 15 W	3 25 W	4 35 W	5 45 W	6 54 W
VDDCR_VDD	Variable	TDC [3]	20	33	44	51	58	
		EDC	70	90	95	105	110	
	(0.6-1.55) [5]	Max Loadstep [4]	60	75	80	90	95	
VDDCR_SOC	Variable	TDC [3]	10	13		15		
		EDC	13	17		20		
	(0.6-1.55) [5]	Max Loadstep [4]	10	13		15		
	1.10	TDC		6.00				

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Title: MP86901_VCORE(2/3)

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19V_DCBATOUT

PWR_DCBATOUT_VDDSOC

PG4802 PG4803 PG4804 PG4801 PG4805 PG4806

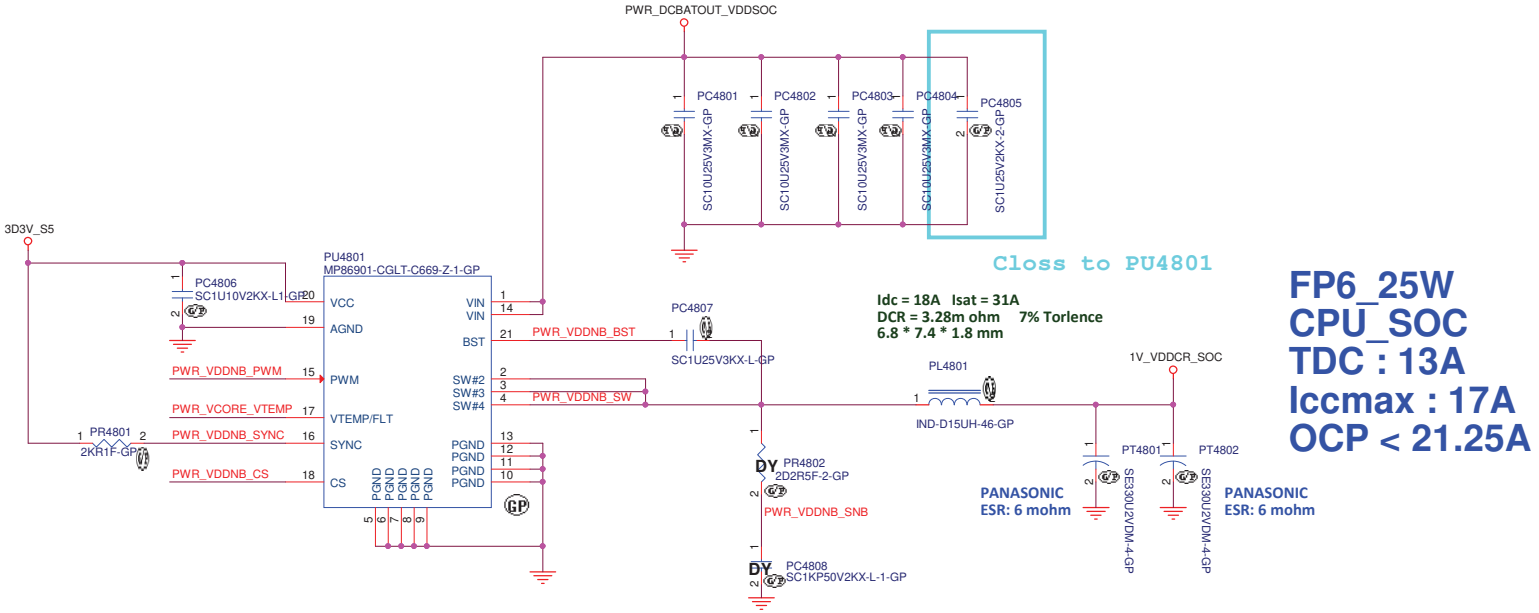
GAP-CLOSE-PWR-GP

46 PWR_VDDNB_PWM

46,47 PWR_VCORE_VTEMP

46 PWR_VDDNB_CS

Main Func = CPU_CORE



LAR2 CZ

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MP86901_VDDCR_SOC(3/3)

Size: Custom | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 48 of 106

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LAR2 CZ

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Title: ***Power (RSVD)***

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Date: Wednesday, July 28, 2021 Sheet 49 of 106

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LAR2 CZ

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Title: ***Power (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

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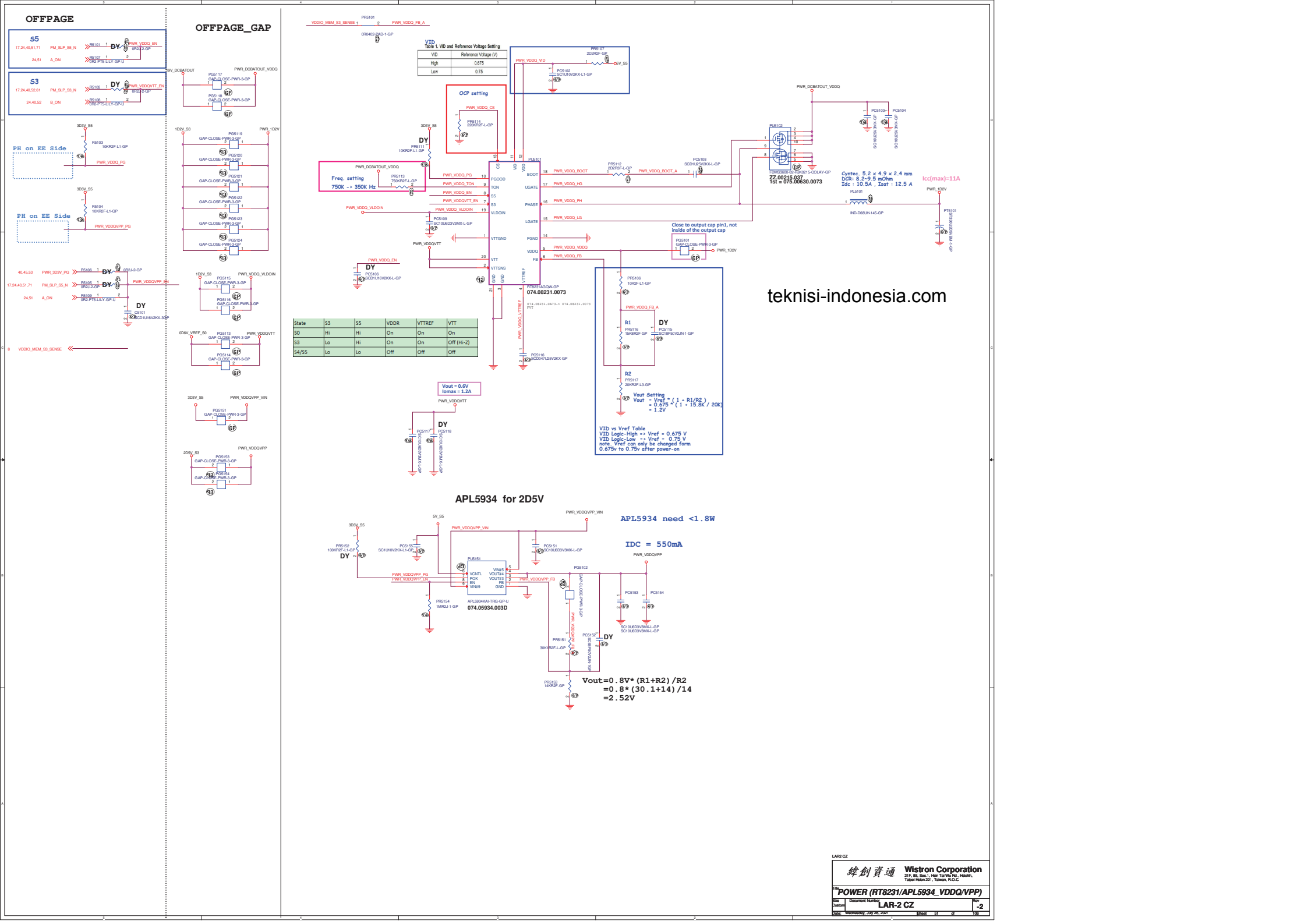
OFFPAGE
OFFPAGE_GAP
S5
S3
PH on EE Side
PH on EE Side
VID
Table 1. VID and Reference Voltage Setting
VID | Reference Voltage (V)
High | 0.875
Low | 0.75
OCP setting
Freq. setting
750K -> 350K Hz
Close to output cap pin1, not inside of the output cap
State | S3 | S5 | VDDR | VTTREF | VTT
S0 | Hi | Hi | On | On | On
S3 | Lo | Hi | On | On | Off (Hi-Z)
S4/S5 | Lo | Lo | Off | Off | Off
Vout = 0.6V
Iomax = 1.2A
APL5934 for 2D5V
APL5934 need <1.8W
IDC = 550mA
Vout=0.8V*(R1+R2)/R2
=0.8*(30.1+14)/14
=2.52V
VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on
Cymtec 5.2 x 4.9 x 2.4 mm
DCR: 8.2~9.5 mOhm
Idc : 10.5A , Isat : 12.5 A
Icc(max)=11A
teknisi-indonesia.com
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Title: POWER (RT8231/APL5934_VDDQ/VPP)
Size: Custom
Document Number: LAR-2 CZ
Rev: -2
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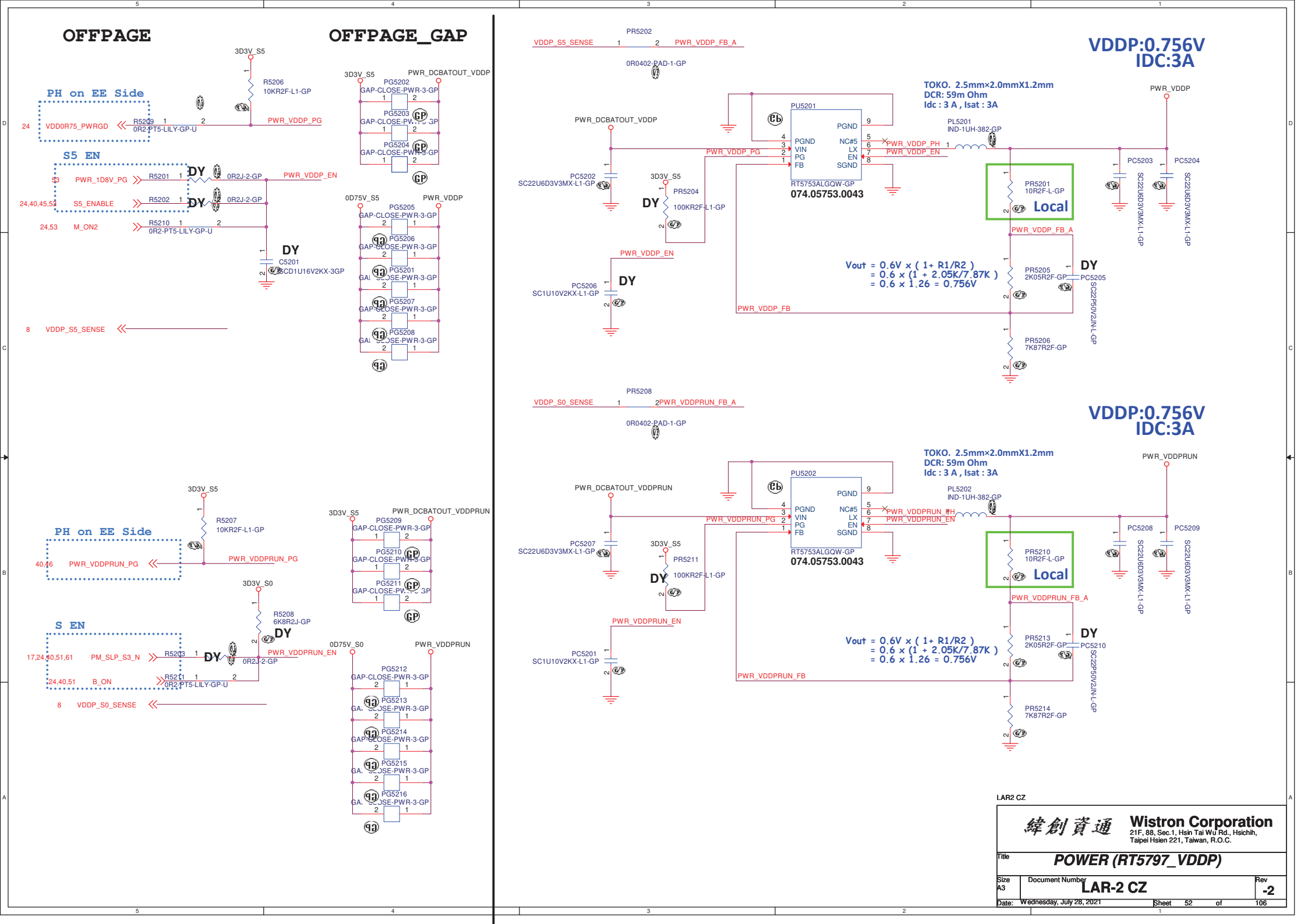
OFFPAGE
OFFPAGE_GAP
PH on EE Side
S5 EN
S EN
VDDP:0.756V
IDC:3A
TOKO. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A
Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 2.05K/7.87K)
= 0.6 x 1.26 = 0.756V
Local
DY
3D3V_S5
PWR_VDDP_PG
PWR_VDDP_EN
PWR_VDDP_FB_A
PWR_VDDP_FB
PWR_VDDPRUN_PG
PWR_VDDPRUN_EN
PWR_VDDPRUN_FB_A
PWR_VDDPRUN_FB
VDDP_S5_SENSE
VDDP_S0_SENSE
PWR_1D8V_PG
S5_ENABLE
M_ON2
B_ON
PM_SLP_S3_N
074.05753.0043
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POWER (RT5797_VDDP)
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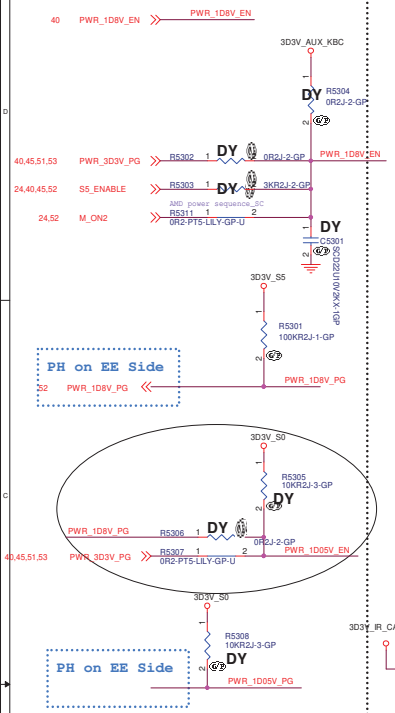
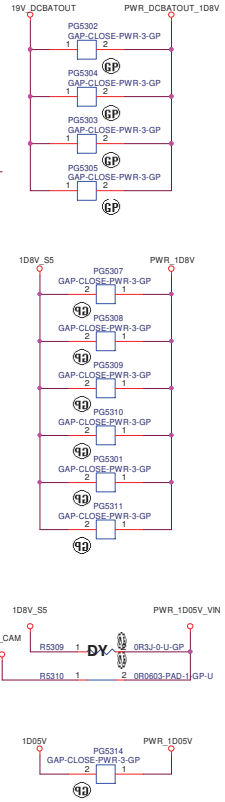
OFFPAGE-Signal

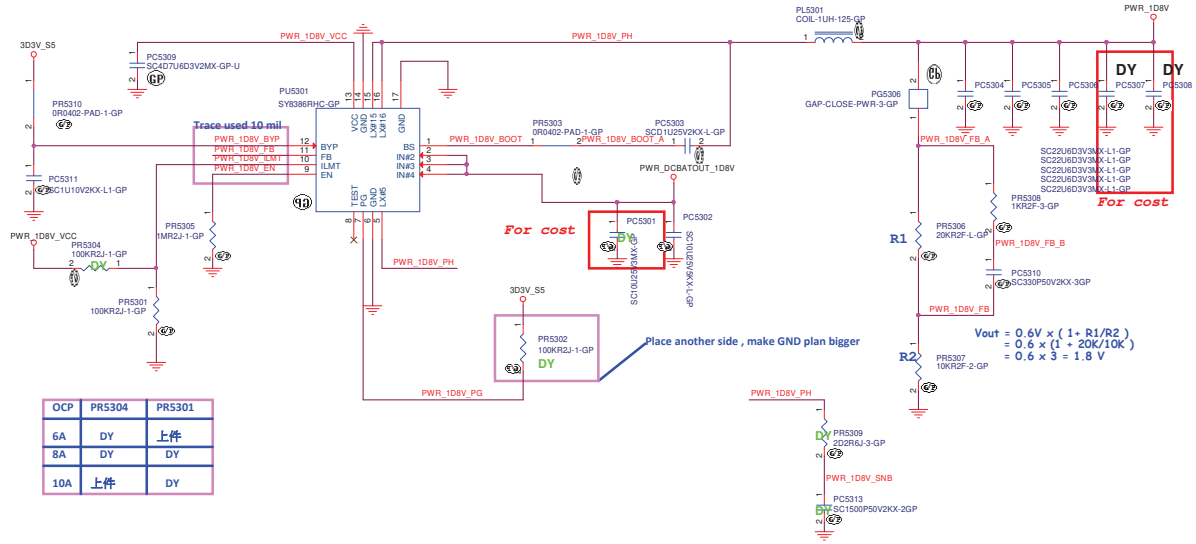


OFFPAGE-GAP



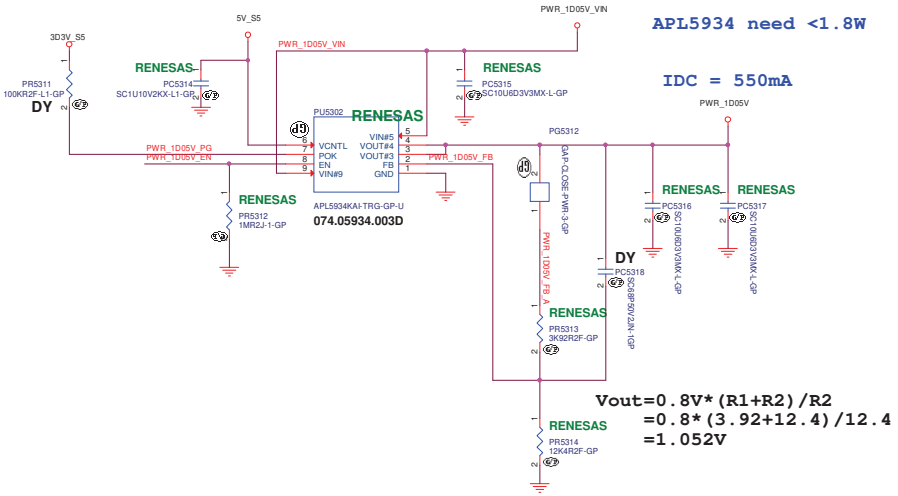
Cyntec 4.45mm × 4.75mm x 2mm
DCR: 23m Ohm
Idc : 4.5 A , Isat : 7.5A

IDC:3.4A



OCP	PR5304	PR5301
6A	DY	上件
8A	DY	DY
10A	上件	DY

APL5934 for 1D05V



LAR2 CZ

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Title: ***POWER(SY8386R 1D8V)***

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LAR2 CZ

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Title: ***POWER(RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

Date: Wednesday, July 28, 2021 Sheet 54 of 106

Main Func = LCD

LCD Backlight Power

19V_DCBATOUT → F5501 POLYSW-TG1A24V-5-GP 69.50007.G71 → 19V_DCBATOUT_LCD

19V_DCBATOUT_LCD → SCD47U25V6KX-L2-GP DY C5515

For LCD DCBATOUT inruch current

3D3V_LCDVDD → R5529 0R0402-PAD-1-GP → 3D3V_LCDVDD_R

3D3V_S5 → U5501 G517F1T12U-GP 074.51712.009F (IN, EN, OUT, GND, OC#) → 3D3V_LCDVDD_R

3D3V_LCDVDD_R → C5502 SCD47U6D3V2MX-GP-U

EDP_VDD_EN_LCD → D5503 RB520S30-GP 83.R2003.A8M → EDP_VDD_EN_LCD_R

EDP_VDD_EN_LCD_R → R5515 100KR2J-1-GP → C5506 SCD47U6D3V2MX-GP-U

24,55 LCD_SELF_TEST_ON → D5501 RB520S30-GP 83.R2003.A8M

83.RB530.08F-> 83.R2003.A8M

8 PANEL_BKLTCTL → R5540 100KR2J-1-GP

3D3V_S0 → R5541 1KR2J-1-GP, R5542 100KR2F-L3-GP → Q5503 PJT138KA-GP 075.00138.0A7C → PANEL_BKLTCTL_LCD_G

PANEL_BKLTCTL_LCD → R5567 0R2-PT5-L8LY-GP-U → C5532 SC100P50V2JN-3GP

3D3V_S0 → R5509 1KR2J-1-GP DY → LCD_BRIGHTNESS_R → D5504 RB520S30-GP 83.R2003.A8M → LCD_BRIGHTNESS

LCD_SELF_TEST_ON → D5505 RB520S30-GP 83.R2003.A8M

8 EDP_VDD_EN → R5543 100KR2J-1-GP

3D3V_S0 → R5544 4K7R2J-2-GP, R5545 100KR2F-L3-GP → Q5504 PJT138KA-GP 075.00138.0A7C → EDP_VDD_EN_G → EDP_VDD_EN_LCD

3D3V_S0 → R5511 DY 0R3J-0-U-GP → 3D3V_S0_TOUCH

3D3V_S5 → R5569 DY 0R3J-0-U-GP

eDP_AUX_CON_N → R5502 DY 100KR2J-1-GP → 3D3V_S0

eDP_AUX_CON_P → R5503 DY 100KR2J-1-GP → 3D3V_S0

24 TOUCH_EC_PWRON_N → R5571 1KR1F-GP → TOUCH_EC_EN_R_N → R5572 330KR1J-GP (3D3V_S5) → TOUCH_EC_EN_G_N → R5570 20KR1J-GP → Q5505 SSM3J327R-GP 84.03327.031 (G, S, D; 3D3V_S5) → 3D3V_S0_TOUCH

C5533 SCD1U16V2KX-3GP (3D3V_S5)

3D3V_S0_TOUCH → R5568 10KR2J-3-GP DY

3D3V_S0_TOUCH → R5517 10KR2J-3-GP

19V_DCBATOUT_LCD → C5503 SCD1U25V2KX-GP, C5504 SCD01U25V2KX-3GP

3D3V_S0_TOUCH → C5505 SCD1U6D3V1KX-GP

LCD Connector

LCD1 HRS-CON30-9-GP 020.K0032.0030

24,55 LCD_SELF_TEST_ON
17 TOUCH_RESET_N
17 TOUCH_EN
17 TOUCH_STOP_N
TS_USB20_CON_N
TS_USB20_CON_P

8 eDP_TX_CPU_N1 / 8 eDP_TX_CPU_P1 → C5531, C5519 SCD1U6D3V1KX-GP → eDP_TX_CON_N1 / eDP_TX_CON_P1

8 eDP_TX_CPU_N0 / 8 eDP_TX_CPU_P0 → C5530, C5521 SCD1U6D3V1KX-GP → eDP_TX_CON_N0 / eDP_TX_CON_P0

8 EDP_AUX_CPU_P / 8 EDP_AUX_CPU_N → C5509, C5510 SCD1U6D3V1KX-GP → eDP_AUX_CON_P / eDP_AUX_CON_N

eDP_HPD_CONN
BLON_OUT_C
LCD_BRIGHTNESS

3D3V_LCDVDD → SC1U10V2KX-1GP DY C5511, SCD1U6D3V1KX-GP C5512

24 BLON_OUT → R5507 1KR2J-1-GP

LCD_SELF_TEST_ON → R5508 100KR2J-1-GP, C5514 SC100P50V2JN-3GP DY, R5565 10KR2J-3-GP, C5513 SC100P50V2JN-3GP, R5566 100KR2J-1-GP

ED5501 AZ5125-02S-R7G-GP DY

R5512 100KR2J-1-GP

Near LCD CONN (LCD1)

3D3V_LCDVDD, 19V_DCBATOUT_LCD, 3D3V_S0_TOUCH

AFTP5501 AFTE14P-GP LCD_SELF_TEST_ON
AFTP5502 AFTE14P-GP TOUCH_RESET_N
AFTP5503 AFTE14P-GP TOUCH_EN
AFTP5504 AFTE14P-GP TOUCH_STOP_N
AFTP5505 AFTE14P-GP BLON_OUT_C
AFTP5506 AFTE14P-GP LCD_BRIGHTNESS

AFTP5509 AFTE14P-GP 3D3V_S0_TOUCH
AFTP5510 AFTE14P-GP 19V_DCBATOUT_LCD
AFTP5511 AFTE14P-GP
AFTP5512 AFTE14P-GP

DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

LCD Self-Test is working under S5: (The function should work even CPU doesn't work)

(1) Put system in S5 state
(2) Press power button with Fn + Left-Ctrl
(3) System enter LCD self-test mode

eDP_HPD_CONN → R5520 0R0201-PAD-2-GP → EDP_HPD_CPU 8,55

3D3V_S0 → R5519 10KR1J-GP DY → EDP_HPD_CPU

R5518 100KR1J-1-GP DY

eDP_HPD_CONN_G1 → Q5502 T2N7002BK-2-GP DY (G, D, S)

eDP_HPD_CONN → Q5501 T2N7002BK-2-GP DY (G, D, S)

For eDP level shift.
1. TGL CPU eDP HPD Vih is 2.475.
2. CML CPU eDP HPD Vih is 2.31.

Co-Layout

38 TS_USB20_N → R5574 0R2J-2-GP → L5502 DLM0NSN900HY2D-GP DY → TS_USB20_CON_N

38 TS_USB20_P → R5573 0R2J-2-GP → L5502 → TS_USB20_CON_P

LAR2 CZ

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Title: Display (LCD/TOUCH/DMIC)
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3D3V_S0 — R5614 1 — DY — 0R2J-2-GP — 3D3V_IR_CAM

3D3V_S5 — R5615 1 — DY — 0R2J-2-GP

3 CCD_PCIE_TX_C_P
3 CCD_PCIE_TX_C_N
3 CCD_PCIE_RX_P
3 CCD_PCIE_RX_N
16 CCD_CLK_CPU_P
16 CCD_CLK_CPU_N

18 CCD_USB20_P
18 CCD_USB20_N
66 CCD_USB20_CON_N
66 CCD_USB20_CON_P
27,66 DMIC_SCL_CODEC_CON
27,66 DMIC_SDA_CODEC_CON

3D3V_IR_CAM — R5613 0R0402-PAD-1-GP — 3D3V_UPD — C5605 SC10U6D3V3MX-GP

3D3V_IR_CAM — C5606 C5607 C5615 C5616 C5617 C5618 SCD1U16V2KX-3GP — Close to pin12 / Close to pin22 / Close to pin34 / Close to pin43

1D05V — C5608 C5609 C5610 C5619 C5620 C5621 C5622 C5623 C5624 C5625 SCD1U25V2KX-3GP — Close to pin6 / Close to pin9 / Close to pin21 / Close to pin30 / Close to pin33 / Close to pin33 / Close to pin42

3D3V_UPD — C5611 C5613 C5612 C5614 SCD1U16V2KX-3GP — Close to pin3 / Close to pin25

D5601 change from 83.01294.011 to 083.01294.0011
083.01294.0011 LIT KEEP
-> 083.00040.0081

083.00040.0081-> 083.01294.0011 change to 75.00054.A7D
EVT verify!!

3D3V_IR_CAM — D5601 BAT54C-12-GP — 75.00054.A7D — R5610 10KR2J-3-GP — UPD_PONRST_N

C5604 SC10U6D3V3MX-GP — C5604 changed to 10uF to countermeasure the delay from 3D3V to 1D05V rising

XTL_24M_X1_UPD — R5605 — XTL_24M_X1
XTL_24M_X2_UPD — R5606 — XTL_24M_X2
0R2J-2-GP — 680R2J-3-GP
X5601 XTAL-24MHZ-182-GP — 082.30006.0531
C5602 SC10P50V2JN-4GP — C5601 SC10P50V2JN-4GP

	C1601	C1602	
TAITIEN 082.30006.0941	8pF	8pF	common table but orcad not common
HARMONY 082.30006.0531	8pF	8pF	common
HOSONIC 082.30006.0561	8pF	8pF	common

3D3V_S5 — R5624 330KR1J-GP — C5630 SCD1U16V2KX-3GP — Q5601 SSM3J327R-GP — 84.03327.031

24,66 CAM_EC_PWRON_N — R5623 1KR1F-GP — CAM_EC_EN_R_N — R5622 20KR1J-GP — CAM_EC_EN_G_N

1D05V — U5601 — RENESAS

VDD10 ×8 — VDD33 ×4 — AVDD33 ×2

U3RXDP1 — UPD_U3RXDP1 — R5625 — 0R2-PT5-LILY-GP-U
U3RXDN1 — UPD_U3RXDN1 — R5626 — 0R2-PT5-LILY-GP-U
U3RXDP2 — UPD_U3RXDP2 — R5627 — 0R2-PT5-LILY-GP-U
U3RXDN2 — UPD_U3RXDN2 — R5628 — 0R2-PT5-LILY-GP-U

U3TXDP1
U3TXDN1
U3TXDP2
U3TXDN2

PECLKP — CCD_CLK_CPU_P
PECLKN — CCD_CLK_CPU_N

PERXP — CCD_PCIE_TX_C_P
PERXN — CCD_PCIE_TX_C_N

PETXP — UPD_CCD_PCIE_RX_P — C5626 SCD1U16V2KX-3GP — CCD_PCIE_RX_P
PETXN — UPD_CCD_PCIE_RX_N — C5627 SCD1U16V2KX-3GP — CCD_PCIE_RX_N

PCI Express Gen.2 (90ohm-differential)

PERST# — PTU_PLT_RST_N
PEWAKE# — PCIE_WAKE_UPD_N — R5612 — DY — 0R2J-2-GP — PCIE_WAKE_CPU_N — 17,18,24,33,61
PECREQ# — CCD_CLKREQ_CPU_N — 16

SPISCK — SPI_CLK_UPD
SPICS# — SPI_CS_UPD_N
SPISI — SPI_SI_UPD
SPISO — SPI_SO_UPD

RREF — UPD_RREF — R5607 — 1K6R2F-GP
IC_L
GND

CCD_USB20_CON_P — R5603 — 0R2J-2-GP — UPD_U2DP1 — U2DP1
CCD_USB20_CON_N — R5604 — 0R2J-2-GP — UPD_U2DM1 — U2DM1

UPD_U2DP2 — U2DP2
UPD_U2DM2 — U2DM2

3D3V_IR_CAM — RN5601 — SRN4K7J-8-GP — OCI1_N — OCI1# — OCI2_N — OCI2#

PPON1
PPON2

XTL_24M_X1_UPD — XT1
XTL_24M_X2_UPD — XT2

3D3V_IR_CAM — R5611 — 10KR2J-3-GP — UPD_PONRST_N — PONRST# — UPD_SMI_N — SMI#

R5629 — 0R2-PT5-LILY-GP-U — UPD_U2DP2
R5630 — 0R2-PT5-LILY-GP-U — UPD_U2DM2

UPD720202K8-701-BAA-A-1-GP — 071.72202.0003

NON_RENESAS — R5601 — 0R2J-2-GP — EL5601 DLM0NSN900HY2D-GP — 068.09002.2001 — R5602 — 0R2J-2-GP — NON_RENESAS

CCD_USB20_N — CCD_USB20_CON_N
CCD_USB20_P — CCD_USB20_CON_P

CCD CONN

068.09002.2001
2nd: 68.02002.061
3rd: 068.00104.0001

ED5601 AZ1043-04F-R7G-GP — 075.01043.0073

CCD_USB20_CON_N — CCD_USB20_CON_N
CCD_USB20_CON_P — CCD_USB20_CON_P
DMIC_SDA_CODEC_CON — DMIC_SDA_CODEC_CON
DMIC_SCL_CODEC_CON — DMIC_SCL_CODEC_CON

075.01043.0073
075.PUSB3.0A73
075.00199.007C-> 075.01043.0073 layout impact.

If 3V3D_S5 to 3D3V_IR_CAM,
R5616.R5617.R5618
need to pull-high and pull-low resistors
to prevent leakage from 3D3V_S5

3D3V_IR_CAM — R5616 10KR2J-3GP — R5609 47KR2J-2GP — R5608 10KR2J-3GP — R5617 10KR2J-3GP

SPI_CS_UPD_N
SPI_SO_UPD
SPI_WP_UPD_N

U5602 — CS# SO WP# GND — VCC NC#7 SCLK SI — MX25L5121EMC-20G-GP — 72.25512.J01

SPI_CLK_UPD
SPI_SI_UPD

C5603 SCD1U16V2KX-3GP — R5618 100KR2J-1-GP

FEROM, P/N old & new version
72.25512.J01& 072.25512.0X01

A — Y — B

Function Table

INPUTS A	INPUTS B	OUTPUT Y
H	H	H
L	X	L
X	L	L

3D3V_IR_CAM — Follow L14

17,24,31,33,61,63,68,89,91 PLT_RST_N — R5620 0R2-PT5-LILY-GP-U — IR_PLT_RST_N
24 PTU_EC_RST_N

U5603 TC7SZ08FU-LJ-CY-GP — 073.7SZ08.000G

C5628 SCD1U6D3V1KX-GP — R5619 10KR2J-L-GP — DY

R5621 100KR2J-1-GP — PTU_PLT_RST_N — C5629 SC180P50V2KX-1-GP-U

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Title: **Display (CRT/IR Camera)**

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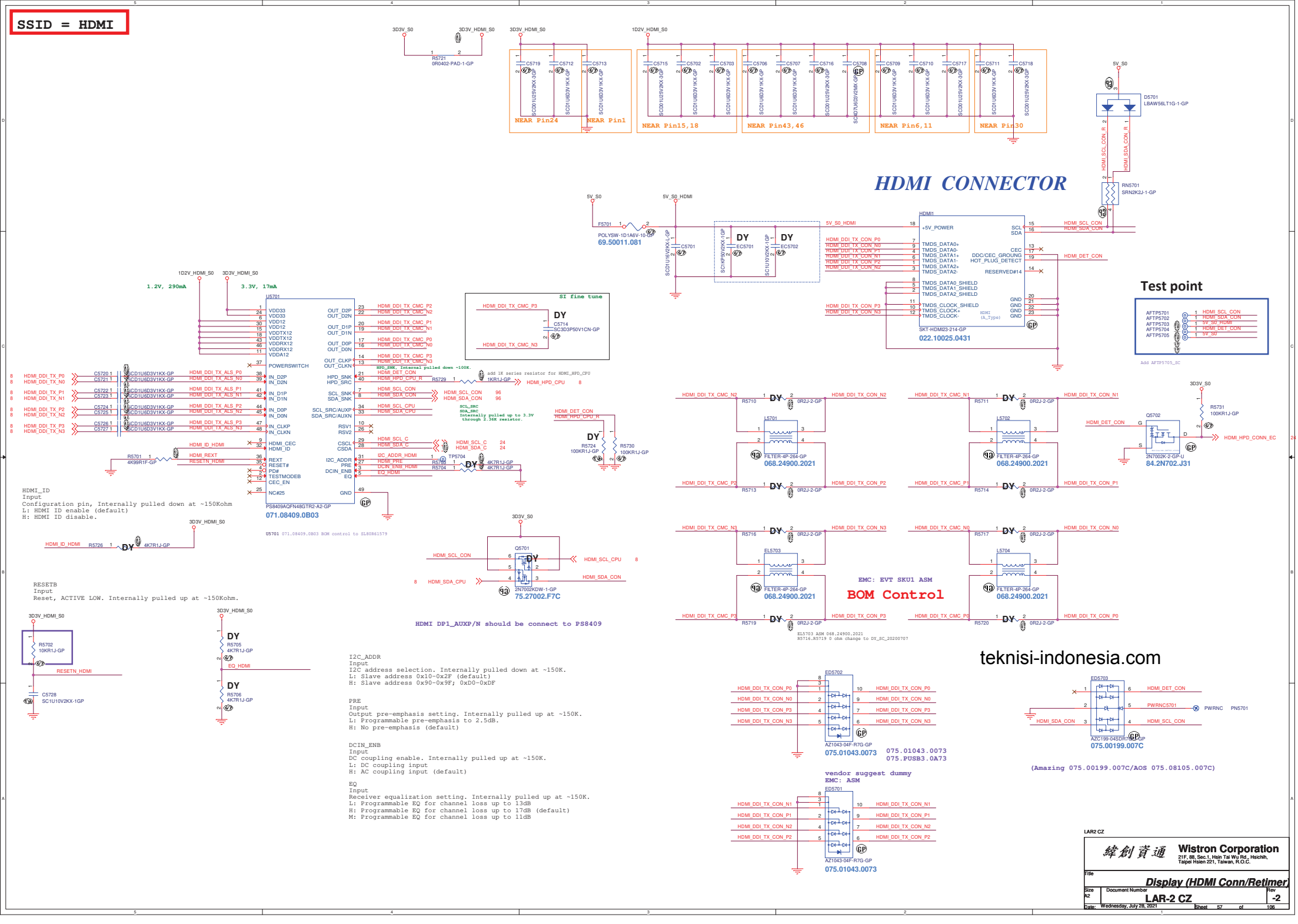
SSID = HDMI

HDMI CONNECTOR



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Title: ***Display (RSVD) DP / DVI***

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Title: ***Display (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

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A4	**LAR-2 CZ**	**-2**

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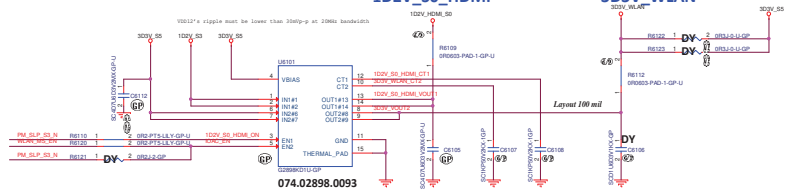
Main Func = WLAN

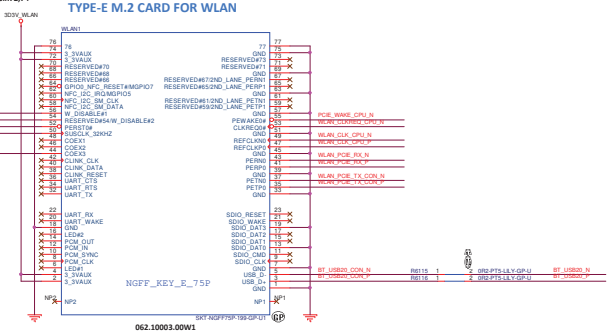
V2 Modern Standby CIRCUIT

1D2V_S0_HDMI

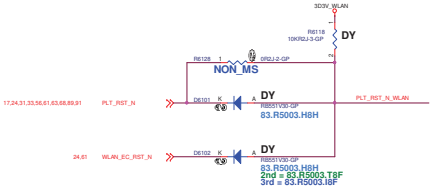


3D3V_WLAN

TYPE-E M.2 CARD FOR WLAN



NON_MS



MS

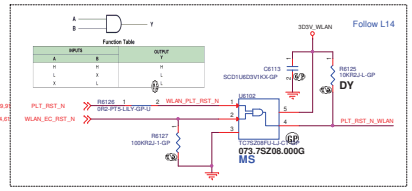


Table 3–1 Key AE 2230-platform and module pinout (M.2 revision fo

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	Voltage on Card Side	WLAN or BT
1	GND	GND		
2	3.3 V	3.3 V	3.3 V	All
3	USB_D+	USB_D+	3.3 V	BT
4	3.3 V	3.3 V	3.3 V	All
5	USB_D-	USB_D-	3.3 V	BT
6	LED1	LED1	3.3v	WLAN
7	GND	GND		
8	Connector Key	Connector Key		
9	Connector Key	Connector Key		
10	Connector Key	Connector Key		
11	Connector Key	Connector Key		
12	Connector Key	Connector Key		
13	Connector Key	Connector Key		
14	Connector Key	Connector Key		
15	Connector Key	Connector Key		
16	LED2	LED2	3.3v	BT
17	NC	NC	NA	
18	GND	GND		
19	NC	NC	NA	
20	NC	NC	NA	
21	NC	NC	NA	
22	NC	NC	NA	
23	NC	NC	NA	
24	Connector Key	Connector Key		
25	Connector Key	Connector Key		
26	Connector Key	Connector Key		
27	Connector Key	Connector Key		
28	Connector Key	Connector Key		
29	Connector Key	Connector Key		
30	Connector Key	Connector Key		
31	Connector Key	Connector Key		
32	NC	NC	NA	
33	GND	GND		
34	NC	NC	NA	
35	PETp0	PERp0	PCIe PHY	WLAN
36	NC	NC	NA	
37	PETn0	PERn0	PCIe PHY	WLAN
38	CLINK RESET (O)(0/3.3 V)	CLINK RESET (I)(0/3.3 V)	3.3 V	WLAN
39	GND	GND		
40	CLINK DATA	CLINK DATA	CLINK PHY (1 V)	WLAN
41	PERp0	PETp0	PCIe PHY	WLAN
42	CLINK CLK	CLINK CLK	CLINK PHY (1 V)	WLAN
43	PERn0	PETn0	PCIe PHY	WLAN
44	COEX3(I/O) (0/1.8V)	COEX3(I/O) (0/1.8 V)	1.8 V	WLAN + BT
45	GND	GND		
46	COEX2(I/O) (0/1.8V)	COEX2(I/O)(0/1.8V)	1.8 V	WLAN + BT
47	REFCLKP0	REFCLKP0	PCIe PHY	WLAN
48	COEX1 (I/O)(0/1.8 V)	COEX1 (I/O)(0/1.8V)	1.8 V	WLAN + BT
49	REFCLKN0	REFCLKN0	PCIe PHY	WLAN
50	SUSCLK (32 kHz) (O)(0/3.3 V)	SUSCLK (32 kHz) (I)(0/3.3 V)	3.3 V	WLAN + BT
51	GND	GND		
52	PERST0# (O)(0/3.3 V)	PERST0# (I)(0/3.3 V)	3.3 V	WLAN
53	CLKREQ0# (IO)(0/3.3 V)	CLKREQ0# (IO)(0/3.3 V)	3.3 V	WLAN
54	W_DISABLE2# (O)(0/3.3 V)	W_DISABLE2# (I)(0/3.3 V)	3.3 V	BT
55	PEWAKE0# (IO)(0/3.3 V)	PEWAKE0# (IO)(0/3.3 V)	3.3 V	WLAN
56	W_DISABLE1# (O)(0/3.3 V)	W_DISABLE1# (I)(0/3.3 V	3.3v	WLAN
57	GND	GND		
58	I2C DATA (IO)/UART_RX (I)(0/1.8)	I2C DATA (IO)/UART_TX (O)(0/1.8 V)	1.8 V	WLAN + BT
59	PETp1	PERp1	PCIe PHY	N/A
60	I2C CLK/UART_TX (O)(0/1.8 V)	I2C CLK/UART_RX (I)(0/1.8 V)	1.8 V	WLAN + BT
61	PETn1	PERn1	PCIe PHY	N/A
62	ALERT#/UART_CTS (I)(0/1.8 V)	ALERT#/UART_RTS (O)(0/1.8 V)	1.8 V	WLAN + BT
63	GND	GND		
64	NFC_RESET#/UART_RTS (O)(0/1.8 V)	NFC_RESET#/UART_CTS (I)(0/1.8 V)	1.8 V	WLAN + BT
65	PERp1	PETp1	PCIe PHY	N/A
66	PERST1# (O)(0/3.3 V)	PERST1# (I)(0/3.3 V)	3.3 V	N/A
67	PERn1	PETn1	PCIe PHY	N/A
68	CLKREQ1# (IO)(0/3.3 V)	CLKREQ1# (IO)(0/3.3 V)	3.3 V	N/A
69	GND	GND		
70	PEWAKE1# (IO)(0/3.3 V)	PEWAKE1# (IO)(0/3.3 V)	3.3 V	N/A
71	REFCLKP1	REFCLKP1	PCIe PHY	N/A
72	3.3 V	3.3 V		
73	REFCLKN1	REFCLKN1	PCIe PHY	N/A
74	3.3 V	3.3 V		
75	GND	GND		

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Title: INT IO (WLAN M.2)

Size: A3 | Document Number: LAR-2 CZ | Rev: -2

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Title ***INT IO (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

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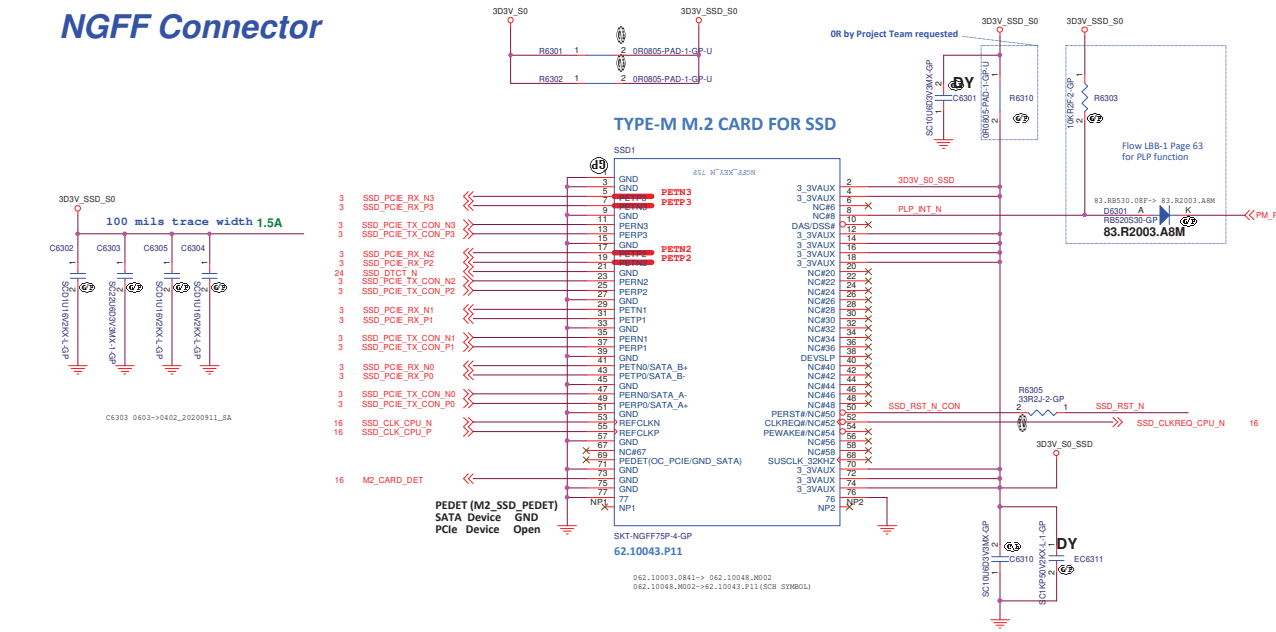
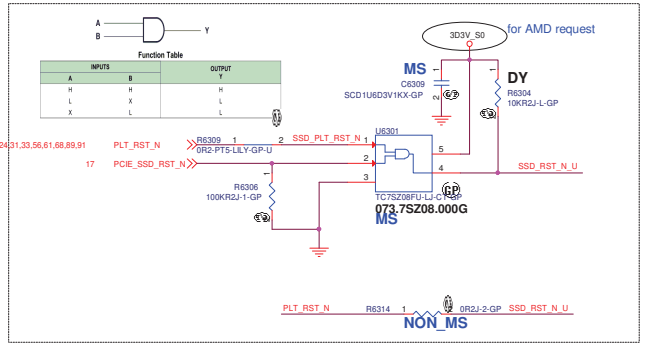
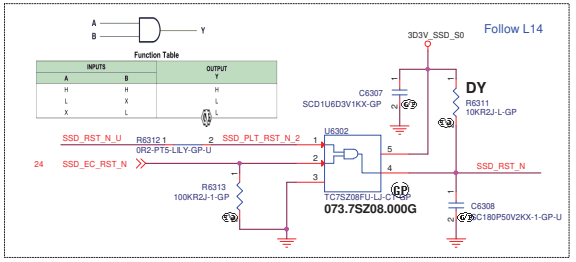
NGFF Connector







5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinout and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (69) will indicate to the platform which I/F of these two is actually connected.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	

Pin #	Function	Definition	Pin #	Function	Definition
1	GND	Ground	2	3.3V	3.3 V Source
3	GND	Ground	4	3.3V	3.3 V Source
5	PETn3	PCIe Tx3-	6	N/C	N/C
7	PETp3	PCIe Tx3+	8	PLP INIT#	PLP INIT#
9	GND	Ground	10	LED1#	Device Activity Signal
11	PERn3	PCIe Rx3-	12	3.3V	3.3 V Source
13	PERp3	PCIe Rx3+	14	3.3V	3.3 V Source
15	GND	Ground	16	3.3V	3.3 V Source
17	PETn2	PCIe Tx2-	18	3.3V	3.3 V Source
19	PETp2	PCIe Tx2+	20	N/C	N/C
21	GND	Ground	22	N/C	N/C
23	PERn2	PCIe Rx2-	24	N/C	N/C
25	PERp2	PCIe Rx2+	26	N/C	N/C
27	GND	Ground	28	N/C	N/C
29	PETn1	PCIe Tx1-	30	PLP_FDBK#	Reserved for PLP_FDBK#
31	PETp1	PCIe Tx1+	32	N/C	N/C
33	GND	Ground	34	N/C	N/C
35	PERn1	PCIe Rx1-	36	N/C	N/C
37	PERp1	PCIe Rx1+	38	N/C	N/C
39	GND	Ground	40	SMB_CLK	SMBus Clock (Default disabled)
41	PETn0	PCIe Tx0-	42	SMB_SDA	SMBus Data (Default disabled)
43	PETp0	PCIe Tx0+	44	ALERT#	Alert notification (Default disabled)
45	GND	Ground	46	N/C	N/C
47	PERn0	PCIe Rx0-	48	N/C	N/C
49	PERp0	PCIe Rx0+	50	PERST#	PCIe Reset
51	GND	Ground	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKn	PCIe Reference Clock-	54	N/C	N/C
55	REFCLKp	PCIe Reference Clock+	56	N/C	N/C
57	GND	Ground	58	N/C	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3 V Source
71	GND	Ground	72	3.3V	3.3 V Source
73	GND	Ground	74	3.3V	3.3 V Source
75	GND	Ground			

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Title: INT IO (SSD M.2/ eMMC)

Size: A2 | Document Number: LAR-2 CZ | Rev: -2

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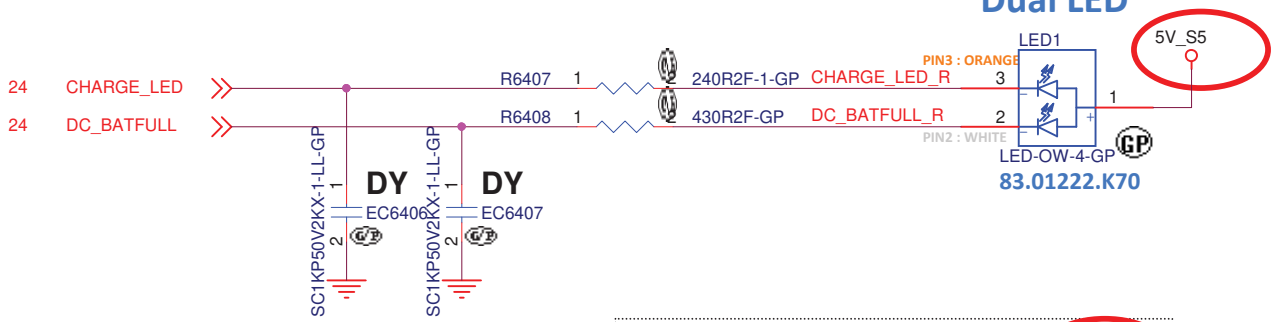
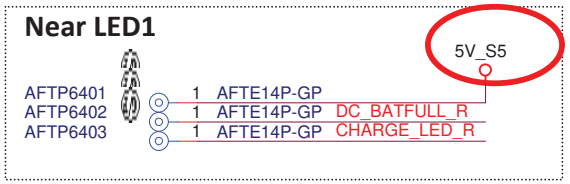
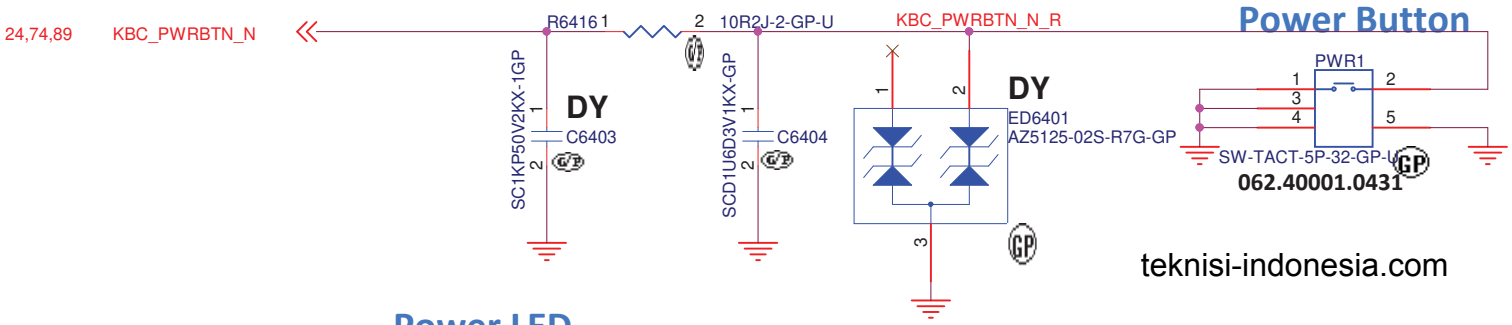
Dual LED



Near LED1

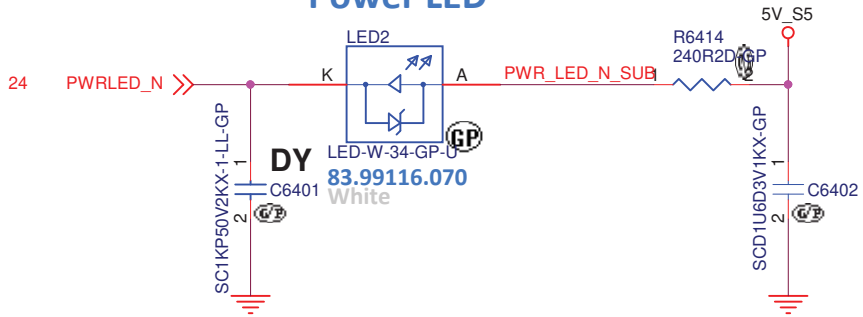


Power Button



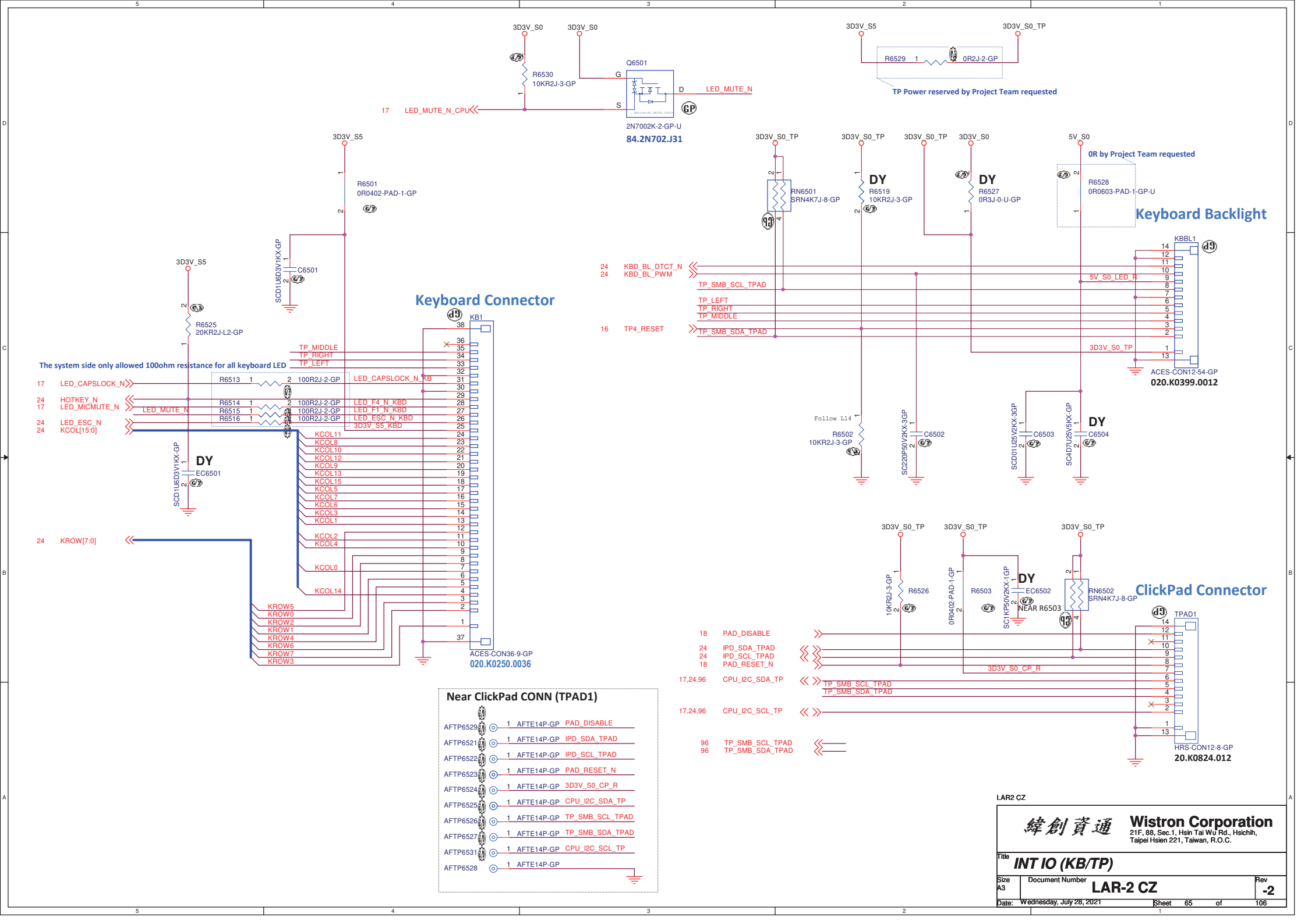
teknisi-indonesia.com

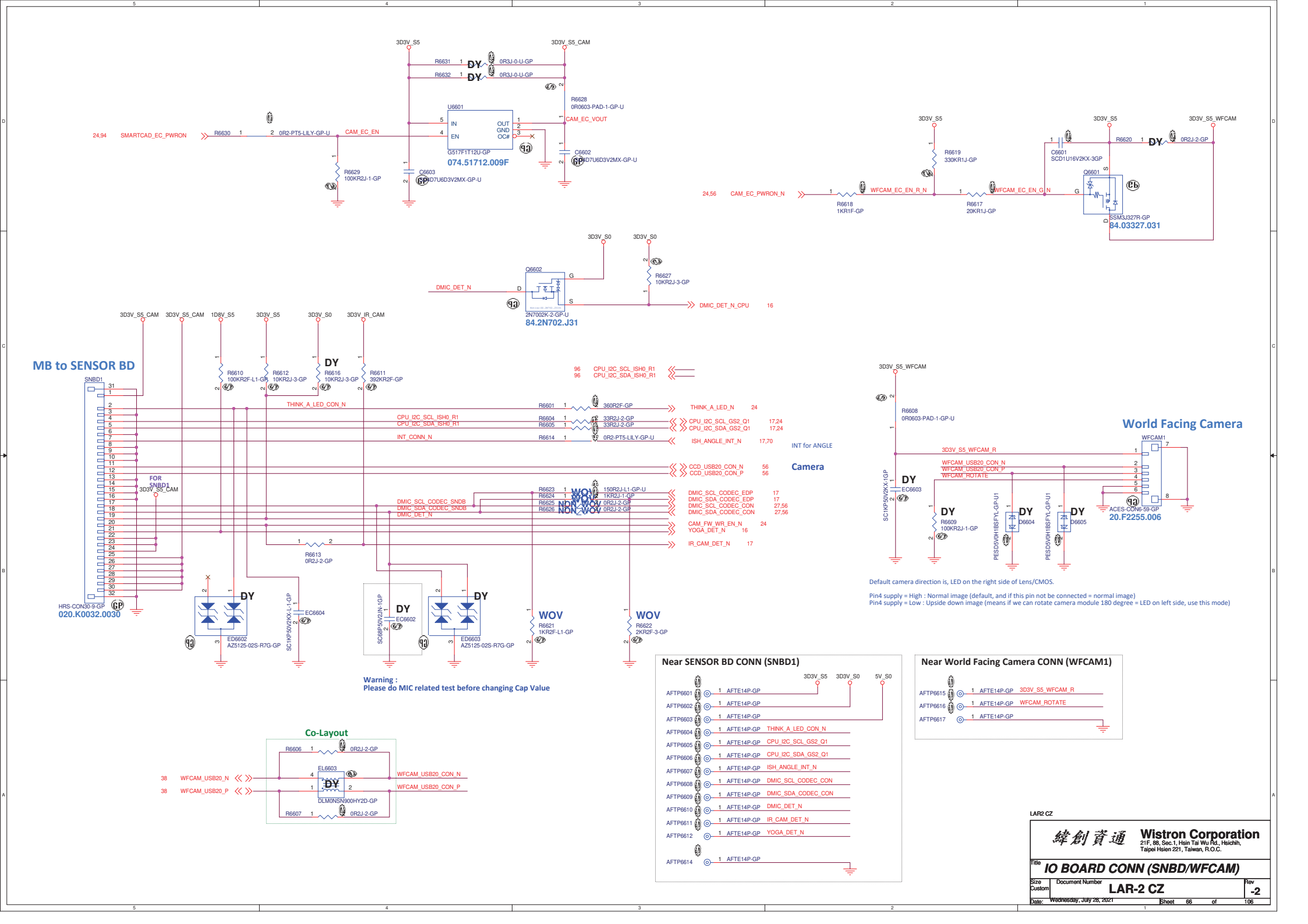
Power LED



LAR2 CZ

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LED/BTN/POWER BTN*		
Size: A4	Document Number: LAR-2 CZ	Rev: -2
Date: Wednesday, July 28, 2021	Sheet 64 of 106	


3D3V_S0
3D3V_S0
R6530
10KR2J-3-GP
Q6501
G
D
S
LED_MUTE_N
17 LED_MUTE_N_CPU
2N7002K-2-GP-U
84.2N702.J31
3D3V_S5
3D3V_S0_TP
R6529 1
0R2J-2-GP
TP Power reserved by Project Team requested
3D3V_S5
R6501
0R0402-PAD-1-GP
SCD1U6D3V1KX-GP
C6501
3D3V_S5
R6525
20KR2J-L2-GP
Keyboard Connector
KB1
The system side only allowed 100ohm resistance for all keyboard LED
17 LED_CAPSLOCK_N
24 HOTKEY_N
17 LED_MICMUTE_N
24 LED_ESC_N
24 KCOL[15:0]
R6513 1 2 100R2J-2-GP LED_CAPSLOCK_N_KB
R6514 1 2 100R2J-2-GP LED_F4_N_KBD
R6515 1 2 100R2J-2-GP LED_F1_N_KBD
R6516 1 2 100R2J-2-GP LED_ESC_N_KBD
3D3V_S5_KBD
LED_MUTE_N
TP_MIDDLE
TP_RIGHT
TP_LEFT
SCD1U6D3V1KX-GP
DY
EC6501
24 KROW[7:0]
KCOL11
KCOL8
KCOL10
KCOL12
KCOL9
KCOL13
KCOL15
KCOL5
KCOL7
KCOL6
KCOL3
KCOL1
KCOL2
KCOL4
KCOL0
KCOL14
KROW5
KROW0
KROW2
KROW1
KROW4
KROW6
KROW7
KROW3
ACES-CON36-9-GP
020.K0250.0036
3D3V_S0_TP
3D3V_S0_TP
3D3V_S0_TP
3D3V_S0
5V_S0
0R by Project Team requested
RN6501
SRN4K7J-8-GP
DY
R6519
10KR2J-3-GP
DY
R6527
0R3J-0-U-GP
R6528
0R0603-PAD-1-GP-U
Keyboard Backlight
KBBL1
24 KBD_BL_DTCT_N
24 KBD_BL_PWM
TP_SMB_SCL_TPAD
TP_LEFT
TP_RIGHT
TP_MIDDLE
16 TP4_RESET
TP_SMB_SDA_TPAD
5V_S0_LED_R
3D3V_S0_TP
ACES-CON12-54-GP
020.K0399.0012
Follow L14
R6502
10KR2J-3-GP
SC220P50V2KX-3GP
C6502
SCD01U25V2KX-3GP
C6503
DY
SC4D7U25V5KX-GP
C6504
3D3V_S0_TP
3D3V_S0_TP
3D3V_S0_TP
R6526
10KR2J-3-GP
0R0402-PAD-1-GP
R6503
DY
SC1KP50V2KX-1GP
EC6502
NEAR R6503
RN6502
SRN4K7J-8-GP
ClickPad Connector
TPAD1
18 PAD_DISABLE
24 IPD_SDA_TPAD
24 IPD_SCL_TPAD
18 PAD_RESET_N
17,24,96 CPU_I2C_SDA_TP
17,24,96 CPU_I2C_SCL_TP
96 TP_SMB_SCL_TPAD
96 TP_SMB_SDA_TPAD
3D3V_S0_CP_R
TP_SMB_SCL_TPAD
TP_SMB_SDA_TPAD
HRS-CON12-8-GP
20.K0824.012
Near ClickPad CONN (TPAD1)
AFTP6529 1 AFTE14P-GP PAD_DISABLE
AFTP6521 1 AFTE14P-GP IPD_SDA_TPAD
AFTP6522 1 AFTE14P-GP IPD_SCL_TPAD
AFTP6523 1 AFTE14P-GP PAD_RESET_N
AFTP6524 1 AFTE14P-GP 3D3V_S0_CP_R
AFTP6525 1 AFTE14P-GP CPU_I2C_SDA_TP
AFTP6526 1 AFTE14P-GP TP_SMB_SCL_TPAD
AFTP6527 1 AFTE14P-GP TP_SMB_SDA_TPAD
AFTP6531 1 AFTE14P-GP CPU_I2C_SCL_TP
AFTP6528 1 AFTE14P-GP
LAR2 CZ
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
INT IO (KB/TP)
Size A3
Document Number
LAR-2 CZ
Rev -2
Date: Wednesday, July 28, 2021
Sheet 65 of 106



LAR2 CZ

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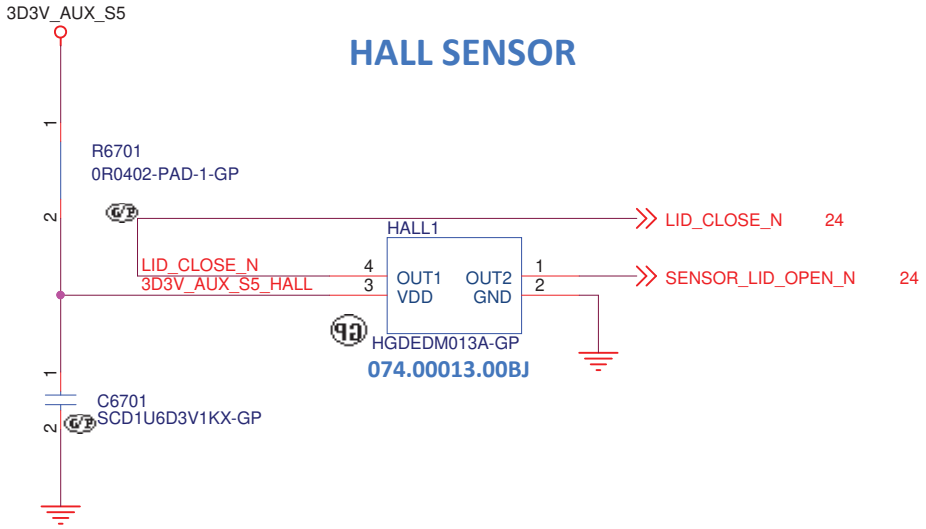
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO BOARD CONN (SNBD/WFCAM)

Size	Document Number	Rev
Custom	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 66 of 106

HALL SENSOR

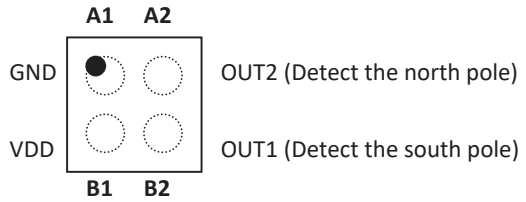


Pin1 need place at "Upper Right Corner"

LID_CLOSE_N : NB Lid function
SENSOR_LID_OPEN#: Tablet detect function

Pin Configuration

TOP VIEW (pads not visible)



BU52072GWZ-E2

LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (Hall-Sensor)***

Size	Document Number	Rev
A4	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 67 of 106

SSID = DEBUG PORT

16,24,96 LPC_AD_CPU_P0
16,24,96 LPC_AD_CPU_P1
16,24,96 LPC_AD_CPU_P2
16,24,96 LPC_AD_CPU_P3
16,24,96 LPC_FRAME_N_CPU
16,24,91 LPC_RST_N
3,56,61,63,89,91 PLT_RST_N
16 LPC_CLK_DBG
8 APU_TCK
8 APU_TMS
8 APU_TDI
8 APU_TDO
8,46 PWR_SVID_PWRGD
8,73 RST_CPU_N
8 APU_DBREQ_N
8 APU_TRST_N
24,61 E51_TXD_EC
16 EGPIO141_RX
16 EGPIO143_TX
16,24 LPC_SERIRQ_CPU
16 EC_SMI_APU

Debug Connector

Layout Note:
Place near trace separated point.

3D3V_S0

LPC_RST_N R6802 0R2-PT5-LILY-GP-U
PLT_RST_N R6803 DY 0R2J-2-GP
LPC_FRAME_N_CPU R6801 0R2-PT5-LILY-GP-U

LPC_AD_CPU_P3
LPC_AD_CPU_P2 RN6803 SRN0J-6-GP
LPC_AD_CPU_P1
LPC_AD_CPU_P0 RN6801 SRN0J-6-GP

LPC_SERIRQ_CPU
LPC_CLK_DBG
PLT_RST_N_DEBUG
LPC_FRAME_N_DEBUG
LPC_AD_CPU_P3_DEBUG
LPC_AD_CPU_P2_DEBUG
LPC_AD_CPU_P1_DEBUG
LPC_AD_CPU_P0_DEBUG
E51_TXD_EC
EC_SMI_APU
EGPIO143_TX
EGPIO141_RX

DBG1 DY ACES-CON14-11-GP
20.F1637.014

EC6801 DY SC8P50V2DN-1GP

1D8V_S5

HDT+ Connectors

HDT1 DY
Notice : ZZ.F1722.02001

1	CPU_VDDIO	CPU_TCK	2
3	GND	CPU_TMS	4
5	GND	CPU_TDI	6
7	GND	CPU_TDO	8
APU_TRST_N_R 9	CPU_TRST#	CPU_PWROK_BUF	10
DBRDY3 11	CPU_DBRDY3	CPU_RST#_BUF	12
DBRDY2 13	CPU_DBRDY2	CPU_DBRDY0	14
DBRDY1 15	CPU_DBRDY1	CPU_DBREQ#	16
17	GND	CPU_PLLTEST0	18
19	CPU_VDDIO	CPU_PLLTEST1	20

SMC-CONN20A-1-GP-U3
20.F1722.020

APU_TCK
APU_TMS
APU_TDI
APU_TDO
PWR_SVID_PWRGD_CON
RST_N_CPU_CON

APU_DBREQ_N_CON R6807 HDT 33R2J-L1-GP APU_DBREQ_N
C6802 CD01U25V2KX-3GP HDT

RN6802 HDT SRN10KJ-6-GP
DBRDY1
DBRDY2
DBRDY3

20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001

DBG1: EVT stage要上

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.
20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

1D8V_S5
R6805 HDT 300R2J-4-GP RST_N_CPU_CON
R6806 HDT 300R2J-4-GP PWR_SVID_PWRGD_CON
LAR2 CZ

APU_TRST_N R6804 HDT APU_TRST_N_R 33R2J-2-GP
C6801 CD01U25V2KX-3GP HDT

1D8V_S5
U6801 HDT
PWR_SVID_PWRGD
RST_CPU_N
PWR_SVID_PWRGD_CON
RST_N_CPU_CON
NC7WV07P6X-GP
73.7WV07.00J

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC/HDT)
Size: A4
Document Number: LAR-2 CZ
Rev: -2
Date: Wednesday, July 28, 2021
Sheet 68 of 106

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LAR2 CZ

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title ***Sensor (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

Date: Wednesday, July 28, 2021 Sheet 69 of 106

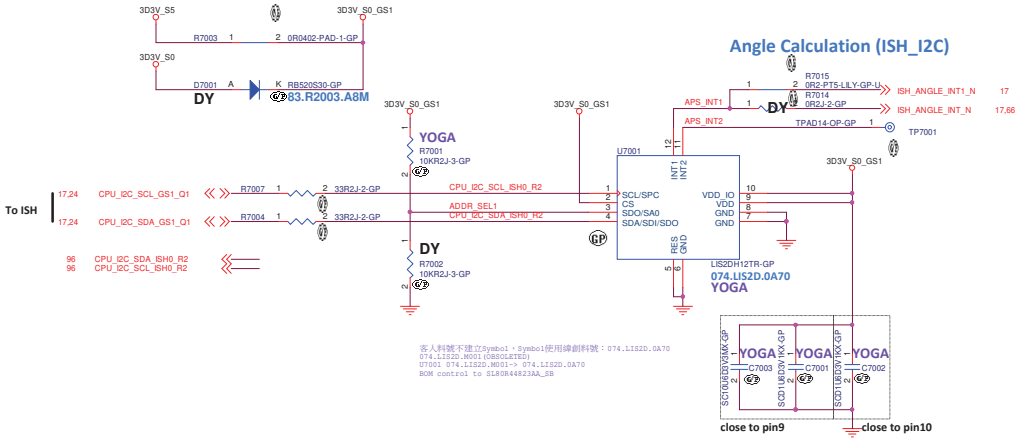


TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address (7bit)
ST LIS2DH12TR	H	19h (7bit)
	L	18h (7bit)

← LOGIC (MB) (SENSOR BD)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← LOGIC

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N	
ST	LIS2DH12TR	074.LIS2D.M001	SL80R44823AA

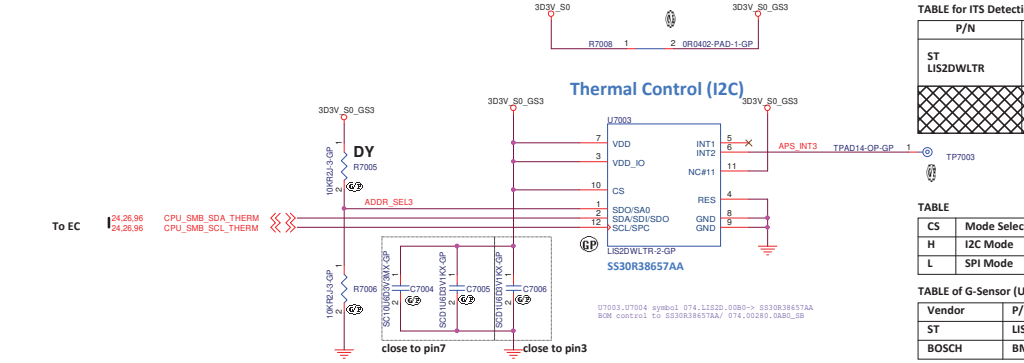


TABLE for ITS Detection (U7003): Tri-axis Digital Accelerometer

P/N	ADDR_SEL3	Address (8bit)
ST LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

← LOGIC

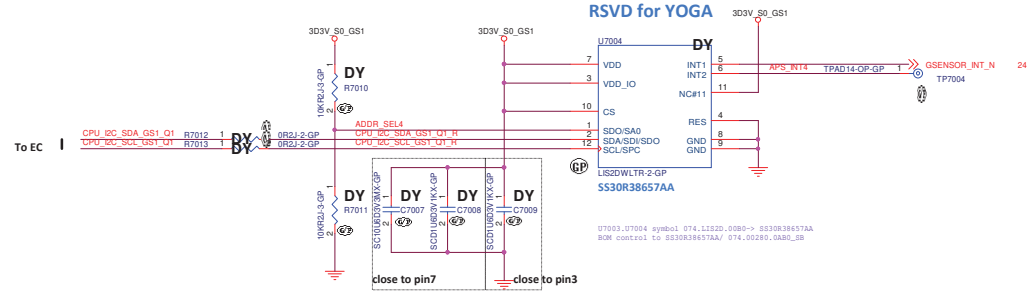
TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← LOGIC

TABLE of G-Sensor (U7003)

Vendor	P/N	Wistron P/N	
ST	LIS2DWLTR	074.LIS2D.00B0	SS30R38657AA
BOSCH	BMA280	074.00280.0AB0	SS30W75630AA Use it at EC side only



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← LOGIC

TABLE of G-Sensor (U7004)

Vendor	P/N	Wistron P/N	
ST	LIS2DWLTR	074.LIS2D.00B0	SS30R38657AA
BOSCH	BMA280	074.00280.0AB0	SS30W75630AA Use it at EC side only

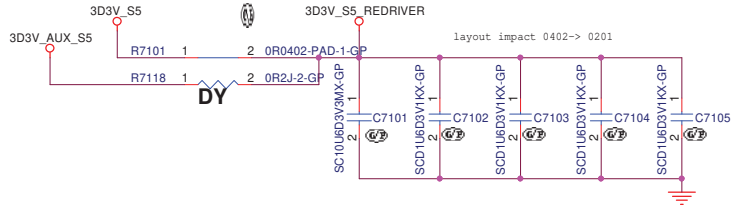
LAR2 CZ

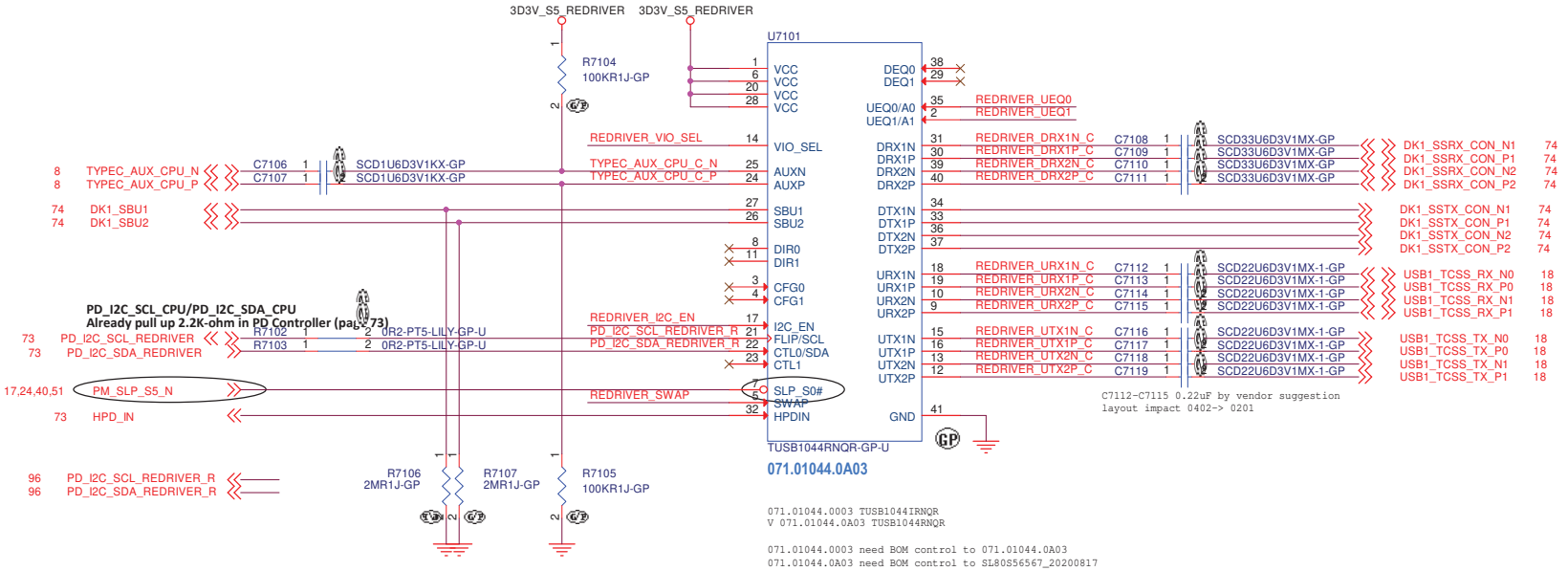
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR (G-SENSOR)

Size: A2 | Document Number: LAR-2 CZ | Rev: -2

Date: Wednesday, July 28, 2021 | Sheet 70 of 106



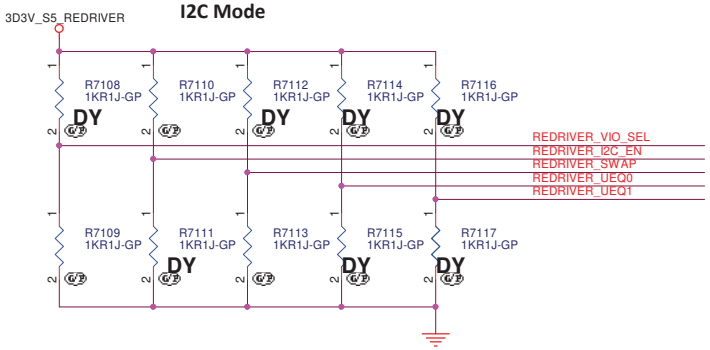


071.01044.0003 TUSB1044IRNQR
V 071.01044.0A03 TUSB1044RNQR

071.01044.0003 need BOM control to 071.01044.0A03
071.01044.0A03 need BOM control to SL80S56567_20200817

To TYPEC USB3

HOST (From CPU)



I2C_EN: 1=I2C enabled
VIO_SEL: 0 = 3.3-V configuration I/O voltage, 3.3-V I 2C interface (Default)
SWAP: 0 - Do not swap channel directions and EQ settings (Default)
UEQ0/A0 and UEQ1/A1:FF

LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THUNDERBOLT RE TIMER(1/2)

Size	Document Number	Rev
A3	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 71 of 106

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LAR2 CZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***THUNDERBOLT RE TIMER(2/2)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	**-2**

Date: Wednesday, July 28, 2021 Sheet 72 of 106

083.20F30.008H->83.R2004.G8F_EVT_20201028 HT limit
HT limit location D7302 83.R2004.G8F

D7301,D7302	Part Number	Vendor Part Number
Main source	083.20F30.008H	ONSEMI NSR20F30NXT5G
2nd source	083.20301.008F	VISHAY VSKY20301608

TABLE BUSPOWER Configuration - ADCIN1 DVI = R2/(R1+R2)				
SPI_MISO	DIV MIN	DIV MAX	Dead_Battery	Default_Config
1	0	0.18	BP_NoRespones	SAFE
1	0.2	0.28	BP_WaitFor3V3_Internal	SAFE
1	0.3	0.38	BP_ECWait_Internal	(Infinitely wait for patch) ==>SAFE
1	0.4	0.48	BP_WaitFor3V3_External	SAFE
1	0.5	0.58	BP_ECWait_Internal	(Infinitely wait for patch) ==>SAFE
1	0.6	1	BP_NoWait (No Switch is closed)	SAFE
0	0	0.08	BP_NoResponse(85 Device)	0
0	0.1	0.18	BP_NoRespone	1
0	0.2	0.28	BP_NoWait	2
0	0.3	0.38	BP_ECWait_Internal	(Infinitely wait for patch until it PTCc)]==>SAFE
0	0.4	0.48	BP_NoWait	3
0	0.5	0.58	BP_ECWait_Internal	(Infinitely wait for patch until it PTCc)]==>SAFE
0	0.6	0.68	BP_NoWait	4
0	0.7	0.78	RSVD	RSVD
0	0.8	0.88	RSVD	RSVD
0	0.9	1.0	BP_NoWait	5

LOGIC

BUSPOWER Config.
BP_NoWait

HT limit location C7305

Please add pull down resistor, avoid floating status (HPD)

USB_OC0_N, USB_OC1_N
why need to connect to PD controller?

TABLE I2C Addressing - ADCIN2

I2C1 (to EC)	TYPE-C PORT A	0X46/0X47
	TYPE-C PORT B	0X4E/0X4F
I2C2 (to CPU)	TYPE-C PORT A	0X70/0X71
	TYPE-C PORT B	0X7E/0X7F

Place to TOP side

083.00520.0D8F change to 83.R2003.A8M
EVT verify

Add SPI ROM for SPI less architecture risk mitigation. 32kB is required at minimum.

1MB(8Mb) 150MIL SOIC 8PIN
WINBOND W25Q80DVSNIG
072.25Q80.0K01/ 072.25806.0D01
-> 072.25Q80.0A01_SA
W25Q80DVSSIG

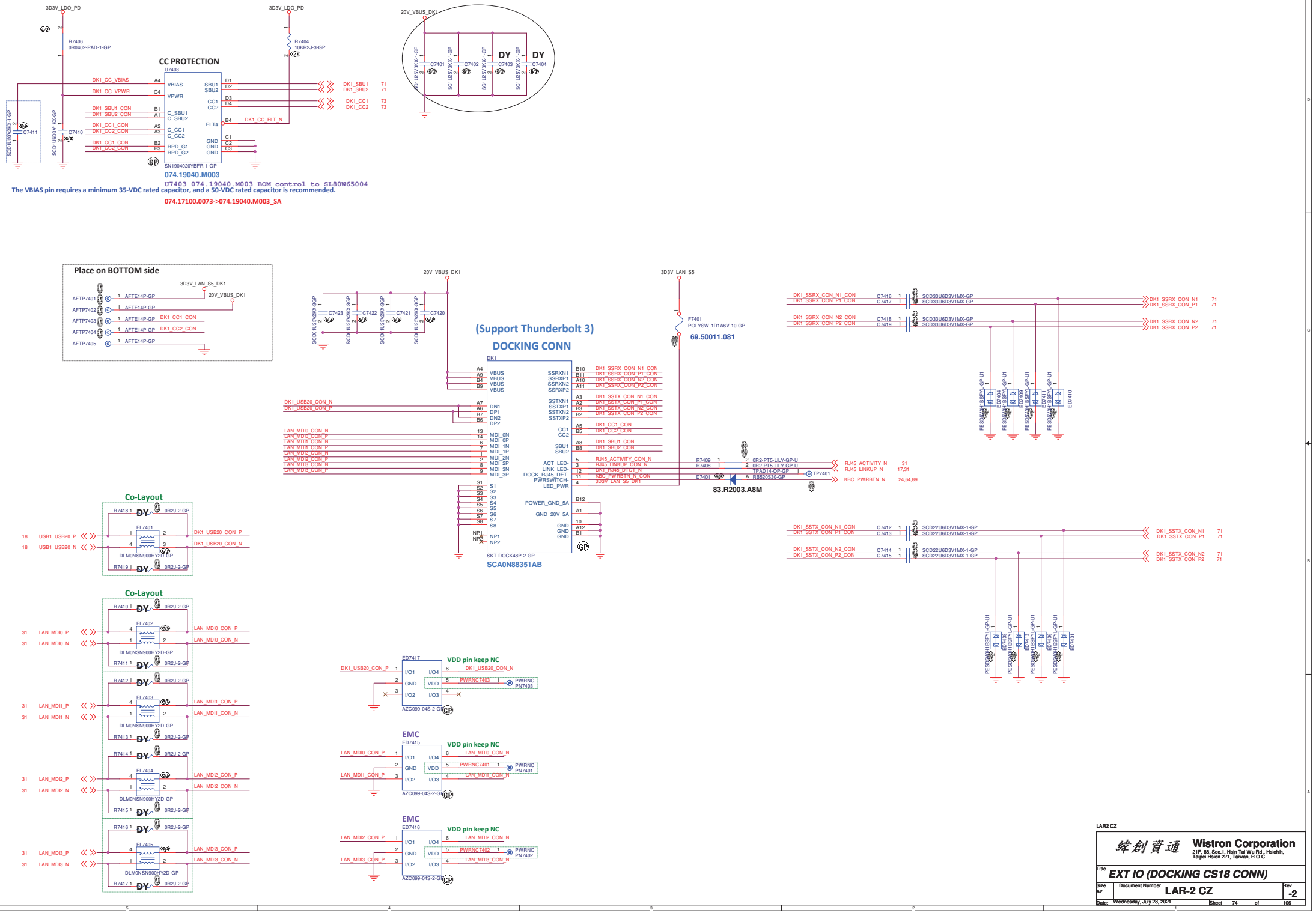
LAR2 CZ

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC PD TPS65988DJ)

Size	Document Number	Rev
A2	LAR-2 CZ	-2

Date: Wednesday, July 28, 2021 Sheet 73 of 106



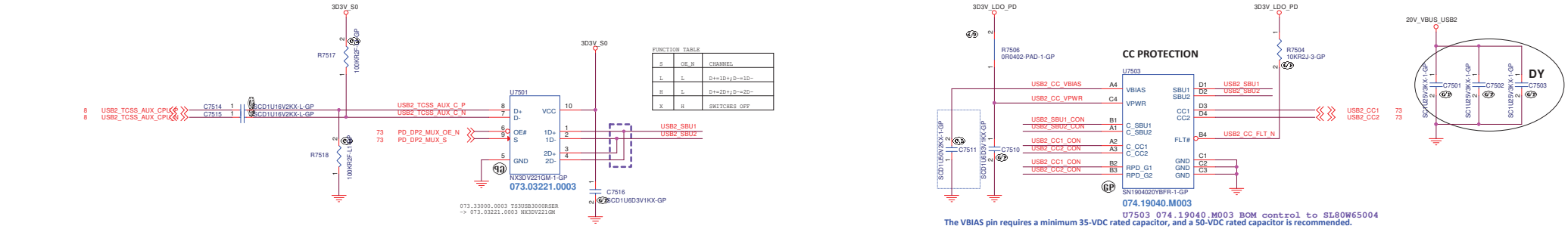
LAR2 CZ

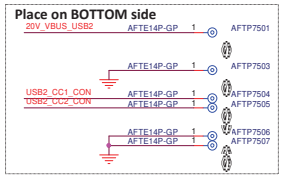
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

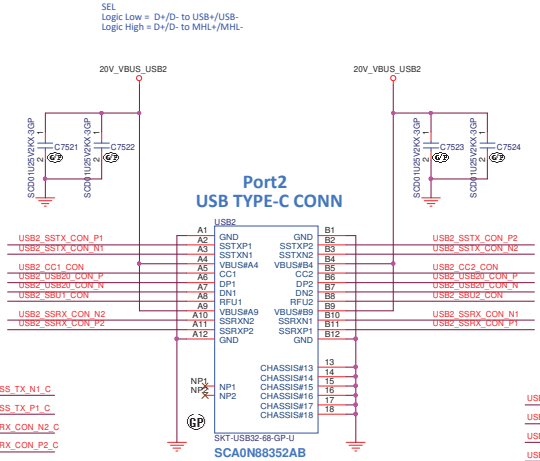
Title: **EXT IO (DOCKING CS18 CONN)**

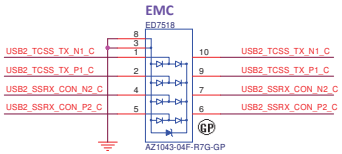
Size	Document Number	Rev
A2	LAR-2 CZ	-2

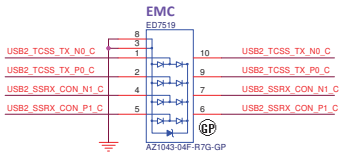
Date: Wednesday, July 28, 2021 Sheet 74 of 106

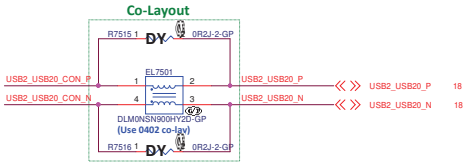


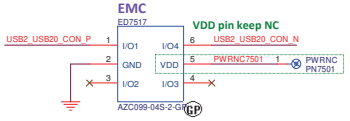


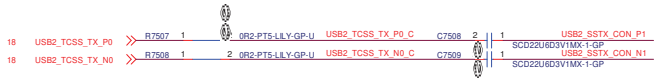


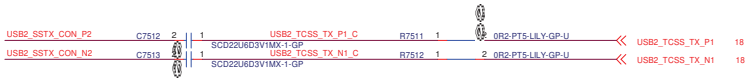


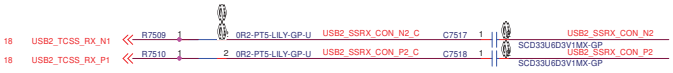


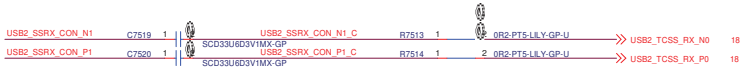












LAR2 CZ

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC CONN)

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Title: ***GPU (RSVD)***

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Title ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: GPU (RSVD)

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title ***GPU (RSVD)***

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Title: *GPU (RSVD)*		
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Title: *GPU (RSVD)*

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Title: ***GPU (RSVD)***

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EMI Spring

SPR1
SPRING-64-GP
34.4H602.001

Stand Off

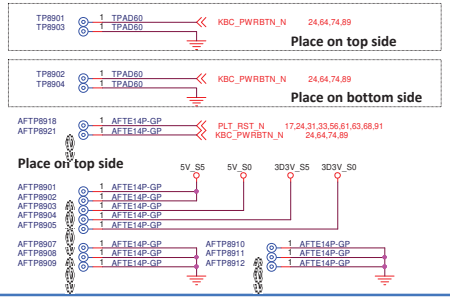
HS1
STFT236B142R128H43-1-GP
34.4EO02.001

HS2
STFT236B142R128H43-1-GP
34.4EO02.001

Screw Pad

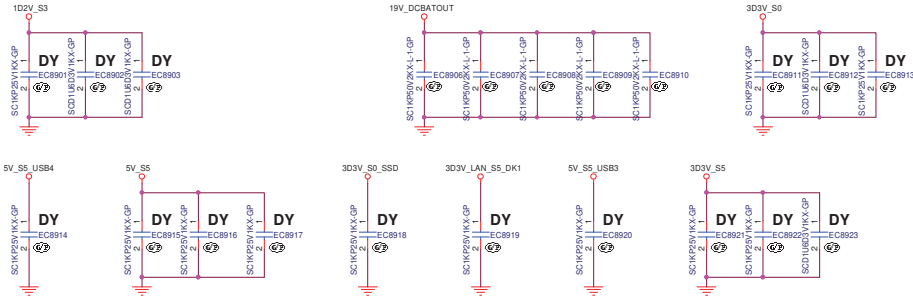
H1 HOLE233R150-GP ZZ.00PAD.WN1
H2 HOLE233R150-GP ZZ.00PAD.WN1
H3 HOLE233R150-GP ZZ.00PAD.WN1
H4 HOLE233R150-GP ZZ.00PAD.WN1
H6 HOLE276R119-GP ZZ.PAD02.071
H7 HOLE276R119-GP ZZ.PAD02.071
H8 HOLE237R103-GP ZZ.00PAD.EJ1
H10 HOLE276R119-GP ZZ.PAD02.071
H11 HOLE276R119-GP ZZ.PAD02.071
H12 HOLE237R103-GP ZZ.00PAD.EJ1
H13 HOLE276R119-GP ZZ.PAD02.071
H14 HOLE237R103-GP ZZ.00PAD.EJ1

Test Point



RF CAPs

EMI CAPs



LAR2 CZ

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Title: UNUSED PARTS (ME/RF/EMI)

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Title: ***INT IO (RSVD)***

Size	Document Number	Rev
A4	**LAR-2 CZ**	-2

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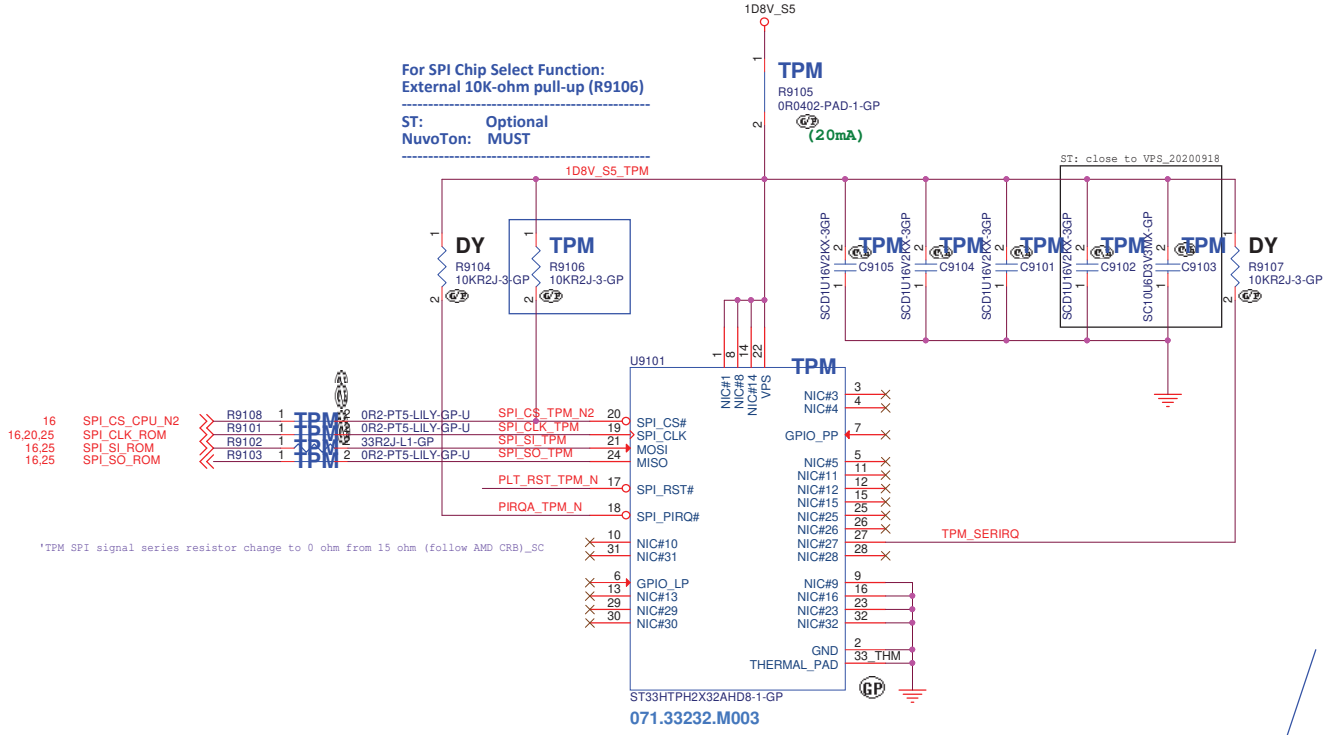


SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

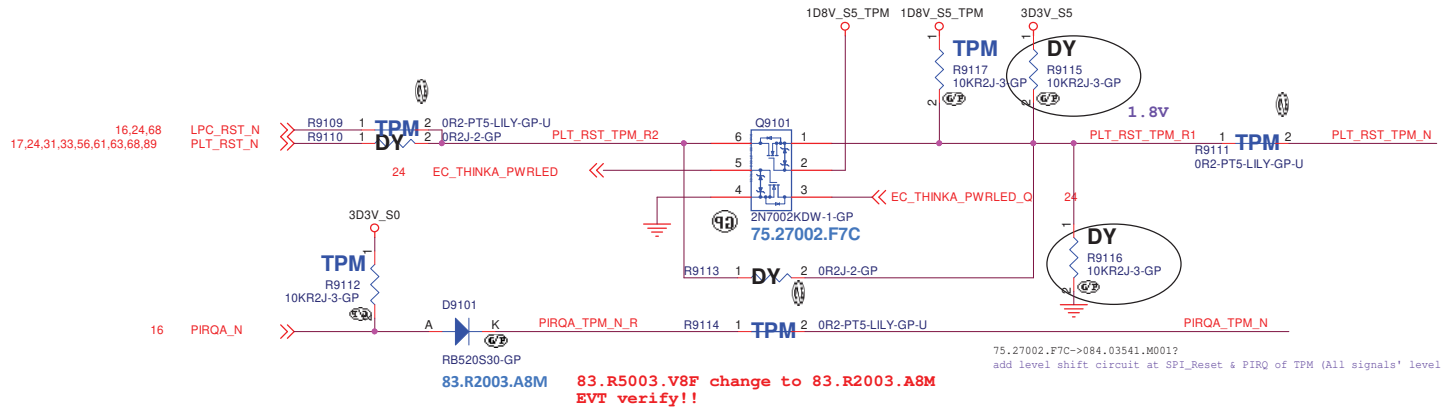
TPM TABLE

1st	ST33HTPH2X32AHD8	071.33232.M003	SL81A16618AA
2nd	NPCT750LADYX	071.00750.0H03	SL80W59122AA

Nuvoton TPM FW: 7.2.1.0 part will be dropped, and instead by new one_20200603
NuvoTon PNLenovo PNTPM FW
NPCT750LADYXSL80W591227.2.2.0
NPCT750LABYXSL80R401587.2.1.0

TABLE 071.33232.M003 071.00750.0H03 ~~071.09670.0I03~~

Pin No	TCG PTP Spec(V38)	ST ST33HTPH2X32AHD8	NuvoTon NPCT750LADYX	Infineon SLB9670VQ2.0 FW7.63
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	NC	NC	NC	NC
4	GPIO	NC	GPIO/PP	NC
5	NC	NC	NC	NC
6	GPIO	GPIO_LP	GPIO3	GPIO
7	GPIO	GPIO_PP	NC	PP
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	NC
30	SDA/GPIO0	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND



83.R2003.A8M **83.R5003.V8F change to 83.R2003.A8M EVT verify!!**

75.27002.F7C->084.03541.M001?
add level shift circuit at SPI_Reset & PIRQ of TPM (All signals' level followed 1.8v) _-1

LAR2 CZ

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Title: **INT IO (TPM)**

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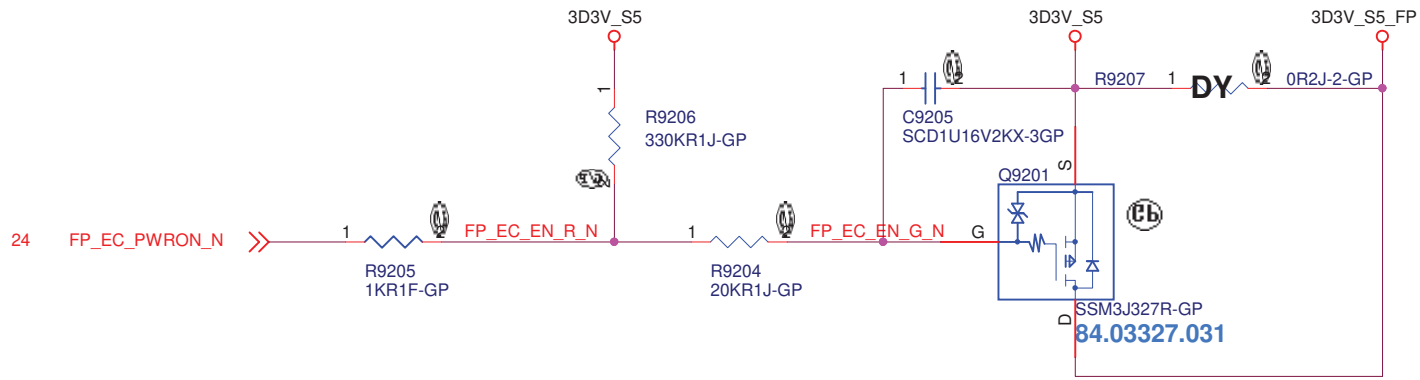

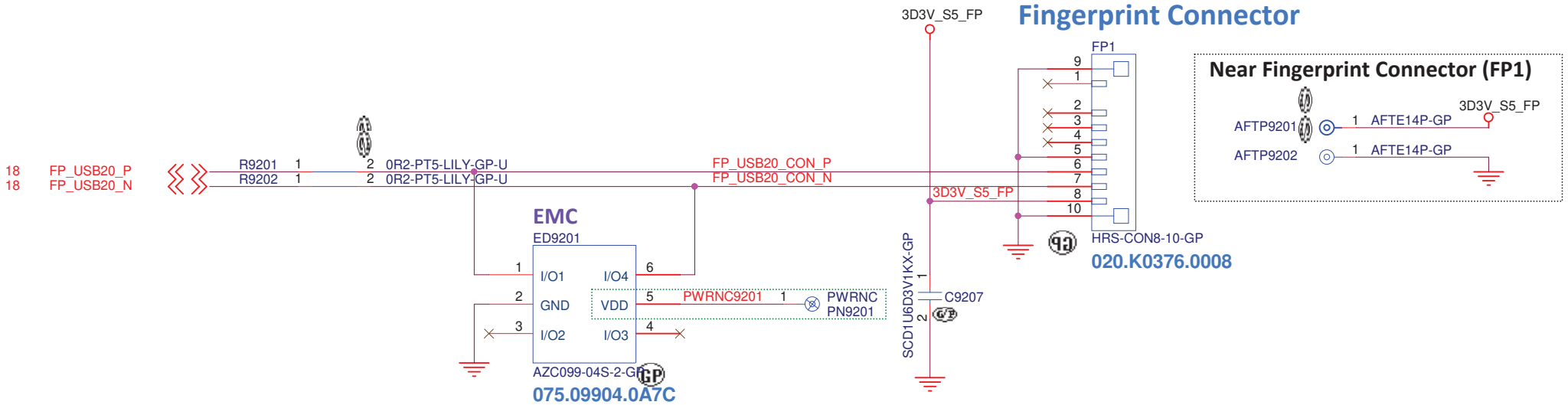

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Title: **INT IO (FINGERPRINT)**

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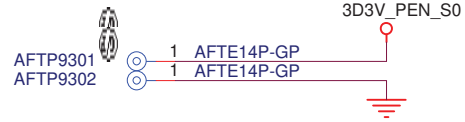
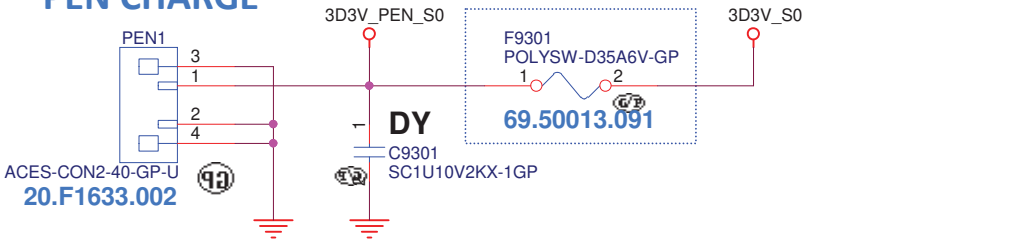
Near PEN CHARGE (PEN1)



PEN CHARGE

MUST use POLYSW, not FUSE, ThinkPad common requirement



LAR2 CZ

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *EXT IO (ACTIVE PEN)*		
Size: A4	Document Number: **LAR-2 CZ**	Rev: **-2**
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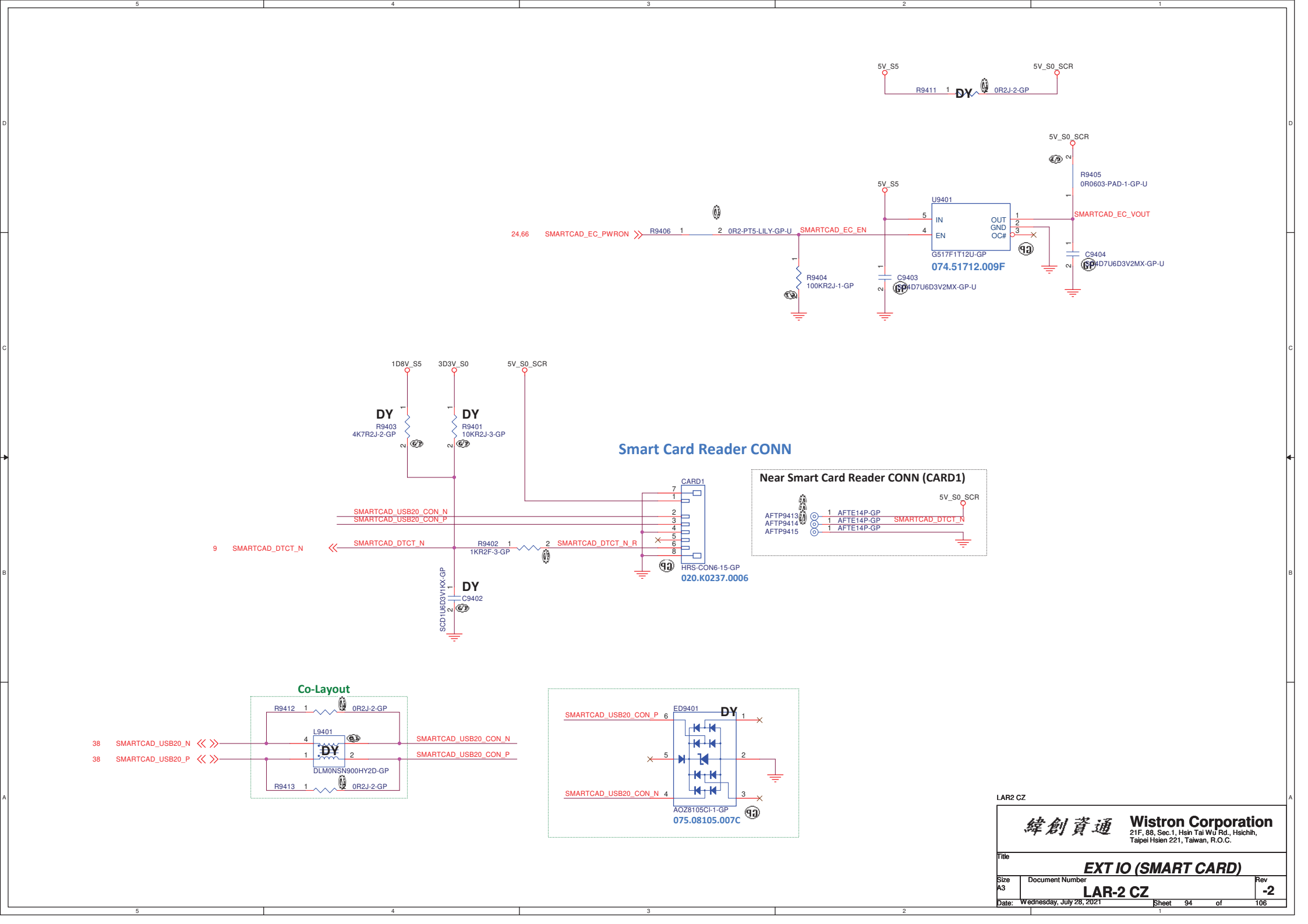

LAR2 CZ

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Title: ***EXT IO (SMART CARD)***

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Title ***EXT IO (RSVD)***

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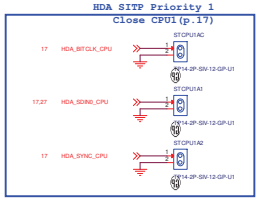
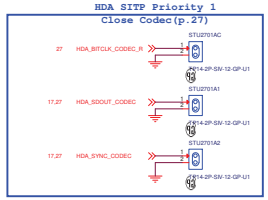
SITP DSN Template for 203088_LAR2

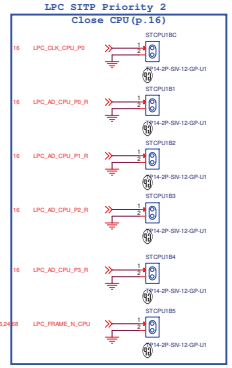
HDA SITP Priority 1
Close CPU1(p.17)



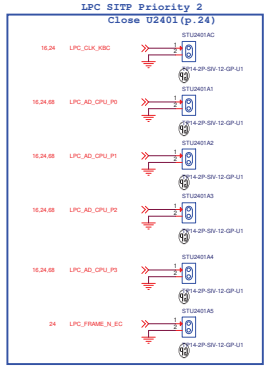
HDA SITP Priority 1
Close Codec(p.27)



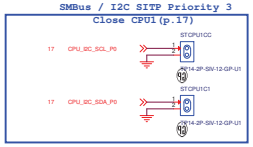
LPC SITP Priority 2
Close CPU(p.16)



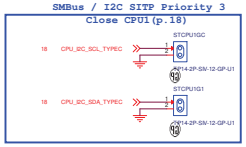
LPC SITP Priority 2
Close U2401(p.24)



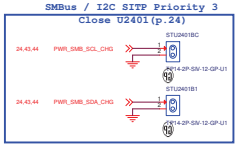
SMBus / I2C SITP Priority 3
Close CPU1(p.17)



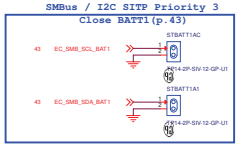
SMBus / I2C SITP Priority 3
Close CPU1(p.18)



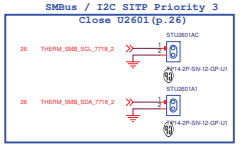
SMBus / I2C SITP Priority 3
Close U2401(p.24)



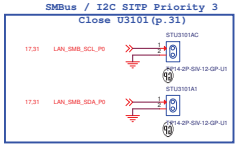
SMBus / I2C SITP Priority 3
Close BATT1(p.43)



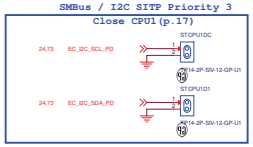
SMBus / I2C SITP Priority 3
Close U2601(p.26)



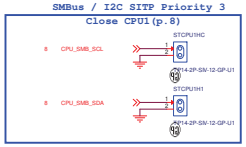
SMBus / I2C SITP Priority 3
Close U3101(p.31)



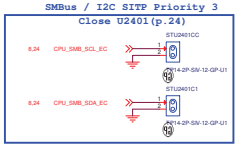
SMBus / I2C SITP Priority 3
Close CPU1(p.17)



SMBus / I2C SITP Priority 3
Close CPU1(p.8)



SMBus / I2C SITP Priority 3
Close U2401(p.24)



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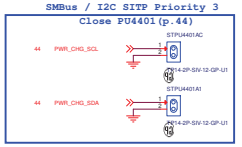
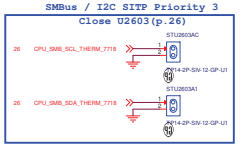
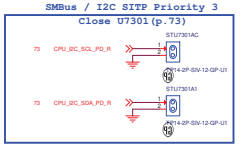
Close PU4401(p.44)



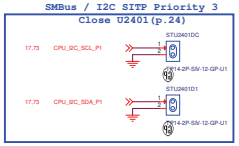
SMBus / I2C SITP Priority 3
Close U2603(p.26)



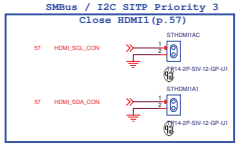
SMBus / I2C SITP Priority 3
Close U7301(p.73)



SMBus / I2C SITP Priority 3
Close U2401(p.24)



SMBus / I2C SITP Priority 3
Close HDMI1(p.57)



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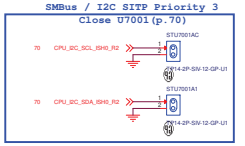

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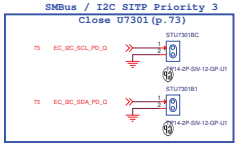

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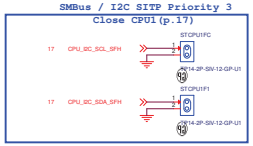

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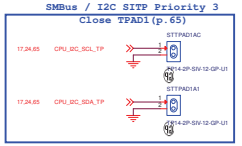

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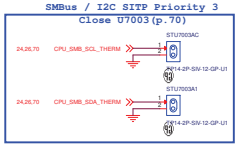

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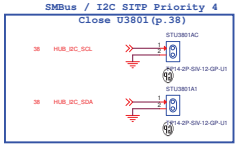

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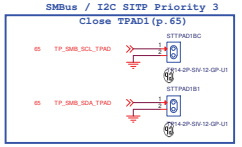

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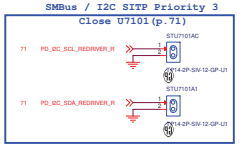

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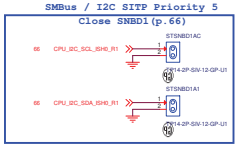

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Title: ***Power Sequence***

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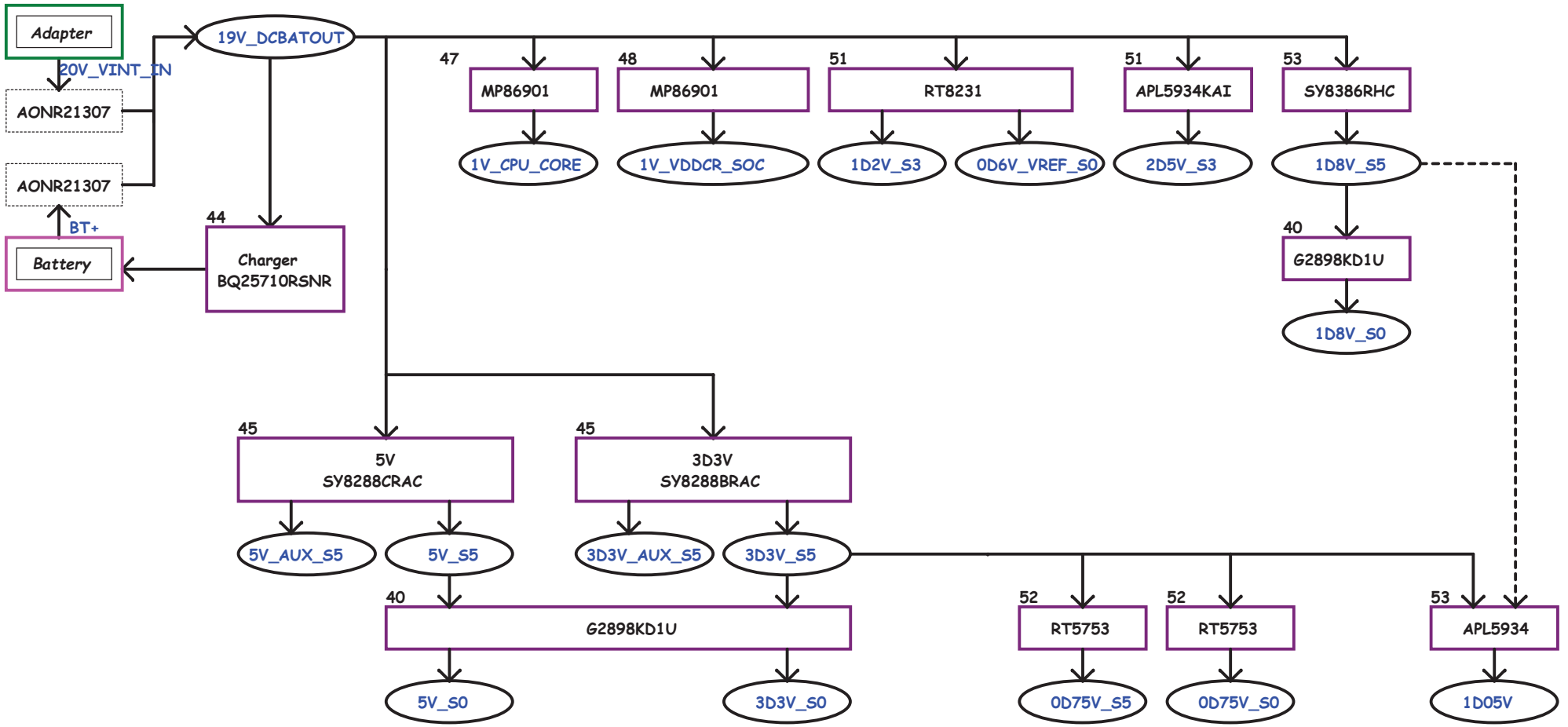

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Title: ***Power Block Diagram***

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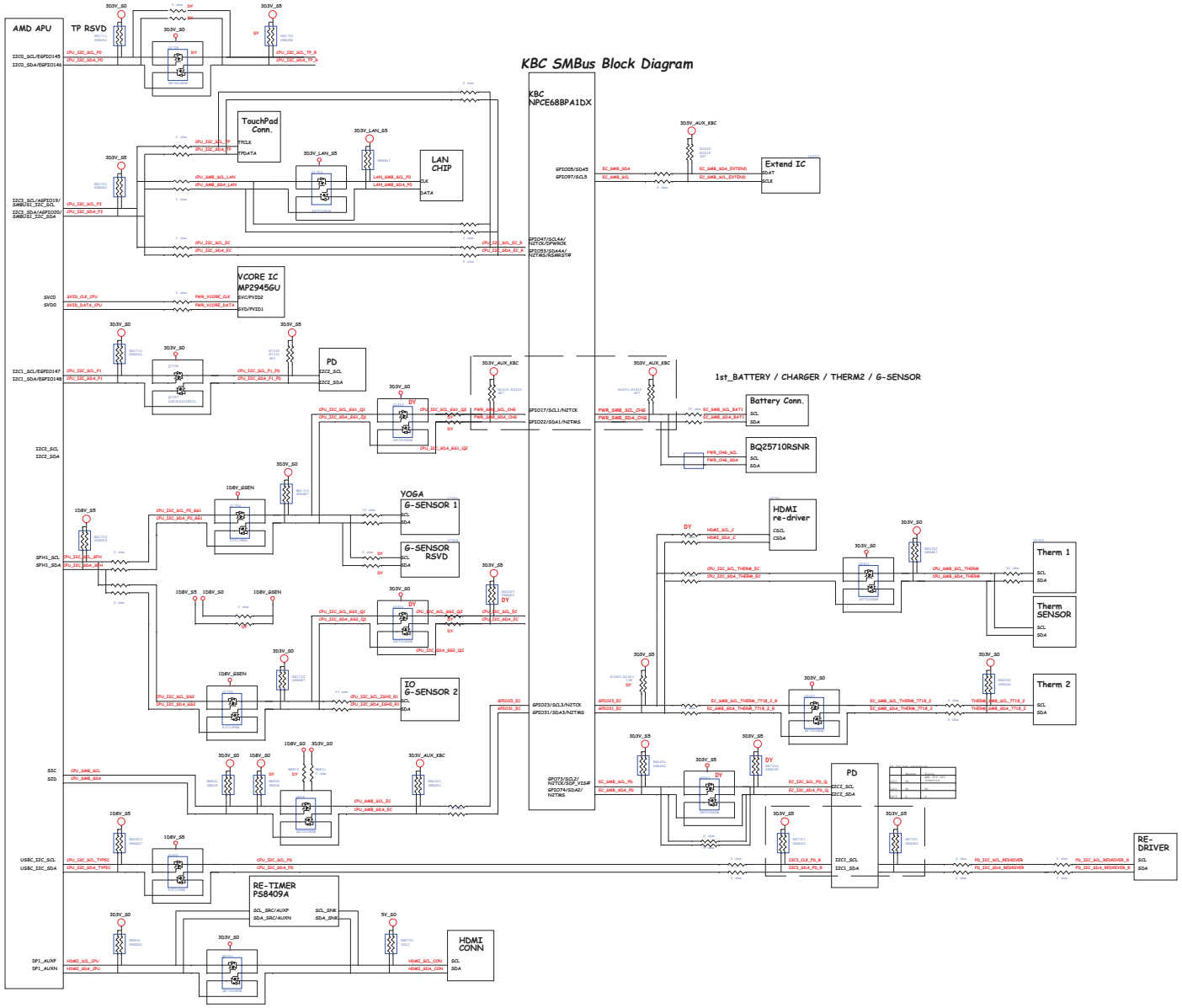
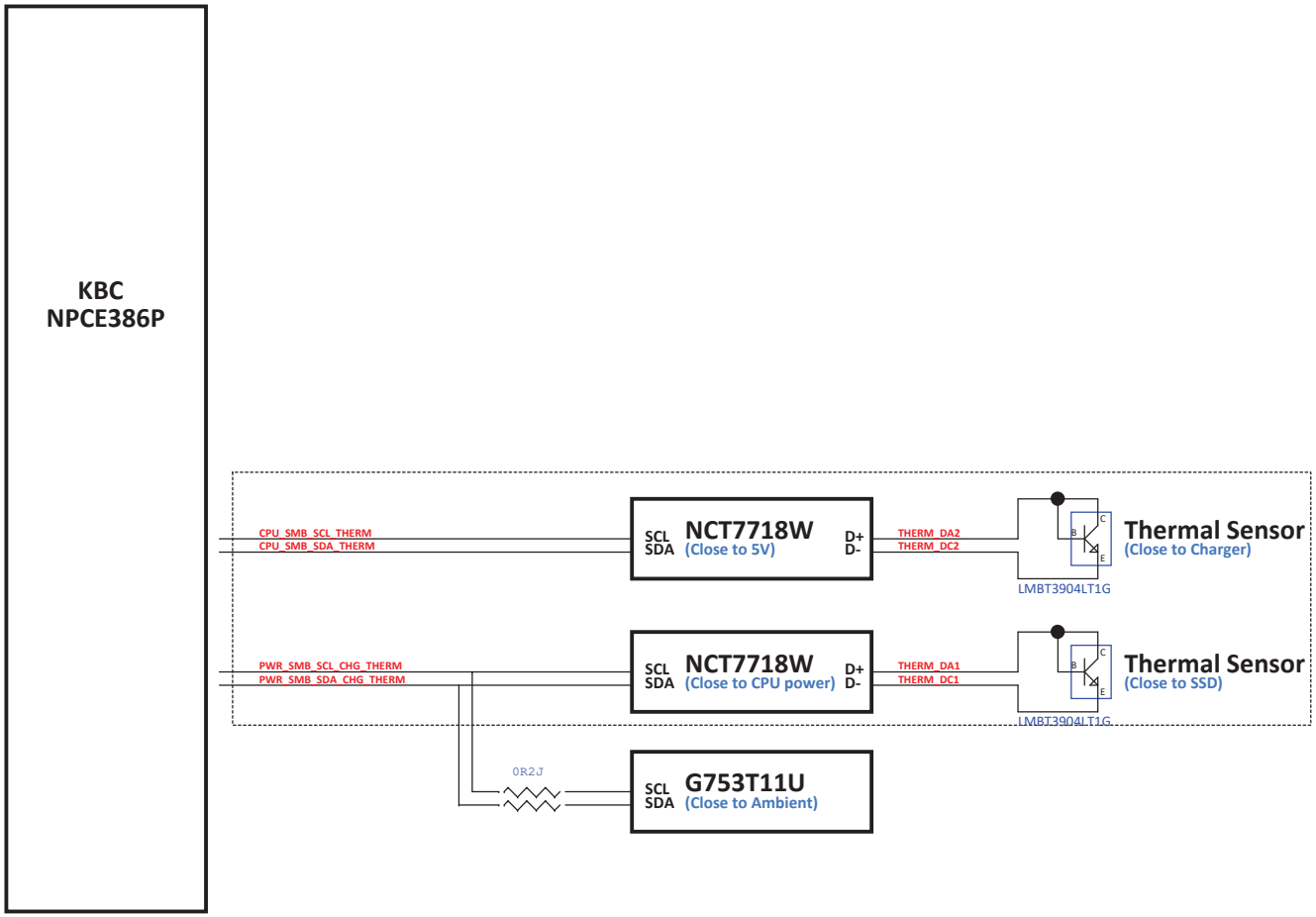
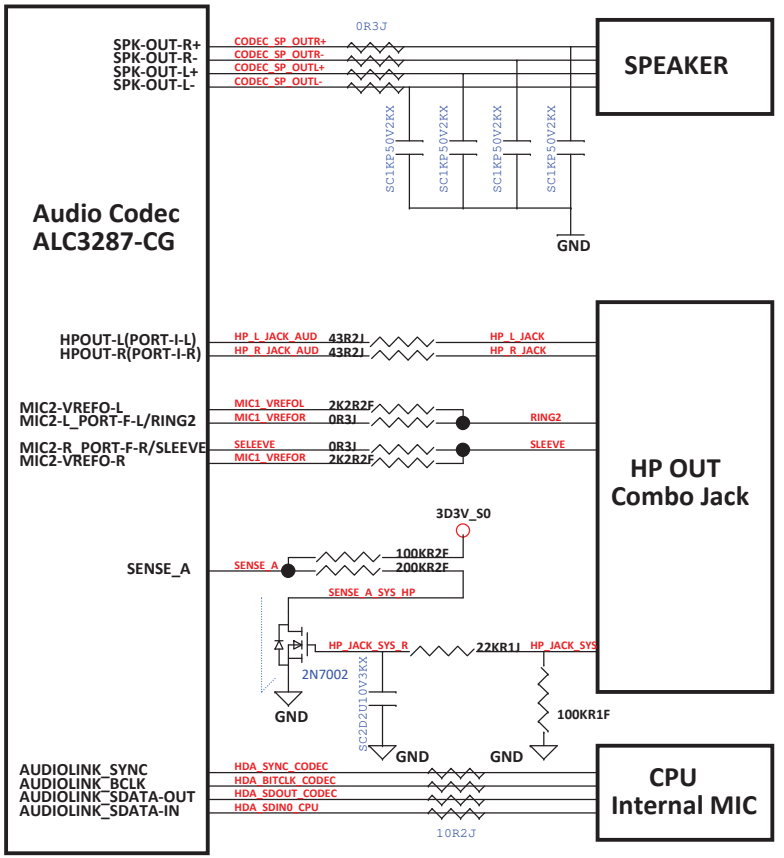
APU SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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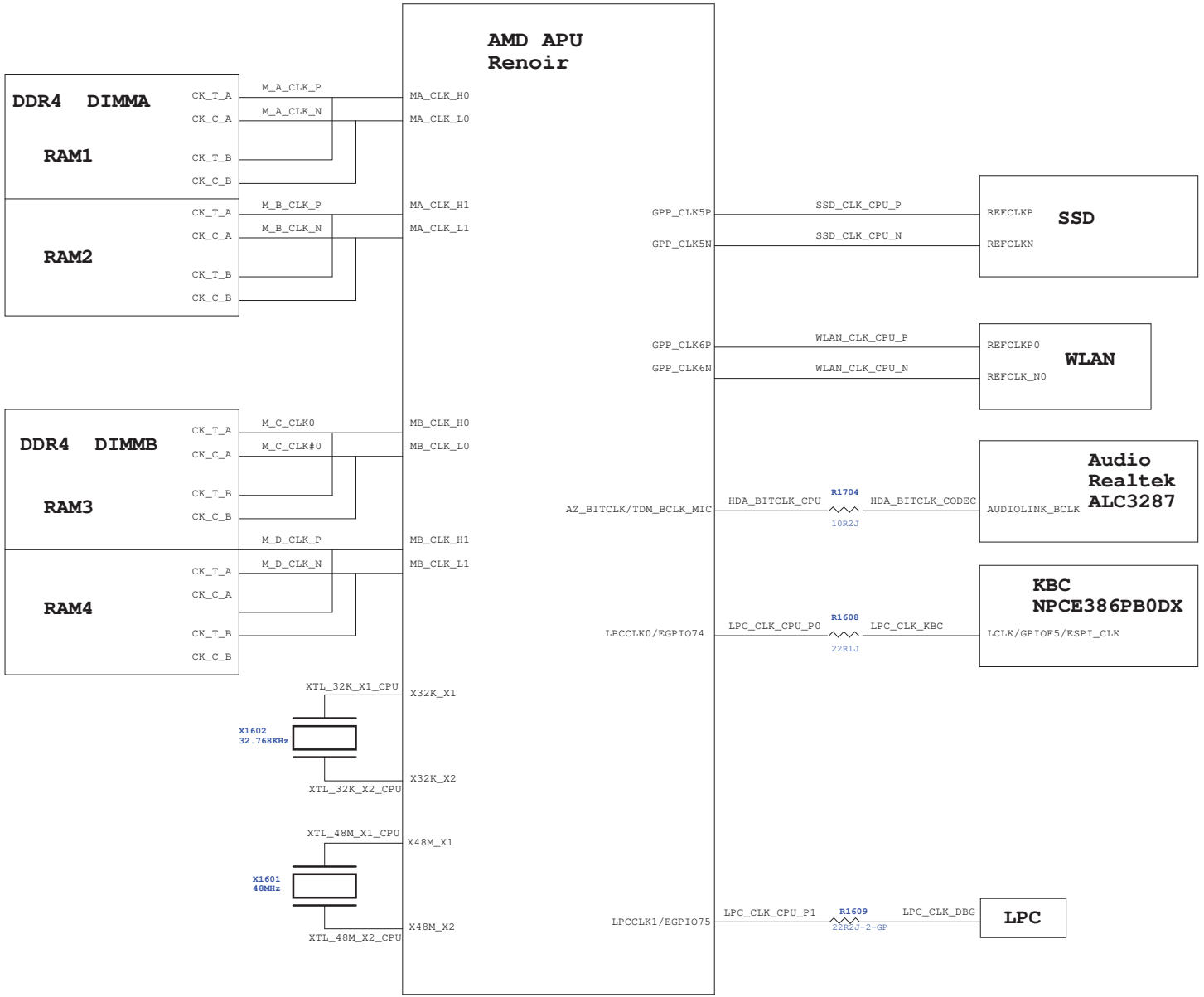
CLK Block Diagram



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Title: CLK Block

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