NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

ALPHARD

2018.12.27

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
FILE NAME			
PCB P/N	60.xxxxx.xxxx	PCB VER	XXX

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
	MAIN BOARD

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 1 of 139

TABLE OF CONTENTS

SMALL BOARD1&2

SMALL BOARD3

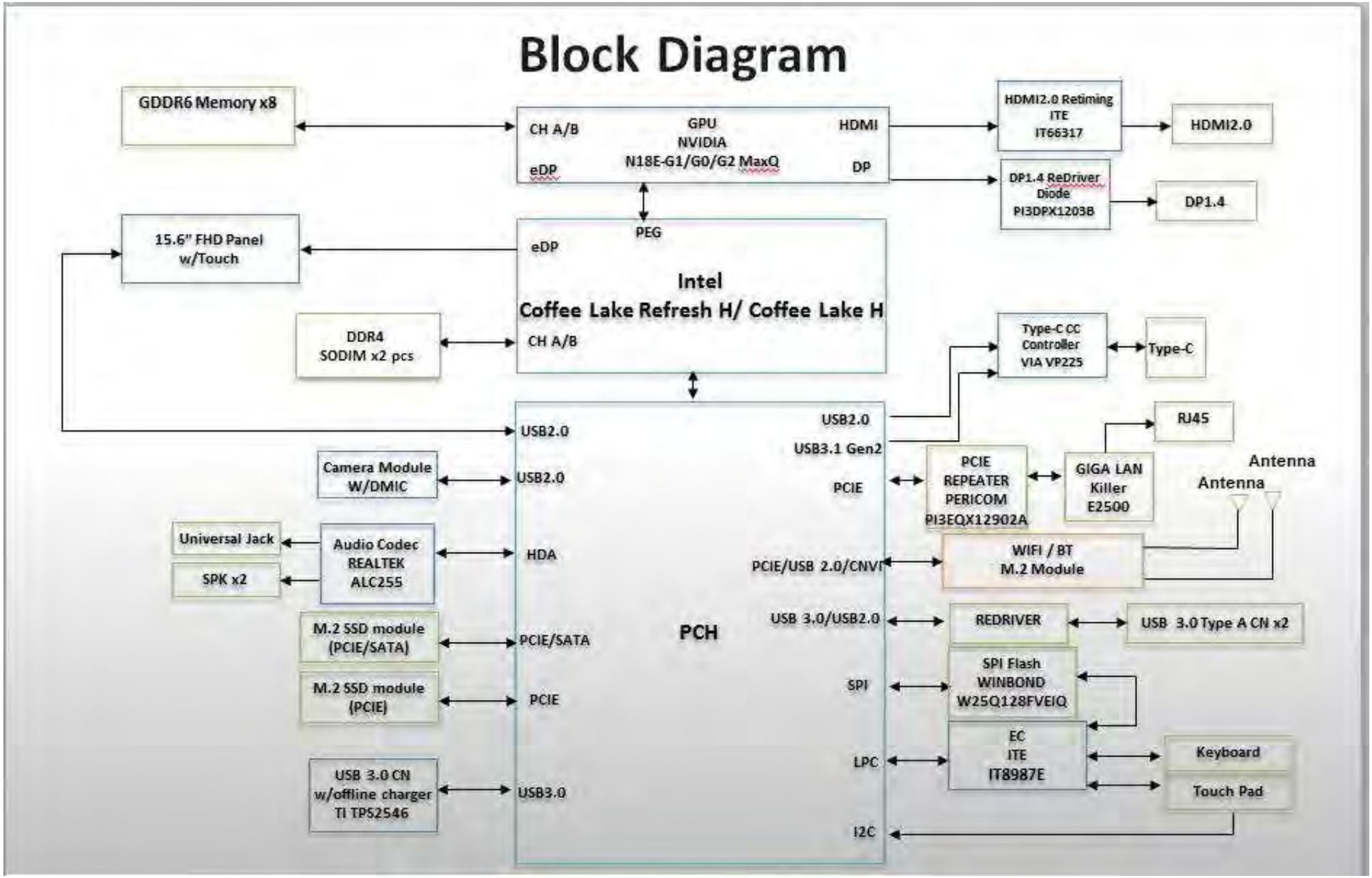
FOR 17 SMALL BOARD1&2

GPU PAGE 71-116 FROM PAGE 72

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION TABLE OF THE CONTENT		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 2 of 139	
PCB P/N 60xxxxxxxxx	PCB VER XXX		

Block Diagram



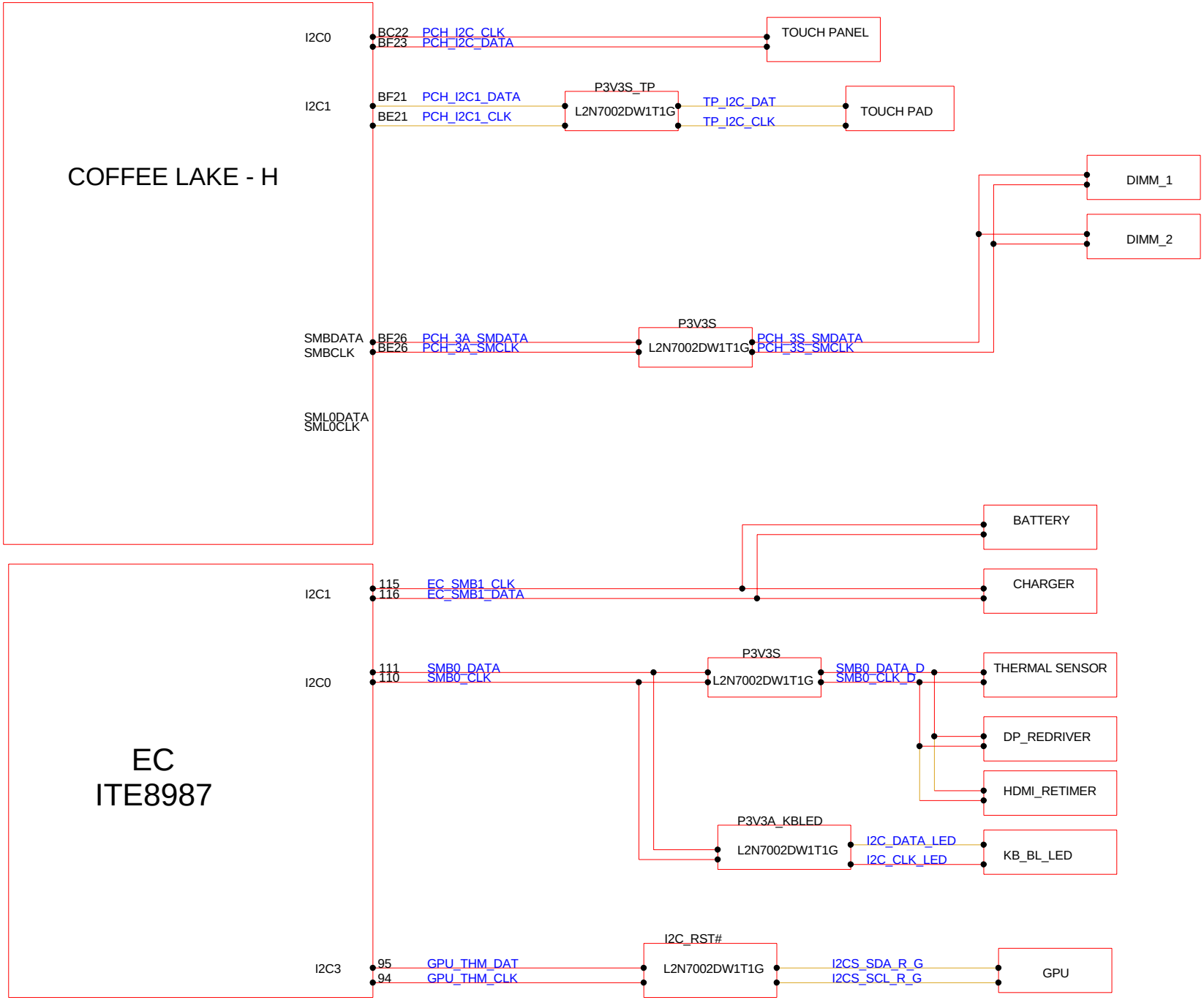
INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 3 of 139



https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

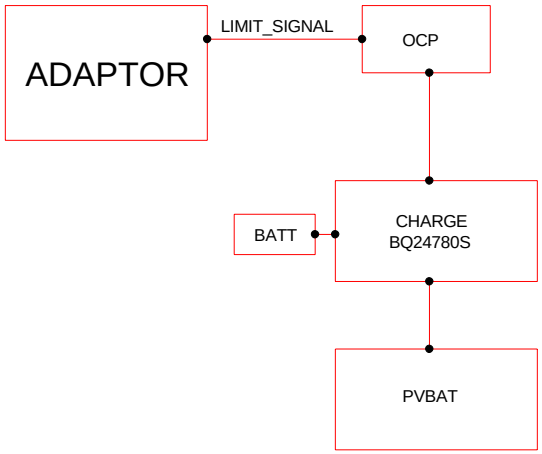
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 4 of 139

POWER BLOCK



IN/EN		OUT
PVBAT, EN_5V	SY8288CRAC	P5V0DS
PVBAT, EN_5V0	SY8284CRAC	P5V0
PVBAT, EN_3V	NB680AGD	P3V3DS
PVBAT, EN_VDDQ, EN_VTT	NB685AGQ	P1V2, P0V6S
PVBAT, EN_1V05V	SY8288CRAC	P1V05A
PVBAT, EN_VCCIO	NB681GD	PVCCIO
PVBAT, EN_PVCORE	NCP81215MNTXG	PVCORE
PVBAT, VRACPU_DRVON	NCP81151MNTBG	PVCCGT
PVBAT, VRACPU_DRVON	NCP81253MNTBG	PVCCSA

IN/EN		OUT
P5V0DS, EN_2V5	RT8097ALGE	P2V5
P3V3DS, EN_1V8	SY8088AAC	P1V8A
P3V3DS, P3V3A_5A_PWEN, CORE_PWEN	APL3523A	P3V3A, P3V3S
P5V0DS, CORE_PWEN, P1V8A, CORE_PWEN	APL3523A	P5V0S, P1V8S
P1V2, VCCPLL_OC_EN	PM514BA	VCCPLL_OC
P1V05A, RESUME_PWEN, CORE_PWEN	APL3523A	PVCCSTG, PVCCST

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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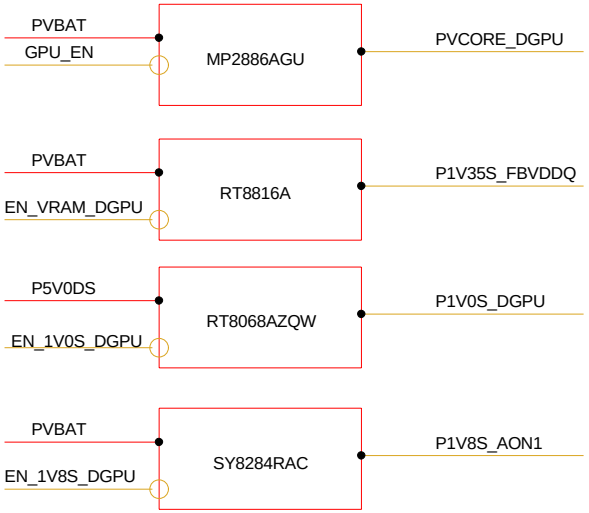
GPU POWER BLOCK

IN/EN OUT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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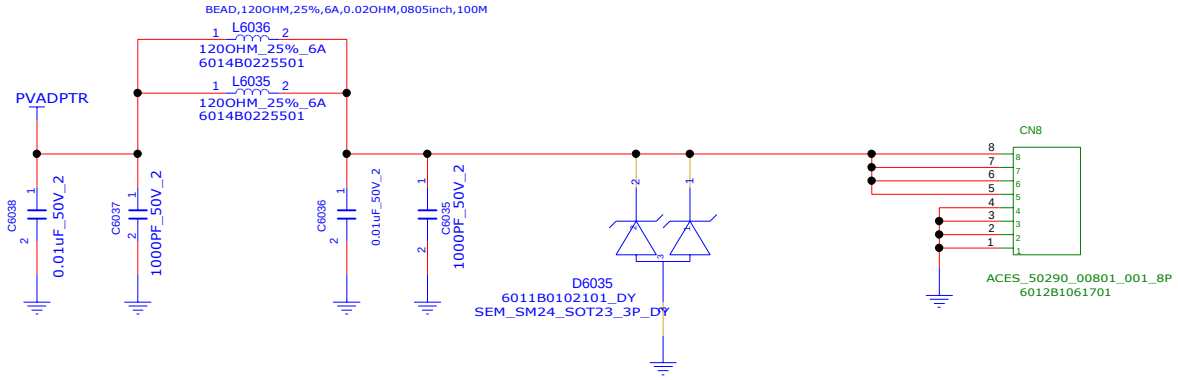


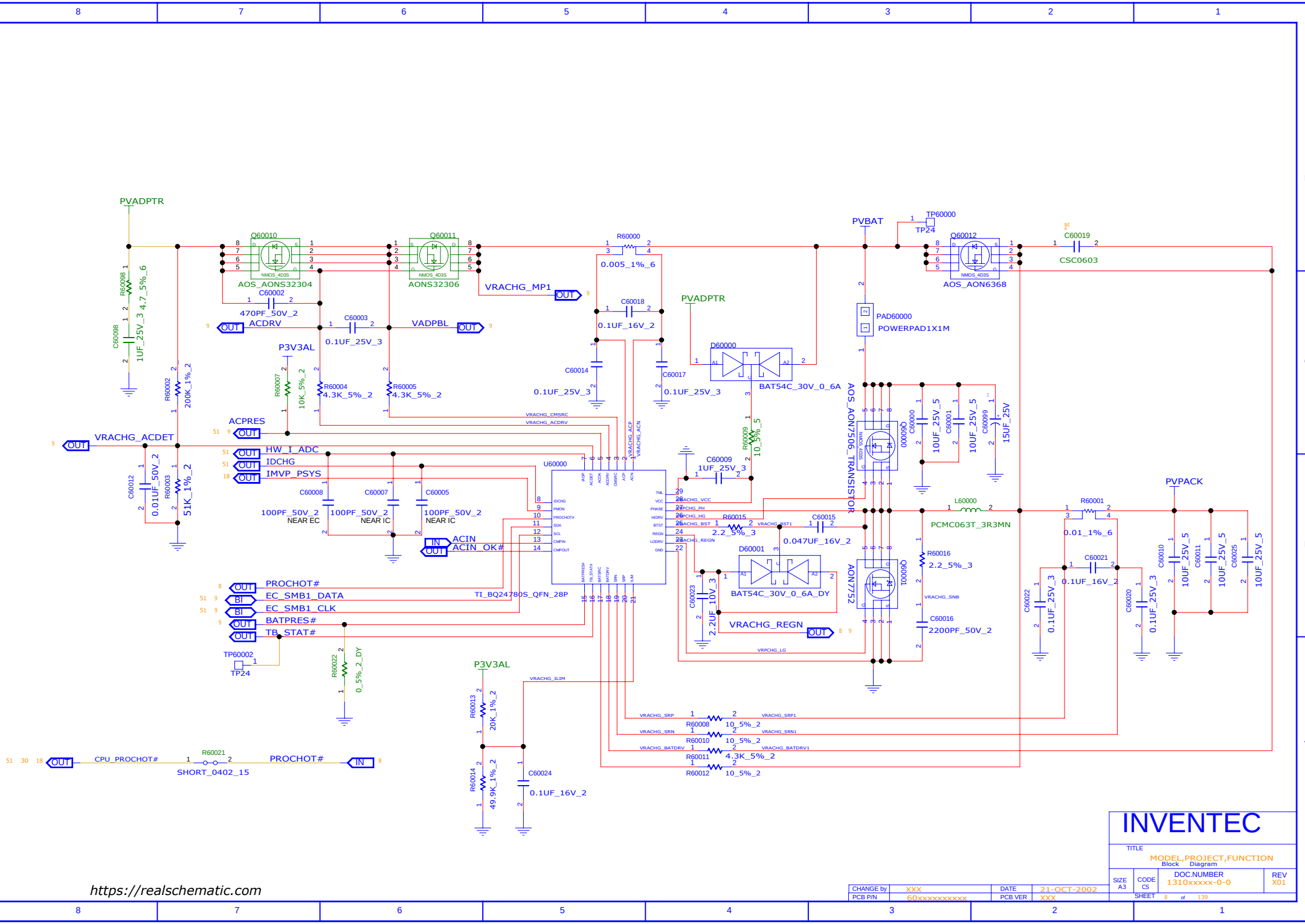
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 7 of 139


PVADPTR
Q60010
AOS_AONS32304
Q60011
AONS32306
R60098
1UF_25V_3
4.7_5%_6
C60098
C60002
470PF_50V_2
ACDRV
C60003
0.1UF_25V_3
VADPBL
VRACHG_MP1
R60000
0.005_1%_6
C60018
0.1UF_16V_2
C60014
0.1UF_25V_3
C60017
0.1UF_25V_3
PVADPTR
D60000
BAT54C_30V_0_6A
PVBAT
TP60000
TP24
Q60012
AOS_AON6368
C60019
CSC0603
PAD60000
POWERPAD1X1M
P3V3AL
R60007
10K_5%_2
R60004
4.3K_5%_2
R60005
4.3K_5%_2
R60002
200K_1%_2
ACPRES
VRACHG_ACDET
R60003
51K_1%_2
C60012
0.01UF_50V_2
HW_I_ADC
IDCHG
IMVP_PSYS
C60008
100PF_50V_2
NEAR EC
C60007
100PF_50V_2
NEAR IC
C60005
100PF_50V_2
NEAR IC
ACIN
ACIN_OK#
U60000
TI_BQ24780S_QFN_28P
VRACHG_CMSRC
VRACHG_ACDRV
VRACHG_ACP
VRACHG_ACN
C60009
1UF_25V_3
R60009
10_5%_5
AOS_AON7506_TRANSISTOR
C60000
C60001
C60099
10UF_25V_5
10UF_25V_5
15UF_25V
L60000
PCMC063T_3R3MN
PVPACK
R60001
0.01_1%_6
C60021
0.1UF_16V_2
C60022
0.1UF_25V_3
C60020
0.1UF_25V_3
C60010
C60011
C60025
10UF_25V_5
R60015
2.2_5%_3
C60015
0.047UF_16V_2
D60001
BAT54C_30V_0_6A_DY
AON7752
R60016
2.2_5%_3
C60016
2200PF_50V_2
C60023
2.2UF_10V_3
VRACHG_REGN
PROCHOT#
EC_SMB1_DATA
EC_SMB1_CLK
BATPRES#
TB_STAT#
TP60002
TP24
R60022
0_5%_2_DY
P3V3AL
R60013
20K_1%_2
R60014
49.9K_1%_2
C60024
0.1UF_16V_2
VRACHG_ILIM
R60008
10_5%_2
R60010
10_5%_2
R60011
4.3K_5%_2
R60012
10_5%_2
CPU_PROCHOT#
R60021
PROCHOT#
SHORT_0402_15
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
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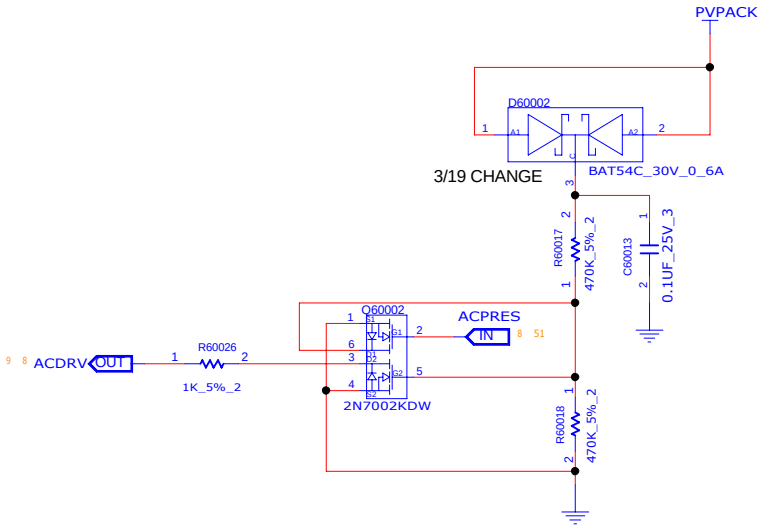
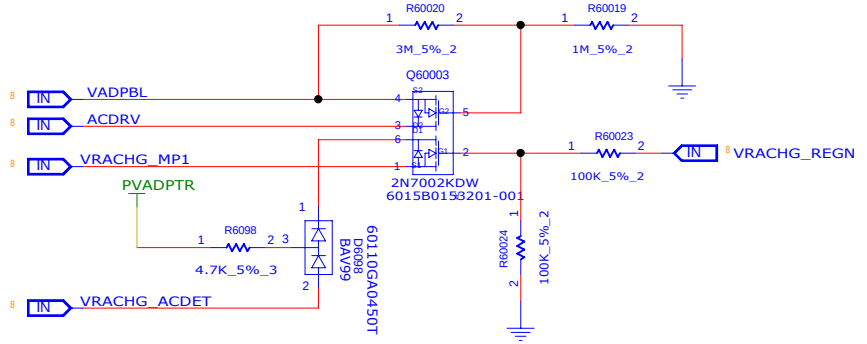
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx
PCB VER XXX
https://realschematic.com

FOR CHARGER

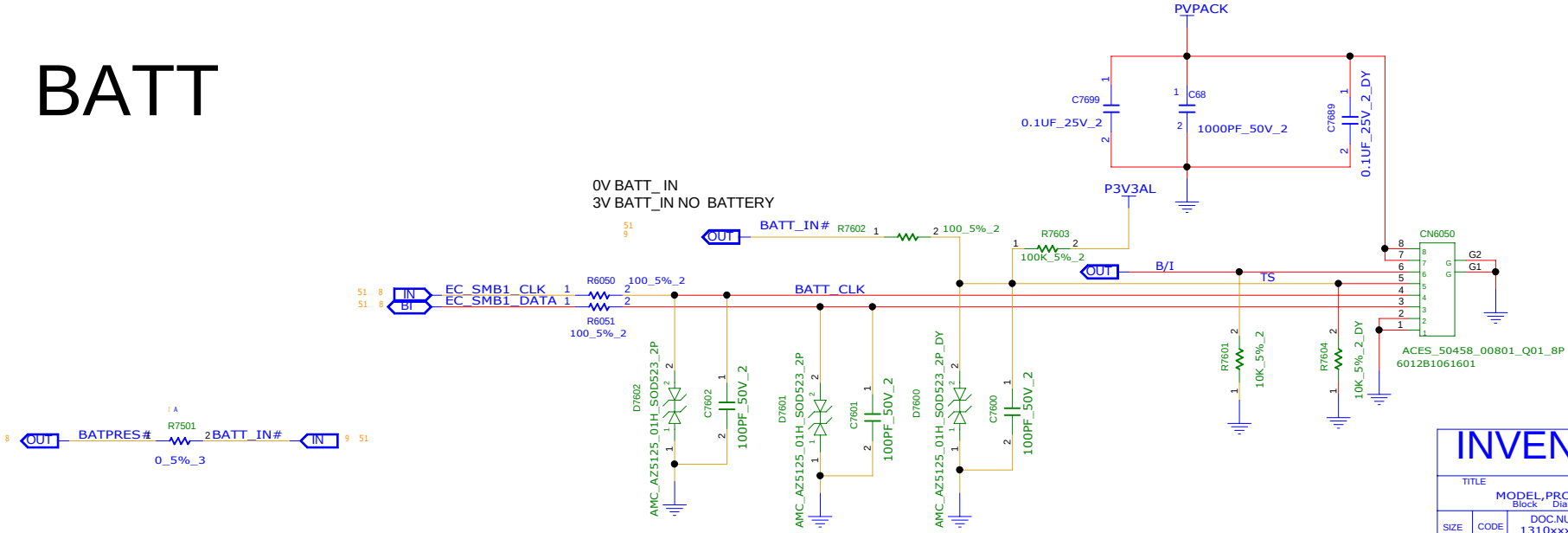
SCP



ARP



BATT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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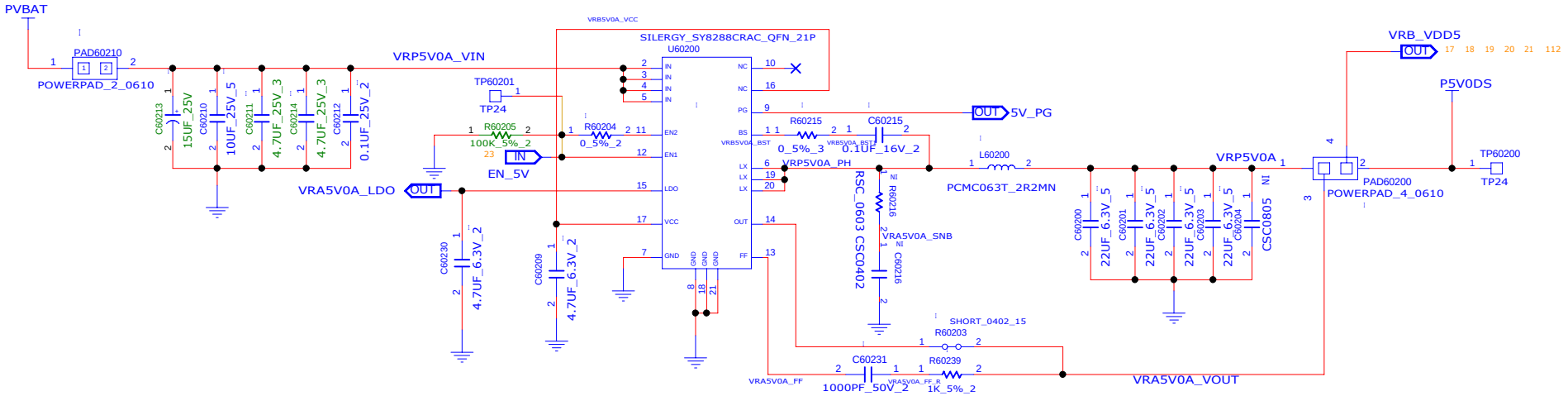

https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P5V0DS

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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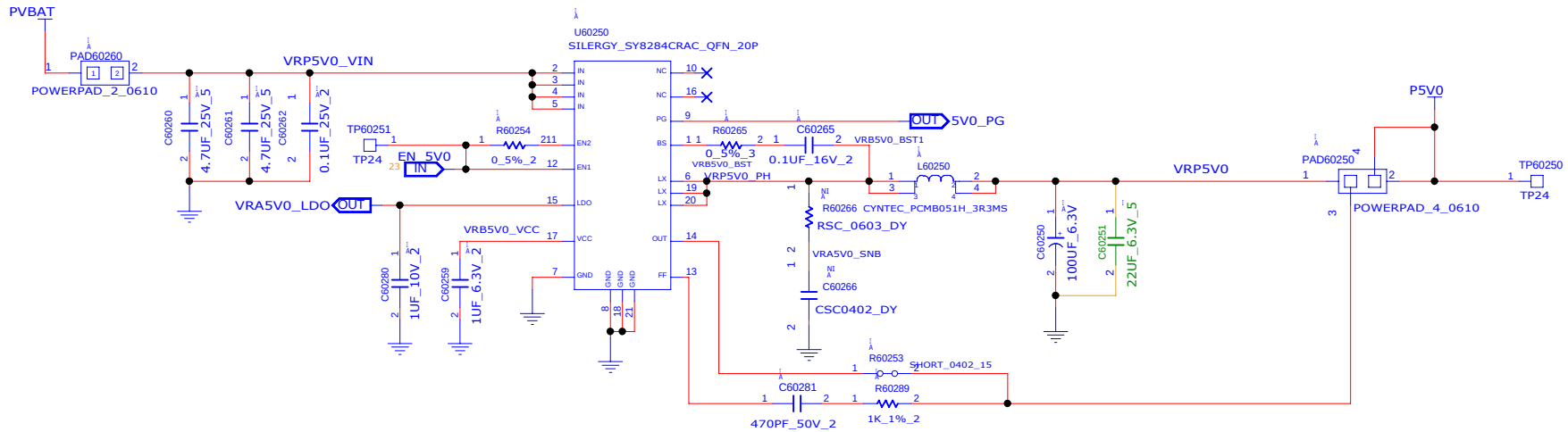

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL_PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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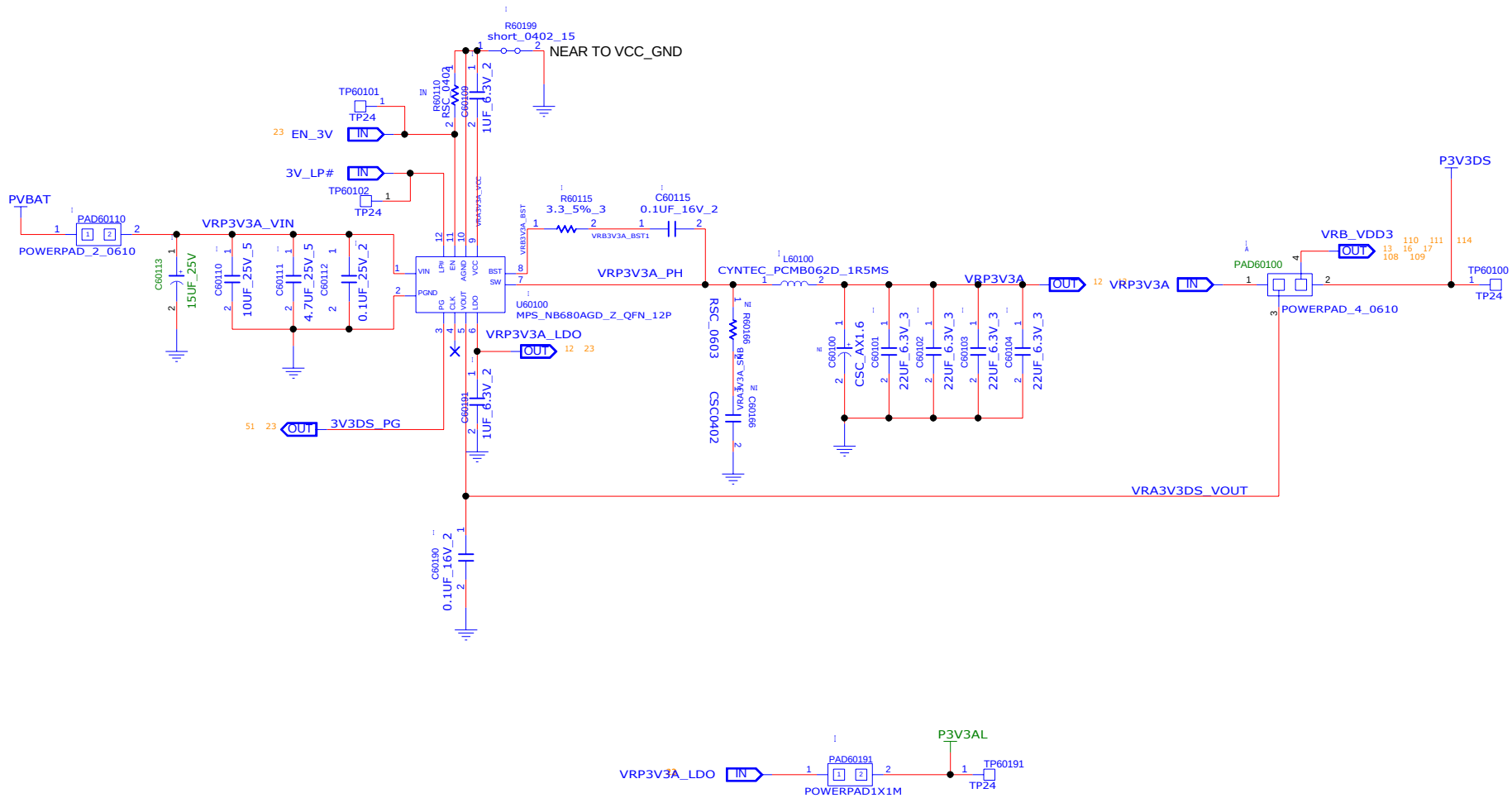

https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P3V3DS_NB680A

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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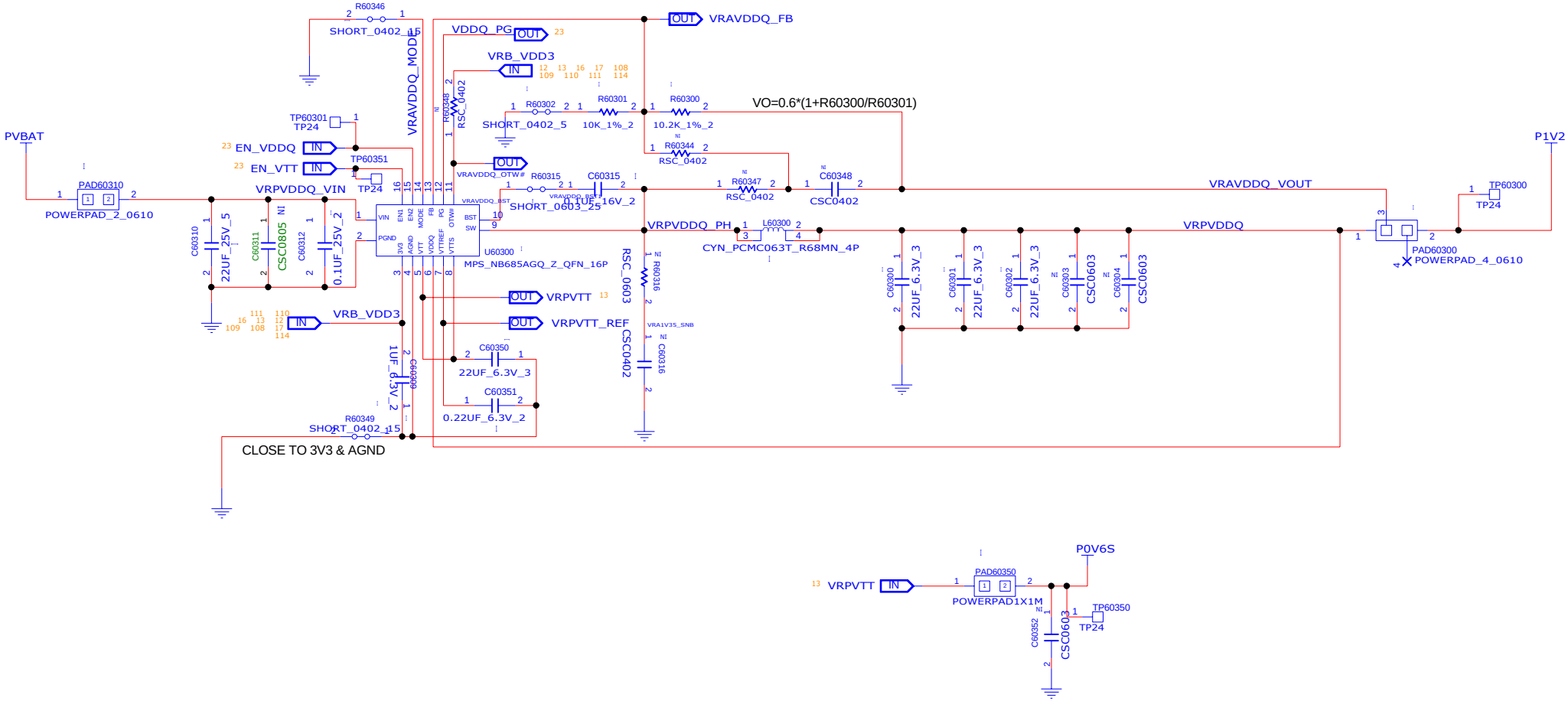
Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



https://realschematic.com

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
VDDQ

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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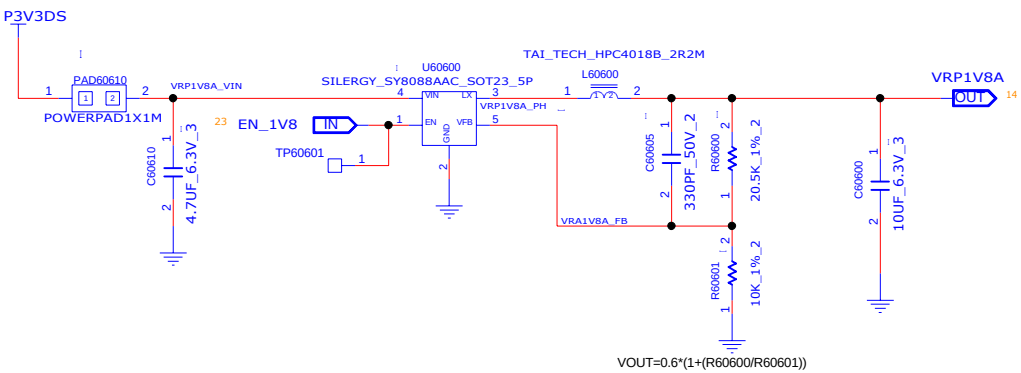

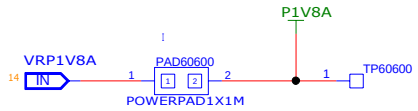

https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
P1V8DS

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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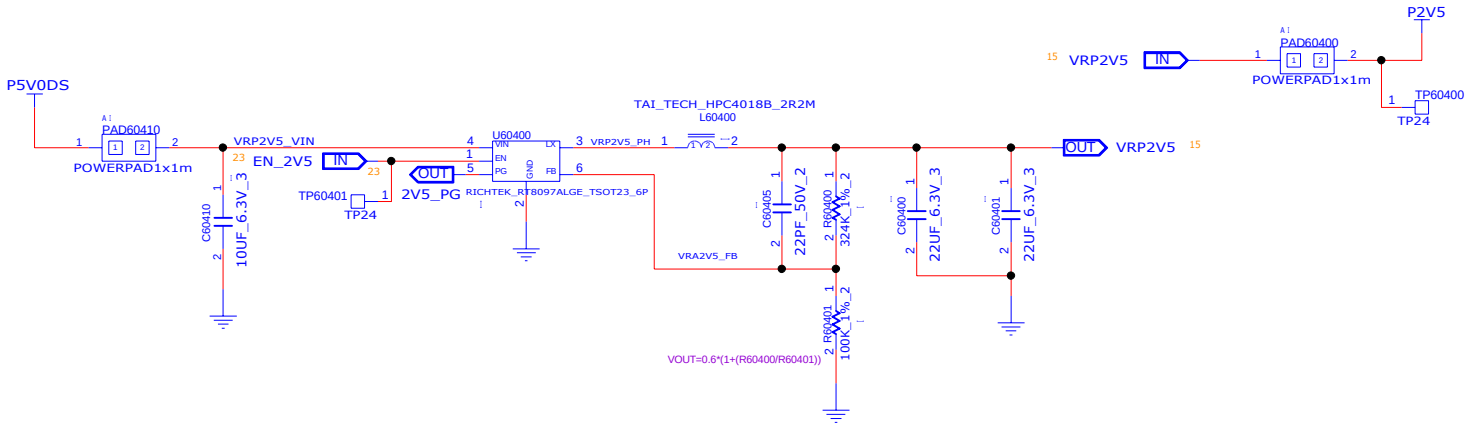

https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P2V5

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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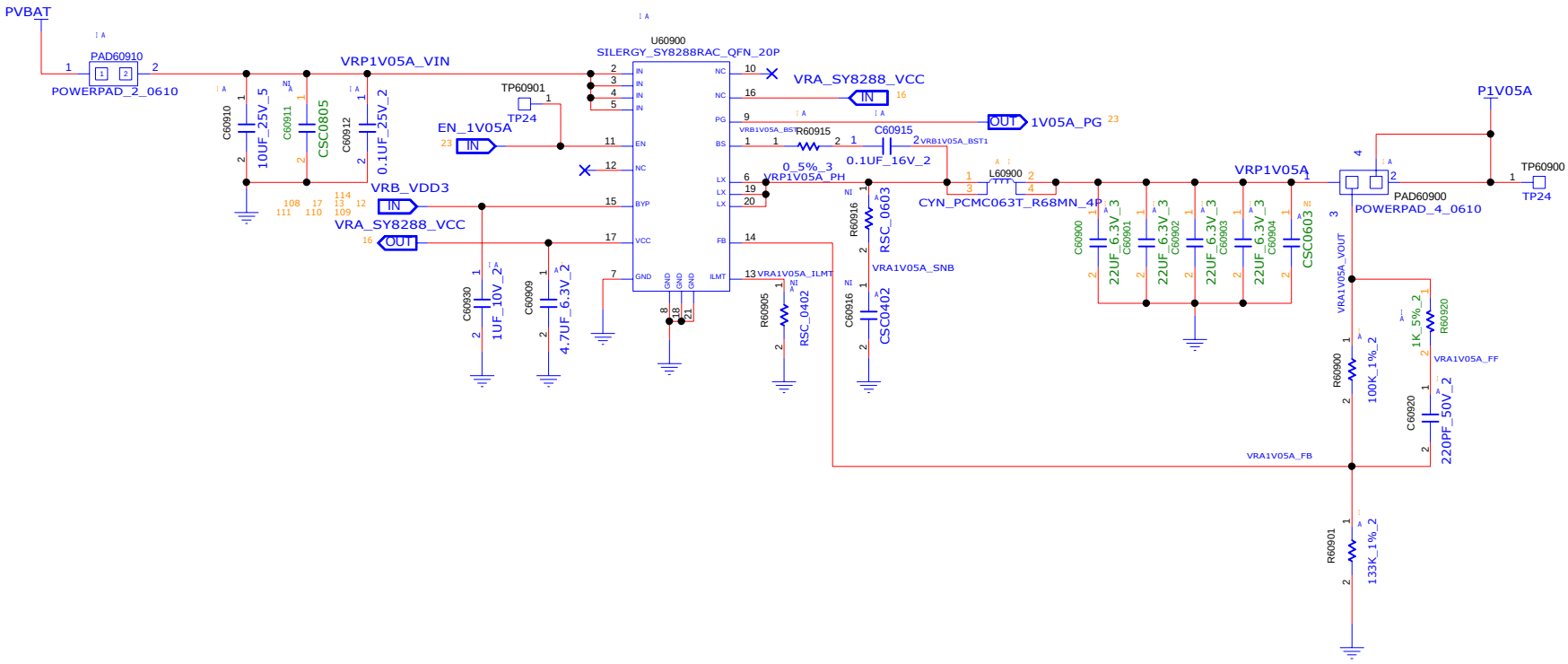

VO=0.6*(1+R60900/R60901)

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION		
	P1V0A		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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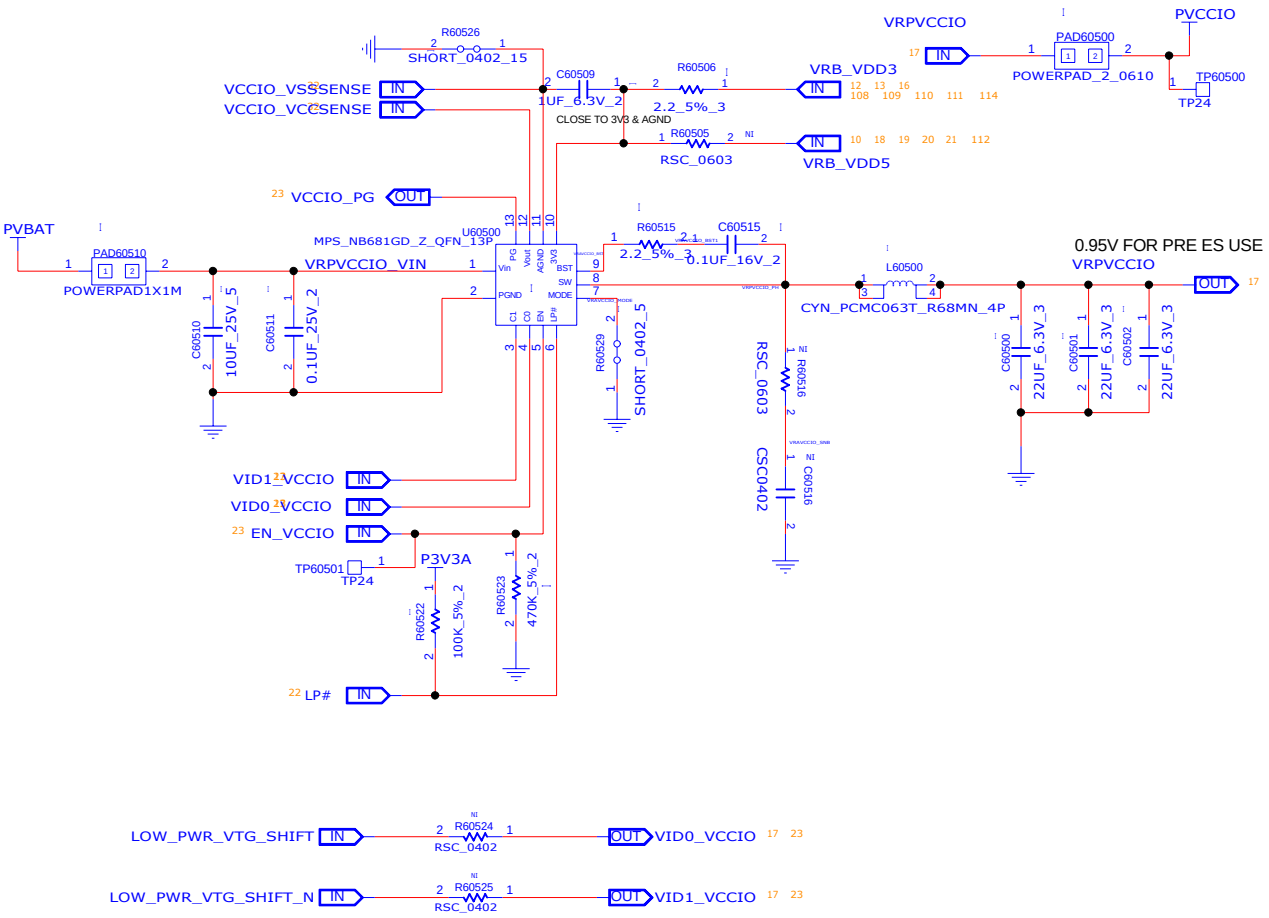
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPIO	100 K
M4	Others	150 K

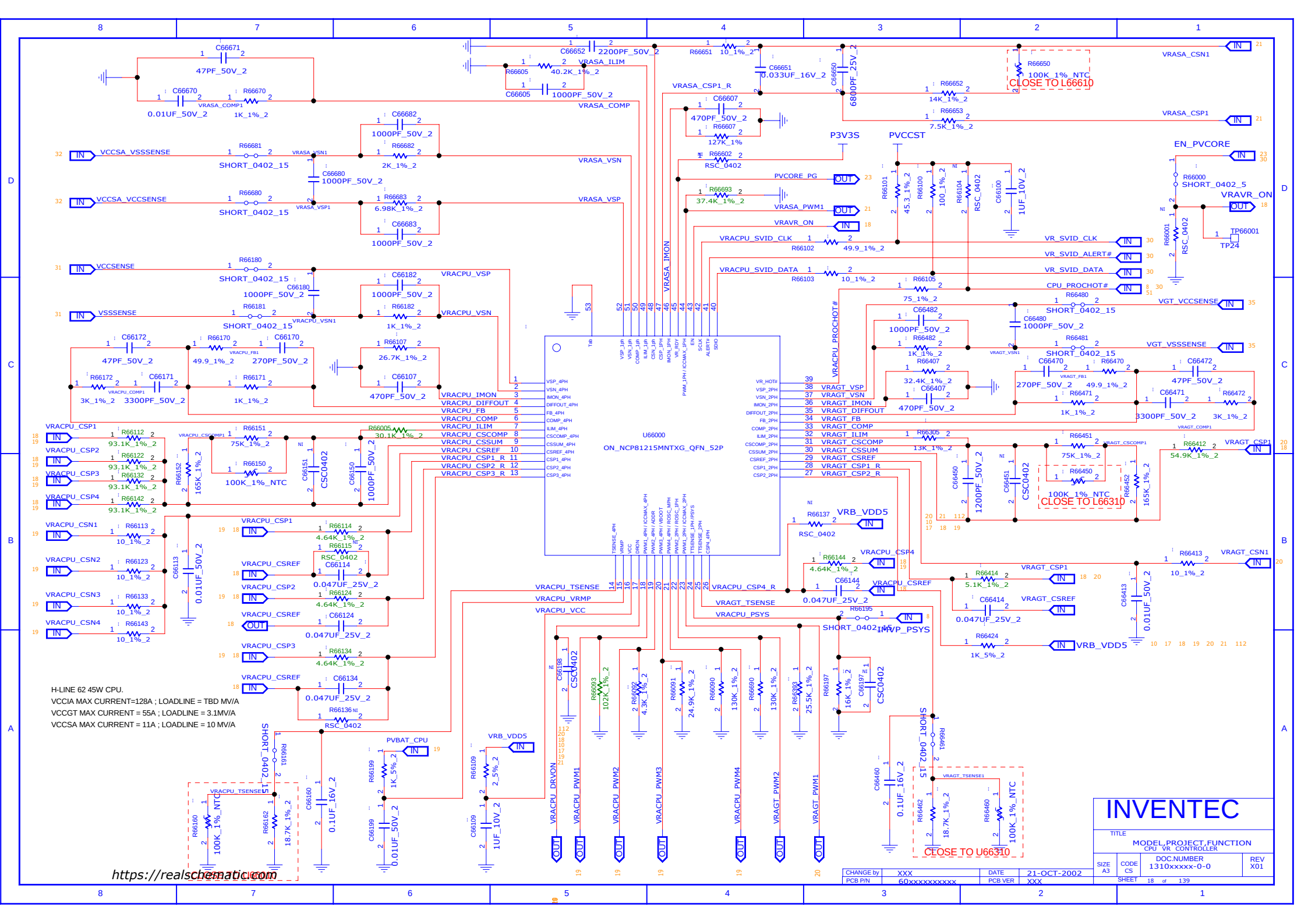
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

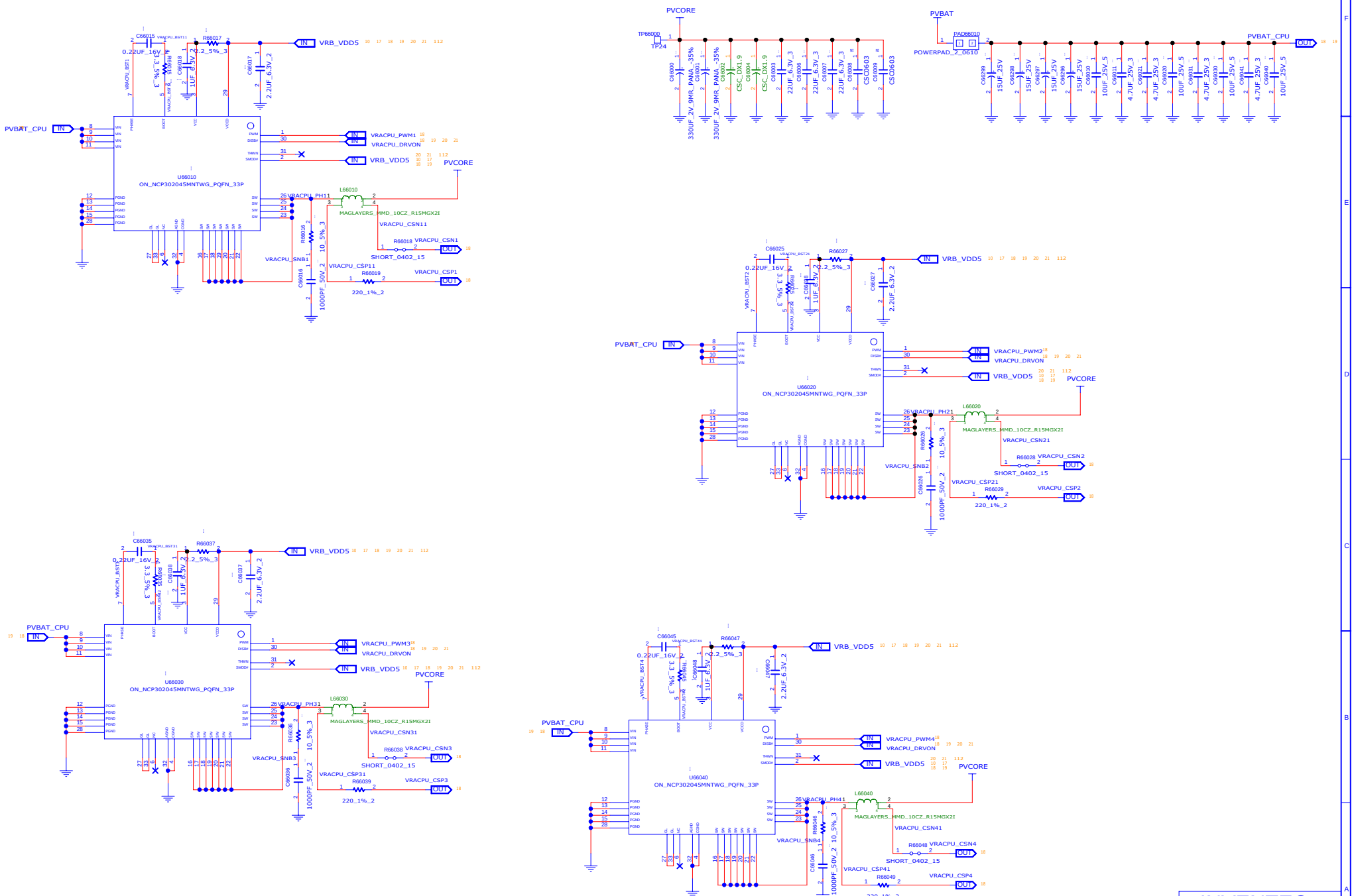


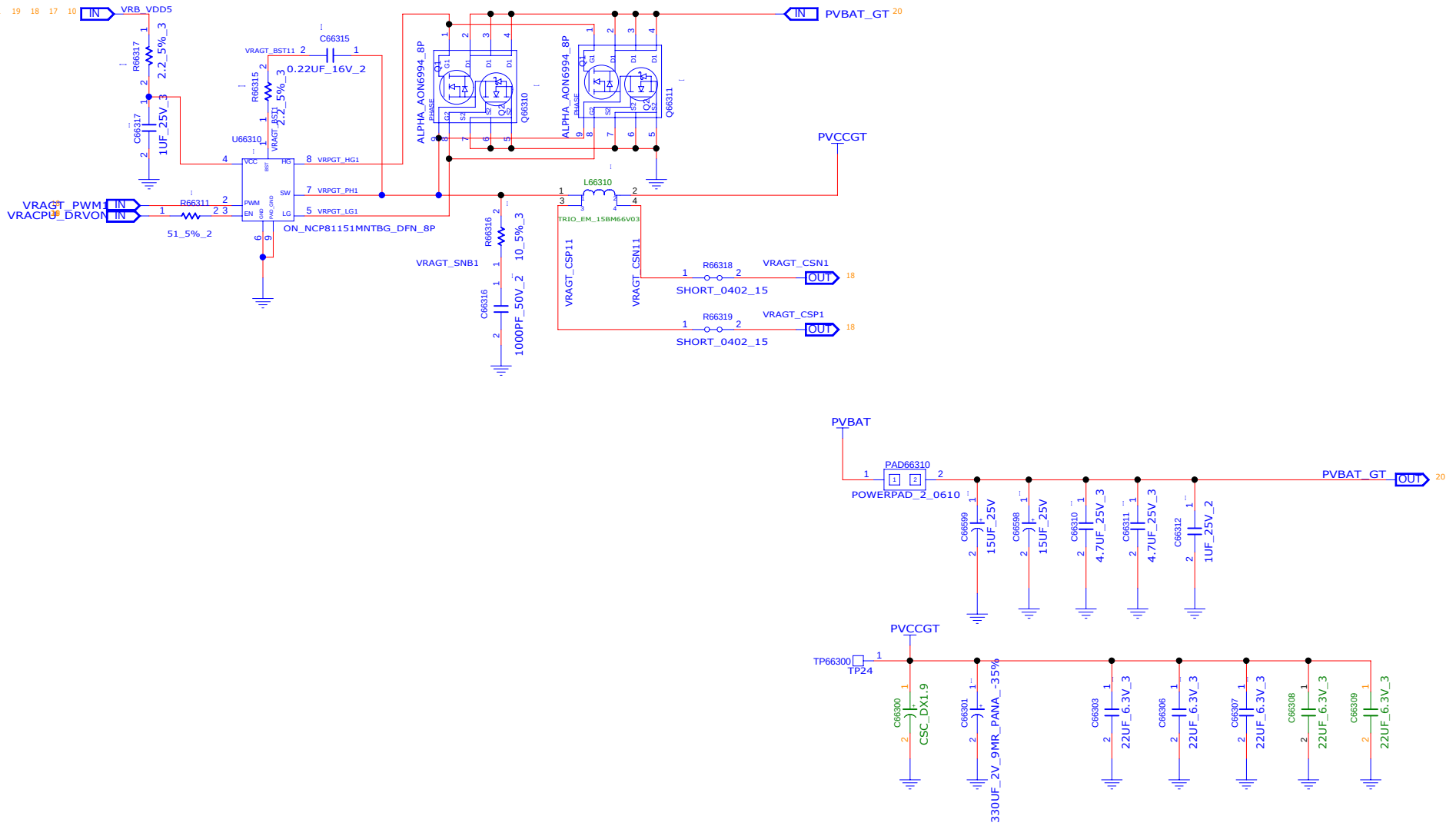
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCIO

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxx	PCB VER	XXX			SHEET 17 of 139	


U66000
ON_NCP81215MNTXG_QFN_52P
H-LINE 62 45W CPU.
VCCIA MAX CURRENT=128A ; LOADLINE = TBD MV/A
VCCGT MAX CURRENT = 55A ; LOADLINE = 3.1MV/A
VCCSA MAX CURRENT = 11A ; LOADLINE = 10 MV/A
CLOSE TO L66610
CLOSE TO L66310
CLOSE TO U66310
INVENTEC
MODEL,PROJECT,FUNCTION
CPU VR CONTROLLER
DOC.NUMBER
1310xxxxx-0-0
REV X01
SIZE A3
CODE CS
SHEET 18 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX
https://realschematic.com


PVBAT_CPU
VRB_VDD5
PVCORE
PVBAT
U66010
ON_NCP302045MNTWG_PQFN_33P
VRACPU_PWM1
VRACPU_DRVON
VRACPU_CSN11
VRACPU_CSP11
VRACPU_SNB1
U66020
VRACPU_PWM2
VRACPU_CSN21
VRACPU_CSP21
VRACPU_SNB2
U66030
VRACPU_PWM3
VRACPU_CSN31
VRACPU_CSP31
VRACPU_SNB3
U66040
VRACPU_PWM4
VRACPU_CSN41
VRACPU_CSP41
VRACPU_SNB4
MAGLAYERS_HMD_10CZ_R15MGX2I
SHORT_0402_15
220_1%_2
1000PF_50V_2
10_5%_3
0.22UF_16V
2.2UF_6.3V_2
1UF_6.3V_2
330UF_2V_9MR_PANA_-35%
CSC_DX1_9
22UF_6.3V_3
15UF_25V
10UF_25V_5
4.7UF_25V_3
POWERPAD_2_0610
INVENTEC
MODEL,PROJECT,FUNCTION
PVCORE
https://realschematic.com



https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCGT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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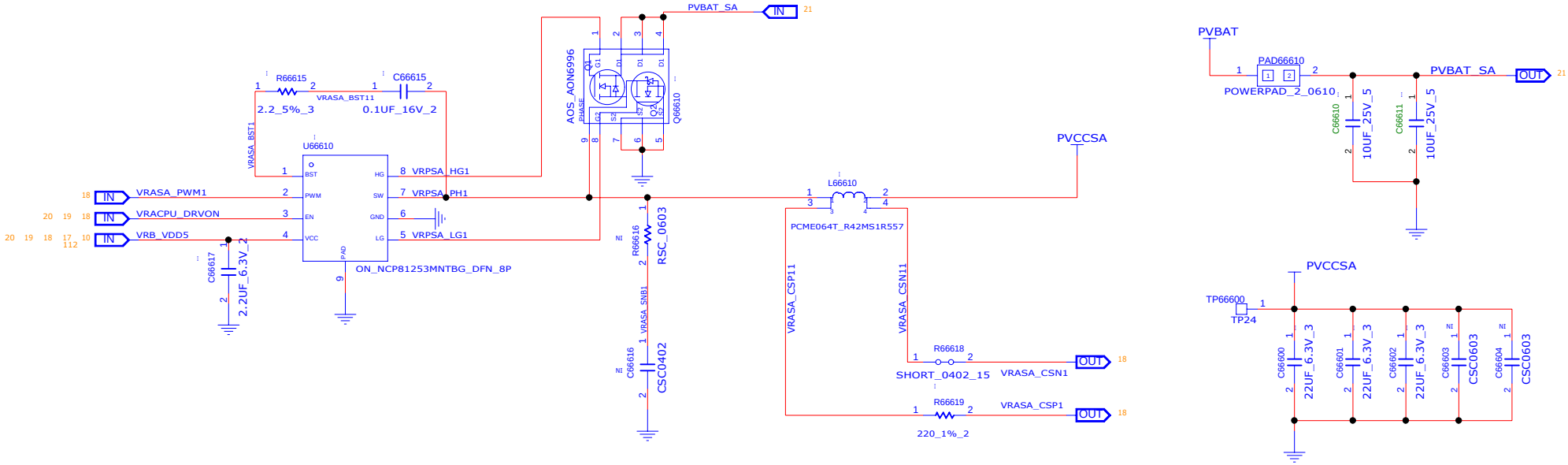

https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCSA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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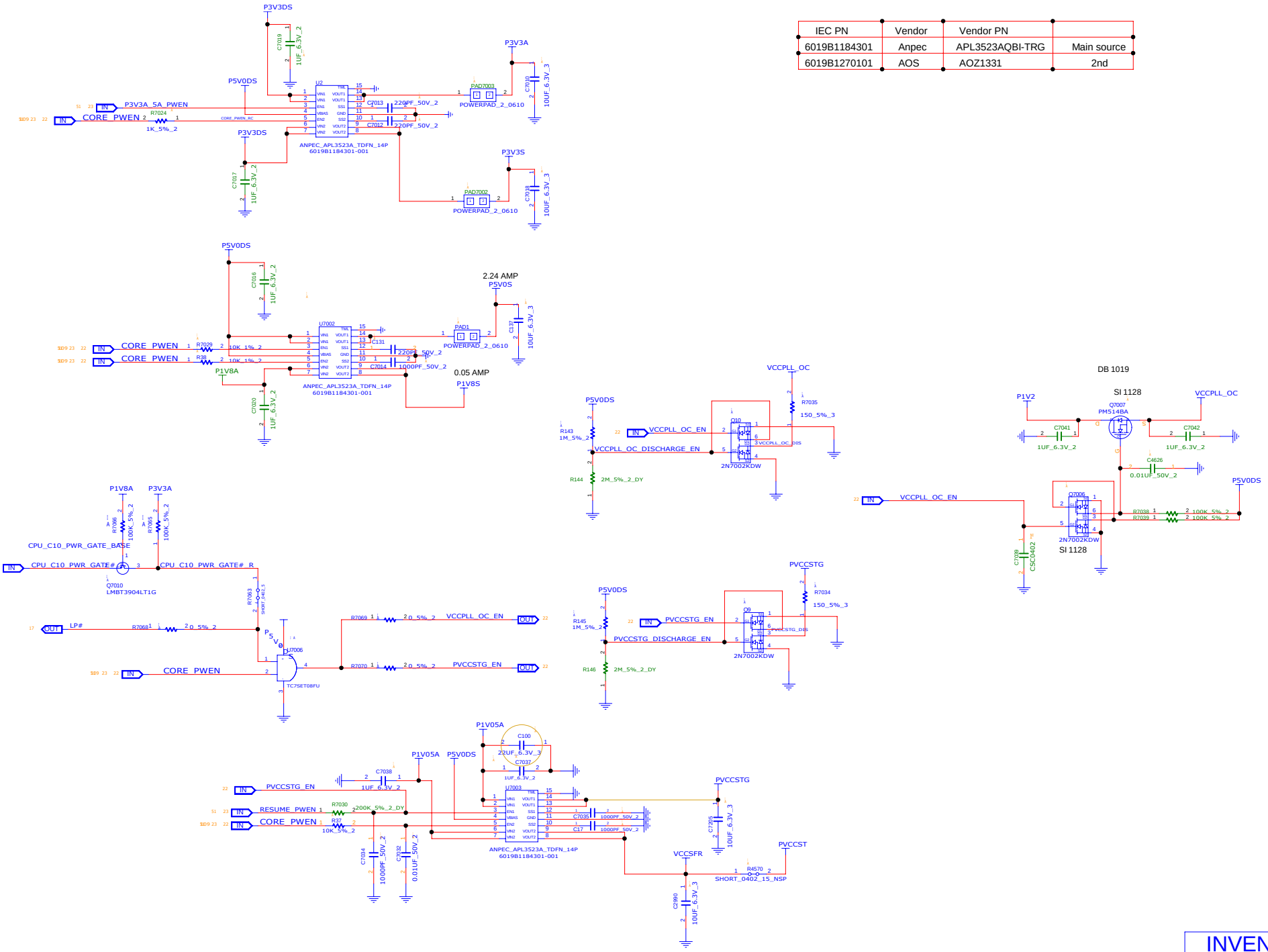


IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd

INVENTEC

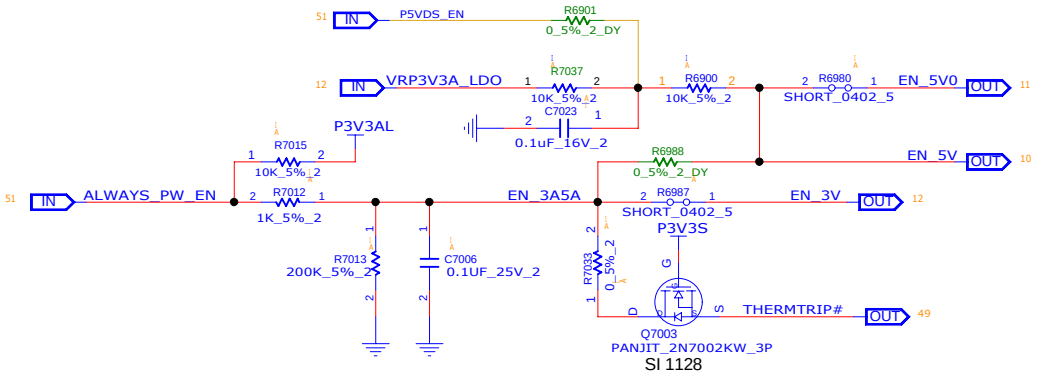
TITLE: MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

SHEET of 22 L39

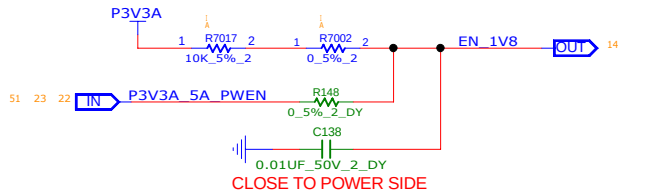
CHANGE SI XXX DATE
PCB P/N 60xxxxxxxxx PCB VER 2.1

1. P3V3DS / P5V0DS

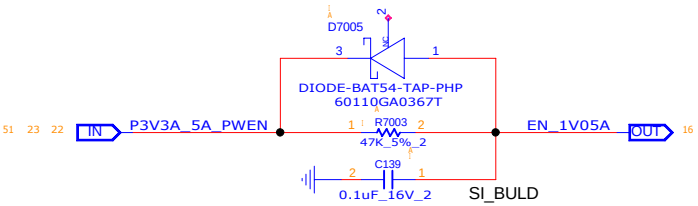


SI 1128

2. P1V0A / P1V8A / P3V3A

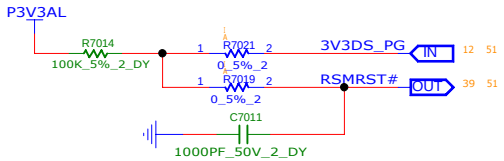


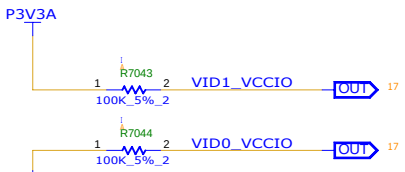
CLOSE TO POWER SIDE



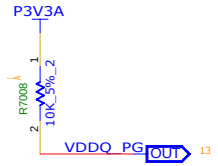
SI_BULD

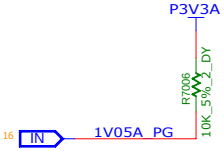
CLOSE TO POWER SIDE

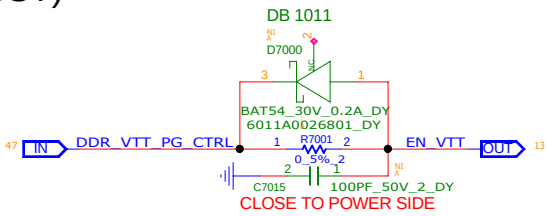




3. P1V2 / P1V8 / VCCSFR(PVCCST)







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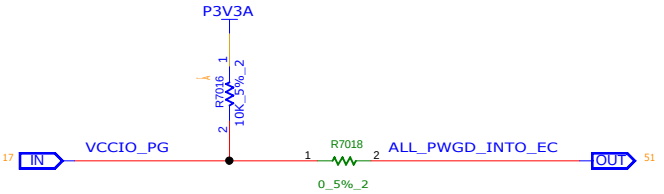
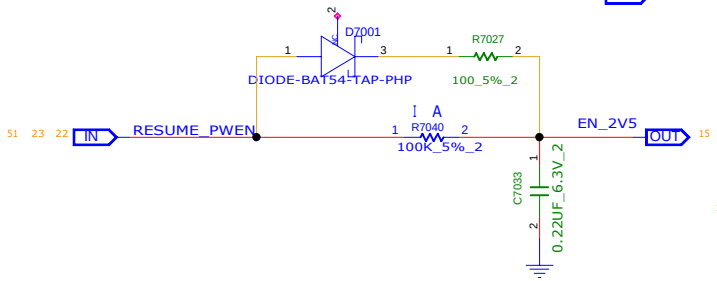
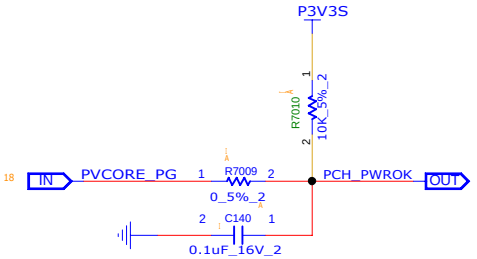
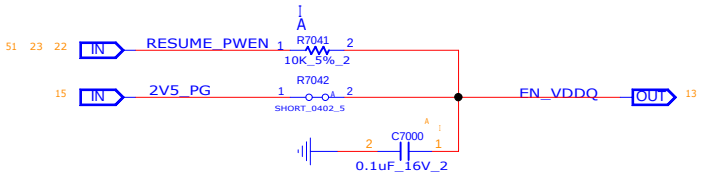
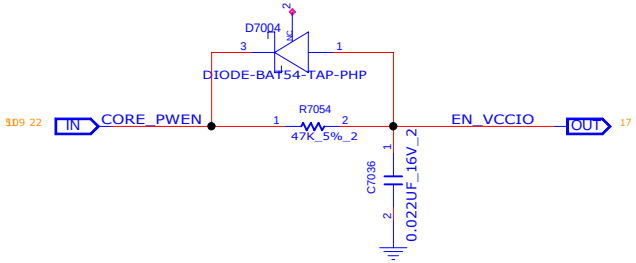
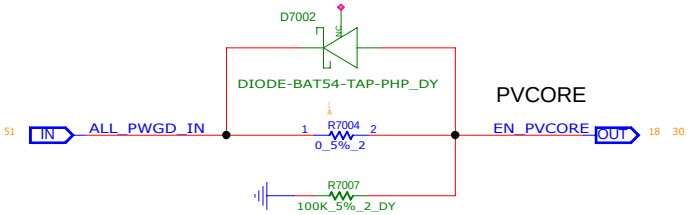












INVENTEC

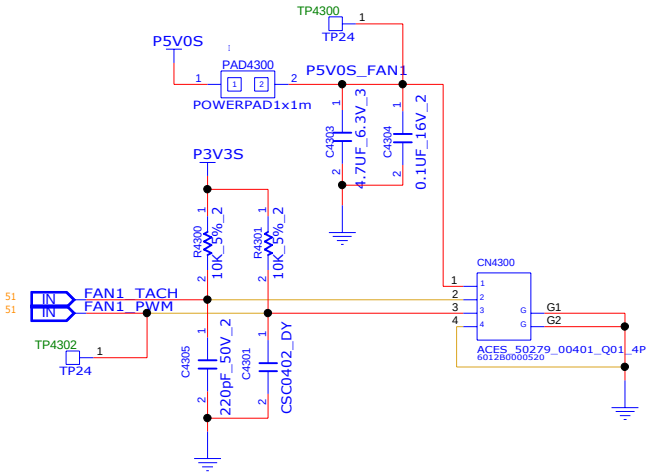
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	
PCB P/N	60NXXXXXXXX	PCB VER	XX

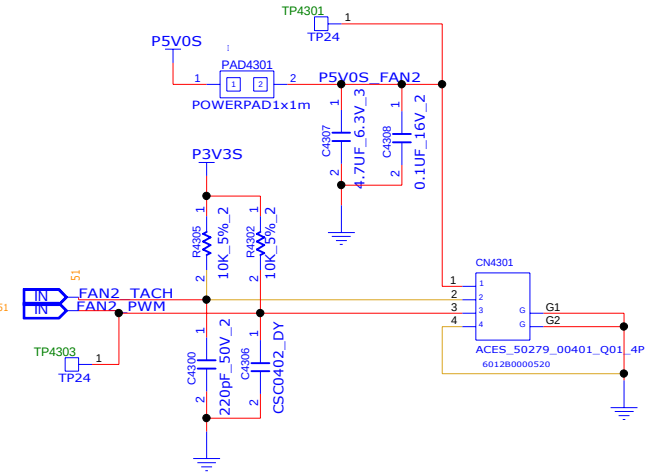
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

DATE: OCT-2002
SHEET of 23 139

REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
FAN & THERMAL

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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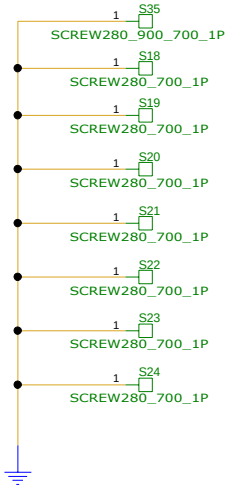
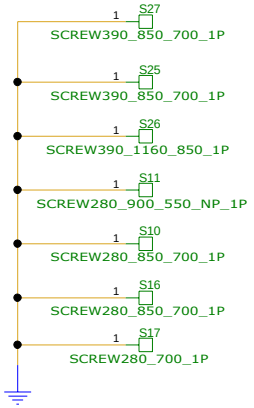
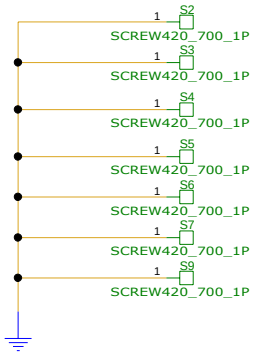
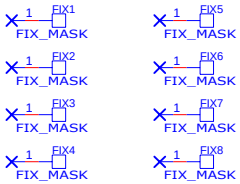
REFERENCE 0~49(PCB SCREW)





PCB





CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
XDP & ME CONN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE1_H-PEG,HDMI

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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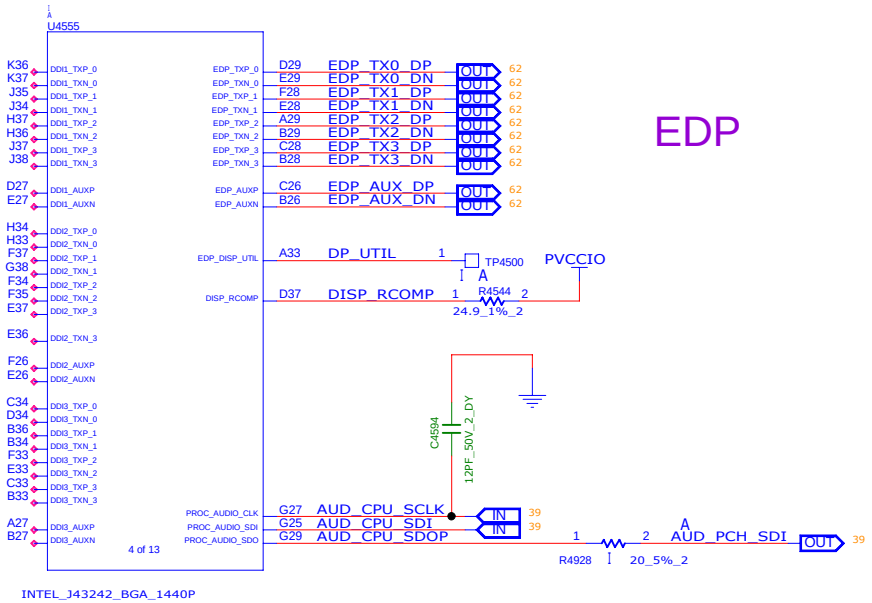
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

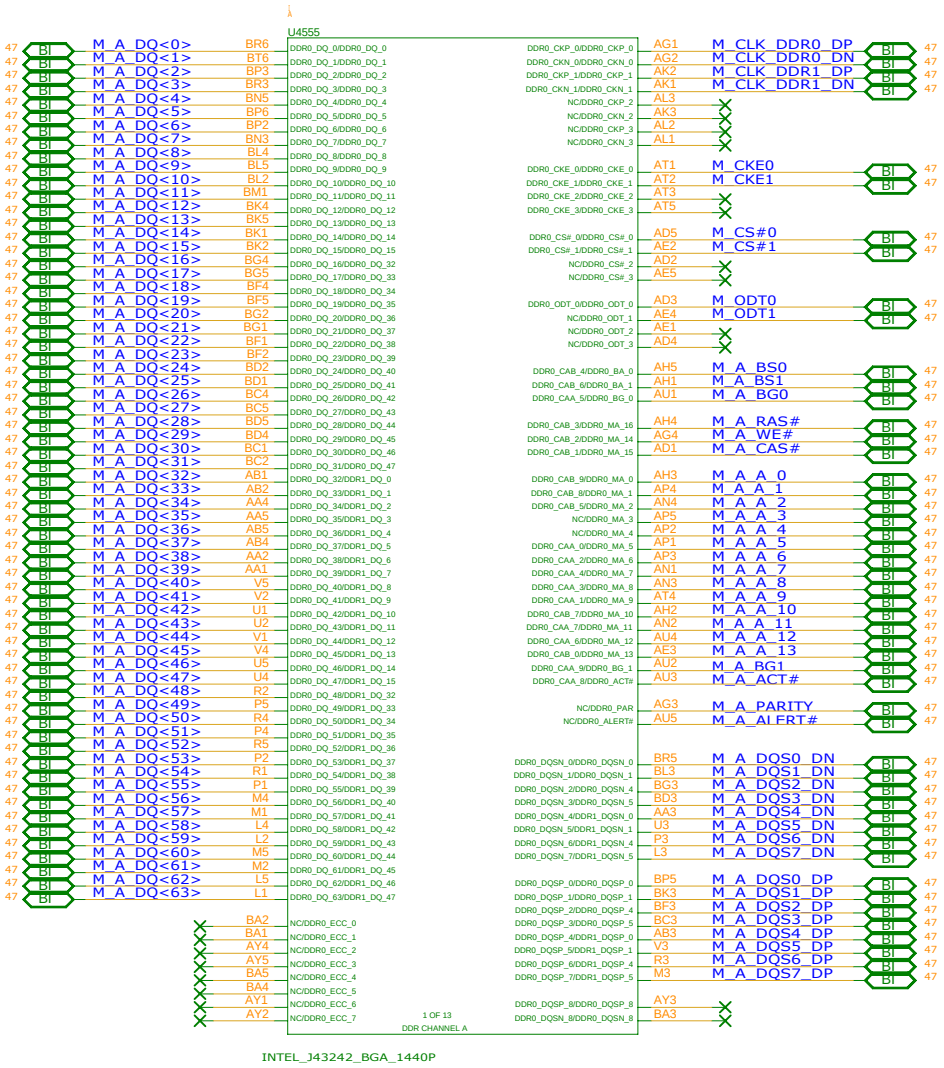


EDP

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE2_H-DDI,EDP		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 27 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE_H-DDR-1

SIZE	CODE	DOC.NUMBER	REV
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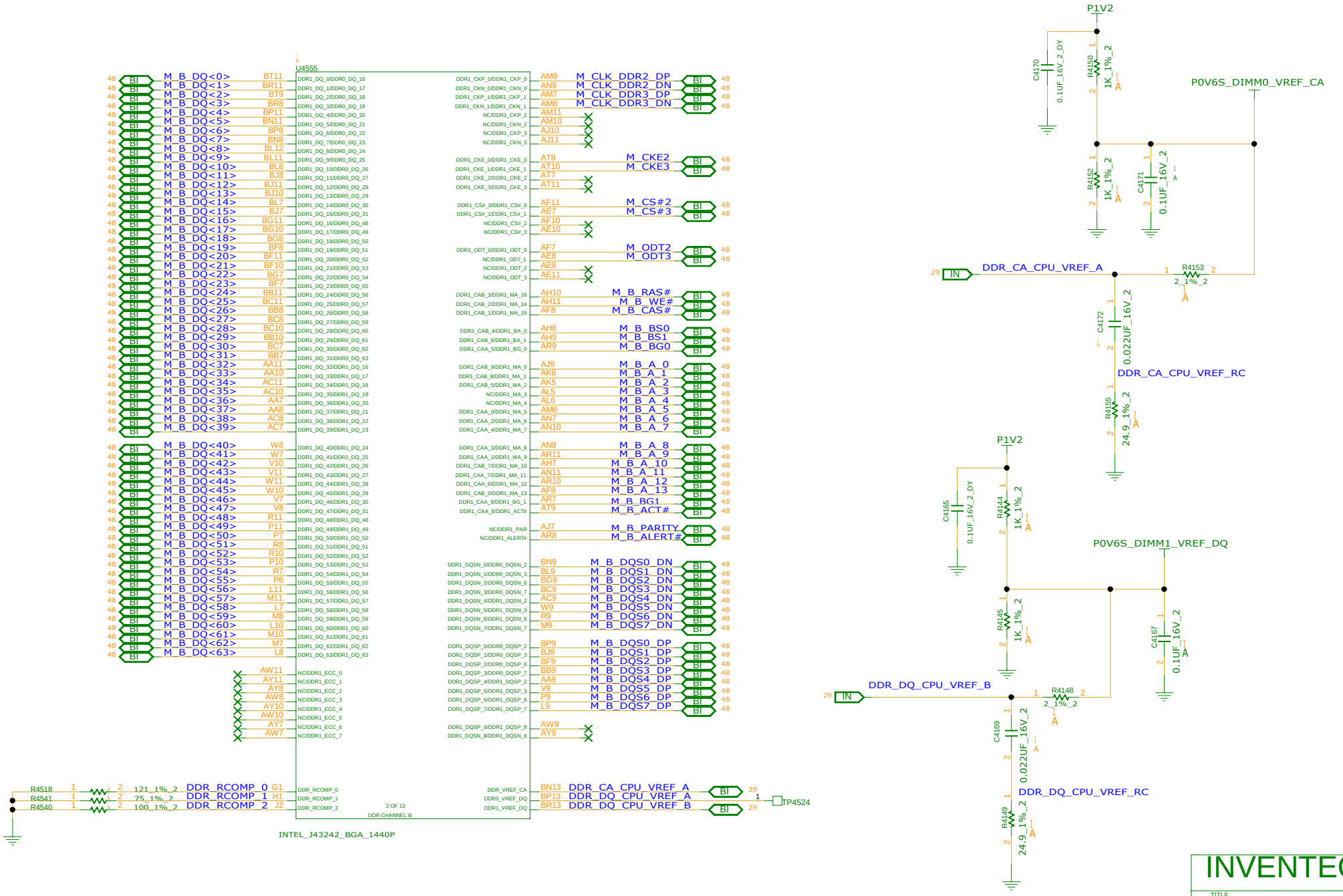
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M_CLK_DDR2_DN
M_CLK_DDR3_DP
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M_CKE3
M_CS#2
M_CS#3
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M_B_WE#
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M_B_A_12
M_B_A_13
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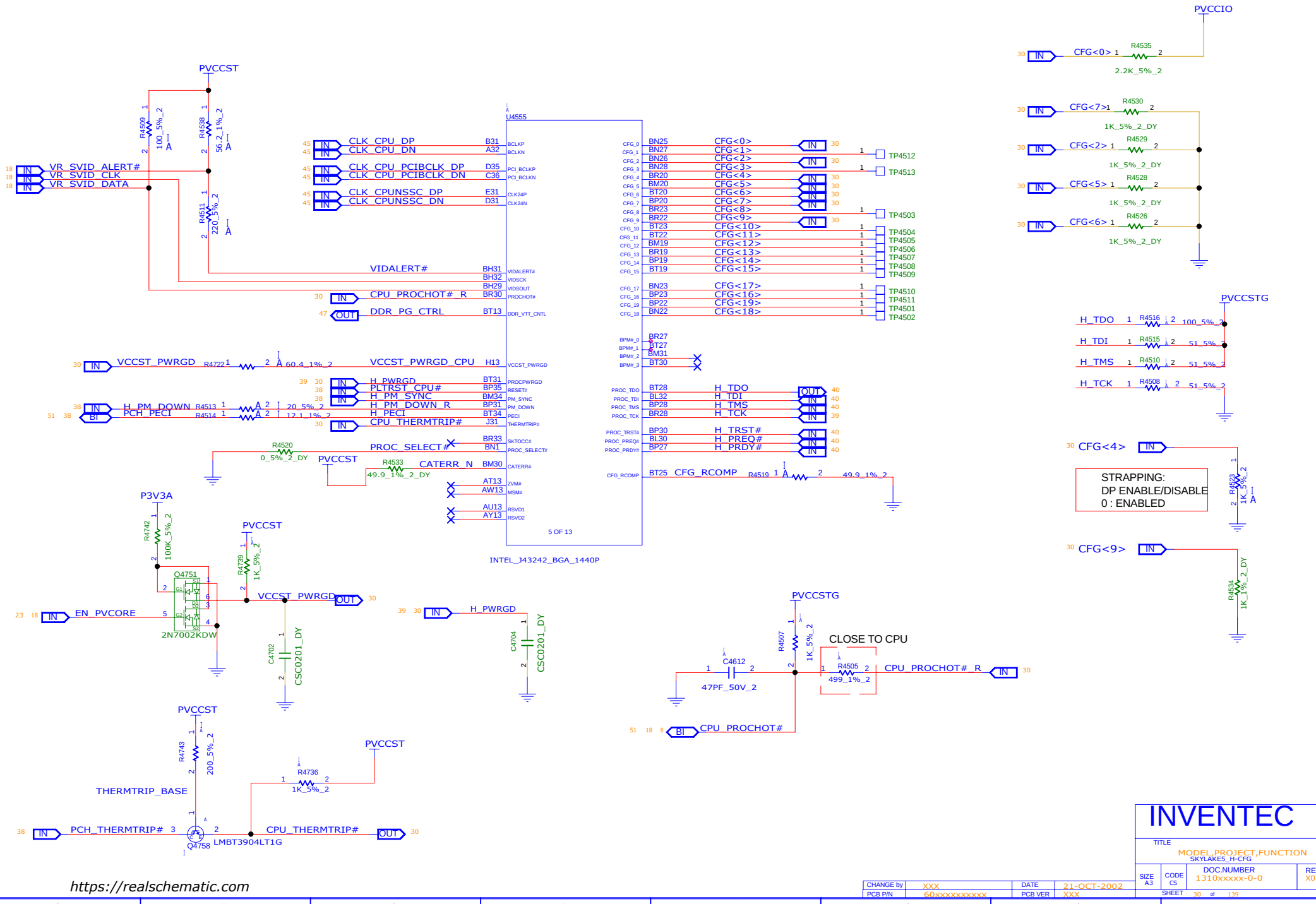
DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2
DDR_CA_CPU_VREF_A
DDR_DQ_CPU_VREF_A
DDR_DQ_CPU_VREF_B
TP4524
2 OF 13
DDR CHANNEL B
INTEL_J43242_BGA_1440P
P1V2
P0V6S_DIMM0_VREF_CA
P0V6S_DIMM1_VREF_DQ
DDR_CA_CPU_VREF_RC
DDR_DQ_CPU_VREF_RC
https://realschematic.com
INVENTEC
MODEL,PROJECT,FUNCTION
SKYLAKE4_H-DDR-2
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET
29 of 139
CHANGE by
XXX
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxxx
PCB VER
XXX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PVCCIO
PVCCSTG
P3V3A
U4555
INTEL_J43242_BGA_1440P
5 OF 13
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA
CLK_CPU_DP
CLK_CPU_DN
CLK_CPU_PCIBCLK_DP
CLK_CPU_PCIBCLK_DN
CLK_CPUNSSC_DP
CLK_CPUNSSC_DN
VIDALERT#
CPU_PROCHOT#_R
DDR_PG_CTRL
VCCST_PWRGD
VCCST_PWRGD_CPU
H_PWRGD
PLTRST_CPU#
H_PM_SYNC
H_PM_DOWN_R
H_PECI
CPU_THERMTRIP#
PROC_SELECT#
CATERR_N
H_PM_DOWN
PCH_PECI
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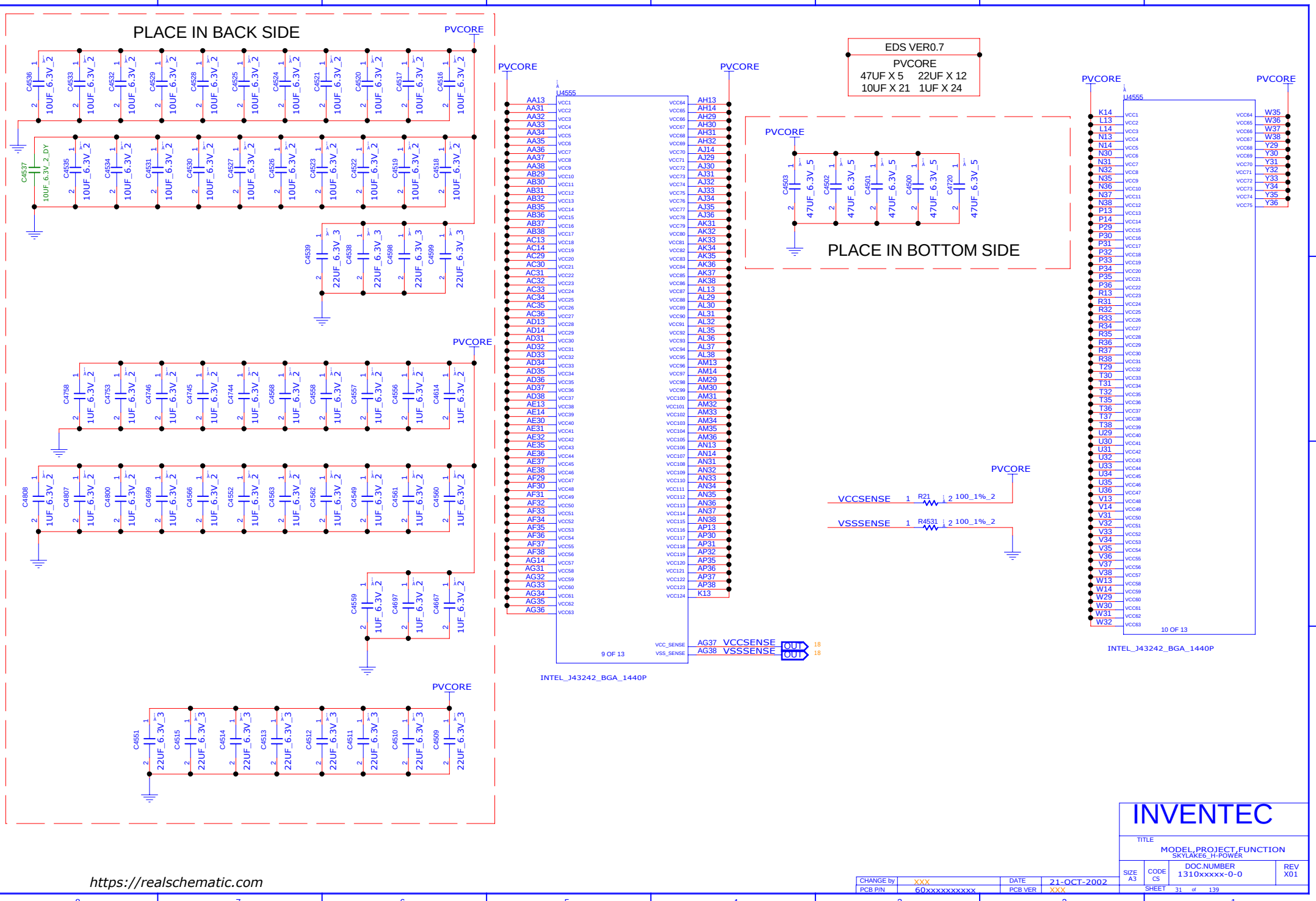
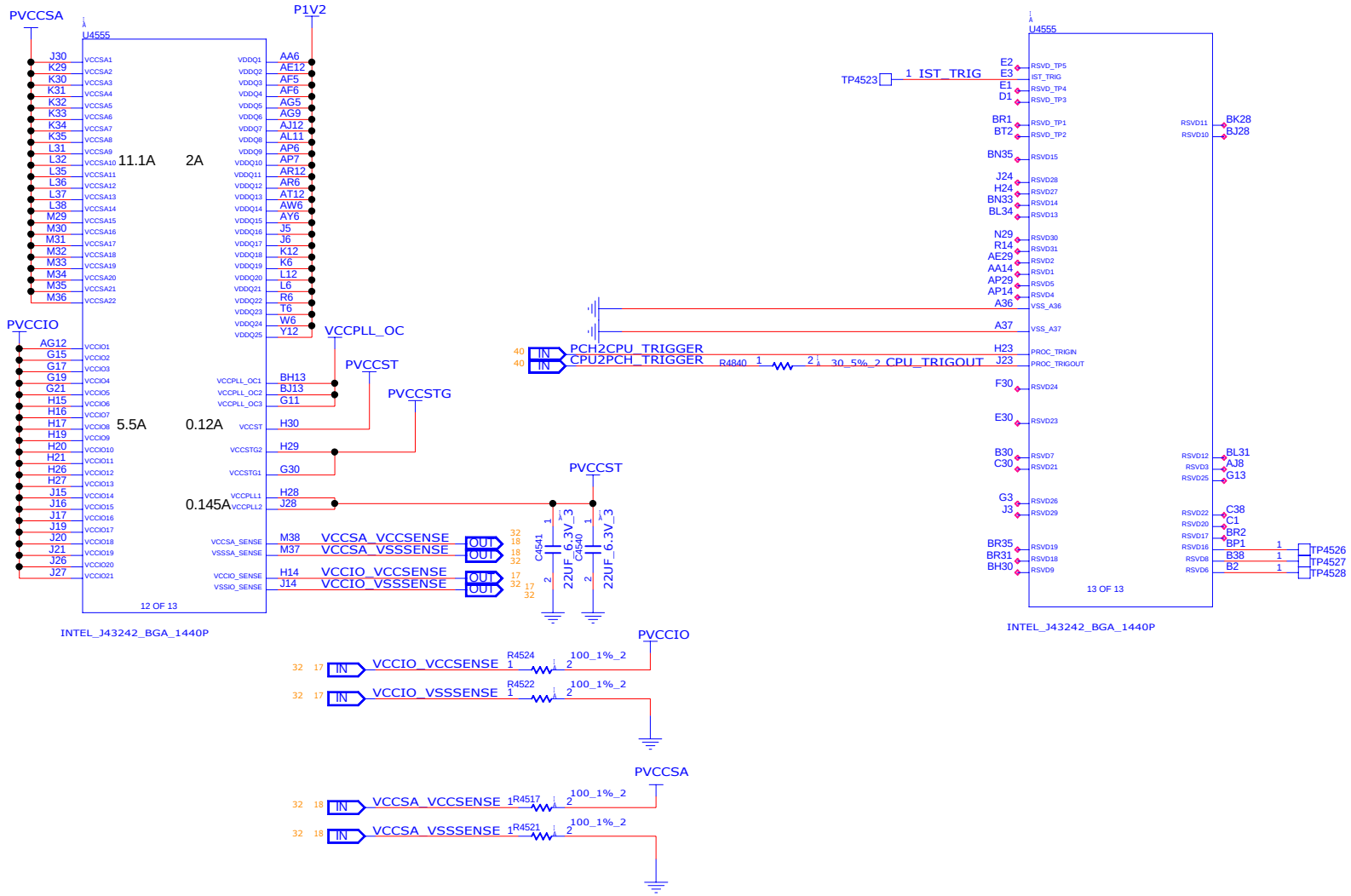
CFG_RCOMP
H_TDO
H_TDI
H_TMS
H_TCK
H_TRST#
H_PREQ#
H_PRDY#
EN_PVCORE
VCCST_PWRGD
2N7002KDW
Q4751
THERMTRIP_BASE
PCH_THERMTRIP#
CPU_THERMTRIP#
LMBT3904LT1G
Q4758
CPU_PROCHOT#
CLOSE TO CPU
STRAPPING:
DP ENABLE/DISABLE
0 : ENABLED
TP4512
TP4513
TP4503
TP4504
TP4505
TP4506
TP4507
TP4508
TP4509
TP4510
TP4511
TP4501
TP4502
https://realschematic.com
INVENTEC
MODEL,PROJECT,FUNCTION
SKYLAKE5_H-CFG
DOC.NUMBER
1310xxxxx-0-0
REV
X01
CHANGE by
XXX
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxxx
PCB VER
XXX
SHEET
30 of 139


PLACE IN BACK SIDE
PVCORE
10UF_6.3V_2
10UF_6.3V_2_DY
22UF_6.3V_3
1UF_6.3V_2
EDS VER0.7
PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24
PLACE IN BOTTOM SIDE
47UF_6.3V_5
U4555
INTEL_J43242_BGA_1440P
9 OF 13
10 OF 13
VCCSENSE
VSSSENSE
R21
R4531
100_1%_2
AG37 VCCSENSE
AG38 VSSSENSE
OUT
INVENTEC
MODEL,PROJECT,FUNCTION
SKYLAKE6_H-POWER
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET 31 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX
https://realschematic.com



https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE7_H-POWER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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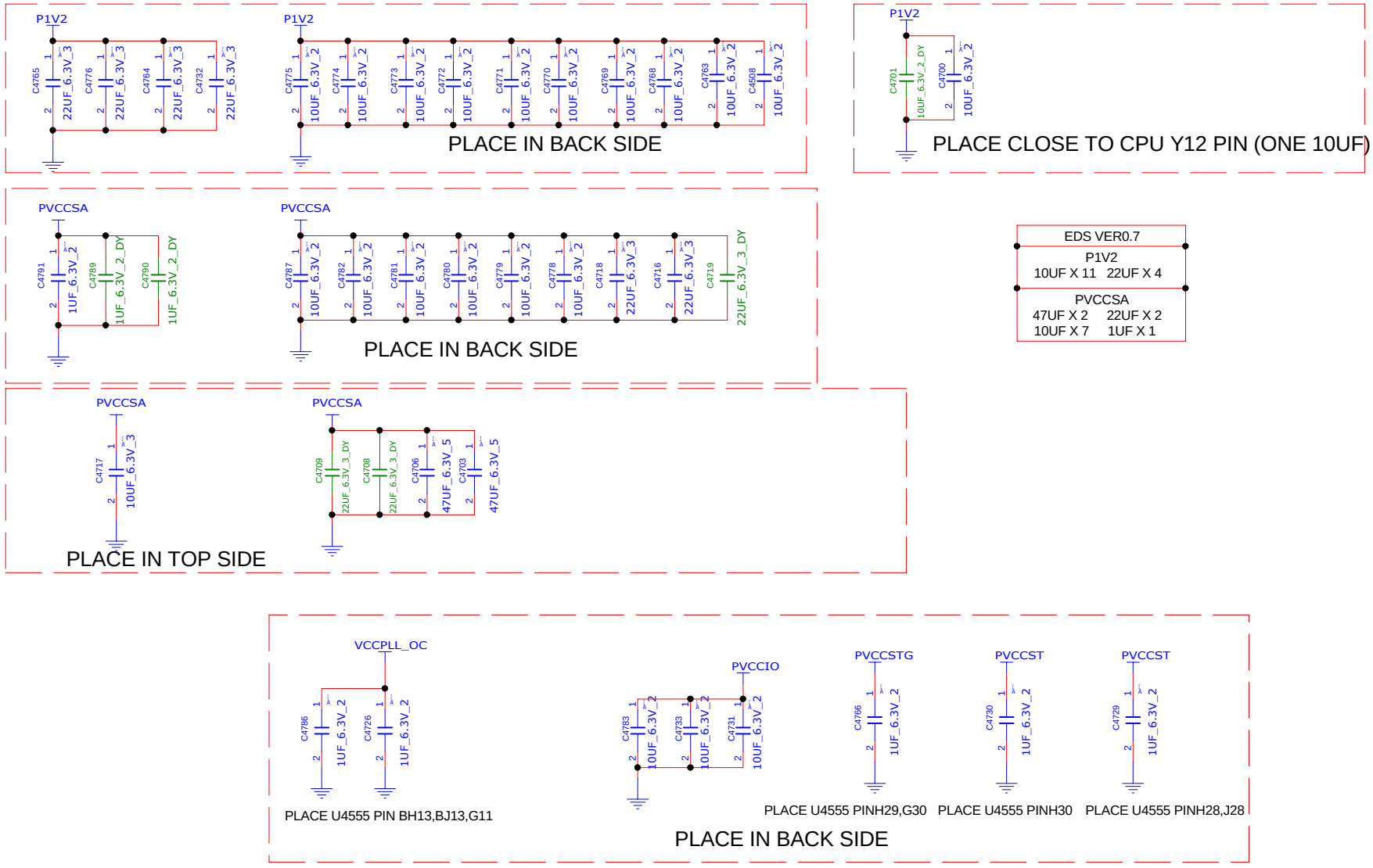

https://realschematic.com

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE8_H-DECOUPLING

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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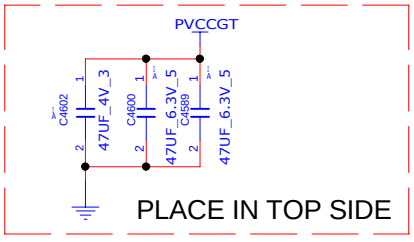
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

EDS VER0.7

PVCCGT
47UF X 3 22UF X 7
10UF X 10 1UF X 12



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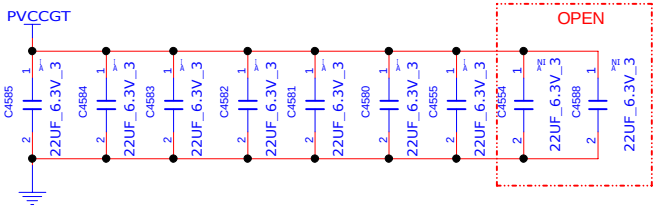
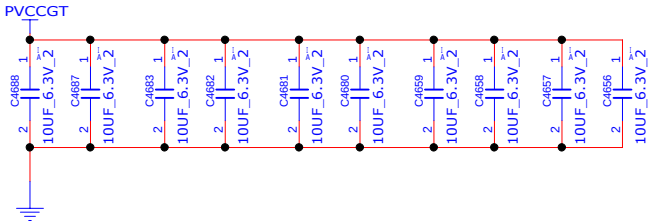
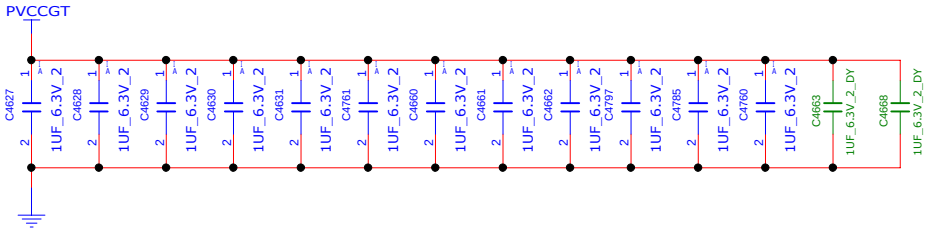
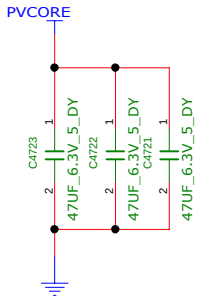


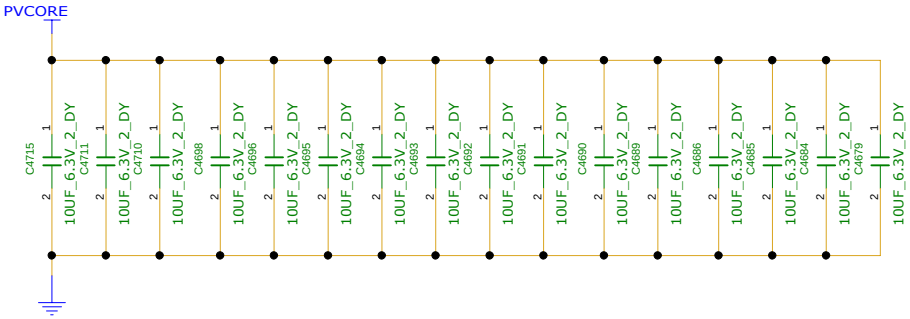
PLACE IN BACK SIDE

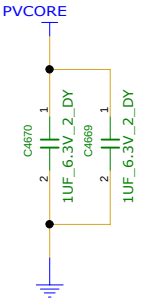




H82 CPU



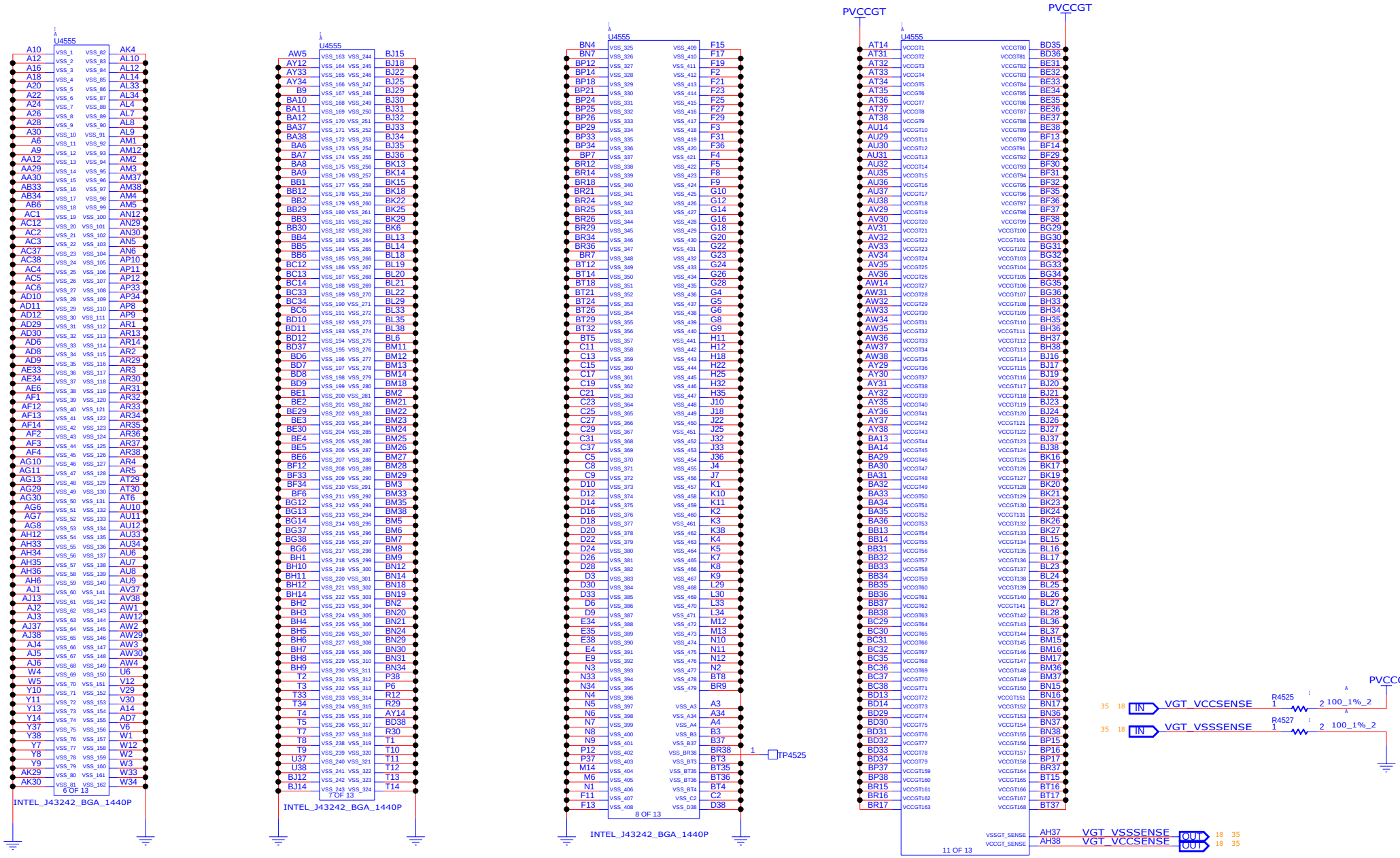




INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE9_H-GT *DECOUPLING		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 34 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE10_H-GND

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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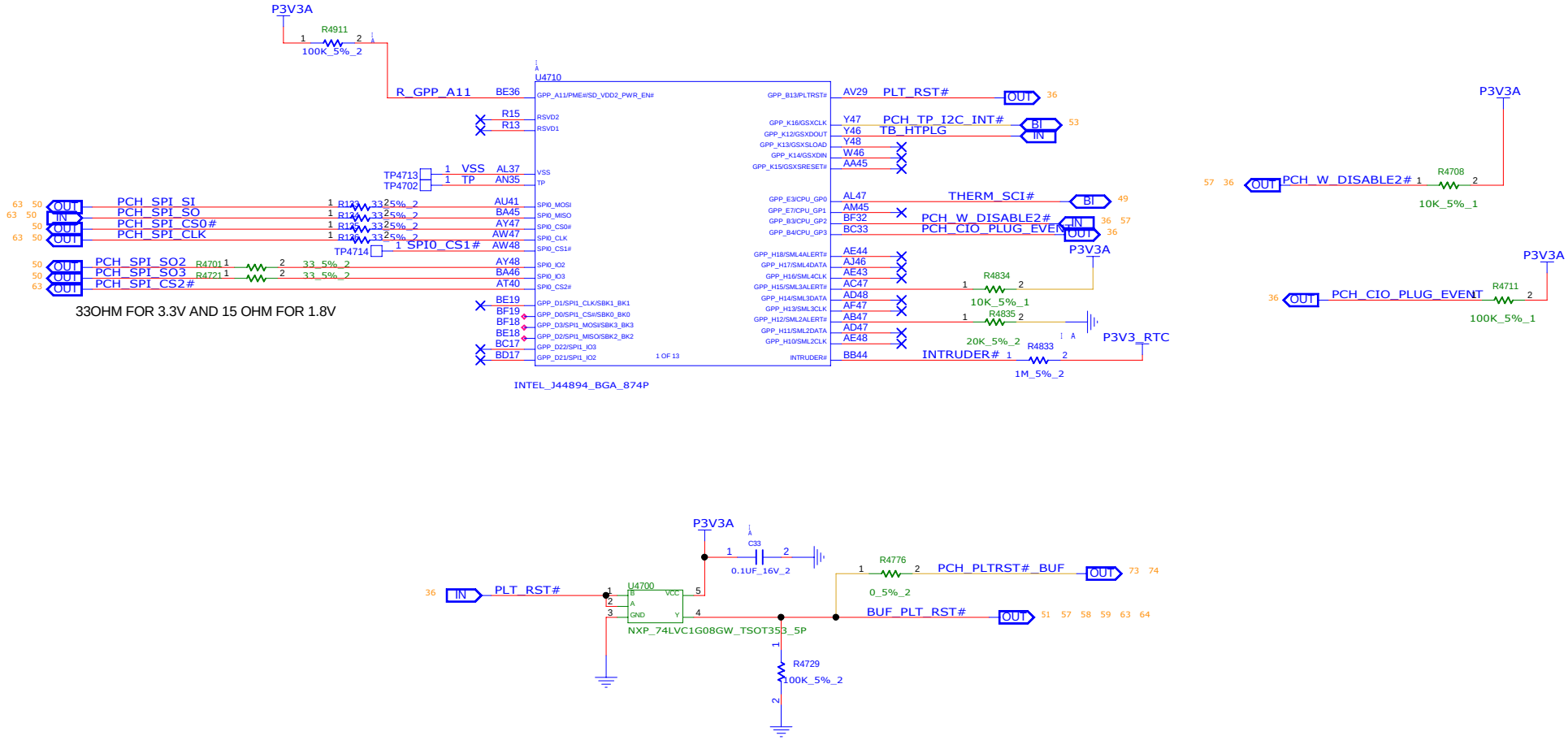

https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-SPI,GPP

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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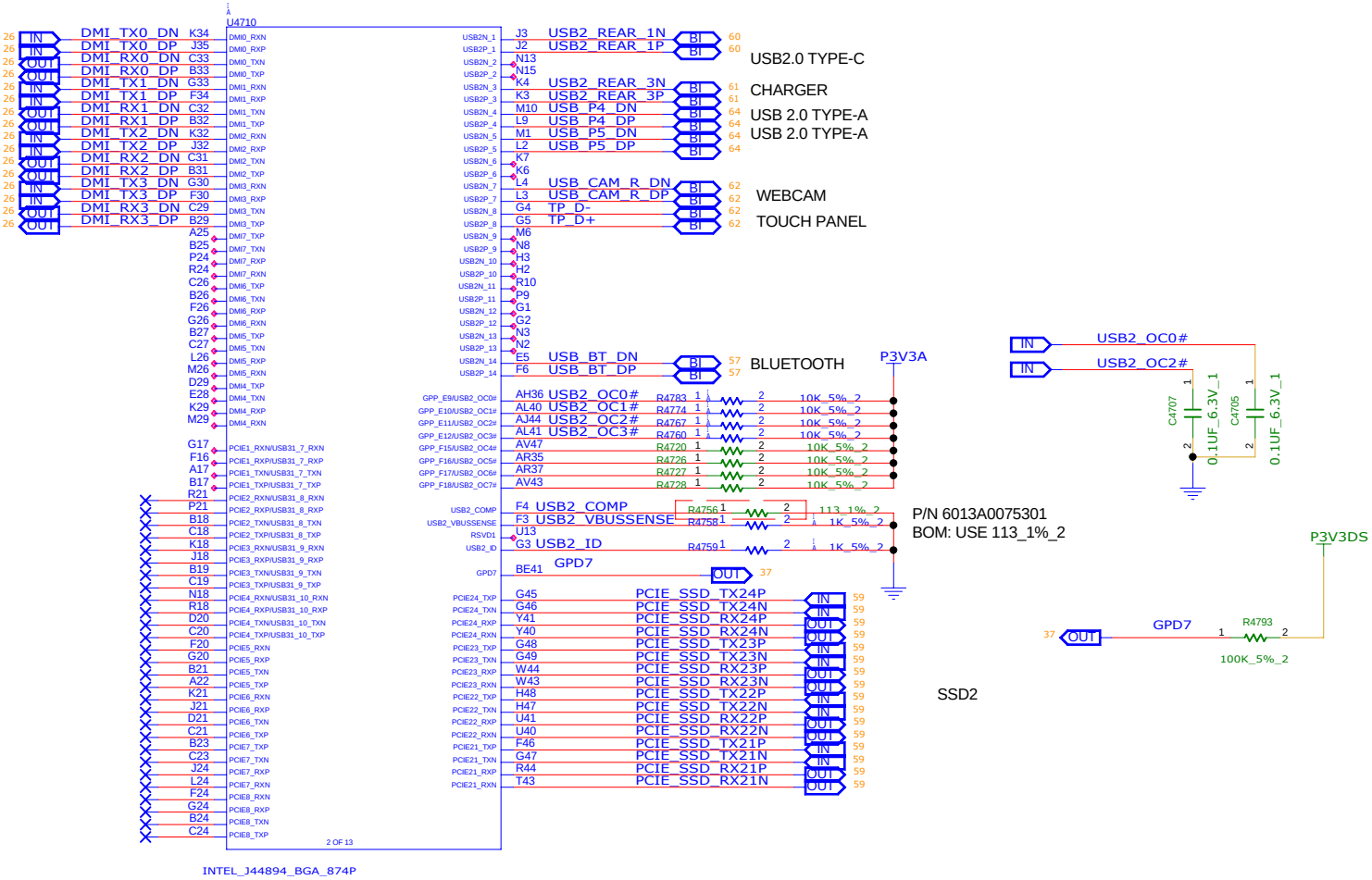
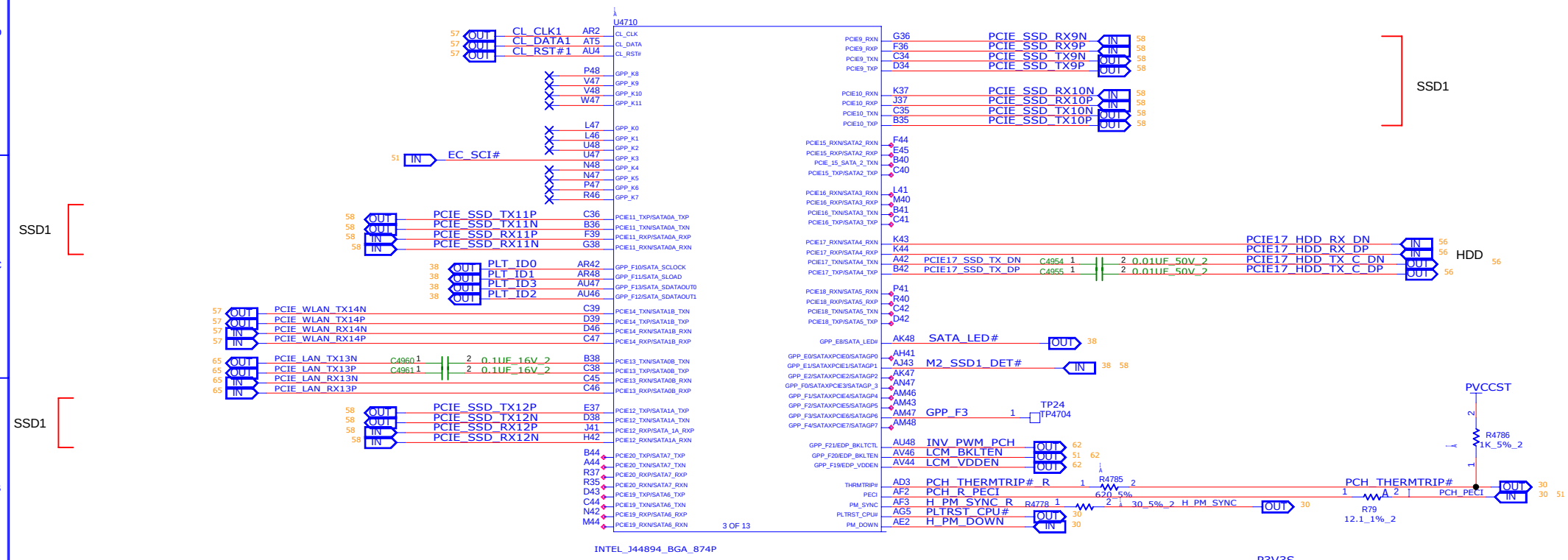


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PCH-DMI,USB2,USB3		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 37 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



	PLT_ID0	PLT_ID1	GPU
GPU	0	0	N18E-G2
	0	1	N18E-G1
	1	0	N18E-G0

	PLT_ID2	PLT_ID3	Size
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

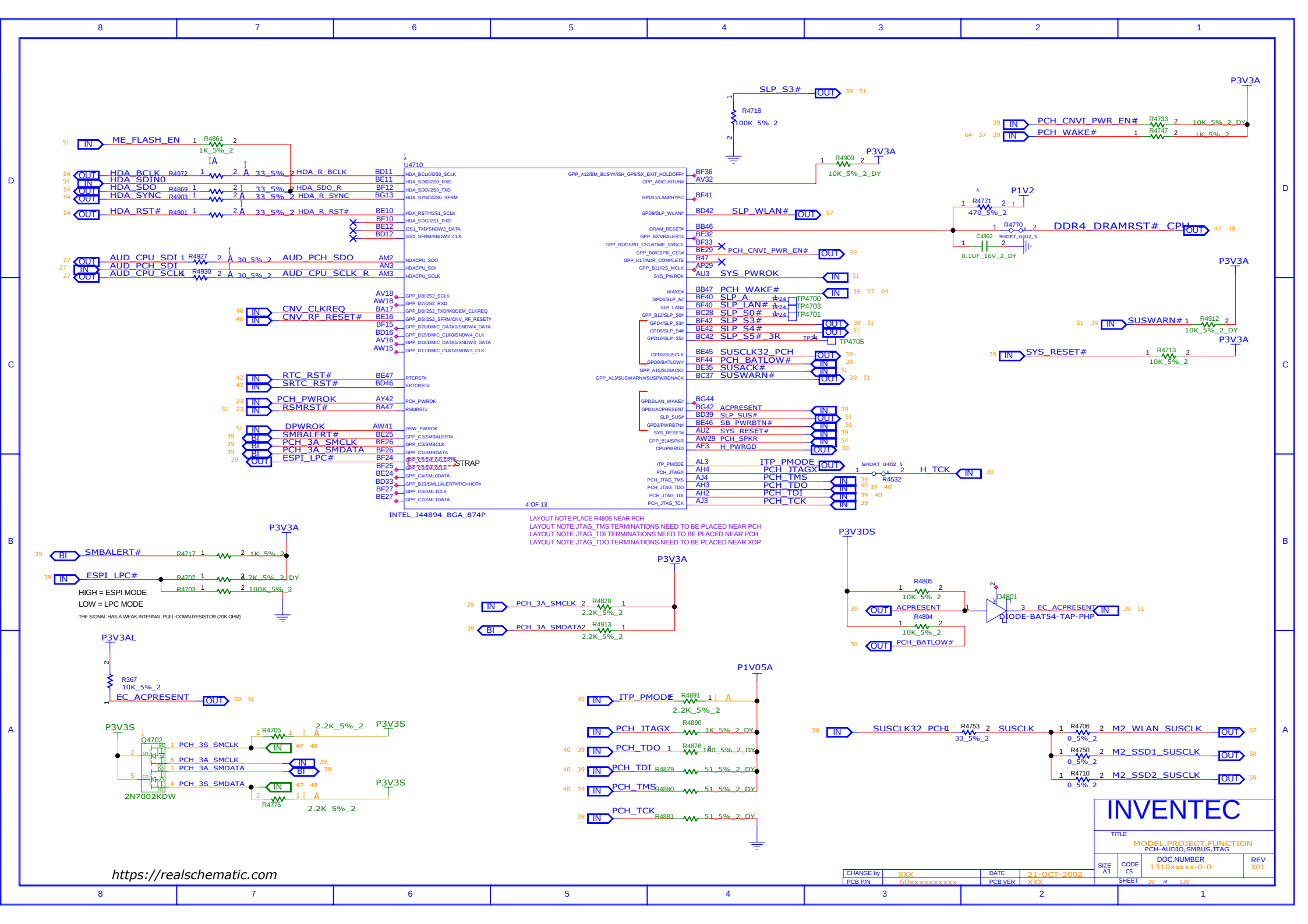
INVENTEC

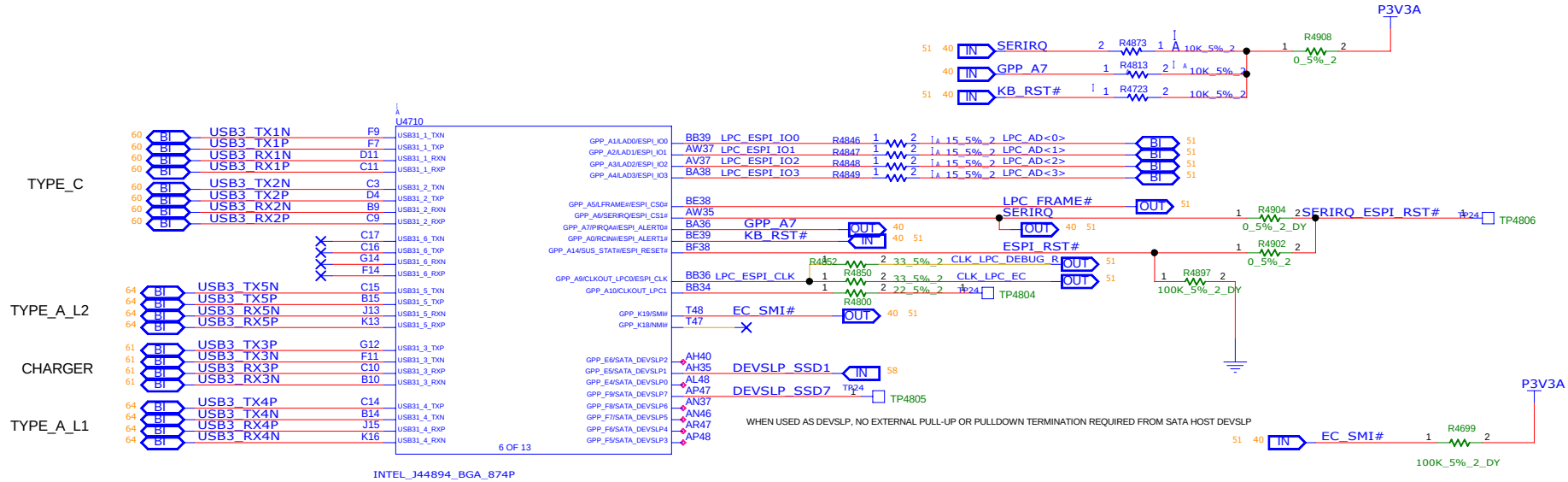
TITLE: MODEL,PROJECT,FUNCTION
PCH-CLINK,FAN,PCIE/SATA,HOST

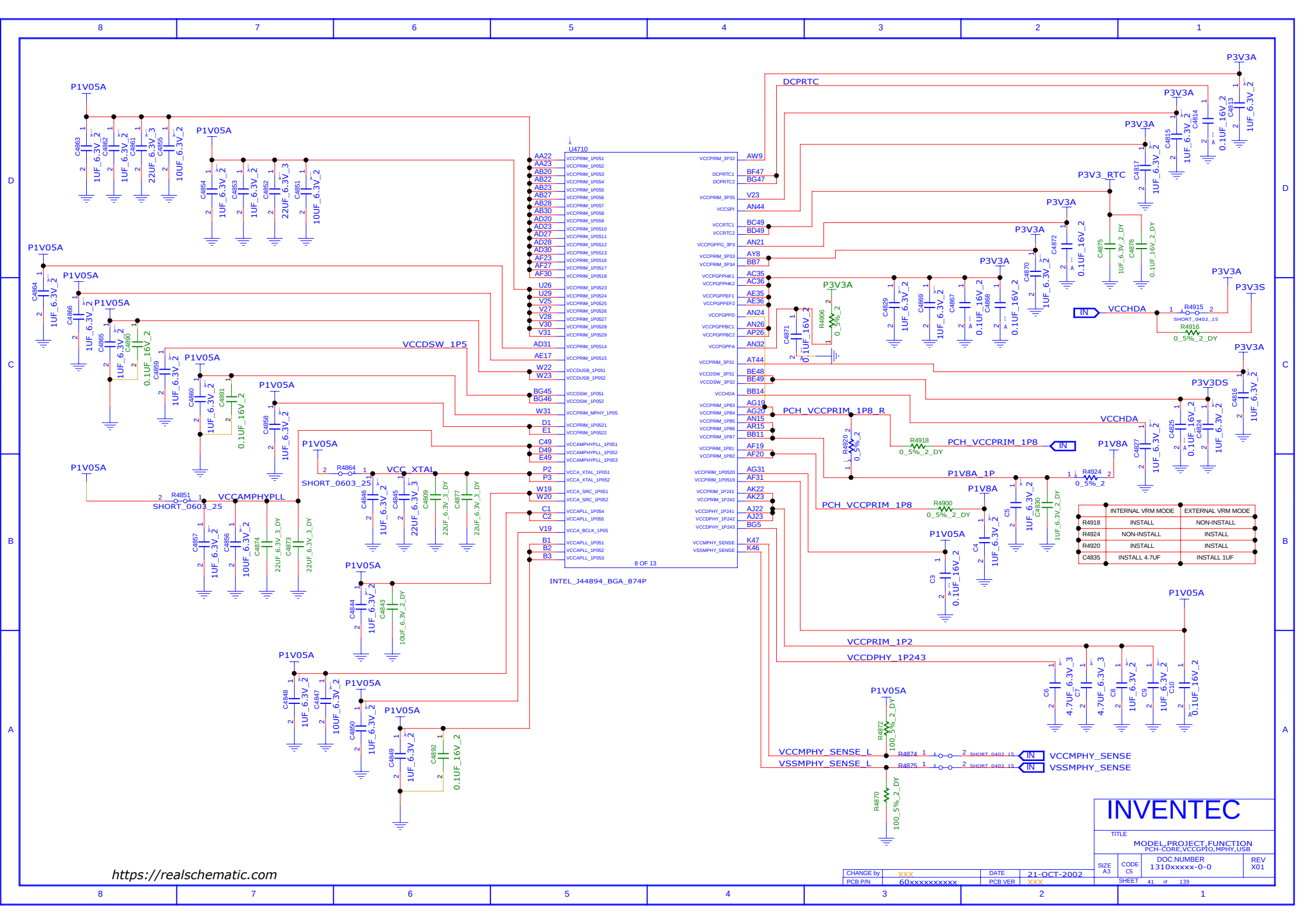
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

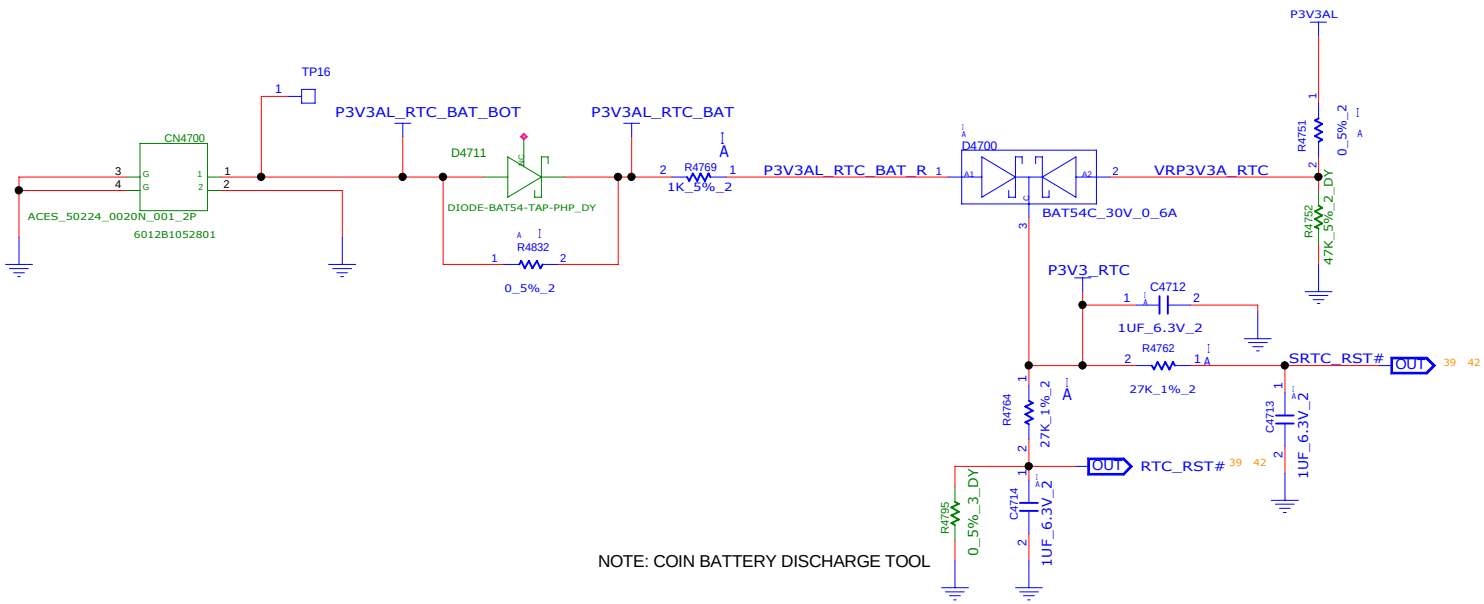
SHEET 38 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX


ME_FLASH_EN
HDA_BCLK
HDA_SDIN0
HDA_SDO
HDA_SYNC
HDA_RST#
AUD_CPU_SDI
AUD_PCH_SDI
AUD_CPU_SCLK
AUD_PCH_SDO
AUD_CPU_SCLK_R
CNV_CLKREQ
CNV_RF_RESET#
RTC_RST#
SRTC_RST#
PCH_PWROK
RSMRST#
DPWROK
SMBALERT#
PCH_3A_SMCLK
PCH_3A_SMDATA
ESPI_LPC#
STRAP
U4710
INTEL_J44894_BGA_874P
4 OF 13
SLP_S3#
SLP_WLAN#
PCH_CNVI_PWR_EN#
PCH_WAKE#
SYS_PWROK
SLP_A
SLP_LAN#
SLP_S0#
SLP_S3#
SLP_S4#
SLP_S5#_3R
SUSCLK32_PCH
PCH_BATLOW#
SUSWARN#
ACPRESENT
SLP_SUS#
SB_PWRBTN#
SYS_RESET#
PCH_SPKR
H_PWRGD
ITP_PMODE
PCH_JTAGX
PCH_TMS
PCH_TDO
PCH_TDI
PCH_TCK
DDR4_DRAMRST#_CPU
SUSWARN#
SYS_RESET#
H_TCK
EC_ACPRESENT
M2_WLAN_SUSCLK
M2_SSD1_SUSCLK
M2_SSD2_SUSCLK
SUSCLK
2N7002KDW
P3V3A
P3V3AL
P3V3S
P3V3DS
P1V2
P1V05A
HIGH = ESPI MODE
LOW = LPC MODE
THE SIGNAL HAS A WEAK INTERNAL PULL-DOWN RESISTOR.(20K OHM)
LAYOUT NOTE:PLACE R4808 NEAR PCH
LAYOUT NOTE:JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE:JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE:JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
INVENTEC
MODEL,PROJECT,FUNCTION
PCH-AUDIO,SMBUS,JTAG
DOC.NUMBER
1310xxxxx-0-0
REV
X01
CHANGE by
XXX
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxxx
PCB VER
XXX
SHEET
39 of 139
https://realschematic.com

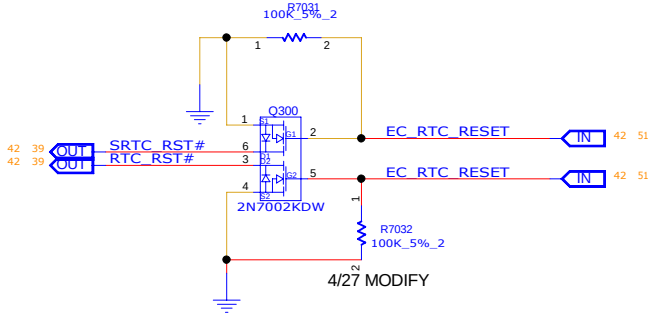



U4710
INTEL_J44894_BGA_874P
8 OF 13
P1V05A
P3V3A
P3V3_RTC
P3V3S
P3V3DS
P1V8A
P1V8A_1P
DCPRTC
VCCDSW_1P5
VCC_XTAL
VCCAMPHYPLL
PCH_VCCPRIM_1P8_R
PCH_VCCPRIM_1P8
VCCHDA
VCCPRIM_1P2
VCCDPHY_1P243
VCCMPHY_SENSE_L
VSSMPHY_SENSE_L
VCCMPHY_SENSE
VSSMPHY_SENSE
SHORT_0603_25
SHORT_0402_15
0_5%_2_DY
INTERNAL VRM MODE
EXTERNAL VRM MODE
R4918 INSTALL NON-INSTALL
R4924 NON-INSTALL INSTALL
R4920 INSTALL INSTALL
C4835 INSTALL 4.7UF INSTALL 1UF
INVENTEC
MODEL,PROJECT,FUNCTION
PCH-CORE,VCCGPIO,MPHY,USB
DOC.NUMBER 1310xxxxx-0-0
REV X01
SIZE A3
CODE CS
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX
SHEET 41 of 139
https://realschematic.com



NOTE: COIN BATTERY DISCHARGE TOOL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R4710	INSTAL	UNINSTAL
R4709	UNINSTAL	INSTAL



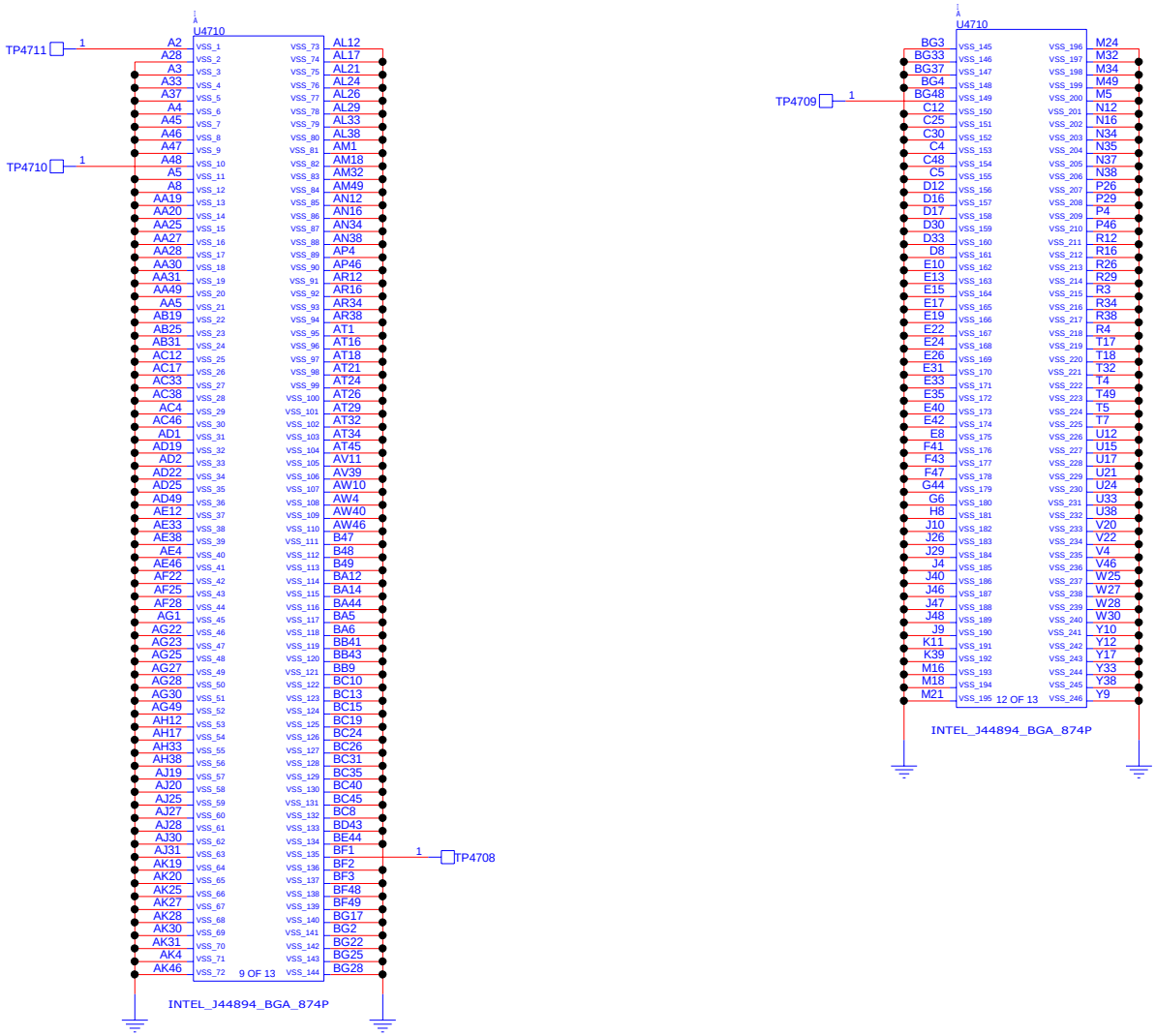
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 42 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GND

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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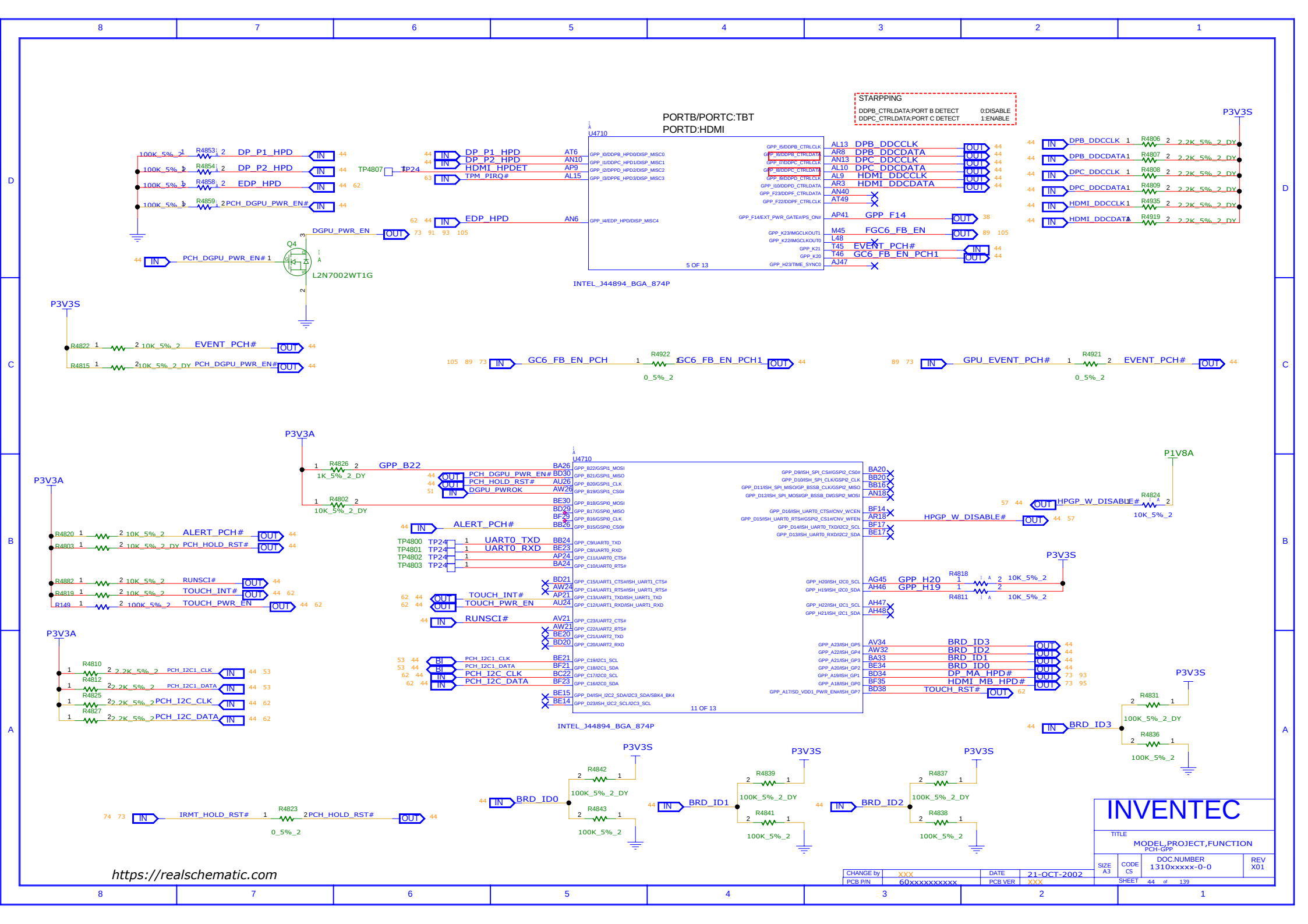
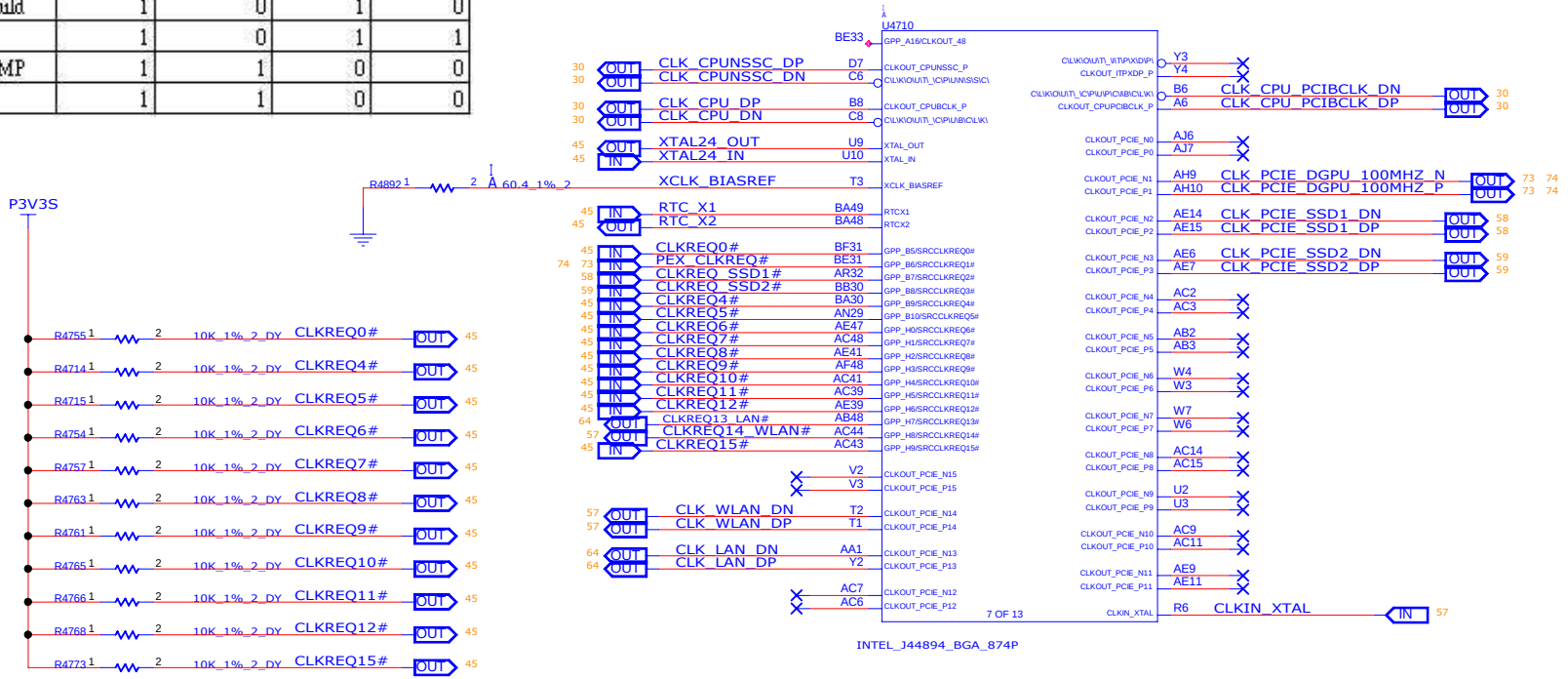
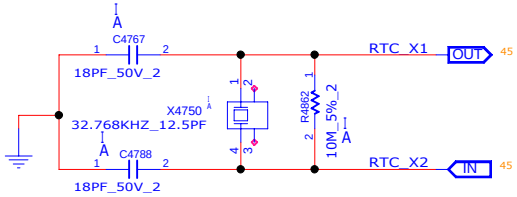
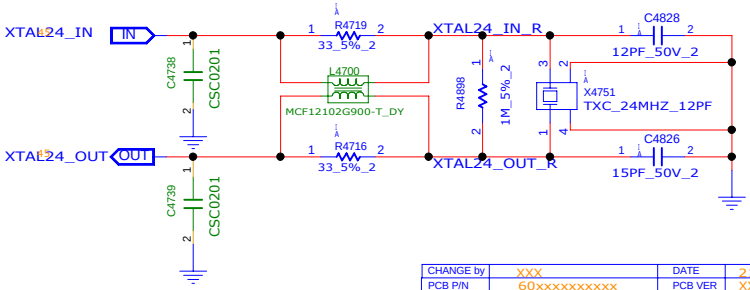

STARPPING
DDPB_CTRLDATA:PORT B DETECT 0:DISABLE
DDPC_CTRLDATA:PORT C DETECT 1:ENABLE
PORTB/PORTC:TBT
PORTD:HDMI
U4710
INTEL_J44894_BGA_874P
5 OF 13
11 OF 13
DP_P1_HPD
DP_P2_HPD
EDP_HPD
HDMI_HPDET
TPM_PIRQ#
PCH_DGPU_PWR_EN#
DGPU_PWR_EN
Q4
L2N7002WT1G
EVENT_PCH#
GC6_FB_EN_PCH
GC6_FB_EN_PCH1
GPU_EVENT_PCH#
GPP_B22
PCH_DGPU_PWR_EN#
PCH_HOLD_RST#
DGPU_PWROK
ALERT_PCH#
UART0_TXD
UART0_RXD
TOUCH_INT#
TOUCH_PWR_EN
RUNSCI#
PCH_I2C1_CLK
PCH_I2C1_DATA
PCH_I2C_CLK
PCH_I2C_DATA
IRMT_HOLD_RST#
DPB_DDCCLK
DPB_DDCDATA
DPC_DDCCLK
DPC_DDCDATA
HDMI_DDCCLK
HDMI_DDCDATA
GPP_F14
FGC6_FB_EN
HPGP_W_DISABLE#
BRD_ID3
BRD_ID2
BRD_ID1
BRD_ID0
DP_MA_HPD#
HDMI_MB_HPD#
TOUCH_RST#
P3V3S
P3V3A
P1V8A
INVENTEC
MODEL_PROJECT,FUNCTION
PCH-GPP
DOC.NUMBER
1310xxxxx-0-0
REV X01
SIZE A3
CODE CS
SHEET 44 of 139
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx
PCB VER XXX
https://realschematic.com

	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	0	1
D build	1	0	1	0
	1	0	1	1
Pre-MP	1	1	0	0
MP	1	1	0	0

1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GPP,CLKOUT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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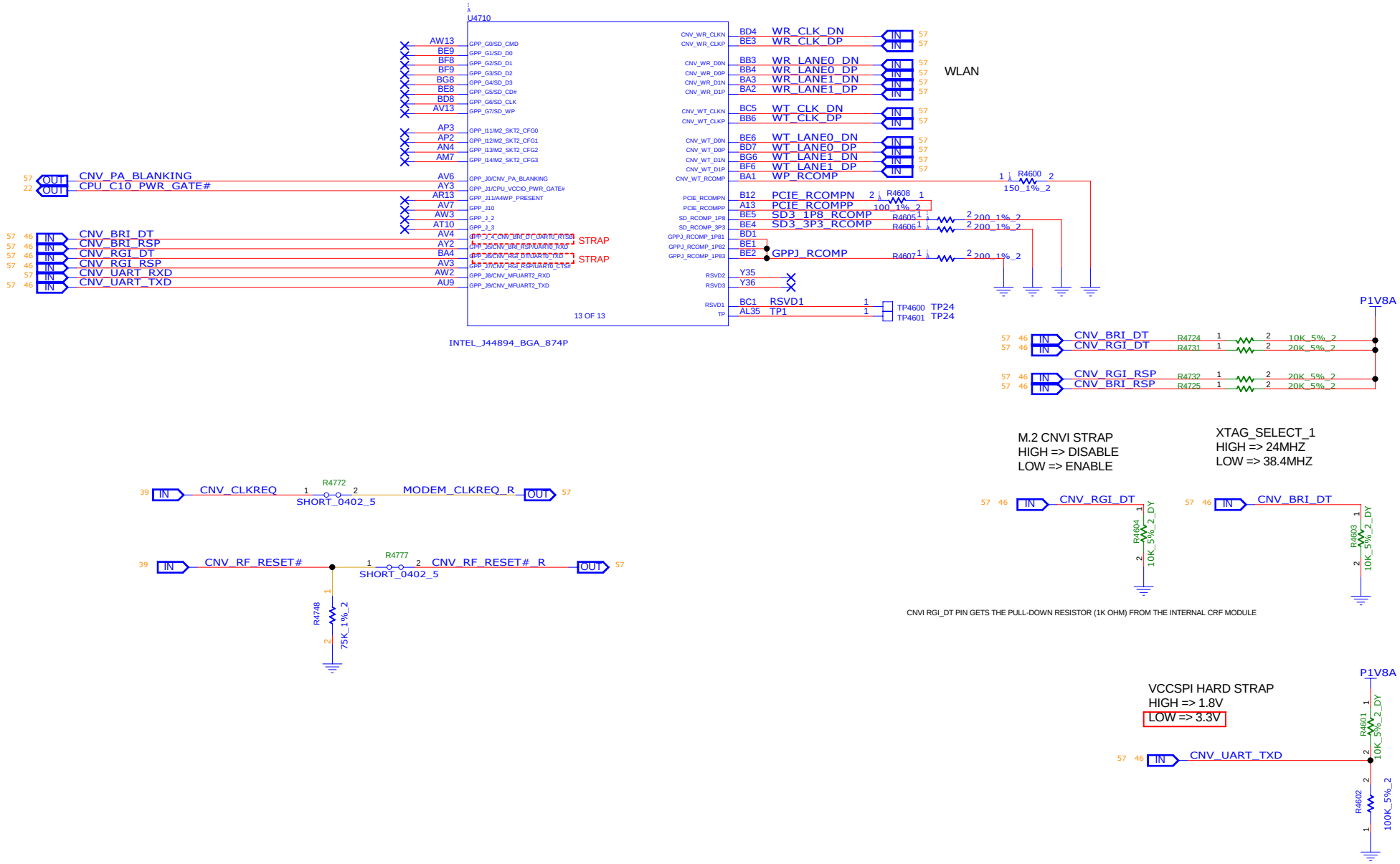
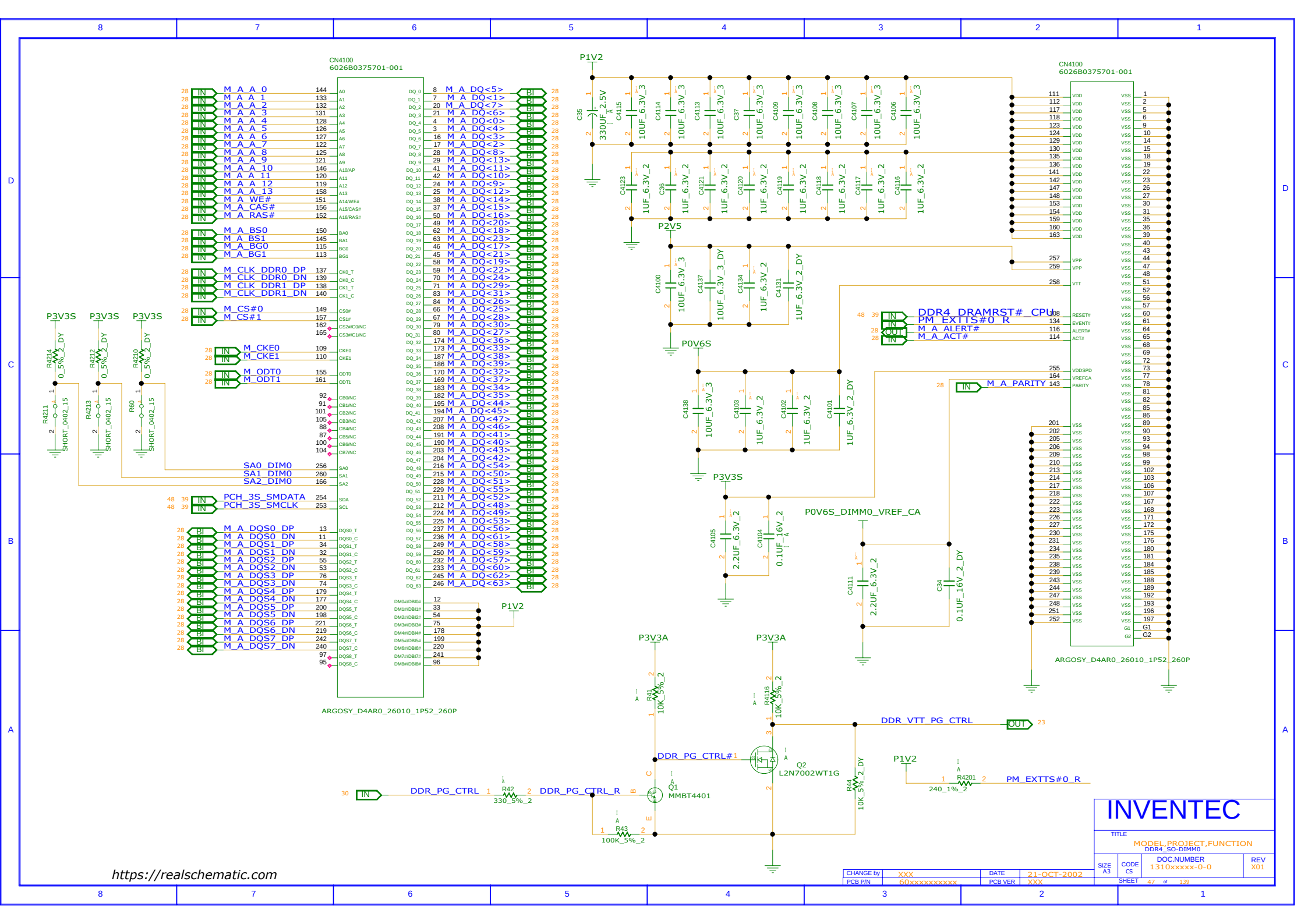
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX


U4710
INTEL_J44894_BGA_874P
13 OF 13
WLAN
CNV_PA_BLANKING
CPU_C10_PWR_GATE#
CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
CNV_UART_RXD
CNV_UART_TXD
STRAP
STRAP
WR_CLK_DN
WR_CLK_DP
WR_LANE0_DN
WR_LANE0_DP
WR_LANE1_DN
WR_LANE1_DP
WT_CLK_DN
WT_CLK_DP
WT_LANE0_DN
WT_LANE0_DP
WT_LANE1_DN
WT_LANE1_DP
WP_RCOMP
PCIE_RCOMPN
PCIE_RCOMPP
SD3_1P8_RCOMP
SD3_3P3_RCOMP
GPPJ_RCOMP
RSVD1
TP1
TP24
P1V8A
M.2 CNVI STRAP
HIGH => DISABLE
LOW => ENABLE
XTAG_SELECT_1
HIGH => 24MHZ
LOW => 38.4MHZ
CNV_CLKREQ
MODEM_CLKREQ_R
SHORT_0402_5
CNV_RF_RESET#
CNV_RF_RESET#_R
CNVI RGI_DT PIN GETS THE PULL-DOWN RESISTOR (1K OHM) FROM THE INTERNAL CRF MODULE
VCCSPI HARD STRAP
HIGH => 1.8V
LOW => 3.3V
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SHEET 46 of 139
https://realschematic.com


CN4100
6026B0375701-001
M_A_A_0
M_A_A_1
M_A_A_2
M_A_A_3
M_A_A_4
M_A_A_5
M_A_A_6
M_A_A_7
M_A_A_8
M_A_A_9
M_A_A_10
M_A_A_11
M_A_A_12
M_A_A_13
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_BS0
M_A_BS1
M_A_BG0
M_A_BG1
M_CLK_DDR0_DP
M_CLK_DDR0_DN
M_CLK_DDR1_DP
M_CLK_DDR1_DN
M_CS#0
M_CS#1
M_CKE0
M_CKE1
M_ODT0
M_ODT1
SA0_DIM0
SA1_DIM0
SA2_DIM0
PCH_3S_SMDATA
PCH_3S_SMCLK
M_A_DQS0_DP
M_A_DQS0_DN
M_A_DQS1_DP
M_A_DQS1_DN
M_A_DQS2_DP
M_A_DQS2_DN
M_A_DQS3_DP
M_A_DQS3_DN
M_A_DQS4_DP
M_A_DQS4_DN
M_A_DQS5_DP
M_A_DQS5_DN
M_A_DQS6_DP
M_A_DQS6_DN
M_A_DQS7_DP
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M_A_DQ<1>
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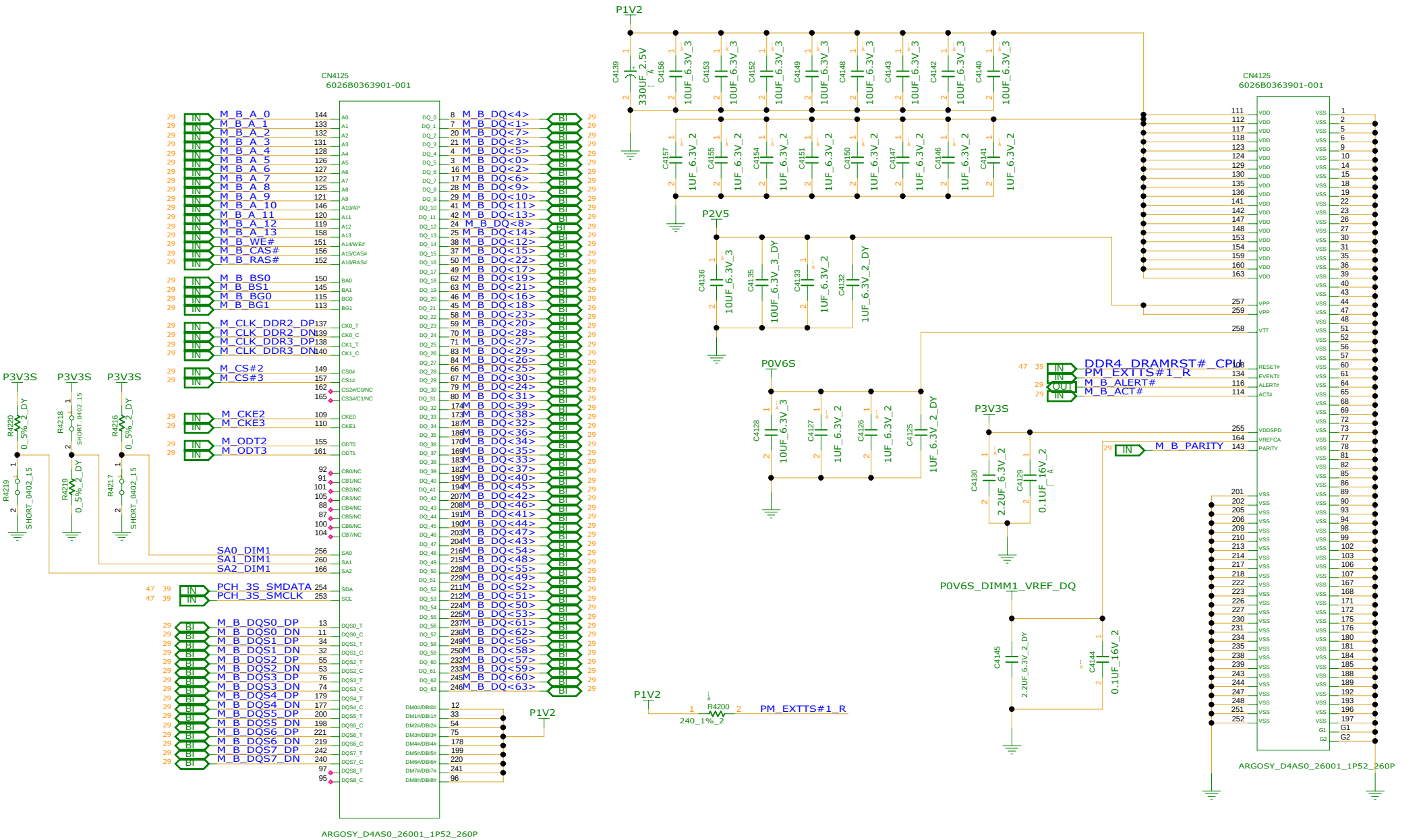
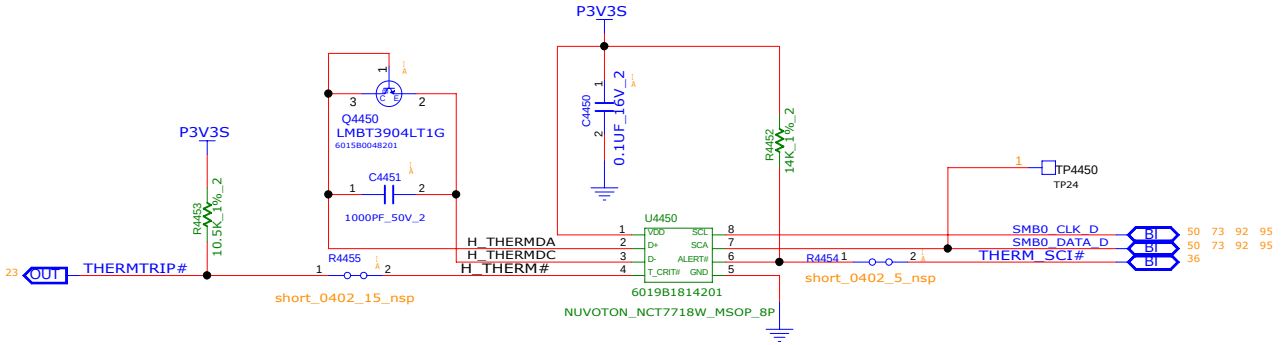
ARGOSY_D4AR0_26010_1P52_260P
P3V3S
R4214 0_5%_2_DY
R4212 0_5%_2_DY
R4210 0_5%_2_DY
R4211 SHORT_0402_15
R4213 SHORT_0402_15
R60 SHORT_0402_15
P1V2
P2V5
P0V6S
P3V3A
C35 330UF_2.5V
C4115 10UF_6.3V_3
C4114 10UF_6.3V_3
C4113 10UF_6.3V_3
C37 10UF_6.3V_3
C4109 10UF_6.3V_3
C4108 10UF_6.3V_3
C4107 10UF_6.3V_3
C4106 10UF_6.3V_3
C4123 1UF_6.3V_2
C36 1UF_6.3V_2
C4121 1UF_6.3V_2
C4120 1UF_6.3V_2
C4119 1UF_6.3V_2
C4118 1UF_6.3V_2
C4117 1UF_6.3V_2
C4116 1UF_6.3V_2
C4100 10UF_6.3V_3
C4137 10UF_6.3V_3_DY
C4134 1UF_6.3V_2
C4131 1UF_6.3V_2_DY
C4138 10UF_6.3V_3
C4103 1UF_6.3V_2
C4102 1UF_6.3V_2
C4101 1UF_6.3V_2_DY
C4105 2.2UF_6.3V_2
C4104 0.1UF_16V_2
C4111 2.2UF_6.3V_2
C34 0.1UF_16V_2_DY
DDR4_DRAMRST#_CPU
PM_EXTTS#0_R
M_A_ALERT#
M_A_ACT#
M_A_PARITY
P0V6S_DIMM0_VREF_CA
DDR_VTT_PG_CTRL
DDR_PG_CTRL
DDR_PG_CTRL_R
DDR_PG_CTRL#1
R42 330_5%_2
R43 100K_5%_2
R41 10K_5%_2
R4116 10K_5%_2
R44 10K_5%_2_DY
R4201 240_1%_2
Q1 MMBT4401
Q2 L2N7002WT1G
CN4100
6026B0375701-001
ARGOSY_D4AR0_26010_1P52_260P
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
DDR4_SO-DIMM0
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 47 of 139
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx
PCB VER XXX
https://realschematic.com



REFERENCE NUMBER:4450~4499

THERM SENSOR



INVENTEC

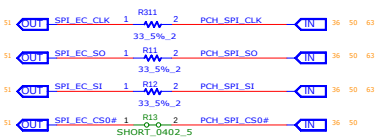
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

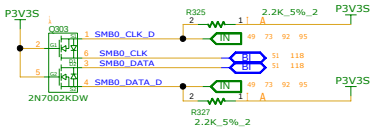
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 49 of 139

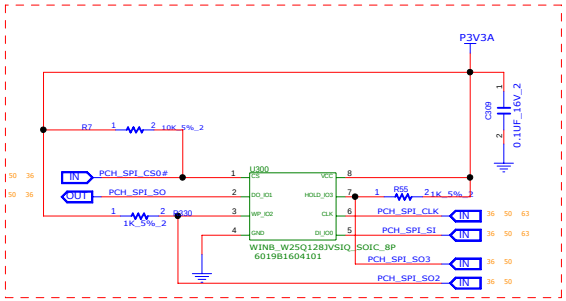
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

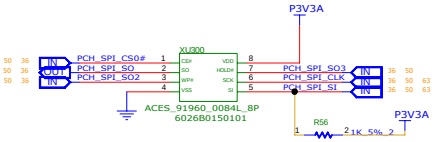
REFERENCE 300~389(KBC)





THERMAL SENSOR
HDMI
DP





R390 FOR INTEL DEBUG

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60Dxxxxxxxxx	PCB VER	XXX

EC

Location 300 ~ 389

2013EE1B

Ver.05_20120824

	VCC(1.8V OR 3.3V)	VSTBY_FSPI(1.8V OR 3.3V)
IT8987E_CX	PIN13 : LPCCLK/GPM4(3) PIN10 : LAD0/GPM0(3) PIN9 : LAD1/GPM1(3) PIN8 : LAD2/GPM2(3) PIN7 : LAD3/GPM3(3) PIN6 : LFRAME#/GPM5(3)	PIN5 : SERIRQ/GPM6(3) PIN105 : FSCK/GPG7 PIN101 : FSCE#/GPG3 PIN102 : FMOSI/GPG4 PIN103 : FMISO/GPG5

FOR DPTF

Intel DS3 function support

U1

ITE_IT8987E_CX_LQFP_128P_HP

6019B1650401

C314 For Intel platform

noise cap

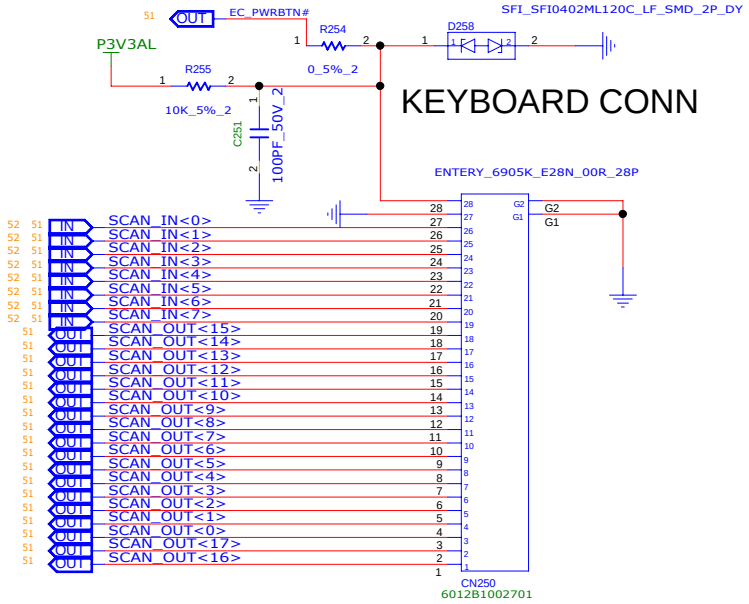
https://realschematic.com

INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

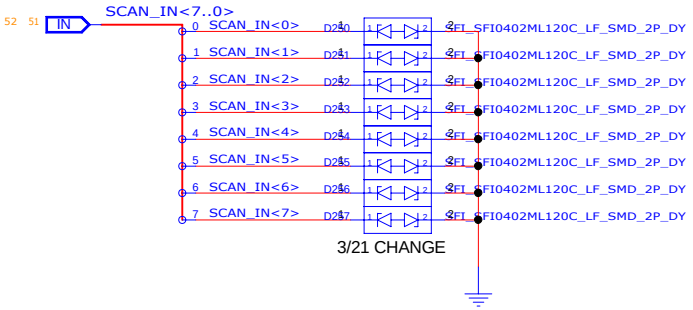
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



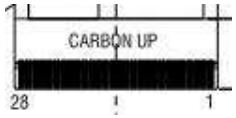
KEYBOARD CONN

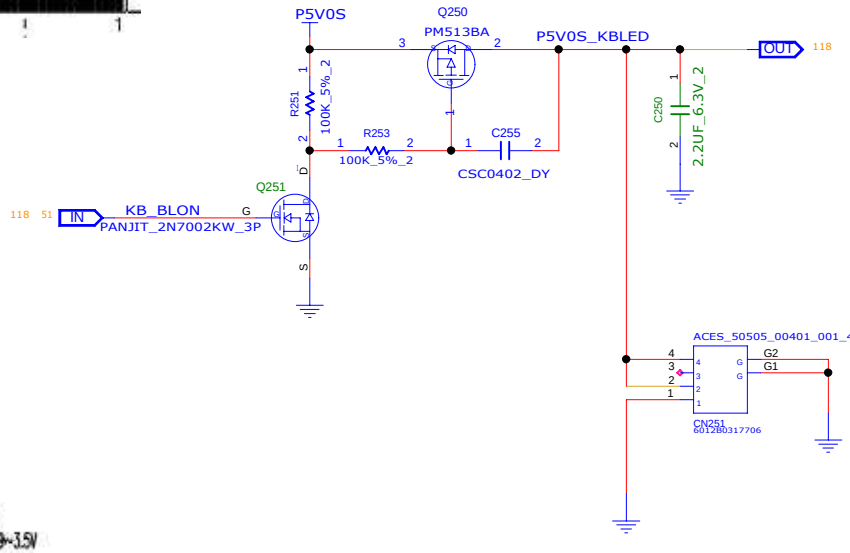
NEE TO CHANGE 6012B1002701
5/2 REVERSE

	14"
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



3/21 CHANGE





KEYBOARD LED CONN

VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

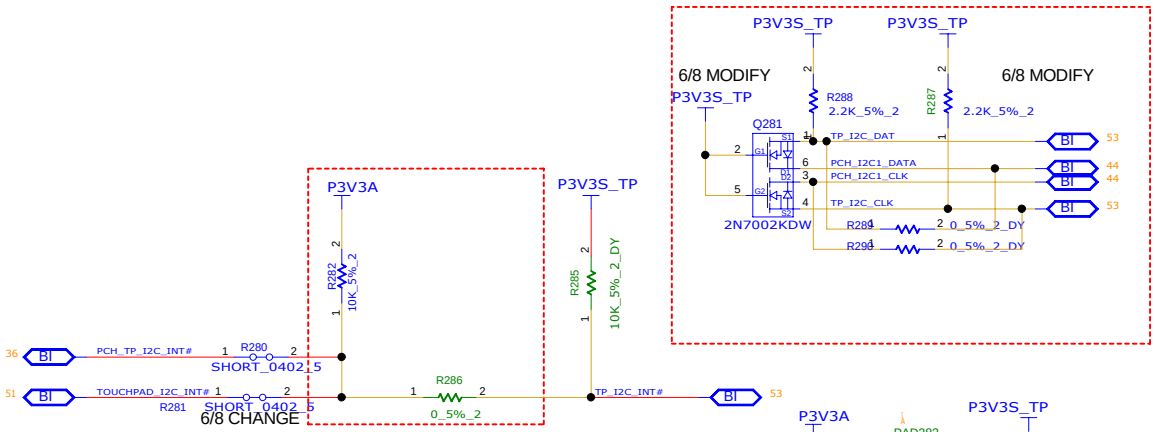
INVENTEC

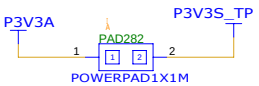
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

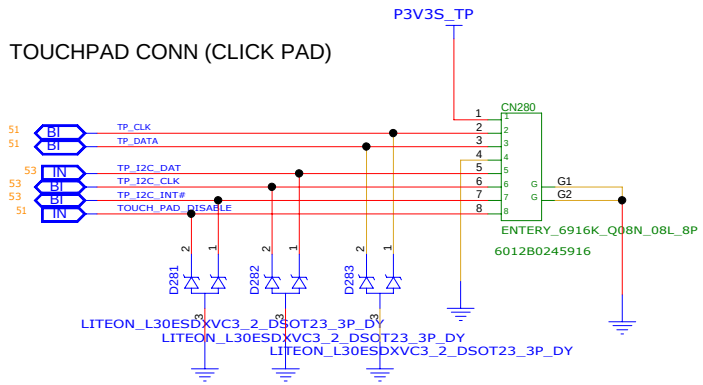
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 52 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX







https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

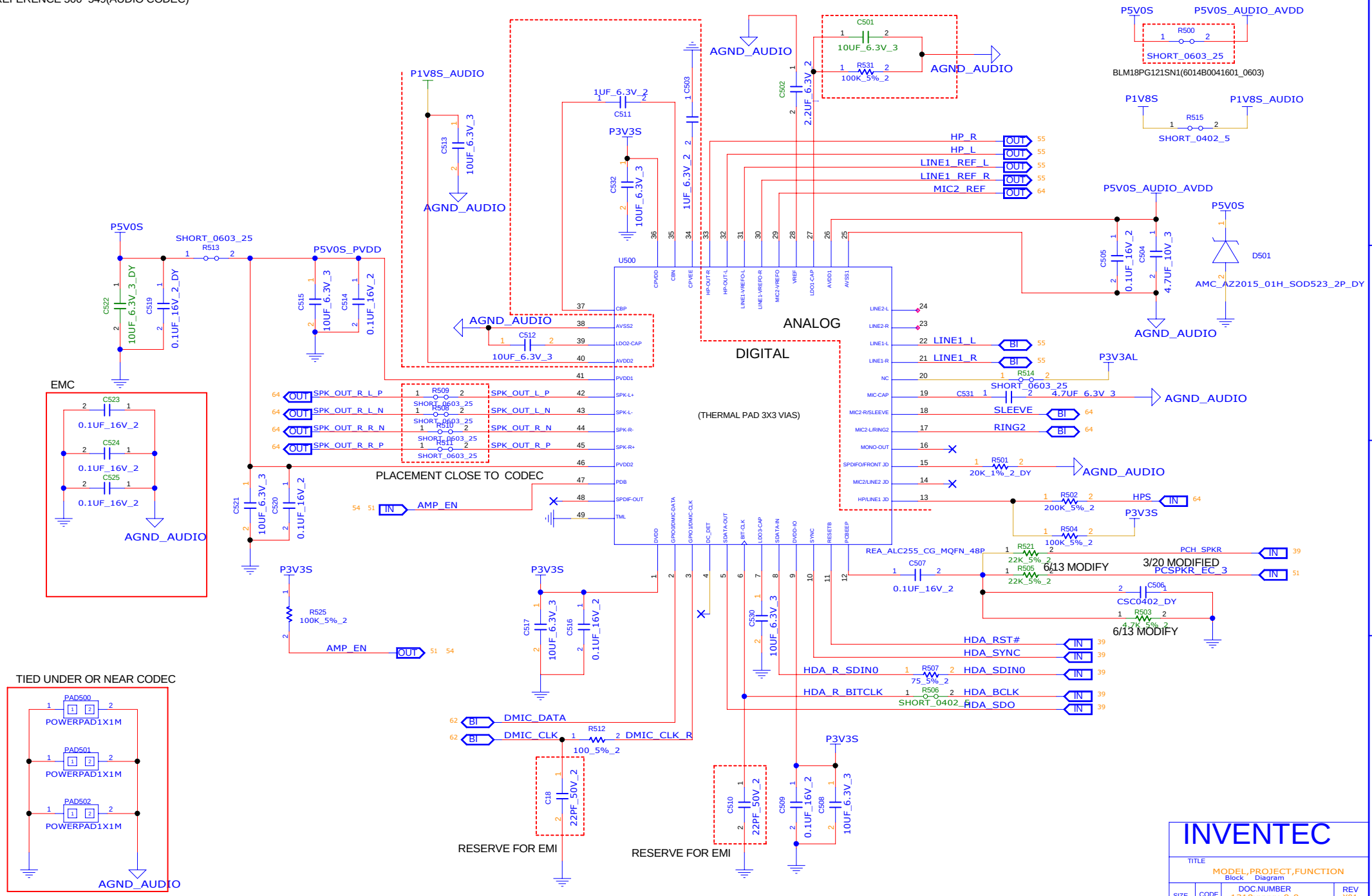
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

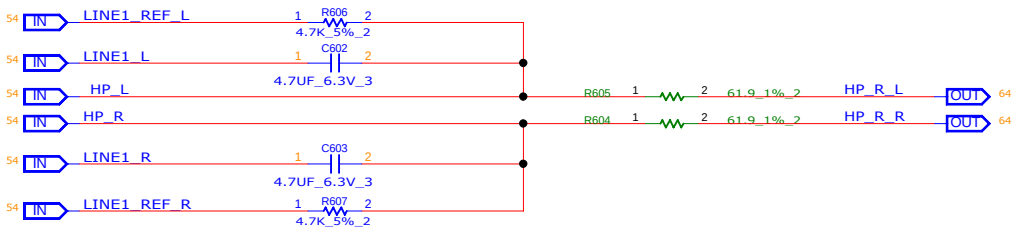
SHEET 53 of 139

REFERENCE 500~549(AUDIO CODEC)



REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

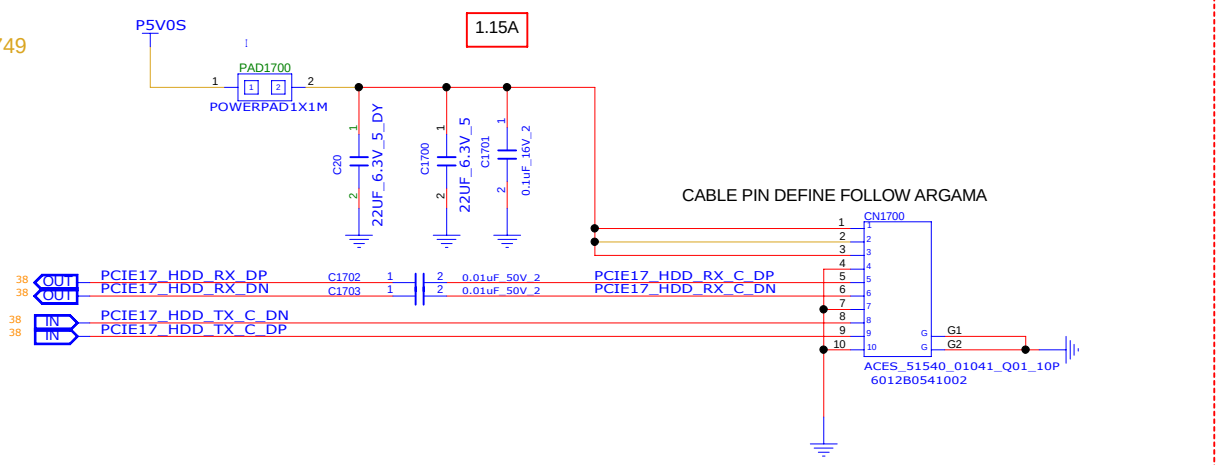
TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 55 of 139

SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

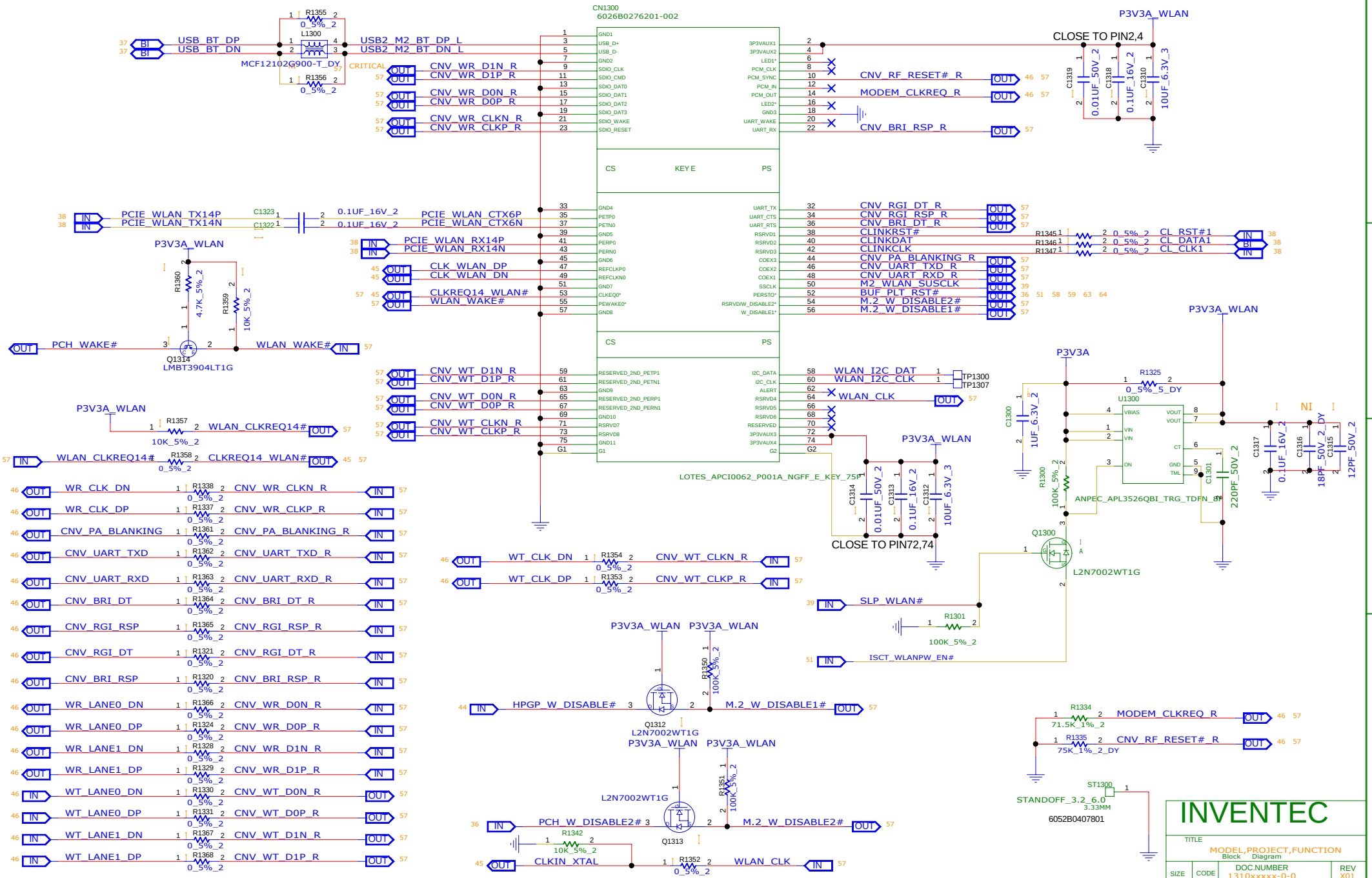
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

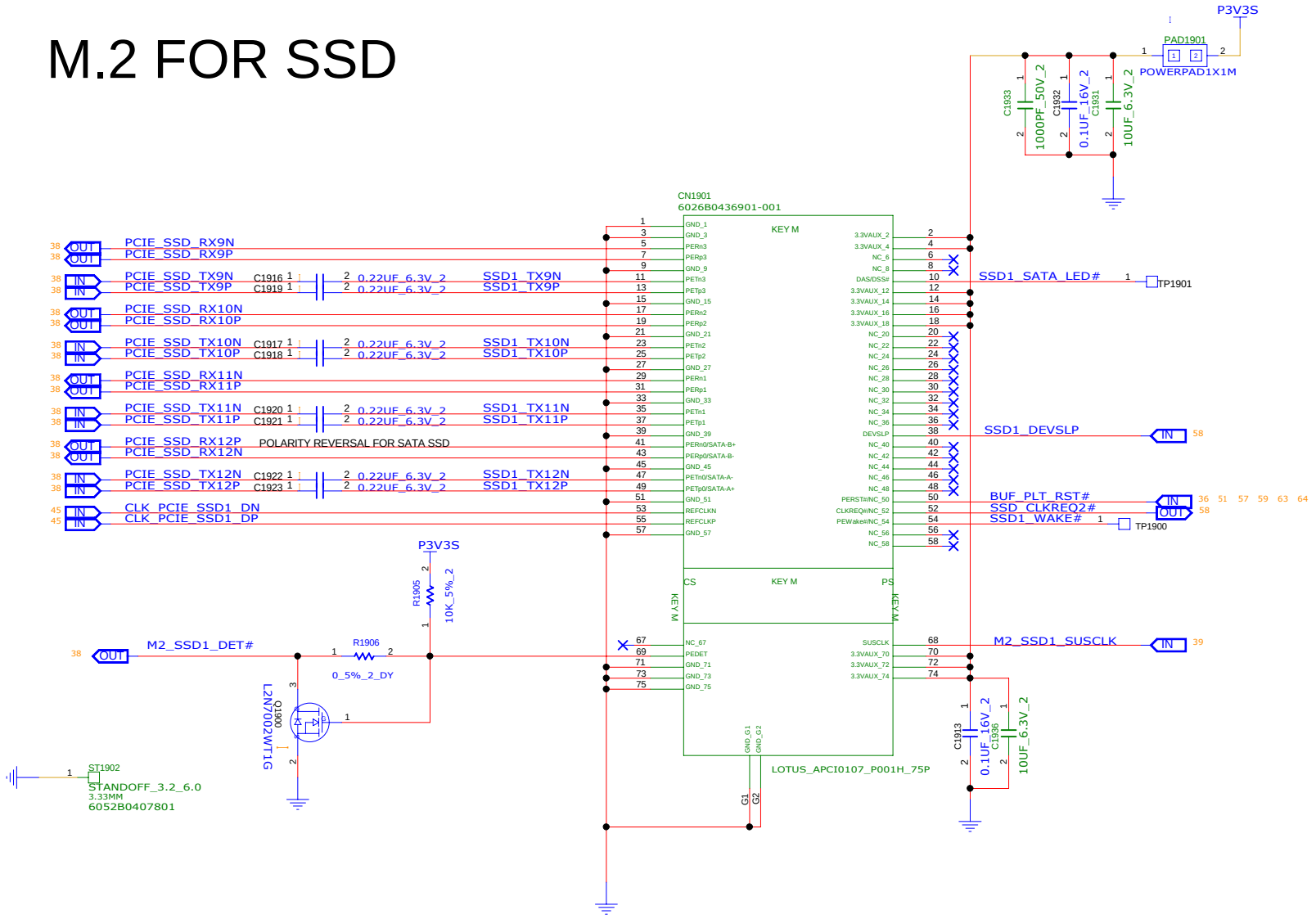
SHEET 56 of 139

M.2 FOR WLAN/BT



https://realschematic.com

M.2 FOR SSD



https://realschematic.com

INVENTEC

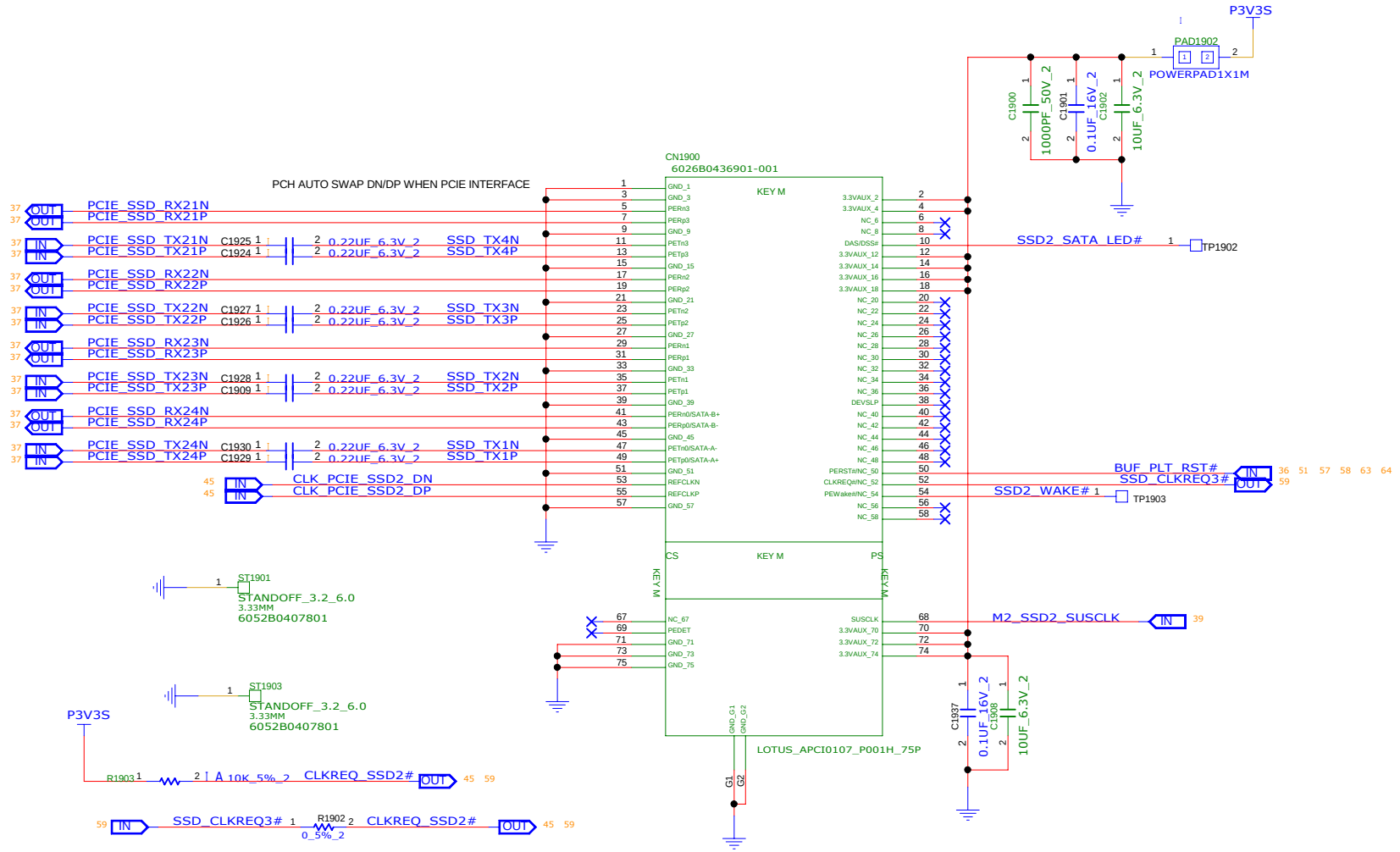
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 58 of 139

NGFF SSD2(PCIE/SATA 2X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

REFERENCE NUMBER:1950~1999

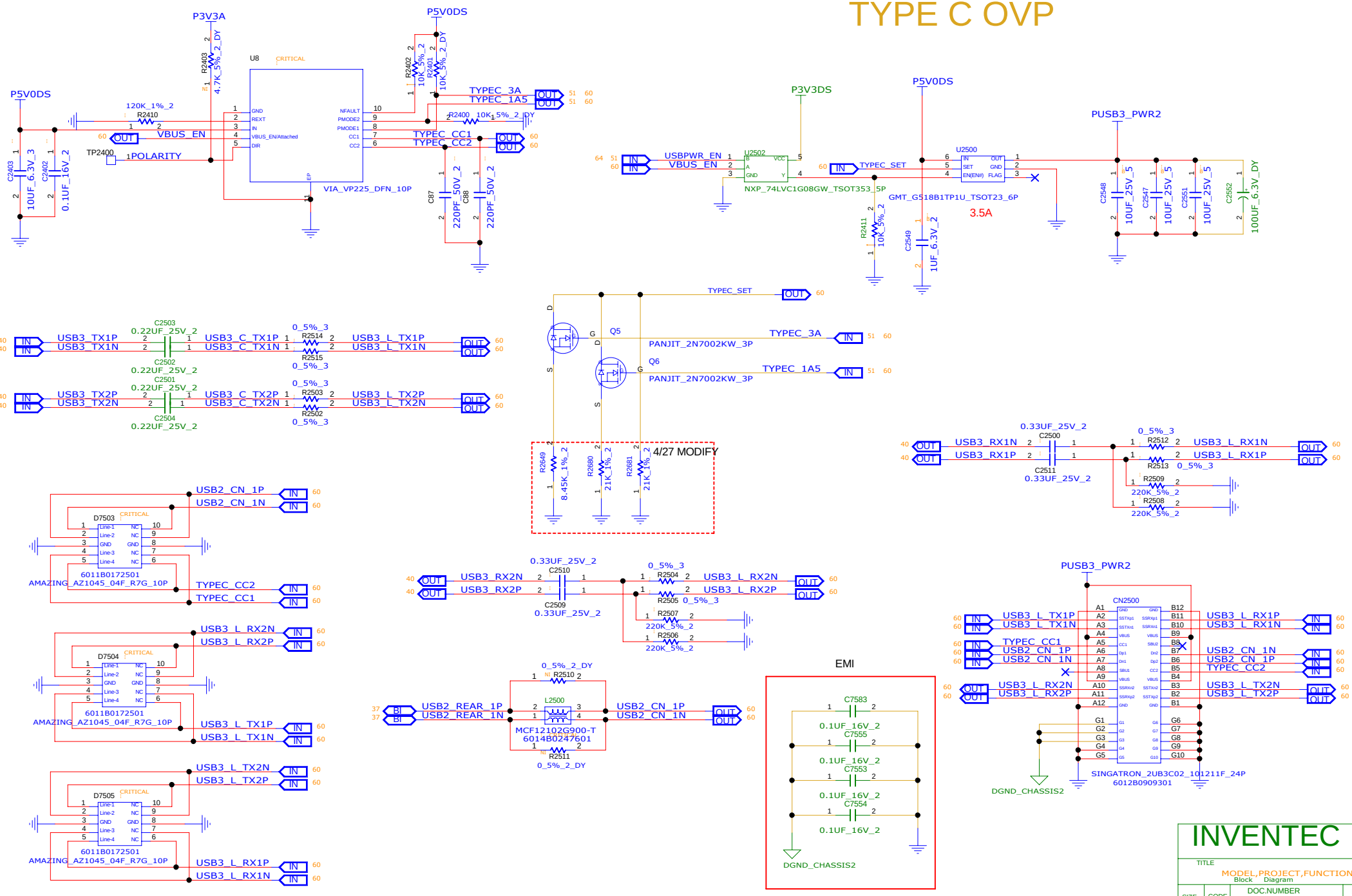
https://realschematic.com

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SATA HDD CONN.		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 59 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TYPE C OVP



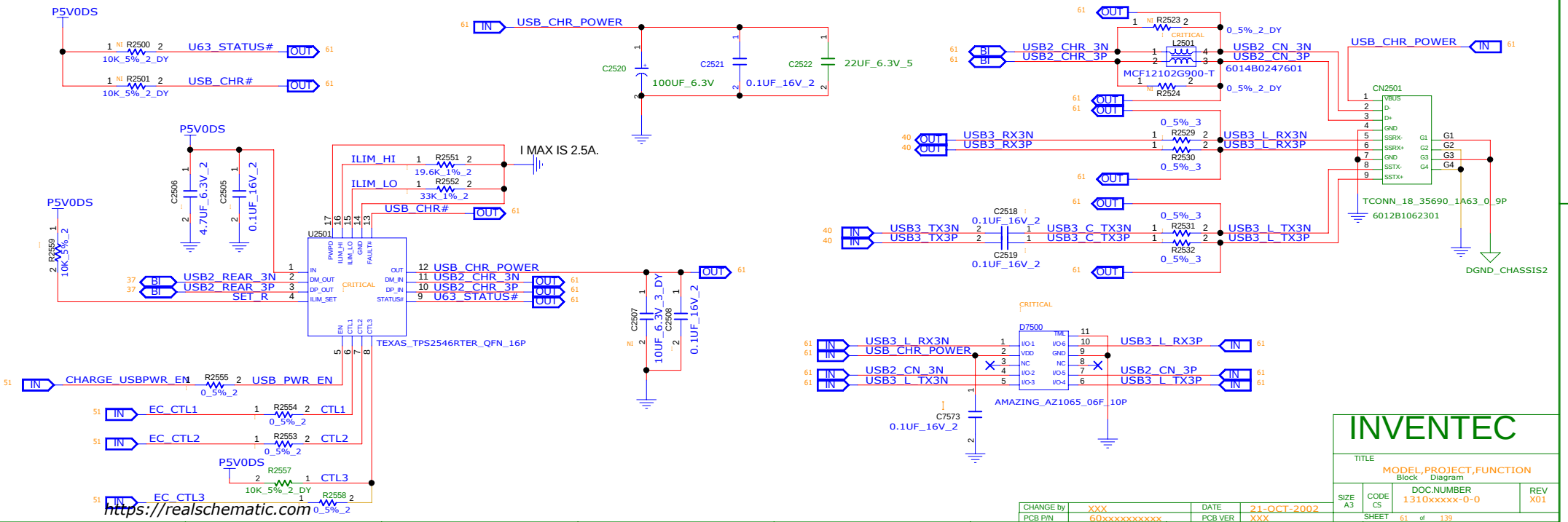
https://realschematic.com

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 60 of 139	
PCB P/N 60xxxxxxxxx	PCB VER XXX		

USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller: TI2546	Ctrl Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

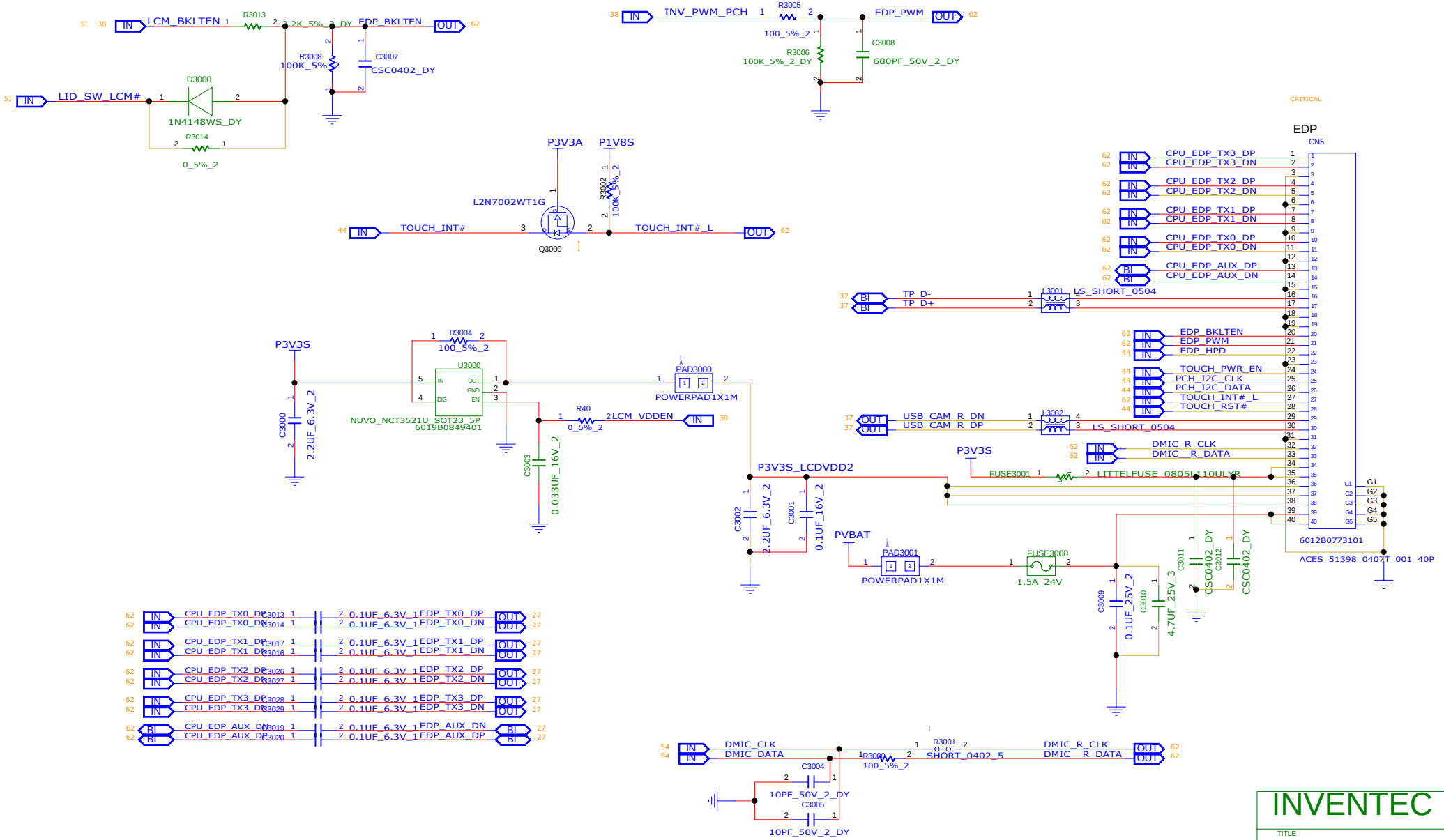
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 61 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

REFFERENCE 3000~3049(LCM)

EDP CONN



https://realschematic.com

INVENTEC

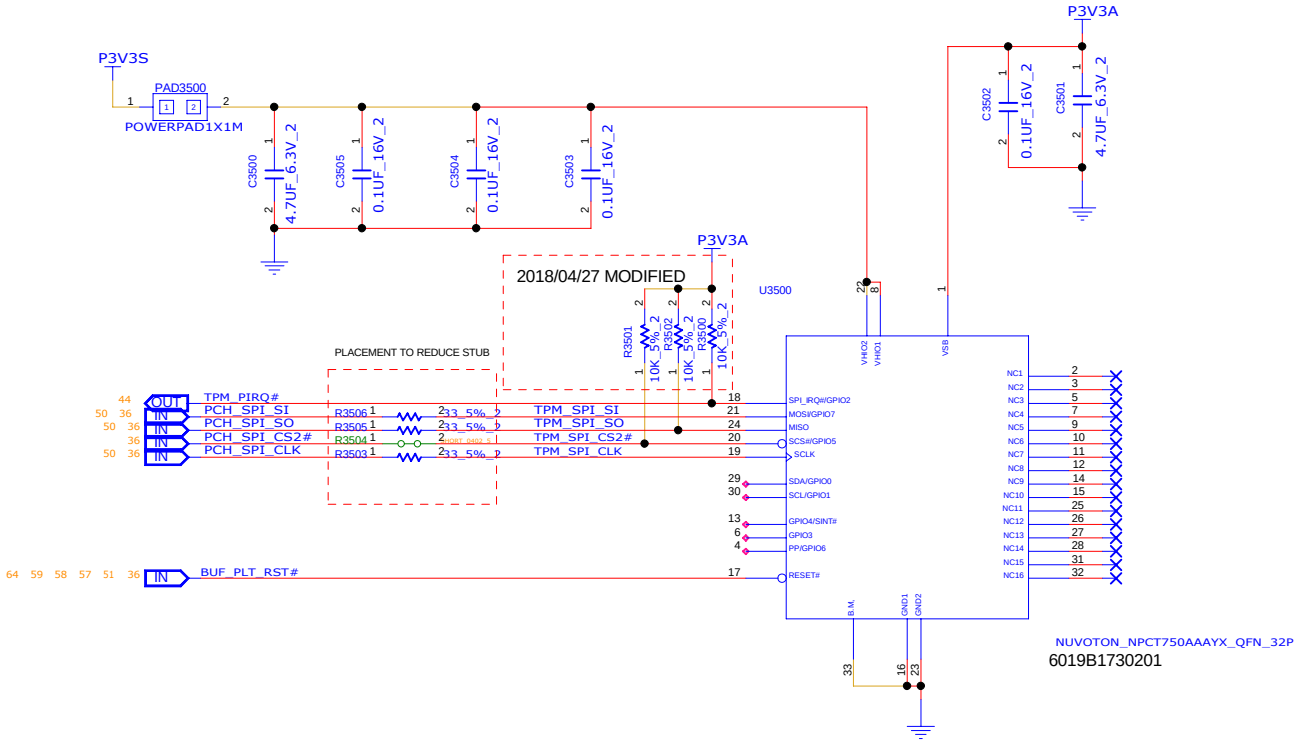
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 62 of 139

TPM DO NOT INSTALL



https://realschematic.com

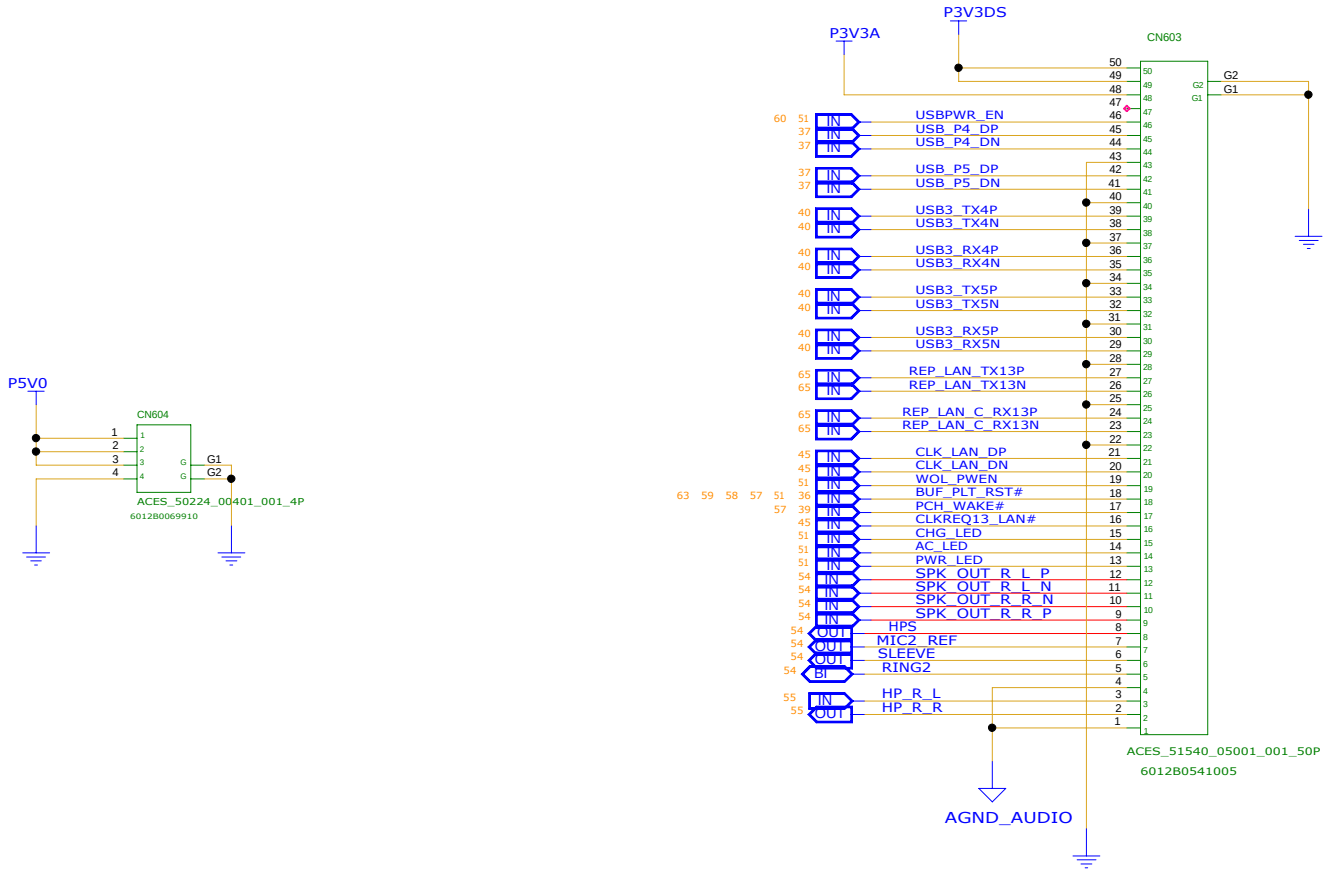
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 63 of 139



https://realschematic.com

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

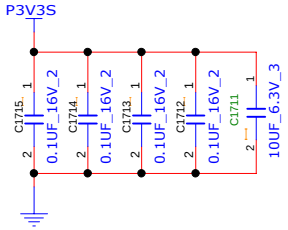
INVENTEC

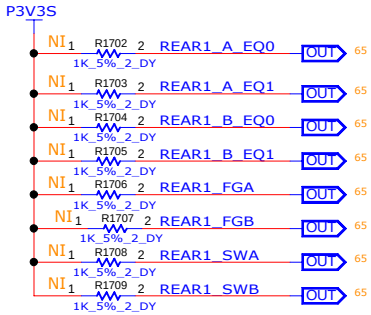
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

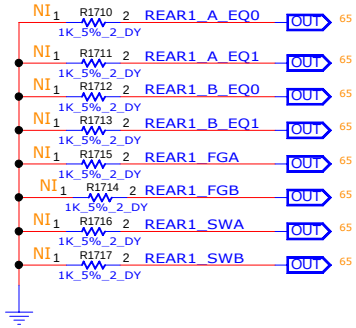
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

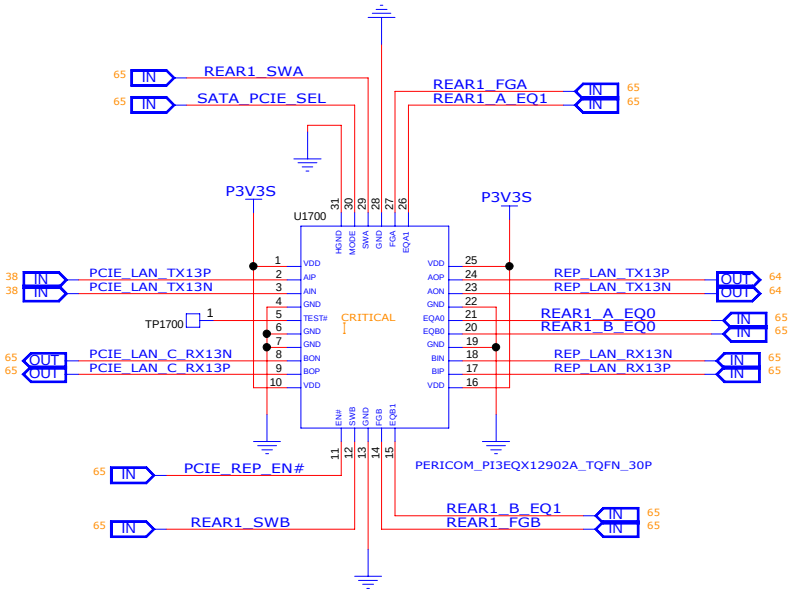
SHEET 64 of 139

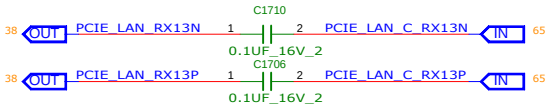
PCIE REPEATER

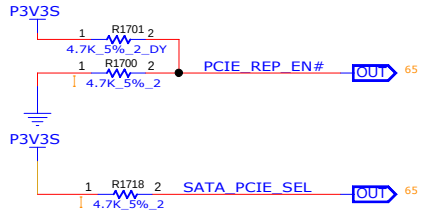


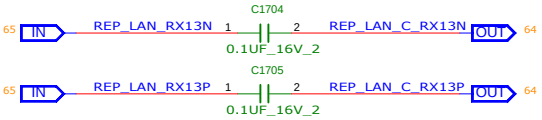










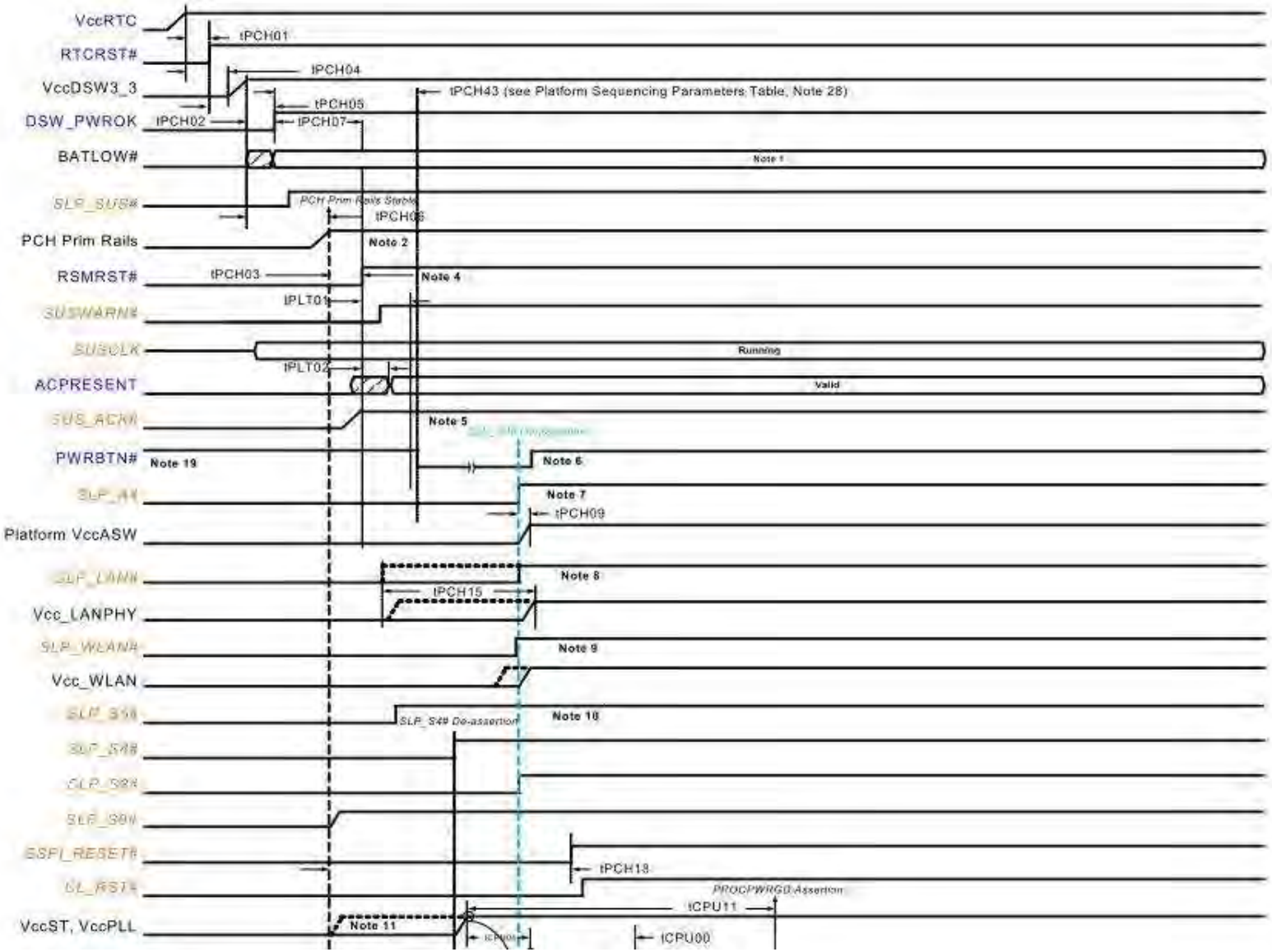


https://realschematic.com

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET 65 of 139	



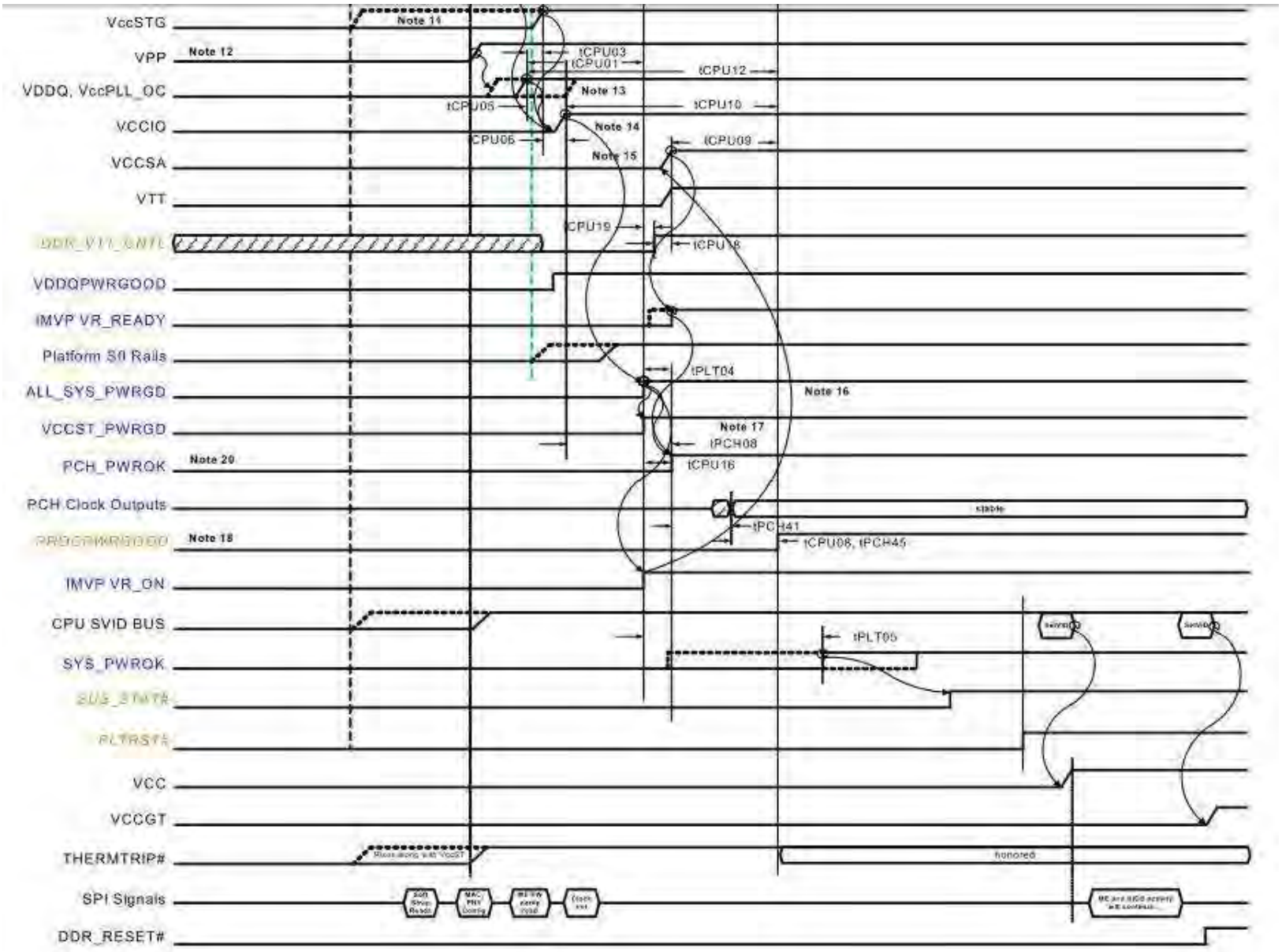
INVENTEC

TITLE: MODEL_PROJECT_FUNCTION Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 66 of 139



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 67 of 139

8 7 6 5 4 3 2 1

D C B A

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 68 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

07e30a1209261000d00169fd1b0036e2

8 7 6 5 4 3 2 1

D C B A

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 69 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8 7 6 5 4 3 2 1

D C B A

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 70 of 139

N18E-G0
N18E-G1
N18E-G2 MAX-Q

8GB DDR5 256M X 16 X 2 X6

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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PCA CODE NAME： N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001
G1 : 6019B1849201
G2 MAXQ:6019B1849301

PCB VERSION：X01
BOARD SIZE:

SCH P/N:
PCB P/N:
PCA P/N:

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MAINBOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU_NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (RT8816A_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (RT8068A)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (RT8068A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
88	GPU VBIOS, STRAPS	118	
89	GPU GPIOS	119	
90	GPU IFP_AB	120	
91	GPU DP IFP_CD	121	
92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
93	GPU DP CONNECTOR	123	
94	GPU HDMI IFP_EF	124	
95	GPU HDMI RETIMER IT66317	125	
96	GPU HDMI CONNECTOR	126	
97	GPU NVHS	127	
98	OVR-M	128	
99	GPU NVDD	129	
100	GPU FBVDD	130	

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL
NI: NON-INSTALL
DY: NON-INSTALL
MP: PRODUCTION
PROTO: PRE-PRODUCTION
CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847601

MICRON MT61K256M32JE-14:A
6019B1847701

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 72 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

CONNECTION TO MAINBOARD

CLK_PCIE_DGPU_100MHZ_P
CLK_PCIE_DGPU_100MHZ_N
PCIE_DGPU_RX15P
PCIE_DGPU_RX15N
PCIE_DGPU_TX15P
PCIE_DGPU_TX15N
PCIE_DGPU_RX14P
PCIE_DGPU_RX14N
PCIE_DGPU_TX14P
PCIE_DGPU_TX14N
PCIE_DGPU_RX13P
PCIE_DGPU_RX13N
PCIE_DGPU_TX13P
PCIE_DGPU_TX13N
PCIE_DGPU_RX12P
PCIE_DGPU_RX12N
PCIE_DGPU_TX12P
PCIE_DGPU_TX12N
PCIE_DGPU_RX11P
PCIE_DGPU_RX11N
PCIE_DGPU_TX11P
PCIE_DGPU_TX11N
PCIE_DGPU_RX10P
PCIE_DGPU_RX10N
PCIE_DGPU_TX10P
PCIE_DGPU_TX10N
PCIE_DGPU_RX9P
PCIE_DGPU_RX9N
PCIE_DGPU_TX9P
PCIE_DGPU_TX9N
PCIE_DGPU_RX8P
PCIE_DGPU_RX8N
PCIE_DGPU_TX8P
PCIE_DGPU_TX8N
PCIE_DGPU_RX7P
PCIE_DGPU_RX7N
PCIE_DGPU_TX7P
PCIE_DGPU_TX7N
PCIE_DGPU_RX6P
PCIE_DGPU_RX6N
PCIE_DGPU_TX6P
PCIE_DGPU_TX6N
PCIE_DGPU_RX5P
PCIE_DGPU_RX5N
PCIE_DGPU_TX5P
PCIE_DGPU_TX5N
PCIE_DGPU_RX4P
PCIE_DGPU_RX4N
PCIE_DGPU_TX4P
PCIE_DGPU_TX4N
PCIE_DGPU_RX3P
PCIE_DGPU_RX3N
PCIE_DGPU_TX3P
PCIE_DGPU_TX3N
PCIE_DGPU_RX2P
PCIE_DGPU_RX2N
PCIE_DGPU_TX2P
PCIE_DGPU_TX2N
PCIE_DGPU_RX1P
PCIE_DGPU_RX1N
PCIE_DGPU_TX1P
PCIE_DGPU_TX1N
PCIE_DGPU_RX0P
PCIE_DGPU_RX0N
PCIE_DGPU_TX0P
PCIE_DGPU_TX0N

DGPU_PWR_EN

GPU PWR ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

PCH_PLTRST#_BUF

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

IRMT_HOLD_RST#

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND

TO PCH

GPU_EVENT_PCH#

PCH INFORM GPU WILL EXIT GC6 MODS

DGPU_PWRLEVEL

15.3.2 PWR_LEVEL* (GPIO12)

The POWER_LEVEL input signal triggers an immediate GPU hardware slow-down, followed by the driver capping the GPU power state to the appropriate limit. There are two events that can trigger this signal assertion: AC to battery power transition or total system power overdraw event.

PEX_CLKREQ#

PCIE CLK REQUESTD#

ALL_POWER_GOOD

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

DP_MA_HPD#

DP HPD TO MAINBOARD
MAKE SURE 10K P3V3S PULL UP

SMB0_DATA_D
SMB0_CLK_D

DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP

HDMI_MB_HPD#

HDMI HPD TO MB

SMB0_DATA_D
SMB0_CLK_D

HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

GPU_OVERT_EC#

3.3V LEVEL
OVER TEMPERATURE TO PCH OR EC

GC6_FB_EN_PCH

3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC

EC_SMBDATA0
EC_SMBCLK0

GPU I2C, COMMUNCATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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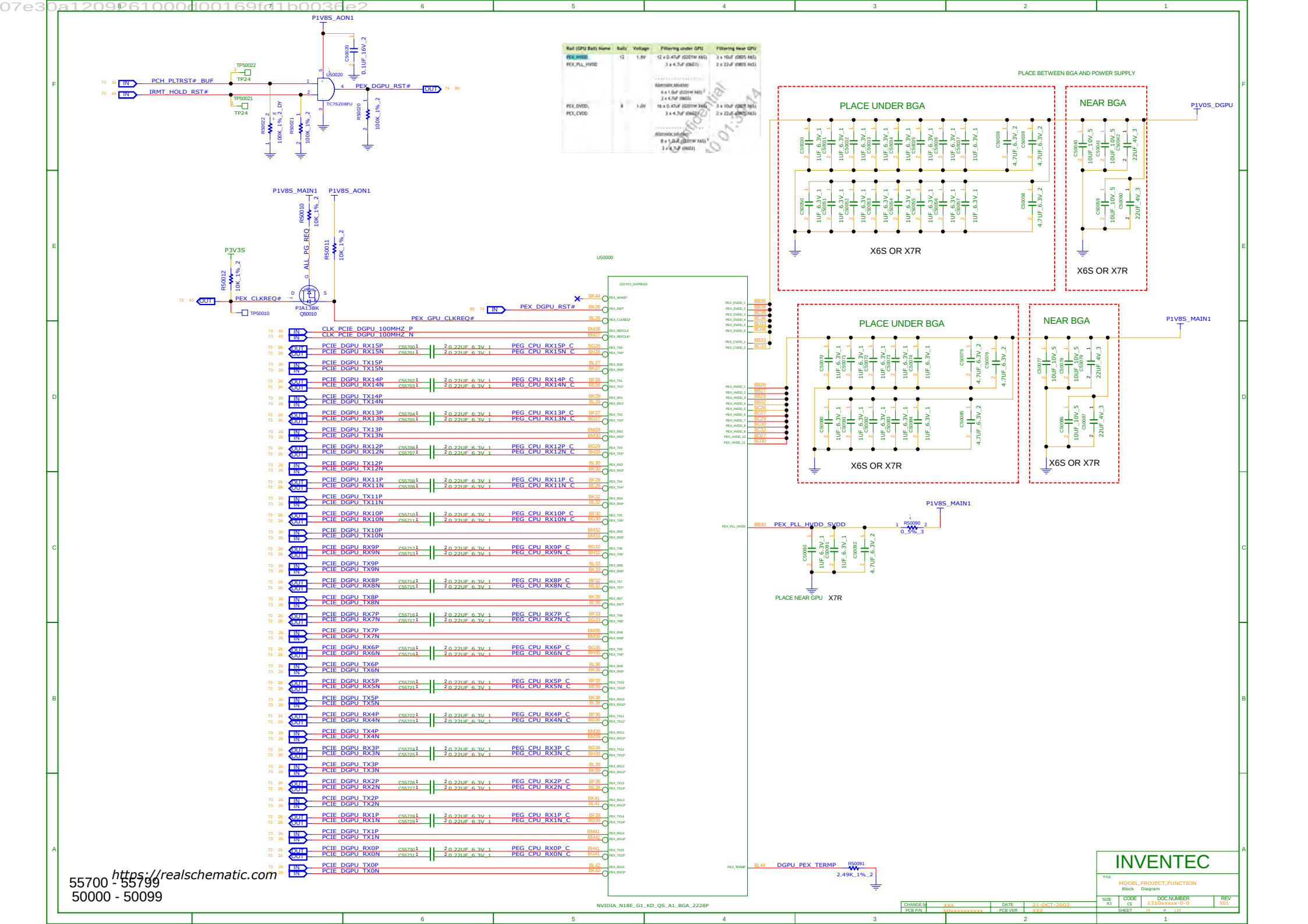
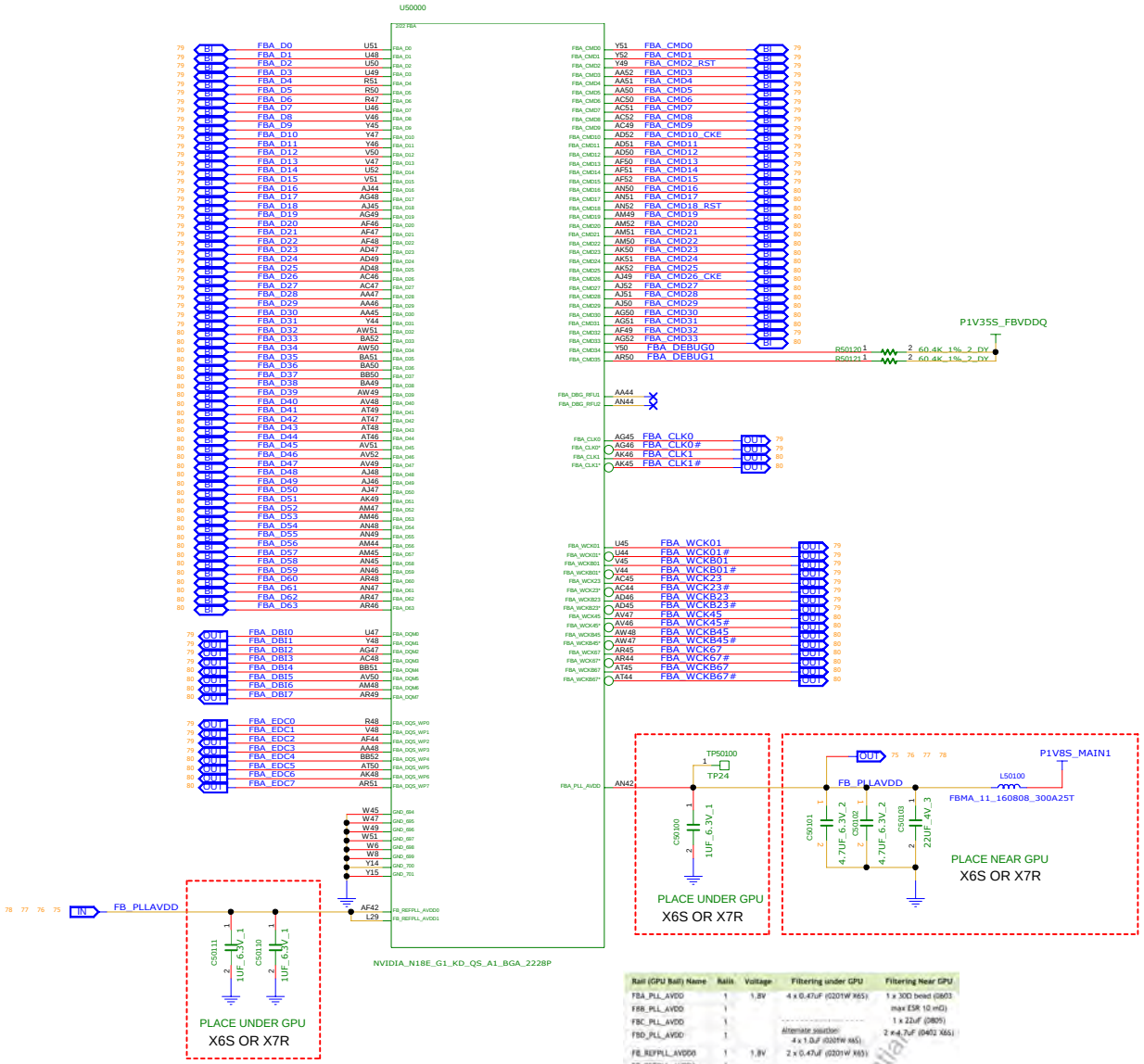


https://realschematic.com

55700 - 55799
50000 - 50099

GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603
FBB_PLL_AVDD	1			max ESR 10 mΩ)
FBC_PLL_AVDD	1		----------	1 x 22uF (0805)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	2 x 4.7uF (0402 X6S)
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		---------- Alternate solution: 2 x 1.0uF (0201W X6S)	



50100 - 50199

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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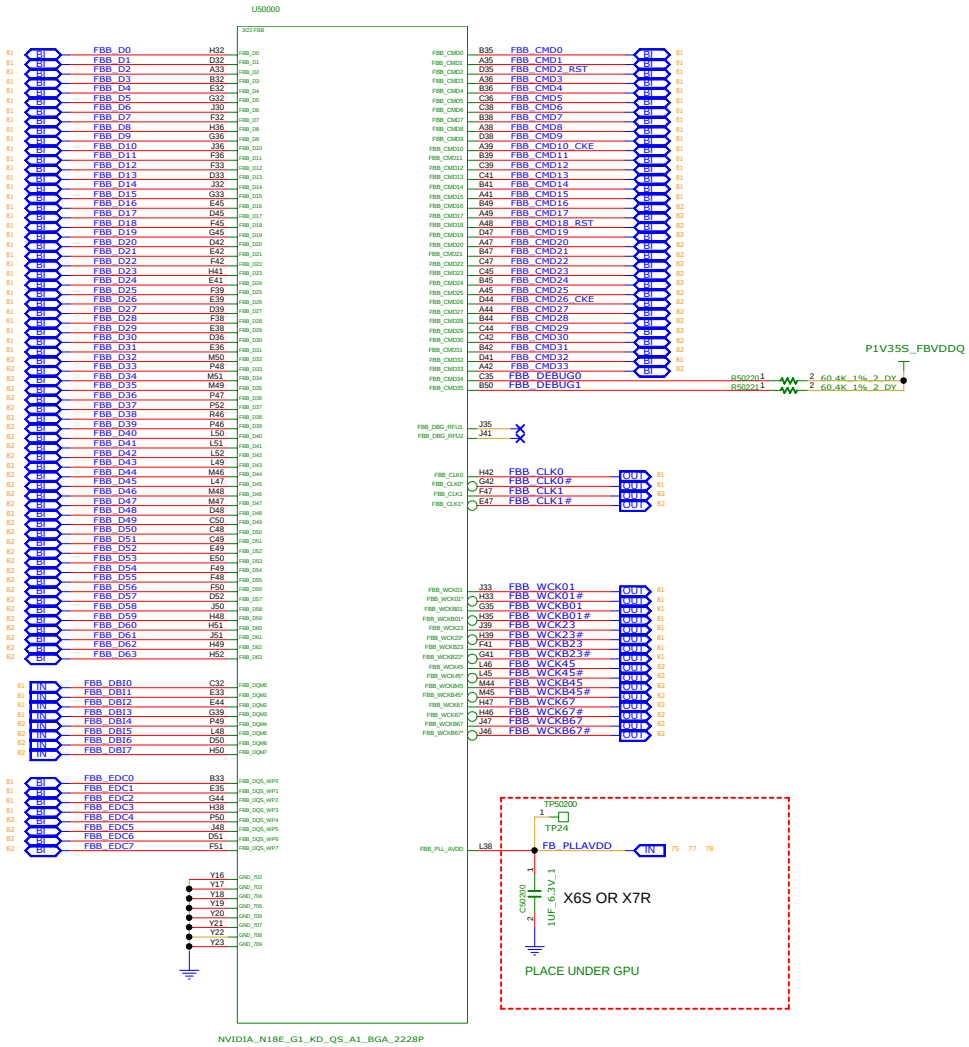
GPU FRAME BUFFER B



https://realschematic.com

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INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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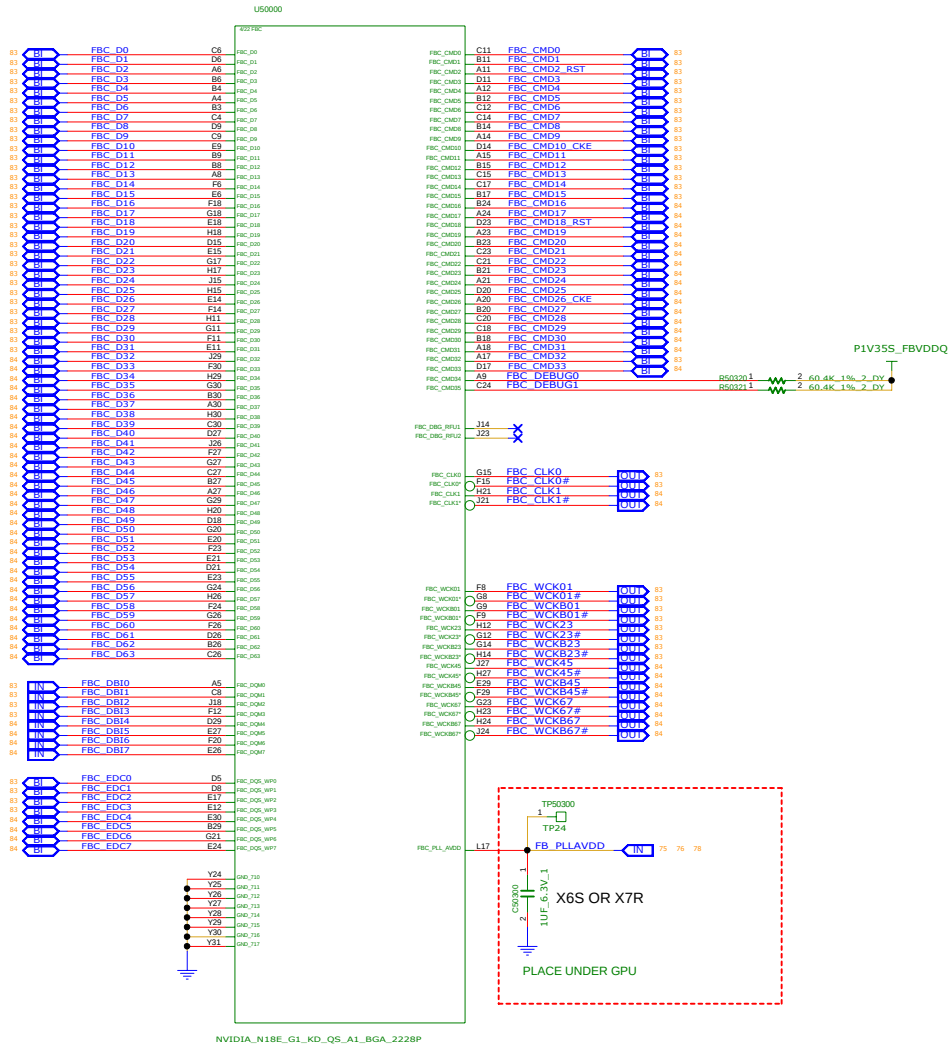
CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

GPU FRAME BUFFER C



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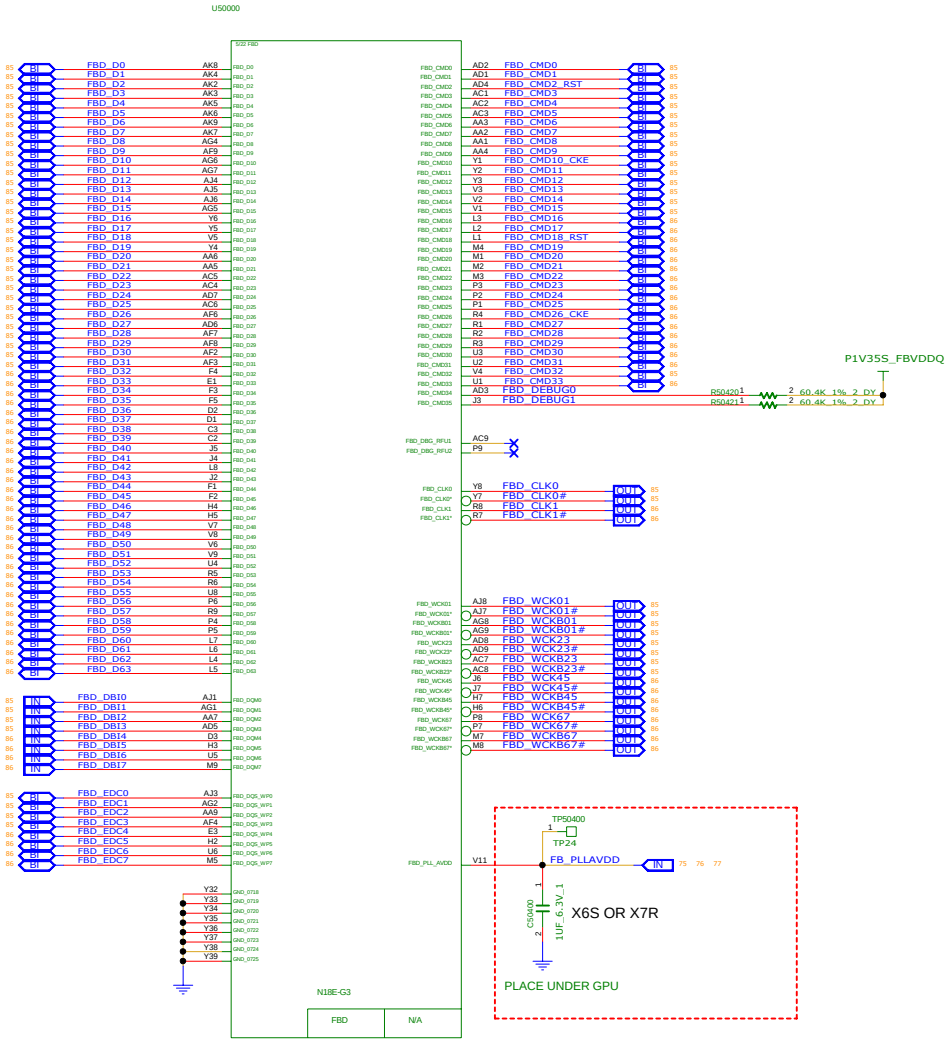
50300 - 50399

INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

GPU FRAME BUFFER D



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INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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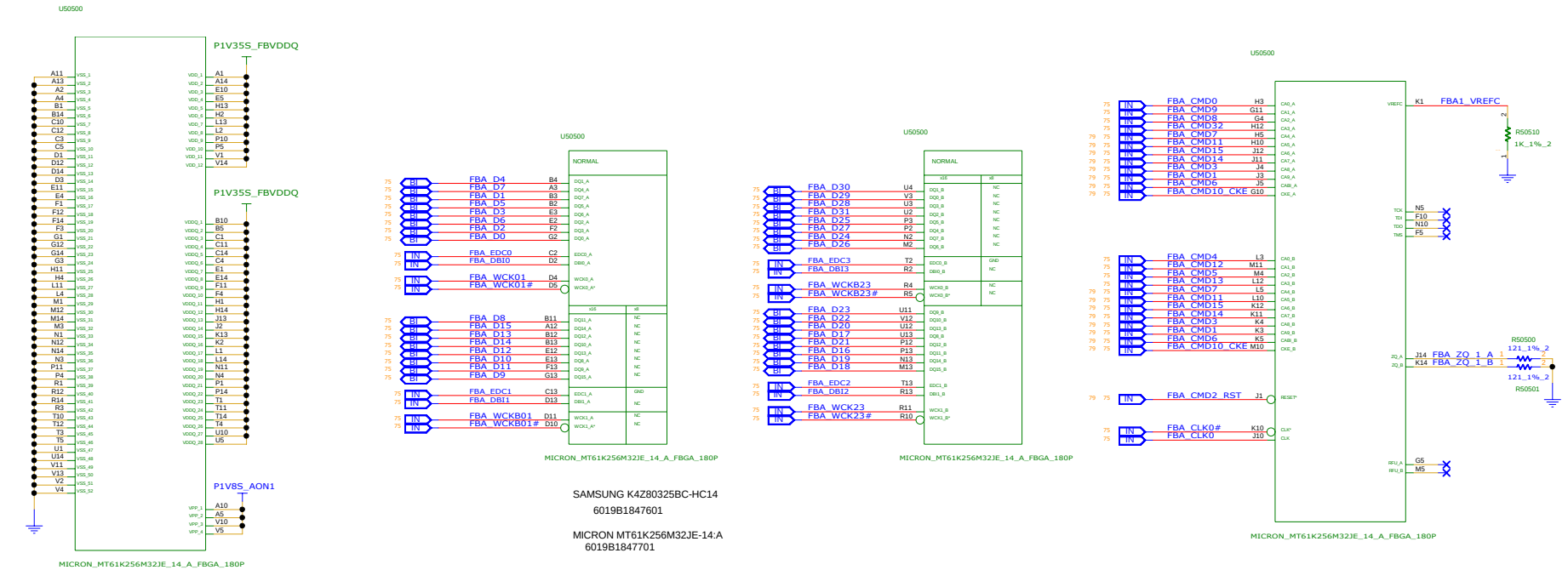
CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



SAMSUNG K4Z80325BC-HC14
6019B1847601

MICRON MT61K256M32JE-14:A
6019B1847701

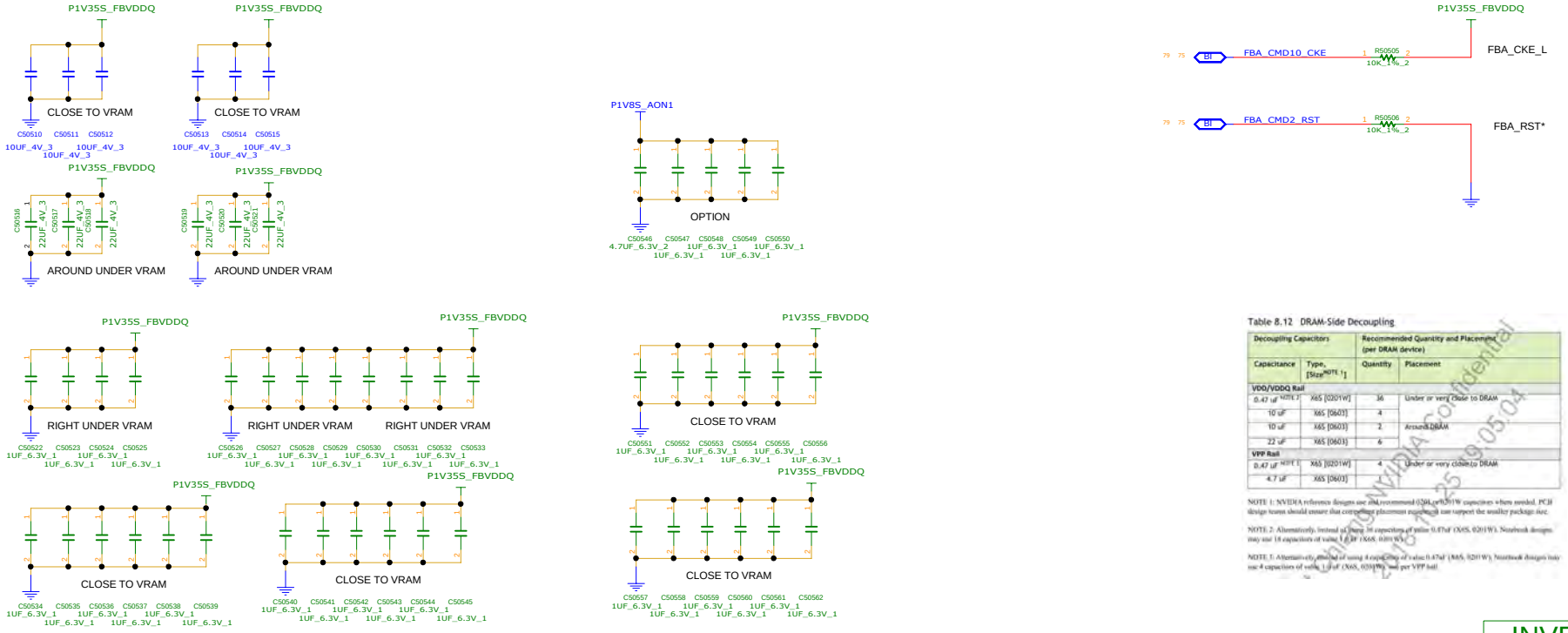


Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

NOTE 1: NVIDIA reference designs use and recommend 0201 or 0201W capacitors when needed. PCB design teams should ensure that component placement restrictions can support the smaller package size.

NOTE 2: Alternatively, instead of using 36 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 18 capacitors of value 1.0 uF (X6S, 0201W).

NOTE 3: Alternatively, instead of using 4 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 2 capacitors of value 1.0 uF (X6S, 0201W) per VPP ball.

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A3	CS	1310xxxxx-D-D	X01

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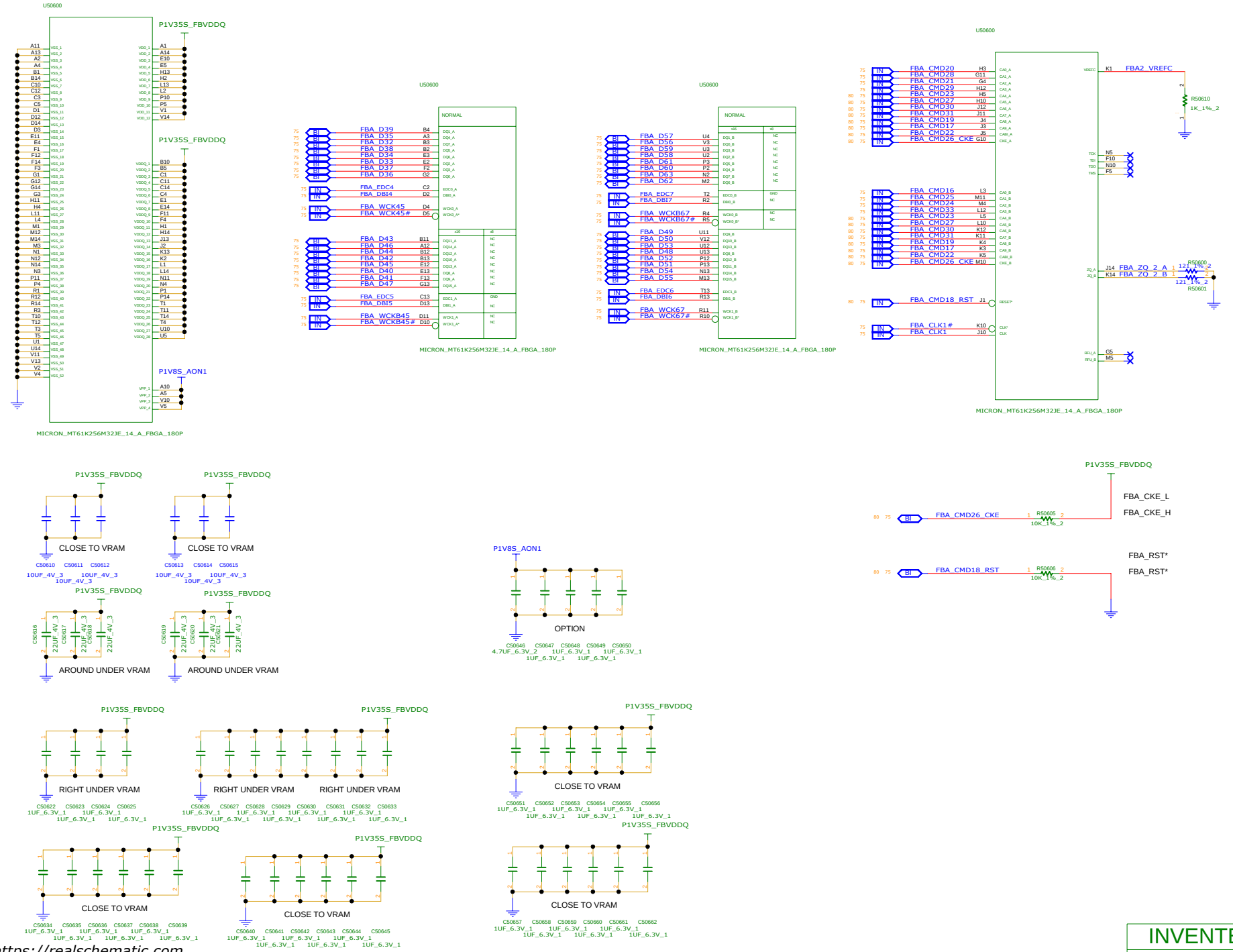
U50600
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
FBA_D39
FBA_D35
FBA_D32
FBA_D38
FBA_D34
FBA_D33
FBA_D37
FBA_D36
FBA_EDC4
FBA_DBI4
FBA_WCK45
FBA_WCK45#
FBA_D43
FBA_D46
FBA_D44
FBA_D42
FBA_D45
FBA_D40
FBA_D41
FBA_D47
FBA_EDC5
FBA_DBI5
FBA_WCKB45
FBA_WCKB45#
FBA_D57
FBA_D56
FBA_D59
FBA_D58
FBA_D61
FBA_D60
FBA_D63
FBA_D62
FBA_EDC7
FBA_DBI7
FBA_WCKB67
FBA_WCKB67#
FBA_D49
FBA_D50
FBA_D53
FBA_D48
FBA_D52
FBA_D51
FBA_D54
FBA_D55
FBA_EDC6
FBA_DBI6
FBA_WCK67
FBA_WCK67#
FBA_CMD20
FBA_CMD28
FBA_CMD21
FBA_CMD29
FBA_CMD23
FBA_CMD27
FBA_CMD30
FBA_CMD31
FBA_CMD19
FBA_CMD17
FBA_CMD22
FBA_CMD26_CKE
FBA_CMD16
FBA_CMD25
FBA_CMD24
FBA_CMD33
FBA_CMD23
FBA_CMD27
FBA_CMD30
FBA_CMD31
FBA_CMD19
FBA_CMD17
FBA_CMD22
FBA_CMD26_CKE
FBA_CMD18_RST
FBA_CLK1#
FBA_CLK1
FBA2_VREFC
R50610
1K_1%_2
FBA_ZQ_2_A
FBA_ZQ_2_B
R50600
R50601
121_1%_2
CLOSE TO VRAM
AROUND UNDER VRAM
OPTION
RIGHT UNDER VRAM
FBA_CKE_L
FBA_CKE_H
FBA_RST*
R50605
R50606
10K_1%_2
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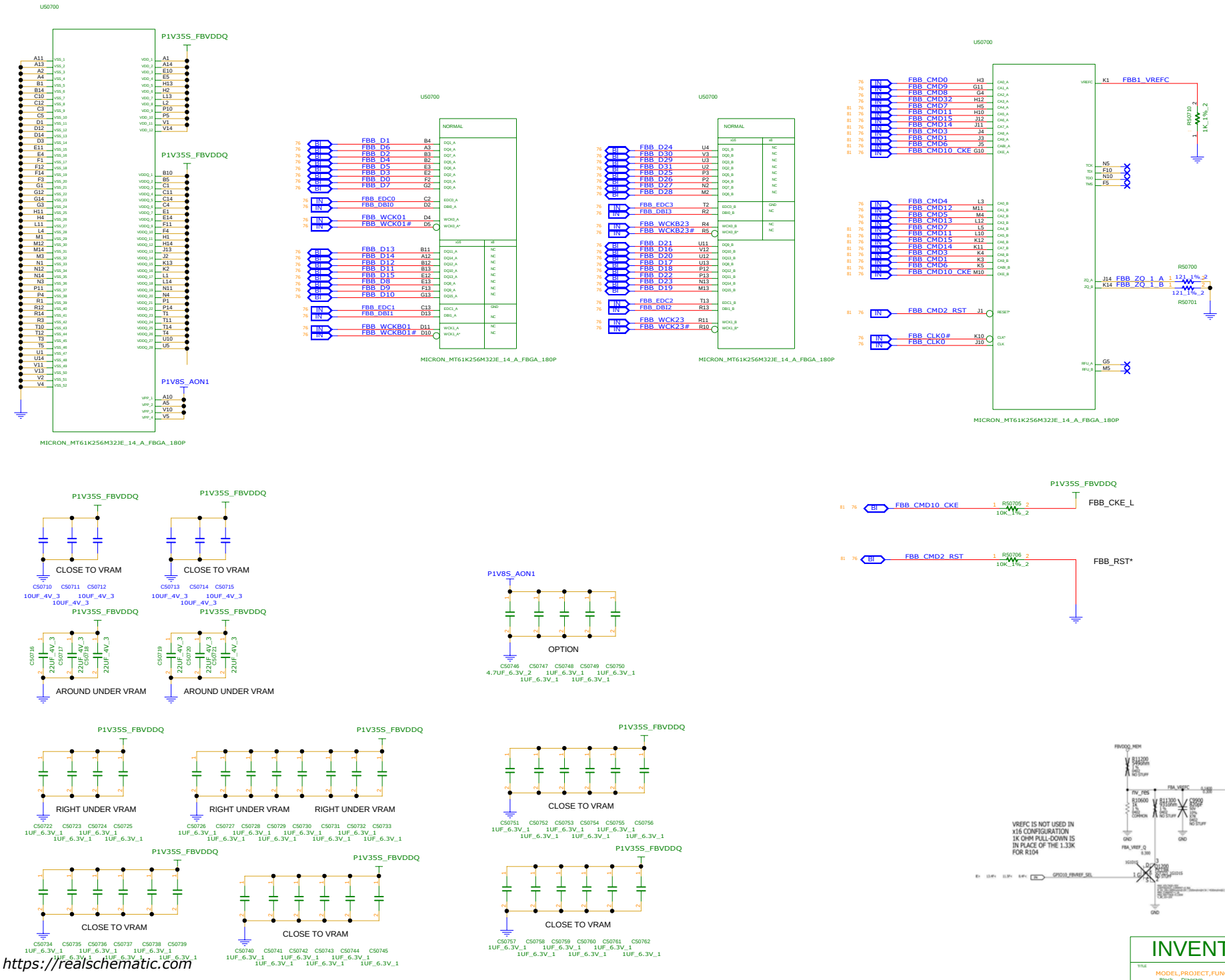

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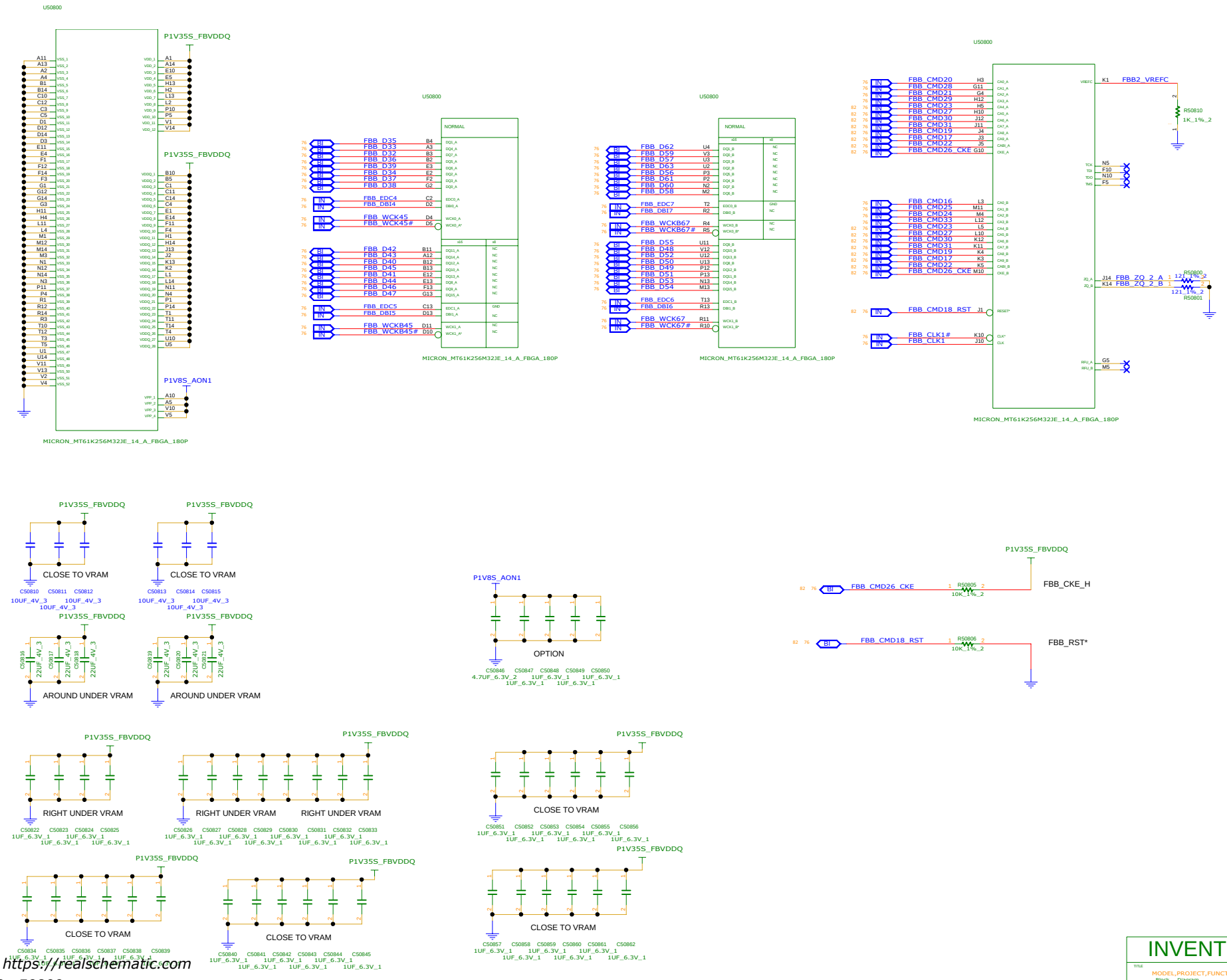

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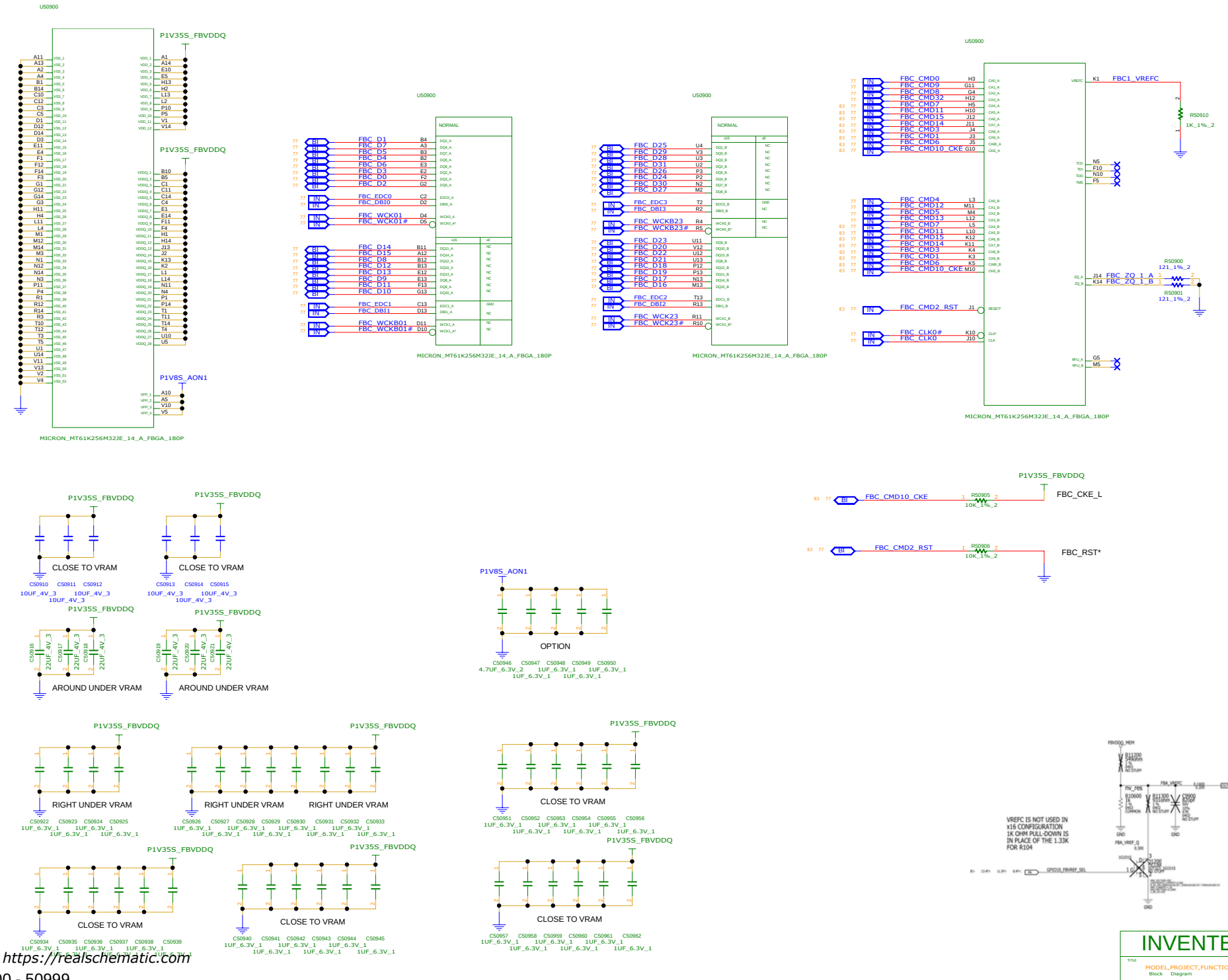
50800 - 50899



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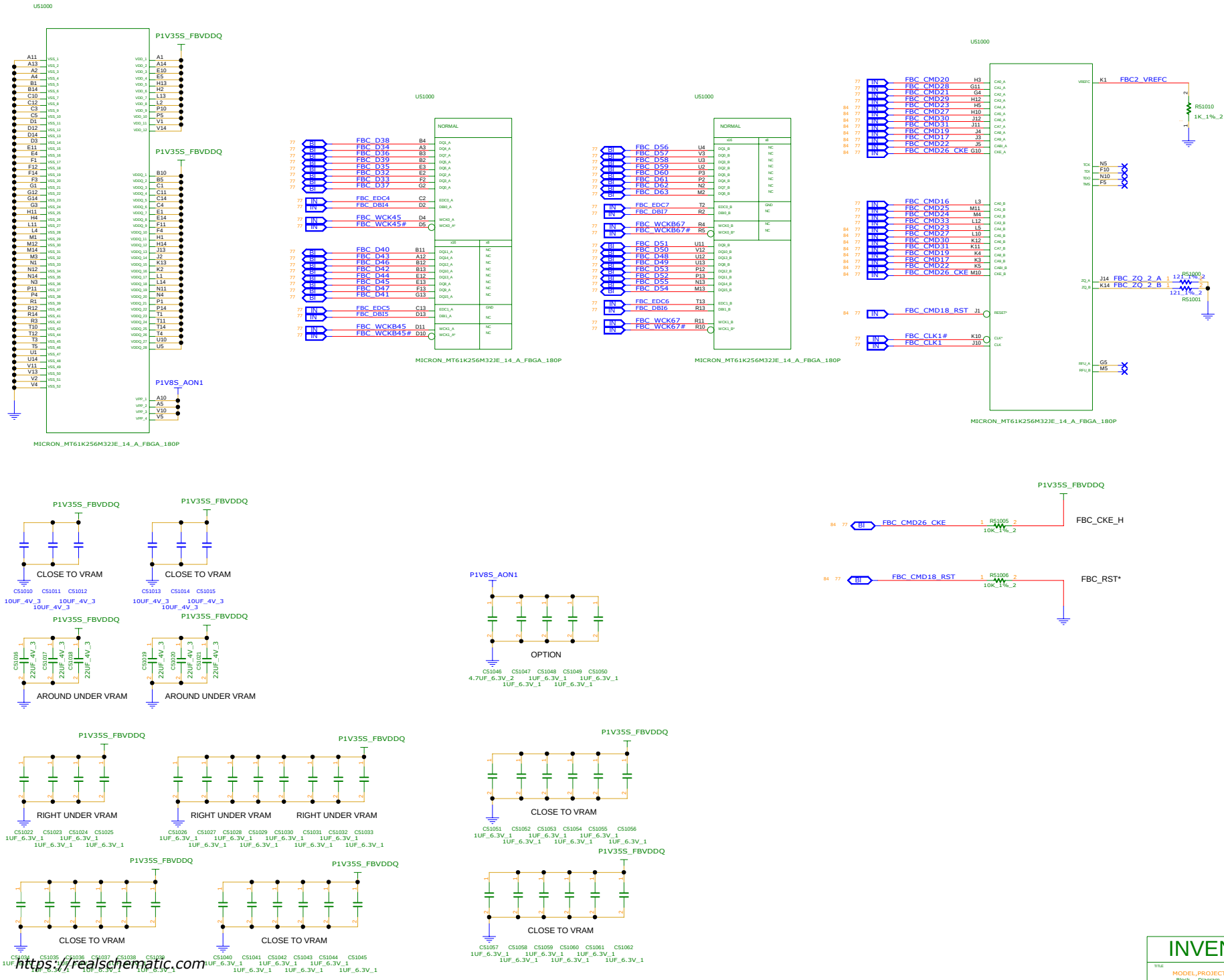

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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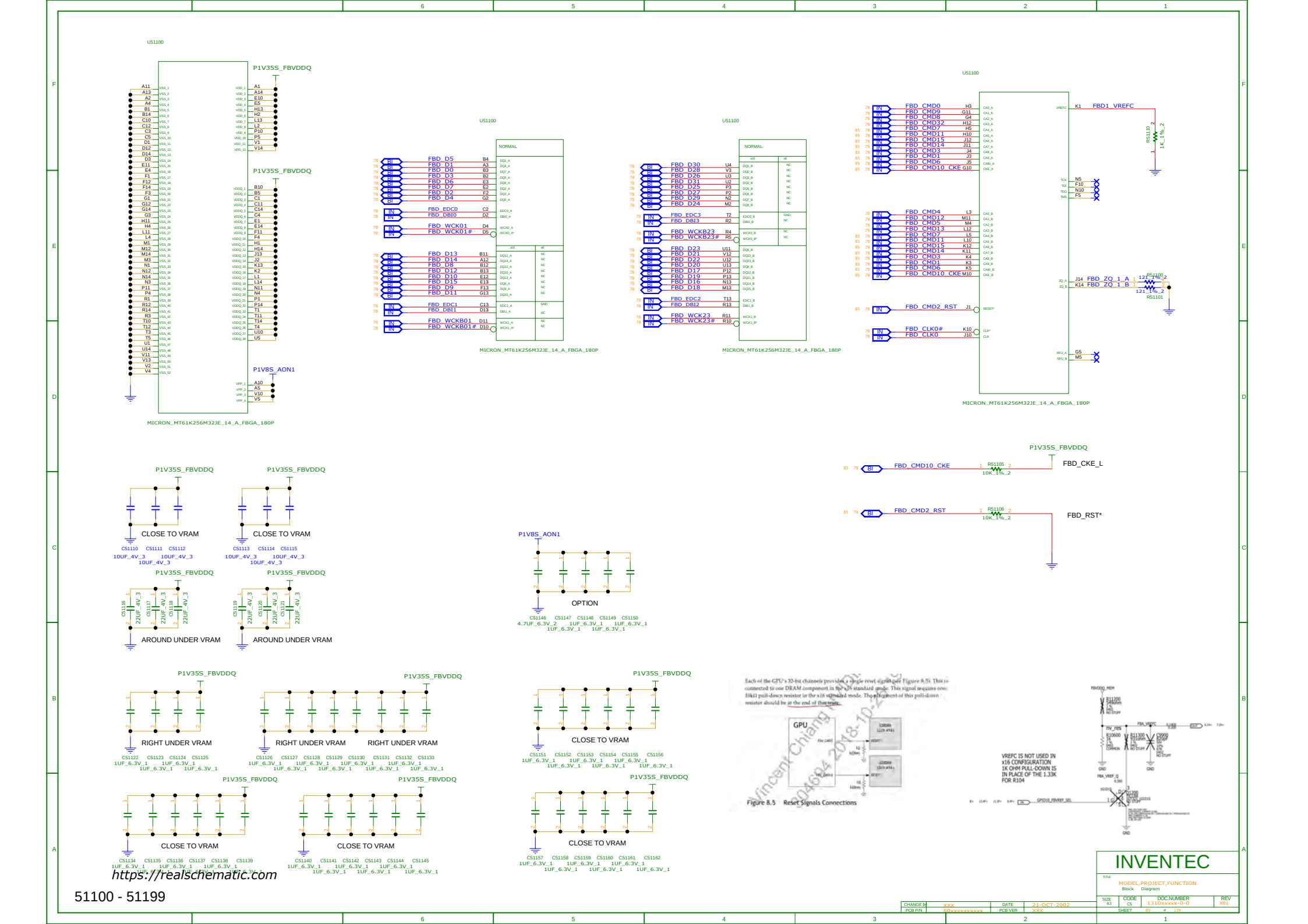

https://realschematic.com

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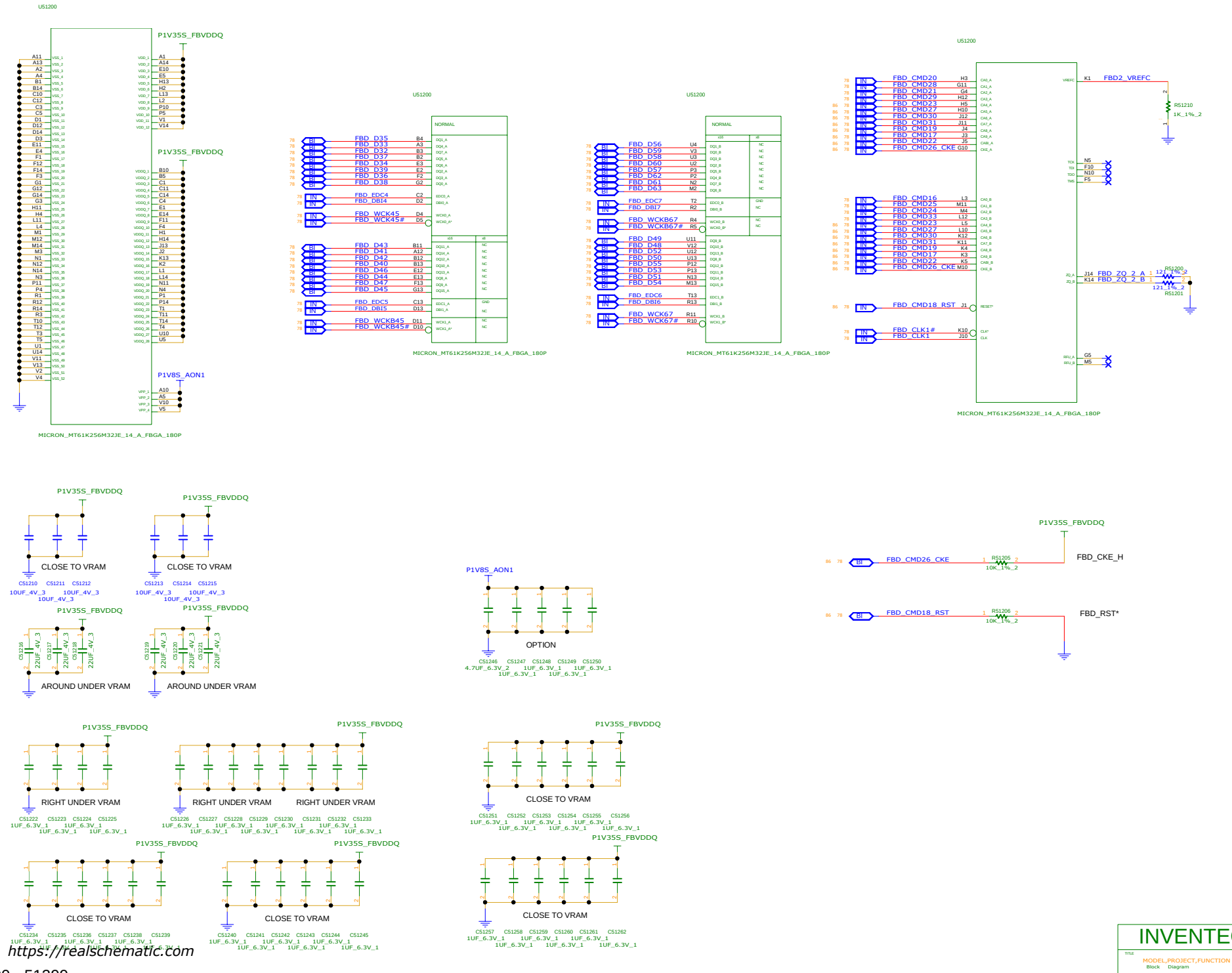

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INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60Gxxxxxxxxx	PCB VER	XXX

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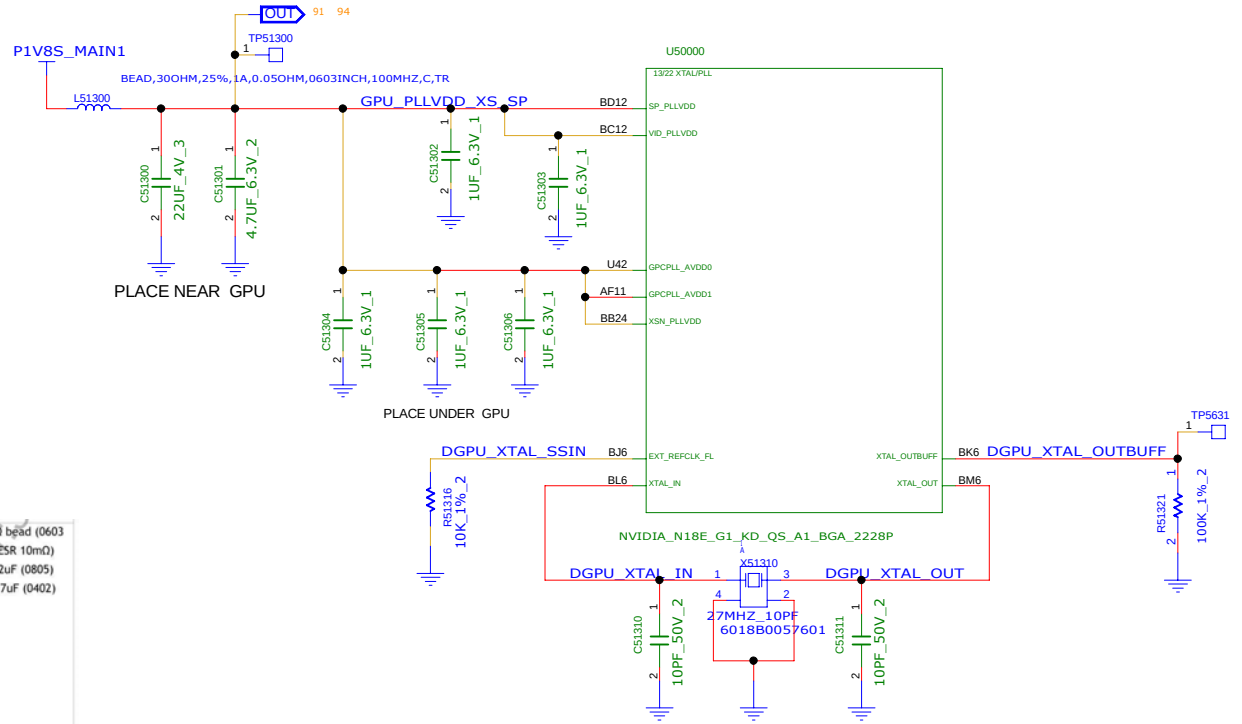
27 MHZ XTAL



CL=2*10-(5+3)=12

$C_{L\_trim} = 2 * (C_{load} - (C_{stray} + C_i))$

Where:

- C_{load} is the crystal load capacitance (from data sheet of XTAL used)
- C_{stray} (i.e. 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- C_i is pin capacitance (5 pF)

Typical CL_trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF.

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10mΩ)
IFPCD_PLLVDD	1			
IFPEF_PLLVDD	1		Alternate solution: 3 x 1.0uF (0201W X6S)	1 x 22uF (0805) 1 x 4.7uF (0402)
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X6S) Alternate solution: 3 x 1.0uF (0201W X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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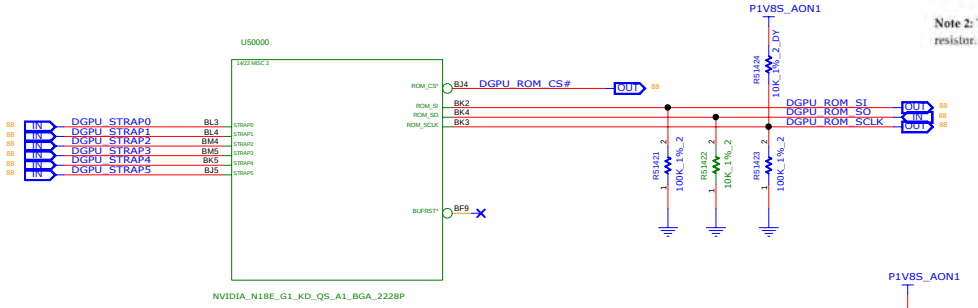
GPU VBIOS, EXTERNAL STRAPS

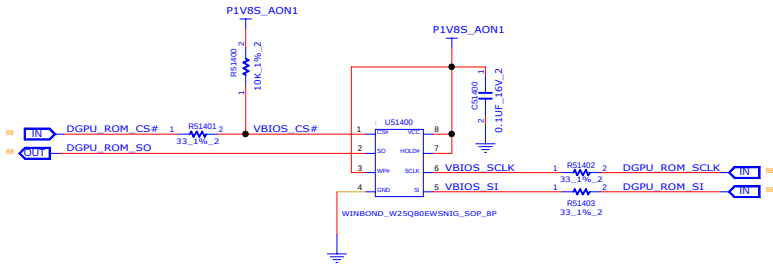
Table 12.4 FS_OVERT* Strap Enablement

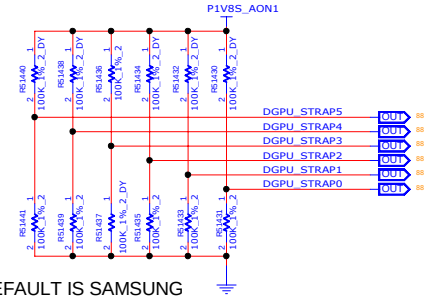
Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.







DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14
6019B1847601
STRAP 0X0=000
SAMSUNG:R51431 STUFF
R51430 NOT STUFF

MICRON MT61K256M32JE-14:A
6019B1847701
STRAP 0X1=001
MICRON :R51430 STUFF
R51431 NOT STUFF

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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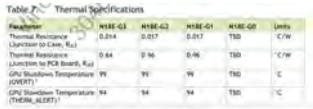
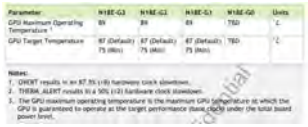
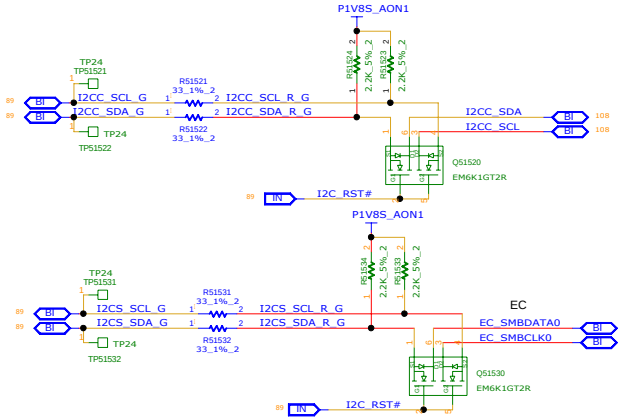
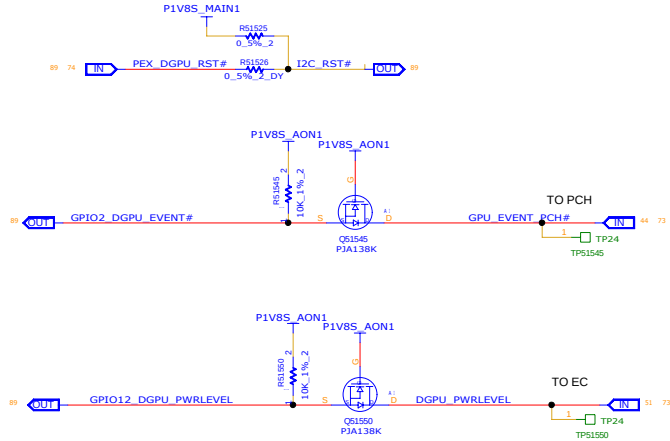
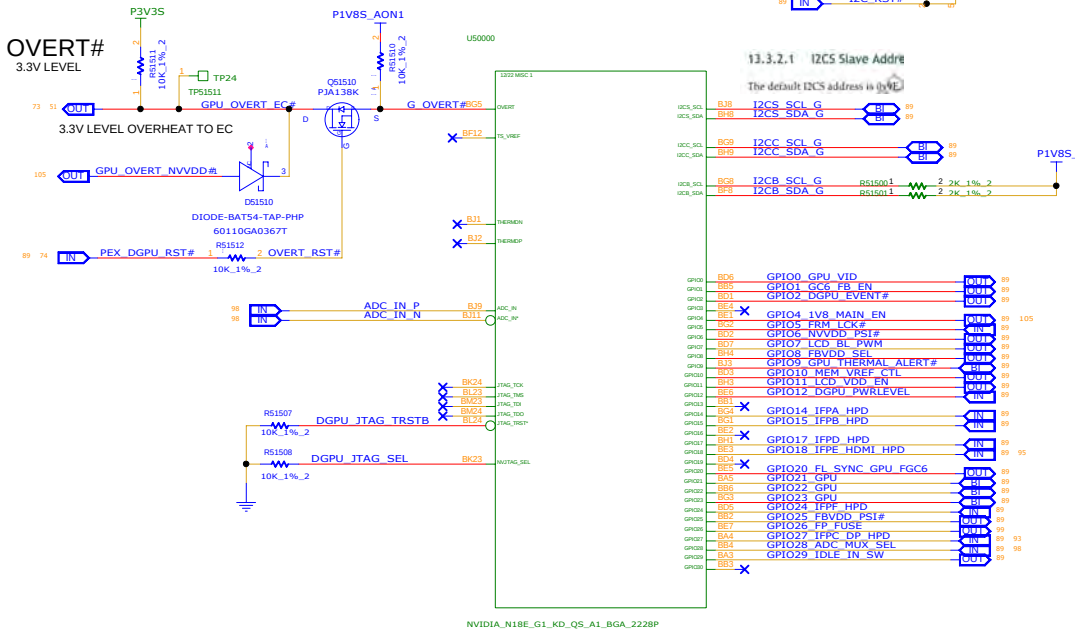
GPU GPIO

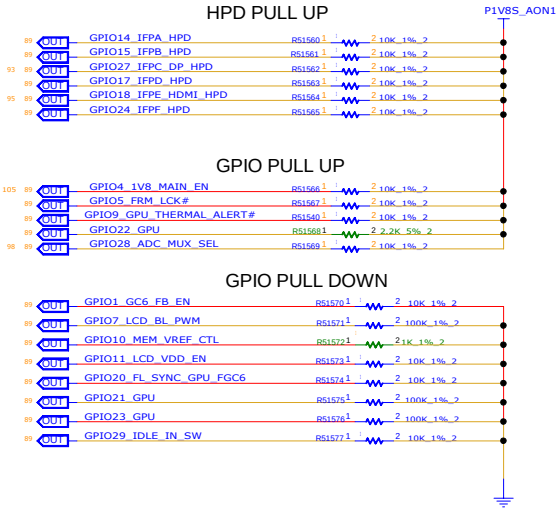


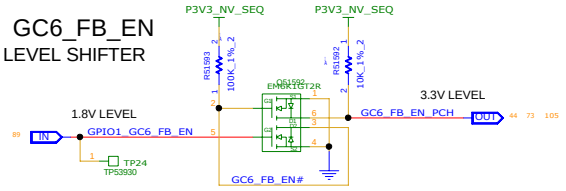


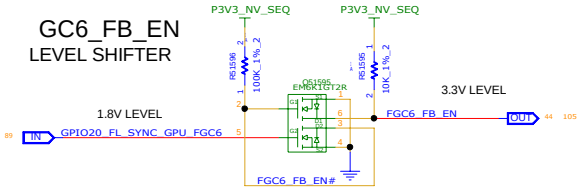


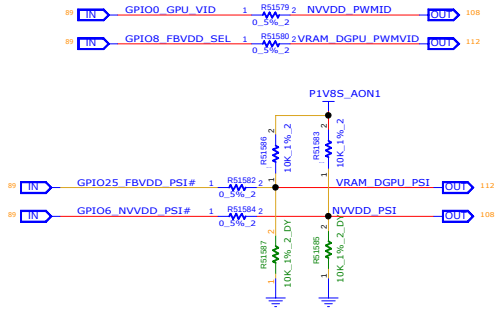












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INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-D	X01

CHANGE NO	XXX	DATE	21-OCT-2002
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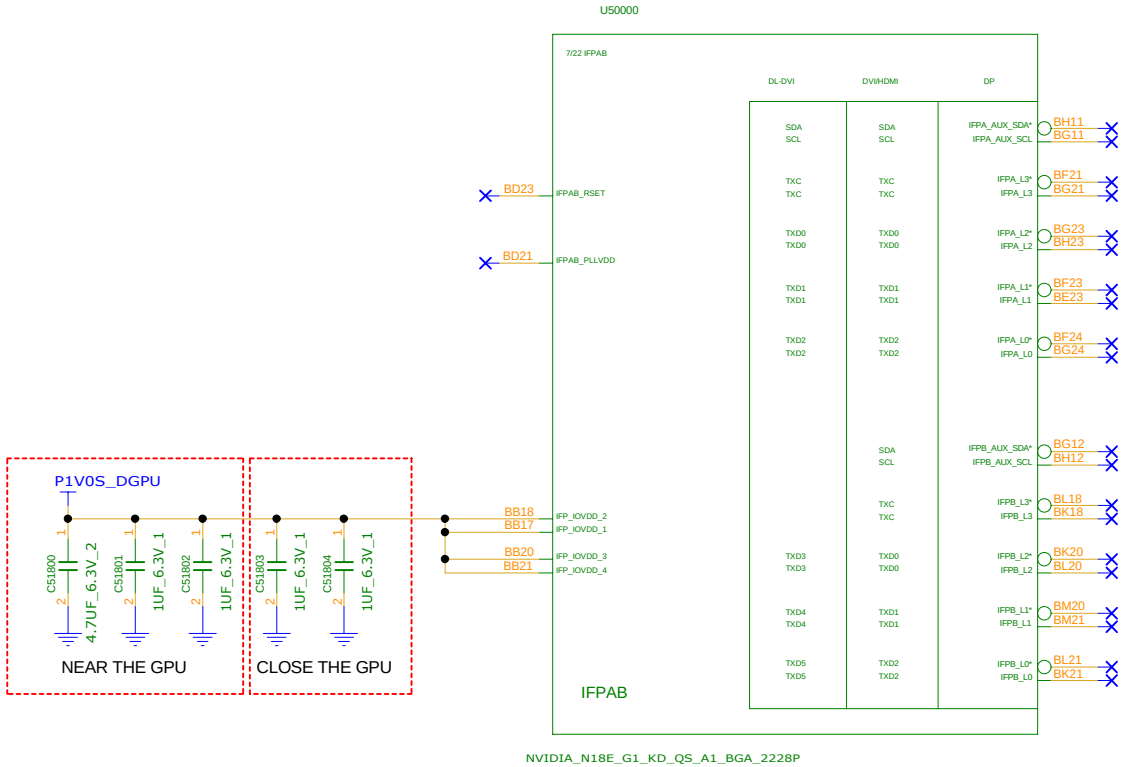

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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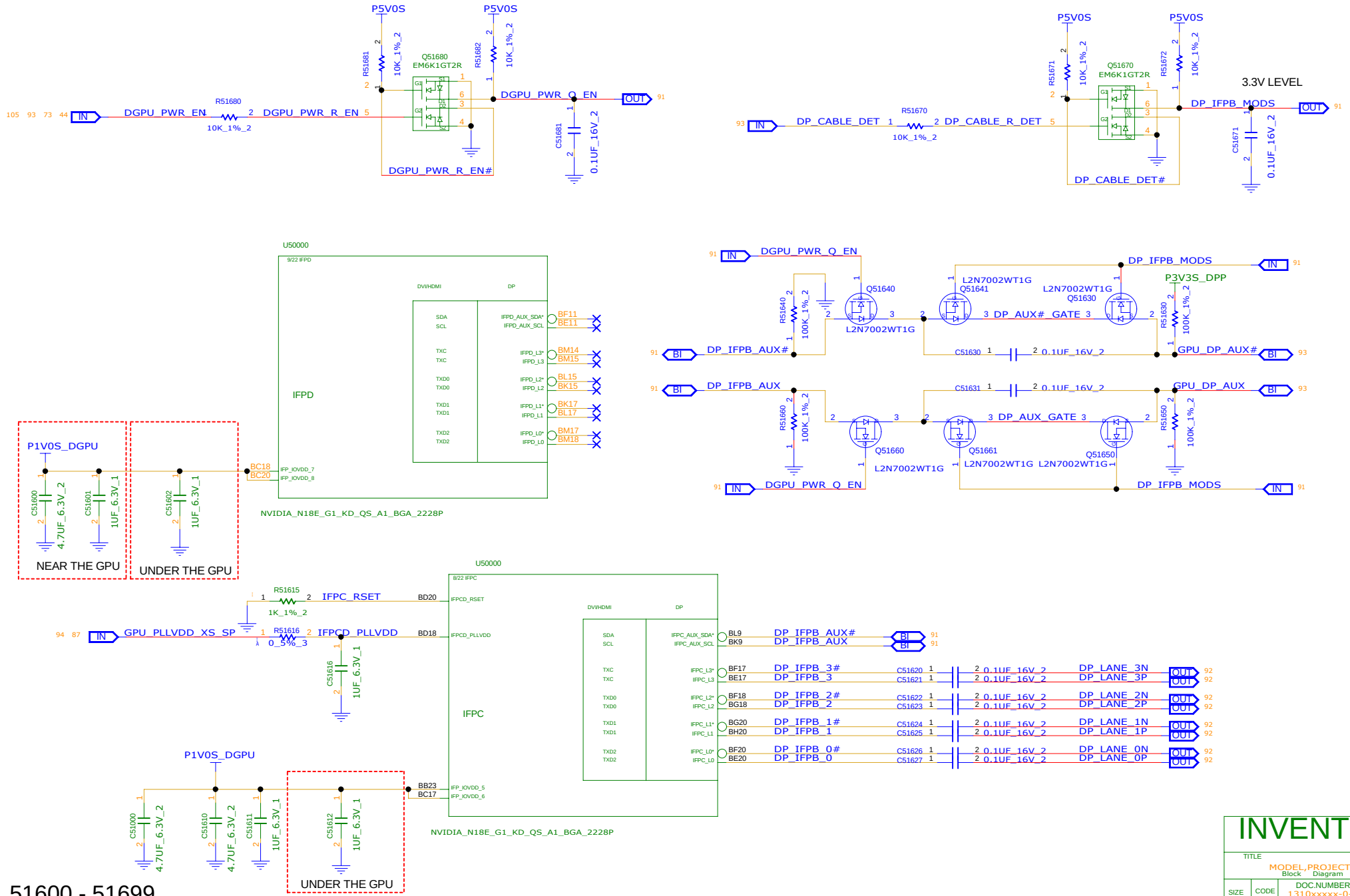
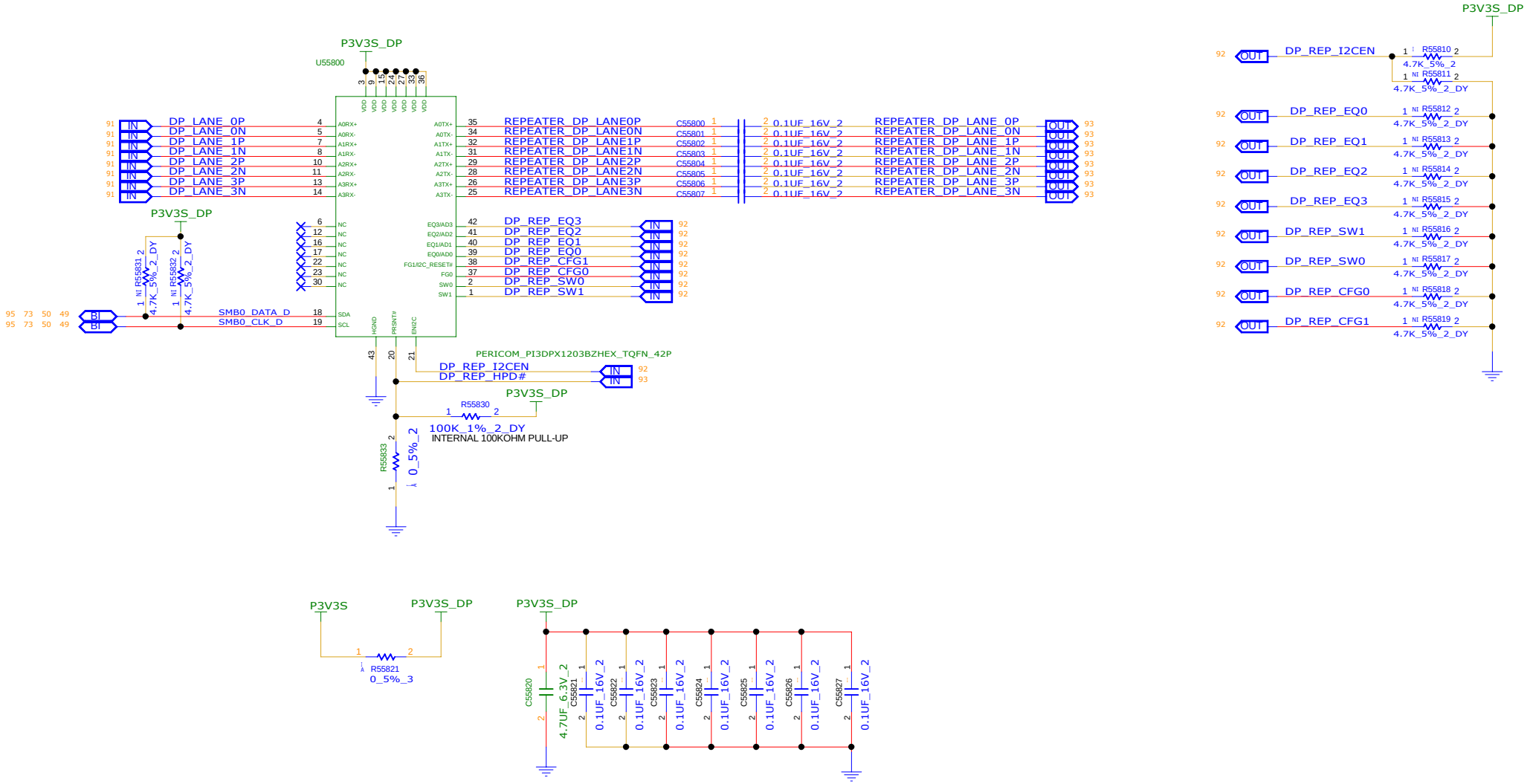


51600 - 51699

DP REDRIVER



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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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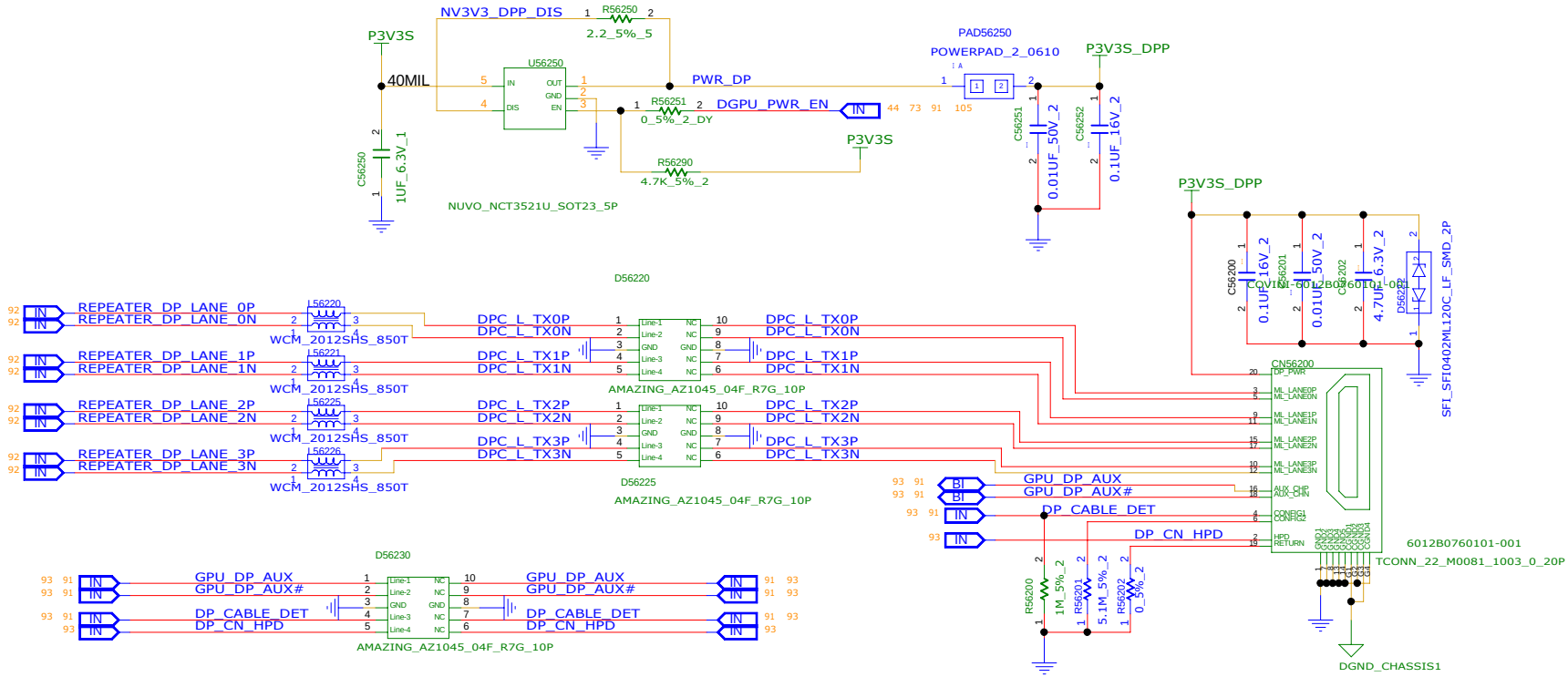

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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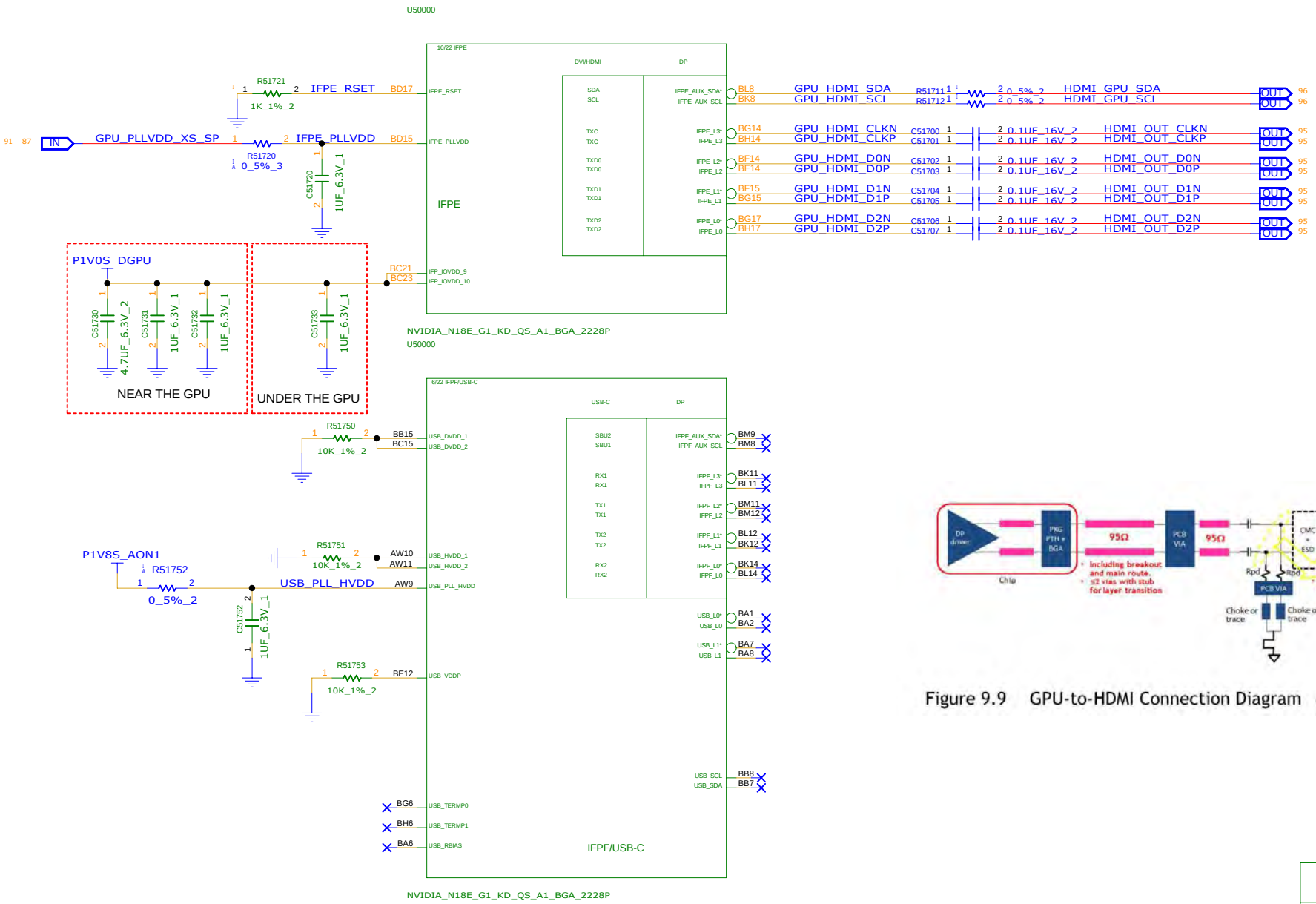

Figure 9.9 GPU-to-HDMI Connection Diagram

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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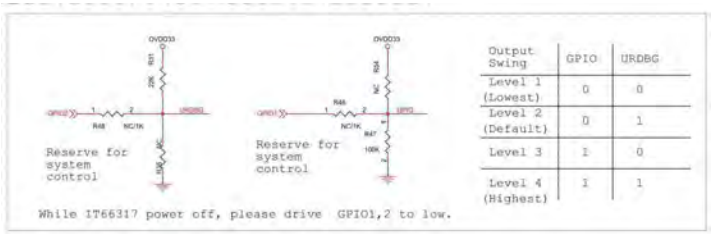
HDMI 2.0 RETIMER



Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

HDMI HPD TO MB

DP HPD TO GPU

TO MAINBOARD

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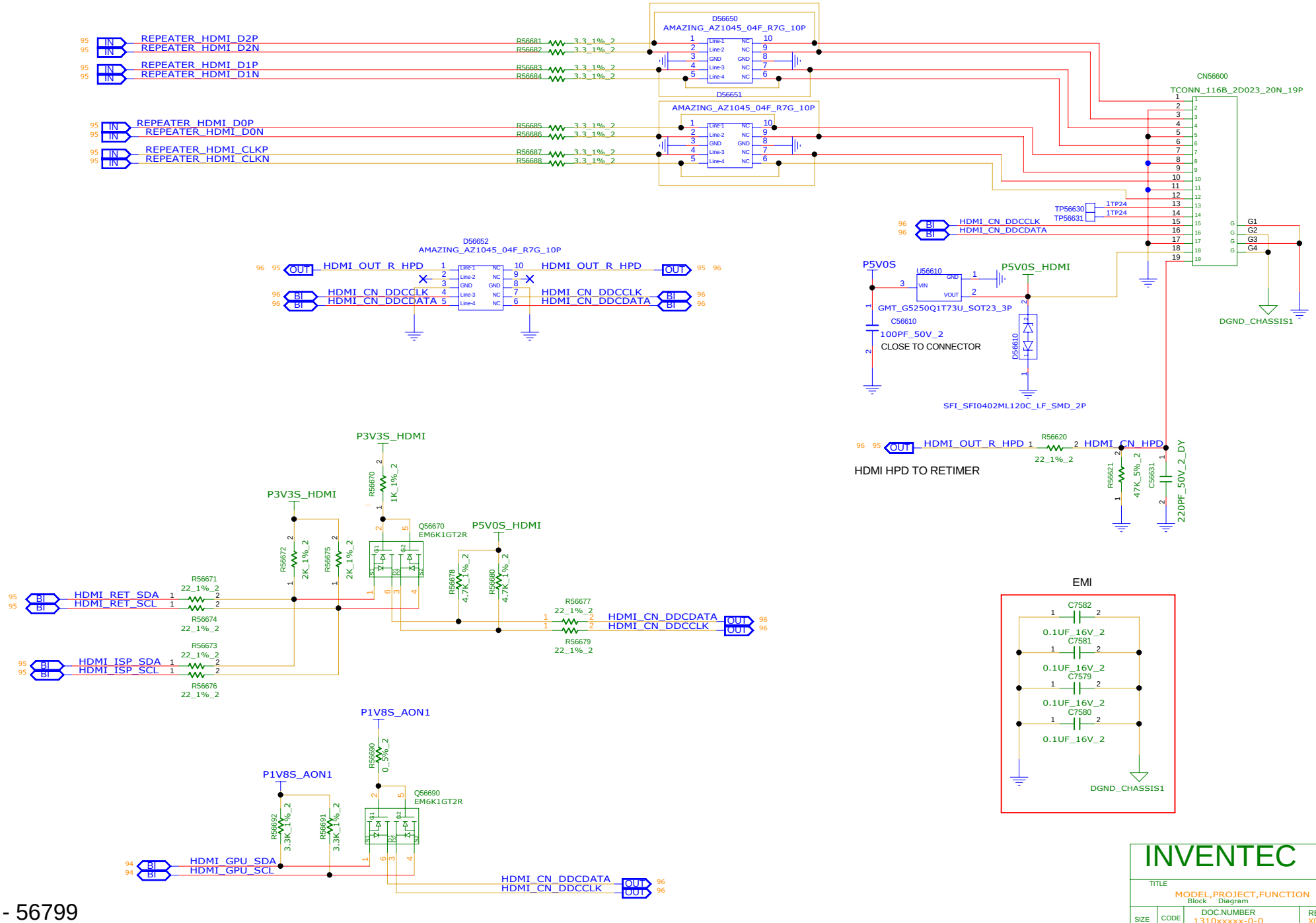
PCB VER	XXX

INVENTEC



56600 - 56799

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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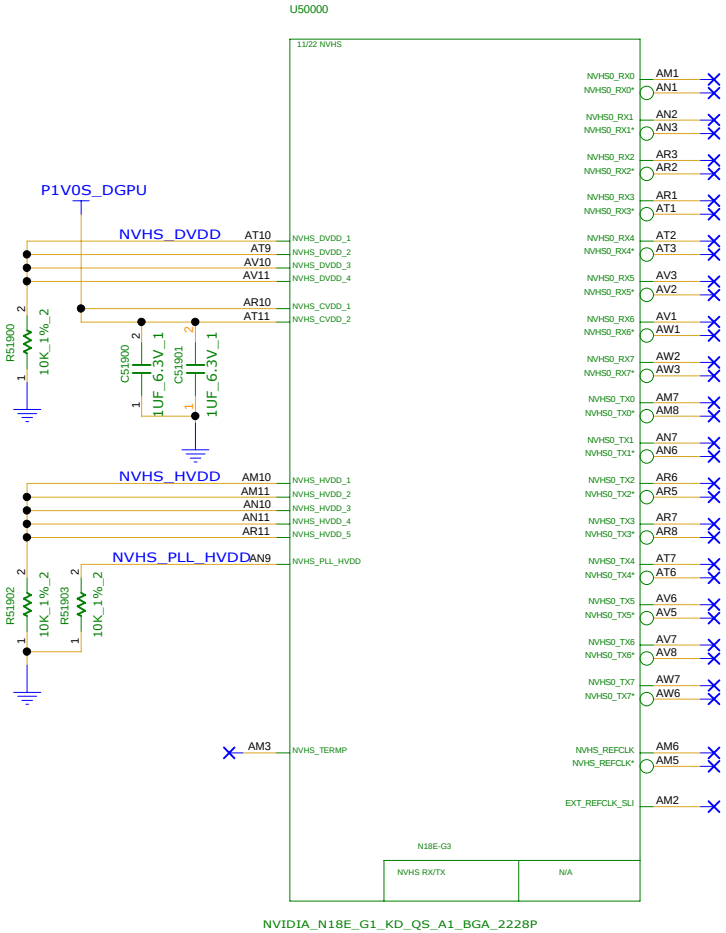

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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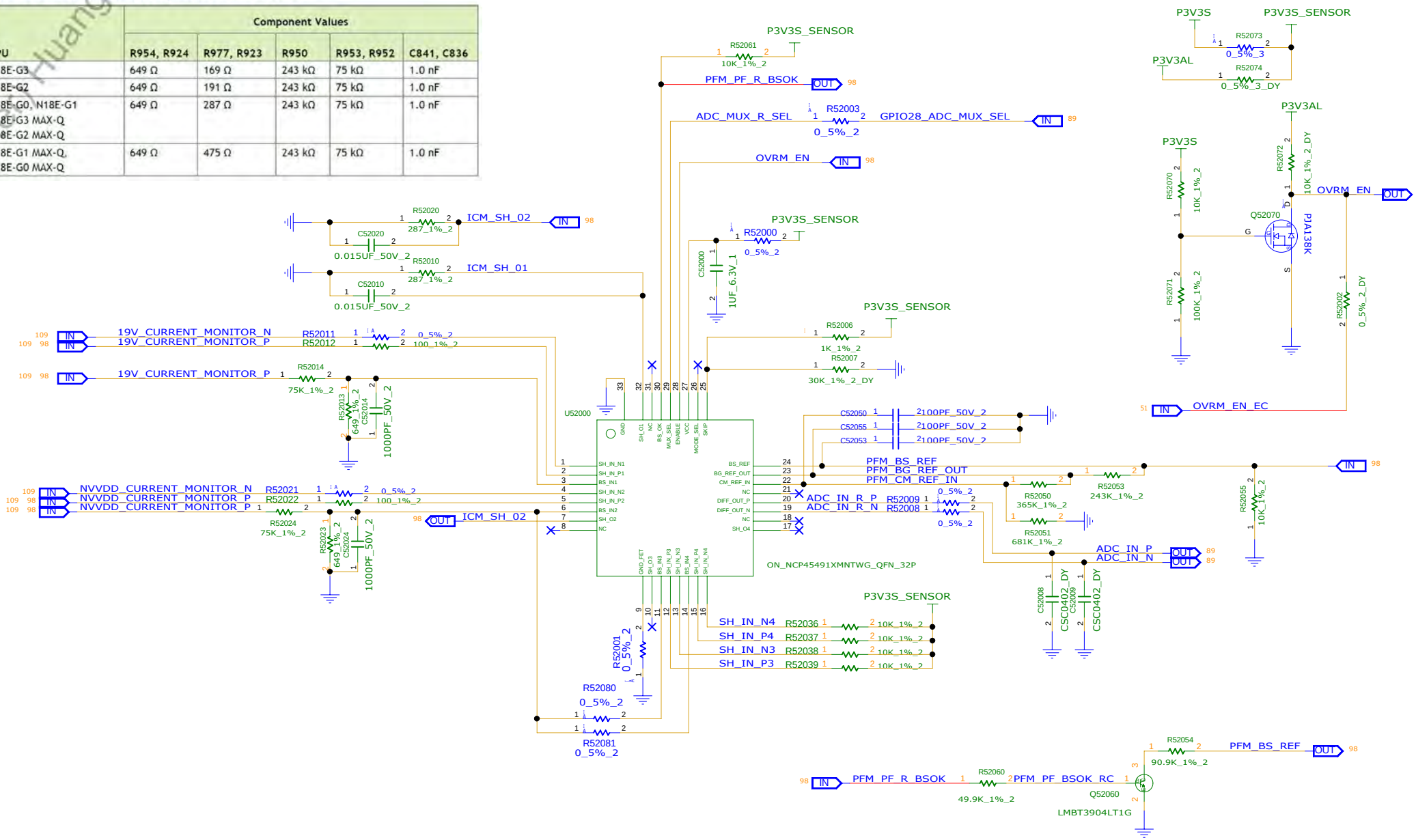
Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1 N18E-G3 MAX-Q N18E-G2 MAX-Q	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G1 MAX-Q, N18E-G0 MAX-Q	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF



52000 - 52099

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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SIZE	CODE	DOC.NUMBER	REV
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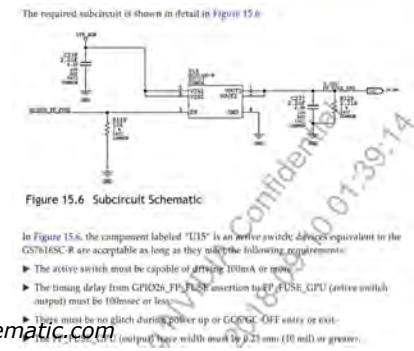
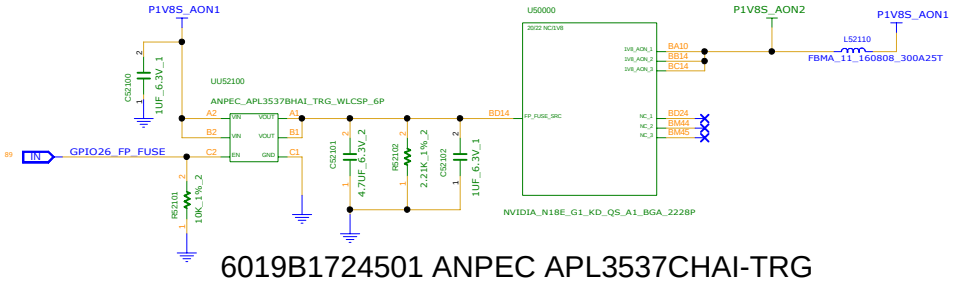


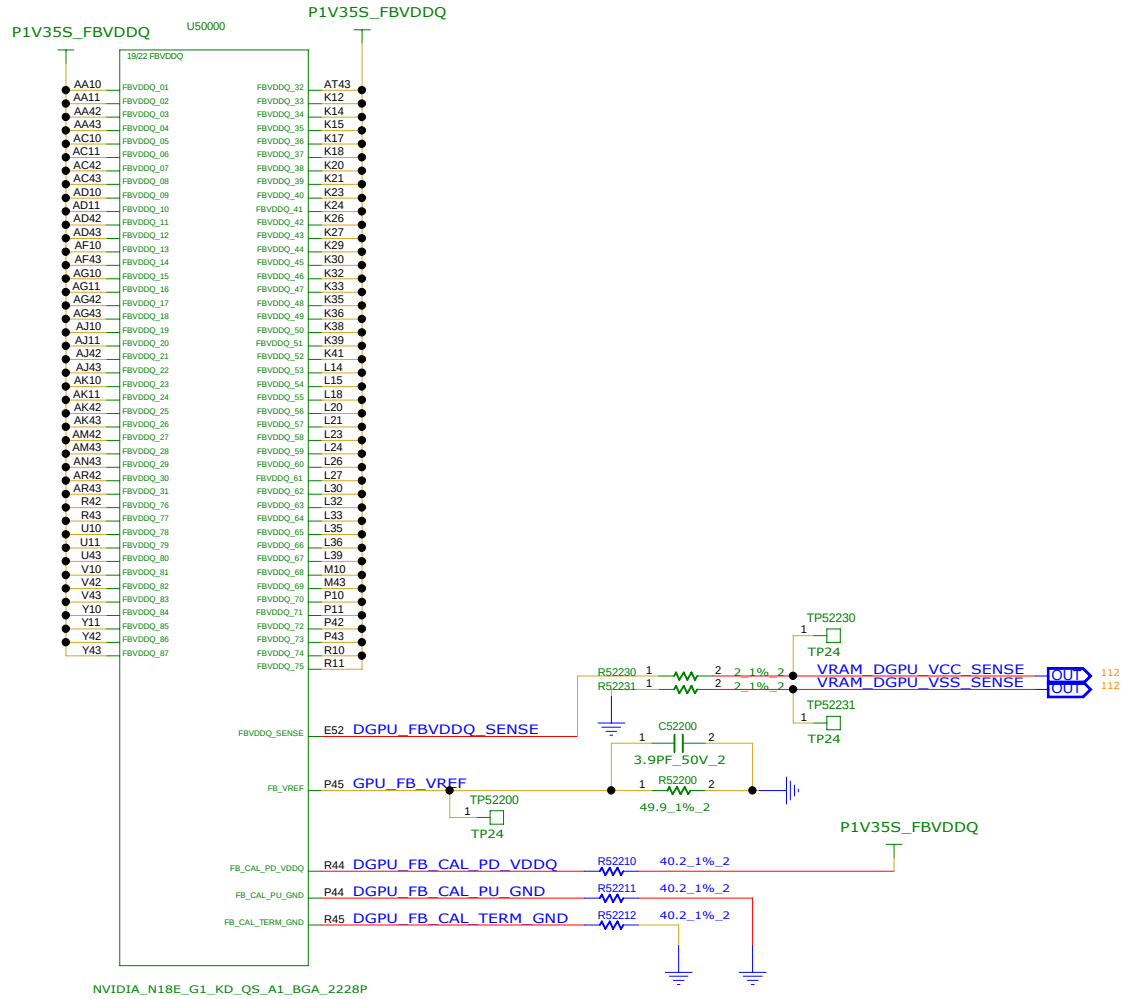


6019B1724501 ANPEC APL3537CHAI-TRG

52100 - 52199

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram



55600 - 55699

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INVENTEC

TITLE
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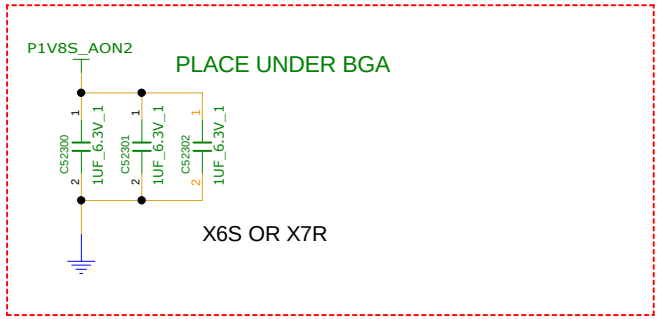
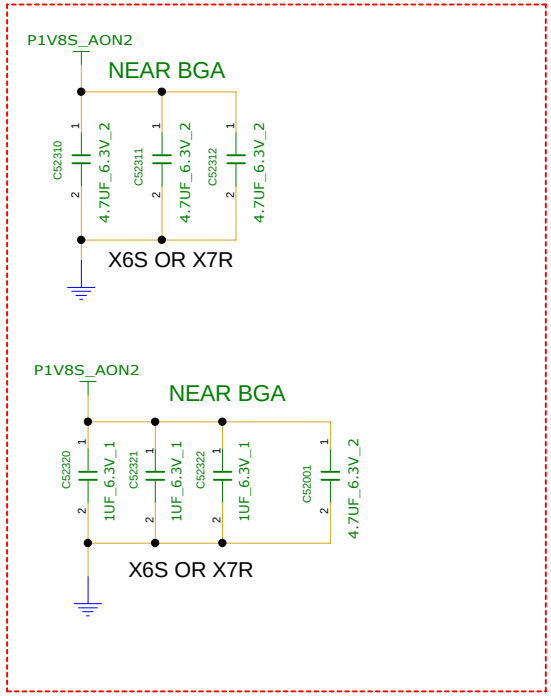
GPU 1V8_AON DECOUPLING





1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S)	3 x 1uF (0402 X6S) 3 x 4.7uF (0603 X6S)
			Alternate solution: 3 x 1.0uF (0201W X6S)	

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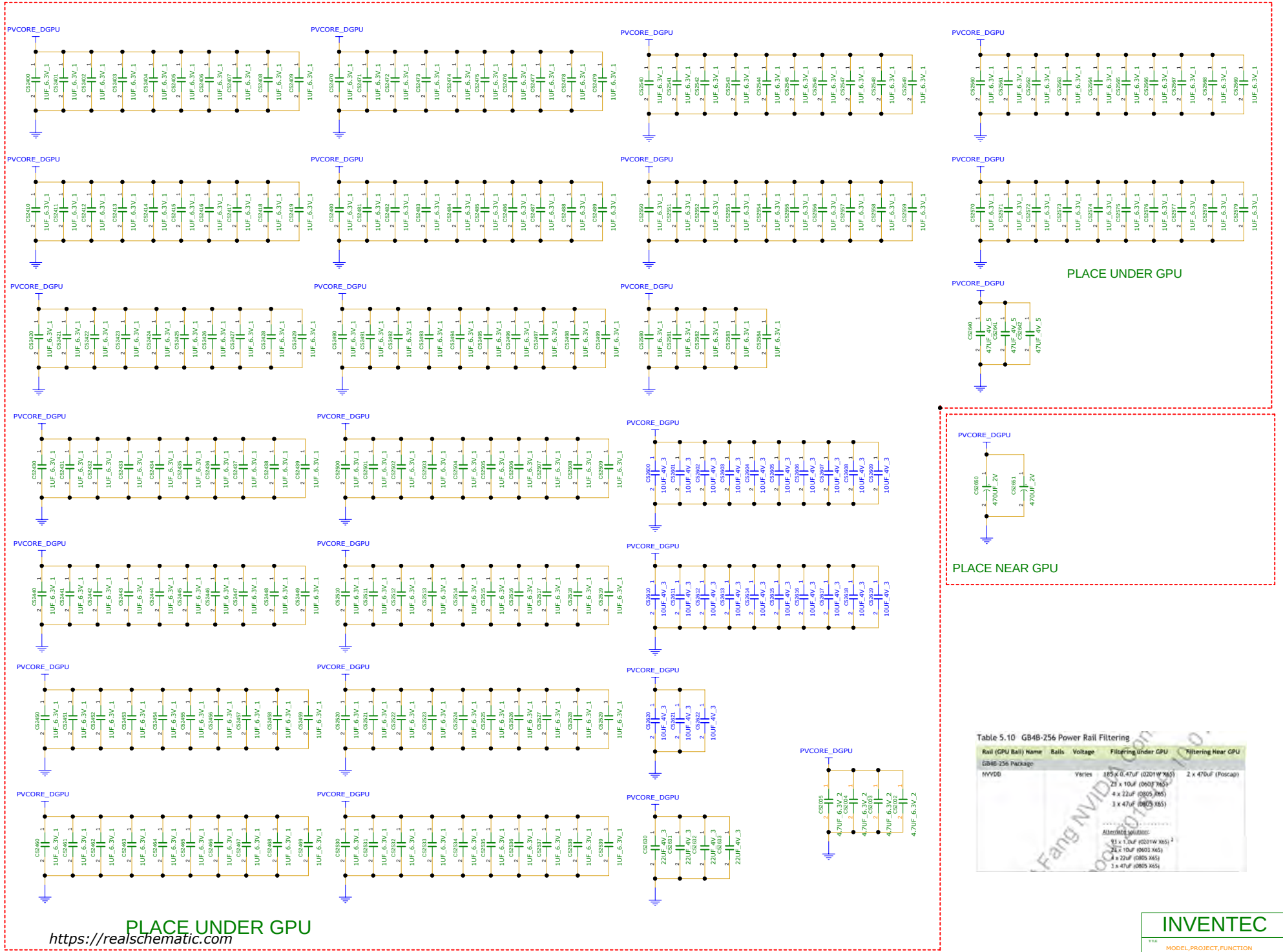
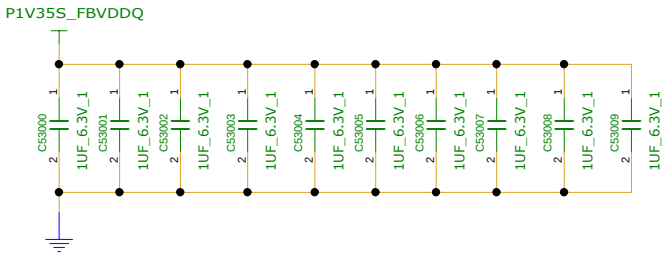
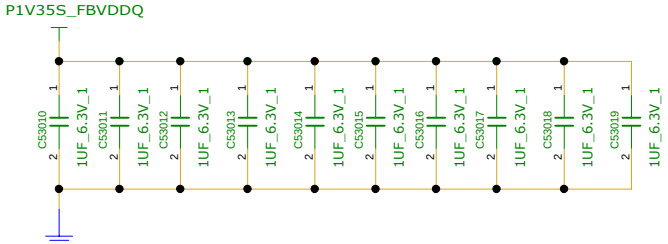
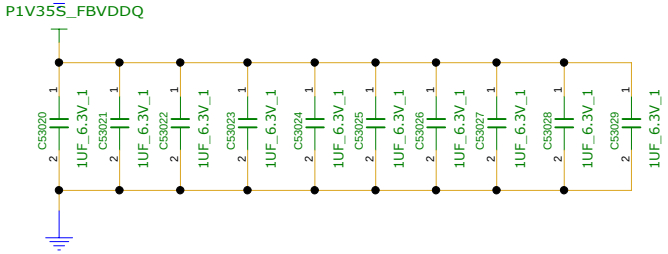
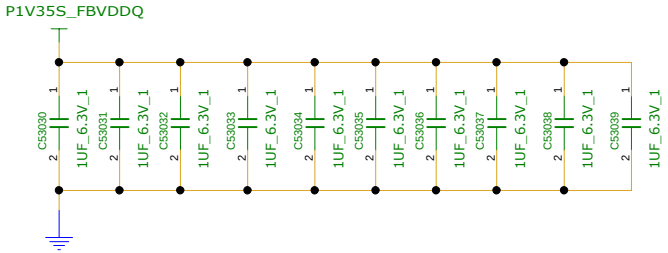
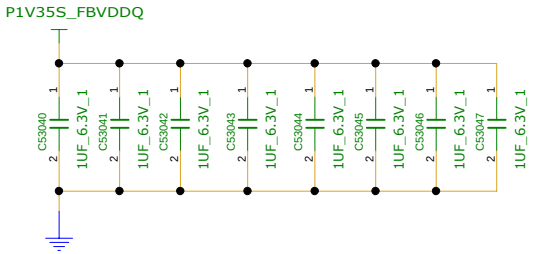




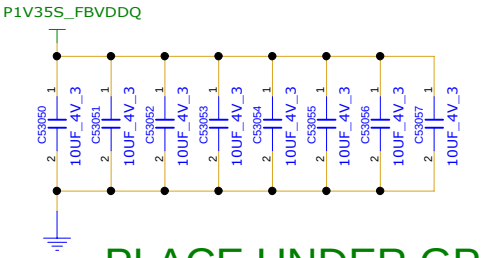




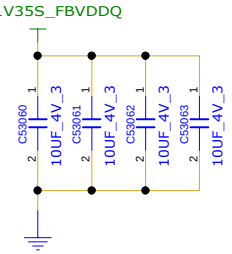




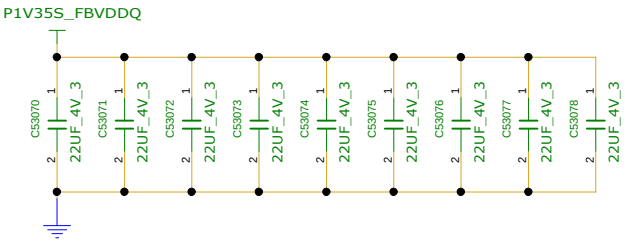
PLACE UNDER GPU



PLACE UNDER GPU



PLACE NEAR GPU



FBVDDQ (GPU side)[1]	1.25V 1.35V	48 x 0.47uF (0201W X6S) 8 x 10uF (0603 X6S) --- Alternate solution: 24 x 1.0uF (0201W X6S)[2] 8 x 10uF (0603 X6S)	4 x 10uF (0603 X6S) 9 x 22uF (0603 X6S)

INVENTEC

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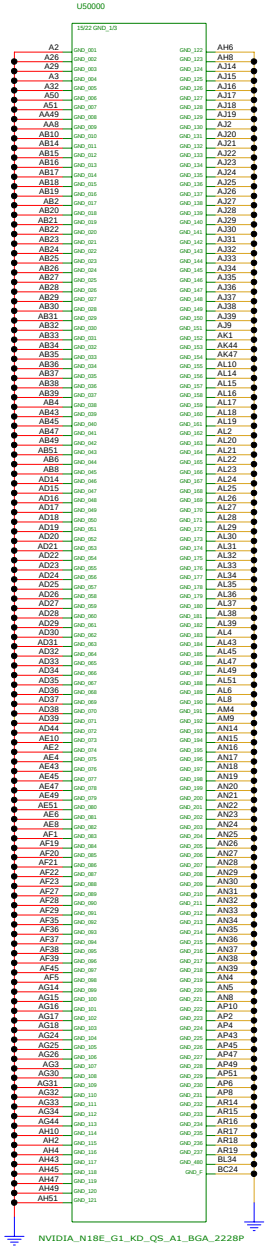
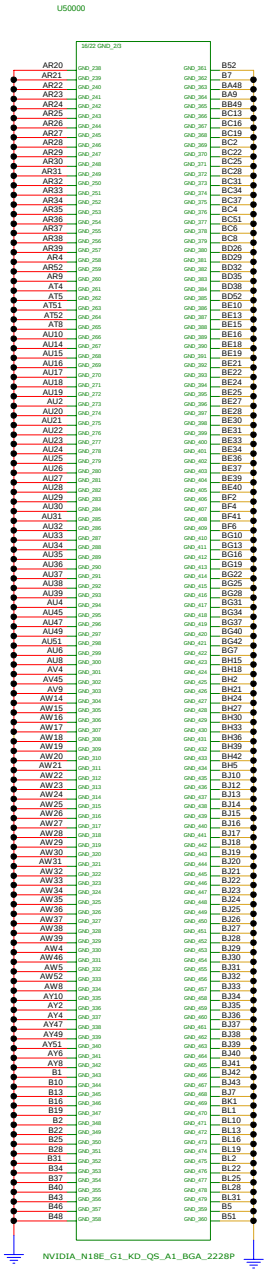
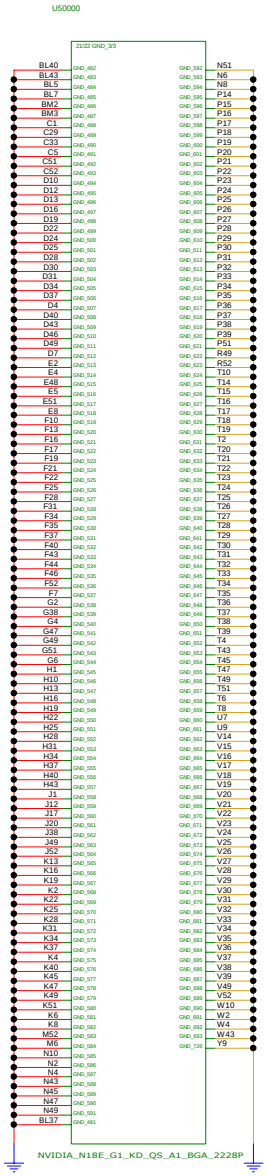
GND







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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-D-D	X01

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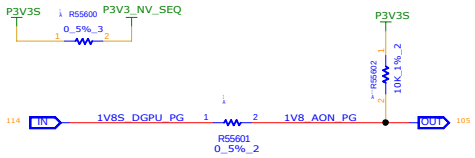
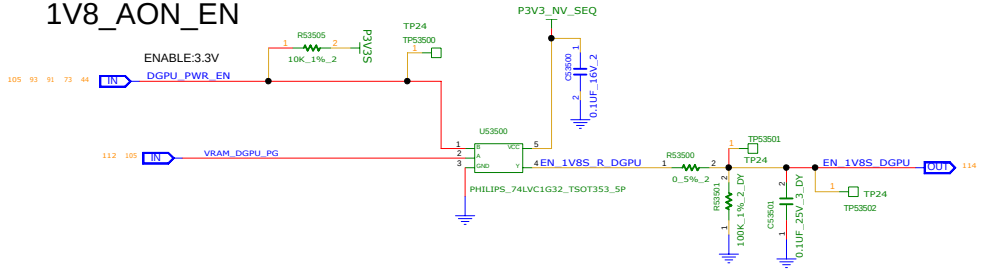
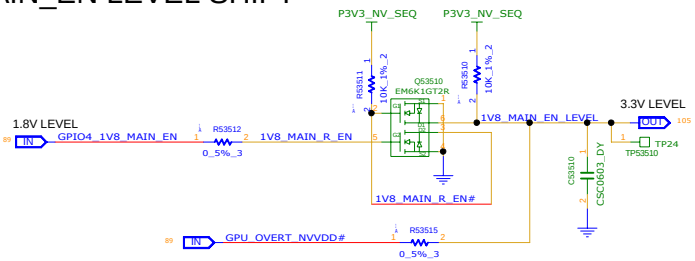


1V8_AON_EN



1V8_MAIN_EN LEVEL SHIFT



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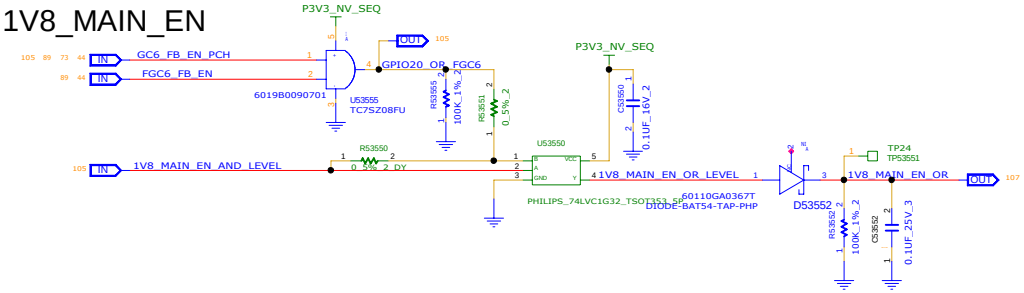
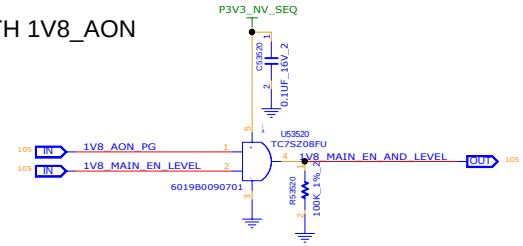
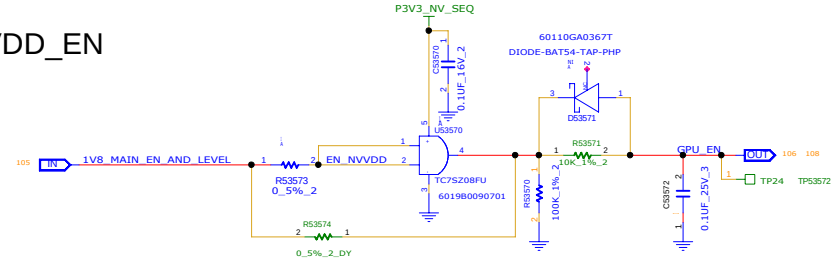


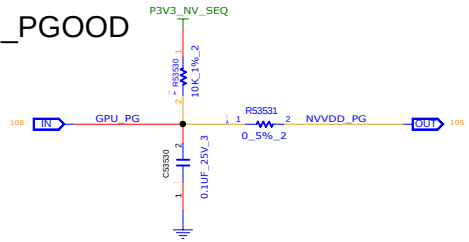
1V8_MAIN_EN AND WITH 1V8_AON



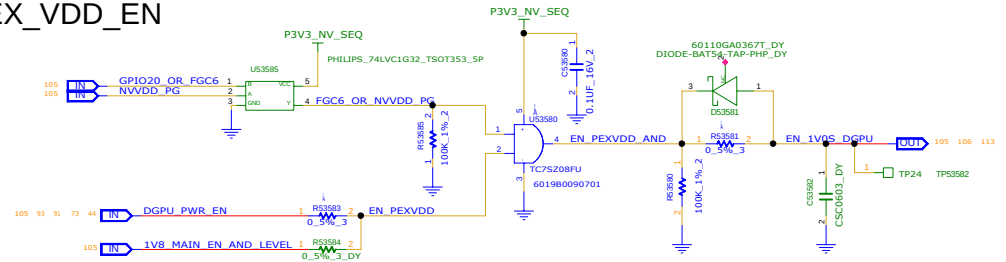
NVVDD_EN



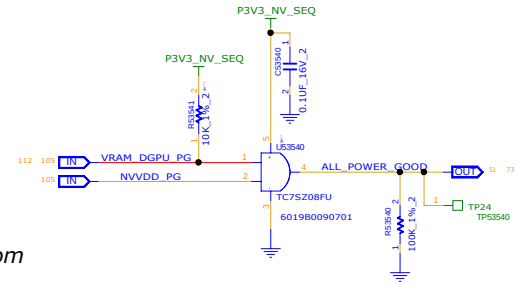
NVVDD_PGOOD



PEX_VDD_EN

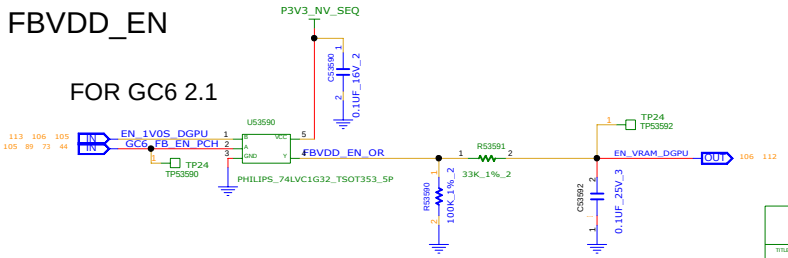


ALL POWER GOOD



FBVDD_EN

FOR GC6 2.1



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INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

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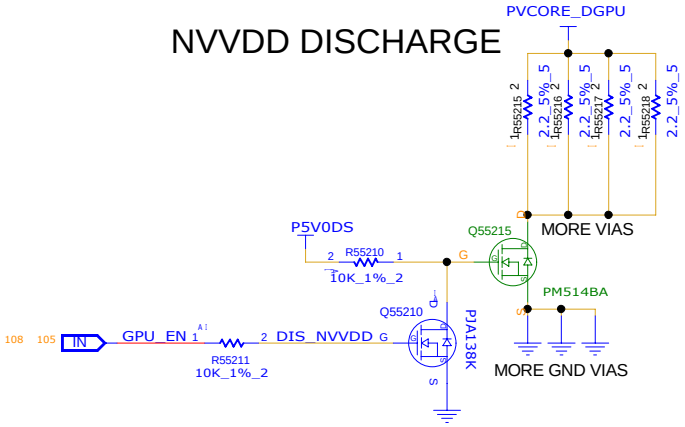
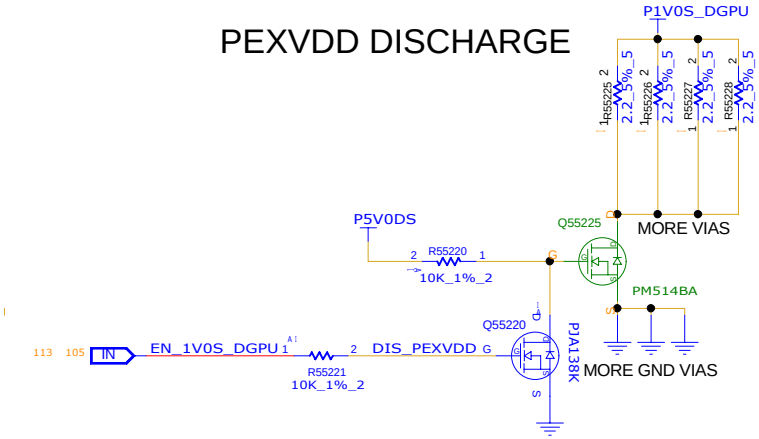
DISCHARGE CIRCUIT

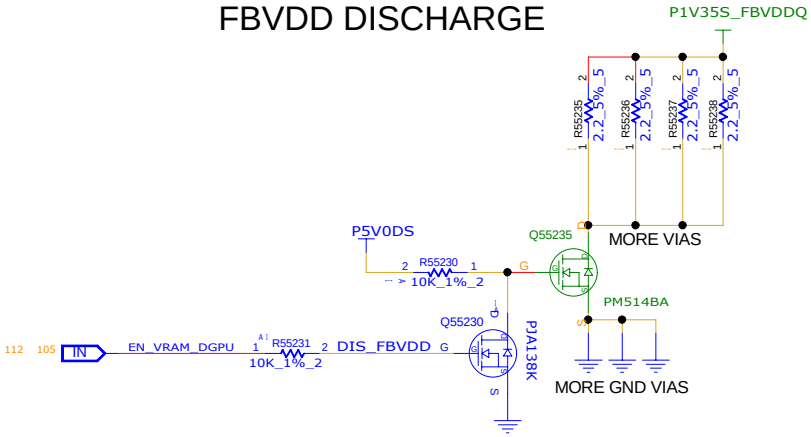
NVVDD DISCHARGE



PEXVDD DISCHARGE



FBVDD DISCHARGE



55200 - 55299

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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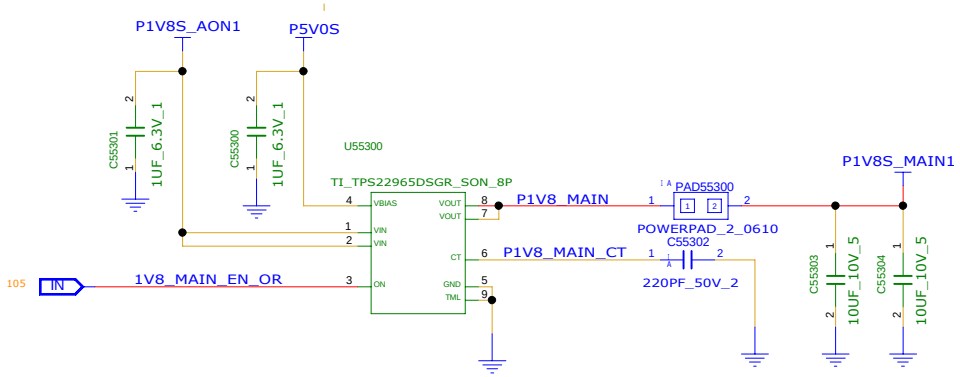
1V8_MAIN



55300 - 55399

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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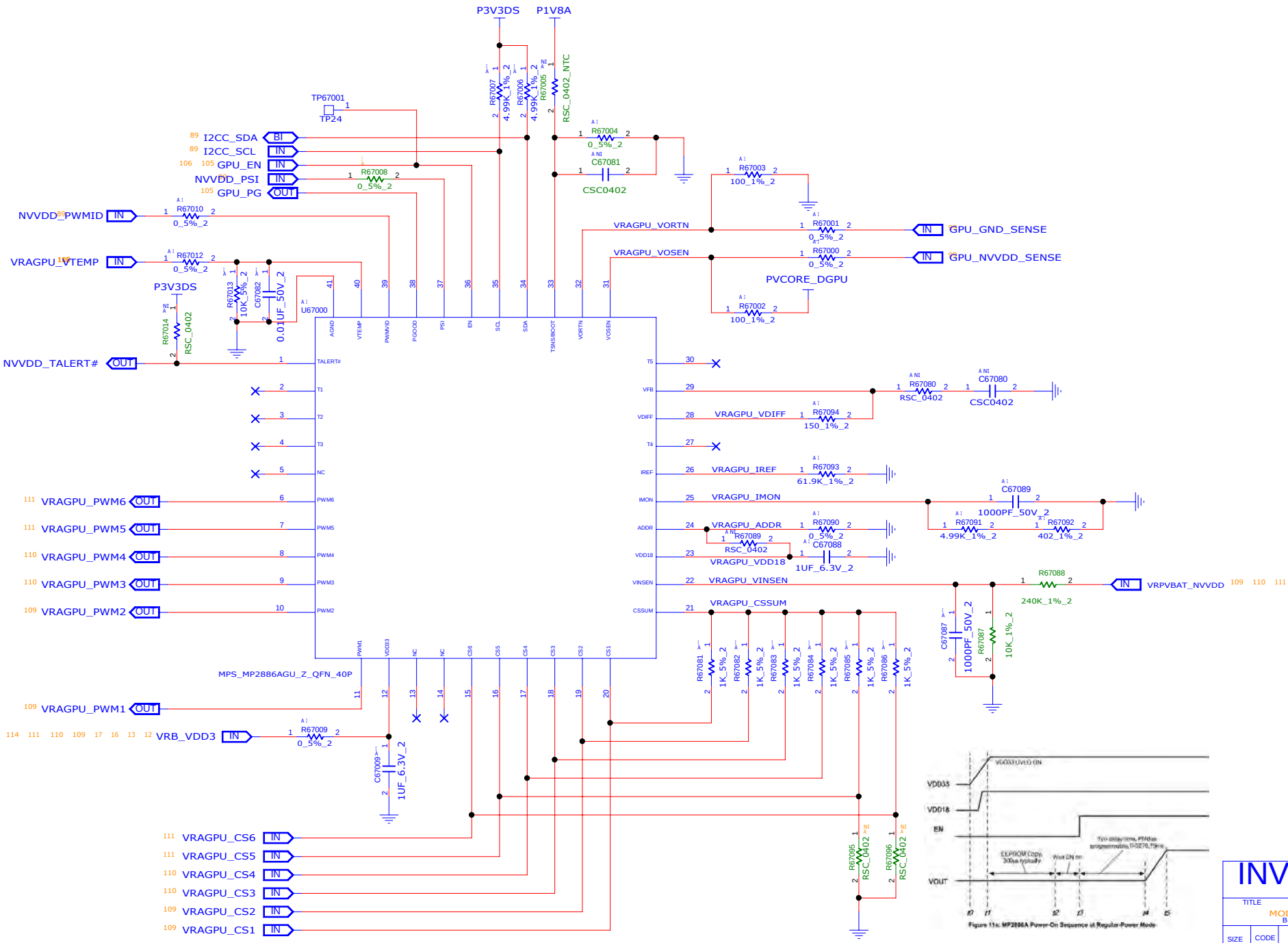

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TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
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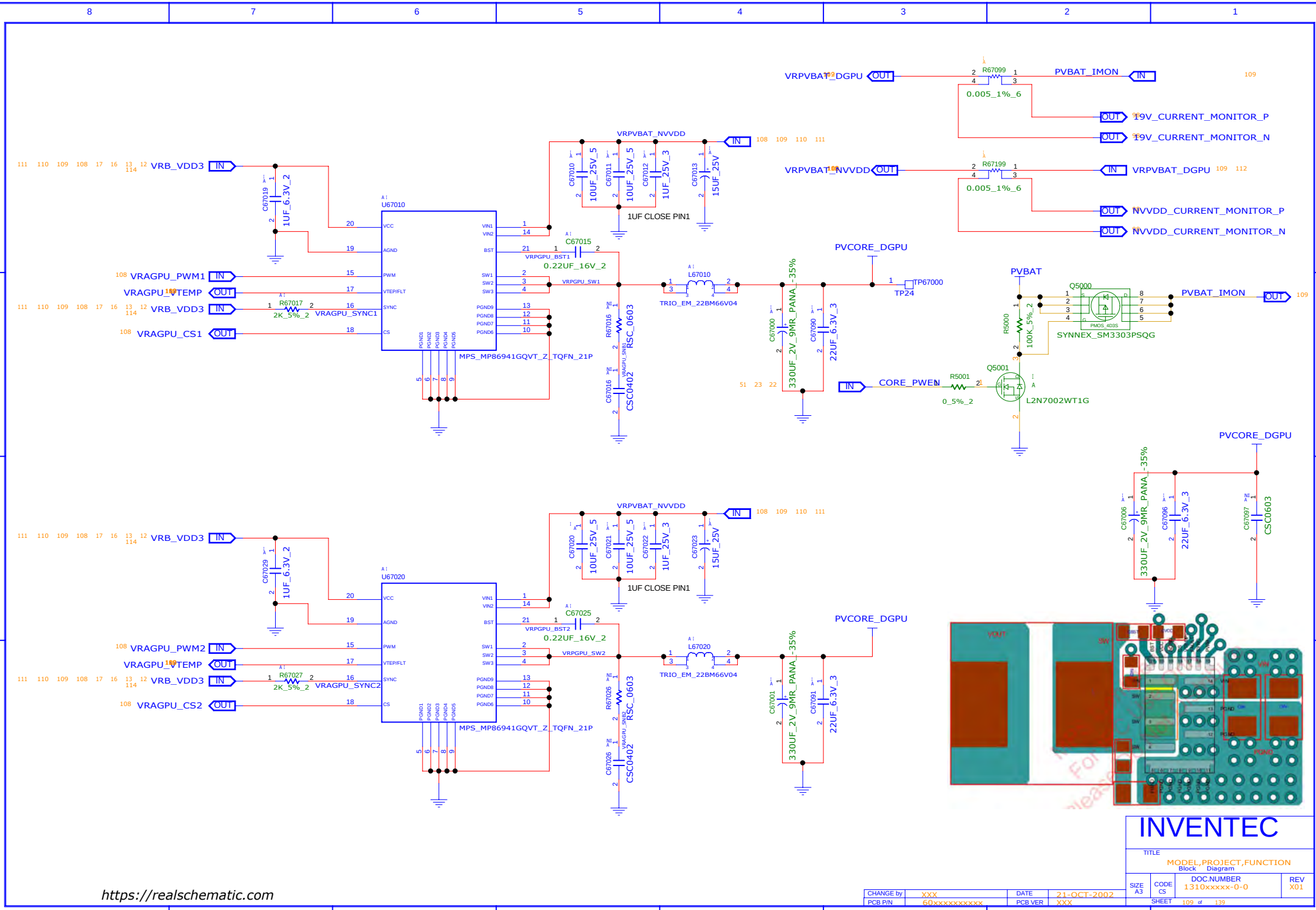

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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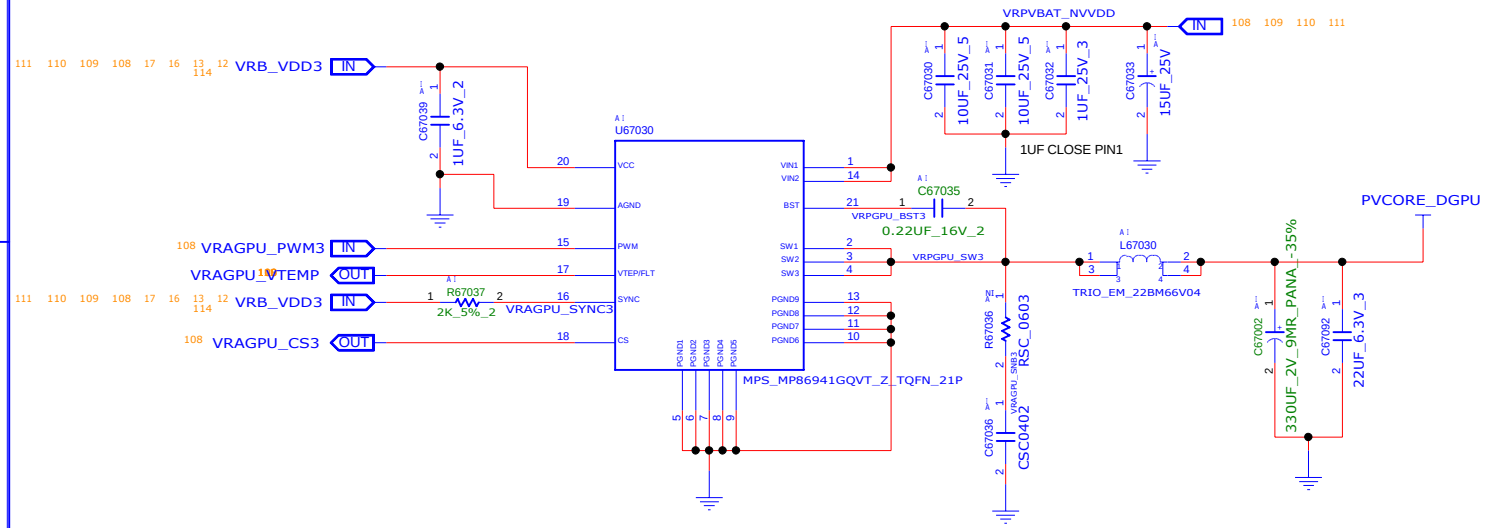

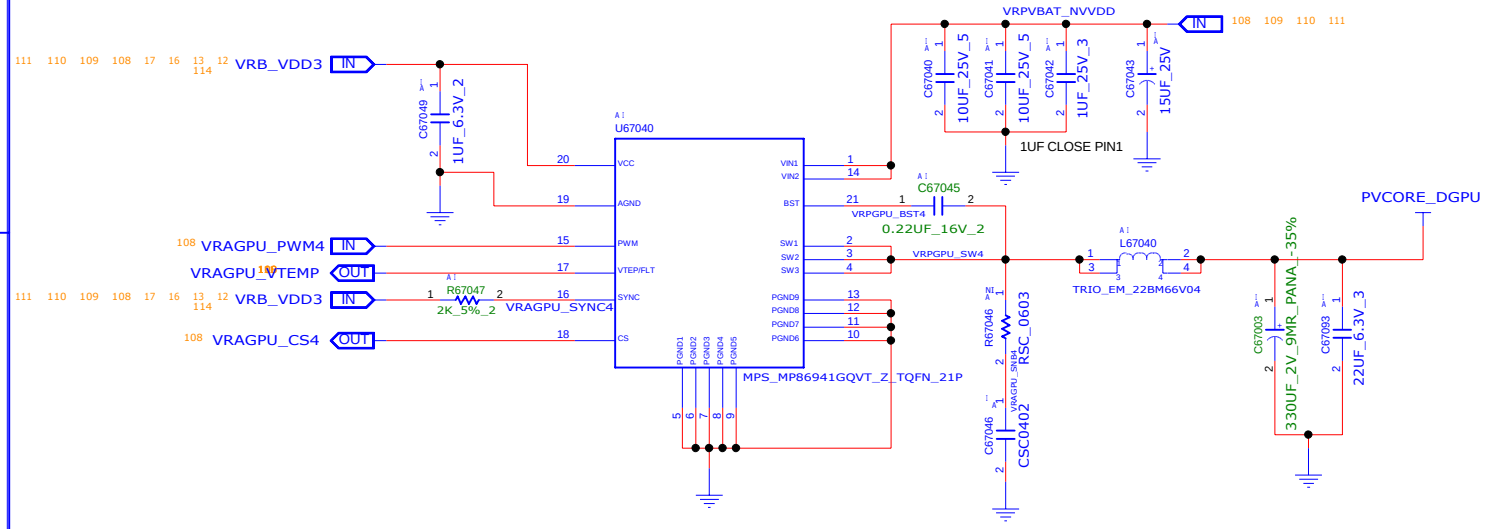

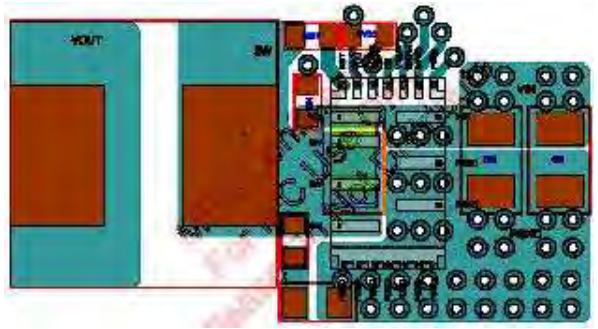

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		REV X01	
CHANGE by	XXX	DATE	21-OCT-2002	SHEET 110 of 139	
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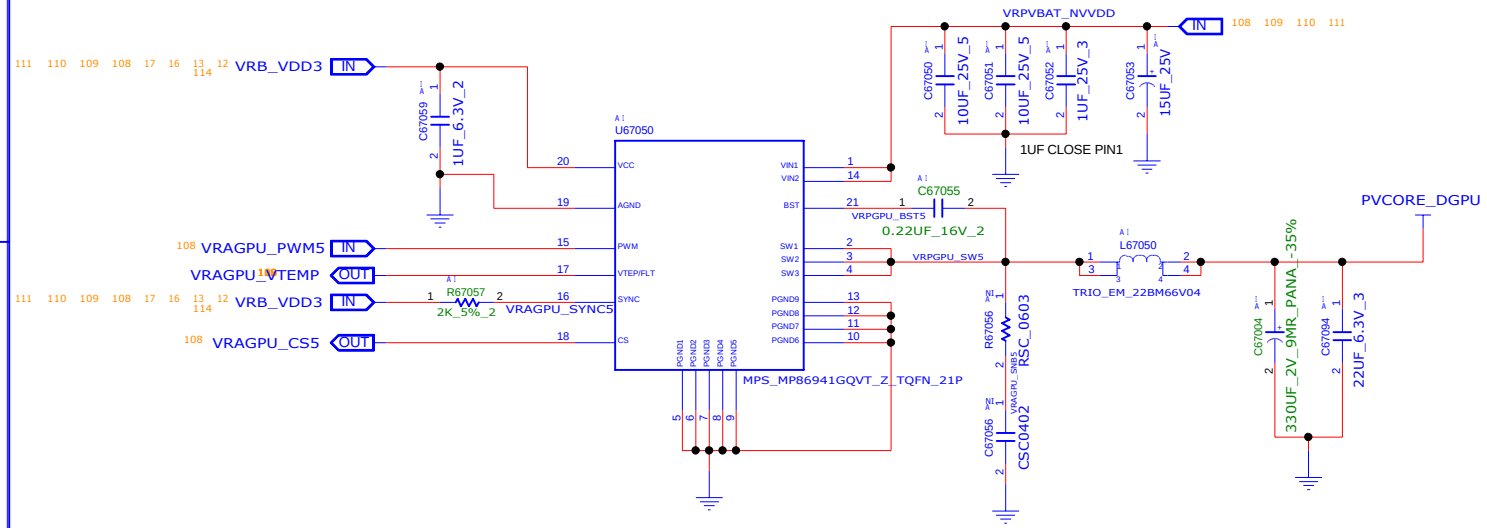

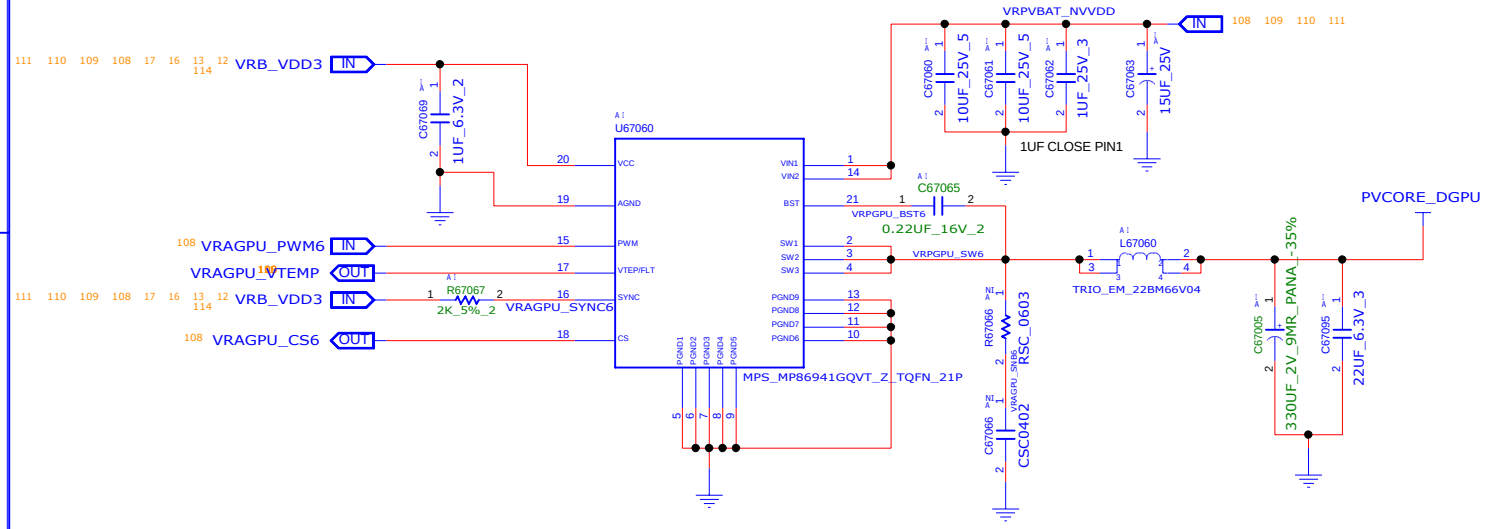

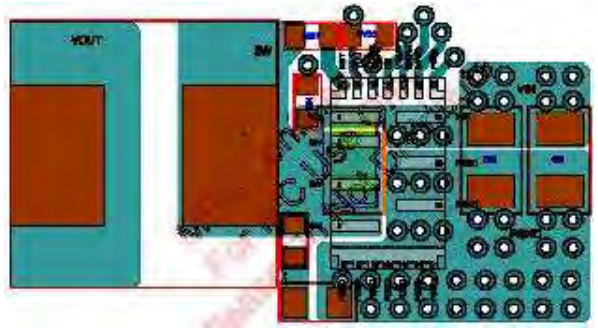

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
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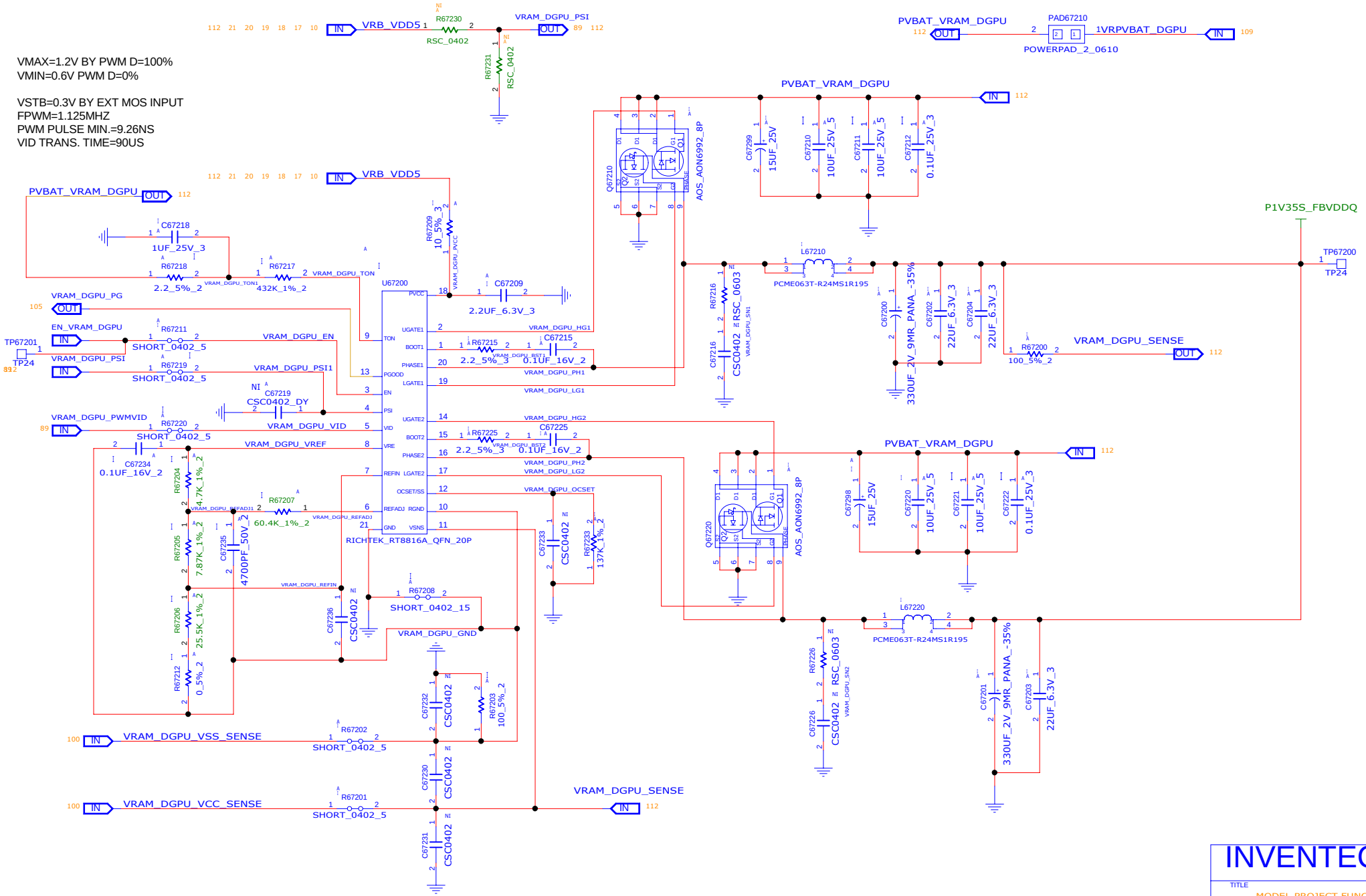
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VMIN=0.6V PWM D=0%
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US
VRB_VDD5
VRAM_DGPU_PSI
R67230
RSC_0402
R67231
PVBAT_VRAM_DGPU
PAD67210
1VRPVBAT_DGPU
POWERPAD_2_0610
AOS_AON6992_8P
C67299
15UF_25V
C67210
10UF_25V_5
C67211
C67212
0.1UF_25V_3
P1V35S_FBVDDQ
TP67200
TP24
L67210
PCME063T-R24MS1R195
R67216
RSC_0603
C67216
CSC0402
VRAM_DGPU_SN1
C67200
330UF_2V_9MR_PANA_-35%
C67202
22UF_6.3V_3
C67204
R67200
100_5%_2
VRAM_DGPU_SENSE
C67218
1UF_25V_3
R67218
2.2_5%_2
R67217
432K_1%_2
VRAM_DGPU_TON
VRAM_DGPU_TON1
R67209
10_5%_3
VRAM_DGPU_PVCC
C67209
2.2UF_6.3V_3
U67200
VRAM_DGPU_PG
EN_VRAM_DGPU
R67211
SHORT_0402_5
VRAM_DGPU_EN
TP67201
VRAM_DGPU_PSI
R67219
VRAM_DGPU_PSI1
C67219
CSC0402_DY
VRAM_DGPU_VID
VRAM_DGPU_PWMVID
R67220
VRAM_DGPU_VREF
C67234
0.1UF_16V_2
R67204
4.7K_1%_2
VRAM_DGPU_REFADJ1
R67207
60.4K_1%_2
VRAM_DGPU_REFADJ
R67205
7.87K_1%_2
C67235
4700PF_50V_2
R67206
25.5K_1%_2
R67212
0_5%_2
VRAM_DGPU_REFIN
R67208
SHORT_0402_15
VRAM_DGPU_GND
RICHTEK_RT8816A_QFN_20P
VRAM_DGPU_HG1
R67215
2.2_5%_3
C67215
0.1UF_16V_2
VRAM_DGPU_BST1
VRAM_DGPU_PH1
VRAM_DGPU_LG1
VRAM_DGPU_HG2
R67225
C67225
VRAM_DGPU_BST2
VRAM_DGPU_PH2
VRAM_DGPU_LG2
VRAM_DGPU_OCSET
C67233
R67233
137K_1%_2
C67232
R67203
100_5%_2
R67202
SHORT_0402_5
VRAM_DGPU_VSS_SENSE
C67230
R67201
VRAM_DGPU_VCC_SENSE
C67231
C67298
C67220
C67221
C67222
L67220
R67226
C67226
C67201
C67203
22UF_6.3V_3
INVENTEC
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1310xxxxx-0-0
REV
X01
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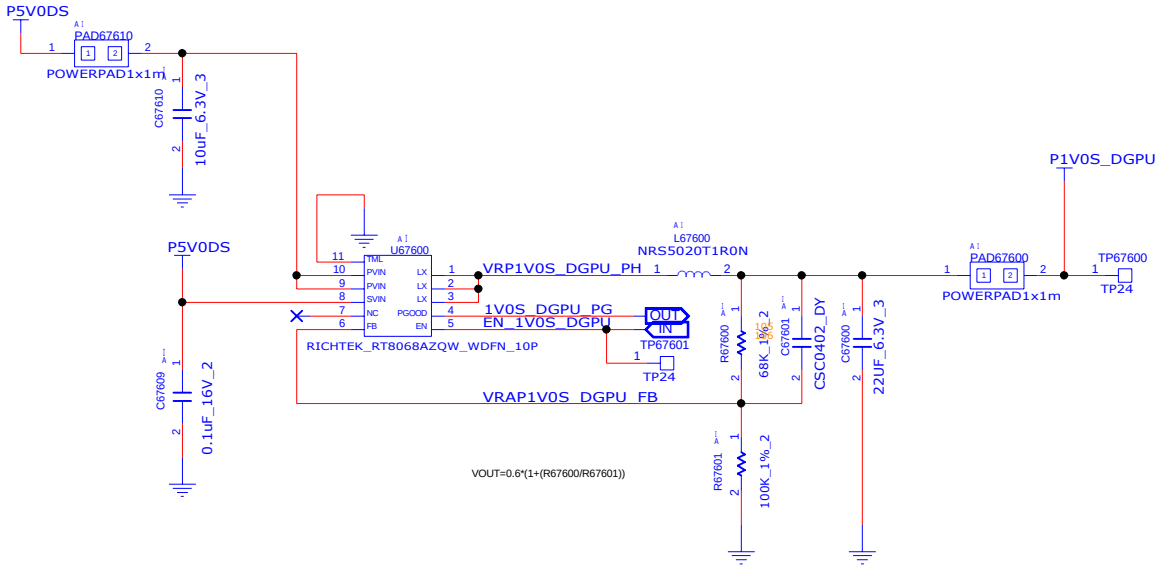
60xxxxxxxxxx
PCB VER
XXX
https://realschematic.com



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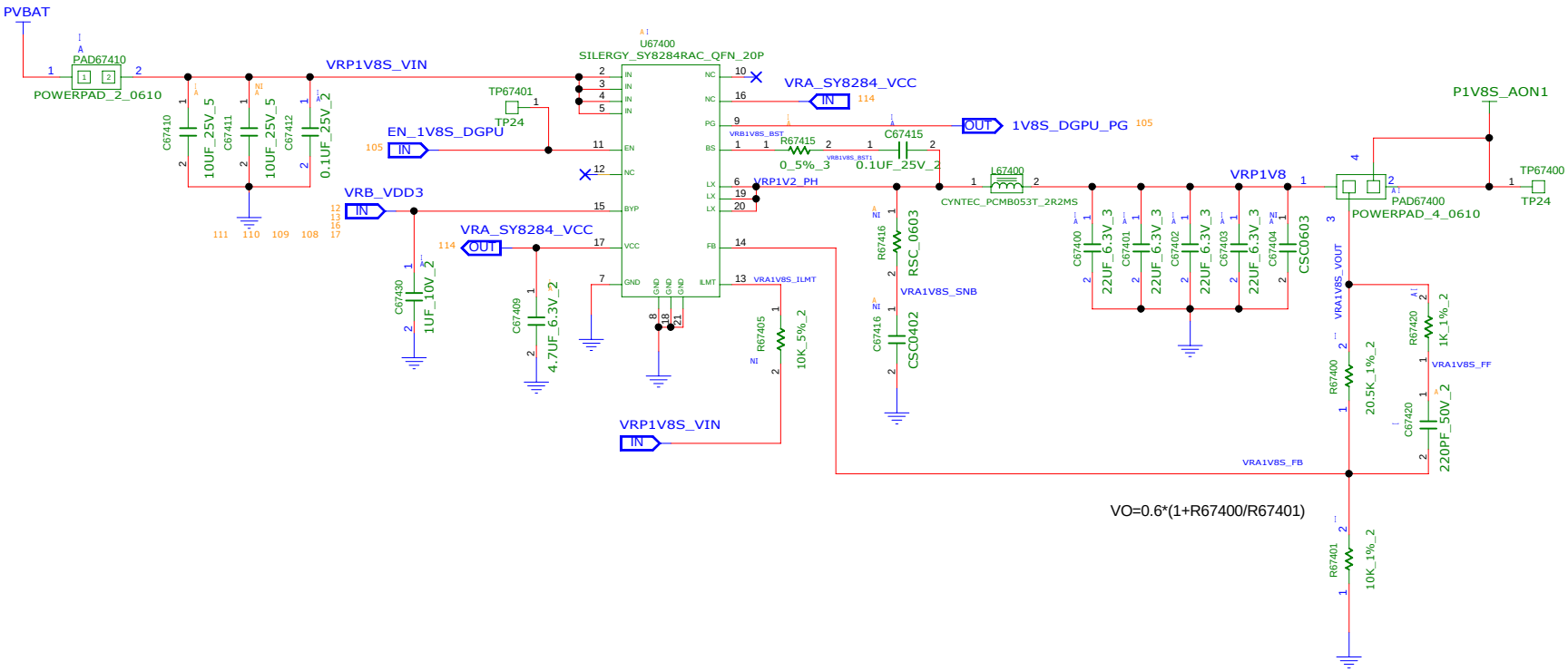

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Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms)[2] (A)	Input EDPp (5ms)[2] (A)	Input EDPc (1sec)[1] (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$Input\ EDPc\ Current\ (A) = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$Input\ EDPp\ (A) at\ V_{new} = Input\ EDPp(A)\ at\ 19V x\ \frac{19\text{V}}{V_{new}(\text{V})}$$

Table 12. Output EDP-Continuous

Product	TGP (W)	NVVDD – (A)	FB TOTAL[5] 1.35V[3, 4] (A)	1.0V Total[1] 1.0V[3] (A)	1.8V Total[2] 1.8V[3] (A)
N18E-G3	150	144	46	1.6	2.3
	160	152			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

Product	TGP (W)	NVVDD - (A)	FB TOTAL[4] 1.35V[2, 3] (A)	1.0V Total[1] 1.0V[2] (A)	1.8V Total[2] 1.8V[5] (A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

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HISTORY

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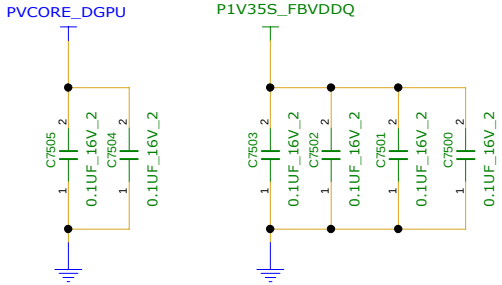
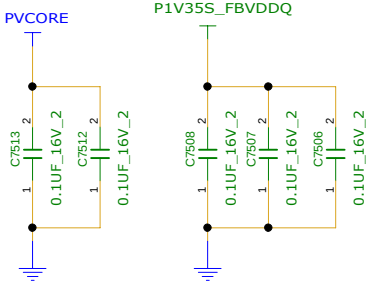
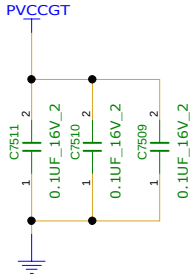
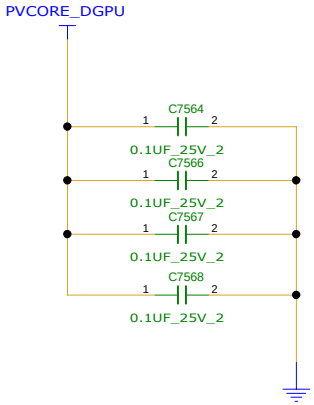
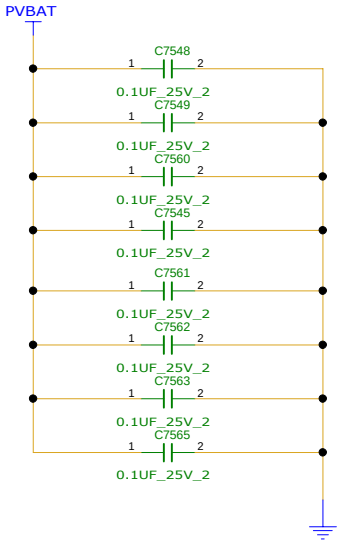
EMI

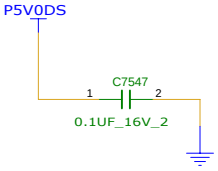


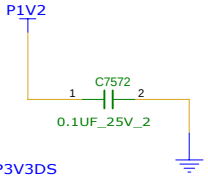


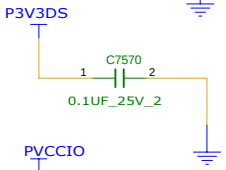


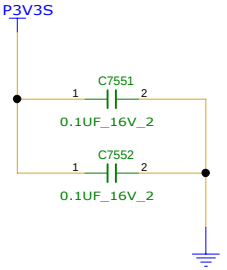


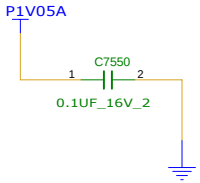


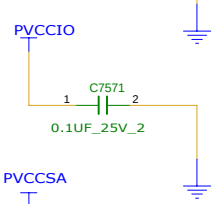


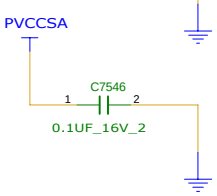












INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
NFC CNNN.

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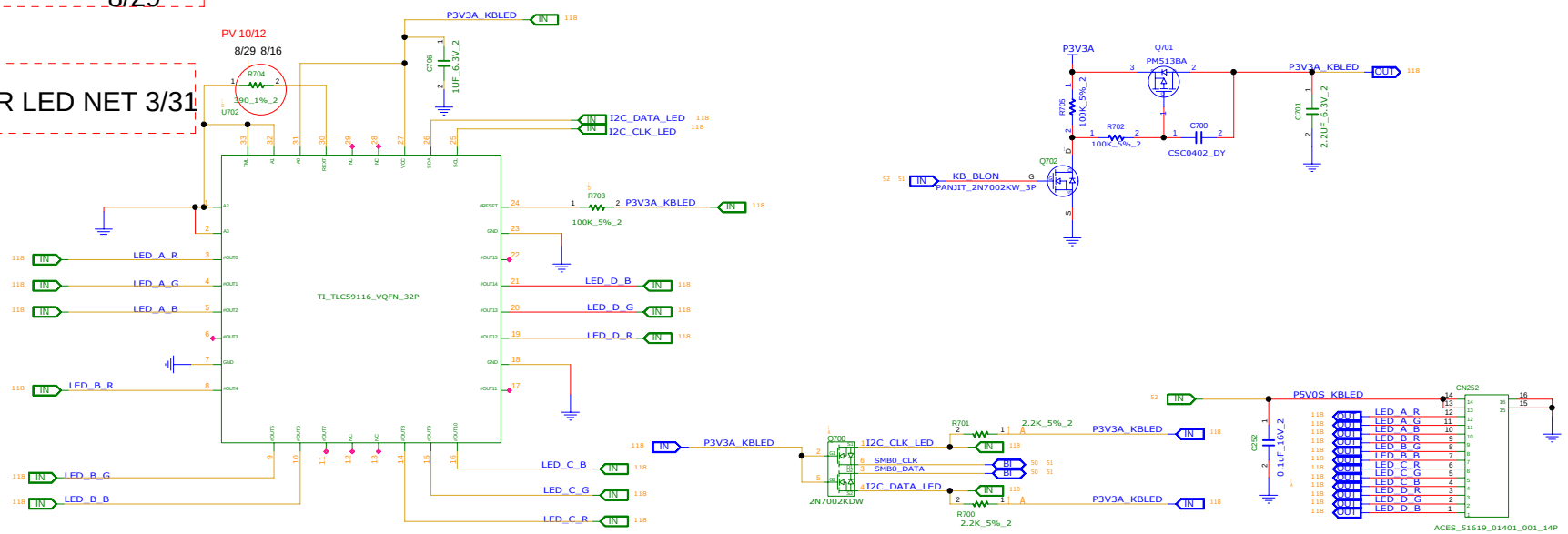
ADJUST LED RES 8/16
8/29

RE-ORDER LED NET 3/31



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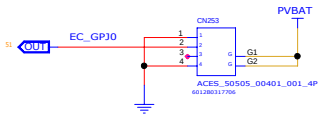

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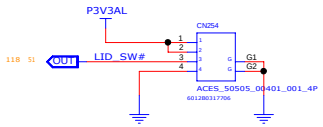

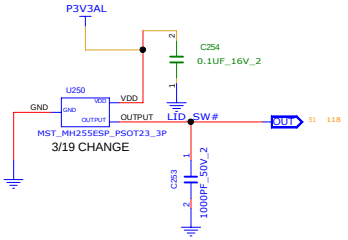

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REFERENCE NUMBER:700~800

INVENTEC

MODEL,PROJECT,FUNCTION
RING LED

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TURBO# BOARD

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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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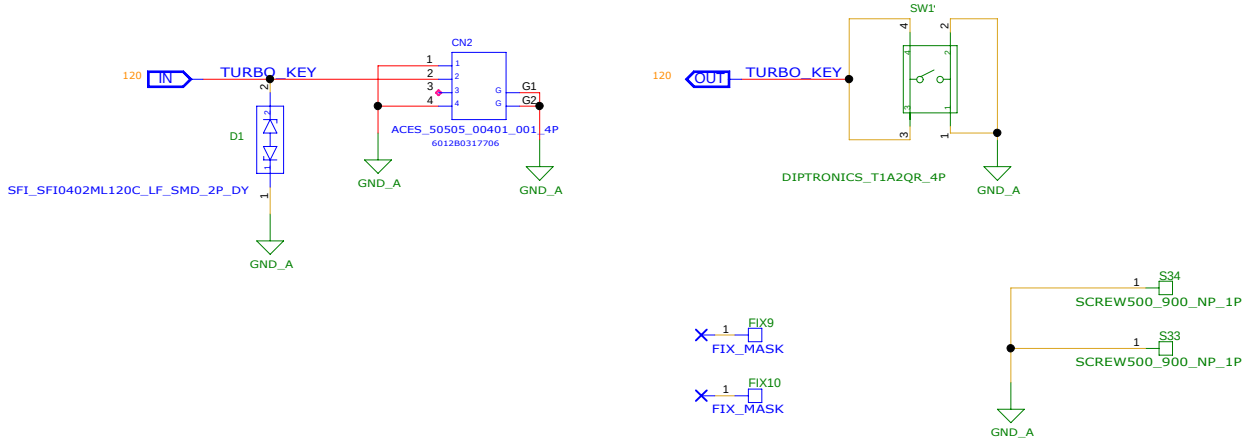
TURBO#



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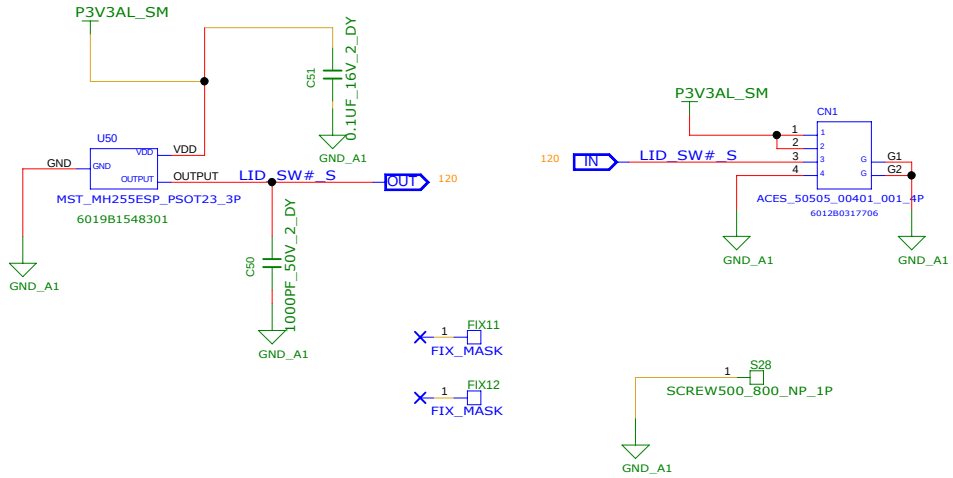

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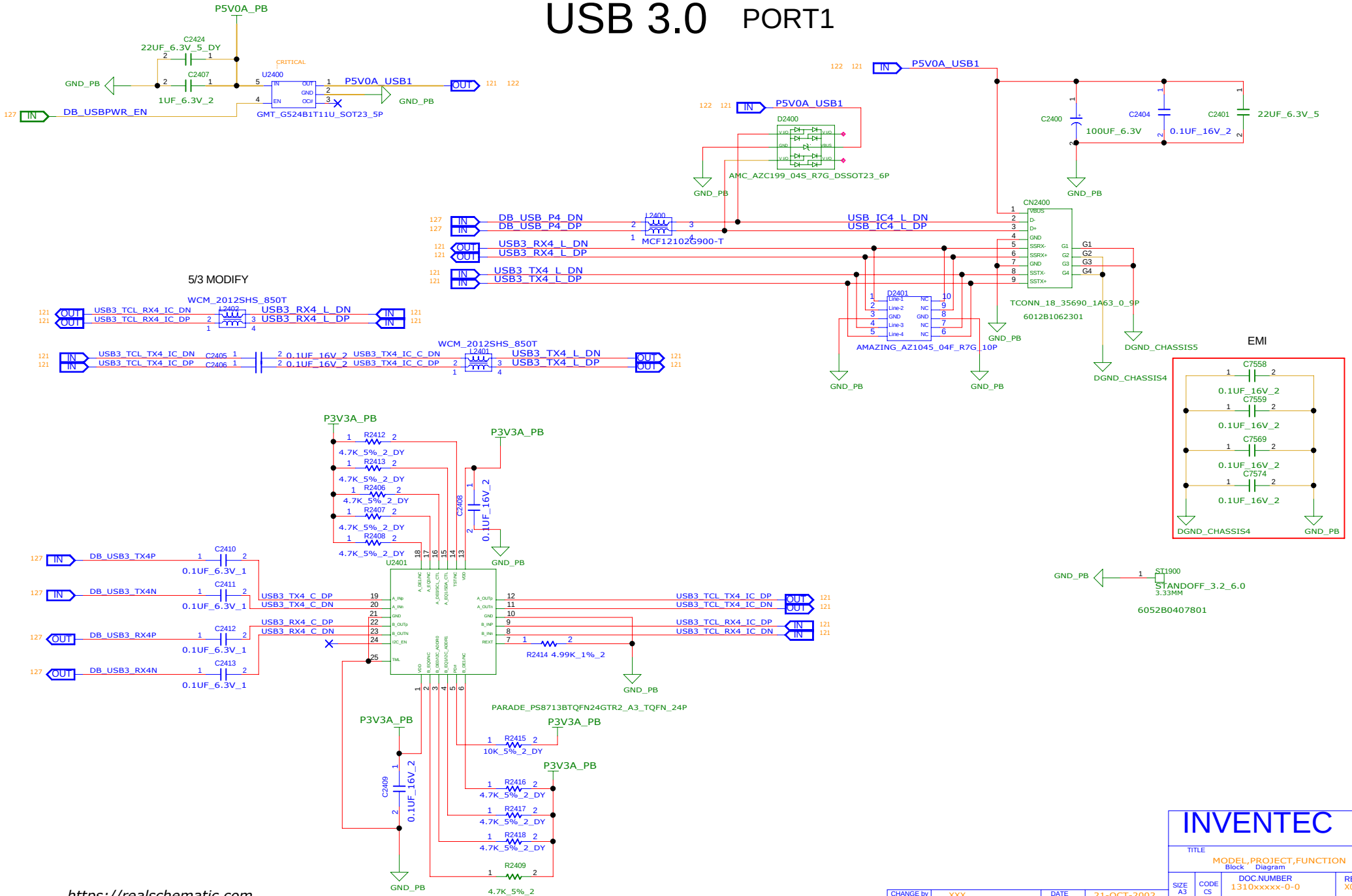
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



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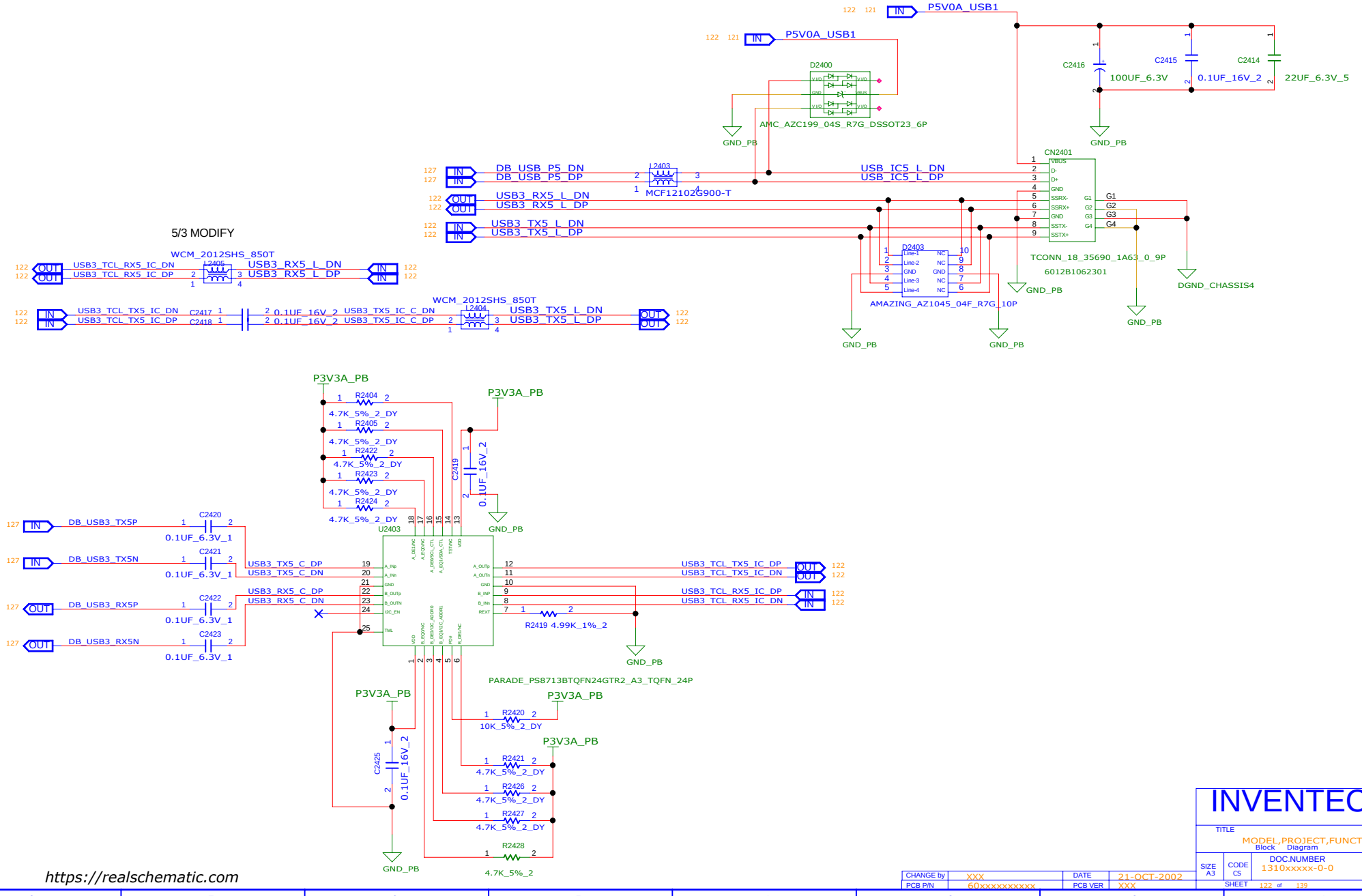
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



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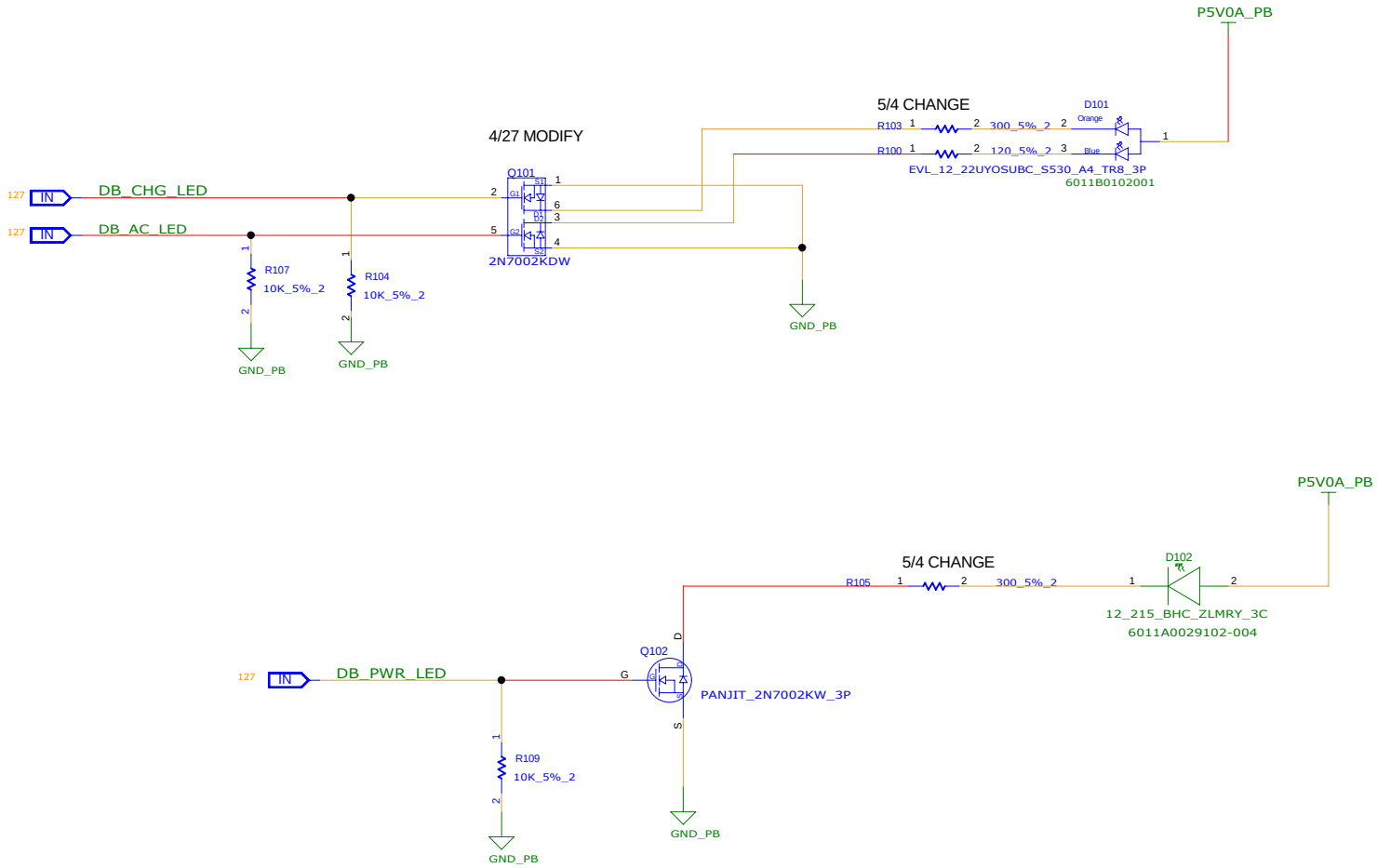

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LAN (CONTROLLER)
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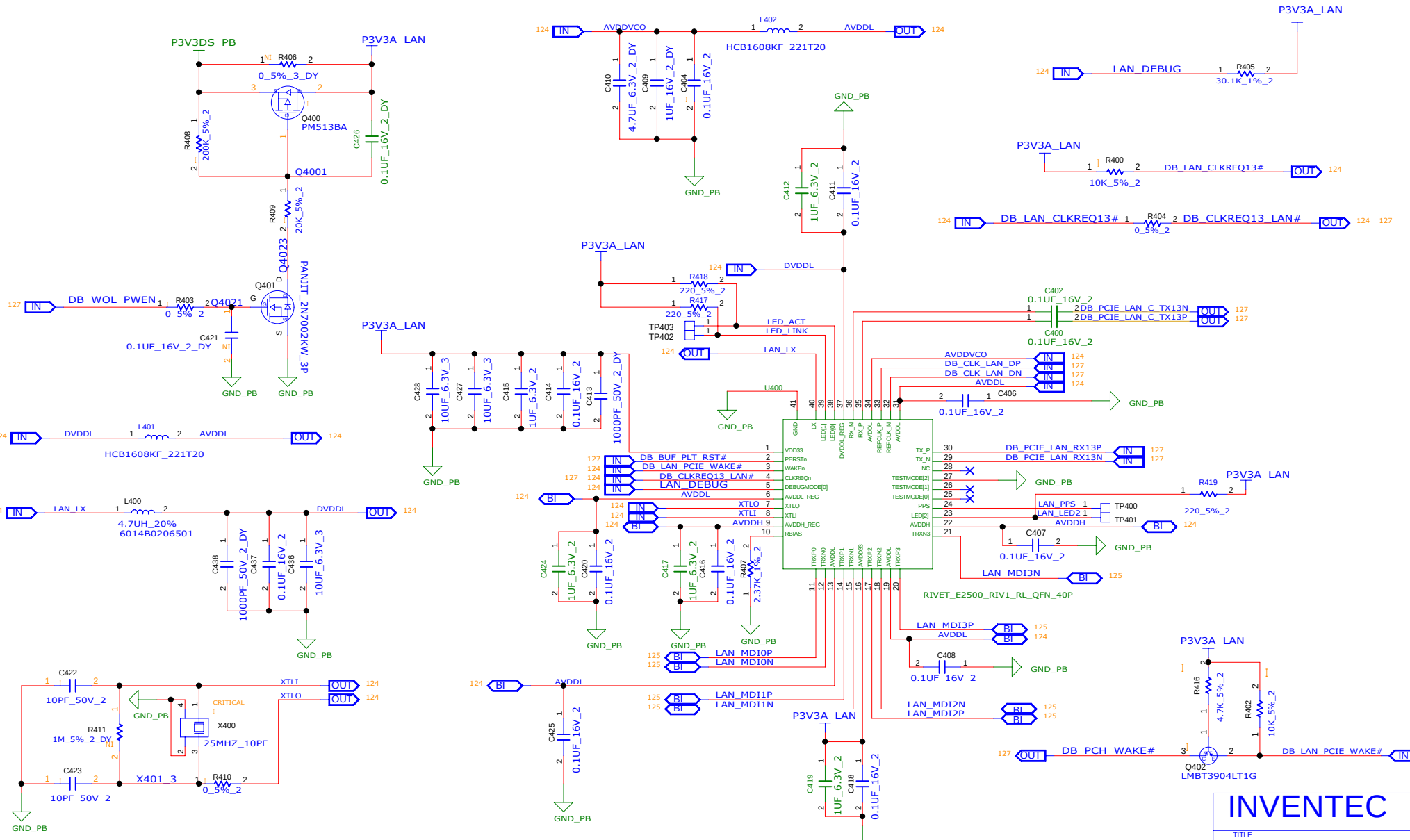

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION USB/DP DE-MUX		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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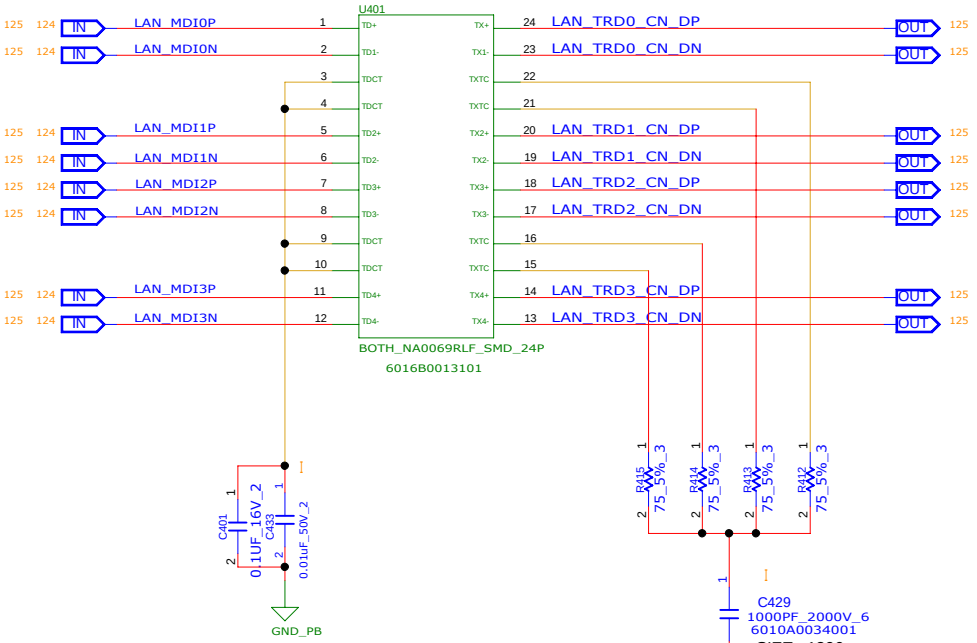
TRANSFORMER



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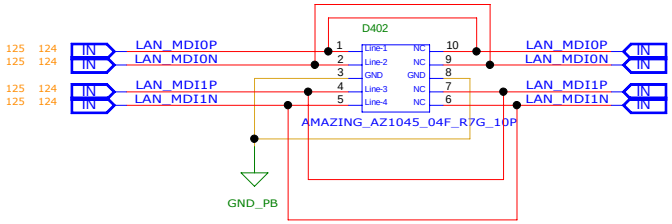

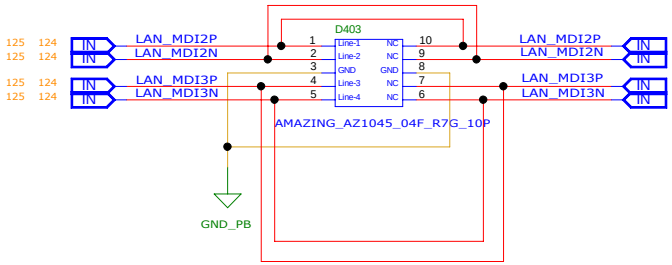

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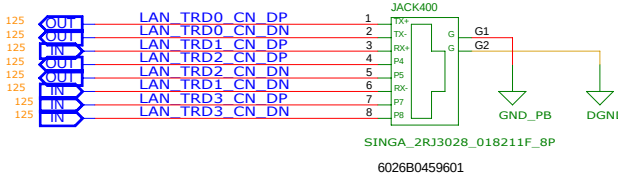

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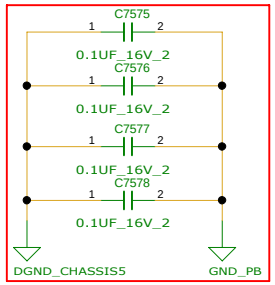

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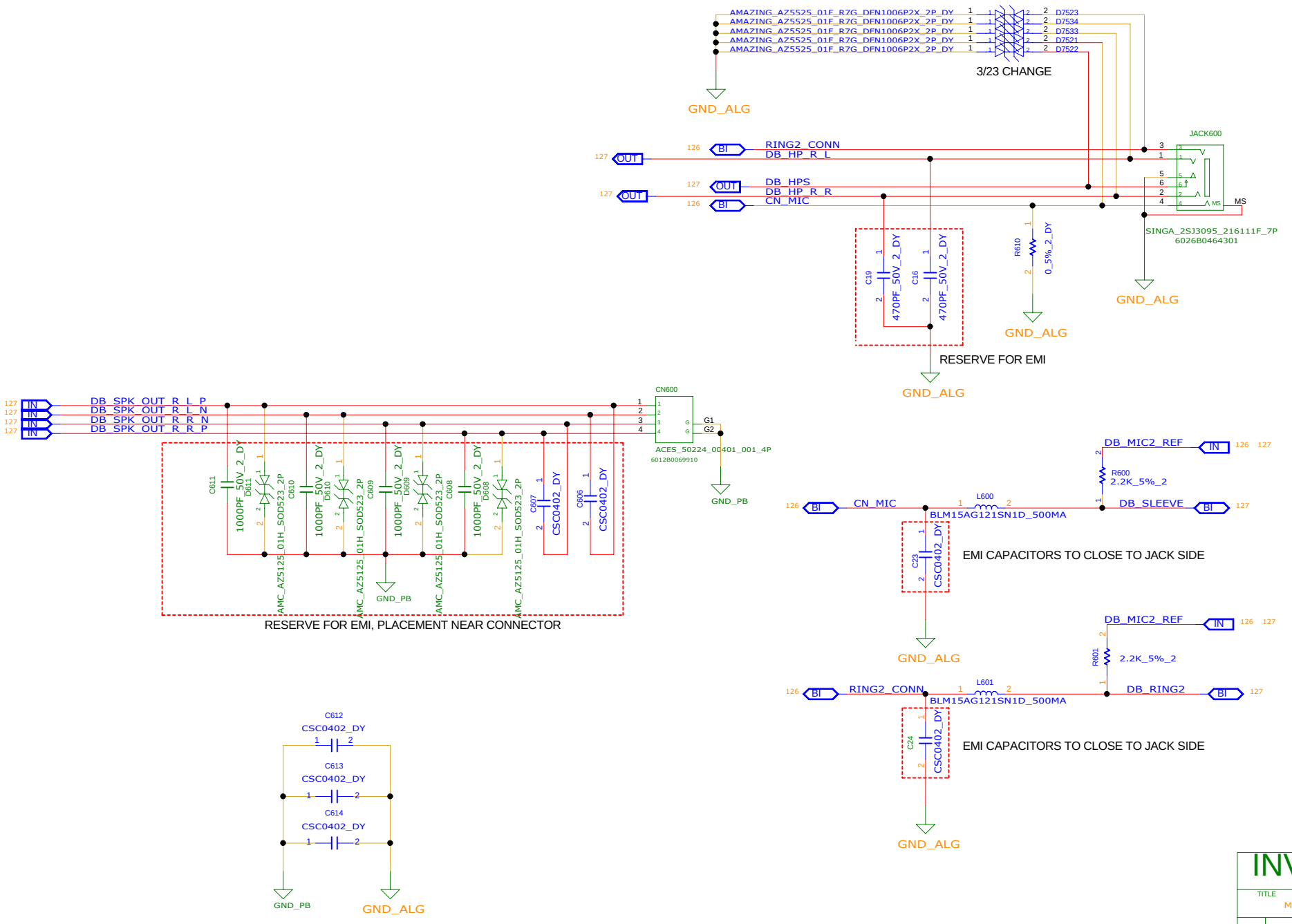

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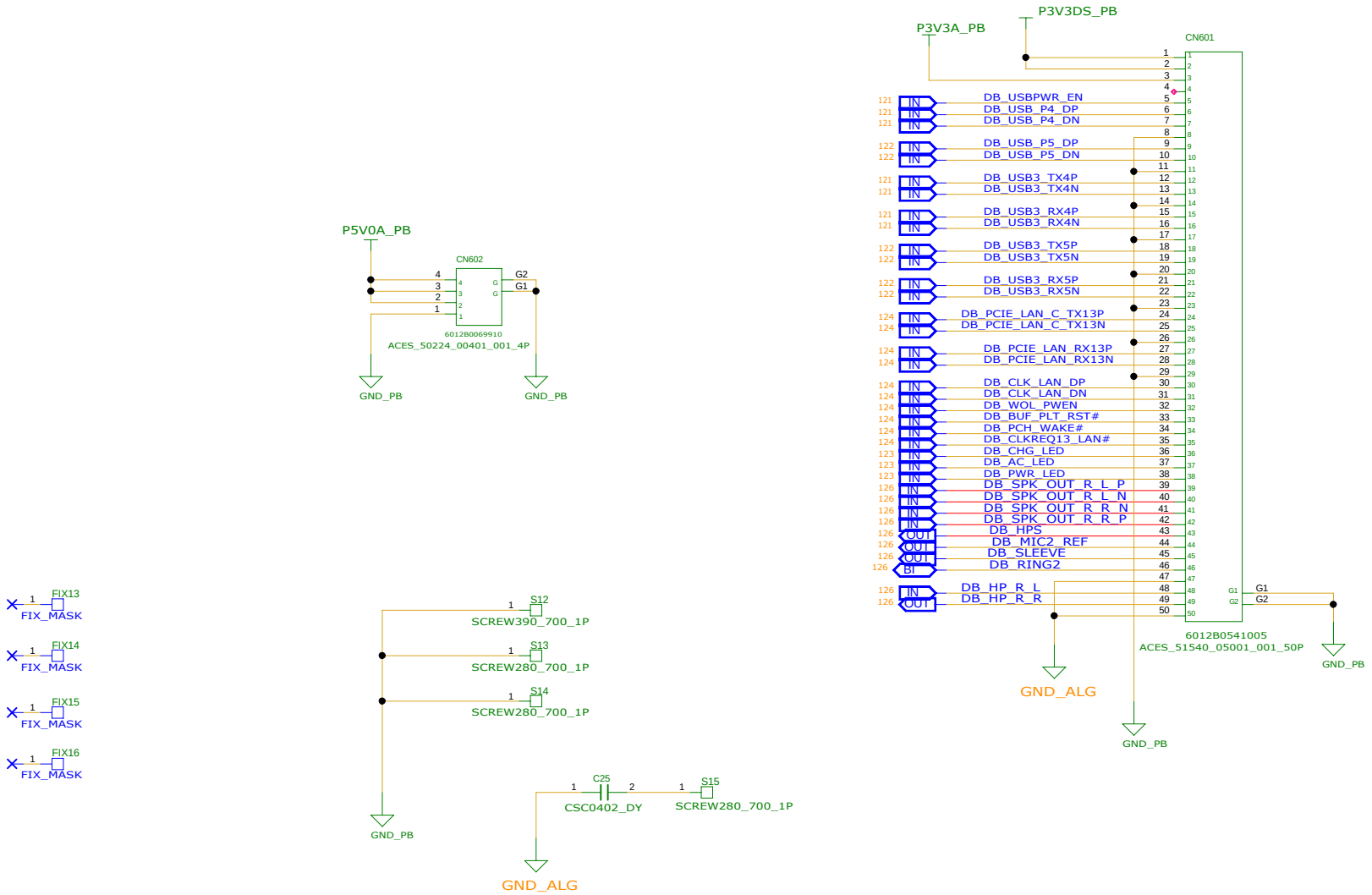

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FOR 17 SMALL BOARD

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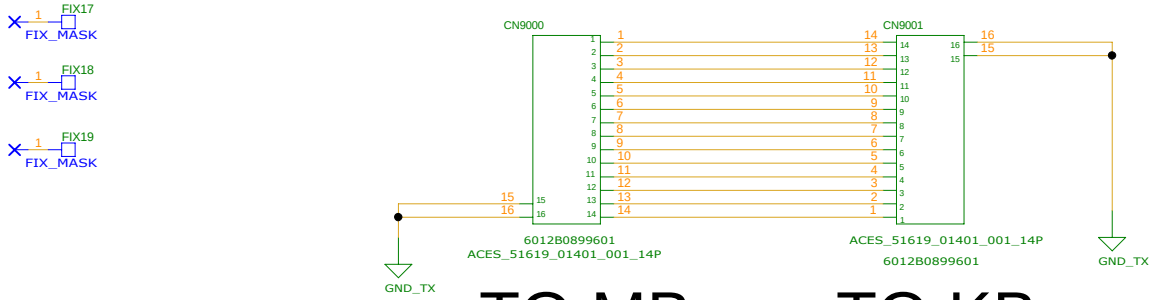

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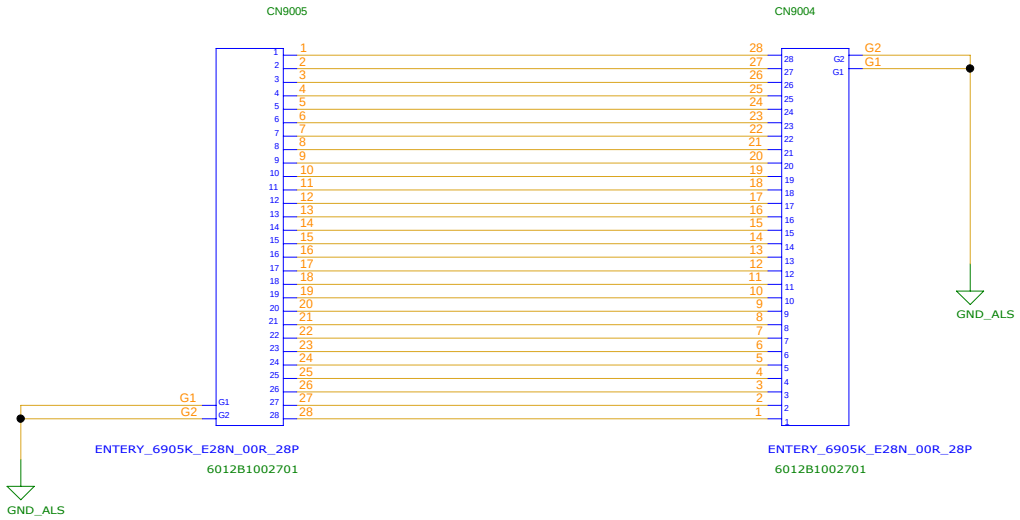

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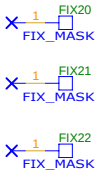

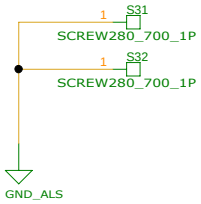

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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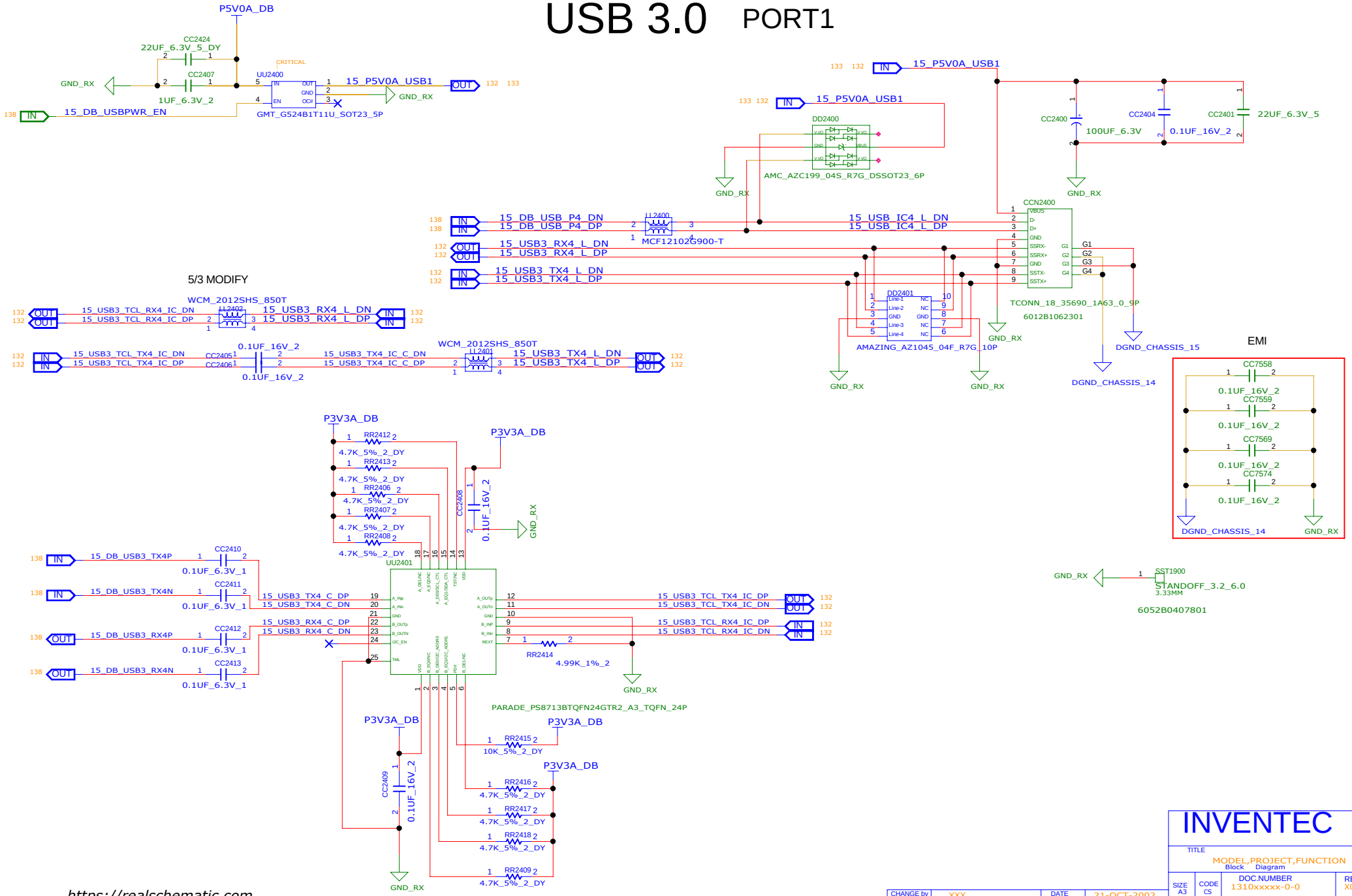
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



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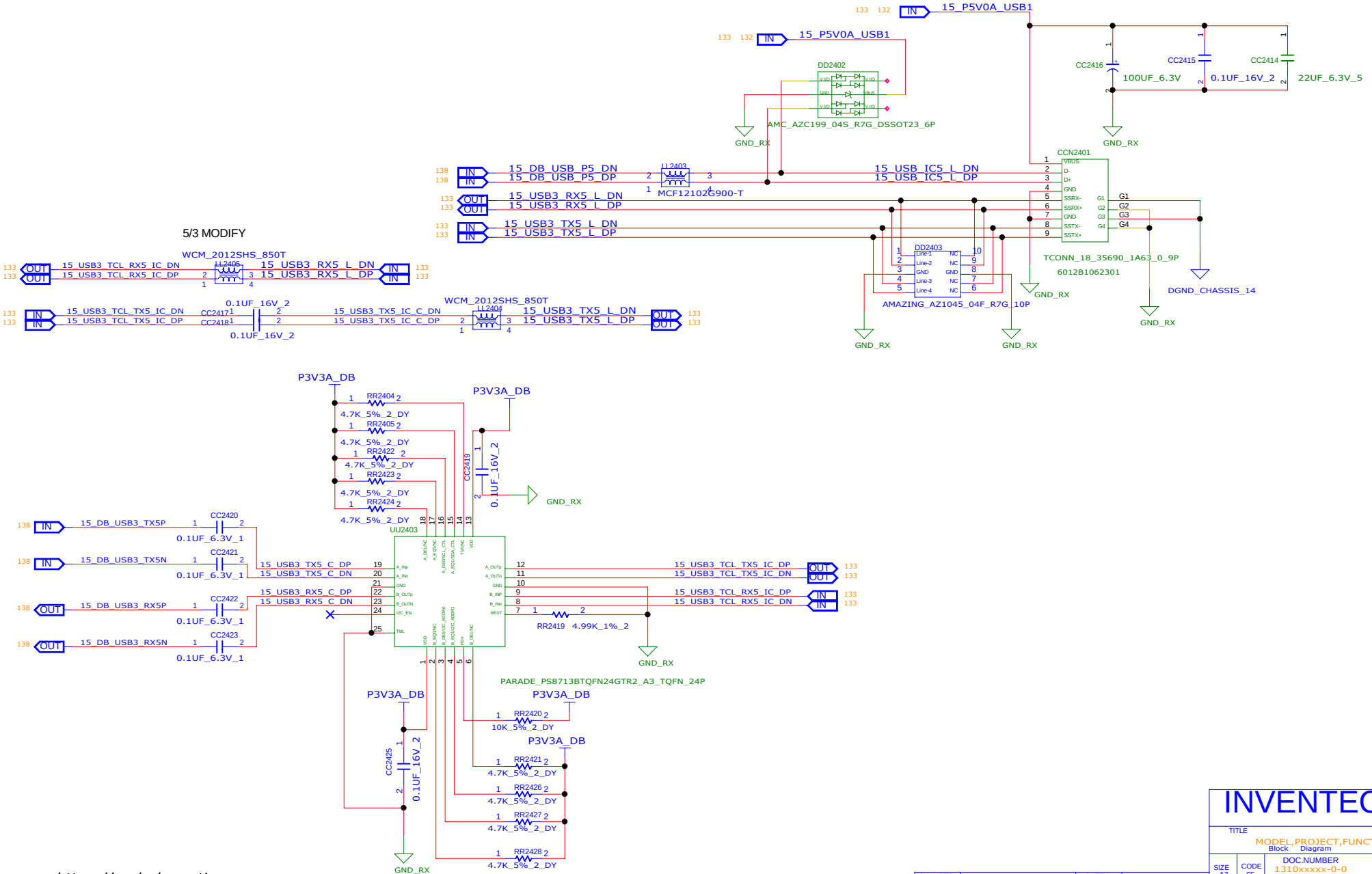
REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



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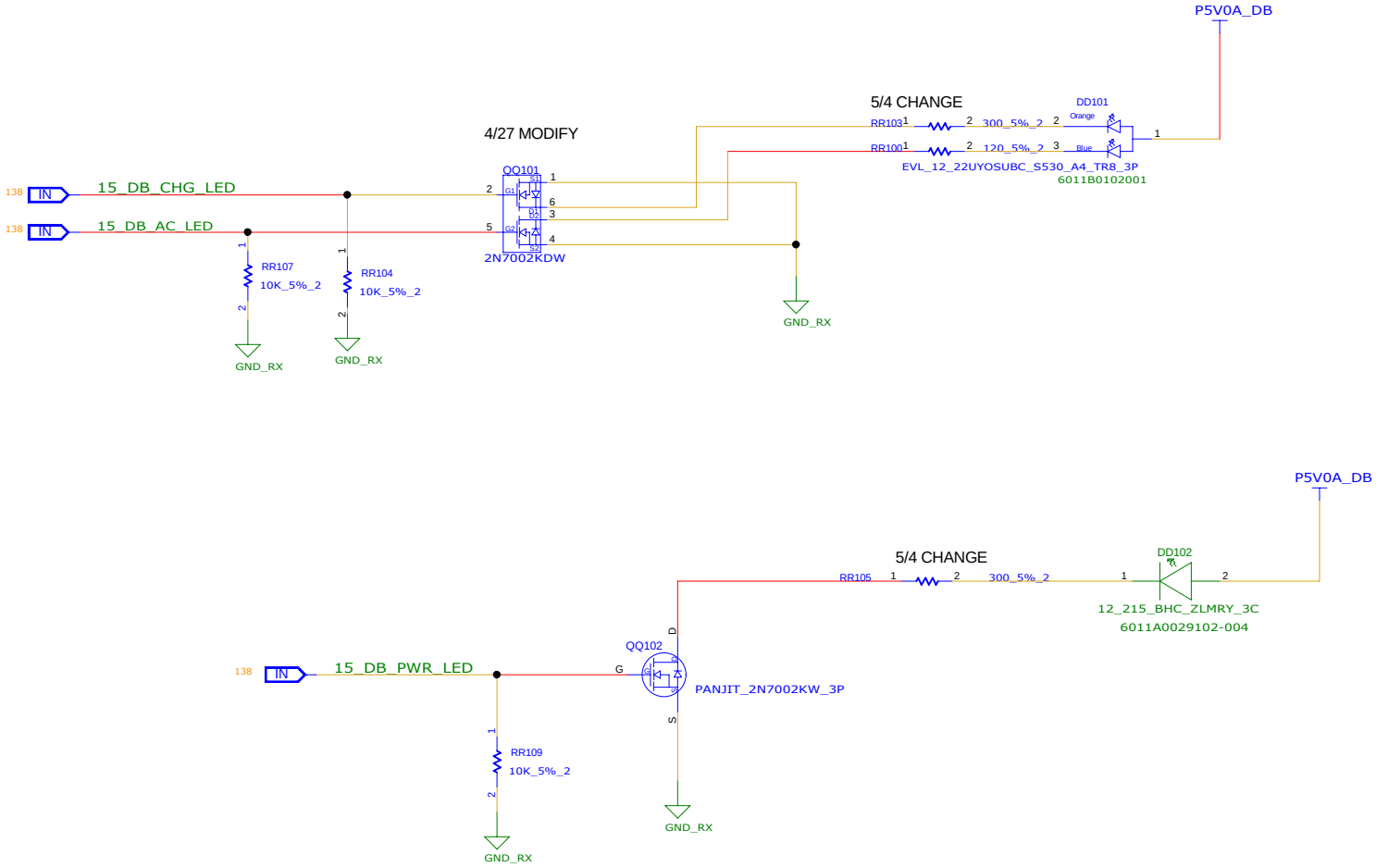

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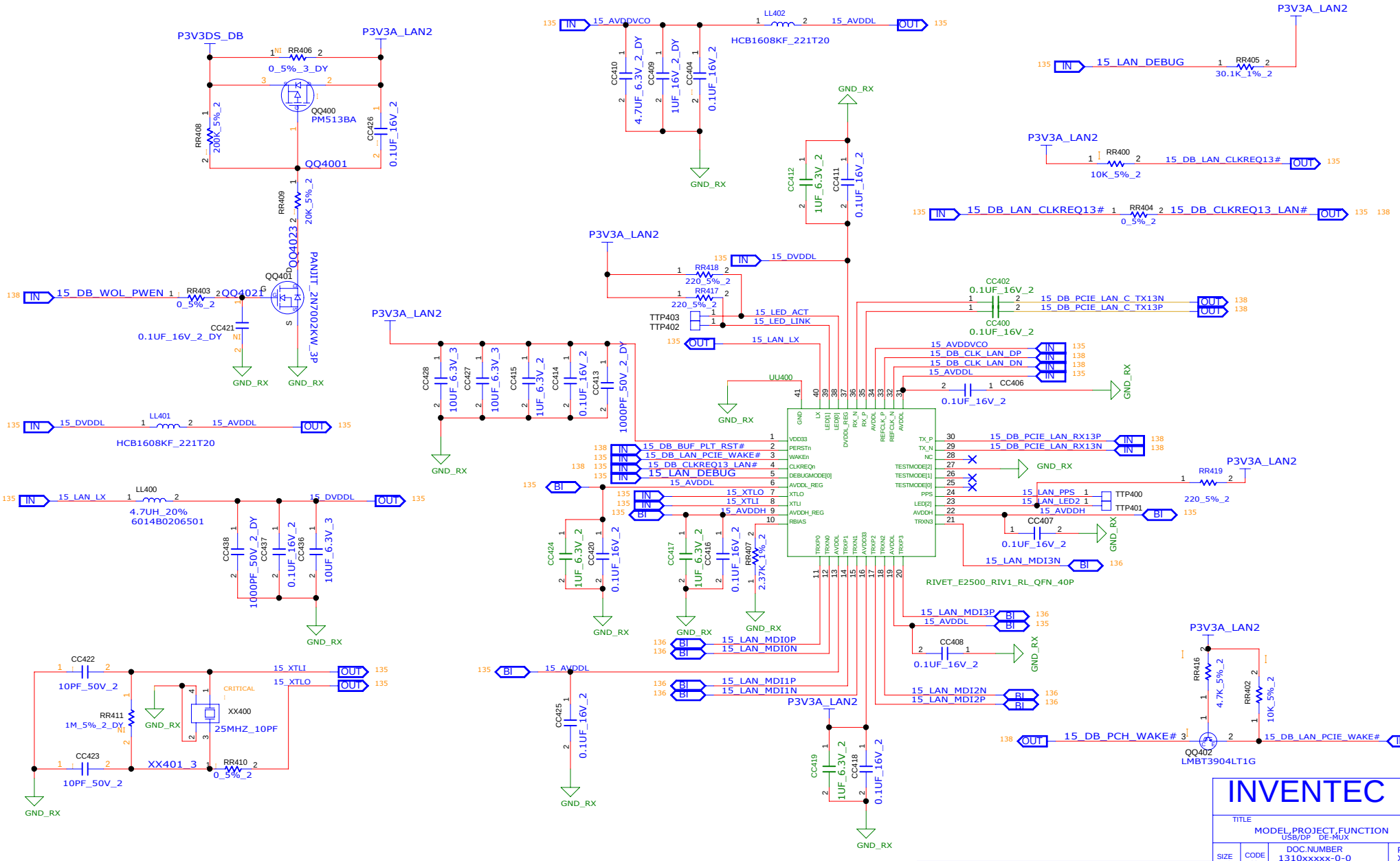
LAN (CONTROLLER)
E2500



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION USB/DP DE-MUX		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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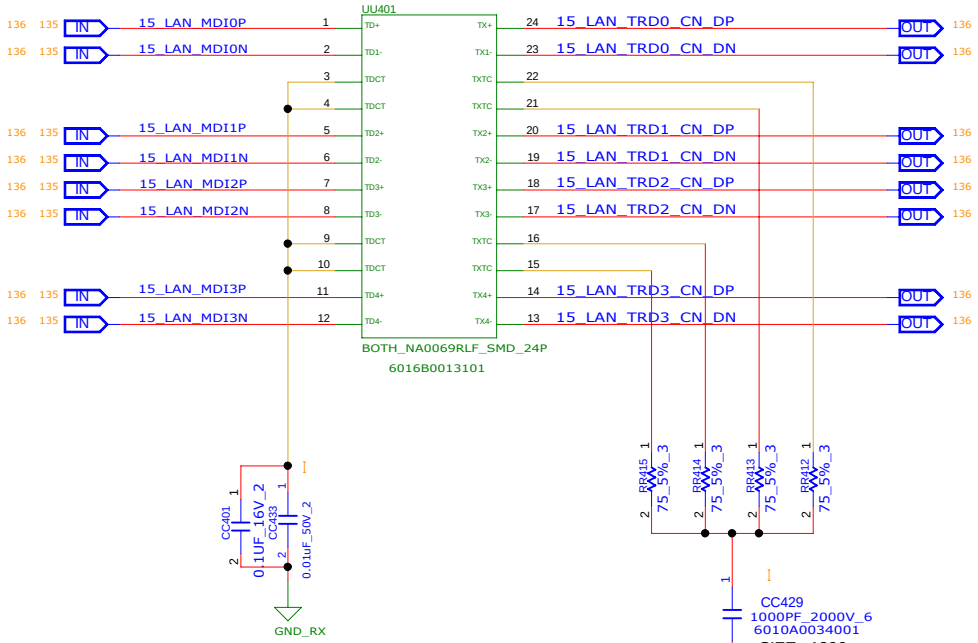
TRANSFORMER



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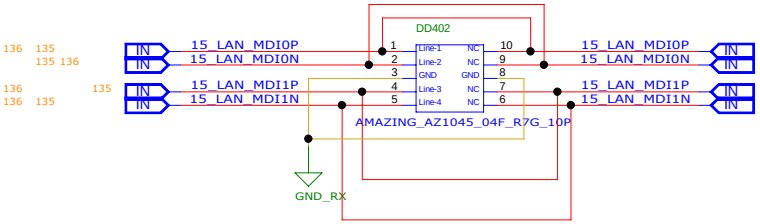
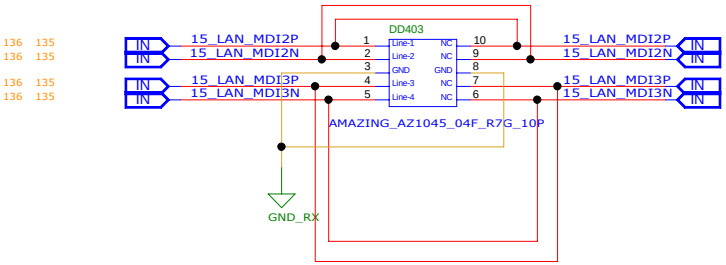
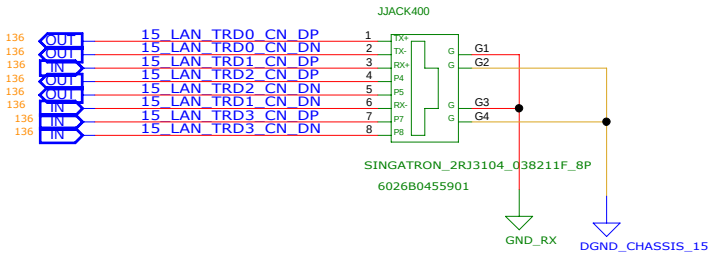
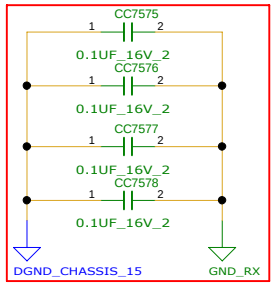




RJ-45



EMI



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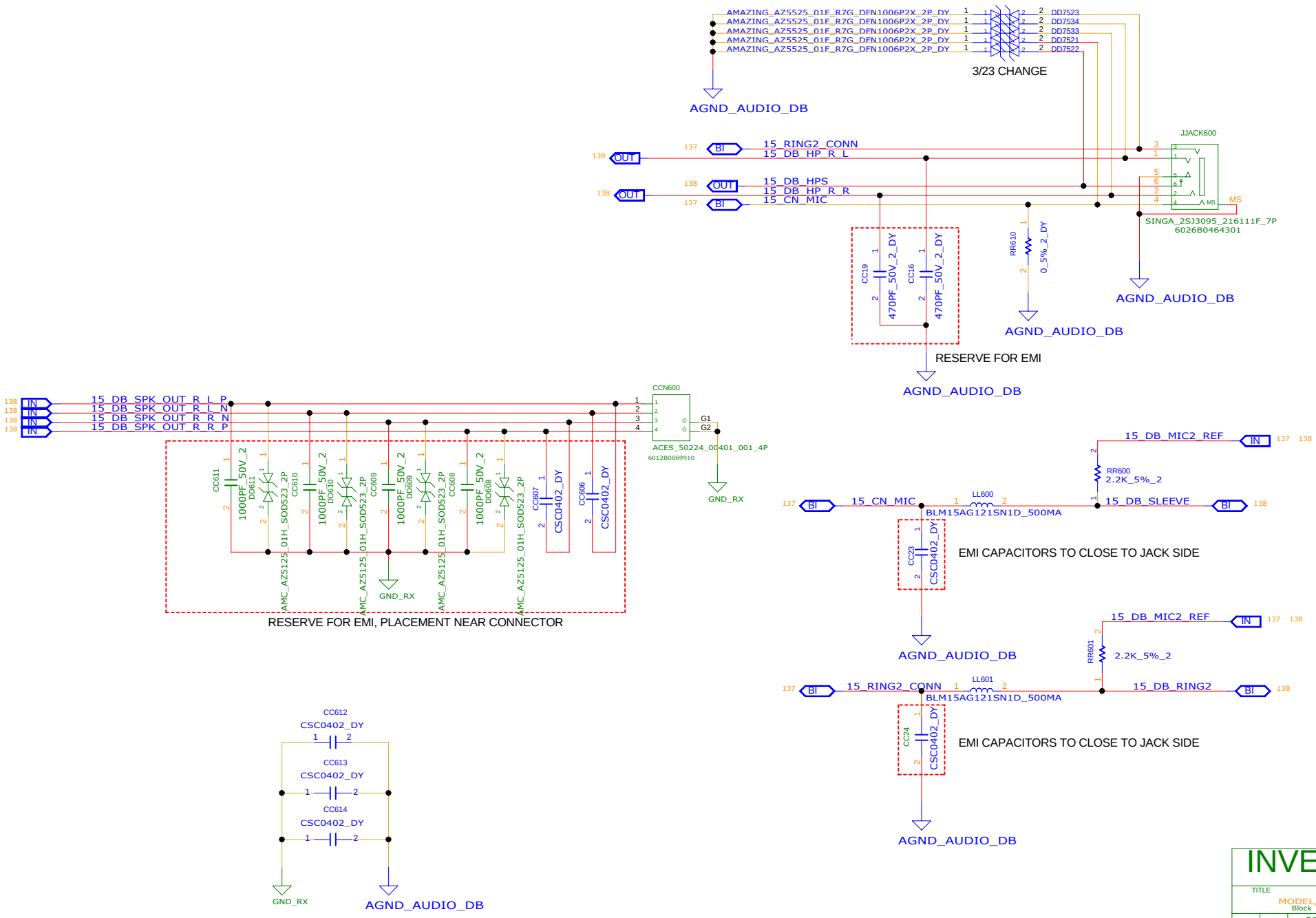

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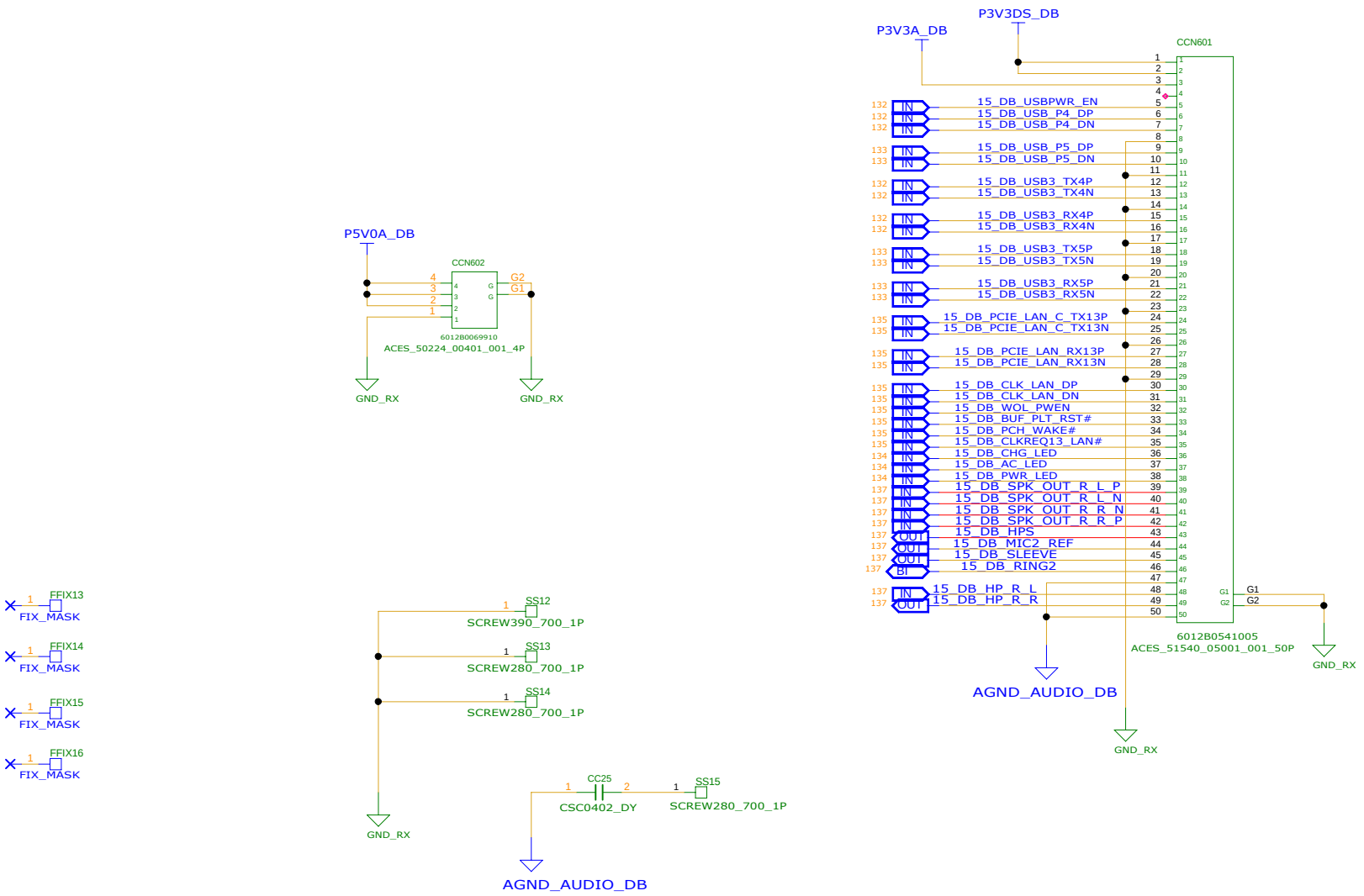

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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8 7 6 5 4 3 2 1

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