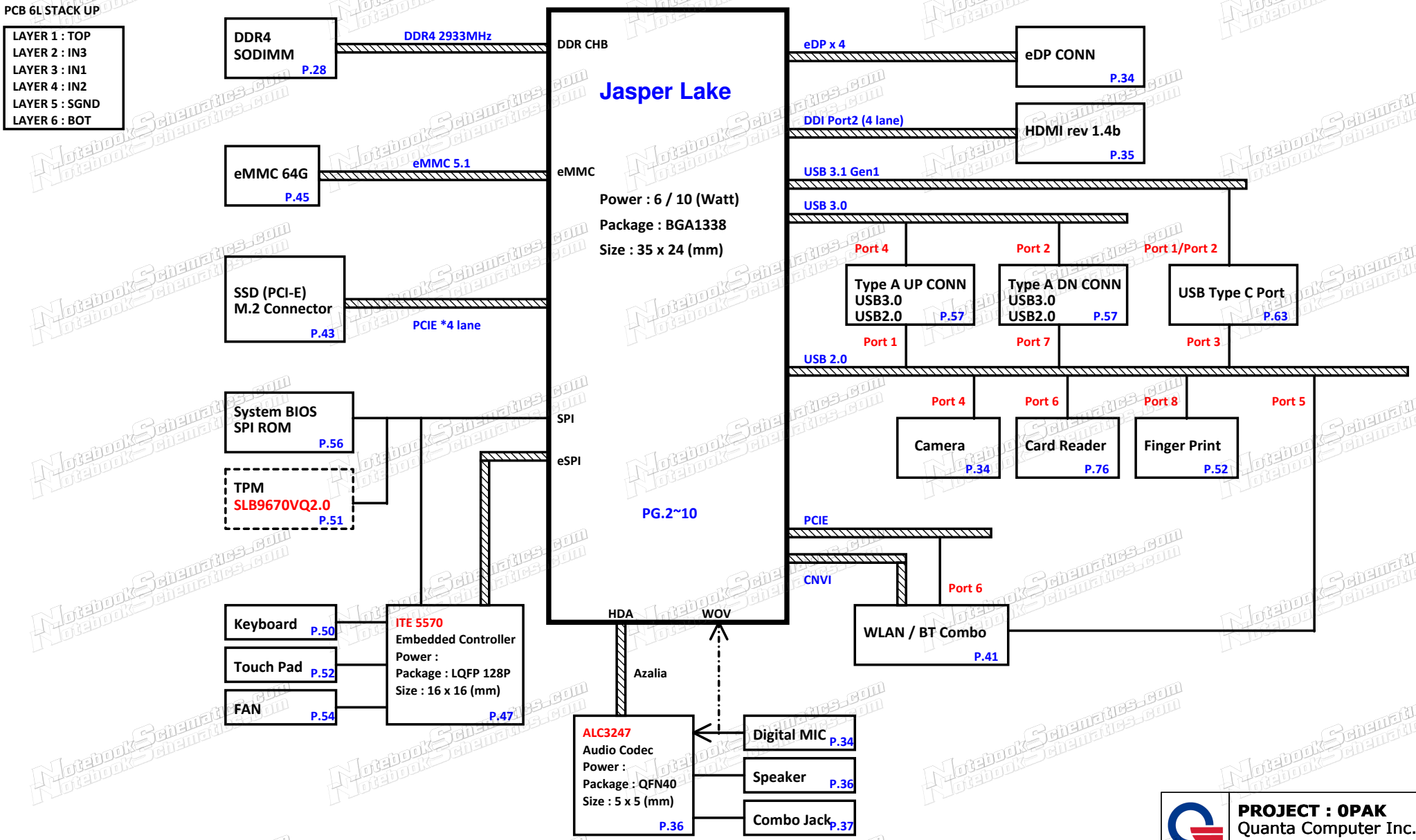
# 0PAK Intel Jasper Lake Platform Block Diagram

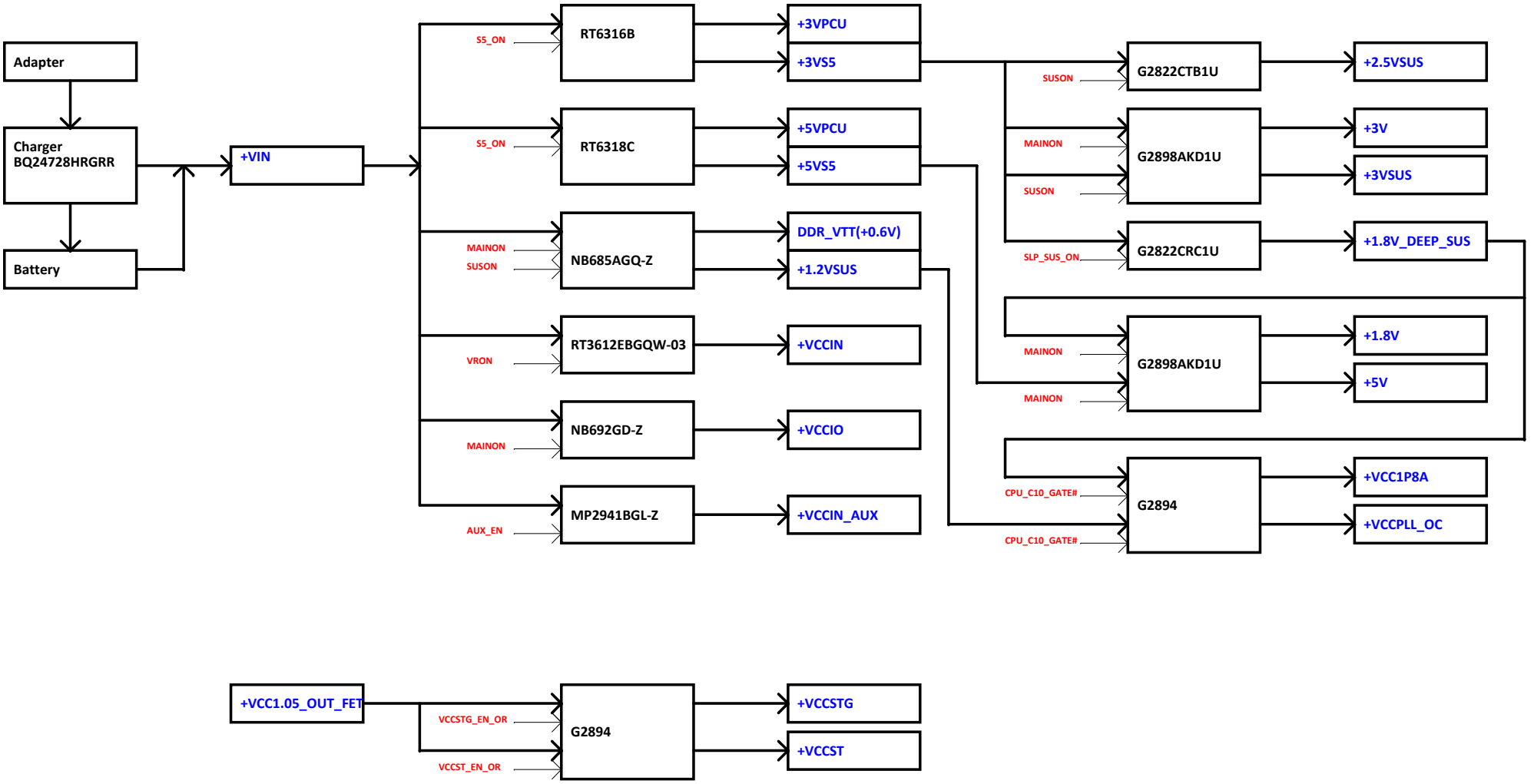



PROJECT : 0PAK
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Intel Block Diagram | 1A |

Date: Wednesday, January 27, 2021 Sheet 1 of 91

# Power Diagram



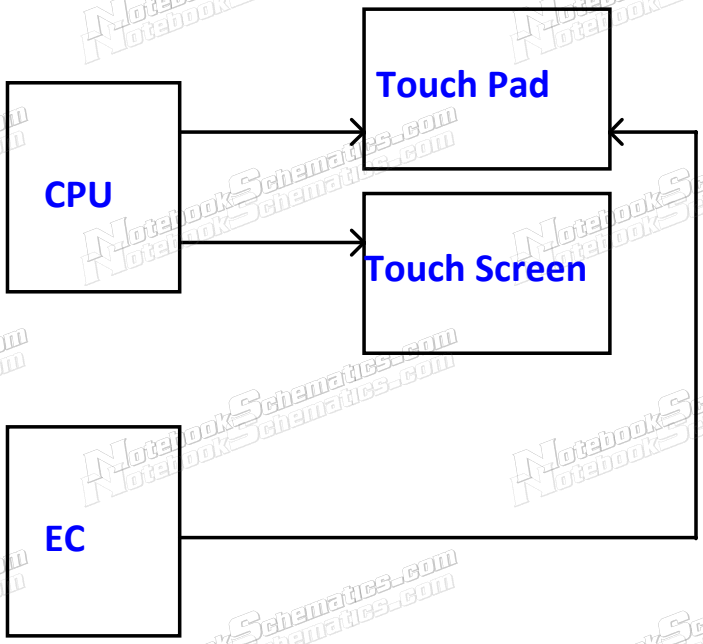

BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Power Diagram (JSL) | 1A |

Date: Wednesday, January 27, 2021 Sheet 2 of 91

# I2C Path






BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | I2C Path (JSL) | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 3 of 91 | |

# Jasper Lake (Memory 2 Channel )
# Only Supoort DDR4 and LPDDR4

04

<28> M_B_DQ[63:0]
<28> M_B_DQSN[7:0]
<28> M_B_DQSP[7:0]
+1.2VSUS <9,28,78,83,88>

U1B

T47 LP4X_1_DQ31/DDR_0_DQ63
T48 LP4X_1_DQ30/DDR_0_DQ62
U49 LP4X_1_DQ29/DDR_0_DQ61
W47 LP4X_1_DQ28/DDR_0_DQ60
U51 LP4X_1_DQ27/DDR_0_DQ59
W51 LP4X_1_DQ26/DDR_0_DQ58
Y48 LP4X_1_DQ25/DDR_0_DQ57
W49 LP4X_1_DQ24/DDR_0_DQ56
V39 LP4X_1_DQ23/DDR_0_DQ55
V41 LP4X_1_DQ22/DDR_0_DQ54
V44 LP4X_1_DQ21/DDR_0_DQ53
T45 LP4X_1_DQ20/DDR_0_DQ52
V45 LP4X_1_DQ19/DDR_0_DQ51
T39 LP4X_1_DQ18/DDR_0_DQ50
T44 LP4X_1_DQ17/DDR_0_DQ49
T41 LP4X_1_DQ16/DDR_0_DQ48
K50 LP4X_1_DQ15/DDR_0_DQ47
L48 LP4X_1_DQ14/DDR_0_DQ46
K49 LP4X_1_DQ13/DDR_0_DQ45
N47 LP4X_1_DQ12/DDR_0_DQ44
L51 LP4X_1_DQ11/DDR_0_DQ43
P51 LP4X_1_DQ10/DDR_0_DQ42
P48 LP4X_1_DQ09/DDR_0_DQ41
P49 LP4X_1_DQ08/DDR_0_DQ40
M45 LP4X_1_DQ07/DDR_0_DQ39
M44 LP4X_1_DQ06/DDR_0_DQ38
M41 LP4X_1_DQ05/DDR_0_DQ37
K45 LP4X_1_DQ04/DDR_0_DQ36
M39 LP4X_1_DQ03/DDR_0_DQ35
K39 LP4X_1_DQ02/DDR_0_DQ34
K44 LP4X_1_DQ01/DDR_0_DQ33
K41 LP4X_1_DQ00/DDR_0_DQ32
F30 LP4X_0_DQ31/DDR_0_DQ31
E30 LP4X_0_DQ30/DDR_0_DQ30
D31 LP4X_0_DQ29/DDR_0_DQ29
B33 LP4X_0_DQ28/DDR_0_DQ28
B30 LP4X_0_DQ27/DDR_0_DQ27
F33 LP4X_0_DQ26/DDR_0_DQ26
D33 LP4X_0_DQ25/DDR_0_DQ25
E33 LP4X_0_DQ24/DDR_0_DQ24
M36 LP4X_0_DQ23/DDR_0_DQ23
P36 LP4X_0_DQ22/DDR_0_DQ22
J36 LP4X_0_DQ21/DDR_0_DQ21
H34 LP4X_0_DQ20/DDR_0_DQ20
H36 LP4X_0_DQ19/DDR_0_DQ19
P34 LP4X_0_DQ18/DDR_0_DQ18
J34 LP4X_0_DQ17/DDR_0_DQ17
M34 LP4X_0_DQ16/DDR_0_DQ16
F25 LP4X_0_DQ15/DDR_0_DQ15
E25 LP4X_0_DQ14/DDR_0_DQ14
D25 LP4X_0_DQ13/DDR_0_DQ13
B28 LP4X_0_DQ12/DDR_0_DQ12
B25 LP4X_0_DQ11/DDR_0_DQ11
F27 LP4X_0_DQ10/DDR_0_DQ10
D28 LP4X_0_DQ09/DDR_0_DQ09
E28 LP4X_0_DQ08/DDR_0_DQ08
P30 LP4X_0_DQ07/DDR_0_DQ07
M30 LP4X_0_DQ06/DDR_0_DQ06
J30 LP4X_0_DQ05/DDR_0_DQ05
H28 LP4X_0_DQ04/DDR_0_DQ04
H30 LP4X_0_DQ03/DDR_0_DQ03
P28 LP4X_0_DQ02/DDR_0_DQ02
J28 LP4X_0_DQ01/DDR_0_DQ01
M28 LP4X_0_DQ00/DDR_0_DQ00

LP4X_1_CLK_DN/DDR_0_CLK1_DN D49
LP4X_1_CLK_DP/DDR_0_CLK1_DP E48
LP4X_0_CLK_DN/DDR_0_CLK0_DN F45
LP4X_0_CLK_DP/DDR_0_CLK0_DP E46
LP4X_0_CKE1 B41
LP4X_0_CKE0/DDR_0_CKE0 F41
LP4X_1_CKE1/DDR_0_CKE1 D42
LP4X_1_CKE0 Q48
LP4X_1_CS1/DDR_0_CS1_N F52
LP4X_1_CS0 Q50
LP4X_0_CS1 H50
LP4X_0_CS0/DDR_0_CS0_N D45
DDR_0_BA1 E50
LP4X_1_CA4/DDR_0_BA0 B44
DDR_0_BG1 D36
LP4X_0_CA5/DDR_0_BG0 F38
LP4X_1_CA3/DDR_0_MA16_RAS_N A45
LP4X_1_CA1/DDR_0_MA15_CAS_N F49
LP4X_1_CA2/DDR_0_MA14_WE_N C46
LP4X_1_CA0/DDR_0_MA13 J48
DDR_0_MA12 B36
DDR_0_MA11 C37
DDR_0_MA10 A47
LP4X_0_CA1/DDR_0_MA09 E39
LP4X_0_CA3/DDR_0_MA08 D38
LP4X_0_CA4/DDR_0_MA07 B39
LP4X_0_CA2/DDR_0_MA06 D37
LP4X_0_CA0/DDR_0_MA05 E35
DDR_0_MA04 C43
DDR_0_MA03 E41
LP4X_1_CA5/DDR_0_MA02 C44
DDR_0_MA01 E43
DDR_0_MA00 C45
DDR_0_ODT1 D47
DDR_0_ODT0 Q49
LP4X_1_DQS3_DP/DDR_0_DQS7_DP V48
LP4X_1_DQS3_DN/DDR_0_DQS7_DN V50
LP4X_1_DQS2_DP/DDR_0_DQS6_DP T42
LP4X_1_DQS2_DN/DDR_0_DQS6_DN V42
LP4X_1_DQS1_DP/DDR_0_DQS5_DP N48
LP4X_1_DQS1_DN/DDR_0_DQS5_DN M50
LP4X_1_DQS0_DP/DDR_0_DQS4_DP K42
LP4X_1_DQS0_DN/DDR_0_DQS4_DN M42
LP4X_0_DQS3_DP/DDR_0_DQS3_DP C32
LP4X_0_DQS3_DN/DDR_0_DQS3_DN D32
LP4X_0_DQS2_DP/DDR_0_DQS2_DP L36
LP4X_0_DQS2_DN/DDR_0_DQS2_DN L34
LP4X_0_DQS1_DP/DDR_0_DQS1_DP C26
LP4X_0_DQS1_DN/DDR_0_DQS1_DN D26
LP4X_0_DQS0_DP/DDR_0_DQS0_DP L30
LP4X_0_DQS0_DN/DDR_0_DQS0_DN L28
JSL New DDR_0_PAR G42
DDR_0_ACT_N F36
JSL New DDR_0_ALERT_N D41
DDR0_VREF_DQ BV45 M1_VREF_DQ
DDR_1_VREF_CA BV42 SMDDR_VREF_DQ1_M3_R
DDR_0_VREF_CA BV44
DDR_VTT_CTL BB41
JSL New RSVD_TP_28 A51
JSL New RSVD_TP_29 B52
PMC_DRAM_RESET_N BV41 M_DRAMRST#

R3204 100_1%_2 MEM_2_RCOMP C48
R3205 100_1%_2 MEM_1_RCOMP D50
R3206 100_1%_2 MEM_0_RCOMP C49
DDR_RCOMP2 JSL New
DDR_RCOMP1
DDR_RCOMP0

Trace length < 500 mils
Trace width = 15 mils
Trace spacing = 20 mils

*JSL_REV2_IP_EXT

TP3200
R3201 *0_4/S
SMDDR_VREF_DQ1_M3 <28>
PV2-change

U1C

M_B_DQ63 BJ47
M_B_DQ62 BH48
M_B_DQ61 BJ49
M_B_DQ60 BM51
M_B_DQ59 BJ51
M_B_DQ58 BL47
M_B_DQ57 BL49
M_B_DQ56 BM48
M_B_DQ55 BP39
M_B_DQ54 BP41
M_B_DQ53 BP44
M_B_DQ52 BM45
M_B_DQ51 BP45
M_B_DQ50 BM39
M_B_DQ49 BM44
M_B_DQ48 BM41
M_B_DQ47 BC47
M_B_DQ46 BC48
M_B_DQ45 BD49
M_B_DQ44 BF51
M_B_DQ43 BC51
M_B_DQ42 BF47
M_B_DQ41 BF49
M_B_DQ40 BF48
M_B_DQ39 BH39
M_B_DQ38 BH41
M_B_DQ37 BH44
M_B_DQ36 BF45
M_B_DQ35 BH45
M_B_DQ34 BF39
M_B_DQ33 BF44
M_B_DQ32 BF41
M_B_DQ31 AG47
M_B_DQ30 AG48
M_B_DQ29 AH49
M_B_DQ28 AK47
M_B_DQ27 AG51
M_B_DQ26 AK51
M_B_DQ25 AK48
M_B_DQ24 AK49
M_B_DQ23 AK41
M_B_DQ22 AK39
M_B_DQ21 AK44
M_B_DQ20 AH44
M_B_DQ19 AK45
M_B_DQ18 AH41
M_B_DQ17 AH45
M_B_DQ16 AH39
M_B_DQ15 AB47
M_B_DQ14 AB48
M_B_DQ13 AB49
M_B_DQ12 AD47
M_B_DQ11 AB51
M_B_DQ10 AE51
M_B_DQ9 AE48
M_B_DQ8 AE49
M_B_DQ7 AD39
M_B_DQ6 AD41
M_B_DQ5 AD44
M_B_DQ4 AB45
M_B_DQ3 AD45
M_B_DQ2 AB44
M_B_DQ1 AB39
M_B_DQ0 AB41

LP4X_3_DQ31/DDR_1_DQ63
LP4X_3_DQ30/DDR_1_DQ62
LP4X_3_DQ29/DDR_1_DQ61
LP4X_3_DQ28/DDR_1_DQ60
LP4X_3_DQ27/DDR_1_DQ59
LP4X_3_DQ26/DDR_1_DQ58
LP4X_3_DQ25/DDR_1_DQ57
LP4X_3_DQ24/DDR_1_DQ56
LP4X_3_DQ23/DDR_1_DQ55
LP4X_3_DQ22/DDR_1_DQ54
LP4X_3_DQ21/DDR_1_DQ53
LP4X_3_DQ20/DDR_1_DQ52
LP4X_3_DQ19/DDR_1_DQ51
LP4X_3_DQ18/DDR_1_DQ50
LP4X_3_DQ17/DDR_1_DQ49
LP4X_3_DQ16/DDR_1_DQ48
LP4X_3_DQ15/DDR_1_DQ47
LP4X_3_DQ14/DDR_1_DQ46
LP4X_3_DQ13/DDR_1_DQ45
LP4X_3_DQ12/DDR_1_DQ44
LP4X_3_DQ11/DDR_1_DQ43
LP4X_3_DQ10/DDR_1_DQ42
LP4X_3_DQ09/DDR_1_DQ41
LP4X_3_DQ08/DDR_1_DQ40
LP4X_3_DQ07/DDR_1_DQ39
LP4X_3_DQ06/DDR_1_DQ38
LP4X_3_DQ05/DDR_1_DQ37
LP4X_3_DQ04/DDR_1_DQ36
LP4X_3_DQ03/DDR_1_DQ35
LP4X_3_DQ02/DDR_1_DQ34
LP4X_3_DQ01/DDR_1_DQ33
LP4X_3_DQ00/DDR_1_DQ32
LP4X_2_DQ31/DDR_1_DQ31
LP4X_2_DQ30/DDR_1_DQ30
LP4X_2_DQ29/DDR_1_DQ29
LP4X_2_DQ28/DDR_1_DQ28
LP4X_2_DQ27/DDR_1_DQ27
LP4X_2_DQ26/DDR_1_DQ26
LP4X_2_DQ25/DDR_1_DQ25
LP4X_2_DQ24/DDR_1_DQ24
LP4X_2_DQ23/DDR_1_DQ23
LP4X_2_DQ22/DDR_1_DQ22
LP4X_2_DQ21/DDR_1_DQ21
LP4X_2_DQ20/DDR_1_DQ20
LP4X_2_DQ19/DDR_1_DQ19
LP4X_2_DQ18/DDR_1_DQ18
LP4X_2_DQ17/DDR_1_DQ17
LP4X_2_DQ16/DDR_1_DQ16
LP4X_2_DQ15/DDR_1_DQ15
LP4X_2_DQ14/DDR_1_DQ14
LP4X_2_DQ13/DDR_1_DQ13
LP4X_2_DQ12/DDR_1_DQ12
LP4X_2_DQ11/DDR_1_DQ11
LP4X_2_DQ10/DDR_1_DQ10
LP4X_2_DQ09/DDR_1_DQ09
LP4X_2_DQ08/DDR_1_DQ08
LP4X_2_DQ07/DDR_1_DQ07
LP4X_2_DQ06/DDR_1_DQ06
LP4X_2_DQ05/DDR_1_DQ05
LP4X_2_DQ04/DDR_1_DQ04
LP4X_2_DQ03/DDR_1_DQ03
LP4X_2_DQ02/DDR_1_DQ02
LP4X_2_DQ01/DDR_1_DQ01
LP4X_2_DQ00/DDR_1_DQ00

JSL New LP4X_3_CLK_DN/DDR_1_CLK1_DN AV51
JSL New LP4X_3_CLK_DP/DDR_1_CLK1_DP AV49
LP4X_2_CLK_DN/DDR_1_CLK0_DN AV47
LP4X_2_CLK_DP/DDR_1_CLK0_DP AV48
M_B_CLKN1 <28>
M_B_CLKP1 <28>
M_B_CLKN0 <28>
M_B_CLKP0 <28>

AY41
JSL New LP4X_2_CKE1 AY42
LP4X_2_CKE0/DDR_1_CKE0 AY45
JSL New LP4X_3_CKE1/DDR_1_CKE1 BB44
JSL New LP4X_3_CKE0
M_B_CKE0 <28>
M_B_CKE1 <28>

AY50
JSL New LP4X_2_CS1 AW48
LP4X_2_CS0/DDR_1_CS0_N BA51
JSL New LP4X_3_CS1/DDR_1_CS1_N AY47
JSL New LP4X_3_CS0
M_B_CS#0 <28>
M_B_CS#1 <28>

LP4X_3_CA0/DDR_1_MA13 AT51 M_B_A13
LP4X_3_CA4/DDR_1_BA0 AN51
M_B_A13 <28>
M_B_BA#0 <28>

DDR_1_BG1 AP44
LP4X_2_CA5/DDR_1_BG0 AT45
M_B_BG#1 <28>
M_B_BG#0 <28>

LP4X_3_CA3/DDR_1_MA16_RAS_N AR49 M_B_A16
LP4X_3_CA1/DDR_1_MA15_CAS_N BA49 M_B_A15
LP4X_3_CA2/DDR_1_MA14_WE_N AP50 M_B_A14
DDR_1_BA1 AN47
M_B_A16 <28>
M_B_A15 <28>
M_B_A14 <28>
M_B_BA#1 <28>

DDR_1_MA12 AP45 M_B_A12
DDR_1_MA11 AP42 M_B_A11
DDR_1_MA10 AT48 M_B_A10
LP4X_2_CA1/DDR_1_MA09 AT42 M_B_A9
LP4X_2_CA3/DDR_1_MA08 AT41 M_B_A8
LP4X_2_CA4/DDR_1_MA07 AT39 M_B_A7
LP4X_2_CA2/DDR_1_MA06 AT44 M_B_A6
LP4X_2_CA0/DDR_1_MA05 AP41 M_B_A5
DDR_1_MA04 AY44 M_B_A4
DDR_1_MA03 BB42 M_B_A3
LP4X_3_CA5/DDR_1_MA02 AR47 M_B_A2
DDR_1_MA01 AN49 M_B_A1
DDR_1_MA00 AP48 M_B_A0
M_B_A12 <28>
M_B_A11 <28>
M_B_A10 <28>
M_B_A9 <28>
M_B_A8 <28>
M_B_A7 <28>
M_B_A6 <28>
M_B_A5 <28>
M_B_A4 <28>
M_B_A3 <28>
M_B_A2 <28>
M_B_A1 <28>
M_B_A0 <28>

2019.12.28
JSL PDG P76 5.4 & 5.5
Memory Down
Processor Not connected
DRAMs Data Mask Tied to GND

DDR_1_ODT1 AM48
DDR_1_ODT0 BA48
M_B_ODT1 <28>
M_B_ODT0 <28>

LP4X_3_DQS3_DP/DDR_1_DQS7_DP BK48 M_B_DQSP7
LP4X_3_DQS3_DN/DDR_1_DQS7_DN BK50 M_B_DQSN7
LP4X_3_DQS2_DP/DDR_1_DQS6_DP BP42 M_B_DQSP6
LP4X_3_DQS2_DN/DDR_1_DQS6_DN BM42 M_B_DQSN6
LP4X_3_DQS1_DP/DDR_1_DQS5_DP BE48 M_B_DQSP5
LP4X_3_DQS1_DN/DDR_1_DQS5_DN BE50 M_B_DQSN5
LP4X_3_DQS0_DP/DDR_1_DQS4_DP BF42 M_B_DQSP4
LP4X_3_DQS0_DN/DDR_1_DQS4_DN BH42 M_B_DQSN4
LP4X_2_DQS3_DP/DDR_1_DQS3_DP AJ48 M_B_DQSP3
LP4X_2_DQS3_DN/DDR_1_DQS3_DN AJ50 M_B_DQSN3
LP4X_2_DQS2_DP/DDR_1_DQS2_DP AH42 M_B_DQSP2
LP4X_2_DQS2_DN/DDR_1_DQS2_DN AK42 M_B_DQSN2
LP4X_2_DQS1_DP/DDR_1_DQS1_DP AC48 M_B_DQSP1
LP4X_2_DQS1_DN/DDR_1_DQS1_DN AC50 M_B_DQSN1
LP4X_2_DQS0_DP/DDR_1_DQS0_DP AD42 M_B_DQSP0
LP4X_2_DQS0_DN/DDR_1_DQS0_DN AB42 M_B_DQSN0

DDR_1_PAR BB45 M_B_PARITY
DDR_1_ACT_N AP39 M_B_ACT#
DDR_1_ALERT_N AY39 M_B_ALERT#
M_B_PARITY <28>
M_B_ACT# <28>
M_B_ALERT# <28>

VREF trace must be at least
20 mils wide and space

*JSL_REV2_IP_EXT

Table 10. System Memory Interface Guideline Signals Terminology

| Memory Type | DDR4 SODIMM and Memory Down (Per Channel) | LPDDR4x Memory Down (All Channels) |
|---|---|---|
| **Signal Details** | | |
| Clock (CLK) | DDR_[1:0]_CLK[1:0]_DP<br>DDR_[1:0]_CLK[1:0]_DN | LP4x_[3:0]_CLK_DP,<br>LP4x_[3:0]_CLK_DN |
| Control (CTRL) | DDR_[1:0]_CS[1:0]_N,<br>DDR_[1:0]_ODT[1:0] | LP4x_[3:0]_CS[1:0] |
| Clock Enable (CKE) | DDR_[1:0]_CKE[1:0] | LP4x_[3:0]_CKE[1:0] |
| Command (CMD) | DDR_[1:0]_MA[16:0],<br>DDR_[1:0]_BG[1:0],<br>DDR_[1:0]_BA[1:0],<br>DDR_[1:0]_ACT_N,<br>DDR_[1:0]_PAR | LP4x_[3:0]_CA[5:0] |
| Alert | DDR_[1:0]_ALERT_N | N/A |
| Strobe | DDR_[1:0]_DQS[7:0]_DN,<br>DDR_[1:0]_DQS[7:0]_DP | LP4x_[3:0]_DQS[3:0]_DN,<br>LP4x_[3:0]_DQS[3:0]_DP |
| Data | DDR_[1:0]_DQ[63:0] | LP4x_[3:0]_DQ[31:0] |
| Reset | PMC_DRAM_RESET_N | PMC_DRAM_RESET_N |
| RCOMP | DDR_RCOMP[2:0] | DDR_RCOMP[2:0] |
| Vref | DDR_[1:0]_VREF_CA | NA |
| VTT | DDR_VTT_CTL | NA |

## DRAMRST-Memory

Trace length < 4500 mils, 50 ohm impendence
Trace spacing = 15 mils

+1.2VSUS
JSL:470R
R3211
470_1%_2
CPU
M_DRAMRST#
R3214 *0_2/S
M_DRAM_RST# <28>
PV2-change
C3201
*0.1U/10V_2
NEED CHECK!!!

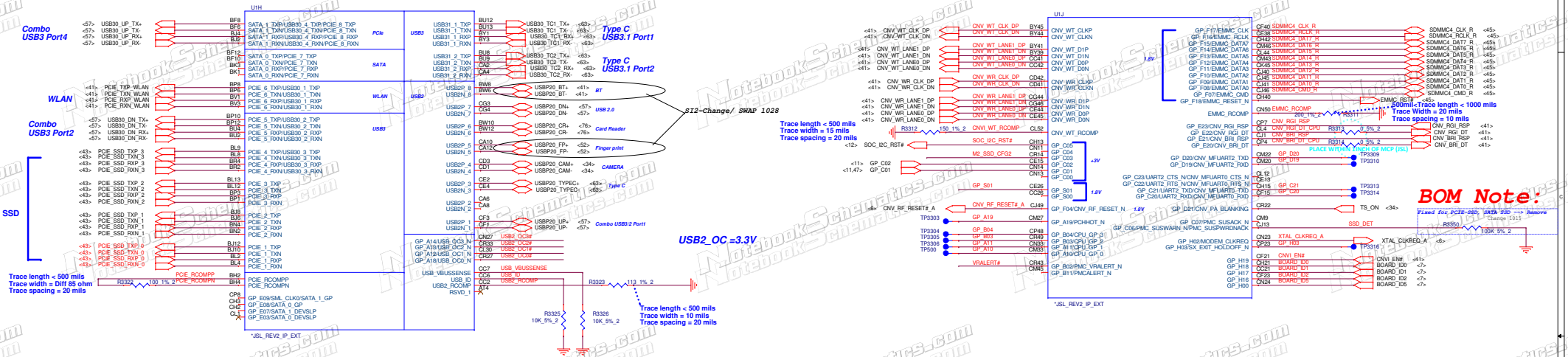
PROJECT : 0PAK
Quanta Computer Inc.
BU5
Size Custom
Document Number JSL (MEMORY)
Rev 1A
Date: Wednesday, January 27, 2021
Sheet 4 of 91

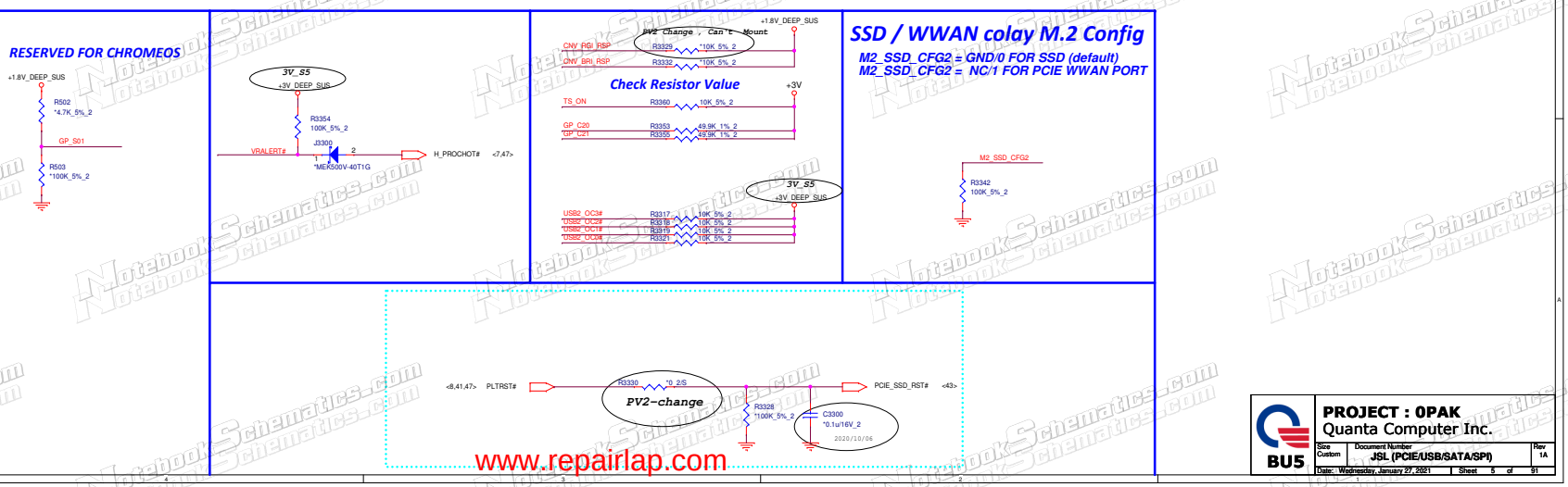
# Jasper Lake (SATA , ODD, CLK ,USB,PCIE,CNVi, GPIO, SMBus)



**PCIE Clock Request:**

*Used for devices that need to request one of the four output clocks.*
*Each clock request maps to the matching clock output (for example, PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]).These signals are multiplexed and may be used by other functions.*



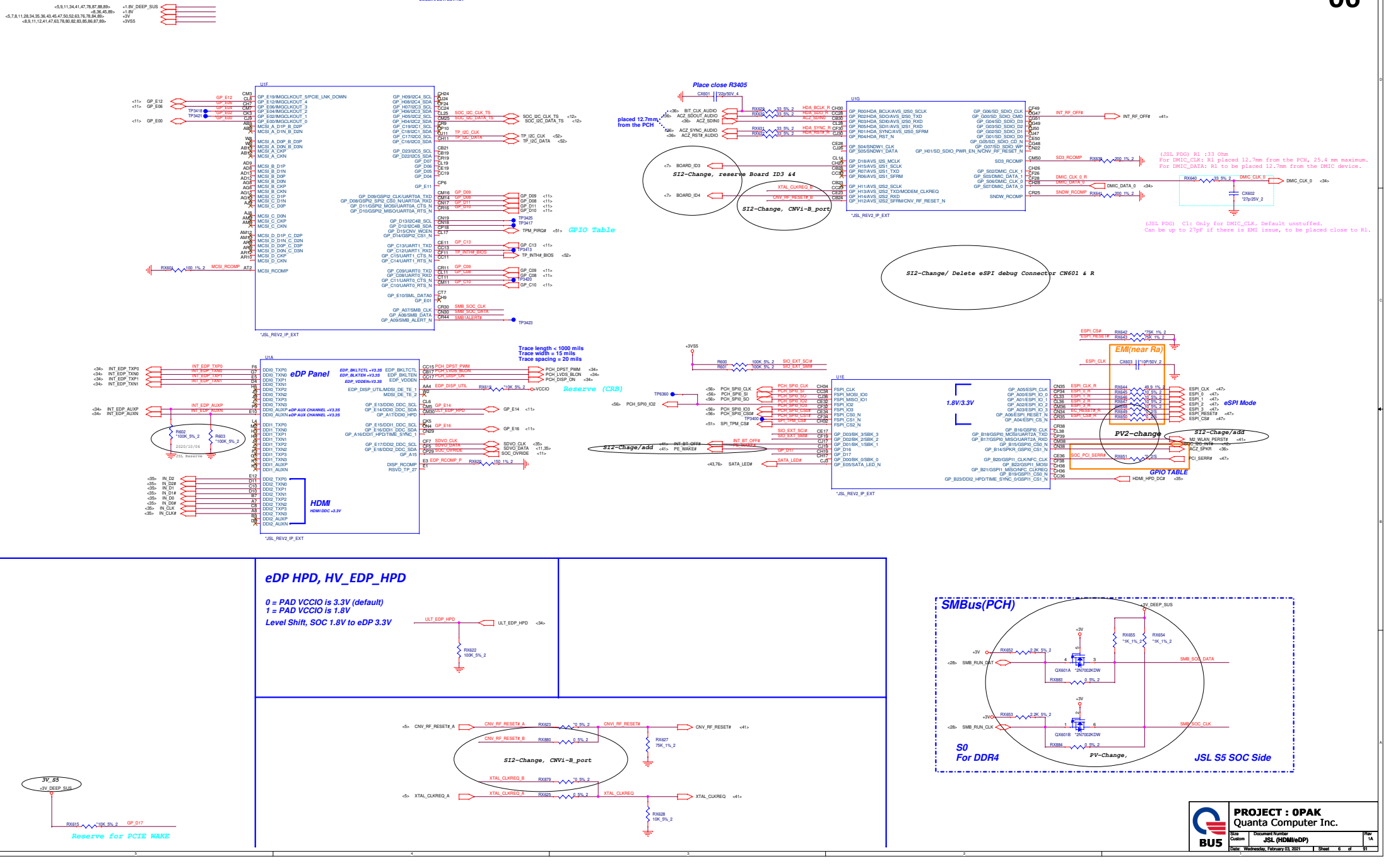




PROJECT : 0PAK
Quanta Computer Inc.
BU5
Size: Custom | Document Number: JSL (PCIE/USB/SATA/SPI) | Rev: 1A
Date: Wednesday, January 27, 2021 | Sheet 5 of 91

# Jasper Lake (DISPLAY/eDP/GPIO/SPI/EMMC/LPC)

EDP_HPD Default = 1.8V
PANEL0_BKLTCTL Default = 1.8V
PANEL0_BKLTEN Default = 1.8V
PANEL0_BKLTEN Default = 1.8V
Default = 3.3V. 3.3V/1.8V

06




## eDP HPD, HV_EDP_HPD

0 = PAD VCCIO is 3.3V (default)
1 = PAD VCCIO is 1.8V
Level Shift, SOC 1.8V to eDP 3.3V









## SMBus(PCH)



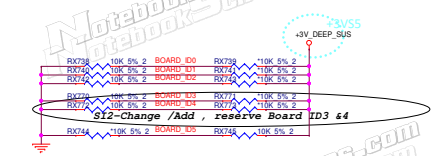

PROJECT : 0PAK
Quanta Computer Inc.
BUS
Size: Custom
Document Number: JSL (HDMI/eDP)
Rev: 1A
Date: Wednesday, February 03, 2021
Sheet 6 of 91

# Jasper Lake (I2C/XDP/GPIO)

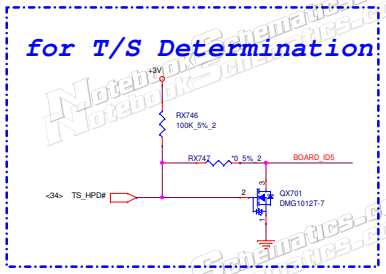
07




## BOARD ID

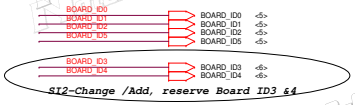



## for T/S Determination



## BOM Note:

| Board ID ( Default) | BIOS Strap Description |
|---|---|
| Board_ID0 =0 | 0 = none TPM<br>1 = TPM |
| Board_ID1 =0 | 0 = EMMC<br>1 = no EMMC(disablde EMMC function) |
| Board_ID2 =0 | 0 = 14" ID<br>1 = 15" ID |
| Board_ID3 =0 | Reserve-1 |
| Board_ID4 =0 | Reserve-2 |
| Board_ID5 | 0 = none touch panel<br>1 = touch panel<br>Active By eDP Cable Define |




## MEMORY ID

## BOM Note:

www.repairlap.com

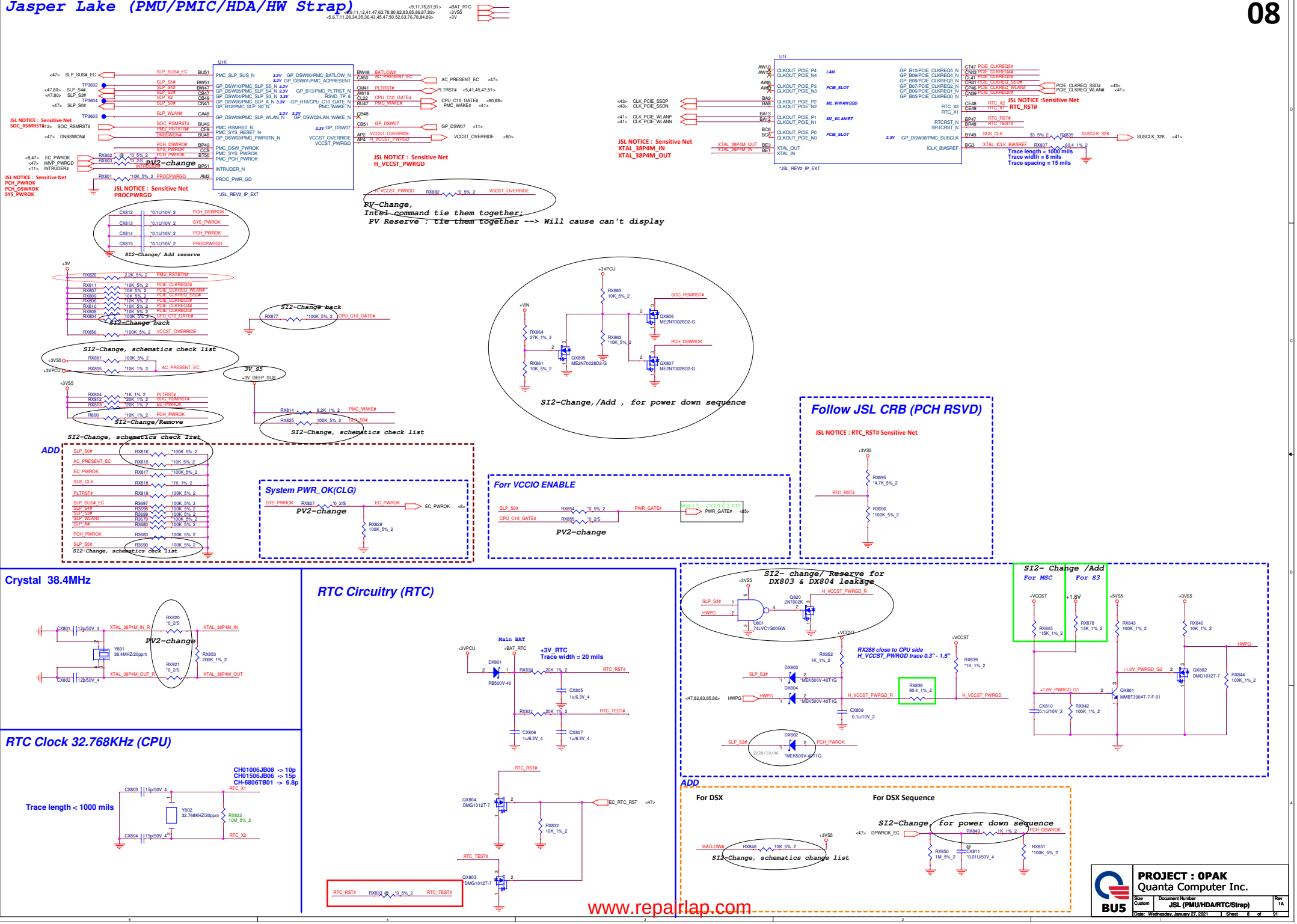
### CFG Signals Functionality and Termination

| CFG | Description | Termination | Resistor |
|---|---|---|---|
| CFG0 | CFG[0]: Stall reset sequence after PCU PLL lock until deasserted:<br>– 1 = (Default) Normal Operation; No stall.<br>– 0 = Stall. | Pull Up to VCCIO | 1K Ohm |
| CFG1,8,9,10,12,13 | RSVD | Pull Up to VCCIO | 1K Ohm |
| CFG2,3,5,6,7,11,14,15 | RSVD | No termination | N/A |
| CFG4 | CFG[4]: eDP enable:<br>– 1 = Disabled.<br>– 0 = Enabled. | Pull Down | 1K Ohm |

PROJECT : 0PAK
Quanta Computer Inc.
BU5
Size: Custom | Document Number: JSL (EMMC/LPC/SMB/ISH) | Rev: 1A
Date: Wednesday, January 27, 2021 | Sheet 7 of 91

# Jasper Lake (PMU/PMIC/HDA/HW Strap)



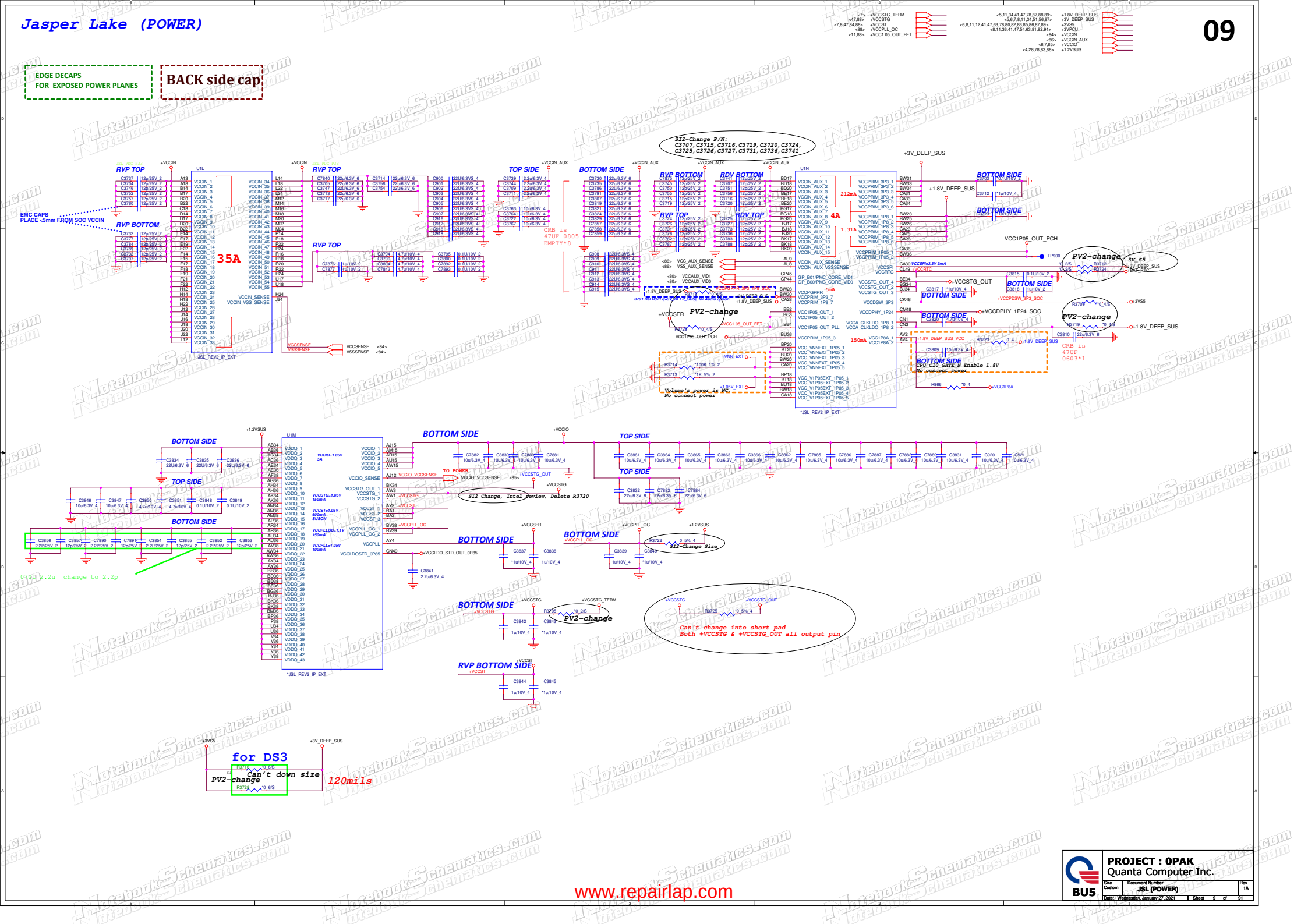


# Jasper Lake (POWER)



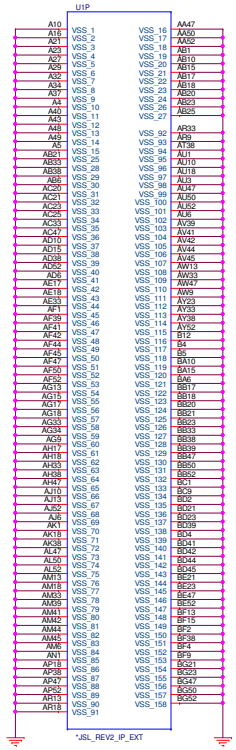
EDGE DECAPS
FOR EXPOSED POWER PLANES

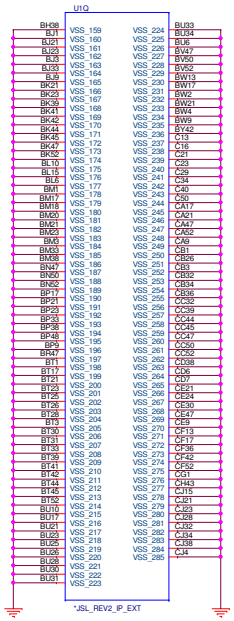
BACK side cap

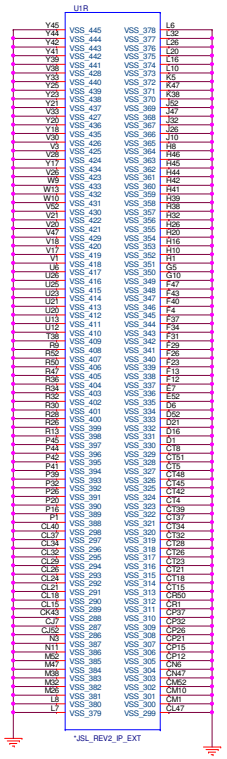





PROJECT : 0PAK
Quanta Computer Inc.
BU5
Size: Custom | Document Number: JSL (POWER) | Rev: 1A
Date: Wednesday, January 27, 2021 | Sheet 9 of 91



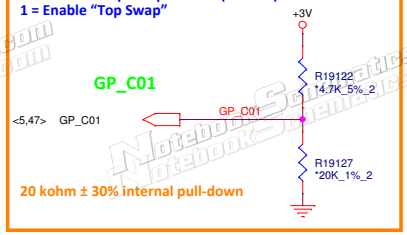






| | | | |
|---|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | | |
| Size: Custom | Document Number: JSL (GND/XDP) | | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 10 of 91 | | |

## TOP SWAP OVERRIDE

0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap"

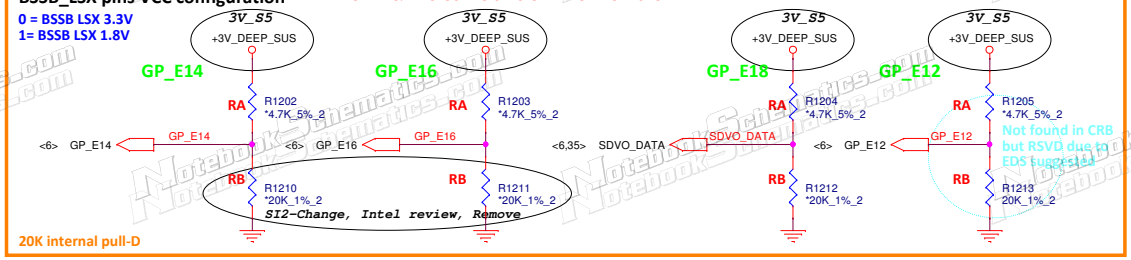



20 kohm ± 30% internal pull-down

## BSSB_LSX pins VCC configuration

PLACE RA & RB CLOSE TO SPI SIGNAL TO AVOID STUB

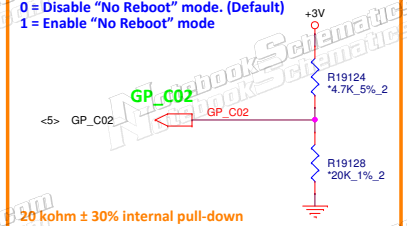
0 = BSSB LSX 3.3V
1= BSSB LSX 1.8V




20K internal pull-D

## NO REBOOT(CRB pull up)

0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode

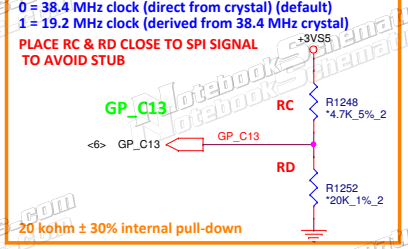



20 kohm ± 30% internal pull-down

## CPUNSSC Clock Frequency

0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)

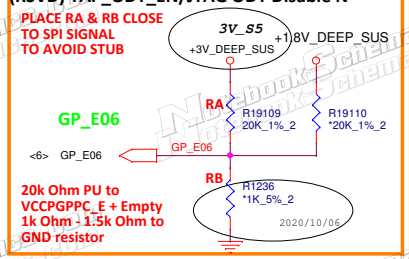
PLACE RC & RD CLOSE TO SPI SIGNAL TO AVOID STUB




20 kohm ± 30% internal pull-down

## (RSVD) TAP_ODT_EN/JTAG ODT Disable N

PLACE RA & RB CLOSE TO SPI SIGNAL TO AVOID STUB

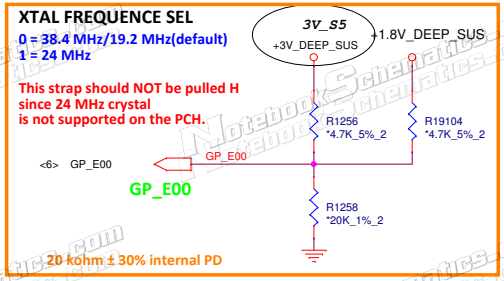



20k Ohm PU to VCCPGPPC_E + Empty
1k Ohm - 1.5k Ohm to GND resistor

## XTAL FREQUENCE SEL

0 = 38.4 MHz/19.2 MHz(default)
1 = 24 MHz

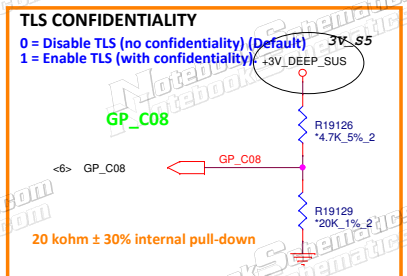
This strap should NOT be pulled H since 24 MHz crystal is not supported on the PCH.




20 kohm ± 30% internal PD

## TLS CONFIDENTIALITY

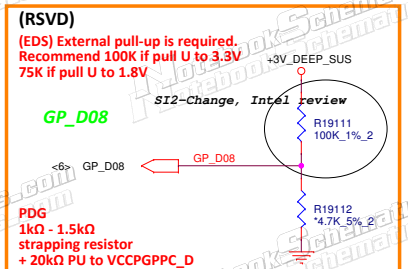
0 = Disable TLS (no confidentiality) (Default)
1 = Enable TLS (with confidentiality)




20 kohm ± 30% internal pull-down

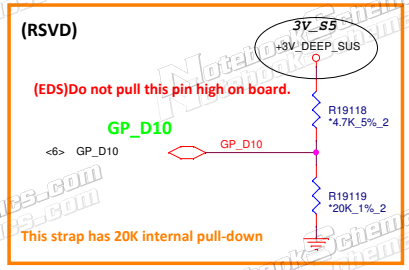
## (RSVD)

(EDS) External pull-up is required.
Recommend 100K if pull U to 3.3V
75K if pull U to 1.8V




PDG
1kΩ - 1.5kΩ
strapping resistor
+ 20kΩ PU to VCCPGPPC_D

## (RSVD)




(EDS)Do not pull this pin high on board.

This strap has 20K internal pull-down

## M.2 CNVi Mode Select

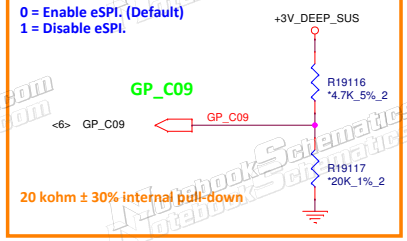
0 = Integrated CNVi enabled.
1 = Integrated CNVi disabled.

stuff on P41

no internal termination.
A weak external pull-up is required.

## eSPI Disable

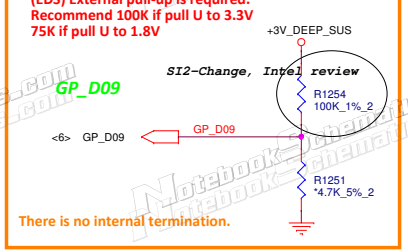
0 = Enable eSPI. (Default)
1 = Disable eSPI.




20 kohm ± 30% internal pull-down

## (RSVD)

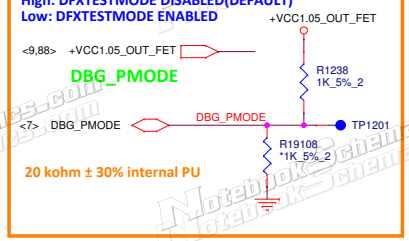
(EDS) External pull-up is required.
Recommend 100K if pull U to 3.3V
75K if pull U to 1.8V




There is no internal termination.

## (RSVD) DBG_PMODE

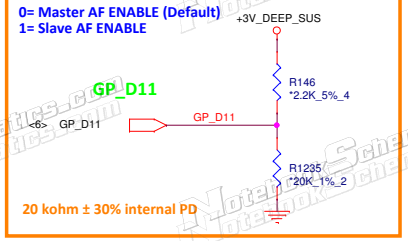
High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED




20 kohm ± 30% internal PU

## eSPI Flash Sharing Mode

0= Master AF ENABLE (Default)
1= Slave AF ENABLE

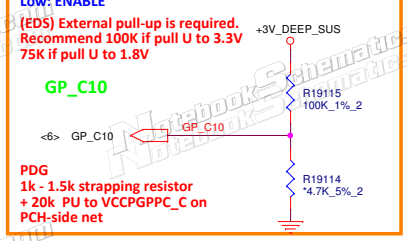



20 kohm ± 30% internal PD

## (RSVD) BOOT_HALT_N Strap

High: DISABLE
Low: ENABLE

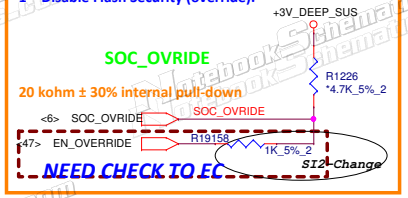
(EDS) External pull-up is required.
Recommend 100K if pull U to 3.3V
75K if pull U to 1.8V




PDG
1k - 1.5k strapping resistor
+ 20k PU to VCCPGPPC_C on PCH-side net

## Flash Descriptor Security Override

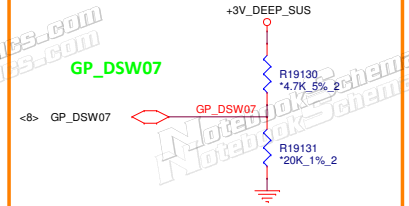
0 = Enable Flash security (Default)
1 = Disable Flash Security (override).




20 kohm ± 30% internal pull-down

## (RSVD) GP_DSW07

This strap should sample LOW.

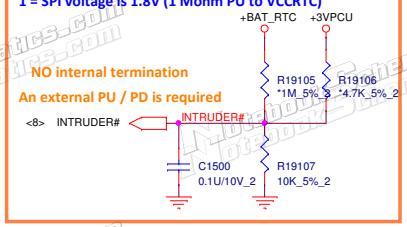



20 kohm ± 30% internal pull-down

## SPI Voltage Configuration

0 = SPI voltage is 3.3V (10 kohm PD to GND)
1 = SPI voltage is 1.8V (1 Mohm PU to VCCRTC)

NO internal termination
An external PU / PD is required




BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

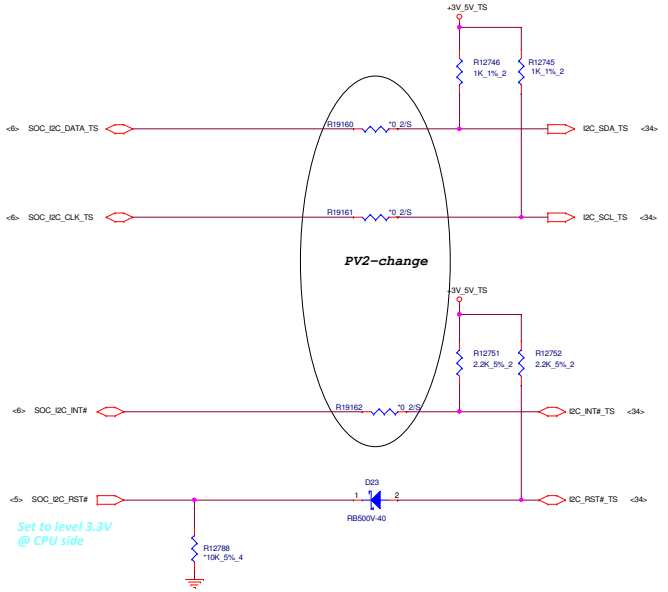
| Size | Document Number | Rev |
|---|---|---|
| Custom | HW STRAPS | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 11 of 91 | |

## SERIRQ

ALL PMU 3.3V/1.8V
Default all 3.3V

## eDP Signal

## Touch Screen (I2C)




## SLP_S3# & SLP_S4#

ALL PMU 3.3V/1.8V
Default all 3.3V

## PWRBTN#/PCIE_WAKE#

SOC_PWRBTN# Default is 3.3V
SOC_PMC_WAKE Default is 3.3V

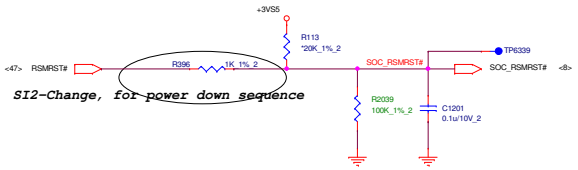
## PLTRST#

ALL PMU 3.3V/1.8V
Default all 3.3V

## SMI & SCI

## IO Thrm Protect

## RSMRST#




BUS

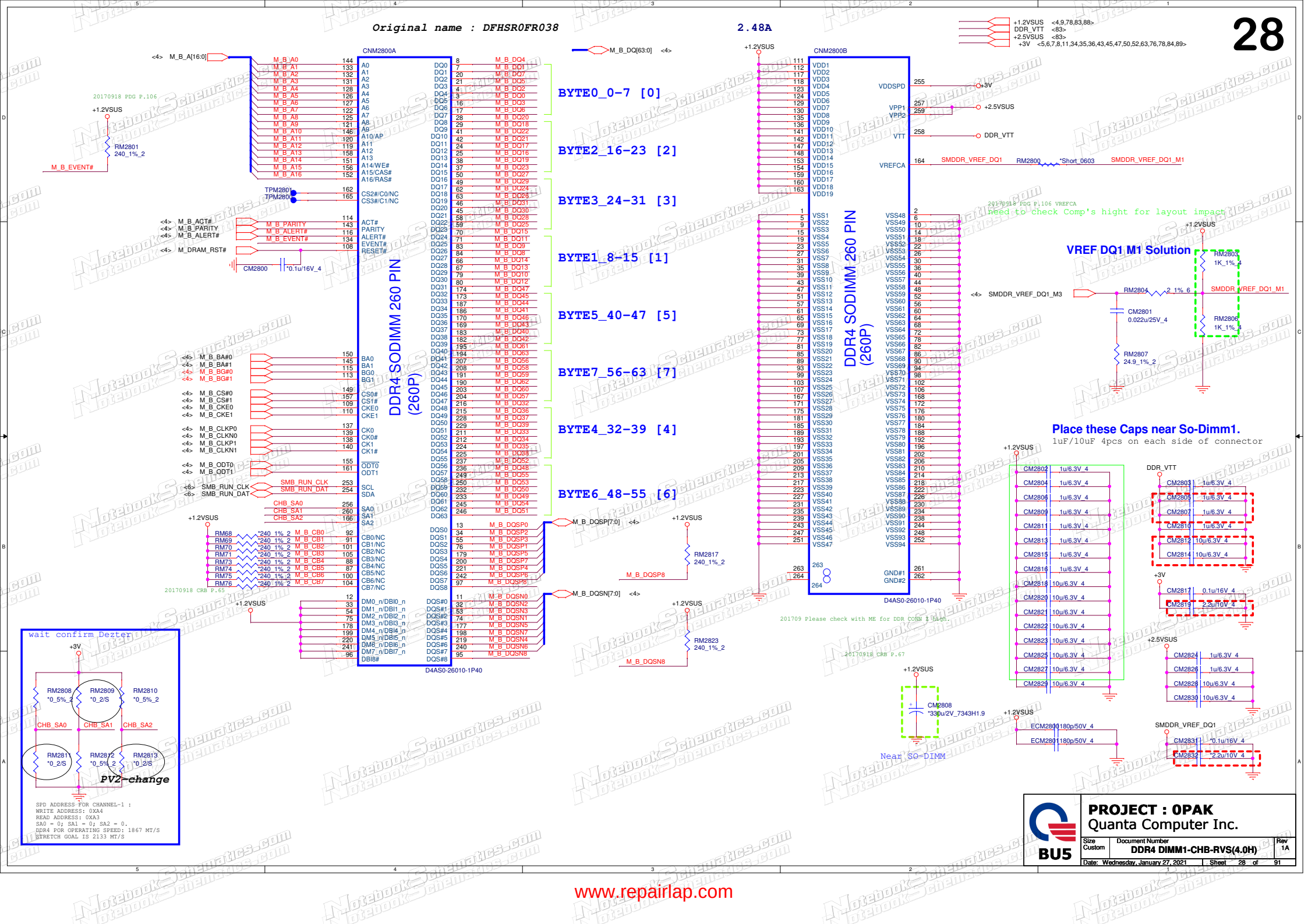
**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Level shift/Thermistor | 1A |

Date: Wednesday, January 27, 2021 | Sheet 12 of 91

Original name : DFHSR0FR038

2.48A

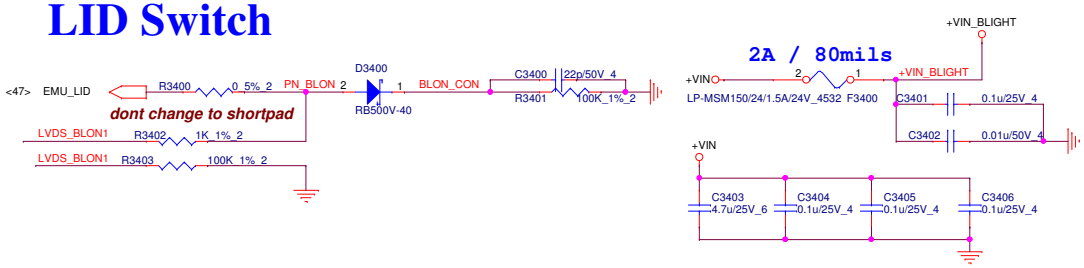



PROJECT : 0PAK
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR4 DIMM1-CHB-RVS(4.0H) | 1A |

Date: Wednesday, January 27, 2021 Sheet 28 of 91

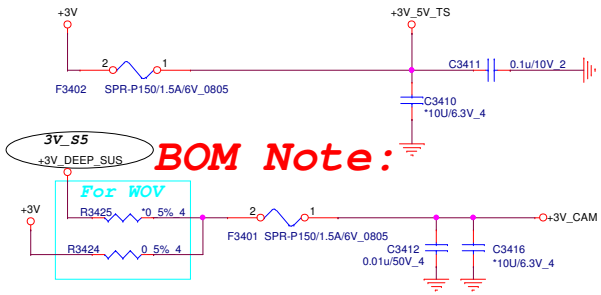
# LID Switch

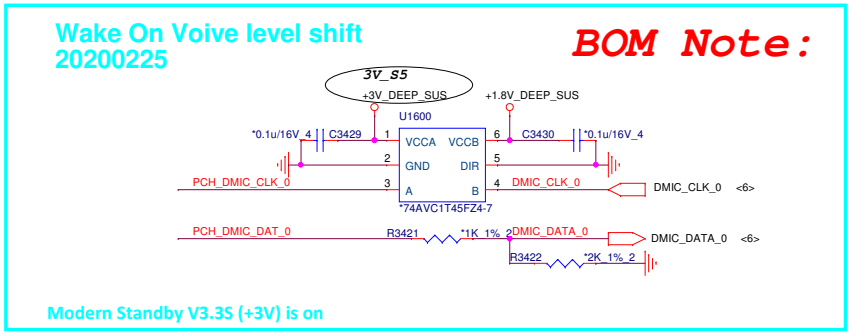






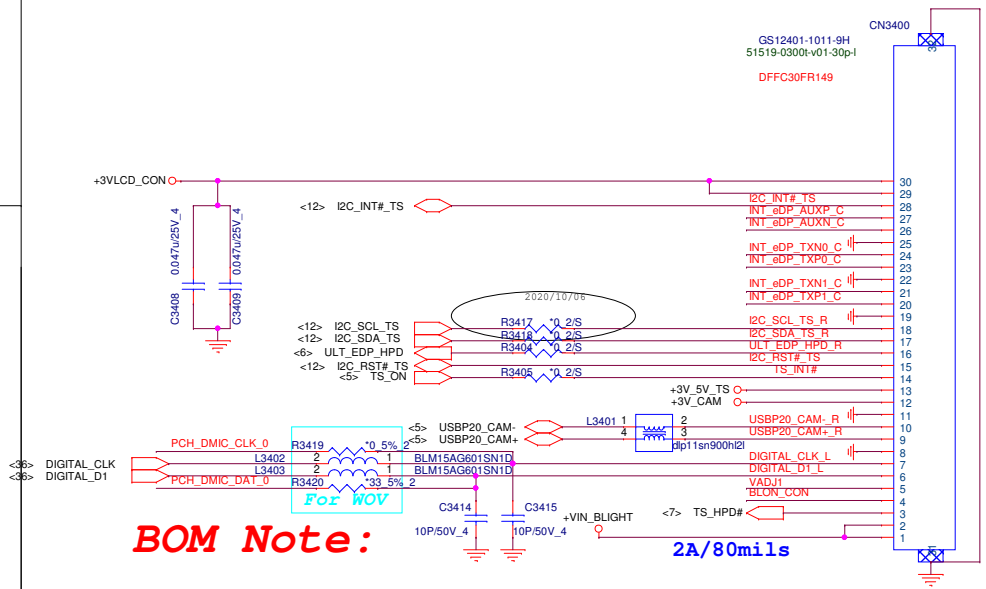
# Touch screen

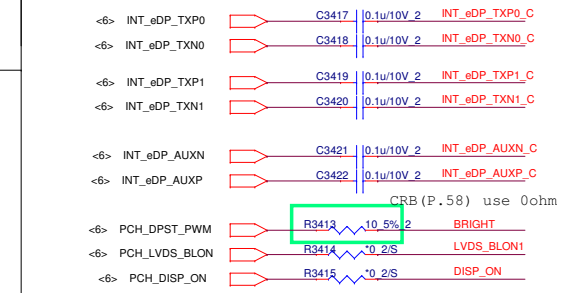


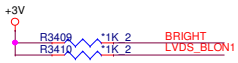



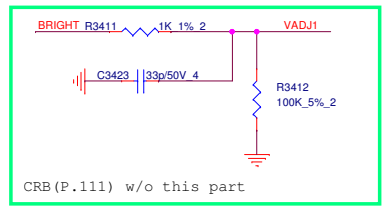

# eDP Conn.

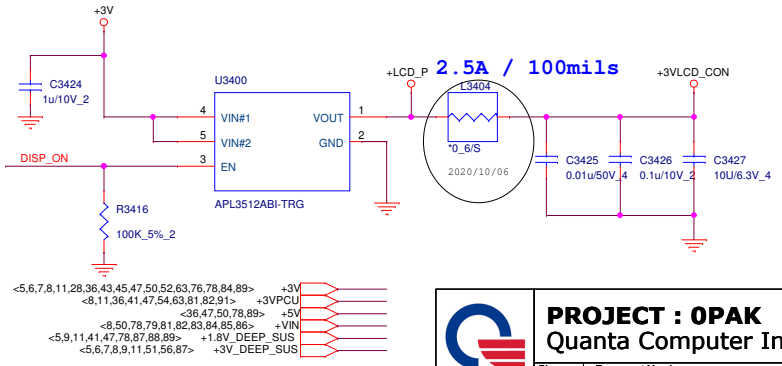




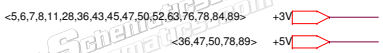

BU5

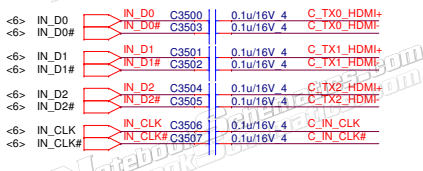
**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | eDP/IR CAM/LID/CAM/MIC/TS | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 34 of 91 | |

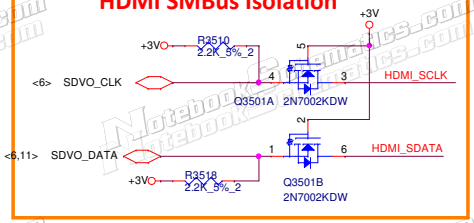
# HDMI CONN



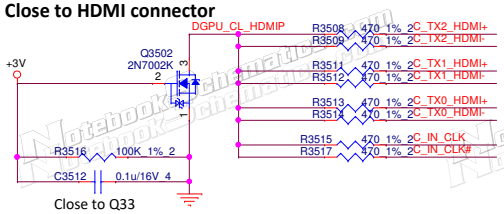


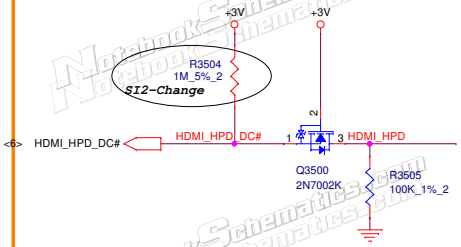

## HDMI SMBus Isolation



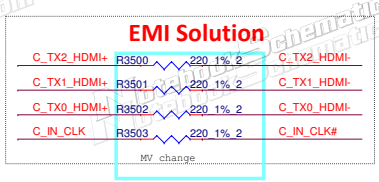

## Close to HDMI connector

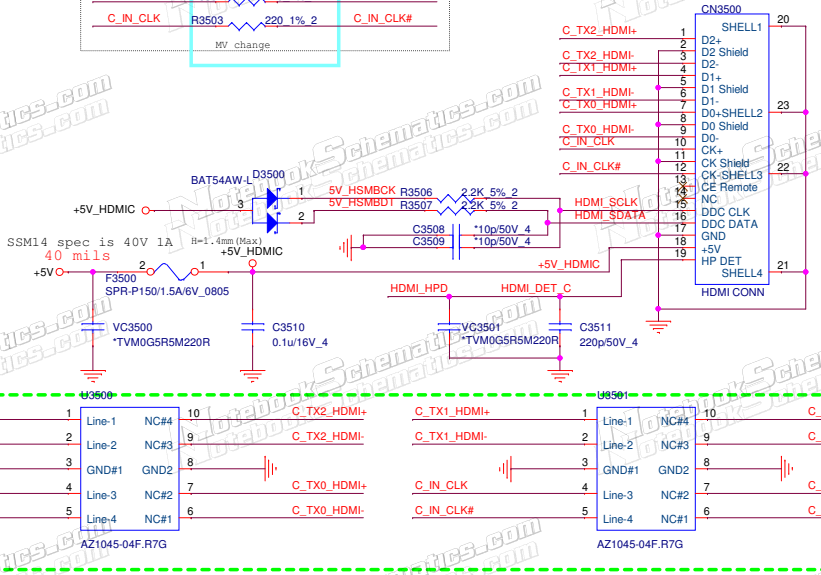



## HPD




## EMI Solution






PROJECT : 0PAK
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | HDMI | 1A |

BU5

Date: Thursday, February 04, 2021 Sheet 35 of 91

# Audio Codec



REALTEK

ANALOG
DIGITAL

ALC3247
(Include Thermal pad)
QFN40 (5x5)

Place on A/DGND moat

Close to audio codec

Close to PIN1

Close to PIN9

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possilbe

TO Headphone jack

BOM Note:

No need headphone amplifier keep codec pin 10 floating

Default: None Amp.

+3V or +1.8V, Based on which platform

SI modify 0530

Close to Speaker
Speaker 4 ohm: 40mils

Speaker Power Down Control Circuit

SI modify 0530

Close to CODEC
place to near U3600 or under codec

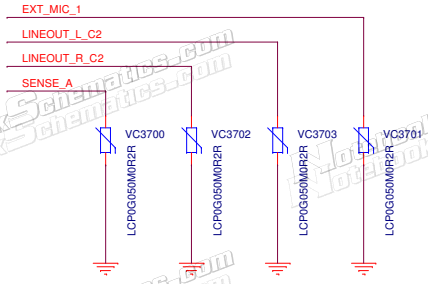
FOR EMI

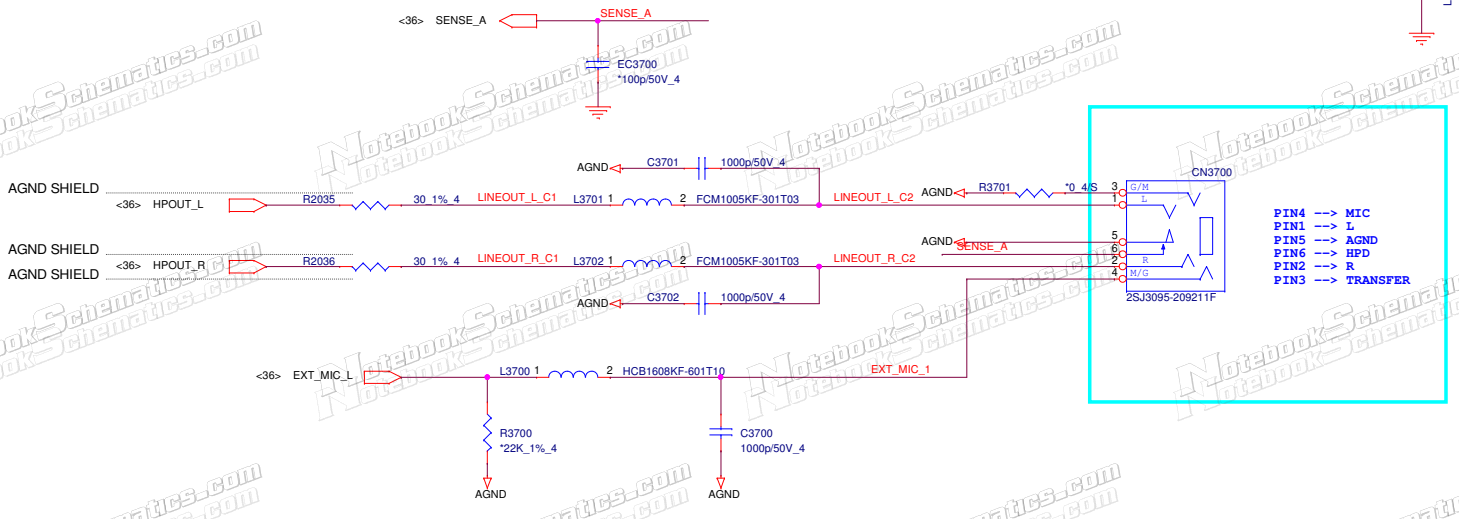
| | |
|---|---|
| PROJECT : 0PAK | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: Codec ALC3247 |
| Rev: 1A | |
| Date: Tuesday, February 02, 2021 | Sheet 36 of 91 |

# Audio Combo Jack



## Audio JACK ESD




| | | |
|---|---|---|
| PROJECT : 0PAK<br>Quanta Computer Inc. | | |
| BU5 | Size: Custom<br>Document Number: Audio Jack | Rev: 1A |
| | Date: Wednesday, January 27, 2021 | Sheet 37 of 91 |

# WLAN

## GLK WLAN Discharge

41

Mini Card
WLAN/BT(Option)

| CNV-i CONN. Pin | Net name | Voltage |
|---|---|---|
| 10 | PPCM_SYNC/LCP_RSTN | GPIO Power Configuration - 1.8v |
| 14 | PCM_OUT/CLKREQ0 | GPIO Power Configuration - 1.8v |
| 22 | UART_RX / BRI_RSP | GPIO Power Configuration - 1.8v |
| 32 | UART_TX / RGI_DT | GPIO Power Configuration - 1.8v |
| 34 | UART_CTS / RGI_RSP | GPIO Power Configuration - 1.8v |
| 36 | UART_RTS / BRI_DT | GPIO Power Configuration - 1.8v |
| 50 | SUSCLK | GPIO Power Configuration - 3.3v |
| 52 | PERST0_N | GPIO Power Configuration - 3.3v |
| 53 | CLKREQ0_N | GPIO Power Configuration - 3.3v |
| 54 | W_DISABLE2_N | GPIO Power Configuration - 3.3v |
| 56 | W_DISABLE1_N | GPIO Power Configuration - 3.3v |

Remove Net RF_LINK# and need check if Ra and Rb can be NI

CN4100
AS0BC26-S30BE-7H
NGFF EKEY

For Current sense

SI2-Change/Add/reserve

Support Wake Function (Reserve )

SI2-Change, Intel review change to 200K

SI2-Change, Intel review change to 1K from 100K

SI2-Change/Add

Reserve for WLAN reset only

NGFF PIN52 is not defined @ CNVi

Reserved the MOSFET at CLKREQ# even the current leakage test passed for HP requested

DO NOT CHANGE TO SHORTPAD

M.2 CNVi Mode Select
0 = Integrated CNVi enabled.
1 = Integrated CNVi disabled.
GP_E22/CNV_RGI_DT

A weak external pull-up is required.

close PCH

PD at CPU side RX1033

CNVi BRI_RSP, RGI_RSP 49.9 Ohm, to be placed close to the connector.
CNVi BRI_DT(R3314), RGI_DT(R3313) 0 Ohm placed at PCH side.

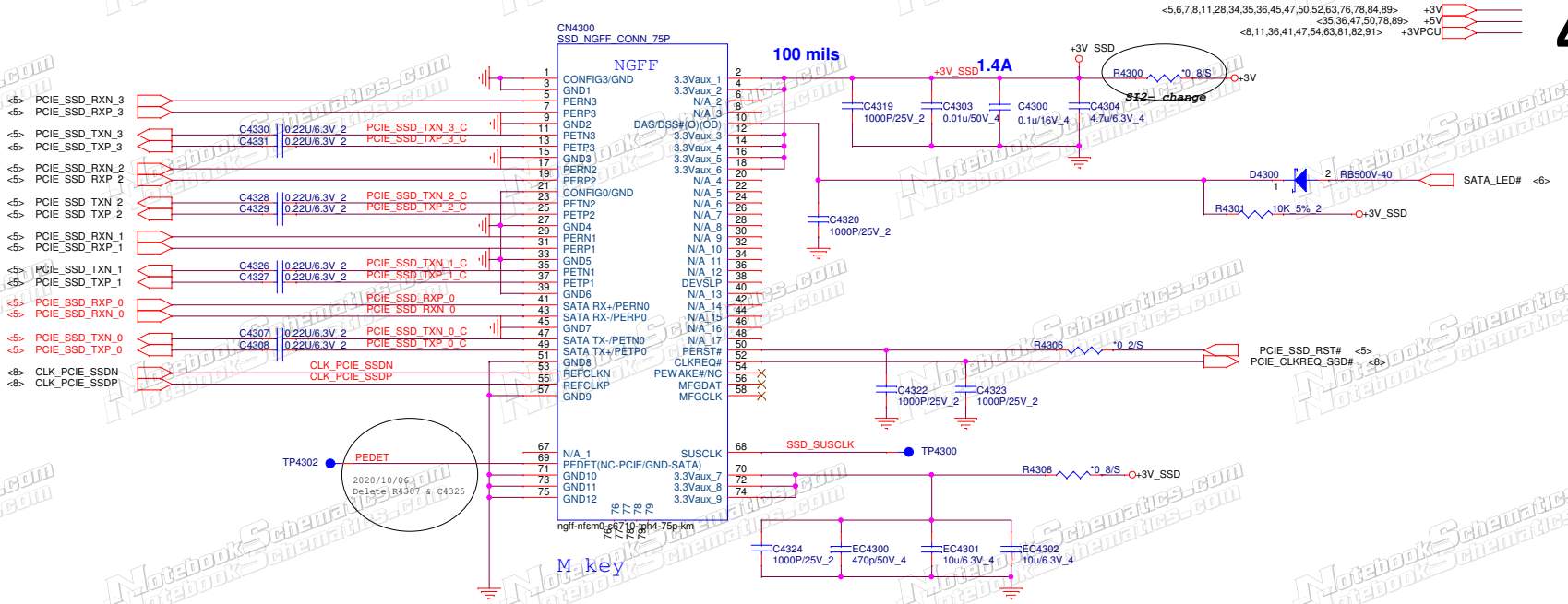
**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | WLAN(NGFF) | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 41 of 91 | |

BU5

# SATA SSD



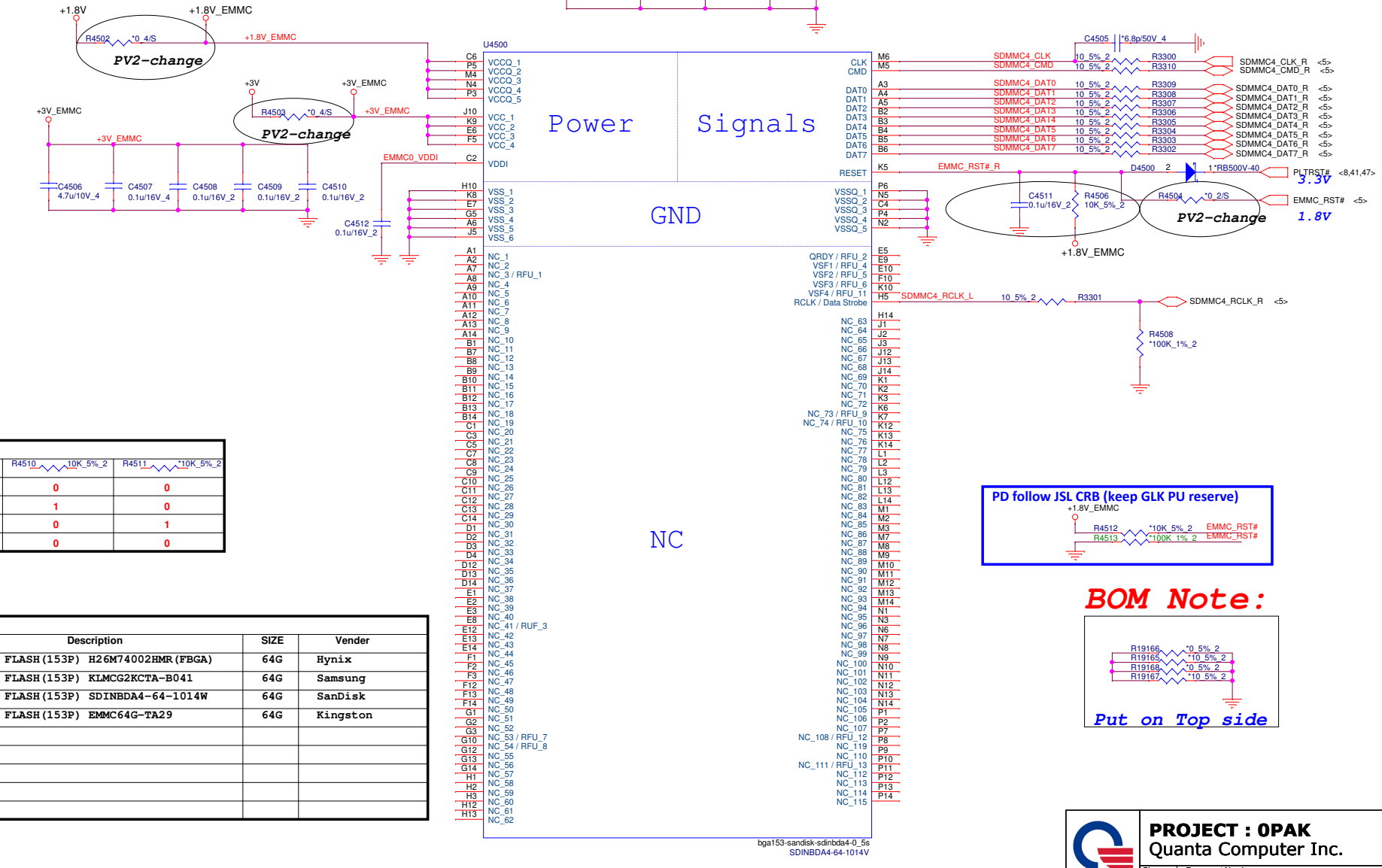



# PCIE AND SATA MUX--> JSL remove 3/9

| | | | |
|---|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: SSD(NGFF) | Rev: 1A |
| | Date: Wednesday, January 27, 2021 | Sheet 43 of 91 | |

<5,6,7,8,11,28,34,35,36,43,47,52,76,78,84,89> +3V
<8,36,89> +1.8V
<5,9,11,34,41,47,78,87,88,89> +1.8V_DEEP_SUS

# BOM Note:




# BOM Note:

| eMMC Setting | | | |
|---|---|---|---|
| Vendor | R4509 *10K_5%_2 | R4510 10K_5%_2 | R4511 *10K_5%_2 |
| 32G | 1 | 0 | 0 |
| 64G | 0 | 1 | 0 |
| 128G | 0 | 0 | 1 |
| None eMMC | 0 | 0 | 1 |

PD follow JSL CRB (keep GLK PU reserve)




# BOM Note:




## BOM

footprint : BGA 153
BGA 153 PIN : 11.5mmX13mm

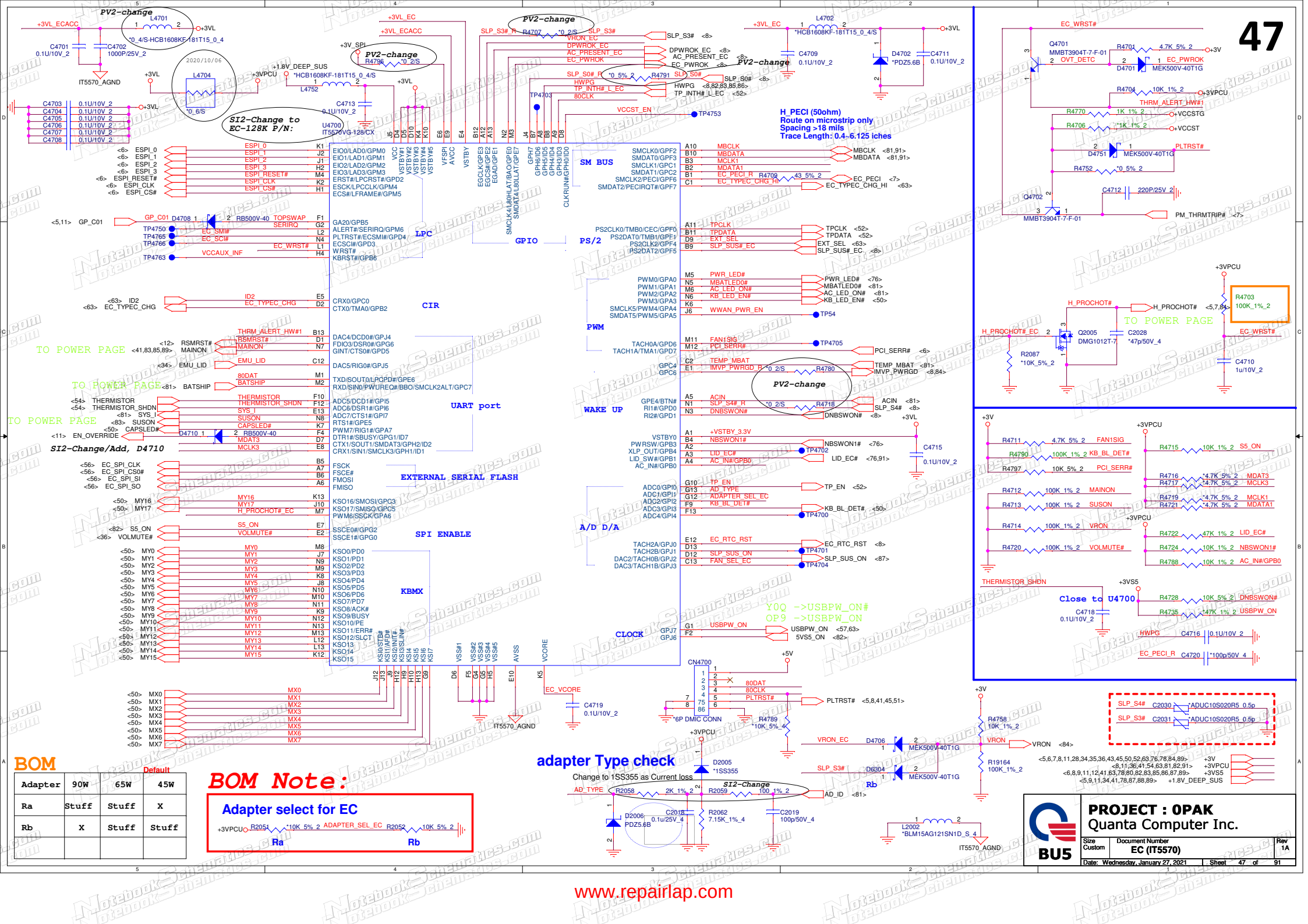
| iNAND (eMMC) V5.1 | | | | |
|---|---|---|---|---|
| TOP BS | QCI P/N | Description | SIZE | Vender |
| AKE3TZPTW03 | AKE3TZPTW02 | IC FLASH(153P) H26M74002HMR(FBGA) | 64G | Hynix |
| AKE3TZ-T504 | AKE3TZ-T503 | IC FLASH(153P) KLMCG2KCTA-B041 | 64G | Samsung |
| AKE3TZ0T105 | AKE3TZ0T106 | IC FLASH(153P) SDINBDA4-64-1014W | 64G | SanDisk |
| AKE3TZ-TP06 | AKE3TZ-TP05 | IC FLASH(153P) EMMC64G-TA29 | 64G | Kingston |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | EMMC | 1A |

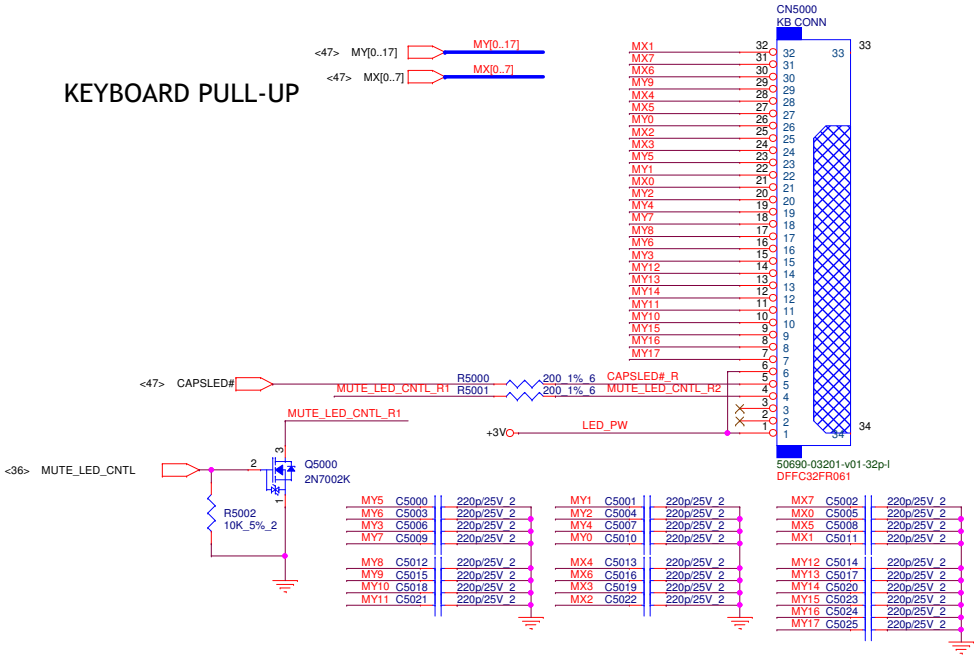
Date: Wednesday, February 03, 2021 Sheet 45 of 91



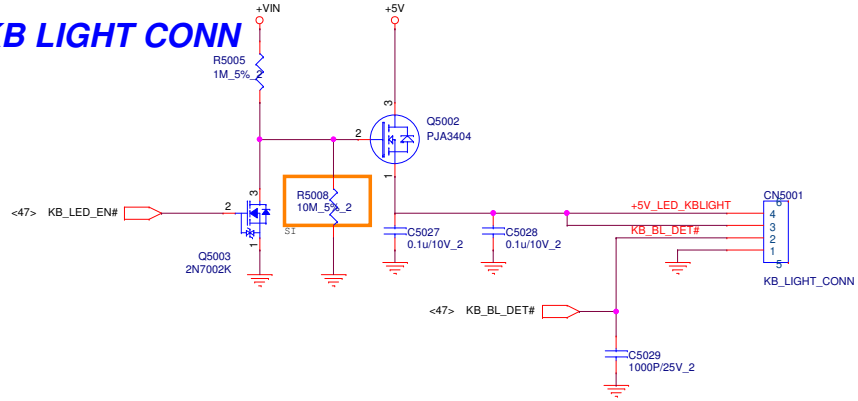

| Adapter | 90W | 65W | 45W |
|---|---|---|---|
| Ra | Stuff | Stuff | X |
| Rb | X | Stuff | Stuff |
| | | | |

# KEYBOARD Con.

KEYBOARD PULL-UP




## KB LIGHT CONN




<6,8,9,11,12,41,47,63,78,80,83,85,86,87,89> +3VS5
<5,6,7,8,11,28,34,35,36,43,47,52,76,78,84,89> +3V
<8,57,78,84,86,89> +5VS5
<64> +TYPEC_VBUS

BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

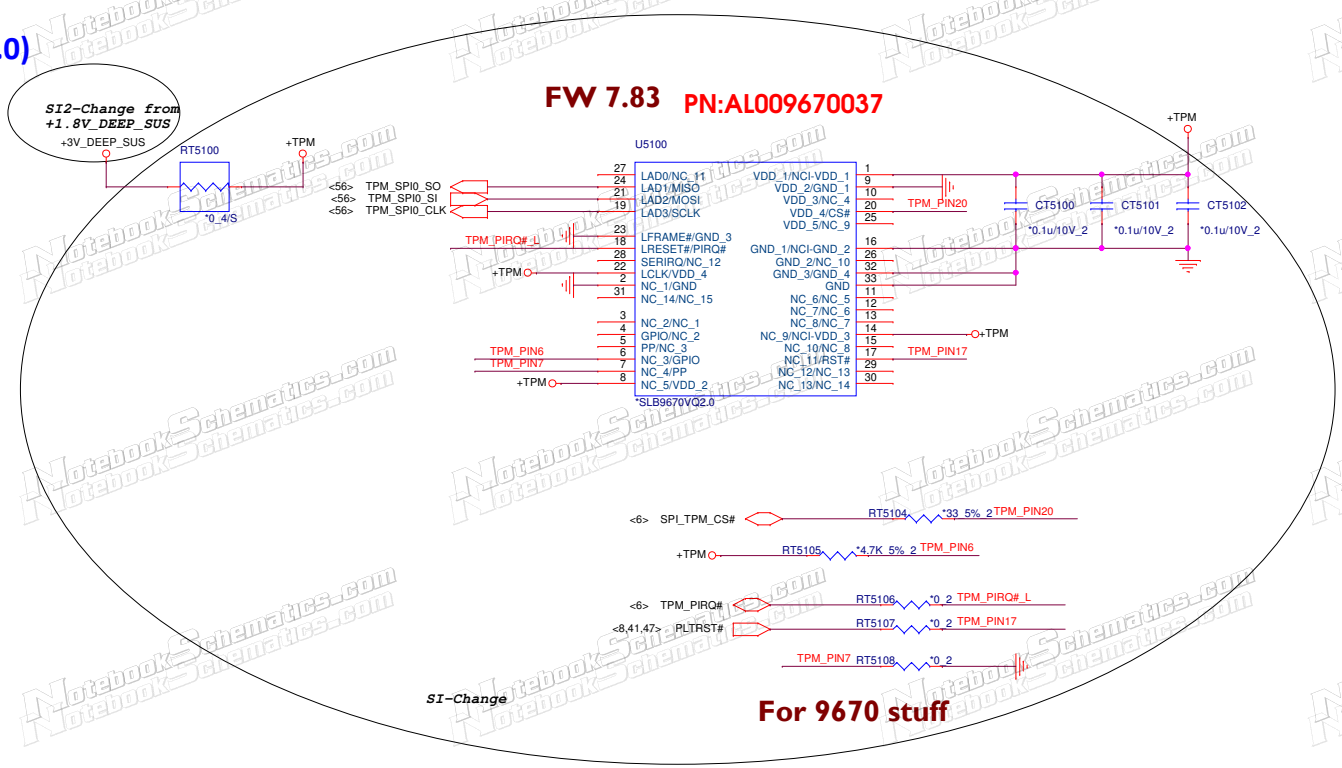
| Size | Document Number | Rev |
|---|---|---|
| Custom | KB/KB LIGHT | 1A |

Date: Wednesday, January 27, 2021 Sheet 50 of 91

# TPM

**BOM Note:**

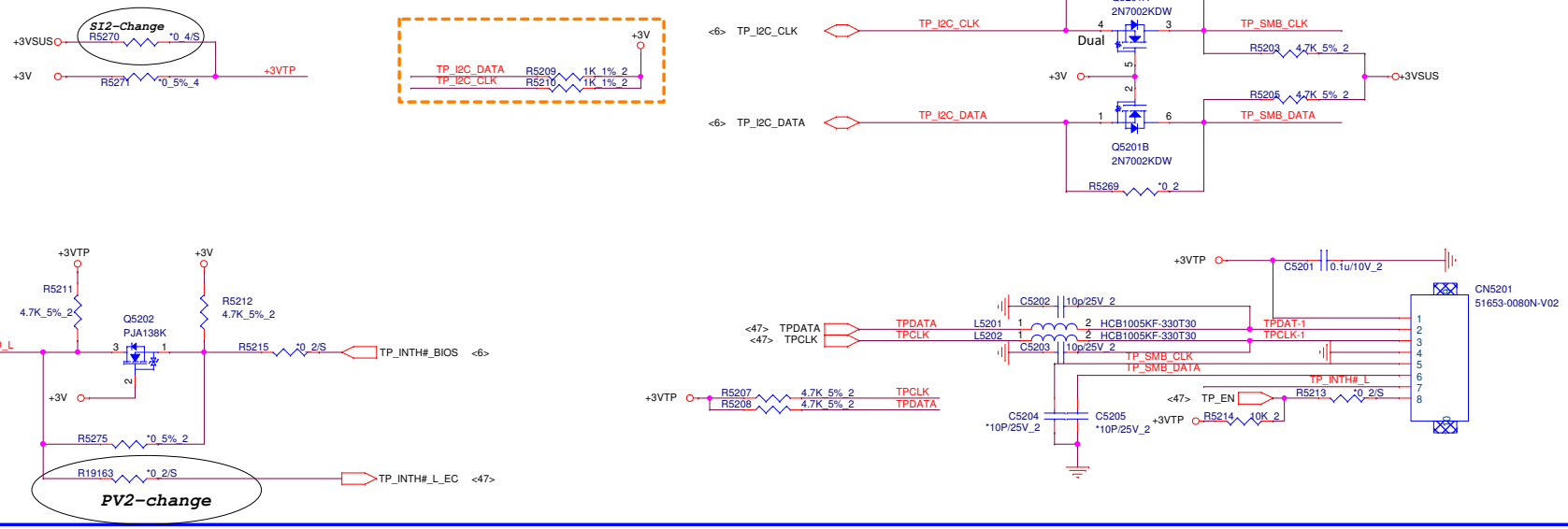
TPM (2.0)



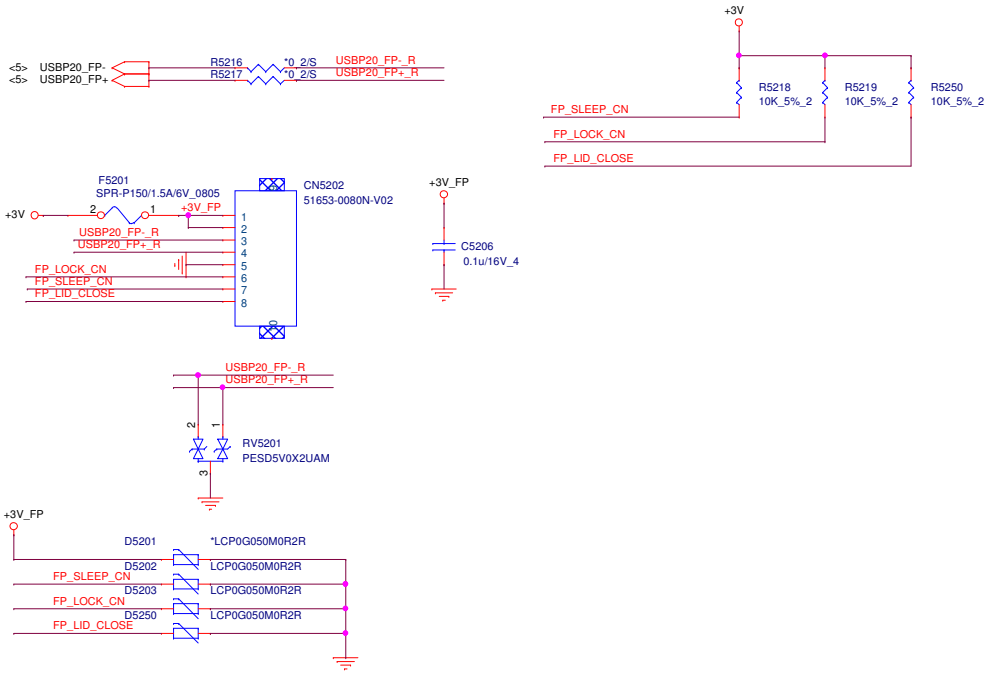



| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: TPM | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 51 of 91 | |

# Touch Pad




# Finger print



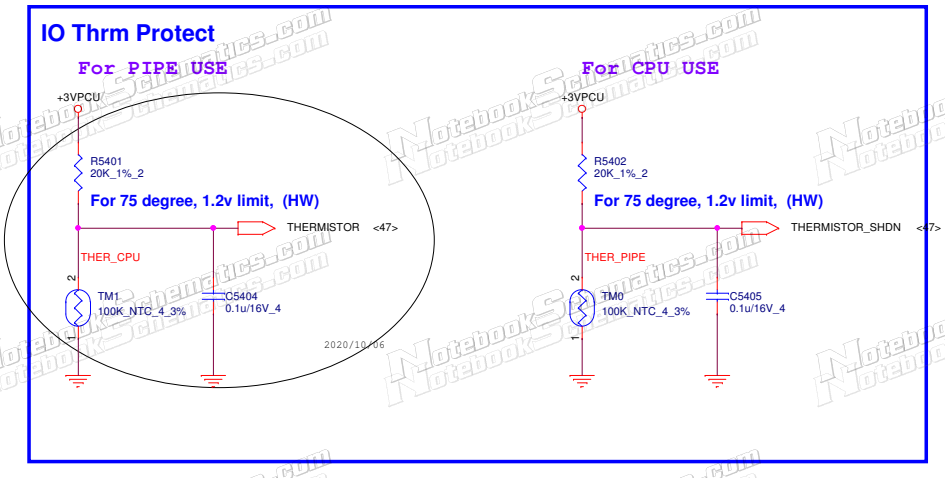

USB 2.0 Re_Driver

| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: Touch pad/Finger Print | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 52 of 91 | |

# FAN/Thermal



<35,36,47,50,78,89> +5V




BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | FAN/Thermal | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 54 of 91 | |

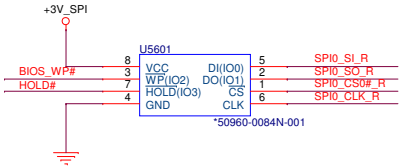
# BIOS ROM 16M (CLG)



## U5600,U5601,U5602 co-lay

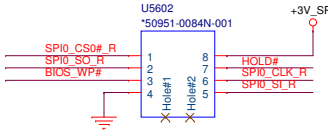
SPI ROM Socket (SO-8)
DG008000011

BOM Note:
DB stage

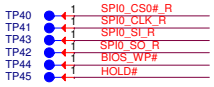


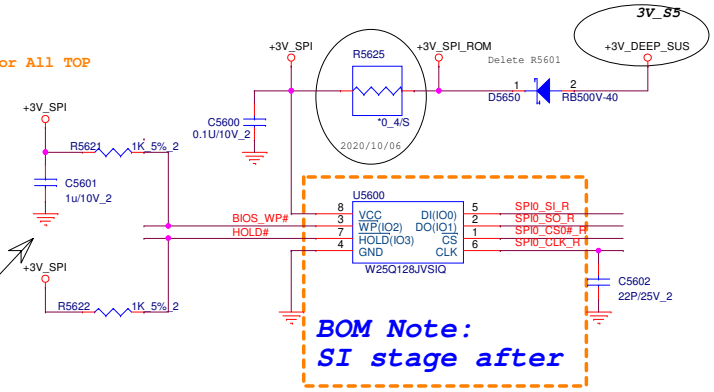

Without Boss /SPI ROM Socket
DFHS08FS046

BOM Note:
DB stage

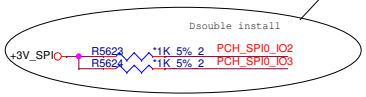


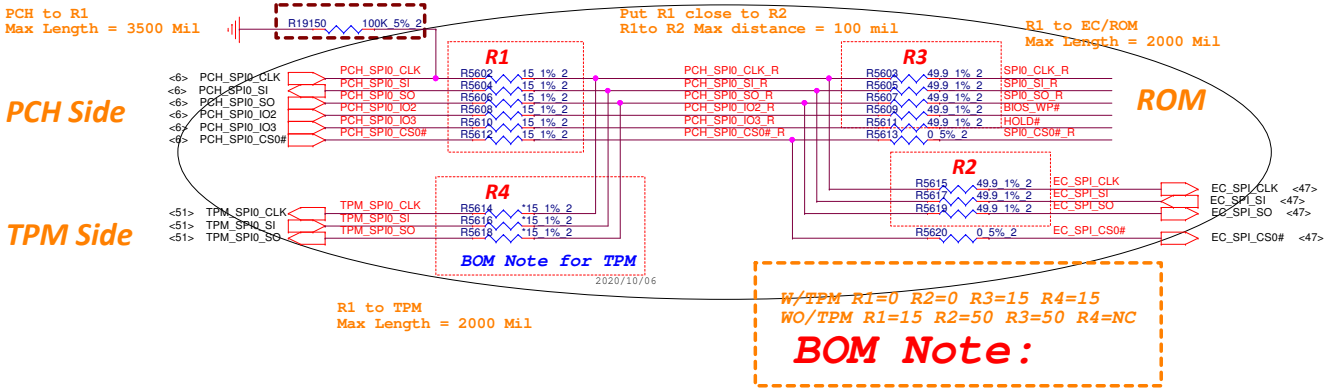

TP40~TP45 need place to All BOT or All TOP




BOM Note:
SI stage after




W/TPM R1=0 R2=0 R3=15 R4=15
WO/TPM R1=15 R2=50 R3=50 R4=NC

BOM Note:

## SPI ROM(SO-8)

BOM Note:

| Vender | Size | P/N |
|---|---|---|
| GigaDevice | 16MB | AKE3DZN0Q02 IC FLASH(8P)GD25B127DSIGR(SOP) |
| MAXIN | 16MB | AKE3DZN0Z03 IC FLASH(8P) MX25L12873FM2I-10G(SOP) |
| XMC | 16MB | AKE3DGN0X00 IC FLASH(8P) XM25QH128AHIGT(SOP) |
| WND | 16MB | AKE3DF-KN01 IC FLASH(8P) W25Q128JVSIQ(SOIC) |
| Socket | | DG008000011 |

## SPI ROM(WSON)

BOM Note:

| Vender | Size | P/N |
|---|---|---|
| GigaDevice | 16MB | AKE2DF00Q00IC FLASH(8P)GD25B127DWIGR(WSON8) |
| MAXIN | 16MB | AKE3DZN0Z06IC FLASH(8P) MX25L12873FZNI-10G(WSON) |
| WND | | |
| | | |
| Socket | | DFHS08FS046 |

<5,6,7,8,9,11,34,51,87> +3V_DEEP_SUS
<8,11,36,41,47,54,63,81,82,91> +3VPCU
<6,8,9,11,12,41,47,63,78,80,82,83,85,86,87,89> +3VS5

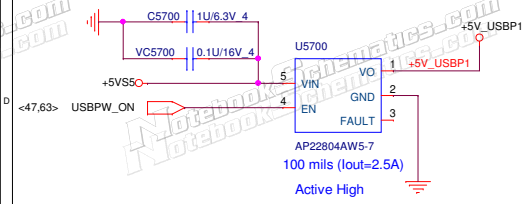
PROJECT : 0PAK
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | FLASH ROM | 1A |

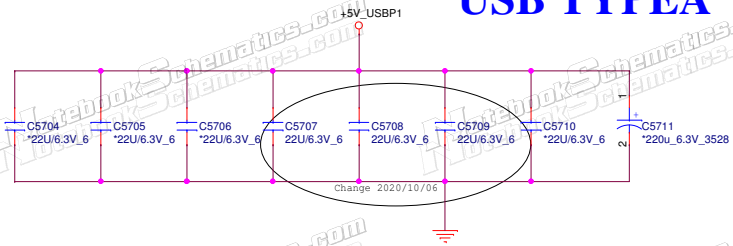
Date: Wednesday, January 27, 2021 Sheet 56 of 91

BU5

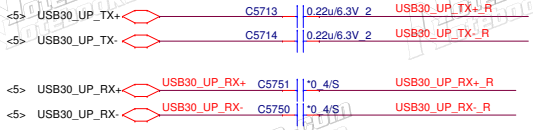
# USB TYPEA

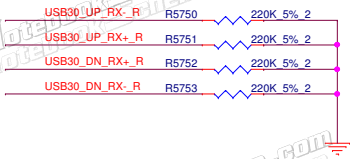



Active High

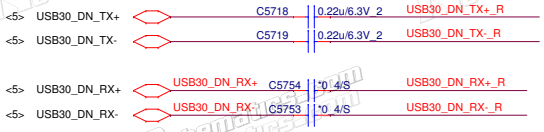


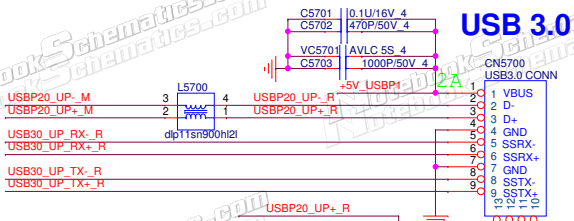

## USB3.0 PORT4

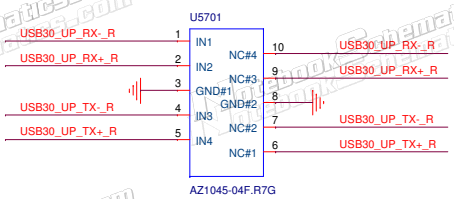


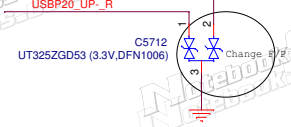



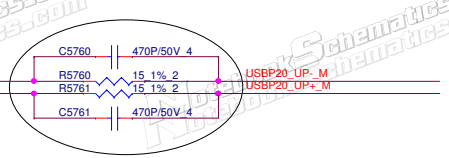

## USB3.0 PORT2

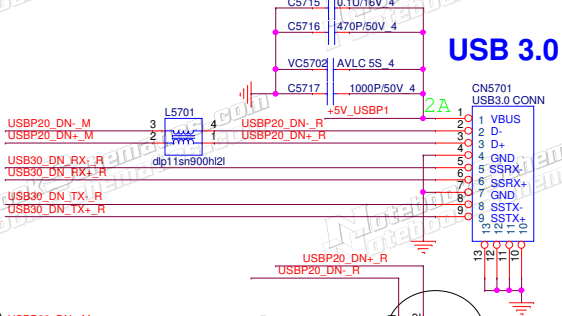


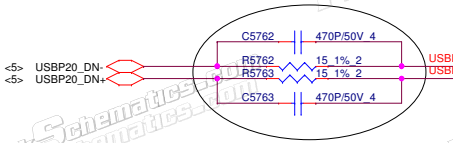



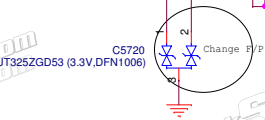



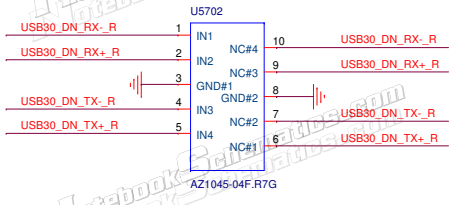



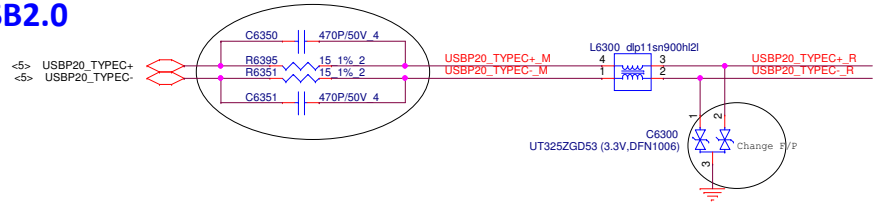


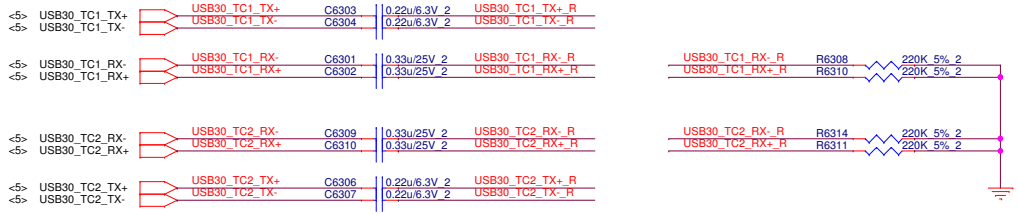

BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

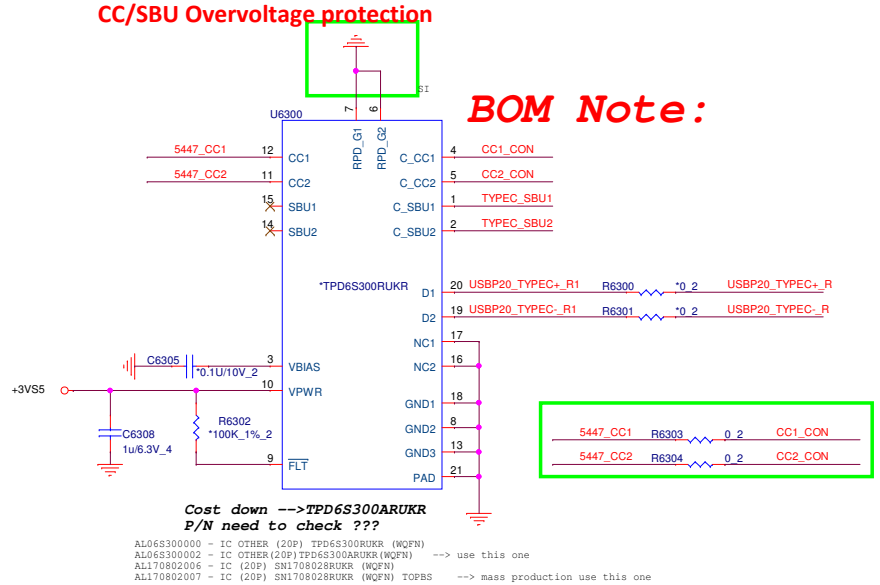
| Size | Document Number | Rev |
|---|---|---|
| Custom | USB TYPEA <RightX2> | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 57 of 91 | |

## USB2.0



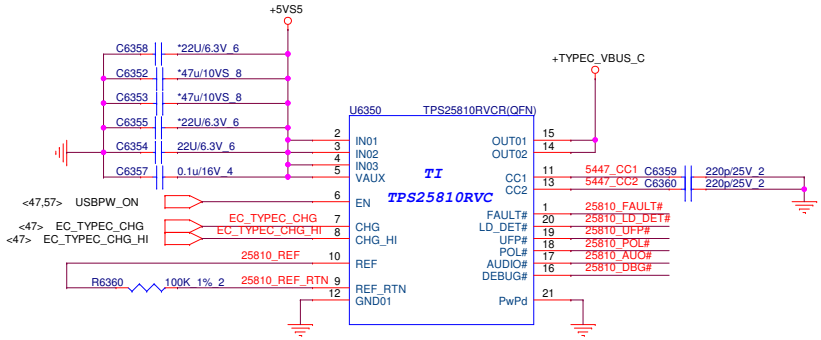

## CC/SBU Overvoltage protection

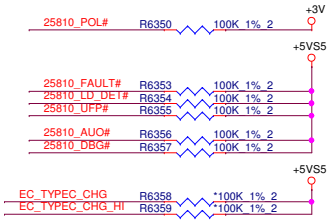



**Cost down -->TPD6S300ARUKR**
**P/N need to check ???**

AL06S300000 - IC OTHER (20P) TPD6S300RUKR (WQFN)
AL06S300002 - IC OTHER(20P)TPD6S300ARUKR(WQFN) --> use this one
AL170802006 - IC (20P) SN1708028RUKR (WQFN)
AL170802007 - IC (20P) SN1708028RUKR (WQFN) TOPBS --> mass production use this one

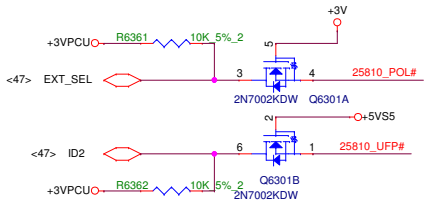
# BOM Note:



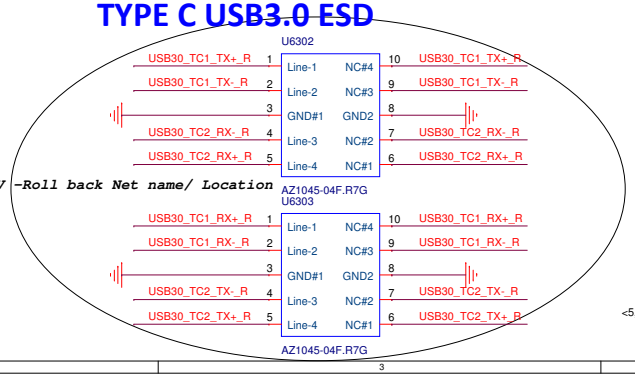




<64> 25810_UFP# 25810_UFP#

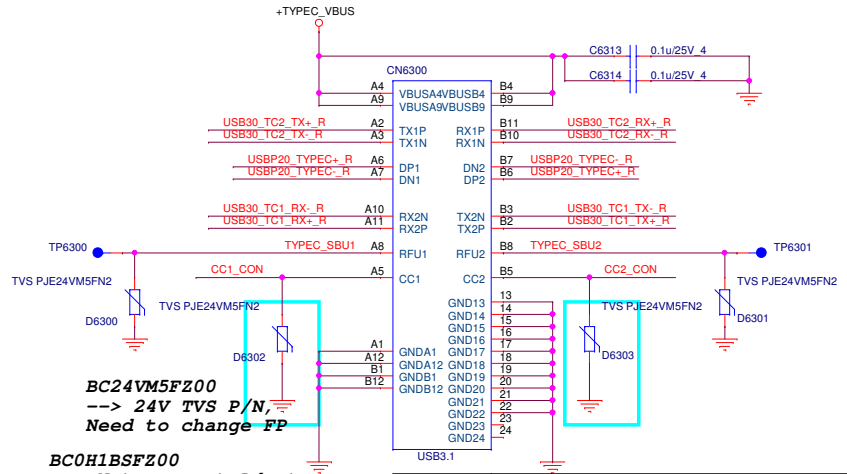
## Add Type-C A/B side recognization




## TYPE C USB3.0 ESD




**PV -Roll back Net name/ Location**



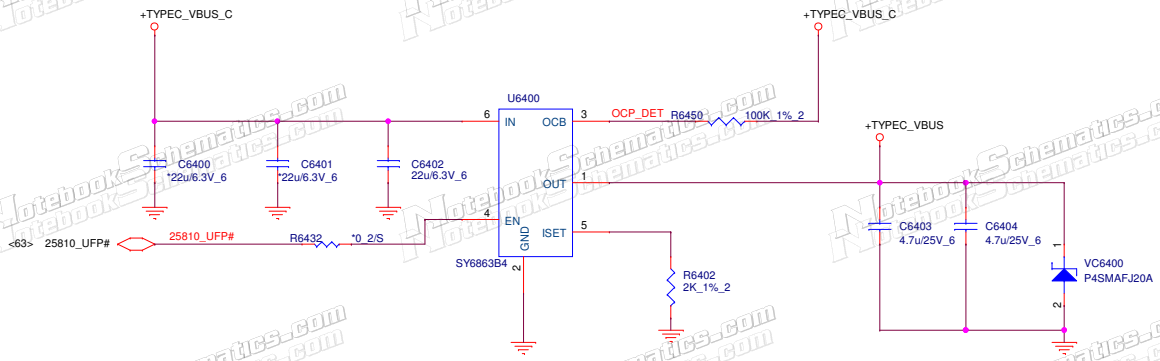

**BC24VM5FZ00**
**--> 24V TVS P/N,**
**Need to change FP**

**BC0H1BSFZ00**
**--> Not support Adapter**

# BOM Note:

<5,6,7,8,11,28,34,35,36,43,47,52,76,78,84,89> +3V
<8,57,78,84,86,89> +5VS5
<64> +TYPEC_VBUS

| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: TYPE-C TPS25810 | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 63 of 91 | |



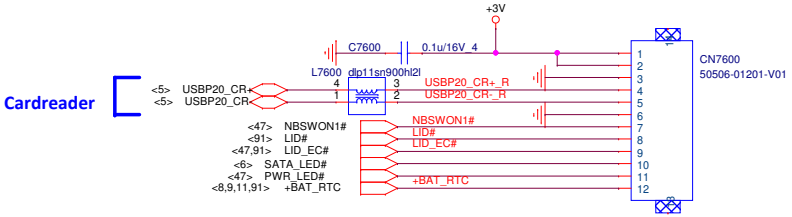



| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: TYPE-C Load Switch | Rev: 1A |
| Date: Tuesday, February 02, 2021 | Sheet 64 of 91 | |

# Daughter Board

## SD only

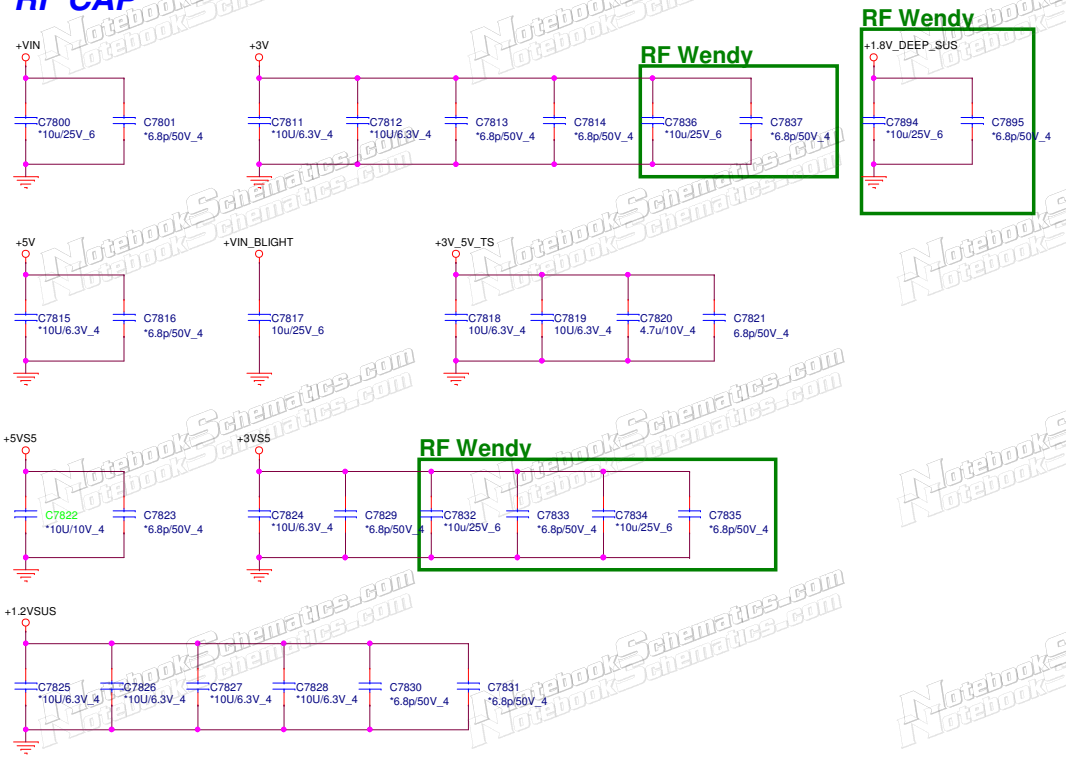
## Daughter Board



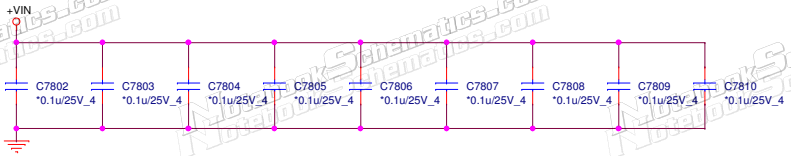

| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: Daughter Board | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 76 of 91 | |

# EMI Cap/RF Cap/HOLE

## RF CAP




## EMI CAP

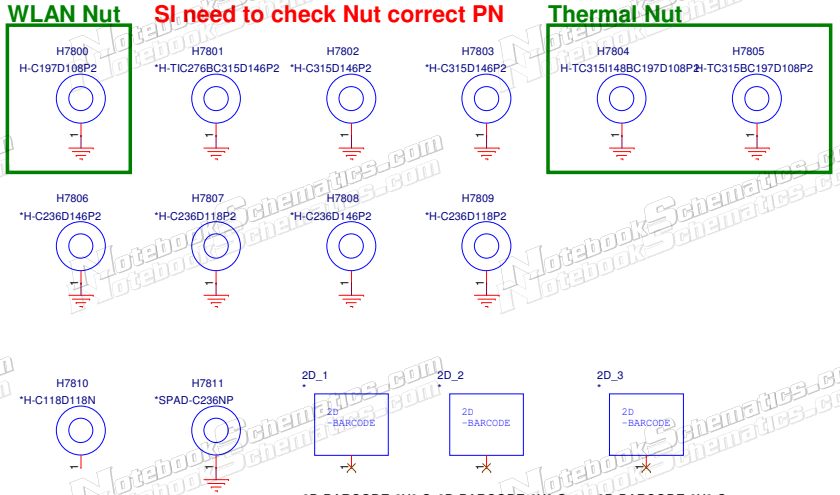



## HOLE

WLAN Nut

SI need to check Nut correct PN

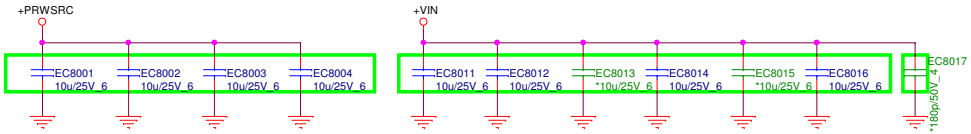
Thermal Nut




2D-BARCODE-8X8-S 2D-BARCODE-8X8-S 2D-BARCODE-8X8-S

| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: EMI Cap/RF Cap/HOLE | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 78 of 91 | |

# Reserve for EMI function test

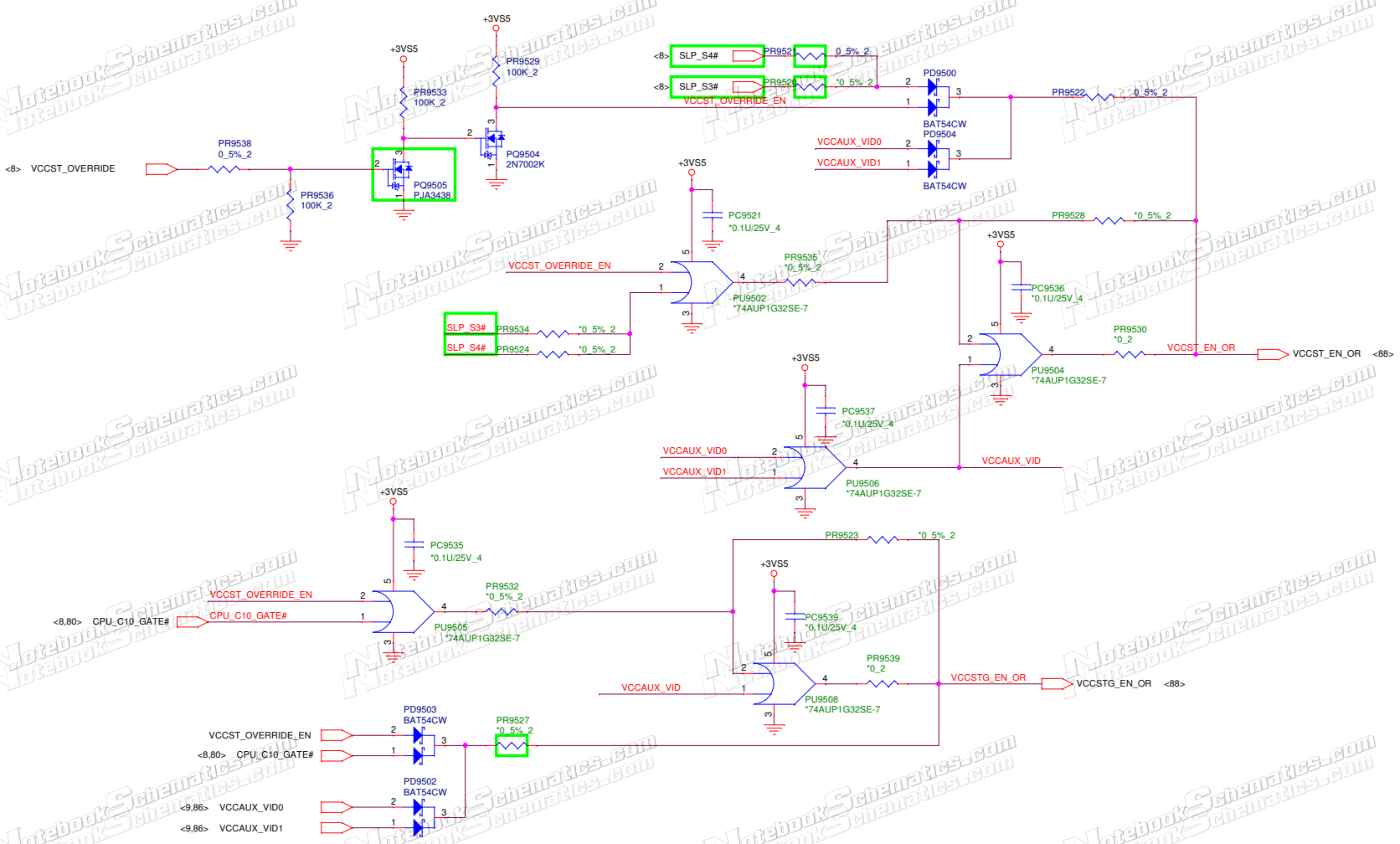



BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Power EMI | 1A |

Date: Wednesday, January 27, 2021 | Sheet 79 of 91

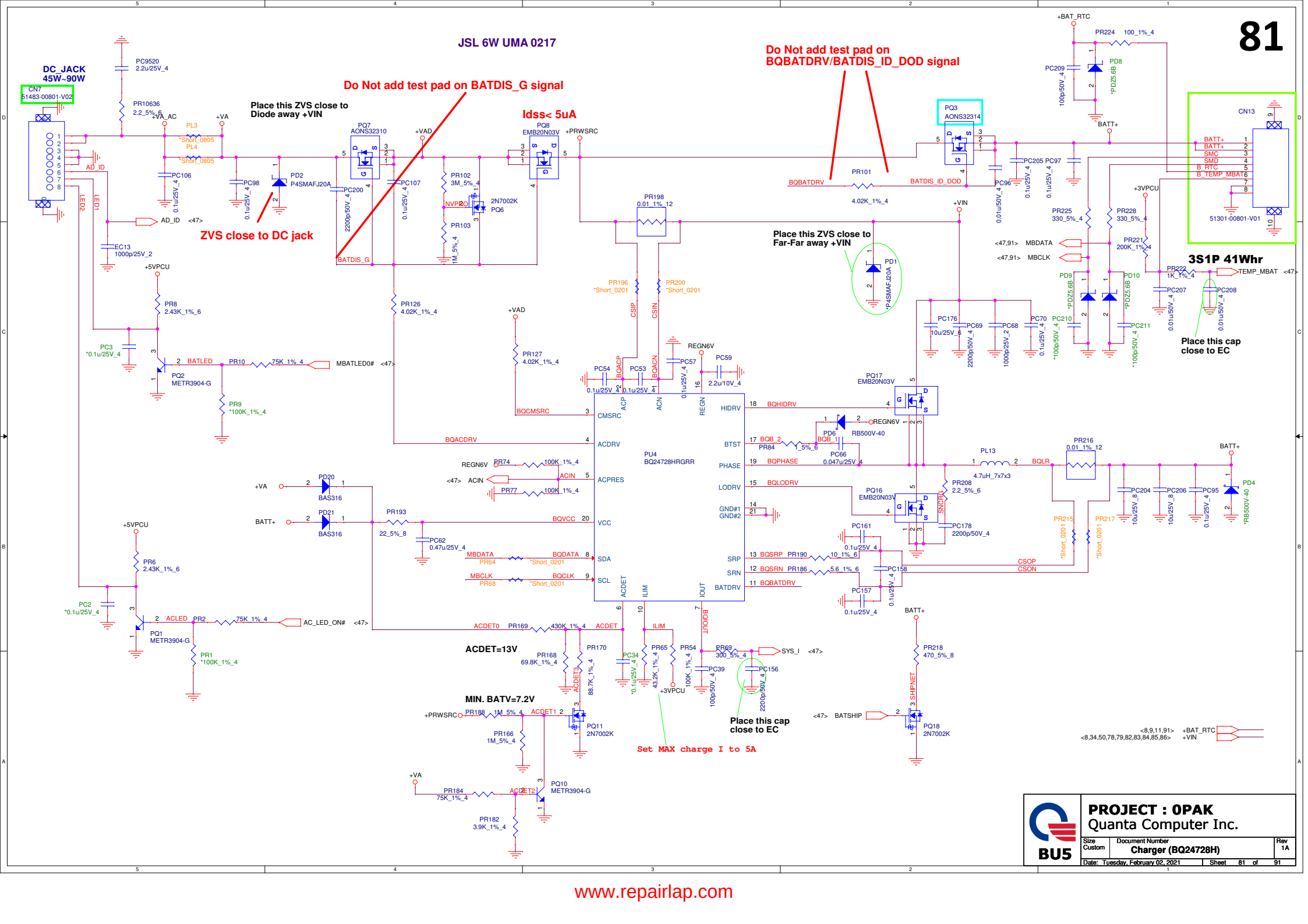


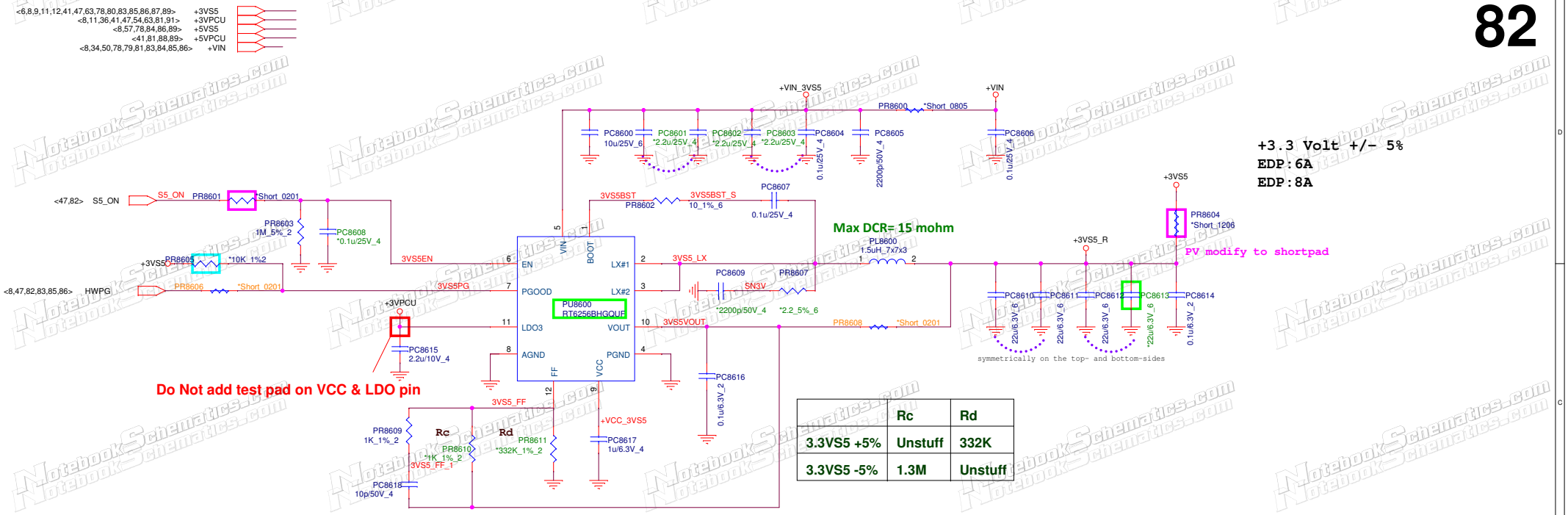

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Sequence CTRL | 1A |

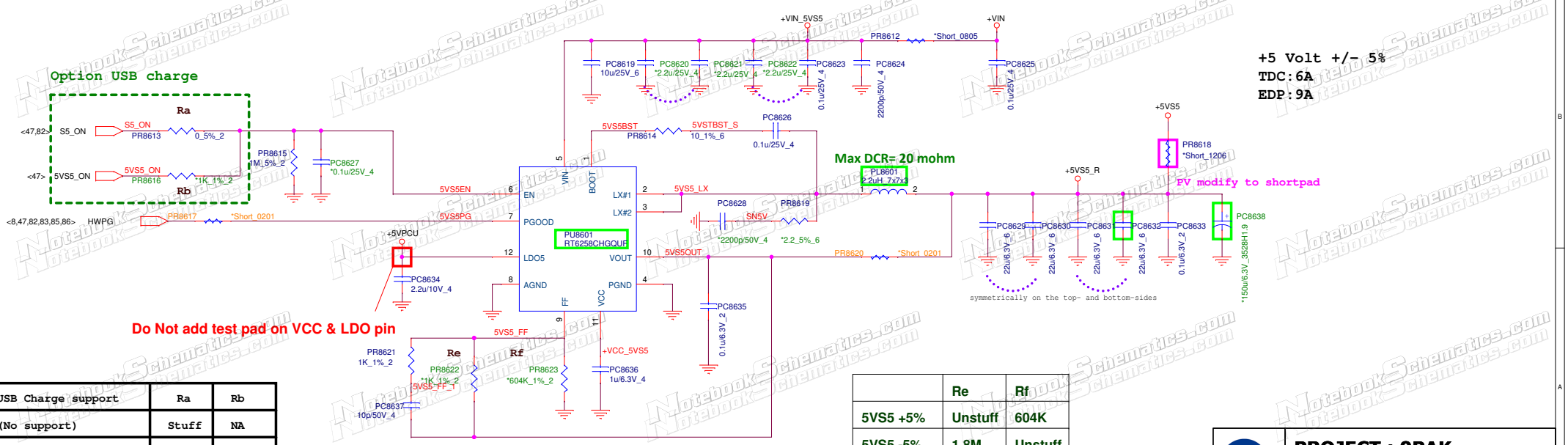
Date: Wednesday, January 27, 2021 Sheet 80 of 91

BU5


81
JSL 6W UMA 0217
DC_JACK
45W~90W
CN7
51483-00801-V02
Do Not add test pad on BATDIS_G signal
Idss< 5uA
Place this ZVS close to
Diode away +VIN
ZVS close to DC jack
Do Not add test pad on
BQBATDRV/BATDIS_ID_DOD signal
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
3S1P 41Whr
ACDET=13V
MIN. BATV=7.2V
Set MAX charge I to 5A
Place this cap
close to EC
PROJECT : 0PAK
Quanta Computer Inc.
BU5
Charger (BQ24728H)
Size Custom
Rev 1A
Date: Tuesday, February 02, 2021
Sheet 81 of 91
www.repairlap.com




| | Rc | Rd |
|---|---|---|
| 3.3VS5 +5% | Unstuff | 332K |
| 3.3VS5 -5% | 1.3M | Unstuff |




| | Re | Rf |
|---|---|---|
| 5VS5 +5% | Unstuff | 604K |
| 5VS5 -5% | 1.8M | Unstuff |

| USB Charge support | Ra | Rb |
|---|---|---|
| (No support) | Stuff | NA |
| (Support) | NA | Stuff |

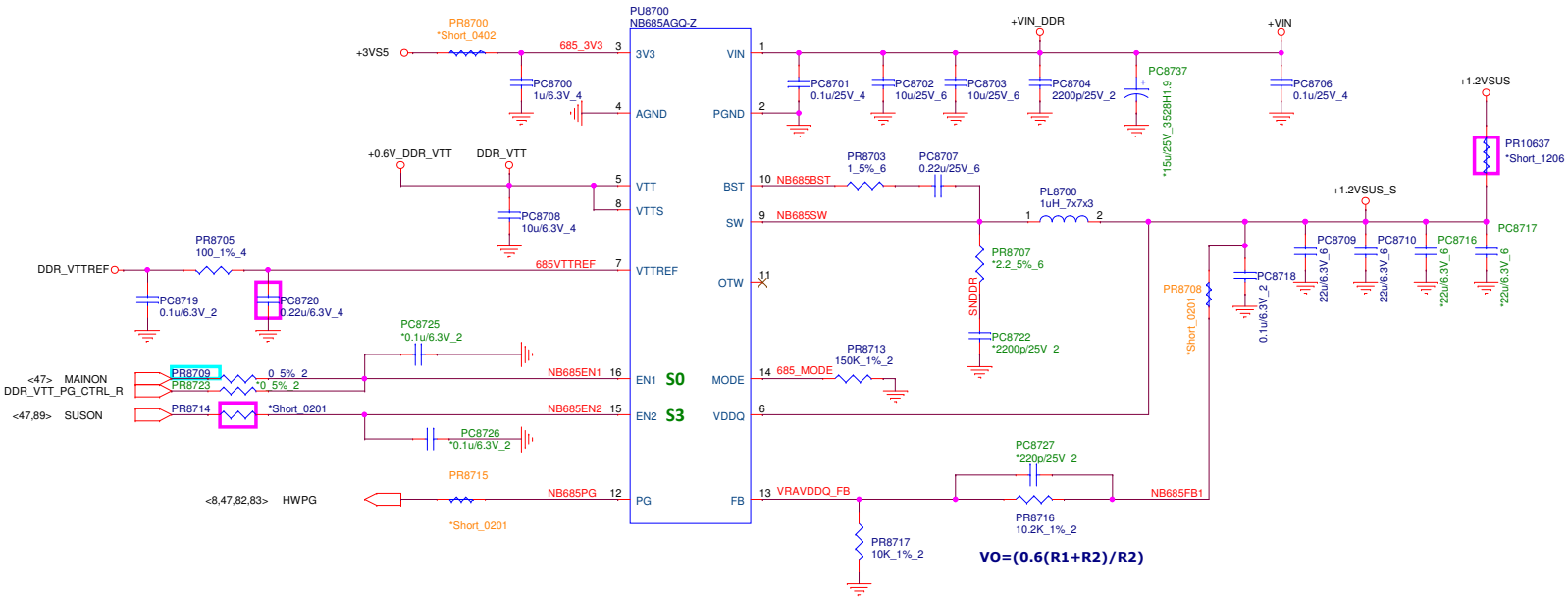
**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | 3/5VS5 - RT6316B/RT6318C | 1A |

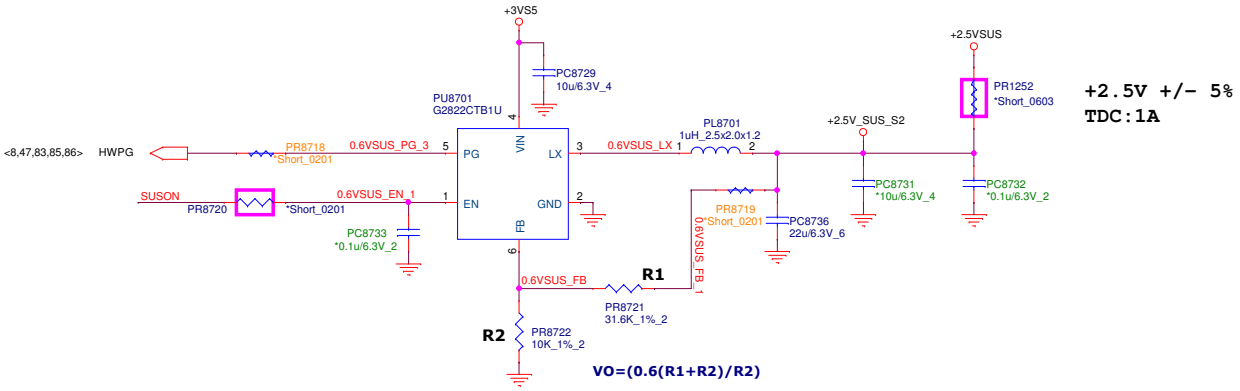
Date: Wednesday, January 27, 2021 Sheet 82 of 91

BU5

+1.2VSUS +/-5%
Continuous current: 8A
Peak current: 10A
OCP minimum: 12A



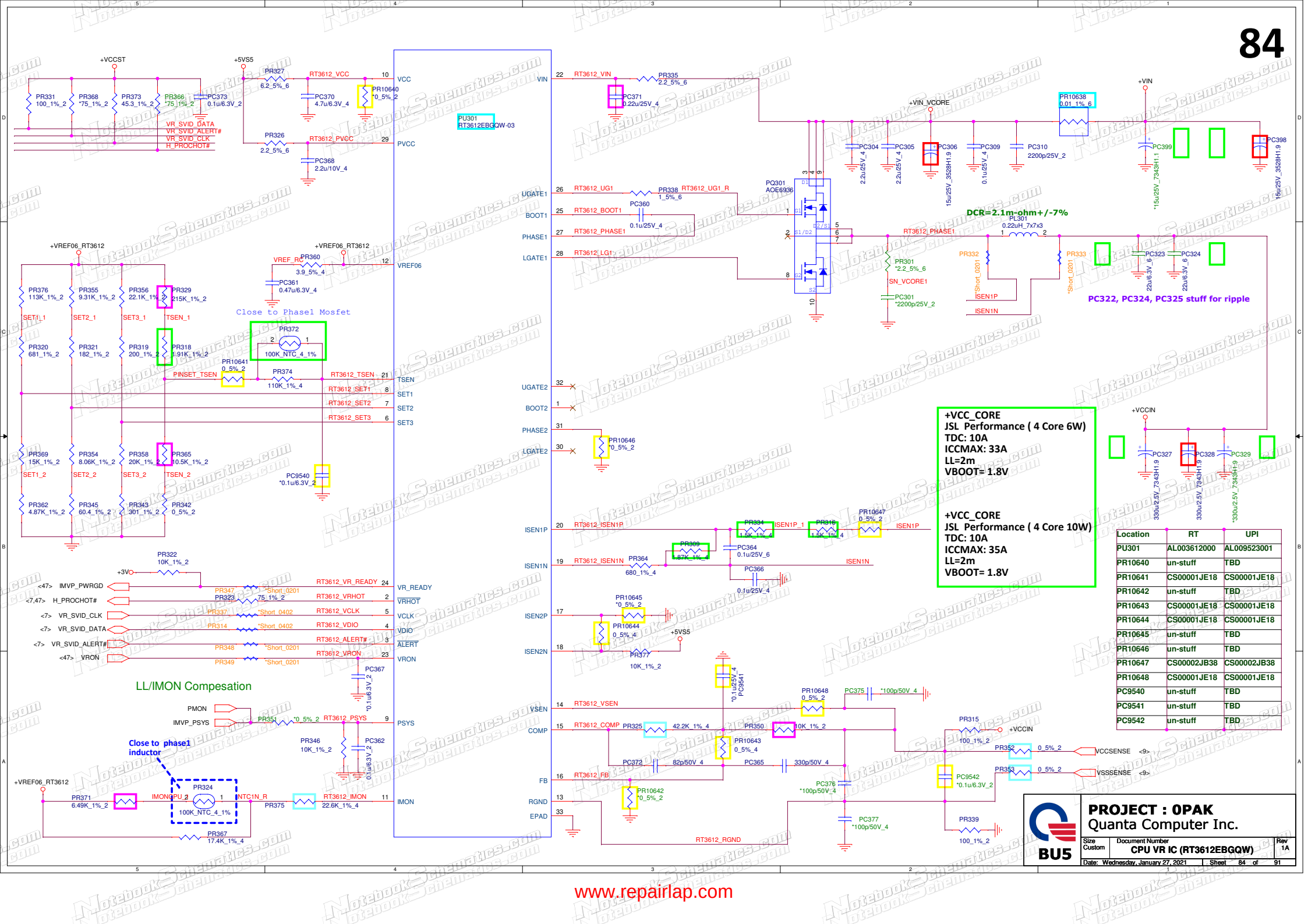

+2.5V +/- 5%
TDC:1A




**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR4 (NB685A) | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 83 of 91 | |

BU5

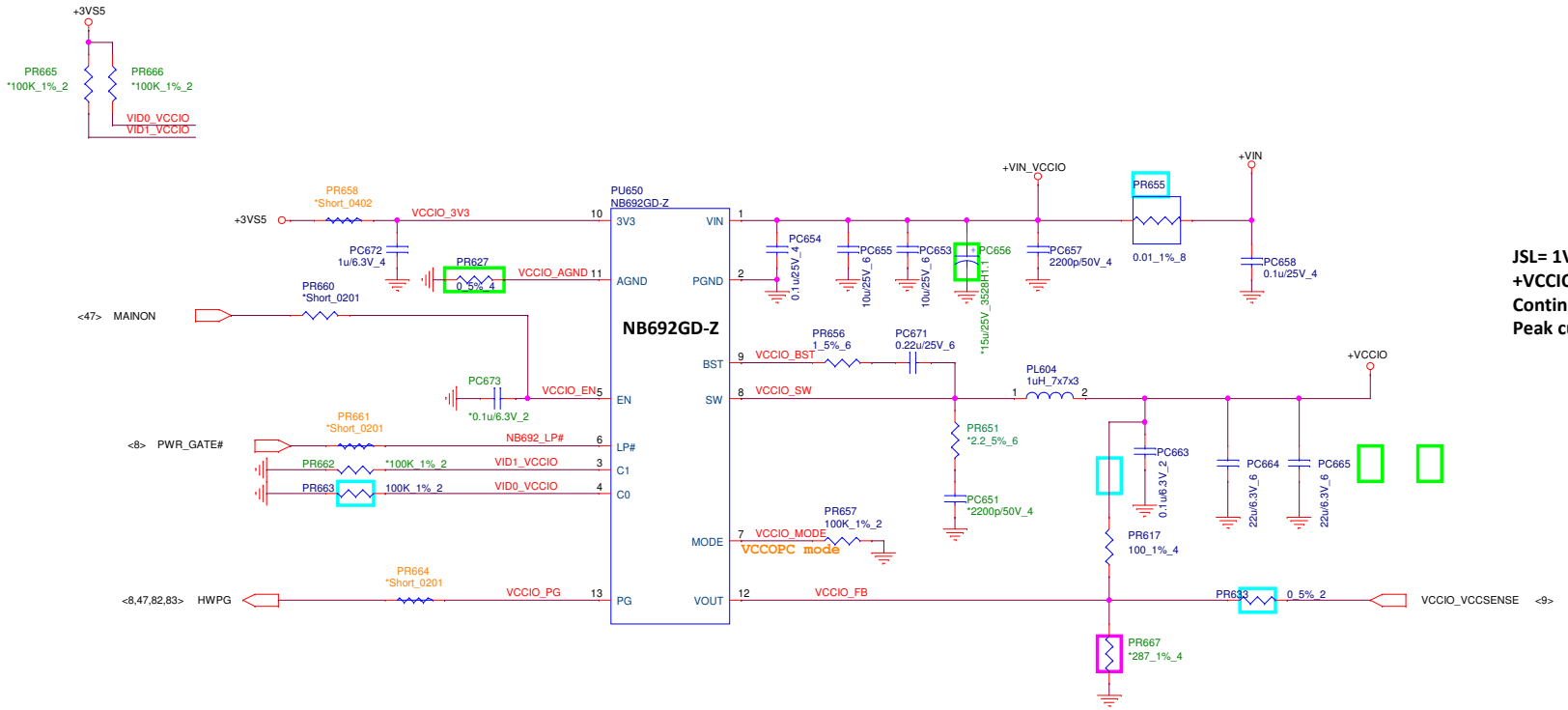



| Location | RT | UPI |
|---|---|---|
| PU301 | AL003612000 | AL009523001 |
| PR10640 | un-stuff | TBD |
| PR10641 | CS00001JE18 | CS00001JE18 |
| PR10642 | un-stuff | TBD |
| PR10643 | CS00001JE18 | CS00001JE18 |
| PR10644 | CS00001JE18 | CS00001JE18 |
| PR10645 | un-stuff | TBD |
| PR10646 | un-stuff | TBD |
| PR10647 | CS00002JB38 | CS00002JB38 |
| PR10648 | CS00001JE18 | CS00001JE18 |
| PC9540 | un-stuff | TBD |
| PC9541 | un-stuff | TBD |
| PC9542 | un-stuff | TBD |

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CPU VR IC (RT3612EBGQW) | 1A |

Date: Wednesday, January 27, 2021 Sheet 84 of 91

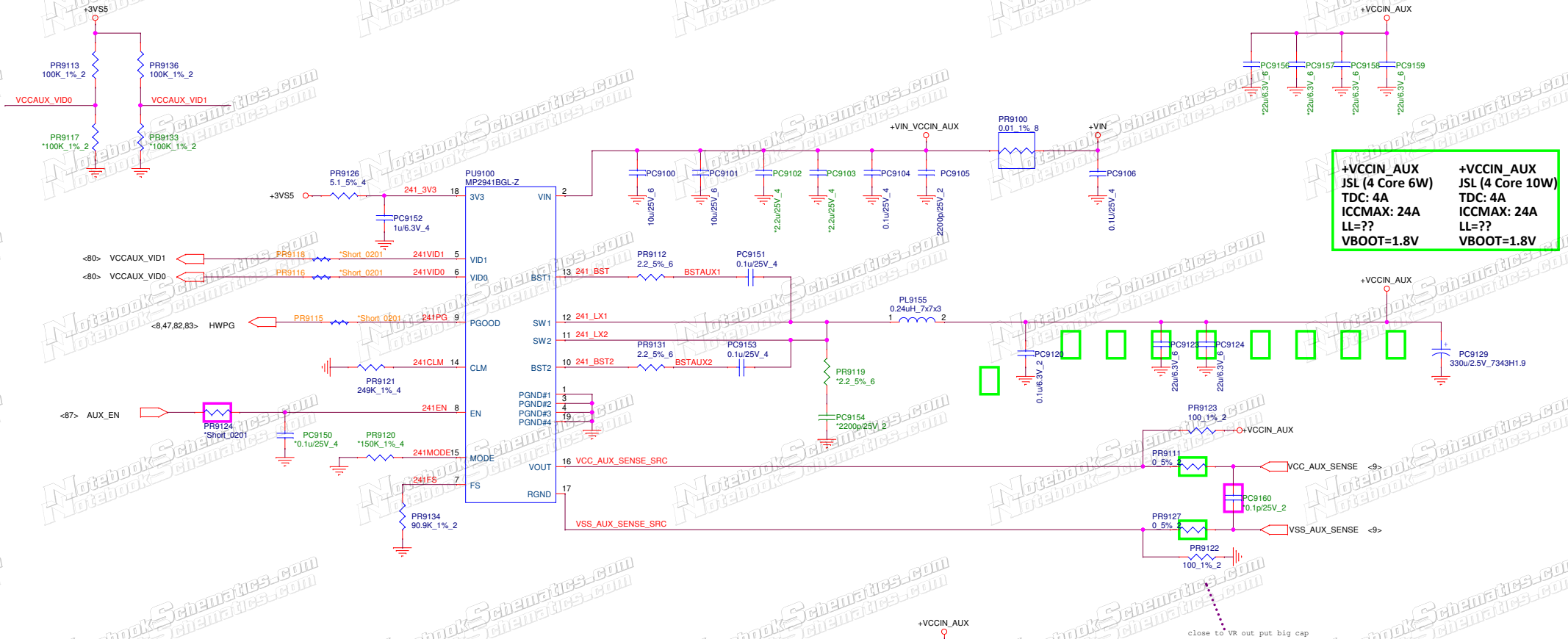



JSL= 1V/LPM=??V
+VCCIO +/-5%
Continuous current: ??A
Peak current: 5A

| VID0_PRIM | VID1_PRIM ( IC internal PU High) | LP# | PRIM |
|---|---|---|---|
| X | X | 0 | 0V |
| 0 | 0 | 1 | 0.8V |
| 0 | 1 | 1 | 1V |
| 1 | 1 | 1 | 1.05V |

Default setting

| | | | |
|---|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | | |
| Size: Custom | Document Number: VCCIO | | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 85 of 91 | | |



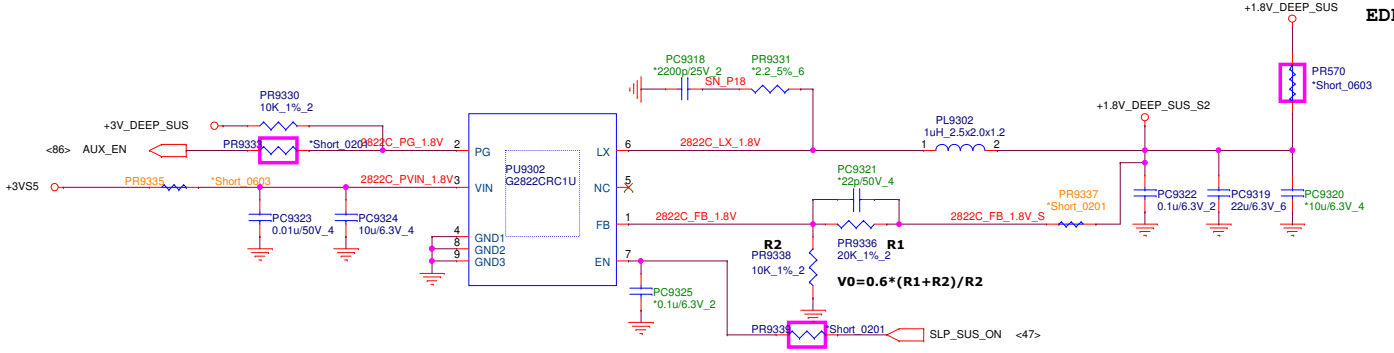

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | VCCIN_AUX IC (MP2941) | 1A |

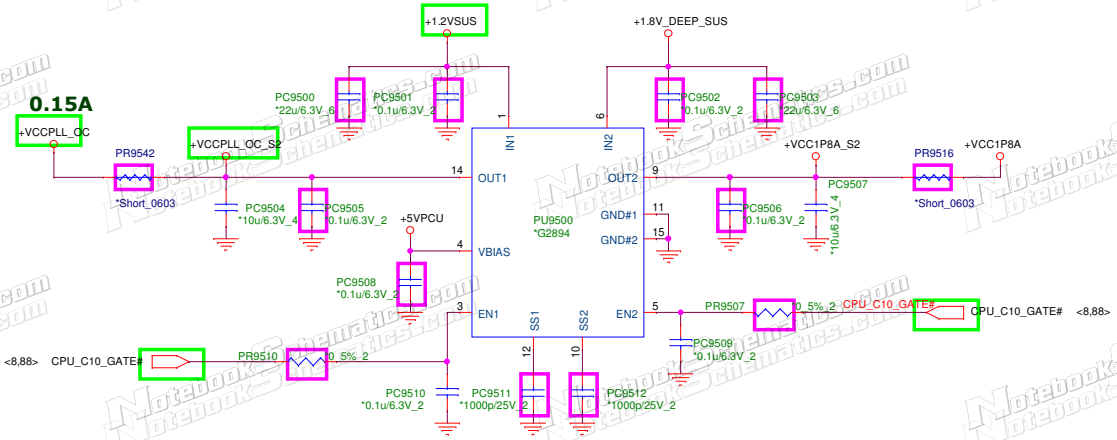
Date: Wednesday, January 27, 2021 Sheet 86 of 91

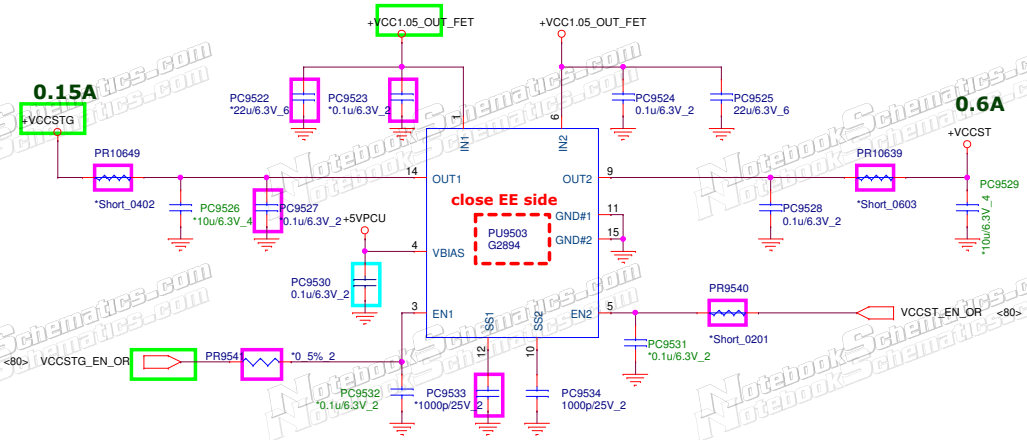
BU5

+1.8V_DEEP_SUS +/- 3%
TDC:2.24A
EDP:3.55A

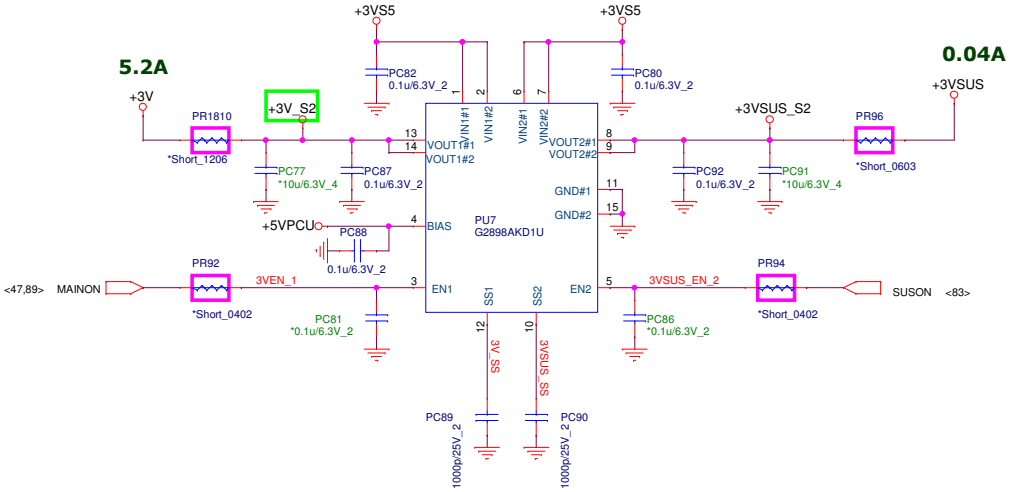


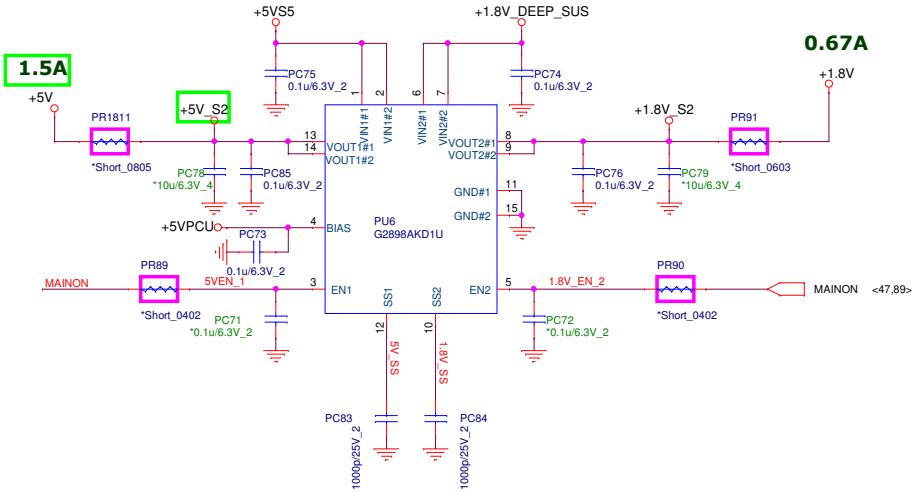

| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: +1.8V_DEEP_SUS | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 87 of 91 | |




| | | |
|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: VCCST\VCCPLL_OC\VCC1P8A | Rev: 1A |
| Date: Wednesday, January 27, 2021 | Sheet 88 of 91 | |

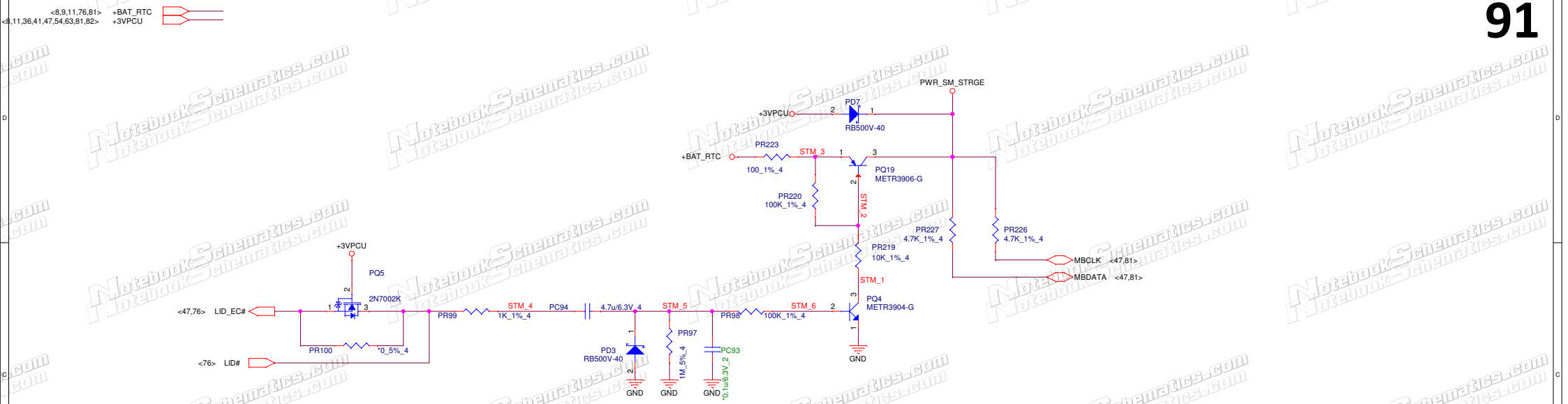



BU5

**PROJECT : 0PAK**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Load switch IC (G2898) | 1A |
| Date: Wednesday, January 27, 2021 | Sheet 89 of 91 | |




| | | | |
|---|---|---|---|
| BU5 | PROJECT : 0PAK<br>Quanta Computer Inc. | | |
| Size: Custom | Document Number: Storage Mode | | Rev: 1A |
| Date: Wednesday, January 27, 2021 | | Sheet 91 of 91 | |