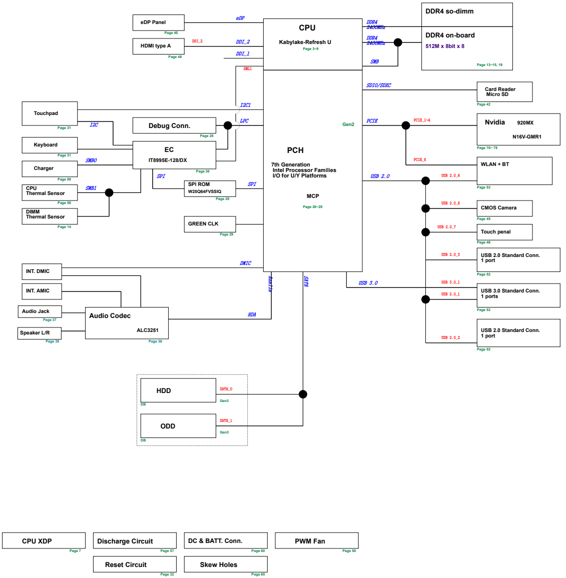
SYSTEM PAGE REF.

X540UV SCHEMATIC Revision 2.0

BLOCK DIAGRAM

Non Connected Standby



Power

- +VCCGT +VCCSA
- +VCCCORE
- +VCCST
  Page 80 & 81
- +1.0VSUS / +1.8VSUS
  Page 83
- +0.95VSG
- +VCCPRIM_CORE
  Page 84
- +1.2V / +VTT / +2.5V
  Page 86
- +3VADSW/+5VSUS
  Page 87
- Load Switch
  Page 88
- Charger
  Page 89
- +VDDC
  Page 91

ASUS	Project Name: X540UPR; Rev: R1.0
Title :	Block Diagram
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 1 of 102

PCH_CPT GPIO

Note	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	
	GPP_A0	Native1	RC_IN#		EXT PU 10K	+3VS	PU at EC
	GPP_A1	Native1	LPC_AD0				
	GPP_A2	Native1	LPC_AD1				
	GPP_A3	Native1	LPC_AD2				
	GPP_A4	Native1	LPC_AD3				
	GPP_A5	Native1	LPC_FRAME#				
	GPP_A6	Native1	INT_SERIRQ		EXT PU 10K	+3VS	
	GPP_A7	GPO	N/A				
	GPP_A8	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS	
	GPP_A9	Native1	CLK_KBCPCI_PCH				
	GPP_A10	Native	CLK_DEBUG				
For 555 N/A	GPP_A11	GPI	N/A	需確認是否具wake 功能			
	GPP_A12	GPO	N/A				
	GPP_A13	Native1	SUSWARN#		EXT PU 10K	+3VSUS	
	GPP_A14	Native1	PCH_SUS_STAT#				
Need Add EC	GPP_A15	Native1	PCH_SUSACK#				
For 555 N/A	GPP_A16	GPO	N/A (SD_1P8_SEL)				
For 555 N/A	GPP_A17	GPO	N/A (SD_PWR_EN#)				
	GPP_A18	GPO	N/A				
	GPP_A19	GPO	N/A				
	GPP_A20	GPO	N/A				
	GPP_A21	GPO	N/A				
	GPP_A22	GPO	N/A				
	GPP_A23	GPO	N/A				
For 555 N/A	GPP_B0	Native	N/A (VCCPRIM_VID0)		EXT PU 10K	+3VS	
For 555 N/A	GPP_B1	Native	N/A (VCCPRIM_VID1)		EXT PU 10K	+3VS	
	GPP_B2	GPO	N/A				
	GPP_B3	GPO	N/A				
	GPP_B4	GPO	N/A				
	GPP_B5	Native	CK_REQ_P0# DGPU		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B6	Native	CK_REQ_P1#		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B7	Native	CK_REQ_P2#		EXT PU 10K	+3VS	
	GPP_B8	Native	CK_REQ_P3#		EXT PU 10K	+3VS	
	GPP_B9	Native	CK_REQ_P4# GLAN		EXT PU 10K	+3VS	
	GPP_B10	Native	CK_REQ_P5# WLAN		EXT PU 10K	+3VS	
	GPP_B11	Native	MPHY_PWREN (N/A)		EXT PU 20K	+3VSUS	
	GPP_B12	Native	PCH_SLP_S0#				
	GPP_B13	Native	PLT_RST#				
	GPP_B14	GPO	PCH_GPPB14				
For 555 N/A	GPP_B15	GPO	N/A (GSPI0_CS_R#)				
For 555 N/A	GPP_B16	GPO	N/A (GSPI0_CLK_R)				
For 555 N/A	GPP_B17	GPO	N/A (GSPI0_MISO_R)				
	GPP_B18	GPO	N/A (PCH_GPPB18)				
	GPP_B19	GPO	BT_ON/OFF#				
	GPP_B20	GPO	GPU_EVENT#		EXT PU 10K	+3VSG	
	GPP_B21	GPI	DGPU_FB_CLAMP_GPIO		EXT PD 10K	PU at DGPU	
	GPP_B22	GPO	PCH_GPPB22				
	GPP_B23	Native	SML1ALERT#		EXT PU 150K	+3VSUS	
	GPP_C0	Native	SMB_CK		EXT PU 2.2K	+3VSUS	
	GPP_C1	Native	SMB_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C2	GPO	GPP_C2				
For 555 N/A	GPP_C3	Native	SML0_CK		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C4	Native	SML0_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C5	GPO	GPP_C5				
	GPP_C6	Native	SML1_CK		EXT PU 2.2K	+3VSUS	
	GPP_C7	Native	SML1_DATA		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C8	GPO	N/A (PCH_GPPC8)				
For 555 N/A	GPP_C9	GPO	N/A (PCH_GPPC9)				
For 555 N/A	GPP_C10	GPO	N/A (PCH_GPPC10)				
For 555 N/A	GPP_C11	GPO	N/A (PCH_GPPC11)				
	GPP_C12	GPI	DIMM_SEL0		EXT PU 10K	+3VSUS	
	GPP_C13	GPI	DIMM_SEL1		EXT PU 10K	+3VSUS	
	GPP_C14	GPI	DIMM_SEL2	UART1_RTS#	EXT PU 10K	+3VSUS	
	GPP_C15	GPI	N/A	UART1_CTS#			
	GPP_C16	GPO	AOAC_WLANLED(N/A)				
For 555 N/A	GPP_C17	GPO	N/A (ALS_INT#)				
For X541UV N/A	GPP_C18	Native	I2C1_SDA_TCH_PAD		PU 4.7K	+3VSUS	
For X541UV N/A	GPP_C19	Native	I2C1_SCL_TCH_PAD		PU 4.7K	+3VSUS	
	GPP_C20	GPI	DGPU_PWROK		EXT PU 10K	+3VSG	PU at DGPU
	GPP_C21	GPO	GPU_RST#		EXT PU 10K	+3VS	
	GPP_C22	GPO	DGPU_PWR_EN#		EXT PU 10K	+3VSUS	
	GPP_C23	GPI	TPanel_INT#		EXT PU 10K	+3VS	
	GPP_D0	GPO	N/A				
	GPP_D1	GPO	N/A				
	GPP_D2	GPO	N/A				
	GPP_D3	GPO	N/A				
For 555 N/A	GPP_D4	GPI	GPIO_SMI_ASM1142(N/A)				
	GPP_D5	GPO	SATA_ODD_PWRGT		EXT PU 10K	+3VS	
	GPP_D6	GPI	SATA_ODD_DA#		EXT PU 10K	+3VS	
	GPP_D7	GPO	N/A				
	GPP_D8	GPO	N/A				
	GPP_D9	GPI	PCB_ID0		EXT PD 10K		
For X541UV N/A	GPP_D10	GPI	DMIC_ID		EXT PD 10K		
	GPP_D11	GPI	TOUCHPAD_ID		EXT PD 10K		
	GPP_D12	GPI	TOUCH_PANEL_ID		EXT PD 10K		
	GPP_D13	GPI	TOUCHPAD_INTR#		EXT PU 10K	+3VS	
	GPP_D14	GPO	WLAN_LED_R				
X541UV Change	GPP_D15	GPO	SNSR_HUB_PWREN				
	GPP_D16	GPO	N/A	UART0_CTS#			
	GPP_D17	GPO	N/A				
	GPP_D18	GPO	N/A				
For 555 N/A	GPP_D19	GPO	(N/A) DMIC_CLK_PCH				
For 555 N/A	GPP_D20	GPO	(N/A) DMIC_DATA_PCH				
	GPP_D21	GPO	N/A				
	GPP_D22	GPO	N/A				

Note	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	
	GPP_D23	GPO	N/A				
	GPP_E0	GPI	DIRECT_ESATA_DETECT_R#		EXT PU 10K	+3VS	
	GPP_E1	GPI	SATA_ODD_PRSNT_R#		EXT PU 10K	+3VS	
	GPP_E2	GPI	MSATA_MPCIE_DET#		EXT PU 10K	+3VS	
	GPP_E3	GPO	N/A				
	GPP_E4	GPO	SATA0_DEVSLP				
	GPP_E5	GPO	SATA1_PHYSLP_DIRECT				
	GPP_E6	GPO	SATA2_DEVSLP				
	GPP_E7	GPO	N/A				
	GPP_E8	NATIVE	PCH_SATA_LED#		EXT PU 10K	+3VS	
	GPP_E9	NATIVE	USB_OC_1_2#_R		EXT PU 10K	+3VSUS	
	GPP_E10	GPI	USB_OC_3_4#		EXT PU 10K	+3VSUS	
	GPP_E11	GPI	USB_OC_5_6#		EXT PU 10K	+3VSUS	
	GPP_E12	GPI	USB_OC_7_8#		EXT PU 10K	+3VSUS	
	GPP_E13	NATIVE	DDPB_HPD_PCH		EXT PD 100K	PD at IC of eDP to VGA	
	GPP_E14	NATIVE	HDMI_HP		EXT PU 1M	+3VS	PD at HDMI conn
	GPP_E15	GPO	EXT_SMI#		EXT PU 10K	+3VS	
	GPP_E16	GPI	EXT_SCI#		EXT PU 10K	+3VS	
	GPP_E17	NATIVE	EDP_HPD_CON			PD at LVDS conn	
	GPP_E18	NATIVE	DDPB_SCL_PCH				
	GPP_E19	NATIVE	DDPB_SDA_PCH		EXT PU 10K	+3VS	
	GPP_E20	NATIVE	DDPC_SCL_PCH		EXT PU 2.2K	+3VS	PU at HDMI conn
	GPP_E21	NATIVE	DDPC_SDA_PCH		EXT PU 2.2K	+3VS	PU at HDMI conn
	GPP_E22	GPO	N/A				
	GPP_E23	GPO	N/A				
	GPP_F0	GPO	N/A				
	GPP_F1	GPO	N/A				
	GPP_F2	GPO	N/A				
	GPP_F3	GPO	N/A				
	GPP_F4	GPO	N/A				
	GPP_F5	GPO	N/A				
	GPP_F6	GPO	N/A				
	GPP_F7	GPO	N/A				
	GPP_F8	GPO	N/A				
	GPP_F9	GPO	N/A				
	GPP_F10	GPO	N/A				
	GPP_F11	GPO	N/A				
	GPP_F12	GPO	N/A				
	GPP_F13	GPO	N/A				
	GPP_F14	GPO	N/A				
	GPP_F15	GPO	N/A				
	GPP_F16	GPO	N/A				
	GPP_F17	GPO	N/A				
	GPP_F18	GPO	N/A				
	GPP_F19	GPO	N/A				
	GPP_F20	GPO	N/A				
	GPP_F21	GPO	N/A				
	GPP_F22	GPO	N/A				
	GPP_F23	GPO	N/A				
For 555 N/A	GPP_G0	GPO	N/A (SDIO_CMD)				
For 555 N/A	GPP_G1	GPO	N/A (SDIO_D0)				
For 555 N/A	GPP_G2	GPO	N/A (SDIO_D1)				
For 555 N/A	GPP_G3	GPO	N/A (SDIO_D2)				
For 555 N/A	GPP_G4	GPO	N/A (SDIO_D3)				
For 555 N/A	GPP_G5	GPO	N/A (SDIO_CD#)				
For 555 N/A	GPP_G6	GPO	N/A (SDIO_CLK)				
For 555 N/A	GPP_G7	GPO	N/A (SDIO_WP)				
For 555 ADD	GPD0	Native	PM_BATLOW_R#		EXT PU 8.2K	+3VA_DSW	
	GPD1	Native	ME_AC_PRESENT_PCH		EXT PU 100K	+3VA_DSW	
	GPD2	GPI	PCH_GPD2#		EXT PU 10K	+3VA_DSW	
	GPD3	Native	PM_PWRBTN#				
	GPD4	Native	PM_SUSB#		EXT PD 100K	PD at EC	
	GPD5	Native	PM_SUSC#		EXT PD 100K	PD at EC	
For 555 ADD	GPD6	Native	PM_SLP_A_R#				
	GPD7	GPO	WLAN_ON#				
For 555 N/A	GPD8	Native	NA (SUS_CK)		EXT PD 1K		
	GPD9	Native	PCH_SLP_WLAN# (N/A)				
	GPD10	Native	SLP_S5# (N/A)				
	GPD11	Native	LAN_PWREN (N/A)				VC lose

EC IT8995 GPIO

Note	Pin Name	Config	Signal Name	Default status	Ext Pull up / down	Power
	GPA0	O	PWR_LED	LOW		
	GPA1	OD	CHG_LED#	HIGH	EXT 10K PU	+3VA_EC
	GPA2	OD	CHG_FULL_LED#	HIGH	EXT 10K PU	+3VA_EC
For 555 N/A	GPA3	Alt	EC_GPA3	LOW		
For 555 N/A	GPA4	O	EC_GPA4	LOW	EXT 10K PU	+3VA_EC
	GPA5	Alt	FAN0_PWM	LOW		
	GPA6	Alt	KB_LED_PWM	LOW		
For 555 N/A	GPA7	O	EC_GPA7 (N/A)	HIGH		
	GPB0	Alt	AC_IN_OC#	HIGH	EXT 10K PU	+3VA
	GPB1	I	LID_SW#	HIGH	EXT 10K PU	+3VA
For 555 N/A	GPB2	OD	(N/A)	LOW	EXT 10K PU	+3VA_EC
	GPB3	I	PWR_SW#	HIGH	EXT 10K PU	+3VA
	GPB4	O	PS_ON	HIGH		
For 555 N/A	GPB5	O	A20GATE (N/A)	LOW	EXT 10K PU	+3VS
	GPB6	OD	RC_IN#	HIGH	EXT 10K PU	+3VS
For 555 N/A	GPC0	O	(N/A)	LOW		
	GPC1	Alt	SMB1_CLK	LOW	EXT 4.7K PU	+3VA_EC
	GPC2	Alt	SMB1_DAT	LOW	EXT 4.7K PU	+3VA_EC
	GPC3	O	PM_PWRBTN#	HIGH		
For 555 N/A	GPC4	I	EC_GPC4 (N/A)	LOW	EXT 10K PU	+3VS
	GPC5	I	PM_SUSC#	HIGH	EXT 100K PD	
	GPC6	Alt	BAT1_IN_OC#	HIGH	EXT 10K PD	
For 555 N/A	GPC7	I	(N/A)	LOW		
	GPD0	I	PCH_SLP_S0#	HIGH		
	GPD1	O	ME_AC_PRESENT	LOW	EXT 100K PU	+3VA_DSW
	GPD2	Alt	BUF_PLT_RST#	HIGH	EXT 100K PD	
	GPD3	OD	EXT_SCI#	HIGH	EXT 10K PU	+3VS
	GPD4	OD	EXT_SMI#	HIGH	EXT 10K PU	+3VS
	GPD5	O	OP_SD#	HIGH		
	GPD6	Alt	FAN0_TACH	LOW	EXT 10K PU	+3VS
For 555 N/A	GPD7	Alt	(N/A)	LOW	EXT 10K PU	+3VS
	GPE0	O	SUSB_EC#	HIGH	EXT 10K PD	
	GPE1	O	SUSC_EC#	HIGH	EXT 10K PD	
	GPE2	O	1.2V_ON	LOW		
	GPE3	O	N/A	HIGH		
For 555 N/A	GPE4	O	(N/A)	HIGH		
	GPE5	I	PM_SUSB#	LOW	EXT 100K PD	
For 555 N/A	GPE6	OD	CAP_LED#	HIGH		
	GPE7	OD	THRO_CPU#	HIGH	EXT 1K PU	+VCCSTG
	GPF0	O	5VSUS_ON	LOW	EXT 10K PU/ 1M PD	+3VA_EC
	GPF1	O	VSUS_ON	LOW	EXT 100K PU	+3VA_EC
	GPF2	Alt	SMB0_CLK	HIGH	EXT 4.7K PU	+3VA_EC
	GPF3	Alt	SMB0_DATA	HIGH	EXT 4.7K PU	+3VA_EC
	GPF4	Alt	TP_CLK	HIGH	EXT 4.7K PU	+3VS
	GPF5	Alt	TP_DAT	HIGH	EXT 4.7K PU	+3VS
	GPF6	Alt	PECI_EC	LOW		
	GPF7	O	PCH_SPI_OV	LOW		
	GPG0	O	DGPU_LIMIT	LOW		
	GPG1	O	PCH_SUSACK#	HIGH		
	GPG2	I	PWRLIMIT_EC#	HIGH	EXT 100K PU	+3VA_EC
For 555 N/A	GPG6	O	(N/A)	LOW		
	GPH0	Alt	PM_CLKRUN#	HIGH	EXT 8.2K PU	+3VS
For 555 N/A	GPH1	Alt	SMB3_CLK N/A	HIGH		
For 555 N/A	GPH2	Alt	SMB3_DAT N/A	HIGH		
	GPH3	O	PM_RSMRST#	HIGH	EXT 10K PD	
	GPH4	O	DPWROK_EC	LOW	EXT 10K PD	
	GPH5	O	PM_PWROK	LOW	EXT 100K PD	
	GPH6	O	PM_SYSPWROK	LOW	EXT 10K PD	
	GPH7	O	LCD_BACKOFF#	HIGH		
	GPI0	I	PM_SLP_SUS#	HIGH	EXT 10K PU/ 100K PD	+3VA_EC
	GPI1	I	3VSUS_PWRGD	LOW		
	GPI2	I	ALL_SYSTEM_PWRGD	LOW	EXT 10K PU	+3VS
	GPI3	I	IMVP8_PWRGD	LOW	EXT 10K PU	+3VS
	GPI4	I	3VA_DSW_PWRGD	LOW	EXT 100K PU	+3VA_DSW
	GPI5	I	ME_SusPwrDnAck_EC	LOW		
	GPI6	Alt	A/D_MAX_POWER	LOW	EXT 0 PD	
	GPI7	Alt	MB_MAX_POWER	LOW	EXT 100K PU/93.1K PD	+3VACC
	GPJ0	I	EC_WAKE_SCI	LOW		
	GPJ1	O	3VADSW_ON	LOW	EXT 100K PU	+3VA_EC
For 555 N/A	GPJ2	Alt	PL_REF_EC N/A	LOW		
	GPJ3	O	WLAN_PWR_EN	LOW		
For 555 N/A	GPJ4	Alt	IBAT_REF_EC N/A	LOW		
For 555 N/A	GPJ5	I	EC_GPJ5	LOW		
For 555 N/A	GPJ6	I	N/A	LOW		+3VS
For 555 N/A	GPJ7	O	N/A	HIGH		

*1: EC config GPI; Function output

Design IP Source:

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
EC Master (SMB1)	SM-Bus Address	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

USB3 Port

USB3_1	USB 3.0 Port 0
USB3_2	USB 3.0 Port 1
USB3_3	USB 3.0 Port 2
USB3_4	

PCI Express

PCIE 1	DGPU
PCIE 2	
PCIE 3	
PCIE 4	
PCIE 5	GLAN
PCIE 6	WLAN
PCIE 9	
PCIE 10	
PCIE 11	
PCIE 12	

SATA Port

SATA 0	HDD
SATA 1	ODD / 2nd HDD

PCI CLK

CLK0	DGPUx4
CLK1	
CLK2	
CLK3	
CLK4	LAN
CLK5	WLAN

USB Port

USB 1	USB 2.0 Port
USB 2	USB 2.0 Port
USB 3	USB 2.0 Port
USB 4	
USB 5	
USB 6	CAMERA
USB 7	TOUCH_PANEL
USB 8	WLAN/BT
USB 9	
USB 10	

USB 3.0 Port 0
USB 3.0 Port 1
USB 3.0 Port 2

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

For X540UPR ADD

BOM

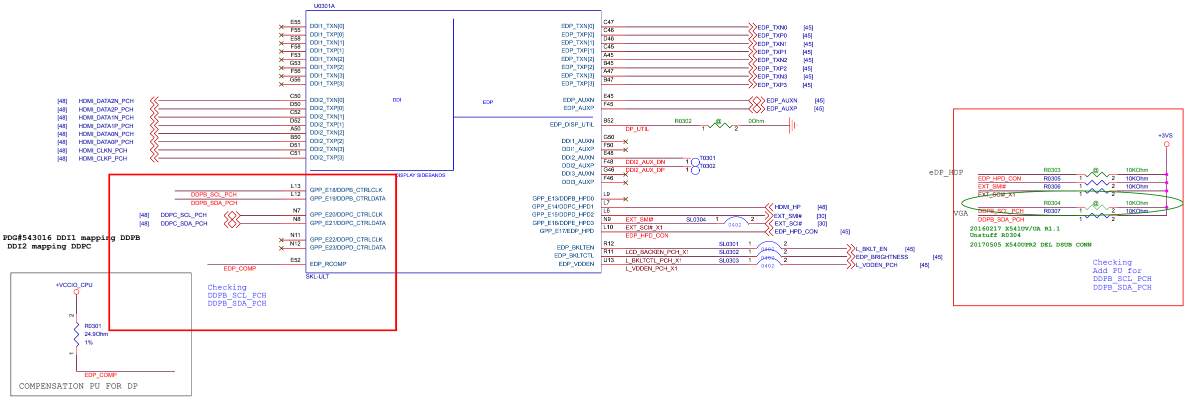
Project Name: X540UPR			Rev: R1.0
Title : System Setting			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE	
Date: Monday, August 21, 2017		Sheet 2 of 102	

Main Board

Display Port

A	EDP
B	VGA
C	HDMI

Intel Version	ASUS P/N
pre-ES	



BOM

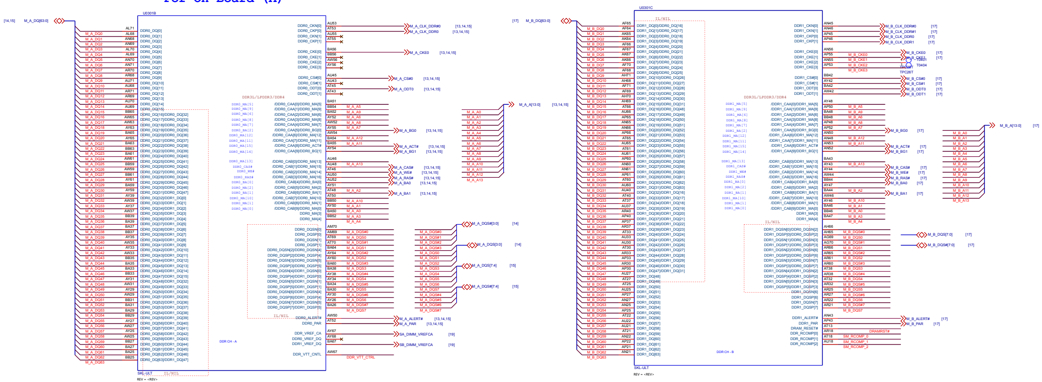
ASUS	Project Name: X540UPR	Rev: R1.0
Title : CPU_DISPLAY		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 3	of 102

Main Board

512M x 8bit x 8

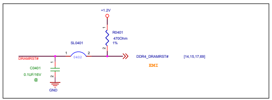
For On Board (A)

For SO-DIMM (B)

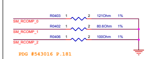


DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

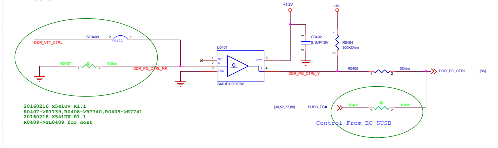
DDR0_Vref_DQ = Not in use in DDR4,
DDR1_Vref_DQ = DDR4_CA_ch1,
DDR_Vref_CA = DD4_CA_ch0



DDR4 COMPENSATION SIGNALS



VTT Enable

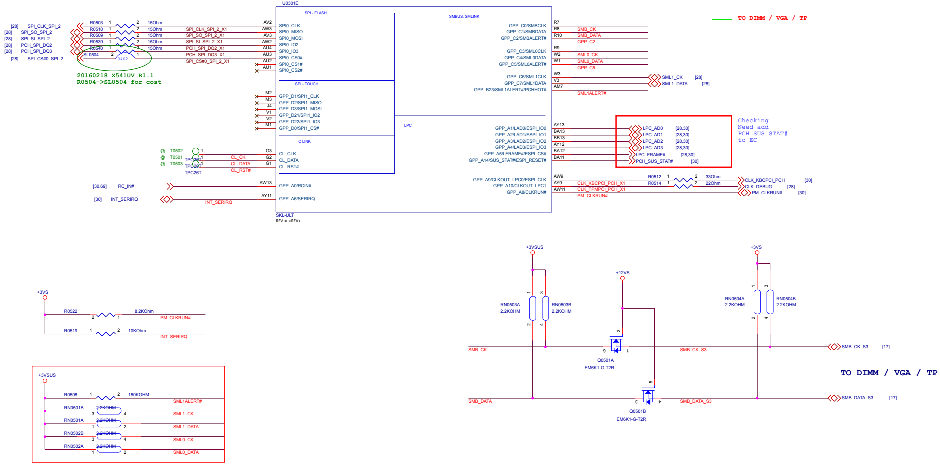


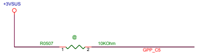
20160216 X541UV R1.1
R0407->R7739,R0408->R7740,R0409->R7741
20160218 X541UV R1.1
R0409->SL0409 for cost

Table 4-44. KBL U DDR4 x8 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max (mils) Length			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group[1&2]	Byte [1&2]	Region	Breakout	Total		
RCOMP[0]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	121	
RCOMP[1]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	80.6	
RCOMP[2]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	100	

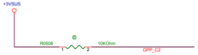
Main Board





GPP_C5: weak internal pull down	
PU	SPI BUS
PD	LPC is selected for EC (Default)

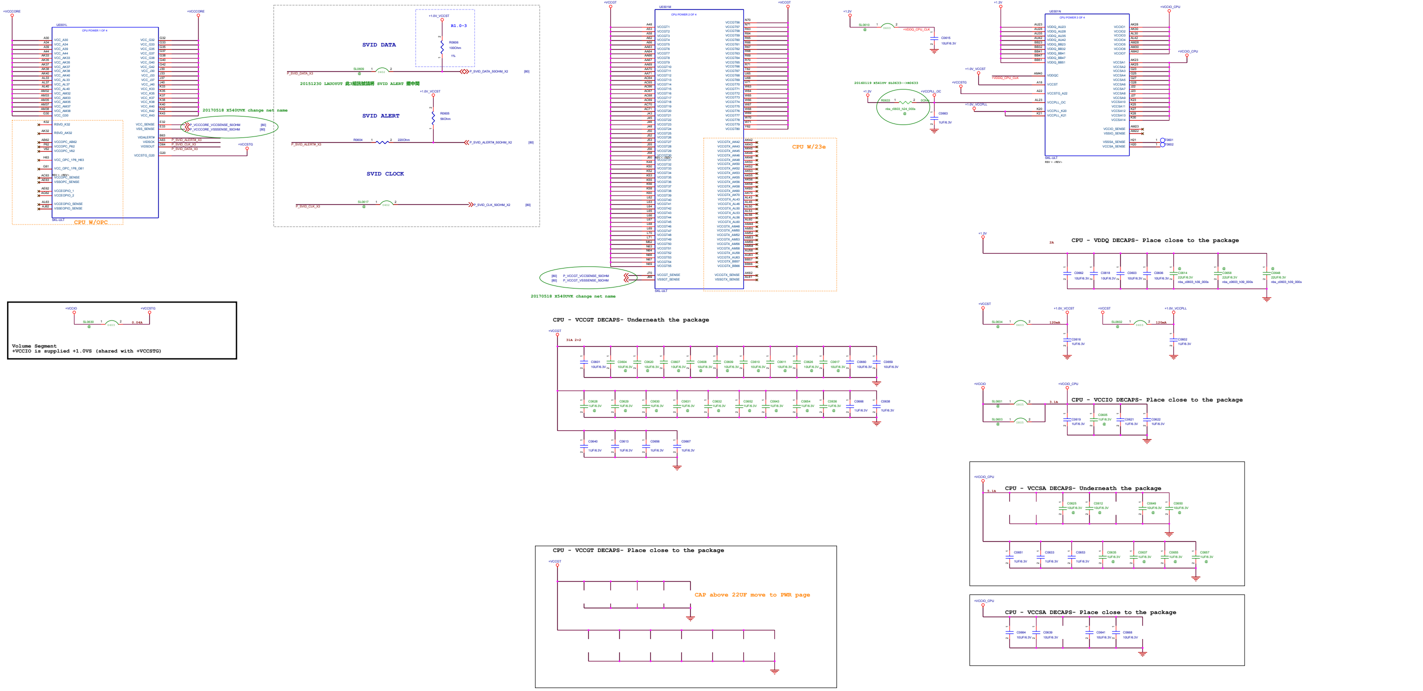
Transport Layer Security (TLS) Confidentiality



GPP_C2: weak internal pull down	
PU	Enable
PD	Disable Intel ME TLS ipher suite (no confodentiality) (Default)

BOM

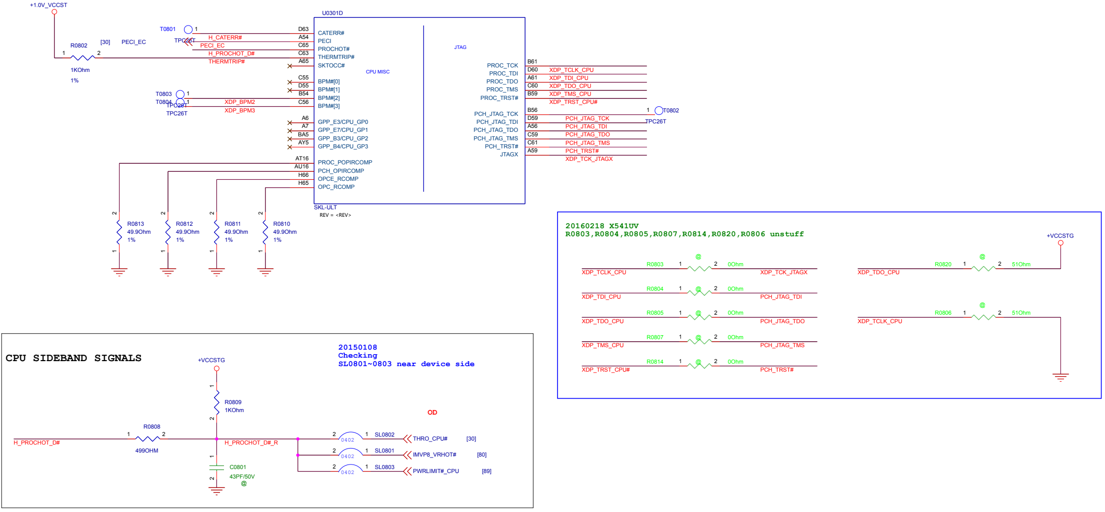
Project Name	X540UPR
Rev	R1.0
Title :	CPU_LPC,SPI,SMB,CLINK
Size	Custom
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	NB_EE
Date:	Monday, August 21, 2017
Sheet	5 of 102



BOM

Project Name	X540UV/UA	Rev R1.0
Title :	CPU_POEWR	
Size D	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Monday, August 21, 2017	Sheet 6	of 102

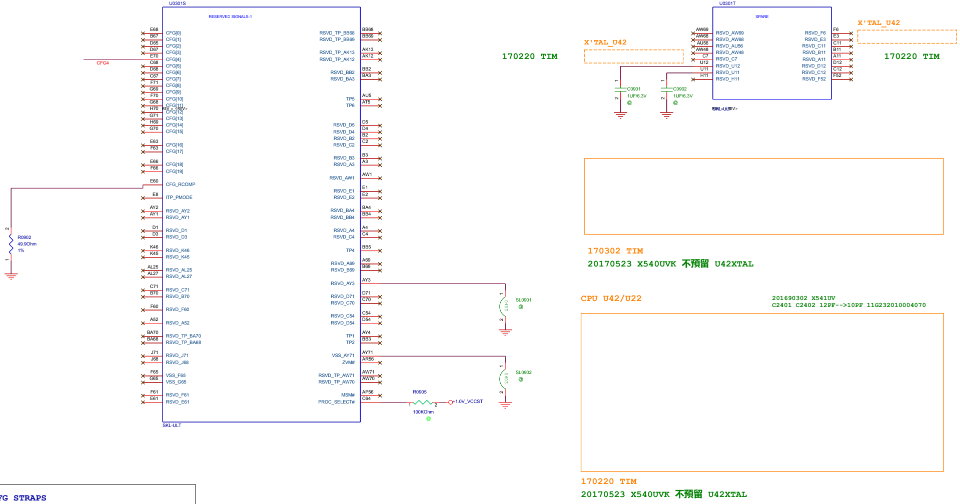
Main Board



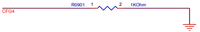
BOM

ASUS	Project Name X540UPR	Rev R1.0
Title : CPU_MISC,JTAG,CLK		
Size B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 8 of 102	

Main Board



CFG STRAPS

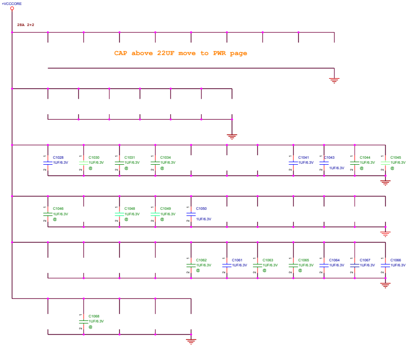


	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

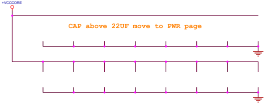
BOM

ASUS	Project Name: X540UPR	Rev: R1.0
Title : CPU_CFG,RSVD		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 9 of 102	

CPU - VCC DECAPS- Underneath the package



CPU - VCC DECAPS- Place close to the package



BOM

Project Name: X540UPR		Rev: R1.0
Title : CPU_POWER_CAP		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 10 of 102	

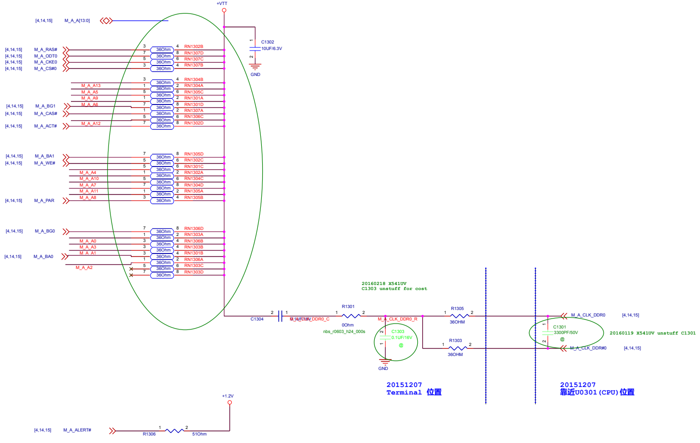


Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0],ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

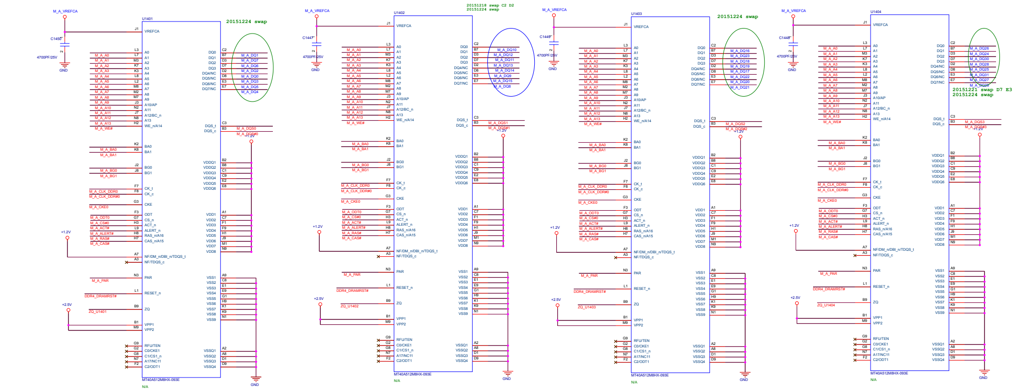
<Variant Name>

Title : DDR4_TERMINATION_A

Engineer: NB_EE

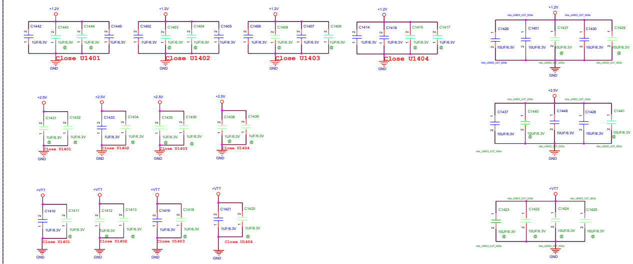
Size: C | Project Name: X540UPR | Rev: R1.0

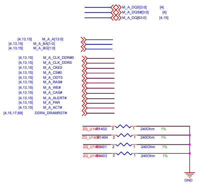
Date: Monday, August 21, 2017 | Sheet 13 of 102



Onboard Memory Source

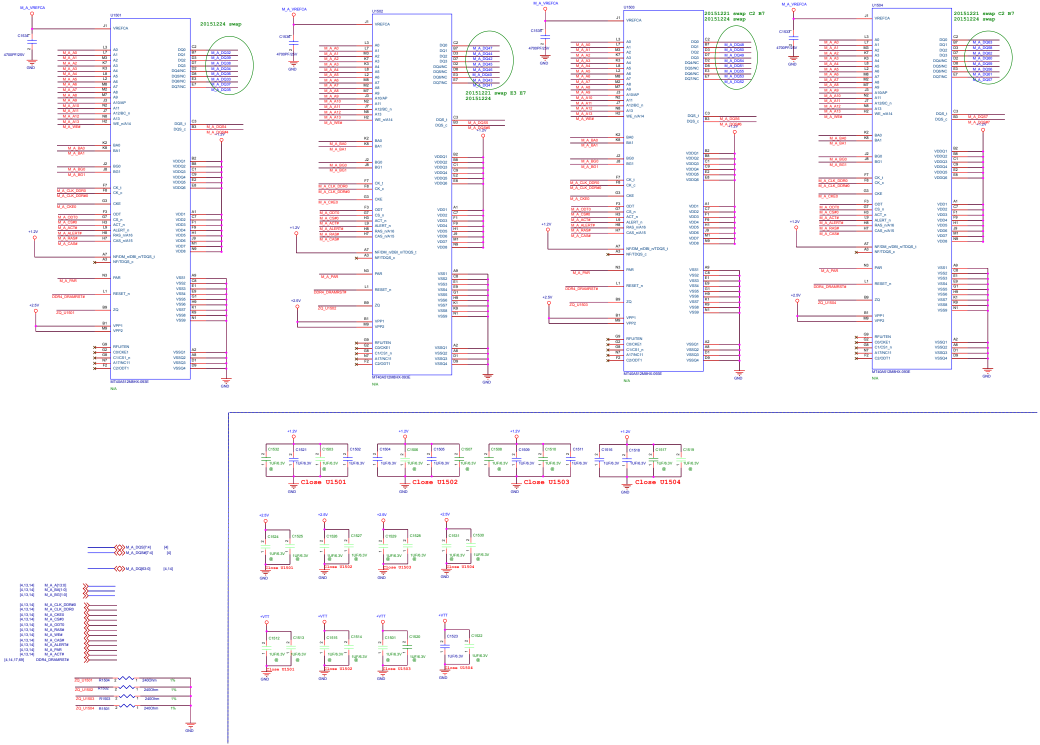
ASUS P/N	Capacity	Vendor
03012-00010000	4Gb 512X8	HYNIX/H5AN4G8NAFR-TFC
03012-00010300	4Gb 512X8	MICRON/MT40A512M8RH-083E:B
03012-00030300	8Gb 1024X8	HYNIX/H5AN8G8NMFR-TFC
03012-00030100	8Gb 1024X8	MICRON/MT40A1G8WE-083E:B





<Variant Name>

Title :	DDR4_ON-BOARD_A_L32	
Engineer:	NB_EE	
Size C	Project Name X540UPR	Rev R1.0
Date: Monday, August 21, 2017	Sheet 14 of 102	



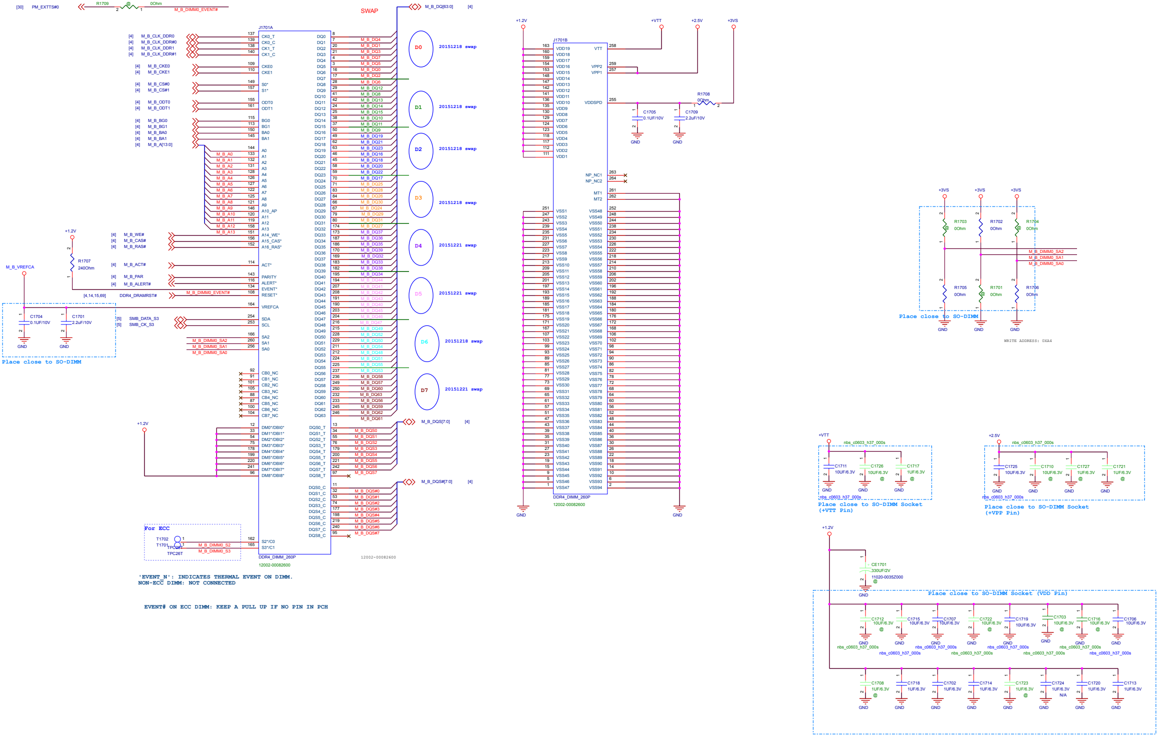
<Variant Name>

Title : DDR4_ON-BOARD_A_H32

Engineer: NB_EE

Size	Project Name	Rev
C	X540UPR	R1.0

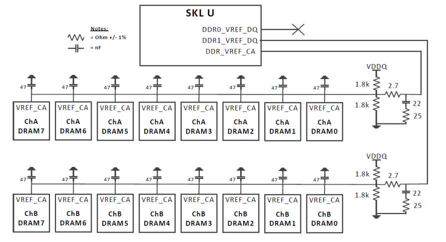
Date: Monday, August 21, 2017 Sheet 15 of 102



<Variant Name>

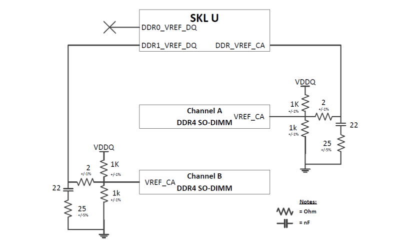
ASUS	Title :	DDR4_SO-DIMM_1
	Engineer:	NB_EE
Size: C	Project Name: X540UPR	Rev: R1.0
Date: Monday, August 21, 2017	Sheet 17 of 102	

Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview



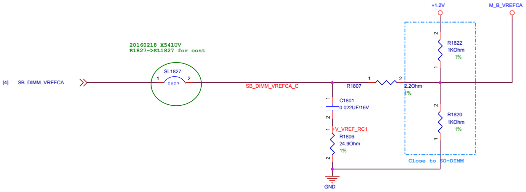
Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

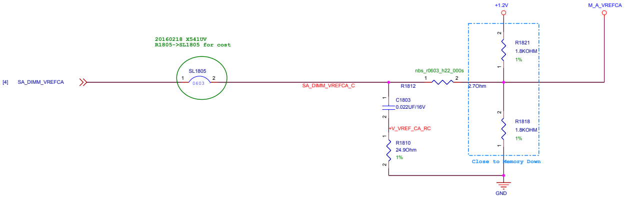
Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

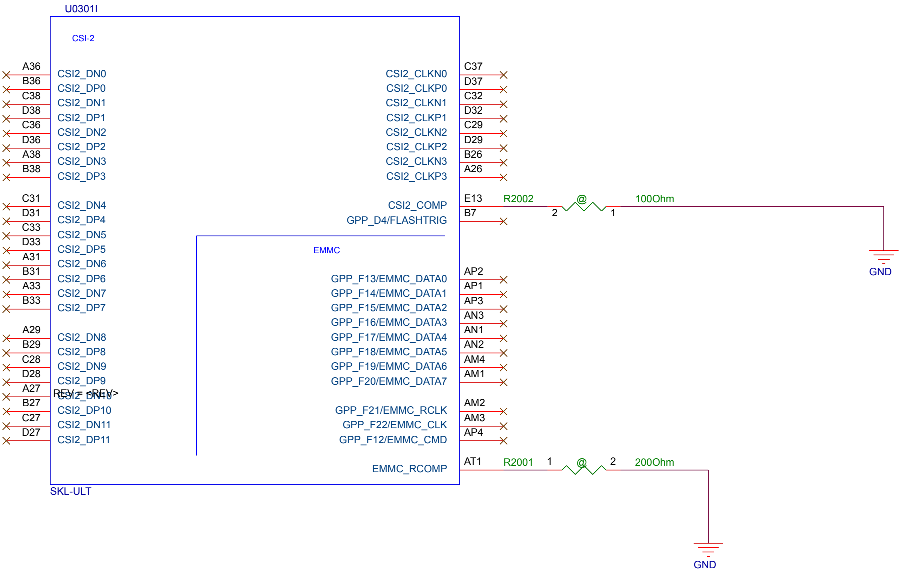
All Vref trace must be 20 mils width





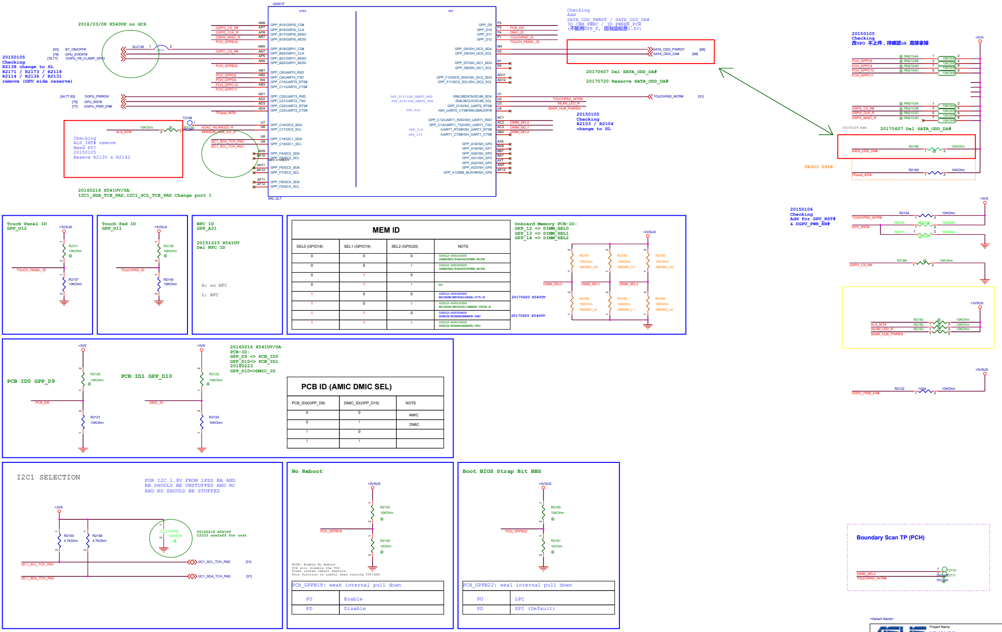
<Variant Name>

Title :	DDR4 CA VOLTAGE		
Engineer:	NB_EE		
Size: C	Project Name: X540UPR		Rev: R1.0
Date: Monday, August 21, 2017		Sheet 19 of 102	



BOM

ASUS	Project Name X540UPR	Rev R1.0
Title : CPU_PCH_CSI2,EMMC		
Size B	Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE	
Date: Monday, August 21, 2017	Sheet 20 of 102	



MEM ID			
SEL0 (GPIO18)	SEL1 (GPIO19)	SEL2 (GPIO20)	NOTE
0	0	0	03012-00010200 SAMSUNG/K4A4G085WE-BCPB
0	0	1	03012-00030000 SAMSUNG/K4A8G085WB-BCPB
0	1	0	
0	1	1	0G
1	0	0	03012-00030500 MICRON/MT40A1G8SA-075:H
1	0	1	03012-00010300 MICRON/MT40A512M8RH-083E:B
1	1	0	03012-00030400 HYNIX/H5AN8G8NAFR-UHC
1	1	1	03012-00010000 HYNIX/H5AN4G8NAFR-TFC

PCB ID (AMIC DMIC SEL)		
PCB_ID0(GPP_D9)	DMIC_ID(GPP_D10)	NOTE
0	0	AMIC
0	1	DMIC
1	0	
1	1	

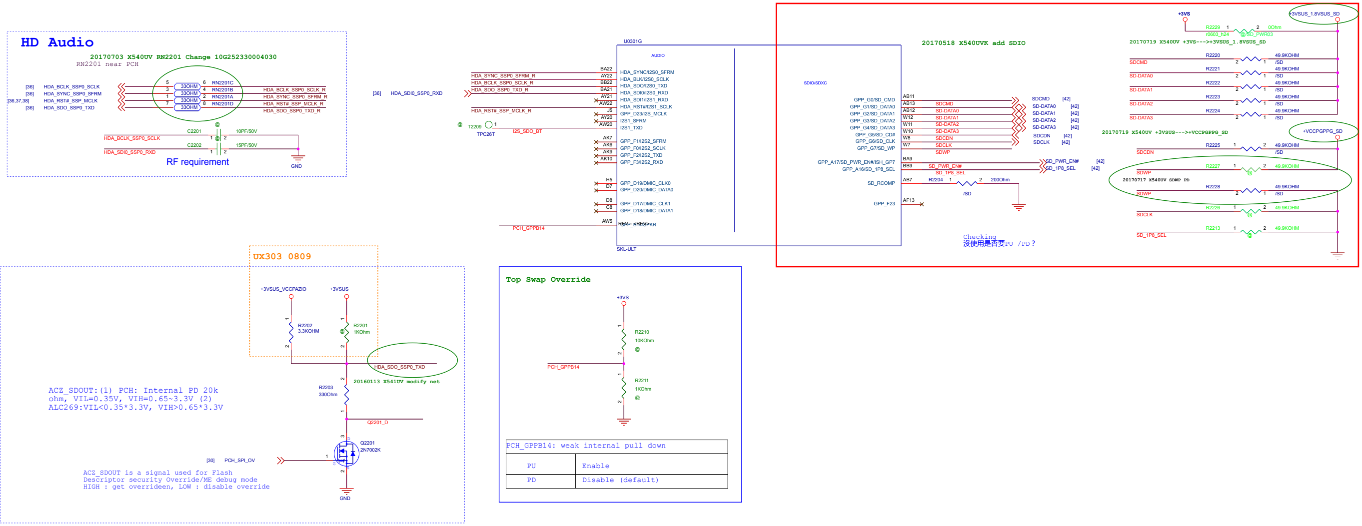
NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weal internal pull down	
PU	Enable
PD	Disable

PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

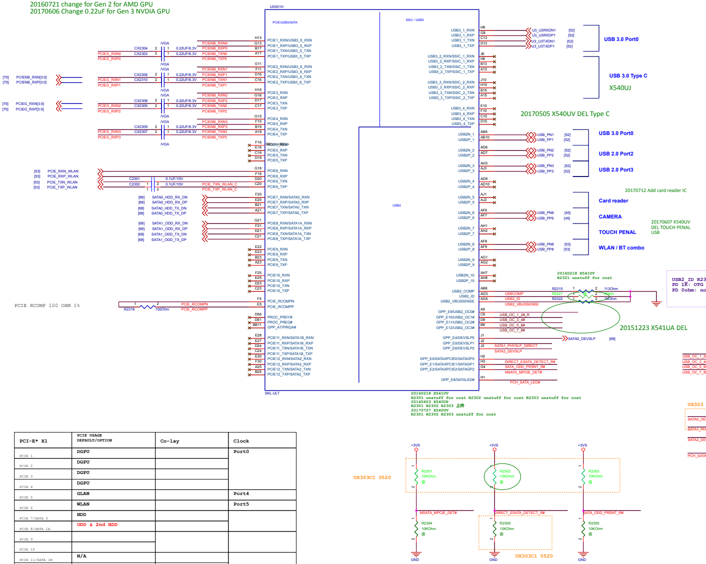
<Variant Name>

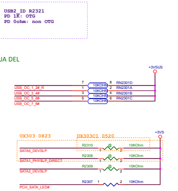
Project Name: X540UPR		Rev: R1.0
Title : CPU_CFG,RSVD,GND		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 21 of 102	



BOM

Project Name: X540UPR		Rev: R1.0
Title : CPU_PCH_AUDIO,SDIO,SDXC		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 22 of 102	





USB 2.0	
1	USB 2.0 Port
2	USB 2.0 Port
3	USB 2.0 Port
4	
5	
6	CAMERA
7	
8	WLAN / BT combo

Mapping

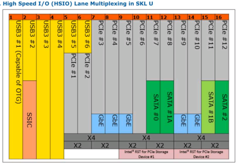
USB 3.0	
1	USB 3.0 Port0
2	
3	
4	

	USB2.0	USB3.0	OC	LOCATION	POWER
	1	1	0	USB3	+5V_USB_CON1
X540UJ X541UV	2			USB2.0	+5V_USB_CON1
X540UV	3			USB2.0	+5V_USB_CON1
	4				
	5				
	6			CAMERA	+3V_CAM
	7				
	8			WLAN / BT combo	+3VS_WLAN
	9				
	10				

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1	DGPU		Port0
PCIE 2	DGPU		
PCIE 3	DGPU		
PCIE 4	DGPU		
PCIE 5	GLAN		Port4
PCIE 6	WLAN		Port5
PCIE 7/SATA 0	HDD		
PCIE 8/SATA 1A	ODD & 2nd HDD		
PCIE 9			
PCIE 10			
PCIE 11/SATA 1B	N/A		

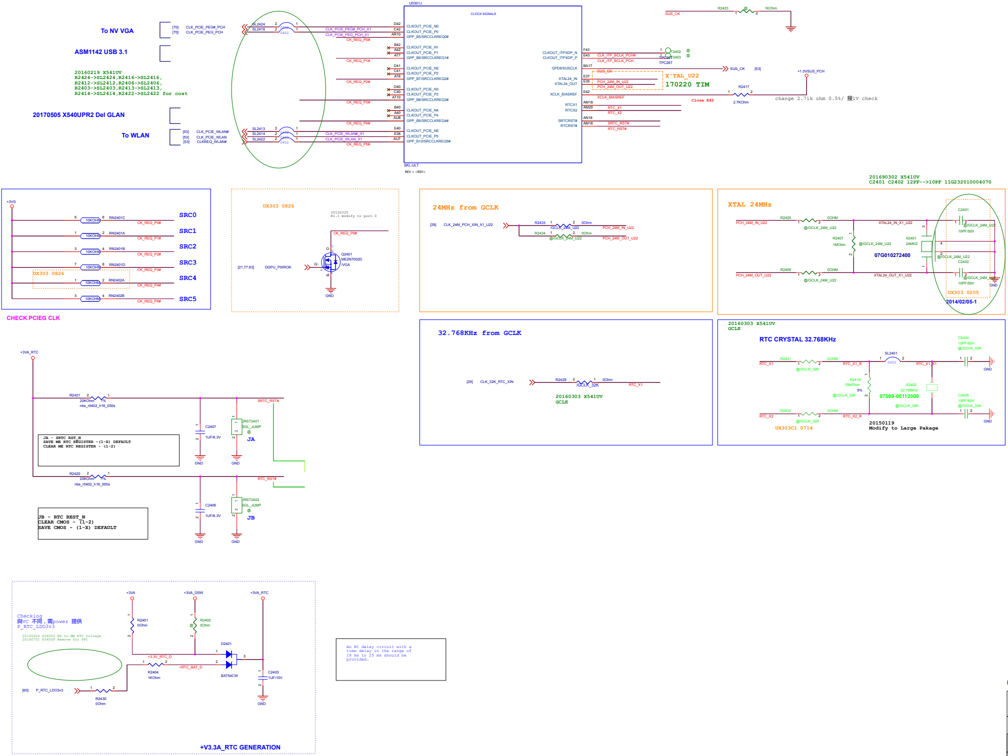
SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	ODD & 2nd HDD
PORT 2	N/A OPTION PCIE
PORT 3	N/A OPTION PCIE

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL U



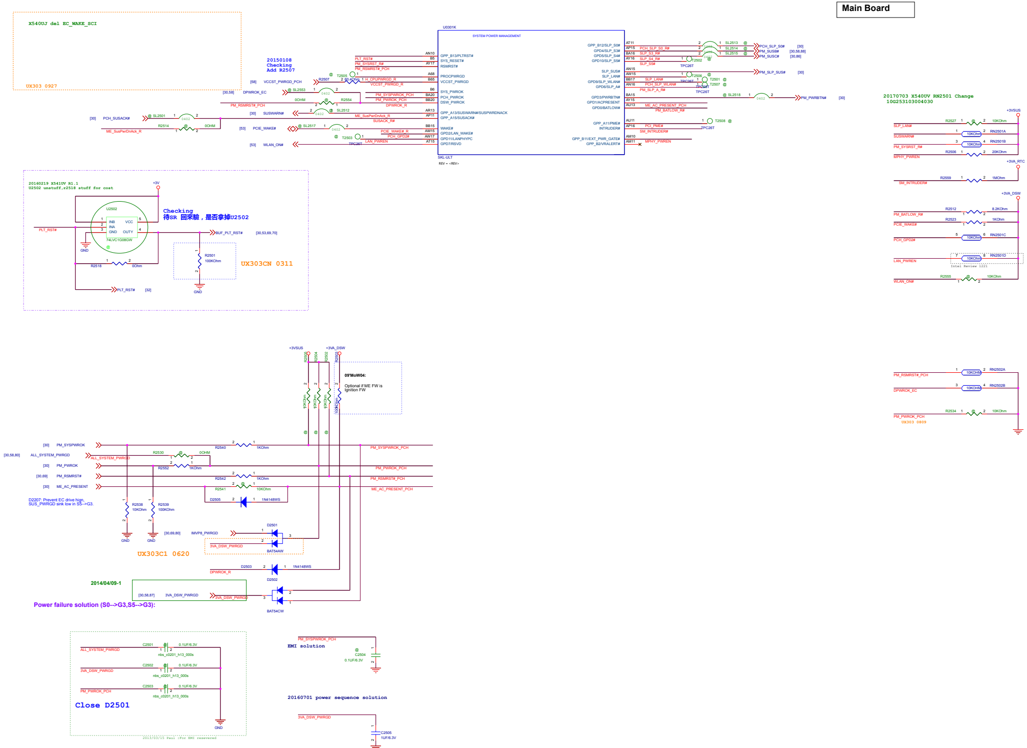
BOM

Project Name	X540UPR	Rev R1.0
Title :	CPU_PCH_PCIE,USB,SATA	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 23 of 102	



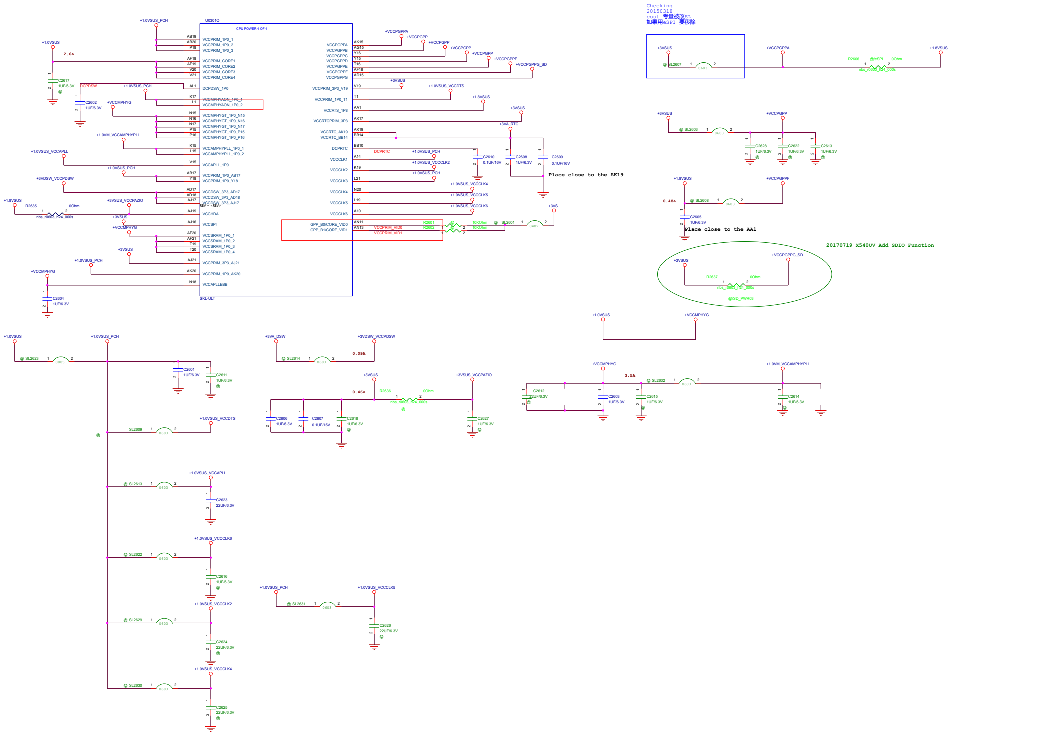
BOM

Project Name	X540UPR	Rev R1.0
Title :	CPU_PCH_CLOCK SIGNALS,RTC	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 24 of 102	



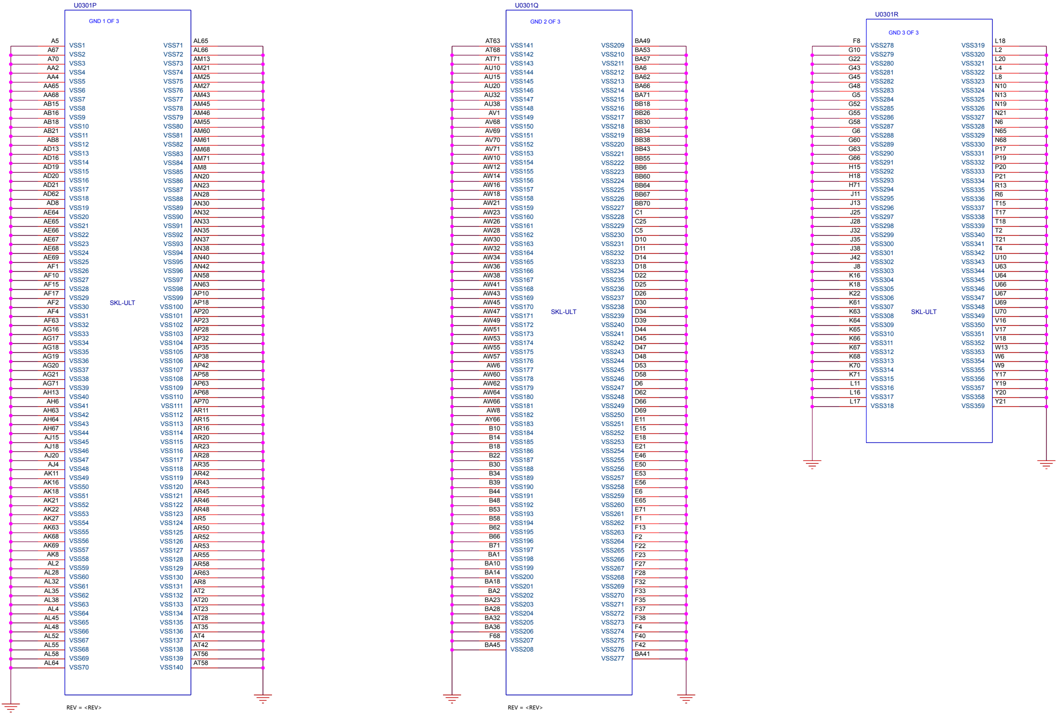
BOM

ASUS	Project Name: X540UPR	Rev: R1.0
Title : CPU_PCH_SYS_POWER		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 25 of 102	



BOM

Project Name	X540UPR	Rev R1.0
Title :	CPU_PCH_POEWR,GND	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 26 of 102	



BOM

REV

Project Name: X540UPR

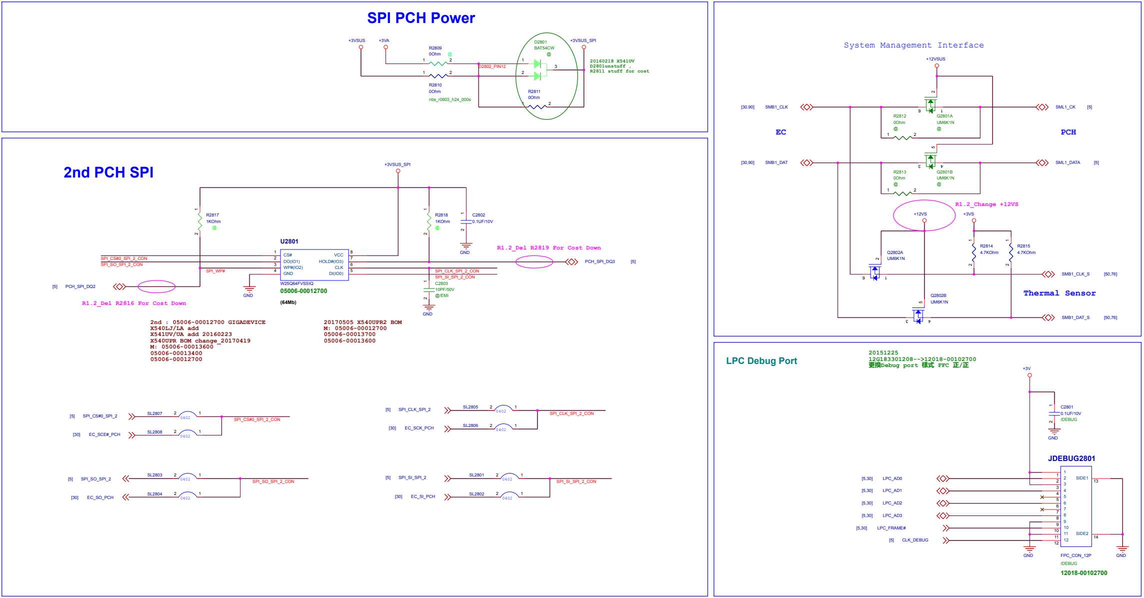
Rev: R1.0

Title : CPU_PCH_POEWR,GND

Size: B

Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE

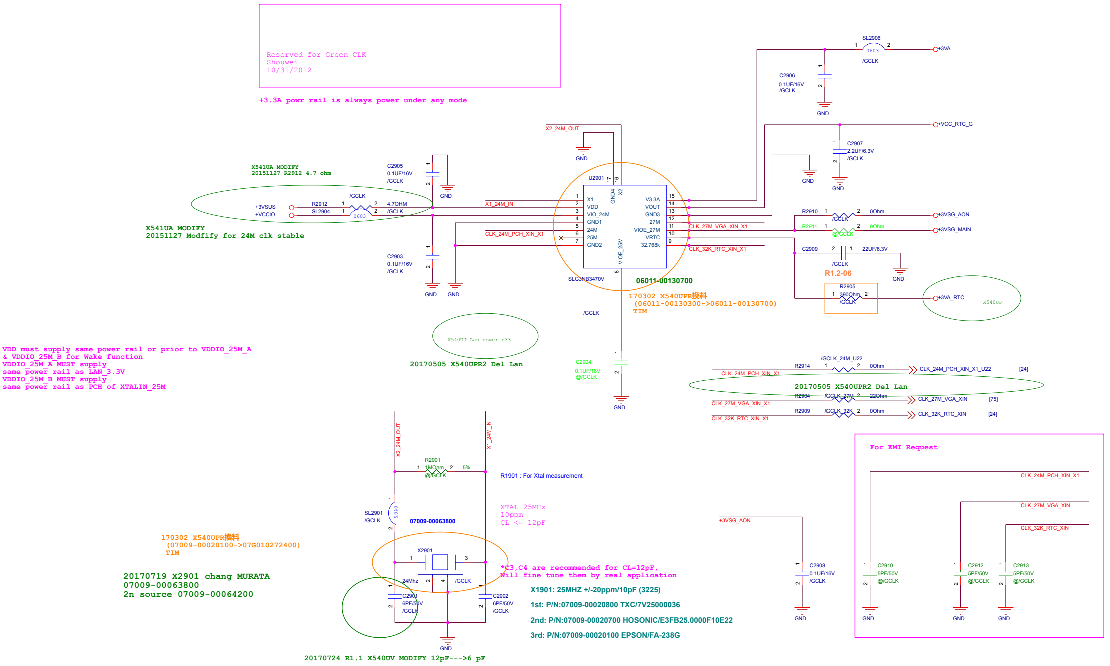
Date: Monday, August 21, 2017 Sheet 27 of 102



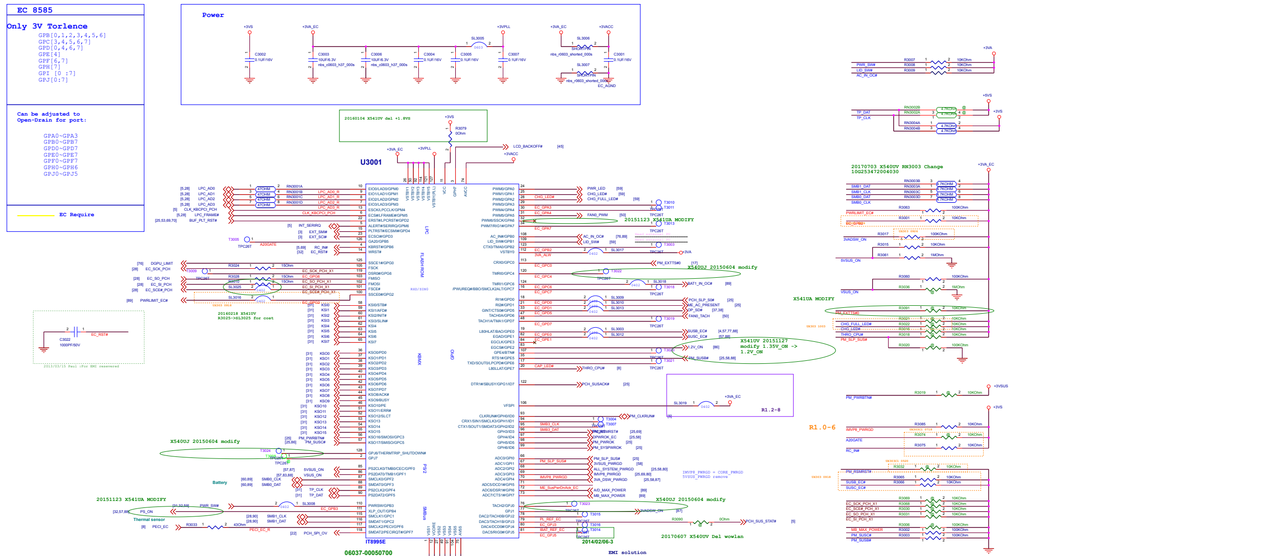
<Variant Name>

ASUSTeK COMPUTER INC.	Title : 28_PCH-SPI ROM,OTH		
	Engineer: NB_EE		
Size: C	Project Name: X540UPR		Rev: R1.0
Date: Monday, August 21, 2017	Sheet 28	of 99	

Silego Green CLK



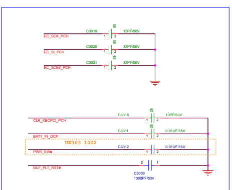
ASUS	Title :	Green CLK Gen	
ASUSTeK COMPUTER INC. NB1	Engineer:	NB_EE	
Size: C	Project Name: X540UPR		Rev: R1.0
Date: Monday, August 21, 2017	Sheet 29 of 99		

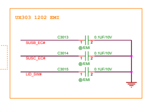


ITE Version	ASUS P/N
IT8995E/AX	06037-00050400
IT8995E-128/CX	06037-00050500
IT8995E-128/DX	06037-00050700

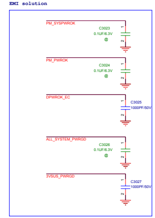
目前是使用下兩顆，此兩顆差異在封裝大小，功能相同：

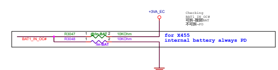
06037-00050500	EMBEDDED CONTRO IT8995E-128/CX	ITE LQFP-128
06037-00050600	EMBEDDED CONTR IT8995VG-128/CX	ITE VFBGA-128





EMI solution

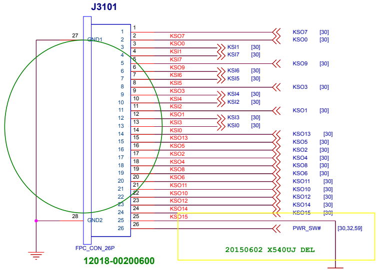




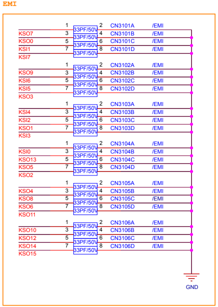
BOM

ASUS	Project Name X540UPR	Rev R1.0
Title : IT8995E-128/CX		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 30 of 102	

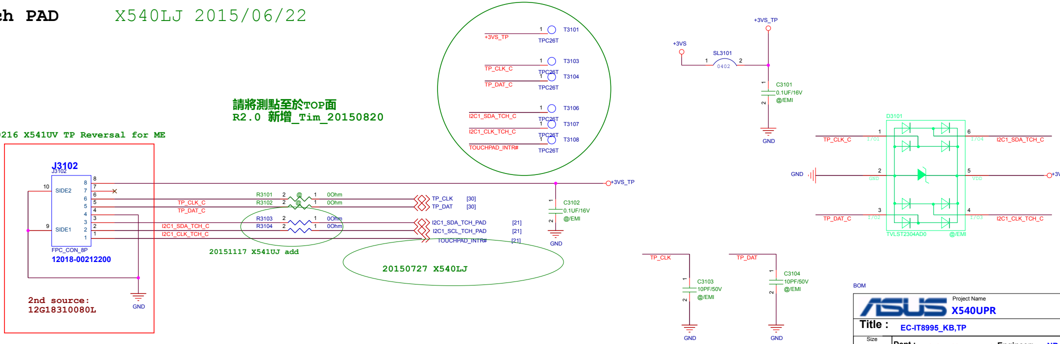
Internal Keyboard



20160316 維持料號ACES
20160526 footprint nbs_fpc_26p_007 --> nbs_fpc_26p_000c



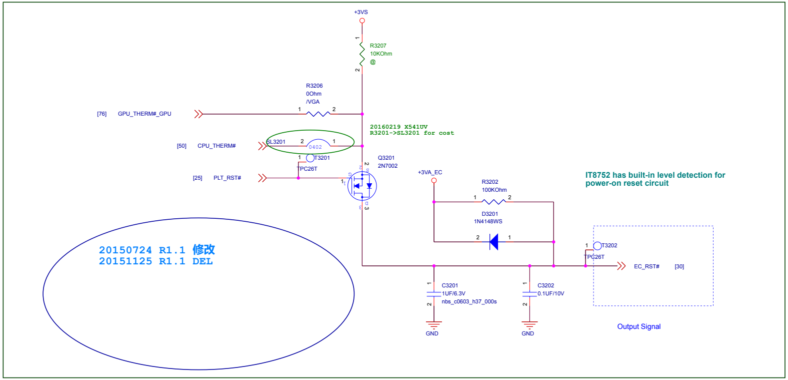
Touch PAD X540LJ 2015/06/22



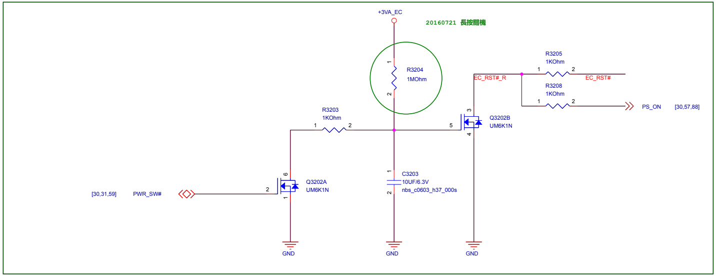
BOM

Project Name: X540UPR		Rev: R1.0
Title : EC-IT8995_KB,TP		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 31	of 99

Thermal Policy

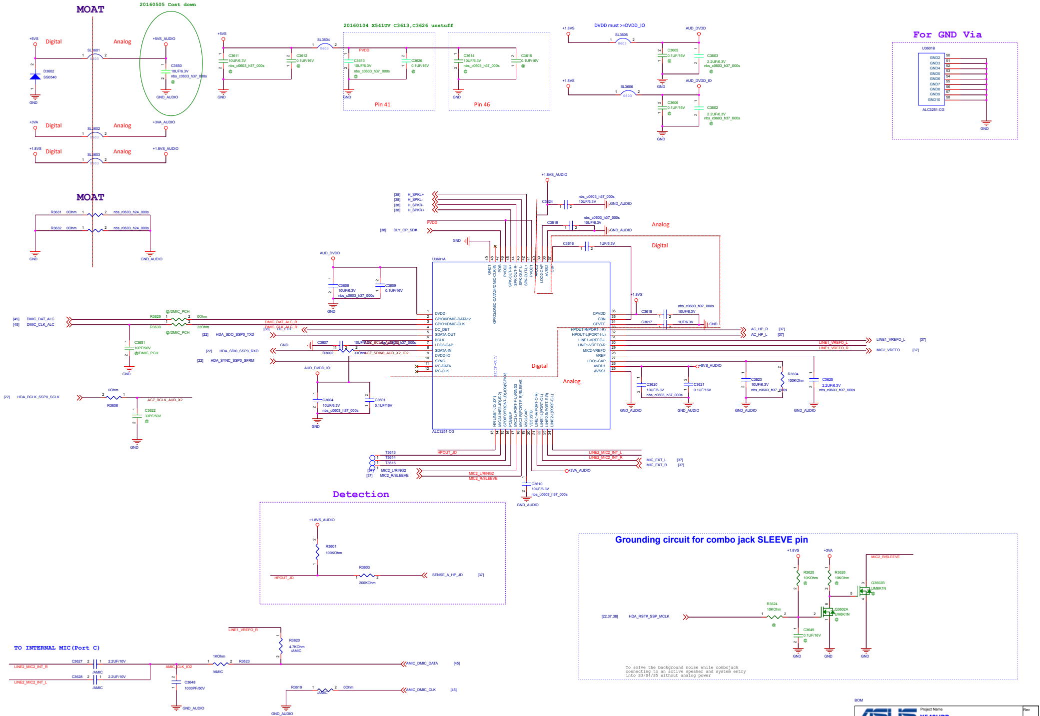


battery embedded (press pwr_sw 10sec, then reset ec)



<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : 32_RST_Reset Circuit	
	Engineer: NB_EE	
Size: B	Project Name: X540UPR	Rev: R1.0
Date: Monday, August 21, 2017	Sheet 32 of 99	



BOM

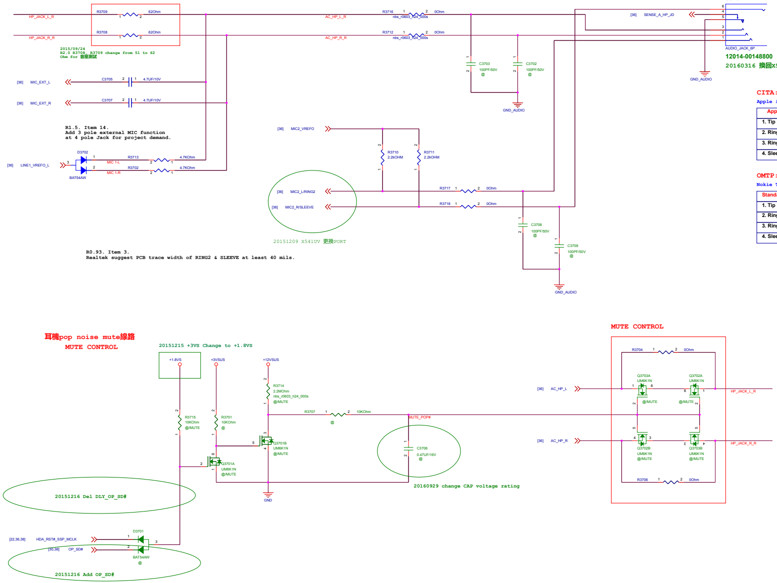
ASUS	Project Name X540UPR	Rev R1.0
Title :	HDD Board-AUD-ALC3236	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 36 of 102	

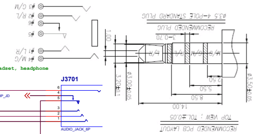
Universal Jack (Normal open type)

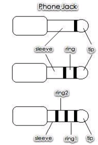
R1.3. Item 12.
Add 4 pole headset jack normal
open type for project demand.

- 尺寸：一般分三種規格，2.5mm、3.5mm、6.35mm。
- 種類：一般分也三種規格，TS 端子 (Mono)、TRS 端子 (Stereo)、TRRS 端子 (Stereo + Mic/Video)。

R1.4. Item 13.
Recommand the HP damping resistance 56 ohm for CB certification.
Depend on your project, you can change the resistance value to meet CB certification
(under 150mV), best chioce is between 140mV~150mV section.







CITA：國際標準

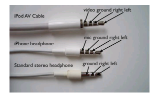
Apple iPhone/HTC/小米 的 Phone Jack 定義：

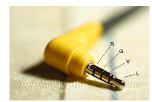
Apple	iPad (Stereo)	iPod (Stereo)	iPhone (Mic)	iPod (AV)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	-	-	Ground	Ground
4. Sleeve	Ground	Ground	Mic	Video

OMTP：國家標準

Nokie Type 的 Phone Jack 定義：

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel

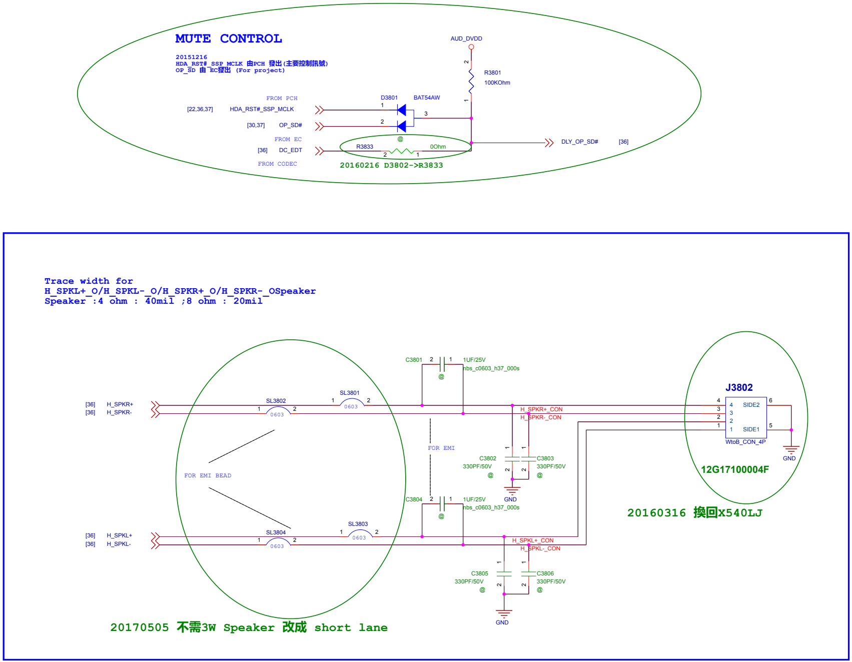




BOM

ASUS	Project Name: X540UPR	Rev: R1.0
Title : IO Board-Audio Jack		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 37 of 99	

20160530
1. Del R3833 & Add D3801
2. AUD_DVDD_IO--->AUD_DVDD



BOM

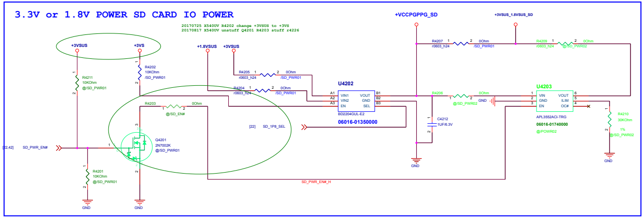
Project Name X540UPR		Rev R1.0
Title : HDD Board-Speaker		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 38	of 99

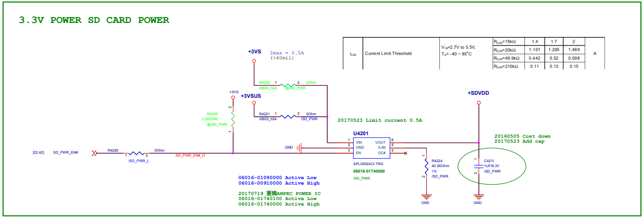
12023-00025900

Without card: CD/GND 狀態為開路 WP/CD狀態 開路
Insert card (unlock):CD/GND 短路 WP/CD短路
Insert card (lock):CD/GND 短路 WP/CD開路

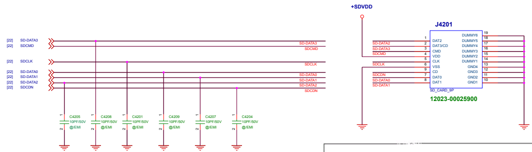
20170725 X540UV SD Power Condition
1./SD_PWR+/SD_PWR01
2./SD_PWR+/SD_PWR01-R4207+/SD_PWR02
3./SD_PWR+/SD_PWR03(@/SD_PWR03) ONLY 3.3V

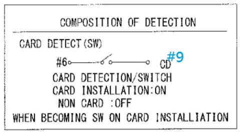
PIN	SD mode
#1	DAT2
#2	DAT3/CD
#3	CMD
#4	V_{DD}
#5	CLK
#6	Vss
#7	DAT0
#8	DAT1
CD	CARD DETECT





I_{LIM}	Current Limit Threshold	V_{IN}=2.7V to 5.5V, T_A= -40 ~ 85°C	R_{ILIM}=15kΩ	1.4	1.7	2	A
			R_{ILIM}=20kΩ	1.101	1.295	1.489	
			R_{ILIM}=49.9kΩ	0.442	0.52	0.598	
			R_{ILIM}=210kΩ	0.11	0.13	0.15	

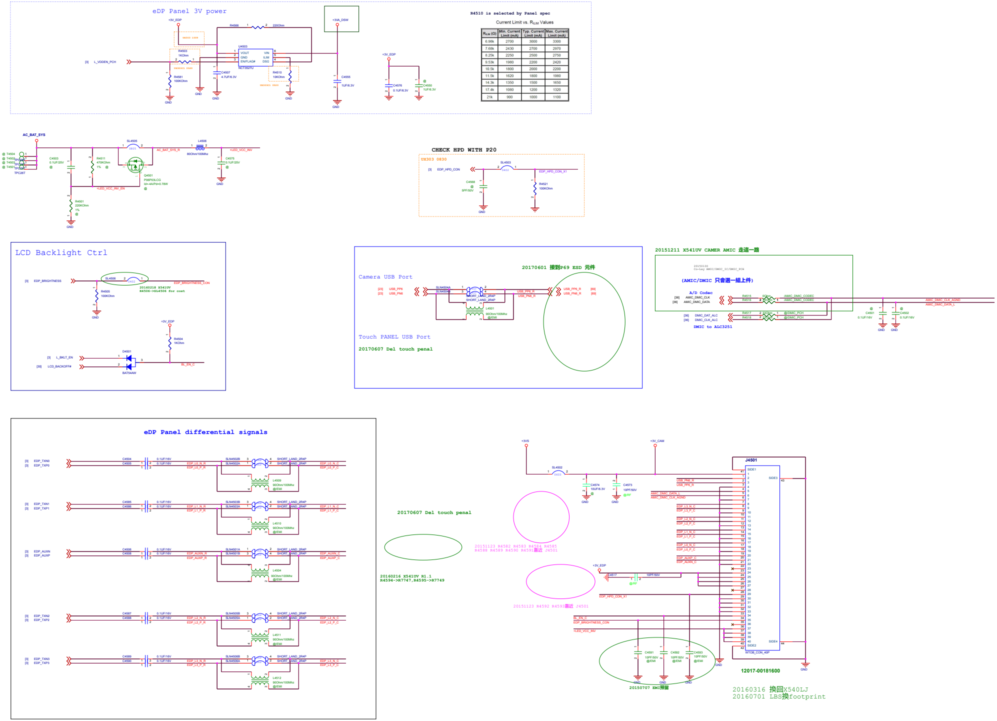




BOM

Project Name: X540UPR		Rev: R1.0
Title : CARD READER CONNECTOR		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE	
Date: Monday, August 21, 2017	Sheet 42 of 102	

eDP (LVDS) Panel



Current Limit vs. R_{ILIM} Values

R_{ILIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
6.98k	2700	3000	3300
7.68k	2430	2700	2970
8.25k	2250	2500	2750
9.53k	1980	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1080	1200	1320
21k	900	1000	1100

BOM

Project Name: X540UPR

Rev: R1.0

Title: LCD Panel_CMOS_DMIC

Size: D

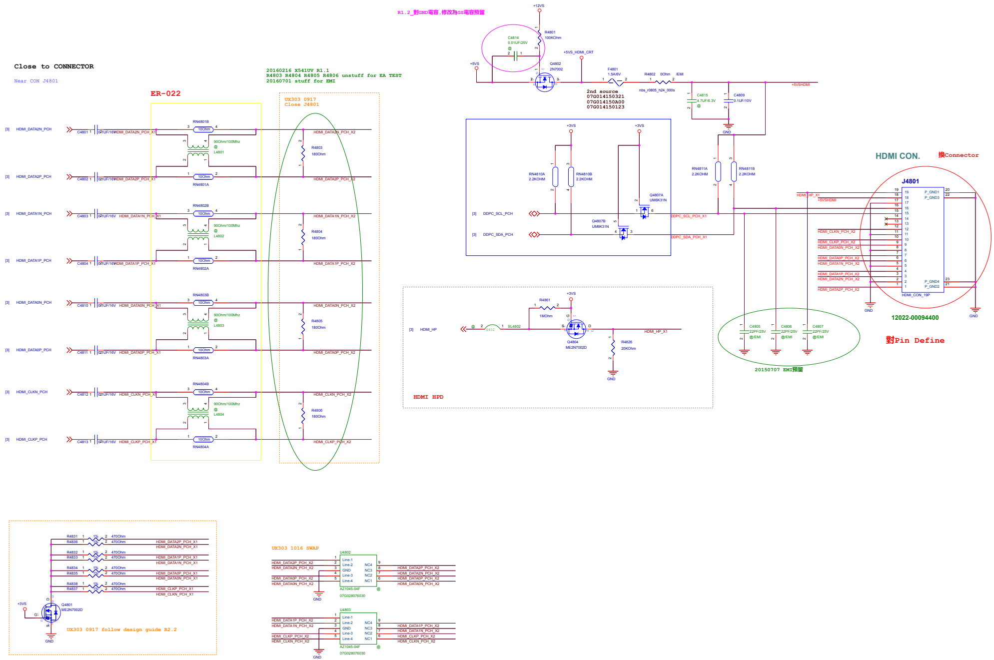
Dept.: ASUSTeK COMPUTER INC.

Engineer: NB_EE

Date: Monday, August 21, 2017

Sheet 45 of 102

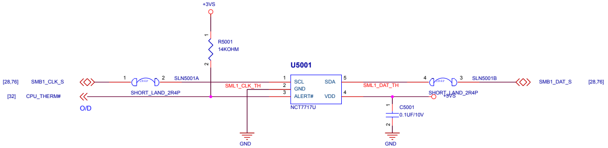
HDMI type-A



BOM

ASUS	Project Name: X540UPR	Rev: R1.0
Title : HDMI-type D		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 48 of 102	

CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

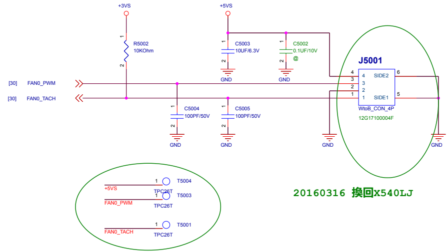
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

	PULL-UP RESISTOR	TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

```
-----------------OTHER SIGNALS
 10 mils
===============GND
 10 mils
=========H_THERMDA(10 mils)
 10 mils
=========H_THERMDC(10 mils)
 10 mils
=========GND
 10 mils
-------------------OTHER SIGNALS
Avoid FSB,Power
```

DC FAN Control

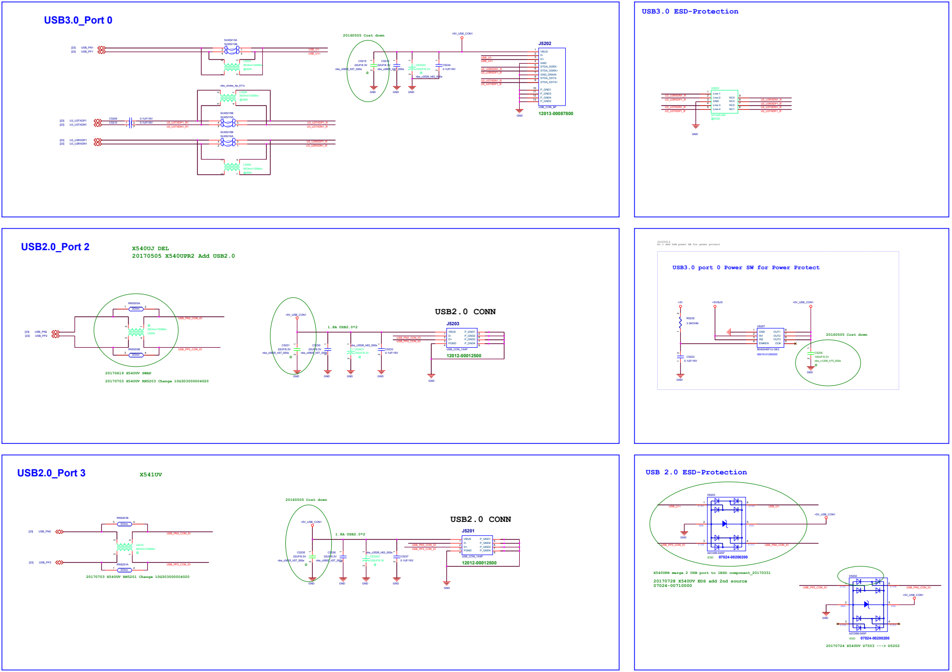


20160316 換回X540LJ

請將測點至於TOP面
R2.0 新增_Tim_20150820

<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : 50_FAN_Thermal Sensor	
	Engineer: NB_EE	
Size: B	Project Name: X540UPR	Rev: R1.0
Date: Monday, August 21, 2017	Sheet 50 of 99	



ASUS

Project Name: X540UPR

Rev: R1.0

Title : USB 3.0 + 2.0 CONN.

Size: D

Dept.: ASUSTeK COMPUTER INC.

Engineer: NB_EE

Date: Monday, August 21, 2017

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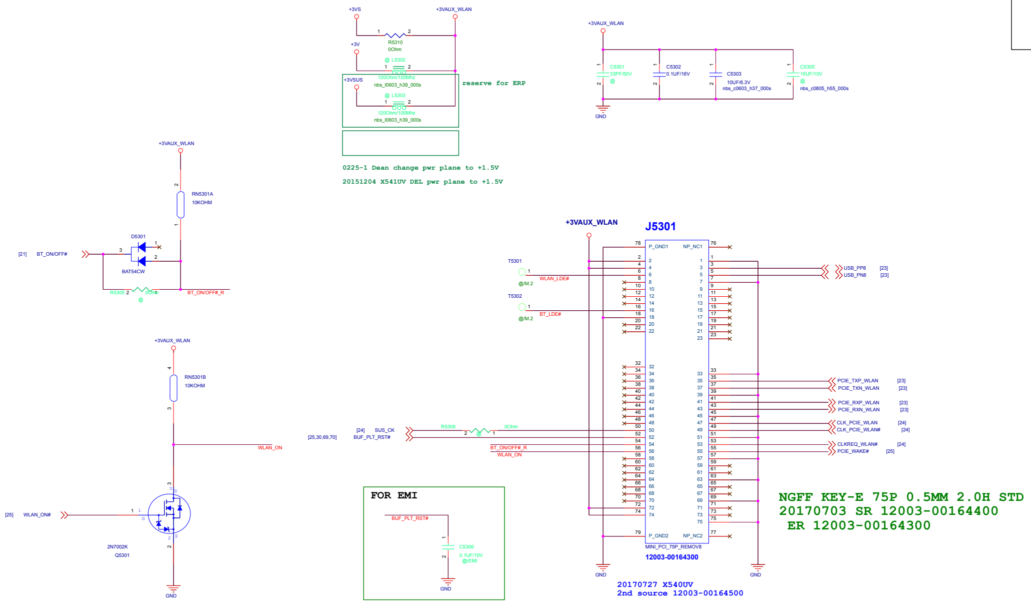
Follow X550VXK
reverse wake on WLAN

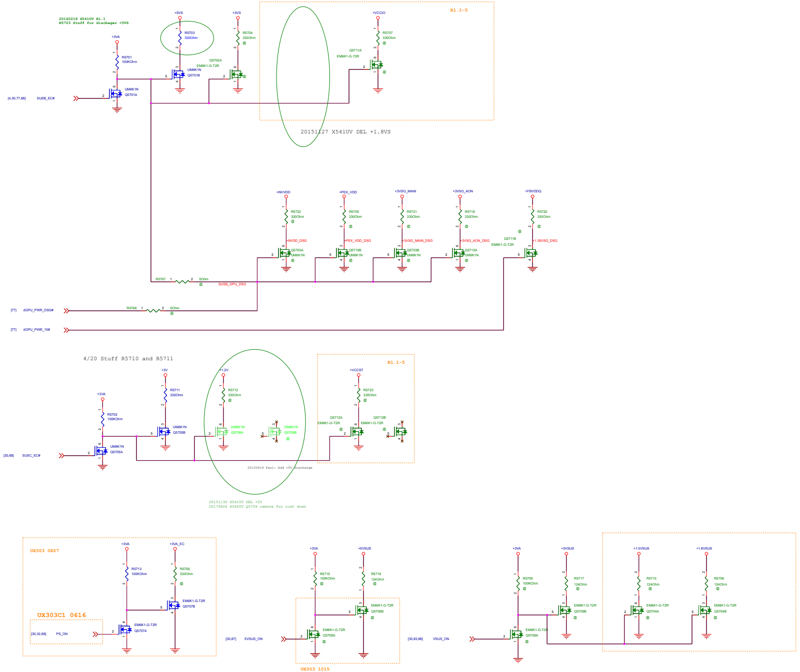
20170620 X540UV USE M.2 Merge Power CAP



<Variant Name>

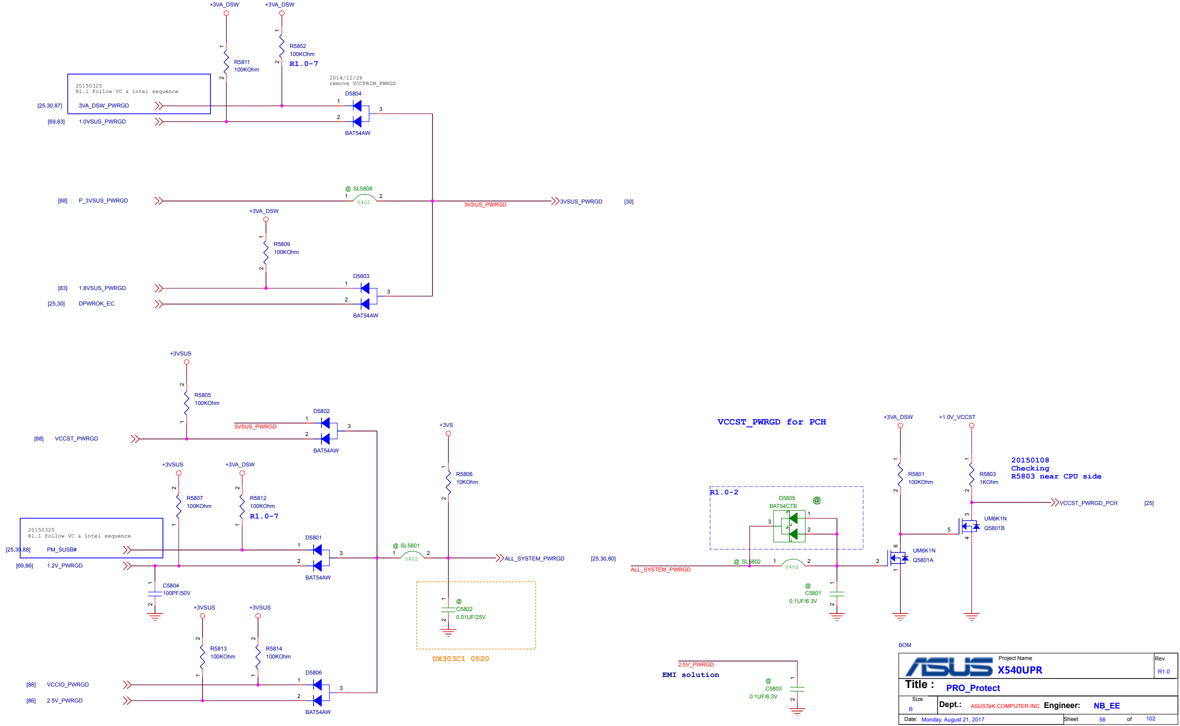
ASUS	Project Name: X540UPR	Rev: R1.0
Title : MINICARD(WLAN)		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 53 of 99	

Main Board

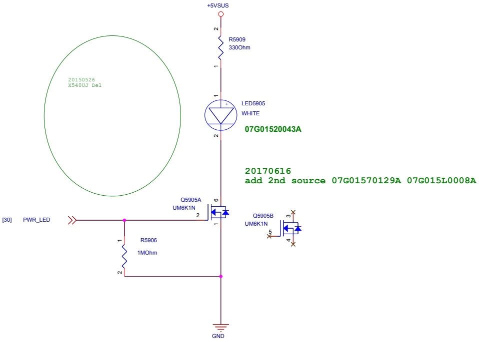


BOM

ASUS	Project Name: X540UV/UA	Rev: R1.0
Title : DSG_Discharge		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Monday, August 21, 2017	Sheet 57 of 102	

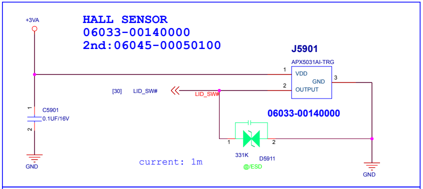

+3VA_DSW
R5811
100KOhm
R5852
100KOhm
R1.0-7
20150325
R1.1 follow VC & intel sequence
2014/12/26
remove VCCPRIM_PWRGD
D5804
BAT54AW
[25,30,87] 3VA_DSW_PWRGD
[69,83] 1.0VSUS_PWRGD
[88] P_3VSUS_PWRGD
@ SL5808
0402
3VSUS_PWRGD
3VSUS_PWRGD [30]
R5809
100KOhm
D5803
BAT54AW
[83] 1.8VSUS_PWRGD
[25,30] DPWROK_EC
+3VSUS
R5805
100KOhm
D5802
BAT54AW
[88] VCCST_PWRGD
+3VS
R5806
10KOhm
R5807
100KOhm
R5812
100KOhm
R1.0-7
D5801
BAT54AW
[25,30,88] PM_SUSB#
[69,86] 1.2V_PWRGD
@ SL5801
ALL_SYSTEM_PWRGD [25,30,80]
C5804
100PF/50V
@ C5802
0.01UF/25V
UX303C1 0520
R5813
100KOhm
R5814
100KOhm
D5806
BAT54AW
[88] VCCIO_PWRGD
[86] 2.5V_PWRGD
VCCST_PWRGD for PCH
+1.0V_VCCST
R5801
100KOhm
R5803
1KOhm
20150108
Checking
R5803 near CPU side
VCCST_PWRGD_PCH [25]
R1.0-2
D5805
BAT54CTB
UM6K1N
Q5801B
UM6K1N
Q5801A
ALL_SYSTEM_PWRGD
@ SL5802
@ C5801
0.1UF/6.3V
2.5V_PWRGD
EMI solution
@ C5803
0.1UF/6.3V
BOM
Project Name
X540UPR
Rev
R1.0
Title : PRO_Protect
Size B
Dept.: ASUSTeK COMPUTER INC.
Engineer: NB_EE
Date: Monday, August 21, 2017
Sheet 58 of 102

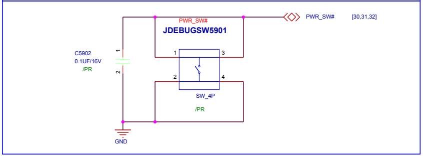
POWER LED



WIRELESS/ BT LED

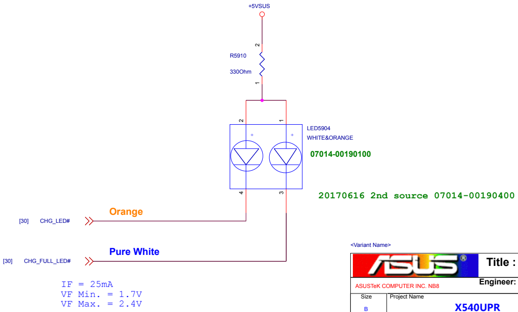
CAP Lock LED





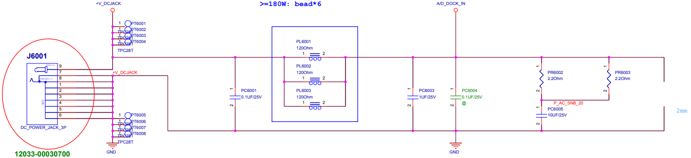
LED indicator

Charger LED



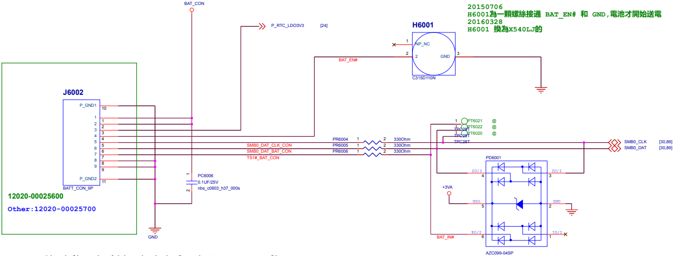
<Variant Name>

ASUS	Title :	59_Power & WIFI & CAP LED	
ASUSTeK COMPUTER INC. NB8	Engineer:	NB_EE	
Size: B	Project Name: X540UPR		Rev: R1.0
Date: Monday, August 21, 2017	Sheet 59	of 99	



換Connector 整個 GND Shape 都要跟PIN腳連起來

Battery Connector



07024-00200200

20170728 X540UV EDS add 2nd source
07024-00710000

Pin define should be checked after battery team confirm

Pin Seq.	Name	Description	Remark
1	P+	Battery pack positive terminal	Output voltage
2	P+	Battery pack positive terminal	Output voltage
3	LDO 3.3V		
4	EN#	External charge & discharge Mosfet control pin.	SYSTEM Connection to GND for charge & discharge
5	SMBC	Serial clock input	SMBC
6	SMBD	Serial data input	SMBD
7	BAT_IN#	EC detect battery_in pin	PACK inside 0 Ω connect to GND
8	P-	Battery pack negative terminal.	GND
9	P-	Battery pack negative terminal.	GND

<Variant Name>

ASUS	Project Name: X540UVK		Rev: R0.1
Title : 60_DC_DC & BAT IN			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Andy	
Date: Monday, August 21, 2017	Sheet 60 of 102		

TOP Hole A BOT Hole B

H6501
GND NP_NC
2D_D110_D98N
s11475
GND

TOP Hole C BOT Hole D

TOP Hole E BOT Hole F

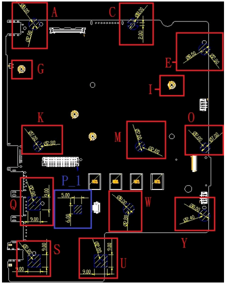
H6503
GND NP_NC
2D_D110_DO122X98N
s11476
GND

TOP Hole K BOT Hole L

H6504
CT276CB315D110
s11477
GND

TOP Hole O BOT Hole P

H6506
CT276CB315D110
s11477
GND



20170626 X540UV使用的NUT使用的
13GNMU10M010-1 FOOTPRINT
20170724 NUT 改成使用料件的料號

BOT CPU NUT

H6517
CT256BID146
13020-00105800
GND

H6518
CT256BID146
13020-00105800
GND

20170724 改料號13020-00105800

TOP VGA NUT

H6521
CT256BID146
/VGA_NUT
13G02D004000
GND

H6522
CT256BID146
/VGA_NUT
13020-01372300
GND

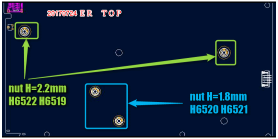
20170724 改料號

TOP CPU NUT

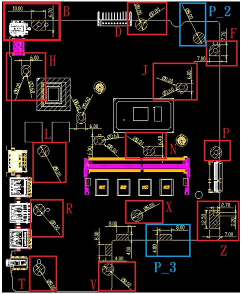
H6519
CT256BID146
13020-01372300
GND

H6520
CT256BID146
13G02D004000
GND

20170724 改料號



X540UP
修改Heat sink
NUT的foot-print，修改為Hole的foot-print
20160324



TOP Hole M BOT Hole N

H6505
CT276CRB315X252D110
s11473
GND

TOP Hole Q BOT Hole R

H6507
GND NP_NC
2D_D110_D98N
s11478
GND

TOP Hole S BOT Hole T

H6508
GND NP_NC
2D_D110_DO98X118N
s09296
GND

TOP Hole U BOT Hole V

H6509
ST354CB315D110
s11397
GND

TOP Hole W BOT Hole X

H6510
C315D110
s09211
GND

TOP Hole Y BOT Hole Z

H6511
GND NP_NC
2D_D94_DO106X87N
s11479
GND

TOP Hole

H6523
C197D197N
s04823

TOP PAD P_1 EMI P.69

H6512
SMD130X169
13040-00740000
GND

20170725 X540UV H6512 不需要測飾貼
20170818 X540UV 修改為SMT GASKET

BOT PAD P_2

H6513
C315
temp_T_0961
GND

20170725 X540UV H6513 不需要測飾貼

BOT PAD P_3

H6514
SMD315X157
temp_T_001472
GND

H6515
SMD315X157
temp_T_001472
GND

H6516
SMD315X157
temp_T_001472
GND

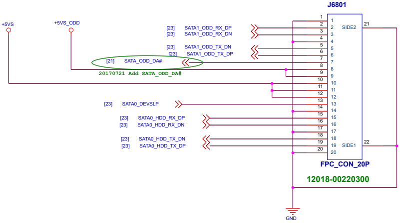
<Variant Name>

ASUS	Title : 65_ME_Conn & Skew Hole		
ASUSTeK COMPUTER INC. NB4	Engineer: NB_EE		
Size C	Project Name X540UPR		Rev R1.0
Date: Monday, August 21, 2017		Sheet 65 of 99	

MB to HDD_B

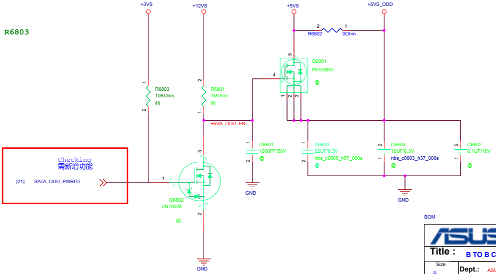
MB端(MB to HDD_B)

20150520 X540UJ



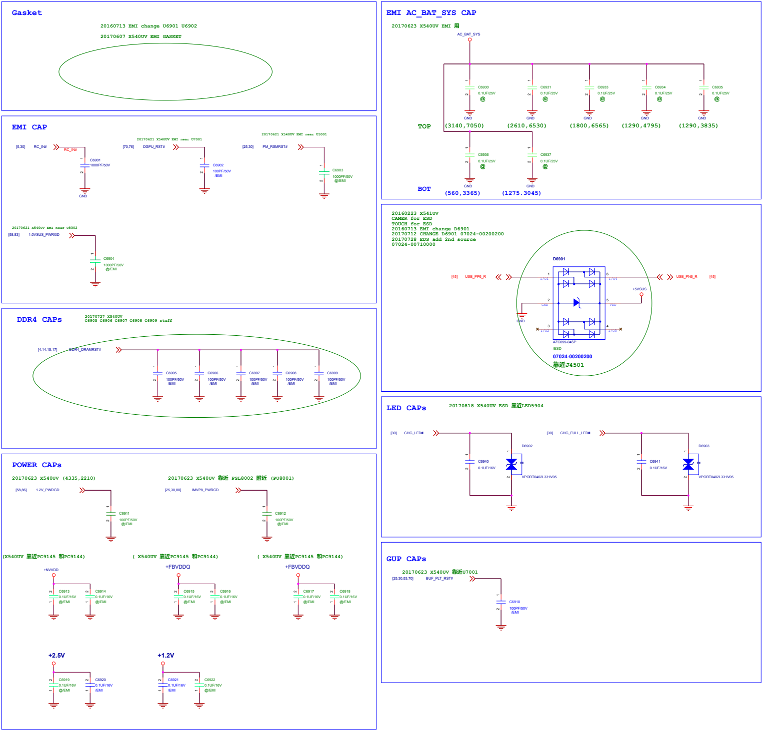
20160630 X541UAK/UVK follow X441 change FPC Connector
20170601 X540UV 20PIN FPC

20170720 X540UV Del
zero power ODD function
20170821 X540UV unstuff R6803



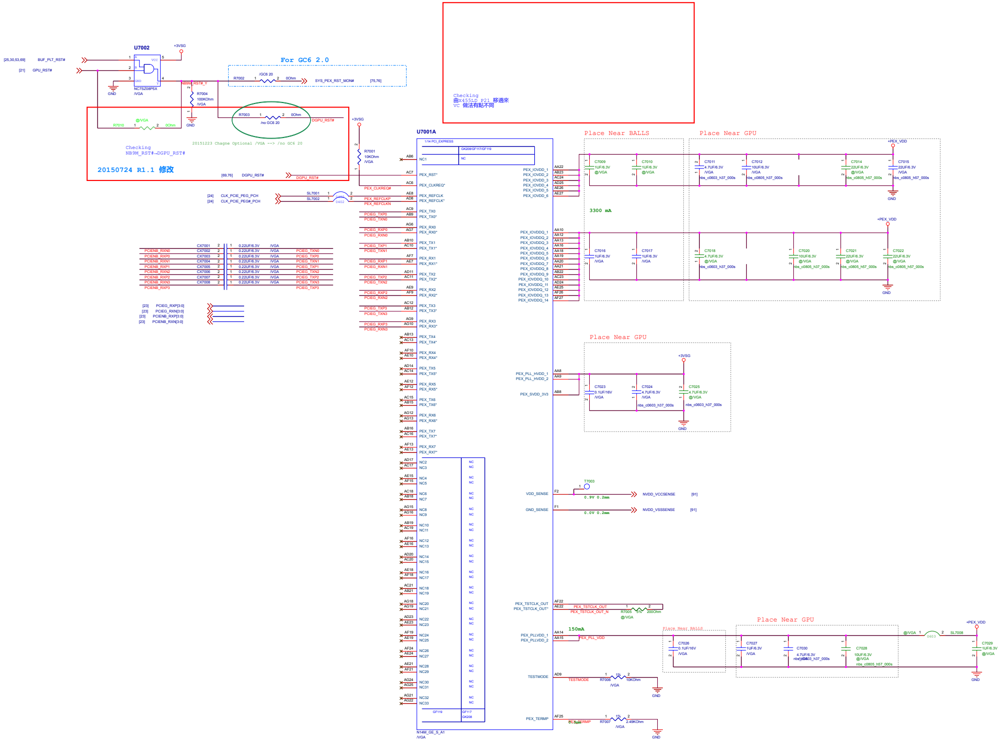
BOM

ASUS	Project Name X540UPR	Rev R1.0
Title : B TO B CONNECTOR		
Size B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 68	of 99



BOM

Project Name	X540UPR	Rev R1.0
Title :	EMI	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 69	of 102



BOM

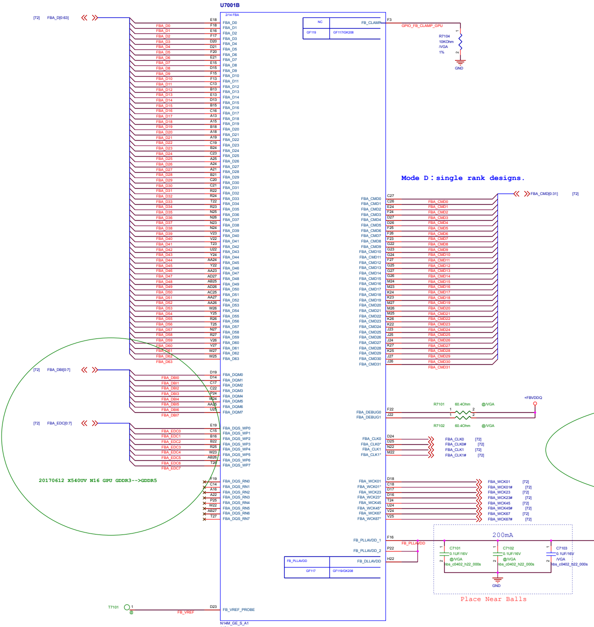
ASUS	Project Name: X540UV/UA	Rev R1.0
Title : N14M-GE_PCIE		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Monday, August 21, 2017	Sheet 70	of 99

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

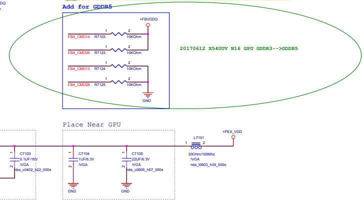
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

Note:
- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.



BOM Mount: 02004-00300400

Add for GDDR5



<Variant Name>

Project Name	X540UV/UA	Rev R1.0
Title :	N14M-GE_FB-IF	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Monday, August 21, 2017	Sheet 71 of 99	

FBA Partition Memory (1 of 2)

MF=0 Normal

FBA Partition Memory (2 of 2)

MF=1 Mirror

CMD mapping mode H

GB2-64 GB4-128*	CH0 0...31
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	ABI#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#

CMD mapping mode H

GB2-64 GB4-128*	CH1 32...63
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	ABI#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#

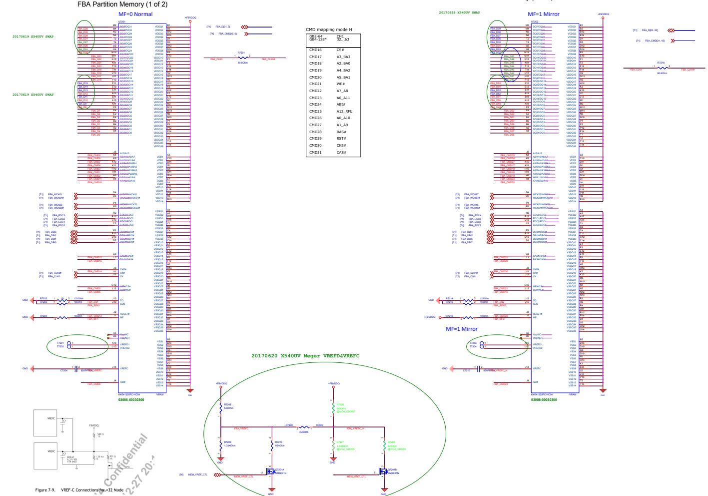


Figure 7-9. VREF-C Connections for ×32 Mode

GDD5 MODE SELECTION

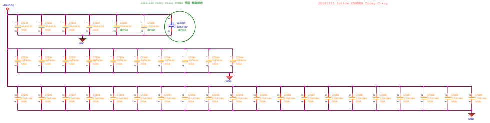
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

USE GDDR5 VRAM 128Mb x 32 (512MB)
1st: P/N: 03008-00030900 HYNIX/H5GC4H24AJR-T2C(A-die) ,Strap: 0x6 (+1.35V)
2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)
3nd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, non-RVL)

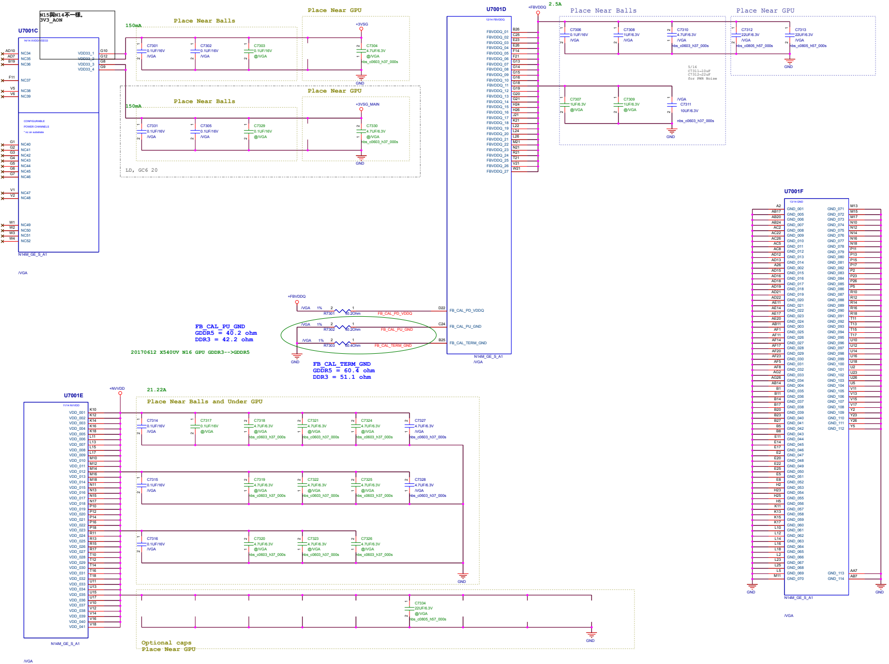
20161220 Corey Chang POWER 预留 解高频音

20161215 follow X505UA Corey Chang



<Variant Name>

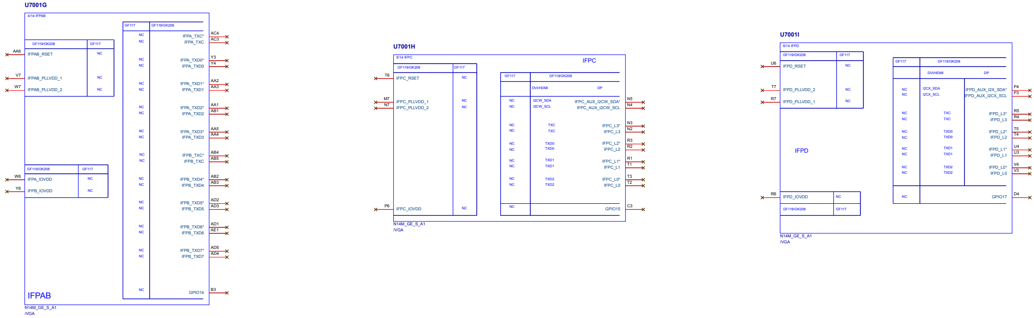
Project Name X540UV/UA		Rev R1.0
Title : DDR3L		
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: NB2_EE2	
Date: Monday, August 21, 2017	Sheet 72 of 103	

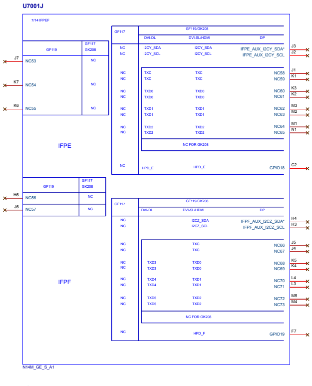


BOM

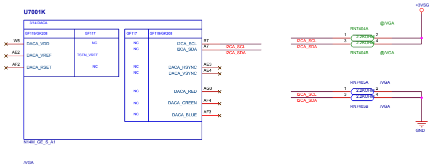
ASUS	Project Name X540UV/UA	Rev R1.0
Title : N14M-GE-VDD		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Monday, August 21, 2017	Sheet 73	of 99

LVDS





CRT



BOM

Project Name: X540UV/UA		Rev: R1.0
Title : N14M-GE_DISPLAY		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Monday, August 21, 2017	Sheet 74	of 99

Table 14. N16V-GMR1 and N16S-GMR/-GTR DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63F	F-die	0x9	900	N/A	Production ready
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x1	900	N/A	Production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0x2	900	N/A	Production ready
				Micron	MT41J256M16LY-091G:N	N-die	0x6	900	N/A	Post-production candidate
			Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0xF	900	N/A	Production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0xE	900	N/A	Production ready
				Micron	MT41J256M16LY-091G:N	N-die	0xA	900	N/A	Post-production candidate

Note: For N16V-GMR1 and N16S-GMR/-GTR, the maximum allowable memory case temperature is 85 °C.

15.5.13 SORx_EXPOSED Straps

SORx_EXPOSED is used to define audio capability on each digital display link.

Display links with audio capability should have the corresponding SORx_EXPOSED bit set to one. These include links used for HDMI, DisplayPort, and DVI ports that can be used with a DVI-to-HDMI dongle or routed to the HDMI or DisplayPort connector on a docking station.

Display links with no audio capability should have the corresponding SORx_EXPOSED bit set to 0. These include LVDS, eDP, or unused links.

Table 15-15 shows the correlation between display configurations and the SORx_EXPOSED strap settings.

Table 15-15. SORx_EXPOSED - Display Link to Usage Bit Mapping

Displays		HDMI/DP	DVI	LVDS	eDP	Not in Use
Standard Mode	IFPAB		SOR0_EXP = 1	SOR0_EXP = 0		SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPEF	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
Split Mode AB	IFPA	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPB	SOR0_EXP = 1	SOR0_EXP = 1			SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPEF					
Split Mode EF	IFPAB					
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPE	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPF	SOR0_EXP = 1	SOR0_EXP = 1		SOR0_EXP = 0	SOR0_EXP = 0

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

15.5.14 DEVID_SEL Strap

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVID straps. This strap only exists in the GB2B-64, GB4B-128, and GB3B-256 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* document for the latest configuration.

15.5.15 PCIE_CFG Strap

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3GIO_PADCFG. This strap only exists in the GB2B-64, GB4B-128, and GB3B-256 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* document for the latest configuration.

15.5.6 SMB_ALT_ADDR Strap

This strap is used to configure the address of the I²C slave device on the GPU's I²CS interface.

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

15.5.5 VGA_DEVICE Strap

The VGA_DEVICE strap is used to identify the device type (or class code) of the GPU within the PCI configuration space. Set 3D Acceleration Device for GPU in Optimus configuration or secondary GPU in SLI configuration.

Table 15-7. VGA_DEVICE Settings

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device (Class Code 302h)
1	Primary Display or VGA Device (Class Code 300h)

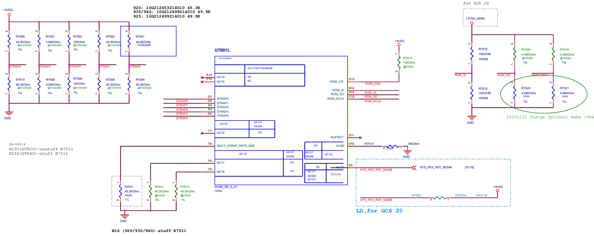
Table 15-1. Device Specific Strap Mode Selection

	All N16x GPUs
Multi_Strap_Ref0_GND	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 40.2k 1% to GND

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

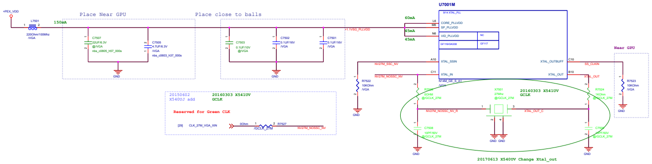
	Size	Part Number			Strap		ROM_SI
VRAM	128x16b (2Gb)	03007-00030400	gDDR3 128M*16 1.35V FBGA-96	MICRON/MT41J128M16JT-093G:K	0xA	1010	PU 15K Ohm
	256x16b (4Gb)	03007-00021100	GDDR3 256M*16-1.35V FBGA96	HYNIX/H5TC4G63CFR-N0C	0x2	0010	PD 15K Ohm
		03007-00021300	GDDR3 256M*16 1.35V FBGA96	MICRON/MT41J256M16LY-091G:N	0x6	0110	PD 34K Ohm



VG BOM 帶入主料時記得要加2nd Source

4.99K = 10G212499114010
10K = 10G212100214010
15K = 10G212150214030
20K = 10G212200214030
24.9K = 10G212249214010
30.1K = 10G212301214010
34.8K = 10G212348214010
45.3K = 10G212453214010
49.9K = 10G212499214010

Xtal



BOM

	Project Name	Rev
ASUS	X540UV/UA	R1.0
Title :	N14M-GE_ROM,XTAL	
Size D	Dept.: ASUSTeK COMPUTER INC. Engineer: NB2_EE2	
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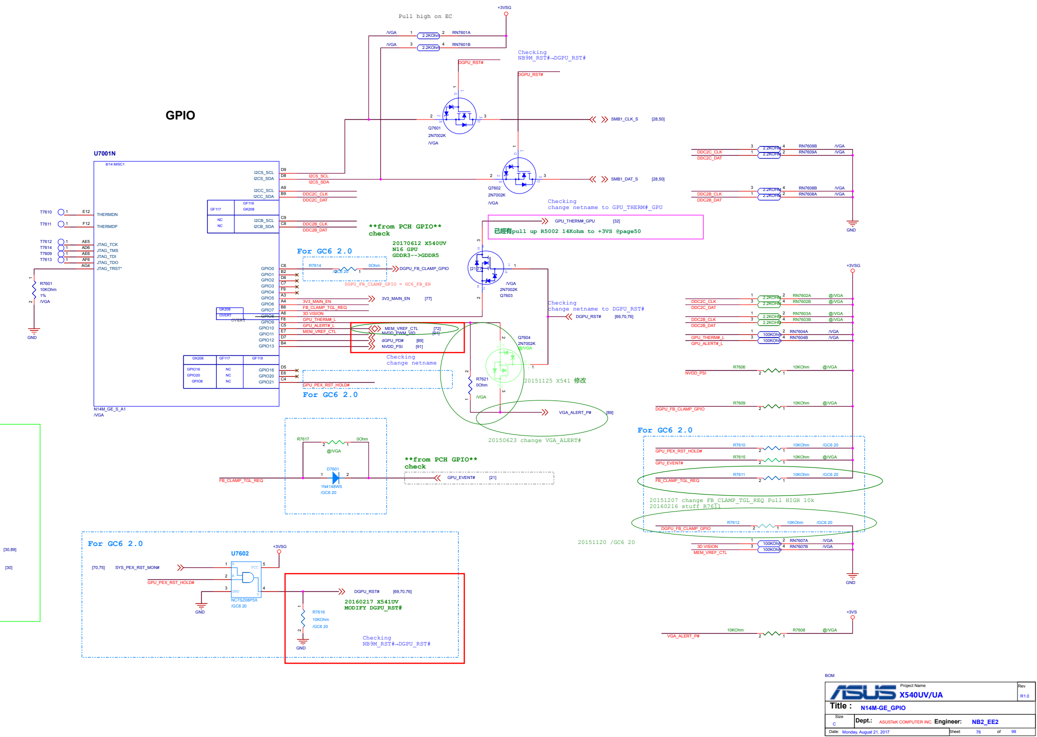
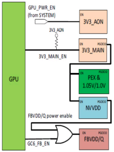
Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdrawn input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON





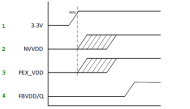
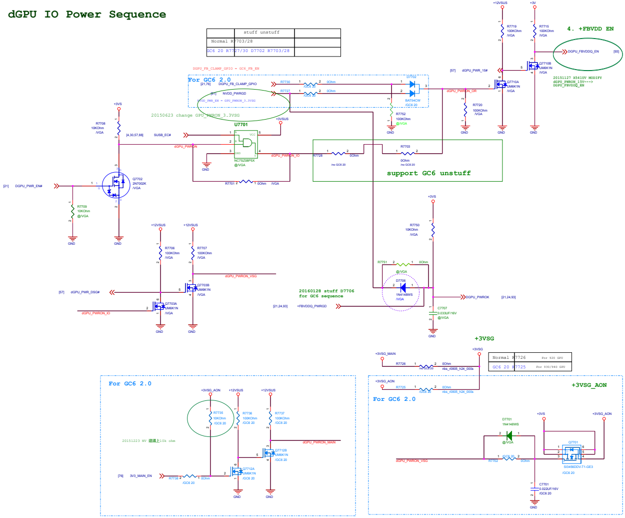
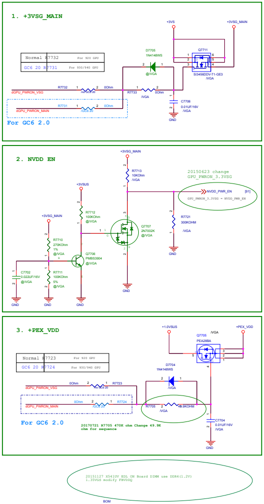


Figure 3-7. Example of Power-Up Sequencing Order

dGPU IO Power Sequence



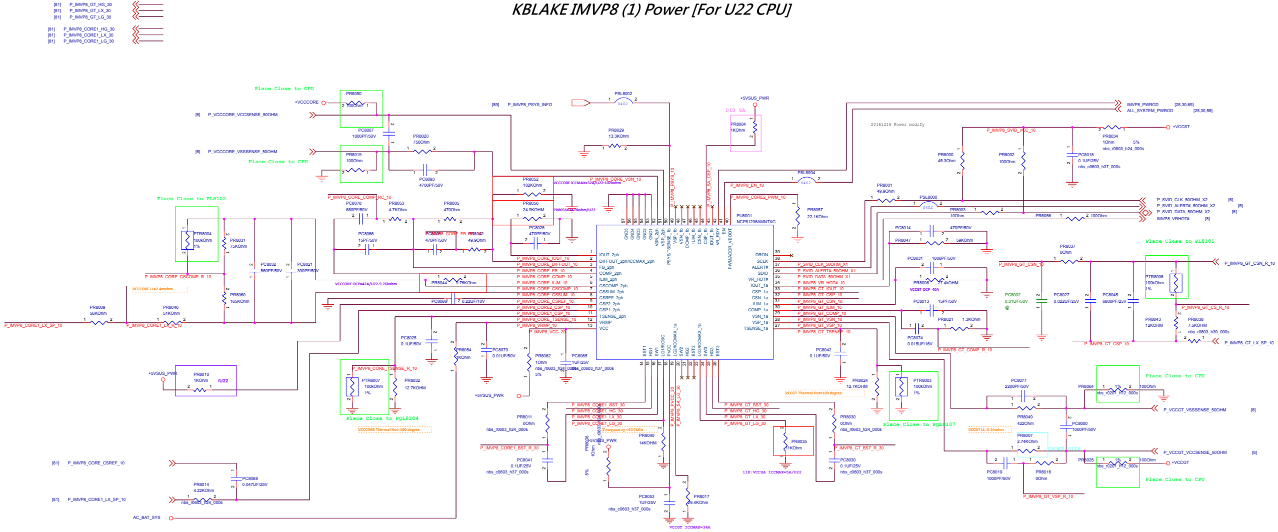
dGPU Core Power Sequence



BOM

ASUS	Project Name: X540UV/UA		Rev R1.0
Title : N14M-GE_POWER			
Size C	Dept.: ASUSTeK COMPUTER INC	Engineer: NB2_EE2	
Date: Monday, August 21, 2017	Sheet 77	of 99	

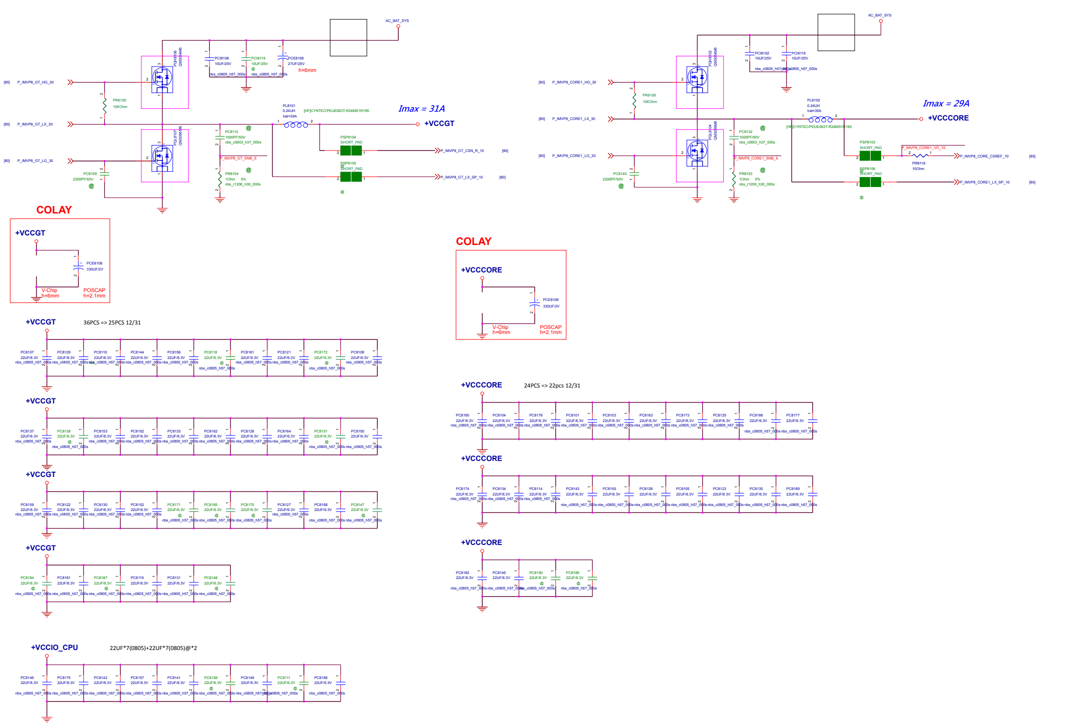
KBLAKE IMVP8 (1) Power [For U22 CPU]



<Variant Name>

ASUS	Project Name: X540UVK	Rev: R0.1
Title : PW_SKYLAKE-U (1)		
Size: A2	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 80 of 102	

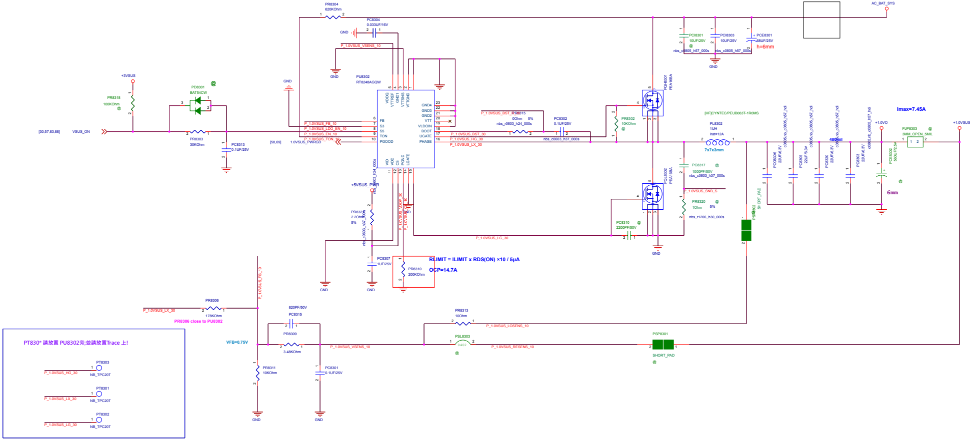
Skylake IMVP8 Power (2) [For CPU]



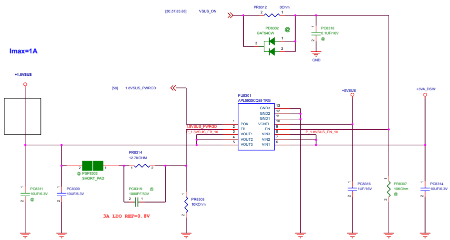
BOM

ASUS	Project Name: X540UVK	Rev: R0.1
Title: PW_SKYLAKE-U (2)		
Size: C	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 81 of 102	

+1.0VSUS (RT8248AGQW)



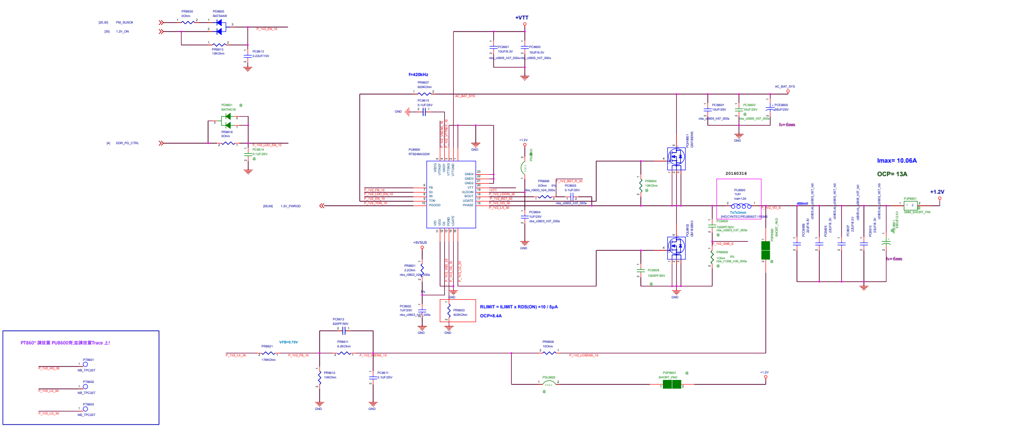
+1.8VSUS [For PCH]



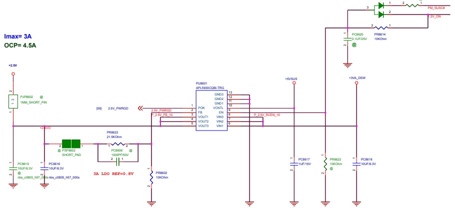
<Variant Name>

ASUS	Project Name: X540UVK	Rev: R0.1
Title : PW_+1.0VSUS / +1.8VSUS		
Size: C	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 83 of 102	

+1.2V / +VTT / +2.5V[For Memory]



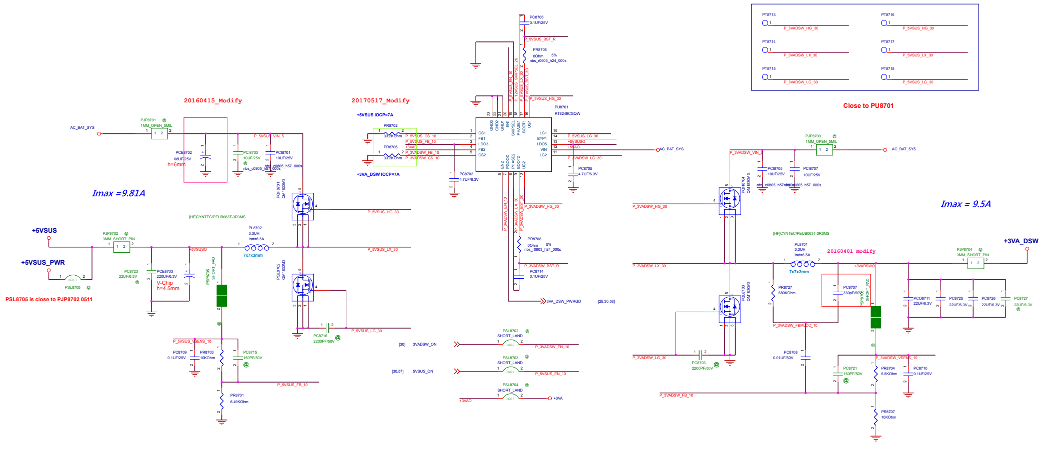
+2.5V

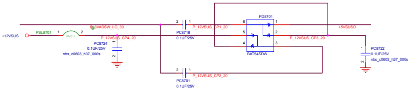


<Core Design>

ASUS	Project Name: X540UVK	Rev: R0.1
Title :	PW_+1.2V/+VTT/+2.5V	
Size: A2	Dept.: NB Power team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 86	of 102

+3VA_DSW / +5VSUS [System Power]





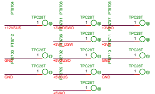
請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

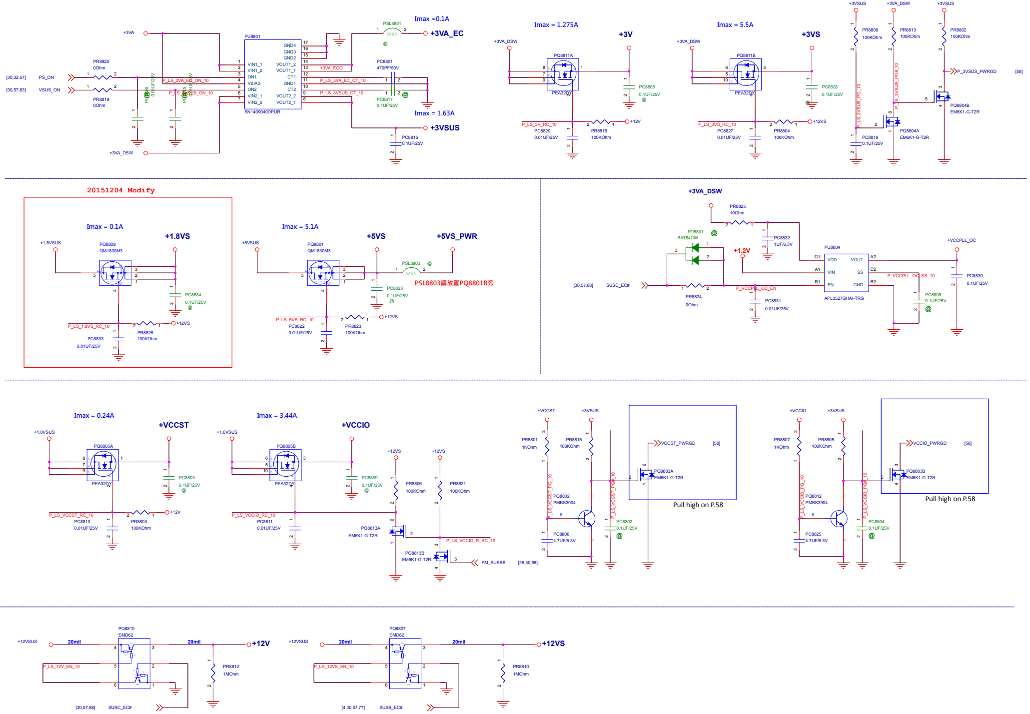
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



BOM

Project Name: X540UVK		Rev: R0.1
Title : PW_+3VA_DSW/+5VSUS		
Size: Custom	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 87 of 102	

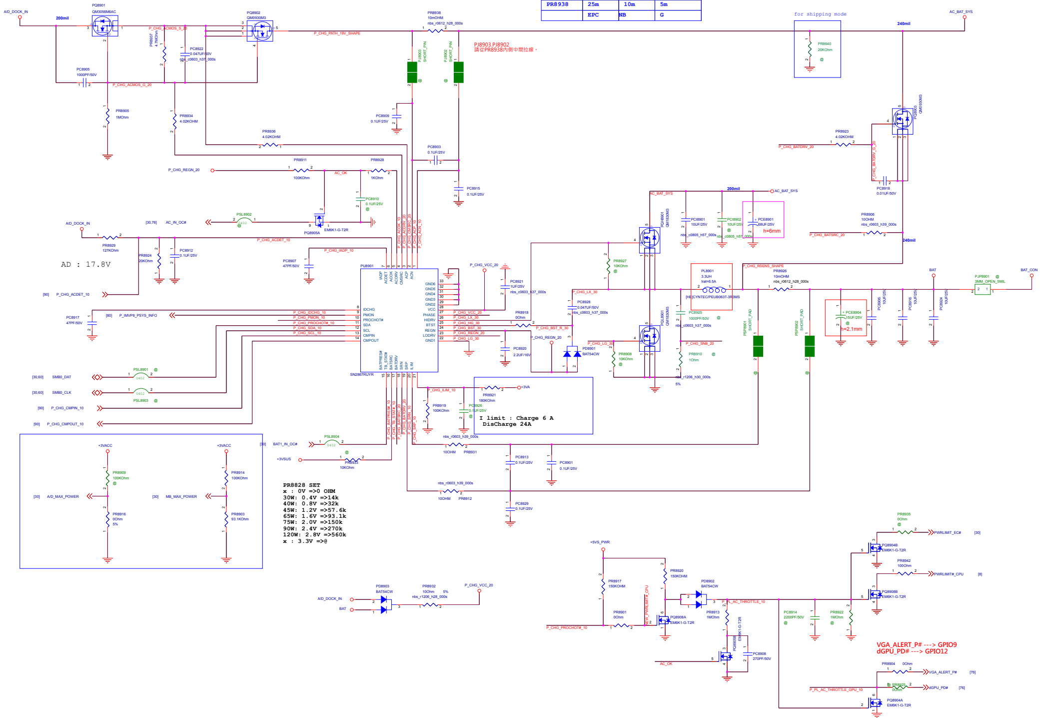
Load Switch



BOM

Project Name	X540UVK	Rev R0.1
Title :	PW_LOAD_SWITCH	
Size Custom	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 88 of 102	

	<=40W	<=120W	>=120W
PR8938	25m	10m	5m
	EPC	NB	G



BOM

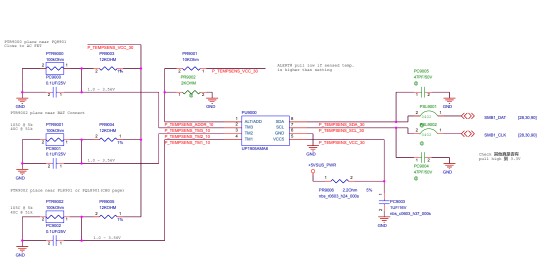
ASUS	Project Name: X540UVK	Rev: R0.1
Title : PW_CHARGER		
Size: A2	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 89 of 102	

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

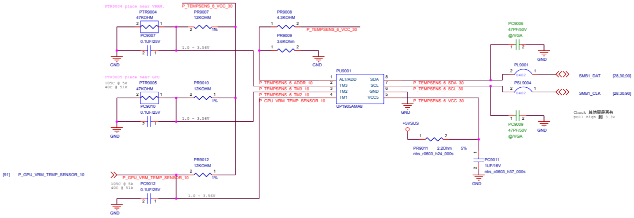
Register Address

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

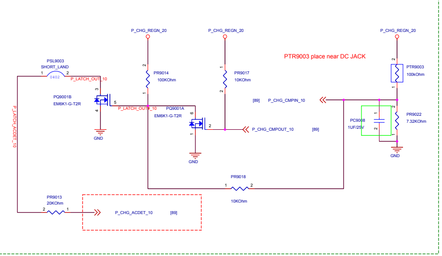


Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9008	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9009	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



DC Jack Thermal Latch

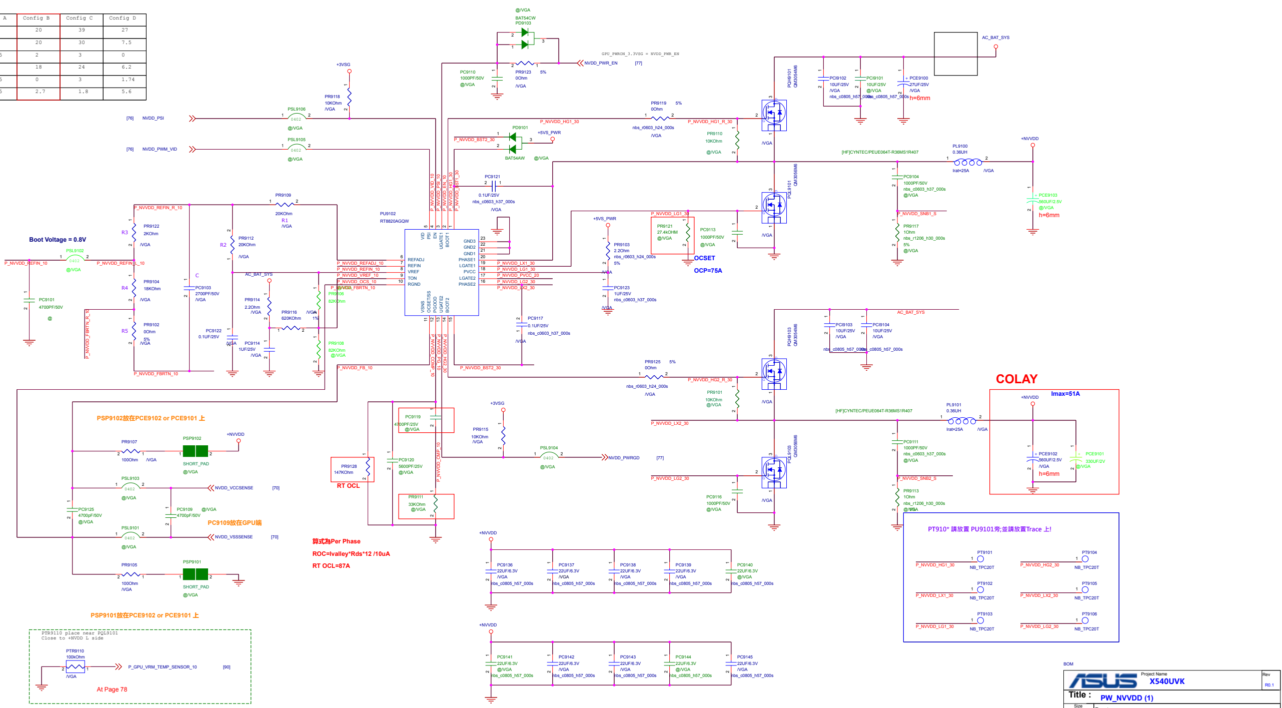


<Variant Name>

ASUS	Project Name: X540UVK	Rev: R0.1
Title : PW_PROTECTION		
Size: A2	Dept.: NB Power Team	Engineer: Andy
Date: Monday, August 21, 2017	Sheet 90 of 102	

PWM-VID Spec

	Config A	Config B	Config C	Config D
R1 (kR)	39	20	39	27
R2 (kR)	39	20	30	7.5
R3 (kR)	1.5	2	3	0
R4 (kR)	30	18	24	6.2
R5 (kR)	1.5	0	3	1.74
C (nF)	1.5	2.7	1.8	5.6



BOM

Project Name	X540UVK	Rev R0.1
Title :	PW_NVVDD (1)	
Size Custom	Dept.: NB Power Team	Engineer: Andy
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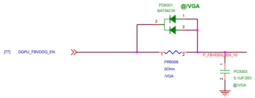
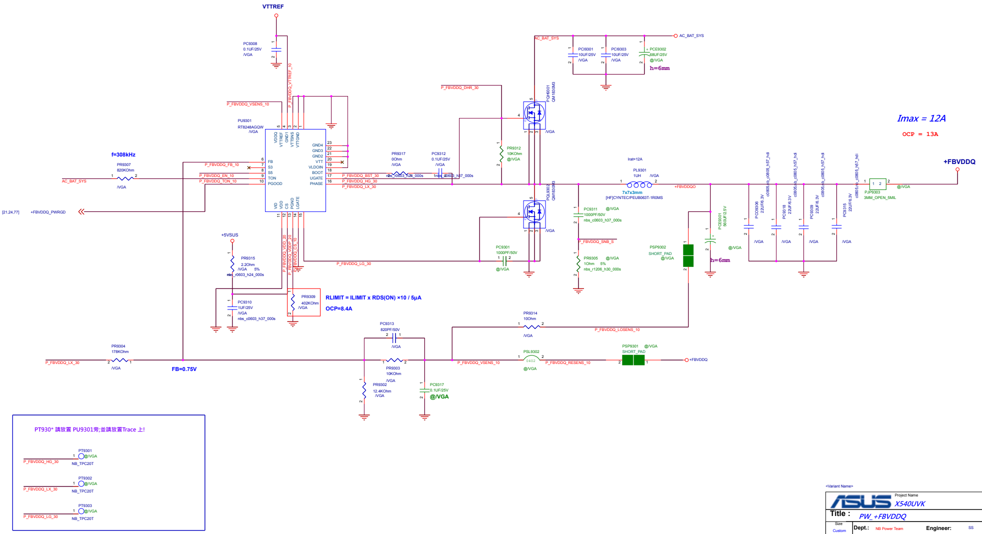
S3 And S5 Truth Table



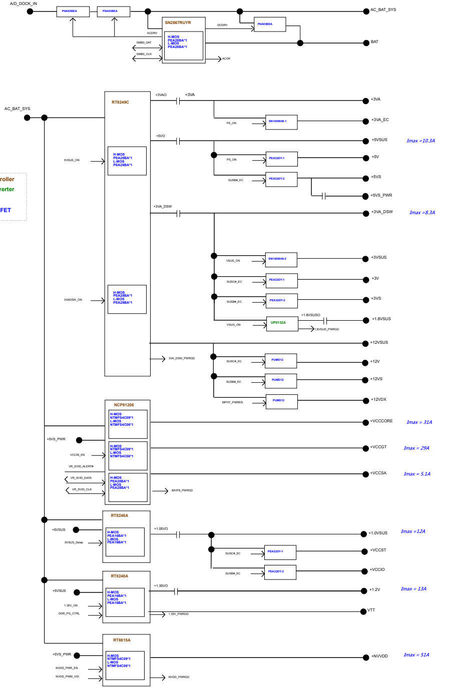
State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+FBVDDQ
[For FRAM]



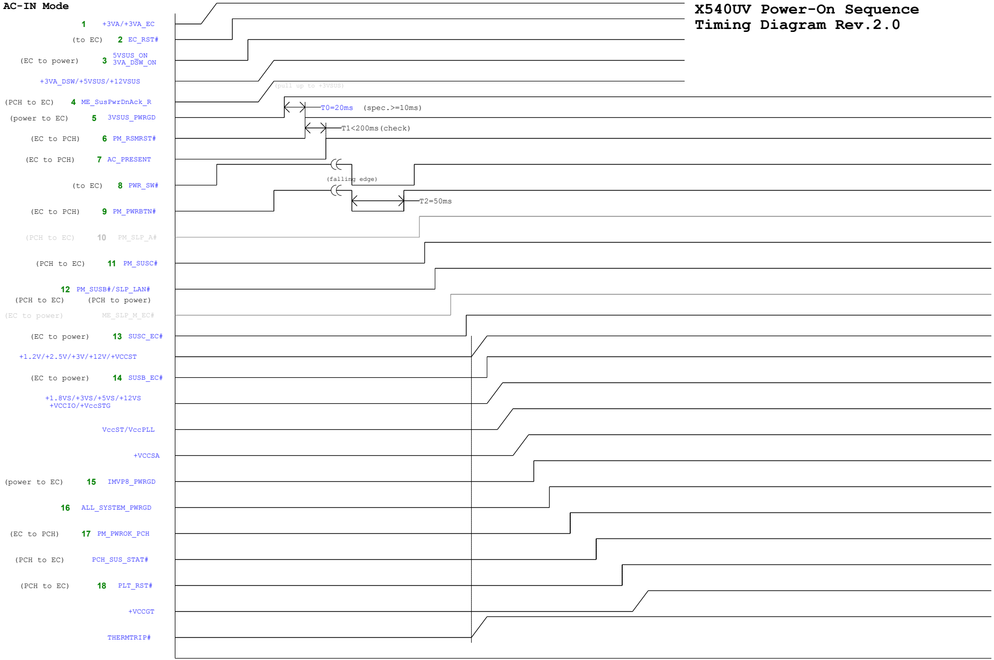
<Variant Name>

ASUS	Project Name: X540UVK	Rev: R0.1
Title : PW_+FBVDDQ		
Size: Custom	Dept.: NB Power Team	Engineer: SS
Date: Monday, August 21, 2017	Sheet 93 of 102	



ASUS	Project Name X540UVK		Rev R1.0
Title : PW_FLOWCHART			
Size Custom	Dept.: NB Power Team	Engineer: Andy	
Date: Monday, August 21, 2017	Sheet 89	of 102	

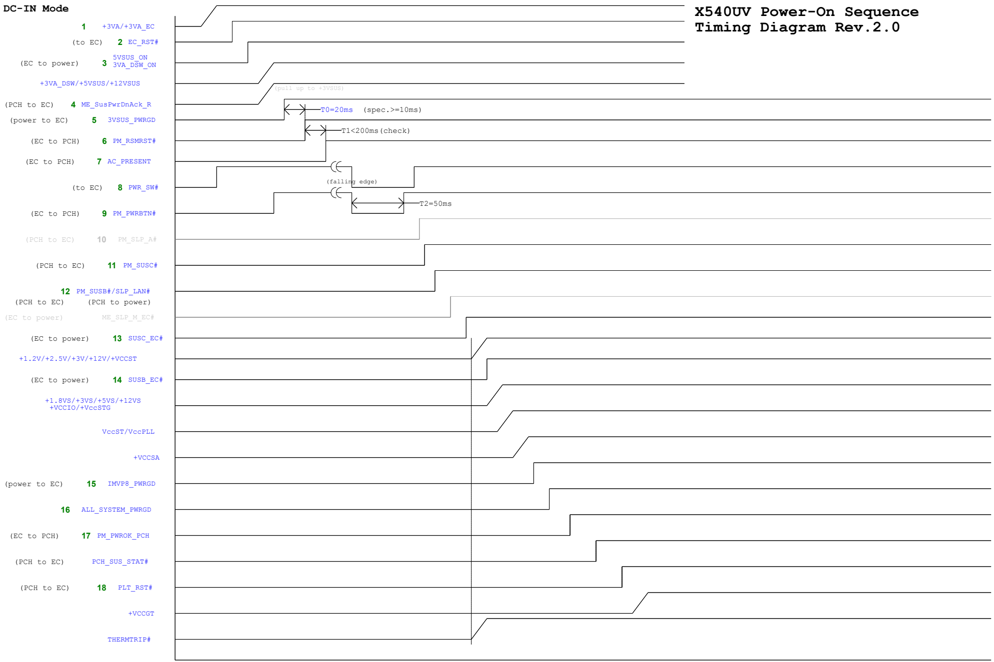
X540UV Power-On Sequence Timing Diagram Rev.2.0



BOM

ASUS	Project Name: X540UPR	Rev: R1.0
Title : Power On Timing		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Monday, August 21, 2017	Sheet 100 of 102	

X540UV Power-On Sequence Timing Diagram Rev.2.0



BOM

ASUS	Project Name X540UPR		Rev R1.0
Title :	Power On Timing		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE	
Date: Monday, August 21, 2017	Sheet 101	of 102	