MS-A9281

Ver: 1.1

CPU:

INTEL - Celeron 847

System Chipset:

INTEL - NM70

OnBoard Chipset:

HD Audio Codec:ALC887 CG

LAN:Realtek RTL8111E CG

SIO:FINTEK F71808AU

Main Memory:

DDRIII (800/1066MHz) * 1 (one Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:ISL95837HRZ (17W)

Other:

SATA(SATA2-300MB/s) *2
USB2.0 *4 (Rear X 2 & Side X 2)
Card Reader (JUSB)
Webcam (JCAMERA1)

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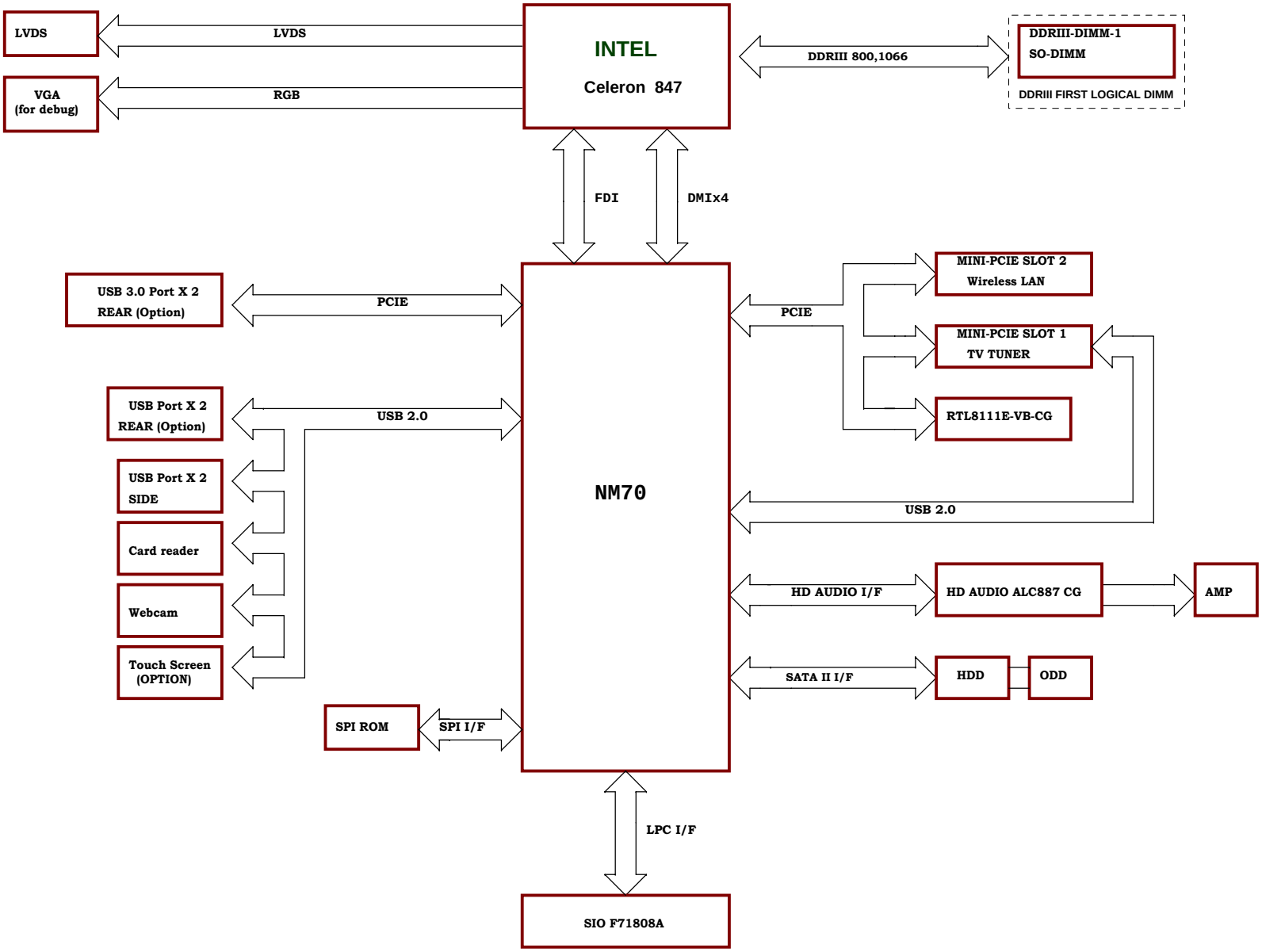
MS-A9281

Size: Custom | Document Description: Cover Sheet | Rev: 1.1

Date: Tuesday, December 18, 2012 | Sheet 1 of 42

MS-A9281 1.0



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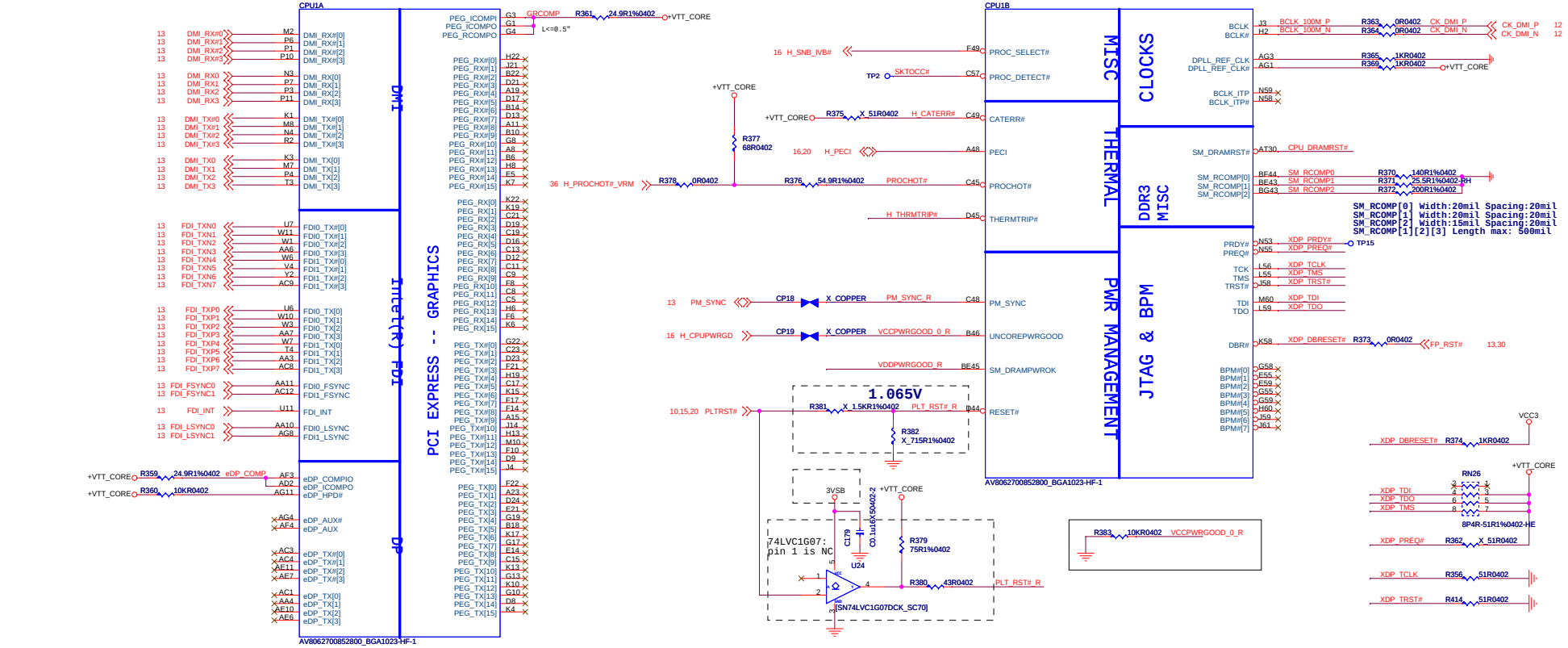
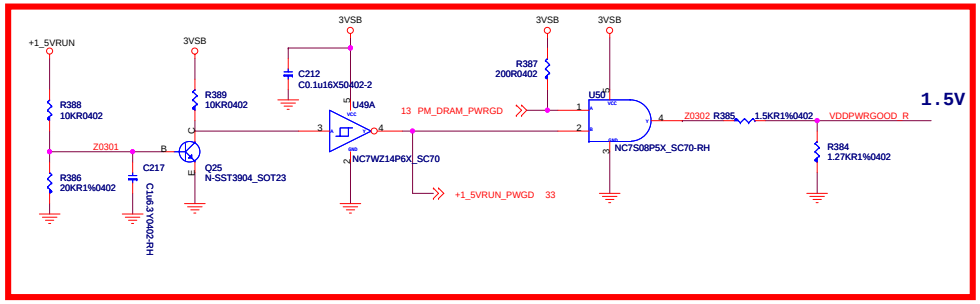
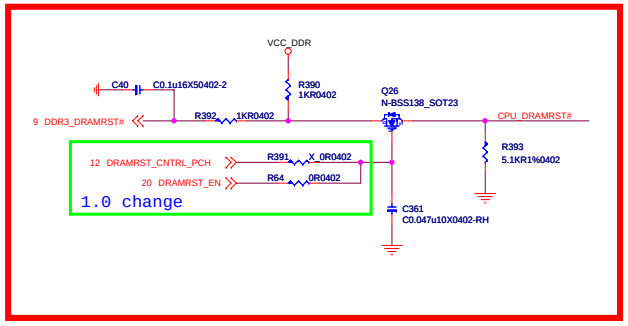
MS-A9281

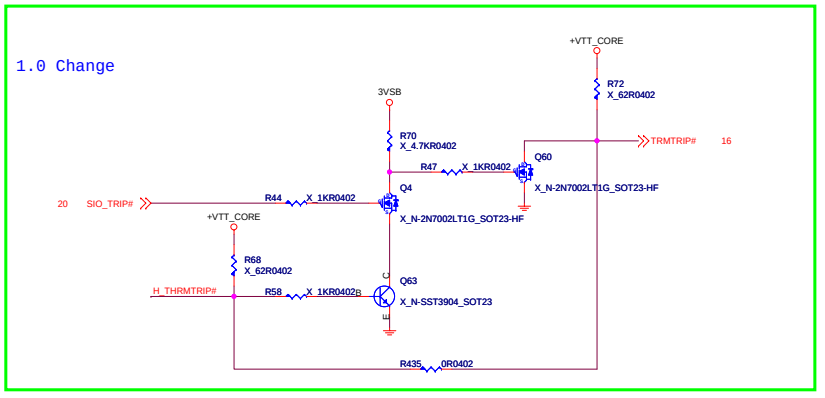
Size	Document Description	Rev
Custom	Block Diagram	1.1

Date: Tuesday, December 18, 2012 Sheet 2 of 42

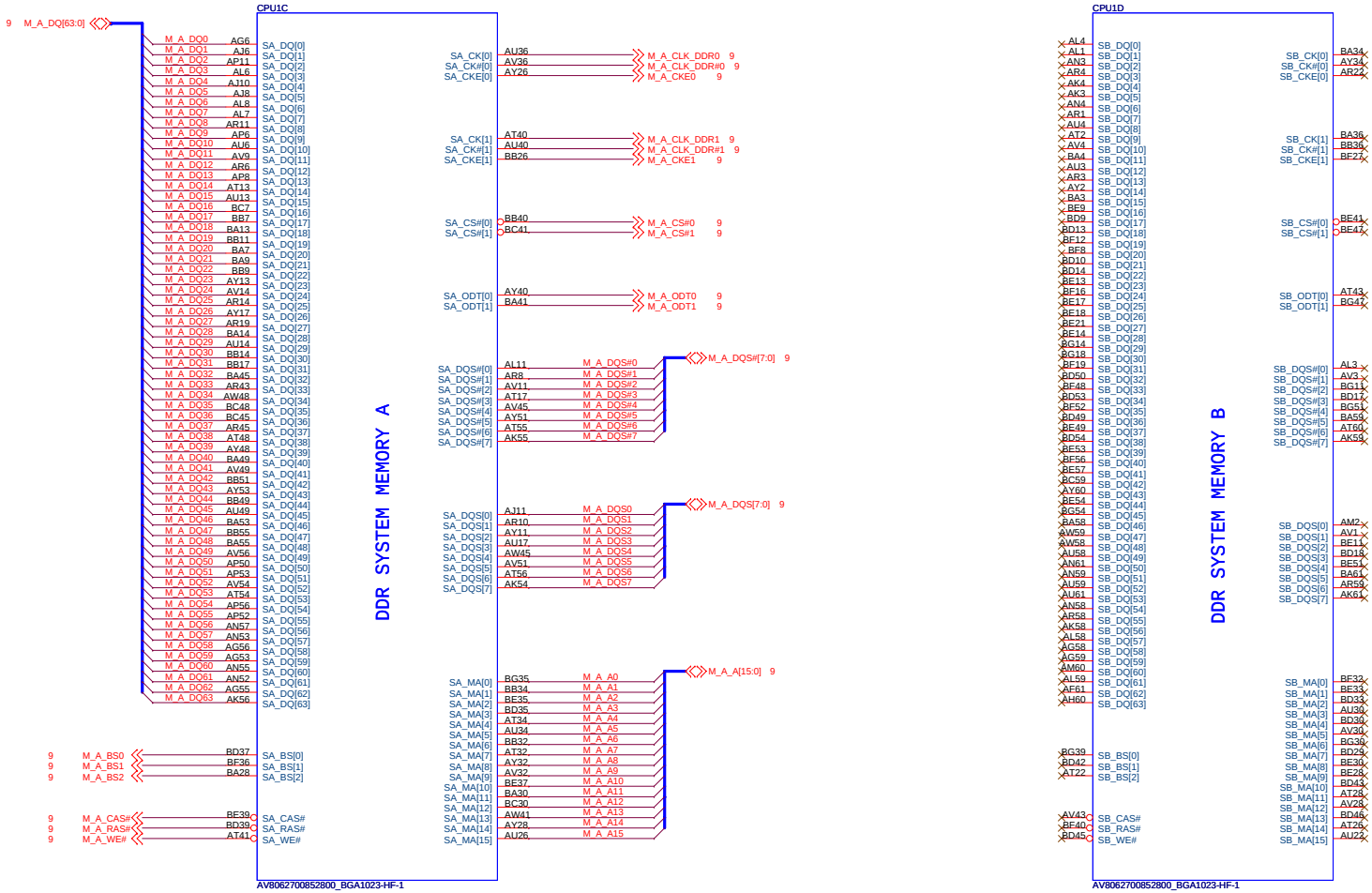








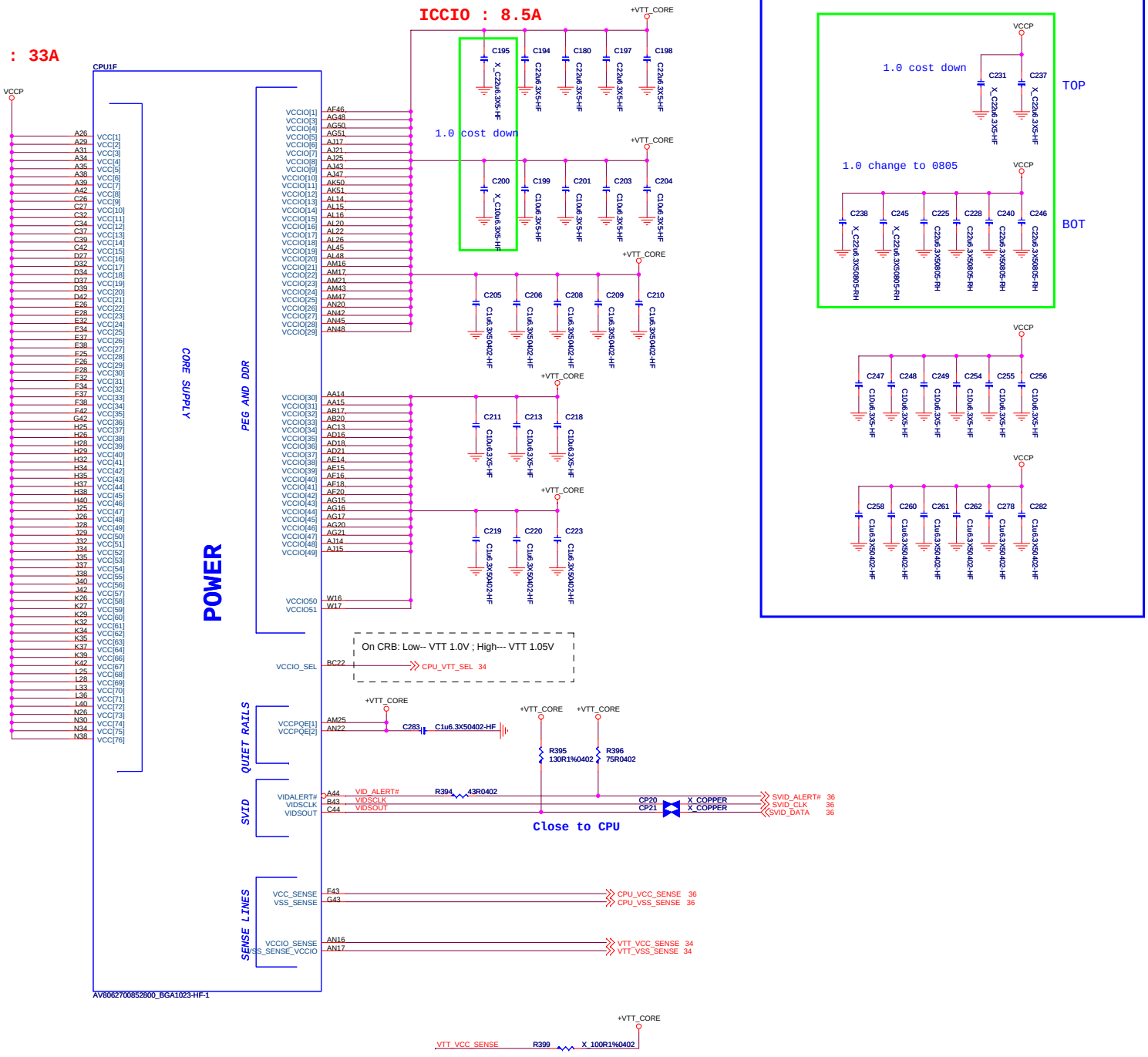
MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: C	Document Description: PROCESSOR-1 (HOST BUS & XDP)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 3 of 42	



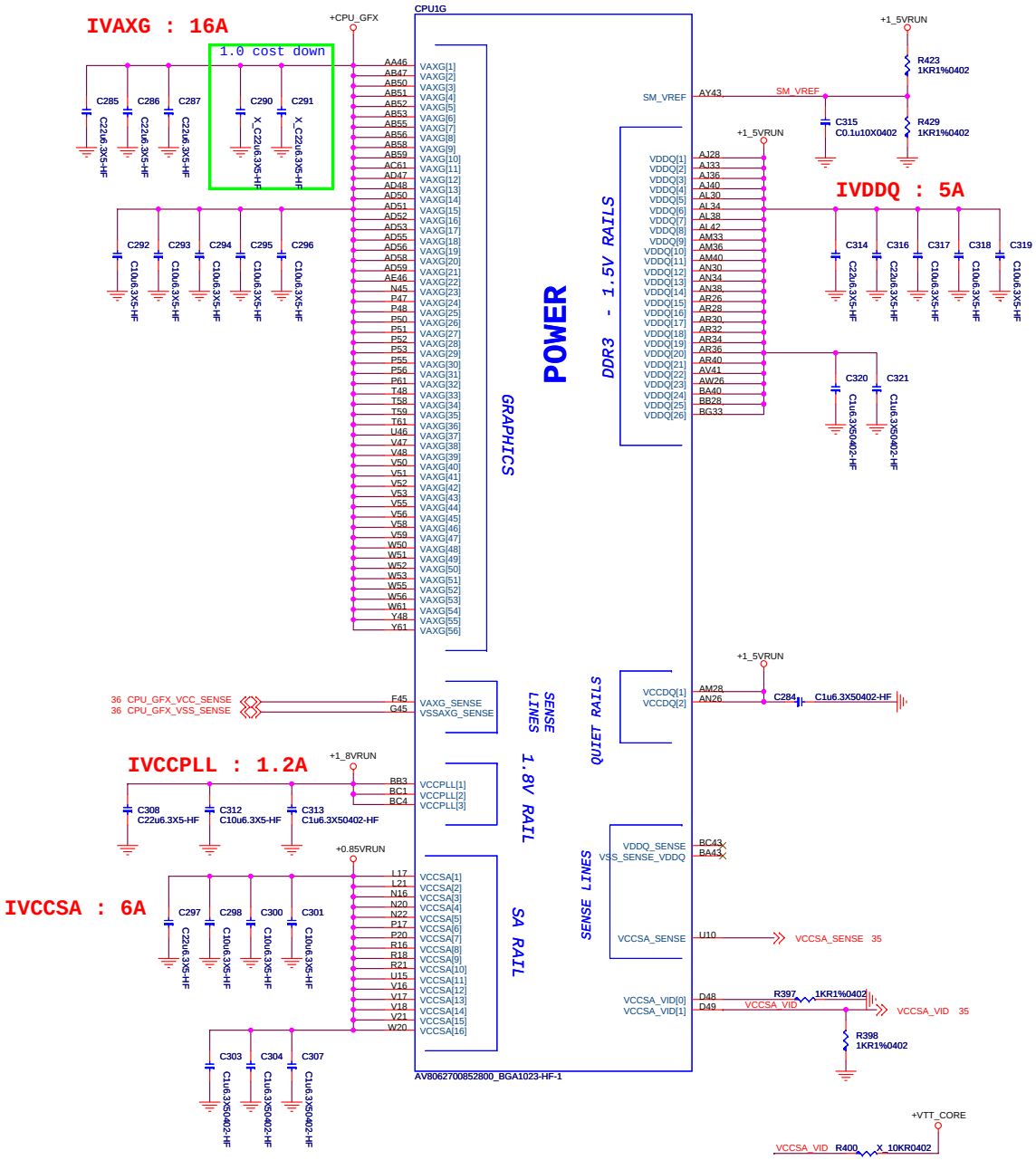
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A9281	
Size: Custom	Document Description: PROCESSOR-2 (DDR3)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 4 of 42	

ICC (MAX) : 33A

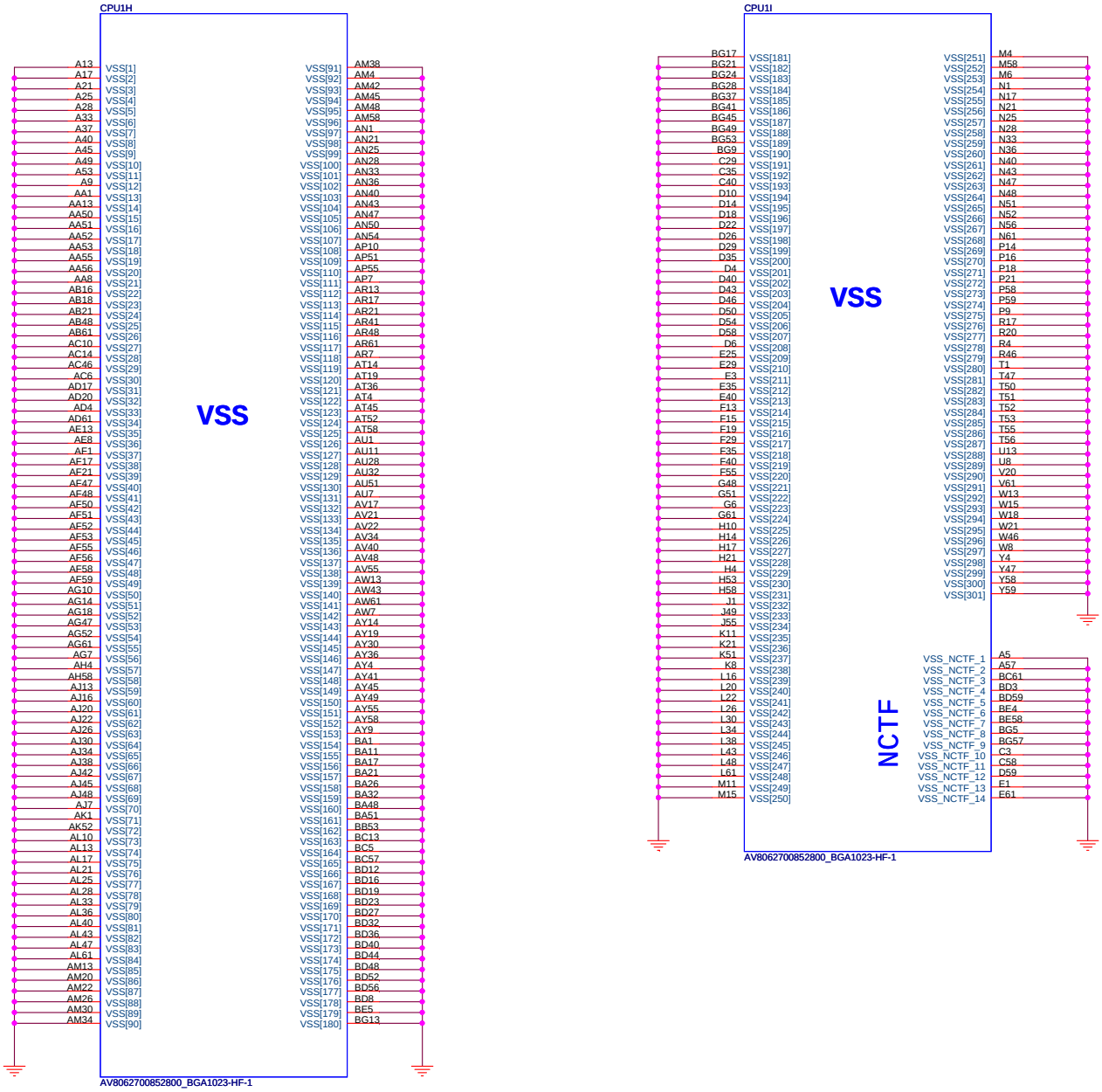
ICCIO : 8.5A



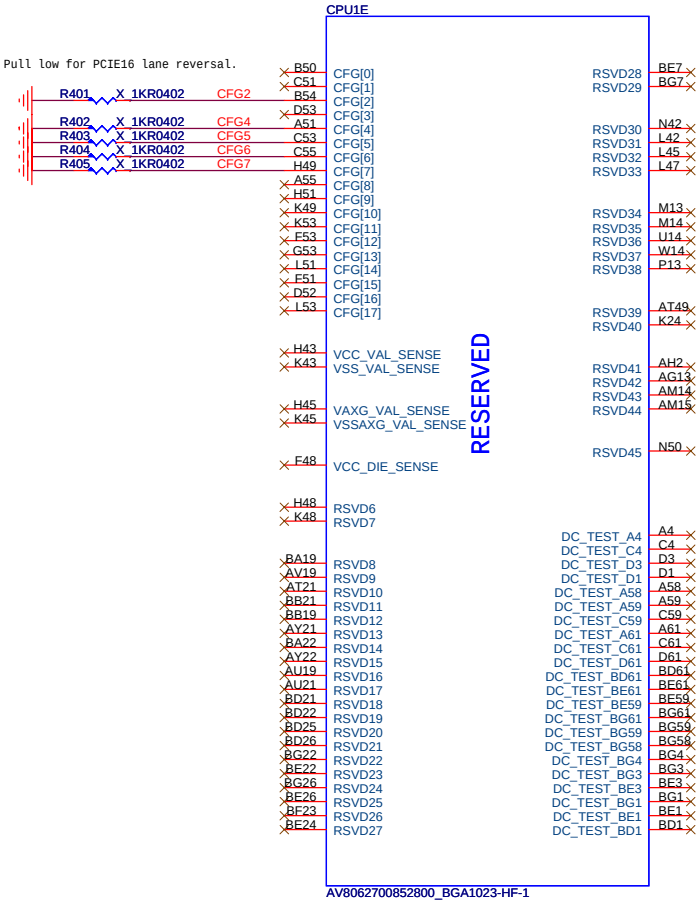
MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: PROCESSOR-3 (POWER)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 5 of 42	



MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: Custom	Document Description: PROCESSOR-4 (GRAPHICS POWER)
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet 6 of 42



MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: Custom	Document Description: PROCESSOR-5 (GND)
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet 7 of 42



CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING	
CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

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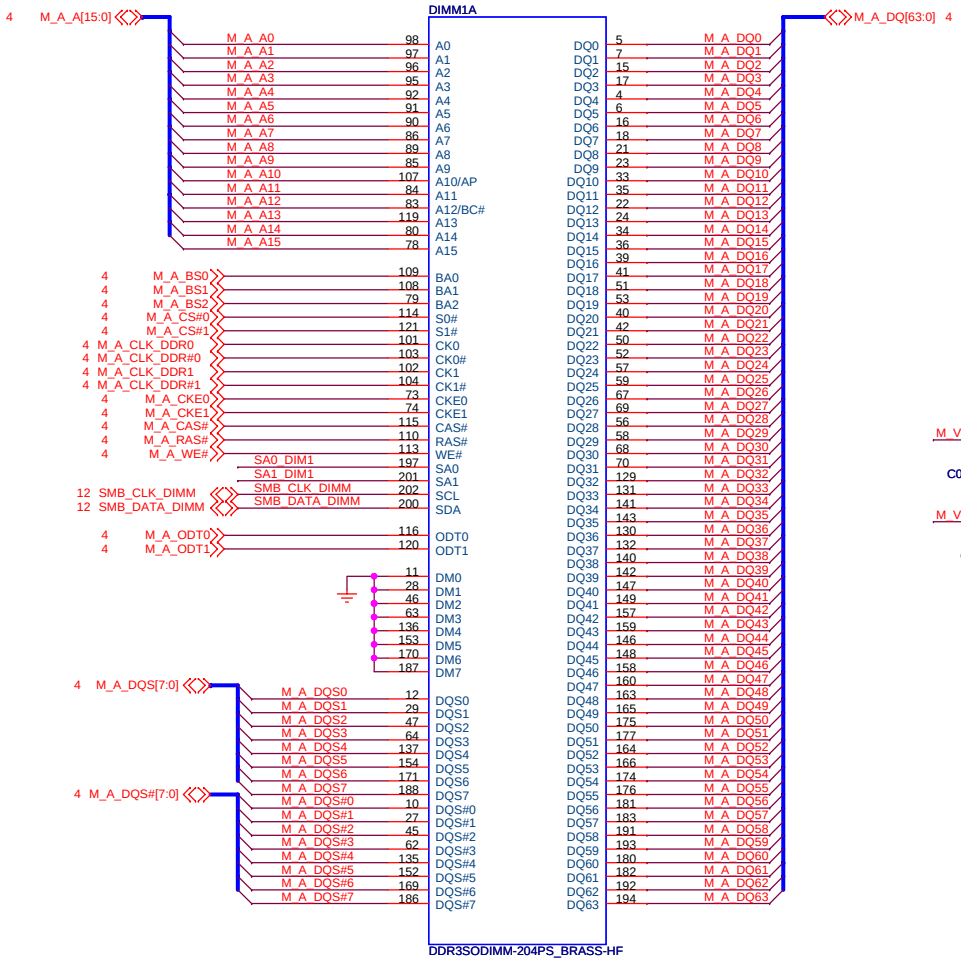
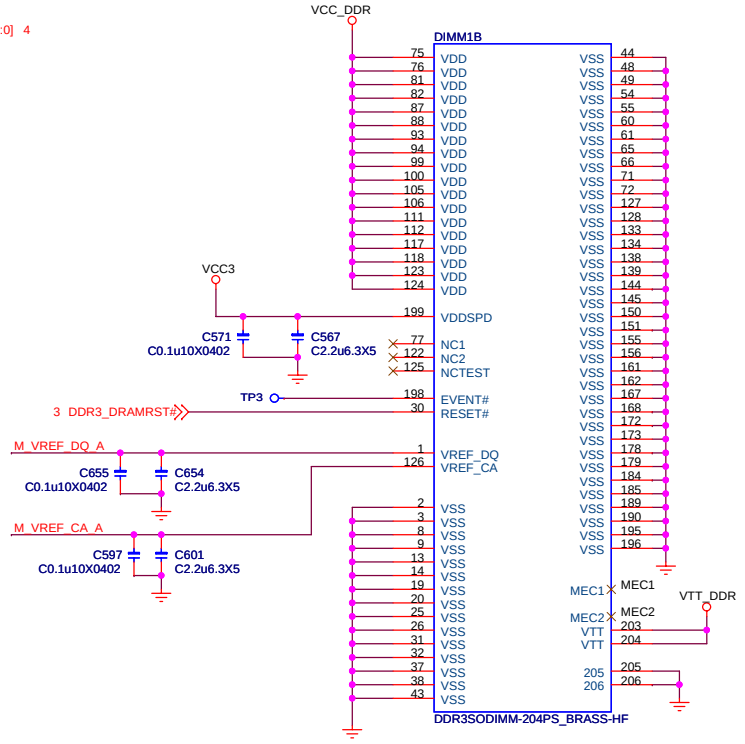
MS-A9281

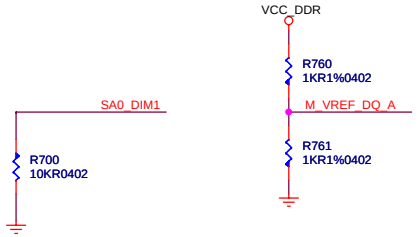
Size	Document Description	Rev
Custom	PROCESSOR-6 (RESERVE)	1.1

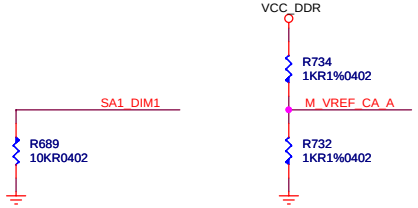
Date: Tuesday, December 18, 2012 Sheet 8 of 42

SODIMM#A



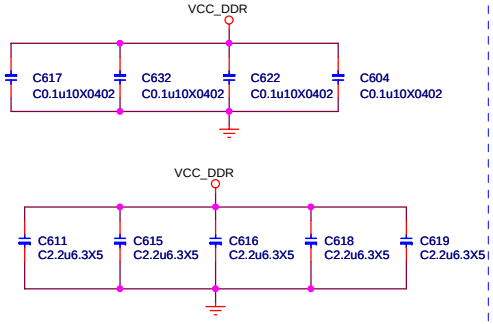




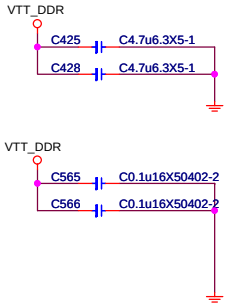


ADDRESS: 000
0xA0

Layout note: Place capacitors between and near DDR connector if possible.



CHANNEL A V_SM_VTT DECOULPING CAPS



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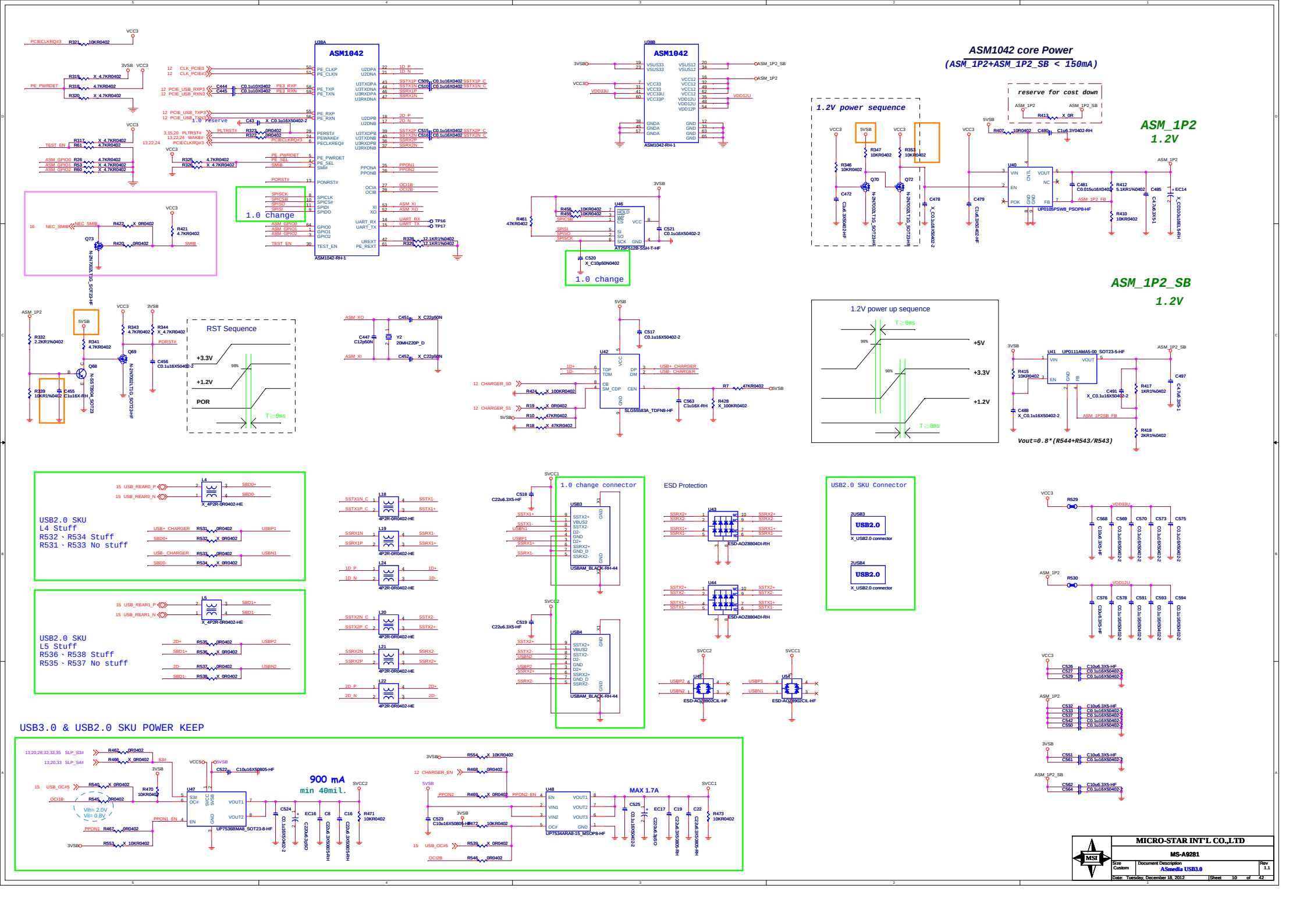
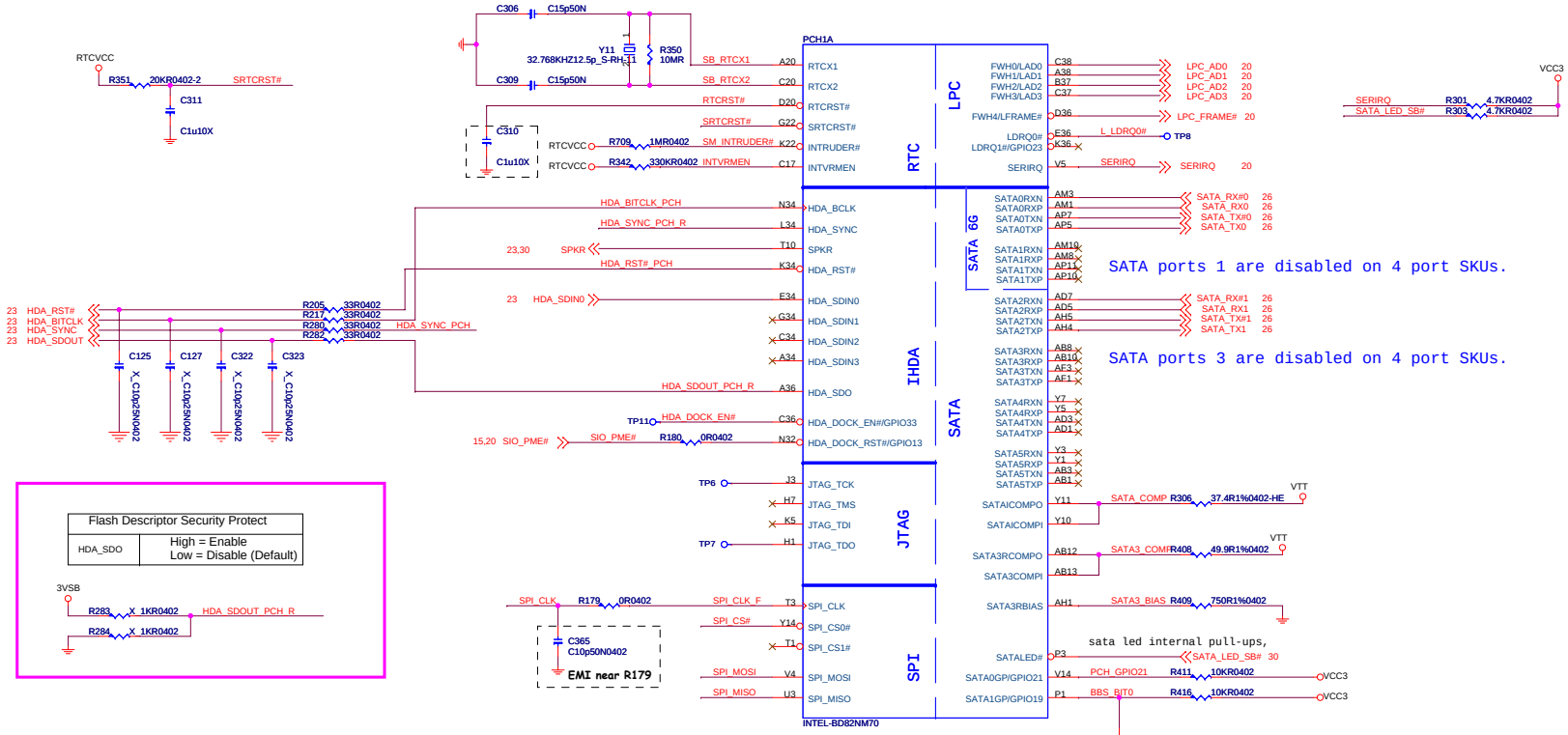
MS-A9281		
Size: Custom	Document Description: DDR III SODIMM 1	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 9 of 42	


ASM1042 core Power
(ASM_1P2+ASM_1P2_SB < 150mA)
ASM_1P2
1.2V
ASM_1P2_SB
1.2V
1.2V power sequence
reserve for cost down
1.2V power up sequence
RST Sequence
1.0 change
1.0 change connector
ESD Protection
USB2.0 SKU Connector
USB2.0 SKU
L4 Stuff
R532、R534 Stuff
R531、R533 No stuff
USB2.0 SKU
L5 Stuff
R536、R538 Stuff
R535、R537 No stuff
USB3.0 & USB2.0 SKU POWER KEEP
900 mA
min 40mil.
MAX 1.7A
Vout=0.8*(R544+R543/R543)
MICRO-STAR INT'L CO.,LTD
MS-A9281
ASmedia USB3.0



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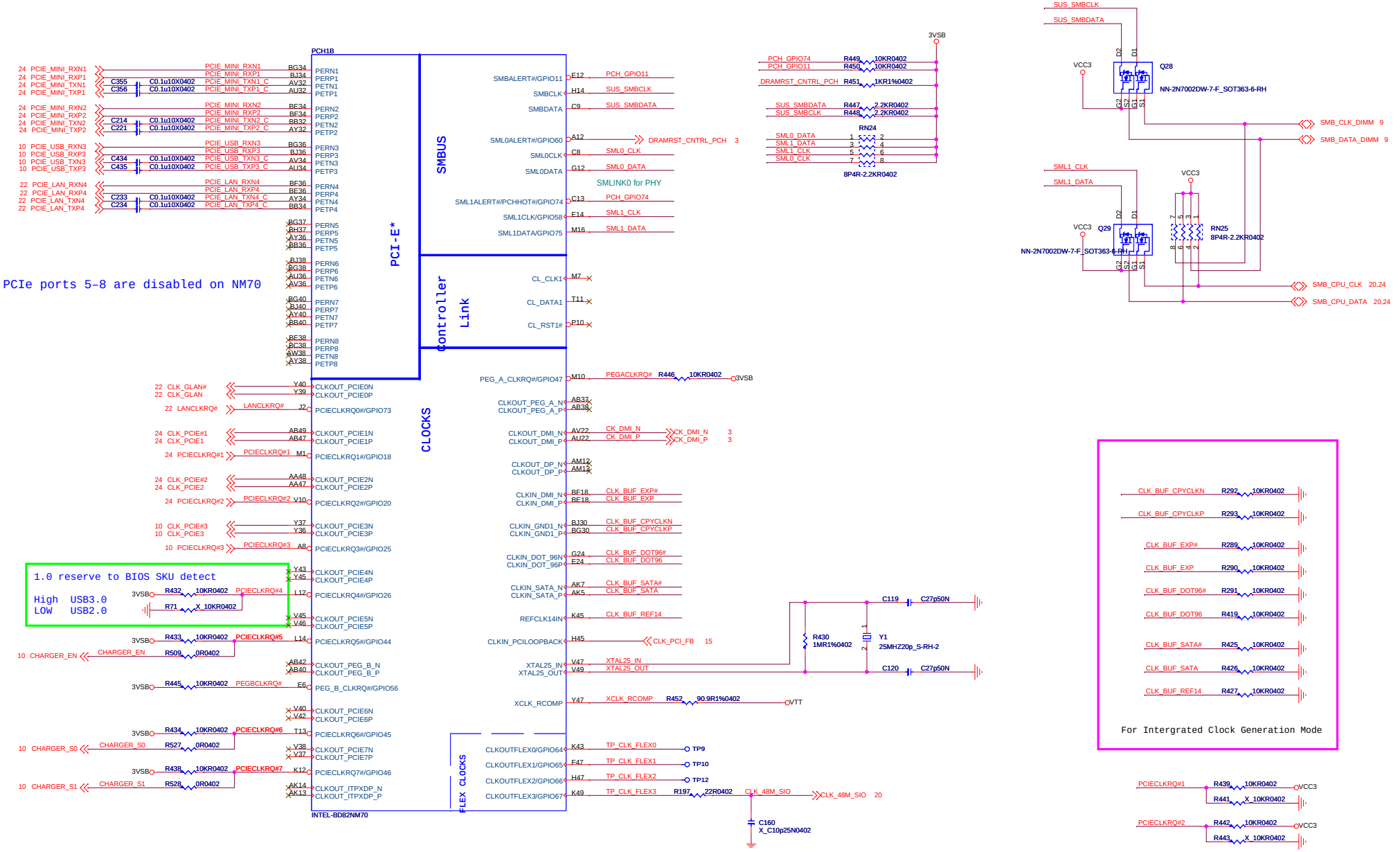
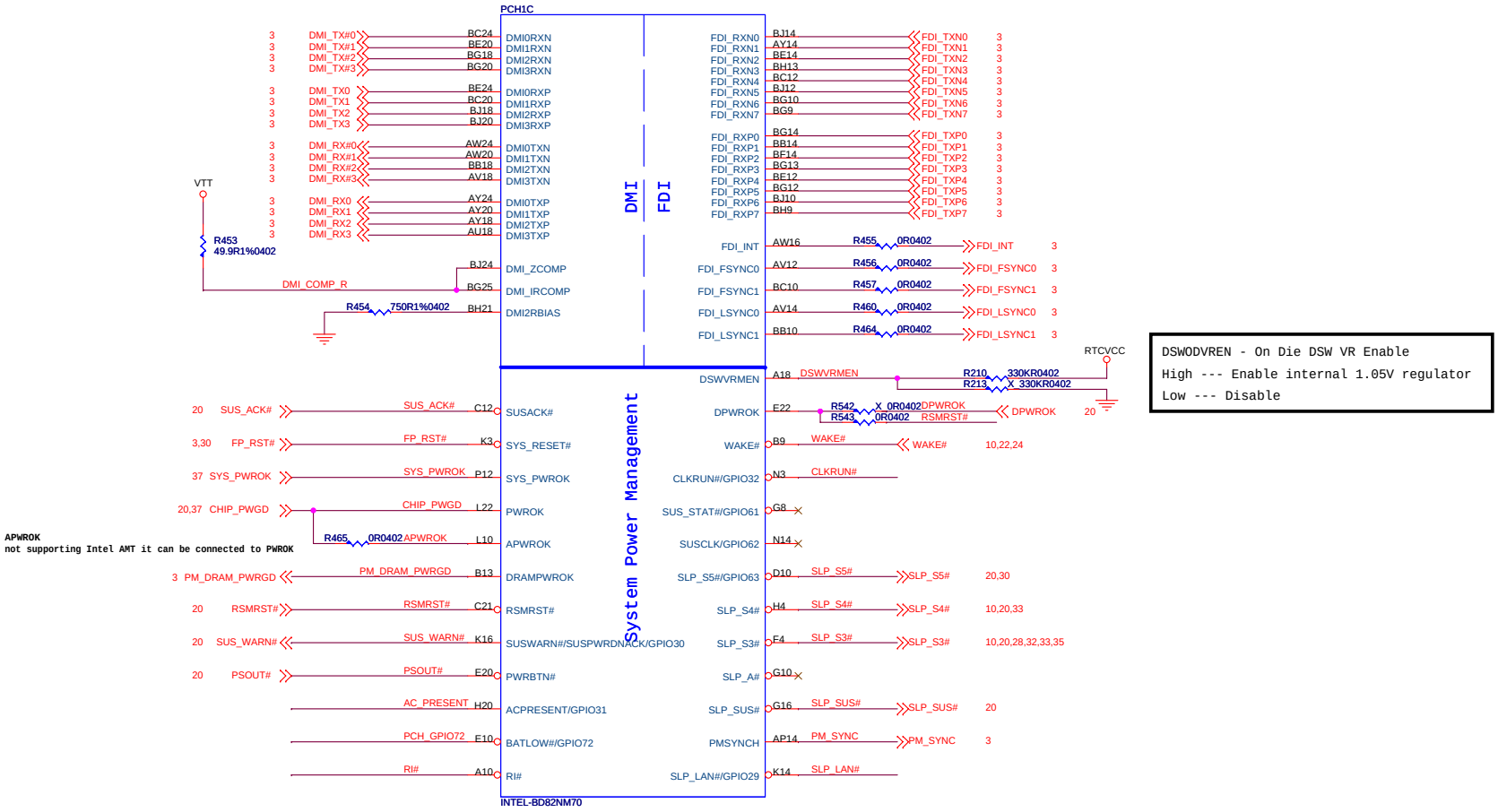
MS-A9281

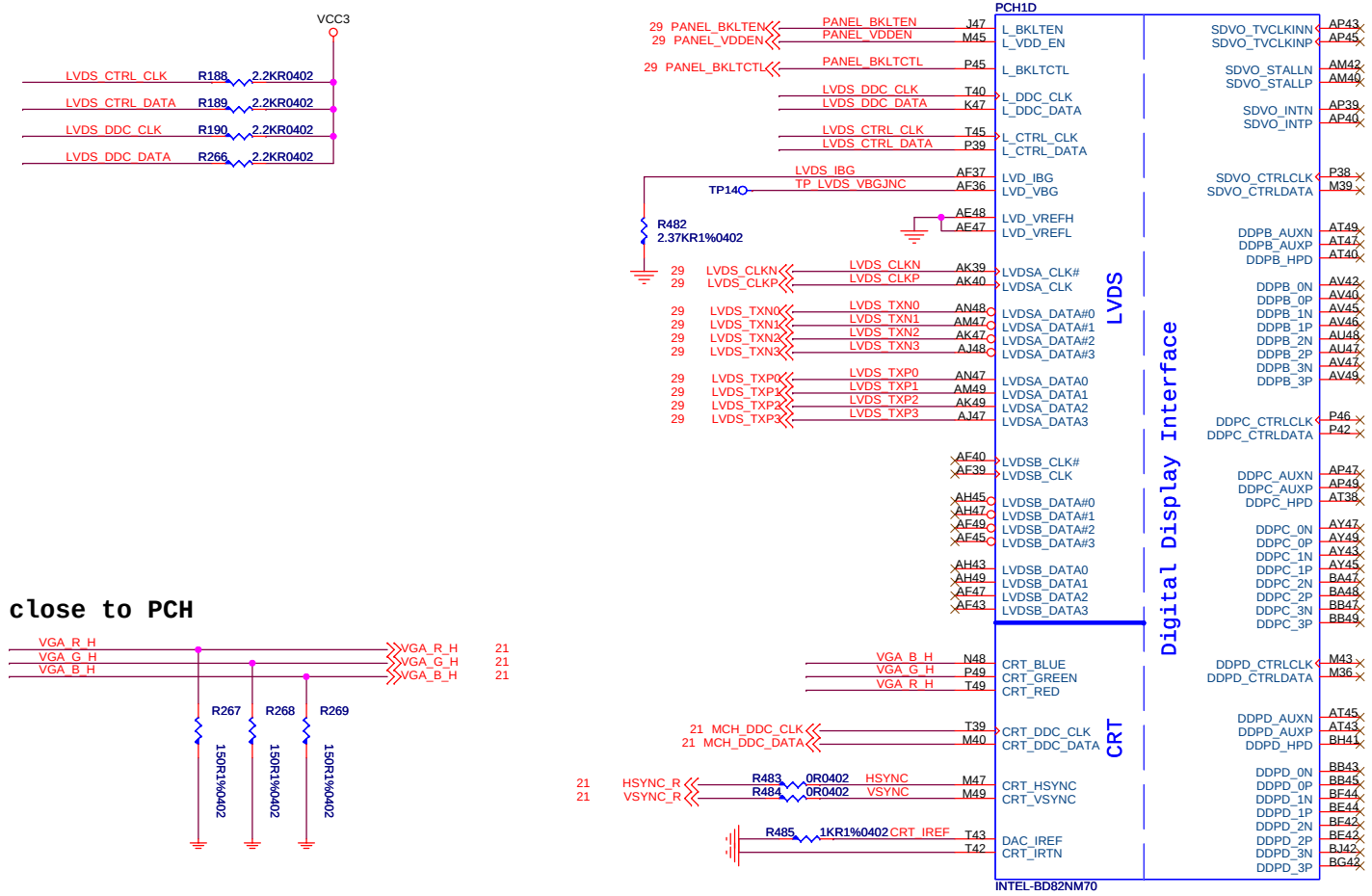
Size	Document Description	Rev
Custom	PCH-1 (HDA/JTAG/SATA)	1.1

Date: Tuesday, December 18, 2012 Sheet 11 of 42

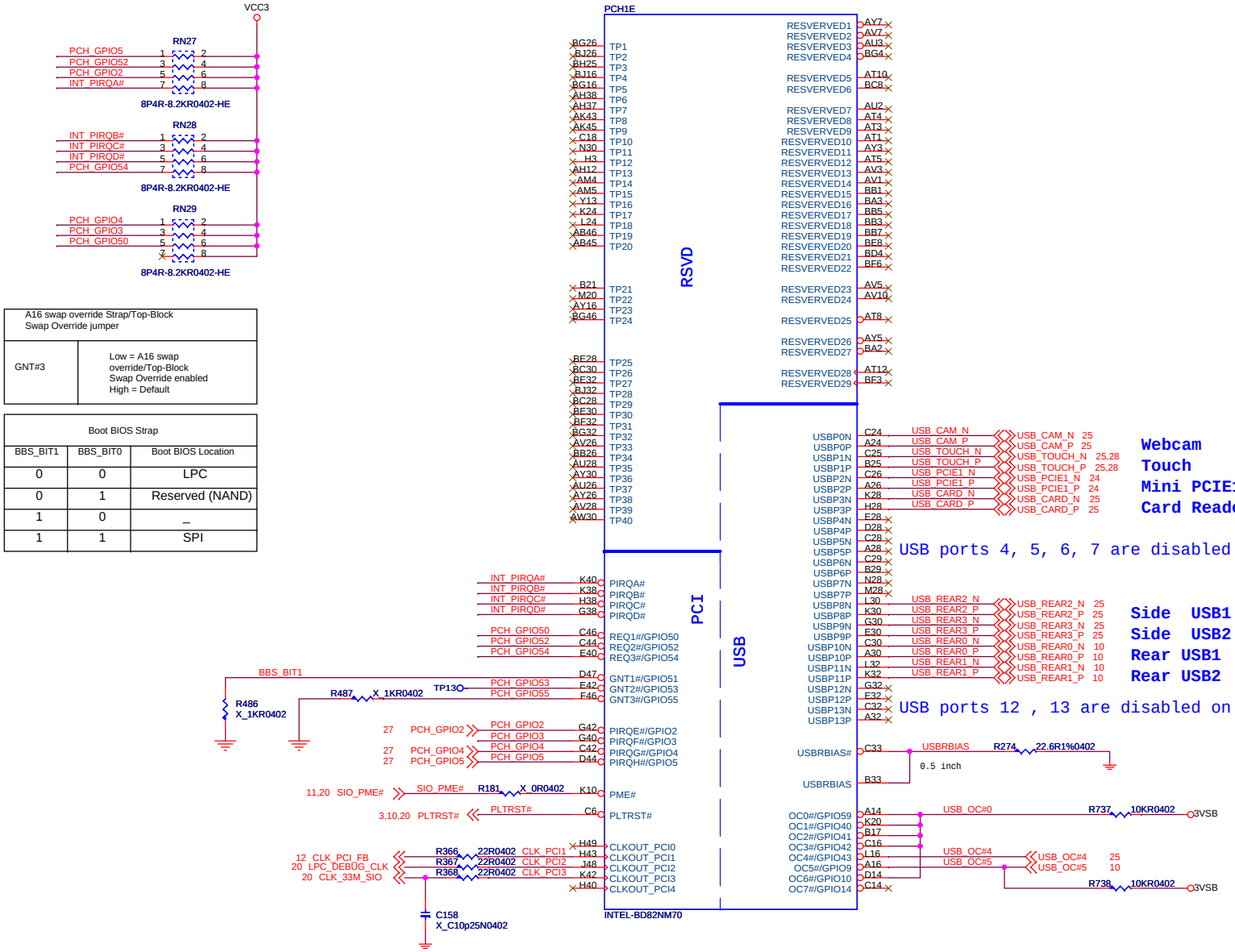

PCH1B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
INTEL-BD82NM70
PCIe ports 5-8 are disabled on NM70
1.0 reserve to BIOS SKU detect
High USB3.0
LOW USB2.0
SMLINK0 for PHY
8P4R-2.2KR0402
NN-2N7002DW-7-F_SOT363-6-RH
For Intergrated Clock Generation Mode
MICRO-STAR INT'L CO.,LTD
MS-A9281
PCH-2 (PCI-E/SMBUS/CLK)
Date: Tuesday, December 18, 2012
Sheet 12 of 42



MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: PCH-3 (DMI/FDI/GPIO)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 13 of 42	



MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: Custom	Document Description: PCH-4 (LVDS/DDI/VGA)
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet 14 of 42



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MS-A9281		
Size: Custom	Document Description: PCH-5 (PCI/USB/NVRAM)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 15 of 42	

GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN

GPIO57 --If not used,require pull up 3VSUS

Integrated Clock Chip Enable	
ICC_EN	High: use CK505 (buffer through mode) intelnal pull high
	Low: use PCH(interated clock mode)

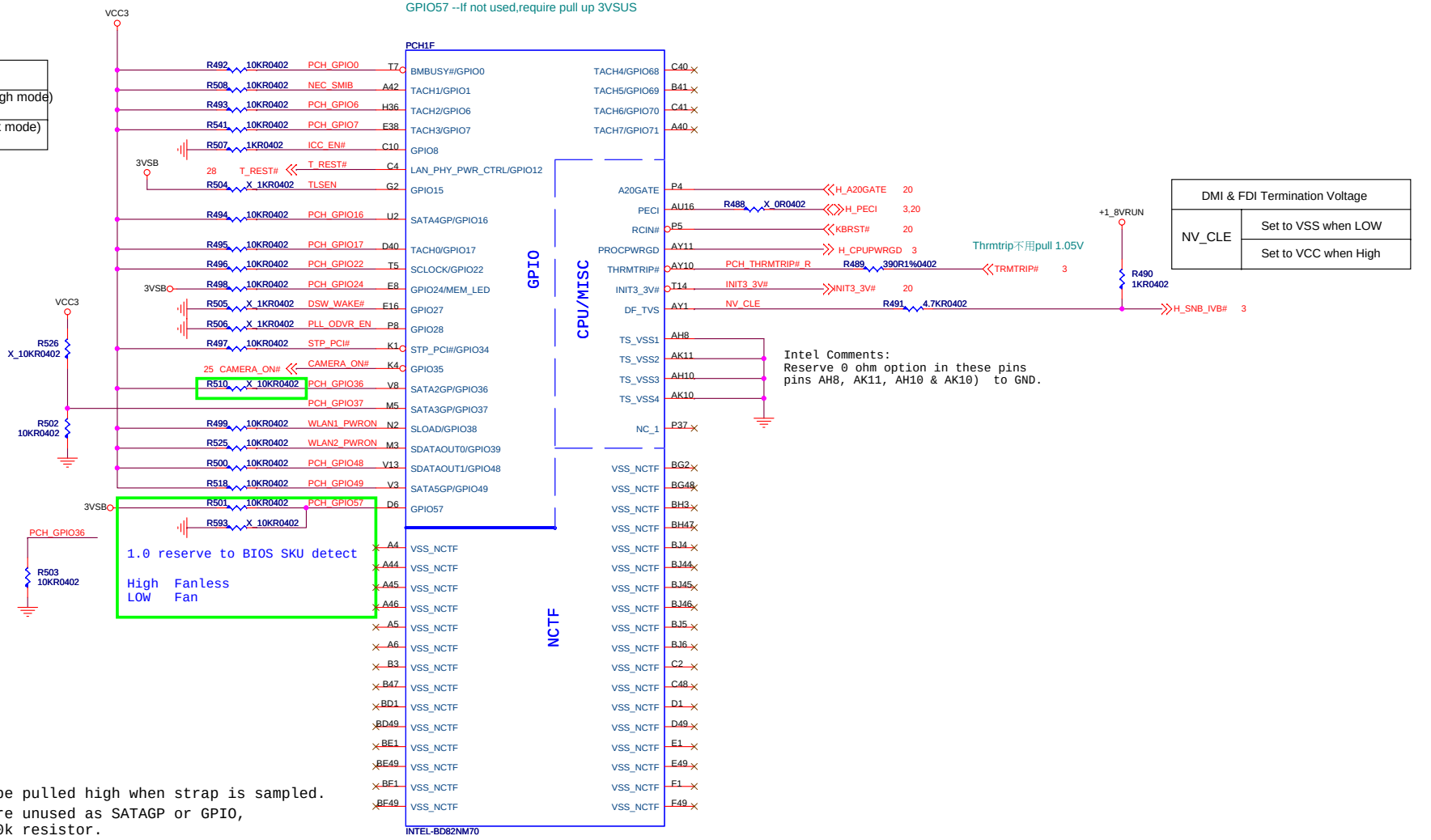
PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

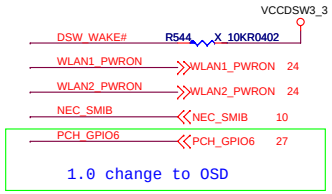
GPIO36 --CRB connector to 3V

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High



PCH EDS1.0:GPl036&37 should not be pulled high when strap is sampled.
PCH EDS1.1:GPl036&37 when pins are unused as SATAGP or GPIO,
terminate them to VSS via 8.2k-10k resistor.



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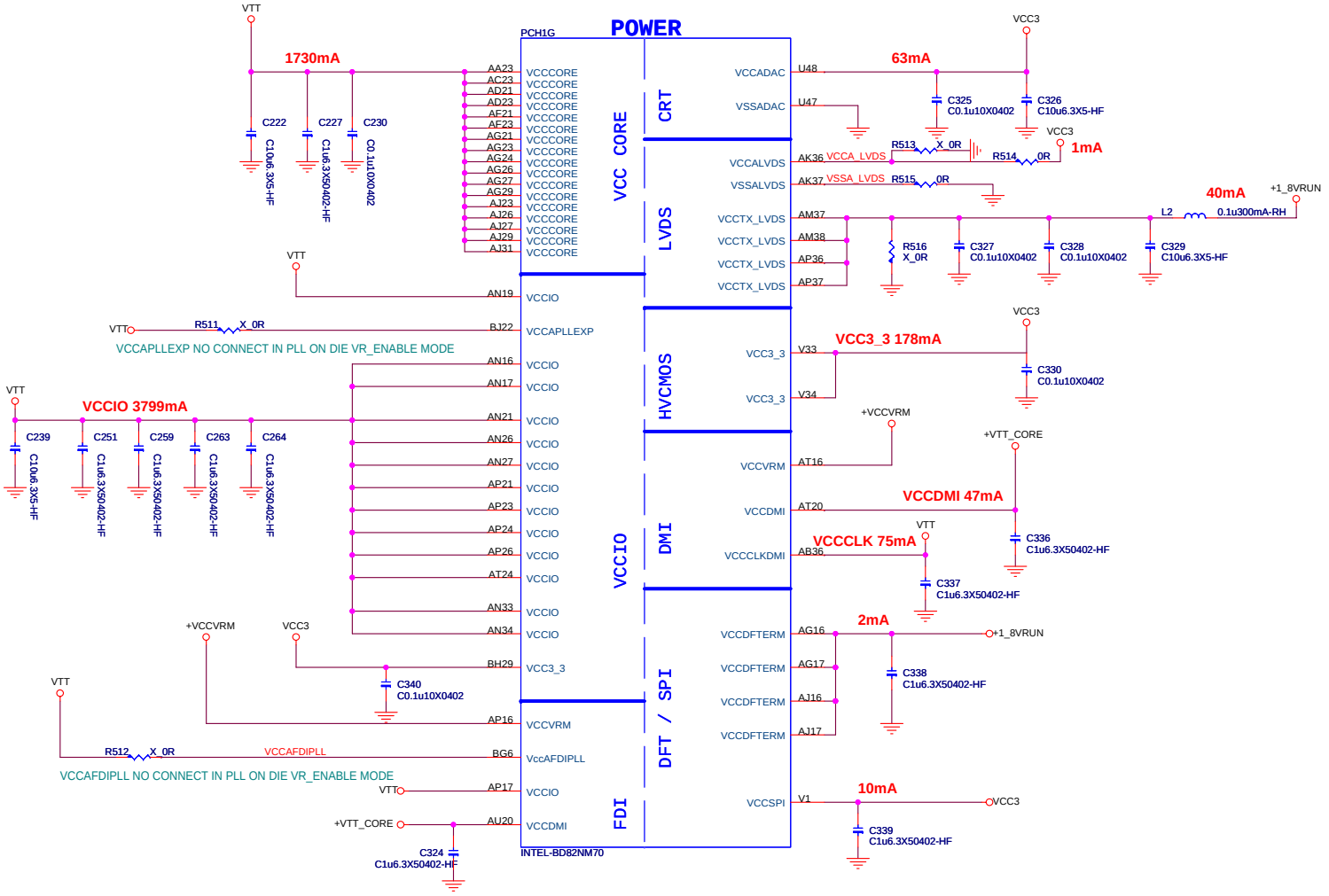
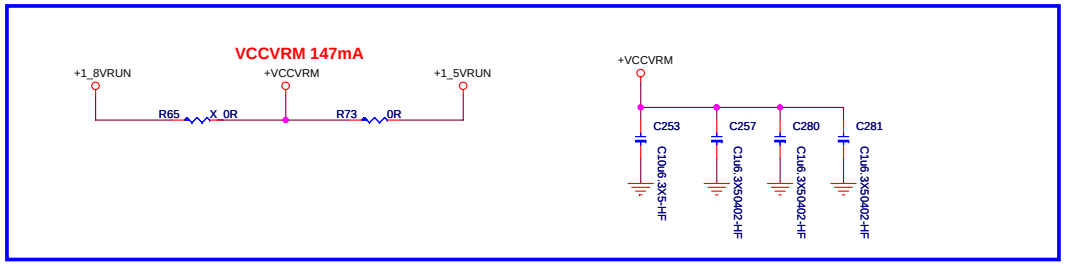
MS-A9281

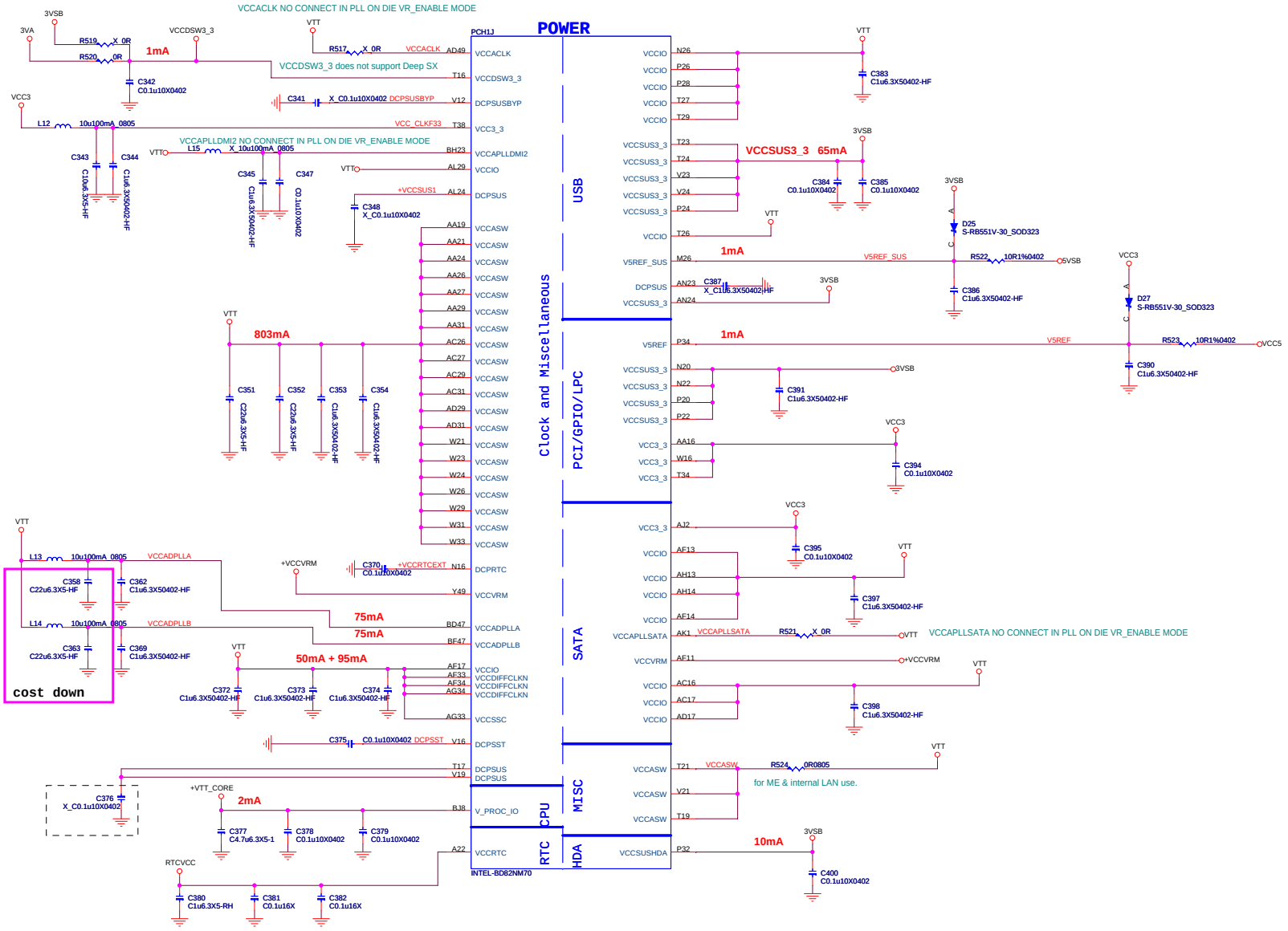
Size	Document Description	Rev
Custom	PCH-6 (GPIO/NCTF/RSVD)	1.1

Date: Tuesday, December 18, 2012 Sheet 16 of 42

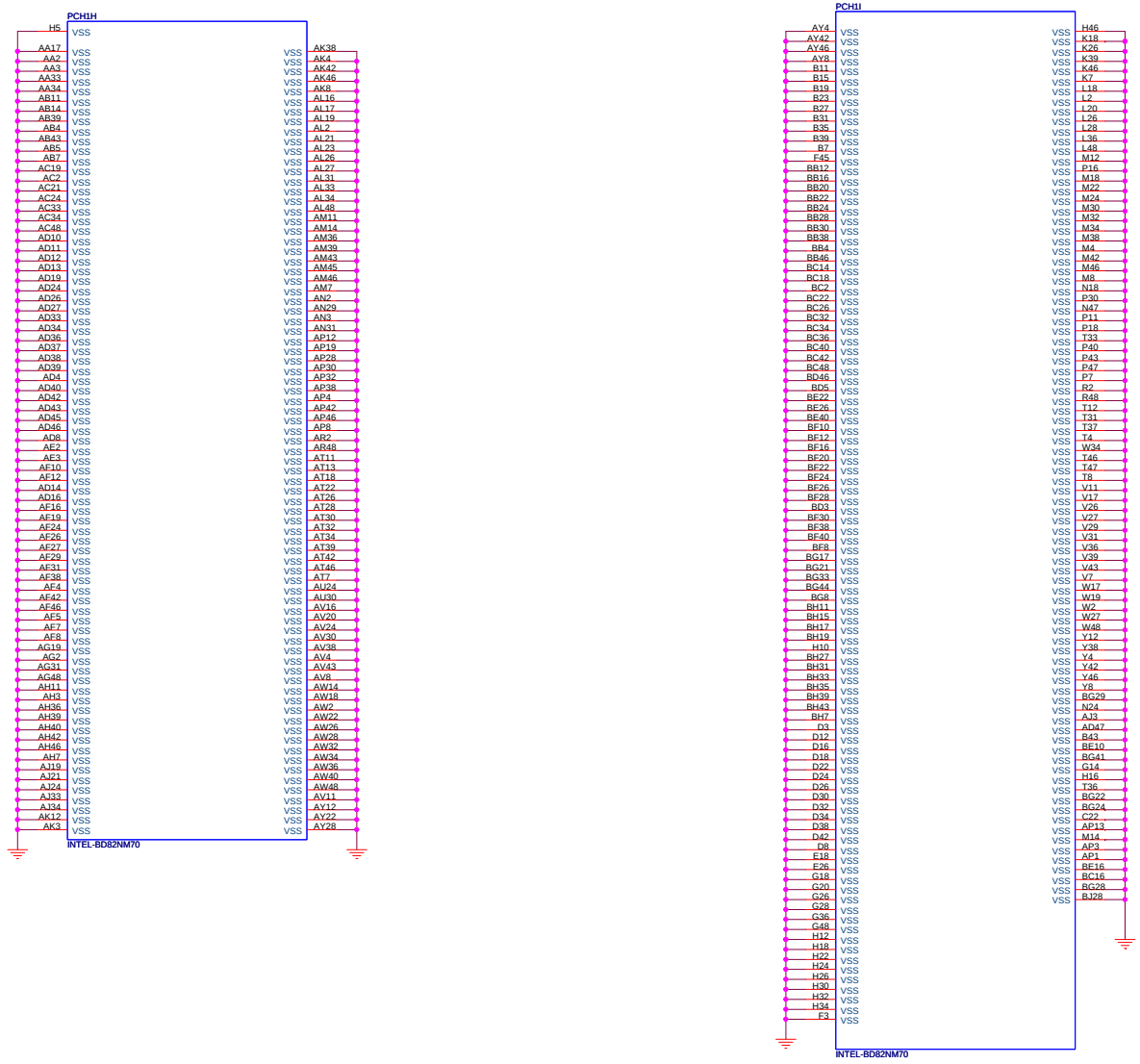




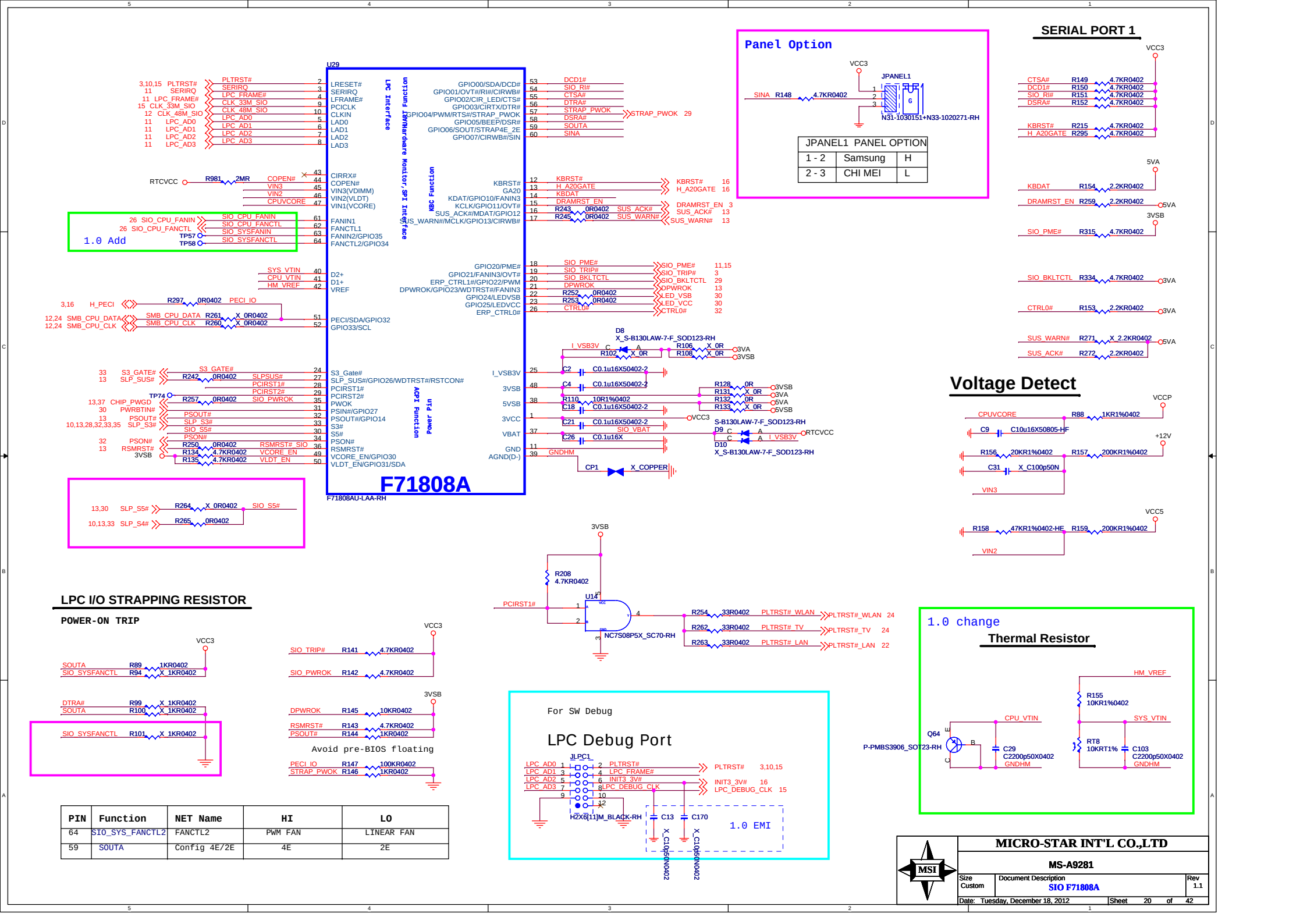
MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: PCH-7 (POWER I)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 17 of 42	



MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: C	Document Description: PCH-8 (POWER II)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 18 of 42	



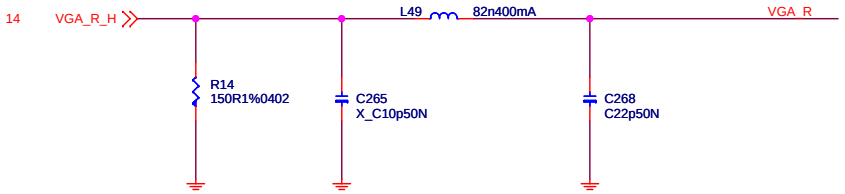
MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: C	Document Description: PCH-9 (GND)	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 19 of 42	

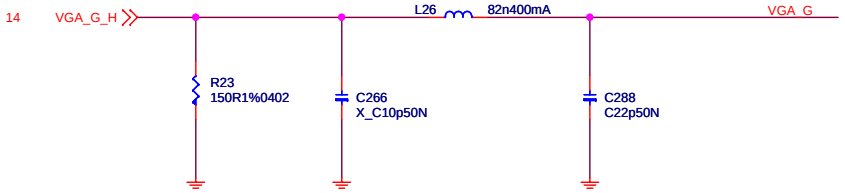


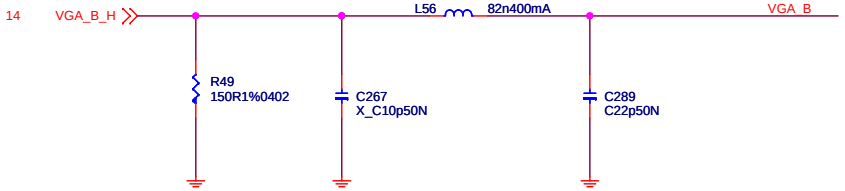
PIN	Function	NET Name	HI	LO
64	SIO_SYS_FANCTL2	FANCTL2	PWM FAN	LINEAR FAN
59	SOUTA	Config 4E/2E	4E	2E

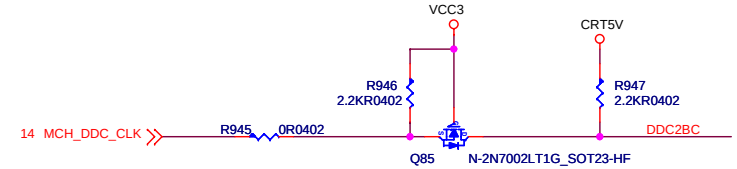
VGA Output for Debug

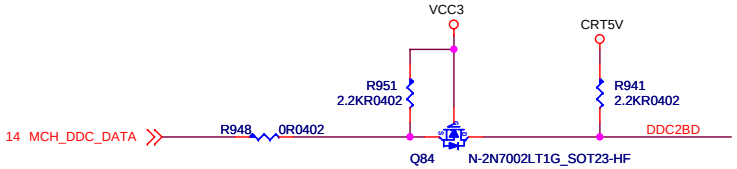
williy

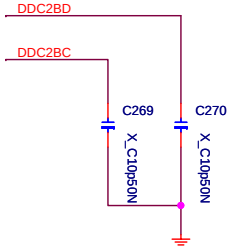


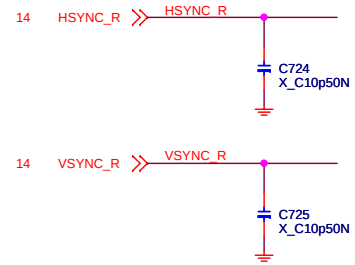


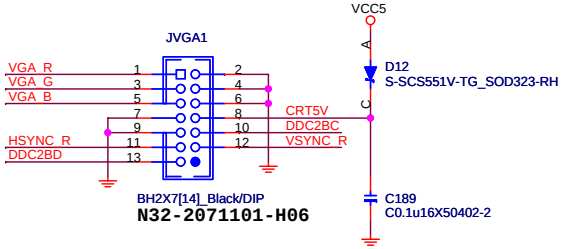




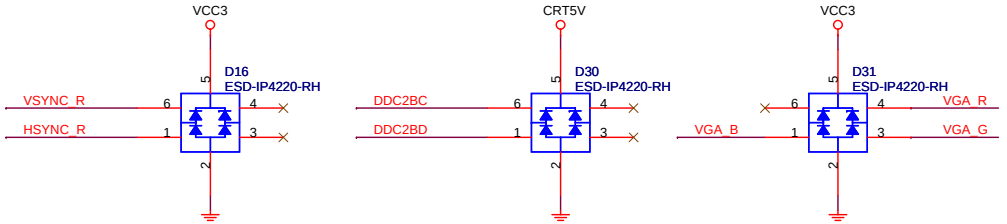








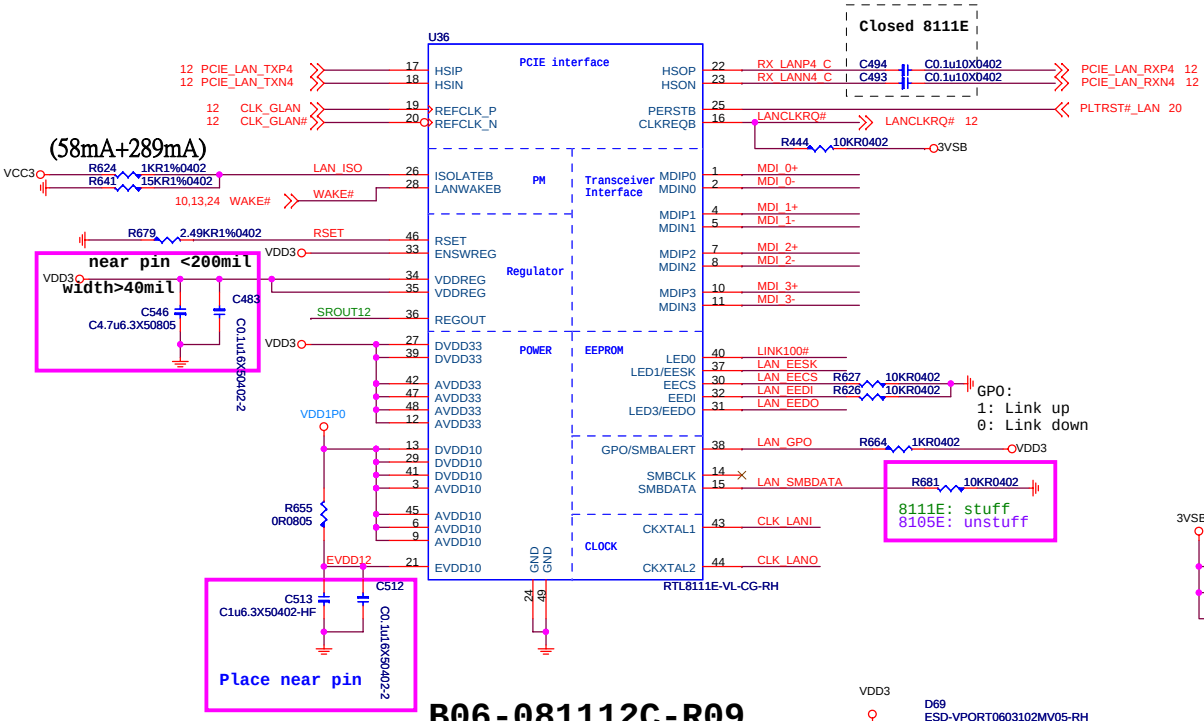
ESD Near Connector < 500 mils



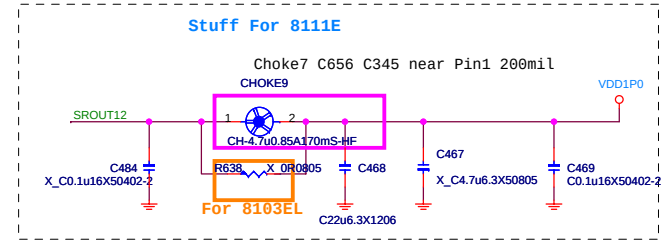
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A9281	
Size B	Document Description VGA	Rev 1.1
Date: Tuesday, December 18, 2012	Sheet 21 of 42	

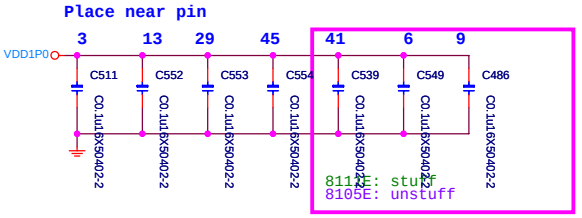
RTL8111E Giga LAN

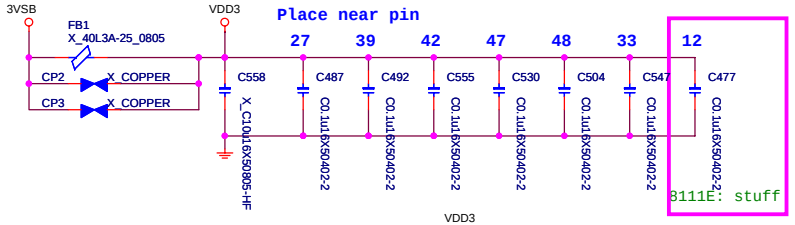
RTL8105E 10/100M LAN

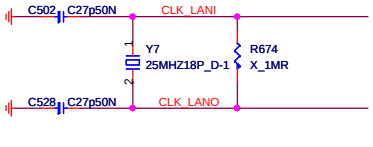


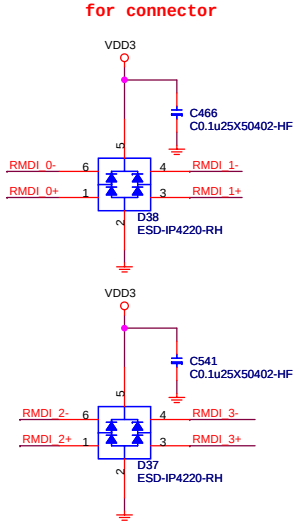
B06-081112C-R09

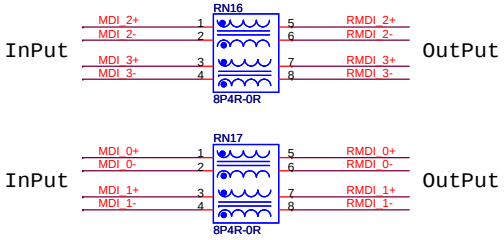


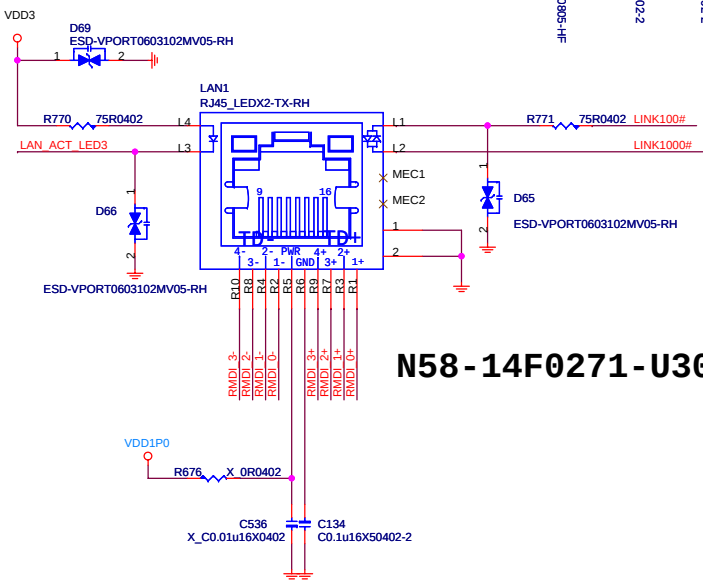






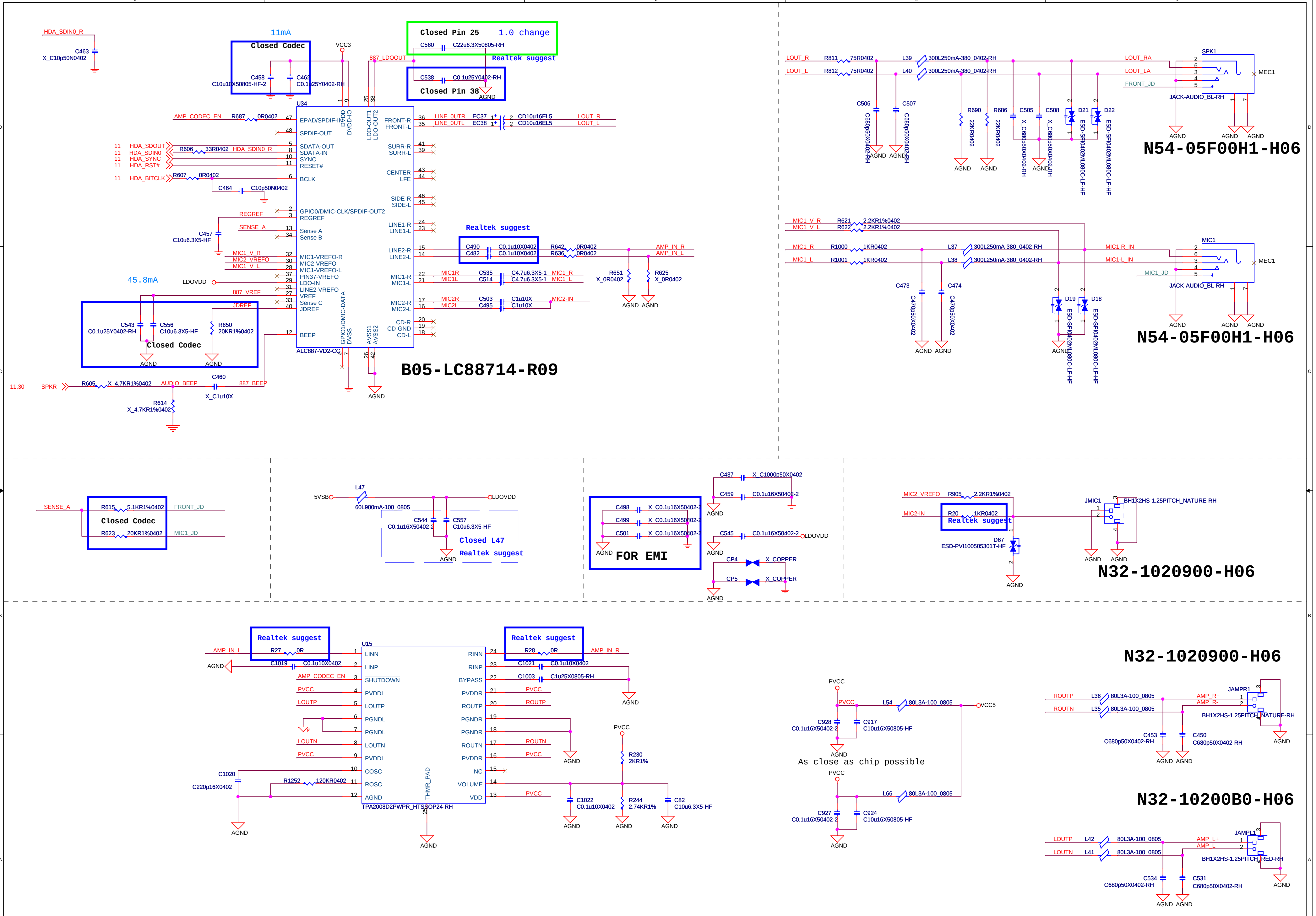






N58-14F0271-U30

MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: Custom	Document Description: LAN-RTL8111E-VB-GR
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet 22 of 42



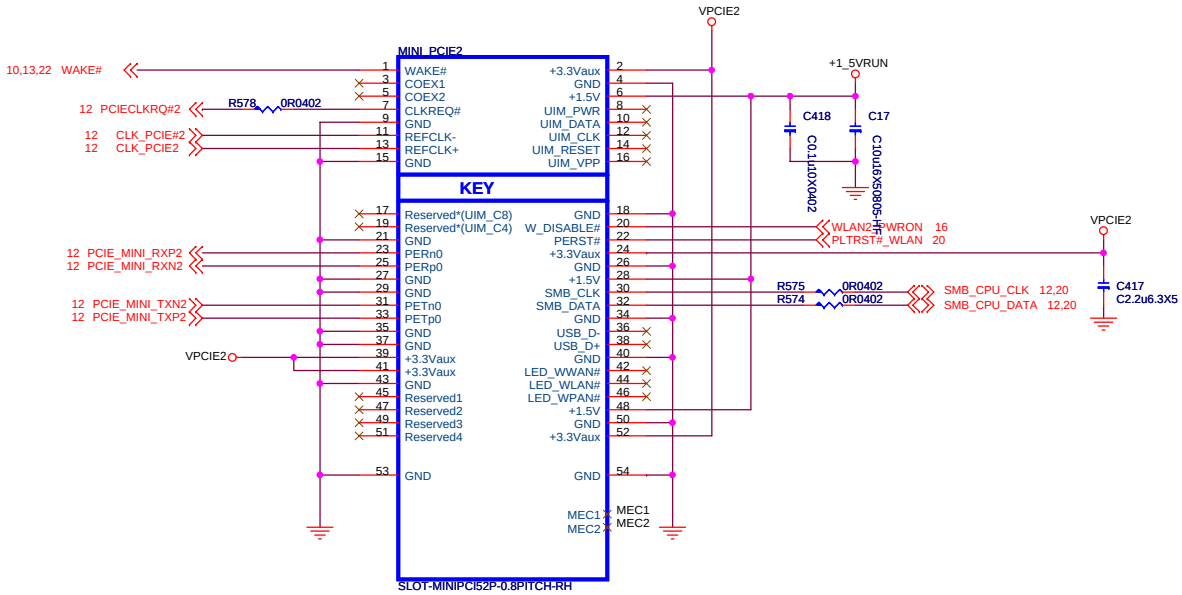
MICRO-STAR INT'L CO.,LTD

MS-A9281

Size	Document Description	Rev
C	Audio Codec ALC887	1.1

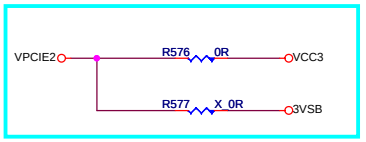
Date: Tuesday, December 18, 2012 Sheet 23 of 42

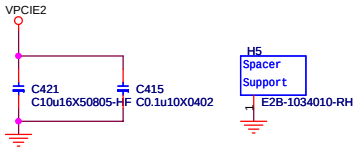
Wireless LAN(Short Card)



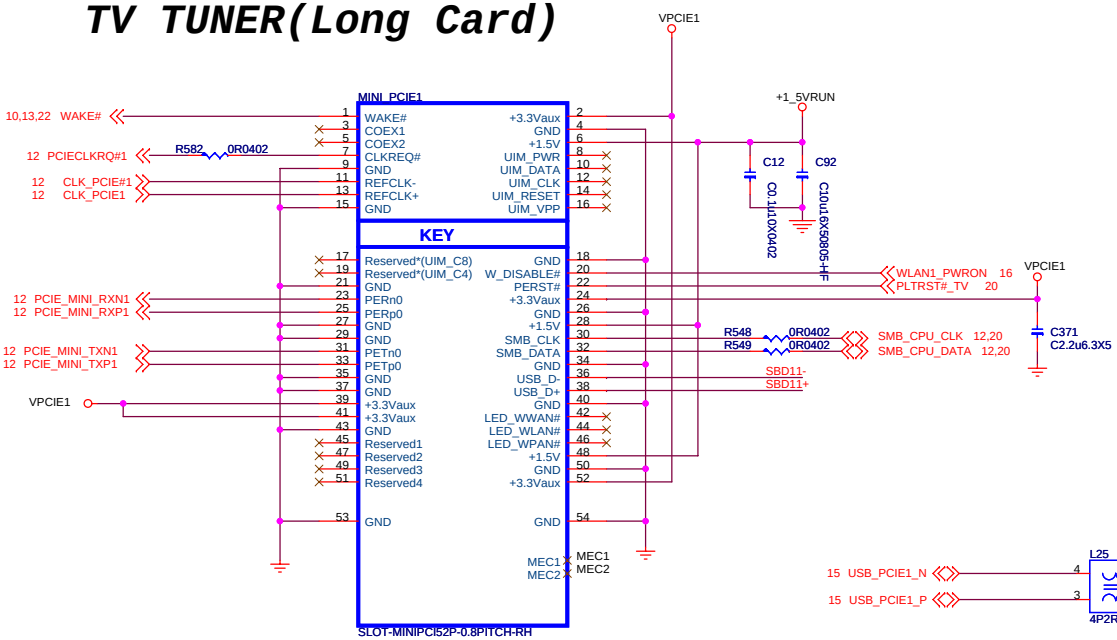
VCC3, 1.5A

+1_5VRUN, 0.5A





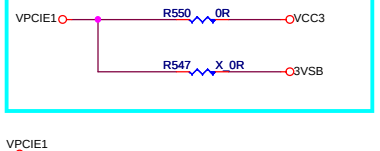
TV TUNER(Long Card)

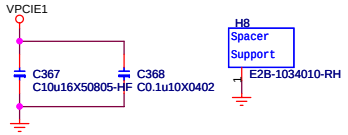


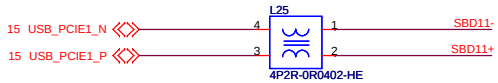
VCC3, 1.5A

+1_5VRUN, 0.5A

Power change to Normal 3/5





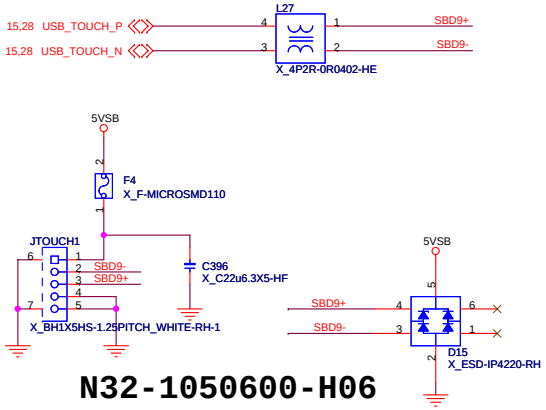


N11-0520040-A81

PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2

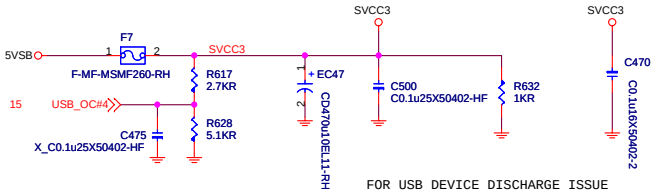
MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: MINI-PCIE Slot	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 24 of 42	

Multi Touch (Option)

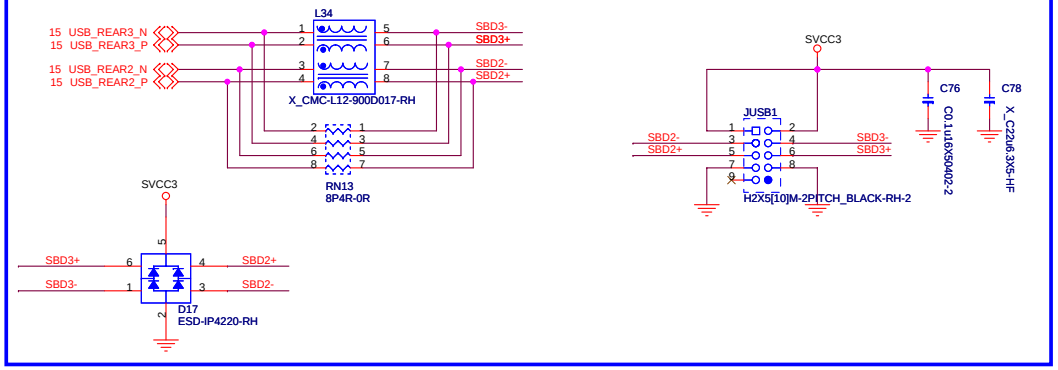


N32-1050600-H06

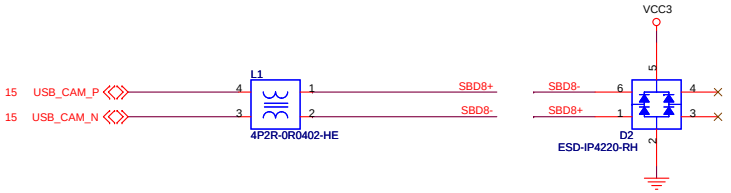
POWER CIRCUIT FOR USB PORT 2,3 (REAR)

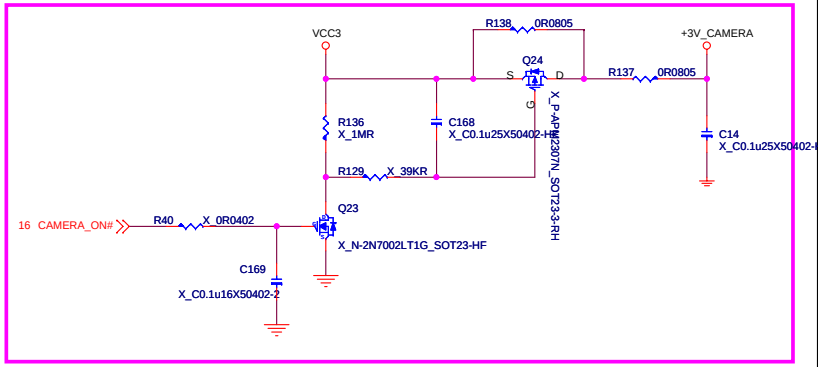


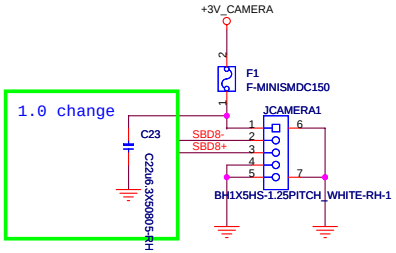
SIDE PANEL USB CONNECTOR FOR USB PORT 2,3



Webcam

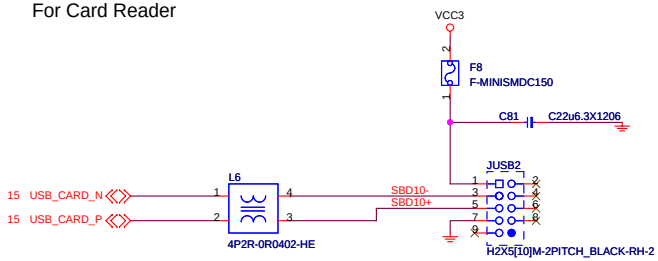






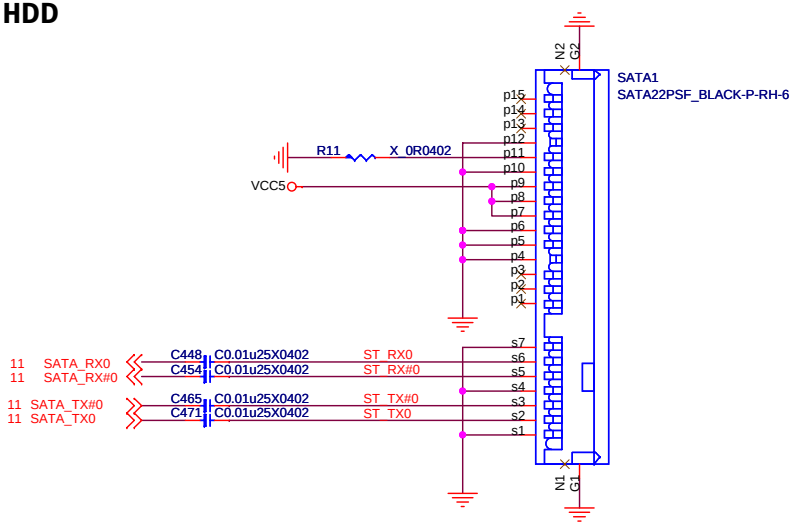
N32-1050600-H06

For Card Reader

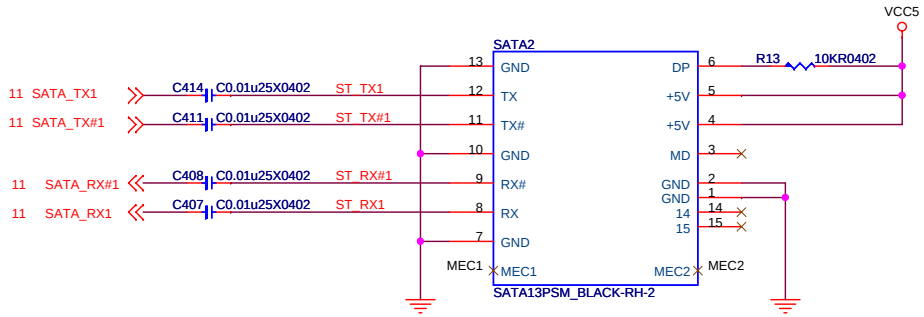


MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: USB / IR / TOUCH / WEBCAM	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 25 of 42	

SATA HDD

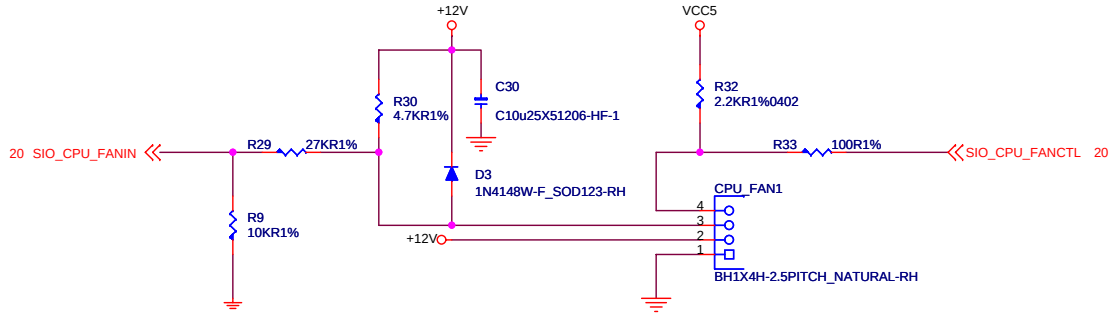


SATA 0DD



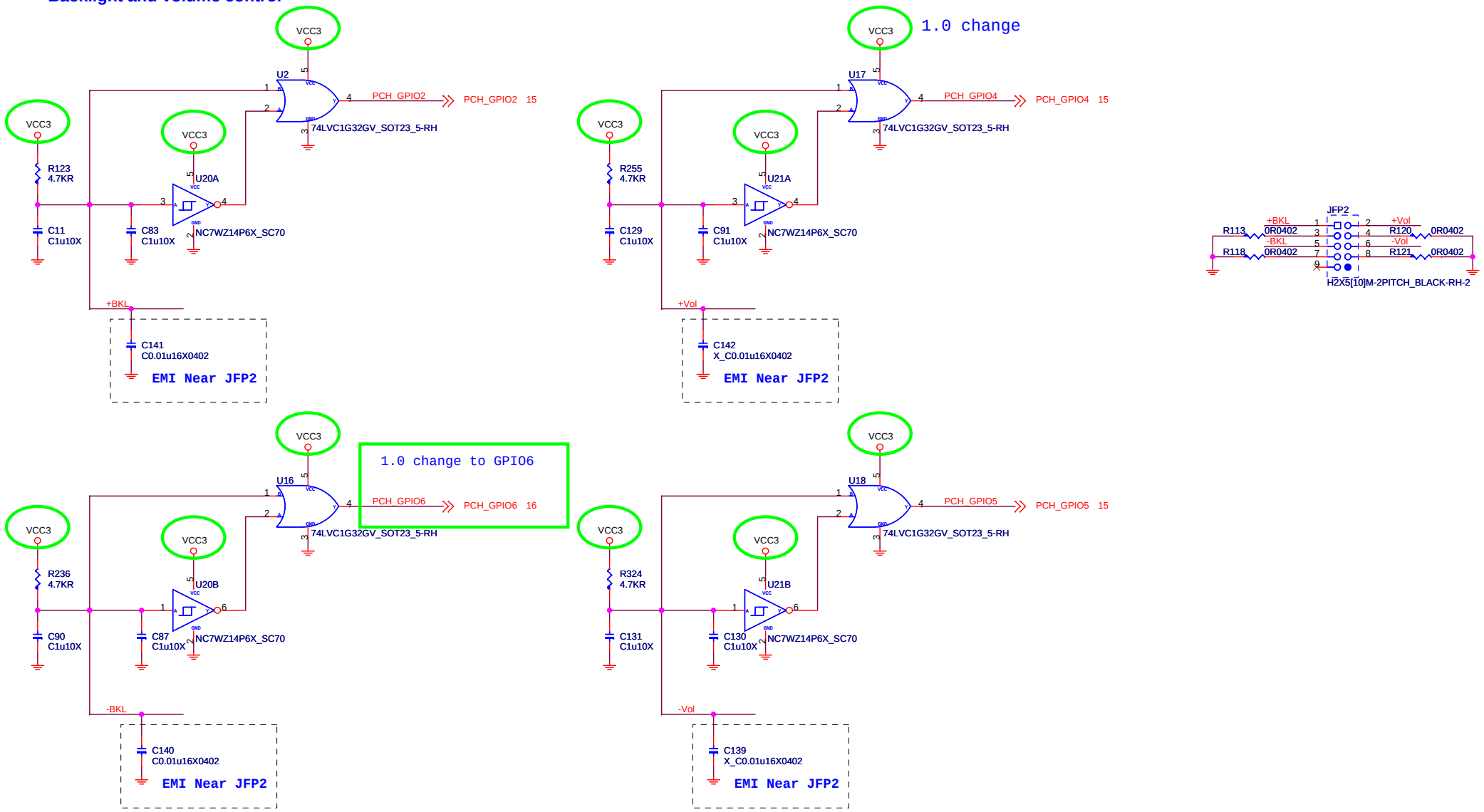
1.0 Add

CPU FAN



MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: SATA / FAN Control	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 26 of 42	

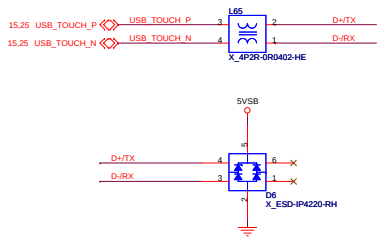
Backlight and volume control

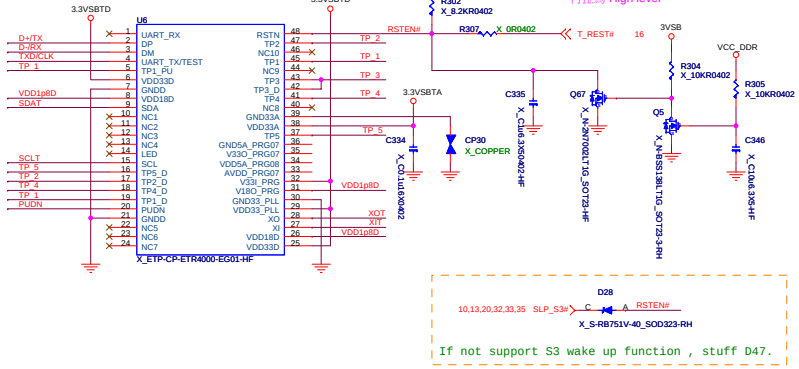


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A9281	
Size B	Document Description OSD JFP2	Rev 1.1
Date: Tuesday, December 18, 2012	Sheet 27 of 42	

Non TOUCH NO STUFF

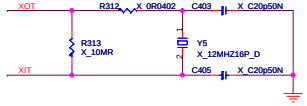
Low Speed USB D+/D-





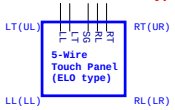
Open-Drain , Default pin type 是 In Put,
開機後 由 BIOS po 為 GPO,
Low level 維持 200ms 後,
再拉為 High level

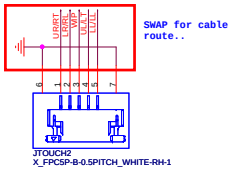
If not support S3 wake up function , stuff D47.



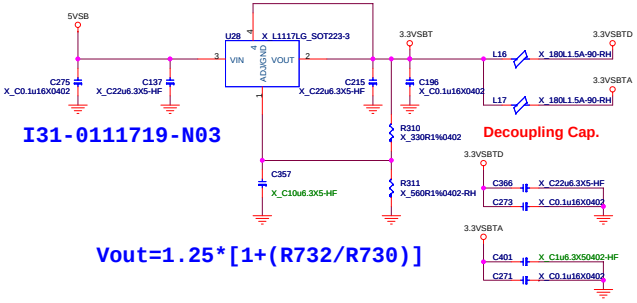
Touch Panel

(Option 1) 5-Wire Resistive
Touch Panel for ELO_type





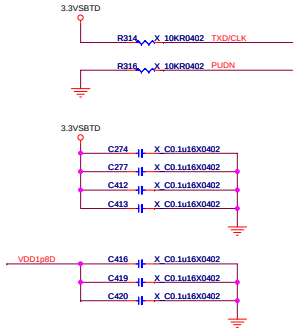
N5A-05F0020-H06

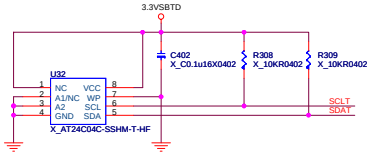


I31-0111719-N03

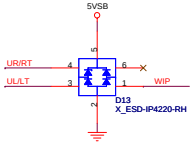
Decoupling Cap.

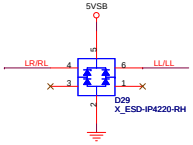
Vout=1.25*[1+(R732/R730)]



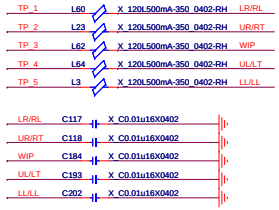


M33-24C0463-A26

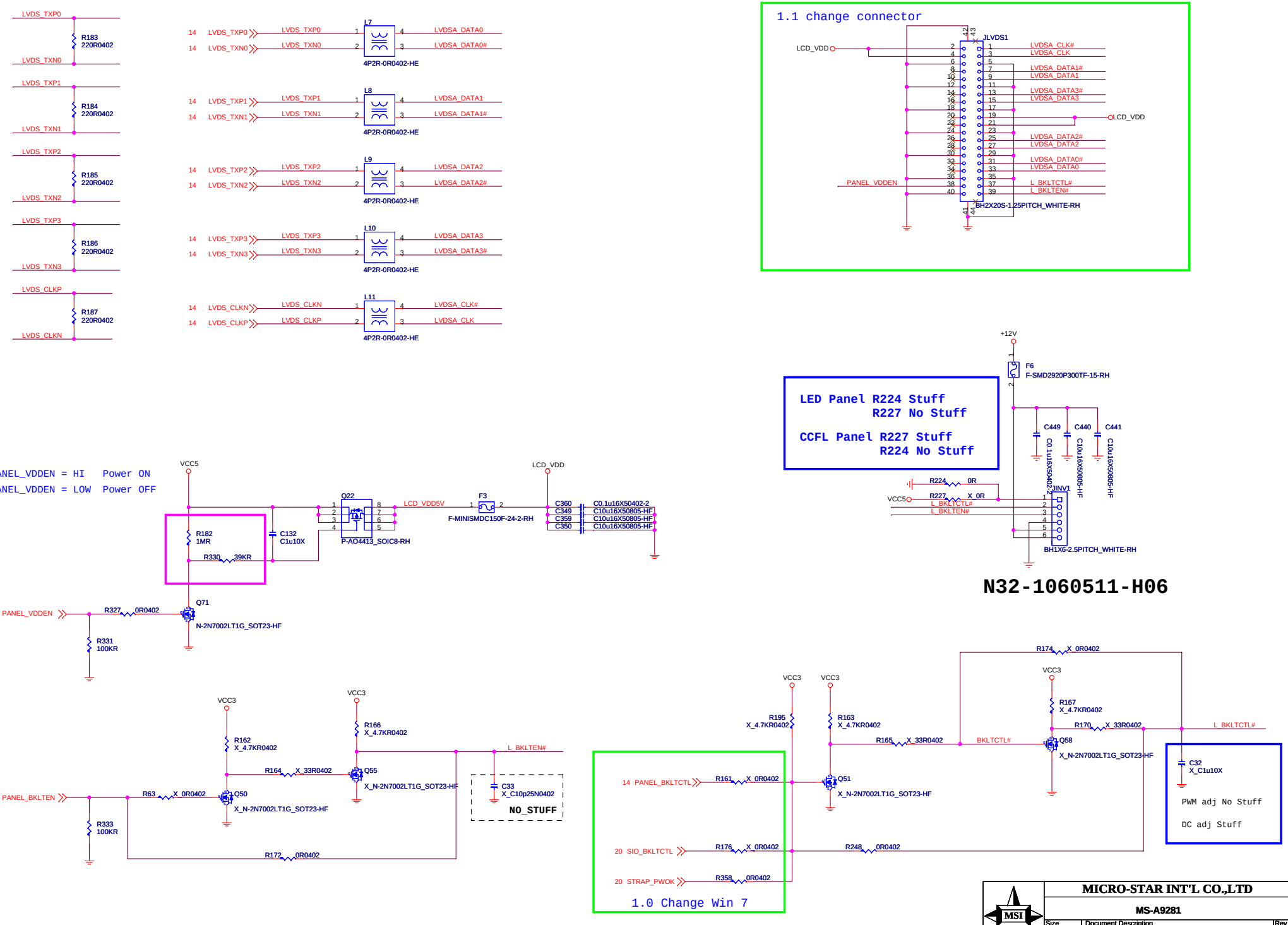




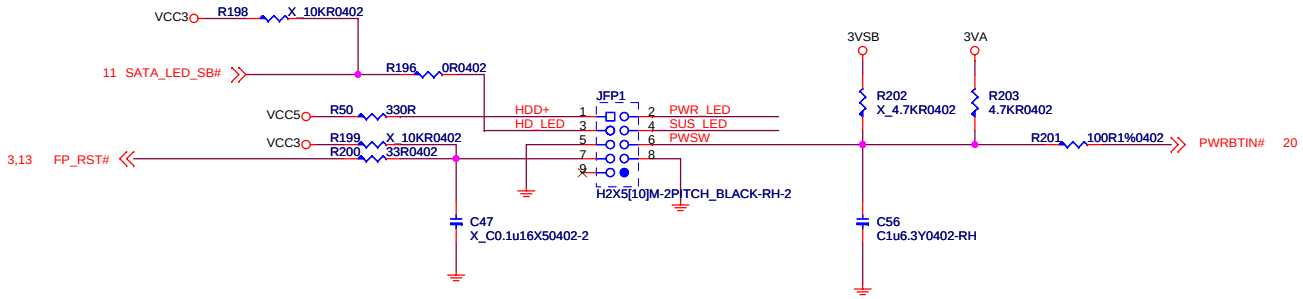
EMI Suppressor



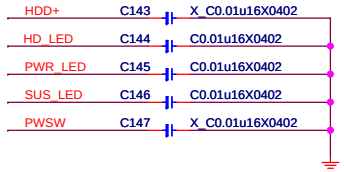
MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: Custom	Document Description: Touch Panel_ETP-CP-ETR4000
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet 28 of 42


LVDS_TXP0
R183 220R0402
LVDS_TXN0
LVDS_TXP1
R184 220R0402
LVDS_TXN1
LVDS_TXP2
R185 220R0402
LVDS_TXN2
LVDS_TXP3
R186 220R0402
LVDS_TXN3
LVDS_CLKP
R187 220R0402
LVDS_CLKN
L7
4P2R-0R0402-HE
LVDSA_DATA0
LVDSA_DATA0#
L8
LVDSA_DATA1
LVDSA_DATA1#
L9
LVDSA_DATA2
LVDSA_DATA2#
L10
LVDSA_DATA3
LVDSA_DATA3#
L11
LVDSA_CLK#
LVDSA_CLK
1.1 change connector
LCD_VDD
JLVDS1
PANEL_VDDEN
L_BKLTCTL#
L_BKLTEN#
BH2X20S-1.25PITCH_WHITE-RH
+12V
F6
F-SMD2920P300TF-15-RH
C449
C440
C441
C0.1u16X50402-2
C10u16X50805-HF
LED Panel R224 Stuff
R227 No Stuff
CCFL Panel R227 Stuff
R224 No Stuff
R224 0R
R227 X_0R
JINV1
BH1X6-2.5PITCH_WHITE-RH
N32-1060511-H06
PANEL_VDDEN = HI Power ON
PANEL_VDDEN = LOW Power OFF
VCC5
Q22
P-AO4413_SOIC8-RH
LCD_VDD5V
F3
F-MINISMDC150F-24-2-RH
C360
C349
C359
C350
R182 1MR
R330 39KR
C132 C1u10X
Q71
N-2N7002LT1G_SOT23-HF
R327 0R0402
R331 100KR
VCC3
R162 X_4.7KR0402
R166 X_4.7KR0402
R164 X_33R0402
Q55
X_N-2N7002LT1G_SOT23-HF
R63 X_0R0402
Q50
R333 100KR
R172 0R0402
C33 X_C10p25N0402
NO_STUFF
R174 X_0R0402
R195 X_4.7KR0402
R163 X_4.7KR0402
R167 X_4.7KR0402
R165 X_33R0402
R170 X_33R0402
BKLTCTL#
Q58
C32 X_C1u10X
PWM adj No Stuff
DC adj Stuff
PANEL_BKLTCTL
R161 X_0R0402
Q51
SIO_BKLTCTL
R176 X_0R0402
R248 0R0402
STRAP_PWOK
R358 0R0402
1.0 Change Win 7
MICRO-STAR INT'L CO.,LTD
MS-A9281
Size Custom
Document Description
LVDS / Inverter
Rev 1.1
Date: Tuesday, December 18, 2012
Sheet 29 of 42

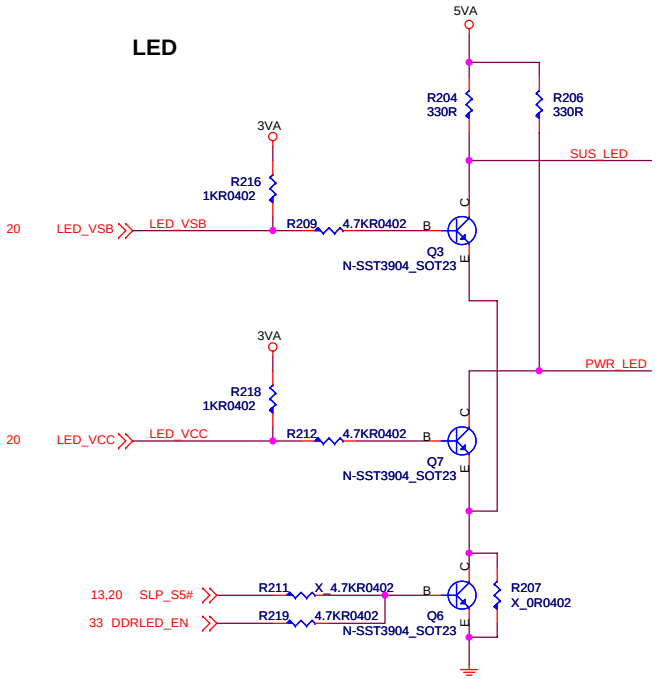
INTEL/PB Front Panel Connector



EMI Near JFP2

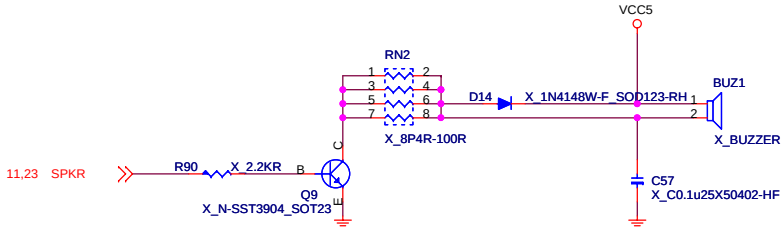


LED

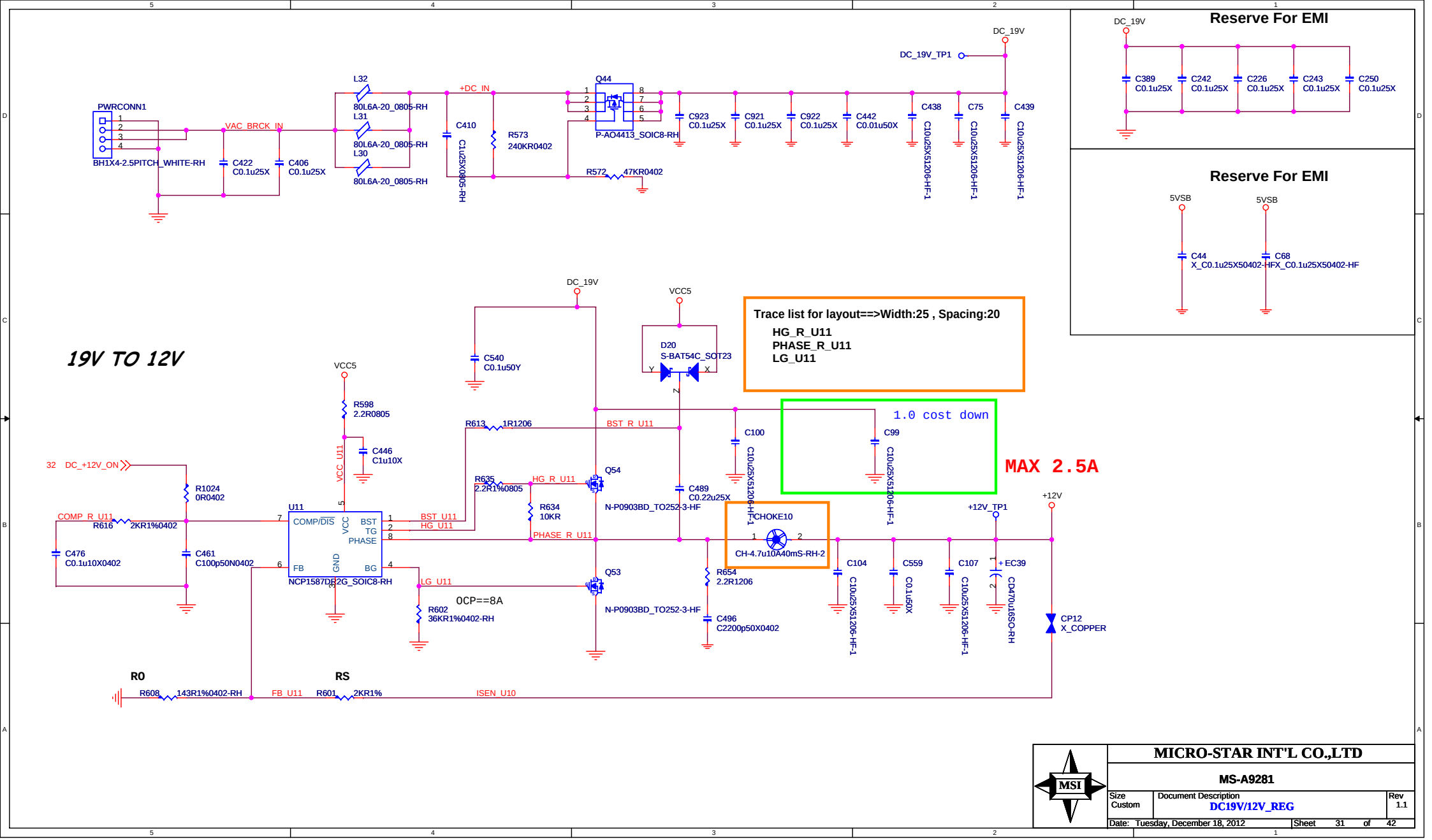


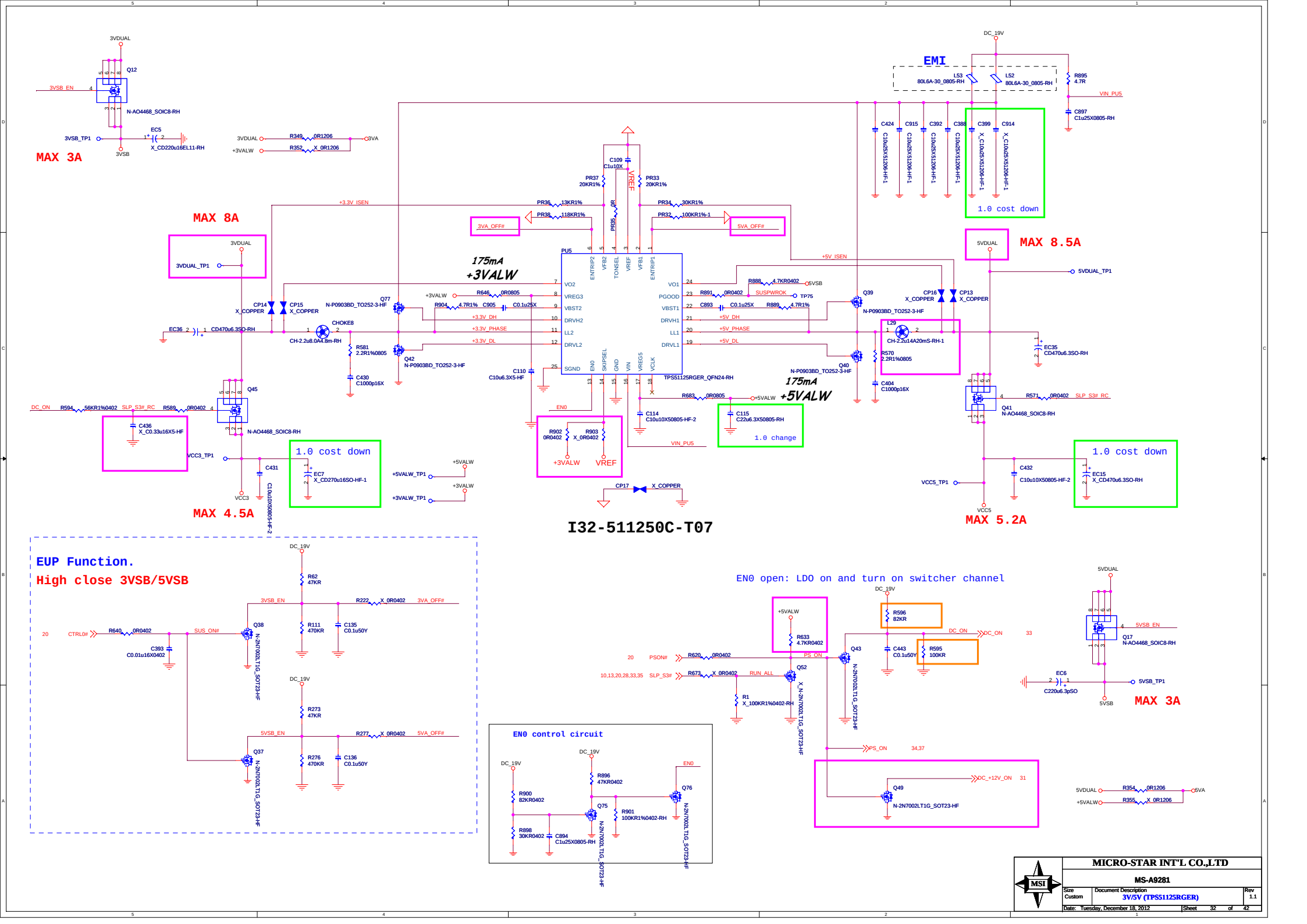
1.0 COST DOWN

SPEAKER BLOCK



MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: Front Panel	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 30 of 42	


DC_19V
DC_19V_TP1
PWRCONN1
BH1X4-2.5PITCH_WHITE-RH
VAC_BRCK_IN
C422 C0.1u25X
C406 C0.1u25X
L32
L31
L30
80L6A-20_0805-RH
+DC_IN
C410 C1u25X0805-RH
R573 240KR0402
Q44
P-AO4413_SOIC8-RH
R572 47KR0402
C923 C0.1u25X
C921 C0.1u25X
C922 C0.1u25X
C442 C0.01u50X
C438 C10u25X51206-HF-1
C75 C10u25X51206-HF-1
C439 C10u25X51206-HF-1
Reserve For EMI
C389 C0.1u25X
C242 C0.1u25X
C226 C0.1u25X
C243 C0.1u25X
C250 C0.1u25X
5VSB
C44 X_C0.1u25X50402-HFX
C68 C0.1u25X50402-HF
19V TO 12V
VCC5
C540 C0.1u50Y
D20 S-BAT54C_SOT23
Trace list for layout==>Width:25 , Spacing:20
HG_R_U11
PHASE_R_U11
LG_U11
1.0 cost down
MAX 2.5A
R598 2.2R0805
C446 C1u10X
R613 1R1206
BST_R_U11
C100 C10u25X51206-HF-1
C99 C10u25X51206-HF-1
32 DC_+12V_ON
R1024 0R0402
R635 2.2R1%0805
HG_R_U11
Q54
N-P0903BD_TO252-3-HF
C489 C0.22u25X
R634 10KR
PHASE_R_U11
CHOKE10
CH-4.7u10A40mS-RH-2
+12V_TP1
+12V
COMP_R_U11
R616 2KR1%0402
U11
COMP/DIS
VCC
BST
TG
PHASE
FB
GND
BG
NCP1587DR2G_SOIC8-RH
BST_U11
HG_U11
LG_U11
C476 C0.1u10X0402
C461 C100p50N0402
0CP==8A
R602 36KR1%0402-RH
Q53
N-P0903BD_TO252-3-HF
R654 2.2R1206
C496 C2200p50X0402
C104 C10u25X51206-HF-1
C559 C0.1u50X
C107 C10u25X51206-HF-1
+ EC39 CD470u16SO-RH
CP12 X_COPPER
R0
R608 143R1%0402-RH
FB_U11
RS
R601 2KR1%
ISEN_U10
MSI
MICRO-STAR INT'L CO.,LTD
MS-A9281
Size Custom
Document Description
DC19V/12V_REG
Rev 1.1
Date: Tuesday, December 18, 2012
Sheet 31 of 42


MAX 3A
MAX 8A
MAX 4.5A
MAX 8.5A
MAX 5.2A
MAX 3A
EMI
1.0 cost down
1.0 change
175mA
+3VALW
175mA
+5VALW
I32-511250C-T07
EUP Function.
High close 3VSB/5VSB
EN0 open: LDO on and turn on switcher channel
EN0 control circuit
MICRO-STAR INT'L CO.,LTD
MS-A9281
3V/5V (TPS51125RGER)
Tuesday, December 18, 2012

VCC_DDR

Iripple=2.8A
2*2*0.8=3.2A>2.8A

Close to Q14

MAX 16A

1.0 change
POWER TEAM

1.0 change
Cost down

1.0 change for cost down

Close to PWM(NCP5217A)
Vout=0.8* (16+15)/16=1.55

I32-5217A0C-005

VTT_DDR

Current Max at 1.2A

MAX 1.2A

near U3 Pin 6

1.0 change
Cost down

MAX 6.2A

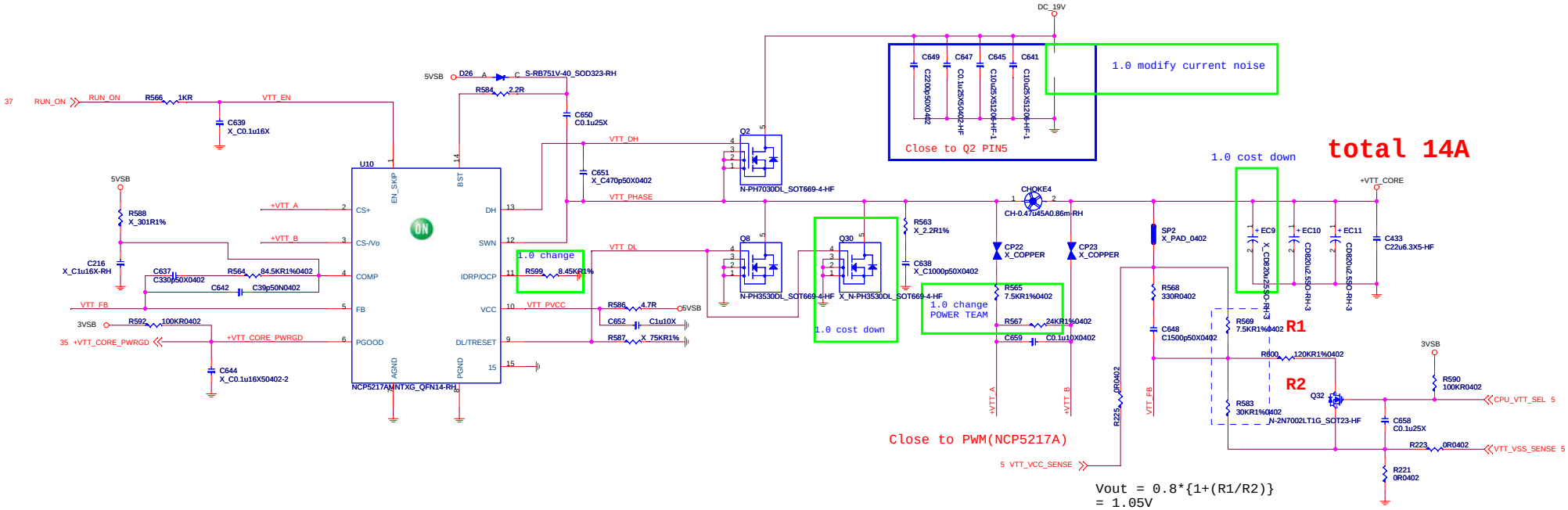
1.0 Change

I31-8331202-N62

EMI

MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: C	Document Description: VCC_DDR & +1_5VRUN	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 33 of 42	

+VTT_CORE Power

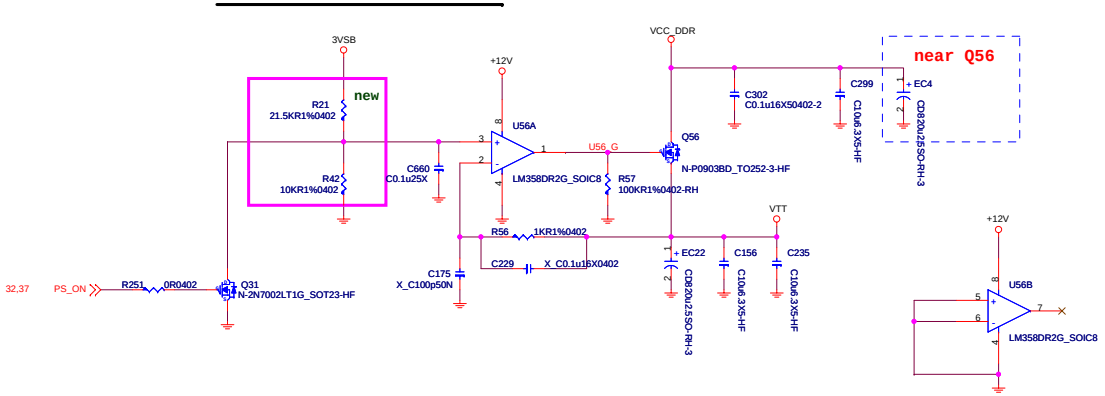


VTT POWER

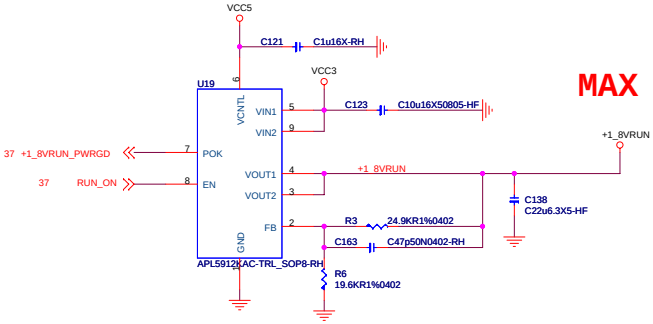
MAX 6.8A

VTT=1.05 V TO PCH

H_VTTVID1=LOW, 1.0V
H_VTTVID1=HIGH, 1.05V



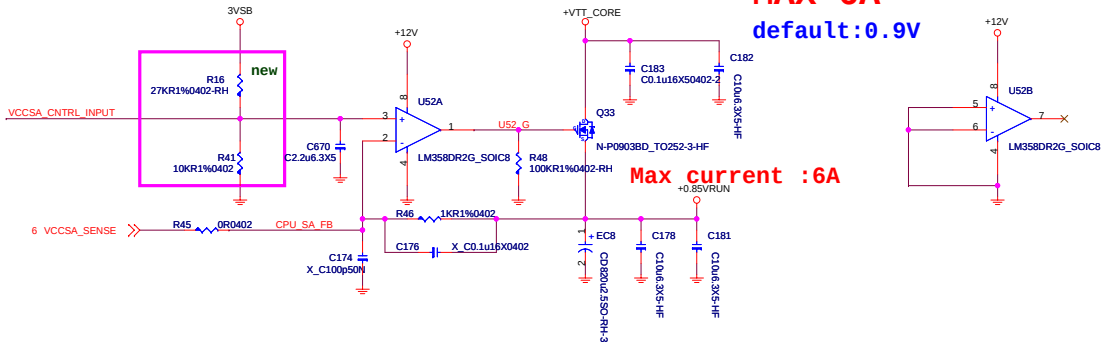
MAX 1.3A



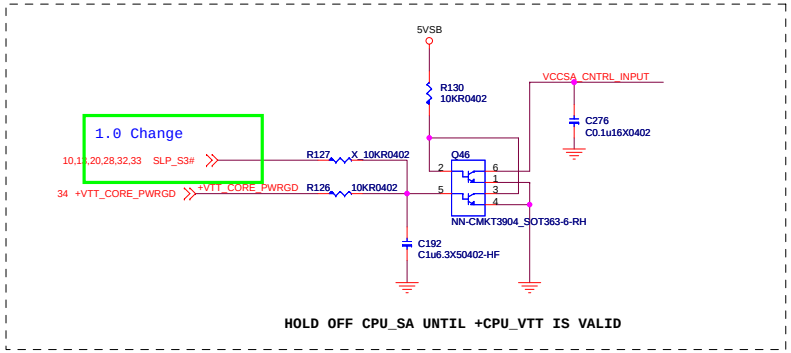
MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: Custom	Document Description: +VTT_CORE & +1_8VRUN
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet 34 of 42

CPU_SA POWER(VCCSA)

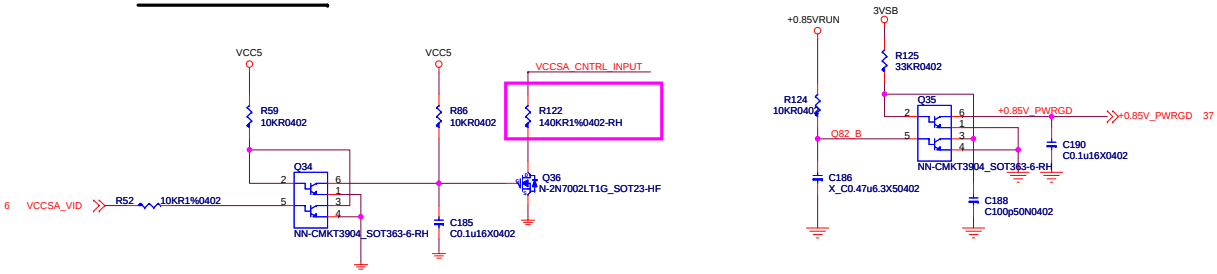
(8.8A)



VCCSA_CNTRL SEQUENCE



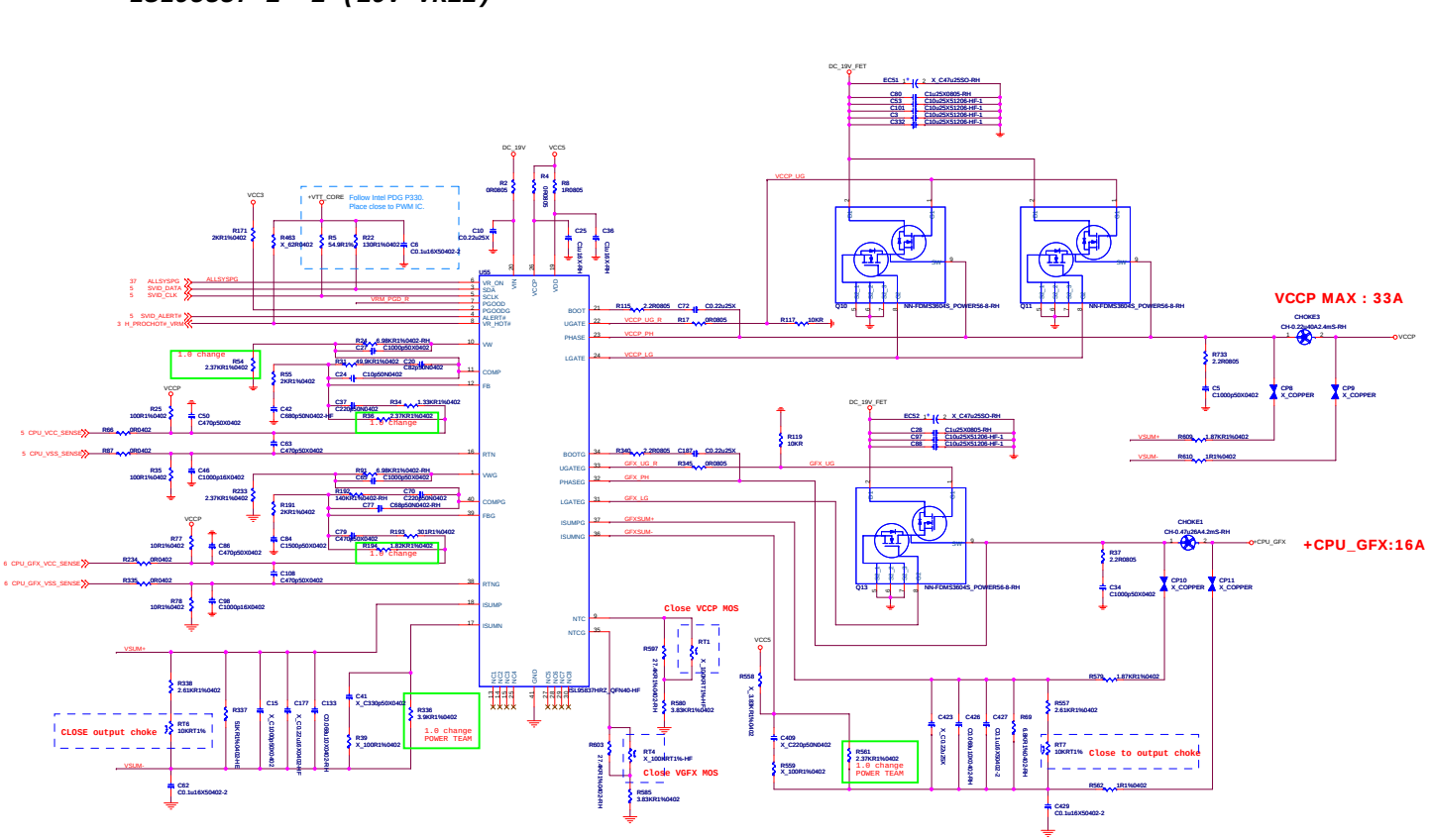
VSSA_SELECT

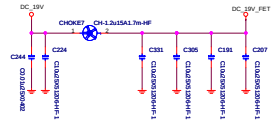


VCCSA_VID=LOW, 0.9V
VCCSA_VID=HIGH, 0.85V

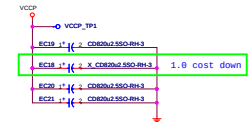
MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: CPU_SA POWER	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 35 of 42	

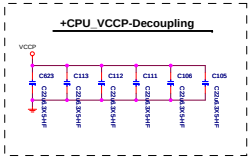
ISL95837 1 +1 (19V VR12)



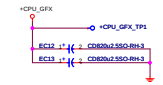


+CPU_VCCP Output Caps

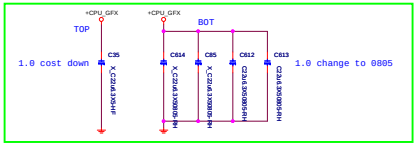


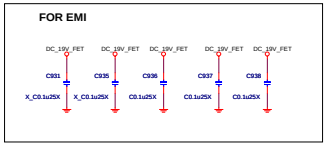


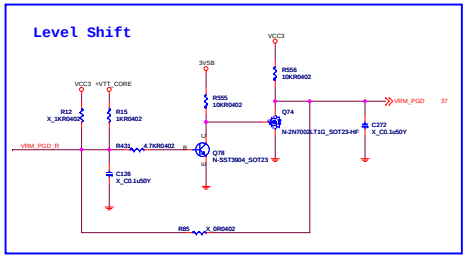
+CPU_GFX Output Caps



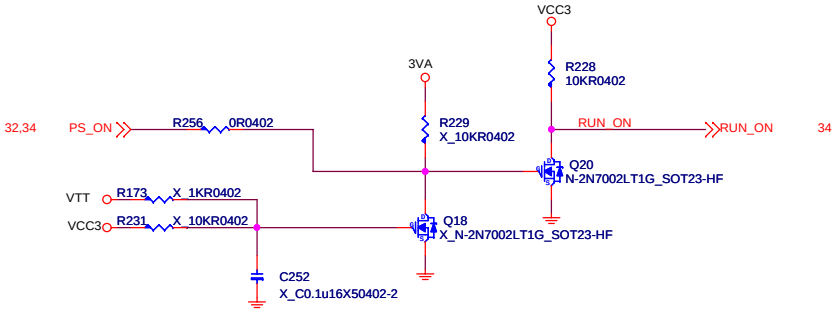
+CPU_GFX Decoupling



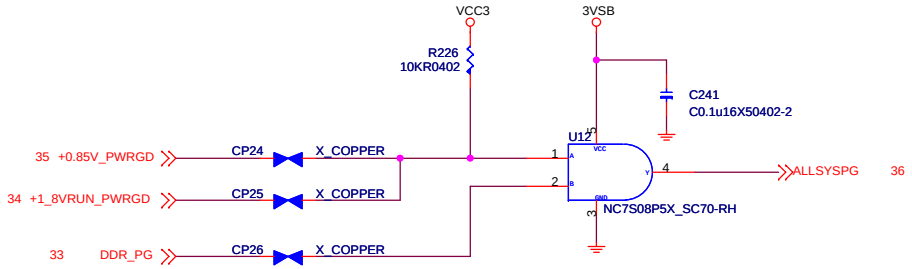


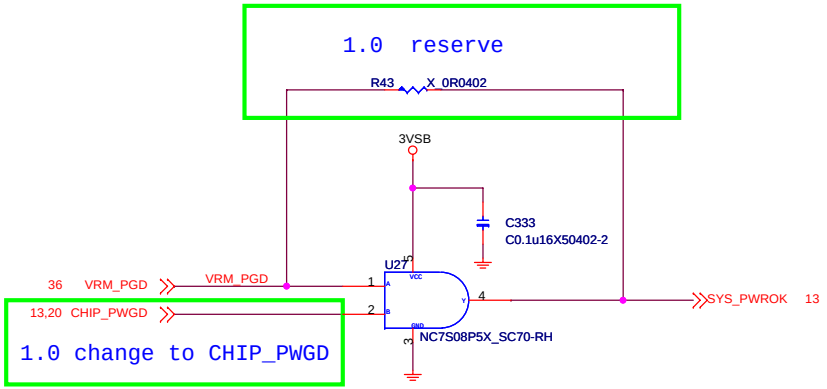


MICRO-STAR INT'L CO.,LTD	
MS-A9281	
Size: D	Document Description: CPU CORE (ISL95837)
Rev: 1.1	
Date: Tuesday, December 18, 2012	Sheet: 36 of 42



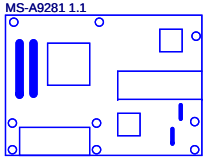
VRM ENABLE



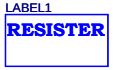


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A9281	
Size: Custom	Document Description: ACPI Controller	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 37 of 42	

PCB1
MS-A9281 1.1

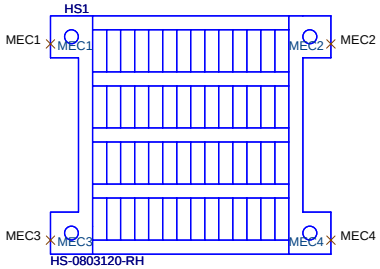


LABEL1

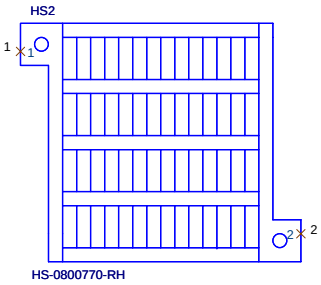


BIOS LABEL

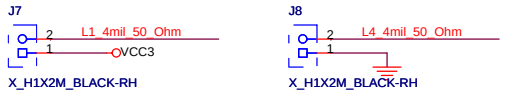
CPU Sink



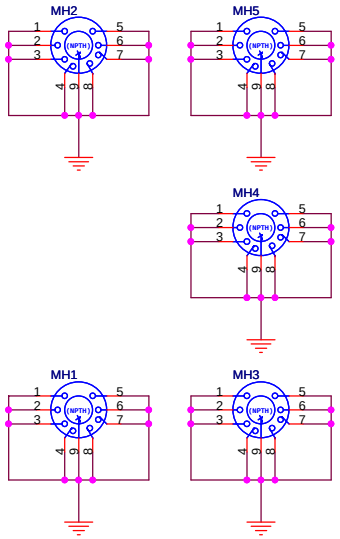
PCH Sink



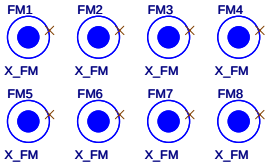
Single End 50ohm



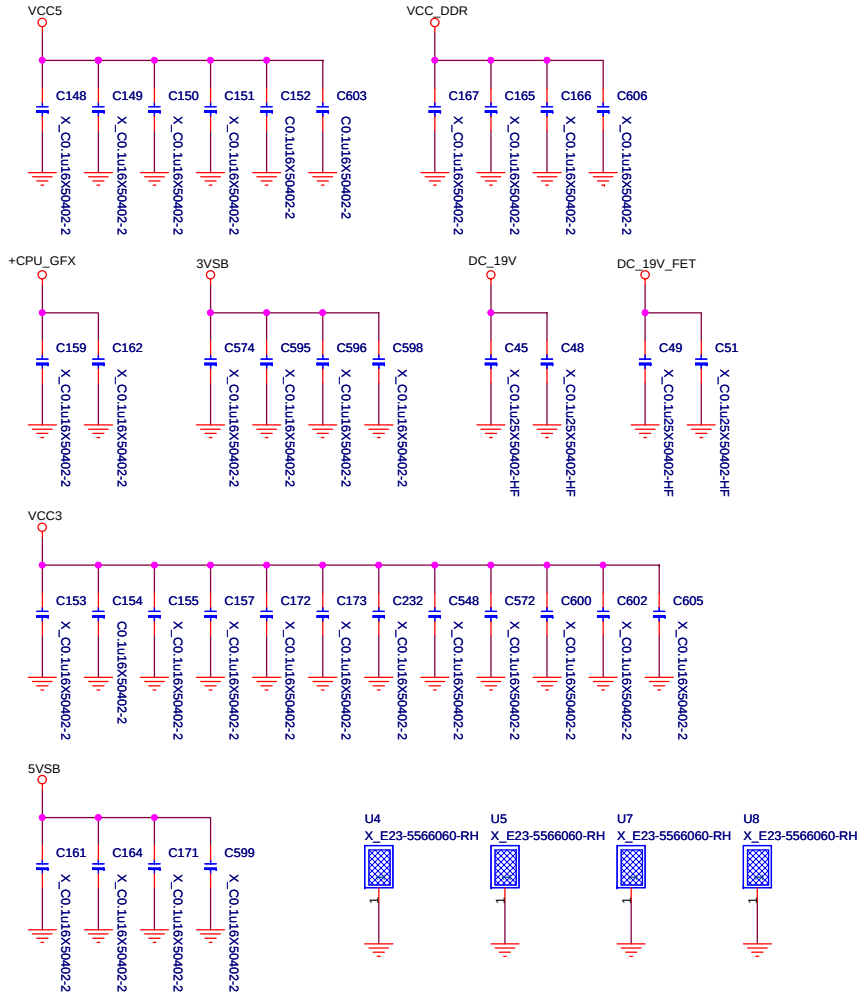
Mounting Holes



Optical Fiducial Marks-120

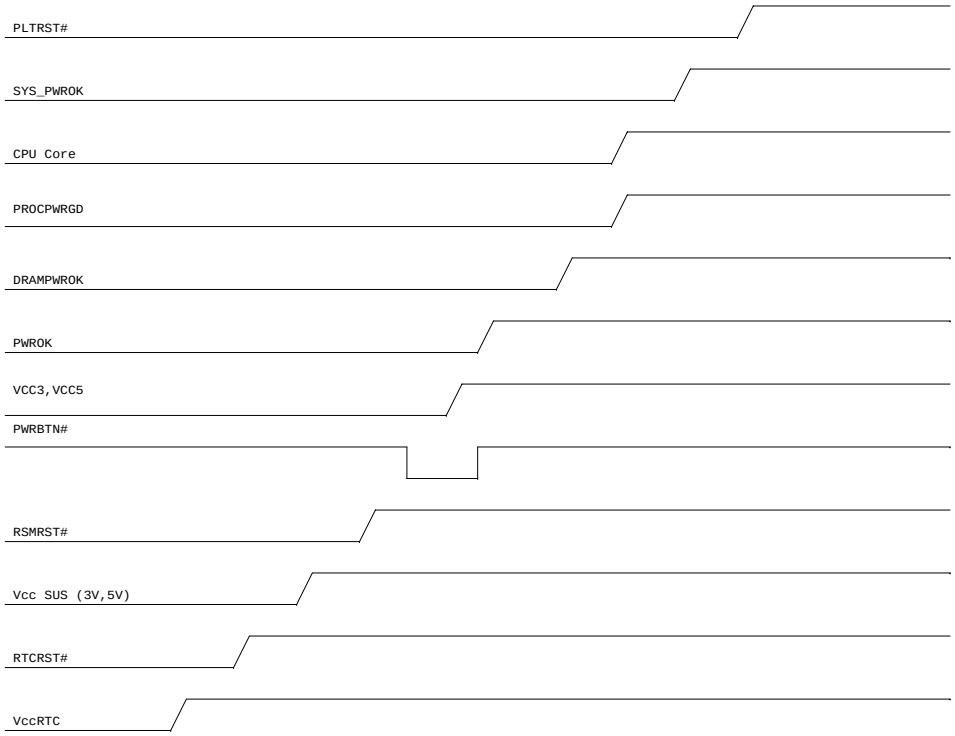


EMI

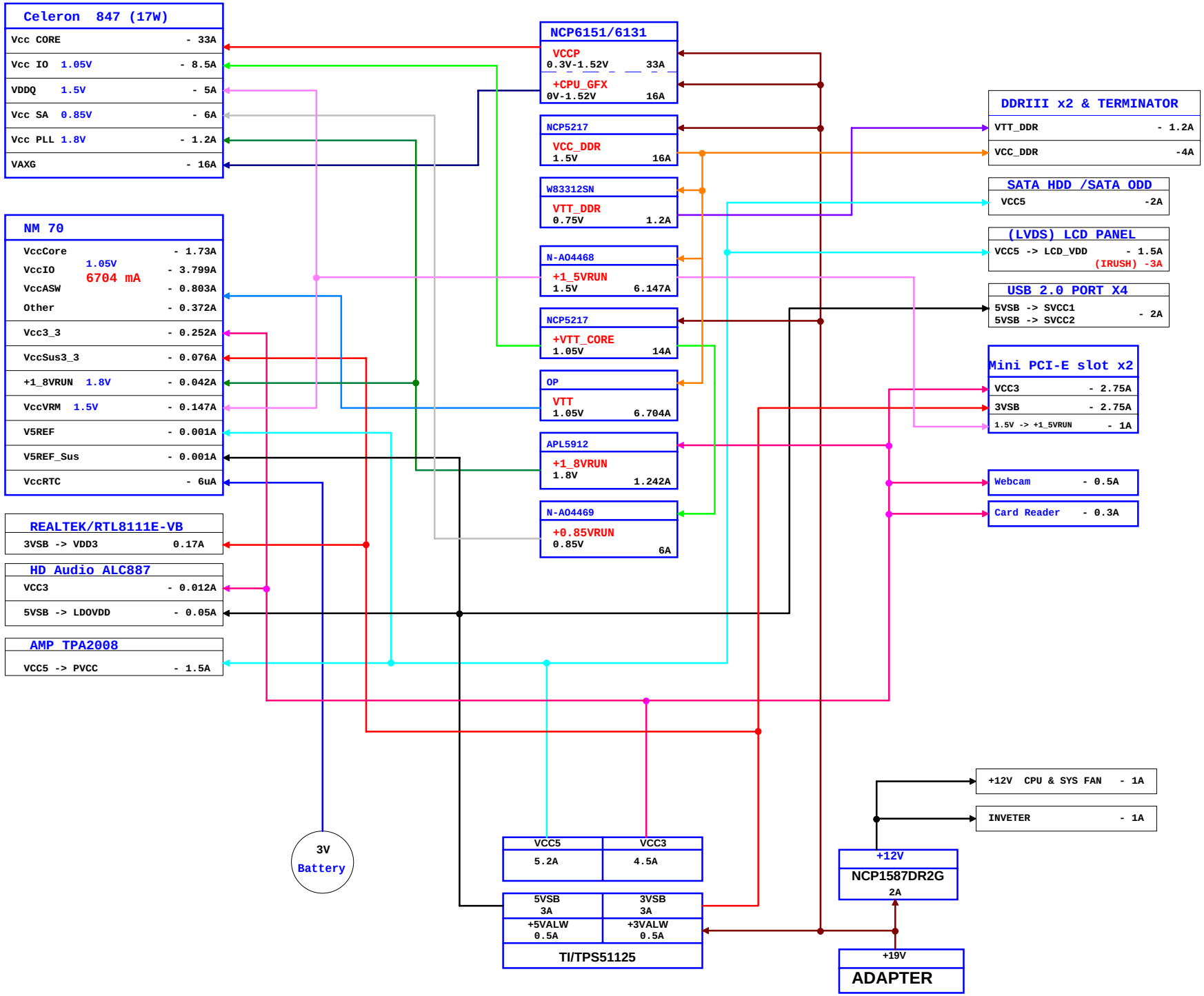


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A9281	
Size: Custom	Document Description: Manual Parts	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 38 of 42	

Power Sequencing and Reset Signal Timings (NM 70)



MICRO-STAR INT'L CO.,LTD		
MS-A9281		
Size: Custom	Document Description: Power Sequencingv	Rev: 1.1
Date: Tuesday, December 18, 2012	Sheet 39 of 42	



MICRO-STAR INT'L CO.,LTD

MS-A9281

Size: Custom | Document Description: Power Delivery | Rev: 1.1

Date: Tuesday, December 18, 2012 | Sheet 40 of 42

0A change to 1.0

01. Page 03 Modify TRMTRIP# circuit.

02. Page 03 DRAMRST# enable control pin change to SIO.

03. Page 05 Remove CAP & Change to 0805 for Cost down.

04. Page 06 Remove CAP for Cost down.

05. Page 09 DIMM1 CONNECTOR chang to N13-2040790-CK3 . (cost down)

06. Page 10 change USB3.0 connector.

07. Page 10 reserve C43 for USB3.0 controller loss.

08. Page 10 Modify USB3.0 SPI ROM circuit.

09. Page 10 reserve USB2.0 SKU circuit.

10. Page 11 Change PCH SPI ROM POWER to VCC3.

11. Page 12 reserve PCH GPIO26 to USB3.0/2.0 SKU detect.

12. Page 16 reserve PCH GPIO57 to FAN SKU detect.

13. Page 16 Modify PCH_GPIO36 Double pull high low R510 no stuff.

14. Page 20 Add about FAN circuit.

15. Page 20 Modify Temperature SENSING CIRCUIT.

16. Page 23 Change CAP to 0805 for Cost down.

17. Page 24 mini PCIE CONNECTOR change to N11-0520240-K06 . (cost down)

18. Page 25 Change CAP to 0805 for Cost down.

19. Page 26 Add FAN circuit.

20. Page 27 OSD POWER change to VCC3

21. Page 27 Modify OSD circuit. (GPIO3 change to GPIO6)

22. Page 29 Change LVDS Connector.

23. Page 29 Panel Backlight Brightness Control change to PCH.

24. Page 30 Remove SPEAKER for Cost down.

25. Page 31 Remove CAP for Cost down.

26. Page 32 Remove CAP & change to 0805 for Cost down.

27. Page 33 Modify VCC_DDR circuit. (POWER TEAM)
    CHOKE2 change to L04-05A7211-L65
    R720 change to 13K ohm
    R729 change to 10.2K ohm

    Change CAP to 0805 for Cost down.
    Remove Q16 for Cost down.

28. Page 34 Modify +VTT_CORE POWER circuit. (POWER TEAM)
    R565 change to 7.5 Kohm
    R567 change to 24K ohm
    R599 change to 8.45K ohm

    Remove Q30 & CAP for Cost down & current noise.

29. Page 36 Modify CPU POWER circuit. (POWER TEAM)
    R194 change to 1.82 Kohm
    R336 change to 3.9K ohm
    R36 change to 2.37K ohm
    R561 change to 2.37K ohm
    R54 change to 2.37K ohm

    Remove CAP & change to 0805 for Cost down & current noise.

30. Page 37 Modify ACPI circuit.

31. New BOM for Touch : Cfg-USB3T OPT:B **11/08**
    Cfg-USB2T OPT:C

1.1 change to 1.1

01. Page 29 LVDS connector change to N32-2200120-H06.

Panther Point (Mobile)

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO0	BMBUSY#	I/O	CORE	Y	3.3V	GPI	PCH_GPIO0	Pull-up 10K to VCC3	No USE
GPIO1	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	NEC_SMIB	Pull-up 10K to VCC3	USB3.0
GPIO2	PIRQE#	I/OD	CORE	Y	5V	GPI	PCH_GPIO2	Pull-up 8.2K to VCC3	+BKL
GPIO3	PIRQF#	I/OD	CORE	Y	5V	GPI	PCH_GPIO3	Pull-up 8.2K to VCC3	-BKL
GPIO4	PIRQG#	I/OD	CORE	Y	5V	GPI	PCH_GPIO4	Pull-up 8.2K to VCC3	+Vol
GPIO5	PIRQH#	I/OD	CORE	Y	5V	GPI	PCH_GPIO5	Pull-up 8.2K to VCC3	-Vol
GPIO6	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	PCH_GPIO6	Pull-up 10K to VCC3	No USE
GPIO7	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	PCH_GPIO7	Pull-up 10K to VCC3	No USE
GPIO8	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	ICC_EN	Pull-down	STRAP
GPIO9	OC5#	I/O	Suspend	Y	3.3V	Native	USB_OC5#	Pull-up 10K to 3VSB	OC5#
GPIO10	OC6#	I/O	Suspend	Y	3.3V	Native	USB_OC0#	Pull-up 10K to 3VSB	OC0#
GPIO11	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_GPIO11	Pull-up 10K to 3VSB	No USE
GPIO12	LAN_PHY_PWR_CTRL	I/O	Suspend	Y	3.3V	Native	T_REST#	N/A	T_REST#
GPIO13	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	SIO_PME#	Pull-up 4.7K to 3VSB	PME#
GPIO14	OC7#	I/O	Suspend	Y	3.3V	Native	NC	N/A	No USE
GPIO15	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	TLSEN	N/A	No USE
GPIO16	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	Pull-UP 10K to VCC3	No USE
GPIO17	Unmultiplexed	I/O	CORE	N	3.3V	GPI	PCH_GPIO17	Pull-up 10K to VCC3	No USE
GPIO18	PCIECLKRQ1#	I/O	CORE	N	3.3V	Native	PCIE_CLKREQ#1	Pull-up 10K to VCC3	PCIECLKREQ1#
GPIO19	SATA1GP	I/O	CORE	N	3.3V	GPI	BBS_BIT0	Pull-up 10K to VCC3	STRAP
GPIO20	PCIECLKRQ2# SMI#	I/O	CORE	N	3.3V	Native	PCIECLKREQ2#	Pull-up 10K to VCC3	PCIECLKREQ2#
GPIO21	SATA0GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO21	Pull-up 10K to VCC3	No USE
GPIO22	SCLOCK	I/O	CORE	N	3.3V	GPI	PCH_GPIO22	Pull-up 10K to VCC3	No USE
GPIO23	LDRQ1#	I/O	CORE	N	3.3V	Native	NC	N/A	No USE
GPIO24	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	Pull-up 10K to 3VSB	No USE
GPIO25	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ3#	Pull-up 10K to VCC3	PCIECLKREQ3#
GPIO26	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKREQ4#	Pull-up 10K to 3VSB	No USE
GPIO27	Unmultiplexed	I/O	DSW	N	3.3V	GPI	DSW_WAKE#	Pull-up 10K to 3VA	No USE
GPIO28	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PLL_ODVR_EN	N/A	No USE
GPIO29	SLP_LAN#	I/O	Suspend	N	3.3V	Native	SLP_LAN#	Pull-up 10K to 3VSB	No USE
GPIO30	SUSWARN# SUSPWRDNACK	I/O	Suspend	N	3.3V	Native	SUS_WARN#	Pull-up 10K to 3VSB	SUS_WARN#
GPIO31	Unmultiplexed	I/O	DSW	N	3.3V	GPI	AC_PRESENT	Pull-up 10K to 3VA	No USE
GPIO32	only CLKRUN#	I/O	CORE	N	3.3V	Native	CLKRUN#	Pull-up 8.2K to VCC3	No USE
GPIO33	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	HDA_DOCK_EN#	N/A	No USE
GPIO34	STP_PCI#	I/O	CORE	N	3.3V	GPI	STP_PCI#	Pull-up 10K to VCC3	No USE
GPIO35	NMI#	I/O	CORE	N	3.3V	GPO	CAMERA_ON#	N/A	CAMERA_ON#
GPIO36	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	Pull-up 10K to VCC3	STRAP
GPIO37	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	Pull-down 10K	STRAP
GPIO38	SLOAD	I/O	CORE	N	3.3V	GPI	WLAN1_PWRON	Pull-up 10K to VCC3	WLAN1_PWRON
GPIO39	SDATAOUT0	I/O	CORE	N	3.3V	GPI	WLAN2_PWRON	Pull-up 10K to VCC3	WLAN2_PWRON
GPIO40	OC1#	I/O	Suspend	N	3.3V	Native	USB_OC0#	Pull-up 10K to 3VSB	OC0#
GPIO41	OC2#	I/O	Suspend	N	3.3V	Native	USB_OC0#	Pull-up 10K to 3VSB	OC0#
GPIO42	OC3#	I/O	Suspend	N	3.3V	Native	USB_OC0#	Pull-up 10K to 3VSB	OC0#
GPIO43	OC4#	I/O	Suspend	N	3.3V	Native	USB_OC4#	Pull-up about 3VSB	OC4#
GPIO44	PCIECLKRQ5#	I/O	Suspend	N	3.3V	Native	CHARGER_EN	Pull-up 10K to 3VSB	CHARGER_EN
GPIO45	PCIECLKRQ6#	I/O	Suspend	N	3.3V	Native	CHARGER_S0	Pull-up 10K to 3VSB	CHARGER_S0

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO46	PCIECLKRQ7#	I/O	Suspend	N	3.3V	Native	CHARGER_S1	Pull-up 10K to 3VSB	CHARGER_S1
GPIO47	PEG_A_CLKRQ#	I/O	Suspend	N	3.3V	Native	PEGACLKREQ#	Pull-up 10K to 3VSB	No USE
GPIO48	SDATAOUT1	I/O	CORE	N	3.3V	GPI	PCH_GPIO48	Pull-up 10K to VCC3	No USE
GPIO49	SATA5GP TEMP_ALERT#	I/O	CORE	N	3.3V	GPI	PCH_GPIO49	Pull-up 10K to VCC3	No USE
GPIO50	Unmultiplexed	I/O	CORE	N	5V	Native	PCH_GPIO50	Pull-up 8.2K to VCC3	No USE
GPIO51	Unmultiplexed	I/O	CORE	N	3.3V	Native	BBS_BIT1	N/A	STRAP
GPIO52	Unmultiplexed	I/O	CORE	N	5V	Native	PCH_GPIO52	Pull-up 8.2K to VCC3	No USE
GPIO53	Unmultiplexed	I/O	CORE	N	3.3V	Native	PCH_GPIO53	N/A	No USE
GPIO54	Unmultiplexed	I/O	CORE	N	5V	Native	PCH_GPIO54	Pull-up 10K to VCC3	No USE
GPIO55	Unmultiplexed	I/O	CORE	N	3.3V	Native	PCH_GPIO55	N/A	No USE
GPIO56	PEG_B_CLKRQ#	I/O	Suspend	N	3.3V	Native	PEGBCLKRQ#	Pull-up 10K to 3VSB	No USE
GPIO57	Unmultiplexed	I/O	Suspend	N	3.3V	GPI	PCH_GPIO57	Pull-up 10K to 3VSB	No USE
GPIO58	SML1CLK	I/O	Suspend	N	3.3V	Native	SML1_CLK	Pull-up 2.2K to 3VSB	SML1CLK
GPIO59	OC0#	I/O	Suspend	N	3.3V	Native	USB_OC0#	Pull-up 10K to 3VSB	OC0#
GPIO60	SML0ALERT#	I/O	Suspend	N	3.3V	Native	DRAMRST_CNTRL_PCH	Pull-up 10K to 3VSB	DEEP S3
GPIO61	SUS_SATA#	I/O	Suspend	N	3.3V	Native	NC	N/A	No USE
GPIO62	SUSCLK	I/O	Suspend	N	3.3V	Native	NC	N/A	No USE
GPIO63	SLP_S5#	I/O	Suspend	N	3.3V	Native	SLP_S5#	N/A	SLP_S5#
GPIO64	CLKOUTFLEX0	I/O	CORE	N	3.3V	Native	TP_CLK_FLEX0	N/A	No USE
GPIO65	CLKOUTFLEX1	I/O	CORE	N	3.3V	Native	TP_CLK_FLEX1	N/A	No USE
GPIO66	CLKOUTFLEX2	I/O	CORE	N	3.3V	Native	TP_CLK_FLEX2	N/A	No USE
GPIO67	CLKOUTFLEX3	I/O	CORE	N	3.3V	Native	TP_CLK_FLEX3	N/A	CLK_48M_SIO
GPIO68	Unmultiplexed	I/O	CORE	N	3.3V	GPI	NC	N/A	No USE
GPIO69	Unmultiplexed	I/O	CORE	N	3.3V	GPI	NC	N/A	No USE
GPIO70	Unmultiplexed	I/O	CORE	N	3.3V	Native	NC	N/A	No USE
GPIO71	Unmultiplexed	I/O	CORE	N	3.3V	Native	NC	N/A	No USE
GPIO72	BATLOW#	I/O	Suspend	N	3.3V	Native	PCH_GPIO72	Pull-up 10K to 3VSB	No USE
GPIO73	PCIECLKRQ0#	I/O	Suspend	N	3.3V	Native	LANCLKRQ#	Pull-up 10K to 3VSB	LANCLKRQ#
GPIO74	SML1ALERT# PCHHOT#	I/O	Suspend	N	3.3V	Native	PCH_GIO74	Pull-up 10K to 3VSB	No USE
GPIO75	SML1DATA	I/O	Suspend	N	3.3V	Native	SML1_DATA	Pull-up 2.2K to 3VSB	SML1DATA

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MS-A9281

Size: Custom | Document Description: BIOS Request Form | Rev: 1.1

Date: Tuesday, December 18, 2012 | Sheet 42 of 42