MS-7765 Ver: 0D AIO(180mm X 275.45mm)

CPU:

INTEL -Sandy/Ivy Bridge LGA 1155 (SOCKET H2)

System Chipset:

INTEL-Q77 (PANTHER POINT)

OnBoard Chipset:

Audio Codec - REALTEK/ALC272
Audio AMPLIFIER - REALTEK/ALC105-GR
Gigabit LAN - INTEL/82579
SIO - NUVOTON/NCT6681D-B
Scaler - PARADE/DP701
Flash ROM: 128 Mb SPI (CHIP)

Main Memory:

DDRIII * 2 (Dual Channel)

Expansion Slots:

Mini PCI-e (X1) * 1
MSATA * 1

PWM:

Controller:Intersil/ISL6363CRZ &ISL6612 3+1ph

Other:

(SATA3-600MB/s) *1 + SATA(SATA2-300MB/s) *1
USB3.0 *2 (SIDE)
USB2.0 *4 (REAR)
USB2.0 *7 (On Board Connector)
DISPLAY PORT OUT*1
LVDS*1
DP_IN*1

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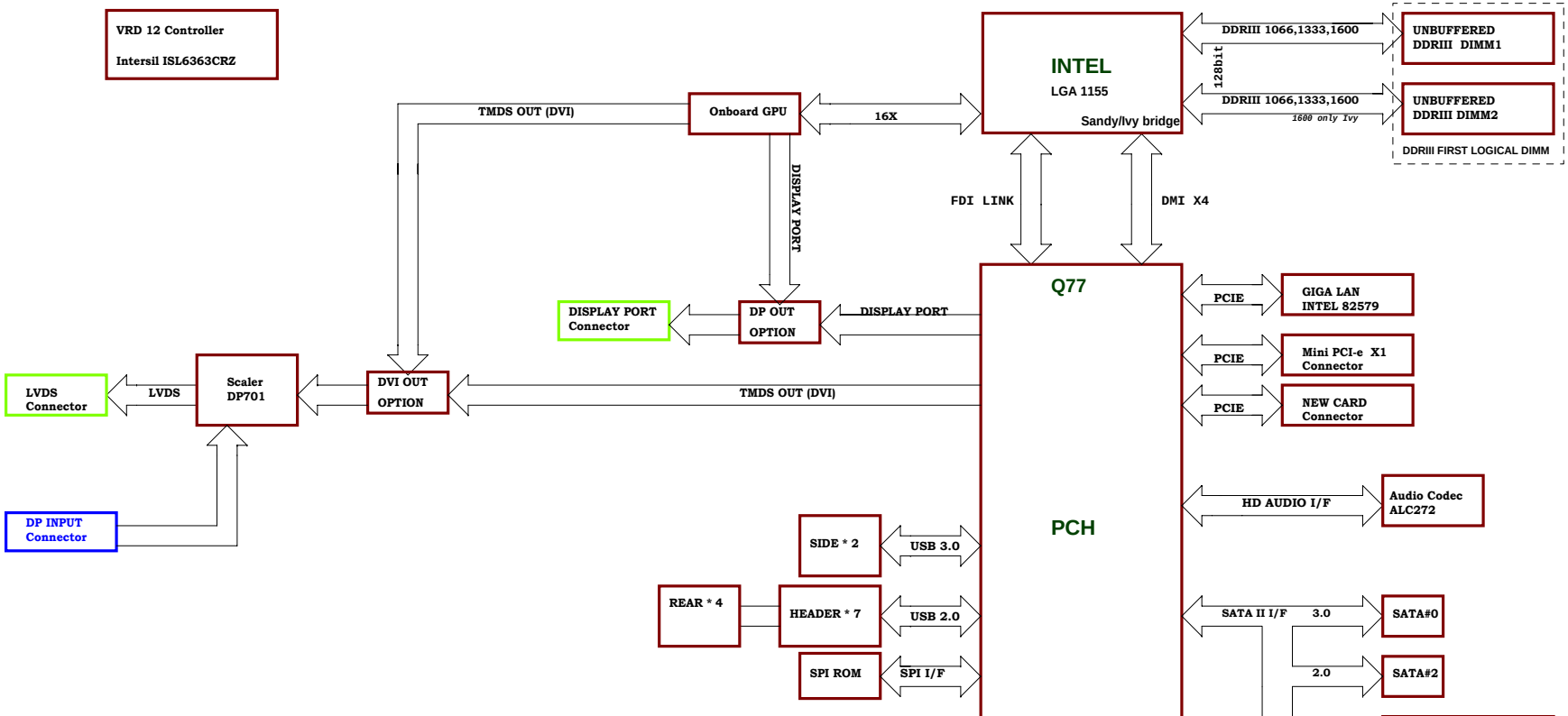

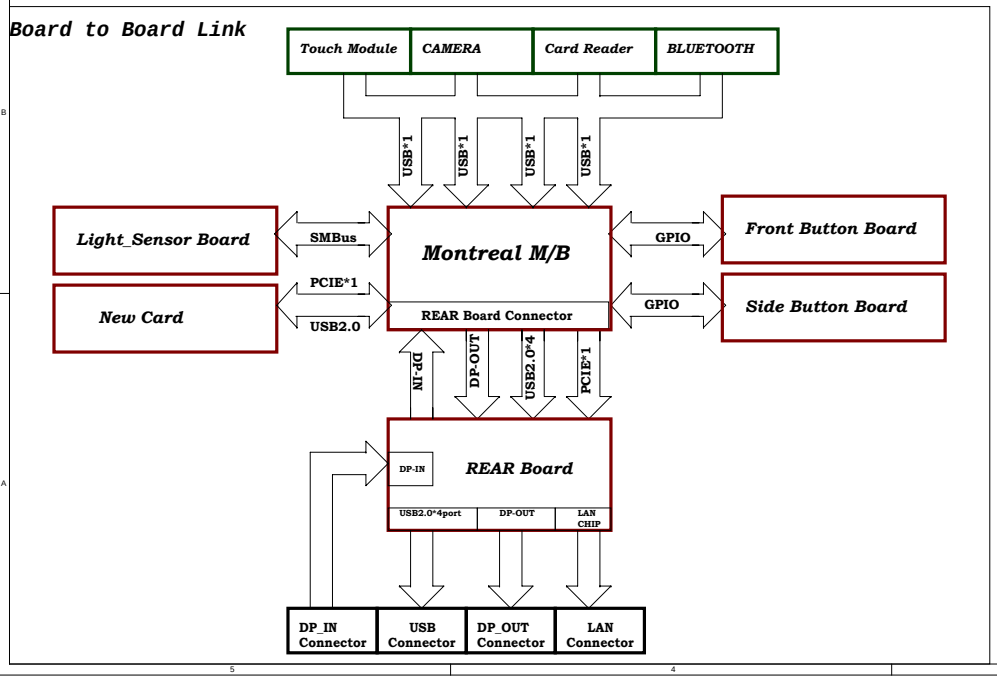

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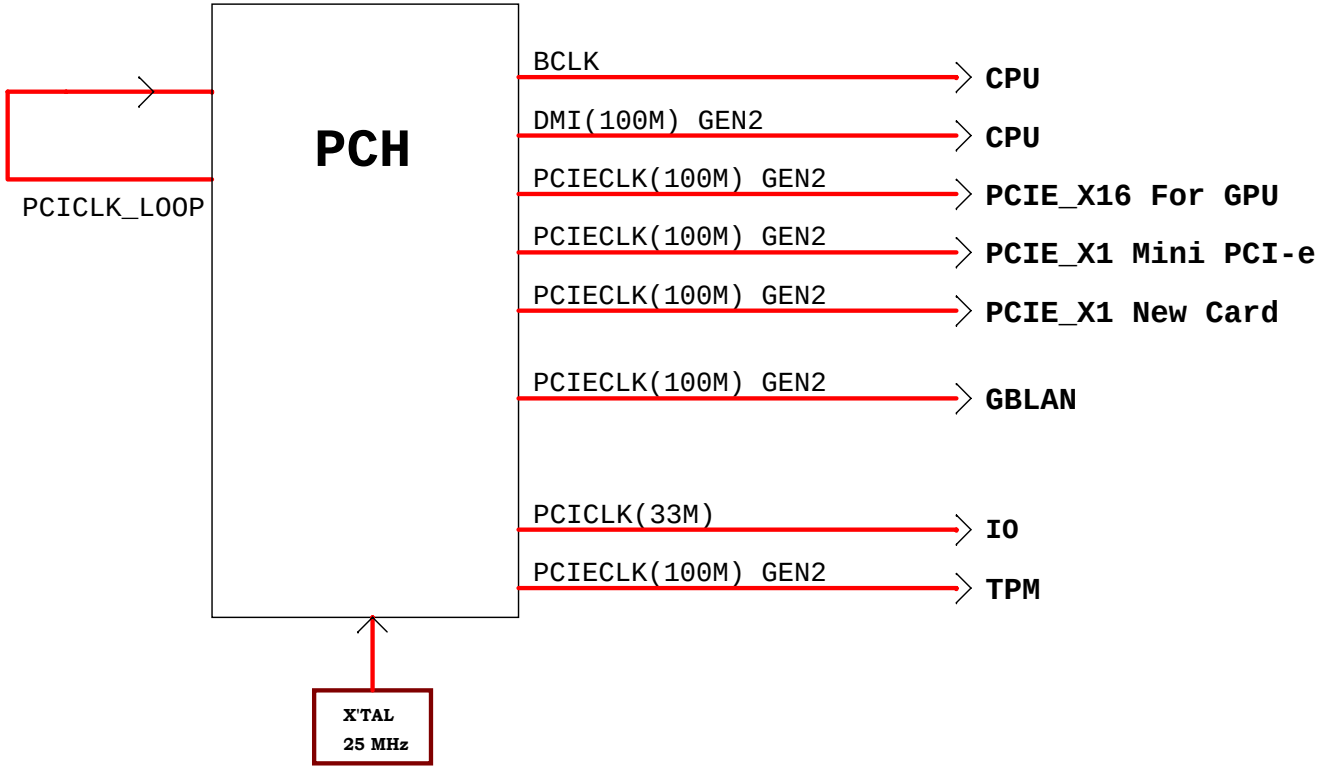
DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-B	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	N/A	
DIMM 3 CH-A	N/A	



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PCH

GPIO	Chip default Func	input/o	Chip default IO setting	Power well	TOL	SMI	Single Name	active H/L	internal/external pull H/L	external PH power well and power level	Location(X is mean sturff)	Value	Note
GPIO0	BMBUSY#	I/O	GPI	Main	3.3V	N	BM_BUSY#	NC	EXT_PH	(+VCC3)	R394	10K	
GPIO1	TACH1	I/O	GPI	Main	3.3V	N	PCH_GPIO1	NC	NC				
GPIO[5:2]	PIRQ[H:E]#	I/OD	GPI	Main	5 V	N	PCI_PIRQ[H:E]#	H	EXT_PH	(+VCC3)	RN7,RN11,RN12,R469	8.2K	
GPIO6	TACH2	I/O	GPI	Main	3.3V	N	MSATA_EN	L	EXT_PH	(+VCC3)	R927	10K	
GPIO7	TACH3	I/O	GPI	Main	3.3V	N	WIRELESS_EN	L	EXT_PH	(+VCC3)	R500	10K	
GPIO8	GPIO8	I/O	GPO	Resume	3.3V	N	IGC_EN_N	NC	EXT_PL	Ground	R474	1K	
GPIO9	OC5#	I/O	Native	Resume	3.3V	N	OC#10_11	NC	EXT_PH	3.3V resume(+3VSB)	R493	8.2K	
GPIO10	OC6#	I/O	Native	Resume	3.3V	Y	SMI#	NC	SMI#	3.3v main(+VCC3)	R1054	10K	
GPIO11	SMBALERT#	I/O	Native	Resume	3.3V	N	PCH_SMBALERT#	NC	EXT_PH	3.3V resume(+3VSB)	R921	10K	
GPIO12	LAN_PHY_PWR_CTRL	I/O	Native	Resume	3.3V	N	LAN_DISABLE#	L	INT_PH	3.3V resume (+LAN_3VSB)	R185	10K	R185 at Real IO board
GPIO13	HAD_DOCK_RST#	I/O	GPI	Resume	3.3V	N	SIO_PME#	L	EXT_PH	3.3V resume(+3VSB)	R926	10K	
GPIO14	OC7#	I/O	Native	Resume	3.3V	N	OC#7	L	EXT_PH	3.3V resume(+3VSB)	R488	8.2K	
GPIO15	GPIO15	I/O	GPO	Resume	3.3V	N	PCH_GPIO15	NC	INT_PH		X_R533	1K	
GPIO16	SATA4GP	I/O	GPI	Main	3.3V	N	LIGHT_SENSOR_DET	H	EXT_PH	(+VCC3)	R386	10K	
GPIO17	GPIO17	I/O	GPI	Main	3.3V	N	DGPUPRSNT#	H	EXT_PH	(+VCC3)	R452	10K	
GPIO18	PCIECLKRQ1#(Mobile only)		Native	NA			NC						
GPIO19	SATA1GP	I/O	GPI	Main	3.3V	N	JUSB2_SENSE#B	NC	INT_PH	(+VCC3)	R401,X_R412	10K	
GPIO20	PCIECLKRQ2#	I/O	Native	Main	3.3V	N	PCIECLKRQ2#	NC	EXT_PH	(+VCC3)	R826,X_R831	10K	
GPIO21	SATA0GP	I/O	GPI	Main	3.3V	N	CARD_READER_DET	NC	EXT_PH	(+VCC3)	R873	10K	
GPIO22	SCLOCK	I/O	GPI	Main	3.3V	N	MB_ID0	NC	EXT_PH	(+VCC3)	R405,X_R404	10K	
GPIO23	LDRQ1#	I/O	Native	Main	3.3V	N	LDRQ1#	NC	NC		X_R929	10K	
GPIO24	PROC_MISSING	I/O	GPO	Resume	3.3V	N	H_SKTOCC_PCH_R	NC	EXT_PH	3.3V resume(+VBAT0)	X_R1032,R1036	2M	
GPIO25	PCIECLKRQ3#(Mobile o	I/O	Native	NA	3.3V	N	NC	NA					
GPIO26	PCIECLKRQ4#(Mobile a	I/O	Native	NA	3.3V	N	NC	NA					
GPIO27	GPIO27	I/O	GPI	DSW	3.3V	N	HDOUT_AMP_DIS#	H	EXT_PH	3.3V DSW(+FATX_3VSB)	R484	10K	
GPIO28	GPIO28	I/O	GPO	Resume	3.3V	N	OD_PLL_VR_EN	NC	EXT_PH	3.3V resume(+3VSB)	X_440,R441	1K	
GPIO29	SLP_LAN#	I/O	GPI	Resume	3.3V	N	SLP_LAN#	NC	??		X_R925	10K	default to SLP_LAN#
GPIO30	SUSWARN#	I/O	Native	Resume	3.3V	N	SUS_WARN#	NC					default to SUS_WARN#
GPIO31	GPIO31	I/O	GPI	DSW	3.3V	N	FRONT_OUT_DISABLE	H	EXT_PH	3.3V DSW(+FATX_3VSB)	R485	10K	
GPIO32	GPIO32	I/O	GPO	Main	3.3V	N	CLKRUN#	NC	EXT_PH	(+VCC3)	X_R409	10K	
GPIO33	GPIO33	I/O	GPO	Main	3.3V	N	SPI_HOLD_GPO#	L					
GPIO34	STP_PCI#	I/O	GPI	Main	3.3V	N	CLR_CMOS	NC	EXT_PH	(+VCC3)	R505	10K	
GPIO35	NMI#	I/O	GPO	Main	3.3V	N	SPI_WP#	L	EXT_PH	3.3V resume(+3.3V_ME)	R416,R417	2.2K	
GPIO36	SATA2GP	I/O	GPI	Main	3.3V	N	SATA2GP_PU	NC			X_R410,X_R420	10K	Internal pull-DOWN
GPIO37	SATA3GP	I/O	GPI	Main	3.3V	N	SATA3GP_PU	NC			X_R424,X_R880	10K	Internal pull-DOWN
GPIO38	SLOAD	I/O	GPI	Main	3.3V	N	MB_ID1		EXT_PH	(+VCC3)	R876,X_R877	10K	
GPIO39	SDATAOUT0	I/O	GPI	Main	3.3V	N	MB_ID2	L	EXT_PH	(+VCC3)	R425,X_R418	10K	
GPIO40	OC1#	I/O	Native	Resume	3.3V	N	USB_OCP#1	L	EXT_PH	3.3V resume(+USB20_SVCC0)	R710,R691		
GPIO41	OC2#	I/O	Native	Resume	3.3V	N	USB_OCP#2	L	EXT_PH	3.3V resume(+3VSB)	R490	8.2K	
GPIO42	OC3#	I/O	Native	Resume	3.3V	N	USB_OCP#3	L	EXT_PH	3.3V resume(SVCC3)	R144,R145		
GPIO43	OC4#	I/O	Native	Resume	3.3V	N	USB_OCP#4	L	EXT_PH	3.3V resume(+USB20_SVCC1)	R714,R699		
GPIO44	PCIECLKRQ5	I/O	Native	Resume	3.3V	N	PCIECLKRQ5#	L	EXT_PH	3.3V resume(+3VSB)	R436	10K	
GPIO45	PCIECLKRQ6	I/O	Native	Resume	3.3V	N	PCH_GPI45	NC	EXT_PH	3.3V resume(+3VSB)	R830	10K	
GPIO46	PCIECLKRQ7	I/O	Native	Resume	3.3V	N	ME_CTL	NC	EXT_PH	3.3V resume(+3VSB)	R458	10K	
GPIO47	PEG_A_CLKRQ#(Mobile	I/O	Native	na	3.3V	N							
GPIO48	SDATAOUT1	I/O	GPI	Main	3.3V	N	MB_ID3	L	EXT_PH	(+VCC3)	R395,X_R391	10K	
GPIO49	SATA5GP and temp_aler	I/O	GPI	Main	3.3V	N	MULTI_TOUCH_DET	L	EXT_PH	(+VCC3)	R400	10K	
GPIO50	REQ1#	I/O	Native	Main	5V	N	PCI_REQ1#	NC	EXT_PH	(+VCC3)	RN11	8.2K	
GPIO51	GNT1#	I/O	Native	Main	3.3V	N	PGNT#1	NC	INT_PH		X_R509,X_R510	10K	
GPIO52	REQ2#	I/O	Native	Main	3.3V	N	PCI_REQ2#	NC	EXT_PH	(+VCC3)	RN11	8.2K	
GPIO53	GNT2#	I/O	Native	Main	3.3V	N	PGNT#2		INT_PH		X_R451	1K	
GPIO54	REQ3#	I/O	Native	Main	5V	N	PCI_REQ3#	NC	EXT_PH	(+VCC3)	RN12	8.2K	
GPIO55	GNT3#	I/O	Native	Main	3.3V	N	PGNT#3		INT_PH		X_R467	1K	
GPIO56	PEG_B_CLKRQ#(Mobile	I/O	Native	na	3.3V	N							
GPIO57	GPIO57	I/O	GPI	Resume	3.3V	N	COM_PORT_DET#	L	EXT_PH	3.3V resume(+3VSB)	R463	10K	
GPIO58	SML1CLK	I/O	Native	Resume	3.3V	N	PCH_SML1CLK	NC	EXT_PH	3.3V resume(+3VSB)	R899	2.2K	
GPIO59	OC0#	I/O	Native	Resume	3.3V	N	OC#0_1	L	EXT_PH	3.3V resume(+USB30_PWR_RIGH	R351,R357		
GPIO60	SML0ALERT#	I/O	Native	Resume	3.3V	N	PCH_SML0ALERT#	L	EXT_PH	3.3V resume(+3VSB)	R920	2.2K	
GPIO61	SUS_STAT#	I/O	Native	Resume	3.3V	N	SUS_STAT#	NC	EXT_PH	3.3v main(+VCC3)	X_R448	10K	default to SUS_SATA#
GPIO62	SUSCLK	I/O	Native	Resume	3.3V	N	SUSCLK	NC(TP93)			TP93		
GPIO63	SLP_S5#	I/O	Native	Resume	3.3V	N	PCH_SLP_S5#	NC			SLP_S5#		
GPIO64	CLKOUTFLEX0	I/O	Native	CORE	3.3V	N	TP_CLKOUTFLEX0	NC(TP87)			TP87		
GPIO65	CLKOUTFLEX1	I/O	Native	CORE	3.3V	N	TP_CLKOUTFLEX1	NC(TP21)			TP21		
GPIO66	CLKOUTFLEX2	I/O	Native	CORE	3.3V	N	TP_CLKOUTFLEX2	NC(TP20)			TP20		
GPIO67	CLKOUTFLEX3	I/O	Native	CORE	3.3V	N	CK_48M_SIO_R	NC(TP100)			TP100		
GPIO68	TACH4	I/O	GPI	CORE	3.3V	N	PCH_GPIO68		EXT_PH	(+VCC3)	R483	10K	
GPIO69	TACH5	I/O	GPI	CORE	3.3V	N	LED_HEADER_DET#	NC(TP23)			TP23	1K	
GPIO70	TACH6	I/O	Native	CORE	3.3V	N	PS2_DET#	L	EXT_PH	(+VCC3)	R470	10K	
GPIO71	TACH7	I/O	Native	CORE	3.3V	N	TP_GPIO71	NC	EXT_PH	(+VCC3)	R468	10K	
GPIO72	GPIO72	I/O	Native	Resume	3.3V	N	PCH_GPI72	NC(TP88)	EXT_PH	3.3V resume(+3VSB)	X_R855	10K	
GPIO73	PCIECLKRQ0#	I/O	Native	NA	3.3V	N	NC						
GPIO74	SML1ALERT#/PCHHOT#	I/O	Native	Resume	3.3V	N	PCH_SML1ALERT#	NC	EXT_PH	3.3V resume(+3VSB)	R922	10K	
GPIO75	SML1DATA	I/O	Native	Resume	3.3V	N	PCH_SML1DATA		EXT_PH	3.3V resume(+3VSB)	R900	2.2K	

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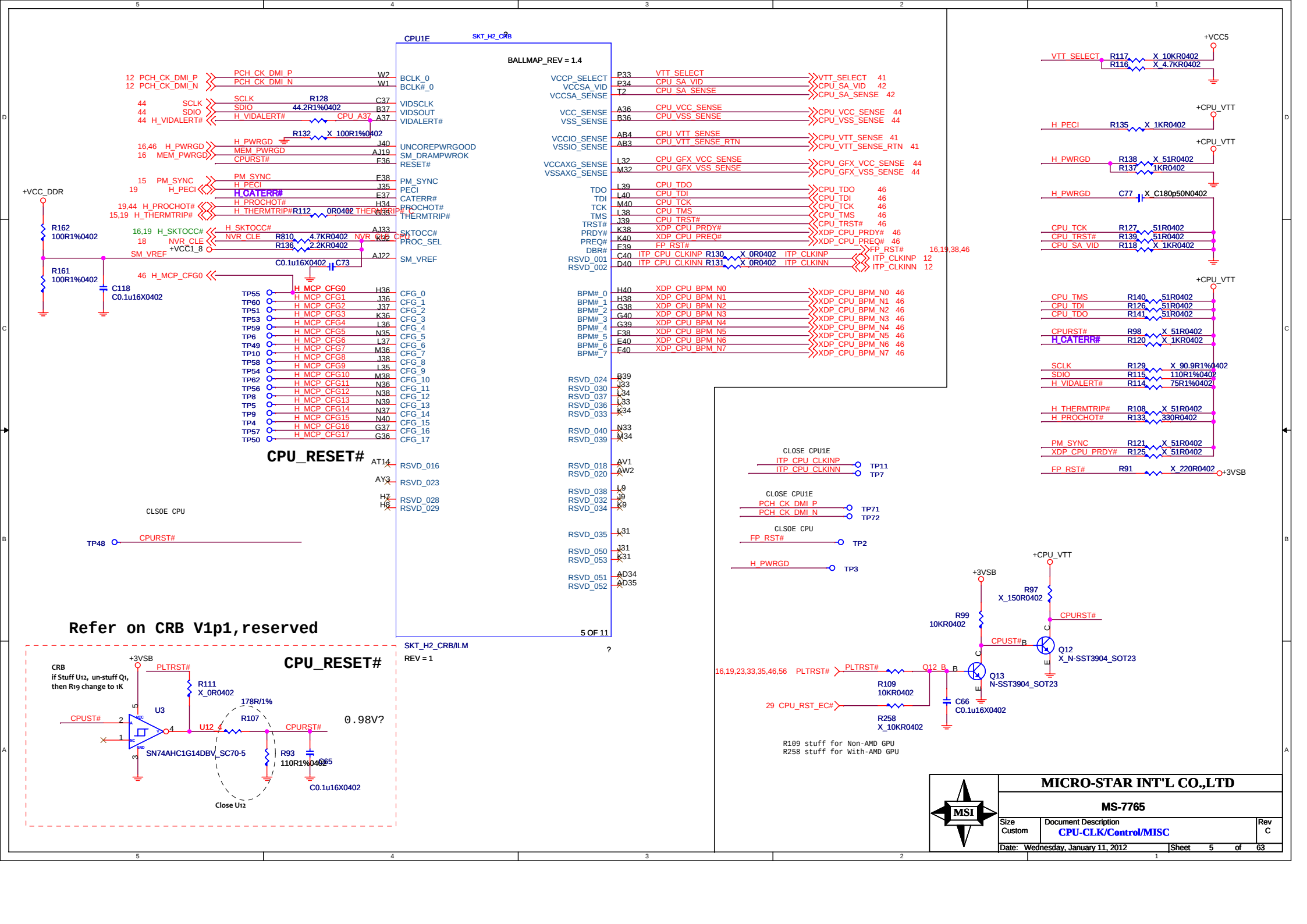
CPU1E
SKT_H2_CRB
BALLMAP_REV = 1.4
5 OF 11
SKT_H2_CRB/ILM
REV = 1
CPU_RESET#
Refer on CRB V1p1,reserved
CPU_RESET#
CRB
if Stuff U12, un-stuff Q1,
then R19 change to 1K
SN74AHC1G14DBV_SC70-5
Close U12
0.98V?
R109 stuff for Non-AMD GPU
R258 stuff for With-AMD GPU
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CPU-CLK/Control/MISC
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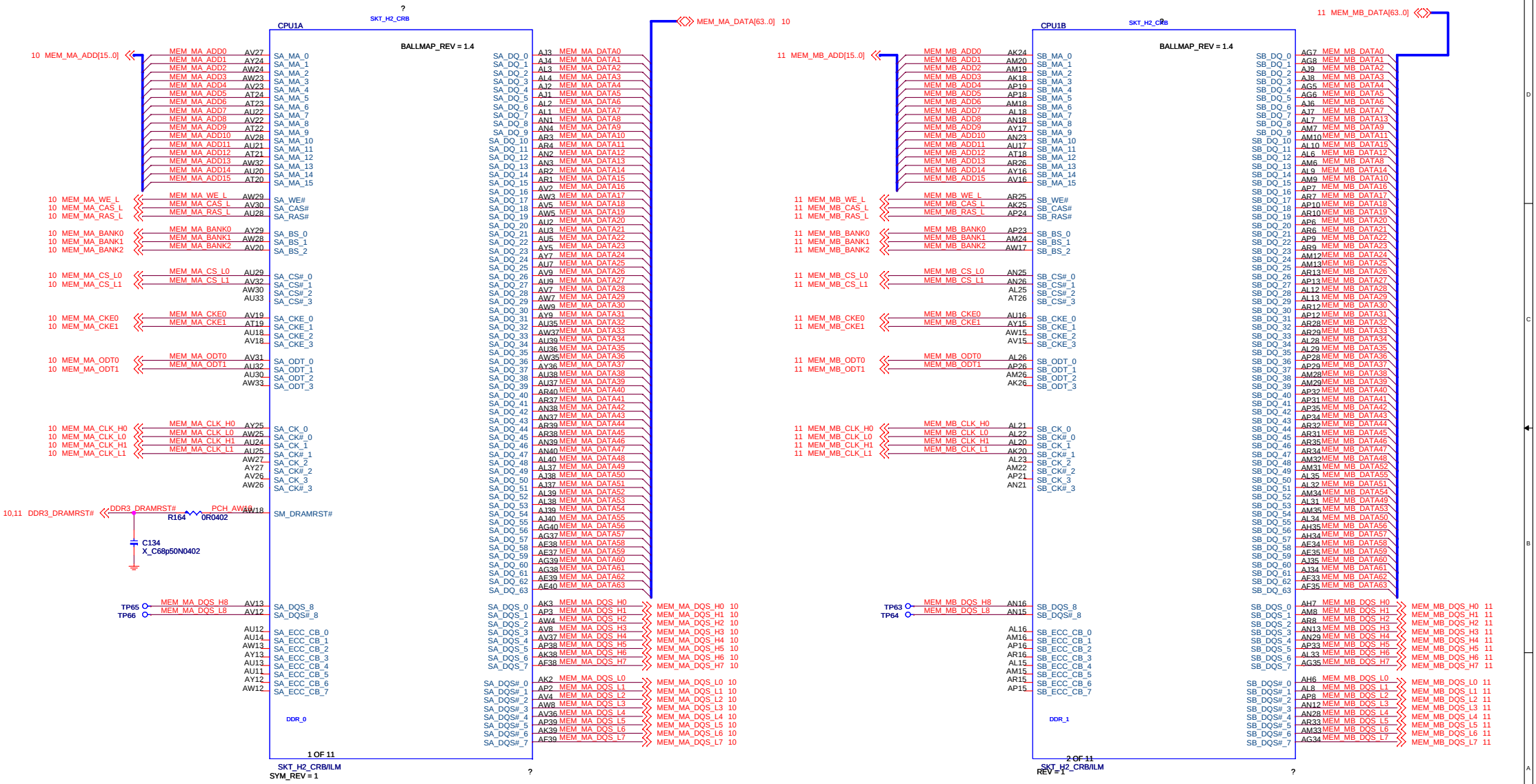

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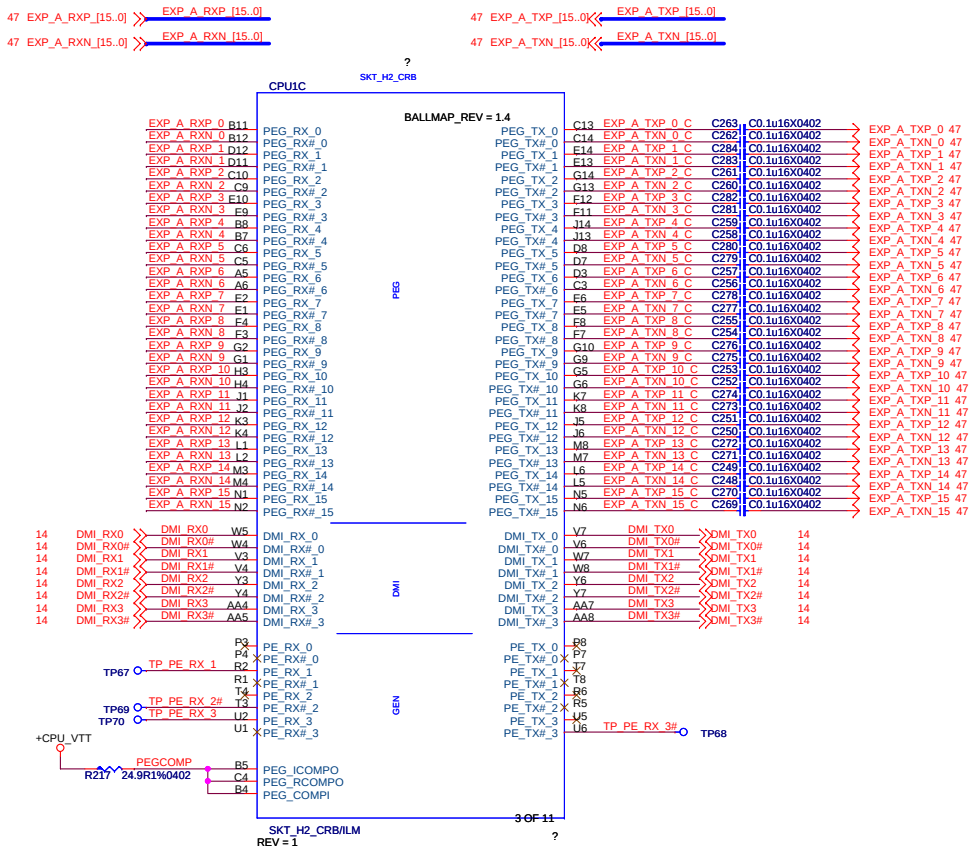
PEG & DMI



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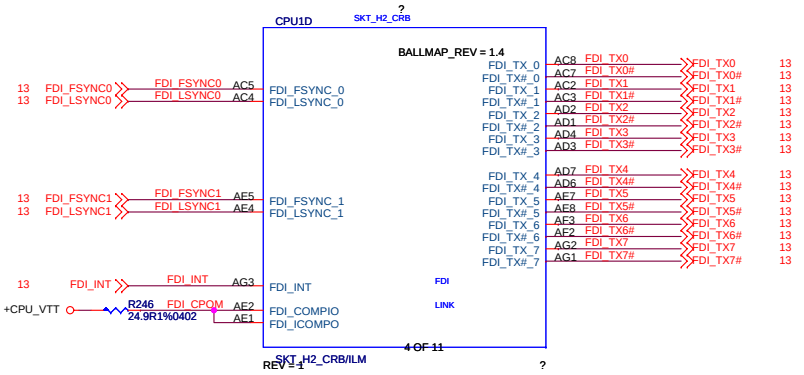

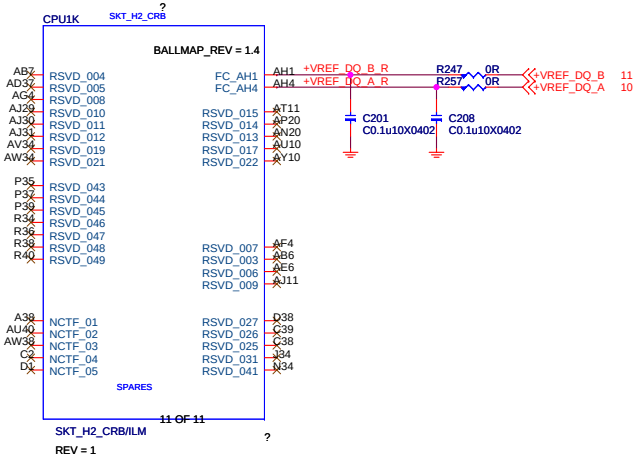

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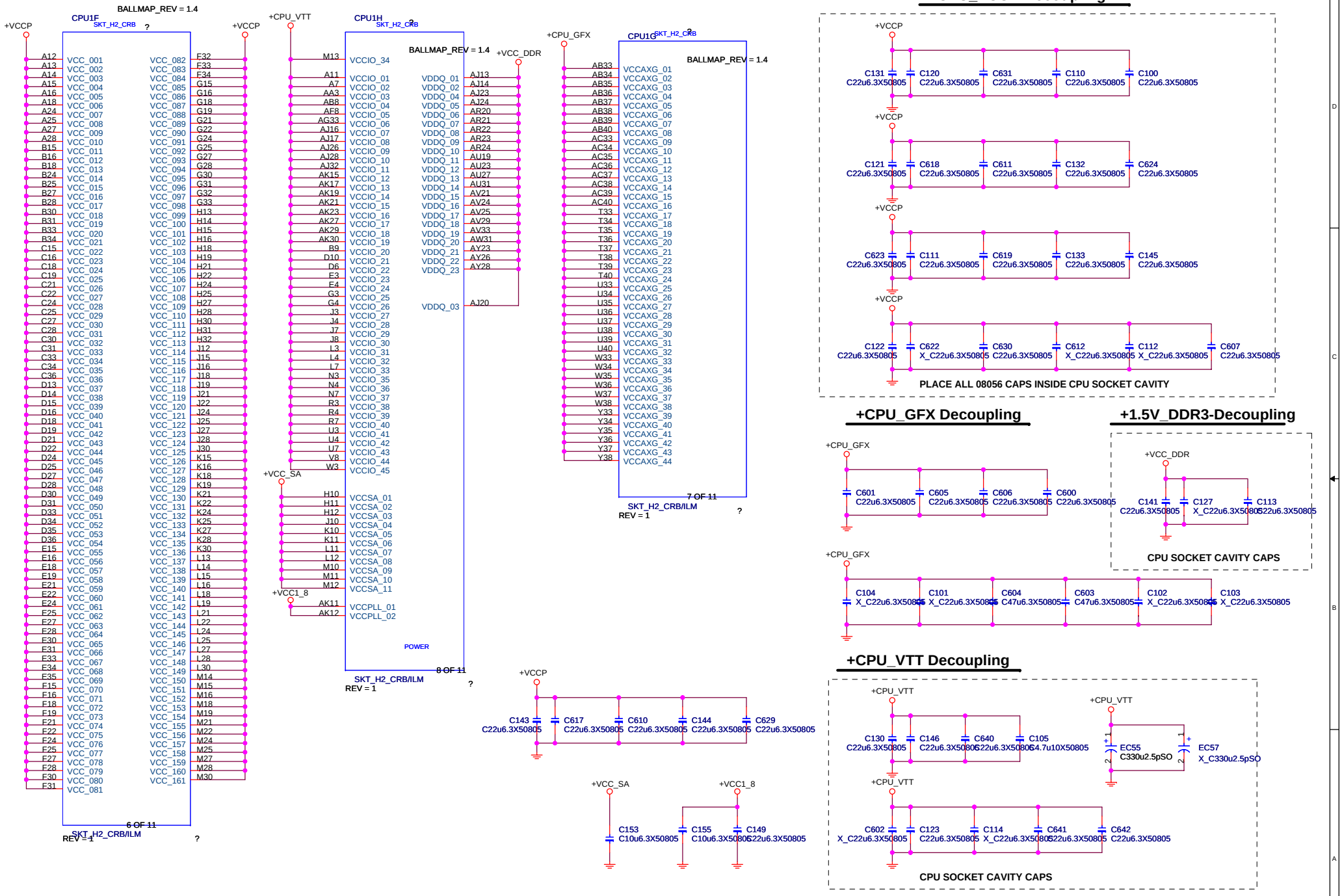
BALLMAP_REV = 1.4
CPU1F
SKT_H2_CRB
+VCCP
+VCCP
VCC_001 VCC_002 VCC_003 VCC_004 VCC_005 VCC_006 VCC_007 VCC_008 VCC_009 VCC_010 VCC_011 VCC_012 VCC_013 VCC_014 VCC_015 VCC_016 VCC_017 VCC_018 VCC_019 VCC_020 VCC_021 VCC_022 VCC_023 VCC_024 VCC_025 VCC_026 VCC_027 VCC_028 VCC_029 VCC_030 VCC_031 VCC_032 VCC_033 VCC_034 VCC_035 VCC_036 VCC_037 VCC_038 VCC_039 VCC_040 VCC_041 VCC_042 VCC_043 VCC_044 VCC_045 VCC_046 VCC_047 VCC_048 VCC_049 VCC_050 VCC_051 VCC_052 VCC_053 VCC_054 VCC_055 VCC_056 VCC_057 VCC_058 VCC_059 VCC_060 VCC_061 VCC_062 VCC_063 VCC_064 VCC_065 VCC_066 VCC_067 VCC_068 VCC_069 VCC_070 VCC_071 VCC_072 VCC_073 VCC_074 VCC_075 VCC_076 VCC_077 VCC_078 VCC_079 VCC_080 VCC_081
VCC_082 VCC_083 VCC_084 VCC_085 VCC_086 VCC_087 VCC_088 VCC_089 VCC_090 VCC_091 VCC_092 VCC_093 VCC_094 VCC_095 VCC_096 VCC_097 VCC_098 VCC_099 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110 VCC_111 VCC_112 VCC_113 VCC_114 VCC_115 VCC_116 VCC_117 VCC_118 VCC_119 VCC_120 VCC_121 VCC_122 VCC_123 VCC_124 VCC_125 VCC_126 VCC_127 VCC_128 VCC_129 VCC_130 VCC_131 VCC_132 VCC_133 VCC_134 VCC_135 VCC_136 VCC_137 VCC_138 VCC_139 VCC_140 VCC_141 VCC_142 VCC_143 VCC_144 VCC_145 VCC_146 VCC_147 VCC_148 VCC_149 VCC_150 VCC_151 VCC_152 VCC_153 VCC_154 VCC_155 VCC_156 VCC_157 VCC_158 VCC_159 VCC_160 VCC_161
6 OF 11
SKT_H2_CRB/ILM
REV = 1
+CPU_VTT
CPU1H
SKT_H2_CRB
BALLMAP_REV = 1.4
+VCC_DDR
VCCIO_34 VCCIO_01 VCCIO_02 VCCIO_03 VCCIO_04 VCCIO_05 VCCIO_06 VCCIO_07 VCCIO_08 VCCIO_09 VCCIO_10 VCCIO_11 VCCIO_12 VCCIO_13 VCCIO_14 VCCIO_15 VCCIO_16 VCCIO_17 VCCIO_18 VCCIO_19 VCCIO_20 VCCIO_21 VCCIO_22 VCCIO_23 VCCIO_24 VCCIO_25 VCCIO_26 VCCIO_27 VCCIO_28 VCCIO_29 VCCIO_30 VCCIO_31 VCCIO_32 VCCIO_33 VCCIO_35 VCCIO_36 VCCIO_37 VCCIO_38 VCCIO_39 VCCIO_40 VCCIO_41 VCCIO_42 VCCIO_43 VCCIO_44 VCCIO_45
VDDQ_01 VDDQ_02 VDDQ_04 VDDQ_05 VDDQ_06 VDDQ_07 VDDQ_08 VDDQ_09 VDDQ_10 VDDQ_11 VDDQ_12 VDDQ_13 VDDQ_14 VDDQ_15 VDDQ_16 VDDQ_17 VDDQ_18 VDDQ_19 VDDQ_20 VDDQ_21 VDDQ_22 VDDQ_23
VDDQ_03
+VCC_SA
VCCSA_01 VCCSA_02 VCCSA_03 VCCSA_04 VCCSA_05 VCCSA_06 VCCSA_07 VCCSA_08 VCCSA_09 VCCSA_10 VCCSA_11
+VCC1_8
VCCPLL_01 VCCPLL_02
POWER
8 OF 11
SKT_H2_CRB/ILM
REV = 1
+CPU_GFX
CPU1G
SKT_H2_CRB
BALLMAP_REV = 1.4
VCCAXG_01 VCCAXG_02 VCCAXG_03 VCCAXG_04 VCCAXG_05 VCCAXG_06 VCCAXG_07 VCCAXG_08 VCCAXG_09 VCCAXG_10 VCCAXG_11 VCCAXG_12 VCCAXG_13 VCCAXG_14 VCCAXG_15 VCCAXG_16 VCCAXG_17 VCCAXG_18 VCCAXG_19 VCCAXG_20 VCCAXG_21 VCCAXG_22 VCCAXG_23 VCCAXG_24 VCCAXG_25 VCCAXG_26 VCCAXG_27 VCCAXG_28 VCCAXG_29 VCCAXG_30 VCCAXG_31 VCCAXG_32 VCCAXG_33 VCCAXG_34 VCCAXG_35 VCCAXG_36 VCCAXG_37 VCCAXG_38 VCCAXG_39 VCCAXG_40 VCCAXG_41 VCCAXG_42 VCCAXG_43 VCCAXG_44
7 OF 11
SKT_H2_CRB/ILM
REV = 1
+VCCP
C143 C617 C610 C144 C629
C22u6.3X50805
+VCC_SA
+VCC1_8
C153 C155 C149
C10u6.3X50805 C22u6.3X50805
+CPU_VCCP-Decoupling
+VCCP
C131 C120 C631 C110 C100
C121 C618 C611 C132 C624
C623 C111 C619 C133 C145
C122 C622 C630 C612 C112 C607
C22u6.3X50805
X_C22u6.3X50805
PLACE ALL 08056 CAPS INSIDE CPU SOCKET CAVITY
+CPU_GFX Decoupling
+CPU_GFX
C601 C605 C606 C600
C104 C101 C604 C603 C102 C103
C22u6.3X50805
X_C22u6.3X50805
C47u6.3X50805
+1.5V_DDR3-Decoupling
+VCC_DDR
C141 C127 C113
CPU SOCKET CAVITY CAPS
+CPU_VTT Decoupling
+CPU_VTT
C130 C146 C640 C105
C602 C123 C114 C641 C642
C22u6.3X50805
X_C22u6.3X50805
4.7u10X50805
EC55
C330u2.5pSO
EC57
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CPU SOCKET CAVITY CAPS
MICRO-STAR INT'L CO.,LTD
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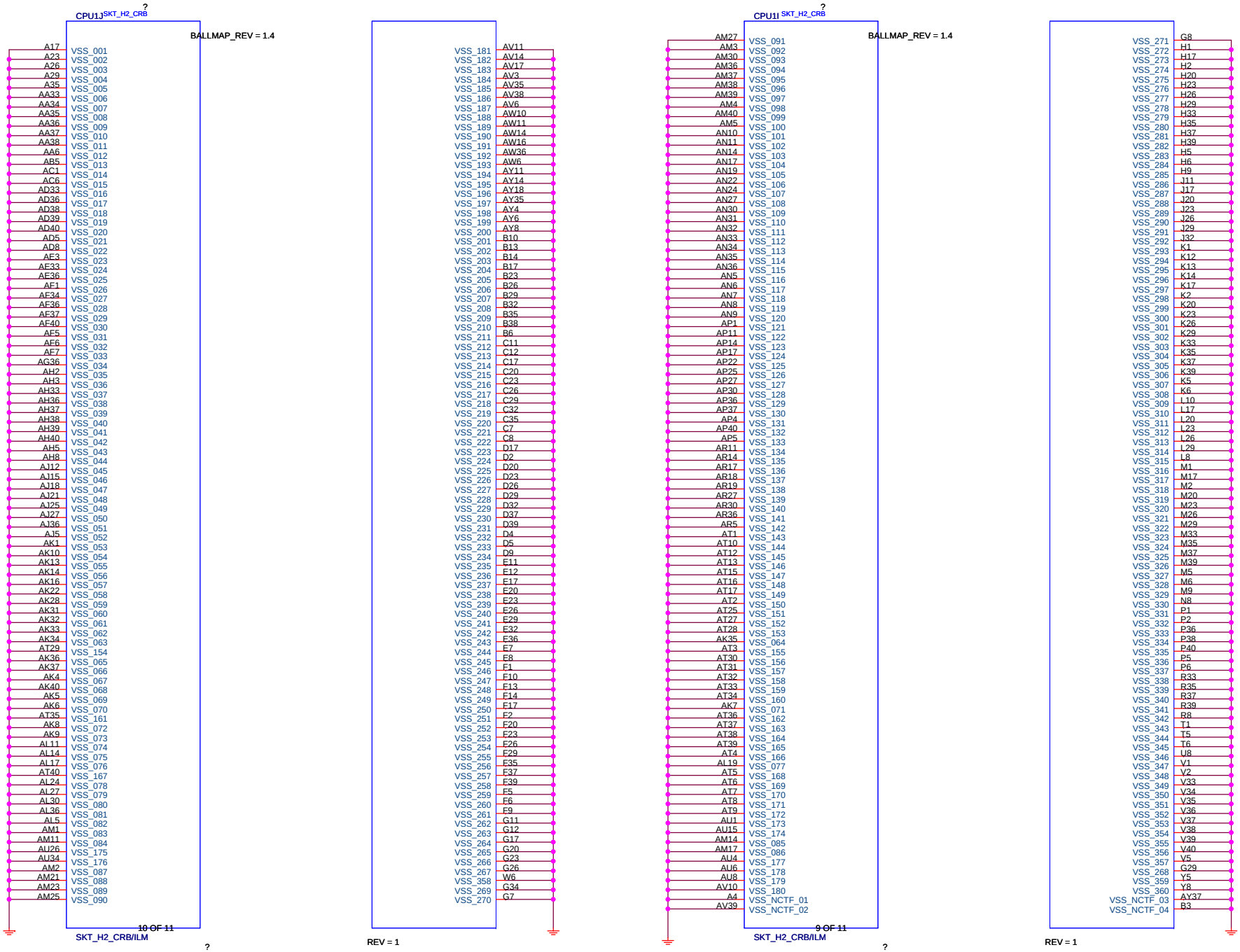

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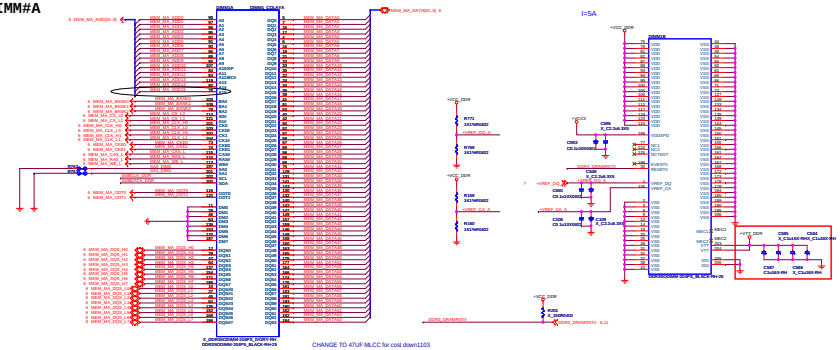
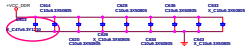
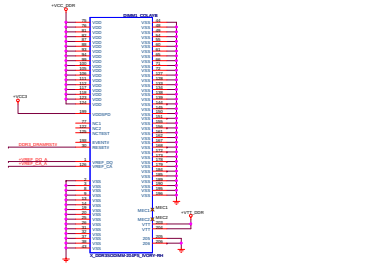
SODIMM#A

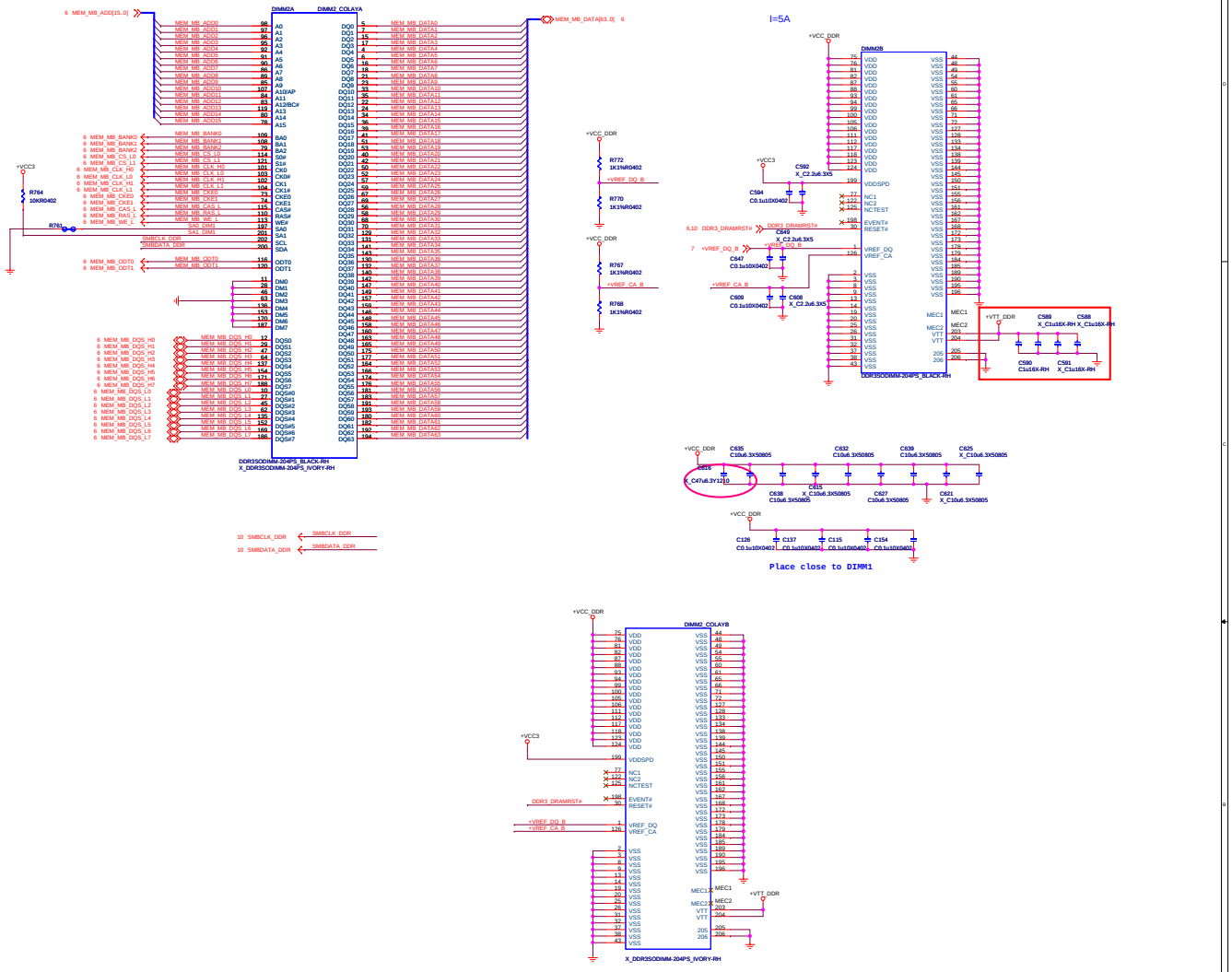






MICRO-STAR INT'L CO.,LTD	
MS-7765	
Size: Custom	Document Description: Channel A DDR III DIMM 1
Date: Monday, January 16, 2012	Sheet 10 of 48

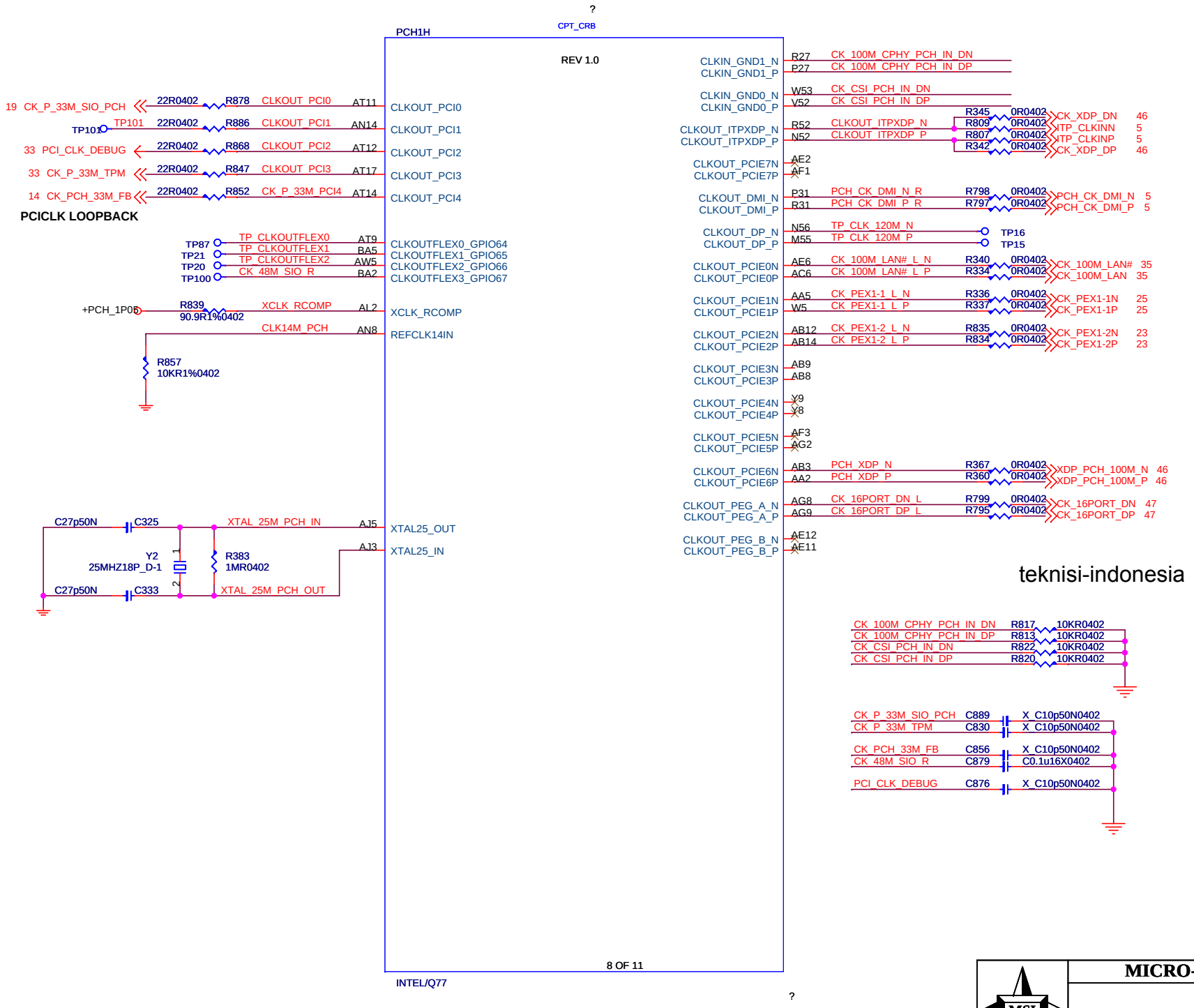
SODIMM#B



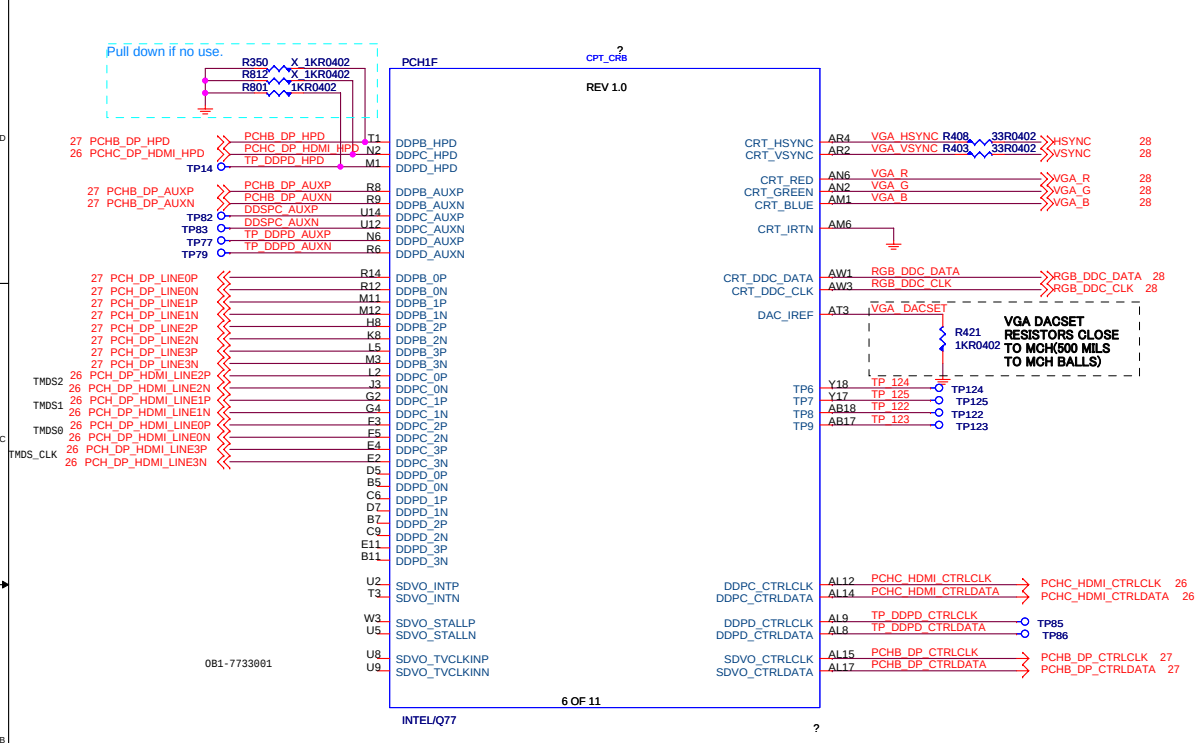
I=5A

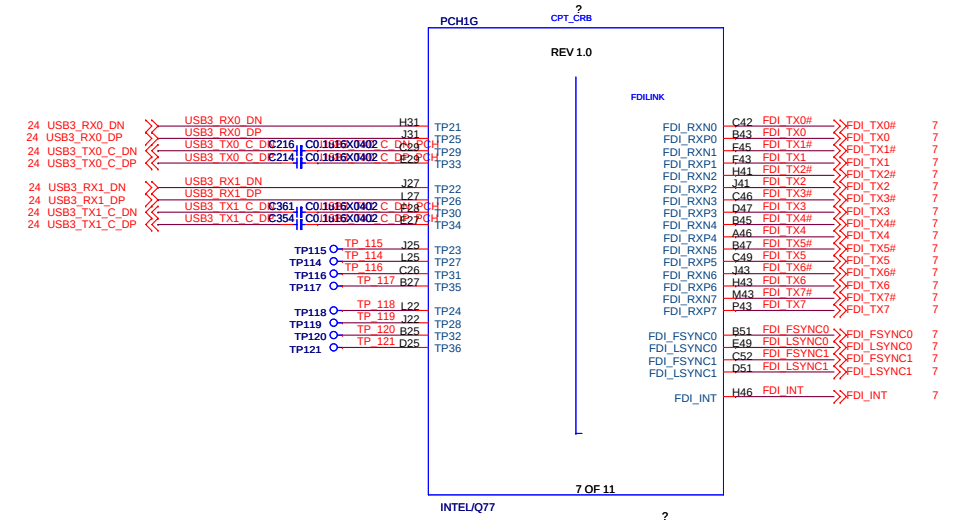
Place close to DIMM1

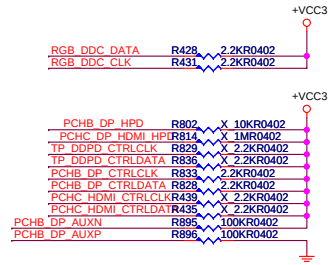
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: Channel B DDR III DIMM 2	Rev: C
Date: Monday, January 16, 2012	Sheet 11 of 63	



MICRO-STAR INT'L CO.,LTD	
MS-7765	
Size: Custom	Document Description: PCH-CLOCK
Rev: C	
Date: Wednesday, January 11, 2012	Sheet 12 of 63





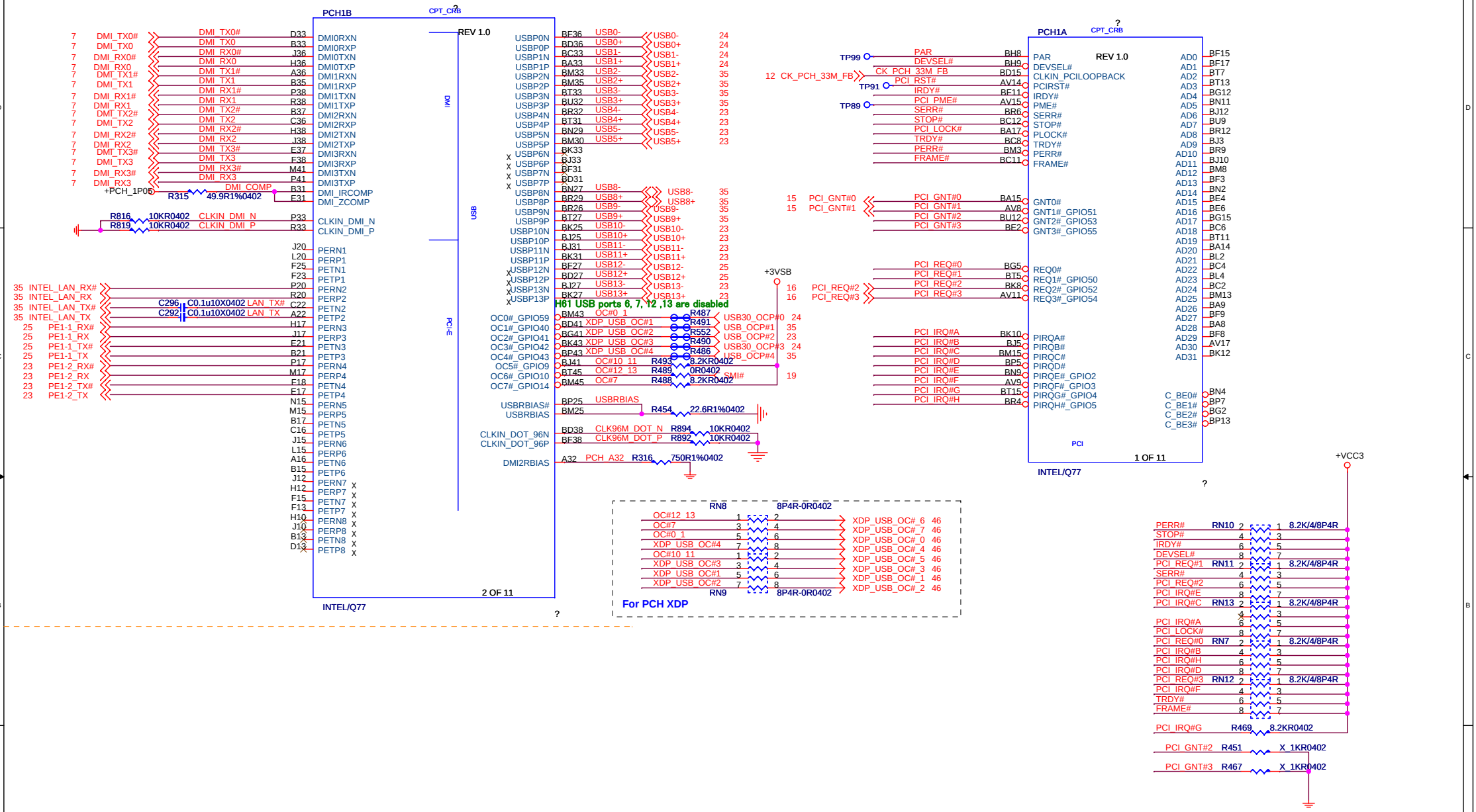


MICRO-STAR INT'L CO.,LTD

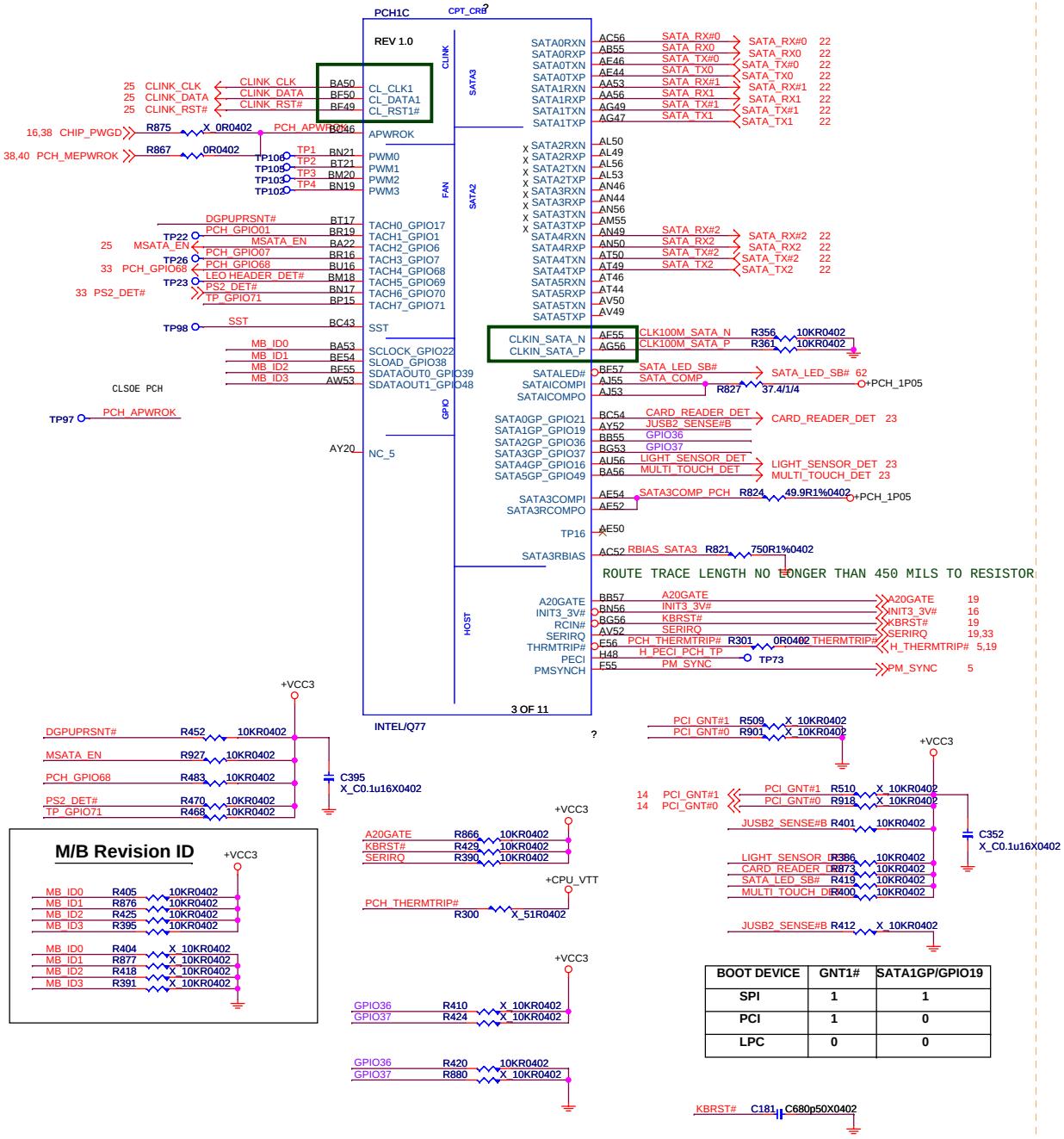
MS-7765

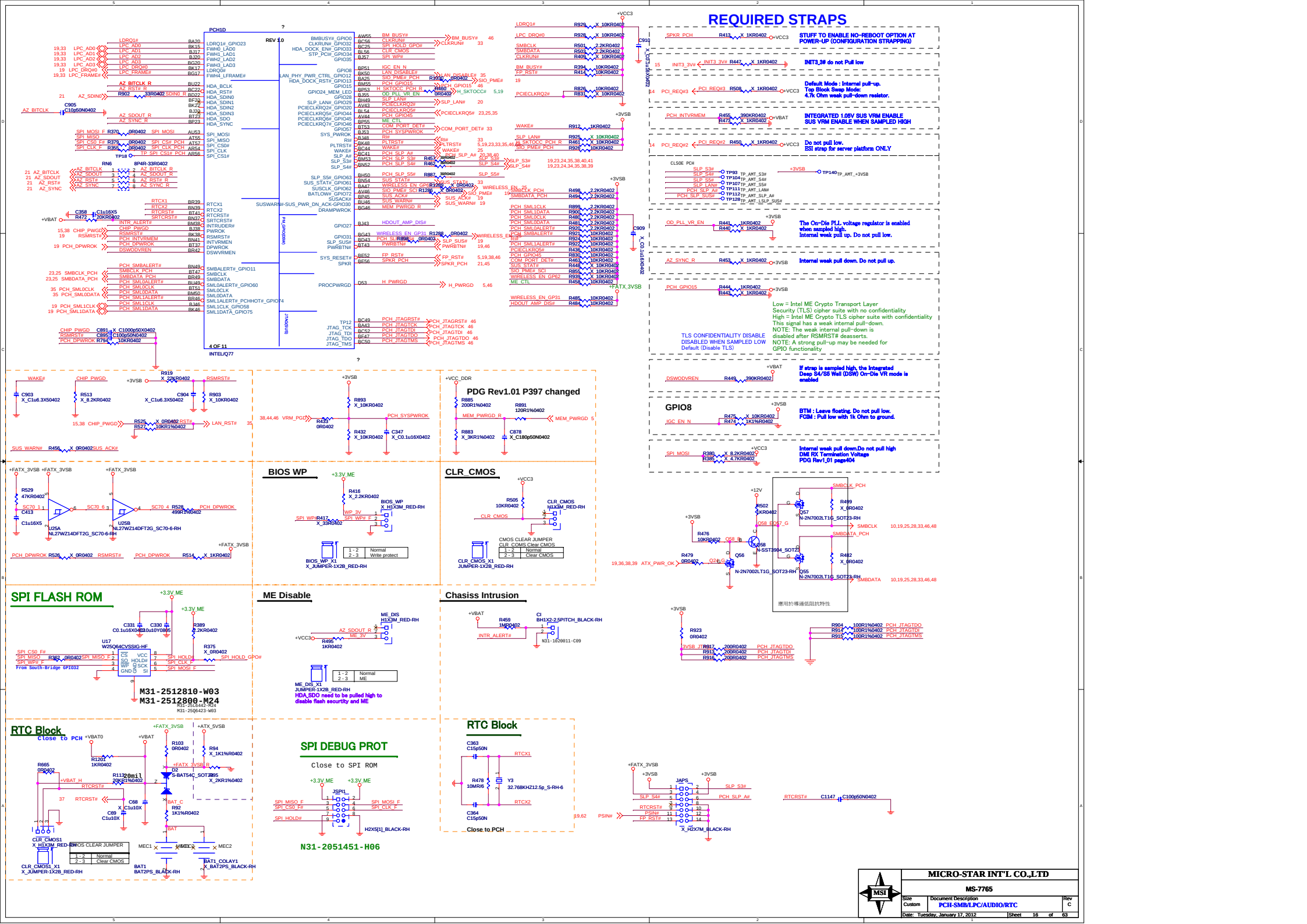
Size	Document Description	Rev
Custom	PCH-DISPLAY/ SPI ROM	C

Date: Monday, January 09, 2012 Sheet 13 of 63



MICRO-STAR INT'L CO.,LTD	
MS-7765	
Size: Custom	Document Description: PCH-PCI/E/DMI/USB
Rev: C	
Date: Friday, December 23, 2011	Sheet 14 of 63


PCH1C
CPT_CRB
REV 1.0
CLINK
SATA3
FAN
SATA2
GPIO
HOST
CL_CLK1
CL_DATA1
CL_RST1#
APWROK
PWM0
PWM1
PWM2
PWM3
TACH0_GPIO17
TACH1_GPIO1
TACH2_GPIO6
TACH3_GPIO7
TACH4_GPIO68
TACH5_GPIO69
TACH6_GPIO70
TACH7_GPIO71
SST
SCLOCK_GPIO22
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48
NC_5
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
CLKIN_SATA_N
CLKIN_SATA_P
SATALED#
SATAICOMPI
SATAICOMPO
SATA0GP_GPIO21
SATA1GP_GPIO19
SATA2GP_GPIO36
SATA3GP_GPIO37
SATA4GP_GPIO16
SATA5GP_GPIO49
SATA3COMPI
SATA3RCOMPO
TP16
SATA3RBIAS
A20GATE
INIT3_3V#
RCIN#
SERIRQ
THRMTRIP#
PECI
PMSYNCH
3 OF 11
INTEL/Q77
ROUTE TRACE LENGTH NO LONGER THAN 450 MILS TO RESISTOR
M/B Revision ID
+VCC3
+CPU_VTT
BOOT DEVICE
GNT1#
SATA1GP/GPIO19
SPI
PCI
LPC
SATA connector
SATA#0
SATA1 HDD
SATA#1
MSTAT SSD
SATA#2
SATA2 ODD
MICRO-STAR INT'L CO.,LTD
MS-7765
Size
Custom
Document Description
PCH-SATA/HOST/FAN/GPIO
Rev
C
Date: Friday, December 23, 2011
Sheet 15 of 63


REQUIRED STRAPS
STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING)
INIT3_3# do not Pull low
Default Mode : Internal pull-up.
Top Block Swap Mode:
4.7k Ohm weak pull-down resistor.
INTEGRATED 1.05V SUS VRM ENABLE
SUS VRM ENABLE WHEN SAMPLED HIGH
Do not pull low.
ESI strap for server platform ONLY
The On-Die PLL voltage regulator is enabled when sampled high.
Internal weak pull up. Do not pull low.
Internal weak pull down.Do not pull up.
Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High = Intel ME Crypto TLS cipher suite with confidentiality
This signal has a weak internal pull-down.
NOTE: The weak internal pull-down is disabled after RSMRST# deasserts.
NOTE: A strong pull-up may be needed for GPIO functionality
TLS CONFIDENTIALITY DISABLE
DISABLED WHEN SAMPLED LOW
Default (Disable TLS)
If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled
GPIO8
BTM : Leave floating. Do not pull low.
FOIM : Pull low with 1k Ohm to ground.
Internal weak pull down.Do not pull high
DMI RX Termination Voltage
PDG Rev1_01 page404
PDG Rev1.01 P397 changed
BIOS WP
CLR_CMOS
SPI FLASH ROM
ME Disable
Chasiss Intrusion
RTC Block
Close to PCH
SPI DEBUG PROT
Close to SPI ROM
N31-2051451-H06
M31-2512810-W03
M31-2512800-M24
HDA_SDO need to be pulled high to disable flash security and ME
PCH1D
INTEL/Q77
4 OF 11
REV 1.0
MICRO-STAR INT'L CO.,LTD
MS-7765
PCH-SMB/LPC/AUDIO/RTC
Rev C
Date: Tuesday, January 17, 2012
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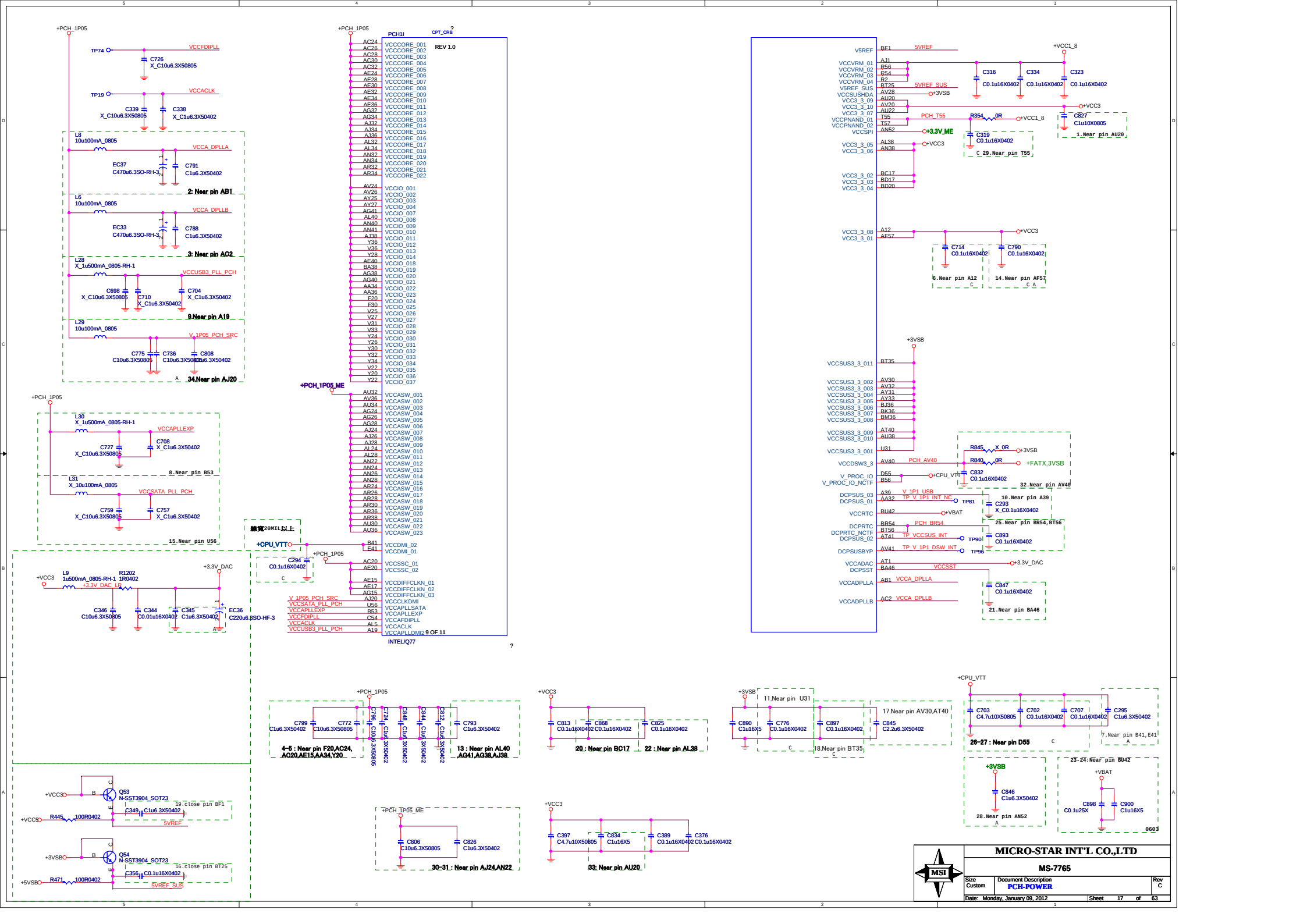
+PCH_1P05
TP74
VCCFDIPLL
C726
X_C10u6.3X50805
TP19
VCCACLK
C339
X_C10u6.3X50805
C338
X_C1u6.3X50402
L8
10u100mA_0805
VCCA_DPLLA
EC37
C470u6.3SO-RH-3
C791
C1u6.3X50402
2: Near pin AB1
L6
10u100mA_0805
VCCA_DPLLB
EC33
C470u6.3SO-RH-3
C788
C1u6.3X50402
3: Near pin AC2
L28
X_1u500mA_0805-RH-1
VCCUSB3_PLL_PCH
C698
X_C10u6.3X50805
C710
X_C1u6.3X50402
C704
X_C1u6.3X50402
9:Near pin A19
L29
10u100mA_0805
V_1P05_PCH_SRC
C775
C10u6.3X50805
C736
C10u6.3X50805
C808
C1u6.3X50402
34:Near pin AJ20
PCH1I
CPT_CR6
REV 1.0
VCCCORE_001
VCCCORE_002
VCCCORE_003
VCCCORE_004
VCCCORE_005
VCCCORE_006
VCCCORE_007
VCCCORE_008
VCCCORE_009
VCCCORE_010
VCCCORE_011
VCCCORE_012
VCCCORE_013
VCCCORE_014
VCCCORE_015
VCCCORE_016
VCCCORE_017
VCCCORE_018
VCCCORE_019
VCCCORE_020
VCCCORE_021
VCCCORE_022
VCCIO_001
VCCIO_002
VCCIO_003
VCCIO_004
VCCIO_007
VCCIO_008
VCCIO_009
VCCIO_010
VCCIO_011
VCCIO_012
VCCIO_013
VCCIO_014
VCCIO_018
VCCIO_019
VCCIO_020
VCCIO_021
VCCIO_022
VCCIO_023
VCCIO_024
VCCIO_025
VCCIO_026
VCCIO_027
VCCIO_028
VCCIO_029
VCCIO_030
VCCIO_031
VCCIO_032
VCCIO_033
VCCIO_034
VCCIO_035
VCCIO_036
VCCIO_037
+PCH_1P05_ME
VCCASW_001
VCCASW_002
VCCASW_003
VCCASW_004
VCCASW_005
VCCASW_006
VCCASW_007
VCCASW_008
VCCASW_009
VCCASW_010
VCCASW_011
VCCASW_012
VCCASW_013
VCCASW_014
VCCASW_015
VCCASW_016
VCCASW_017
VCCASW_018
VCCASW_019
VCCASW_020
VCCASW_021
VCCASW_022
VCCASW_023
VCCDMI_02
VCCDMI_01
VCCSSC_01
VCCSSC_02
VCCDIFFCLKN_01
VCCDIFFCLKN_02
VCCDIFFCLKN_03
VCCCLKDMI
VCCAPLLSATA
VCCAPLLEXP
VCCAFDIPLL
VCCACLK
VCCAPLLDMI2
9 OF 11
INTEL/Q77
V_1P05_PCH_SRC
VCCSATA_PLL_PCH
VCCAPLLEXP
VCCFDIPLL
VCCACLK
VCCUSB3_PLL_PCH
4~5 : Near pin F20,AC24, AC20,AE15,AA34,Y20
13 : Near pin AL40 AG41,AG38,AJ38
20 : Near pin BC17
22 : Near pin AL38
26~27 : Near pin D55
30~31 : Near pin AJ24,AN22
33: Near pin AU20
V5REF
VCCVRM_01
VCCVRM_02
VCCVRM_03
VCCVRM_04
VCCSUSHDA
VCC3_3_09
VCC3_3_10
VCC3_3_07
VCCPNAND_01
VCCPNAND_02
VCCSPI
VCC3_3_05
VCC3_3_06
VCC3_3_02
VCC3_3_03
VCC3_3_04
VCC3_3_08
VCC3_3_01
5VREF
5VREF_SUS
+3VSB
PCH_T55
+3.3V_ME
+VCC1_8
+VCC3
C316
C0.1u16X0402
C334
C0.1u16X0402
C323
C0.1u16X0402
R354
0R
C827
C1u10X0805
1.Near pin AU20
C319
C0.1u16X0402
C 29.Near pin T55
C714
C0.1u16X0402
C790
C0.1u16X0402
6.Near pin A12
14.Near pin AF57
VCCSUS3_3_011
VCCSUS3_3_002
VCCSUS3_3_003
VCCSUS3_3_004
VCCSUS3_3_005
VCCSUS3_3_006
VCCSUS3_3_007
VCCSUS3_3_008
VCCSUS3_3_009
VCCSUS3_3_010
VCCSUS3_3_001
VCCDSW3_3
V_PROC_IO
V_PROC_IO_NCTF
DCPSUS_03
DCPSUS_01
VCCRTC
DCPRTC
DCPRTC_NCTF
DCPSUS_02
DCPSUSBYP
VCCADAC
DCPSST
VCCADPLLA
VCCADPLLB
PCH_AV40
+CPU_VTT
V_1P1_USB
TP_V_1P1_INT_NC
TP81
+VBAT
PCH_BR54
TP_VCCSUS_INT
TP90
TP_V_1P1_DSW_INT
TP96
VCCSST
+3.3V_DAC
VCCA_DPLLA
VCCA_DPLLB
R845
X_0R
R840
0R
+FATX_3VSB
C832
C0.1u16X0402
32.Near pin AV40
10.Near pin A39
C293
X_C0.1u16X0402
25.Near pin BR54,BT56
C893
C0.1u16X0402
C847
C0.1u16X0402
21.Near pin BA46
L30
X_1u500mA_0805-RH-1
VCCAPLLEXP
C727
X_C10u6.3X50805
C708
X_C1u6.3X50402
8.Near pin B53
L31
X_10u100mA_0805
VCCSATA_PLL_PCH
C759
X_C10u6.3X50805
C757
X_C1u6.3X50402
15.Near pin U56
+3.3V_DAC
L9
1u500mA_0805-RH-1
R1202
1R0402
+3.3V_DAC_L2
C346
C10u6.3X50805
C344
C0.01u16X0402
C345
C1u6.3X50402
EC36
C220u6.3SO-HF-3
+CPU_VTT
C294
C0.1u16X0402
C799
C1u6.3X50402
C772
C10u6.3X50805
C795
C724
C1u6.3X50402
C848
C1u6.3X50402
C844
C1u6.3X50402
C812
C1u6.3X50402
C793
C1u6.3X50402
C813
C0.1u16X0402
C868
C0.1u16X0402
C825
C0.1u16X0402
C890
C1u16X5
C776
C0.1u16X0402
C897
C0.1u16X0402
C845
C2.2u6.3X50402
11.Near pin U31
17.Near pin AV30,AT40
18.Near pin BT35
C703
C4.7u10X50805
C702
C0.1u16X0402
C707
C0.1u16X0402
C295
C1u6.3X50402
7.Near pin B41,E41
C846
C1u6.3X50402
28.Near pin AN52
C898
C0.1u25X
C900
C1u16X5
0603
Q53
N-SST3904_SOT23
C349
C1u6.3X50402
19.close pin BF1
R445
100R0402
5VREF
Q54
N-SST3904_SOT23
C356
C0.1u16X0402
16.close pin BT25
R471
100R0402
5VREF_SUS
C806
C10u6.3X50805
C826
C1u6.3X50402
C397
C4.7u10X50805
C834
C1u16X5
C389
C0.1u16X0402
C376
C0.1u16X0402
MICRO-STAR INT'L CO.,LTD
MS-7765
Size
Custom
Document Description
PCH-POWER
Rev
C
Date: Monday, January 09, 2012
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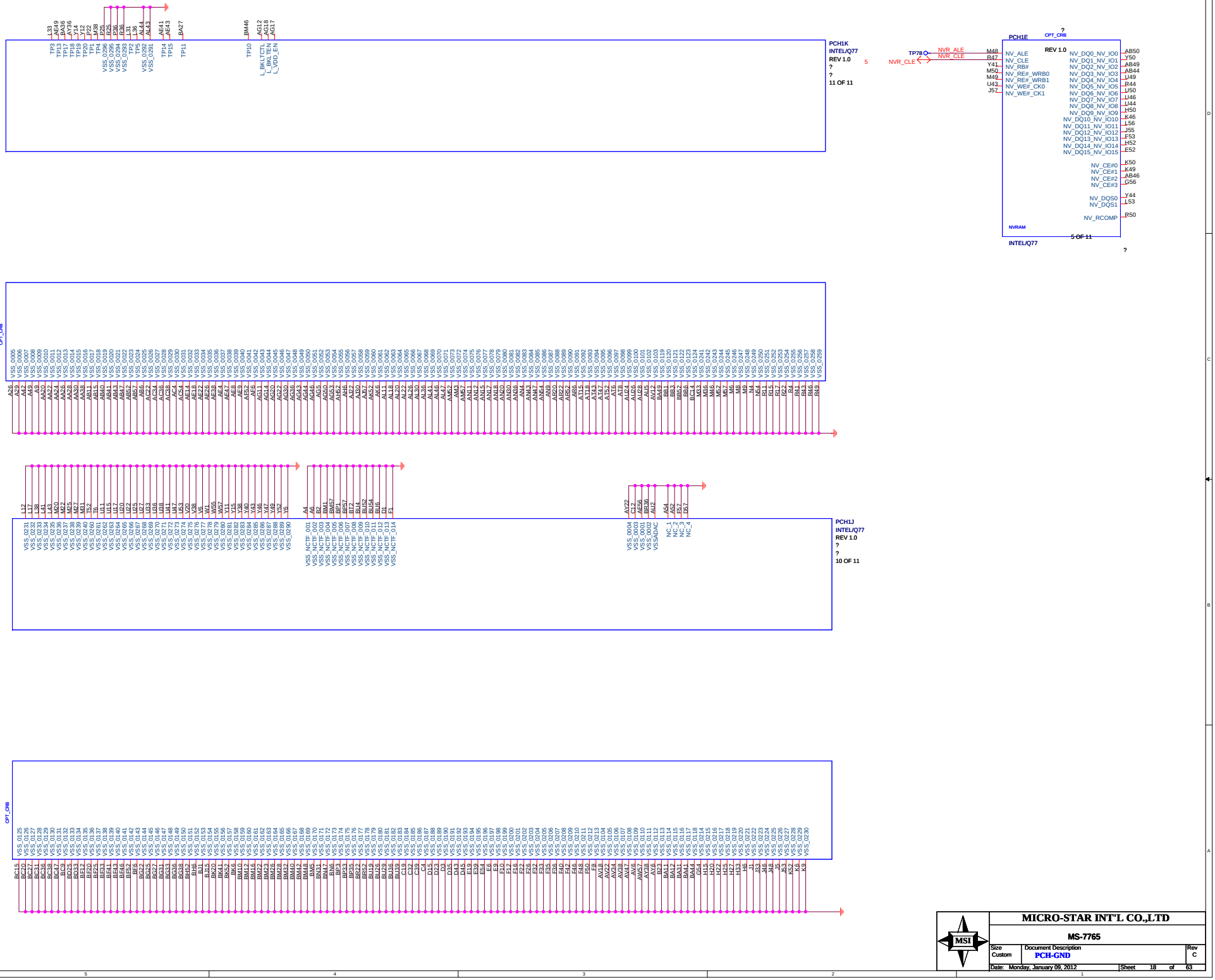
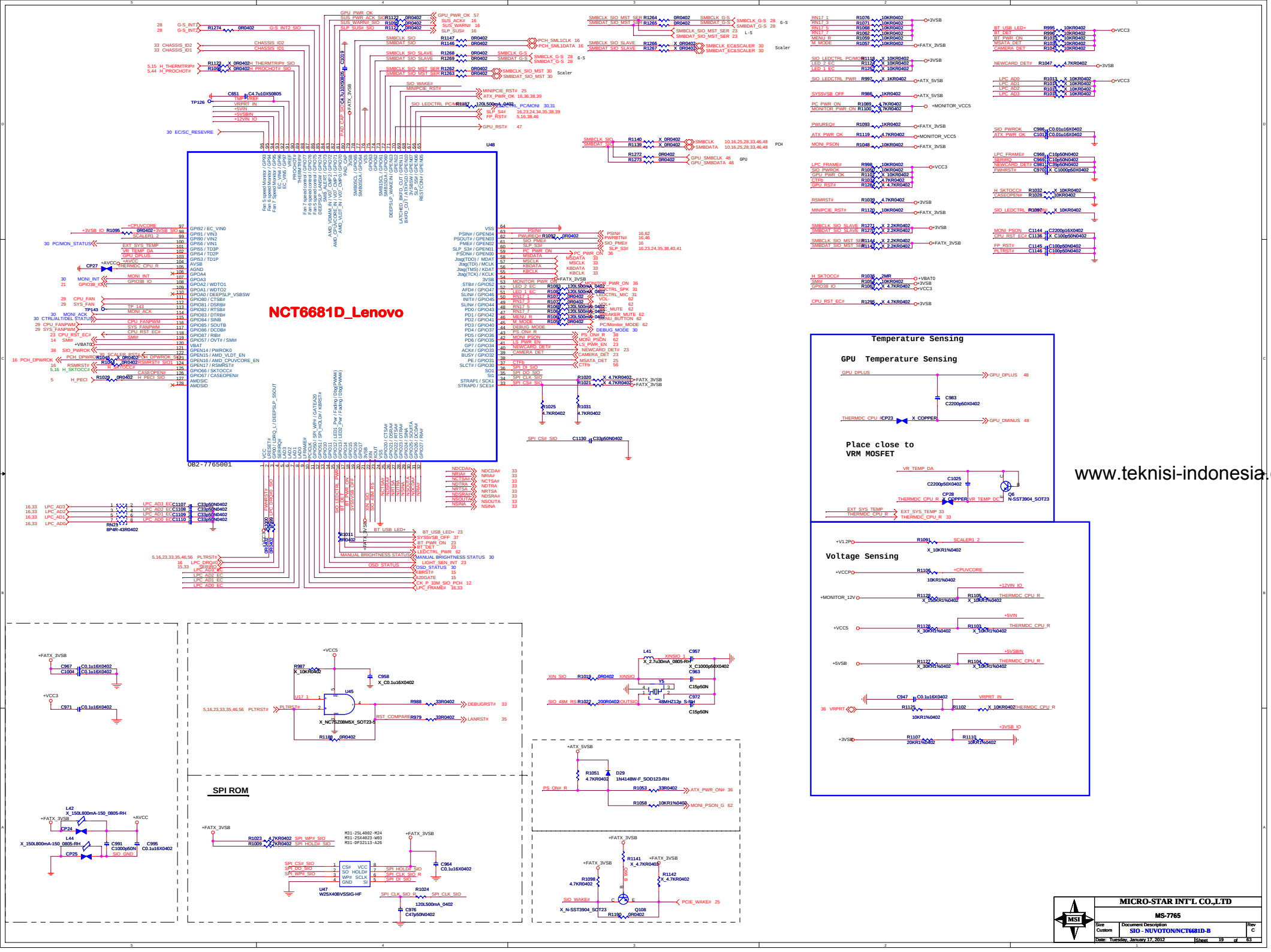


MICRO-STAR INT'L CO.,LTD			
MS-7765			
Size: Custom	Document Description: PCH-GND		Rev: C
Date: Monday, January 09, 2012		Sheet 18 of 63	



MICRO-STAR INT'L CO.,LTD		
MS-7765		
Size: Custom	Document Description: SIO - NUVOTON/NCT6681D-B	Rev: C
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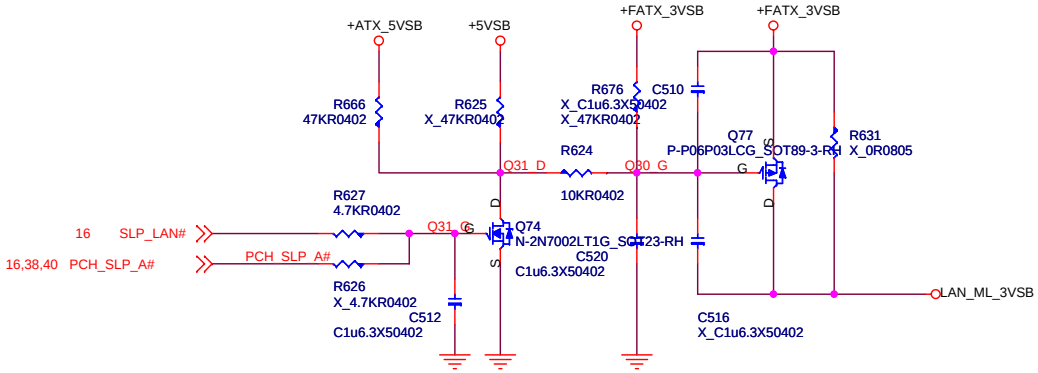
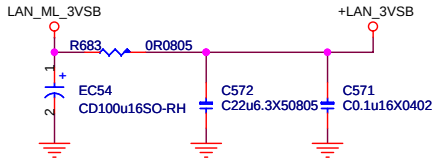
Gigabit LAN INTEL 82579

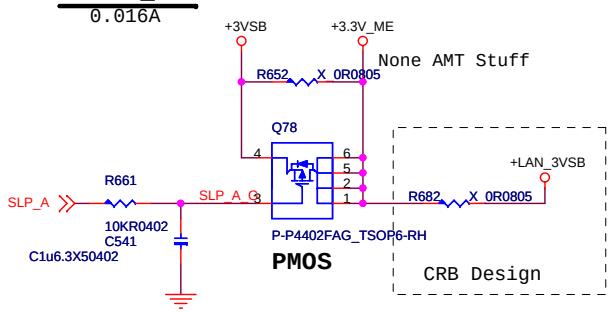
LAN Power

Note:These caps closed to PHY
82579 SPEC: 94mA
PDG page 323 : 0.218A

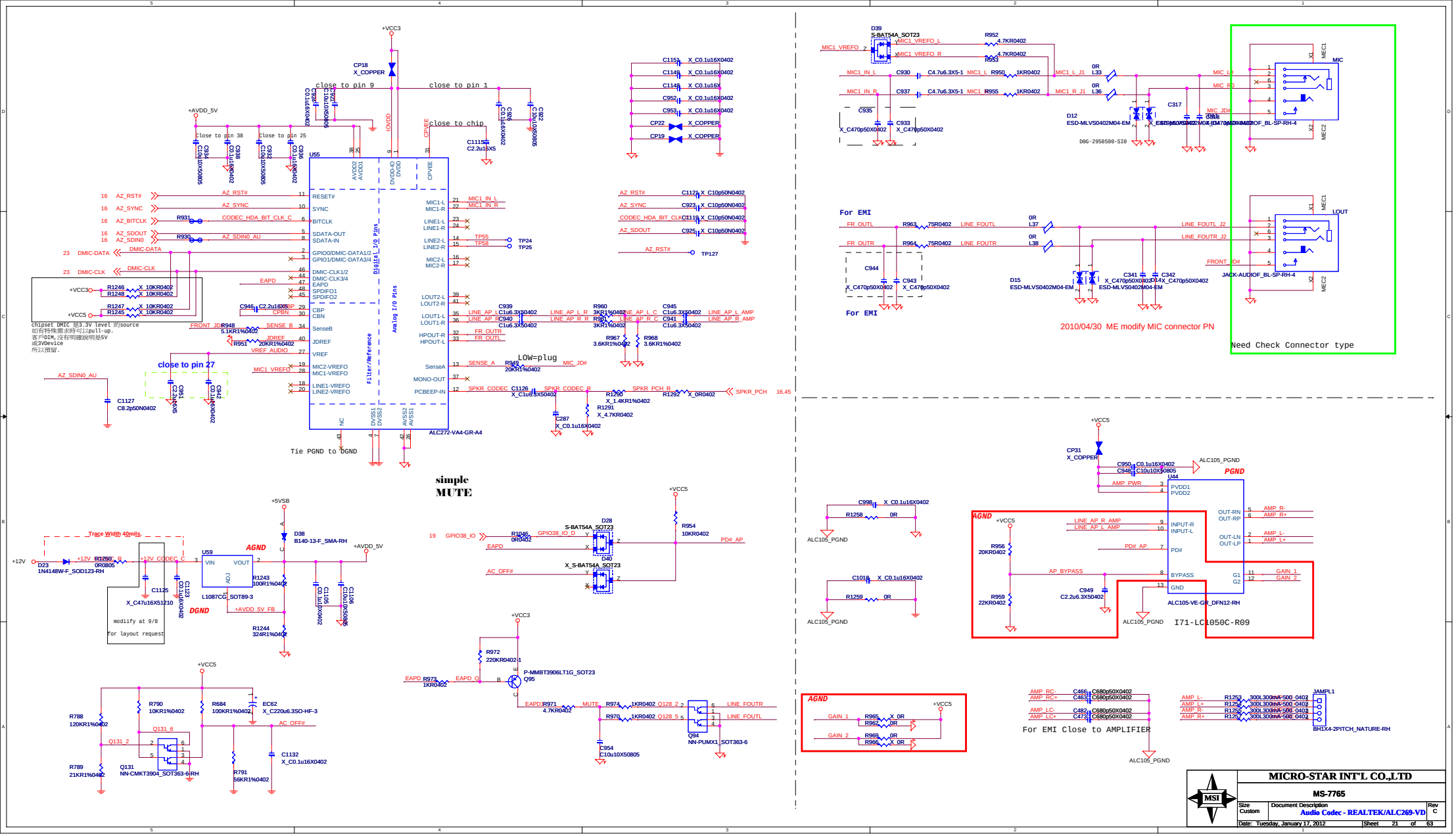




+3.3V_ME
0.016A



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: Gigabit LAN - INTEL/WG82579	Rev: C
Date: Wednesday, November 23, 2011	Sheet 20 of 63	


ALC272-VA4-GR-A4
simple MUTE
For EMI
2010/04/30 ME modify MIC connector PN
Need Check Connector type
I71-LC1050C-R09
MICRO-STAR INT'L CO.,LTD
MS-7765
Audio Codec - REALTEK/ALC269-VD
Date: Tuesday, January 17, 2012
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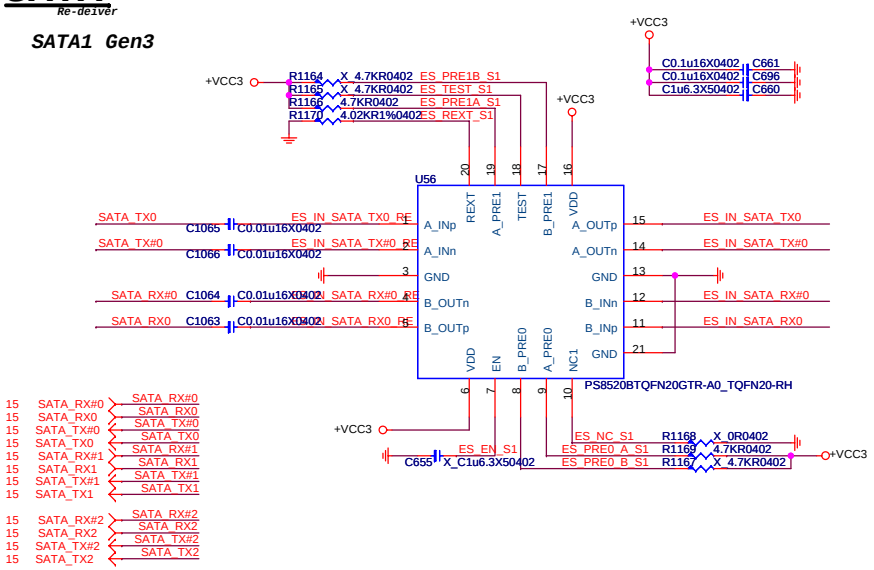
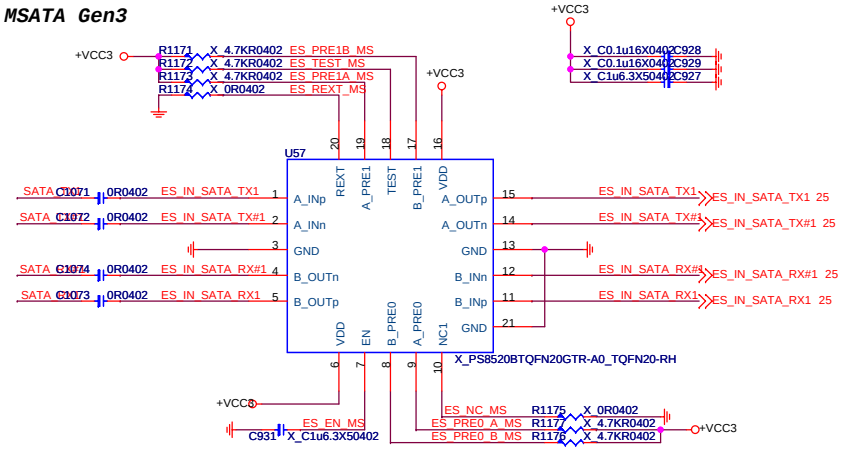
SATA

Re-deiver

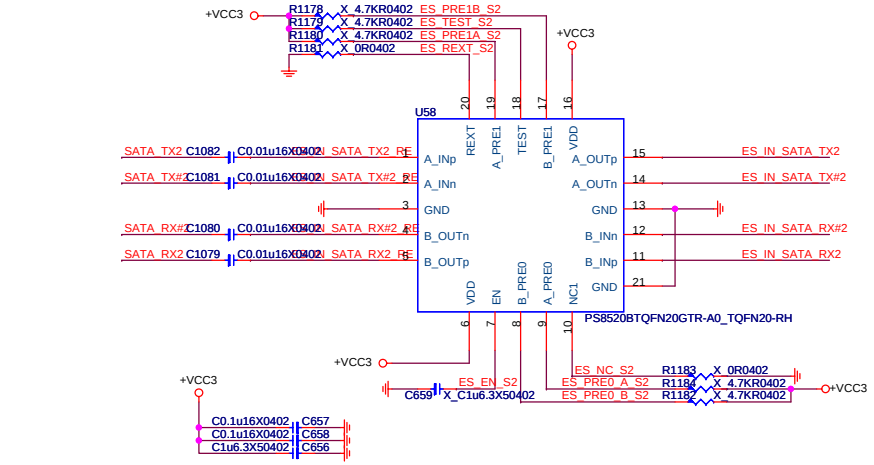
SATA1 Gen3

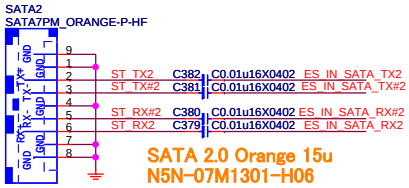


MSATA Gen3

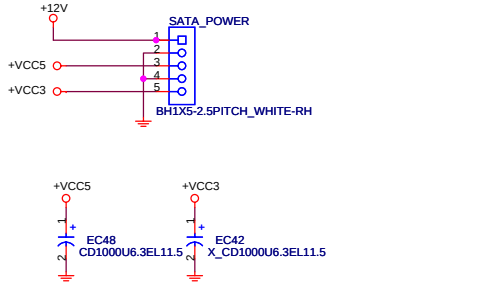


SATA2 Gen2



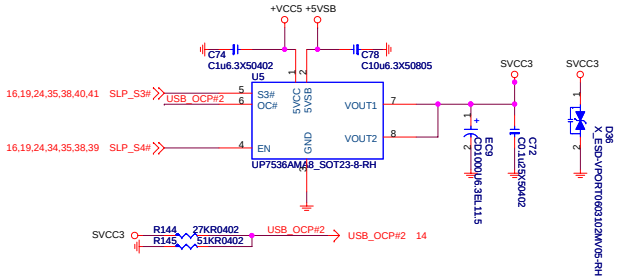


Power Connector



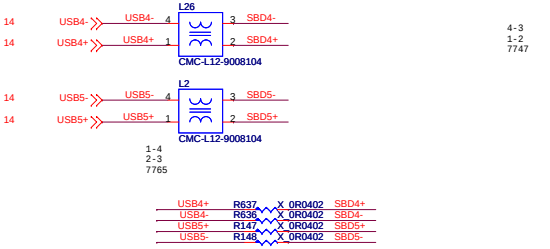
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: Power Delivery	Rev: C
Date: Wednesday, January 11, 2012	Sheet 22 of 63	

POWER CIRCUIT FOR USB PORT 4, 5

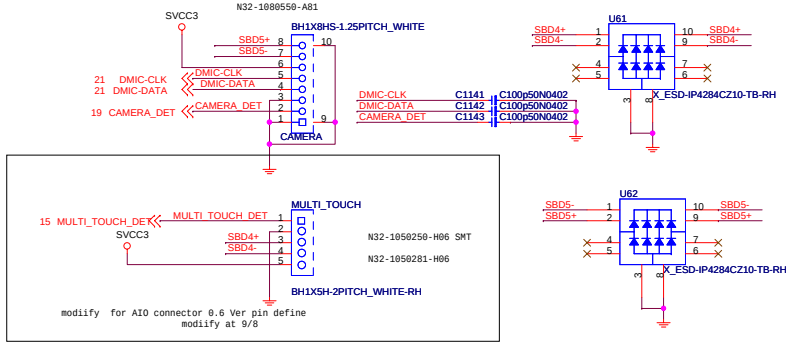


USB CONNECTOR FOR USB PORT 4,5

NEAR USB CONNECTOR

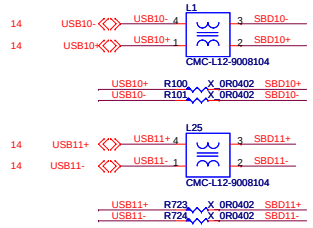


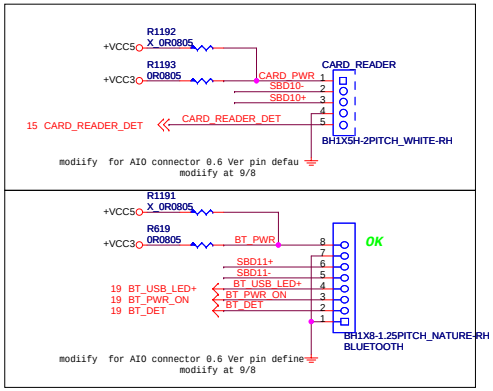
4-3
1-2
7747



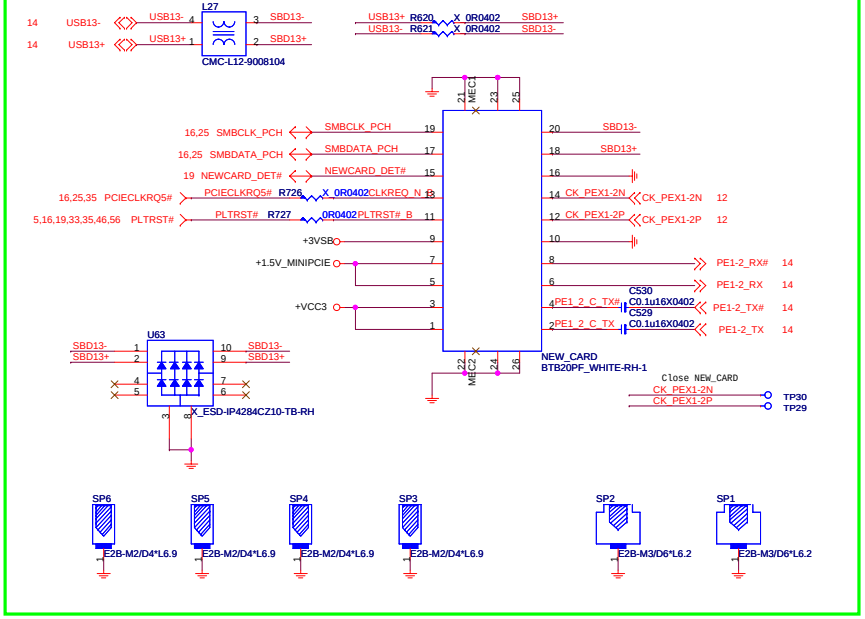
USB CONNECTOR FOR USB PORT 10,11

NEAR USB CONNECTOR

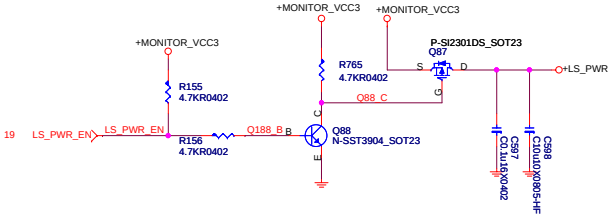


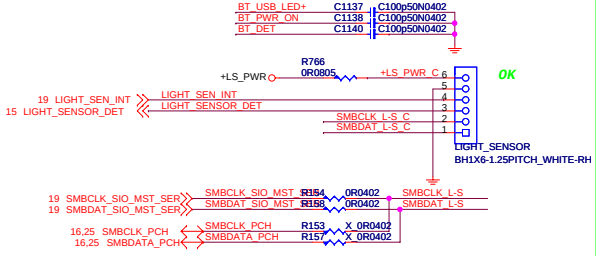


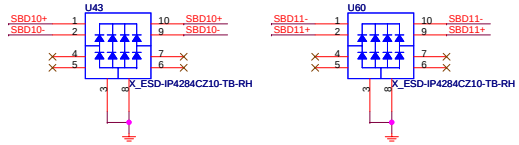
New card header

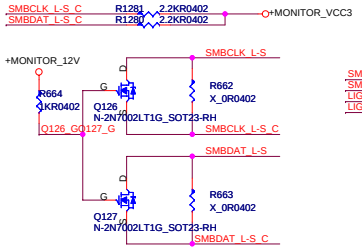


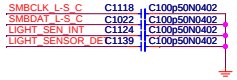
POWER CIRCUIT FOR Light sensor











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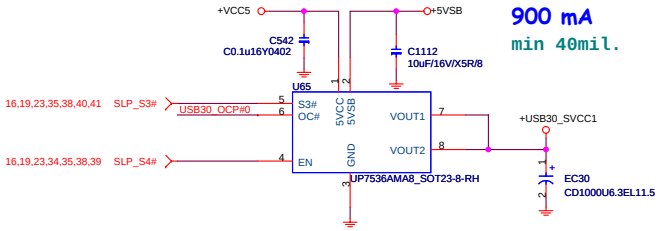
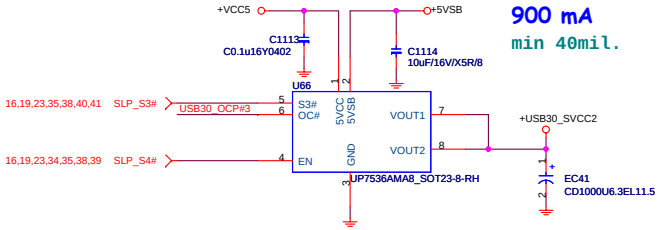
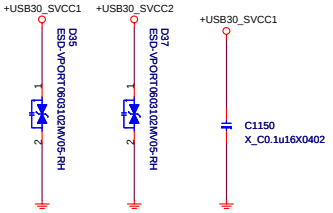
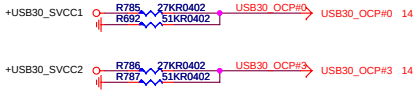
POWER CIRCUIT FOR USB PORT 0, 1

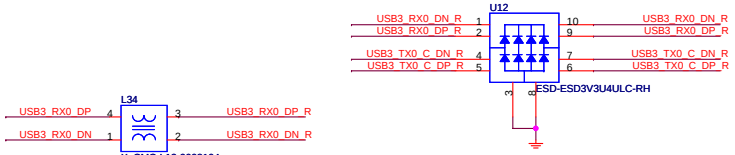




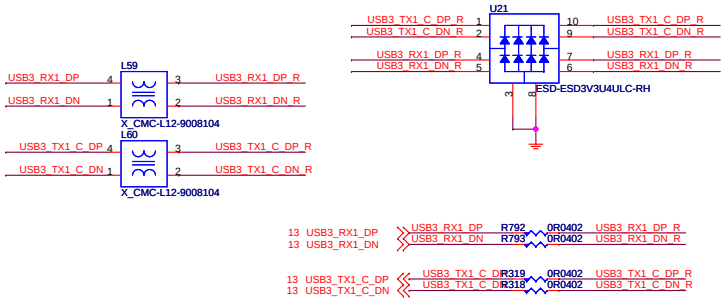


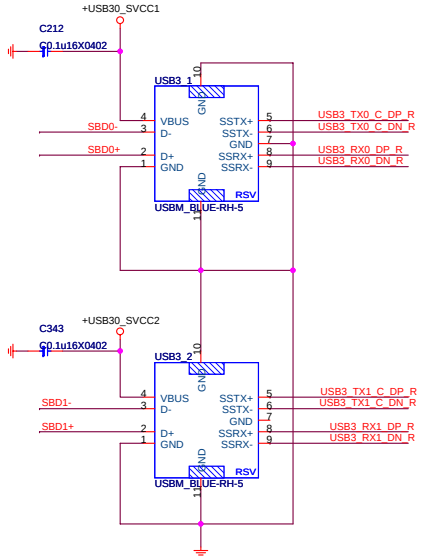


RIGHT SIDE USB CONNECTOR FOR USB3.0 PORT 0,1

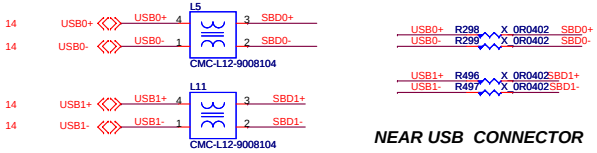


default is 0 ohm
5KV is 22 ohm
7KV is 33 ohm

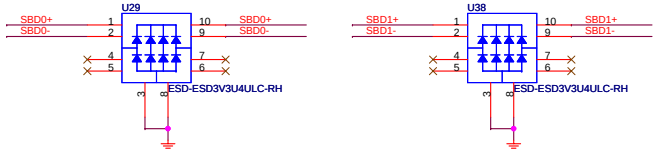




RIGHT SIDE USB CONNECTOR FOR USB2.0 PORT 0,1



NEAR USB CONNECTOR



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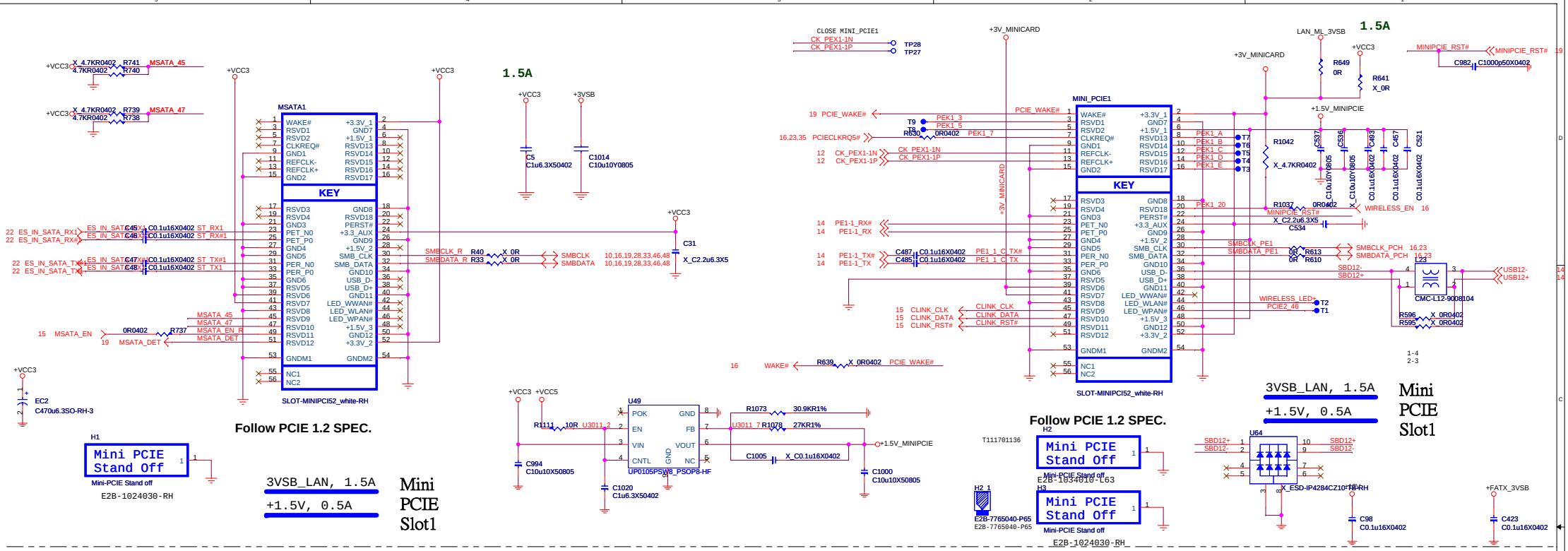

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HDMI

Stuff for PCH DVI To SCALER

13 PCH_DP_HDMI_LINE0N — C974 X_C0.1u16X0402 — HDMI_TXD0-
13 PCH_DP_HDMI_LINE0P — C975 X_C0.1u16X0402 — HDMI_TXD0+

48 MXM_DP_HDMI_LINE0N — C497 C0.1u16X0402
48 MXM_DP_HDMI_LINE0P — C499 C0.1u16X0402

Stuff for GPU DVI To SCALER

13 PCH_DP_HDMI_LINE1N — C978 X_C0.1u16X0402 — HDMI_TXD1-
13 PCH_DP_HDMI_LINE1P — C979 X_C0.1u16X0402 — HDMI_TXD1+

48 MXM_DP_HDMI_LINE1N — C501 C0.1u16X0402
48 MXM_DP_HDMI_LINE1P — C503 C0.1u16X0402

13 PCH_DP_HDMI_LINE2N — C980 X_C0.1u16X0402 — HDMI_TXD2-
13 PCH_DP_HDMI_LINE2P — C984 X_C0.1u16X0402 — HDMI_TXD2+

48 MXM_DP_HDMI_LINE2N — C505 C0.1u16X0402
48 MXM_DP_HDMI_LINE2P — C511 C0.1u16X0402

13 PCH_DP_HDMI_LINE3N — C965 X_C0.1u16X0402 — HDMI_TXC-
13 PCH_DP_HDMI_LINE3P — C973 X_C0.1u16X0402 — HDMI_TXC+

48 MXM_DP_HDMI_LINE3N — C492 C0.1u16X0402
48 MXM_DP_HDMI_LINE3P — C495 C0.1u16X0402

13 PCHC_HDMI_CTRLCLK — R1001 X_0R0402 — HDMI_DDC_CLK_RR
13 PCHC_HDMI_CTRLDATA — R1002 X_0R0402 — HDMI_DDC_DATA_RR

48 MXM3_HDMI_CTRLCLK — R1005 0R0402
48 MXM3_HDMI_CTRLDATA — R1006 0R0402

13 PCHC_DP_HDMI_HPD — R991 X_0R0402 — HDMI_HPD
48 MXM3_DP_HDMI_HPD — R992 0R0402

BOM OPTION NOTE
Stuff for PCH DVI To SCALER
C974,C975,C978,C979,C980,C984
C965,C973,R1001,R1002

Stuff for GPU DVI To SCALER
C497,C499,C501,C503,C505,C511
C492,C495,R991,R992

Close to scaler

HDMI_TXC- 1 2
HDMI_TXC+ 3 4
HDMI_TXD0- 5 6 8P4R-680R RN14
HDMI_TXD0+ 7 8
HDMI_TXD1- 1 2
HDMI_TXD1+ 3 4
HDMI_TXD2- 5 6 8P4R-680R RN15
HDMI_TXD2+ 7 8

Q122_D

+VCC3 — R616 0R0402 — Q122_G
C494 X_C0.1u16X0402
Q122 N-2N7002LT1G_SOT23-RH

HDMI To SCALER

HDMI_TXD0+ — HDMI_TXD0+ 30
HDMI_TXD0- — HDMI_TXD0- 30
HDMI_TXD1+ — HDMI_TXD1+ 30
HDMI_TXD1- — HDMI_TXD1- 30
HDMI_TXD2+ — HDMI_TXD2+ 30
HDMI_TXD2- — HDMI_TXD2- 30
HDMI_TXC+ — HDMI_TXC+ 30
HDMI_TXC- — HDMI_TXC- 30

+VCC3 — R1017 2.2KR0402 — Q100 X_N-2N7002LT1G_SOT23-RH — R1026 X_2.2KR0402 — +VCC5
HDMI_DDC_CLK_RR (Follow DP701 PDG) — HDMI_DDC_CLK_R — HDMI_DDC_CLK_R 30
+VCC3 — R1156 0R0402

+VCC3 — R1018 2.2KR0402 — Q101 X_N-2N7002LT1G_SOT23-RH — R1027 X_2.2KR0402 — +VCC5
HDMI_DDC_DATA_RR (Follow DP701 PDG) — HDMI_DDC_DATA_R — HDMI_DDC_DATA_R 30
R1157 0R0402

+VCC3 — R993 X_4.7KR0402 — R1279 0R0402 — Q96 X_N-2N7002LT1G_SOT23-RH — HDMI_HOT_DET 30
HDMI_HPD (Follow DP701 PDG)
+12V — R990 X_100KR0402

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DP_OUTPUT

Close to rear board

DP_OUTPUT
PCH To FINGER

13 PCH_DP_LINE0P — R1117 X_0R0402 — OUT_DP_LINE0P 35
13 PCH_DP_LINE0N — R1116 X_0R0402 — OUT_DP_LINE0N 35
13 PCH_DP_LINE1P — R1115 X_0R0402 — OUT_DP_LINE1P 35
13 PCH_DP_LINE1N — R1114 X_0R0402 — OUT_DP_LINE1N 35

BOM OPTION NOTE
Stuff for PCH DVI To SCALER
R1114~R1117
R1130~R1133
C1027,C1028,C1022,C1023

13 PCH_DP_LINE2P — R1132 X_0R0402 — OUT_DP_LINE2P 35
13 PCH_DP_LINE2N — R1133 X_0R0402 — OUT_DP_LINE2N 35
13 PCH_DP_LINE3P — R1130 X_0R0402 — OUT_DP_LINE3P 35
13 PCH_DP_LINE3N — R1131 X_0R0402 — OUT_DP_LINE3N 35

13 PCHB_DP_AUXP — C1027 X_C0.1u16X0402 — OUT_DP_AUXP 35
13 PCHB_DP_AUXN — C1028 X_C0.1u16X0402 — OUT_DP_AUXN 35

DP_OUTPUT
MXM To FINGER

48 MXM5_DP_AUXP — C552 C0.1u16X0402
48 MXM5_DP_AUXN — C551 C0.1u16X0402

13 PCHB_DP_CTRLCLK — R783 X_0R0402 — OUT_DP_DDC_CLK 35
13 PCHB_DP_CTRLDATA — R784 X_0R0402 — OUT_DP_DDC_DAT 35

48 MXM5_DP_AUXP — R689 0R0402
48 MXM5_DP_AUXN — R690 0R0402

48 MXM_DP_LINE0P — MXM_DP_LINE0P R695 0R0402 — OUT_DP_LINE0P 35
48 MXM_DP_LINE0N — MXM_DP_LINE0N R696 0R0402 — OUT_DP_LINE0N 35
48 MXM_DP_LINE1P — MXM_DP_LINE1P R698 0R0402 — OUT_DP_LINE1P 35
48 MXM_DP_LINE1N — MXM_DP_LINE1N R697 0R0402 — OUT_DP_LINE1N 35

48 MXM_DP_LINE2P — MXM_DP_LINE2P R706 0R0402 — OUT_DP_LINE2P 35
48 MXM_DP_LINE2N — MXM_DP_LINE2N R705 0R0402 — OUT_DP_LINE2N 35
48 MXM_DP_LINE3P — MXM_DP_LINE3P R708 0R0402 — OUT_DP_LINE3P 35
48 MXM_DP_LINE3N — MXM_DP_LINE3N R707 0R0402 — OUT_DP_LINE3N 35

BOM OPTION NOTE
Stuff for GPU Display port To output
R695~R697
R705~R708
C551,C552,R689,R690

13 PCHB_DP_HPD — R717 X_0R0402 — DP_OUT_HPD 35
48 MXM5_DP_HPD — R716 0R0402

+12V — R713 4.7KR0402 — +DP_PWR_EN
+VCC3
Q80
N-APM2308AC-TRL_SOT23-3-RH
+DP_PWR_OUT

DP_INPUT Driver

Close to rear board

+DP_PWR_FS
C549 C0.1u16X0402 — C535 C0.1u16X0402

30 SDP_HPD — R582 1MR0402 — SDP_HPD

Rear Board to re-driver

35 IN_DP_LINE0P — C556 C0.1u16X0402 — IN_DP_LINE0P_RE
35 IN_DP_LINE0N — C566 C0.1u16X0402 — IN_DP_LINE0N_RE
35 IN_DP_LINE1P — C559 C0.1u16X0402 — IN_DP_LINE1P_RE
35 IN_DP_LINE1N — C560 C0.1u16X0402 — IN_DP_LINE1N_RE
35 IN_DP_LINE2P — C561 C0.1u16X0402 — IN_DP_LINE2P_RE
35 IN_DP_LINE2N — C562 C0.1u16X0402 — IN_DP_LINE2N_RE
+DP_PWR_FS
35 IN_DP_LINE3P — C563 C0.1u16X0402 — DP_LINE3P_RE
35 IN_DP_LINE3N — C564 C0.1u16X0402 — DP_LINE3N_RE
35 IN_DP_HOT_DET — R721 1KR0402 — IN_DP_HOT_DET_RE

U33
PS8311
PS8311QFN48GTR-A0-RH

IN_DP_DDPB_AUXP_RE — R236 0R0402 — IN_DP_DDPB_AUXP 35
IN_DP_DDPB_AUXN_RE — R245 0R0402 — IN_DP_DDPB_AUXN 35

SIN_DP_AUXP
SIN_DP_AUXN
AC_AUXP — C997 C0.1u16X0402
AC_AUXN — C1007 C0.1u16X0402
CEXT
REXT
PC0 — R635 4.99KR1%0402 — C528 C2.2u6.3X50402

+MONITOR_12V — R628 4.7KR0402 — +DP_PWR_FS_EN
+MONITOR_VCC3
Q76
N-APM2308AC-TRL_SOT23-3-RH
+DP_PWR_FS

R648 4.7KR0402

re-driver to scaler

30 SIN_DP_LINE3N — C518 C0.1u16X0402 — SIN_DP_LINE3N_RE
30 SIN_DP_LINE3P — C515 C0.1u16X0402 — SIN_DP_LINE3P_RE
30 SIN_DP_LINE2N — C514 C0.1u16X0402 — SIN_DP_LINE2N_RE
30 SIN_DP_LINE2P — C506 C0.1u16X0402 — SIN_DP_LINE2P_RE
30 SIN_DP_LINE1N — C502 C0.1u16X0402 — SIN_DP_LINE1N_RE
30 SIN_DP_LINE1P — C500 C0.1u16X0402 — SIN_DP_LINE1P_RE
30 SIN_DP_LINE0N — C498 C0.1u16X0402 — SIN_DP_LINE0N_RE
30 SIN_DP_LINE0P — C496 C0.1u16X0402 — SIN_DP_LINE0P_RE

CLOSE to scaler

IN_DP_HOT_DET — IN_DP_HOT_DET 35
+V33P — R722 X_4.7KR0402

+DP_PWR_FS
C1026 C0.1u16X0402 — C1015 X_C0.1u16X0402

NC
R643 X_1MR0402 — R633 1KR0402 — AUXDCP — AUXDCP 30
SIN_DP_AUXP — C523 C0.1u16X0402 — AUXP — AUXP 30
+MONITOR_VCC3
R642 1MR0402
NC
R645 X_1MR0402 — R634 1KR0402 — AUXDCN — AUXDCN 30
SIN_DP_AUXN — C524 C0.1u16X0402 — AUXN — AUXN 30
R644 1MR0402

PEQ — R1129 4.7KR0402 — +DP_PWR_FS
PIO — R701 X_4.7KR0402 / R712 4.7KR0402 — +DP_PWR_FS
CFG1 — R678 4.7KR0402 — +DP_PWR_FS
CFG0 — R671 4.7KR0402 — +DP_PWR_FS
PC0 — R650 4.7KR0402 — +DP_PWR_FS

3 Level Input:
L: LOW (internal pull down ~150Kohm)
H: HIGH
M: VDD/2, connect both pull-up and pull-down resistors

PEQ: Programmable Equalization setting
=>L: Low RX EQ setting (LEQ), default
M: High RX EQ setting(HEQ)

PIO = L: IN_HPDX = OUT_HPD,3.3V output
= H: IN_HPDX = OUT_HPD#, inverted HPD, 0.9V output
=> = M: IN_HPDX = OUT_HPD#, inverted HPD, 3.3V output

CFG1: AUX interception configuration
=> L: Normal Aux interception
H: AUX interception with fixed output swing of 600mV and no pre-emphasis

CFG0:AUX channel operation configuration
=> L: AUX CH is off when chip is in automatic power down
H: AUX CH is operational when chip is in automatic power down

PC0: Automatic Equalization configue
=>L: Automatic equalization is enabled
H: Automatic equalization is disabled

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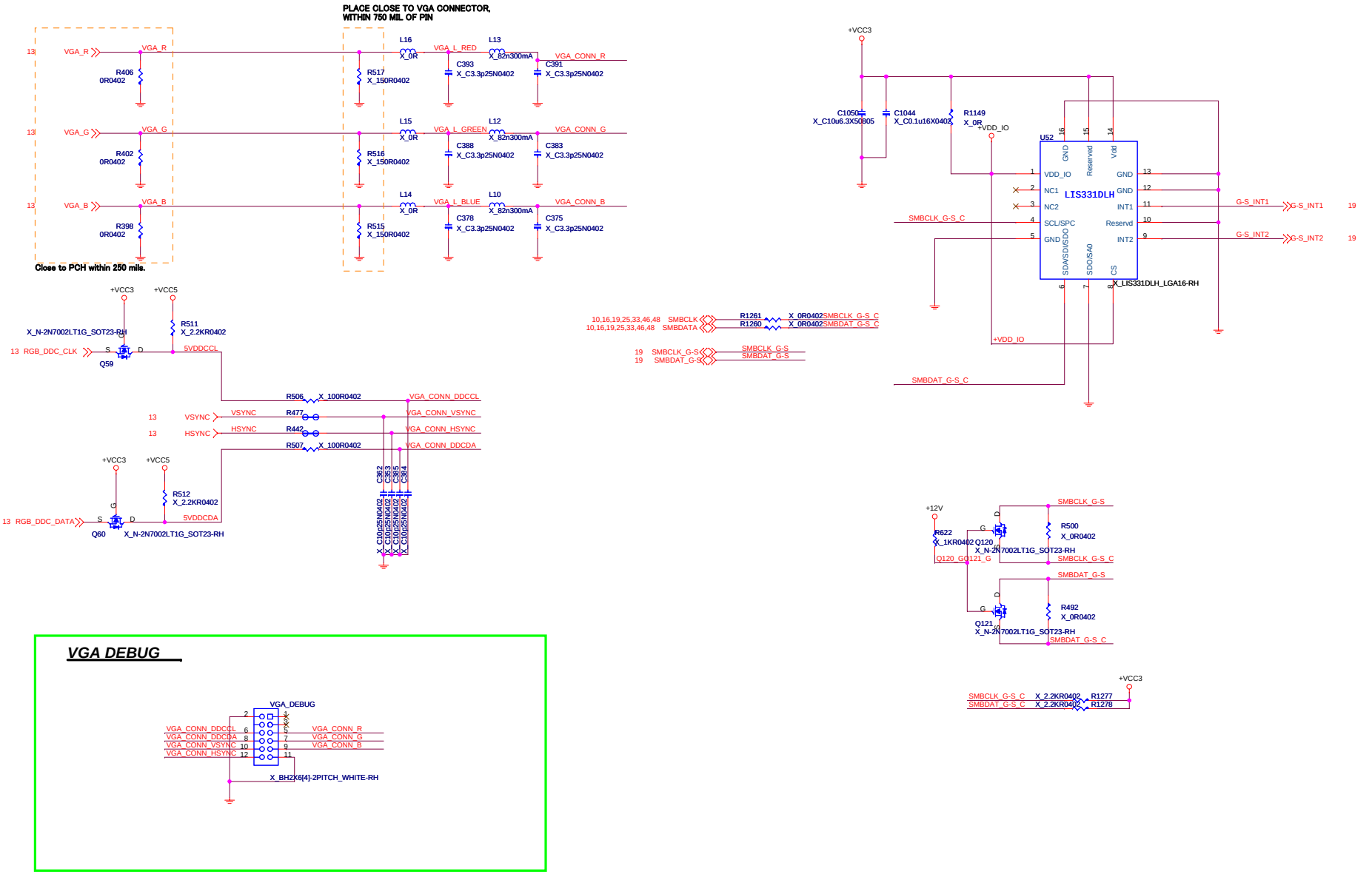

MICRO-STAR INT'L CO.,LTD	
MS-7765	
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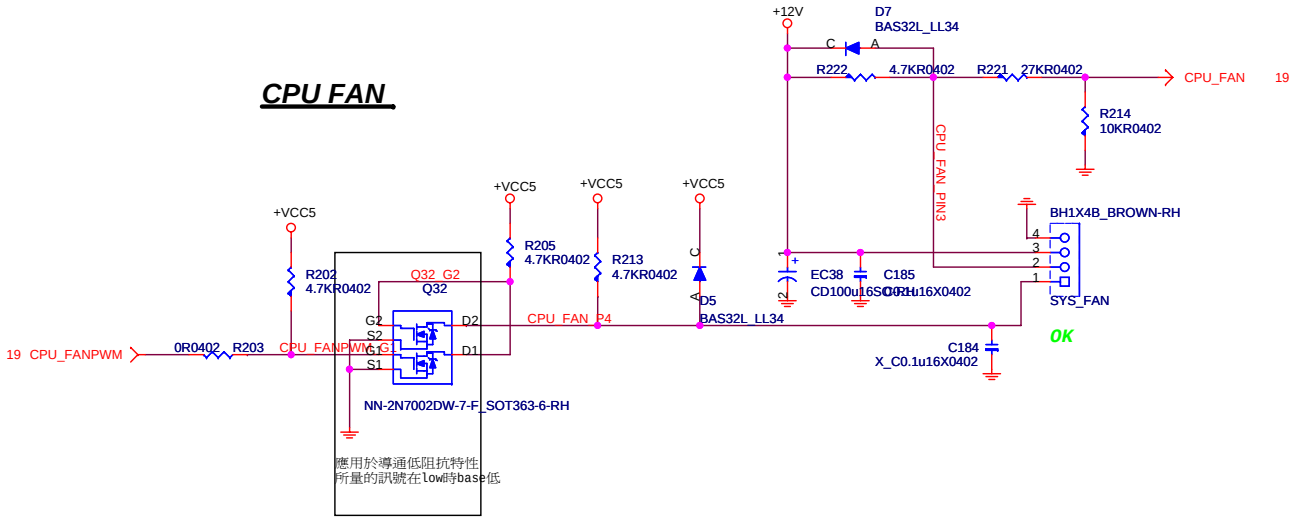
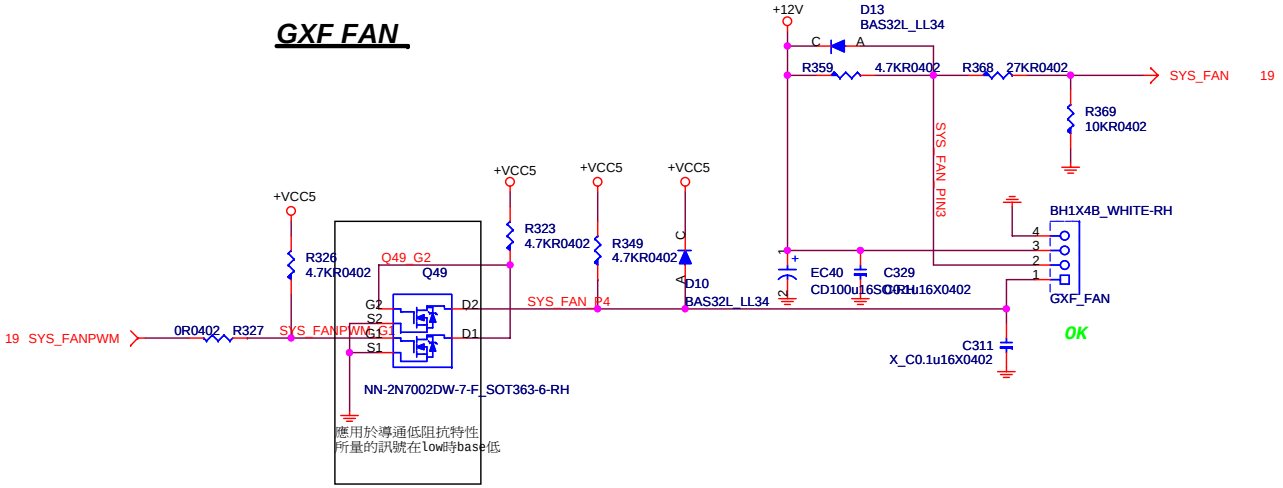
FAN-COUNTROL CIRCUIT

CPU FAN



GXF FAN



MSI	MICRO-STAR INT'L CO.,LTD	
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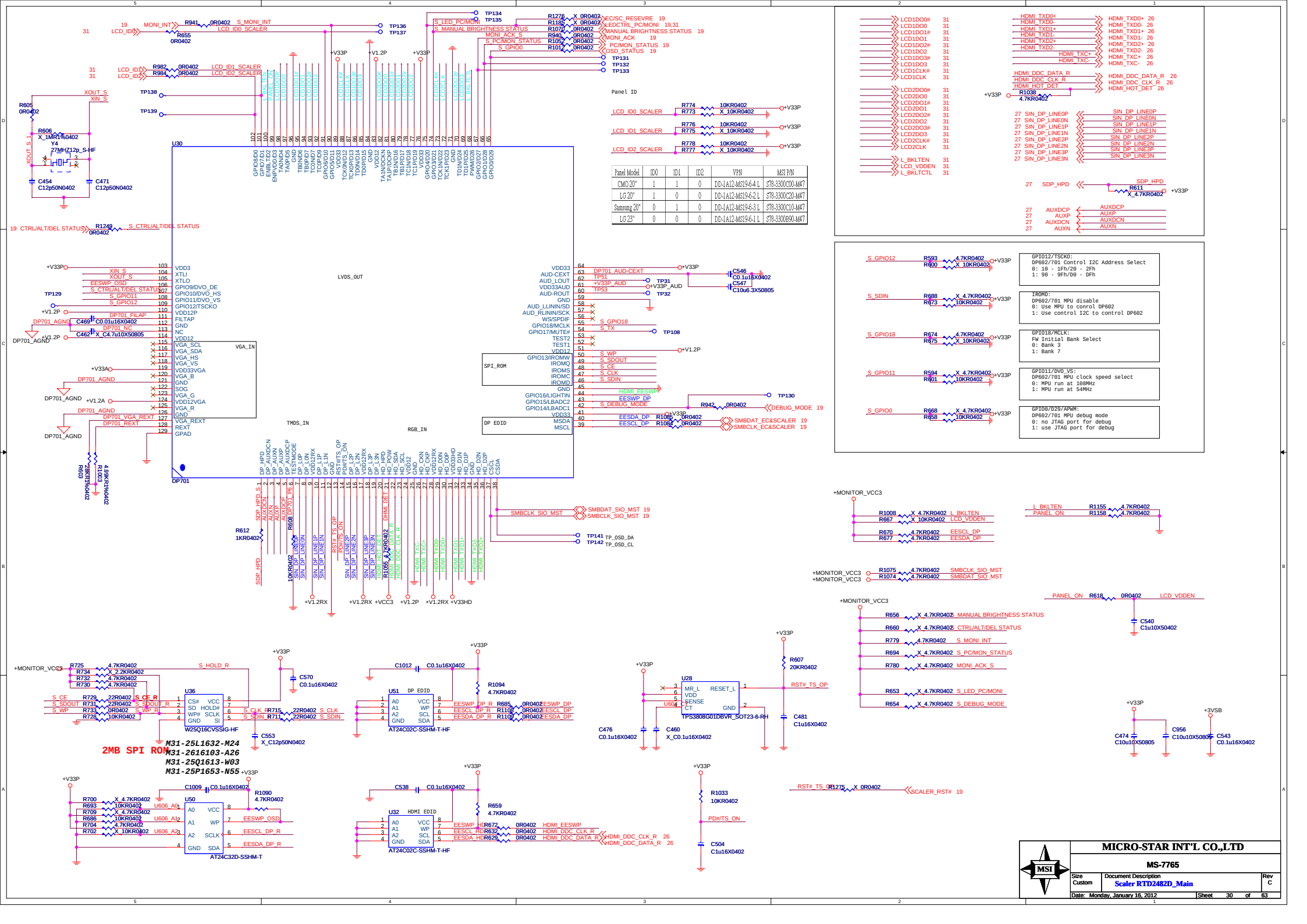
U30
DP701
VGA_IN
LVDS_OUT
SPI_ROM
DP_EDID
TMDS_IN
RGB_IN
Panel ID
LCD_ID0_SCALER
LCD_ID1_SCALER
LCD_ID2_SCALER
Panel Model | ID0 | ID1 | ID2 | VPN | MSI P/N
CM0 20'' | 1 | 1 | 0 | DD-1A12-MS19-6-4 L | S78-3300C00-M47
LG 20'' | 1 | 0 | 0 | DD-1A12-MS19-6-2 L | S78-3300C20-M47
Samsung 20'' | 0 | 1 | 0 | DD-1A12-MS19-6-3 L | S78-3300C10-M47
LG 23'' | 0 | 0 | 0 | DD-1A12-MS19-6-1 L | S78-3300B90-M47
GPIO12/TSCKO:
DP602/701 Control I2C Address Select
0: 10 - 1Fh/20 - 2Fh
1: 90 - 9Fh/D0 - DFh
IROMD:
DP602/701 MPU disable
0: Use MPU to conrol DP602
1: Use control I2C to control DP602
GPIO18/MCLK:
FW Initial Bank Select
0: Bank 3
1: Bank 7
GPIO11/DVO_VS:
DP602/701 MPU clock speed select
0: MPU run at 108MHz
1: MPU run at 54MHz
GPIO8/D29/APWM:
DP602/701 MPU debug mode
0: no JTAG port for debug
1: use JTAG port for debug
2MB SPI ROM
M31-25L1632-M24
M31-2616103-A26
M31-25Q1613-W03
M31-25P1653-N55
U36
W25Q16CVSSIG-HF
U51 DP EDID
AT24C02C-SSHM-T-HF
U28
TPS3808G01DBVR_SOT23-6-RH
U50
AT24C32D-SSHM-T
U32 HDMI EDID
AT24C02C-SSHM-T-HF
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Scaler RTD2482D_Main
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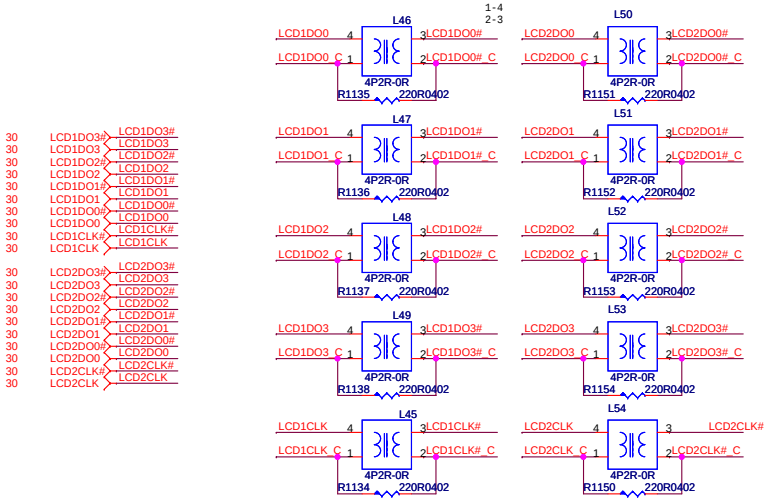
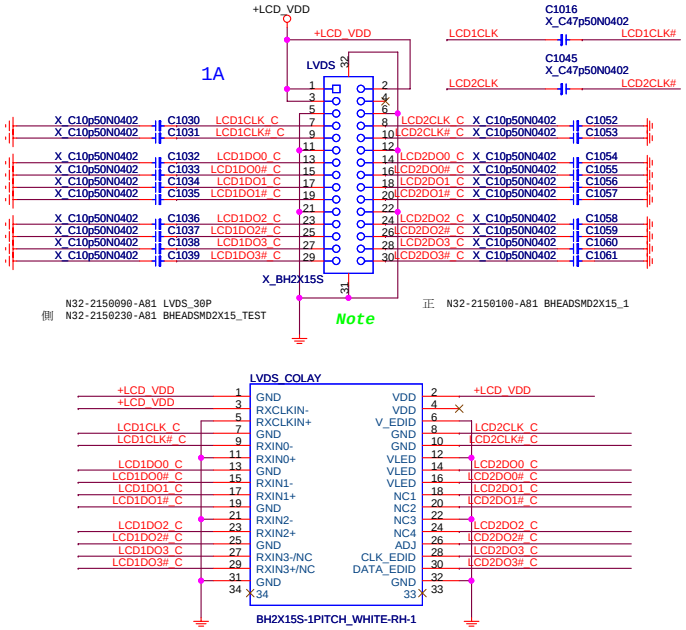
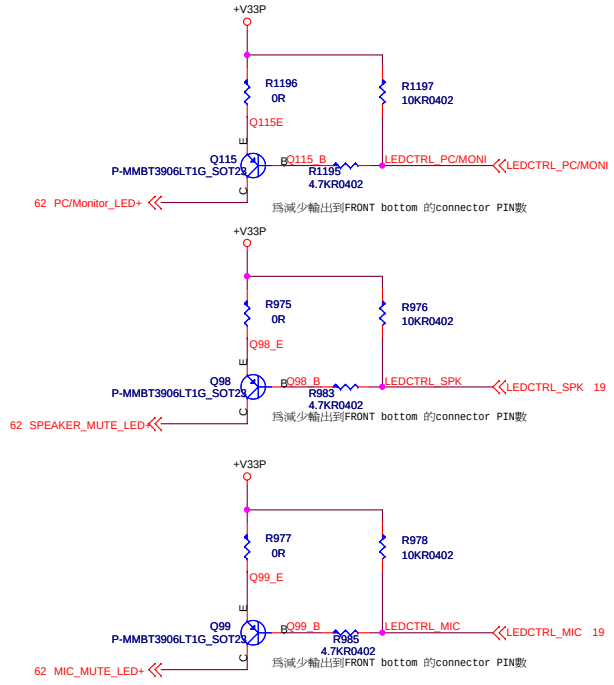
LVDS Connector

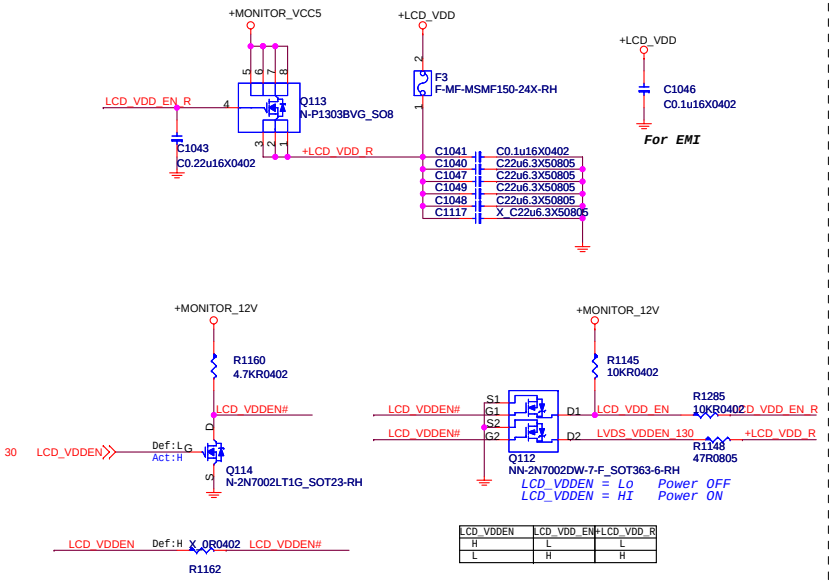




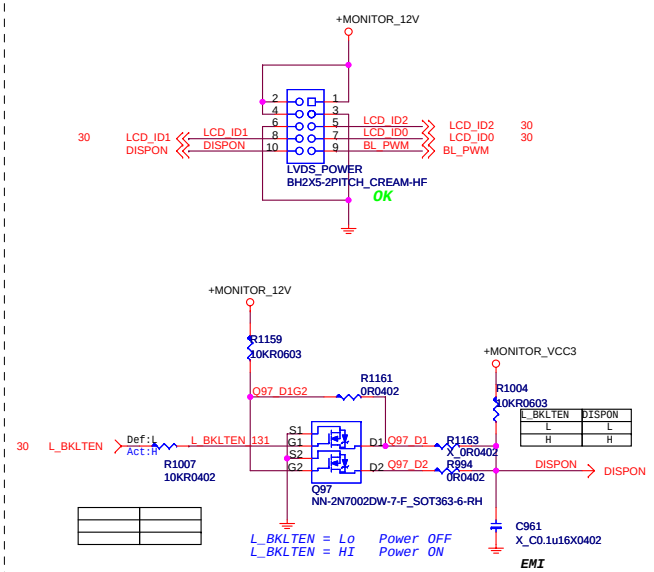
OSD Button LED Control



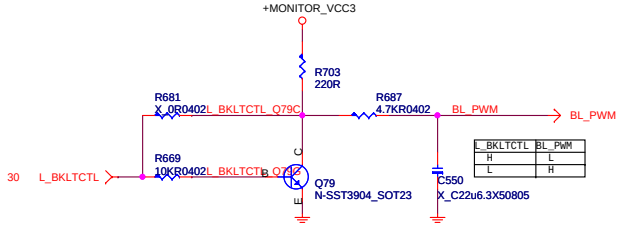
Panel Controller Power



Panel Converter Power



Panel Backlight Control



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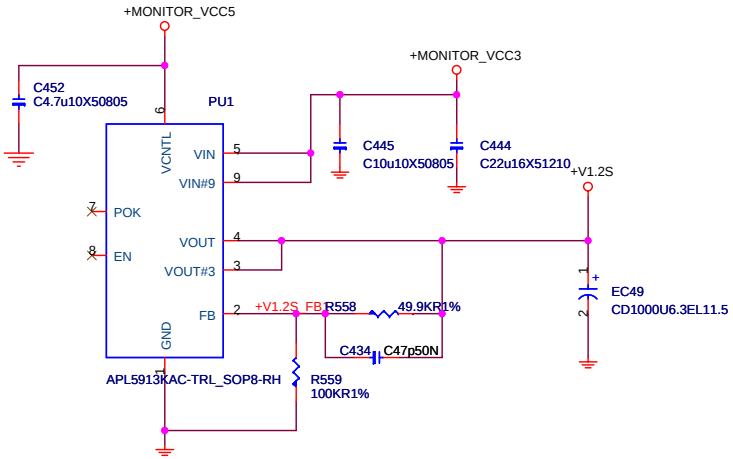
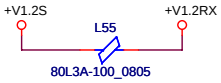
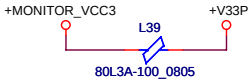
DP701 Power

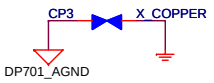


VDD12RX
9,17,28

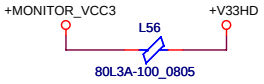


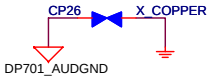
VDD33
41,64,76,89,103





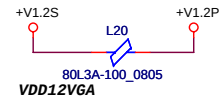
VDD33HD
31



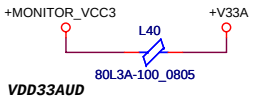


VDD12P
110 AGND

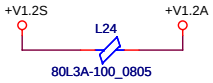
VDD12
24,51,83,114



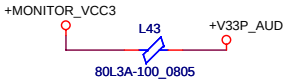
VDD33VGA
119 AGND

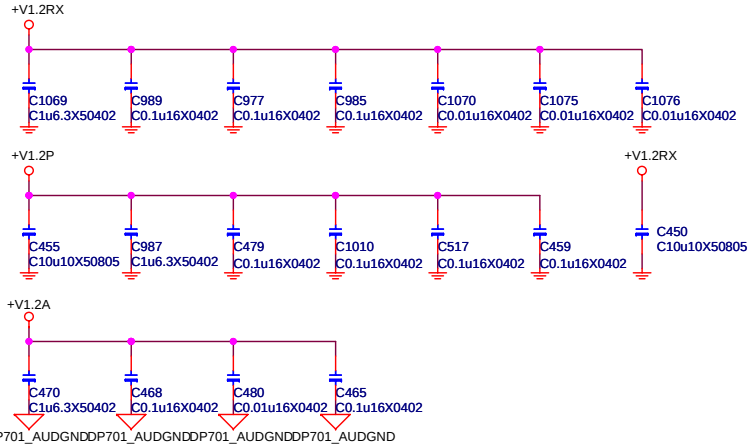


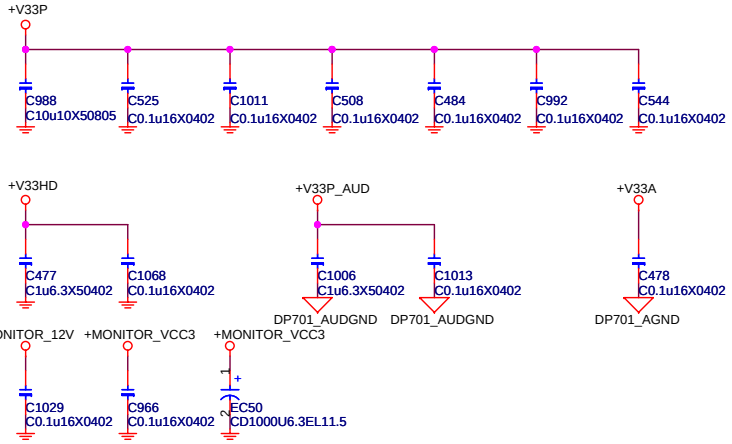
VDD12VGA
124 AGND



VDD33AUD
61 AUDGND







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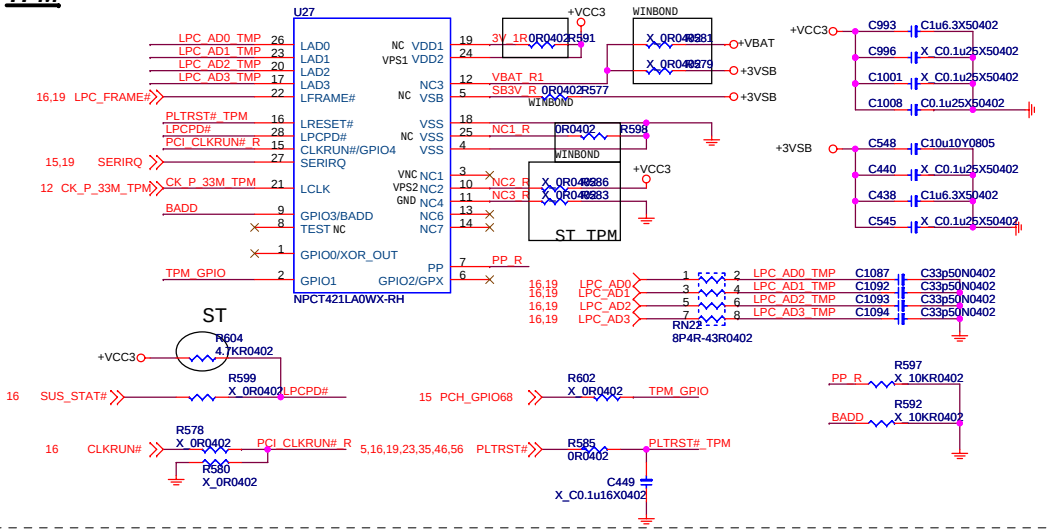
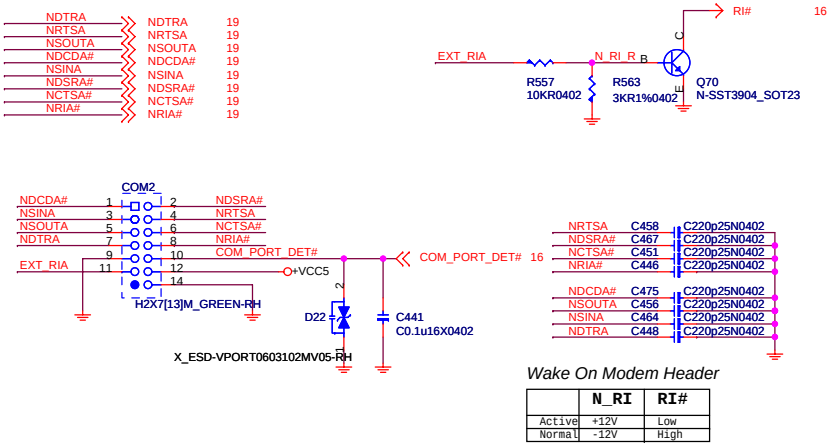
TPM



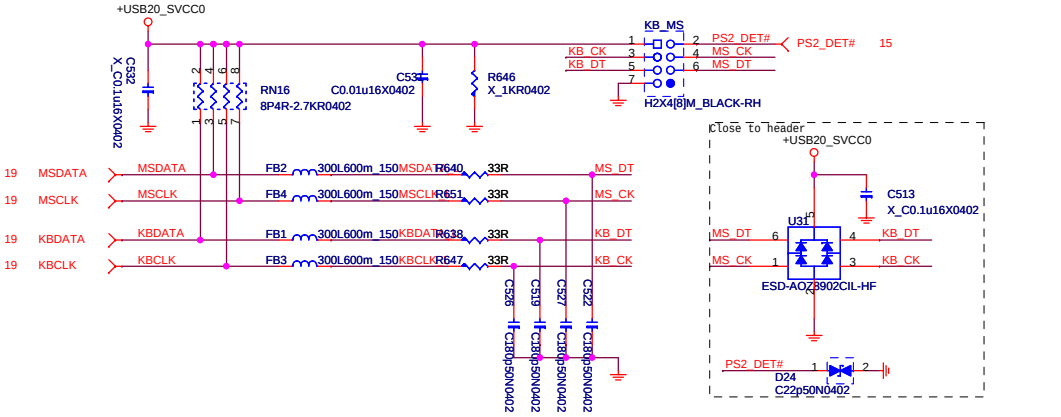
SERIAL PORT 1



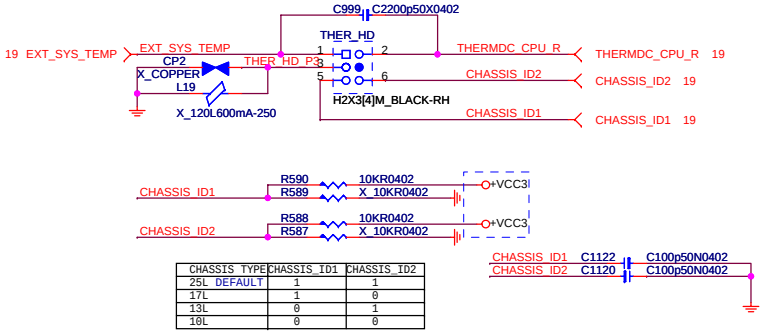
Wake On Modem Header

	N_RI	RI#
Active	+12V	Low
Normal	-12V	High

PS2 KB/MS HEADER

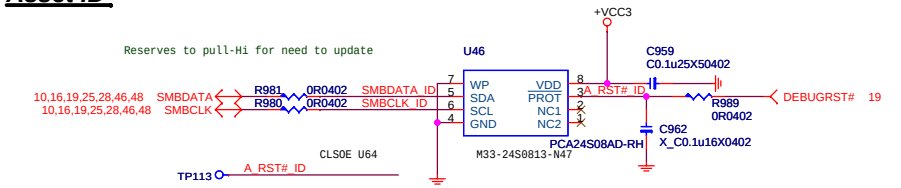


Sys sensor header

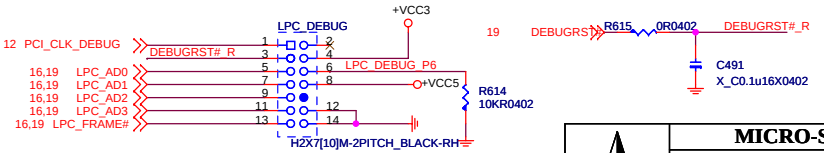


CHASSIS_TYPE	CHASSIS_ID1	CHASSIS_ID2
25L DEFAULT	1	1
17L	1	0
13L	0	1
10L	0	0

Asset ID



LPC DEBUG



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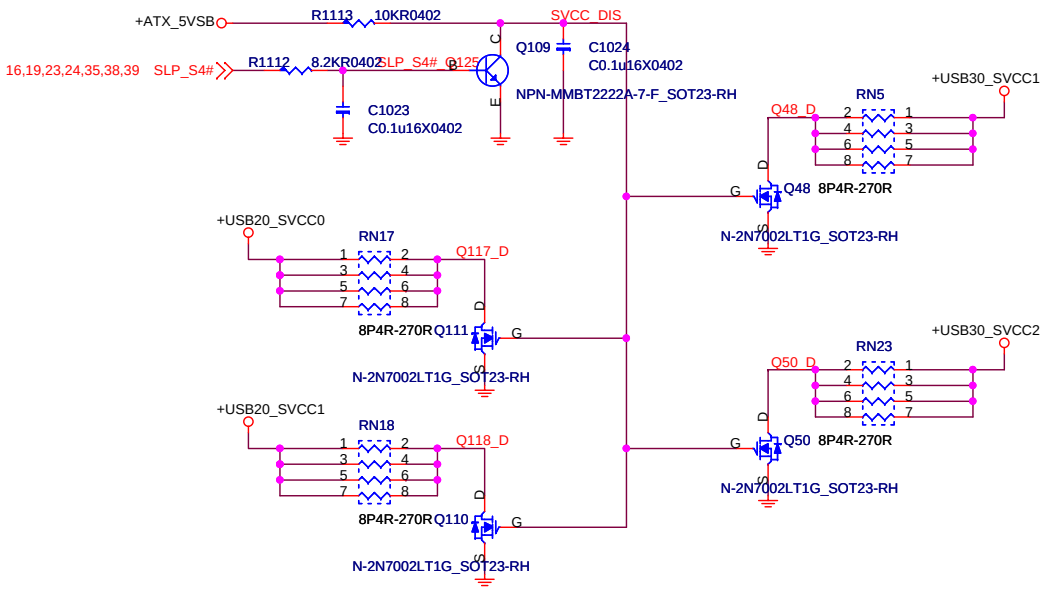
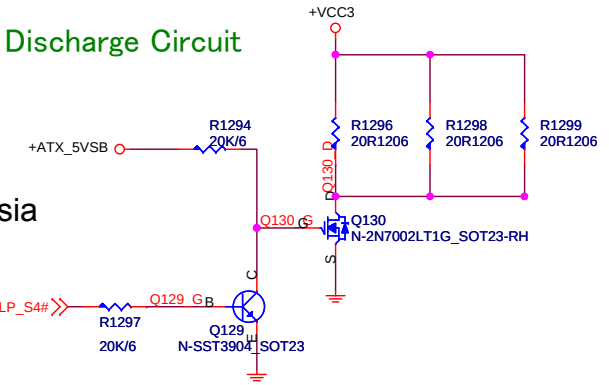
USB power discharge circuit



Discharge Circuit



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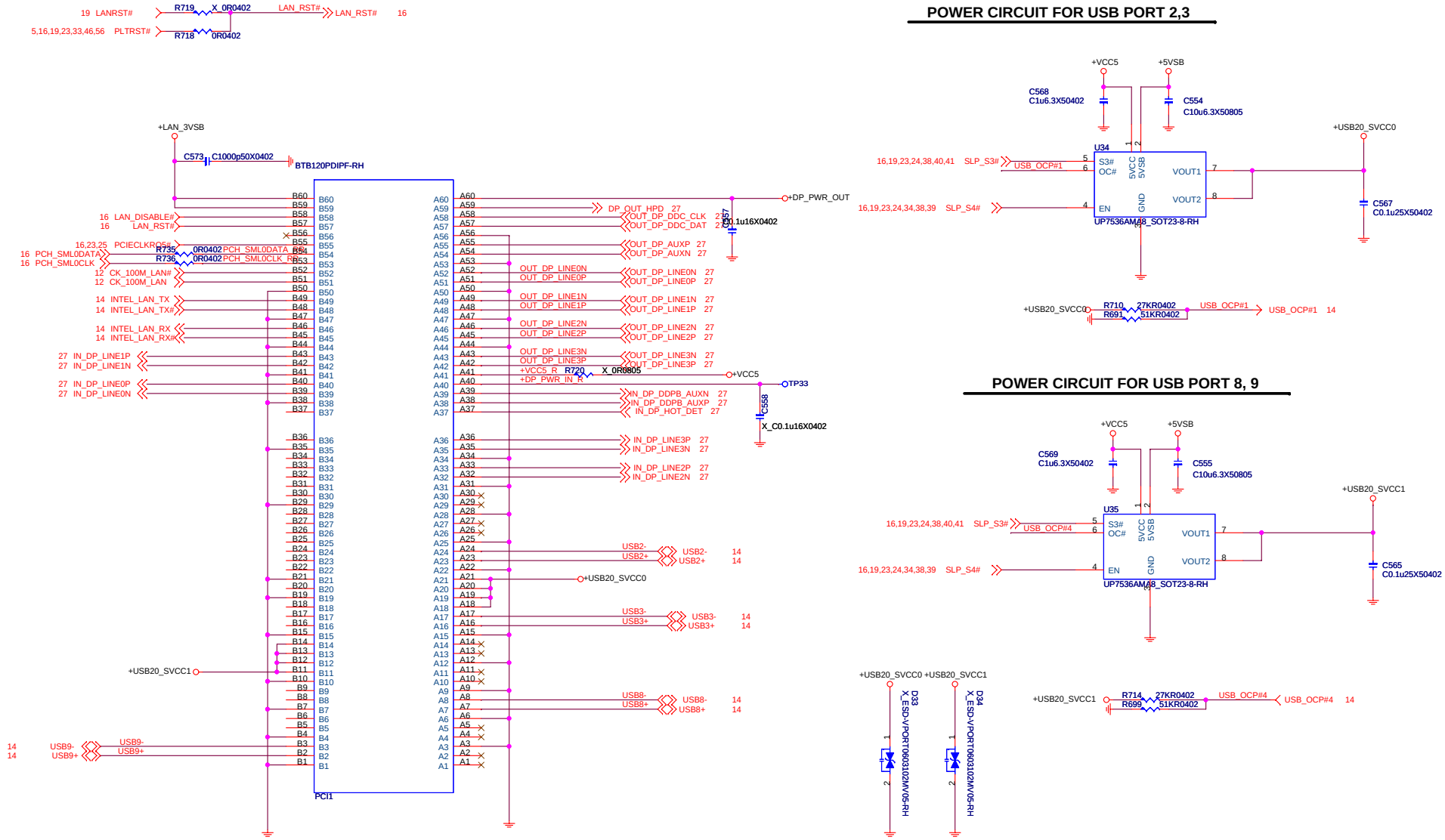

POWER CIRCUIT FOR USB PORT 2,3

POWER CIRCUIT FOR USB PORT 8, 9

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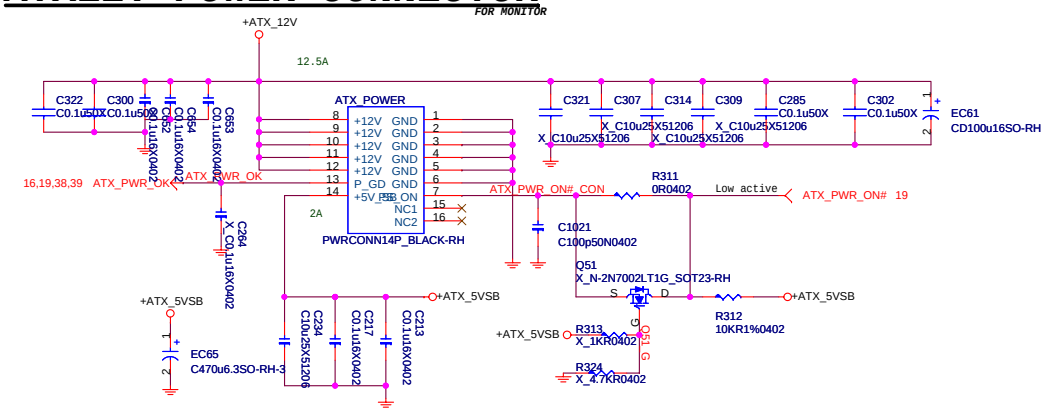
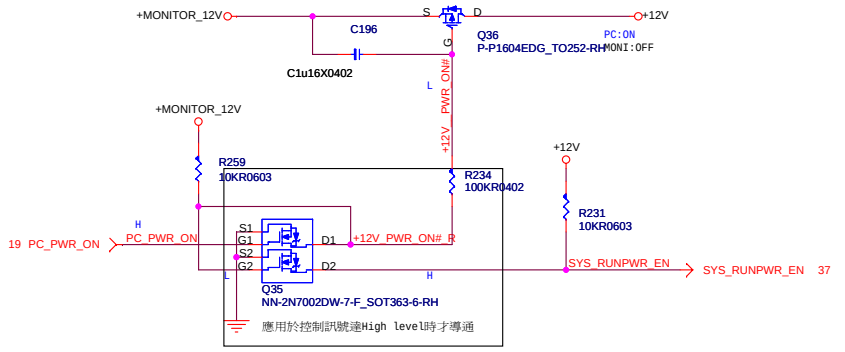
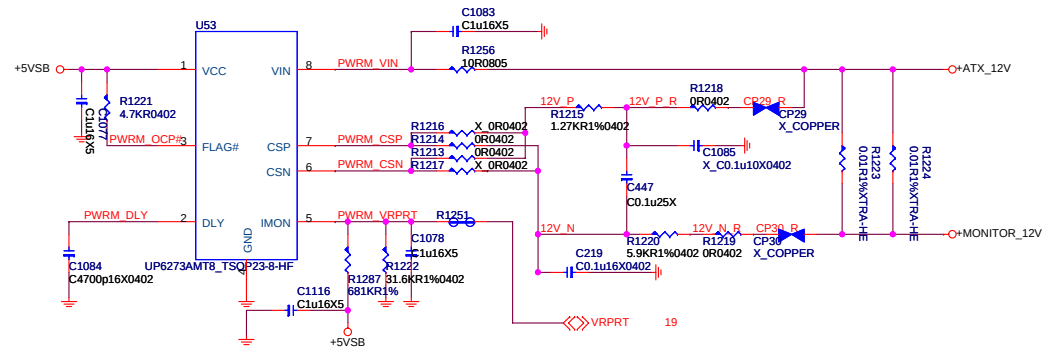
ATX12V POWER CONNECTOR



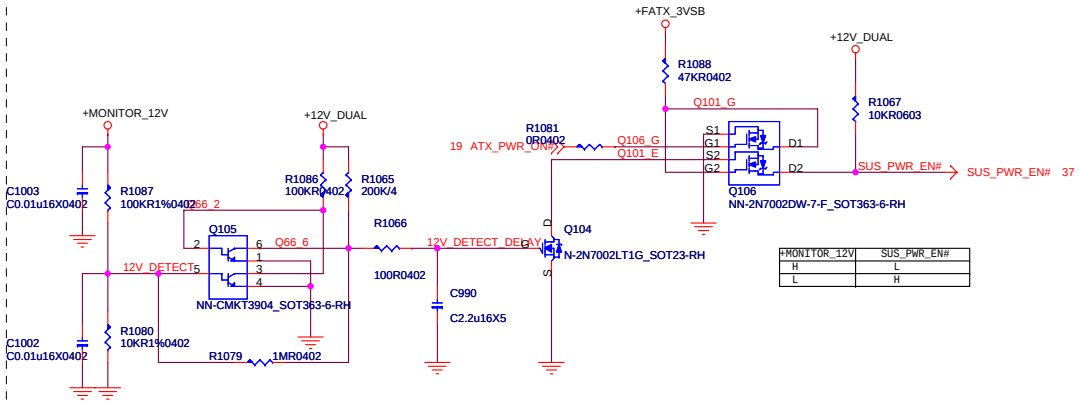
12V POWER FOR SYSTEM



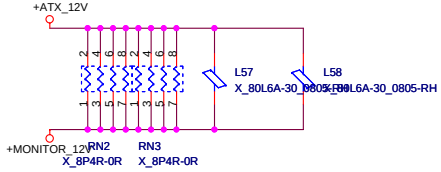
POWER METER



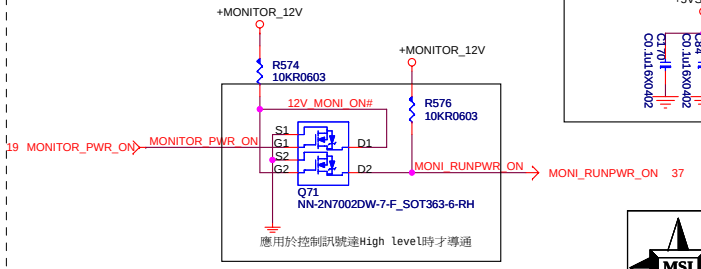
Monitor Power Contorl



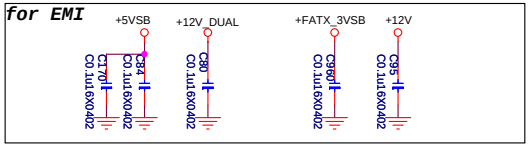
12V DUAL FOR SYSTEM



Monitor Power Contorl



for EMI



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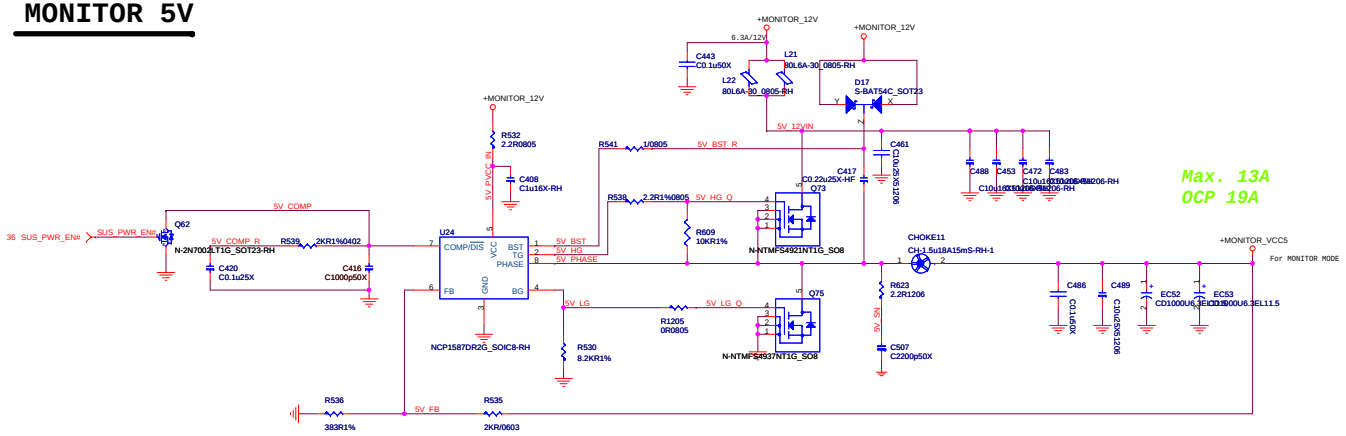
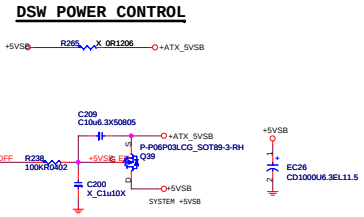
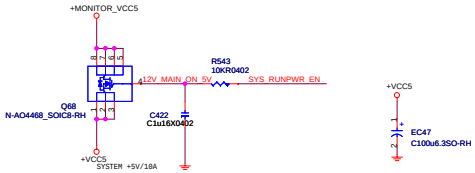
MONITOR 5V



DSW POWER CONTROL

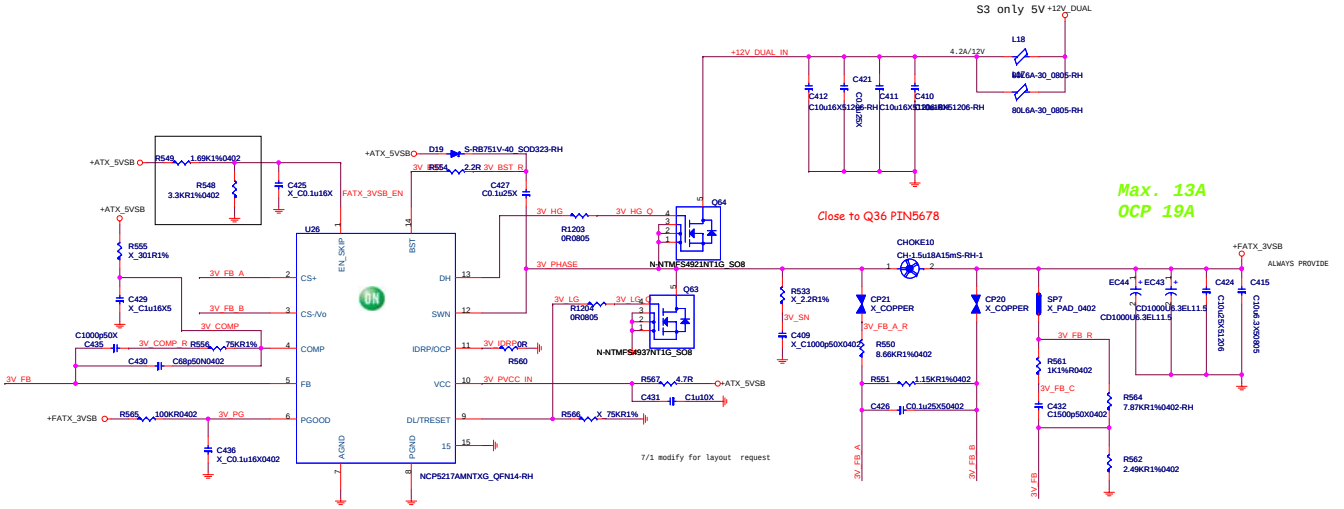


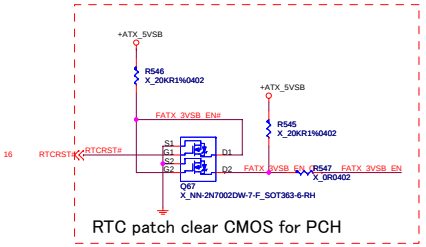
PC 5V

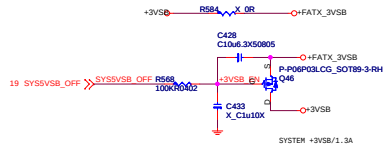


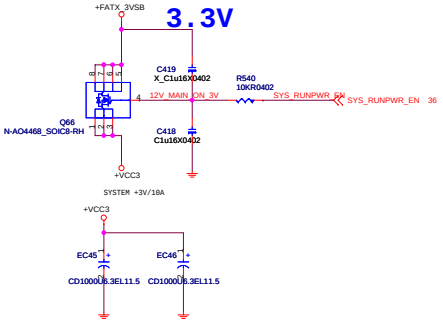
DSW_3VSB

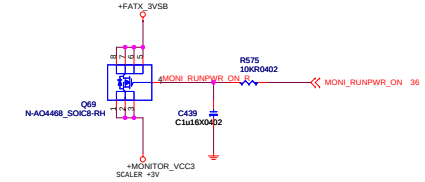
DSW POWER CONTROL











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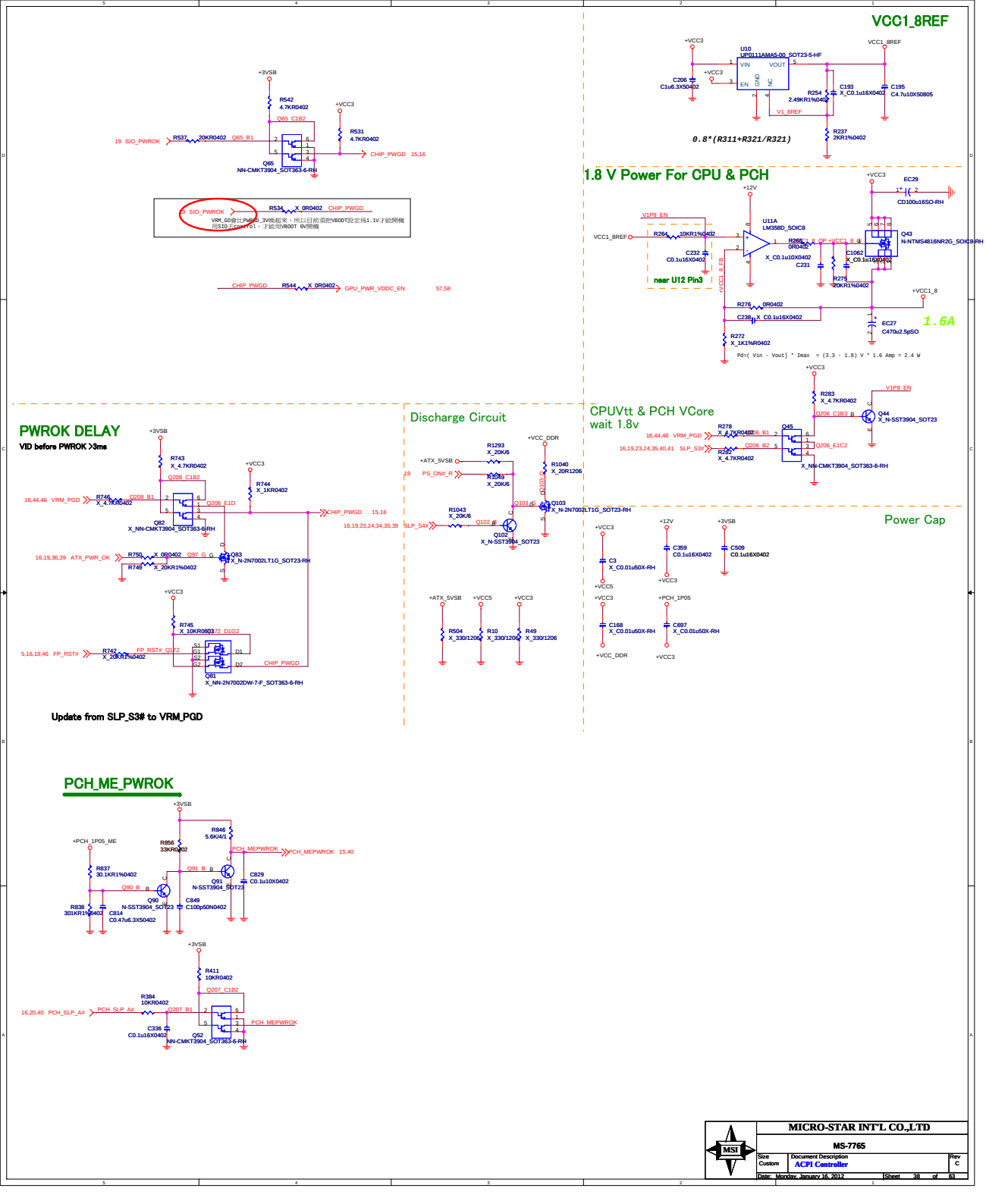
VCC1_8REF
+VCC3
U10
UP0111AMA5-00_SOT23-5-HF
VIN
VOUT
EN
GND
NC
C206
C1u6.3X50402
C193
X_C0.1u16X0402
C195
C4.7u10X50805
R254
2.49KR1%0402
V1_8REF
R237
2KR1%0402
0.8*(R311+R321/R321)
1.8 V Power For CPU & PCH
+12V
V1P8_EN
VCC1_8REF
R264
10KR1%0402
near U12 Pin3
U11A
LM358D_SOIC8
R265
0R0402
C232
C0.1u16X0402
X_C0.1u10X0402
C231
C1062
X_C0.1u16X0402
R275
20KR1%0402
Q43
N-NTMS4816NR2G_SOIC8-RH
EC29
CD100u16SO-RH
+VCC1_8
R276
0R0402
C238
X_C0.1u16X0402
EC27
C470u2.5pSO
1.6A
R272
X_1K1%R0402
Pd=(Vin - Vout] * Imax = (3.3 - 1.8) V * 1.6 Amp = 2.4 W
CPUVtt & PCH VCore
wait 1.8v
R283
X_4.7KR0402
Q206_C1B3
Q44
X_N-SST3904_SOT23
16,44,46 VRM_PGD
R278
X_4.7KR0402
Q206_B1
Q45
Q206_B2
16,19,23,24,35,40,41 SLP_S3#
R282
X_4.7KR0402
Q206_E1C2
X_NN-CMKT3904_SOT363-6-RH
PWROK DELAY
VID before PWROK >3ms
+3VSB
R743
X_4.7KR0402
Q208_C1B2
+VCC3
R744
X_1KR0402
16,44,46 VRM_PGD
R746
X_4.7KR0402
Q208_B1
Q208_E1D
Q82
X_NN-CMKT3904_SOT363-6-RH
CHIP_PWGD 15,16
16,19,23,24,34,35,39 SLP_S4#
16,19,36,39 ATX_PWR_OK
R750
X_0R0402
Q97_G
Q83
X_N-2N7002LT1G_SOT23-RH
R749
X_20KR1%0402
R745
X_10KR0603
Q72_D1G2
5,16,19,46 FP_RST#
R742
X_20KR1%0402
FP_RST#_Q72
Q81
X_NN-2N7002DW-7-F_SOT363-6-RH
Update from SLP_S3# to VRM_PGD
Discharge Circuit
+VCC_DDR
+ATX_5VSB
R1293
X_20K/6
19 PS_ON#_R
R1039
X_20K/6
R1040
X_20R1206
Q103_D
Q103_G
Q103
X_N-2N7002LT1G_SOT23-RH
R1043
X_20K/6
Q102_B
Q102
X_N-SST3904_SOT23
+VCC5
R504
X_330/1206
R10
X_330/1206
R49
X_330/1206
Power Cap
+12V
+3VSB
C3
X_C0.01u50X-RH
C359
C0.1u16X0402
C509
C0.1u16X0402
+PCH_1P05
C168
X_C0.01u50X-RH
C697
X_C0.01u50X-RH
PCH_ME_PWROK
+PCH_1P05_ME
R846
5.6K/4/1
R856
33KR0402
PCH_MEPWROK
PCH_MEPWROK 15,40
R837
30.1KR1%0402
Q91_B
Q90_B
Q91
N-SST3904_SOT23
C829
C0.1u10X0402
Q90
N-SST3904_SOT23
C849
C100p50N0402
R838
301KR1%0402
C814
C0.47u6.3X50402
R411
10KR0402
Q207_C1B2
R384
10KR0402
16,20,40 PCH_SLP_A#
PCH_SLP_A#
Q207_B1
C336
C0.1u16X0402
Q52
NN-CMKT3904_SOT363-6-RH
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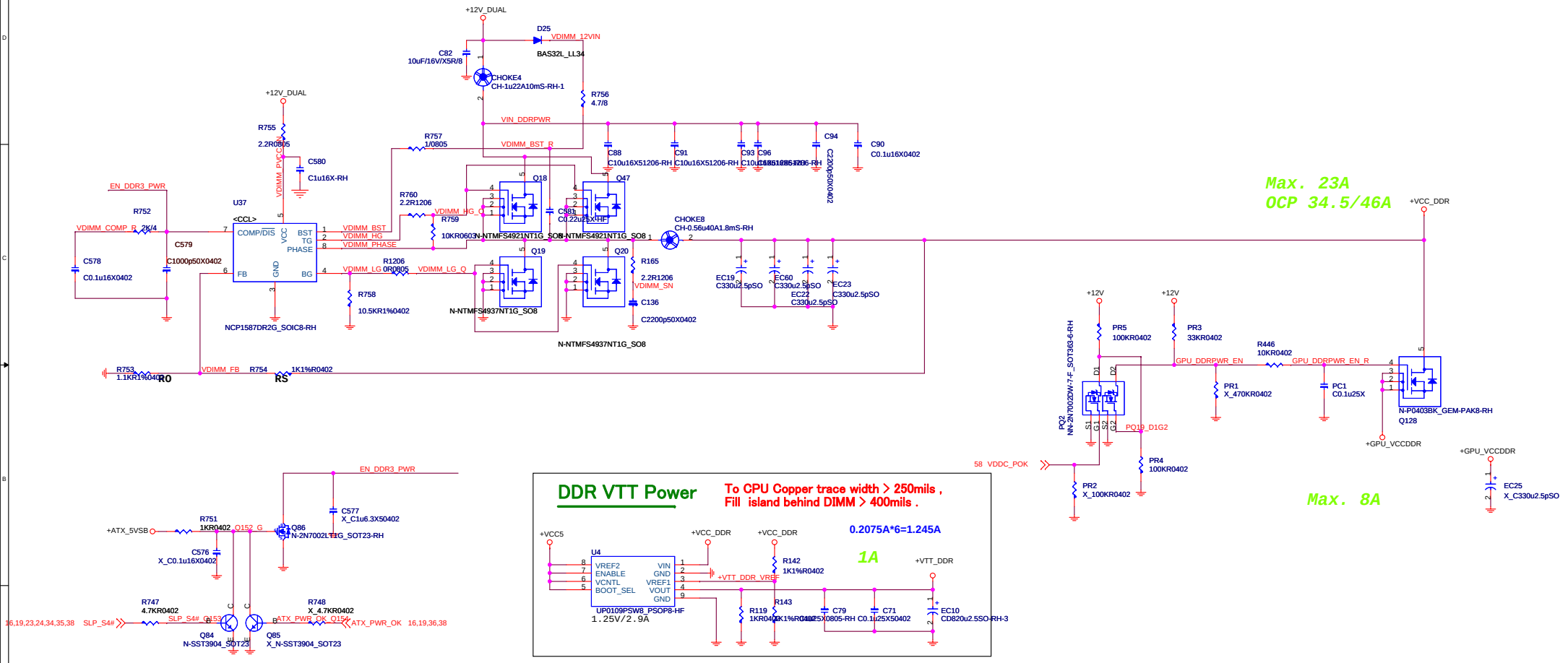
DDR III 1.5V POWER

PN:I32-0158703-005



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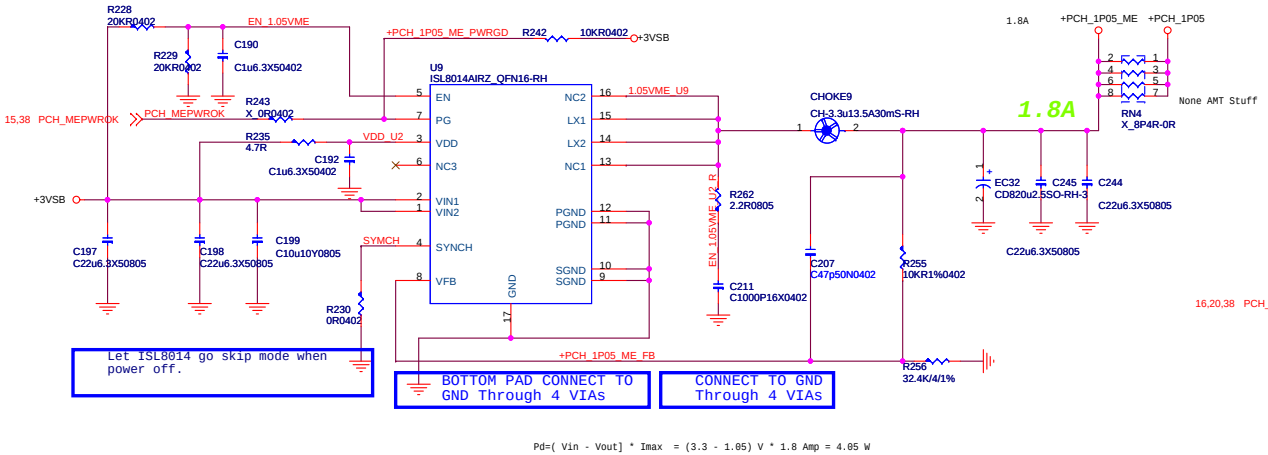
PCH_1P05_ME

(4>1.8A)

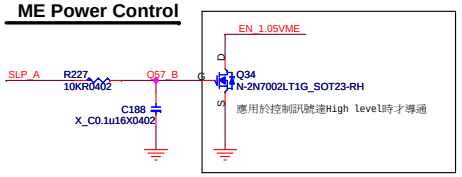
VCCIO_ME : OCP Max=6A

6.2A(PCH)+1.8A=8A

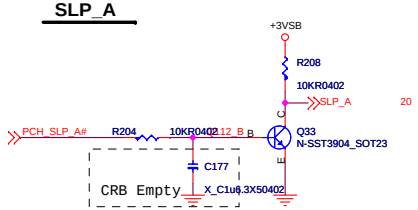


Pd=(Vin - Vout] * Imax = (3.3 - 1.05) V * 1.8 Amp = 4.05 W

ME Power Control



SLP_A



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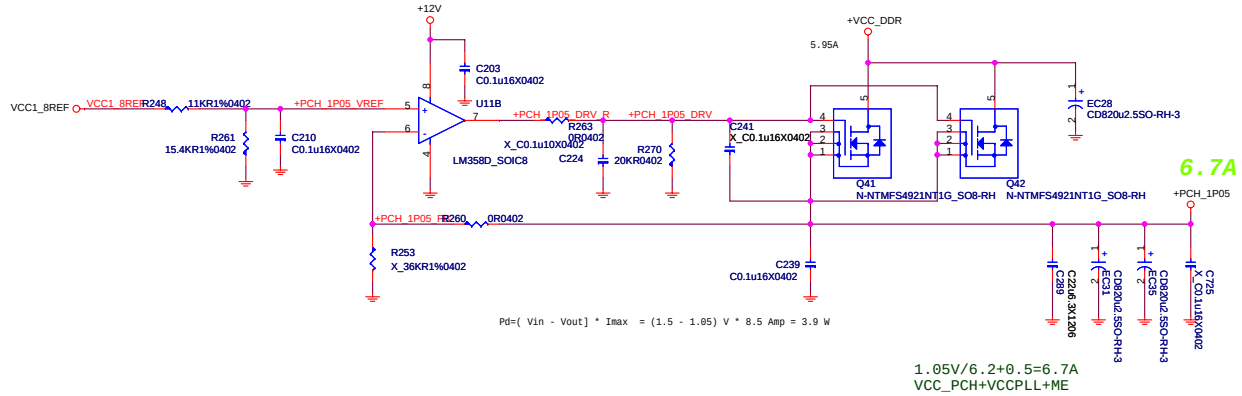
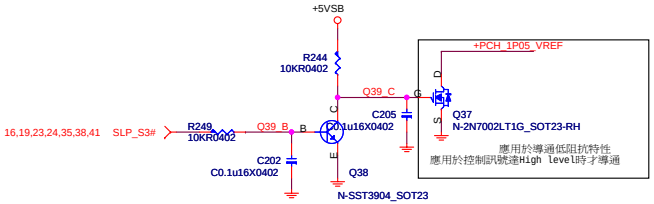
PCH Core Power



Pd=(Vin - Vout] * Imax = (1.5 - 1.05) V * 8.5 Amp = 3.9 W

1.05V/6.2+0.5=6.7A

VCC_PCH+VCCPLL+ME



MICRO-STAR INT'L CO.,LTD		
MS-7765		
Size: Custom	Document Description: PCH Power	Rev: C
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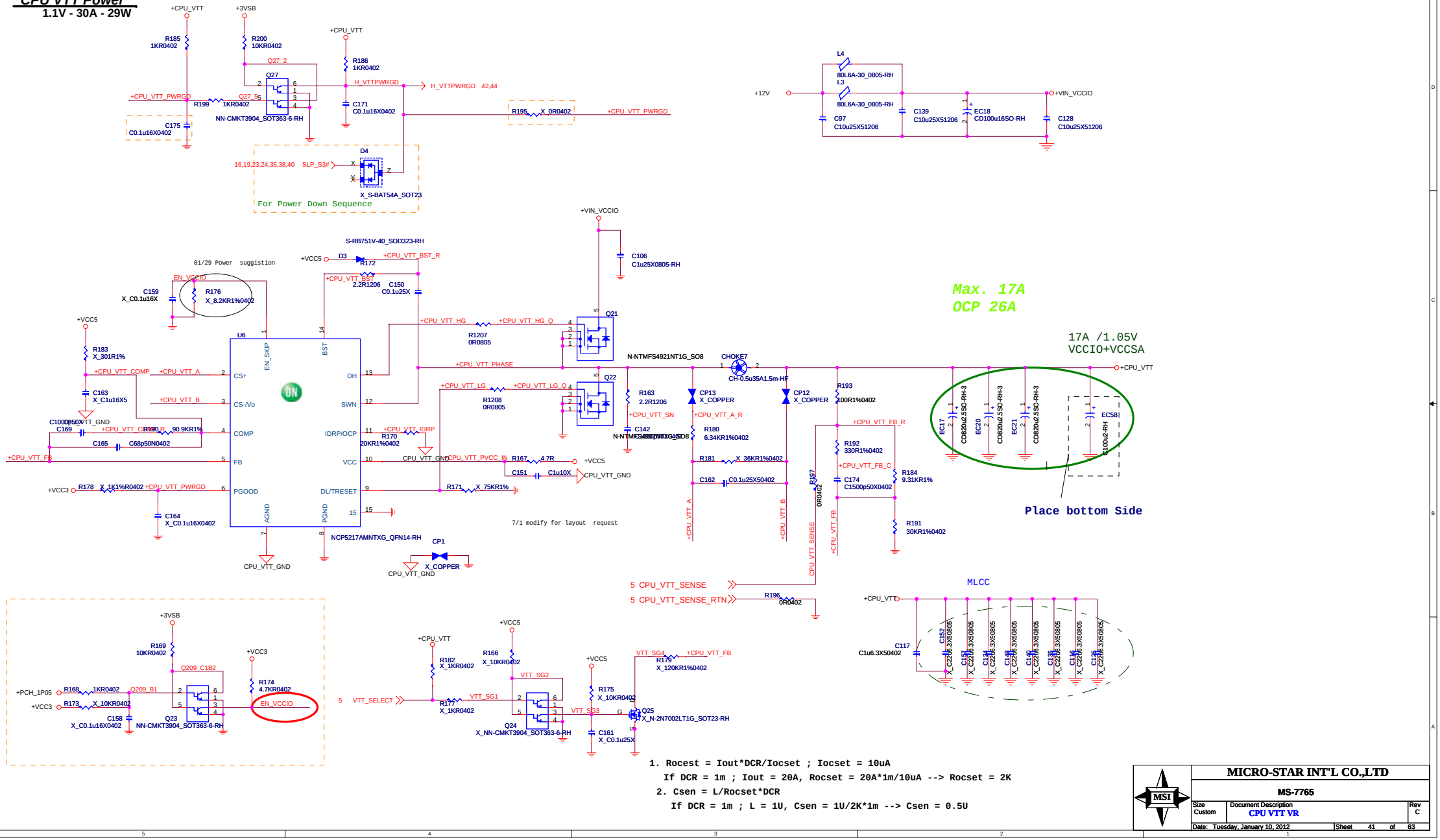
CPU VTT Power

1.1V - 30A - 29W



1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K
2. Csen = L/Rocset*DCR
   If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

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Size: Custom	Document Description: CPU VTT VR	Rev: C
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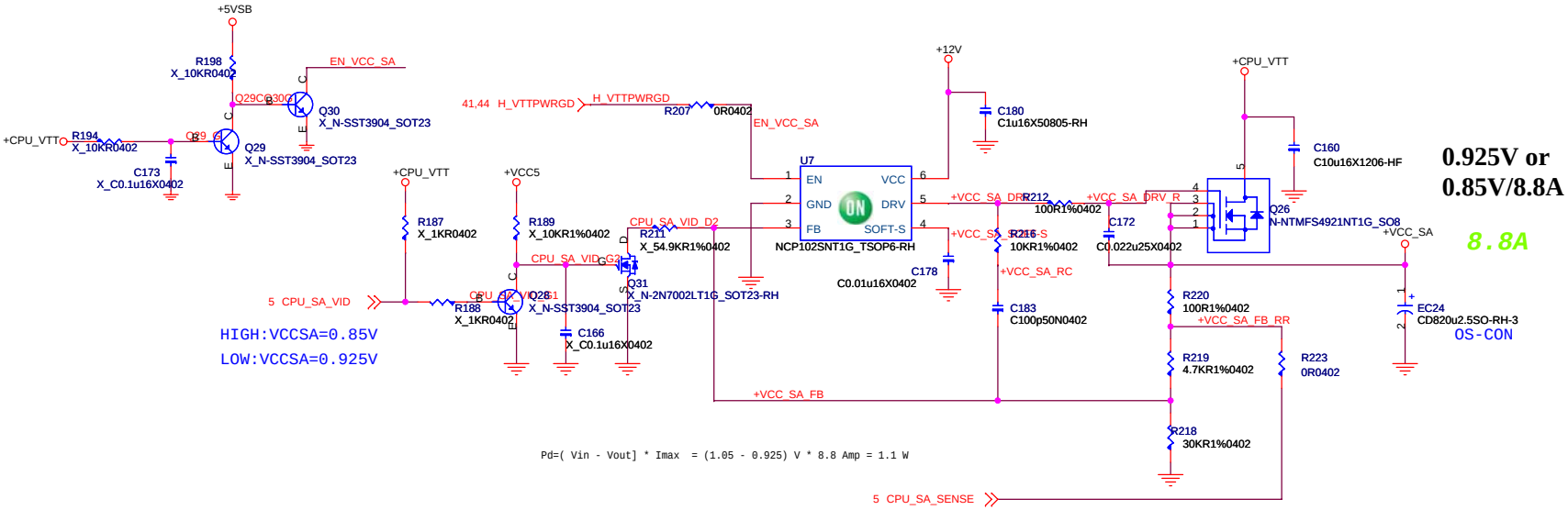
VCCSA



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: VCCSA VR	Rev: C
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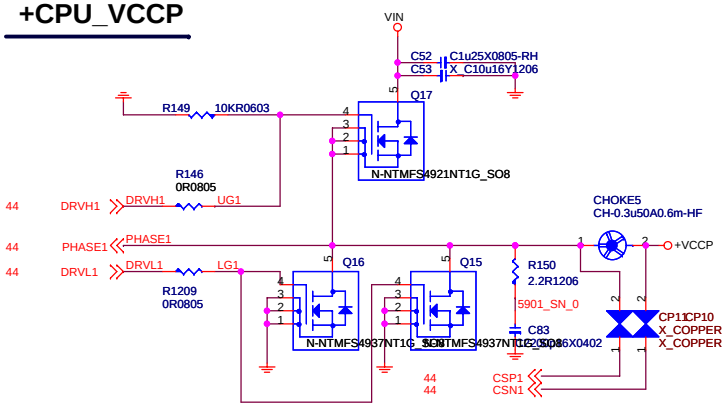
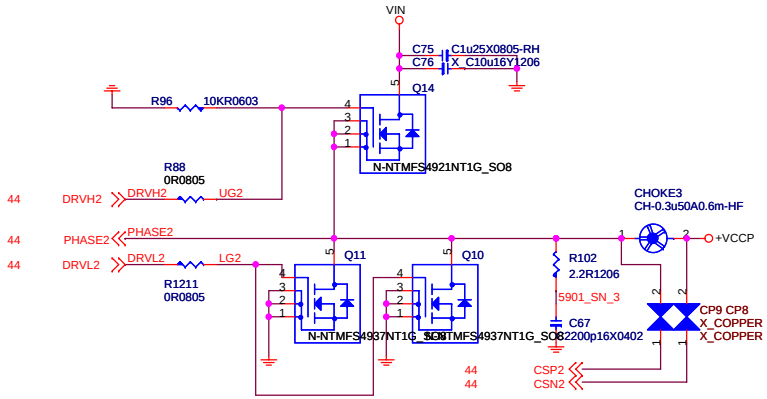
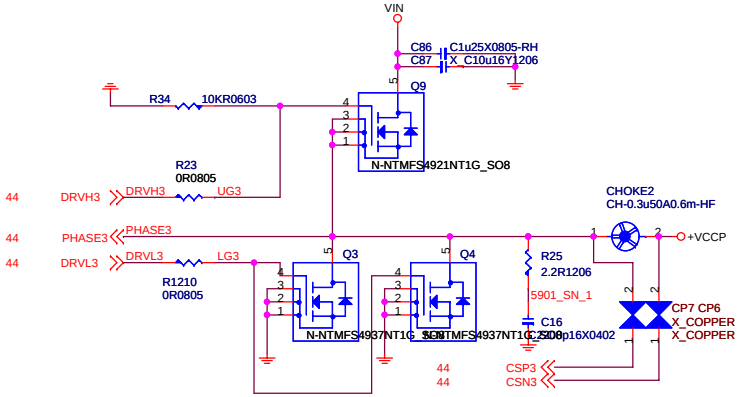
+CPU_VCCP

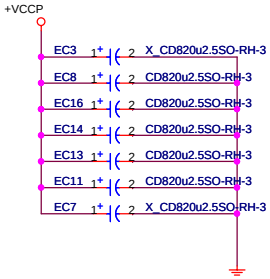


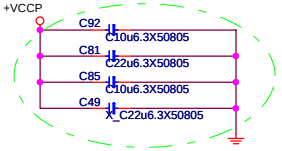


Max.75A
OCP 112A

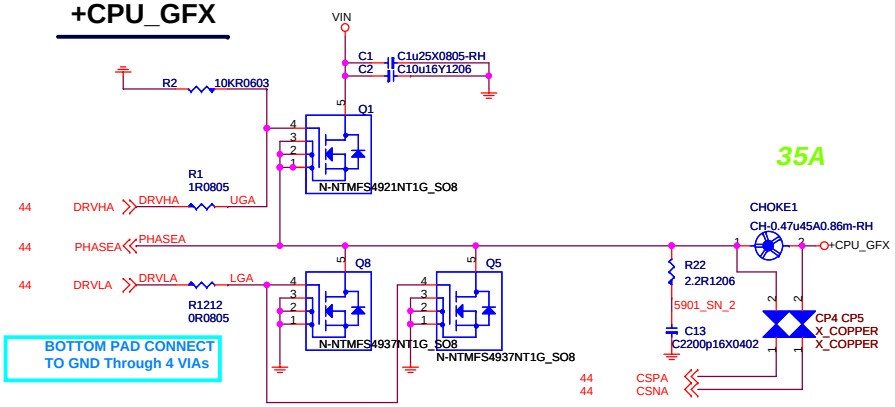


+CPU_VCCP Output Caps

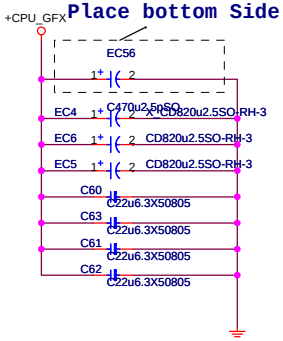




+CPU_GFX



BOTTOM PAD CONNECT TO GND Through 4 VIAs



MICRO-STAR INT'L CO.,LTD		
MS-7765		
Size: Custom	Document Description: VCORE & VGFX POWER	Rev: C
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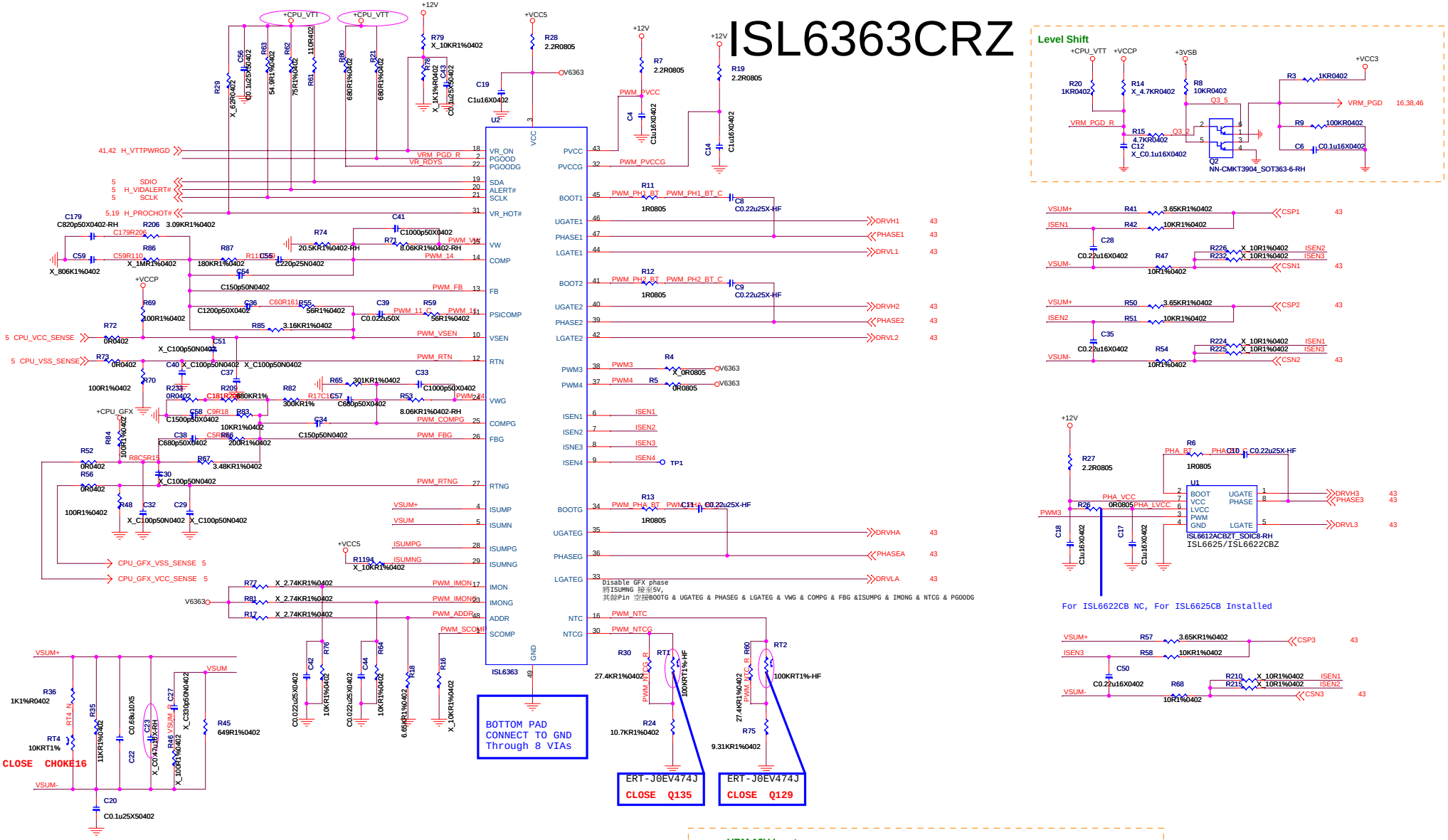
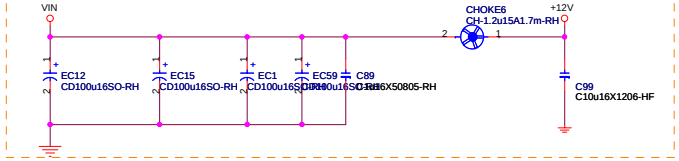
ISL6363CRZ





MICRO-STAR INT'L CO.,LTD	
MS-7765	
Size: Custom	Document Description: Intersil/ISL6363CRZ &ISL6612 3+1 PHASE
Rev: C	
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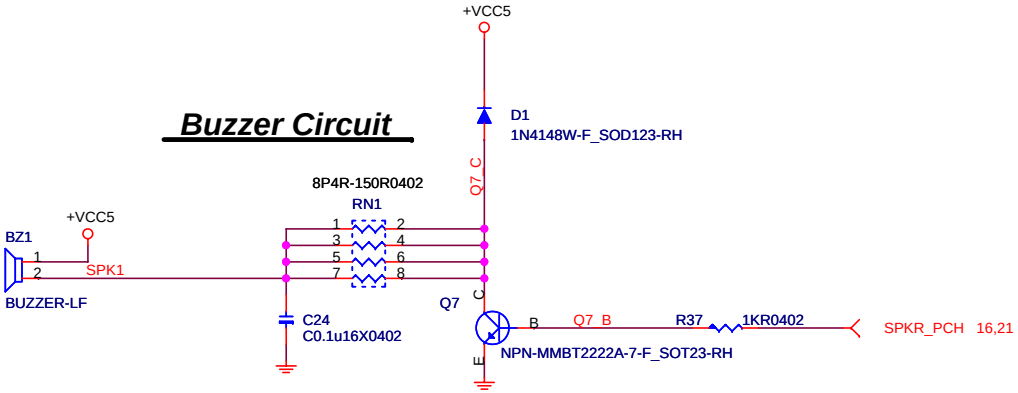
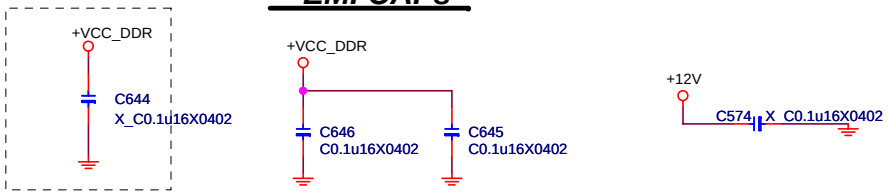
Buzzer Circuit

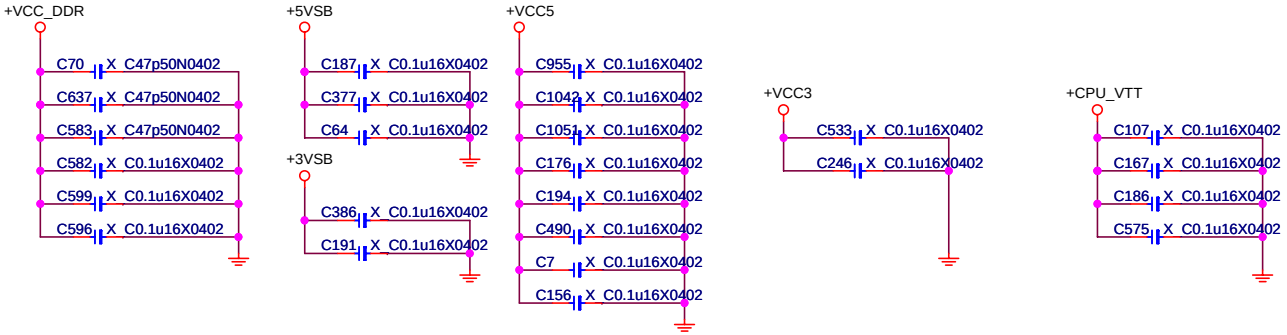


EMI CAPs



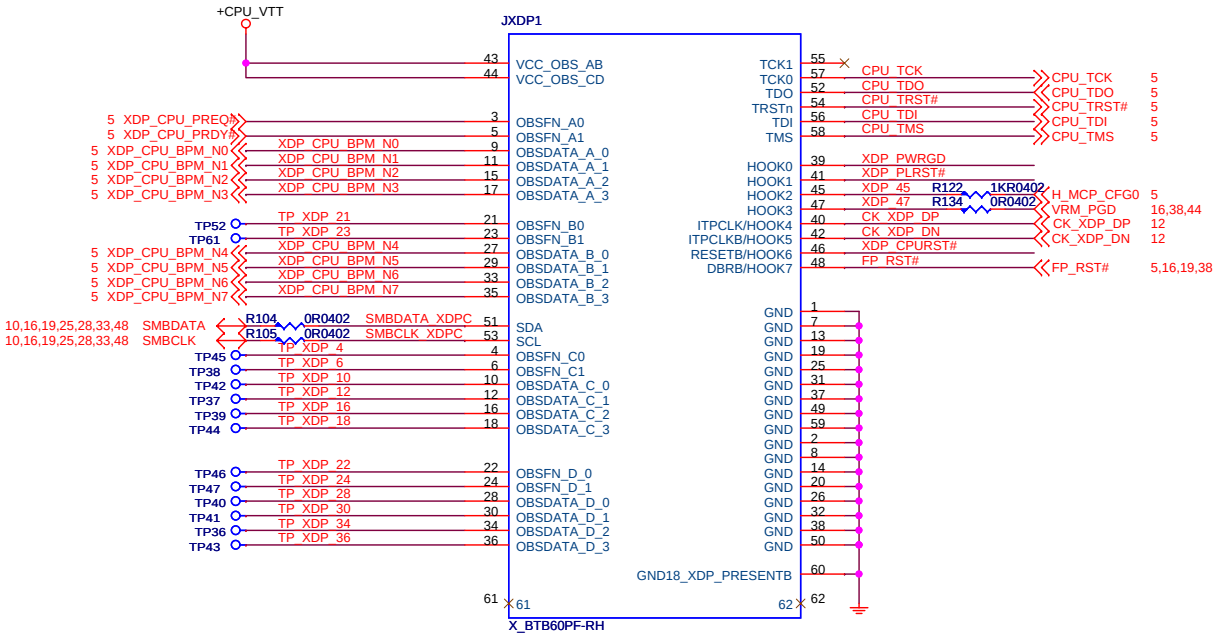
For EMI

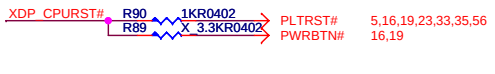
For EMI

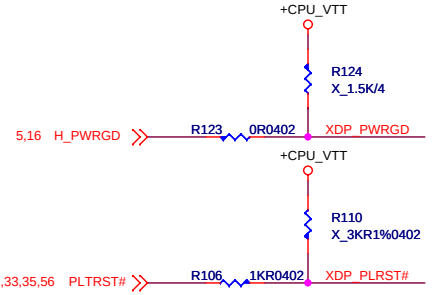


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: EMI & Buzzer	Rev: C
Date: Friday, December 16, 2011	Sheet 45 of 63	

CPU XDP

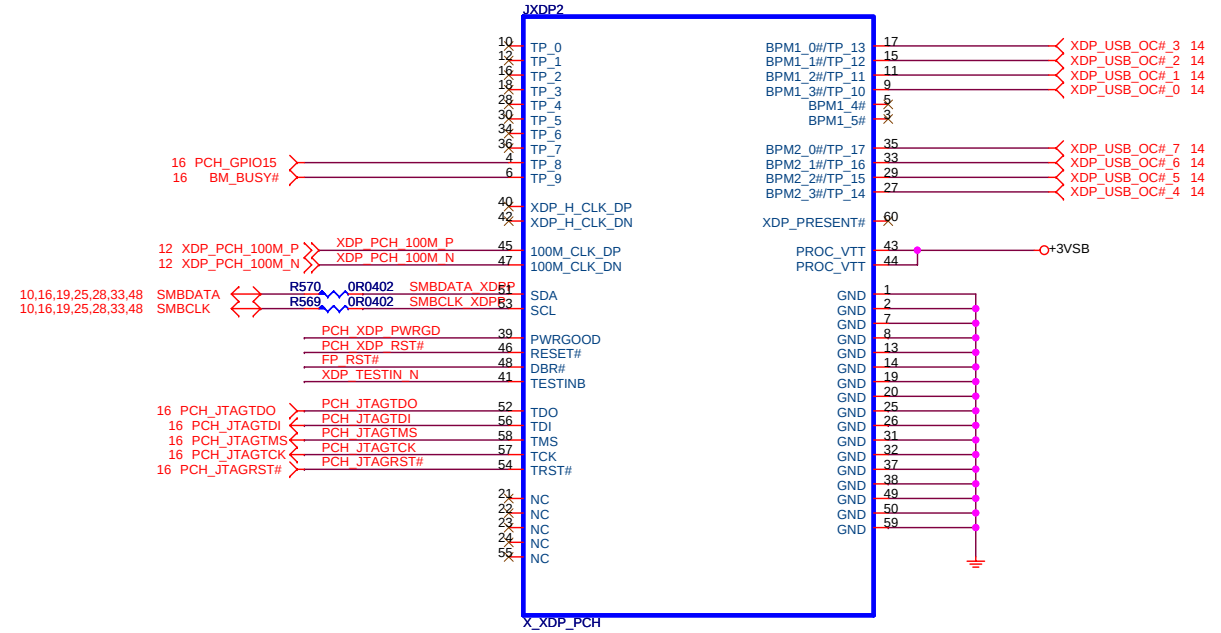


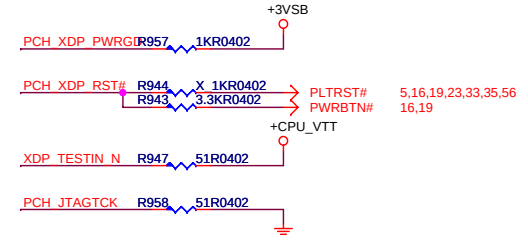


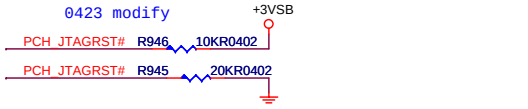


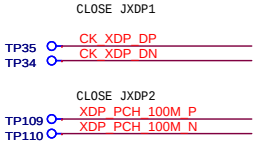
N5C-60F0040-S88

PCH XDP PORT









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MS-7765		
Size: Custom	Document Description: CPU/PCH XDP	Rev: C
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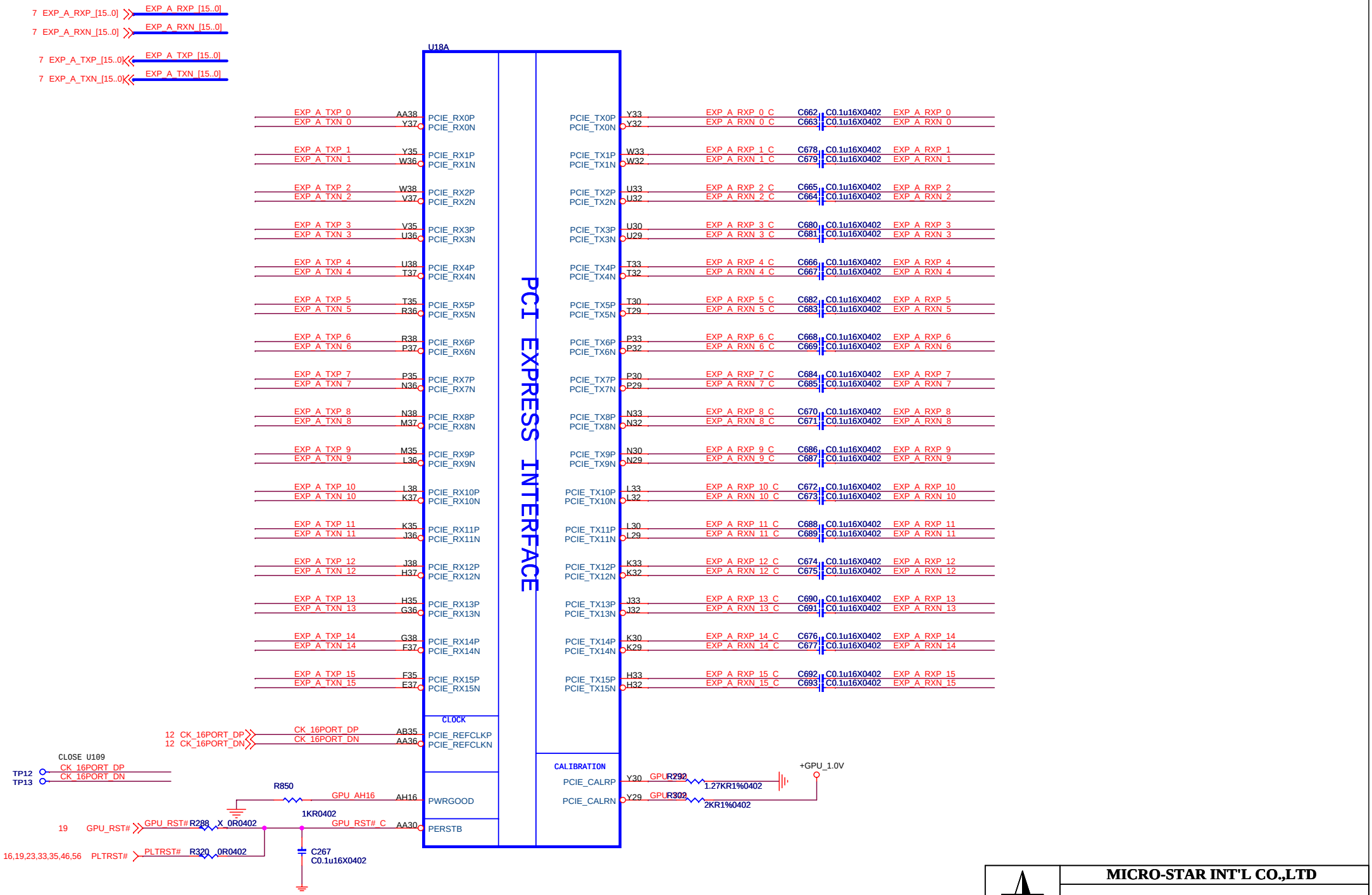
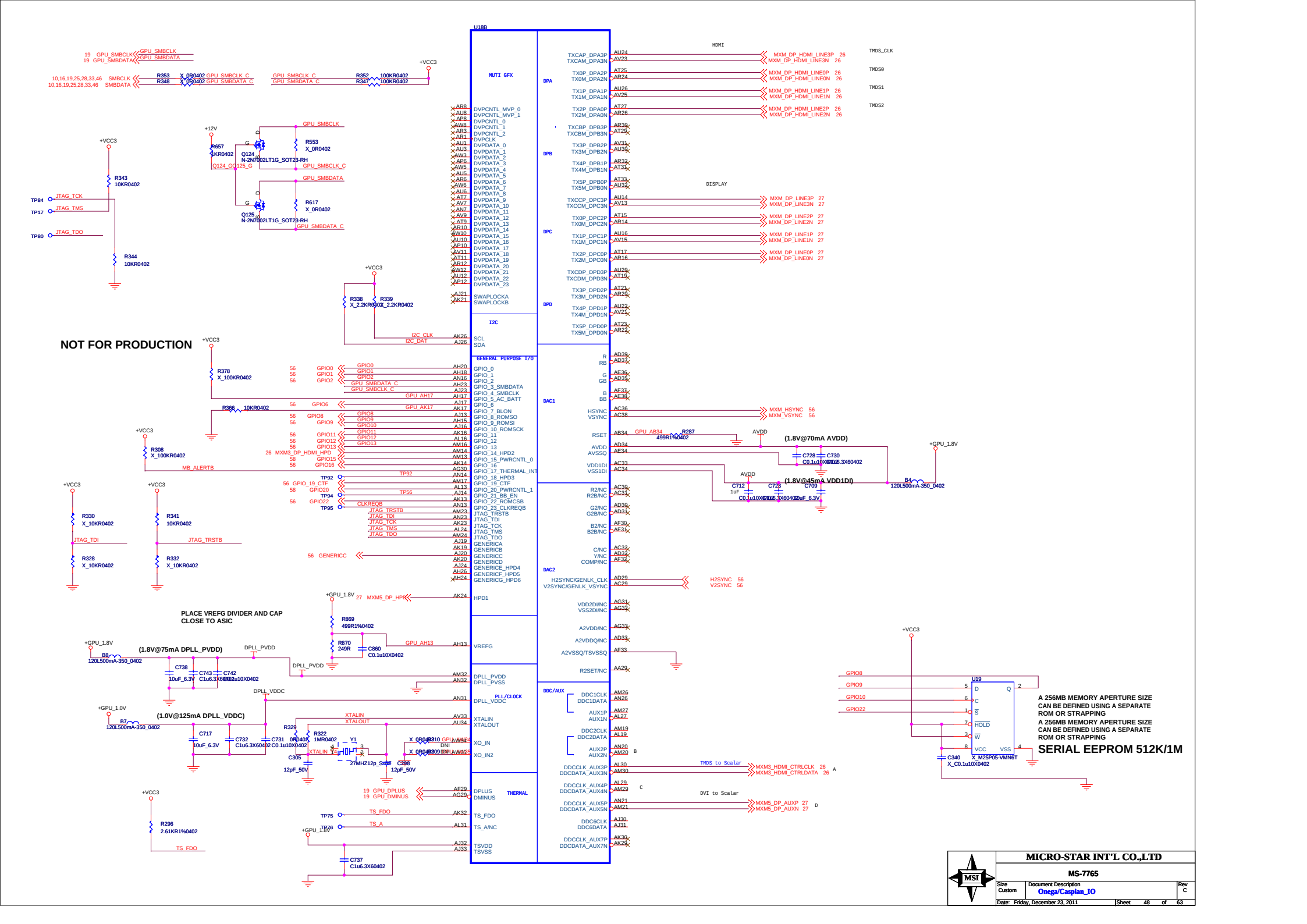


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: Onega/Caspian_PCIE	Rev: C
Date: Wednesday, January 11, 2012	Sheet 47 of 63	


NOT FOR PRODUCTION
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING
A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING
SERIAL EEPROM 512K/1M
(1.8V@70mA AVDD)
(1.8V@45mA VDD1DI)
(1.8V@75mA DPLL_PVDD)
(1.0V@125mA DPLL_VDDC)
MUTI GFX
HDMI
DISPLAY
I2C
GENERAL PURPOSE I/O
PLL/CLOCK
THERMAL
MICRO-STAR INT'L CO.,LTD
MS-7765
Onega/Caspian_IO
Date: Friday, December 23, 2011
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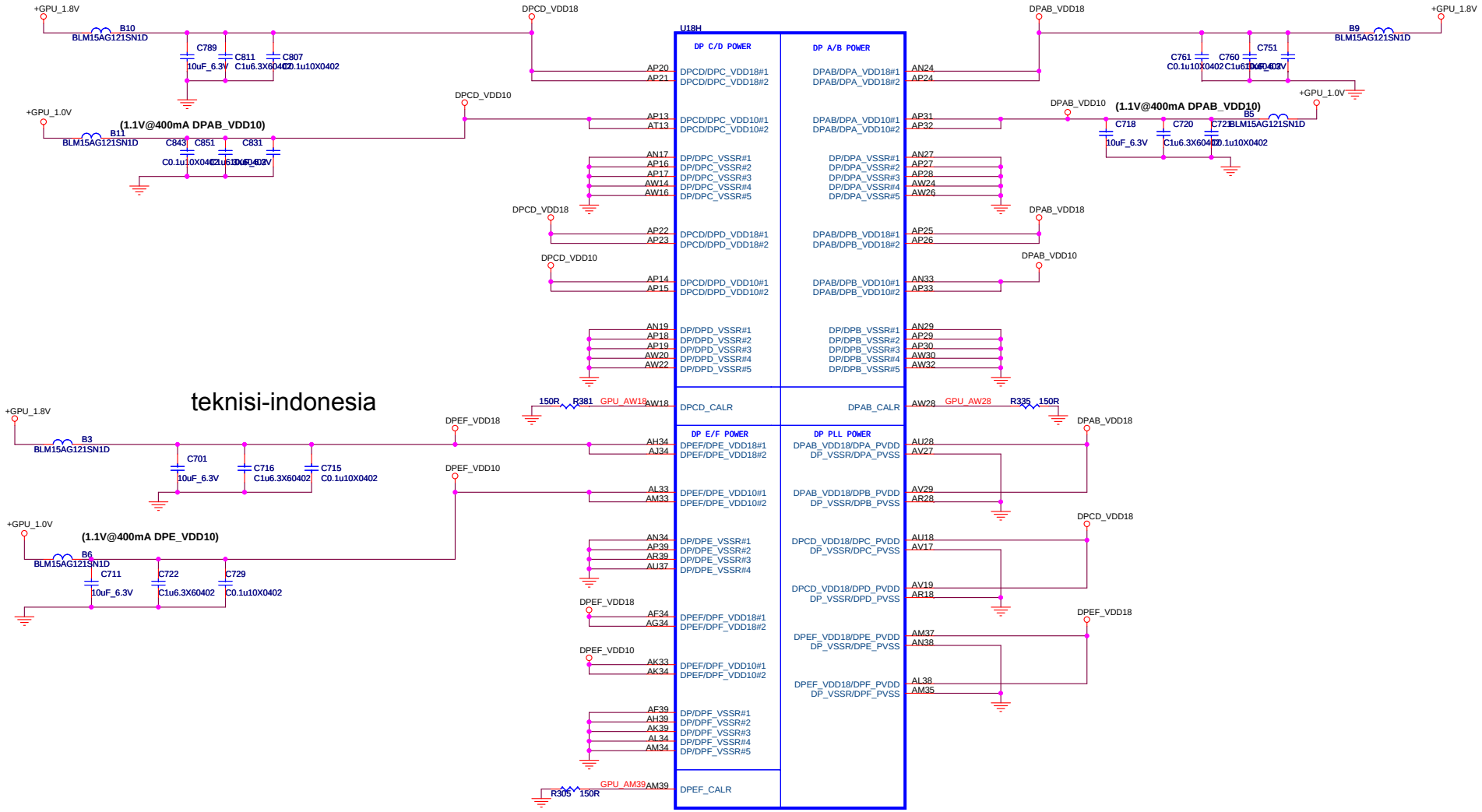

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Size: Custom	Document Description: Onega/Caspian_DP A--D		Rev: C
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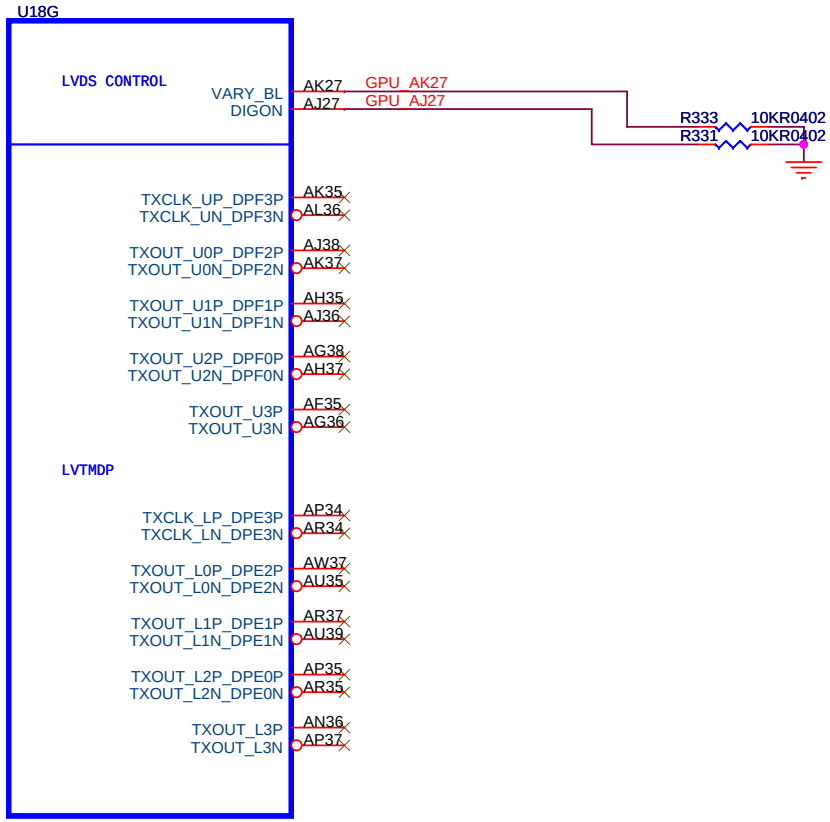
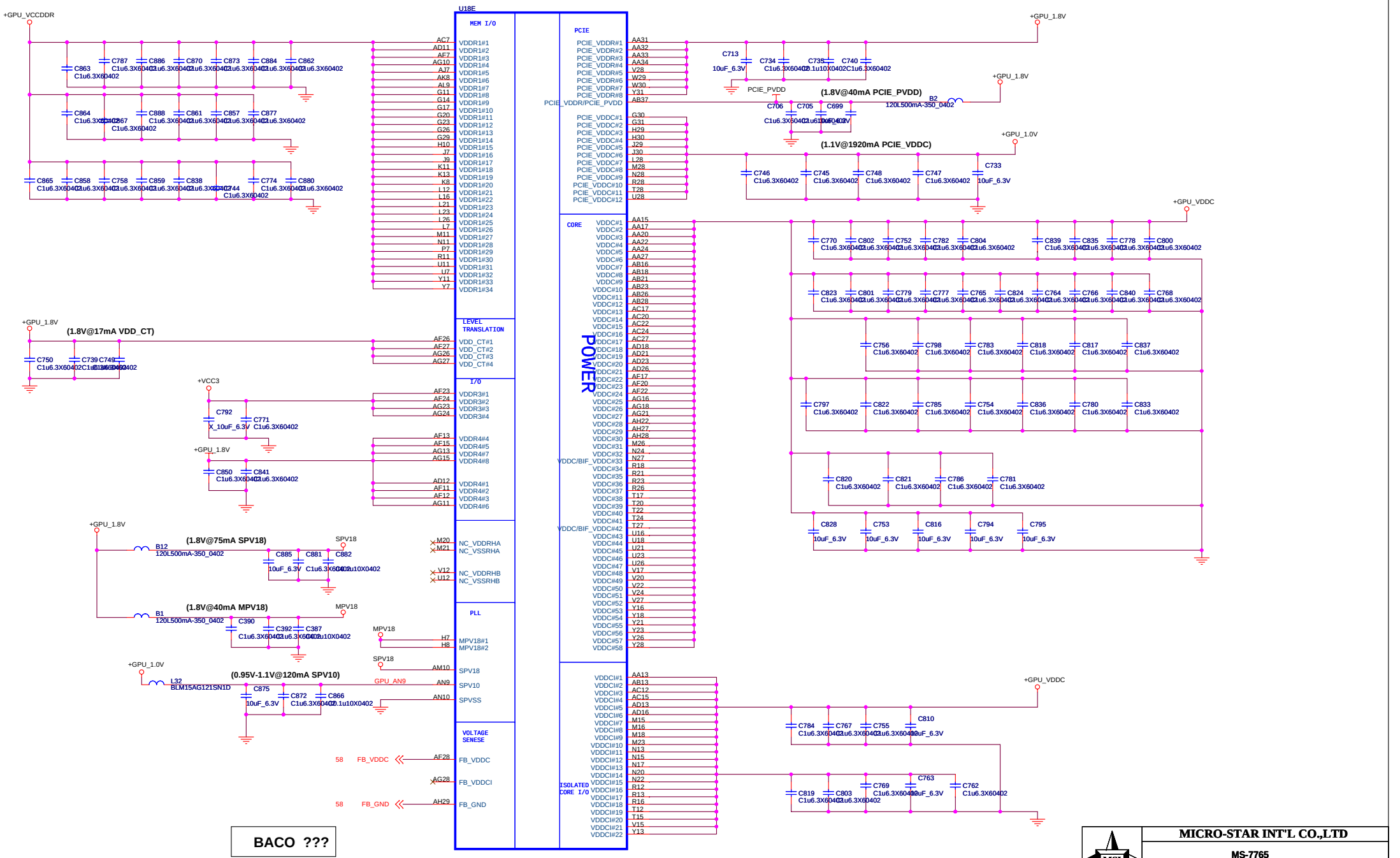
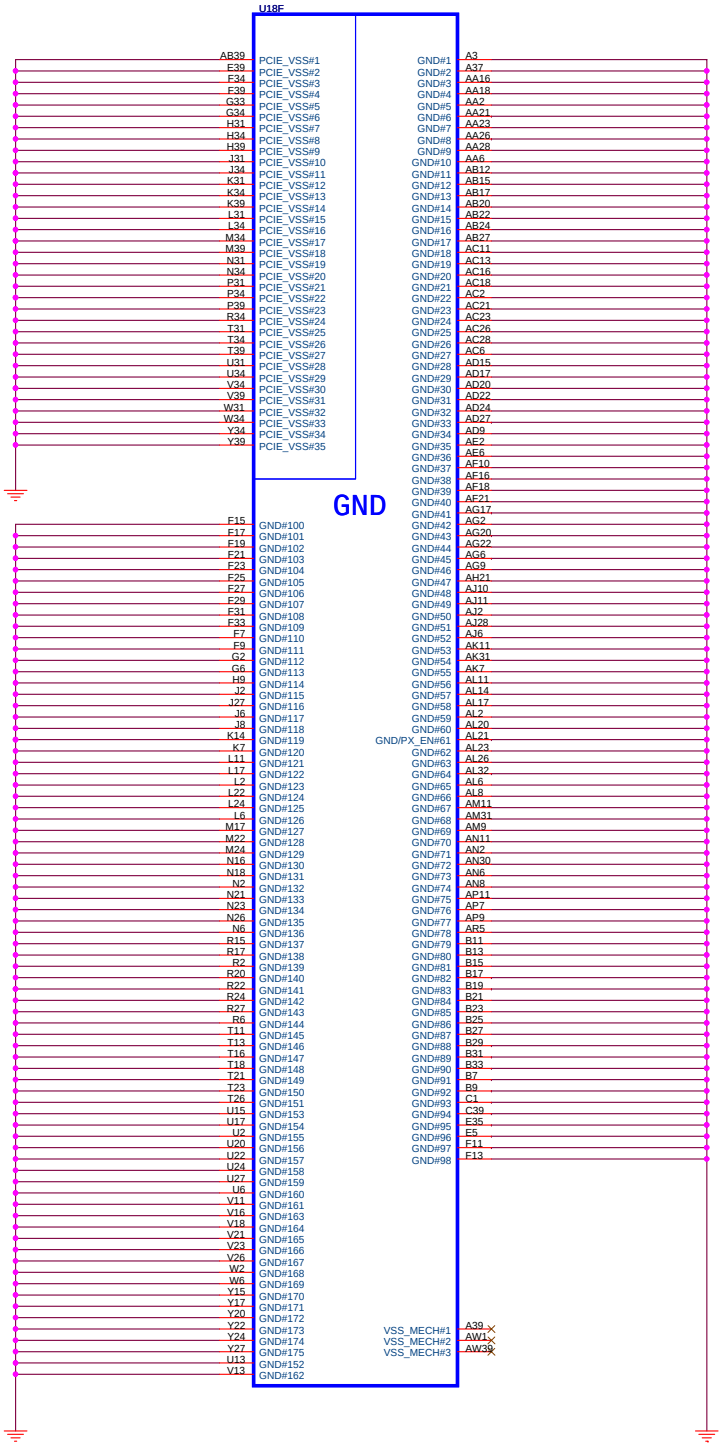


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: Onega/Caspian_LVDS	Rev: C
Date: Friday, December 23, 2011	Sheet 50 of 63	


U18E
MEM I/O
PCIE
CORE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
+GPU_VCCDDR
+GPU_1.8V
+GPU_1.0V
+GPU_VDDC
+VCC3
(1.8V@17mA VDD_CT)
(1.8V@75mA SPV18)
(1.8V@40mA MPV18)
(0.95V-1.1V@120mA SPV10)
(1.8V@40mA PCIE_PVDD)
(1.1V@1920mA PCIE_VDDC)
PCIE_PVDD
PCIE_VDDR/PCIE_PVDD
ISOLATED CORE I/O
VDDC/BIF_VDDC
B1 120L500mA-350_0402
B2 120L500mA-350_0402
B12 120L500mA-350_0402
L32 BLM15AG121SN1D
FB_VDDC
FB_VDDCI
FB_GND
GPU_AN9
BACO ???



MICRO-STAR INT'L CO.,LTD		
MS-7765		
Size: Custom	Document Description: Onega/Caspian_GND	Rev: C
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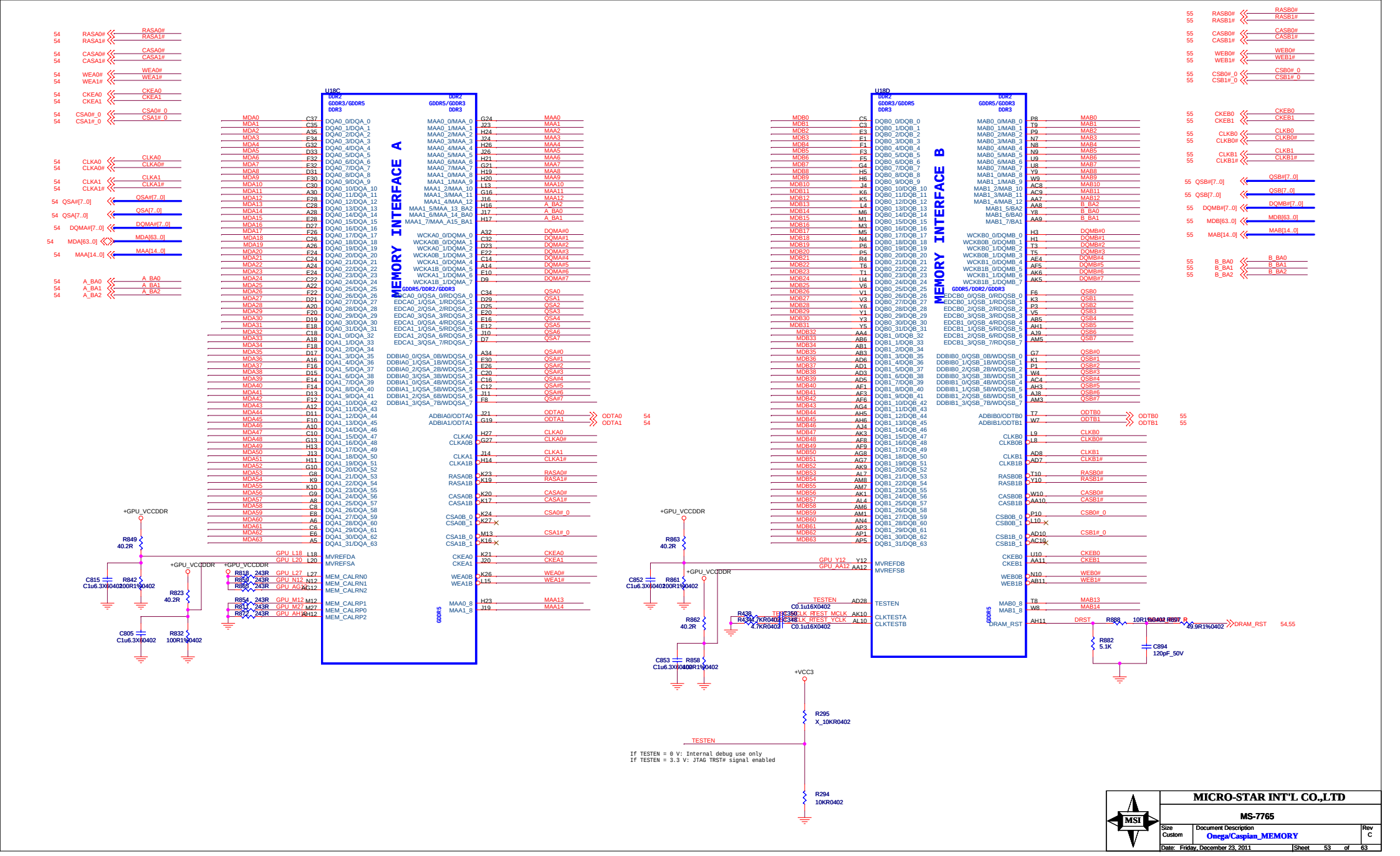
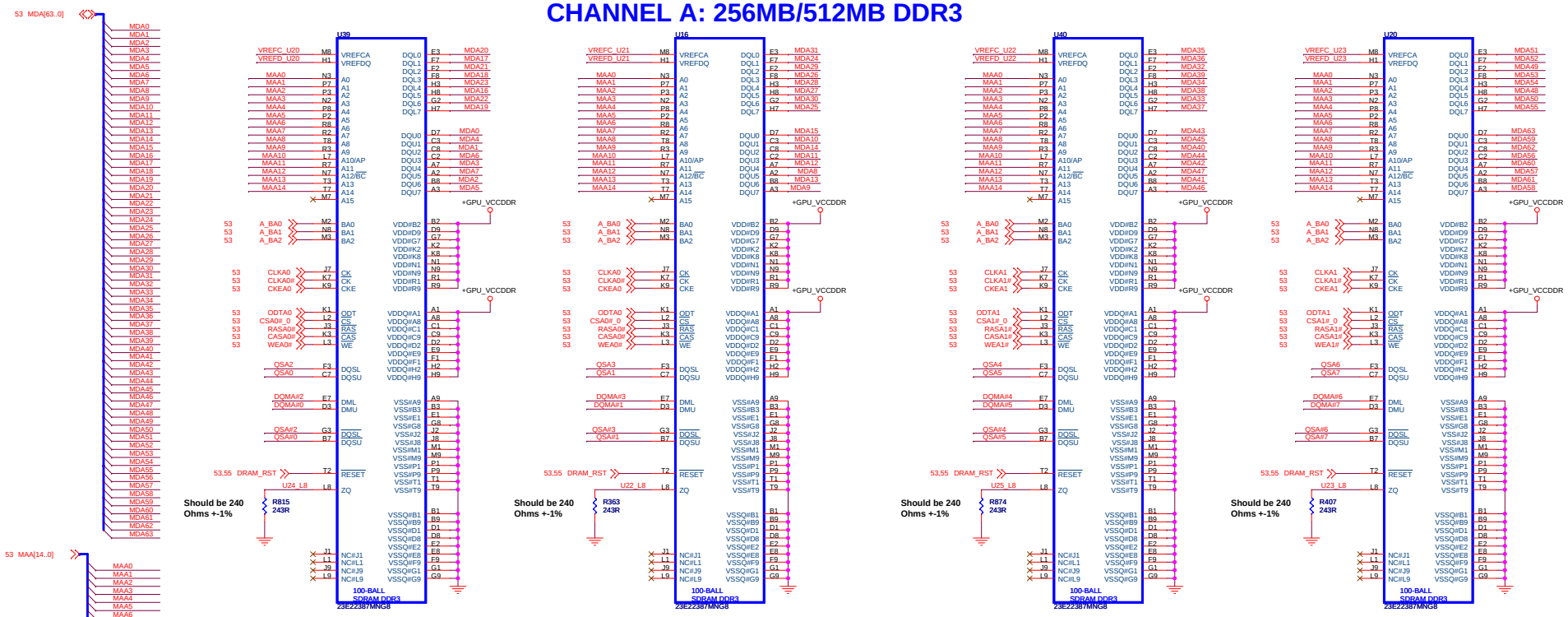
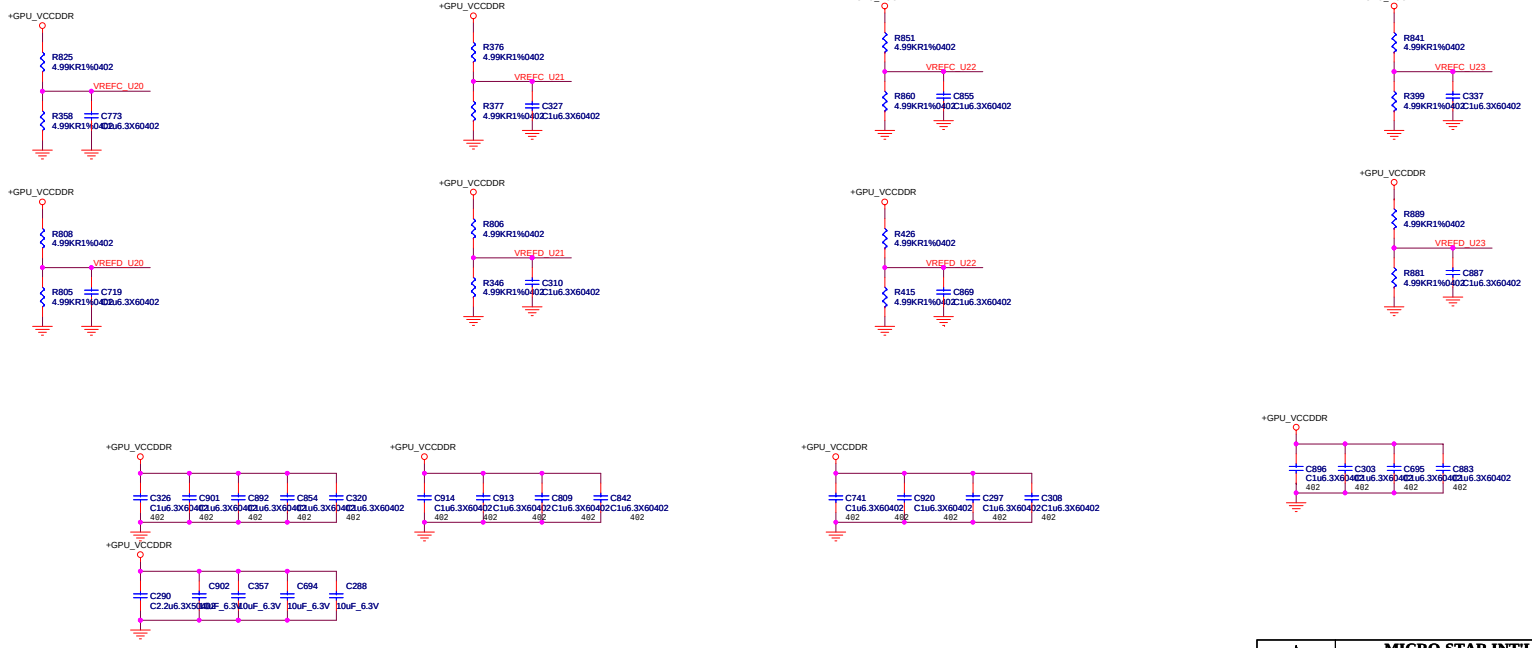
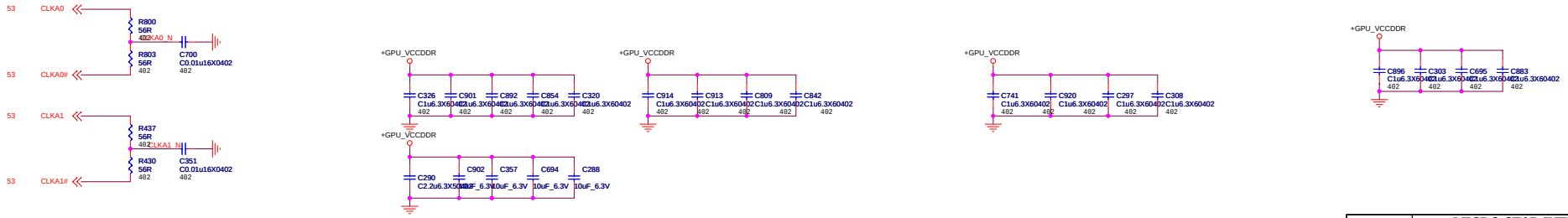


MICRO-STAR INT'L CO.,LTD	
MS-7765	
Size: Custom	Document Description: Onega/Caspian_MEMORY
Rev: C	
Date: Friday, December 23, 2011	Sheet 53 of 63

CHANNEL A: 256MB/512MB DDR3







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MS-7765		
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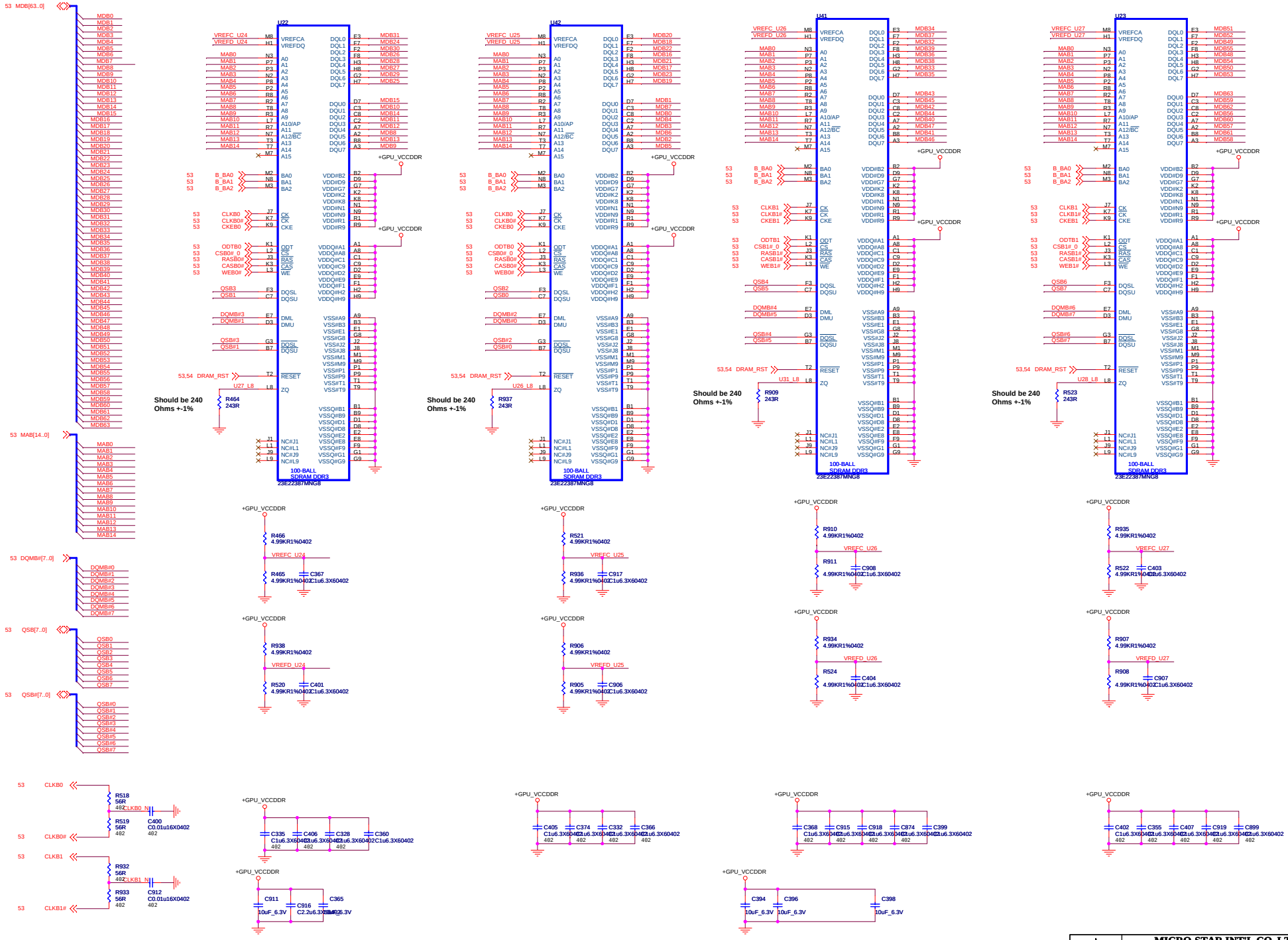
CHANNEL B: 256MB/512MB DDR3



MICRO-STAR INT'L CO.,LTD	
MS-7765	
Size: Custom	Document Description: DDR3 64MX16 B
Rev: C	
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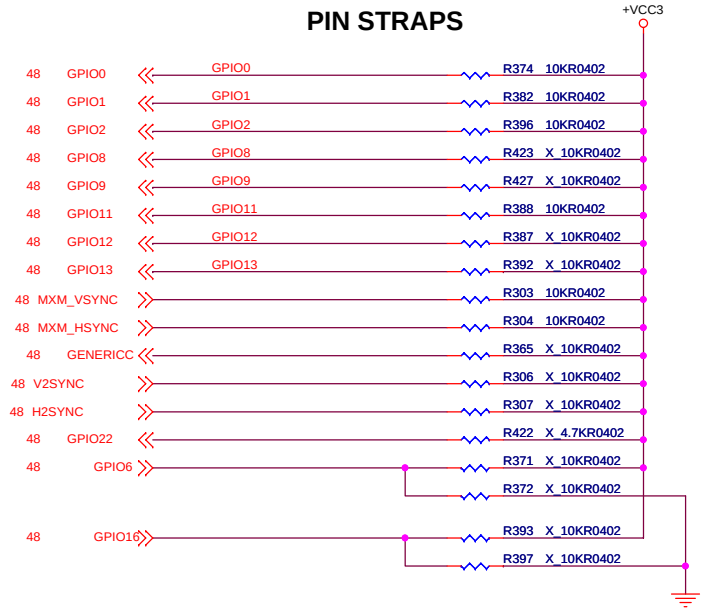
PIN STRAPS



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1
MEMORY CINFIG	[GPIO6,GPIO16]		
HYNIX	[0:1]		
SAMSUNG	[1:0]		

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

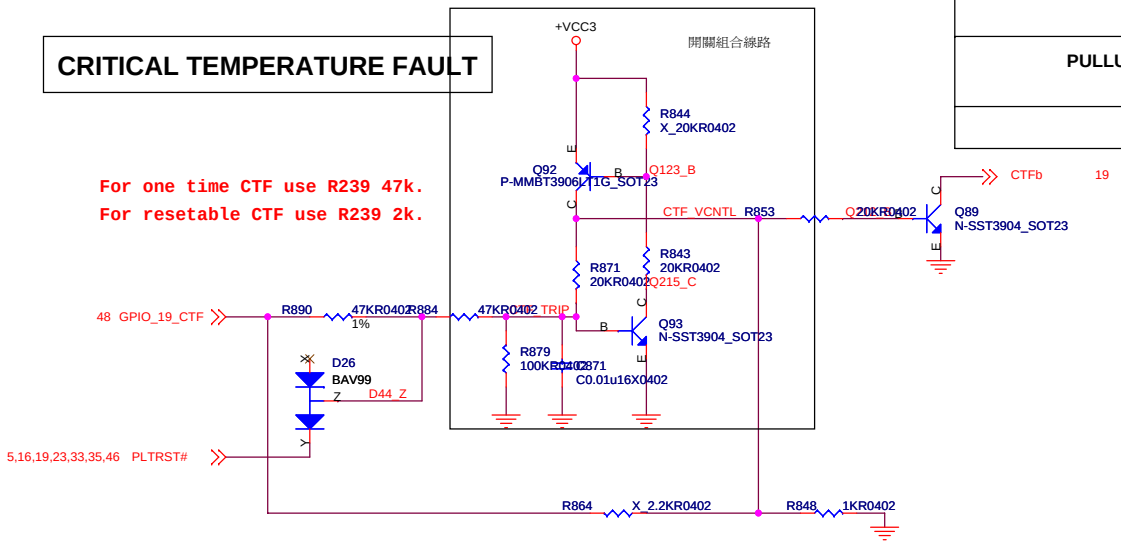
H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN

CRITICAL TEMPERATURE FAULT

For one time CTF use R239 47k.
For resetable CTF use R239 2k.



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	MS-7765		
Size: Custom	Document Description: THERM & STRAPS		Rev: C
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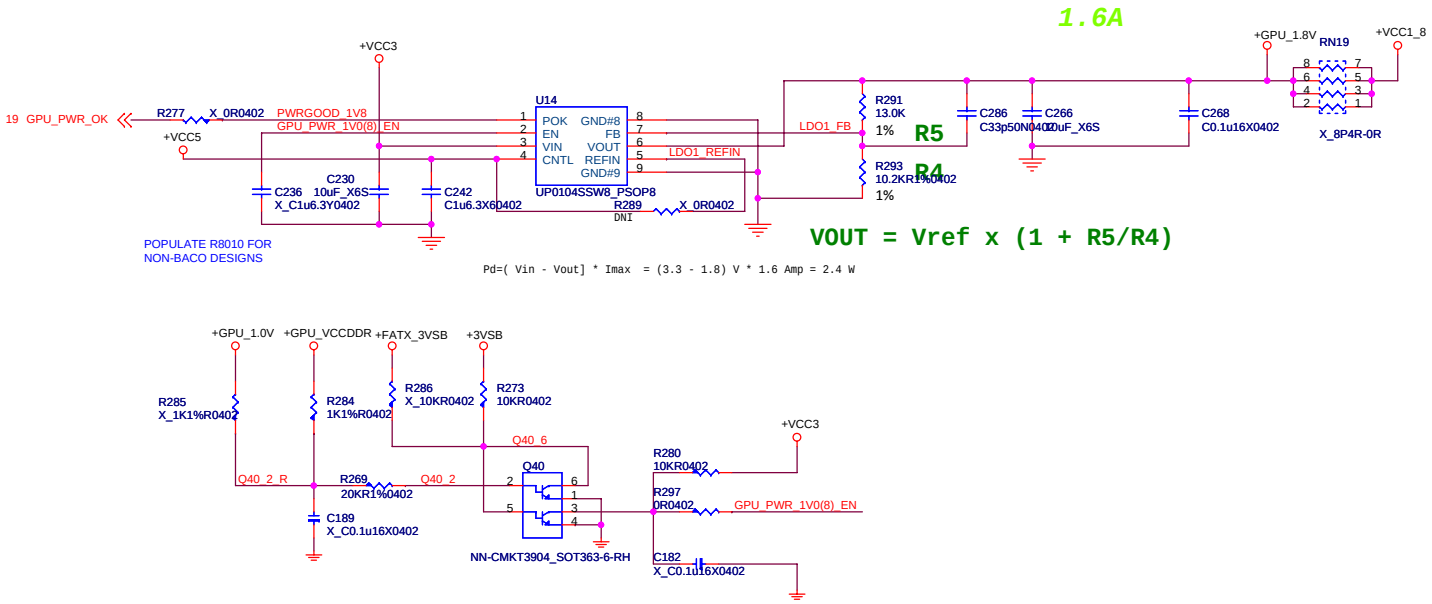
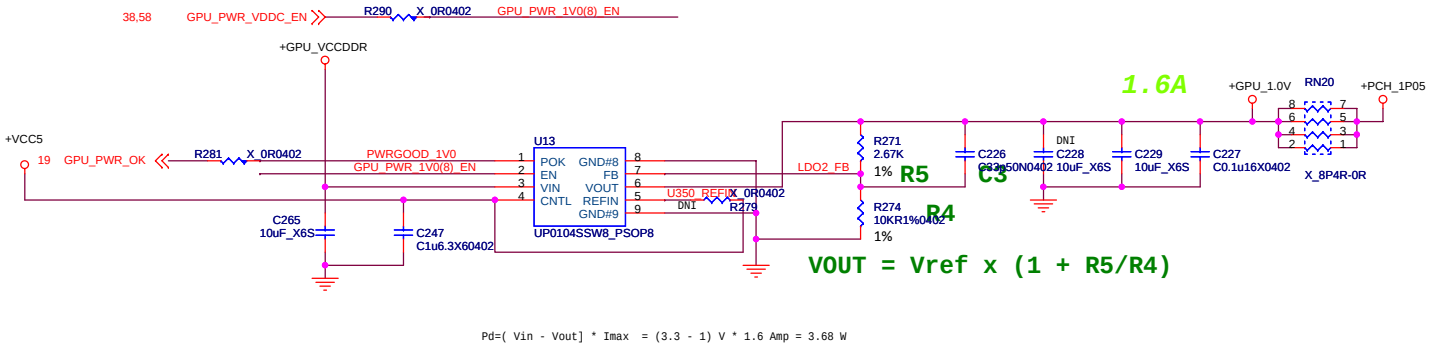
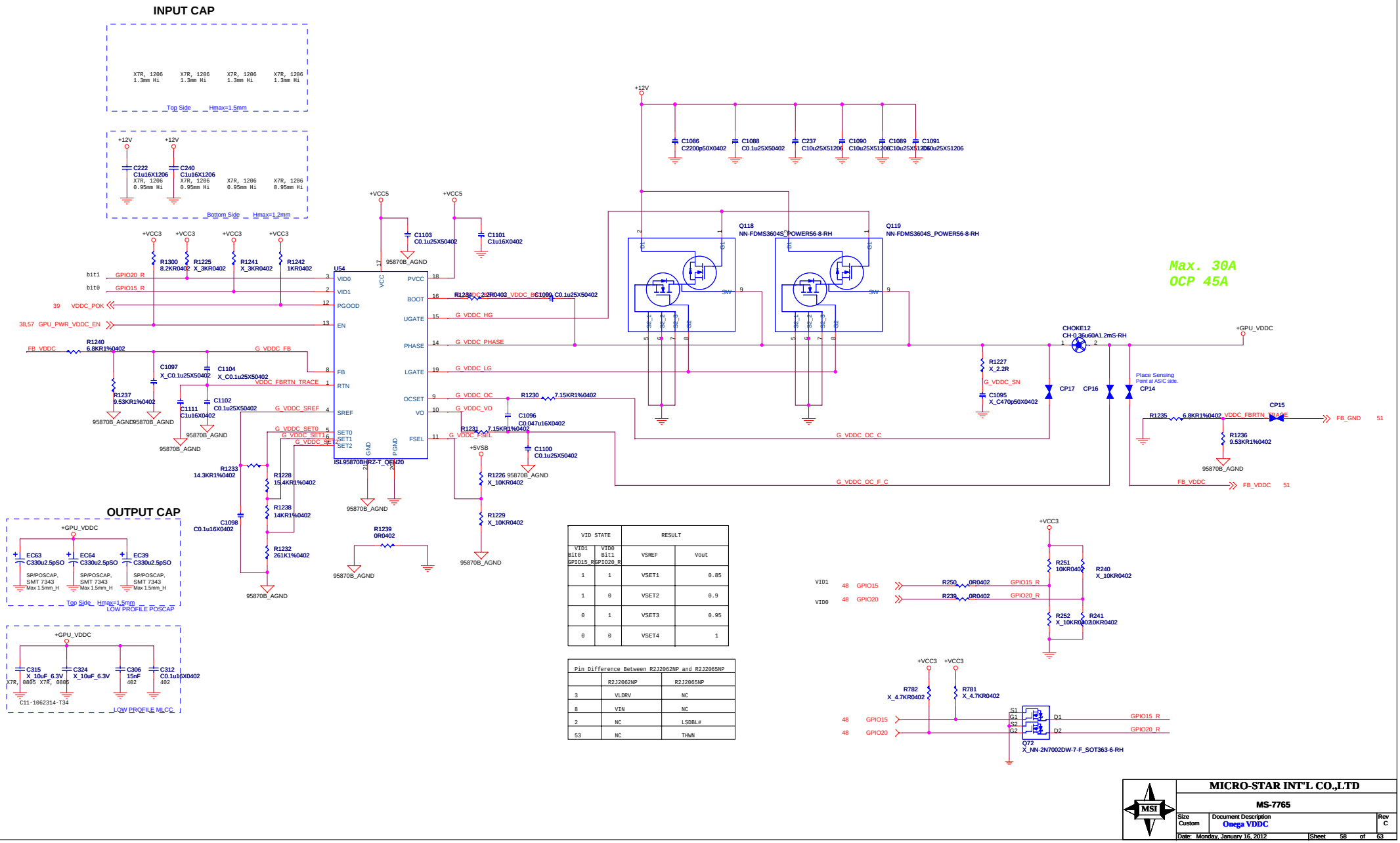
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.0V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
Size: Custom	Document Description: POWER MANAGEMENT&LDO	Rev: C
Date: Monday, January 16, 2012	Sheet 57 of 63	



VID STATE		RESULT	
VID1 Bit0 GPIO15_R	VID0 Bit1 GPIO20_R	VSREF	Vout
1	1	VSET1	0.85
1	0	VSET2	0.9
0	1	VSET3	0.95
0	0	VSET4	1

Pin Difference Between R2J2062NP and R2J2065NP

	R2J2062NP	R2J2065NP
3	VLDRV	NC
8	VIN	NC
2	NC	LSDBL#
53	NC	THWN

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7765	
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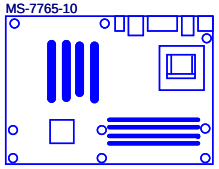
PCB

PCB1
MS-7765-10



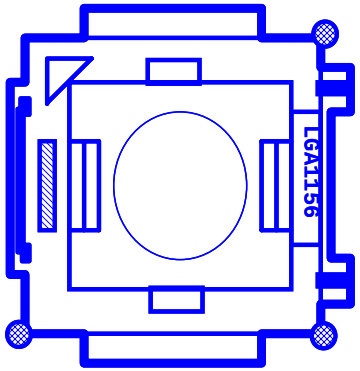
PCB
PN : P30-0776510-G37
AVL : P30-0776510-E48

BAT1_X1

BAT-BCR2032P-RH

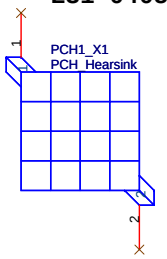
CPU SOCKET

CPU1_X1
CPU SOCKET



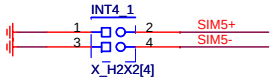
E21-7557060-F02
E21-7557050-L06

E31-0405610-K08 卡勾

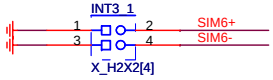


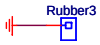
E31-0401634-K08

4/6.5 90 ohm



4/6.5 90 ohm





X_FINGER,BECU

U3_X1_1
U3_X1_2

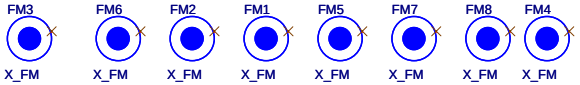
Rubber4
GASKE

Rubber1
Rubber2
X_rubber1/2 X_rubber1/2

Simulation

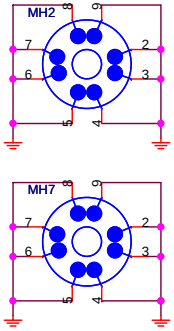
5.5mils 50 ohm

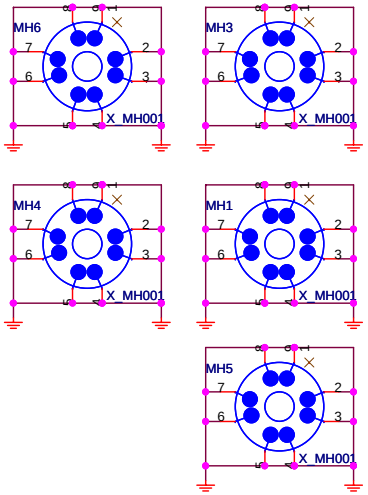
Optical Fiducial Marks-120



Mounting Holes

Modify for factory request.





MHG1
Spacer
Support
X_E2B-1022010-RH

MHG2
Spacer
Support
X_E2B-1022010-RH

MHG4
Spacer
Support
X_E2B-1022010-RH

MHG3
Spacer
Support
X_E2B-1022010-RH

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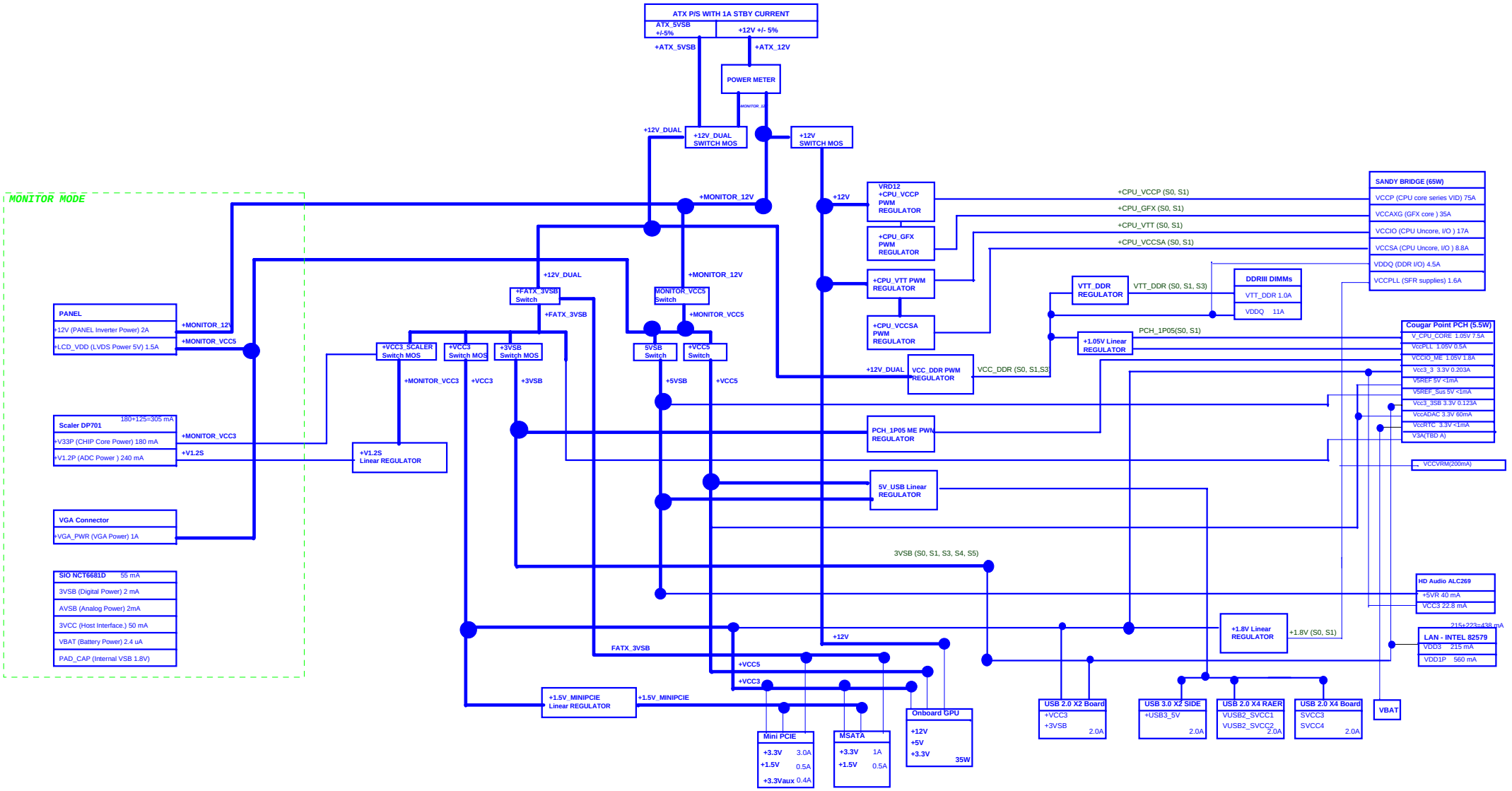
ATX P/S WITH 1A STBY CURRENT
ATX_5VSB +/-5%
+12V +/- 5%
+ATX_5VSB
+ATX_12V
POWER METER
MONITOR_12
+12V_DUAL
+12V_DUAL SWITCH MOS
+12V SWITCH MOS
MONITOR MODE
+MONITOR_12V
+12V
VRD12 +CPU_VCCP PWM REGULATOR
+CPU_GFX PWM REGULATOR
+CPU_VTT PWM REGULATOR
+CPU_VCCSA PWM REGULATOR
+CPU_VCCP (S0, S1)
+CPU_GFX (S0, S1)
+CPU_VTT (S0, S1)
+CPU_VCCSA (S0, S1)
SANDY BRIDGE (65W)
VCCP (CPU core series VID) 75A
VCCAXG (GFX core) 35A
VCCIO (CPU Uncore, I/O) 17A
VCCSA (CPU Uncore, I/O) 8.8A
VDDQ (DDR I/O) 4.5A
VCCPLL (SFR supplies) 1.6A
VTT_DDR REGULATOR
VTT_DDR (S0, S1, S3)
DDRIII DIMMs
VTT_DDR 1.0A
VDDQ 11A
+1.05V Linear REGULATOR
PCH_1P05(S0, S1)
Cougar Point PCH (5.5W)
V_CPU_CORE 1.05V 7.5A
VccPLL 1.05V 0.5A
VCCIO_ME 1.05V 1.8A
Vcc3_3 3.3V 0.203A
V5REF 5V <1mA
V5REF_Sus 5V <1mA
Vcc3_3SB 3.3V 0.123A
VccADAC 3.3V 60mA
VccRTC 3.3V <1mA
V3A(TBD A)
VCCVRM(200mA)
+12V_DUAL
VCC_DDR PWM REGULATOR
VCC_DDR (S0, S1,S3)
PANEL
+12V (PANEL Inverter Power) 2A
+LCD_VDD (LVDS Power 5V) 1.5A
+MONITOR_12V
+MONITOR_VCC5
+FATX_3VSB Switch
MONITOR_VCC5 Switch
+FATX_3VSB
+MONITOR_VCC5
+VCC3_SCALER Switch MOS
+VCC3 Switch MOS
+3VSB Switch MOS
5VSB Switch
+VCC5 Switch
+MONITOR_VCC3
+VCC3
+3VSB
+5VSB
+VCC5
Scaler DP701
180+125=305 mA
+V33P (CHIP Core Power) 180 mA
+V1.2P (ADC Power) 240 mA
+MONITOR_VCC3
+V1.2S
+V1.2S Linear REGULATOR
PCH_1P05 ME PWR REGULATOR
5V_USB Linear REGULATOR
VGA Connector
+VGA_PWR (VGA Power) 1A
SIO NCT6681D 55 mA
3VSB (Digital Power) 2 mA
AVSB (Analog Power) 2mA
3VCC (Host Interface.) 50 mA
VBAT (Battery Power) 2.4 uA
PAD_CAP (Internal VSB 1.8V)
3VSB (S0, S1, S3, S4, S5)
HD Audio ALC269
+5VR 40 mA
VCC3 22.8 mA
215+223=438 mA
LAN - INTEL 82579
VDD3 215 mA
VDD1P 560 mA
+1.8V Linear REGULATOR
+1.8V (S0, S1)
FATX_3VSB
+12V
+VCC5
+VCC3
+1.5V_MINIPCIE Linear REGULATOR
+1.5V_MINIPCIE
Mini PCIE
+3.3V 3.0A
+1.5V 0.5A
+3.3Vaux 0.4A
MSATA
+3.3V 1A
+1.5V 0.5A
Onboard GPU
+12V
+5V
+3.3V
35W
USB 2.0 X2 Board
+VCC3
+3VSB
2.0A
USB 3.0 X2 SIDE
+USB3_5V
2.0A
USB 2.0 X4 RAER
VUSB2_SVCC1
VUSB2_SVCC2
2.0A
USB 2.0 X4 Board
SVCC3
SVCC4
2.0A
VBAT
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PS_ON#

PC Mode

SLP_S5#

SLP_S3#

12V

5V

3.3V

MONI_ON

CPU_VTT

VCC_1_8REF

PCH_1_8

VCC_SA

VCC_DDR

PCH_Core(1.05V)

PWROK

CPU_SVID

CPU_VCCP

VRM_PWG

SYS_PWTOK

PL_RST

PCI_RST

PS_ON# OR
MONI_PSON

Monitor Mode

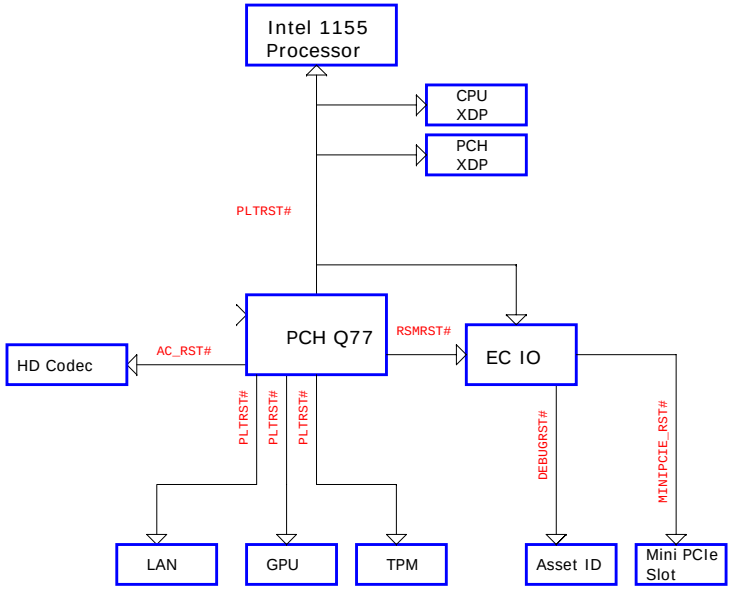
12V

5V

3.3V

MONI_ON

RESET MAP



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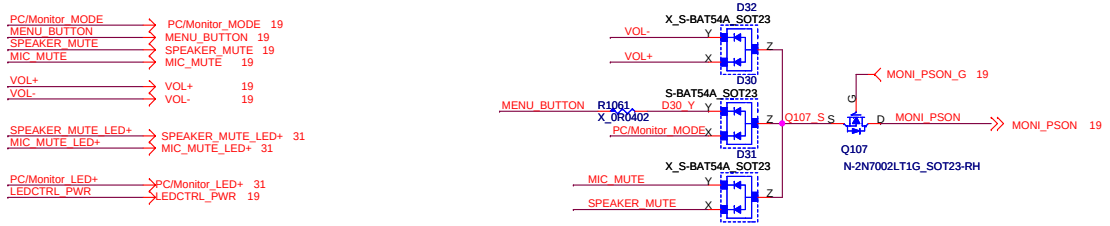
PC/Monitor_MODE
MENU_BUTTON
SPEAKER_MUTE
MIC_MUTE

VOL+
VOL-

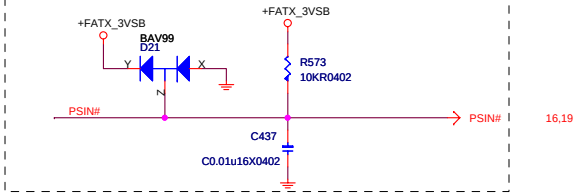
SPEAKER_MUTE_LED+
MIC_MUTE_LED+

PC/Monitor_LED+
LEDCTRL_PWR

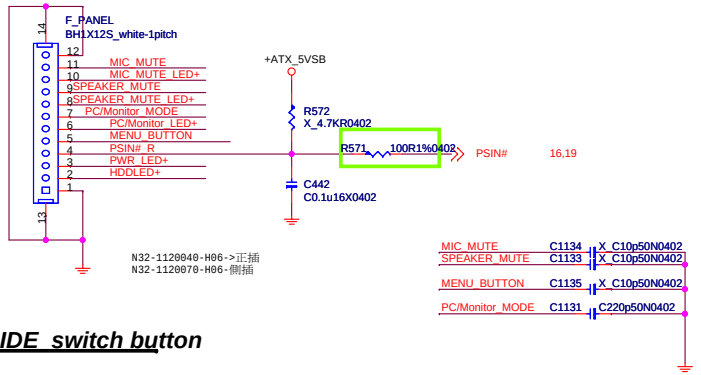


Button	Function	PST	LED		Initial Default	Power on default
			On	Off		
F1	Mic Mute OSD Exit	Front	Mute	Un-mute	Un-mute	Last status
F2	Speaker Mute OSD Left	Front	Mute	Un-mute	Un-mute	Last status
F3	PC Monitor OSD Right	Front	Monitor	PC	PC	PC
F4	Menu Enter	Front				
F5	Power Button	Front	On	Off		
S1	Volume Up	Side				
S2	Volume Down	Side				

POWER BUTTON

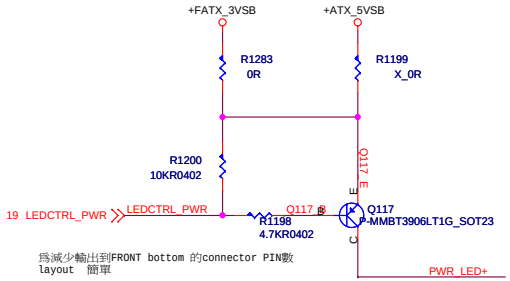


Front switch button

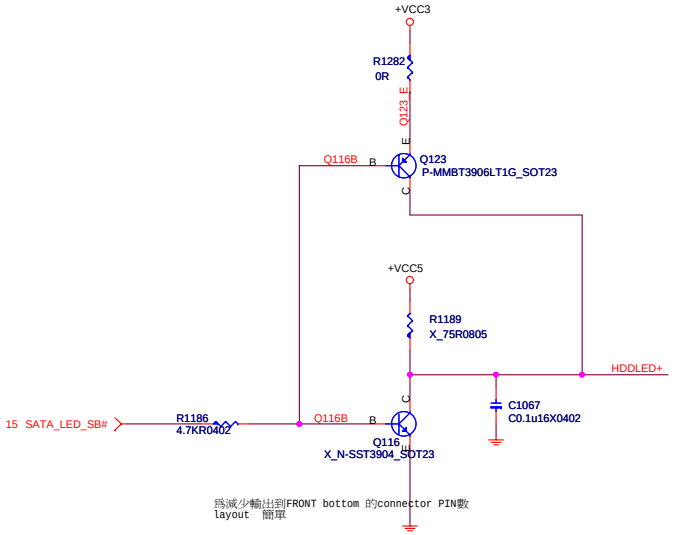


SIDE switch button

Power LED



HDD LED



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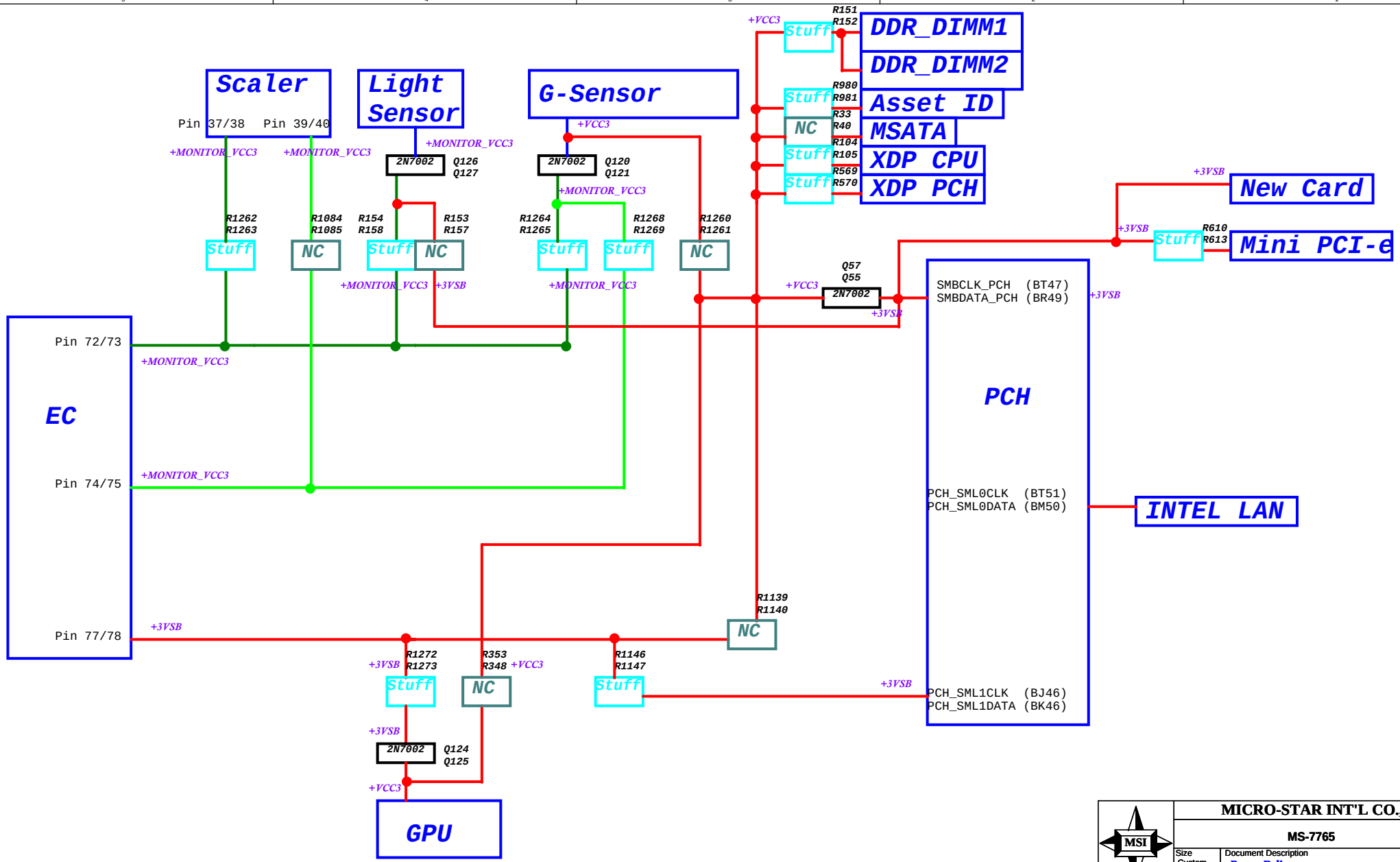

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