Moonknight N/V/L 13" Schematics
Tiger Lake UP3 (28W)

2020-12-10
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*

Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	A00

Date: Friday, January 29, 2021 Sheet 1 of 106

Project code : XXXXXXXXXXXX
MB PCB P/N : XXXXX
MB Revision : SA
DB PCB P/N : XXXXX
DB Revision : SA

Moonknight N/V/L 13" TGL Block Diagram

Moonknight-N/V 13"

VRAM(GDDR6) *2
2GB
81-82

GDDR5

GPU X7901
NVIDIA
N18S-G5 25W
76-80

PCIE4 x 4

eDP 13" Panel
FHD / FHD+ / QHD+
55

eDPx4

LCD1

DDI-A 4-lane

HDMI 1.4
57

DDI 4-lane

M.2 2280
63

PCIEx4

SATAx1

Intel CPU
Tiger LAKE-U 4+2
1449 Pin
PCH-LP

4 TCSS Lanes
12 PCIe*3.0 Lanes (SATA*2, USB31*4)
1 PCIE4.0x4 Lanes
10 USB2.0
CNVi2.0
ESPI / SPI
HDA/SNDW
CSI
(Remove SD/EMMC)

X1801
X1802

3,4,5,6,7,8,9,10,11,15
16,17,18,19,20,21,22,23

LPDDR4x Channel A
NON-INTERLEAVE MODE
LPDDR4x Channel B

MD x32
Type-3: 4266 4/8/16GB/32GB
12

MD x32
Type-3: 4266 4/8/16GB/32GB
13

Moonknight-N/V 13"

Moonknight-N/V 13"

USB BD

USB-A port1
35

USB3.0

USB 3.1
re-Driver
35

USB3.0

USB2.0

USB-A port2
35

USB3.0

USB 3.1
re-Driver
35

USB3.0

USB2.0

microSD Card
SD3.0
33

Card Reader
Realtek
RTS5144
33

USB2.0

AUD Jack

Moonknight-L 13"

(2W, 4ohm)
2CH Speaker

Audio Codec
RealTek ALC3204
27

HDA

I2C

Camera module
on Panel side

Internal Digital MIC

Camera
55

I2C

USB2.0

TCP0

TBT RETIMER
INTEL
Burnside BRIDGE
71

SPI

TX+/-, RX+/- x 2

I2C

CLK

XTL
X7101

USB2.0

TYPEC PD controller
CCG6
72

CC control pin

Type-C Port1
Option1: TBT/USB4/ DP/PD
Option2: /USB4/ DP/PD
73

Flash ROM

USB2.0

CC control pin

Type-C Port2
Option1: TBT/USB4/ DP/PD
Option2: /USB4/ DP/PD
73

I2C

CLK

XTL
X7501

TCP1

TBT RETIMER
INTEL
Burnside BRIDGE
75

TX+/-, RX+/- x 2

SPI

Moonknight-N/V 13"

CNVi/PCIE x 1

M.2 E KEY WLAN
61

ISH I2C

3 Axis Accelerometer
ST LIS2DW12TR
70

eSPI BUS

eSPI debug port
68

SPI

KBC
MICROCHIP
MEC1515
X2401
24

SMBUS

Thermal
NUVOTON
NCT7718W
26

Fan Control
PWM
26

FAN

Fan Control
PWM
26

FAN

I2C

Flash ROM 32MB
MX25L25673GM2I-08G
25

TPM
NPCT750JADYX
91

Touch PAD
Image sensor

Int.
KB

Moonknight-V/L 13"

I2C

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
Custom	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 2 of 106

SSID = CPU

24	PECI_CPU	
15	DBG_PMODE	
22,24,44,46,72	PROCHOT#_CPU	
24,65	TOUCH_PAD_INTR#	
21	SDRAM_ID4	

20201011
Delete reserve R309

1D05V_VCCSTG
R301 1 1KR2F-3-GP EAR_N_TEST_NCTF

1D05V_VCCSTG_TERM
R302 1 1KR2F-3-GP PROCHOT#_CPU

1D05V_VCCST
R304 1 1KR2F-3-GP THERMTRIP#_CPU
R307 1 1KR2F-3-GP CPU_CATERR

CPU_POPI_RCOMP R305 1 49D9R2F-GP
PCH_OPI_RCOMP R306 1 49D9R2F-GP

1D05V_VCCSTG_TERM
20200724
R311 Change to 100R.
R311 1 100R2J-2-GP XDP_TDO_CPU
R308 1 DY 51R2J-2-GP XDP_PREQ#
R313 1 XDP 51R2J-2-GP XDP_TDI
R314 1 XDP 51R2J-2-GP XDP_TMS
XDP_TCLK R310 1 XDP 51R2J-2-GP
XDP_TRST# R312 1 DY 51R2J-2-GP

PROCHOT#_CPU R303 1 499R2F-GP

CPU1U 21 OF 21

CPU_CATERR	M7	CATERR#	
PECI_CPU	BK9	PECI	
PROCHOT#_CPU_R	E2	PROCHOT#	
THERMTRIP#_CPU	M5	THRMTRIP#	
CPU_POPI_RCOMP	CT39	PROC_POPIRCOMP	
PCH_OPI_RCOMP	CB9	PCH_OPIRCOMP	
	CW12	TP#CW12	
	CM39	TP#CM39	
DBG_PMODE	DF4	DBG_PMODE	
	DB42	GPP_B4/CPU_GP3	
TOUCH_PAD_INTR#	DB41	GPP_B3/CPU_GP2	
	DF8	GPP_E7/CPU_GP1	
	DU5	GPP_E3/CPU_GP0	
	DF31	GPP_H2	
	DV32	GPP_H1	
	DW32	GPP_H0	
SDRAM_ID4	DJ27	GPP_H19/TIME_SYNC0	

TGL-U-GP-U1

PROC_TRST#	K4	XDP_TRST#	TP309
PROC_TMS	B9	XDP_TMS	TP310
PROC_TDO	D12	XDP_TDO_CPU	TP311
PROC_TDI	A12	XDP_TDI	TP312
PROC_TCK	B6	XDP_TCLK	TP313
PCH_JTAGX	D8		
PCH_TMS	A9		
PCH_TDO	E12		
PCH_TDI	B12		
PCH_TCK	A7	PCH_TCK	TP314
PCH_TRST#	H4		
PROC_PREQ#	C11	XDP_PREQ#	
PROC_PRDY#	D11	XDP_PRDY#	TP302
EAR_N_TEST_NCTF	G1	EAR_N_TEST_NCTF	
GPP_F7	DT15		
GPP_F9	DR15		
GPP_F10	DT14		

XDP

20200722
GC6_GC6_EVENT# Reserve TP.

<Core Design>

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Title	CPU (THML/JTAG)	
Size A3	Document Number MOONKNIGHT_NVL_TGL	Rev X02
Date: Friday, January 29, 2021	Sheet 3 of 106	

SSID = CPU

eDP

55	eDP_TX_CPU_N0
55	eDP_TX_CPU_P0
55	eDP_TX_CPU_N1
55	eDP_TX_CPU_P1
55	eDP_TX_CPU_N2
55	eDP_TX_CPU_P2
55	eDP_TX_CPU_N3
55	eDP_TX_CPU_P3
55	eDP_AUX_CPU_N
55	eDP_AUX_CPU_P
55	EDP_HPD
24	L_BKLT_EN
55	eDP_VDD_EN
55	L_BKLT_CTRL

HDMI

57	HDMI_DDI_TX_P3
57	HDMI_DDI_TX_N3
57	HDMI_DDI_TX_P0
57	HDMI_DDI_TX_N0
57	HDMI_DDI_TX_P1
57	HDMI_DDI_TX_N1
57	HDMI_DDI_TX_P2
57	HDMI_DDI_TX_N2
57	CPU_DPB_CTRL_CLK
57	CPU_DPB_CTRL_DATA
57	CPU_DISP_HPDB

TBT

71	USB1_TCSS_TX_N0
71	USB1_TCSS_TX_P0
71	USB1_TCSS_TX_N1
71	USB1_TCSS_TX_P1
71	USB1_TCSS_RX_N0
71	USB1_TCSS_RX_P0
71	USB1_TCSS_RX_N1
71	USB1_TCSS_RX_P1
71	USB1_TCSS_AUX_N
71	USB1_TCSS_AUX_P
75	TBT_LSX0_TXD
15,75	TBT_LSX0_RXD

TBT2

75	USB2_TCSS_TX_N0
75	USB2_TCSS_TX_P0
75	USB2_TCSS_TX_N1
75	USB2_TCSS_TX_P1
75	USB2_TCSS_RX_N0
75	USB2_TCSS_RX_P0
75	USB2_TCSS_RX_N1
75	USB2_TCSS_RX_P1
75	USB2_TCSS_AUX_N
75	USB2_TCSS_AUX_P
71	TBT_LSX1_TXD
15,71	TBT_LSX1_RXD

Other

15	GPP_D12
15	GPP_D10
65	KB_DET#

3D3V_S0

20200813
ADD RN401 PU 3D3V_S0

RN401
SRN2K2J-1-GP
CPU_DPB_CTRL_CLK
CPU_DPB_CTRL_DATA

3D3V_S0

R406
10KR2J-3-GP
KB_DET#

20200717
ADD R406 10K PU 3D3V_S0 FOR KB_DET
Follow Shuri Nakia0715.

R404 DY 100KR2J-1-GP CPU_DISP_HPD1

3D3V_S5_VCCPRIM

R403 10KR2J-3-GP USB_OC1#
R405 10KR2J-3-GP USB_OC2#

3D3V_S5_VCCPRIM

CPU1A — 1 OF 21

eDP_TX_CPU_P3	AC2	DDIA_TXP3	eDP
eDP_TX_CPU_N3	AC1	DDIA_TXN3	
eDP_TX_CPU_P2	AD2	DDIA_TXP2	
eDP_TX_CPU_N2	AD1	DDIA_TXN2	
eDP_TX_CPU_P1	AF1	DDIA_TXP1	
eDP_TX_CPU_N1	AF2	DDIA_TXN1	
eDP_TX_CPU_P0	AG2	DDIA_TXP0	
eDP_TX_CPU_N0	AG1	DDIA_TXN0	
eDP_AUX_CPU_P	AJ2	DDIA_AUX_P	
eDP_AUX_CPU_N	AJ1	DDIA_AUX_N	
	DN4	GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD	
	DT6	GPP_E23/DDPA_CTRLDATA	
EDP_HPD	DR5	GPP_E14/DDSP_HPDA/DISP_MISCA	eDP
HDMI_DDI_TX_P3	T12	DDIB_TXP3	HDMI
HDMI_DDI_TX_N3	T11	DDIB_TXN3	
HDMI_DDI_TX_P0	Y11	DDIB_TXP2	
HDMI_DDI_TX_N0	Y9	DDIB_TXN2	
HDMI_DDI_TX_P1	T9	DDIB_TXP1	
HDMI_DDI_TX_N1	P9	DDIB_TXN1	
HDMI_DDI_TX_P2	V11	DDIB_TXP0	
HDMI_DDI_TX_N2	V9	DDIB_TXN0	
	AB9	DDIB_AUX_P	
	AD9	DDIB_AUX_N	
CPU_DPB_CTRL_CLK	DM29	GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN	
CPU_DPB_CTRL_DATA	DK27	GPP_H17/DDPB_CTRLDATA	
CPU_DISP_HPDB	DG43	GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD	
	DG47	GPP_A21/DDPC_CTRLCLK/I2S5_TXD	
	DJ47	GPP_A22/DDPC_CTRLDATA/I2S5_RXD	
TBT_LSX0_TXD	DU8	GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD	TBT2
TBT_LSX0_RXD	DV8	GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD	
TBT_LSX1_TXD	DF6	GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD	TBT
TBT_LSX1_RXD	DD6	GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD	
GPP_D10	DN23	GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#	
	DM23	GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK	
GPP_D12	DK23		
	DN21	GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO	
	DF43	GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI	
CPU_DISP_HPD1	DF45	GPP_A17/DISP_MISCC/I2S4_TXD	
	DF47	GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK	
USB_OC1#	DH52	GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM	
USB_OC2#	DK45	GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	
		GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK	
eDP_VDD_EN	DM8	EDP_VDDEN	eDP
L_BKLT_EN	DN8	EDP_BKLTEN	
L_BKLT_CTRL	DG10	EDP_BKLTCTL	

TGL-U-GP-U1

TCP0_TXRX_P1	AY2	USB2_TCSS_RX_P1	TBT2
TCP0_TXRX_N1	AY1	USB2_TCSS_RX_N1	
TCP0_TXRX_P0	BB1	USB2_TCSS_RX_P0	
TCP0_TXRX_N0	BB2	USB2_TCSS_RX_N0	
TCP0_TX_P1	AM5	USB2_TCSS_TX_P1	
TCP0_TX_N1	AM7	USB2_TCSS_TX_N1	
TCP0_TX_P0	AT7	USB2_TCSS_TX_P0	
TCP0_TX_N0	AT5	USB2_TCSS_TX_N0	
TCP0_AUX_P	AP7	USB2_TCSS_AUX_P	
TCP0_AUX_N	AP5	USB2_TCSS_AUX_N	
TCP1_TXRX_P1	AT2	USB1_TCSS_RX_P1	TBT
TCP1_TXRX_N1	AT1	USB1_TCSS_RX_N1	
TCP1_TXRX_P0	AU1	USB1_TCSS_RX_P0	
TCP1_TXRX_N0	AU2	USB1_TCSS_RX_N0	
TCP1_TX_P1	AD5	USB1_TCSS_TX_P1	
TCP1_TX_N1	AD7	USB1_TCSS_TX_N1	
TCP1_TX_P0	AH7	USB1_TCSS_TX_P0	
TCP1_TX_N0	AH5	USB1_TCSS_TX_N0	
TCP1_AUX_P	AF7	USB1_TCSS_AUX_P	
TCP1_AUX_N	AF5	USB1_TCSS_AUX_N	
	BF1		
TCP2_TXRX_P1	BF2		
TCP2_TXRX_N1	BE2		
TCP2_TXRX_P0	BE1		
TCP2_TXRX_N0	BD7		
TCP2_TX_P1	BD5		
TCP2_TX_N1	AY5		
TCP2_TX_P0	AY7		
TCP2_TX_N0	BB5		
TCP2_AUX_P	BB7		
TCP2_AUX_N			
	BK1		
TCP3_TXRX_P1	BK2		
TCP3_TXRX_N1	BJ2		
TCP3_TXRX_P0	BJ1		
TCP3_TXRX_N0	BM7		
TCP3_TX_P1	BM5		
TCP3_TX_N1	BH5		
TCP3_TX_P0	BH7		
TCP3_TX_N0	BK5		
TCP3_AUX_P	BK7		
TCP3_AUX_N			
	AN2	TCSS_RCOMP_P	
TC_RCOMP_P	AN1	TCSS_RCOMP_N	R402 1 150R2F-1-GP
TC_RCOMP_N			
	M8		
DSI_DE_TE_2			
	AB1	DISP_RCOMP	R401 1 150R2F-1-GP
DDI_RCOMP			
	CE4		
DISP_UTILS/DSI_DE_TE_1			

GP

<Core Design>

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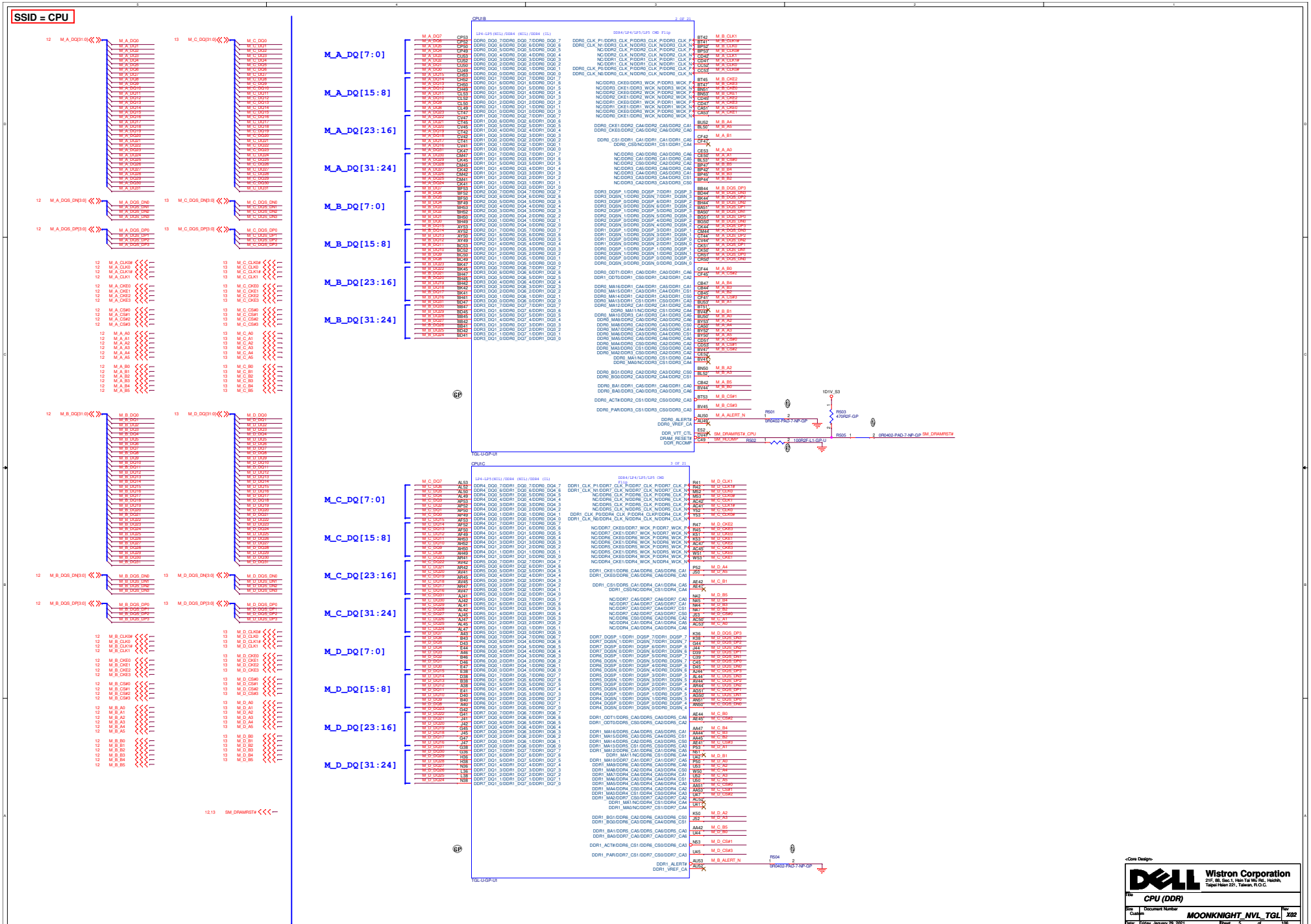
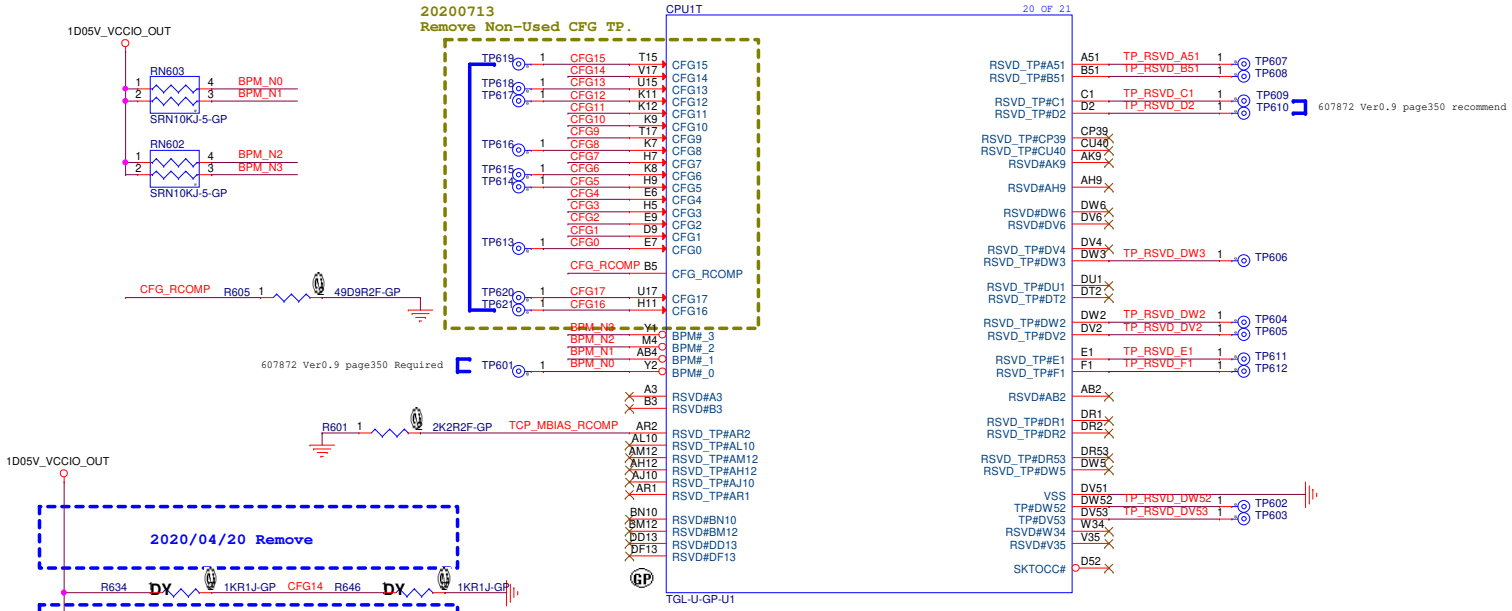
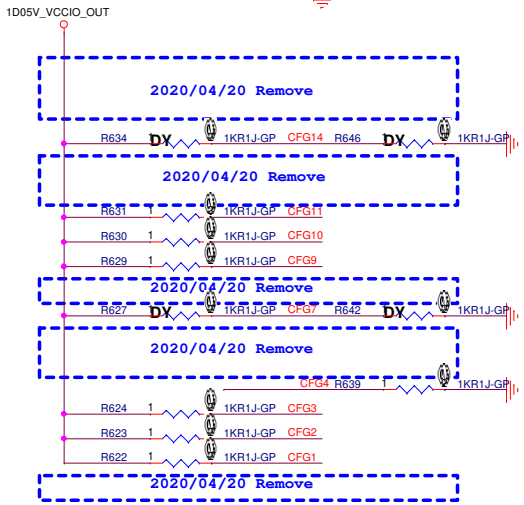
Title	CPU (DDI/EDP/TBT/TPC/)	
Size A3	Document Number MOONKNIGHT_NVL_TGL	Rev X02
Date: Friday, January 29, 2021	Sheet 4 of 106	

SSID = CPU



SSID = CPU





CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

<Core Design>

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Title: CPU (CFG/IST)

Size: A3 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 29, 2021 | Sheet 6 of 106

SSID = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_ALERT#_CPU
46 SVID_CLK_CPU
46 SVID_DATA_CPU

CPU1M 13 OF 21

1V_CPU_CORE

VCCIN: A24, A26, A29, A30, A33, A35, AY39, B24, B26, B29, B30, B33, B35, BA10, BA40, BB39, BB9, BC10, BC40, BD39, BD9, BE10, BE40, BF9, BG10, BG40, BH12, BH39, BH9, BJ10, BJ40, BK39, BL10, BL40, BM39, BN40, BP12, BP39, BR10, BR40, BT12, BT39, BU10, BU40, BV12, BY12, CA10, CB12, D24, D26, D29, D30, D33, D35, E24, E26, E27, E29, E30, E32, E33, G2, G24, G26, G30

1V_CPU_CORE

VCCIN: G32, H24, H26, H30, H32, J1, J2, K1, K2, K24, K26, K30, K32, L24, L26, L30, L32, N24, N26, N30, N32, P24, P26, P28, P30, P32, T21, T23, T25, T27, T31, U23, U27, U29, U31, U33, V23, V25, V27, V29, V31, V33, W22, W24, W28, W32

VCCIN_SENSE — R38 — VCCCORE_SENSE
VSSIN_SENSE — R37 — VSSCORE_SENSE

VIDSOUT — M12 — SVID_DATA_CPU
VIDSCK — M11 — SVID_CLK_CPU
VIDALERT# — P12 — SVID_ALERT#_CPU

TGL-U-GP-U1

20200724
C701 C702 follow Cyborg reserve footprint.

1D05V_VCCST

R703 1 — 100R2F-L1-GP-U — SVID_DATA_CPU
R701 2 — 1 — 56R2J-4-GP — SVID_ALERT#_CPU
R707 DY — 1 — 56R2J-4-GP — SVID_CLK_CPU

DY C702 2 SCD1U25V2KX-1-DL-GP
DY C701 2 SCD1U25V2KX-1-DL-GP

3.Length matchin 25mil, and close SOC in 2inch "

Layout note: **Layout Note:**

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE
   impedance=50 ohm
3. Length match<25mil

1V_CPU_CORE

R704 1 — 100R2F-L1-GP-U — VCCCORE_SENSE
R705 1 — 100R2F-L1-GP-U — VSSCORE_SENSE

<Core Design>

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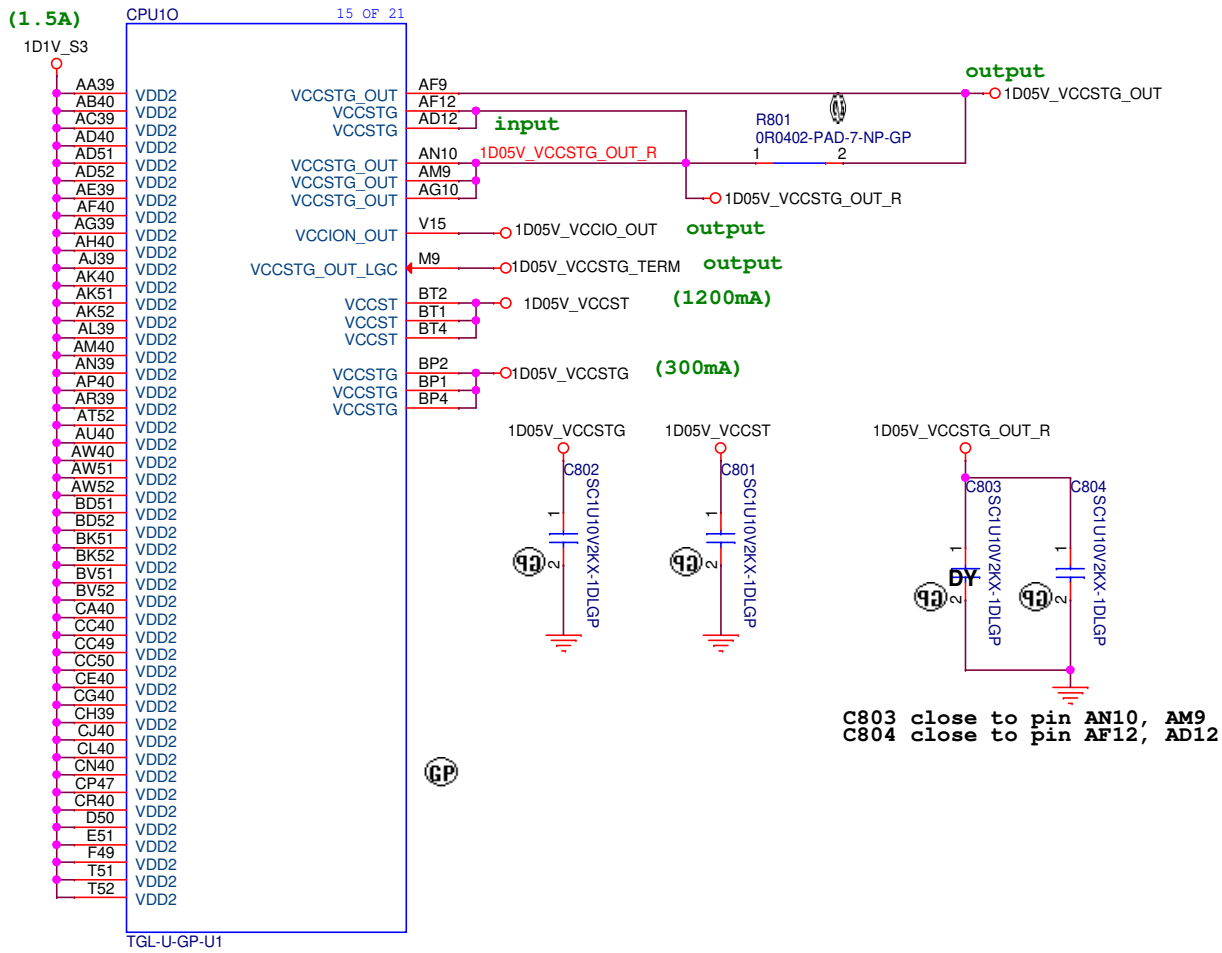
Title	CPU (VCCIN/VID)	
Size A4	Document Number MOONKNIGHT_NVL_TGL	Rev X02
Date: Friday, January 29, 2021	Sheet 7 of 106	

SSID = CPU



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

<Core Design>

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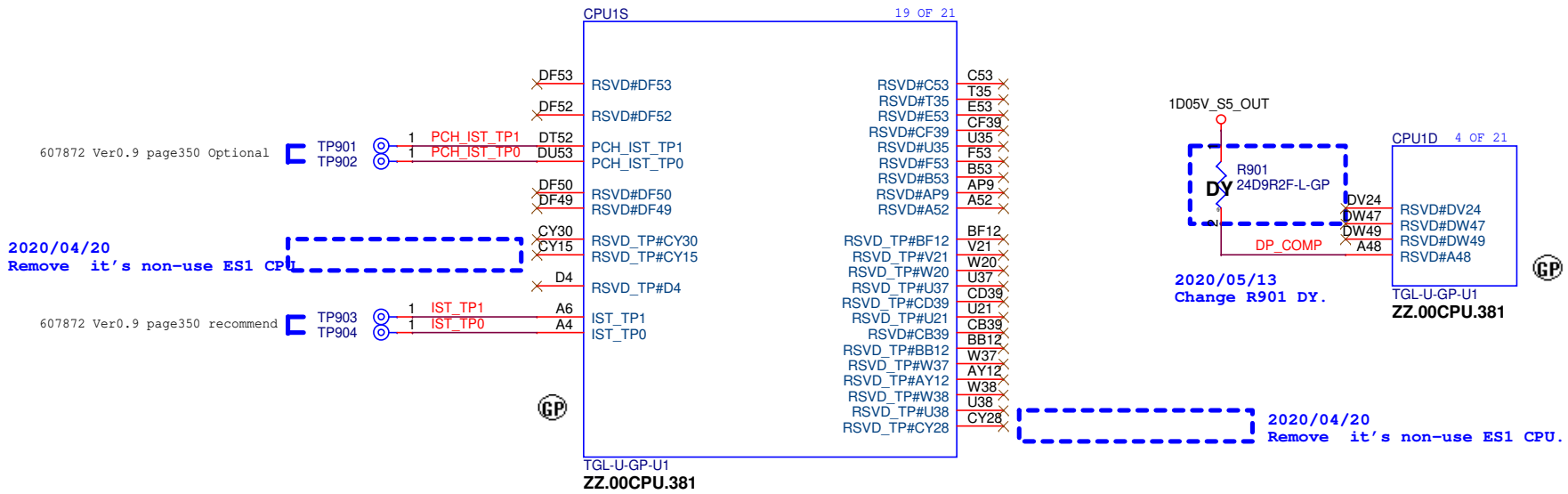
Title	CPU (VDDQ/VCC/VCCST)	
Size A4	Document Number MOONKNIGHT_NVL_TGL	Rev X02
Date: Friday, January 29, 2021	Sheet 8 of 106	

SSID = CPU



<Core Design>

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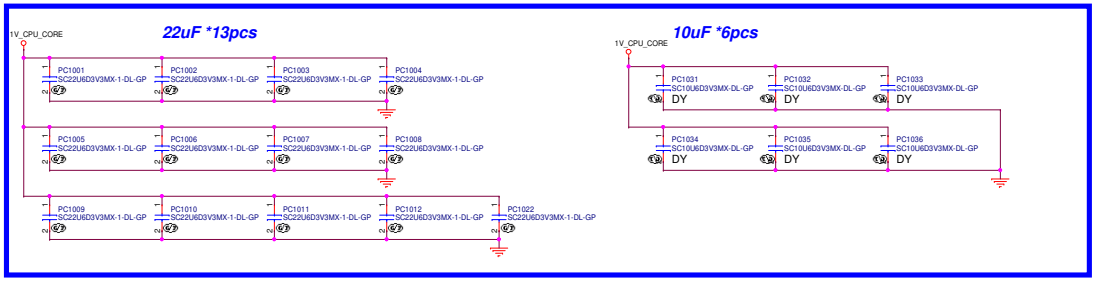
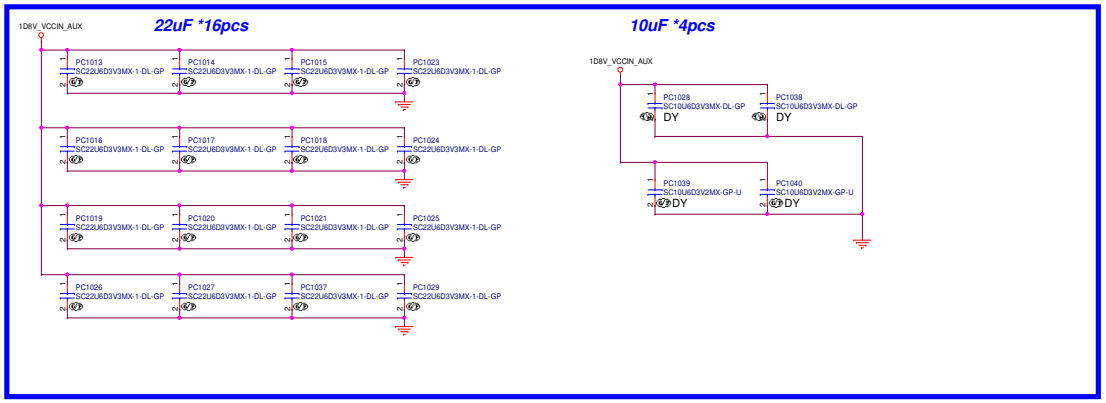
Title	***CPU (RSVD)***	
Size: A4	Document Number: ***MOONKNIGHT_NVL_TGL***	Rev: ***X02***
Date: Friday, January 29, 2021	Sheet 9 of 106	

Main Func = CPU



2020/04/20
Move from Page10 to Page89



2020/04/20
Move from Page10 to Page89

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

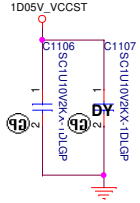
Title: CPU (CORE Power Cap1)

Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

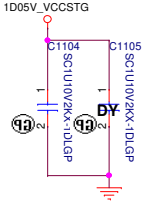
Date: Friday, January 29, 2021 | Sheet 10 of 106

SSID = CPU

1D05V_VCCST

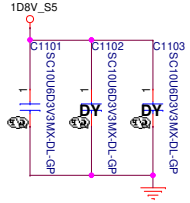


1D05V_VCCSTG



20200727
FC1128 FC1129 FC1130
Move from Page11 to Page89 .

1D8V_S5



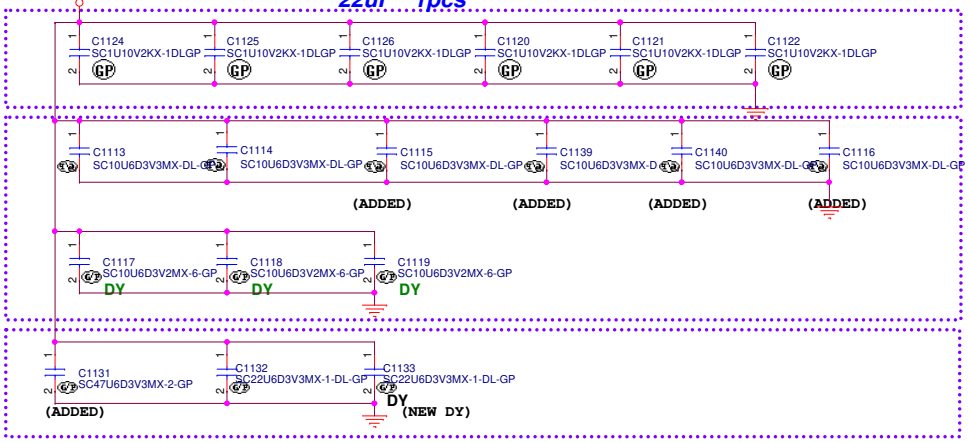
1uF *6pcs
10uF *6pcs
47UF *1pcs
22uF *1pcs

PLACE on Primary SIDE

PLACE on Back SIDE

PLACE Close to VR

1D1V_S3



Decoupling Solution

Power Rail	Decap Placement	Form Factor	Value	Number	Note
VCCDD2	Secondary Side	0402	10uF	8	Place on the back side of the SOC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	Primary Side	0603	47uF	2	Place them as close to the VR as possible. 2 caps should be stuffed.
		0402	1uF	8	Place on the primary side, as close as possible to the vias that connect to the outer row of SOC pins, use wide traces to connect the capacitor pins to the vias. Make sure to put atleast 1 via down near the outer Vdd2 BGA and 1 via down near the cap pad

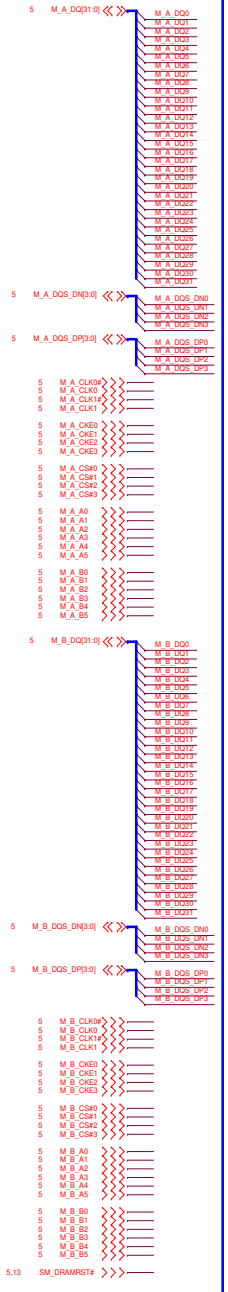
<Core Design>

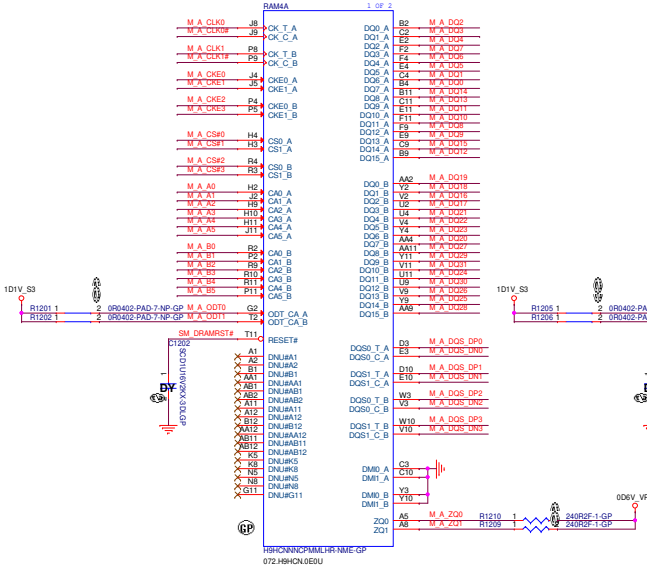
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

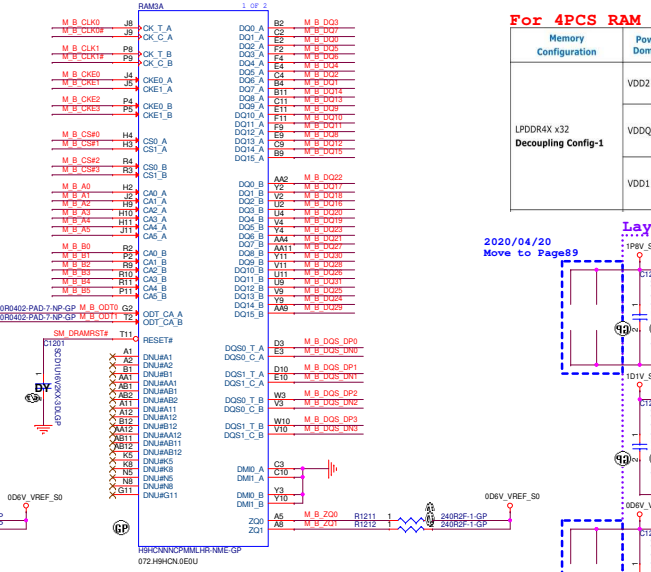
Title	CPU (Power Cap2)	
Size A3	Document Number MOONKNIGHT_NVL_TGL	Rev X02
Date: Friday, January 29, 2021	Sheet 11 of 106	

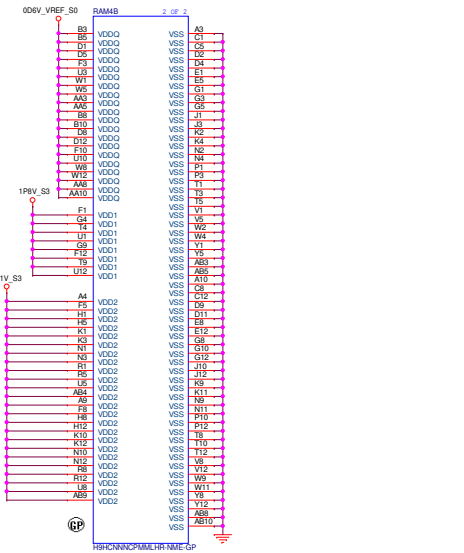
SSID = MEMORY

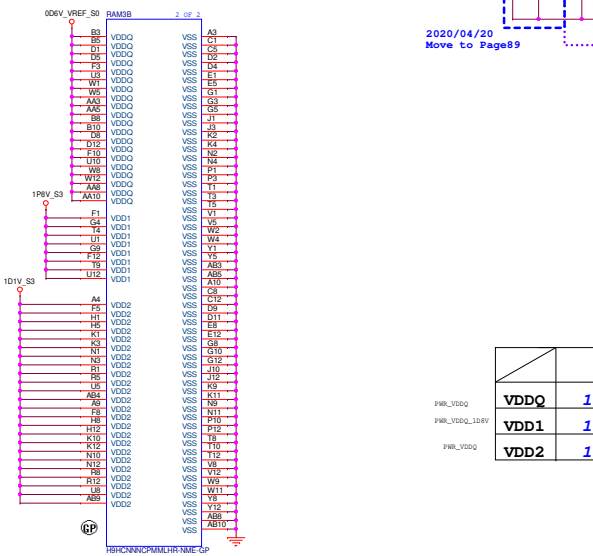
DQS_A swizzling map:









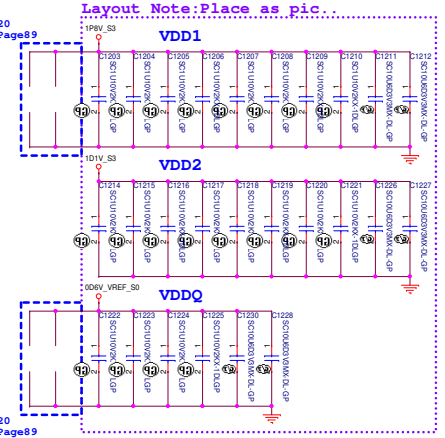


For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

2020/04/20 Move to Page89

Layout Note:Place as pic..



2020/04/20 Move to Page89

	LPDDR4		LPDDR4X		
VDDQ	1.1V	410mA	0.6V	185mA	PWR_VDDQ_VTT
VDD1	1.8V	6.8mA	1.8V	12mA	PWR_VDDQ_1D8V
VDD2	1.1V	290mA	1.1V	465mA	1D1V_S3

PWR_VDDQ
PWR_VDDQ_1D8V
PWR_VDDQ

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

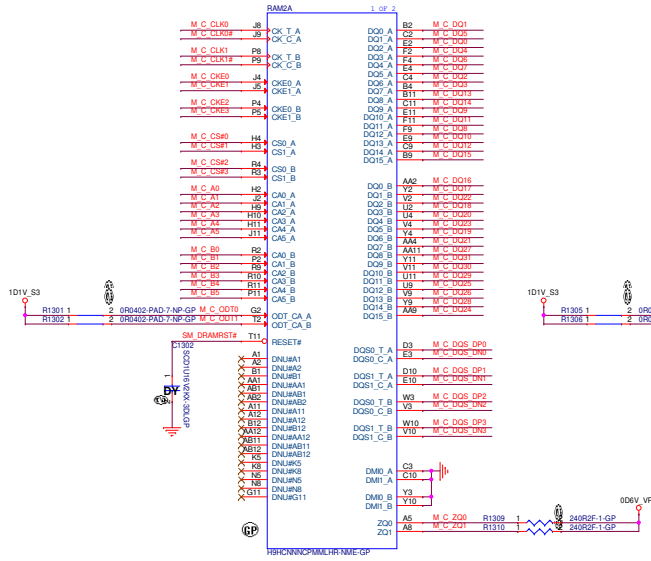
Title: DDR (DDR4-CHA)

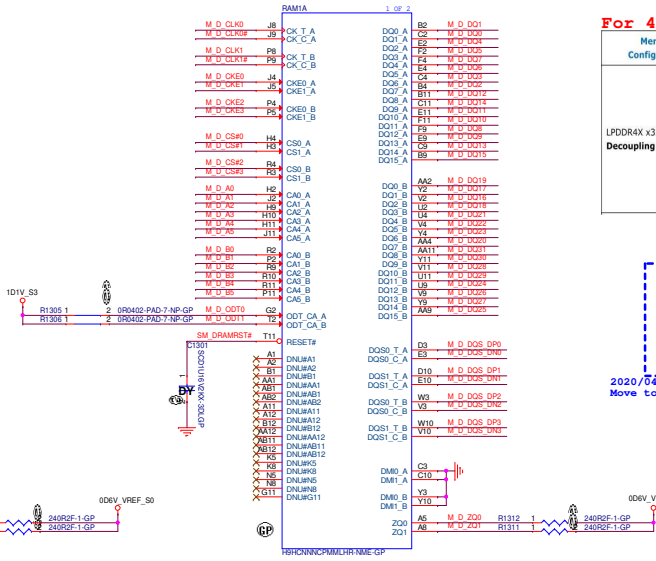
Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

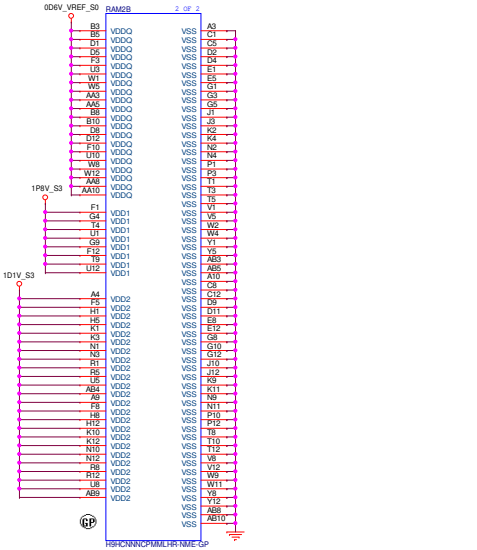
Date: Friday, January 29, 2021 | Sheet 12 of 106

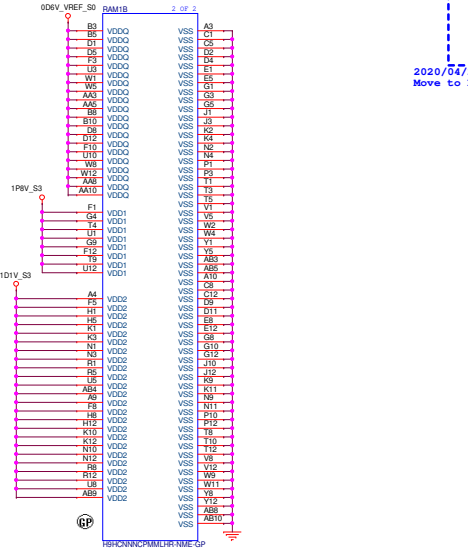
SSID = MEMORY

DQS_B swizzling map:





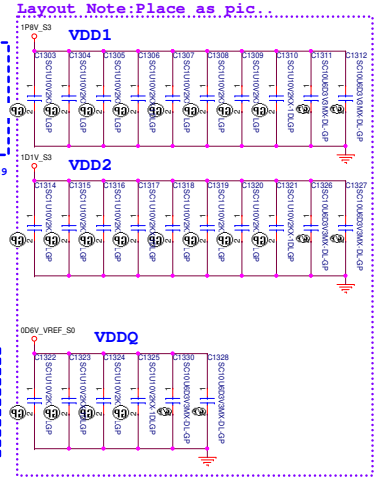




For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic.



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 29, 2021 | Sheet 13 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR (RSVD)*		
Size: A4	Document Number: *MOONKNIGHT_NVL_TGL*	Rev: *X02*
Date: Friday, January 29, 2021	Sheet 14 of 106	

SSID = CPU

18,24,25,91 SPI0_SI_CPU
18,24,25 SPI0_WP_CPU
18,24,25 SPI0_HOLD_CPU

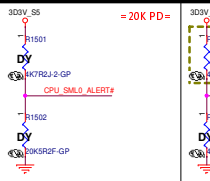
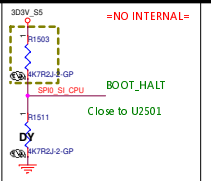
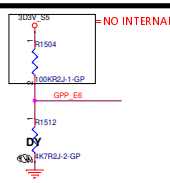
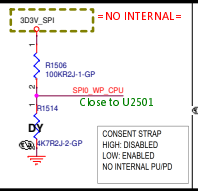
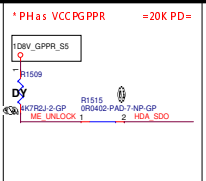
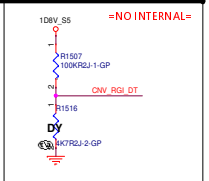
21 CNV_RGI_DT
18 CPU_SML0_ALERT#
18 GPP_E6
19 HDA_SDO
4,75 TBT_LSX0_RXD
4 GPP_D10
3 DBG_PMODE
4 GPP_D12
4,71 TBT_LSX1_RXD

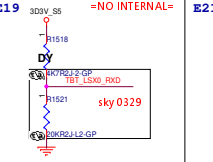
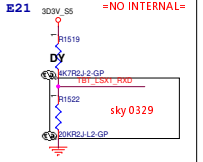
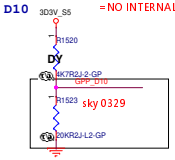
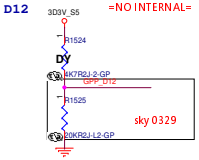
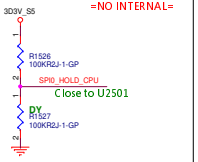
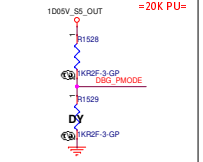
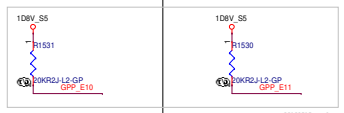
Added, MKT NVL 13 EIV, 2020/03/16

18 GPP_E10
18 GPP_E11

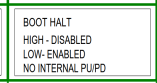
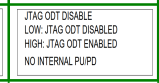
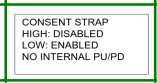
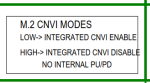
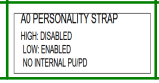
20200724
R1503 100K change 4.7K.

20200724
3D3V_S5 change 3D3V_SPI.

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)	
Schematic				=20K PD=				
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE	
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE	

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic								
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
							
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
							

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
A2	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 15 of 106

SSID = PCH

GPU

76 GFX_PCIE_TX_P0
76 GFX_PCIE_TX_N0
76 GFX_PCIE_RX_P0
76 GFX_PCIE_RX_N0

76 GFX_PCIE_TX_P1
76 GFX_PCIE_TX_N1
76 GFX_PCIE_RX_P1
76 GFX_PCIE_RX_N1

76 GFX_PCIE_TX_P2
76 GFX_PCIE_TX_N2
76 GFX_PCIE_RX_P2
76 GFX_PCIE_RX_N2

76 GFX_PCIE_TX_P3
76 GFX_PCIE_TX_N3
76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3

M.2 SSD

63 SSD_PCIE_TX_P7
63 SSD_PCIE_TX_N7
63 SSD_PCIE_RX_P7
63 SSD_PCIE_RX_N7

63 SSD_PCIE_TX_P6
63 SSD_PCIE_TX_N6
63 SSD_PCIE_RX_P6
63 SSD_PCIE_RX_N6

63 SSD_PCIE_TX_P5
63 SSD_PCIE_TX_N5
63 SSD_PCIE_RX_P5
63 SSD_PCIE_RX_N5

63 SSD_PCIE_TX_P8
63 SSD_PCIE_TX_N8
63 SSD_PCIE_RX_P8
63 SSD_PCIE_RX_N8

63 M2_PEDET1
63 M2_DEVSLP1

WLAN

61 WLAN_PCIE_TX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_RX_N
61 WLAN_RF_DIS#

USB1

USB3.1 Type-A Port1 (IO)

66 USB1_USB31_TX_P
66 USB1_USB31_TX_N
66 USB1_USB31_RX_P
66 USB1_USB31_RX_N

66 USB1_USB20_P
66 USB1_USB20_N

35 USB_OC0#

USB2

USB3.1 Type-A Port2 (IO)

66 USB2_USB31_TX_P
66 USB2_USB31_TX_N
66 USB2_USB31_RX_P
66 USB2_USB31_RX_N

66 USB4_USB20_P
66 USB4_USB20_N

Card Reader

66 CARD1_USB20_P
66 CARD1_USB20_N

Camera

55 CCD_USB20_P
55 CCD_USB20_N

Finger Print

92 FP1_USB20_N
92 FP1_USB20_P

TBT2

72 USB3_USB20_P
72 USB3_USB20_N

BT

61 BT_USB20_P
61 BT_USB20_N

PD

71,75 PCH_TBT_PERST#
71,75 TBT_FORCE_PWR
20200727
Net name follow GPIO Table.

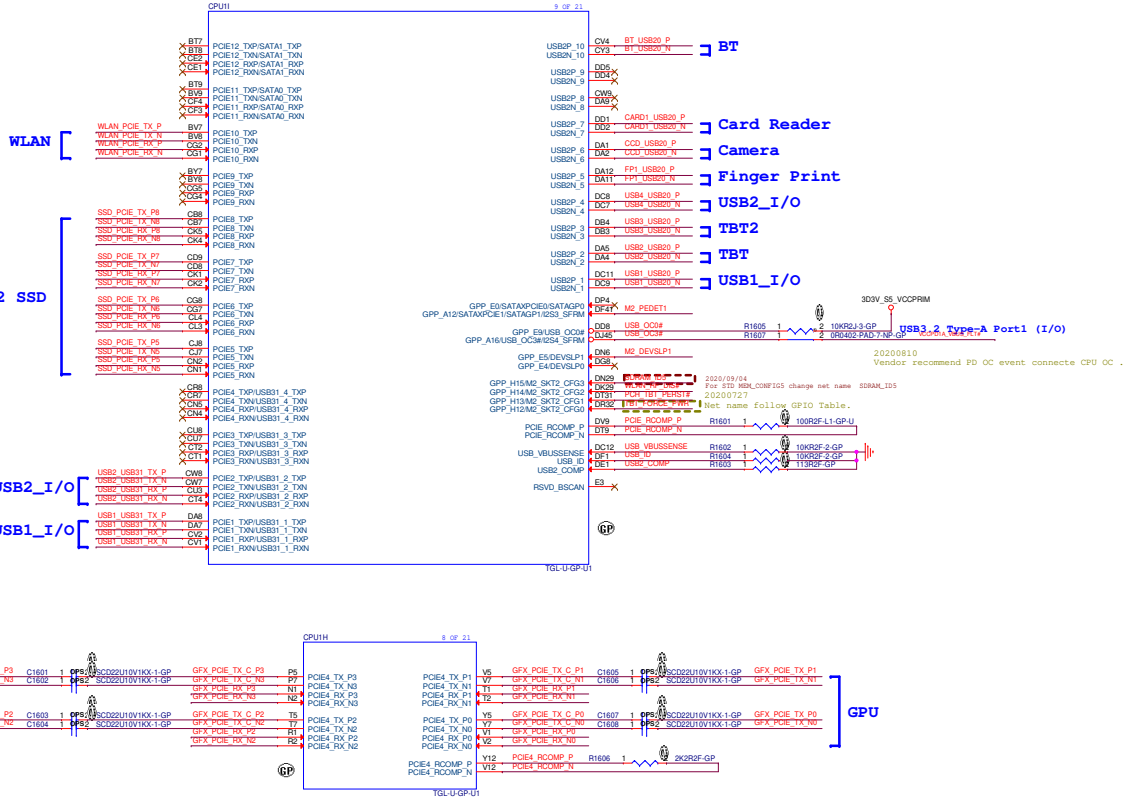
MM

21 SDRAM_ID5

TBT

72 USB2_USB20_P
72 USB2_USB20_N

44,72,74 VCCPD1A_VBUS_FLT#



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 29, 2021 | Sheet 16 of 106

SSID = PCH

61,63,71,75,76,91 PCH_PLTRST#
40,55 SIO_SLP_S3#
40,92 SIO_SLP_S4#
24,25,45 3V_5V_PWRGD
24 SIO_PWRBTN#
24,64 PCH_RSMRST#
24,26 IMVP_VR_ON
24 SYS_PWROK
24,40 SIO_SLP_SUS#
40 VCCST_OVERRIDE
40 CPU_C10_GATE#
24 PCH_DPWROK
44 AC_IN#
24,40,46 ALL_SYS_PWRGD
46 PWR_VCORE_VR_READY
61 PCIE_WAKE#

Type-C BB

72 TBT_PD_ALERT#
24,40,50 VCCIN_AUX_PWRGD
24,71 TCP1_RETIMER_PERST_R_N
24 EC_RESET#

CPU1L — 12 OF 21 — TGL-U-GP-U1

SIO_SLP_SUS# DV49 SLP_SUS#
SIO_SLP_S4# DM43 GPD10/SLP_S5#
SIO_SLP_S3# DU41 GPD5/SLP_S4#
DJ43 GPD4/SLP_S3#
DR41 GPD6/SLP_A#
DT44 GPD9/SPL_WLAN#
DD42 GPP_B12/SLP_S0#
DN39 SLP_LAN#
PM_RSMRST# DM35 RSMRST#
SYS_RESET# DD10 SYS_RESET#
PCH_PLTRST# DD41 GPP_B13/PLTRST#
DSW_PWROK_R DK35 DSW_PWROK
SYS_PWROK DF10 SYS_PWROK
PCH_PWROK DN35 PCH_PWROK
RTC_INTRUDER# DM37 INTRUDER#
SPI_VCC_SEL DT49 SPIVCCIOSEL

PROCPWRGD BM9 TP_VCORE_PWRGD 1 TP1702 follow 612304 Ver0.9
GPD3/PWRBTN# DK41 SIO_PWRBTN#
GPD0/BATLOW# DN41 PCH_BATLOW#
GPD1/ACPRESENT DK43 AC_PRESENT
GPP_B11/PMCALERT# CW40 TBT_PD_ALERT#
GPP_H18/CPU_C10_GATE# DN27 CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF# DG31 TPM_PRSNT#
WAKE# DK39 PCIE_WAKE#
GPD2/LAN_WAKE# DM41
GPD11/LANPHYPC/DSWLDO_MON DT41
GPD7 DN43 GPD7_R R1748 1 DY 2 0R2J-2-GP TCP1_RETIMER_PERST_R_N
CE5 VCCSTPWRGOOD_TCSS R1731 1 2 0R0402-PAD-7-NP-GP VCCST_OVERRIDE
VCCSTPWRGOOD_TCSS BP8 VCCST_PWRGD_R
VCCST_PWRGD BP9 VCCST_OVERRIDE_R R1728 1 2 0R0402-PAD-7-NP-GP VCCST_OVERRIDE
VCCST_OVERRIDE
DR12
GPP_F20/EXT_PWR_GATE#
GPP_F21/EXT_PWR_GATE#

DR12: EXT_PWR_GATE#
DW12: EXT_PWR_GATE2#

20200724
TPM_SEL Change NET NAME to TPM_PRSNT#.

1D8V_S5
R1742 100KR2J-1-GP fwTPM
TPM_PRSNT#
R1743 100KR2J-1-GP TPM

ID	Description	Setting	Mapping
TPM_SEL	TPM SUPPORT	1	fwTPM
		0	TPM

Moved from Page 91 to Page 17, MKT NVL 13 EIV, 2020/03/24

PCH_DPWROK R1723 0R2J-2-GP
ALL_SYS_PWRGD D1704 LRB520S-30T1G-GP
PWR_VCORE_VR_READY R17451 0R0402-PAD-7-NP-GP
IMVP_VR_ON R17461 0R0402-PAD-7-NP-GP
NON-G3

3rd = 083.52030.0C8F
2ND = 083.52030.008F
83.R2003.A8M

3D3V_AUX_S5 R17371 100KR2J-1-GP 2 PM_RSMRST#_M
Q1702 2N7002KDW-1-GP
D1701 RB520S30-GP AC_IN# AC_PRESENT PM_RSMRST#
75.27002.F7C

SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V

SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V

RTC_AUX_S5 R1704 1MR2F-GP RTC_INTRUDER#
R1714 1MR2F-GP DY C1701 SCD1U16V2KX-3DLGP
20200513 Need to check??
3D3V_S5_VCCPRIM R1705 DY 4K7R2J-2-GP SPI_VCC_SEL
R1706 4K7R2J-2-GP

20200814 Follow Cyborg PU to 3D3V_S5_VCCPRIM.
3D3V_S5_VCCPRIM R1701 1 2 10KR2J-3-GP SYS_RESET#
3D3V_S5_VCCPRIM R1713 1 100KR2J-1-GP AC_PRESENT
R1715 1 2 10KR2J-3-GP PCH_BATLOW#
3D3V_S5 R1716 1 2 1KR2F-3-GP PCIE_WAKE#

VCCST_OVERRIDE R1730 1 2 100KR2J-1-GP
PCH_PWROK R1732 1 2 100KR2J-1-GP
SYS_PWROK R1733 1 2 100KR2J-1-GP
PCH_PLTRST# R1744 1 2 100KR2J-1-GP
From PDG Request

3V_5V_PWRGD R1729 1 68KR2J-GP DSW_PWROK_R
DY C1703 SCD1U16V2KX-3DLGP DY

20200727
Follow Cyborg remove R1747 C1704.

Volatge Level 1V

3D3V_S5 C1702 SCD1U16V2KX-3DLGP
1D05V_VCCST R1702 1KR2F-3-GP
U1701 74LVC1G07GW-GP
ALL_SYS_PWRGD VCCST_PWRGD_RR R1703 1 2 60D4R2F-GP VCCST_PWRGD_R
73.01G07.0HG
2ND = 073.7SZ07.000G

3D3V_AUX_S5 R1707 1 2 100KR2J-1-GP R1708 10KR2J-3-GP
Q1701 2N7002KDW-1-GP
3V_5V_POK# 3V_5V_POK_C
PM_RSMRST# R1709 1 DY 1KR2J-1-GP PCH_RSMRST#
D1709 RB520S30-GP 3V_5V_PWRGD
D1706 RB520S30-GP VCCIN_AUX_PWRGD
R1711 100KR2J-1-GP
83.R2003.A8M 2nd = 083.52030.008F 3rd = 083.52030.0C8F
83.R2003.A8M 2nd = 083.52030.008F 3rd = 083.52030.0C8F

SCD1U16V2KX-3DLGP C1714 3D3V_S5
U1703 G3904M41U-GP 20191223 Change Part number 074.03904.0053
VDD PWROK
PCHRST PWRGD
PCHPOK NC#
EC_EN GND
PCH_RSMRST# PCH_RSMRST#_U R1773 0R0402-PAD-7-NP-GP
PCH_DPWROK PCH_DPWROK_R R1775 0R0402-PAD-7-NP-GP
EC_RESET# EC_PCH_SPI_EN_R R1774 0R0402-PAD-7-NP-GP
3D3V_S5_U R1771 0R0402-PAD-7-NP-GP 3D3V_S5_R
3V_5V_PWRGD_U R1772 0R0402-PAD-7-NP-GP 3V_5V_PWRGD
074.03904.0053

Power on sequence for G3 sharing

2020/08/03 Follow shuri Nakia R1738 change 390K.

3D3V_S5 3D3V_S5_VCCPRIM R1738 390KR2J-1-GP R17211 100KR2J-1-GP
3D3V_S5_PCH_R 3D3V_S5_R C1713 SCD1U16V2KX-3DLGP
U1710 74LVC1G08GW-1-GP
73.01G08.L04
2ND = 073.7SZ08.000G
3RD = 073.01G08.IHG
3V_5V_PWRGD D1708 RB520S30-GP
83.R2003.A8M 2nd = 083.52030.008F 3rd = 083.52030.0C8F
R17761 DY 0R2J-2-GP
3D3V_S5_R D1702 RB520S30-GP PCH_DPWROK
83.R2003.A8M 2nd = 083.52030.008F
DSW_PWROK_R D1703 RB520S30-GP PCH_DPWROK
83.R2003.A8M 2nd = 083.52030.008F

DSW_PWROK_R C1712 SCD1U16V2KX-3DLGP
R1734 0R0402-PAD-7-NP-GP
Q1703 2N7002KDW-1-GP
Q1703_2_3 R1735 DY 100KR2J-1-GP
R1736 10KR2F-2-GP
DSW_PWROK
R1739 1MR2F-GP
20200724
R1739 Change to 1M PD.
SIO_SLP_SUS# R1777 DY 0R1J-GP SIO_SLP_SUS#
D1707 LRB520S-30T1G-GP
083.52030.008F
2nd = 83.R2003.A8M
3rd = 083.52030.0C8F
PCH_RSMRST# DSW_PWROK
U1702 74LVC1G08GW-1-GP
73.01G08.L04
2ND = 073.7SZ08.000G
3RD = 073.01G08.IHG
PM_RSMRST#

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: Custom | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02
Date: Friday, January 29, 2021 | Sheet 17 of 106

SSID = PCH

SPI ROM

24,25,91 SPI0_CLK_CPU
15,24,25 SPI0_HOLD_CPU
15,24,25 SPI0_WP_CPU
24,25,91 SPI0_SO_CPU
15,24,25,91 SPI0_SI_CPU
18,24,25 SPI0_CS_ROM_N0

EC

24,68 ESPI_CPU_IO0
24,68 ESPI_CPU_IO1
24,68 ESPI_CPU_IO2
24,68 ESPI_CPU_IO3
24,68 ESPI_CPU_CS#
24,68 ESPI_CPU_RST#
24,68 ESPI_CPU_CLK

WLAN

61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 CLK_PCIE_WLAN_REQ#

M.2 SSD

63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 CLK_PCIE_NVME_REQ#

20200721
Remove SATA_LED# Off Page

GPU

76 GFX_CLK_CPU_N
76 GFX_CLK_CPU_P
76 CLK_PCIE_PEG_REQ#

20200727
Net name follow GPIO Table.

79,86 GC6_FB_EN
76 DGPU_HOLD_RST#

XDP

SMBUS

71,75 CPU_SML0_SMBCLK
71,75 CPU_SML0_SMBDATA
72 CPU_SML1_SMBCLK
72 CPU_SML1_SMBDATA
24,26,79 EC_I2C_SCL_THM
24,26,79 EC_I2C_SDA_THM

OTHER

24,61 SUSCLK

HW STRAP

15 CPU_SML0_ALERT#
15 GPP_E6
15 GPP_E10
15 GPP_E11

MEMORY

20 MEM_CHA_EN

SD

66 HOST_SD_WP#

TPM

18,91 SPI0_CS_CPU_N2

SIV Auto Test

96 SPI0_SO_R_CPU
18,24,25 SPI0_CS_ROM_N0
18,91 SPI0_CS_CPU_N2

20200810
Follow Shuri Change to 22ohm.

SPI0_CLK_CPU R18261 22R2J-2-GP SPI0_CLK_R_CPU
SPI0_HOLD_CPU R18271 22R2J-2-GP SPI0_HOLD_R_CPU
SPI0_WP_CPU R18281 22R2J-2-GP SPI0_WP_R_CPU
SPI0_SO_CPU R18291 22R2J-2-GP SPI0_SO_R_CPU
SPI0_SI_CPU R18301 22R2J-2-GP SPI0_SI_R_CPU
SPI0_CS_ROM_N0 SPI0_CS_CPU_N2

20200513
Delete 0 ohm Res.

20200721
Remove SATA_LED# net .

20200727
Net name follow GPIO Table.

GPP_E11
GPP_E10
DGPU_HOLD_RST#
GPP_E6
GC6_FB_EN
HOST_SD_WP#
MEM_CHA_EN

CPU1E
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DJ37 SPI0_CLK
DG35 SPI0_IO3
DJ39 SPI0_IO2
DJ33 SPI0_MISO
DJ35 SPI0_MOSI
DF35 SPI0_CS1#
DG37 SPI0_CS0#
DF39 SPI0_CS2#
DJ6 GPP_E11/SPI1_CLK/THC0_SPI1_CLK
DN5 GPP_E2/SPI1_IO3/THC0_SPI1_IO3
DR9 GPP_E1/SPI1_IO2/THC0_SPI1_IO2
DM6 GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
DK6 GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
DK8 GPP_E10/SPI1_CS#/THC0_SPI1_CS#
DV11 GPP_E8/SPI1_CS1#/SATA_LED#
DW9 GPP_E17/THC0_SPI1_INT#
DT8 GPP_E6/THC0_SPI1_RST#
DN15 GPP_F11/THC1_SPI2_CLK
DK13 GPP_F15/GSXSRESET#/THC1_SPI2_IO3
DM13 GPP_F14/GSXDIN/THC1_SPI2_IO2
DN13 GPP_F13/GSXSLOAD/THC1_SPI2_IO1
DJ15 GPP_F12/GSXDOUT/THC1_SPI2_IO0
DK15 GPP_F16/GSXCLK/THC1_SPI2_CS#
DN10 GPP_F18/THC1_SPI2_INT#
DV14 GPP_F17/THC1_SPI2_RST#
DH3 CL_CLK
DH4 CL_DATA
DF2 CL_RST#

TGL-U-GP-U1

DK21 GPP_C0/SMBCLK CPU_SMB_SCL
DM19 GPP_C1/SMBDATA CPU_SMB_SDA
DN19 GPP_C2/SMBALERT# CPU_SMB_ALERT#
XDP

DK19 GPP_C3/SML0CLK CPU_SML0_SMBCLK
DM17 GPP_C4/SML0DATA CPU_SML0_SMBDATA
DN17 GPP_C5/SML0ALERT# CPU_SML0_ALERT#
BB (TBT/TBT2)

DK17 GPP_C6/SML1CLK CPU_SML1_SMBCLK
DJ17 GPP_C7/SML1DATA CPU_SML1_SMBDATA
PD I2C2S_I2C

CY50 GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#
DN53 GPP_A5/ESPI_CLK PCH_ESPI_CLK
DJ53 GPP_A3/ESPI_IO3/SUSACK# PCH_ESPI_IO3
DH50 GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK PCH_ESPI_IO2
DP50 GPP_A1/ESPI_IO1 PCH_ESPI_IO1
DP52 GPP_A0/ESPI_IO0 PCH_ESPI_IO0
DK52 GPP_A4/ESPI_CS# PCH_ESPI_CS#
DL50 GPP_A6/ESPI_RESET# ESPI_RESET#

R1804 33R2F-3-GP ESPI_CPU_CLK
R1808 15R2F-2-GP ESPI_CPU_IO3
R1807 15R2F-2-GP ESPI_CPU_IO2
R1806 15R2F-2-GP ESPI_CPU_IO1
R1805 15R2F-2-GP ESPI_CPU_IO0
R1809 2R0402-PAD-7-NP-GP ESPI_CPU_CS#
R1810 2R0402-PAD-7-NP-GP ESPI_CPU_RST#
R1814 75KR2J-GP
to EC,debug14pin

RN1808 SRN0J-6-GP
CPU_SML0_SMBCLK EC_I2C_SCL_THM
CPU_SML0_SMBDATA EC_I2C_SDA_THM

20200819
Layout Swap.
RN1803 SRN1KJ-7-GP
CPU_SMB_SDA
CPU_SMB_SCL

20200820
Layout Swap.
RN1801 SRN1KJ-7-GP
CPU_SML0_SMBDATA
CPU_SML0_SMBCLK
RN1807 SRN1KJ-7-GP
CPU_SML1_SMBCLK
CPU_SML1_SMBDATA

R1823 10KR2J-3-GP CPU_SMB_ALERT#
R1824 10KR2J-3-GP

ID	Description	Setting	Mapping
MEM_Speed SEL	CPU Version	1	B1 CPU
		0	B0 CPU

1D8V_S5
R1802
B1 CPU
10KR2J-3-GP
MEM_SPEED_SEL
R1803
B0 CPU
10KR2J-3-GP

20200724
R1802 and R1803 property follow Shuri..

CPU1K
11 OF 21

BW1 BW2 CLKOUT_PCIE_P6 CLKOUT_PCIE_N6
CB2 CB1 CLKOUT_PCIE_P5 CLKOUT_PCIE_N5
M.2 SSD
SSD_CLK_CPU_P BW4 CLKOUT_PCIE_P4
SSD_CLK_CPU_N BW5 CLKOUT_PCIE_N4
CL7 CL8 CLKOUT_PCIE_P3 CLKOUT_PCIE_N3
CB4 CB5 CLKOUT_PCIE_P2 CLKOUT_PCIE_N2
WLAN
WLAN_CLK_CPU_P BY4 CLKOUT_PCIE_P1
WLAN_CLK_CPU_N BY3 CLKOUT_PCIE_N1
GPU Gen4
GFX_CLK_CPU_P CN7 CLKOUT_PCIE_P0
GFX_CLK_CPU_N CN8 CLKOUT_PCIE_N0
R18191 60D4R2F-GP XCLK_BIASREF DJ5 XCLK_BIASREF

GPP_F19/SRCCLKREQ6# DU14
GPP_H11/SRCCLKREQ5# DF23 MEM_SPEED_SEL
GPP_H10/SRCCLKREQ4# DG25 CLK_PCIE_NVME_REQ#
GPP_D8/SRCCLKREQ3# DT24
GPP_D7/SRCCLKREQ2# DT30
GPP_D6/SRCCLKREQ1# DV30 CLK_PCIE_WLAN_REQ#
GPP_D5/SRCCLKREQ0# DW30 CLK_PCIE_PEG_REQ#
XTAL_OUT DM1 XTL_38D4M_X2_CPU
XTAL_IN DL1 XTL_38D4M_X1_CPU
GPD8/SUSCLK DW41 SUSCLK
RTCX2 DT47 XTL_32K_X2_CPU
RTCX1 DR47 XTL_32K_X1_CPU
RTCRST# DN37 RTC_RST#
SRTCRST# DK37 SRTC_RST#

20201011
Change RN1805(CHIP NTW 10K J I 4P 1*1) and add R1825 res
3D3V_S0
RN1805 SRN10KJ-5-GP
CLK_PCIE_WLAN_REQ#
CLK_PCIE_NVME_REQ#
CLK_PCIE_PEG_REQ#
R1825 10KR2J-3-GP

20200727
Net name follow GPIO Table.

RTC_AUX_S5
RN1802 SRN20KJ-1-GP
SRTC_RST#
RTC_RST#
G1801 GAP-OPEN
C1803 SC1U10V2KX-1DLGP
C1804 SC1U10V2KX-1DLGP

Layout: Place at the open door area.

XTL_32K_X2_CPU
XTL_32K_X1_CPU
R1811 10MR2J-L-GP
C1802 SC15P50V2JN-DL-GP
X1801 XTAL-32D768KHZ-88-GP
082.30003.0191
2ND = 082.30003.0301
C1801 SC15P50V2JN-DL-GP

XTL_38D4M_X2_CPU
XTL_38D4M_X1_CPU
R1831 33R2J-2-GP
R1832 33R2J-2-GP
R1820 200KR2F-L-GP
XTL_38D4M_X2_CPU_R
XTL_38D4M_X1_CPU_R
X1802 XTAL-38D4MHZ-35-GP
082.30040.0221
2nd = 082.30040.0231
C1806 SC10P50V2JN-4DLGP
C1805 SC10P50V2JN-4DLGP

20201005
Change C1805 and C1806 from 12pF to 10pF Cap.
20201011
EMC request to change R1831/R1832 from 0 to 33 ohm.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: A3
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
Date: Friday, January 29, 2021
Sheet 18 of 106

SSID = PCH

Audio

27,96 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27,96 HDA_SDOUT_CODEC
19,27 HDA_SDI0
15 HDA_SDO
55 DMIC_PCH_CLK_Q
55 DMIC_PCH_DATA_Q

GPU

24,85 DGPU_PWROK
86 DGPU_PWR_EN

G SENSOR

70 FFS_INT2

RTC

25 RTC_DET#

BT

61 BT_RADIO_DIS#

ME

98 ME_FWP_SW

20200728 Remove HDMI_SEL Pin

SIV Auto Test

19,27 HDA_SDI0

R1936 10KR2J-3-GP
DGPU_PWR_EN
OPS
20200430 Add for N18S-G5

1D8V_S5
R1910 1KR1J-GP RTC_DET#
SNDW_RCOMP R1903 200R2F-L-GP

HDA_BITCLK_CODEC R1904 10R2J-2-GP-U HDA_BCLK
HDA_SYNC_CODEC R1901 10R2J-2-GP-U HDA_SYNC
HDA_SDOUT_CODEC R1905 10R2J-2-GP-U HDA_SDO
ME_FWP_SW R1902 1KR1J-GP HDA_SDI0

DMIC_PCH_CLK
DMIC_PCH_DATA
FFS_INT2
DGPU_PWR_EN
BT_RADIO_DIS#
SNDW_RCOMP

20200728 Remove HDMI_SEL Pin

7_OF_21 CPU1G

GPP_D0/HDA_BCLK/I2S0_SCLK
GPP_D1/HDA_SYNC/I2S0_SFRM
GPP_D2/HDA_SDO/I2S0_TXD
GPP_D3/HDA_SDI0/I2S0_RXD
GPP_D4/HDA_RST#
GPP_A7/I2S2_SCLK/DMIC_CLK_A0
GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
GPP_A10/I2S2_RXD/DMIC_DATA1
GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
GPP_A11/PMC_I2C_SDA/I2S3_SCLK
GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
SNDW_RCOMP

GPP_F8_I2S_MCLK2_INOUT
GPP_D19/I2S_MCLK1
GPP_A23/I2S1_SCLK
GPP_R7/I2S1_SFRM
GPP_R6/I2S1_TXD
GPP_R5/HDA_SDI1/I2S1_RXD
GPP_S6/SNDW3_CLK/DMIC_CLK_A0
GPP_S7/SNDW3_DATA/DMIC_DATA0
GPP_S4/SNDW2_CLK/DMIC_CLK_A1
GPP_S5/SNDW2_DATA/DMIC_DATA1
GPP_S2/SNDW1_CLK/DMIC_CLK_B0
GPP_S3/SNDW1_DATA/DMIC_CLK_B1
GPP_S0/SNDW0_CLK
GPP_S1/SNDW0_DATA

DGPU_PWROK
RTC_DET#
TBT_DET#
VRAM_ID1
VRAM_ID2
PROJECT_ID2
PROJECT_ID3

20200728 Remove BOARD_ID1 BOARD_ID2 SEL
20200728 Remove PROJECT_ID1 PROJECT_ID0
2020/09/04 For ETD PCH_VRAM_ID1 change to VRAM_ID1 PCH_VRAM_ID2 change to VRAM_ID2

TGL-U-GP-U1

PROJECT_ID[3:2]

1D8V_S5_VCCPRIM
R1911 Inspiron/Vostro 10KR2J-3-GP PROJECT_ID3
R1912 Latitude 10KR2J-GP
R1913 Inspiron/Latitude 10KR2J-3-GP PROJECT_ID2
R1914 Vostro 10KR2J-3-GP

20200728 Remove PROJECT_ID1 PROJECT_ID0

ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A

R1934 0R1J-GP DY
U1901_2 U1901_4
3D3V_S5
DMIC_PCH_CLK
R1935 0R0402-PAD-7-NP-GP
U1901 M74VHC1GT50DFT1G-GP 73.1GT50.00H
R1930 0R0402-PAD-7-NP-GP
DMIC_PCH_CLK_Q
C1902 SCD1U16V2KX-3DLGP
R1908 1KR1F-GP DY
C1901 SC27P50V2JN-2-GP DY

20200618
Delete PROJECT_ID4 net

20200728
Remove BOARD_ID1 BOARD_ID2 SEL

R1932 0R1J-GP DY
U1902_4 U1902_2
1D8V_S5
R1931 0R0402-PAD-7-NP-GP
U1902 M74VHC1GT50DFT1G-GP 73.1GT50.00H
R1933 0R0402-PAD-7-NP-GP
DMIC_PCH_DATA
DMIC_PCH_DATA_Q
C1903 SC27P50V2JN-2-GP DY
R1929 1KR1F-GP DY
C1904 SCD1U16V2KX-3DLGP

1D8V_S5_VCCPRIM
R1925 UMA 10KR2J-3-GP VRAM_ID2
R1926 2GB VRAM/4GB VRAM 10KR2J-3-GP
R1927 4GB VRAM/UMA 10KR2J-3-GP VRAM_ID1
R1928 2GB VRAM 10KR2J-3-GP

CY19 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

1D8V_S5_VCCPRIM
R1906 NON-TBT 10KR2J-3-GP TBT_DET#
R1907 TBT 10KR2J-3-GP

ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	Non-TBT
		0	TBT

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
Date: Friday, January 29, 2021
Sheet 19 of 106

SSID = PCH

TOUCH PAD/E3

65,66 PCH_I2C1_SCL_TP
65,66 PCH_I2C1_SDA_TP

G SENSOR

70 FFS_INT1
70 ISH_I2C0_ACC_SCL
70 ISH_I2C0_ACC_SDA
70 ISH_ACC1_INT#
70 ISH_ACC2_INT#

AUDIO

24,27 SPKR

KEYBOARD

65 KB_LED_BL_DET

OTHER

24 TABLE_MODE#
24 NB_MODE#

MEMORY

18 MEM_CHA_EN

eDP

55 DBC_PANEL_EN
55 LCD_CBL_DET#

LID

24,67,92 LID_CL_SIO#

UART

68 CPU_UART2_TXD
68 CPU_UART2_RXD

91 TPM_SPI_IRQ#

PCH to BB

75 PCH_I2C_SCL_TBT
75 PCH_I2C_SDA_TBT

20200727
ALS used I2C7

3D3V_VCCDSW

10KR2J-3-GP 1 2 R2001 LCD_CBL_DET#

PAID_L

20200810
Reserve 10K PU for L panel ID.

CPU1F

MEM_CHB_EN
SPKR
TPM_SPI_IRQ#
FFS_INT1
LCD_CBL_DET#
CPU_UART2_TXD
CPU_UART2_RXD
PCH_I2C1_SCL_TP
PCH_I2C1_SDA_TP
DBC_PANEL_EN

GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

TGL-U-GP-U1

20200427
Delete R2004/R2005 0ohm Res.

PCH to Touch Pad / E3
SDA/SCL/INT Pull UP on TP side(page65)
20201011
Delete TBT_I2C_SCL/TBT_I2C_SDA of test point

6 OF 21

GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7
GPP_E15/ISH_GP6
GPP_D18/ISH_GP5
GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP
GPP_T3/I2C7_SCL
GPP_T2/I2C7_SDA
GPP_U5/GSPI3_CLK
GPP_U4/GSPI3_CS0#

KB_LED_BL_DET
ISH_I2C0_ACC_SCL
ISH_I2C0_ACC_SDA
PCH_I2C_SCL_TBT
PCH_I2C_SDA_TBT
ISH_LID_CL#_NB
ISH_TABLE_MODE#
ISH_ACC2_INT#
ISH_ACC1_INT#
GPP_RCOMP

2020/02/06 Modify

3D3V_S0

RN2025
SRN2K2J-1-GP

Accelerometer sensor

Non-TBT

R2003 1 LID_CL_SIO#
0R0402-PAD-7-NP-GP

R2009 1 2 TABLE_MODE#
0R0402-PAD-7-NP-GP

R2021 1 2 200R2F-L-GP

20200727
ALS change used I2C7.
20201011
Remove ALS of I2C PU RN2021.

R2002 1 10KR1J-GP NB_MODE#

Pull high to enable DDR

1D8V_S5 R2031 CHA EN 10KR2J-3-GP
MEM_CHA_EN
R2030 CHA DIS 10KR2J-3-GP

1D8V_S5 R2033 CHB EN 10KR2J-3-GP
MEM_CHB_EN
R2032 CHB DIS 10KR2J-3-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (UART/I2C/ISH)	
Size A3	Document Number MOONKNIGHT_NVL_TGL	Rev X02
Date: Friday, January 29, 2021	Sheet 20 of 106	

SSID = PCH

61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1
61 CNV_WR_CLKN
61 CNV_WR_CLKP

61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1
61 CNV_WT_CLKN
61 CNV_WT_CLKP

61 CNV_BRI_RSP
15 CNV_RGI_DT
61 CNV_RGI_DT_R

61 CNV_BRI_DT_R
61 CNV_RGI_RSP

61 CLKREQ_CNV

61 CNV_RF_RESET#

MEMORY

3 SDRAM_ID4
16 SDRAM_ID5

CPU1J 10 OF 21

D22 CSI_F_DP1
B22 CSI_F_DN1
E22 CSI_F_DP0
D20 CSI_F_DN0
A20 CSI_F_CLK_P
B20 CSI_F_CLK_N

B18 CSI_E_DP1/CSI_F_DP2
A18 CSI_E_DN1/CSI_F_DN2
D18 CSI_E_DP0/CSI_F_DP3
E18 CSI_E_DN0/CSI_F_DN3
C16 CSI_E_CLK_P
D16 CSI_E_CLK_N

D15 CSI_C_DP2
E15 CSI_C_DN2
A15 CSI_C_DP3
B15 CSI_C_DN3

L18 CSI_C_DP1
N18 CSI_C_DN1
L20 CSI_C_DP0
N20 CSI_C_DN0
G20 CSI_C_CLK_P
H20 CSI_C_CLK_N

H16 CSI_B_DP1
G16 CSI_B_DN1
G18 CSI_B_DP0
H18 CSI_B_DN0
L16 CSI_B_CLK_P
N16 CSI_B_CLK_N

G14 CSI_B_DP2
H14 CSI_B_DN2
L14 CSI_B_DP3
N14 CSI_B_DN3

R2103 1 150R2F-1-GP CSI_RCOMP K14 CSI_RCOMP

SDRAM_ID0 DK25 GPP_H23/IMGCLKOUT4
SDRAM_ID1 DM25 GPP_H22/IMGCLKOUT3
SDRAM_ID2 DN25 GPP_H21/IMGCLKOUT2
SDRAM_ID3 DJ25 GPP_H20/IMGCLKOUT1
DR30 GPP_D4/IMGCLKOUT_0/BK4/SBK4

TGL-U-GP-U1

CNVI_WT_D1P DK47 CNV_WT_DP1
CNVI_WT_D1N DM47 CNV_WT_DN1
CNVI_WT_D0P DN49 CNV_WT_DP0
CNVI_WT_D0N DR49 CNV_WT_DN0
CNVI_WT_CLKP DN45 CNV_WT_CLKP
CNVI_WT_CLKN DN47 CNV_WT_CLKN

CNVI_WR_D1P DU43 CNV_WR_DP1
CNVI_WR_D1N DV43 CNV_WR_DN1
CNVI_WR_D0P DR44 CNV_WR_DP0
CNVI_WR_D0N DT43 CNV_WR_DN0
CNVI_WR_CLKP DV44 CNV_WR_CLKP
CNVI_WR_CLKN DW44 CNV_WR_CLKN

CNVI_WT_RCOMP DN51 CNV_WT_RCOMP R2102 1 2 150R2F-1-GP

GPP_F3/CNV_RGI_RSP/UART0_CTS# DJ13 CNV_RGI_RSP
GPP_F2/CNV_RGI_DT/UART0_TXD DG13 CNV_RGI_DT R21101 CNV_RGI_DT_R
GPP_F1/CNV_BRI_RSP/UART0_RXD DF15 CNV_BRI_RSP
GPP_F0/CNV_BRI_DT/UART0_RTS# DF17 CNV_BRI_DT R21111 2 CNV_BRI_DT_R
0R0402-PAD-7-NP-GP
0R0402-PAD-7-NP-GP

GPP_F5/MODEM_CLKREQ/CRF_XTAL_CLKREQ DJ10 CLKREQ_CNV
GPP_F6/CNV_PA_BLANKING DV15
GPP_F4/CNV_RF_RESET# DK18 CNV_RF_RESET#

DRAM Support list

1.Micron:2FG92$CA IC,LP4X,16GB,4266,X32,16G,TGL MT53E512M32D2NP-046 WT:E DRAM 8G;DDP	2.Micron:K7HT2$CA IC,LP4X,32GB,4266,X32,16G,TGL IC SDRAM DDR4 32G MT53E1G32D2NP-046 WT:A DRAM 16G;DDP
3.Samsung:15NY1$AA IC SDRAM LPDDR4X 16GB K4U6E3S4AA-MGCR DRAM 8G;SDP	4.Samsung:K7HT2$AA IC SDRAM LPDDR4X 32GB K4UBE3D4AA-MGCR DRAM 16G;SDP

MEM_CONFIG Mapping table

ID	Description	Setting	Mapping
SDRAM_ID[4:3]	On-board memory configuration for chip vendor	11	DIMM Design
		10	Micron
		01	Hynix
		00	Samsung
SDRAM_ID[2:1]	On-board memory configuration for total memory size per channel	11	32GB
		10	16GB
		01	8GB
		00	4GB

1D8V_S5 R2112 Micron 10KR2J-3-GP SDRAM_ID4 R2113 Samsung/Hynix 10KR2J-3-GP

1D8V_S5 R2114 Hynix 10KR2J-3-GP SDRAM_ID3 R2115 Samsung/Micron 10KR2J-3-GP

1D8V_S5 R2116 16GB/32GB 10KR2J-3-GP SDRAM_ID2 R2117 4GB/8GB 10KR2J-3-GP

1D8V_S5 R2118 8GB/32GB 10KR2J-3-GP SDRAM_ID1 R2119 4GB/16GB 10KR2J-3-GP

2020/09/04
For STD
MEM_CONFIG1 change to SDRAM_ID1
MEM_CONFIG2 change to SDRAM_ID2
MEM_CONFIG3 change to SDRAM_ID3
MEM_CONFIG4 change to SDRAM_ID4

CY19 Board ID Mapping table

ID	Description	Setting	Mapping
SDRAM_ID[5:0]	SDP/DDP/QDP/ODP Configuration	11	ODP
		10	QDP
		01	DDP
		00	SDP

1D8V_S5 R2106 ODP/QDP 10KR2J-3-GP SDRAM_ID5 R2107 SDP/DDP 10KR2J-3-GP

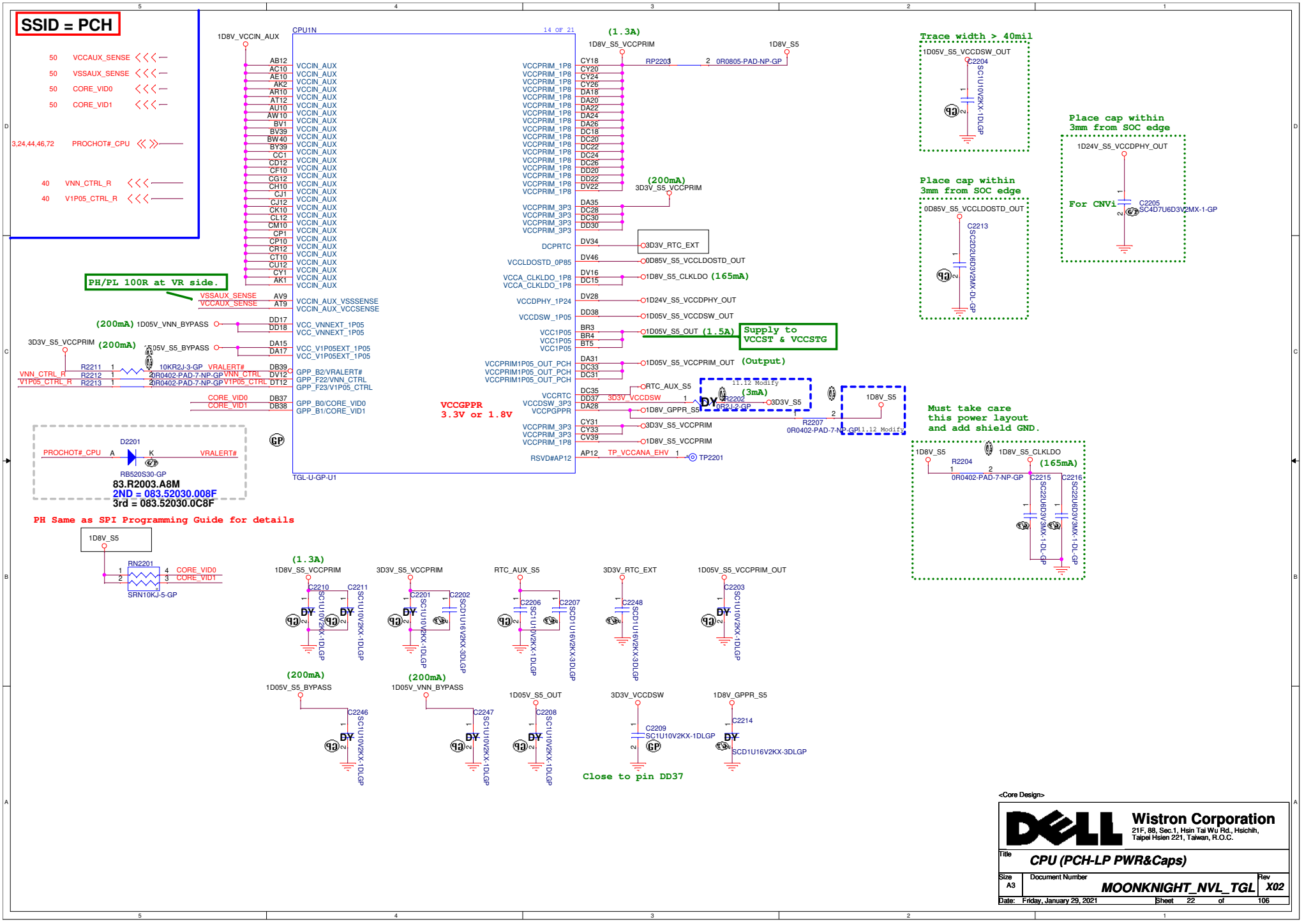
1D8V_S5 R2108 ODP/DDP 10KR2J-3-GP SDRAM_ID0 R2109 SDP/QDP 10KR2J-3-GP

2020/09/04
For STD
MEM_CONFIG0 change net name SDRAM_ID0
MEM_CONFIG5 change net name SDRAM_ID5

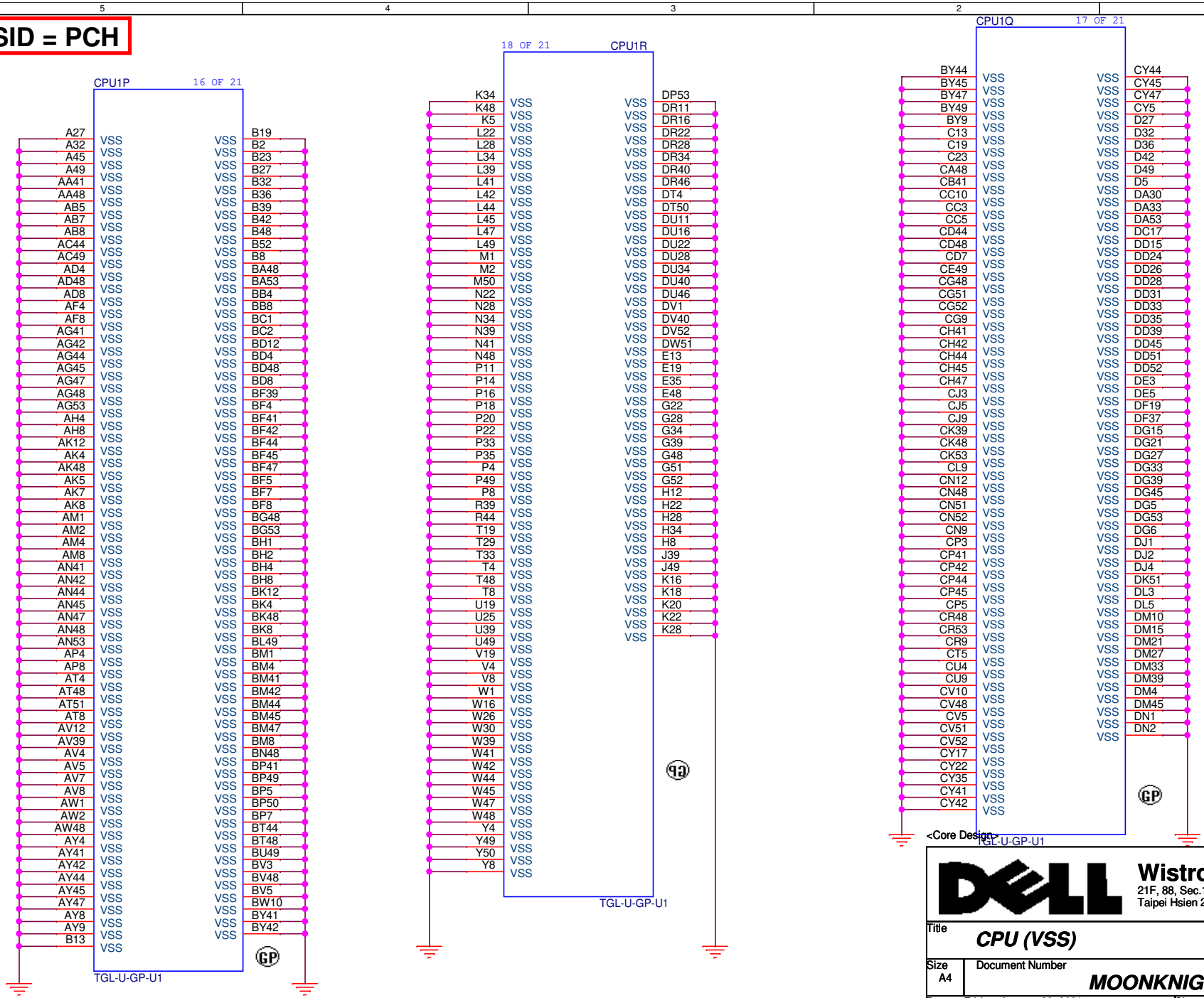
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)
Size: A3 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02
Date: Friday, January 29, 2021 | Sheet 21 of 106


SSID = PCH
50 VCCAUX_SENSE
50 VSSAUX_SENSE
50 CORE_VID0
50 CORE_VID1
3,24,44,46,72 PROCHOT#_CPU
40 VNN_CTRL_R
40 V1P05_CTRL_R
CPU1N
14 OF 21
TGL-U-GP-U1
1D8V_VCCIN_AUX
VCCIN_AUX
VCCIN_AUX_VSSSENSE
VCCIN_AUX_VCCSENSE
VSSAUX_SENSE
VCCAUX_SENSE
PH/PL 100R at VR side.
(200mA) 1D05V_VNN_BYPASS
VCC_VNNEXT_1P05
VCC_V1P05EXT_1P05
3D3V_S5_VCCPRIM (200mA)
1D05V_S5_BYPASS
10KR2J-3-GP
R0402-PAD-7-NP-GP
VRALERT#
VNN_CTRL
V1P05_CTRL
GPP_B2/VRALERT#
GPP_F22/VNN_CTRL
GPP_F23/V1P05_CTRL
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
(1.3A)
1D8V_S5_VCCPRIM
RP2203
0R0805-PAD-NP-GP
1D8V_S5
VCCPRIM_1P8
VCCPRIM_3P3
(200mA)
3D3V_S5_VCCPRIM
DCPRTC
3D3V_RTC_EXT
VCCLDOSTD_0P85
0D85V_S5_VCCLDOSTD_OUT
VCCA_CLKLDO_1P8
VCCA_CLKLDO_1P8
1D8V_S5_CLKLDO (165mA)
VCCDPHY_1P24
1D24V_S5_VCCDPHY_OUT
VCCDSW_1P05
1D05V_S5_VCCDSW_OUT
VCC1P05
1D05V_S5_OUT (1.5A)
Supply to VCCST & VCCSTG
VCCPRIM1P05_OUT_PCH
1D05V_S5_VCCPRIM_OUT (Output)
VCCRTC
RTC_AUX_S5
VCCDSW_3P3
3D3V_VCCDSW
R2202
3D3V_S5
(3mA)
11.12 Modify
R2207
VCCPGPPR
1D8V_GPPR_S5
3.3V or 1.8V
1D8V_S5_VCCPRIM
RSVD#AP12
TP_VCCANA_EHV
TP2201
Trace width > 40mil
1D05V_S5_VCCDSW_OUT
C2204
SC1U10V2KX-1DLGP
Place cap within 3mm from SOC edge
0D85V_S5_VCCLDOSTD_OUT
C2213
SC22U6D3V2MX-DL-GP
Place cap within 3mm from SOC edge
1D24V_S5_VCCDPHY_OUT
For CNVi
C2205
SC4D7U6D3V2MX-1-GP
Must take care this power layout and add shield GND.
1D8V_S5
1D8V_S5_CLKLDO
R2204
0R0402-PAD-7-NP-GP
(165mA)
C2215
C2216
SC22U6D3V3MX-1-DL-GP
D2201
PROCHOT#_CPU
VRALERT#
RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F
PH Same as SPI Programming Guide for details
1D8V_S5
RN2201
CORE_VID0
CORE_VID1
SRN10KJ-5-GP
(1.3A)
1D8V_S5_VCCPRIM
C2210
C2211
SC1U10V2KX-1DLGP
3D3V_S5_VCCPRIM
C2201
C2202
SCD1U16V2KX-3DLGP
RTC_AUX_S5
C2206
C2207
SCD1U16V2KX-3DLGP
3D3V_RTC_EXT
C2248
1D05V_S5_VCCPRIM_OUT
C2203
(200mA)
1D05V_S5_BYPASS
C2246
(200mA)
1D05V_VNN_BYPASS
C2247
1D05V_S5_OUT
C2208
3D3V_VCCDSW
C2209
SC1U10V2KX-1DLGP
1D8V_GPPR_S5
C2214
SCD1U16V2KX-3DLGP
Close to pin DD37
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCH-LP PWR&Caps)
Size A3
Document Number
MOONKNIGHT_NVL_TGL
Rev X02
Date: Friday, January 29, 2021
Sheet 22 of 106

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CPU (VSS)***	
Size: A4	Document Number: ***MOONKNIGHT_NVL_TGL***	Rev: ***X02***
Date: Friday, January 29, 2021	Sheet 23 of 106	

SSID = KBC

BOARD_ID VERSION A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Mooonknight_X00	100.0K	10.0K	3.0V
Mooonknight_X01	100.0K	17.8K	2.801V
Mooonknight_X02	100.0K	27.0K	2.598V
Mooonknight_A00	100.0K	37.4K	2.402V
Mooonknight_X03	100.0K	49.9K	2.201V
Mooonknight_X04	100.0K	64.9K	2.001V
Mooonknight_A02	100.0K	82.5K	1.805V
Mooonknight_A01	100.0K	107K	1.594V
Mooonknight_A02	100.0K	154K	1.299V
Mooonknight_A03	100.0K	200K	1.100V

MODEL_ID_DET (GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
N UMA	100.0K	10.0K	3.0V
V UMA	100.0K	17.8K	2.801V
L UMA	100.0K	27.0K	2.598V
TBD	100.0K	37.4K	2.402V
N DIS	100.0K	49.9K	2.201V
V DIS	100.0K	64.9K	2.001V
TBD	100.0K	82.5K	1.805V
TBD	100.0K	107K	1.594V
TBD	100.0K	154K	1.299V
TBD	100.0K	200K	1.100V

Added Second Fan, MET NVL 13 EIV, 2020/02/26

EC to TBT/TP

SIV Auto Test

RTC GEN 9 reset circuit

Power Switch Logic (PSL)

Layout Note:

Modified, MET NVL 13 EIV, 2020/03/24

Modified, MET NVL 13 EIV, 2020/03/24

For eSPI

For G3 Flash Share

For eSPI

BATTER /CHARGER
CPU/ Thermal/TYPEC

20201210
R2401change from 27K to 37.4K for A00.

20200724
Remove C2415 C2421 for Placement.
R2246 Change to 0402 size for Placement
20201011
Delete C2415

20200727
Add a 100K to GND PD resistor
at PCH_RSMRST# to pre-set this GPIO pin low initially..

20200716
Add TYPEC_DCIN2_EN# net to control Q7409 Q7410

20200903
SUS_CLK_PCH add U2403 OSC option

20200819
Layout Swap.

20200805
Remove TBT_EC_GPIO.

20200817
Follow Shuri Cyborg R2468 change to stuff.
Follow Shuri Cyborg R2467 change to DY.

20200820
GPIO202 change from I_BATT to SIO_SLP_SUS#

20200805
SIO_PWRBTN# connect to 3DV_S5_VCCPRIM

2020/08/19
Only 32MB ROM part remove CS1

2020/08/19
Only 32MB ROM part remove CS1

Wistron Corporation	21F, 88, Sec 2, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC Nuvoton MEC1515
Size	A3
Document Number	MOONKNIGHT_NVL_TGL
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Date	Friday, January 31, 2020
Sheet	34 of 100

Main Func = SPI Flash

15,18,24,91 SPI0_SI_CPU
18,24,91 SPI0_SO_CPU
18,24,91 SPI0_CLK_CPU
15,18,24 SPI0_WP_CPU
15,18,24 SPI0_HOLD_CPU
18,24,25 SPI0_CS_ROM_N0

25,96 SPI_CLK_ROM_R

SIV Auto Test
25,96 SPI_CLK_ROM_R
18,24,25 SPI0_CS_ROM_N0

SPI Flash BIOS3(32M) only.

3D3V_S5 R2501 0R0402-PAD-7-NP-GP 3D3V_SPI
20200513 Add 0ohm Res.

3D3V_SPI R2519 4K7R2J-2-GP

BIOS_NV 32M W25Q256JVEIQ-GP
SPI0_SO_CPU R2506 1 22R2J-2-GP SPI_SO_HOLD_R
SPI0_WP_CPU R2507 1 22R2J-2-GP SPI_WP_HOLD_R
SPI0_CS_ROM_N0 SPI_CS_ROM_R
CS# VCC DO/IO1 IO3 IO2 CLK GND DI/IO0 GND
SPI_HOLD_ROM_R R2503 1 22R2J-2-GP SPI0_HOLD_CPU
SPI_CLK_ROM_R R2508 1 22R2J-2-GP SPI0_CLK_CPU
SPI_SI_ROM_R R2509 1 22R2J-2-GP SPI0_SI_CPU

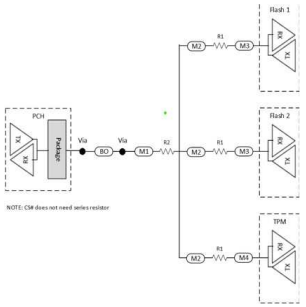
072.25256.0N01
2nd = 072.25256.0G03

3D3V_SPI C2501 SC1U16V2KX-1DLGP

BIOS_L 32M W25R256JVEIQ-GP
SPI0_CS_ROM_N0 SPI_CS_ROM_R
SPI_SO_ROM_R SPI_HOLD_ROM_R
SPI_WP_HOLD_R SPI_CLK_HOLM_R
SPI_SI_ROM_R

072.25256.0L01
2nd = 072.77256.M002
3rd = 072.25256.M007

Remove SPI ROM socket, MKT NVL 13 EIV, 2020/04/07



Main Func = RTC

24 RTCRST_ON
24 VCCDSW_EN
17,24,45 3V_5V_PWRGD
19 RTC_DET#

Delivery Voltage 3.19V

TP2508 RTC_VCC_C
TP2507

+RTC_VCC R2510 External_RTC 1KR2J-1-GP
External_RTC RTC1 RTC_VCC_C
ETY CON2-22-GP-U
20.F1841.002
2ND = 20.F1639.002

+RTC_VCC R2512 0R2J-2-GP External_RTC
BATT_RTC_R R2513 0R2J-2-GP Internal_RTC

3D3V_AUX_S5 D2501 A K RB520S30-GP
RTC_VCC_R D2502 A K RB520S30-GP C2503 SCD1U16V2KX-3DLGP
3rd = 083.52030.0C8F
2ND = 083.52030.008F
83.R2003.A8M

83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

Q2505 2N7002K-2-GP-U
R2504 10MR2J-L-GP
RTC_DET#
84.2N702.J31
2ND = 084.27002.0N31

20200803
Co-Lay External RTC and internal RTC solution.

3D3V_RTC Q2507 PJA3415AE-GP
RTC_AUX_S5
084.03415.0C31

R2511 4K7R2J-2-GP
RTC_3P3_EN_D
Q2510 2N7002K-2-GP-U
84.2N702.J31
2ND = 084.27002.0N31

RTCRST_ON R2567 1 1MR2J-1-GP RTC_3P3_EN_G
R2518 100KR2J-1-GP
C2517 SCD022U16V2KX-3DLGP

3D3V_S5 R2520 100KR2J-1-GP
VCCDSW_EN
3V_5V_PWRGD D2503 BAT54A-11-GP
75.BAT54.07D
2ND = 075.00054.0A7D
3RD = 075.00054.0Z7D

3D3V_S5 R2514 10KR2J-3-GP
3V_5V_DSW_OK

U2502 APL3553ABI-TRG-GP
EN OC# GND VOUT VIN
3D3V_S5

3D3V_VCCDSW R2521 0R0402-PAD-7-NP-GP 3D3V_S5_VCCPRIM

074.03553.007F
2ND = 074.51712.009F
3RD = 074.09742.0A9F

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02
Date: Friday, January 29, 2021 | Sheet 25 of 106

Main Func = Thermal Sensor

18,24,79 EC_I2C_SCL_THM
18,24,79 EC_I2C_SDA_THM
17,24 IMVP_VR_ON
40 PURE_HW_SHUTDOWN#

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

3D3V_S0
RP2601 0R0402-PAD-7-NP-GP
3D3V_THM
20201011
Change RP2601 to 0402 size.
C2602 SCD1U16V2KX-3DLGP
R2604 10K5R2F-GP
R2603 7K5R2F-1-GP
RN2602 SRN2K2J-1-GP
U2601
VDD SCL
D+ SDA
D- ALERT#
T_CRIT# GND
NCT7718W-GP
74.07718.0B9
2ND = 074.00788.00B9
NCT7718_DXP
NCT7718_DXN
C2606 SC470P50V2KX-3DLGP
C2607 SC2200P50V2KX-2DLGP
DY
Q2603 LMBT3904LT1G-GP
84.T3904.H11
2ND = 084.03904.0I11
3RD = 084.03904.0H11
R2601 0R0402-PAD-7-NP-GP
T_CRIT#
ALERT#
CPU_SMB_SCL_THM
CPU_SMB_SDA_THM
Q2601
2N7002KDW-1-GP
75.27002.F7C
EC_I2C_SDA_THM
EC_I2C_SCL_THM
20201011
Delete reserve C2608 and C2609 Cap
Layout Note:
1. System sensor put on palm rest.
2. C2607 close U2601.
3. Both DXN and DXP routing 10 mil trace width and 10 mil spacing.
Q2602
IMVP_VR_ON
THERM_SYS_SHDN#
PURE_HW_SHUTDOWN#
C2610 SCD1U16V2KX-3DLGP
2N7002K-2-GP-U
84.2N702.J31
2ND = 084.27002.0N31

Main Func = Thermal Sensor

24 PWM_FAN1
24 FAN_TACH1
24 PWM_FAN2
24 FAN_TACH2

Added Second Fan, MKT NVL 13 EIV, 2020/02/26

Layout Note:
5V_FAN1_VCC: Trace width = 15mil
5V_S0 RP2602 0R0402-PAD-7-NP-GP
5V_FAN1_VCC
Change to 0402 OR 2020/0708
C2604 SC4D7U6D3V2MX-1-GP
C2605 SCD1U16V2KX-3DLGP
FAN1
FAN_TACH1
PWM_FAN1
TP2604
ACES-CON4-96-GP
020.F001A.0004
2ND = 020.F1274.0004
TP2603
TP2601
5V_FAN1_VCC
FAN_TACH1

Layout Note:
5V_FAN2_VCC: Trace width = 15mil
5V_S0 RP2603 0R0402-PAD-7-NP-GP
5V_FAN2_VCC
Change to 0402 OR 2020/0708
C2611 SC4D7U6D3V2MX-1-GP
C2612 SCD1U16V2KX-3DLGP
FAN2
FAN_TACH2
PWM_FAN2
TP2607
ACES-CON4-29-GP
20.F1639.004
2ND = 020.F0097.0004
TP2606
TP2605
5V_FAN2_VCC
FAN_TACH2

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A3
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
Date: Friday, January 29, 2021
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Main Func = Audio

Audio Codec Chip ALC3204

19 HDA_SDI0
7,96 HDA_SDOUT_CODEC
7,96 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC
29 AUD_SPK_R+
29 AUD_SPK_R-
29 AUD_SPK_L+
29 AUD_SPK_L-
55 DMIC_SCL_CODEC
55 DMIC_SDA_CODEC
66 AUD_SENSE
24 NB_MUTE#
20,24 SPKR
24 BEEP
29,66 AUD_RING
29,66 AUD_SLEEVE
29 LINE1_L
29 LINE1_R
29 LINE1_VREFO
29 MIC2_VREFO_R
29,66 AUD_HP1_JACK_L
29,66 AUD_HP1_JACK_R

5V_S0 RP2701 0R0805-PAD-NP-GP +5V_PVDD

1D8V_S0 RP2709 0R0402-PAD-7-NP-GP 1D8V_CPVDD

20201011
Change RP2709 to 0402 size.

20201011
Change RP2703 to 0402 size.

moat Analog Digital

1.8V power rail should be supplied by linear regulator, not awitching regulator.if switch regulator is uvilable, please make sure that switch requency operates at out-band(over 20KHz)

1D8V_S0 R2719 0R0402-PAD-7-NP-GP C2710 SC10U6D3V3MX-DL-GP AUD_AGND

+5V_PVDD >2A

SIV Auto Test

DVDD must >= DVDD_IO

1D8V_S0 RP2715 0R0402-PAD-7-NP-GP 1D8V_DVDD

20201011
Change RP2715 to 0402 size.

3D3V_S0 RP2725 0R0402-PAD-7-NP-GP DVDD_R

20201011
Change RP2725 to 0402 size.

place close to pin1

20200715
C2720 Change to 0603 Common part

SPKR BEEP D2703 BAT54C-12-GP 75.00054.A7D
AUD_PC_BEEP_C C2735 SCD1U16V2KX-3DLGP AUD_PC_BEEP
R2735 1KR2J-1-GP C2739 SC100P50V2JN-3DLGP

Open drain output. pull up to DVDD or max. 5V
For RTC Gen9 reset circuit change power rail. 20170921
3D3V_RTC R2708 0R0402-PAD-7-NP-GP V3D3_STB
3D3V_S0 R2716 DY 100KR2J-1-GP DVSS

HDA_SDI0 R2724 0R0402-PAD-7-NP-GP HDA_CODEC_SDIN0
HDA_BITCLK_CODEC R2723 22R2J-2-GP HDA_BITCLK_CODEC_R

20200819
Follow Shuri Change R2723 from 0 to 22 ohm.

3D3V_S0 R2717 100KR2J-1-GP 20180911 Vendor stuff
NB_MUTE#

3D3V_S0 R2710 100KR2J-1-GP
AUD_SENSE R2711 200KR2F-1-GP AUD_HPJD_N

AUD_HP1_JACK_L
AUD_HP1_JACK_R

1D8V_CPVDD C2705 SC2D2U6D3V2MX-DL-GP C2704 SCD1U16V2KX-3DLGP
C2708 SC2D2U10V3KX-1DLGP C2709 SC2D2U10V3KX-1DLGP

U2701 ALC3204 QFN40 (5X5) 071.03204.0003

30	CBP		
29	CPVDD		
28	CBN		
27	CPVEE		
26	HP-OUT-R		
25	HP-OUT-L		
24	LINE1-VREFO-L		
23	MIC2-VREFO		
22	VREF		
21	LDO1-CAP		
31	AVSS2		
32	LDO2-CAP		
33	AVDD2		
34	PVDD1		
35	SPK-L+		
36	SPK-L-		
37	SPK-R-		
38	SPK-R+		
39	PVDD2		
40	PDB		
41	GND		
1	DVDD		
2	GPIO0/DMIC-DATA12		
3	GPIO1/DMIC-CLK		
4	SDATA-OUT		
5	BIT-CLK		
6	LDO3-CAP		
7	SDATA-IN		
8	DVDD-IO		
9	SYNC		
10	DC_DET		
20	AVDD1		
19	AVSS1		
18	LINE1-L		
17	LINE1-R		
16	VD33STB		
15	MIC2-CAP		
14	SLEEV/MIC2-R		
13	RING2/MIC2-L		
12	HP/LINE1-JD_JD1		
11	PCBEEP		

ALC3204-CG-GP

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_L+ AUD_SPK_L- AUD_SPK_R- AUD_SPK_R+

AUD_AGND C2702 SC2D2U6D3V2MX-DL-GP C2703 SC2D2U6D3V2MX-DL-GP R2702 100KR2J-1-GP

+5V_AVDD RP2703 0R0402-PAD-7-NP-GP 5V_S0
C2707 SC10U6D3V3MX-DL-GP C2706 SCD1U16V2KX-3DLGP

Layout Note:
Place close to Pin 20

C2715 SC10U6D3V3MX-DL-GP

Analog Digital moat

place close to pin8

C2723 SC4D7U6D3V2MX-1-GP
C2722 SC10U6D3V3MX-DL-GP

Azalia I/F EMI

HDA_SDOUT_CODEC EC2709 SC22P50V2JN-4DLGP
HDA_BITCLK_CODEC EC2710 SC22P50V2JN-4DLGP
DMIC_SDA_CODEC EC2711 DY SC22P50V2JN-4DLGP
DMIC_SCL_CODEC EC2706 DY SC33P50V2JN-3DLGP

moat 20180904 EMC modify
EC2701 EC2702 EC2703 EC2704 EC2705 SC1KP50V2KX-1DLGP
AUD_AGND

R2704 R2705 R2706 0R0603-PAD-7-NP-GP
AUD_AGND

Layout Note:
Tied at point only under Codec or near the Codec

20200522
Vendor suggest:
1.EC2711 DY that use PCH DMIC.
2.EC2710, EC2709 should be place nearby PCH
<Core Design>

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Title: Audio Codec ALC3204
Size: A3 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02
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<Core Design>

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Title: *(Reserved)*

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Main Func = Audio

27 AUD_SPK_R+
27 AUD_SPK_R-
27 AUD_SPK_L-
27 AUD_SPK_L+

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_R+ ER2901 1 — 2 0R0603-PAD-7-NP-GP — AUD_SPK_R+_C 1
AUD_SPK_R- ER2902 1 — 2 0R0603-PAD-7-NP-GP — AUD_SPK_R-_C 2
AUD_SPK_L+ ER2903 1 — 2 0R0603-PAD-7-NP-GP — AUD_SPK_L+_C 3
AUD_SPK_L- ER2904 1 — 2 0R0603-PAD-7-NP-GP — AUD_SPK_L-_C 4

SPK1
ACES-CON4-29-GP
20.F1639.004
2ND = 020.F0097.0004

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

EC2902 SC1KP50V2KX-1DLGP
EC2901 SC1KP50V2KX-1DLGP
EC2903 SC1KP50V2KX-1DLGP
EC2904 SC1KP50V2KX-1DLGP
20180911
Vendor modify

AUD_SPK_L-_C 1
AUD_SPK_L+_C 1
AUD_SPK_R-_C 1
AUD_SPK_R+_C 1
TP2901
TP2902
TP2903
TP2904

27 LINE1_L
27,66 AUD_HP1_JACK_L
27 LINE1_VREFO
27,66 AUD_HP1_JACK_R
27 LINE1_R

27 MIC2_VREFO_R
27,66 AUD_SLEEVE
27,66 AUD_RING

LINE1_L C2907 1 — SC10U6D3V3MX-DLI-GP — AUD_HP1_JACK_L
20200721 Cyborg 4.7K.
20200721 Cyborg 10K.

D2901
LINE1_VREFO 3
75.00056.07D
BAW56-9-GP-U
LINE1_VREFO_L 1
LINE1_VREFO_R 2
RN2902
SRN4K7J-8-GP
2ND = 075.00056.0A7D
3rd = 075.00056.0B7D
20200721 Cyborg 10K.

AUD_HP1_JACK_R
LINE1_R C2908 1 — SC10U6D3V3MX-DLI-GP
20200721 Cyborg 4.7K.
RN2901
SRN2K2J-1-GP
MIC2_VREFO_R
AUD_RING
AUD_SLEEVE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Audio IO
Size: A4
Document Number: MOONKNIGHT_NVL_TGL
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<Core Design>

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Title: *(Reserved)*

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

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<Core Design>

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Title

(Reserved)

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<Core Design>

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Title: *(Reserved)*		
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<Core Design>

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Title

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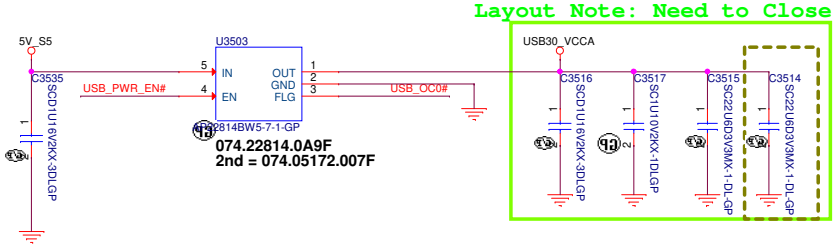
Main Func = USB 3.1 Gen1

16 USB_OC0#
24 USB_PWR_EN#

USB3.1 Port (IO Board)

Layout Note: Need to Close CON



20200721
C3514 change to mount.

<Core Design>

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Title	USB3.1 IO Power	
Size A3	Document Number MOONKNIGHT_NVL_TGL	Rev X02
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<Core Design>

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Title
USB30

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<Core Design>

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Title
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<Core Design>

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Title: *(Reserved)*

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<Core Design>

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Title
(Reserved)

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SSID = Power Plane & Sequence

17,92 SIO_SLP_S4#
17,55 SIO_SLP_S3#
17,24 SIO_SLP_SUS#

17 CPU_C10_GATE#
24 ALWON
26 PURE_HW_SHUTDOWN#

17 VCCST_OVERRIDE
17,24,46 ALL_SYS_PWRGD

53 PWR_1D8V_EN
50,53 PWR_1D8V_PG
17,24,50 VCCIN_AUX_PWRGD

45 3V_5V_EN
22 V1P05_CTRL_R
22 VNN_CTRL_R

51 PWR_VDD_EN
51 VDDQ_EN
51 PWR_VDDQ_PG

54 PWR_VNN1D05V_VID2
54 PWR_VNN1D05V_VID1
54 PWR_VNN1D05V_PG
54 PWR_1D05V_EN
54 PWR_VNN_EN

RUN Power

5V_S0

5V_S0 Comsumption
Peak current 5A

U4006 TPS22975-GP
074.22975.0093
2ND = 74.03526.093

6A/Rds(on):4.5mOhm/Tr:7~20us

U4001 G5027CRD1D-GP-U
074.05027.0B93
2ND = 074.05201.0A93

(1200mA)

150mA

Q4003 PJA3415AE-GP
084.03415.0C31

Q4004 2N7002K-2-GP-U
84.2N702.J31
2ND = 084.27002.0N31

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

U4009 TPS22975-GP
074.22975.0093
2ND = 74.03526.093

6A/Rds(on):4.5mOhm/Tr:7~20us

U4002 G5027CRD1D-GP-U
074.05027.0B93
2ND = 074.05201.0A93

(300mA)

2020/04/20
Remove it's non-use ES1 CPU.

Power Sequence / Pull High PWRGD

Q4002 PJA138KA-GP
084.00138.0A31
2ND = 84.05067.031

Q4001 2N7002K-2-GP-U
84.2N702.J31
2ND = 084.27002.0N31

83.R2004.G8F
2ND = 83.00751.08F

NON-BYPASS

BYPASS

1D05V_BYPASS_CTRL

PM_SLP_S3#

3rd = 083.52030.0C8F
2ND = 083.52030.008F
83.R2003.A8M

For LPDDR4x only: 0D6V_S3 Power on to after 1D1V_S3

For PWR_VDDQ_EN RC delay
Layout Note:Place Close to PU5101

20200728
Remove R4048 R4047 U4010 DSW property component.

20200728
Remove R4025 DSW property component.

83.00355.G1F

20200305(DVT1)
For customer request

20200803
Remove customer request circuit.

<Core Design>

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Title: Sequence (Power Plane Enable)
Size: A2
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<Core Design>

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Title
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<Core Design>

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Title: *(Reserved)*

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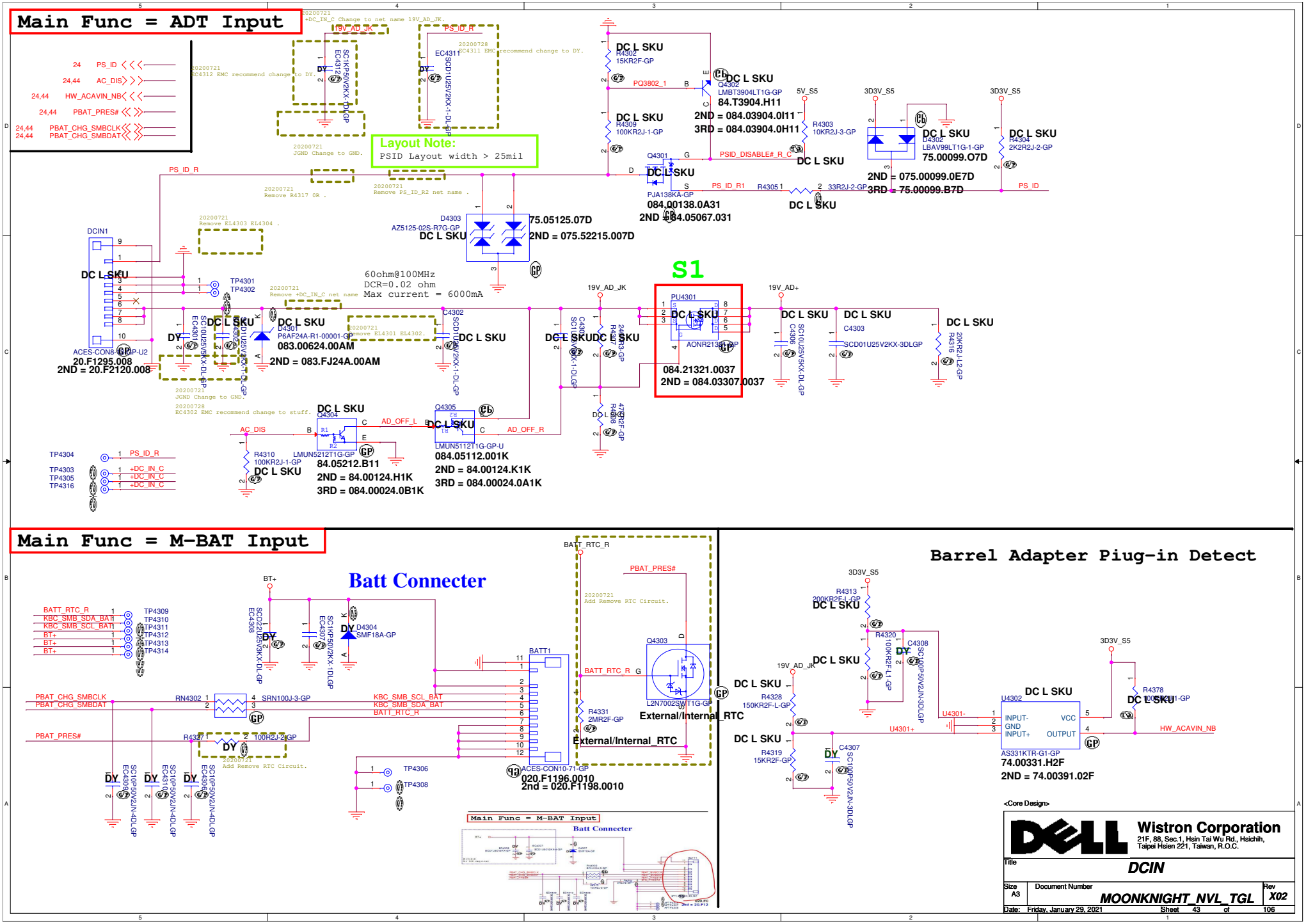
Main Func = ADT Input
Layout Note:
PSID Layout width > 25mil
S1
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA
Main Func = M-BAT Input
Batt Connecter
Barrel Adapter Piug-in Detect
External/Internal_RTC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!!

PBAT_CHG_SMBDAT
PBAT_CHG_SMBCLK
HW_ACAV_IN
AC_INT
GPU_PWR_LEVEL
PWR_CHG_ADA
PBAT_PRSN
AC_DIS
HW_ACAVIN_NB
PWR_CHG_PROCHOT#_CPU
PWR_CHG_CSOP_R
PWR_CHG_CSON_R
PWR_CORE_PSYS
ALL_SYS_PWRGD
PWR_VCORE_VR_READY
PWR_VGA_NVVDDS_EN
PWR_VGA_NVVDDS_PG
VCCPO1A_VBUS_FLTR

S2

084.21321.0037

084.21319.0031
2nd = 084.02425.0031

75.27002.F7C

83.R2003.A8M
2nd = 083.52030.008F

10*11.2*3
DCR=8~9 mohm
Idc=13A, Isats=16A
2nd = 68.2R21F.10V
068.2R10.2351

075.07321.0073
2nd = 075.36304.0073
3rd = 075.00018.0A73

074.09538.0C73

External_RTC

84.27002.J31
2nd = 084.27002.0M31

Modified, MBT NVL 13 EVT, 2020/03/30

TypeC Layout.2 TypeC Layout Barrel Layout

+3D3V_VDD_DCIN

75.00054.A7G

074.02025.000F
2nd = 074.02925.000F

Vout=1.24*(1+(R1/R2))

Vcore_OVP

Charger LDO

74.00331.H2F

83.00355.G1F

Location	Gen11	Gen10
PR44J0	DY	Stuff
PR44J6	DY	Stuff
PR44J7	DY	Stuff
PR44J8	DY	Stuff
PC44D0	Stuff	DY
PC44D1	Stuff	DY
PC44D1	Stuff	DY
PR44D0	Stuff	DY
PR44D1	Stuff	DY
PR44D2	Stuff	DY
PR44D3	Stuff	DY
PR44D4	Stuff	DY
PR44D5	Stuff	DY
PR44D7	Stuff	Stuff
PR44D8	Stuff	Stuff
PR44D9	DY	DY
PC44D0	Stuff	Stuff

If need to use battery internal LDO, please help to follow below table to modify.

	PR4434	PC4430	PR4436	EC to ken "SUPPORT_3VLDO_AS_BATTPRES"
Coin cell battery	DY	Stuff	Stuff	Disable
Battery internal LDO	Stuff	DY	DY	Enable

23	SUPPORT_3VLDO_AS_BATTPRES	[Code comment] Set true for enable support used 3VLDO as battery present pin. [Wistron EC] If battery present pin signal is from battery RTC power but coin battery, EC will not get battery present if battery is over discharging. Stradale set True, Bandon/Bandon_MLK set faslse. Depend on HW design. CHARGER_OUT_VOLTAGE_AC_ONLY must be larger than charger MINIMUM_VOLTAGE(0x3E) value.	

Barrel Prochot

Follow custormer circuits.

TypeC Prochot

Follow custormer circuits.

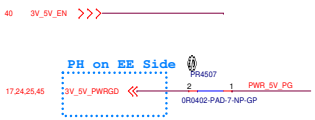
TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLim(1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	No	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

Wistron Corporation
Power (Charger ISL9538)
MOONKNIGHT_NVL_TGL

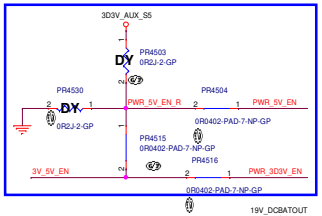
SSID = PWR.Plane.Regulator_5V

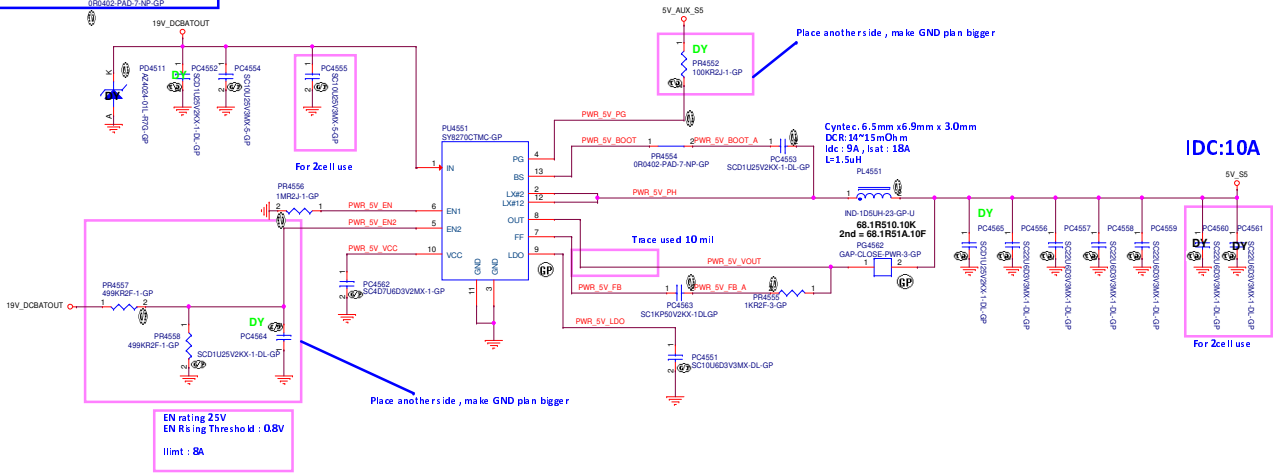
OFFPAGE-Signal



OFFPAGE-GAP

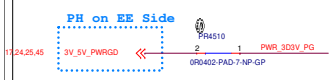
SY8270C For 5V



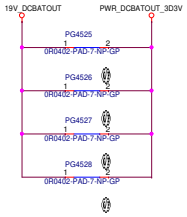


SSID = PWR.Plane.Regulator_3D3V

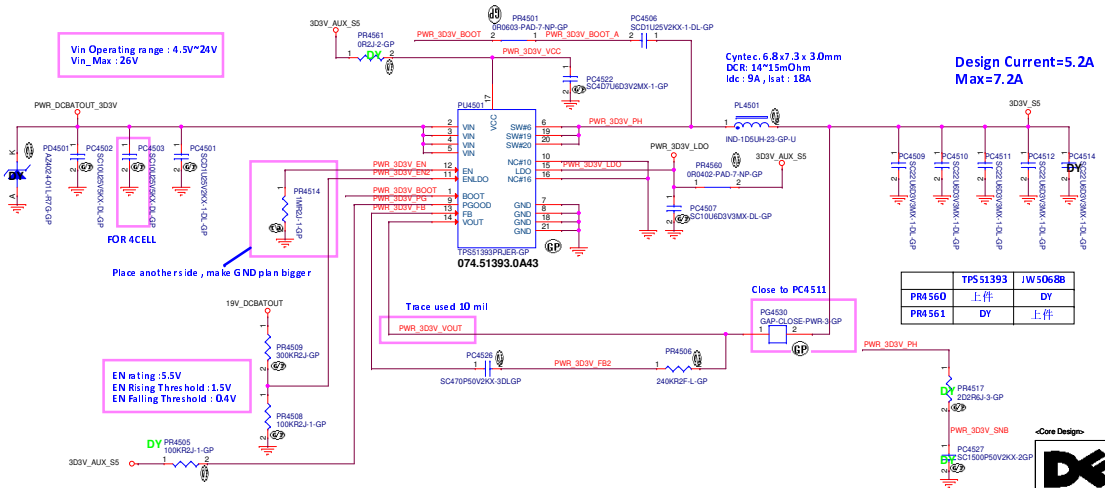
OFFPAGE-Signal



OFFPAGE-GAP



TPS51393 For 3D3V



	TPS51393	JW5068B
PR4560	上件	DY
PR4561	DY	上件

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Title: POWER (SY8288_5V/3D3V)

Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 29, 2021 | Sheet 45 of 106

Main Func = CPU_CORE

OFFPAGE

SVID

- SVID_CLK_CPU (7) — PR4632 0R0402-PAD-7-NP-GP — PWR_VCORE_SCLK_R
- SVID_DATA_CPU (7) — PR4633 0R0402-PAD-7-NP-GP — PWR_VCORE_SDIO_R
- SVID_ALERT#_CPU (7) — PR4634 0R0402-PAD-7-NP-GP — PWR_VCORE_ALERT#_R

- PROCHOT#_CPU (22,24,44,72) — PR4631 0R0402-PAD-7-NP-GP — PWR_VCORE_VRHOT_R
- PWR_CORE_PSYS (44) — PWR_CORE_PSYS
- PWR_VCORE_VR_READY (17) — PR4636 0R0402-PAD-7-NP-GP — PWR_VCORE_VR_READY
- ALL_SYS_PWRGD (7,24,40) — PR4635 0R0402-PAD-7-NP-GP — PWR_VCORE_VR_EN

VCORE SENSE

- VSSCORE_SENSE (7) — VSSCORE_SENSE
- VCCCORE_SENSE (7) — VCCCORE_SENSE

- PWR_VCORE_UGATE1 (47)
- PWR_VCORE_PHASE1 (47)
- PWR_VCORE_LGATE1 (47)
- PWR_VCORE_UGATE2 (47)
- PWR_VCORE_PHASE2 (47)
- PWR_VCORE_LGATE2 (47)
- PWR_VCORE_ISEN2 (47)
- PWR_VCORE_ISEN1 (47)
- PWR_VCORE_ISUMP (47)
- PWR_VCORE_ISUMN (47)

1D05V_VCCST

PR4603 1KR2F-3-GP

PR4607 100R2F-L1-GP-U

PWR_VCORE_VRHOT_R

3D3V_S0

PR4609 10KR2F-2-GP

PWR_VCORE_VR_READY

PWR_VCORE_VR_EN

PC4612 SC4700P50V2KX-1DLGP

PR4602 12K1R2F-L1-GP-U

PC4609 SC330P50V2KX-3-DL-GP

PR4608 93K1R2F-L-GP

PU4601 ISL95869HRTZ-T-GP 074.95869.0073

PWR_CORE_PSYS
PWR_VCORE_IMON
PWR_VCORE_NTC
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RTN
PWR_VCORE_ISUMNT

PSYS IMON NTC COMP FB RTN ISUMN ISUMP

VR_ENABLE VR_READY VR_HOT# SCLK SDIO ALERT# VDD5 VIN GND

PROG1 PROG2 BOOT1 UGATE1 PHASE1 LGATE1 PWM3 VDDP

PWR_VCORE_PROG1
PWR_VCORE_PROG2
PWR_VCORE_BOOT1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_VCORE_LGATE1
PWR_VCORE_VDDP

ISEN1 ISEN2 ISEN3 BOOT2 UGATE2 PHASE2 LGATE2

PWR_VCORE_BOOT2
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_VCORE_LGATE2

PR4619 78K7R2F-GP

PR4620 9K31R2F-GP

PROG1
VBOOT:0V
F=750kHz

PR4621 0R0603-PAD-7-NP-GP — PWR_VCORE_BOOT1_N — PC4610 SCD22U25V2KX-4-GP

PR4625 0R0402-PAD-7-NP-GP — o5V_S5

PC4625 SC1U10V2KKX-1DLGP

PR4611 0R0603-PAD-7-NP-GP — PWR_VCORE_BOOT2_N — PC4611 SCD22U25V2KX-4-GP

PR4616 10KR2F-2-GP

PWR_VCORE_NTC_N

PR4618 47K4R2F-4-GP — B=4500

PR4655 27K4R2F-GP

2nd = 069.60006.0001

PR4615 1K5R2F-2-GP

PC4608 SC82P50V2JN-3-DL-GP

PWR_VCORE_COMP_N

PR4614 2KR2F-3-GP

PR4613 392R2F-GP

PR4612 392R2F-GP

PC4607 SC220P50V2KX-3DLGP

PC4606 SC220P50V2KX-3DLGP

PWR_VCORE_FB1

PWR_VCORE_FB4

PWR_VCORE_FB2

PC4604 SC330P50V2KX-1-DL-GP

VCCCORE_SENSE

PR4667 0R0402-PAD-7-NP-GP

PR4640 100R2F-L1-GP-U

1V_CPU_CORE

PWR_VCORE_FB3

PR4665 0R0402-PAD-7-NP-GP

PC4605 SC330P50V2KX-3-DL-GP

PC4615 SCD01U25V2KX-3DLGP

PR4666 0R0402-PAD-7-NP-GP

VSSCORE_SENSE

PC4638 SC330P50V2KX-3-DL-GP

PR4626 100R2F-L1-GP-U

PR4627 511R2F-2-GP

PC4623 SC2200P50V2KX-2DLGP

PWR_VCORE_ISUMN_N

PR4628 3K48R2F-GP

PC4614 SCD22U25V2KX-3DLGP

PC4618 SCD22U25V2KX-3DLGP

PWR_VCORE_ISUMP_N

PR4629 0R0402-PAD-7-NP-GP

PC4616 SC2200P50V2KX-2DLGP

PC4602 SCD01U25V2KX-3DLGP

PR4630 11KR2F-L-GP

PR4653 2K61R2F-1-GP

PR4650 NTC-10K-29-GP-U 69.60011.201 — B=3370

2nd = 69.60013.131

PC4603 SCD01U25V2KX-3DLGP

PWR_VCORE_ISEN2
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP
PWR_VCORE_ISUMNP_2
PWR_VCORE_ISUMN

PC4626 SCD1U25V2KX-1-DL-GP

Close to IC

5V_S5

PR4617 0R0402-PAD-7-NP-GP

PC4613 SC1U10V2KX-1DLGP

PD4601 AZ4024-01L-R7G-GP

PR4601 0R0402-PAD-7-NP-GP

19V_DCBATOUT

PC4601 SCD22U25V2KX-4-GP

<Core Design>

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))

Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

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Main Func = CPU_CORE

OFFPAGE

46 PWR_VCORE_UGATE1 >> PWR_VCORE_UGATE1
46 PWR_VCORE_PHASE1 >> PWR_VCORE_PHASE1
46 PWR_VCORE_LGATE1 >> PWR_VCORE_LGATE1

46 PWR_VCORE_UGATE2 >> PWR_VCORE_UGATE2
46 PWR_VCORE_PHASE2 >> PWR_VCORE_PHASE2
46 PWR_VCORE_LGATE2 >> PWR_VCORE_LGATE2

46 PWR_VCORE_ISEN2 << PWR_VCORE_ISEN2
46 PWR_VCORE_ISEN1 << PWR_VCORE_ISEN1
46 PWR_VCORE_ISUMP << PWR_VCORE_ISUMP
46 PWR_VCORE_ISUMN << PWR_VCORE_ISUMN

19V_DCBATOUT
PC4721 SC10U25V6MX-5-GP
PC4719 SC10U25V6MX-5-GP
PC4702 SC10U25V6MX-5-GP
PC4703 SC10U25V6MX-5-GP
PC4704 SC10U25V6MX-5-GP
PC4705 SC10U25V6MX-5-GP
PC4706 SC10U25V6KX-1-GP

PWR_VCORE_LGATE1
PU4701 10
PWR_VCORE_UGATE1 1
PWR_VCORE_PHASE1 2
3
4
8
7 PWR_VCORE_PHASE1
6
5
9
AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073
PD4701 K A AZ9024-01L-R7G-GP

TGL 15W
Base mode
TDC=30A
ICCMAX=46A

Cyntec 6.8mmx7.6mmx3mm
DCR: 0.9m ohm +/-7%
Idc : 35A , Isat : 41A

1V_CPU_CORE
PL4701 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141
PR4705 2D2R6J-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP
PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP
PT4701 SE330U2D5VDM-2GP
79.3371V.2PL
2nd = 079.3371V.0031
PT4702 SE330U2D5VDM-2GP
79.3371V.2PL
2nd = 079.3371V.0031
PWR_VCORE_ISEN1
PR4721 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4708 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2
PWR_VCORE_ISUMP_GA
PWR_VCORE_ISUMN_GA
PR4709 10R2F-L-GP
PR4722 100KR2F-L1-GP

FOR acoustic noise
Change to 25V
height=2.8mm.2020/07/02
19V_DCBATOUT
TC4701 ST100U25VDM-1-GP
TC4702 ST100U25VDM-1-GP
077.C1071.0071
2nd = 077.C1071.0101
077.C1071.0071
2nd = 077.C1071.0101

19V_DCBATOUT
PC4722 SC10U25V6MX-5-GP
PC4720 SC10U25V6MX-5-GP
PC4717 SC10U25V6MX-5-GP
PC4714 SC10U25V6MX-5-GP
PC4716 SC10U25V6MX-5-GP
PC4715 SC10U25V6MX-5-GP
PC4718 SC10U25V6KX-1-GP

PWR_VCORE_LGATE2
PU4702 10
PWR_VCORE_UGATE2 1
PWR_VCORE_PHASE2 2
3
4
8
7 PWR_VCORE_PHASE2
6
5
9
AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073
PD4702 K A AZ9024-01L-R7G-GP

Cyntec 6.8mmx7.6mmx3mm
DCR: 0.9m ohm +/-7%
Idc : 35A , Isat : 41A

1V_CPU_CORE
PL4702 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141
PR4714 2D2R6J-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP
PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISEN2
PR4723 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4716 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP_GB
PWR_VCORE_ISUMN_GB
PR4715 10R2F-L-GP
PR4724 100KR2F-L1-GP

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (ISL95869_VCORE(2/2))
Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02
Date: Friday, January 29, 2021 | Sheet 47 of 106

Main Func = CPU_CORE

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<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 48 of 106

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A	*MOONKNIGHT_NVL_TGL*	*X02*

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Main Func = VCCIN_AUX

OFFPAGE

VID

22 CORE_VID0 — PR5014 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_VID0

22 CORE_VID1 — PR5015 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_VID1

53 PWR_1D8V_PG — PR5012 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_EN_R

7,24,40 VCCIN_AUX_PWRGD — PR5013 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_PG

VCCIN_AUX SENSE

22 VCCAUX_SENSE — PR5017 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_FB_O

22 VSSAUX_SENSE — PR5018 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_RGND

20200713
Remove R Sense
VCCIN_AUX_P
VCCIN_AUX_N

20200713
Remove R Sense
VCCIN_AUX_P
VCCIN_AUX_N

19V_DCBATOUT

PC5015 SC5D1U50V3KX-5GP (DY) · PC5016 SC5D1U50V3KX-5GP (DY) · PC5006 SC5D1U50V3KX-5GP · PC5007 SC5D1U50V3KX-5GP · PC5012 SC5D1U50V3KX-5GP · PC5013 SC5D1U50V3KX-5GP · PD5001 HZ4C04-01L-RTC-GP

PWR_VCCIN_AUX_BOOT — PC5009 SCD1U25V2KX-1-DL-GP

19V_DCBATOUT — PR5024 2D2R2J-GP — PC5014 SCD1U50V2KX-4-GP

3D3V_S5 — PR5004 10KR2F-2-GP

10/09 3D3V_S0 -> 3D3V_S5_charon

5V_S5 — PR5002 100KR2F-L1-GP — PWR_VCCIN_AUX_CS

PR5001 2D2R2J-GP — PWR_VCCIN_AUX_VCC — PC5008 SC1U10V2KX-1DLGP

PWR_VCCIN_AUX_PG

PWR_VCCIN_AUX_EN_R — PR5003 2D2R2J-GP — PC5010 SC1U10V2KX-1DLGP — PWR_VCCIN_AUX_EN

PWR_VCCIN_AUX_VID1

PWR_VCCIN_AUX_VID0

PR5003 (DY) — PWR_VCCIN_AUX_FSW — 10KR2F-2-GP

PU5001 RT6543A5OW-GP 074.06543.0073

Pin	Net
1	PWR_VCCIN_AUX_CS
15	PWR_VCCIN_AUX_VCC
4	PWR_VCCIN_AUX_PG
19	PWR_VCCIN_AUX_EN
17	PWR_VCCIN_AUX_VID1
18	PWR_VCCIN_AUX_VID0
9	PWR_VCCIN_AUX_FSW
10	PWR_VCCIN_AUX_BOOT
20	PWR_VCCIN_AUX_VSYS
11	PWR_VCCIN_AUX_UG
12	PWR_VCCIN_AUX_LX
13	PWR_VCCIN_AUX_LG
14	PGND
2	PWR_VCCIN_AUX_ISENP
3	PWR_VCCIN_AUX_ISENN
8	PWR_VCCIN_AUX_FB_O
5	PWR_VCCIN_AUX_COMP
6	PWR_VCCIN_AUX_FB
7	PWR_VCCIN_AUX_RGND
21	AGND

19V_DCBATOUT

PU5002 / PU5003 FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073
2nd = 075.36304.0073
3rd = 075.00019.0A73

TGL_U42 15W
Baseline
TDC=14A
ICCMAX=27A

Cyntec. 6.8 x 7.3 x 2.4mm
DCR: 2.2~2.8 mOhm
Idc : 25A , Isat : 50A

1D8V_VCCIN_AUX

PL5001 IND-D2UH-30-GP
2nd = 068.R2010.1021

PR5021 4K87R2F-GP — PR5016 0R0402-PAD-7-NP-GP — PC5011 SCD1U25V2KX-1-DL-GP

PR5007 100R2F-L1-GP-U — PT5001 SE330U2D5VDM-2GP
79.3371V.2PL
2nd = 079.3371V.0031

PR5008 294R2F — PWR_VCCIN_AUX_RC — PR5022 887R2F-L

PR5023 NTC-10K-29-GP-U
B=3370K 69.60011.201
2nd = 69.60013.131

PWR_VCCIN_AUX_FB_O

PC5003 SC2200P50V2KX-2DLGP — PWR_VCCIN_AUX_COMP_R — PR5011 10KR2F-2-GP

PC5002 SC470P50V2KX-3DLGP (DY) — PWR_VCCIN_AUX_FB_R — PR5009 1K6R2F-GP

PC5004 SC22P50V2JN-4DLGP

PR5010 6K62R2F-GP

PR5006 100R2F-L1-GP-U

<Core Design>

DELL Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT6543A_VCCIN_AUX)

Size: A2 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 29, 2021 | Sheet 50 of 106

OFFPAGE

S5(PM_SLP_S4#)
40 PWR_VDD_EN → PWR_VDD_EN

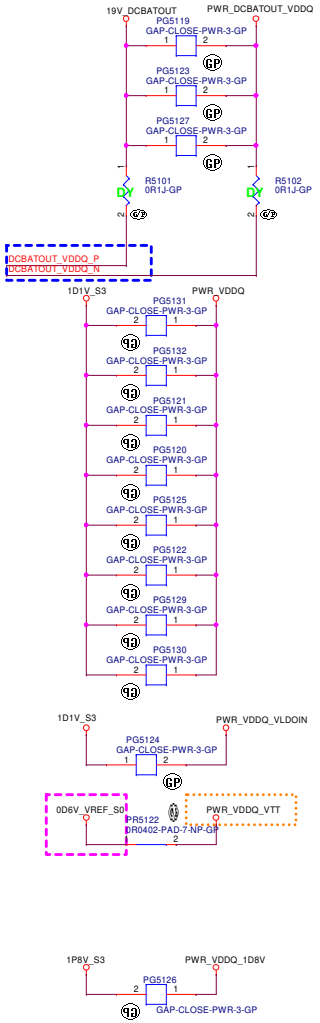
S3(VTT_CNTL)
40 VDDQ_EN → VDDQ_EN

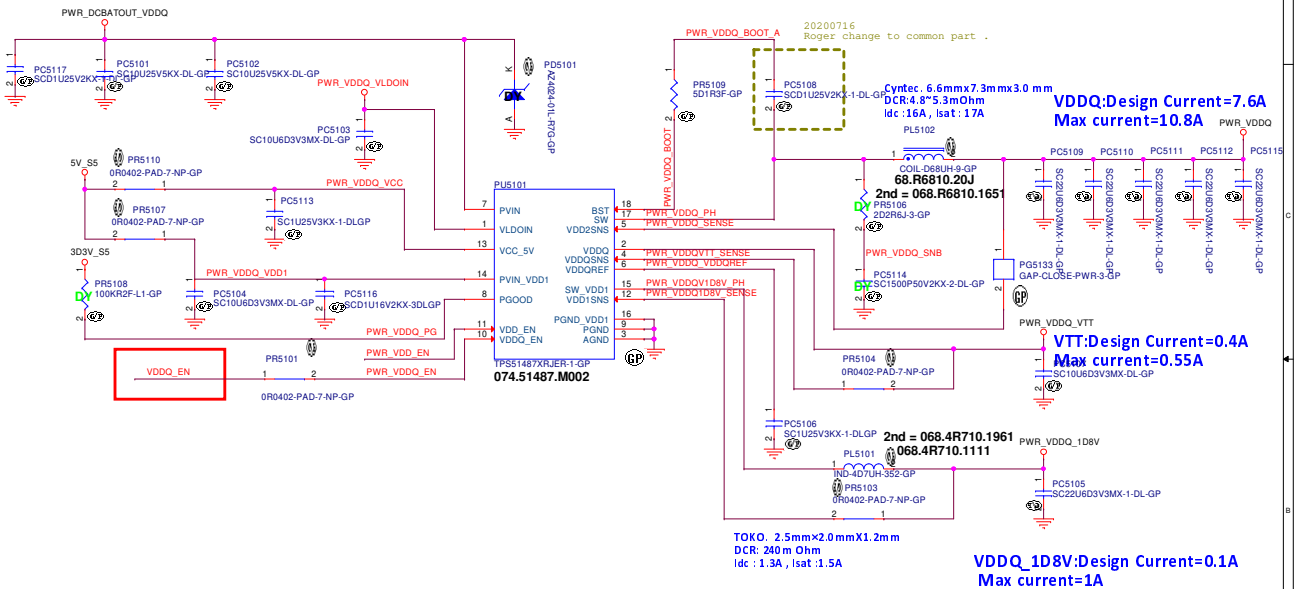
PH on EE Side
40 PWR_VDDQ_PG → PWR_VDDQ_PG

66 DCBATOUT_VDDQ_P → DCBATOUT_VDDQ_P
66 DCBATOUT_VDDQ_N → DCBATOUT_VDDQ_N

20200424 Add for P66 use. (Follow Shuri)

OFFPAGE_GAP





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS51487X_VDDQVTT)

Size	Document Number	Rev
Custom	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 51 of 106

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

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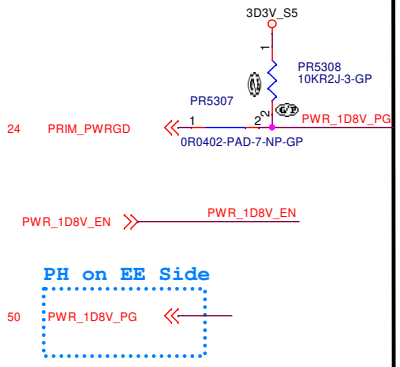
B	*MOONKNIGHT_NVL_TGL*	*X02*

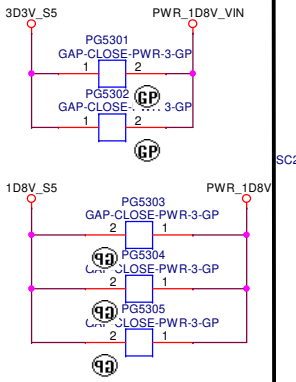
Date: Friday, January 29, 2021 Sheet 52 of 106

Main Func = 1D8V/1D2V

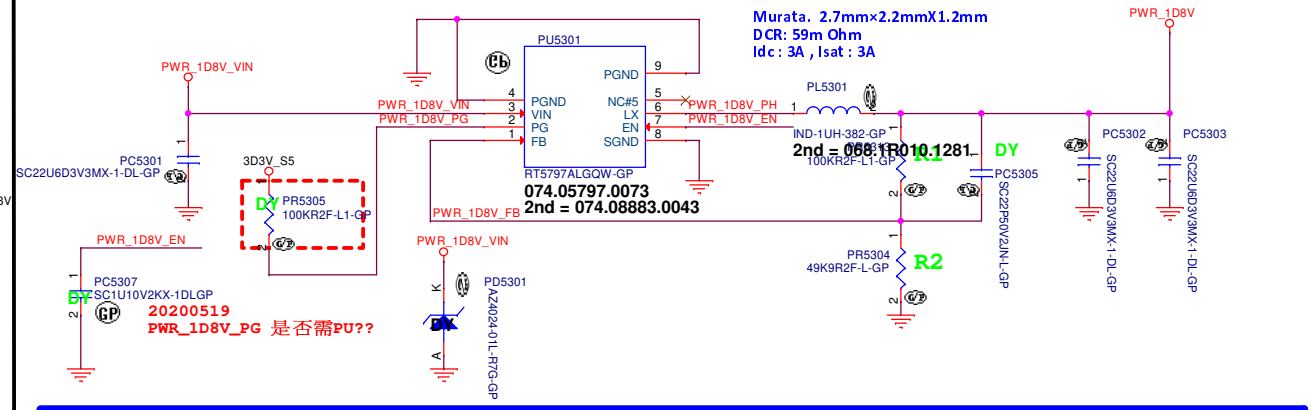
OFFPAGE



OFFPAGE_GAP



Design Current=1.7A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (RT5797_1D8V_S5)	
Size: B	Document Number: MOONKNIGHT_NVL_TGL	Rev: X02
Date: Friday, January 29, 2021	Sheet 53 of 106	

OFFPAGE

PH on EE Side

VCCIN_AUX_PWRGD
40 PWR_VNN_EN → PWR_VNN_EN

1D05V_BP_PWRGD
40 PWR_VNN1D05V_PG ← PWR_VNN1D05V_PG

40 PWR_1D05V_EN → PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
40 PWR_VNN1D05V_VID2 → PWR_VNN1D05V_VID2

PM_SLP_S3#
40 PWR_VNN1D05V_VID1 → PWR_VNN1D05V_VID1

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

OFFPAGE-GAP

1D05V_VNN_BYPASS — R5499 0R0402-PAD-7-NP-GP — PWR_VNN

1D05V_S5_BYPASS — R5498 0R0402-PAD-7-NP-GP — PWR_1D05V

3D3V_S5 — PR5420 100KR2J-1-GP — PWR_VNN1D05V_PG

PWR_VNN1D05V_VINA / PWR_VNN1D05V_VINB — PD5401 / PD5402 AZ4024-01L-R7G-GP

PC5401 SC1U10V2KX-1DLGP — 5V_S5 — 2D2R2F-GP

PC5402 SC4D7U5V3KX-2-GP

19V_DCBATOUT — PC5403 SC4D7U25V3KX-2-GP

PR5422 0R0402-PAD-7-NP-GP — PWR_VNN1D05V_VINA

PR5410 0R0402-PAD-7-NP-GP — PWR_VNN1D05V_VINB

PU5401 APW8743CQBI-TRG-GP

Pin	Signal
VCC	PWR_VNN1D05V_VCC
VIN1	PWR_VNN1D05V_VINA
VIN2	PWR_VNN1D05V_VINB
VID1	PWR_VNN1D05V_VID1
BOOT1	PWR_VNN1D05V_BOOTA
BOOT2	PWR_VNN1D05V_BOOTB
VID2	PWR_VNN1D05V_VID2
POK	PWR_VNN1D05V_PG
EN1	PWR_VNN_EN
EN2	PWR_1D05V_EN
LX1	PWR_VNN1D05V_PHA
LX2	PWR_VNN1D05V_PHB
VOUT2	PWR_VNN1D05V_FB2
VOUT1	PWR_VNN1D05V_VOUT1
AGND	
PGND	
PGND	

PC5404 SCD1U25V2KX-1-DL-GP — PWR_VNN1D05V_BOOTA_A

PC5405 SCD1U25V2KX-1-DL-GP — PWR_VNN1D05V_BOOTB_A

PC5406 DY SCD1U16V2KX-L-GP

PR5423 0R0402-PAD-NP-GP — PWR_VNN1D05V_PHB

PR5401 0R0402-PAD-7-NP-GP — PWR_VNN1D05V_PHA

Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A
Design Current=0.14A
Max current=0.2A

PL5401 IND-1UH-382-GP
2nd = 068.1R010.1281

PWR_VNN — PC5411 SC22U6D3V3MX-1-DL-GP — PC5412 SC22U6D3V3MX-1-DL-GP

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

PL5402 IND-10UH-330-GP
2nd = 068.10010.1A81

PWR_1D05V — PC5414 DY SC100P50V2JN-3GP — PR5408 0R0402-PAD-7-NP-GP — PC5410 SC22U6D3V3MX-1-DL-GP — PC5413 SC22U6D3V3MX-1-DL-GP

PR5419 0R0402-PAD-7-NP-GP — PWR_VNN

PR5407 0R2J-2-GP DY

PR5430 0R2J-2-GP DY

3D3V_S5 3D3V_S5

PR5426 10KR2F-2-GP DY — PWR_VNN1D05V_VID1

PR5427 10KR2F-2-GP DY — PWR_VNN1D05V_VID2

PR5433 10KR2F-2-GP

PR5428 10KR2F-2-GP

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

Design Current=0.14A
Max current=0.2A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER(APW8743_VNN1D05V)

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Main Func = LCD

4 eDP_TX_CPU_P0
4 eDP_TX_CPU_N0
4 eDP_TX_CPU_P1
4 eDP_TX_CPU_N1
4 eDP_TX_CPU_P2
4 eDP_TX_CPU_N2
4 eDP_TX_CPU_P3
4 eDP_TX_CPU_N3
4 eDP_AUX_CPU_P
4 eDP_AUX_CPU_N
4 EDP_HPD
4 eDP_VDD_EN
4 L_BKLT_CTRL
24 LCD_TST
24 PANEL_BKEN
24 PANEL_MONITOR
24 LCD_VCC_TEST_EN
17,40 SIO_SLP_S3#
24 CABLE1_OCP#
24 CABLE2_OCP#
16 CCD_USB20_P
16 CCD_USB20_N
27 DMIC_SCL_CODEC
27 DMIC_SDA_CODEC
19 DMIC_PCH_CLK_Q
19 DMIC_PCH_DATA_Q
20 DBC_PANEL_EN

20200727
ALS change to used I2C7
20 LCD_CBL_DET#

EL5501 DLMINSN900HY2D-GP
CCD_USB20_N ↔ CCD_USB20_CON_N
CCD_USB20_P ↔ CCD_USB20_CON_P
068.09002.2001

ED5501 AZ5315-02F-GP
83.05315.0A0
2nd = 079.5V0X2.0070

20200819
Layout Swap.

RN5501 SRN100J-3-GP
BKLT_CTRL ↔ LCD_BRIGHTNESS
PANEL_BKEN ↔ BLON_OUT_C
RN5505 SRN100J-3-GP
eDP_HPD_CON ↔ EDP_HPD
LCD_TST_C ↔ LCD_TST

R5502 0R2J-2-GP
D5502 BAT54C-12-GP
75.00054.A7D
BKLT_CTRL ↔ L_BKLT_CTRL
LCD_TST

RN5502 SRN100KJ-5-GP
eDP_HPD_CON
LVDS_VDD_EN
BLON_OUT_C
BKLT_CTRL

3D3V_S5
5V_S5
C5542 SC1U10V2KX-2GP
C5502 SC47D0U6V3MX-1GP
C5543 SC47D0U6V3MX-1GP
3D3V_LCDVDD_S0
C5508 SC1U10V2KX-1DGP
C5507 SC1U10V2KX-3GP

D5501 BAT54C-12-GP
75.00054.A7D
eDP_VDD_EN
LCD_VCC_TEST_EN
LVDS_VDD_EN
SIO_SLP_S3#

U5501 G2895BLK21U-GP
IN1 IN2 EN1 EN2 VB GND FLAG1 FLAG2 OUT1 OUT2 THERMAL_PAD
CABLE1_OCP#
CABLE2_OCP#

R5504 0R0402-PAD-7-NP-GP
CABLE1_OCP# ↔ CABLE2_OCP#

3D3V_HINGE_S0
C5516 SCD1U16V2KX-3DLGP
3D3V_MIC_VCC
RP5502 0R0402-PAD-7-NP-GP
C5515 SC47D1M63V2MX-1-GP
3D3V_CAMERA_S0
RP5503 0R0402-PAD-7-NP-GP
C5503 SC4D7U6V3MX-1-GP

INVERTER POWER
3RD = 69.41501.151
2ND = 69.41501.141
069.41501.0061

19V_DCBATOUT
D5503 SC4R2U41VLR1G-GP
F5503 FUSE-1D5A32V-12-GP
19V_DCBATOUT_LCD
C5514 SC100U25VKX-1GP
C5512 SC1U25VKX-1-GP
C5513 SC1H5V0KX-1DLGP

3D3V_S5
RN5506 SRN10KJ-5-GP
RN5504 SRN33J-5-GP-U
DMIC_PCH_CLK_Q
DMIC_PCH_DATA_Q
DMIC_SCL_CON
DMIC_SDA_CON
RN5503 SRN33J-5-GP-U
DMIC_SCL_CODEC
DMIC_SDA_CODEC
EC5504 SC2S6P6V2AN1DGP
EC5503 SC2S6P6V2AN1DGP

20200713
Remove 50 Pin Non-B To B eDP connector

20200714
Reserve ALS I2C signal.

20200803
LCD1 Change to 020.F1308.0040

eDP Panel / HD Camera

LCD1 IPEX-CON40-8-GP
19V_DCBATOUT_LCD
DBC_PANEL_EN
eDP_TX_CPU_N3 C5521 SCD1U16V2KX-3DLGP eDP_TX_CON_N3
eDP_TX_CPU_P3 C5522 SCD1U16V2KX-3DLGP eDP_TX_CON_P3
eDP_TX_CPU_N2 C5519 SCD1U16V2KX-3DLGP eDP_TX_CON_N2
eDP_TX_CPU_P2 C5520 SCD1U16V2KX-3DLGP eDP_TX_CON_P2
eDP_TX_CPU_N1 C5501 SCD1U16V2KX-3DLGP eDP_TX_CON_N1
eDP_TX_CPU_P1 C5504 SCD1U16V2KX-3DLGP eDP_TX_CON_P1
eDP_TX_CPU_N0 C5506 SCD1U16V2KX-3DLGP eDP_TX_CON_N0
eDP_TX_CPU_P0 C5509 SCD1U16V2KX-3DLGP eDP_TX_CON_P0
eDP_AUX_CPU_P C5510 SCD1U16V2KX-3DLGP eDP_AUX_CON_P
eDP_AUX_CPU_N C5511 SCD1U16V2KX-3DLGP eDP_AUX_CON_N
3D3V_LCDVDD_S0
R5510 0R0402-PAD-7-NP-GP
LCD_TST_C
LCD_CBL_DET#
eDP_HPD_CON
BLON_OUT_C
LCD_BRIGHTNESS
DIAGLOOP
3D3V_MIC_VCC
CCD_USB20_CON_P
CCD_USB20_CON_N
DMIC_SDA_CON
DMIC_SCL_CON
3D3V_CAMERA_S0

M-BIST/ LCD BIST -20180425

LCD BIST for G10 (Was test only for G9)

19V_DCBATOUT_LCD
D5504 RB551V30-GP
83.R5003.H8H
2ND = 83.R5003.T8F
BL_PWR_MONITOR_R
R5532 10KR2J-3-GP
R5533
C5557 SC2200P50V2KX-2DLGP
BL_PWR_MONITOR_BJT_B
19V_DCBATOUT
Q5512 MMBT3906-3-GP
BL_PWR_MONITOR_BJT_C
R5534 4K7R2J-2-GP
BL_PWR_MONITOR
3D3V_S5
R5535 100KR2J-1-GP
PANEL_PWRGD
Q5508 LMBT3904LT1G-GP
84.T3904.H11
2ND = 084.03904.0I11
3RD = 084.03904.0H11
R5536 0R0402-PAD-7-NP-GP
PANEL_MONITOR
C5558 SCD1U16V2KX-3DLGP
3D3V_S0
R5540 0R0402-PAD-7-NP-GP
LCDVDD_MONITOR_BJT_E
Q5509 MMBT3906-3-GP
LCDVDD_MONITOR_BJT_C
R5539 4K7R2J-2-GP
LCDVDD_MONITOR
Q5510 MBT3904LT1G-GP
84.T3904.H11
2ND = 084.03904.0I11
3RD = 084.03904.0H11
3D3V_LCDVDD_S0
D5505 RB551V30-GP
83.R5003.H8H
2ND = 83.R5003.T8F
LCDVDD_MONITOR_R
R5537 10KR2J-3-GP
R5538
C5555 SC2200P50V2KX-2DLGP
LCDVDD_MONITOR_BJT_B

«Core Design»

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: A2
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*MOONKNIGHT_NVL_TGL*	*X02*

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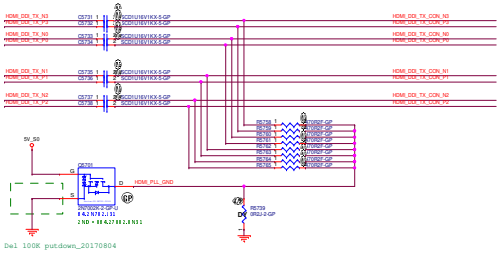
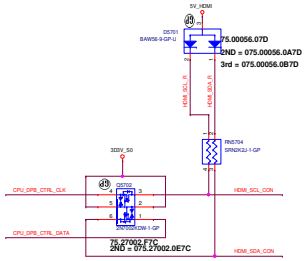
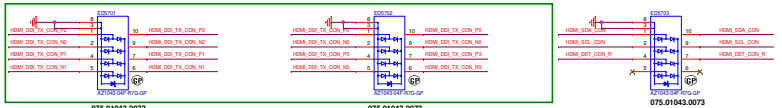
Main Func = HDMI



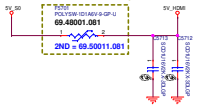


20200728
Remove HDMI Chock, add 180R,between P and N signals
EMC solution

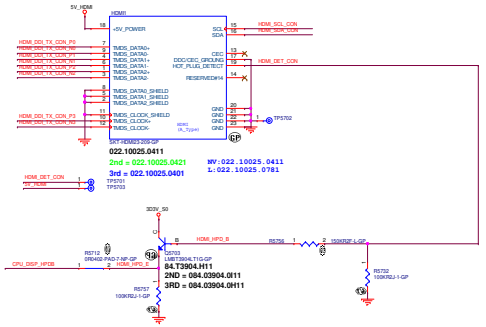


HDMI CONNECTOR

20200721
HDMI Power Switch chang Fuse.



20200728
Remove HDMI_SEL



Title: Display (HDMI Level Shifter/Conn)
Size: A1
Document Number: MOONKNIGHT_NVL_TGL
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<Core Design>

Wistron Corporation
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Title
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<Core Design>

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Title
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<Core Design>

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Title

(Reserved)

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Main Func = WLAN

PCIE

16 WLAN_PCIE_TX_N
16 WLAN_PCIE_TX_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P

PCIE_CLK

18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
18 CLK_PCIE_WLAN_REQ#

USB2.0

16 BT_USB20_P
16 BT_USB20_N

Single end

19 BT_RADIO_DIS#
16 WLAN_RF_DIS#
17,63,71,75,76,91 PCH_PLTRST#
18,24 SUSCLK

Debug

66 3D3V_WLAN_P
66 3D3V_WLAN_N

Power EN (Madesimo)

21 CNV_BRI_DT_R
21 CNV_RGI_DT_R
21 CLKREQ_CNV
21 CNV_RF_RESET#
21 CNV_WT_DN0
21 CNV_WT_DP0
21 CNV_WT_DN1
21 CNV_WT_DP1
21 CNV_WT_CLKN
21 CNV_WT_CLKP
21 CNV_WR_DN0
21 CNV_WR_DP0
21 CNV_WR_DN1
21 CNV_WR_DP1
21 CNV_WR_CLKN
21 CNV_WR_CLKP
21 CNV_BRI_RSP
21 CNV_RGI_RSP
17 PCIE_WAKE#

3D3V_S5 — R6140 0R0603-PAD-7-NP-GP — 3D3V_WLAN

1.1A

C6106 close 3D3V_WALN
C6109 close PIN 2,4
C6110 close PIN 72,74

R6138 0R1J-GP DY
R6139 0R1J-GP DY
C6106 SCD1U16V2KX-3DLGP
C6110 SCD1U16V2KX-3DLGP
C6109 SCD1U16V2KX-3DLGP

3D3V_WLAN_P
3D3V_WLAN_N

2020/04/27
Delete reserve C6111

20200721
Placement note Cap position

20200721
Remove C6113 C6114 C6115.

AFTE14P-GP TP6101 — 1 3D3V_WLAN
AFTE14P-GP TP6105 — 1 CLK_PCIE_WLAN_REQ#
AFTE14P-GP TP6106 — 1 WIFI_RF_EN_R
AFTE14P-GP TP6107 — 1 BLUETOOTH_EN_R
AFTE14P-GP TP6108 — 1 PCH_PLTRST#
AFTE14P-GP TP6109 — 1 BT_USB20_CON_N
AFTE14P-GP TP6110 — 1 BT_USB20_CON_P
AFTE14P-GP TP6111 — 1 PCIE_WAKE#

2020/04/22
Delete CNV_BRI_DT_R/CNV_BRI_RSP/CNV_RGI_RSP PU 20K(DY) on 1D8V_S5

3D3V_WLAN — R6145 10KR2J-3-GP — R6144 0R0402-PAD-7-NP-GP — WLAN_RF_DIS# — WIFI_RF_EN_R

3D3V_WLAN — R6146 10KR2J-3-GP — R6143 0R0402-PAD-7-NP-GP — BT_RADIO_DIS# — BLUETOOTH_EN_R

WLAN1

76	76	77	77
74	3_3VAUX	75	GND
72	3_3VAUX	73	CNV_WT_CLKP
70	RESERVED#70	71	CNV_WT_CLKN
68	RESERVED#68	69	RESERVED#73
66	RESERVED#66	67	GND
64	GPIO0_NFC_RESET#/MGPIO7	65	CNV_WT_DP0
62	NFC_I2C_IRQ/MGPIO5	63	CNV_WT_DN0
60	NFC_I2C_SM_CLK	61	GND
58	NFC_I2C_SM_DATA	59	CNV_WT_DP1
56	W_DISABLE#1	57	CNV_WT_DN1
54	RESERVED#54/W_DISABLE#2	55	GND
52	PERST0#	53	PCIE_WAKE#
50	SUSCLK_32KHZ	51	CLKREQ0#
48	COEX1	49	CLK_PCIE_WLAN_REQ#
46	COEX2	47	GND
44	COEX3	45	WLAN_CLK_CPU_N
42	CLINK_CLK	43	REFCLKN0
40	CLINK_DATA	41	REFCLKP0
38	CLINK_RESET	39	GND
36	UART_CTS	37	PERN0
34	UART_RTS	35	PERP0
32	UART_TX	33	GND
22	UART_RX	23	PETN0
20	UART_WAKE	21	PETP0
18	GND	19	GND
16	LED#2	17	SDIO_RESET
14	PCM_OUT	15	SDIO_WAKE
12	PCM_IN	13	SDIO_DAT3
10	PCM_SYNC	11	SDIO_DAT2
8	PCM_CLK	9	SDIO_DAT1
6	LED#1	7	SDIO_DAT0
4	3_3VAUX	5	SDIO_CMD
2	3_3VAUX	3	SDIO_CLK
		1	GND
NP2	NP2	NP1	USB_D-
			USB_D+
			GND
		NP1	NP1

SKT-NGFF75P-164-GP

NGFF_KEY_E_75P

062.10003.0B11
2ND = 062.10007.0371

3D3V_WLAN — R6106 DY 10KR2J-3-GP — CLKIN_XTAL_LCP_R

WIFI_RF_EN_R
BLUETOOTH_EN_R
PCH_PLTRST#

SUSCLK — R6135 33R2J-2-GP — SUSCLK_WLAN

CNV_RGI_RSP — R6109 49D9R2F-GP — CNV_BRI_DT_R / CNV_RGI_RSP_R / CNV_RGI_DT_R

CNV_BRI_RSP — R6118 49D9R2F-GP — CNV_BRI_RSP_R

CLKREQ_CNV — R6141 33R2J-2-GP — BT_PCMOUT_CLKREQ0_R

CNV_RF_RESET# — R6142 33R2J-2-GP — BT_PCMFRM_CRF_RST_N

3D3V_WLAN — R6134 75KR2F-GP — R6133 DY 71K5R2F-1-GP

WLAN_PCIE_TX_CON_N — C6107 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_N
WLAN_PCIE_TX_CON_P — C6108 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_P

2020/04/22
Delete R6147, R6148,R6136 and R6137 0ohm Res

20200819
Layout Swap.

R6111 1 — 2 0R0402-PAD-7-NP-GP
BT_USB20_CON_N — BT_USB20_N
BT_USB20_CON_P — BT_USB20_P
R6110 1 — 2 0R0402-PAD-7-NP-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF_WLAN CONN

Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 61 of 106

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<Core Design>

Wistron Corporation
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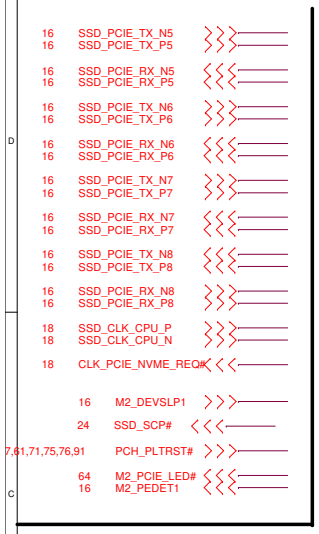
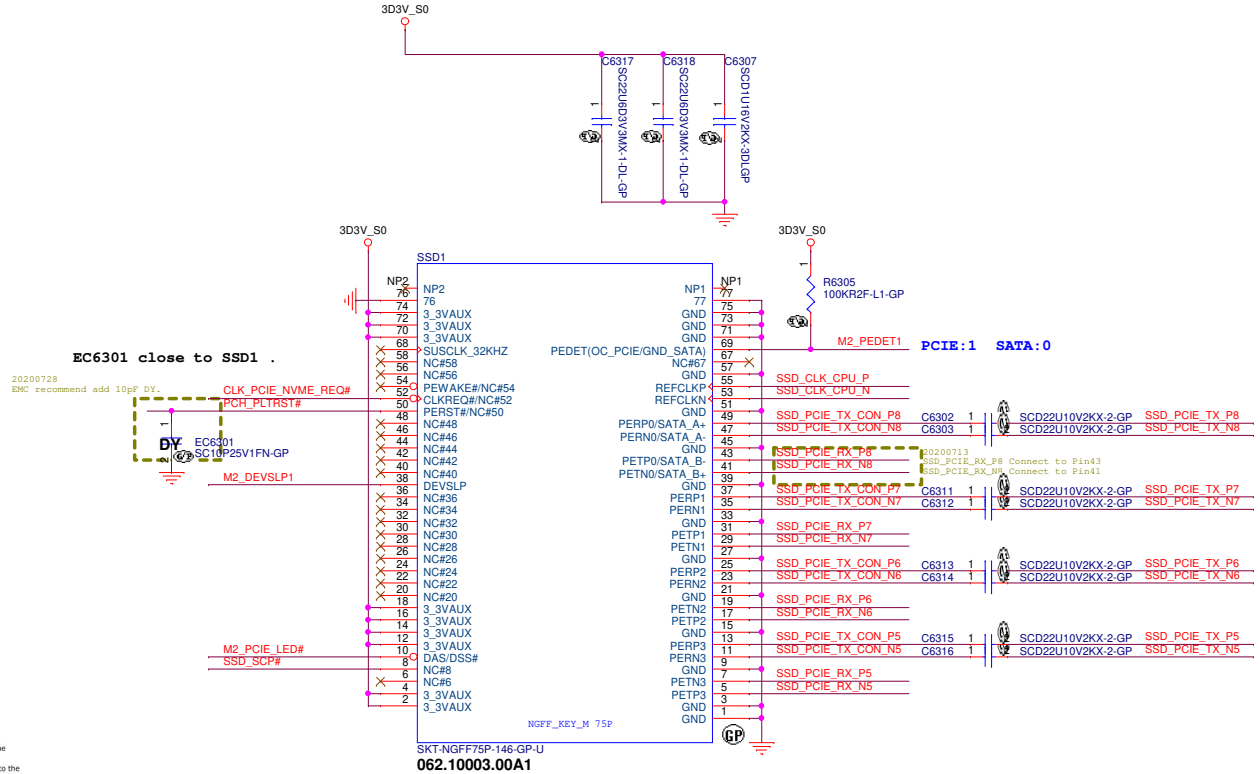
Title	*(Reserved)*	
Size: A3	Document Number: *MOONKNIGHT_NVL_TGL*	Rev: *X02*
Date: Friday, January 29, 2021	Sheet 62 of 106	

Main Func = SSD M.2





062.10003.00A1
2ND = 062.10003.0991
3rd = 062.10003.0411

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title: **SSD M.2/eMMC**

Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	X02

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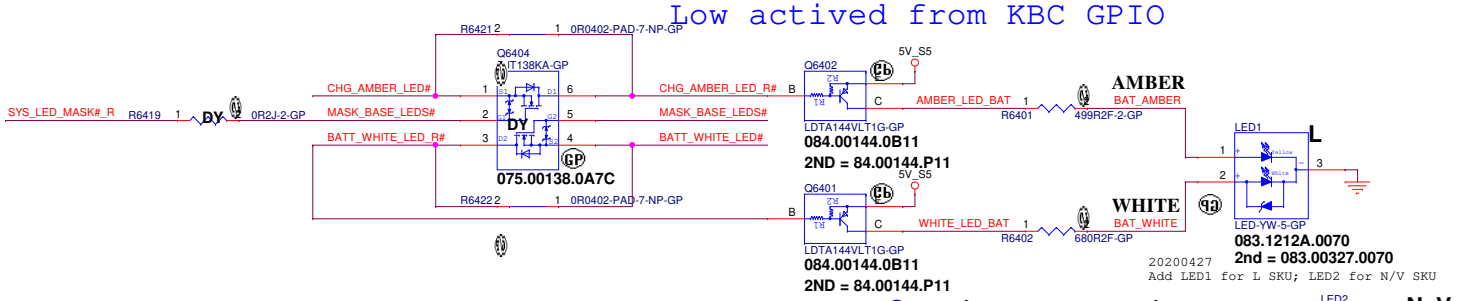
Main Func = Power BTN

24 CHG_AMBER_LED#
24 BATT_WHITE_LED#
24 SYS_LED_MASK#_R

Battery LED1 (AMBER_LED)

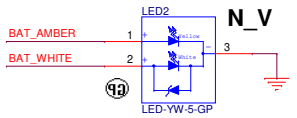
Low actived from KBC GPIO



20200427
Add LED1 for L SKU; LED2 for N/V SKU

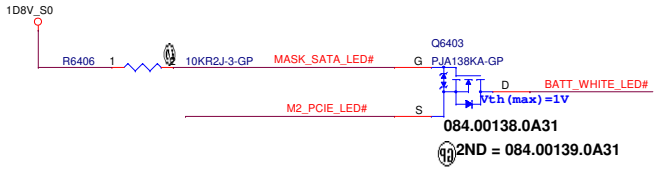
Battery LED2 (WHITE_LED)

Low actived from KBC GPIO



24 MASK_SATA_LED#
63 M2_PCIE_LED#

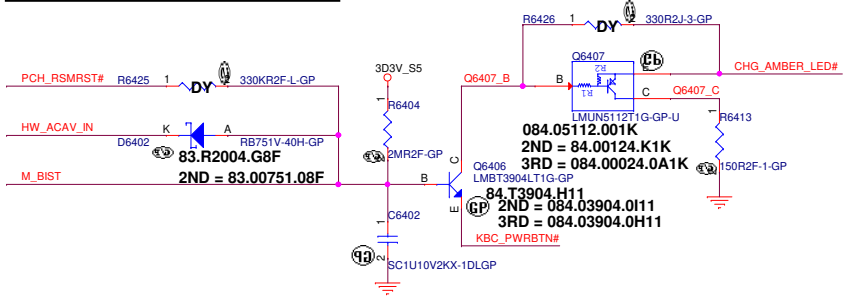
SATA LED



24,66 KBC_PWRBTN#
24,44 HW_ACAV_IN
17,24 PCH_RSMRST#
24 M_BIST

M-BIST for G10

M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by



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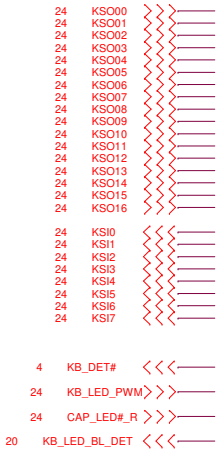
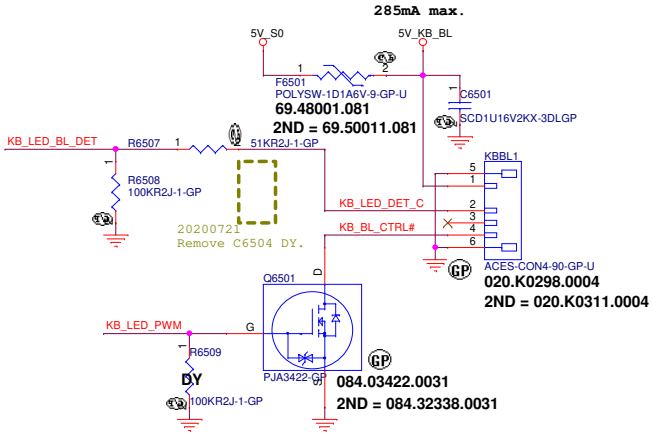
Title: LED Board&Power Button

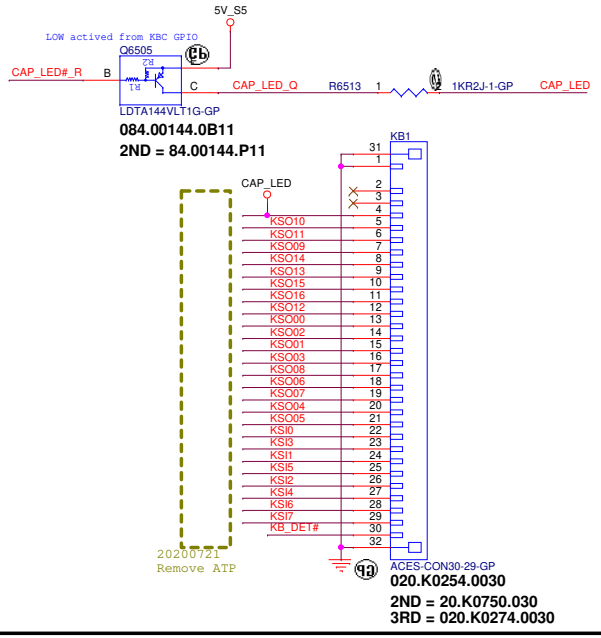
Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	X02

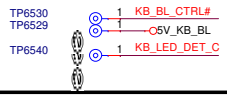
Date: Friday, January 29, 2021 Sheet 64 of 106

Main Func = Keyboard

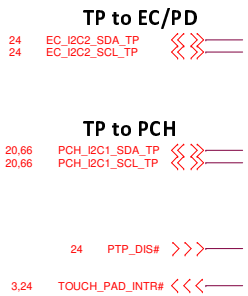


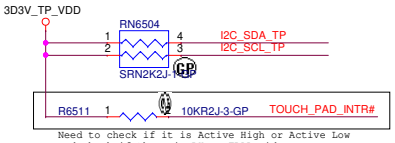


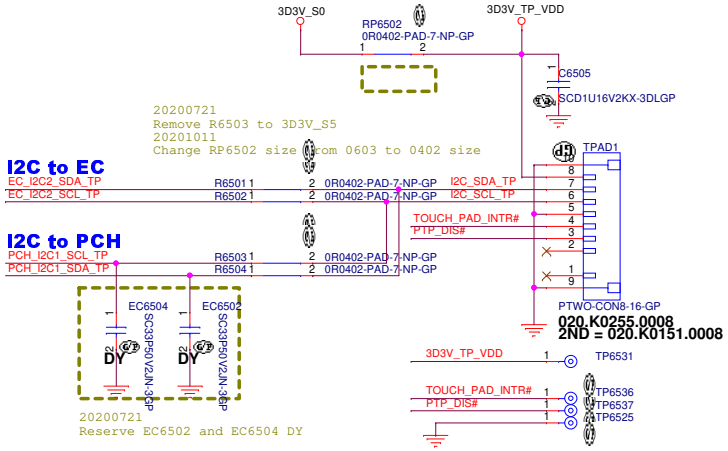




Main Func = TPAD







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Title: Key Board&Touch Pad

Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 65 of 106

Main Func = IO Connector

16 USB2_USB31_TX_P
16 USB2_USB31_TX_N
16 USB2_USB31_RX_P
16 USB2_USB31_RX_N

16 USB1_USB31_TX_N
16 USB1_USB31_TX_P
16 USB1_USB31_RX_N
16 USB1_USB31_RX_P

16 USB4_USB20_N
16 USB4_USB20_P
16 USB1_USB20_N
16 USB1_USB20_P
16 CARD1_USB20_N
16 CARD1_USB20_P

18 HOST_SD_WP#
24,64 KBC_PWRBTN#

27,29 AUD_HP1_JACK_L
27,29 AUD_HP1_JACK_R
27,29 AUD_SLEEVE
27,29 AUD_RING
27 AUD_SENSE

Modified IO Conn from 30P to 40P, MKT NVL 13 EIV, 2020/03/09
Note(AR): Need check conn list if release

Modified IO Conn pin definition, MKT NVL 13 EIV, 2020/03/24

EL6603
DLM0NSN900HY2D-GP
USB1_USB20_N
USB1_USB20_P
USB1_USB20_N_CMC
USB1_USB20_P_CMC
068.09002.2001
2nd = 68.02002.061

EL6602 CLOSE TO IO1

EL6602
DLM0NSN900HY2D-GP
L-SKU
USB4_USB20_N
USB4_USB20_P
USB4_USB20_N_CMC
USB4_USB20_P_CMC
068.09002.2001
2nd = 68.02002.061

EL6601 CLOSE TO IO1

IO1
STM-CON40-GP
L
USB30_VCCA
3D3V_S5
KBC_PWRBTN#
USB1_USB20_N_CMC
USB1_USB20_P_CMC
USB1_USB31_TX_N
USB1_USB31_TX_P
USB1_USB31_RX_N
USB1_USB31_RX_P
AUD_AGND
AUD_SLEEVE
AUD_HP1_JACK_R
AUD_SENSE
AUD_HP1_JACK_L
AUD_RING
HOST_SD_WP#
USB4_USB20_N_CMC
USB4_USB20_P_CMC
USB2_USB31_TX_N
USB2_USB31_TX_P
USB2_USB31_RX_N
USB2_USB31_RX_P
CARD1_USB20_P
CARD1_USB20_N
20.F2406.040
2nd = 020.F0847.0040
3rd = 020.F1427.0040

IO2
STM-CON30-6-GP
N_V
USB4_USB20_P_CMC
USB4_USB20_N_CMC
3D3V_S0
HOST_SD_WP#
AUD_AGND
AUD_RING
AUD_HP1_JACK_L
AUD_SENSE
AUD_HP1_JACK_R
AUD_SLEEVE
USB1_USB31_RX_P
USB1_USB31_RX_N
USB1_USB31_TX_P
USB1_USB31_TX_N
USB1_USB20_P_CMC
USB1_USB20_N_CMC
KBC_PWRBTN#
3D3V_S5
USB30_VCCA
020.F1027.0030
2nd = 020.F1428.0030

20200814
IO1/IO2 Change Pin define for IOB.

44 PWR_CHG_CSOP_R
44 PWR_CHG_CSON_R

20,65 PCH_I2C1_SDA_TP
20,65 PCH_I2C1_SCL_TP

61 3D3V_WLAN_N
61 3D3V_WLAN_P

51 DCBATOUT_VDDQ_P
51 DCBATOUT_VDDQ_N

20200713
Remove R Sense
VCCIN_AUX_P
VCCIN_AUX_N

3D3V_WLAN_P
3D3V_WLAN_N
PCH_I2C1_SCL_TP
DCBATOUT_VDDQ_N
DCBATOUT_VDDQ_P
PCH_I2C1_SDA_TP
3D3V_S0
PWR_CHG_CSOP_R
PWR_CHG_CSON_R
DY
CN1
HRS-CONN20A-2-GP
20.F1450.020

20200713
Remove R Sense
VCCIN_AUX_P
VCCIN_AUX_N

PWR_CHG_CSOP_R Converter

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Title: IO Board Connector
Size: A3
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
Date: Friday, January 29, 2021
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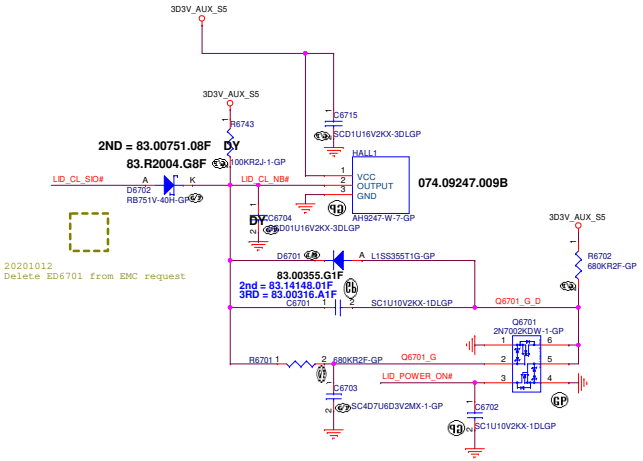
Main Func = HALL SENSOR

20,24,92 LID_CL_SIO#
24 LID_POWER_ON#



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Title: Sensor (Hall-Sensor)

Size	Document Number	Rev
C	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 67 of 108

Main Func = Debug

18,24 ESPI_CPU_IO0
18,24 ESPI_CPU_IO1
18,24 ESPI_CPU_IO2
18,24 ESPI_CPU_IO3

18,24 ESPI_CPU_RST#
18,24 ESPI_CPU_CS#
18,24 ESPI_CPU_CLK

24 HOST_DEBUG_TX

20 CPU_UART2_TXD
20 CPU_UART2_RXD

20200721
Debug power change to use 3D3V_S0.

3D3V_S0 3D3V_S5 3D3V_DB1

R6804 1 DY 0R2J-2-GP
R6805 1 DEBUG 0R2J-2-GP

DB1

ESPI_CPU_CLK
ESPI_CPU_RST#
ESPI_CPU_CS#
ESPI_CPU_IO3
ESPI_CPU_IO2
ESPI_CPU_IO1
ESPI_CPU_IO0

DEBUG

20200728
R6801 change to stuff, follow Cyborg.

HOST_DEBUG_TX R6801 1 DEBUG 0R2J-2-GP HOST_DEBUG_TX_CON
CPU_UART2_TXD R6802 1 DEBUG 0R2J-2-GP UART_2_CTXD_DRXD_CON
CPU_UART2_RXD R6803 1 DEBUG 0R2J-2-GP UART_2_CRXD_DTXD_CON

ACES-CON14-5-GP
20.F0765.014

20191212
Follow CY20

3D3V_S0
R6807 1 DEBUG 51KR2J-1-GP CPU_UART2_RXD
R6808 1 51KR2J-1-GP CPU_UART2_TXD
DEBUG

20200427
Add UART PU 3D3V_S0

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Title: Dubug connector

Size	Document Number	Rev
A4	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 68 of 106

(Blanking)

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Title

Reserved

Size	Document Number	Rev
A4	***MOONKNIGHT_NVL_TGL***	***X02***

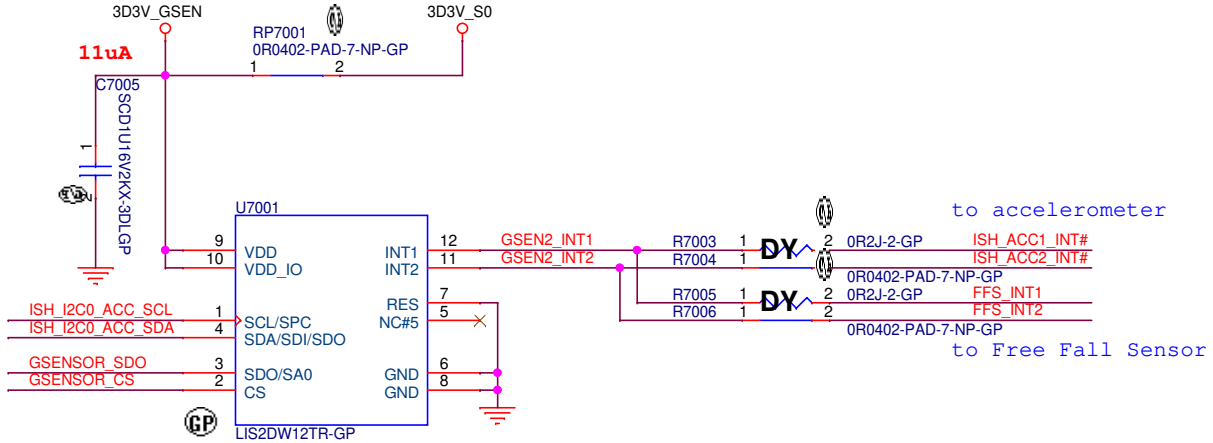
Date: Friday, January 29, 2021 Sheet 69 of 106

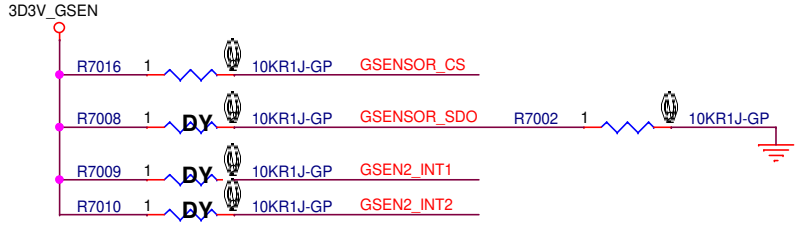
Main Func = G-sensor

20 ISH_ACC1_INT#
20 ISH_ACC2_INT#

20 FFS_INT1
19 FFS_INT2

20 ISH_I2C0_ACC_SCL
20 ISH_I2C0_ACC_SDA





<Core Design>

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Title: Sensor

Size	Document Number	Rev
A4	MOONKNIGHT_NVL_TGL	X02

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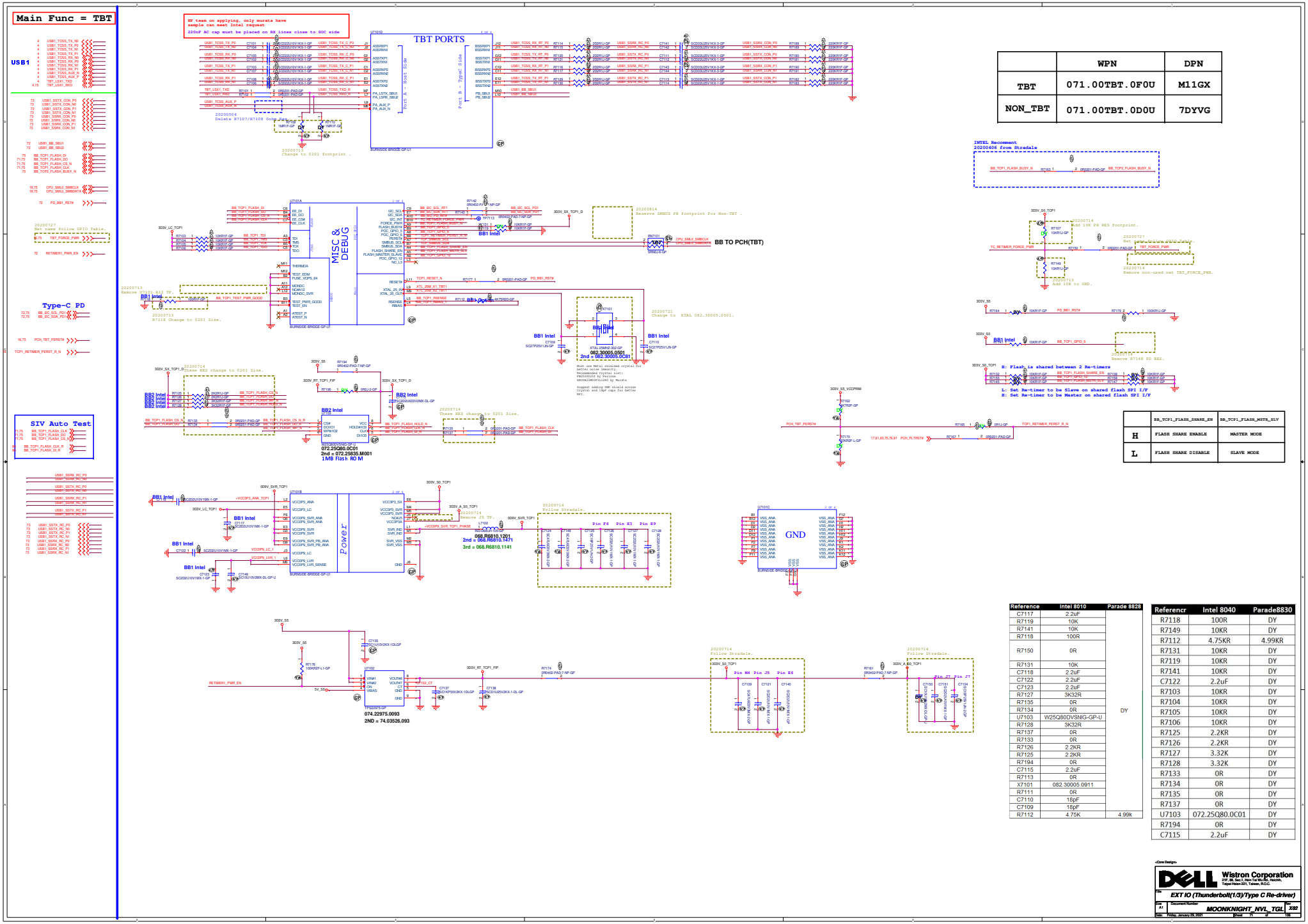

	WPN	DPN
TBT	071.00TBT.0F0U	M11GX
NON_TBT	071.00TBT.0D0U	7DYVG

	BB_TCP1_FLASH_SHARE_EN	BB_TCP1_FLASH_MSTR_SLV
H	FLASH SHARE ENABLE	MASTER MODE
L	FLASH SHARE DISABLE	SLAVE MODE

Reference	Intel 8010	Parade 8828
C7117	2.2uF	
R7119	10K	
R7141	10K	
R7118	100R	
R7150	0R	
R7131	10K	
C7118	2.2uF	
C7122	2.2uF	
C7123	2.2uF	
R7127	3K32R	
R7135	0R	
R7134	0R	DY
U7103	W25Q80DVSNIG-GP-U	
R7128	3K32R	
R7137	0R	
R7133	0R	
R7126	2.2KR	
R7125	2.2KR	
R7127	3.32K	
R7194	0R	
C7115	2.2uF	
R7113	0R	
X7101	082.30005.0911	
R7111	0R	
C7110	18pF	
C7109	18pF	
R7112	4.75K	4.99k

Referencr	Intel 8040	Parade8830
R7118	100R	DY
R7149	10KR	DY
R7112	4.75KR	4.99KR
R7131	10KR	DY
R7119	10KR	DY
R7141	10KR	DY
C7122	2.2uF	DY
R7103	10KR	DY
R7104	10KR	DY
R7105	10KR	DY
R7106	10KR	DY
R7125	2.2KR	DY
R7126	2.2KR	DY
R7127	3.32K	DY
R7128	3.32K	DY
R7133	0R	DY
R7134	0R	DY
R7135	0R	DY
R7137	0R	DY
U7103	072.25Q80.0C01	DY
R7194	0R	DY
C7115	2.2uF	DY

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File: EXT IO (Thunderbolt(1/3)/Type C Re-driver)

Size: A1 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 29, 2021 | Sheet 71 of 105

Main Func = TypeC

SWD Programming

Follow Hellcat15 Upsell TGL

CCG 6DF

PD to SOC

PD to EC

PD to BB

VIN_P0

VIN_P1

VOUT1

VOUT2

From/To Type-C Conn

From/To BB1

From/To BB2

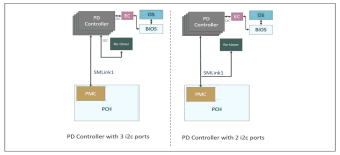
From PCH

PD to EC

Normal: High
Active : Low

1uF x 2, 100nF x 2

Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



Notes:
CCG6DF device's I2C address is determined by SWD_CLK pin.
1K resistors not populated = I2C address 0x08 (default)
1K resistor connected to GND = I2C address 0x40
1K resistor connected to VDDD = I2C address 0x42

100K ≤ R7+R8 ≤ 500K

100K ≤ R9+R10 ≤ 500K

50K ≤ R7, R8, R9, R10 ≤ 500K

Resistor values for MOD_ID settings are decided based on the table shown below.
Please make sure to choose these resistors (R7, R8, R9 and R10) based on the above guidelines

MOD_ID Settings			
Voltage Levels	MOD_ID1	MOD_ID2	Description
L0 = 0V	L0	L0	TBT Config1 (with BB Retimer)
L1 = VDD/3	L1	L0	TBT Config2 (with BB Retimer cascaded)
L2 = 2*VDD/3	L2	L0	non-TBT Config1 (with BB Retimer)
L3 = 3*VDD/3	L3	L0	non-TBT Config2 (with BB Retimer Replacement)
L4 = 4*VDD/3	L4	L0	TBT Config3 (with Maple Ridge)
L5 = 5*VDD/3	L5	L0	Reserved
		Max3 (0 - L3	
L6 = 6*VDD/3	L6	Max3 (4 - L7	non-TBT Max1 & Max2 Config
L7 = 7*VDD/3	L7	Max4 (4 - L7	non-TBT Max3 & Max4 Config

20200715
Follow Stradale Value

NON-TBT

20200811
Vendor recommend value for ID1 ID2

	W/V 2port	L 1port
R7216	715KR	715KR
R7218	100KR	100KR
R7207	DY	715KR
R7226	100KR	100KR

20200715
Remove T2

Dell TGL Platform MOD_ID Options

MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

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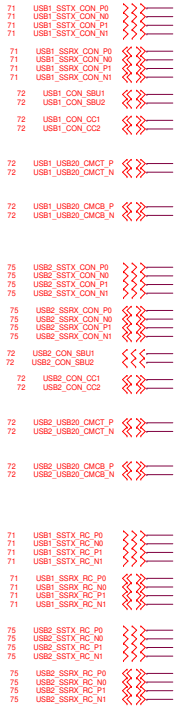
Taipei Hsien 221, Taiwan, R.O.C.

File: EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size: A1 | Document Number: MOONKNIGHT_NVL_TGL | Rev: X02

Date: Friday, January 24, 2020 | Sheet 72 of 106

Main Func = Type-C Port1/2



20V_VCCPD1_VBUS

C7301 SC1G225V1KX3-GP
C7305 SC1G225V1KX3-GP
C7308 SC1G475V6MX5-GP

20200527
Add for power drap from Stradale.

C7321 SC100P50V2JN-3GP

USB1

USB1_SSTX_CON_P0 USB1_SSTX_CON_N0 USB1_SSTX_CON_P1 USB1_SSTX_CON_N1
USB1_CON_CC1 USB1_USB20_CONT_P USB1_USB20_CONT_N USB1_CON_SBU1
USB1_SSRX_CON_N1 USB1_SSRX_CON_P1
USB1_CON_CC2 USB1_USB20_CONB_P USB1_USB20_CONB_N USB1_CON_SBU2
USB1_SSRX_CON_N0 USB1_SSRX_CON_P0

GND SSTXP1 SSTXN1 VBUS CC1 DP1 DN1 SBU1 VBUS SSRXN2 SSRXP2 GND
GND SSTXP2 SSTXN2 VBUS CC2 DP2 DN2 SBU2 VBUS SSRXN1 SSRXP1 GND
NP1 NP2

SKT-USB32-85-GP-U

022.10005.M082

20200821
Type C connector need change to 022.10005.M082

C7322 SC100P50V2JN-3GP

20V_VCCPD2_VBUS

C7309 SC1G225V1KX3-GP
C7310 SC1G225V1KX3-GP
C7313 SC1G475V6MX5-GP

20200715
Remove C7311 C7312

20200527
Add for power drap from Stradale.

C7302 SC100P50V2JN-3GP

USB2

USB2_SSTX_CON_P0 USB2_SSTX_CON_N0 USB2_SSTX_CON_P1 USB2_SSTX_CON_N1
USB2_CON_CC1 USB2_USB20_CONT_P USB2_USB20_CONT_N USB2_CON_SBU1
USB2_SSRX_CON_N1 USB2_SSRX_CON_P1
USB2_CON_CC2 USB2_USB20_CONB_P USB2_USB20_CONB_N USB2_CON_SBU2
USB2_SSRX_CON_N0 USB2_SSRX_CON_P0

GND SSTXP1 SSTXN1 VBUS CC1 DP1 DN1 SBU1 VBUS SSRXN2 SSRXP2 GND
GND SSTXP2 SSTXN2 VBUS CC2 DP2 DN2 SBU2 VBUS SSRXN1 SSRXP1 GND
NP1 NP2

SKT-USB32-85-GP-U

022.10005.M082

20200821
Type C connector need change to 022.10005.M082

C7303 SC100P50V2JN-3GP

USB1_USB20_CMCT_P → EL7301 → USB1_USB20_CONT_P
USB1_USB20_CMCT_N → EL7301 → USB1_USB20_CONT_N
DLM0NSN900HY2D-GP

068.09002.2001
2ND = 68.02002.061

USB2_USB20_CMCT_P → EL7303 → USB2_USB20_CONT_P
USB2_USB20_CMCT_N → EL7303 → USB2_USB20_CONT_N
DLM0NSN900HY2D-GP

068.09002.2001
2ND = 68.02002.061

20200714
Change DY Part to 0201 Size

USB1_USB20_CMCB_P → EL7302 → USB1_USB20_CONB_P
USB1_USB20_CMCB_N → EL7302 → USB1_USB20_CONB_N
DLM0NSN900HY2D-GP

068.09002.2001
2ND = 68.02002.061

USB2_USB20_CMCB_P → EL7304 → USB2_USB20_CONB_P
USB2_USB20_CMCB_N → EL7304 → USB2_USB20_CONB_N
DLM0NSN900HY2D-GP

068.09002.2001
2ND = 68.02002.061

USB1_SSRX_RC_P0 ED7302
USB1_SSRX_RC_N0 ED7303
USB1_SSRX_RC_P1 ED7304
USB1_SSRX_RC_N1 ED7305
USB1_SSTX_RC_N0 ED7301
USB1_SSTX_RC_P1 ED7306
USB1_SSTX_RC_N1 ED7315
ED7316

PESD5V0H1BSFYL-GP-U1

083.5V0H1.00AF
2ND = 083.58017.00AF

20200714
Remove DY Part for layout space.

USB2_SSRX_RC_P0 ED7321
USB2_SSRX_RC_N0 ED7322
USB2_SSRX_RC_P1 ED7323
ED7324
USB2_SSTX_RC_P0 ED7325
USB2_SSTX_RC_N0 ED7326
USB2_SSTX_RC_P1 ED7327
USB2_SSTX_RC_N1 ED7328

PESD5V0H1BSFYL-GP-U1

083.5V0H1.00AF
2ND = 083.58017.00AF

20200714
Remove DY Part for layout space.

USB1_USB20_CONB_P ED7320
USB1_USB20_CONB_N ED7319
USB1_USB20_CONT_P ED7309
USB1_USB20_CONT_N ED7310
USB1_CON_CC1 ED7311
USB1_CON_CC2 ED7312
USB1_CON_SBU1 ED7313
USB1_CON_SBU2 ED7314

PESD5V0H1BSFYL-GP-U1

083.5V0H1.00AF
2ND = 083.58017.00AF

20200714
Remove DY Part for layout space.

USB2_USB20_CONB_P ED7330
USB2_USB20_CONB_N ED7331
USB2_USB20_CONT_P ED7332
USB2_USB20_CONT_N ED7333
USB2_CON_CC1 ED7334
USB2_CON_CC2 ED7335
USB2_CON_SBU1 ED7336
USB2_CON_SBU2 ED7337

PESD5V0H1BSFYL-GP-U1

083.5V0H1.00AF
2ND = 083.58017.00AF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

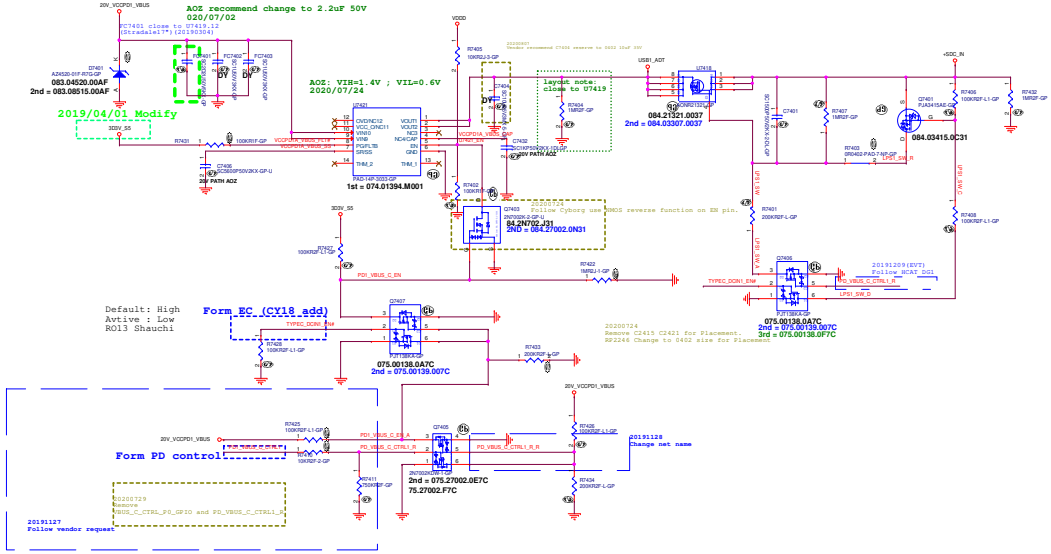
Size	Document Number	Rev
A2	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 73 of 106

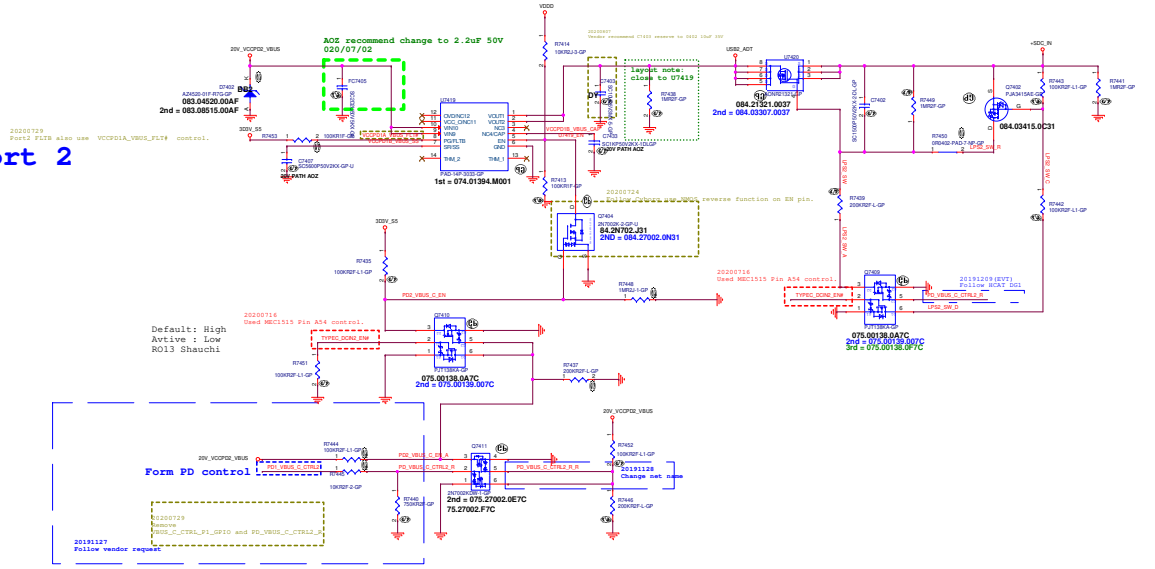
Main FUNC = LPS

Follow Hellcat15 Upsell TGL

TYPE-C Port 1



TYPE-C Port 2

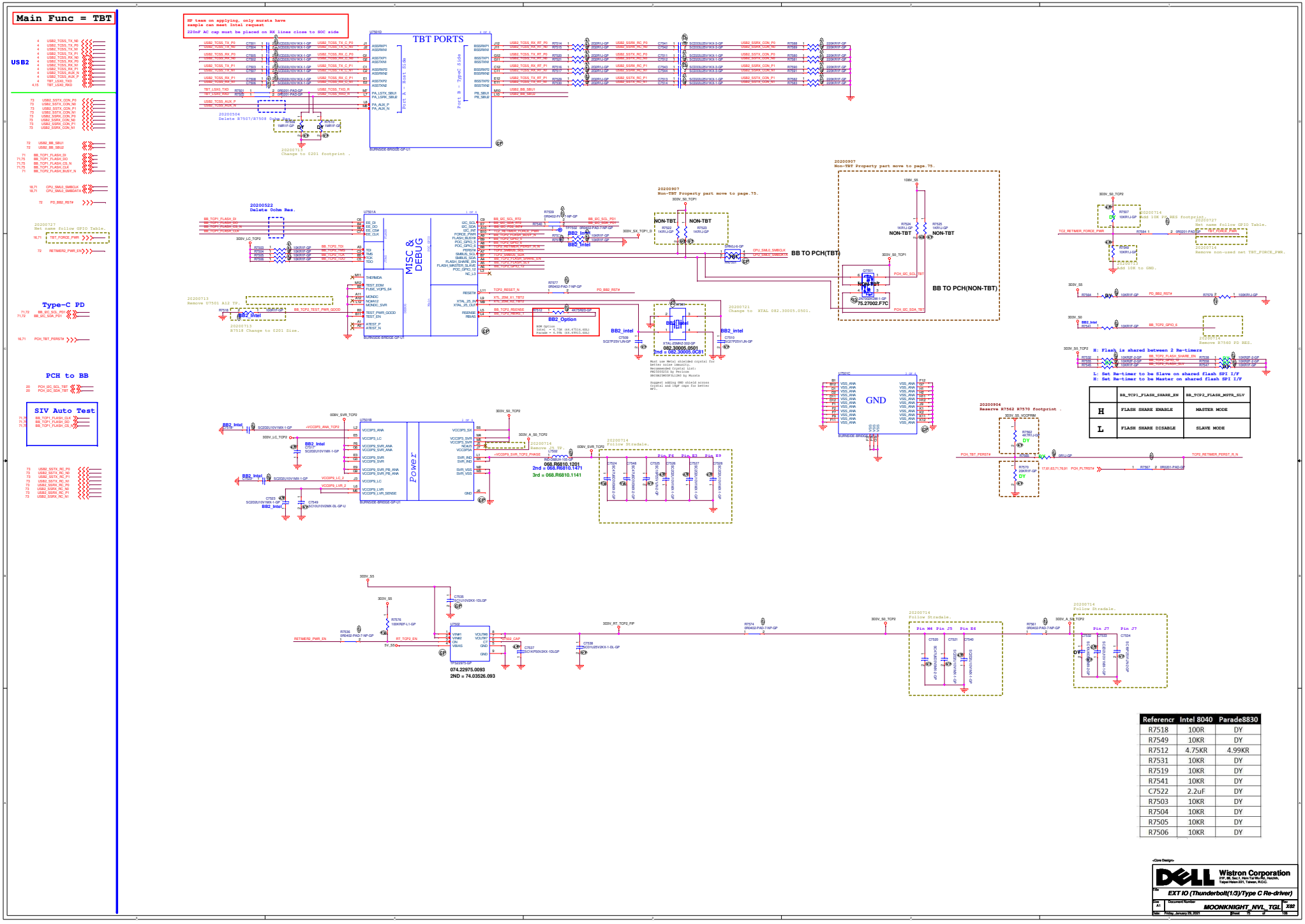


Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

EXT IO(LPS)

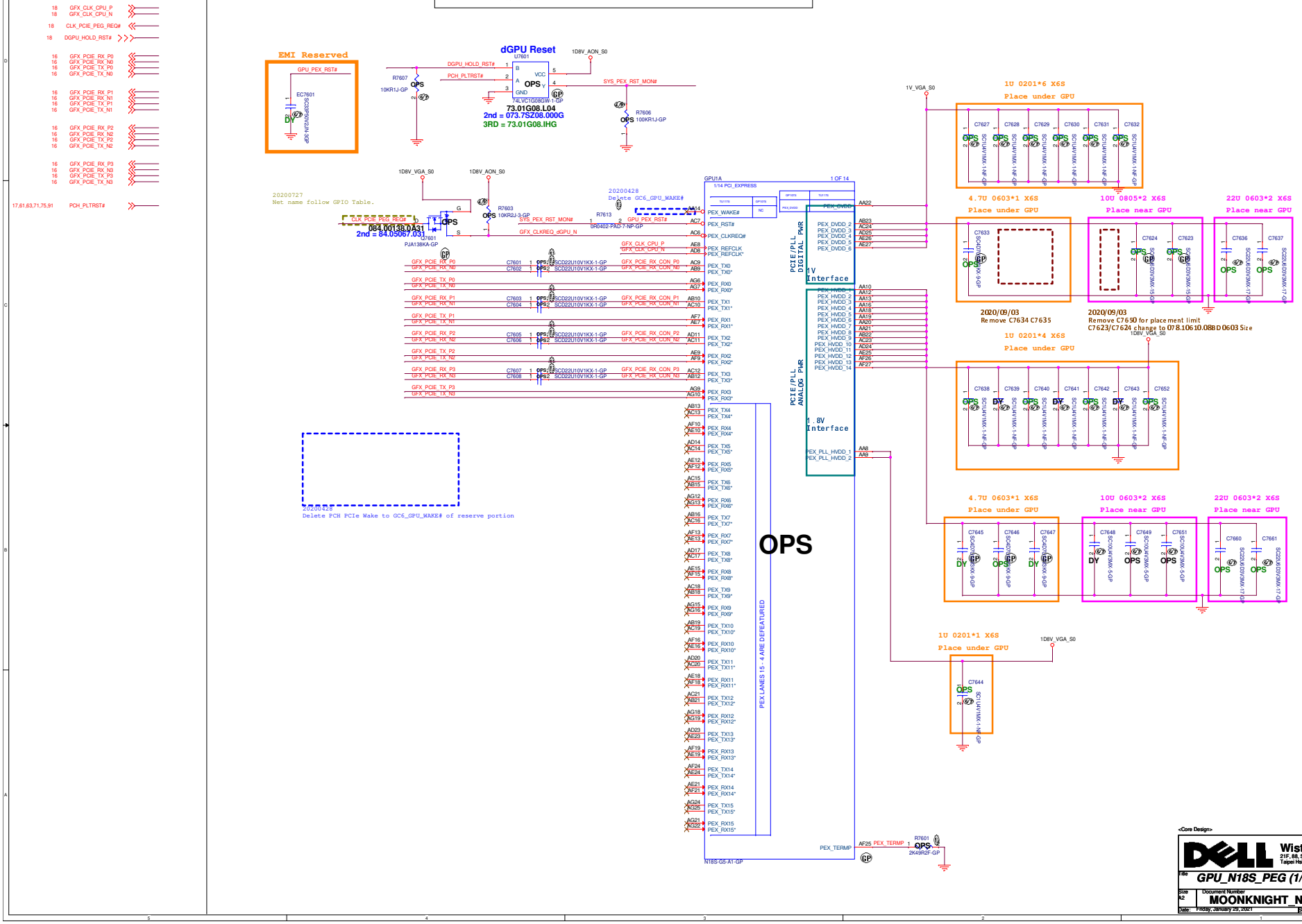
MOONKNIGHT_NVL_TGL

X02

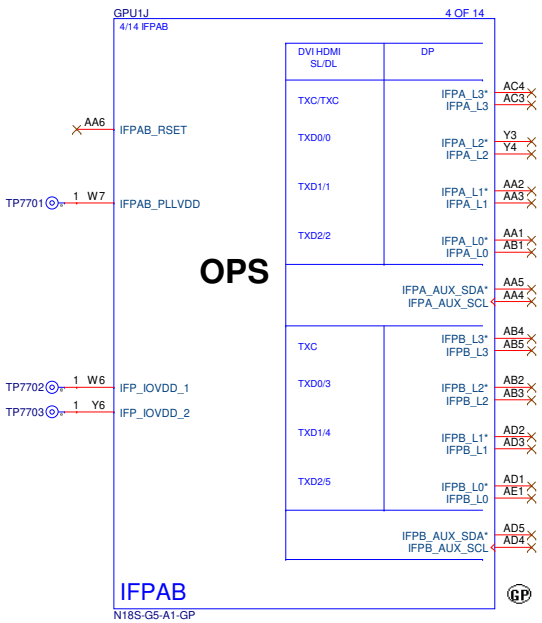


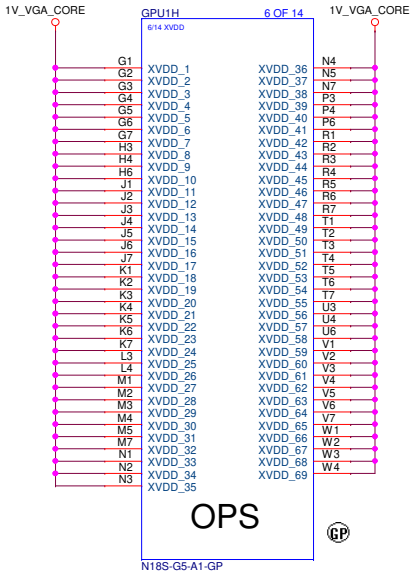
Referencr	Intel 8040	Parade8830
R7518	100R	DY
R7549	10KR	DY
R7512	4.75KR	4.99KR
R7531	10KR	DY
R7519	10KR	DY
R7541	10KR	DY
C7522	2.2uF	DY
R7503	10KR	DY
R7504	10KR	DY
R7505	10KR	DY
R7506	10KR	DY

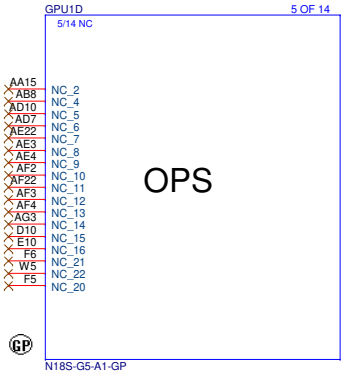
▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.



Main Func = dGPU







<Core Design>

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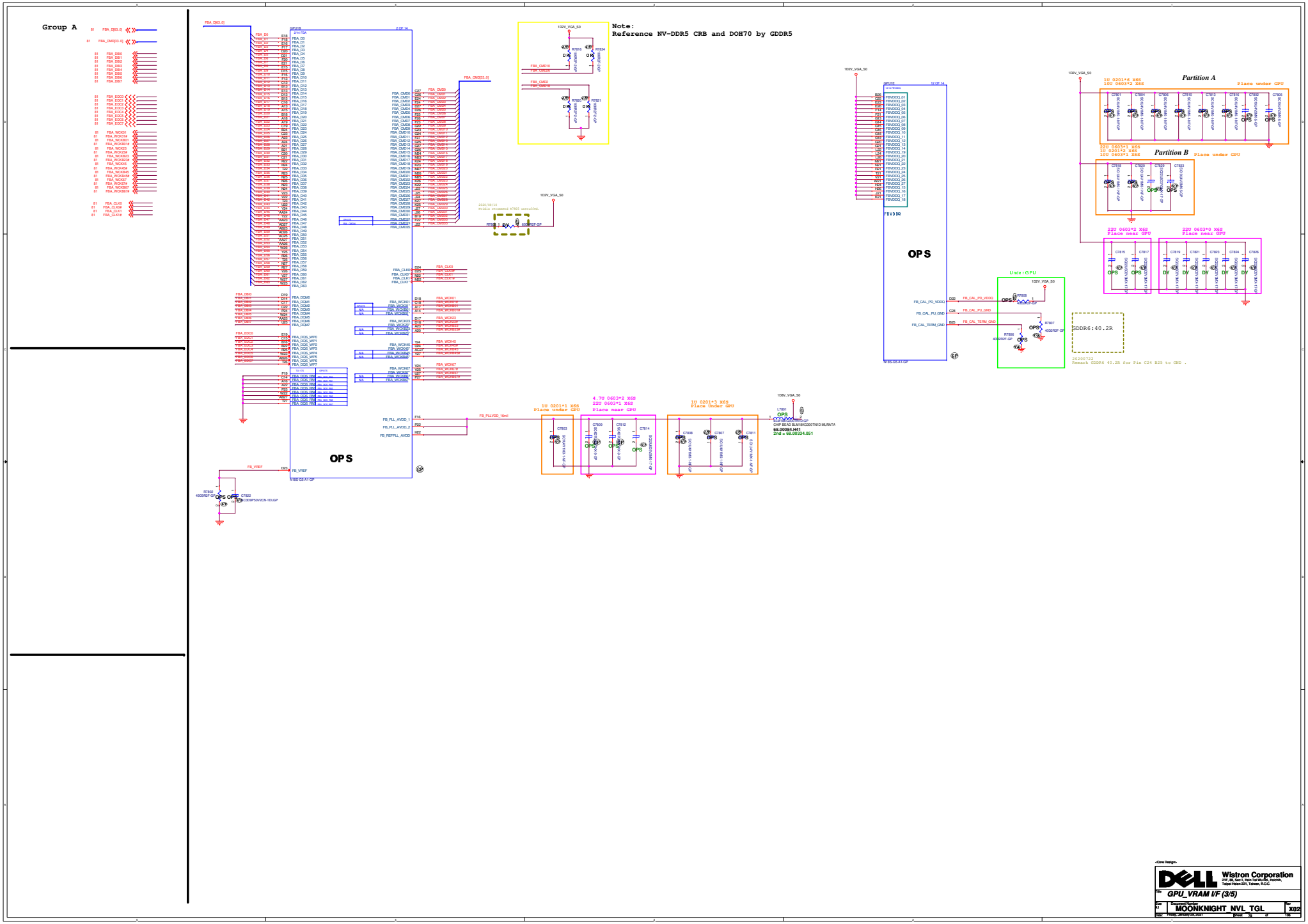
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU_DIGITALOUT (2/5)*

Size	Document Number	Rev
A3	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 77 of 106


Group A
Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5
OPS
Partition A
Partition B
Place under GPU
Under GPU
Place near GPU
Place Under GPU
SDDR6:40.2R
Wistron Corporation
GPU_VRAM I/F (3/5)
MOONKNIGHT_NVL_TGL
X02

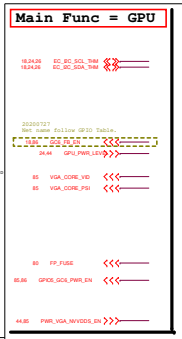


Table 12.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000) Samsung
L	L	H	1 (0x0001) Micron
L	H	L	2 (0x0002) Hynix
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Wistron Corporation	
File:	GPU_GPIO/STRAP
Project Code:	MOONKNIGHT_NVL_TGL
Document Number:	
Rev:	X02

Main Func = GPU

79 FP_FUSE
85 VGACORE_VDD_SENSE_1
85 VGACORE_GND_SENSE_1

RF RESERVED

22U 0603*10 X6S
Place under GPU

10U 0603*2 X6S
Place Close VRAM

10U 0603*12 X6S
Place under GPU

1U 0201*5 X6S
Place under GPU

1U 0201*2 X6S
Place under GPU

1V_VGA_CORE

GPU1C 11 OF 14

GPU1I 13 OF 14

GPU1G 7 OF 14

GPU1F 14 OF 14

VDD_SENSE
GND_SENSE
VGACORE_VDD_SENSE_1
VGACORE_GND_SENSE_1

OPTIONAL GND:
XVDD AREA
PCB ADR/CMD
PWR REFERENCE

OPS

1D8V_AON_S0

FP_FUSE_SRC

2020/08/10
Nvidia recommend PinG8 G9 NC

20200720
Reference U8610 change U8001

U8001
G5017B11U-GP

074.05017.009Z
2nd = 074.04622.009Z

Place near GPU
1U 0201*3 X6S
4.7U 0603*3 X6S

<Core Design>

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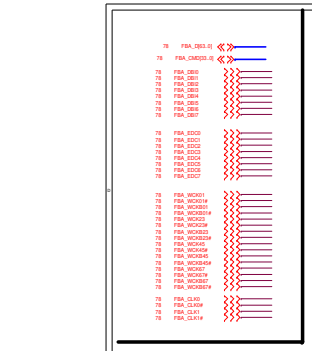
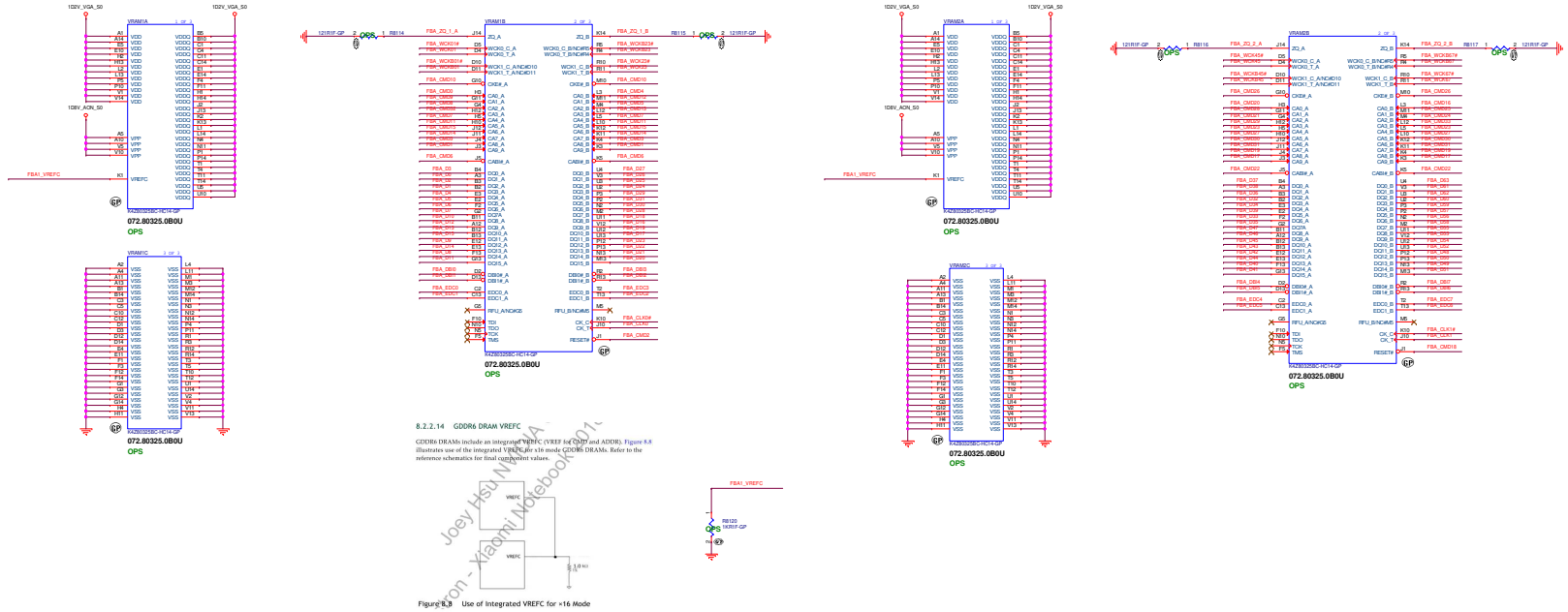
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER/GND (5/5)

Size	Document Number	Rev
A2	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 80 of 106

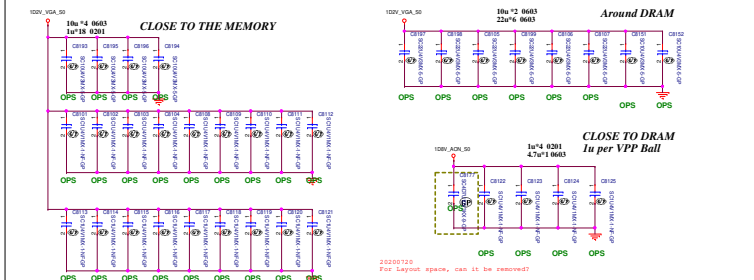


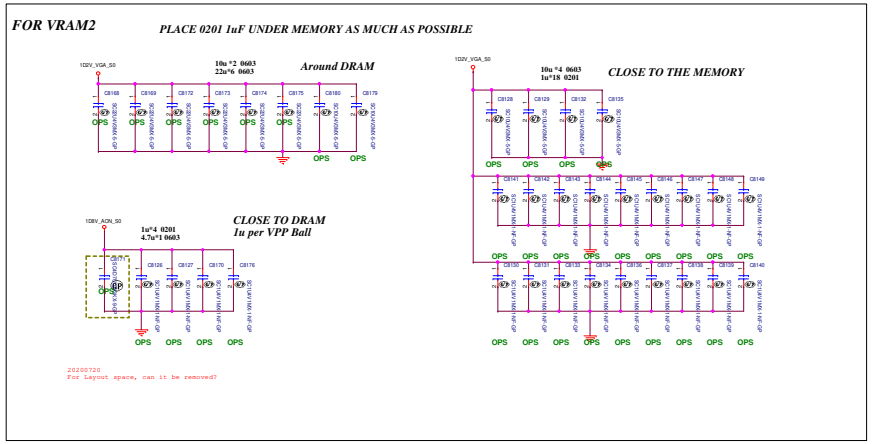


8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

Figure 8.8 Use of Integrated VREFC for ×16 Mode





«Core Design»
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: VRAM 1,2 (1/4)
Size: A3
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
Date: Friday, January 07, 2022
Sheet 81 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A4	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 82 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A4	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 83 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A4	MOONKNIGHT_NVL_TGL	X02

Date: Friday, January 29, 2021 Sheet 84 of 106

OFFPAGE-Signal

OFFPAGE-GAP

RT8816B For NVVDDS

VGA : N17S-G5
EDP-Continuous : 35A
EDP-Peak : 75A

1.Check Efisde
2. Modify DAT

PH on EE side

EE need check

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

For VGA_CORE sequence
EE need check

Table 1	
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

VGA : N17S-G5 / NVVDDS
EDP-Continuous : 35A
EDP-Peak : 75A

Modified, MKT NVL 13 EIV, 2020/03/05

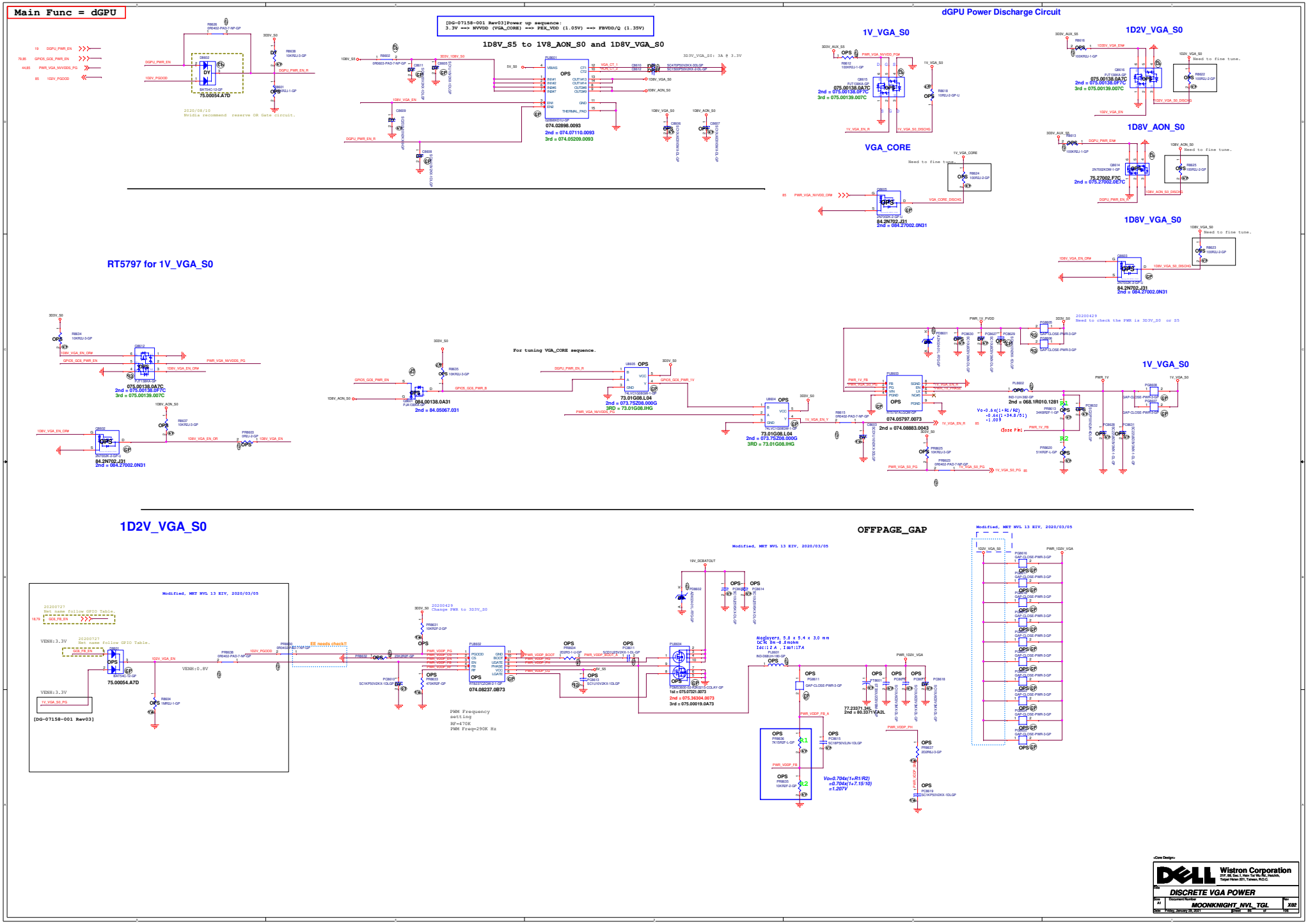
2020/09/03
PCB516 PCB519 Change to 0603 Size.

Wistron Corporation
3Fl, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

GPU (RT8816B_VGA)

MOONKNIGHT_NVL_TGL

X02


Main Func = dGPU
[DG-07158-001 Rev03]Power up sequence:
3.3V ==> NVVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> FBVDD/Q (1.35V)
1D8V_S5 to 1V8_AON_S0 and 1D8V_VGA_S0
dGPU Power Discharge Circuit
1V_VGA_S0
1D2V_VGA_S0
VGA_CORE
1D8V_AON_S0
1D8V_VGA_S0
RT5797 for 1V_VGA_S0
For tuning VGA_CORE sequence.
1V_VGA_S0
1D2V_VGA_S0
OFFPAGE_GAP
Modified, MKT NVL 13 EIV, 2020/03/05
[DG-07158-001 Rev03]
Wistron Corporation
DISCRETE VGA POWER
MOONKNIGHT_NVL_TGL
X02

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*MOONKNIGHT_NVL_TGL*	

Date: Friday, January 29, 2021 Sheet 87 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***MOONKNIGHT_NVL_TGL***	***X02***

Date: Friday, January 29, 2021 Sheet 88 of 106

Main Func = UnusedParts

Fix PCB BD, 2020/07/27

H2 HOLE268R162-GP — ZZ.00PAD.PW1
H12 HOLE268R162-GP — ZZ.00PAD.PW1
H15 HOLE268R162-GP — ZZ.00PAD.PW1

Fix PCB Edge , 2020/07/27

H16 HOLE256R142-OG-1-GP — ZZ.00PAD.6U1

FOR FAN, 2020/07/27

H4 HOLE256R142-OG-1-GP — ZZ.00PAD.6U1

FOR WLAN, 2020/07/27

HS2 STF237R113H81-GP — 434.0HH0K.0001

FOR SSD, 2020/07/27

HS1 STFT237B158R128H48-1-GP — 434.0HH0J.0001

FOR CPU, 2020/07/27

H17 HOLE233R150-GP — ZZ.00PAD.WN1
H18 HOLE233R150-GP — ZZ.00PAD.WN1
H19 HOLE233R150-GP — ZZ.00PAD.WN1
H20 HOLE233R150-GP — ZZ.00PAD.WN1

FOR GPU, 2020/07/27

H21 HOLE233R150-GP — ZZ.00PAD.WN1
H22 HOLE233R150-GP — ZZ.00PAD.WN1
H23 HOLE233R150-GP — ZZ.00PAD.WN1

Main Func = RF Capacitors

2020/04/20
Move from Page12
(FC1202, FC1201) to Page89

1P8V_S3
FC8903 SC20U6D3V5MX-DLGP
FC8904 SC20U6D3V5MX-DLGP

2020/04/20
Move from Page13
(FC1302, FC1301) to Page89

1P8V_S3
FC8907 SC20U6D3V5MX-DLGP
FC8908 SC20U6D3V5MX-DLGP

0D6V_VREF_S0
FC8905 SC20U6D3V5MX-DLGP
FC8906 SC20U6D3V5MX-DLGP

2020/04/20
Move from Page12
(FC1206, FC1205) to Page89

0D6V_VREF_S0
FC8905 SC20U6D3V5MX-DLGP
FC8910 SC20U6D3V5MX-DLGP

2020/04/20
Move from Page13
(FC1313,FC1314) to Page89

1V_CPU_CORE

RF 15pF * 3pcs
12pF * 3pcs

FC8901 SC15P50V2JN-DL-GP
FC8902 SC12P50V2JN-DL-GP
FC8911 SC15P50V2JN-DL-GP
FC8912 SC12P50V2JN-DL-GP
FC8913 SC15P50V2JN-DL-GP
FC8914 SC12P50V2JN-DL-GP

20200302
Follow Intel RF spec

2020/04/20
Move from Page10 to Page89
vaule please refer shiur.

20200302
Follow Intel RF spec

1D8V_VCCIN_AUX

RF 15pF * 3pcs
12pF * 4pcs
0.1uF*3pcs

2020/04/20
Move from Page10 to Page89
vaule please refer shiur.

FC8915 SC12P50V2JN-DL-GP
FC8916 SC15P50V2JN-DL-GP
FC8917 SC15P50V2JN-DL-GP
FC8918 SC12P50V2JN-DL-GP
FC8919 SC12P50V2JN-DL-GP
FC8920 SC15P50V2JN-DL-GP
FC8921 SC12P50V2JN-DL-GP

EMC CAPS - PLACE <4mm FROM SOC VDDQ,
WITH EACH PAIR <12mm APART

2020/04/20
Move from Page11 to Page89

1D1V_S3
FC8922 SC20U6D3V5MX-DLGP
FC8923 SC20U6D3V5MX-DLGP
FC8924 SC20U6D3V5MX-DLGP
FC8925 SC20U6D3V5MX-DLGP
FC8926 SC20U6D3V5MX-DLGP
FC8927 SC20U6D3V5MX-DLGP
FC8928 SC20U6D3V5MX-DLGP
FC8929 SC20U6D3V5MX-DLGP
FC8930 SC20U6D3V5MX-DLGP
FC8931 SC20U6D3V5MX-DLGP
FC8932 SC20U6D3V5MX-DLGP
FC8933 SC20U6D3V5MX-DLGP
FC8934 SC20U6D3V5MX-DLGP
FC8935 SC20U6D3V5MX-DLGP
FC8936 SC20U6D3V5MX-DLGP
FC8937 SC20U6D3V5MX-DLGP
FC8938 SC20U6D3V5MX-DLGP

2020/07/27
Move from Page11 to Page89

1D1V_S3
FC8939 SC22U6D3V5MX-DLGP
FC8940 SC22U6D3V5MX-DLGP
FC8941 SC22U6D3V5MX-DLGP

Main Func = EMI Capacitors

19V_DCBATOUT
EC8909 SCD1U16V2KX-3DLGP
EC8910 SCD1U16V2KX-3DLGP
EC8911 SCD1U16V2KX-3DLGP
EC8912 SCD1U16V2KX-3DLGP
EC8913 SCD1U16V2KX-3DLGP
EC8914 SCD1U16V2KX-3DLGP
EC8915 SCD1U16V2KX-3DLGP
EC8916 SCD1U16V2KX-3DLGP

1D8V_VCCIN_AUX
EC8945 SCD1U16V2KX-3DLGP
EC8946 SCD1U16V2KX-3DLGP
EC8947 SCD1U16V2KX-3DLGP

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Title: UNUSED PARTS/EMI Capacitors
Size: A2
Document Number: MOONKNIGHT_NVL_TGL
Rev: X02
Date: Friday, January 29, 2021
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Title: *(Reserved)*

Size	Document Number	Rev
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Main Func = TPM

20 TPM_SPI_IRQ#
17,61,63,71,75,76 PCH_PLTRST#
18,24,25 SPI0_CLK_CPU
15,18,24,25 SPI0_SI_CPU
18,24,25 SPI0_SO_CPU
18 SPI0_CS_CPU_N2
17,40 CPU_C10_GATE#

SIV Auto Test

96 SPI_CLK_TPM
96 SPI_SI_ROM_TPM
96 SPI_CS_TPM_N2

5mA

40mA

20200805
Change Res from 15ohm to 33ohm

20200724
U9101 GPIO0~6 follow Cyborg.

U9101
NPCT750JADYX-GP
071.00750.M003

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Title: INT IO (TPM)

Size	Document Number	Rev
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Main Func = FPR

16 FP1_USB20_N
16 FP1_USB20_P
24 FPR_SCAN#
24,64,66 KBC_PWRBTN#
17,40 SIO_SLP_S4#
20,24,67 LID_CL_SIO#

	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

GF5288WN1+GF128A+GM168 Module design

CN PIN Map

Pin NO.	INFO
1	VCC 3.3V
2	PWBTN
3	USB N
4	USB P
5	GND
6	LID closed
7	GPIO Key shielding
8	GND (ID pin)

3D3V_S5
R9212 100KR2J-1-GP
SIO_SLP_S4# Q9202 2N7002K-2-GP-U
84.2N702.J31
2ND = 084.27002.0N31
FP_EN# Q9201 PJA3415AE-GP
084.03415.0C31

20201005
Change RP9213 to 0402 size.

3D3V_FPR_VDD
FP1 PTWO-CON8-11-GP
FP_3D3V RP9213 0R0402-PAD-7-NP-GP

20200518
Remove KBC_PWRBTN# it move to IO1 conn

FP1_USB20_N R9209 0R0402-PAD-7-NP-GP FP1_USB20_CON_N
FP1_USB20_P R9210 0R0402-PAD-7-NP-GP FP1_USB20_CON_P
LID_CL_SIO D9201 RB520S30-GP LID_CL_SIO# FPR_SCAN#
3D3V_FPR_VDD R9201 100KR2J-1-GP
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

3D3V_FPR_VDD R9202 100KR2J-1-GP LID_CL_SIO#_R
ED9201
FP1_USB20_CON_N
FP1_USB20_CON_P
LID_CL_SIO#
AZ1043-04F-R7G-GP
075.01043.0073
2ND = 075.08810.0A73

C9201 SC1U10V2KX-1DLGP
20.K0767.008
2ND = 020.K0376.0008

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Title: *INT IO (Finger Printer)*

Size	Document Number	Rev
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Title: *(Reserved)*

Size	Document Number	Rev
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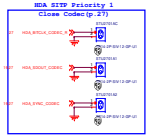
SITP DSN Template for 203046_Moonknight 13

HDA SITP Priority 1
Close CPU1(p.19)

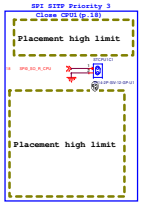
HDA SITP Priority 1
Close Codec(p.27)



ESPI SITP Priority 2
Close CPU(p.18)

ESPI SITP Priority 2
Close EC(p.24)

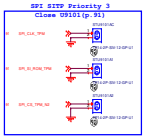
SPI SITP Priority 3
Close CPU1(p.18)



SPI SITP Priority 3
Close BIOS1(p.25)

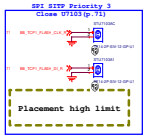
SPI SITP Priority 3
Close BIOS2(p.25)

SPI SITP Priority 3
Close U9101(p.91)



SPI SITP Priority 3
Close U7101(p.71)

SPI SITP Priority 3
Close U7103(p.71)



SPI SITP Priority 3
Close UTS01(p.73)

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Title

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Size	Document Number	Rev
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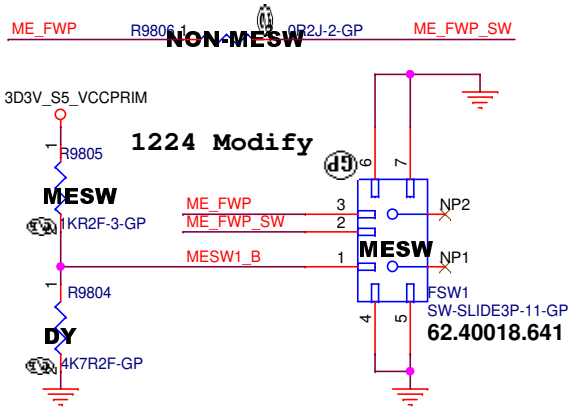
Main Func = SWITCH

24 ME_FWP
19 ME_FWP_SW

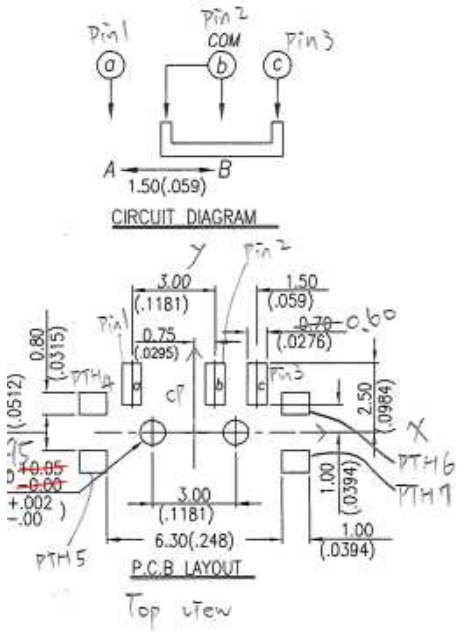
Firmware SW

Default setting:pull LOW
DY for MP



	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

*Symbol same as 62.40018.461



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Title: *CRT_Switch*

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Title: *Debug (XDP/HDT conn)*

Size	Document Number	Rev
B	MOONKNIGHT_NVL_TGL	X02

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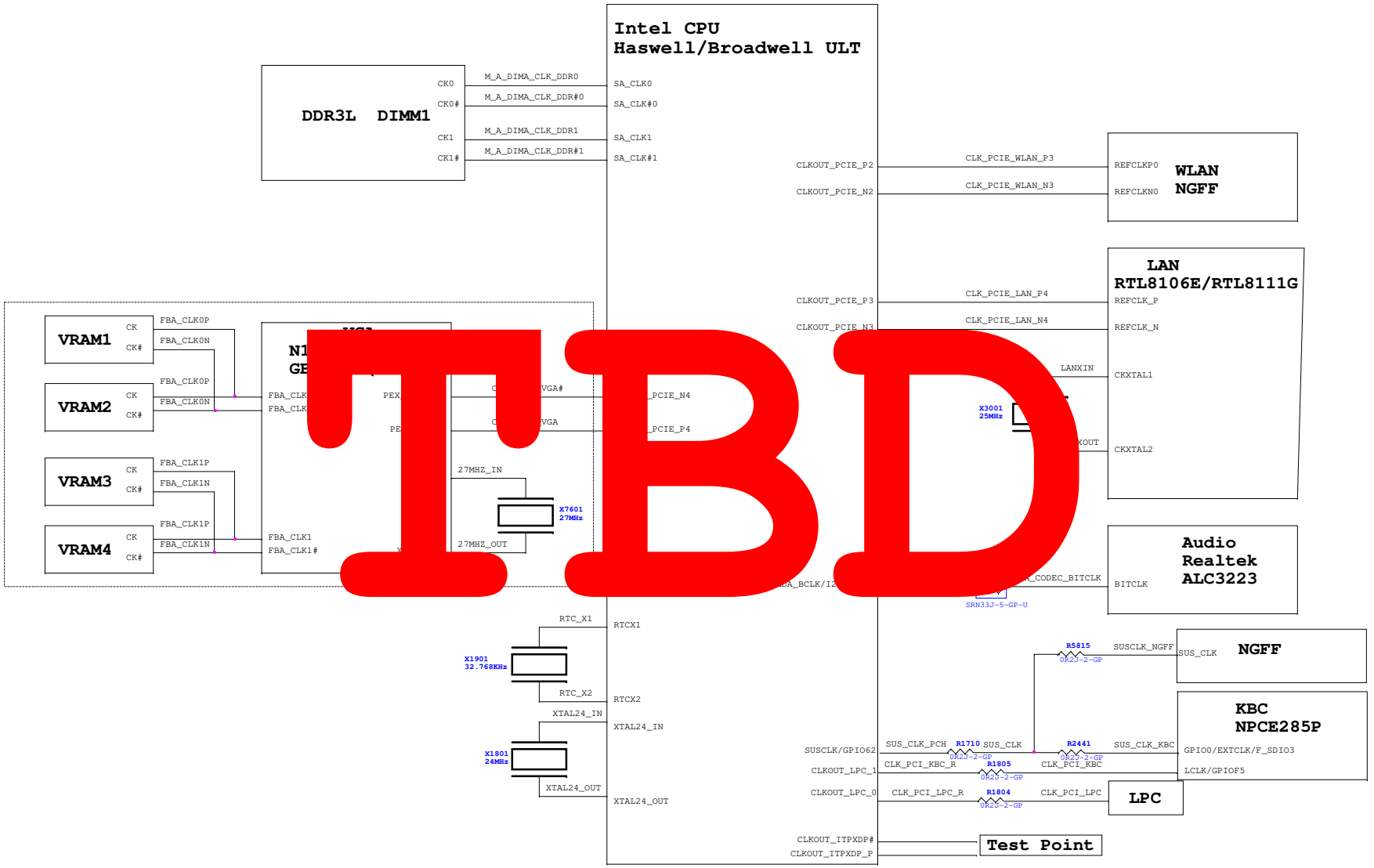
CLK Block Diagram



TBD

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Size: A2
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Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: *Change History*

Size	Document Number	Rev
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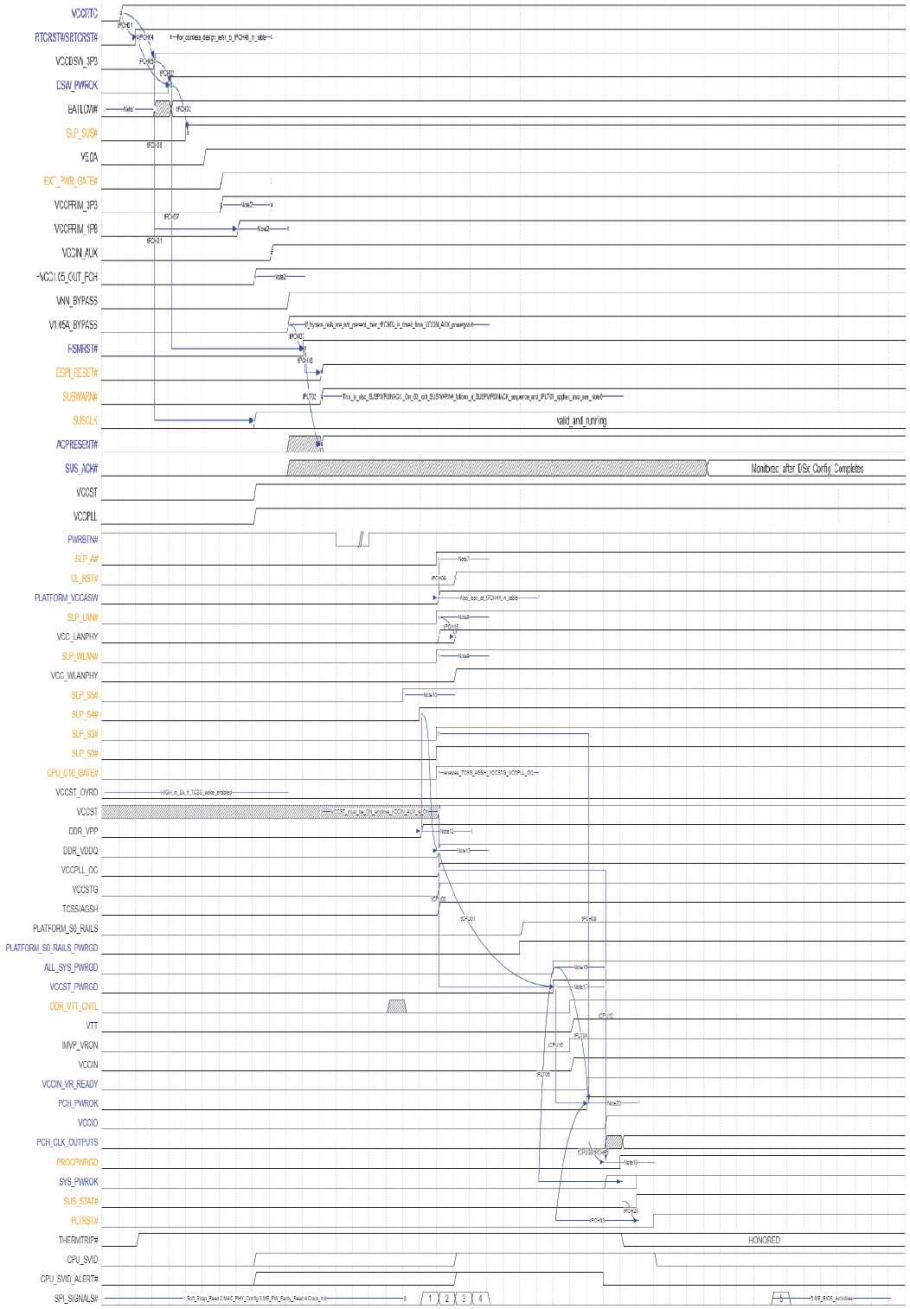
G3 to S5 Sequence



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DELL	**Wistron Corporation** 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Power Sequence***	
Size: A2	Document Number: ***MOONKNIGHT_NVL_TGL***	Rev: ***X02***
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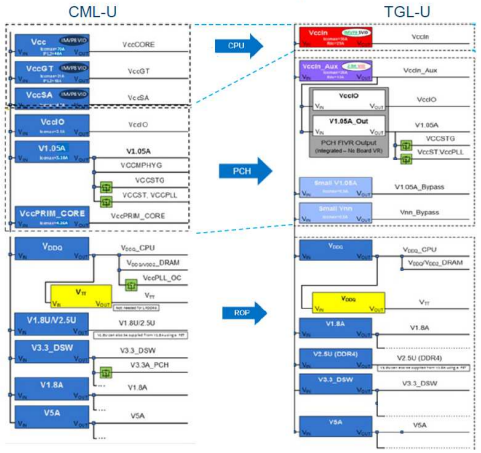
CML-U and TGL-U Power and VR Considerations (Cont..)

- TGL-U has IMVP9/FIVR implementation for both CPU and PCH power rails, whereas CML-U has IMVP8/discrete VRs for different power rails.
  - TGL-U IMVP9 Power map:
    - VCCIN: VCC_CORE and VCCGT
    - VCCIN_AUX: VCCSA, VCCIO, VNN, V1.05
  - CML-U IMVP8 Power map:
    - VCC_CORE
    - VCCGT
    - VCCSA



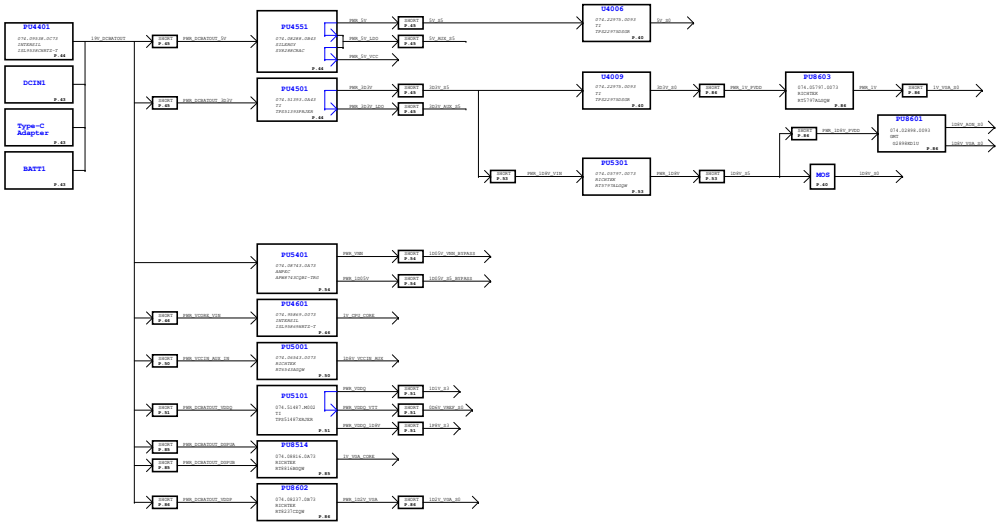


Table 10. Power Rail Descriptions for TGL U

Name	Description
VCCIN_AUX	**FIVR Input rail:** 1.8V
VCC_VNEXT_1P05	**Used for FIVR PRIM_CORE bypass mode during Sx**: 1.05V
VCC_V1P05EXT_1P05	**Used for FIVR PCH IO bypass mode during Sx:** 1.05V
VCCA_CLKLDO_1P8	**Analog supply for internal clocks:** 1.8V
VCCPRIM1P05 _OUT_PCH	**1.05V Primary Well**: for CNVi and other internal I/O blocks.
VCCDSW_1P05	**Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.
VCCPRIM_1P8	**1.8V Primary Well**.
VCCPRIM_3P3	**3.3V Primary Well**.
VCCPGPPR	**Audio Power 3.3V, 1.8V, or 1.5V**. If powered at 3.3V, the 3.3V supply can come from VCCPRIM_3P3 supply. If powered at 1.8V, the 1.8V supply can come from VCCPRIM_1P8 supply.
VCCDSW_3P3	**3.3V Deep Sx Well**.
VCCRTC	**RTC Well Supply**. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. *Notes:* 1. VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. 2. Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide (PDG) for implementation details.
VCCLDOSTD_0P85	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose.
VCC1P05 _OUT_FET	**FIVR output rail:** 1.05V, used for CPU rails VCCST/STG.
VSS	Ground

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Title: Power Block Diagram
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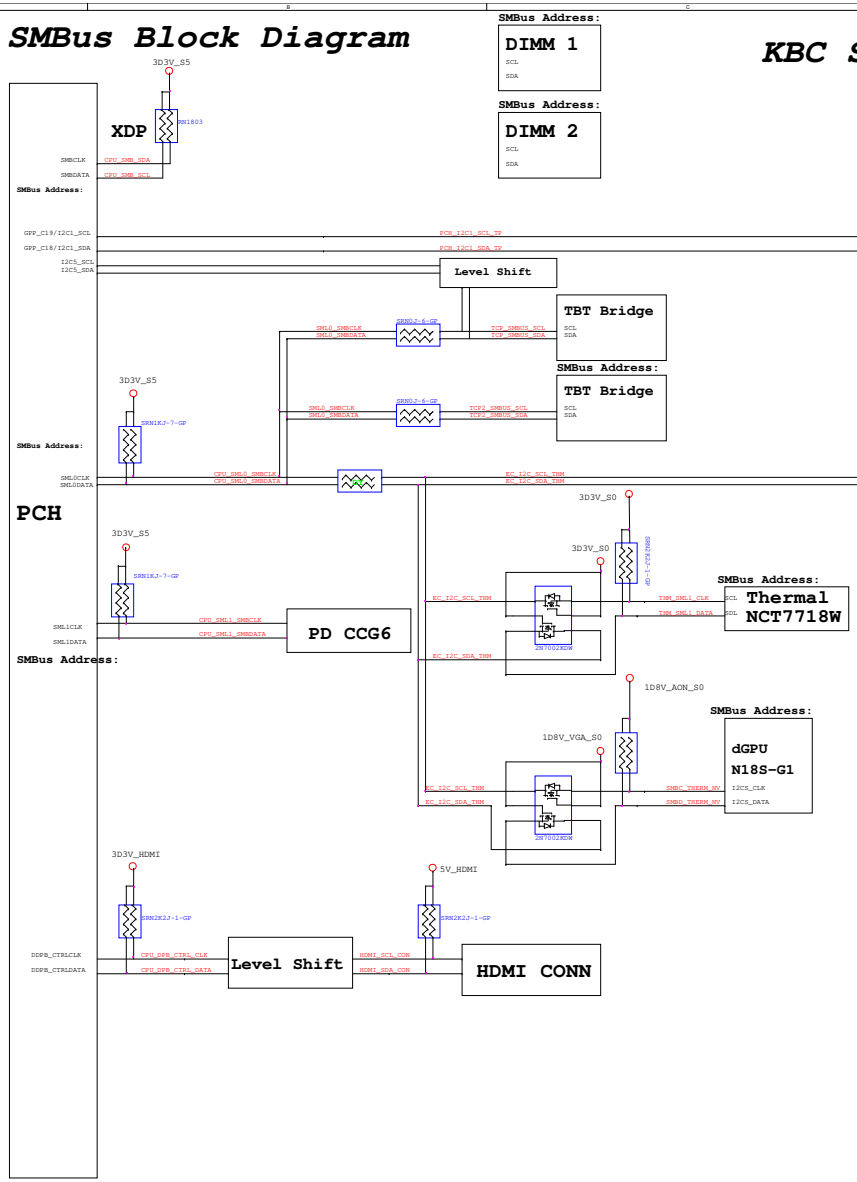
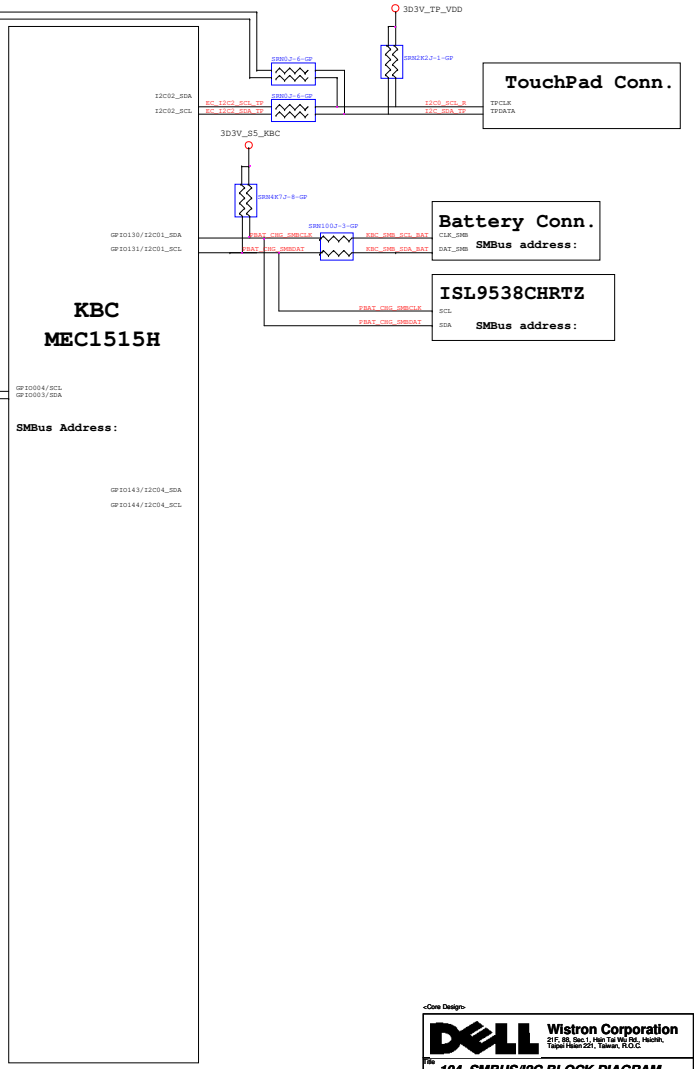
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title			
104_SMBUS/I2C BLOCK DIAGRAM			
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Title

Thermal/Audio Block Diagram

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Title: ***CLK Block***

Size	Document Number	Rev
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