1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X1798 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0025718024	ENGINEERING RELEASED	2020-10-14

LAST_MODIFICATION=Wed Oct 14 15:32:37 2020

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DRAWING TITLE: SCHEM,MLB-TGA,X1798

Apple Inc.

DRAWING NUMBER: 051-05371 | SIZE: D

REVISION: 6.0.0

BRANCH:

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05371	1	SCH,MLB,TGA,X1798	SCH	CRITICAL	
820-02009	1	PCBF,MLB,TGA,X1798	MLB	CRITICAL	
685-00338	1	COMMON PARTS,MLB,TGA,X1798	CMNPTS	CRITICAL	MLB_CMNPTS

BOM GROUP	BOM OPTIONS
X1798_COMMON	COMMON,ALTERNATE,ALT_CMN,BOOT_CONFIG2,EUSB_LS:B0_OTP6,ENET:1G,SE:PROD_SW_MU,SSD_2L,CODEC_WAKE_PU,DC:A
REF_DESKTOP	DESKTOP_COINCELL,PBUS_15P8VDCIN
X1798_TUNE	PCC,PCC_AVE,LOADISNS:Y
X1798_DEV	VITAMIN-C:NO

BOM GROUP	BOM OPTIONS		
J456_BOARDID	<rdar://55446207>	BOARDID3	BOARDID:001_01000
J457_BOARDID	<rdar://56207309>	BOARDID3,BOARDID1	BOARDID:001_01010

BoardRev

BOM GROUP	BOM OPTIONS	
J456_POC	BOARD_REV3,BOARD_REV2,BOARD_REV1,BOARD_REV0	0x0
J456_P1	BOARD_REV3,BOARD_REV2,BOARD_REV1	0x1
J456_P2	BOARD_REV3,BOARD_REV2, BOARD_REV0	0x2
J456_PEVT	BOARD_REV3,BOARD_REV2	0x3
J456_EVT	BOARD_REV3, BOARD_REV1,BOARD_REV0	0x4
J456_DVT	BOARD_REV3, BOARD_REV1	0x5

Module Parts

CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00815	1	SOC,TGA,B1+8G,8C,LP,C12,M,SCK,MCM2502	U0600	CRITICAL	CPU:8GB_MI
339S00817	1	SOC,TGA,B1+8G,8C,LP,C12,H,SCK,MCM2502	U0600	CRITICAL	CPU:8GB_HY
339S00831	1	SOC,TGA,B1+16G,8C,LP,D12,M,SCK,MCM2502	U0600	CRITICAL	CPU:16GB_MI
339S00833	1	SOC,TGA,B1+16G,8C,LP,D12,H,SCK,MCM2502	U0600	CRITICAL	CPU:16GB_HY

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00816	339S00815	CPU:8GB_MI	U0600	Lo Pwr, ATK package
339S00819	339S00815	CPU:8GB_MI	U0600	Hi Pwr, SCK package
339S00820	339S00815	CPU:8GB_MI	U0600	Hi Pwr, ATK package
339S00818	339S00817	CPU:8GB_HY	U0600	Lo Pwr, ATK package
339S00821	339S00817	CPU:8GB_HY	U0600	Hi Pwr, SCK package
339S00822	339S00817	CPU:8GB_HY	U0600	Hi Pwr, ATK package
339S00832	339S00831	CPU:16GB_MI	U0600	Lo Pwr, ATK package
339S00835	339S00831	CPU:16GB_MI	U0600	Hi Pwr, SCK package
339S00836	339S00831	CPU:16GB_MI	U0600	Hi Pwr, ATK package
339S00834	339S00833	CPU:16GB_HY	U0600	Lo Pwr, ATK package
339S00837	339S00833	CPU:16GB_HY	U0600	Hi Pwr, SCK package
339S00838	339S00833	CPU:16GB_HY	U0600	Hi Pwr, ATK package

DEV CPUs

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-23697	339S00815	CPU:8GB_MI	U0600	Lo Pwr, SCK package
998-23698	339S00815	CPU:8GB_MI	U0600	Lo Pwr, ATK package
998-24136	339S00815	CPU:8GB_MI	U0600	Lo Pwr, ASE package
998-23701	339S00815	CPU:8GB_MI	U0600	Hi Pwr, SCK package
998-23702	339S00815	CPU:8GB_MI	U0600	Hi Pwr, ATK package
998-24138	339S00815	CPU:8GB_MI	U0600	Hi Pwr, ASE package
998-23699	339S00817	CPU:8GB_HY	U0600	Lo Pwr, SCK package
998-23700	339S00817	CPU:8GB_HY	U0600	Lo Pwr, ATK package
998-24137	339S00817	CPU:8GB_HY	U0600	Lo Pwr, ASE package
998-23703	339S00817	CPU:8GB_HY	U0600	Hi Pwr, SCK package
998-23704	339S00817	CPU:8GB_HY	U0600	Hi Pwr, ATK package
998-24139	339S00817	CPU:8GB_HY	U0600	Hi Pwr, ASE package
998-23713	339S00831	CPU:16GB_MI	U0600	Lo Pwr, SCK package
998-23714	339S00831	CPU:16GB_MI	U0600	Lo Pwr, ATK package
998-24144	339S00831	CPU:16GB_MI	U0600	Lo Pwr, ASE package
998-23717	339S00831	CPU:16GB_MI	U0600	Hi Pwr, SCK package
998-23718	339S00831	CPU:16GB_MI	U0600	Hi Pwr, ATK package
998-24146	339S00831	CPU:16GB_MI	U0600	Hi Pwr, ASE package
998-23715	339S00833	CPU:16GB_HY	U0600	Lo Pwr, SCK package
998-23716	339S00833	CPU:16GB_HY	U0600	Lo Pwr, ATK package
998-24145	339S00833	CPU:16GB_HY	U0600	Lo Pwr, ASE package
998-23719	339S00833	CPU:16GB_HY	U0600	Hi Pwr, SCK package
998-23720	339S00833	CPU:16GB_HY	U0600	Hi Pwr, ATK package
998-24147	339S00833	CPU:16GB_HY	U0600	Hi Pwr, ASE package

PMICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00439	1	IC,PMU,Sera,B0,OTP-LPH-S1,WLCSP440	U8100	CRITICAL	<rdar://66012730>
343S00441	1	IC,PMU,Simetra,A1,OTP-LPG-S1,WLCSP196	U7700	CRITICAL	<rdar://62916971>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-23652	343S00439		U8100	Sera B0, OTP-LPH
998-22883	343S00441		U7700	Simetra A1. OTP-LPG

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00628	2	IC,PARROT,CD2E224,B0,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_OTP6

SE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-19915	1	IC,SN210V,CERES,DEV KEY,B1,SW=V7,WLCSP81	U5000	CRITICAL	SE:DEV_SW_V7
998-21255	1	IC,SN210V,B1,CERES,DEV,SW=H3,WLCSP81	U5000	CRITICAL	SE:DEV_SW_H3
338S00629	1	IC,SN210V,B1,CERES,DEV,SW=LN,WLCSP81	U5000	CRITICAL	SE:DEV_SW_LN
338S00630	1	IC,SN210V,B1,CERES,PROD,SW=MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU

NAND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00480	1	NAND,3DV4,160GB,S5E,256GB,TO,SLGA110	UN000	CRITICAL	NAND:256GB_TO
335S00462	1	NAND,3DV4,128GB,S5E,256GB,TO,SLGA110	UN100	CRITICAL	NAND:256GB_TO
335S00437	2	NAND,3DV5,128GB,S5E,512GB,H,SLGA110	UN000,UN100	CRITICAL	NAND:256GB_HY
335S00481	1	NAND,3DV4,288GB,S5E,256GB,TO,SLGA110	UN000	CRITICAL	NAND:512GB_TO
335S00464	1	NAND,3DV4,256GB,S5E,256GB,TO,SLGA110	UN100	CRITICAL	NAND:512GB_TO
335S00482	1	NAND,3DV5,320GB,S5E,512GB,H,SLGA110	UN000	CRITICAL	NAND:512GB_HY
335S00438	1	NAND,3DV5,256GB,S5E,512GB,H,SLGA110	UN100	CRITICAL	NAND:512GB_HY
335S00466	2	NAND,3DV4,512GB,S5E,256GB,TO,SLGA110	UN000,UN100	CRITICAL	NAND:1TB_TO
335S00483	1	NAND,3DV5,576GB,S5E,512GB,H,SLGA110	UN000	CRITICAL	NAND:1TB_HY
335S00439	1	NAND,3DV5,512GB,S5E,512GB,H,SLGA110	UN100	CRITICAL	NAND:1TB_HY
335S00468	2	NAND,3DV4,1TB,S5E,512GB,TO,SLGA110	UN000,UN100	CRITICAL	NAND:2TB_TO
335S00458	2	NAND,3DV5,1TB,S5E,512GB,H,SLGA110	UN000,UN100	CRITICAL	NAND:2TB_HY

DC/DC Sockets

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
939-00813	1	PCBA,Kanha,X1711	U0600	CRITICAL	CPU:SOCKET
939-00815	2	PCBA,Bandipur,X1711	UN000,UN100	CRITICAL	NAND:SOCKET

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BOM Configuration

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Main BOM Variants:

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00338	COMMON PARTS,MLB,TGA,X1798	X1798_COMMON,REF_DESKTOP,X1798_TUNE,J456_BOARDID,J456_DVT
985-01203	DEV PARTS,MLB,TGA,X1798	X1798_DEV

Configuration BOMs:

BOM NUMBER	BOM NAME	BOM OPTIONS
639-09115	PCBA,MLB,TGA, 8GB HY,256GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:256GB_TO
639-10654	PCBA,MLB,TGA, 8GB MI,256GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:256GB_TO
639-10997	PCBA,MLB,TGA,16GB HY,256GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:256GB_TO
639-10998	PCBA,MLB,TGA,16GB MI,256GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:256GB_TO
639-10999	PCBA,MLB,TGA, 8GB HY,256GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:256GB_HY
639-11000	PCBA,MLB,TGA, 8GB MI,256GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:256GB_HY
639-10655	PCBA,MLB,TGA,16GB HY,256GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:256GB_HY
639-10656	PCBA,MLB,TGA,16GB MI,256GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:256GB_HY
639-11003	PCBA,MLB,TGA, 8GB HY,512GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:512GB_TO
639-11004	PCBA,MLB,TGA, 8GB MI,512GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:512GB_TO
639-11001	PCBA,MLB,TGA,16GB HY,512GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:512GB_TO
639-11002	PCBA,MLB,TGA,16GB MI,512GB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:512GB_TO
639-13063	PCBA,MLB,TGA, 8GB HY,512GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:512GB_HY
639-13064	PCBA,MLB,TGA, 8GB MI,512GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:512GB_HY
639-13065	PCBA,MLB,TGA,16GB HY,512GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:512GB_HY
639-13066	PCBA,MLB,TGA,16GB MI,512GB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:512GB_HY
639-11007	PCBA,MLB,TGA, 8GB HY,1TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:1TB_TO
639-11008	PCBA,MLB,TGA, 8GB MI,1TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:1TB_TO
639-11005	PCBA,MLB,TGA,16GB HY,1TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:1TB_TO
639-11006	PCBA,MLB,TGA,16GB MI,1TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:1TB_TO
639-13040	PCBA,MLB,TGA, 8GB HY,1TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:1TB_HY
639-13041	PCBA,MLB,TGA, 8GB MI,1TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:1TB_HY
639-13042	PCBA,MLB,TGA,16GB HY,1TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:1TB_HY
639-13043	PCBA,MLB,TGA,16GB MI,1TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:1TB_HY
639-11011	PCBA,MLB,TGA, 8GB HY,2TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:2TB_TO
639-11012	PCBA,MLB,TGA, 8GB MI,2TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:2TB_TO
639-11009	PCBA,MLB,TGA,16GB HY,2TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:2TB_TO
639-11010	PCBA,MLB,TGA,16GB MI,2TB TO,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:2TB_TO
639-11646	PCBA,MLB,TGA, 8GB HY,2TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_HY,NAND:2TB_HY
639-11647	PCBA,MLB,TGA, 8GB MI,2TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU: 8GB_MI,NAND:2TB_HY
639-11648	PCBA,MLB,TGA,16GB HY,2TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_HY,NAND:2TB_HY
639-11649	PCBA,MLB,TGA,16GB MI,2TB HY,X1798	MLB_CMNPTS,ALTERNATE,CPU:16GB_MI,NAND:2TB_HY

DCDC BOM:

BOM NUMBER	BOM NAME	BOM OPTIONS
939-09871	PCBA,MLB,NO CPU/MEM,NO SSD,X1798	MLB_CMNPTS,ALTERNATE,CPU:SOCKET,NAND:SOCKET

SYNC_MASTER=karrim SYNC_DATE=09/15/2020

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Top Side MCO Parts

LS COWLING BOSS

J456

ZT0410
3.0OD1.75ID-1.65H-SM
CRITICAL
860-01577
PACK_OPTION=J456

ZT0411
3.0OD1.75ID-1.65H-SM
CRITICAL
860-01577
PACK_OPTION=J456

ZT0412
3.0OD1.75ID-1.65H-SM
CRITICAL
860-01577
PACK_OPTION=J456

USB-C COWLING BOSS

J457

ZT0413
3.0OD1.75ID-1.55H-SM
CRITICAL
860-01807
PACK_IGNORE=TRUE
PACK_OPTION=J457

ZT0414
3.0OD1.75ID-1.55H-SM
CRITICAL
860-01807
PACK_IGNORE=TRUE
PACK_OPTION=J457

ENCLOSURE SPACER

ZT0420
BOSS-3.45OD1.12H-1.8NP-2P-SM
CRITICAL
860-01581

ZT0421
BOSS-3.45OD1.12H-1.8NP-2P-SM
CRITICAL
860-01581
PACK_IGNORE=TRUE
PACK_OPTION=J457

ZT0422
BOSS-3.45OD1.12H-1.8NP-2P-SM
CRITICAL
860-01581
PACK_IGNORE=TRUE
PACK_OPTION=J457

ZT0423
BOSS-3.45OD1.12H-1.8NP-2P-SM
CRITICAL
860-01581
PACK_IGNORE=TRUE
PACK_OPTION=J457

Bottom Side MCO Parts

THERMAL MOD BOSS

860-01602
ZT0440
BOSS-3.6OD2.36H-1.8NP-2P-SM
PACK_OPTION=J456

ANTENNA GROUND TAB BOSS

ZT0460
BOSS-3.0OD1.75ID-1.25H-SM
CRITICAL
860-01582

ZT0461
BOSS-3.0OD1.75ID-1.25H-SM
CRITICAL
860-01582

ZT0462
BOSS-3.0OD1.75ID-1.25H-SM
CRITICAL
860-01582

ZT0463
BOSS-3.0OD1.75ID-1.25H-SM
CRITICAL
860-01582

ZT0464
BOSS-3.0OD1.75ID-1.25H-SM
CRITICAL
860-01582

ZT0465
BOSS-3.0OD1.75ID-1.25H-SM
CRITICAL
860-01582

SOC Heatsink Parts

CPU THERM STAGE HOLES 3.15 MM

ZT0400
3P9R3P15
OMIT
998-0845

CPU THERM STAGE HOLES 3.6 MM

ZT0401
4.0R3.6-NSP
OMIT
998-03850

ZT0402
4.0R3.6-NSP
OMIT
998-03850

CPU THERM STAGE SLOT 3.15 x 4.00 MM

ZT0403
TH-NSP
3.15X3.65-4.0X4.5
OMIT
998-21397

WIFI Shield Can SLOT

ZT0430
TH-NSP
SL-1.3X0.5-1.8X1.0
OMIT
998-10777

ZT0431
TH-NSP
SL-1.3X0.5-1.8X1.0
OMIT
998-10777

WIFI Shield Can

SH0430
SM
SHLD-CU-ALOY-X1797
806-26653

METAL SLED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-24419	2	SLED,METAL,X1798	SLED1,SLED2	CRITICAL	

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=michael
SYNC_DATE=02/26/2020
PAGE TITLE
PD Parts

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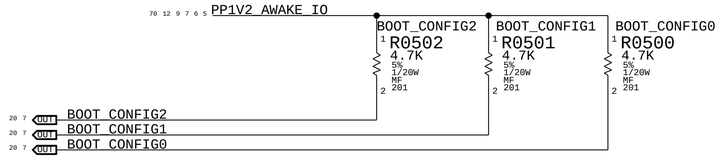
OK2INTEGRATE

BOOT CONFIG ID

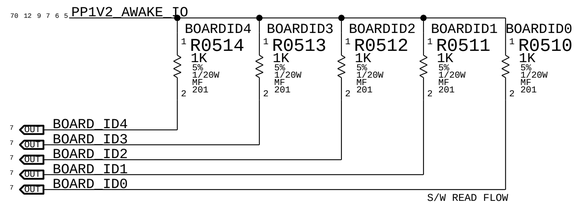


BOOT_CFG[2:0]	MODE
000	SPI1 NOR (12 MHZ)
001	SPI1 NOR (12 MHZ) TESTMODE
010	SPI0 NAND
011	SPI0 NAND TESTMODE
POR ---> 100	SPI1 NOR (40 MHZ)
101	SPI1 NOR (40 MHZ) TESTMODE
110	SPI1 NOR (6 MHZ)
111	SPI1 NOR (6MHZ) TESTMODE

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

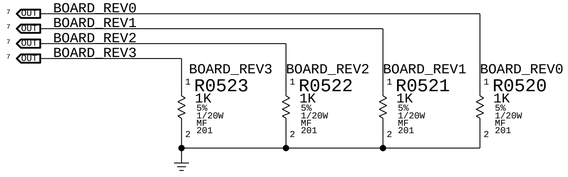


S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

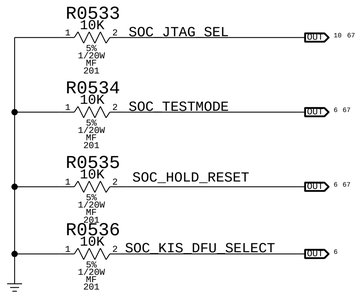
NOTE: STUFFING RESISTOR MEANS 0



board rev should start at 0b0000 and increment each rev.

S/W READ FLOW

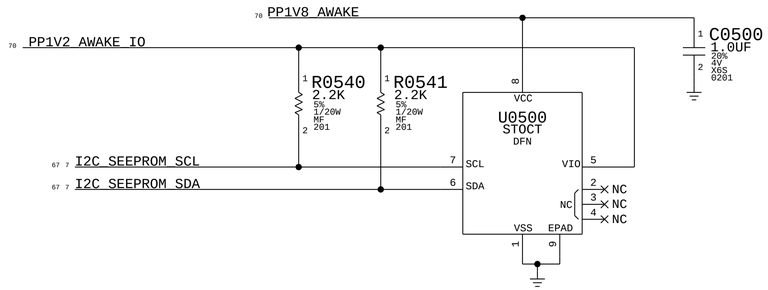
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ



SEP EEPROM (128-Kbit)

(Write: 0xA2, Read 0xA3)

APN:335S00455



OCELOT I2C pulls

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
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BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: Support

Apple Inc.

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OK2INTEGRATE

SOC: CIO, USB, DRAM, RESETS, CLOCKS, SWD, FPWM

OMIT_TABLE

U0600
TMLR68A0-B09
BGA
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68 67 33 10 IN	PMU_RESET_L	R2	LP4_IN_RESET_N	
68 67 46 33 6 IN	SOC_FORCE_DFU	AA49	FORCE_DFU	
6	SOC_REQUEST_DFU1	AK55	REQUEST_DFU1	
6	SOC_REQUEST_DFU2	AJ54	REQUEST_DFU2	
67 5 IN	SOC_TESTMODE	AD2	TESTMODE IPD	RESET
68 67 48 46 33 IN	PMU_ACTIVE_READY	AL54	CFSB	
67 5 IN	SOC_HOLD_RESET	AC1	HOLD_RESET IPD	
5	SOC_KIS_DFU_SELECT	AB49	KIS_DFU_SELECT	
45 BI	EUSB_ATC0_P	BB54	ATC0_USB_EDP	
45 BI	EUSB_ATC0_N	BB55	ATC0_USB_EDM	
44 IN	CIO_ATC0_LSRX_1V2	BE18	USB_C0_LSRX	
44 OUT	CIO_ATC0_LSTX_1V2	BE13	USB_C0_LSTX	
6	SOC_ATC0_USB_RESREF	BB53	ATC0_USB_RESREF	
	TP_ATC0_HPD	V48	USB_C0_HPD/TMU_CLK_OUT0	
45 BI	EUSB_ATC1_P	BC54	ATC1_USB_EDP	
45 BI	EUSB_ATC1_N	BC55	ATC1_USB_EDM	
44 IN	CIO_ATC1_LSRX_1V2	BD3	USB_C1_LSRX	
44 OUT	CIO_ATC1_LSTX_1V2	BE10	USB_C1_LSTX	
6	SOC_ATC1_USB_RESREF	BC53	ATC1_USB_RESREF	
	TP_ATC1_HPD	R48	USB_C1_HPD/TMU_CLK_OUT1	
67 6	USB_VBUS_DETECT	AG1	EUSB_VBUS_DETECT	
46 BI	USBC_ATC0_D2R_P<1>	BE50	ATCPHY0_RX0_P	ATC
46 BI	USBC_ATC0_D2R_N<1>	BF50	ATCPHY0_RX0_N	
46 OUT	USBC_ATC0_R2D_C_P<1>	BC49	ATCPHY0_TX0_P	
46 OUT	USBC_ATC0_R2D_C_N<1>	BD49	ATCPHY0_TX0_N	
46 BI	USBC_ATC0_D2R_P<2>	BE48	ATCPHY0_RX1_P	
46 BI	USBC_ATC0_D2R_N<2>	BF48	ATCPHY0_RX1_N	
46 OUT	USBC_ATC0_R2D_C_P<2>	BC47	ATCPHY0_TX1_P	
46 OUT	USBC_ATC0_R2D_C_N<2>	BD47	ATCPHY0_TX1_N	
67 46 BI	USBC_ATC0_AUX_P	AY51	ATCPHY0_AUX_P	
67 46 BI	USBC_ATC0_AUX_N	AY52	ATCPHY0_AUX_N	
6	SOC_ATCPHY0_RCAL_POS	BE52	ATCPHY0_RCAL_P	
6	SOC_ATCPHY0_RCAL_NEG	BF52	ATCPHY0_RCAL_N	
46 BI	USBC_ATC1_D2R_P<1>	BF44	ATCPHY1_RX0_P	
46 BI	USBC_ATC1_D2R_N<1>	BE44	ATCPHY1_RX0_N	
46 OUT	USBC_ATC1_R2D_C_P<1>	BD43	ATCPHY1_TX0_P	
46 OUT	USBC_ATC1_R2D_C_N<1>	BC43	ATCPHY1_TX0_N	
46 BI	USBC_ATC1_D2R_P<2>	BF46	ATCPHY1_RX1_P	
46 BI	USBC_ATC1_D2R_N<2>	BE46	ATCPHY1_RX1_N	
46 OUT	USBC_ATC1_R2D_C_P<2>	BD45	ATCPHY1_TX1_P	
46 OUT	USBC_ATC1_R2D_C_N<2>	BC45	ATCPHY1_TX1_N	
46 BI	USBC_ATC1_AUX_P	BA52	ATCPHY1_AUX_P	
46 BI	USBC_ATC1_AUX_N	BA51	ATCPHY1_AUX_N	
6	SOC_ATCPHY1_RCAL_POS	BF42	ATCPHY1_RCAL_P	
6	SOC_ATCPHY1_RCAL_NEG	BE42	ATCPHY1_RCAL_N	

GND_VOID=TRUE

DFU_STATUS	V51	SOC_DFU_STATUS	OUT 45 46 67 68	
CLOCKS	XI0	BE36 SOC_XTAL24M_IN		
	XO0	BF36 SOC_XTAL24M_OUT		
	TST_CLKOUT	P54 TP_TST_CLKOUT	67	
	ANALOGMUX_OUT	AL48 TP_SOC_AMUX_OUT	OUT 72	
SWD	SWD_TCK_OUT1	AJ1 SWD_NAND0_SWCLK	OUT 67 72	
	SWD_TMS2	U54 SWD_NAND0_SWDIO	BI 67 72	
	SWD_TMS3	V54 TP_SWD_TMS3		
	SWD_TMS4	AH3 TP_SWD_TMS4		
FPW	FPWM0/MASTER_SYNC_GEN_0	V50 WLAN_TIME_SYNC	IN 51	IPD
	FPWM1	Y49 NC_KBD_BKLT_PWM	OUT 73	
	FPWM2	U50 NC_FPWM2	73	

AMUX_OUT can go to TP or to AMUX_IN on PMU

R0651 499 1% 1/20W MF 201
CRITICAL Y0600 1.00X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
SOC_24M_O_R
CRITICAL C0650 15PF 5% 50V C0G 0201
CRITICAL C0651 15PF 5% 50V C0G 0201

6 SOC_ATCPHY0_RCAL_POS → R0600 200 1% 1/20W MF 201
6 SOC_ATCPHY0_RCAL_NEG → C0600 10PF 5% 25V C0G 0201
6 SOC_ATCPHY1_RCAL_POS → R0601 200 1% 1/20W MF 201
6 SOC_ATCPHY1_RCAL_NEG → C0601 10PF 5% 25V C0G 0201

70 12 9 7 6 5 PP1V2_AWAKE_IO → R0630 10K 5% 1/20W MF 201 → 6 SOC_REQUEST_DFU1
70 12 9 7 6 5 PP1V2_AWAKE_IO → R0631 10K 5% 1/20W MF 201 → 6 SOC_REQUEST_DFU2
68 67 46 33 6 SOC_FORCE_DFU → R0632 47K 5% 1/20W MF 201

6 SOC_ATC0_USB_RESREF → R0641 200 1% 1/20W MF 201
6 SOC_ATC1_USB_RESREF → R0640 200 1% 1/20W MF 201

70 12 9 7 6 5 PP1V2_AWAKE_IO → R0639 0 5% 1/20W MF 0201 → 67 6 USB_VBUS_DETECT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON,24MHZ.XTAL
197S0588	197S0591		Y0600	TXC,24MHZ,XTAL

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020
PAGE TITLE
SOC: CIO, USB, RESETS, CLOCKS, SWD

Apple Inc.

DRAWING NUMBER 051-05371 SIZE D
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OK2INTEGRATE

all signals are 1.2 unless otherwise specified.
all signals on this page reference PP1V2_AWAKE_GRP if they are 1.2V
if they are 1.8V they reference PP1V8_AWAKE_GRP

SOC: I/Os

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I2S

72 OUT	TDM_SPKRAMP_L_BCLK_R	AK4	I2S0_BCLK			
73 IN	NC_TDM_SPKRAMP_L_D2R	AJ3	I2S0_DIN	IPD		
72 OUT	TDM_SPKRAMP_L_R2D_R	AJ5	I2S0_DOUT			
72 OUT	TDM_SPKRAMP_L_FSYNC_R	AJ4	I2S0_LRCK			
73	NC_SOC_I2S0_MCK	AK3	I2S0_MCK			
20 OUT	TDM_SPKRAMP_R_BCLK_R	AG3	I2S1_BCLK			
73 IN	NC_TDM_SPKRAMP_R_D2R	AF3	I2S1_DIN	IPD		
20 OUT	TDM_SPKRAMP_R_R2D_R	AG4	I2S1_DOUT			
20 OUT	TDM_SPKRAMP_R_FSYNC_R	AF2	I2S1_LRCK			
73	NC_SOC_I2S1_MCK	AG2	I2S1_MCK			
20 OUT	TDM_CODEC_BCLK_R	AK5	I2S2_BCLK			
67 63 IN	TDM_CODEC_D2R	AL6	I2S2_DIN	IPD		
20 OUT	TDM_CODEC_R2D_R	AJ7	I2S2_DOUT			
20 OUT	TDM_CODEC_FSYNC_R	AM4	I2S2_LRCK			
73	NC_SOC_I2S2_MCK	AK6	I2S2_MCK			
73	NC_I2S3_BCLK	AH6	I2S3_BCLK			
73	NC_I2S3_D2R	AH4	I2S3_DIN			
73	NC_I2S3_R2D	AG5	I2S3_DOUT			
73	NC_I2S3_LRCLK	AJ6	I2S3_LRCK			
73	NC_I2S3_MCLK	AF5	I2S3_MCK			

SPI

			SPI0_MISO	IPD	AL4	BOOT_CONFIG2 IN 5 20
			SPI0_MOSI		AK2	BOOT_CONFIG1 OUT 5 20
			SPI0_SCLK		AK1	BOOT_CONFIG0 OUT 5 20
			SPI1_MISO	IPD	AD4	SPI_SOCROM_MISO IN 19
			SPI1_MOSI		AE4	SPI_SOCROM_MOSI_R OUT 19
			SPI1_SCLK		AF4	SPI_SOCROM_CLK_R OUT 19
			SPI1_SSIN		AE3	SPI_SOCROM_CS_L OUT 19
			SPI2_MISO	IPD	AF53	NC_SPI_1V8_TOUCHID_MISO IN 73
			SPI2_MOSI		AF54	NC_SPI_1V8_TOUCHID_MOSI_R OUT 73
			SPI2_SCLK		AF55	NC_SPI_1V8_TOUCHID_CLK_R OUT 73
			SPI2_SSIN		AF52	NC_SOC_SPI2_SSIN 73
			SPI3_MISO		Y1	NC_SPI_IPD_MISO IN 73
			SPI3_MOSI		W1	NC_SPI_IPD_MOSI_R OUT 73
			SPI3_SCLK		AB1	NC_SPI_IPD_CLK_R OUT 73
			SPI3_SSIN		AA1	NC_SPI_IPD_CS_L OUT 73
			SPI4_MISO	IPD	AC4	SPI_TCON_MISO IN 57 67
			SPI4_MOSI		AB4	SPI_TCON_MOSI_R OUT 20
			SPI4_SCLK		AA4	SPI_TCON_CLK_R OUT 20
			SPI4_SSIN		AB3	SPI_TCON_CS_L OUT 57 67

1.8V IO

I2C

67 46 38 23 OUT	I2C_UPC_SCL	W52	I2C0_SCL			
67 46 38 23 BI	I2C_UPC_SDA	V52	I2C0_SDA			
67 38 OUT	I2C_SPKRAMP_L_SCL	AA48	I2C1_SCL			
67 38 BI	I2C_SPKRAMP_L_SDA	Y48	I2C1_SDA			
73 OUT	NC_I2C_CODEC_SCL	AB50	I2C2_SCL			
73 BI	NC_I2C_CODEC_SDA	Y50	I2C2_SDA			
38 OUT	I2C_SPKRAMP_R_SCL	AF6	I2C3_SCL			
38 BI	I2C_SPKRAMP_R_SDA	AE6	I2C3_SDA			
38 OUT	NC_I2C_DFR_SCL	AF50	I2C4_SCL			
38 BI	NC_I2C_DFR_SDA	AG49	I2C4_SDA			

1.8V IO

SEP

			SGPIO0		AC3	DBL_CLICK_DET IN 33
			SGPIO1		AC2	NC_DISABLE_STROBE OUT 61
			SI2C0_SCL		Y5	I2C_SEEPROM_SCL OUT 5 67
			SI2C0_SDA		Y4	I2C_SEEPROM_SDA BI 5 67
			SSPI0_MISO		AC5	NC_FTCAM_DISABLE_L OUT 61
			SSPI0_MOSI		AD5	NC_SSPI0_MOSI 73
			SSPI0_SCLK		AD6	NC_DMIC_DISABLE_L OUT 61

SPMI

73	NC_SPMI2_CLK	AK7	AP_SPMI2_SCLK			
73	NC_SPMI2_DATA	AL7	AP_SPMI2_SDATA			

THROTTLE

IPU FOR ALL THROTTLE_TRIGGER

			SOCHOT1		AK52	SOC_SOCHOT_L OUT 7 33 46 67 69
			THROTTLE_TRIGGER0/MTR_ADC_DOUT		AK53	BUCK1_THERMAL_THROTTLE_L IN 33 34
			THROTTLE_TRIGGER1/MTR_ADC_CLKOUT		AL53	BUCK0_THERMAL_THROTTLE_L IN 33 34
			THROTTLE_TRIGGER2/PLL_DIGOBS_0		AJ55	P15V8AON_ILIMIT_L IN 20 34
			THROTTLE_TRIGGER3/PLL_DIGOBS_1		AJ53	P15V8_AON_PRE_UPO_L IN 34
			THROTTLE_TRIGGER4		AJ49	PMU_VDDMAIN_UVWARN_L IN 33 34

PORTABLES SHOULD NC TRIGGER2

1.8V IO

PP1V2_AWAKE_IO (70 12 9 6 5) — R0790 47K 5% 1/20W MF 201 (1) — (2) SOC_SOCHOT_L (69 67 46 33 7)

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UPC_FORCE_PWR will likely be removed in the future

TOUCHID_PWR_EN gets pulled up to S2 on TOUCHID page This is OK because the GPIO is failsafe

PD needed on DFR PAGE

GPIO

38 IN	UPC_I2C_INT_L	AJ51	GPIO[0]	IPU		
	TP_SOC_GPIO01	AA50	GPIO[1]			
73 IN	NC_SPKR_ID0	V53	GPIO[2]	IPU		
73 IN	NC_SPKR_ID1	U53	GPIO[3]	IPU		
73 OUT	NC_SPKRAMP_RESET_L	T53	GPIO[4]			
73 IN	NC_SPKRAMP_INT_L	W53	GPIO[5]	IPU		
67 63 IN	CODEC_INT_L	W50	GPIO[6]	IPU		
67 46 23 OUT	SWD_UPC_SWCLK	U52	GPIO[7]			
73 IN	NC_GPU_CFG_L	AC48	GPIO[8]			
	TP_SOC_GPIO09	R53	GPIO[9]			
67 38 IN	CCG_I2C_INT_L	R52	GPIO[10]			
5 IN	BOARD_REV0	N55	GPIO[11]			
5 IN	BOARD_REV1	AH54	GPIO[12]			
5 IN	BOARD_REV2	Y52	GPIO[13]			
5 IN	BOARD_REV3	AA51	GPIO[14]			
56 IN	DMIC_ID	R54	GPIO[15]			
	TP_SOC_GPIO16	AC50	GPIO[16]			
46 BI	SWD_UPC_SWDIO0	U51	GPIO[17]			
67 23 BI	SWD_UPC_SWDIO1	AK50	GPIO[18]			
73 IN	NC_DFR_TOUCH_INT_L	T52	GPIO[19]			
73 OUT	NC_IPD_SPI_EN	V49	GPIO[20]			
73 IN	NC_TOUCHID_INT	AJ52	GPIO[21]	IPU		
20 OUT	SWD_UPC_SWDIO2	AJ50	GPIO[22]			
67 46 OUT	UPC_FORCE_PWR	AC49	GPIO[23]			
73 OUT	NC_DFR_PWR_EN	R51	GPIO[24]			
73 OUT	NC_SPI_DFR_CS_L	AL49	GPIO[25]			
73 IN	NC_ENET_SYNC_1588	AF49	GPIO[26]			

UART

			UART0_RXD		AB53	UART_DEBUGPRT_D2R IN 46 67 69
			UART0_TXD		AC53	UART_DEBUGPRT_R2D OUT 46 67 69
			UART1_CTSN		AC54	NC_DFR_1V8_TOUCH_RESET_L OUT 73
			UART1_RTSN		AA53	NC_DFR_1V8_DISP_RESET_L OUT 73
			UART1_RXD	IPD	AA54	NC_DFR_1V8_DISP_INT IN 73
			UART1_TXD	IPD	AC55	BT_TIME_SYNC_1V8 IN 51 52 67
			UART2_CTSN	IPU	W55	UART_WLAN_D2R_CTS_L IN 51 67
			UART2_RTSN		Y54	UART_WLAN_R2D_RTS_L OUT 51 67
			UART2_RXD	IPU	Y53	UART_WLAN_D2R IN 51 67
			UART2_TXD		Y55	UART_WLAN_R2D OUT 51 67
			UART3_CTSN		AC51	NC_UART3_D2R_CTS_L 73
			UART3_RTSN		AC52	NC_UART3_R2D_RTS_L 73
			UART3_RXD		AF48	NC_UART3_D2R 73
			UART3_TXD		AB52	NC_UART3_R2D 73
			UART4_CTSN		AJ48	NC_UART4_D2R_CTS_L 73
			UART4_RTSN		AK48	NC_UART4_R2D_RTS_L 73
			UART4_RXD		AL52	NC_UART4_D2R 73
			UART4_TXD		AL50	NC_UART4_R2D 73
			UART6_RXD		AF51	UART_TCON_D2R IN 20
			UART6_TXD		AG50	UART_TCON_R2D OUT 20
			UART7_RXD		AM2	TP_UART7_RXD
			UART7_TXD		AJ2	TP_UART7_TXD

1.8V IO

Use UART2 if your wireless module is 1.2V IO

1.8V IO R2D is for desktop only

BOARD ID

5 IN	BOARD_ID0	W49	BOARD_ID0/SOC_DEBUG1			
5 IN	BOARD_ID1	R55	BOARD_ID1/SOC_DEBUG2			
5 IN	BOARD_ID2	T55	BOARD_ID2/SOC_DEBUG3			
5 IN	BOARD_ID3	V55	BOARD_ID3/SPI0_SSIN			
5 IN	BOARD_ID4	U55	BOARD_ID4			

NAND

			NAND_SYS_CLK0		AG52	NAND0_CLK24M_0_R OUT 20
			NAND_SYS_CLK1		AH53	NAND0_CLK24M_1_R OUT 20
			SSD_BFH		AH51	NAND_BFH OUT 53 54 67
			SSD_RESETN		AG53	NAND0_RESET_L OUT 7 53 54 67

67 54 53 7 NAND0_RESET_L — NOSTUFF R0791 47K 5% 1/20W MF 201 (1) — (2)

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: AP I/Os

Apple Inc.

DRAWING NUMBER 051-05371 SIZE D
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OK2INTEGRATE

SOC: LPDP & MIPI

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LPDP TX

NC_LPDPRX_AUX0	AP7	LPDPRX_AUX_D0_P	
NC_LPDPRX_AUX1	AR7	LPDPRX_AUX_D1_P	
NC_LPDPRX_AUX2	AT7	LPDPRX_AUX_D2_P	
NC_LPDPRX_AUX3	AV7	LPDPRX_AUX_D3_P	
NC_LPDPRX_AUX4	AW7	LPDPRX_AUX_D4_P	
NC_LPDPRX_AUX5	AY7	LPDPRX_AUX_D5_P	
NC_LPDPRX_AUX6	AP8	LPDPRX_AUX_D6_P	
NC_LPDPRX_AUX7	AR8	LPDPRX_AUX_D7_P	
NC_LPDPRX_AUX8	AT8	LPDPRX_AUX_D8_P	
NC_LPDPRX_AUX9	AV8	LPDPRX_AUX_D9_P	
NC_LPDPRX_AUX10	AW8	LPDPRX_AUX_D10_P	
NC_LPDPRX_AUX11	AY8	LPDPRX_AUX_D11_P	

LPDP RX

NC_LPDPRX_RXP<0>	AP1	LPDPRX_RX_D0_P	
NC_LPDPRX_RXN<0>	AP2	LPDPRX_RX_D0_N	
NC_LPDPRX_RXP<1>	AR1	LPDPRX_RX_D1_P	
NC_LPDPRX_RXN<1>	AR2	LPDPRX_RX_D1_N	
NC_LPDPRX_RXP<2>	AT1	LPDPRX_RX_D2_P	
NC_LPDPRX_RXN<2>	AT2	LPDPRX_RX_D2_N	
NC_LPDPRX_RXP<3>	AV1	LPDPRX_RX_D3_P	
NC_LPDPRX_RXN<3>	AV2	LPDPRX_RX_D3_N	
NC_LPDPRX_RXP<4>	AW1	LPDPRX_RX_D4_P	
NC_LPDPRX_RXN<4>	AW2	LPDPRX_RX_D4_N	
NC_LPDPRX_RXP<5>	AY1	LPDPRX_RX_D5_P	
NC_LPDPRX_RXN<5>	AY2	LPDPRX_RX_D5_N	
NC_LPDPRX_RXP<6>	AP4	LPDPRX_RX_D6_P	
NC_LPDPRX_RXN<6>	AP5	LPDPRX_RX_D6_N	
NC_LPDPRX_RXP<7>	AR4	LPDPRX_RX_D7_P	
NC_LPDPRX_RXN<7>	AR5	LPDPRX_RX_D7_N	
NC_LPDPRX_RXP<8>	AT4	LPDPRX_RX_D8_P	
NC_LPDPRX_RXN<8>	AT5	LPDPRX_RX_D8_N	
NC_LPDPRX_RXP<9>	AV4	LPDPRX_RX_D9_P	
NC_LPDPRX_RXN<9>	AV5	LPDPRX_RX_D9_N	
NC_LPDPRX_RXP<10>	AW4	LPDPRX_RX_D10_P	
NC_LPDPRX_RXN<10>	AW5	LPDPRX_RX_D10_N	
NC_LPDPRX_RXP<11>	AY4	LPDPRX_RX_D11_P	
NC_LPDPRX_RXN<11>	AY5	LPDPRX_RX_D11_N	

NO_TEST=1

NC_LPDPRX0_RCAL_POS	AU1	LPDPRX0_RCAL_P
NC_LPDPRX0_RCAL_NEG	AU2	LPDPRX0_RCAL_N
NC_LPDPRX1_RCAL_POS	AU4	LPDPRX1_RCAL_P
NC_LPDPRX1_RCAL_NEG	AU5	LPDPRX1_RCAL_N

NO_TEST=1 NO_TEST=1 NO_TEST=1

LPDP TX

GND_VOID=TRUE

LPDP_TX0P	AR55	LPDP_INT_DATA_C_P<0>	OUT 57
LPDP_TX0N	AR54	LPDP_INT_DATA_C_N<0>	OUT 57
LPDP_TX1P	AT55	LPDP_INT_DATA_C_P<1>	OUT 57
LPDP_TX1N	AT54	LPDP_INT_DATA_C_N<1>	OUT 57
LPDP_TX2P	AU54	LPDP_INT_DATA_C_P<2>	OUT 57
LPDP_TX2N	AU55	LPDP_INT_DATA_C_N<2>	OUT 57
LPDP_TX3P	AV55	LPDP_INT_DATA_C_P<3>	OUT 57
LPDP_TX3N	AV54	LPDP_INT_DATA_C_N<3>	OUT 57
LPDP_TX4P	AW55	NC_LPDP_TX4P	73
LPDP_TX4N	AW54	NC_LPDP_TX4N	73
LPDP_TX5P	AY55	NC_LPDP_TX5P	73
LPDP_TX5N	AY54	NC_LPDP_TX5N	73
LPDP_AUX_P	AU52	LPDP_INT_AUX_C_P	BI 57
LPDP_AUX_N	AU51	LPDP_INT_AUX_C_N	BI 57
LPDP_RCAL_P	AV52	SOC_LPDP_INT_RCAL_POS	8
LPDP_RCAL_N	AV51	SOC_LPDP_INT_RCAL_NEG	8

DISPLAY

IPD

DISP_HPD	AG55	LPDP_INT_HPD	IN 57 67
DISP_POL	AH55	NC_DISPLAY_POL	73
DISP_SPI_MISO/DWI_CLK	AC6	SPI_DISP_BKLT_MISO	IN 59 67
DISP_SPI_MOSI/DWI_DO	AC7	SPI_DISP_BKLT_MOSI_R	OUT 20
DISP_SPI_SCLK/DISP_I2C_SCL	AD7	SPI_DISP_BKLT_CLK_R	OUT 20
DISP_SPI_SSIN/DISP_I2C_SDA	AB6	SPI_DISP_BKLT_CS_L	BI 20
DISP_SPMI_SCLK	W4	NC_DISP_SPMI_CLK	73
DISP_SPMI_SDATA	W3	NC_DISP_SPMI_DATA	73
DISP_FSYNC	T49	NC_DISP_FSYNC	73
DISP_LSYNC	R50	DISP_BKLT_LSYNC	OUT 59
DISP_TOUCH_BSYNC0	T50	NC_DISP_TOUCH_BSYNC0	73
DISP_TOUCH_BSYNC1	R49	NC_DISP_TOUCH_BSYNC1	73
DISP_TOUCH_EB	U49	NC_DISP_TOUCH_EB	73
DFR_BSYNC/DISP_INT	AM5	BKLT_FAULT_INT_L	IN 59
DFR_DISP_TE	AL51	NC_DFR_DISP_TE	IN 73

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ISP I2C

NC_ISP_I2C0_SCL	Y2	ISP_I2C0_SCL/ISP_GPIO_8	38
NC_ISP_I2C0_SDA	Y3	ISP_I2C0_SDA/ISP_GPIO_9	38
NC_ISP_I2C1_SCL	AA5	ISP_I2C1_SCL/ISP_GPIO_10	38
NC_ISP_I2C1_SDA	AA6	ISP_I2C1_SDA/ISP_GPIO_11	38
I2C_CAM_SCL	AA3	ISP_I2C2_SCL	38 OUT
I2C_CAM_SDA	AA2	ISP_I2C2_SDA	38 BI
NC_ISP_I2C3_SCL	AA7	ISP_I2C3_SCL	38
NC_ISP_I2C3_SDA	AB7	ISP_I2C3_SDA	38

ISP GPIO

FTCAM_RESET_L	Y6	ISP_GPIO_0	67 61 OUT
NC_ISP_GPIO1	W6	ISP_GPIO_1	73
NC_ISP_GPIO2	Y7	ISP_GPIO_2	73
NC_ISP_GPIO3	W7	ISP_GPIO_3	73

ISP SPMI

NC_ISP_SPMI0_CLK	AG7	ISP_SPMI0_SCLK/ISP_GPIO_5	73
NC_ISP_SPMI0_DATA	AF7	ISP_SPMI0_SDATA/ISP_GPIO_4	73
NC_ISP_SPMI1_CLK	AG6	ISP_SPMI1_SCLK/ISP_GPIO_7	73
NC_ISP_SPMI1_DATA	AH7	ISP_SPMI1_SDATA/ISP_GPIO_6	73

ISP CLK

NC_SENSOR0_CLK	AD1	SENSOR0_CLK	73
NC_SENSOR1_CLK	AE1	SENSOR1_CLK	73
NC_SENSOR2_CLK	AD3	SENSOR2_CLK	73
NC_SENSOR3_CLK	AF1	SENSOR3_CLK	73

MIPI_C

MIPI0C_DPCLK	L15	NC_MIPI0C_CLKP	73
MIPI0C_DNCLK	L14	NC_MIPI0C_CLKN	73
MIPI0C_DPDATA0	K15	NC_MIPI0C_DATAP<0>	73
MIPI0C_DNDATA0	K14	NC_MIPI0C_DATAN<0>	73
MIPI0C_DPDATA1	M14	NC_MIPI0C_DATAP<1>	73
MIPI0C_DNDATA1	M15	NC_MIPI0C_DATAN<1>	73
MIPI1C_DPCLK	L11	MIPI_FTCAM_CLK_P	IN 57 67
MIPI1C_DNCLK	L12	MIPI_FTCAM_CLK_N	IN 57 67
MIPI1C_DPDATA0	M12	MIPI_FTCAM_DATA_P<0>	IN 57 67
MIPI1C_DNDATA0	M11	MIPI_FTCAM_DATA_N<0>	IN 57 67
MIPI1C_DPDATA1	K11	MIPI_FTCAM_DATA_P<1>	IN 57 67
MIPI1C_DNDATA1	K12	MIPI_FTCAM_DATA_N<1>	IN 57 67
MIPID_DPCLK	K9	NC_MIPI_DFR_CLKP	OUT 73
MIPID_DNCLK	K8	NC_MIPI_DFR_CLKN	OUT 73
MIPID_DPDATA0	L9	NC_MIPI_DFR_DATAP	OUT 73
MIPID_DNDATA0	L8	NC_MIPI_DFR_DATAN	OUT 73
MIPI0C_REXT	K17	SOC_MIPI1C_REXT	8
MIPI1C_REXT	L17	GND	8
MIPID_REXT	M9		

GND_VOID=TRUE

MIPI_D

SOC_MIPI1C_REXT / GND

8 SOC_MIPI1C_REXT
8 GND

PACK_OPTION=NO_DFR
R0800 200 1% 1/20W MF 201
MAKE_BASE=TRUE
PLACE_NEAR=U0600.K17:6MM
PACK_IGNORE=TRUE
PACK_OPTION=DFR

PACK_OPTION=NO_FTCAM
R0820 200 1% 1/20W MF 201
MAKE_BASE=TRUE
PLACE_NEAR=U0600.L17:6MM
PACK_OPTION=FTCAM

SOC_LPDP_INT_RCAL_POS / SOC_LPDP_INT_RCAL_NEG

8 SOC_LPDP_INT_RCAL_POS
8 SOC_LPDP_INT_RCAL_NEG

R0895 200 1% 1/20W MF 201
C0895 10PF 5% 25V C0G 0201

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: LPDP & MIPI

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D
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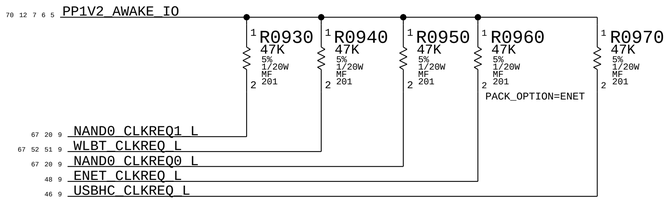
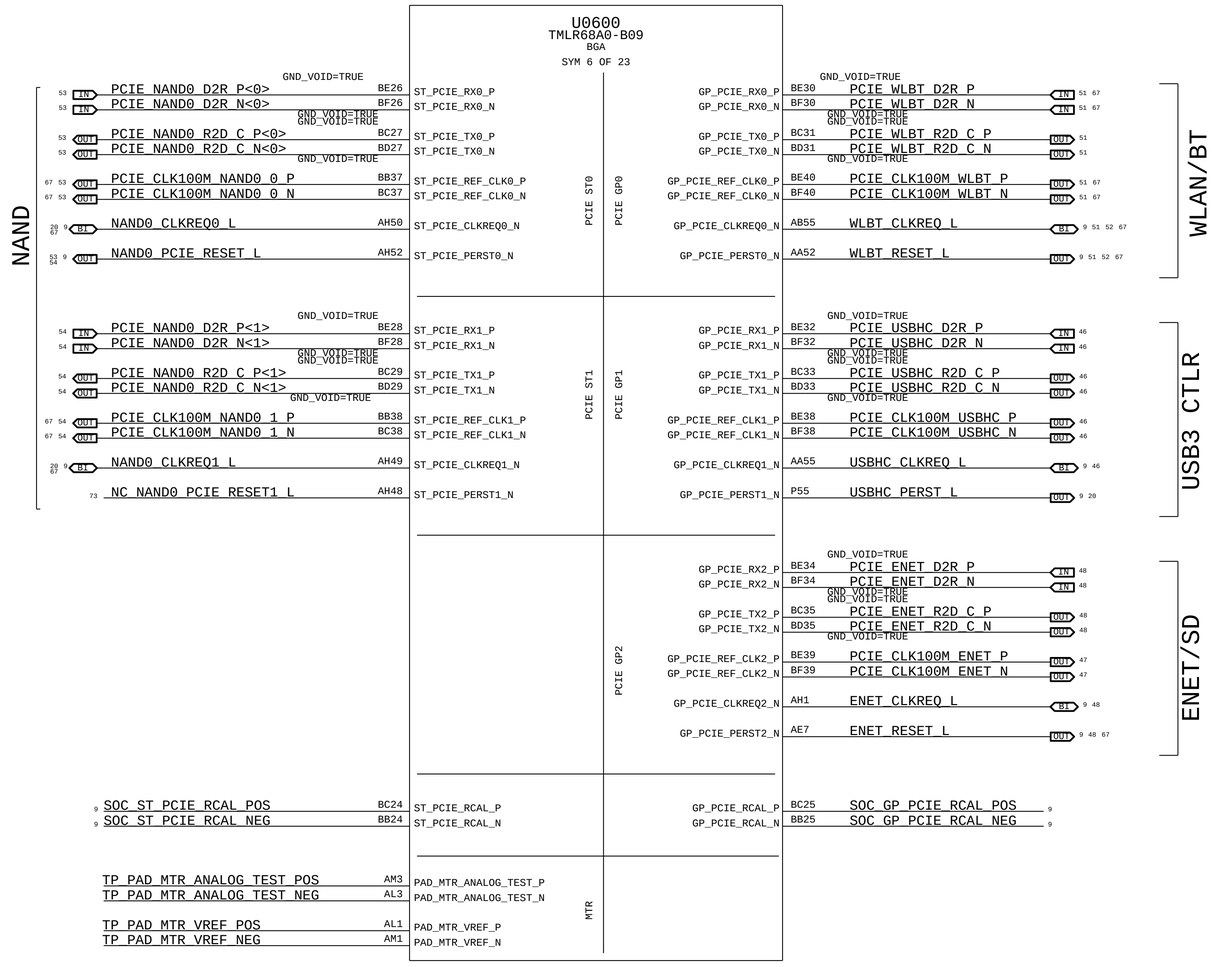
OK2INTEGRATE

SOC: PCIE

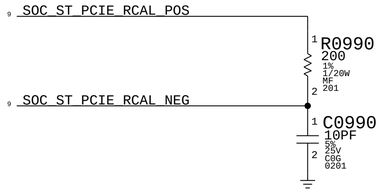
PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
75 NF AND 265 NF FOR GEN1/2 AND BETWEEN
176 NF AND 265 NF FOR GEN 3/4

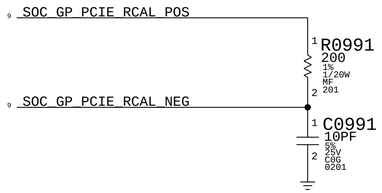
R0970 IS NEEDED DUE TO RDAR://53793006

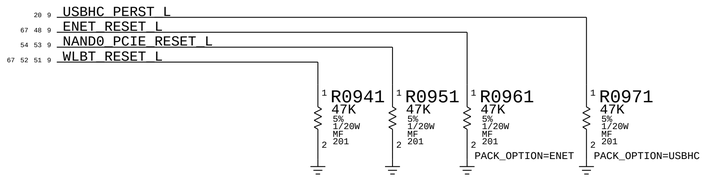




TO BE CHECKED WITH SEG- DO NOT MATCH WITH SILVAL
IS THE PULL-UP VOLTAGE CORRECT?







BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: PCIE

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D
REVISION: 6.0.0
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OK2INTEGRATE

AOP, NUB, and SMC GPIO's are referenced to PP1V25_S2_AOP

SOC: AOP

U0600
TMLR68A0-B09
BGA
SYM 7 OF 23

AOP GPIO

TP_AOP_FUNC0	BB18	AOP_FUNC[0]		
TP_AOP_FUNC1	BC16	AOP_FUNC[1]		
TP_AOP_FUNC2	BC12	AOP_FUNC[2]		
TP_AOP_FUNC3	BC13	AOP_FUNC[3]		
TP_AOP_FUNC4	BA16	AOP_FUNC[4]		
TP_AOP_FUNC5	BA13	AOP_FUNC[5]		
output if gyro, input for radar				
73 OUT NC_SPI_GYRO_CS_L	BA15	AOP_FUNC[6]		
73 IN NC_GYRO_INT	BD13	AOP_FUNC[7]		
73 IN NC_GYRO_MOTION_INT	BD16	AOP_FUNC[8]		
72 IN LID_OPEN MAKE_BASE=TRUE	BA14	AOP_FUNC[9]	IPD	
PACK_OPTION=HAS_LID				
TP_AOP_FUNC10	BB12	AOP_FUNC[10]		
67 52 51 OUT WLAN_CONTEXT_A	BD20	AOP_FUNC[11]		
67 52 51 OUT WLAN_CONTEXT_B	BA11	AOP_FUNC[12]		
38 IN ALS_INT_L	BD18	AOP_FUNC[13]		
TP_AOP_FUNC14	BA10	AOP_FUNC[14]		

AOP I2C

I2C0 is ALS for portables

38 OUT I2C_AOP_CAMALS_SCL	BC20	AOP_I2CM0_SCL	
38 BI I2C_AOP_CAMALS_SDA	BB19	AOP_I2CM0_SDA	
38 OUT NC_I2C_AOP_ENET_SCL	BB16	AOP_I2CM1_SCL	
38 BI NC_I2C_AOP_ENET_SDA	BE15	AOP_I2CM1_SDA	

AOP PDM

73 NC_PDM_CLK1	BB9	AOP_PDM_IN_CLK1/AOP_I2S1_BCLK	
73 NC_PDM_CLK2	BC9	AOP_PDM_IN_CLK2/AOP_I2S0_MCK	
67 61 OUT PDM_DMIC_CLK3	BC6	AOP_PDM_IN_CLK3/AOP_I2S0_LRCK	
67 61 OUT PDM_DMIC_CLK4	BD9	AOP_PDM_IN_CLK4/AOP_I2S0_DOUT	
73 NC_PDM_CLK5	BC8	AOP_PDM_IN_CLK5/AOP_I2S0_DIN	
73 NC_PDM_CLK6	BD8	AOP_PDM_IN_CLK6/AOP_I2S0_BCLK	
73 NC_PDM_DATA1	BE21	AOP_PDM_IN_DATA1/AOP_I2S1_MCK	
73 NC_PDM_DATA2	BE16	AOP_PDM_IN_DATA2/AOP_I2S1_LRCK	
67 61 IPD IN PDM_DMIC_DATA3 CKPLUS_WAIVE=CLK_DATA_CON	BE19	AOP_PDM_IN_DATA3/AOP_I2S1_DOUT/AOP_PDM_IN_CLK7	
67 61 IPD IN PDM_DMIC_DATA4 CKPLUS_WAIVE=CLK_DATA_CON	BD5	AOP_PDM_IN_DATA4/AOP_I2S1_DIN/AOP_PDM_IN_CLK8	

AOP SPI

73 IN NC_AOP_GYRO_MISO	BF15	AOP_SPI0_MISO	
73 OUT NC_AOP_GYRO_MOSI	BF14	AOP_SPI0_MOSI	
73 OUT NC_AOP_GYRO_CLK	BF17	AOP_SPI0_SCLK	

AOP SPMI

73 NC_AOP_SPMI0_SCLK	BF18	AOP_SPMI0_SCLK/AOP_UART0_TXD	
73 NC_AOP_SPMI0_SDATA	BF19	AOP_SPMI0_SDATA/AOP_UART0_RXD	
20 OUT SPMI_SE_CLK_R	BF20	AOP_SPMI1_SCLK/AOP_UART1_TXD	
20 BI SPMI_SE_DATA_R	BF21	AOP_SPMI1_SDATA/AOP_UART1_RXD	

AOP UART

TP_AOP_UART2_D2R	BB3	AOP_UART2_RXD	
TP_AOP_UART2_R2D	BB4	AOP_UART2_TXD	

AOP RESET

PP1V25_S2			
R1083 10K 5% 1/20W MF 201			
33 IN PMU_CLK32K_SOC	BE6	RT_CLK32768	
	BF10	CFSB_AON	
68 67 33 6 IN PMU_RESET_L	BB5	COLD_RESETN	
67 TP_AON_SLEEP1_RESET_L	BB21	AON_SLEEP1_RESETN	
33 OUT SOC_WDOG	BF12	WDOG	

AOP DEBUG

XW1022 SHORT-14L-0.1MM-SM			
PP1V25_S2 SOC_DBG_PROBE_VALID	BF6	DBG_PROBE_VALID	
44 BI EUSB_DBG_P	BF24	DBG_USB_EDP	
44 BI EUSB_DBG_N	BE24	DBG_USB_EDM	
SOC_USBDBG_RESREF	BE23	DBG_USB_RESREF	

R1042 200 1% 1/20W MF 201

NUB GPIO

NUB_CLK_OUT0	BA17	NC_DFR_TOUCH_CLK32K_RESET_L	OUT 73
NUB_DOCK_ATTENTION/CTM_TRIGGER	BC15	TP_SOC_DOCK_ATTENTION	
NUB_DOCK_CONNECT	BC17	SOC_DOCK_CONNECT	IN 10 67 69
NUB_GPIO_0/AOP_FUNC15/NUB_CLK_OUT1	BD14	BL_PWR_ON	OUT 20
NUB_GPIO_1/AOP_PDM_IN_CLK0	BD15	CODEC_RESET_L	OUT 63 65 67
NUB_GPIO_2/AOP_PDM_IN_DATA0	BD21	TP_SOC_SW_DBG	OUT 72
NUB_GPIO_3/AOP_LEAP_MADI_IN	BD17	ENET_LOW_PWR	IN 20
IPU NUB_GPIO_4/AOP_LEAP_MADI_OUT	BB13	TP_SMC_FIXTURE_MODE_L	IN 72
NUB_GPIO_5/AOP_PDM_OUT_CLK0	BD19	NC_CHGR_INT_L_LOM_PMU_RESET_EN	IN 73
NUB_GPIO_6/AOP_PDM_OUT_DATA0/AOP_FUNC16	BD22	CCG_SMC_I2C_INT_L	IN 39 67
NUB_GPIO_7/AOP_FUNC17	BB10	NC_ACDC_ID	IN 73
NUB_GPIO_8/AOP_FUNC18	BD12	NC_ACDC_BURST_EN_L	OUT 73
NUB_GPIO_9/AOP_FUNC19	BD11	NC_SPI_DP2HDMI_HOLD_L	OUT 73
NUB_GPIO_10/AOP_FUNC20	BC10	NC_HDMI_CEC_AOP_TX	OUT 73
NUB_GPIO_11/KIS_GPIO0/AOP_FUNC21	BB7	NC_HDMI_CEC_AOP_RX	IN 73
NUB_GPIO_12/KIS_GPIO1/AOP_FUNC22	BD10	NC_HDMI_HPD_AOP	IN 73

NUB SPMI

NUB_SPMI0_SCLK	BB15	SPMI_NUB_MPMU_CLK_R	OUT 20
NUB_SPMI0_SDATA	BC14	SPMI_NUB_MPMU_DATA_R	BI 20
NUB_SPMI1_SCLK	BA12	SPMI_NUB_SPMU_CLK_R	OUT 20
NUB_SPMI1_SDATA	BC11	SPMI_NUB_SPMU_DATA_R	BI 20

NUB SWD

NUB_SWD_TCK_OUT0	BC18	SWD_NUB_SWCLK	OUT 29 33 67
NUB_SWD_TMS0	BC19	SWD_NUB_PMU_SWDIO	BI 29 33 67
NUB_SWD_TMS1	BC21	TP_NUB_SWD_TMS1	

JTAG

JTAG_SEL	BE4	SOC_JTAG_SEL	IN 5 67
IPU JTAG_TCK	BF5	SWD_SOC_SWCLK	IN 46 67 69
IPU JTAG_TDI	BF16	DEBUG_JTAG_SOC_TDI	20
JTAG_TDO	BC1	DEBUG_JTAG_SOC_TDO	20
IPU JTAG_TMS	BB1	SWD_SOC_SWDIO	BI 46 67 69
IPD JTAG_TRSTN	BF7	TP_JTAG_SOC_TRST_L	67

SMC I2C

SMC_I2CM0_SCL	BC3	I2C_SMC_PWR_FAN1_SCL	OUT 39
SMC_I2CM0_SDA	BC2	I2C_SMC_PWR_FAN1_SDA	BI 39
SMC_I2CM1_SCL/SMC_UART1_TXD	BD4	I2C_SMC_UPC_SCL	OUT 23 39 46 67
SMC_I2CM1_SDA/SMC_UART1_RXD	BB2	I2C_SMC_UPC_SDA	BI 23 39 46 67
SMC_I2CM2_SCL	BD6	I2C_SMC_SNS1_SCL	OUT 39 67
SMC_I2CM2_SDA	BC5	I2C_SMC_SNS1_SDA	BI 39 67
SMC_I2CM3_SCL	BC7	I2C_SMC_IPD_FAN0_SCL	OUT 39
SMC_I2CM3_SDA	BD7	I2C_SMC_IPD_FAN0_SDA	BI 39
SMC_I2CM4_SCL	BE7	I2C_SMC_SNS0_SCL	OUT 39 67
SMC_I2CM4_SDA	BF9	I2C_SMC_SNS0_SDA	BI 39 67

SMC UART

IPU SMC_UART0_RXD	BF4	UART_SMC_DEBUGPRT_D2R	IN 46 67 69
SMC_UART0_TXD	BF8	UART_SMC_DEBUGPRT_R2D	OUT 46 67 69

SMC GPIO

IPU SMC_GPIO0	BF11	UPC_SMC_I2C_INT_L	IN 39
SMC_GPIO1	BF13	TP_SMC_GPIO1	
SMC_FPWM0	BE12	NC_SMC_FAN_PWM	OUT 73
SMC_FPWM1	BE9	NC_SMC_FAN_TACH	IN 73

DOC_ATTENTION should be a TP for non dev programs,

SOC_SW_DBG SHOULD GO TO A LED IF POSSIBLE. NEEDS A TEST POINT AT MINIMUM

FIXTURE_MODE_L should be aliased to a TP for non dev programs, The TP is required

69 67 10 SOC_DOCK_CONNECT

R1066 47K 5% 1/20W MF 201

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: AOP

Apple Inc.

DRAWING NUMBER 051-05371 SIZE D

REVISION 6.0.0

BRANCH

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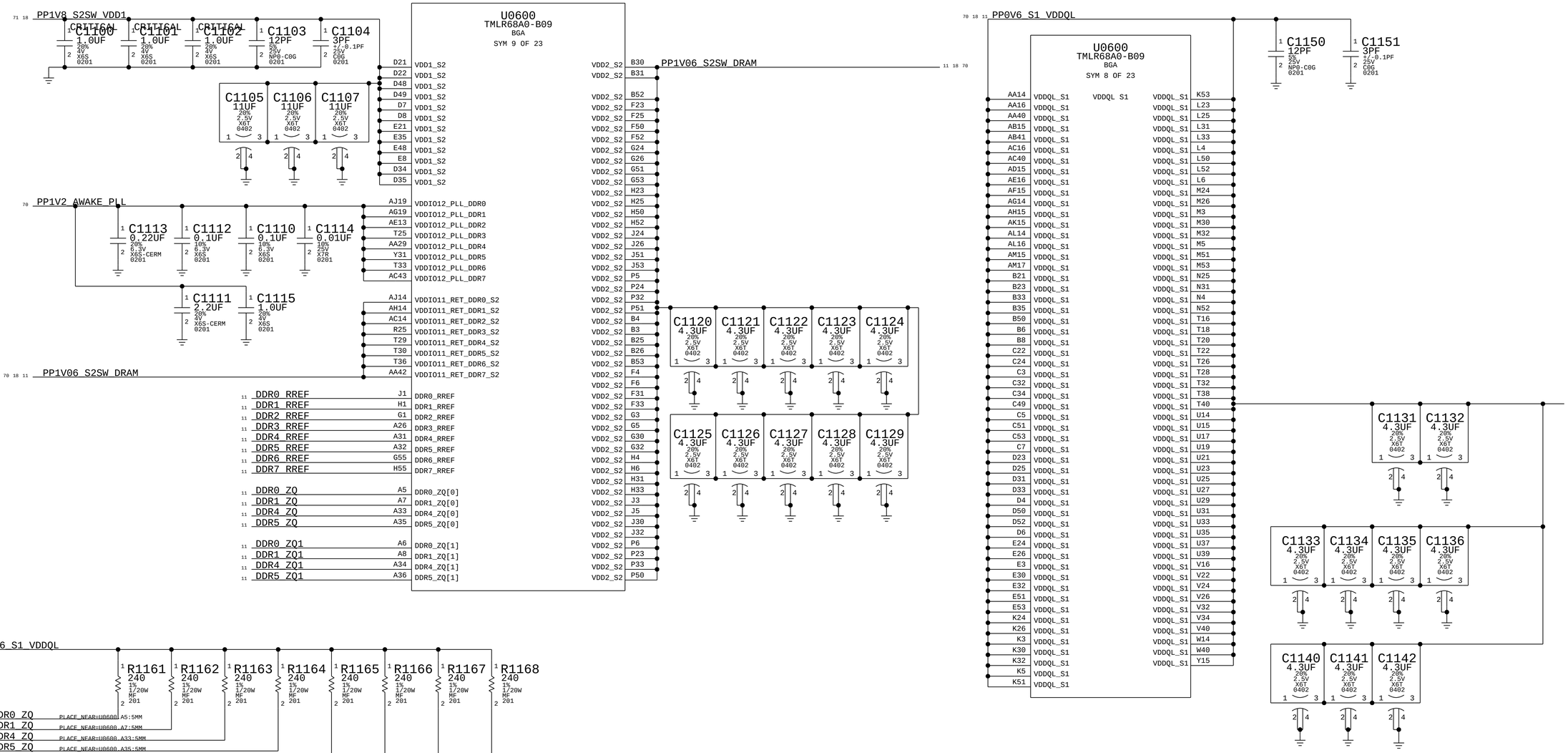
OK2INTEGRATE

SOC: POWER (DDR,SRAM)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00139	138S00138		ALL	4.7UF 20% 4V 0201
138S00164	138S00138		ALL	4.7UF 20% 4V 0201



BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: POWER (DDR,SRAM)

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D

REVISION: 6.0.0

BRANCH:

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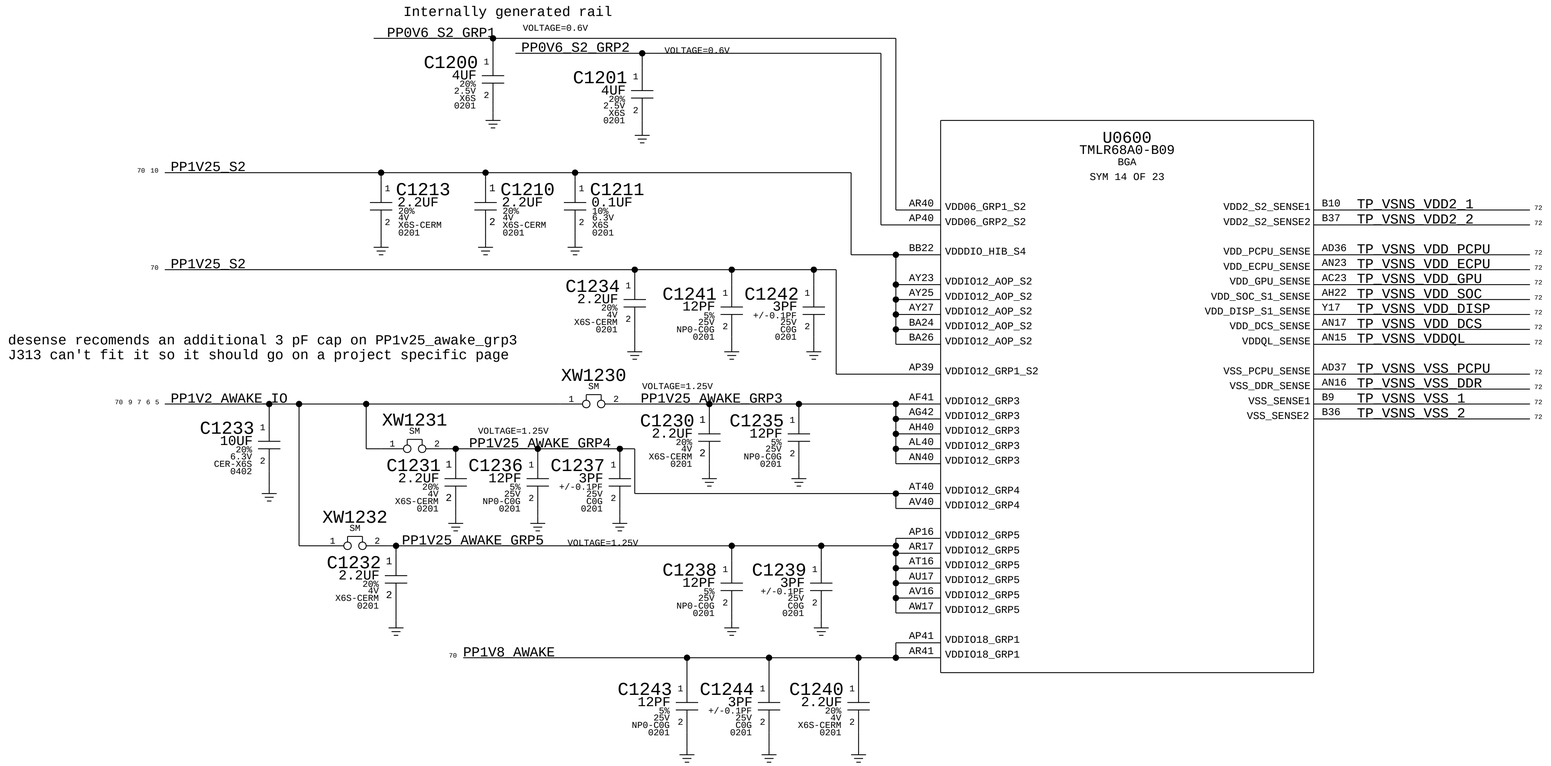
OK2INTEGRATE

SOC: POWER (IO)



BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: POWER (IO)

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D

REVISION: 6.0.0

BRANCH:

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OK2INTEGRATE

SOC: POWER (CPU, GPU)

U0600 TMLR68A0-B09 BGA SYM 11 OF 23

AE33	VDD_PCPU	VDD_PCPU	AP45
AE35	VDD_PCPU	VDD_PCPU	AP46
AE36	VDD_PCPU	VDD_PCPU	AP47
AE37	VDD_PCPU	VDD_PCPU	AP48
AF33	VDD_PCPU	VDD_PCPU	AP49
AF36	VDD_PCPU	VDD_PCPU	AP50
AF39	VDD_PCPU	VDD_PCPU	AP51
AG34	VDD_PCPU	VDD_PCPU	AP52
AG38	VDD_PCPU	VDD_PCPU	AR30
AH34	VDD_PCPU	VDD_PCPU	AR32
AH39	VDD_PCPU	VDD_PCPU	AR33
AJ33	VDD_PCPU	VDD_PCPU	AR35
AJ34	VDD_PCPU	VDD_PCPU	AR36
AK29	VDD_PCPU	VDD_PCPU	AR37
AK33	VDD_PCPU	VDD_PCPU	AR39
AK35	VDD_PCPU		
AK36	VDD_PCPU	VDD_ECPU	AK25
AK38	VDD_PCPU	VDD_ECPU	AL26
AK40	VDD_PCPU	VDD_ECPU	AL28
AK41	VDD_PCPU	VDD_ECPU	AL29
AK42	VDD_PCPU	VDD_ECPU	AN24
AK43	VDD_PCPU	VDD_ECPU	AN29
AK44	VDD_PCPU	VDD_ECPU	AP25
AK45	VDD_PCPU	VDD_ECPU	AR26
AK46	VDD_PCPU	VDD_ECPU	AR28
AL30	VDD_PCPU		
AL32	VDD_PCPU	VDD_SOC_S1	AB23
AL37	VDD_PCPU	VDD_SOC_S1	AC33
AL41	VDD_PCPU	VDD_SOC_S1	AC38
AL42	VDD_PCPU	VDD_SOC_S1	AE23
AL43	VDD_PCPU	VDD_SOC_S1	AE32
AL44	VDD_PCPU	VDD_SOC_S1	AE38
AL45	VDD_PCPU	VDD_SOC_S1	AF28
AL46	VDD_PCPU	VDD_SOC_S1	AG23
AM29	VDD_PCPU	VDD_SOC_S1	AG39
AM34	VDD_PCPU	VDD_SOC_S1	AJ20
AM38	VDD_PCPU	VDD_SOC_S1	AJ22
AM41	VDD_PCPU	VDD_SOC_S1	AJ24
AM42	VDD_PCPU	VDD_SOC_S1	AJ26
AM43	VDD_PCPU	VDD_SOC_S1	AJ28
AM44	VDD_PCPU	VDD_SOC_S1	AJ30
AM45	VDD_PCPU	VDD_SOC_S1	AJ32
AM46	VDD_PCPU	VDD_SOC_S1	AL20
AM47	VDD_PCPU	VDD_SOC_S1	AL22
AM48	VDD_PCPU	VDD_SOC_S1	AL24
AM49	VDD_PCPU	VDD_SOC_S1	AM39
AM50	VDD_PCPU	VDD_SOC_S1	AN18
AM51	VDD_PCPU	VDD_SOC_S1	AN20
AM52	VDD_PCPU	VDD_SOC_S1	AN22
AM53	VDD_PCPU	VDD_SOC_S1	AR18
AM54	VDD_PCPU	VDD_SOC_S1	AR22
AM55	VDD_PCPU	VDD_SOC_S1	AR24
AN33	VDD_PCPU	VDD_SOC_S1	AT33
AN34	VDD_PCPU	VDD_SOC_S1	AT35
AN38	VDD_PCPU	VDD_SOC_S1	AT37
AN42	VDD_PCPU	VDD_SOC_S1	AU18
AN43	VDD_PCPU	VDD_SOC_S1	AU20
AN44	VDD_PCPU	VDD_SOC_S1	AU22
AN45	VDD_PCPU	VDD_SOC_S1	AU24
AN46	VDD_PCPU	VDD_SOC_S1	AU26
AN47	VDD_PCPU	VDD_SOC_S1	AU28
AN48	VDD_PCPU	VDD_SOC_S1	AU30
AN49	VDD_PCPU	VDD_SOC_S1	AU38
AN50	VDD_PCPU	VDD_SOC_S1	Y21
AN51	VDD_PCPU	VDD_SOC_S1	Y26
AN52	VDD_PCPU	VDD_SOC_S1	Y36
AN53	VDD_PCPU		
AN54	VDD_PCPU		
AN55	VDD_PCPU		
AP29	VDD_PCPU		
AP33	VDD_PCPU		
AP38	VDD_PCPU		
AP43	VDD_PCPU		
AP44	VDD_PCPU		

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AA24	VDD_GPU	VDD_GPU	AE26
AA26	VDD_GPU	VDD_GPU	AE27
AA28	VDD_GPU	VDD_GPU	AE29
AA31	VDD_GPU	VDD_GPU	AE30
AA33	VDD_GPU	VDD_GPU	AE31
AA35	VDD_GPU	VDD_GPU	AE42
AA37	VDD_GPU	VDD_GPU	AE43
AB25	VDD_GPU	VDD_GPU	AE44
AB27	VDD_GPU	VDD_GPU	AE45
AB28	VDD_GPU	VDD_GPU	AE46
AB30	VDD_GPU	VDD_GPU	AE47
AB32	VDD_GPU	VDD_GPU	AE48
AB34	VDD_GPU	VDD_GPU	AE49
AB36	VDD_GPU	VDD_GPU	AE50
AC24	VDD_GPU	VDD_GPU	AE51
AC26	VDD_GPU	VDD_GPU	AE52
AC31	VDD_GPU	VDD_GPU	AE53
AC35	VDD_GPU	VDD_GPU	AE54
AC37	VDD_GPU	VDD_GPU	AE55
AD25	VDD_GPU	VDD_GPU	AF24
AD27	VDD_GPU	VDD_GPU	AF32
AD32	VDD_GPU	VDD_GPU	AG25
AD34	VDD_GPU	VDD_GPU	AG27
AD41	VDD_GPU	VDD_GPU	AG31
AD42	VDD_GPU	VDD_GPU	AG33
AD43	VDD_GPU		
AD44	VDD_GPU	VDD_DISP_S1	AA19
AD45	VDD_GPU	VDD_DISP_S1	AA21
AD46	VDD_GPU	VDD_DISP_S1	AA23
AD47	VDD_GPU	VDD_DISP_S1	AB22
AD48	VDD_GPU	VDD_DISP_S1	AC19
AD49	VDD_GPU	VDD_DISP_S1	AD22
AD50	VDD_GPU	VDD_DISP_S1	AE19
AD51	VDD_GPU	VDD_DISP_S1	AE21
AD52	VDD_GPU	VDD_DISP_S1	AG21
AD53	VDD_GPU		
AD54	VDD_GPU		
AD55	VDD_GPU		
AE24	VDD_GPU		

PPVDD_PCPU_AWAKE (70 18 13)

C1300 3PF +/-0.1PF 25V C0G 0201 — C1301 12PF 5% 25V NP0-C0G 0201

PPVDD_PCPU_AWAKE → 13 18 70

PPVDD_GPU_AWAKE (70 18 13) — 0.575V @ 4400MA

C1340 12PF 5% 25V NP0-C0G 0201 — C1341 3PF +/-0.1PF 25V C0G 0201

PPVDD_GPU_AWAKE → 13 18 70

C1353 C1354 C1355 C1356 C1357 11UF 20% 2.5V X6T 0402

PPVDD_ECPU_AWAKE → 18 70

C1320 C1321 C1322 C1323 C1324 C1325 11UF 20% 2.5V X6T 0402

PPVDD_DISP_S1 → 18 70

C1370 12PF 5% 25V NP0-C0G 0201

C1361 C1362 C1363 C1364 11UF 20% 2.5V X6T 0402

C1365 C1366 11UF 20% 2.5V X6T 0402

PPVDD_SOC_S1 → 34 70

C1330 C1331 C1332 C1333 11UF 20% 2.5V X6T 0402

C1334 C1335 C1336 C1337 11UF 20% 2.5V X6T 0402

C1350 C1351 C1352 11UF 20% 2.5V X6T 0402

C1310 C1311 C1312 C1313 C1314 C1315 C1316 C1317 11UF 20% 2.5V X6T 0402

C1318 C1319 11UF 20% 2.5V X6T 0402

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: POWER (SOC, CPU, GPU)

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D

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OK2INTEGRATE

SOC: POWER (SRAM, SOC)

PPVDD_CPU_SRAM_AWAKE

C1400 11UF 20% 2.5V X6T 0402
C1401 11UF 20% 2.5V X6T 0402
C1402 11UF 20% 2.5V X6T 0402
C1403 11UF 20% 2.5V X6T 0402
C1404 11UF 20% 2.5V X6T 0402
C1405 11UF 20% 2.5V X6T 0402
C1406 12PF 5% 25V NP0-C0G 0201
C1407 3PF +/-0.1PF 25V C0G 0201

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VDD_CPU_SRAM: AE34, AE39, AG36, AH35, AH37, AJ36, AJ38, AK27, AK31, AK37, AL33, AL35, AL38, AM25, AM26, AM31, AM36, AN26, AN27, AN30, AN32, AN35, AN37, AP27, AP36, AR31, AR34, AR38

VDD_SRAM_S1: AA18, AA32, AB20, AB24, AB31, AB35, AC21, AC28, AC30, AD20, AD21, AD24, AD28, AD30, AD35, AF20, AF22, AF26, AF30, AG28, AH19, AH21, AH23, AH25, AH27, AH29, AH31, AK19, AK21, AK23, AM19, AM21, AM23, AP21, AP23, AT19, AT21, AT23, AT25, AT27, AT29, AT31, AT39, AU36, AV37

PP0V76_S1_SRAM

C1420 11UF 20% 2.5V X6T 0402
C1421 11UF 20% 2.5V X6T 0402
C1422 11UF 20% 2.5V X6T 0402
C1423 11UF 20% 2.5V X6T 0402
C1424 11UF 20% 2.5V X6T 0402
C1425 11UF 20% 2.5V X6T 0402

PPVDD_DCS_S1

C1410 11UF 20% 2.5V X6T 0402
C1411 11UF 20% 2.5V X6T 0402
C1412 11UF 20% 2.5V X6T 0402
C1413 11UF 20% 2.5V X6T 0402

VDD_DCS_S1: AA39, AB17, AB38, AC18, AC39, AD17, AE18, AF17, AG18, AJ18, AK17, AL18, W17, W22, W24, W26, W31, W33, W35, W39, Y18, Y20, Y23, Y25, Y27, Y29, Y32, Y34, Y38

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: POWER (SRAM)

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D
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OK2INTEGRATE

LPDP_RX Power may be grounded,
Wait until Dev Bringup is complete before grounding it.
Until then connect it to PP1V2_AWAKE

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BGA
SYM 13 OF 23

PP0V805_S1_VDD_FIXED
PP0V72_S2_VDD_LOW
PP0V805_S1_SOC_VDDFIXEDPCIE_R
PP0V805_S1_SOC_VDDFIXEDPLL_F
PP0V805_S1_SOC_VDDFIXEDXTAL_R
PP0V72_S2_VDD_LOWFLPLL_R
PP0V72_S2_VDD_LOWULPLL_R
PP0V855_S2SW_CIO
PP1V2_S2_CIO
PP1V25_S2
PP1V2_AWAKE_IO
PP1V2_AWAKE_PLL
PP1V2_AWAKE_PLL_PCIE_R
PP1V25_S2_ULPPLL_R
PP1V25_AWAKE_XTAL_F
PP1V25_AWAKE_FMON_R

FL1510 120OHM-25%-0.25A-0.5OHM
FL1580 240-OHM-0.2A-0.9-OHM

BOM_COST_GROUP=SOC

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OK2INTEGRATE

SOC: GND (1)

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A10	VSS	VSS	AB42
A11	VSS		AB44
A12	VSS		AB45
A13	VSS		AB46
A14	VSS		AB47
A15	VSS		AB48
A16	VSS		AB5
A17	VSS		AB51
A18	VSS		AB54
A19	VSS		AB8
A2	VSS		AB9
A20	VSS		AC10
A21	VSS		AC11
A22	VSS		AC12
A23	VSS		AC15
A24	VSS		AC17
A25	VSS		AC20
A27	VSS		AC22
A28	VSS		AC25
A29	VSS		AC27
A3	VSS		AC29
A30	VSS		AC32
A37	VSS		AC34
A38	VSS		AC36
A39	VSS		AC41
A4	VSS		AC44
A40	VSS		AC45
A41	VSS		AC46
A42	VSS		AC47
A43	VSS		AC8
A44	VSS		AC9
A45	VSS		AD10
A46	VSS		AD11
A47	VSS		AD12
A48	VSS		AD13
A49	VSS		AD14
A50	VSS		AD16
A51	VSS		AD18
A52	VSS		AD19
A53	VSS		AD23
A54	VSS		AD26
A9	VSS		AD29
AA10	VSS		AD31
AA11	VSS		AD33
AA12	VSS		AD38
AA13	VSS		AD39
AA15	VSS		AD8
AA17	VSS		AD9
AA20	VSS		AE10
AA22	VSS		AE11
AA25	VSS		AE12
AA27	VSS		AE14
AA30	VSS		AE15
AA34	VSS		AE17
AA36	VSS		AE2
AA38	VSS		AE20
AA41	VSS		AE22
AA43	VSS		AE25
AA44	VSS		AE28
AA45	VSS		AE41
AA46	VSS		AE5
AA47	VSS		AE8
AA8	VSS		AE9
AA9	VSS		AF10
AB10	VSS		AF11
AB11	VSS		AF12
AB12	VSS		AF13
AB13	VSS		AF14
AB14	VSS		AF16
AB16	VSS		AF18
AB18	VSS		AF19
AB19	VSS		AF21
AB2	VSS		AF23
AB21	VSS		AF25
AB26	VSS		AF27
AB29	VSS		AF31
AB33	VSS		AF34
AB37	VSS		AF35
AB39	VSS		AF37
AB40	VSS		AF38

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AF40	VSS	VSS	AK12
AF42	VSS		AK13
AF43	VSS		AK14
AF44	VSS		AK16
AF45	VSS		AK18
AF46	VSS		AK20
AF47	VSS		AK22
AF8	VSS		AK24
AF9	VSS		AK26
AG10	VSS		AK28
AG11	VSS		AK30
AG12	VSS		AK39
AG15	VSS		AK47
AG20	VSS		AK49
AG22	VSS		AK51
AG24	VSS		AK54
AG26	VSS		AK8
AG30	VSS		AK9
AG32	VSS		AL10
AG35	VSS		AL11
AG37	VSS		AL12
AG41	VSS		AL13
AG43	VSS		AL15
AG44	VSS		AL17
AG45	VSS		AL19
AG46	VSS		AL2
AG47	VSS		AL21
AG48	VSS		AL23
AG51	VSS		AL25
AG54	VSS		AL27
AG8	VSS		AL31
AG9	VSS		AL36
AH10	VSS		AL39
AH11	VSS		AL47
AH12	VSS		AL5
AH18	VSS		AL55
AH2	VSS		AL8
AH20	VSS		AL9
AH24	VSS		AM10
AH26	VSS		AM11
AH28	VSS		AM12
AH30	VSS		AM13
AH33	VSS		AM14
AH36	VSS		AM16
AH38	VSS		AM18
AH41	VSS		AM20
AH42	VSS		AM22
AH43	VSS		AM24
AH44	VSS		AM27
AH45	VSS		AM30
AH46	VSS		AM32
AH47	VSS		AM33
AH5	VSS		AM35
AH8	VSS		AM37
AH9	VSS		AM40
AJ10	VSS		AM6
AJ11	VSS		AM7
AJ12	VSS		AM8
AJ13	VSS		AM9
AJ15	VSS		AN1
AJ21	VSS		AN10
AJ23	VSS		AN11
AJ25	VSS		AN12
AJ27	VSS		AN13
AJ29	VSS		AN14
AJ31	VSS		AN19
AJ35	VSS		AN2
AJ37	VSS		AN21
AJ40	VSS		AN25
AJ41	VSS		AN28
AJ42	VSS		AN3
AJ43	VSS		AN31
AJ44	VSS		AN36
AJ45	VSS		AN39
AJ46	VSS		AN4
AJ47	VSS		AN41
AJ8	VSS		AN5
AJ9	VSS		AN6
AK10	VSS		AN7
AK11	VSS		AN8

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AN9	VSS	VSS	AT52
AP10	VSS		AT53
AP11	VSS		AT6
AP12	VSS		AT9
AP13	VSS		AU10
AP14	VSS		AU11
AP15	VSS		AU12
AP18	VSS		AU13
AP20	VSS		AU14
AP22	VSS		AU15
AP24	VSS		AU16
AP26	VSS		AU21
AP28	VSS		AU23
AP3	VSS		AU25
AP30	VSS		AU27
AP32	VSS		AU29
AP34	VSS		AU3
AP35	VSS		AU31
AP37	VSS		AU33
AP42	VSS		AU37
AP53	VSS		AU39
AP54	VSS		AU41
AP55	VSS		AU44
AP6	VSS		AU45
AP9	VSS		AU46
AR10	VSS		AU47
AR11	VSS		AU48
AR12	VSS		AU49
AR13	VSS		AU50
AR14	VSS		AU53
AR15	VSS		AU6
AR16	VSS		AU7
AR19	VSS		AU8
AR21	VSS		AU9
AR23	VSS		AV10
AR25	VSS		AV12
AR27	VSS		AV13
AR29	VSS		AV14
AR3	VSS		AV15
AR42	VSS		AV17
AR43	VSS		AV18
AR44	VSS		AV19
AR45	VSS		AV21
AR46	VSS		AV22
AR47	VSS		AV24
AR48	VSS		AV26
AR49	VSS		AV28
AR50	VSS		AV3
AR51	VSS		AV35
AR52	VSS		AV38
AR53	VSS		AV41
AR6	VSS		AV44
AR9	VSS		AV45
AT10	VSS		AV46
AT11	VSS		AV47
AT12	VSS		AV48
AT13	VSS		AV49
AT14	VSS		AV50
AT15	VSS		AV53
AT17	VSS		AV6
AT18	VSS		AV9
AT22	VSS		AW10
AT24	VSS		AW12
AT26	VSS		AW14
AT28	VSS		AW15
AT3	VSS		AW16
AT30	VSS		AW25
AT34	VSS		AW27
AT36	VSS		AW29
AT38	VSS		AW3
AT41	VSS		AW30
AT43	VSS		AW31
AT44	VSS		AW32
AT45	VSS		AW34
AT46	VSS		AW36
AT47	VSS		AW40
AT48	VSS		AW41
AT49	VSS		AW42
AT50	VSS		AW43
AT51	VSS		AW44

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AW45	VSS	VSS	BA28
AW46	VSS		BA29
AW47	VSS		BA3
AW48	VSS		BA30
AW49	VSS		BA31
AW50	VSS		BA34
AW51	VSS		BA36
AW52	VSS		BA4
AW53	VSS		BA40
AW6	VSS		BA41
AW9	VSS		BA44
AY10	VSS		BA45
AY11	VSS		BA46
AY12	VSS		BA47
AY14	VSS		BA48
AY17	VSS		BA49
AY22	VSS		BA5
AY24	VSS		BA50
AY3	VSS		BA53
AY33	VSS		BA54
AY35	VSS		BA55
AY37	VSS		BA6
AY38	VSS		BA7
AY39	VSS		BA8
AY40	VSS		BA9
AY41	VSS		BB11
AY42	VSS		BB14
AY44	VSS		BB17
AY45	VSS		BB20
AY46	VSS		BB23
AY47	VSS		BB26
AY48	VSS		BB27
AY49	VSS		BB28
AY50	VSS		BB29
AY53	VSS		BB30
AY6	VSS		BB31
AY9	VSS		BB32
B1	VSS		BB33
B11	VSS		BB34
B12	VSS		BB35
B13	VSS		BB36
B14	VSS		BB39
B15	VSS		BB40
B16	VSS		BB41
B17	VSS		BB42
B18	VSS		BB43
B19	VSS		BB44
B2	VSS		BB45
B20	VSS		BB46
B22	VSS		BB47
B24	VSS		BB48
B27	VSS		BB49
B28	VSS		BB50
B29	VSS		BB51
B32	VSS		BB52
B34	VSS		BB6
B38	VSS		BB8
B39	VSS		BC22
B40	VSS		BC23
B41	VSS		BC26
B42	VSS		BC28
B43	VSS		BC30
B44	VSS		BC32
B45	VSS		BC34
B46	VSS		BC36
B47	VSS		BC39
B49	VSS		BC4
B5	VSS		BC40
B51	VSS		BC41
B54	VSS		BC42
B55	VSS		BC44
B7	VSS		BC46
BA1	VSS		BC48
BA18	VSS		BC50
BA19	VSS		BC51
BA2	VSS		BC52
BA20	VSS		BD1
BA21	VSS		BD2
BA25	VSS		BD23
BA27	VSS		BD24

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BD25	VSS	VSS	C21
BD26	VSS		C23
BD28	VSS		C25
BD30	VSS		C26
BD32	VSS		C27
BD34	VSS		C28
BD36	VSS		C29
BD37	VSS		C30
BD38	VSS		C31
BD39	VSS		C33
BD40	VSS		C35
BD41	VSS		C36
BD42	VSS		C37
BD44	VSS		C38
BD46	VSS		C39
BD48	VSS		C4
BD50	VSS		C40
BD51	VSS		C41
BD52	VSS		C42
BD53	VSS		C43
BD54	VSS		C44
BD55	VSS		C45
BE1	VSS		C46
BE11	VSS		C47
BE14	VSS		C48
BE17	VSS		C50
BE2	VSS		C52
BE20	VSS		C54
BE22	VSS		C55
BE25	VSS		C6
BE27	VSS		C8
BE29	VSS		C9
BE3	VSS		D1
BE31	VSS		D10
BE33	VSS		D11
BE35	VSS		D12
BE37	VSS		D13
BE41	VSS		D14
BE43	VSS		D15
BE45	VSS		D16
BE47	VSS		D17
BE49	VSS		D18
BE5	VSS		D19
BE51	VSS		D2
BE53	VSS		D20
BE54	VSS		D24
BE55	VSS		D26
BE8	VSS		D27
BF2	VSS		D28
BF22	VSS		D29
BF23	VSS		D3
BF25	VSS		D30
BF27	VSS		D32
BF29	VSS		D36
BF3	VSS		D37
BF31	VSS		D38
BF33	VSS		D39
BF35	VSS		D40
BF37	VSS		D41
BF41	VSS		D42
BF43	VSS		D43
BF45	VSS		D44
BF47	VSS		D45
BF49	VSS		D46
BF51	VSS		D47
BF53	VSS		D5
BF54	VSS		D51
C1	VSS		D53
C10	VSS		D54
C11	VSS		D55
C12	VSS		D9
C13	VSS		E1
C14	VSS		E10
C15	VSS		E11
C16	VSS		E12
C17	VSS		E13
C18	VSS		E14
C19	VSS		E15
C2	VSS		E16
C20	VSS		E17

BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE

SOC: GND

Apple Inc.

DRAWING NUMBER 051-05371 SIZE D

REVISION 6.0.0

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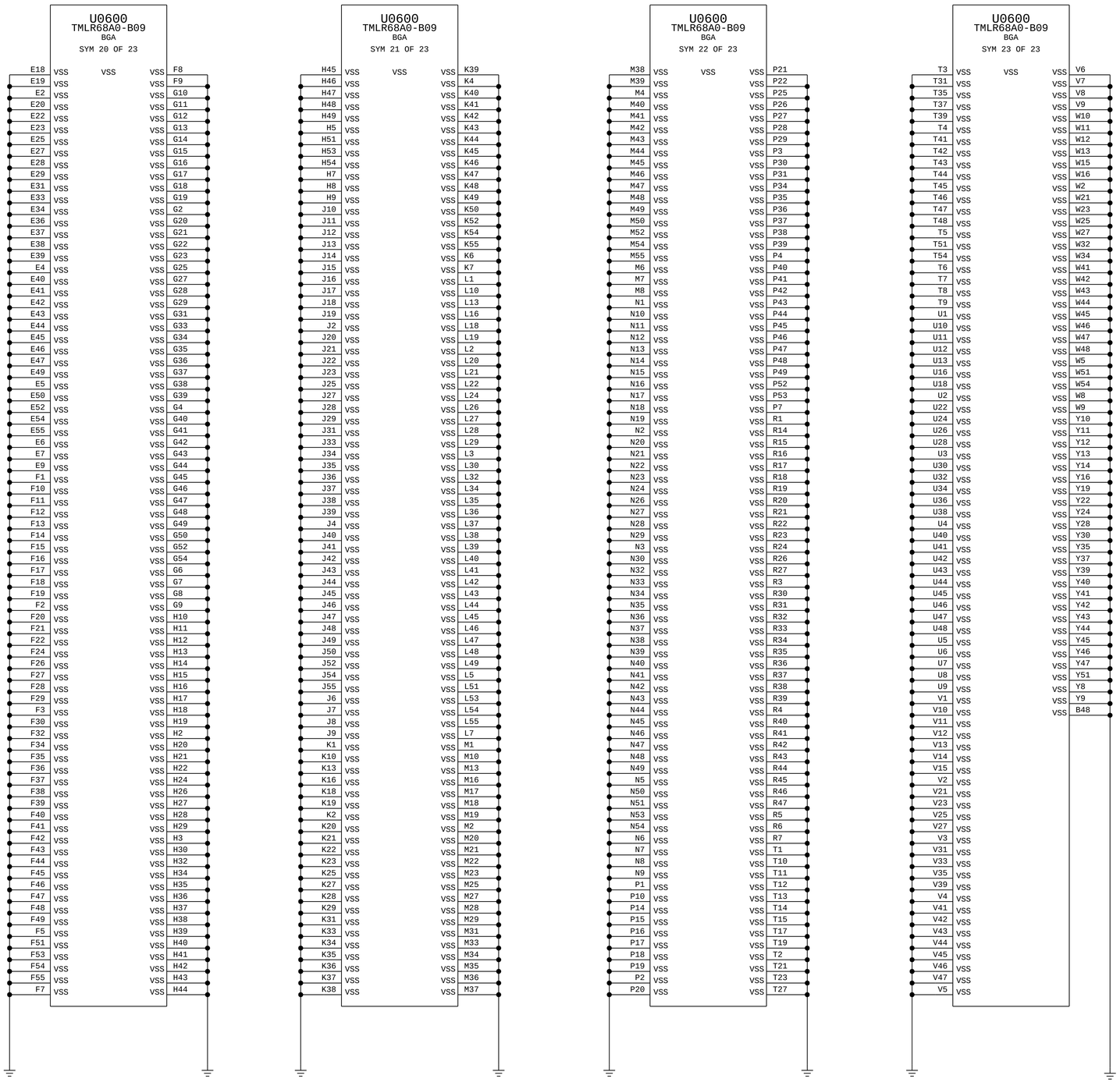
OK2INTEGRATE

SOC: GND (2)



BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SOC: GND-2

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D

REVISION: 6.0.0

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71 11 PP1V8_S2SW_VDD1

C1800	C1801	C1802	C1803	C1804	C1805	
12PF	3PF	12PF	3PF	12PF	3.0PF	
5%	+/-0.1PF	5%	+/-0.1PF	5%	+/-0.1PF	
25V	25V	25V	25V	25V	25V	
NP0-C0G	C0G	NP0-C0G	C0G	NP0-C0G	C0G	
0201	0201	0201	0201	0201	0201	
				PACK_IGNORE=TRUE PACK_OPTION=REMOVE		PACK_IGNORE=TRUE PACK_OPTION=REMOVE

70 11 PP1V06_S2SW_DRAM

C1810	C1811	C1812	C1813	C1814	C1815
12PF	3PF	12PF	3PF	12PF	3PF
5%	+/-0.1PF	5%	+/-0.1PF	5%	+/-0.1PF
25V	25V	25V	25V	25V	25V
NP0-C0G	C0G	NP0-C0G	C0G	NP0-C0G	C0G
0201	0201	0201	0201	0201	0201

70 11 PP0V6_S1_VDDQL

C1820	C1821	C1822	C1823	C1824	C1825
12PF	3PF	12PF	3PF	12PF	3PF
5%	+/-0.1PF	5%	+/-0.1PF	5%	+/-0.1PF
25V	25V	25V	25V	25V	25V
NP0-C0G	C0G	NP0-C0G	C0G	NP0-C0G	C0G
0201	0201	0201	0201	0201	0201

70 13 PPVDD_PCPU_AWAKE

C1830	C1831	C1832	C1833	C1834	C1835	
12PF	3PF	12PF	3PF	12PF	3.0PF	
5%	+/-0.1PF	5%	+/-0.1PF	5%	+/-0.1PF	
25V	25V	25V	25V	25V	25V	
NP0-C0G	C0G	NP0-C0G	C0G	NP0-C0G	C0G	
0201	0201	0201	0201	0201	0201	
						PACK_IGNORE=TRUE PACK_OPTION=REMOVE

70 13 PPVDD_GPU_AWAKE

C1840	C1841	C1842	C1843	C1844	C1845
12PF	3PF	12PF	3PF	12PF	3PF
5%	+/-0.1PF	5%	+/-0.1PF	5%	+/-0.1PF
25V	25V	25V	25V	25V	25V
NP0-C0G	C0G	NP0-C0G	C0G	NP0-C0G	C0G
0201	0201	0201	0201	0201	0201

70 14 PPVDD_CPU_SRAM_AWAKE

C1850	C1851	C1852	C1853
12PF	3PF	12PF	3PF
5%	+/-0.1PF	5%	+/-0.1PF
25V	25V	25V	25V
NP0-C0G	C0G	NP0-C0G	C0G
0201	0201	0201	0201

70 14 PPVDD_DCS_S1

C1854	C1855	C1856	C1857
12PF	3PF	12PF	3PF
5%	+/-0.1PF	5%	+/-0.1PF
25V	25V	25V	25V
NP0-C0G	C0G	NP0-C0G	C0G
0201	0201	0201	0201

70 14 PP0V76_S1_SRAM

C1860	C1861	C1862	C1863
12PF	3PF	12PF	3PF
5%	+/-0.1PF	5%	+/-0.1PF
25V	25V	25V	25V
NP0-C0G	C0G	NP0-C0G	C0G
0201	0201	0201	0201

70 15 PP0V805_S1_VDD_FIXED

C1864	C1865
12PF	3PF
5%	+/-0.1PF
25V	25V
NP0-C0G	C0G
0201	0201

70 15 PP0V805_S1_VDD_FIXED

C1866	C1867
12PF	3PF
5%	+/-0.1PF
25V	25V
NP0-C0G	C0G
0201	0201

70 15 PP0V72_S2_VDD_LOW

C1870	C1871	
12PF	3.0PF	
5%	+/-0.1PF	
25V	25V	
NP0-C0G	C0G	
0201	0201	
PACK_IGNORE=TRUE PACK_OPTION=REMOVE		PACK_IGNORE=TRUE PACK_OPTION=REMOVE

70 13 PPVDD_ECPU_AWAKE

C1872	C1873
12PF	3PF
5%	+/-0.1PF
25V	25V
NP0-C0G	C0G
0201	0201

70 13 PPVDD_DISP_S1

C1874
3PF
+/-0.1PF
25V
C0G
0201

BOM_COST_GROUP=DESENSE

SYNC_MASTER=aaron SYNC_DATE=05/04/2020

PAGE TITLE

SOC: DESENSE CAPS

Apple Inc.

DRAWING NUMBER 051-05371 SIZE D

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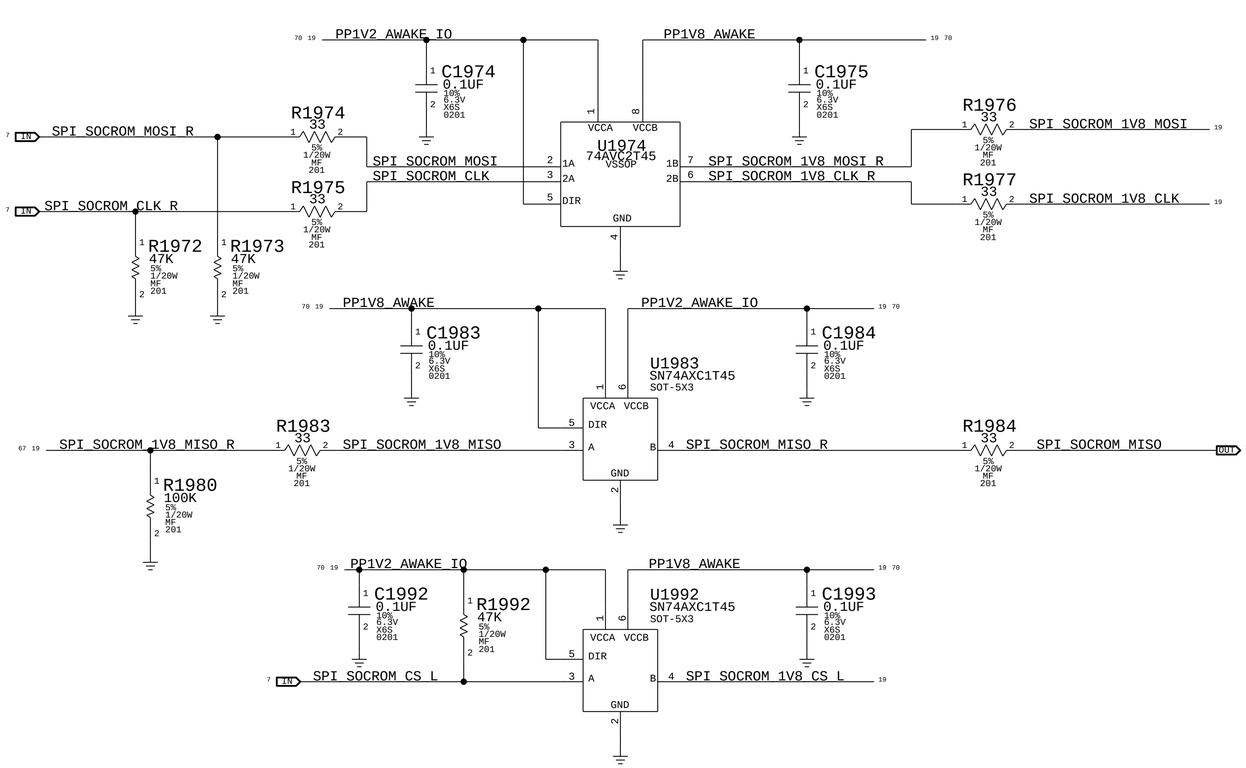
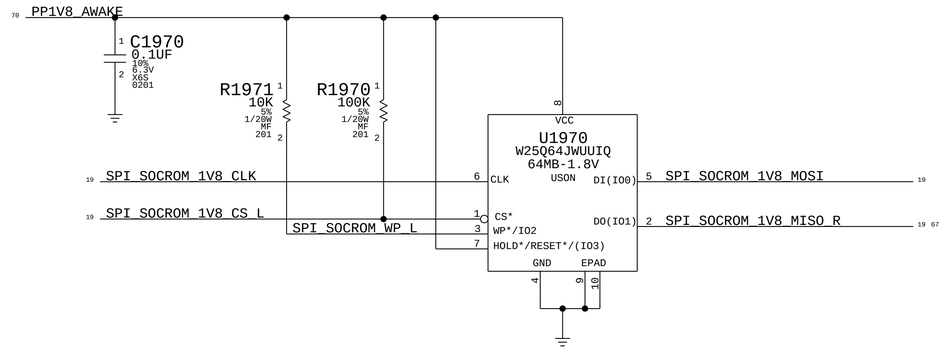
OK2INTEGRATE

SPI NOR (1.8V 64 M-BIT)





BOM_COST_GROUP=SOC

SYNC_MASTER=aaron SYNC_DATE=09/11/2020

PAGE TITLE: SPI NOR

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D

REVISION: 6.0.0

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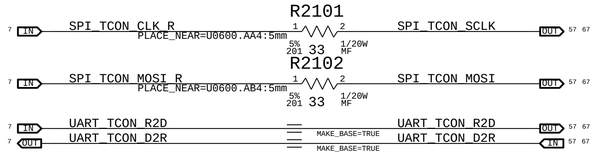
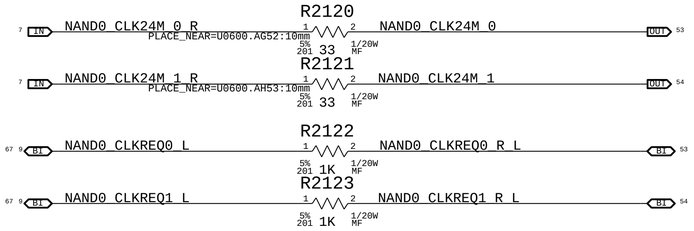
Display SIGNALS

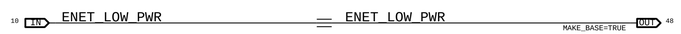


Backlight SIGNALS

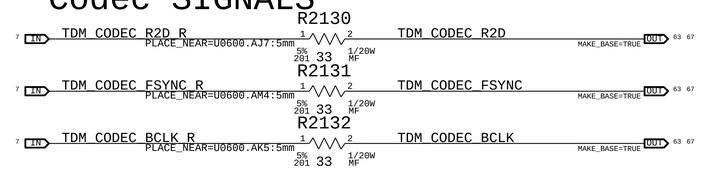
NAND SIGNALS



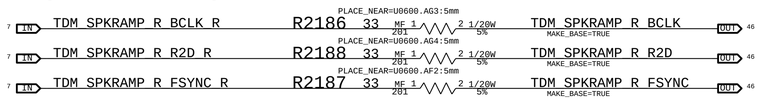
Ethernet SIGNALS



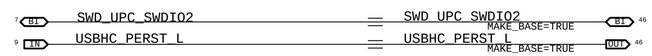
Codec SIGNALS



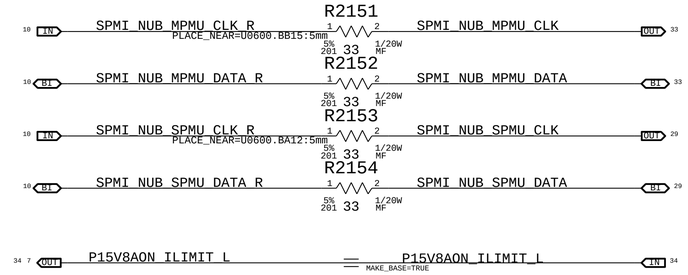
SpeakerAmp SIGNALS

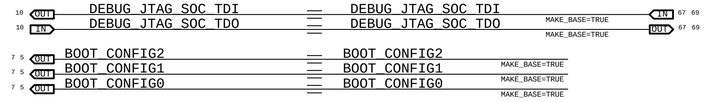


USB-C Ace2 SIGNALS

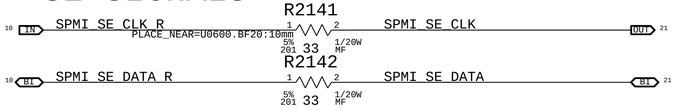


PMU SIGNALS





SE SIGNALS



BOM_COST_GROUP=SOC

PAGE TITLE: SoC Project Support

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D

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Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***

Per TGA Power Block Diagram v0.3

PP1V8_S2 (70) — IccMax SE only: 125mA
C5014 1.0UF 20% 6.3V X5R 0201-1 (U5000.F9:3mm)

PP1V25_S2 (70) — IccMax SE only: 10mA — Based on SPMI only use case
C5002 0.22UF 20% 6.3V X5R 0201 (U5000.F8:3mm)
C5003 0.22UF 20% 6.3V X5R 0201 (U5000.E7:3mm)

VDDBOOST_SE — R5030 0 1/20W MF 0201 5% — VUP_SE

VDDPLL_SE
VDDNV_SE
VDDC_SE

C5008 0.22UF 20% 6.3V X5R 0201 (U5000.B5:3mm)
C5009 0.22UF 20% 6.3V X5R 0201 (U5000.E8:3mm)
C5010 0.22UF 20% 6.3V X5R 0201 (U5000.E9:3mm)

PP3V8_AON_VDDMAIN (71) — IccMax: 100mA — As per NXP preliminary estimate, final pending
C5051 2.2UF 20% 10V X5R 0201

U5000
SN210VUK/B101V7
WLCSP
OMIT_TABLE

H9	PMUVCC1		
J9	PMUVCC2		
G8	SIMVCC1		
H8	SIMVCC2		
A8	VDDBOOST		
A9	VDDBOOST		
B4	VDDA	NC	
E9	VDDC		
F9	VDDCIN		
F8	VDDIO		
E7	VDDIO_I2C		
J1	VDDIO_SE		
A5	VDDMIX	NC	
E8	VDDNV		
B2	VDDPA	NC	
B5	VDDPLL		
A2	VUP		
A7	VBAT		
D9	VBATPWR		

D4	NFC_CLK_32K		
H6	NFC_CLK_REQ	NC	
A6	NFC_CLK_XTAL1		
G4	NFC_DWL_REQ	21 SE_CTLR_FW_DWLD	
F6	NFC_GPIO0	TP_SE_GPIO0	
J7	NFC_GPIO1		50K internal pull-down
J5	NFC_GPIO2_AO	NC	
H4	NFC_GPIO3_AO	NC	
E6	NFC_HSU_CTS	R5042 47K 1/20W MF 201 5% (NO_TEST) — UART_SE_R2D_RTS_L — NC_UART_SE_D2R_CTS_L	
F5	NFC_HSU_RTS		
G5	NFC_HSU_RX	R5041 47K 1/20W MF 201 5% (NO_TEST) — UART_SE_R2D — NC_UART_SE_D2R	
E5	NFC_HSU_TX		
E4	NFC_I2C_SCL	NC	
F4	NFC_I2C_SDA	NC	
J6	NFC_IRQ	NC	
G9	NFC_SIM_SWIO1	NC	
J8	NFC_SIM_SWIO2	NC	
H7	NFC_SPMI_SCLK	20 IN SPMI_SE_CLK	
G7	NFC_SPMI_SDATA	20 BI SPMI_SE_DATA	
H5	NFC_WKUP_REQ	21 SE_DEV_WAKE	
B6	NFC_XTAL2	NC	
G6	TM		
A3	RXP		
A4	RXN		

R5050 1M 5% 1/20W MF 201
R5051 1M 5% 1/20W MF 201

H3	SE_GPIO0	NC	
F3	SE_GPIO1	NC	Pulls to be added in system, can be NC'd if unused
G1	SE_I2C_SCL	NC_I2C_SE_SCL (IN 72)	
H1	SE_I2C_SDA	NC_I2C_SE_SDA (BI 72)	
F2	SE_ISO_CLK	NC	
F1	SE_ISO_IO	NC	
G3	SE_ISO_RST	NC	
G2	SE_SPI_CLK	NC	
J2	SE_SPI_CS	NC	
H2	SE_SPI_MISO	NC	
E2	SE_SPI_MOSI	NC	
D2	TXVCASCP	NC	
D1	TXVCASCN	NC	
B3	RXVCM	NC	
C2	TXVCM	NC	
A1	TX1	NC	
C1	TX2	NC	
D7	VCASCHI	NC	
C7	VCASCLO	NC	
B8	BOOST_LX	PP3V8_AON_VDDMAIN (71)	
B9	BOOST_LX		
B7	VHV	VHV_SE	
D3	VTUNE	NC	
D5	VEN	SE_PWR_EN (IN 33 67)	
C5	VREF	VREF_SE	

F7	VSS_DIG		
J3	VSS_DIG		
E1	VSS_DIG_2		
J4	VSS_DIG_LN		
C3	VSS_NFC		
B1	VSS_PA		
C4	VSS_PLL		
D6	VSS_PMU		
C8	VSS_PWR		
C9	VSS_PWR		
C6	VSS_REF		
D8	VSS_SUB		
E3	VSS_SUB		

C5004 0.1UF 10% 6.3V CERM-X5R 0201
C5017 0.22UF 20% 6.3V X5R 0201

R5000 47K 1/20W MF 201 5% — SE_CTLR_FW_DWLD (21)
R5006 47K 1/20W MF 201 5% — SE_DEV_WAKE (21)

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

SYNC_MASTER=will SYNC_DATE=02/20/2020
PAGE TITLE: Secure Element

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Power Input Connector

Port Caps

Pending qual and TDP increase

CRITICAL
L5105
500HM-25%-12A-0.00160HM
1206
155S00588

67 PPBUS_AON_PORT_CONN

OMIT_TABLE
514-00164
CRITICAL
J5100
RCPT-DC-RJ45-X1843
F-ST-TH

PWR
PWR
PWR
PWR
PWR
CC
ENET_MDI_TRAN_P<0>
ENET_MDI_TRAN_N<0>
ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>
ENET_MDI_TRAN_P<2>
ENET_MDI_TRAN_N<2>
ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_N<3>
GND
GND

PBUS_CC OUT 23 67

ENETCONN_MDI_T_P<0> BI 49 67
ENETCONN_MDI_T_N<0> BI 49 67
ENETCONN_MDI_T_P<1> BI 49 67
ENETCONN_MDI_T_N<1> BI 49 67
ENETCONN_MDI_T_P<2> BI 49 67
ENETCONN_MDI_T_N<2> BI 49 67
ENETCONN_MDI_T_P<3> BI 49 67
ENETCONN_MDI_T_N<3> BI 49 67

R5180
0
5%
3/4W
FF-LF
2010
102S0699

PPBUS_AON_PORT_CLAMP

NOSTUFF
Q5181
376S00344
AON2240
DFN

371S00157
SOD323F
TDZ18J
D5180
CRITICAL

R5182
1K
5%
1/20W
MF
201
117S0006

PBUS_PORT_EFUSE_OVP

C5181
0.01UF
10%
25V
X7R
0201
132S00070

R5181
120
5%
3/4W
FF-LF
2010
102S0734

CRITICAL
377S00202
U5180
TVS1800
SON

GND GND GND EPAD

PPBUS_AON_PORT 23 67

U5150.4:3mm C5140 2.2UF 10% 50V X5R 0603 138S1086
U5150.4:3mm C5141 2.2UF 10% 50V X5R 0603 138S1086
U5150.4:3mm C5142 0.1UF 10% 25V X7R-CERM-1 0402 132S0438
U5150.4:4mm EMC C5143 1000PF 5% 50V CERM-C0G 0402 131S0720
U5150.4:4mm EMC C5144 1000PF 5% 50V CERM-C0G 0402 131S0720

NOSTUFF
R5130
100K
1%
1/20W
MF
201
118S0014

NOSTUFF C5148 2.2UF 10% 50V X5R 0603 138S1086
NOSTUFF C5149 2.2UF 10% 50V X5R 0603 138S1086

CRITICAL
U5150
TPS259827ON
VQFN-THICKSTNCL
353S02330
2.7mohm typ
4.5mohm max

IN IN IN IN IN
OUT OUT OUT OUT OUT OUT OUT OUT
EN/UVLO
LDSTRT
NRETRY
RETRY_DLY
DVDT
GND GND GND
EPAD
PG
IMON
ILIM
ITIMER

PBUS_PORT_EFUSE_UVLO
EN/UVLO - 1V2 RISING, 0V1 HYS
PBUS_PORT_EFUSE_LDSTRT
LDSTRT - 1V2 RISING, 0V1 HYS
PBUS_PORT_EFUSE_NRETRY
PBUS_PORT_EFUSE_RETRY_DLY
PBUS_PORT_EFUSE_DVDT
VIN + 4V

NOSTUFF C5152 0.01UF 10% 25V X7R 0201 132S00070
C5151 0.01UF 10% 25V X7R 0201 132S00070
C5150 18NF 10% 50V X7R 0402 132S00236

C5160 4.7UF 20% 25V CER-X5R 0402 138S00187
C5161 4.7UF 20% 25V CER-X5R 0402 138S00187

PP_VDDD 23 67
R5159
20K
5%
1/20W
MF
201
117S0053

PBUS_PORT_EFUSE_PGOOD OUT 22 23 26 67 68

PBUS_PORT_EFUSE_IMON 67
MAKE_BASE=TRUE
PBUS_PORT_EFUSE_IMON OUT 40
Connected to 45k 2.2uF RC Filter
PBUS_PORT_EFUSE_ILIM 67
PBUS_PORT_EFUSE_ITIMER 67
PBUS_PORT_EFUSE_IMON OUT 25

C5155
0.01UF
10%
25V
X7R
0201
132S00070

R5155
100
1%
1/20W
MF
201
118S0011

R5156
649
1%
1/20W
MF
201
118S0478

PPBUS_AON 71

PLACE_SIDE=TOP
CRITICAL
C5104 68UF 20% 25V TANT-POLY CASE-D-SM 128S00117
C5112 68UF 20% 25V TANT-POLY CASE-D-SM 128S00117
C5114 68UF 20% 25V TANT-POLY CASE-D-SM 128S00117

H3mm : PLACE TOP LAYER

NOSTUFF CRITICAL C5100 22UF 20% 25V POLY-TANT CASED2-SM 128S0385
NOSTUFF CRITICAL C5102 22UF 20% 25V POLY-TANT CASED2-SM 128S0385
NOSTUFF CRITICAL C5106 22UF 20% 25V POLY-TANT CASED2-SM 128S0385
NOSTUFF CRITICAL C5108 22UF 20% 25V POLY-TANT CASED2-SM 128S0385
NOSTUFF CRITICAL C5110 22UF 20% 25V POLY-TANT CASED2-SM 128S0385

H2mm : PLACE BOTTOM LAYER

128s00117 used as primary source due to larger foorprint
128s00006 added as second source

128s00385 used as primary source due to larger foorprint
128s00217 added as second source

R5132
1K
1%
1/20W
MF
201
118S0012

67 23 IN PBUS_PORT_EFUSE_EN_3V3

C5131
1000PF
10%
25V
X7R
0201
132S00052

R5131
10K
1%
1/20W
MF
201
118S0013

TOTAL CAPACITANCE NOT TO EXCEED 1mF

SYSTEM CAPACITANCE

MAIN MLB + USB IO BOARD

540uF POLY TANT Capacitance

8x 22uF + 3x 68uF + 16x 10uF

366uF CERAMIC Capacitance

32x 10uF + 8x 4.7uF + 4x 2.2uF + Misc 1uF or less
* Value not derated for DC BIAS

SUDDEN POWER FAIL (SPF) Caps

SUDDEN POWER FAIL SOC SIGNAL

PP3V8_AON_VDDMAIN 26 40 71

R5185
20K
5%
1/20W
MF
201
117S0053

PBUS_PORT_EFUSE_PGOOD_L

376S00074
Q5185
SSM6N15AFEAP
SOT563
VER-1

NOSTUFF
C5185
0.01UF
10%
25V
X7R
0201
132S00070

MPMU_SNS_DIV OUT 31

R5186
180K
1%
1/20W
MF
201
118S0151

PBUS_PORT_EFUSE_PWROK 67

Q5185
SSM6N15AFEAP
SOT563
VER-1

68 67 26 23 22 PBUS_PORT_EFUSE_PGOOD

DC INLET BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
677-22697	1	CONN,RCPT,MAGNETO,X1843,GREY	J5100	CRITICAL	DC:A
677-22699	1	CONN,RCPT,MAGNETO,X1843,YELLOW	J5100	CRITICAL	DC:B
677-22700	1	CONN,RCPT,MAGNETO,X1843,GREEN	J5100	CRITICAL	DC:C
677-22702	1	CONN,RCPT,MAGNETO,X1843,BLUE	J5100	CRITICAL	DC:D
677-22704	1	CONN,RCPT,MAGNETO,X1843,RED	J5100	CRITICAL	DC:E
677-22703	1	CONN,RCPT,MAGNETO,X1843,PURPLE	J5100	CRITICAL	DC:F
677-22698	1	CONN,RCPT,MAGNETO,X1843,ORANGE	J5100	CRITICAL	DC:G

LDSTRT = GND disables watchdog timer

tretry [ms] = 0.0468 x C5151 [pF] + 0.2ms
C5151 = 10nF : 413ms RETRY timer

C5152 = Open : 4x auto-retry before LATCH OFF
= GND : disable auto-retry

slew rate [V/ms] = 4600 / C5150 [pF]
C5150 = 18nF : 0.256 V/ms slew rate (64ms)

ILIM = (1460 / C5150) + 0.11A
R5150 = 100 ohm : ILIM = 12.9A/14.7A
(MIN/TYP)

ILIM Blanking [ms] = C5155 [nF] x 0.98V / 2.1uA
C5155 = 10nF : 4.7ms typ ILIM Blanking

FAST ILIM = 2.1x ILIM
Pulling ILIM to GND triggers a FAULT
ILIM = OPEN sets ILIM = 0A

IMON : V = R5156 x 246uA/A x IPBUS
R5156 = 649 : Sets 0.16 V/A

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power Connectors

Apple Inc.

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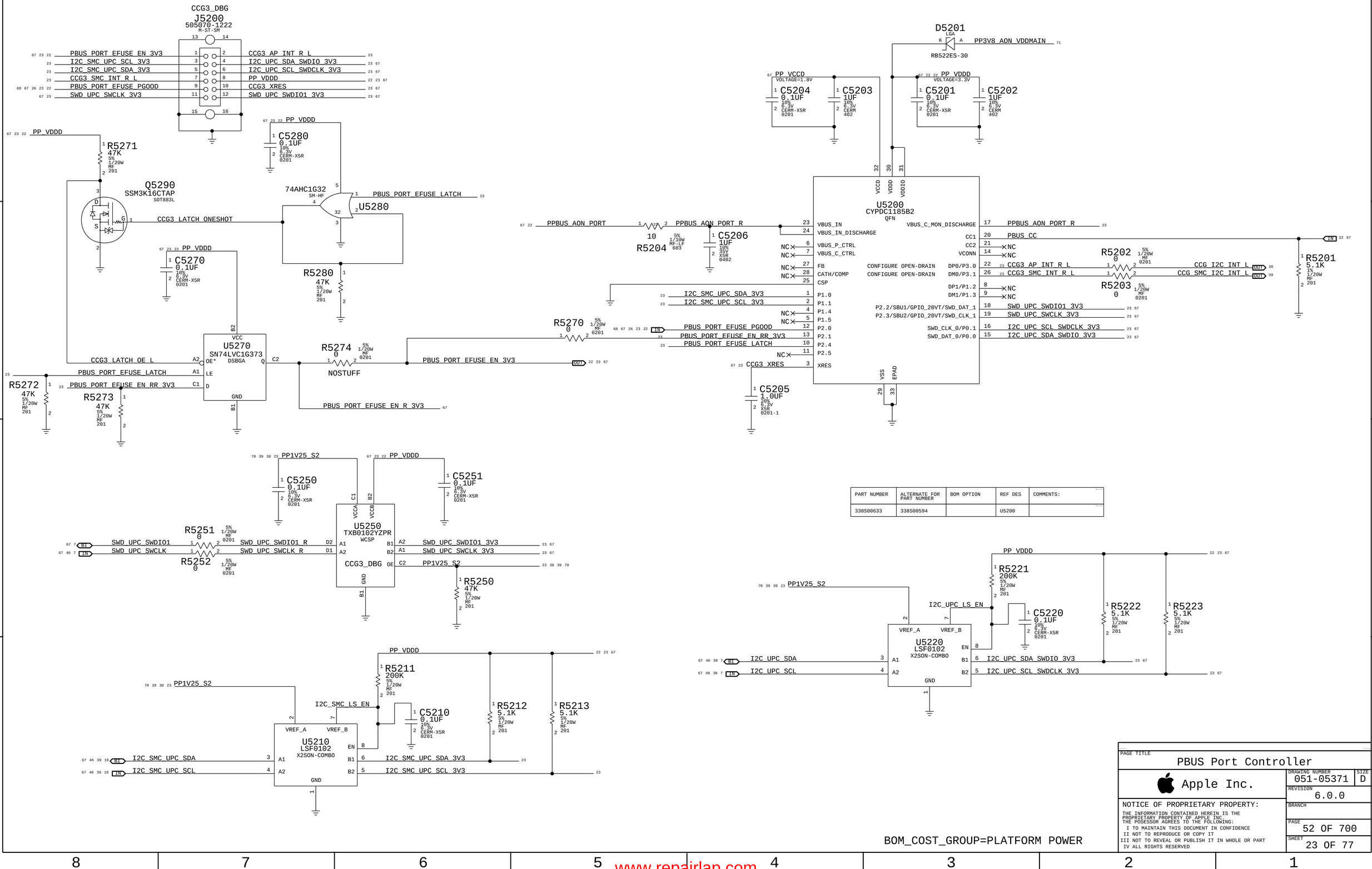

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00633	338S00594		U5200	

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PBUS Port Controller

Apple Inc.

DRAWING NUMBER 051-05371
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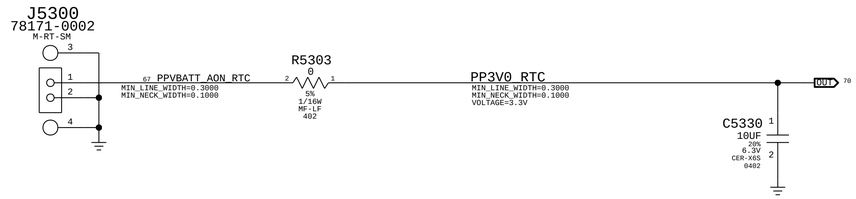
Battery Connector



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Battery Connector

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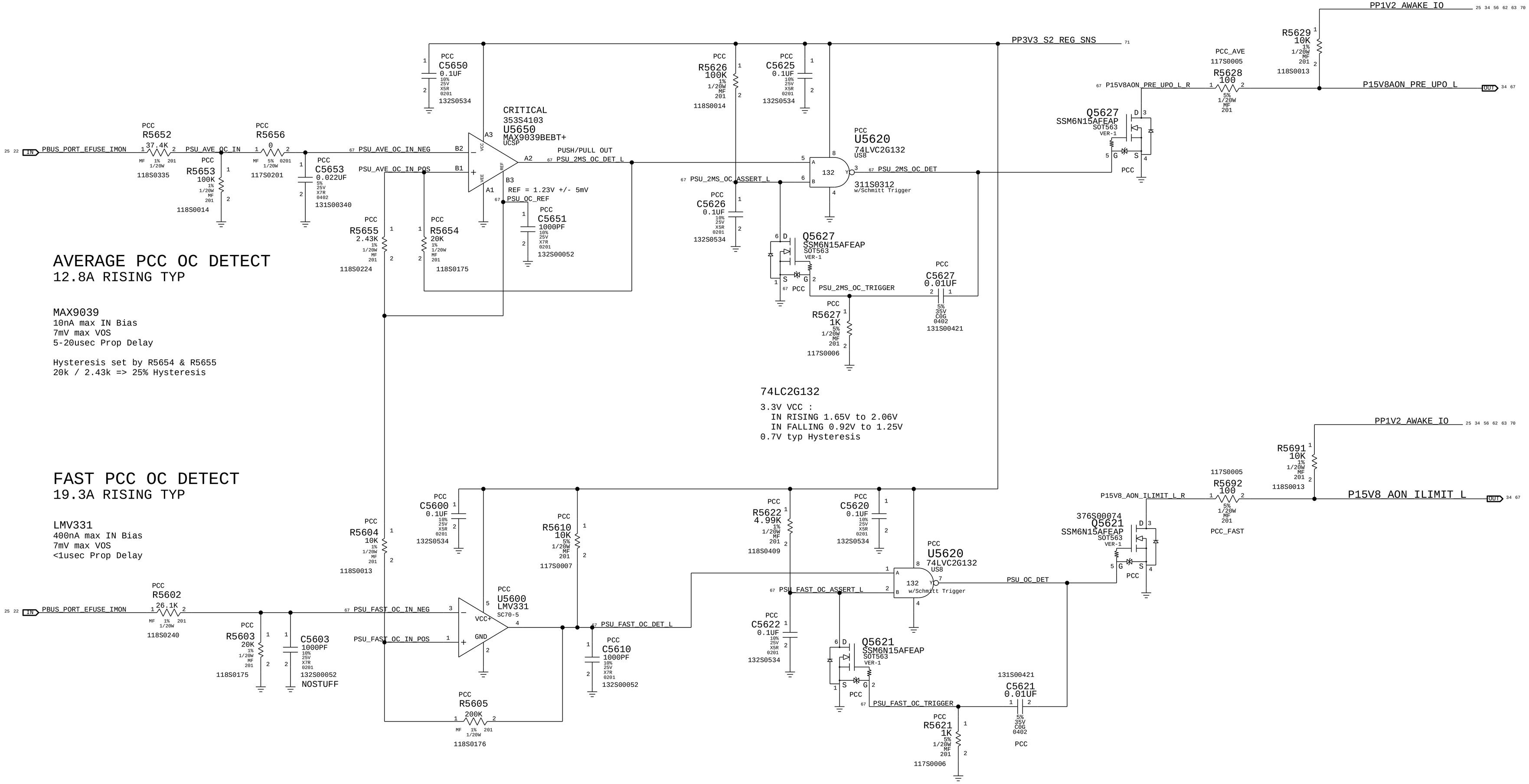
PSU Overcurrent Detection/Protection



AVERAGE PCC OC DETECT
12.8A RISING TYP

MAX9039
10nA max IN Bias
7mV max VOS
5-20usec Prop Delay

Hysteresis set by R5654 & R5655
20k / 2.43k => 25% Hysteresis

REF = 1.23V +/- 5mV

74LC2G132
3.3V VCC :
IN RISING 1.65V to 2.06V
IN FALLING 0.92V to 1.25V
0.7V typ Hysteresis

FAST PCC OC DETECT
19.3A RISING TYP

LMV331
400nA max IN Bias
7mV max VOS
<1usec Prop Delay

ASSERTION PERIOD

BOM_COST_GROUP=SENSORS

PAGE TITLE	PSU/PCC Sensor
Apple Inc.	DRAWING NUMBER 051-05371 SIZE D
	REVISION 6.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
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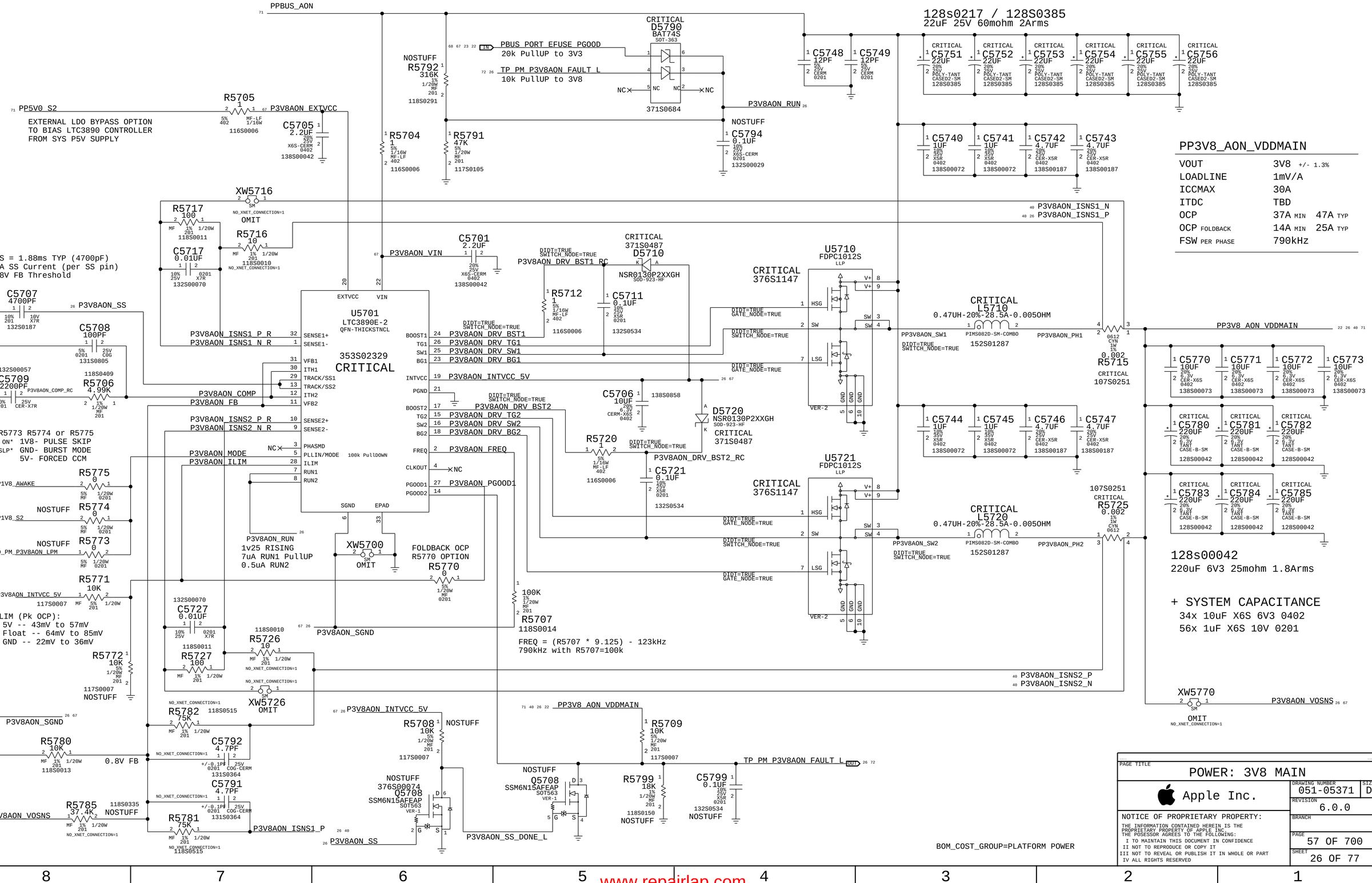
	SHEET 25 OF 77



SLAVE PMU BUCKS

U7700 SIM BGA SYM 1 OF 4 OMIT_TABLE

PP3V8_AON_VDDMAIN_SPMU

C7700 C7701 C7702 C7703 C7704 C7705 C7706 C7707 C7708 C7709 10UF 20% 6.3V CER-X6S 0402

C770A C770B C770C C770D C770E C770F C770G C770H C770I C770J 1UF 20% 10V X6S-CERM 0201

C770K C770L 1UF 20% 10V X6S-CERM 0201

C770M C770N 12PF 5% 25V NP0-C0G 0201

C771M C771N 3PF +/-0.1PF 25V C0G 0201

C772M C772N 12PF 5% 25V NP0-C0G 0201

C772N 3PF +/-0.1PF 25V C0G 0201

C773M 12PF 5% 50V NP0-C0G 0201

C773N 3PF +/-0.1PF 25V C0G 0201

C774M 12PF 5% 50V NP0-C0G 0201

C774N 3PF +/-0.1PF 25V C0G 0201

C775M 12PF 5% 25V NP0-C0G 0201

C775N 3PF +/-0.1PF 25V C0G 0201

C776M 12PF 5% 25V NP0-C0G 0201

C776N 3PF +/-0.1PF 25V C0G 0201

PP1V5_VLDOINT_SPMU

C7716 C771A 0.1UF 10% 10V X6S-CERM 0201

PP5V_BSTLQ_SPMU VOLTAGE=5V

C7717 C7714 C7715 0.1UF 10% 10V X6S-CERM 0201

PP1V25_S2

PP1V8_S2

FED BY SPMU BUCK13 (1.2V)POWER ALIAS=>

FED BY MPMU BUCK3 (1.8V)POWER ALIAS=>

VSS_ANA_SPMU

BUCK INPUTS

VDD_BUCK5_4_10 ×4 (C13 C14 G13 G14)
VDD_BUCK6 ×3 (M2 N2 P2)
VDD_BUCK12 ×2 (N6 P6)
VDD_BUCK13 ×2 (L13 L14)

MAIN INPUTS

VDD_MAIN_BUCK6 (L1)
VDD_MAIN_SOUTH (L9)
VDD_MAIN (E8)
VDD_MAIN_LDO ×2 (D2 E2)
VDD_MAIN_SNS (D8)
VDD_SNS_SPARE (E10)

BUCK OUTPUTS

VDD_ANA ×8 (C12 D3 E7 G12 K3 L8 L12 M6)
VDD_DIG ×4 (D5 D10 J3 J10)
VDD_BOOST (D9)
VDD_BOOST_LDO ×2 (B2 C2)
VDD_BOOST_SNS (E9)
VDD_HI_INT1 (D4)
VDD_HI_INT2 (L4)
VDD_HI_INT3 (L7)
VDD_HI_INT4 (M10)
VDD_HI_INT5 (J11)
VDD_HI_INT6 (A11)
VDD_HI_INT7 (C9)
VDDIO_1V2 (G10)
VDDIO_BUCK3 (H10)
VPP (K6)

PLACE_NEAR=U7700.L1:5MM
PLACE_NEAR=U7700.C13:5MM
PLACE_NEAR=U7700.G13:5MM
PLACE_NEAR=U7700.M2:5MM
PLACE_NEAR=U7700.N6:5MM
PLACE_NEAR=U7700.L13:5MM
PLACE_NEAR=U7700.D9:5MM
PLACE_NEAR=U7700.C9:5MM
PLACE_NEAR=U7700.D4:5MM
PLACE_NEAR=U7700.L7:5MM
PLACE_NEAR=U7700.G10:5MM
PLACE_NEAR=U7700.H10:5MM

BUCK4_LX0 F14 — BUCK4_LX0 — DIDT=TRUE SWITCH_NODE=TRUE — L7740 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
BUCK4_LX1 D13 D14 — BUCK4_LX1 — DIDT=TRUE SWITCH_NODE=TRUE — L7741 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
BUCK4_FB F11 — BUCK4_FB — R770A 0 5% 1/20W MF 0201 — BUCK4_FB_R — XW7700 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK4_VSS_FB F12 — VSS_ANA_SPMU
BUCK5_LX_0 H13 BUCK5_LX_1 H14 — BUCK5_LX0 — DIDT=TRUE SWITCH_NODE=TRUE — L7750 0.47UH-20%-4A-0.027OHM 2012
BUCK5_FB H11 — BUCK5_FB — R770B 0 5% 1/20W MF 0201 — BUCK5_FB_R — XW7701 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK5_VSS_FB H12 — VSS_ANA_SPMU
BUCK6_LX_0 M3 BUCK6_LX_1 N3 BUCK6_LX_2 P3 — BUCK6_LX0 — DIDT=TRUE SWITCH_NODE=TRUE — L7760 0.47UH-20%-6.9A-0.022OHM PIUA25201B-SM
BUCK6_FB L3 — BUCK6_FB — R770C 0 5% 1/20W MF 0201 — BUCK6_FB_R — XW7760 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK6_VSS_FB K2 — VSS_ANA_SPMU
BUCK6_VOUT_0 M1 BUCK6_VOUT_1 N1 BUCK6_VOUT_2 P1 — PP2V5_AWAKESW_NANDVCC
BUCK10_LX_0 B13 BUCK10_LX_1 B14 — BUCK10_LX0 — DIDT=TRUE SWITCH_NODE=TRUE — L77A0 0.47UH-20%-4A-0.027OHM 2012
BUCK10_FB B11 — BUCK10_FB — R770D 0 5% 1/20W MF 0201 — BUCK10_FB_R — XW77A0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK10_VSS_FB B12 — VSS_ANA_SPMU
BUCK12_LX_0 N5 BUCK12_LX_1 P5 — BUCK12_LX0 — DIDT=TRUE SWITCH_NODE=TRUE — L77C0 0.47UH-20%-4A-0.027OHM 2012
BUCK12_FB L5 — BUCK12_FB — R770E 0 5% 1/20W MF 0201 — BUCK12_FB_R — XW77C0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK12_VSS_FB M5 — VSS_ANA_SPMU
BUCK13_LX_0 K13 BUCK13_LX_1 K14 — BUCK13_LX0 — DIDT=TRUE SWITCH_NODE=TRUE — L77D0 0.47UH-20%-4A-0.027OHM 2012
BUCK13_FB K11 — BUCK13_FB — R770F 0 5% 1/20W MF 0201 — BUCK13_FB_R — XW77D0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK13_VSS_FB K12 — VSS_ANA_SPMU

PP1V06_S2SW_DRAM: C7740 C7741 C7742 C7743 C7744 C7745 C7746 C7747 15UF 20% 2V X6S 0402
C7713 C7712 C7711 C7710 15UF 20% 2V X6S 0402
C777M 12PF 5% 25V NP0-C0G 0201
C777N 3PF +/-0.1PF 25V C0G 0201

PP0V76_S1_SRAM: C7750 C7751 C7752 C7753 C7754 C7755 C7756 C7757 15UF 20% 2V X6S 0402
C778M 12PF 5% 25V NP0-C0G 0201
C778N 3PF +/-0.1PF 25V C0G 0201

PP2V5_AWAKESW_NANDVCC: C7760 C7761 C7762 C7763 C7764 C7765 C776C C776D 10UF 20% 6.3V CER-X6S 0402
C7766 C7767 C7768 C7769 C776A C776B C776E C776F 10UF 20% 6.3V CER-X6S 0402
C779M 12PF 5% 25V NP0-C0G 0201
C779N 3PF +/-0.1PF 25V C0G 0201

PP0V6_S1_VDDQL: C77A0 C77A1 C77A2 C77A3 C7723 C7722 15UF 20% 2V X6S 0402
C7790 12PF 5% 25V NP0-C0G 0201
C7791 3PF +/-0.1PF 25V C0G 0201

PP0V88_S1: C77C0 C77C1 C77C2 C77C3 C7719 C7718 C7721 C7720 15UF 20% 2V X6S 0402
C7792 12PF 5% 25V NP0-C0G 0201
C7793 3PF +/-0.1PF 25V C0G 0201

PP1V25_S2: C77D6 C77D3 C77D4 C77D5 C77D7 C77D8 15UF 20% 2V X6S 0402
C7794 12PF 5% 25V NP0-C0G 0201
C7795 3PF +/-0.1PF 25V C0G 0201

CRITICAL

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=saurabh SYNC_DATE=04/27/2020

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SLAVE PMU LDO

LDO INPUTS

LDO OUTPUTS

U7700 OMIT_TABLE
SIM
BGA
SYM 2 OF 4

LDO INPUTS

FROM BUCK13 POWER ALIAS => OR OPTION BUCK14 — 70 PP1V25_S2 — M7 VDD_LDO4
FROM BUCK13 POWER ALIAS => OR OPTION BUCK14 — 70 28 PPVDD_PMU_LDO_PREREG — C4 VDD_LDO8
FROM BUCK4 POWER ALIAS => — 70 PP1V06_S2SW_DRAM — N7 VDD_LDO11
FROM BUCK12 POWER ALIAS => — 70 28 PP0V88_S1 — P7 VDD_LDO12
71 41 28 27 PP3V8_AON_VDDMAIN_SPMU — A1 VDD_LDO15, A2 VDD_LDO15
FROM BUCK13 POWER ALIAS => OR OPTION BUCK14 — 70 28 PPVDD_PMU_LDO_PREREG — B4 VDD_LDO20

FROM BUCK3 POWER ALIAS => — 70 PP1V8_S2 — M11 VDD_SW4
FROM BUCK13 POWER ALIAS => — 70 29 PP1V25_S2 — M13 VDD_SW5, N13 VDD_SW5, P13 VDD_SW5
N11 VDD_SW6, P11 VDD_SW6, N9 VDD_SW7, P9 VDD_SW7
FROM BUCK12 POWER ALIAS => — 70 28 PP0V88_S1

71 41 28 27 PP3V8_AON_VDDMAIN_SPMU — J2 VDD_MAIN_BSTLQ

THIS IS AN OUTPUT(1.5V) => — E1 VLDOINT

67 27 PP1V5_VLDOINT_SPMU
VOLTAGE=1.5V

SWITCHED RAILS

LDO OUTPUTS

VLDO4 M8 PP0V72_S2_VDD_LOW — 28 70
VLDO6 D1 NC_SPMU_VLDO6 — 30
VLDO8 C3 PP1V2_AWAKE_PLL — 28 70
VLDO9 E3 UNUSED_SPMU_VLDO9 — 28 30
VLDO11 N8 PP0V855_S2SW_CIO — 28 70
VLDO12 P8 PP0V805_S1_VDD_FIXED — 28 70
VLDO15 A3 NC_SPMU_VLDO15 — 30
VLDO17 B1 NC_SPMU_VLDO17 — 30
VLDO18 C1 NC_SPMU_VLDO18 — 30
VLDO20 B3 PP1V2_S2_CIO — 28 70

BUCK_SW4 M12
BUCK_SW5 M14 PP1V225_AWAKESW_VCCQ — 28 70
BUCK_SW5 N14
BUCK_SW5 P14
BUCK_SW6 N12 PP0V88_AWAKESW_NAND — 28 70
BUCK_SW6 P12
BUCK_SW7 N10
BUCK_SW7 P10

BSTLQ_LX G1 SPMU_BSTLQ_LX
BSTLQ_FB J1 27 PP5V_BSTLQ_SPMU — SWITCH_NODE=TRUE DIDT=TRUE
BSTLQ_VOUT H1 — VOLTAGE=5V

VCP_OUT_SPARE M9 NO_TEST=1, NC_SPMU_VCP_OUT_SPARE
VMBX_SPARE F10 NC_SPMU_VMBX_SPARE, NO_TEST=1

67 PP1V8_AWAKE_SPMU_GPIO — VOLTAGE=1.8V

<==BUCK4_SW USED FOR SPMU GPIO, INTERNALLY CONNECTED

PLACE_NEAR=U7700.M12:5MM
C7822 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U7700.M12:5MM
C7898 12PF 5% 25V NP0-C0G 0201
C7899 3PF +/-0.1PF 25V C0G 0201

L7800
0.47UH-20%-1.7A-0.175OHM
PIJT1005FE-SM-COMBO
G1 — 1 — 2 — PP3V8_AON_VDDMAIN_SPMU — 27 28 41 71

XW78D0 SM

PP5V_BSTLQ_VOUT_SPMU — VOLTAGE=5V — 67

PLACE_NEAR=U7700.H1:5MM
C7892 12PF 5% 25V NP0-C0G 0201
PLACE_NEAR=U7700.H1:5MM
C7893 3PF +/-0.1PF 25V C0G 0201
CRITICAL C7800 20UF 20% 10V X5R 0402
CRITICAL C7801 20UF 20% 10V X5R 0402
CRITICAL C7831 0.1UF 10% 10V X6S-CERM 0201
PLACE_NEAR=U7700.H1:5MM
GND — 29 30

PLACE_NEAR=U7700.J1:5MM
CRITICAL C7825 0.1UF 10% 10V X6S-CERM 0201

DECOUPLING : BSTLQ
PP3V8_AON_VDDMAIN_SPMU — 27 28 41 71
PLACE_NEAR=L7800.2:5MM
C7890 12PF 5% 25V NP0-C0G 0201
PLACE_NEAR=L7800.2:5MM
C7891 3PF +/-0.1PF 25V C0G 0201
CRITICAL C7815 1UF 20% 10V X6S-CERM 0201
CRITICAL C7816 1UF 20% 10V X6S-CERM 0201
PLACE_NEAR=U7700.J2:5MM
PLACE_NEAR=U7700.J2:5MM

CRITICAL C7810 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7811 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7812 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : VDD_LDO8
PPVDD_PMU_LDO_PREREG — 28 70
PLACE_NEAR=U7700.C4:5MM
CRITICAL C7813 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : VDD_LDO20
PPVDD_PMU_LDO_PREREG — 28 70
PLACE_NEAR=U7700.B4:5MM
CRITICAL C7814 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : LDO20
PLACE_NEAR=U7700.B3:5MM
PP1V2_S2_CIO — 28 70
NOSTUFF
CRITICAL C7804 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.B3:5MM
CRITICAL C780A 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : LDO8
PLACE_NEAR=U7700.C3:5MM
PP1V2_AWAKE_PLL — 28 70
PLACE_NEAR=U7700.C3:5MM
CRITICAL C7805 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7806 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : LDO12
PLACE_NEAR=U7700.P8:5MM
PP0V805_S1_VDD_FIXED — 28 70
CRITICAL C7821 10UF 20% 6.3V CER-X6S 0402
CRITICAL C780B 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.P8:5MM

DECOUPLING : LDO11
PP0V855_S2SW_CIO — 28 70
PLACE_NEAR=U7700.N8:5MM
CRITICAL C7809 10UF 20% 6.3V CER-X6S 0402
NOSTUFF
CRITICAL C780C 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.N8:5MM

DECOUPLING : LDO9
PLACE_NEAR=U7700.E3:5MM
UNUSED_SPMU_VLDO9 — 28 30
CRITICAL C7824 1UF 20% 10V X6S-CERM 0201
CRITICAL C7835 1UF 20% 10V X6S-CERM 0201
PLACE_NEAR=U7700.E3:5MM

DECOUPLING : LDO4
PP0V72_S2_VDD_LOW — 28 70
PLACE_NEAR=U7700.M8:5MM
CRITICAL C7820 10UF 20% 6.3V CER-X6S 0402
CRITICAL C780D 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.M8:5MM

DECOUPLING : SW6/7
PLACE_NEAR=U7700.N12:5MM
PP0V88_AWAKESW_NAND — 28 70
PLACE_NEAR=U7700.N12:5MM
CRITICAL C7830 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7829 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7828 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.N12:5MM
C7894 12PF 5% 25V NP0-C0G 0201
C7895 3PF +/-0.1PF 25V C0G 0201
PLACE_NEAR=U7700.N12:5MM
PLACE_NEAR=U7700.N12:5MM

DECOUPLING : SW5
PLACE_NEAR=U7700.M14:5MM
PP1V225_AWAKESW_VCCQ — 28 70
PLACE_NEAR=U7700.M14:5MM
CRITICAL C7802 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7803 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.M14:5MM
C7896 12PF 5% 25V NP0-C0G 0201
C7897 3PF +/-0.1PF 25V C0G 0201
PLACE_NEAR=U7700.M14:5MM

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=saurabh — SYNC_DATE=04/27/2009

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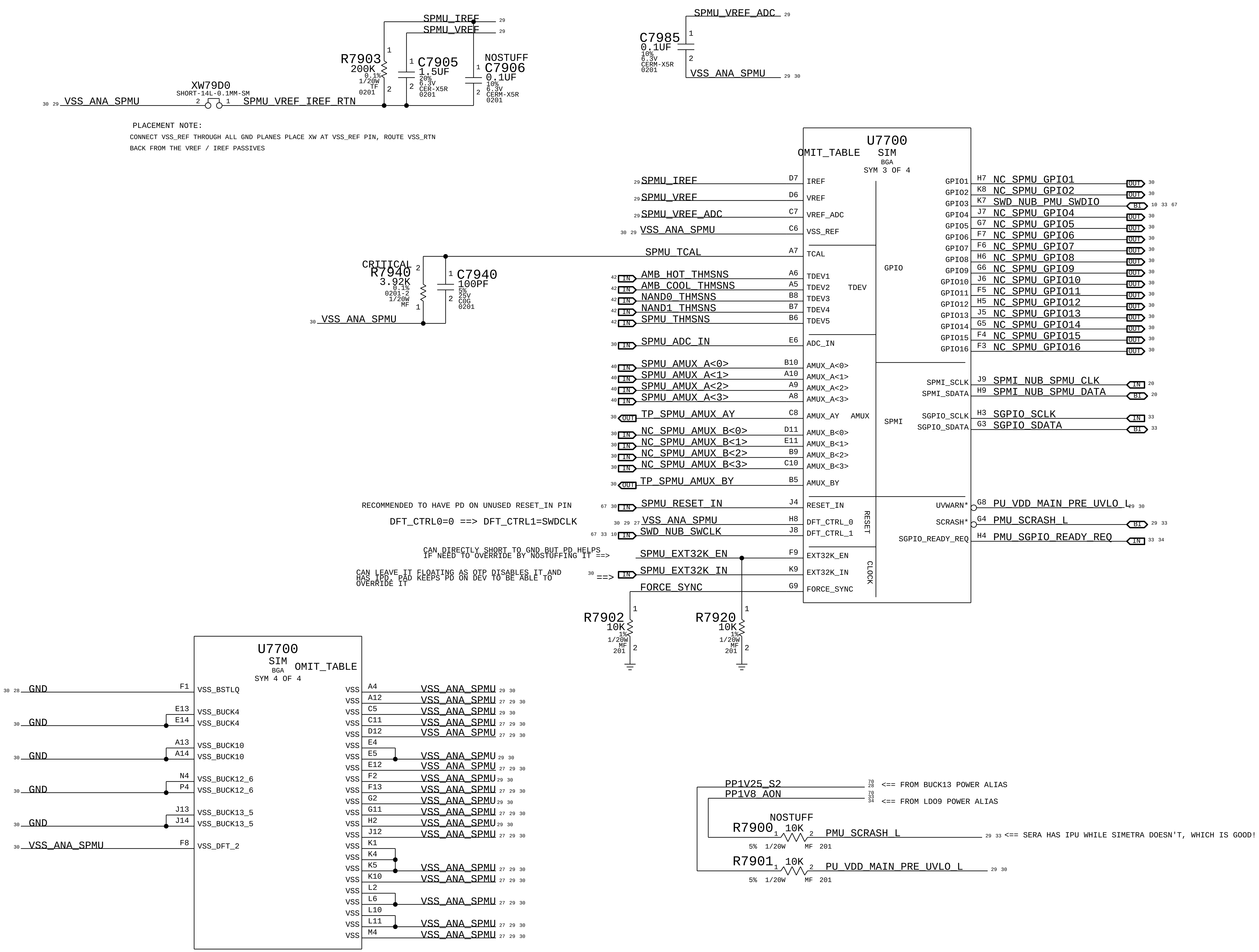
SLAVE PMU GND,ADC,& GPIO



SPMU_IREF
SPMU_VREF
R7903
200K
0.1%
1/20W
TF
0201
C7905
1.5UF
20%
6.3V
CER-X5R
0201
NOSTUFF
C7906
0.1UF
10%
6.3V
CERM-X5R
0201
XW79D0
SHORT-14L-0.1MM-SM
VSS_ANA_SPMU
SPMU_VREF_IREF_RTN
PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN
BACK FROM THE VREF / IREF PASSIVES
SPMU_VREF_ADC
C7985
0.1UF
10%
6.3V
CERM-X5R
0201
VSS_ANA_SPMU
U7700
OMIT_TABLE
SIM
BGA
SYM 3 OF 4
SPMU_IREF
SPMU_VREF
SPMU_VREF_ADC
VSS_ANA_SPMU
SPMU_TCAL
CRITICAL
R7940
3.92K
0.1%
0201-2
1/20W
MF
C7940
100PF
5%
25V
C0G
0201
AMB_HOT_THMSNS
AMB_COOL_THMSNS
NAND0_THMSNS
NAND1_THMSNS
SPMU_THMSNS
SPMU_ADC_IN
SPMU_AMUX_A<0>
SPMU_AMUX_A<1>
SPMU_AMUX_A<2>
SPMU_AMUX_A<3>
TP_SPMU_AMUX_AY
NC_SPMU_AMUX_B<0>
NC_SPMU_AMUX_B<1>
NC_SPMU_AMUX_B<2>
NC_SPMU_AMUX_B<3>
TP_SPMU_AMUX_BY
RECOMMENDED TO HAVE PD ON UNUSED RESET_IN PIN
SPMU_RESET_IN
DFT_CTRL0=0 ==> DFT_CTRL1=SWDCLK
SWD_NUB_SWCLK
CAN DIRECTLY SHORT TO GND BUT PD HELPS IF NEED TO OVERRIDE BY NOSTUFFING IT ==>
SPMU_EXT32K_EN
CAN LEAVE IT FLOATING AS OTP DISABLES IT AND HAS IPD. PAD KEEPS PD ON DEV TO BE ABLE TO OVERRIDE IT
SPMU_EXT32K_IN
FORCE_SYNC
IREF
VREF
VREF_ADC
VSS_REF
TCAL
TDEV1
TDEV2
TDEV3
TDEV4
TDEV5
TDEV
ADC_IN
AMUX_A<0>
AMUX_A<1>
AMUX_A<2>
AMUX_A<3>
AMUX_AY
AMUX
AMUX_B<0>
AMUX_B<1>
AMUX_B<2>
AMUX_B<3>
AMUX_BY
RESET_IN
DFT_CTRL_0
DFT_CTRL_1
RESET
EXT32K_EN
EXT32K_IN
FORCE_SYNC
CLOCK
GPIO
SPMI
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
NC_SPMU_GPIO1
NC_SPMU_GPIO2
SWD_NUB_PMU_SWDIO
NC_SPMU_GPIO4
NC_SPMU_GPIO5
NC_SPMU_GPIO6
NC_SPMU_GPIO7
NC_SPMU_GPIO8
NC_SPMU_GPIO9
NC_SPMU_GPIO10
NC_SPMU_GPIO11
NC_SPMU_GPIO12
NC_SPMU_GPIO13
NC_SPMU_GPIO14
NC_SPMU_GPIO15
NC_SPMU_GPIO16
SPMI_SCLK
SPMI_SDATA
SPMI_NUB_SPMU_CLK
SPMI_NUB_SPMU_DATA
SGPIO_SCLK
SGPIO_SDATA
UVWARN*
SCRASH*
SGPIO_READY_REQ
PU_VDD_MAIN_PRE_UVLO_L
PMU_SCRASH_L
PMU_SGPIO_READY_REQ
R7902
10K
1%
1/20W
MF
201
R7920
10K
1%
1/20W
MF
201
U7700
SIM
BGA
SYM 4 OF 4
OMIT_TABLE
GND
VSS_BSTLQ
VSS_BUCK4
VSS_BUCK10
VSS_BUCK12_6
VSS_BUCK13_5
VSS_DFT_2
VSS
VSS_ANA_SPMU
PP1V25_S2
<== FROM BUCK13 POWER ALIAS
PP1V8_AON
<== FROM LDO9 POWER ALIAS
NOSTUFF
R7900
10K
5%
1/20W
MF
201
PMU_SCRASH_L
<== SERA HAS IPU WHILE SIMETRA DOESN'T, WHICH IS GOOD!
R7901
10K
5%
1/20W
MF
201
PU_VDD_MAIN_PRE_UVLO_L

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PMU: SLAVE GPIO & GND

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SLAVE PMU AMUX ALIAS

NC_SPMU_AMUX_B<0..3> — NC_SPMU_AMUX_B<0..3> (OUT, 29)
MAKE_BASE=TRUE NO_TEST=1

SLAVE PMU GPIOS

29 NC_SPMU_GPIO1	NC_SPMU_GPIO1	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO2	NC_SPMU_GPIO2	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO4	NC_SPMU_GPIO4	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO5	NC_SPMU_GPIO5	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO6	NC_SPMU_GPIO6	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO7	NC_SPMU_GPIO7	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO8	NC_SPMU_GPIO8	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO9	NC_SPMU_GPIO9	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO10	NC_SPMU_GPIO10	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO11	NC_SPMU_GPIO11	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO12	NC_SPMU_GPIO12	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO13	NC_SPMU_GPIO13	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO14	NC_SPMU_GPIO14	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO15	NC_SPMU_GPIO15	MAKE_BASE=TRUE NO_TEST=1
29 NC_SPMU_GPIO16	NC_SPMU_GPIO16	MAKE_BASE=TRUE NO_TEST=1

SLAVE PMU PROBE POINTS

29 (OUT) SPMU_EXT32K_IN
FLOATING IS OK AS OTP DISABLES IT W/ IPD. PAD KEEPS PD ON DEV TO BE ABLE TO OVERRIDE IT
NOSTUFF R8001 100K 5% 1/20W MF 201 (1–2)

29 (OUT) SPMU_ADC_IN
PLACE_NEAR=U7700.E6:5MM
R8002 1M 5% 1/20W MF 201 (1–2)

67 29 (OUT) SPMU_RESET_IN
R8003 100K 5% 1/20W MF 201 (1–2)

27 (IN) BUCK4_LX0 — PP8040 P4MM SM (PP, 1)
27 (IN) BUCK4_LX1 — PP8041 P4MM SM (PP, 1)
27 (IN) BUCK5_LX0 — PP8050 P4MM SM (PP, 1)
27 (IN) BUCK6_LX0 — PP8060 P4MM SM (PP, 1)
27 (IN) BUCK10_LX0 — PP80A0 P4MM SM (PP, 1)
27 (IN) BUCK12_LX0 — PP80C0 P4MM SM (PP, 1)
27 (IN) BUCK13_LX0 — PP80D0 P4MM SM (PP, 1)

VSS alias connection

29 GND
29 GND
29 GND
29 GND
29 28 GND

& WIDTH XW IS LAYOUT DEPENDENT

29 VSS_ANA_SPMU
29 VSS_ANA_SPMU
29 27 VSS_ANA_SPMU
29 27 VSS_ANA_SPMU
29 27 VSS_ANA_SPMU
29 VSS_ANA_SPMU
29 VSS_ANA_SPMU
29 VSS_ANA_SPMU
29 VSS_ANA_SPMU
29 VSS_ANA_SPMU

67 VSS_ANA_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
VOLTAGE=0

XW8001 (2–1) SHORT-12L-0.25MM-SM
XW8002 (2–1) SHORT-12L-0.25MM-SM

XW8000 SHORT-12L-0.25MM-SM (1–2)
40 GND_SPMU_AMUX

29 TP_SPMU_AMUX_AY — TP_SPMU_AMUX_AY MAKE_BASE=TRUE
29 TP_SPMU_AMUX_BY — TP_SPMU_AMUX_BY MAKE_BASE=TRUE

29 (IN) PU_VDD_MAIN_PRE_UVLO_L — PU_VDD_MAIN_PRE_UVLO_L MAKE_BASE=TRUE

SIMETRA UNUSED LDO

NC_SPMU_VLDO6		NC_SPMU_VLDO6	28
NC_SPMU_VLDO15	NO_TEST MAKE_BASE=TRUE	NC_SPMU_VLDO15	28
NC_SPMU_VLDO17	NO_TEST MAKE_BASE=TRUE	NC_SPMU_VLDO17	28
NC_SPMU_VLDO18	NO_TEST MAKE_BASE=TRUE	NC_SPMU_VLDO18	28
UNUSED_SPMU_VLDO9	NO_TEST MAKE_BASE=TRUE	UNUSED_SPMU_VLDO9	28

BOM_COST_GROUP=PLATFORM POWER

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MASTER PMU BUCKS

PP3V8_AON_VDDMAIN_MPMU

C81F8 C81F9 C81E0 C81E1 C81C0 C81C1 C81C2 C81C3 C81C4 — 1UF 20% 10V X6S-CERM 0201

C81F6 C81F7 C81C6 C81C7 C81C8 C81C9 C81CA C81CB C81CC C81CD — 1UF 20% 10V X6S-CERM 0201

CRITICAL C81D0 C81D1 C81D2 C81D3 C81D4 C81D5 C81D6 C81D7 C81D8 — 10UF 20% 6.3V CER-X6S 0402

CRITICAL C81D9 C81DA C81DB C81DC C81DD C81F2 C81F3 C81F4 C81F5 — 10UF 20% 6.3V CER-X6S 0402

PLACE_NEAR=U8100.L1:5MM PLACE_NEAR=U8100.R1:5MM PLACE_NEAR=U8100.W1:5MM PLACE_NEAR=U8100.Y7:5MM

C81FJ C81FK C81FL C81FM C81FN C81FP C81FQ C81FR — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

PLACE_NEAR=U8100.B1:5MM PLACE_NEAR=U8100.F1:5MM PLACE_NEAR=U8100.K1:5MM PLACE_NEAR=U8100.A15:5MM

C81FA C81FB C81FC C81FD C81FE C81FF C81FG C81FH — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

PLACE_NEAR=U8100.B15:5MM

C81F0 12PF 5% 25V NP0-C0G 0201; C81F1 3PF +/-0.1PF 25V C0G 0201

C8130 10UF 20% 6.3V CER-X6S 0402

FROM BUCK13 POWER ALIAS =>
OPTION BUCK14

70 PPVDD_PMU_LDO_PRERE

67 33 32 PP1V5_VLDOINT_MPMU

U8100
OMIT_TABLE SER
BGA
SYM 1 OF 6

L1	VDD_BUCK0_2_7_11	BUCK0_LX0 W6 Y6
L2	VDD_BUCK0_2_7_11	
L3	VDD_BUCK0_2_7_11	
L4	VDD_BUCK0_2_7_11	
R1	VDD_BUCK0_2_7_11	BUCK0_LX1 V1 V2 V3 V4
R2	VDD_BUCK0_2_7_11	
R3	VDD_BUCK0_2_7_11	
R4	VDD_BUCK0_2_7_11	
W1	VDD_BUCK0_2_7_11	BUCK0_LX2 P1 P2 P3 P4
W2	VDD_BUCK0_2_7_11	
W3	VDD_BUCK0_2_7_11	
W4	VDD_BUCK0_2_7_11	
W7	VDD_BUCK0_2_7_11	BUCK0_LX3 T1 T2 T3 T4
W11	VDD_BUCK0_2_7_11	
W15	VDD_BUCK0_2_7_11	
W19	VDD_BUCK0_2_7_11	
Y7	VDD_BUCK0_2_7_11	BUCK0_LX4 M1 M2 M3 M4
Y11	VDD_BUCK0_2_7_11	
Y15	VDD_BUCK0_2_7_11	
Y19	VDD_BUCK0_2_7_11	
A7	VDD_BUCK1_8_9	BUCK0_FB U6
A11	VDD_BUCK1_8_9	BUCK0_VSS_FB T6
B1	VDD_BUCK1_8_9	BUCK1_LX0 A6 B6
B2	VDD_BUCK1_8_9	
B3	VDD_BUCK1_8_9	
B4	VDD_BUCK1_8_9	BUCK1_LX1 C1 C2 C3 C4
B7	VDD_BUCK1_8_9	
B11	VDD_BUCK1_8_9	
F1	VDD_BUCK1_8_9	BUCK1_LX2 G1 G2 G3 G4
F2	VDD_BUCK1_8_9	
F3	VDD_BUCK1_8_9	
F4	VDD_BUCK1_8_9	BUCK1_LX3 E1 E2 E3 E4
K1	VDD_BUCK1_8_9	
K2	VDD_BUCK1_8_9	
K3	VDD_BUCK1_8_9	
K4	VDD_BUCK1_8_9	BUCK1_LX4 J1 J2 J3 J4
A15	VDD_BUCK3_14	
B15	VDD_BUCK3_14	
K19	VDD_LDO2	BUCK1_FB D6
L20	VDD_LDO3_14	BUCK1_VSS_FB E6
K21	VDD_LDO5	BUCK2_LX0 Y20
J19	VDD_LDO19	BUCK2_LX1 W18 Y18
C18	VDD_MAIN_WBOOST	
F20	VDD_MAIN_WBOOST	BUCK2_LX2 W16 Y16
F15	VDD_MAIN_WIDAC	
K11	VDD_MAIN	BUCK2_FB V20
V17	VDD_MAIN1	BUCK2_VSS_FB U20
E19	VDD_MAIN_DRV	
K10	VDD_MAIN_SNS	
F19	VDD_MAIN_SNS_WLED	
H8	VDD_BOOST_SNS	
R16	VDDIO_1V2	
N16	VDDIO_BUCK3	
N20	VDD_RTC_ALT	
K6	VPP	

VOLTAGE INPUTS | BUCK OUTPUTS | SENSE

67 40 31 PMU_VDD_HI

FED BY SPMU BUCK13 (1.2V)POWER ALIAS=>
FED BY MPMU BUCK3 (1.8V)POWER ALIAS=>70

PP1V25_S2
PP1V8_S2
70 PP3V0_RTC
COINCELL BATTERY =>
34 32 31 VSS_ANA_MPMU

PLACE_NEAR=U8100.R16:5MM
CRITICAL C8131 0.1UF 10% 10V X6S-CERM 0201
CRITICAL C8132 0.1UF 10% 10V X6S-CERM 0201
PLACE_NEAR=U8100.N16:5MM

71 41 34 33 31 PP3V8_AON_VDDMAIN_MPMU

PLACE_NEAR=U8110.5:5MM
C8128 0.1UF 10% 6.3V CERM-X5R 0201

OMIT_TABLE
R8100 887K 0.1% 1/20W TF 0201
71 PPBUS_AON
22 MPMU_SNS_DIV
R8101 453K 1% 1/20W MF 201
OMIT_TABLE

U8110
OPA333DCKG4
SC70-5-COMBO
PMU_VDD_HI 31 40 67

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_3S	<== FOR 3S BATTERY
103S00480	1	RES,MF,453KOHM,0.1,1/20W,0201	R8101	CRITICAL	PBUS_3S	
103S00481	1	RES,MF,910KOHM,0.1,1/20W,0201	R8100	CRITICAL	PBUS_12VDCIN	<== FOR 12V DCIN
103S00043	1	RES,MF,280KOHM,0.1,1/20W,0201	R8101	CRITICAL	PBUS_12VDCIN	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_15P8VDCIN	<== FOR 15.8V DCIN
103S00086	1	RES,MF,205KOHM,0.1%,1/20W,0201	R8101	CRITICAL	PBUS_15P8VDCIN	

CRITICAL L8100 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
BUCK0_LX0 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL L8101 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK0_LX1 DIDT=TRUE SWITCH_NODE=TRUE
152S01268

BUCK0_LX2 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL L8102 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK0_LX3 DIDT=TRUE SWITCH_NODE=TRUE
152S01268

BUCK0_LX4 DIDT=TRUE SWITCH_NODE=TRUE

R810A 0 5% 1/20W MF 0201
BUCK0_FB — BUCK0_FB_R
XW8100 SHORT-14L-0.1MM-SM
PLACE_NEAR=U8100.U6:5MM
VSS_ANA_MPMU 31 32 34

NO_XNET_CONNECTION=1

CRITICAL L8110 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
BUCK1_LX0 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL L8111 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK1_LX1 DIDT=TRUE SWITCH_NODE=TRUE
152S01268

BUCK1_LX2 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL L8112 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK1_LX3 DIDT=TRUE SWITCH_NODE=TRUE
152S01268

BUCK1_LX4 DIDT=TRUE SWITCH_NODE=TRUE

R810B 0 5% 1/20W MF 0201
BUCK1_FB — BUCK1_FB_R
XW8110 SHORT-14L-0.1MM-SM
PLACE_NEAR=U8100.D6:5MM
VSS_ANA_MPMU 32 34

NO_XNET_CONNECTION=1

CRITICAL L8120 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
BUCK2_LX0 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL L8121 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK2_LX1 DIDT=TRUE SWITCH_NODE=TRUE

BUCK2_LX2 DIDT=TRUE SWITCH_NODE=TRUE
152S01268

R810C 0 5% 1/20W MF 0201
BUCK2_FB — BUCK2_FB_R
XW8120 SHORT-14L-0.1MM-SM
PLACE_NEAR=U8100.V20:5MM
VSS_ANA_MPMU 32 33 34

NO_XNET_CONNECTION=1

CRITICAL C8100 C8101 C8102 C8103 C8104 C8105 — 15UF 20% 2V X6S 0402
PPVDD_PCPU_AWAKE 70

CRITICAL C8109 C810A C810B C810C C810D C810E — 15UF 20% 2V X6S 0402

PLACE_NEAR=L8100.2:5MM PLACE_NEAR=L8101.3:5MM
C81H0 C81H1 C81H2 C81H3 — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

NOSTUFF CRITICAL C8110 C8111 C8112 C8113 C8114 C8115 C811D C811E — 15UF 20% 2V X6S 0402
PPVDD_GPU_AWAKE 34 70

CRITICAL C8119 C811A C811B C811C C8116 NOSTUFF CRITICAL C8117 — 15UF 20% 2V X6S 0402

PLACE_NEAR=L8110.2:5MM PLACE_NEAR=L8111.3:5MM
PLACE_NEAR=L8110.2:5MM PLACE_NEAR=L8111.4:5MM
C81H4 C81H5 C81H6 C81H7 — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

CRITICAL C8120 NOSTUFF C8121 C8122 C8123 C8124 C8125 C8126 C8127 — 15UF 20% 2V X6S 0402
PPVDD_SOC_S1 70

PLACE_NEAR=L8120.2:5MM
C81H8 C81H9 — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=kaur-ath SYNC_DATE=04/27/2020
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MASTER PMU BUCKS & GND

U8100 SER BGA SYM 6 OF 6 OMIT_TABLE

VSS_BUCK0: N1 N2 N3 N4 U1 U2 U3 U4 W5 Y1 Y2 Y3 Y4 Y5 — GND
VSS_BUCK1: A1 A2 A3 A4 A5 B5 D1 D2 D3 D4 H1 H2 H3 H4 — GND
VSS_BUCK2: W17 W21 W22 Y17 Y21 Y22 — GND
VSS_BUCK3: A17 B17 — GND
VSS_BUCK7: W13 Y13 — GND
VSS_BUCK8: A9 B9 — GND
VSS_BUCK9_14: A13 B13 — GND
VSS_BUCK11: W9 Y9 — GND
VSS_BSTLQ: V22 — GND
VSS_WLED_LP: A21 A22 B21 B22
VSS_WLED_HP1: A20 B20 C20
VSS_WLED_HP2: D21 D22
VSS_REF: J11 — VSS_ANA_MPMU
VSS_DFT_2: K7 — VSS_ANA_MPMU

VSS_ANA_MPMU: A18 B8 B18 C6 C13 C17 D7 D15 D20 E7 E15 E20 F6 F22 G6 G18 H6 H18 J6 J13 J18 K18 L7 L9 L11 L12 L15 N5 N18 N22 P7 R18 T5 T18 U5 U19 V5 V9 V18 W12 W20

UNUSED ADC_IN PIN NEED 1M PD

MPMU_ADC_IN (34) — K9 ADC_IN
PP1V5_VLDOINT_MPMU (67 33 31) — PLACE_NEAR=U8100.C15:5MM
C8206 0.1UF 10% 10V X6S-CERM 0201

VDD_ANA: C7 C11 C15 F5 F18 J15 K5 K8 L5 P18 R5 V7 V11 V15 V19
VDD_DIG: D9 E16 J7 M18 P9 R17

MPMU_VREF (32) — K12 VREF
MPMU_VBAT (34) — J10 VBAT
MPMU_IBAT (34) — J9 IBAT
MPMU_IREF (32) — J8 IREF

UNUSED VBAT/IBAT PINS NEED 1M PD

U8100 SER BGA SYM 2 OF 6 OMIT_TABLE

BUCK OUTPUTS

BUCK3_LX: A16 BUCK3_LX0 (34) DIDT=TRUE SWITCH_NODE=TRUE
BUCK3_LX: B16
L8230 CRITICAL 0.47UH-20%-4A-0.027OHM 2012
R820A 0 5% 1/20W MF 0201
XW8230 SHORT-14L-0.1MM-SM NO_XNET_CONNECTION=1
BUCK3_FB: D16 BUCK3_FB (PLACE_NEAR=U8100.D16:5MM) — BUCK3_FB_R
BUCK3_VSS_FB: C16 VSS_ANA_MPMU (32 34)

L8270 1.0UH-20%-4A-0.038OHM CRITICAL PIKA20161B-COMBO
BUCK7_LX0: Y12 BUCK7_LX0 (34) DIDT=TRUE SWITCH_NODE=TRUE
L8271 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
BUCK7_LX1: W14 BUCK7_LX1 (34) DIDT=TRUE SWITCH_NODE=TRUE
BUCK7_LX1: Y14
R820B 0 5% 1/20W MF 0201 CRITICAL
XW8270 SHORT-14L-0.1MM-SM NO_XNET_CONNECTION=1
BUCK7_FB: U12 BUCK7_FB (PLACE_NEAR=U8100.U12:5MM) — BUCK7_FB_R
BUCK7_VSS_FB: V12 VSS_ANA_MPMU (32 34)

L8280 1.0UH-20%-4A-0.038OHM CRITICAL PIKA20161B-COMBO
BUCK8_LX0: A8 BUCK8_LX0 (34) DIDT=TRUE SWITCH_NODE=TRUE
L8281 0.22UH-20%-6.7A-0.023OHM CRITICAL PINA20121T-SM
BUCK8_LX1: A10 BUCK8_LX1 (34) DIDT=TRUE SWITCH_NODE=TRUE
BUCK8_LX1: B10
XW8280 SHORT-14L-0.1MM-SM NO_XNET_CONNECTION=1
BUCK8_FB: D8 BUCK8_FB
R820C 0 5% 1/20W MF 0201
BUCK8_VSS_FB: C8 VSS_ANA_MPMU (34) — BUCK8_FB_R (PLACE_NEAR=U8100.D8:5MM)

L8290 0.47UH-20%-4A-0.027OHM CRITICAL 2012
BUCK9_LX: A12 BUCK9_LX0 (34) DIDT=TRUE SWITCH_NODE=TRUE
BUCK9_LX: B12
XW8290 SHORT-14L-0.1MM-SM NO_XNET_CONNECTION=1
BUCK9_FB: D12 BUCK9_FB
R820D 0 5% 1/20W MF 0201
BUCK9_VSS_FB: C12 VSS_ANA_MPMU (34) — BUCK9_FB_R (PLACE_NEAR=U8100.D12:5MM)

L82B0 1.0UH-20%-4A-0.038OHM CRITICAL PIKA20161B-COMBO
BUCK11_LX0: Y8 BUCK11_LX0 (34) DIDT=TRUE SWITCH_NODE=TRUE
L82B1 0.22UH-20%-6.7A-0.023OHM CRITICAL PINA20121T-SM
BUCK11_LX1: W10 BUCK11_LX1 (34) DIDT=TRUE SWITCH_NODE=TRUE
BUCK11_LX1: Y10
R820E 0 5% 1/20W MF 0201
XW82B0 SHORT-14L-0.1MM-SM NO_XNET_CONNECTION=1
BUCK11_FB: U8 BUCK11_FB
BUCK11_VSS_FB: V8 VSS_ANA_MPMU (32 34) — BUCK11_FB_R (PLACE_NEAR=U8100.U8:5MM)

BUCK14_LX: A14 BUCK14_LX (34)
BUCK14_LX: B14
VIN FROM BUCK13 IS POR FOR LDO4,20,8. IF PDN (VMIN VIOLATION, WHEN LDO8 IN DROPOUT MODE) IS AN ISSUE THEN BUCK14 WILL BE THE BACKUP OPTION. THIS WOULD THEN REQUIRE ADDING BEAD AND CAPS
BUCK14_FB: D14 BUCK14_FB_MPMU (34)
BUCK14_VSS_FB: C14 VSS_ANA_MPMU (32 33 34)

SWITCHED RAILS

PP1V8_S2 (70 26) FROM BUCVK3 POWER ALIAS => VDD_SW1: R21 R22 VDD_SW2: T20 VDD_SW3: R19
PP1V25_S2 (70 68 32) FROM BUCK13 POWER ALIAS => VDD_SW3: R20

BUCK_SW1: P21 PP1V8_AWAKE (26 32 70)
BUCK_SW1: P22
BUCK_SW2: T19 NC_MPMU_BUCK_SW2 (NO_TEST=1)
BUCK_SW3: P19
BUCK_SW3: P20 PP1V2_AWAKE_IO (32 70)

PP1V8_S2 (70)
CRITICAL C8230 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8231 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8232 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8233 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8234 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8235 10UF 20% 6.3V CER-X6S 0402 (PLACE_NEAR=L8230.1:5MM)
C82D0 12PF 5% 25V NPO-C0G 0201
C82D1 3PF ±/-0.1PF 25V C0G 0201 (PLACE_NEAR=L8230.1:5MM)
CRITICAL C8236 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8237 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8238 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8239 10UF 20% 6.3V CER-X6S 0402
CRITICAL C823A 10UF 20% 6.3V CER-X6S 0402
CRITICAL C823B 10UF 20% 6.3V CER-X6S 0402

PPVDD_CPU_SRAM_AWAKE (70)
NOSTUFF C8270 15UF 20% 2V X6S 0402
NOSTUFF C8271 15UF 20% 2V X6S 0402
CRITICAL C8272 15UF 20% 2V X6S 0402
CRITICAL C8273 15UF 20% 2V X6S 0402
CRITICAL C8274 15UF 20% 2V X6S 0402
CRITICAL C8275 15UF 20% 2V X6S 0402 (PLACE_NEAR=L8270.1:5MM)
CRITICAL C8276 15UF 20% 2V X6S 0402
CRITICAL C8277 15UF 20% 2V X6S 0402
C82D2 12PF 5% 25V NPO-C0G 0201 (PLACE_NEAR=L8271.1:5MM)
C82D3 3PF ±/-0.1PF 25V C0G 0201

PPVDD_DISP_S1 (70)
CRITICAL C8280 15UF 20% 2V X6S 0402
CRITICAL C8281 15UF 20% 2V X6S 0402
CRITICAL C8282 15UF 20% 2V X6S 0402
CRITICAL C8283 15UF 20% 2V X6S 0402
CRITICAL C8284 15UF 20% 2V X6S 0402
CRITICAL C8285 15UF 20% 2V X6S 0402 (PLACE_NEAR=L8280.1:5MM)
C82D4 12PF 5% 25V NPO-C0G 0201
C82D5 3PF ±/-0.1PF 25V C0G 0201 (PLACE_NEAR=L8281.1:5MM)

PPVDD_DCS_S1 (70)
CRITICAL C8295 15UF 20% 2V X6S 0402
CRITICAL C8290 15UF 20% 2V X6S 0402
CRITICAL C8291 15UF 20% 2V X6S 0402
CRITICAL C8292 15UF 20% 2V X6S 0402
CRITICAL C8293 15UF 20% 2V X6S 0402
CRITICAL C8294 15UF 20% 2V X6S 0402 (PLACE_NEAR=L8290.1:5MM)
C82D6 12PF 5% 25V NPO-C0G 0201 (PLACE_NEAR=L8290.1:5MM)
C82D7 3PF ±/-0.1PF 25V C0G 0201

PPVDD_ECPU_AWAKE (70)
CRITICAL C82B6 15UF 20% 2V X6S 0402
CRITICAL C82B7 15UF 20% 2V X6S 0402
CRITICAL C82B8 15UF 20% 2V X6S 0402
CRITICAL C82B9 15UF 20% 2V X6S 0402
NOSTUFF C82B1 15UF 20% 2V X6S 0402
NOSTUFF C82B2 15UF 20% 2V X6S 0402
CRITICAL C82B3 15UF 20% 2V X6S 0402
CRITICAL C82B4 15UF 20% 2V X6S 0402
C82D8 12PF 5% 25V NPO-C0G 0201 (PLACE_NEAR=L82B1.1:5MM)
C82D9 3PF ±/-0.1PF 25V C0G 0201 (PLACE_NEAR=L82B0.1:5MM)

DECOUPLING : VDD_SW3
PP1V25_S2 (32 68 70) — PLACE_NEAR=U8100.R19:5MM
CRITICAL C8201 10UF 20% 6.3V CER-X6S 0402

MPMU_VREF (32)
MPMU_IREF (32)
C8204 1.5UF 20% 6.3V CER-X5R 0201
R8201 200K 0.1% 1/20W TF 0201
NOSTUFF C8205 0.1UF 10% 6.3V CERM-X5R 0201
XW82B2 SHORT-14L-0.1MM-SM
VSS_ANA_MPMU (34 33 32) — MPMU_VREF_IREF_RTN

CRITICAL C8240 15UF 20% 2V X6S 0402
CRITICAL C8241 15UF 20% 2V X6S 0402
PP1V2_AWAKE_IO (32 70)

CRITICAL C8202 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8203 10UF 20% 6.3V CER-X6S 0402
PP1V8_AWAKE (26 32 70)

PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN BACK FROM THE VREF / IREF PASSIVES

BOM_COST_GROUP=PLATFORM POWER

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MASTER PMU LDO,ADC, & GPIO

U8100 SER OMIT_TABLE
BGA
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IDAC_OUT<0>	NC_MPMU_IDAC_OUT<0>	G17	WLED_LP_LX	C21	NC_MPMU_WLED_LP_LX_0 NO_TEST=1
IDAC_OUT<1>	NC_MPMU_IDAC_OUT<1>	G16	WLED_LP_LX	C22	NC_MPMU_WLED_LP_LX_1 NO_TEST=1
IDAC_OUT<2>	NC_MPMU_IDAC_OUT<2>	G14			
IDAC_OUT<3>	NC_MPMU_IDAC_OUT<3>	G13			
IDAC_OUT<4>	NC_MPMU_IDAC_OUT<4>	H17	WLED_HP1_LX	A19	NC_MPMU_WLED_HP1_LX_0 NO_TEST=1
IDAC_OUT<5>	NC_MPMU_IDAC_OUT<5>	H16	WLED_HP1_LX	B19	NC_MPMU_WLED_HP1_LX_1 NO_TEST=1
IDAC_OUT<6>	NC_MPMU_IDAC_OUT<6>	H14	WLED_HP1_LX	C19	NC_MPMU_WLED_HP1_LX_2 NO_TEST=1
IDAC_OUT<7>	NC_MPMU_IDAC_OUT<7>	H13			
IDAC_OUT<8>	NC_MPMU_IDAC_OUT<8>	J16			
IDAC_OUT<9>	NC_MPMU_IDAC_OUT<9>	J14	WLED_HP2_LX	E21	NC_MPMU_WLED_HP2_LX_0 NO_TEST=1
IDAC_OUT<10>	NC_MPMU_IDAC_OUT<10>	K17	WLED_HP2_LX	E22	NC_MPMU_WLED_HP2_LX_1 NO_TEST=1
IDAC_OUT<11>	NC_MPMU_IDAC_OUT<11>	K16			
IDAC_OUT<12>	NC_MPMU_IDAC_OUT<12>	K14			
IDAC_OUT<13>	NC_MPMU_IDAC_OUT<13>	K13	WLED_VOUT_FB	E18	NC_MPMU_WLED_VOUT_FB NO_TEST=1
IDAC_OUT<14>	NC_MPMU_IDAC_OUT<14>	L17			
IDAC_OUT<15>	NC_MPMU_IDAC_OUT<15>	L16			
IDAC_OUT<16>	NC_MPMU_IDAC_OUT<16>	L14	VCP_OUT_SPARE	U21	NC_MPMU_VCP_OUT_SPARE NO_TEST=1
IDAC_OUT<17>	NC_MPMU_IDAC_OUT<17>	L13	VMBX_SPARE	J12	NC_MPMU_VMBX_SPARE NO_TEST=1
BSTLQ_LX					
BSTLQ_VOUT		T22			
VDD_BOOST		H9			
VDD_SNS_SPARE		H10			
VDD_HI_INT1		T21			
VDD_HI_INT2		H11			
VDD_HI_INT3		D13			
VDD_HI_INT4		D17			
VDD_HI_INT5		H12			
VDD_HI_INT6		L18			

CRITICAL L8300 0.47UH-20%-1.7A-0.175OHM
PIJT1005FE-SM-COMBO
SWITCH_NODE=TRUE DIOT=TRUE
PP3V8_AON_VDDMAIN_MPMU
MPMU_BSTLQ_LX
PP5V_BSTLQ_VOUT_MPMU
PP3V8_AON_VDDMAIN_MPMU
PP5V_BSTLQ_MPMU
VOLTAGE=5V
C83A0 12PF 5% 25V NP0-C0G 0201
C83A1 3PF +/-0.1PF 25V C0G 0201
C83A2 12PF 5% 25V NP0-C0G 0201
C83A3 3PF +/-0.1PF 25V C0G 0201
C8300 20UF 20% 10V X5R 0402
C8301 20UF 20% 10V X5R 0402
C8302 0.1UF 10% 10V X6S-CERM 0201
C8310 0.1UF 10% 10V X6S-CERM 0201
C8311 0.1UF 10% 10V X6S-CERM 0201
C8316 0.1UF 10% 10V X6S-CERM 0201
C8317 0.1UF 10% 10V X6S-CERM 0201
XW83D0 SM
PLACE_NEAR=U8100.T21:5MM
PLACE_NEAR=U8100.L18:5MM
PLACE_NEAR=U8100.T22:5MM
PLACE_NEAR=U8100.D17:5MM
PLACE_NEAR=U8100.H12:5MM
GND

U8100 SER OMIT_TABLE
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VDD_BOOST_LDO		G19	VLDO1	J22	PP2V5_S2
VDD_BOOST_LDO		G21	VLDO2	K20	NC_MPMU_VLDO2 NO_TEST=1
VDD_BOOST_LDO		H19	VLDO3	L21	PP1V2_S2
VDD_BOOST_LDO		H21	VLDO5	K22	NC_MPMU_VLDO5
VDD_BOOST_LDO		J21	VLDO7	H22	PP3V3_S2_UPC
VDD_MAIN_LDO		M20	VLDO9	M19	PP1V8_AON
LDO1_EN		N17	VLDO10	G20	NC_MPMU_VLDO10
VLDOINT		M21	VLDO13	H20	NC_MPMU_VLDO13
VLDORTC		N21	VLDO14	L19	NC_MPMU_VLDO14
			VLDO16	G22	NC_MPMU_VLDO16
			VLDO19	J20	NC_MPMU_VLDO19 NO_TEST=1
			VREF_ADC	H7	MPMU_VREF_ADC

LDO OUTPUTS

PP3V8_AON_VDDMAIN_MPMU
CRITICAL C8314 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8315 10UF 20% 6.3V CER-X6S 0402
LDO1 NOT USED ==> INT PD ENABLED
NC_MPMU_LDO1_EN
THIS IS AN OUTPUT ==> PP1V5_VLDOINT_MPMU
THIS IS AN OUTPUT ==> MPMU_VLDORTC
VOLTAGE=1.5V
PACK_OPTION=PORTABLE
MAKE_BASE=TRUE
CRITICAL C8326 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C8327 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C8328 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C8329 1.0UF 20% 6.3V X5R 0201-1
PACK_OPTION=DESKTOP
PACK_OPTION=DESKTOP
PACK_OPTION=DESKTOP
PACK_OPTION=DESKTOP
PORTABLE= NO CAPS NEEDED
DESKTOP =4X1UF

C8321 0.1UF 10% 6.3V CERM-X5R 0201
VSS_ANA_MPMU

PP1V2_S2
CRITICAL C8307 10UF 20% 6.3V CER-X6S 0402
CRITICAL C830A 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8309 10UF 20% 6.3V CER-X6S 0402

PP1V5_VLDOINT_MPMU
PLACE_NEAR=U8100.M21:5MM
CRITICAL C8322 10UF 20% 6.3V CER-X6S 0402
CRITICAL C830D 10UF 20% 6.3V CER-X6S 0402
C830G 220PF 10% 16V CER-X7R 0201
C830H 220PF 10% 16V CER-X7R 0201
PLACE_NEAR=U8100.M21:5MM
PLACE_NEAR=U8100.M21:5MM

PP1V8_AON
CRITICAL C8304 1UF 20% 10V X6S-CERM 0201
CRITICAL C830C 1UF 20% 10V X6S-CERM 0201

PP3V3_S2_UPC
NOSTUFF CRITICAL C8303 10UF 20% 6.3V CER-X6S 0402
CRITICAL C830E 10UF 20% 6.3V CER-X6S 0402

INTEGRATOR ALIAS TO:
1V8 OCARINA=Y
1V2 OCARINA=N

PP1V25_S2
R8343 10K 5% 1/20W MF 201 PMU_SYS_ALIVE 33 46 57 67 68 72
NOSTUFF

PP1V8_AON <== LDO9 POWER ALIAS
R8324 10K 5% 1/20W MF 201 PMU_ONOFF_L 33 66 67 68
R8325 100K 5% 1/20W MF 201 PU_PMU_RSLOC_RST_L 33 34
R8338 100K 5% 1/20W MF 201 NOSTUFF MPMU_FAULT_OUT_L 33 67
R8339 10K 5% 1/20W MF 201 NOSTUFF PMU_CRASH_L 33 67
OTP HAS IPU

FEED BY PP1V8_AON (LDO9)POWER ALIAS ==>
PP1V8_AON 70 34 33 29
XW83D1 SHORT-14L-0.1MM-SM
MPMU_VBUS_DET R7
VSS_ANA_MPMU E9
PMU_SHDN M8
R8322 10K 5% 1/20W MF 201 NOSTUFF

NXTAL_MEMS=0 ==> XTAL
VSS_ANA_MPMU N19
MPMU_XIN L22
MPMU_XOUT M22

U8100 SER OMIT_TABLE
BGA
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VDDMAIN_VREG_THMSNS		E8	TDEV1		
SOC_THMSNS		F9	TDEV2		
AMB_COOL1_THMSNS		F8	TDEV3		
NC_MPMU_TDEV4		F7	TDEV4		
NC_MPMU_TDEV5		G9	TDEV5		
WLANBT_THMSNS		G10	TDEV6		
BKLT_THMSNS		G8	TDEV7		
MPMU_THMSNS		G7	TDEV8		
MPMU_TCAL		F10	TCAL		
			GPIO1	P16	PU_IPD_LID_OPEN_1V8
			GPIO2	T9	NC_CHGR_AUX_OK
			GPIO3	T7	SWD_NUB_PMU_SWDIO
			IPU GPIO4	R11	CODEC_WAKE_L
			GPIO5	T8	WLBT_WAKE
			GPIO6	U7	ENET_WAKE_L
			GPIO7	T11	NC_HDMI_CEC_IRQ
			GPIO8	U10	USB3_WAKE_L
			GPIO9	R12	NC_HDMI_RESET_L
			GPIO10	U9	P5V_S2_PWR_EN_PWRSEQ
			GPIO11	T12	P3V3_S2_PWR_EN
			TDEV GPIO GPIO12	U11	PVDD1_PWR_EN
			GPIO13	T13	WLBT_PWR_EN
			GPIO14	U13	ENET_PWR_EN
			GPIO15	M13	SE_PWR_EN
			GPIO16	M14	PD_MPMU_GPIO16
			GPIO17	N14	NAND0_LPB_L
			GPIO18	R13	BL_PWR_EN
			GPIO19	U14	PD_PM_P3V8AON_LPM
			GPIO20	U15	LCD_PWR_EN
			GPIO21	T14	TP_MPMU_NAND0_RESET_L
			GPIO22	U16	P5V_S2_PWR_EN_IBOOT
			GPIO23	U17	USB3_PWR_EN
			GPIO24	R14	UWB_PWR_EN
			GPIO25	N10	P2V5_NAND0_DISCHARGE_EN
			GPIO26	P8	FAN_PWR_EN
			GPIO27	P17	NC_MPMU_GPIO27
PMU_ONOFF_L		P10	BUTTON1		
PU_PMU_RSLOC_RST_L		M6	BUTTON2		
NC_MPMU_BUTTON3		N8	BUTTON3		
NC_MPMU_BUTTON4		P11	BUTTON4		
					BUTTONS BUTTON01 N7 NC_MPMU_BUTTON01 <= NOT USED 34
					BUTTON02 N9 NC_MPMU_BUTTON02 <= NOT USED 34
					BUTTON03 M7 NC_MPMU_BUTTON03 <= NOT USED 34
					DBLCLICK_DET N6 DBL_CLICK_DET
SOC_WDOG		N11	RESET_IN1		
PMU_RESET_1V8		M10	RESET_IN2		
SOC_SOCHOT_L		M9	RESET_IN3		
					RESET RESET* N13 PMU_RESET_L 1V2 OUTPUT
		R7	VBUS_DET		FORCE_DFU T10 SOC_FORCE_DFU PMOS OD
VSS_ANA_MPMU		E9	BRICK_ID1		FAULT_OUT* M12 MPMU_FAULT_OUT_L
		E10	BRICK_ID2		SCRASH* N12 PMU_SCRASH_L
		M8	SHDN IPD		SGPIO_READY_REQ M15 PMU_SGPIO_READY_REQ
					SGPIO_SCLK N15 SGPIO_SCLK_R
					SPMI SGPIO_SDATA P15 SGPIO_SDATA_R
					SPMI_SCLK R15 SPMI_NUB_MPMU_CLK
					SPMI_SDATA T15 SPMI_NUB_MPMU_DATA
			NXTAL_MEMS		SLEEP_32K U18 PMU_CLK32K_SOC_R R8331 33 PMU_CLK32K_SOC
			XIN		CLOCKS OUT_32K T16 PMU_CLK32K_WLBT_R R8330 33 PMU_CLK32K_WLBT
			XOUT		
MPMU_AMUX_A<0>		E13	AMUX_A<0>		CRASH* P12 PMU_CRASH_L
MPMU_AMUX_A<1>		F11	AMUX_A<1>		DFT_CTRL0 M16 VSS_ANA_MPMU
MPMU_AMUX_A<2>		E12	AMUX_A<2>		DFT_CTRL1 M17 SWD_NUB_SWCLK
MPMU_AMUX_A<3>		E11	AMUX_A<3>		SYS_ALIVE M11 PMU_SYS_ALIVE
TP_MPMU_AMUX_AY		G12	AMUX_AY		ACTIVE_READY P13 PMU_ACTIVE_READY
NC_MPMU_AMUX_B<0>		E14	AMUX_B<0>		REQUEST_DFU R6 MPMU_REQUEST_DFU
NC_MPMU_AMUX_B<1>		F14	AMUX_B<1>		CPU_TRIGGER0* P6 BUCK0_THERMAL_THROTTLE_L OD
NC_MPMU_AMUX_B<2>		F12	AMUX_B<2>		CPU_TRIGGER1* R9 PMU_VDDHI_UVWARN_L OD
NC_MPMU_AMUX_B<3>		F13	AMUX_B<3>		GPU_TRIGGER0* R8 BUCK1_THERMAL_THROTTLE_L OD
TP_MPMU_AMUX_BY		G11	AMUX_BY		GPU_TRIGGER1* R10 MPMU_GPU_TRIGGER1_L OD
			AMUX		THROTTLE UVWARN* P14 PMU_VDDMAIN_UVWARN_L OD
					VDD_BOOST_UVLO* T17 TP_MPMU_BOOST_UVLO_L OD

VDDMAIN_VREG_THMSNS 42
SOC_THMSNS 42
AMB_COOL1_THMSNS 42
NC_MPMU_TDEV4 42
NC_MPMU_TDEV5 42
WLANBT_THMSNS 42
BKLT_THMSNS 42
MPMU_THMSNS 42
MPMU_TCAL
CRITICAL R8320 3.92K 0.1% 1/20W MF 0201-2
C8320 100PF 5% 25V C0G 0201
VSS_ANA_MPMU 34
PU_IPD_LID_OPEN_1V8 34
NC_CHGR_AUX_OK 34
SWD_NUB_PMU_SWDIO 10 29 67
CODEC_WAKE_L 63 67
WLBT_WAKE 51 52 67
ENET_WAKE_L 34
GPIO6=ENET_WAKE_L ==> DESKTOP
GPIO6=IPD_PWR_EN ==> PORTABLE
GPIO6 NEED PD ON PORTABLES
NC_HDMI_CEC_IRQ 34 <= FOR J274 ONLY
USB3_WAKE_L 46 <= FOR DESKTOPS ONLY
NC_HDMI_RESET_L 34 <= FOR J274 ONLY
P5V_S2_PWR_EN_PWRSEQ 33 GPIO10=P5VS2_PWR_EN ==> DESKTOP
GPIO10=LCD_PWR_EN ==> PORTABLE
P3V3_S2_PWR_EN 33 34
PVDD1_PWR_EN 33 36 67
WLBT_PWR_EN 33 51 52 67
ENET_PWR_EN 33 GPIO14=ENET_PWR_EN ==> DESKTOP
GPIO14=TPAD_XSD_WAKE_L ==> PORTABLE
SE_PWR_EN 33 34
PD_MPMU_GPIO16 33 34
NAND0_LPB_L 53 54 67
BL_PWR_EN 59 HDMI_CECFET_EN==> FOR J274 ONLY
PD_PM_P3V8AON_LPM 26 33 FOR PORTABLES
LCD_PWR_EN 34 GPIO20=LCD_PWR_EN ==>J456/J457
TP_MPMU_NAND0_RESET_L 34 GPIO20=HDMI_PWR_EN ==>J274
P5V_S2_PWR_EN_IBOOT 34 GPIO20=P5VS2_PWR_EN ==>PORTABLE
USB3_PWR_EN 46 <= FOR DESKTOP ONLY
UWB_PWR_EN 34 FOR J456 ONLY (ENABLE UWB LDO)
P2V5_NAND0_DISCHARGE_EN 55 67
FAN_PWR_EN 34 43 67
NC_MPMU_GPIO27 34
NC_MPMU_BUTTON01 <= NOT USED 34
NC_MPMU_BUTTON02 <= NOT USED 34
NC_MPMU_BUTTON03 <= NOT USED 34
DBL_CLICK_DET 7
PMU_RESET_L 6 10 67 68
SOC_FORCE_DFU PMOS OD 6 46 67 68
MPMU_FAULT_OUT_L 33 67
PMU_SCRASH_L 29
PMU_SGPIO_READY_REQ 29 34
SGPIO_SCLK_R 33
SGPIO_SDATA_R 33
SPMI_NUB_MPMU_CLK 20
SPMI_NUB_MPMU_DATA 20
PMU_CLK32K_SOC 10
PMU_CLK32K_WLBT 51 52 67
PLACE_NEAR=U8100.U18:5MM
PLACE_NEAR=U8100.T16:5MM
PMU_CRASH_L 33 67
VSS_ANA_MPMU 32 34
P3V3_S2_PWR_EN 33 36 67
P5V_S2_PWR_EN_PWRSEQ 34
PD_MPMU_GPIO16 33 34
ENET_PWR_EN 33 34
MPMU_REQUEST_DFU 33
PD_PM_P3V8AON_LPM 26 33 34
PVDD1_PWR_EN 33 37 67
MPMU_BOOST_UVLO IS OD. IF NEED TO PROBE OR USE IT , ADD A PU INTERNAL PULL CAN BE ENABLED AS WELL!

R8313 0 1/20W 5% MF 0201
MPMU_XTAL1_R
CRITICAL Y8301 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM
CRITICAL C8312 18PF 5% 25V C0G-CERM 0201
CRITICAL C8313 18PF 5% 25V C0G-CERM 0201
NOSTUFF R8318 1M 5% 1/20W MF 201
MPMU_XOUT 33
MPMU_XIN 33
VSS_ANA_MPMU 32 34
INTERNAL XTAL DRIVER CIRCUIT IS CONNECTED TO CLOSEST VSS PIN N22

NOSTUFF
R8326 100K 5% 1/20W MF 201 WLBT_PWR_EN 33 51 52 67
R8327 100K 5% 1/20W MF 201 NOSTUFF SE_PWR_EN 21 33 67
R8328 100K 5% 1/20W MF 201 NOSTUFF P5V_S2_PWR_EN_PWRSEQ 34
R8329 100K 5% 1/20W MF 201 P3V3_S2_PWR_EN 33 36 67
R8335 100K 5% 1/20W MF 201 PD_MPMU_GPIO16 33 34
R8336 100K 5% 1/20W MF 201 NOSTUFF ENET_PWR_EN 33 34
R8334 10K 5% 1/20W MF 201 MPMU_REQUEST_DFU 33
R8337 100K 5% 1/20W MF 201 PD_PM_P3V8AON_LPM 26 33 34
R8344 100K 5% 1/20W MF 201 NOSTUFF PVDD1_PWR_EN 33 37 67

SGPIO_SCLK_R 33 R8341 20 5% 1/20W MF 201 SGPIO_SCLK 29
PLACE_NEAR=U8100.N15:5MM
SGPIO_SDATA_R 33 R8342 20 5% 1/20W MF 201 SGPIO_SDATA 29
PLACE_NEAR=U8100.P15:5MM

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=sauriah SYNC_DATE=04/27/2020
PAGE TITLE
PMU: MASTER LDO & GPIO

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PP1V2 LDO VDD IN Option (LDO3,8,20)

STUFF R8411 FOR POR (BUCK13), R8422 FOR BUCK14 PRE-REGULATOR.
R8411 & R8422 ARE RATED FOR 20A

NOSTUFF
R8411 0 5% 1/16W MF 0402
116S00014
PP1V25_S2 (70) → PPVDD_PMU_LDO_PREREG (70)

R8422 0 5% 1/16W MF 0402
116S00014
PP1V4_LDO_PREREG (70)

L84E0
0.47UH-20%-4A-0.027OHM
2012
BUCK14_LX (32) — BUCK14_LX (34)
MAKE_BASE=TRUE
DIDT=TRUE
SWITCH_NODE=TRUE

R84E0 0 5% 1/20W MF 0201
PLACE_NEAR=UB100.D14:5MM
BUCK14_FB_MPMU (32) — BUCK14_FB_MPMU — BUCK14_FB_R
MAKE_BASE=TRUE

XW84E0
SHORT-14L-0.1MM-SM
NO_XNET_CONNECTION=1

PP1V4_LDO_PREREG (70)
PLACE_NEAR=L84E0.1:5MM
CRITICAL C84E0 15UF 20% 2V X6S 0402
CRITICAL C84E1 15UF 20% 2V X6S 0402
CRITICAL C84E2 15UF 20% 2V X6S 0402
CRITICAL C84E3 15UF 20% 2V X6S 0402
CRITICAL C84E4 15UF 20% 2V X6S 0402
CRITICAL C84E5 15UF 20% 2V X6S 0402
C84EA 12PF 5% 25V NP0-C0G 0201
PLACE_NEAR=L84E0.1:5MM
C84EB 3PF +/-0.1PF 25V C0G 0201

MASTER PMU SIGNALS

NC_MPMU_LDO1_EN (33) — NC_MPMU_LDO1_EN
NC_MPMU_BUTTON3 (33) — NC_MPMU_BUTTON3
NC_MPMU_BUTTON4 (33) — NC_MPMU_BUTTON4
NC_MPMU_BUTTONO1 (33) — NC_MPMU_BUTTONO1
NC_MPMU_BUTTONO2 (33) — NC_MPMU_BUTTONO2
NC_MPMU_BUTTONO3 (33) — NC_MPMU_BUTTONO3
GPIO7 NC_HDMI_CEC_IRQ (33) — NC_HDMI_CEC_IRQ
GPIO9 NC_HDMI_RESET_L (33) — NC_HDMI_RESET_L
GPIO21 TP_MPMU_NAND0_RESET_L (33) — TP_MPMU_NAND0_RESET_L
P5V_S2_PWR_EN_PWRSEQ (33) — P5V_S2_PWR_EN_PWRSEQ (35) (67)
ENET_PWR_EN (33) — ENET_PWR_EN (50) (67)
LCD_PWR_EN (33) — LCD_PWR_EN (57) (67)
NO_TEST=1, MAKE_BASE=TRUE

GPIO27 NC_MPMU_GPIO27 (33) — NC_MPMU_GPIO27
GPIO6 ENET_WAKE_L (33) — ENET_WAKE_L (48) (67)
MPMU_GPU_TRIGGER1_L (33) — R8433 0 5% 1/20W MF 0201 — P15V8AON_ILIMIT_L (20)
GPIO1 PU_IPD_LID_OPEN_1V8 (33) (34) — PU_IPD_LID_OPEN_1V8
MAKE_BASE=TRUE

PP2V5_S2 (34) (33)
NOSTUFF
CRITICAL C8420 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8421 10UF 20% 6.3V CER-X6S 0402

FROM 2MS PCC CIRCUIT
PMU_VDDHI_UVWARN_L (34) (33) IN — R8444 0 5% 1/20W MF 0201 — P15V8_AON_PRE_UPO_L — TO SOC (7) (34) OUT
P15V8_AON_PRE_UPO_L
MAKE_BASE=TRUE

FROM SERA
PD_PM_P3V8AON_LPM (33) (26) IN — PD_PM_P3V8AON_LPM
NC_CHGR_AUX_OK (33) IN — NC_CHGR_AUX_OK
PD_MPMU_GPIO16 (33) IN — PD_MPMU_GPIO16
PU_PMU_RSLOC_RST_L (33) IN — PU_PMU_RSLOC_RST_L (67)
PP2V5_S2 (34) (33) IN — PP2V5_S2 (70) OUT
MAKE_BASE=TRUE, NO_TEST=1

PP8412 P4MM SM PP — BUCK1_LX2 (31) IN
PP8413 P4MM SM PP — BUCK1_LX3 (31) IN
PP8414 P4MM SM PP — BUCK1_LX4 (31) IN
PP8420 P4MM SM PP — BUCK2_LX0 (31) IN
PP8421 P4MM SM PP — BUCK2_LX1 (31) IN
PP8422 P4MM SM PP — BUCK2_LX2 (31) IN
PP8430 P4MM SM PP — BUCK3_LX0 (32) IN
PP8406 P4MM SM PP — BUCK0_LX0 (31) IN
PP8407 P4MM SM PP — BUCK0_LX1 (31) IN
PP8408 P4MM SM PP — BUCK0_LX2 (31) IN
PP8409 P4MM SM PP — BUCK0_LX3 (31) IN
PP840A P4MM SM PP — BUCK0_LX4 (31) IN
PP8410 P4MM SM PP — BUCK1_LX0 (31) IN
PP8411 P4MM SM PP — BUCK1_LX1 (31) IN

PP8470 P4MM SM PP — BUCK7_LX0 (32) IN
PP8471 P4MM SM PP — BUCK7_LX1 (32) IN
PP8480 P4MM SM PP — BUCK8_LX0 (32) IN
PP8481 P4MM SM PP — BUCK8_LX1 (32) IN
PP8490 P4MM SM PP — BUCK9_LX0 (32) IN
PP84B0 P4MM SM PP — BUCK11_LX0 (32) IN
PP84B1 P4MM SM PP — BUCK11_LX1 (32) IN
PP84E0 P4MM SM PP — BUCK14_LX (34)

UWB_PWR_EN (33)
FAN_PWR_EN (67) (43) (33)
MPMU_VBAT (32) OUT
MPMU_ADC_IN (32) OUT
MPMU_IBAT (32) OUT
PLACE_NEAR=U8100.K9:5MM
PMU_RESET_1V8 (67) (46) (33) OUT
P5V_S2_PWR_EN_IBOOT (35) (33)
NOSTUFF R8407 100K 5% 1/20W MF 201
R8412 100K 5% 1/20W MF 201
R8404 1M 5% 1/20W MF 201
R8403 1M 5% 1/20W MF 201
R8402 1M 5% 1/20W MF 201
NOSTUFF R8405 100K 5% 1/20W MF 201
NOSTUFF R8406 100K 5% 1/20W MF 201

SERA UNUSED LDO

NC_MPMU_VLDO5 — NC_MPMU_VLDO5 (33)
NC_MPMU_VLDO10 — NC_MPMU_VLDO10 (33)
NC_MPMU_VLDO13 — NC_MPMU_VLDO13 (33)
NC_MPMU_VLDO14 — NC_MPMU_VLDO14 (33)
NC_MPMU_VLDO16 — NC_MPMU_VLDO16 (33)
NO_TEST, MAKE_BASE=TRUE

PP1V8_AON (70) (33) (29)
R8410 100K 5% 1/20W MF 201
R8418 100K 5% 1/20W MF 201
TP_MPMU_BOOST_UVLO_L (33)
PU_IPD_LID_OPEN_1V8 (34) (33)

PP8405 P4MM SM PP
PMU_SGPIO_READY_REQ (33) (29) IN

MASTER PMU AMUX ALIAS

NC_MPMU_AMUX_B<0..3> — NC_MPMU_AMUX_B<0..3> (33) OUT
MAKE_BASE=TRUE, NO_TEST=1
TP_MPMU_AMUX_AY (33) — TP_MPMU_AMUX_AY
TP_MPMU_AMUX_BY (33) — TP_MPMU_AMUX_BY
MAKE_BASE=TRUE

VSS alias connection

OF XW IS LAYOUT DEPENDENT

VSS_ANA_MPMU (32) (31) — VSS_ANA_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
VOLTAGE=0
GND_MPMU_AMUX (41) (46) — XW8410 SHORT-8L-0.25MM-SM

XW8401 XW8402 XW8403 XW8404
SHORT-12L-0.1MM-SM

NOSTUFF R8445 0 5% 1/20W MF 0201
P15V8_AON_ILIMIT_L (67) (25) — P15V8AON_ILIMIT_L (7) (20) (34)
FROM FAST PCC CIRCUIT
R8446 0 5% 1/20W MF 0201
P15V8_AON_PRE_UPO_L (7) (34)
P15V8_AON_PRE_UPO_L (67) (25) — NOSTUFF R8447 0 5% 1/20W MF 0201 — P15V8_AON_PRE_UPO_L (7) (34)
FROM 2MS PCC CIRCUIT
R8448 0 5% 1/20W MF 0201 — P15V8AON_ILIMIT_L (7) (20) (34)

GND (32) ×8
MAKE_BASE=TRUE
BOM_COST_GROUP=PLATFORM POWER

PP1V2_AWAKE_IO (70) (63) (62) (56) (25)
R8450 10K 5% 1/20W MF 201 — BUCK0_THERMAL_THROTTLE_L (7) (33)
NOSTUFF R8451 10K 5% 1/20W MF 201 — PMU_VDDHI_UVWARN_L (33) (34)
R8452 10K 5% 1/20W MF 201 — BUCK1_THERMAL_THROTTLE_L (7) (33)
R8454 10K 5% 1/20W MF 201 — PMU_VDDMAIN_UVWARN_L (7) (33)

ADDITIONAL VDD_MAIN DECOUPLING CAPS

PP3V8_AON_VDDMAIN_MPMU (71) (41) (34) (33) (31)
C84C0 C84C1 C84C2 C84C3 C84C4 C84C5 C84C6 C84C7 1UF 20% 10V X6S-CERM 0201

PP3V8_AON_VDDMAIN_MPMU (71) (41) (34) (33) (31)
C84C8 C84C9 C84CA C84CB C84CC C84CD C84CE 1UF 20% 10V X6S-CERM 0201

PPVDD_SOC_S1 (70) (13)
C8401 C8402 C8403 C8404 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=L8121.3:5MM

GPU RAIL N&V DOE CAPS

PPVDD_GPU_AWAKE (70) (31)
C8410 C8411 C8412 C8413 C8414 C8415 15UF 20% 2V X6S 0402
PLACE_SIDE=BOTTOM

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PP5V_S2_SYS_REG

PPBUS_AON

CRITICAL
CC321
22UF
20%
25V
POLY-TANT
CASED2-SM
128S0385

25V PBUS CAP

128s0217 / 128S0385
22uF 25V 60mohm 2Arms

CRITICAL
CC312
2.2UF
20%
25V
X6S-CERM
0402
138S00042

CRITICAL
CC313
2.2UF
20%
25V
X6S-CERM
0402
138S00042

CRITICAL
353S02228
UC310
SN621371
VQFN

1	VIN	SW	2
8	EN	VOS	6
9	SS/TR	FB	5
11	VSEL	PG	7
10	MODE	FB2	4
	GND		3

MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
DUOTRUE
SWITCH_NODE=TRUE

CRITICAL
152S00476
LC310
1.5UH-20%-3.9A-0.048OHM
1210

P5V_S2_SYS_SW

RC314
0
5%
1/20W
MF
0201
117S0201

IN P5V_S2_PWR_EN_PWRSEQ
MPMU GPIO10
1V8 PUSH/PULL

RC341
0
5%
1/20W
MF
0201
117S0201
NOSTUFF

IN P5V_S2_PWR_EN_IBOOT
MPMU GPIO22
1V8 PUSH/PULL
MAKE_BASE=TRUE

P5V_S2_SYS_EN
P5V_S2_SYS_SS

CC314
4700PF
10%
16V
X7R
201
132S0187

XWC310
SM
OMIT

300us max Start-Up Delay
1.32ms typ with CC314 = 4.7nF
tss = CC3314 * 0.7V / 2.5uA

P5V_S2_SYS_VOS
P5V_S2_SYS_FB
PU_P5V_S2_SYS_PGOOD
OUT

RC390
10K
5%
1/20W
MF
201
117S0007

XWC311
SM
OMIT

P5V_S2_SYS_OS_XW

RC309
15
5%
1/20W
MF
201
117S0030

P5V_S2_SYS_FB_LPF

CC319
0.1UF
10%
16V
CER
0201
132S00048

RC310
0
5%
1/20W
MF
0201
117S0201

CC320
150PF
5%
50V
CER-C0G
0201
131S00142

RC312
61.9K
1%
1/20W
MF
201
118S0465

VFB : 0.70V +/- 1%

RC313
10K
0.1%
1/20W
MF
0201-1
103S00092

P5V_S2_SYS_AGND

PP5V0_S2

CRITICAL
CC315
150UF
20%
6.3V
TANT
CASE-B-SM
128S00038

CRITICAL
CC317
10UF
20%
6.3V
CER-X6S
0402
138S00073

CRITICAL
CC318
10UF
20%
6.3V
CER-X6S
0402
138S00073

128s00038
150uF 6.3V 18mohm 2Arms

PP5V_S2_SYS

VOUT	5V03 +/- 1.3%
ICCMAX	2A
ITDC	1A
OCP	3.5A MIN 4.5A TYP
FSW	1500kHz

BOM_COST_GROUP=PLATFORM POWER

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* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=3V3_S2_PBUS-B12
PACK_OPTION=3V3_S2_PBUS-D2
PACK_OPTION=3V3_S2_PBUS-D12
PACK_OPTION=3V3_S2_PBUS-25V_D2

START UP TIME <5 MS

71 PPBUS_AON

CAPDERATE POLY-TANT CRITICAL
CC710 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE POLY-TANT CRITICAL
CC711 33UF 20% 16V TANT CASE-T 128S00009
PACK_IGNORE=TRUE
PACK_OPTION=3V3_S2_PBUS-B12

CAPDERATE POLY-TANT CRITICAL
CC721 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264
PACK_IGNORE=TRUE
PACK_OPTION=3V3_S2_PBUS-D2

CAPDERATE POLY-TANT CRITICAL
CC722 33UF 20% 16V TANT CASED12-SM 128S0436
PACK_IGNORE=TRUE
PACK_OPTION=3V3_S2_PBUS-D12

CRITICAL
CC723 22UF 20% 25V POLY-TANT CASED2-SM 128S0385
PACK_OPTION=3V3_S2_PBUS-25V_D2

25V PBUS CAP

128s0217 / 128S0385
22uF 25V 60mohm 2Arms

CRITICAL
CC712 2.2UF 20% 50V X6S-CERM 0402 138S00042
CRITICAL
CC713 2.2UF 20% 50V X6S-CERM 0402 138S00042

67 33 EN
P3V3_S2_PWR_EN
MPMU GPIO11
1V8 PUSH/PULL

RC714 0 5% 1/20W MF 0201 117S0201
67 P3V3_S2_EN

P3V3_S2_SS

CC714 0.01UF 10% 16V X7R-CERM 0201 132S0411

300us max Start-Up Delay
2.8ms typ with CC714 = 10nF
tss = CC714 * 0.7V / 2.5uA

XWC710 SM

UC710 SN621371 VQFN 353S02228 CRITICAL

1	VIN	SW	2
8	EN	VOS	6
9	SS/TR	FB	5
11	VSEL	PG	7
10	MODE	FB2	4
	GND		

MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
DIDT=TRUE
SWITCH_NODE=TRUE

P3V3_S2_SW
P3V3_S2_VOS
P3V3_S2_FB
P3V3_S2_PGOOD
36 67 OUT

CRITICAL
LC710 1.5UH-20%-3.9A-0.048OHM 1210 152S00476

XWC711 SM
P3V3_S2_OS_XW

RC709 15 5% 1/20W MF 201 117S0030
P3V3_S2_FB_LPF
CC719 0.1UF 10% 16V CER 0201 132S00048

RC710 0 5% 1/20W MF 0201 117S0201

RC711 2.26K 1% 1/20W MF 0201 118S0204
P3V3_S2_FB_R

CC720 150PF 5% 50V CER-C0G 0201 131S00142

CRITICAL
RC712 127K 0.1% 1/20W MF 0201 103S0442

CRITICAL
RC713 34.8K 0.1% 1/20W MF 0201-1 103S00058

P3V3_S2_AGND

VOUT=3.3V
EDC=2.5A
TDC=2.0A
F=1.5MHz

POLY-TANT CRITICAL
CC715 150UF 20% 6.3V TANT CASE-B-SM 128S00038
CRITICAL
CC717 10UF 20% 6.3V CER-X6S 0402 138S00073
CRITICAL
CC718 10UF 20% 6.3V CER-X6S 0402 138S00073
PP3V3_S2 36 71

128s00038
150uF 6.3V 18mohm 2Arms

PP3V3_S2 36 71
RC790 10K 5% 1/20W MF 201 117S0007
PGOOD PullUP Resistor
P3V3_S2_PGOOD 36 67

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=vincent SYNC_DATE=05/16/2020
PAGE TITLE
POWER: 3V3 S2

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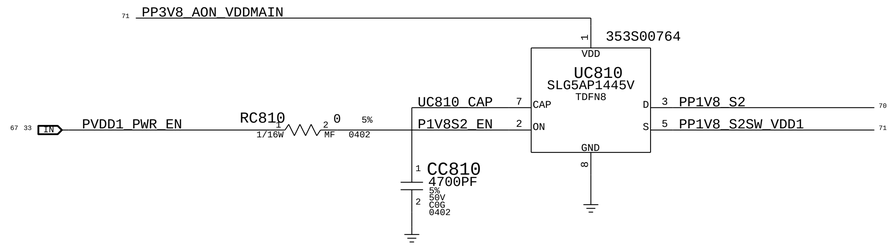
1V8 S2 EXTERNAL SOC DRAM SWITCH



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=vincent SYNC_DATE=10/18/2019

PAGE TITLE
POWER: Misc LDOs and FETs

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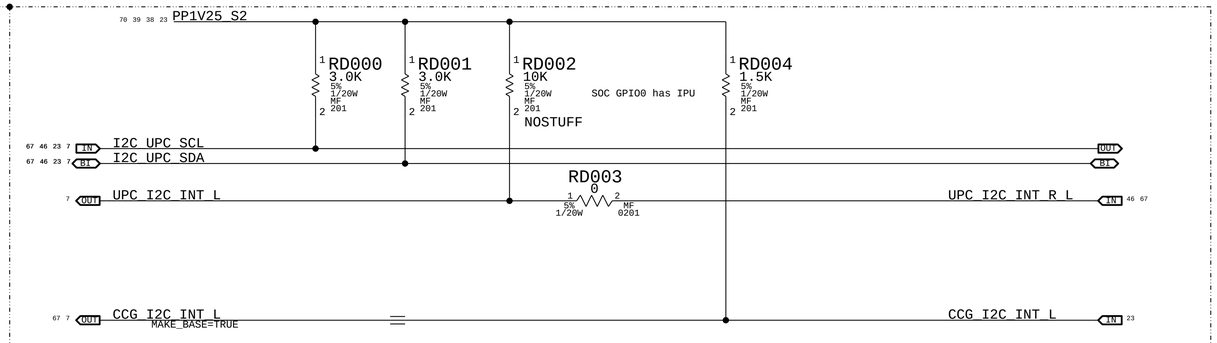
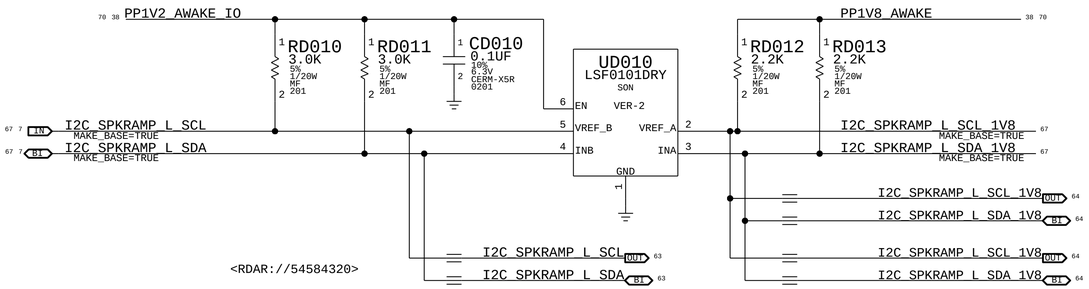
AP_I2C0

DEVICE	8-BIT	7-BIT
Ace2 All-Call	0xD6	0x6B
Ace2 ATC0 (debug)	0x70	0x38
Ace2 ATC1	0x7E	0x3F
Ace2 ATC2	0x76	0x3B
Ace2 ATC3	0x78	0x3C
CCG3 Pwr mgmt	TBD	TBD
Ace Bridge Arkanoid conn	0x??	
Ace Aardvark Arkanoid conn	0x??	



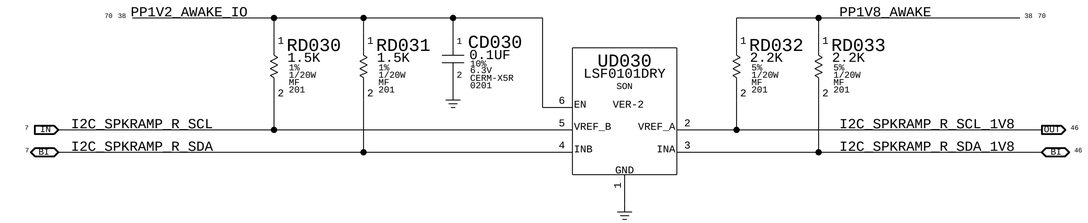
AP_I2C1

DEVICE	8-BIT	7-BIT
Left SpkrAmp A	0X28	0X14
Left SpkrAmp B	0X2A	0X15
CODEC	0X90	0X48



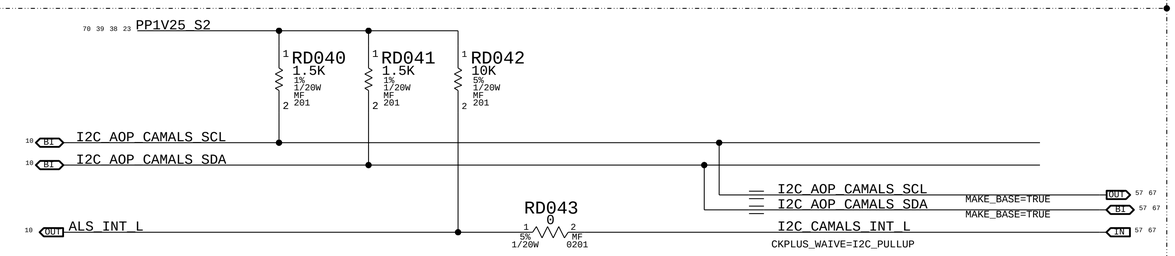
AP_I2C3

DEVICE	8-BIT	7-BIT
Right SpkrAmp A	0X28	0X14
Right SpkrAmp B	0X2A	0X15



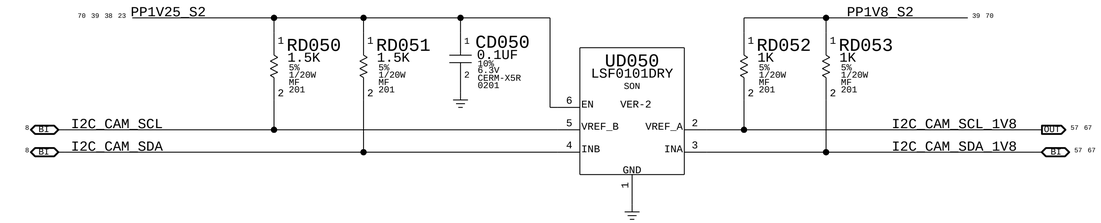
AOP_I2C0

DEVICE	8-BIT	7-BIT
ALS	0X52	0X29



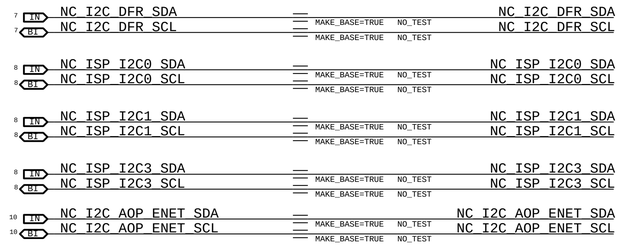
ISP_I2C2

DEVICE	8-BIT	7-BIT
Camera	0X40	0X20
Camera PMU	0X48	0X24
Camera PMU OTP	0X58	0X2C



Unused

AP_I2C2 (unused)
AP_I2C4 (DFR unused)
ISP_I2C0 (Unused image processor port)
ISP_I2C1 (Unused image processor port)
ISP_I2C3 (Unused image processor port)
AOP_I2CM1 (Unused enet I2C port)



BOM_COST_GROUP=SMC

PAGE TITLE
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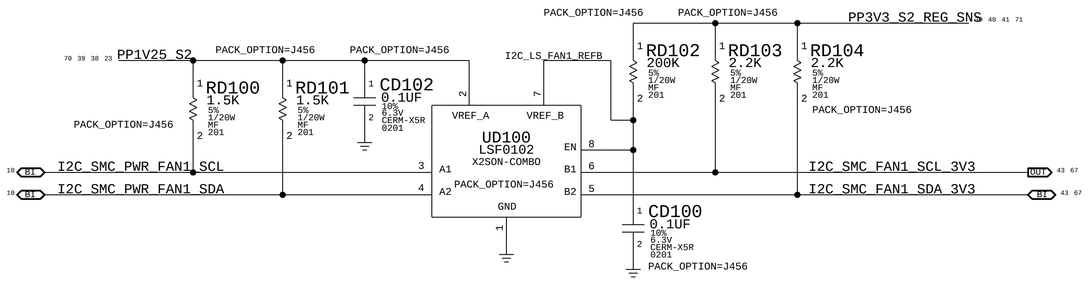
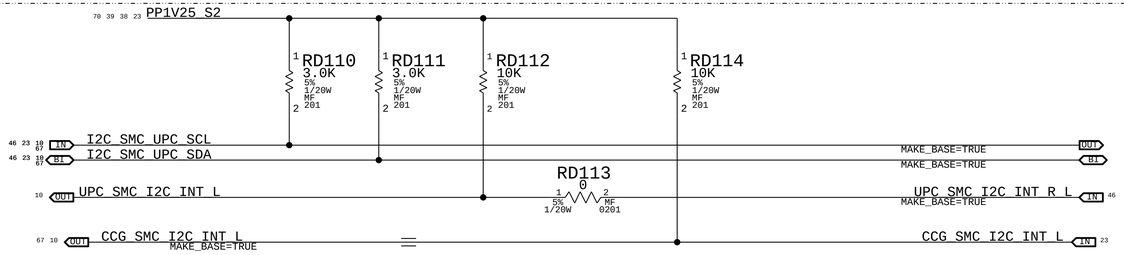
SMC_I2C0

DEVICE	8-BIT	7-BIT
Fan Ctlr 1	0XA4	0X52



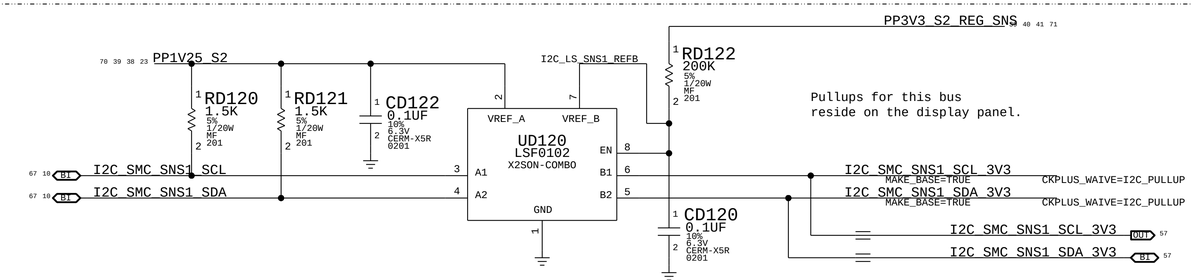
SMC_I2C1

DEVICE	8-BIT	7-BIT
TBD	0x6E	0x37
Ace2 ATC0 (debug)	0x70	0x38
Ace2 ATC1 (?)	0x7E	0x3F
Ace2 ATC2	0x76	0x3B
Ace2 ATC3	0x78	0x3C
TBD	0xD4	0x6A
Ace2 All-Call	0xD6	0x6B
Ace Bridge Arkanoid conn	0x??	



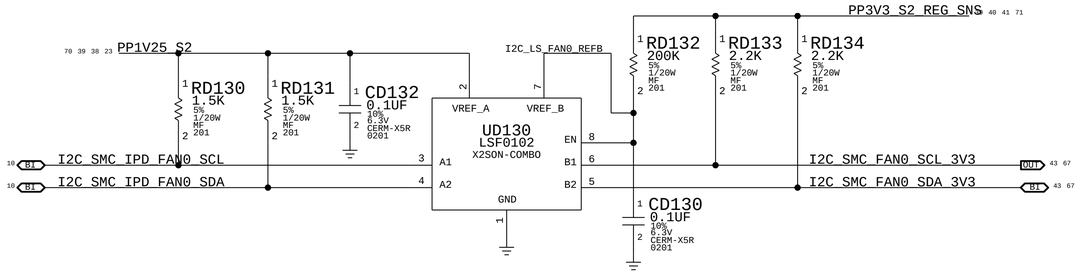
SMC_I2C2

DEVICE	8-BIT	7-BIT
SLG46826	0x10,0x12,0x14,0x16	
TMP468	0x90 (Disp temp sns ch1-6)	
Digital Pot	0xA2	



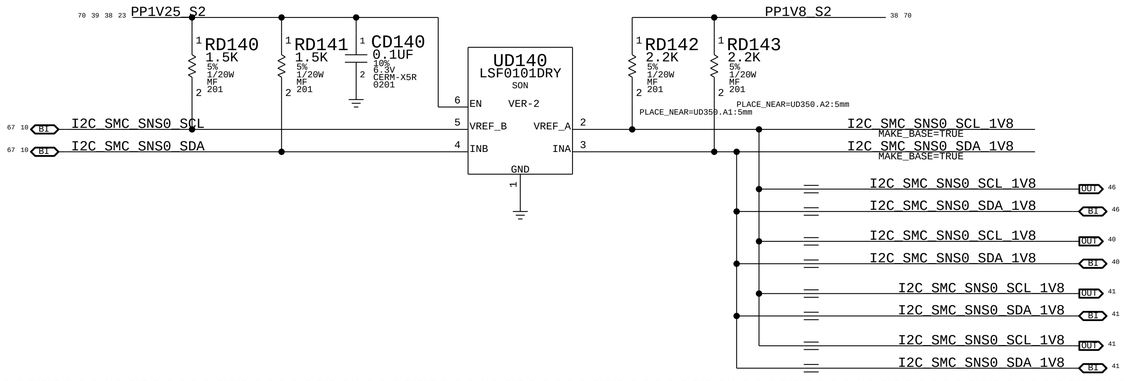
SMC_I2C3

DEVICE	8-BIT	7-BIT
Fan Ctlr 0	0XA4	0X52



SMC_I2C4

DEVICE	8-BIT	7-BIT
USB brd temp sensors	0x92	0x49
USB port power sensor	0x80	0x40
Rt spkramps I/V sensors	0x82	0x41
PP3V8AON power sensor	0x8A	0x45
MPMU high side pwr sns	0x84	0x42
SPMU high side pwr sns	0x88	0x44



PAGE TITLE

I2C Connections 2

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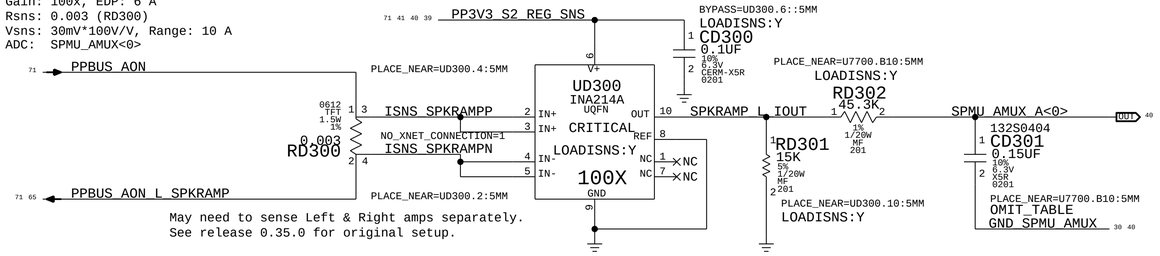
Left Audio Amps current sensing (IALR)

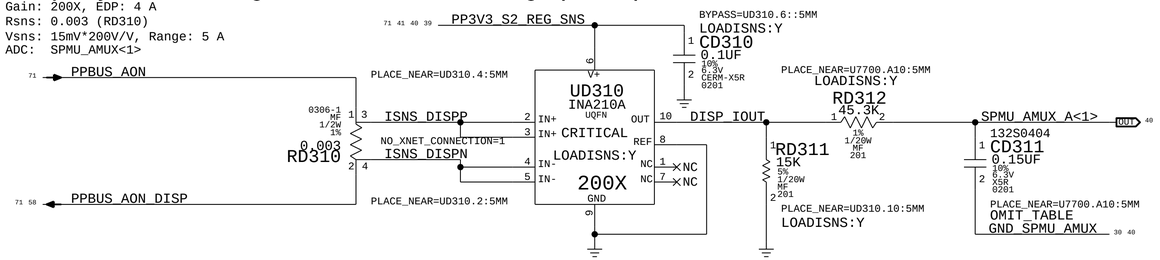
Gain: 100x, EDP: 6 A
Rsns: 0.003 (RD300)
Vsns: 30mV*100V/V, Range: 10 A
ADC: SPMU_AMUX<0>



May need to sense Left & Right amps separately.
See release 0.35.0 for original setup.

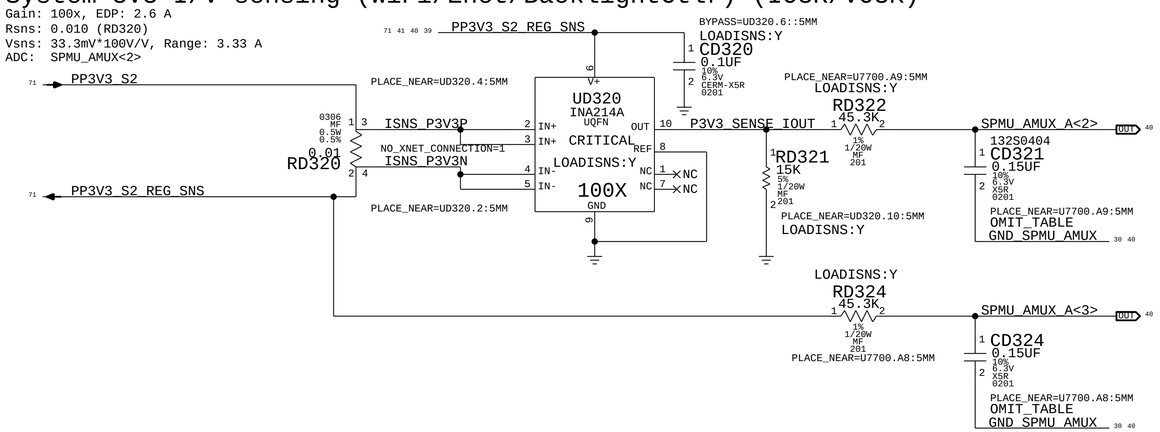
Display & Backlight current sensing (IBLR)

Gain: 200X, EDP: 4 A
Rsns: 0.003 (RD310)
Vsns: 15mV*200V/V, Range: 5 A
ADC: SPMU_AMUX<1>



System 3V3 I/V sensing (WiFi/Enet/BacklightCtlr) (IO3R/VO3R)

Gain: 100x, EDP: 2.6 A
Rsns: 0.010 (RD320)
Vsns: 33.3mV*100V/V, Range: 3.33 A
ADC: SPMU_AMUX<2>



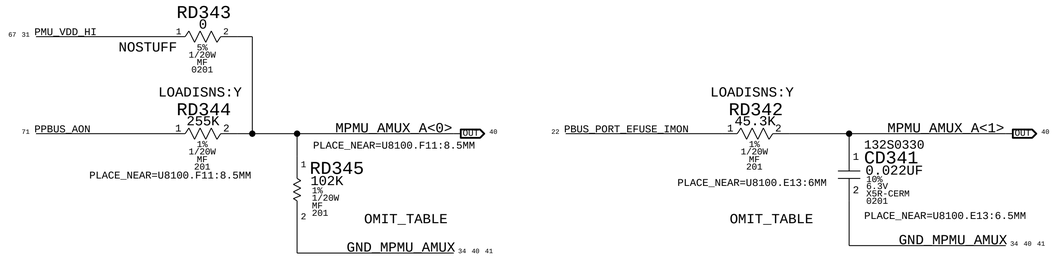
Make cap in RC filter
that feeds ADC a
short if sensor is not used

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	CD301,CD311,CD321,CD324		LOADISNS:N
138S0831	4	CAP,CER,X5R,2.2UF,20%,6.3V,0201	CD301,CD311,CD321,CD324		LOADISNS:Y

INA21X PARTS HAVE MINOR LEAKAGE PATH FROM INPUTS TO OUTPUT WHEN UNPOWERED.
PULL-DOWN RESISTERS ON INA OUTPUTS BLEED OFF THE LEAKAGE CURRENT TO PREVENT
SIGNAL PUMP-UP.

PSU input I/V & Predictive Throtling sensing (ID0R/VD0R)

EDP: 9 A (10A??)
Isns: Vadc = 246uA/A * I * R5156, Range: 14.7A,max for R5156=649ohms
Vsns: Vadc = PPVBUS * RD345 / (RD345 + RD344) = 4.514V nom for 15.8V input
ADC: MPMU_AMUX<0> voltage, MPMU_AMUX<1> current

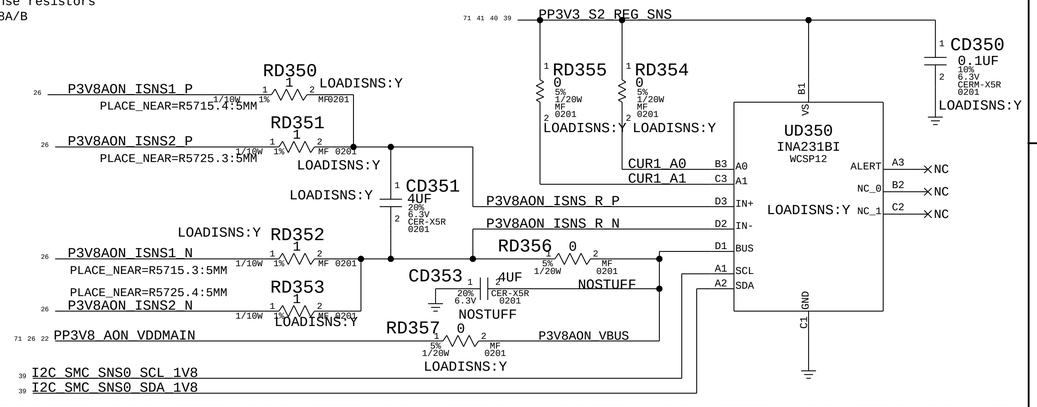


Short input to ADC
if sensor not used

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	RD345		LOADISNS:N
118S0020	1	RES,MF,102KOHM,1,1/20W,0201	RD345		LOADISNS:Y
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	CD341		LOADISNS:N
138S0831	1	CAP,CER,X5R,2.2UF,20%,6.3V,0201	CD341		LOADISNS:Y

PPVCC_MAIN Vreg output current measurement (IMVC/VMVR)

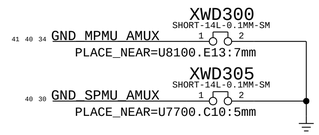
Uses Vreg's existing sense resistors
Bus: SMC I2C2, Addr: 0x8A/B



I2C Write = 0X8A
I2C Read = 0X8B

AMUX input aliases

SPMU_AMUX_A<0> = SPMU_AMUX_A<0> (MAKE_BASE=TRUE)
SPMU_AMUX_A<1> = SPMU_AMUX_A<1> (MAKE_BASE=TRUE)
SPMU_AMUX_A<2> = SPMU_AMUX_A<2> (MAKE_BASE=TRUE)
SPMU_AMUX_A<3> = SPMU_AMUX_A<3> (MAKE_BASE=TRUE)
MPMU_AMUX_A<0> = MPMU_AMUX_A<0> (MAKE_BASE=TRUE)
MPMU_AMUX_A<1> = MPMU_AMUX_A<1> (MAKE_BASE=TRUE)
MPMU_AMUX_A<2> = MPMU_AMUX_A<2> (MAKE_BASE=TRUE)
MPMU_AMUX_A<3> = MPMU_AMUX_A<3> (MAKE_BASE=TRUE)

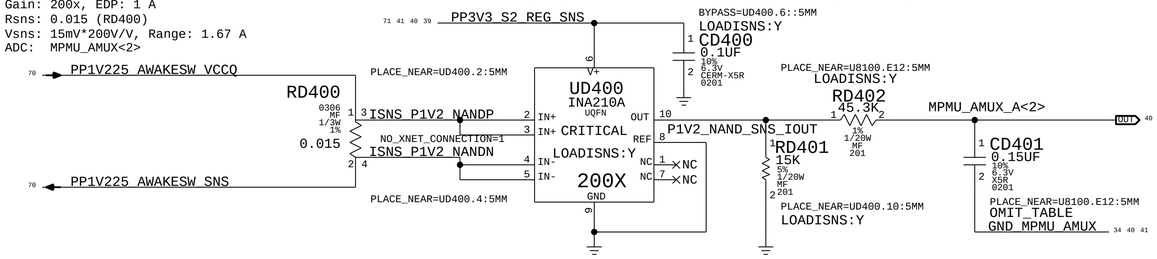


BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors (1)
Apple Inc.
DRAWING NUMBER: 051-05371
SIZE: D
REVISION: 6.0.0
BRANCH:
PAGE: 133 OF 700
SHEET: 40 OF 77

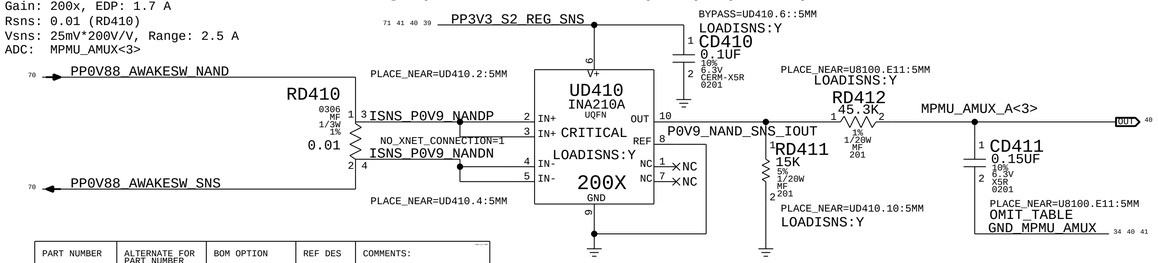
NAND PP1V25_AWAKESW current sensing (Buck SW5 output) (IM1C)

Gain: 200x, EDP: 1 A
Rsns: 0.015 (RD400)
Vsns: 15mV*200V/V, Range: 1.67 A
ADC: MPMU_AMUX<2>



NAND PP0V9 current sensing (Buck SW6+7 output) (IM0C)

Gain: 200x, EDP: 1.7 A
Rsns: 0.01 (RD410)
Vsns: 25mV*200V/V, Range: 2.5 A
ADC: MPMU_AMUX<3>



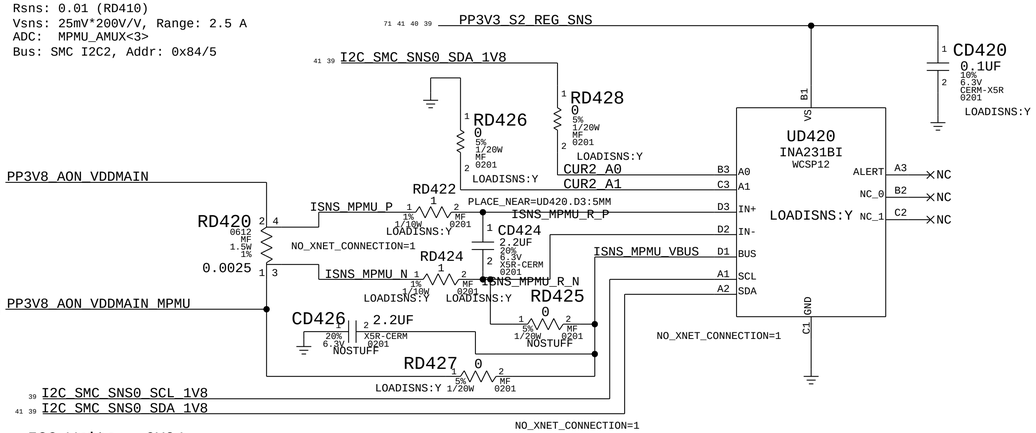
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0276	107S00020		RD410	

Power sensors on USB Adapter board

Location	I2C bus/addr	SMC key
USBC 5V current	SMC I2C2/0x80	IU5C
USBC 5V voltage	SMC I2C2/0x80	VU5C
Right Spkr Amp current	SMC I2C2/0x82	IAPR
Right Spkr Amp voltage	SMC I2C2/0x82	VAPR

MPMU high side I/V sensing (IPMR/VPMR)

Gain: 200x, EDP: 1.7 A
Rsns: 0.01 (RD410)
Vsns: 25mV*200V/V, Range: 2.5 A
ADC: MPMU_AMUX<3>
Bus: SMC I2C2, Addr: 0x84/5



I2C Write = 0X84
I2C Read = 0X85
(A0=SDA, A1=Gnd)

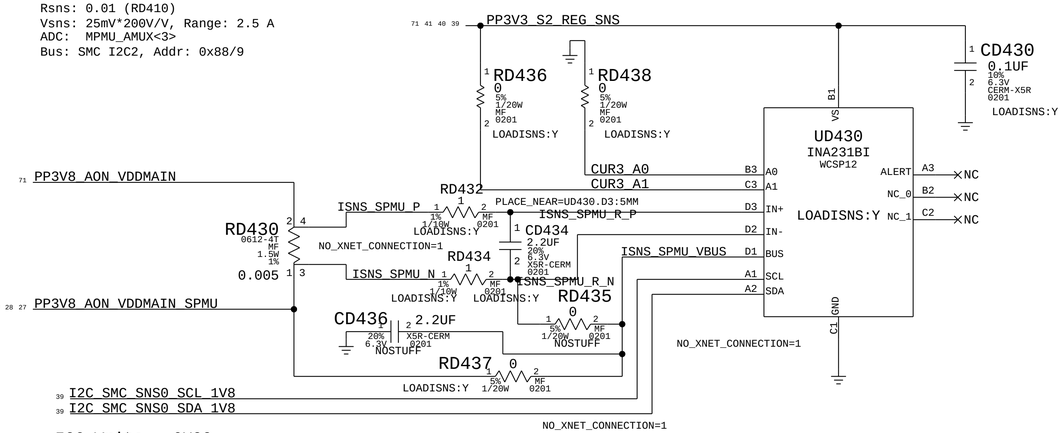
Make cap in RC filter
that feeds ADC a
short if sensor is not used

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	2	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	CD401,CD411		LOADISNS:N
138S0831	2	CAP,CER,X5R,2.2UF,20%,6.3V,0201	CD401,CD411		LOADISNS:Y

INA21X PARTS HAVE MINOR LEAKAGE PATH FROM INPUTS TO OUTPUT WHEN UNPOWERED.
PULL-DOWN RESISTERS ON INA OUTPUTS BLEED OFF THE LEAKAGE CURRENT TO PREVENT
SIGNAL PUMP-UP.

SPMU high side I/V sensing (IPSR/VPSR)

Gain: 200x, EDP: 1.7 A
Rsns: 0.01 (RD410)
Vsns: 25mV*200V/V, Range: 2.5 A
ADC: MPMU_AMUX<3>
Bus: SMC I2C2, Addr: 0x88/9



I2C Write = 0X88
I2C Read = 0X89
(A0=Gnd, A1=Vs)

BOM_COST_GROUP=SENSORS

DESIGN: T585/TGA_140
LAST CHANGE: Thu Dec 20 16:56:50 2018

PAGE TITLE
Power Sensors (2)

Apple Inc.

DRAWING NUMBER 051-05371 SIZE D
REVISION 6.0.0
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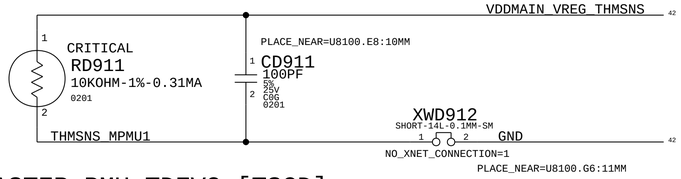
THERMAL SENSORS

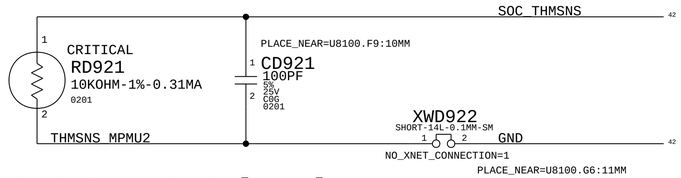
MASTER PMU TDEV1 [TMVR]

LOCATION: U5710 & U5721, FETs in 3.8V AON VR Vreg



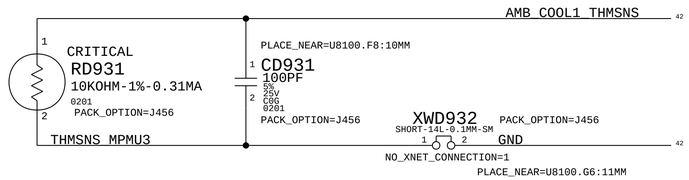
MASTER PMU TDEV2 [TSCD]

LOCATION: SOC proximity



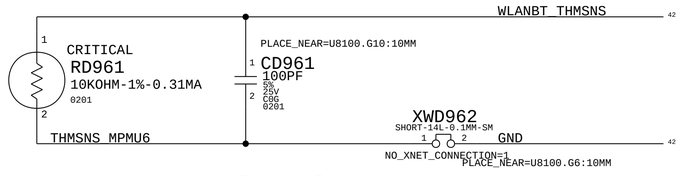
MASTER PMU TDEV3 [Txxx]

LOCATION: Left side MLB air intake (near Fan1)



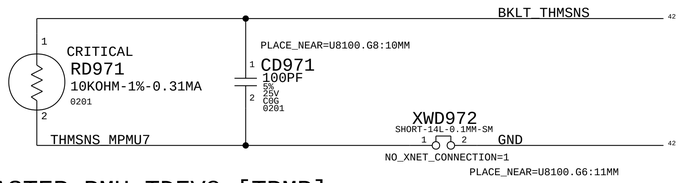
MASTER PMU TDEV6 [TW0P]

LOCATION: WLANBT, back side



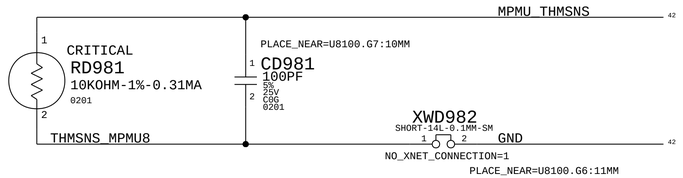
MASTER PMU TDEV7 [Tb0P]

LOCATION: Backlight Ctlr proximity



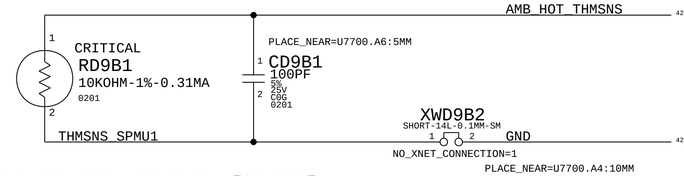
MASTER PMU TDEV8 [TPMP]

LOCATION: MPMU proximity



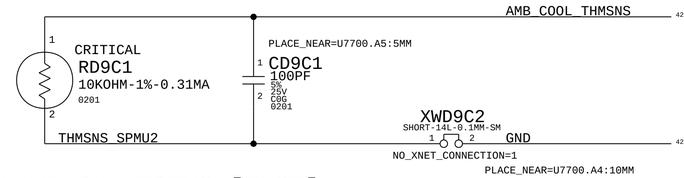
SLAVE PMU TDEV1 [TmhP]

LOCATION: MLB maximally hot location



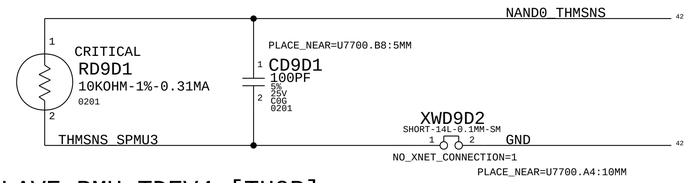
SLAVE PMU TDEV2 [TaMP]

LOCATION: Right side MLB air intake (near Fan0)



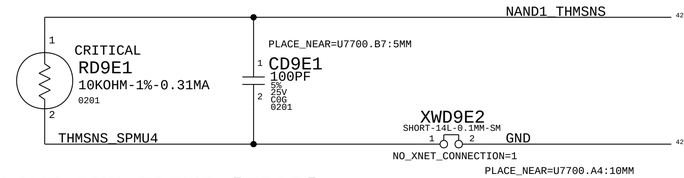
SLAVE PMU TDEV3 [TH0T]

LOCATION: NAND proximity, top side



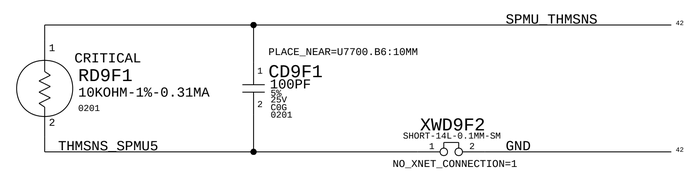
SLAVE PMU TDEV4 [TH0B]

LOCATION: NAND proximity, bottom side



SLAVE PMU TDEV5 [TPSP]

LOCATION: SPMU proximity

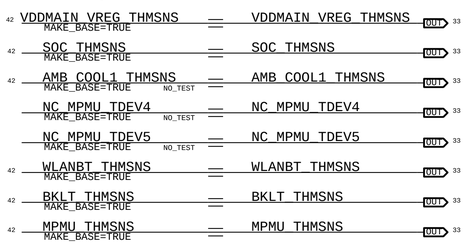


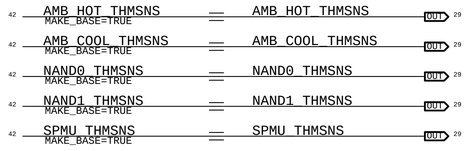
Thermal sensors on USB Adapter board

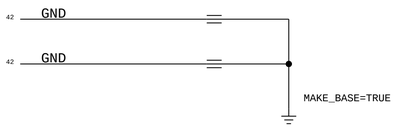
Location	Channel	SMC key
TMP464 local	Local	TIOP
Left Port ACE die	D1	TT0D
LeftMiddle Port ACE die	D2	TT1D
USB Adapt Bd ambient	D3	TPSD
USBC 5V Vreg prox	D4	T5VP

All USB Adapter board sensors
are on SMC I2C2 bus @ 0x90/1

TDEV input alias







BOM_COST_GROUP=SENSORS

PAGE TITLE
Temperature Sensors

Apple Inc.

DRAWING NUMBER 051-05371
SIZE D
REVISION 6.0.0
BRANCH
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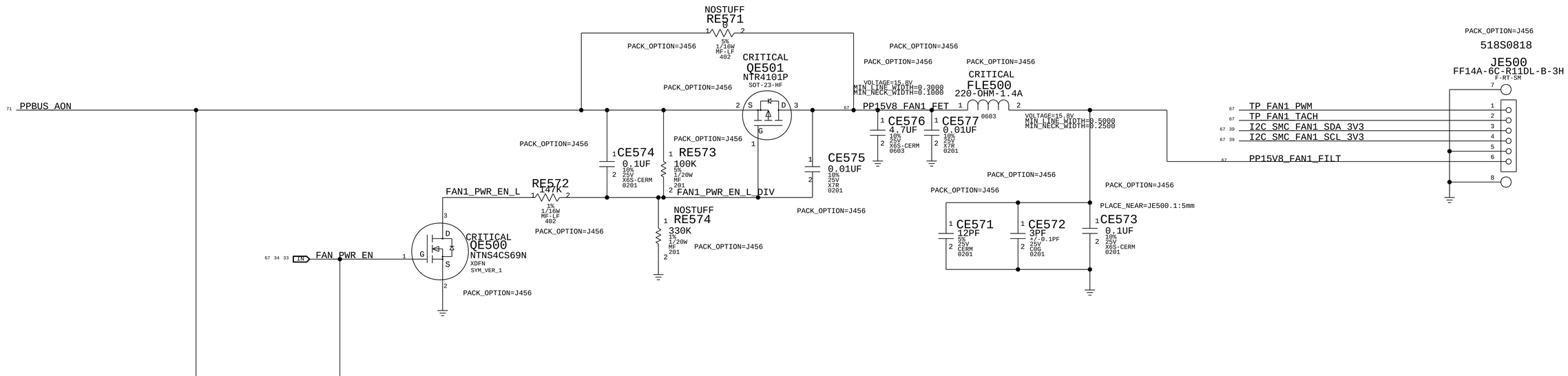
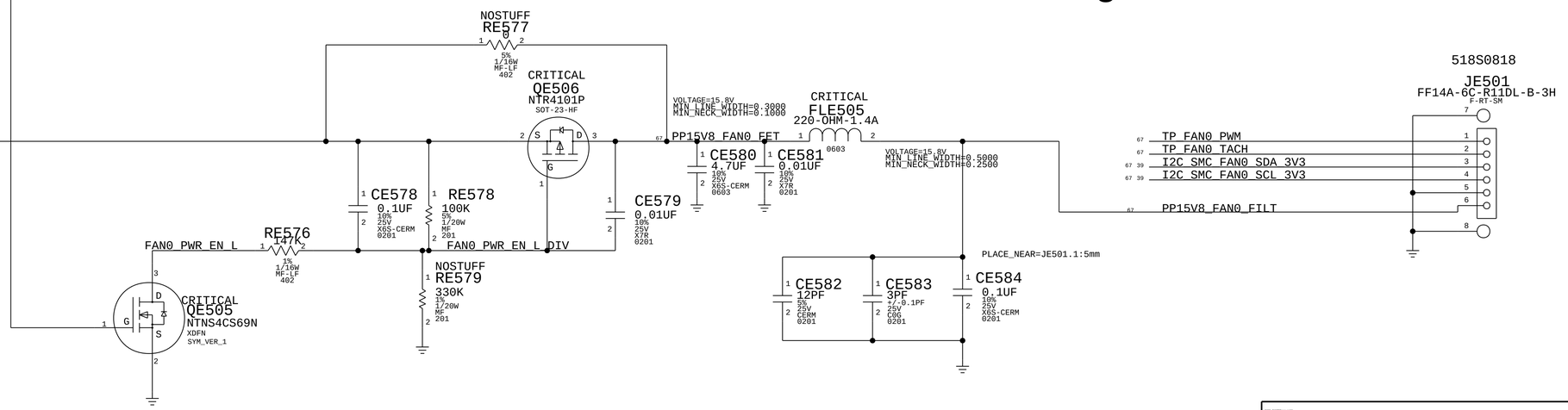
Fan Controller(located BY SOC)
Fan "1" ONLY on J456 design - SMC I2C0



Fan Controller (Located BY AUDIO AMP)
Fan "0" common to J456 & J457 designs - SMC I2C3



BOM_COST_GROUP=FAN

PAGE TITLE
FAN: System Fan Connector

Apple Inc.

DRAWING NUMBER 051-05371
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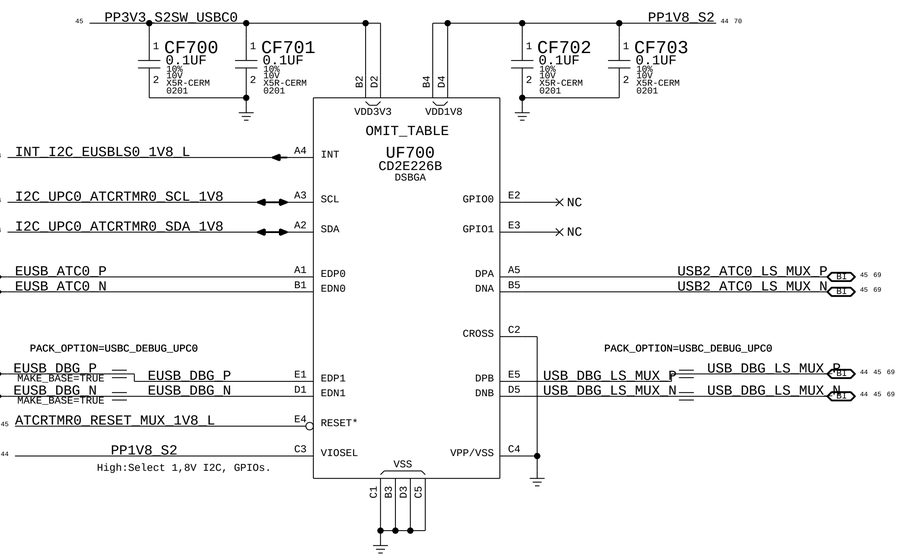
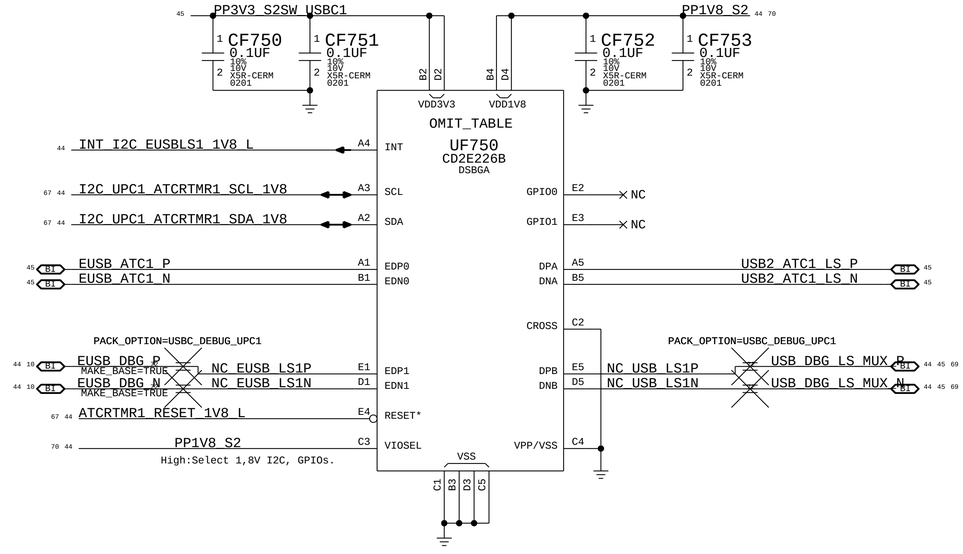
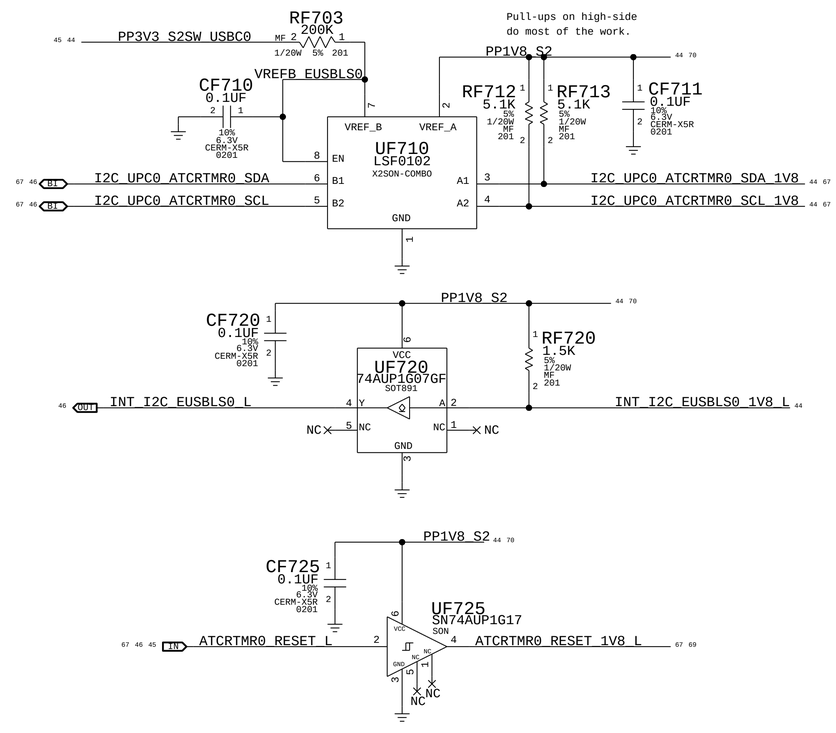
** OK2INTEGRATE **





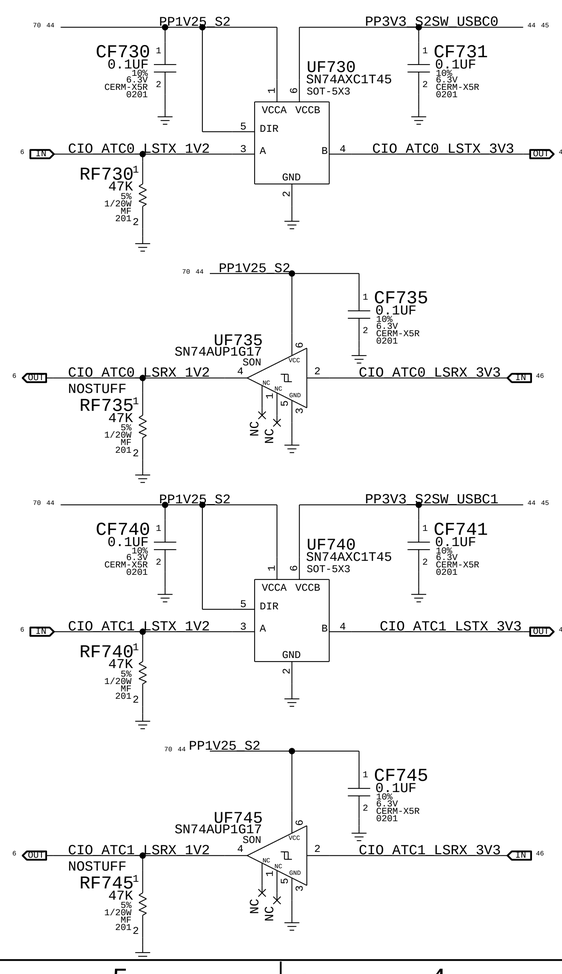


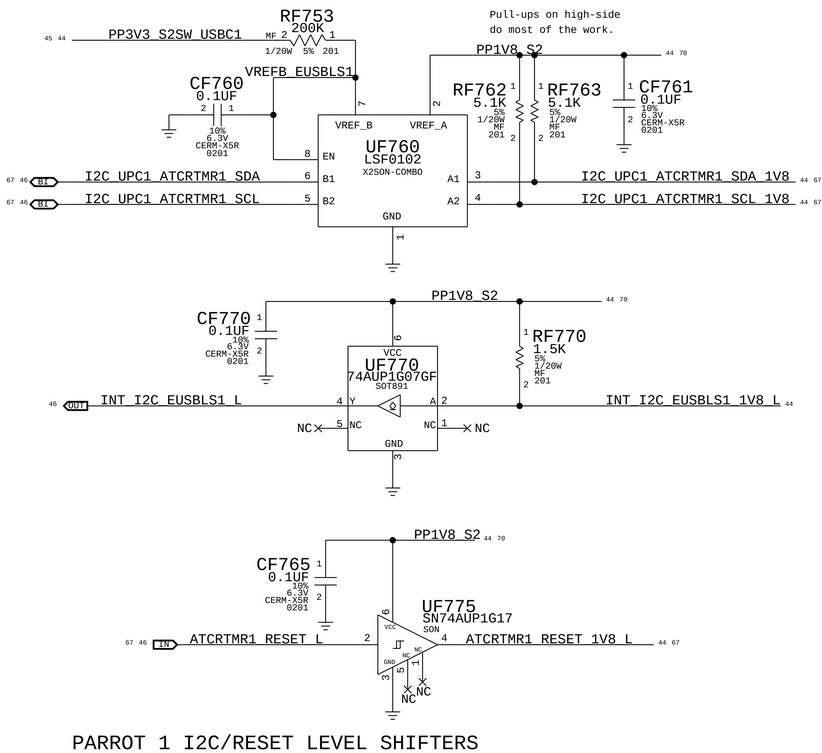
PARROT 0 I2C/RESET LEVEL SHIFTERS

TBT LS RX/TX LEVEL SHIFTERS

SOC

BBR Retimer





PARROT 1 I2C/RESET LEVEL SHIFTERS

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: HS Level Shifters

Apple Inc.

DRAWING NUMBER: 051-05371 | SIZE: D

REVISION: 6.0.0

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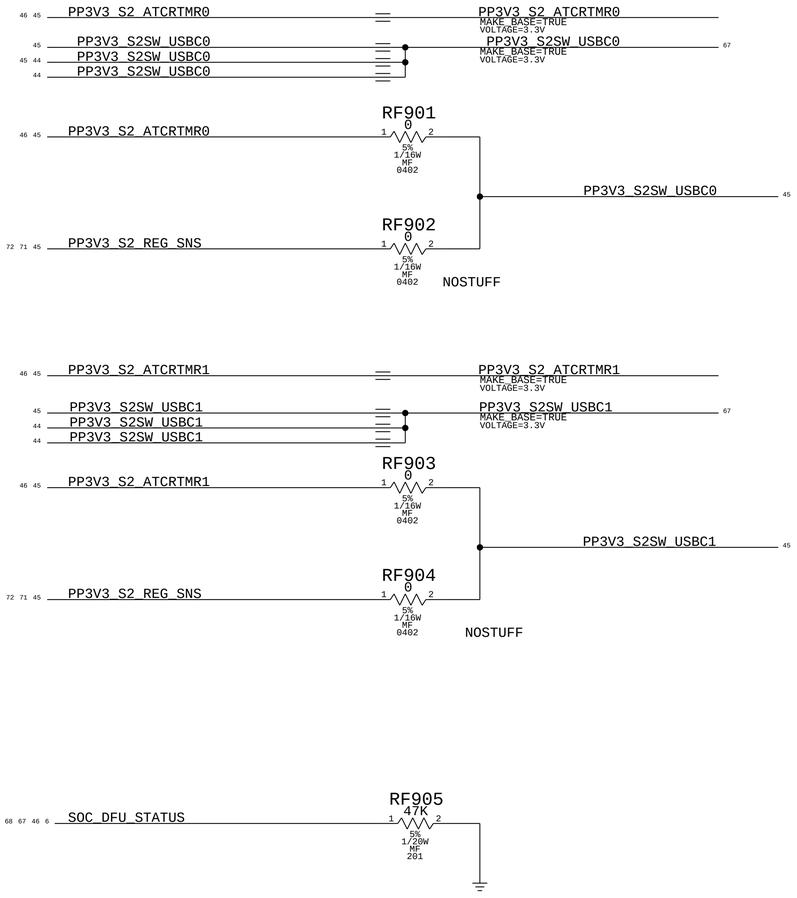

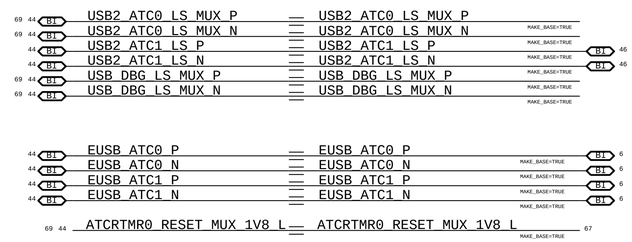

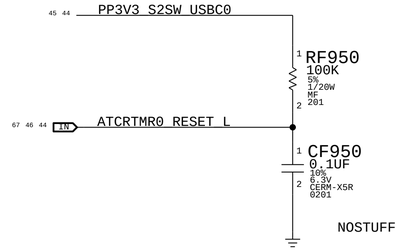

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Backup

Apple Inc.

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516S00266
JG614
20759-042E-02
F-ST-SM
RECEPTACLE

			43	PWR	44	PPBUS_AON	46 71 72
39	OUT	UPC_SMC_I2C_INT_R_L	1	SIGNAL	2	UPC_FORCE_PWR	IN 7 67
67 39 23 10	IN	I2C_SMC_UPC_SCL	3		4	I2C_SMC_SNS0_SCL_1V8	IN 39
67 39 23 10	BI	I2C_SMC_UPC_SDA	5		6	I2C_SMC_SNS0_SDA_1V8	BI 39
			7		8		
67 38	OUT	UPC_I2C_INT_R_L	9		10	USB3_WAKE_L	OUT 33
67 38 23 7	IN	I2C_UPC_SCL	11		12	USBHC_PERST_L	IN 20
67 38 23 7	BI	I2C_UPC_SDA	13		14	USBHC_CLKREQ_L	BI 9
			15		16		
33	IN	USB3_PWR_EN	17		18	TP_SPKRAMP_INT_L	
38	IN	I2C_SPKRAMP_R_SCL_1V8 CKPLUS_WAIVE=I2C_PULLUP	19		20	TP_SPKRAMP_RESET_L	Not used with ADI Amps
38	BI	I2C_SPKRAMP_R_SDA_1V8 CKPLUS_WAIVE=I2C_PULLUP	21		22	PMU_SYS_ALIVE	IN 33 57 67 68 72
			23		24		
72 70 46		PP3V3_S2_UPC	25		26	PP3V3_S2_UPC	46 70 72
			27		28		
72 71 46		PP3V3_S2_REG_SNS	29		30	PP3V3_S2_REG_SNS	46 71 72
			31		32		
72 70 46		PP1V8_S2	33		34	PP1V8_S2	46 70 72
			35		36	PP1V8_AWAKE	62 64 70
72 70 46		PP1V25_S2	37		38	PP1V25_S2	46 70 72
			39		40	PP1V2_AWAKE_IO	70 72
		TP_PPVBATT_41	41		42	TP_PPVBATT_42	
				PWR			
			45		46	PPBUS_AON	46 71 72
				GND			
			47		48		
			49		50		
			51		52		
			53		54		
			55		56		
			57		58		
			59		60		
			61		62		
			63		64		
			65		66		
			67		68		

516S00266
JG612
20759-042E-02
F-ST-SM
RECEPTACLE

			43	PWR	44	PP3V8_AON_VDDMAIN	71 72
45		PP3V3_S2_ATCRTMR0	1	SIGNAL	2	SWD_UPC_SWDIO2	BI 20
			3		4	TP_SPARE_TIOGAPASS2	
45		PP3V3_S2_ATCRTMR1	5		6	TP_SPARE_TIOGAPASS3	
			7		8	TP_SPARE_TIOGAPASS4	
			9		10		
44	IN	CIO_ATC0_LSTX_3V3	11		12	CIO_ATC0_LSRX_3V3	OUT 44
44	IN	CIO_ATC1_LSTX_3V3	13		14	CIO_ATC1_LSRX_3V3	OUT 44
67 44	BI	I2C_UPC0_ATCRTMR0_SCL	15		16	I2C_UPC0_ATCRTMR0_SDA CKPLUS_WAIVE=I2C_PULLUP	BI 44 67
44	IN	INT_I2C_EUSBLS0_L CKPLUS_WAIVE=I2C_PULLUP	17		18	ATCRTMR0_RESET_L CKPLUS_WAIVE=I2C_PULLUP	IN 44 45 67
			19		20		
68 67 48 33 6	IN	PMU_ACTIVE_READY	21		22	PMU_RESET_1V8	OUT 33 34 67
69	OUT	SOC_DOCK_CONNECT_UPC	23		24	SOC_DFU_STATUS	IN 5 45 67 68
69 67 10	OUT	SWD_SOC_SWCLK	25		26	UART_DEBUGPRT_D2R	OUT 7 67 69
69 67 10	BI	SWD_SOC_SWDIO	27		28	UART_DEBUGPRT_R2D	IN 7 67 69
69 67 10	OUT	UART_SMC_DEBUGPRT_D2R	29		30	SOC_FORCE_DFU	OUT 5 33 67 68
69 67 10	IN	UART_SMC_DEBUGPRT_R2D	31		32	SOC_SOCHOT_L	IN 7 33 67 69
			33		34		
67 23 7	IN	SWD_UPC_SWCLK	35		36	USB_DBG_LS_P	BI 67 69
7	BI	SWD_UPC_SWDIO0	37		38	USB_DBG_LS_N	BI 67 69
44	IN	INT_I2C_EUSBLS1_L	39		40	I2C_UPC1_ATCRTMR1_SCL CKPLUS_WAIVE=I2C_PULLUP	BI 44 67
67 44	IN	ATCRTMR1_RESET_L	41		42	I2C_UPC1_ATCRTMR1_SDA CKPLUS_WAIVE=I2C_PULLUP	BI 44 67
				PWR			
			45		46	PPBUS_AON	46 71 72
				GND			
			47		48		
			49		50		
			51		52		
			53		54		
			55		56		
			57		58		
			59		60		
			61		62		
			63		64		
			65		66		
			67		68		

9 IN PCIE_USBHC_R2D_C_N — CC602 0.22UF 1 2 6.3V 0201 20% X5R GND_VOID=TRUE

9 IN PCIE_USBHC_R2D_C_P — CC601 0.22UF 1 2 6.3V 0201 20% X5R GND_VOID=TRUE

518S0887
JG603
20525-160E-02
F-RT-SM

				61			
			1		2		
		NC	3		4	NC	
		NC	5		6	NC	
		NC	7		8	NC	
			9		10	TP_TDM_SPKRAMP_R_D2R	
20	IN	TDM_SPKRAMP_R_FSYNC	11		12	TDM_SPKRAMP_R_BCLK	IN 20
		NC	13		14	TDM_SPKRAMP_R_R2D	IN 20
		TP_SPKRAMP_ICC	15		16	USB2_ATC0_LS_P	BI 69 67
		USB2_ATC0_LS_N	17		18	USB2_ATC1_LS_P	BI 69 67
		USB2_ATC1_LS_N	19		20		BI 45
9	OUT	PCIE_USBHC_D2R_N GND_VOID=TRUE	21		22	PCIE_USBHC_D2R_P GND_VOID=TRUE	OUT 9
		PCIE_USBHC_R2D_N GND_VOID=TRUE	23		24	PCIE_USBHC_R2D_P GND_VOID=TRUE	
6	IN	USBC_ATC0_R2D_C_P<2> GND_VOID=TRUE	25		26	USBC_ATC0_R2D_C_N<2> GND_VOID=TRUE	IN 6
6	IN	USBC_ATC1_R2D_C_P<2> GND_VOID=TRUE	27		28	USBC_ATC1_R2D_C_N<2> GND_VOID=TRUE	IN 6
6	BI	USBC_ATC1_D2R_P<2> GND_VOID=TRUE	29		30	USBC_ATC1_D2R_N<2> GND_VOID=TRUE	BI 6
6	BI	USBC_ATC1_D2R_P<1> GND_VOID=TRUE	31		32	USBC_ATC1_D2R_N<1> GND_VOID=TRUE	BI 6
6	IN	USBC_ATC1_R2D_C_P<1> GND_VOID=TRUE	33		34	USBC_ATC1_R2D_C_N<1> GND_VOID=TRUE	IN 6
9	IN	PCIE_CLK100M_USBHC_N	35		36	PCIE_CLK100M_USBHC_P	IN 9
6	BI	USBC_ATC0_D2R_P<2> GND_VOID=TRUE	37		38	USBC_ATC0_D2R_N<2> GND_VOID=TRUE	BI 6
6	BI	USBC_ATC0_D2R_P<1> GND_VOID=TRUE	39		40	USBC_ATC0_D2R_N<1> GND_VOID=TRUE	BI 6
6	IN	USBC_ATC0_R2D_C_P<1> GND_VOID=TRUE	41		42	USBC_ATC0_R2D_C_N<1> GND_VOID=TRUE	IN 6
6	BI	USBC_ATC1_AUX_P	43		44	USBC_ATC1_AUX_N	BI 6
67 6	BI	USBC_ATC0_AUX_P	45		46		BI 6
		NC	47		48	NC	
		NC	49		50		
67 6	BI	USBC_ATC0_AUX_N	51		52		
			53		54		
			55		56		
			57		58		
			59		60		
			61		62		
			63		64		
			65		66		
			67		68		
			69		70		
			71		72		
			73				

BOM_COST_GROUP=USB-C

LAST CHANGE: Tue May 28th 22:57:37 2019

PAGE TITLE
USB-C: Connectors to mlb

Apple Inc.

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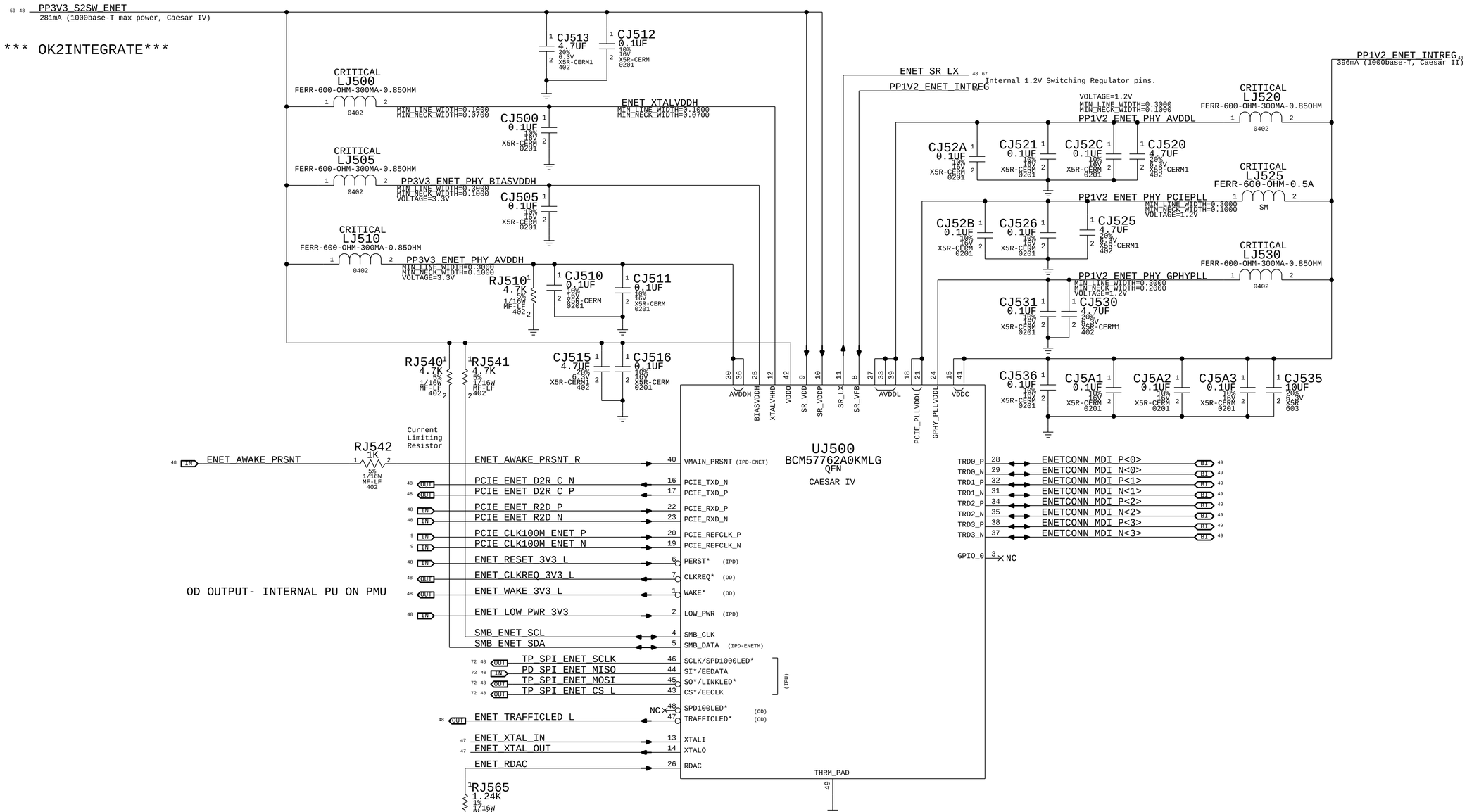

PAGE TITLE
ENET: 1G ENET PHY (Caesar IV)

Apple Inc.

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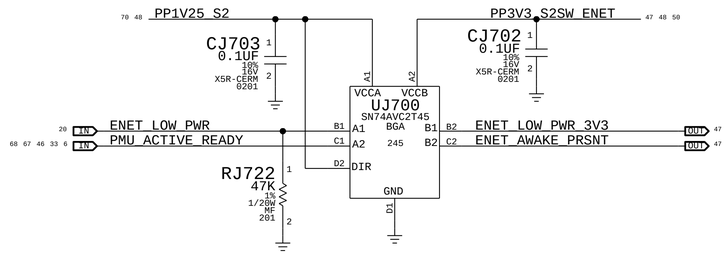
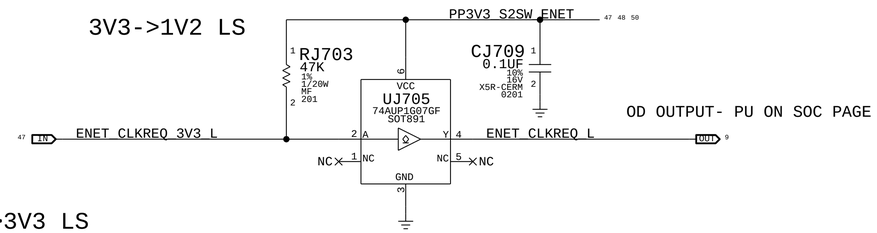
*** OK2INTEGRATE***

LEVEL SHIFTERS

1V2->3V3 LS
DIRECTION IS A->B

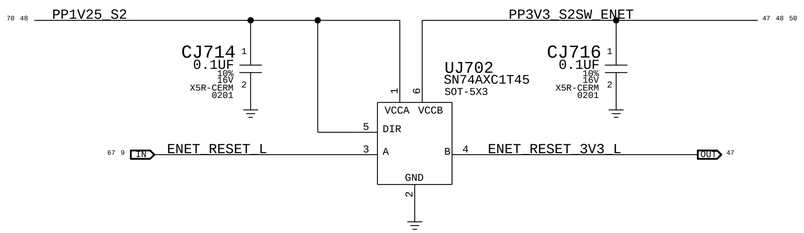


3V3->1V2 LS

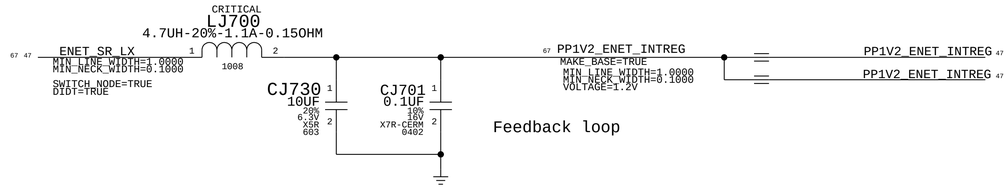


OD OUTPUT- PU ON SOC PAGE

1V2->3V3 LS

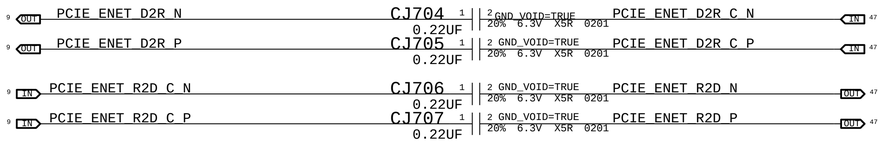


CAESAR IV 1.2V INT.VR CMPTS

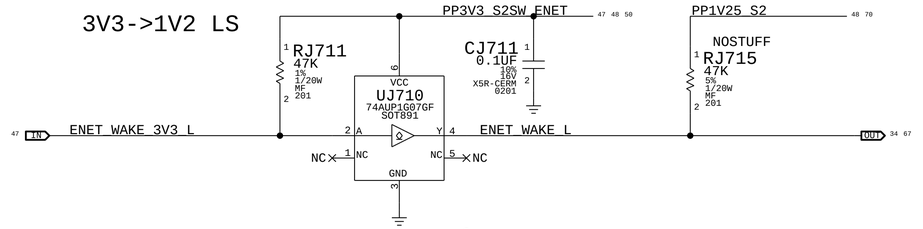


Feedback loop

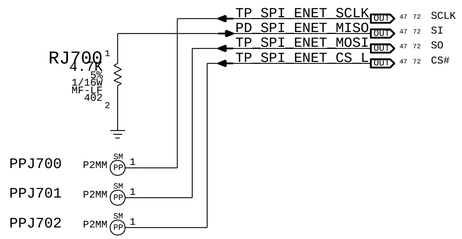
ENET PCIE AC Caps



3V3->1V2 LS



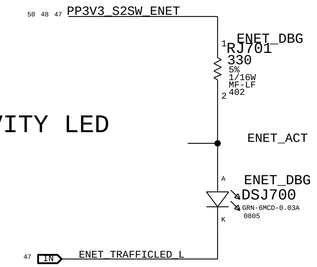
CAESAR IV NON-VOLATILE MEMORY STRAPPING



CAESAR 4 HAS INTERNAL PULLUPS ON THESE PINS

SO	SI	CS#	SCLK	COMPATIBLE NVRAM (ROM CONTAINS MAC ADDRESS, PCIE CONFIG, NIC PROXY)
-	0	1	-	AUTO SENSE (ON CHIP), ATMEL - AT45DB011D, AT45DB021D, ST - M45PE10, M45PE20
-	1	0	-	EEPROM - 24C64, 24C512 - 376 KHZ.
-	1	1	-	MICROCHIP - 24LC04, 24LC08 - 376 KHZ.

1G ETHERNET ACTIVITY LED



BOM_COST_GROUP=ETHERNET

SYNC_MASTER=will SYNC_DATE=11/22/2019

PAGE TITLE: ENET: 1G SUPPORT 1

Apple Inc.

DRAWING NUMBER: 051-05371 SIZE: D
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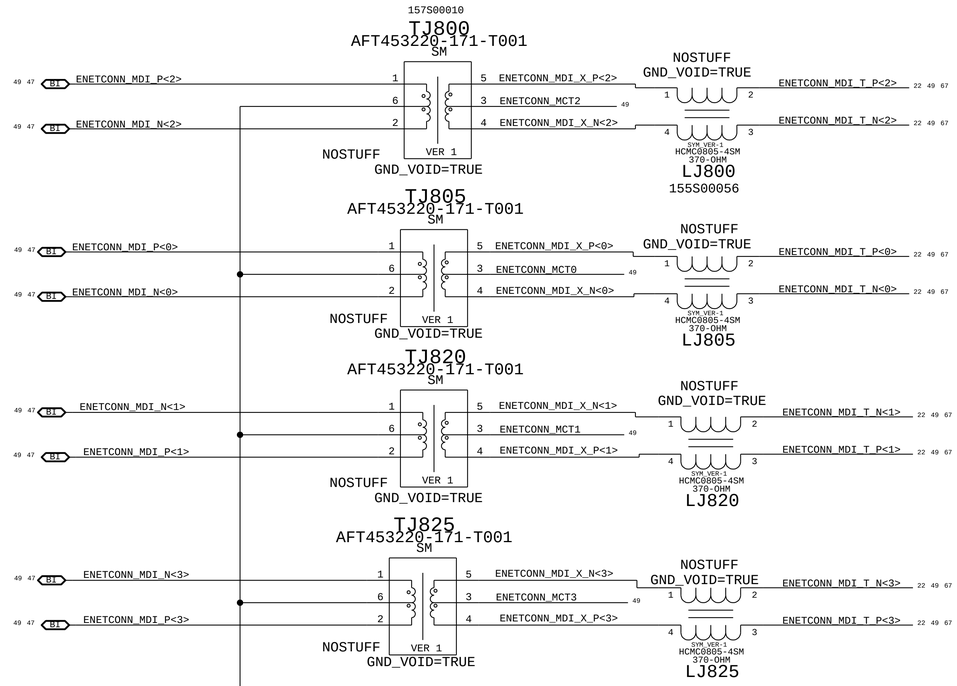
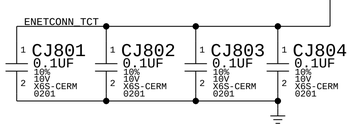
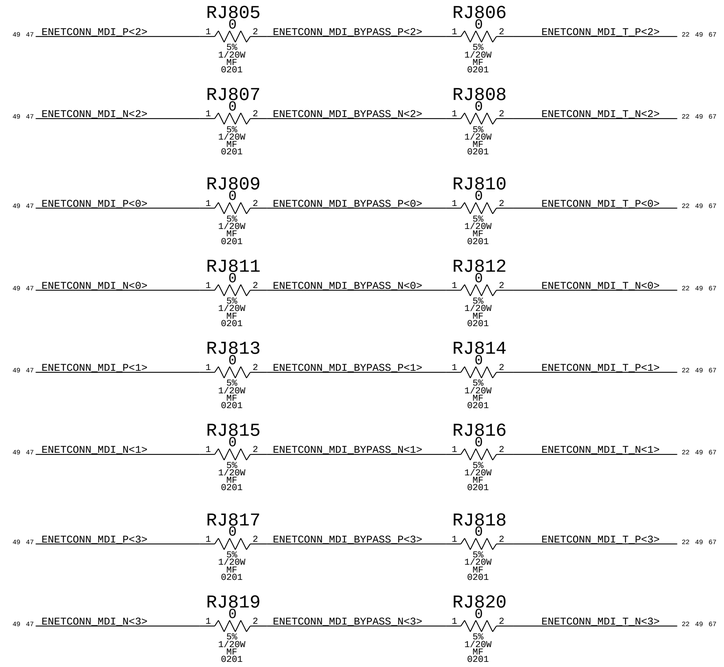
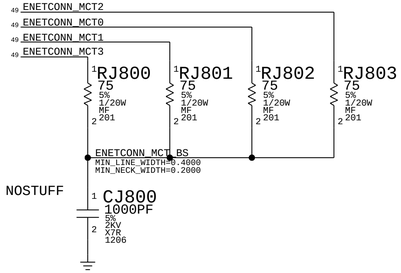
*** 0K2PLACE ***









BOM_COST_GROUP=ETHERNET

PAGE TITLE: ENET: SUPPORT 2

Apple Inc.

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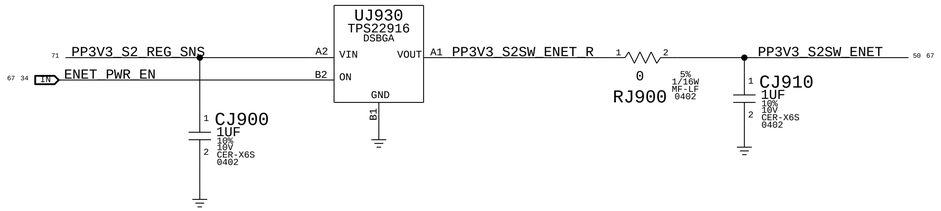
ENET POWER INPUT



67 50 PP3V3_S2SW_ENET — PP3V3_S2SW_ENET 47 48

MAKE_BASE=TRUE
VOLTAGE=3.3V

BOM_COST_GROUP=ETHERNET

PAGE TITLE
ENET: EXTERNAL SWITCHES/LDOS

Apple Inc.

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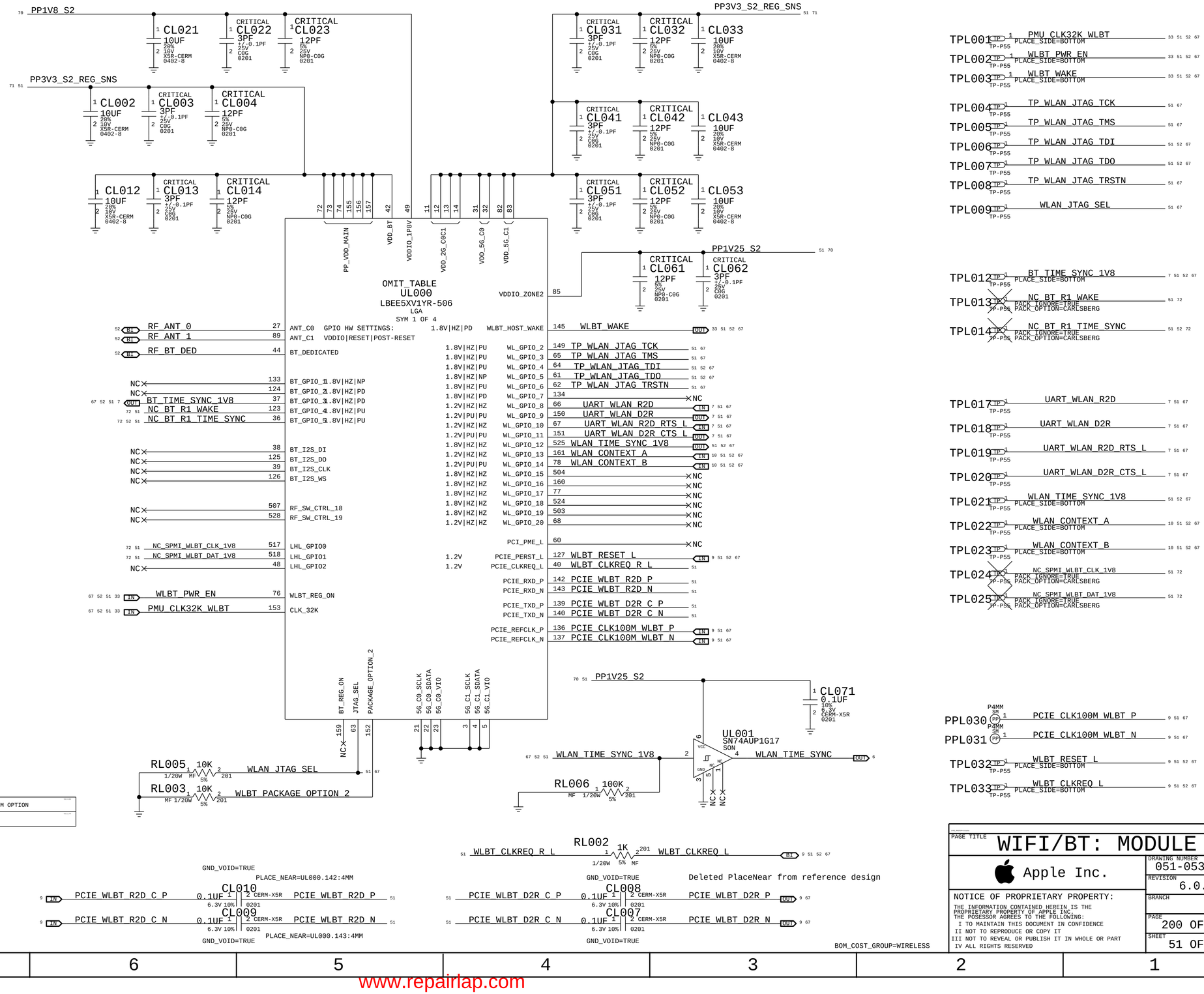
*** OK2INTEGRATE ***

RASPUTIN WIFI/BT MODULE

FOR HOSTINTERFACE TABLES REFER TO:
RDAR://PROBLEM/53187294

FOR DESIGN, DOCUMENTATION, SYSTEM INTEGRATION QUESTIONS:
RDAR://PROBLEM/44786407



RASPUTIN BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00763	1	MODULE, WLAN BT, RASPUTIN, ES6.11, M, LGA549	UL000	CRITICAL	

RASPUTIN ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00758	339S00763	ANY	UL000	RASPUTIN USI ES6.5

PAGE TITLE: WIFI/BT: MODULE

Apple Inc.

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RASPUTIN WIFI/BT MODULE GND

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 2 OF 4

1			119
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6			121
7			122
8			128
9			129
10			130
15			131
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58	GND	GND	179
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OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 3 OF 4

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302			383

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 4 OF 4

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461			548
462			549

ANTENNA CONNECTORS

2G_C1
5G_C0
BT_C0

JL100
IR050D15010C
F-ST-SM
1 RF_ANT_0 → BT 51 52
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=SUNWAY

JL100
20449-001E-03
F-ST-SM
1 RF_ANT_0 51 52
2 3 4
PACK_OPTION=T664_IPEX

JL110
20449-001E-03
F-ST-SM
1 RF_ANT_0 51 52
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=IPEX

JL120
20431-001E-01
F-SM
2 SIGNAL 1 RF_ANT_0 51 52
GND
4 5
PACK_IGNORE=TRUE
PACK_OPTION=ANT_MAC_MINI

2G_C0
5G_C1
BT_C1

JL101
IR050D15010C
F-ST-SM
1 RF_ANT_1 → BT 51 52
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=SUNWAY

JL101
20449-001E-03
F-ST-SM
1 RF_ANT_1 51 52
2 3 4
PACK_OPTION=T664_IPEX

JL111
20449-001E-03
F-ST-SM
1 RF_ANT_1 51 52
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=IPEX

JL121
20431-001E-01
F-SM
2 SIGNAL 1 RF_ANT_1 51 52
GND
4 5
PACK_IGNORE=TRUE
PACK_OPTION=ANT_MAC_MINI

BT_C0_DED

JL102
20449-001E-03
F-ST-SM
1 52 RF_BT_DED_ANT
2 3 4
PACK_OPTION=T664_IPEX

PACK_OPTION=3X_ANTENNA
RL102 0 1/20W MF 2 5% 0201
RF_BT_DED_FOUT

CL101 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
PACK_OPTION=3X_ANTENNA

CL102 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
PACK_OPTION=3X_ANTENNA

PACK_OPTION=3X_ANTENNA
UL101
2.4G
0603
1 IN OUT 3
GND
2 4
RF_BT_DED_FIN

PACK_OPTION=3X_ANTENNA
RL104 0 1/20W MF 2 5% 0201
RF_BT_DED → BT 51

CL103 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
PACK_OPTION=3X_ANTENNA

CL105 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
PACK_OPTION=3X_ANTENNA

JL122
20431-001E-01
F-ST-SM
2 SIGNAL 1 RF_BT_DED_ANT 52
GND
4 5
PACK_IGNORE=TRUE
PACK_OPTION=ANT_MAC_MINI

WLBT DEBUG CONNECTOR

JL103
505070-1222
M-ST-SM
14 13
16 15

67 51	WLAN_TIME_SYNC_1V8	2 1	TP_WLAN_JTAG_TDI 51 67
67 51 18	WLAN_CONTEXT_A	4 3	TP_WLAN_JTAG_TDO 51 67
67 51 18	WLAN_CONTEXT_B	6 5	NC_BT_R1_TIME_SYNC 51 72
67 51 33	WLBT_WAKE	8 7	WLBT_CLKREQ_L 9 51 67
67 51 33	WLBT_PWR_EN	10 9	BT_TIME_SYNC_1V8 7 51 67
67 51 9	WLBT_RESET_L	12 11	PMU_CLK32K_WLBT 33 51 67

BOMOPTION=WLBT_DBG
PACK_OPTION=WLBT_DBG_CONN

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

Apple Inc.

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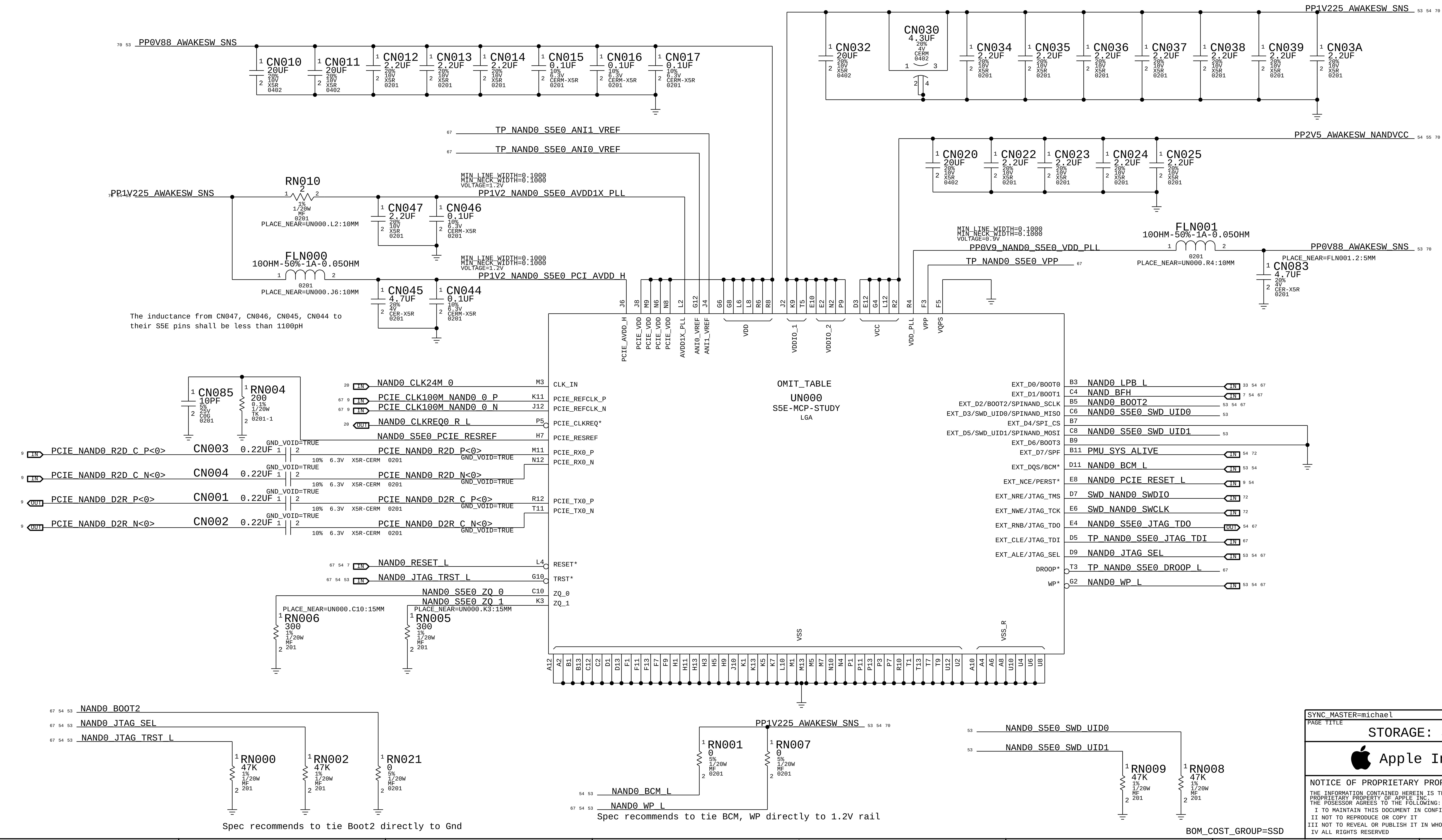
*** OK2INTEGRATE ***

NAND0 S5E0



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PAGE TITLE: STORAGE: SSD0 S5E <0>

DRAWING NUMBER: 051-05371 SIZE: D

Apple Inc.

REVISION: 6.0.0

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

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*** OK2INTEGRATE ***

NAND0 S5E1

PP0V88_AWAKESW_SNS — CN110 20UF, CN111 20UF, CN112 2.2UF, CN113 2.2UF, CN114 2.2UF, CN115 0.1UF, CN116 0.1UF, CN117 0.1UF

PP1V225_AWAKESW_SNS — CN132 20UF, CN130 4.3UF, CN134 2.2UF, CN135 2.2UF, CN136 2.2UF, CN137 2.2UF, CN138 2.2UF, CN139 2.2UF, CN13A 2.2UF

PP2V5_AWAKESW_NANDVCC — CN120 20UF, CN122 2.2UF, CN123 2.2UF, CN124 2.2UF, CN125 2.2UF

TP_NAND0_S5E1_ANI1_VREF

TP_NAND0_S5E1_ANI0_VREF

PP1V225_AWAKESW_SNS — RN110 2 (1% 1/25W MF 0201) PLACE_NEAR=UN100.L2:10MM

PP1V2_NAND0_S5E1_AVDD1X_PLL — CN147 2.2UF, CN146 0.1UF

MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V

FLN100 10OHM-50%-1A-0.05OHM (0201) PLACE_NEAR=UN100.J6:10MM

PP1V2_NAND0_S5E1_PCI_AVDD_H — CN145 4.7UF, CN144 0.1UF

MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V

The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

PP0V9_NAND0_S5E1_VDD_PLL — FLN101 10OHM-50%-1A-0.05OHM (0201) PLACE_NEAR=UN100.R4:10MM — CN183 4.7UF — PP0V88_AWAKESW_SNS

MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V

PLACE_NEAR=FLN101.2:5MM

TP_NAND0_S5E1_VPP

CN185 10PF (5% 25V C0G 0201) — RN104 200 (0.1% 1/20W TF 0201-1)

PCIE_NAND0_R2D_C_P<1>	CN103 0.22UF	PCIE_NAND0_R2D_P<1>	GND_VOID=TRUE
PCIE_NAND0_R2D_C_N<1>	CN104 0.22UF	PCIE_NAND0_R2D_N<1>	GND_VOID=TRUE
PCIE_NAND0_D2R_P<1>	CN101 0.22UF	PCIE_NAND0_D2R_C_P<1>	GND_VOID=TRUE
PCIE_NAND0_D2R_N<1>	CN102 0.22UF	PCIE_NAND0_D2R_C_N<1>	GND_VOID=TRUE

10% 6.3V X5R-CERM 0201

NAND0_CLK24M_1	M3	CLK_IN
PCIE_CLK100M_NAND0_1_P	K11	PCIE_REFCLK_P
PCIE_CLK100M_NAND0_1_N	J12	PCIE_REFCLK_N
NAND0_CLKREQ1_R_L	P5	PCIE_CLKREQ*
NAND0_S5E1_PCIE_RESREF	H7	PCIE_RESREF
PCIE_NAND0_R2D_P<1>	M11	PCIE_RX0_P
PCIE_NAND0_R2D_N<1>	N12	PCIE_RX0_N
PCIE_NAND0_D2R_C_P<1>	R12	PCIE_TX0_P
PCIE_NAND0_D2R_C_N<1>	T11	PCIE_TX0_N
NAND0_RESET_L	L4	RESET*
NAND0_JTAG_TRST_L	G10	TRST*
NAND0_S5E1_ZQ_0	C10	ZQ_0
NAND0_S5E1_ZQ_1	K3	ZQ_1

PLACE_NEAR=UN100.C10:15MM — RN106 300 (1% 1/20W MF 201) SSD_2L

PLACE_NEAR=UN100.K3:15MM — RN105 300 (1% 1/20W MF 201) SSD_2L

OMIT_TABLE

UN100 S5E-MCP-STUDY LGA

PCIE_AVDD_H: J6
PCIE_VDD: J8, M9, N6, N8
PCIE_VDD: L2
AVDDIX_PLL: G12
ANI0_VREF: J4
ANI1_VREF: G6
VDD: G8, L6, L8, R6, R8
VDDIO_1: J2, K9, T5
VDDIO_2: E10, E2, N2, P9
VCC: D3, E12, G4, L12, R2
VDD_PLL: R4
VPP: F3
VQPS: F5
VSS: A12, A2, B13, C12, C2, D1, D13, F1, F11, F13, F7, F9, H1, H11, H13, H3, H5, H9, J10, K1, K13, K5, K7, L10, M1, M13, M5, M7, N10, N4, P1, P11, P13, P3, P7, R10, T1, T13, T7, T9, U12, U2
VSS_R: A10, A4, A6, A8, U10, U4, U6, U8

EXT_D0/BOOT0	B3	NAND0_LPB_L
EXT_D1/BOOT1	C4	NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND0_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND0_S5E1_SWD_UID0
EXT_D4/SPI_CS	B7	
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND0_S5E1_SWD_UID1
EXT_D6/BOOT3	B9	
EXT_D7/SPF	B11	PMU_SYS_ALIVE
EXT_DQS/BCM*	D11	NAND0_BCM_L
EXT_NCE/PERST*	E8	NAND0_PCIE_RESET_L
EXT_NRE/JTAG_TMS	D7	SWD_NAND0_SWDIO
EXT_NWE/JTAG_TCK	E6	SWD_NAND0_SWCLK
EXT_RNB/JTAG_TDO	E4	TP_NAND0_S5E1_JTAG_TDO
EXT_CLE/JTAG_TDI	D5	NAND0_S5E0_JTAG_TDO
EXT_ALE/JTAG_SEL	D9	NAND0_JTAG_SEL
DROOP*	T3	TP_NAND0_S5E1_DROOP_L
WP*	G2	NAND0_WP_L

PP1V225_AWAKESW_SNS — RN108 47K (1% 1/20W MF 201) SSD_2L

NAND0_S5E1_SWD_UID0

NAND0_S5E1_SWD_UID1 — RN109 47K (1% 1/20W MF 201) SSD_2L

BOM_COST_GROUP=SSD

SYNC_MASTER=michael SYNC_DATE=05/04/2020

PAGE TITLE: STORAGE: SSD0 S5E <1>

Apple Inc.

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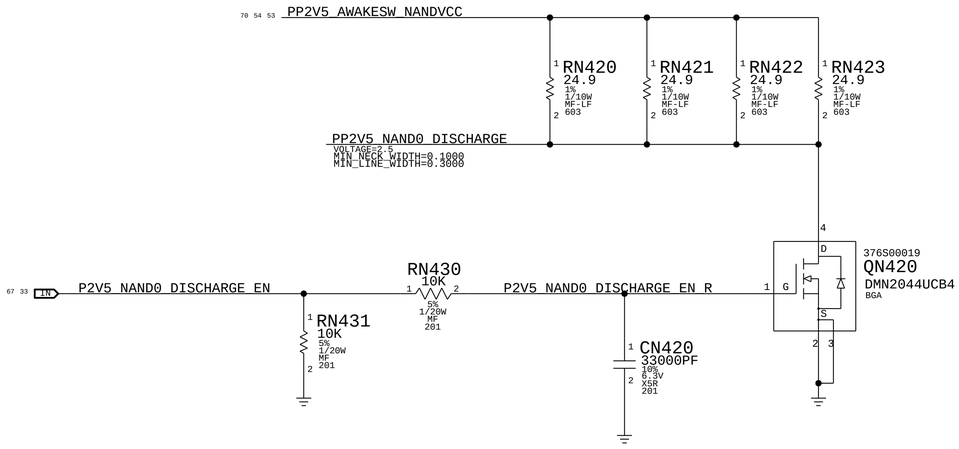
OK2INTEGRATE

THIS EXTERNAL NAND VCC DISCHARGE CIRCUITRY IS FOR SYSTEM THAT DOES NOT USE OCARINA



PAGE TITLE	STORAGE: NON OCARINA SUPPORT
	Apple Inc.
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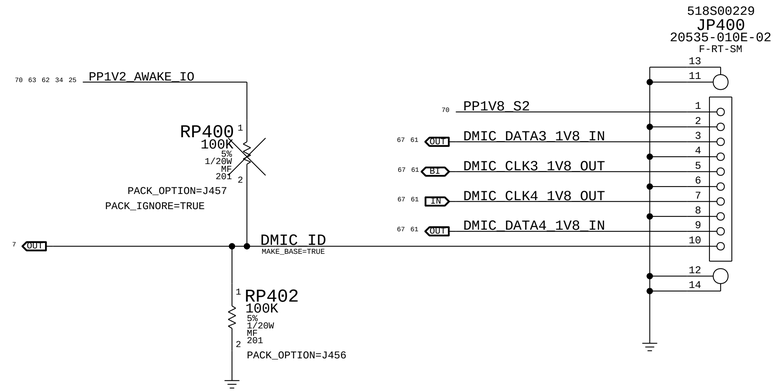
DMIC connector



BOM_COST_GROUP=AUDIO

SYNC_MASTER=tony SYNC_DATE=03/30/2020

PAGE TITLE

DMIC connector

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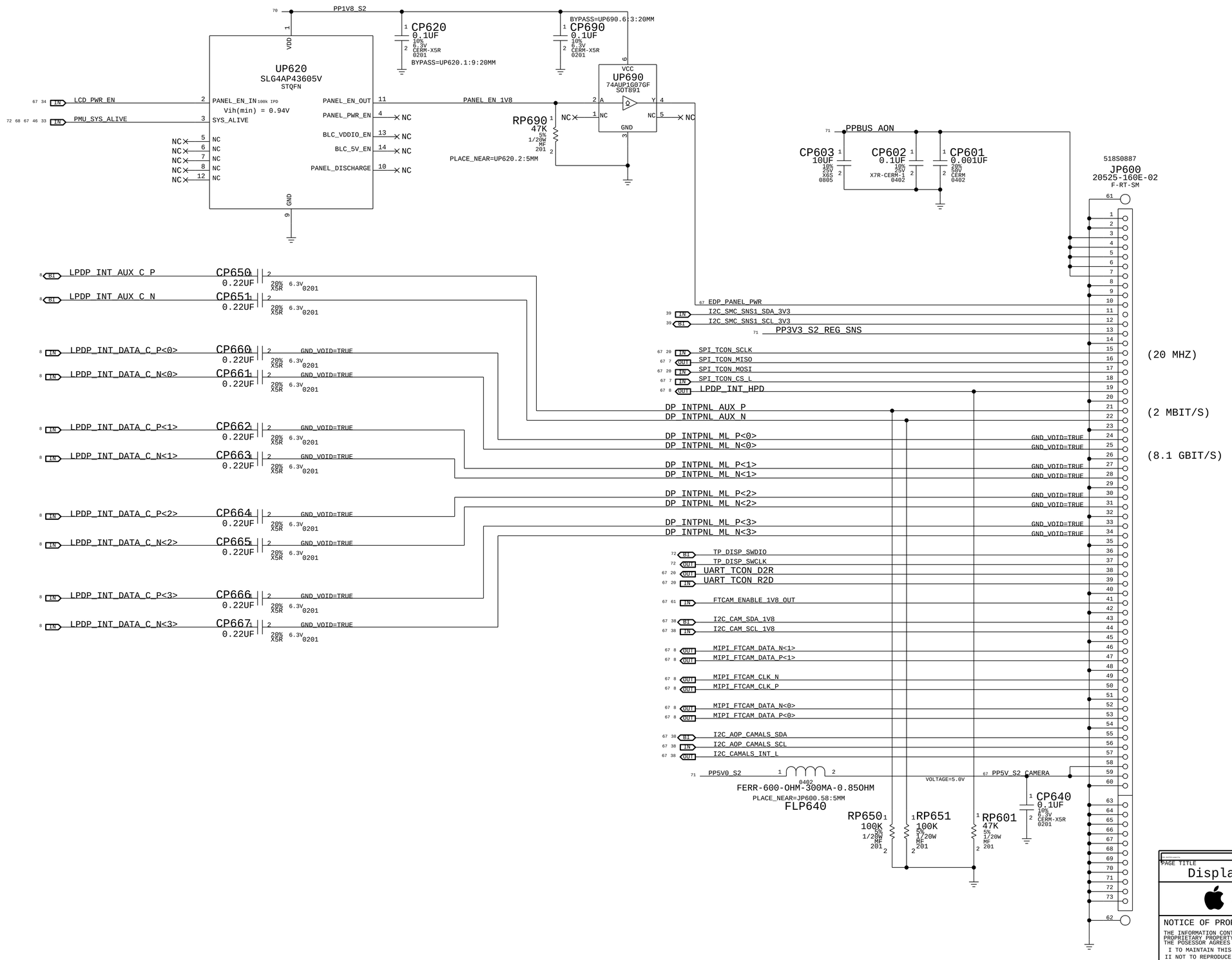

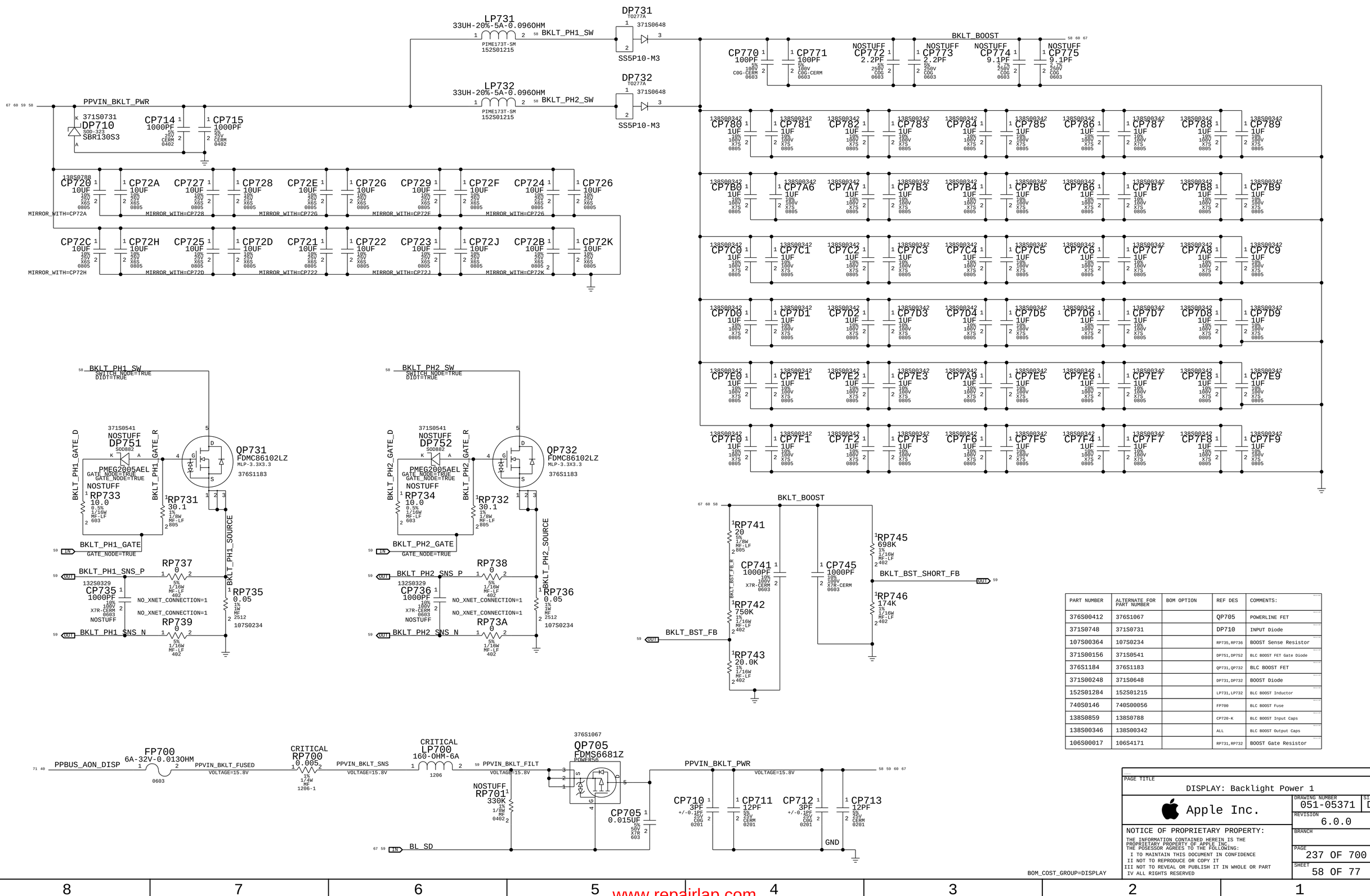

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00412	376S1067		QP705	POWERLINE FET
371S0748	371S0731		DP710	INPUT Diode
107S00364	107S0234		RP735,RP736	BOOST Sense Resistor
371S00156	371S0541		DP751,DP752	BLC BOOST FET Gate Diode
376S1184	376S1183		QP731,QP732	BLC BOOST FET
371S00248	371S0648		DP731,DP732	BOOST Diode
152S01284	152S01215		LP731,LP732	BLC BOOST Inductor
740S0146	740S00056		FP700	BLC BOOST Fuse
138S0859	138S0788		CP720-K	BLC BOOST Input Caps
138S00346	138S00342		ALL	BLC BOOST Output Caps
106S00017	106S4171		RP731,RP732	BOOST Gate Resistor

PAGE TITLE
DISPLAY: Backlight Power 1

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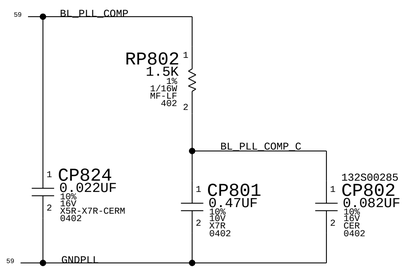
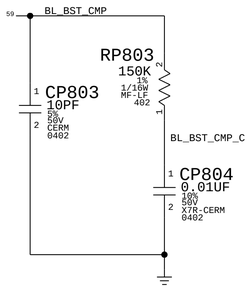
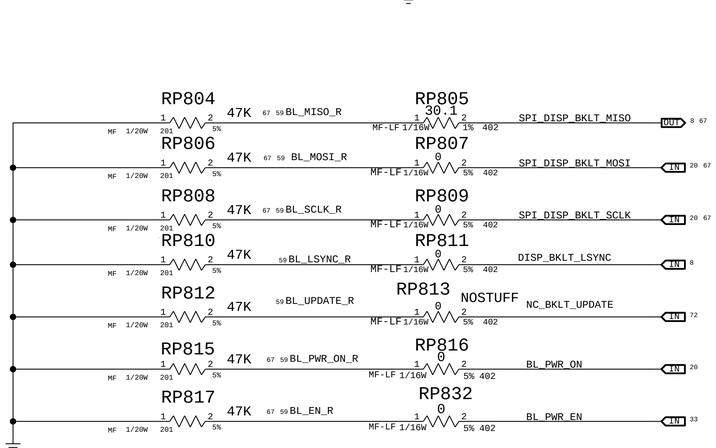
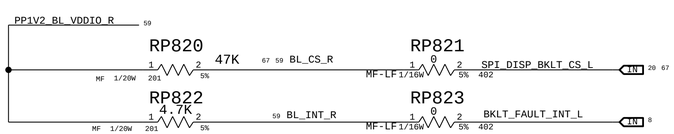
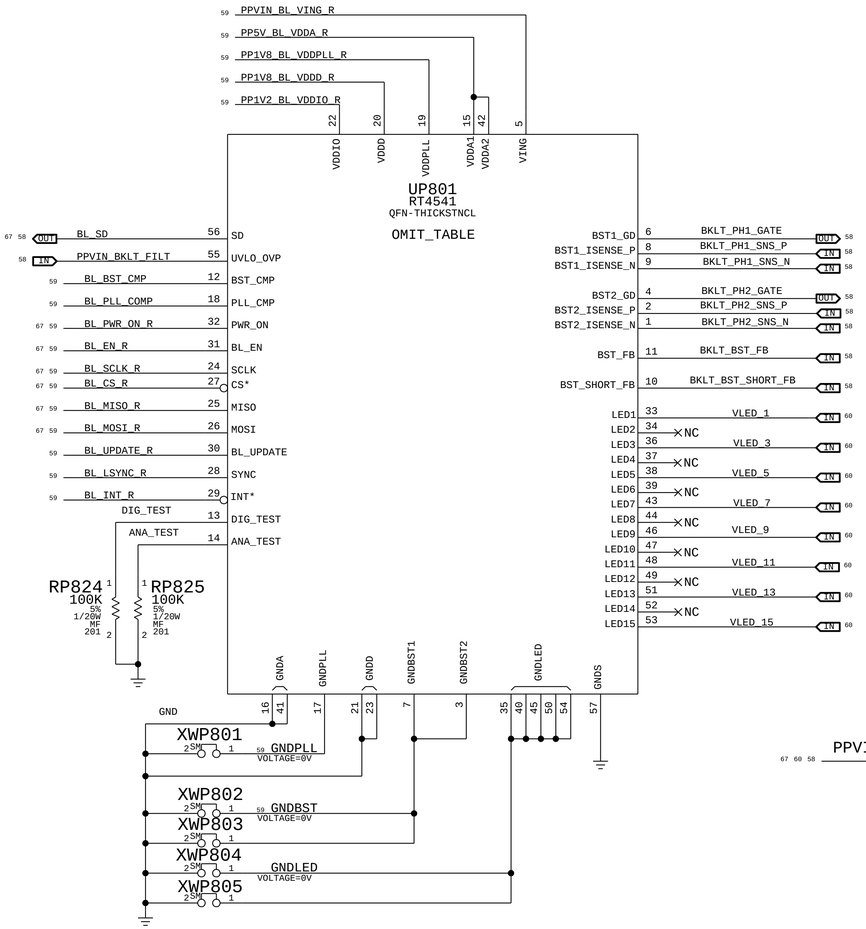
BOM_COST_GROUP=DISPLAY

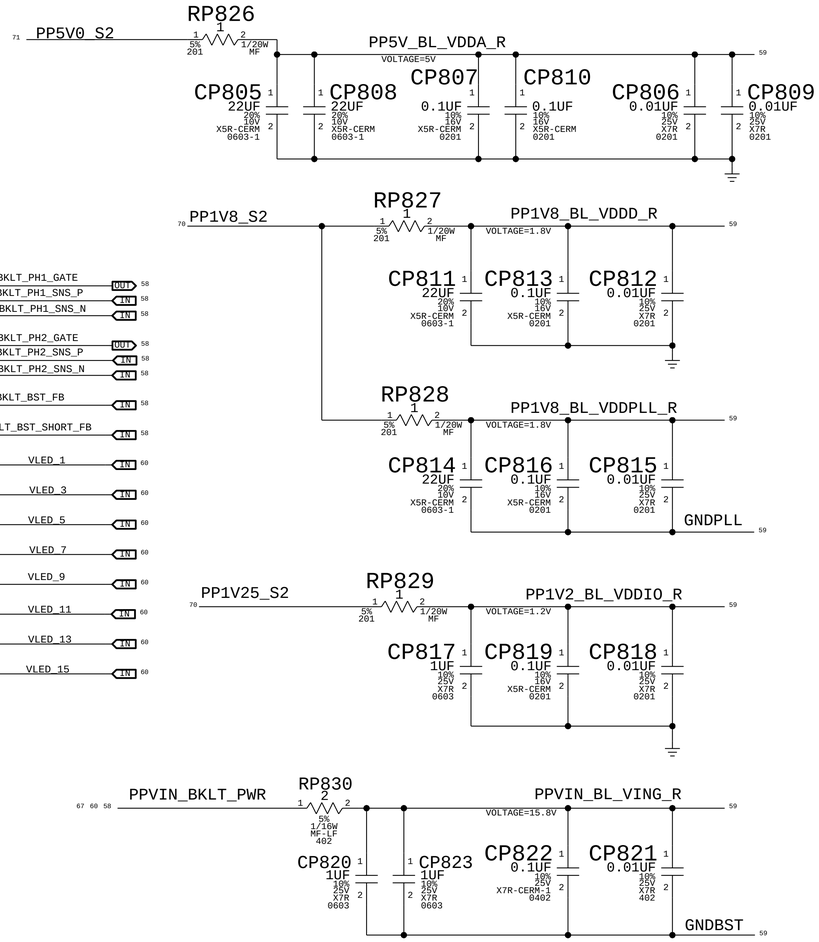












PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02654	1	IC, PIPA, RT4541-09, LED BACKLIGHT DRVR, QFN56	UP801	CRITICAL	

BOM_COST_GROUP=DISPLAY

PAGE TITLE
DISPLAY: Backlight Controller

Apple Inc.

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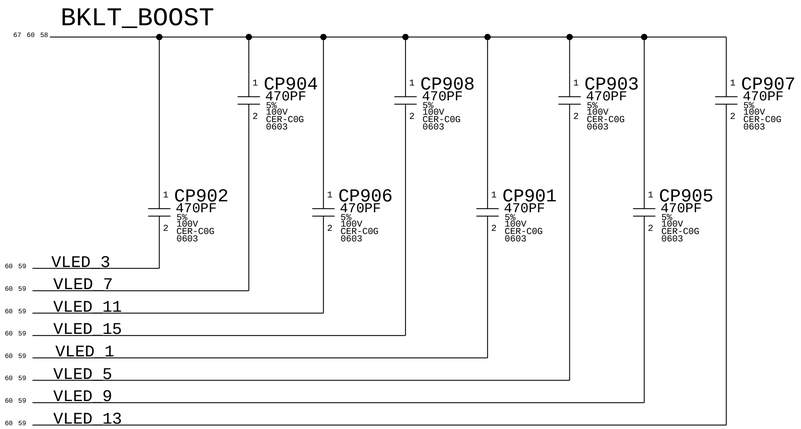

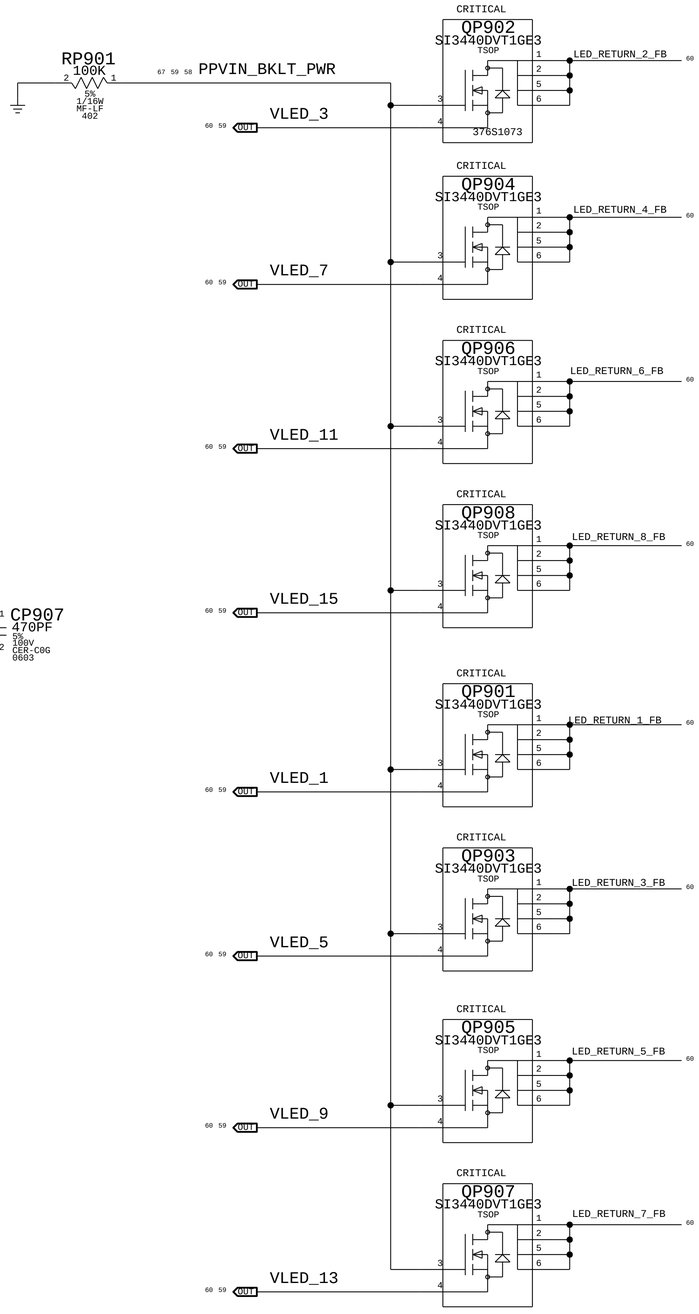

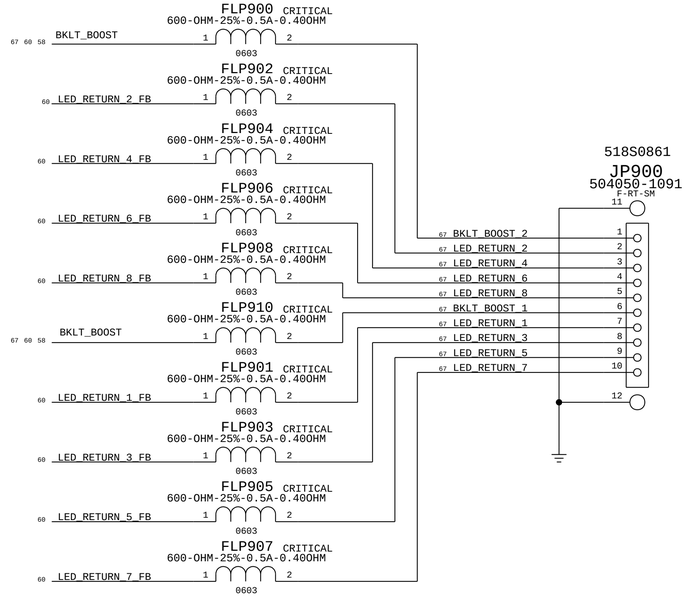

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FLP900 TO FLP911

BOM_COST_GROUP=DISPLAY

PAGE TITLE
DISPLAY: Backlight Power 3

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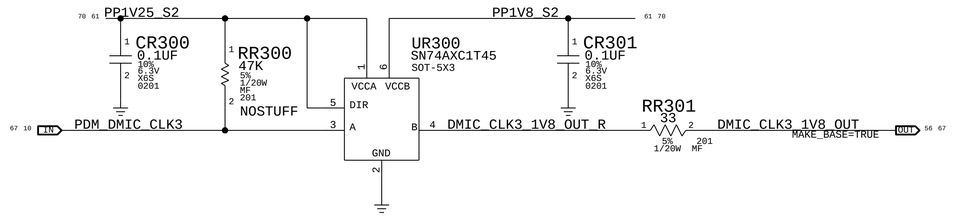
NC Aliases

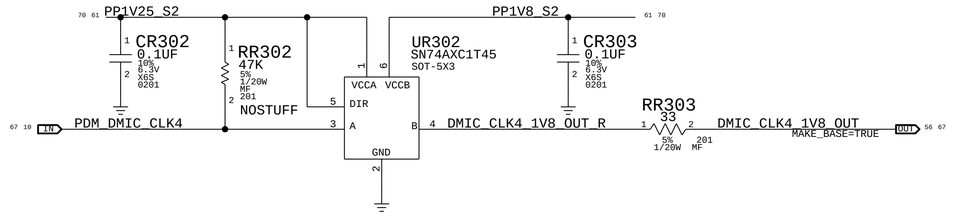
7 IN NC_DISABLE_STROBE = NC_DISABLE_STROBE MAKE_BASE=TRUE

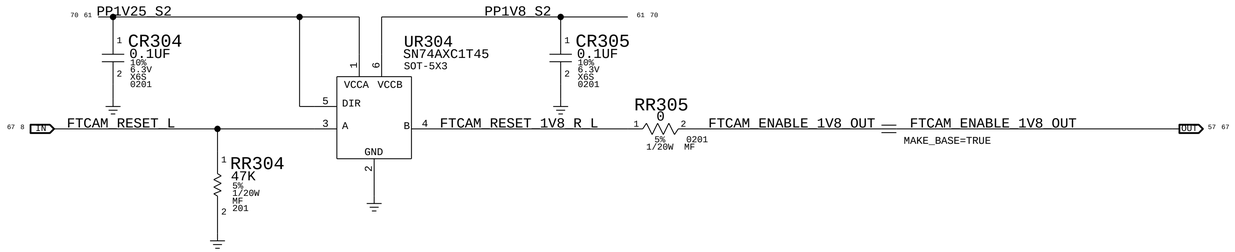
7 IN NC_FTCAM_DISABLE_L = NC_FTCAM_DISABLE_L MAKE_BASE=TRUE

7 IN NC_DMIC_DISABLE_L = NC_DMIC_DISABLE_L MAKE_BASE=TRUE

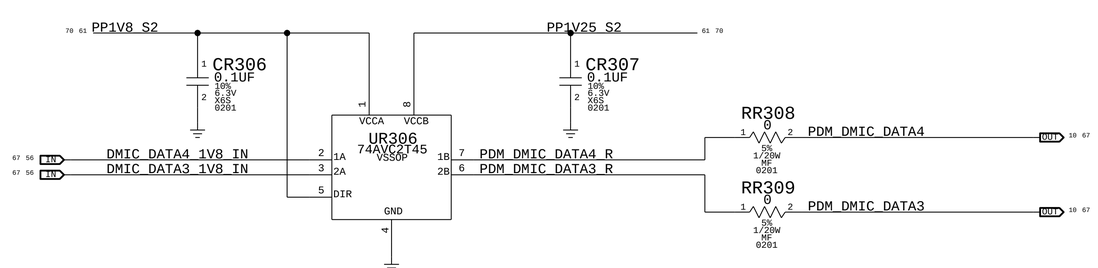
Level Shifter - DMIC & FTCAM







DIRECTION IS A->B for second source



From connector

To connector

BOM_COST_GROUP=SOC

SYNC_MASTER=samantha SYNC_DATE=05/21/2020

PAGE TITLE: SECDIS: Level Shifters

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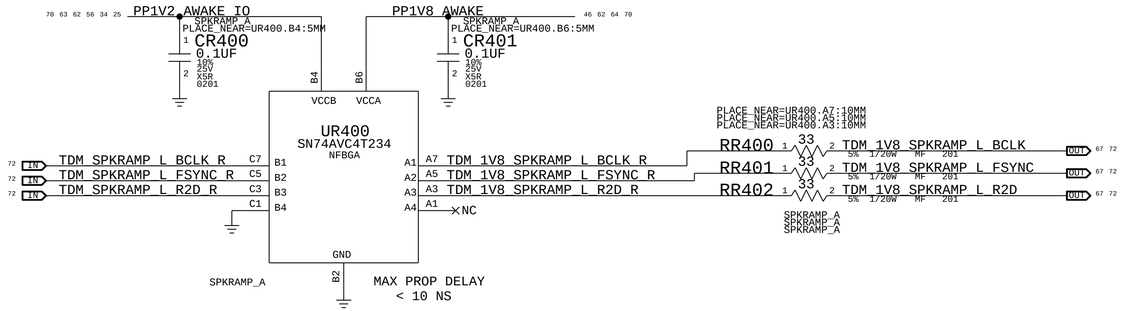
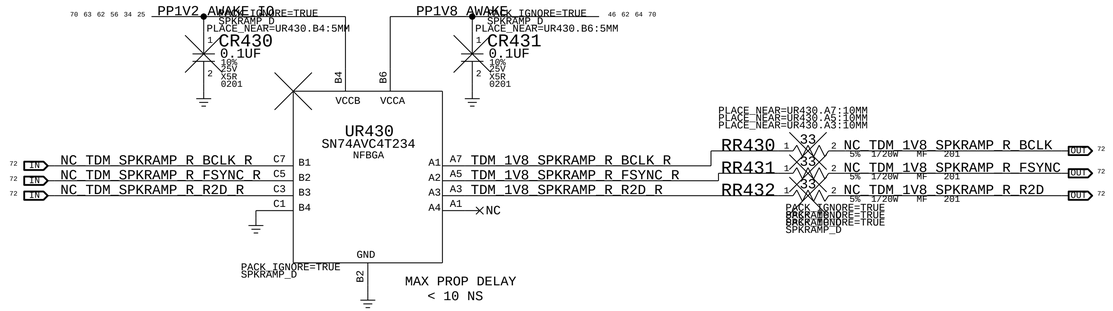
*** OK2INTEGRATE ***

AUDIO 1.2V <-> 1.8V LEVEL SHIFTERS





AUDIO TEST POINTS

COPY BELOW THE AUDIO TEST POINTS THAT WILL BE LOCATED ON THIS DESIGN

AMPLIFIERS I2C ADDRESSES VS PU/PD RESISTORS

SSM3515				
I2C @ 7-BIT	I2C @ 8-BIT	ADDR PIN	P-U RES.	P-D RES.
0X14	0X28	47K TO GND	NOSTUFF	117S0105
0X15	0X2A	OPEN	NOSTUFF	NOSTUFF
0X16	0X2C	47K TO 1.8V	117S0105	NOSTUFF
0X17	0X2E	0R TO 1.8V	117S0201	NOSTUFF

SYNC_MASTER=david SYNC_DATE=09/28/2020

PAGE TITLE: AUDIO SUPPORT

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*** OK2INTEGRATE ***

AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B

CHANGES FROM PREVIOUS DESIGNS:
- REMOVED LDO TO GENERATE LOCAL 1.8V <RDAR://50645294>
- CHANGED VL SUPPLY FROM 1.8V TO 1.2V <RDAR://TBD>
- SUPPLIED VD_FILT EXTERNALLY <RDAR://TBD>
- CHANGED VP SUPPLY FROM 3.3V TO 3.8V <RDAR://TBD>

NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1
- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND
- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR. CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.
- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP WHEN THE OTHER RAILS GO DOWN) VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  - 3.1UA (1V8 OFF, RST# LOW)
  - 3.6UA (1V8 ON, RST# LOW)
  - 36UA (1V8 ON, RST# HIGH)

BOM_COST_GROUP=AUDIO

SYNC_MASTER=adrien SYNC_DATE=07/13/2020

PAGE TITLE: AUDIO JACK CODEC

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*** OK2INTEGRATE ***

NOTES:

- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- COPY TEST POINTS FROM PAGE 1 OF THIS REF DESIGN

BOM_COST_GROUP=AUDIO

SYNC_MASTER=davld SYNC_DATE=08/07/2020

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

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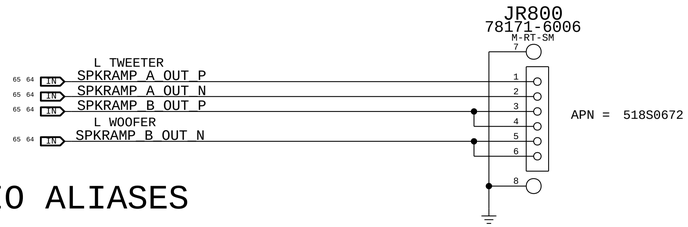
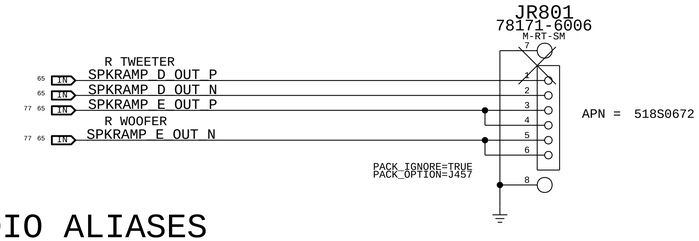
SPEAKER CONNECTOR



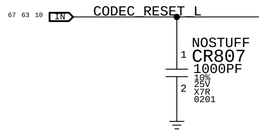
AUDIO ALIASES

SPKRAMP_A_OUT_P	SPKRAMP_A_OUT_P	MAKE_BASE=TRUE
SPKRAMP_A_OUT_N	SPKRAMP_A_OUT_N	MAKE_BASE=TRUE
SPKRAMP_B_OUT_P	SPKRAMP_B_OUT_P	MAKE_BASE=TRUE
SPKRAMP_B_OUT_N	SPKRAMP_B_OUT_N	MAKE_BASE=TRUE



AUDIO ALIASES

SPKRAMP_D_OUT_P	SPKRAMP_D_OUT_P	MAKE_BASE=TRUE
SPKRAMP_D_OUT_N	SPKRAMP_D_OUT_N	MAKE_BASE=TRUE
SPKRAMP_E_OUT_P	SPKRAMP_E_OUT_P	MAKE_BASE=TRUE
SPKRAMP_E_OUT_N	SPKRAMP_E_OUT_N	MAKE_BASE=TRUE

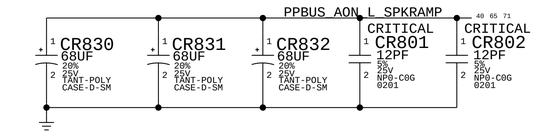


HEAVY THERMAL VIAS
ARRAY TO GND PLANE

0dBFS = 14Vpk

Amplifiers Bulk Capacitance

APN 128S00117



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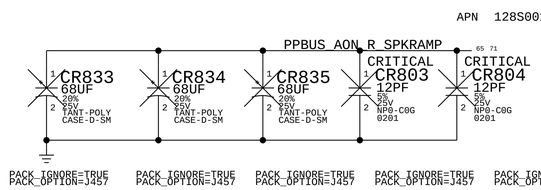

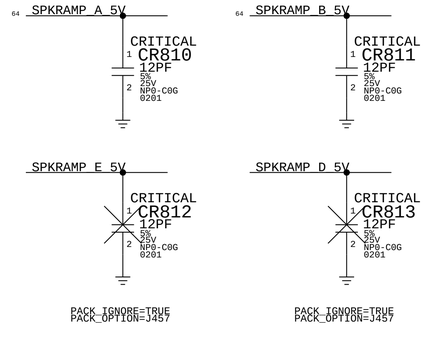

PPBUS_AON_L_SPKRAMP	PPBUS_AON_L_SPKRAMP	
	PPBUS_AON_L_SPKRAMP	
PPBUS_AON_R_SPKRAMP	PPBUS_AON_R_SPKRAMP	
	PPBUS_AON_R_SPKRAMP	

BOM_COST_GROUP=AUDIO

PAGE TITLE: Audio Connectors

Apple Inc.

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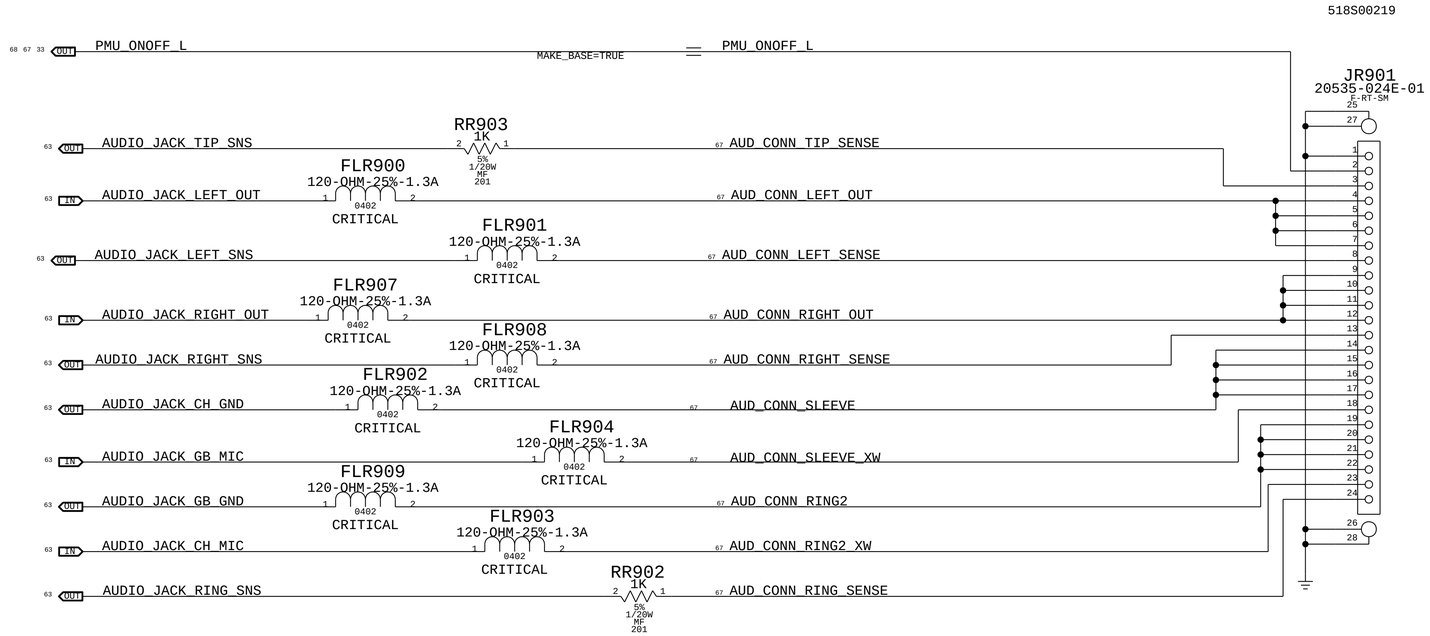
518S00219



AUDIO JACK FLEX CABLE DETECT IS NO LONGER USED

BOM_COST_GROUP=AUDIO

PAGE TITLE
Audio Jack Connector

Apple Inc.

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DFU Test Points	FUNC_TEST	
I2C_SEEPROM_SCL	TRUE	5 7 67
I2C_SEEPROM_SDA	TRUE	5 7 67
PMU_ACTIVE_READY	TRUE	6 33 46 48 68
PMU_ONOFF_L	TRUE	33 66 68
PMU_RESET_L	TRUE	6 10 33 68
PMU_SHDN	TRUE	33
PMU_SYS_ALIVE	TRUE	33 46 57 68 72
PU_PMU_RSLOC_RST_L	TRUE	34
SOC_DFU_STATUS	TRUE	6 45 46 68
SOC_SOCHOT_L	TRUE	7 33 46 69
DFUMUX_SEL	TRUE	69
I2C_SMC_UPC_SCL	TRUE	10 23 39 46
I2C_SMC_UPC_SDA	TRUE	10 23 39 46
KISMUX_SEL	TRUE	69
SOC_DOCK_CONNECT	TRUE	10 69
SOC_FORCE_DFU	TRUE	6 33 46 68
SWD_SOC_SWCLK	TRUE	10 46 69
SWD_SOC_SWDIO	TRUE	10 46 69
TP_SMC_FIXTURE_MODE_L	TRUE	72
UART_DEBUGPRT_D2R	TRUE	7 46 69
UART_DEBUGPRT_R2D	TRUE	7 46 69
UART_SMC_DEBUGPRT_D2R	TRUE	10 46 69
UART_SMC_DEBUGPRT_R2D	TRUE	10 46 69
USB_DBG_LS_N	TRUE	46 69
USB_DBG_LS_P	TRUE	46 69
USB2_ATC0_LS_N	TRUE	46 69
USB2_ATC0_LS_P	TRUE	46 69
GND	TRUE	

Parrot DFU Test Points	FUNC_TEST	
ATCRTMR0_RESET_L		44 45 46
I2C_UPC0_ATCRTMR0_SCL	TRUE	44 46
I2C_UPC0_ATCRTMR0_SDA	TRUE	44 46
PP3V3_S2SW_USBC0	TRUE	45

Power DFU Test Points	FUNC_TEST	
PBUS_CC	TRUE	22 23
PP1V25_S2	TRUE	70
PP1V8_AON	TRUE	70
PP3V3_S2_UPC	TRUE	70
PP3V8_AON_VDDMAIN	TRUE	71
PP5V0_S2	TRUE	71
PPBUS_AON	TRUE	71
PPBUS_AON_DISP	TRUE	71
PPBUS_AON_PORT_CONN	TRUE	22
GND	TRUE	

SOC DFU Test Points	FUNC_TEST	
I2C_SEEPROM_SCL	TRUE	5 7 67
I2C_SEEPROM_SDA	TRUE	5 7 67

CCG3 Port Power DFU Test Points	FUNC_TEST	
I2C_UPC_SCL	TRUE	7 23 38 46
I2C_UPC_SCL_SWDCLK_3V3	TRUE	23
I2C_UPC_SDA	TRUE	7 23 38 46
I2C_UPC_SDA_SWDIO_3V3	TRUE	23
GND	TRUE	

Audio FCT Test Points	FUNC_TEST	
AUD_CONN_LEFT_OUT	TRUE	66
AUD_CONN_LEFT_SENSE	TRUE	66
AUD_CONN_RIGHT_OUT	TRUE	66
AUD_CONN_RIGHT_SENSE	TRUE	66
AUD_CONN_RING_SENSE	TRUE	66
AUD_CONN_RING2	TRUE	66
AUD_CONN_RING2_XW	TRUE	66
AUD_CONN_SLEEVE	TRUE	66
AUD_CONN_SLEEVE_XW	TRUE	66
AUD_CONN_TIP_SENSE	TRUE	66
DMIC_CLK3_1V8_OUT	TRUE	56 61
DMIC_CLK4_1V8_OUT	TRUE	56 61
DMIC_DATA3_1V8_IN	TRUE	56 61
DMIC_DATA4_1V8_IN	TRUE	56 61
GND_AUDIO_CODEC	TRUE	63
I2C_SPKRAMP_L_SCL	TRUE	7 38 67
I2C_SPKRAMP_L_SDA	TRUE	7 38 67
SPKRAMP_A_OUT_N	TRUE	65
SPKRAMP_A_OUT_P	TRUE	65
SPKRAMP_B_OUT_N	TRUE	65
SPKRAMP_B_OUT_P	TRUE	65

SOC Test Points	FUNC_TEST	
TP_TST_CLKOUT	TRUE	6

BKLT FCT Test Points	FUNC_TEST	
BL_EN_R	TRUE	59
BL_PWR_ON_R	TRUE	59
PPVIN_BKLT_PWR	TRUE	58 59 60
BKLT_BOOST_1	TRUE	60
BKLT_BOOST_2	TRUE	60
LED_RETURN_1	TRUE	60
LED_RETURN_2	TRUE	60
LED_RETURN_3	TRUE	60
LED_RETURN_4	TRUE	60
LED_RETURN_5	TRUE	60
LED_RETURN_6	TRUE	60
LED_RETURN_7	TRUE	60
LED_RETURN_8	TRUE	60

Camera FCT Test Points	FUNC_TEST	
I2C_CAM_SCL_1V8	TRUE	38 57
I2C_CAM_SDA_1V8	TRUE	38 57
FTCAM_ENABLE_1V8_OUT	TRUE	57 61
I2C_AOP_CAMALS_SCL	TRUE	38 57
I2C_AOP_CAMALS_SDA	TRUE	38 57
I2C_CAMALS_INT_L	TRUE	38 57
MIPI_FTCAM_CLK_N	TRUE	8 57
MIPI_FTCAM_CLK_P	TRUE	8 57
MIPI_FTCAM_DATA_N<0>	TRUE	8 57
MIPI_FTCAM_DATA_N<1>	TRUE	8 57
MIPI_FTCAM_DATA_P<0>	TRUE	8 57
MIPI_FTCAM_DATA_P<1>	TRUE	8 57
PP5V_S2_CAMERA	TRUE	57

Display FCT Test Points	FUNC_TEST	
EDP_PANEL_PWR	TRUE	57
LCD_PWR_EN	TRUE	34 57
LPDP_INT_HPD	TRUE	8 57
SPI_TCON_CS_L	TRUE	7 57
SPI_TCON_MISO	TRUE	7 57
SPI_TCON_MOSI	TRUE	20 57
SPI_TCON_SCLK	TRUE	20 57
TP_DISP_SWCLK	TRUE	72
TP_DISP_SWDIO	TRUE	72
UART_TCON_D2R	TRUE	20 57
UART_TCON_R2D	TRUE	20 57

FAN0 FCT/Mac-1 Test Points	FUNC_TEST	
I2C_SMC_FAN0_SCL_3V3	TRUE	39 43
I2C_SMC_FAN0_SDA_3V3	TRUE	39 43
PP15V8_FAN0_FILT	TRUE	43
FAN_PWR_EN	TRUE	33 34 43
GND	TRUE	

FAN1 FCT/Mac-1 Test Points	FUNC_TEST	
I2C_SMC_FAN1_SCL_3V3	TRUE	39 43
I2C_SMC_FAN1_SDA_3V3	TRUE	39 43
PP15V8_FAN1_FILT	TRUE	43
GND	TRUE	

NAND FCT Test Points	FUNC_TEST	
TP_NAND0_S5E0_ANI0_VREF	TRUE	53
TP_NAND0_S5E0_ANI1_VREF	TRUE	53
TP_NAND0_S5E1_ANI0_VREF	TRUE	54
TP_NAND0_S5E1_ANI1_VREF	TRUE	54

SOC Power FCT Test Points	FUNC_TEST	
PP0V6_S1_VDDQL	TRUE	70
PP0V72_S2_VDD_LOW	TRUE	70
PP0V76_S1_SRAM	TRUE	70
PP0V805_S1_VDD_FIXED	TRUE	70
PP0V855_S2SW_CIO	TRUE	70
PP0V88_AWAKESW_NAND	TRUE	70
PP0V88_S1	TRUE	70
PP1V06_S2SW_DRAM	TRUE	70
PP1V2_AWAKE_IO	TRUE	70
PP1V2_AWAKE_PLL	TRUE	70
PP1V2_S2	TRUE	70
PP1V2_S2_CIO	TRUE	70
PP1V225_AWAKESW_VCCQ	TRUE	70
PP1V4_LDO_PREREG	TRUE	70
PP1V8_AWAKE	TRUE	70
PP1V8_S2	TRUE	70
PP2V5_AWAKESW_NANDVCC	TRUE	70
PP3V0_RTC	TRUE	70
PP3V3_S2SW_USBC1	TRUE	45
PPVDD_CPU_SRAM_AWAKE	TRUE	70
PPVDD_ECPU_AWAKE	TRUE	70
PPVDD_GPU_AWAKE	TRUE	70
PP3V3_S2_REG_SNS	TRUE	71

SOC Sense FCT Test Points	FUNC_TEST	
TP_VSNS_VDD_DCS	TRUE	72
TP_VSNS_VDD_DISP	TRUE	72
TP_VSNS_VDD_PCPU	TRUE	72
TP_VSNS_VDD_SOC	TRUE	72

Audio Test Points	NEED_TP	
CODEC_RESET_L	TRUE	10 63 65
CODEC_INT_L	TRUE	7 63
CODEC_WAKE_L	TRUE	33 63
I2C_SPKRAMP_L_SCL_1V8	TRUE	38
I2C_SPKRAMP_L_SDA_1V8	TRUE	38
TDM_1V8_SPKRAMP_L_BCLK	TRUE	62 72
TDM_1V8_SPKRAMP_L_FSYNC	TRUE	62 72
TDM_1V8_SPKRAMP_L_R2D	TRUE	62 72
TDM_CODEC_BCLK	TRUE	20 63
TDM_CODEC_D2R	TRUE	7 63
TDM_CODEC_FSYNC	TRUE	20 63
TDM_CODEC_R2D	TRUE	20 63

BKLT Test Points	NEED_TP	
BKLT_BOOST	TRUE	58 60
BL_CS_R	TRUE	59
BL_MISO_R	TRUE	59
BL_MOSI_R	TRUE	59
BL_SCLK_R	TRUE	59

Camera Test Points	NEED_TP	
FTCAM_RESET_L	TRUE	8 61

CCG3 Test Points	NEED_TP	
CCG_I2C_INT_L	TRUE	7 38
CCG_SMC_I2C_INT_L	TRUE	10 39
CCG3_XRES	TRUE	23
PP_VCCD	TRUE	23
PP_VDDD	TRUE	22 23

Display Test Points	NEED_TP	
I2C_SMC_SNS1_SCL	TRUE	10 39
I2C_SMC_SNS1_SDA	TRUE	10 39
SPI_DISP_BKLT_CS_L	TRUE	20 59
SPI_DISP_BKLT_MISO	TRUE	8 59
SPI_DISP_BKLT_MOSI	TRUE	20 59
SPI_DISP_BKLT_SCLK	TRUE	20 59

ENET Test Points	NEED_TP	
ENET_RESET_L	TRUE	9 48
ENET_WAKE_L	TRUE	34 48
ENET_SR_LX	TRUE	47 48

Fan Test Points	NEED_TP	
PP15V8_FAN0_FET	TRUE	43
PP15V8_FAN1_FET	TRUE	43
TP_FAN0_PWM	TRUE	43
TP_FAN0_TACH	TRUE	43
TP_FAN1_PWM	TRUE	43
TP_FAN1_TACH	TRUE	43

NAND Test Points	NEED_TP	
NAND_BEH	TRUE	7 53 54
NAND0_BOOT2	TRUE	53 54
NAND0_CLKREQ0_L	TRUE	9 20
NAND0_CLKREQ1_L	TRUE	9 20
NAND0_JTAG_SEL	TRUE	53 54
NAND0_JTAG_TRST_L	TRUE	53 54
NAND0_LPB_L	TRUE	33 53 54
NAND0_RESET_L	TRUE	7 53 54
NAND0_S5E0_JTAG_TDO	TRUE	53 54
P2V5_NAND0_DISCHARGE_EN	TRUE	33 55
SWD_NAND0_SWCLK	TRUE	6 72
SWD_NAND0_SWDIO	TRUE	6 72
TP_NAND0_S5E0_DROOP_L	TRUE	53
TP_NAND0_S5E0_JTAG_TDI	TRUE	53
TP_NAND0_S5E0_VPP	TRUE	53
TP_NAND0_S5E1_VPP	TRUE	54
TP_NAND0_S5E1_DROOP_L	TRUE	54
NAND0_WP_L	TRUE	53 54

PMIC Test Points	NEED_TP	
MPMU_FAULT_OUT_L	TRUE	33
MPMU_VLDORTC	TRUE	33
P3V3_S2_PWR_EN	TRUE	33 36
P5V_S2_PWR_EN_IBOOT	TRUE	35
P5V_S2_PWR_EN_PWRSEQ	TRUE	34 35
PMU_RESET_1V8	TRUE	33 34 46
PMU_VDD_HI	TRUE	31 40
SE_PWR_EN	TRUE	21 33
SPMU_RESET_IN	TRUE	29 30
PMU_CRASH_L	TRUE	33
SWD_NUB_PMU_SWDIO	TRUE	10 29 33
SWD_NUB_SWCLK	TRUE	10 29 33
TP_AON_SLEEP1_RESET_L	TRUE	10

Power Test Points	NEED_TP	
P15V8AON_PRE_UPO_L	TRUE	25 34
P3V8AON_EXTVCC	TRUE	26
P3V8AON_SGND	TRUE	26
PP1V5_VLDOINT_MPMU	TRUE	31 32 33
PP1V5_VLDOINT_SPMU	TRUE	27 28
PP1V8_AWAKE_SPMU_GPIO	TRUE	28
PP1V8_S2SW_VDD1	TRUE	71
PP2V5_S2	TRUE	70
PP3V3_S2SW_ENET	TRUE	50
PP3V8_AON_VDDMAIN_MPMU	TRUE	71
PP3V8_AON_VDDMAIN_SPMU	TRUE	71
PP3V8_CODEC_VP	TRUE	63
PP5V_BSTLQ_VOUT_MPMU	TRUE	33
PP5V_BSTLQ_VOUT_SPMU	TRUE	28
PPBUS_AON_PORT	TRUE	22 23
PPVBATT_AON_RTC	TRUE	24
PPVDD_DCS_S1	TRUE	70
PPVDD_DISP_S1	TRUE	70
PPVDD_PCPU_AWAKE	TRUE	70
PPVDD_PMU_LDO_PREREG	TRUE	70
PPVDD_SOC_S1	TRUE	70
P3V8AON_INTVCC_5V	TRUE	26
P3V8AON_VOSNS	TRUE	26
VSS_ANA_MPMU	TRUE	34
VSS_ANA_SPMU	TRUE	30

Pwr Ctrl Test Points	NEED_TP	
BL_SD	TRUE	58 59
ENET_PWR_EN	TRUE	34 50
P3V3_S2_PGOOD	TRUE	36
P5V_S2_SYS_EN	TRUE	35
PBUS_PORT_EFUSE_EN_3V3	TRUE	22 23
PBUS_PORT_EFUSE_IMON	TRUE	22
PBUS_PORT_EFUSE_PGOOD	TRUE	22 23 26 68
PBUS_PORT_EFUSE_PWROK	TRUE	22
PP1V2_ENET_INTREG	TRUE	48
PSU_2MS_OC_ASSERT_L	TRUE	25
PSU_2MS_OC_DET	TRUE	25
PSU_2MS_OC_DET_L	TRUE	25
PSU_FAST_OC_ASSERT_L	TRUE	25
PSU_FAST_OC_DET_L	TRUE	25
PU_P5V_S2_SYS_PGOOD	TRUE	71
PVDD1_PWR_EN	TRUE	33 37
SOC_HOLD_RESET	TRUE	5 6
P15V8_AON_ILIMIT_L	TRUE	25 34
P15V8AON_PRE_UPO_L_R	TRUE	25
P3V3_S2_EN	TRUE	36
P3V8AON_VIN	TRUE	26
PBUS_PORT_EFUSE_ILIM	TRUE	22
PBUS_PORT_EFUSE_ITIMER	TRUE	22
PBUS_PORT_EFUSE_LDSTRT	TRUE	22
PBUS_PORT_EFUSE_UVLO	TRUE	22
PP1V225_AWAKESW_SNS	TRUE	70
PSU_2MS_OC_TRIGGER	TRUE	25
PSU_AVE_OC_IN_NEG	TRUE	25
PSU_FAST_OC_IN_NEG	TRUE	25
PSU_FAST_OC_TRIGGER	TRUE	25
PSU_OC_REF	TRUE	25
TP_PM_P3V8AON_FAULT_L	TRUE	72

Pwr Ctrl Test Points	NEED_TP	
PDM_DMIC_CLK3	TRUE	10 61
PDM_DMIC_CLK4	TRUE	10 61
PDM_DMIC_DATA3	TRUE	10 61
PDM_DMIC_DATA4	TRUE	10 61

Sensor Test Points	NEED_TP	
TP_VSNS_VDD_ECPU	TRUE	72
TP_VSNS_VDD_GPU	TRUE	72
TP_VSNS_VDD2_1	TRUE	72
TP_VSNS_VDD2_2	TRUE	72
TP_VSNS_VDDQL	TRUE	72
TP_VSNS_VSS_1	TRUE	72
TP_VSNS_VSS_2	TRUE	72
TP_VSNS_VSS_DDR	TRUE	72
TP_VSNS_VSS_PCPU	TRUE	72

SOC Test Points	NEED_TP	
DEBUG_JTAG_SOC_TDI	TRUE	20 69
DEBUG_JTAG_SOC_TDO	TRUE	20 69
SOC_JTAG_SEL	TRUE	5 10
SOC_TESTMODE	TRUE	5 6
SPI_SOCROM_1V8_MISO_R	TRUE	19
TP_JTAG_SOC_TRST_L	TRUE	10
TP_NAND0_S5E1_JTAG_TDO	TRUE	72
TP_SOC_AMUX_OUT	TRUE	72
TP_SOC_SW_DBG	TRUE	72
USB_VBUS_DETECT	TRUE	6

USB-C Test Points	NEED_TP	
ATCRTMR0_RESET_1V8_L	TRUE	44 69
ATCRTMR0_RESET_MUX_1V8_L	TRUE	45
ATCRTMR1_RESET_1V8_L	TRUE	44
ATCRTMR1_RESET_L	TRUE	44 46
I2C_UPC0_ATCRTMR0_SCL_1V8	TRUE	44
I2C_UPC0_ATCRTMR0_SDA_1V8	TRUE	44
I2C_UPC1_ATCRTMR1_SCL	TRUE	44 46
I2C_UPC1_ATCRTMR1_SCL_1V8	TRUE	44
I2C_UPC1_ATCRTMR1_SDA	TRUE	44 46
I2C_UPC1_ATCRTMR1_SDA_1V8	TRUE	44
I2C_SMC_SNS0_SCL	TRUE	10 39
I2C_SMC_SNS0_SDA	TRUE	10 39
SWD_UPC_SWCLK	TRUE	7 23 46
SWD_UPC_SWCLK_3V3	TRUE	23
SWD_UPC_SWDIO1	TRUE	7 23
SWD_UPC_SWDIO1_3V3	TRUE	23
UPC_FORCE_PWR	TRUE	7 46
UPC_I2C_INT_R_L	TRUE	38 46
USBC_ATC0_AUX_N	TRUE	6 46
USBC_ATC0_AUX_P	TRUE	6 46

WiFi Test Points	NEED_TP	
TP_WLAN_JTAG_TCK	TRUE	51
TP_WLAN_JTAG_TDI	TRUE	51 52
TP_WLAN_JTAG_TDO	TRUE	51 52
TP_WLAN_JTAG_TMS	TRUE	51
TP_WLAN_JTAG_TRSTN	TRUE	51
WLAN_JTAG_SEL	TRUE	51
BT_TIME_SYNC_1V8	TRUE	7 51 52
PCIE_CLK100M_WLBT_N	TRUE	9 51
PCIE_CLK100M_WLBT_P	TRUE	9 51
PCIE_WLBT_D2R_N	TRUE	9 51
PCIE_WLBT_D2R_P	TRUE	9 51
PMU_CLK32K_WLBT	TRUE	33 51 52
UART_WLAN_D2R	TRUE	7 51
UART_WLAN_D2R_CTS_L	TRUE	7 51
UART_WLAN_R2D	TRUE	7 51
UART_WLAN_R2D_RTS_L	TRUE	7 51
WLAN_CONTEXT_A	TRUE	10 51 52
WLAN_CONTEXT_B	TRUE	10 51 52
WLAN_TIME_SYNC_1V8	TRUE	51 52
WLBT_CLKREQ_L	TRUE	9 51 52
WLBT_PWR_EN	TRUE	33 51 52
WLBT_RESET_L	TRUE	9 51 52
WLBT_WAKE	TRUE	33 51 52

53 9 IN PCIE_CLK100M_NAND0_0_P 1 PP P4MM SM PPN000
53 9 IN PCIE_CLK100M_NAND0_0_N 1 PP P4MM SM PPN001

PCIE_CLK100M_NAND0_1_P	TRUE	9 54	
PCIE_CLK100M_NAND0_1_N	TRUE	9 54	

ENET FCT Test Points	FUNC_TEST	
ENETCONN_MDI_T_P<0>	TRUE	22 49
ENETCONN_MDI_T_N<0>	TRUE	22 49
ENETCONN_MDI_T_P<1>	TRUE	22 49
ENETCONN_MDI_T_N<1>	TRUE	22 49
ENETCONN_MDI_T_P<2>	TRUE	22 49
ENETCONN_MDI_T_N<2>	TRUE	22 49
ENETCONN_MDI_T_P<3>	TRUE	22 49
ENETCONN_MDI_T_N<3>	TRUE	22 49
PBUS_PORT_EFUSE_EN_R_3V3	TRUE	23

67 38 7 IN I2C_SPKRAMP_L_SCL 1 PP P4MM SM PPD000
67 38 7 IN I2C_SPKRAMP_L_SDA 1 PP P4MM SM PPD001

BOM_COST_GROUP=DEBUG

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Apple Inc.

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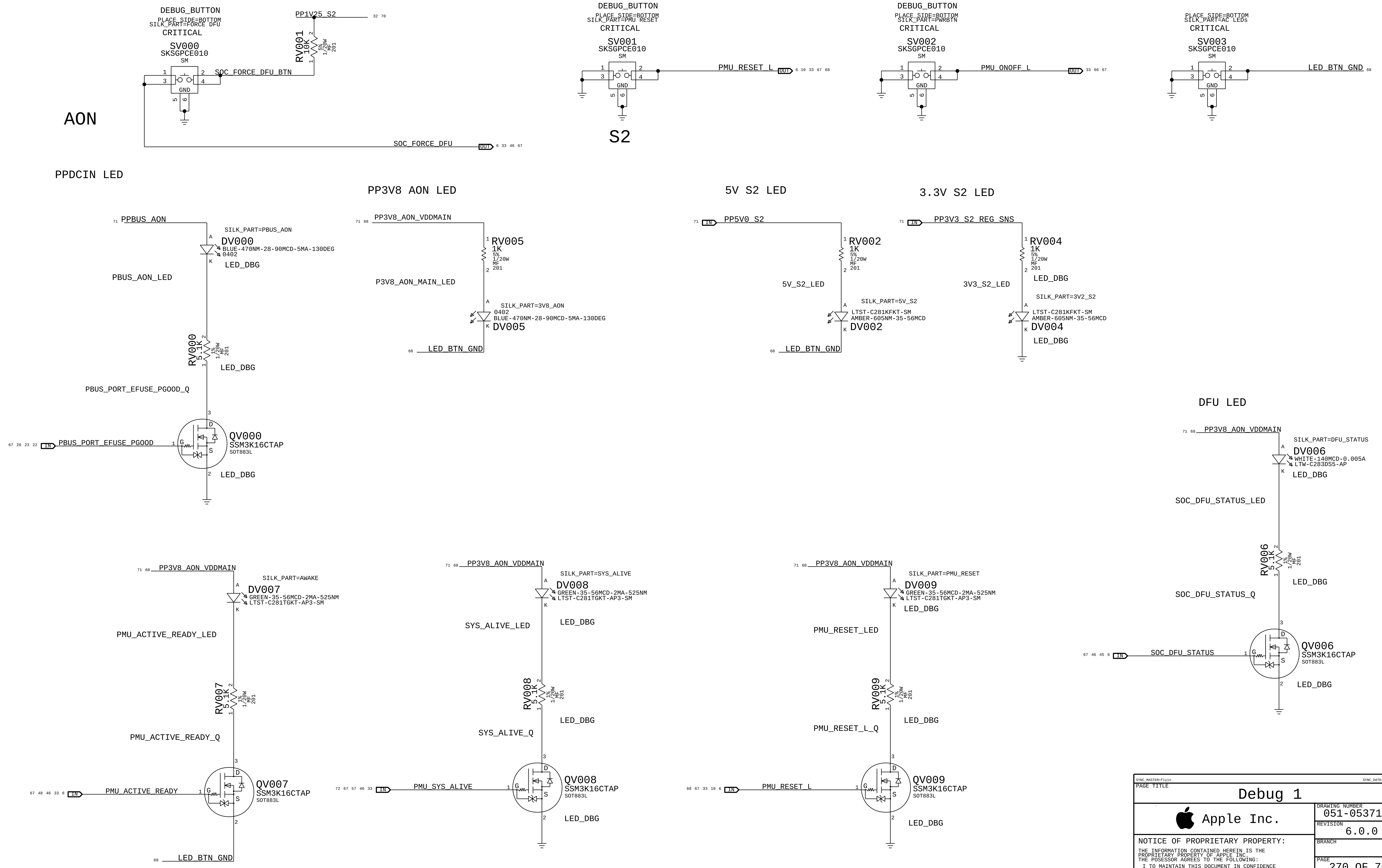
Debug Buttons and LEDs



DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=FORCE DFU
CRITICAL
SV000
SKSGPCE010
SM
GND
SOC_FORCE_DFU_BTN
PP1V25_S2
32 70
RV001
10K
5%
1/20W
MF
201
AON
SOC_FORCE_DFU
OUT
6 33 46 67
DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=PMU RESET
CRITICAL
SV001
SKSGPCE010
PMU_RESET_L
6 10 33 67 68
S2
DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=PWRBTN
CRITICAL
SV002
SKSGPCE010
PMU_ONOFF_L
33 66 67
PLACE_SIDE=BOTTOM
SILK_PART=AC LEDs
CRITICAL
SV003
SKSGPCE010
LED_BTN_GND
68
PPDCIN LED
PP3V8 AON LED
5V S2 LED
3.3V S2 LED
PPBUS_AON
SILK_PART=PBUS_AON
DV000
BLUE-470NM-28-90MCD-5MA-130DEG
0402
LED_DBG
PBUS_AON_LED
RV000
5.1K
1%
1/20W
MF
201
PBUS_PORT_EFUSE_PGOOD_Q
67 26 23 22
IN
PBUS_PORT_EFUSE_PGOOD
QV000
SSM3K16CTAP
SOT883L
PP3V8_AON_VDDMAIN
71 68
RV005
1K
5%
1/20W
MF
201
P3V8_AON_MAIN_LED
SILK_PART=3V8_AON
0402
BLUE-470NM-28-90MCD-5MA-130DEG
DV005
LED_BTN_GND
PP5V0_S2
RV002
1K
5V_S2_LED
SILK_PART=5V_S2
LTST-C281KFKT-SM
AMBER-605NM-35-56MCD
DV002
PP3V3_S2_REG_SNS
RV004
1K
3V3_S2_LED
SILK_PART=3V2_S2
DV004
DFU LED
PP3V8_AON_VDDMAIN
SILK_PART=DFU_STATUS
DV006
WHITE-140MCD-0.005A
LTW-C283DS5-AP
SOC_DFU_STATUS_LED
RV006
5.1K
SOC_DFU_STATUS_Q
67 46 45 6
SOC_DFU_STATUS
QV006
SSM3K16CTAP
SOT883L
SILK_PART=AWAKE
DV007
GREEN-35-56MCD-2MA-525NM
LTST-C281TGKT-AP3-SM
PMU_ACTIVE_READY_LED
RV007
5.1K
PMU_ACTIVE_READY_Q
67 48 46 33 6
PMU_ACTIVE_READY
QV007
SSM3K16CTAP
SOT883L
SILK_PART=SYS_ALIVE
DV008
GREEN-35-56MCD-2MA-525NM
LTST-C281TGKT-AP3-SM
SYS_ALIVE_LED
RV008
5.1K
SYS_ALIVE_Q
72 67 57 46 33
PMU_SYS_ALIVE
QV008
SSM3K16CTAP
SOT883L
SILK_PART=PMU_RESET
DV009
GREEN-35-56MCD-2MA-525NM
LTST-C281TGKT-AP3-SM
PMU_RESET_LED
RV009
5.1K
PMU_RESET_L_Q
68 67 33 10 6
PMU_RESET_L
QV009
SSM3K16CTAP
SOT883L

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NOTICE OF PROPRIETARY PROPERTY:

SOC USB DFU MUX

20K LIMITS USB MINI-B
FROM BACK POWERING MLB

71 PP3V3_S2_REG_SNS
VITAMIN-C:YES
RX412 20K 5% 1/20W MF 201

VITAMIN-C:YES
BYPASS=UX410::5MM
CX410 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S2_DFUMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1000

VITAMIN-C:YES
RX410 100K 5% 1/20W MF 201

VIT-C CONN

69 USB2_ATC0_LS_VITAMINC_P
69 USB2_ATC0_LS_VITAMINC_N
67 46 BI USB2_ATC0_LS_P
67 46 BI USB2_ATC0_LS_N

DEBUG SPI ACE

UX410
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES

VCC 9 · 2UA MAX IDD
GND 3

M+ 5 · M- 4 · D+ 7 · D- 6 · OE* 8

LVL SHFTR

Y+ 1 USB2_ATC0_LS_MUX_P → BI 44 45
Y- 2 USB2_ATC0_LS_MUX_N → BI 44 45

SEL 10 → DFUMUX_SEL → 67 69

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

VITAMIN-C:NO RX414 0 1 2
NO_XNET_CONNECTION=1 0201 MF 5% 1/20W

VITAMIN-C:NO RX416 0 1 2
NO_XNET_CONNECTION=1 0201 MF 5% 1/20W

SOC DBG MUX

20K LIMITS USB MINI-B
FROM BACK POWERING MLB

71 PP3V3_S2_REG_SNS
VITAMIN-C:YES
RX413 20K 5% 1/20W MF 201

VITAMIN-C:YES
BYPASS=UX411::5MM
CX411 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S2_DBGMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1000

VITAMIN-C:YES
RX411 100K 5% 1/20W MF 201

VIT-C CONN

69 USB_DBG_LS_VITAMINC_P
69 USB_DBG_LS_VITAMINC_N
67 46 BI USB_DBG_LS_P
67 46 BI USB_DBG_LS_N

DEBUG SPI ACE

UX411
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES

VCC 9 · 2UA MAX IDD
GND 3

M+ 5 · M- 4 · D+ 7 · D- 6 · OE* 8

LVL SHFTR

Y+ 1 USB_DBG_LS_MUX_P → BI 44 45
Y- 2 USB_DBG_LS_MUX_N → BI 44 45

SEL 10 → KISMUX_SEL → 67 69

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

VITAMIN-C:NO RX415 0 1 2
NO_XNET_CONNECTION=1 0201 MF 5% 1/20W

VITAMIN-C:NO RX417 0 1 2
NO_XNET_CONNECTION=1 0201 MF 5% 1/20W

PARROT DBG MUX

20K LIMITS USB MINI-B
FROM BACK POWERING MLB

71 PP3V3_S2_REG_SNS
VITAMIN-C:YES
RX418 20K 5% 1/20W MF 201

VITAMIN-C:YES
BYPASS=UX412::5MM
CX415 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S2_PRTMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1000

VIT-C CONN

69 VITC_RTMR_RESET_L
69 VITC_RTMR_PWR_EN
67 44 BI ATCRTMR0_RESET_1V8_L
72 BI UNUSED_USBC0_3V3_LDO_EN

DEBUG SPI ACE

UX412
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES

VCC 9 · 2UA MAX IDD
GND 3

M+ 5 · M- 4 · D+ 7 · D- 6 · OE* 8

LVL SHFTR

Y+ 1 ATCRTMR0_RESET_MUX_1V8_L → BI 44 45
Y- 2 UNUSED_USBC0_3V3_LDO_EN_VITC → BI 72

SEL 10 → DFUMUX_SEL → 67 69

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

VITAMIN-C:NO RX420 1K 1 2
NO_XNET_CONNECTION=1 201 MF 5% 1/20W

VITAMIN-C:NO RX421 0 1 2
NO_XNET_CONNECTION=1 0201 MF 5% 1/20W

VITAMIC-C MK2 CONNECTOR

516S1074
SILK_PART=VITAMIN-C
VITAMIN-C:YES
JX401
AA25D-S038VA1
F-ST-SM

SOC ATC0 DFU

69 USB2_ATC0_LS_VITAMINC_P
69 USB2_ATC0_LS_VITAMINC_N
69 USB_DBG_LS_VITAMINC_P
69 USB_DBG_LS_VITAMINC_N

SOC KIS DBG

RFU
RFU
RFU

1	2	SOC_SOCHOT_L	OUT 7 33 46 67
3	4	DFUMUX_SEL	67 69
5	6	KISMUX_SEL	67 69
7	8	SOC_DOCK_CONNECT_VITAMINC	69
9	10	TP_DC_MUX_SEL	
11	12	SWD_SOC_SWDIO	BI 10 46 67
13	14	SWD_SOC_SWCLK	OUT 10 46 67
15	16	DEBUG_JTAG_SOC_TDO	IN 20 67
17	18	DEBUG_JTAG_SOC_TDI	OUT 20 67
19	20	UART_DEBUGPRT_R2D	IN 7 46 67
21	22	UART_DEBUGPRT_D2R	OUT 7 46 67
23	24	UART_SMC_DEBUGPRT_R2D	IN 10 46 67
25	26	UART_SMC_DEBUGPRT_D2R	OUT 10 46 67
27	28	VITC_RTMR_RESET_L	69
29	30	VITC_RTMR_PWR_EN	69
31	32	PP1V8_S2	70
33	34	PP1V25_S2	70
35	36		
37	38		
41	42	PP5V0_S2	71

KOBA
SOC UART
SMC UART

71 PP3V8_AON_VDDMAIN

VITAMIN-C:YES CX405 0.1UF 10% 10V X5R-CERM 0201
BYPASS=JX401::5MM

VITAMIN-C:YES CX406 0.1UF 10% 10V X5R-CERM 0201
BYPASS=JX401::5MM

VITAMIN-C:YES CX404 2.2UF 20% 25V X6S-CERM 0402
BYPASS=JX401::5MM

VITAMIN-C:YES CX460 1.0UF 20% 6.3V X5R 0201-1
BYPASS=JX401::5MM

VITAMIN-C:YES CX401 0.1UF 10% 10V X5R-CERM 0201

VITAMIN-C:YES CX402 0.1UF 10% 10V X5R-CERM 0201
BYPASS=JX401::5MM

VITAMIN-C:YES CX403 0.1UF 10% 10V X5R-CERM 0201
BYPASS=JX401::5MM

DOCK CONNECT

TO SOC
1V2 NUB AOP, S2

67 10 OUT SOC_DOCK_CONNECT

FROM ACE GPIO 7, PMOS OPEN DRAIN
1V2 S2
RX491 100 5% 1/20W MF 201
SOC_DOCK_CONNECT_UPC → IN 46

VITAMIN-C:YES
FROM VITAMIN C
1V2 S2
RX492 10 5% 1/20W MF 201
SOC_DOCK_CONNECT_VITAMINC → 69

BOM_COST_GROUP=DEBUG

SYNC_MASTER=michael SYNC_DATE=10/16/2019
PAGE TITLE
DEBUG: VITAMIN-C

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PMIC POWER CONNECTIONS

SERA BUCK0

67 PPVDD_PCPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_PCPU_AWAKE 31
→ PPVDD_PCPU_AWAKE 13 18

SERA BUCK1

67 PPVDD_GPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_GPU_AWAKE 31 34
→ PPVDD_GPU_AWAKE 13 18

SERA BUCK2

67 PPVDD_SOC_S1
MAKE_BASE=TRUE
VOLTAGE=0.85V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_SOC_S1 31
→ PPVDD_SOC_S1 13 34

SERA BUCK3

67 PP1V8_S2
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V8_S2 32
→ PP1V8_S2 59
→ PP1V8_S2 57
→ PP1V8_S2 56
→ PP1V8_S2 44
→ PP1V8_S2 44
→ PP1V8_S2 38 39
(SERA BUCK SW1 INPUT)
→ PP1V8_S2 26 32
(P1V8 SWITCH INPUT)
→ PP1V8_S2 37
→ PP1V8_S2 21
→ PP1V8_S2 61
(SIMETRA SW4 INPUT)
→ PP1V8_S2 28
→ PP1V8_S2 44
→ PP1V8_S2 44
→ PP1V8_S2 69
→ PP1V8_S2 51
(SIMETRA IO)
→ PP1V8_S2 27
(SERA IO)
→ PP1V8_S2 31
J456
→ PP1V8_S2 46 72
J457
→ PP1V8_S2 72

SERA BUCK7

67 PPVDD_CPU_SRAM_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.001V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_CPU_SRAM_AWAKE 32
→ PPVDD_CPU_SRAM_AWAKE 14 18

SERA BUCK8

67 PPVDD_DISP_S1
MAKE_BASE=TRUE
VOLTAGE=1.01V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_DISP_S1 32
→ PPVDD_DISP_S1 13 18

SERA BUCK9

67 PPVDD_DCS_S1
MAKE_BASE=TRUE
VOLTAGE=0.842V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_DCS_S1 32
→ PPVDD_DCS_S1 14 18

SERA BUCK11

67 PPVDD_ECPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=0.93V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PPVDD_ECPU_AWAKE 32
→ PPVDD_ECPU_AWAKE 13 18

SERA BUCK14

67 PP1V4_LDO_PREREG
MAKE_BASE=TRUE
VOLTAGE=1.4V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V4_LDO_PREREG 34
→ PP1V4_LDO_PREREG 34

SERA LD01

67 PP2V5_S2
MAKE_BASE=TRUE
VOLTAGE=2.5V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP2V5_S2 34

SERA LD03

67 PP1V2_S2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V2_S2 33

SERA LD07

67 PP3V3_S2_UPC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP3V3_S2_UPC 33
J456
→ PP3V3_S2_UPC 46 72
J457
→ PP3V3_S2_UPC 72

SERA LD09

67 PP1V8_AON
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V8_AON 33
→ PP1V8_AON 29 33 34

SERA RTC

67 PP3V0_RTC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP3V0_RTC 24
→ PP3V0_RTC 31

SERA BUCK SW1

67 PP1V8_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V8_AWAKE 26 32
→ PP1V8_AWAKE 63
→ PP1V8_AWAKE 12
→ PP1V8_AWAKE 38
→ PP1V8_AWAKE 19
→ PP1V8_AWAKE 19
→ PP1V8_AWAKE 5
→ PP1V8_AWAKE 46 62 64

SERA BUCK SW3

67 PP1V2_AWAKE_IO
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V2_AWAKE_IO 32
→ PP1V2_AWAKE_IO 63
→ PP1V2_AWAKE_IO 15
→ PP1V2_AWAKE_IO 5 6 7 9 12
→ PP1V2_AWAKE_IO 38
→ PP1V2_AWAKE_IO 25 34 56 62 63
→ PP1V2_AWAKE_IO 15
→ PP1V2_AWAKE_IO 19
→ PP1V2_AWAKE_IO 15
→ PP1V2_AWAKE_IO 15
→ PP1V2_AWAKE_IO 5
→ PP1V2_AWAKE_IO 46 72
→ PP1V2_AWAKE_IO 15
→ PP1V2_AWAKE_IO 15

SIMETRA BUCK4

67 PP1V06_S2SW_DRAM
MAKE_BASE=TRUE
VOLTAGE=1.06V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V06_S2SW_DRAM 27
→ PP1V06_S2SW_DRAM 11 18
(SIMETRA LDO11 INPUT)
→ PP1V06_S2SW_DRAM 28

SIMETRA BUCK5

67 PP0V76_S1_SRAM
MAKE_BASE=TRUE
VOLTAGE=0.76V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V76_S1_SRAM 27
→ PP0V76_S1_SRAM 14 18

SIMETRA BUCK6

67 PP2V5_AWAKESW_NANDVCC
MAKE_BASE=TRUE
VOLTAGE=2.5V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP2V5_AWAKESW_NANDVCC 27
→ PP2V5_AWAKESW_NANDVCC 53 54 55

SIMETRA BUCK10

67 PP0V6_S1_VDDQL
MAKE_BASE=TRUE
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V6_S1_VDDQL 27
→ PP0V6_S1_VDDQL 11 18

SIMETRA BUCK12

67 PP0V88_S1
MAKE_BASE=TRUE
VOLTAGE=0.88V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V88_S1 27
→ PP0V88_S1 28

SIMETRA BUCK13

67 PP1V25_S2
MAKE_BASE=TRUE
VOLTAGE=1.225V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
<rdar://57602463> ->
→ PP1V25_S2 27
→ PP1V25_S2 33
→ PP1V25_S2 15
→ PP1V25_S2 10 12
→ PP1V25_S2 59
→ PP1V25_S2 63
→ PP1V25_S2 48
→ PP1V25_S2 12
→ PP1V25_S2 23 38 39
→ PP1V25_S2 44
(SERA SW3 INPUT)
→ PP1V25_S2 32 68
→ PP1V25_S2 21
(SIMETRA SW5 INPUT)
→ PP1V25_S2 61
→ PP1V25_S2 28 29
→ PP1V25_S2 15
→ PP1V25_S2 15
→ PP1V25_S2 69
→ PP1V25_S2 51
(SERA IO)
→ PP1V25_S2 31
(SIMETRA IO)
→ PP1V25_S2 27
(LDO PREREG SELECT)
→ PP1V25_S2 34
(SIMETRA LDO4 INPUT)
→ PP1V25_S2 28
J456
→ PP1V25_S2 46 72
J457
→ PP1V25_S2 72

SIMETRA BUCK SW5

67 PP1V225_AWAKESW_VCCQ
MAKE_BASE=TRUE
VOLTAGE=1.225V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V225_AWAKESW_VCCQ 28
→ PP1V225_AWAKESW_VCCQ 41

67 PP1V225_AWAKESW_SNS
MAKE_BASE=TRUE
VOLTAGE=1.225V
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.3000
→ PP1V225_AWAKESW_SNS 41
→ PP1V225_AWAKESW_SNS 53 54

SIMETRA BUCK SW6 AND SW7

67 PP0V88_AWAKESW_NAND
MAKE_BASE=TRUE
VOLTAGE=0.88V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V88_AWAKESW_NAND 28
→ PP0V88_AWAKESW_NAND 41

PP0V88_AWAKESW_SNS
MAKE_BASE=TRUE
VOLTAGE=0.88V
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.3000
→ PP0V88_AWAKESW_SNS 41
→ PP0V88_AWAKESW_SNS 53
→ PP0V88_AWAKESW_SNS 54

SIMETRA LD04

67 PP0V72_S2_VDD_LOW
MAKE_BASE=TRUE
VOLTAGE=0.72V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V72_S2_VDD_LOW 28
→ PP0V72_S2_VDD_LOW 15
→ PP0V72_S2_VDD_LOW 15 18
→ PP0V72_S2_VDD_LOW 15
→ PP0V72_S2_VDD_LOW 15
→ PP0V72_S2_VDD_LOW 15

SIMETRA LD08

67 PP1V2_AWAKE_PLL
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V2_AWAKE_PLL 28
→ PP1V2_AWAKE_PLL 11
→ PP1V2_AWAKE_PLL 15
→ PP1V2_AWAKE_PLL 15
→ PP1V2_AWAKE_PLL 15

SIMETRA LD011

67 PP0V855_S2SW_CIO
MAKE_BASE=TRUE
VOLTAGE=0.855V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V855_S2SW_CIO 28
→ PP0V855_S2SW_CIO 15
→ PP0V855_S2SW_CIO 15

SIMETRA LD012

67 PP0V805_S1_VDD_FIXED
MAKE_BASE=TRUE
VOLTAGE=0.805V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP0V805_S1_VDD_FIXED 28
→ PP0V805_S1_VDD_FIXED 15 18
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15 18
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15

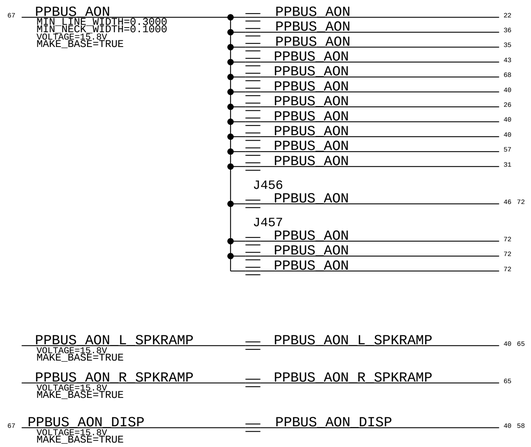
SIMETRA LD020

67 PP1V2_S2_CIO
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
→ PP1V2_S2_CIO 28
→ PP1V2_S2_CIO 15
→ PP1V2_S2_CIO 15

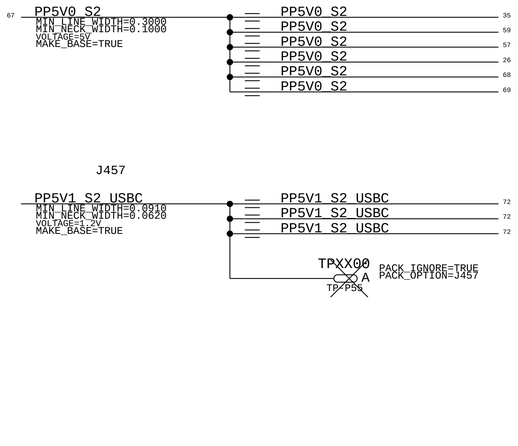
67 PPVDD_PMU_LDO_PREREG
MAKE_BASE=TRUE
VOLTAGE=3.4V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.3000
(SERA LDO3/14 INPUT)
→ PPVDD_PMU_LDO_PREREG 34
(SIMETRA LDO8 INPUT)
→ PPVDD_PMU_LDO_PREREG 31
(SIMETRA LDO20 INPUT)
→ PPVDD_PMU_LDO_PREREG 28
→ PPVDD_PMU_LDO_PREREG 28

SYNC_MASTER=peter
SYNC_DATE=12/09/2019

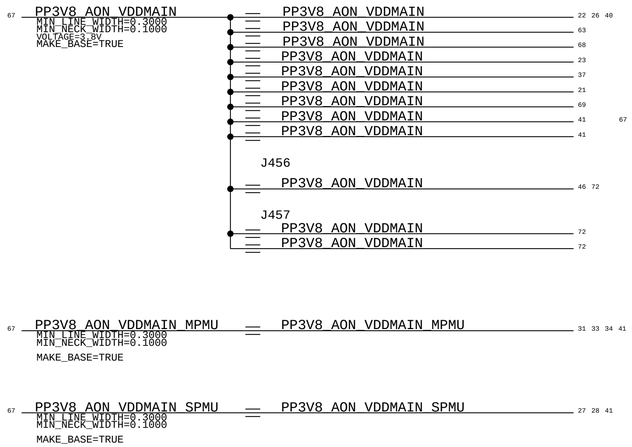
PBUS Rails



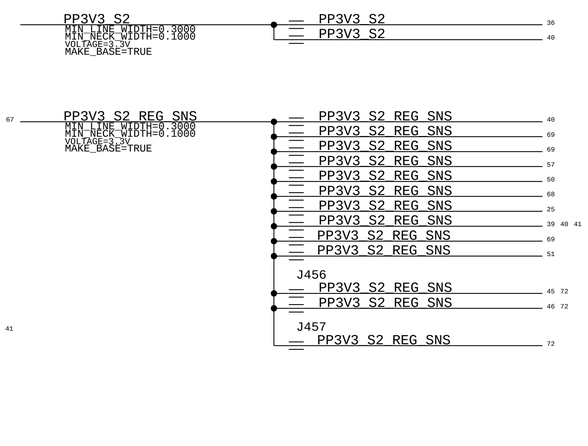
5V S2 Rails



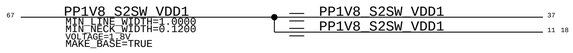
3.8V AON Rails



3.3V S2 Rails

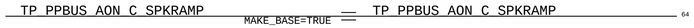


1.8V S2 SOC DRAM Rail

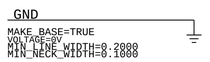


POWER SIGNAL ALIASES

SPKR UNUSED



Digital Ground



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TGA ALIASES

12	TP_VSNS_VDD2_1	TP_VSNS_VDD2_1	MAKE_BASE=TRUE
12	TP_VSNS_VDD2_2	TP_VSNS_VDD2_2	MAKE_BASE=TRUE
12	TP_VSNS_VDD_PCPU	TP_VSNS_VDD_PCPU	MAKE_BASE=TRUE
12	TP_VSNS_VDD_ECPU	TP_VSNS_VDD_ECPU	MAKE_BASE=TRUE
12	TP_VSNS_VDD_GPU	TP_VSNS_VDD_GPU	MAKE_BASE=TRUE
12	TP_VSNS_VDD_SOC	TP_VSNS_VDD_SOC	MAKE_BASE=TRUE
12	TP_VSNS_VDD_DISP	TP_VSNS_VDD_DISP	MAKE_BASE=TRUE
12	TP_VSNS_VDD_DCS	TP_VSNS_VDD_DCS	MAKE_BASE=TRUE
12	TP_VSNS_VDDQL	TP_VSNS_VDDQL	MAKE_BASE=TRUE
12	TP_VSNS_VSS_PCPU	TP_VSNS_VSS_PCPU	MAKE_BASE=TRUE
12	TP_VSNS_VSS_DDR	TP_VSNS_VSS_DDR	MAKE_BASE=TRUE
12	TP_VSNS_VSS_1	TP_VSNS_VSS_1	MAKE_BASE=TRUE
12	TP_VSNS_VSS_2	TP_VSNS_VSS_2	MAKE_BASE=TRUE
6	TP_SOC_AMUX_OUT	TP_SOC_AMUX_OUT	MAKE_BASE=TRUE

DISPLAY DBG TPs

<RDAR://51837131>

57	TP_DISP_SWDIO	TP_DISP_SWDIO	MAKE_BASE=TRUE
57	TP_DISP_SWCLK	TP_DISP_SWCLK	MAKE_BASE=TRUE

MISC TPs

10	TP_SMC_FIXTURE_MODE_L	TP_SMC_FIXTURE_MODE_L	MAKE_BASE=TRUE
10	TP_SOC_SW_DBG	TP_SOC_SW_DBG	MAKE_BASE=TRUE

ENET ALIASES

48 47	TP_SPI_ENET_SCLK	TP_SPI_ENET_SCLK	MAKE_BASE=TRUE
48 47	PD_SPI_ENET_MISO	PD_SPI_ENET_MISO	MAKE_BASE=TRUE
48 47	TP_SPI_ENET_MOSI	TP_SPI_ENET_MOSI	MAKE_BASE=TRUE
48 47	TP_SPI_ENET_CS_L	TP_SPI_ENET_CS_L	MAKE_BASE=TRUE

DISPLAY UNUSED SIGNALS

NO_TEST	NC_BKLT_UPDATE	NC_BKLT_UPDATE	MAKE_BASE=TRUE 59

SE ALIASES

21	NC_I2C_SE_SDA	NC_I2C_SE_SDA	NO_TEST MAKE_BASE=TRUE
21	NC_I2C_SE_SCL	NC_I2C_SE_SCL	NO_TEST MAKE_BASE=TRUE

NAND ALIASES

67 6	SWD_NAND0_SWCLK	SWD_NAND0_SWCLK	MAKE_BASE=TRUE 53
		SWD_NAND0_SWCLK	54
67 6	SWD_NAND0_SWDIO	SWD_NAND0_SWDIO	MAKE_BASE=TRUE 53
		SWD_NAND0_SWDIO	54
68 67 57 46 33	PMU_SYS_ALIVE	PMU_SYS_ALIVE	MAKE_BASE=TRUE 53 54
54	TP_NAND0_S5E1_JTAG_TDO	TP_NAND0_S5E1_JTAG_TDO	47 MAKE_BASE=TRUE

WIFI ALIASES

53	NC_SPMI_WLBT_CLK_1V8	NC_SPMI_WLBT_CLK_1V8	NO_TEST MAKE_BASE=TRUE
53	NC_SPMI_WLBT_DAT_1V8	NC_SPMI_WLBT_DAT_1V8	NO_TEST MAKE_BASE=TRUE
51	NC_BT_R1_WAKE	NC_BT_R1_WAKE	NO_TEST MAKE_BASE=TRUE
52 51	NC_BT_R1_TIME_SYNC	NC_BT_R1_TIME_SYNC	NO_TEST MAKE_BASE=TRUE

USB ALIASES

44	NC_USB_LS1P	NC_USB_LS1P	MAKE_BASE=TRUE NO_TEST
44	NC_USB_LS1N	NC_USB_LS1N	MAKE_BASE=TRUE NO_TEST
44	NC_EUSB_LS1P	NC_EUSB_LS1P	MAKE_BASE=TRUE NO_TEST
44	NC_EUSB_LS1N	NC_EUSB_LS1N	MAKE_BASE=TRUE NO_TEST

POWER ALIASES

26	TP_PM_P3V8AON_FAULT_L	TP_PM_P3V8AON_FAULT_L	67 MAKE_BASE=TRUE

AUDIO ALIASES

67 62	TDM_1V8_SPKRAMP_L_BCLK	TDM_1V8_SPKRAMP_L_BCLK	MAKE_BASE=TRUE 64
		TDM_1V8_SPKRAMP_L_BCLK	64
		TDM_1V8_SPKRAMP_L_BCLK	64
67 62	TDM_1V8_SPKRAMP_L_FSYNC	TDM_1V8_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE 64
		TDM_1V8_SPKRAMP_L_FSYNC	64
		TDM_1V8_SPKRAMP_L_FSYNC	64
67 62	TDM_1V8_SPKRAMP_L_R2D	TDM_1V8_SPKRAMP_L_R2D	MAKE_BASE=TRUE 64
		TDM_1V8_SPKRAMP_L_R2D	64
		TDM_1V8_SPKRAMP_L_R2D	64
7	TDM_SPKRAMP_L_BCLK_R	TDM_SPKRAMP_L_BCLK_R	62
7	TDM_SPKRAMP_L_FSYNC_R	TDM_SPKRAMP_L_FSYNC_R	MAKE_BASE=TRUE 62
7	TDM_SPKRAMP_L_R2D_R	TDM_SPKRAMP_L_R2D_R	MAKE_BASE=TRUE 62
	NC_TDM_SPKRAMP_R_BCLK_R	NC_TDM_SPKRAMP_R_BCLK_R	62
	NC_TDM_SPKRAMP_R_FSYNC_R	NC_TDM_SPKRAMP_R_FSYNC_R	MAKE_BASE=TRUE 62
	NC_TDM_SPKRAMP_R_R2D_R	NC_TDM_SPKRAMP_R_R2D_R	MAKE_BASE=TRUE 62
62	NC_TDM_1V8_SPKRAMP_R_BCLK	NC_TDM_1V8_SPKRAMP_R_BCLK	MAKE_BASE=TRUE
62	NC_TDM_1V8_SPKRAMP_R_FSYNC	NC_TDM_1V8_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE
62	NC_TDM_1V8_SPKRAMP_R_R2D	NC_TDM_1V8_SPKRAMP_R_R2D	MAKE_BASE=TRUE

SHARED POWER ALIASES

J456

70 46	PP1V2_AWAKE_IO	PP1V2_AWAKE_IO	
70 46	PP1V25_S2	PP1V25_S2	
71 45	PP3V3_S2_REG_SNS	PP3V3_S2_REG_SNS	
70 46	PP1V8_S2	PP1V8_S2	
71 46	PP3V3_S2_REG_SNS	PP3V3_S2_REG_SNS	
70 46	PP3V3_S2_UPC	PP3V3_S2_UPC	
71 46	PP3V8_AON_VDDMAIN	PP3V8_AON_VDDMAIN	
71 46	PPBUS_AON	PPBUS_AON	

J457

70	PP3V3_S2_UPC	PP3V3_S2_UPC	
70	PP1V8_S2	PP1V8_S2	
71	PP5V1_S2_USBC	PP5V1_S2_USBC	
71	PP5V1_S2_USBC	PP5V1_S2_USBC	
71	PP5V1_S2_USBC	PP5V1_S2_USBC	
71	PPBUS_AON	PPBUS_AON	
71	PPBUS_AON	PPBUS_AON	
70	PP1V25_S2	PP1V25_S2	
71	PP3V8_AON_VDDMAIN	PP3V8_AON_VDDMAIN	
71	PP3V8_AON_VDDMAIN	PP3V8_AON_VDDMAIN	
71	PP3V3_S2_REG_SNS	PP3V3_S2_REG_SNS	
71	PPBUS_AON	PPBUS_AON	
65	PPBUS_AON_R_SPKRAMP	PPBUS_AON_R_SPKRAMP	
65	PPBUS_AON_R_SPKRAMP	PPBUS_AON_R_SPKRAMP	

VITAMIN C ALIASES

69	UNUSED_USBC0_3V3_LDO_EN_VITC	UNUSED_USBC0_3V3_LDO_EN_VITC	MAKE_BASE=TRUE
69	UNUSED_USBC0_3V3_LDO_EN	UNUSED_USBC0_3V3_LDO_EN	MAKE_BASE=TRUE

The retimer must be locally powered on J456 for vitamin c to operate see RF902

Test Point Just To A Connection

TPXY00 PACK_IGNORE=TRUE PACK_OPTION=REMOVE

TP-PSM

10	LID_OPEN	LID_OPEN	MAKE_BASE=TRUE

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TGA UNUSED SIGNALS

7 1276	NC_SPI_1V8_TOUCHID_MISO	NC_SPI_1V8_TOUCHID_MISO		
7 1280	NC_SPI_1V8_TOUCHID_MOSI_R	NC_SPI_1V8_TOUCHID_MOSI_R	NO_TEST=1	MAKE_BASE=TRUE
7 1281	NC_SPI_1V8_TOUCHID_CLK_R	NC_SPI_1V8_TOUCHID_CLK_R	NO_TEST=1	MAKE_BASE=TRUE
7 1215	NC_TOUCHID_INT	NC_TOUCHID_INT	NO_TEST=1	MAKE_BASE=TRUE
7 1216	NC_SPI_IPD_MISO	NC_SPI_IPD_MISO	NO_TEST=1	MAKE_BASE=TRUE
7 1217	NC_SPI_IPD_MOSI_R	NC_SPI_IPD_MOSI_R	NO_TEST	MAKE_BASE=TRUE
7 1218	NC_SPI_IPD_CLK_R	NC_SPI_IPD_CLK_R	NO_TEST	MAKE_BASE=TRUE
7 1219	NC_SPI_IPD_CS_L	NC_SPI_IPD_CS_L	NO_TEST	MAKE_BASE=TRUE
7 1220	NC_IPD_SPI_EN	NC_IPD_SPI_EN	NO_TEST	MAKE_BASE=TRUE
10 1221	NC_AOP_GYRO_CLK	NC_AOP_GYRO_CLK	NO_TEST=1	MAKE_BASE=TRUE
10 1222	NC_AOP_GYRO_MISO	NC_AOP_GYRO_MISO	NO_TEST=1	MAKE_BASE=TRUE
10 1223	NC_AOP_GYRO_MOSI	NC_AOP_GYRO_MOSI	NO_TEST=1	MAKE_BASE=TRUE
10 1224	NC_AOP_GYRO_CS_L	NC_AOP_GYRO_CS_L	NO_TEST=1	MAKE_BASE=TRUE
10 1225	NC_GYRO_INT	NC_GYRO_INT	NO_TEST=1	MAKE_BASE=TRUE
10 1226	NC_GYRO_MOTION_INT	NC_GYRO_MOTION_INT	NO_TEST=1	MAKE_BASE=TRUE
6 1255	NC_KBD_BKLT_PWM	NC_KBD_BKLT_PWM	NO_TEST=1	MAKE_BASE=TRUE
7 1256	NC_DFR_TOUCH_INT_L	NC_DFR_TOUCH_INT_L	NO_TEST=1	MAKE_BASE=TRUE
10 1257	NC_DFR_TOUCH_CLK32K_RESET_L	NC_DFR_TOUCH_CLK32K_RESET_L	NO_TEST=1	MAKE_BASE=TRUE
7 1258	NC_DFR_PWR_EN	NC_DFR_PWR_EN	NO_TEST=1	MAKE_BASE=TRUE
8 1259	NC_DFR_DISP_TE	NC_DFR_DISP_TE	NO_TEST=1	MAKE_BASE=TRUE
8 1260	NC_MIPI_DFR_DATAP	NC_MIPI_DFR_DATAP	NO_TEST=1	MAKE_BASE=TRUE
8 1261	NC_MIPI_DFR_DATAN	NC_MIPI_DFR_DATAN	NO_TEST=1	MAKE_BASE=TRUE
8 1262	NC_MIPI_DFR_CLKP	NC_MIPI_DFR_CLKP	NO_TEST=1	MAKE_BASE=TRUE
8 1263	NC_MIPI_DFR_CLKN	NC_MIPI_DFR_CLKN	NO_TEST=1	MAKE_BASE=TRUE
7 1264	NC_DFR_1V8_TOUCH_RESET_L	NC_DFR_1V8_TOUCH_RESET_L	NO_TEST=1	MAKE_BASE=TRUE
7 1265	NC_DFR_1V8_DISP_RESET_L	NC_DFR_1V8_DISP_RESET_L	NO_TEST=1	MAKE_BASE=TRUE
7 1266	NC_DFR_1V8_DISP_INT	NC_DFR_1V8_DISP_INT	NO_TEST=1	MAKE_BASE=TRUE
7 1267	NC_SPI_DFR_CS_L	NC_SPI_DFR_CS_L	NO_TEST=1	MAKE_BASE=TRUE
10 1238	NC_SPI_DP2HDMI_HOLD_L	NC_SPI_DP2HDMI_HOLD_L	NO_TEST=1	MAKE_BASE=TRUE
10 1239	NC_HDMI_HPD_AOP	NC_HDMI_HPD_AOP	NO_TEST=1	MAKE_BASE=TRUE
10 1240	NC_HDMI_CEC_AOP_TX	NC_HDMI_CEC_AOP_TX	NO_TEST=1	MAKE_BASE=TRUE
10 1241	NC_HDMI_CEC_AOP_RX	NC_HDMI_CEC_AOP_RX	NO_TEST=1	MAKE_BASE=TRUE
7 1242	NC_ENET_SYNC_1588	NC_ENET_SYNC_1588	NO_TEST=1	MAKE_BASE=TRUE
10 1243	NC_ACDC_ID	NC_ACDC_ID	NO_TEST=1	MAKE_BASE=TRUE
10 1245	NC_ACDC_BURST_EN_L	NC_ACDC_BURST_EN_L	NO_TEST	MAKE_BASE=TRUE
10 1246	NC_SMC_FAN_PWM	NC_SMC_FAN_PWM	NO_TEST	MAKE_BASE=TRUE
10 1247	NC_SMC_FAN_TACH	NC_SMC_FAN_TACH	NO_TEST=1	MAKE_BASE=TRUE
7 1248	NC_SPKR_ID0	NC_SPKR_ID0	NO_TEST=1	MAKE_BASE=TRUE
7 1249	NC_SPKR_ID1	NC_SPKR_ID1	NO_TEST=1	MAKE_BASE=TRUE
7 1250	NC_I2C_CODEC_SCL	NC_I2C_CODEC_SCL	NO_TEST=1	MAKE_BASE=TRUE
7 1251	NC_I2C_CODEC_SDA	NC_I2C_CODEC_SDA	NO_TEST=1	MAKE_BASE=TRUE
7 1008	NC_TDM_SPKRAMP_L_D2R	NC_TDM_SPKRAMP_L_D2R	NO_TEST=1	MAKE_BASE=TRUE
7 1009	NC_TDM_SPKRAMP_R_D2R	NC_TDM_SPKRAMP_R_D2R	NO_TEST=1	MAKE_BASE=TRUE
7 1270	NC_SPKRAMP_RESET_L	NC_SPKRAMP_RESET_L	NO_TEST=1	MAKE_BASE=TRUE
7 1271	NC_SPKRAMP_INT_L	NC_SPKRAMP_INT_L	NO_TEST=1	MAKE_BASE=TRUE

8 1187	NC_LPDP_TX4P	NC_LPDP_TX4P		
8 1188	NC_LPDP_TX4N	NC_LPDP_TX4N	MAKE_BASE=TRUE	NO_TEST
8 1189	NC_LPDP_TX5P	NC_LPDP_TX5P	MAKE_BASE=TRUE	NO_TEST
8 1190	NC_LPDP_TX5N	NC_LPDP_TX5N	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
8 1065	NC_MIPI0C_CLKP	NC_MIPI0C_CLKP		
8 1066	NC_MIPI0C_CLKN	NC_MIPI0C_CLKN	MAKE_BASE=TRUE	NO_TEST
8 1067	NC_MIPI0C_DATAP<0..1>	NC_MIPI0C_DATAP<0..1>	MAKE_BASE=TRUE	NO_TEST
8 1068	NC_MIPI0C_DATAN<0..1>	NC_MIPI0C_DATAN<0..1>	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
8 1172	NC_ISP_GPIO1	NC_ISP_GPIO1		
8 1173	NC_ISP_GPIO2	NC_ISP_GPIO2	MAKE_BASE=TRUE	NO_TEST
8 1174	NC_ISP_GPIO3	NC_ISP_GPIO3	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
8 1175	NC_ISP_SPMI0_CLK	NC_ISP_SPMI0_CLK		
8 1176	NC_ISP_SPMI0_DATA	NC_ISP_SPMI0_DATA	MAKE_BASE=TRUE	NO_TEST
8 1177	NC_ISP_SPMI1_CLK	NC_ISP_SPMI1_CLK	MAKE_BASE=TRUE	NO_TEST
8 1178	NC_ISP_SPMI1_DATA	NC_ISP_SPMI1_DATA	MAKE_BASE=TRUE	NO_TEST
7 1179	NC_SPMI2_CLK	NC_SPMI2_CLK	MAKE_BASE=TRUE	NO_TEST
7 1180	NC_SPMI2_DATA	NC_SPMI2_DATA	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
8 1181	NC_SENSOR0_CLK	NC_SENSOR0_CLK		
8 1182	NC_SENSOR1_CLK	NC_SENSOR1_CLK	MAKE_BASE=TRUE	NO_TEST
8 1183	NC_SENSOR2_CLK	NC_SENSOR2_CLK	MAKE_BASE=TRUE	NO_TEST
8 1184	NC_SENSOR3_CLK	NC_SENSOR3_CLK	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
7 1185	NC_SOC_SPI2_SSIN	NC_SOC_SPI2_SSIN		
9 1192	NC_NAND0_PCIE_RESET1_L	NC_NAND0_PCIE_RESET1_L	MAKE_BASE=TRUE	NO_TEST
7 1194	NC_SSPI0_MOSI	NC_SSPI0_MOSI	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
10 1195	NC_PDM_CLK1	NC_PDM_CLK1		
10 1196	NC_PDM_CLK2	NC_PDM_CLK2	MAKE_BASE=TRUE	NO_TEST
10 1197	NC_PDM_CLK5	NC_PDM_CLK5	MAKE_BASE=TRUE	NO_TEST
10 1198	NC_PDM_CLK6	NC_PDM_CLK6	MAKE_BASE=TRUE	NO_TEST
10 1199	NC_PDM_DATA1	NC_PDM_DATA1	MAKE_BASE=TRUE	NO_TEST
10 1200	NC_PDM_DATA2	NC_PDM_DATA2	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
10 1201	NC_AOP_SPMI0_SCLK	NC_AOP_SPMI0_SCLK		
10 1202	NC_AOP_SPMI0_SDATA	NC_AOP_SPMI0_SDATA	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
10 1072	NC_CHGR_INT_L_LOM_PMU_RESET_EN	NC_CHGR_INT_L_LOM_PMU_RESET_EN	MAKE_BASE=TRUE	

8 1105	NC_LPDPRX_AUX0	NC_LPDPRX_AUX0		
8 1106	NC_LPDPRX_AUX1	NC_LPDPRX_AUX1	MAKE_BASE=TRUE	NO_TEST
8 1107	NC_LPDPRX_AUX2	NC_LPDPRX_AUX2	MAKE_BASE=TRUE	NO_TEST
8 1108	NC_LPDPRX_AUX3	NC_LPDPRX_AUX3	MAKE_BASE=TRUE	NO_TEST
8 1109	NC_LPDPRX_AUX4	NC_LPDPRX_AUX4	MAKE_BASE=TRUE	NO_TEST
8 1110	NC_LPDPRX_AUX5	NC_LPDPRX_AUX5	MAKE_BASE=TRUE	NO_TEST
8 1111	NC_LPDPRX_AUX6	NC_LPDPRX_AUX6	MAKE_BASE=TRUE	NO_TEST
8 1120	NC_LPDPRX_AUX7	NC_LPDPRX_AUX7	MAKE_BASE=TRUE	NO_TEST
8 1121	NC_LPDPRX_AUX8	NC_LPDPRX_AUX8	MAKE_BASE=TRUE	NO_TEST
8 1122	NC_LPDPRX_AUX9	NC_LPDPRX_AUX9	MAKE_BASE=TRUE	NO_TEST
8 1123	NC_LPDPRX_AUX10	NC_LPDPRX_AUX10	MAKE_BASE=TRUE	NO_TEST
8 1124	NC_LPDPRX_AUX11	NC_LPDPRX_AUX11	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
8 1125	NC_LPDPRX_RXP<0..11>	NC_LPDPRX_RXP<0..11>		
8 1126	NC_LPDPRX_RXN<0..11>	NC_LPDPRX_RXN<0..11>	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
8 1135	NC_DISP_TOUCH_BSYNC0	NC_DISP_TOUCH_BSYNC0		
8 1136	NC_DISP_TOUCH_BSYNC1	NC_DISP_TOUCH_BSYNC1	MAKE_BASE=TRUE	NO_TEST
8 1137	NC_DISP_TOUCH_EB	NC_DISP_TOUCH_EB	MAKE_BASE=TRUE	NO_TEST
8 1138	NC_DISP_SPMI_CLK	NC_DISP_SPMI_CLK	MAKE_BASE=TRUE	NO_TEST
8 1139	NC_DISP_SPMI_DATA	NC_DISP_SPMI_DATA	MAKE_BASE=TRUE	NO_TEST
8 1140	NC_DISP_FSYNC	NC_DISP_FSYNC	MAKE_BASE=TRUE	NO_TEST
8 1141	NC_DISPLAY_POL	NC_DISPLAY_POL	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
7 1142	NC_I2S3_BCLK	NC_I2S3_BCLK		
7 1153	NC_I2S3_D2R	NC_I2S3_D2R	MAKE_BASE=TRUE	NO_TEST
7 1152	NC_I2S3_R2D	NC_I2S3_R2D	MAKE_BASE=TRUE	NO_TEST
7 1155	NC_I2S3_LRCLK	NC_I2S3_LRCLK	MAKE_BASE=TRUE	NO_TEST
7 1154	NC_I2S3_MCLK	NC_I2S3_MCLK	MAKE_BASE=TRUE	NO_TEST
7 1155	NC_SOC_I2S0_MCK	NC_SOC_I2S0_MCK	MAKE_BASE=TRUE	NO_TEST
7 1156	NC_SOC_I2S1_MCK	NC_SOC_I2S1_MCK	MAKE_BASE=TRUE	NO_TEST
7 1157	NC_SOC_I2S2_MCK	NC_SOC_I2S2_MCK	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
6 1158	NC_FPWM2	NC_FPWM2		
			MAKE_BASE=TRUE	NO_TEST
7 1283	NC_UART3_D2R_CTS_L	NC_UART3_D2R_CTS_L		
7 1284	NC_UART3_R2D_RTS_L	NC_UART3_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST
7 1285	NC_UART3_D2R	NC_UART3_D2R	MAKE_BASE=TRUE	NO_TEST
7 1287	NC_UART3_R2D	NC_UART3_R2D	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST
7 1288	NC_UART4_D2R_CTS_L	NC_UART4_D2R_CTS_L		
7 1289	NC_UART4_R2D_RTS_L	NC_UART4_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST
7 1291	NC_UART4_D2R	NC_UART4_D2R	MAKE_BASE=TRUE	NO_TEST
7 1292	NC_UART4_R2D	NC_UART4_R2D	MAKE_BASE=TRUE	NO_TEST
			MAKE_BASE=TRUE	NO_TEST

7 1321	NC_GPU_CFG_L	NC_GPU_CFG_L	
			MAKE_BASE=TRUE NO_TEST

SYNC_MASTER=aaron SYNC_DATE=02/28/2020

PAGE TITLE

Signal Alias - 2

Apple Inc.

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SI ANALYSYS	REQUIRED
CALIBRE_SI (YES/NO)	YES
POWERDC (YES/NO)	YES
POWERSI (YES/NO)	NO
XTALK (YES/NO)	YES

POWER RULES		
PHYSICAL RULE NAME RULES PREFIXED: A_PWR	LOAD CURRENT (mA)	CURRENT DENSITY(A/mm^2)
DISP_VIN	5000	90
BKLT_VIN	3500	90
BKLT_LED	100	20
BKLT_BOOST	1000	50

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup. Shortest distance is used unless "L" is defined	EXAMPLE: 1,2,3,L,4L,5-10L 2-10
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from Hybrid Table and stackup. Shortest distance is used unless "L" defined	EXAMPLE: 2,2V,2VL,3,3VL,4-10VL PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup. Shortest distance is used unless "L" is defined	EXAMPLE: 2,4,6,3L 4_6,5_7

Physcial Set Default is 45 Ohm with necking

Constraint Net Assignments for Display

DOMAIN (S,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_PWR_DISP_VIN	PPBUS_AON_DISP
P	A_PWR_BKLT_VIN	PPVIN_BKLT*
P	A_PWR_BKLT_LED	LED_RETURN*,VLED*

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= 2			
RULE NAME= 50_OHM_RF		ZONE NAME= PRIMARY	
ISL4	ISL2,ISL6	50	0.145
ISL9	ISL7,ISL11	50	0.145
BOTTOM	ISL10	50	0.256

CAPPED RULE EXAMPLE:SMD2ALL,SMD_TO_SMD,MVIA2ALL,SHAPE2ALL	LAYER ALL=ALL LAYERS BOT=BOTTOM LAYER	VALUE (MM)	RULE NAME(S) EXAMPLE: 2D,2V,3DL-5DL,3VL	HYBRID RULE NAME EXAMPLE: 50_THIN	ZONE
SMD2ALL	BOT	0.20	2	50_OHM_RF	PRIMARY
MVIA2SHAPE	ALL	=0.25	2	50_OHM_RF	PRIMARY
BBVIA2SHAPE	ALL	=0.25	2	50_OHM_RF	PRIMARY

Per WiFi team, override A_dielectric_2X_50_Ohm_Rf_Se spacing with:
MicroVia to Shape = 0.25 all layers
Burried Via to Shape = 0.25 all layers

Class Definitions and Net Assignments

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN (S,P,S)	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
I2C	P	A_45_OHM_SE	INT*I2C*,!I2C*SPI*,!NC_*,!TP_*	Y
SPI	P	A_45_OHM_SE	*SPI*CLK*,*SPI*CS*,*SPI*MOSI*,*SPI*MISO*,!NC_*,!TP_*	Y
SPMI	P	A_45_OHM_SE	*SPMI*,!NC_*,!TP_*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*,SWD_SOC*,SWD_UPC*	Y
JTAG	P	A_45_OHM_SE	*JTAG*TCK,*JTAG*TMS,*JTAG*TDI,*JTAG*TDO,*JTAG*SEL	Y
CLK24M	P	A_45_OHM_SE	SOC_XTAL24M*,NAND0_CLK24M*,SOC_24M*	Y
CLK32K	P	A_45_OHM_SE	*CLK32K*,!NC_*	Y
TDM_SPKRAMP	P	A_45_OHM_SE	TDM_*SPKRAMP_*,!NC_*,!TP_*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
UART	P	A_45_OHM_SE	UART*	Y
CIO_ATC	P	A_45_OHM_SE	CIO_ATC*_LS*X*	Y
RESETS	P	A_45_OHM_SE	*RESET*,*RST*,*PERST*,!NC_*,!TP_*	Y
SOC_CTRL	P	A_45_OHM_SE	SOC_WDOG,SOC_SOCHOT_L,SOC*DFU*,SOC*DOCK*	Y
FAULT	P	A_45_OHM_SE	*_FAULT_*	Y
PDM_DMIC	P	A_45_OHM_SE	PDM_DMIC*,DMIC_*,!TP_*,!NC_*	Y
BOARD_INFO	P	A_45_OHM_SE	BOARD_ID*,BOARD_REV*	Y
TIME_SYNC	P	A_45_OHM_SE	*TIME_SYNC*,!NC_*	Y
USBC_ATC	P	A_85_OHM_DIFF	DP:DP_USBC_ATC*R2D*,DP:DP_USBC_ATC*D2R*	Y
USBC_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC*AUX*	Y
PCIE	P	A_85_OHM_DIFF	DP:DP_PCIE*R2D*,DP:DP_PCIE*D2R*	Y
DISPLAYPORT	P	A_85_OHM_DIFF	DP:DP_DP_INTPNL*	Y
MIPI_CSI	P	A_85_OHM_DIFF	DP:DP_MIPI*	Y
RCAL_PCIE	P	M_WIDTH_P1MM	SOC_*_PCIE_RCAL*,*RESREF*	Y
RCAL_CIO	P	M_WIDTH_P1MM	SOC_ATCPHY*_RCAL*	Y
RCAL_MIPI	P	M_WIDTH_P1MM	*MIPI*REXT	Y
DDR	P	A_45_OHM_SE	DDR*ZQ*,DDR*RR*	Y
CLK100M	P	A_85_OHM_DIFF	DP:DP_*CLK100M*	Y
SENSE	P	M_SNS_DIFF	DP:DP_*ISNS*,DP:DP_BKLT_PH*_SNS*	Y
POWER	P	M_PWR_P3MM	PP*,*SNUB*,LED_RET*,VLED*,BUCK*_LX*,VSS_*	Y
GROUND	P	M_PWR_P3MM	GND*,CODEC*_GND,*_AGND,*_SGND,LED_BTN_GND	Y
POWER_GATE	P	M_PWR_P3MM	BKLT_PH*_GATE*	Y
BACKLIGHT	P	A_PWR_BKLT_BOOST	BKLT_BOOST*,BKLT_PH*_SW	Y
BUCK	P	M_VR_FB	BUCK*_FB*	Y
CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
NAND_MISC	P	A_45_OHM_SE	NAND*B*,NAND*SWD*,NAND*WP*	Y
NAND_Z	P	M_WIDTH_P1MM	NAND*ZQ*	Y
PMU_CTRL	P	A_45_OHM_SE	PMU_SYS*,PMU_ACTE*,PMU_SH*,PMU*CRA*,PMU_ON*,UPC_FORCE*	Y
WAKE	P	A_45_OHM_SE	*_WAKE*,!TP_*,!NC_*	Y
USB2	P	A_85_OHM_DIFF	DP:DP_EUSB_ATC*,DP:DP_*USB*DBG*,DP:DP_USB2_ATC*	Y
ENET	P	M_96IN_100OUT_OHM_DIFF	DP:DP_ENETCONN_MDI*	Y
SPKRAMP_OUT	P	M_SPKRAMP_OUT_DIFF	DP:DP_SPKRAMP*OUT*	Y
ANTENNA	P	A_50_OHM_RF_SE	RF_ANT_0,RF_ANT_1,RF_BT_DED*	Y
AUDIO_P3MM	P	M_AUD_P3MM	AUD*OUT,AUDIO_JACK*GND,AUD*SLEEVE,AUD*RING2	Y
AUDIO_P2MM	P	M_AUD_P2MM	AUD*SENSE,AUD*_XW,!*TIP*,!*RING_*	Y
AUDIO_P1MM	P	M_AUD_P1MM	AUD*SNS,AUD*MIC,AUD*TIP*,AUD*RING_*,SPKRAMP_*_5V	Y
POWER_ENABLES	P	A_45_OHM_SE	*PWR_EN*,!NC_*,!USB3_*,!SE_*	Y

Class Definitions and Net Assignments

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN (S,P,S)	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	S	A_DIELECTRIC_2X	=	Y
SPI	S	A_DIELECTRIC_2X	=	Y
SPMI	S	A_DIELECTRIC_3X	=	Y
SWD	S	A_DIELECTRIC_2X	=	Y
JTAG	S	A_DIELECTRIC_2X	=	Y
CLK24M	S	A_DIELECTRIC_8X	=	Y
CLK32K	S	A_DIELECTRIC_8X	=	Y
TDM_SPKRAMP	S	A_DIELECTRIC_4X	=	Y
TDM_CODEC	S	A_DIELECTRIC_4X	=	Y
UART	S	A_DIELECTRIC_2X	=	Y
CIO_ATC	S	A_DIELECTRIC_3X	=	Y
RESETS	S	A_DIELECTRIC_5X	=	Y
SOC_CTRL	S	A_DIELECTRIC_4X	=	Y
FAULT	S	A_DIELECTRIC_5X	=	Y
PDM_DMIC	S	A_DIELECTRIC_4X	=	Y
BOARD_INFO	S	A_DIELECTRIC_2X	=	Y
TIME_SYNC	S	A_DIELECTRIC_3X	=	Y
USBC_ATC	S	A_DIELECTRIC_5XIN_7XOUT	=	Y
USBC_AUX	S	A_DIELECTRIC_5XIN_7XOUT	=	Y
PCIE	S	A_DIELECTRIC_4XIN_6XOUT	=	Y
DISPLAYPORT	S	A_DIELECTRIC_4XIN_6XOUT	=	Y
MIPI_CSI	S	A_DIELECTRIC_5XIN_7XOUT	=	Y
RCAL_PCIE	S	A_DIELECTRIC_2X	=	Y
RCAL_CIO	S	A_DIELECTRIC_2X	=	Y
RCAL_MIPI	S	A_DIELECTRIC_2X	=	Y
DDR	S	A_DIELECTRIC_2X	=	Y
CLK100M	S	A_DIELECTRIC_4XIN_6XOUT	=	Y
SENSE	S	A_DIELECTRIC_2X	=	Y
POWER	S	M_PWR_P1MM	=	Y
GROUND	S	M_PWR_P1MM	=	Y
POWER_GATE	S	A_DIELECTRIC_3X	=	Y
BACKLIGHT	S	A_DIELECTRIC_5X	=	Y
BUCK	S	DEFAULT	=	Y
CLKREQ	S	A_DIELECTRIC_3X	=	Y
NAND_MISC	S	A_DIELECTRIC_2X	=	Y
NAND_Z	S	A_DIELECTRIC_2X	=	Y
PMU_CTRL	S	A_DIELECTRIC_3X	=	Y
WAKE	S	A_DIELECTRIC_2X	=	Y
USB2	S	A_DIELECTRIC_2X	=	Y
ENET	S	A_DIELECTRIC_2X	=	Y
SPKRAMP_OUT	S	A_DIELECTRIC_2X	=	Y
ANTENNA	S	A_DIELECTRIC_2X_50_OHM_RF_SE	=	Y
AUDIO_P3MM	S	A_DIELECTRIC_2X	=	Y
AUDIO_P2MM	S	A_DIELECTRIC_2X	=	Y
AUDIO_P1MM	S	A_DIELECTRIC_2X	=	Y
POWER_ENABLES	S	A_DIELECTRIC_2X	=	Y

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN (S,P,S)	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_DISPLAYPORT	E	LPDP	DP:DP_DP_INTPNL_ML*	Y
E_MIPI_CSI	E	MIPI	DP:DP_MIPI_FTCAM*	Y
E_BACKLIGHT	E	BACKLIGHT	LED_RETURN*,VLED*	Y

SYNC_MASTER=aaron SYNC_DATE=08/07/2019

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Constraints Physical and Spacing

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	GROUND	DEFAULT
SPI	GROUND	DEFAULT
SPMI	GROUND	DEFAULT
SWD	GROUND	DEFAULT
JTAG	GROUND	DEFAULT
CLK24M	GROUND	DEFAULT
CLK32K	GROUND	DEFAULT
TDM_SPKRAMP	GROUND	DEFAULT
TDM_CODEC	GROUND	DEFAULT
UART	GROUND	DEFAULT
RESETS	GROUND	DEFAULT
SOC_CTRL	GROUND	DEFAULT
FAULT	GROUND	DEFAULT
PDM_DMIC	GROUND	DEFAULT
BOARD_INFO	GROUND	DEFAULT
TIME_SYNC	GROUND	DEFAULT
USBC_ATC	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
USBC_AUX	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
PCIE	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
DISPLAYPORT	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
MIPI_CSI	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
RCAL_PCIE	GROUND	DEFAULT
RCAL_CIO	GROUND	DEFAULT
RCAL_MIPI	GROUND	DEFAULT
CLK100M	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
SENSE	GROUND	DEFAULT
POWER	GROUND	DEFAULT
CLKREQ	GROUND	DEFAULT
NAND_MISC	GROUND	DEFAULT
PMU_CTRL	GROUND	DEFAULT
WAKE	GROUND	DEFAULT
USB2	GROUND	M_DEFAULT_WITH_7X_LINE2SHAPE
ENET	GROUND	DEFAULT
SPKRAMP_OUT	GROUND	DEFAULT
AUDIO_P3MM	GROUND	DEFAULT
AUDIO_P2MM	GROUND	DEFAULT
AUDIO_P1MM	GROUND	DEFAULT
POWER_ENABLES	GROUND	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	POWER	DEFAULT
SPI	POWER	DEFAULT
SPMI	POWER	DEFAULT
SWD	POWER	DEFAULT
JTAG	POWER	DEFAULT
CLK24M	POWER	DEFAULT
CLK32K	POWER	DEFAULT
TDM_SPKRAMP	POWER	DEFAULT
TDM_CODEC	POWER	DEFAULT
UART	POWER	DEFAULT
RESETS	POWER	DEFAULT
SOC_CTRL	POWER	DEFAULT
FAULT	POWER	DEFAULT
PDM_DMIC	POWER	DEFAULT
BOARD_INFO	POWER	DEFAULT
TIME_SYNC	POWER	DEFAULT
USBC_ATC	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
USBC_AUX	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
PCIE	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
DISPLAYPORT	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
MIPI_CSI	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
RCAL_PCIE	POWER	DEFAULT
RCAL_CIO	POWER	DEFAULT
RCAL_MIPI	POWER	DEFAULT
CLK100M	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
SENSE	POWER	DEFAULT
POWER	POWER	DEFAULT
CLKREQ	POWER	DEFAULT
NAND_MISC	POWER	DEFAULT
PMU_CTRL	POWER	DEFAULT
WAKE	POWER	DEFAULT
USB2	POWER	M_DEFAULT_WITH_7X_LINE2SHAPE
ENET	POWER	DEFAULT
SPKRAMP_OUT	POWER	DEFAULT
AUDIO_P3MM	POWER	DEFAULT
AUDIO_P2MM	POWER	DEFAULT
AUDIO_P1MM	POWER	DEFAULT
POWER_ENABLES	POWER	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
DISPLAYPORT	DISPLAYPORT	A_DIELECTRIC_3X
MIPI_CSI	MIPI_CSI	A_DIELECTRIC_2X

SYNC_MASTER=T668_MLB SYNC_DATE=11/22/2019

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Constraints Class to Class

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0276	107S00020	ALT_CMN	ALL	<rdar://57775168>
107S00071	107S00053	ALT_CMN	ALL	<rdar://60385123>
107S00104	107S00061	ALT_CMN	ALL	<rdar://60422997>
107S00298	107S0208	ALT_CMN	ALL	<rdar://59969910>
107S0150	107S0208	ALT_CMN	ALL	<rdar://59969910>
107S0249	107S0251	ALT_CMN	ALL	<rdar://60385933>
128S00043	128S00042	ALT_CMN	ALL	<rdar://60657909>
128S0329	128S00042	ALT_CMN	ALL	<rdar://60657909>
132S00237	132S00236	ALT_CMN	ALL	<rdar://57918329>
138S00264	138S00008	ALT_CMN	ALL	<rdar://59973969>
138S00116	138S00071	ALT_CMN	ALL	<rdar://59975810>
138S00117	138S00071	ALT_CMN	ALL	<rdar://59975810>
138S00047	138S00073	ALT_CMN	ALL	<rdar://59975717>
138S00330	138S00081	ALT_CMN	ALL	<rdar://59976784>
138S00229	138S00107	ALT_CMN	ALL	<rdar://59973498>
138S00284	138S00136	ALT_CMN	ALL	<rdar://60005233>
138S00332	138S00328	ALT_CMN	ALL	<rdar://60004440>
138S00343	138S00329	ALT_CMN	ALL	<rdar://59961139>
138S0846	138S0811	ALT_CMN	ALL	<rdar://60393457>
138S00049	138S0831	ALT_CMN	ALL	<rdar://59975326>
138S00181	138S0835	ALT_CMN	ALL	<rdar://60005148>
138S00291	138S0835	ALT_CMN	ALL	<rdar://60005148>
138S0863	138S0853	ALT_CMN	ALL	<rdar://59969237>
138S00087	138S1086	ALT_CMN	ALL	<rdar://59969145>
152S00398	152S00204	ALT_CMN	ALL	<rdar://60004366>
152S00997	152S00476	ALT_CMN	ALL	<rdar://59975214>
152S00343	152S00839	ALT_CMN	ALL	<rdar://60611255>
152S00979	152S00874	ALT_CMN	ALL	<rdar://59900944>
152S01344	152S00883	ALT_CMN	ALL	<rdar://59451603>
152S00963	152S00885	ALT_CMN	ALL	<rdar://60603921>
152S1130	152S00937	ALT_CMN	ALL	<rdar://60426444>
152S01317	152S01268	ALT_CMN	ALL	<rdar://60004155>
152S01338	152S01287	ALT_CMN	ALL	<rdar://60651969>
155S0384	155S00056	ALT_CMN	ALL	<rdar://60388513>
155S0830	155S0316	ALT_CMN	ALL	<rdar://60395329>
155S00155	155S0441	ALT_CMN	ALL	<rdar://60422558>
155S0660	155S0513	ALT_CMN	ALL	<rdar://59973638>
155S0823	155S0644	ALT_CMN	ALL	<rdar://59974240>
155S00034	155S0706	ALT_CMN	ALL	<rdar://59971765>
197S00295	197S0609	ALT_CMN	ALL	<rdar://59974434>
311S00267	311S00244	ALT_CMN	ALL	<rdar://60436593>
311S00268	311S00246	ALT_CMN	ALL	<rdar://59975911>
311S00203	311S0312	ALT_CMN	ALL	<rdar://65008199>
311S00013	311S0508	ALT_CMN	ALL	<rdar://60005340>
335S00500	335S00494	ALT_CMN	ALL	<rdar://60339904>
353S01505	353S01389	ALT_CMN	ALL	<rdar://60392132>
353S01506	353S01404	ALT_CMN	ALL	<rdar://59969807>
353S02402	353S1429	ALT_CMN	ALL	<rdar://59969324>
353S4376	353S3384	ALT_CMN	ALL	<rdar://59968946>
371S00185	371S00193	ALT_CMN	ALL	<rdar://60425338>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1137	376S00019	ALT_CMN	ALL	<rdar://60005089>
376S00332	376S00074	ALT_CMN	ALL	<rdar://60424909>
376S0855	376S00074	ALT_CMN	ALL	<rdar://60424909>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S00419	107S00001	ALT_CMN	ALL	<rdar://66647460>
107S00109	107S00094	ALT_CMN	ALL	<rdar://60388049>
107S00056	107S00096	ALT_CMN	ALL	<rdar://60427619>
107S00325	107S00232	ALT_CMN	ALL	<rdar://65054196>
128S00039	128S00038	ALT_CMN	ALL	<rdar://60380846>
128S00006	128S00117	ALT_CMN	ALL	<rdar://63415919>
128S0217	128S0385	ALT_CMN	ALL	<rdar://63028367>
138S0750	138S00097	ALT_CMN	ALL	<rdar://65003595>
138S1068	138S00215	ALT_CMN	ALL	<rdar://62540428>
155S0275	155S00188	ALT_CMN	ALL	<rdar://59974104>
155S00076	155S0546	ALT_CMN	ALL	<rdar://66353782>
311S00269	311S00234	ALT_CMN	ALL	<rdar://59976218>
371S00308	371S0684	ALT_CMN	ALL	<rdar://62677103>
376S0948	376S00076	ALT_CMN	ALL	<rdar://65567876>
376S00224	376S00282	ALT_CMN	ALL	<rdar://60005032>
376S1128	376S00282	ALT_CMN	ALL	<rdar://60005032>
376S00001	376S0659	ALT_CMN	ALL	<rdar://60002740>

SYNC_MASTER=aaron SYNC_DATE=12/09/2019

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BOM Alternates

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PACK OPTIONS FOR PRODUCT CONFIGURATION

PACK_OPTIONS TO INCLUDE IN NETLIST
J456

PACK OPTIONS FOR REFERENCE DESIGN CONFIGURATION

PACK_OPTIONS TO INCLUDE IN NETLIST
ENET
USBHC
FTCAM
NO_DFR

REF_SOC_H13G

NA

REF_SE_CERES

PACK_OPTIONS TO INCLUDE IN NETLIST
DESKTOP

REF_PMU_SERA_SIMETRA

PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-25V_D2

REF_VR_3V3_TPS62135

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_DEBUG_UPC0, USBC_SPI_UPC0

REF_USBC_ACE2

NA

REF_1GBE

PACK_OPTIONS TO INCLUDE IN NETLIST
3X_ANTENNA
T664_IPEX
WLBT_DBG_CONN

REF_WIRELESS_RASPUTIN

NA

REF_STORAGE_S5E

REF_SECDIS_SAK
Removed 5/21/2020

NA

REF_CODEC_CLIFDEN

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B

REF_SPKRAMP_SSM3515

CHECKPLUS WAIVERS FOR PRODUCT CONFIGURATION

65 IN SPKRAMP_E_OUT_P CKPLUS_WAIVE=SINGLE_COMP_NET
65 IN SPKRAMP_E_OUT_N CKPLUS_WAIVE=SINGLE_COMP_NET

J456 DRI	SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/SOFT	SYNC_DATE/TIME
AARON	T585	REF_SOC_H13G	5-19	0.69.0	H	2020_09_11
AARON	J456.ABARBER1	MLB	21,236-239	X.X.X	H	See Minor Releases
WILL	T585	REF_SE_CERES	50	0.13.0	H	2020_02_28
VINCENT	J456.VTRIM	MLB	57,123,127	X.X.X	H	See Minor Releases
SAURABH	T585	REF_PMU_SERA_SIMETRA	77-79,81-83	1.6.0	H	2020_04_27
TONY	J456.HURTADOT	MLB	130-137,139,234	X.X.X	H	See Minor Releases
SAURABH	J456.KUMARS3	MLB	142	X.X.X	H	See Minor Releases
PETER	J456.PJOHNSTON	MLB	157,159,166,167	X.X.X	H	See Minor Releases
WILL	J456.WSTEWART	MLB	185,187,188	X.X.X	H	See Minor Releases
WILL	J456.WSTEWART	MLB	189	X.X.X	H	See Minor Releases
ROSSANA	T585	REF_WIRELESS_RASPUTIN	200,201	0.39.0	H	2020_04_28
MICHAEL	T585	REF_STORAGE_S5E	220,221	0.36.0	H	2020_05_04
MICHAEL	T585	REF_STORAGE_NON_OCARINA_SUPPORT	224	0.5.0	H	2020_03_09
DAVID/Ilia	T585	REF_SPKRAMP_SSM3515	244,246	0.8.0	H	2020_09_28
DAVID/Ilia	T585	REF_CODEC_CLIFDEN	245	1.8.0	H	2020_07_13
	J456	MLB	248,249	X.X.X	H	See Minor Releases

SYNC_MASTER=aaron SYNC_DATE=10/10/2019

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Pack Options

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