

**COMPAL
CONFIDENTIAL**

MODEL NAME : DAP20

PCB NO : LA-F601P

BOM P/N : 451A9F31LXX

GPIO MAP: Gen9 GPIO Master_XXXX



WHITEHAVEN 17

Coffee Lake H-type (2 chip)

REV : 1.0(A00)

2018.03.11

- @ : Nopop Component**
- EMC@, RF@, ESD@, EMC@ : EMI/ESD/RF part POP**
- CONN@ : Connector Component**
- XDP@ : Total debug Component (pop them until ST)**
- DS3@ : Deep sleep support**
- NDS3@ : non Deep sleep support**
- LPC@ : LPC interface**
- eSPI@ : eSPI interface**

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1707-03

Part Number	Description
DAB0002L000	PCB 26K LA-F602P REV0 MB AR 3

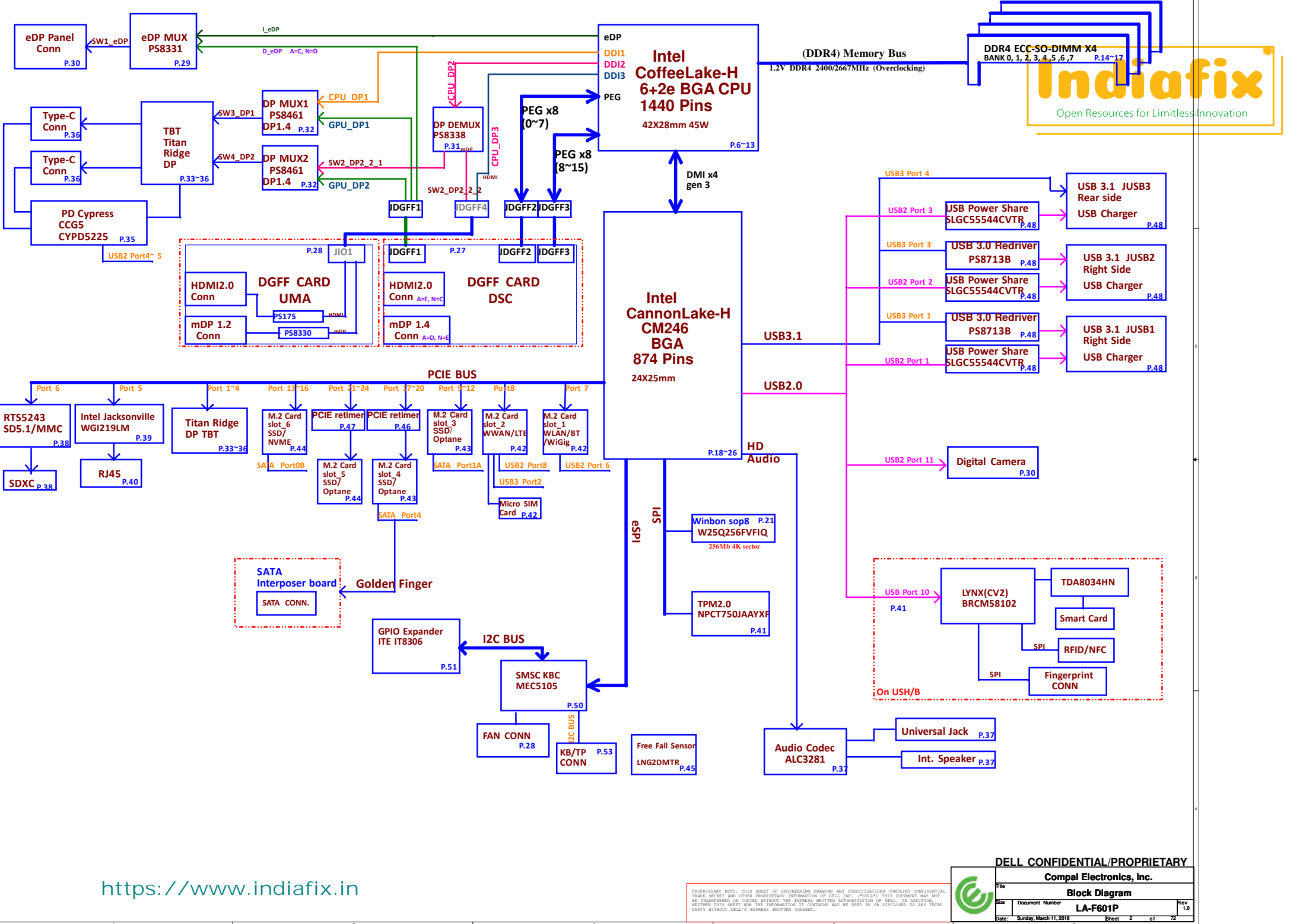
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Compal Electronics, Inc.		
Cover Sheet		
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		Block Diagram	
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	ON	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	ON	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF

PM TABLE

State \ power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM +1.8V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.2V_RUN +3.3V_DGFF +5V_DGFF +DGFF_PWR_SRC +0.675V_DDR_VTT	(M-OFF) +VCC_CORE +VCC_GT +VCC_IO +VCC_SA +1.0V_VCCSTG +1.8V_RUN
S0	ON	ON	ON	ON
S3	ON	ON	OFF	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF

PCH	USB2 PORT#	DESTINATION
	1	JUSB1
	2	JUSB2
	3	JUSB3
	4	Cypress PD
	5	Cypress PD
	6	NA
	7	NA
	8	M.2 Slot-2 (WWAN/LTE)
	9	17" NA/ 15" Touch screen
	10	USH
	11	Camera
	12	NA
	13	NA
14	M.2 Slot-1 (BT)	

USH	0	BIO
	1	NA



PCI EXPRESS	DESTINATION
PORT 1~4	TBT-Titan Ridge
PORT 5	10/100/1G LOM
PORT 6	MMI(Card reader)
PORT 7	M.2 Slot-1 (WLAN/Wigig)
PORT 8	M.2 Slot-2 (WWAN/LTE)
Lane 9~12	SLOT3 SSD 2280/ Optane
PORT13~16	SLOT6 SSD 2280/NVME
PORT17~20	SLOT4 SSD 2280/ Optane
PORT21~24	SLOT5 PCIE only 2280/ Optane

USB3.0	DESTINATION
Port 1	JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE)
Port 3	JUSB2
Port 4	JUSB3
Port 5	NA
Port 6	NA

SATA	DESTINATION
SATA 0B	SLOT6 SSD
SATA 1A	SLOT3 SSD
SATA 2	NA
SATA 3	NA
SATA 4	SLOT4 SSD/HDD
SATA 5	NA

Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	GA-150LL	0.5
		Add Plating		0.95
Top	3.7	Copper foil	0.5oz	0.65
	3.7	Prepreg	1086	2.7
GND/VCC	3.7	Copper foil	1oz	1.3
	3.8	Core	2116	4
IN1	3.8	Copper foil	0.5oz	0.65
	3.8	Prepreg	2116	4.65
GND/VCC	3.8	Copper foil	0.5oz	0.65
	3.8	Core	4mil	4
IN2	3.8	Copper foil	0.5oz	0.65
	3.8	Prepreg	2116	4.65
GND/VCC	3.8	Copper foil	1oz	1.3
	3.8	Core	2116	4
GND/VCC	3.8	Copper foil	1oz	1.3
	3.8	Prepreg	2116	4.65
IN3	3.8	Copper foil	0.5oz	0.65
	3.8	Core	4mil	4
GND/VCC	3.8	Copper foil	0.5oz	0.65
	3.8	Prepreg	2116	4.65
IN4	3.8	Copper foil	0.5oz	0.65
	3.8	Core	2116	4
GND/VCC	3.8	Copper foil	1oz	1.3
	3.7	Prepreg	1086	2.7
Bottom	3.7	Copper foil	0.5oz	0.65
		Add Plating		0.95
		SolderMask		0.5
Overall Thickness (1.45mm ±0.05)			57.8	1.8342

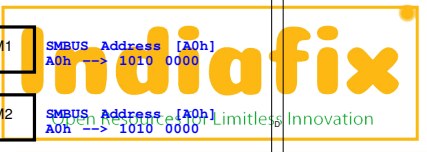
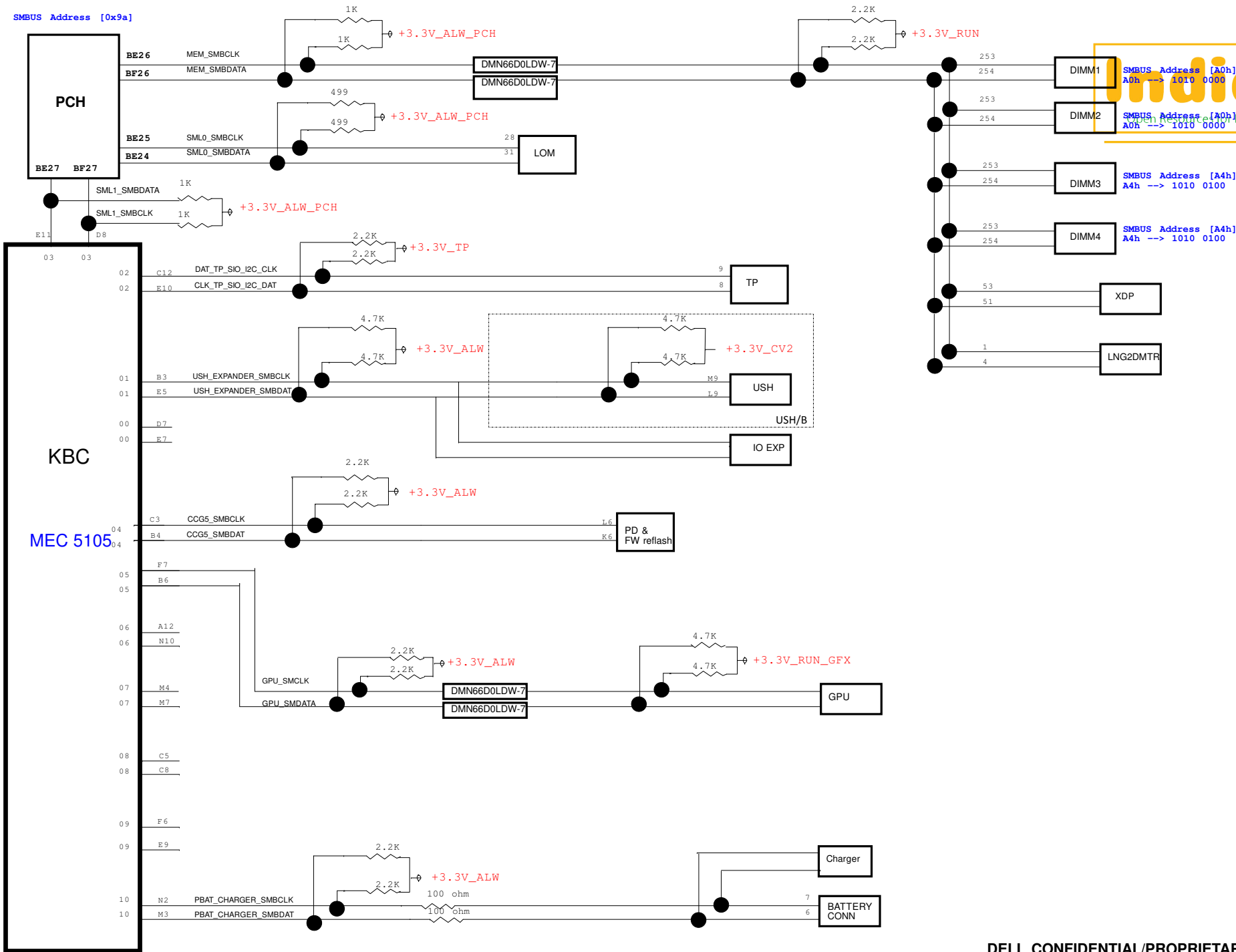
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SMBUS Address [0x9a]



MEC 5105

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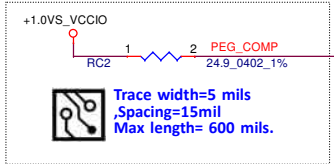
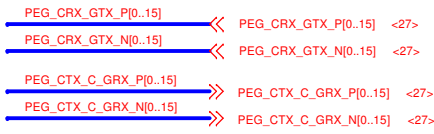
SMBUS Bolck Diagram

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CFL-H

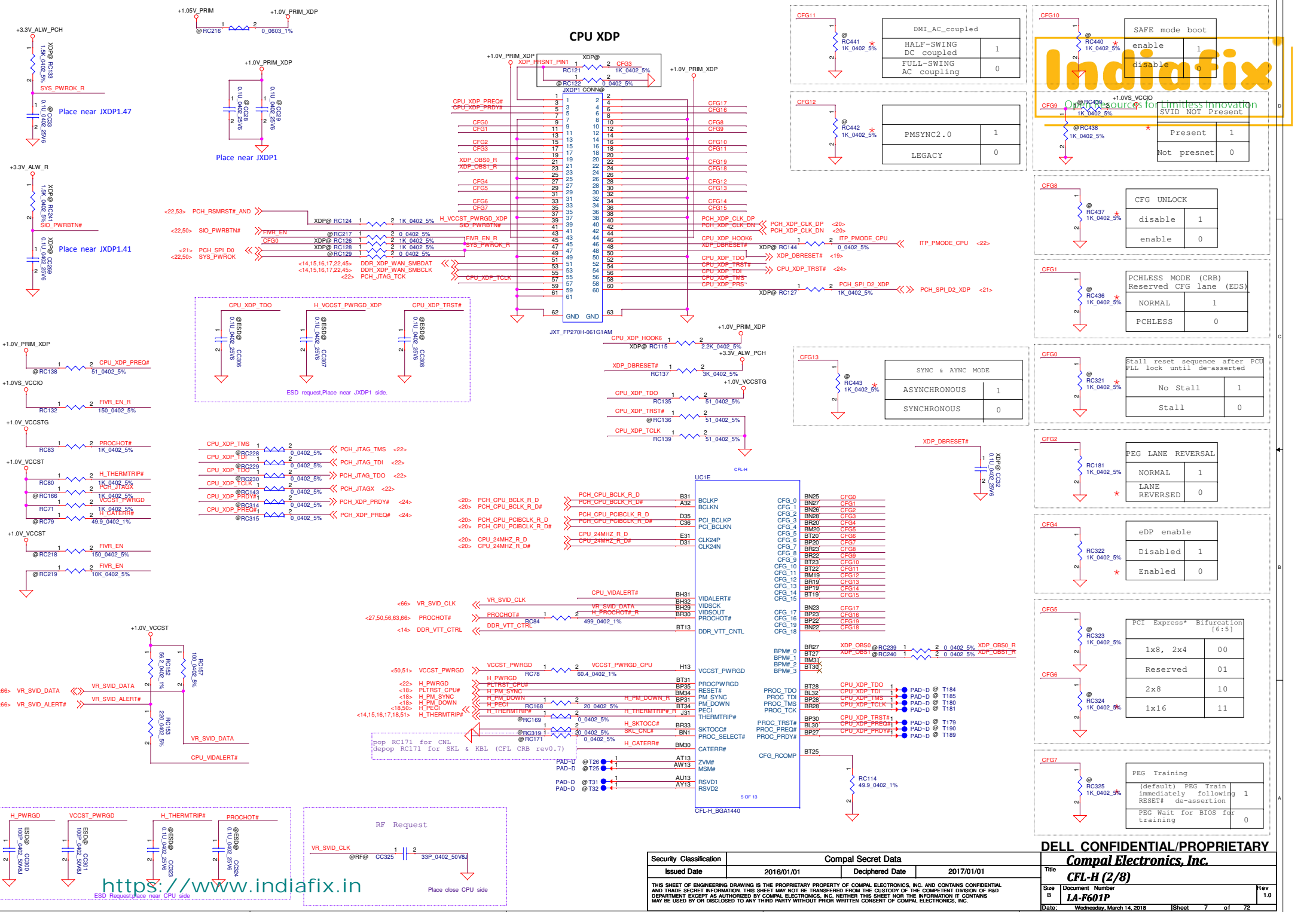
UC1C

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CFL-H_BGA1440



CPU XDP

CFG1

DMI_AC_coupled	
HALF-SWING DC coupled	1
FULL-SWING AC coupling	0

CFG10

SAFE mode boot	
enable	1
disable	0

CFG12

PMSYNC2.0	1
LEGACY	0

CFG9

Limitless Innovation	
Present	1
Not presnet	0

CFG8

CFG UNLOCK	
disable	1
enable	0

CFG1

PCHLESS MODE (CRB) Reserved CFG lane (EDS)	
NORMAL	1
PCHLESS	0

CFG13

SYNC & AYNC MODE	
ASYNCHRONOUS	1
SYNCHRONOUS	0

CFG0

Stall reset sequence after PCU PLL lock until de-asserted	
No Stall	1
Stall	0

CFG2

PEG LANE REVERSAL	
NORMAL	1
LANE REVERSED	0

CFG4

eDP enable	
Disabled	1
Enabled	0

CFG5

PCI Express* Bifurcation [6:5]	
1x8, 2x4	00
Reserved	01
2x8	10
1x16	11

CFG6

PEG Training	
(default) PEG Train immediately following 1 RESET# de-assertion	
PEG Wait for BIOS for training	0

CFG7

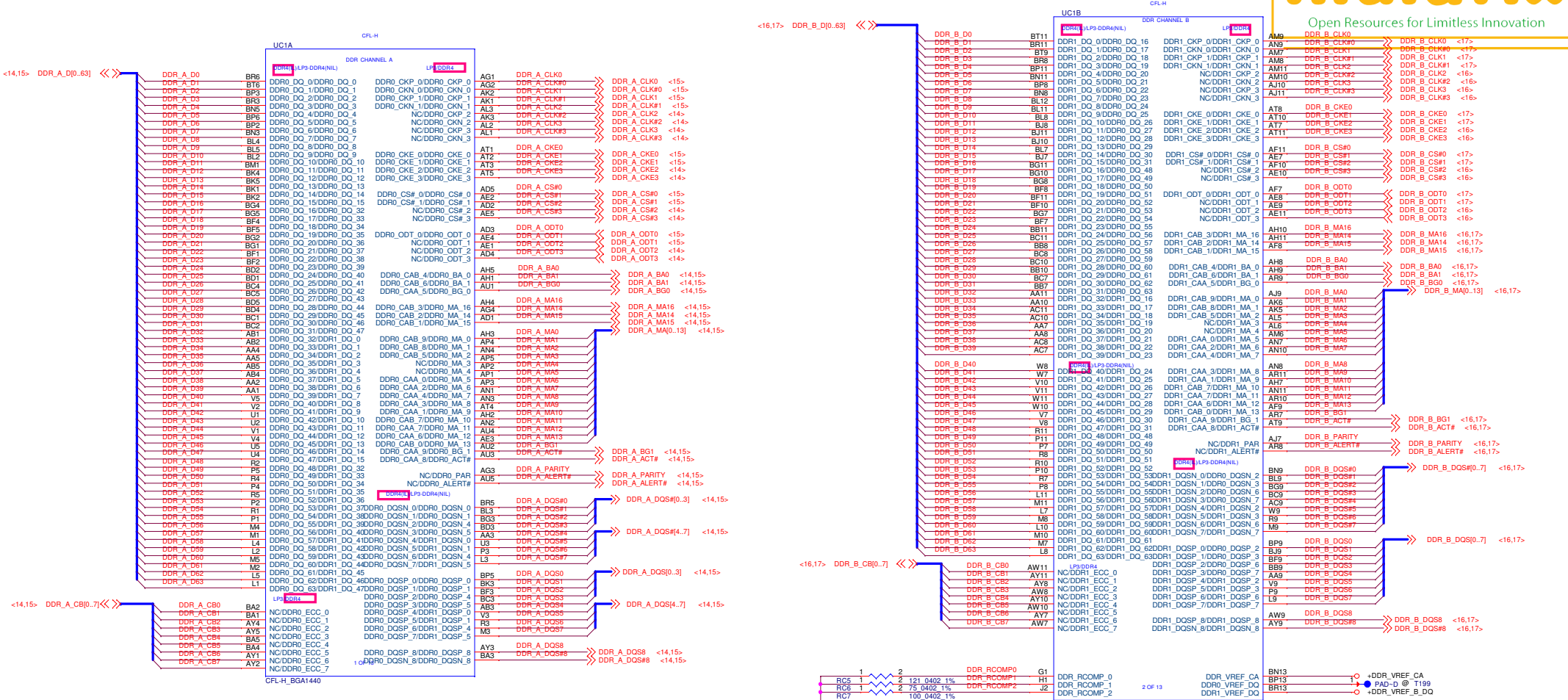
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(default) PEG Train immediately following 1 RESET# de-assertion	
PEG Wait for BIOS for training	0

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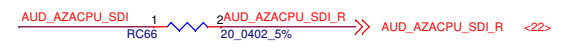
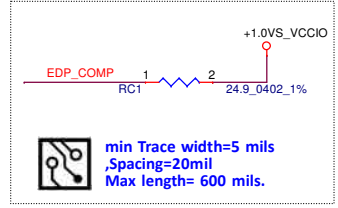
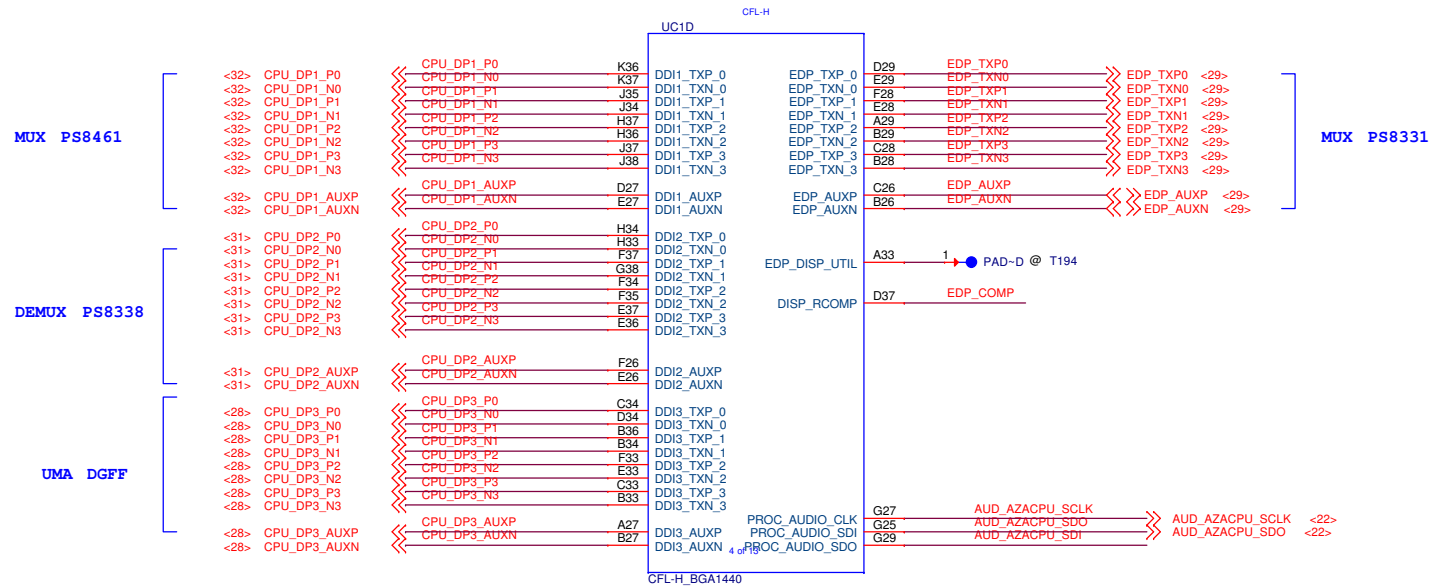
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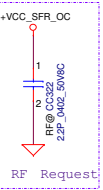
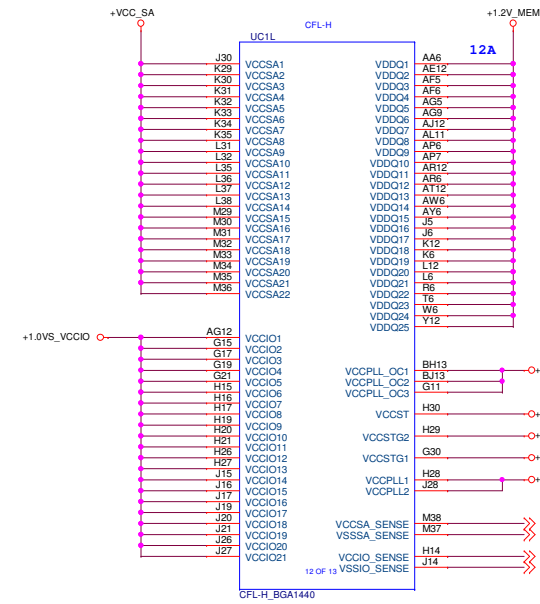
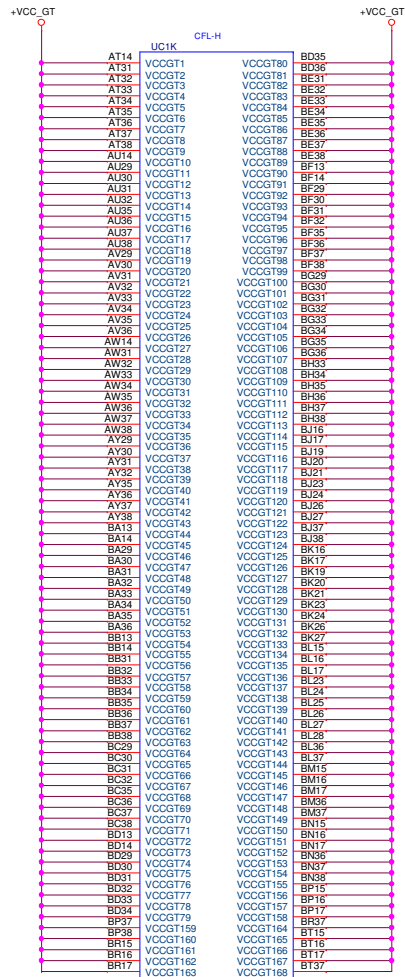
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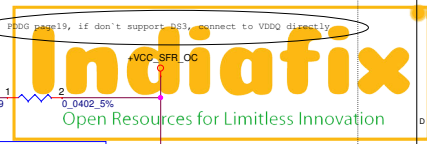
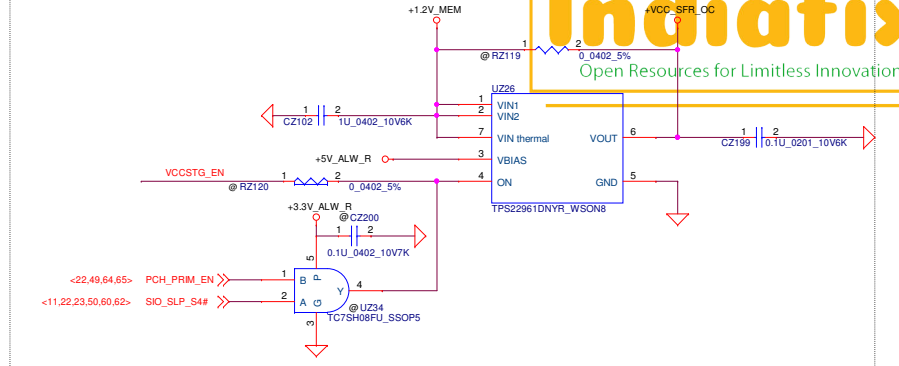


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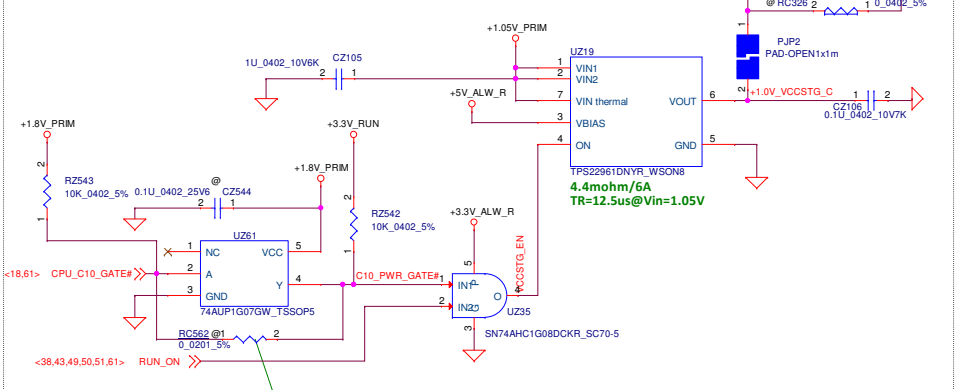
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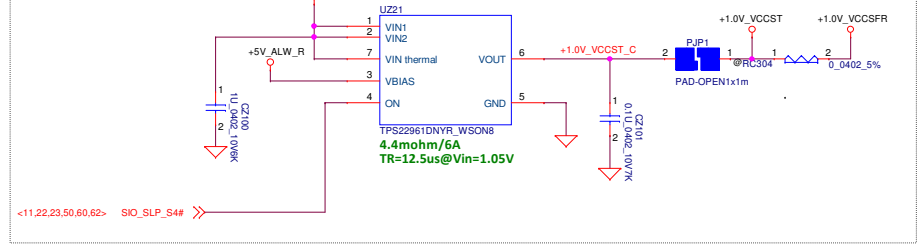
+VCCPLL_OC source



+1.0V_VCCSTG source

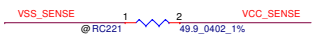
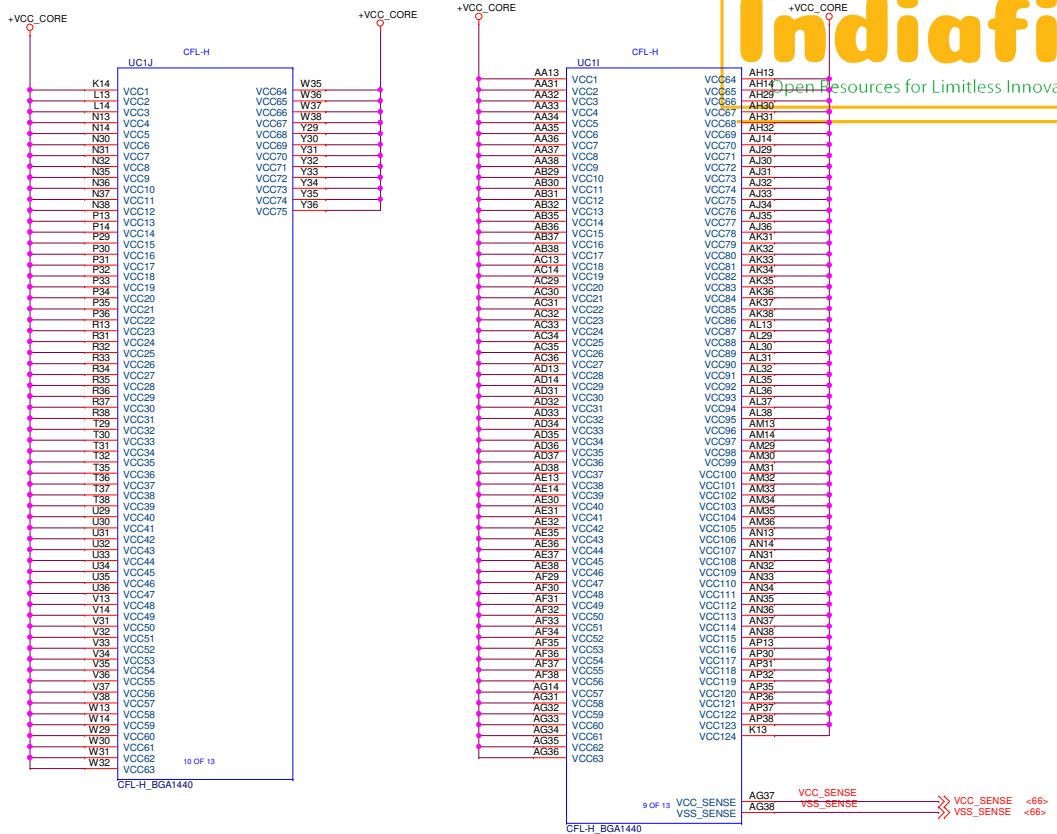
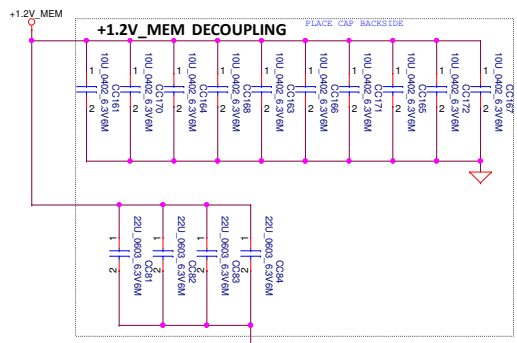
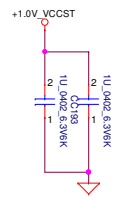
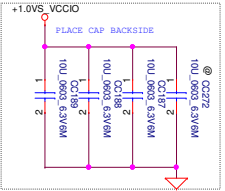
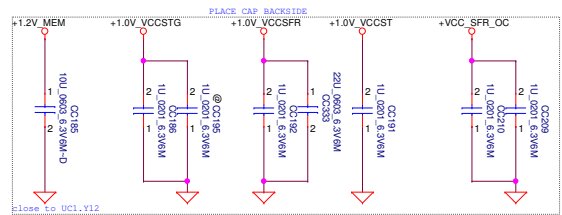


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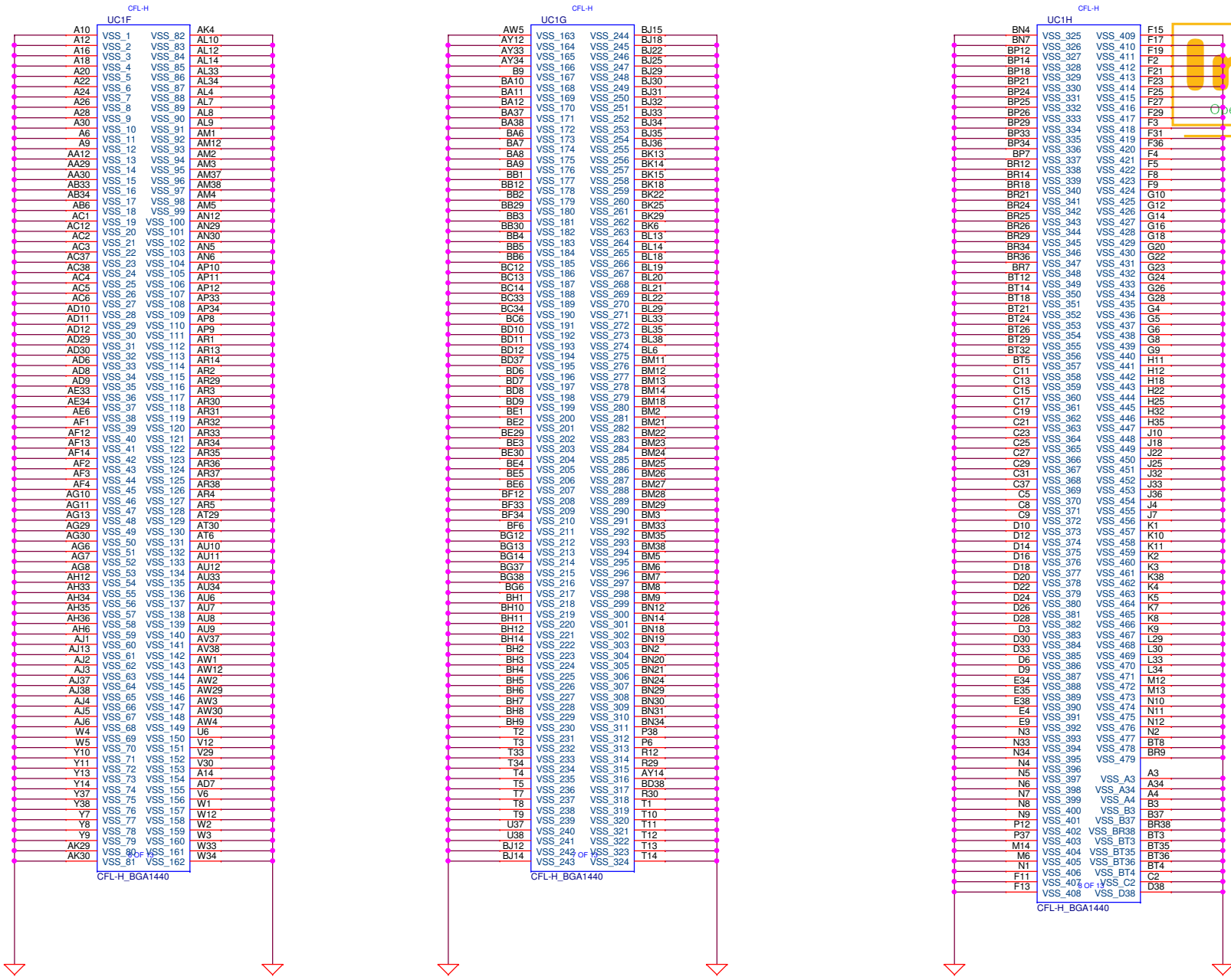
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				Size	
				Document Number	
				LA-F601P	
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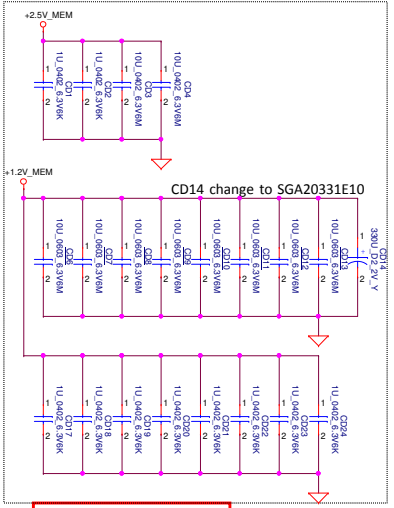
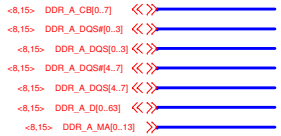
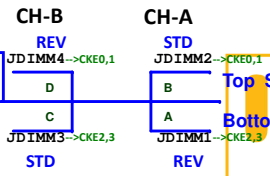
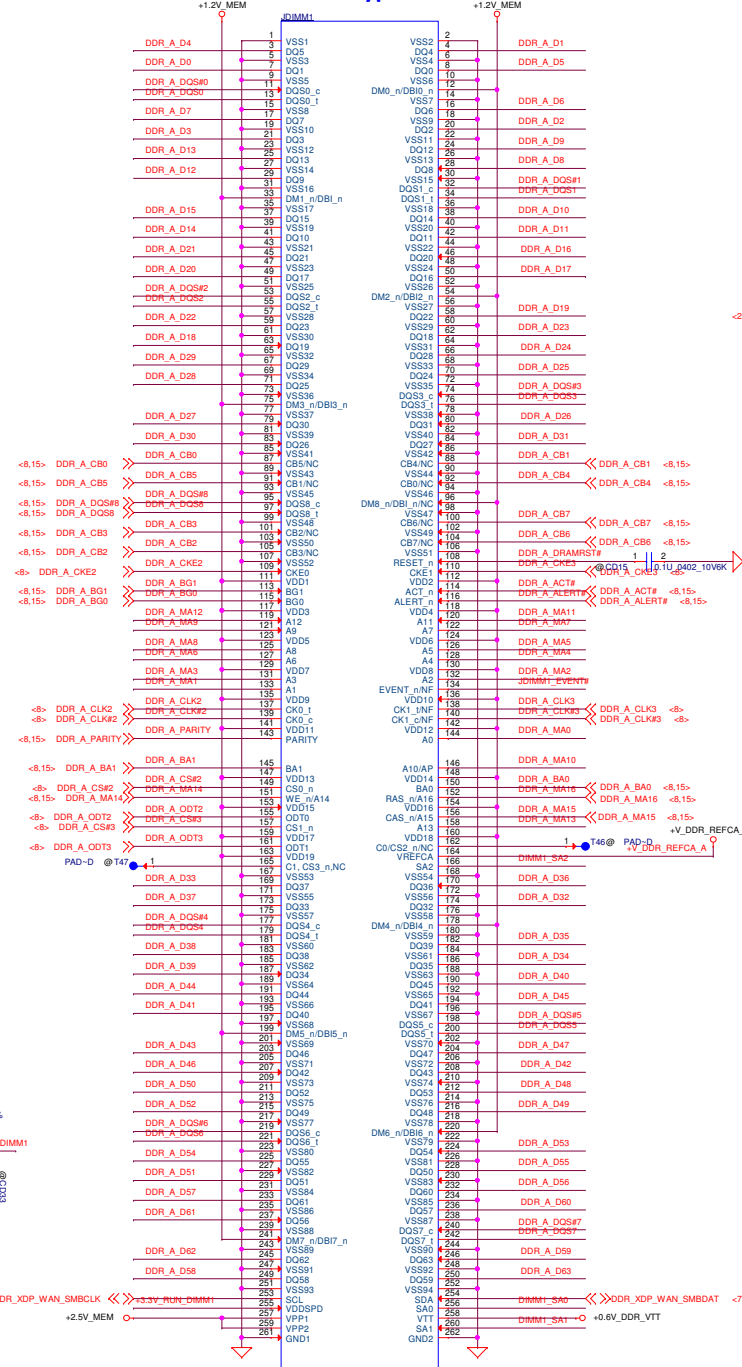
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Size	Document Number	Rev
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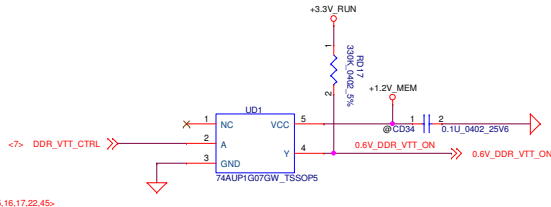
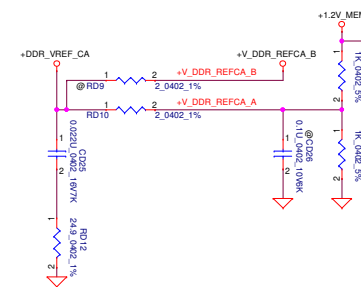
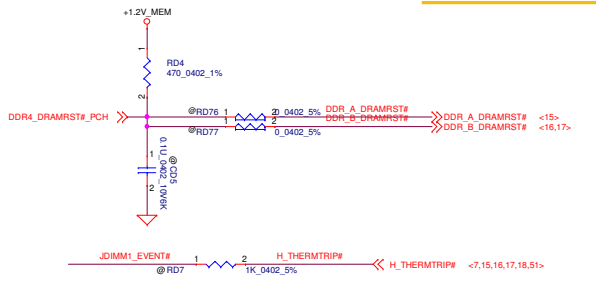
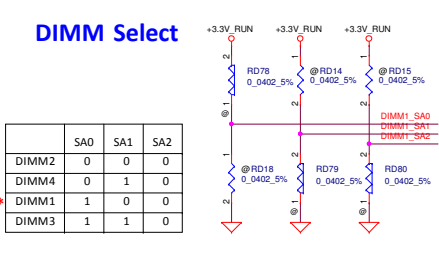
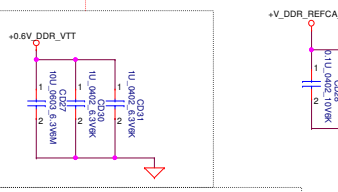
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All VREF traces should have 10 mil trace width

JDIMM1 REV Type H=5.2



Layout Note: Place near JDIMM1.258



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Compal Electronics, Inc.

DDRIII-SODIMM SLOT1

LA-F601P

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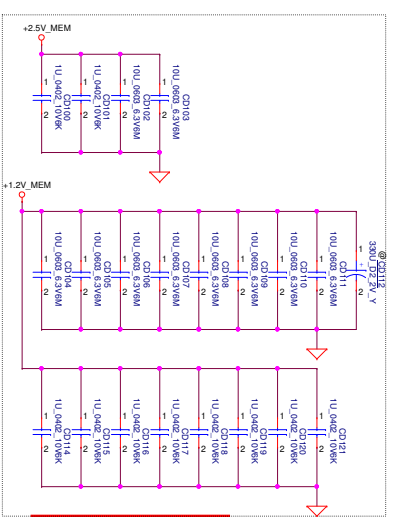
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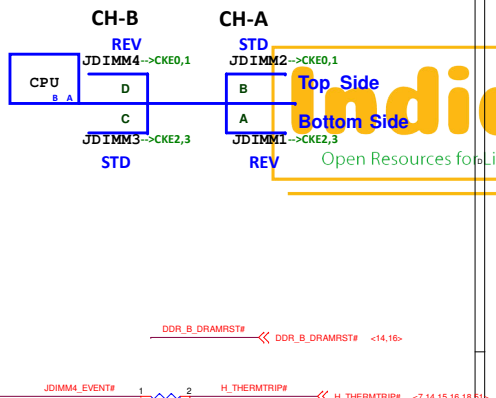
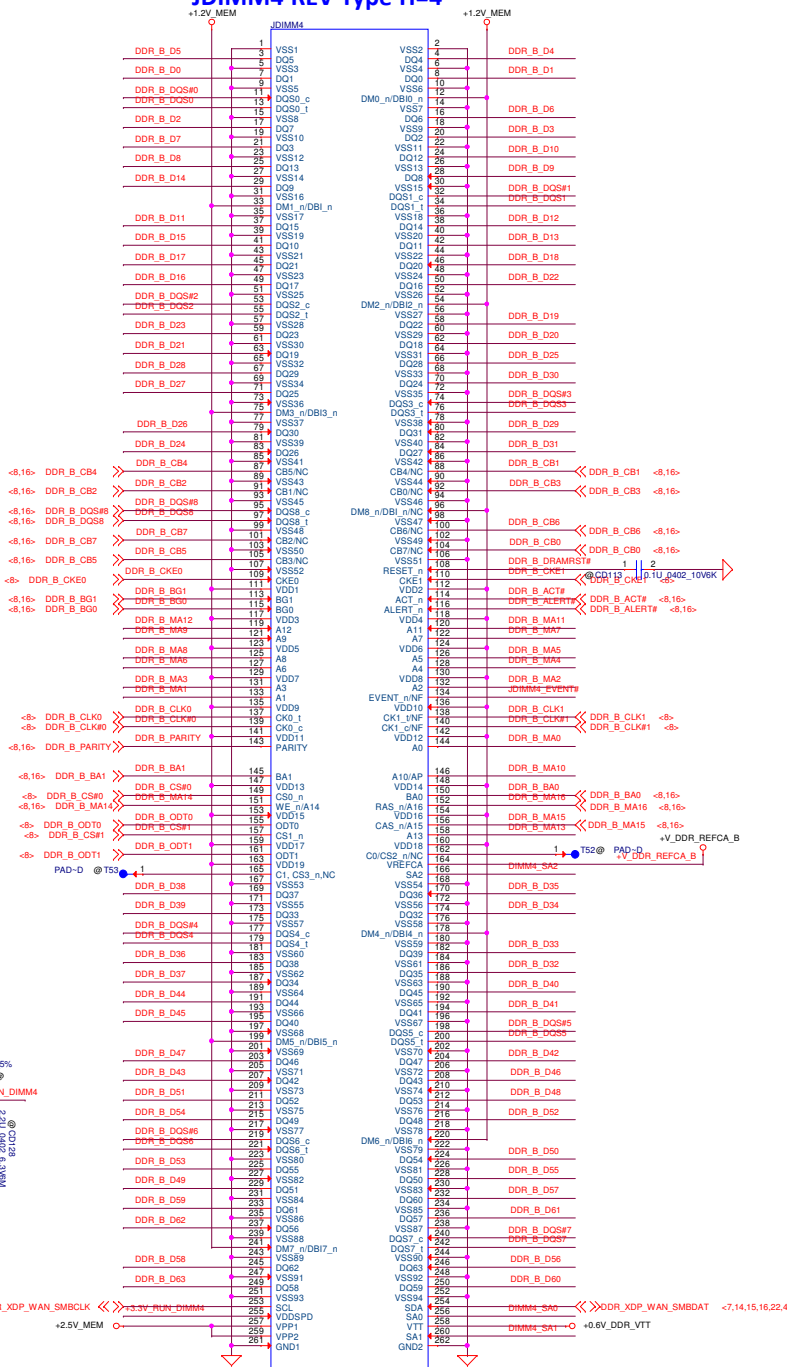
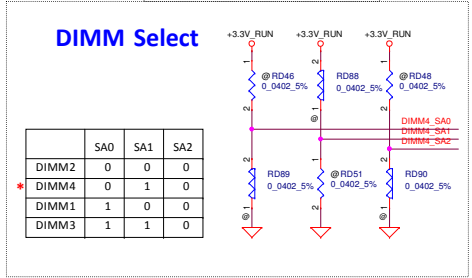
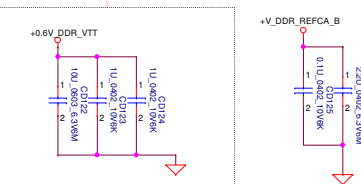
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JDIMM4 REV Type H=4

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- <-8.16> DDR_B_DQS[0..7] <<>
- <-8.16> DDR_B_DQS#0..7 <<>
- <-8.16> DDR_B_D[0..63] <<>
- <-8.16> DDR_B_MA[0..13] <<>



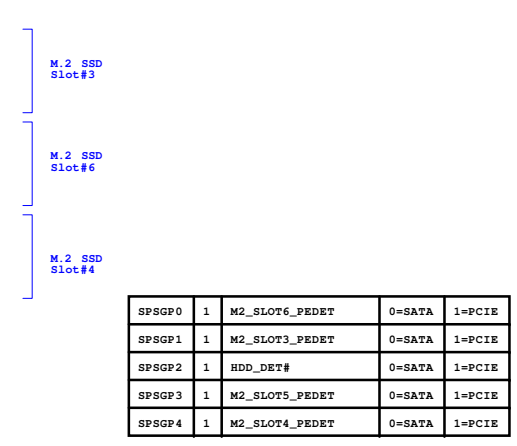
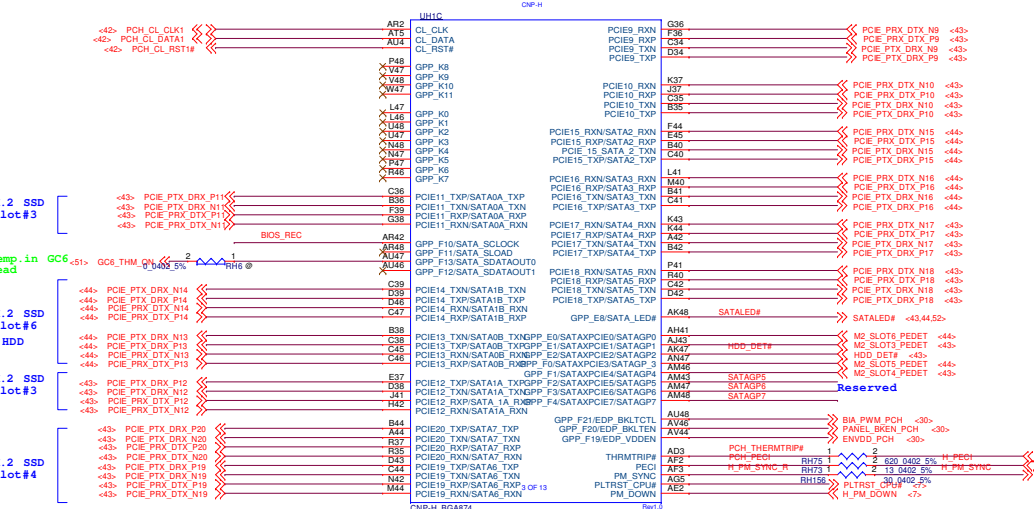
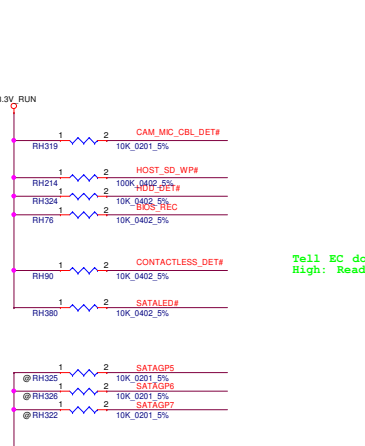
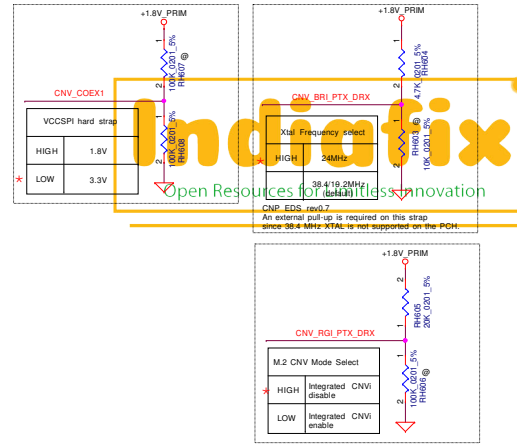
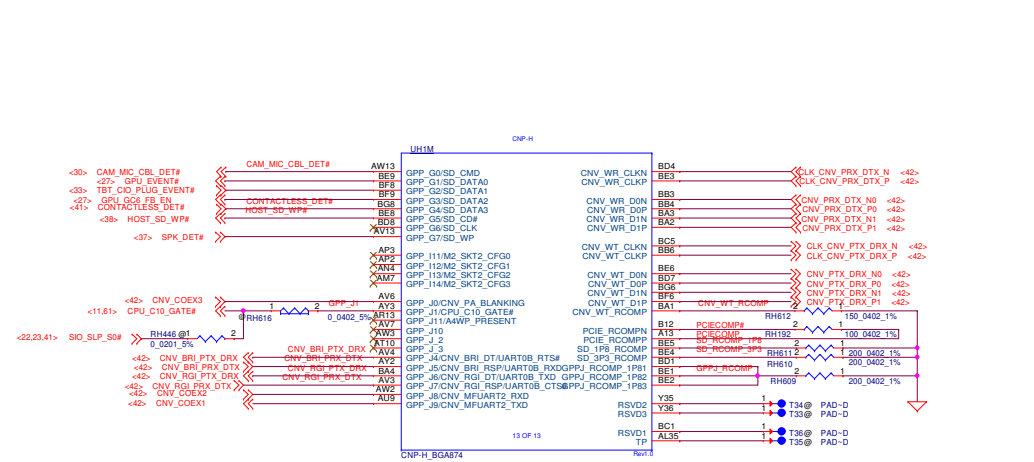
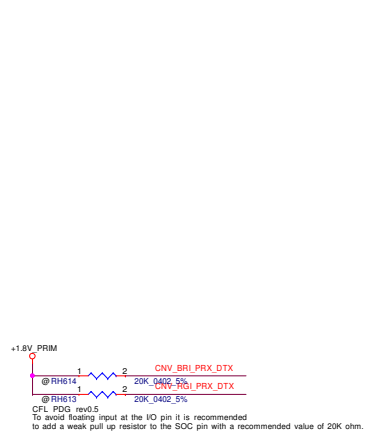
Layout Note:
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Tell EC don't read GFX Temp in GC6 (s1)
High: Read; Low: Don't read

SFSPG#	1	M2_SLOT#_PEDET	0=SATA	1=PCIE
SFSPG1	1	M2_SLOT3_PEDET	0=SATA	1=PCIE
SFSPG2	1	HDD_DET#	0=SATA	1=PCIE
SFSPG3	1	M2_SLOT5_PEDET	0=SATA	1=PCIE
SFSPG4	1	M2_SLOT4_PEDET	0=SATA	1=PCIE

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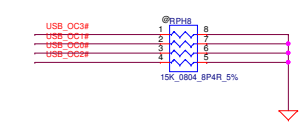
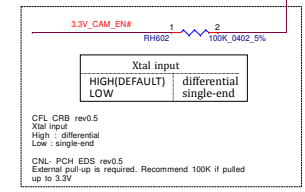
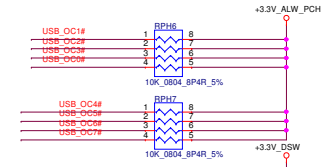
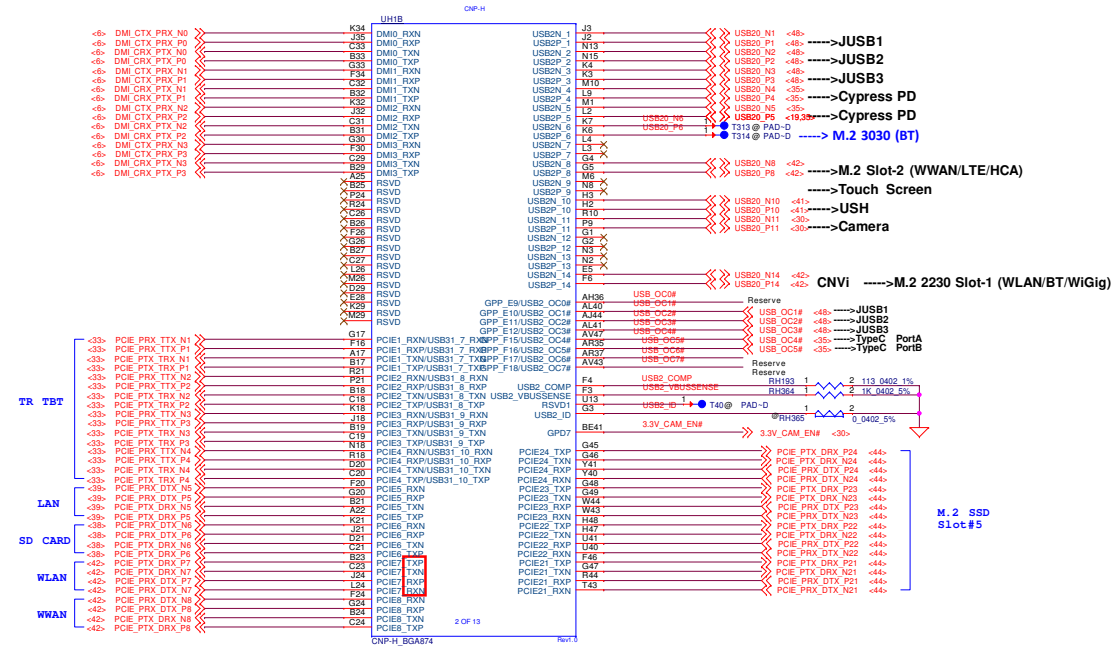
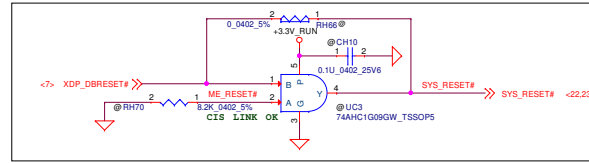
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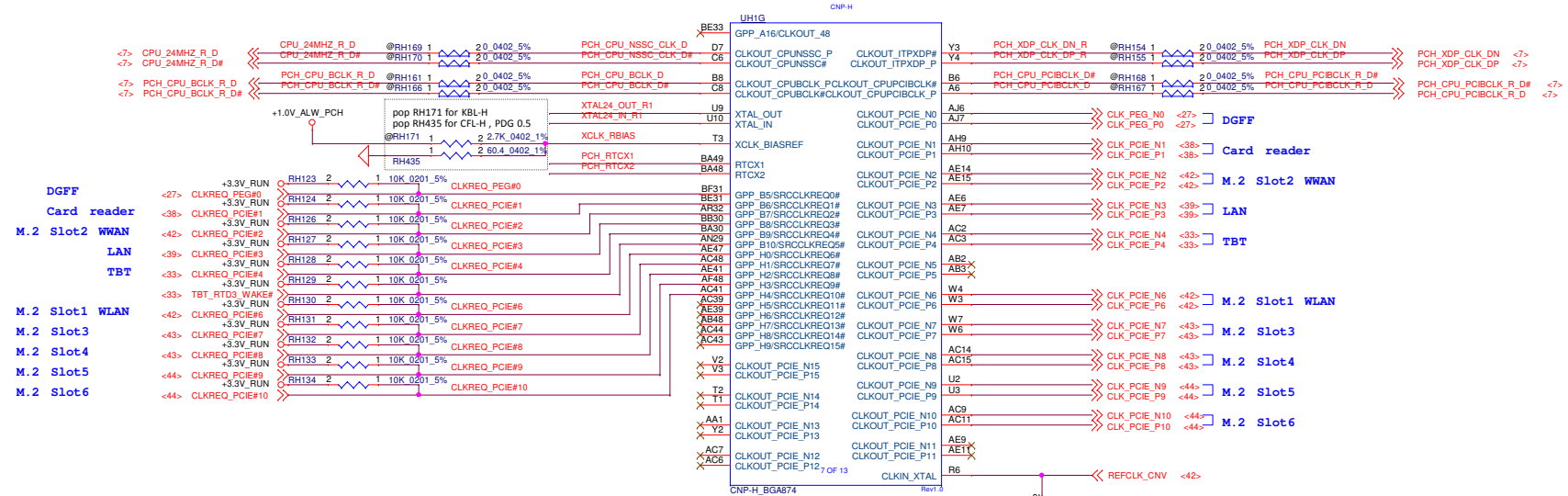
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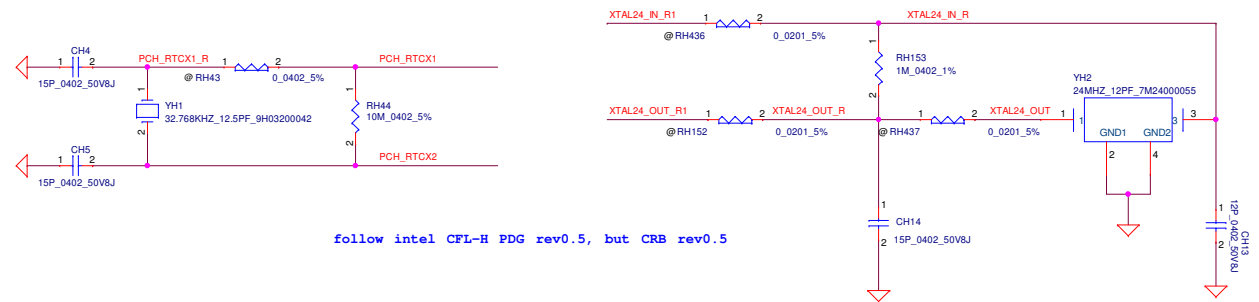
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CannonLake PCH-H (2/9)

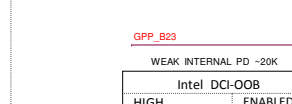
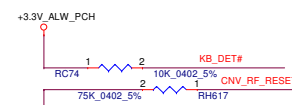
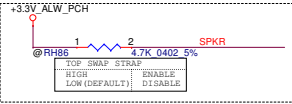
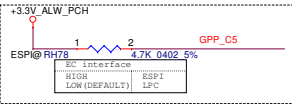
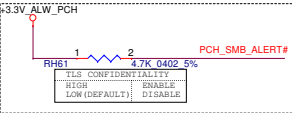
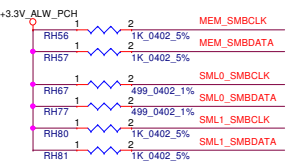
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- DGFF
- Card reader
- M.2 Slot2 WWAN
- LAN
- TBT
- M.2 Slot1 WLAN
- M.2 Slot3
- M.2 Slot4
- M.2 Slot5
- M.2 Slot6



follow intel CFL-H PDG rev0.5, but CRB rev0.5



WEAK INTERNAL PD ~20K

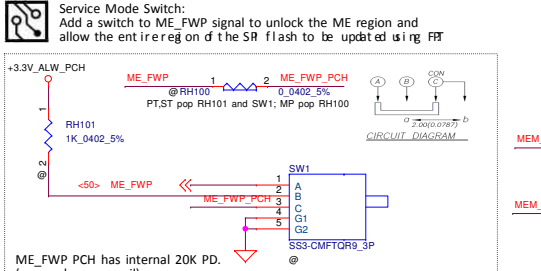
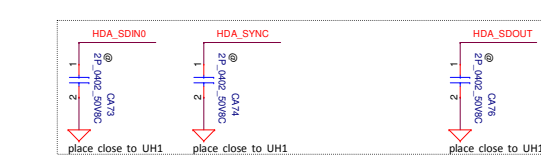
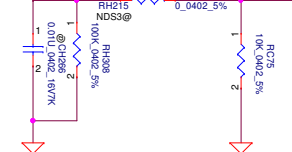
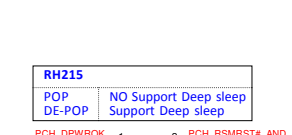
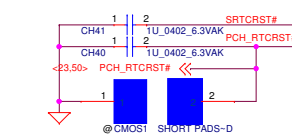
Intel DCI-OOB

HIGH LOW(DEFAULT) ENABLED DISABLED

If USB 3.0 Port 1 is used for 4-wire DCIOOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.

If USB 3.0 Port 1 is used for DCIOOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.

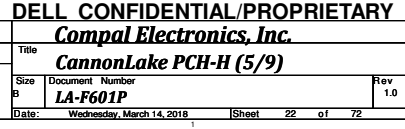
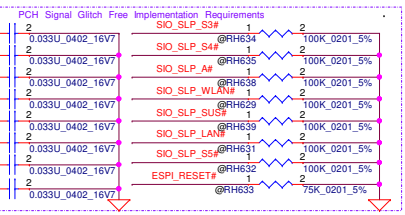
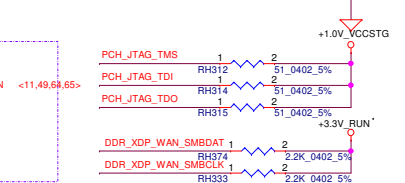
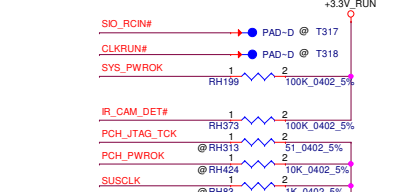
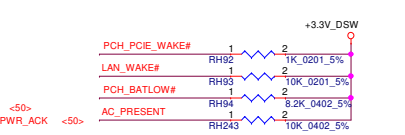
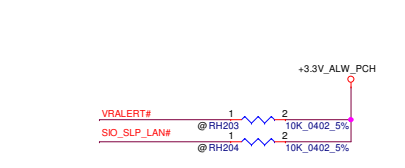
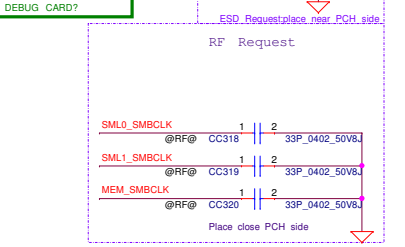
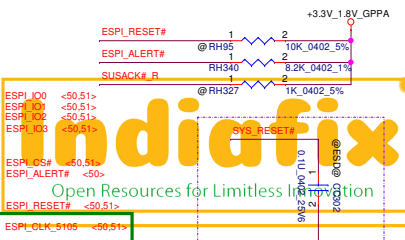
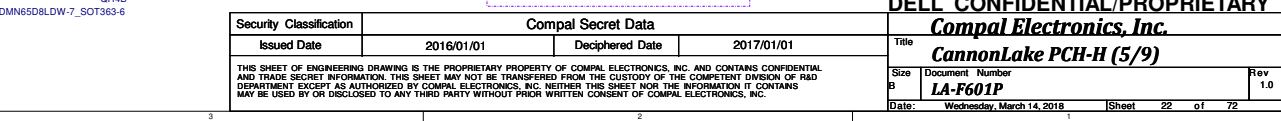
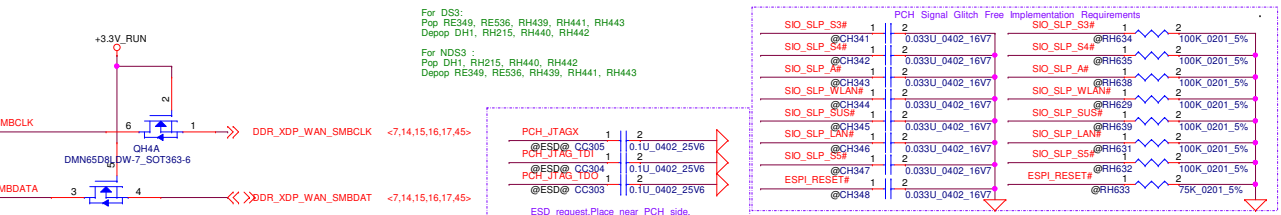
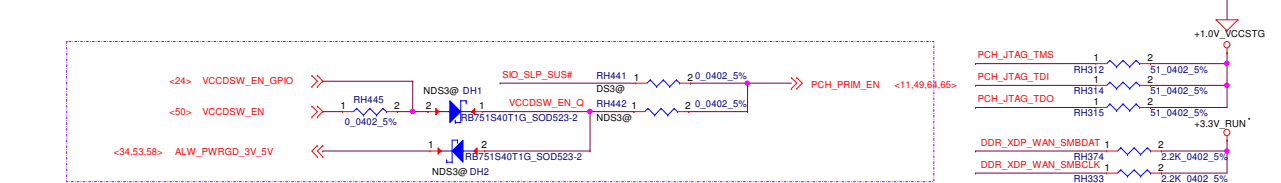
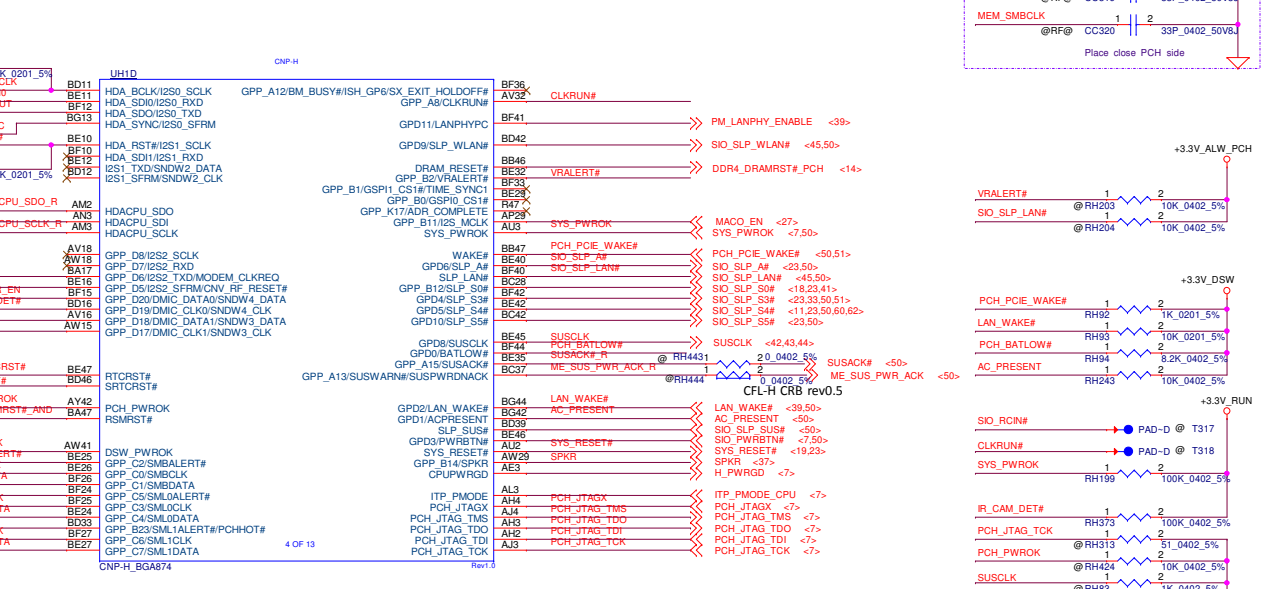
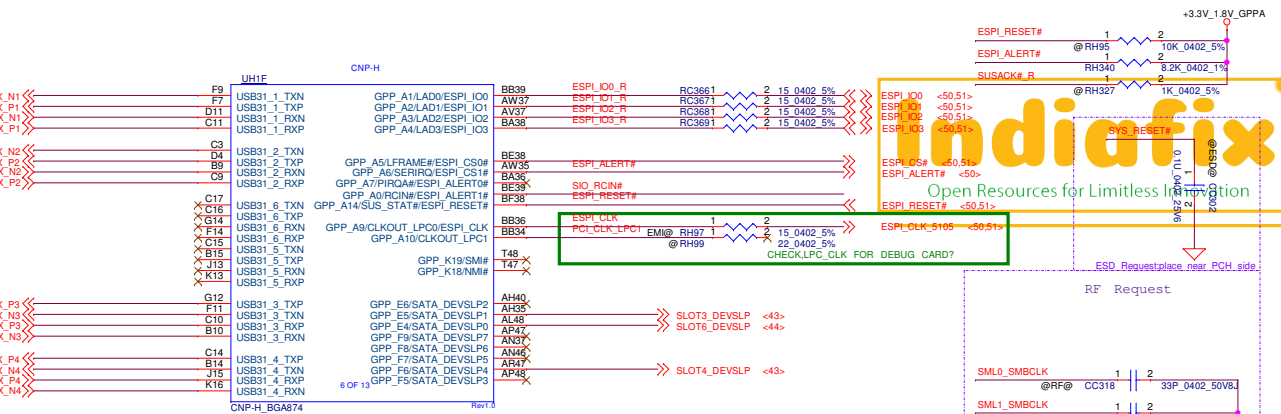
If DCIOOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.



ME_FWP_PCH has internal 20K PD. (suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE

For ME FWP (DEFAULT) Pin1 & Pin3 short HIGH = DISABLE (ME can update) --> Pin2 & Pin3 short



RF Request

ESD Request place near PCH side.

Place close PCH side

ESD request place near PCH side.

ESD request place near PCH side.

ESD request place near PCH side.

ESD request place near PCH side.

ESD request place near PCH side.

ESD request place near PCH side.

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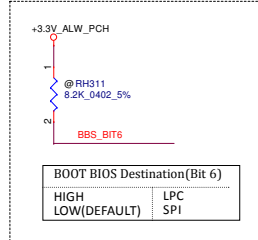
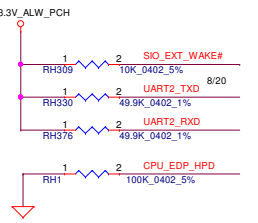
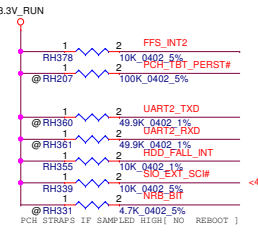
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CanonLake PCH-H (5/9)

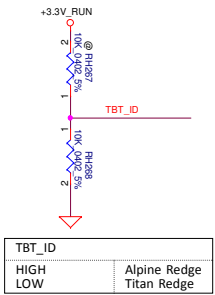
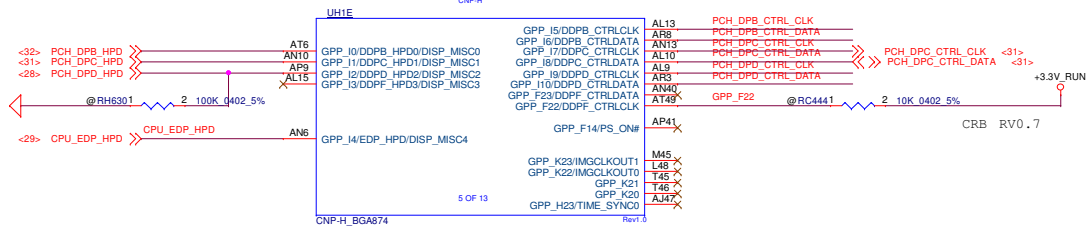
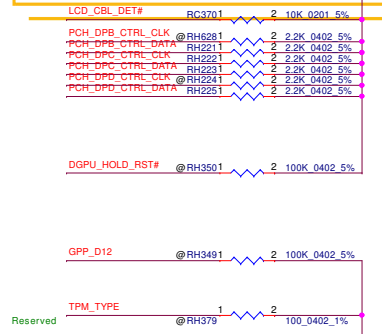
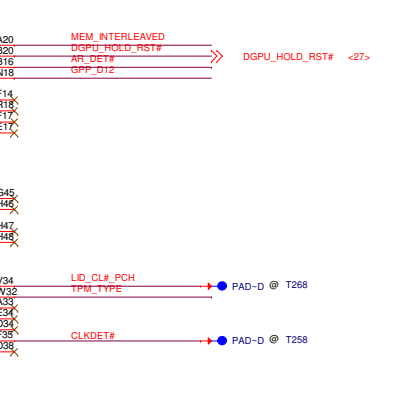
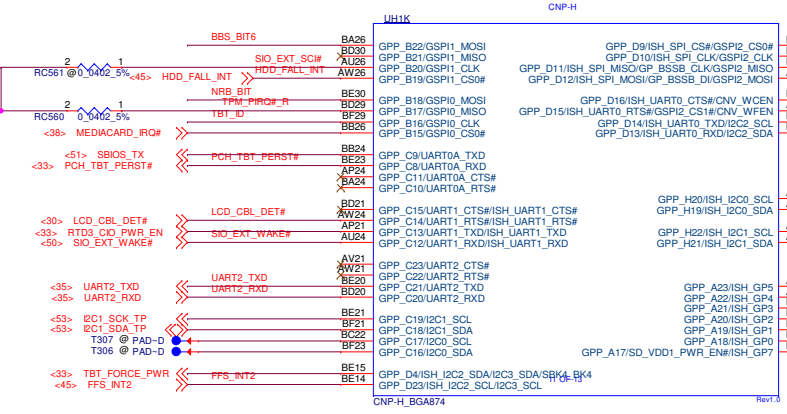
Size B Document Number **LA-F601P** Rev 1.0

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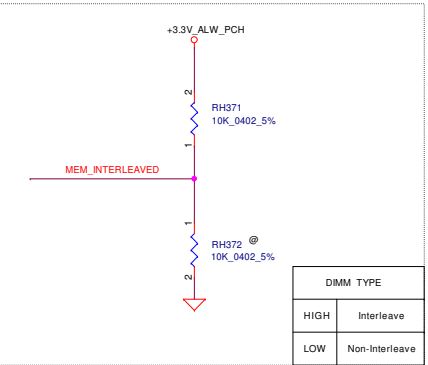
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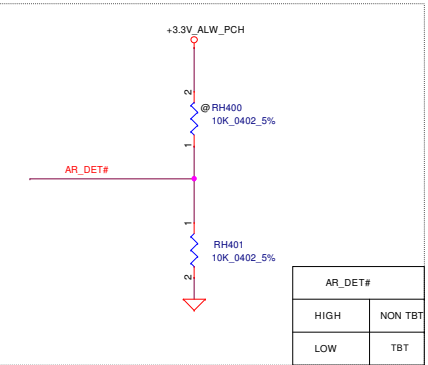
BOOT BIOS Destination (Bit 6)	
HIGH	LPC
LOW (DEFAULT)	SPI



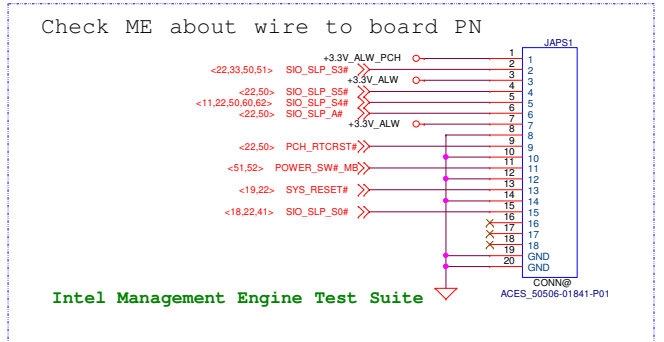
TBT_ID	
HIGH	Alpine Redge
LOW	Titan Redge



DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave



AR_DET#	
HIGH	NON TBT
LOW	TBT

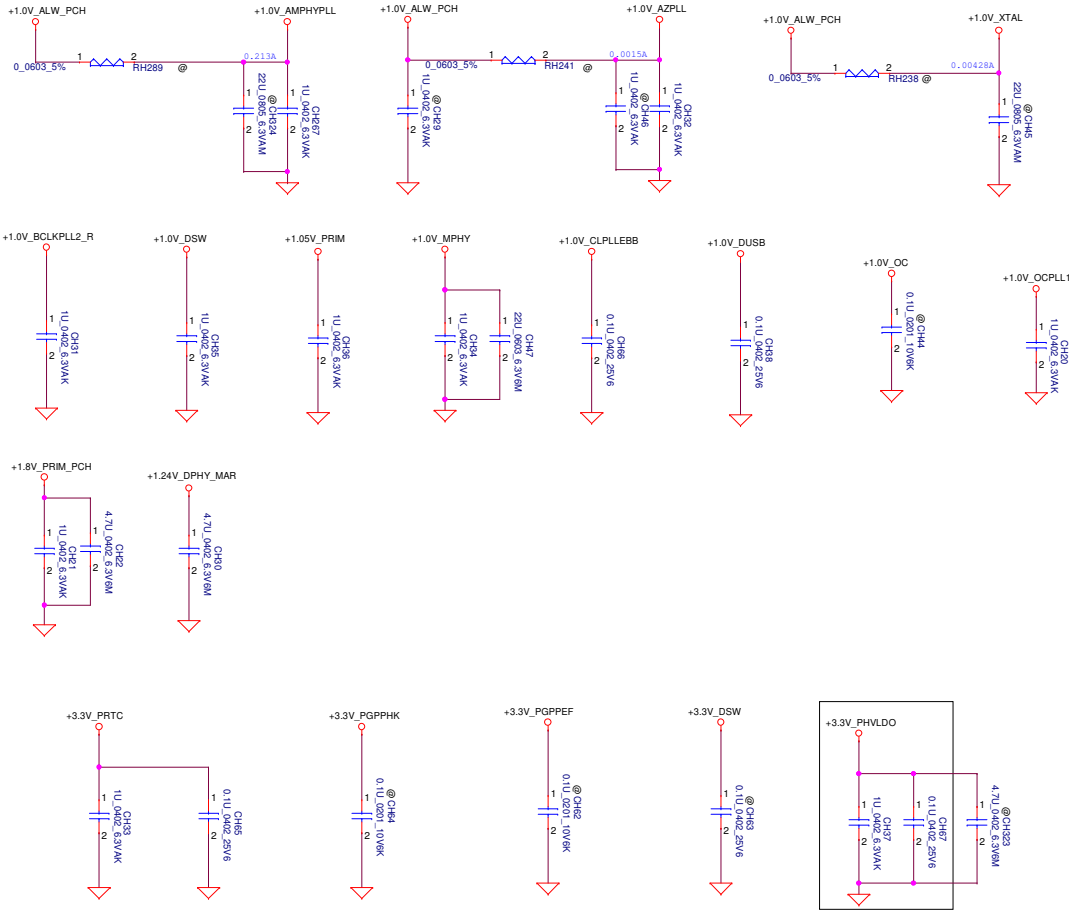


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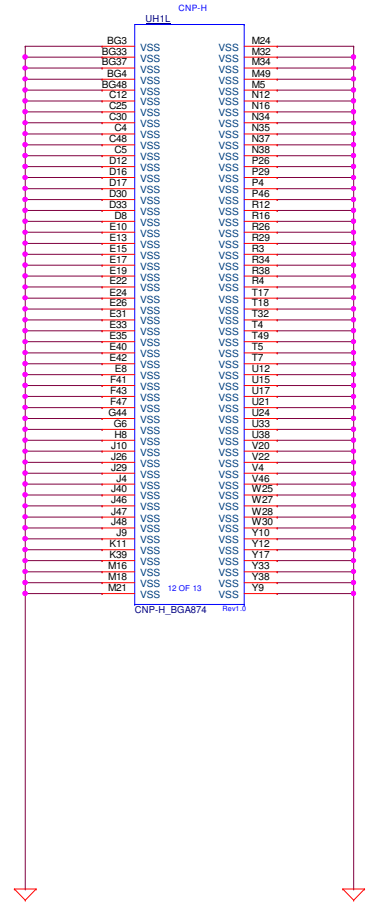
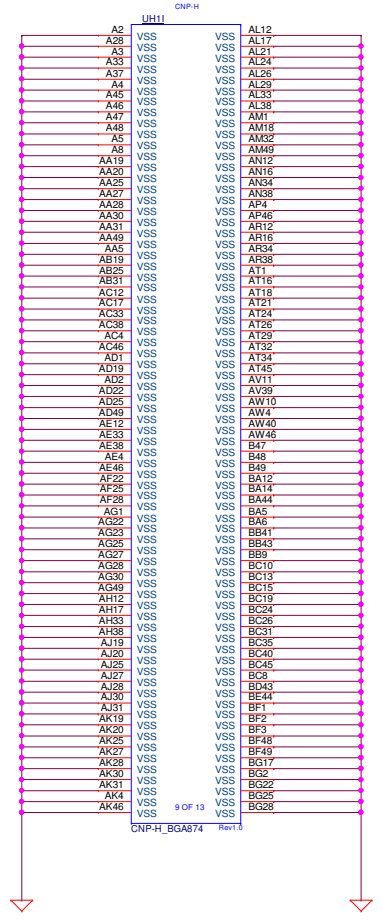
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CannonLake PCH-H (6/9)		
Size	Document Number	Rev
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CFL-H PDG rev0.5
4.7uF x1

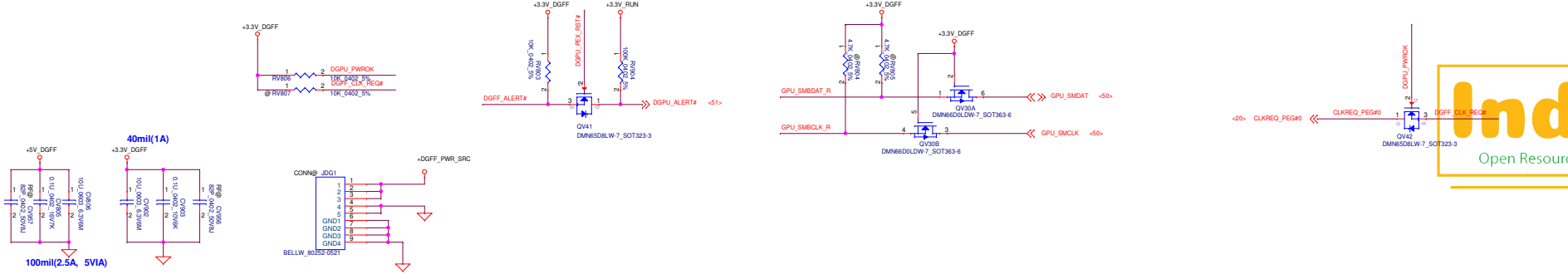
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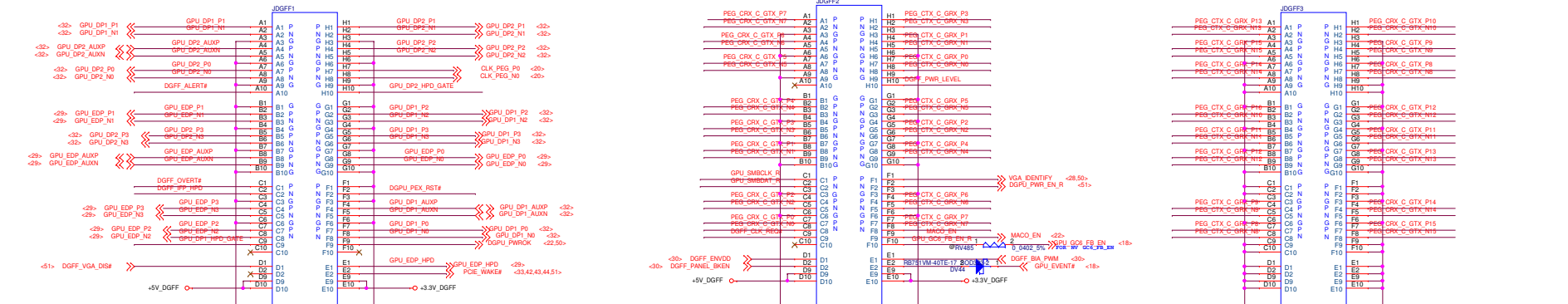
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2 DP channels from GPU
(A & B & EDP)

PCIe x8 Lanes 0-7

PCIe x8 Lanes 8-15

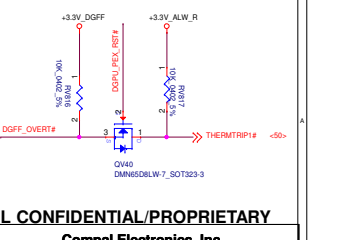
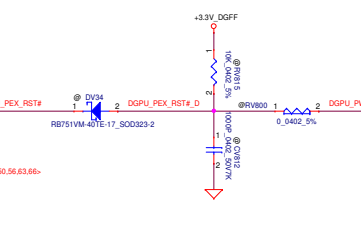
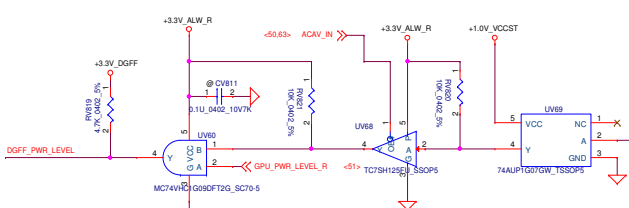
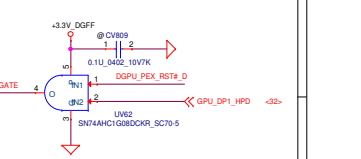
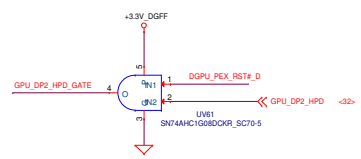
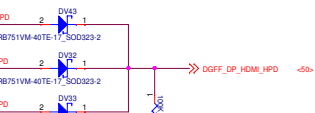


X-Beam I/per pin=0.5A
I/per connector=0.75A

TBT/DP MUX1 PortA
TBT/DP MUX2 PortB
eDP MUX PortC

Component	Value	Part Number	Notes
REG_CRX_GTX_P0	1	0.22u 0402 187K	REG_CRX_C_GTX_P0
REG_CRX_GTX_P1	1	0.22u 0402 187K	REG_CRX_C_GTX_P1
REG_CRX_GTX_P2	1	0.22u 0402 187K	REG_CRX_C_GTX_P2
REG_CRX_GTX_P3	1	0.22u 0402 187K	REG_CRX_C_GTX_P3
REG_CRX_GTX_P4	1	0.22u 0402 187K	REG_CRX_C_GTX_P4
REG_CRX_GTX_P5	1	0.22u 0402 187K	REG_CRX_C_GTX_P5
REG_CRX_GTX_P6	1	0.22u 0402 187K	REG_CRX_C_GTX_P6
REG_CRX_GTX_P7	1	0.22u 0402 187K	REG_CRX_C_GTX_P7
REG_CRX_GTX_P8	1	0.22u 0402 187K	REG_CRX_C_GTX_P8
REG_CRX_GTX_P9	1	0.22u 0402 187K	REG_CRX_C_GTX_P9
REG_CRX_GTX_P10	1	0.22u 0402 187K	REG_CRX_C_GTX_P10
REG_CRX_GTX_P11	1	0.22u 0402 187K	REG_CRX_C_GTX_P11
REG_CRX_GTX_P12	1	0.22u 0402 187K	REG_CRX_C_GTX_P12
REG_CRX_GTX_P13	1	0.22u 0402 187K	REG_CRX_C_GTX_P13
REG_CRX_GTX_P14	1	0.22u 0402 187K	REG_CRX_C_GTX_P14
REG_CRX_GTX_P15	1	0.22u 0402 187K	REG_CRX_C_GTX_P15

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FUNCTION TABLE	A Input	OE Enable	Y Output
1	L	L	L
2	L	H	2

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File DGFF CONN.

Size Document Number LA-F601P

Date Friday, March 08, 2018

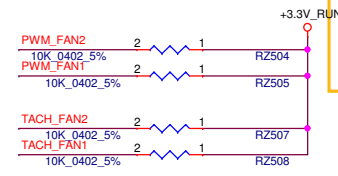
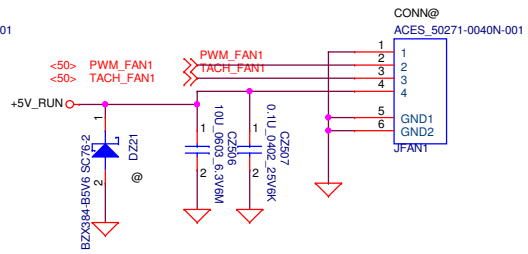
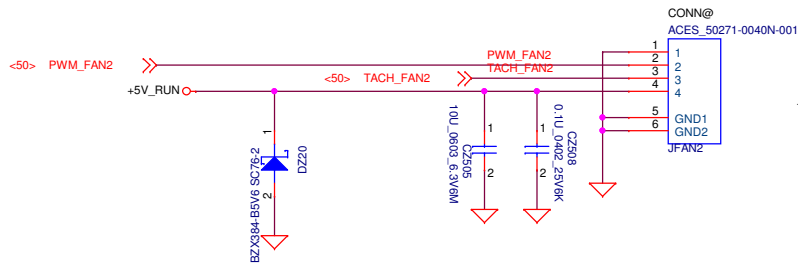
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Rev 1.0

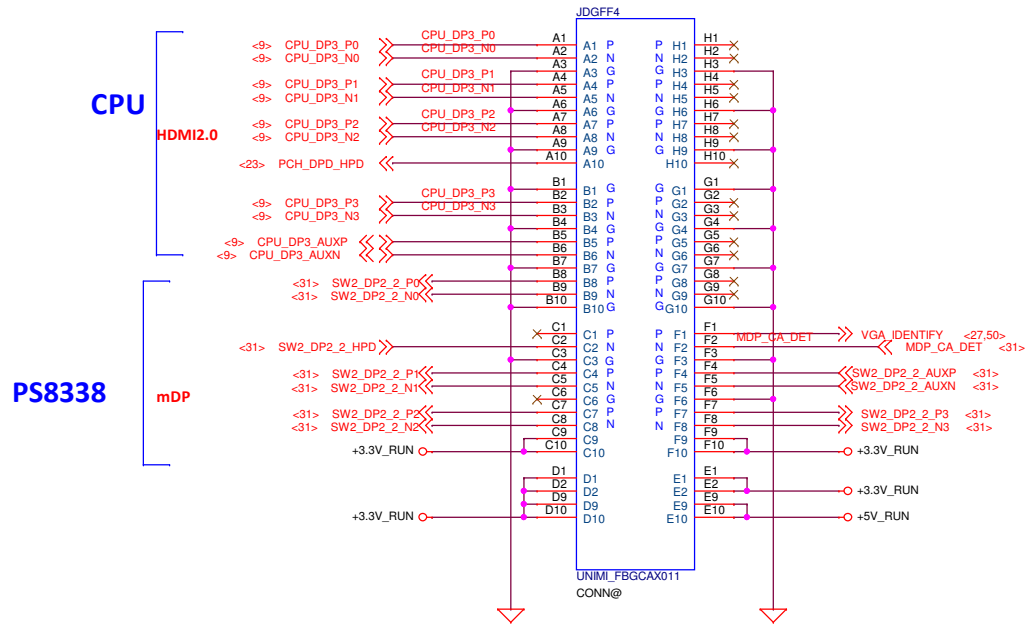


DGFF FAN

CPU FAN



UMA DGFF CON.

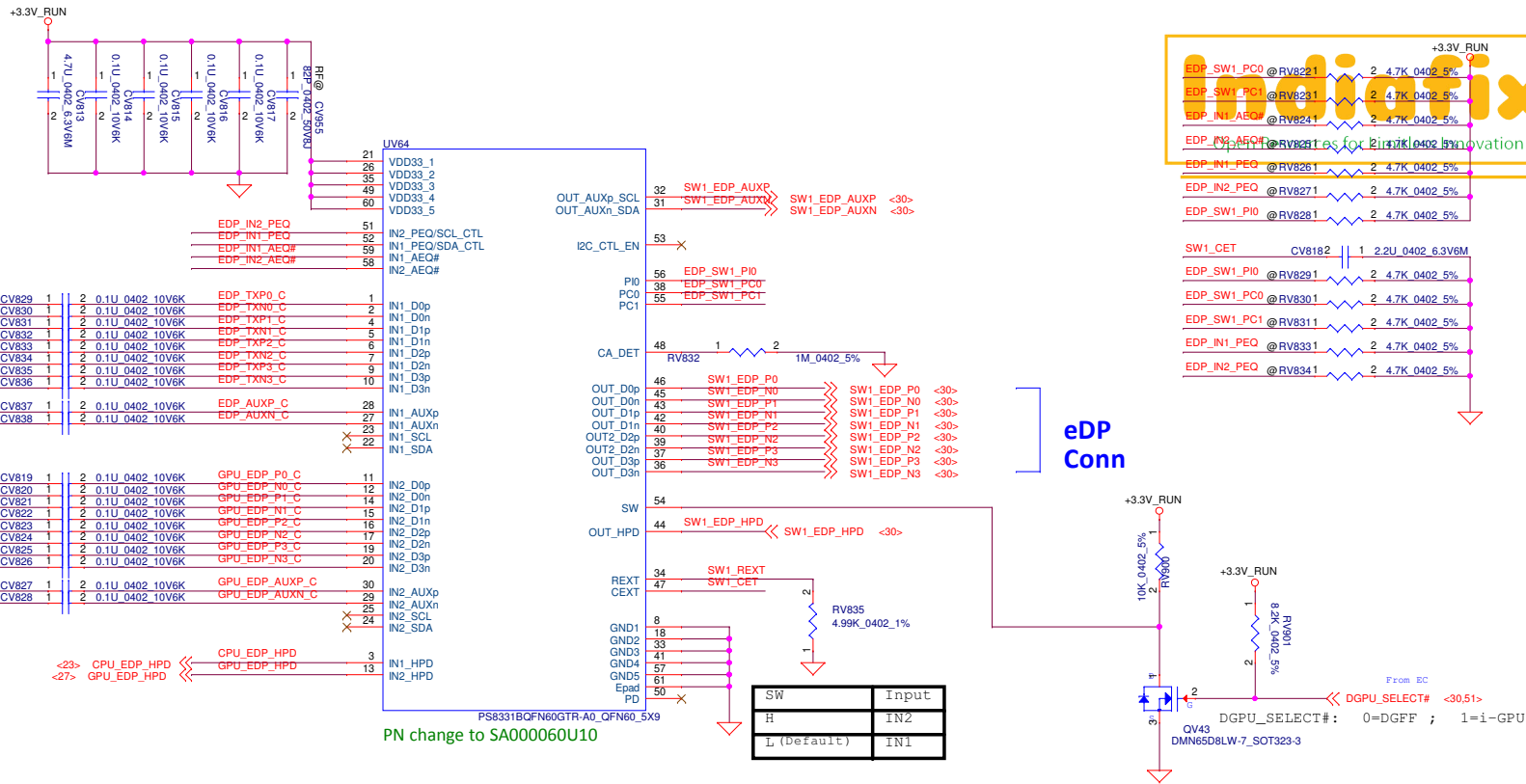


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FAN control		
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INy_PEQ = Programmable input equalization levels
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

PI0 = Auto test enable
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
 L: default
 H: +20%
 M: -16.7%

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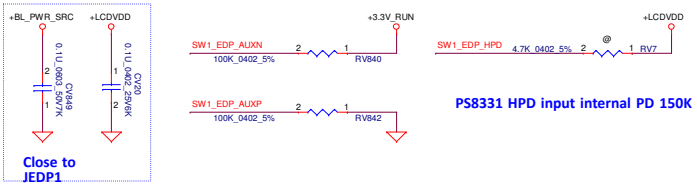
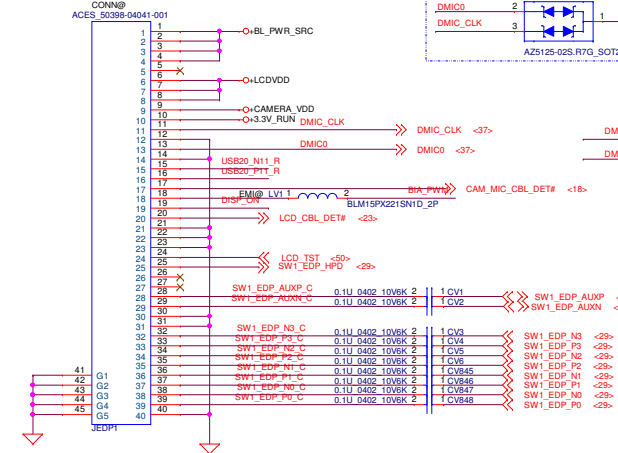
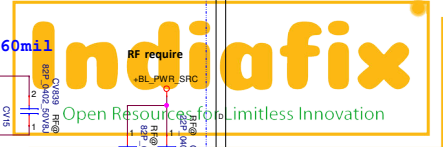
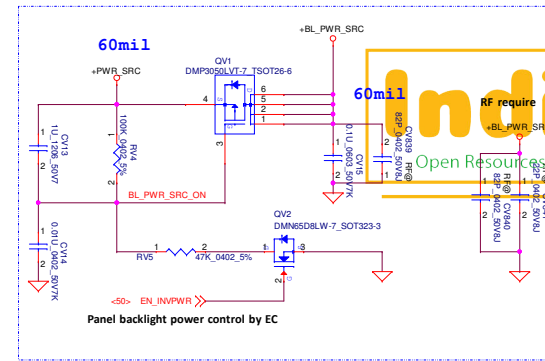
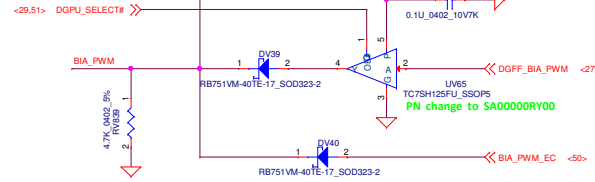
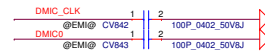
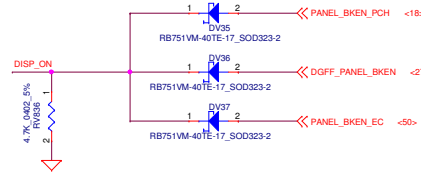
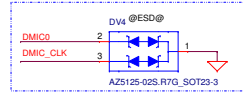
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Size: Document Number **LA-F601P** Rev 1.0

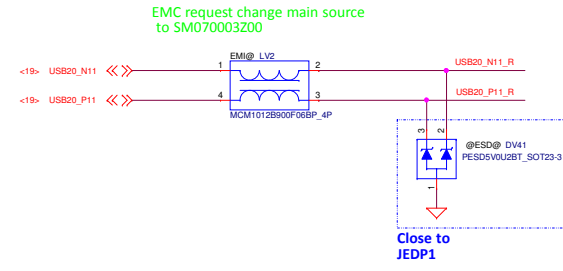
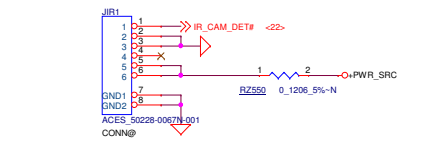
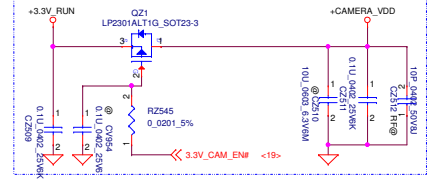
Date: Friday, March 09, 2018 Sheet 29 of 72

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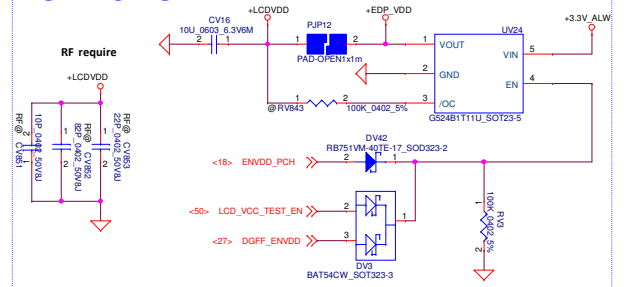
Close to JEDP1



Webcam PWR CTRL



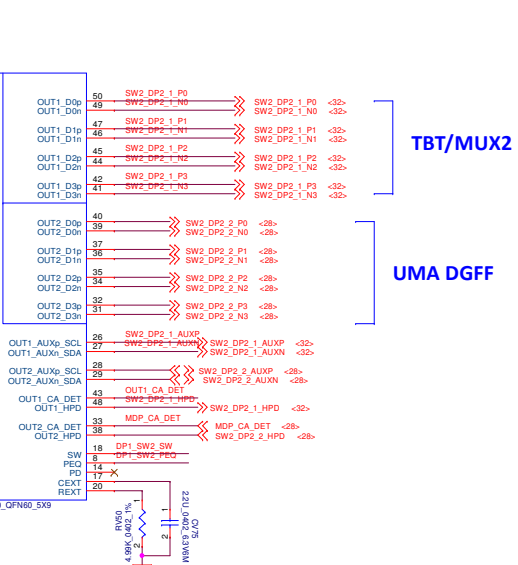
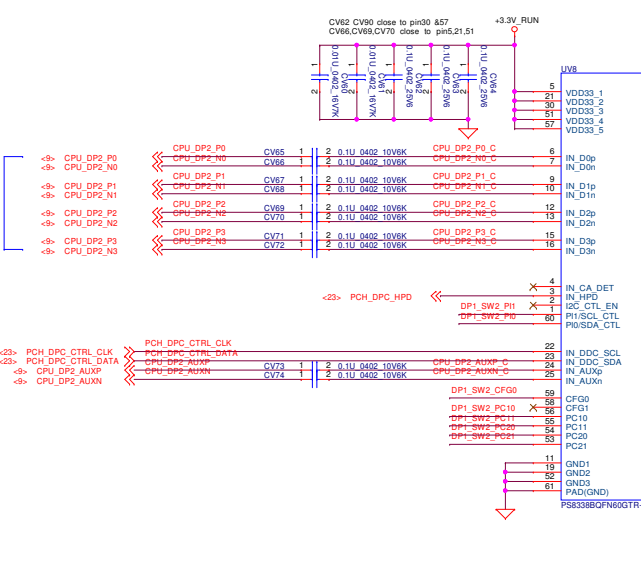
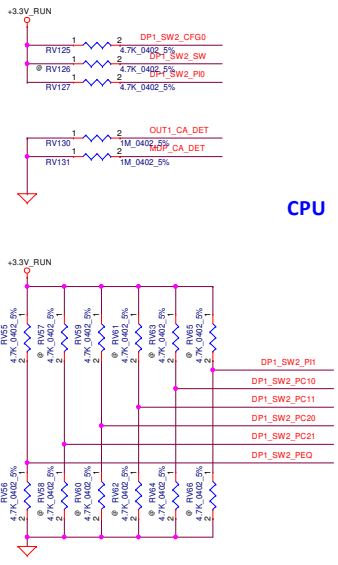
LCD Power



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CPU

TBT/MUX2

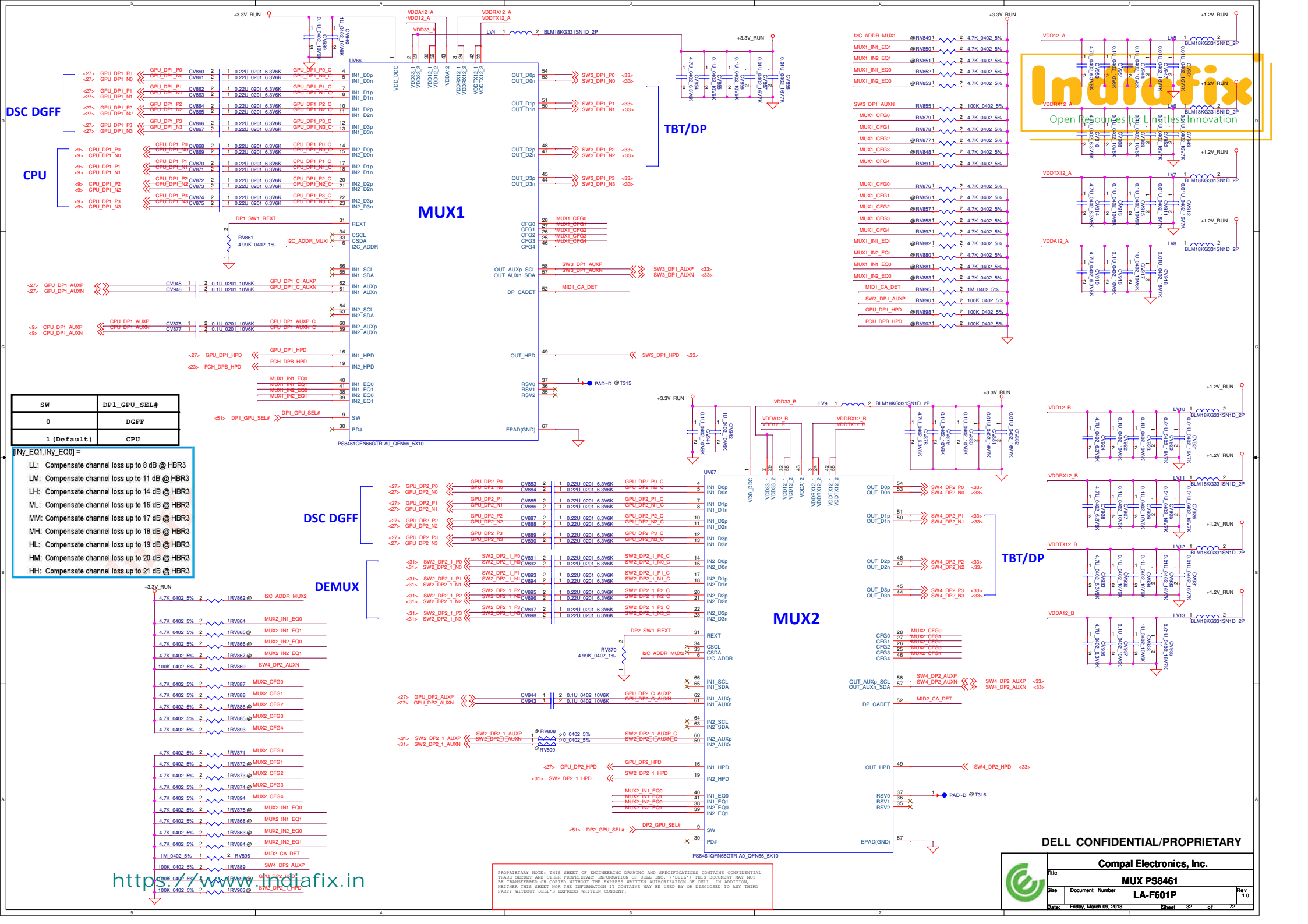
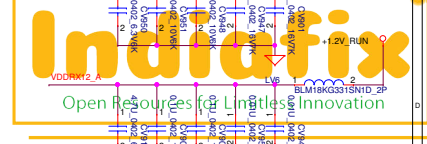
UMA DGFF

Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
 For Control Switching Mode (CFG0 = L):
 SW = L: Port1 is selected (default)
 SW = H: Port2 is selected

	H	L
CFG0	V	V
SW	V	V

For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
 SW = L: Port1 has higher priority when both ports are plugged (default)
 SW = H: Port2 has higher priority when both ports are plugged

Programmable input equalization levels. Internal pull down at ~150KΩ, 3.3V I/O
 PEQ =
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2
Overwritten by I2C register in I2C Control Mode



DSC DGFF

CPU

SW	DP1_GPU_SEL#
0	DGFF
1 (Default)	CPU

- [Ny_E01, Ny_E00] =
- LL: Compensate channel loss up to 8 dB @ HBR3
 - LM: Compensate channel loss up to 11 dB @ HBR3
 - LH: Compensate channel loss up to 14 dB @ HBR3
 - ML: Compensate channel loss up to 16 dB @ HBR3
 - MM: Compensate channel loss up to 17 dB @ HBR3
 - MH: Compensate channel loss up to 18 dB @ HBR3
 - HL: Compensate channel loss up to 19 dB @ HBR3
 - HM: Compensate channel loss up to 20 dB @ HBR3
 - HH: Compensate channel loss up to 21 dB @ HBR3

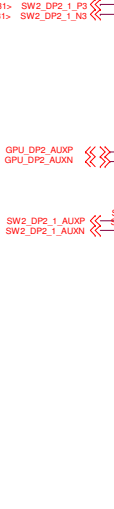
+3.3V_RUN



MUX1

DSC DGFF

DEMUX



TBT/DP

MUX2

TBT/DP

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File: MUX PS8461

Size: Document Number LA-F601P

Date: Friday, March 09, 2018

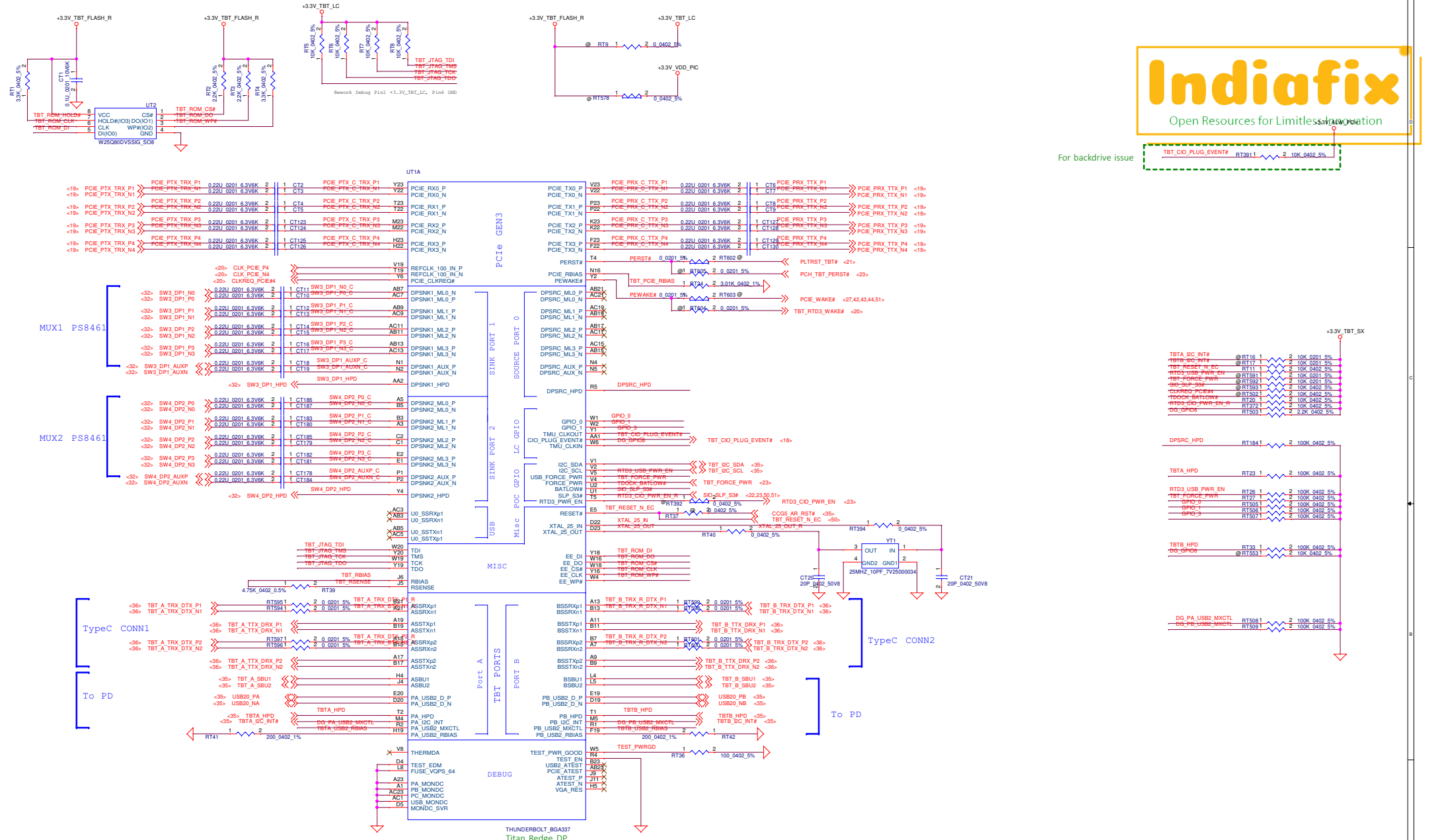
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For backdrive issue

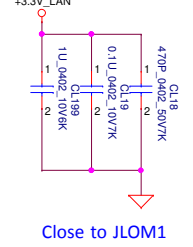
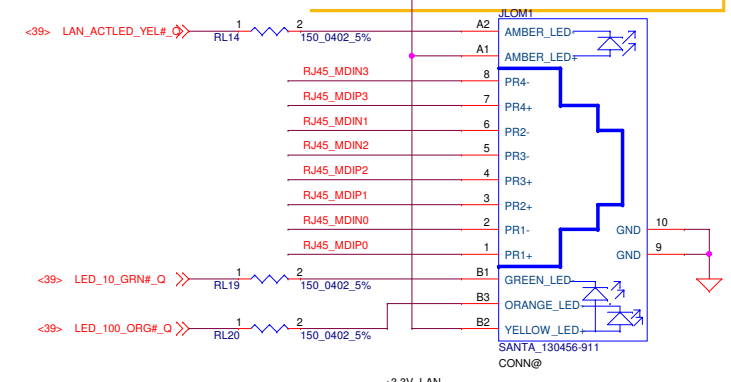
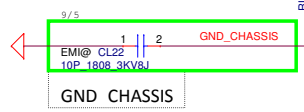
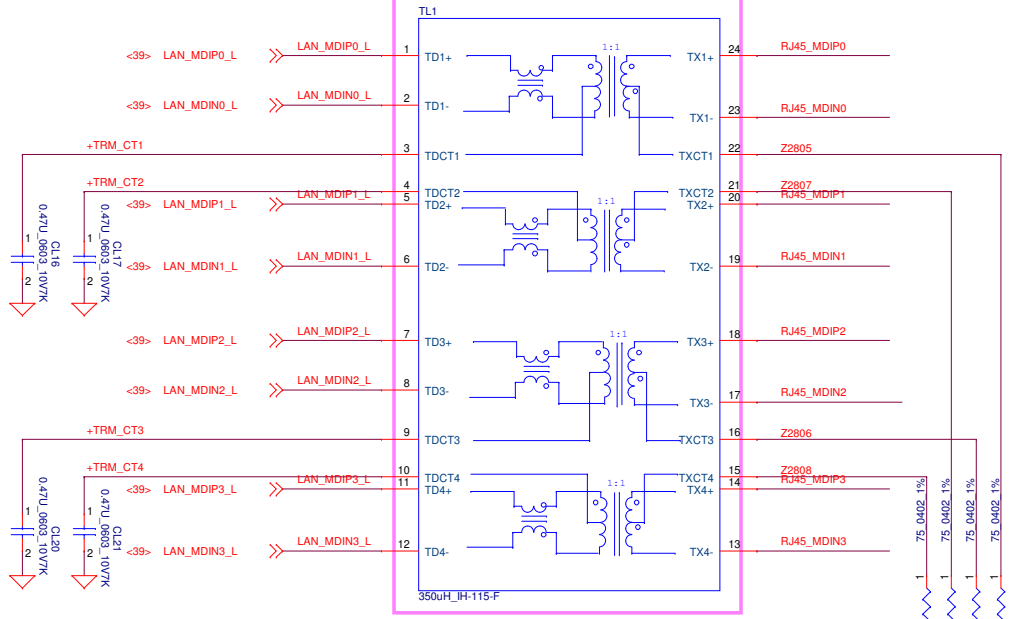


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DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc. TBT-TR(1/2) DP, PCIe			
Doc No	LA-F601P	Rev	1.0
Date	Wednesday, March 14, 2018	Sheet	33 of 72

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DVT1 change from SP050006P00 to SP050006Y00



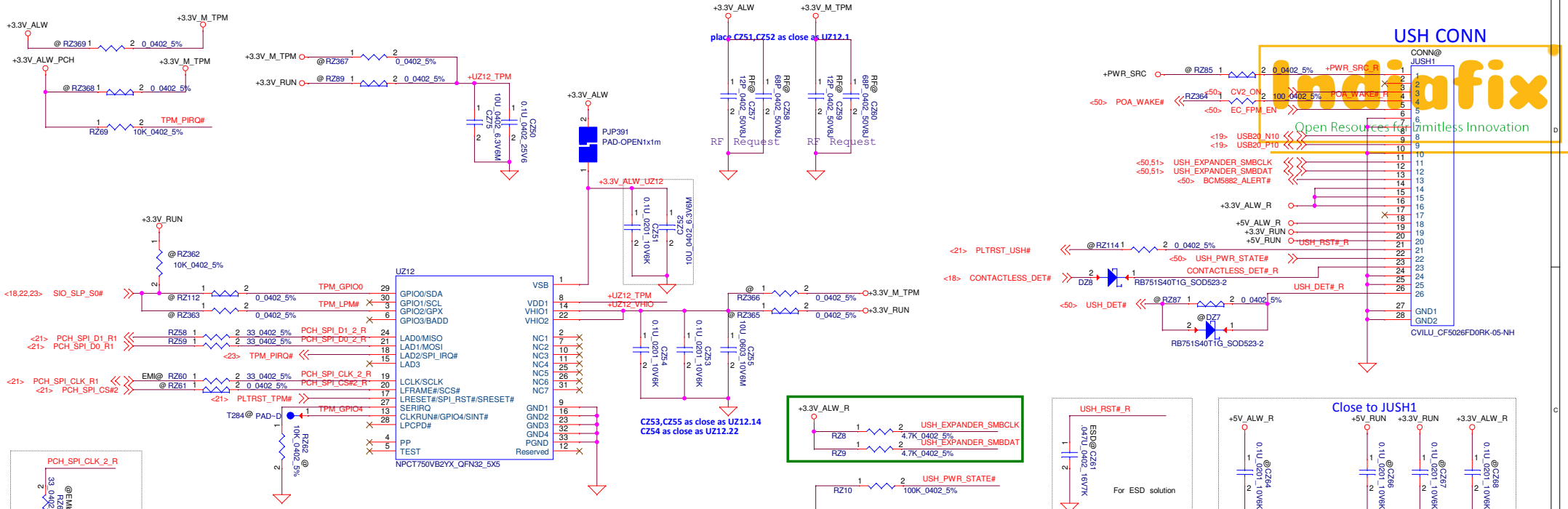
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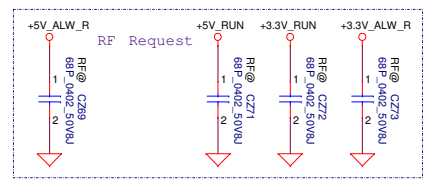
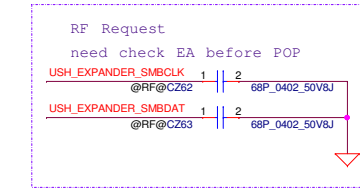
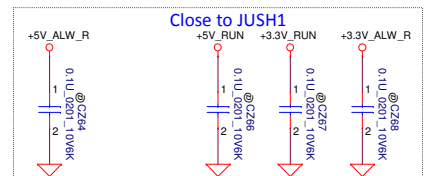
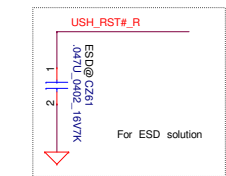
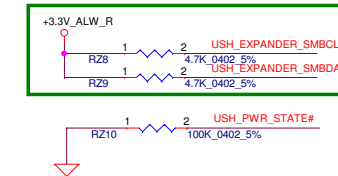
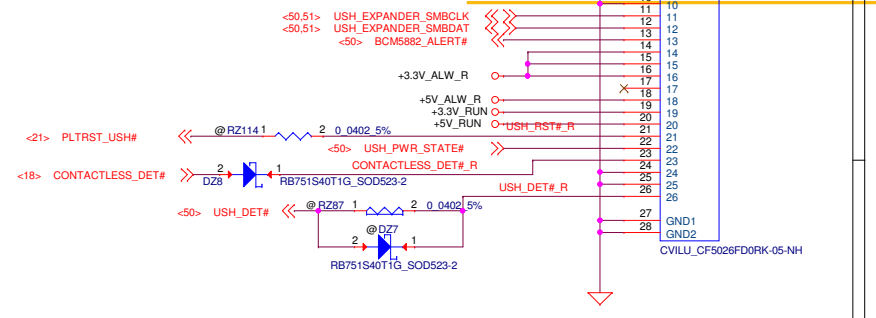
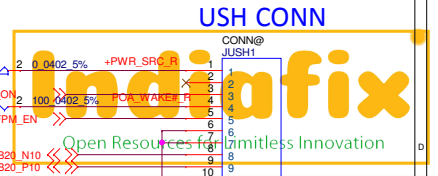


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Size	Document Number	LA-F601P	
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		Rev	1.0

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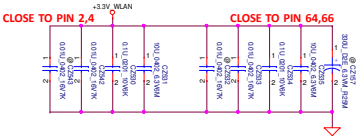
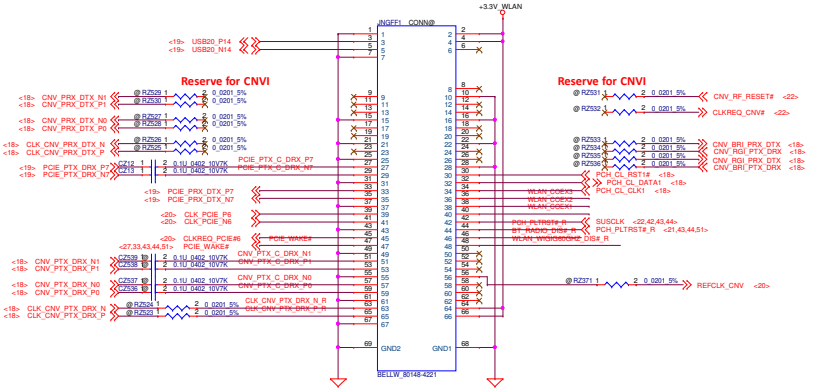


	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62	RZ365, RZ367	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365	RZ367, RZ366, RZ62	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V_SPI power

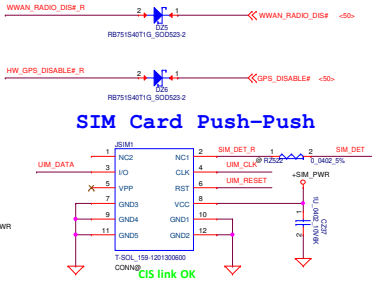
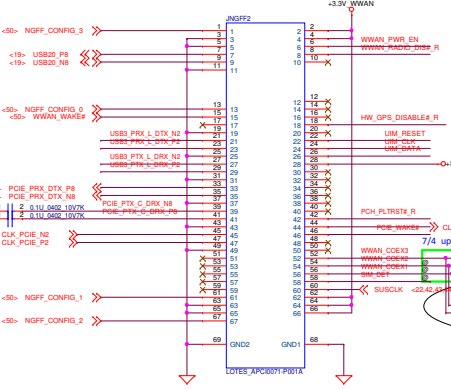
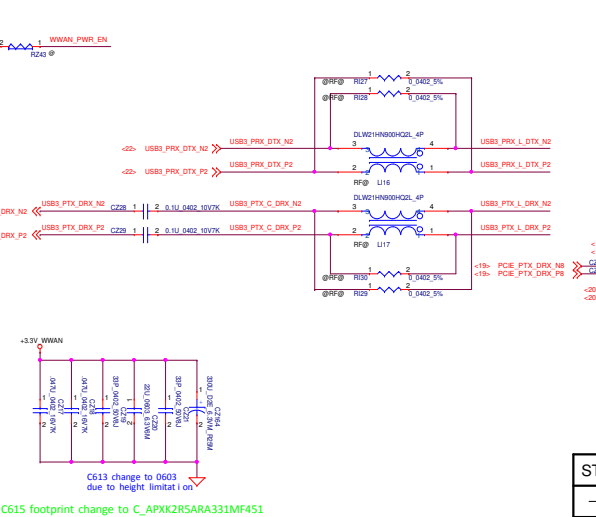


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WLAN/BT NGFF slot_1 Key A



WWAN/LTE NGFF slot_2 Key B



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCI-E
15	1	1	1	1	Cache

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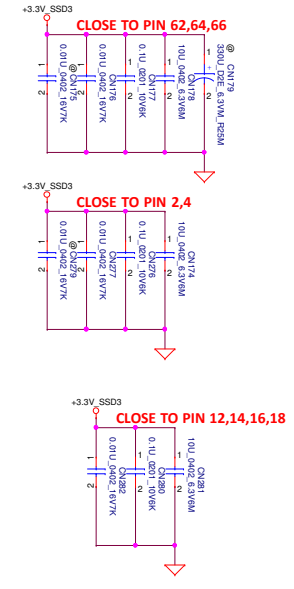
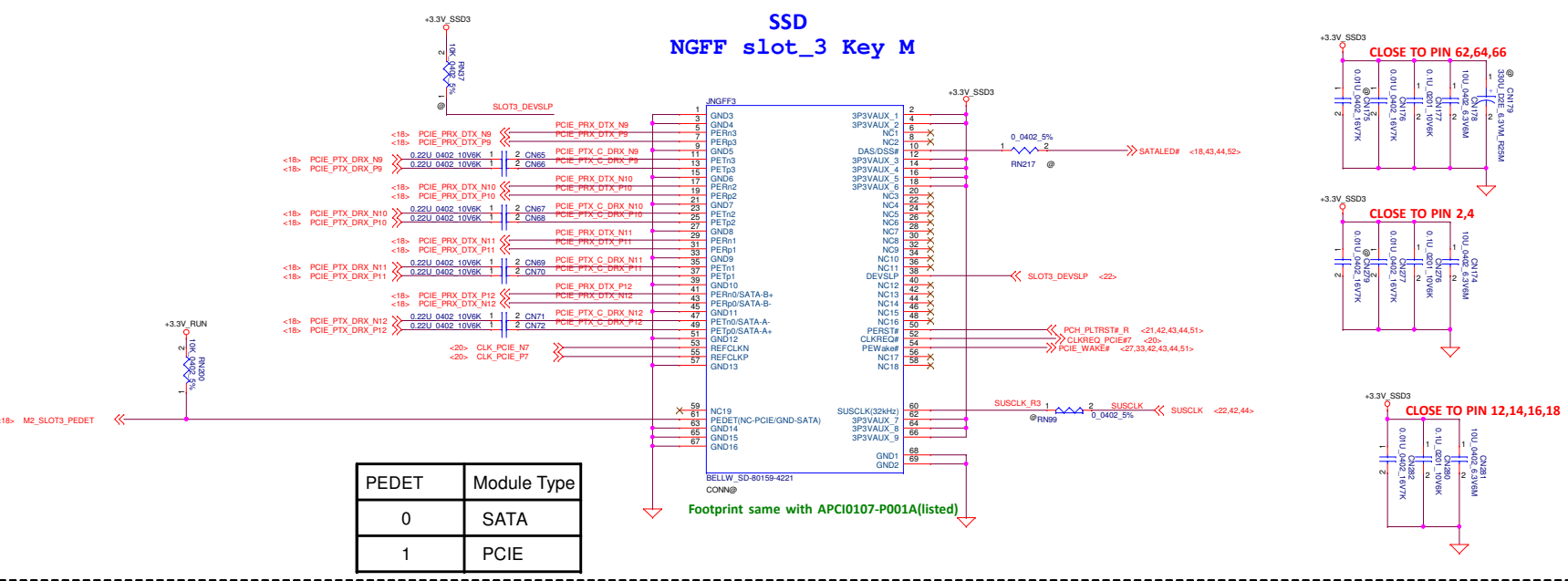
M.2 Card-1/2

LA-F601P

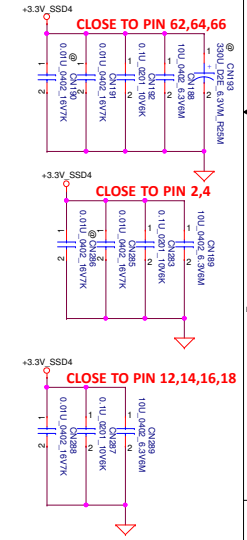
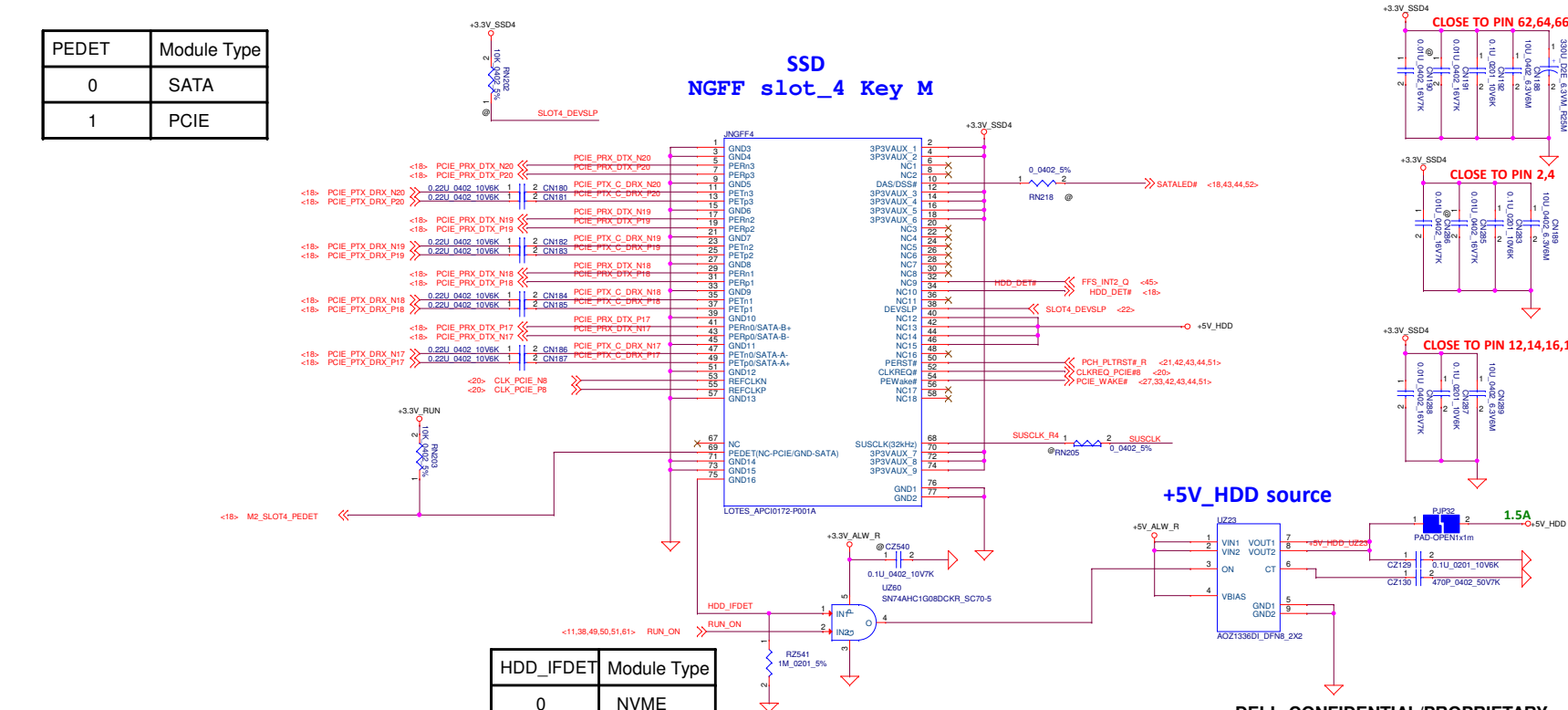
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PEDET	Module Type
0	SATA
1	PCIE

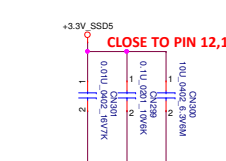
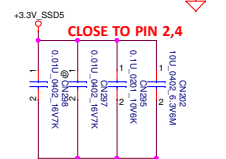
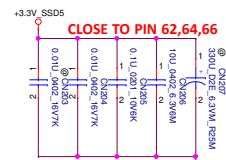
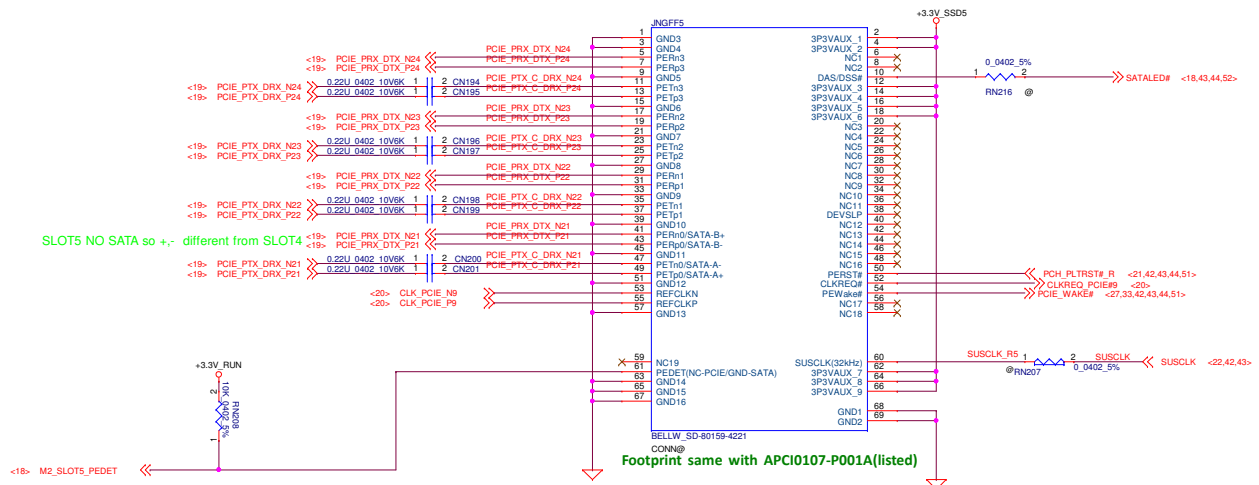


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M.2 Card-2/2		
Size	Document Number	Rev
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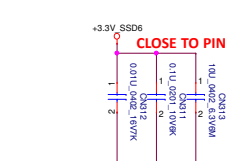
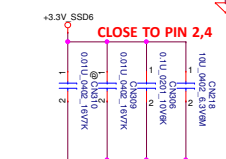
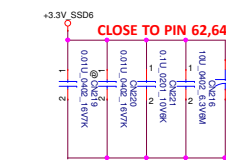
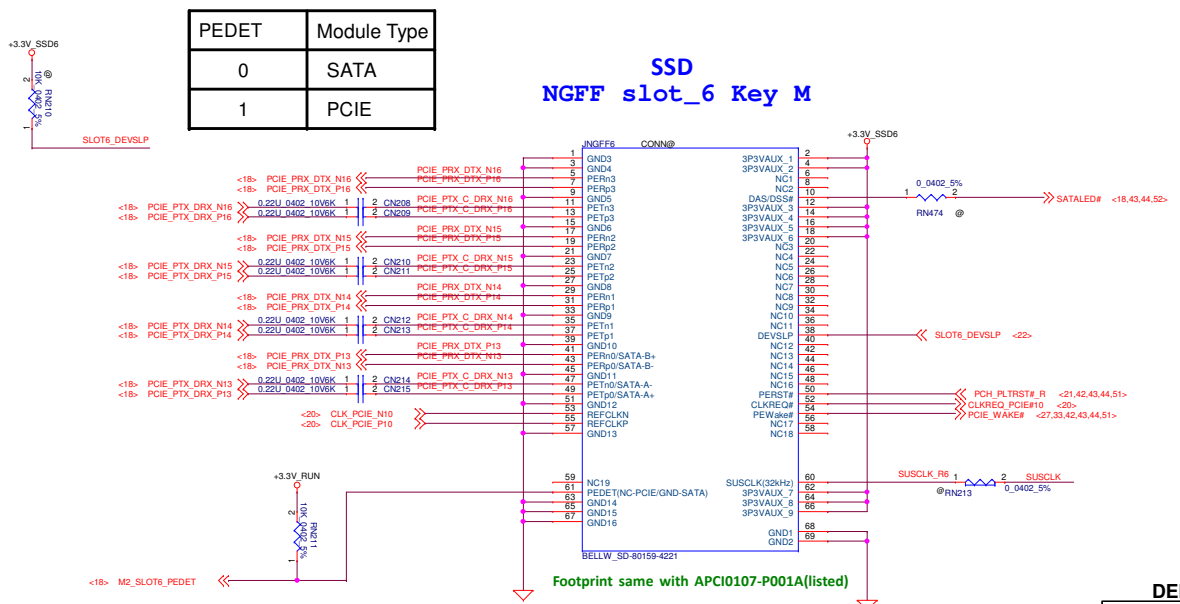
SSD NGFF slot_5 Key M



SLOTS NO SATA so +/- different from SLOT4

PEDET	Module Type
0	SATA
1	PCIe

SSD NGFF slot_6 Key M



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M.2 Card-2/2

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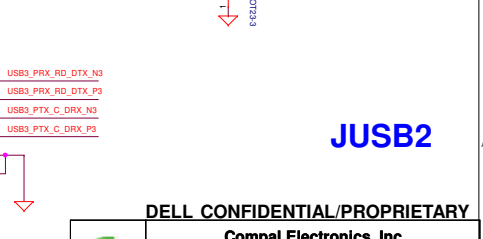
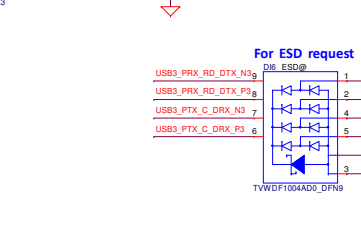
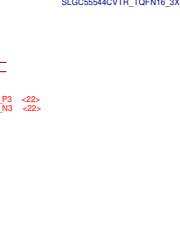
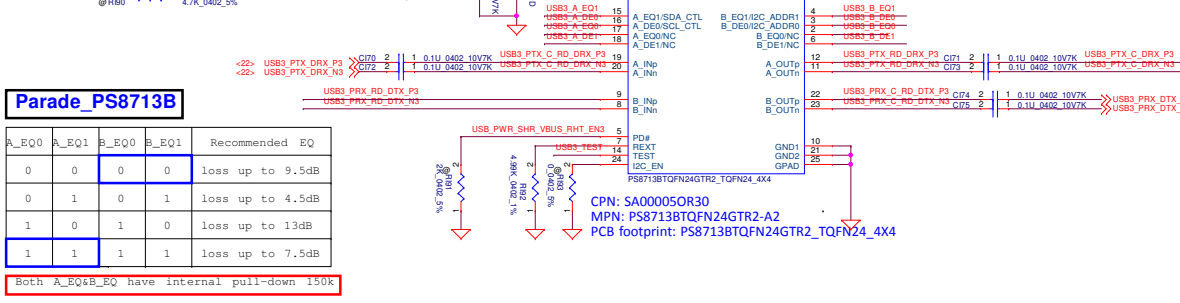
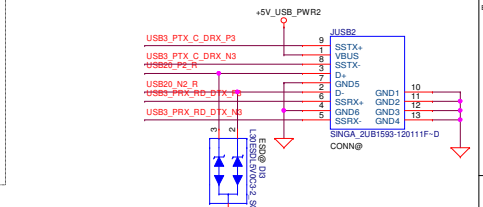
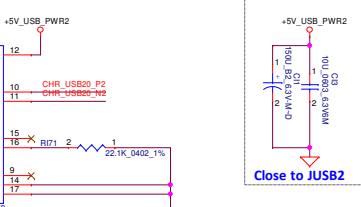
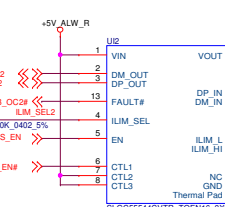
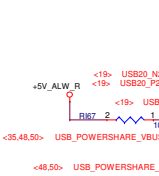
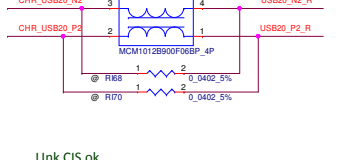
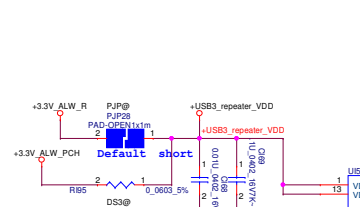
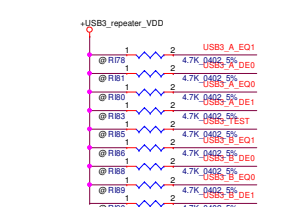
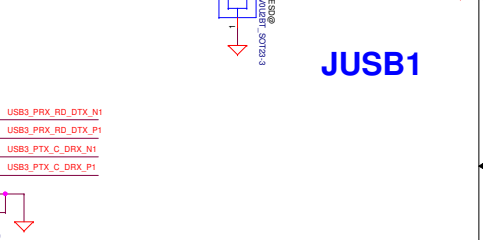
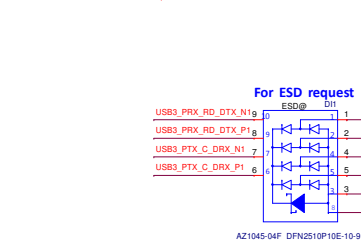
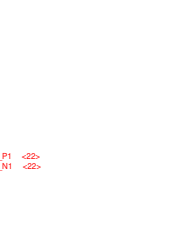
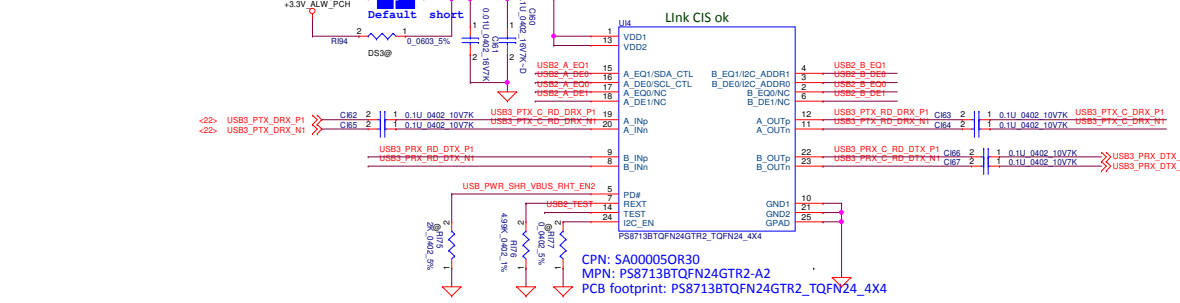
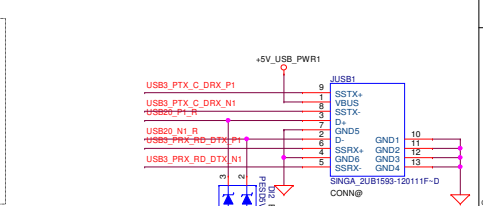
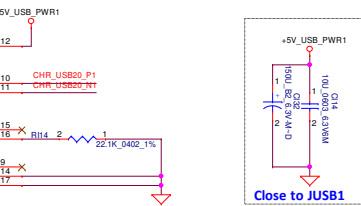
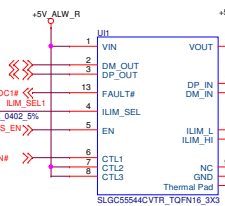
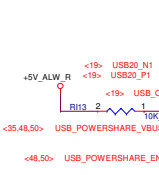
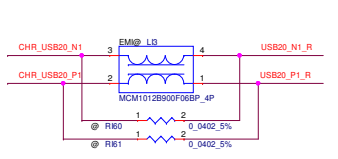
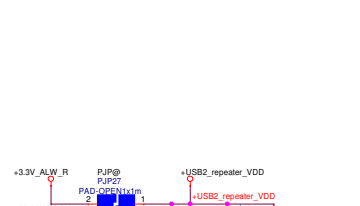
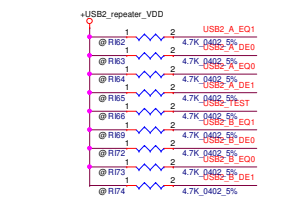
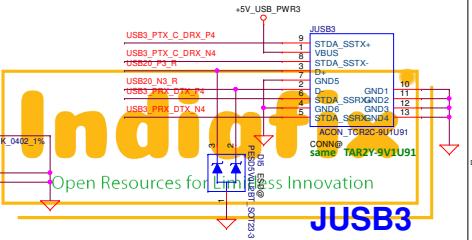
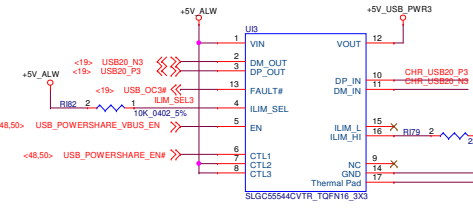
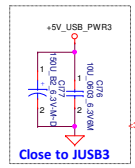
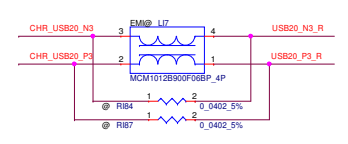
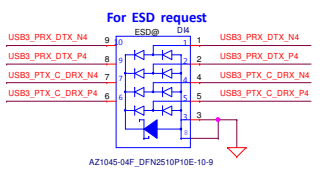
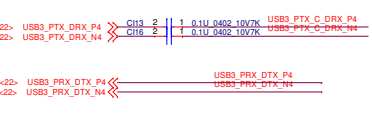
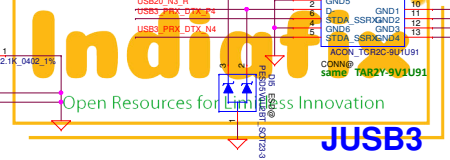
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HDD PCIE/SATA repeater			
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DEL PS8559

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HDD PCIE/SATA repeater			
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Parade_PS8713B

A_EQ0	A_EQ1	B_EQ0	B_EQ1	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 4.5dB
1	0	1	0	loss up to 13dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150K

CPN: SA00005OR30
 MPN: PS8713BTQFN24GTR2-A2
 PCB footprint: PS8713BTQFN24GTR2_TQFN24_4X4

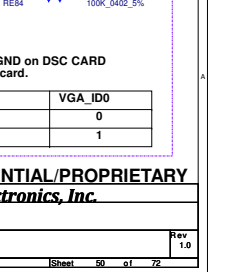
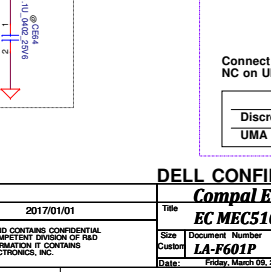
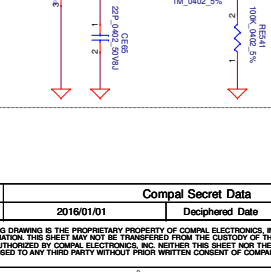
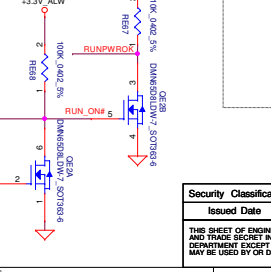
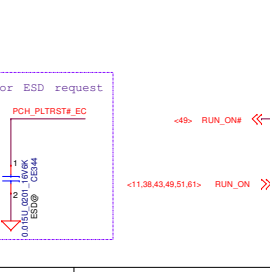
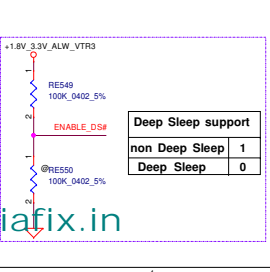
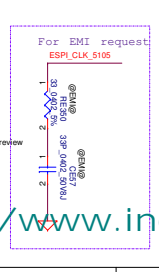
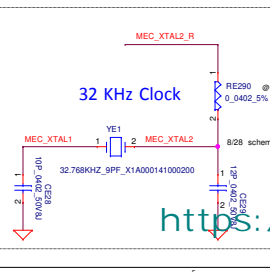
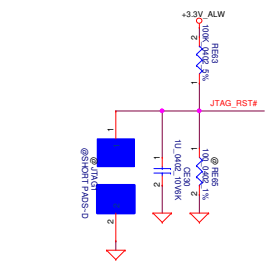
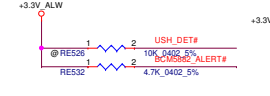
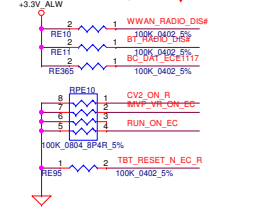
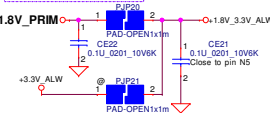
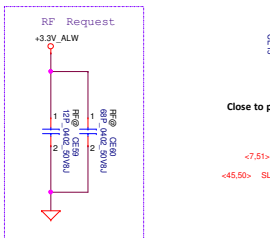
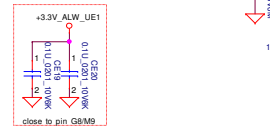
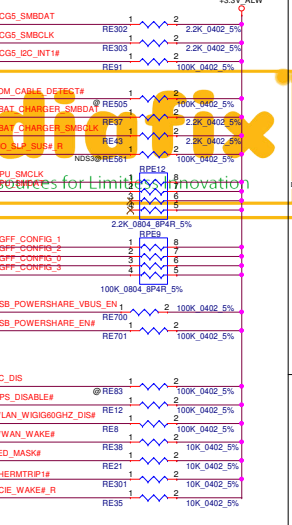
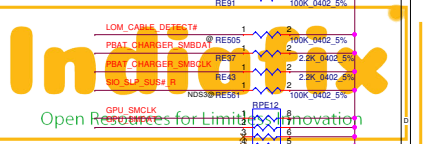
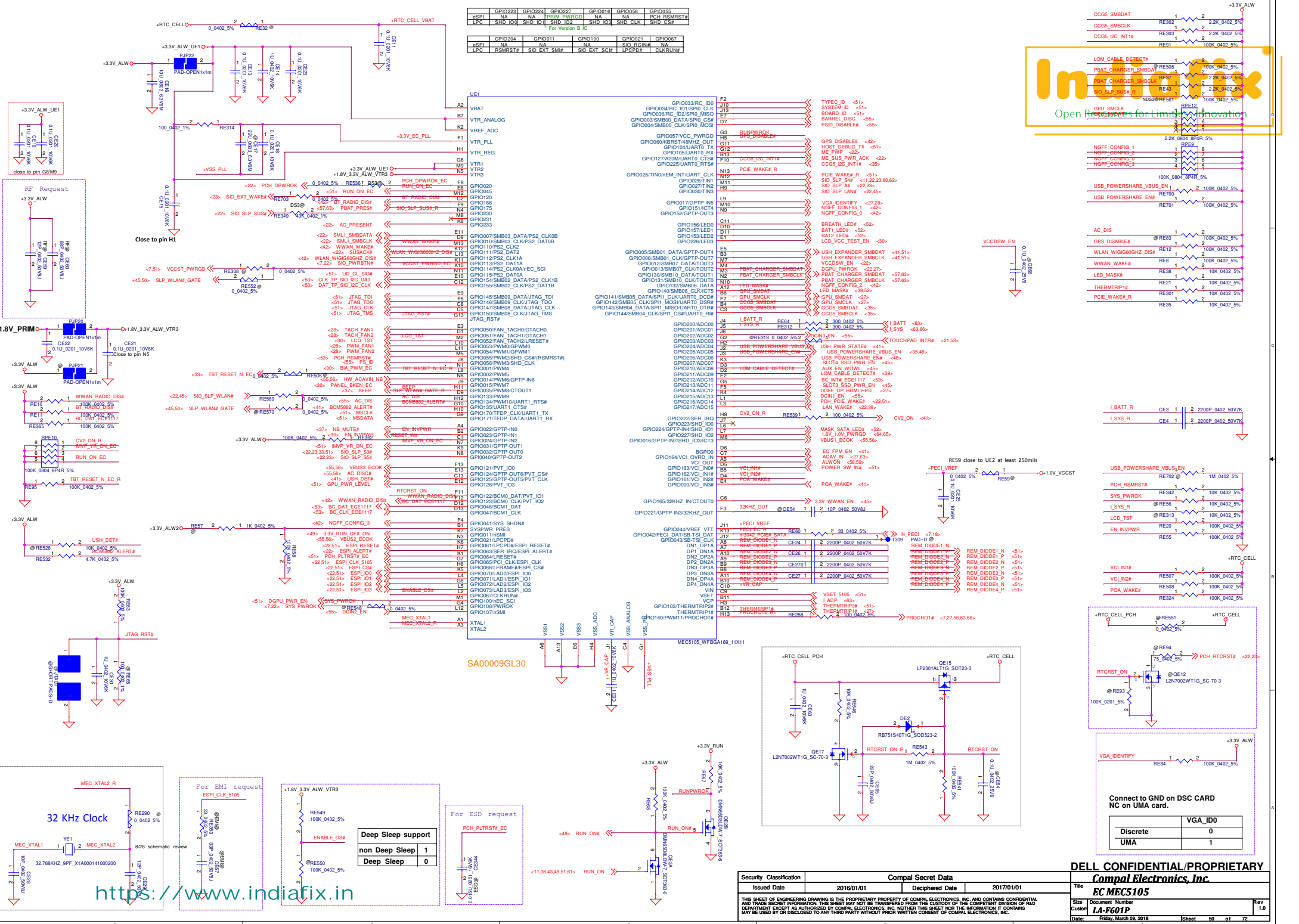
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File: **USB3.0**

Doc Number: **LA-F601P**

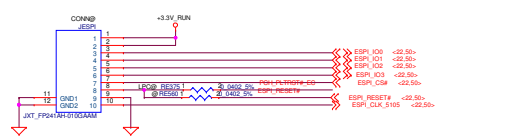
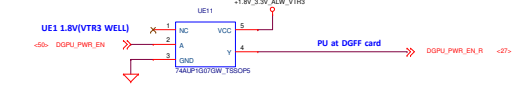
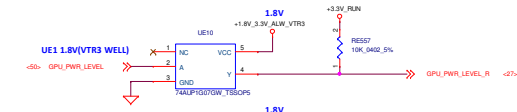
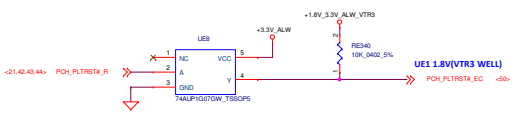
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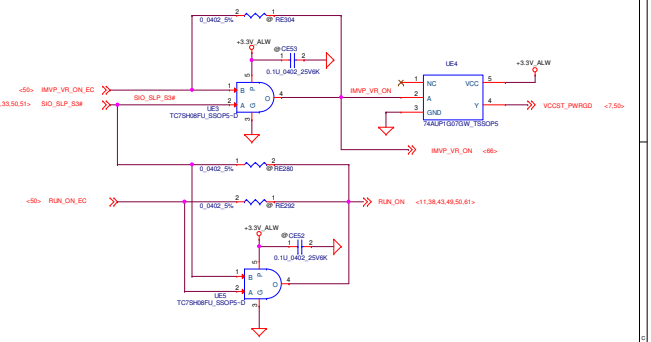
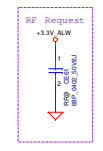
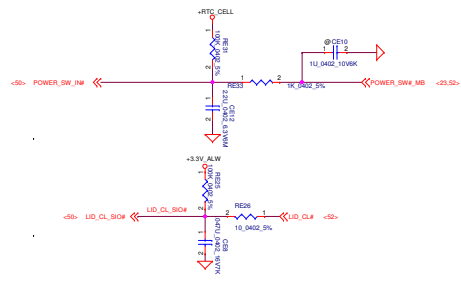
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Issued Date	Deciphered Date
2016/01/01	2017/01/01

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Compal Electronics, Inc.
MECS105
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 Document Number
 LA-F601P
 Rev 1.0
 Date: Friday, March 09, 2016
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LPC 80Port	Debug	LPC	ESPI
1		+3.3V_RUN	+3.3V_RUN
2		+3.3V_RUN	+3.3V_RUN
3		LPC_LAD0	ESPI_100
4		LPC_LAD1	ESPI_101
5		LPC_LAD2	ESPI_102
6		LPC_LAD3	ESPI_103
7		LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA	NA
9	GND	GND	GND
10	LPC_CLOCK	ESPI_CLK	ESPI_CLK



REV	CE62	RE93
4700p	240K	4700p
4700p	130K	4700p
4700p	62K	4700p
4700p	33K	4700p
4700p	8.2K	4700p
4700p	4.3K	4700p
4700p	2K	4700p
4700p	1K	4700p

REV	CE40	RE79
X00	240K	4700p
X01	130K	4700p
X02	62K	4700p
X03	33K	4700p
A00	8.2K	4700p
A00	4.3K	4700p
A00	2K	4700p
A00	1K	4700p

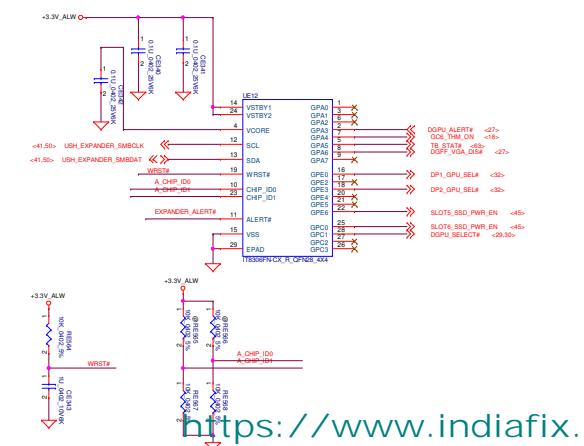
REV	C1465	R3754
***	240K	4700p
***	130K	4700p
***	6.2K	4700p
***	4.3K	4700p
***	2K	4700p
***	1K	4700p

TypeC_ID rise time is measured from 5%-68%

BOARD_ID rise time is measured from 5%-68%

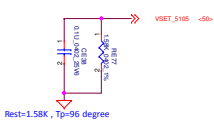
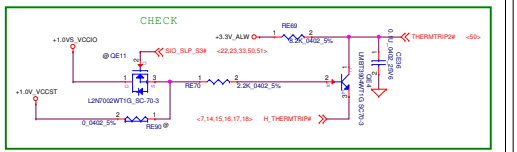
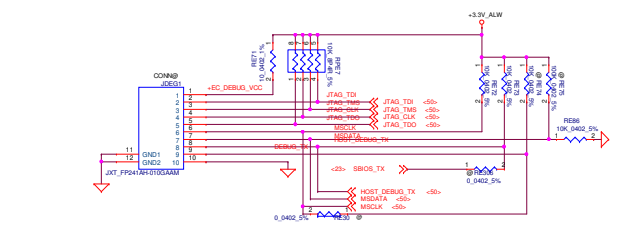
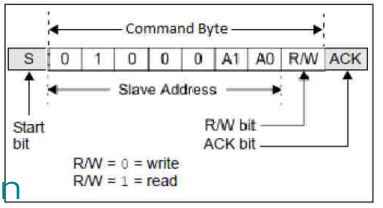
PANEL_ID rise time is measured from 5%-68%

SIO IT8306

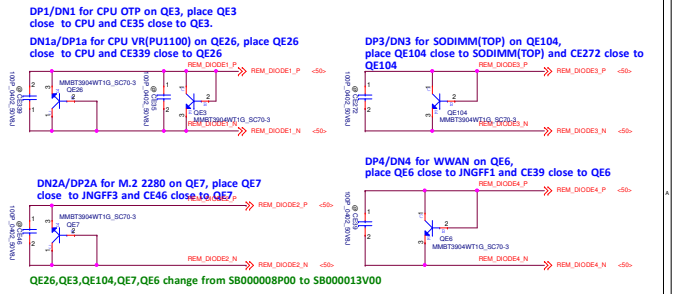


For I2C SAD+Read/Write patterns
 Command SAD[7:3], ID[1], ID[0], R/W= SAD+R/W

Command	SAD[7:3]	ID[1]	ID[0]	R/W	Pattern
Read	01000	0	0	0	01000001 (41h)
Write	01000	0	0	1	01000000 (40h)
Read	01000	0	1	0	01000011 (43h)
Write	01000	0	1	1	01000010 (42h)
Read	01000	1	0	0	01000101 (45h)
Write	01000	1	0	1	01000100 (44h)
Read	01000	1	1	0	01000111 (47h)
Write	01000	1	1	1	01000110 (46h)



Channel	Location
DP1/DN1	CPU QTP
DP1A/DN1A	CPU VR
DP2A/DN2A	M.2 2280
DP3/DN3	DIMM(TOP)
DP4/DN4	WWAN



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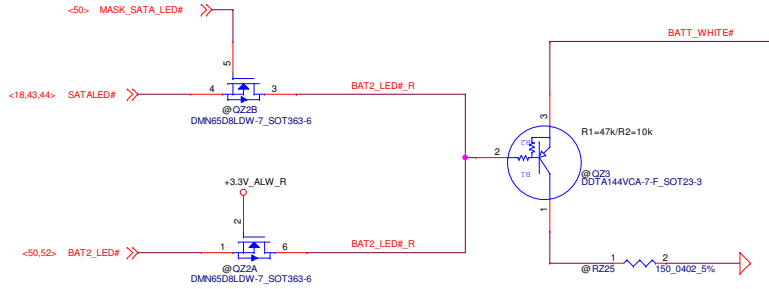
Security Classification	Compal Secret Data	Deciphered Date	Title
Issued Date	2016/01/01	2017/01/01	MEC5105 ELECTRONICS

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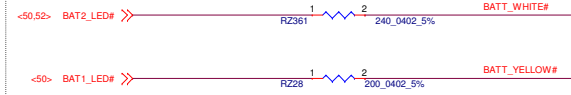
Rev	Document Number	Date
1.0	LA-F601P	2016/01/01

HDD LED MUX

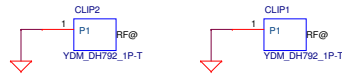
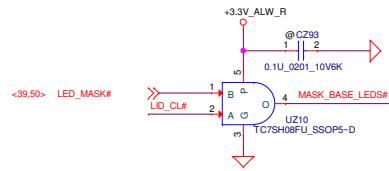
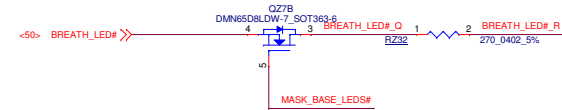
means EC can switch battery white led and HDD LED by hot key * Fn+H



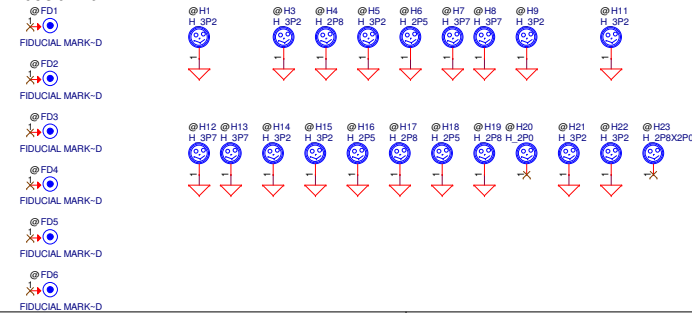
Battery LED



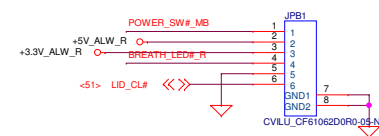
Breath LED



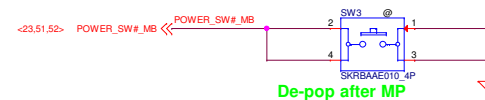
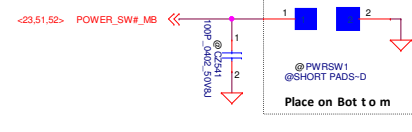
Fiducial Mark



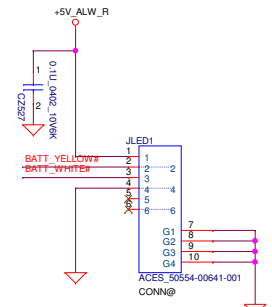
Power But t on CONN



Power Switch for debug



To LED/B Conn



Footprint same with CF2006FV0RK-NH

LED Circuit Control Table		
	LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

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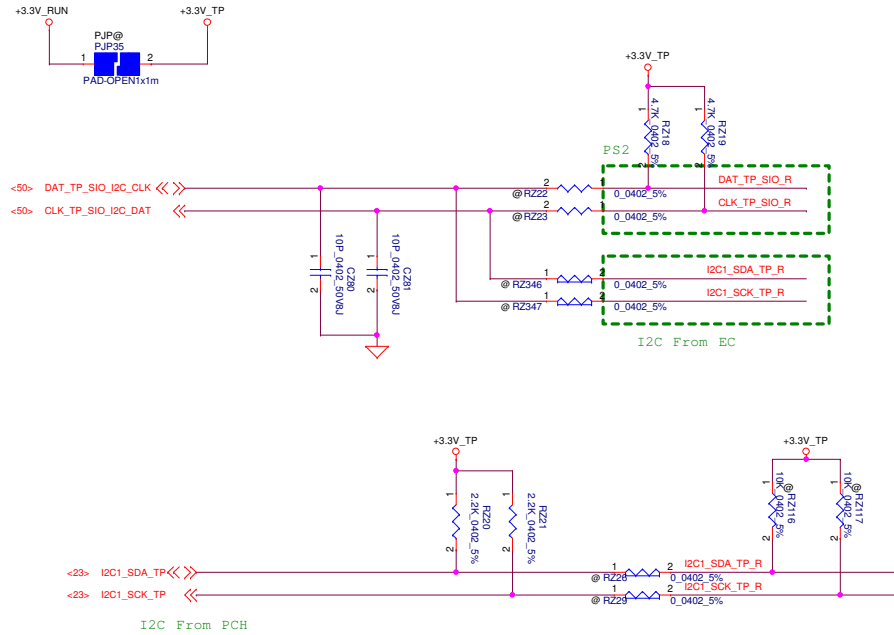
Compal Electronics, Inc.



Title	LED / Screw hole		Rev
Size	Document Number	LA-F601P	1.0
Date	Friday, March 16, 2018	Sheet 02 of 72	

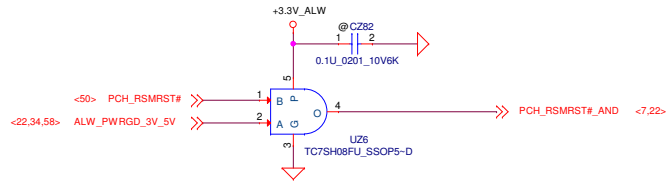
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Touch Pad

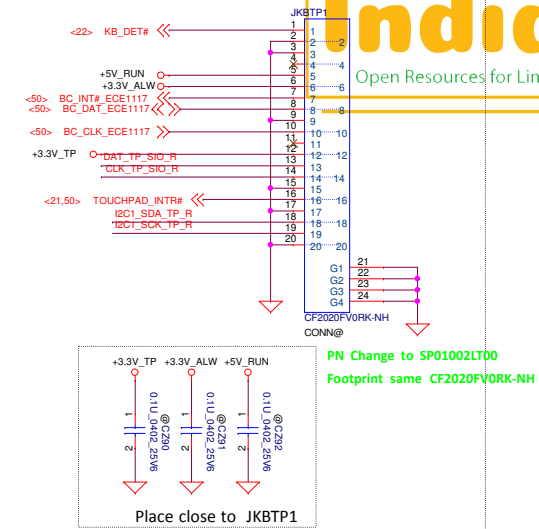


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize intel I2C drivers for Win7)
 For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
 Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

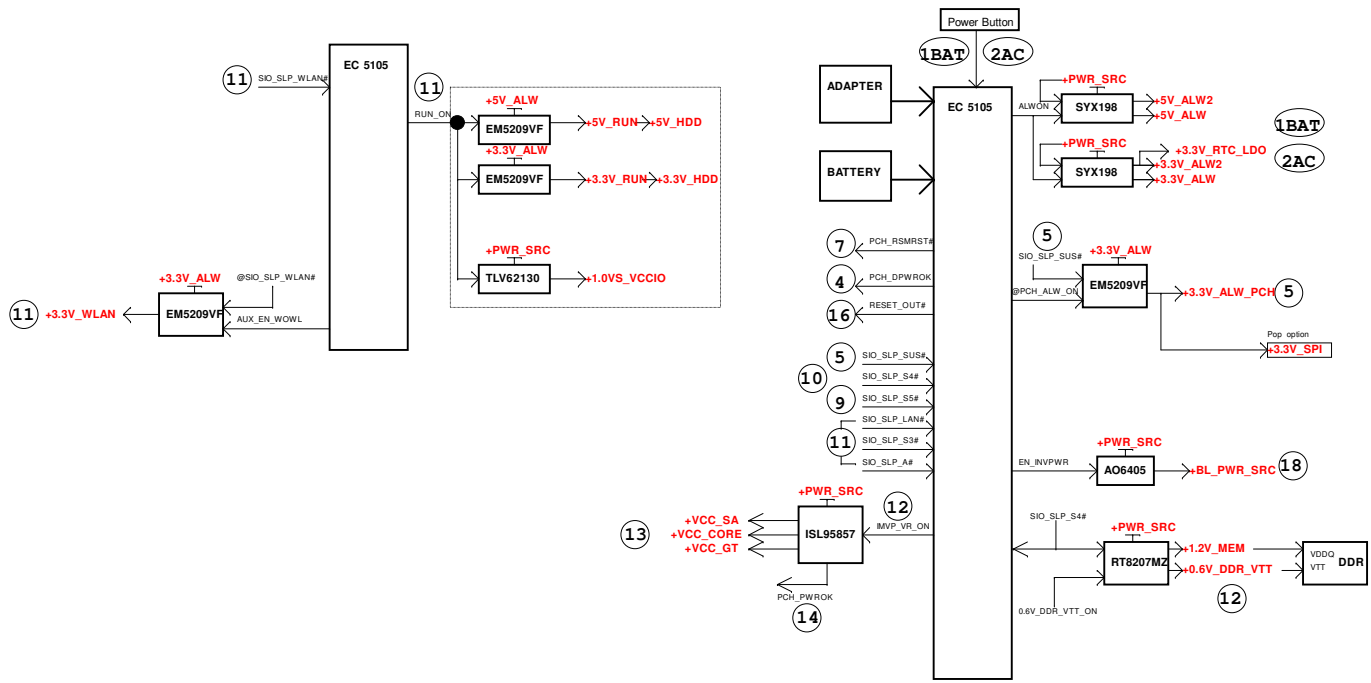
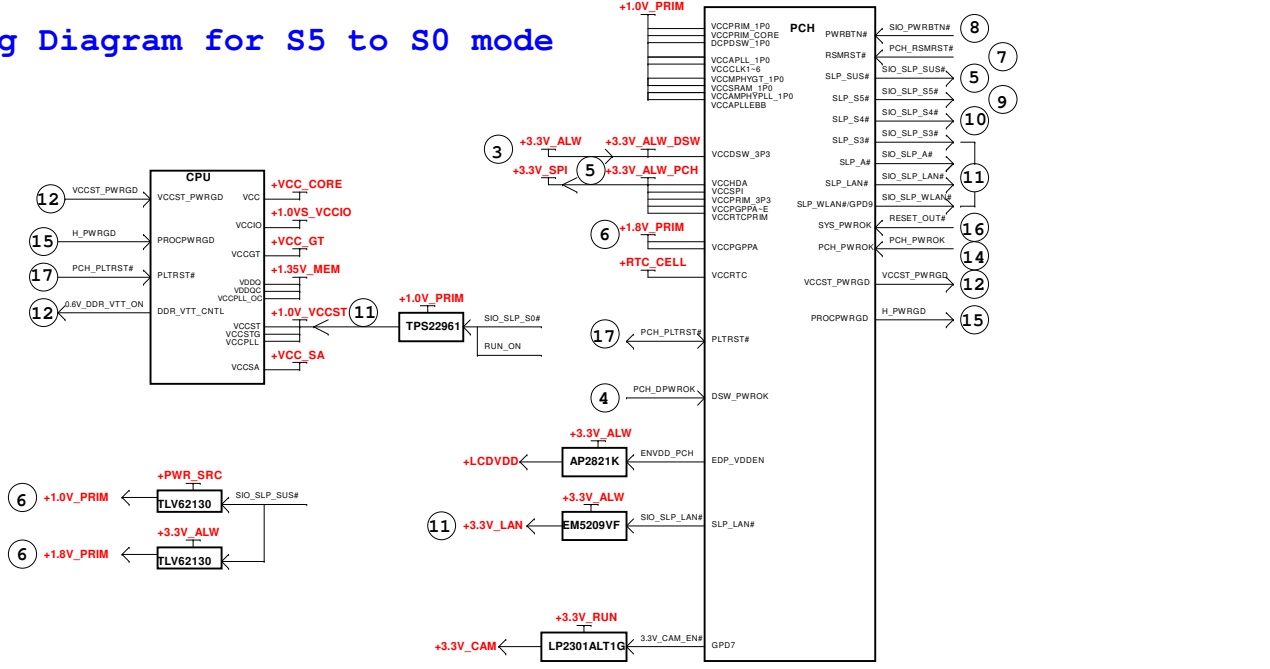
RSMRST circuit

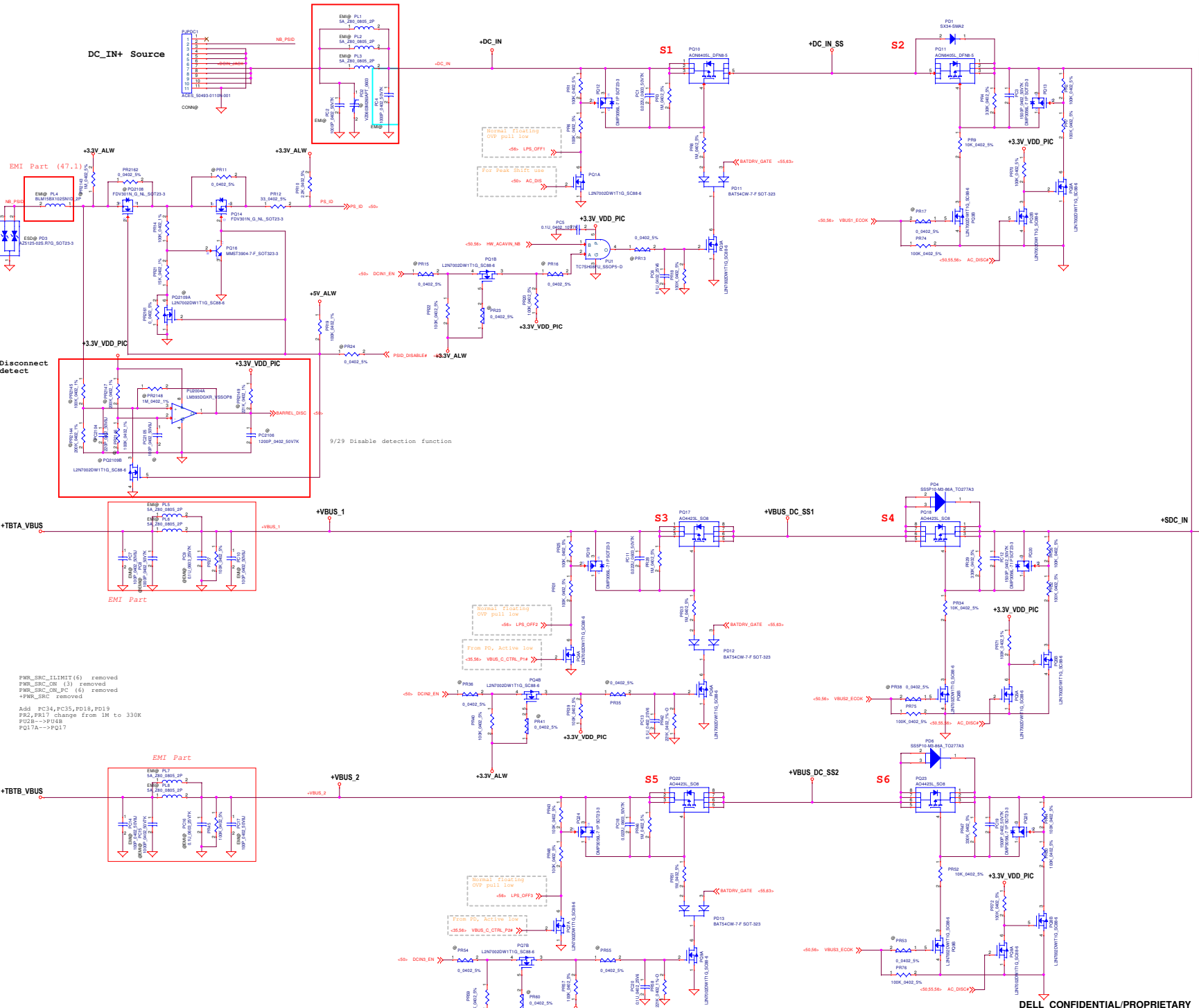


Keyboard



Timing Diagram for S5 to S0 mode





EMI Part (47.1)

Disconnect detect

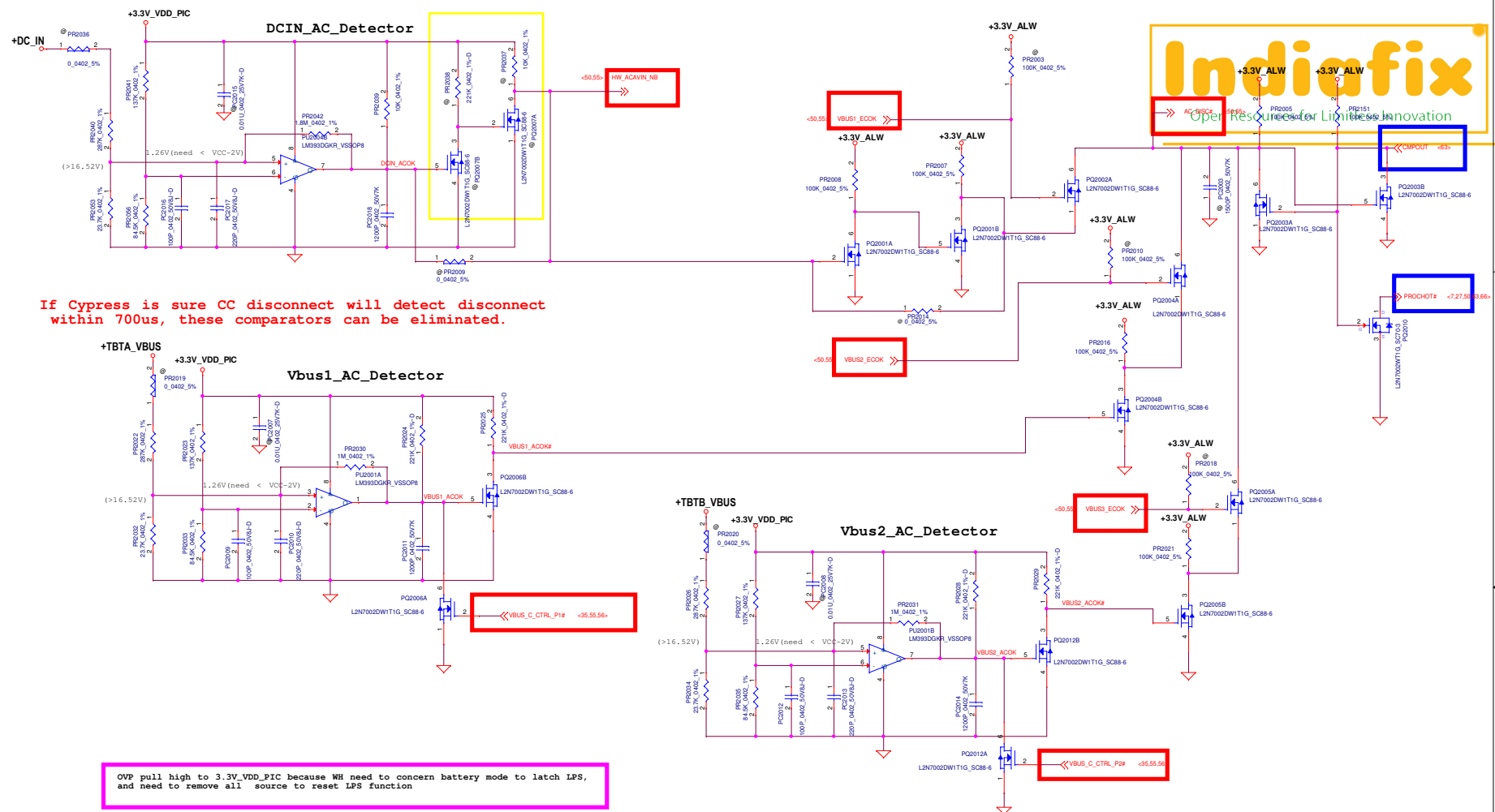
+TBTA_VBUS

+TBTB_VBUS

PWR_SRC_LIMIT (6) removed
 PWR_SRC_CN (3) removed
 PWR_SRC_CN_PIC (6) removed
 #PWR_SRC removed
 Add PC34, PC35, PD18, PD19
 PR2, PR17 change from 1M to 330K
 PR18 -> PR14B
 PQ17A -> PQ17

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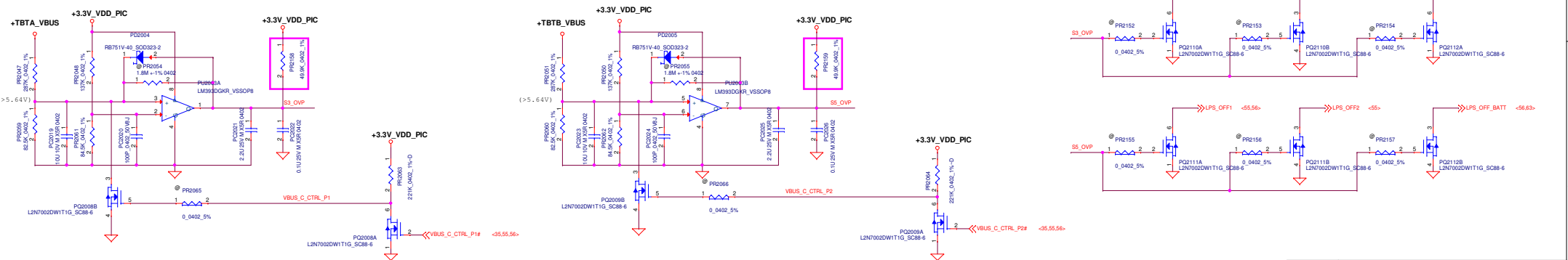


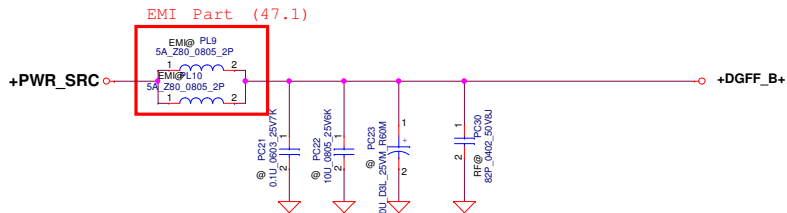
If Cypress is sure CC disconnect will detect disconnect within 700us, these comparators can be eliminated.

OVP pull high to 3.3V_VDD_PIC because WH need to concern battery mode to latch LPS, and need to remove all source to reset LPS function

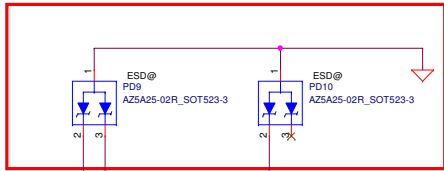
S3 OVP

S5 OVP

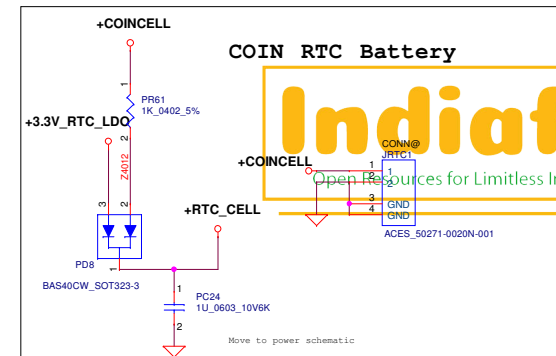




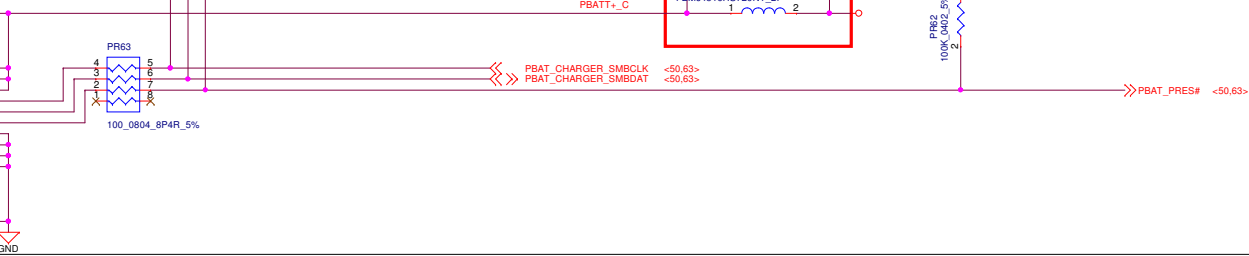
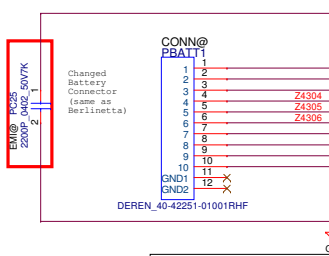
ESD Diodes



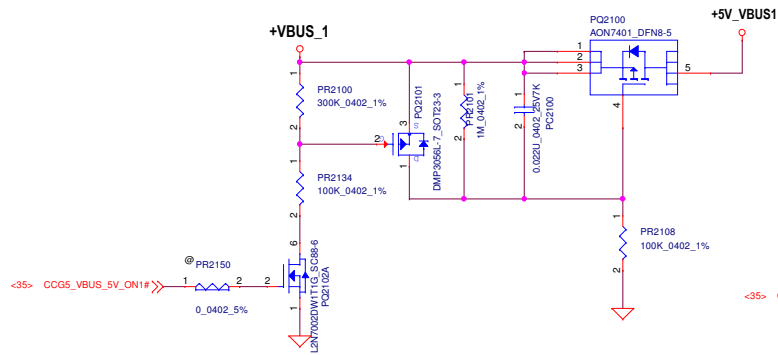
EMI Part (47.1)



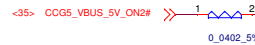
EMI Part (47.1) Primary Battery Connector



+5V_Vbus circuit



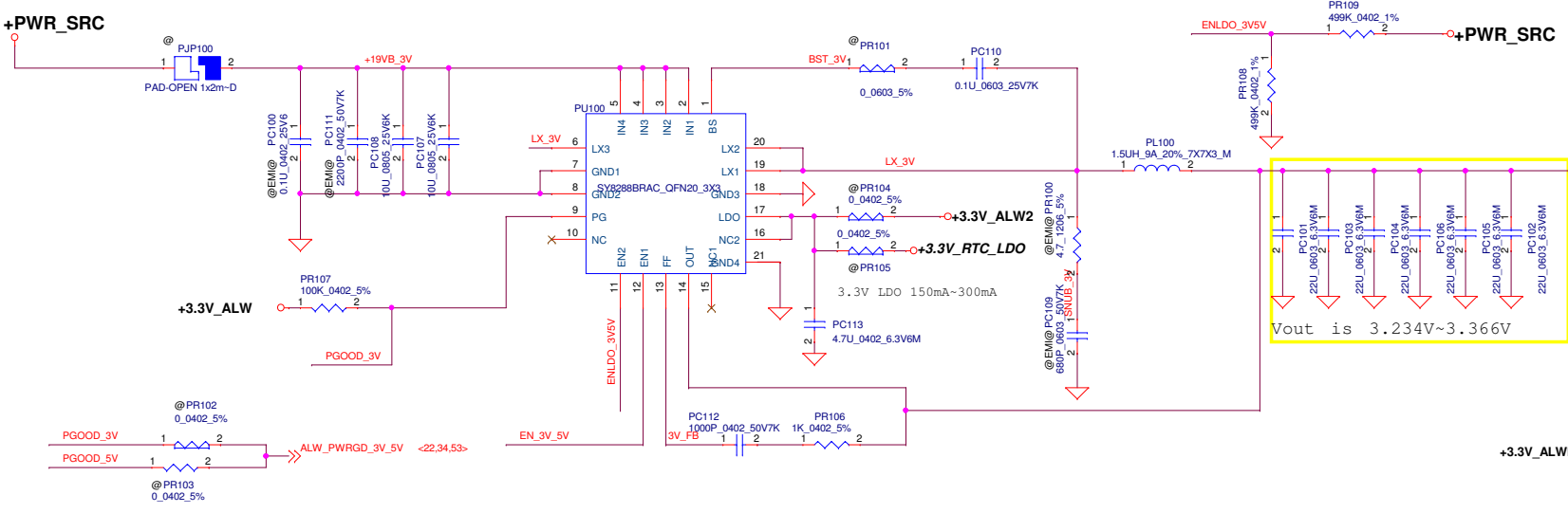
Check parts. Package is correct, schematic symbol is wrong.



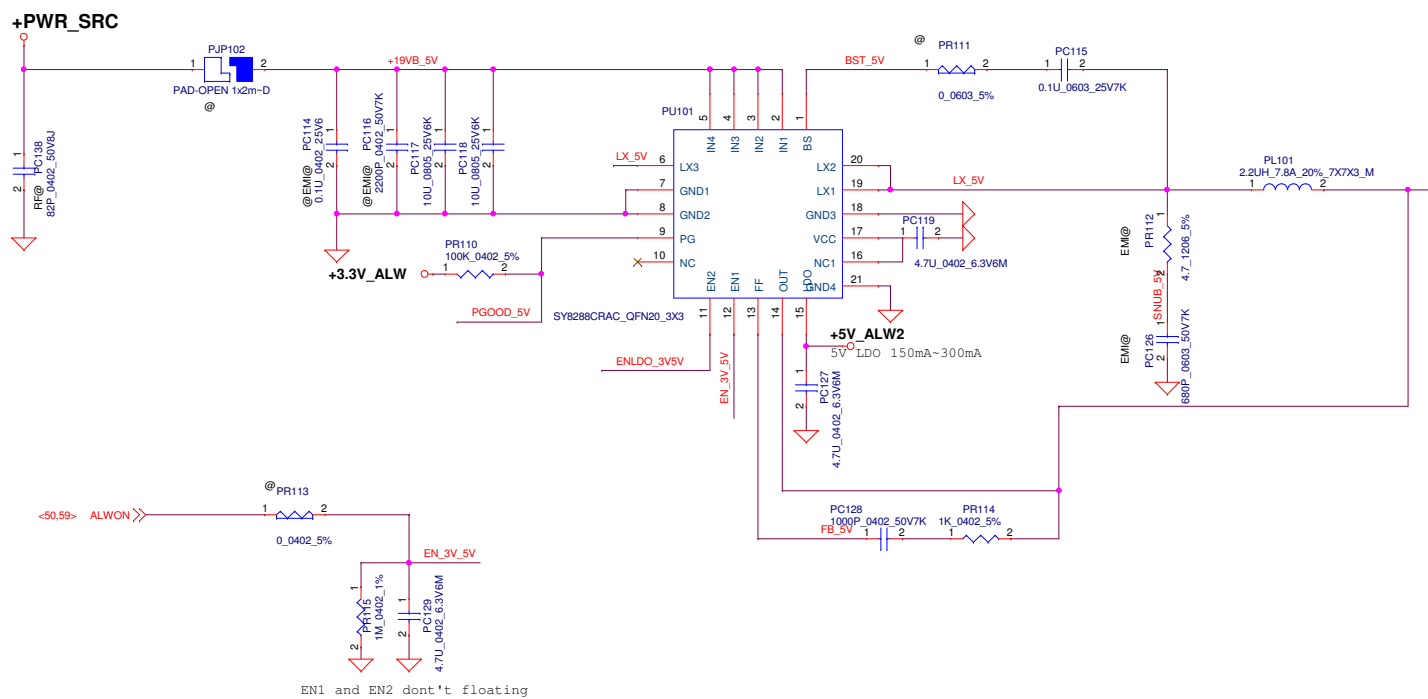
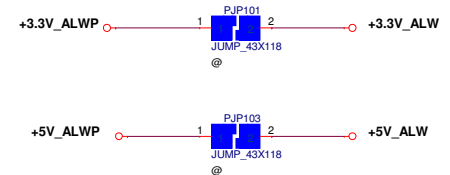
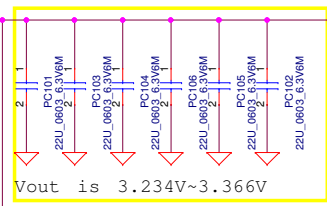
Check parts. Package is correct, schematic symbol is wrong.

Check parts. Package is correct, schematic symbol is wrong.

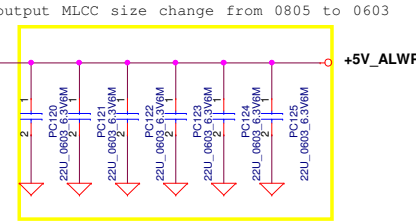
Check parts, couldn't read from Merle's screen capture. Package is correct, symbol is wrong.



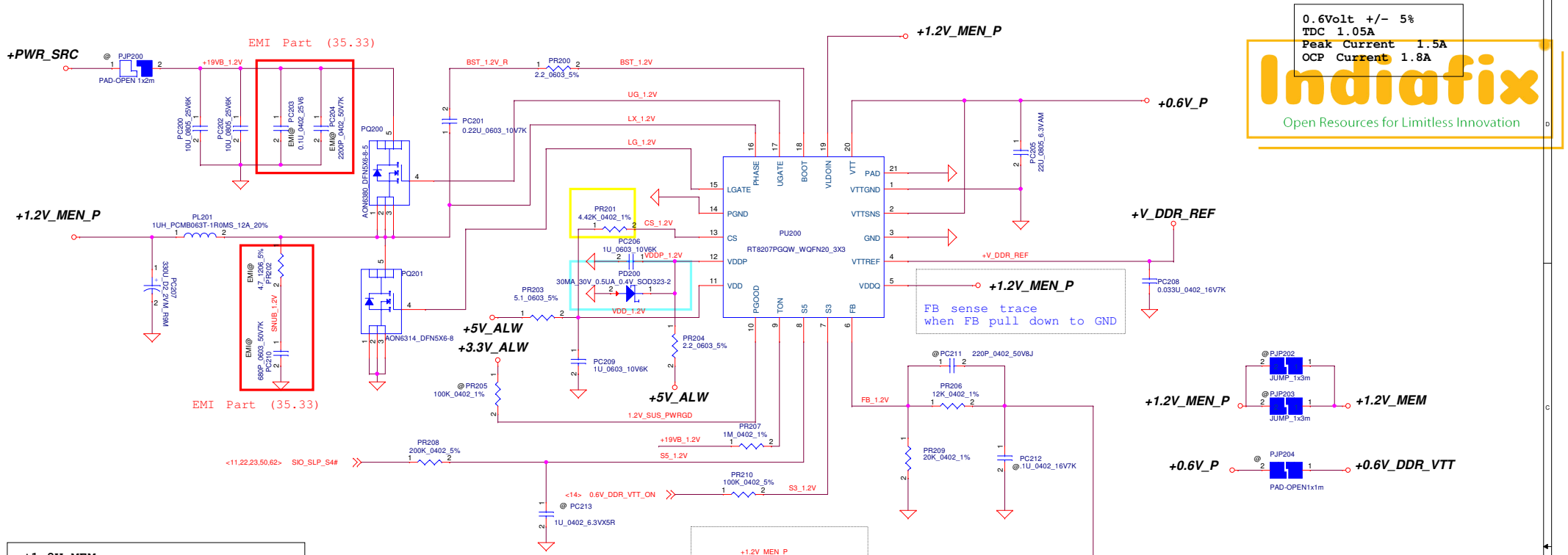
3V_ALW
 TDC 6.72A
 Peak Current 9.6A
 Current limit :12A
 TYP MAX
 Choke DCR 14.0mohm , 15.0mohm



5V_ALW
 TDC 7.46A
 Peak Current 7.83 A
 Current limit :12A
 TYP MAX
 Choke DCR 21.0mohm , 23.0mohm



EN1 and EN2 don't floating



0.6Volt +/- 5%
 TDC 1.05A
 Peak Current 1.5A
 OCP Current 1.8A

Indiafix

Open Resources for Limitless Innovation

+1.2V_MEM
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 TDC 9.57A
 Peak Current 13.67A
 OCP current 14.853A

	TYP	MAX
H/S Rds (on)	8.2mohm	10.5mohm
L/S Rds (on)	2.8mohm	3.5mohm
Choke DCR	7.4mohm	
Bulk cap ESR	9mohm	
Switching Frequency:	253kHz	

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

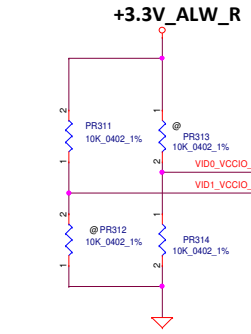
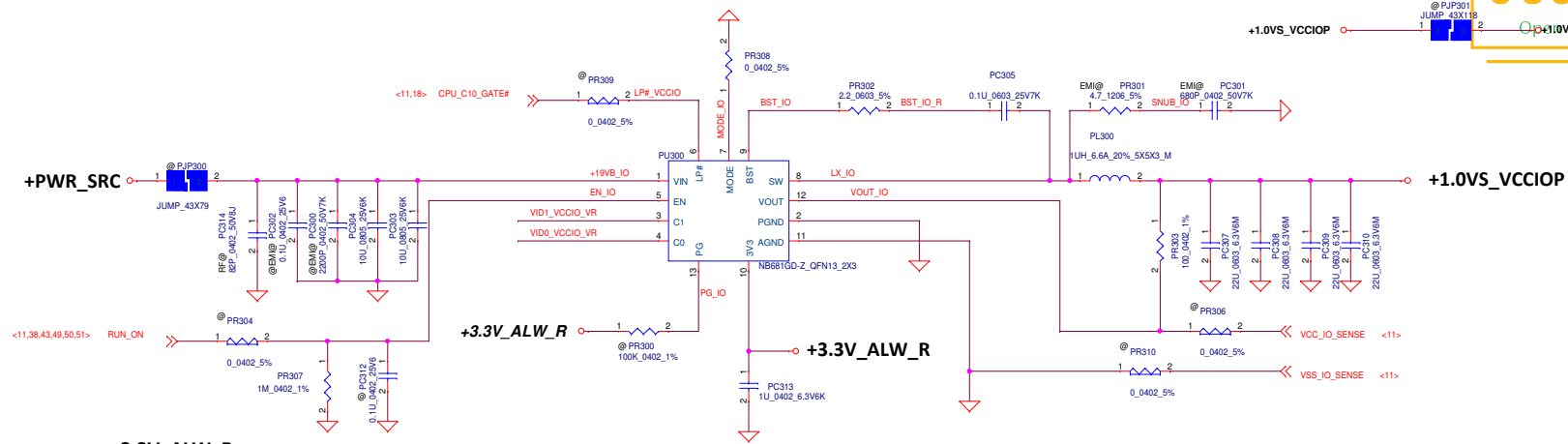
+1.2V_MEN_P
 FB sense trace

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Compal Electronics, Inc.
1.2VP/0.6VSP
 LA-F602P
 Date: Friday, March 09, 2018
 Sheet 60 of 72

File	Document Number	Rev
Size	1.0	1.0

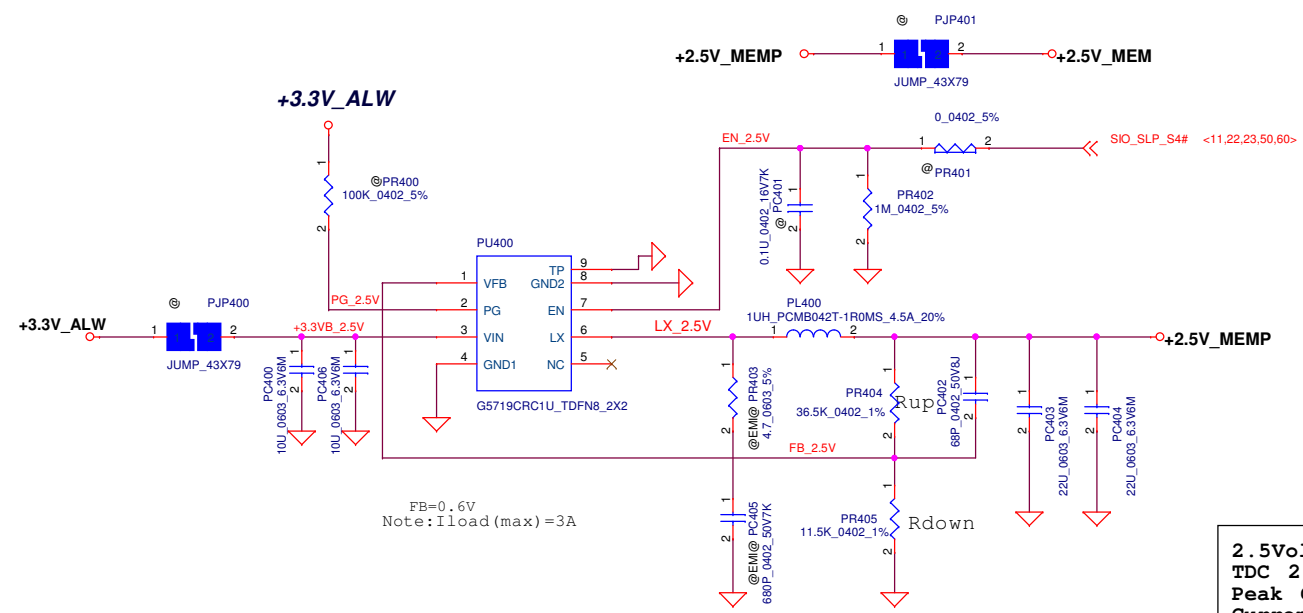


Vref mode =GND
 LP#=0, Vout=0V
 LP#=1, C1=0, C0=0, Vout=0.85V
 LP#=1, C1=0, C0=1, Vout=0.875V
 LP#=1, C1=1, C0=0, Vout=0.95V
 LP#=1, C1=1, C0=1, Vout=0.975V

Switching frequency 750 kHz

+1.0VS_VCCIO(0.95V)
 TDC 4.48 A
 Peak Current 6.4 A
 OCP Current 7.6 A
 MAX
 Choke DCR 14.0mohm

proximal
 PR303 0ohm PR306 100ohm PR310 100ohm
 remote
 PR303 100ohm PR306 0ohm PR310 0ohm



FB=0.6V
Note: Iload (max) = 3A

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

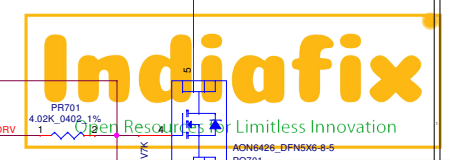
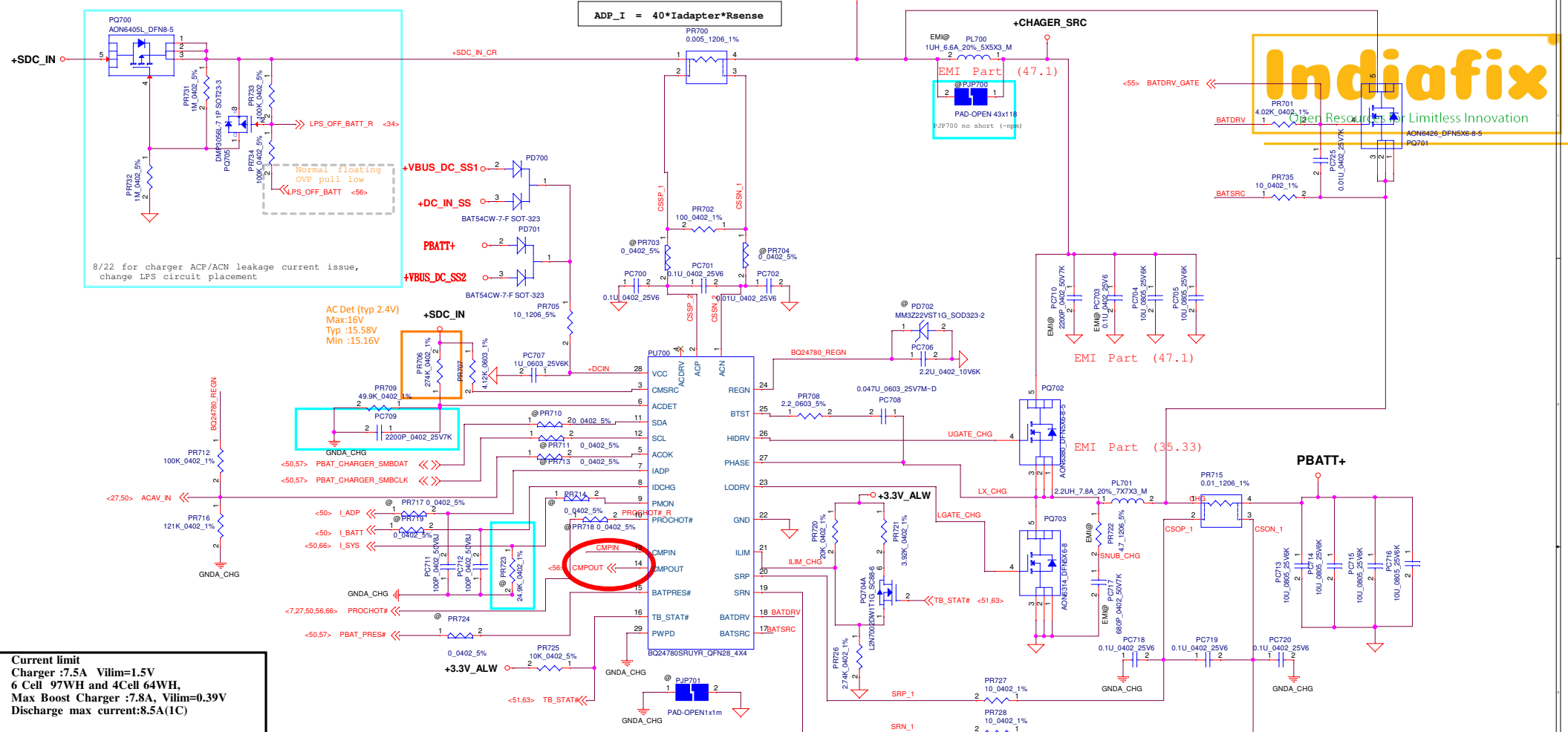
2.5Volt
TDC 2.1A
Peak Current 3A
Current Limit: 3.5A

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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Compal Electronics, Inc.			
Title +2.5V_MEM			
Size	Document Number	Rev	
	LA-F602P	1.0	
Date:	Friday, March 09, 2018	Sheet	62 of 72

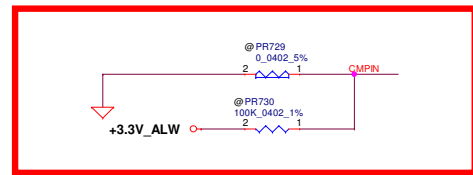
Iada=0~9. 23A (180W)
 $ADP_I = 40 * I_{adapter} * R_{sense}$
 +PWR_SRC



8/22 for charger ACP/ACN leakage current issue, change LPS circuit placement

AC Det (typ 2.4V)
 Max:16V
 Typ :15.58V
 Min :15.16V

Current limit
 Charger :7.5A Vilim=1.5V
 6 Cell 97WH and 4Cell 64WH,
 Max Boost Charger :7.8A, Vilim=0.39V
 Discharge max current:8.5A(1C)



2016/7/22
 For Temp voltage test ,
 +DC_IN setting for ACAVIN_NB need less than 17.55V ,
 so change PR737 from SD034665380
 (S RES 1/16W 665K +-1% 0402) to
 SD034634380(S RES 1/16W 634K +-1% 0402)

CMP_REF=2.3V (CMP_REF=2.3V
 +DC_IN>17V then ACAVIN_NB high +DC_IN>17.6V then ACAVIN_NB high
 for 3cell bat tery 13 05V for 4cell battery 17.4V Ma nar se tting)

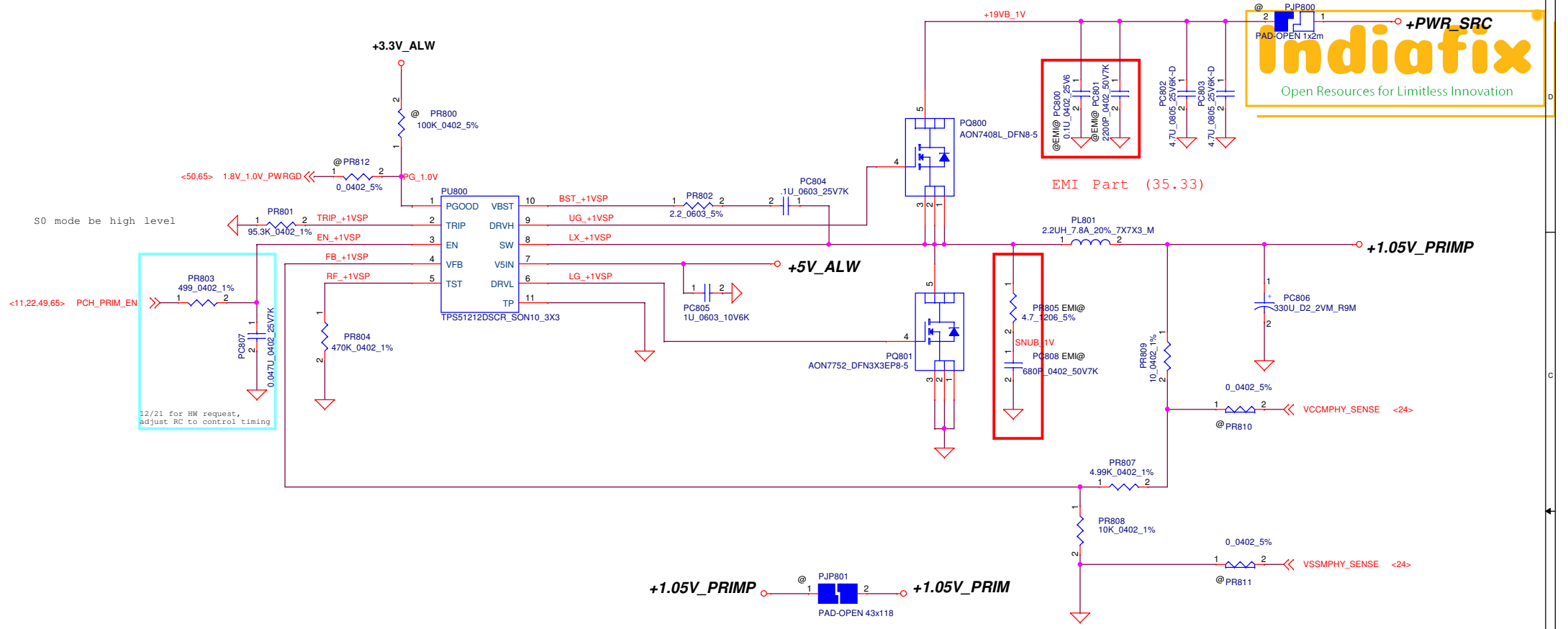
Crane and Miramar setting

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Compal Electronics, Inc.			
PWR_Charger			
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S0 mode be high level

<11.22,49,65> PCH_PRIM_EN

12/21 for HW request, adjust RC to control timing

EMI Part (35.33)

+1.05V_PRIMP @ PJP801 PAD-OPEN 43x118 +1.05V_PRIM

$$V_{out} = 0.7V * (1 + R1/R2) = 0.7V * (1 + (4.99/10))$$

$$V_{out} = 1.0493V$$

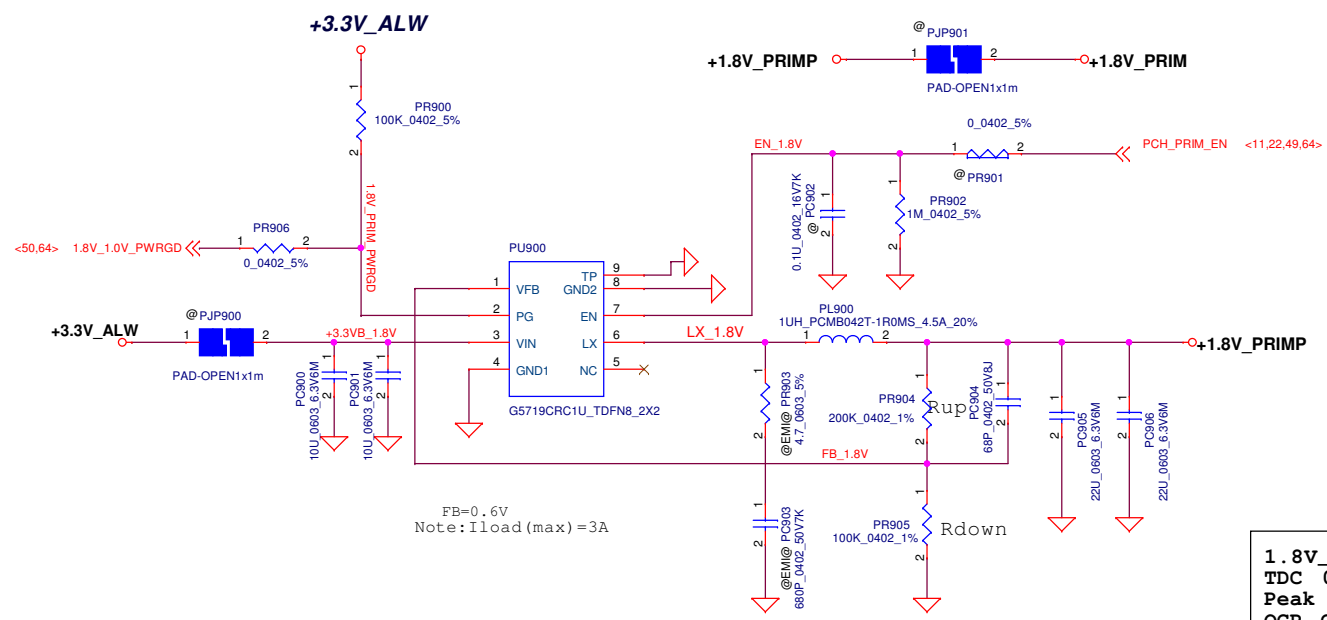
+1.05V_PRIMP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 5.398A
Peak Current 7.5A
OCP current 9A

	TYP	MAX
H/S Rds(on)	22.7mohm	32mohm
L/S Rds(on)	11.6mohm	14.5mohm
Choke DCR	13.5mohm	
Bulk cap ESR	9mohm	

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Compal Electronics, Inc.			
+1.05V_PRIM			
Size	Document Number	Rev 1.0	
LA-F602P		Date:	Friday, March 09, 2018
		Sheet	64 of 72






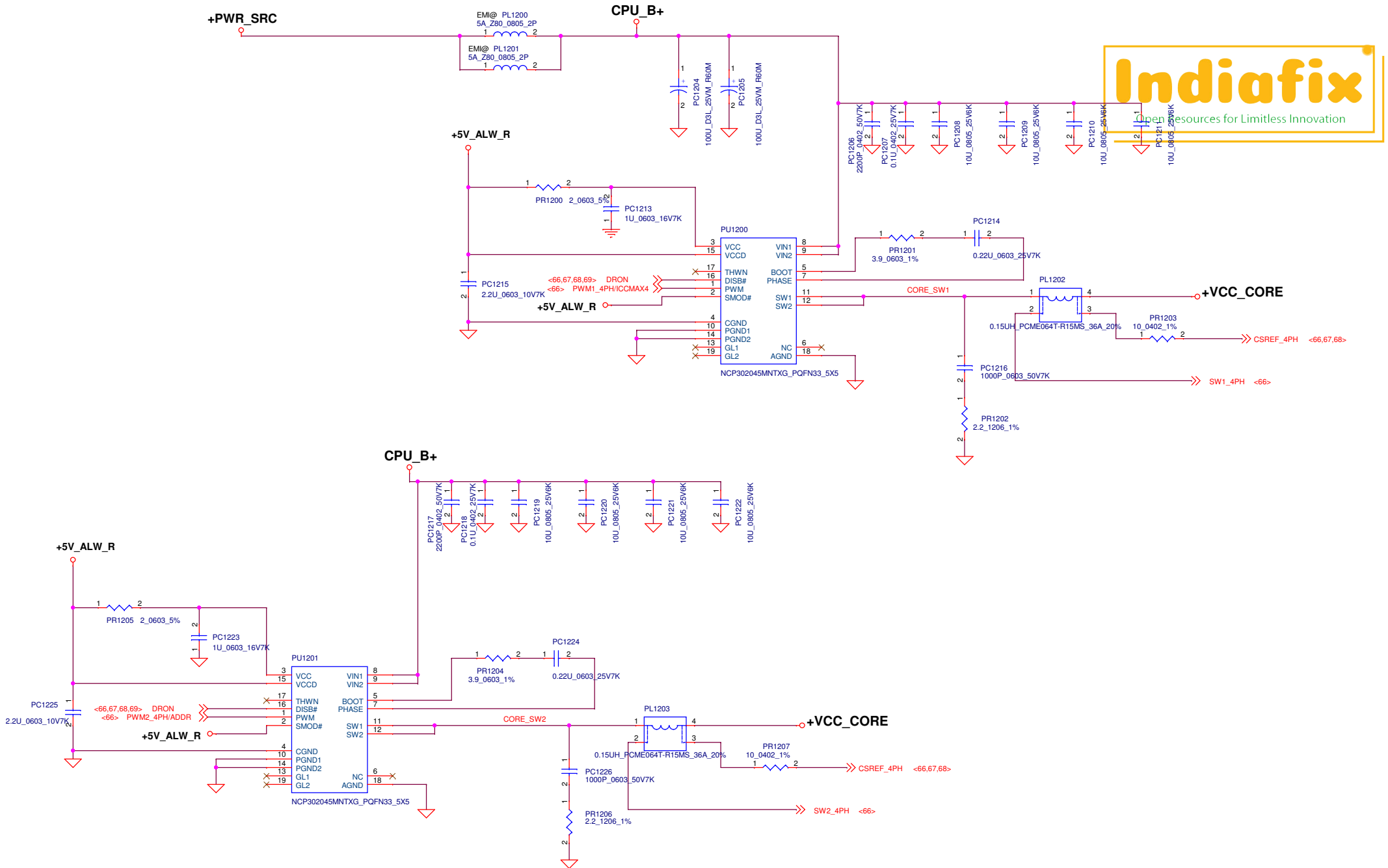
Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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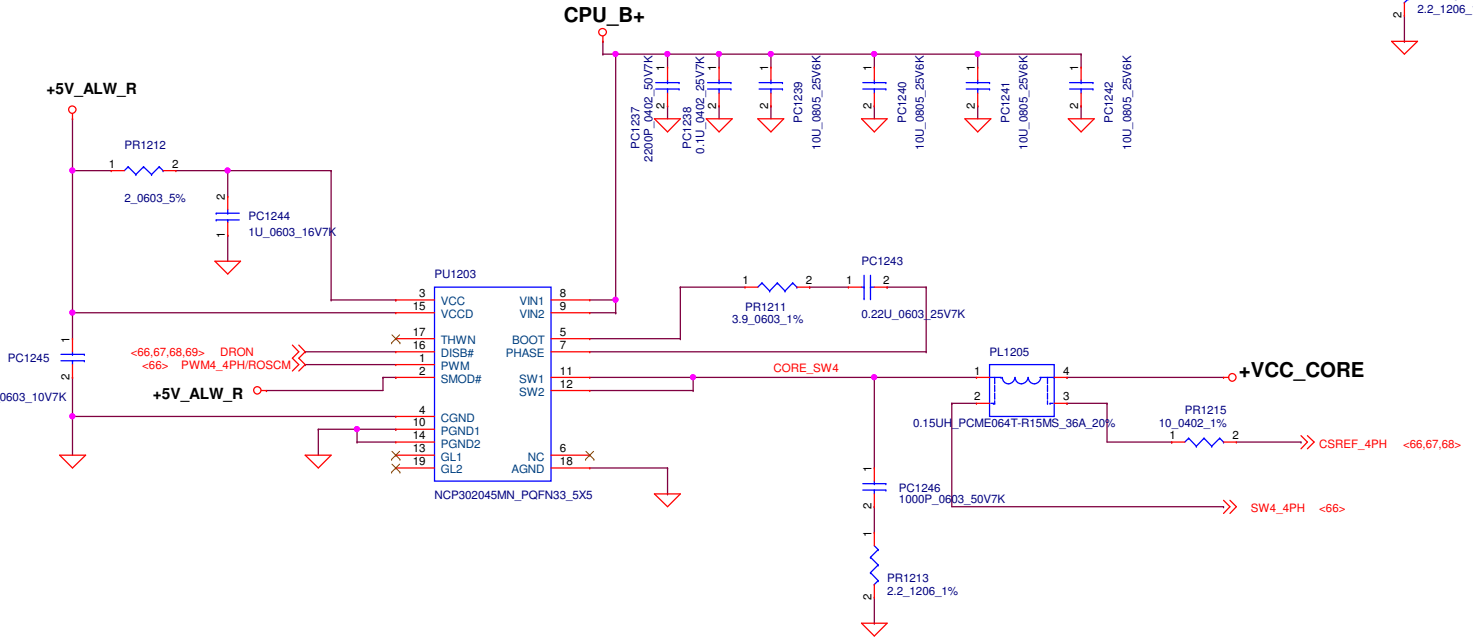
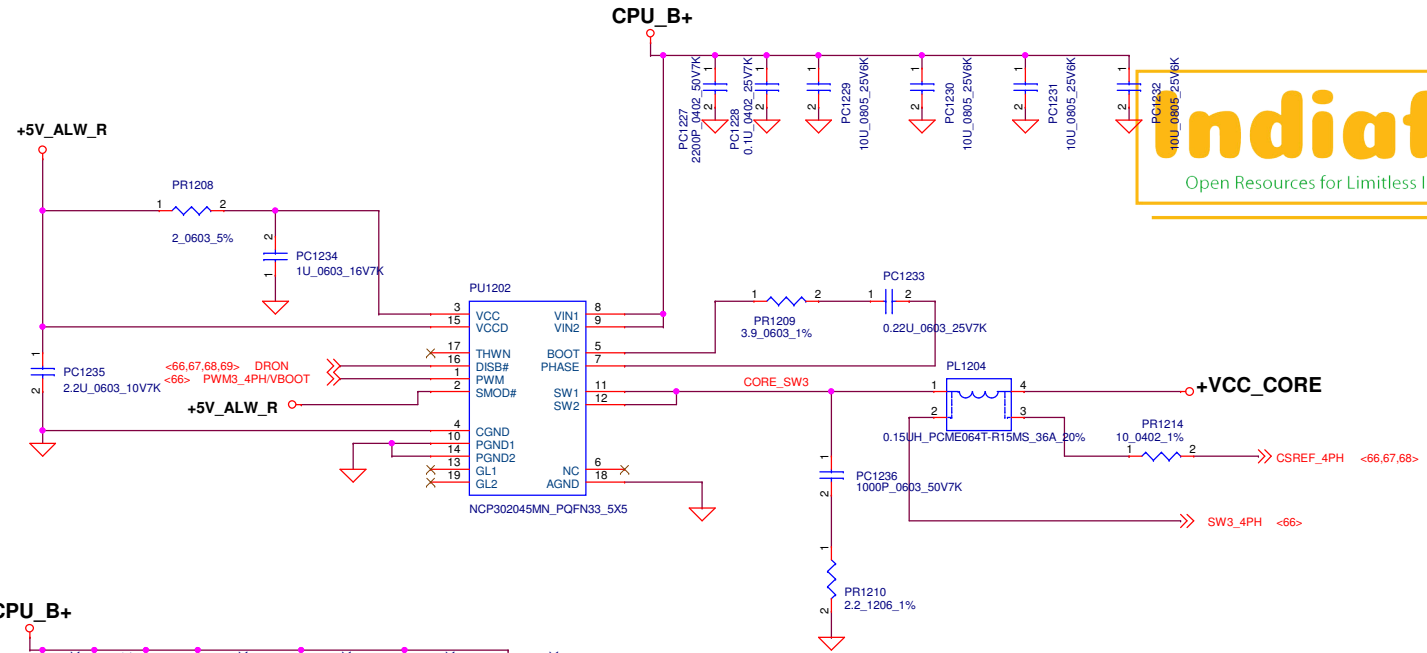
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Title		+1.8V PRIM	
Size	Document Number	LA-F602P	
Date:	Friday, March 09, 2018	Sheet	65 of 72
		Rev	1.0



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title		
				+VCC CORE Phase 1 & 2		
				Size	Document Number	Rev
				LA-F602P		1.0
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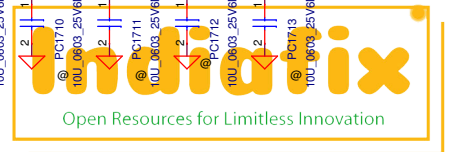
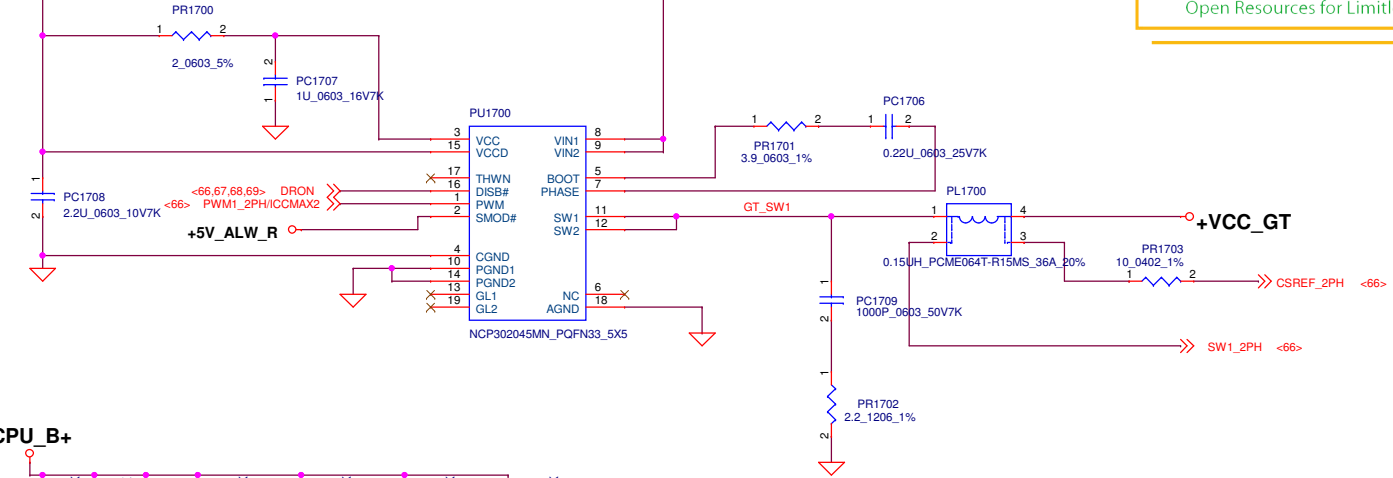
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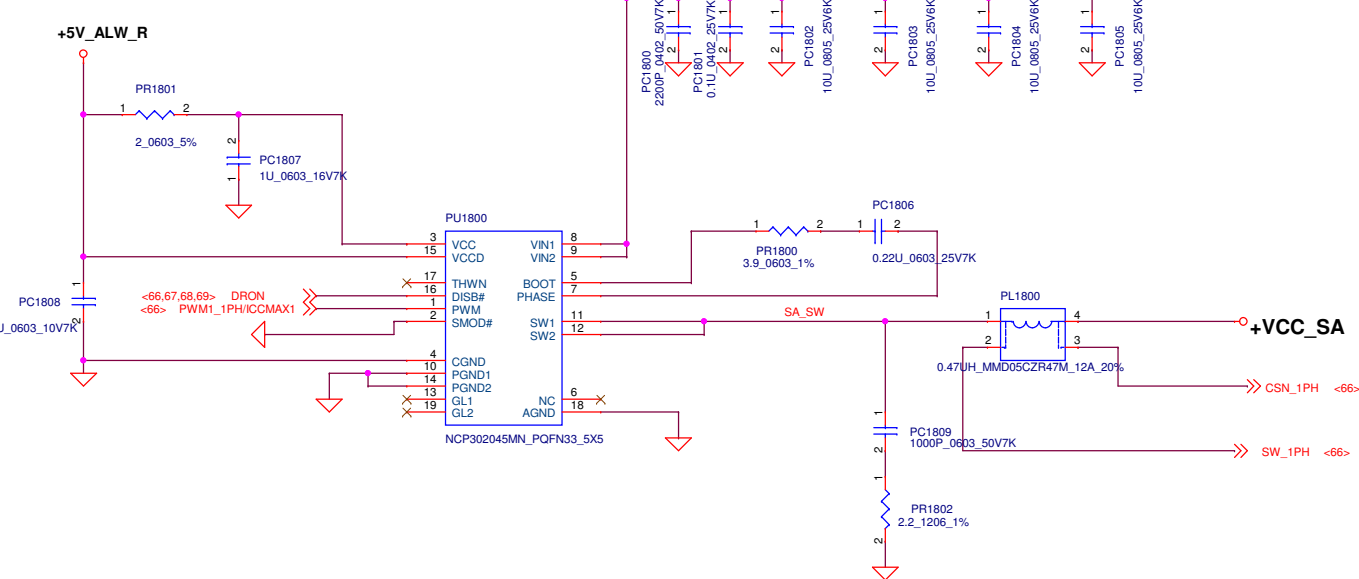
CPU B+

+5V_ALW_R



CPU B+

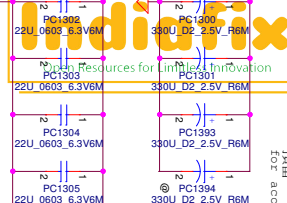
+5V_ALW_R



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+VCC_CORE

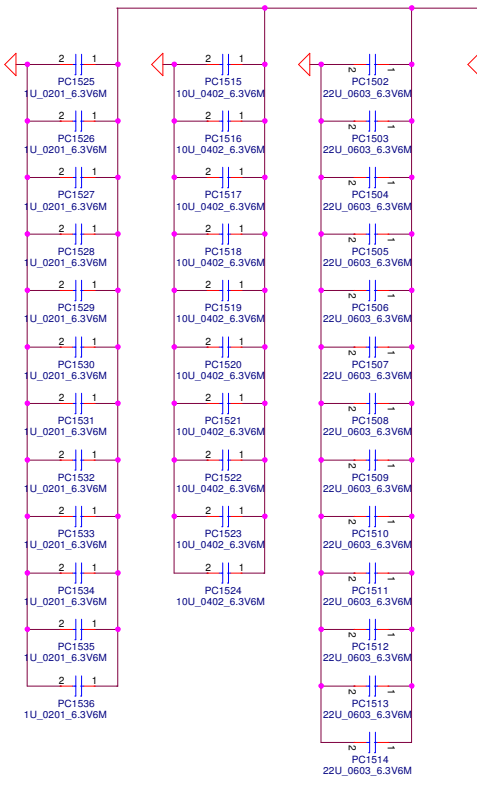
預留一欄 on CPU B01
for acoustic noise



VCC_CORE	X3
330UF	X2
22UF_0603	X22
10UF_0402	X21
1UF_0201	X48

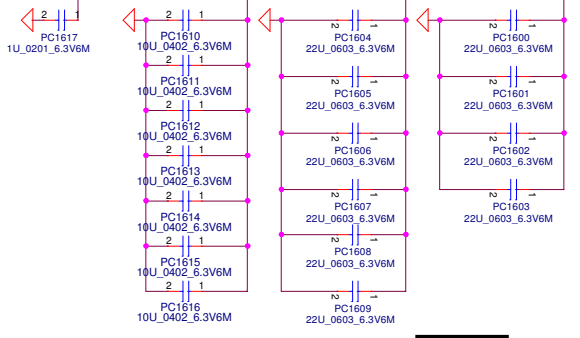
+VCC_GT

預留一欄 on CPU B01
for acoustic noise



VCC_GT	X1
470UF	X1
22UF_0603	X13
10UF_0402	X10
1UF_0201	X12

+VCC_SA



VCC_SA	X4 (VR output)
22UF_0603	X6
22UF_0603	X6
10UF_0402	X7
1UF_0201	X1



Compal Electronics, Inc.
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Version Change List (P. I. R. List)



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	
1	56	POWER	7/28	COMPAL	For detector setting , modify resistor to set input voltage need >17.16V when AC plug in	PR2032/PR2034/PR2053 change to SD034294280 S RES 1/16W 29.4K +-1% 0402	
2	63	POWER	7/28	COMPAL	For Battery discharging design, modify MOS and add RC component for FAE request	PQ701 change from SB00000MZ00 S TR AON6405L 1P DFN to SB000017B00 S TR AON6426 1N DFN5X6-8 PR701 change from 2.2 ohm to 4.02K ohm add PR735 10 ohm and PC725 0.01U	Rev.01
3	61	POWER	8/7	COMPAL	To support modern standby function , change VCCIO IC to achieve	PU300 change from SA00008I400 S IC SY8288RAC QFN 20P PWM to SA000085000 S IC NB681GD-Z QFN 13P PWM	Rev.03
4	57 58 61	POWER	8/22	COMPAL	For RF team request, add RF CAP to +PWR_SRC	Add PC30/PC138/PC314 SE071820J80 S CER CAP 82P 50V J NPO 0402	Rev.03
5	60	POWER	8/22	COMPAL	Add diode to avoid VCC 5V negative voltage issue	Add PD200 SCS00009P00 S SCH DIO 30MA 30V 0.5UA 0.4V SOD323-2	Rev.03
6	63	POWER	8/22	COMPAL	Move PQ700 circuit to left of PR700 for leakage issue, ACP/ACN will leak voltage when battery mode	Move PQ700 circuit	Rev.03
7	55	POWER	8/23	COMPAL	To improve +SDC_IN drop and Pq11 close slowly problem,pop diode to achieve	Pop PD1 SCS00000W00 S SCH DIO SX34 SMA	Rev.03
8	55	POWER	8/23	COMPAL	To improve VBUS_ECOK action, add pull low resistor	Add PR74/PR75/PR76 100K ohm	Rev.03
9	56	POWER	8/23	COMPAL	To improve LM393 design , change reference voltage	Add PR74/PR75/PR76 100K ohm	Rev.03
10	55	POWER	10/18	COMPAL	For AC/DC switch function, add diode to make it achieved	Add PD11/PD12/PD13	Rev.04
11	55	POWER	10/18	COMPAL	Disable fast swap function, so depop barrel disconnected detector	depop disconnected detector and add PR2161/PR2162 to recovery to P8 circuit	Rev.04
12	57 58 59 63 67	POWER	10/18	COMPAL	For EMI requestion, remove 1000P/1U tested MLCC on input side	remove 14 1000P and 14 1U MLCC on +DGFF_B+ rail, 3.3V_ALW/5V_ALW/3.3V_ALW_R/5V_ALW_R input side, +CHAGER_SRC rail and CPU_B+ input side	Rev.04
13	55 57 60 63 64	POWER	12/21	COMPAL	change PMOS and NMOS footprint to improve SMT process	Change PQ10/PQ11/PQ700 footprint to common footprint Q_P_DFN56-8-5 Change PQ2100/PQ2104 footprint to common footprint Q_P_DFN33-8-5 Change PQ701/PQ702/PQ703/PQ200/PQ201 footprint to common footprint Q_N_DFN33-8-5 Change PQ800/PQ801 footprint to common footprint Q_N_DFN33-8-5	Rev.06
14	63	POWER	12/21	COMPAL	Change ACDET CAP to make it quickly detected	Change PC709 from 0.1UF to 2200PF	Rev.06
15	64	POWER	12/21	COMPAL	For HW request, adjust enable pin RC to control 1.05V_PRIM timing	Change PR803 from 0 ohm to 499 ohm Pop PC807 and change from 0.22U to 0.047U	Rev.06