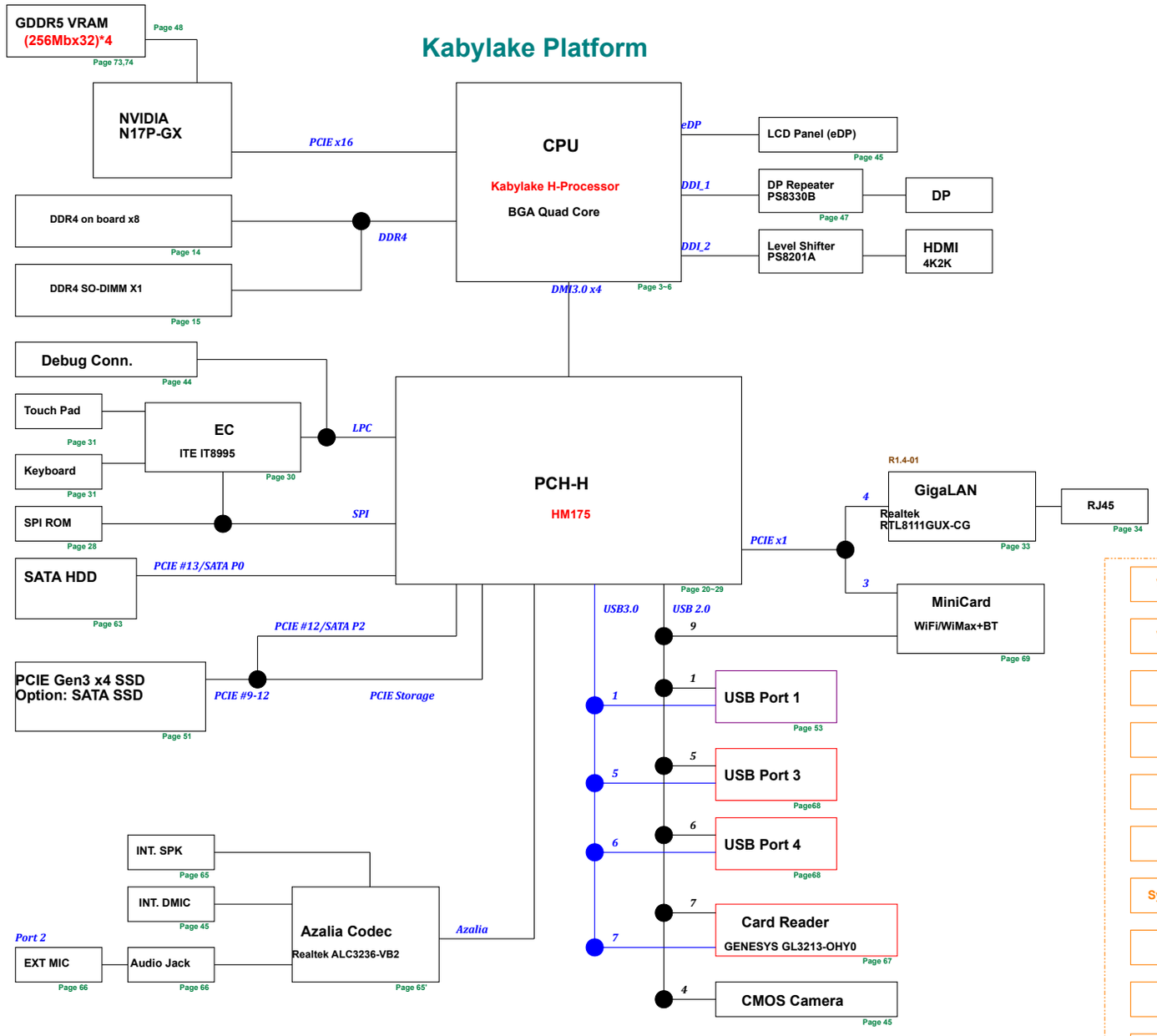
FX502VE/D Block Diagram

Kabylake Platform



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Project Name: FX502VD			Rev: 2.0
Title : Block Diagram			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang	
Date: Wednesday, February 15, 2017	Sheet 1 of 102		

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	BC1B#	Native	BC_1B#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_33DEV1_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_33DEV2_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#B	Native	ME_BusParInBack		PU 10K(E)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_FREQ_REQ0#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN# _X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_CLAN# _X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT# _X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MSWV_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP914	PD		
GPP_B15	GPI	Native	GSPI0_CS# (Test Point)			
GPP_B16	GPI	Native	GSPI0_CLK (Test Point)			
GPP_B17	GPI	Native	GSPI0_MISO (Test Point)			
GPP_B18	GPO	Strap	PCH_GPP918	PD		
GPP_B19	GPI	GPO	PCH_GPP919/WT_ON_PCH		PD 10K(E)	
GPP_B20	GPI	GPO	PCH_GPP920/SPIWEDATA_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP921/SCKFRAM_PCH		PU 10K(E)	+3VS
GPP_B22	GPO	Strap	PCH_GPP922	PD		
GPP_B23	GPO	GPO	SMILLASERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	SRC	Strap	PCH_GPPC2	PD		
GPP_C3	SMLOCLK	Native	SMLO_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLODATA	Native	SMLO_DAT		PU 2.2K	+3VSUS
GPP_C5	SRC	Strap	PCH_GPPC5	PD		+3VSUS
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SELO		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NPC_ID		PD 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(E)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(E)	+3VS
GPP_C18	GPI	Native	I2C1 _SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1 _SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(E)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 10K(E)	+3VSUS
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT			
GPP_D1	GPO	GPO	GPIO_3 PCH2E_PWR			
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#		PD 100K(E)	
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCH_I2C		PD 10K	
GPP_D10	GPI	Strap	PCH_I2C1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID		PD 10K(E)	
GPP_D12	GPI	Strap	TOUCH_PANEL_ID		PD 10K(E)	
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(E)	+3VSUS
GPP_D14	GPO	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPO	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)		PU 10K(E)	+3V
GPP_E4	GPI	Native	MOFFO_DEVSLP		PU 10K(E)	+3VS
GPP_E5	GPI	Native	SATA1_DEVSLP		PU 10K(E)	+3VS
GPP_E6	GPI	Native	MOFF1_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(E)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	(N.C)			
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	SATA1_HDD_DEVSLP		PU 10K(E)	+3VS
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPI	(N.C)		(N.C)	
GPP_F20	GPI	GPI	(N.C)			
GPP_F21	GPI	GPI	(N.C)		(N.C)	
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPI	(N.C)			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1# _X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H5	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H6	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H7	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H8	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H9	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	(N.C)		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPI	(N.C)		(N.C)	
GPP_I1	GPI	GPI	(N.C)		(N.C)	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	GPI	(N.C)			
GPP_I4	GPI	GPI	GPP_I4		PU 100K	
GPP_I5	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I6	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)
GPP_I7	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I8	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)
GPP_I9	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I10	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	PCH_GPD2#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(E)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 150K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS5#		PD 150K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(E)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PHYEN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	(N.C)	
GPA1	OD	GPO	CHG_LED#	PU 10K (E)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (E)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	Alt	PWM	PM_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_EC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	HDMI_ON#2	PD 10K	
GPB6	OD	GPO	BC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (E)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_THRMTRIP#	PU 10K (E)	+3VSUS
GPC4	I	GPI	EC_SATA/CHG#4	PU 10K (E)	+3VSUS
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	O	GPO	EC_SPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/WAC_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/USB_SS#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PU 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN# _WCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUS6#	PU 100K	
GPE6	OD	GPO	EC_GPE6		
GPE7	OD	GPO	THRO_CPU#	PU 10K(E) (N.C)	+3VA_EC (N.C)

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0 CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0 DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PHOLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCK#/EC_SCK#_PCH	PU 10K (E)	
GPG4	GPI		EC_SI/EC_SI_PCH	PU 10K (E)	
GPG5	GPI		EC_SO/EC_SO_PCH	PU 10K (E)	
GPG6	O	GPO	USB30_5VSUS		
GPG7	GPI		EC_SCK_PCH	PU 10K (E)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3 CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3 DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_SUSC#2#	PU 10K(E)	
GPH4	O	GPO	DPWROK_EC	PU 10K	
GPH5	O	GPO	PM_PWROK	PU 10K	
GPH6	O	GPO	PM_SYSPWROK	PU 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S0#		
GPI1	I	GPI	SYSSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	(N.C)	(N.C)
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	(N.C)	(N.C)
GPI7	Alt	AD	WA_MAX_POWER	PU 100K x PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB11_5VSUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_GPJ6/PBA_WAKE#	PU 100K(E)	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/ECG0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/ECD1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/ECG2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/ECC3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ECCK		CLK_EBCH33_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h

EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
VGA Thermal Sensor	90h
CPU Thermal Sensor	98h
Power Thermal Sensor	70h

Device Identification

CPU Thermal Sensor	
1st	0000231809
2nd	

GL520VW PCIE & USB Function define

Skylake HM170

%UO	HDD Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06	USB3_IO	
07	USB3#07 / PCIE#01	CardReader, USB3(RSV)	SRC1
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN	SRC4
11	PCIE#05 / GBE		SRC5
12	PCIE#06	TBT	
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE		
16	PCIE#10 / SATA#1	PCIE*4 SSD	SRC6
17	PCIE#11	SATA SSD	
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	1st HDD	
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	
USB2_03	
USB2_04	Camera
USB2_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2
USB2_07	CardReader
USB2_08	N-Key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x 2	x 4	NA
8	USB3 #8	PCIE #2			
9	USB3 #9	PCIE #3	x 2		
10	USB3 #10	PCIE #4	GbE		
11	PCIE #5		GbE	x 2	x 4
12	PCIE #6				NA
13	PCIE #7			x 2	
14	PCIE #8				
15	PCIE #9	SATA #0	GbE	x 2	x 4
16	PCIE #10	SATA #1			Intel IRST PCIE Storage Device #1
17	PCIE #11				
18	PCIE #12		GbE		
19	PCIE #13	SATA #0*	GbE	x 2	x 4
20	PCIE #14	SATA #1*			Intel IRST PCIE Storage Device #2
21	PCIE #15	SATA #2		x 2	
22	PCIE #16	SATA #3			
23	PCIE #17	SATA #4		x 2	x 4
24	PCIE #18	SATA #5			Intel IRST PCIE Storage Device #3
25	PCIE #19	SATA #6		x 2	
26	PCIE #20	SATA #7			

SKL PCH-H H170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7				
8	USB3 #8				
9	PCIE #3			x 2	NA
10	PCIE #4		GbE		
11	PCIE #5		GbE	x 2	x 4
12	PCIE #6				NA
13	PCIE #7			x 2	
14	PCIE #8				
15	PCIE #9	SATA #0	GbE	x 2	x 4
16	PCIE #10	SATA #1			Intel IRST PCIE Storage Device #1
17	PCIE #11				
18	PCIE #12		GbE		
19	PCIE #13	SATA #0*	GbE	x 2	x 4
20	PCIE #14	SATA #1*			Intel IRST PCIE Storage Device #2
21	PCIE #15	SATA #2		x 2	
22	PCIE #16	SATA #3			
23	SATA #4			NA	NA
24	SATA #5				
25	PCIE #19			x 2	
26	PCIE #20				

SKL PCH-H HM170 HSIO

1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x 2	x 4	NA
8	USB3 #8	PCIE #2			
9	PCIE #3		x 2		
10	PCIE #4		GbE		
11	PCIE #5		GbE	x 2	x 4
12	PCIE #6				NA
13	PCIE #7			x 2	
14	PCIE #8				
15	PCIE #9	SATA #0	GbE	x 2	x 4
16	PCIE #10	SATA #1			Intel IRST PCIE Storage Device #1
17	PCIE #11				
18	PCIE #12		GbE		
19	PCIE #13	SATA #0*	GbE	x 2	x 4
20	PCIE #14	SATA #1*			Intel IRST PCIE Storage Device #2
21	PCIE #15	SATA #2		x 2	
22	PCIE #16	SATA #3			
23				NA	NA
24					
25				NA	
26					

PCIEG

EDS_544924
table 2-17

R0.1-25

U0301C

BGA1440

	E25	PEG_RXP[0]	PEG_TXP[0]	B25			
PCIENB_RXP0	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PCIENB_TXP0		
PCIENB_RXN0					PCIENB_TXN0		
	E24	PEG_RXP[1]	PEG_TXP[1]	B24			
PCIENB_RXP1	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PCIENB_TXP1		
PCIENB_RXN1					PCIENB_TXN1		
	E23	PEG_RXP[2]	PEG_TXP[2]	B23			
PCIENB_RXP2	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PCIENB_TXP2		
PCIENB_RXN2					PCIENB_TXN2		
	E22	PEG_RXP[3]	PEG_TXP[3]	B22			
PCIENB_RXP3	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PCIENB_TXP3		
PCIENB_RXN3					PCIENB_TXN3		
	E21	PEG_RXP[4]	PEG_TXP[4]	B21			
PCIENB_RXP4	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PCIENB_TXP4		
PCIENB_RXN4					PCIENB_TXN4		
	E20	PEG_RXP[5]	PEG_TXP[5]	B20			
PCIENB_RXP5	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PCIENB_TXP5		
PCIENB_RXN5					PCIENB_TXN5		
	E19	PEG_RXP[6]	PEG_TXP[6]	B19			
PCIENB_RXP6	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PCIENB_TXP6		
PCIENB_RXN6					PCIENB_TXN6		
	E18	PEG_RXP[7]	PEG_TXP[7]	B18			
PCIENB_RXP7	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PCIENB_TXP7		
PCIENB_RXN7					PCIENB_TXN7		
	D17	PEG_RXP[8]	PEG_TXP[8]	A17			
PCIENB_RXP8	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PCIENB_TXP8		
PCIENB_RXN8					PCIENB_TXN8		
	F16	PEG_RXP[9]	PEG_TXP[9]	C16			
PCIENB_RXP9	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PCIENB_TXP9		
PCIENB_RXN9					PCIENB_TXN9		
	D15	PEG_RXP[10]	PEG_TXP[10]	A15			
PCIENB_RXP10	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PCIENB_TXP10		
PCIENB_RXN10					PCIENB_TXN10		
	F14	PEG_RXP[11]	PEG_TXP[11]	C14			
PCIENB_RXP11	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PCIENB_TXP11		
PCIENB_RXN11					PCIENB_TXN11		
	D13	PEG_RXP[12]	PEG_TXP[12]	A13			
PCIENB_RXP12	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PCIENB_TXP12		
PCIENB_RXN12					PCIENB_TXN12		
	F12	PEG_RXP[13]	PEG_TXP[13]	C12			
PCIENB_RXP13	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PCIENB_TXP13		
PCIENB_RXN13					PCIENB_TXN13		
	D11	PEG_RXP[14]	PEG_TXP[14]	A11			
PCIENB_RXP14	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PCIENB_TXP14		
PCIENB_RXN14					PCIENB_TXN14		
	F10	PEG_RXP[15]	PEG_TXP[15]	C10			
PCIENB_RXP15	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PCIENB_TXP15		
PCIENB_RXN15					PCIENB_TXN15		

+VCCIO — 24.9Ohm — R0301 — 1% — PEG_RCOMP — G2 PEG_RCOMP

21 DMI_TXP0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_RXP0	21	
21 DMI_TXN0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_RXN0	21	
21 DMI_TXP1	E6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_RXP1	21	
21 DMI_TXN1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_RXN1	21	
21 DMI_TXP2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_RXP2	21	
21 DMI_TXN2	E5	DMI_RXN[2]	DMI_TXN[2]	A5	DMI_RXN2	21	
21 DMI_TXP3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_RXP3	21	
21 DMI_TXN3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_RXN3	21	

BGA1140

R0301 close to CPU
PEG_COMP trace length <400mils

PCIENB_RXN[15:0] 70

PCIENB_RXN0 … PCIENB_RXN15

PCIENB_RXP[15:0] 70

PCIENB_RXP0 … PCIENB_RXP15

PCIENB_TXN0	CX0301	1	2	0.22UF/6.3V	PCIEG_RXN15
PCIENB_TXN1	CX0302	1	2	0.22UF/6.3V	PCIEG_RXN14
PCIENB_TXN2	CX0303	1	2	0.22UF/6.3V	PCIEG_RXN13
PCIENB_TXN3	CX0304	1	2	0.22UF/6.3V	PCIEG_RXN12
PCIENB_TXN4	CX0305	1	2	0.22UF/6.3V	PCIEG_RXN11
PCIENB_TXN5	CX0306	1	2	0.22UF/6.3V	PCIEG_RXN10
PCIENB_TXN6	CX0307	1	2	0.22UF/6.3V	PCIEG_RXN9
PCIENB_TXN7	CX0308	1	2	0.22UF/6.3V	PCIEG_RXN8
PCIENB_TXN8	CX0309	1	2	0.22UF/6.3V	PCIEG_RXN7
PCIENB_TXN9	CX0310	1	2	0.22UF/6.3V	PCIEG_RXN6
PCIENB_TXN10	CX0311	1	2	0.22UF/6.3V	PCIEG_RXN5
PCIENB_TXN11	CX0312	1	2	0.22UF/6.3V	PCIEG_RXN4
PCIENB_TXN12	CX0313	1	2	0.22UF/6.3V	PCIEG_RXN3
PCIENB_TXN13	CX0314	1	2	0.22UF/6.3V	PCIEG_RXN2
PCIENB_TXN14	CX0315	1	2	0.22UF/6.3V	PCIEG_RXN1
PCIENB_TXN15	CX0316	1	2		PCIEG_RXN0

PCIEG_RXN[15:0] 70

PCIENB_TXP0	CX0317	1	2	0.22UF/6.3V	PCIEG_RXP15
PCIENB_TXP1	CX0318	1	2	0.22UF/6.3V	PCIEG_RXP14
PCIENB_TXP2	CX0319	1	2	0.22UF/6.3V	PCIEG_RXP13
PCIENB_TXP3	CX0320	1	2	0.22UF/6.3V	PCIEG_RXP12
PCIENB_TXP4	CX0321	1	2	0.22UF/6.3V	PCIEG_RXP11
PCIENB_TXP5	CX0322	1	2	0.22UF/6.3V	PCIEG_RXP10
PCIENB_TXP6	CX0323	1	2	0.22UF/6.3V	PCIEG_RXP9
PCIENB_TXP7	CX0324	1	2	0.22UF/6.3V	PCIEG_RXP8
PCIENB_TXP8	CX0325	1	2	0.22UF/6.3V	PCIEG_RXP7
PCIENB_TXP9	CX0326	1	2	0.22UF/6.3V	PCIEG_RXP6
PCIENB_TXP10	CX0327	1	2	0.22UF/6.3V	PCIEG_RXP5
PCIENB_TXP11	CX0328	1	2	0.22UF/6.3V	PCIEG_RXP4
PCIENB_TXP12	CX0329	1	2	0.22UF/6.3V	PCIEG_RXP3
PCIENB_TXP13	CX0330	1	2	0.22UF/6.3V	PCIEG_RXP2
PCIENB_TXP14	CX0331	1	2	0.22UF/6.3V	PCIEG_RXP1
PCIENB_TXP15	CX0332	1	2		PCIEG_RXP0

PCIEG_RXP[15:0] 70

Display

U0301D

BGA1440

47 DDI1_TXP0_DP	K36	DDI1_TXP[0]	EDP_TXP[0]	D29	EDP_TXP0	45	
47 DDI1_TXN0_DP	K37	DDI1_TXN[0]	EDP_TXN[0]	E29	EDP_TXN0	45	
47 DDI1_TXP1_DP	J35	DDI1_TXP[1]	EDP_TXP[1]	F28	EDP_TXP1	45	
47 DDI1_TXN1_DP	J34	DDI1_TXN[1]	EDP_TXN[1]	E28	EDP_TXN1	45	
DP 47 DDI1_TXP2_DP	H37	DDI1_TXP[2]	EDP_TXP[2]	B29	EDP_TXN2	45	EDP
47 DDI1_TXN2_DP	H36	DDI1_TXN[2]	EDP_TXN[2]	A29	EDP_TXP2	45	
47 DDI1_TXP3_DP	J37	DDI1_TXP[3]	EDP_TXP[3]	B28	EDP_TXN3	45	
47 DDI1_TXN3_DP	J38	DDI1_TXN[3]		C28	EDP_TXP3	45	
47 DDI1_AUXP_DP	D27	DDI1_AUXP	EDP_AUXP	C26	EDP_AUXP	45	
47 DDI1_AUXN_DP	E27	DDI1_AUXN	EDP_AUXN	B26	EDP_AUXN	45	
48 DDI2_TXP2_HDMI	H34	DDI2_TXP[0]					
48 DDI2_TXN2_HDMI	H33	DDI2_TXN[0]					
HDMI 48 DDI2_TXP1_HDMI	F37	DDI2_TXP[1]	EDP_DISP_UTIL	A33	eDP_DISP_UTIL	1	T0301
48 DDI2_TXN1_HDMI	G38	DDI2_TXN[1]					
48 DDI2_TXP0_HDMI	F34	DDI2_TXP[2]					
48 DDI2_TXN0_HDMI	F35	DDI2_TXN[2]	EDP_RCOMP	D37	eDP_RCOMP	R0302 1 1% 2 24.9Ohm	+VCCIO
48 DDI2_TXP3_HDMI_CLK	E37	DDI2_TXP[3]					
48 DDI2_TXN3_HDMI_CLK	E36	DDI2_TXN[3]					
	F26	DDI2_AUXP					
	E26	DDI2_AUXN					
	C34	DDI3_TXP[0]					
	D34	DDI3_TXN[0]					
	B36	DDI3_TXP[1]					
	B34	DDI3_TXN[1]					
	F33	DDI3_TXP[2]					
	E33	DDI3_TXN[2]					
	C33	DDI3_TXP[3]					
	B33	DDI3_TXN[3]					
	A27	DDI3_AUXP	PROC_AUDIO_CLK	G27	AUD_AZACPU_SCLK		20
	B27	DDI3_AUXN	PROC_AUDIO_SDI	G25	AUD_AZACPU_SDO		20
			PROC_AUDIO_SDO	G29	AUD_AZACPU_SDI		20

AUD_AZACPU_SDI_X 2 — R0303 200Ohm

GL502VD Add

GL502VD Add

eDP_RCOMP's trace length <100mils

GL502VD Add

R0303 Place Near CPU

Project Name: FX502VD			Rev: 2.0
Title : CPU_DMI,PEG,FDI,eDP,DDI			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang	
Date: Wednesday, February 15, 2017	Sheet 3	of 102	

Memory Channel A

U0301A — BGA1440

M_A_DQ[63:0]

M_A_DQ0	BR6	DDR0_DQ[0]
M_A_DQ1	BT6	DDR0_DQ[1]
M_A_DQ2	BP3	DDR0_DQ[2]
M_A_DQ3	BR3	DDR0_DQ[3]
M_A_DQ4	BN5	DDR0_DQ[4]
M_A_DQ5	BP6	DDR0_DQ[5]
M_A_DQ6	BP2	DDR0_DQ[6]
M_A_DQ7	BN3	DDR0_DQ[7]
M_A_DQ8	BL4	DDR0_DQ[8]
M_A_DQ9	BL5	DDR0_DQ[9]
M_A_DQ10	BL2	DDR0_DQ[10]
M_A_DQ11	BM1	DDR0_DQ[11]
M_A_DQ12	BK4	DDR0_DQ[12]
M_A_DQ13	BK5	DDR0_DQ[13]
M_A_DQ14	BK1	DDR0_DQ[14]
M_A_DQ15	BK2	DDR0_DQ[15]
M_A_DQ16	BG5	DDR0_DQ[16]/DDR0_DQ[32]
M_A_DQ17	BF4	DDR0_DQ[17]/DDR0_DQ[33]
M_A_DQ18	BF5	DDR0_DQ[18]/DDR0_DQ[34]
M_A_DQ19	BG2	DDR0_DQ[19]/DDR0_DQ[35]
M_A_DQ20	BG1	DDR0_DQ[20]/DDR0_DQ[36]
M_A_DQ21	BF1	DDR0_DQ[21]/DDR0_DQ[37]
M_A_DQ22	BF2	DDR0_DQ[22]/DDR0_DQ[38]
M_A_DQ23	BD2	DDR0_DQ[23]/DDR0_DQ[39]
M_A_DQ24	BD1	DDR0_DQ[24]/DDR0_DQ[40]
M_A_DQ25	BC4	DDR0_DQ[25]/DDR0_DQ[41]
M_A_DQ26	BC5	DDR0_DQ[26]/DDR0_DQ[42]
M_A_DQ27	BD5	DDR0_DQ[27]/DDR0_DQ[43]
M_A_DQ28	BD4	DDR0_DQ[28]/DDR0_DQ[44]
M_A_DQ29	BC1	DDR0_DQ[29]/DDR0_DQ[45]
M_A_DQ30	BC2	DDR0_DQ[30]/DDR0_DQ[46]
M_A_DQ31	AB1	DDR0_DQ[31]/DDR0_DQ[47]
M_A_DQ32	AB2	DDR0_DQ[32]/DDR1_DQ[0]
M_A_DQ33	AA4	DDR0_DQ[33]/DDR1_DQ[1]
M_A_DQ34	AA5	DDR0_DQ[34]/DDR1_DQ[2]
M_A_DQ35	AB5	DDR0_DQ[35]/DDR1_DQ[3]
M_A_DQ36	AB4	DDR0_DQ[36]/DDR1_DQ[4]
M_A_DQ37	AA2	DDR0_DQ[37]/DDR1_DQ[5]
M_A_DQ38	AA1	DDR0_DQ[38]/DDR1_DQ[6]
M_A_DQ39	V5	DDR0_DQ[39]/DDR1_DQ[7]
M_A_DQ40	V2	DDR0_DQ[40]/DDR1_DQ[8]
M_A_DQ41	U1	DDR0_DQ[41]/DDR1_DQ[9]
M_A_DQ42	U2	DDR0_DQ[42]/DDR1_DQ[10]
M_A_DQ43	V1	DDR0_DQ[43]/DDR1_DQ[11]
M_A_DQ44	V4	DDR0_DQ[44]/DDR1_DQ[12]
M_A_DQ45	U5	DDR0_DQ[45]/DDR1_DQ[13]
M_A_DQ46	U4	DDR0_DQ[46]/DDR1_DQ[14]
M_A_DQ47	R4	DDR0_DQ[47]/DDR1_DQ[15]
M_A_DQ48	P5	DDR0_DQ[48]/DDR1_DQ[32]
M_A_DQ49	R4	DDR0_DQ[49]/DDR1_DQ[33]
M_A_DQ50	P4	DDR0_DQ[50]/DDR1_DQ[34]
M_A_DQ51	R5	DDR0_DQ[51]/DDR1_DQ[35]
M_A_DQ52	P2	DDR0_DQ[52]/DDR1_DQ[36]
M_A_DQ53	R1	DDR0_DQ[53]/DDR1_DQ[37]
M_A_DQ54	P1	DDR0_DQ[54]/DDR1_DQ[38]
M_A_DQ55	M4	DDR0_DQ[55]/DDR1_DQ[39]
M_A_DQ56	M1	DDR0_DQ[56]/DDR1_DQ[40]
M_A_DQ57	L4	DDR0_DQ[57]/DDR1_DQ[41]
M_A_DQ58	L2	DDR0_DQ[58]/DDR1_DQ[42]
M_A_DQ59	M5	DDR0_DQ[59]/DDR1_DQ[43]
M_A_DQ60	M2	DDR0_DQ[60]/DDR1_DQ[44]
M_A_DQ61	L5	DDR0_DQ[61]/DDR1_DQ[45]
M_A_DQ62	L1	DDR0_DQ[62]/DDR1_DQ[46]
M_A_DQ63		DDR0_DQ[63]/DDR1_DQ[47]

BA2	DDR0_ECC[0]	DDR0_DQSP[0] / DDR0_DQSP[4]
BA1	DDR0_ECC[1]	DDR0_DQSN[0] / DDR0_DQSN[4]
AY4	DDR0_ECC[2]	DDR0_DQSP[1] / DDR0_DQSP[5]
AY5	DDR0_ECC[3]	DDR0_DQSN[1] / DDR0_DQSN[5]
BA5	DDR0_ECC[4]	DDR0_DQSP[2] / DDR0_DQSP[6]
BA4	DDR0_ECC[5]	DDR0_DQSN[2] / DDR0_DQSN[6]
AY1	DDR0_ECC[6]	DDR0_DQSP[3] / DDR0_DQSP[7]
AY2	DDR0_ECC[7]	DDR0_DQSN[3] / DDR0_DQSN[7]

AG1	DDR0_CKP[0]	M_A_DIM0_CK_DDR0_DP
AG2	DDR0_CKN[0]	M_A_DIM0_CK_DDR0_DN
AK2	DDR0_CKP[1]	M_A_DIM0_CK_DDR1_DN — T0401 @
AL3	DDR0_CKN[1]	M_A_DIM0_CK_DDR1_DP — T0402 @
AK3	DDR0_CLKP[2]	
AL2	DDR0_CLKN[2]	
AL1	DDR0_CLKP[3]	
	DDR0_CLKN[3]	
AT1	DDR0_CKE[0]	M_A_DIM0_CKE0
AT2	DDR0_CKE[1]	
AT3	DDR0_CKE[2]	M_A_DIM0_CKE1 — T0403 @
AT5	DDR0_CKE[3]	
AD5	DDR0_CS#[0]	M_A_DIM0_CS0#
AE2	DDR0_CS#[1]	
AD2	DDR0_CS#[2]	M_A_DIM0_CS1# — T0408 @
AE5	DDR0_CS#[3]	
AD3	DDR0_ODT[0]	M_A_DIM0_ODT0
AE4	DDR0_ODT[1]	
AE1	DDR0_ODT[2]	M_A_DIM0_ODT1_2DIE — T0409 @
AD4	DDR0_ODT[3]	

AH5	DDR0_CAB[4]/DDR0_BA[0]	M_A_BA0 13,14
AH1	DDR0_CAB[6]/DDR0_BA[1]	M_A_BA1 13,14
AU1	DDR0_CAA[5]/DDR0_BG[0]	M_A_BG0 13,14
		M_A_A[16:14] 13,14
AH4	DDR0_CAB[3]/DDR0_MA[16]	M_A_A16
AG4	DDR0_CAB[2]/DDR0_MA[14]	M_A_A14
AD1	DDR0_CAB[1]/DDR0_MA[15]	M_A_A15
		M_A_A[13:0] 13,14
AH3	DDR0_CAB[9]/DDR0_MA[0]	M_A_A0
AP4	DDR0_CAB[8]/DDR0_MA[1]	M_A_A1
AN4	DDR0_CAB[5]/DDR0_MA[2]	M_A_A2
AP5	DDR0_MA[3]	M_A_A3
AP2	DDR0_MA[4]	M_A_A4
AP1	DDR0_CAA[0]/DDR0_MA[5]	M_A_A5
AP3	DDR0_CAA[2]/DDR0_MA[6]	M_A_A6
AN1	DDR0_CAA[4]/DDR0_MA[7]	M_A_A7
AN3	DDR0_CAA[3]/DDR0_MA[8]	M_A_A8
AT4	DDR0_CAA[1]/DDR0_MA[9]	M_A_A9
AH2	DDR0_CAB[7]/DDR0_MA[10]	M_A_A10
AN2	DDR0_CAA[7]/DDR0_MA[11]	M_A_A11
AU4	DDR0_CAA[6]/DDR0_MA[12]	M_A_A12
AE3	DDR0_CAB[0]/DDR0_MA[13]	M_A_A13
AU2	DDR0_CAA[9]/DDR0_BG[1]	M_A_BG1 13,14
AU3	DDR0_CAA[8]/DDR0_ACT#	M_A_ACT# 13,14
AG3	DDR0_PAR	M_A_PARITY 13,14
AU5	DDR0_ALERT#	M_A_ALERT# 13,14

BR5	DDR0_DQSN[0]	M_A_DQS#[3:0] 14
BL3	DDR0_DQSN[1]	M_A_DQS#0
BG3	DDR0_DQSN[2]/DDR0_DQSN[4]	M_A_DQS#1
BD3	DDR0_DQSN[3]/DDR0_DQSN[5]	M_A_DQS#2
AB3	DDR0_DQSP[4]/DDR1_DQSP[0]	M_A_DQS#3
V3	DDR0_DQSP[5]/DDR1_DQSP[1]	M_A_DQS[7:4] 14
R3	DDR0_DQSP[6]/DDR1_DQSP[4]	M_A_DQS4
M3	DDR0_DQSP[7]/DDR1_DQSP[5]	M_A_DQS5
		M_A_DQS6
BP5	DDR0_DQSP[0]	M_A_DQS7
BK3	DDR0_DQSP[1]	M_A_DQS[3:0] 14
BF3	DDR0_DQSP[2]/DDR0_DQSP[4]	M_A_DQS0
BC3	DDR0_DQSP[3]/DDR0_DQSP[5]	M_A_DQS1
AA3	DDR0_DQSN[4]/DDR1_DQSN[0]	M_A_DQS2
U3	DDR0_DQSN[5]/DDR1_DQSN[1]	M_A_DQS3
P3	DDR0_DQSN[6]/DDR1_DQSN[4]	M_A_DQS[7:4] 14
L3	DDR0_DQSN[7]/DDR1_DQSN[5]	M_A_DQS4
		M_A_DQS5
AY3	DDR0_DQSP[8]	M_A_DQS6
BA3	DDR0_DQSN[8]	M_A_DQS7

DDR CHANNEL A

BGA1140

Memory Channel B

U0301B — BGA1440

M_B_DQ[63:0]

M_B_DQ0	BT11	DDR1_DQ[0]/DDR0_DQ[16]
M_B_DQ1	BR11	DDR1_DQ[1]/DDR0_DQ[17]
M_B_DQ2	BT8	DDR1_DQ[2]/DDR0_DQ[18]
M_B_DQ3	BR8	DDR1_DQ[3]/DDR0_DQ[19]
M_B_DQ4	BP11	DDR1_DQ[4]/DDR0_DQ[20]
M_B_DQ5	BN11	DDR1_DQ[5]/DDR0_DQ[21]
M_B_DQ6	BP8	DDR1_DQ[6]/DDR0_DQ[22]
M_B_DQ7	BN8	DDR1_DQ[7]/DDR0_DQ[23]
M_B_DQ8	BL12	DDR1_DQ[8]/DDR0_DQ[24]
M_B_DQ9	BL11	DDR1_DQ[9]/DDR0_DQ[25]
M_B_DQ10	BL8	DDR1_DQ[10]/DDR0_DQ[26]
M_B_DQ11	BJ8	DDR1_DQ[11]/DDR0_DQ[27]
M_B_DQ12	BJ11	DDR1_DQ[12]/DDR0_DQ[28]
M_B_DQ13	BJ10	DDR1_DQ[13]/DDR0_DQ[29]
M_B_DQ14	BL7	DDR1_DQ[14]/DDR0_DQ[30]
M_B_DQ15	BJ7	DDR1_DQ[15]/DDR0_DQ[31]
M_B_DQ16	BG11	DDR1_DQ[16]/DDR0_DQ[48]
M_B_DQ17	BG10	DDR1_DQ[17]/DDR0_DQ[49]
M_B_DQ18	BG8	DDR1_DQ[18]/DDR0_DQ[50]
M_B_DQ19	BF8	DDR1_DQ[19]/DDR0_DQ[51]
M_B_DQ20	BF11	DDR1_DQ[20]/DDR0_DQ[52]
M_B_DQ21	BF10	DDR1_DQ[21]/DDR0_DQ[53]
M_B_DQ22	BG7	DDR1_DQ[22]/DDR0_DQ[54]
M_B_DQ23	BF7	DDR1_DQ[23]/DDR0_DQ[55]
M_B_DQ24	BB11	DDR1_DQ[24]/DDR0_DQ[56]
M_B_DQ25	BC11	DDR1_DQ[25]/DDR0_DQ[57]
M_B_DQ26	BB8	DDR1_DQ[26]/DDR0_DQ[58]
M_B_DQ27	BC8	DDR1_DQ[27]/DDR0_DQ[59]
M_B_DQ28	BC10	DDR1_DQ[28]/DDR0_DQ[60]
M_B_DQ29	BB10	DDR1_DQ[29]/DDR0_DQ[61]
M_B_DQ30	BC7	DDR1_DQ[30]/DDR0_DQ[62]
M_B_DQ31	BB7	DDR1_DQ[31]/DDR0_DQ[63]
M_B_DQ32	AA11	DDR1_DQ[32]/DDR1_DQ[16]
M_B_DQ33	AA10	DDR1_DQ[33]/DDR1_DQ[17]
M_B_DQ34	AC11	DDR1_DQ[34]/DDR1_DQ[18]
M_B_DQ35	AC10	DDR1_DQ[35]/DDR1_DQ[19]
M_B_DQ36	AA7	DDR1_DQ[36]/DDR1_DQ[20]
M_B_DQ37	AA8	DDR1_DQ[37]/DDR1_DQ[21]
M_B_DQ38	AC8	DDR1_DQ[38]/DDR1_DQ[22]
M_B_DQ39	AC7	DDR1_DQ[39]/DDR1_DQ[23]
M_B_DQ40	W8	DDR1_DQ[40]/DDR1_DQ[24]
M_B_DQ41	W7	DDR1_DQ[41]/DDR1_DQ[25]
M_B_DQ42	V10	DDR1_DQ[42]/DDR1_DQ[26]
M_B_DQ43	V11	DDR1_DQ[43]/DDR1_DQ[27]
M_B_DQ44	W11	DDR1_DQ[44]/DDR1_DQ[28]
M_B_DQ45	W10	DDR1_DQ[45]/DDR1_DQ[29]
M_B_DQ46	V7	DDR1_DQ[46]/DDR1_DQ[30]
M_B_DQ47	V8	DDR1_DQ[47]/DDR1_DQ[31]
M_B_DQ48	R11	DDR1_DQ[48]
M_B_DQ49	P11	DDR1_DQ[49]
M_B_DQ50	P7	DDR1_DQ[50]
M_B_DQ51	R8	DDR1_DQ[51]
M_B_DQ52	R10	DDR1_DQ[52]
M_B_DQ53	P10	DDR1_DQ[53]
M_B_DQ54	R7	DDR1_DQ[54]
M_B_DQ55	P8	DDR1_DQ[55]
M_B_DQ56	L11	DDR1_DQ[56]
M_B_DQ57	M11	DDR1_DQ[57]
M_B_DQ58	L7	DDR1_DQ[58]
M_B_DQ59	M8	DDR1_DQ[59]
M_B_DQ60	L10	DDR1_DQ[60]
M_B_DQ61	M10	DDR1_DQ[61]
M_B_DQ62	M7	DDR1_DQ[62]
M_B_DQ63	L8	DDR1_DQ[63]

AW11	DDR1_ECC[0]	DDR1_DQSN(0)/DDR0_DQSN[2]
AY11	DDR1_ECC[1]	DDR1_DQSN(1)/DDR0_DQSN[3]
AY8	DDR1_ECC[2]	DDR1_DQSN(2)/DDR0_DQSN[6]
AW8	DDR1_ECC[3]	DDR1_DQSN(3)/DDR0_DQSN[7]
AY10	DDR1_ECC[4]	DDR1_DQSN(4)/DDR1_DQSN[2]
AW10	DDR1_ECC[5]	DDR1_DQSN(5)/DDR1_DQSN[3]
AY7	DDR1_ECC[6]	DDR1_DQSN[6]
AW7	DDR1_ECC[7]	DDR1_DQSN[7]

AM9	DDR1_CKP[0]	M_B_CLK_DDR0 16
AN9	DDR1_CKN[0]	M_B_CLK_DDR#0 16
AM8	DDR1_CKP[1]	M_B_CLK_DDR#1 16
AM7	DDR1_CKN[1]	M_B_CLK_DDR1 16
AM11	DDR1_CLKP[2]	
AM10	DDR1_CLKN[2]	
AJ10	DDR1_CLKP[3]	
AJ11	DDR1_CLKN[3]	
AT8	DDR1_CKE[0]	M_B_CKE0 16
AT10	DDR1_CKE[1]	M_B_CKE1 16
AT7	DDR1_CKE[2]	
AT11	DDR1_CKE[3]	
AF11	DDR1_CS#[0]	M_B_CS#0 16
AE7	DDR1_CS#[1]	M_B_CS#1 16
AF10	DDR1_CS#[2]	
AE10	DDR1_CS#[3]	
AF7	DDR1_ODT[0]	M_B_ODT0 16
AE8	DDR1_ODT[1]	M_B_ODT1 16
AE9	DDR1_ODT[2]	
AE11	DDR1_ODT[3]	

AH10	DDR1_CAB[3]/DDR1_MA[16]	M_B_RAS# 16
AH11	DDR1_CAB[2]/DDR1_MA[14]	M_B_WE# 16
AF8	DDR1_CAB[1]/DDR1_MA[15]	M_B_CAS# 16
AH8	DDR1_CAB[4]/DDR1_BA[0]	M_B_BA0 16
AH9	DDR1_CAB[6]/DDR1_BA[1]	M_B_BA1 16
AR9	DDR1_CAA[5]/DDR1_BG[0]	M_B_BG0 16
		M_B_A[13:0] 16
AJ9	DDR1_CAB[9]/DDR1_MA[0]	M_B_A0
AK6	DDR1_CAB[8]/DDR1_MA[1]	M_B_A1
AK5	DDR1_CAB[5]/DDR1_MA[2]	M_B_A2
AL5	DDR1_MA[3]	M_B_A3
AL6	DDR1_MA[4]	M_B_A4
AM6	DDR1_CAA[0]/DDR1_MA[5]	M_B_A5
AN7	DDR1_CAA[2]/DDR1_MA[6]	M_B_A6
AN10	DDR1_CAA[4]/DDR1_MA[7]	M_B_A7
AN8	DDR1_CAA[3]/DDR1_MA[8]	M_B_A8
AR11	DDR1_CAA[1]/DDR1_MA[9]	M_B_A9
AH7	DDR1_CAB[7]/DDR1_MA[10]	M_B_A10
AN11	DDR1_CAA[7]/DDR1_MA[11]	M_B_A11
AR10	DDR1_CAA[6]/DDR1_MA[12]	M_B_A12
AF9	DDR1_CAB[0]/DDR1_MA[13]	M_B_A13
AR7	DDR1_CAA[9]/DDR1_BG[1]	M_B_BG1 16
AT9	DDR1_CAA[8]/DDR1_ACT#	M_B_ACT# 16
AJ7	DDR1_PAR	M_B_PARITY 16
AR8	DDR1_ALERT#	M_B_ALERT# 16

BP9	M_B_DQS0	M_B_DQS[7:0] 16
BL9	M_B_DQS1	
BG9	M_B_DQS2	
BC9	M_B_DQS3	
AC9	M_B_DQS4	
W9	M_B_DQS5	
R9	M_B_DQS6	
M9	M_B_DQS7	
BR9	M_B_DQS0	M_B_DQS[7:0] 16
BJ9	M_B_DQS1	
BF9	M_B_DQS2	
BB9	M_B_DQS3	
AA9	M_B_DQS4	
V9	M_B_DQS5	
P9	M_B_DQS6	
L9	M_B_DQS7	

AJ9	DDR1_CKP[2]	
AH9	DDR1_CKN[2]	
AK9	DDR1_CKP[3]	
AJ9	DDR1_CKN[3]	

DDR CHANNEL B

BGA1140

DDR4 COMPENSATION SIGNALS

R0401	1	2	121Ohm	1%	G1
R0402			75Ohm	1%	H1
R0403	11	2	100Ohm	1%	J2

SM_RCOMP0 — SM_RCOMP1 — SM_RCOMP2

DDR_RCOMP[0] — DDR_RCOMP[1] — DDR_RCOMP[2]

DDR_VREF_CA — DDR0_VREF_DQ — DDR1_VREF_DQ

BN13 — BP13 — BR13

+V_DDR_CA_VREF 18

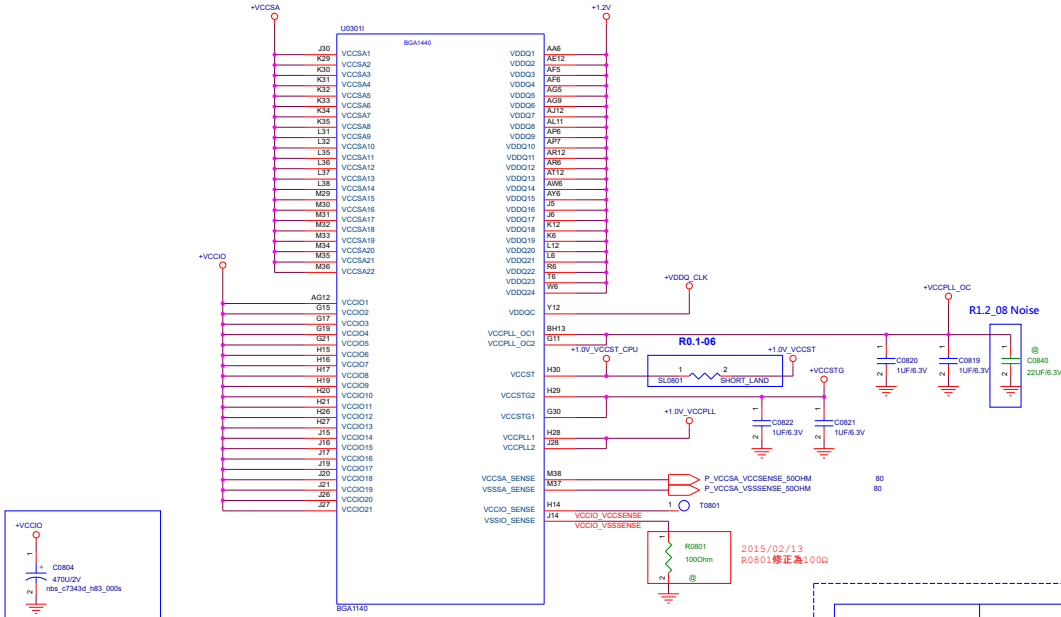
SB_DIMM_VREFDQ 18

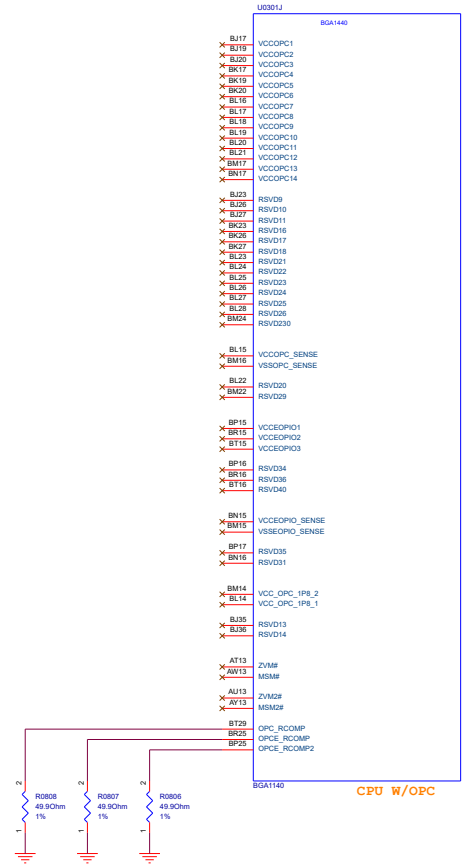
ASUS	Project Name: FX502VD		Rev: 2.0
Title : CPU_DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang	
Date: Wednesday, February 15, 2017	Sheet 4 of 102		

ASUS	Project Name: FX502VD	Rev: 2.0
Title : CPU XDP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang
Date: Wednesday, February 15, 2017	Sheet 7 of 102	

Main Board

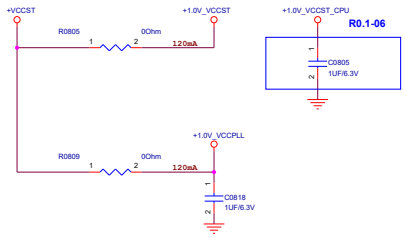
OPC Power Rails



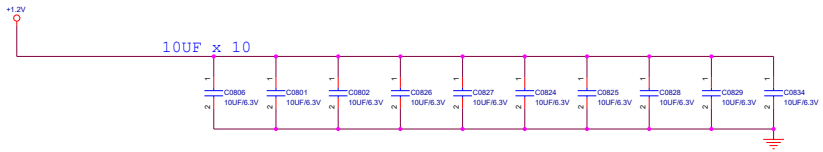


Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST
			+1.0V_VCCPLL
	+1.2V	+VDDQ_CPU	+VDDQ_CLK
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

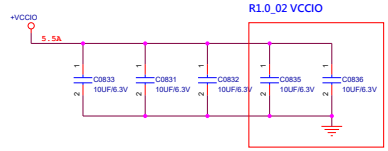
+1.0V_VCCST/+1.0V_VCCPLL DECAPS Place Back Side (TOP)



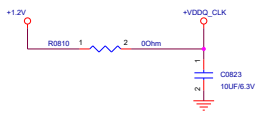
+VDDQ DECAPS Place Back Side (TOP)



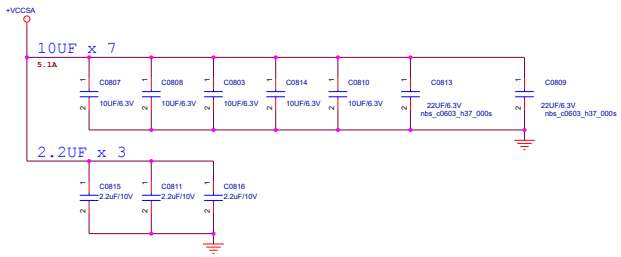
+VCCIO DECAPS Place Back Side (TOP)

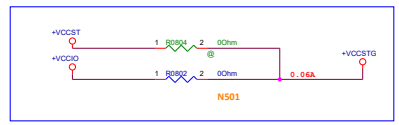


+VDDQ_CLK DECAPS Place Back Side (TOP)



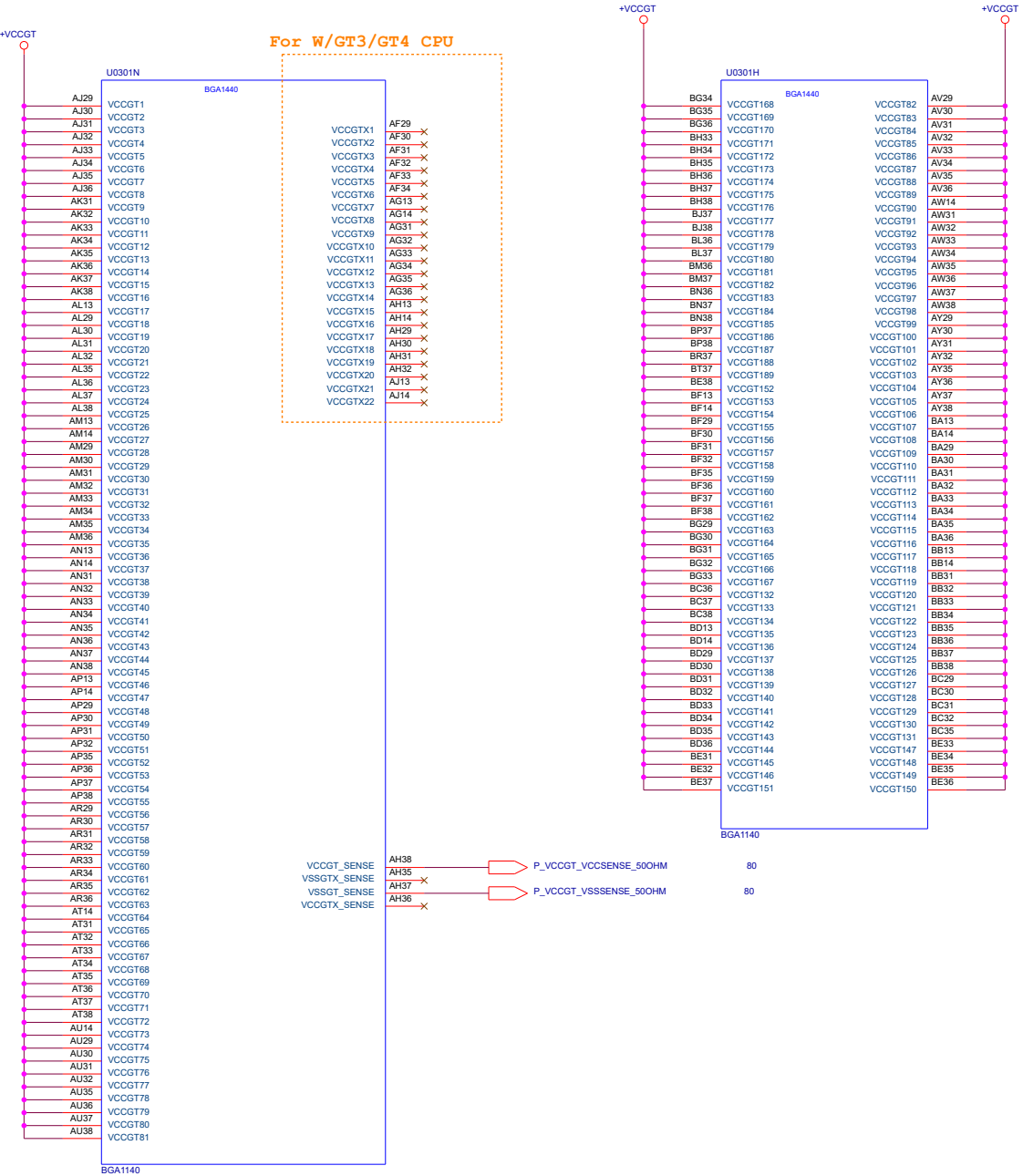
+VCCSA DECAPS Place Back Side (TOP)





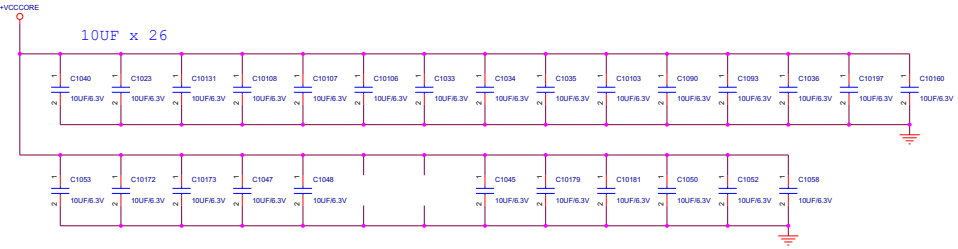
Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)

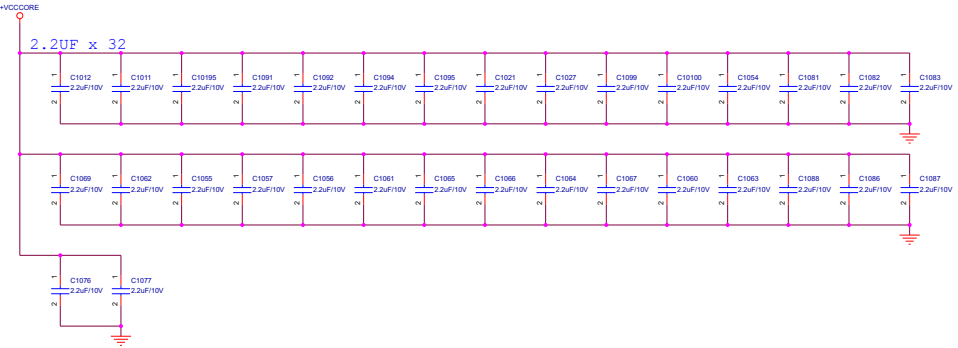
ASUS	Project Name: FX502VD	Rev: 2.0
Title : CPU_PWR		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang
Date: Wednesday, February 15, 2017	Sheet 8 of 102	



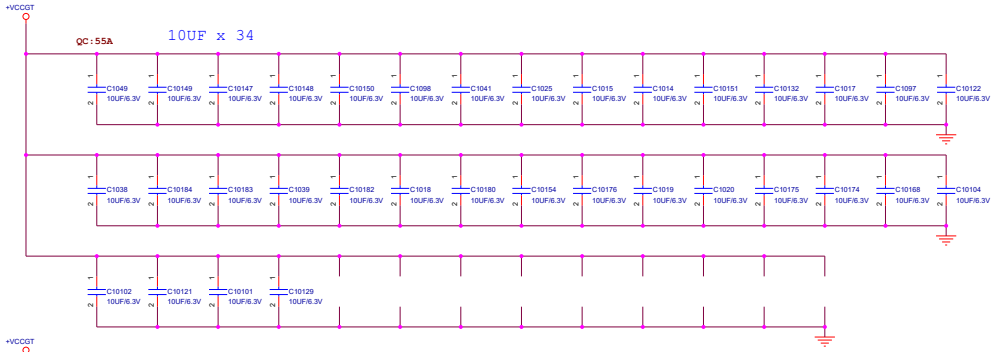
Project Name: FX502VD		Rev: 2.0
Title : NB_****		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang
Date: Wednesday, February 15, 2017	Sheet 9 of 102	

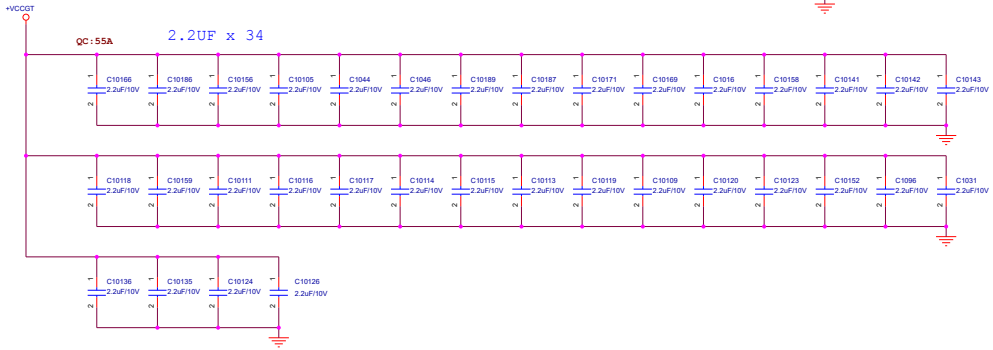
+VCCORE DECAPS Place Back Side (TOP)



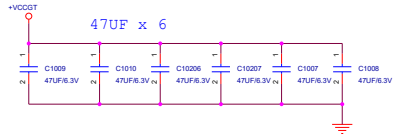


+VCCGT DECAPS Place Back Side (TOP)





+VCCGT DECAPS- Place close to the package(BOT)



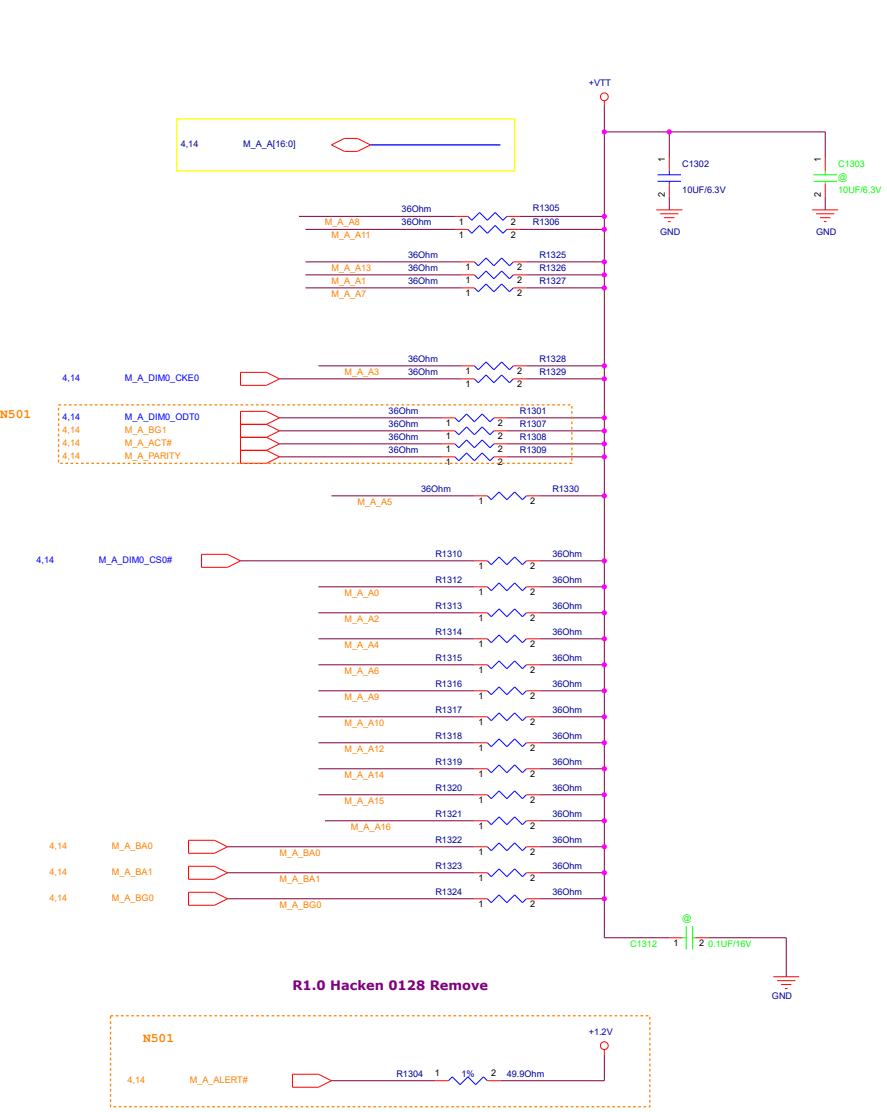
Backside cap	
Intel	GL502VD
8x22uF	43x10uF
35x10uF	
68x1uF	34x2.2uF
594uF	594uF

22uF移至PWR頁面P.81

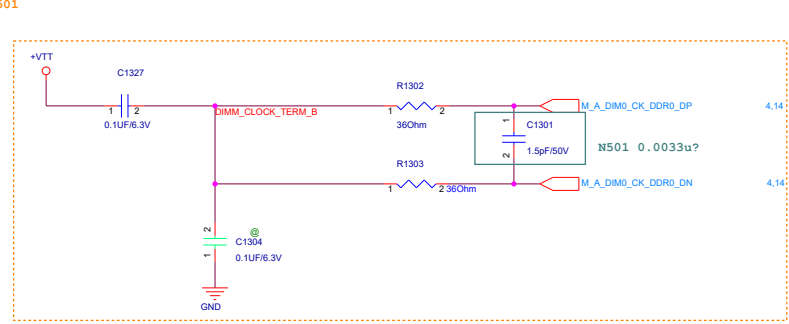
Project Name: GL502VD		Rev: 1.0
Title : 010_CPU_POWER_CAP		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 10 of 102	

Main Board

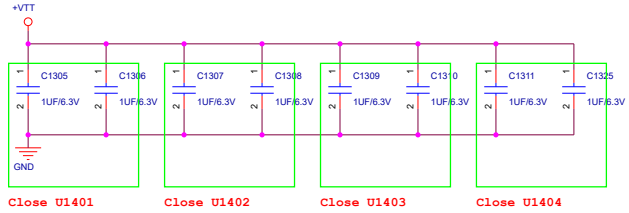
ASUS	Project Name: GL502VD	Rev: 1.0
Title : Intel Alpine-Ridge		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 11 of 102	

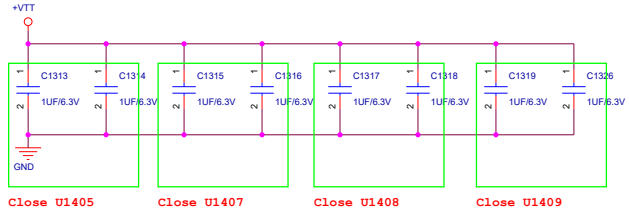


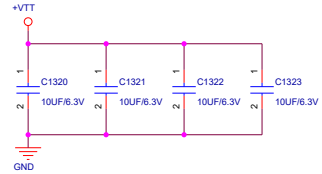
R1.0 Hacken 0128 Remove



3.Page13.Delete C1309 and Clock Pull up power change from +1.2V to +0.6V -20121212



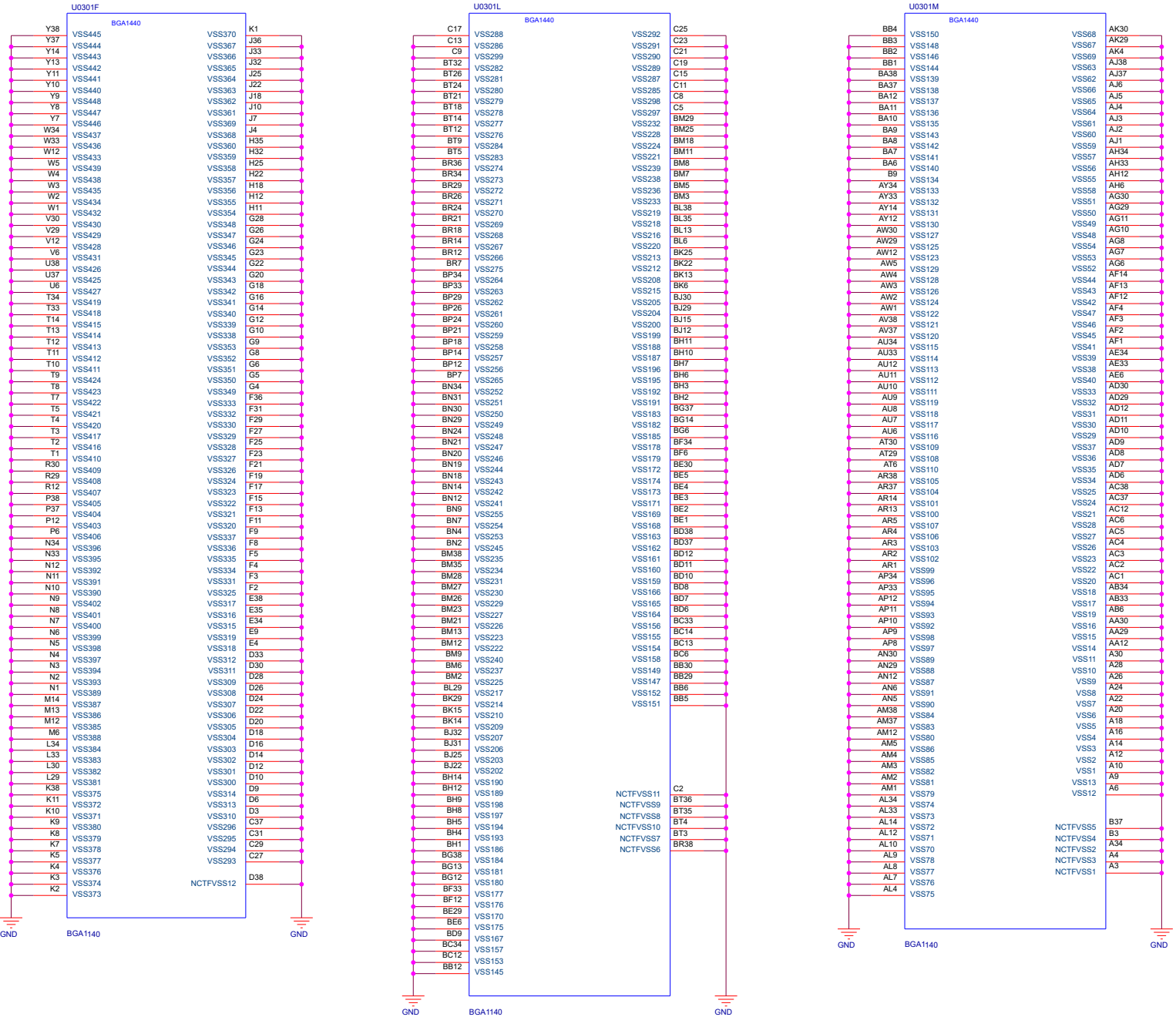




ASUSTeK COMPUTER INC.	Title : DDR4_TERMINATION	
	Engineer: Ben_Fang	
Size: Custom	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 13 of 102	

<Variant Name>

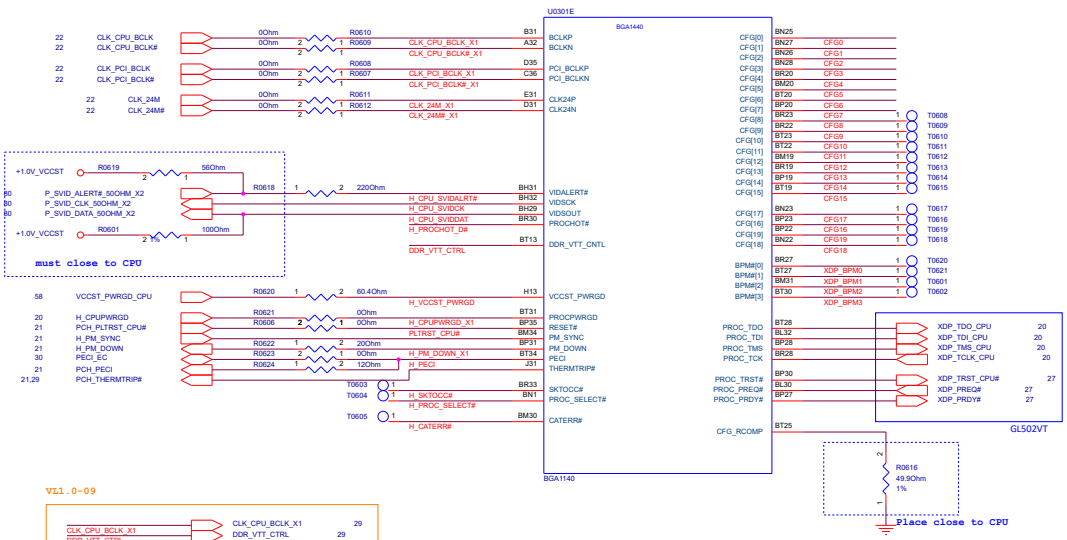
	Title : DDR4_ON-BOARD_A2	
ASUSTeK COMPUTER INC.	Engineer: Ben_Fang	
Size: Custom	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 15 of 102	

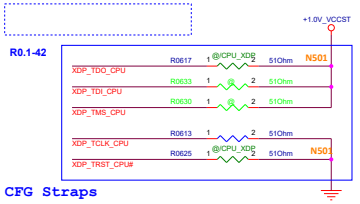


Main Board

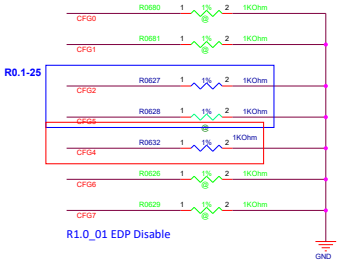
Project Name: FX502VD			Rev: 2.0
Title : CPU_CFG,RSVD,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang	
Date: Wednesday, February 15, 2017		Sheet 5 of 102	

CFG





CFG Straps



CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

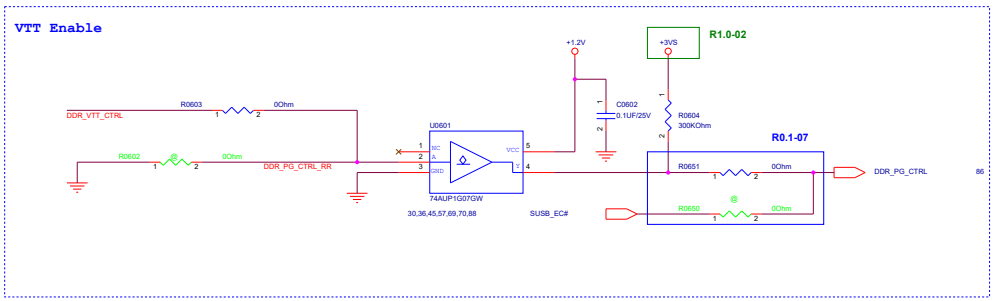
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

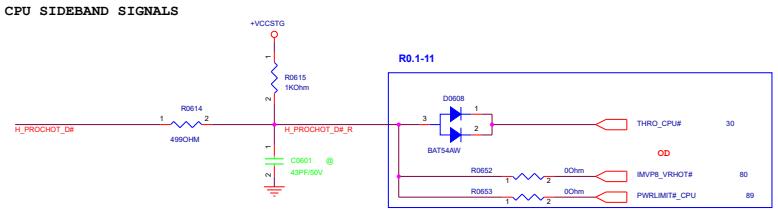
CFG[19:8] : Reserved Configuration Lanes

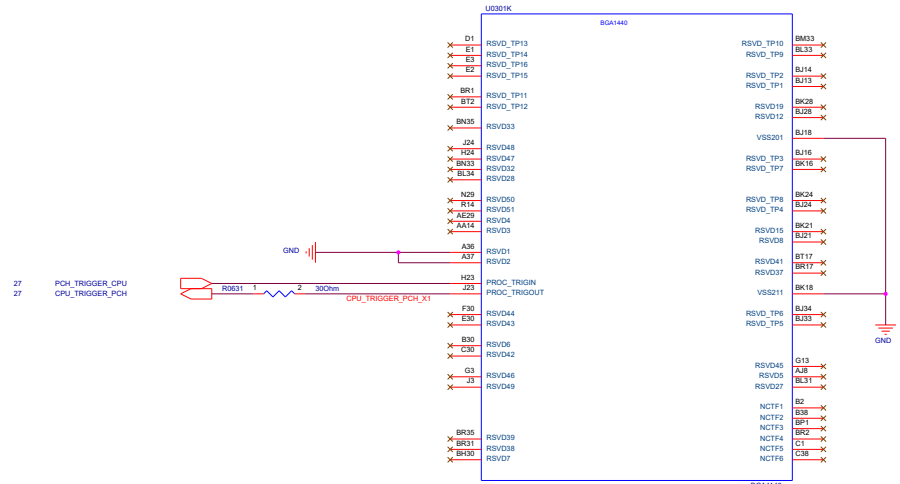
Reserved Configuration Lanes

Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 2014I209

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120







ASUS	Project Name: FX502VD		Rev: 2.0
Title : NB_****			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Wade_Huang	
Date: Wednesday, February 15, 2017	Sheet 6 of 102		

<Variant Name>

Title : NB_****

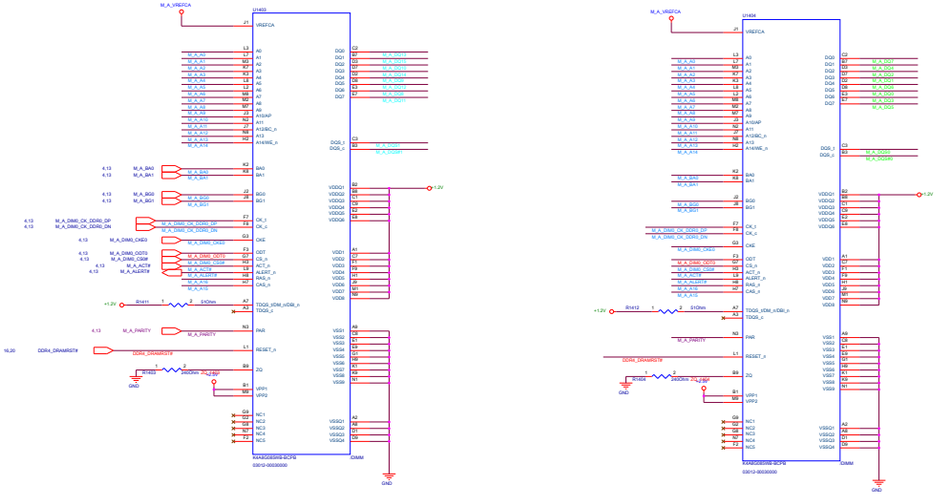
ASUSTeK COMPUTER INC. NB1

Engineer: Ben_Fang

Size	Project Name	Rev
A	GL502VD	1.0

Date:	Wednesday, February 15, 2017	Sheet	17	of	102

ASUS	Project Name: GL502VD	Rev: 1.0
Title :	TPS65982 & USB 3.1 Type-C	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 12 of 102	


M_A_VREFCA
U1403
U1404
U1401
U1402
U1405
U1407
U1408
U1409
VREFCA
DDR4_DRAMRST#
RANGO0S056-BCP8
03012-00030000
DIMM
GND
+1.2V
+2.5V
Close to 2C Pin 91/99
Close U1401
Close U1402
Close U1403
Close U1404
Close U1405
Close U1407
Close U1408
Close U1409
Close U1401~U1404 pin J1
Close U1405~U1409 pin J1
DIM Thermal Sensor
SMB1_CLK_S
SMB1_DAT_S
Near Top memory IC
Set to 90℃, BIOS set to 85 degree
Close to 2C Pin 90
Close to 2C Pin 98
Top Placement of VREF
M_A_VREFCA
C1401
C1402
C1403
C1404
C1405
C1406
C1407
C1408
C1409
C1410
C1411
C1412
C1413
C1414
C1415
C1416
C1417
C1418
C1419
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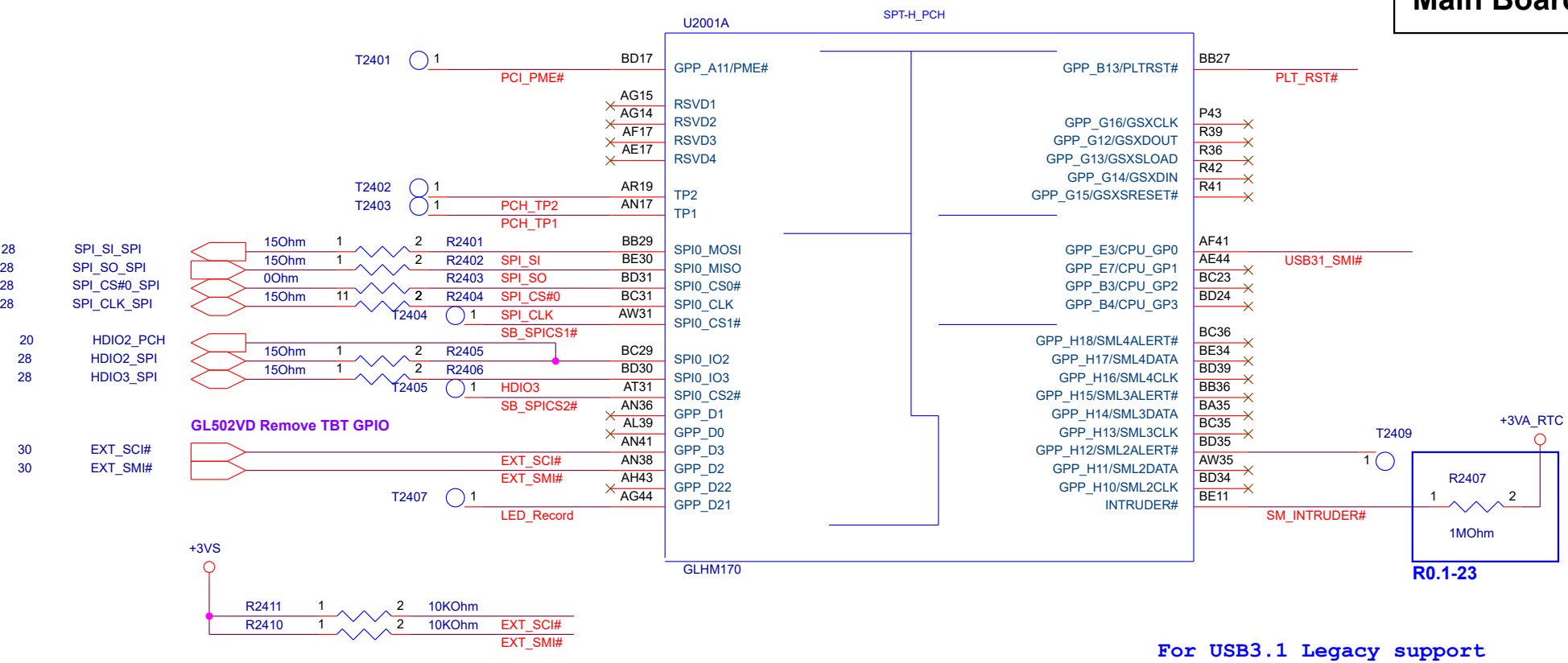
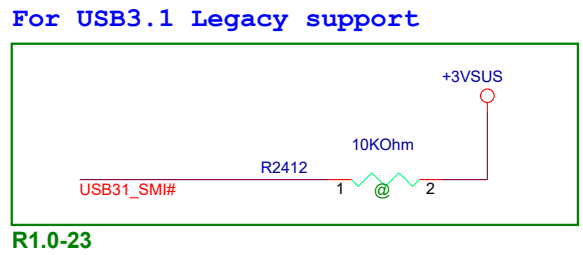
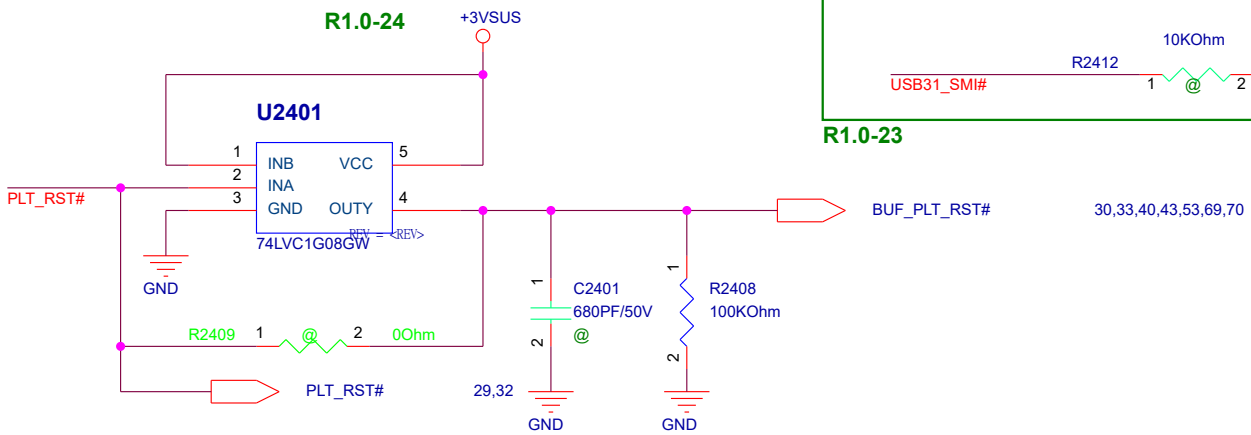
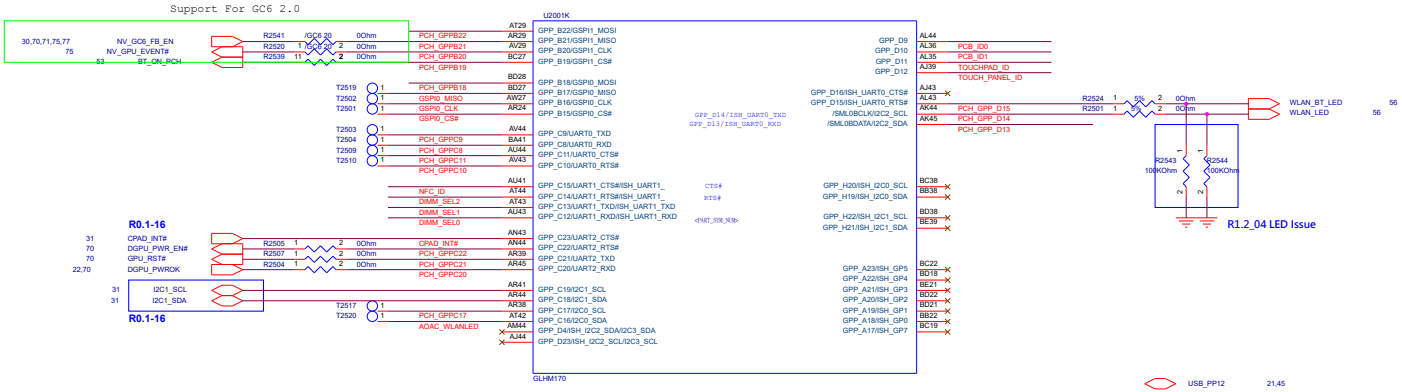
C1468
C1469
C1470
C1471
C1472
C1473
C1474
C1475
C1476
CE1401
CE1402
R1401
R1402
R1403
R1404
R1405
R1406
R1407
R1408
R1409
R1410
R1411
R1412
R1413
R1414
R1415
R1416
R1417
R1418
R1419
R1420
0.1UF/16V
10UF/6.3V
0.047UF/6.3V
220UF/20V
10PF/50V
240Ohm 1%
34Ohm 1%
51Ohm
1K
7.5K
4.7K
M_A_DQ[63:0]
M_A_DQS[7:0]
M_A_DQS#[7:0]
M_A_DM[7:0]
M_A_A[16:14]
M_A_A[13:0]
M_A_BA[1:0]
M_A_BG[1:0]
M_A_CKE[1:0]
M_A_ODT[1:0]
M_A_CS#[1:0]
M_A_ACT#
M_A_ALERT#
M_A_PARITY
M_A_RESET#
M_A_CLK_DDR[3:0]
M_A_CLK#_DDR[3:0]
SMB_CLK
SMB_DAT
ALERT#
PM_EXTTS#0
16,30
4,13
16,20
<Variant Name>
Title : DDR4_ON-BOARD_A1
Engineer: Ben_Fang
Size: Custom
Project Name: GL502VD
Rev: 1.0
Date: Wednesday, February 15, 2017
Sheet 13 of 100

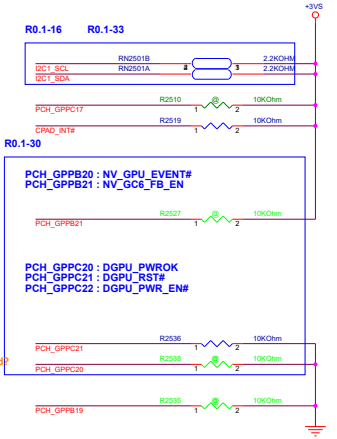


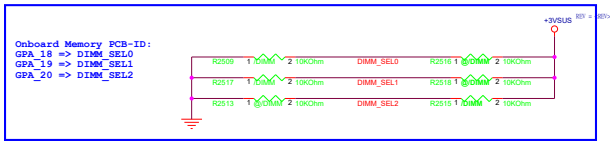




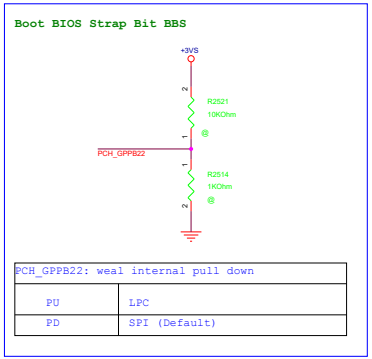
Project Name: GL502VD		Rev: 1.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 24 of 102	

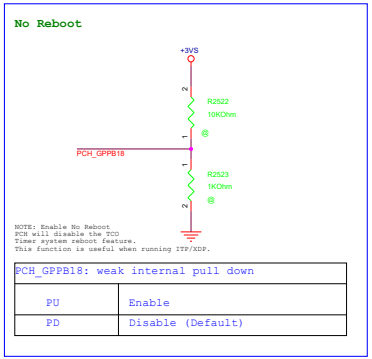


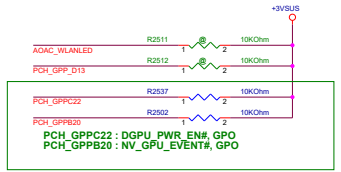


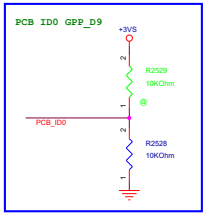


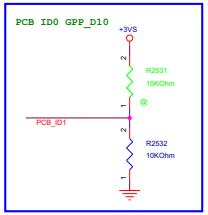
	MIcron (8Gb) 03012-00030100 DDR4 2400 1024M*8 1.2V MT40A1G8SNW-083E:A	Hynix (8Gb) 03012-00030400 DDR4 2400 1024M*8 1.2V H5AN8G8NAFR-UHC	Samsung (4Gb) 03012-00010200 DDR4 2133 512M*8 1.2V K4A4G085WE-BCPB	MIcron (4Gb) 03012-00010300 DDR4 2400 512M*8 1.2V MT40A512M8RH-083E:B
DIMM_SEL0	L	L	L	H
DIMM_SEL1	L	L	H	L
DIMM_SEL2	L	H	L	L

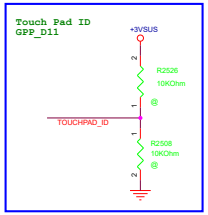


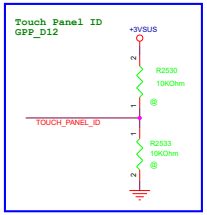


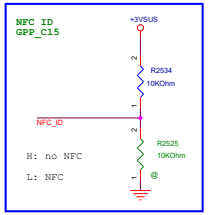




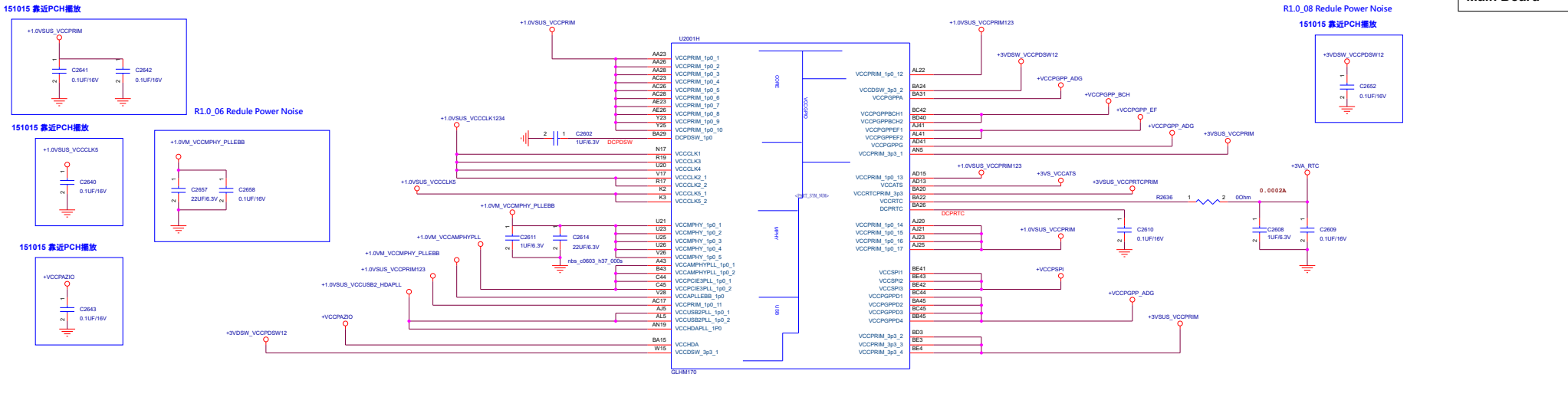


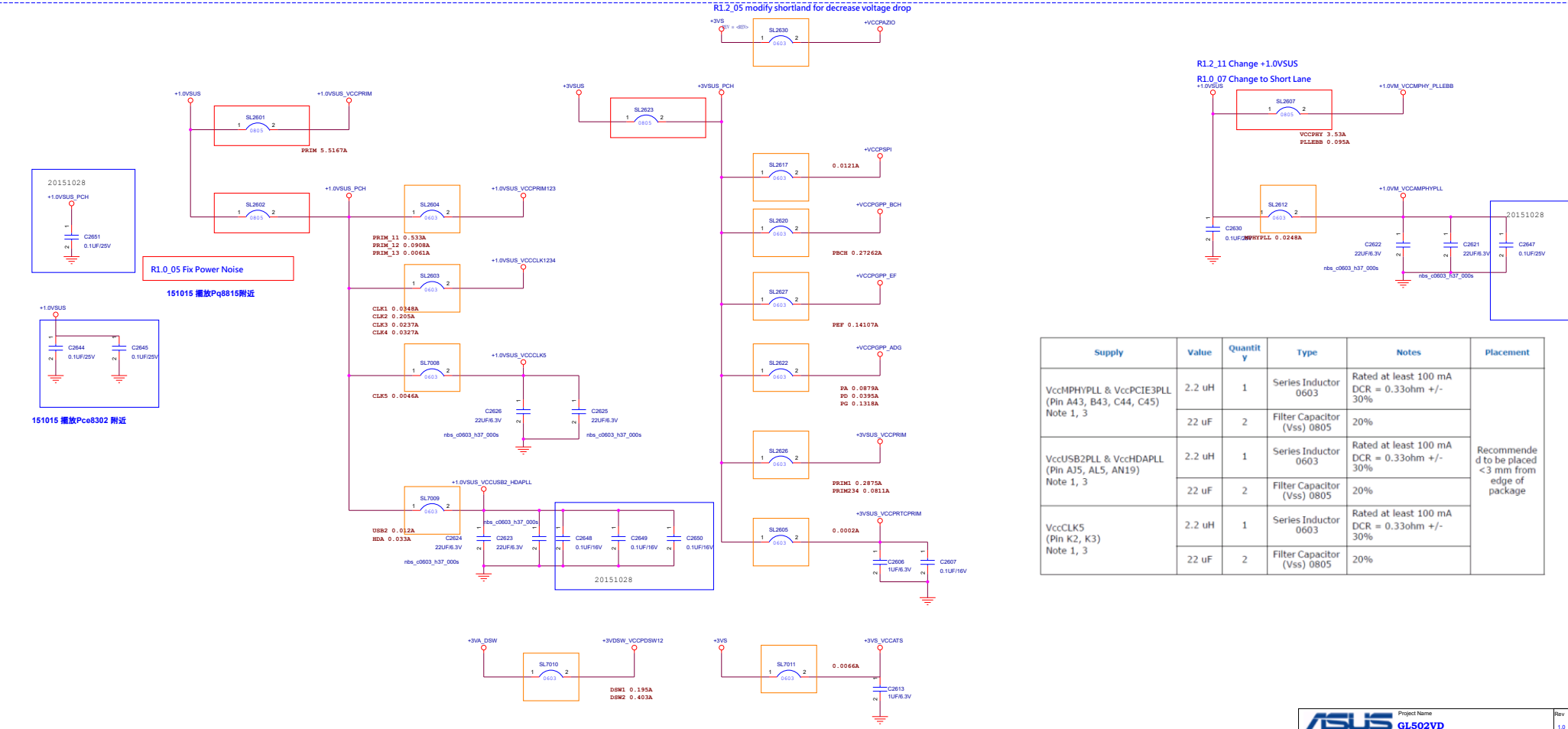






Project Name	GL502VD
Rev	1.0
Title :	PCH-CPT(6)_GPIO,MISC
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	Ben_Fang
Date:	Wednesday, February 15, 2017
Sheet	25 of 102

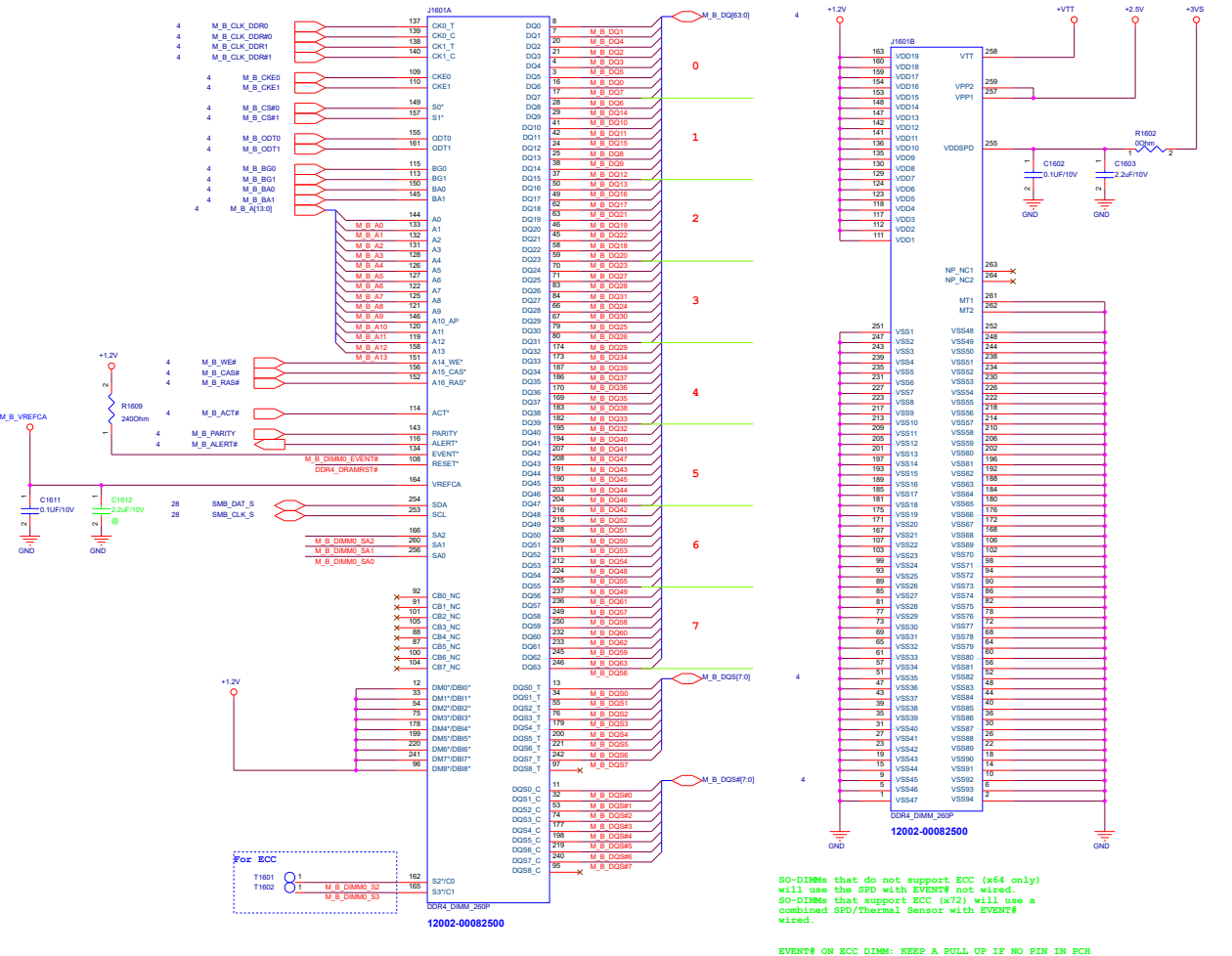




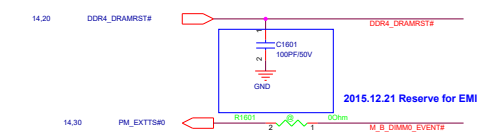
Supply	Value	Quantity	Type	Notes	Placement
VccMPHYPLL & VccPCIE3PLL (Pin A43, B43, C44, C45) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	Recommended to be placed <3 mm from edge of package
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccUSB2PLL & VccHDAPLL (Pin AJ5, AL5, AN19) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccCLK5 (Pin K2, K3) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	

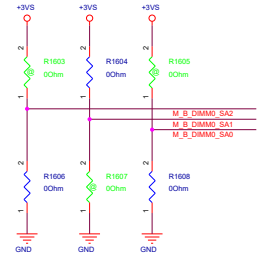
ASUS	Project Name: GL502VD		Rev: 1.0
Title :	PCH-CPT(7)_POWER,GND		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 26 of 102		

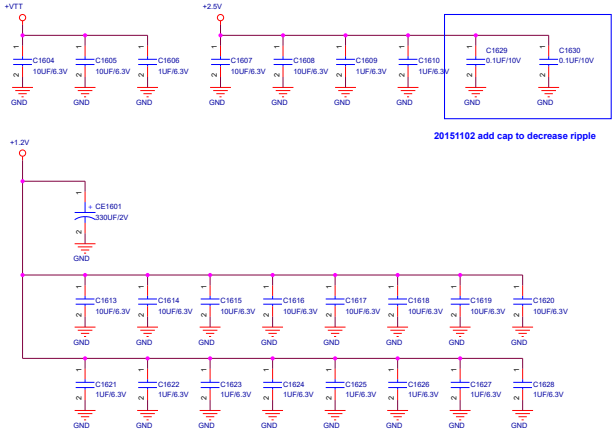
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)



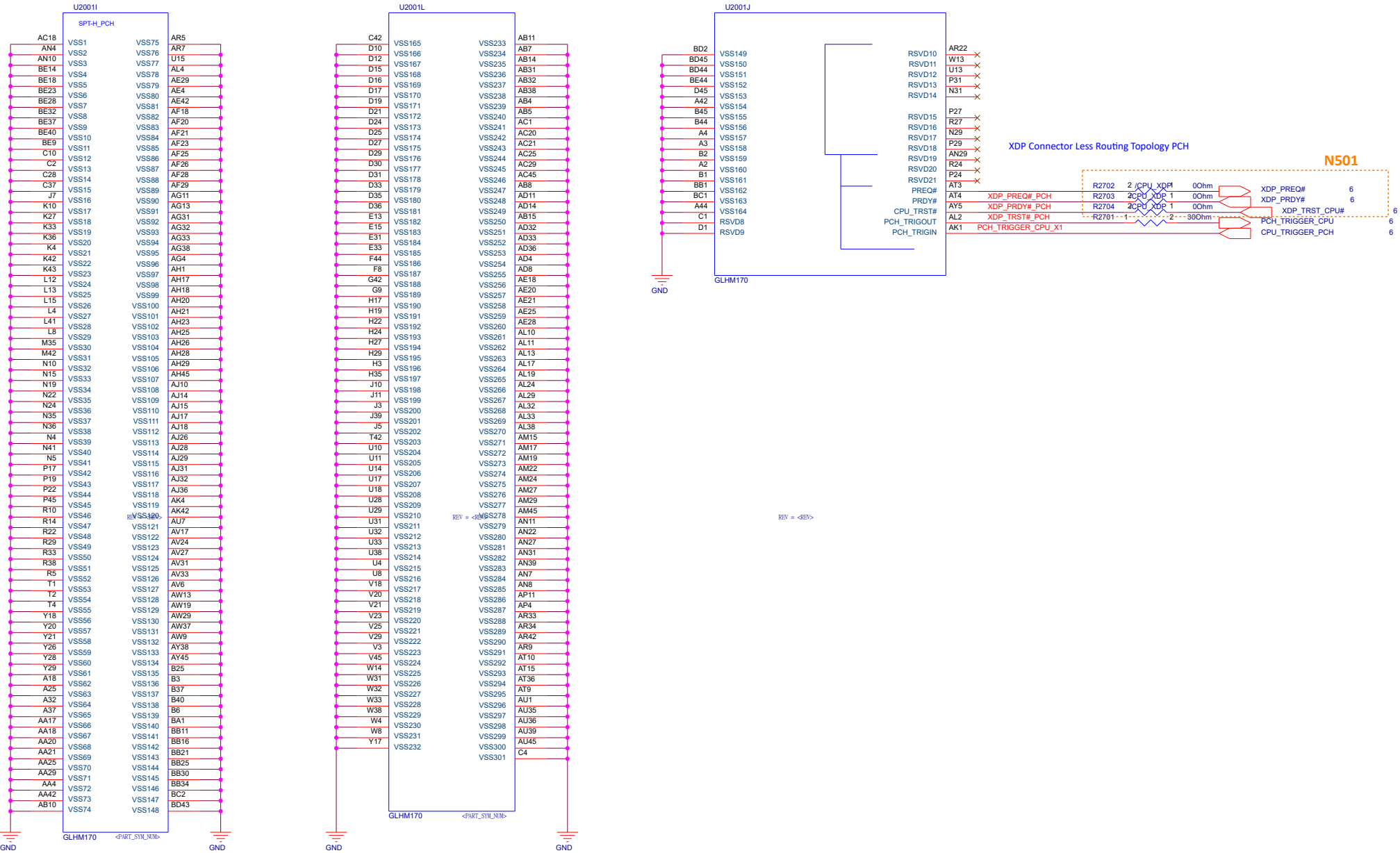
Main Board





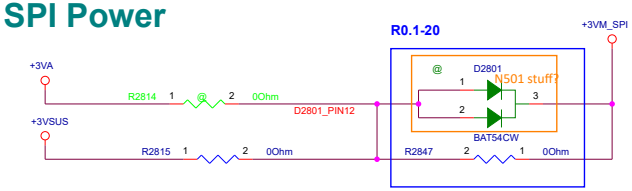


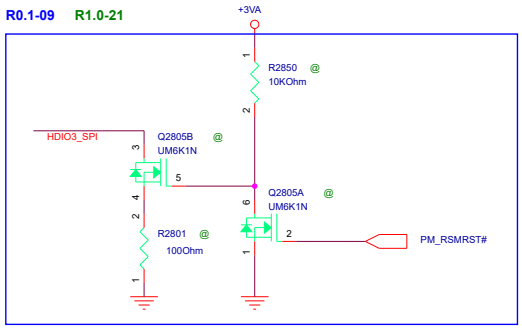
Project Name	GL502VD	Rev 1.0
Title :	DIM_DDR4 SO-DIMM B1	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 16 of 102	



Project Name: GL502VD		Rev: 1.0
Title : PCH-CPT(8)_POWER,GND		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 27 of 102	

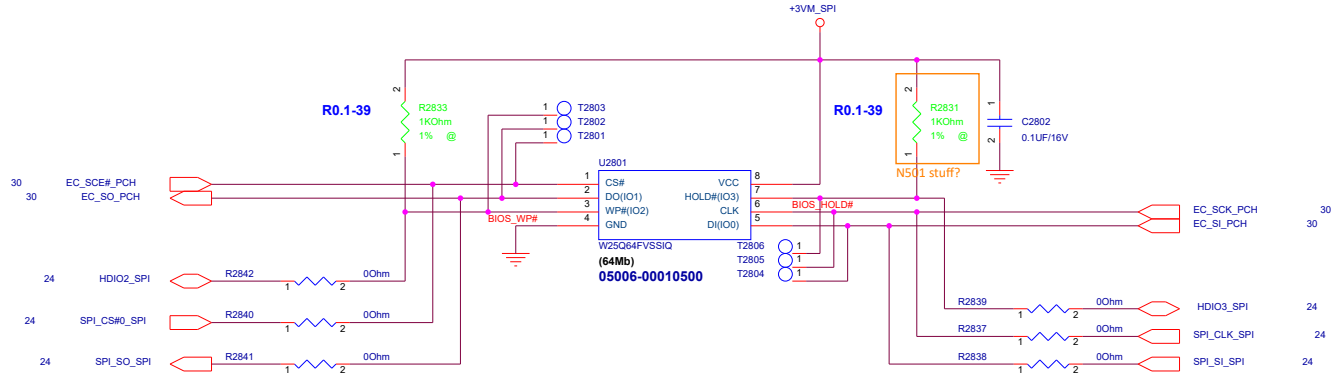
SPI Power



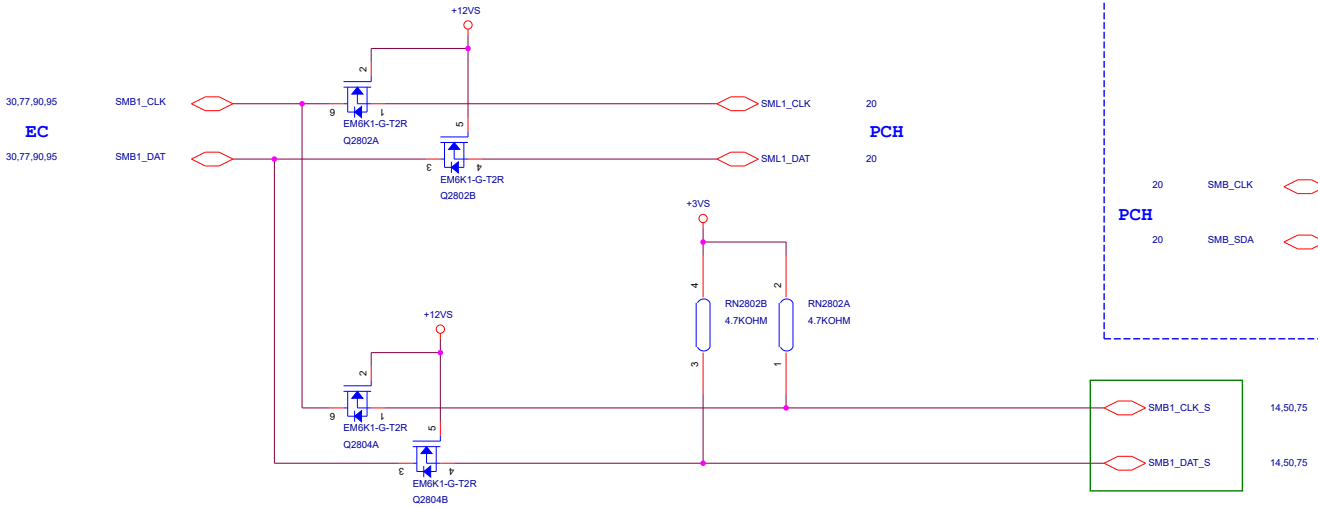


1st SPI ROM

Main: 05006-00010500 (fixed quad bit)



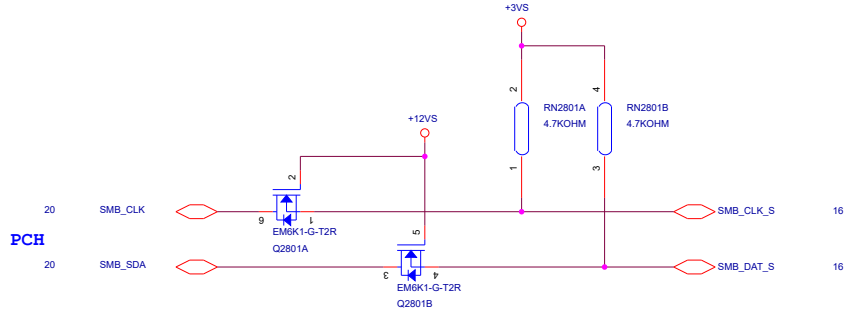
System Management Interface



R0.1-13 R1.0-01

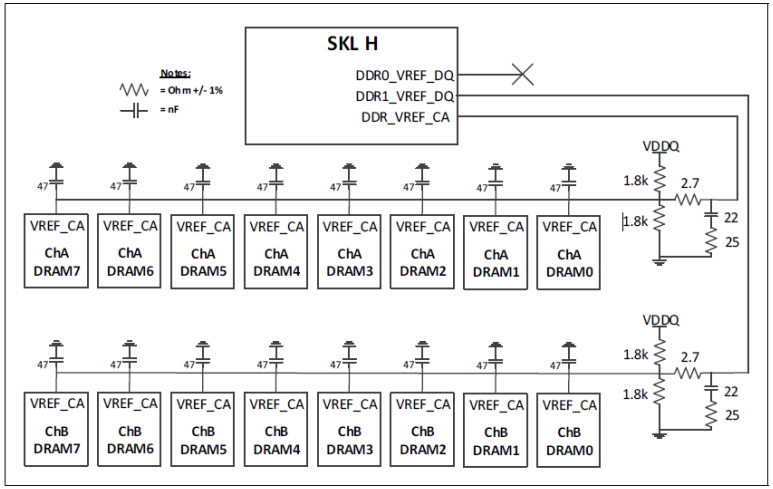
CPU,VGA Thermal Sensor
Power Thermal Sensor

SMBus Interface

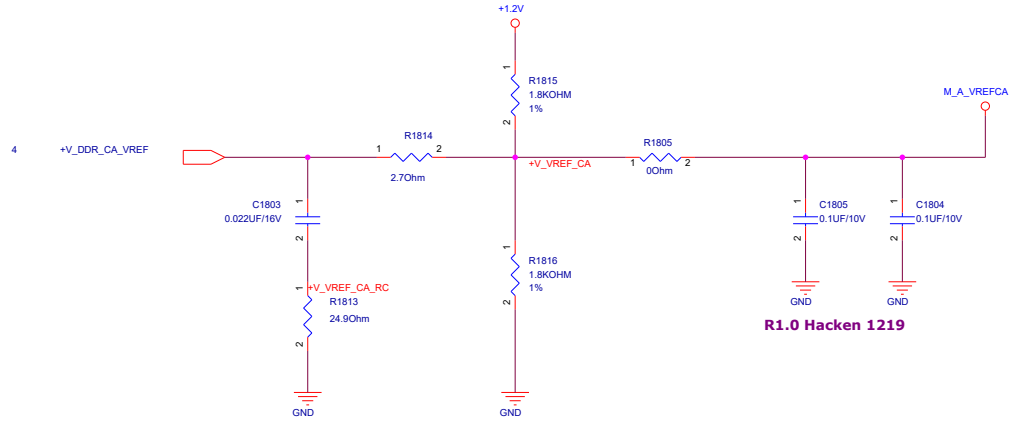


Project Name: GL502VD			Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 28 of 102		

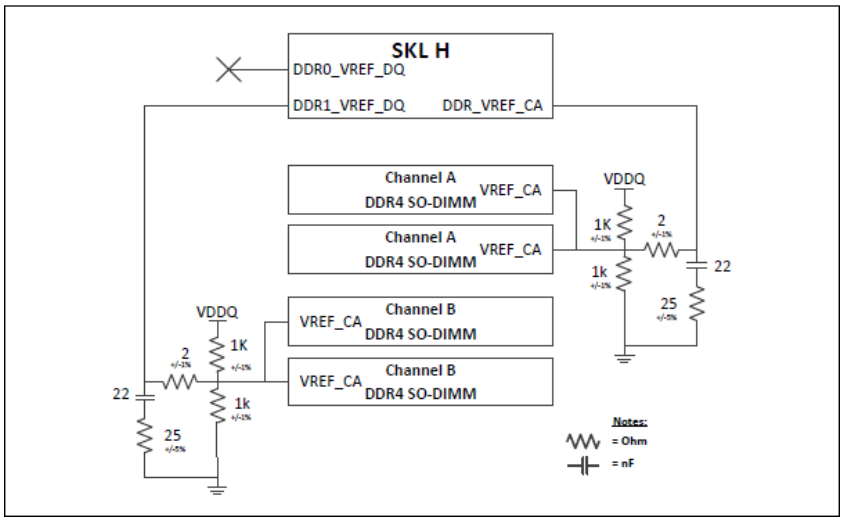
Figure 4-27. SKL H DDR4/DDR4-RS x8 Memory Down V_{REF-CA} Overview



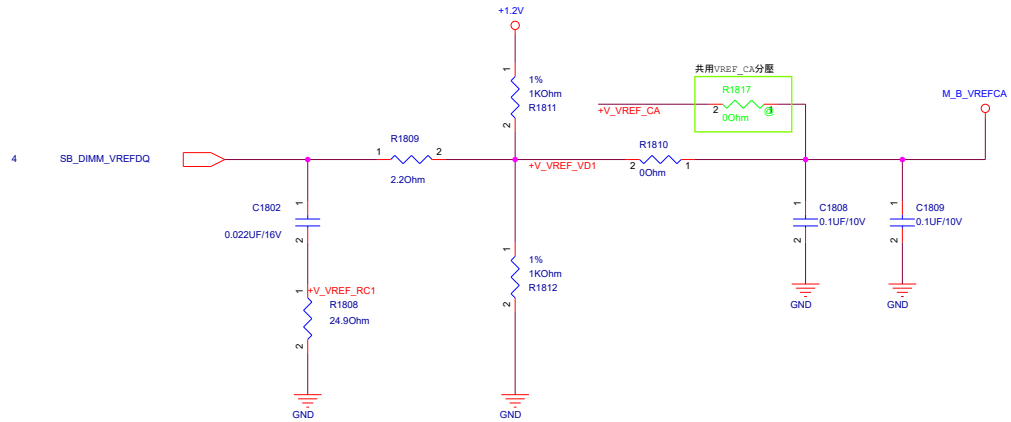
SO-DIMM0 Vref



SKL H DDR4/DDR4-RS SO-DIMM V_{REF-CA} Overview



SO-DIMM1 Vref



Project Name: GL502VD		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 18 of 102	

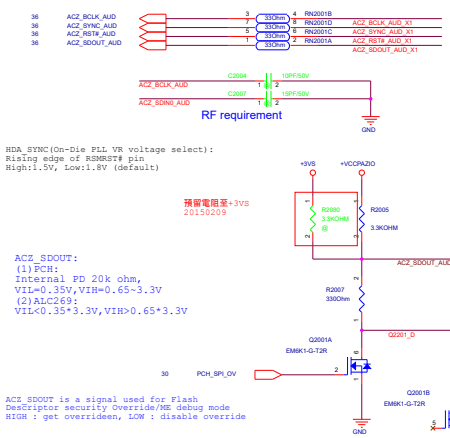
VL1.0-09

20,30,58,80	ALL_SYSTEM_PWRGD	1	T2900
6	CLK_CPU_BCLK_X1	1	T2902
6	DDR_VTT_CTRL	1	T2903
20	DPWROK_R	1	T2904
6	H_CPUPWRGD_X1	1	T2905
6	H_VCCST_PWRGD	1	T2906
20	ME_AC_PRESENT_X1	1	T2907
20	ME_SusPwrDnAck	1	T2908
20,40,53	SUS_CLK	1	T2909
22,30	PCH_SUS_STAT#	1	T2910
6,21	PCH_THERMTRIP#	1	T2911
24,32	PLT_RST#	1	T2912
20	PM_PWROK_X1	1	T2913
20,30	PM_SLP_SUS#	1	T2915
20,30,57,58	PM_SUSB#	1	T2916
20	PM_SYSPWROK_X1	1	T2917
20	PWRBTN#	1	T2918
20	RTCRST#	1	T2919
20	SLP_S0#	1	T2922
20	SLP_S3#	1	T2923
20	SLP_S4#	1	T2924

Project Name	GL502VD		Rev 1.0
Title :	PCH-XDP		
Size B	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 29 of 102		

Main Board

HD Audio

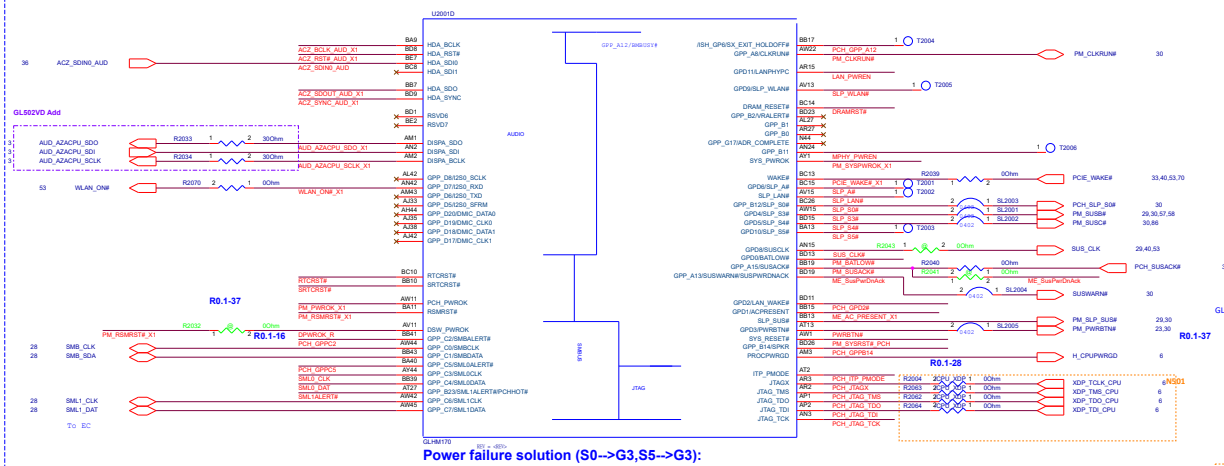


HDA_SYNC(On-Die PLL VR voltage select):
RisIng edge of RSMRST# pin
High:1.5V, Low:1.8V (default)

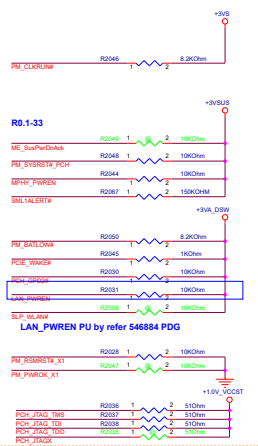
預留電阻至+3VS
20150209

ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIL=0.35V,VIH=0.65~3.3V
(2)ALC269:
VIL<0.35*3.3V,VIH>0.65*3.3V

ACZ_SDOUT is a signal used for Flash
Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

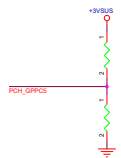


Power failure solution (S0-->G3,S5-->G3):



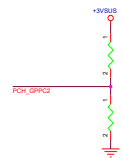
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST	
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+VCCPAZIO
		+3VS		

eSPI or LPC



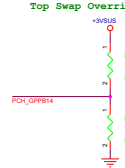
PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

TLS Confidentiality



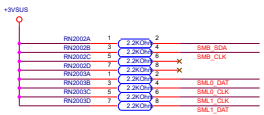
PCH_GPPC2: weak internal pull down	
PU	Enable
PD	Disable (default)

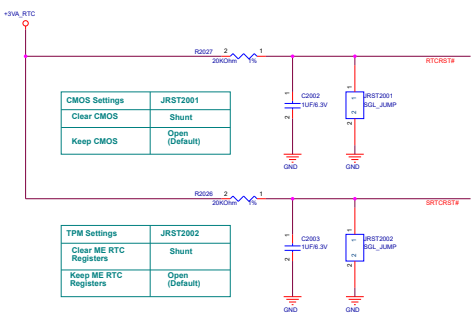
Top Swap Override



PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

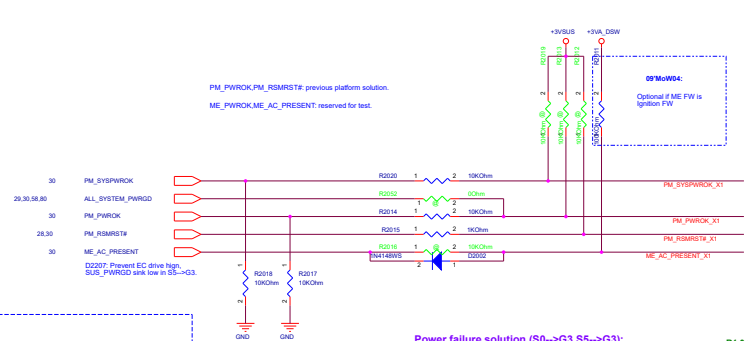
SMBUS

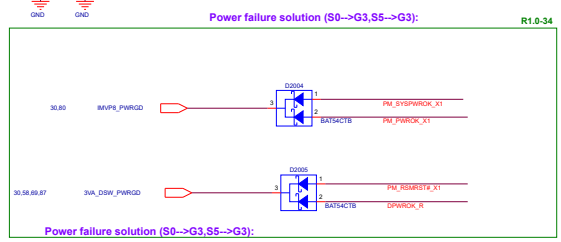


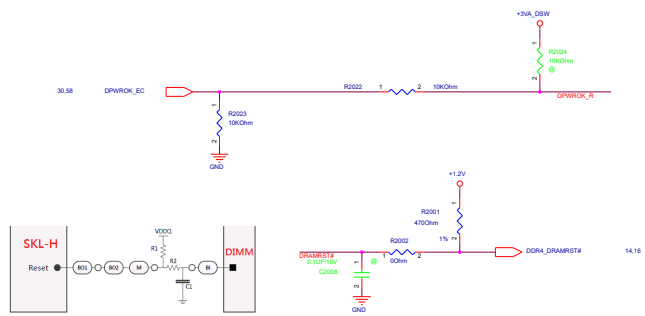


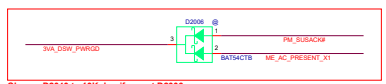
CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)





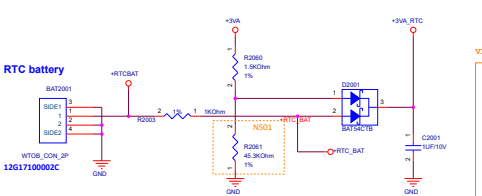




Change D2040 to 10Kohm if mount D2006

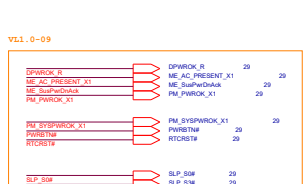
Deep SX discharge (S0-->DSX,S5-->DSX)

RTC battery



USE RTC Battery:
P/N: 0B100-00020300 BATT-LI CR2032 3V/220mAH
P/N: 0B100-00020400 BATT-LI CR2032 3V/220mAH

VL1.0-09

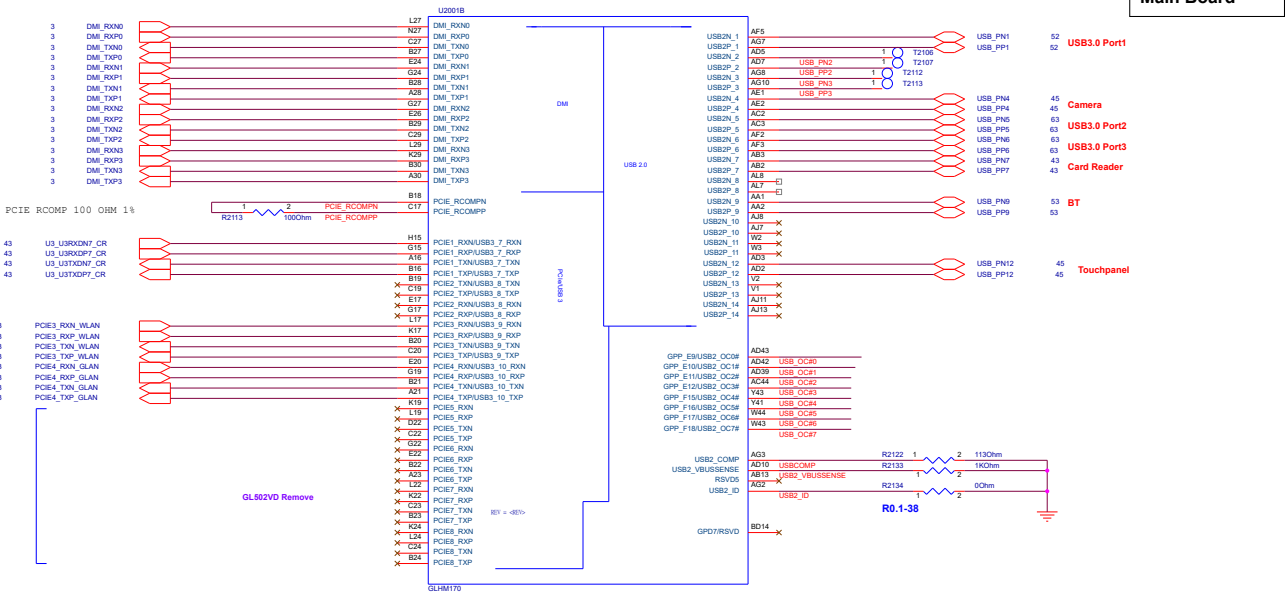


Project Name	GL502VD	Rev	1.0
Title :	PCH-CPT(1)SATA,IHDA,RTC,JTAG		
Size	Custom	Dept.:	ASUSTeK COMPUTER
Engineer:	Ben_Fang		
Date:	Wednesday, February 15, 2017	Sheet	20 of 102

PCIE Setting

GL502VM PCIE/SATA Function define
Skylake HM170

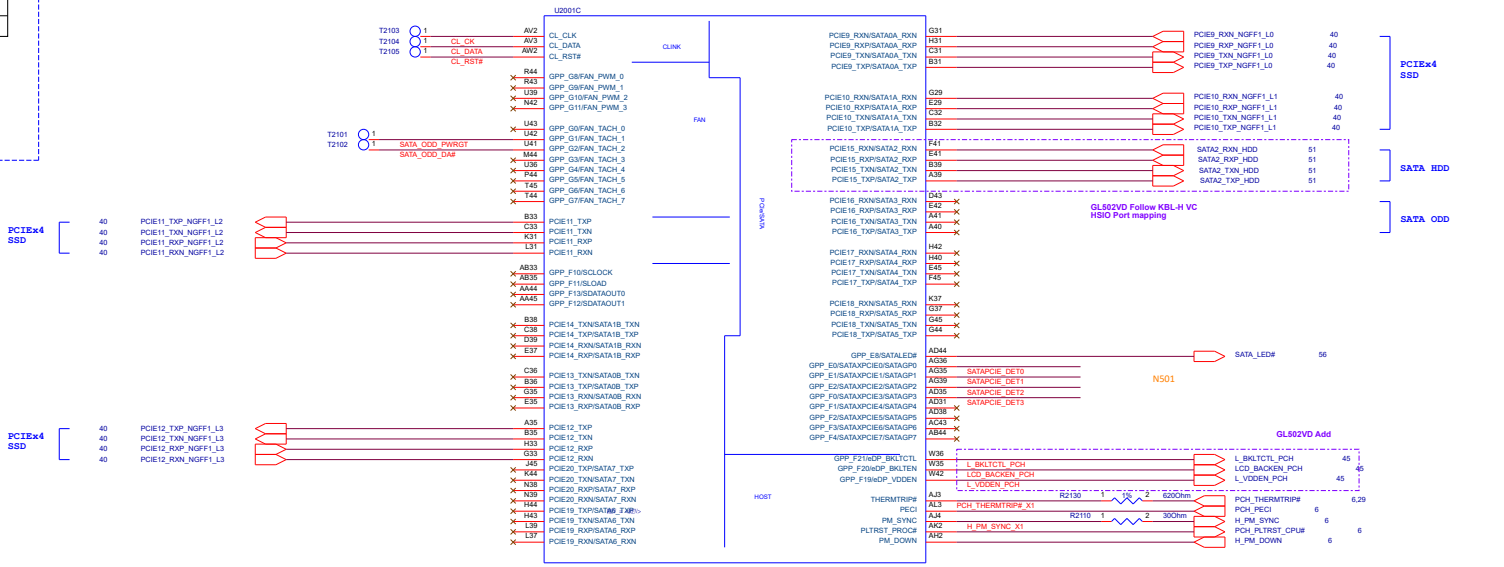
HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06	USB3_IO	
07	USB3#07 / PCIE#01	CardReader_USB3	SRC1
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN	SRC4
11	PCIE#05 / GBE	TBT(NC)	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD SATA SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	1st HDD	
23			
24			
25			
26			



USB Setting

GL502VD USB Function define
HM170

USB 2.0	Function	USB 3.0	Function
USB2_01	USB3.0 MB Port1	USB3_01	MB USB3.0
USB2_02		USB3_02	
USB2_03		USB3_03	
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 Port2	USB3_05	USB3.0 IO Port1
USB2_06	USB3.0 Port3	USB3_06	USB3.0 IO Port2
USB2_07	CardReader	USB3_07	Card reader
USB2_08		USB3_08	
USB2_09	BT		
USB2_10			
USB2_11			
USB2_12			



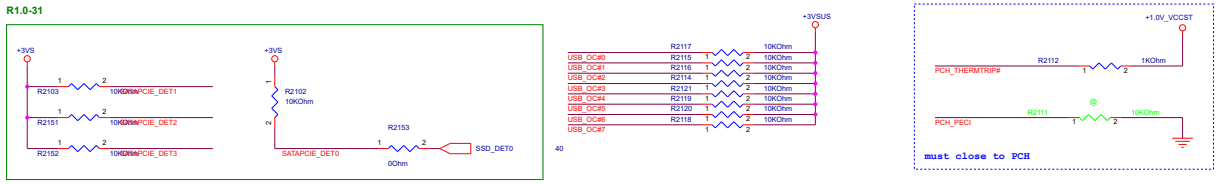
GL502VD PCIE/SATA Function define

	Function
PCIE-01	
PCIE-02	
PCIE-03	WLAN
PCIE-04	GLAN
PCIE-05	
PCIE-06	
PCIE-07	
PCIE-08	
PCIE-09 (SATA-0A)	PCIE SSD
PCIE-10 (SATA-1A)	PCIE SSD
PCIE-11	PCIE SSD
PCIE-12	PCIE SSD

	Function
PCIE-13 (SATA-0B)	
PCIE-14 (SATA-1B)	
PCIE-15 (SATA-2)	HDD
PCIE-16 (SATA-3)	
PCIE-17 (SATA-4)	
PCIE-18 (SATA-5)	
PCIE-19 (SATA-6)	
PCIE-20 (SATA-7)	

	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	
CLKREQ-3	WLAN
CLKREQ-4	GLAN
CLKREQ-5	
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

R1.0-31



ASUS	Project Name: GL502VD		Rev: 1.0
Title : PCH-CPT(2)_PCIE,CLK,USB			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 21 of 102		

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8995VG-128/CX	06037-00050600

Power

R1.0-29

+3VS, +3VA_EC, +3VPLL, +3VACC, EC_AGND

C3002 0.1UF/16V
C3051 0.1UF/16V
C3052 0.1UF/16V
C3053 0.1UF/16V
C3054 0.1UF/16V
C3004 0.1UF/16V
C3005 0.1UF/16V
C3007 0.1UF/16V
C3001 0.1UF/16V
SL3005 0603
SL3006 SHORT_LAND
SL3007 SHORT_LAND

U3001 IT8995VG-128/CX

LPC: LPC_AD0, LPC_AD1, LPC_AD2, LPC_AD3, CLK_KBCPCI_PCH, LPC_FRAME#, BUF_PLT_RST#, INT_SERIRQ, EXT_SMI#, EXT_SCI#, RC_IN#, EC_RST#

FLASH ROM: DGPU_LIMIT, EC_SCK_PCH, EC_SO_PCH, EC_SI_PCH, EC_SCE#_PCH, PWRLIMIT_EC#

KBMX: KSI0~KSI7, KSO0~KSO15

GPIO: PM_PWRBTN#, PM_SUSC#, EC_GPJ6, USB_CHARGE_ON#, PM_SLP_SUS#, SUSWARN#, 3VA_DSW_PWRGD_EC, PM_CLKRUN#, P_SMB3_CLK, P_SMB3_DAT, PM_RSMRST#, DPWROK_EC, PM_PWROK, PM_SYSPWROK, 3VSUS_PWRGD, ALL_SYSTEM_PWRGD, IMVP8_PWRGD, A/D_MAX_POWER, MB_MAX_POWER, 3VADSW_ON, PCH_SUS_STAT#, EC_GPJ5

PS/2: 5VSUS_ON, VSUS_ON, P_SMB0_CLK, P_SMB0_DAT, TP_CLK, TP_DAT

SWBAN: PWR_SW#, PS_ON_EC, SMB1_CLK, SMB1_DAT, PECI_EC, PCH_SPI_OV

Battery

Thermal sensor

PU/PD

PWR_SW#, AC_IN_OC#, LID_SW#, CHG_LED#, CHG_FULL_LED#, PM_EXTTS#0, THRO_CPU#, PWRLIMIT_EC#, SMB1_DAT, SMB1_CLK, P_SMB0_CLK, P_SMB0_DAT, P_SMB3_DAT, P_SMB3_CLK

3VADSW_ON, 5VSUS_ON

for load code

ClickPad Schematic: TP_DAT, TP_CLK

N501: BAT1_IN_OC#

2015.08.21 EMI Modify

For EMI

EC_RST#, PM_SYSPWROK, PM_PWROK, DPWROK_EC, RC_IN#, 3VSUS_PWRGD, KB_LED_PWM, CHG_FULL_LED#, PWR_LED, CHG_LED#, NUM_LED#, ALL_SYSTEM_PWRGD, IMVP8_PWRGD

For EMI 2015.08.21 EMI Modify

3VADSW_ON, A/D_MAX_POWER, MB_MAX_POWER

Close U3001

CLK_KBCPCI_PCH, BAT1_IN_OC#, PWR_SW#, BUF_PLT_RST#

R1.0-34

3VA_DSW_PWRGD, IMVP8_PWRGD, 3VA_DSW_PWRGD_EC

R1.0-25 R1.0-38 To CC logic at p49

INTR#, ID#, USB31_5VBUS#, EC_GPC4, EC_GPJ6, EC_GPJ0

R0.1-41

R0.1-42

<Variant Name>

ASUSTeK COMPUTER

Title : CR_KBC_IT8521

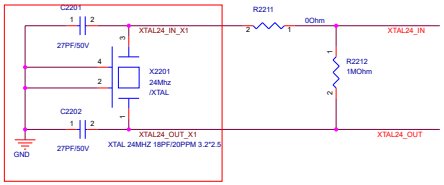
Engineer: Ben_Fang

Size: C | Project Name: GL502VD | Rev: 1.0

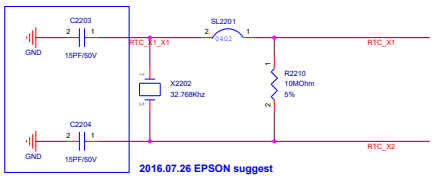
Date: Wednesday, February 15, 2017 | Sheet 30 of 102

XTAL 24MHz

R1.2_15 TXC Suggest

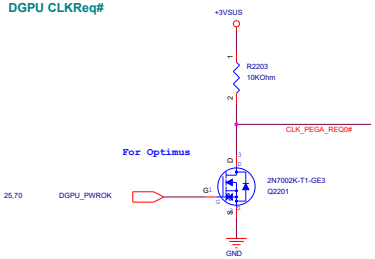


RTC CRYSTAL 32.768KHz

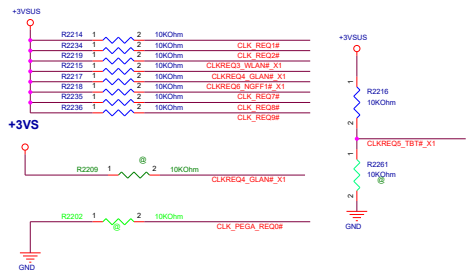


2016.07.26 EPSON suggest

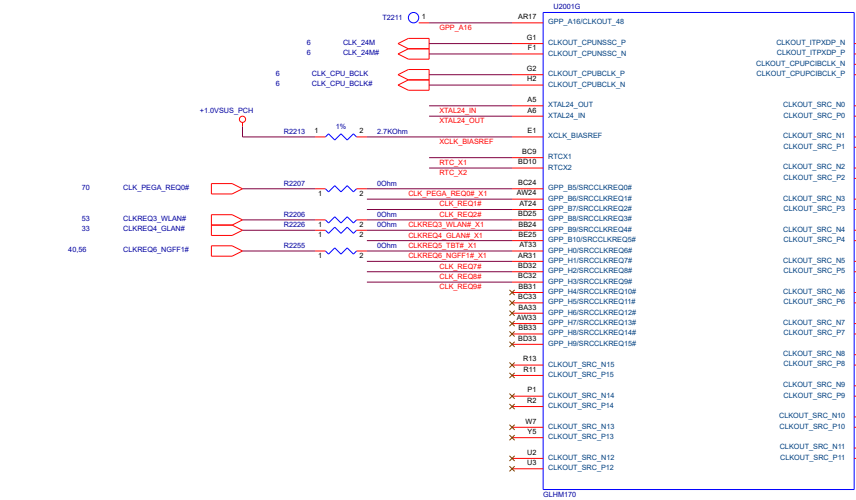
DGPU CLKReq#



PCH CLKREQ Setting:



CLKREQ4_GLAN#_X1



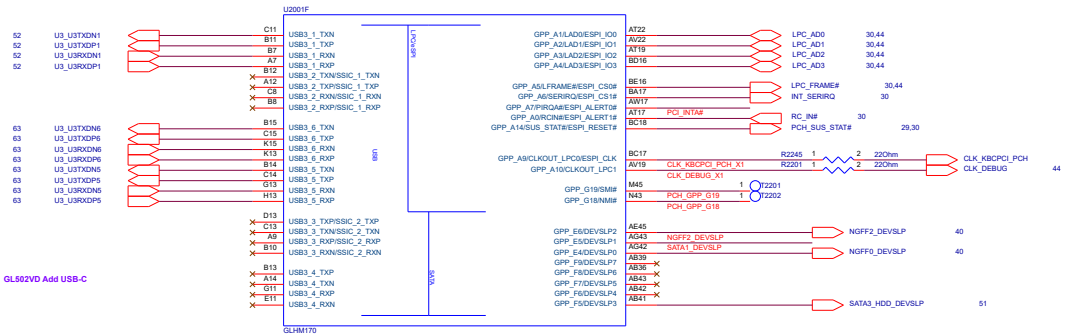
REV = <REV>

MB USB3.0 (Charger)

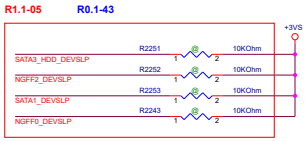
USB3.0 IO Port2

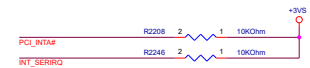
USB3.0 IO Port1

GL502VD Add USB-C



REV = <REV>





ASUS	Project Name: GL502VD		Rev: 1.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 22 of 102		

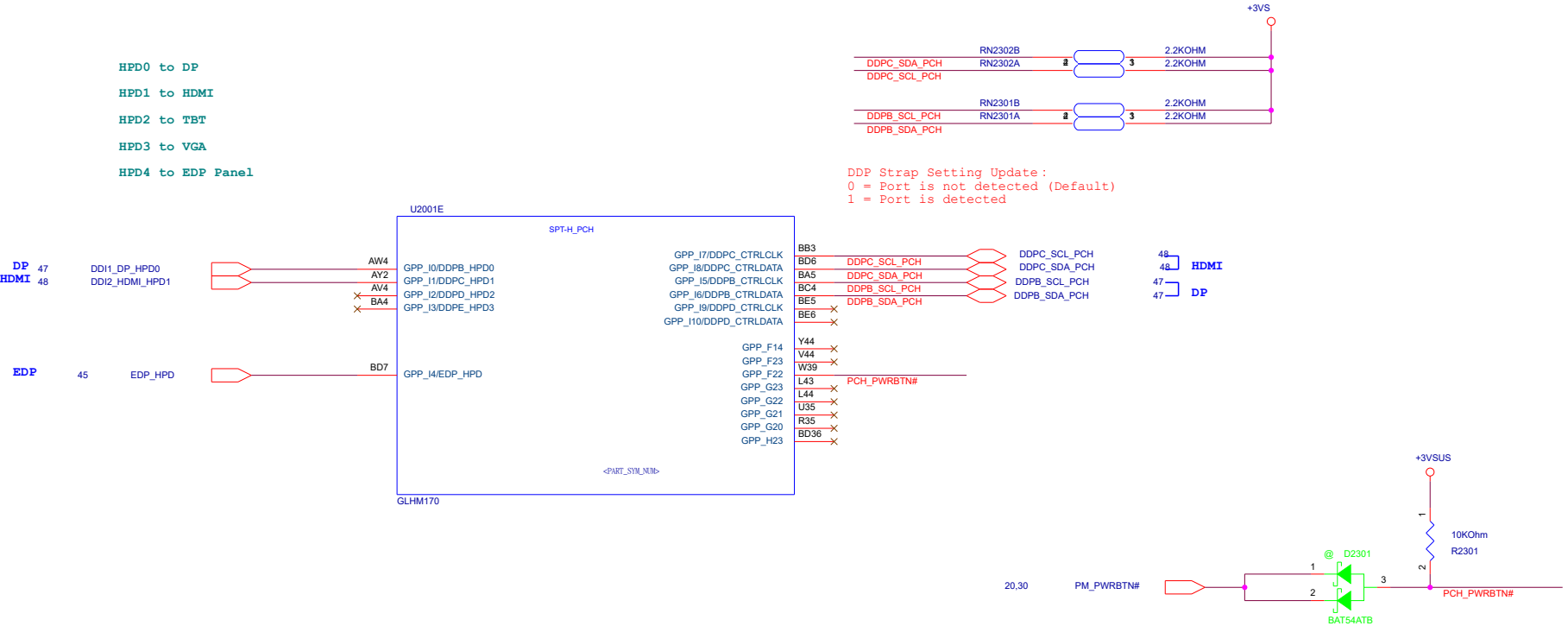
HPD0 to DP

HPD1 to HDMI

HPD2 to TBT

HPD3 to VGA

HPD4 to EDP Panel



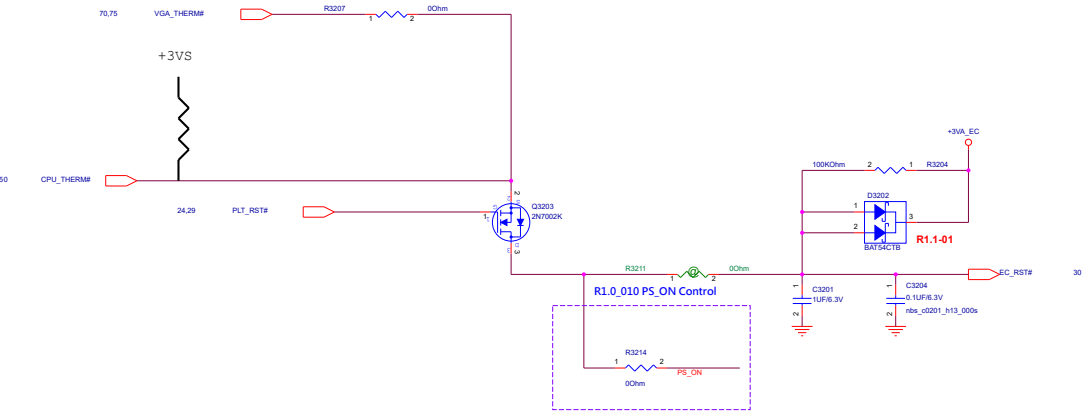
Project Name: GL502VD		Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 23 of 102	

<variant Name>

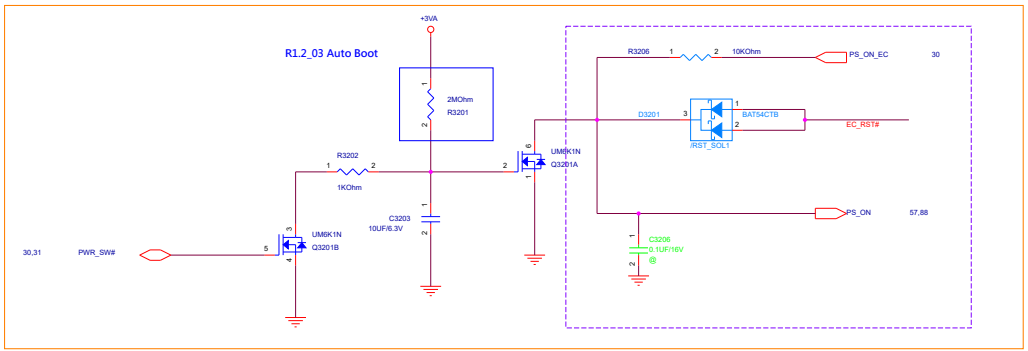
ASUSTeK COMPUTER INC. NB1	Title :	Aud_HP Jack, MIC	
	Engineer:	Ben_Fang	
Size: Custom	Project Name: GL502VD		Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 38 of 102		

Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



Battery embedded (press pwr_sw 10sec, then reset ec)



EC power off solution:
Solution1 Mount R3206, D3201/ Unmount R3216
Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

R1.2-65

<Variant Name>

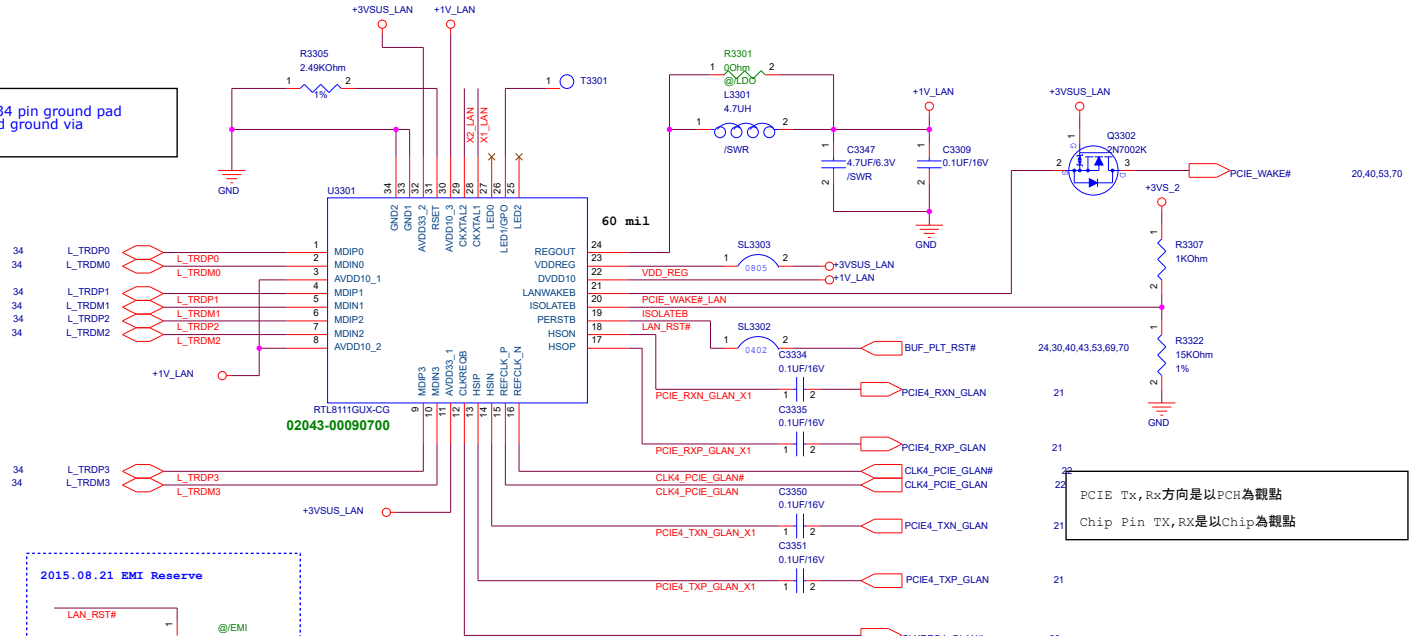
ASUSTeK COMPUTER	Title :	RST_Reset Circuit	
	Engineer:	Ben_Fang	
Size: B	Project Name: GL502VD		Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 32 of 102		

<Variant Name>

ASUSTeK COMPUTER INC. NB1	**Title :** Card Reader-RTS5226	
	Engineer: Ben_Fang	
Size: C	Project Name: **GL502VD**	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 42 of 102	

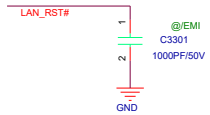
The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad
need ground via



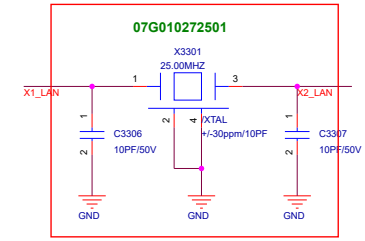
PCIE Tx,Rx方向是以PCH為觀點
Chip Pin TX,RX是以Chip為觀點

2015.08.21 EMI Reserve



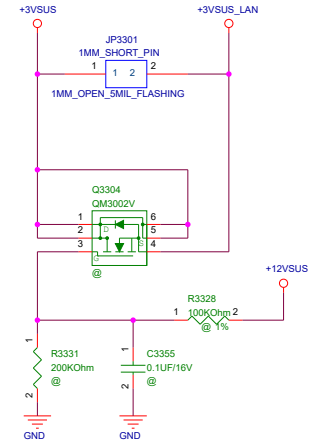
CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side

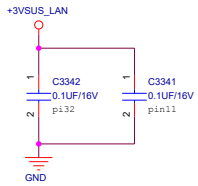
R1.2_15 TXC Suggest

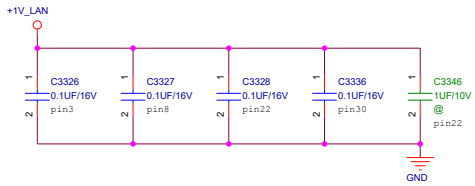


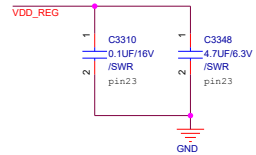
X3301: 25MHZ +/-30ppm/10pF (3225)
1st: P/N:07G010272501 TXC/7V25000011
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms







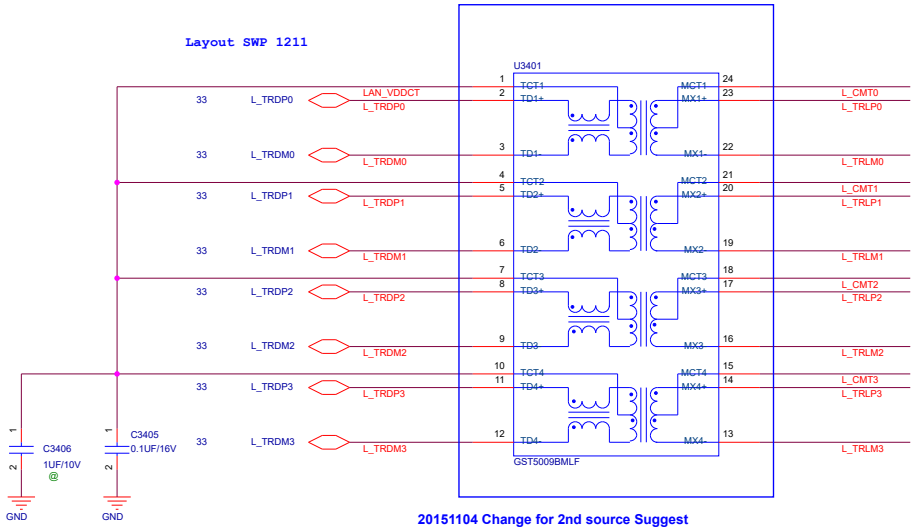


C3348, C3310 close to pin 23
reserved for SWR mode

ASUS	Project Name: GL502VD		Rev: 1.0
Title : LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017		Sheet 33 of 102	

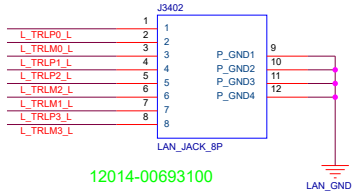
R1.2_02 follow GL502VT

Layout SWP 1211



20151104 Change for 2nd source Suggest

LAN Connector

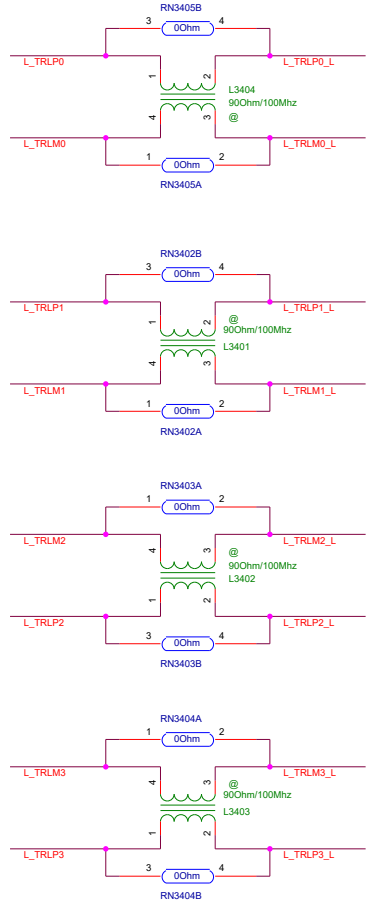


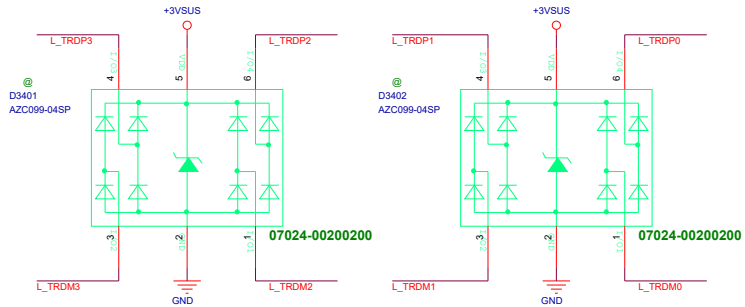
12014-00693100

J3402 LAN Jack

1st Source: P/N:12014-00161700 FOXCONN/JM3611-NS640003-7H

2nd Source: P/N:12014-00035500 SINGATRON/2RJ1648-000111F

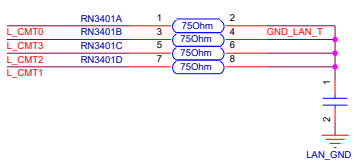




D3401,D3402 ESD Diode

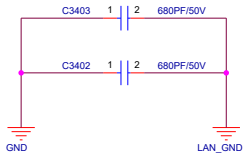
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



GND_LAN_T 上禁止加任何零件

2012/2/16 EMI

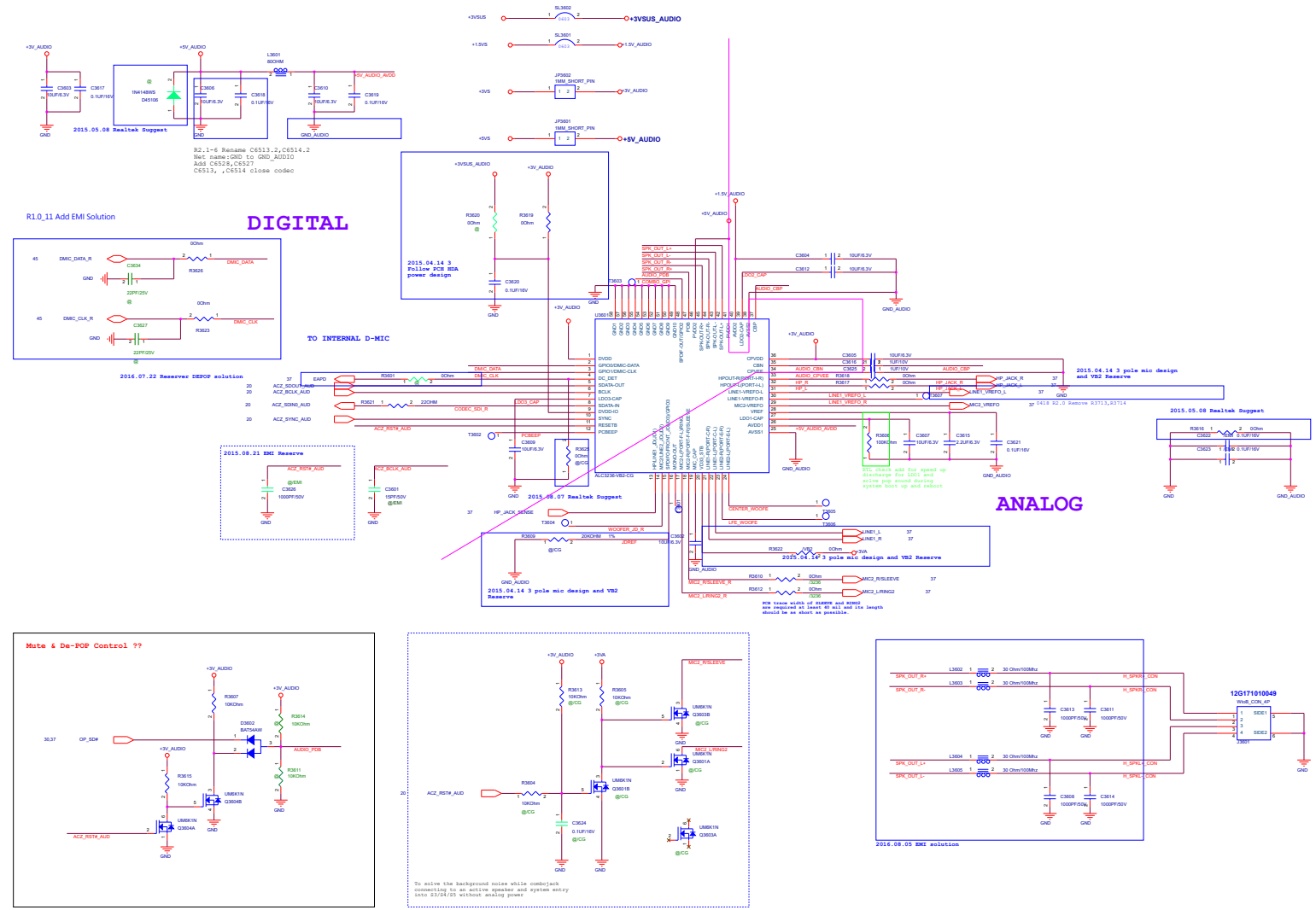


Place near chassis GND

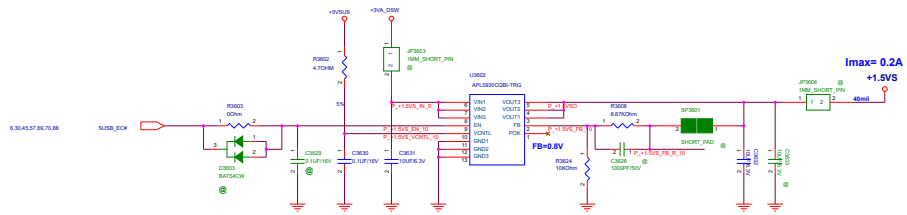
ASUS	Project Name: GL502VD	Rev: 1.0
Title : LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 34 of 102	

<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : TBD	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 35 of 102	

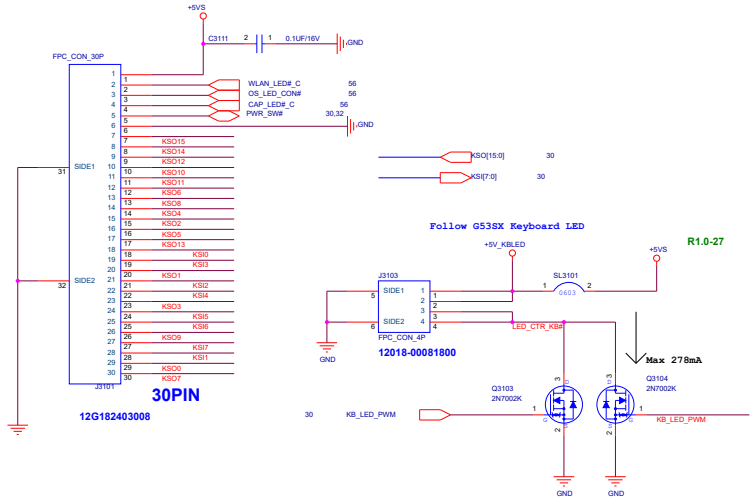


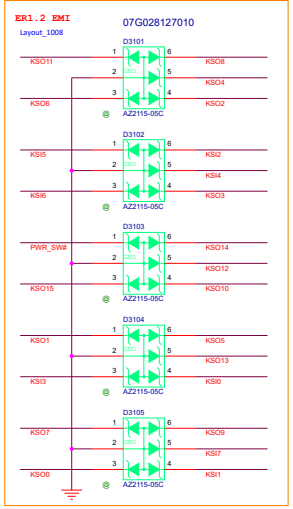
+1.5VS

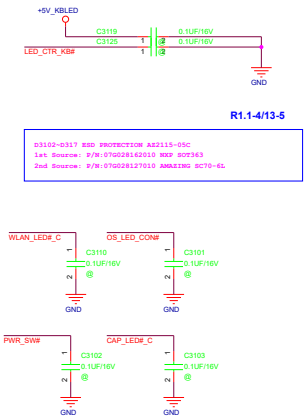


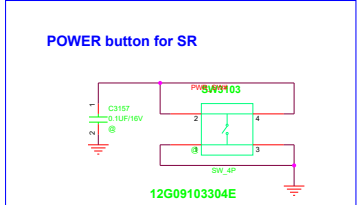
ASUS	Project Name: GL502VD		Rev: 1.0
Title :	AUDIO ALC3236-CG/VB2		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017		Sheet: 36 of 102	

Keyboard Connector

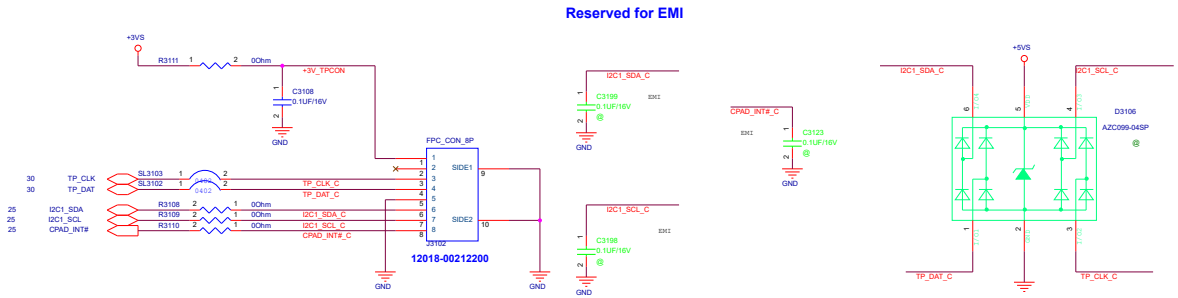




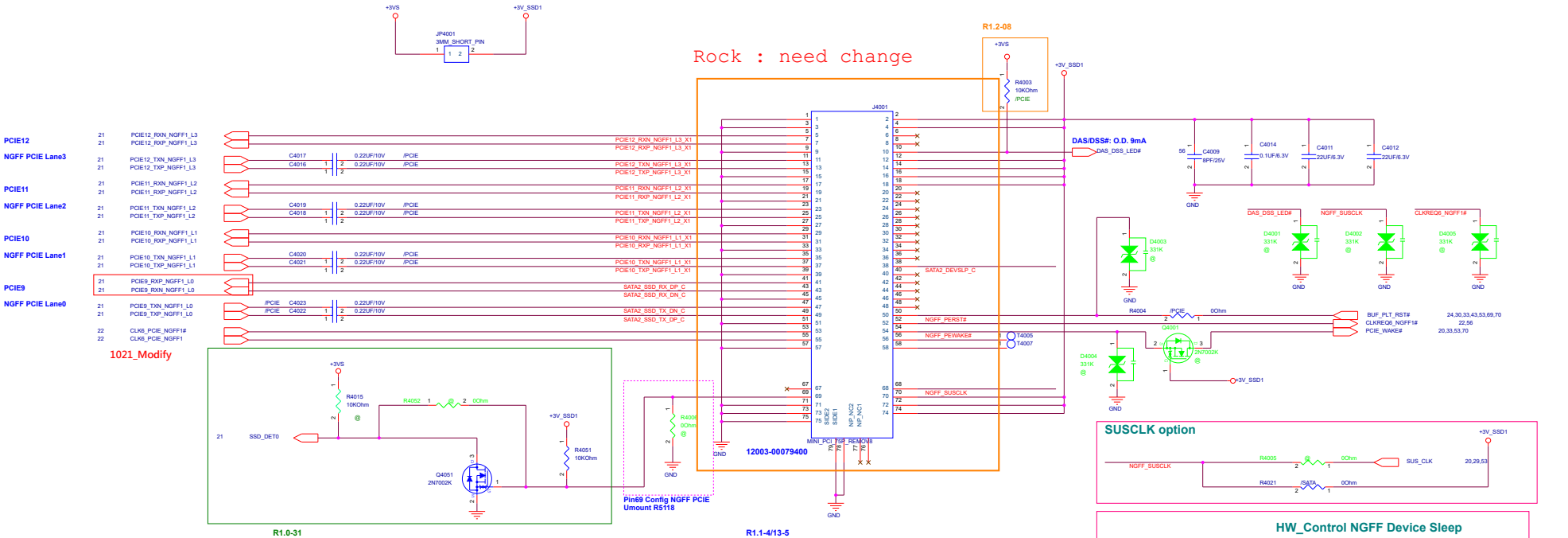




Click touch Pad Connector

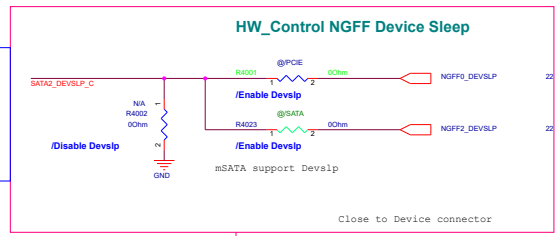


NGFF_SSD



SUSCLK option

HW_Control NGFF Device Sleep



SATA SSD

J4001_NGFF M-KEY PCIEx4 Connector H=3.0mm

1st Source: P/N:12003-00075100 ACES/51733-06702-012

2nd Source: P/N:12003-00075900 ARGOSY/NASM0-S6701-TPH4

3rd Source: P/N:12003-00076200 LOTES/APCI0079-P002A

4th Source: P/N:12003-00077200 DRAGONSTATE/213MAAA32FA

5th Source: P/N:12003-00076700 SINGATRON/2NF3001-012111F

SSD NUT

H4001 SMD236X236

HW Disable SSD Devslp	Mount R4002=0ohm, Unmount R4001=0ohm
HW Enable SSD Devslp	Unmount R4002=0ohm, Mount R4001=0ohm

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : MiniCard_SSD

Engineer: Ben_Fang

Size: C | Project Name: GL502VD | Rev: 1.0

Date: Wednesday, February 15, 2017 | Sheet 40 of 102

<Variant Name>

	Project Name **GL502VD**	Rev 1.0

Title : USB 3.1 MB Type-C

Size Custom	**Dept.:** ASUSTeK COMPUTER	**Engineer:** Ben_Fang

Date: Wednesday, February 15, 2017	Sheet	49	of	102

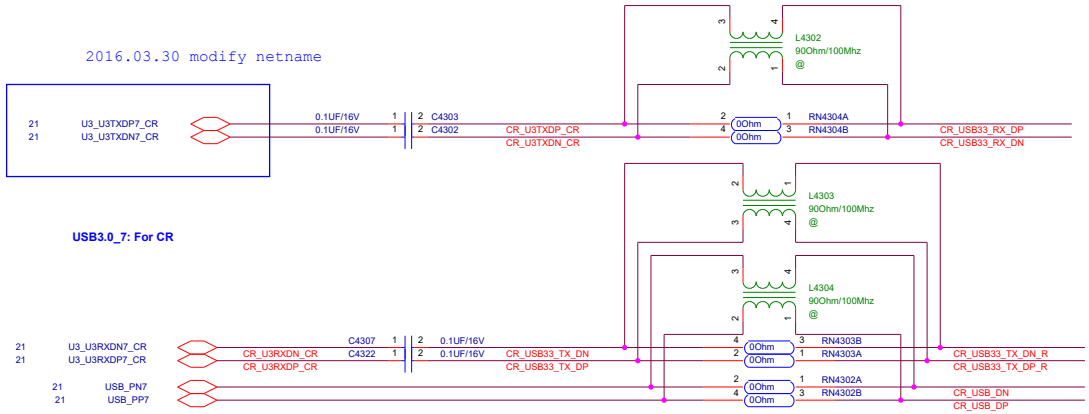
<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : CB_*****	
	Engineer: Ben_Fang	
Size: A	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 41 of 102	

CR I/O Conn. (MB)

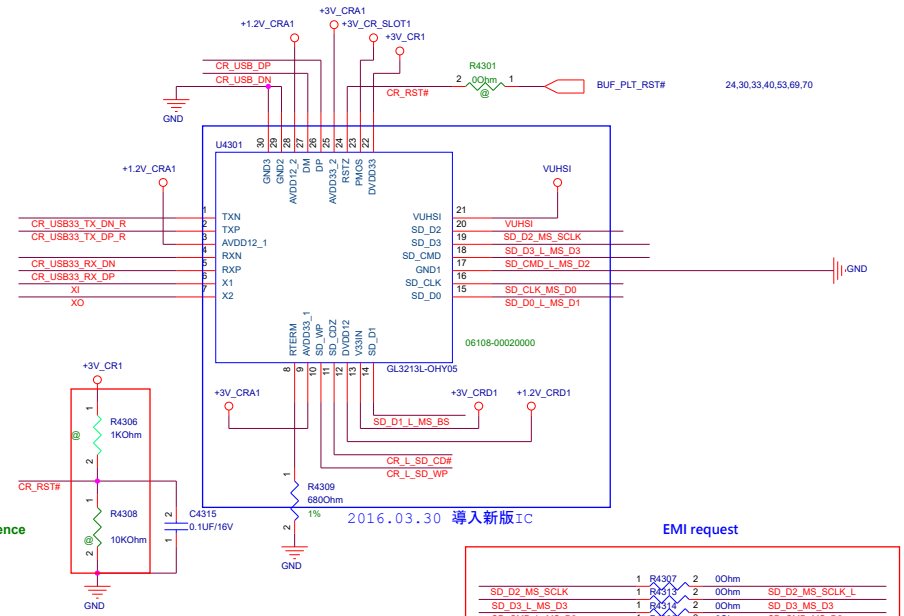
Main Board

2016.03.30 modify netname

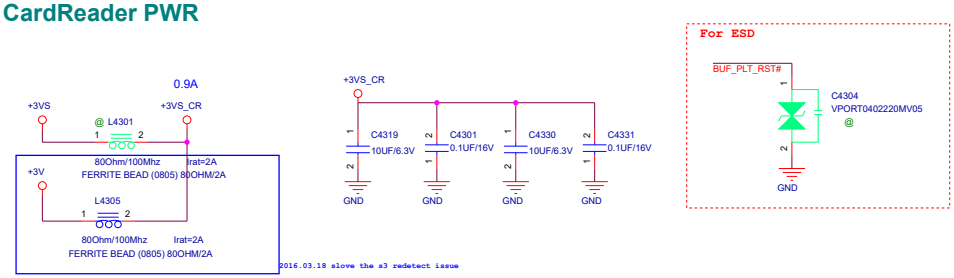


USB3.0_7: For CR

USB2.0_7: For CR



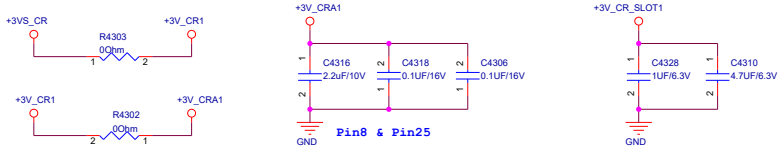
CardReader PWR

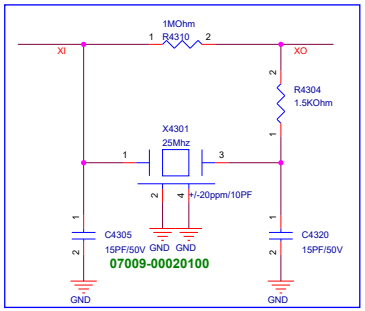


R1.2-18 Sequence

EMI request

SD_D2_MS_SCLK	R4307	0Ohm		SD_D2_MS_SCLK_L
SD_D3_L_MS_D3	R4313	0Ohm		SD_D3_MS_D3
SD_CMD_L_MS_D2	R4314	0Ohm		SD_CMD_MS_D2
SD_CLK_MS_D0	R4305	0Ohm		SD_CLK_L_MS_D0
SD_D0_L_MS_D1	R4315	0Ohm		SD_D0_MS_D1
SD_D1_L_MS_BS	R4316	0Ohm		SD_D1_MS_BS
CR_L_SD_CD#	R4317	0Ohm		CR_SD_CD#
CR_L_SD_WP	R4318	0Ohm		CR_SD_WP



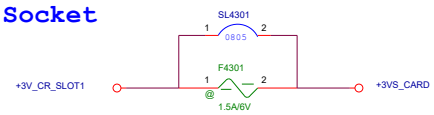


X4201: 25MHZ +/-20ppm/10pF (3225)

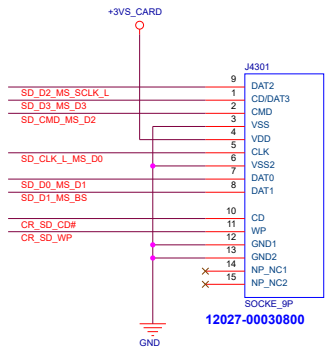
1st: P/N:07009-00020100 EPSON/FA-238G

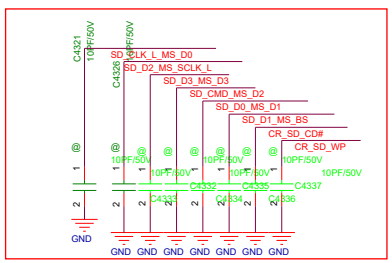
2nd: P/N:07009-00020800 TXC/7V25000036

CR Socket

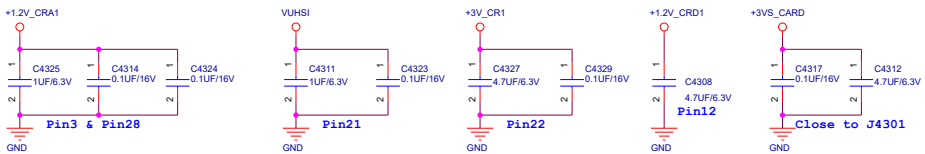


Reserved fuse for safety





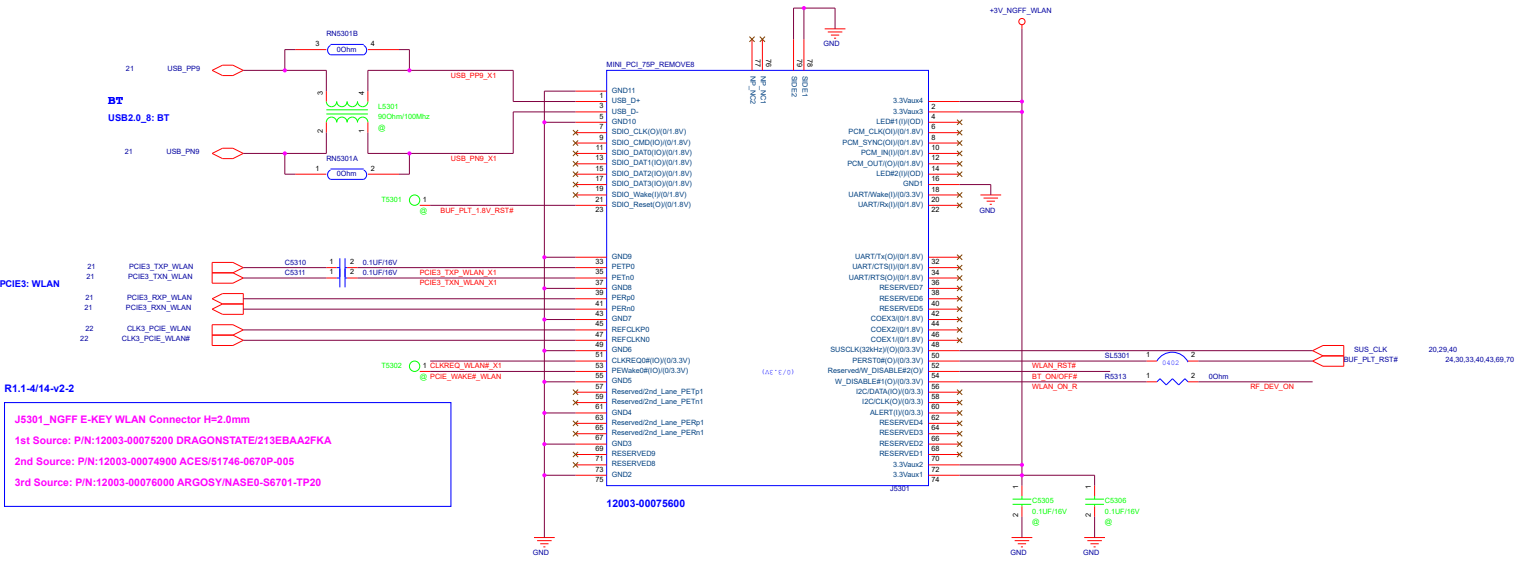
R1.0_011 Add EMI Solution



ASUS	Project Name: GL502VD		Rev: 1.0
Title : CB IO CON			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017		Sheet 43 of 102	

R1.1-02

NGFF M.2 TYPE_E-KEY WIFI



R1.1-4/14-v2-2

J5301_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FKA

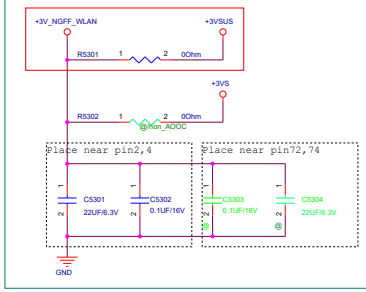
2nd Source: P/N:12003-00074900 ACES/51746-0670P-005

3rd Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

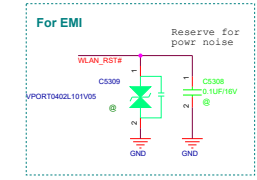
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

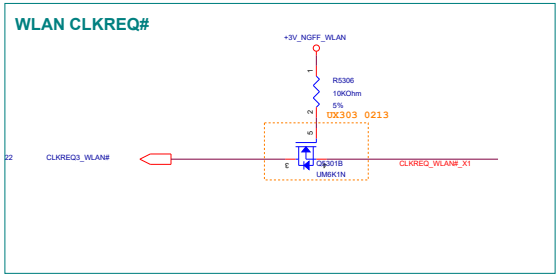
WLAN PWR to +3VSUS



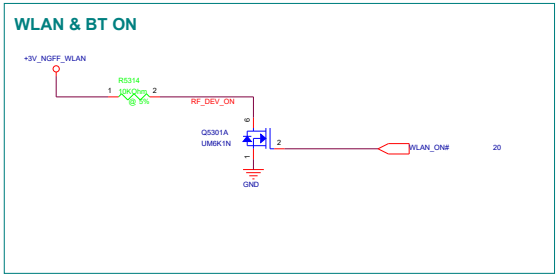
For EMI



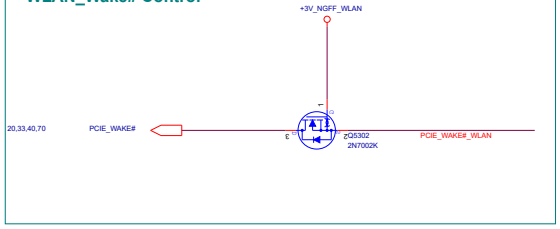
WLAN CLKREQ#



WLAN & BT ON

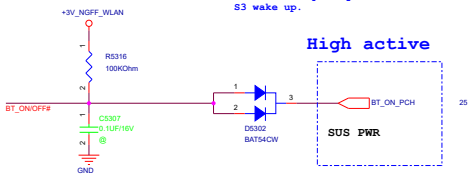


WLAN_Wake# Control



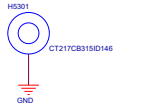
To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

High active



Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

NGFF NUT



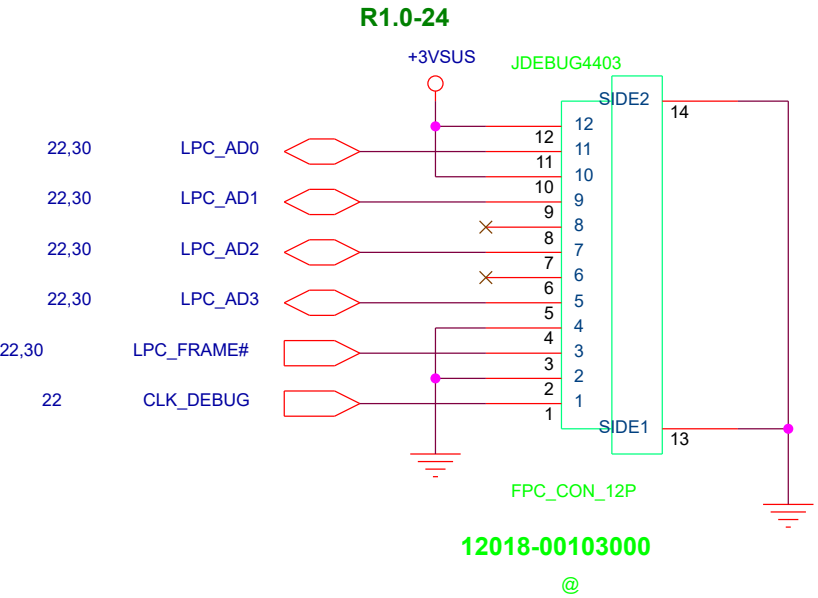
13020-00780900

74	3.3Vaux	GND	75
72	3.3Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PERn1	67
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	Reserved/2nd Lane PERp1	65
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	GND	63
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETn1	61
58	NFC I2C SM DATA (IO)(0/3.3)	Reserved/2nd Lane PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (?)(0/1.8V)	REFCLKN0	49
46	COEX2(?)(0/1.8V)	REFCLKP0	47
44	COEX3(?)(0/1.8V)	GND	45
42	CLink CLK	PERn0	43
40	CLink DATA	PERp0	41
38	CLink RESET (O)(0/3.3V)	GND	39
36	UART CTS (O)(0/1.8V)	PETn0	37
34	UART RTS (I)(O/1.8V)	PETp0	35
32	UART Tx (O)(0/1.8V)	GND	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(0/1.8V)	SDIO Reset(O)(0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake(I)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (OI)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (OI)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	1

<Variant Name>

ASUSTeK COMPUTER	Title :	WiFi/WiMax
	Engineer:	Ben_Fang
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 53 of 102	

LPC Debug Port



<Variant Name>

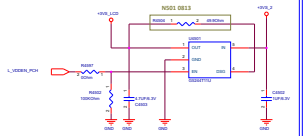
ASUSTeK COMPUTER INC. NB1	Title : DEBUG_LPC	
	Engineer: Ben_Fang	
Size: A	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 44 of 102	

<Variant Name>

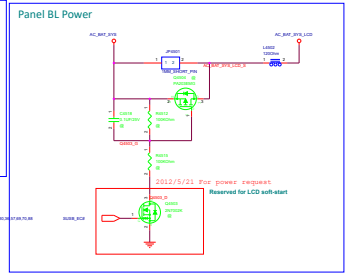
ASUSTeK COMPUTER INC	Title : TBD	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 54 of 102	

IO Board

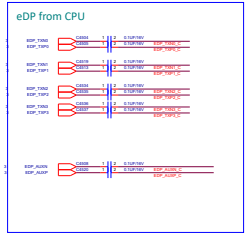
LCD Power switch



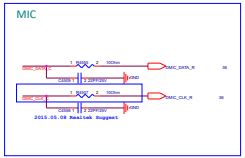
Panel BL Power



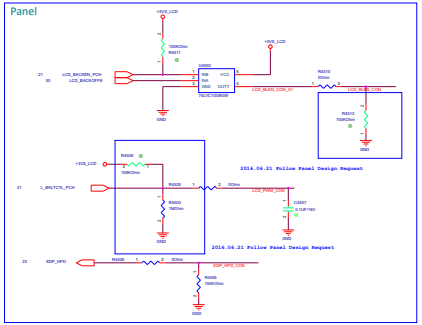
eDP from CPU



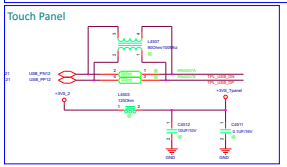
MIC



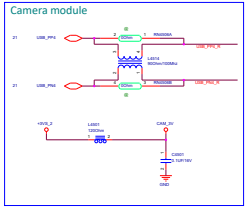
Panel



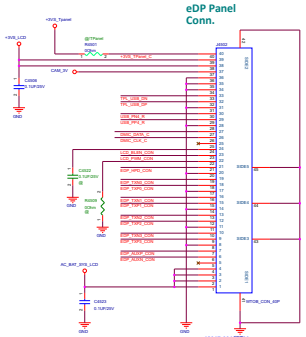
Touch Panel



Camera module



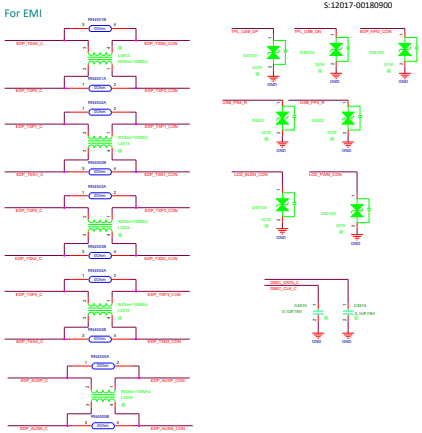
eDP Panel Conn.



12017-00180900

S:12017-00180900

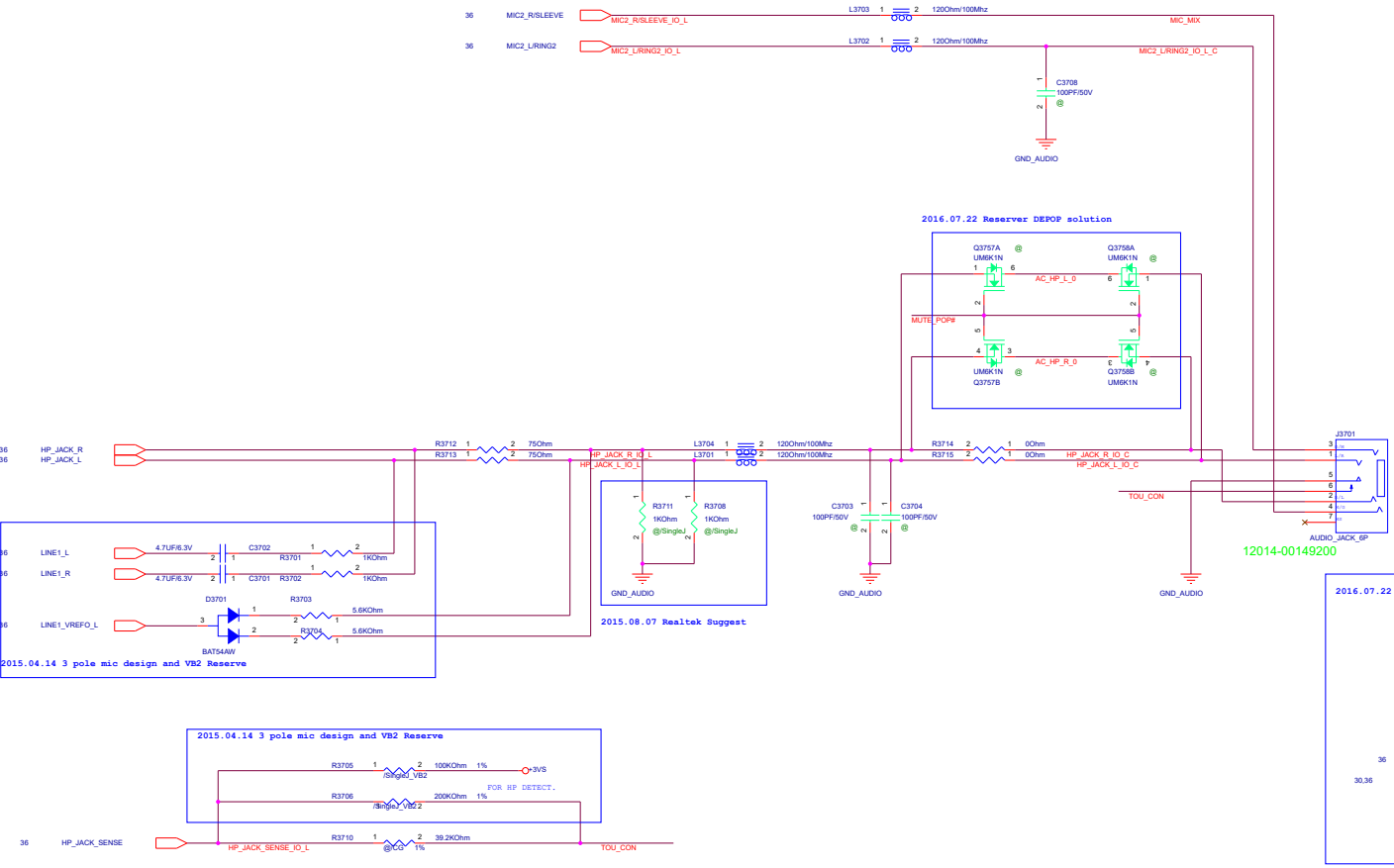
For EMI

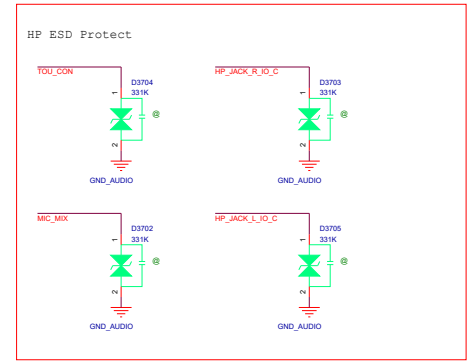


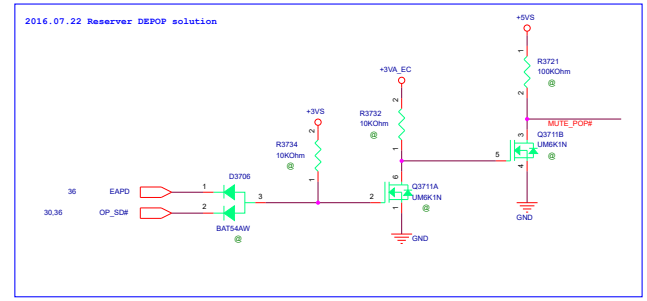
Title :	CRT eDP		
Engineer:	Ben_Fang		
Size: C	Project Name: GL502VD		Rev: 1B
Date: Wednesday, February 15, 2017	Sheet: 65	of: 102	

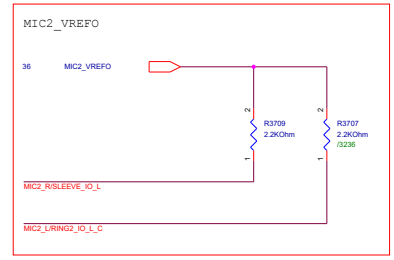
Headphone&MIC

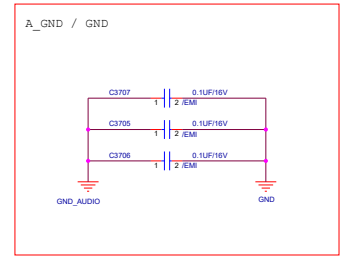
HP & MIC Connector







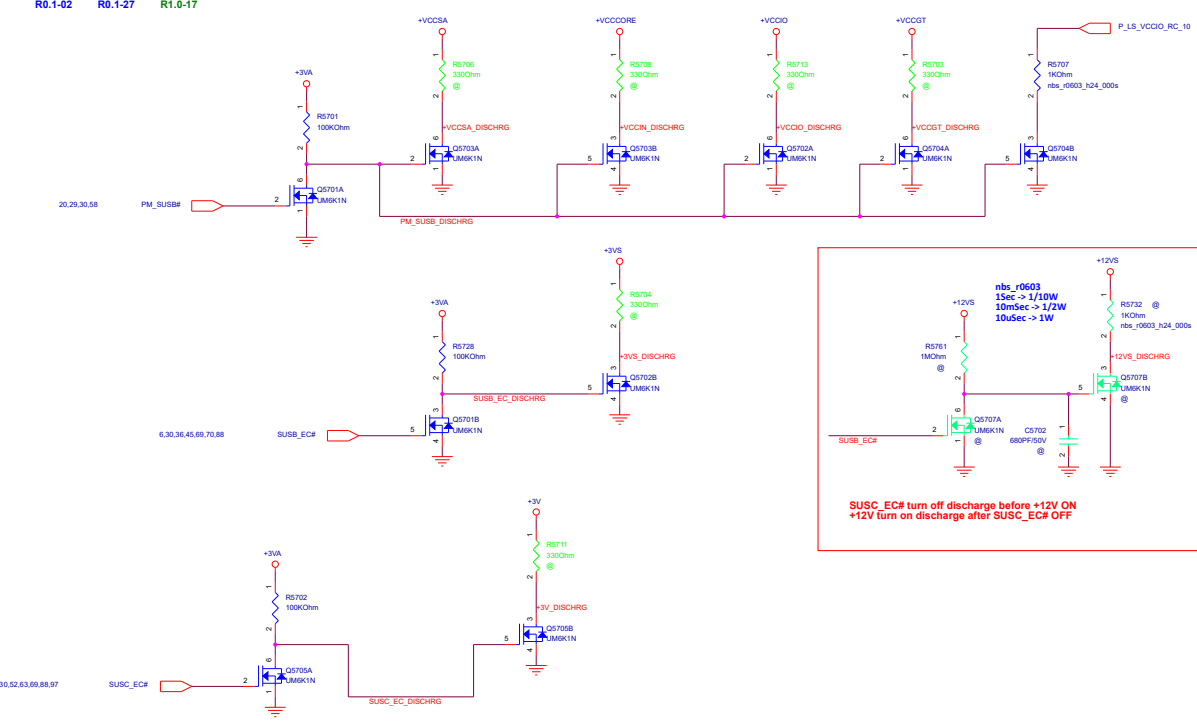




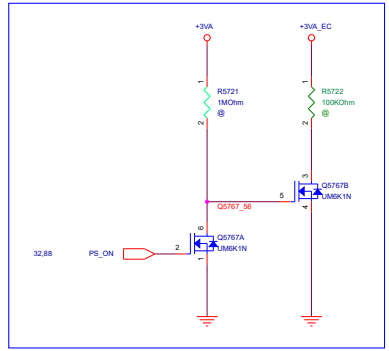
ASUS	Project Name: GL502VD		Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 37 of 102		

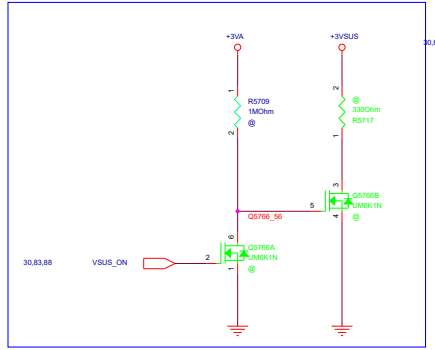
ASUS	Project Name: GL502VD	Rev: 1.0
Title : USB 3.1 ASM1142		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Ben_Fang
Date: Wednesday, February 15, 2017	Sheet: 46 of 102	

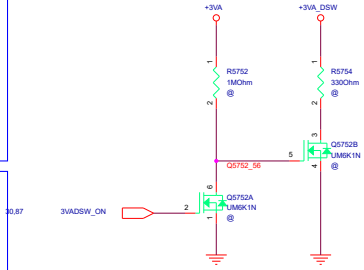
R0.1-02 R0.1-27 R1.0-17



88

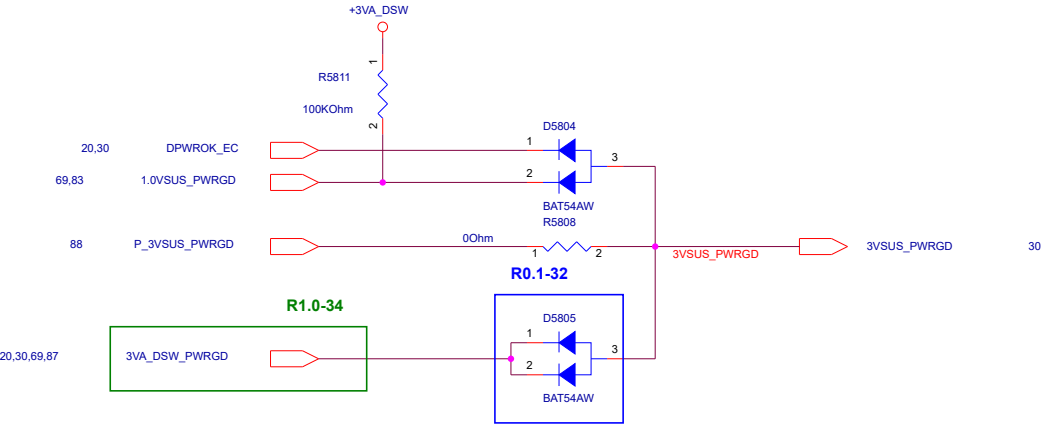




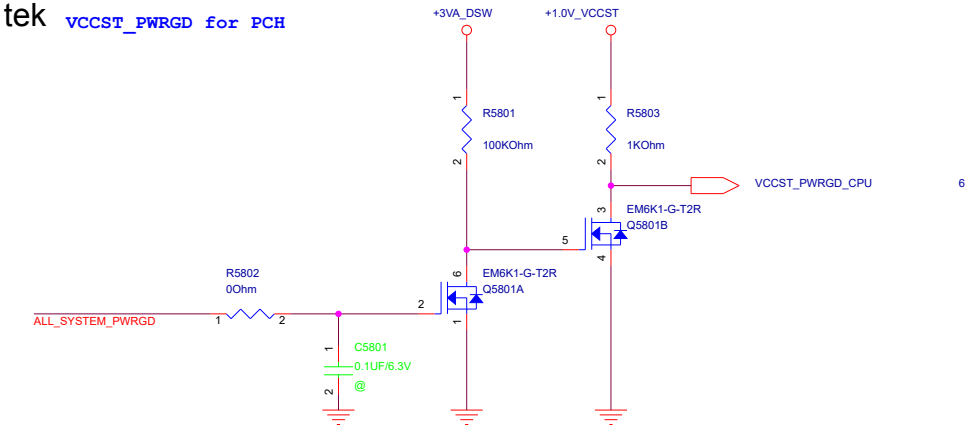


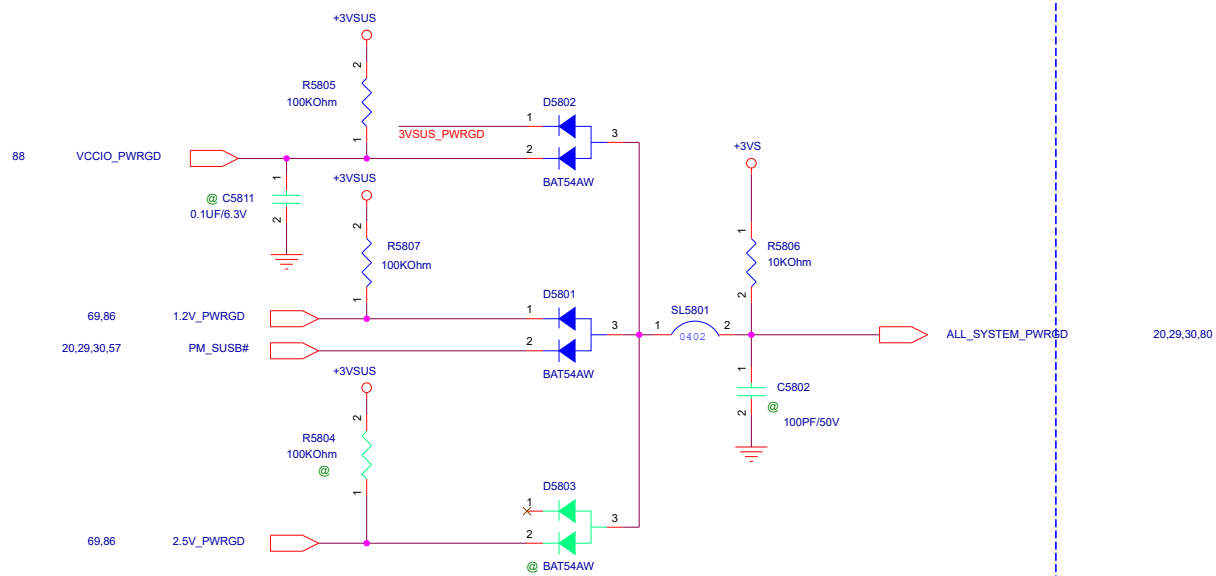
<Variant Name>

ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: Ben_Fang	
Size: Custom	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 57 of 102	



tek **VCCST_PWRGD for PCH**





<Variant Name>

ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: Ben_Fang	
Size: Custom	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 58 of 102	

Rev	Date	Description
R1.0	2016/09/07	1 : Modify GPU to N17P-G0/G1 (P.70-78) 2 : Change display to optimus (P.2,9,10,,23,45,47,48) 3 : Remove UMT fuction (P.11,22,29) 4 : Add new PC Beep/Hot KEY mapping (P.21,22) 5 : ADD USB-C Gen1 (P.54)
	2016/09/08	1 : Add +VCORE power and Cap (P.8-10)
R1.1		
R1.2	2015/12/11	

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: RD1_EE1

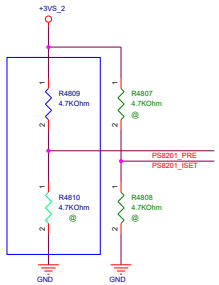
Size: D | Project Name: GL502VD | Rev: 1.0

Date: Wednesday, February 15, 2017 | Sheet 102 of 102

HDMI Active-Level Shift

PS8201_PRE

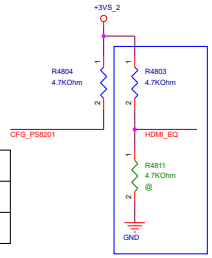
	pre-emphasis
L	0 db
M	1.6 dB
H	2.5 dB



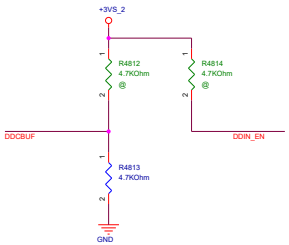
2016.07.20 VR solution

	HDMI_EQ
L	6.5dB@3Gbps
M	3dB@3Gbps
H	9.5dB@3Gbps

	CFG_PS8201
L	HDMI ID disable
H	HDMI ID enable

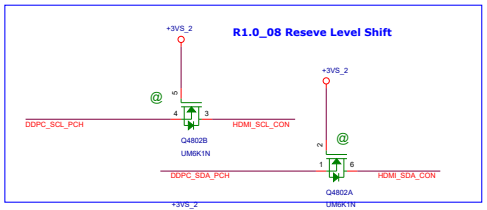


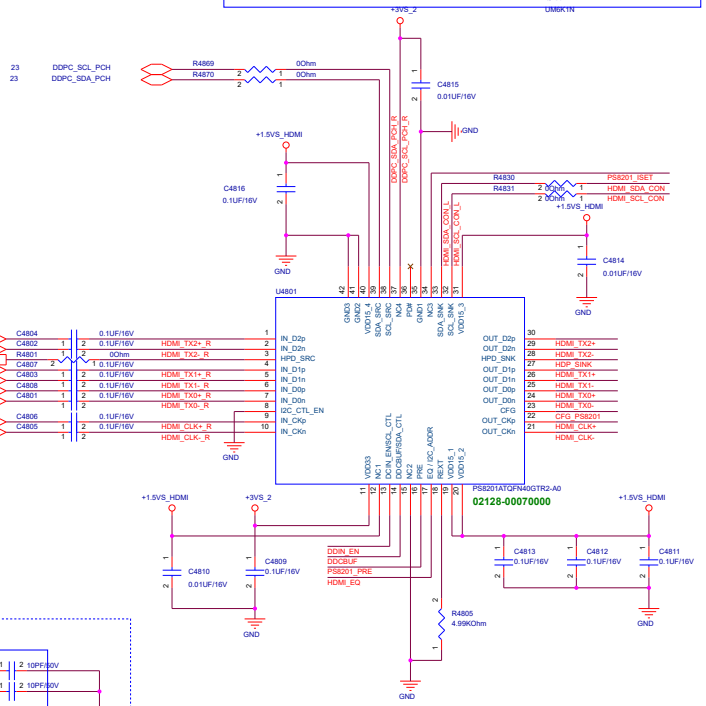
2016.07.20 VR solution



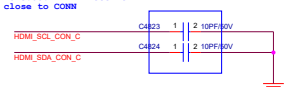
FIX can't read 4K2K HDMI Monitor EDID BUG

Reverse R4812, Mount R4813 Pull-down

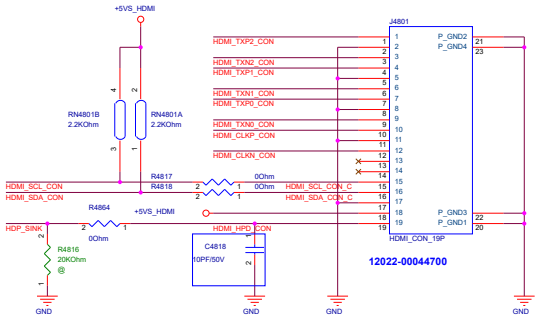




2015.08.21 EMI Reserve close to CONN



HDMI Conn.

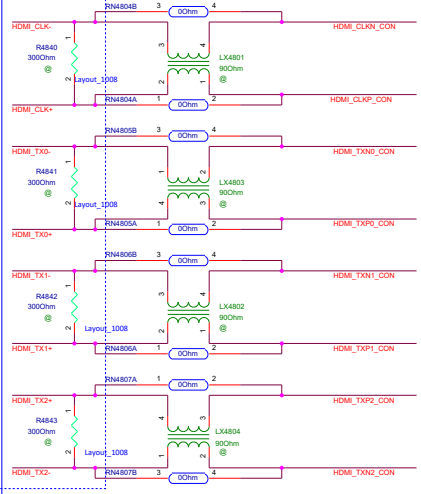


12022-00044700

2016.05.11 EMI Reserve

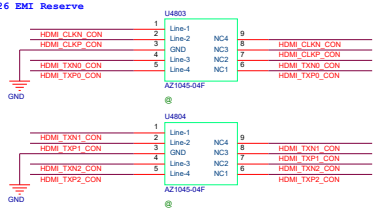
HDMI EMI

2016.07.20 VR solution

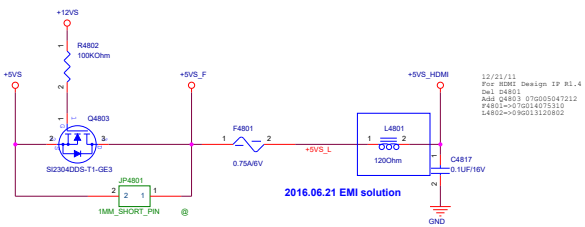


N56V C.M Choke : M 09G092090110

2015.08.26 EMI Reserve

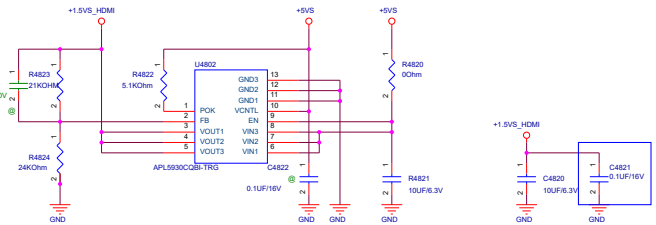


HDMI PWR_+5VS_HDMI



2016.06.21 EMI solution

HDMI LDO 1.5VS



Project Name	GL502VD		Rev 1.0
Title :	HDMI Conn.		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Ben_Fang
Date: Wednesday, February 15, 2017	Sheet 48	of	102

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

(EC to power) CPU_VRON

19 +VCCIN

CLK_PWRGD

(inversion of CLK_EN#)

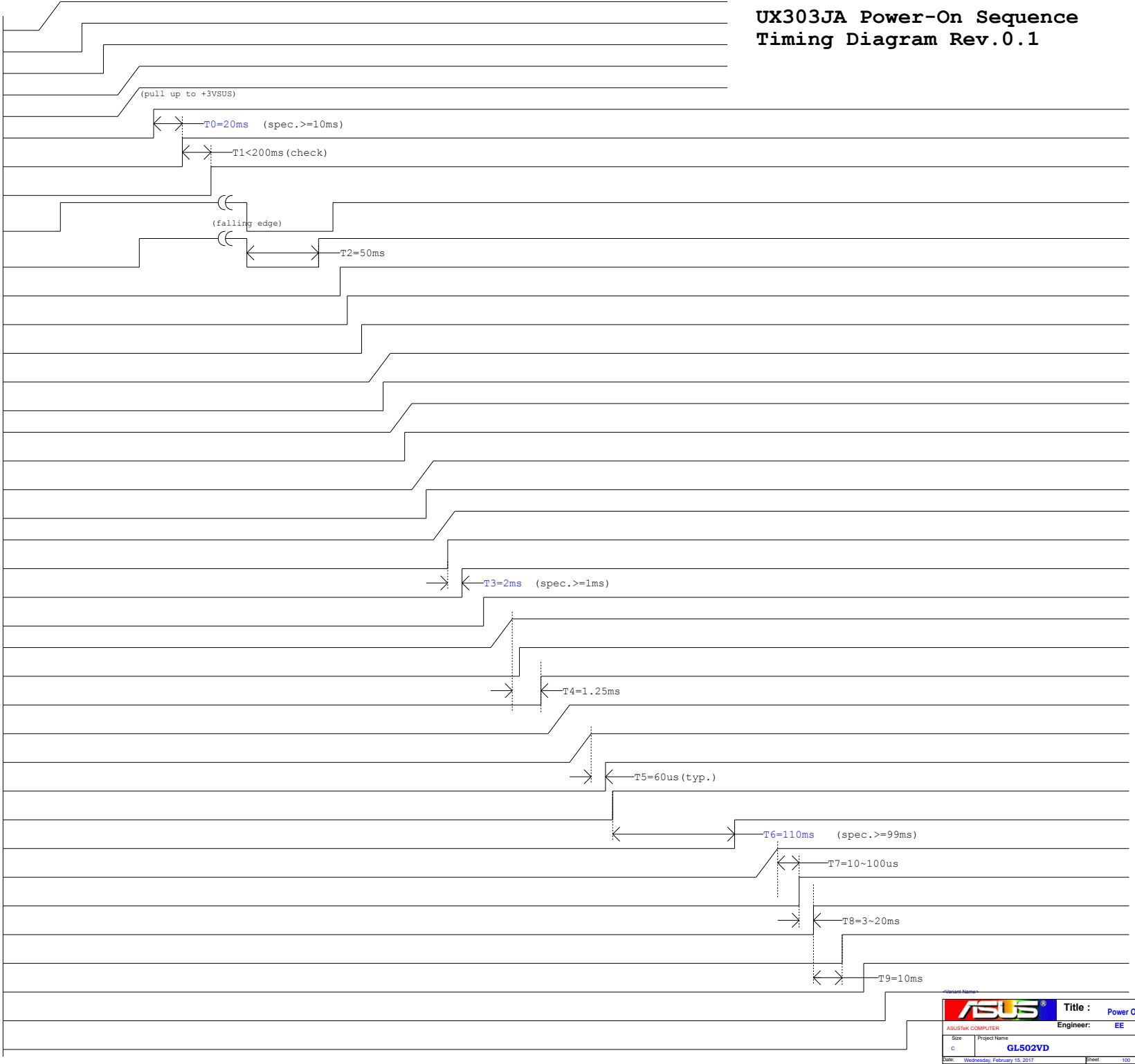
(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#



<Variant Name>

ASUSTeK COMPUTER

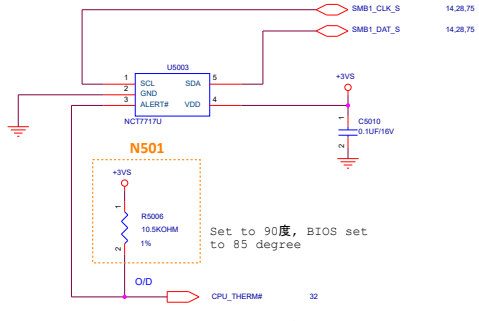
Title : Power On Timing

Engineer: EE

Size	Project Name	Rev
C	GL502VD	1.0

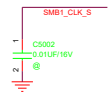
Date: Wednesday, February 15, 2017 Sheet 100 of 102

CPU Thermal Sensor

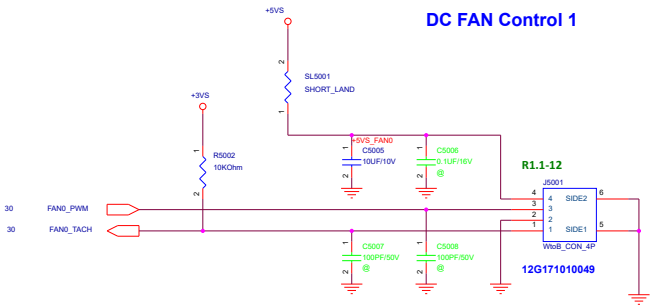


Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

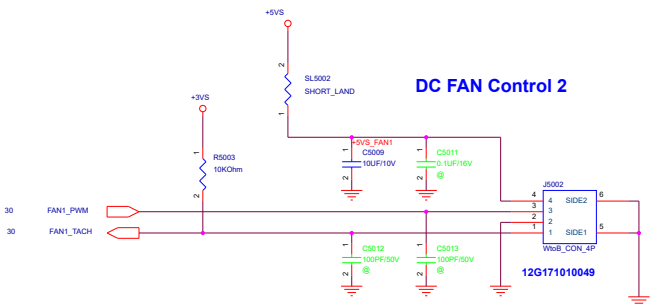
Reserve for
powr noise



DC FAN Control 1

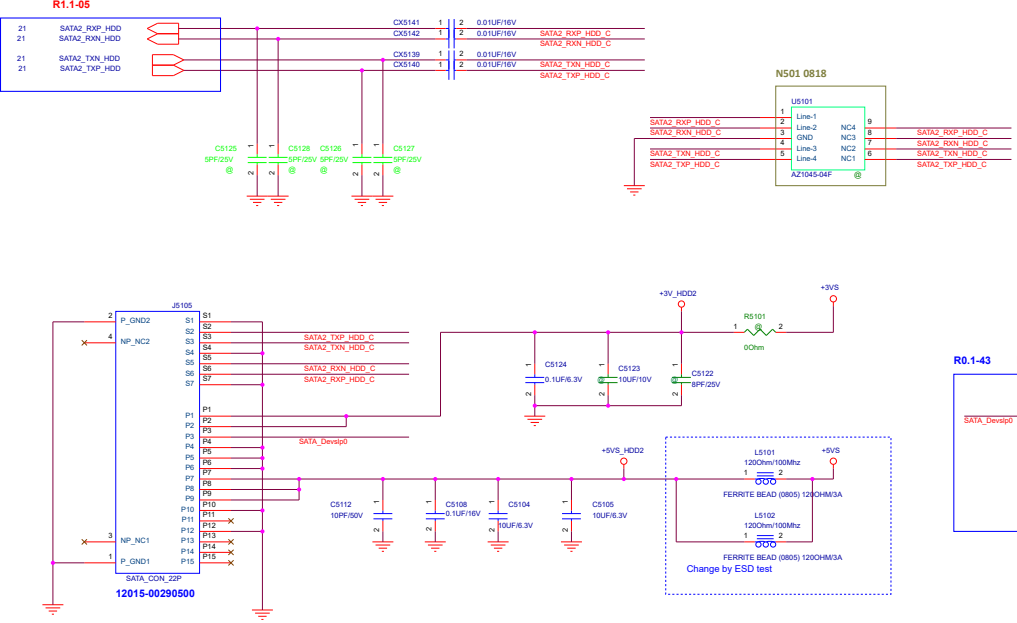


DC FAN Control 2

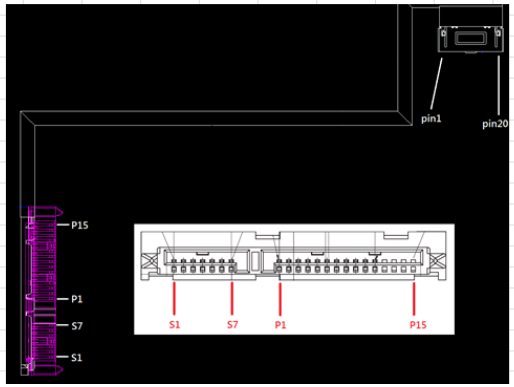


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : FAN_Thermal Sensor & Fan	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 50 of 102	



SATA Connector		
Pin	net	Note
P15	NC	
P14	NC	
P13	NC	
P12	Ground	
P11	NC	
P10	Ground	
P9	+5V	power
P8	+5V	
P7	+5V	
P6	Ground	
P5	Ground	
P4	Ground	
P3	Devslp	Impedance 50Ω
P2	+3V	power
P1	+3V	
S7	Ground	
S6	SATA_RX_P	Differential Pairs, Impedance 85Ω
S5	SATA_RX_N	Differential Pairs, Impedance 85Ω
S4	Ground	
S3	SATA_TX_N	Differential Pairs, Impedance 85Ω
S2	SATA_TX_P	Differential Pairs, Impedance 85Ω
S1	Ground	



20 pin HDD Board connector		
Pin	net	Note
pin1	Ground	
pin2	NC	
pin3	+5V	power
pin4	+5V	
pin5	+5V	
pin6	+5V	
pin7	NC	
pin8	Ground	
pin9	Devslp	Impedance 50Ω
pin10	NC	
pin11	+3V	power
pin12	+3V	
pin13	NC	
pin14	Ground	
pin15	SATA_RX_P	Differential Pairs, Impedance 85Ω
pin16	SATA_RX_N	Differential Pairs, Impedance 85Ω
pin17	Ground	
pin18	SATA_TX_N	Differential Pairs, Impedance 85Ω
pin19	SATA_TX_P	Differential Pairs, Impedance 85Ω
pin20	Ground	

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : XDD_HDD & ODD CON

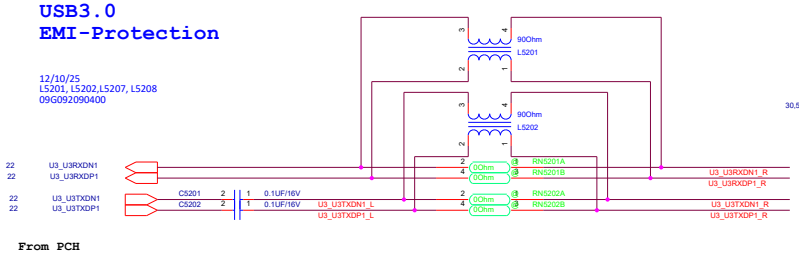
Engineer: Ben_Fang

Size: C | Project Name: GL502VD | Rev: 1.0

Date: Wednesday, February 15, 2017 | Sheet 51 of 102

USB3.0 EMI-Protection

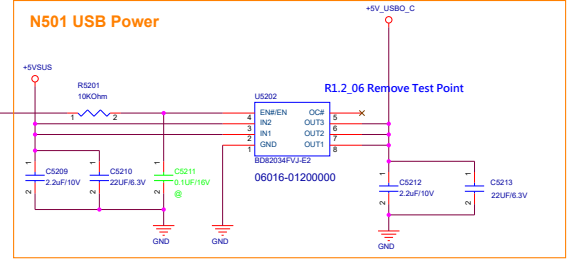
12/10/25
L5201, L5202,L5207, L5208
09G092090400



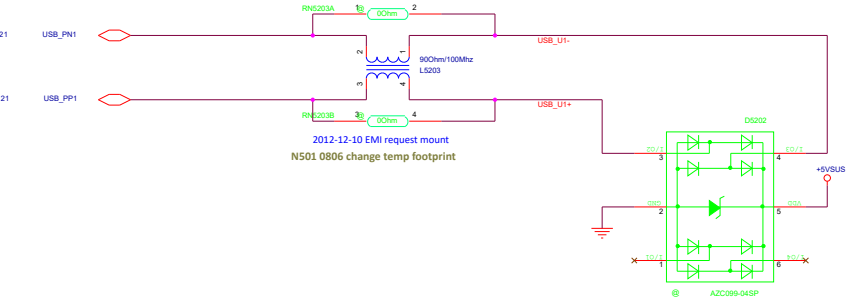
From PCH

30,57,63,69,88,97 SUSC_EC#

N501 USB Power



USB2.0 EMI-Protection

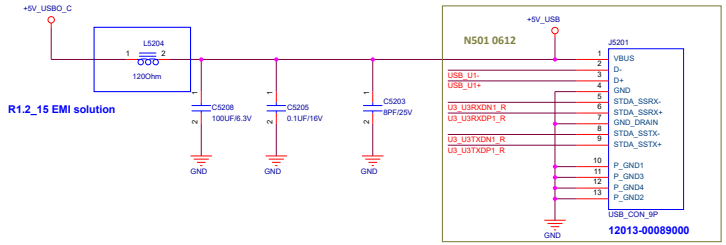


2012-12-10 EMI request mount

N501 0806 change temp footprint

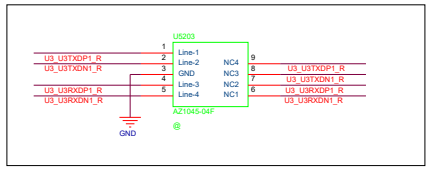
USB3.0_Port 0

N501 0808 change temp footprint



R1.2_15 EMI solution

12013-00089000



U5203 ESD PROTECTION

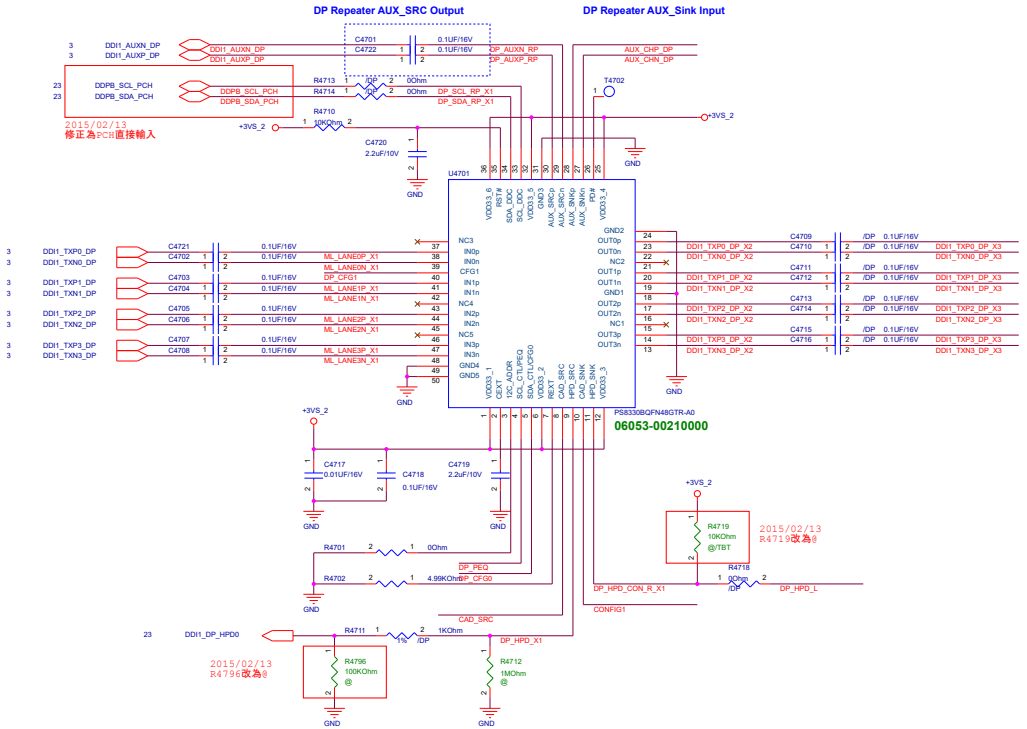
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

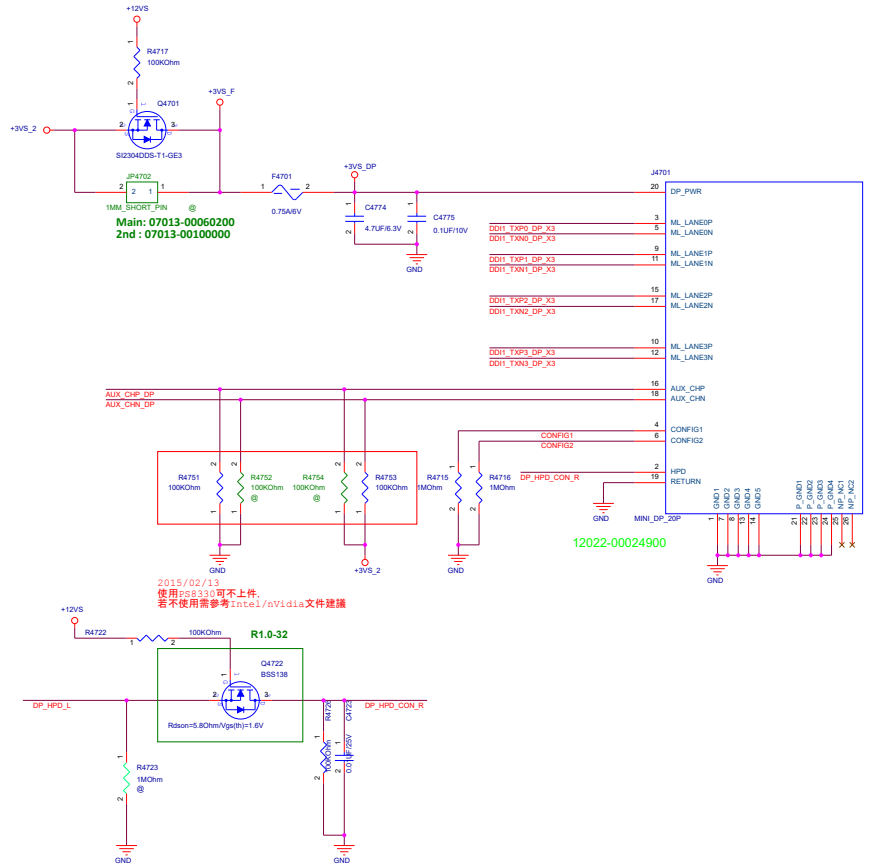
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

<Variant Name>

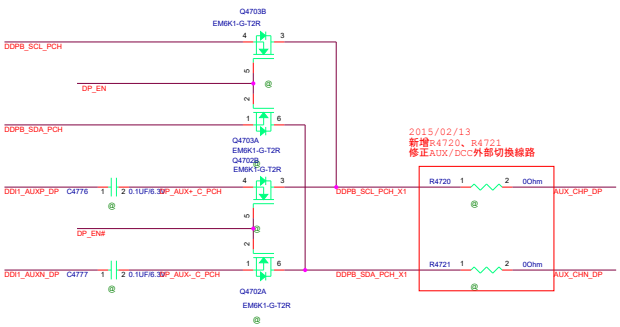
ASUSTeK COMPUTER INC. NB1	Title :	USB Charger
	Engineer:	Ben_Fang
Size: Custom	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 52 of 102	

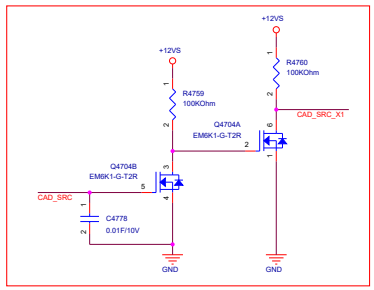
DP Repeater_PS8330B

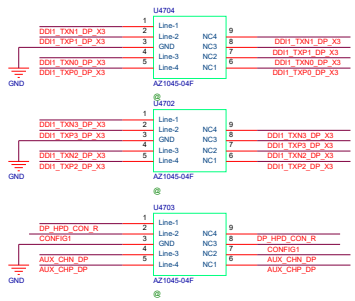


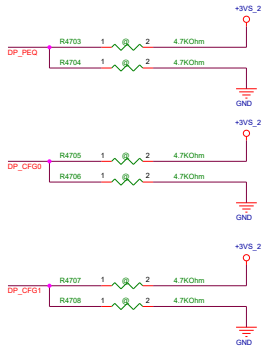


Follow SKL-H PDG 5.4.4 P150
Figure 5-13. DisplayPort*
Auxiliary Channel Dual Mode Support Protection Circuit





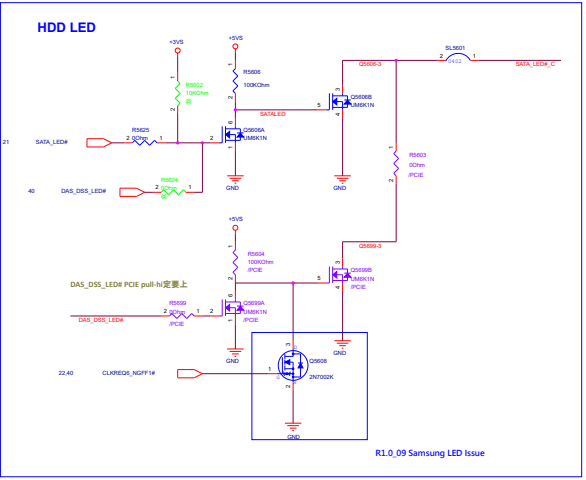


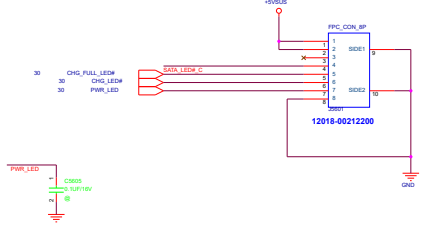


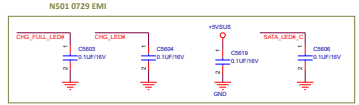
ASUS	Project Name: GL502VD		Rev: 1.0
Title :	Display Port Conn.		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ben_Fang	
Date: Wednesday, February 15, 2017	Sheet 47 of 102		

2014/05/29 Add HDD & SSD LED control circuit.

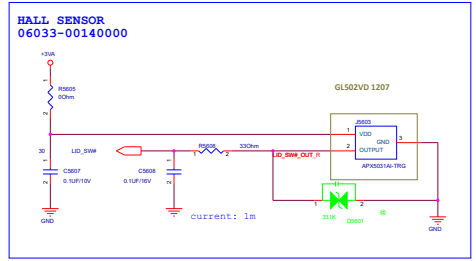
HDD LED



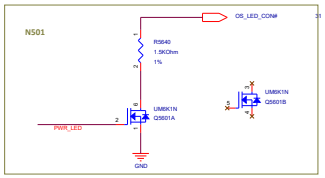




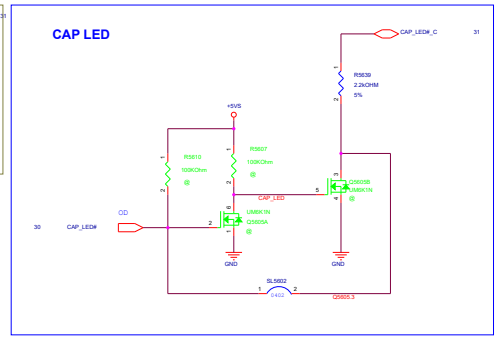
HALL SENSOR
06033-00140000



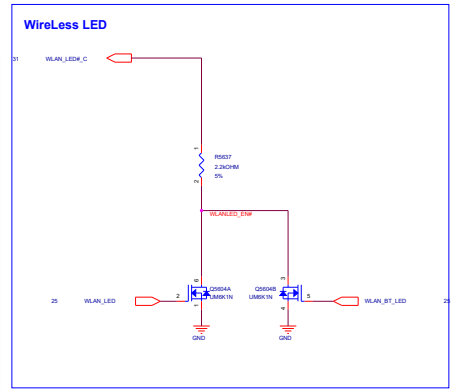
OS LED



CAP LED



WireLess LED



<Variant Name>

ASUSTeK COMPUTER INC. NB3

Title : LED & LID

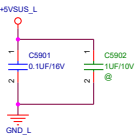
Engineer: Ben_Fang

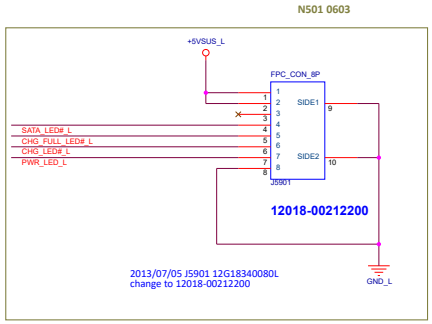
Size	Project Name	Rev
C	GL502VD	1.0

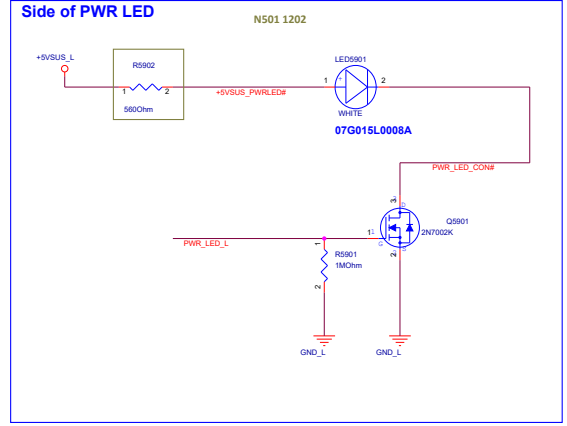
Date: Wednesday, February 15, 2017 Sheet 56 of 102

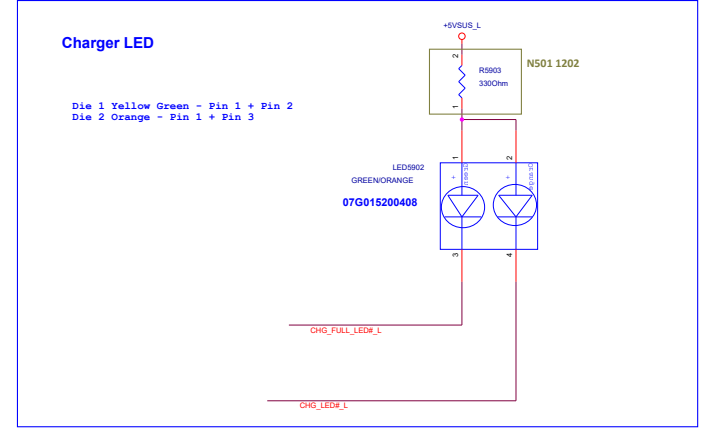
Main Board

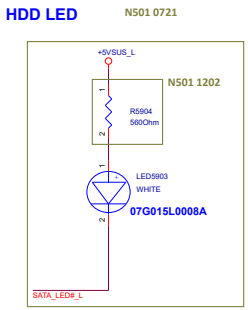
ASUS	Project Name: UX550	Rev: 1.0
Title :	POWER_+VGFX_CORE	
Size: B	Dept.: NB Power team	Engineer: EE
Date: Wednesday, February 15, 2017	Sheet 96 of 102	

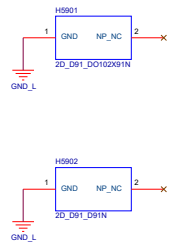


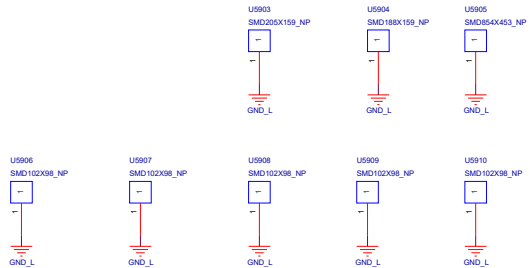


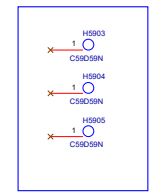




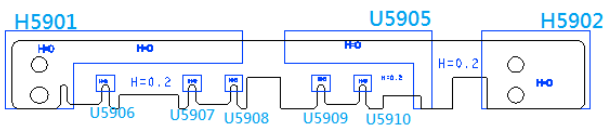


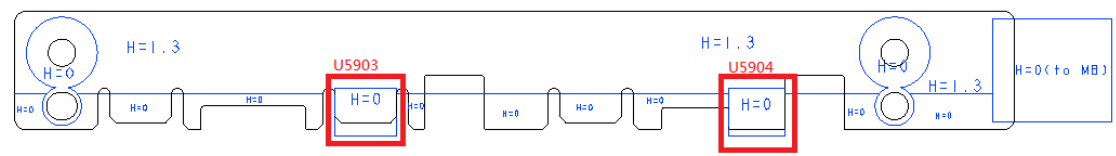






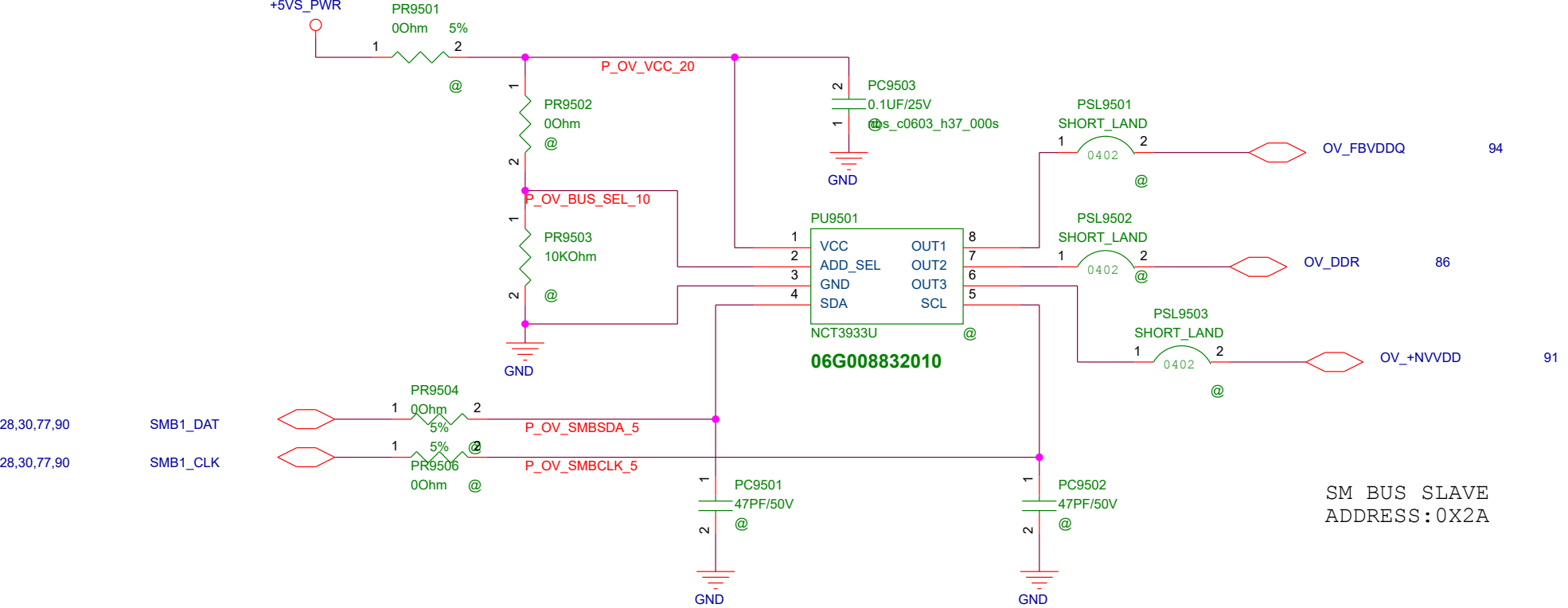
2015.11.05 add by ME





<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : I/O_Main board Conn.	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 59 of 102	



<Variant Name>

Project Name: GL502VD		Rev: R1.0
Title : PW_OV		
Size: A	Dept.: NB Power team	Engineer: Edison
Date: Wednesday, February 15, 2017	Sheet 95 of 102	

UX303JA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 13 SUSC_EC#

+0.6V/+1.2V/+1.8V/+3V/+5V

(EC to power) 14 SUSB_EC#

+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS

(power to EC) ME_+VM_PWRGD

(EC to PCH) ME_PWROK

15 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) GFX_VR_ON

16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

(power to EC) GFX_PWRGD

18 ALL_SYSTEM_PWRGD

(EC to power) CPU_VRON

19 +VCCIN

CLK_PWRGD

(inversion of CLK_EN#)

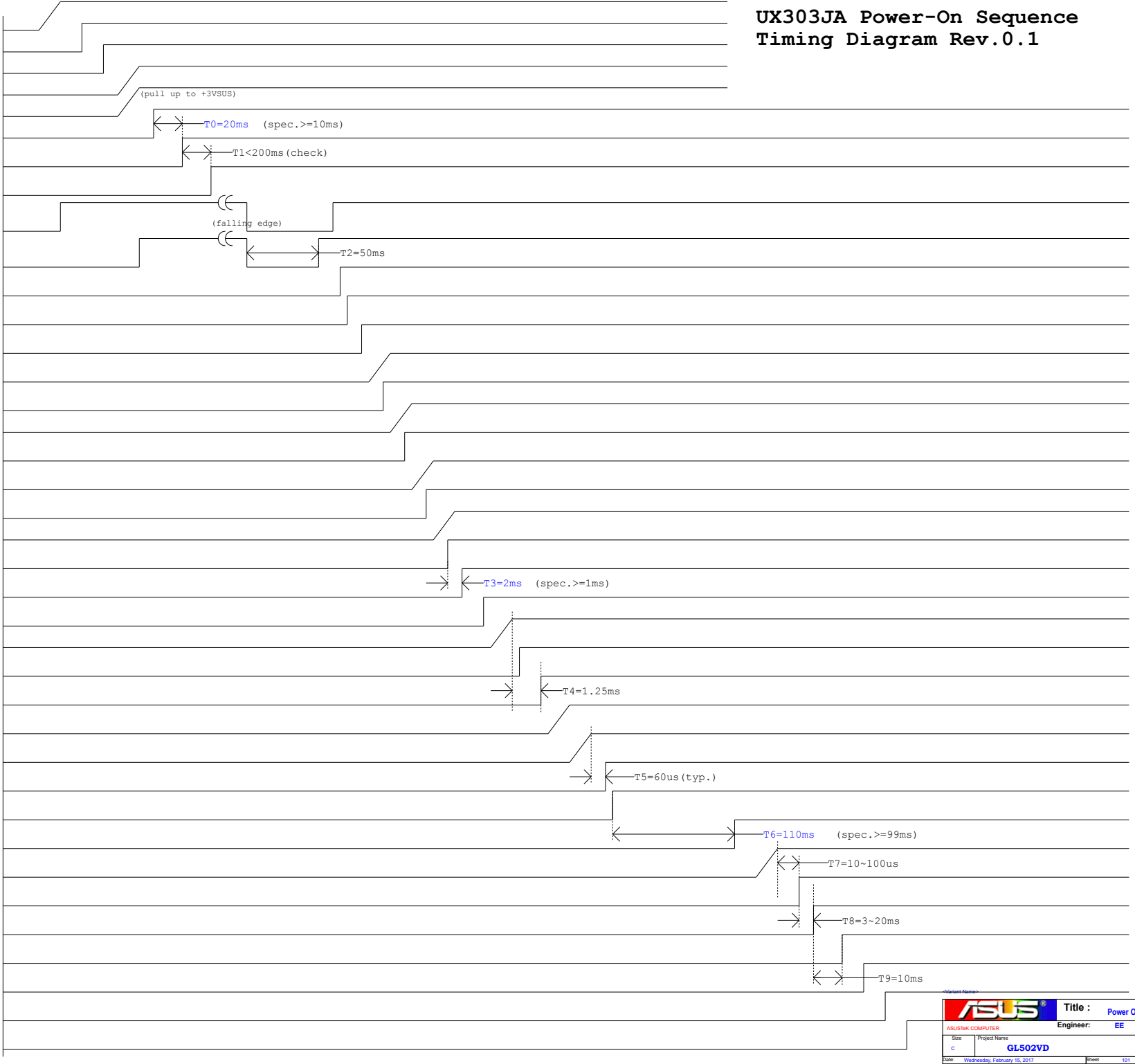
(power to EC) 20 CORE_PWRGD

(EC to PCH) 21 PM_PWROK

(PCH to CPU) H_DRAM_PWRGD

(PCH to CPU) H_CPUPWRGD

(PCH to CPU) 22 BUF_PLT_RST#



<Variant Name>

ASUSTeK COMPUTER

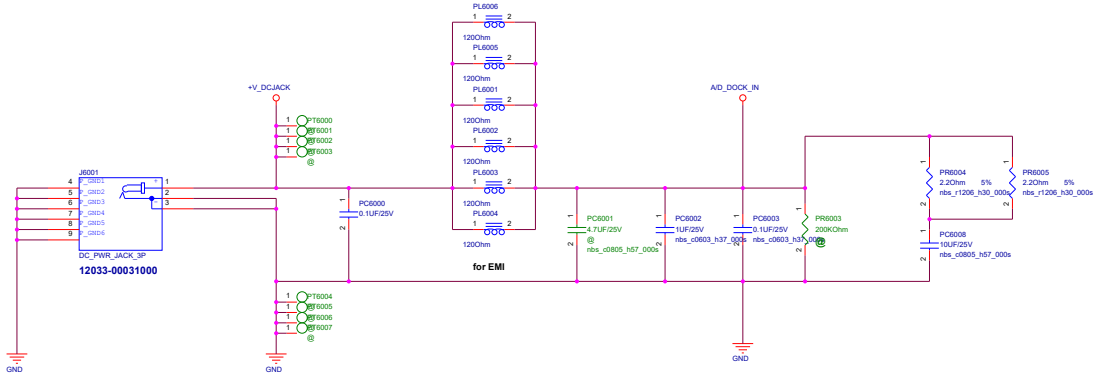
Title : Power On Timing

Engineer: EE

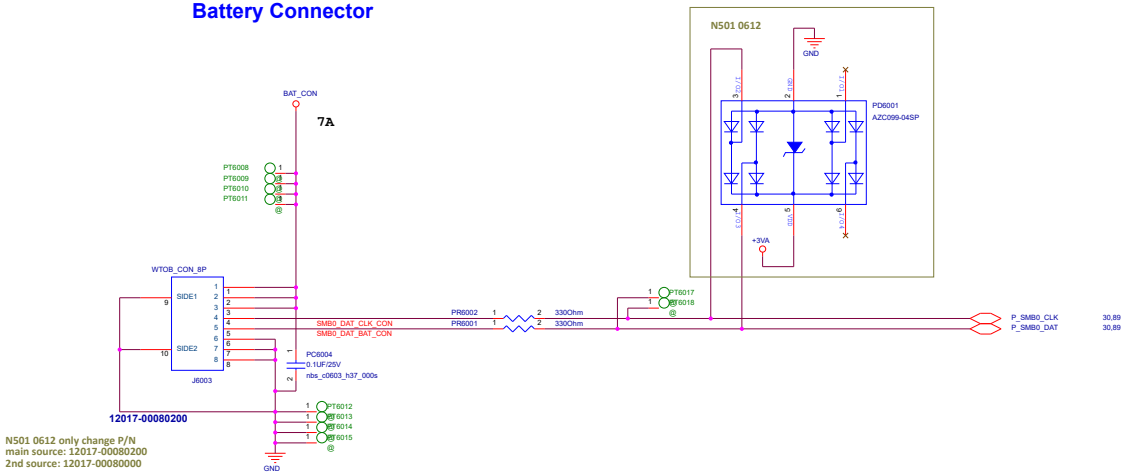
Size	Project Name	Rev
C	GL502VD	1.0

Date: Wednesday, February 15, 2017 Sheet 101 of 102

DC-IN Connector



Battery Connector



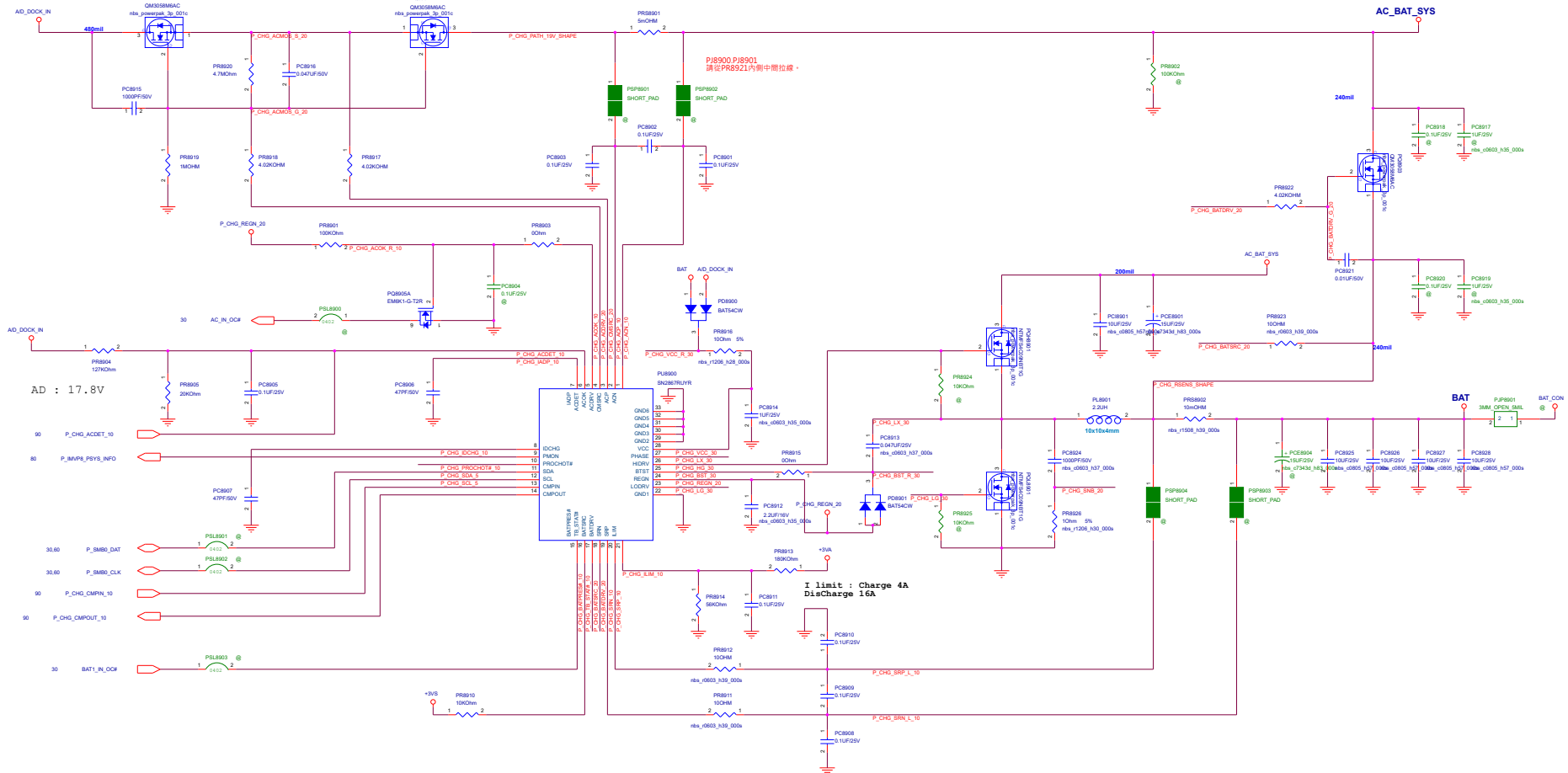
N501 0612 only change P/N
main source: 12017-00080200
2nd source: 12017-00080000

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer:		
Size: C	Project Name: GL502VD		Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 60 of 102		

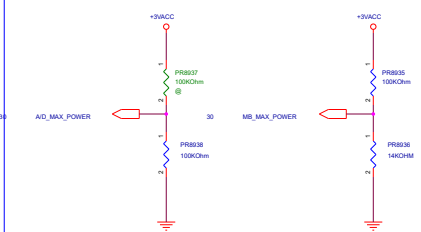
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer: Ben_Fang	
Size: A	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 61 of 102	

PRS8901	<=40W	<=120W	>=120W
	20m	10m	5m
	10125-0004m000	10G21DR01015111	10G21DR00515111



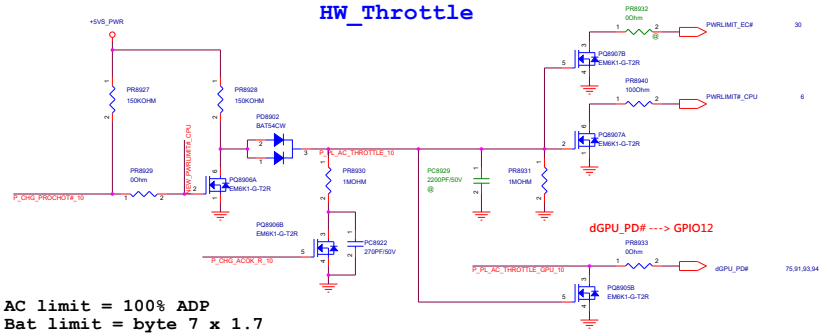
Adaptor select
total power = 90% ADP



Adaptor select

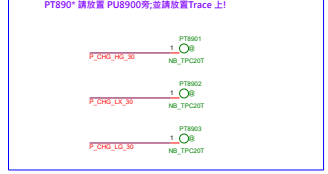
PR8936 \ PR8921	N Series 10m	G Series 5m
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle



AC limit = 100% ADP
Bat limit = byte 7 x 1.7

PT890* 請放置 PU8900旁;並請放置Trace 上!



ASUS	Project Name: GL502VD		Rev: 1.0
Title : PW_CHARGER			
Size: A2	Dept.: NB Power Team	Engineer: Edison	
Date: Wednesday, February 15, 2017	Sheet 89 of 102		

<Variant Name>

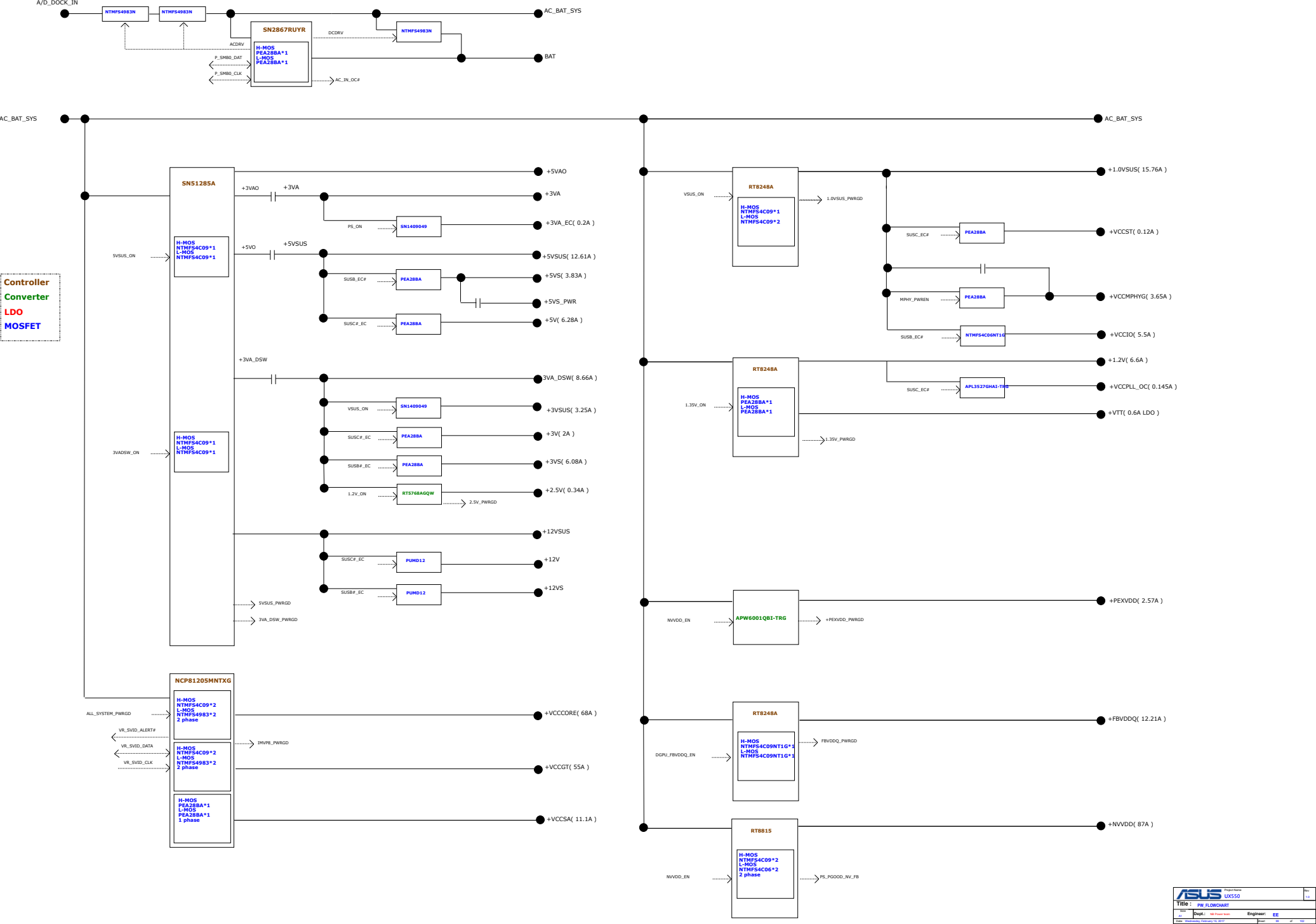
Title : I/O board(1-1)_CR_RTS5139

ASUSTeK COMPUTER INC. NB3

Engineer: Ben_Fang

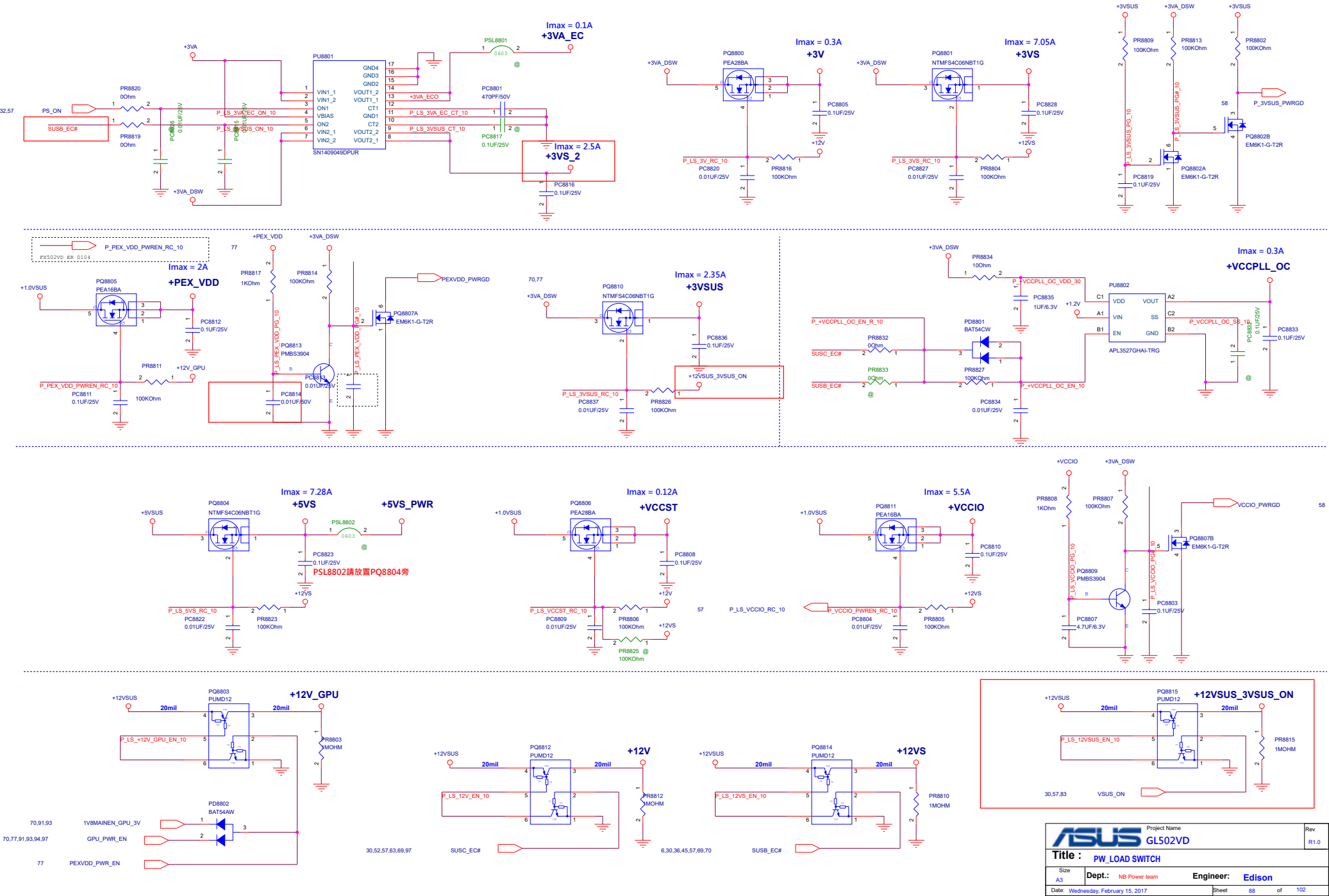
Size	Project Name	Rev
C	**GL502VD**	1.0

Date:	Wednesday, February 15, 2017	Sheet	62	of	102


A/D_DOCK_IN
NTMFS4983N
NTMFS4983N
AC_BAT_SYS
SN2867RUYR
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
ACDRV
DCDRV
NTMFS4983N
BAT
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
AC_BAT_SYS
SN51285A
+5VAO
+3VAO
+3VA
+3VA
PS_ON
SN1409049
+3VA_EC(0.2A)
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C09*1
5VSUS_ON
+5VO
+5VSUS
+5VSUS(12.61A)
SUSB_EC#
PEA28BA
+5VS(3.83A)
+5VS_PWR
SUSC#_EC
PEA28BA
+5V(6.28A)
+3VA_DSW
3VA_DSW(8.66A)
VSUS_ON
SN1409049
+3VSUS(3.25A)
SUSC#_EC
PEA28BA
+3V(2A)
SUSB#_EC
PEA28BA
+3VS(6.08A)
1.2V_ON
RT5768AGQW
+2.5V(0.34A)
2.5V_PWRGD
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C09*1
3VADSW_ON
+12VSUS
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
5VSUS_PWRGD
3VA_DSW_PWRGD
NCP81205MNTXG
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
2 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
IMVP8_PWRGD
+VCCCORE(68A)
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
2 phase
+VCCGT(55A)
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
1 phase
+VCCSA(11.1A)
Controller
Converter
LDO
MOSFET
AC_BAT_SYS
RT8248A
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C09*2
VSUS_ON
1.0VSUS_PWRGD
+1.0VSUS(15.76A)
SUSC_EC#
PEA28BA
+VCCST(0.12A)
MPHY_PWREN
PEA28BA
+VCCMPHYG(3.65A)
SUSB_EC#
NTMFS4C06NT1G
+VCCIO(5.5A)
RT8248A
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
1.35V_ON
1.35V_PWRGD
+1.2V(6.6A)
SUSC_EC#
APL3527GHAI-TRG
+VCCPLL_OC(0.145A)
+VTT(0.6A LDO)
NVVDD_EN
APW6001QBI-TRG
+PEXVDD_PWRGD
+PEXVDD(2.57A)
RT8248A
H-MOS
NTMFS4C09NT1G*1
L-MOS
NTMFS4C09NT1G*1
DGPU_FBVDDQ_EN
FBVDDQ_PWRGD
+FBVDDQ(12.21A)
RT8815
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4C06*2
2 phase
NVVDD_EN
PS_PGOOD_NV_FB
+NVVDD(87A)
ASUS
Project Name
UX550
Rev
1.0
Title :
PW_FLOWCHART
Size
A4
Dept.:
MB Power team
Engineer:
EE
Date: Wednesday, February 15, 2017
Sheet
80
of
150

Load Switch

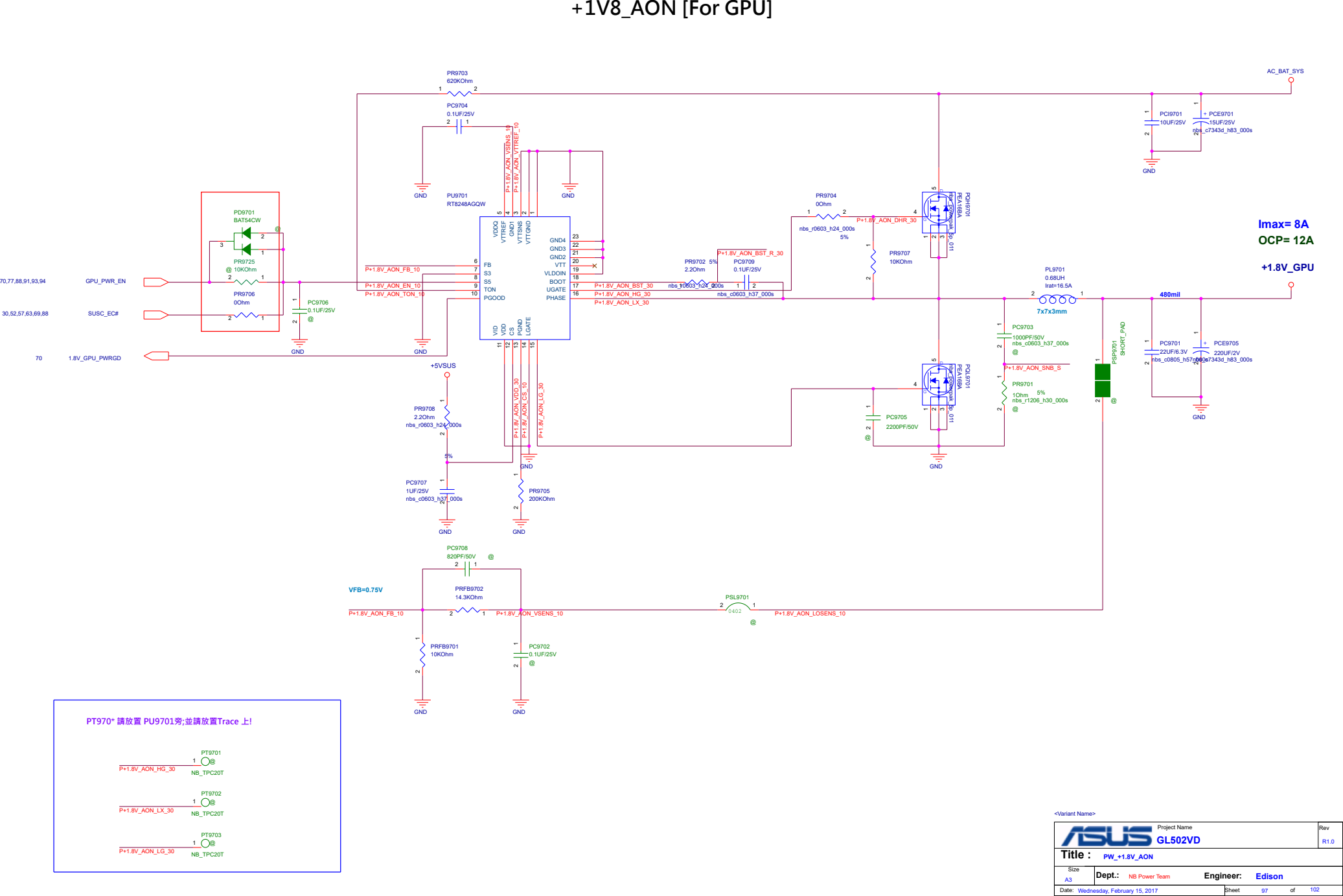
Main Board



Project Name	GL502VD	Rev	R1.0
Title :	PW_LOAD SWITCH		
Size	A3	Dept.: NB Power team	Engineer: Edison
Date:	Wednesday, February 15, 2017	Sheet	88 of 102

ASUS	Project Name: UX550	Rev: 1.0
Title :	POWER_+VGFX_CORE	
Size: Custom	Dept.: NB Power team	Engineer: EE
Date: Wednesday, February 15, 2017	Sheet 98 of 102	

+1V8_AON [For GPU]



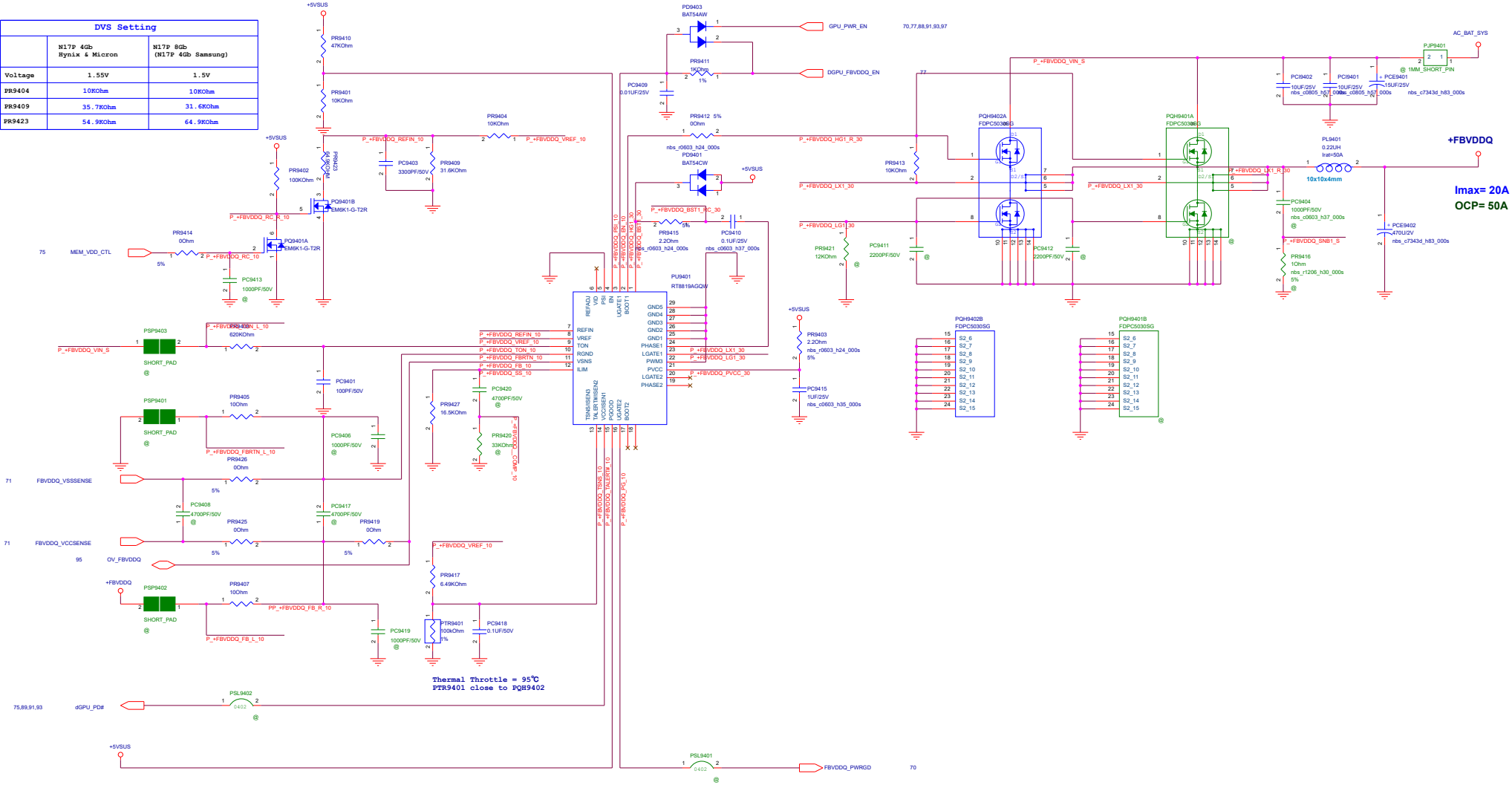
PT970* 請放置 PU9701旁;並請放置Trace 上!

<Variant Name>

Project Name: GL502VD		Rev: R1.0
Title : PW_+1.8V_AON		
Size: A3	Dept.: NB Power Team	Engineer: Edison
Date: Wednesday, February 15, 2017	Sheet 97 of 102	

+FBVDDQ [For VRAM]

DVS Setting		
	N17P 4Gb Hynix & Micron	N17P 8Gb (N17P 4Gb Samsung)
Voltage	1.55V	1.5V
PR9404	10KOhm	10KOhm
PR9409	35.7KOhm	31.6KOhm
PR9423	54.9KOhm	64.9KOhm



PT940* 請放置 PU9401旁;並請放置Trace 上!

PT9401 — P_+FBVDDQ_HG1_30 — NB_TPC20T

PT9402 — P_+FBVDDQ_LX1_30 — NB_TPC20T

PT9403 — P_+FBVDDQ_LG1_30 — NB_TPC20T

<Variant Name>

ASUS	Project Name: GL502VD	Rev: R1.0
Title : PW_+FBVDDQ		
Size: C	Dept.: NB Power Team	Engineer: Edison
Date: Wednesday, February 15, 2017	Sheet 94 of 102	

Project Name

GL502VD

Rev

R1.0

Title : PW_

Size

A3

Dept.: NB Power team

Engineer: Edison

Date: Wednesday, February 15, 2017

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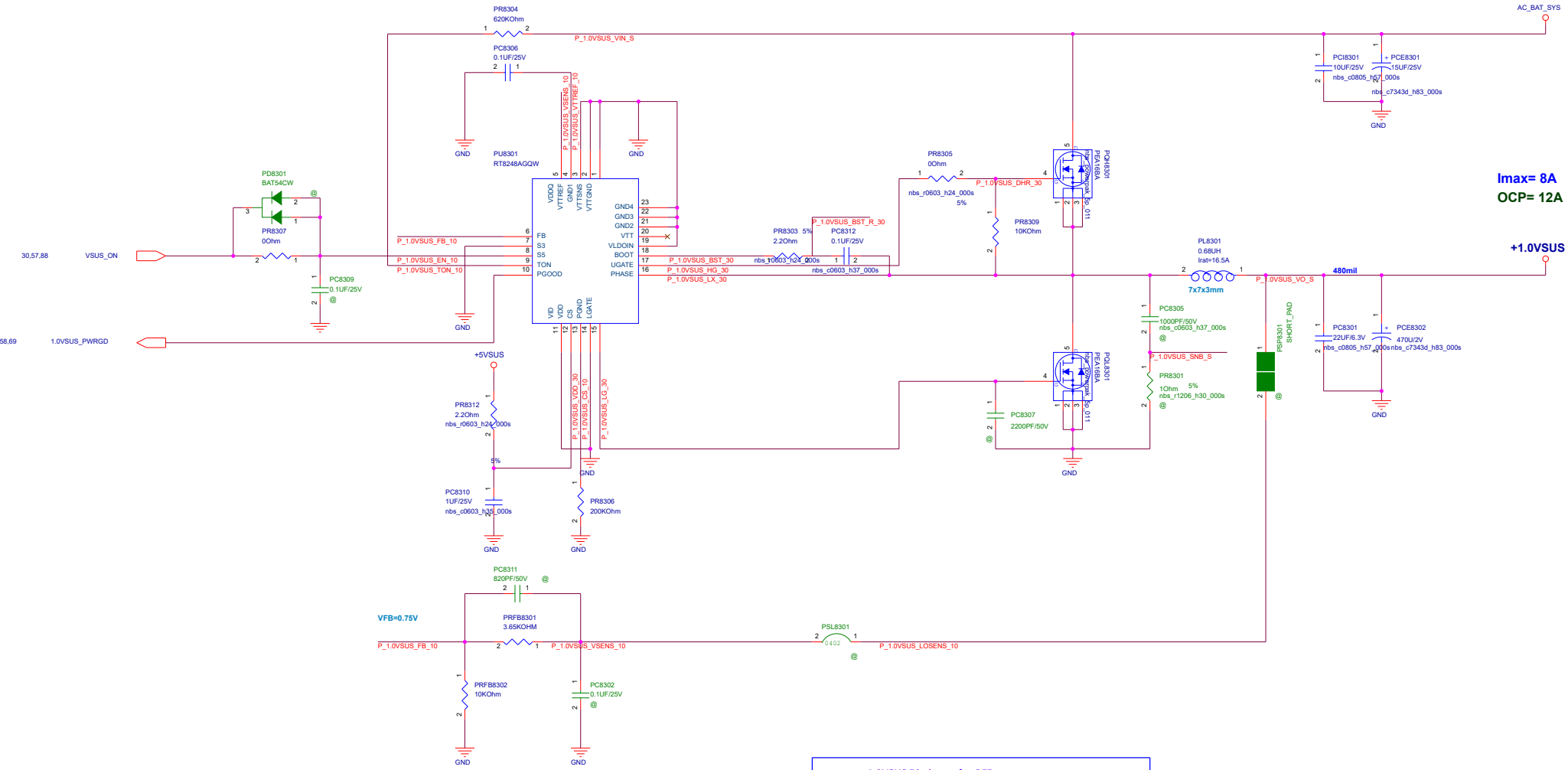
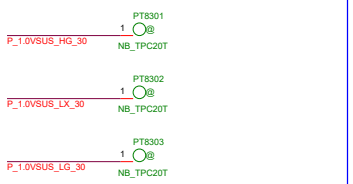
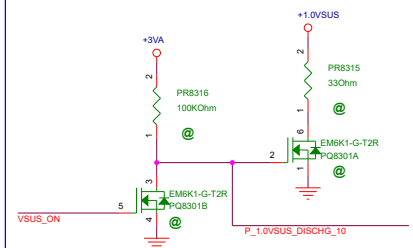
+1.0VSUS [For PCH]



PT830* 請放置 PU8301旁;並請放置Trace 上!

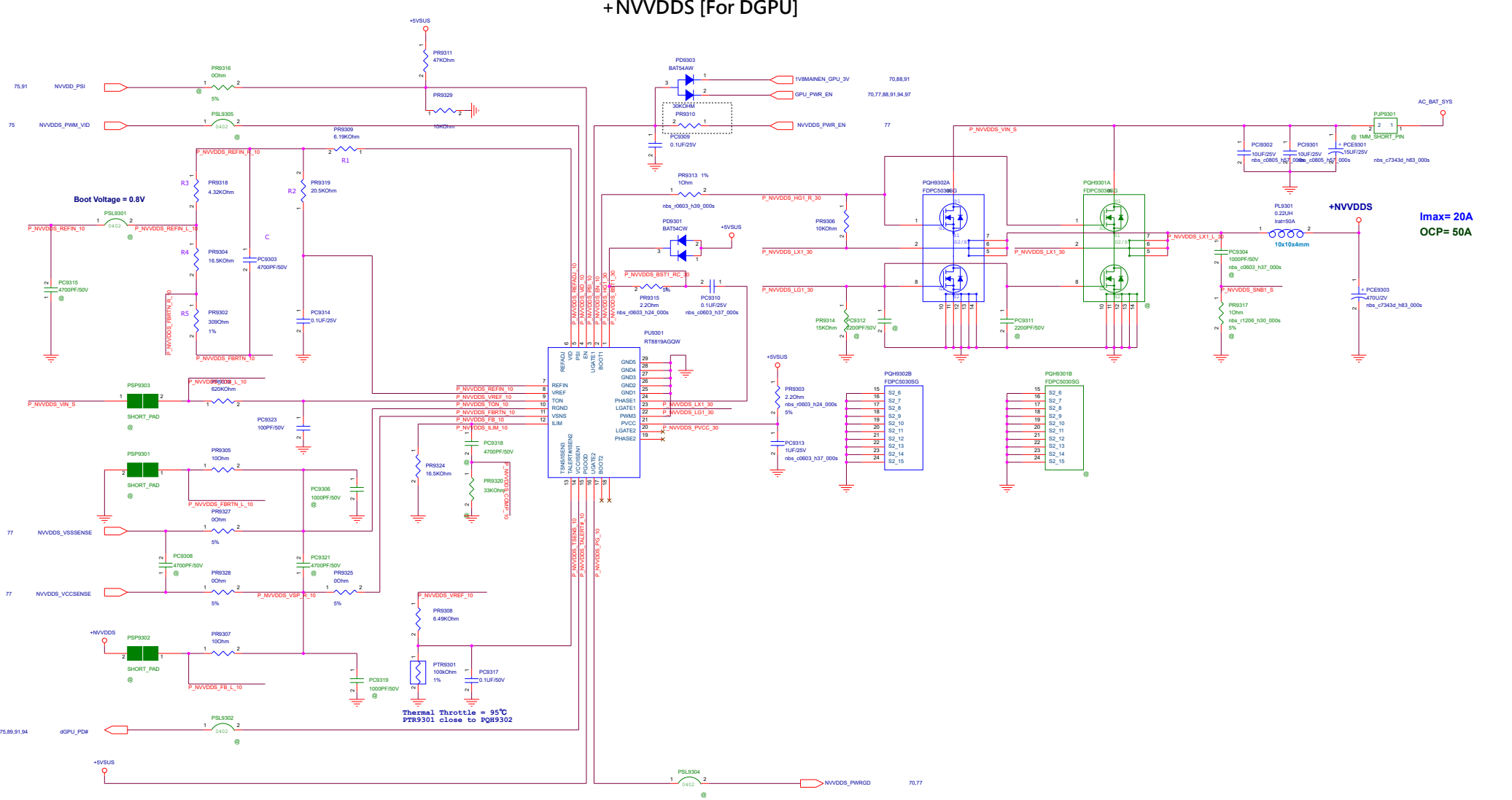


+1.0VSUS Discharge for OFF sequence



Project Name: GL502VD			Rev: R1.0
Title : PW_+1.0VSUS			
Size: A3	Dept.: NB Power team	Engineer: Edison	
Date: Wednesday, February 15, 2017	Sheet 83 of 102		

+NVVDDS [For DGPU]



Project Name

UX550

Rev

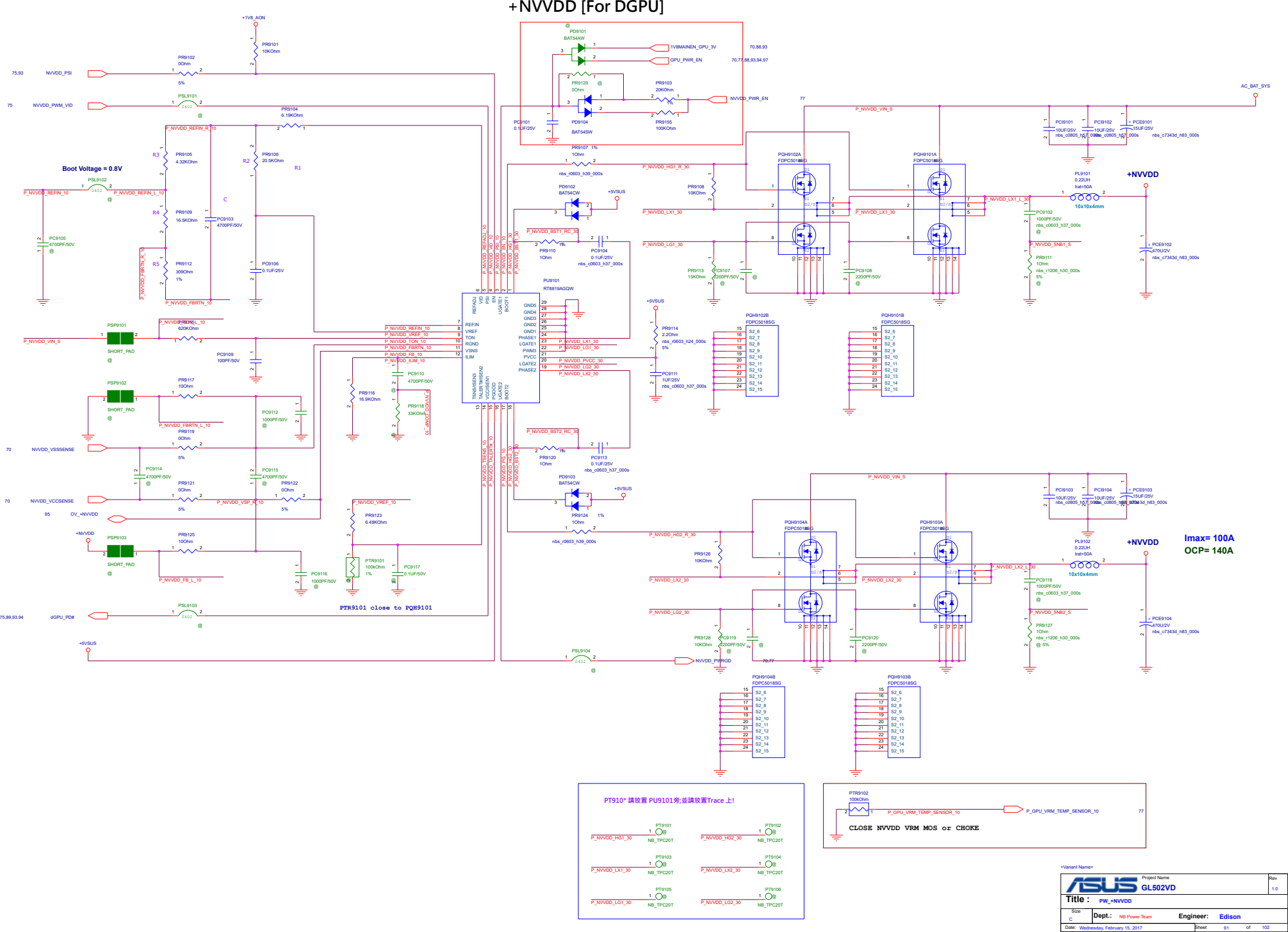
1.0

Title : PW_PEX_VDD

Size	Dept.:	Engineer:
A3	NB Power team	Joe

Date:	Sheet	of
Wednesday, February 15, 2017	92	102

+NVVDD [For DGPU]

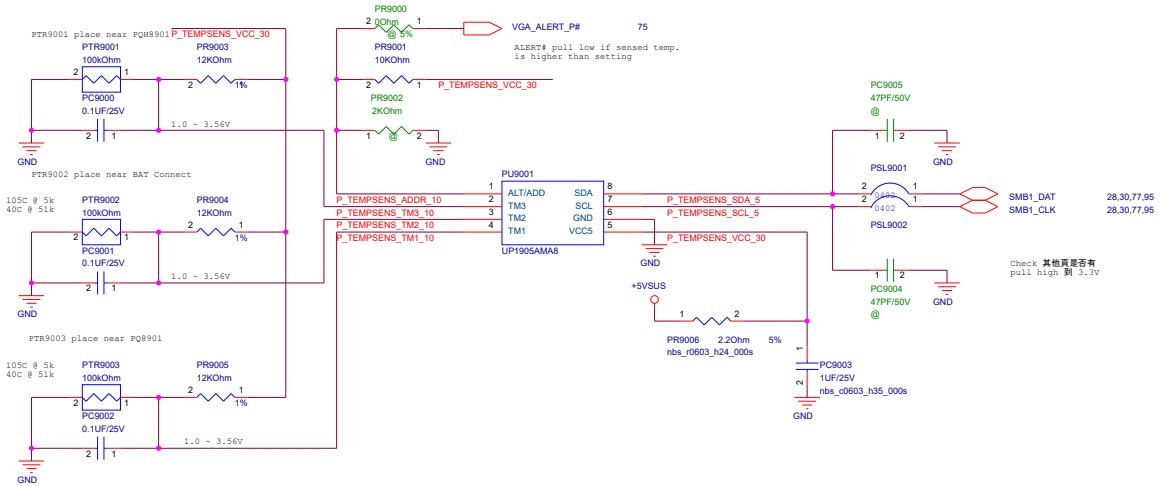


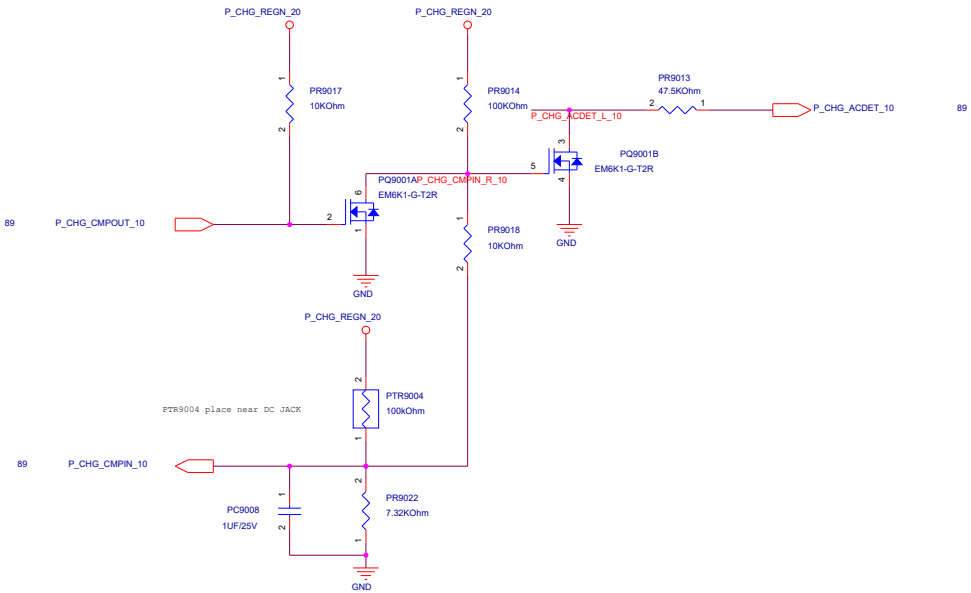
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert





<Variant Name>

ASUS	Project Name: GL502VD	Rev: R1.0
Title : PW_PROTECTION		
Size: A3	Dept.: NB Power Team	Engineer: Edison
Date: Wednesday, February 15, 2017	Sheet 90 of 102	

Title : SBU_DGPU_*****_R0.9

ASUSTeK COMPUTER

Engineer: Ben_Fang

Size	Project Name	Rev
B	GL502VD	1.0

Date: Wednesday, February 15, 2017 Sheet 79 of 102

NVVDD Backside cap(pcs)				
	NVIDIA		UX502	
	N16	N17	N16	N17
0.1uF	10	0	10	0
1uF	4	10	4	10
10uF	2	4	2	4
22uF				

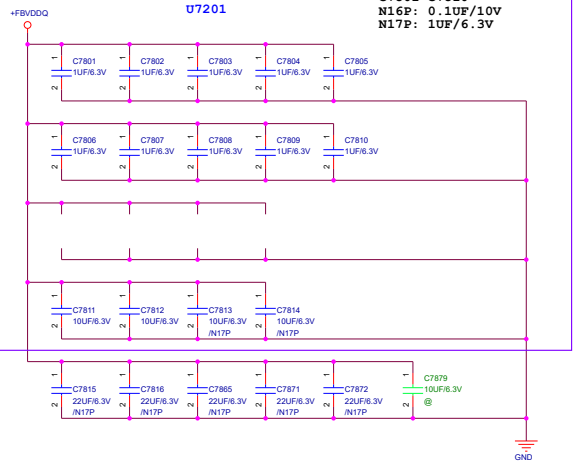
Location is close to DRAM for clamshell mode

0.1uF*10 (only N16P)
1uF*4(N16P) *10(N17P)
10uF*5
22uFX5

0.1uF*10,1uF*4,10uF*4 place under VRAM

U7201

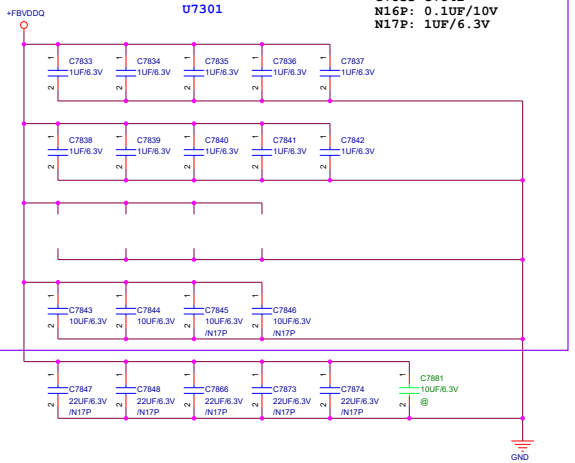
C7801~C7810
N16P: 0.1UF/10V
N17P: 1UF/6.3V



0.1uF*10,1uF*4,10uF*4 place under VRAM

U7301

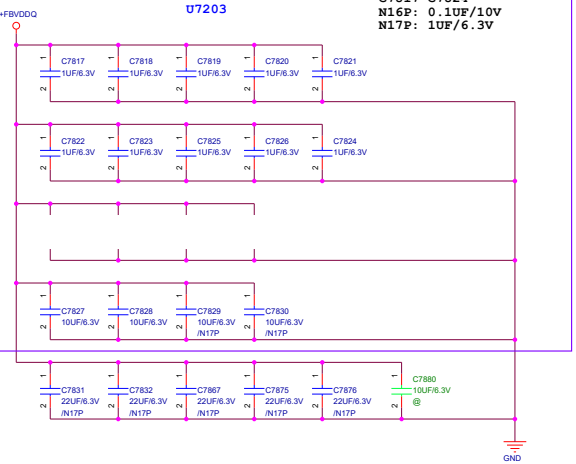
C7833~C7842
N16P: 0.1UF/10V
N17P: 1UF/6.3V



0.1uF*10,1uF*4,10uF*4 place under VRAM

U7203

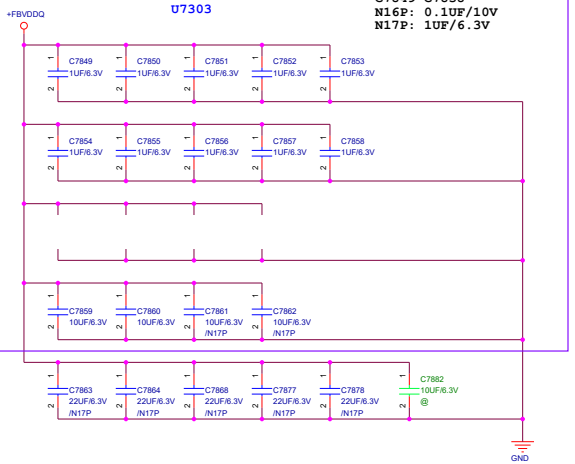
C7817~C7824
N16P: 0.1UF/10V
N17P: 1UF/6.3V



0.1uF*10,1uF*4,10uF*4 place under VRAM

U7303

C7849~C7858
N16P: 0.1UF/10V
N17P: 1UF/6.3V



<Variant Name>

ASUSTeK COMPUTER

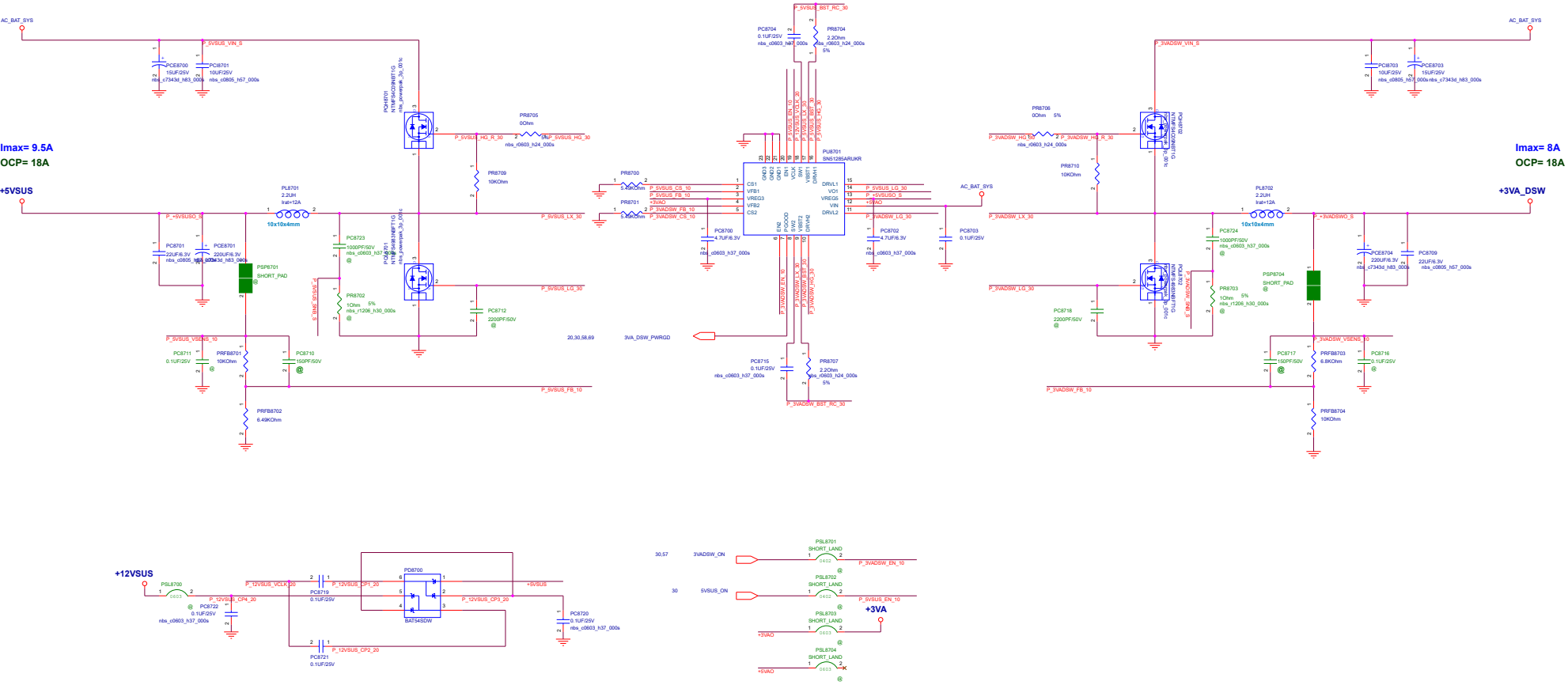
Title : VRAM CAP

Engineer: Ben_Fang

Size	Project Name	Rev
C	GL502VD	1.0

Date: Wednesday, February 15, 2017 Sheet 78 of 102

+3VA_DSW / +5VSUS [System Power]



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

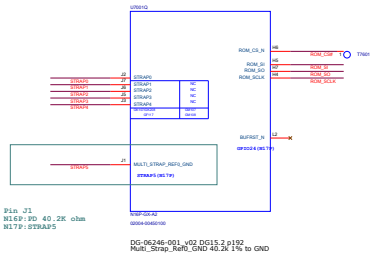
Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!

<variant Name>

Project Name: GL502VD			Rev: R1.0
Title: PW_+3VA_DSW/+5VSUS			
Size: A2	Dept.: NB Power team	Engineer: Edison	
Date: Wednesday, February 15, 2017	Sheet 87 of 102		



XTAL

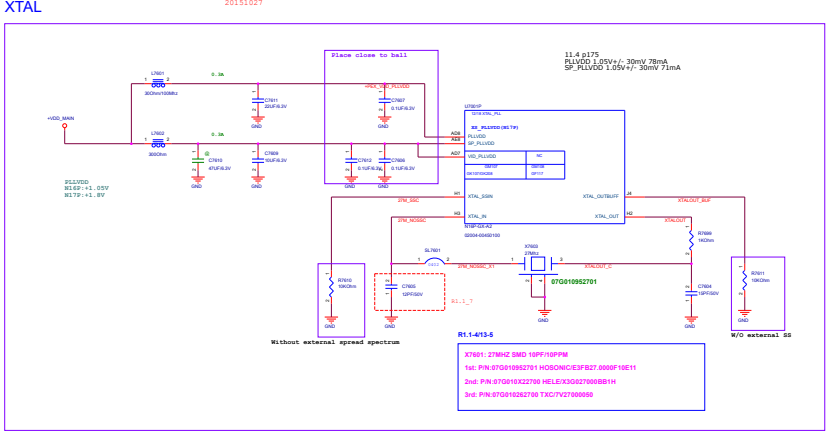
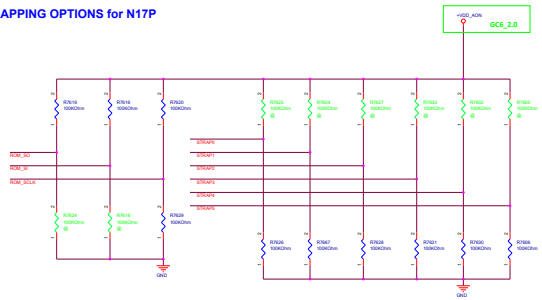


Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

STRAPPING OPTIONS for N17P



N17P Strap use 100Kohm

N17P USE GDDR5 VRAM 256Mb x 32 (1024MB)

VRAM Source	STRAP2	STRAP1	STRAP0	RAMCFG Setting	
03008-00050400 MICRON/MT51J256M32HF-70:A	L	L	H	0x1	256Mb x 32 (1024MB) *4 pcs
03008-00051100 HYNIX/H5GC8H24MJR-R0C	L	H	L	0x2	
03008-00031000 SAMSUNG/K4G41325FE-HC28	H	H	H	0x7	128Mb x 32 (512MB) *4 pcs
03008-00030800 ELPIDA/EDW4032BABG-70-F-D	L	L	M	0x8	

	STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
	L	L	L	0	0	0	0
	L	L	H	0	0	0	1

N17P SORx_EXPOSED Strap

Row Index	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
8	H	H	H	ENABLE	DISABLE	DISABLE	DISABLE
0	H	H	M	DISABLE	DISABLE	DISABLE	DISABLE

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Notes:
1. For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
2. N17P-Gx runs WCLK up to 3000 MHz with FBVDD = 1.35V. DVS is required to run WCLK > 3000 MHz.

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDM, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is eDP Supported on:			See This Row of Table 5.5
		IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	12
3	3	--	--	--	11
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	yes	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

STRAPPING OPTIONS for N16P

DG-07158-001_v05_secured p.197
Table 15-3. GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print fot pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kohm pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print fot pull-up to 3V3_AON and pull-down to GND. Do not Stuff.			

Table 15-2.

	PU	PD
4.99Kohm	1000	0000
10.0Kohm	1001	0001
15.0Kohm	1010	0010
20.0Kohm	1011	0011
24.9Kohm	1100	0100
30.1Kohm	1101	0101
34.8Kohm	1110	0110
45.3Kohm	1111	0111

	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

Change R7615 & R7606 VRAM Vendor

USE GDDR5 VRAM 128Mb x 32 (512MB)

Samsung strap 0x3 Samsung/K4G41325FC-HC03 - pull-down 20Kohm +1.35V

Micron strap 0x4 Micron/EDW4032BABG-60-F - pull-down 24.9Kohm +1.35V

USE GDDR5 VRAM 256Mb x 32 (1024MB)

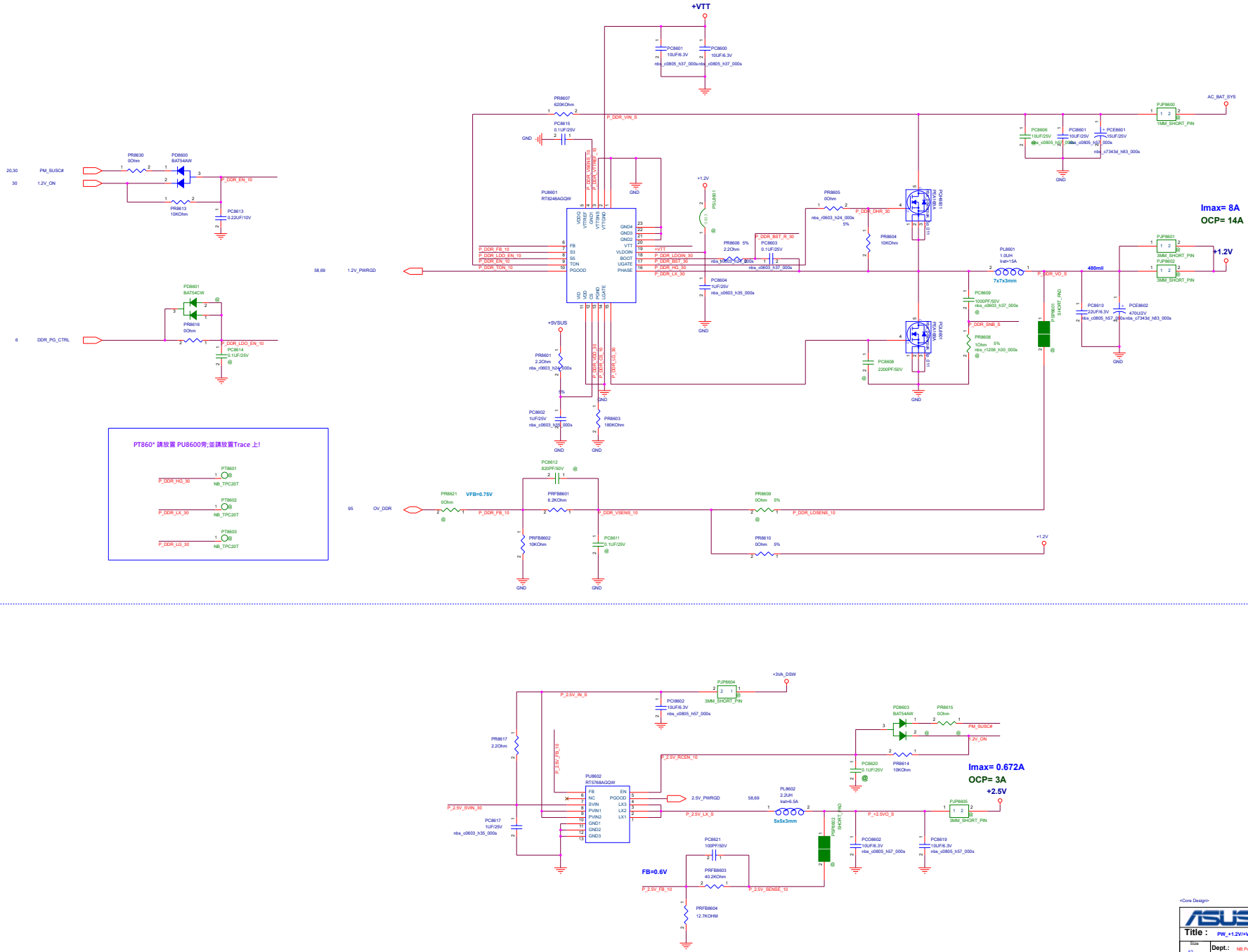
Micron strap 0x9 MICRON/MT51J256M32HF-60:A - pull-up 10Kohm +1.35V

Samsung strap 0x8 SAMSUNG/K4G80325FB-HC03 - pull-up 4.99Kohm +1.35V

<Variant Name>

ASUSTeK COMPUTER | Title : VGA_XTALSTRAPPING(1) | Engineer: Ben_Fang | Size: D | Project Name: GL502VD | Rev: 1.0 | Date: Wednesday, February 15, 2017 | Sheet 76 of 102

+1.2V / +VTT / +2.5V[For Memory]



<Core Design>

ASUS	Project Name: GL502VD		Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: Edison	
Date: Wednesday, February 15, 2017	Sheet: 86 of 102		

Project Name

GL502

Rev

1.0

Title : POWER_+VGFX_CORE

Size	Dept.:	Engineer:
A	NB Power team	Edison

Date: Wednesday, February 15, 2017

DG-07158-001_v05_secured Table 12-2.

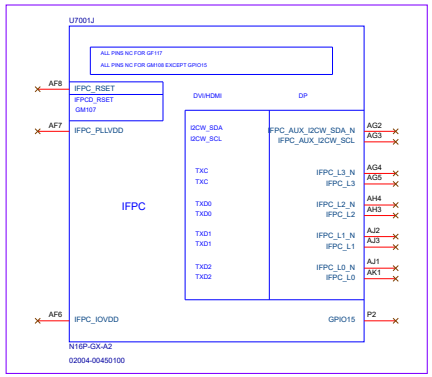
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	OUT		NVVDD_PWM_VID
1	OUT		GC6_FB_EN
2	OUT		GPU_EVENT# /WAKE*
3	OUT		VDDS_PWM
4	OUT		1V8_MAIN_EN
5	OUT		FRM_LCK
6	IN		NVVDD_PSI
7	OUT		LCD_BL_PWM
8	IN		MEM_VDD_CTL
9	I/O		THERM_ALERT
10	OUT		MEM_VREF_CTL
11	OUT		LCD_VDD
12	IN		PWR_LEVEL
13	OUT		LCD_BLEN
14	IN		HPD_IFPA
15	IN		HPD_IFPB
16	IN		SYS_PEX_RST_MON#
17	IN		HPF_IFPD
18	IN		HPD_IFPE
19	IN		3D VISION/STEREO
20			NVVDDS_PSI
21	OUT		UNUSED
OVERT	I/O	High	OVERT

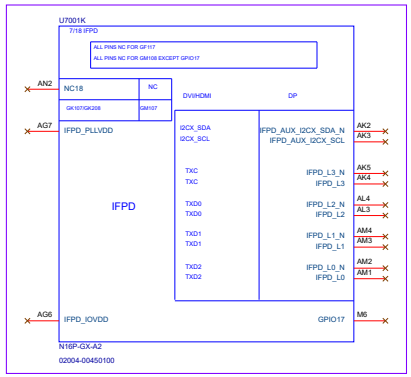
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

DG-06246-001_v02 p157 DG8.6
IPF not used
IFPxy_IOCDD/IFPxy_PLLVDD 10K PD
Other pin NC

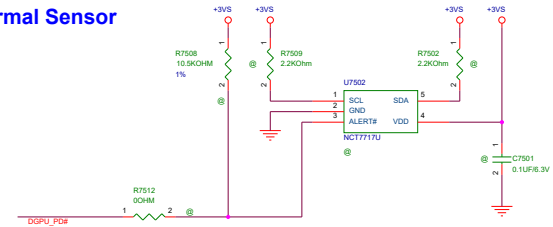
DP(link C)



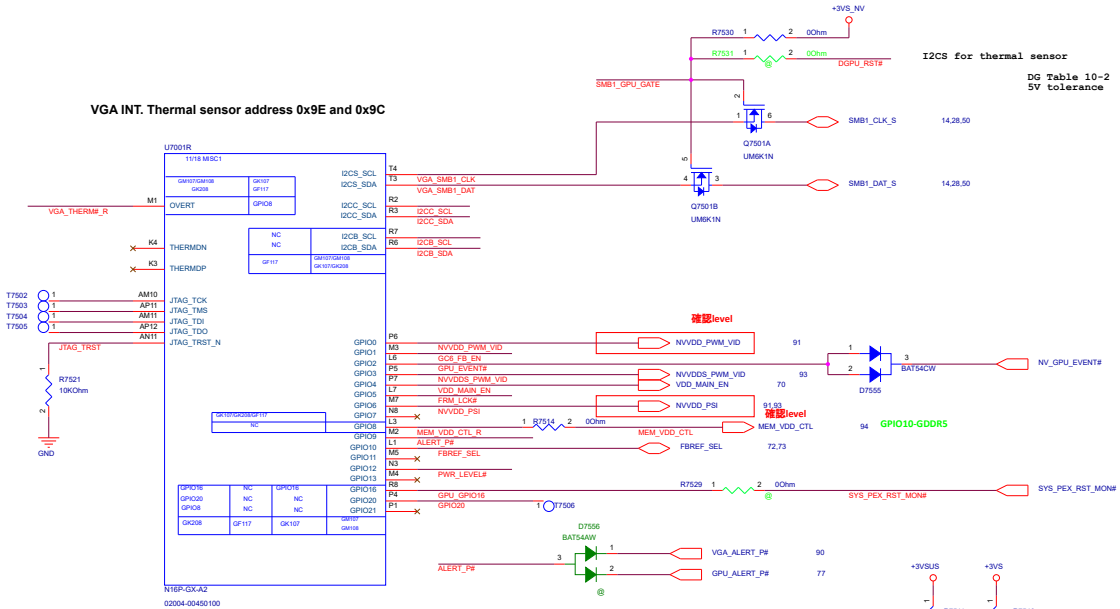
DVI(link D)

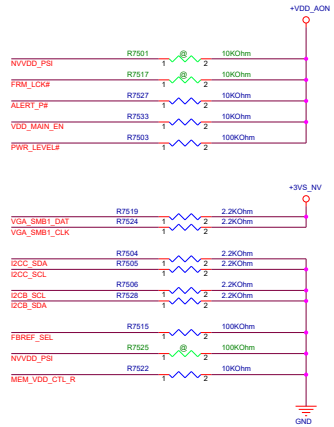


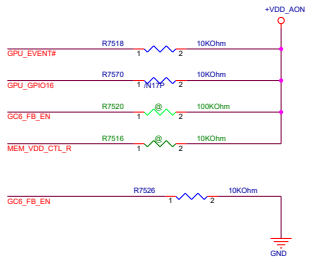
Thermal Sensor

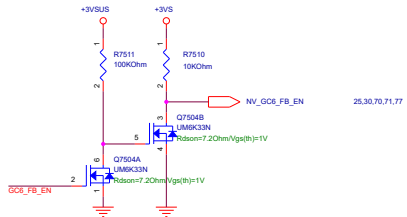


GPIO, TEMP SENSOR, JTAG

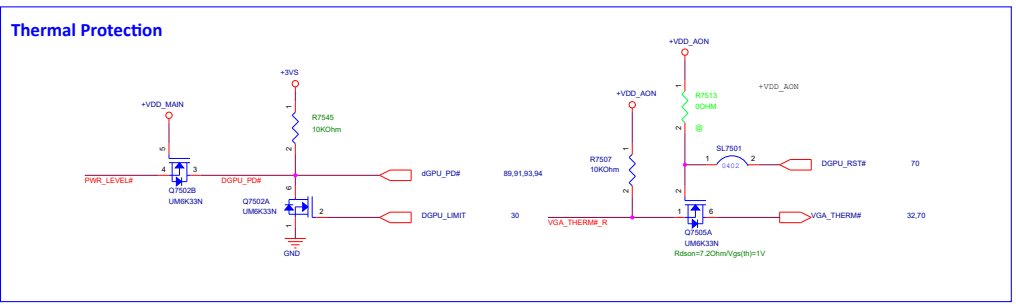






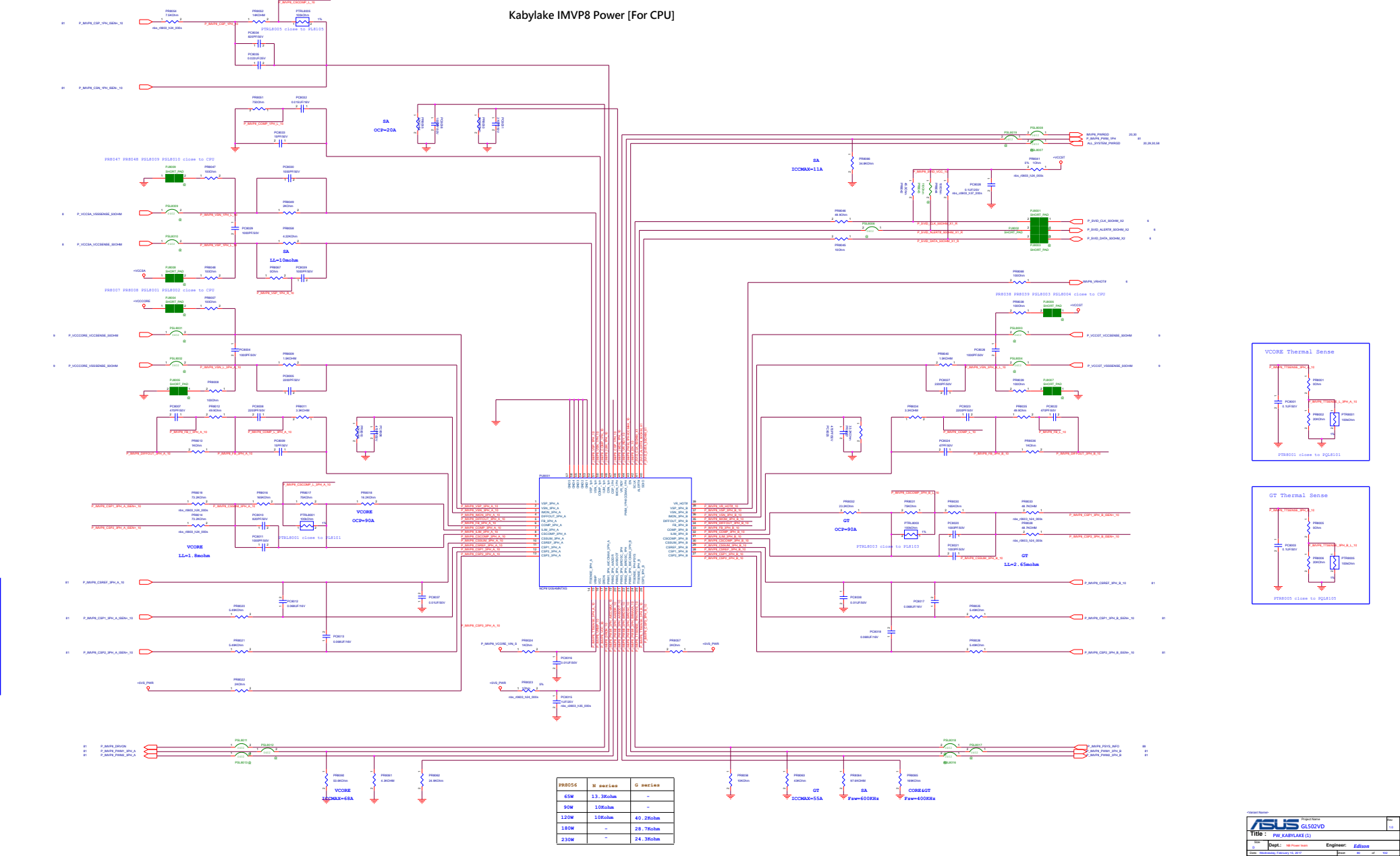


Thermal Protection



ASUS	Project Name: GL502	Rev: 1.0
Title :	POWER_+VGFX_CORE	
Size: A	Dept.: NB Power team	Engineer: Edison
Date: Wednesday, February 15, 2017	Sheet 82 of 102	

Kabylake IMVP8 Power [For CPU]



PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

Project Name	GL502VD	Rev 1.0
Title :	PW_KABYLAKE (1)	
Size: D	Dept.: NB Power team	Engineer: Edison
Date: Wednesday, February 15, 2017	Sheet 80 of 102	

NVVDD POWER AND DECOUPLING

NVVDD Backside cap(pcs)				
	NVIDIA		UX502	
	N16	N17		N17
1uF	8	9		9
4.7uF	15	16		16

高度限制：4.7uF換成1uF

UNDER GPU 1uF x 23pcs

UNDER GPU

Colay MLCC with POSCAP

4.7uF x 5pcs
22uF x 7pcs
330uF x 1pcs

PLACE near GPU close to XVDD BALL

PLACE near GPU close to XVDD BALL

NVVDD GROUND

DG-062746-001_v03
for GC6,
FBVDDQ need turn on by FB_CLAMP

PLACE near balls

PLACE NEAR BGA

Power Source

Icontin.= 1.36A
V = 3.3V

3A
120mil

Address Selection Table

Address	0x78	0x7C	0x7A	0x7B	0x7E	0x72	0x73
R7722	10k	4.7k	2k	6.8k	8.2k	6.1k	0k
R7728	Open	4.7k	4.22k	6.8k	6.7k	3.6k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05
R/W	R	W	W	R	R	R
Function	Temp. alert threshold setting		Second temp. data		bit 4 = 1 bit 5 = 1 bit 6 = 1	

Power Squence Control

GC6_2.0

Discharge

Engineer: Ben_Fang

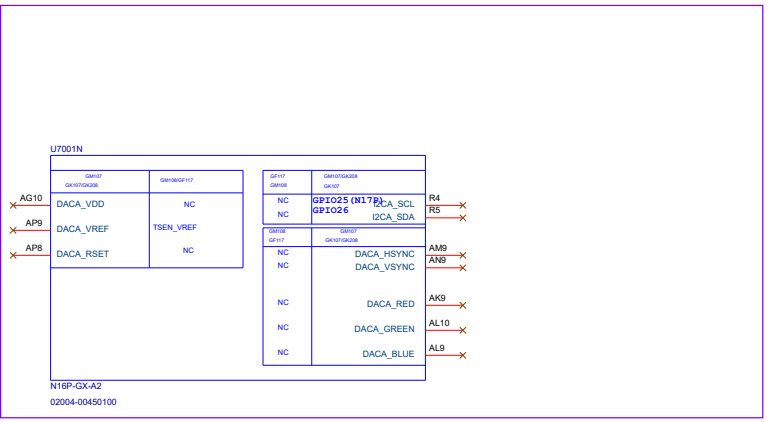
Title : VGA_PWG/GND(8)

GL502VD

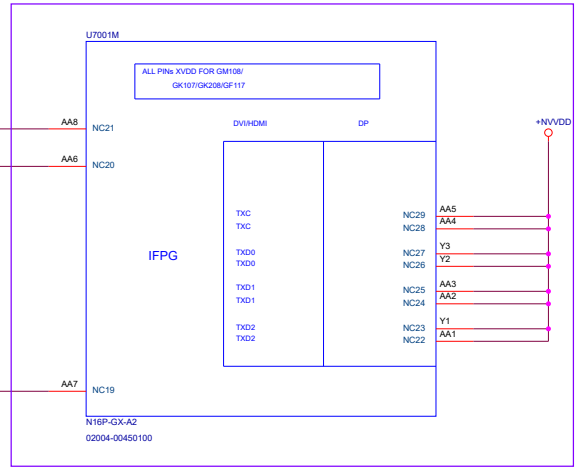
<Variant Name>

ASUSTek Computer INC	Title : PWR_ BAT_CON & GAUGE	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 65 of 102	

CRT DAC_A

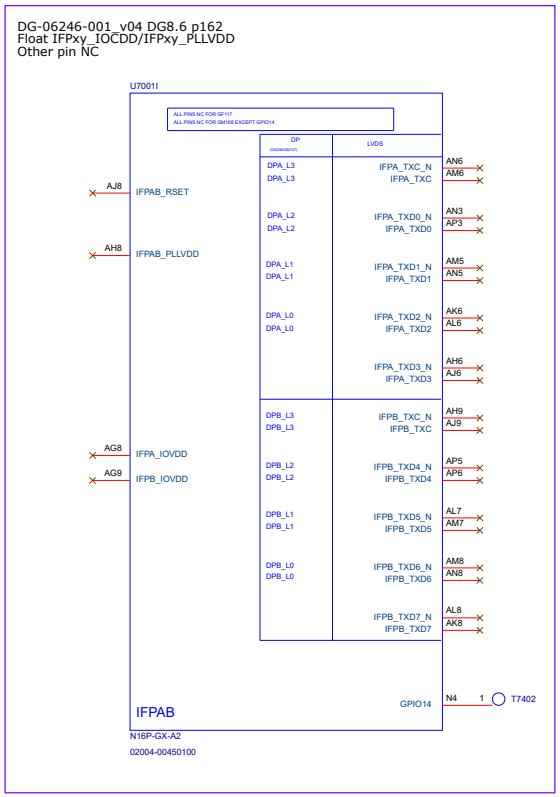


LVDS IFPG

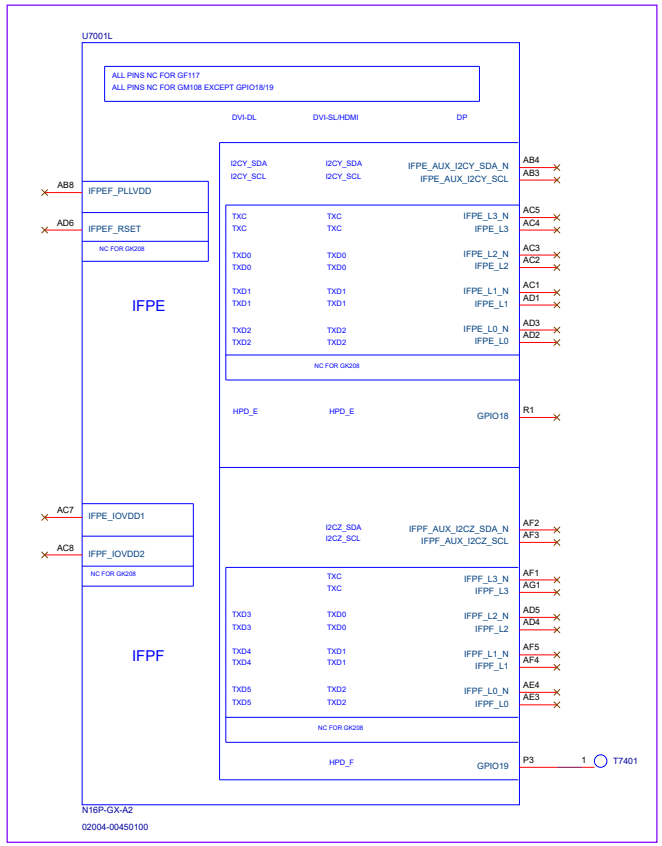


LVDS IFPA/B

DG-06246-001_v04 DG8.6 p162
Float IFPxy_IOCDD/IFPxy_PLLVDD
Other pin NC

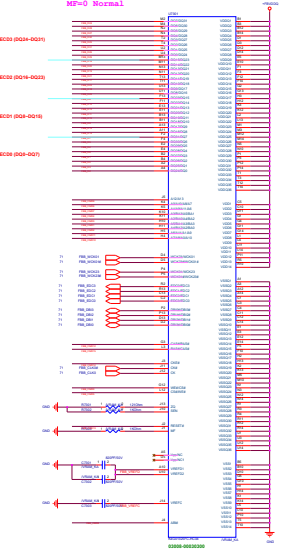


LVDS IFPE/F



<Variant Name>

ASUSTeK COMPUTER	Title : VGA_CRT/LVDS(5)	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 74 of 102	

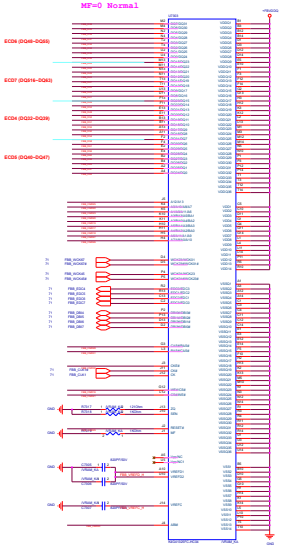


FBB Partition Memory (1 of 2)

USE GDDR5 VRAM 128Mb x 32 (512MB)
1st: P/N: 03000-00030300 SAMSUNG/K4G41325FC-HC03 (C-die), Strap: 0x3 (+1.35V)
2nd: P/N: 03000-00030400 Micron/EDW4032BABG-60-F (A-die)_Strap: 0x4 (+1.35V)

USE GDDR5 VRAM 256Mb x 32 (1024MB)
1st: P/N: 03000-00032200 MICRON/MT51J256M32HF-60:A (A-die)_Strap: 0x9 (+1.35V)
2nd: P/N: 03000-00050100 SAMSUNG/K4G80325FB-HC03 (B-die), Strap: 0x8 (+1.35V)

	PR9210
+1.35V	8.06Kohm
+1.5V	10Kohm



FBB Partition Memory (2 of 2)

Title :	VGA VRAM Ch 2
Engineer:	Ben_Fang
Size	Project Name
Custom	G1S02VD
Date: Wednesday, February 01, 2012	Sheet 1 of 1

Kabylake IMVP8 Power [For CPU]

PT810* 請放置 PU8101旁;並請放置Trace 上!

PT810* 請放置 PU8103旁;並請放置Trace 上!

PT810* 請放置 PU8102旁;並請放置Trace 上!

PT810* 請放置 PU8104旁;並請放置Trace 上!

PT810* 請放置 PU8105旁;並請放置Trace 上!

Imax = 68A
OCP = 90A

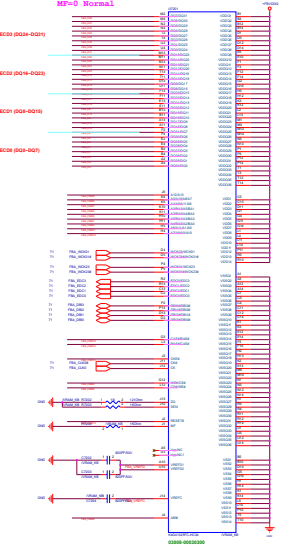
Imax = 55A
OCP = 70A

+VCCCORE

+VCCGT

+VCCSA

Project Name	GL502VD		Rev
Title :	PW_KABYLAKE (2)		R1.0
Size: A2	Dept.: NB Power team	Engineer: Edison	
Date: Wednesday, February 15, 2017	Sheet 81 of 102		



FBA Partition Memory (1 of 2)

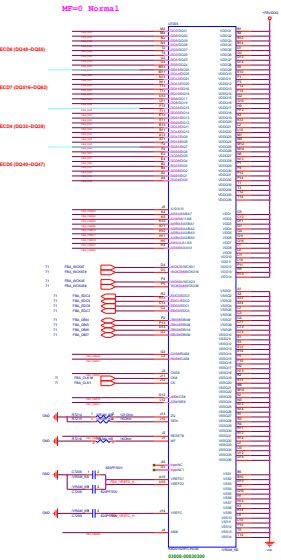
GDDS MODE SELECTION

MODE	NP	ESC1	ESC2
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

USE GDDR5 VRAM 128Mb x 32 (512MB)
1st: P/N: 03000-00030200 SAMSUNG/K4G4122IFC-HC03 (C-die), Strap: 0x3 (+1.35V)
2nd: P/N: 03000-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

USE GDDR5 VRAM 256Mb x 32 (1024MB)
1st: P/N: 03000-00030300 MICRON/MT51J256M32HF-60:A (A-die), Strap: 0x9 (+1.35V)
2nd: P/N: 03000-00050100 SAMSUNG/K4G80325FB-HC03 (B-die), Strap: 0x8 (+1.35V)

	PR5310
+1.35V	0.06Kohm
+1.5V	100Kohm

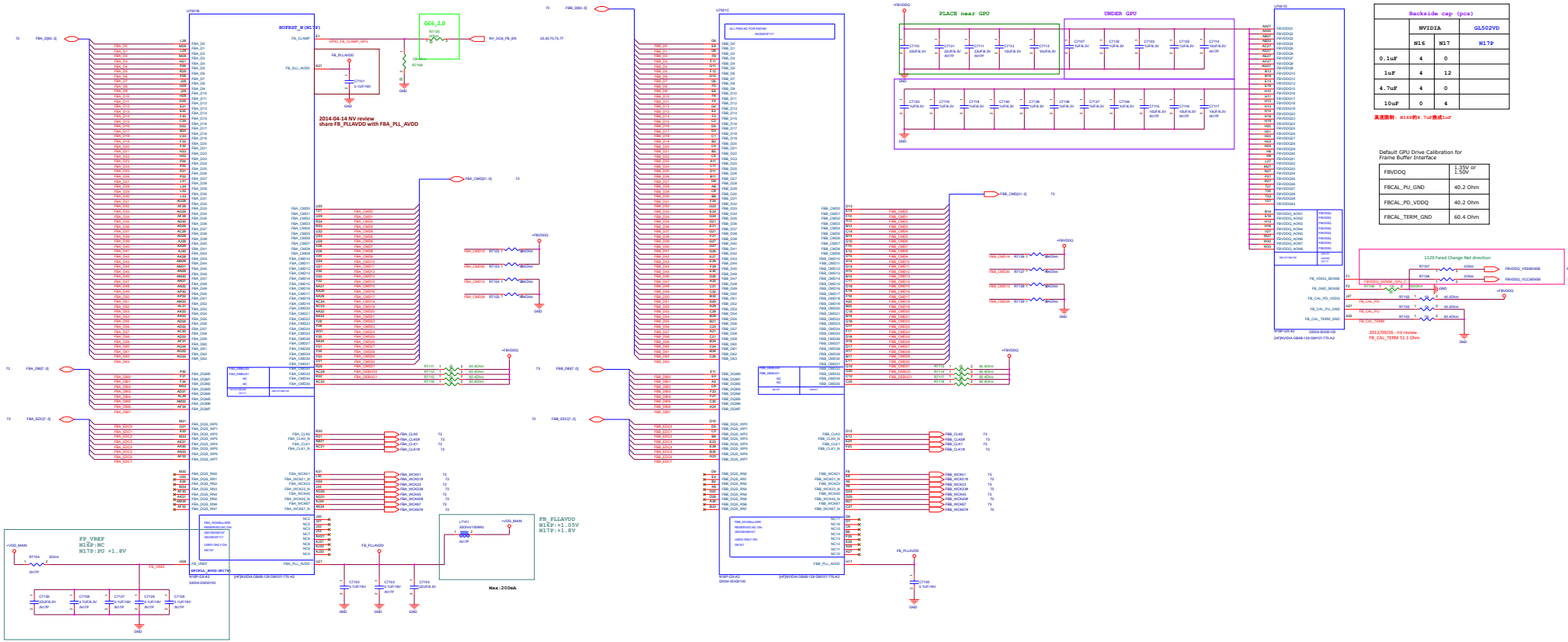


FBA Partition Memory (2 of 2)

Title :	VGA VRAM CK_A
Engineer:	Ben_Feng
Size:	Project Name: GL502VD
Rev:	
Custom	
Date:	Sheet of

GPU MEMORY INTERFACE: PARTITION A

GPU MEMORY INTERFACE: PARTITION B



Backside cap (pcs)			
	NVIDIA		GL502VD
	N16	N17	N17P
0.1uF	4	0	
1uF	4	12	
4.7uF	4	0	
10uF	0	4	

高度限制：N16P的4.7uF換成1uF

Default GPU Drive Calibration for Frame Buffer Interface

FBVDDQ	1.35V or 1.50V
FBCAL_PU_GND	40.2 Ohm
FBCAL_PD_VDDQ	40.2 Ohm
FBCAL_TERM_GND	60.4 Ohm

Variant Name:

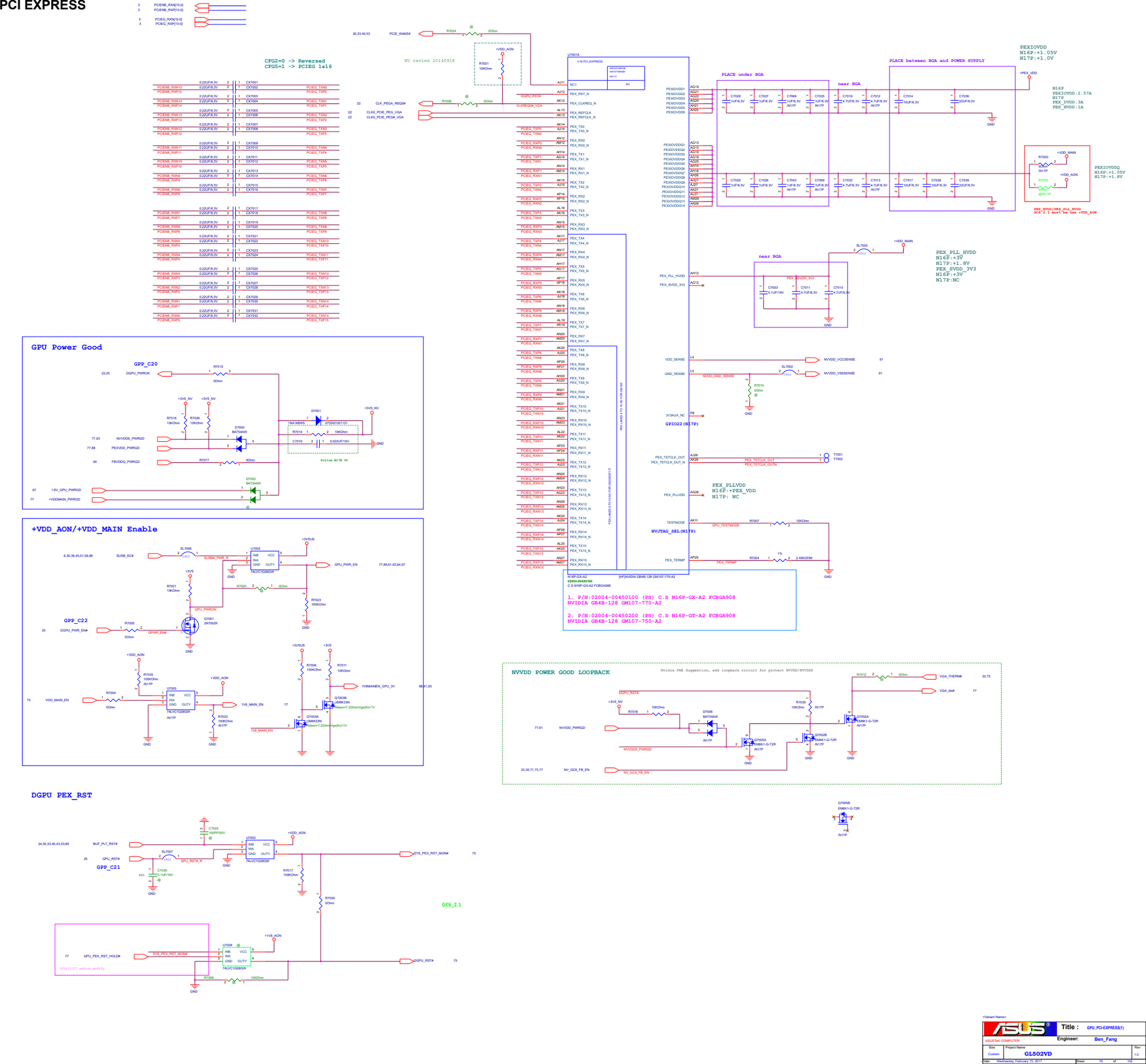
Title : VGA_FB-F_(2GDR5)(2)

Engineer: Ben_Fang

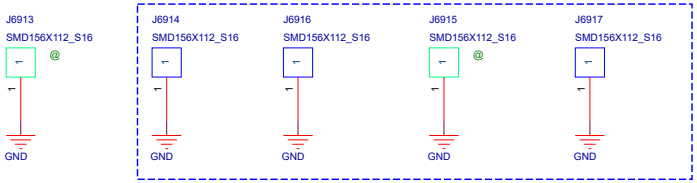
Size	Project Name	Rev
Custom	GL502VD	1.0

Date: Wednesday, February 15, 2017 Sheet 71 of 100

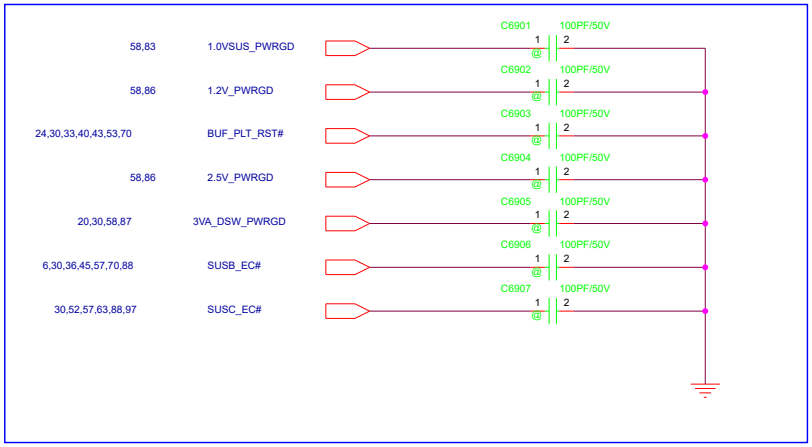
PCI EXPRESS

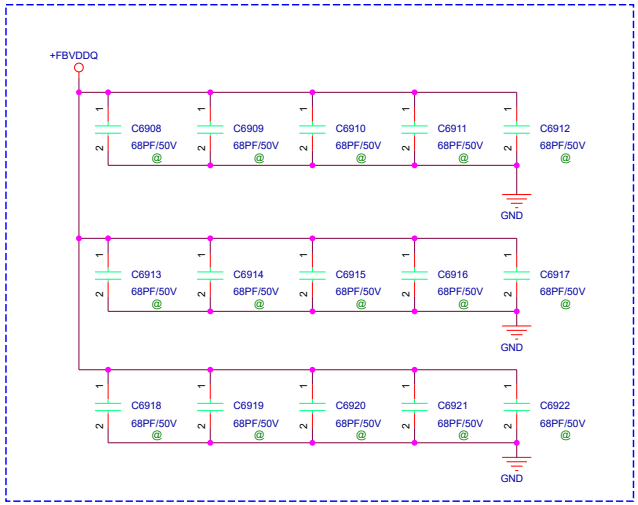

CFG2=0 -> Reversed
CFG5=1 -> PCIEG 1x16
NV review 20140918
PLACE under BGA
PLACE between BGA and POWER SUPPLY
near BGA
PEXIOVDD
N16P:+1.05V
N17P:+1.0V
N16P
PEXIOVDD:2.57A
N17P
PEX_DVDD:3A
PEX_HVDD:1A
PEXIOVDDQ
N16P:+1.05V
N17P:+1.8V
PEX_HVDD/PEX_PLL_HVDD
GC6_2.1 must be Use +VDD_AON
PEX_PLL_HVDD
N16P:+3V
N17P:+1.8V
PEX_SVDD_3V3
N16P:+3V
N17P:NC
PEX_PLLVDD
N16P:+PEX_VDD
N17P: NC
GPIO22(N17P)
NVJTAG_SEL(N17P)
GPU Power Good
GPP_C20
+VDD_AON/+VDD_MAIN Enable
GPP_C22
DGPU PEX_RST
GPP_C21
NVVDD POWER GOOD LOOPBACK
Nvidia FAE Suggestion, add loopback circuit for protect NVVDD/NVVDDS
GC6_2.1
1. P/N:02004-00450100 (PS) C.S N16P-GX-A2 FCBGA908
NVIDIA GB4B-128 GM107-770-A2
2. P/N:02004-00450200 (PS) C.S N16P-GT-A2 FCBGA908
NVIDIA GB4B-128 GM107-750-A2
Title : GPU_PCI-EXPRESS(1)
ASUSTeK COMPUTER
Engineer: Ben_Fang
Size: Custom
Project Name: GL502VD
Rev: 1.0
Date: Wednesday, February 15, 2017
Sheet 70 of 102

R1.2_17 EMI Reserve 100pf to Gnd



2015.10.07 For EMI Request





2016.06.20 For EMI Request

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : OTH_EMI	
	Engineer: Ben_Fang	
Size: B	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 69 of 102	

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : OTH_for test only	
	Engineer: Ben_Fang	
Size: A	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 68 of 102	

shielding case screw hole

PCH NUT

2016.05.06
delete H6711,H6712

H6731 2D_D94
H6732 2D_D110_DO94X106N
H6735 2D_D94_D94N
H6736 2D_D110_DO94X106
H6744 CT354CB315D94
H6742 CT256CB315I114D94
H6741 CT256CB315I114D94
H6743 CT256CB315I114D94

H6733 14D_D110_C31D31N
2016.05.06 update
H6734 RT591X512CB315D110

2016.05.06 update
H6760 C354D94
H6745 CT354CRB315x335D94

FAN NUT
H6705 CT217CB176D146
H6707 CT217CB176D146
H6708 CT217CB176D146
H6709 CT217CB176D146
H6710 CT217CB176D146

GPU bracket tooling hole

R1.2_18 Remove GPU Breaket

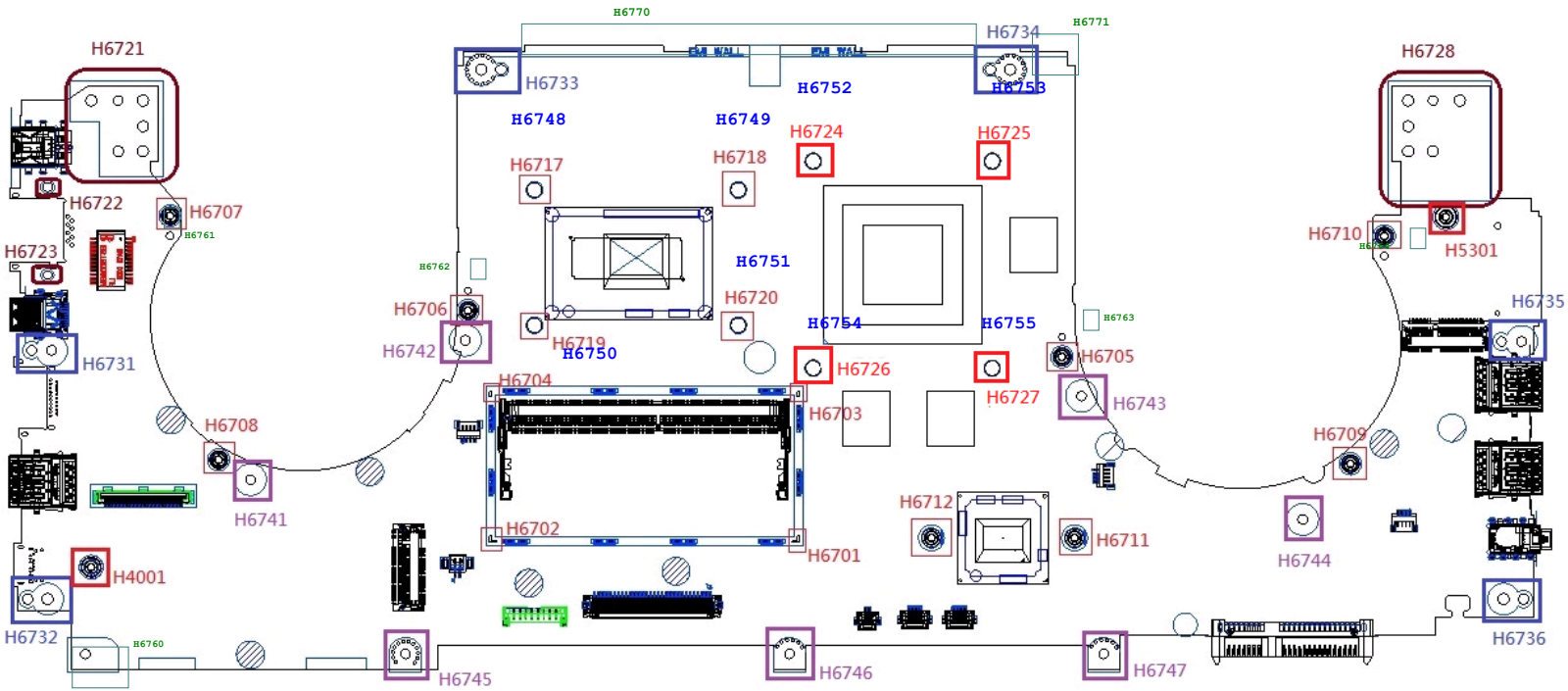
CPU skrew hole

CPU NUT
H6748 CT217CB176D146
H6749 CT217CB176D146
H6750 CT217CB176D146
H6751 CT217CB176D146

GPU NUT
2016.05.06 update
H6752 CT236CB176D146
H6753 CT236CB176D146
H6754 CT236CB176D146
H6755 CT236CB176D146

H6721 7D_D104_D110_D114
H6728 7D_D114_D104_D110
H6722 OT111X99BIDO91X79
H6723 OT111X99BIDO91X79
H6756 OB169X94DO130X55
H6757 OB169X94DO130X55

<COMPONMENT BOT>



H6761 O79X67DO79X67N
H6764 O79X67DO79X67N
2016.05.06
delete H6762
H6763 C67D67N
H6746 CT354CRB315x335D94
H6747 CT354CRB315x335D94

<Variant Name>

ASUSTeK COMPUTER INC. NB3

Title : I/O board FUNC key
Engineer: Ben_Fang

Size	Project Name	Rev
C	GL502VD	1.0

Date: Wednesday, February 15, 2017 Sheet 67 of 102

<Variant Name>

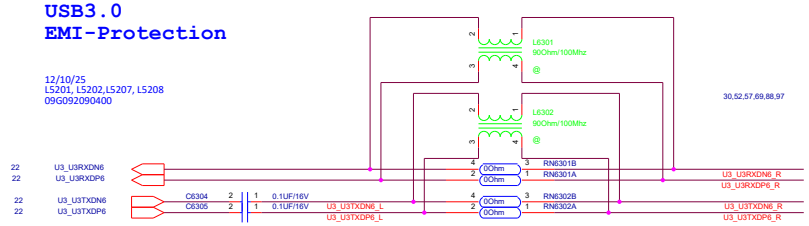
ASUSTeK COMPUTER INC. EPAD	Title : EC_IT8569	
	Engineer: Ben_Fang	
Size: Custom	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 66 of 102	

<Variant Name>

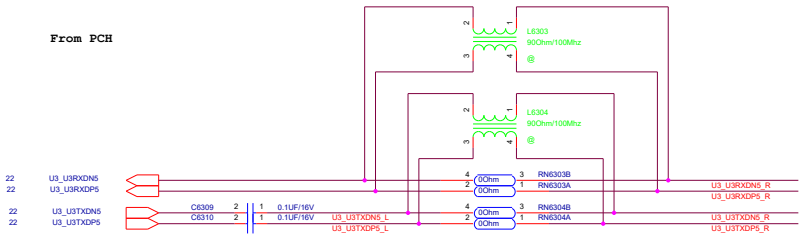
ASUSTek Computer INC	Title : PWR_ BAT_CON & GAUGE	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 64 of 102	

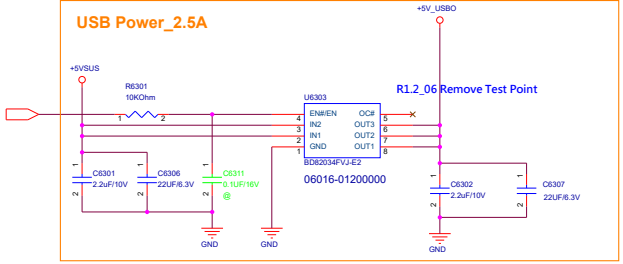
USB3.0 EMI-Protection

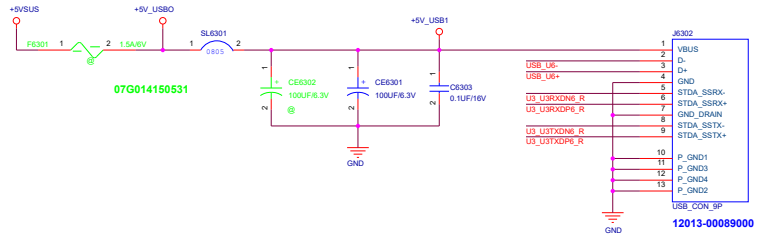
12/10/25
L5201, L5202,L5207, L5208
09G092090400

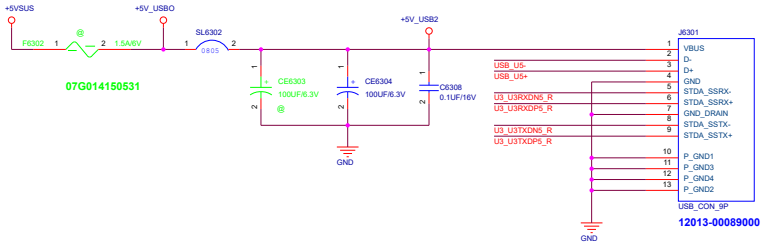


From PCH



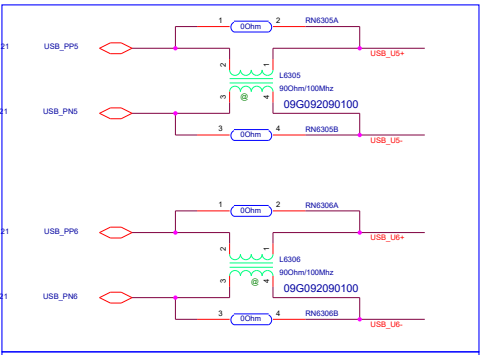






USB2.0 EMI-Protection

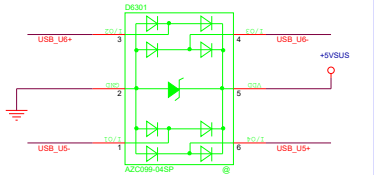
R1.1-4/13-5



L5204 & L5206 C.M. CHOKE(0805)90 OHM/330mA
1st Source: P/N:09G09209011D INPAQ/MCM2012D900FBE
2nd Source: P/N:09G092090300 TAI-TECH/WCM2012F2SF-900T04
3rd Source: P/N:09G092090110 MURATA/DLW21SN900SQ2L
4th Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S
5th Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L

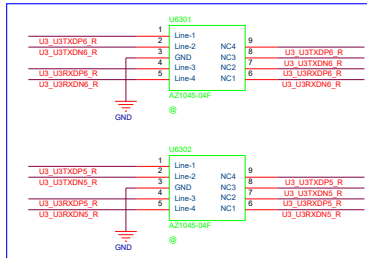
R1.1-4/13-5

D5201 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



USB3.0/USB 2.0 ESD-Protection

R1.1-4/13-5



U5201 & U5203 ESD PROTECTION
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : USB Port	
	Engineer: Ben_Fang	
Size: C	Project Name: GL502VD	Rev: 1.0
Date: Wednesday, February 15, 2017	Sheet 63 of 102	