Project Name :GMXBGXX

Platform : FP7r2+GN21

PAGE CONTENT

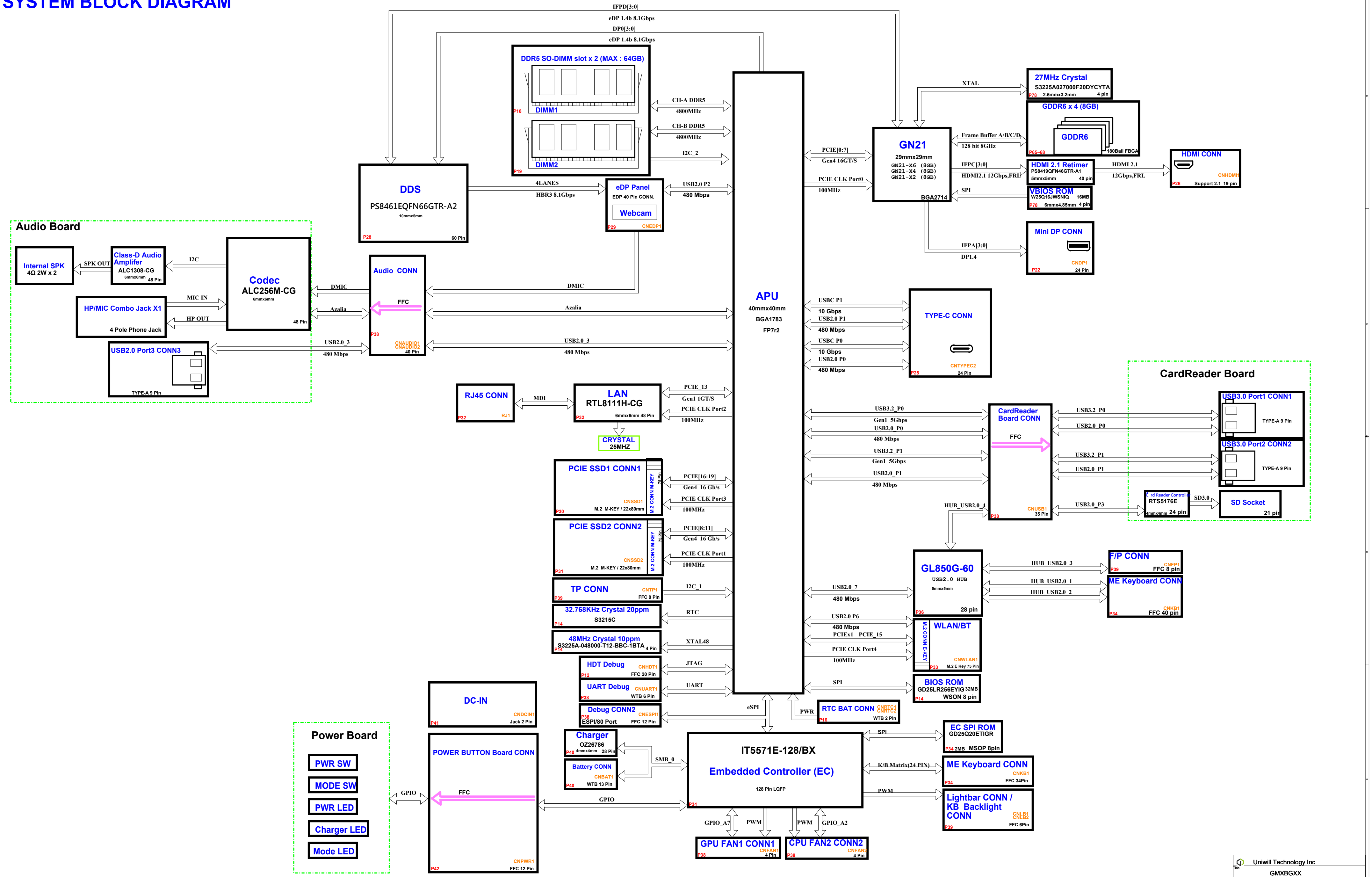
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

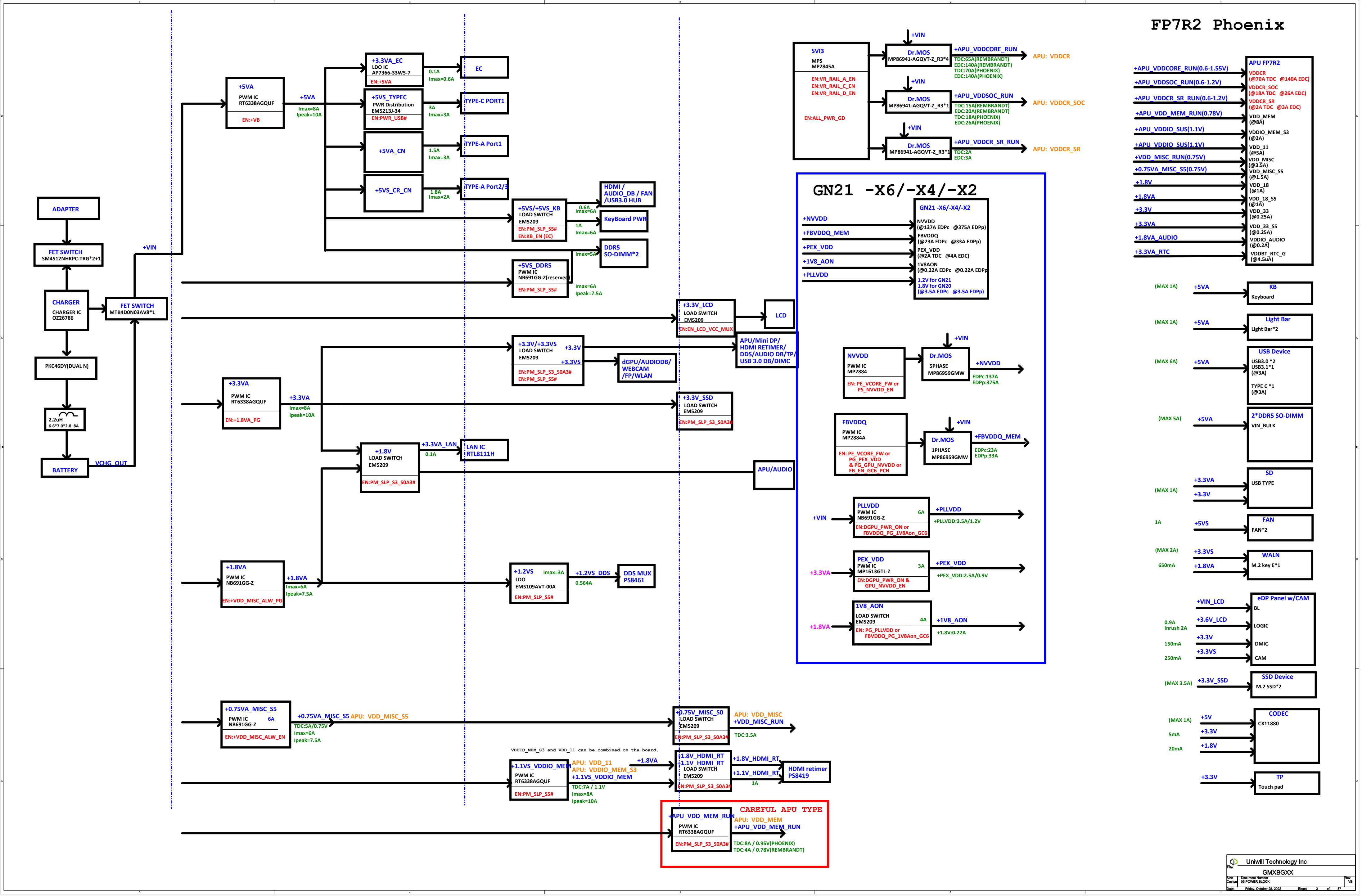
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

SYSTEM BLOCK DIAGRAM

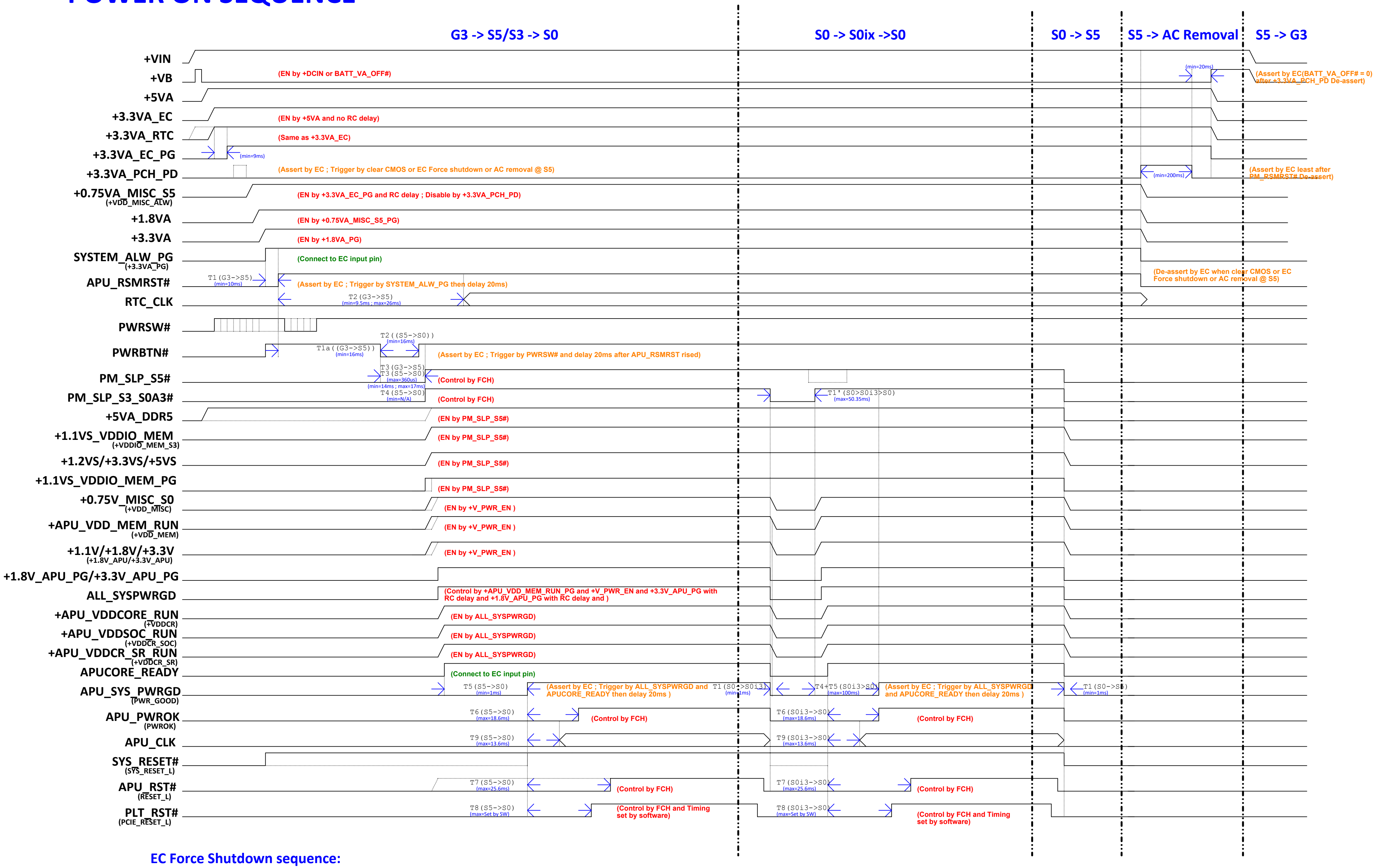


Uniwill Technology Inc			
Title	GMXBGXX		
Size: Custom	Document Number: 02 SYSTEM BLOCK		Rev: V8
Date: Friday, October 28, 2022	Sheet 2	of 87	

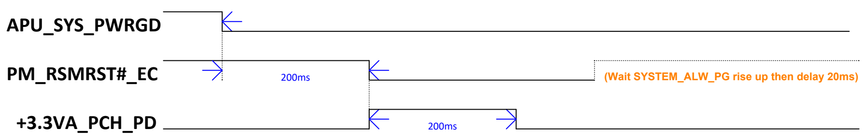


FP7R2 Phoenix
ADAPTER
FET SWITCH SM4512NHKPC-TRG*2+1
CHARGER
CHARGER IC OZ26786
FET SWITCH MTB4D0N03AV8*1
+VIN
PKC46DY(DUAL N)
2.2uH 6.6*7.0*2.8_8A
BATTERY
VCHG_OUT
+5VA PWM IC RT6338AGQUF EN:+VB
+5VA Imax=8A Ipeak=10A
+3.3VA_EC LDO IC AP7366-33W5-7 EN:+5VA
0.1A Imax=0.6A
EC
+5VS_TYPEC PWR Distribution EM5213J-34 EN:PWR_USB#
3A Imax=3A
TYPE-C PORT1
+5VA_CN
1.5A Imax=3A
TYPE-A Port1
+5VS_CR_CN
1.8A Imax=2A
TYPE-A Port2/3
+5VS/+5VS_KB LOAD SWITCH EM5209 EN:PM_SLP_S5# EN:KB_EN (EC)
0.6A Imax=6A
HDMI / AUDIO_DB / FAN /USB3.0 HUB
1A Imax=6A
KeyBoard PWR
Imax=5A
DDR5 SO-DIMM*2
+5VS_DDR5 PWM IC NB691GG-Z(reserved) EN:PM_SLP_S5#
Imax=6A Ipeak=7.5A
+3.3V_LCD LOAD SWITCH EM5209 EN:EN_LCD_VCC_MUX
LCD
+3.3V/+3.3VS LOAD SWITCH EM5209 EN:PM_SLP_S3_S0A3# EN:PM_SLP_S5#
+3.3V +3.3VS
APU/Mini DP/ HDMI RETIMER/ DDS/AUDIO DB/TP/ USB 3.0 DB/DIMC
dGPU/AUDIODB/ WEBCAM /FP/WLAN
+3.3VA PWM IC RT6338AGQUF EN:+1.8VA_PG
+3.3VA Imax=8A Ipeak=10A
+3.3V_SSD LOAD SWITCH EM5209 EN:PM_SLP_S3_S0A3#
+1.8V LOAD SWITCH EM5209 EN:PM_SLP_S3_S0A3#
+3.3VA_LAN 0.1A
LAN IC RTL8111H
APU/AUDIO
+1.8VA PWM IC NB691GG-Z EN:+VDD_MISC_ALW_PG
+1.8VA Imax=6A Ipeak=7.5A
+1.2VS LDO EM5109AVT-00A EN:PM_SLP_S5# Imax=3A
+1.2VS_DDS 0.564A
DDS MUX PS8461
+0.75VA_MISC_S5 PWM IC NB691GG-Z 6A EN:+VDD_MISC_ALW_EN
+0.75VA_MISC_S5 APU: VDD_MISC_S5
TDC:5A/0.75V Imax=6A Ipeak=7.5A
+0.75V_MISC_S0 LOAD SWITCH EM5209 EN:PM_SLP_S3_S0A3#
APU: VDD_MISC +VDD_MISC_RUN TDC:3.5A
VDDIO_MEM_S3 and VDD_11 can be combined on the board.
+1.1VS_VDDIO_MEM PWM IC RT6338AGQUF EN:PM_SLP_S5#
APU: VDD_11 APU: VDDIO_MEM_S3 +1.1VS_VDDIO_MEM TDC:7A / 1.1V Imax=8A Ipeak=10A
+1.8VA
+1.8V_HDMI_RT +1.1V_HDMI_RT LOAD SWITCH EM5209 EN:PM_SLP_S3_S0A3#
+1.8V_HDMI_RT +1.1V_HDMI_RT 1A
HDMI retimer PS8419
CAREFUL APU TYPE
+APU_VDD_MEM_RUN PWM IC RT6338AGQUF EN:PM_SLP_S3_S0A3#
APU: VDD_MEM +APU_VDD_MEM_RUN
TDC:8A / 0.95V(PHOENIX) TDC:4A / 0.78V(REMBRANDT)
SVI3 MPS MP2845A EN:VR_RAIL_A_EN EN:VR_RAIL_C_EN EN:VR_RAIL_D_EN EN:ALL_PWR_GD
+VIN Dr.MOS MP86941-AGQVT-Z_R3*4
+APU_VDDCORE_RUN TDC:65A(REMBRANDT) EDC:140A(REMBRANDT) TDC:70A(PHOENIX) EDC:140A(PHOENIX)
APU: VDDCR
+VIN Dr.MOS MP86941-AGQVT-Z_R3*1
+APU_VDDSOC_RUN TDC:15A(REMBRANDT) EDC:20A(REMBRANDT) TDC:18A(PHOENIX) EDC:26A(PHOENIX)
APU: VDDCR_SOC
+VIN Dr.MOS MP86941-AGQVT-Z_R3*1
+APU_VDDCR_SR_RUN TDC:2A EDC:3A
APU: VDDCR_SR
GN21 -X6/-X4/-X2
+NVVDD +FBVDDQ_MEM +PEX_VDD +1V8_AON +PLLVDD
GN21 -X6/-X4/-X2
NVVDD (@137A EDPc @375A EDPp)
FBVDDQ (@23A EDPc @33A EDPp)
PEX_VDD (@2A TDC @4A EDC)
1V8AON (@0.22A EDPc @0.22A EDPp)
1.2V for GN21 1.8V for GN20 (@3.5A EDPc @3.5A EDPp)
NVVDD PWM IC MP2884 EN: PE_VCORE_FW or PS_NVVDD_EN
+VIN Dr.MOS 5PHASE MP86959GMW
+NVVDD EDPc:137A EDPp:375A
FBVDDQ PWM IC MP2884A EN: PE_VCORE_FW or PG_PEX_VDD & PG_GPU_NVVDD or FB_EN_GC6_PCH
+VIN Dr.MOS 1PHASE MP86959GMW
+FBVDDQ_MEM EDPc:23A EDPp:33A
+VIN PLLVDD PWM IC NB691GG-Z 6A EN:DGPU_PWR_ON or FBVDDQ_PG_1V8Aon_GC6
+PLLVDD +PLLVDD:3.5A/1.2V
+3.3VA PEX_VDD PWM IC MP1613GTL-Z 3A EN:DGPU_PWR_ON & GPU_NVVDD_EN
+PEX_VDD +PEX_VDD:2.5A/0.9V
+1.8VA 1V8_AON LOAD SWITCH EM5209 4A EN: PG_PLLVDD or FBVDDQ_PG_1V8Aon_GC6
+1V8_AON +1.8V:0.22A
+APU_VDDCORE_RUN(0.6-1.55V) +APU_VDDSOC_RUN(0.6-1.2V) +APU_VDDCR_SR_RUN(0.6-1.2V) +APU_VDD_MEM_RUN(0.78V) +APU_VDDIO_SUS(1.1V) +APU_VDDIO_SUS(1.1V) +VDD_MISC_RUN(0.75V) +0.75VA_MISC_S5(0.75V) +1.8V +1.8VA +3.3V +3.3VA +1.8VA_AUDIO +3.3VA_RTC
APU FP7R2
VDDCR (@70A TDC @140A EDC)
VDDCR_SOC (@18A TDC @26A EDC)
VDDCR_SR (@2A TDC @3A EDC)
VDD_MEM (@8A)
VDDIO_MEM_S3 (@2A)
VDD_11 (@5A)
VDD_MISC (@3.5A)
VDD_MISC_S5 (@1.5A)
VDD_18 (@1A)
VDD_18_S5 (@1A)
VDD_33 (@0.25A)
VDD_33_S5 (@0.25A)
VDDIO_AUDIO (@0.2A)
VDDBT_RTC_G (@4.5uA)
(MAX 1A) +5VA KB Keyboard
(MAX 1A) +5VA Light Bar Light Bar*2
(MAX 6A) +5VA USB Device USB3.0 *2 USB3.1*1 (@3A) TYPE C *1 (@3A)
(MAX 5A) +5VA 2*DDR5 SO-DIMM VIN_BULK
(MAX 1A) +3.3VA +3.3V SD USB TYPE
1A +5VS FAN FAN*2
(MAX 2A) 650mA +3.3VS +1.8VA WALN M.2 key E*1
+VIN_LCD +3.6V_LCD +3.3V +3.3VS
0.9A Inrush 2A 150mA 250mA
eDP Panel w/CAM BL LOGIC DMIC CAM
(MAX 3.5A) +3.3V_SSD SSD Device M.2 SSD*2
(MAX 1A) +5V 5mA +3.3V 20mA +1.8V
CODEC CX11880
+3.3V TP Touch pad
Uniwill Technology Inc
GMXBGXX
03 POWER BLOCK
Friday, October 28, 2022
Sheet 3 of 87

POWER ON SEQUENCE

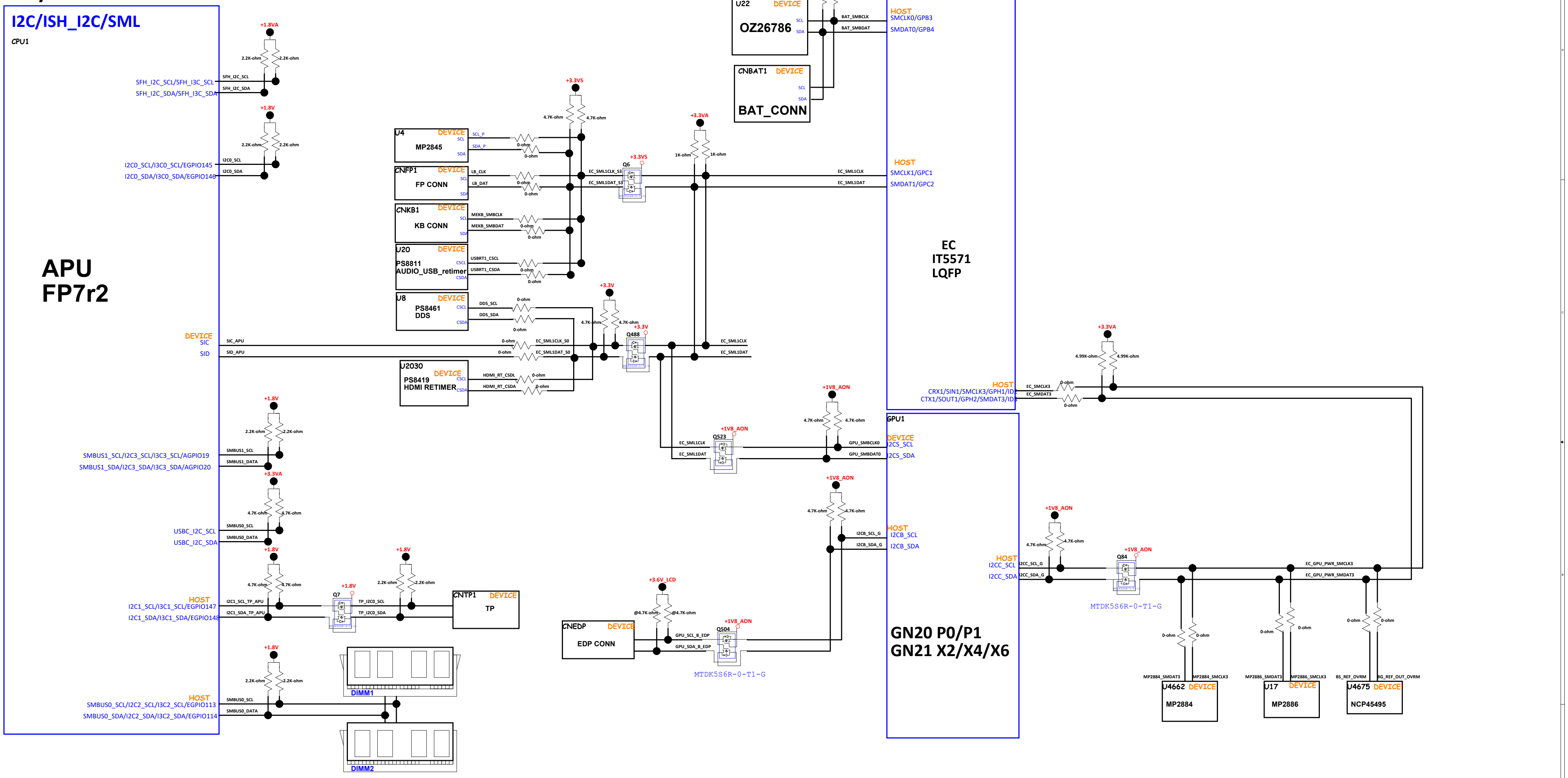


EC Force Shutdown sequence:



Uniwill Technology Inc		
Title	GMXBGXX	
Size Custom	Document Number 04 CPU SEQUENCE	Rev VB
Date: Friday, October 28, 2022	Sheet 4 of 87	

I2C/SMBUS BLOCK

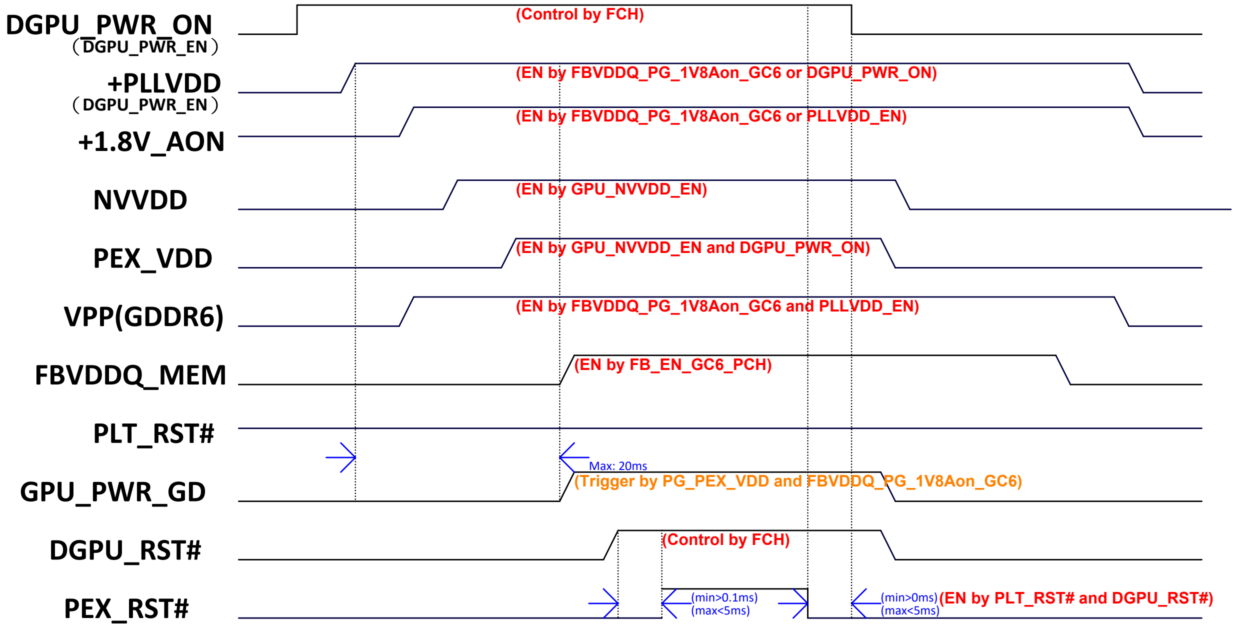


Uniwill Technology Inc

GMXBGXX

05 SMBUS BLOCK

DGPU POWER SEQUENCE

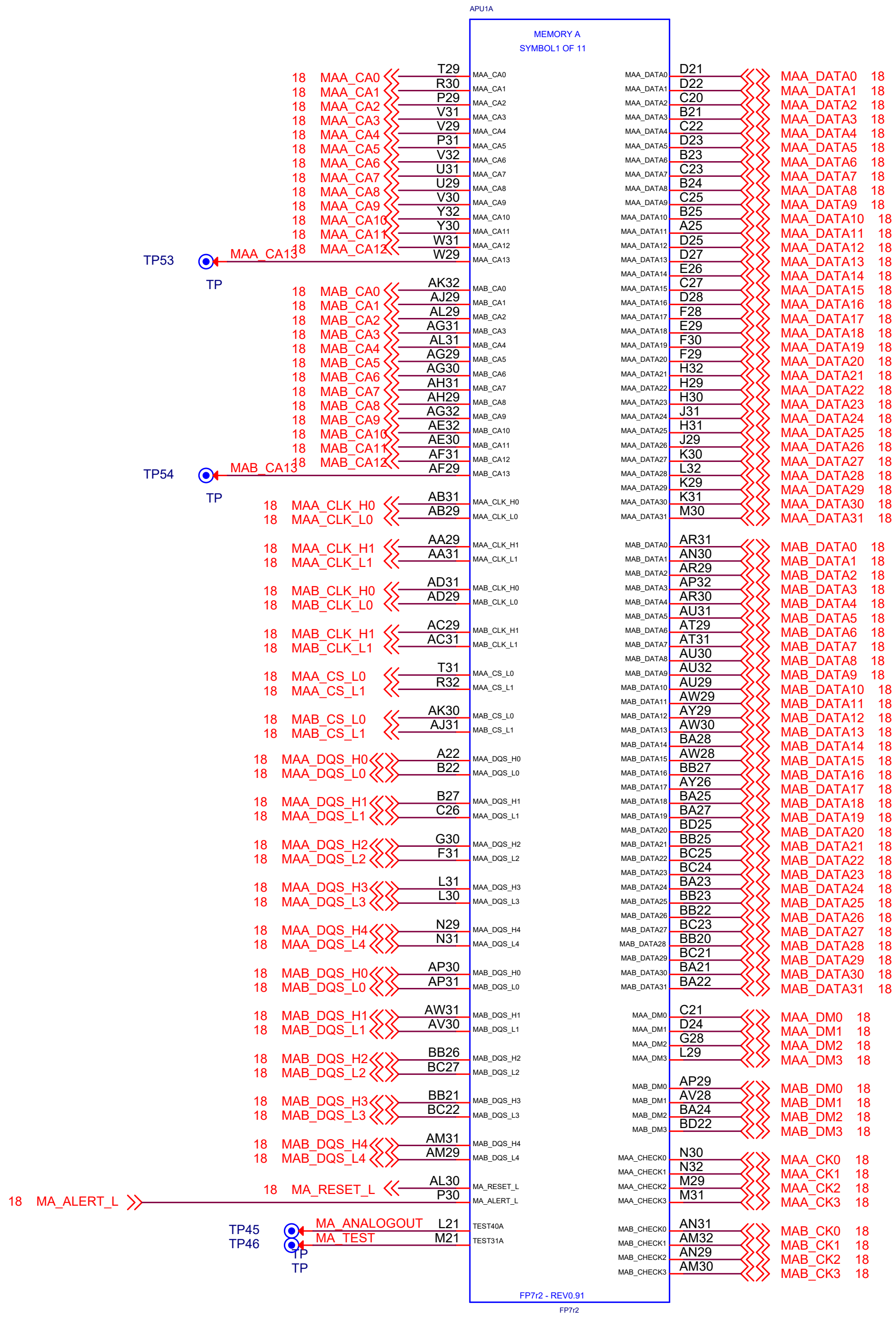


Power-Up Sequence :
1V2 ->1V8AON->NVVDD->PEXVDD->FBVDD(Q)

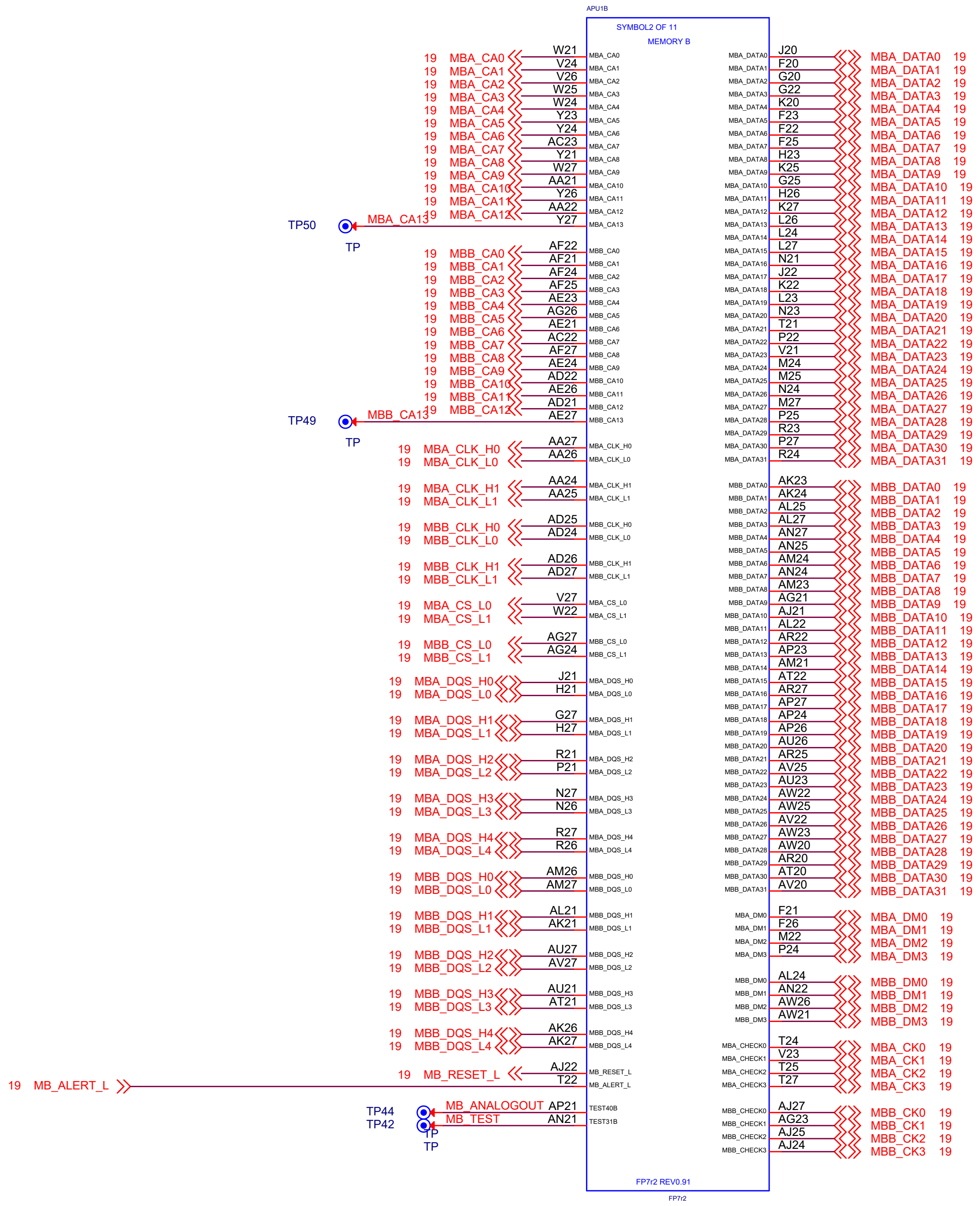
Power-Down Sequence :
PEXVDD -> NVVDD ->FBVDD(Q) -> (1V2 and 1V8AON)

1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.It is recommended that the delay from 1V2 on to PEXVDD/GPU_PGOOD assertion not exceed 20ms

Uniwill Technology Inc					
Title: GMXBGXX					
Size: A	Document Number: 08 Reserved				Rev: VB
Date: Friday, October 28, 2022		Sheet	8	of	87

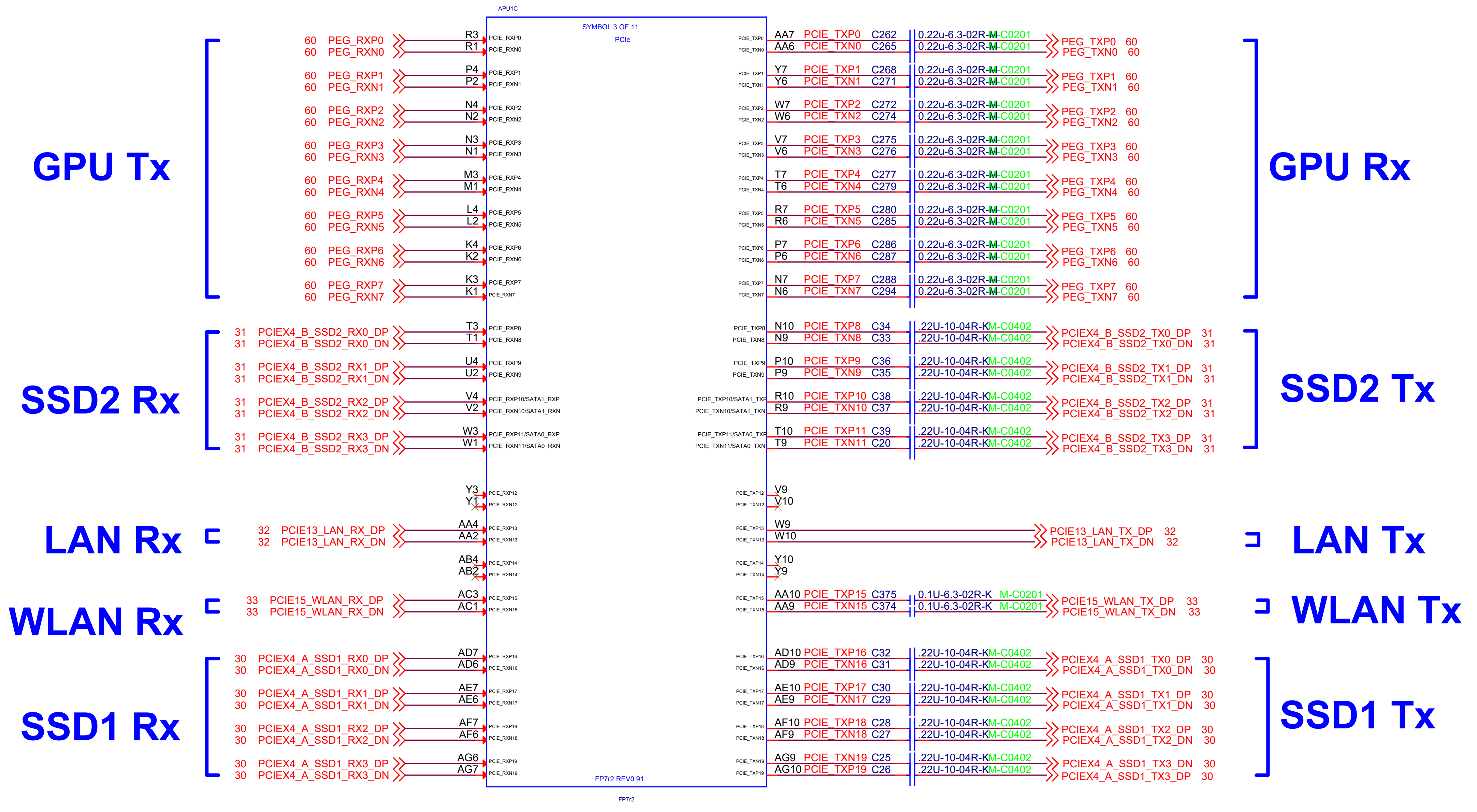


Uniwill Technology Inc			
Title: GMXBGXX			
Size: B	Document Number: 09 AMD DDR5 CHA		Rev: VB
Date: Friday, October 28, 2022	Sheet 9	of 87	



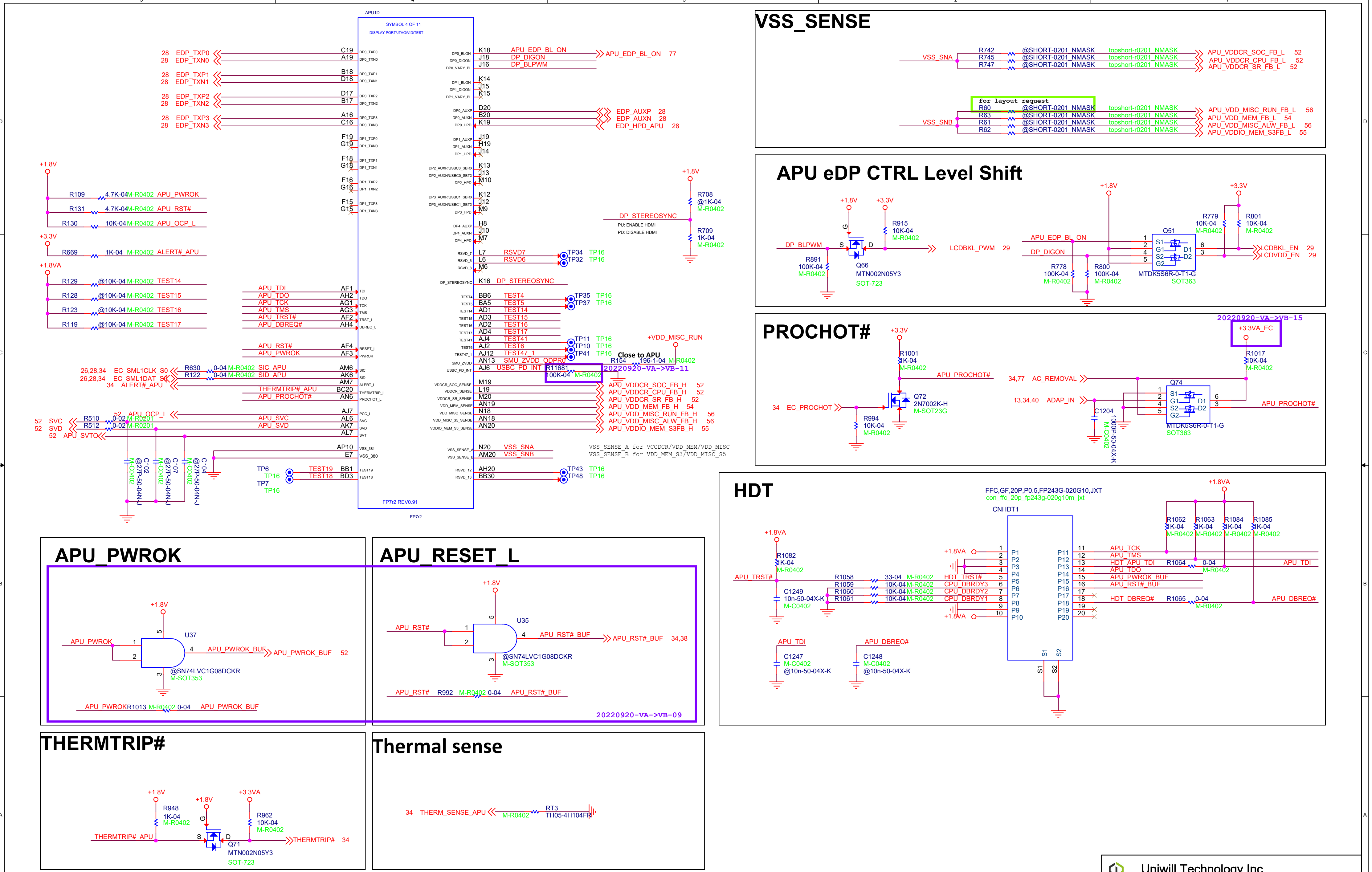
Uniwill Technology Inc

Title	GMXBGXX	
Size B	Document Number 10 AMD DDR5 CHB	Rev VB
Date: Friday, October 28, 2022	Sheet 10 of 87	



Uniwill Technology Inc

Title	GMXBGXX	
Size: Custom	Document Number: 11 AMD PCIE/SATA I/F	Rev: VB
Date: Friday, October 28, 2022	Sheet 11 of 87	

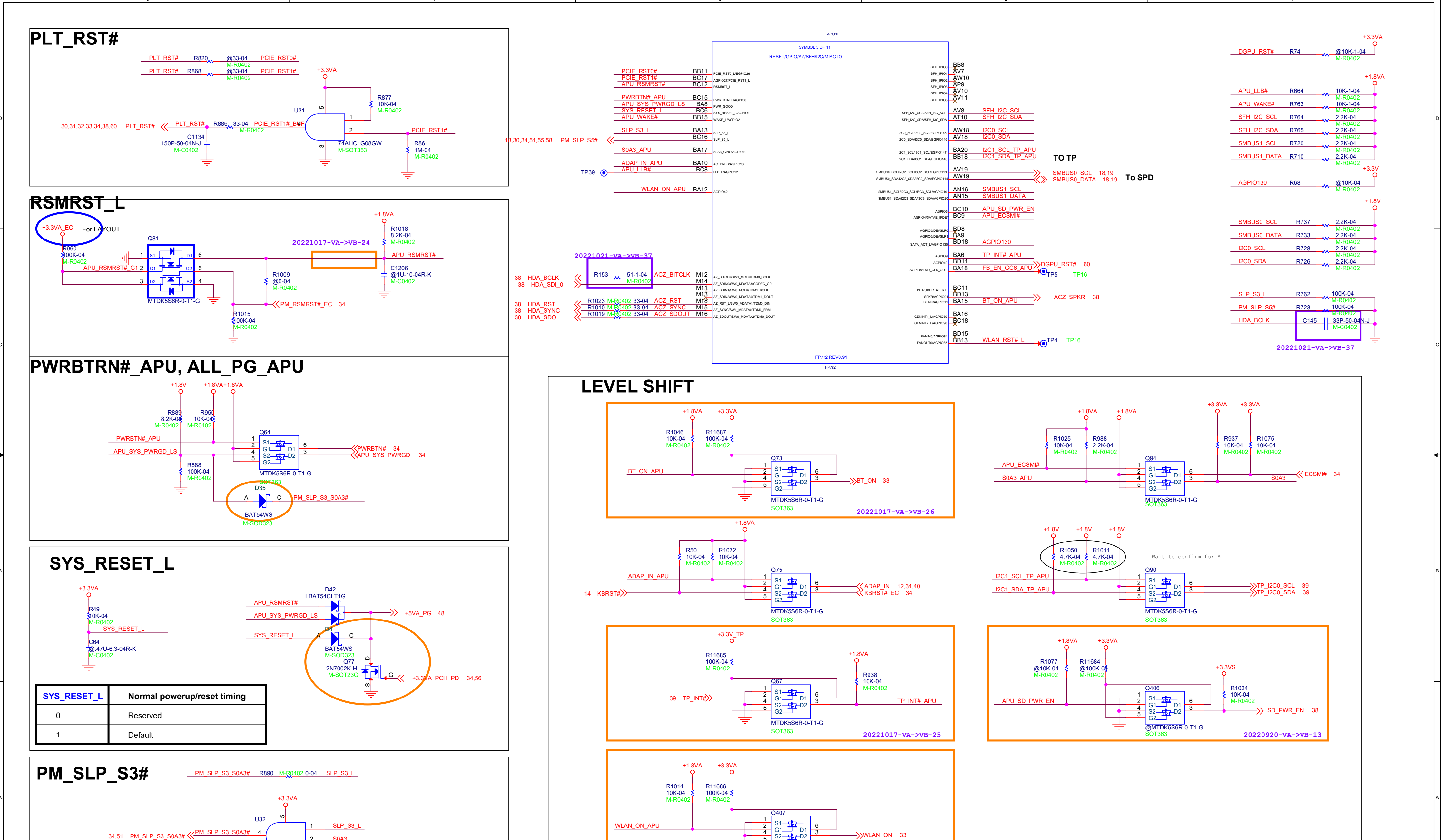


Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	12 AMD DP/JTAG/SVI3/MISC/HDT	VB

Date: Friday, October 28, 2022 Sheet 12 of 87



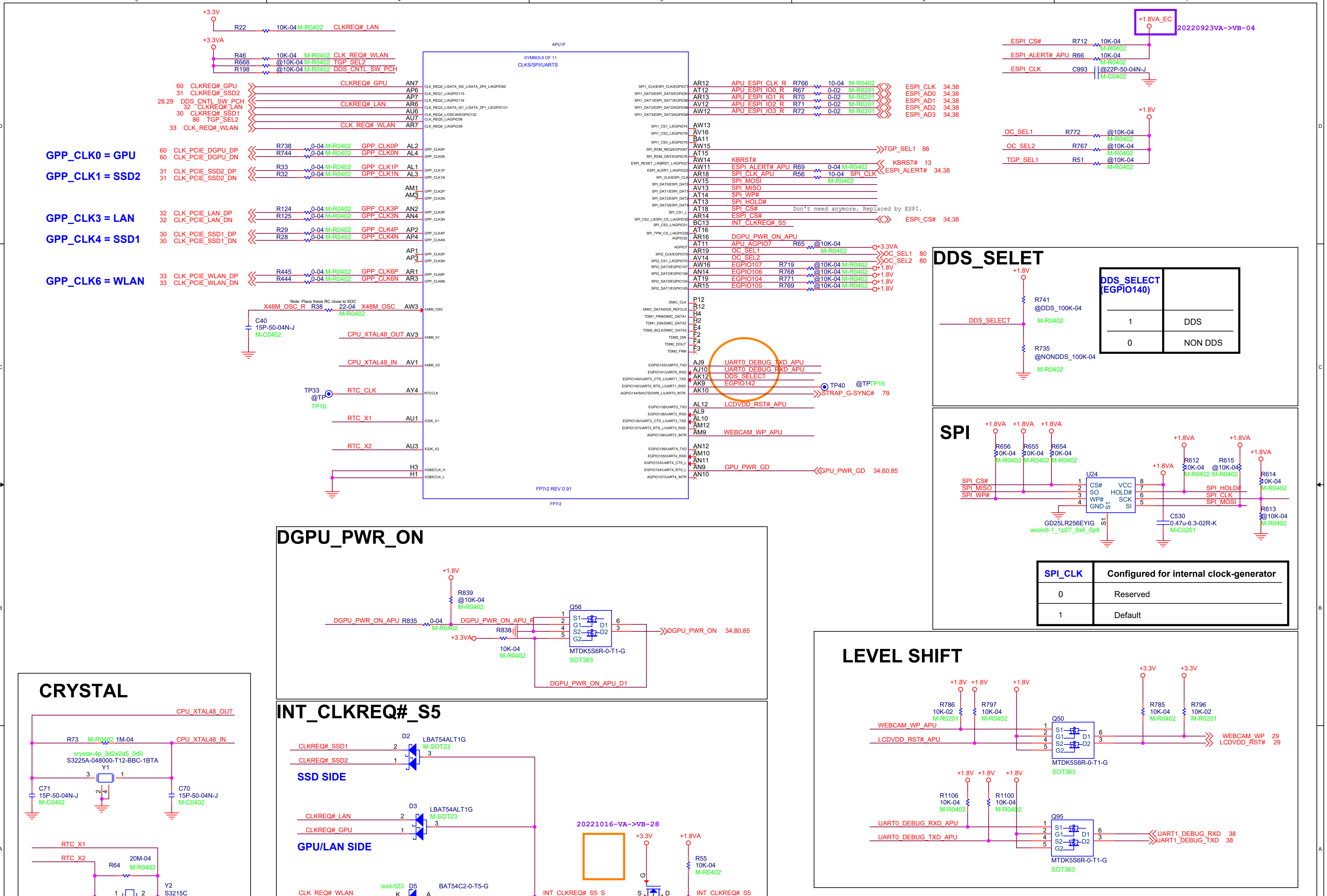
SYS_RESET_L	Normal powerup/reset timing
0	Reserved
1	Default

Uniwill Technology Inc

Title: GMXBGXX

Size: Custom | Document Number: 13 AMD AZ/I2C/ACPI/GPIO | Rev: VB

Date: Friday, October 28, 2022 | Sheet 13 of 87



DDS_SELECT (EGPIO140)	
1	DDS
0	NON DDS

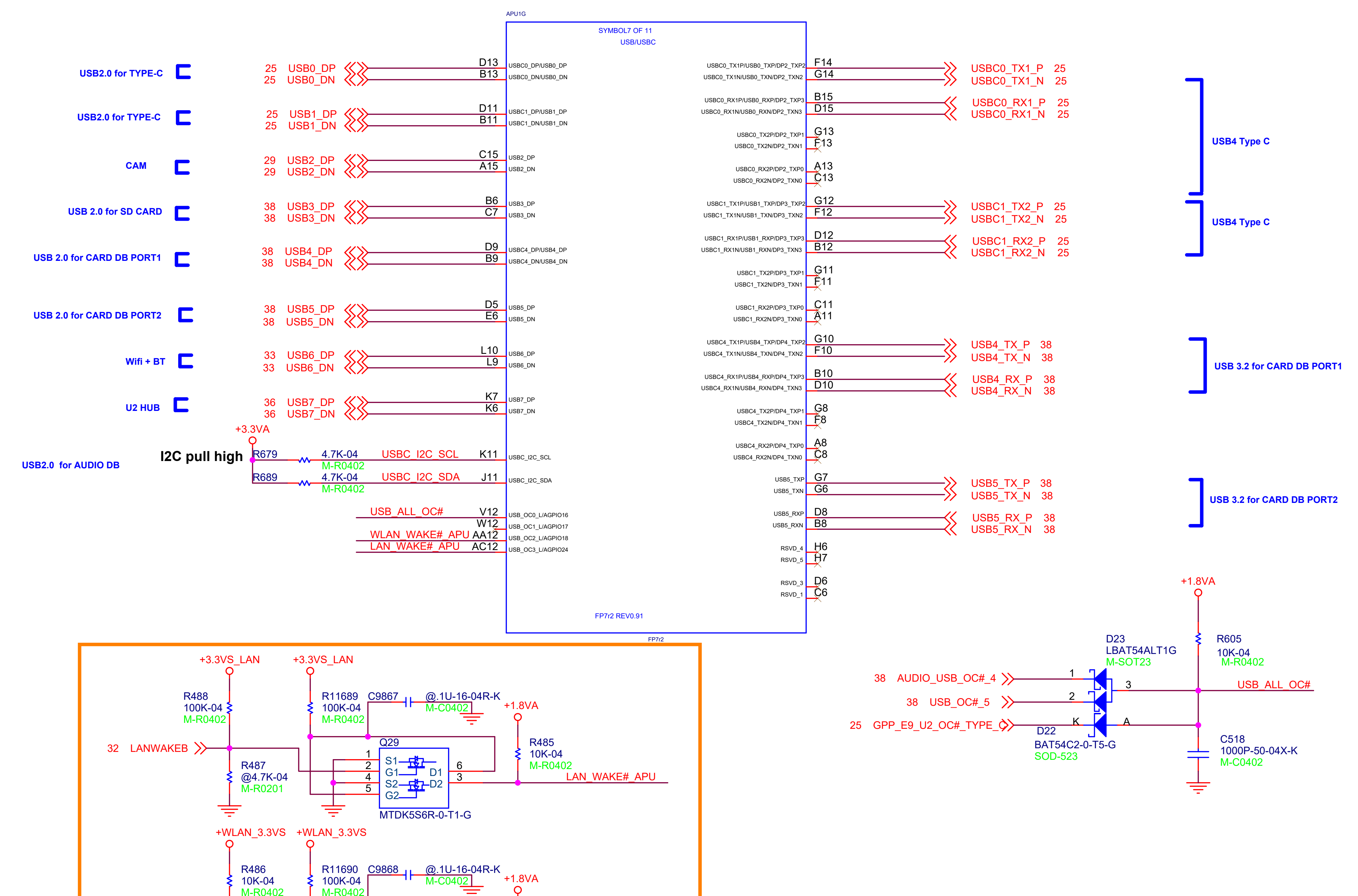
SPI_CLK	Configured for internal clock-generator
0	Reserved
1	Default

Uniwill Technology Inc

Title: GMXBGXX

Size: Custom | Document Number: 14 AMD CLK/UART/SPI/eSPI | Rev: VB

Date: Friday, October 28, 2022 | Sheet 14 of 87

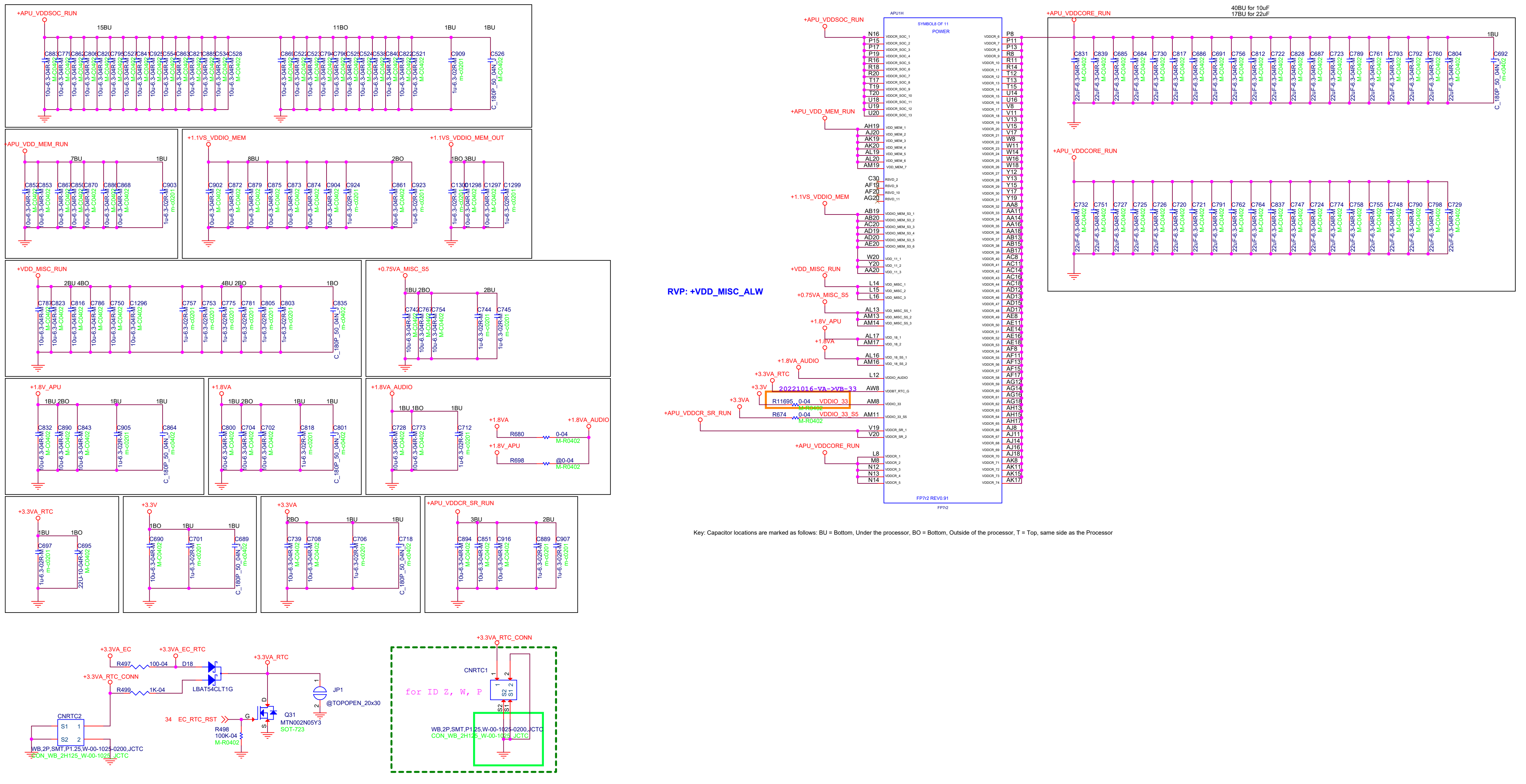


Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	15 AMD USB	VB

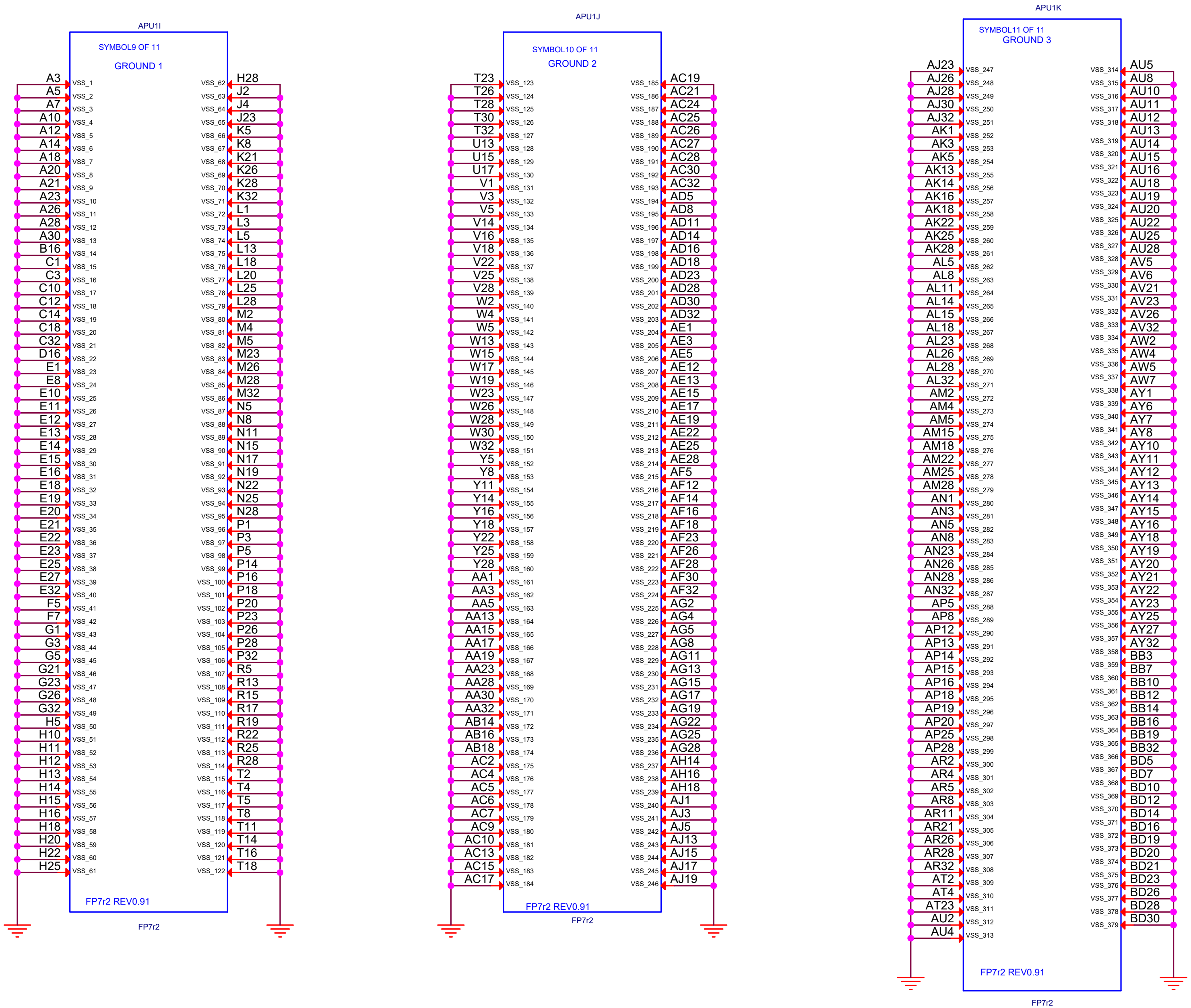
Date: Friday, October 28, 2022 Sheet 15 of 87



Key: Capacitor locations are marked as follows: BU = Bottom, Under the processor, BO = Bottom, Outside of the processor, T = Top, same side as the Processor

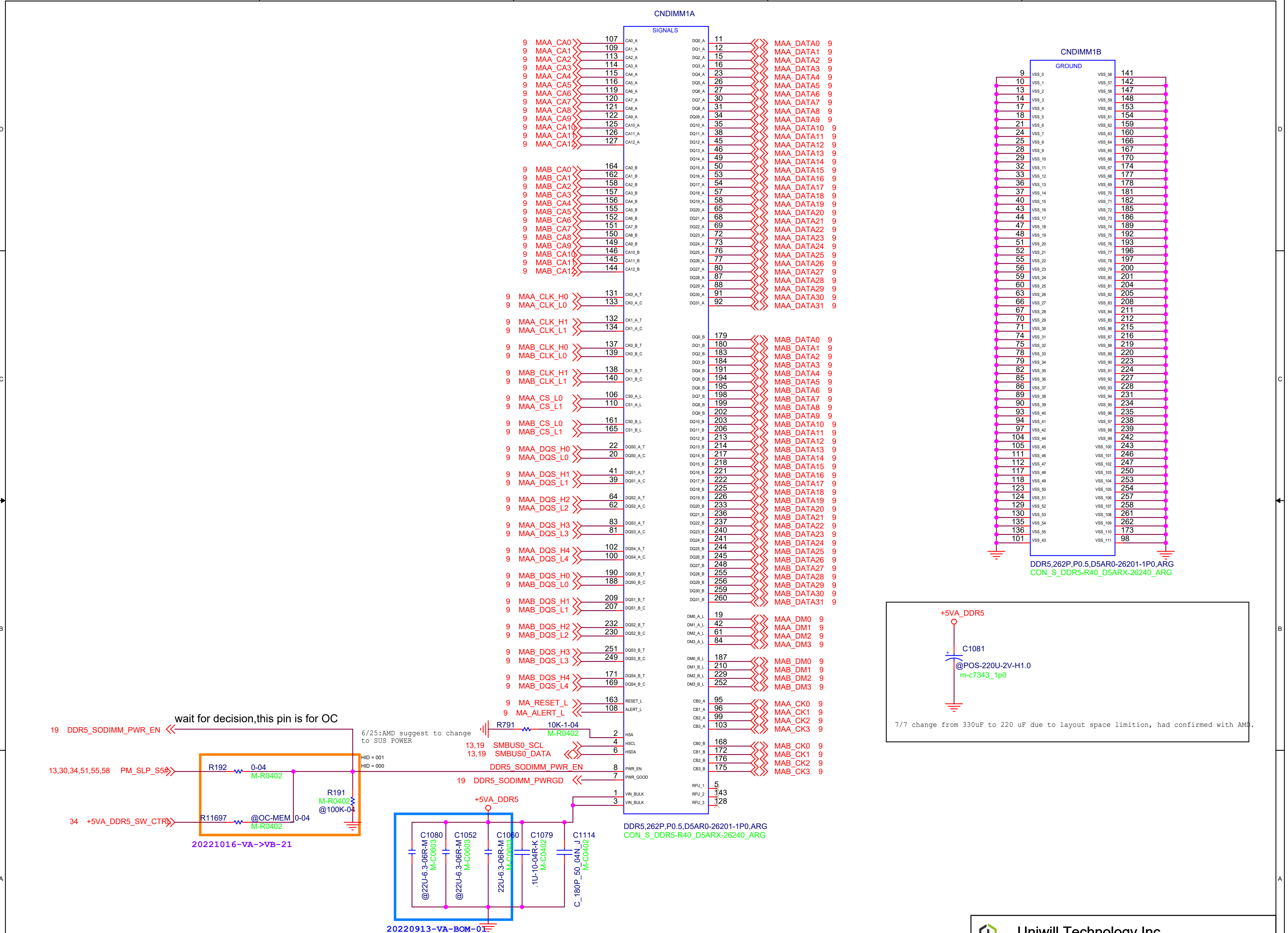
Uniwill Technology Inc

Title	GMXBGXX	
Size Custom	Document Number 16 AMD POWER	Rev VB
Date: Friday, October 28, 2022	Sheet 16 of 87	



Uniwill Technology Inc

Title	GMXBGXX	
Size Custom	Document Number 17 AMD GND	Rev VB
Date: Friday, October 28, 2022	Sheet 17 of 87	

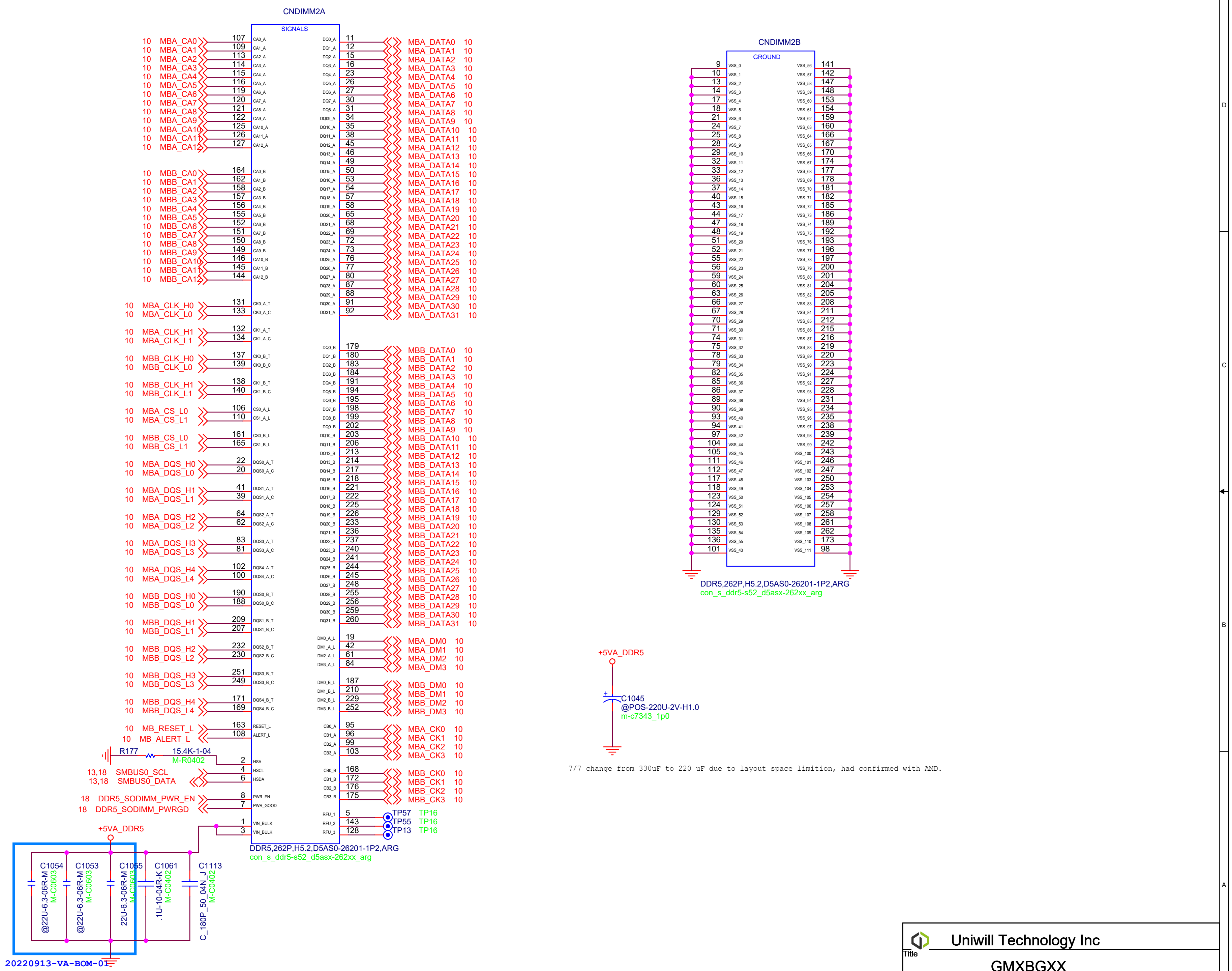


Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	18 DDR5 SODIMM-A	VB

Date: Friday, October 28, 2022 Sheet 18 of 87



Uniwill Technology Inc

Title	GMXBGXX	
Size: Custom	Document Number: 19 DDR5 SODIMM-B	Rev: VB
Date: Friday, October 28, 2022	Sheet 19 of 87	

Uniwill Technology Inc			
Title	GMXBGXX		
Size A	Document Number 20 Reserved		Rev VB
Date: Friday, October 28, 2022	Sheet 20	of 87	

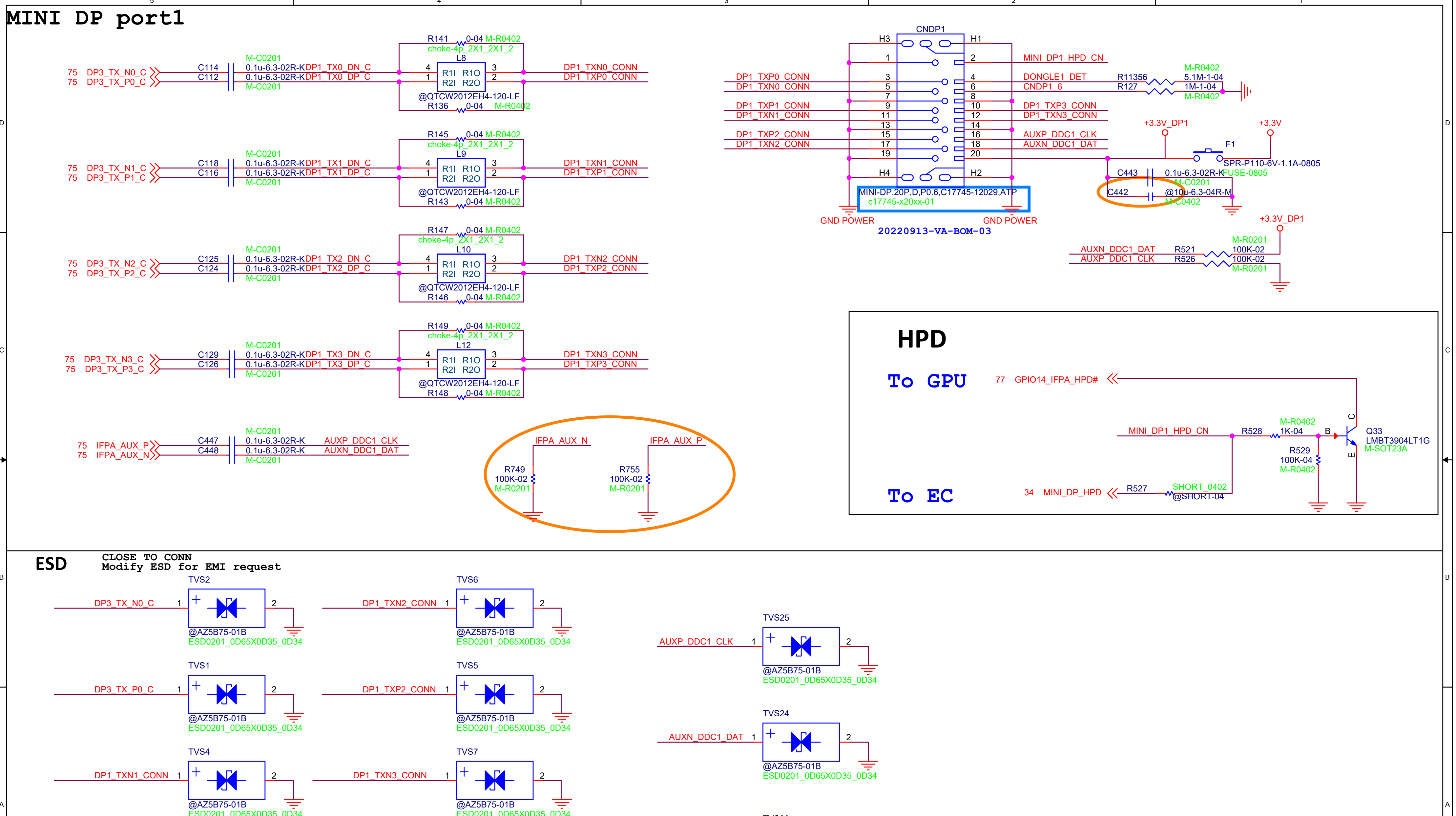
Uniwill Technology Inc

Title

GMXBGXX

Size	Document Number	Rev
A	21 Reserved	VB

Date: Friday, October 28, 2022 Sheet 21 of 87



Uniwill Technology Inc	
Title	GMXBGXX
Size: B	Document Number: 22 MINI DP	Rev: VB
Date: Friday, October 28, 2022	Sheet 22 of 87

5 4 3 2 1

D

C

B

A

Uniwill Technology Inc			
Title	GMXBGXX		
Size A	Document Number 23 MUX		Rev VB
Date: Friday, October 28, 2022	Sheet 23 of 87		

5 4 3 2 1

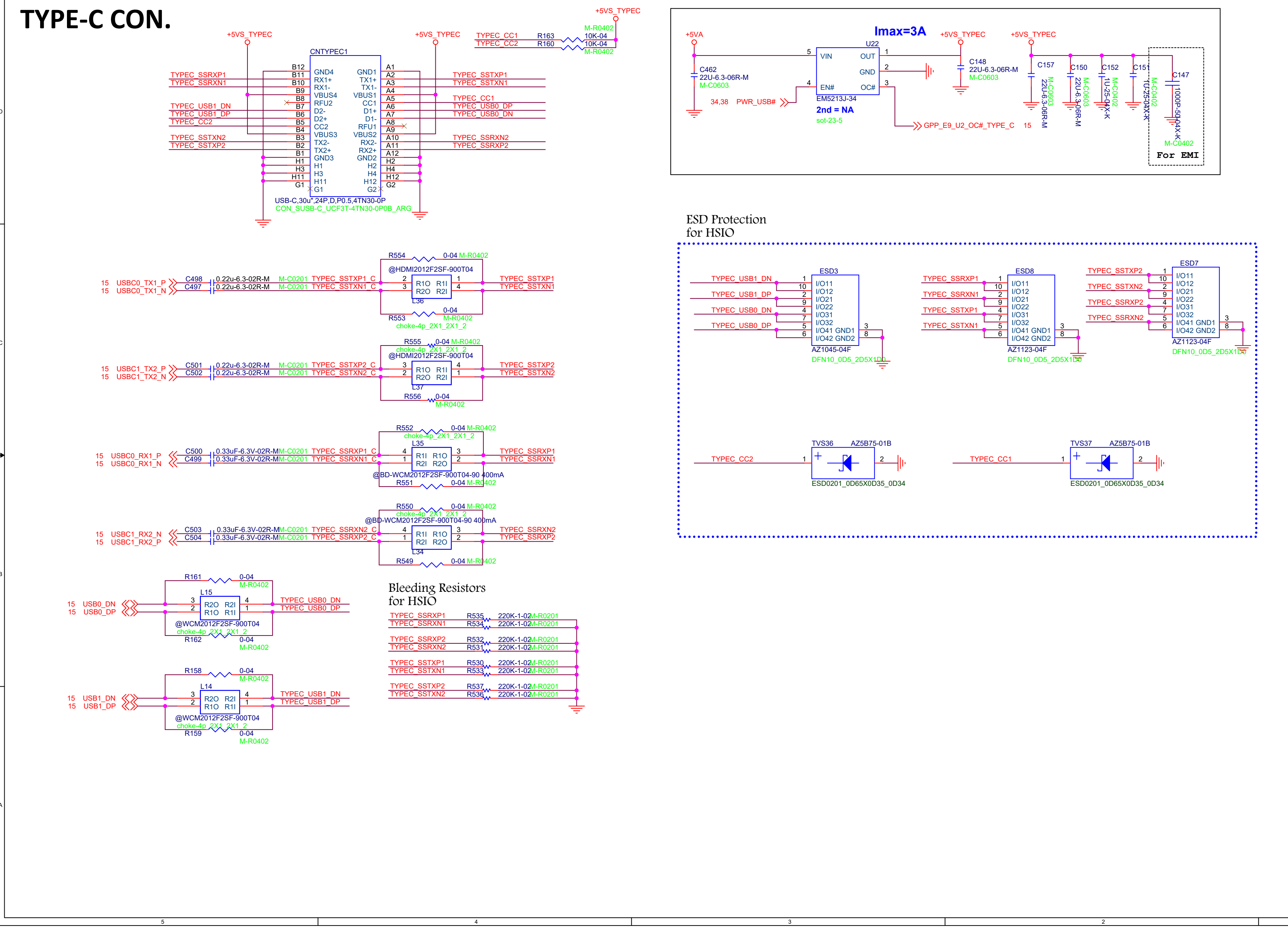
Uniwill Technology Inc

Title

GMXBGXX

Size	Document Number	Rev
Custom	24 PD_IT8851	VB

Date: Friday, October 28, 2022 Sheet 24 of 87



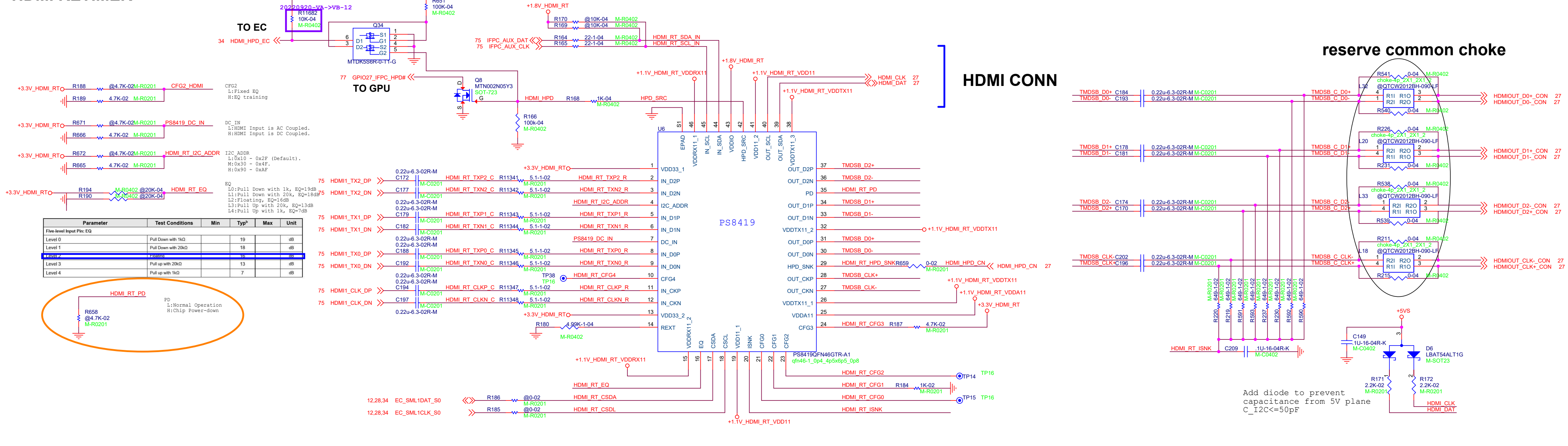
Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	25 TYPE-C	VB

Date: Friday, October 28, 2022 Sheet 25 of 87

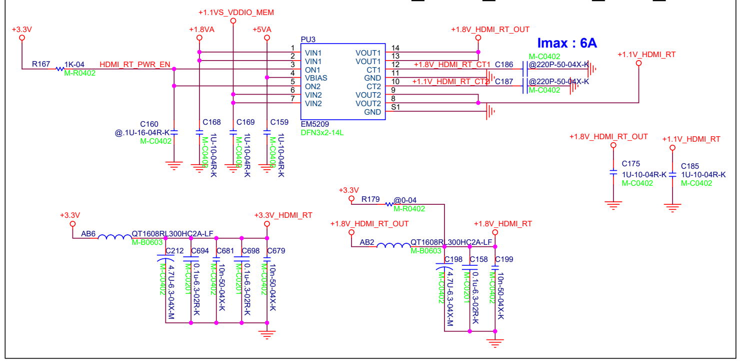
HDMI RETIMER



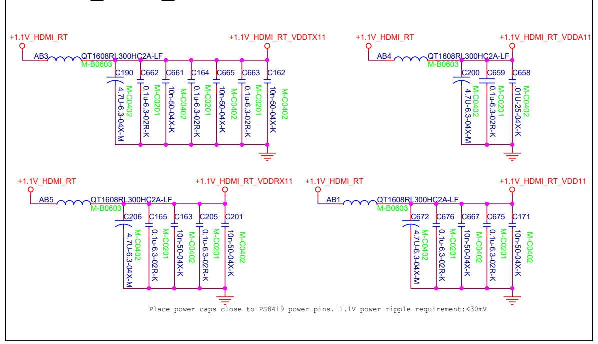
Parameter	Test Conditions	Min	Typ[b]	Max	Unit
Five-level Input Pin: EQ					
Level 0	Pull Down with 1kΩ		19		dB
Level 1	Pull Down with 20kΩ		18		dB
Level 2	Floating		16		dB
Level 3	Pull up with 20kΩ		13		dB
Level 4	Pull up with 1kΩ		7		dB

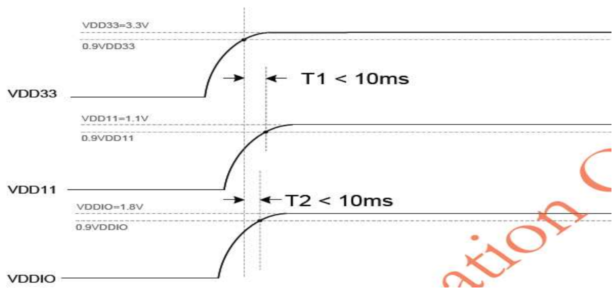
HDMI RETIMER POWER

+3.3V_HDMI_RT/+1.8V_VDD_IO



+1.1V_HDMI_RT

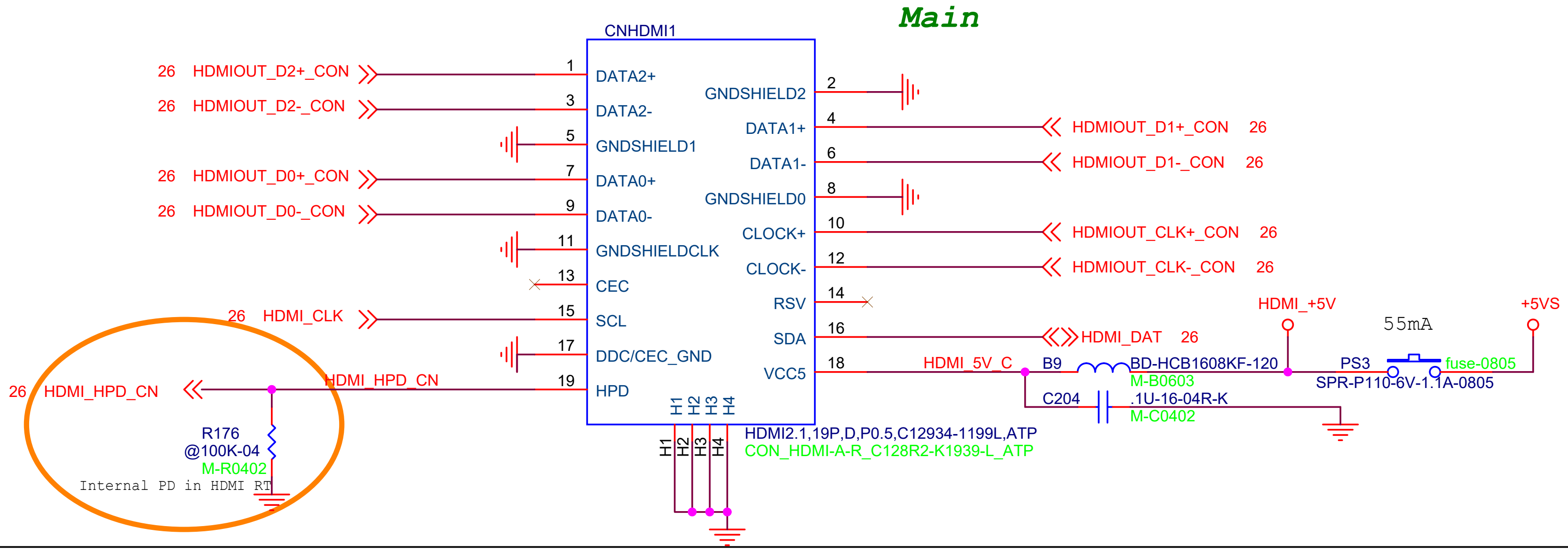




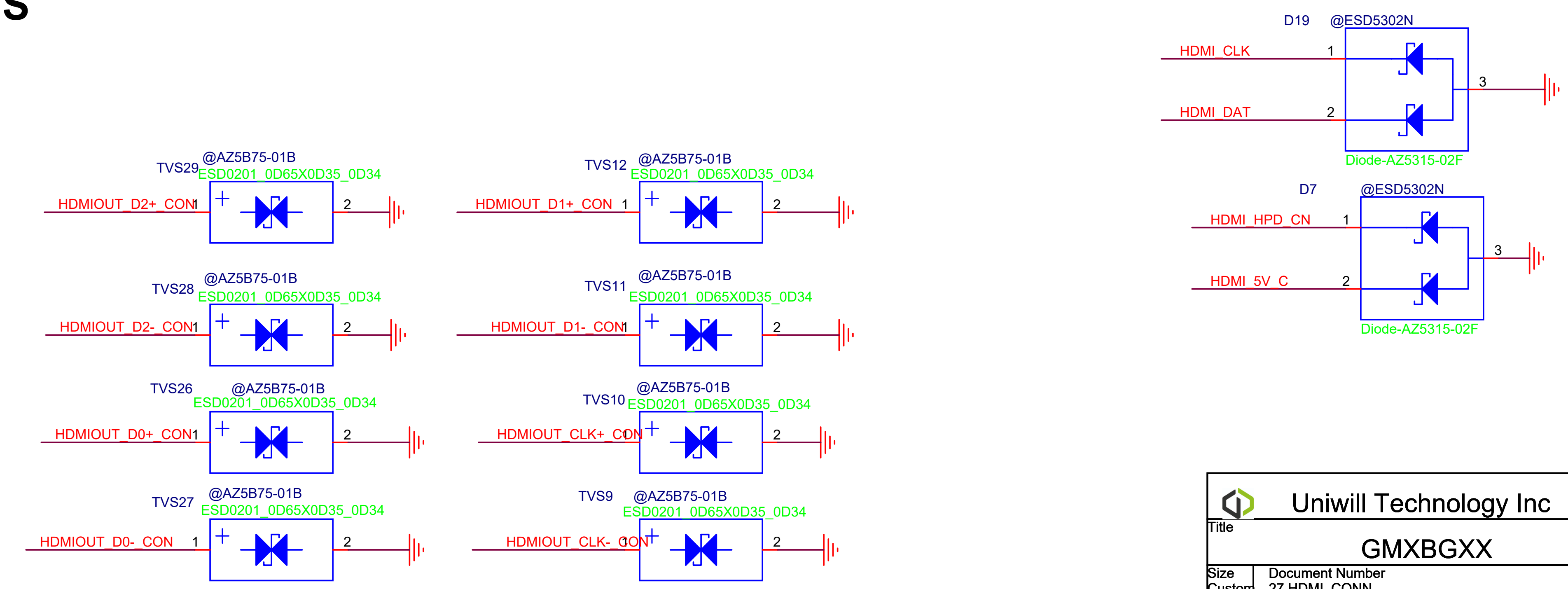
Uniwill Technology Inc

Title	GMXBGXX	
Size Custom	Document Number 26 HDMI_RETIMER	Rev VB
Date: Friday, October 28, 2022	Sheet 26 of 87	

HDMI CONN

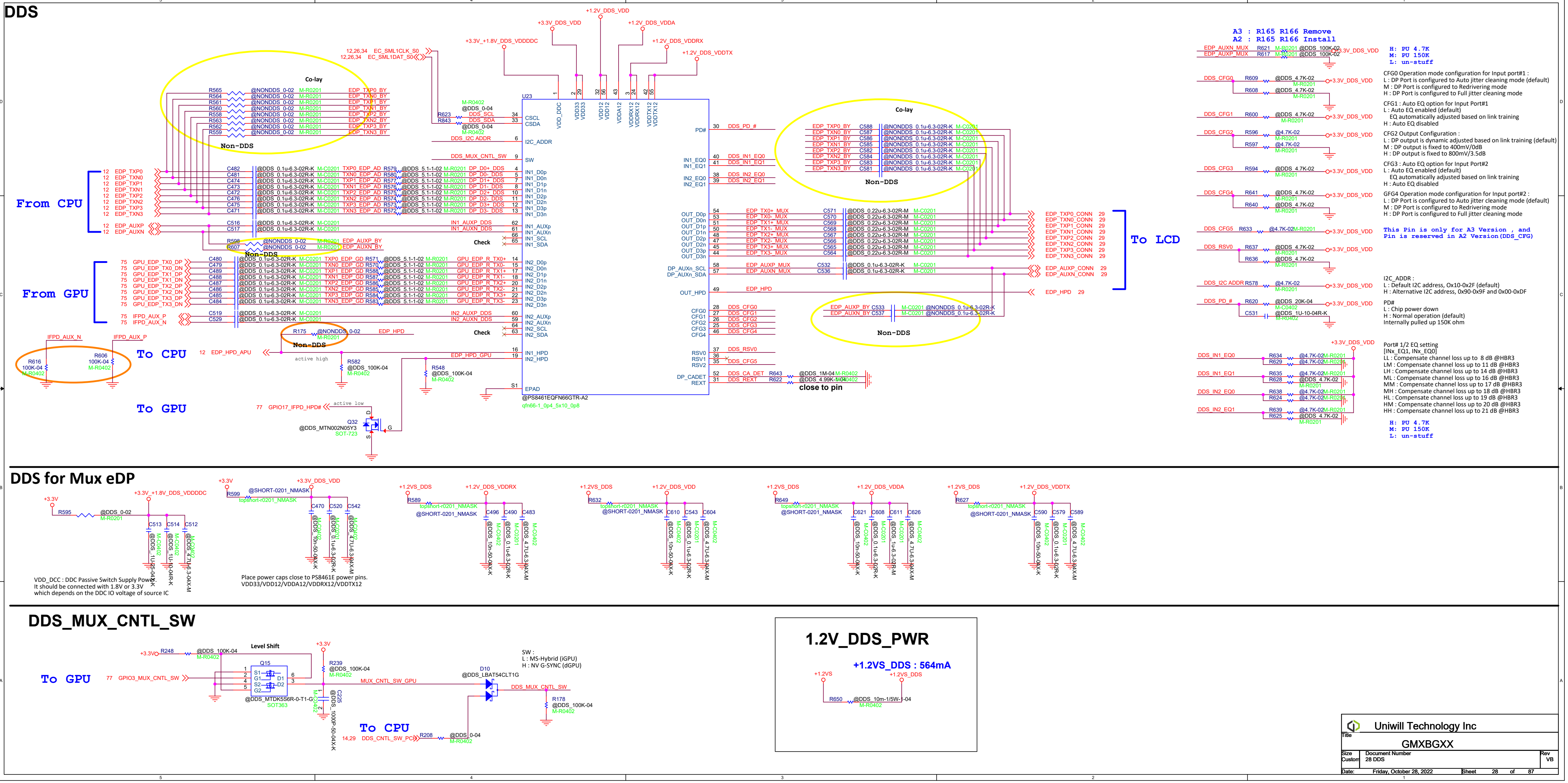


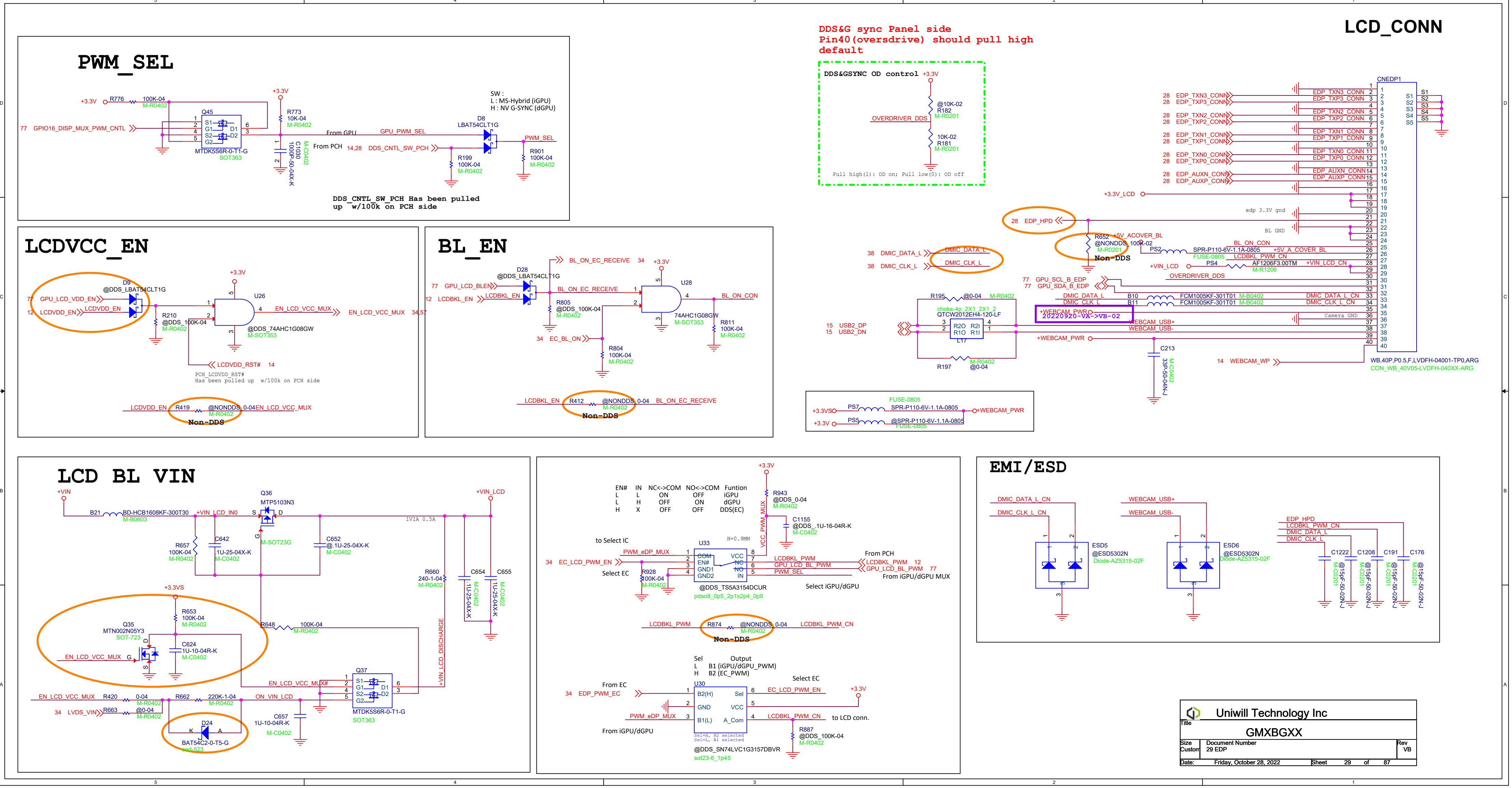
TVS



Uniwill Technology Inc

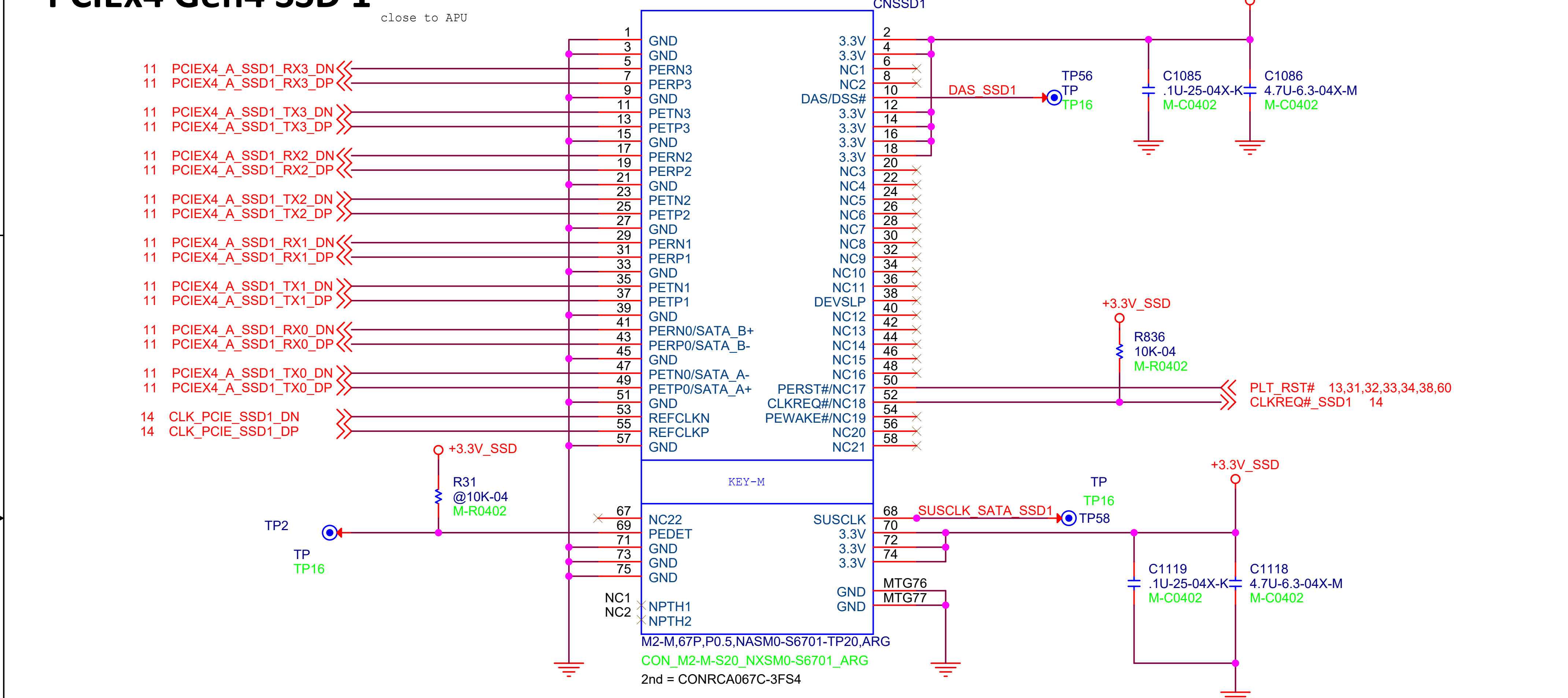
Title	GMXBGXX	
Size: Custom	Document Number: 27 HDMI_CONN	Rev: VB
Date: Friday, October 28, 2022	Sheet 27 of 87	


DDS
DDS for Mux eDP
DDS_MUX_CNTL_SW
1.2V_DDS_PWR
+1.2VS_DDS : 564mA
From CPU
From GPU
To LCD
To CPU
To GPU
Co-lay
Non-DDS
Level Shift
close to pin
A3 : R165 R166 Remove
A2 : R165 R166 Install
H: PU 4.7K
M: PU 150K
L: un-stuff
CFG0 Operation mode configuration for Input port#1 :
L : DP Port is configured to Auto jitter cleaning mode (default)
M : DP Port is configured to Redrivering mode
H : DP Port is configured to Full jitter cleaning mode
CFG1 : Auto EQ option for Input Port#1
L : Auto EQ enabled (default)
EQ automatically adjusted based on link training
H : Auto EQ disabled
CFG2 Output Configuration :
L : DP output is dynamic adjusted based on link training (default)
M : DP output is fixed to 400mV/0dB
H : DP output is fixed to 800mV/3.5dB
CFG3 : Auto EQ option for Input Port#2
L : Auto EQ enabled (default)
EQ automatically adjusted based on link training
H : Auto EQ disabled
GFG4 Operation mode configuration for Input port#2 :
L : DP Port is configured to Auto jitter cleaning mode (default)
M : DP Port is configured to Redrivering mode
H : DP Port is configured to Full jitter cleaning mode
This Pin is only for A3 Version , and
Pin is reserved in A2 Version(DDS_CFG)
I2C_ADDR :
L : Default I2C address, 0x10-0x2F (default)
H : Alternative I2C address, 0x90-0x9F and 0x00-0x2DF
PD#
L : Chip power down
H : Normal operation (default)
Internally pulled up 150K ohm
Port#1/2 EQ setting
[INx_EQ1, INx_EQ0]
LL : Compensate channel loss up to 8 dB @HBR3
LM : Compensate channel loss up to 11 dB @HBR3
LH : Compensate channel loss up to 14 dB @HBR3
ML : Compensate channel loss up to 16 dB @HBR3
MM : Compensate channel loss up to 17 dB @HBR3
MH : Compensate channel loss up to 18 dB @HBR3
HL : Compensate channel loss up to 19 dB @HBR3
HM : Compensate channel loss up to 20 dB @HBR3
HH : Compensate channel loss up to 21 dB @HBR3
H: PU 4.7K
M: PU 150K
L: un-stuff
VDD_DCC : DDC Passive Switch Supply Power.
It should be connected with 1.8V or 3.3V
which depends on the DDC IO voltage of source IC
Place power caps close to PS8461E power pins.
VDD33/VDD12/VDDA12/VDDRX12/VDDTX12
SW :
L : MS-Hybrid (iGPU)
H : NV G-SYNC (dGPU)
U23
@PS8461EQFN66GTR-A2
Uniwill Technology Inc
Title
GMXBGXX
Size Custom
Document Number
28 DDS
Rev
VB
Date: Friday, October 28, 2022
Sheet 28 of 87

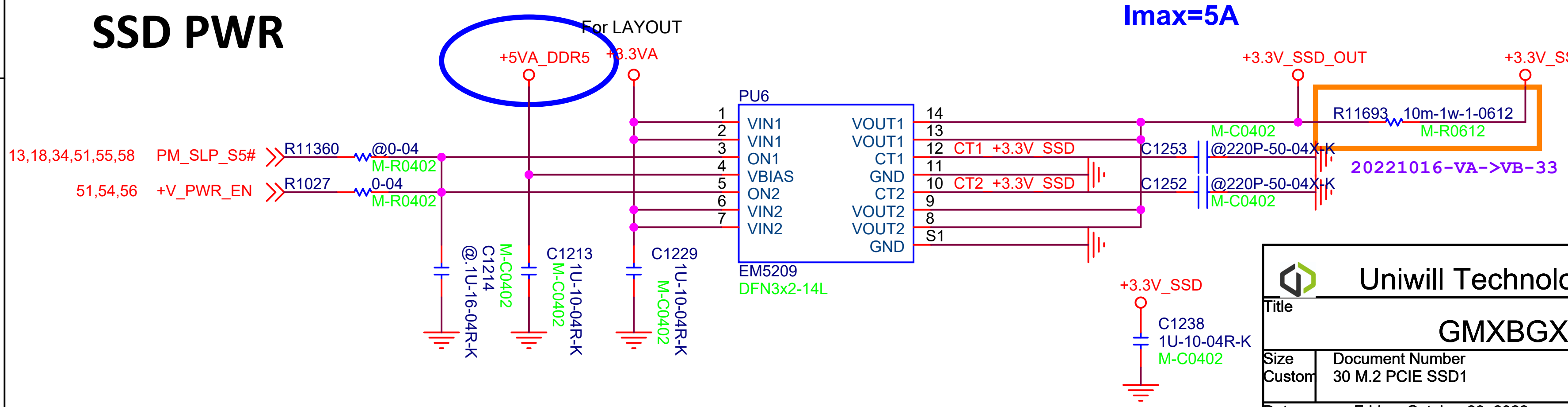

LCD_CONN
DDS&G sync Panel side
Pin40(oversdrive) should pull high
default
DDS&GSYNC OD control
OVERDRIVER_DDS
Pull high(1): OD on; Pull low(0): OD off
PWM_SEL
SW :
L : MS-Hybrid (iGPU)
H : NV G-SYNC (dGPU)
77 GPIO16_DISP_MUX_PWM_CNTL
From GPU
GPU_PWM_SEL
From PCH
14,28 DDS_CNTL_SW_PCH
PWM_SEL
DDS_CNTL_SW_PCH Has been pulled
up w/100k on PCH side
LCDVCC_EN
GPU_LCD_VDD_EN
LCDVDD_EN
EN_LCD_VCC_MUX
LCDVDD_RST#
PCH_LCDVDD_RST#
Has been pulled up w/100k on PCH side
Non-DDS
BL_EN
BL_ON_EC_RECEIVE
GPU_LCD_BLEN
LCDBKL_EN
BL_ON_CON
34 EC_BL_ON
Non-DDS
LCD BL VIN
+VIN
+VIN_LCD
+VIN_LCD_IN0
EN_LCD_VCC_MUX
LVDS_VIN
ON_VIN_LCD
+VIN_LCD_DISCHARGE
1VIA 0.5A
EN# IN NC<->COM NO<->COM Funtion
L L ON OFF iGPU
L H OFF ON dGPU
H X OFF OFF DDS(EC)
to Select IC
PWM_eDP_MUX
34 EC_LCD_PWM_EN
Select EC
From PCH
LCDBKL_PWM
GPU_LCD_BL_PWM
PWM_SEL
From iGPU/dGPU MUX
Select iGPU/dGPU
Non-DDS
LCDBKL_PWM_CN
Sel Output
L B1 (iGPU/dGPU_PWM)
H B2 (EC_PWM)
From EC
34 EDP_PWM_EC
Select EC
EC_LCD_PWM_EN
to LCD conn.
From iGPU/dGPU
EMI/ESD
DMIC_DATA_L_CN
DMIC_CLK_L_CN
WEBCAM_USB+
WEBCAM_USB-
EDP_HPD
LCDBKL_PWM_CN
DMIC_DATA_L
DMIC_CLK_L
CNEDP1
EDP_TXN3_CONN
EDP_TXP3_CONN
EDP_TXN2_CONN
EDP_TXP2_CONN
EDP_TXN1_CONN
EDP_TXP1_CONN
EDP_TXN0_CONN
EDP_TXP0_CONN
EDP_AUXN_CONN
EDP_AUXP_CONN
+3.3V_LCD
28 EDP_HPD
38 DMIC_DATA_L
38 DMIC_CLK_L
+5V_ACOVER_BL
BL_ON_CON
LCDBKL_PWM_CN
+VIN_LCD
+VIN_LCD_CN
OVERDRIVER_DDS
77 GPU_SCL_B_EDP
77 GPU_SDA_B_EDP
15 USB2_DP
15 USB2_DN
+WEBCAM_PWR
20220920--VA->VB-02
14 WEBCAM_WP
Camera GND
WB,40P,P0.5,F,LVDFH-04001-TP0,ARG
CON_WB_40V05-LVDFH-040XX-ARG
+3.3VS
+3.3V
+WEBCAM_PWR
Uniwill Technology Inc
Title
GMXBGXX
Size Custom
Document Number
29 EDP
Rev VB
Date: Friday, October 28, 2022
Sheet 29 of 87

PCIEx4 Gen4 SSD 1

close to APU



SSD PWR



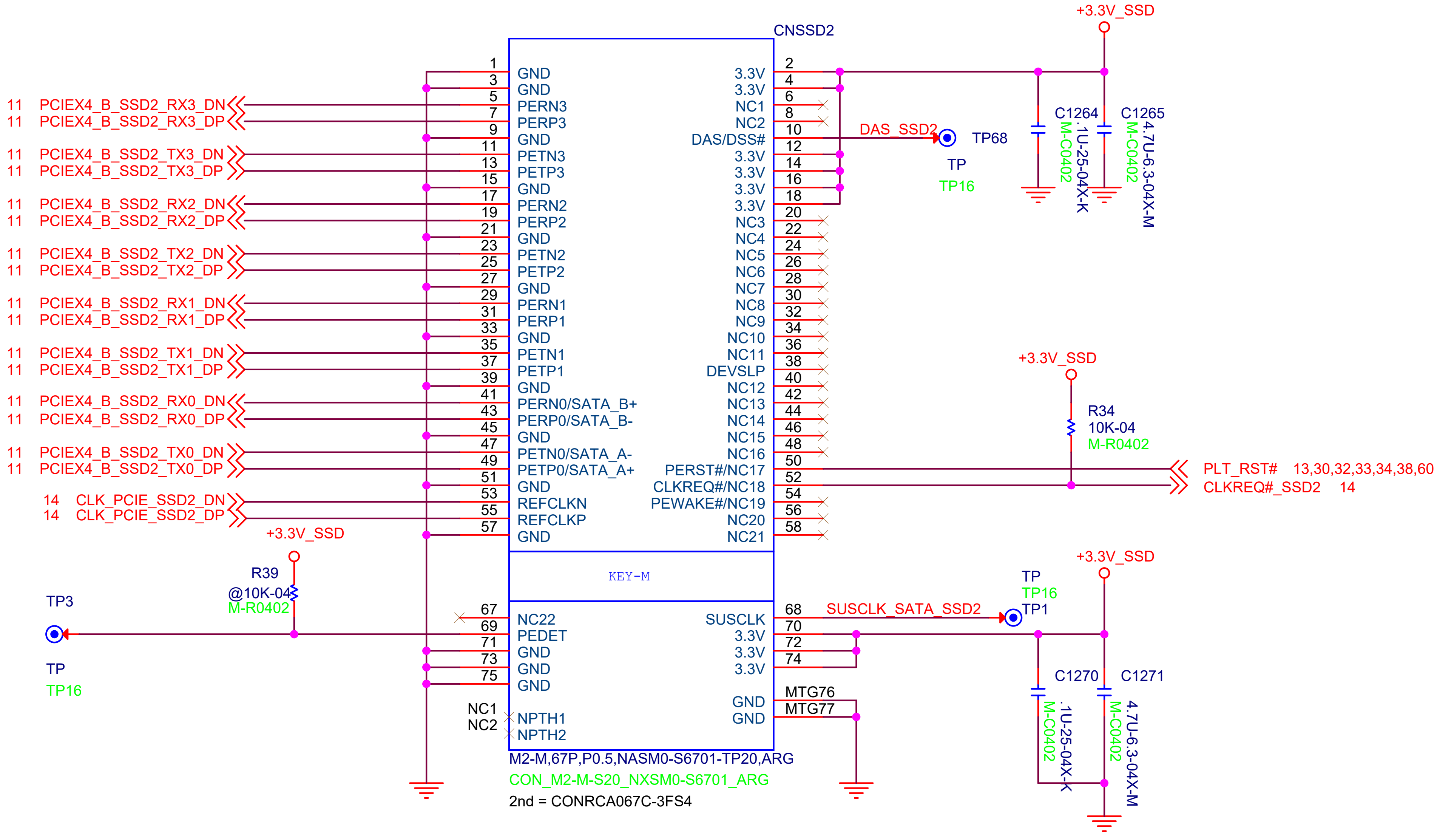
Uniwill Technology Inc

Title: GMXBGXX

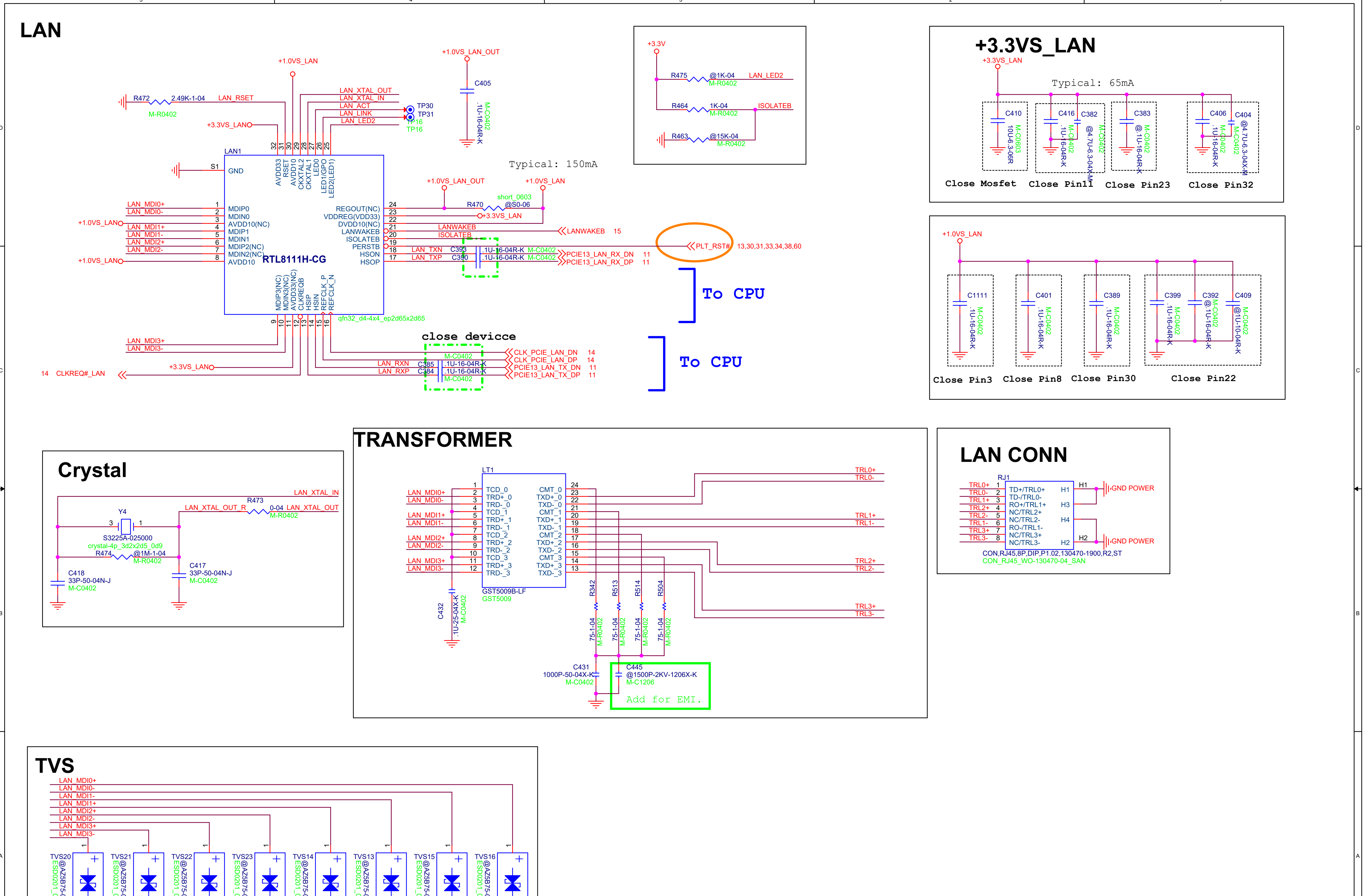
Size: Custom | Document Number: 30 M.2 PCIE SSD1 | Rev: VB

Date: Friday, October 28, 2022 | Sheet 30 of 87

PCIEx4 Gen4 SSD2



Uniwill Technology Inc		
Title: GMXBGXX		
Size: A	Document Number: 31 M.2 PCIE SSD2	Rev: VB
Date: Friday, October 28, 2022	Sheet 31 of 87	



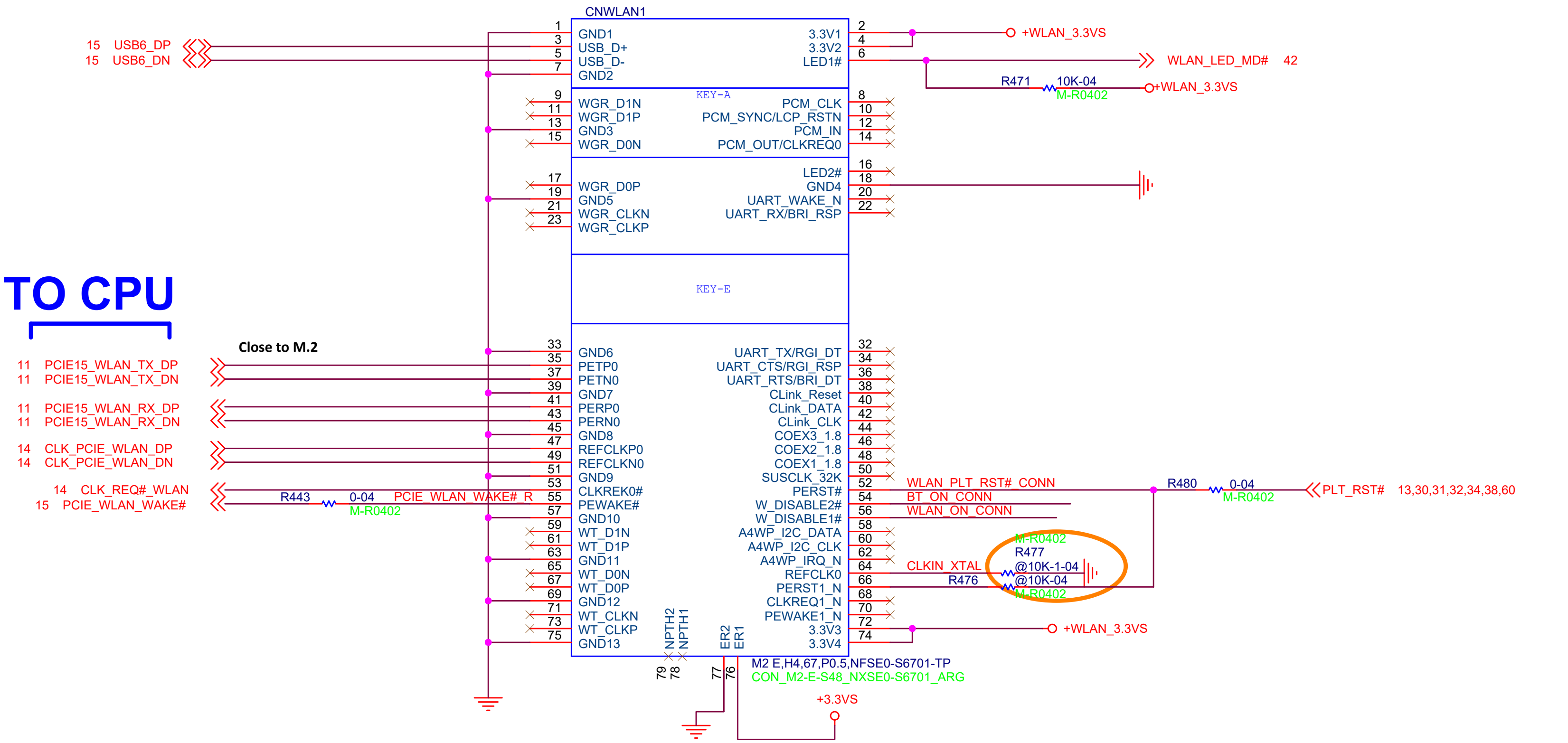
Uniwill Technology Inc

Title: GMXBGXX

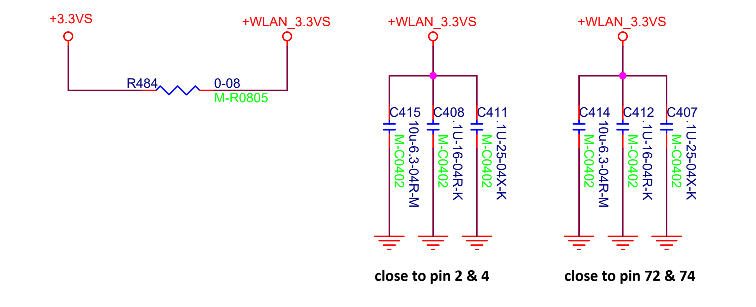
Size	Document Number	Rev
Custom	32 LAN RTL8125B(S)	VB

Date: Friday, October 28, 2022 Sheet 32 of 87

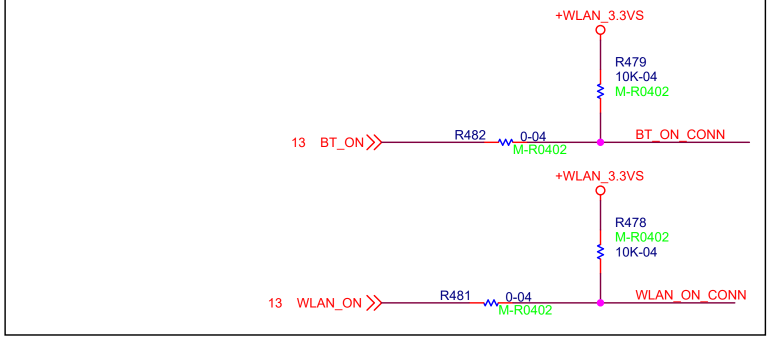
WLAN/BT CONN



WLAN PWR

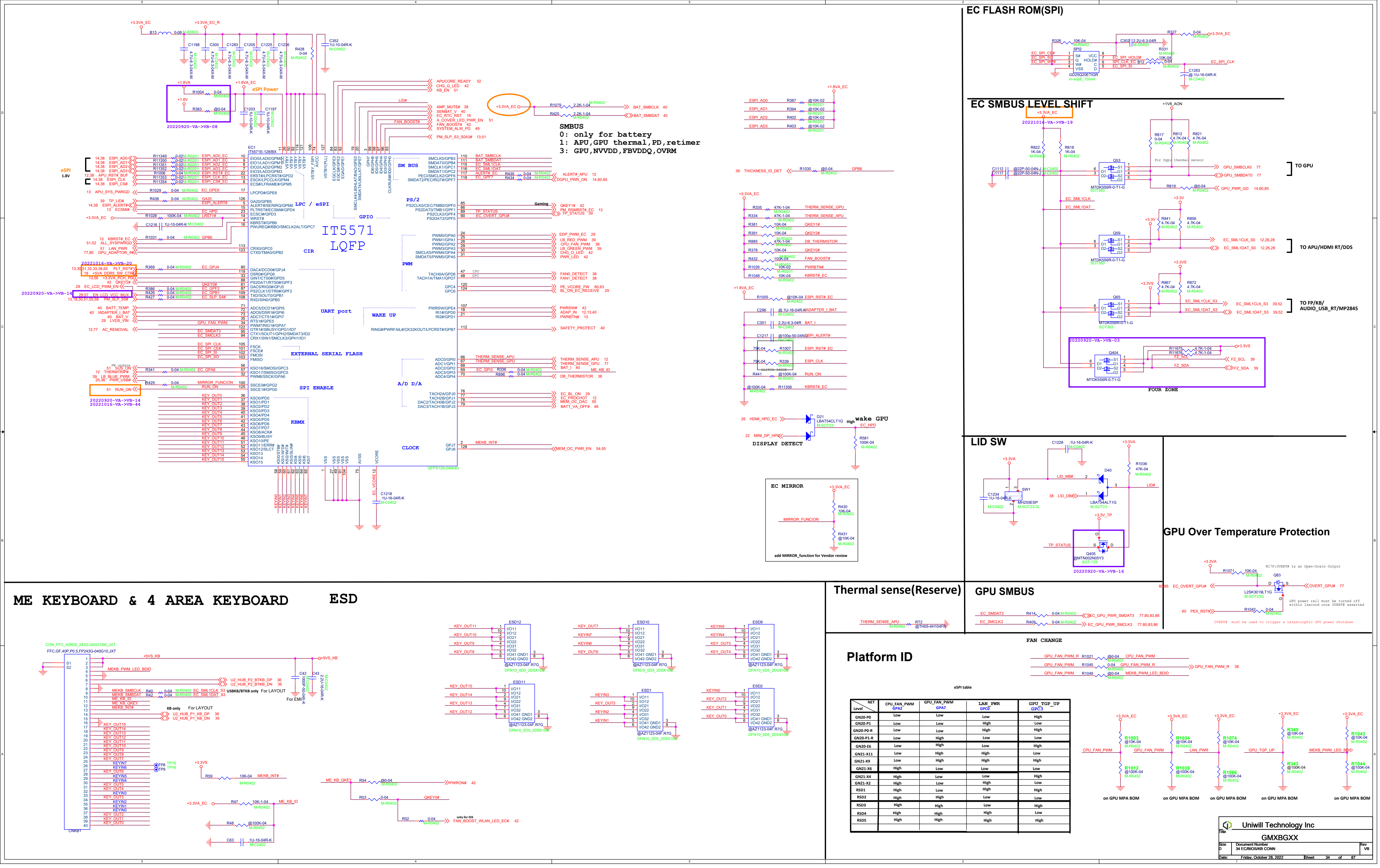


WLAN PWR



Uniwill Technology Inc

Title	GMXBGXX	
Size B	Document Number 33 WLAN	Rev VB
Date: Friday, October 28, 2022	Sheet 33 of 87	



Platform ID

eSPI table

NET / Level	CPU_FAN_PWM GPA2	GPU_FAN_PWM GPA7	LAN_PWR GPC0	GPU_TGP_UP GPC3
GN20-P0	Low	Low	Low	High
GN20-P1	Low	Low	High	Low
GN20-P0-R	Low	Low	High	High
GN20-P1-R	Low	High	Low	Low
GN20-E6	Low	High	Low	High
GN21-X11	Low	High	High	Low
GN21-X9	Low	High	High	High
GN21-X6	High	Low	Low	Low
GN21-X4	High	Low	Low	High
GN21-X2	High	Low	High	Low
RSD1	High	Low	High	High
RSD2	High	High	Low	Low
RSD3	High	High	Low	High
RSD4	High	High	High	Low
RSD5	High	High	High	High

Uniwill Technology Inc

Title: GMXBGXX

Size: D | Document Number: 34 EC/BIOS/KB CONN | Rev: VB

Date: Friday, October 28, 2022 | Sheet 34 of 87

5 4 3 2 1

D

C

B

A

Uniwill Technology Inc

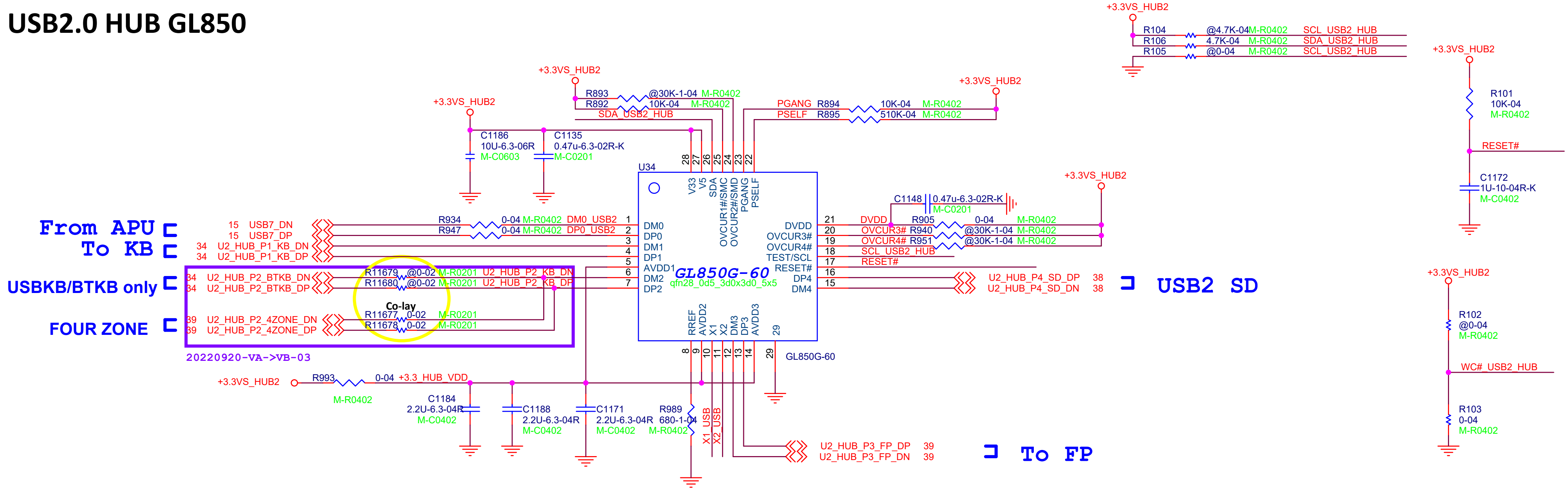
Title

GMXBGXX

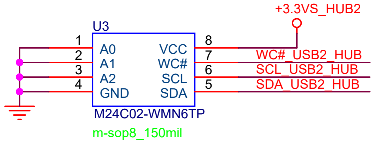
Size	Document Number	Rev
Custom	35 USB3 HUB	VB

Date: Friday, October 28, 2022 Sheet 35 of 87

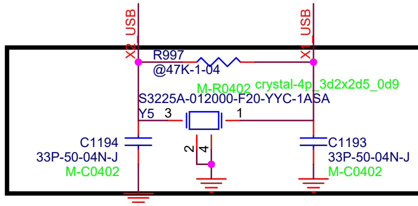
USB2.0 HUB GL850



USB2.0 HUB EEPROM

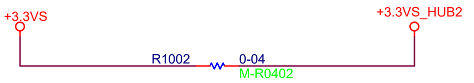


USB2.0 HUB Crystal



Check load cap
2-1 Circuit : 250B
2-2 Load Capacitance : 20pF+0.3pF
2-3 Level of Drive : 50uW

Load switch change to +3.3VS



Uniwill Technology Inc

Title	GMXBGXX	
Size B	Document Number 36 USB2 HUB	Rev VB
Date: Friday, October 28, 2022	Sheet 36 of 87	

Uniwill Technology Inc

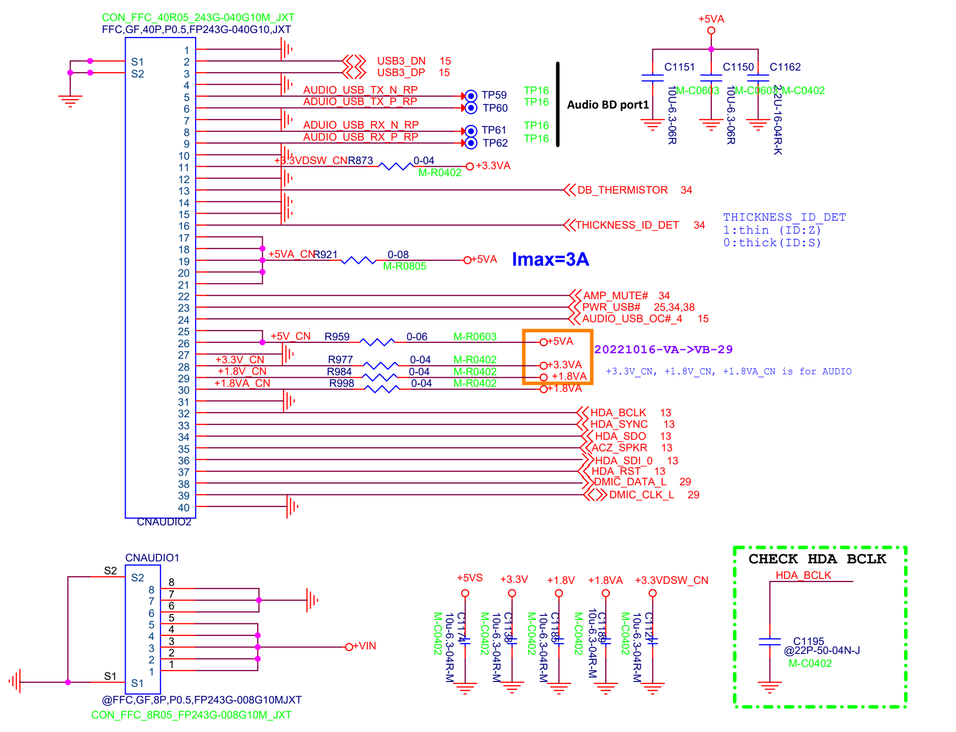
Title

GMXBGXX

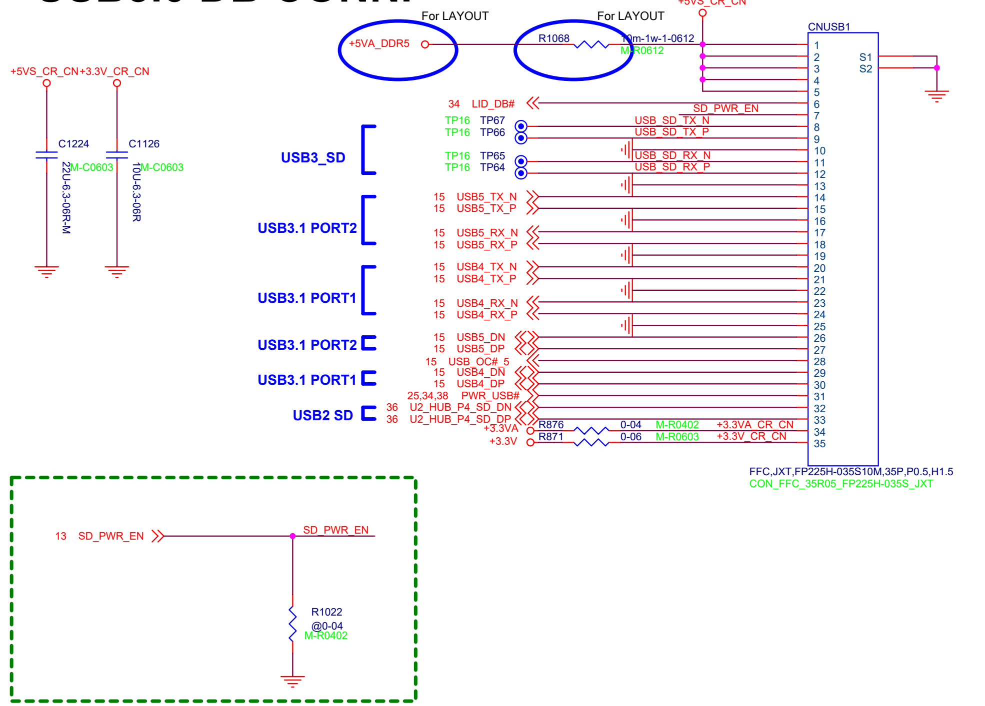
Size	Document Number	Rev
Custom	37 Reserved	VB

Date: Friday, October 28, 2022 Sheet 37 of 87

Audio&USB DB CONN.

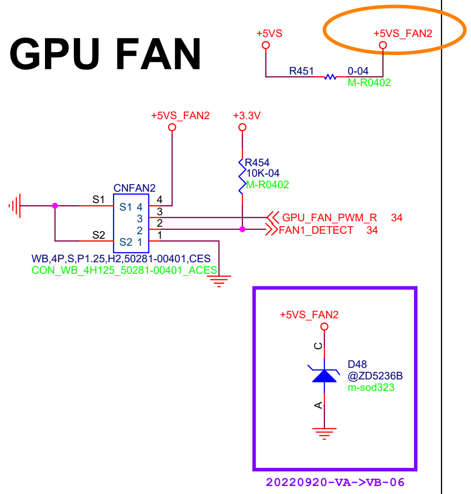


USB3.0 DB CONN.



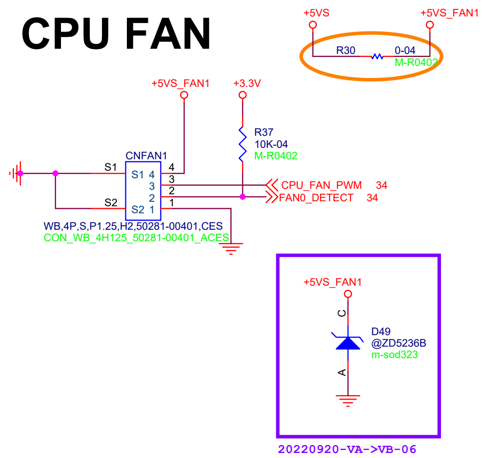
FAN CONTROLLER

GPU FAN

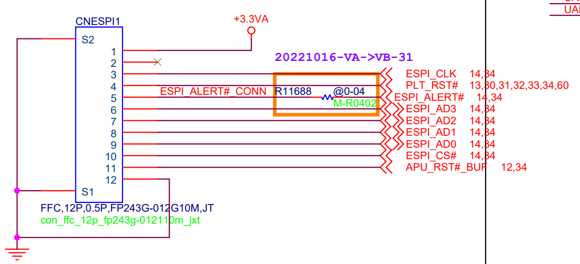


FAN CONTROLLER

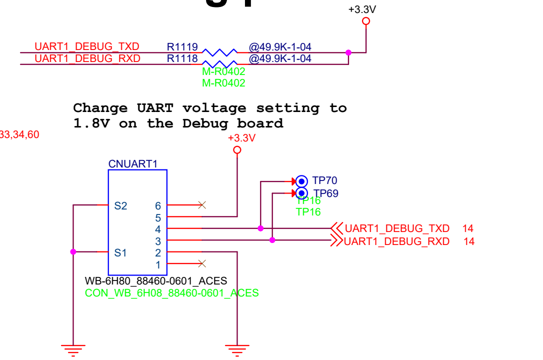
CPU FAN



ESPI debug port

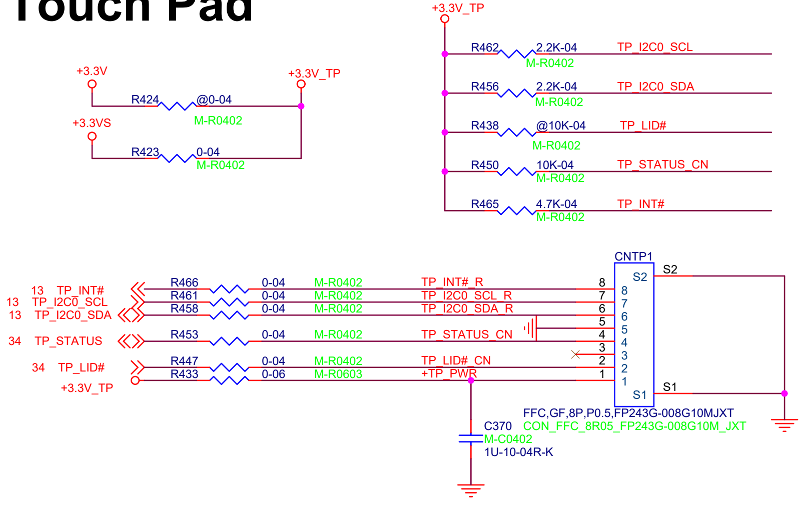


UART debug port

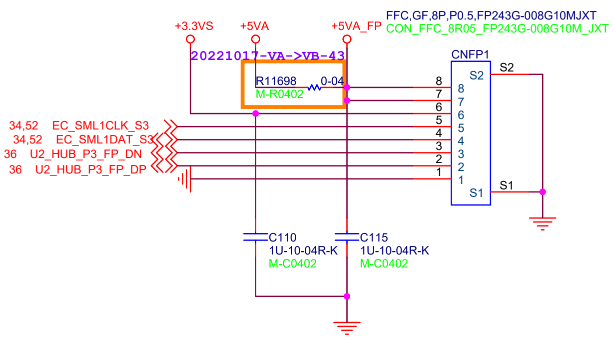


Uniwill Technology Inc		
Title	GMXBGXX	
Size Custom	Document Number 38 Audio/USB/FAN/Debug	Rev VB
Date: Friday, October 28, 2022	Sheet 38 of 87	

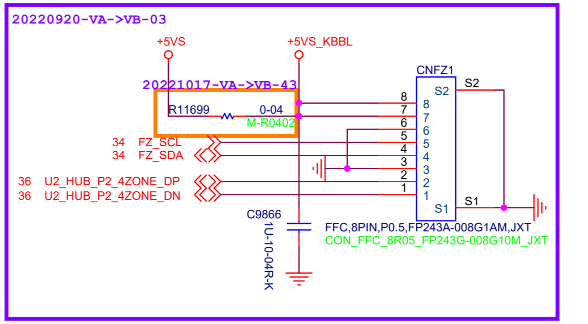
Touch Pad



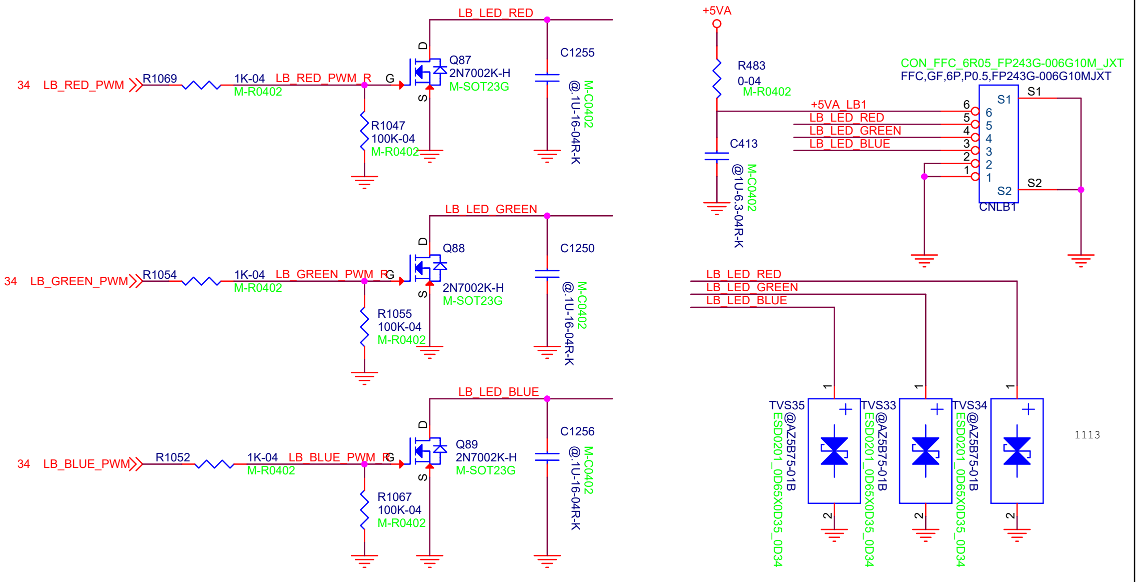
Finger Print



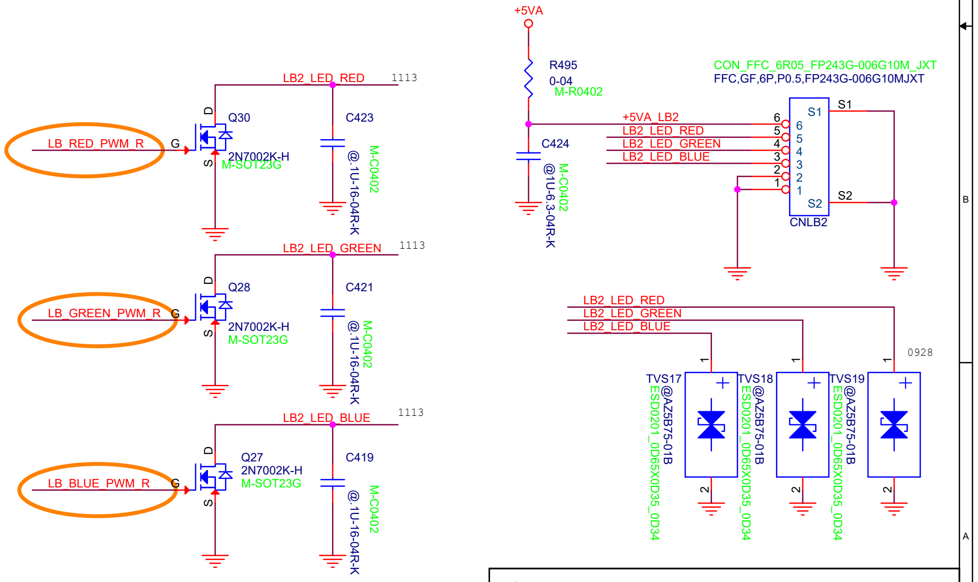
For Four Zone(A cover Logo LED)



Light bar Control

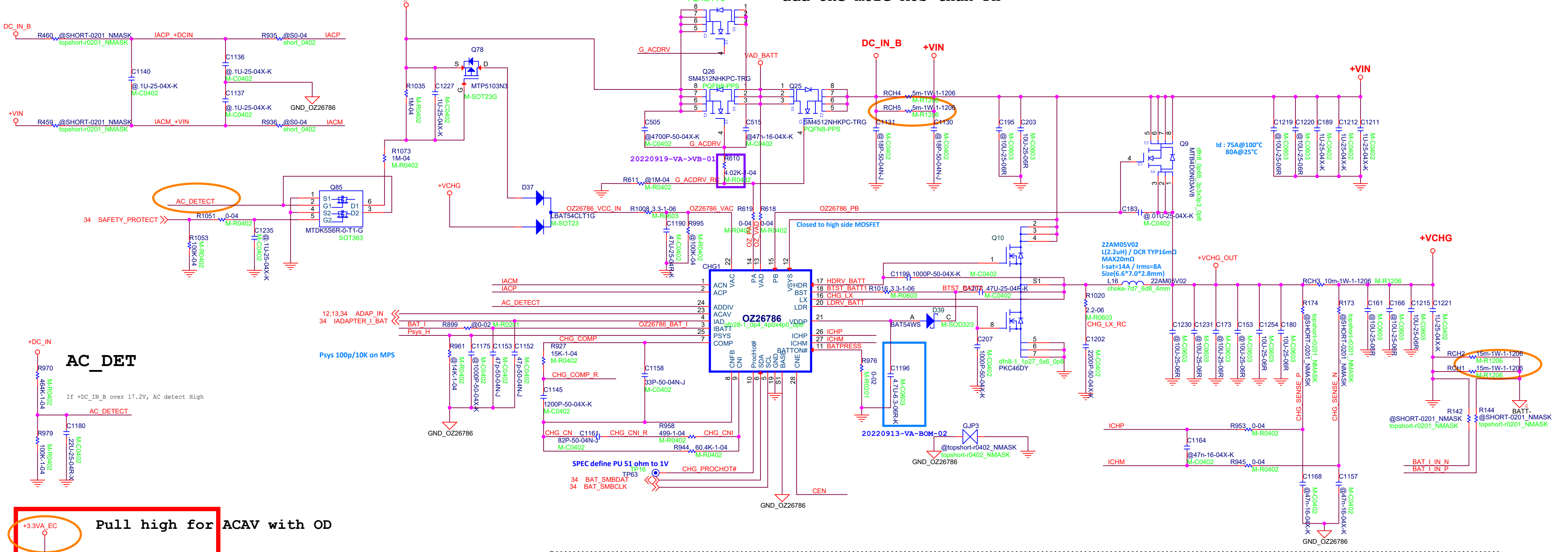


Keyboard Backlight Control



Uniwill Technology Inc		
Title	GMXBGXX	
Size Custom	Document Number 39 TP/LB/KBL/FP/Water Cooling	Rev VB
Date: Friday, October 28, 2022	Sheet 39 of 87	

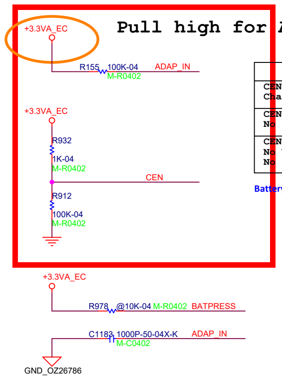
add one more MOS than PH



AC_DET

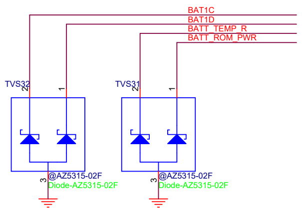
If +DC_IN_B over 17.2V, AC detect High

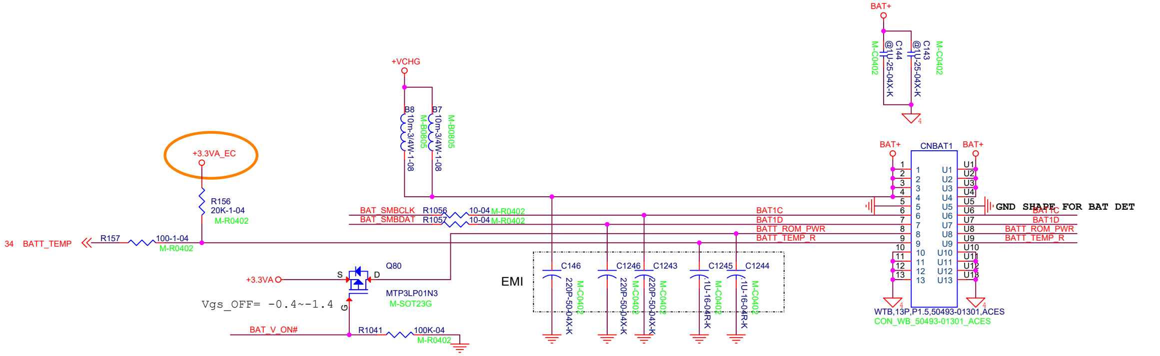
Pull high for ACAV with OD



Status	Charger power comsuption
CEN High Charger all function work	0.7mA
CEN High No Psys. Prochot#, IBATT	0.3mA
CEN Low No VDDP, No SMBus, OB Mosfet ON No Psys. Prochot#, IBATT	40uA

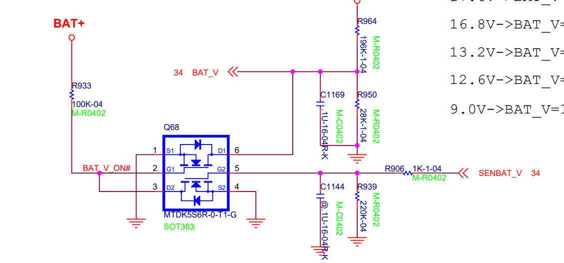
Battery mode EC shutdown , +3.3VA off, CEN low





Battery Voltage Detect

CHECK OK



17.6V->BAT_V=2.2V

16.8V->BAT_V=2.1V

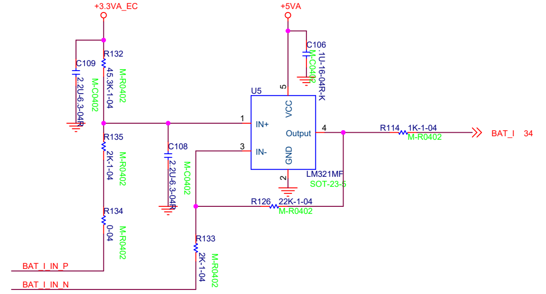
13.2V->BAT_V=1.65V

12.6V->BAT_V=1.575V

9.0V->BAT_V=1.125V

Charge / Discharge Detect

CHECK OK

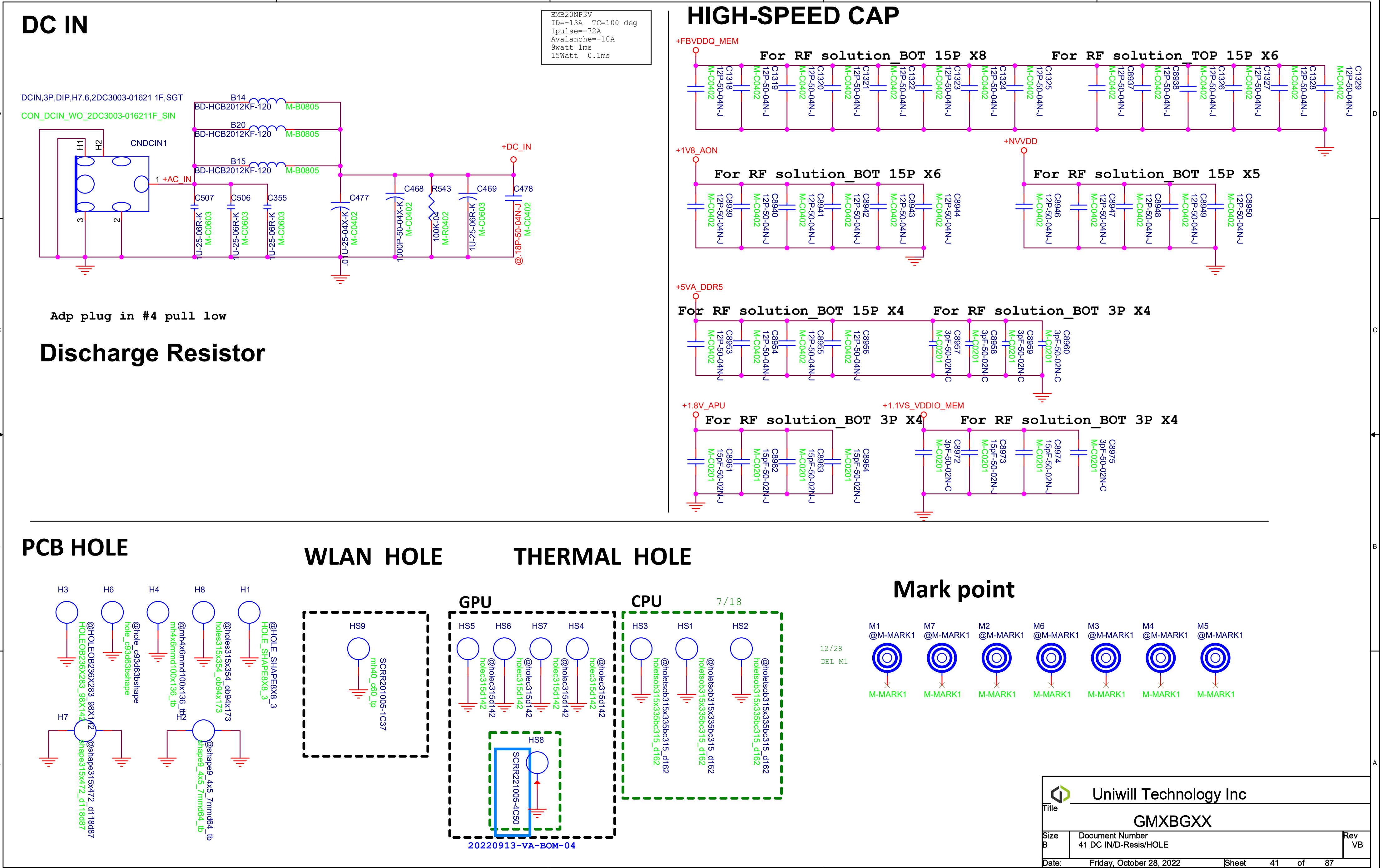


RCH4 //RCH5 =7.5mohm

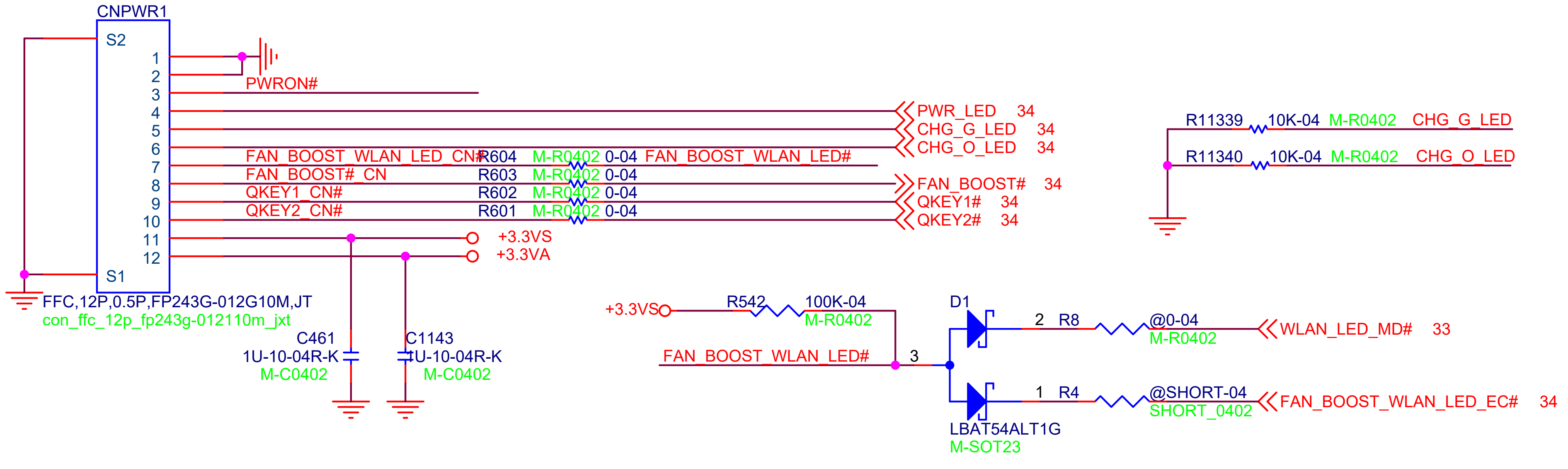
BAT_I	ICHG (0.0862V/1A)
2.3640V	8A
2.1916V	6A
2.0192V	4A
1.8468V	2A
1.7606V	1A
1.6744V	0A
1.5882V	-1A
1.5020V	-2A
1.3296V	-4A
1.1572V	-6A
0.9848V	-8A
0.8124V	-10A
0.6400V	-12A
0.4676V	-14A
0.2952V	-16A

RCH4 //RCH5 =15mohm

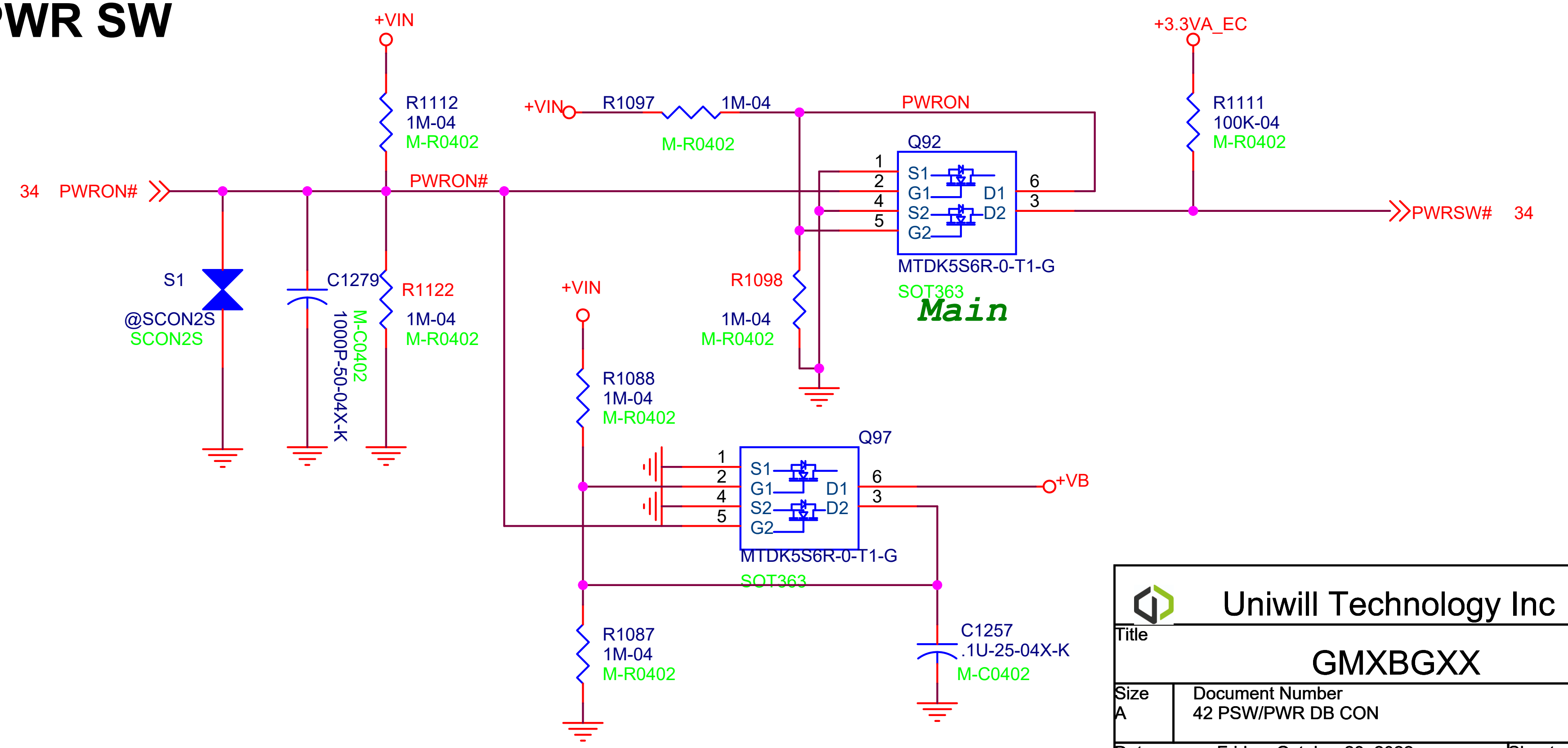
BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A


DC IN
EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms
DCIN,3P,DIP,H7.6,2DC3003-01621 1F,SGT
CON_DCIN_WO_2DC3003-016211F_SIN
CNDCIN1
H1
H2
1 +AC_IN
2
3
B14
BD-HCB2012KF-120
M-B0805
B20
BD-HCB2012KF-120
M-B0805
B15
BD-HCB2012KF-120
M-B0805
+DC_IN
C507
1U-25-06R-K
M-C0603
C506
1U-25-06R-K
M-C0603
C355
1U-25-06R-K
M-C0603
C477
.01U-25-04X-K
M-C0402
C468
1000P-50-04X-K
M-C0402
R543
100K-04
M-R0402
C469
1U-25-06R-K
M-C0603
C478
@.18P-50-04N-J
M-C0402
Adp plug in #4 pull low
Discharge Resistor
HIGH-SPEED CAP
+FBVDDQ_MEM
For RF solution_BOT 15P X8
For RF solution_TOP 15P X6
C1318
C1319
C1320
C1321
C1322
C1323
C1324
C1325
C8937
C8938
C1326
C1327
C1328
C1329
12P-50-04N-J
M-C0402
+1V8_AON
For RF solution_BOT 15P X6
C8939
C8940
C8941
C8942
C8943
C8944
12P-50-04N-J
M-C0402
+NVVDD
For RF solution_BOT 15P X5
C8946
C8947
C8948
C8949
C8950
12P-50-04N-J
M-C0402
+5VA_DDR5
For RF solution_BOT 15P X4
C8953
C8954
C8955
C8956
12P-50-04N-J
M-C0402
For RF solution_BOT 3P X4
C8957
C8958
C8959
C8960
3pF-50-02N-C
M-C0201
+1.8V_APU
For RF solution_BOT 3P X4
C8961
C8962
C8963
C8964
15pF-50-02N-J
M-C0201
+1.1VS_VDDIO_MEM
For RF solution_BOT 3P X4
C8972
3pF-50-02N-C
M-C0201
C8973
15pF-50-02N-J
M-C0201
C8974
15pF-50-02N-J
M-C0201
C8975
3pF-50-02N-C
M-C0201
PCB HOLE
H3
@HOLEOB236X283_98X142
HOLEOB236X283_98X142
H6
@hole_c93d63bshape
hole_c93d63bshape
H4
@mh4x6mmd100x136_tb
mh4x6mmd100x136_tb
H8
@holes315x354_ob94x173
holes315x354_ob94x173
H1
@HOLE_SHAPE8X8_3
HOLE_SHAPE8X8_3
H7
@shape315x472_d118d87
shape315x472_d118d87
H2
@shape9_4x5_7mmd64_tb
shape9_4x5_7mmd64_tb
WLAN HOLE
HS9
SCRR201005-1C37
mh40_c60_tp
THERMAL HOLE
GPU
HS5
HS6
HS7
HS4
@holec315d142
holec315d142
HS8
SCRR221005-4C50
20220913-VA-BOM-04
CPU
7/18
HS3
HS1
HS2
@holetsob315x335bc315_d162
holetsob315x335bc315_d162
Mark point
12/28
DEL M1
M1
M7
M2
M6
M3
M4
M5
@M-MARK1
M-MARK1
Uniwill Technology Inc
Title
GMXBGXX
Size
B
Document Number
41 DC IN/D-Resis/HOLE
Rev
VB
Date: Friday, October 28, 2022
Sheet 41 of 87

POWER DB CONN.



PWR SW



Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
A	42 PSW/PWR DB CON	VB

Date: Friday, October 28, 2022 Sheet 42 of 87

Uniwill Technology Inc

Title

GMXBGXX

Size	Document Number	Rev
C	43 Reserved	VB

Date: Friday, October 28, 2022 Sheet 43 of 87

Uniwill Technology Inc	
Title	GMXBGXX
Size: B	Document Number: 44 Reserved	Rev: VB
Date: Friday, October 28, 2022	Sheet 44 of 87

Uniwill Technology Inc

Title	GMXBGXX
Size: A	Document Number: 45 Reserved
Rev	VB
Date:	Friday, October 28, 2022
Sheet	45 of 87

5 4 3 2 1

D

C

B

A

Uniwill Technology Inc

Title

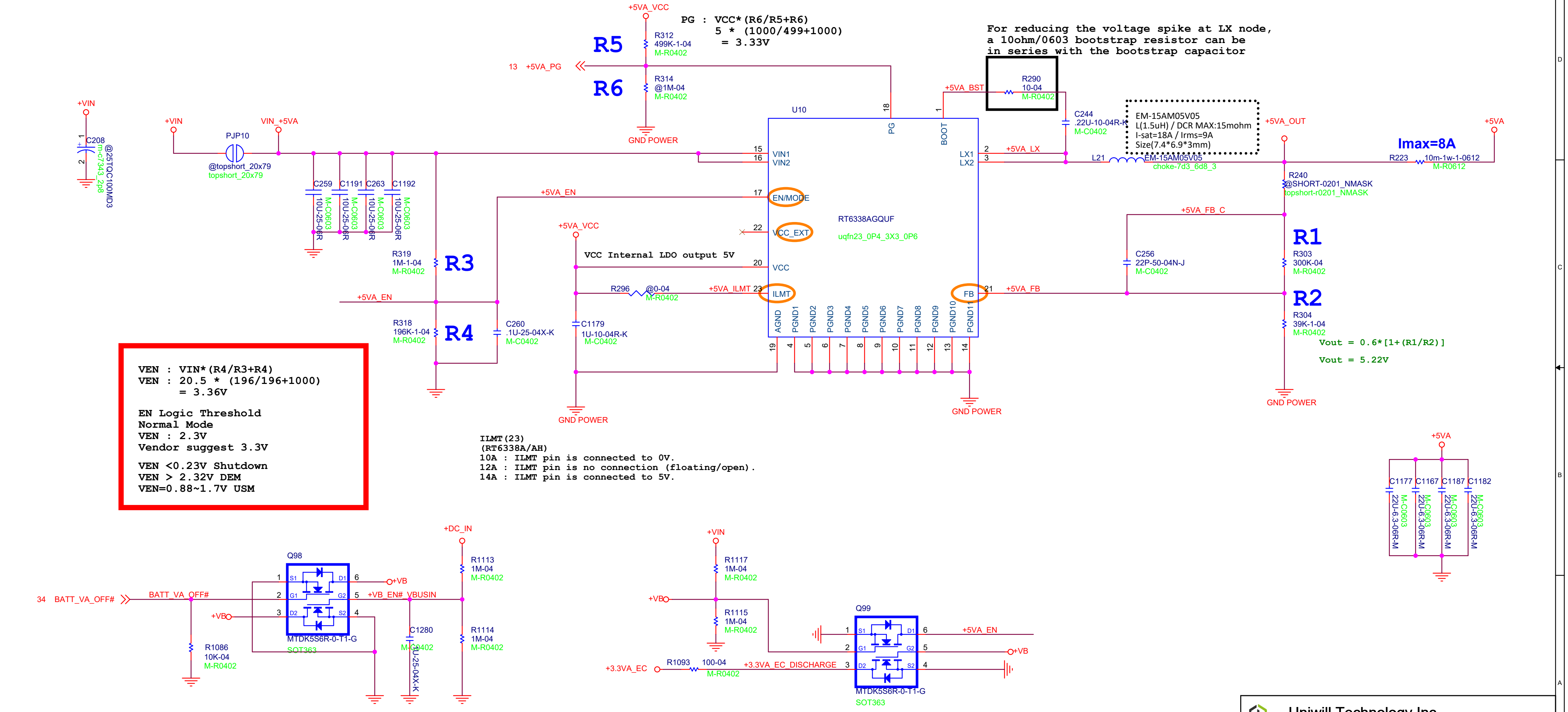
GMXBGXX

Size	Document Number	Rev
A	46 Reserved	VB

Date: Friday, October 28, 2022 Sheet 46 of 87

5 4 3 2 1

+5VA

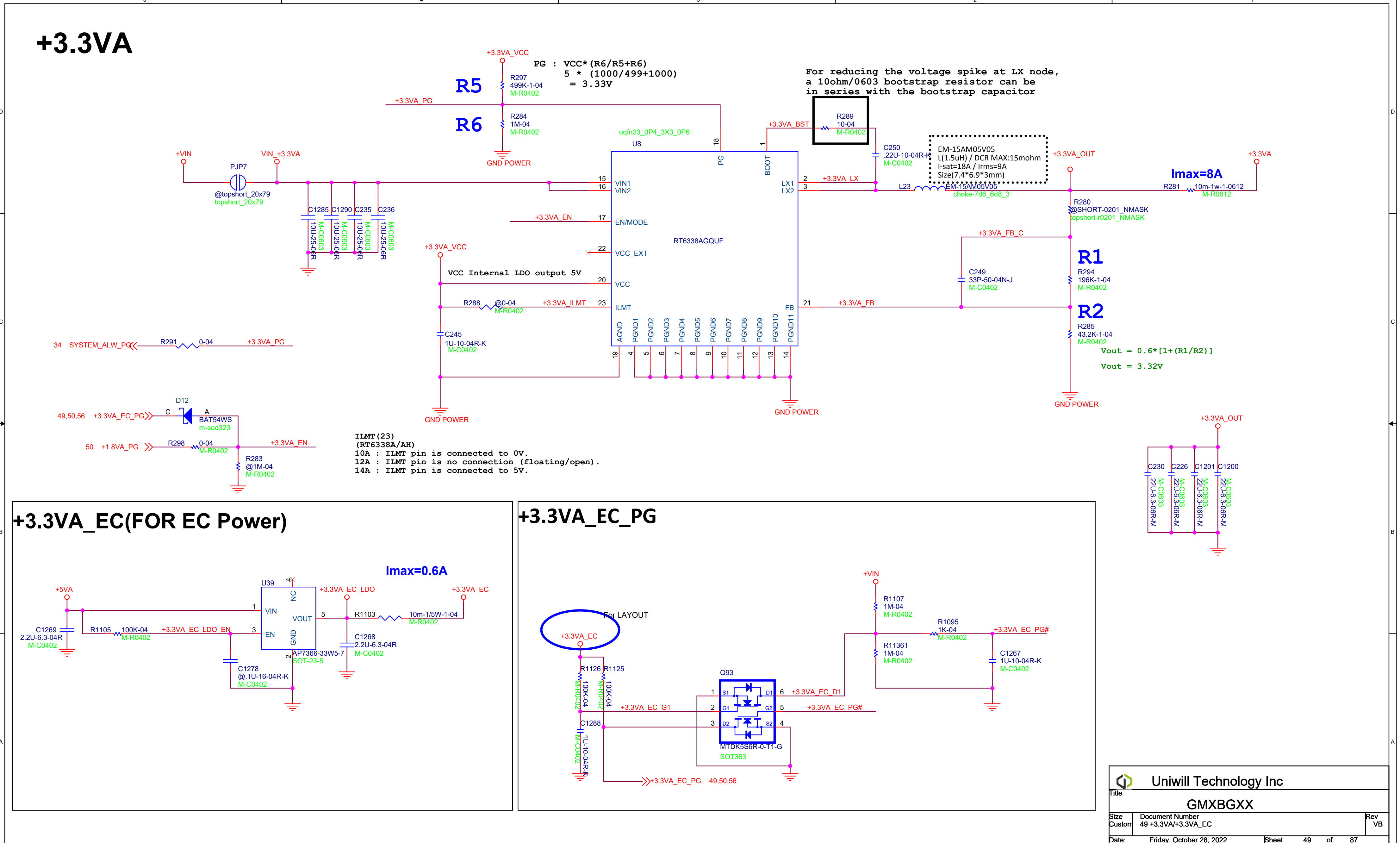


Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	48 +5VA	VB

Date: Friday, October 28, 2022 — Sheet 48 of 87



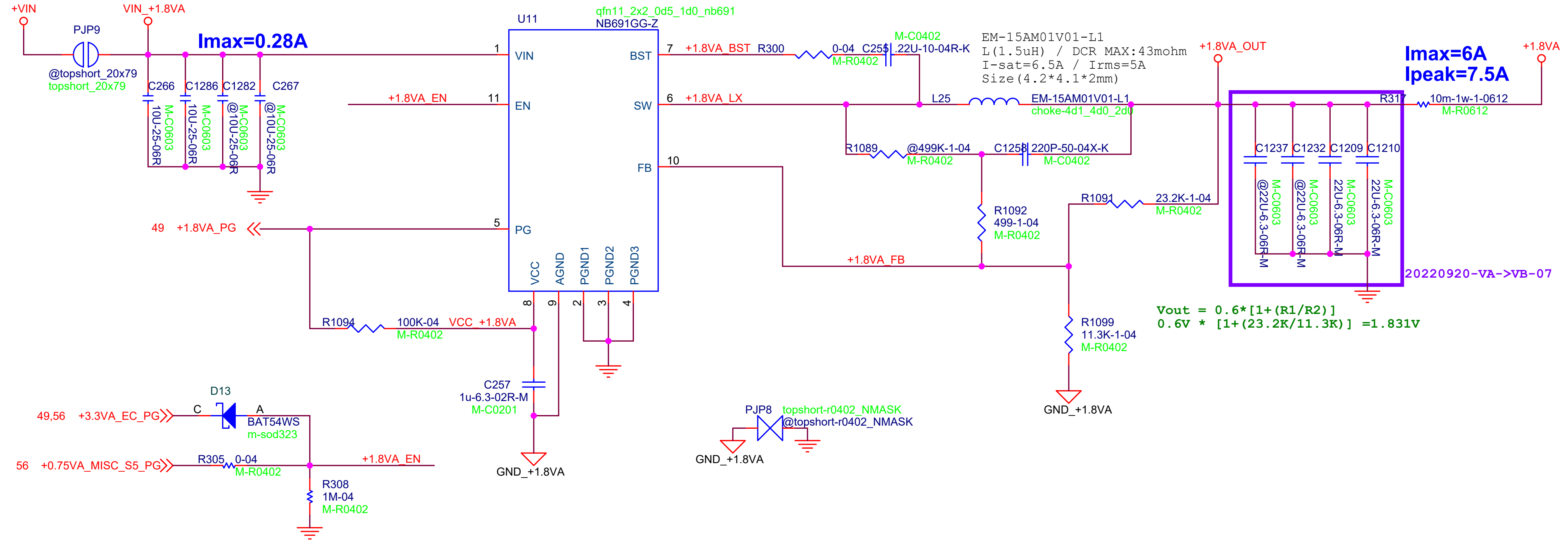
Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	49 +3.3VA/+3.3VA_EC	VB

Date: Friday, October 28, 2022 Sheet 49 of 87

+1.8VA

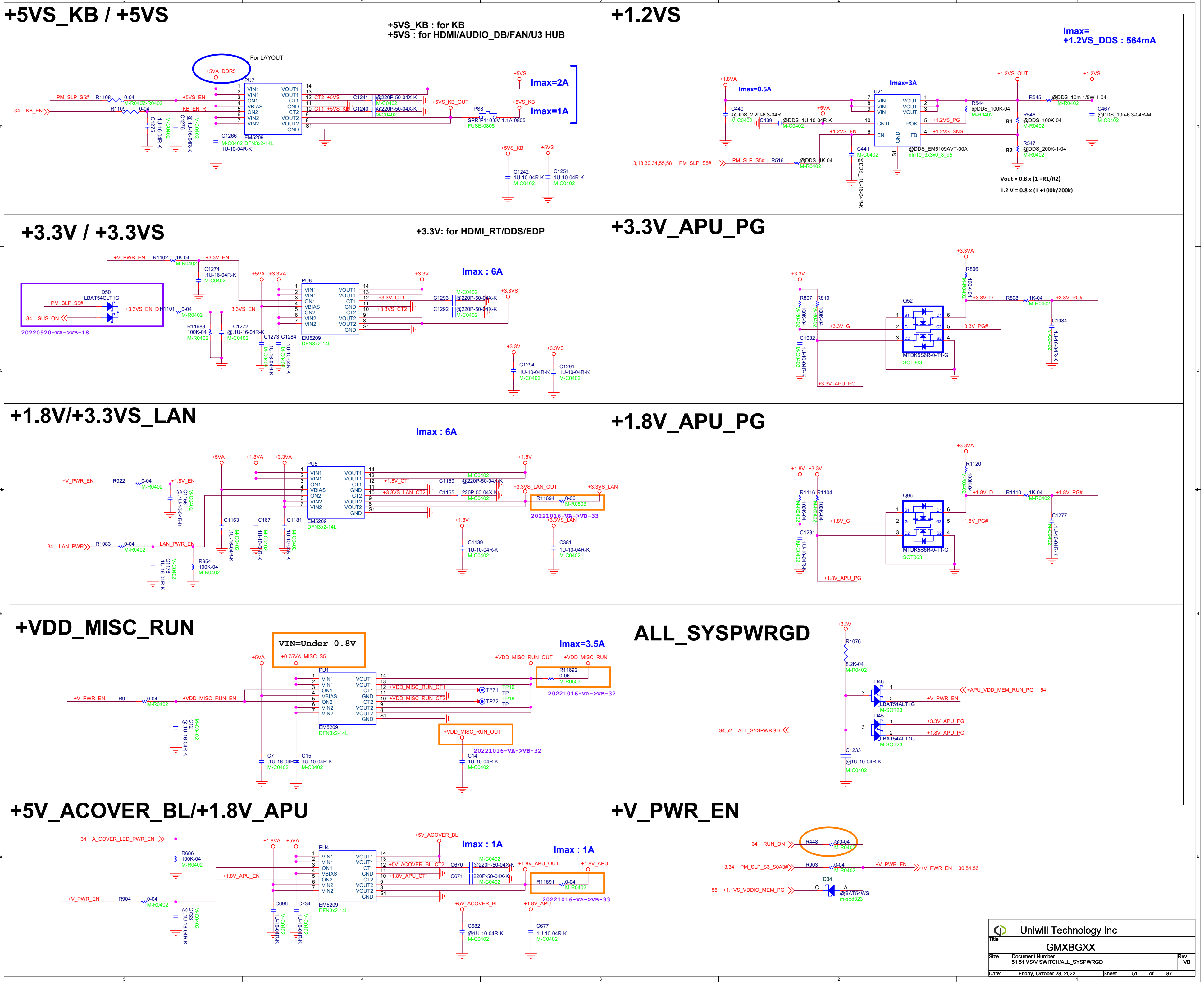


Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	50 +1.8VA	VB

Date: Friday, October 28, 2022 | Sheet 50 of 87

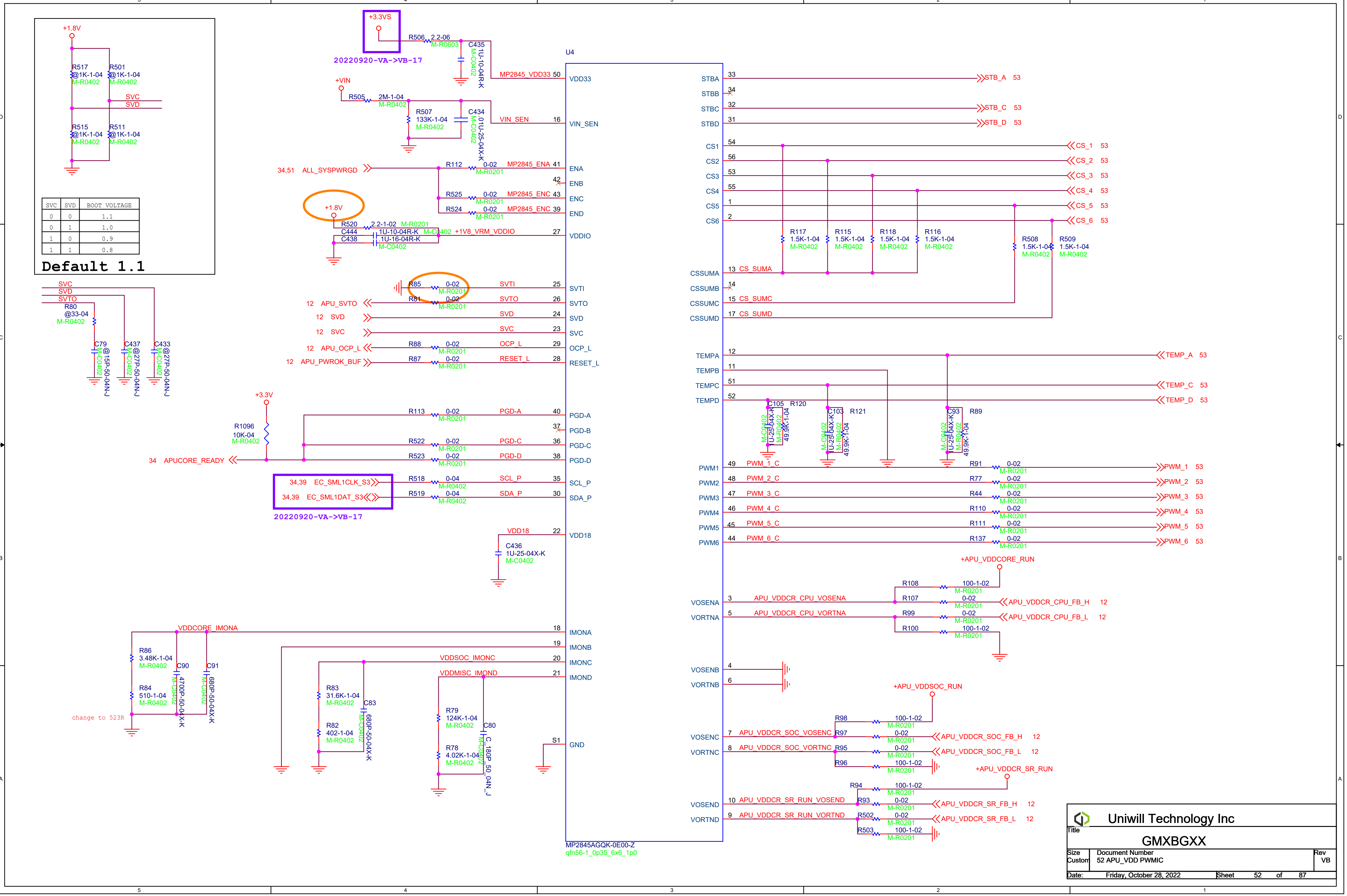


Uniwill Technology Inc

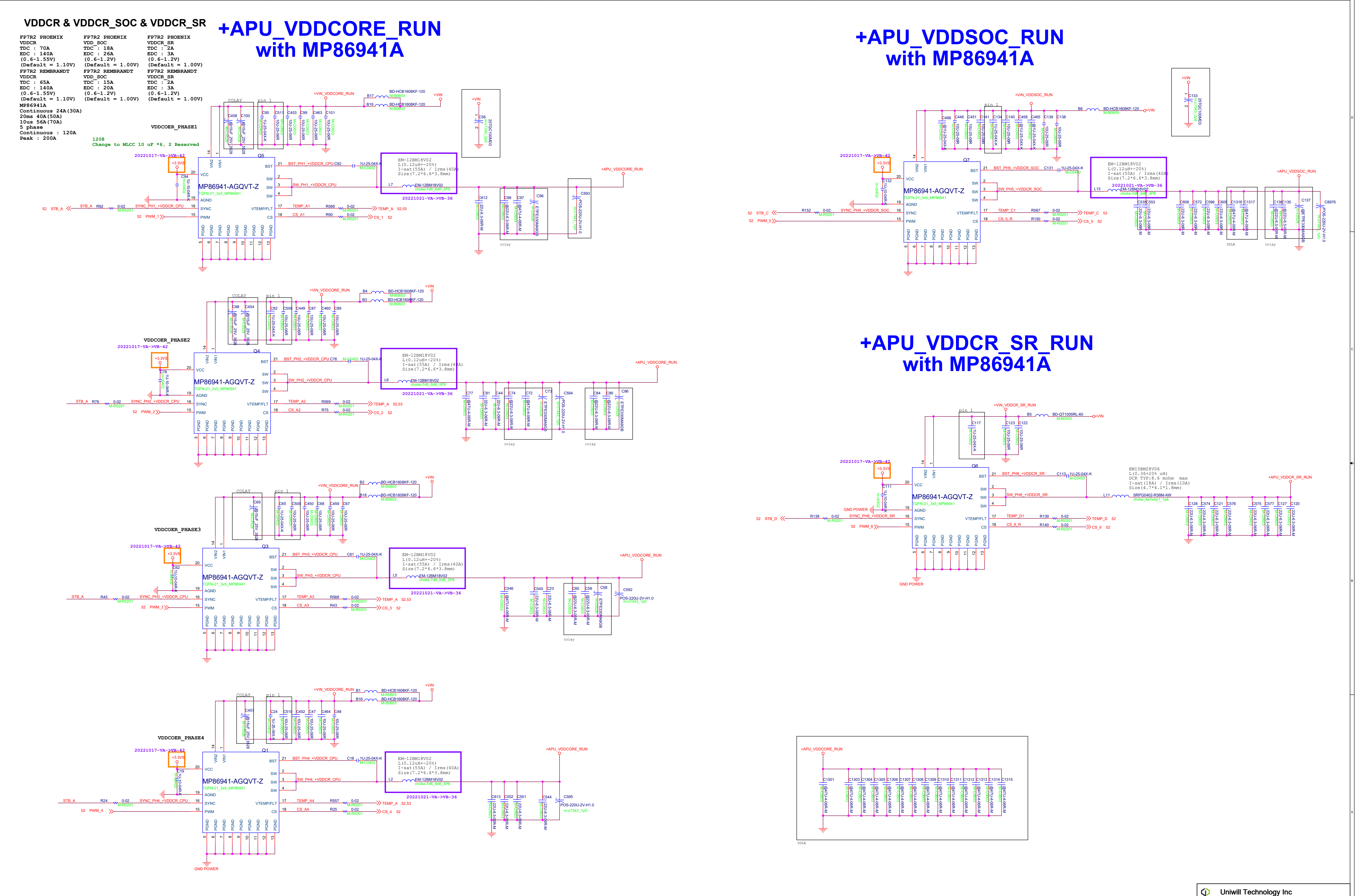
Title: GMXBGXX

Size	Document Number	Rev
	51 51 VS/V SWITCH/ALL_SYSPWRGD	VB

Date: Friday, October 28, 2022 Sheet 51 of 87



+1.8V
R517 @1K-1-04 M-R0402
R501 @1K-1-04 M-R0402
SVC
SVD
R515 @1K-1-04 M-R0402
R511 @1K-1-04 M-R0402
SVC SVD BOOT VOLTAGE
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
Default 1.1
+3.3VS
R506 2.2-06 M-R0603
C435 1U-10-04R-K M-C0402
20220920-VA->VB-17
MP2845_VDD33
+VIN
R505 2M-1-04 M-R0402
R507 133K-1-04 M-R0402
C434 .01U-25-04X-K M-C0402
VIN_SEN
34,51 ALL_SYSPWRGD
R112 0-02 M-R0201 MP2845_ENA
R525 0-02 M-R0201 MP2845_ENC
R524 0-02 M-R0201 MP2845_END
+1.8V
R520 2.2-1-02 M-R0201
C444 1U-10-04R-K M-C0402
C438 1U-16-04R-K M-C0402
+1V8_VRM_VDDIO
SVC
SVD
SVTO
R80 @33-04 M-R0402
C79 @15P-50-04N-J M-C0402
C437 @27P-50-04N-J M-C0402
C433 @27P-50-04N-J M-C0402
R85 0-02 M-R0201 SVTI
12 APU_SVTO R84 0-02 M-R0201 SVTO
12 SVD
12 SVC
12 APU_OCP_L R88 0-02 M-R0201 OCP_L
12 APU_PWROK_BUF R87 0-02 M-R0201 RESET_L
+3.3V
R1096 10K-04 M-R0402
R113 0-02 M-R0201 PGD-A
R522 0-02 M-R0201 PGD-C
R523 0-02 M-R0201 PGD-D
34 APUCORE_READY
34,39 EC_SML1CLK_S3 R518 0-04 M-R0402 SCL_P
34,39 EC_SML1DAT_S3 R519 0-04 M-R0402 SDA_P
20220920-VA->VB-17
VDD18
C436 1U-25-04X-K M-C0402
VDDCORE_IMONA
R86 3.48K-1-04 M-R0402
R84 510-1-04 M-R0402
C90 4700P-50-04X-K M-C0402
C91 680P-50-04X-K M-C0402
change to 523R
VDDSOC_IMONC
R83 31.6K-1-04 M-R0402
R82 402-1-04 M-R0402
C83 680P-50-04X-K M-C0402
VDDMISC_IMOND
R79 124K-1-04 M-R0402
R78 4.02K-1-04 M-R0402
C80 180P-50-04N-J M-C0402
U4
VDD33 50
VIN_SEN 16
ENA 41
ENB 42
ENC 43
END 39
VDDIO 27
SVTI 25
SVTO 26
SVD 24
SVC 23
OCP_L 29
RESET_L 28
PGD-A 40
PGD-B 37
PGD-C 36
PGD-D 38
SCL_P 35
SDA_P 30
VDD18 22
IMONA 18
IMONB 19
IMONC 20
IMOND 21
GND S1
STBA 33
STBB 34
STBC 32
STBD 31
CS1 54
CS2 56
CS3 53
CS4 55
CS5 1
CS6 2
CSSUMA 13
CSSUMB 14
CSSUMC 15
CSSUMD 17
TEMPA 12
TEMPB 11
TEMPC 51
TEMPD 52
PWM1 49
PWM2 48
PWM3 47
PWM4 46
PWM5 45
PWM6 44
VOSENA 3
VORTNA 5
VOSENB 4
VORTNB 6
VOSENC 7
VORTNC 8
VOSEND 10
VORTND 9
MP2845AGQK-0E00-Z
qfn56-1_0p35_6x6_1p0
STB_A 53
STB_C 53
STB_D 53
CS_1 53
CS_2 53
CS_3 53
CS_4 53
CS_5 53
CS_6 53
R117 1.5K-1-04 M-R0402
R115 1.5K-1-04 M-R0402
R118 1.5K-1-04 M-R0402
R116 1.5K-1-04 M-R0402
R508 1.5K-1-04 M-R0402
R509 1.5K-1-04 M-R0402
CS_SUMA
CS_SUMC
CS_SUMD
TEMP_A 53
TEMP_C 53
TEMP_D 53
C105 1U-25-04X-K M-C0402
R120 49.9K-1-04 M-R0402
C103 1U-25-04X-K M-C0402
R121 49.9K-1-04 M-R0402
C93 1U-25-04X-K M-C0402
R89 49.9K-1-04 M-R0402
PWM_1_C R91 0-02 M-R0201 PWM_1 53
PWM_2_C R77 0-02 M-R0201 PWM_2 53
PWM_3_C R44 0-02 M-R0201 PWM_3 53
PWM_4_C R110 0-02 M-R0201 PWM_4 53
PWM_5_C R111 0-02 M-R0201 PWM_5 53
PWM_6_C R137 0-02 M-R0201 PWM_6 53
+APU_VDDCORE_RUN
R108 100-1-02 M-R0201
APU_VDDCR_CPU_VOSENA R107 0-02 M-R0201 APU_VDDCR_CPU_FB_H 12
APU_VDDCR_CPU_VORTNA R99 0-02 M-R0201 APU_VDDCR_CPU_FB_L 12
R100 100-1-02 M-R0201
+APU_VDDSOC_RUN
R98 100-1-02 M-R0201
APU_VDDCR_SOC_VOSENC R97 0-02 M-R0201 APU_VDDCR_SOC_FB_H 12
APU_VDDCR_SOC_VORTNC R95 0-02 M-R0201 APU_VDDCR_SOC_FB_L 12
R96 100-1-02 M-R0201
+APU_VDDCR_SR_RUN
R94 100-1-02 M-R0201
APU_VDDCR_SR_RUN_VOSEND R93 0-02 M-R0201 APU_VDDCR_SR_FB_H 12
APU_VDDCR_SR_RUN_VORTND R502 0-02 M-R0201 APU_VDDCR_SR_FB_L 12
R503 100-1-02 M-R0201
Uniwill Technology Inc
Title
GMXBGXX
Size Custom
Document Number 52 APU_VDD PWMIC
Rev VB
Date: Friday, October 28, 2022
Sheet 52 of 87



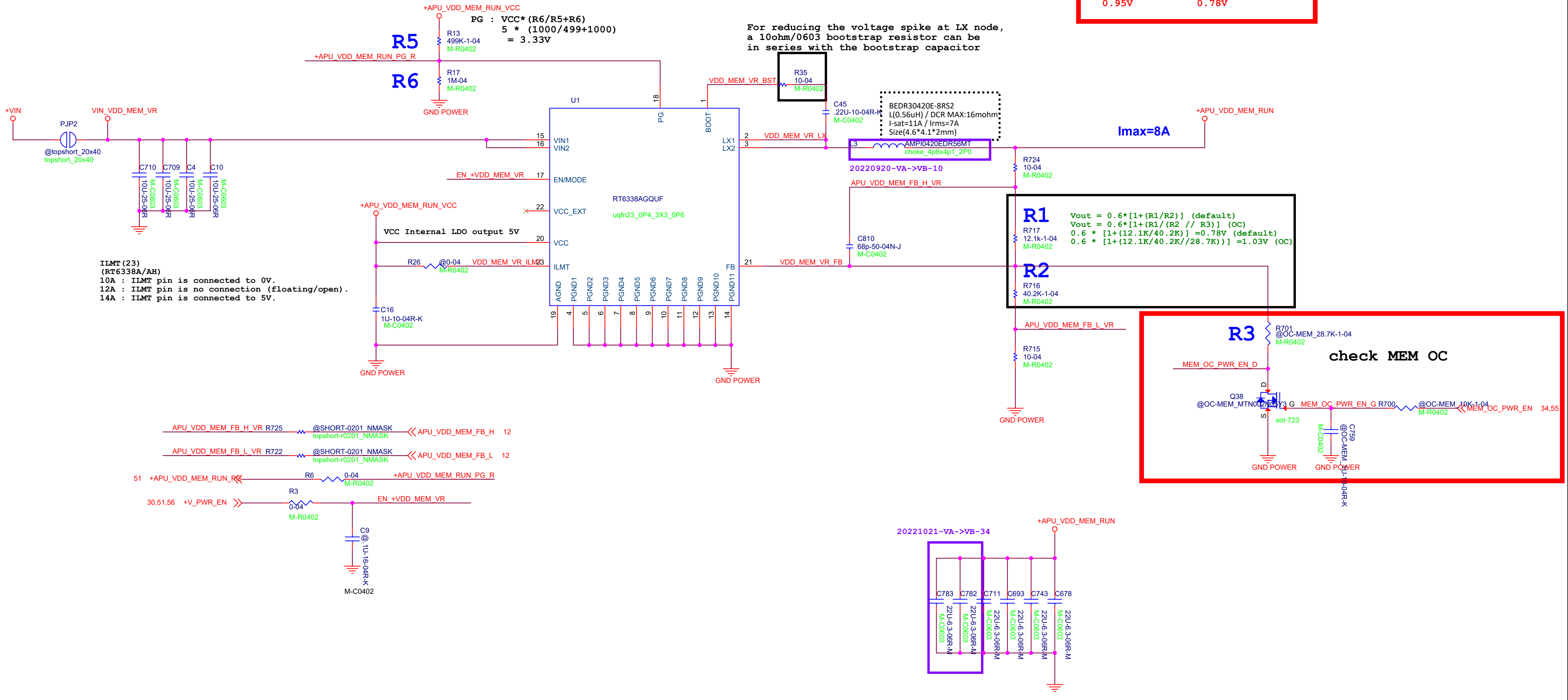
VDDCR & VDDCR_SOC & VDDCR_SR
FP7R2 PHOENIX VDDCR TDC : 70A EDC : 140A (0.6-1.55V) (Default = 1.10V)
FP7R2 PHOENIX VDD_SOC TDC : 18A EDC : 26A (0.6-1.2V) (Default = 1.00V)
FP7R2 PHOENIX VDDCR_SR TDC : 2A EDC : 3A (0.6-1.2V) (Default = 1.00V)
FP7R2 REMBRANDT VDDCR TDC : 65A EDC : 140A (0.6-1.55V) (Default = 1.10V)
FP7R2 REMBRANDT VDD_SOC TDC : 15A EDC : 20A (0.6-1.2V) (Default = 1.00V)
FP7R2 REMBRANDT VDDCR_SR TDC : 2A EDC : 3A (0.6-1.2V) (Default = 1.00V)
MP86941A
Continuous 24A(30A)
20ms 40A(50A)
10us 56A(70A)
5 phase
Continuous : 120A
Peak : 200A
1208
Change to MLCC 10 uF *6, 2 Reserved
+APU_VDDCORE_RUN
with MP86941A
+APU_VDDSOC_RUN
with MP86941A
+APU_VDDCR_SR_RUN
with MP86941A
VDDCOER_PHASE1
VDDCOER_PHASE2
VDDCOER_PHASE3
VDDCOER_PHASE4
MP86941-AGQVT-Z
TQFN-21_3x5_MP86941
EM-12BM18V02
L(0.12uH+-20%)
I-sat(55A) / Irms(40A)
Size(7.2*6.6*3.8mm)
EM15BM28V06
L(0.36+20% uH)
DCR TYP:8.6 mohm max
I-sat(18A) / Irms(10A)
Size(4.7*4.1*1.8mm)
SRPG0402-R36M-AW
20221017-VA->VB-42
20221021-VA->VB-36
+VIN_VDDCORE_RUN
+VIN_VDDSOC_RUN
+VIN_VDDCR_SR_RUN
+APU_VDDCORE_RUN
+APU_VDDSOC_RUN
+APU_VDDCR_SR_RUN
+VIN
+3.3VS
GND POWER
STB_A
STB_C
STB_D
PWM_1
PWM_2
PWM_3
PWM_4
PWM_5
PWM_6
TEMP_A
TEMP_C
TEMP_D
CS_1
CS_2
CS_3
CS_4
CS_5
CS_6
BD-HCB1608KF-120
BD-QT1005RL-60
POS-220U-2V-H1.0

VDD_MEM(MUST CHECK APU)

+APU_VDD_MEM_RUN

REMBRANDT & PHOENIX boot voltage difference

FP7R2 PHOENIX	FP7R2 REMBRANDT
VDD_MEM	VDD_MEM
TDC : 8A	TDC : 4A
0.95V	0.78V



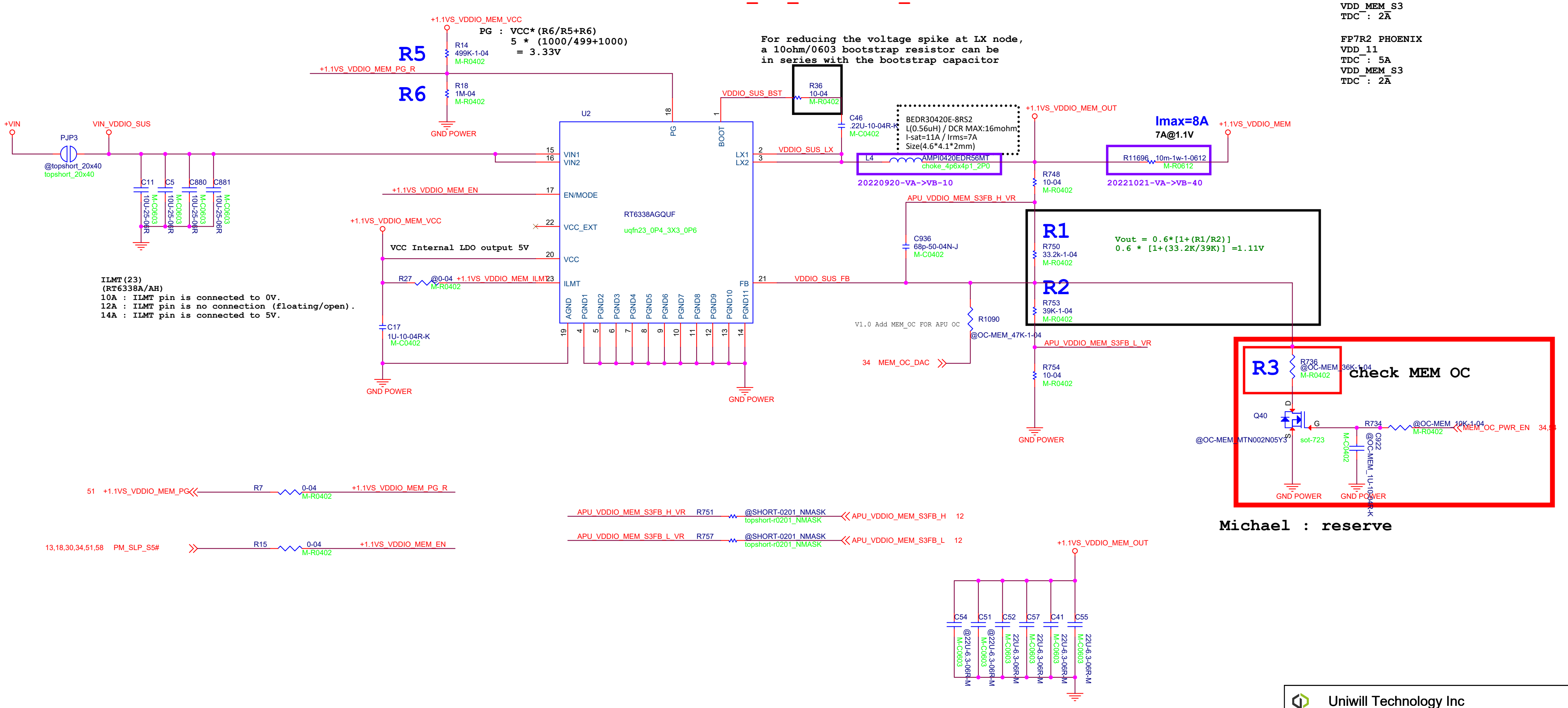
VDDIO_MEM_S3 & VDD_11

+APU_VDDIO_SUS

VDDIO_MEM_S3 and VDD_11 can be combined on the board.

FP7R2 REMBRANDT
VDD_11
TDC : 5A
VDD_MEM_S3
TDC : 2A

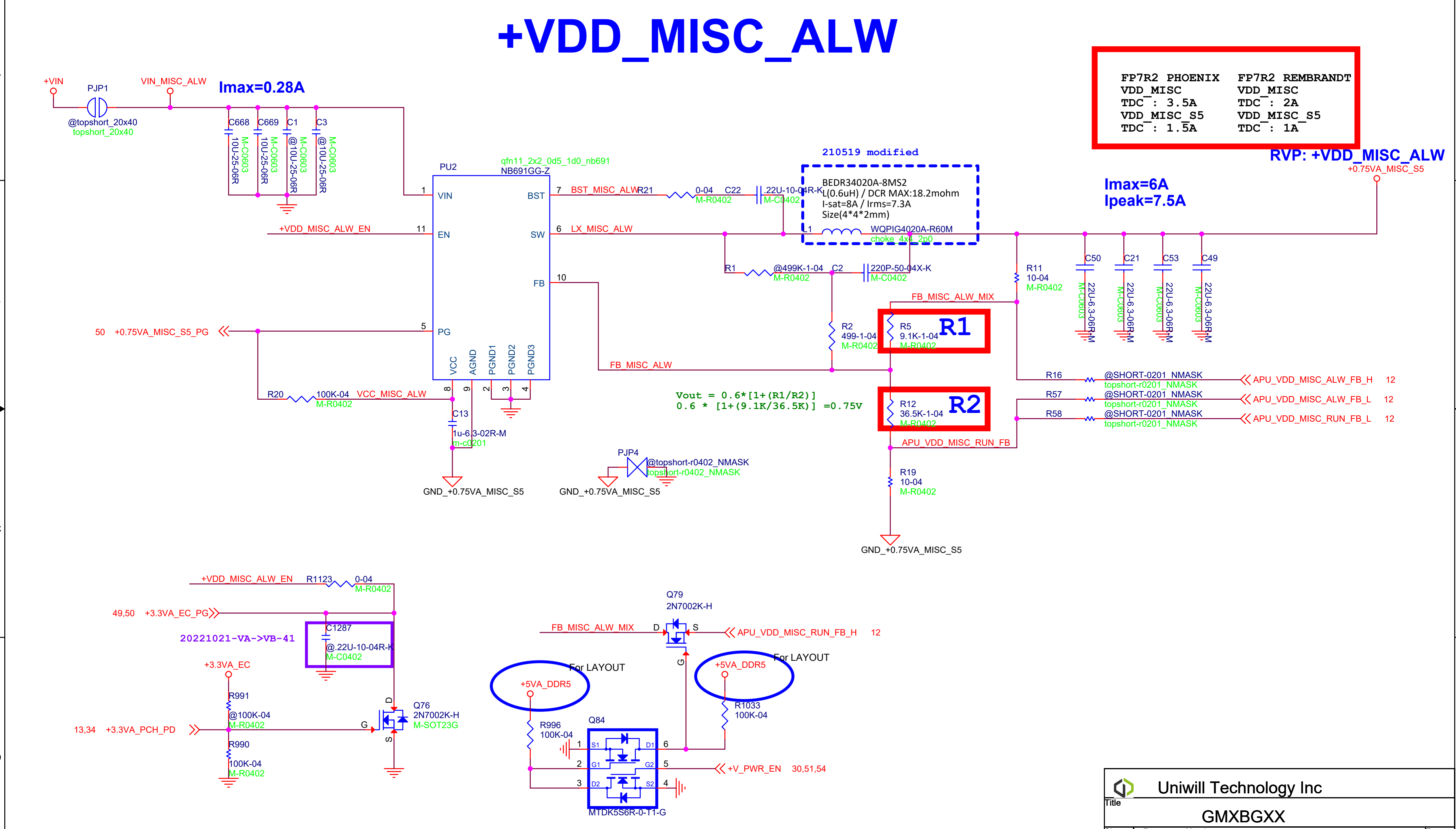
FP7R2 PHOENIX
VDD_11
TDC : 5A
VDD_MEM_S3
TDC : 2A



Uniwill Technology Inc

Title	GMXBGXX	
Size Custom	Document Number 55 APU_VDD_MISC_S5	Rev VB
Date: Friday, October 28, 2022	Sheet 55 of 87	

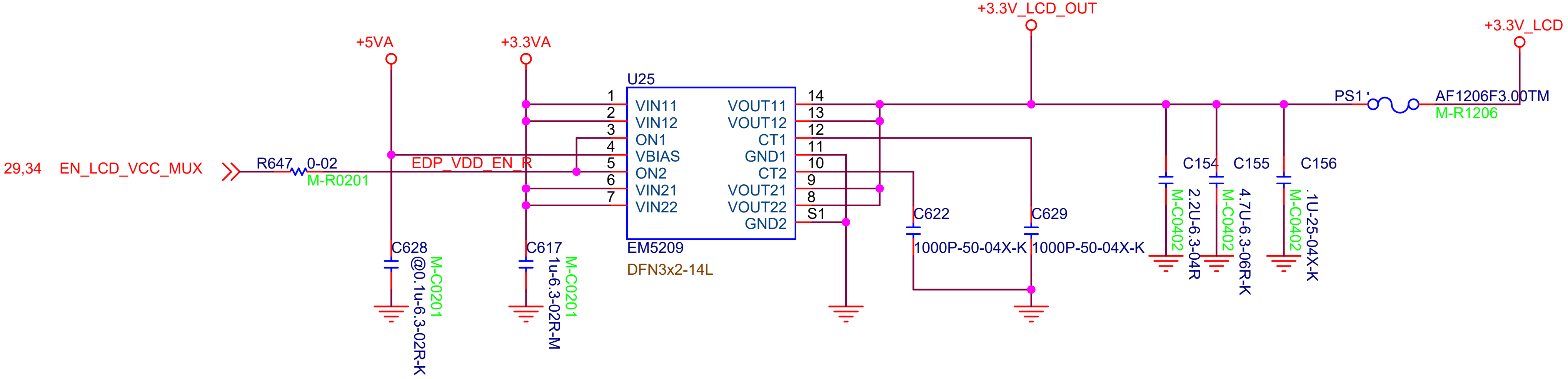
VDD_MISC & VDD_MISC_S5



Uniwill Technology Inc

Title	GMXBGXX	
Size B	Document Number: 56 APU_VDDIO_MEM_S3	Rev VB
Date: Friday, October 28, 2022	Sheet 56 of 87	

+3.6V_LCD Converter



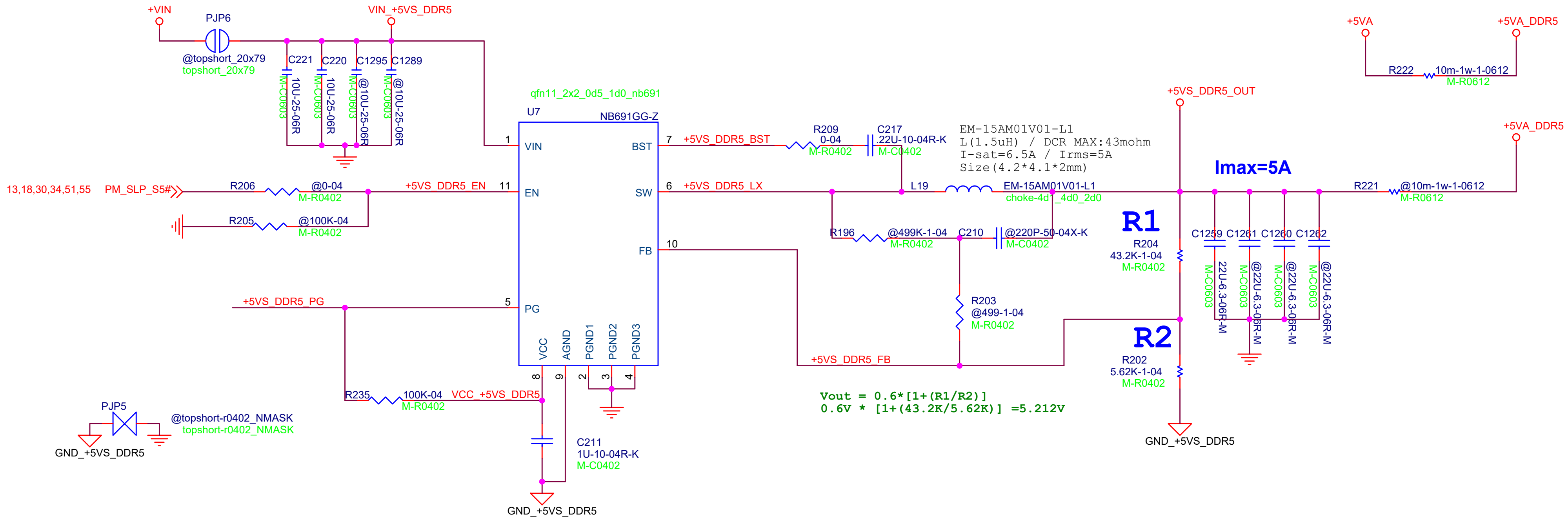
Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
A	57 +3.3V_LCD	VB

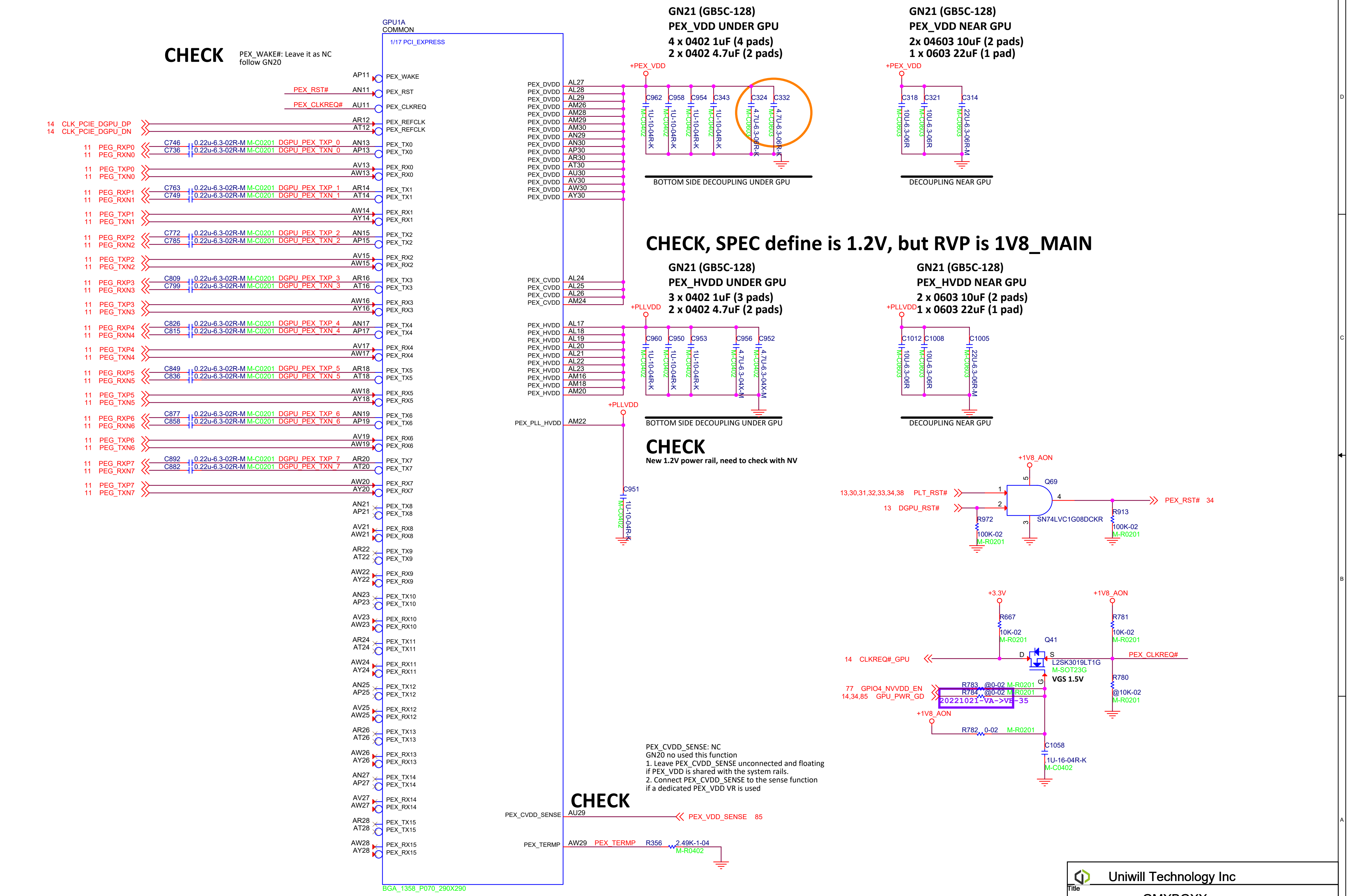
Date: Friday, October 28, 2022 Sheet 57 of 87

+5VS_DDR5 Converter (reserved)



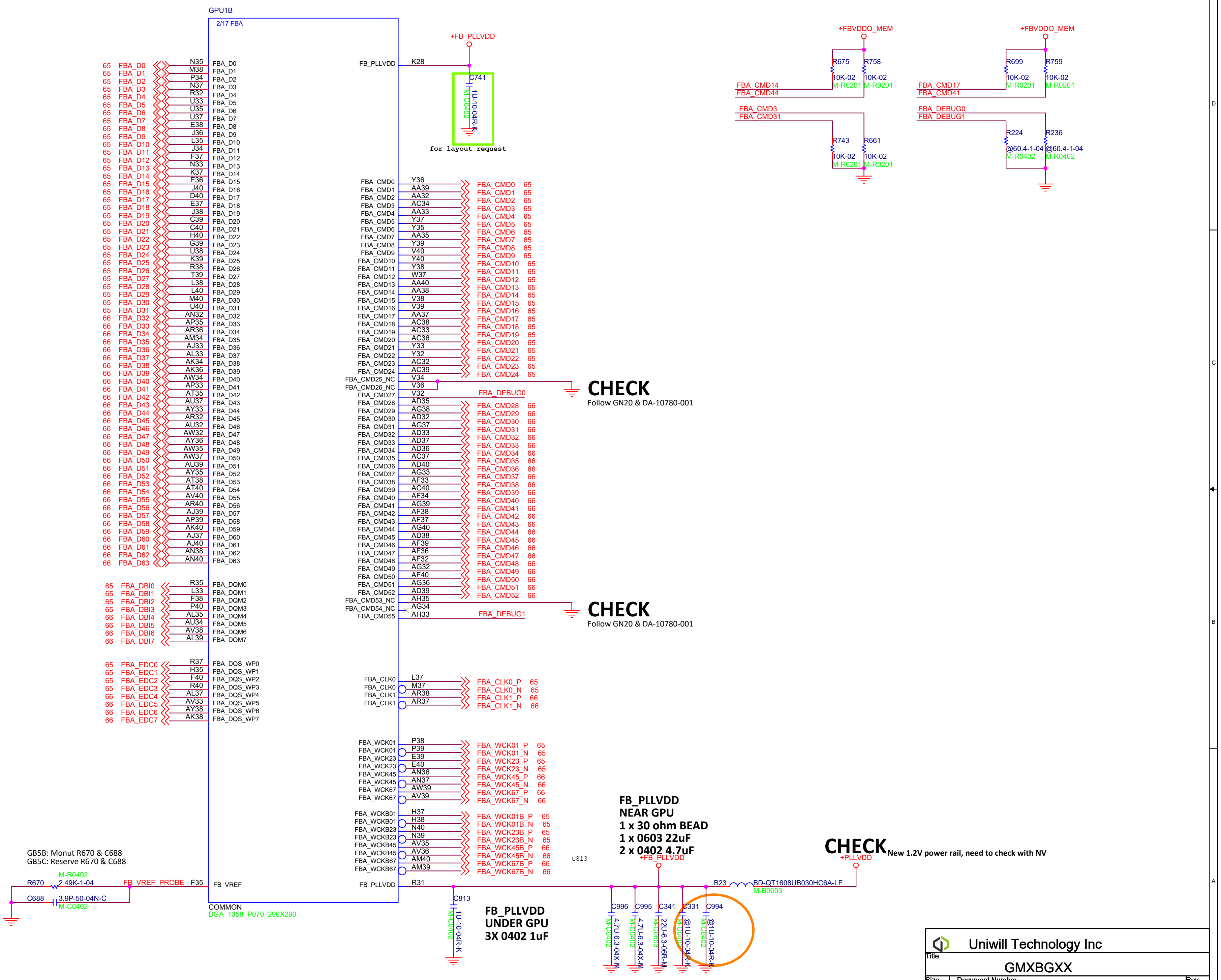
Uniwill Technology Inc			
Title	GMXBGXX		
Size: Custom	Document Number: 58 +5VS_DDR5		Rev: VB
Date: Friday, October 28, 2022	Sheet 58 of 87		

Uniwill Technology Inc		
Title: GMXBGXX		
Size: C	Document Number: 59 Reserved	Rev: VB
Date: Friday, October 28, 2022	Sheet 59 of 87	



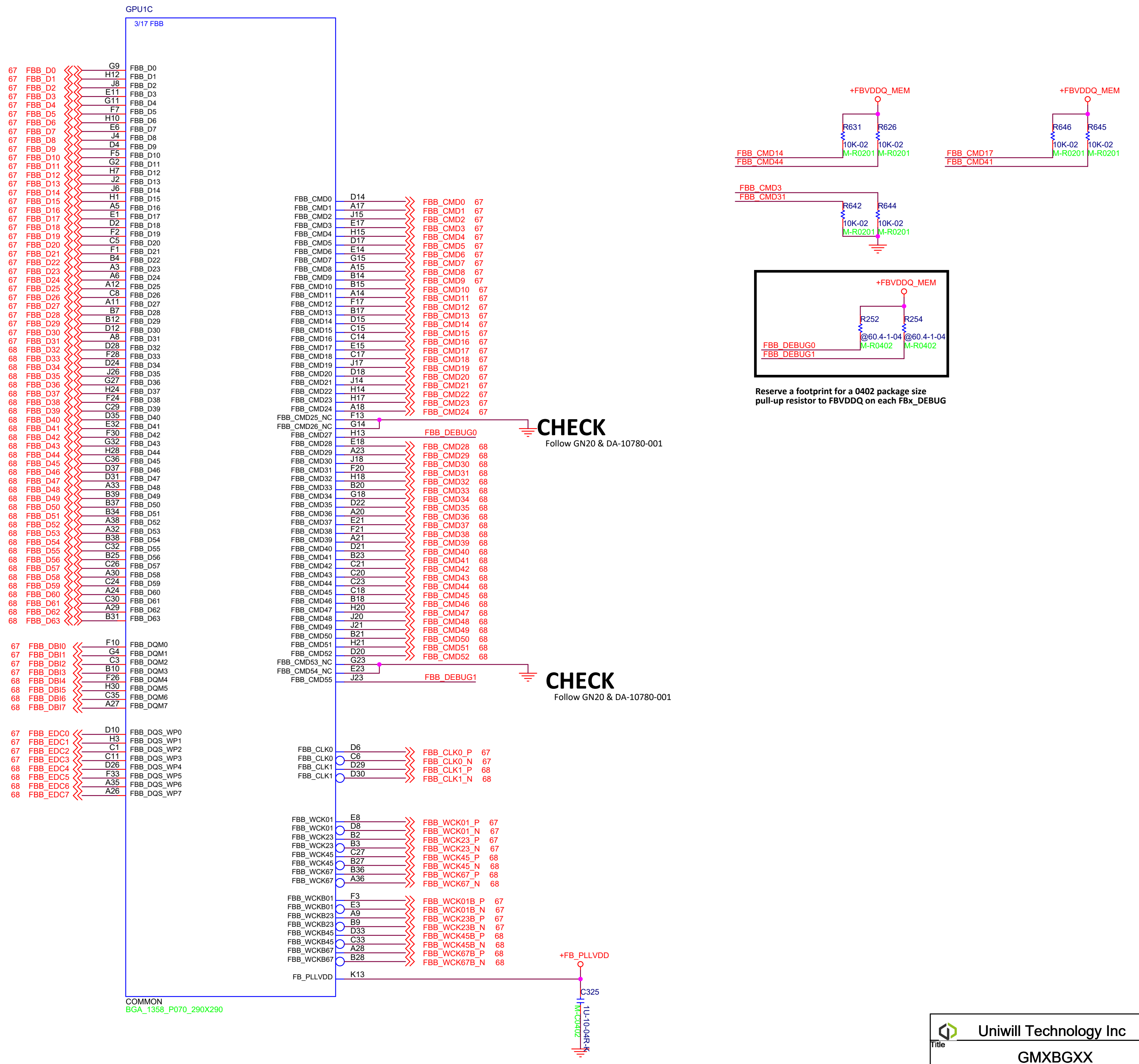
Uniwill Technology Inc

Title	GMXBGXX	
Size: Custom	Document Number: 60 GPU GN21 GFX-PCIE	Rev: VB
Date: Friday, October 28, 2022	Sheet 60 of 87	



Uniwill Technology Inc

Title	GMXBGXX	
Size Custom	Document Number 61 GPU GN21 Frame Buffer A	Rev VB
Date: Friday, October 28, 2022	Sheet 61 of 87	



Uniwill Technology Inc

Title	GMXBGXX	
Size: Custom	Document Number: 62 GPU GN21 Frame Buffer B	Rev: VB
Date: Friday, October 28, 2022	Sheet 62 of 87	

5 4 3 2 1

D

C

B

A

Uniwill Technology Inc

Title

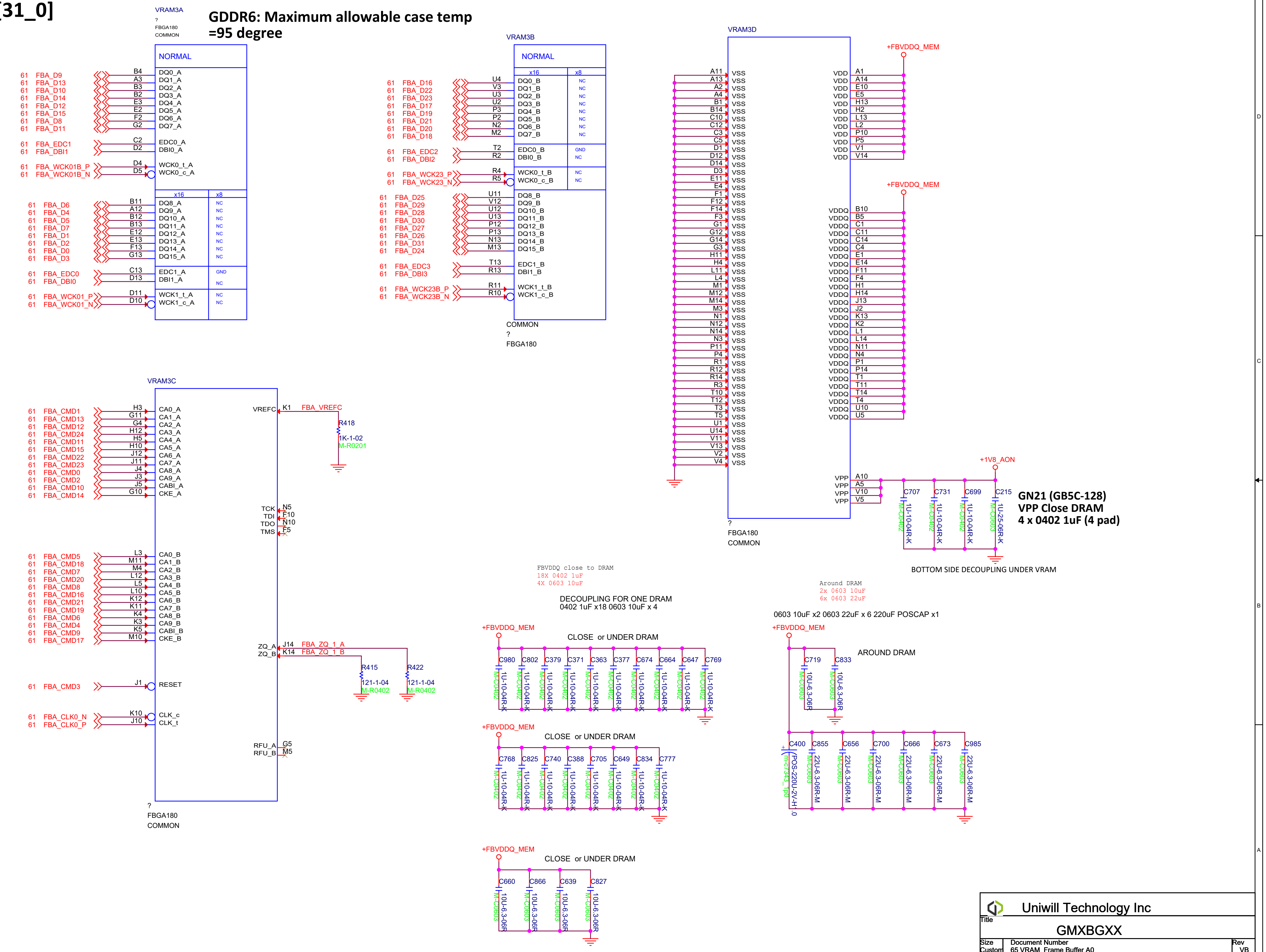
GMXBGXX

Size	Document Number	Rev
Custom	64 GPU GN21 reserved	VB

Date: Friday, October 28, 2022 Sheet 64 of 87

MEM_FBA[31_0]

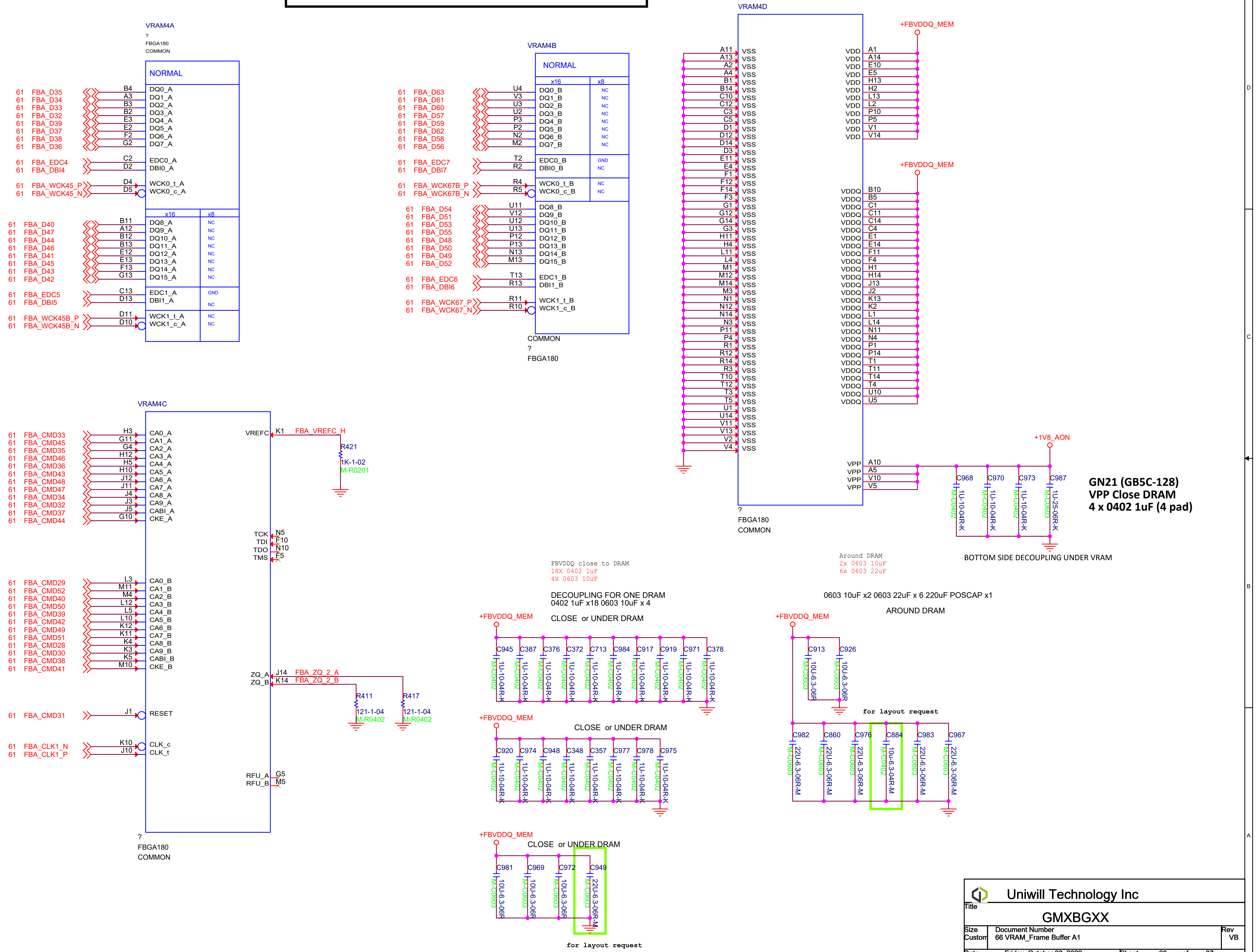
GDDR6: Maximum allowable case temp =95 degree



Uniwill Technology Inc			
Title	GMXBGXX		
Size Custom	Document Number 65 VRAM_Frame Buffer A0		Rev VB
Date:	Friday, October 28, 2022	Sheet 65 of 87	

MEM_FBA[63_32]

Maximum VRAM case Temp is 85 celcisus degree

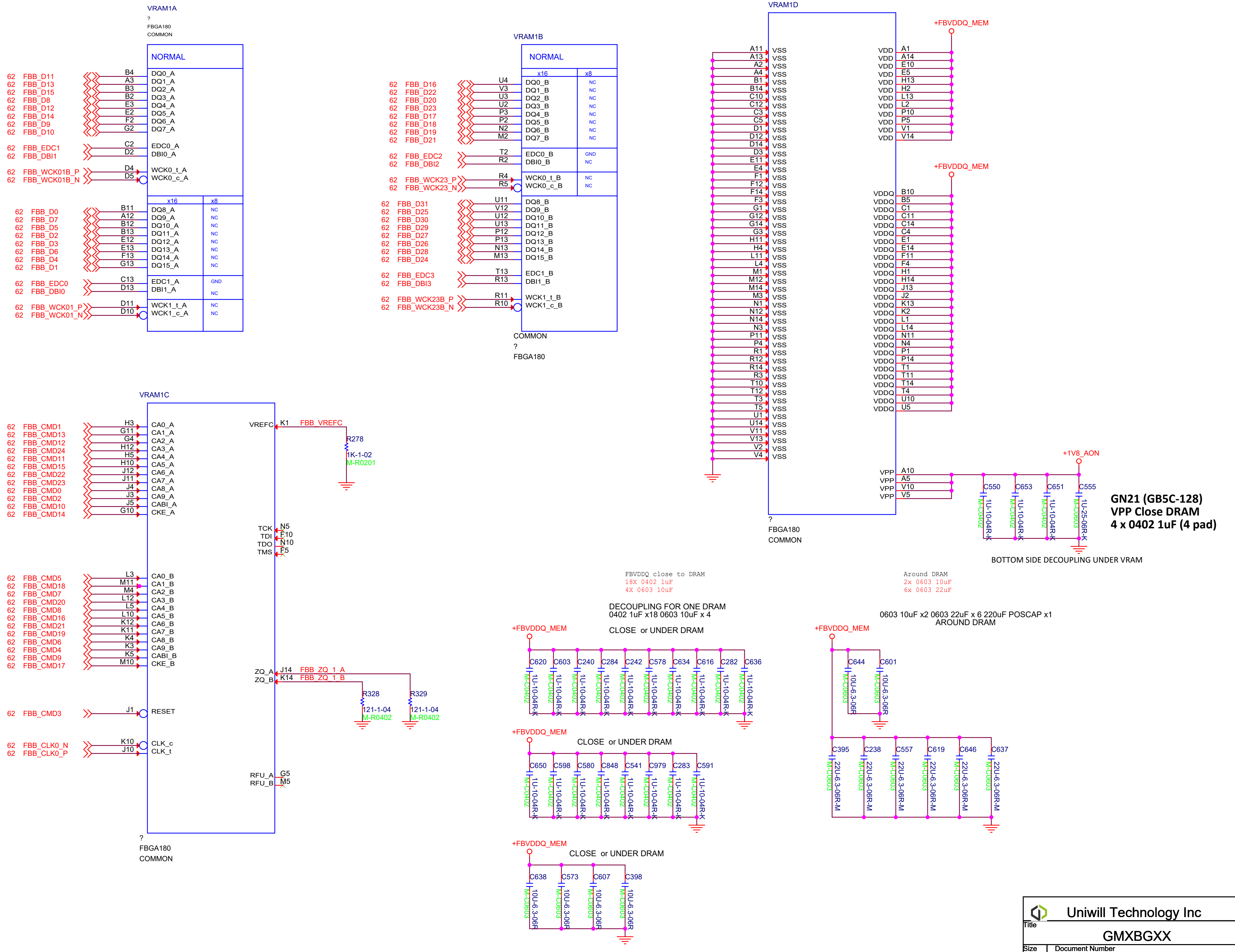


Uniwill Technology Inc

Title	GMXBGXX	
Size: Custom	Document Number: 66 VRAM_Frame Buffer A1	Rev: VB
Date: Friday, October 28, 2022	Sheet 66 of 87	

MEM_FBB[31_0]

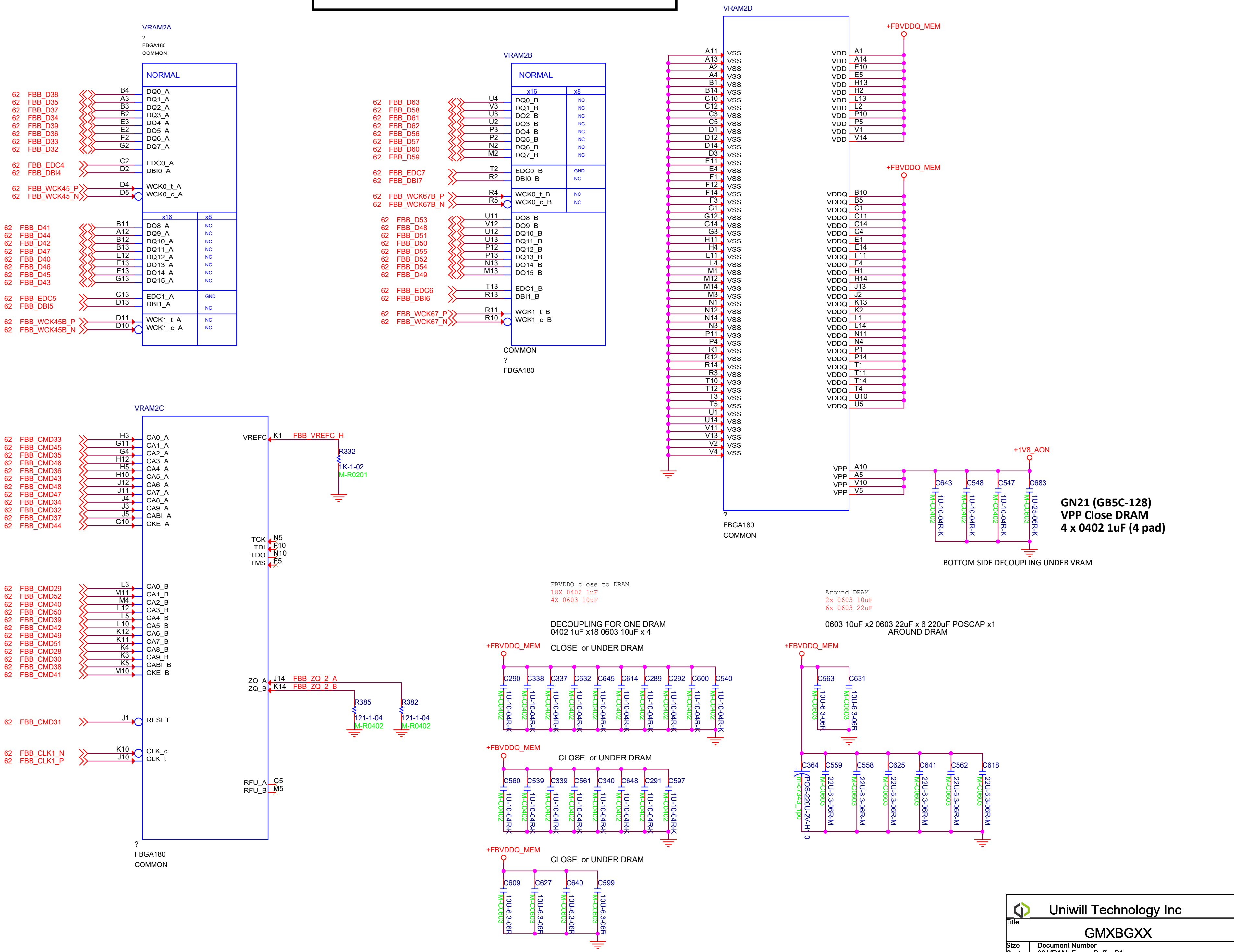
Maximum VRAM case Temp is 85 celcisus degree



Uniwill Technology Inc		
Title	GMXBGXX	
Size: Custom	Document Number: 67 VRAM_Frame Buffer B0	Rev: VB
Date: Friday, October 28, 2022	Sheet 67 of 87	

MEM_FBB[63_32]

Maximum VRAM case Temp is 85 celcisus degree



Uniwill Technology Inc

Title

GMXBGXX

Size	Document Number	Rev
C	69 VRAM reserved	VB

Date: Friday, October 28, 2022 Sheet 69 of 87

Uniwill Technology Inc

Title

GMXBGXX

Size	Document Number	Rev
C	70 VRAM reserved	VB

Date: Friday, October 28, 2022 Sheet 70 of 87

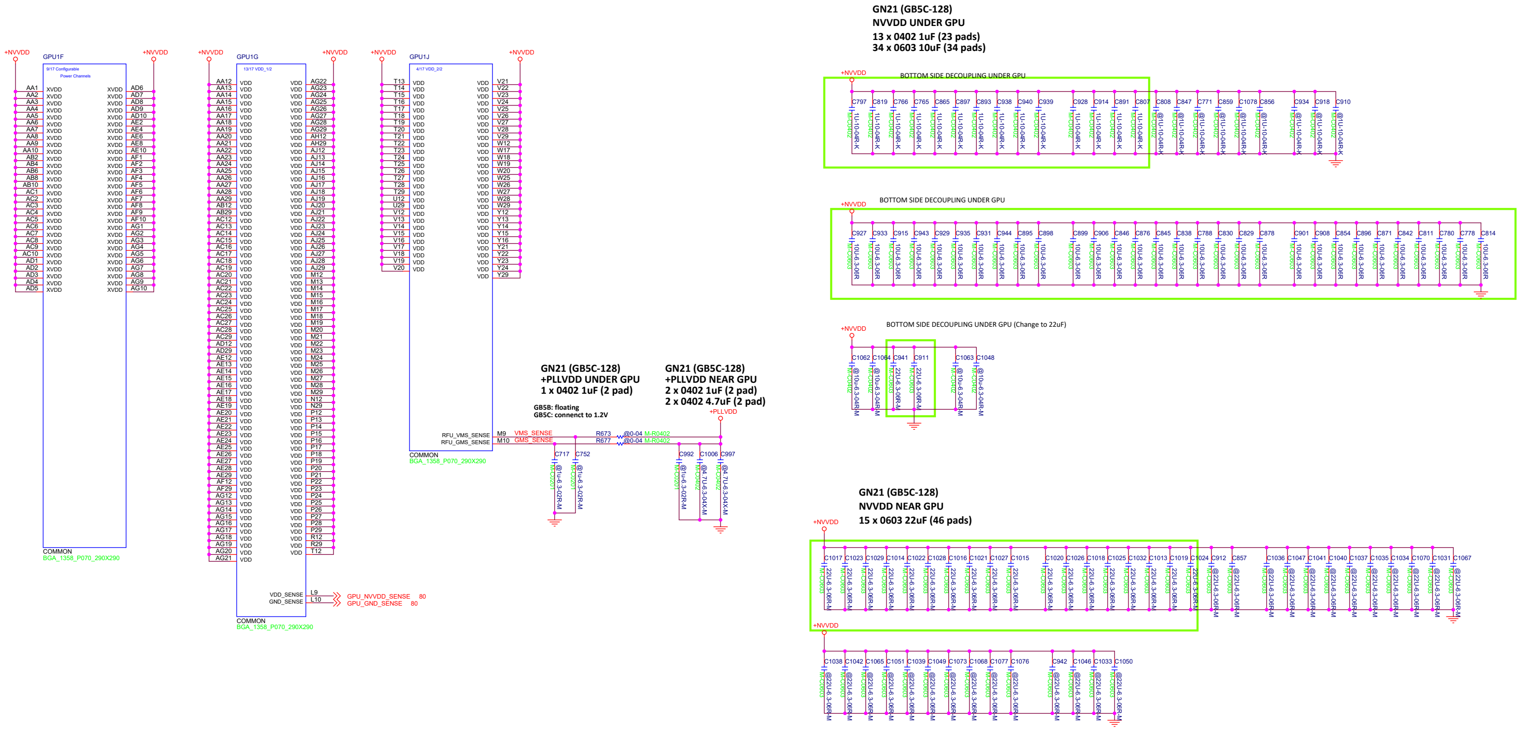
Uniwill Technology Inc

Title

GMXBGXX

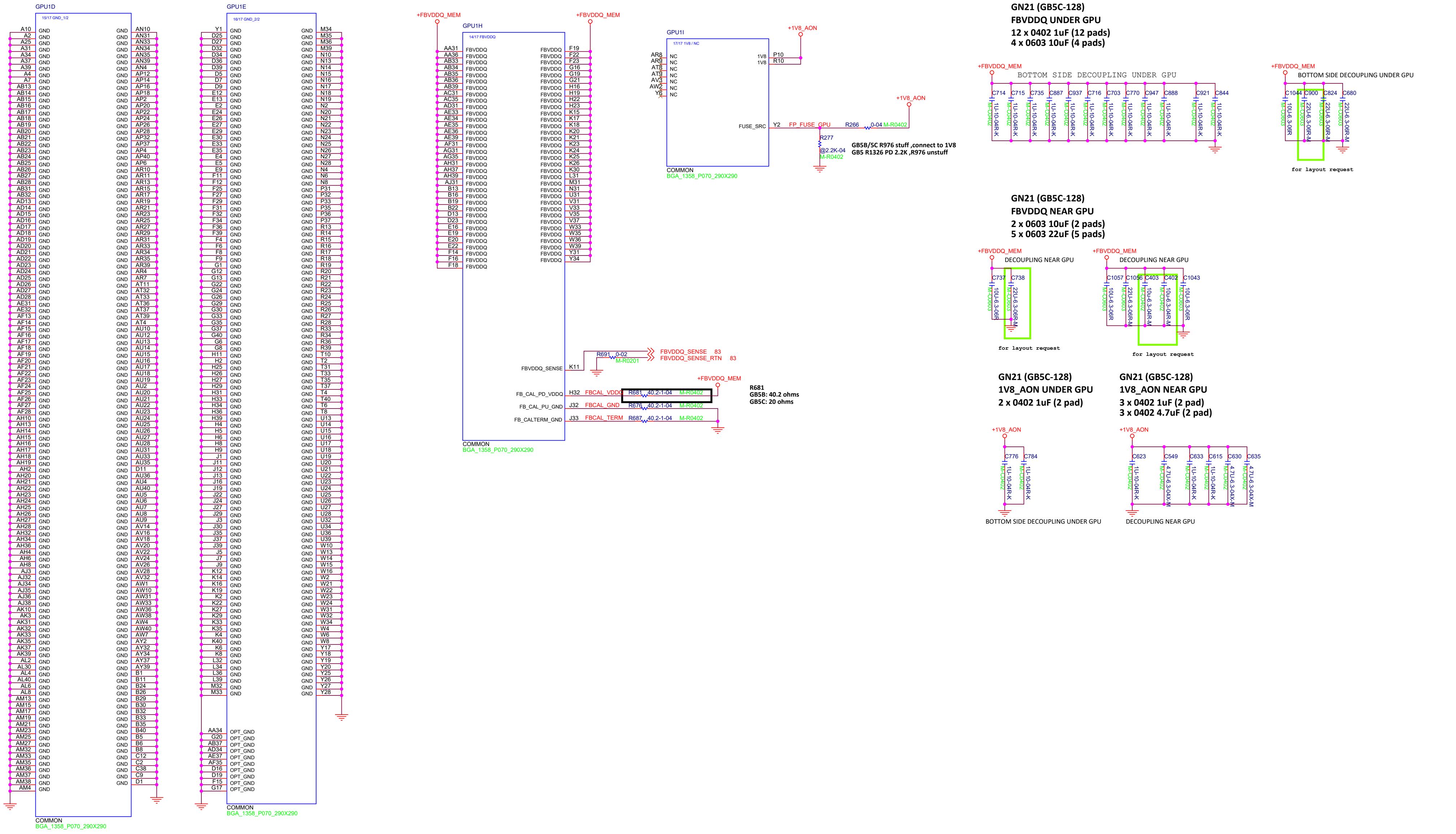
Size	Document Number	Rev
C	72 VRAM reserved	VB

Date: Friday, October 28, 2022 Sheet 72 of 87



Uniwill Technology Inc

Title	GMXBGXX	
Size D	Document Number 73 GPU GN21 PWR NVVDD	Rev VB
Date: Friday, October 28, 2022	Sheet 73 of 87	

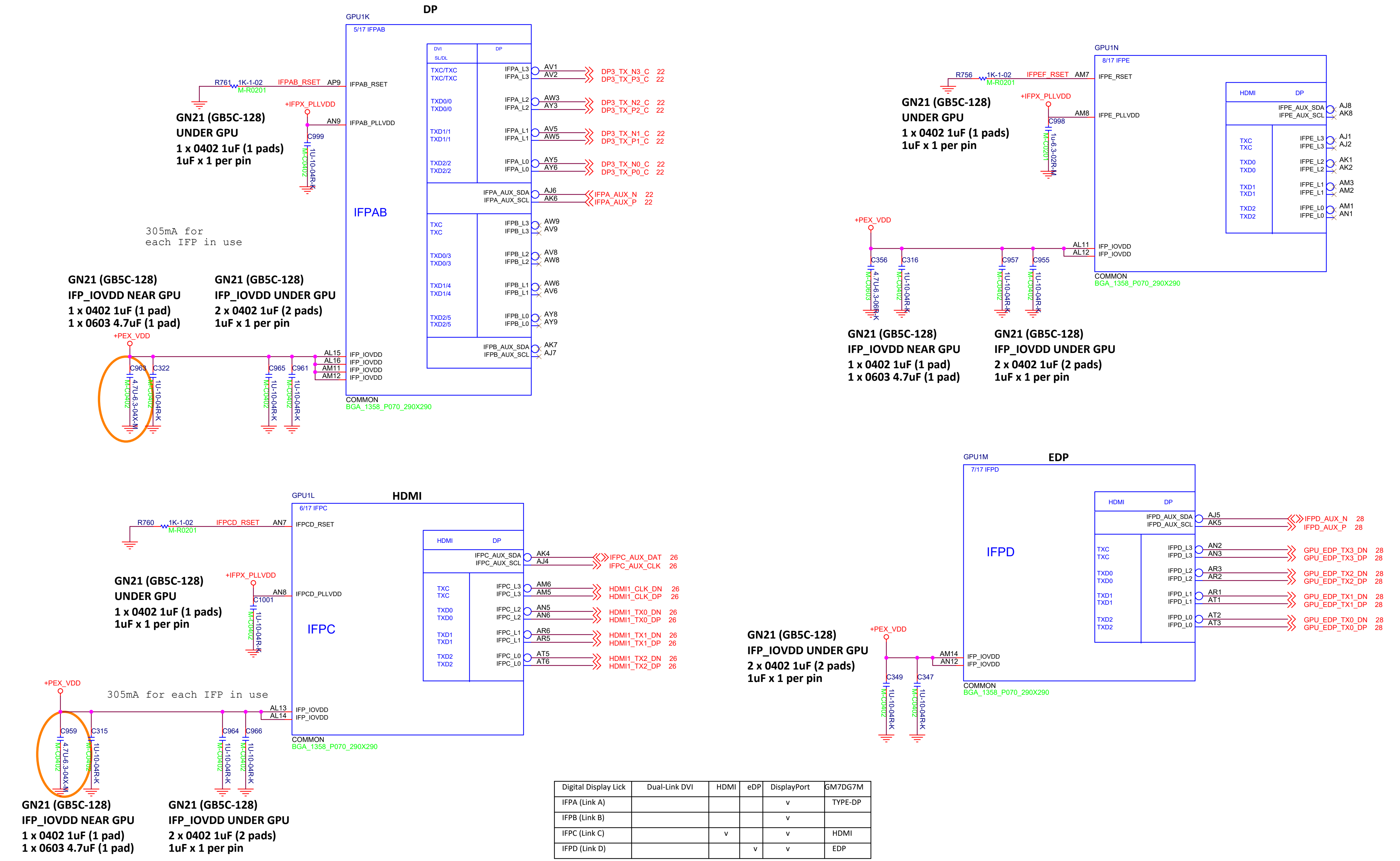


Uniwill Technology Inc

Title: GMXBGXX

Size	Document Number	Rev
Custom	74 GPU GN21 FBVDDQ/1V8_AON/GND	VB

Date: Friday, October 28, 2022 Sheet 74 of 87



Digital Display Lick	Dual-Link DVI	HDMI	eDP	DisplayPort	GM7DG7M
IFPA (Link A)				v	TYPE-DP
IFPB (Link B)				v	
IFPC (Link C)		v		v	HDMI
IFPD (Link D)			v	v	EDP

Uniwill Technology Inc

Title: GMXBGXX

Size: Custom | Document Number: 75 GPU GN21_IFPA_B _C _D _E | Rev: VB

Date: Friday, October 28, 2022 | Sheet 75 of 87

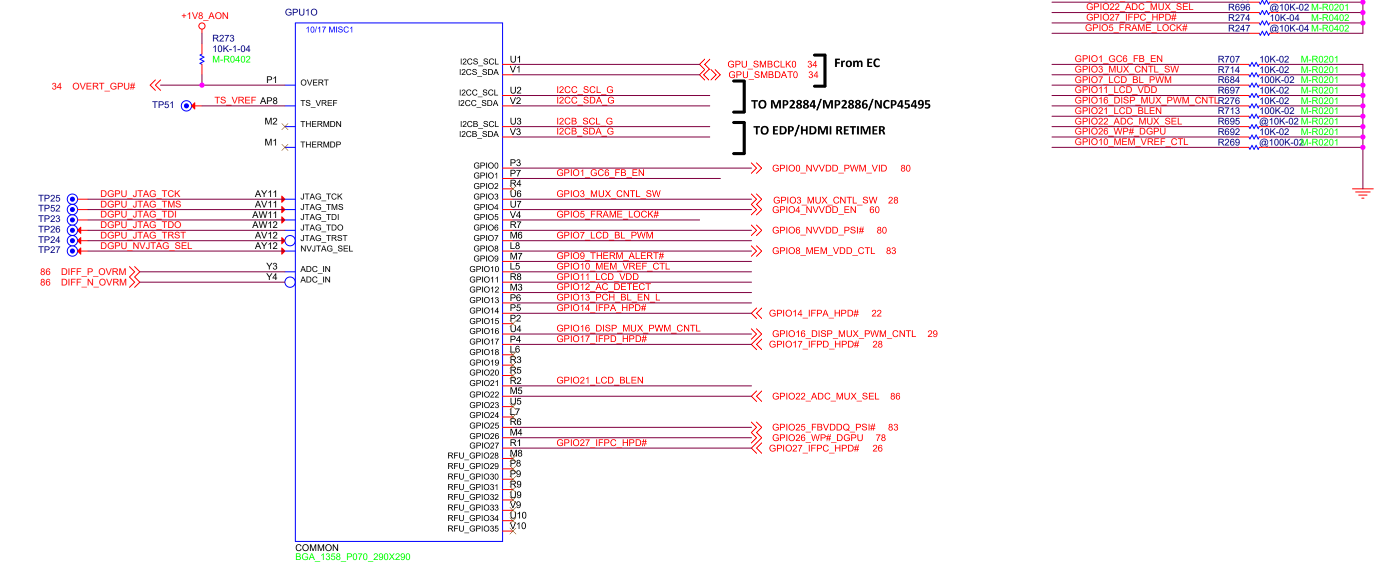
Uniwill Technology Inc

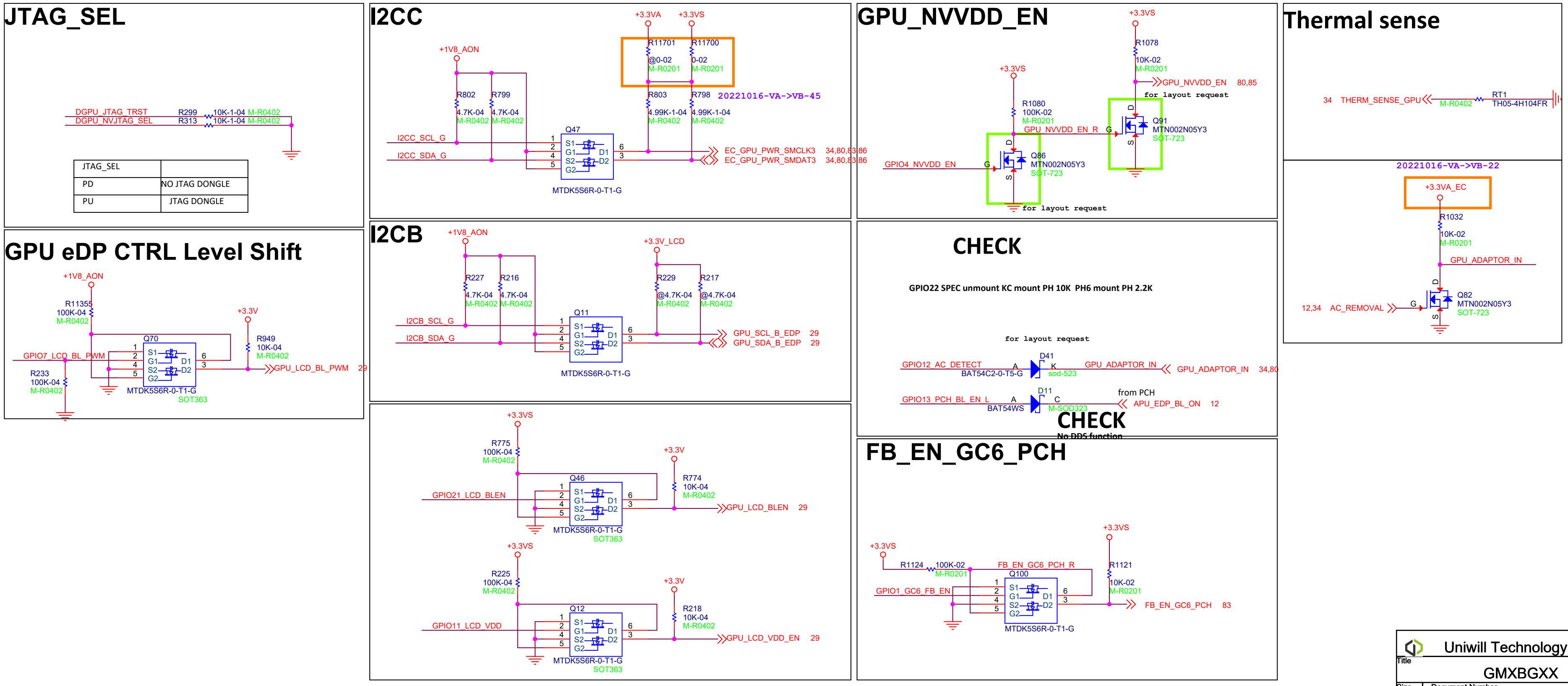
Title	GMXBGXX	
Size A	Document Number 76 GPU reserved	Rev VB
Date:	Friday, October 28, 2022	Sheet 76 of 87

GPIO6 : PH & PD reserved at VR side
GPIO8 : PH & PD reserved at VR side
GPIO25 : PH & PD reserved at VR side

I2CS:	Slave	For Dgpu thermal sensor
I2CC	Master	for Currtent Monitor/GPU/MP2884/EC
I2CB	Master	for LCD SMBUS

GPIO0 we follow SPEC define : GPIO0_NVVDD_PWM_VID
GPIO1 we follow SPEC define : GPIO1_GC6_FB_EN
GPIO2 we follow SPEC define : GPIO2_GPUEVENT#
GPIO3 we follow SPEC define : DISP_MUX_CNTL
GPIO4 we follow SPEC define : NVVDD_EN
GPIO5 we follow SPEC define : GPIO5_FRAME_LOCK#
GPIO7 we follow SPEC define : LCD_BL_PWM
GPIO8 we follow SPEC define : MEM_VDD_CTL
GPIO9 we follow SPEC define : THERM_ALERT# but no used
GPIO10 we follow SPEC define : unused
GPIO11 we follow SPEC define : LCD_VDD
GPIO12 we follow SPEC define : AC_DETECT
GPIO13 we follow SPEC define : PCH_BL_EN_L
GPIO14 we follow SPEC define : IFPA_HPD# for TYPE-DP
GPIO15 we follow SPEC define : GPIO15_IFPB_HPD# but no used
GPIO16 we follow SPEC define : DISP_MUX_PWM_CNTL
GPIO17 we follow SPEC define : IFPD_HPD# for HDMI
GPIO18 we follow SPEC define : unused
GPIO19 we follow SPEC define : unused
GPIO20 we follow SPEC define : unused
GPIO21 we follow SPEC define : LCD_BLEN
GPIO22 we follow SPEC define : ADC_MUX_SEL
GPIO23 we follow SPEC define : unused
GPIO24 we follow SPEC define : unused
GPIO25 we follow SPEC define : GPIO25_FBVDDQ_PSI#
GPIO26 we follow SPEC define : WP#_DGPU
GPIO27 we follow SPEC define : GPIO27_IFPC_HPD#

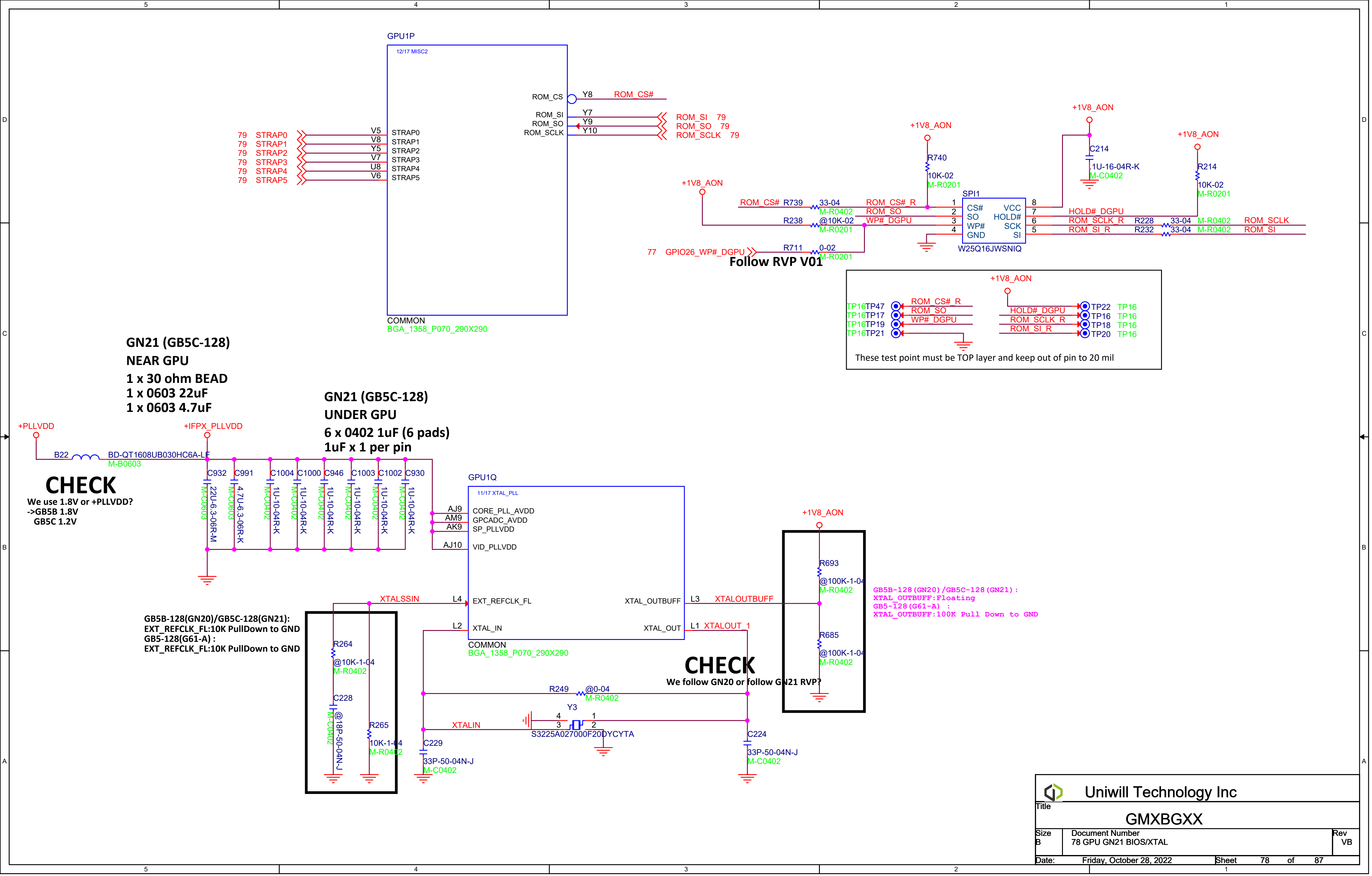




JTAG_SEL	
PD	NO JTAG DONGLE
PU	JTAG DONGLE

Uniwill Technology Inc

Title	GMXBGXX	
Size C	Document Number: 77 GPU GN21 GPIO/Thermal/I2C	Rev VB
Date: Friday, October 28, 2022	Sheet 77 of 87	


GPU1P
12/17 MISC2
ROM_CS
ROM_SI
ROM_SO
ROM_SCLK
Y8 ROM_CS#
Y7
Y9
Y10
ROM_SI 79
ROM_SO 79
ROM_SCLK 79
79 STRAP0
79 STRAP1
79 STRAP2
79 STRAP3
79 STRAP4
79 STRAP5
V5 STRAP0
V8 STRAP1
Y5 STRAP2
V7 STRAP3
U8 STRAP4
V6 STRAP5
COMMON
BGA_1358_P070_290X290
+1V8_AON
R740
10K-02
M-R0201
C214
1U-16-04R-K
M-C0402
R214
10K-02
M-R0201
SPI1
CS# VCC
SO HOLD#
WP# SCK
GND SI
W25Q16JWSNIQ
ROM_CS# R739 33-04 M-R0402 ROM_CS#_R
ROM_SO
R238 @10K-02 M-R0201 WP#_DGPU
77 GPIO26_WP#_DGPU R711 0-02 M-R0201
Follow RVP V01
HOLD#_DGPU
ROM_SCLK_R R228 33-04 M-R0402 ROM_SCLK
ROM_SI_R R232 33-04 M-R0402 ROM_SI
TP16 TP47 ROM_CS#_R
TP16 TP17 ROM_SO
TP16 TP19 WP#_DGPU
TP16 TP21
HOLD#_DGPU TP22 TP16
ROM_SCLK_R TP16 TP16
ROM_SI_R TP18 TP16
TP20 TP16
These test point must be TOP layer and keep out of pin to 20 mil
GN21 (GB5C-128)
NEAR GPU
1 x 30 ohm BEAD
1 x 0603 22uF
1 x 0603 4.7uF
GN21 (GB5C-128)
UNDER GPU
6 x 0402 1uF (6 pads)
1uF x 1 per pin
+PLLVDD
+IFPX_PLLVDD
B22 BD-QT1608UB030HC6A-LF M-B0603
CHECK
We use 1.8V or +PLLVDD?
->GB5B 1.8V
GB5C 1.2V
C932 22U-6.3-06R-M M-C0603
C991 4.7U-6.3-06R-K M-C0603
C1004 1U-10-04R-K M-C0402
C1000 1U-10-04R-K M-C0402
C946 1U-10-04R-K M-C0402
C1003 1U-10-04R-K M-C0402
C1002 1U-10-04R-K M-C0402
C930 1U-10-04R-K M-C0402
GPU1Q
11/17 XTAL_PLL
AJ9 CORE_PLL_AVDD
AM9 GPCADC_AVDD
AK9 SP_PLLVDD
AJ10 VID_PLLVDD
XTALSSIN L4 EXT_REFCLK_FL
L2 XTAL_IN
XTAL_OUTBUFF L3 XTALOUTBUFF
XTAL_OUT L1 XTALOUT_1
COMMON
BGA_1358_P070_290X290
GB5B-128(GN20)/GB5C-128(GN21):
EXT_REFCLK_FL:10K PullDown to GND
GB5-128(G61-A) :
EXT_REFCLK_FL:10K PullDown to GND
R264 @10K-1-04 M-R0402
C228 @18P-50-04N-J M-C0402
R265 10K-1-04 M-R0402
R249 @0-04 M-R0402
Y3
XTALIN
S3225A027000F20DYCYTA
C229 33P-50-04N-J M-C0402
C224 33P-50-04N-J M-C0402
CHECK
We follow GN20 or follow GN21 RVP?
+1V8_AON
R693 @100K-1-04 M-R0402
R685 @100K-1-04 M-R0402
GB5B-128(GN20)/GB5C-128(GN21):
XTAL_OUTBUFF:Floating
GB5-128(G61-A) :
XTAL_OUTBUFF:100K Pull Down to GND
Uniwill Technology Inc
Title
GMXBGXX
Size B
Document Number 78 GPU GN21 BIOS/XTAL
Rev VB
Date: Friday, October 28, 2022
Sheet 78 of 87

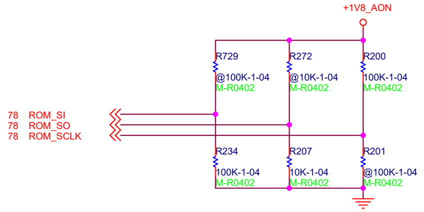
GB5B PU 100K or 10K

GB5B	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

GB5C PU 200K or 20K

GB5C	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.05	1.8	1.854
M	0.39	0.6	0.75
L	0	0	0.21
Invalid	0.75V<pin voltage<1.05V		
	0.21V<pin voltage<0.39V		

FS_OVERT			
FUNCTION	ROM_SO	ROM_SI	ROM_SCLK
GB5:enable	L	L	L
GB5B/5C:enable	L	L	H
GB5B/5C:disable	L	L	L



For GN21 BOM

GN21-X2 GDDR6						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
16Gb	Samsung	K4ZAF325BC-SC16 C-die	0XA	L	M	H
16Gb	Hynix	H56G42AS4DX014 A-die	0X8	L	L	M

For GN20 BOM

GN20 GDDR6						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H
	Hynix	H56C8H24AIR-S2C A-die	0X2	L	H	L

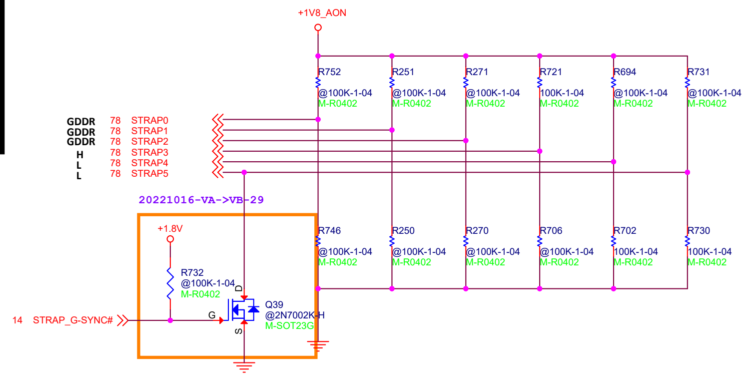
Strap5,4,3 LLH			
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
0	0	0	1

1:SMB_ALT_ADDR dual GPU alternate
0:SMB_ALT_ADDR single GPU

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG reduced signal amplitude
0:PCIE_CFG normal signal swing

1:VGA_DEVICE class code 300
0:VGA_DEVICE class code 302



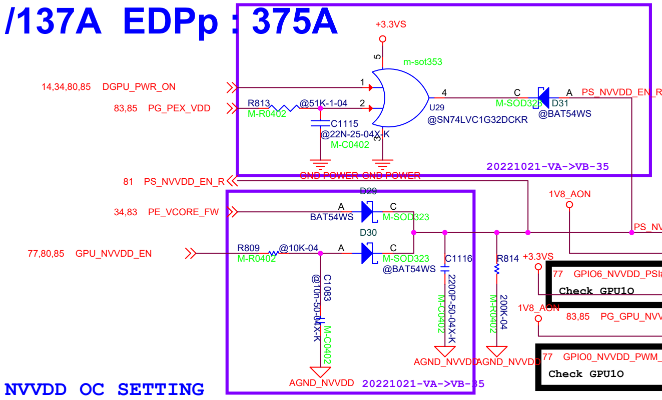
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	M	L	1001	FS_OVERT ENABLE	DEFAULT
L	L	M	1000	FS_OVERT DISABLE	

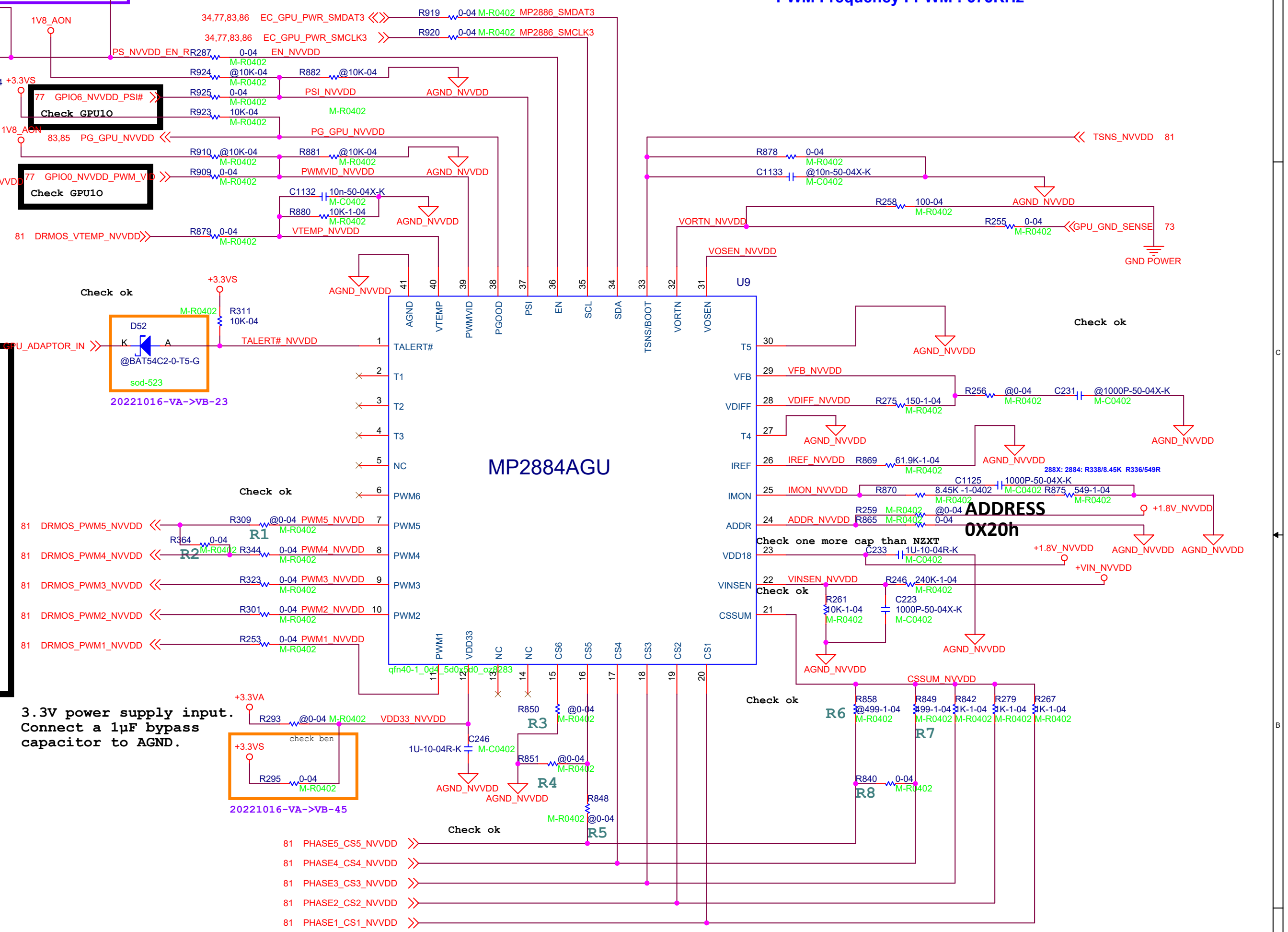
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

NVVDD
EDPc : 118A /137A EDPp : 375A

MB2 NVVDD VID Requirements
Voltage range programmability:0.3V~1.3V
Number of programmable voltages: 160 Levels
Programmable voltage steps: 6.25mV
Boot Voltage :0.75V
Setting Time: < 100uS for rising, no restriction on falling

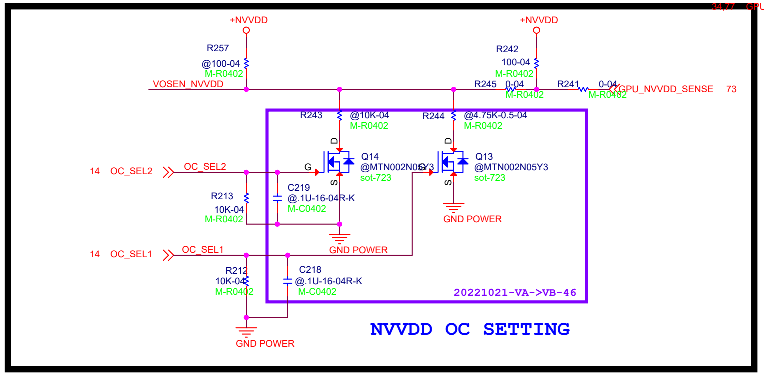
NVVDD Voltage Tolerance Specification
Output Voltage DC Tolerance:+/-2.5%
AC Tolerance within 20MHz2 (Normal operation,
DVS and AutoPSI) :Undershoot: -6% Overshoot: +10%
PWM Frequency FPWM : 675KHz





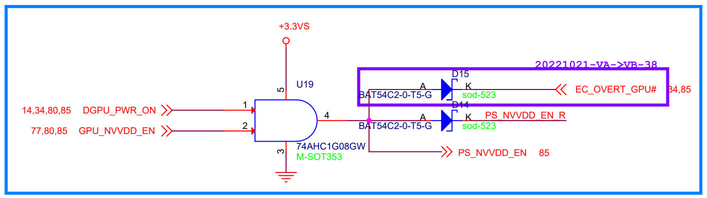
V11 ADD NVVDD OC SETTING

OC_SEL2	OC_SEL1	Default NVVDD	NVVDD +5%	NVVDD +10%
L	L	ON	OFF	OFF
H	L	OFF	ON	OFF
L	H	OFF	OFF	ON



NVVDD OC SETTING

for NV sequence request



	MP2886A 5 Driver 5	MP2884A 4 Driver 5	MP2886A 4 Driver 5
R1	0	X	X
R2	X	0	0
R3	0	X	0
R4	X	X	0
R5	0	X	X
R6	1K	X	X
R7	1K	499	499
R8	X	0	0

Uniwill Technology Inc

Title	GMXBGXX	
Size C	Document Number: 80 POWER GN21 NVVDD PWMIC	Rev VB
Date: Friday, October 28, 2022	Sheet 80 of 87	

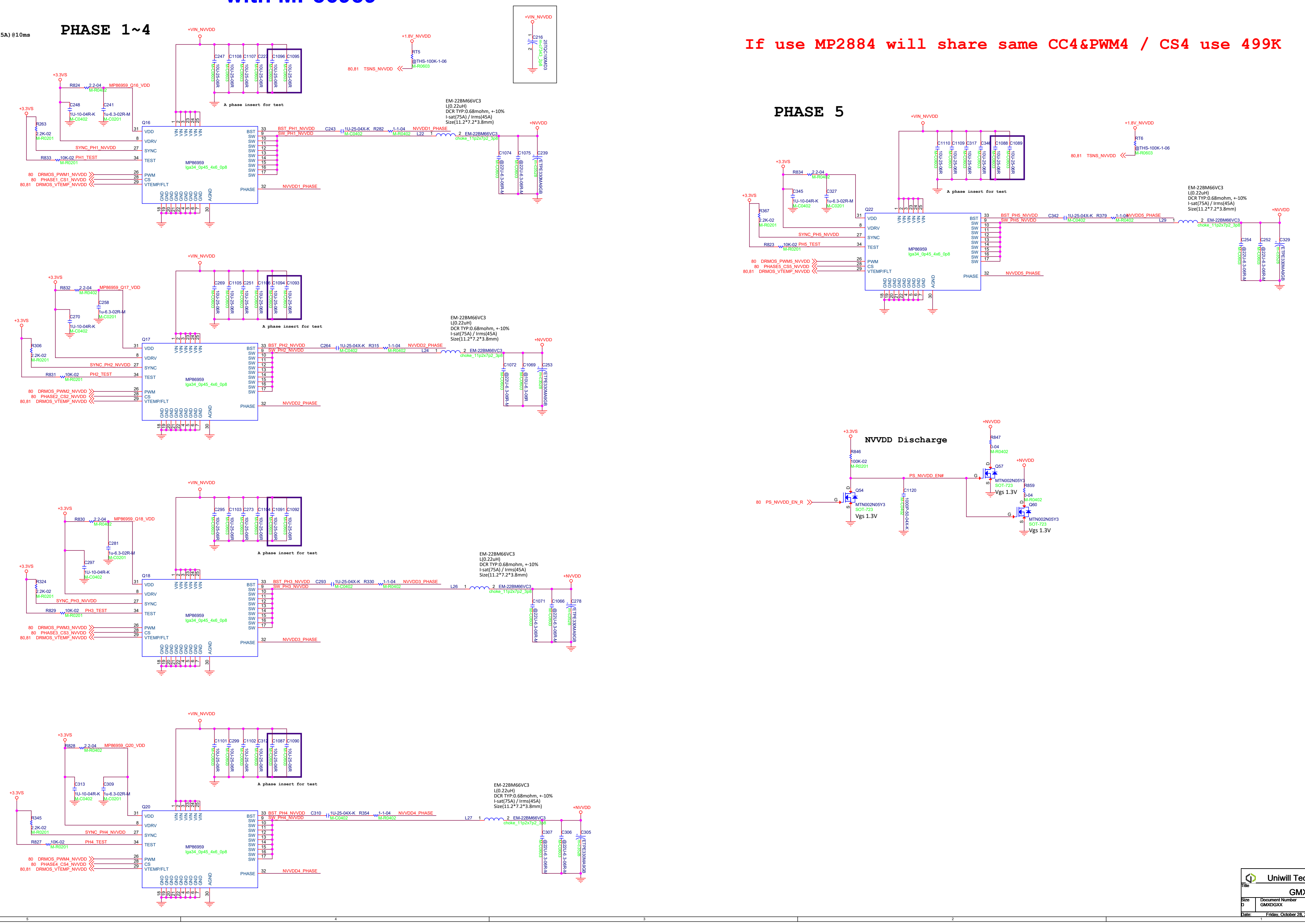
NVVDD
EDPc : 118A /137A EDPp : 375A

+NVVDD with MP86959

GN21 MB2 (115+25W)
NVVDD
Continuous : 137A
Peak : 375A

MP86959
SPEC : 36A(45A) / PEAK :65A(75A)@10ms
5 phase
Continuous : 180A
Peak : 325A

If use MP2884 will share same CC4&PWM4 / CS4 use 499K



5 4 3 2 1

D C B A

Uniwill Technology Inc

Title
GMXBGXX

Size	Document Number	Rev
Custom	82 Reserved	VB

Date: Friday, October 28, 2022 Sheet 82 of 87

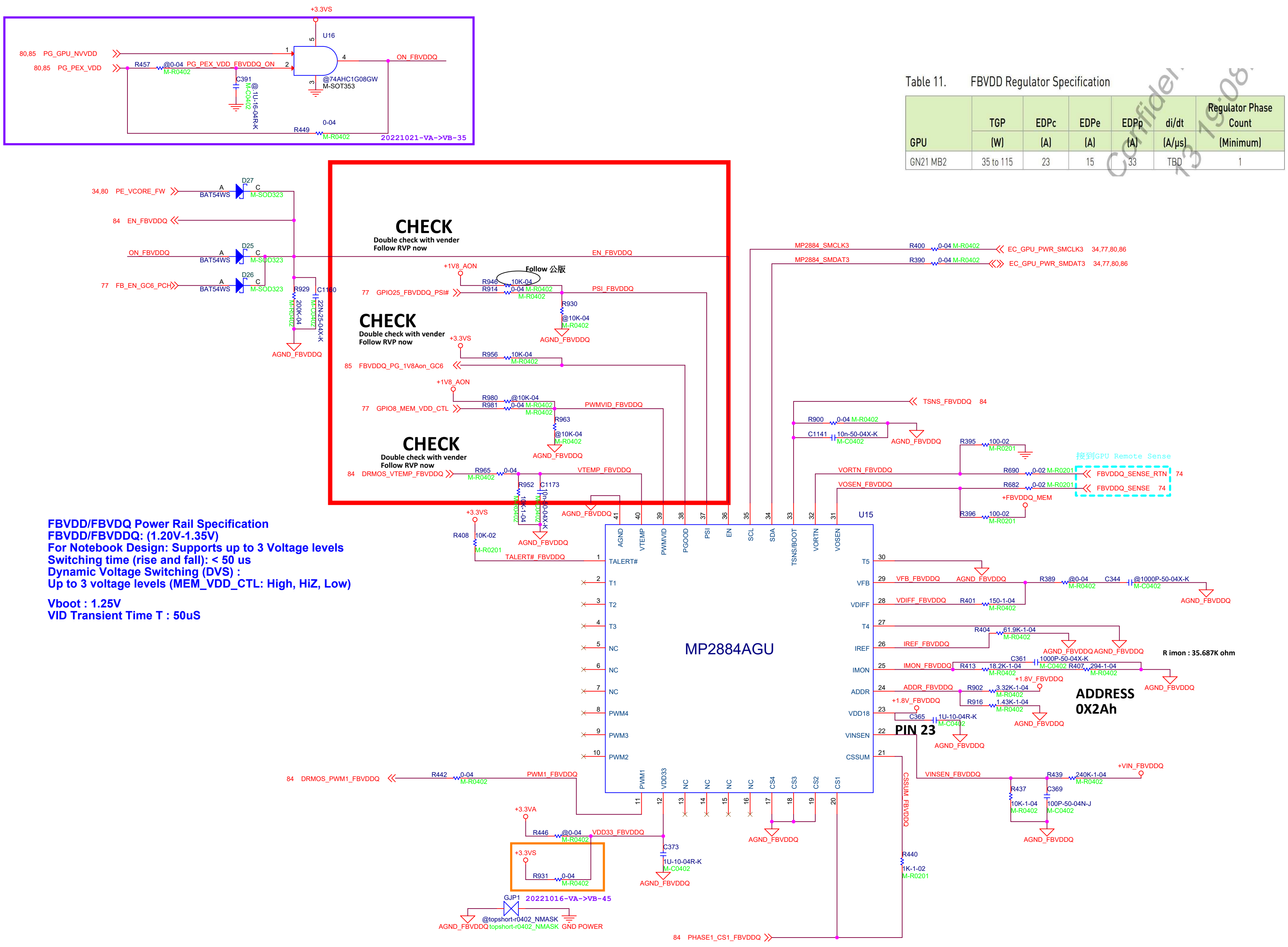


Table 11. FBVDD Regulator Specification

GPU	TGP (W)	EDPc (A)	EDPe (A)	EDPp (A)	di/dt (A/μs)	Regulator Phase Count (Minimum)
GN21 MB2	35 to 115	23	15	33	TBD	1

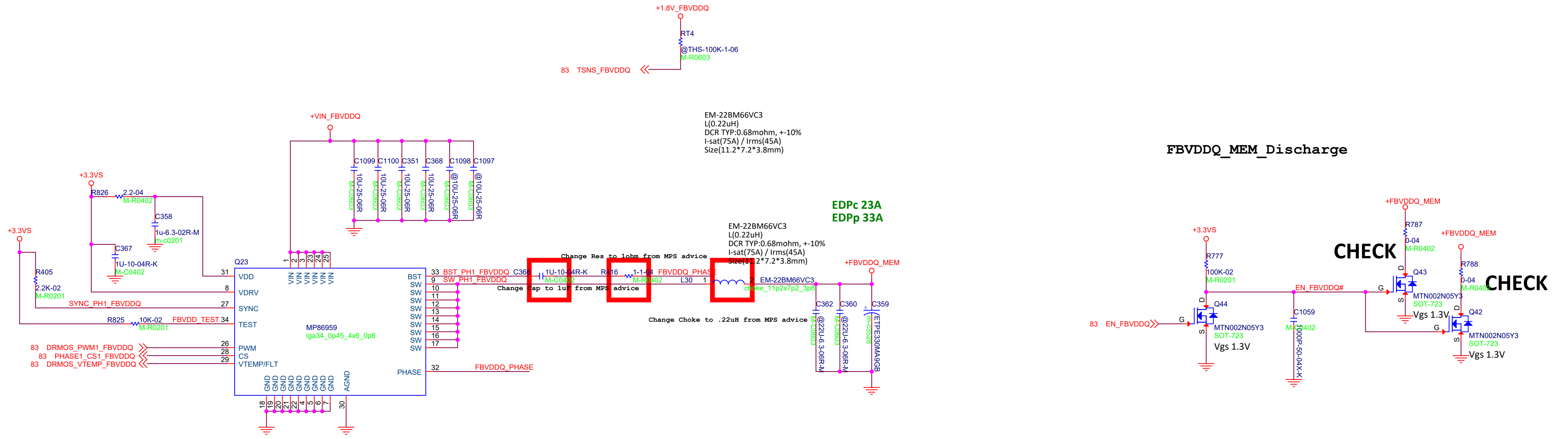
FBVDD/FBVDQ Power Rail Specification
FBVDD/FBVDDQ: (1.20V-1.35V)
For Notebook Design: Supports up to 3 Voltage levels
Switching time (rise and fall): < 50 us
Dynamic Voltage Switching (DVS) :
Up to 3 voltage levels (MEM_VDD_CTL: High, HiZ, Low)

Vboot : 1.25V
VID Transient Time T : 50uS

+FBVDD

GN21 MB2
FBVDD
Continuous : 23A
PEAK : 33A

MP869959
SPEC : 36A(45A) / PEAK :65A(75A)@10ms
1 phase
Continuous : 36A
Peak : 65A



Uniwill Technology Inc

Title	GMXBGXX	
Size: Custom	Document Number: GMXDGXX	Rev: VB
Date: Friday, October 28, 2022	Sheet 84 of 87	

PEX_VDD

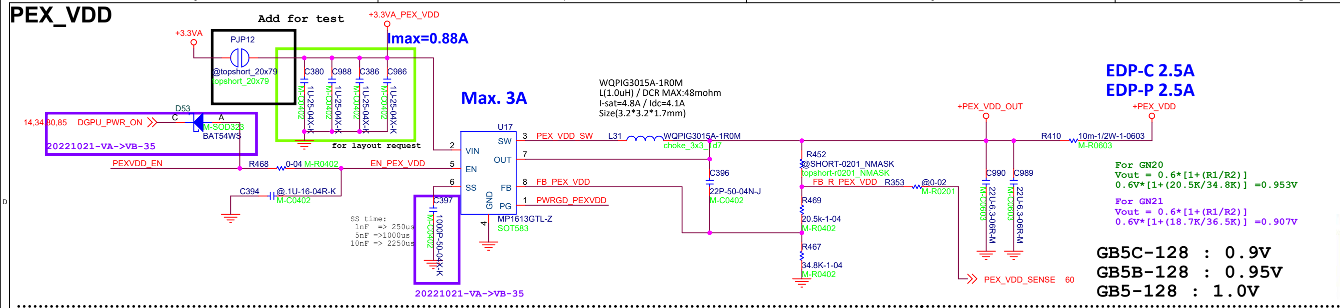
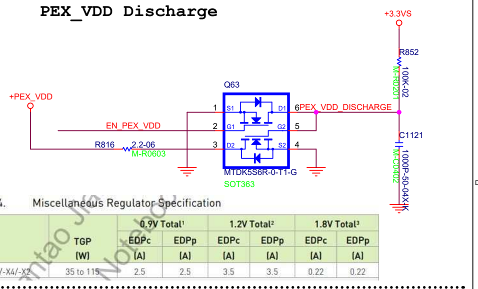


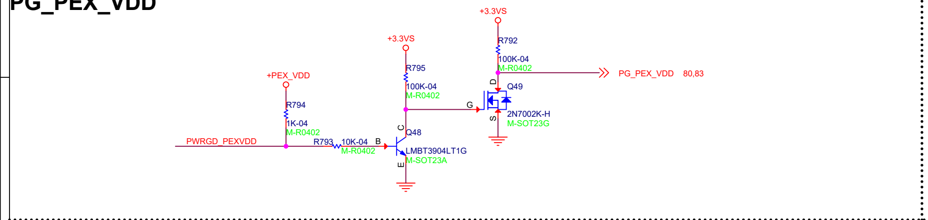
Table 14. Miscellaneous Regulator Specification

GPU	TGP [W]	0.9V Total EDPc [A]	0.9V Total EDPp [A]	1.2V Total EDPc [A]	1.2V Total EDPp [A]	1.8V Total EDPc [A]	1.8V Total EDPp [A]
GN21-X6/-X4/-X2	35 to 115	2.5	2.5	3.5	3.5	0.22	0.22

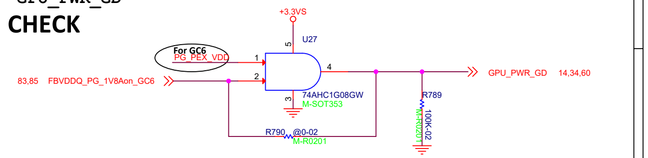
PEX_VDD Discharge



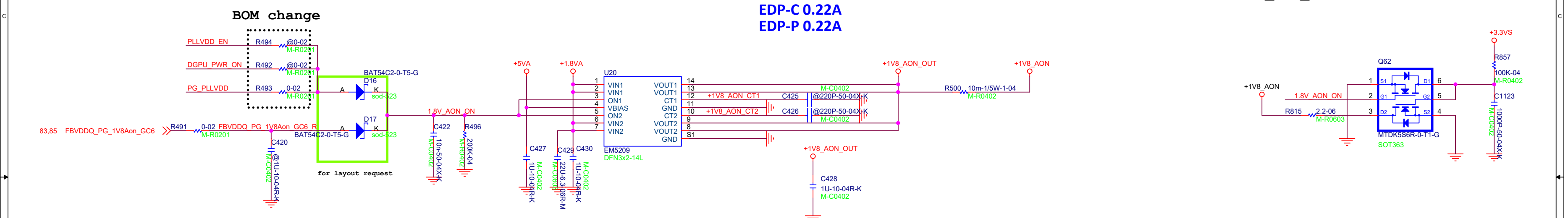
PG_PEX_VDD



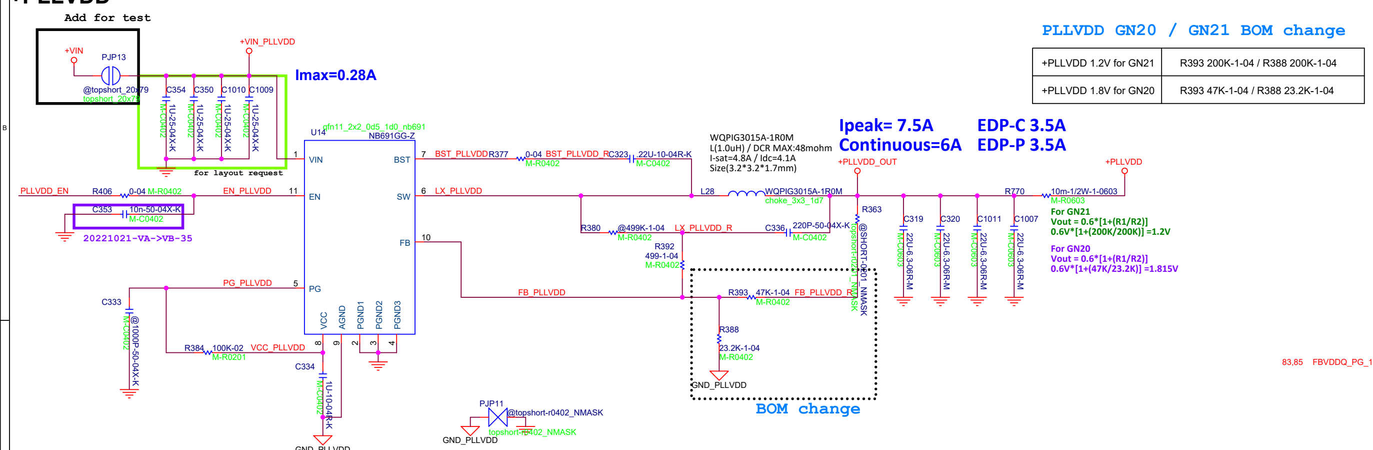
GPU_PWR_GD CHECK



+1V8_AON



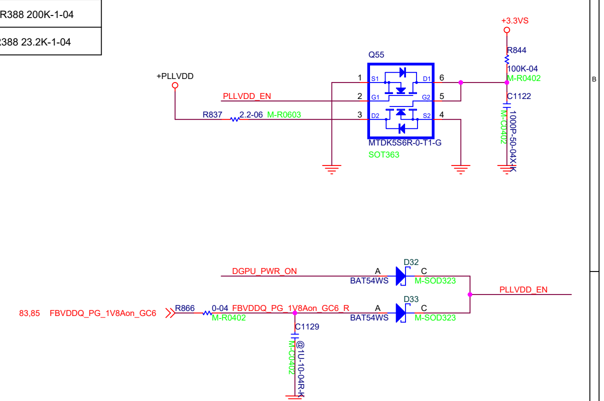
+PLLVDD



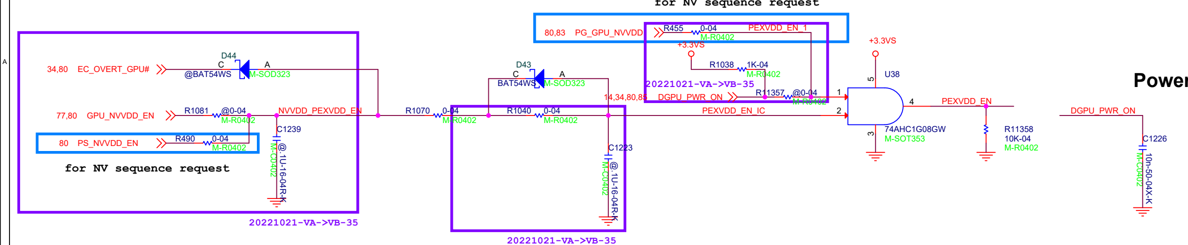
PLLVDD GN20 / GN21 BOM change

+PLLVDD 1.2V for GN21	R393 200K-1-04 / R388 200K-1-04
+PLLVDD 1.8V for GN20	R393 47K-1-04 / R388 23.2K-1-04

+PLLVDD_Discharge



for NV sequence request



Sequence

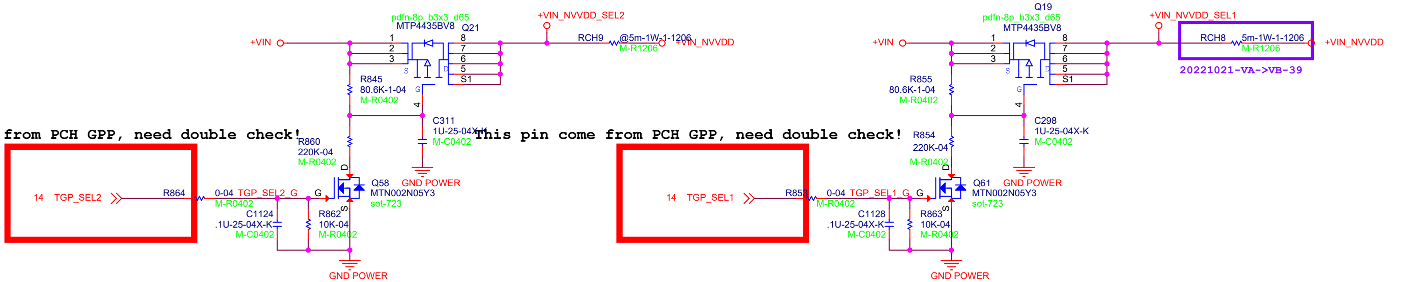
Power-Up Sequence : 1V2 ->1V8AON->NVVDD->PEXVDD->FBVDD(Q)

Power-Down Sequence : PEXVDD -> NVVDD ->FBVDD(Q) -> (1V2 and 1V8AON)

Uniwill Technology Inc		
Title	GMXBGXX	
Size: Custom	Document Number: 85 POWER GN21 PEX_VDD/1V8_AON_K	Rev: VB
Date: Friday, October 28, 2022	Sheet 85 of 87	

This pin come from PCH GPP, need double check!

This pin come from PCH GPP, need double check!

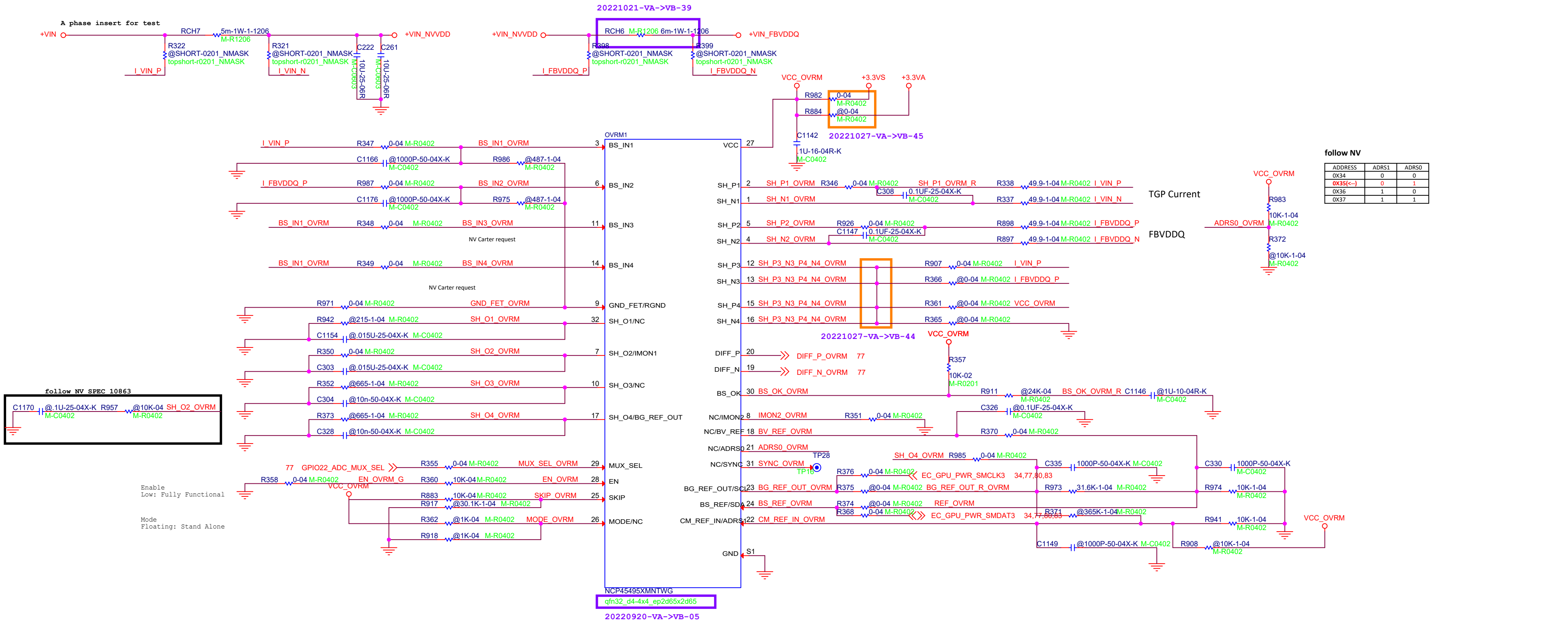


NVVDD Peak current 375A

place 10uf cap in +VIN_NVVDD
near to the 5 mohm resistor,
prevent 19v noise

TGP_SEL2	TGP_SEL1	Default TGP	TGP+	TGP+
L	L			
H	L	ON	OFF	OFF
L	H			

TGP_SEL2	TGP_SEL1	Default TGP	TGP +5%	TGP +10%
L	L	ON	OFF	OFF
H	L	OFF	ON	OFF
L	H	OFF	OFF	ON



follow NV

ADDRESS	ADRS1	ADRS0
0X34	0	0
0X35(<--)	0	1
0X36	1	0
0X37	1	1

Version A BOM change list

01 Change C1060 C1055 VALUE from 22uF-10V-06R-M to 22U-6.3-06R-M for Procurement requirements

02 Change C1196 VALUE from 4.7U-10-06R-K to 4.7U-6.3-06R-K for Procurement requirements

03 Change CNDP1 VALUE from MINI-DP,20P,D,P0.6,C17722-120A9,ATP to MINI-DP,20P,D,P0.6,C17745-12029,ATP for ME requirements

04 Change H5 from SCRR223022-1C35 to SCRR221005-4C50 for ME requirements

Version A to B change list

01 Change R610 footprint from 0603 to 0402

02 Change CNEDP1 pin 35 to +WEBCAM_PWR

03 ADD 4 ZONE KB CONN for IDZ

04 ESPI_CS# / ESPI_ALERT#_APU PULL HIGH change to +1.8VA_EC

05 change NCP45495XMNTWG new footprint

06 Reserved D48 D49 for FAN HW solution

07 stuff C1210_C1209 unstuff C1237_C1232 for MPS power solution

08 Unmount R383, Mount R1004 for prevent 1.8V leakage voltage

09 Unmount U37, U35, Mount R1013, R992 for Cost down

10 Change L3/L4 VALUE & footprint to new part (AMPI0420EDR56MT /choke_4p6x4p1_2P0) for POWER solution

11 CPU PIN USBC_PD_INT(AJ6) pull down 100K follow RG

12 HDMI_HPD_EC PULL HIGH 10K to +3.3V_HDMI_RT for HDMI Issue

13 reserve

14 Re-adjust EC GPIO let EN_LCD_VCC_MUX change from GPG0 to GPB1 due to the default setting is GPO while EC bootup

15 Change R1017 of power source from +3.3V to +3.3VA_EC for prevent leakage current in S5/DC

16 Remove D38, Add a N MOSFET between TP_STATUS and LID# for prevent leakage in S5

17 Change R54 of power source from +3.3VA to +3.3VS, to solve the voltage from CS pin leak to +3.3V
Change U4 of PMBUS from EC_SML1CLK/ EC_SML1DAT to EC_SML1CLK_S3/ EC_SML1DAT_S3

18 add D50, R11683 for reserve SUS_ON turn on +3.3VS path

19 Change R818, R822 of pull up PWR rail from +3.3VA to +3.3VA_EC for correct sequence

20 Delete TP29, Re-define EC GPG0 from WLAN_EN to +5VA_DDR5_SW_CTRL for DDR5 power consumption too high in S5

21 Add R11697 for DDR5 power enable to do once power cycle while system boot up, to solve DDR5 power consumption too high

22 Change R1032 of pull up PWR rail from +3.3VS to +3.3VA_EC, to solve GPU_ADAPTOR_IN leak to +3.3VS in AC/S5

23 Delete R310, Add D52 between GPU_ADAPTOR_IN and TALERT#_NVVDD for isolated both different pull up power rail

24 Delete D36, to avoid the APU_RSMRST# has diode forward voltage before rise up

25 Let NET S0A3_APU move to Q94
Modify TP_INT# level shift circuit, to prevent leakage current from +1.8VA in S5

26 Modify Q73 BT_ON_APU level shift circuit, to prevent leakage current from +1.8VA in S5

27 Add Q407, modify WLAN_ON_APU level shift circuit, to prevent leakage current from +1.8VA in S5

28 Delete R10 for prevent +3.3V leak to +1.8VA through Q2 body diode un-stuff R10

29 Change R959, R977, R984 of power rail from S0 to S5 for co-use daughter board with intel

30 Un-stuff R732, Q39, don't need to reserve for G-sync control function

31 Add R11688 and unstuff, it's for disconnect ESPI_ALERT# from debug IC to MB. Due to ESPI_ALERT# will keeping low when use debug board on the AMD platform

32 Modify Q29 LAN_WAKE#_APU level shift circuit, to prevent leakage current from +1.8VA in S5
Add Q408, modify WLAN_WAKE#_APU level shift circuit, to prevent leakage current from +1.8VA in S5

33 Add R11691, R11692, R11693, R11693, R11694, R11695 for power measured requirement

34 Base on test result, Stuff C783,C782 to improve power ripple for transient

35 Chage GPU Power Sequence:
a. Unstuff D30,R809,C1083,D31,U29,C1115,R813,R11357,R784,C1223
b. stuff: R55,R455
c. change C1116 to 2200p
d. change C353 to 10n
e. change C397 to 1000p
f. change R1040 to 0ohm

36 Change L7 / L6 / L5 / L2 / L13 VALUE to EM-12BM18V02 for POWER solution

37 Change R153/C145 VALUE to 51-1-04/33P-50-04N-J for EMI HDA solution

38 D15 connect to EC_OVERT_GPU# for POWER Issue

39 Change RCH6/RCH8 VALUE 5m-1W-1-1206 to 10m-1W-1-1206 for EMI HDA solution

40 Add R-SENSE(R11696) for +1.1VS_VDDIO_MEM

41 Unstuff C1278 for 0.75V Power Sequence

42 Change Q1,Q3,Q4,Q5,Q6,Q7 of VCC PWR rail from +3.3V to +3.3VS for leakage voltage from CS pin while Modern standby

43 Move RUN_ON from GPG6 of EC to GPG0 of EC

44 Correct OVRM circuit, follow common design

45 Stuff R982, Unstuff R884, Change OVRM1, U9, U15, Q47 to VS power rail

46 Unstuff R243,R244,Q14,Q13 and R245 change to 0ohm for reserve NVVDD OC Setting

Version B to B1 change list

Version C to 1.0 change list