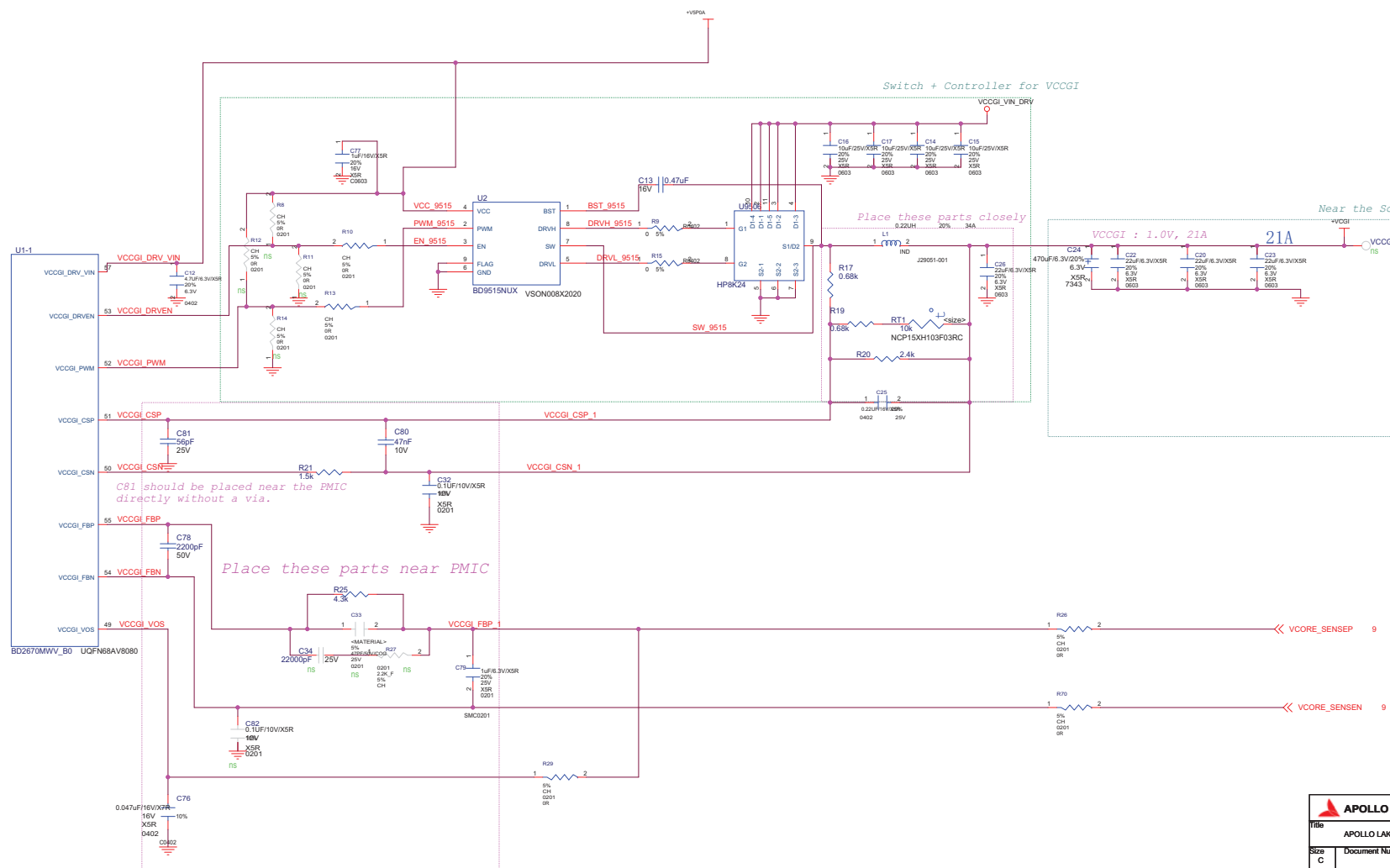
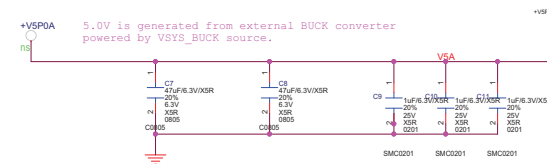
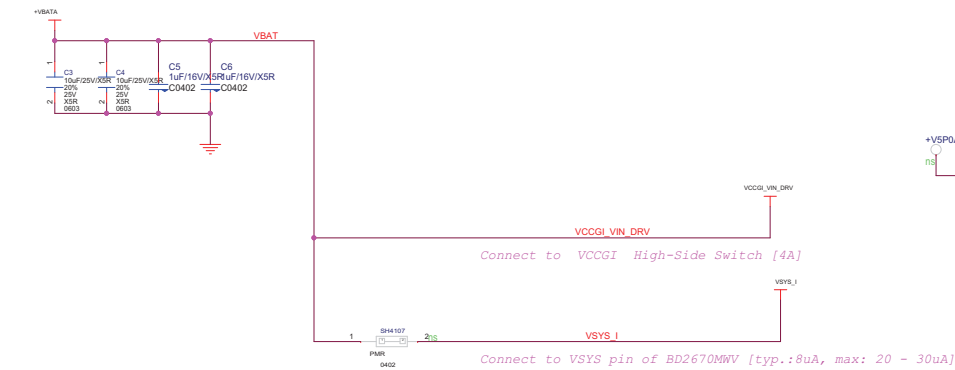
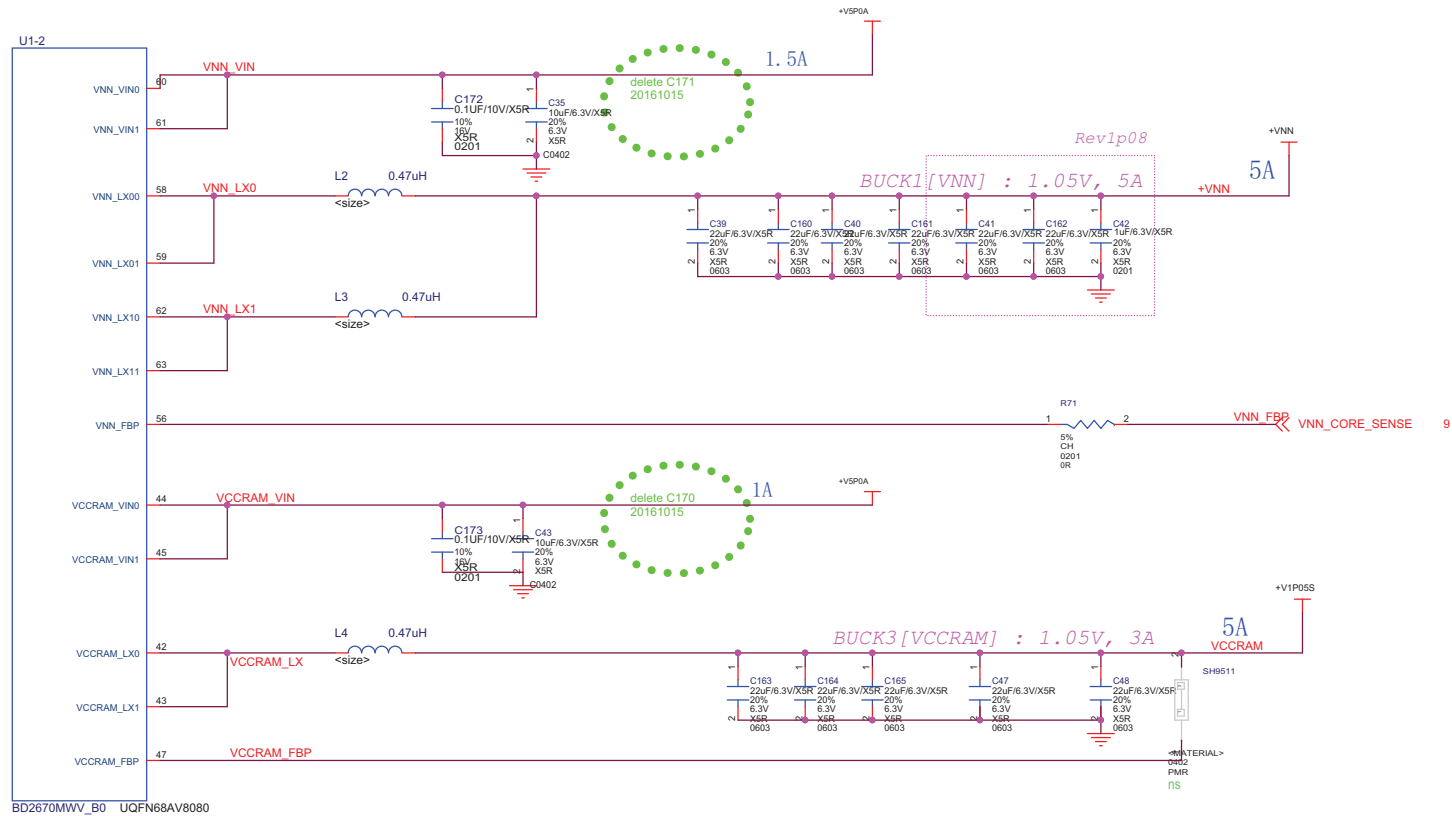


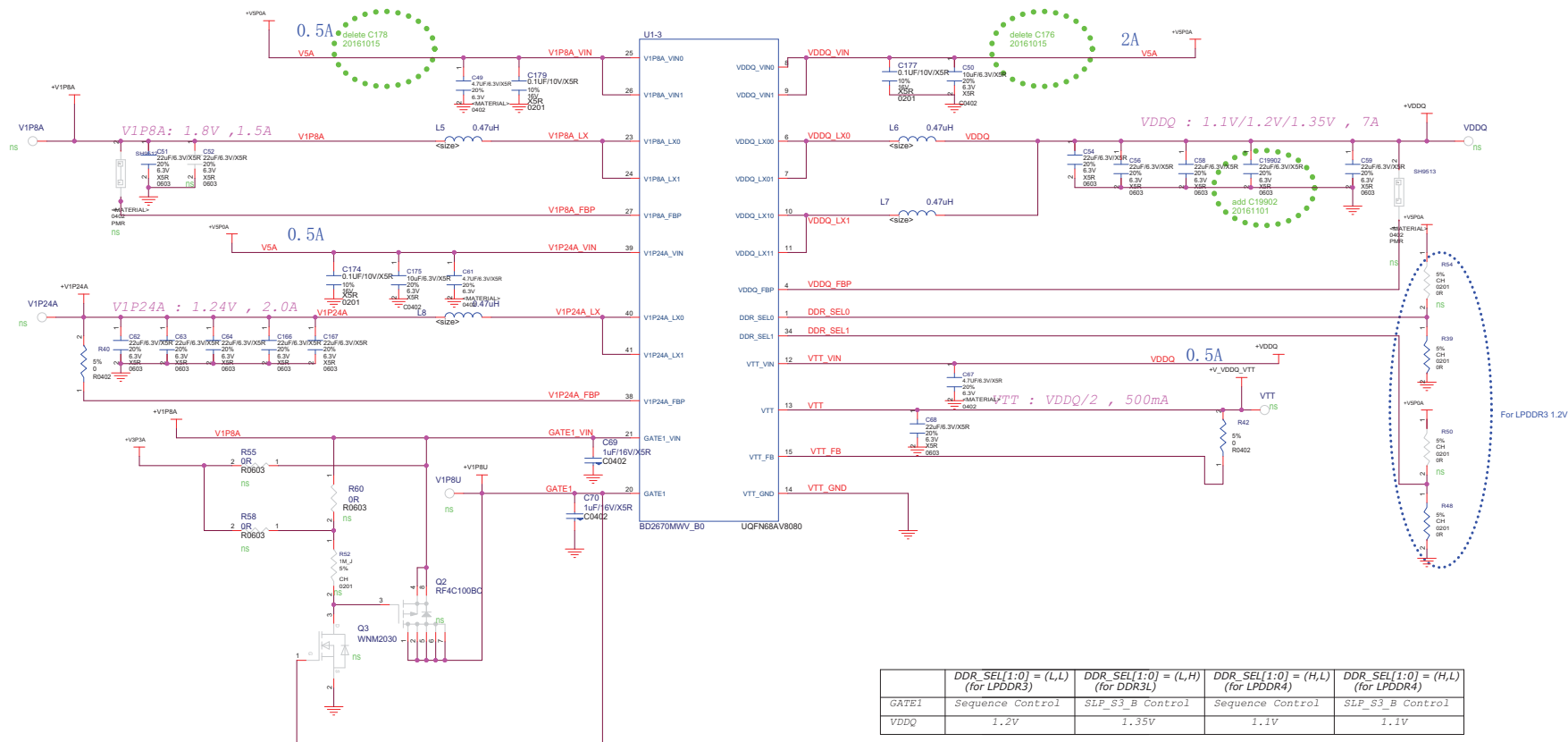
2S/3S battery input [5.4V to 21V]



VNN[BUCK1], VCCRAM[BUCK3]

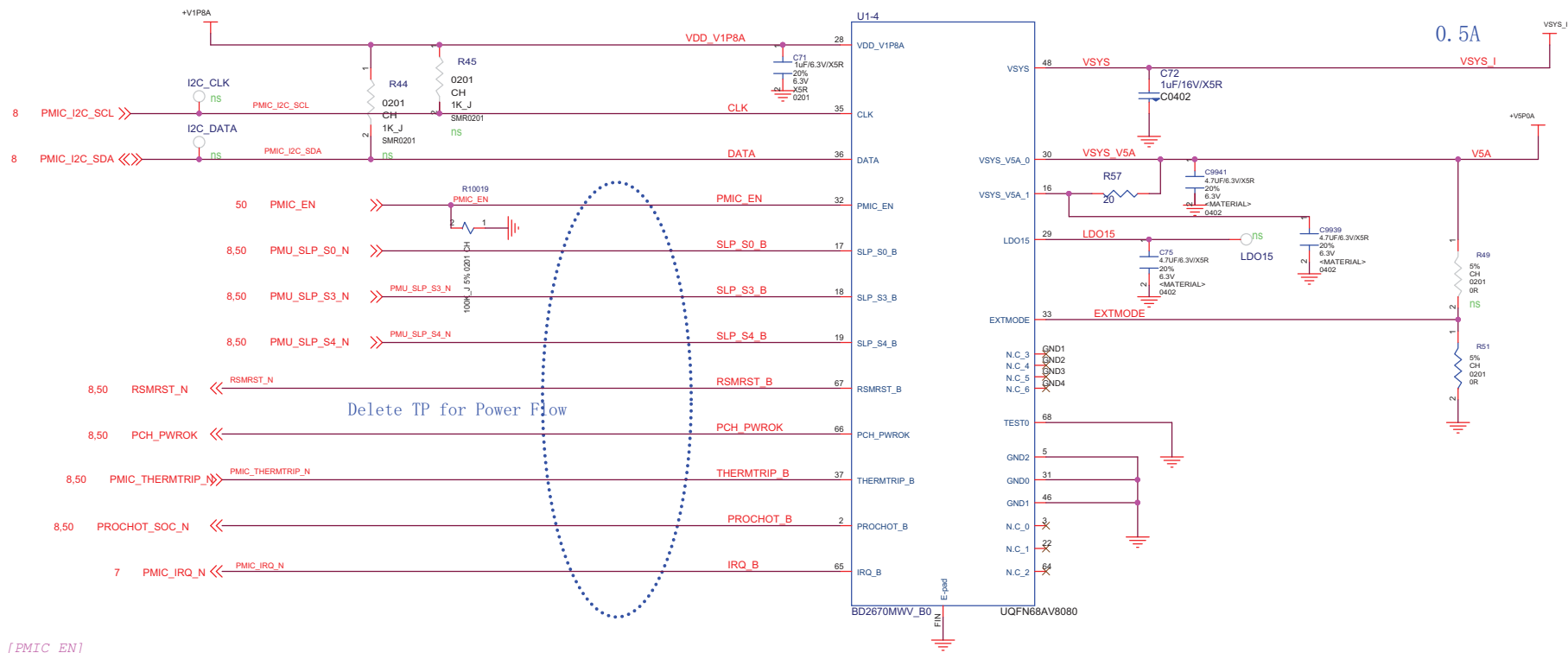


V1P8A[BUCK4], V1P24A[BUCK5], VDDQ[BUCK6]



	DDR_SEL[1:0] = (L,L) (for LPDDR3)	DDR_SEL[1:0] = (L,H) (for DDR3L)	DDR_SEL[1:0] = (H,L) (for LPDDR4)	DDR_SEL[1:0] = (H,L) (for LPDDR4)
GATE1	Sequence Control	SLP_S3 B Control	Sequence Control	SLP_S3 B Control
VDDQ	1.2V	1.35V	1.1V	1.1V

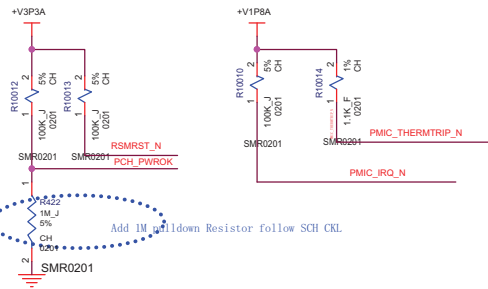
I2C , Other signals




[PMIC_EN]
Connected to EC.

[PCH_PWROK, RSMRST_B, PROCHOT_B, IRQ_B]
These pins are open drain outputs and
need pull-up resistors according to the condition of the connected devices.

[SLP_S0_B, SLP_S3_B, SLP_S4_B, THERMTRIP_B]
Connected to SoC.



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