COMPAL CONFIDENTIAL

MODEL NAME : *QAM00*
PCB NO : *LA-7731P*
BOM P/N : *4319ET31L01*
GPIO MAP:

Dalmore 12 UMA

@ *Ivy Bridge + Panther POINT*

2011-8-30

REV : 0.3 (X01)

@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
M/B SPI ROM		5@
TAA SPI ROM		6@
SATA re-driver with CD function		7@
Normal E-SATA re-driver		8@

MB PCB

Part Number	Description
DA60000P700	PCB 0FH LA-7731P REV0 M/B UMA

@HDMI Royalty

Part Number	Description
RO0000002HM	HDMI Royalty

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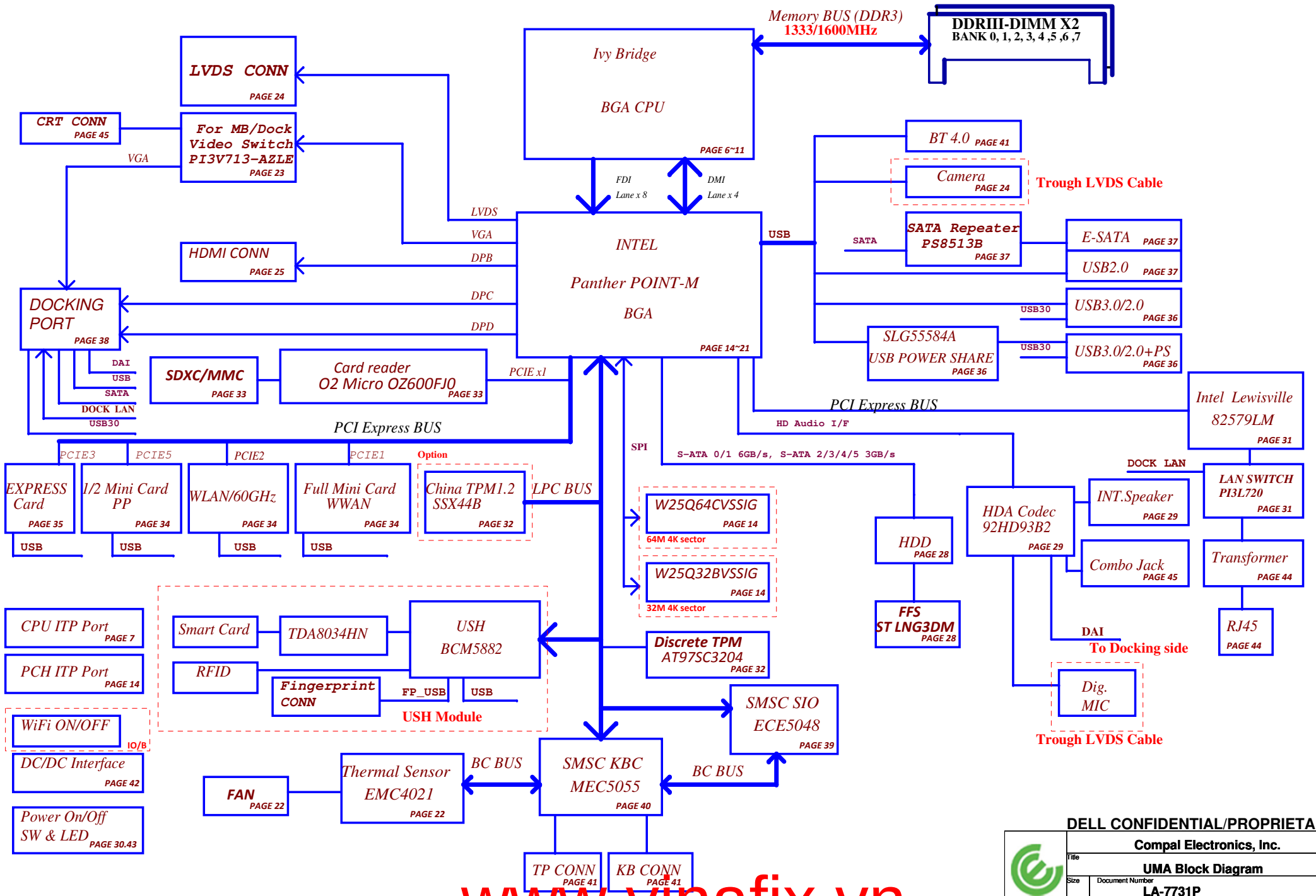
Title	Cover Sheet	
Size	Document Number: LA-7731P	Rev: 0.3
Date: Thursday, September 01, 2011	Sheet 1 of 59	

Block Diagram



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Title: UMA Block Diagram

Size | Document Number: LA-7731P | Rev: 0.3

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

SATA	DESTINATION
SATA 0	HDD
SATA 1	NA
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Right side)
	1	JUSB2 (Bot side)
	2	NA
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(PP)
	7	USH->BIO
	8	DOCKING
	9	JESATA1 (Left)
	10	Express card
	11	Bluetooth
	12	Camera
	13	NA

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	None
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Sig 1		Copper foil	1oz	1.35
		4.7	Prepreg	7628HRC+2116HRCx2+7628HRC	23.60
4	Sig 2		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	GND/PWR		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)			47.6		46.32000

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

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Title: Index and Config.

Size: | Document Number: LA-7731P | Rev: 0.3

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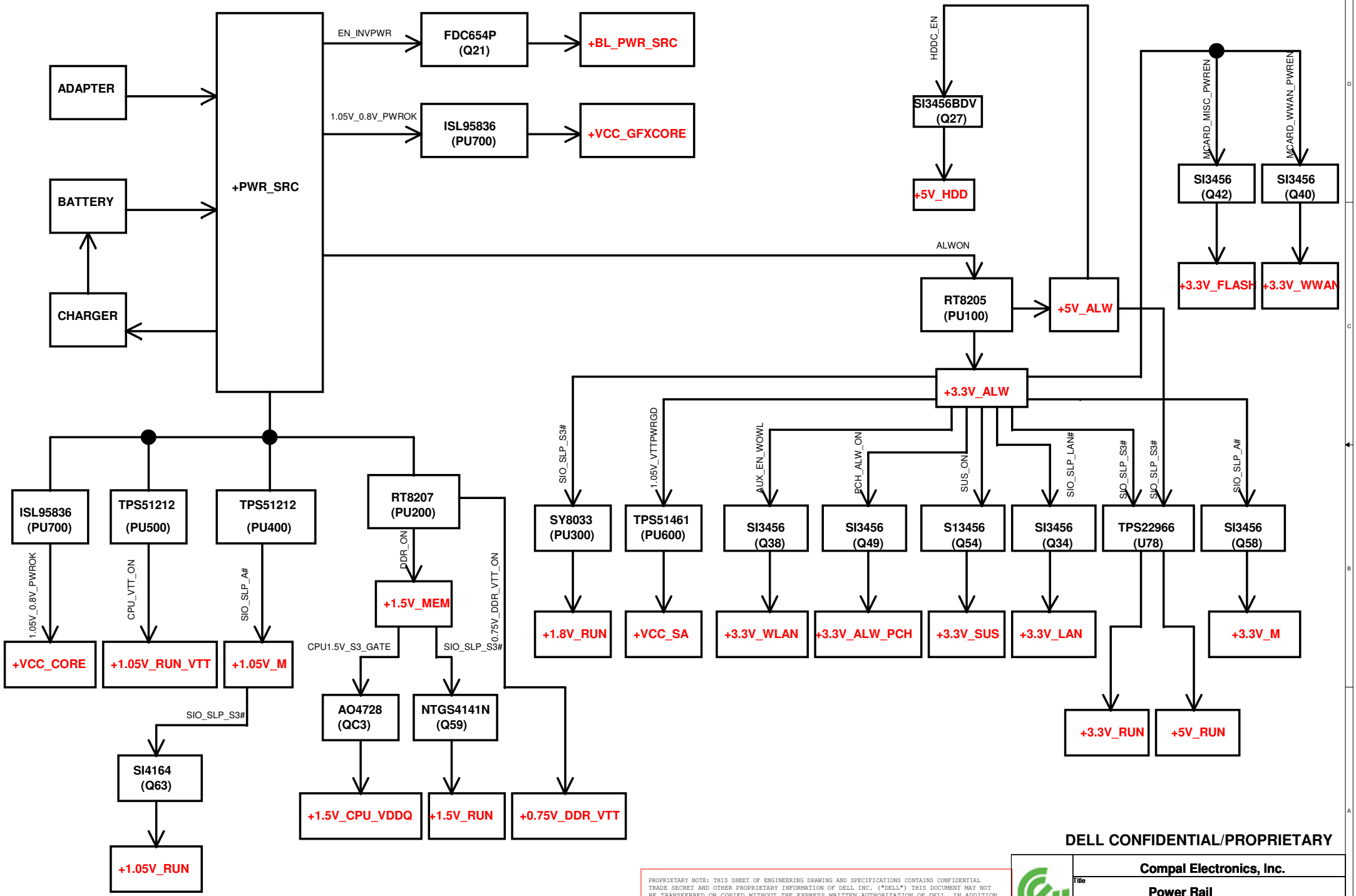

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Title	Power Rail
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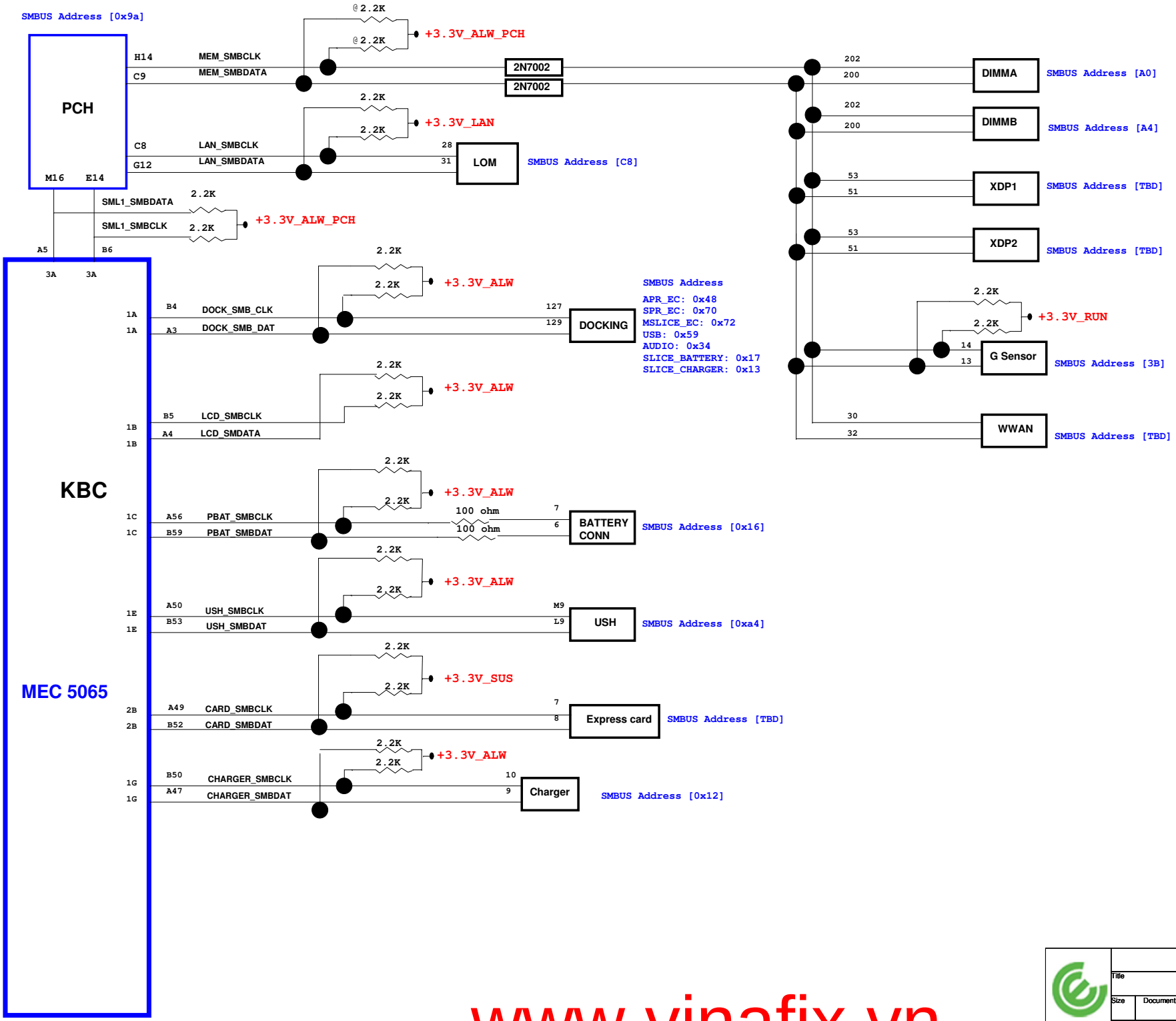

Compal Electronics, Inc.	
Title	SMBUS TOPOLOGY
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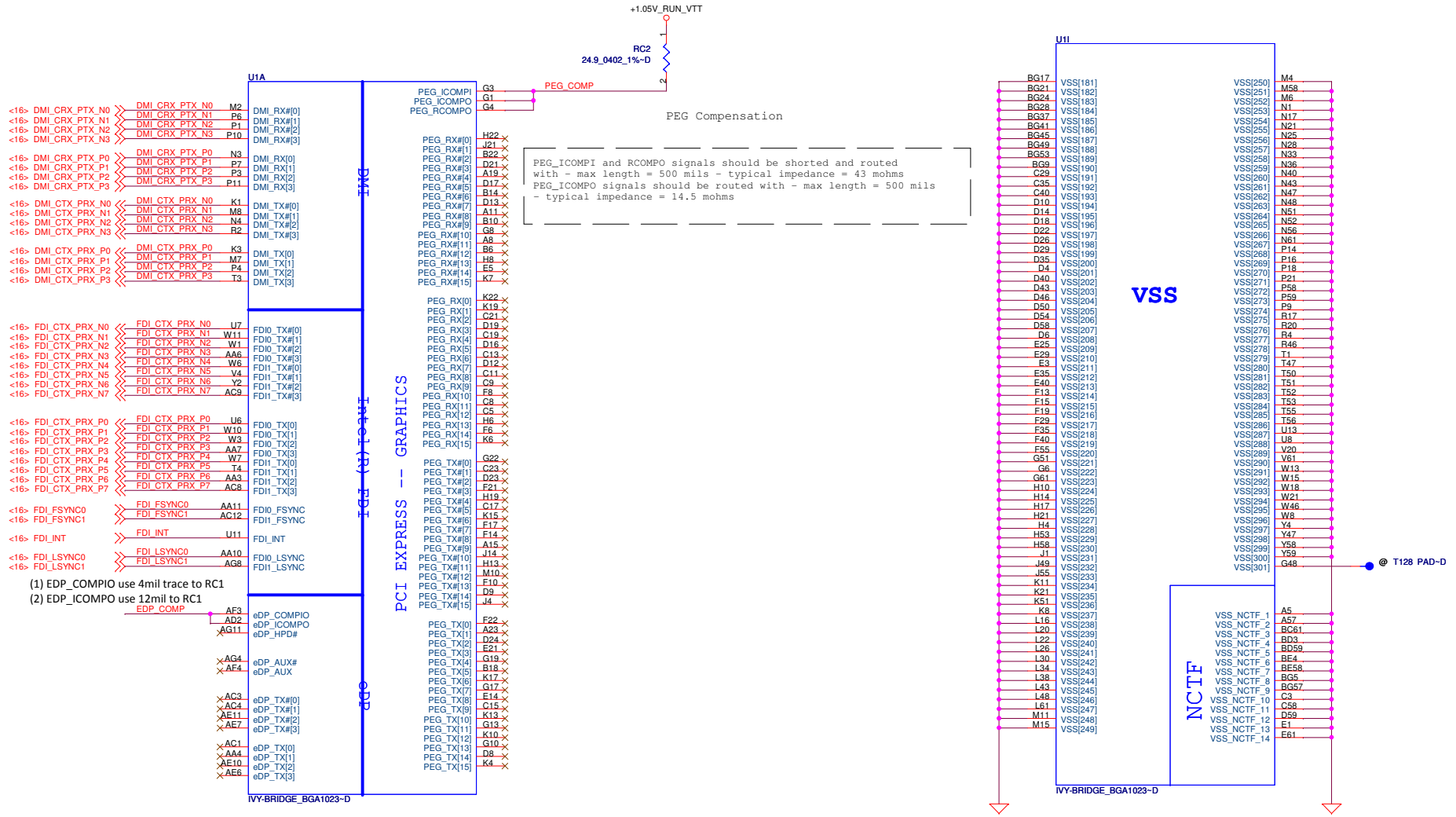
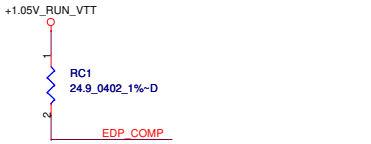
(1)PEG_RCOMPO (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2)PEG_ICOMPO use 12mil connect to RC2



eDP Compensation



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Title	Sandy Bridge (1/6)
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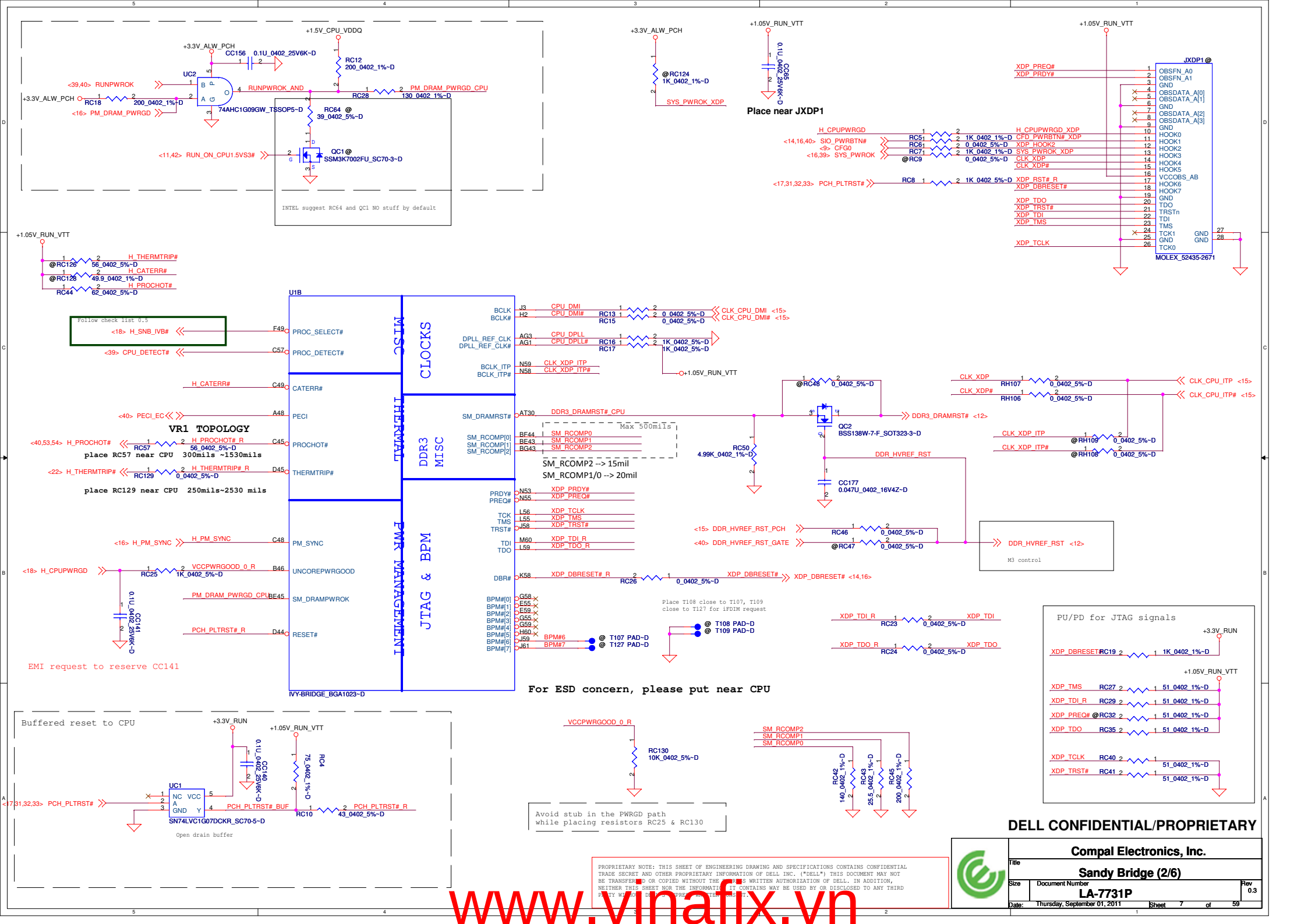
+1.5V_CPU_VDDQ
+3.3V_ALW_PCH
CC156 0.1U_0402_25V6K~D
UC2
74AHC1G09GW_TSSOP5~D
RC12 200_0402_1%~D
RC28 130_0402_1%~D
RC18 200_0402_1%~D
RC64 @ 39_0402_5%~D
QC1@ SSM3K7002FU_SC70-3~D
RUNPWROK_AND
PM_DRAM_PWRGD_CPU
<39,40> RUNPWROK
<16> PM_DRAM_PWRGD
<11,42> RUN_ON_CPU1.5VS3#
INTEL suggest RC64 and QC1 NO stuff by default
+3.3V_ALW_PCH
@RC124 1K_0402_1%~D
SYS_PWROK_XDP
+1.05V_RUN_VTT
CC65 0.1U_0402_25V6K~D
Place near JXDP1
JXDP1@
MOLEX_52435-2671
H_CPUPWRGD
SIO_PWRBTN#
CFG0
SYS_PWROK
RC51 1K_0402_1%~D
RC61 0_0402_5%~D
RC71 1K_0402_1%~D
@RC9 0_0402_5%~D
RC8 1K_0402_5%~D
PCH_PLTRST#
XDP_PREQ#
XDP_PRDY#
XDP_TCLK
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_RST#_R
XDP_DBRESET#
H_CPUPWRGD_XDP
CFD_PWRBTN#_XDP
XDP_HOOK2
SYS_PWROK_XDP
CLK_XDP
CLK_XDP#
+1.05V_RUN_VTT
@RC126 56_0402_5%~D
@RC128 49.9_0402_1%~D
RC44 62_0402_5%~D
H_THERMTRIP#
H_CATERR#
H_PROCHOT#
U1B
IVY-BRIDGE_BGA1023~D
MISC
CLOCKS
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT
THERMAL
PROC_SELECT#
PROC_DETECT#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
BCLK_ITP
BCLK_ITP#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
CPU_DMI
CPU_DMI#
CPU_DPLL
CPU_DPLL#
CLK_XDP_ITP
CLK_XDP_ITP#
DDR3_DRAMRST#_CPU
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
XDP_PRDY#
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI_R
XDP_TDO_R
XDP_DBRESET#_R
BPM#6
BPM#7
RC13 0_0402_5%~D
RC15 0_0402_5%~D
RC16 1K_0402_5%~D
RC17 1K_0402_5%~D
CLK_CPU_DMI <15>
CLK_CPU_DMI# <15>
+1.05V_RUN_VTT
Max 500mils
SM_RCOMP2 --> 15mil
SM_RCOMP1/0 --> 20mil
RC50 4.99K_0402_1%~D
@RC48 0_0402_5%~D
QC2 BSS138W-7-F_SOT323-3~D
DDR3_DRAMRST# <12>
DDR_HVREF_RST
CC177 0.047U_0402_16V4Z~D
CLK_XDP
CLK_XDP#
RH107 0_0402_5%~D
RH106 0_0402_5%~D
CLK_CPU_ITP <15>
CLK_CPU_ITP# <15>
CLK_XDP_ITP
CLK_XDP_ITP#
@RH109 0_0402_5%~D
@RH108 0_0402_5%~D
<15> DDR_HVREF_RST_PCH
<40> DDR_HVREF_RST_GATE
RC46 0_0402_5%~D
@RC47 0_0402_5%~D
DDR_HVREF_RST <12>
M3 control
XDP_DBRESET# <14,16>
RC26 0_0402_5%~D
Place T108 close to T107, T109 close to T127 for iFDIM request
@ T108 PAD~D
@ T109 PAD~D
@ T107 PAD~D
@ T127 PAD~D
XDP_TDI_R RC23 0_0402_5%~D XDP_TDI
XDP_TDO_R RC24 0_0402_5%~D XDP_TDO
PU/PD for JTAG signals
+3.3V_RUN
+1.05V_RUN_VTT
XDP_DBRESET# RC19 1K_0402_1%~D
XDP_TMS RC27 51_0402_1%~D
XDP_TDI_R RC29 51_0402_1%~D
XDP_PREQ# @RC32 51_0402_1%~D
XDP_TDO RC35 51_0402_1%~D
XDP_TCLK RC40 51_0402_1%~D
XDP_TRST# RC41 51_0402_1%~D
VR1 TOPOLOGY
place RC57 near CPU 300mils ~1530mils
place RC129 near CPU 250mils~2530 mils
<40,53,54> H_PROCHOT#
RC57 56_0402_5%~D
H_PROCHOT#_R
<22> H_THERMTRIP#
RC129 0_0402_5%~D
H_THERMTRIP#_R
<16> H_PM_SYNC
H_PM_SYNC
<18> H_CPUPWRGD
RC25 1K_0402_5%~D
VCCPWRGOOD_0_R
PM_DRAM_PWRGD_CPU
PCH_PLTRST#_R
CC141 0.1U_0402_25V6K~D
EMI request to reserve CC141
Follow check list 0.5
<18> H_SNB_IVB#
<39> CPU_DETECT#
F49
C57
C49
A48
C45
D45
C48
B46
BE45
D44
For ESD concern, please put near CPU
Buffered reset to CPU
+3.3V_RUN
+1.05V_RUN_VTT
UC1
SN74LVC1G07DCKR_SC70-5~D
Open drain buffer
CC140 0.1U_0402_25V6K~D
RC4 75_0402_1%~D
RC10 43_0402_5%~D
PCH_PLTRST#_BUF
<17,31,32,33> PCH_PLTRST#
PCH_PLTRST#_R
VCCPWRGOOD_0_R
RC130 10K_0402_5%~D
Avoid stub in the PWRGD path while placing resistors RC25 & RC130
SM_RCOMP2
SM_RCOMP1
SM_RCOMP0
RC42 140_0402_1%~D
RC43 25.5_0402_1%~D
RC45 200_0402_1%~D
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Title
Sandy Bridge (2/6)
Size
Document Number
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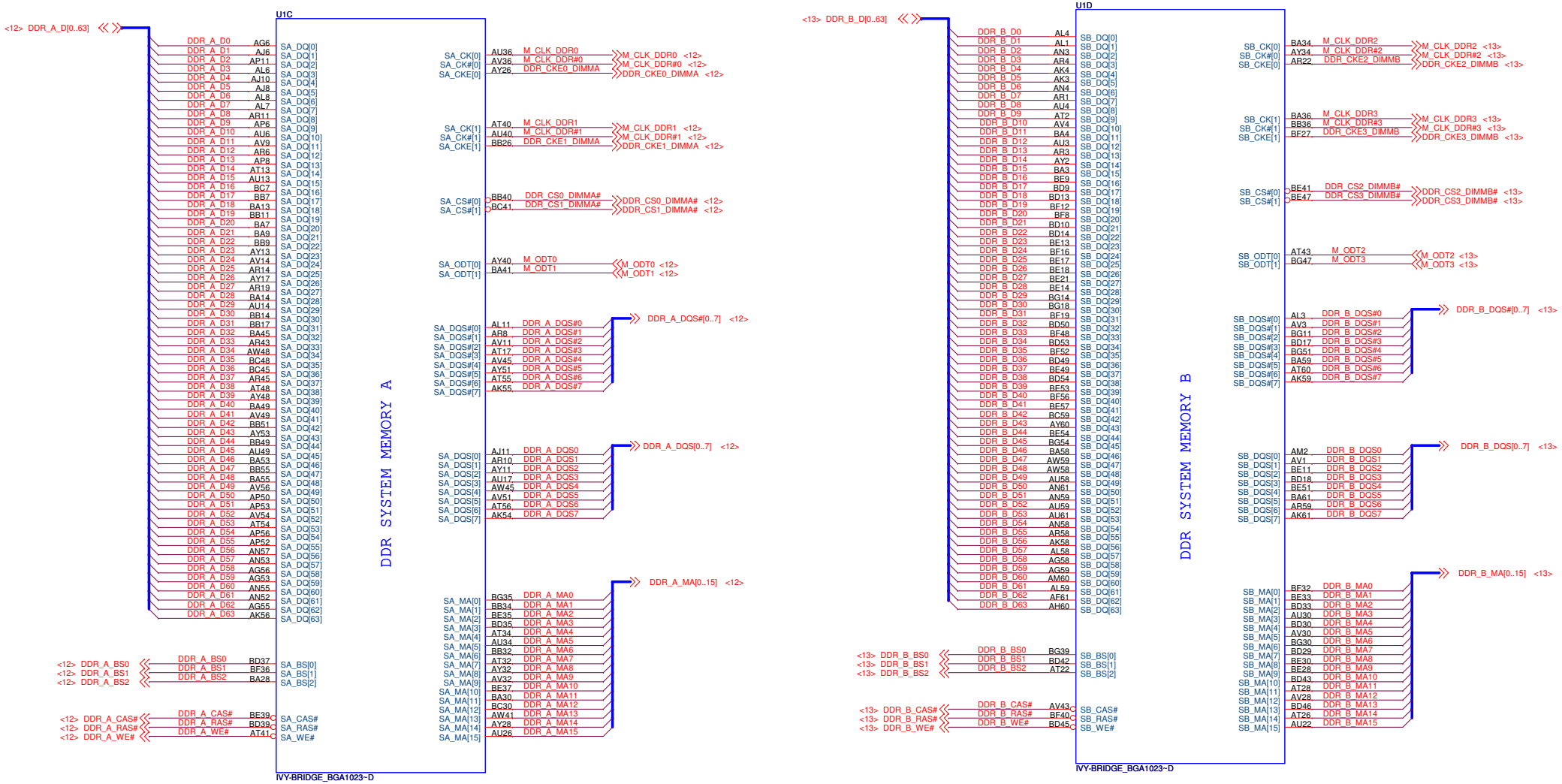

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Title: Sandy Bridge (3/6)

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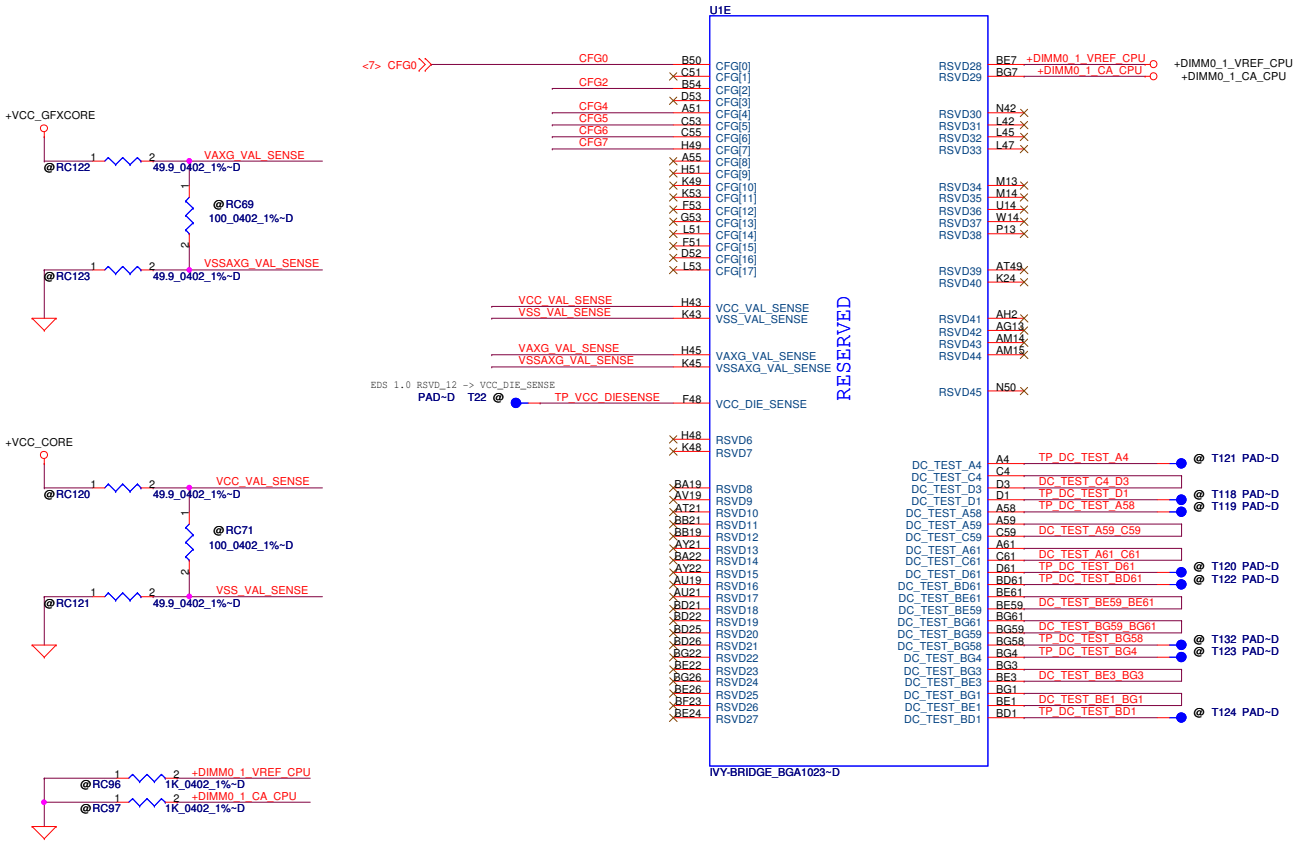
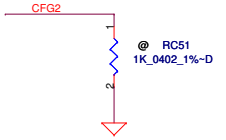
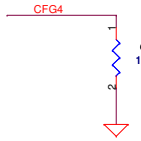
CFG Straps for Processor

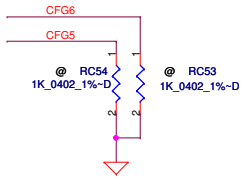




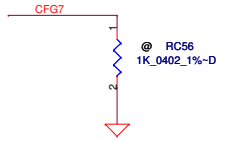
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: Sandy Bridge (4/6)
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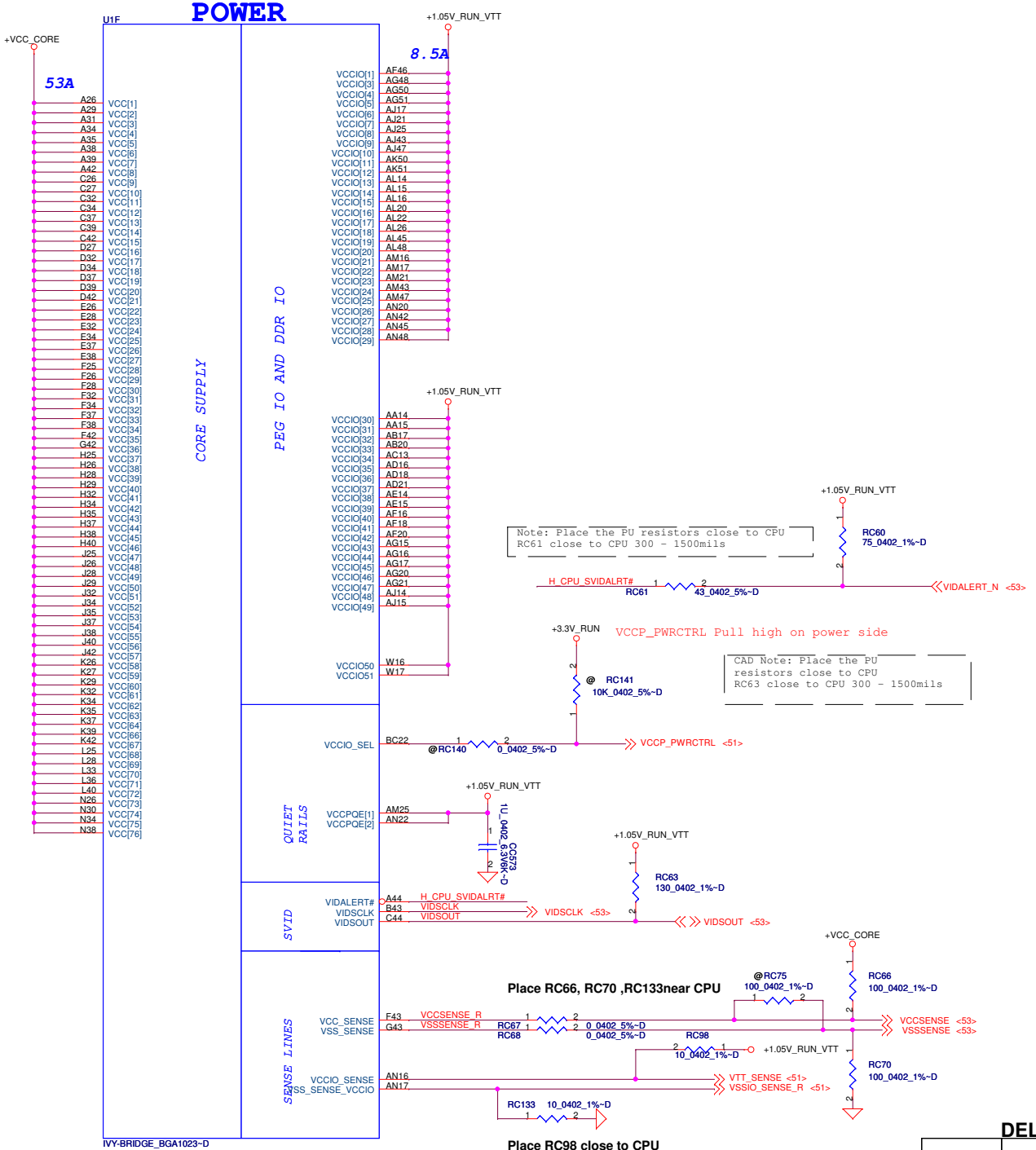
POWER



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

Compal Electronics, Inc.

Title: Sandy Bridge (5/6)

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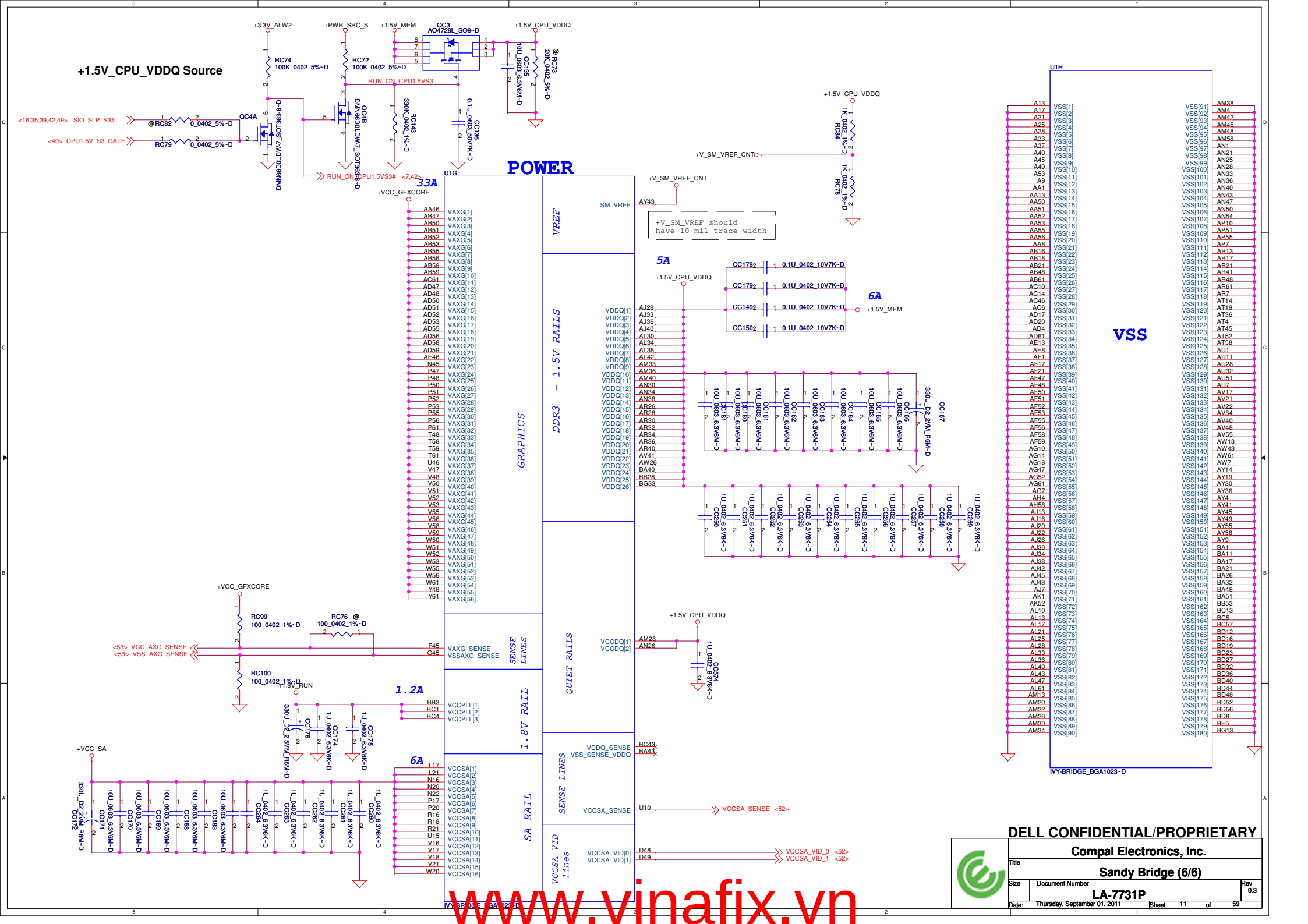
+1.5V_CPU_VDDQ Source
POWER
VSS
GRAPHICS
DDR3 - 1.5V RAILS
VREF
SENSE LINES
QUIET RAILS
1.8V RAIL
SA RAIL
VCCSA VID lines
+V_SM_VREF should have 10 mil trace width
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H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

CONN@

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Title	DDRIII-SODIMM SLOT1
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H=4mm

2-3A to 1 DIMMs/channel

JDIMMB Reverse Type

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2.203,204

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

JDIMM2

TYCO_2-2013287-1

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

INTEL HDA_SYNC isolation circuit

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs

CMOS place near DIMM

CH6 close to JXDP2

CH1 close to JXDP2

No Reboot Strap
SPKR: Low = Default; High = No Reboot

BBS_BIT0 - BIOS BOOT STRAP BIT 0

200 MIL SO8
64Mb Flash ROM
W25Q64CVSSIG_SO8~D

200 MIL SO8
32Mb Flash ROM
W25Q32BVSSIG_SO8~D

ACES_50169-01441-002
CONN@

Compal Electronics, Inc.		
Title: PCH (1/8)		
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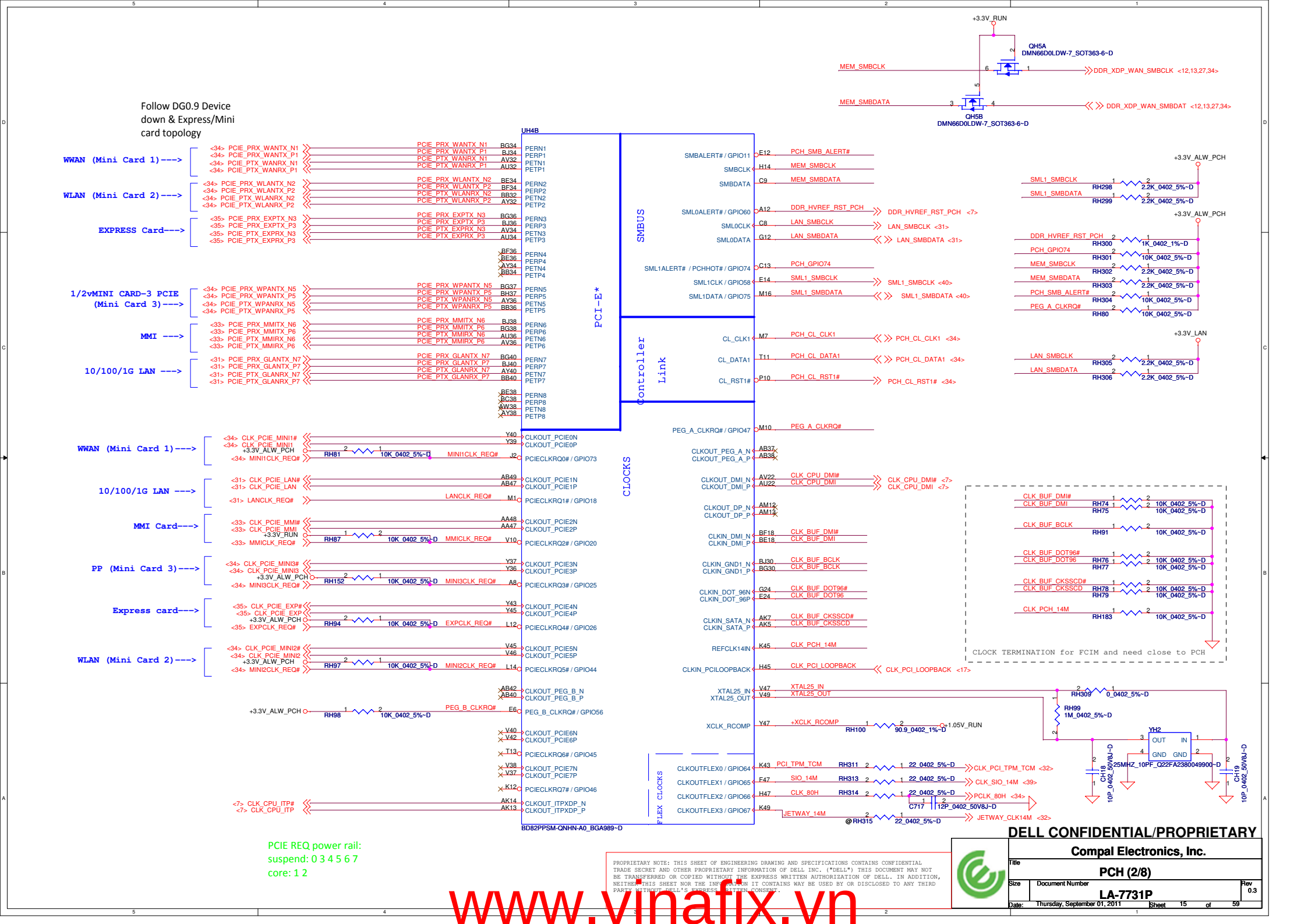
Follow DG0.9 Device down & Express/Mini card topology
UH4B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
BD82PPSM-QNHN-A0_BGA989~D
WWAN (Mini Card 1)--->
WLAN (Mini Card 2)--->
EXPRESS Card--->
1/2vMINI CARD-3 PCIE (Mini Card 3)--->
MMI --->
10/100/1G LAN --->
PP (Mini Card 3)--->
Express card--->
PCIE_PRX_WANTX_N1
PCIE_PRX_WANTX_P1
PCIE_PTX_WANRX_N1
PCIE_PTX_WANRX_P1
PCIE_PRX_WLANTX_N2
PCIE_PRX_WLANTX_P2
PCIE_PTX_WLANRX_N2
PCIE_PTX_WLANRX_P2
PCIE_PRX_EXPTX_N3
PCIE_PRX_EXPTX_P3
PCIE_PTX_EXPRX_N3
PCIE_PTX_EXPRX_P3
PCIE_PRX_WPANTX_N5
PCIE_PRX_WPANTX_P5
PCIE_PTX_WPANRX_N5
PCIE_PTX_WPANRX_P5
PCIE_PRX_MMITX_N6
PCIE_PRX_MMITX_P6
PCIE_PTX_MMIRX_N6
PCIE_PTX_MMIRX_P6
PCIE_PRX_GLANTX_N7
PCIE_PRX_GLANTX_P7
PCIE_PTX_GLANRX_N7
PCIE_PTX_GLANRX_P7
CLK_PCIE_MINI1#
CLK_PCIE_MINI1
CLK_PCIE_LAN#
CLK_PCIE_LAN
CLK_PCIE_MMI#
CLK_PCIE_MMI
CLK_PCIE_MINI3#
CLK_PCIE_MINI3
CLK_PCIE_EXP#
CLK_PCIE_EXP
CLK_PCIE_MINI2#
CLK_PCIE_MINI2
MINI1CLK_REQ#
LANCLK_REQ#
MMICLK_REQ#
MINI3CLK_REQ#
EXPCLK_REQ#
MINI2CLK_REQ#
PEG_B_CLKRQ#
CLK_CPU_ITP#
CLK_CPU_ITP
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / PCHHOT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67
PCH_SMB_ALERT#
MEM_SMBCLK
MEM_SMBDATA
DDR_HVREF_RST_PCH
LAN_SMBCLK
LAN_SMBDATA
PCH_GPIO74
SML1_SMBCLK
SML1_SMBDATA
PCH_CL_CLK1
PCH_CL_DATA1
PCH_CL_RST1#
CLK_CPU_DMI#
CLK_CPU_DMI
CLK_BUF_DMI#
CLK_BUF_DMI
CLK_BUF_BCLK
CLK_BUF_DOT96#
CLK_BUF_DOT96
CLK_BUF_CKSSCD#
CLK_BUF_CKSSCD
CLK_PCH_14M
CLK_PCI_LOOPBACK
+XCLK_RCOMP
PCI_TPM_TCM
SIO_14M
CLK_80H
JETWAY_14M
QH5A DMN66D0LDW-7_SOT363-6~D
QH5B DMN66D0LDW-7_SOT363-6~D
MEM_SMBCLK
MEM_SMBDATA
DDR_XDP_WAN_SMBCLK <12,13,27,34>
DDR_XDP_WAN_SMBDAT <12,13,27,34>
+3.3V_RUN
+3.3V_ALW_PCH
+1.05V_RUN
CLOCK TERMINATION for FCIM and need close to PCH
YH2 25MHZ_10PF_Q22FA2380049900~D
PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2
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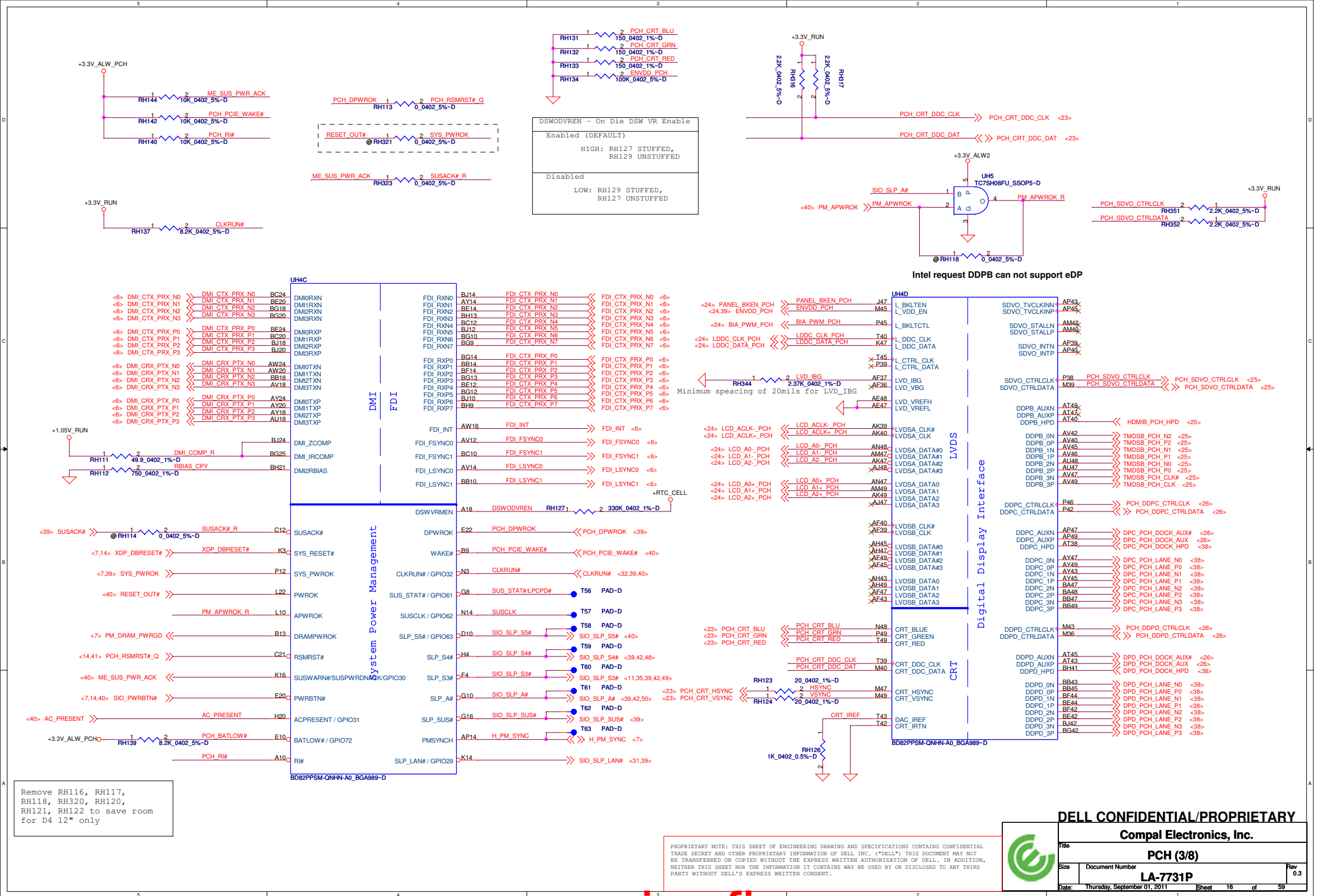

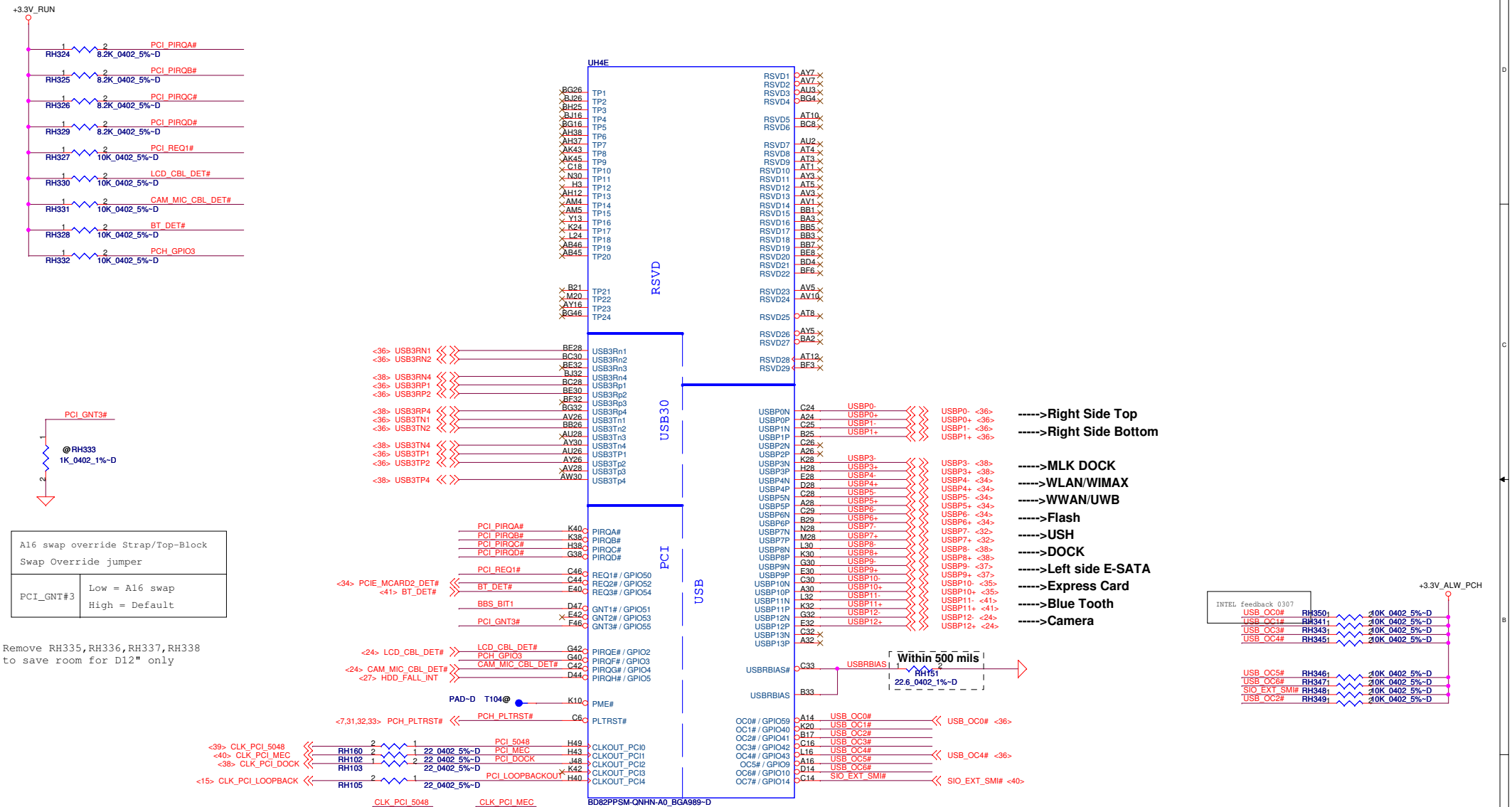

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+3.3V_ALW_PCH
RH53 4.7K_0402_5%~D
SLP_ME_CSW_DEV#

Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT DISABLED - LOW

+3.3V_ALW_PCH
SIO_EXT_WAKE# RH177 10K_0402_5%~D
PCH_GPIO15 RH354 1K_0402_1%~D

INTEL feedback 0302
PCH_GPIO36 RH174 10K_0402_5%~D
PCH_GPIO37 RH172 10K_0402_5%~D
DBC_ENABLE RH273 10K_0402_5%~D

+3.3V_ALW_PCH
KB_DET# RH170 10K_0402_5%~D

+3.3V_RUN
PCH_GPIO36 @RH171 10K_0402_5%~D
PCH_GPIO37 @RH173 1K_0402_1%~D
ESATA_CD# RH175 10K_0402_5%~D
TEMP_ALERT# RH266 10K_0402_5%~D
PCH_GPIO22 RH181 10K_0402_5%~D
PCH_GPIO7 RH178 10K_0402_5%~D
DBC_ENABLE @RH269 8.2K_0402_5%~D
PCH_GPIO6 RH163 10K_0402_5%~D

UH4F

<40> SIO_EXT_SCI#	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40	CONTACTLESS_DET# <32>
<32> USH_DET#	A42	TACH1 / GPIO1	TACH5 / GPIO69	B41	PCH_GPIO69
PCH_GPIO6	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41	PCIE_MCARD3_DET# <34>
PCH_GPIO7	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40	USB_MCARD2_DET# <34>
<39> SIO_EXT_WAKE#	C10	GPIO8			
<31> PM_LANPHY_ENABLE	C4	LAN_PHY_PWR_CTRL / GPIO12			
PCH_GPIO15	G2	GPIO15	A20GATE	P4	SIO_A20GATE <40>
<37> ESATA_CD#	U2	SATA4GP / GPIO16	PECI	AU16	
			RCIN#	P5	SIO_RCIN# <40>
<24> DBC_ENABLE	D40	TACH0 / GPIO17	PROCPWRGD	AY11	H_CPUPWRGD <7>
PCH_GPIO22	T5	SCLOCK / GPIO22	THRMTRIP#	AY10	PCH_THRMTRIP# R
<34> PCIE_MCARD1_DET#	E8	GPIO24	INIT3_3V#	T14	
<35> EXPRCRD_DET#	E16	GPIO27	DF_TVS	AY1	DF_TVS
<39> SLP_ME_CSW_DEV#	P8	GPIO28	TS_VSS1	AH8	
	K1	STP_PCI# / GPIO34	TS_VSS2	AK11	
<34> USB_MCARD1_DET#	K4	GPIO35	TS_VSS3	AH10	
PCH_GPIO36	V8	SATA2GP / GPIO36	TS_VSS4	AK10	
PCH_GPIO37	M5	SATA3GP / GPIO37	NC_1	P37	
TPM_ID0	N2	SLOAD / GPIO38			
TPM_ID1	M3	SDATAOUT0 / GPIO39			
<27> FFS_INT2	V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2	VSS_NCTF_15
<39> TEMP_ALERT#	V3	SATA5GP / GPIO49 / TEMP_ALERT#	VSS_NCTF_16	BG48	VSS_NCTF_16
<41> KB_DET#	D6	GPIO57	VSS_NCTF_17	BH3	VSS_NCTF_17
			VSS_NCTF_18	BH47	VSS_NCTF_18
VSS_NCTF_1	A4	VSS_NCTF_1	VSS_NCTF_19	BJ4	VSS_NCTF_19
VSS_NCTF_2	A44	VSS_NCTF_2	VSS_NCTF_20	BJ44	VSS_NCTF_20
VSS_NCTF_3	A45	VSS_NCTF_3	VSS_NCTF_21	BJ45	VSS_NCTF_21
VSS_NCTF_4	A46	VSS_NCTF_4	VSS_NCTF_22	BJ46	VSS_NCTF_22
VSS_NCTF_5	A5	VSS_NCTF_5	VSS_NCTF_23	BJ5	VSS_NCTF_23
VSS_NCTF_6	A6	VSS_NCTF_6	VSS_NCTF_24	BJ6	VSS_NCTF_24
VSS_NCTF_7	B3	VSS_NCTF_7	VSS_NCTF_25	C2	VSS_NCTF_25
VSS_NCTF_8	B47	VSS_NCTF_8	VSS_NCTF_26	C48	VSS_NCTF_26
VSS_NCTF_9	BD1	VSS_NCTF_9	VSS_NCTF_27	D1	VSS_NCTF_27
VSS_NCTF_10	BD49	VSS_NCTF_10	VSS_NCTF_28	D49	VSS_NCTF_28
VSS_NCTF_11	BE1	VSS_NCTF_11	VSS_NCTF_29	E1	VSS_NCTF_29
VSS_NCTF_12	BE49	VSS_NCTF_12	VSS_NCTF_30	E49	VSS_NCTF_30
VSS_NCTF_13	BF1	VSS_NCTF_13	VSS_NCTF_31	F1	VSS_NCTF_31
VSS_NCTF_14	BF49	VSS_NCTF_14	VSS_NCTF_32	F49	VSS_NCTF_32

BD82PPSM-QNHN-A0_BGA989~D

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

+3.3V_RUN
CONTACTLESS_DET# RH256 10K_0402_5%~D
PCH_GPIO69 RH260 1.5K_0402_1%~D

+1.05V_RUN_VTT
RH262 56_0402_5%~D
CH97 0.1U_0402_25V6K~D

+3.3V_RUN
SIO_A20GATE RH158 10K_0402_5%~D
SIO_RCIN# RH203 10K_0402_5%~D
SIO_EXT_SCI# RH263 10K_0402_5%~D
USH_DET# RH164 100K_0402_5%~D

Due to remove VCCDFERM jumper(PJP66), need to change the power rail to +1.8V_RUN for D12" only

PLACE RH150 CLOSE TO THE BRANCHING POINT (TO CPU and NVRAM CONNECTOR)

+1.8V_RUN
RH149 need to close to CPU
RH149 2.2K_0402_5%~D
<7> H_SNB_IVB# RH150 0_0402_5%~D
DF_TVS_R RH358 1K_0402_1%~D
DF_TVS

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

+3.3V_RUN
RH267 10K_0402_5%~D
TPM_ID0
@RH270 10K_0402_5%~D

+3.3V_RUN
RH268 20K_0402_5%~D
TPM_ID1
@RH271 2.2K_0402_5%~D

	TPM_ID0	TPM_ID1
USH2.0	1	1

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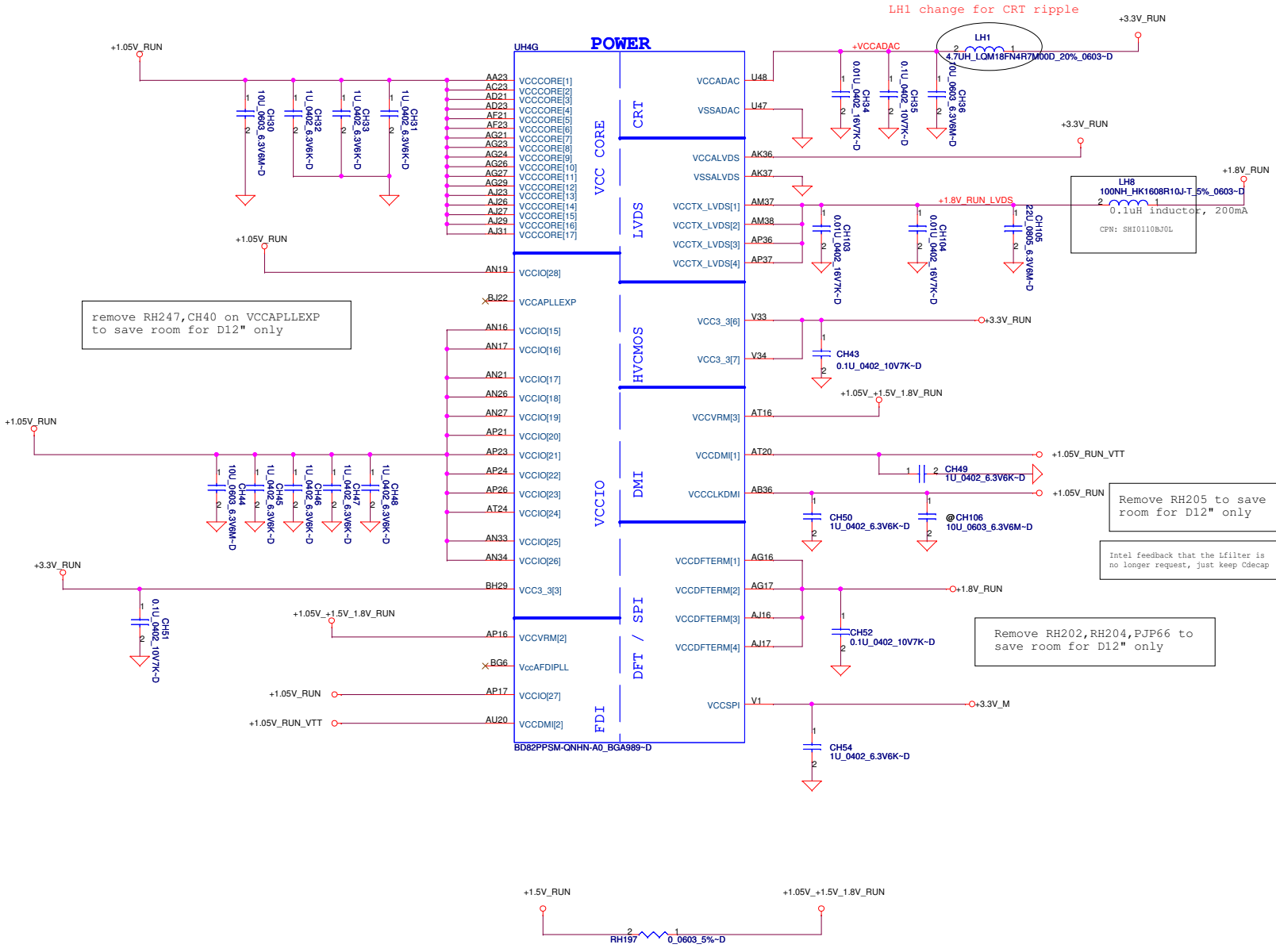

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VCCDFTERM	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLLEXP	1.05	0.05

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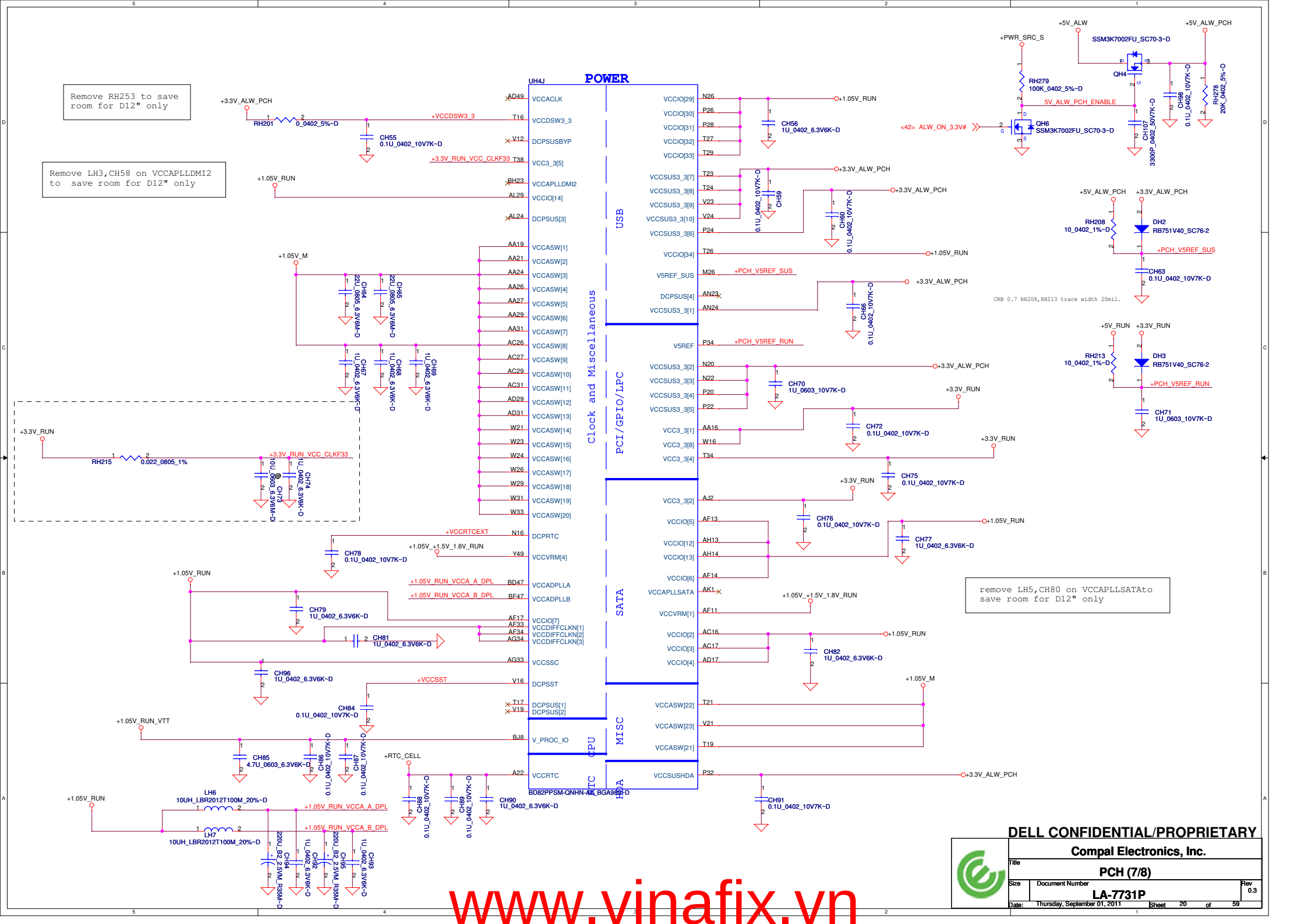
POWER
UH4J
Remove RH253 to save room for D12" only
Remove LH3,CH58 on VCCAPLLDMI2 to save room for D12" only
remove LH5,CH80 on VCCAPLLSATAto save room for D12" only
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
HDA
VCCACLK
VCCDSW3_3
DCPSUSBYP
VCC3_3[5]
VCCAPLLDMI2
VCCIO[14]
DCPSUS[3]
VCCASW[1]
VCCASW[2]
VCCASW[3]
VCCASW[4]
VCCASW[5]
VCCASW[6]
VCCASW[7]
VCCASW[8]
VCCASW[9]
VCCASW[10]
VCCASW[11]
VCCASW[12]
VCCASW[13]
VCCASW[14]
VCCASW[15]
VCCASW[16]
VCCASW[17]
VCCASW[18]
VCCASW[19]
VCCASW[20]
DCPRTC
VCCVRM[4]
VCCADPLLA
VCCADPLLB
VCCIO[7]
VCCDIFFCLKN[1]
VCCDIFFCLKN[2]
VCCDIFFCLKN[3]
VCCSSC
DCPSST
DCPSUS[1]
DCPSUS[2]
V_PROC_IO
VCCRTC
BD82PPSM-QNHN-A0_BGA989-D
VCCIO[29]
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
VCCSUS3_3[7]
VCCSUS3_3[8]
VCCSUS3_3[9]
VCCSUS3_3[10]
VCCSUS3_3[6]
VCCIO[34]
V5REF_SUS
DCPSUS[4]
VCCSUS3_3[1]
V5REF
VCCSUS3_3[2]
VCCSUS3_3[3]
VCCSUS3_3[4]
VCCSUS3_3[5]
VCC3_3[1]
VCC3_3[8]
VCC3_3[4]
VCC3_3[2]
VCCIO[5]
VCCIO[12]
VCCIO[13]
VCCIO[6]
VCCAPLLSATA
VCCVRM[1]
VCCIO[2]
VCCIO[3]
VCCIO[4]
VCCASW[22]
VCCASW[23]
VCCASW[21]
VCCSUSHDA
+3.3V_ALW_PCH
+1.05V_RUN
+3.3V_RUN
+1.05V_M
+5V_ALW
+5V_ALW_PCH
+PWR_SRC_S
SSM3K7002FU_SC70-3~D
QH4
QH6
RH279 100K_0402_5%~D
5V_ALW_PCH_ENABLE
<42> ALW_ON_3.3V#
RH208 10_0402_1%~D
DH2 RB751V40_SC76-2
+PCH_V5REF_SUS
RH213 10_0402_1%~D
DH3 RB751V40_SC76-2
+PCH_V5REF_RUN
CRB 0.7 RH208,RH213 trace width 20mil.
RH201 0_0402_5%~D
RH215 0.022_0805_1%
+VCCDSW3_3
+3.3V_RUN_VCC_CLKF33
+VCCRTCEXT
+1.05V_+1.5V_1.8V_RUN
+1.05V_RUN_VCCA_A_DPL
+1.05V_RUN_VCCA_B_DPL
+VCCSST
+1.05V_RUN_VTT
+RTC_CELL
LH6 10UH_LBR2012T100M_20%~D
LH7 10UH_LBR2012T100M_20%~D
CH55 0.1U_0402_10V7K~D
CH56 1U_0402_6.3V6K~D
CH57 0.1U_0402_10V7K~D
CH58 0.1U_0402_10V7K~D
CH59 0.1U_0402_10V7K~D
CH60 0.1U_0402_10V7K~D
CH63 0.1U_0402_10V7K~D
CH64 22U_0805_6.3V6M~D
CH65 22U_0805_6.3V6M~D
CH66 0.1U_0402_10V7K~D
CH67 1U_0402_6.3V6K~D
CH68 1U_0402_6.3V6K~D
CH69 1U_0402_6.3V6K~D
CH70 1U_0603_10V7K~D
CH71 1U_0603_10V7K~D
CH72 0.1U_0402_10V7K~D
CH73 10U_0603_6.3V6M~D
CH74 1U_0402_6.3V6K~D
CH75 0.1U_0402_10V7K~D
CH76 0.1U_0402_10V7K~D
CH77 1U_0402_6.3V6K~D
CH78 0.1U_0402_10V7K~D
CH79 1U_0402_6.3V6K~D
CH81 1U_0402_6.3V6K~D
CH82 1U_0402_6.3V6K~D
CH83 1U_0402_6.3V6K~D
CH84 220U_B2_2.5VM_R35M~D
CH85 4.7U_0603_6.3V6K~D
CH86 0.1U_0402_10V7K~D
CH87 0.1U_0402_10V7K~D
CH88 0.1U_0402_10V7K~D
CH89 0.1U_0402_10V7K~D
CH90 1U_0402_6.3V6K~D
CH91 0.1U_0402_10V7K~D
CH96 1U_0402_6.3V6K~D
CH98 0.1U_0402_10V7K~D
CH107 3300P_0402_50V7K~D
RH278 20K_0402_5%~D
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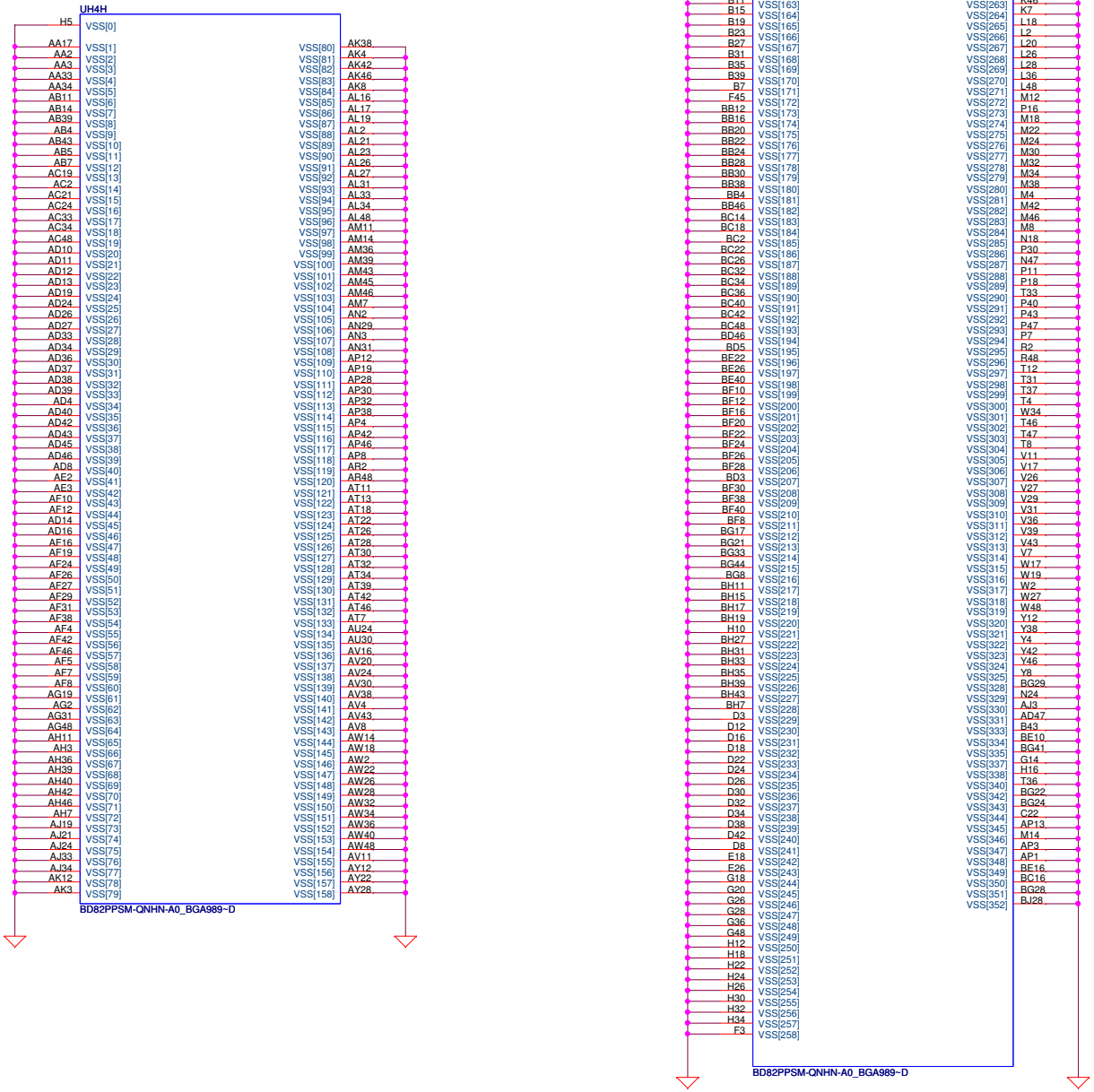

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Place under CPU
Place C266 close to the Q12 as possible

@C266 100P_0402_50V8J~D
Q12 MMBT3904WT1G_SC70-3~D
REM_DIODE1_P_4021
REM_DIODE1_N_4021

(1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.

@C272 100P_0402_50V8J~D
Q14 MMBT3904WT1G_SC70-3~D
100P_0402_50V8J~D
@C277
Q13 MMBT3904WT1G_SC70-3~D
REM_DIODE2_P_4021
REM_DIODE2_N_4021

+FAN1_VOUT
RB751V40_SC76-2 D2
22U_0805_6.3V6M~D C219
FAN1_DET#
FAN1_TACH_FB
JFAN1 CONN@
GND1
GND2
ACES_50271-0040N-001

+3.3V_M
BC_INT#_EMC4021 R385 10K_0402_5%~D
FAN1_TACH_FB R426 10K_0402_5%~D
FAN1_DET# R402 10K_0402_5%~D

+5V_RUN
10U_0805_10V6K~D C276
0.1U_0402_25V6K~D C275
+3.3V_RUN
10U_0603_6.3V6M~D C305
0.1U_0402_25V6K~D C238

Change to EMC4021 for cost saving

place C270/C271 close to U9

+3.3V_M
R389 10K_0402_5%~D VDD_PWRGD
C270 2200P_0402_50V7K~D REM_DIODE1_N_4021 REM_DIODE1_P_4021
C271 2200P_0402_50V7K~D REM_DIODE2_N_4021 REM_DIODE2_P_4021

U9
VDD_H
VDD_H
VDD_L
VDD_PWRGD
DN1/THERM
DP1/VREF_T
DN2/DP4
DP2/DN4
N/C
N/C
VCP
VIN
VSET
TACH/GPIO1
TEST3
GPIO3/PWM/THERMTRIP_SIO
3V_PWROK#
VDD
ADDR_MODE/XEN
TEST1
TEST2
VSS
RTC_PWR3V
EMC4021-1-EZK-TR_QFN32_5X5~D

THERMTRIP2#
N/C
SYS_SHDN#
POWER_SW#
ACAVAIL_CLR
ATF_INT#/BC_IRQ#
FAN_OUT
FAN_OUT
SMCLK/BC_CLK
SMDATA/BC_DATA

<54> MAX8731_IINP
4.7K_0402_5%~D R387 VCP2
VSET_4021

SMSC request
R404 10K_0402_5%~D FAN1_TACH_FB
FAN1_DET#

<40> PCH_PWRGD#
R391 1K_0402_1%~D 3V_PWROK#

+RTC_CELL
1U_0402_2.2V6K~D C274

THERMTRIP2#
THERM_STP# <47>
@R390 47K_0402_1%~D +RTC_CELL
POWER_SW#
ACAV_IN <40,54,55>
BC_INT#_EMC4021 <40>
+FAN1_VOUT
BC_CLK_EMC4021 <40>
BC_DAT_EMC4021 <40>

+VCC_4021
+ADDR_XEN
4.7K_0402_5%~D R393
+VCC_4021

R403 10K_0402_5%~D SMSC request

+3.3V_M
R388 22_0402_5%~D
0.1U_0402_25V6K~D C273
1U_0402_6.3V6K~D C1179

+3.3V_M
R395 8.2K_0402_5%~D
+1.05V_RUN_VTT
R399 2.2K_0402_5%~D
Q16 PMST3904_SOT323-3~D
THERMTRIP2#
<7> H_THERMTRIP#
0.1U_0402_25V6K~D C278

VSET_4021
0.1U_0402_25V6K~D C282
R406 953_0402_1%~D
Rest=953, Tp=88degree

+RTC_CELL
C281 0.1U_0402_25V6K~D
U10 TC7SH08FU_SSOP5~D
POWER_SW#
DOCK_PWR_SW# <40>
POWER_SW_IN# <40>

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.
Title: FAN & Thermal Sensor
Size: Document Number: LA-7731P
Rev: 0.3
Date: Thursday, September 01, 2011
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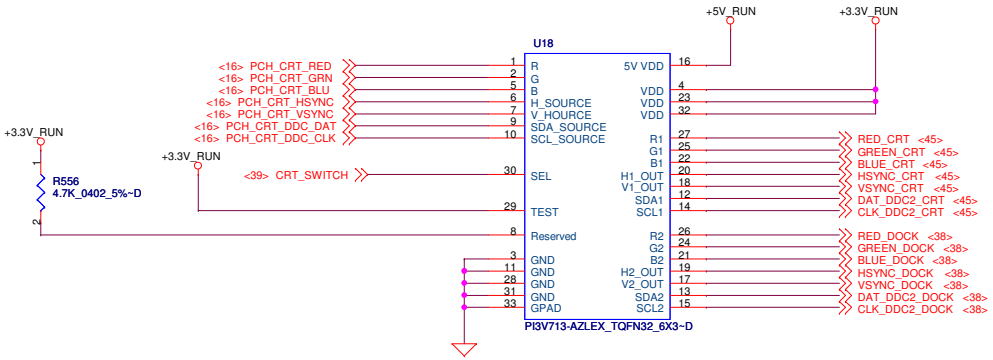
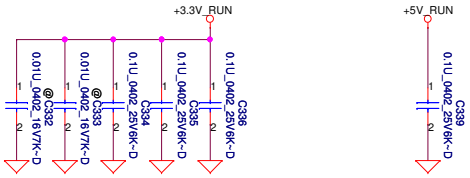
SW for MB/DOCK

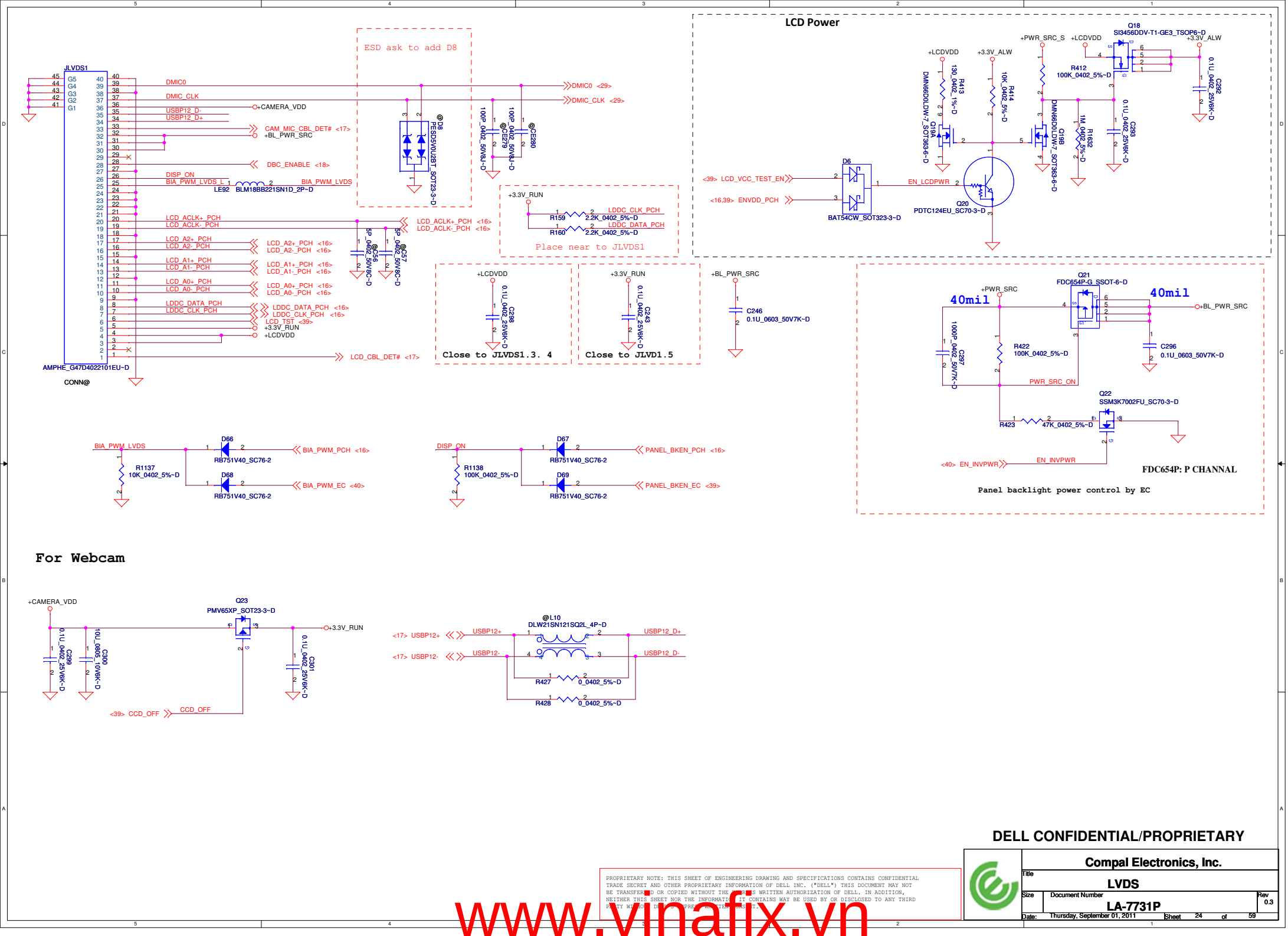


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



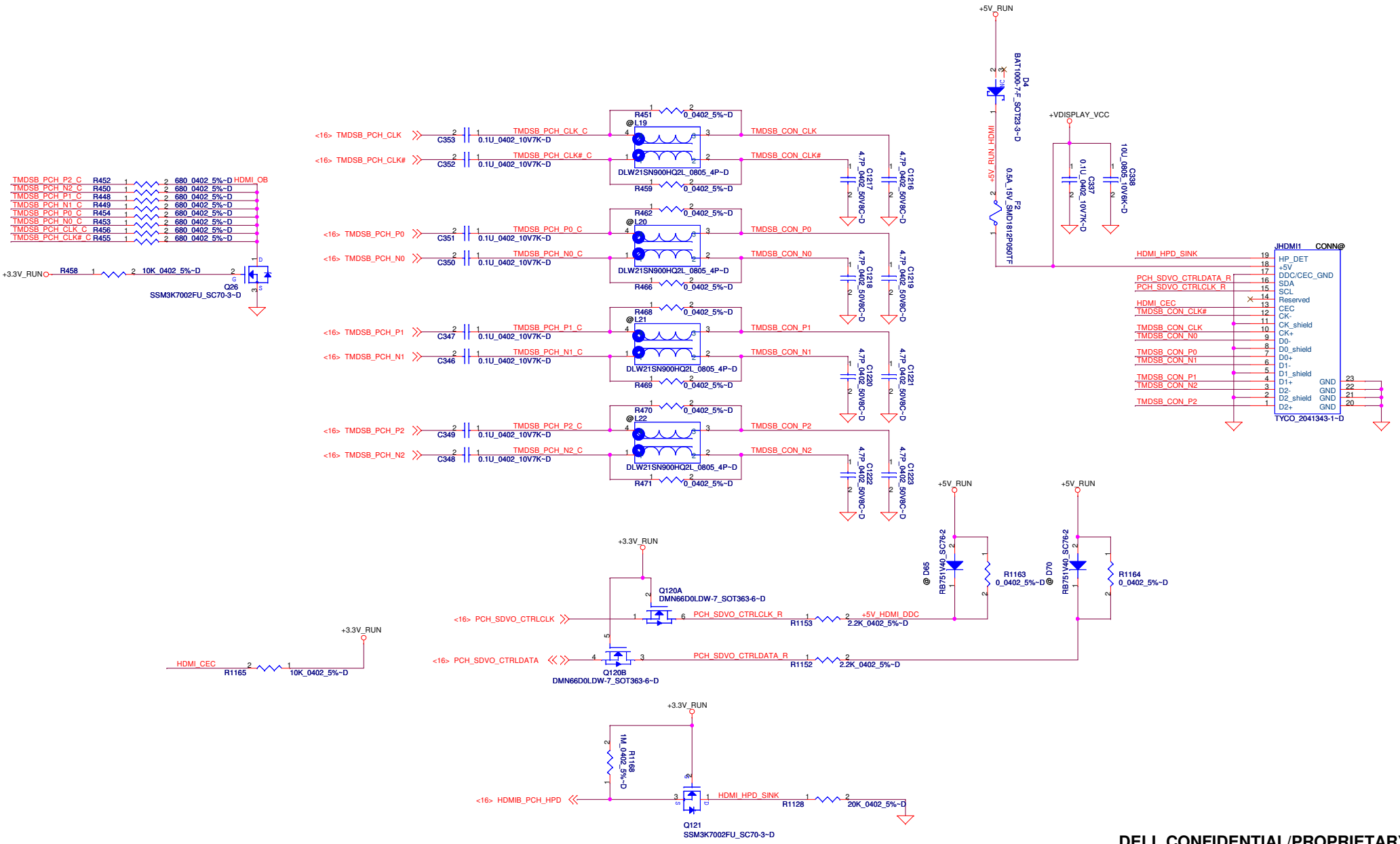
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: CRT/Video switch		
Size	Document Number: LA-7731P	Rev: 0.3
Date: Thursday, September 01, 2011	Sheet 23 of 59	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: LVDS		
Size	Document Number: LA-7731P	Rev: 0.3
Date: Thursday, September 01, 2011	Sheet 24 of 59	



DELL CONFIDENTIAL/PROPRIETARY

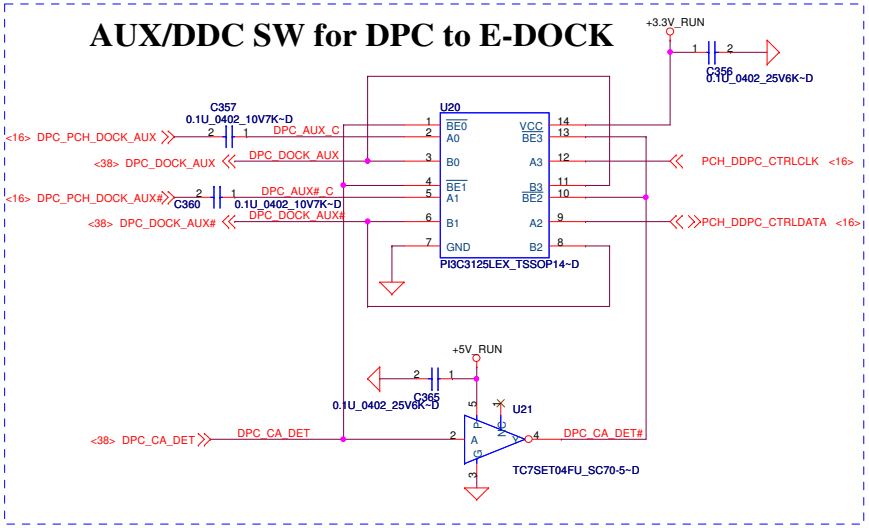
Compal Electronics, Inc.

Title: HDMI port

Size | Document Number: LA-7731P | Rev: 0.3

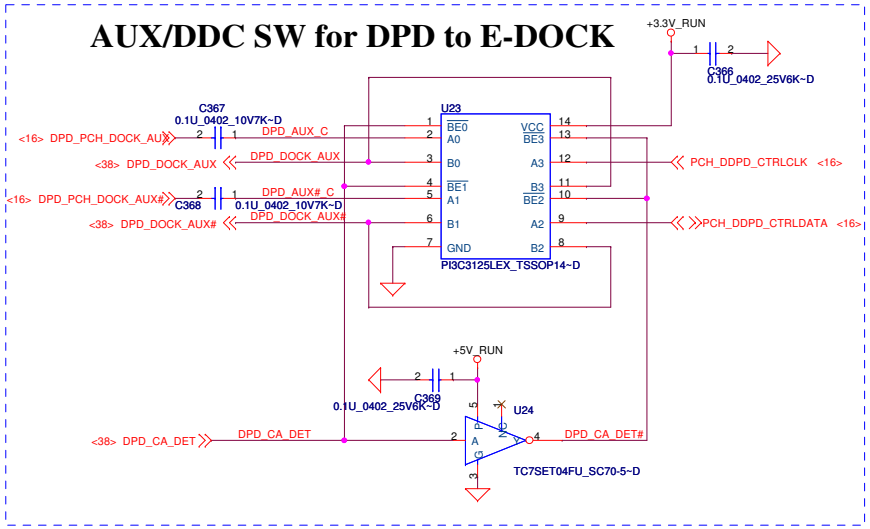
Date: Thursday, September 01, 2011 | Sheet 25 of 59

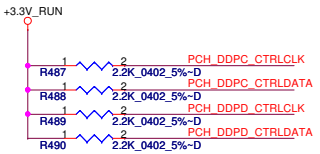
AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample availabe on May.

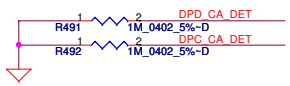
AUX/DDC SW for DPD to E-DOCK





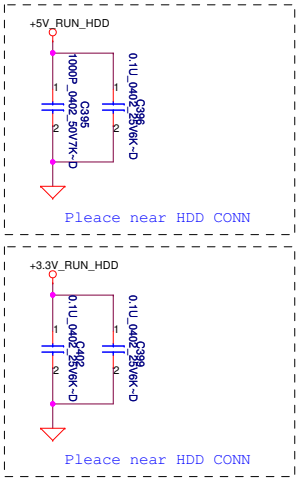
Intel WW18 Strapping option

Intel WW18 Strapping option

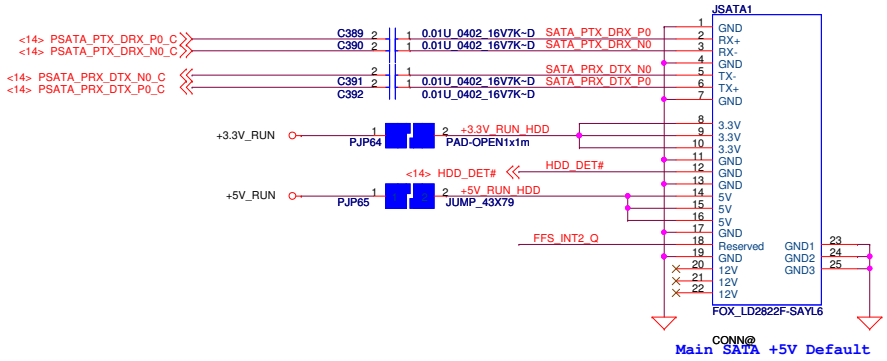


DELL CONFIDENTIAL/PROPRIETARY

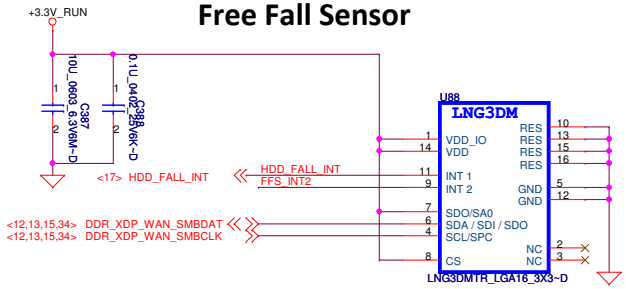
Compal Electronics, Inc.	
Title	DP125
Size	Document Number: LA-7731P
Rev	0.3
Date: Thursday, September 01, 2011	Sheet 26 of 59

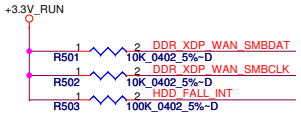


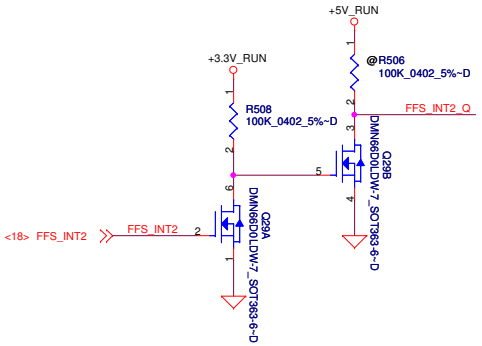
For HDD Temp.



Free Fall Sensor







DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: HDD CONNECTOR

Size | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 27 of 59

DELL CONFIDENTIAL/PROPRIETARY

	Compal Electronics, Inc.	
	Title: ODD CONNECTOR	
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Date: Thursday, September 01, 2011	Sheet 28 of 59	

Internal Speakers Header

15 mils trace

DVDD_IO should match with HDA Bus level

JSPK1 CONN@
ACES_50271-0040N-001

ESD ask to add DE1,DE2

Place C994, C952~C957 close to Codec

Place R1096 close to codec

Place R1097 close to codec

Place LE3 close to codec

Place C962 close to Codec

Place C963~C966 close to Codec

U72
92HD93B2X5NLGXYAX8_QFN48_7X7~D

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Close to U72 pin5

Close to U72 pin6

Place closely to Pin 13.

Place closely to Pin 14

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

EMI request to add C984,C985

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Intel
PORT D	Internal SPK
PORT E	DOCK
PORT F	DOCK

R1664, C1165, R1665
place close to Combo Jack

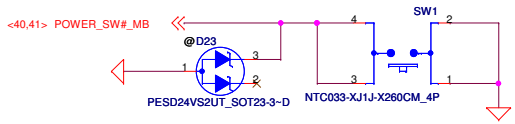
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Azalia (HD) Codec

Size: | Document Number: LA-7731P | Rev: 0.3

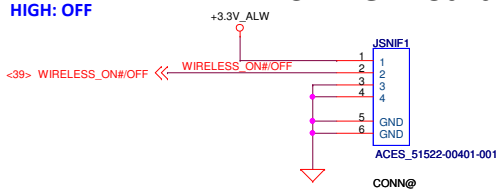
Date: Thursday, September 01, 2011 | Sheet 29 of 59

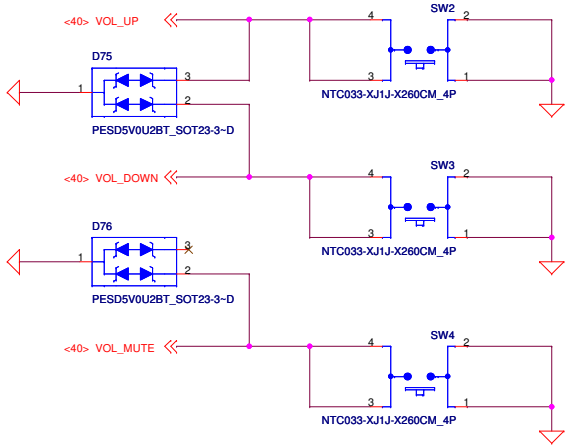


POWER & INSTANT ON SWITCH

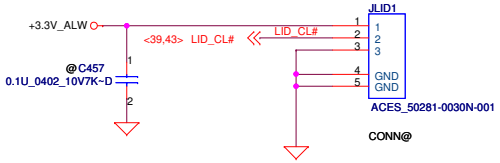
Defult on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

Sniffer Board



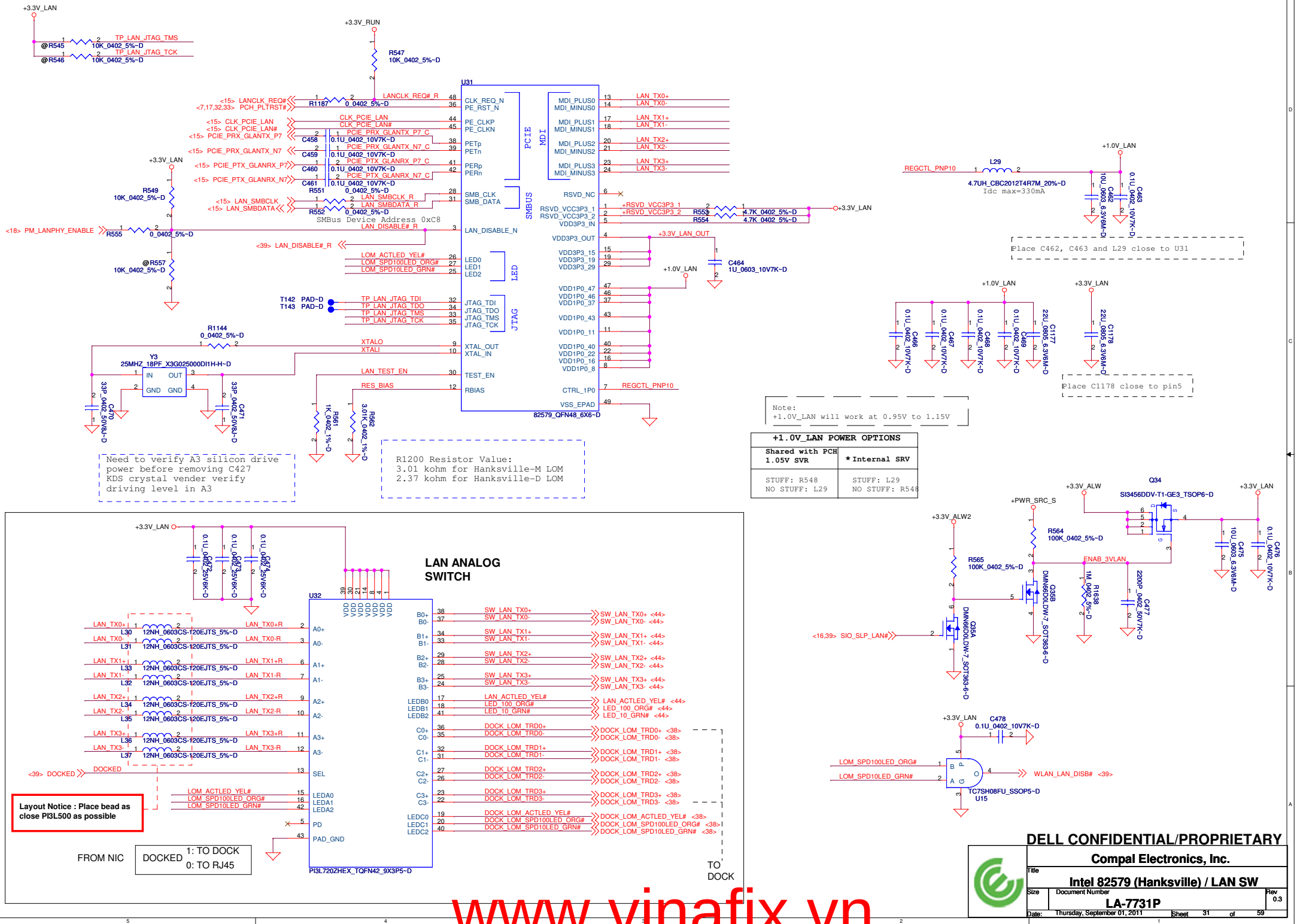


Lid board



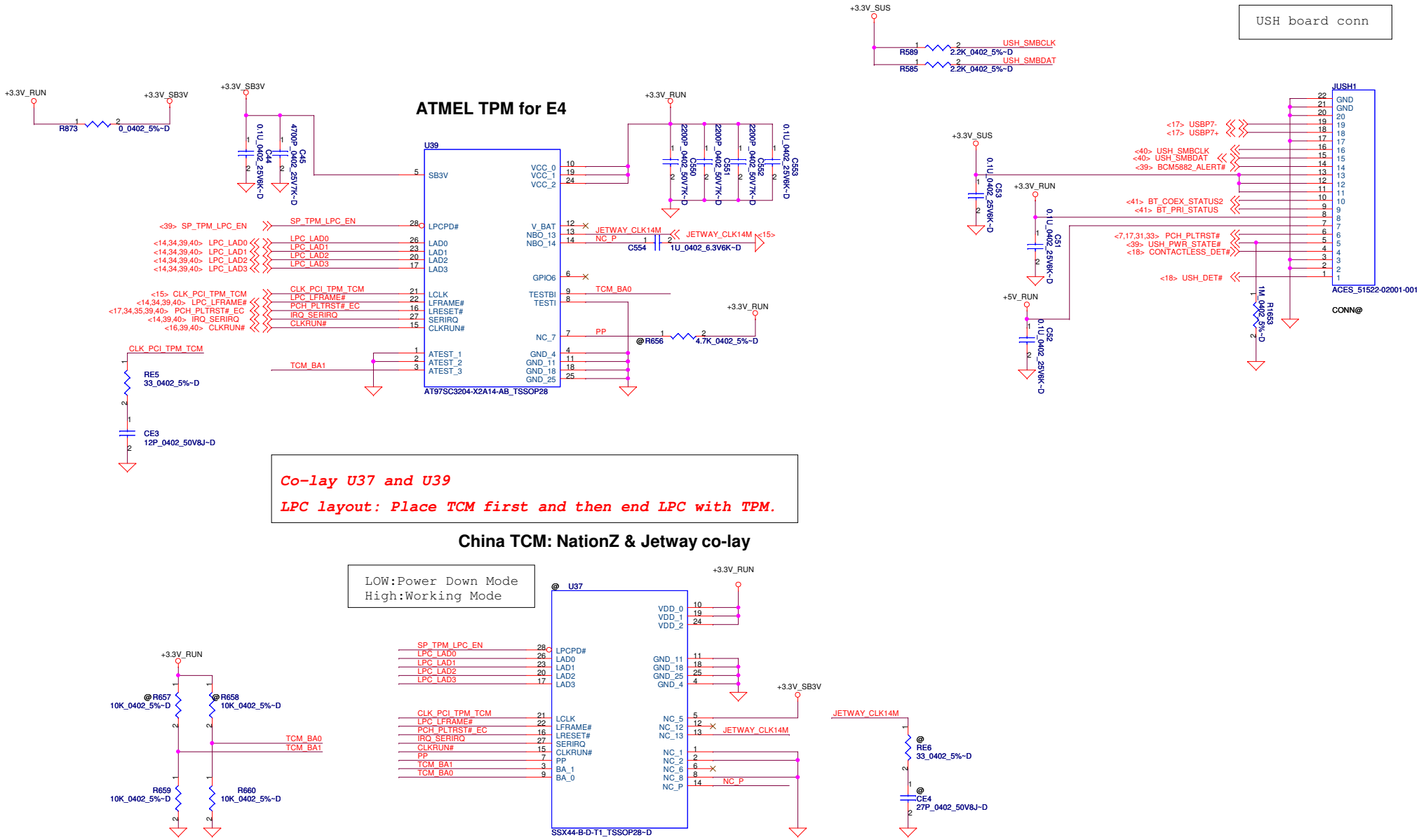
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	PWR SW/Sub-board Connector
Size	Document Number: LA-7731P
Rev	0.3
Date: Thursday, September 01, 2011	Sheet 30 of 59



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Intel 82579 (Hanksville) / LAN SW		
Size	Document Number: LA-7731P	Rev: 0.3
Date: Thursday, September 01, 2011	Sheet 31 of 59	



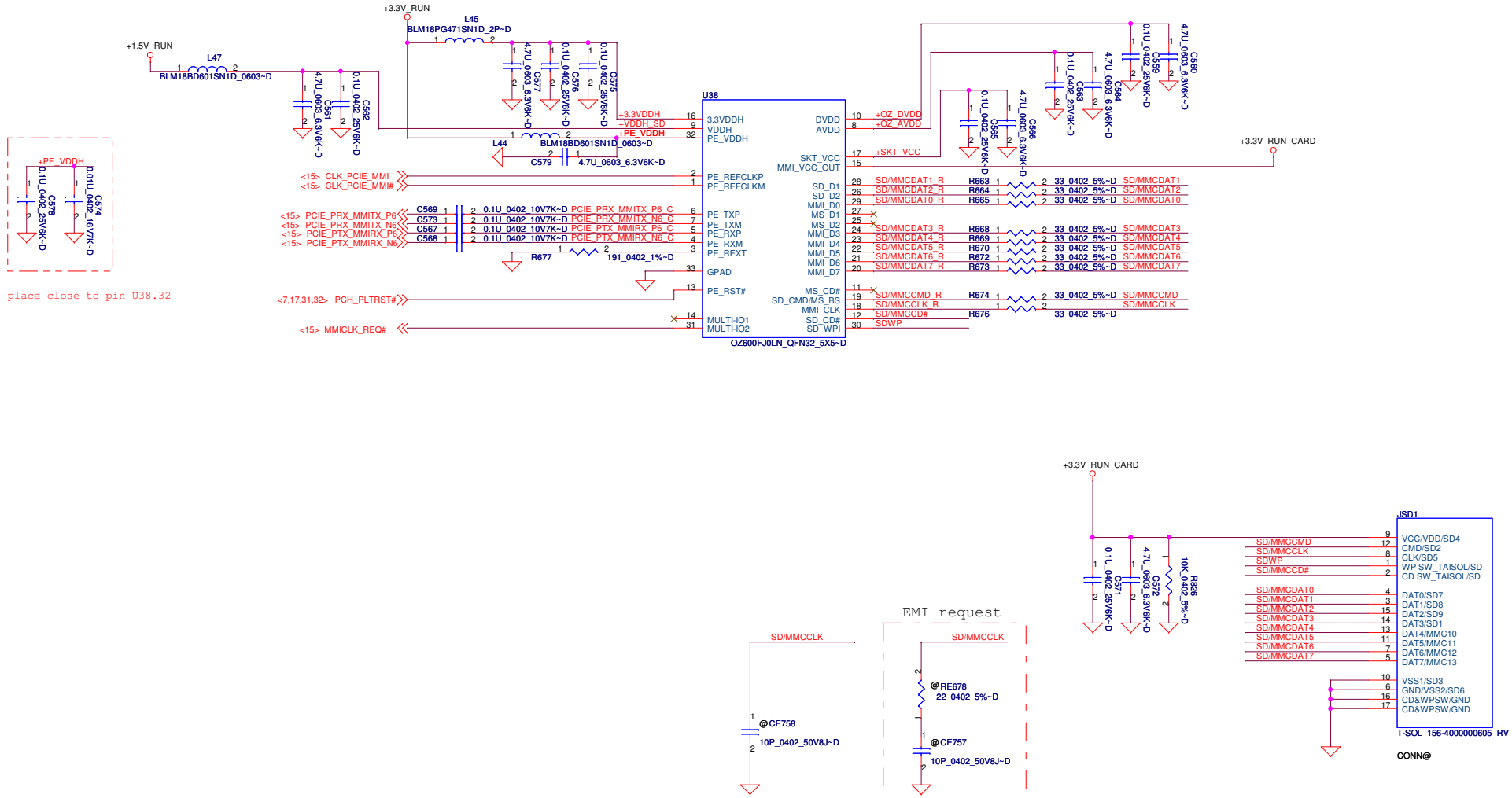
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: TPM/TCM

Size | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 32 of 59

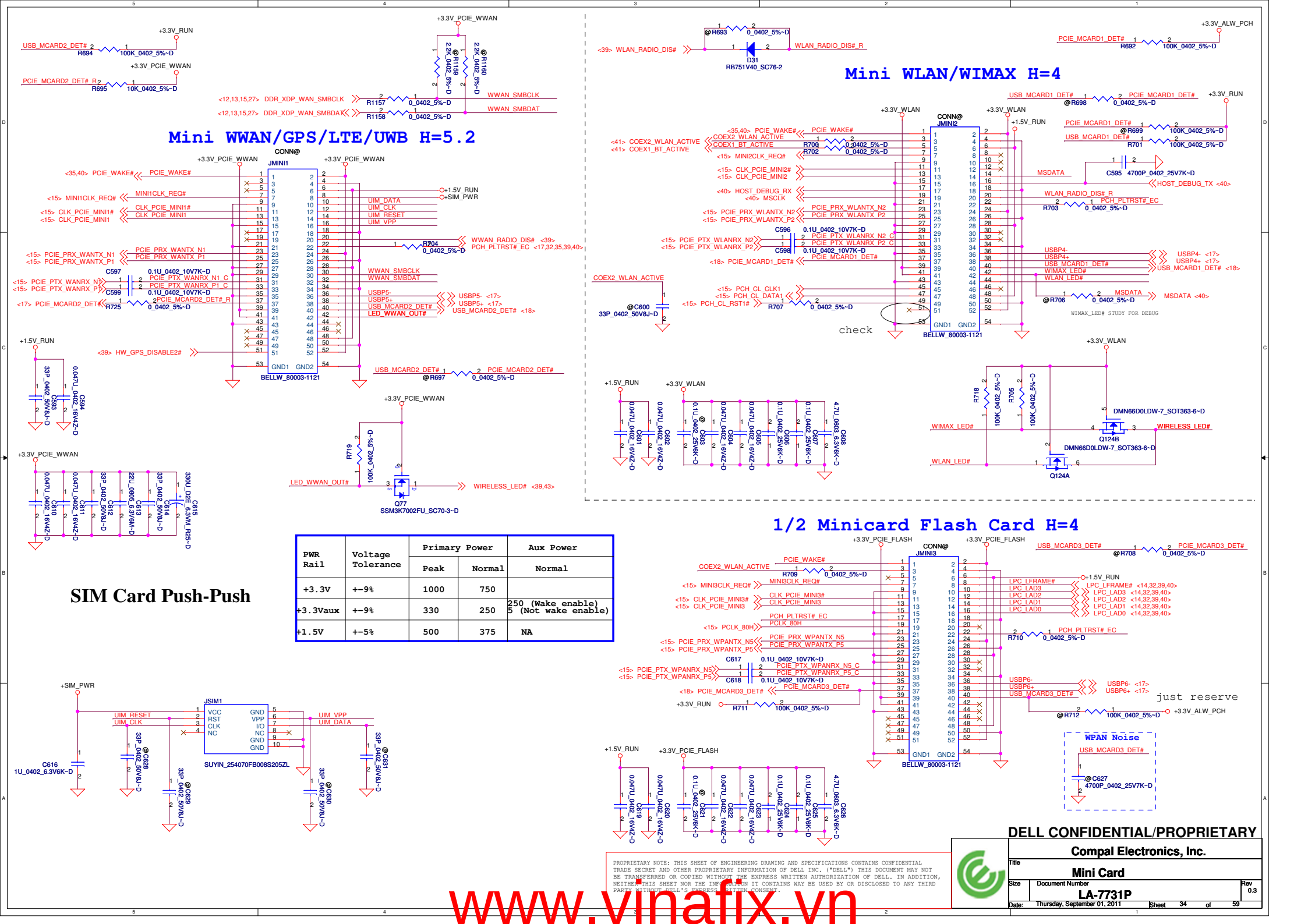


Compal Electronics, Inc.

Title: Card Reader

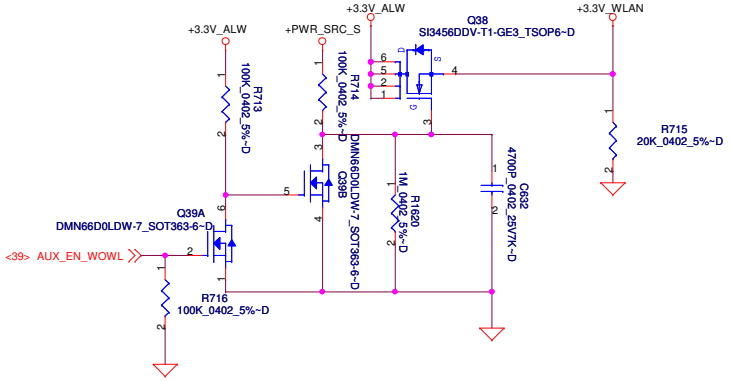
Size | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 33 of 59

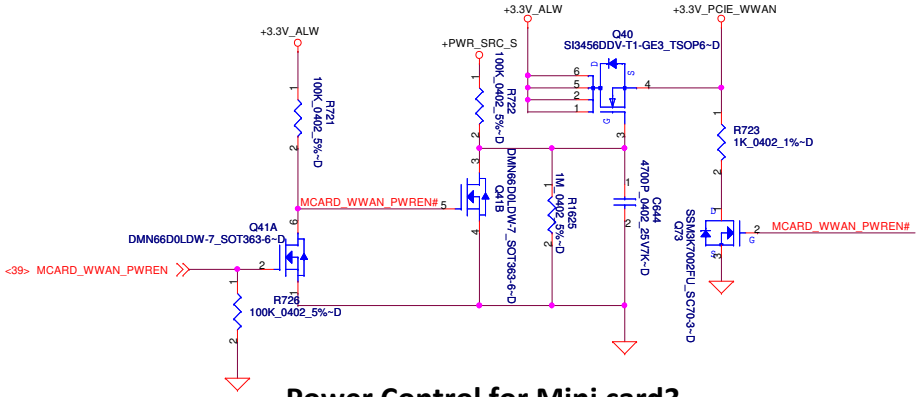


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

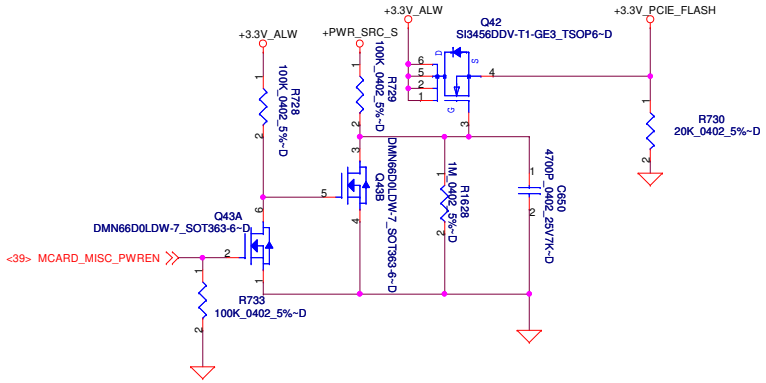
Power Control for Mini card1



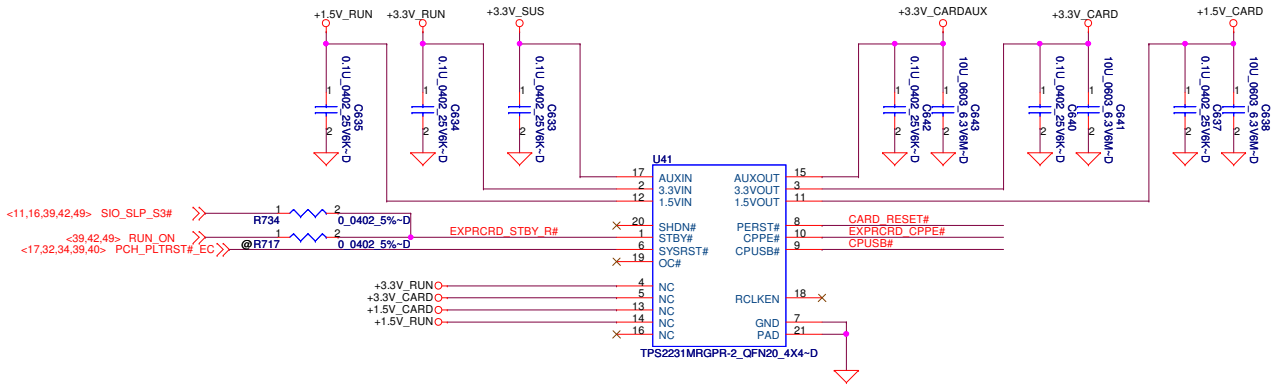
Power Control for Mini card2



Power Control for Mini card3

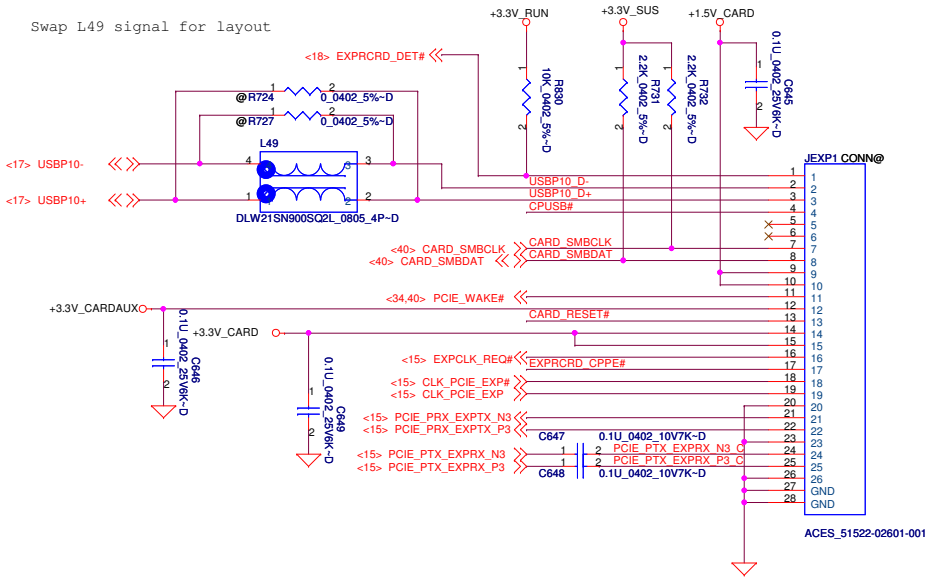


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.

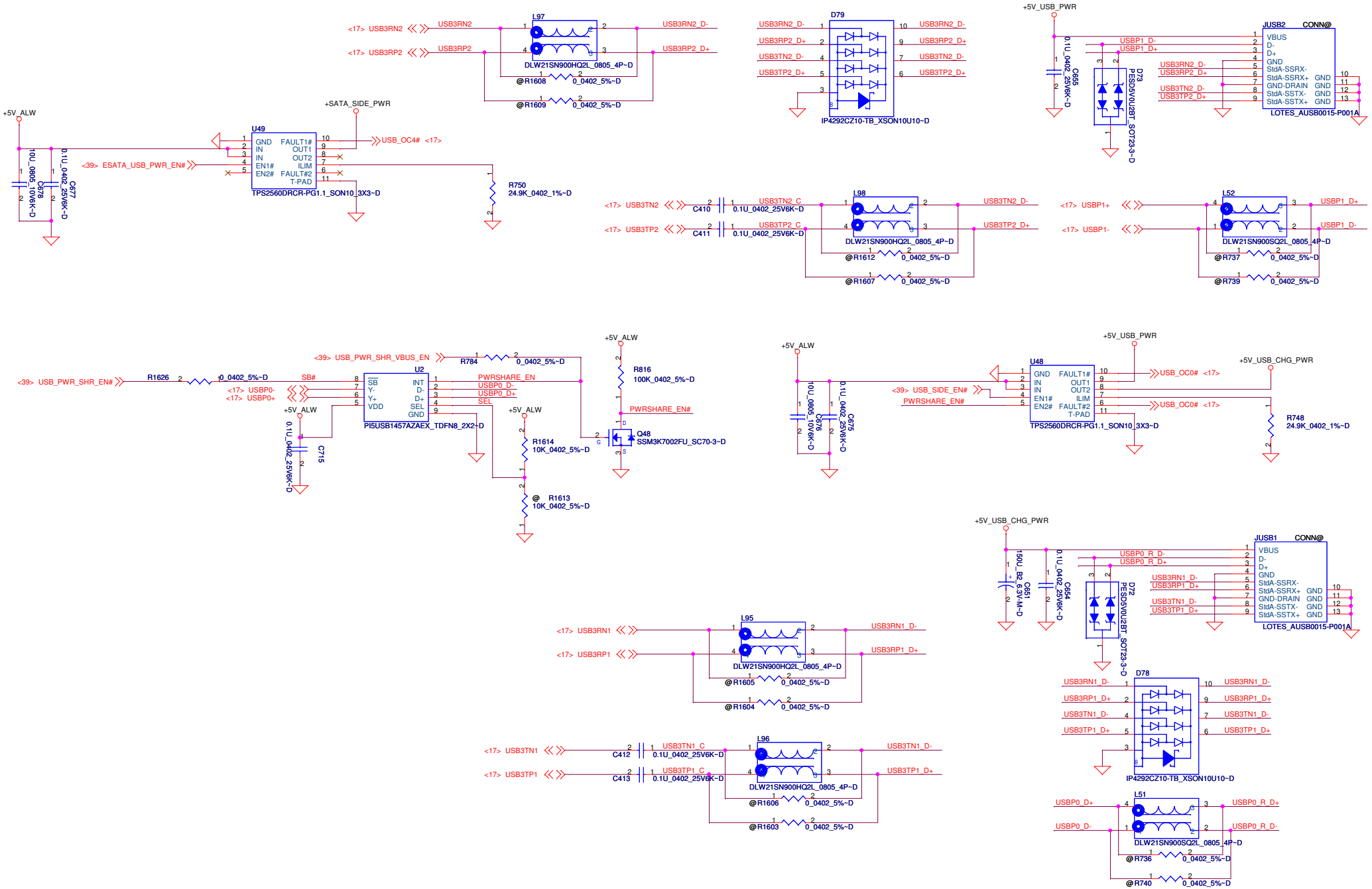


Compal Electronics, Inc.

Title: PCIE-SATA SW / PCIE PWR

Size: | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 35 of 59



Compal Electronics, Inc.

Title: USB 3.0 x2

Size: | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 36 of 59

ESATA Repeater

If use 412CD part only, de-pop R745, R751, pop R746
If use 412A part, de-pop R746, pop R745, R751

8@ U44
PS8513BTQFN20GTR-A0
SA00004WR00

+3.3V_RUN

R741 0_0402_5%~D

U44 7@
SN75LVCP412CDRTJR_QFN20_4X4~D

<18> ESATA_CD#
7@ R746 0_0402_5%~D ESATA_CD#_R
8@ R745 0_0402_5%~D ESATA_PTX_DRX_P4

<14> ESATA_PTX_DRX_P4_C — C663 0.01U_0402_16V7K~D — ESATA_PTX_DRX_P4
<14> ESATA_PTX_DRX_N4_C — C664 0.01U_0402_16V7K~D — ESATA_PTX_DRX_N4
<14> ESATA_PRX_DTX_N4_C — C665 0.01U_0402_16V7K~D — ESATA_PRX_DTX_N4
<14> ESATA_PRX_DTX_P4_C — C666 0.01U_0402_16V7K~D — ESATA_PRX_DTX_P4

C661 0.01U_0402_16V7K~D
C662 0.1U_0402_25V6K~D
R1595 0_0402_5%~D
R1594 0_0402_5%~D
@R742 0_0402_5%~D
R743 0_0402_5%~D
REXT
ESATA_PE1
ESATA_PE2
ESATA_PTX_DRX_P4_RP
ESATA_PTX_DRX_N4_RP
ESATA_PRX_DTX_P4_RP
ESATA_PRX_DTX_N4_RP

8@ R751 0_0402_5%~D ESATA_CD#_R

+SATA_SIDE_PWR
C687 150U_B2_6.3V-M~D
C688 0.1U_0402_25V6K~D

JESA1
TAIWI_EU134-115CRL-TW
CONN@

ESATA_PTX_DRX_P4_RP — C671 0.01U_0402_16V7K~D — SATA_PTX_DRX_P4
ESATA_PTX_DRX_N4_RP — C672 0.01U_0402_16V7K~D — SATA_PTX_DRX_N4
ESATA_PRX_DTX_N4_RP — C673 0.01U_0402_16V7K~D — SATA_PRX_DTX_N4
ESATA_PRX_DTX_P4_RP — C674 0.01U_0402_16V7K~D — SATA_PRX_DTX_P4

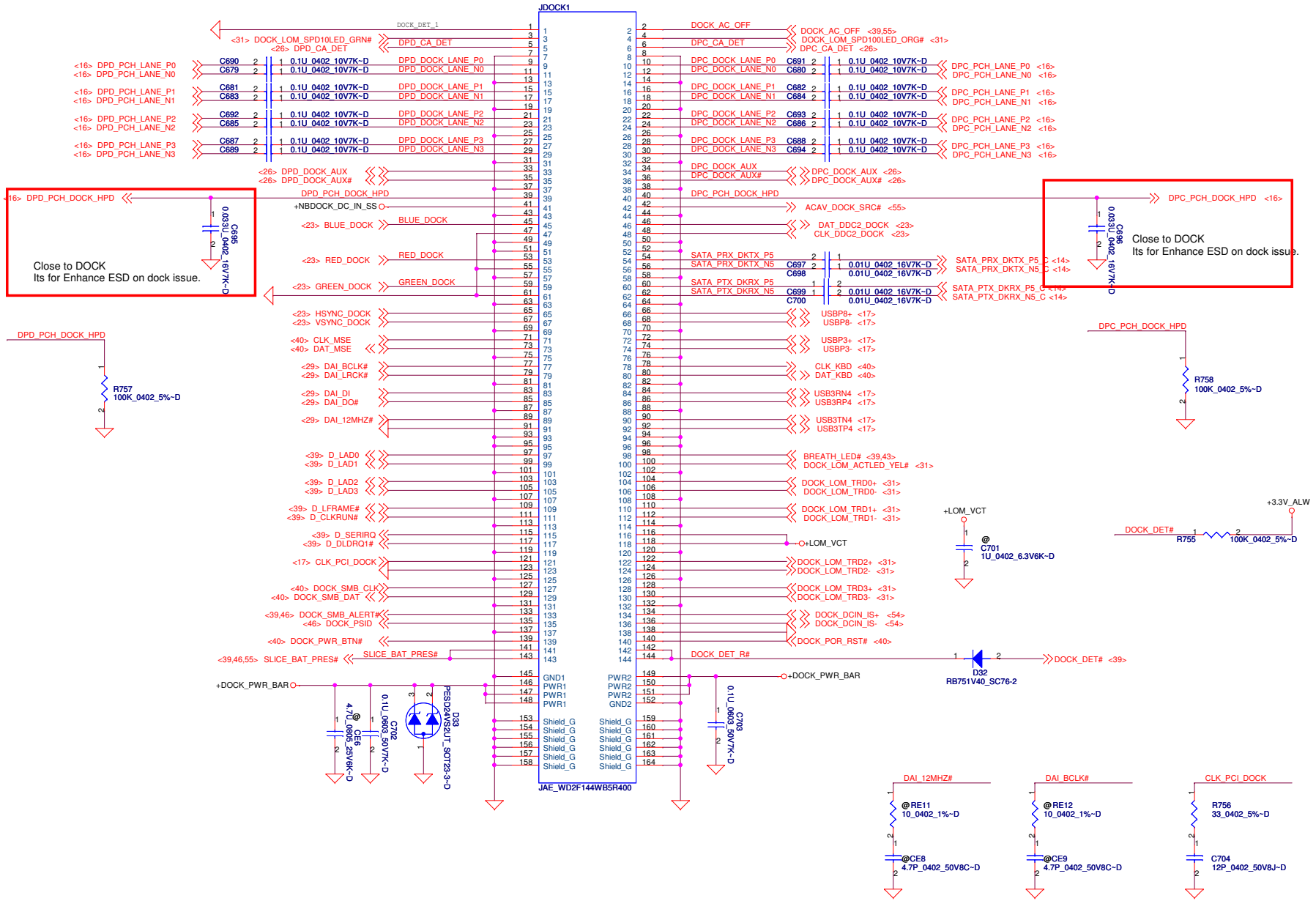
<17> USBP9+ — L90 DLW21SN900SQ2L_0805_4P~D — USBP9_D+
<17> USBP9- — USBP9_D-
@R1150 0_0402_5%~D
@R1151 0_0402_5%~D

D74 PESD5V0U2BT_SOT23-3~D

Place D74 close to JESATA1

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	USB/ESATA/IO/MDC
Size	Document Number: LA-7731P
Rev	0.3
Date: Thursday, September 01, 2011	Sheet 37 of 59



Compal Electronics, Inc.

Title: DOCKING CONN

Size: | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 38 of 59

D12" does not support E-Module, ECE5048(U46) pin B7,A15,B15,A16,B32,A42,A49 not used, but do not assign GPIO for these pins.

	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)

DB Version 0.4
ECE5048-LZY_DQFN132_11X11~D

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: ECE5048

Size | Document Number: LA-7731P | Rev: 0.3

Date: Thursday, September 01, 2011 | Sheet 39 of 59

D12" does not support E-Module, MEC5055 (U51) pin A17,B36 not used, but do not assign GPIO for these pins.

32 KHz Clock

Place closely pin A29

R875	C744	REV
240K	4700p	X00
* 130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

C739 close to U51.B12

CHIPSET_ID for BID function

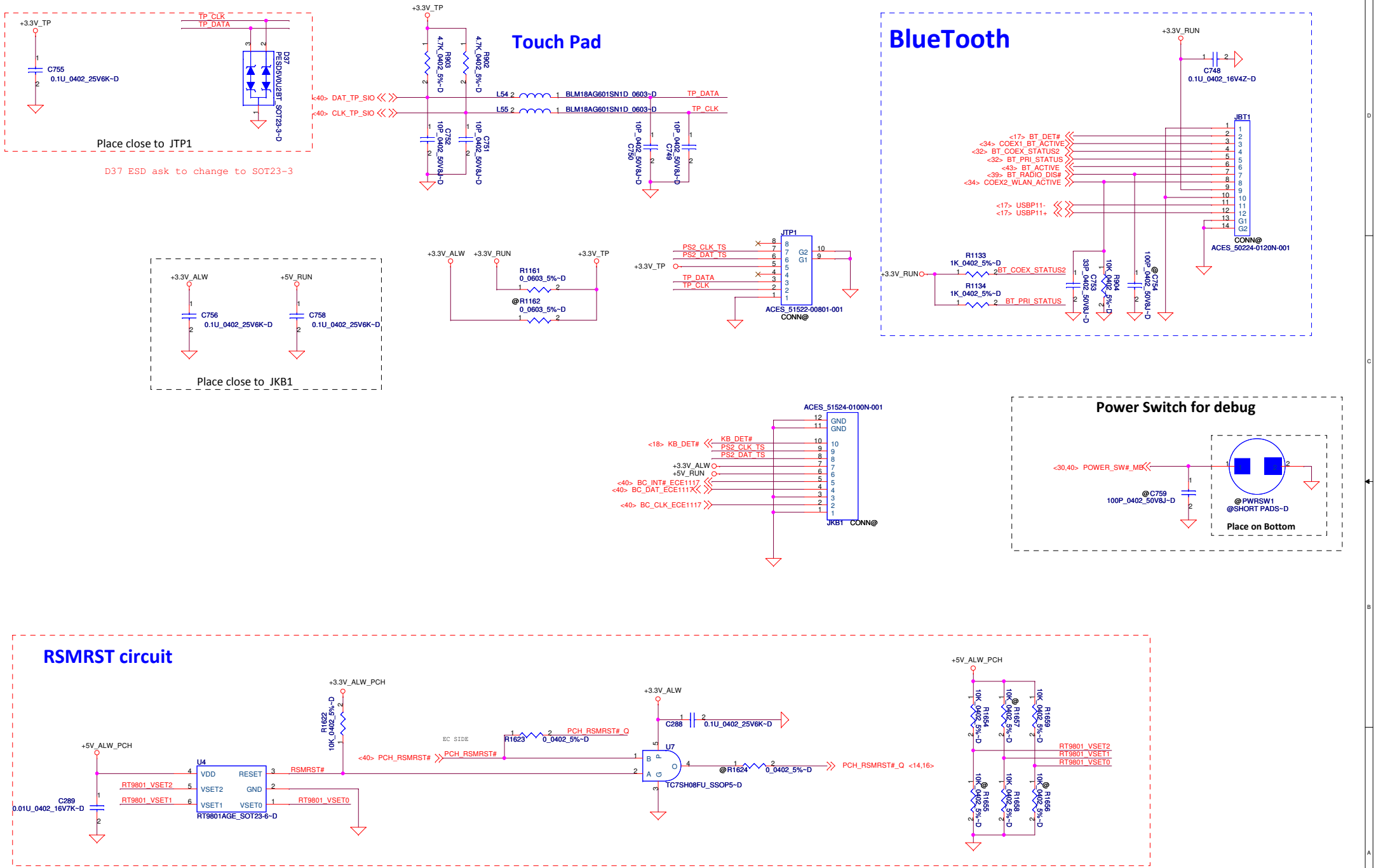
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: MEC5055

Size: Document Number: LA-7731P Rev: 0.3

Date: Thursday, September 01, 2011 Sheet 40 of 59



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Touch PAD/Int KB/BT
Size	Document Number: LA-7731P
Rev	0.3
Date:	Thursday, September 01, 2011
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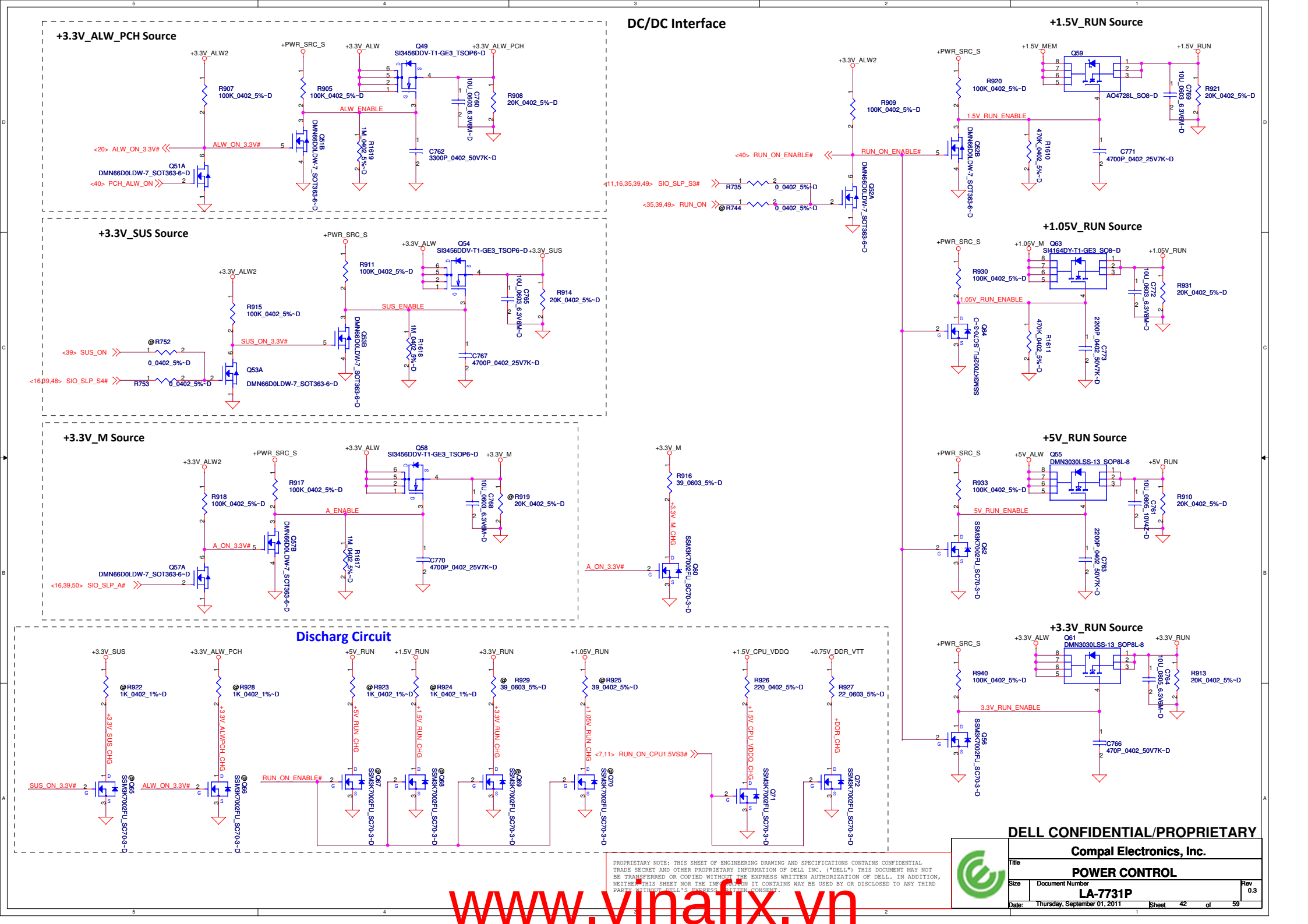
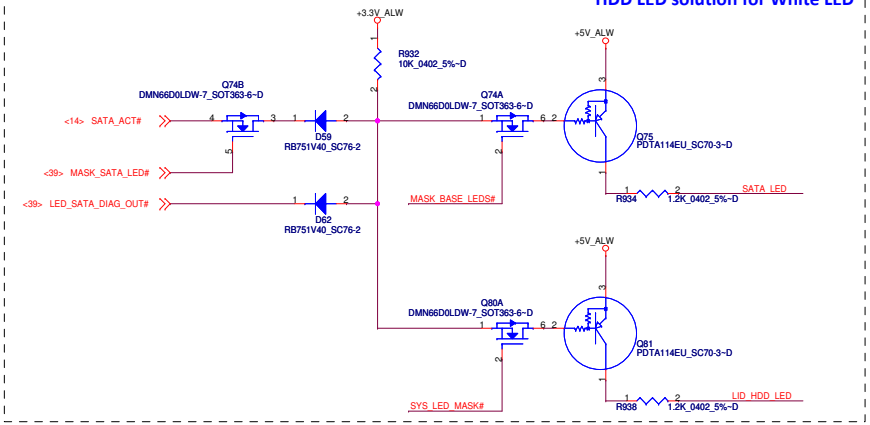
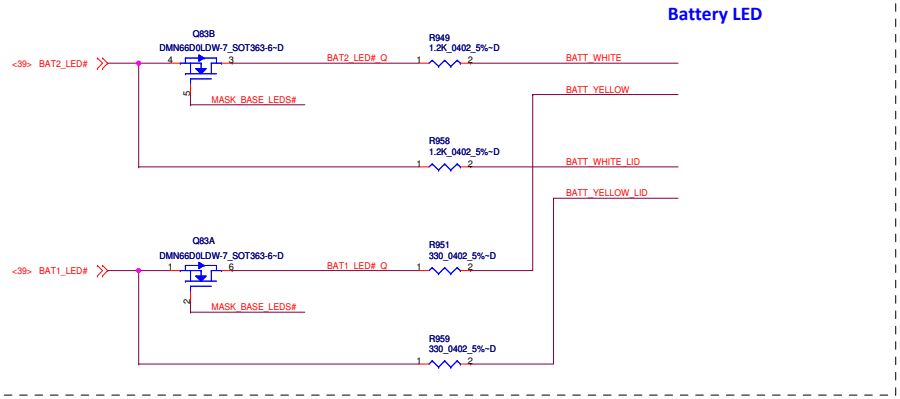


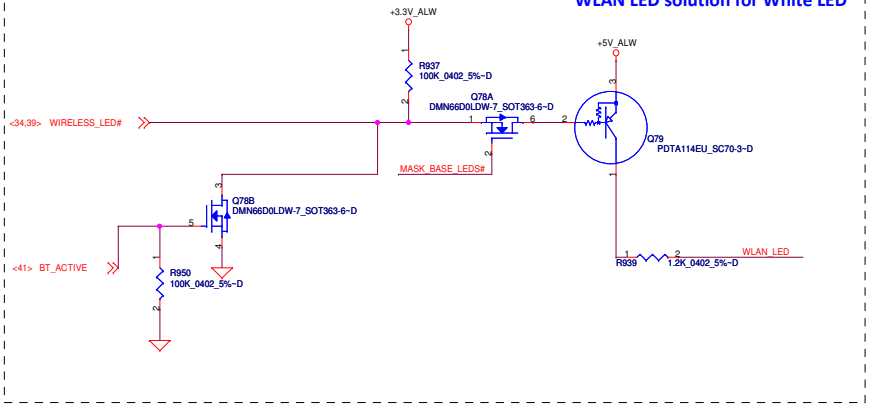
HDD LED solution for White LED



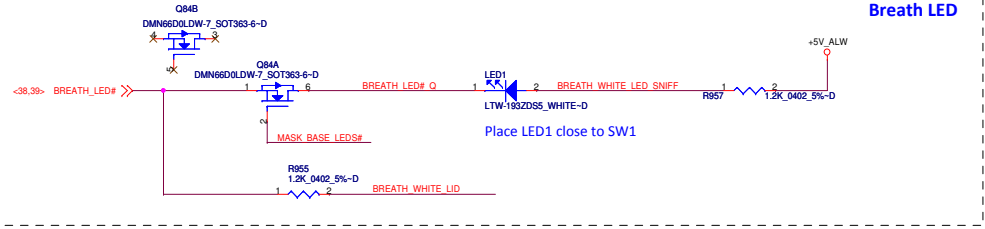
Battery LED



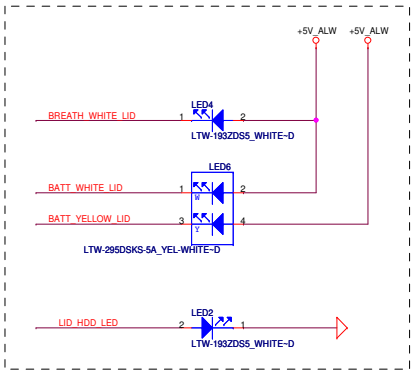
WLAN LED solution for White LED



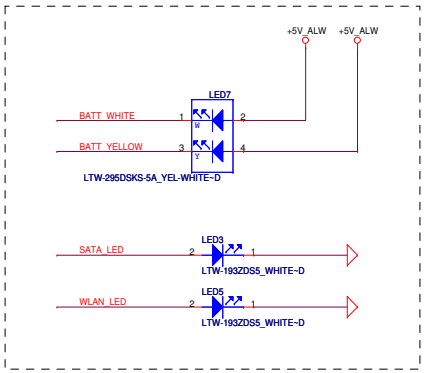
Breath LED



Status LED when LID Close



Status LED when LID Open

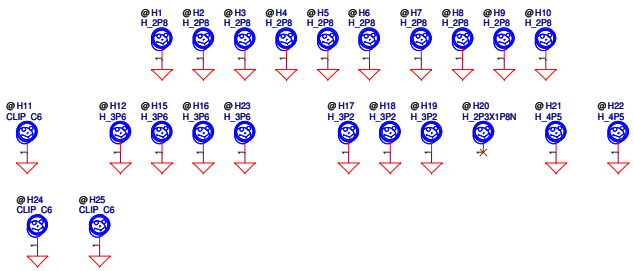


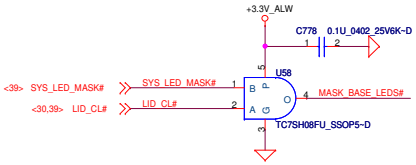
LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D





Compal Electronics, Inc.

Title: PAD and Standoff

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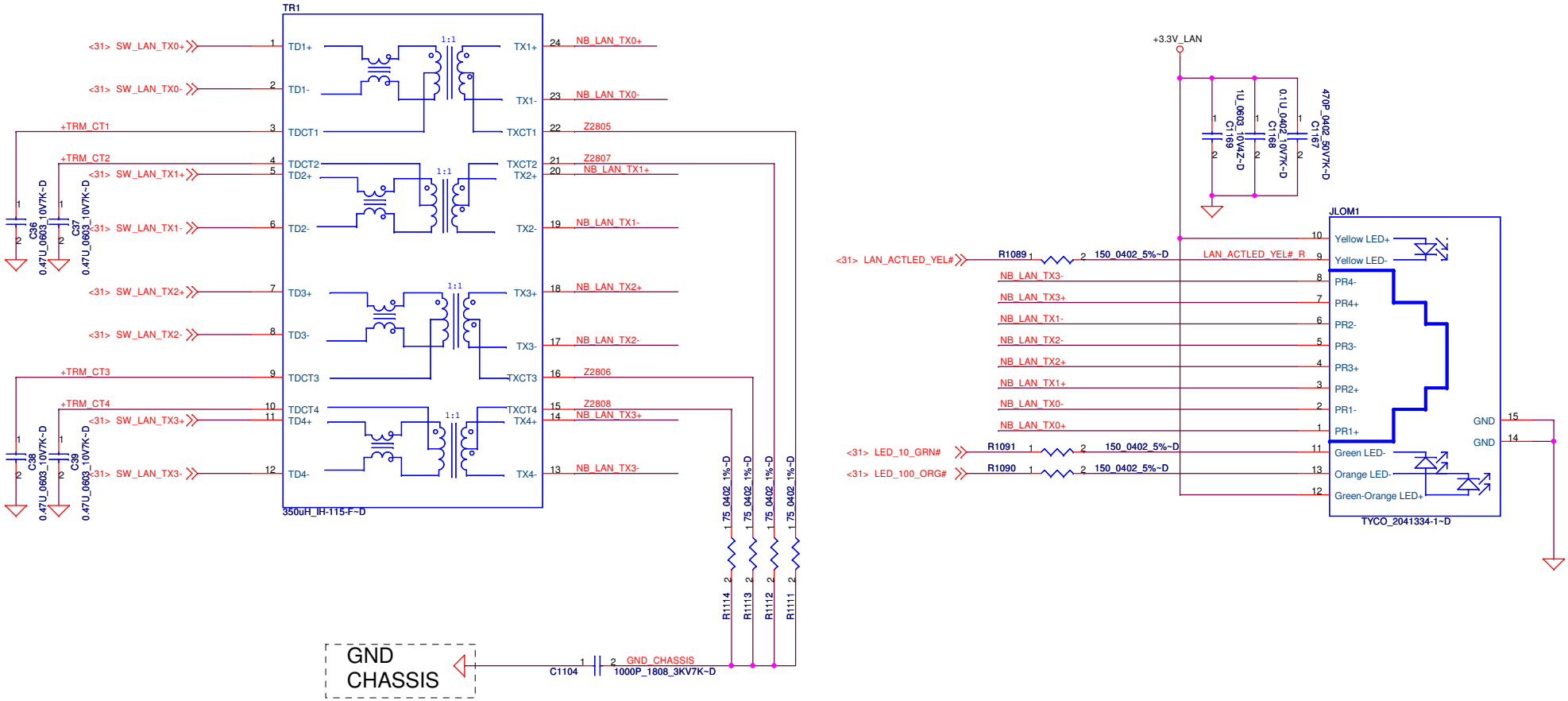

Compal Electronics, Inc.		
Title: RJ45		
Size	Document Number: LA-7731P	Rev: 0.3
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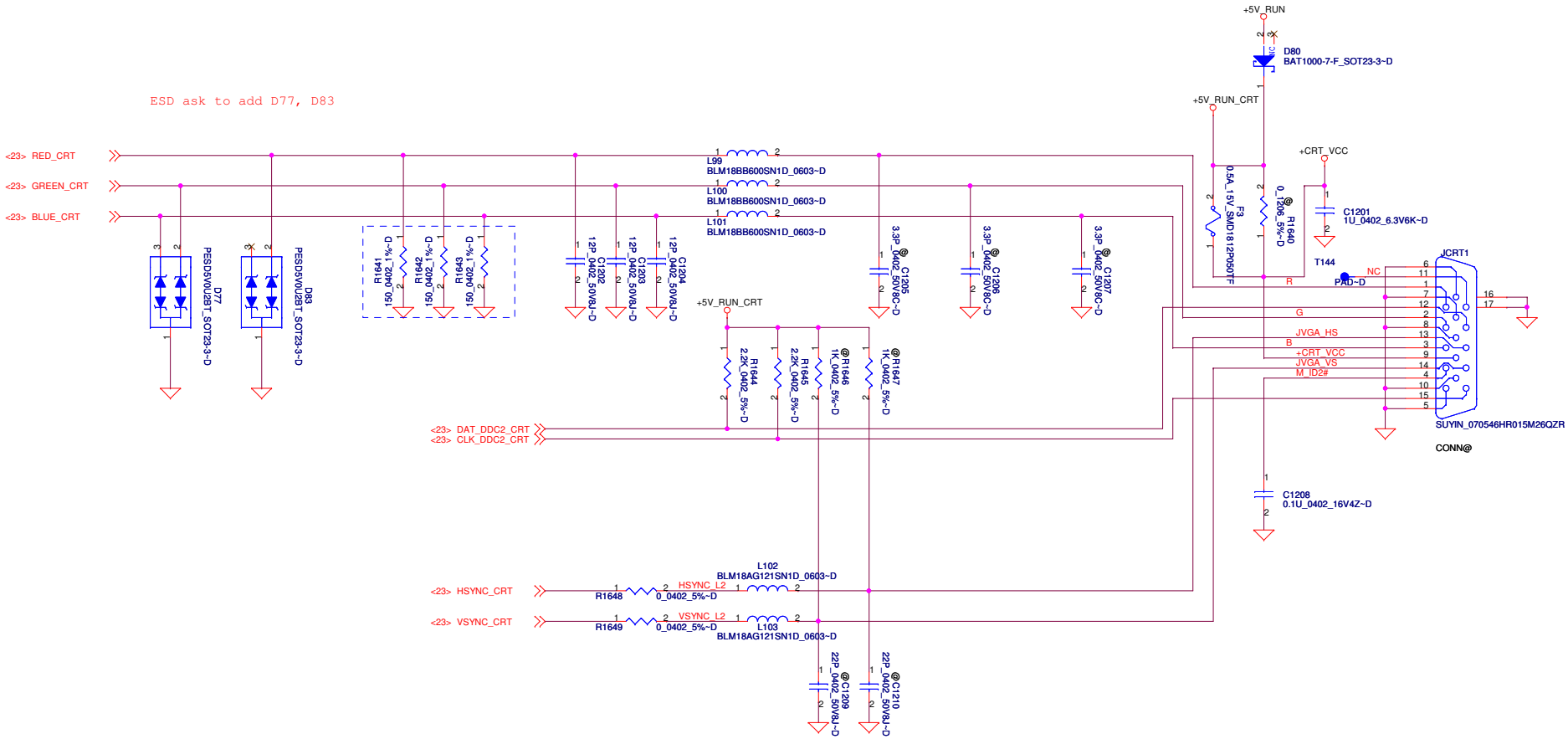
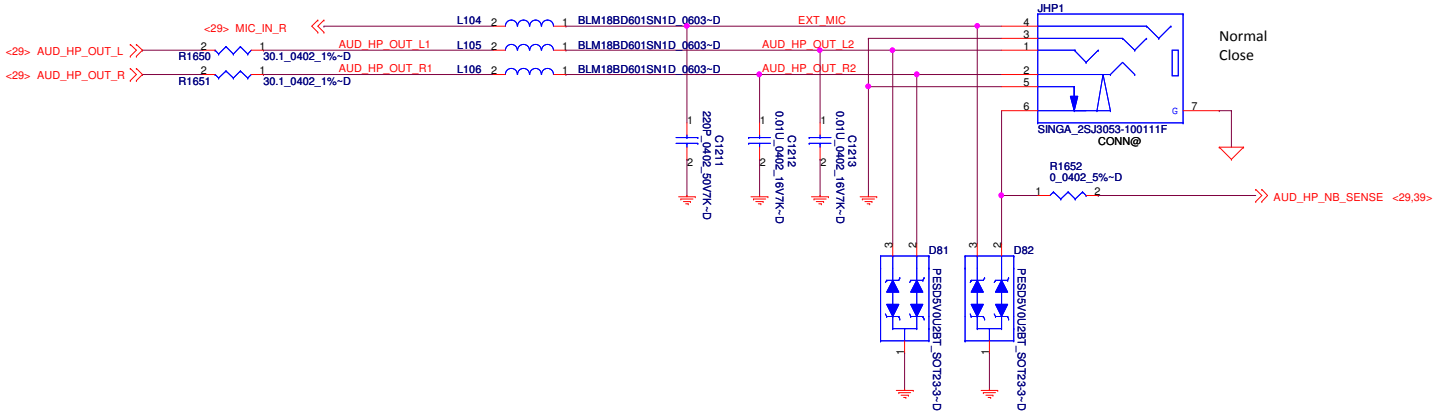


Combo Jack



Compal Electronics, Inc.		
Title: CRT & Combo Jack		
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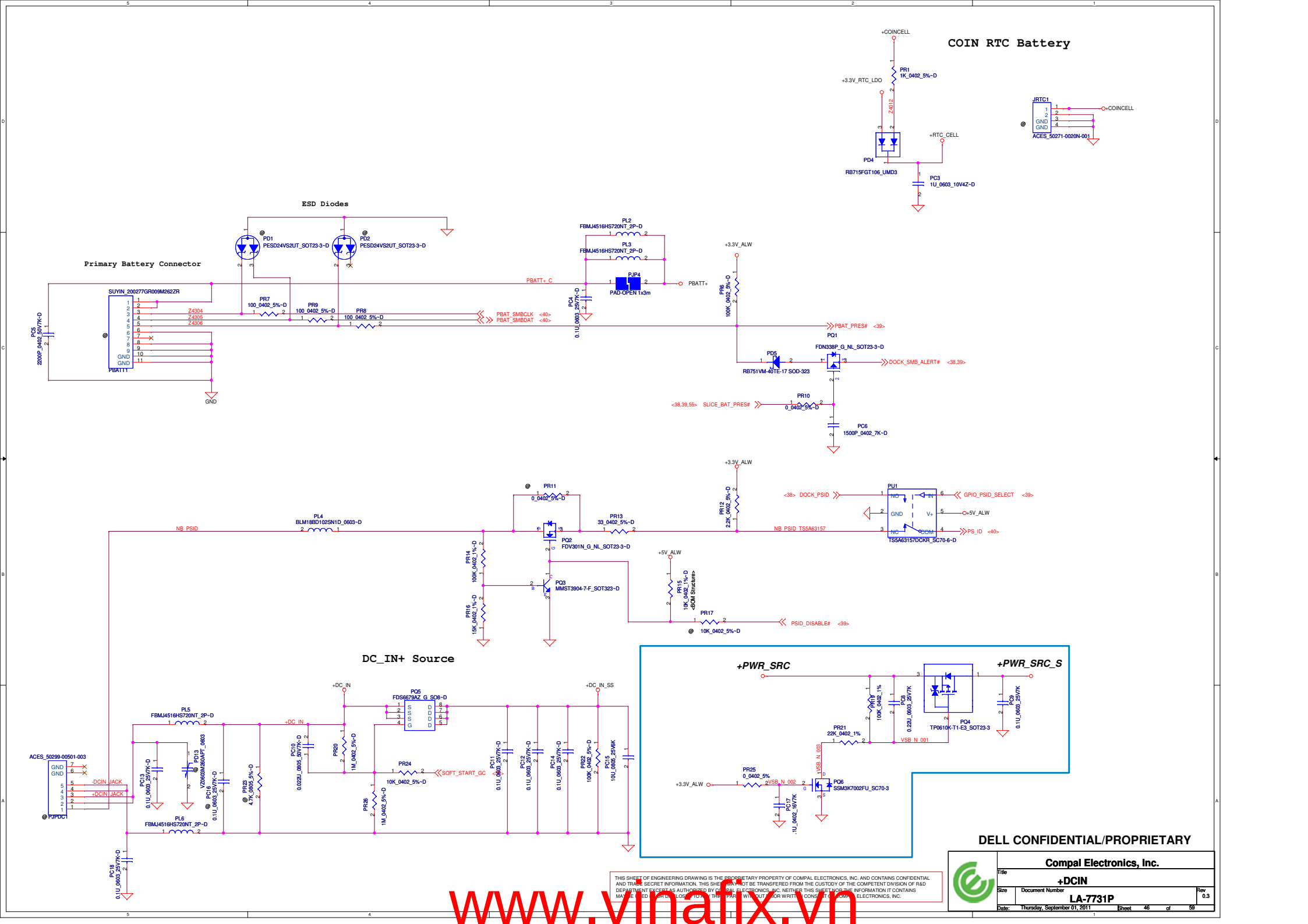
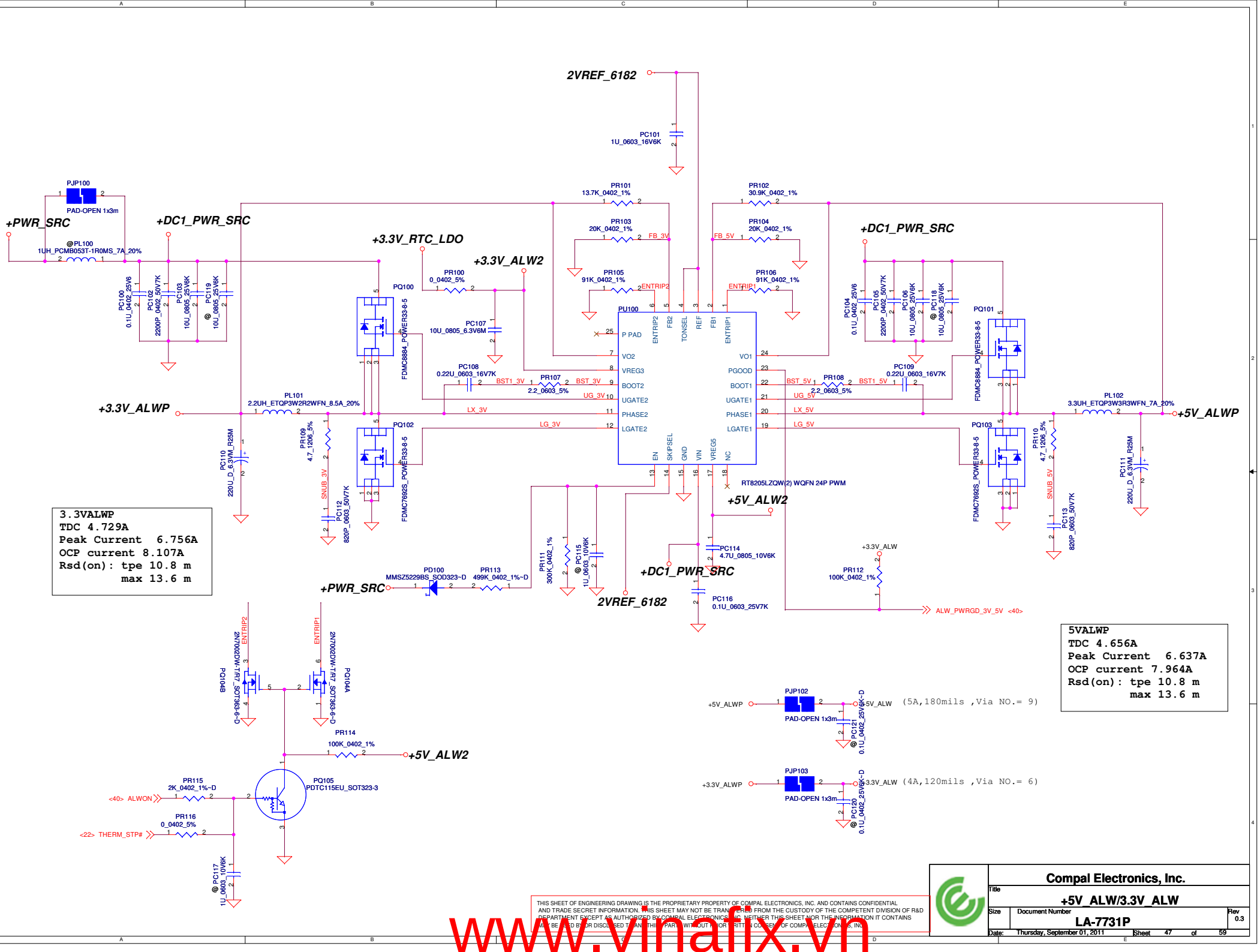
Date: Friday, September 02, 2011	Sheet 45 of 59	





Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

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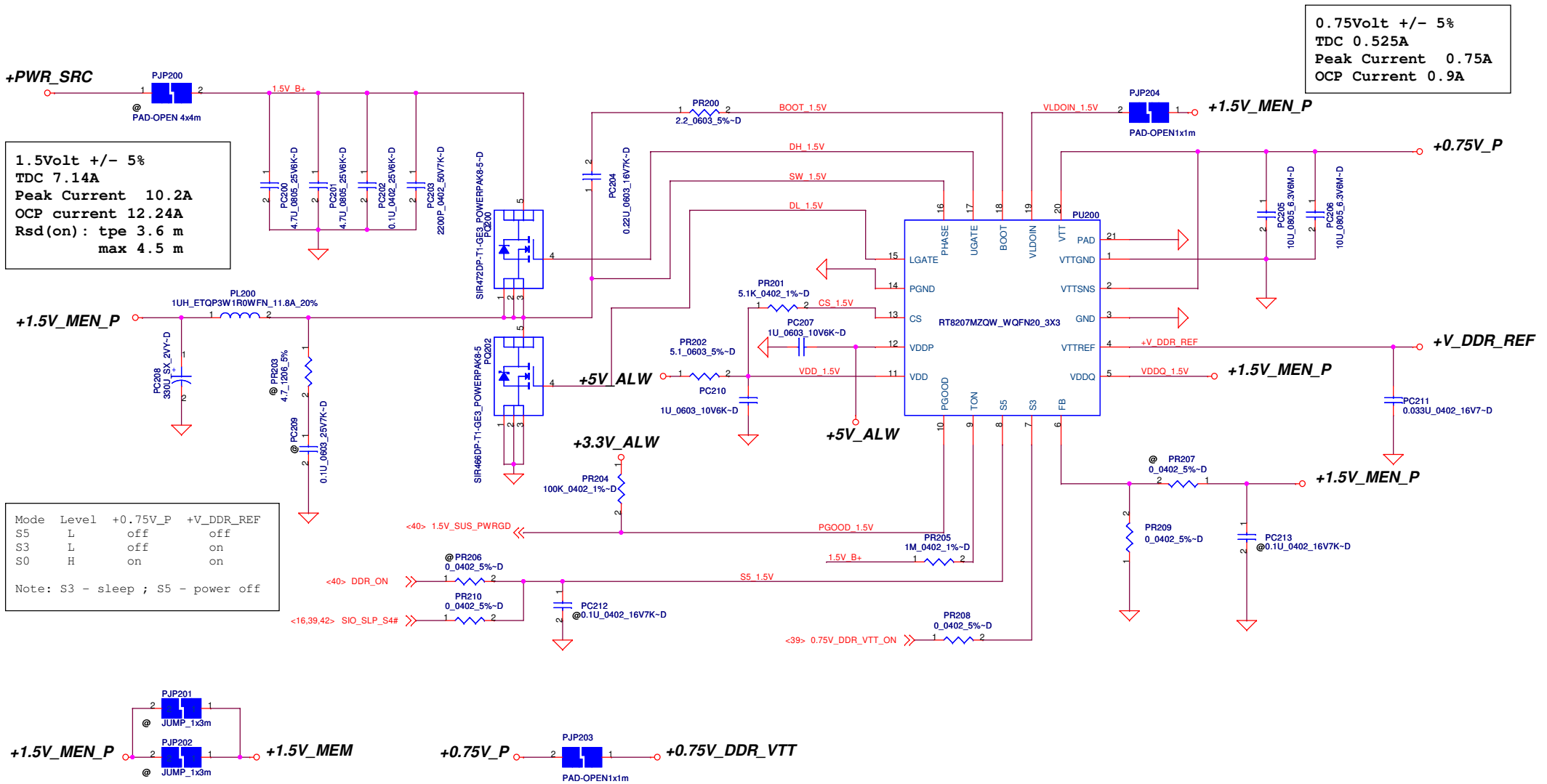

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title	+1.5V_MEN/+0.75V_DDR_VTT	
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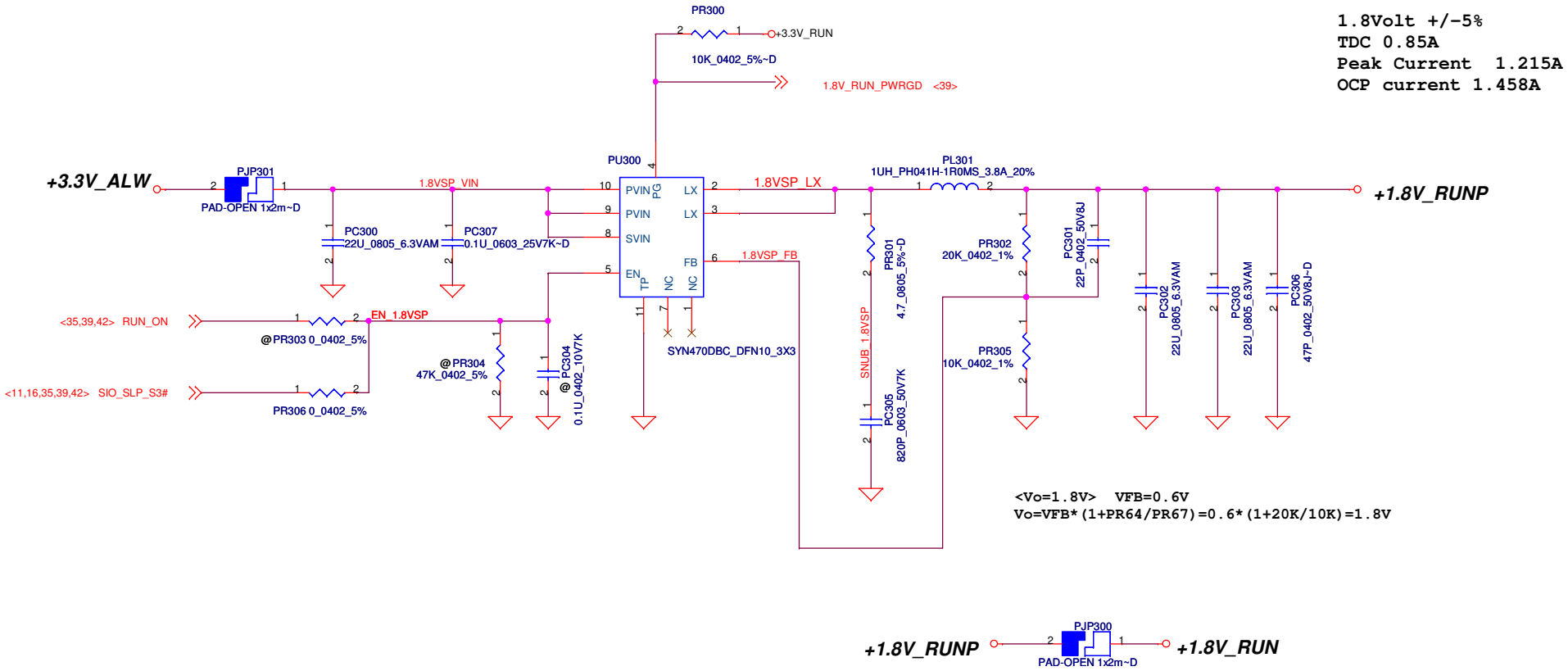
Date: Thursday, September 01, 2011	Sheet 48 of 59	



Compal Electronics, Inc.

Title: +1.8V_RUN

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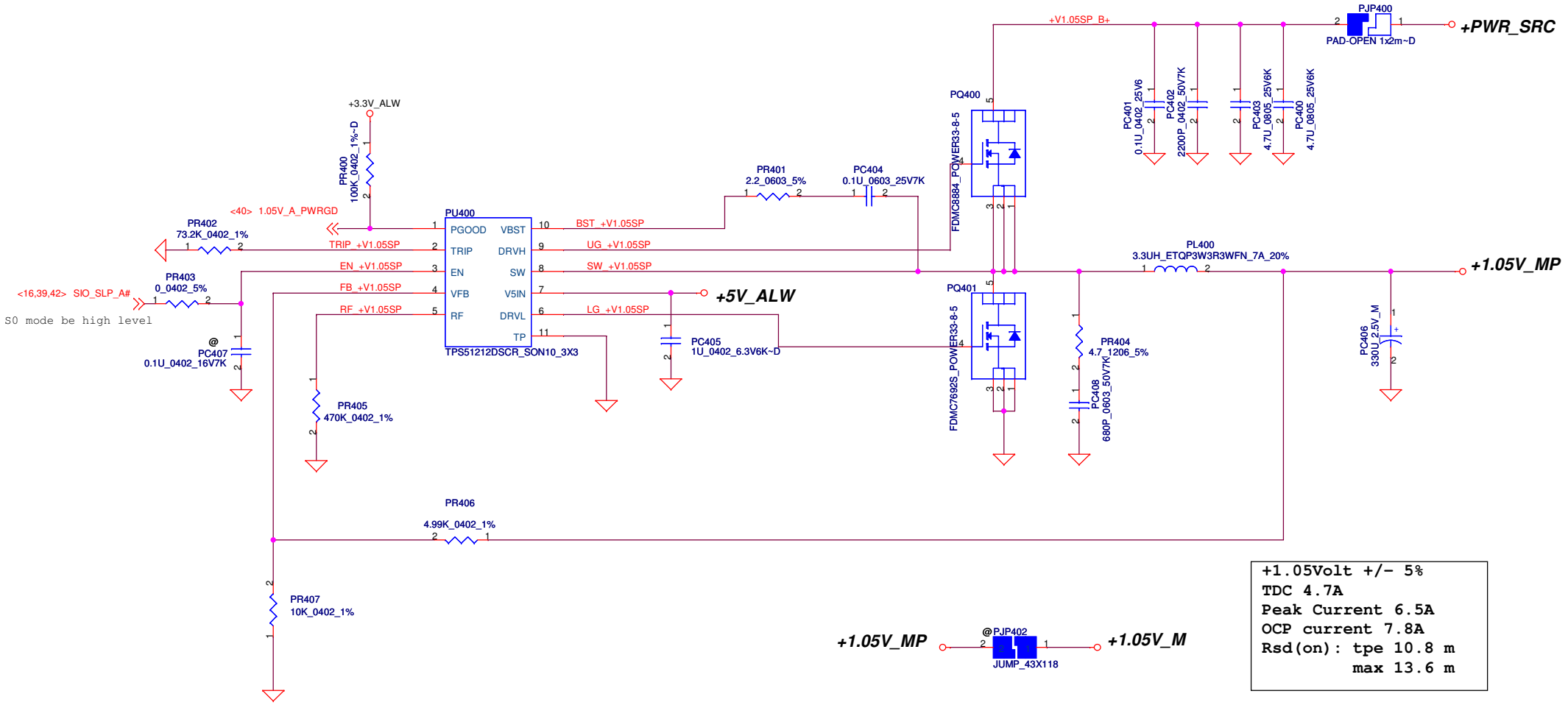

Compal Electronics, Inc.		
Title: +1.05V_M		
Size	Document Number: LA-7731P	Rev: 0.3
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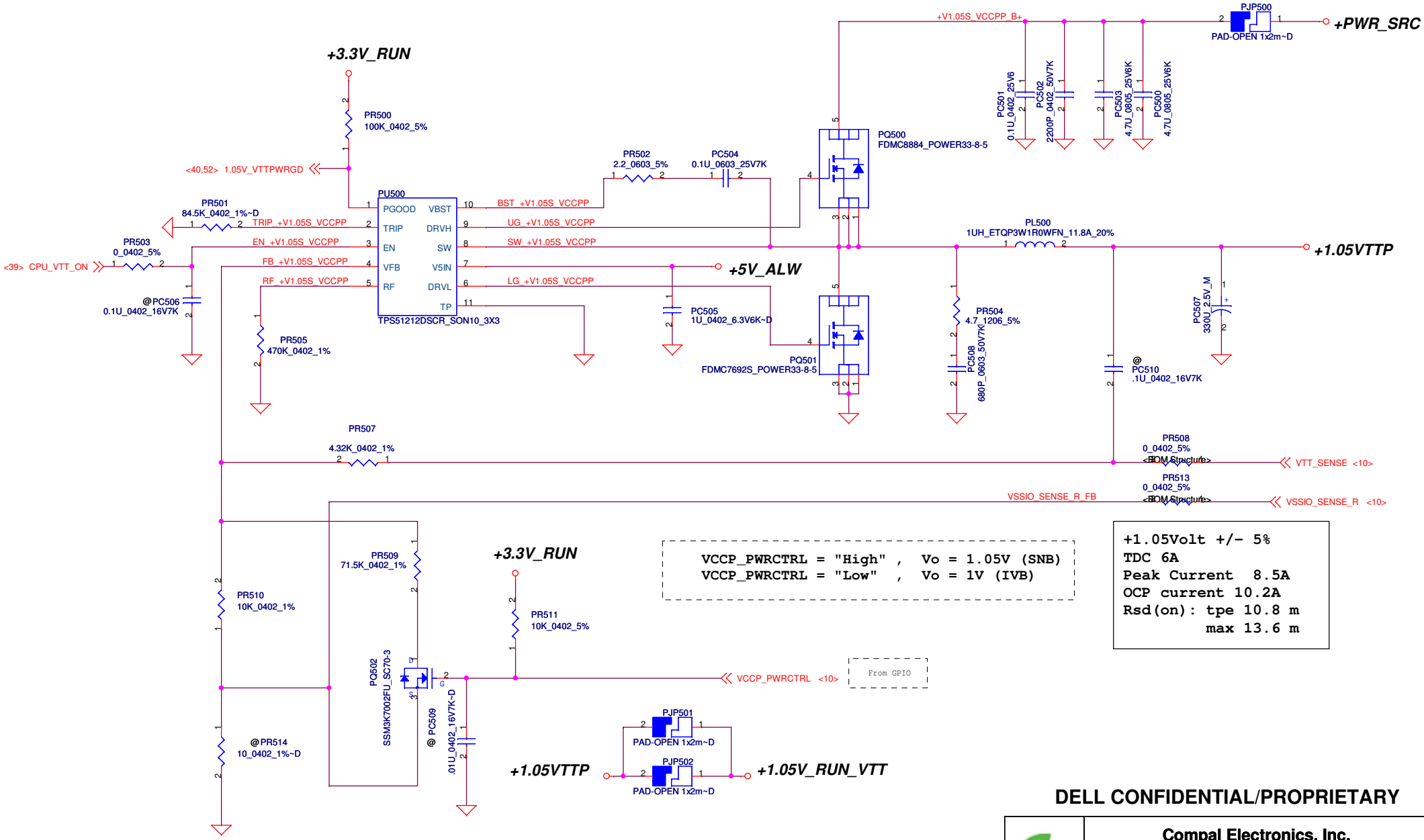

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: +1.05V_RUN_VTT		
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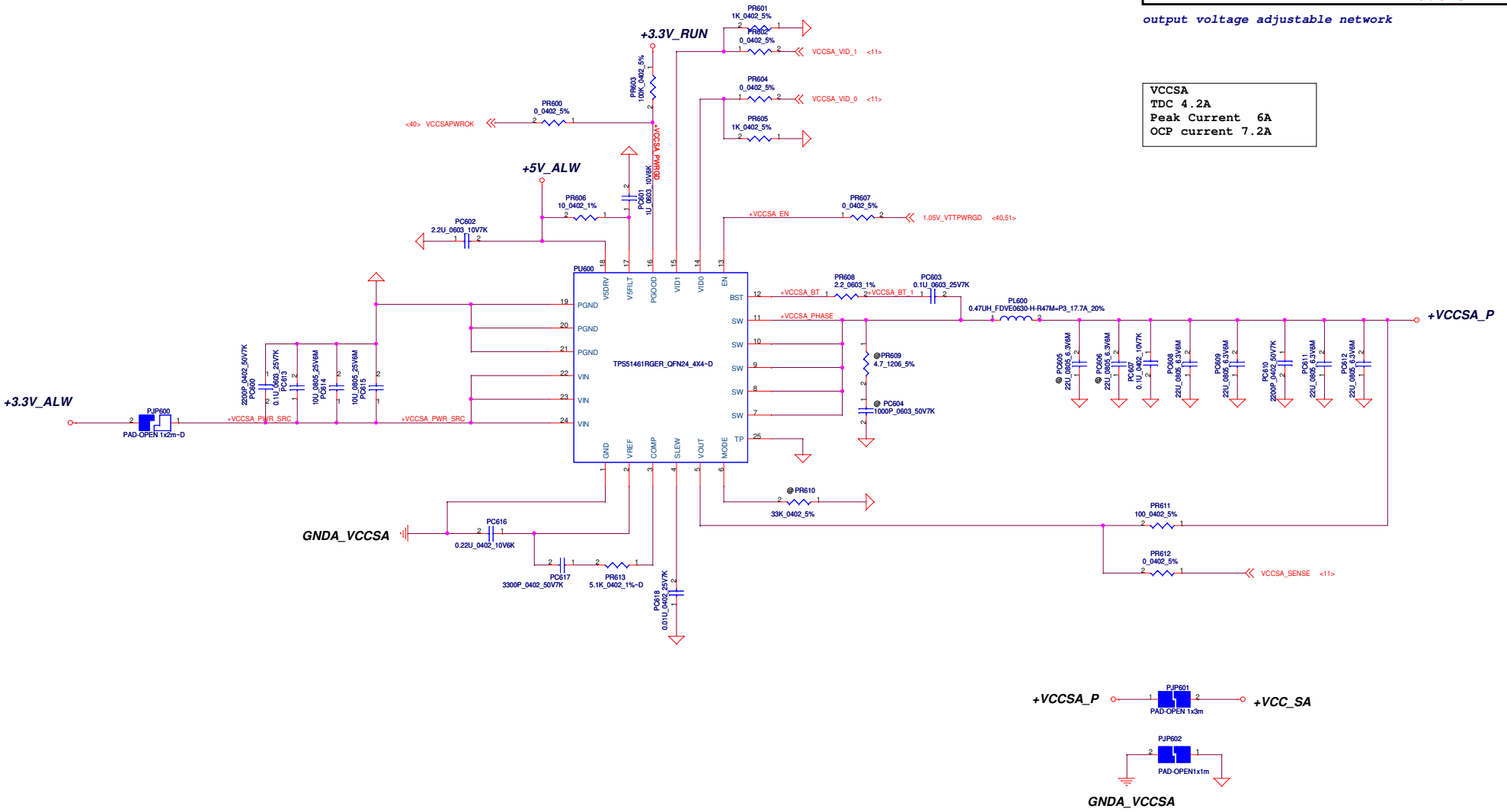
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: +VCC_SA

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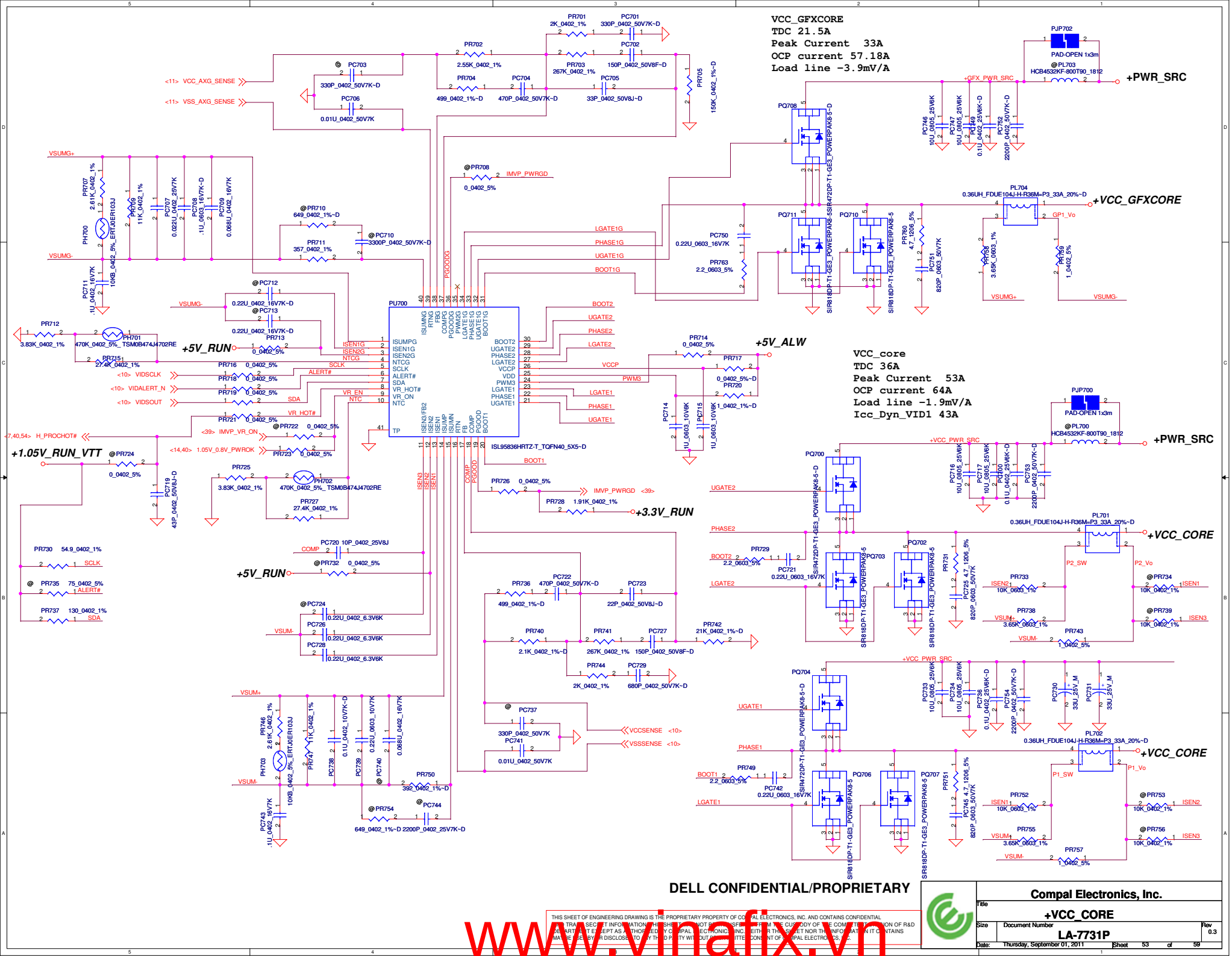
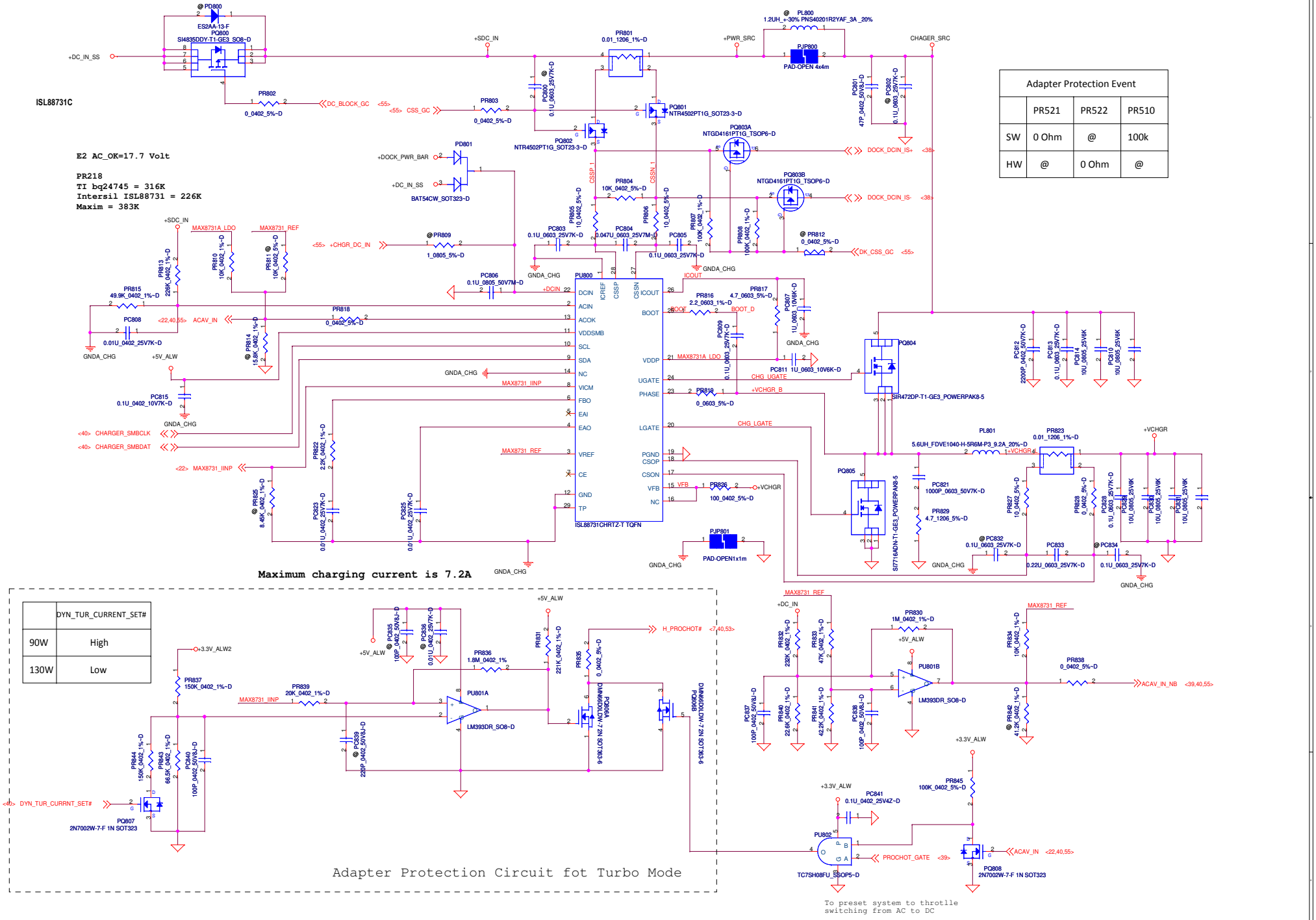
Date: Thursday, September 01, 2011 | Sheet 52 of 59





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Charger
Size	Document Number: LA-7731P
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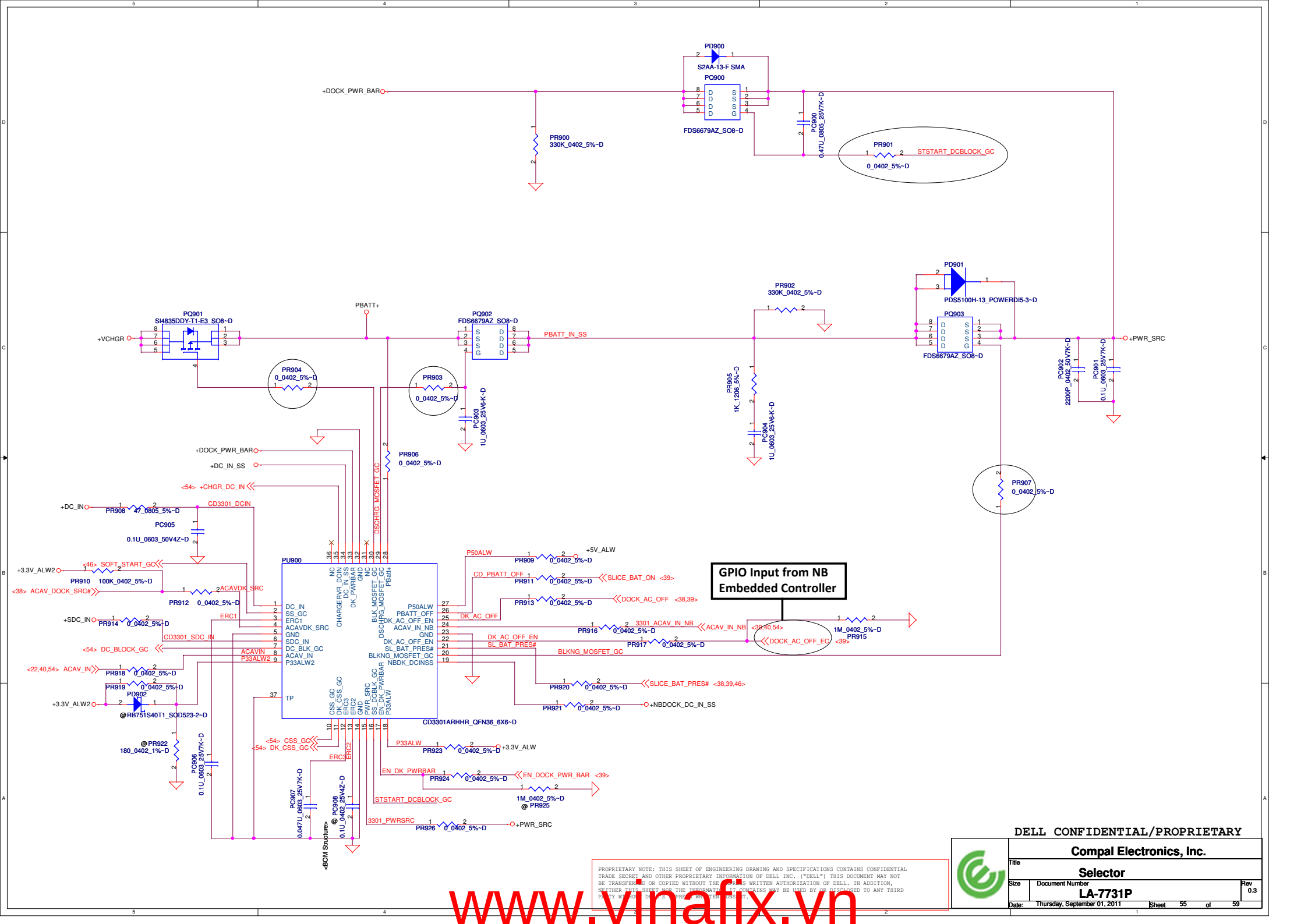
Date: Thursday, September 01, 2011	Sheet 54 of 59



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Selector

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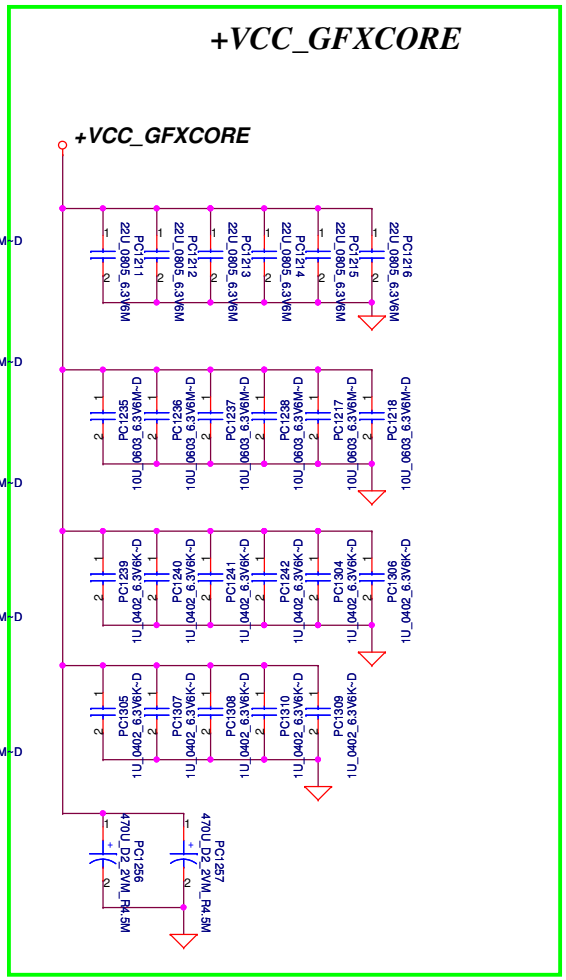
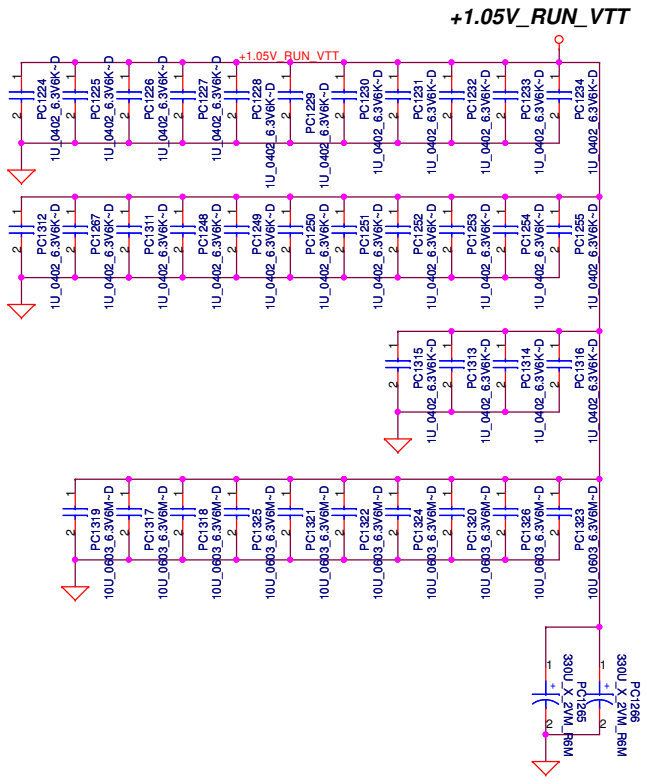
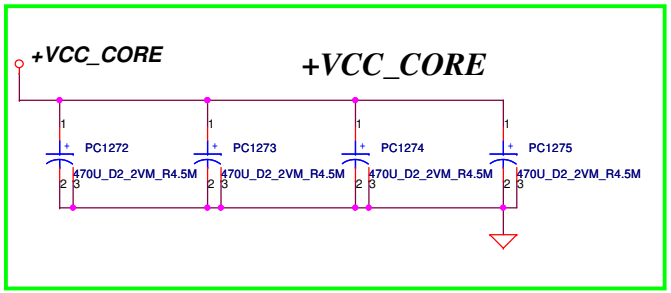


Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: PROCESSOR DECOUPLING		
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48	+1.5V_MEN	8/16	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	46	DCIN	8/16	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	47	+5V/3.3V	8/16	Dell	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	53	Vcore/GFX core	8/16	Compal RF_team	Suppress WWAN BB noise.	Pop PC751,PR760,PC725,PR731, PC745,PR751(680pF 0603, 4.7 ohm 1206)	X01
5	50 51	+1.05VM/ +1.05VTT	8/16	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC406, PC507	X01
6	53	Vcore/GFX core	8/16	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
7	47,53 ,54	Vcore, Charger +5V/3.3V	8/16	Compal RF_team	EMI solution.	Pop PL700.PL1300,PL100	X01
8	53	Vcore/GFX core	8/16	Compal	adjust OCP and DC load line.	PR740 change to 2.1k ohm, PR750 change to 392 ohm.	X01
9							X01
10							X01
11							X01
12							X01

Compal Electronics, Inc.

Title: PWR_PIR 1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39,40,42	HW	7/14/2011	DELL	E4 uses SIO_SLP_S4# for power control	Add @R752, R753	X01
2	11	HW	7/14/2011	Compal	Change DDR channel A signal to DSL	Add CC149,CC152,CC178,CC179	X01
3	18	HW	7/26/2011	DELL	Follow GPIO map rev1.0	Change RH273 from 1k to 10k	X01
4	29	HW	7/26/2011	Compal	EMI request	Pop CE981, CE982, CE983	X01
5	35	HW	7/26/2011	Compal	Solve Express card PAID issue	Add R830	X01
6	7,22	HW	7/27/2011	Compal	Solve ESD issue	Reserve D84,D85	X01
7	25	HW	7/27/2011	Compal	Layout routing	Swap HDMI trace connection on L19,L20,L21,L22 for layout routing	X01
8	29	HW	7/28/2011	Compal	EMI request	Add CE984,CE985	X01
9	7	HW	8/1/2011	Compal	EMI request	Reserve CC141	X01
10	17	HW	8/3/2011	Intel	Request from Intel review feedback	Pop RH332	X01
11	14,39	HW	8/4/2011	SMSC	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
12	20,42	HW	8/4/2011	Compal	Vgs less than cut-in voltage in battery mode	Add QH6,RH279,CH107	X01
13	42	HW	8/4/2011	Compal	Load SW sources output rising time mismatch and COS. cost concern.	Change back to E3 +3.3V/5V_RUN discrete solution. Add Q55,Q56,Q61,Q62,R933,R940,R1627, remove U78,R749,R747, C1199,C1198,C1197,C1196,change C761,C764 to 10uF	X01
14	10	HW	8/4/2011	Compal	Follow INTEL PDDG 0.8	De-pop RC140	X01
15	32	HW	8/4/2011	Compal	RESET_OUT# power sequence issue	Add R1653, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
16	40	HW	8/4/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
17	34	HW	8/4/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
18	23	HW	8/4/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
19	16	HW	8/4/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5 circuit for backup HW solution	X01
20	41	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
21	29	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642 Reserve for ALC290 only: C1204, C1205, R171, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963	X01
22	29	HW	8/4/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
23	40	HW	8/8/2011	COMPAL	Please depop VOL_MUTE/UP/DOWN due to EC code enable internal PU resistors (3V_ALW)	De-pop R1169,R1197,R1118	X01
24	41	HW	8/8/2011	COMPAL	For debug purpose	Add R1624	X01
25	42	HW	8/8/2011	COMPAL	power suggestion	Change Q59 to AO4728L	X01
26	43	HW	8/9/2011	COMPAL	Align with E4	Change LED6, LED7 power source from +3.3V_ALW to +5V_ALW	X01
27	14,40	HW	8/10/2011	COMPAL	Crystal EA result	Change C741, C743 from 22p to 39p, CH2, CH3 from 15p to 18p, CH18, CH19 from 12p to 10p for crystal EA	X01
28	41	HW	08/11/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
29	26	HW	08/11/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
30	43	HW	08/11/2011	COMPAL	Tune white light LED brightness	Change R934,R938,R939,R949,R958,R957 and R955 to 2.2K ohm	X01

Compal Electronics, Inc.

Title: EE P.I.R (1/2)

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
31	20,22,34 38,39,43	HW	8/11/2011	COMPAL	Cost saving	Change D2,D31,D32,D34,D59,D62,DH2,DH3, D65,D66,D67,D68,D69,D70 to SCS00002G00	X01
32	11	HW	8/12/2011	COMPAL	Solve S3 wake up issue	Pop RC79 and de-pop RC82	X01
33	36,41	HW	8/14/2011	ME	ME change connector	Change JUSB1,JUSB2,JBT1	X01
34	30	HW	8/16/2011	ME	ME change connector	Change JLID1	X01
35	17,32 39,40	HW	8/18/2011	COMPAL	RF request	Pop R885, C747, R795, C713, RE5 and change CE3 to 12pF and pop it, and add CH109,CH110	X01
36	36	HW	8/19/2011	COMPAL	Follow Intel design guide	Change C410~C413 from 0.01uF to 0.1uF	X01
37	25	HW	8/24/2011	COMPAL	EMI request to solve HDMI issue	Add C1216~C1223	X01
38	7	HW	8/25/2011	COMPAL	ESD request	Change RC25 to 1k and pop CC141	X01
39	40	HW	8/26/2011	SMSC	SMSC request	Reserve R941, R942	X01
40	24,33	HW	8/26/2011	EMI	EMI request to solve SD/DMIC issue	Reserve CE758, CE279, CE280	X01
41	43	HW	8/27/2011	ME	Solve standoff shift issue	Change H11,H24,H25 to 6mm	X01
42	43	HW	8/29/2011	COMPAL	Tune white light LED brightness	Change R934,R938,R939,R949,R958,R957 and R955 to 1.2K ohm	X01
42	14	HW	8/29/2011	ME	change TAA connector	Change JTAA1	X01

Compal Electronics, Inc.
Title: EE P.I.R (2/2)
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