Commercial AMD Rembrandt ORS

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Title	Cover Page	LCFC	
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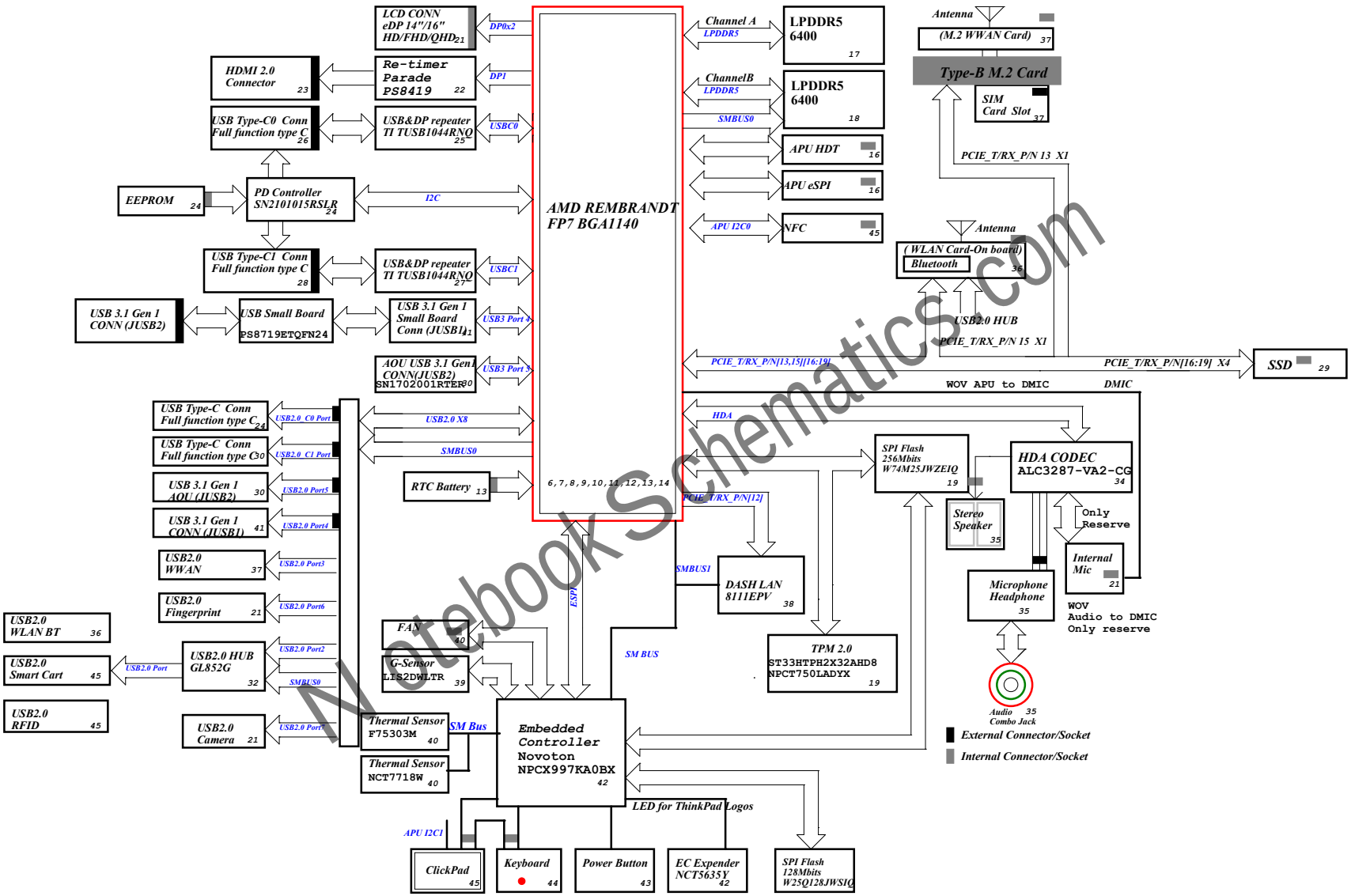

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Title: Block Diagram_EE

LCFC

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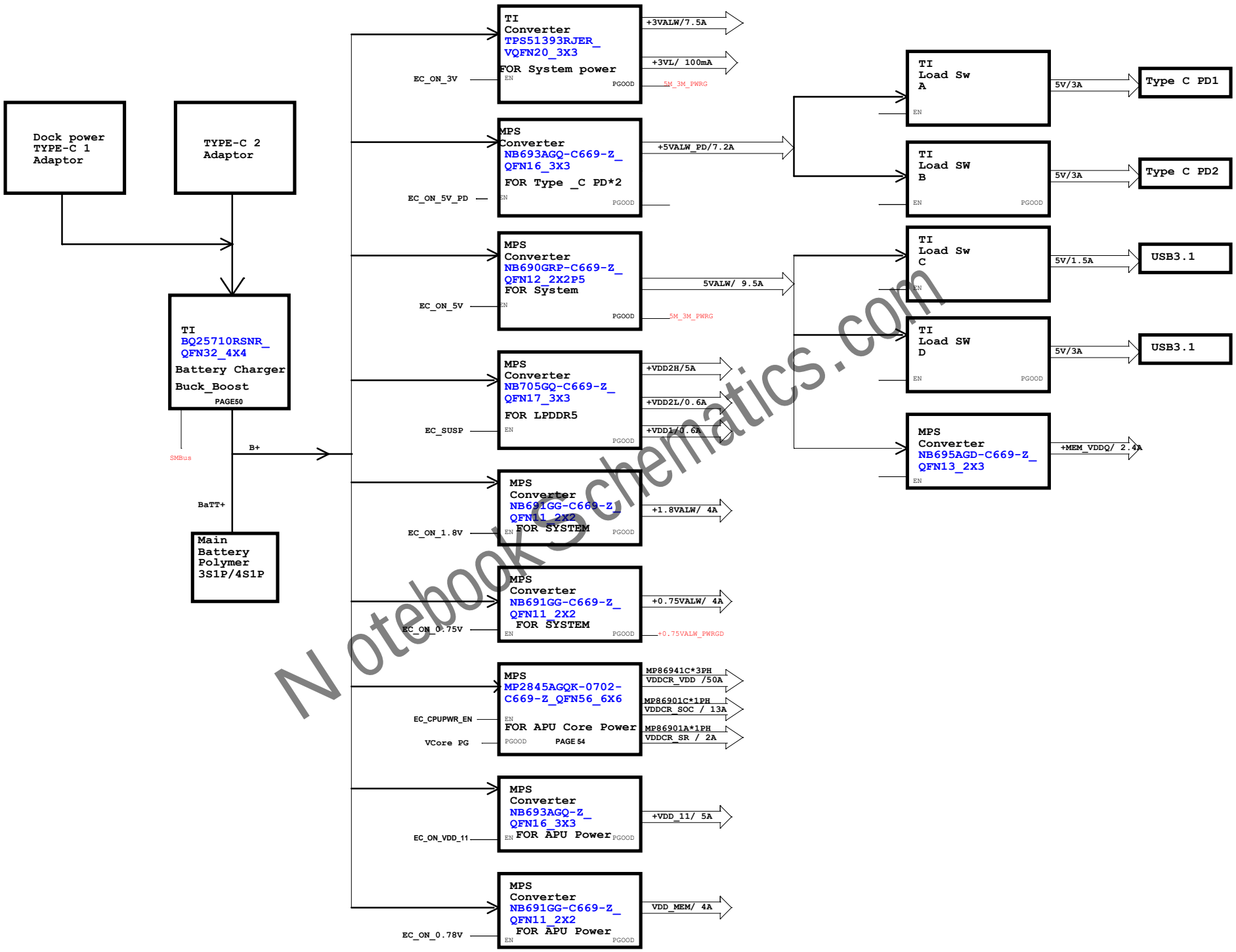

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Title: Block Diagram_PWR

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PD I2C address table

Port	Master	Slave	End Port	Address	Description
I2C_EC	EC	PD	PORTA	0x23	ADCIN1=0.1079#2 ; ADCIN2=1#7 ADCIN1 decoded value = 2 ADCIN2 decoded value = 7 I2C address index = #4 A port: 0100011 B port: 0100111
			PORTB	0x27	
I2C2S	APU	PD	PORTA	0x23	Confirm with Max
			PORTB	0x27	
I2C3M	PD	APU	USBC0	0x5C	The USB PD I2C Slave responds to a 7-bit address.
			USBC1	0x52	
	PD	EEPROM	EEPROM	0x50	
	PD	Redriver-C0	Redriver-C0		[GPIO1,GPIO0] : LL=0x10; LH=0x20; HL=0x30; HH=0x40;
		Redriver-C1	Redriver-C1		

EC I2C address table

Port	Master	Slave	End Port	Address	Description
SDA1A SCL1A	EC	P sensor	P sensor	0x44	The I2C device has a 7 bit Slave Address (default 0x44H) in the control byte
SDA2A SCL2A	EC	Expander1	Expander1		The I2C slave address is {0011A2,A1,A0,R/W} Address:0011000R/W
	EC	Expander2	Expander2		Address:0011001R/W
	EC	Expander3	Expander3		Address:0011010R/W
	EC	Expander4	Expander4		Address:0011011R/W
SDA2B SCL2B	EC	HDMI	HDMI	0x10 - 0x2F	
	EC	APU	APU Thermal	0x98	confirm with David Liu
SDA3A SCL3A	EC	VRM	VRM	0x20	To support multiple VR devices used with the same PMBusTM interface, PMBusTM address programming either by ADDR
	EC	CHARGER	CHARGER	0x12	The device performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus.
	EC	Battery	Battery	0x16	Confirm with Luodi
SDA4A SCL4A	EC	TS 1	TS 1	0x4D	1001_101xb
	EC	TS 2	TS 2 (SMBUS)	0x4C	NCT7718W I2C/ SMBusTM address is 1001100xb
	EC	G sensor	G sensor (I2C)	0x18(ST) 0x18(BOSCH)	The Slave Address (SAD) associated to the LIS2DWL is 001100xb where the x bit is modified by the SA0/SDO pin in order to modify the device address (0x1000)
SDA5A SCL5A	APU	PD	PD	N/A	Refer to PD table
SDA6A SCL6A	EC	TYPEA Port Debug	TYPEA		
	EC	TYPEC Port Debug	TYPEC		

APU I2C address table

Port	Master	Slave	End Port	Address	Description
I2C0	APU	PD	PORTA	0x23	Confirm with Max
			PORTB	0x27	
		NFC	NFC	0x29	
I2C1	APU	T_PANEL	T_PANEL	0x10 ELAN 0x34 Melfas 0x39 Raydium	
I2C2	APU	CP	CP	0x15	I2C device address: 0x15
	APU	USB Hub	USB Hub	0x2C	
I2C3 (SMBUS)	APU	TYPEC0 REDRIVE	TYPEC	PS8828:0X10~0X23 PS8830:0X10	
	APU	TYPEC1 REDRIVE	TYPEC	PS8828:0X90~0XD3 PS8830:0X40	
SFH_I2C	APU	G-Sensor1#	G-Sensor	0011001b	
	APU	G-Sensor2#	G-Sensor	0011000b	

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Title: Map/SMBUS/HSIO

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Title	Notes_For BOM	LCFC
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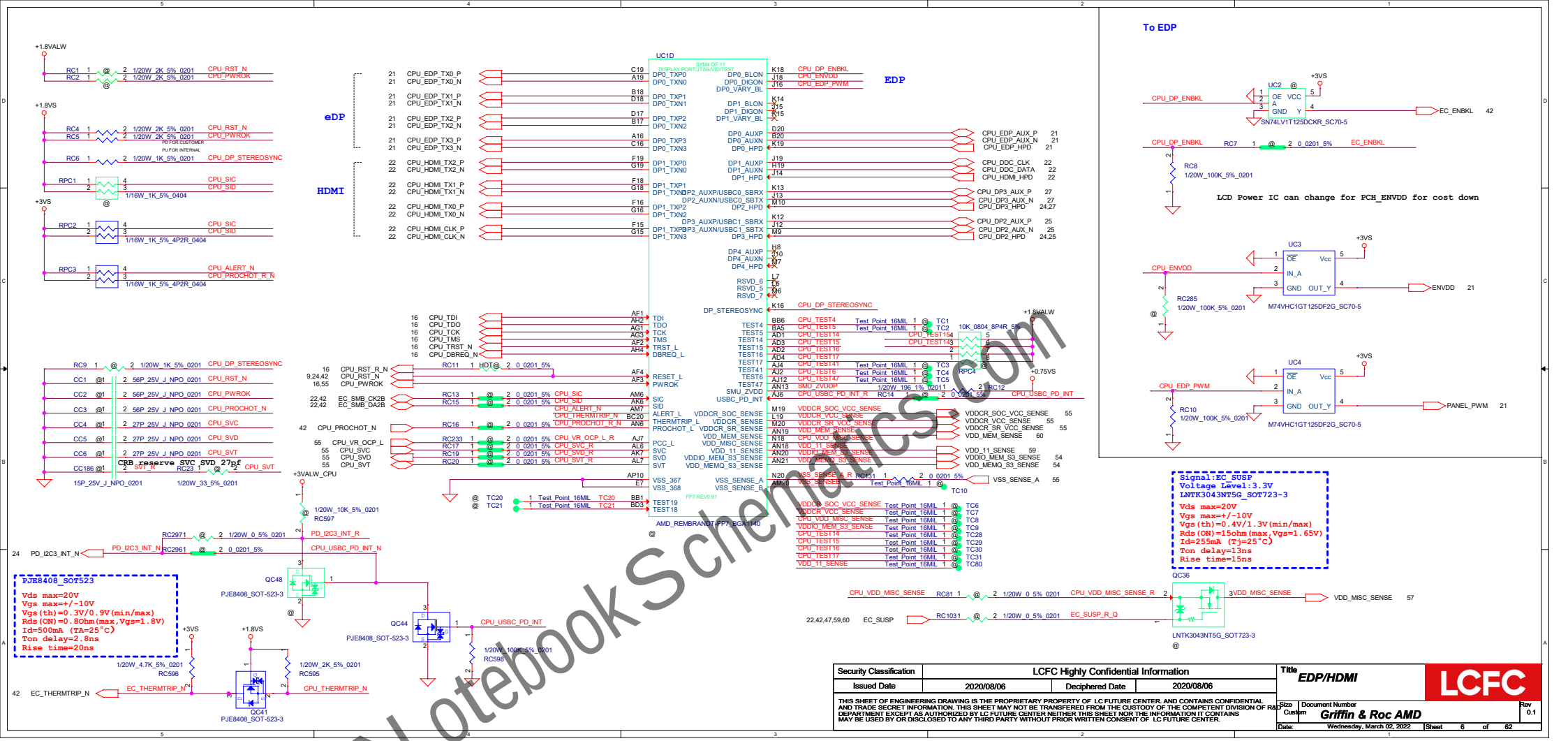

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Title: EDP/HDMI

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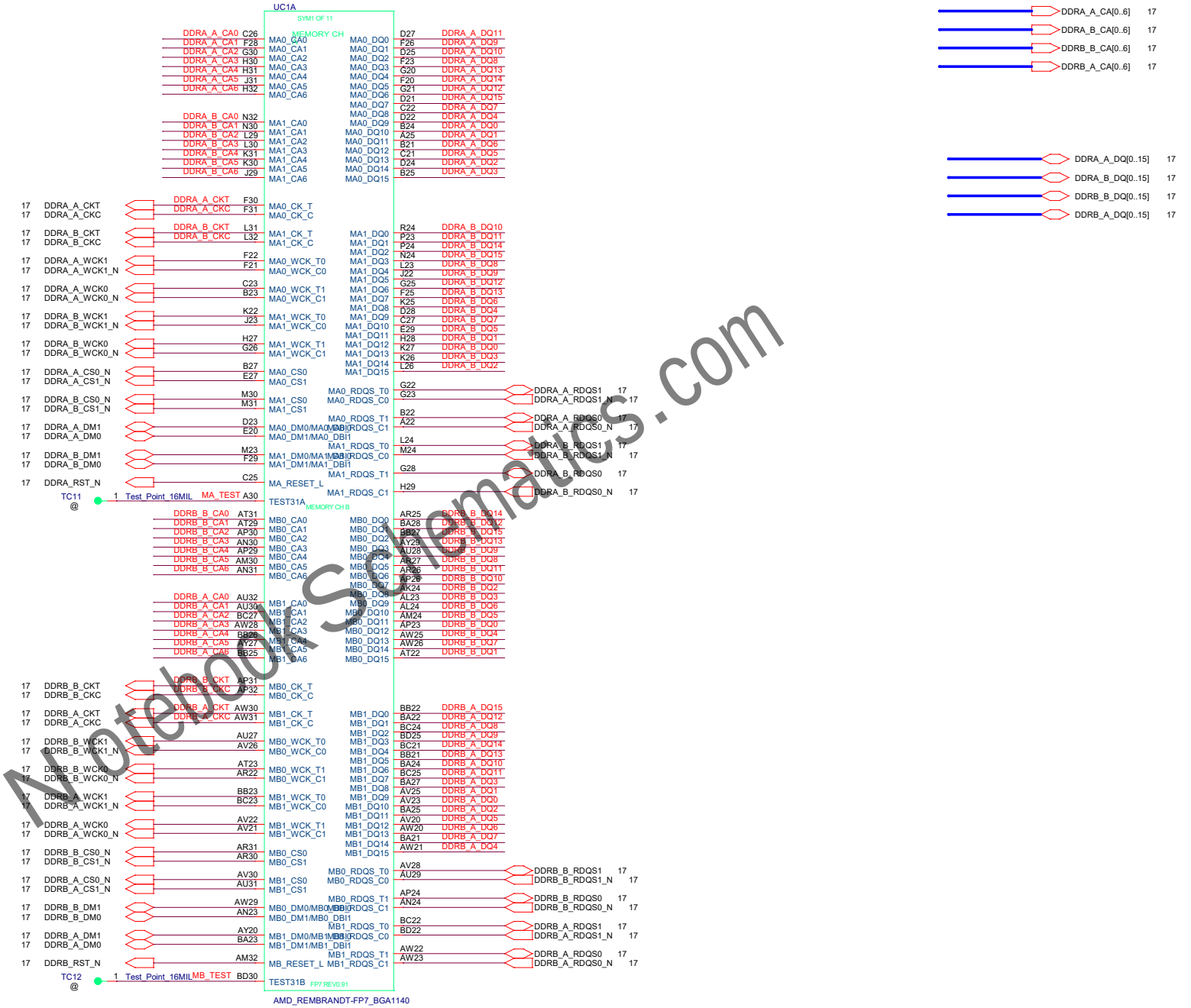

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *LPDDR5-CHA*

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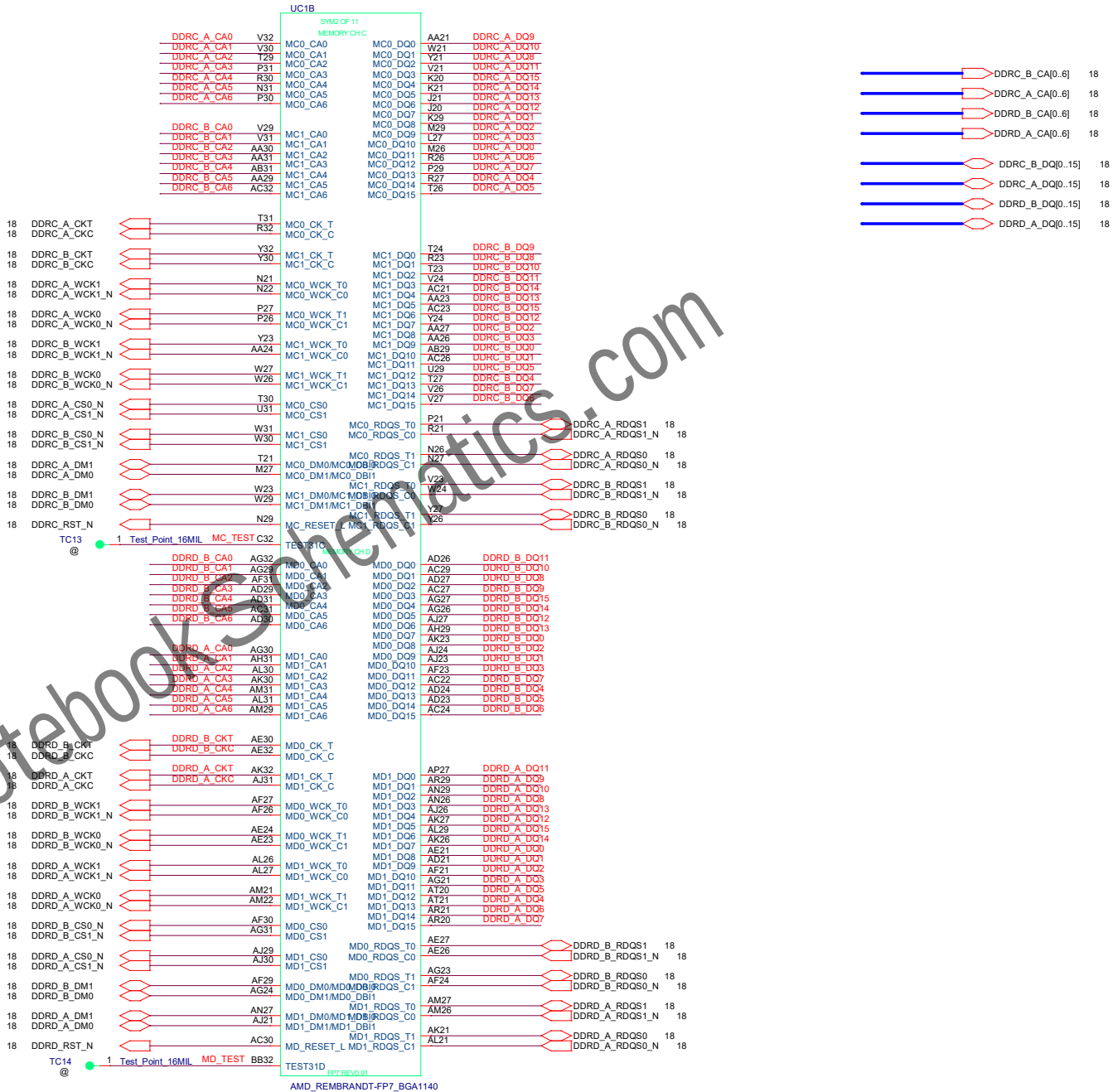

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *LPDDR5-CHB*

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STRAP PINS	Description
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET_L	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

48MHz/10pF Crystal

PJT7838
Vds max=30V
Vgs max=+/-20V
Vgs(th)=0.5V/1.0V(min/max)
Rds(ON)=6ohm(max,Vgs=1.8V)
Id=400mA (TA=25°C)
Ton delay=2.3ns
Rise time=20ns

EPRIVACY Enable:High Voltage 2.5V
level shift IC max VOH=2.3V not enough

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Title: SPI/CLK/LPC/UART

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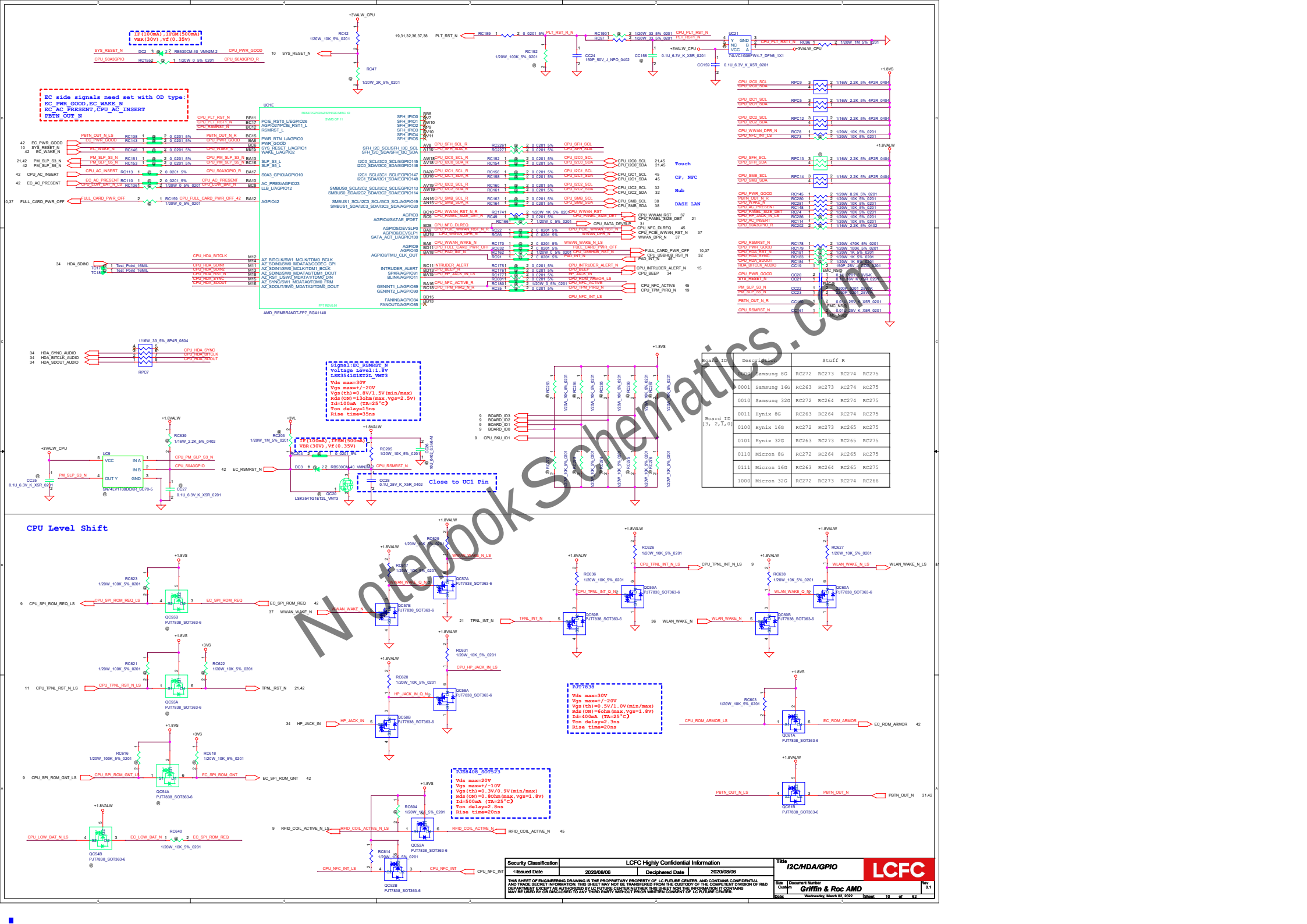

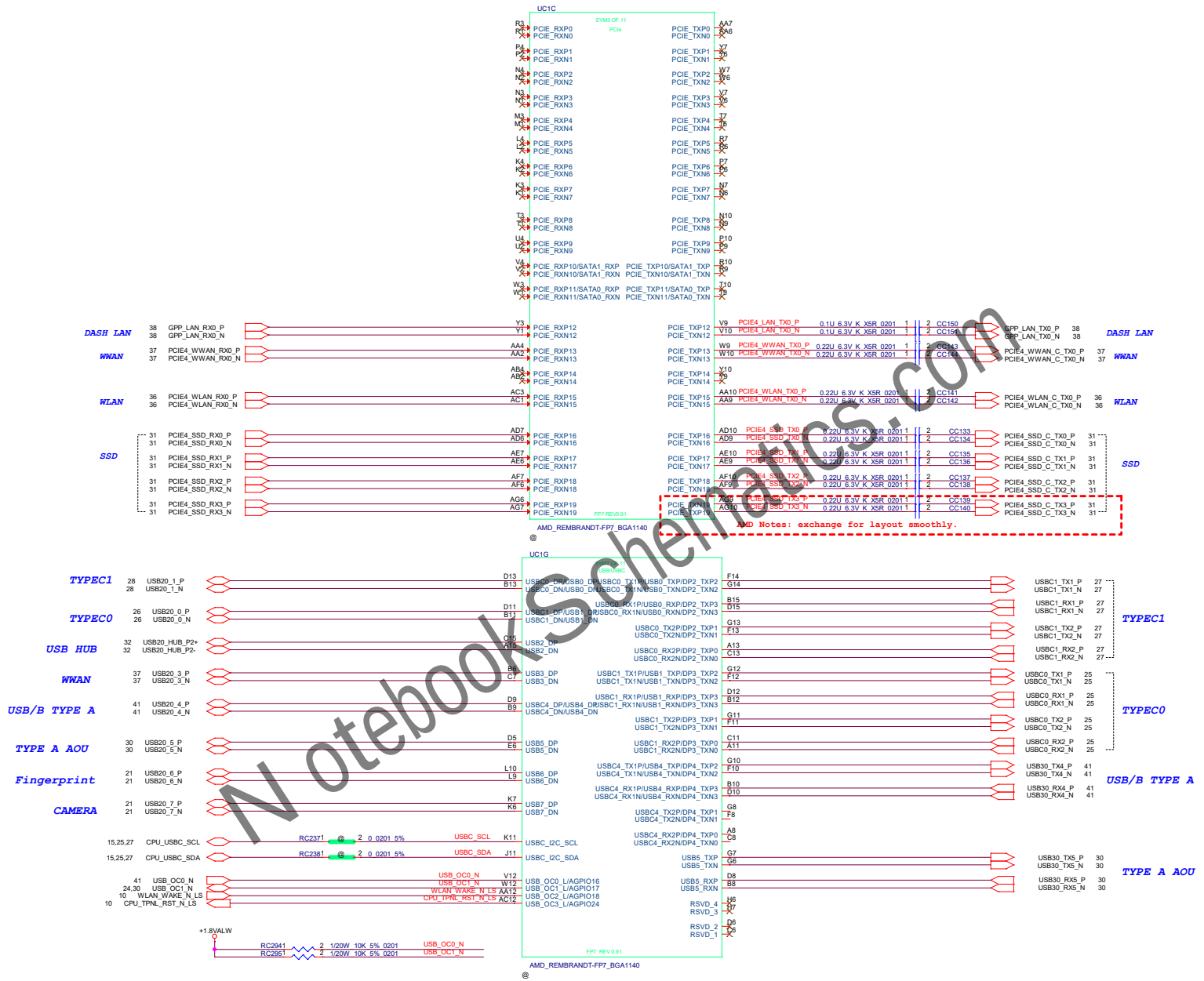

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Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PCIE/USB

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Title: *WIFIBT/CAM*

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Size	Document Number	Rev
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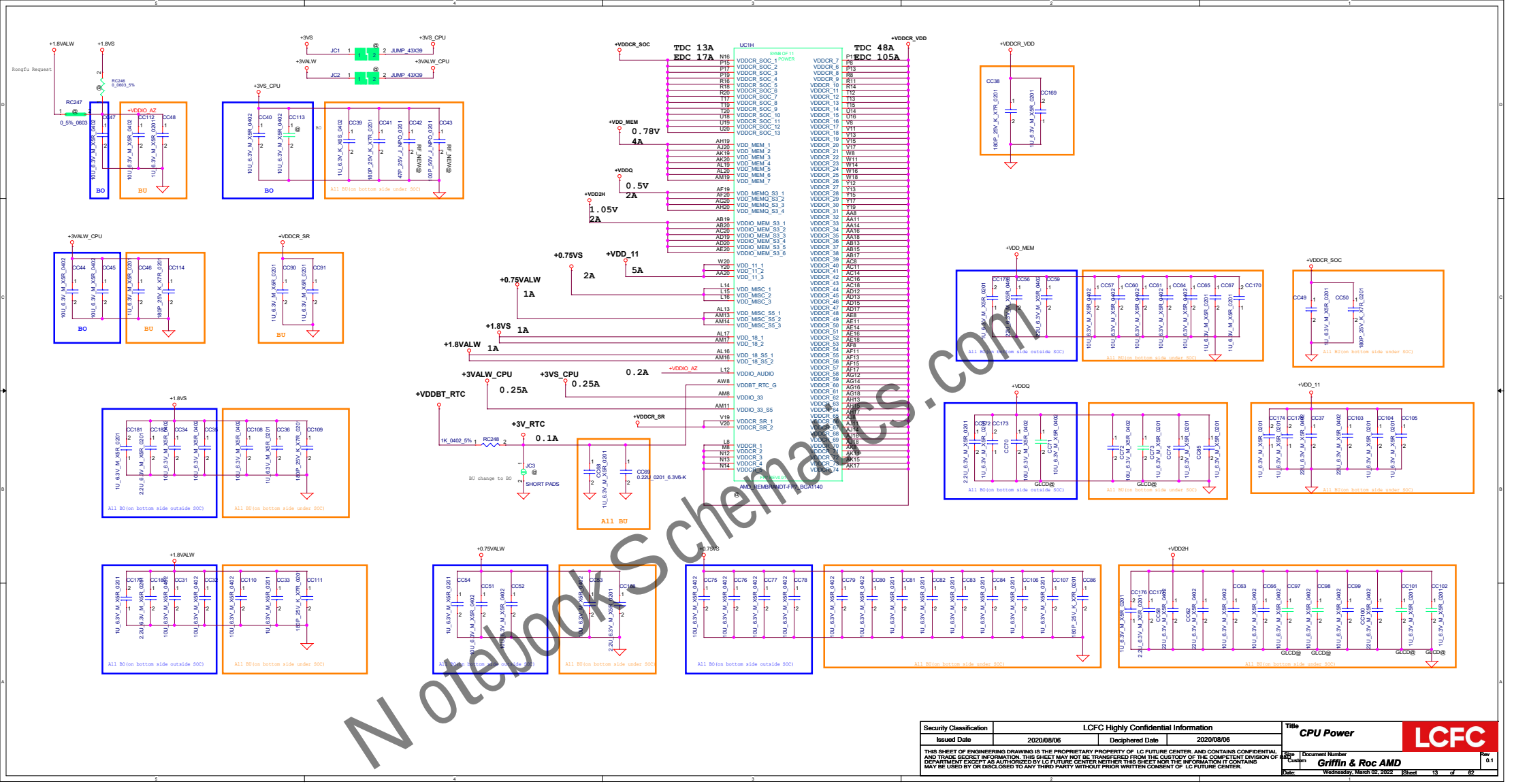

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: CPU Power

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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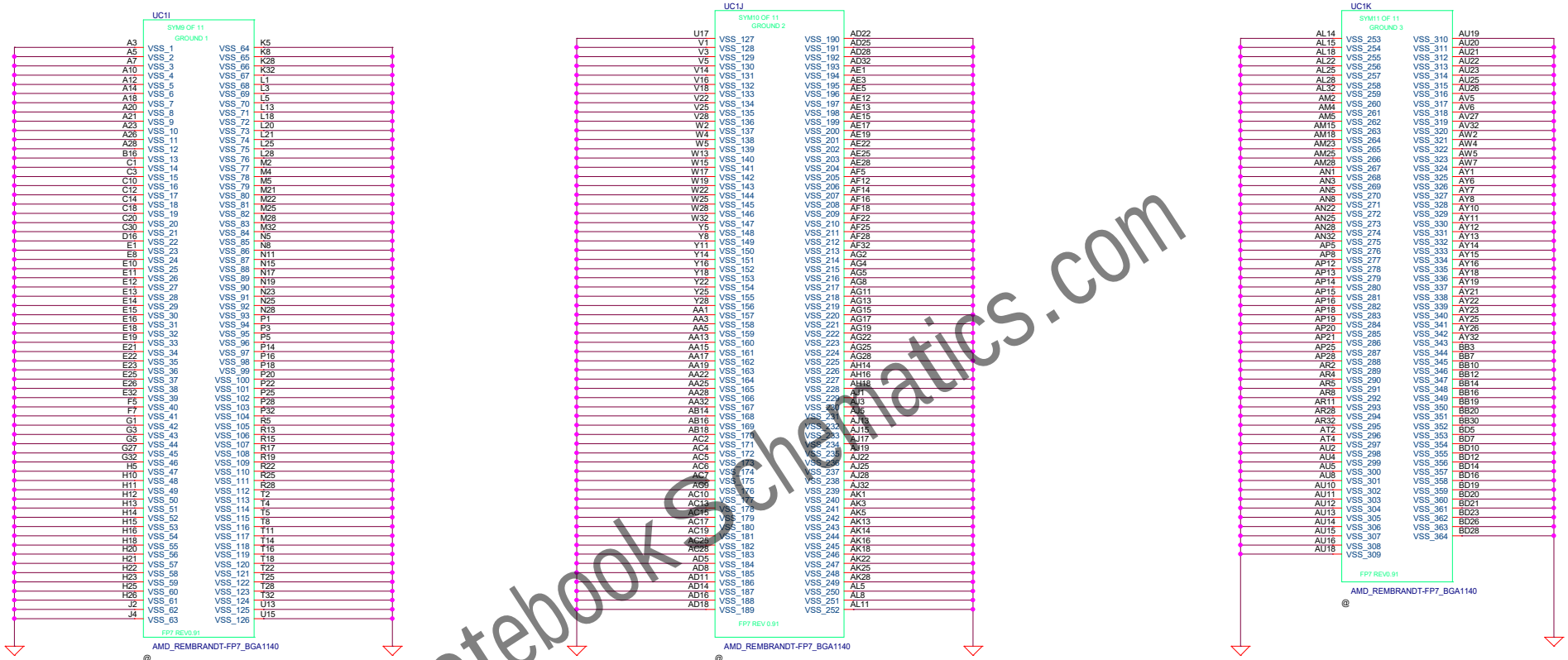

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *GND*

LCFC

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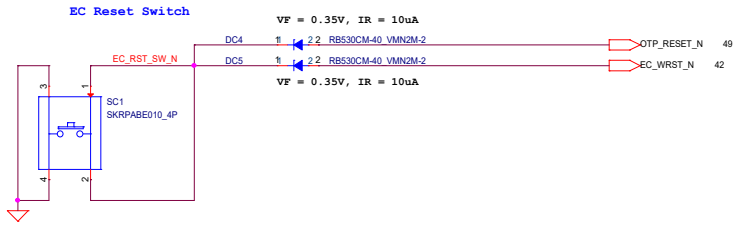

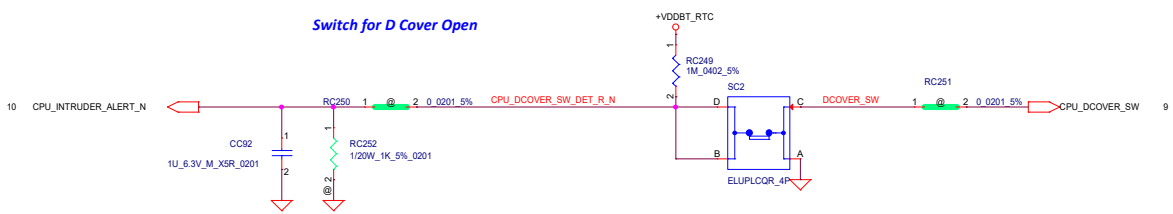

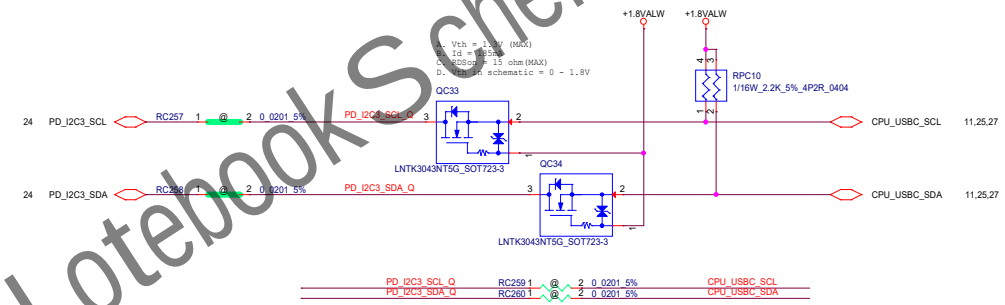

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Title: SMBUS/SW

LCFC

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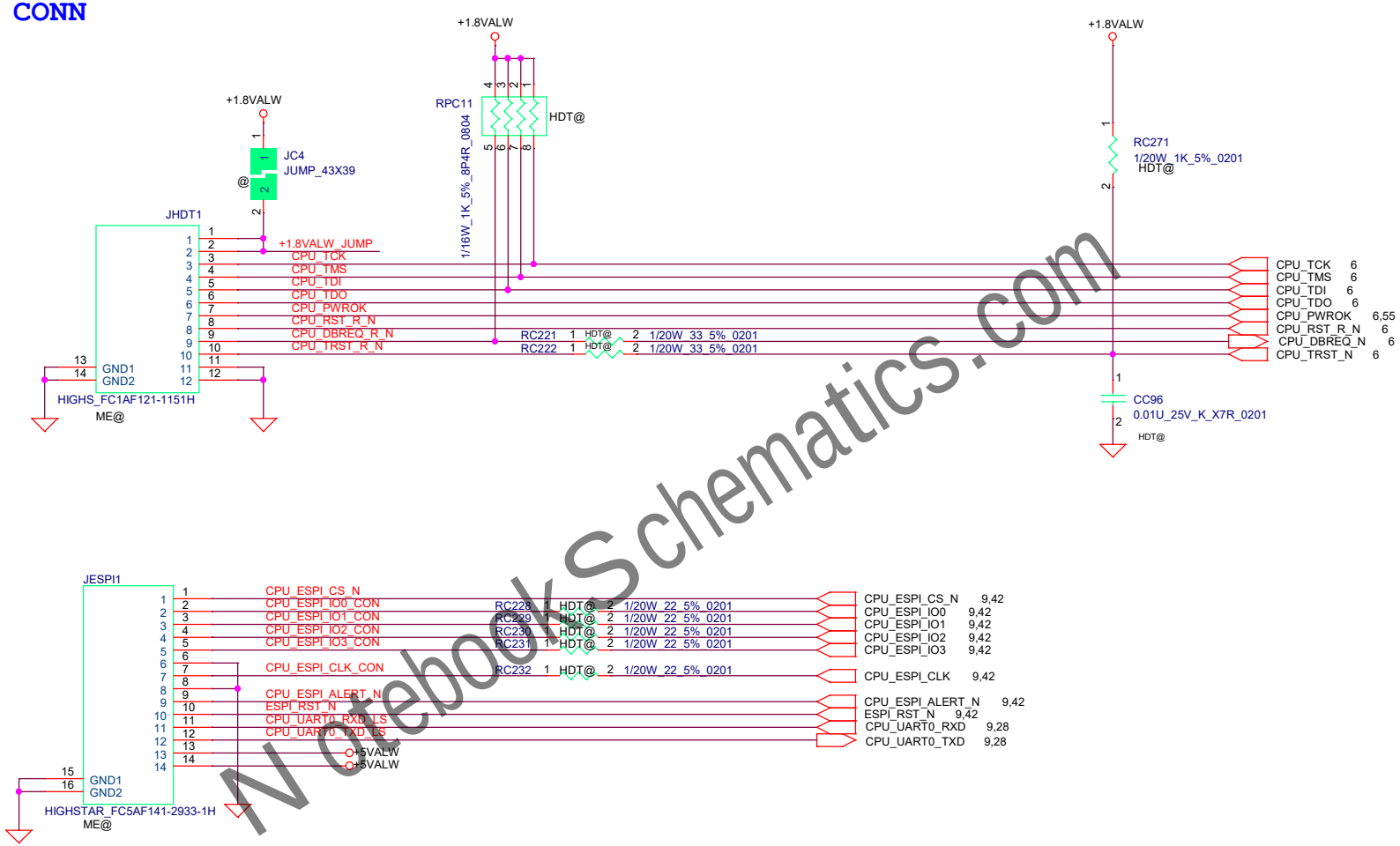
Debug CONN



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	HDT/eSPI Debug		LCFC
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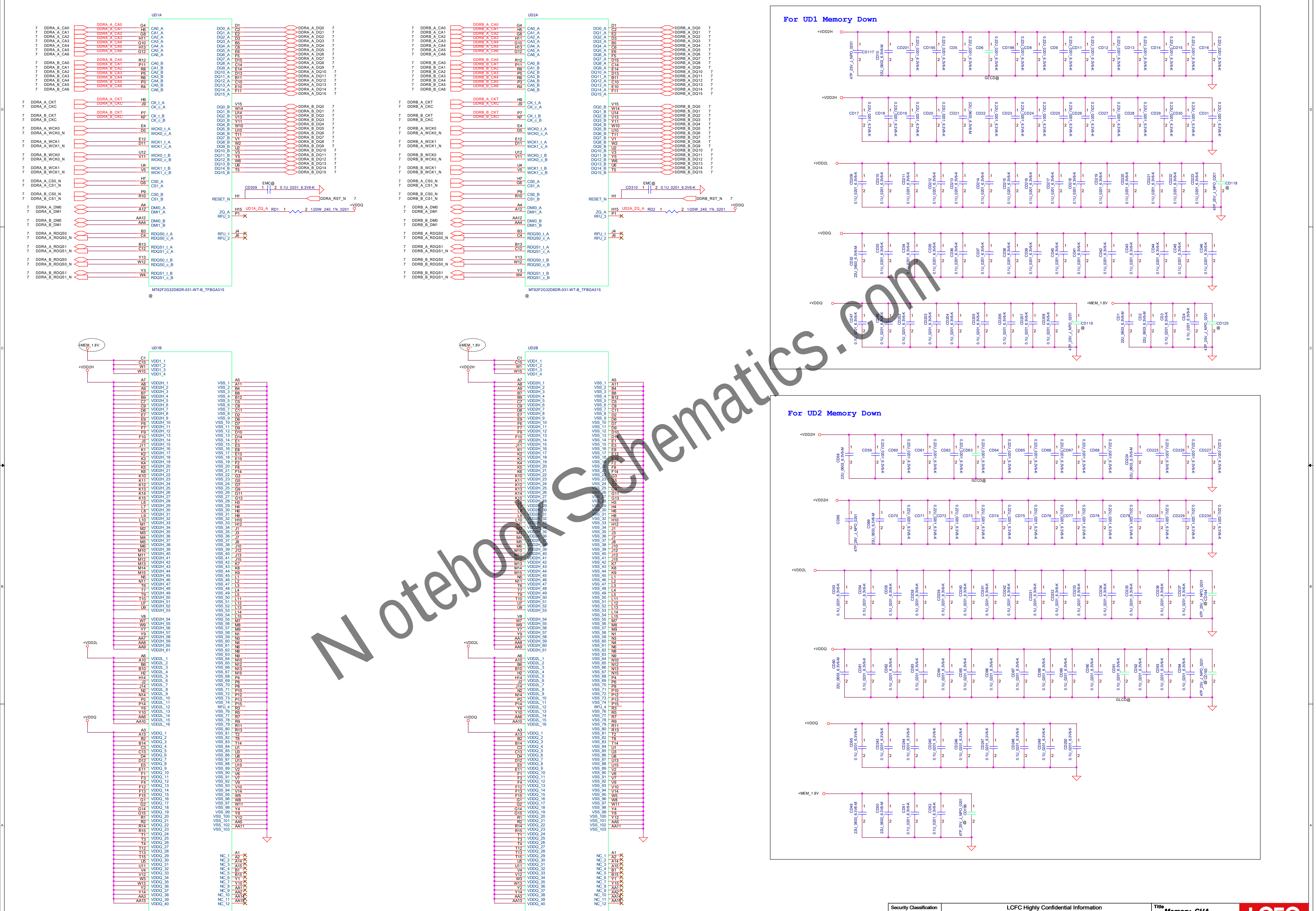

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Title: Memory_CHA

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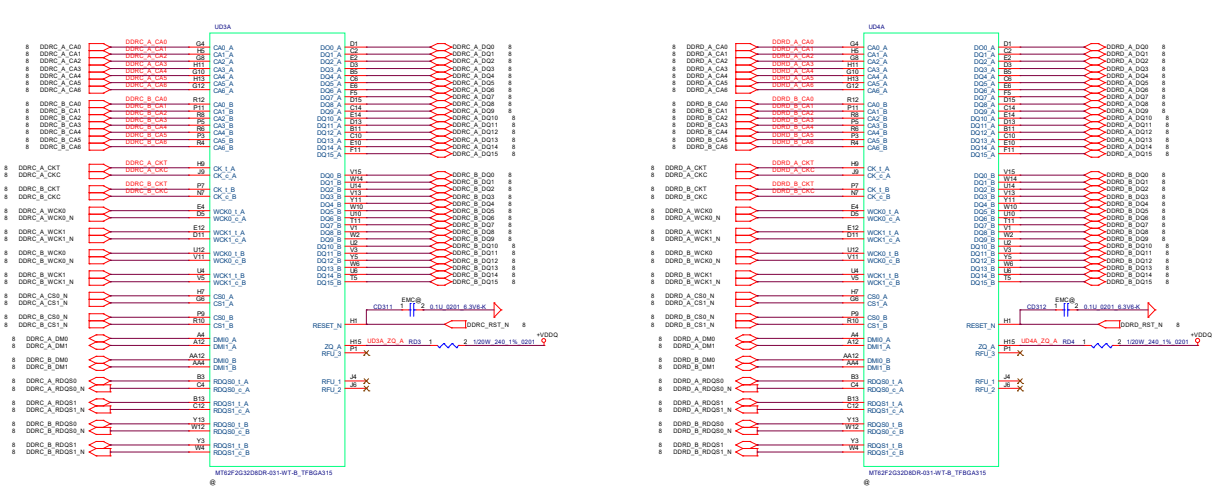

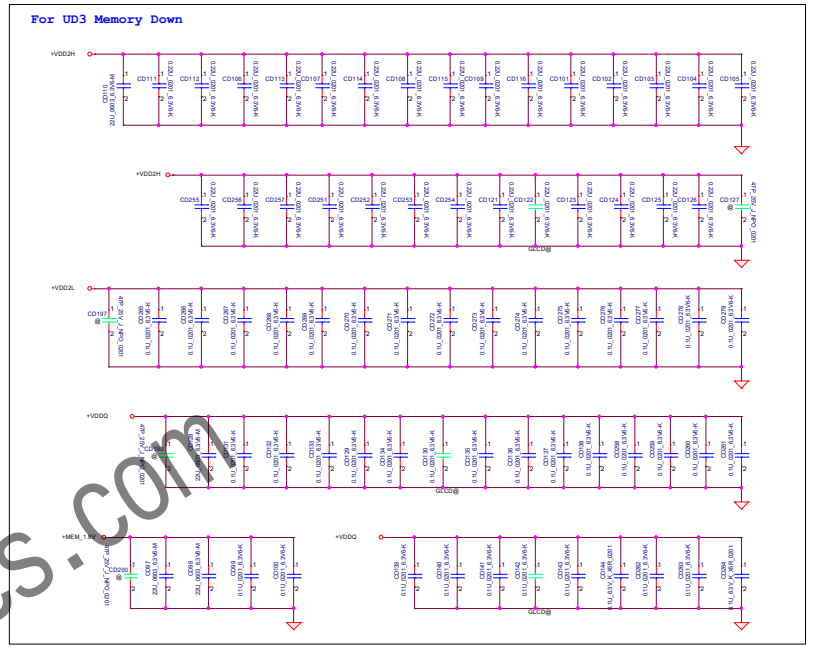

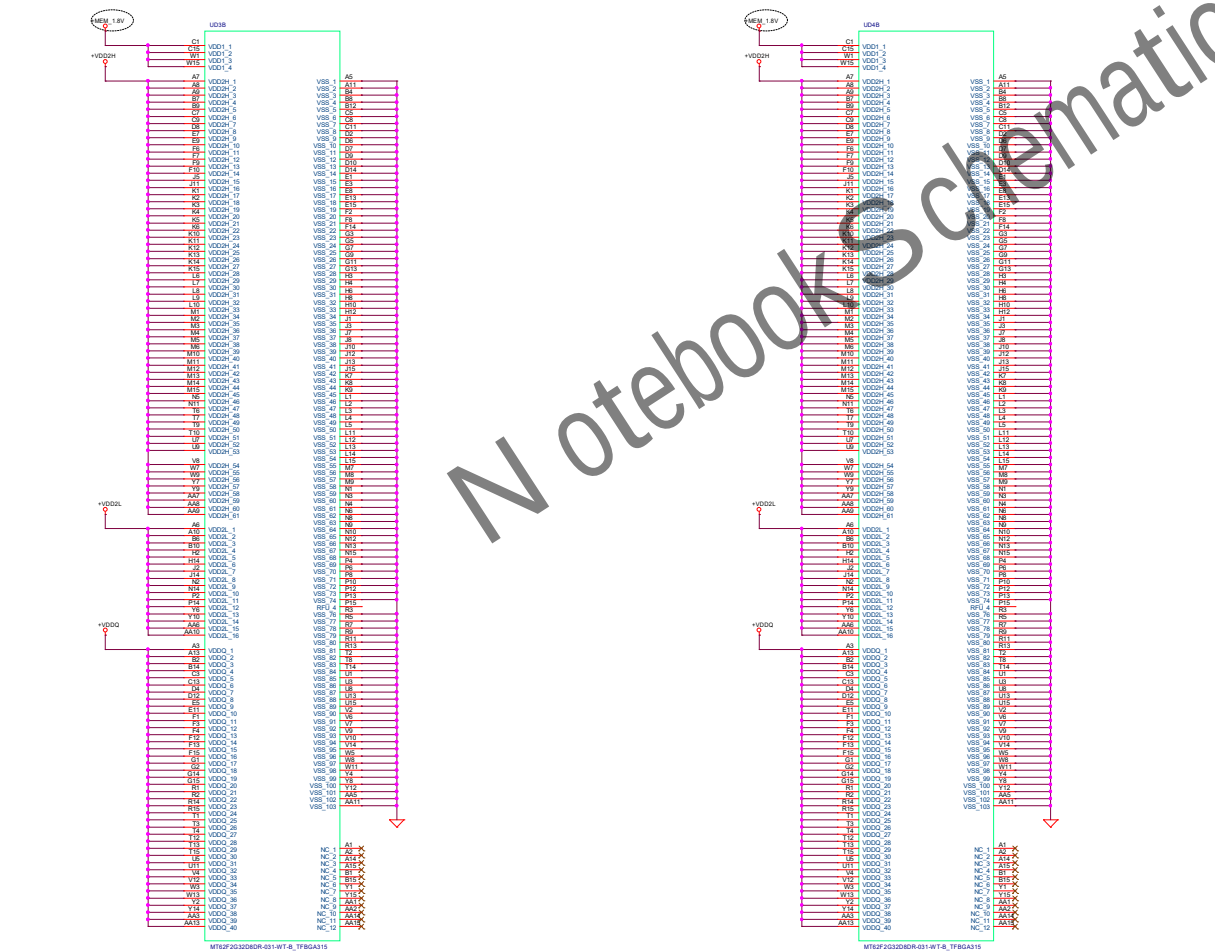

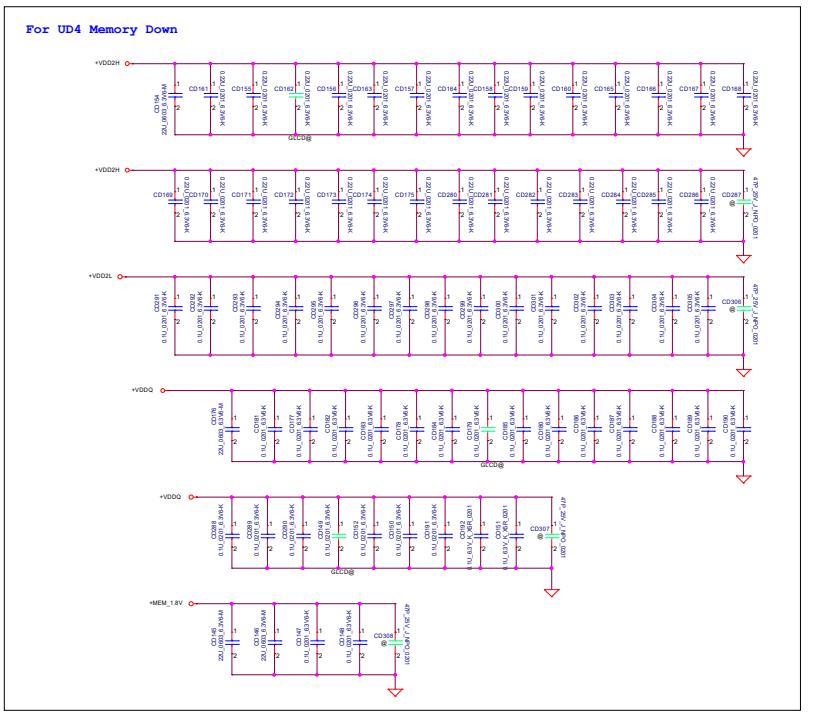

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Title	Memory_CHB	LCFC	
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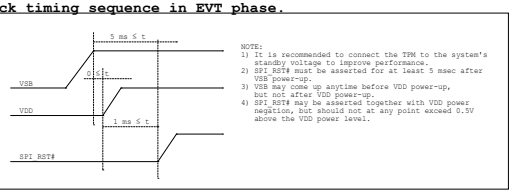
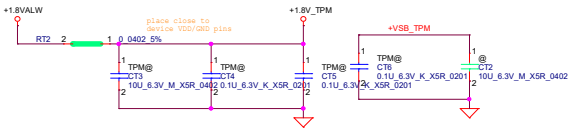
TABLE of TPM		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT760LAAYX	SA0000C3000
ST Micro	ST33HTPH2X32AHE0	SA0000C8600
INFINEON	9672VU2.0 FW15.21	SA0000CNZ00

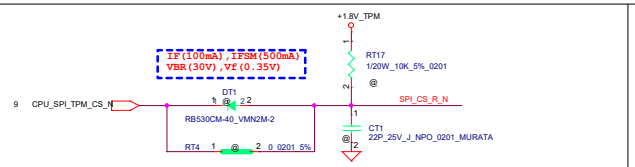
NOTE:
Check timing sequence in EVT phase.



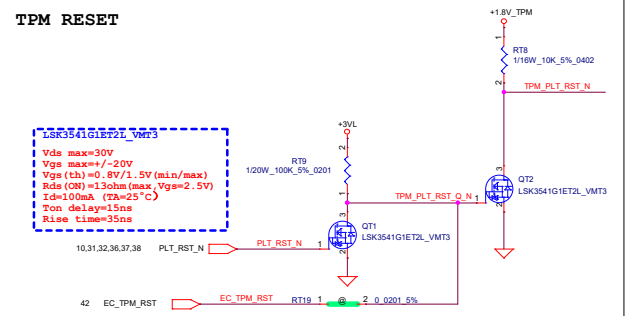
TABLE

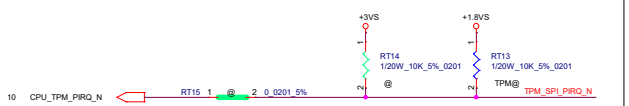
Pin No	Nuvoton NPCT760LAAYX	ST Micro ST33HTPH2X32AHE0	INFINEON SLB9670VQ2.0FW7.85
1	VSB	NiC	NCI/VDD
2	NC	GND	GND
3	NC	NiC	NCI
4	GPIO/PP	NiC	NCI
5	NC	NiC	NCI
6	GPIO3	GPIO_LP	GPIO
7	NC	GPIO_PP	PP
8	VHIO	NiC	VDD
9			
10	NC	NiC	GND
11	NC	NiC	NCI
12	NC	NiC	NCI
13	NC	NiC	NCI
14	GPIO4	NiC	NCI
15	NC	NiC	NCI/VDD
16	NC	NiC	NCI
	GND	NiC	NCI/VDD
17			
18	RLTRST#	SPI_RST#	RST#
19	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
20	SCLK	SPI_CLK	SCLK
21	SCS#/GPIO5	SPI_CS#	CS#
22	MOSI/GPIO7	MOSI	MOSI
23	VHIO	VPS	VDD
24	GND	NiC	GND
	MISO	MISO	MISO
25			
26	NC	NiC	NCI
27	NC	NiC	NCI
28	NC	NiC	NCI
29	NC	NiC	NCI
30	SDA/GPIO0	NiC	NC
31	SCL/GPIO1	NiC	NC
32	NC	NiC	NCI
	NC	NiC	GND

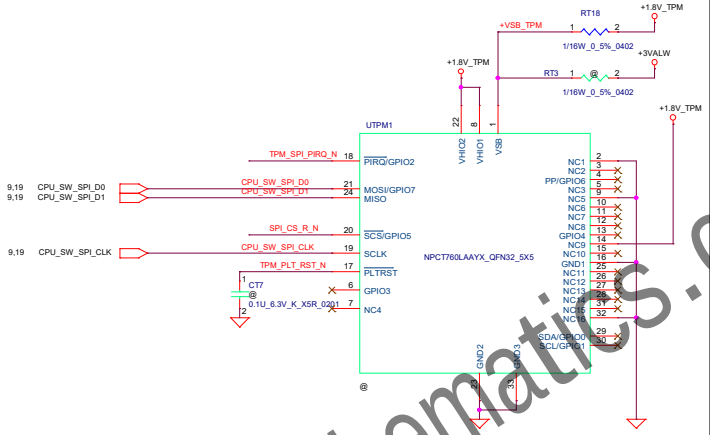




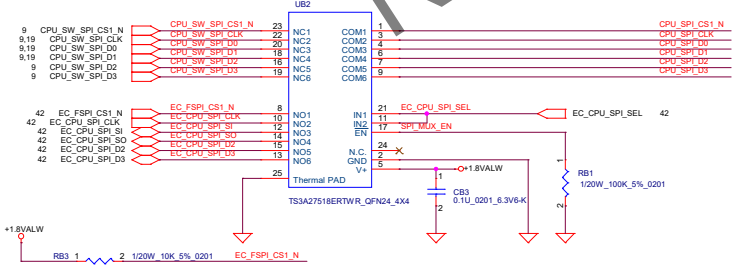
TPM RESET

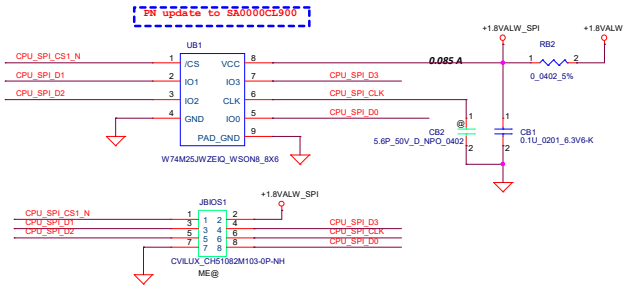






SPI SWITCH





EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

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Title: *SPI ROM/TPM*

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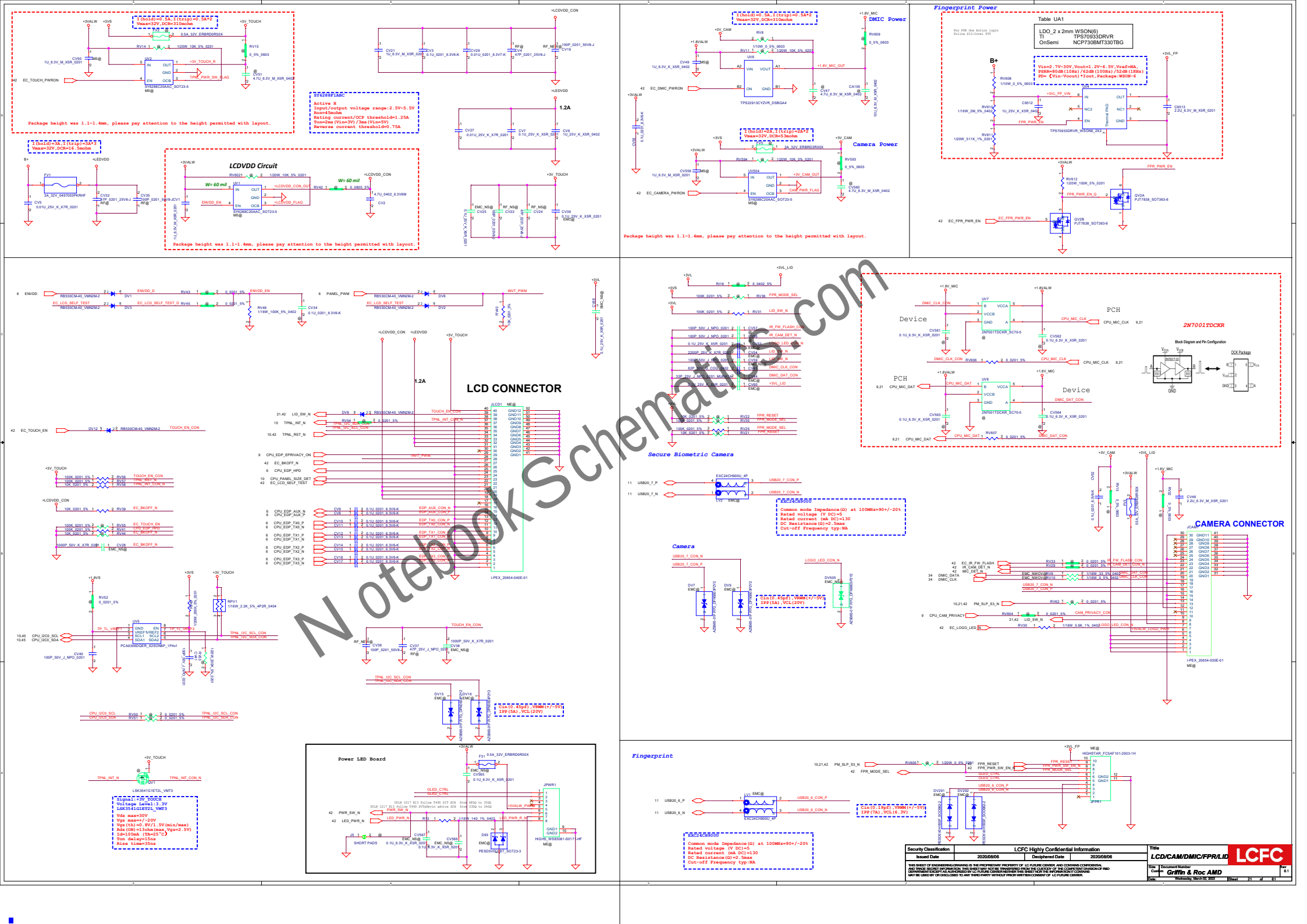

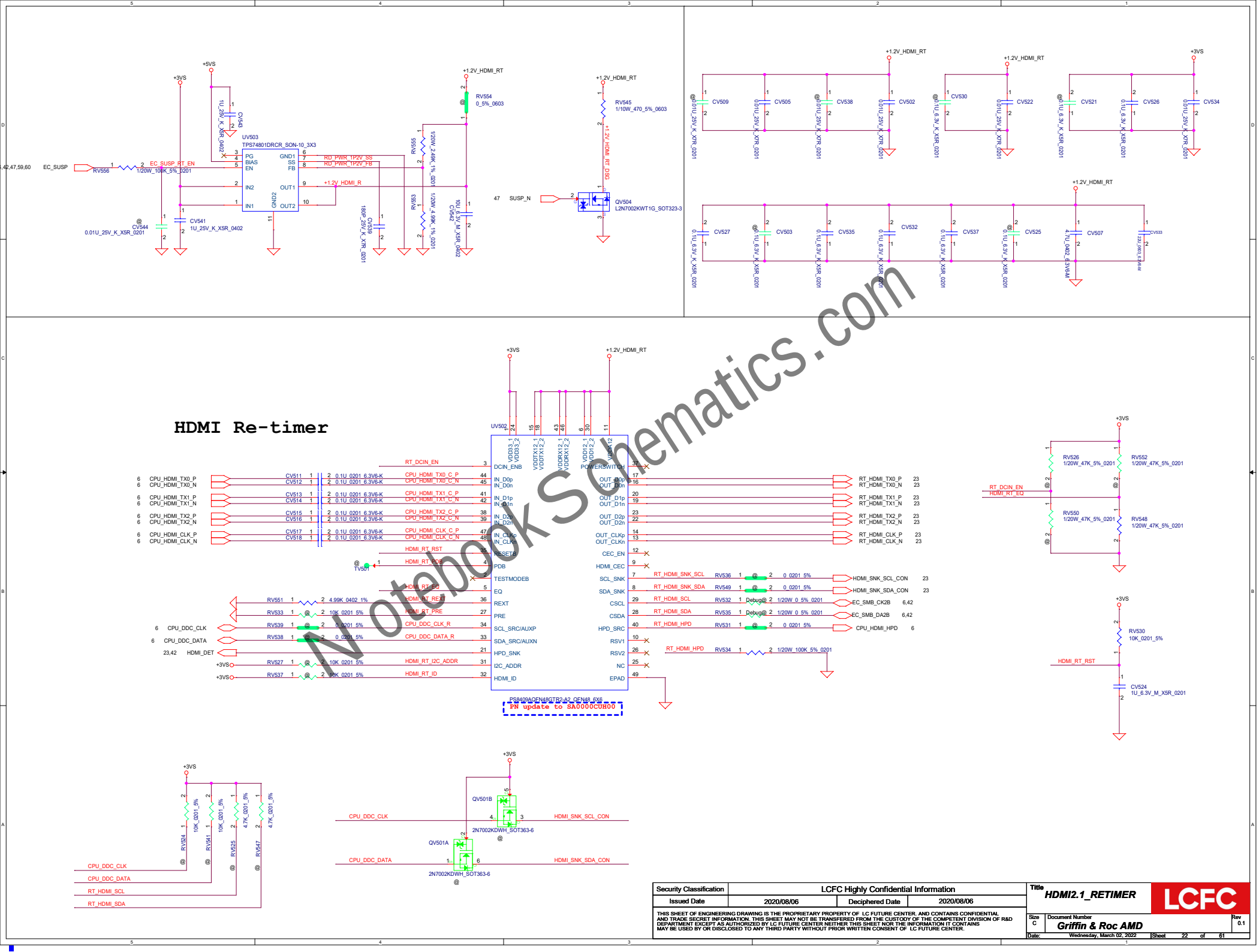

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Title: HDMI2.1_RETIMER

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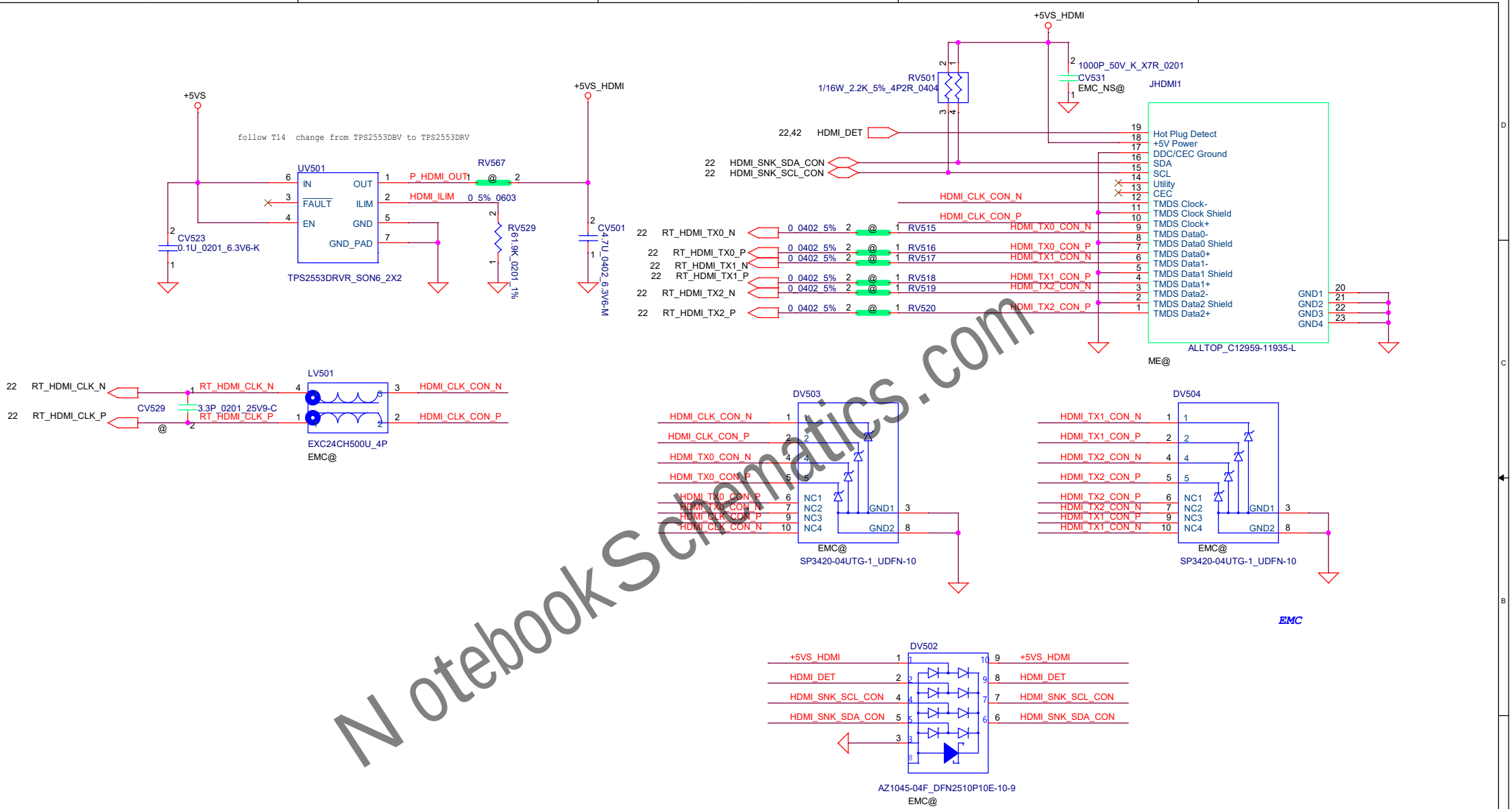

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Title: HDMI_CONN

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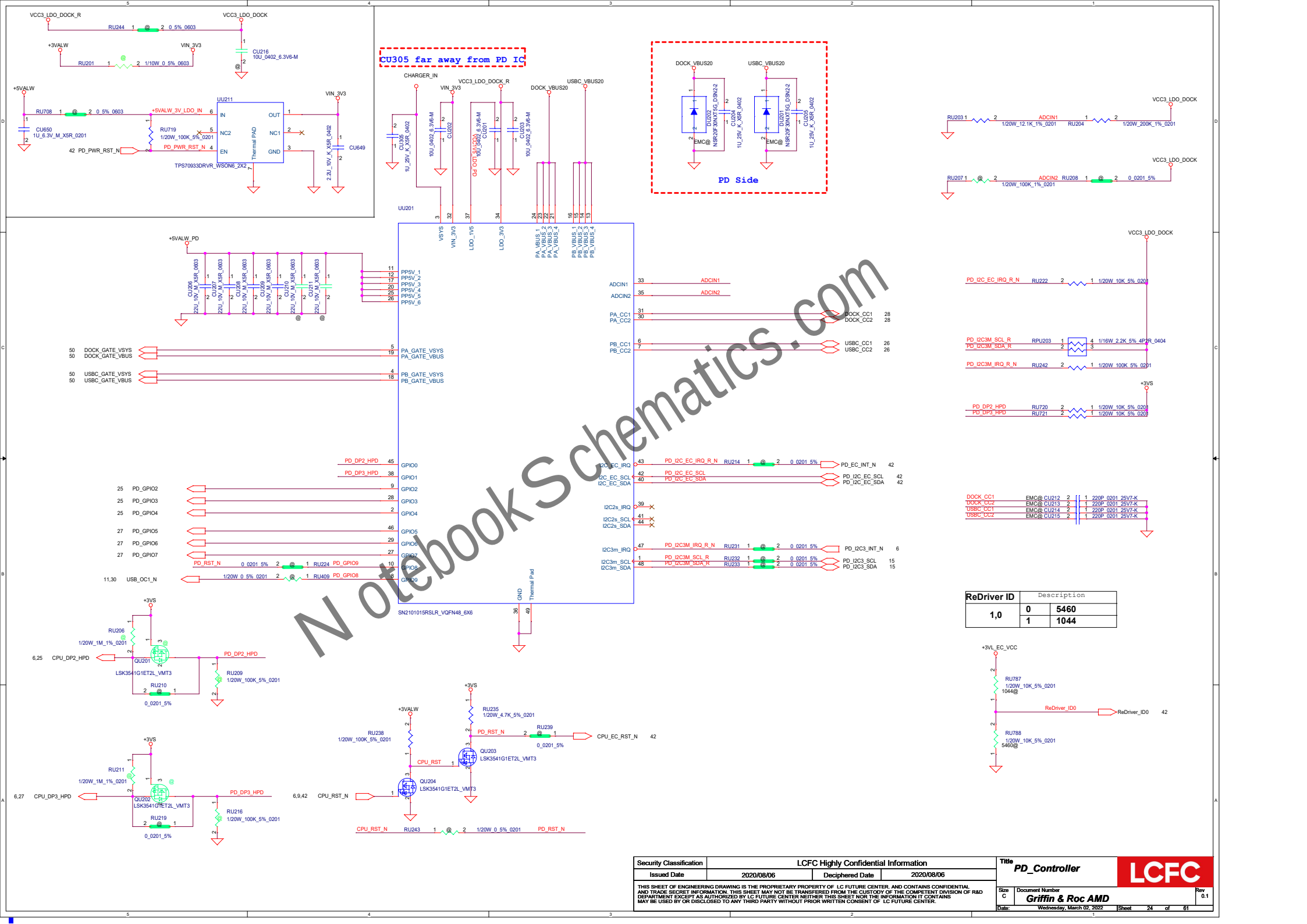


ReDriver ID	Description	
1,0	0	5460
	1	1044

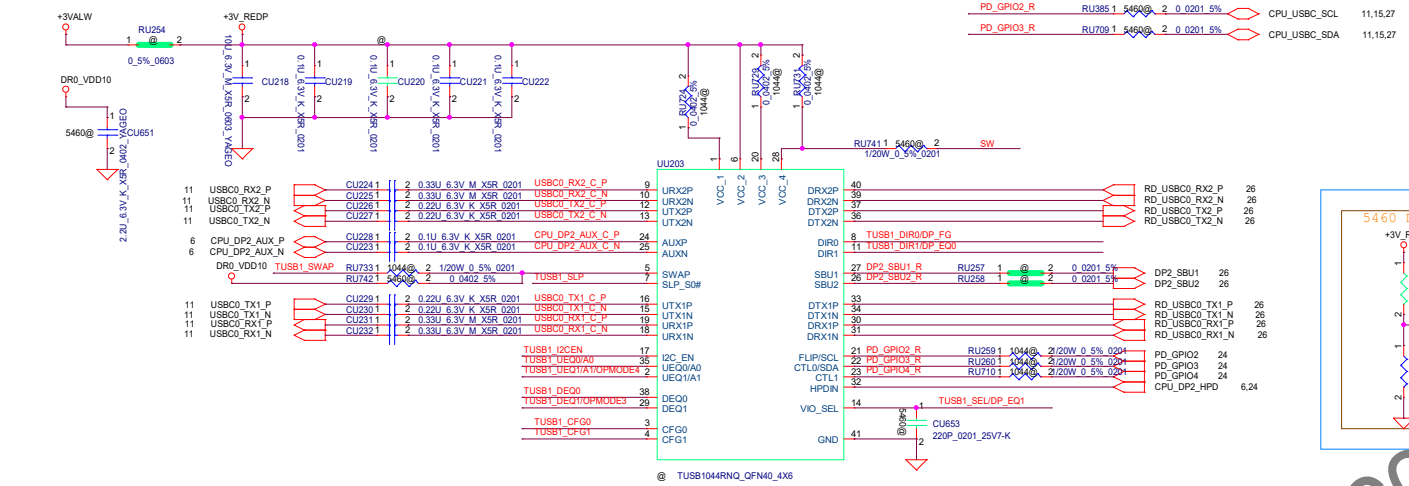
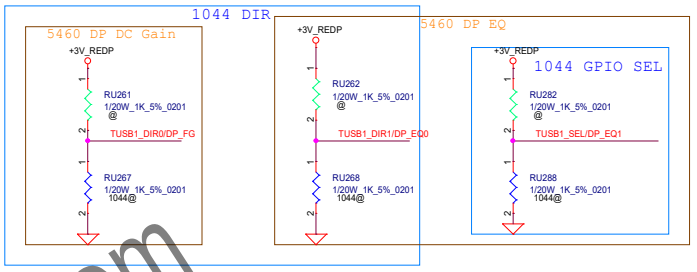
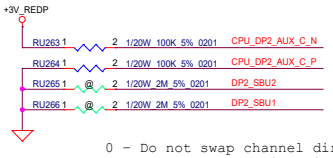


TABLE of DIR/EQ		
	1044	5460
RU282	1K	1K/200K/47K
RU288	1K	1K
RU262	@	1K/200K/47K
RU268	1k	1K
RU261	@	1K/200K/47K
RU267	1k	1K



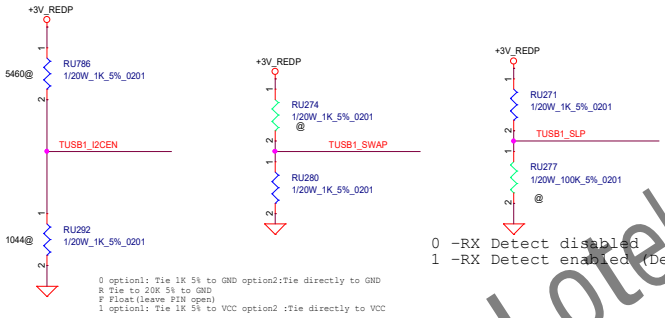
EQ setting



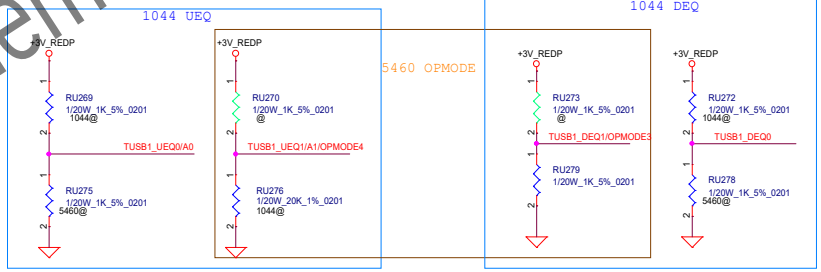
0 - Do not swap channel directions and EQ settings (Default)
1. - Swap channel directions and EQ settings

TABLE of 1044&5406		
	1044	5460
RU269	1k	1K/200K/47K
RU275	1K/20k	1K
RU270	1k	@
RU276	1K/20k	1K

TABLE of 1044&5406		
	1044	5460
RU272	1k	1K/200K/47K
RU278	1K/20k	1K
RU273	1k	@
RU279	1K/20k	1K

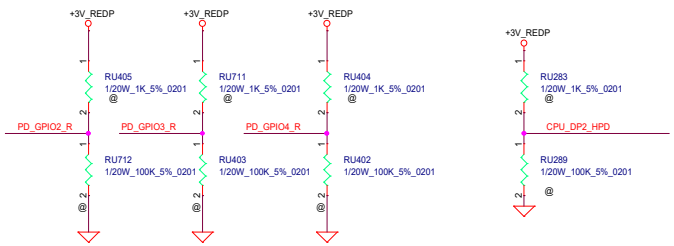


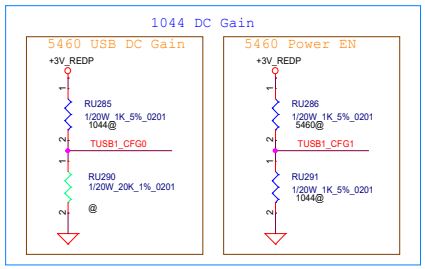
0 -RX Detect disabled
1 -RX Detect enabled (Default)

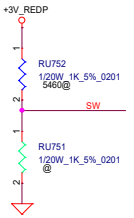


This PIN selects I/O valtage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8V configuration I/O voltage,3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface

TABLE of 1044&5406		
	1044	5460
RU285	1k	1K/200K/47K
RU290	1K/20k	1K
RU286	1k	@
RU291	1K/20k	1K

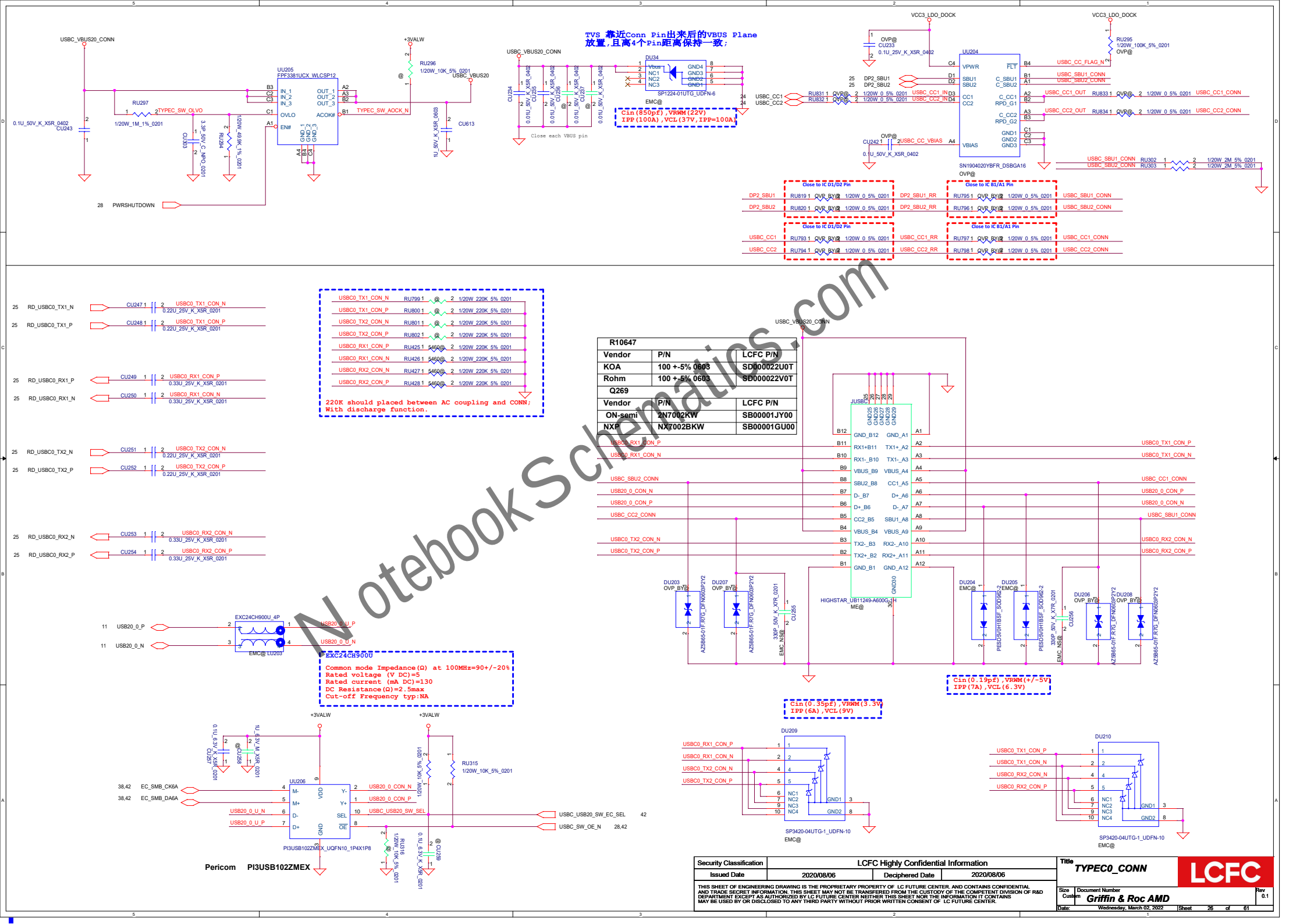






Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	TYPEC0_REDRIVER		
Size	C	Document Number	Griffin & Roc AMD
Rev	0.1		
Date:	Wednesday, March 02, 2022	Sheet	25 of 61



R10647		
Vendor	P/N	LCFC P/N
KOA	100 +-5% 0603	SD000022U0T
Rohm	100 +-5% 0603	SD000022V0T
Q269		
Vendor	P/N	LCFC P/N
ON-semi	2N7002KW	SB00001JY00
NXP	NX7002BKW	SB00001GU00

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: TYPEC0_CONN

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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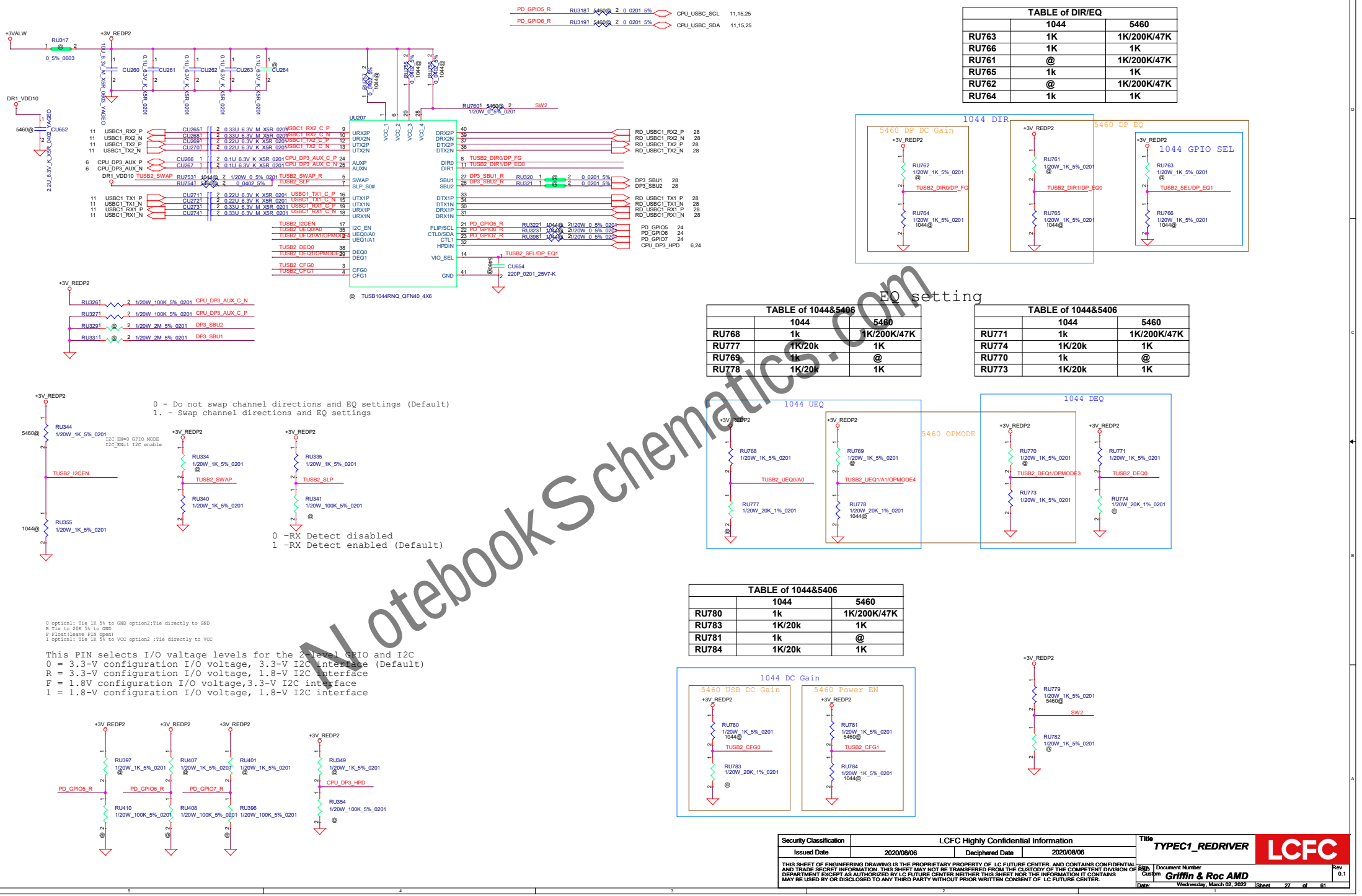

TABLE of DIR/EQ		
	1044	5460
RU763	1K	1K/200K/47K
RU766	1K	1K
RU761	@	1K/200K/47K
RU765	1k	1K
RU762	@	1K/200K/47K
RU764	1k	1K

EQ setting

TABLE of 1044&5406		
	1044	5460
RU768	1k	1K/200K/47K
RU777	1K/20k	1K
RU769	1k	@
RU778	1K/20k	1K

TABLE of 1044&5406		
	1044	5460
RU771	1k	1K/200K/47K
RU774	1K/20k	1K
RU770	1k	@
RU773	1K/20k	1K

0 - Do not swap channel directions and EQ settings (Default)
1. - Swap channel directions and EQ settings

0 -RX Detect disabled
1 -RX Detect enabled (Default)

TABLE of 1044&5406		
	1044	5460
RU780	1k	1K/200K/47K
RU783	1K/20k	1K
RU781	1k	@
RU784	1K/20k	1K

0 option1: Tie 1K 5% to GND option2:Tie directly to GND
R Tie to 20K 5% to GND
F Float(leave PIN open)
1 option1: Tie 1K 5% to VCC option2 :Tie directly to VCC

This PIN selects I/O valtage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8V configuration I/O voltage,3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: TYPEC1_REDRIVER

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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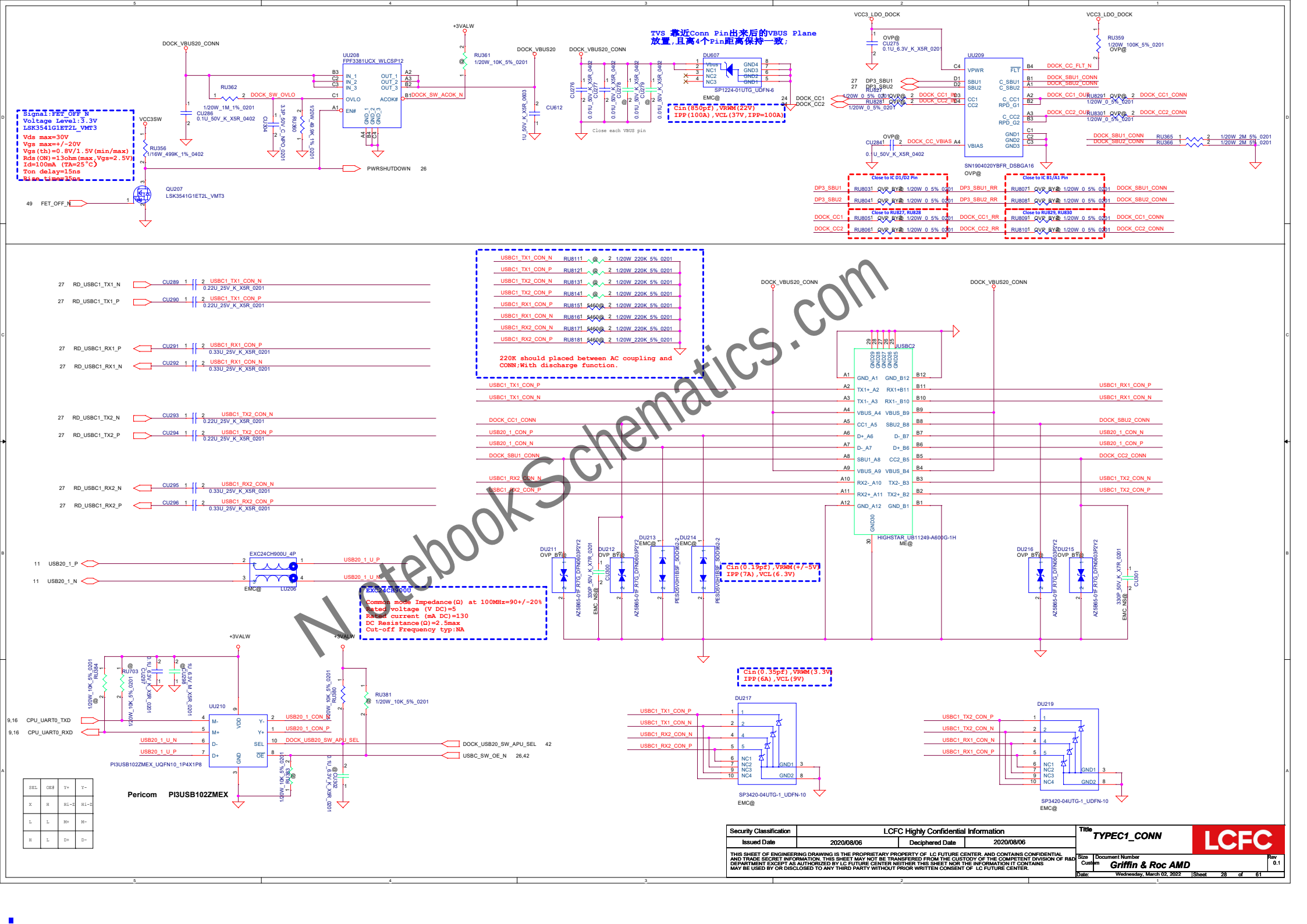
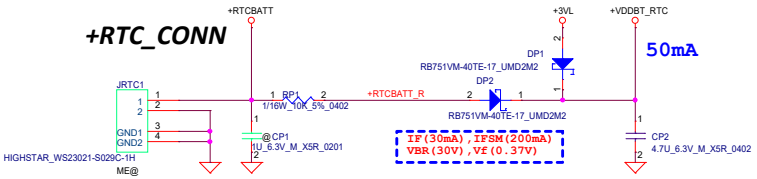
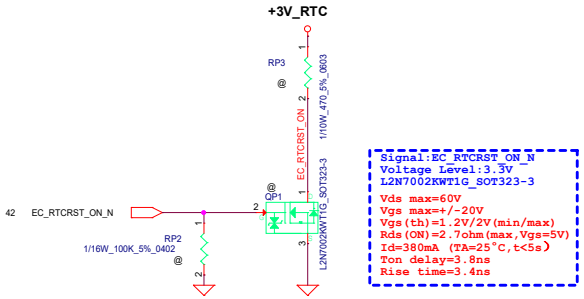
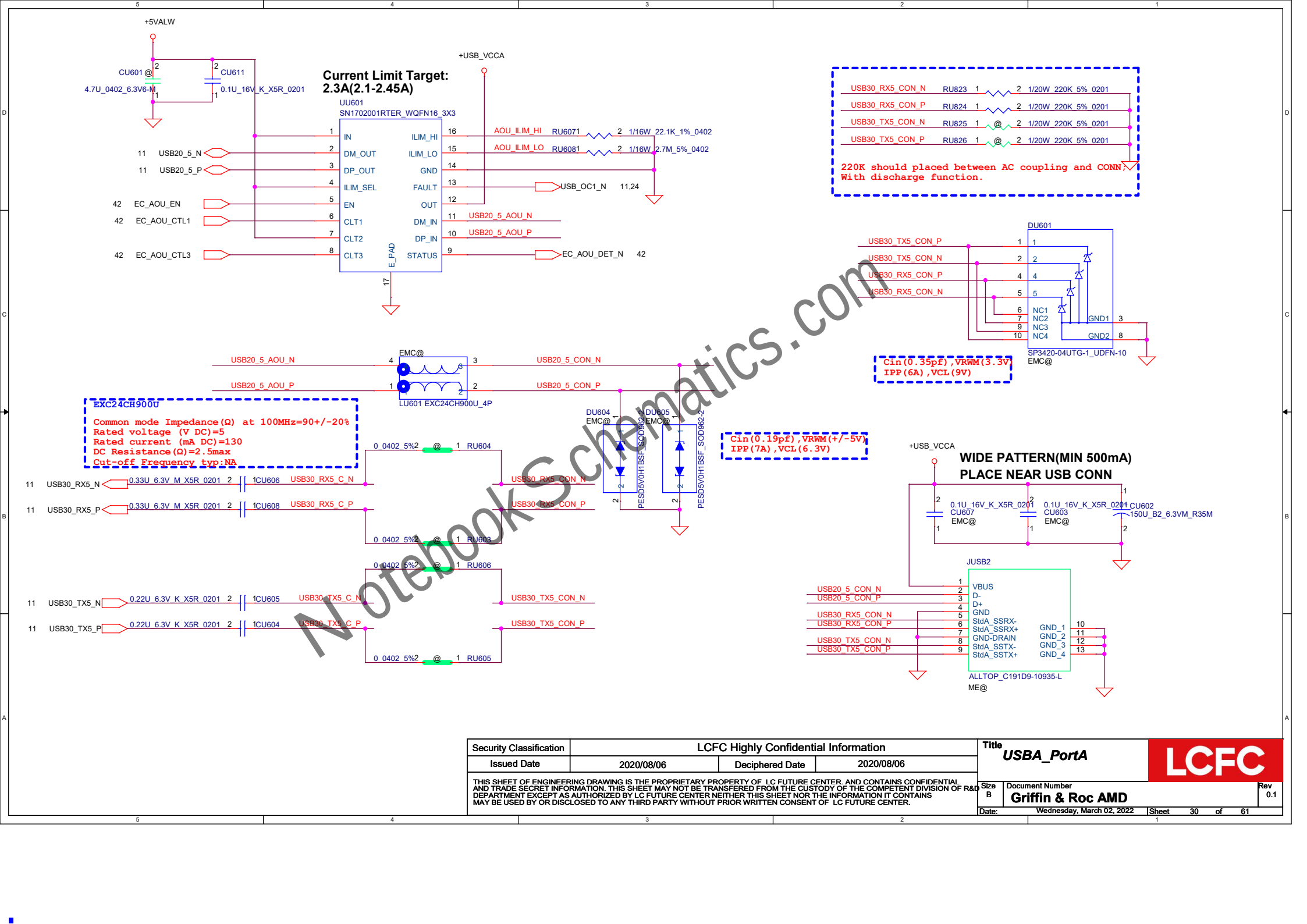






Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	RTC		
Size	Document Number		Rev
C	Griffin & Roc AMD		0.1
Date:	Wednesday, March 02, 2022	Sheet	29 of 61



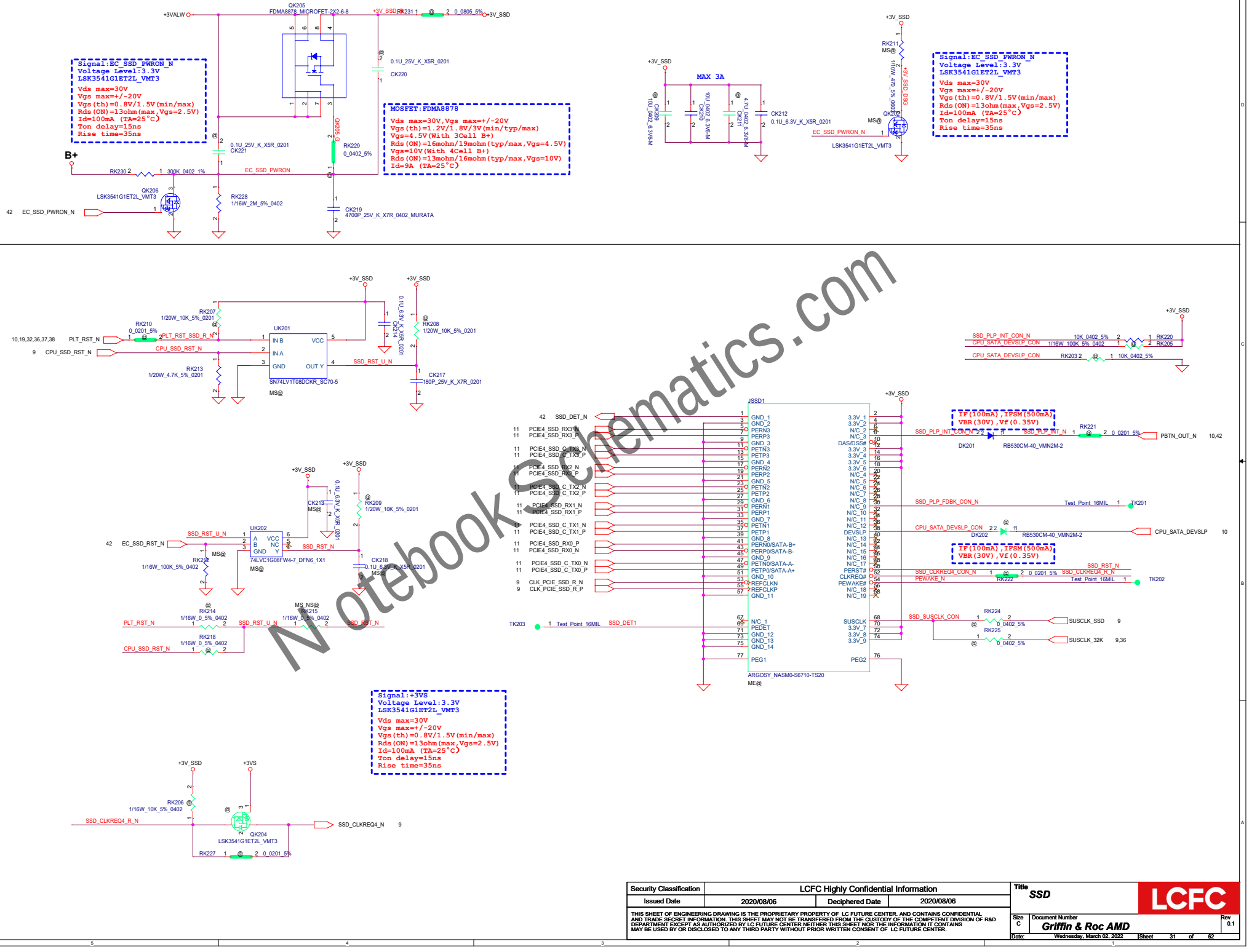
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *USBA_PortA*

LCFC

Size	Document Number	Rev
B	Griffin & Roc AMD	0.1

Date: Wednesday, March 02, 2022 Sheet 30 of 61



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	SSD	LCFC	
Size	C	Document Number	Griffin & Roc AMD
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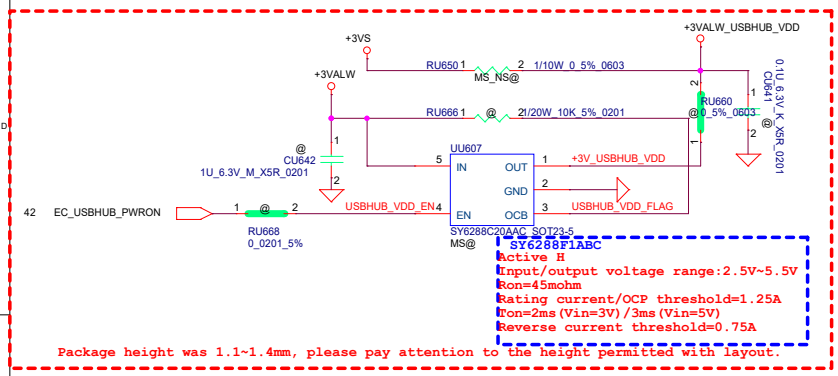
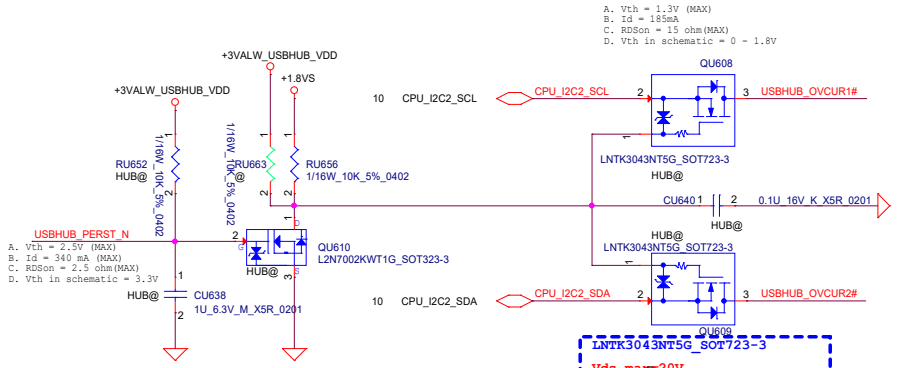
+3VALW TO +3VALW_USBHUB_VDD



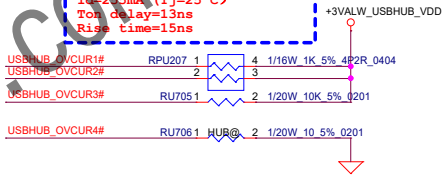


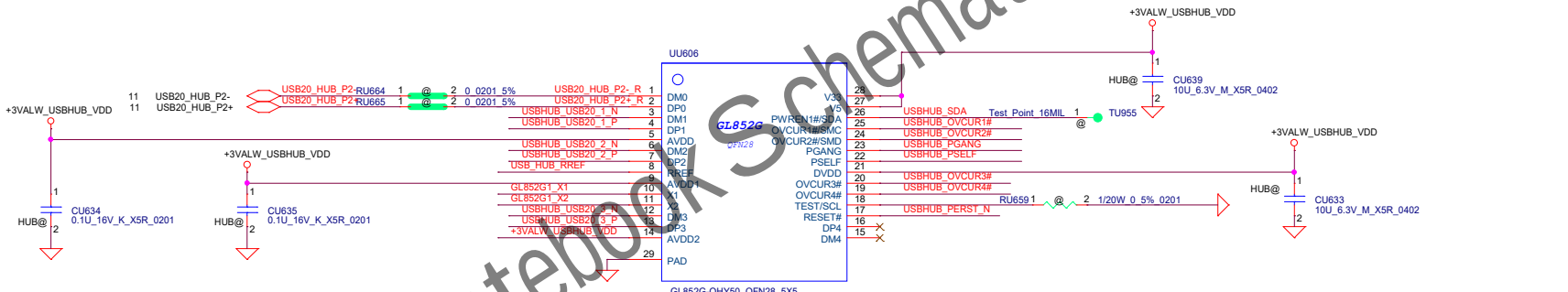
Signal:USBHUB_PERST_N
Voltage Level:3.3V
L2N7002KWT1G_SOT323-3

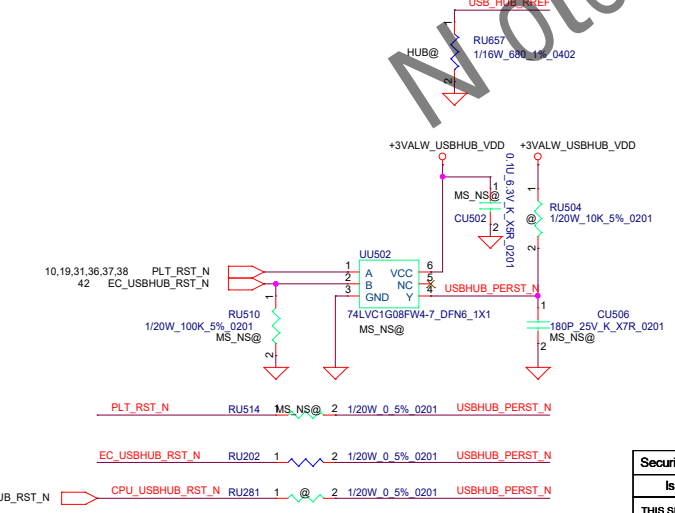
Vds max=60V
Vgs max=+/-20V
Vgs(th)=1.2V/2V(min/max)
Rds(ON)=2.7ohm(max,Vgs=5V)
Id=380mA (TA=25°C,t<5s)
Ton delay=3.8ns
Rise time=3.4ns

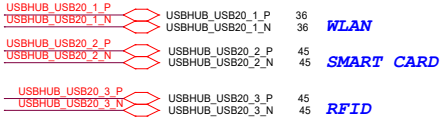
LNTK3043NT5G_SOT723-3

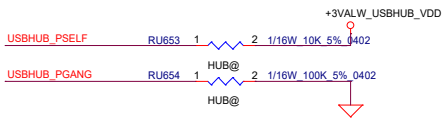
Vds max=20V
Vgs max=+/-10V
Vgs(th)=0.4V/1.3V(min/max)
Rds(ON)=150ohm(max,Vgs=1.65V)
Id=255mA (Tj=25°C)
Ton delay=13ns
Rise time=15ns





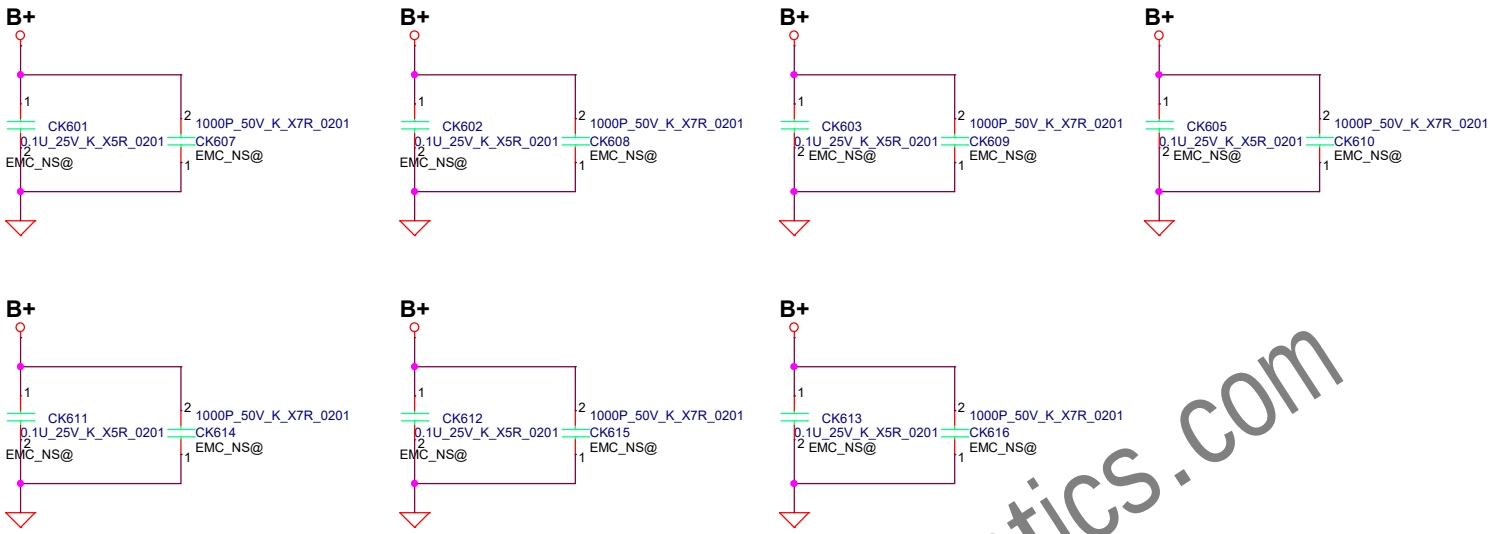






Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title	USB HUB		
Size: Custom	Document Number: Griffin & Roc AMD		Rev: 0.1
Date: Wednesday, March 02, 2022	Sheet 32 of 61		



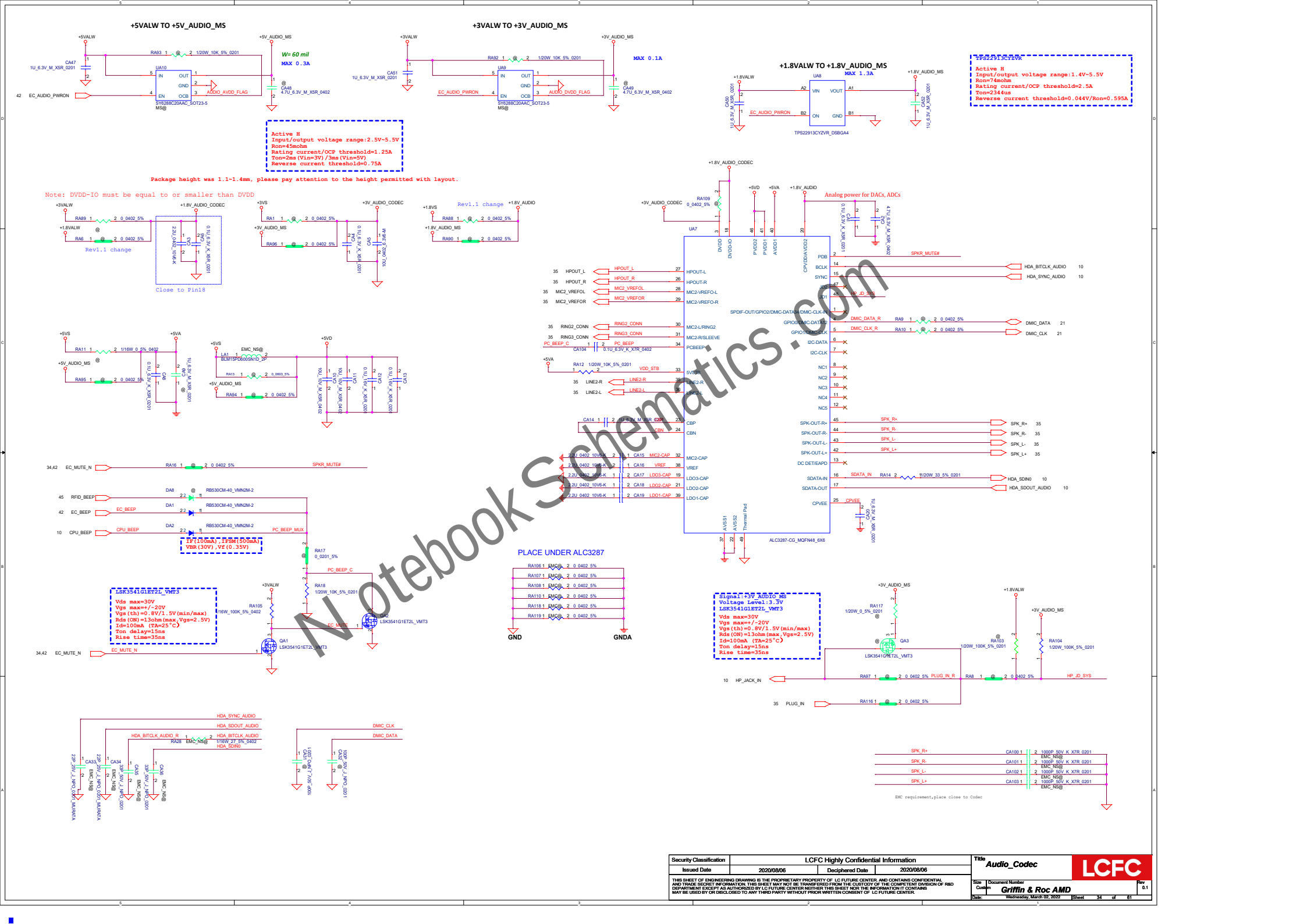
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: ***EMI CAP***

LCFC

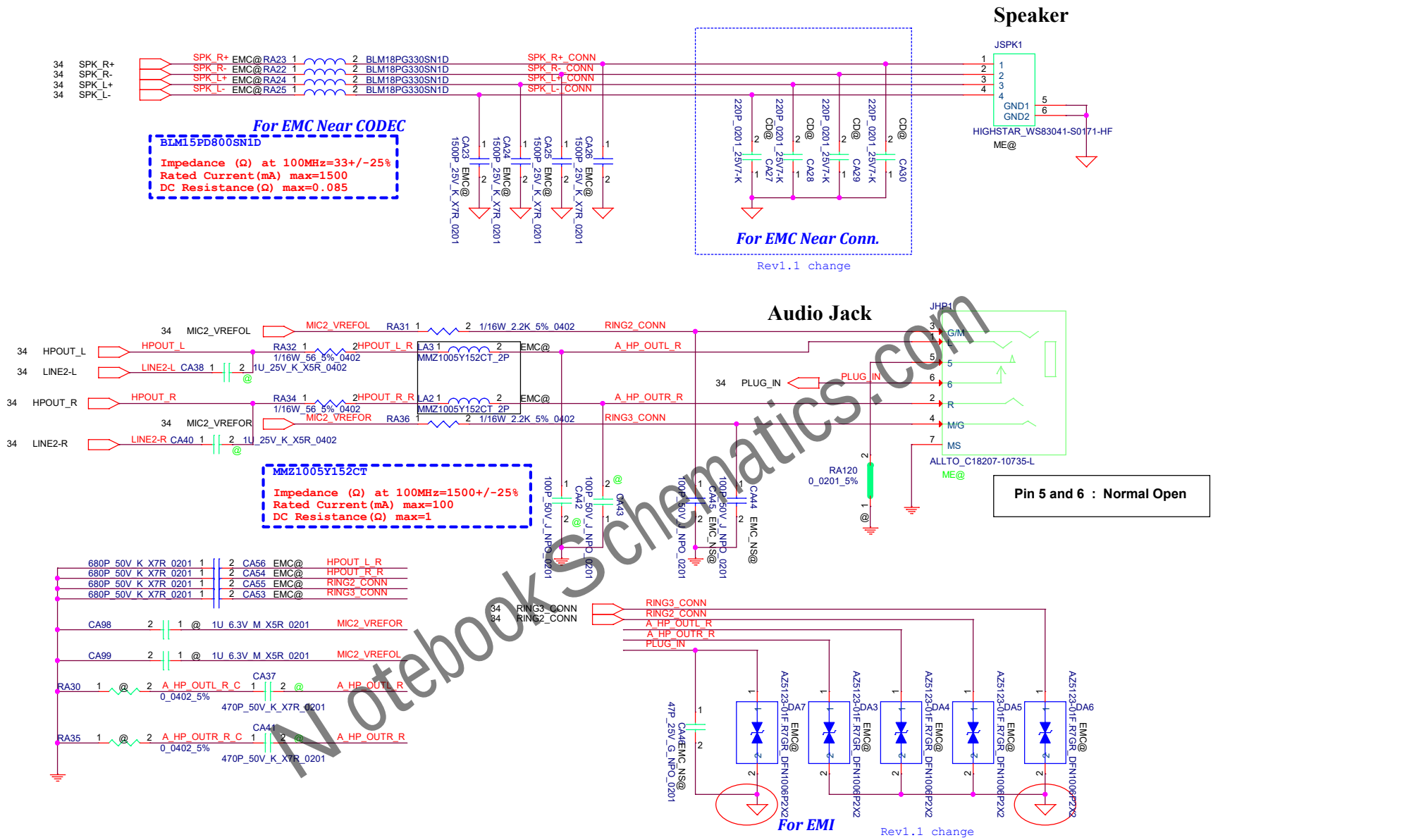
Size	Document Number	Rev
B	***Griffin & Roc AMD***	0.1

Date: Wednesday, March 02, 2022 Sheet 33 of 61



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	Audio_Codec		
Size	Document Number		Rev
Custom	Griffin & Roc AMD		0.1
Date:	Wednesday, March 02, 2022	Sheet	34 of 61



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	Audio_SPK/Jack		LCFC
Size B	Document Number Griffin & Roc AMD		Rev 0.1
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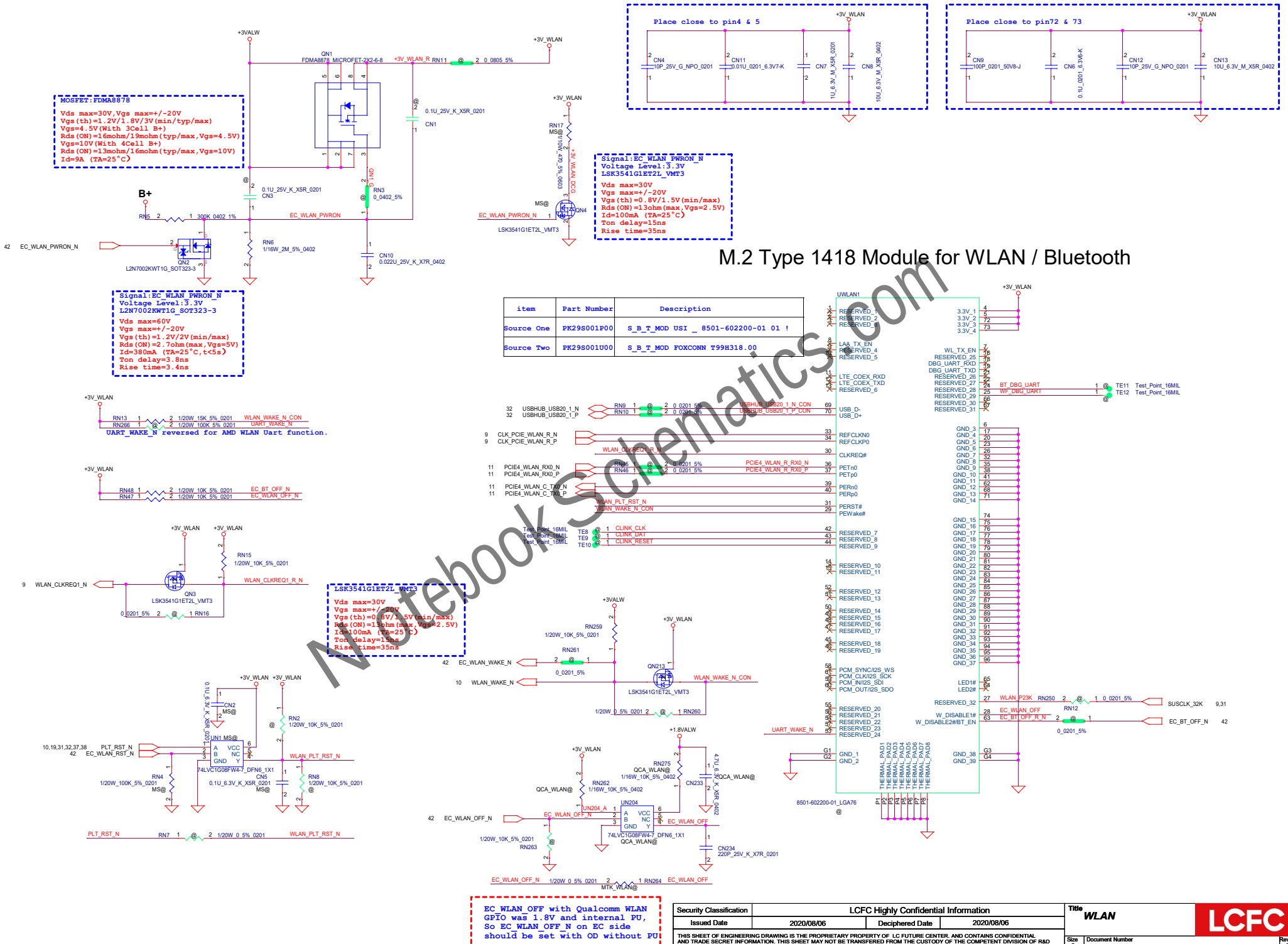
M.2 Type 1418 Module for WLAN / Bluetooth



item	Part Number	Description
Source One	PK29S001P00	S_B_T_MOD USI _ 8501-602200-01 01 !
Source Two	PK29S001U00	S_B_T_MOD FOXCONN T99H318.00

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: WLAN

LCFC

Size: C | Document Number: Griffin & Roc AMD | Rev: 0.1

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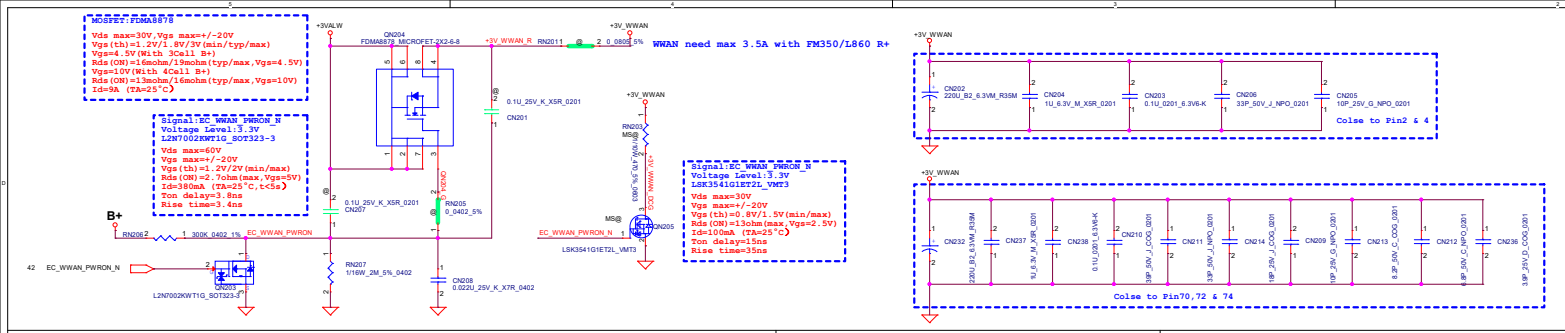
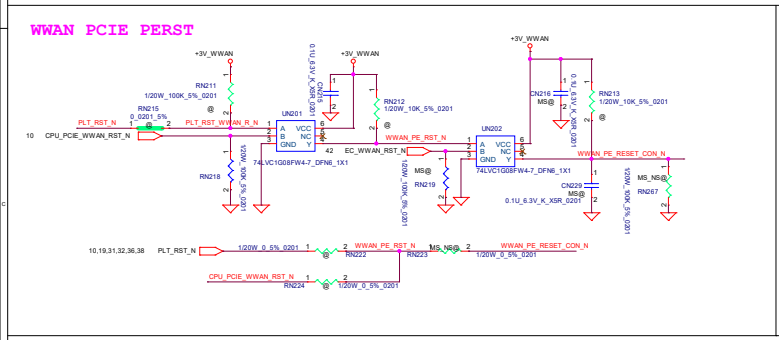
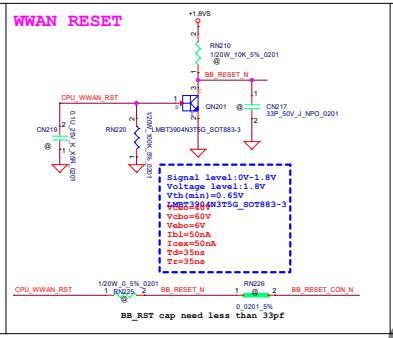
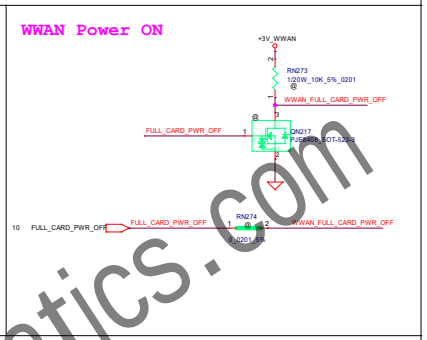
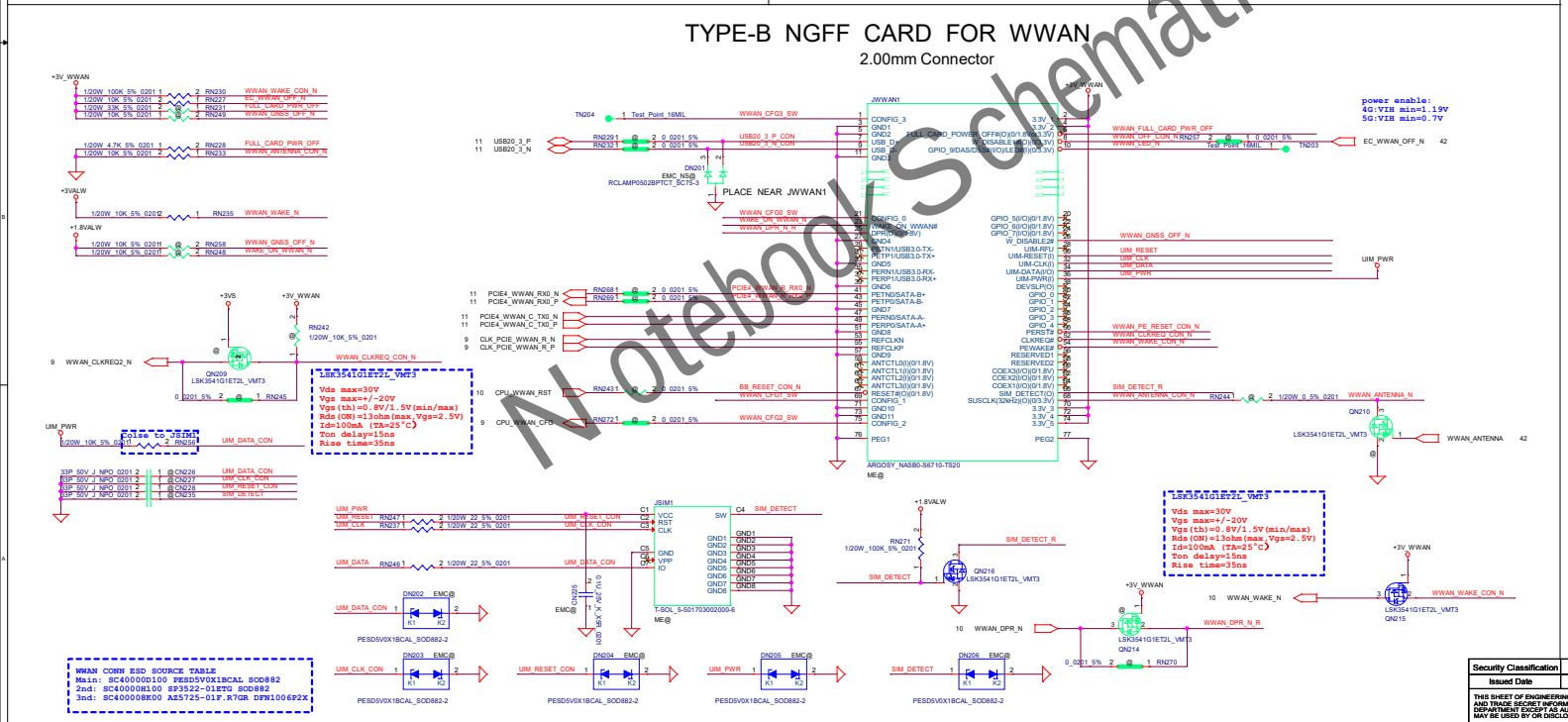










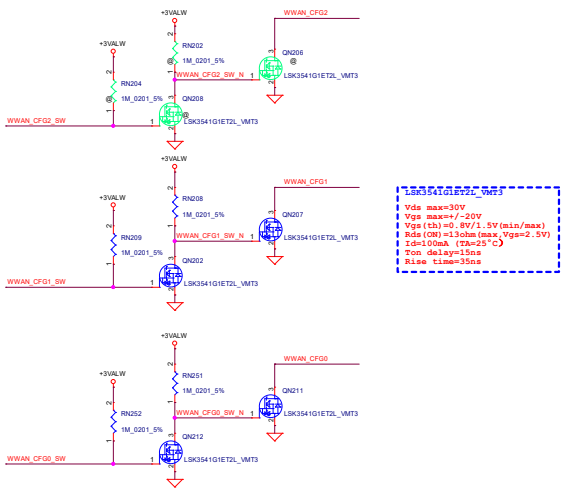
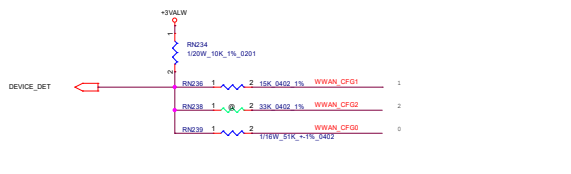


TABLE 3-15. Socket 2 Add-in Card Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	NC	GND	GND	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	NC	NC	GND	WWAN - PCIe	1
4	GND	GND	GND	NC	WWAN-PCIe, USB3.1 Gen1	0 Notes 4,5
5	GND	NC	GND	NC	WWAN-PCIe, USB3.1 Gen1	1 Notes 4,5
6	GND	GND	NC	NC	WWAN-PCIe, USB3.1 Gen1	2 Notes 4,5
7	GND	NC	NC	NC	WWAN-PCIe, USB3.1 Gen1	3 Notes 4,5
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	NC	GND	GND	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	NC	NC	GND	WWAN - SSIC	3
12	NC	GND	GND	NC	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	GND	NC	NC	WWAN-PCIe, USB3.1 Gen1	Vendor-defined Notes 3,5
15	NC	NC	NC	NC	No Add-in Card Present	N/A

TABLE:

	Module Configuration Decodes				
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	
Fibcom					
FM350-GL	GND	NC	NC	NC	
L860-GL	NC	GND	NC	NC	
Quectel					
EM05-G	NC	GND	GND	GND	
EM05-CE	NC	GND	GND	GND	



Vcc	3.32V							
R10955	10K +/- 1%							
DEVICE_DETECT1#	1.533V	1.686V	1.782V	1.992V	2.215V	2.548V	2.776V	3.32V
WWAN_CFG1	V	V	V	V	X	X	X	X
WWAN_CFG2	V	V	X	X	V	V	X	X
WWAN_CFG0	V	X	V	X	V	X	V	X
Configuration				L860 EM05			FM350	NWWAN

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: WWAN

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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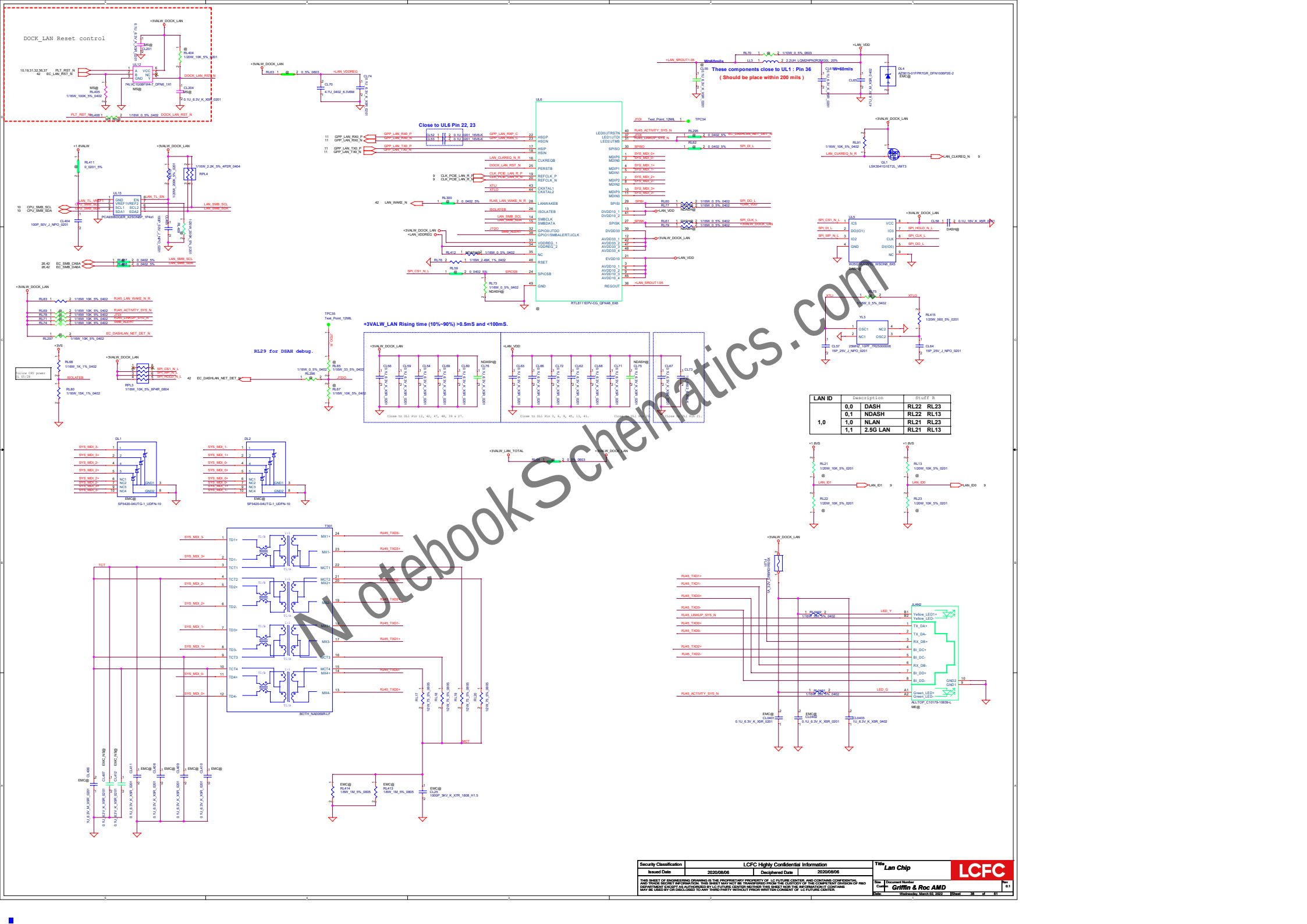
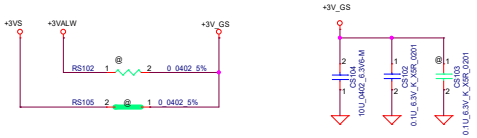
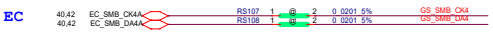
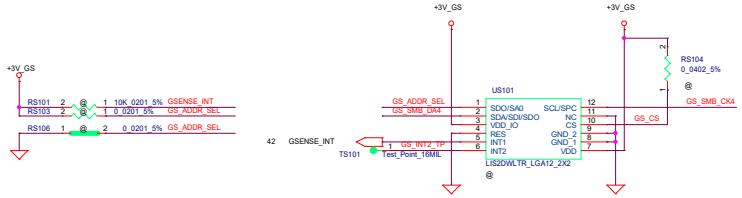


G sensor# (On Board)



EC





TABLE

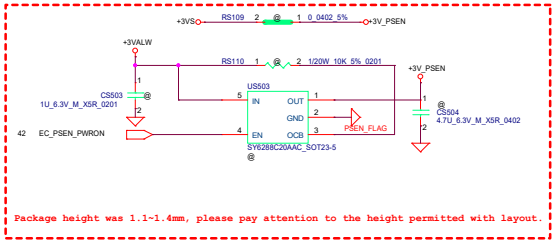
P/N	ADDR_SEL	Address
LIS2DWLTR/ BMA422	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

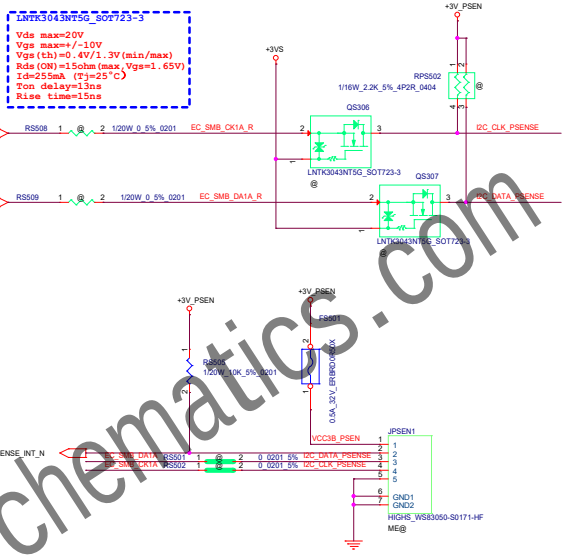
TABLE of G-Sensor (U148)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA422	SA0000C1V00
Kionix	KX022-1020	SA000081E00

Table 17. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

P sensor





Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: Sensor

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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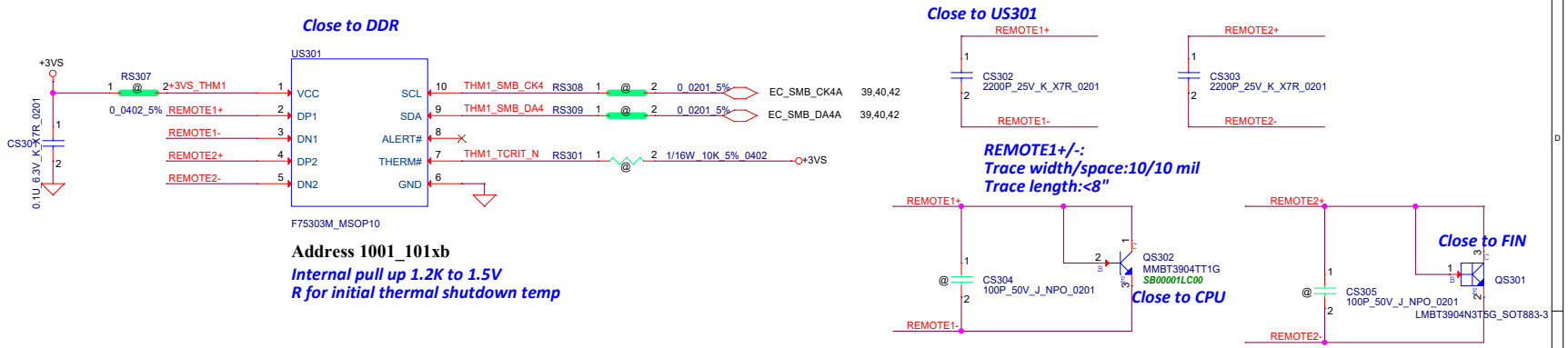
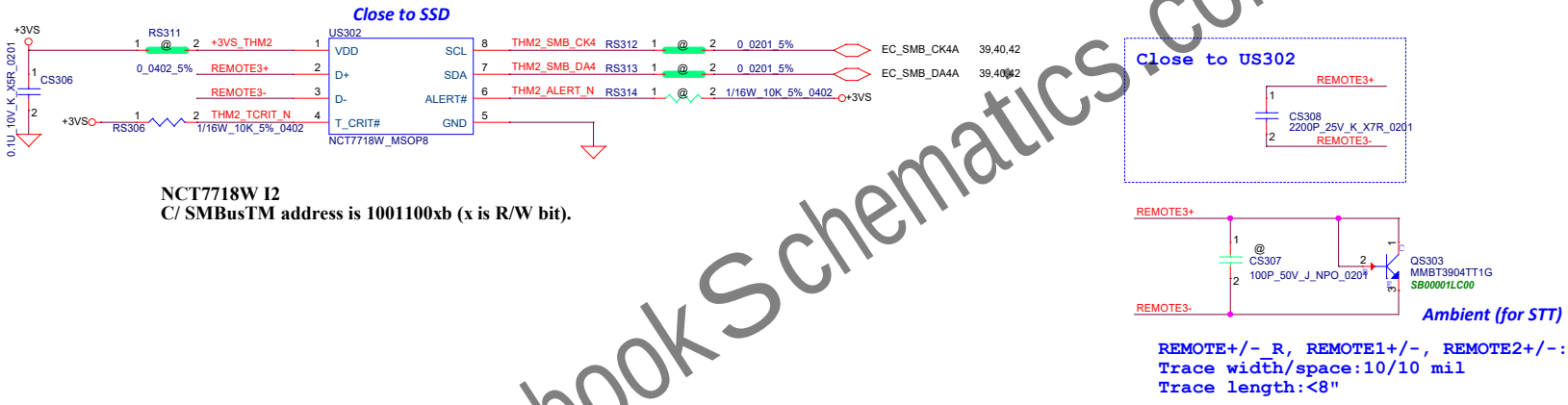
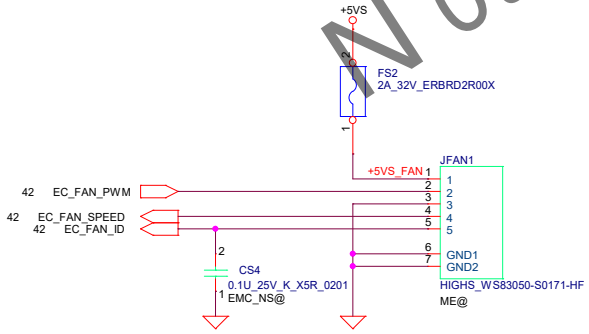




FAN CURRENT
IS 0.5A MAX

FUSE 2.0A



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: Thermal

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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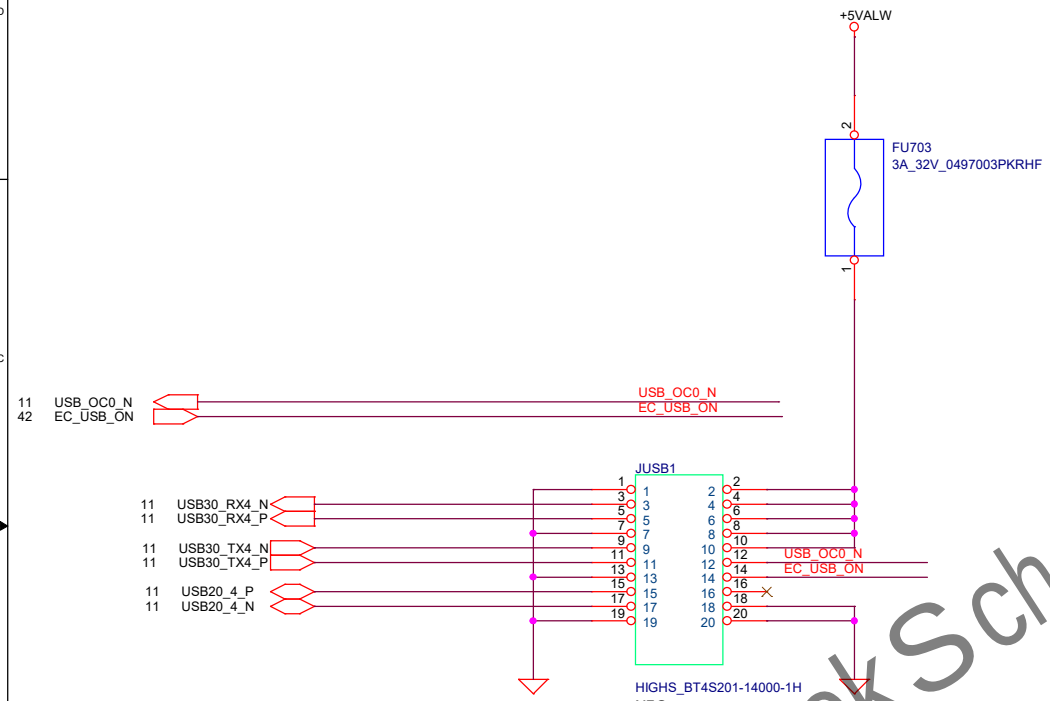
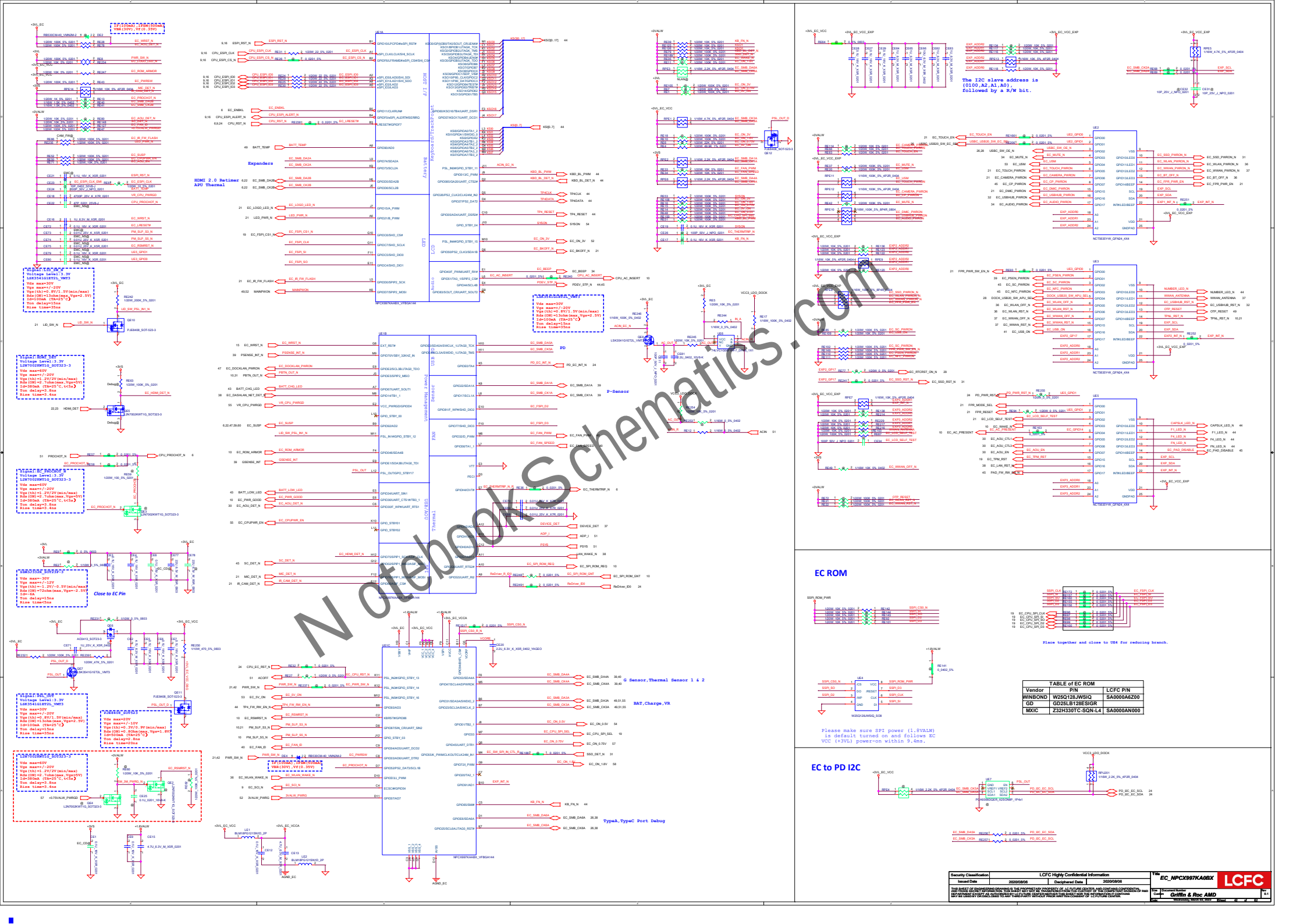


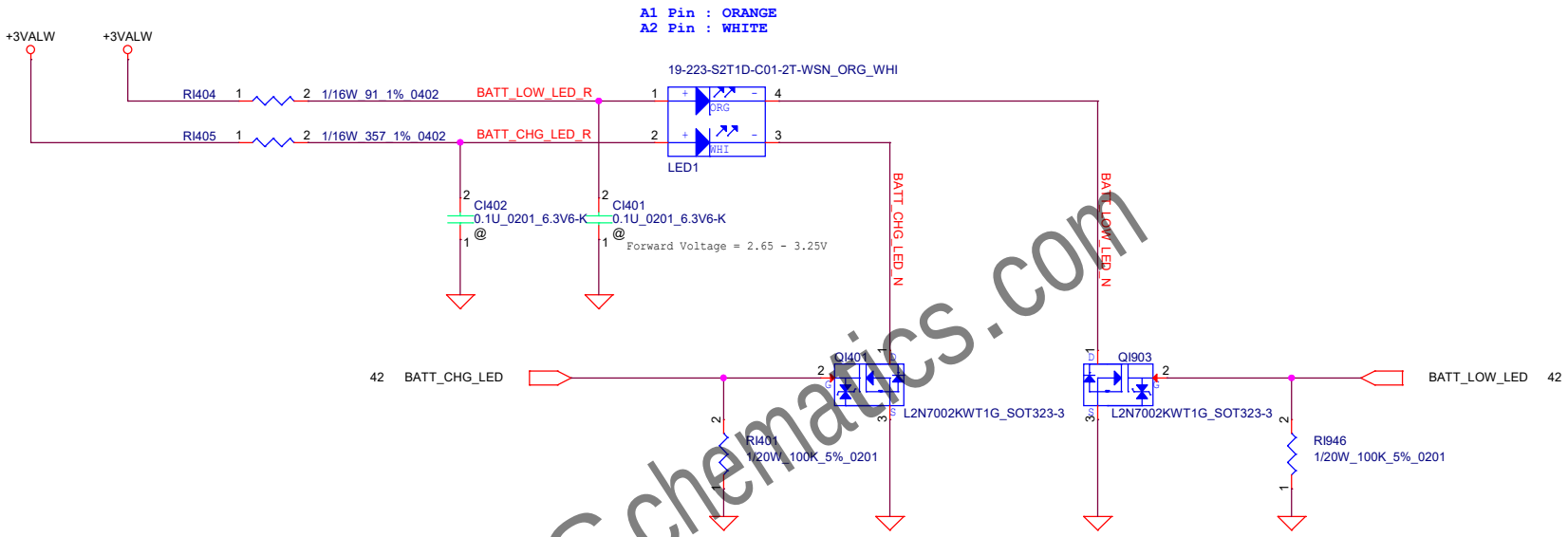
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: **Sub Board CONN**

LCFC

Size: B	Document Number: Griffin & Roc AMD	Rev: 0.1
Date: Wednesday, March 02, 2022	Sheet 41 of 61	





Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: **BATTERY LED**

LCFC

Size: B	Document Number: Griffin & Roc AMD	Rev: 0.1
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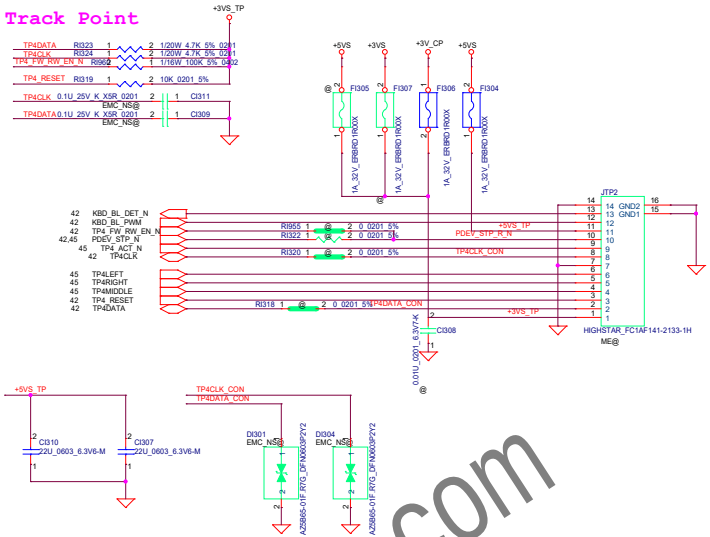
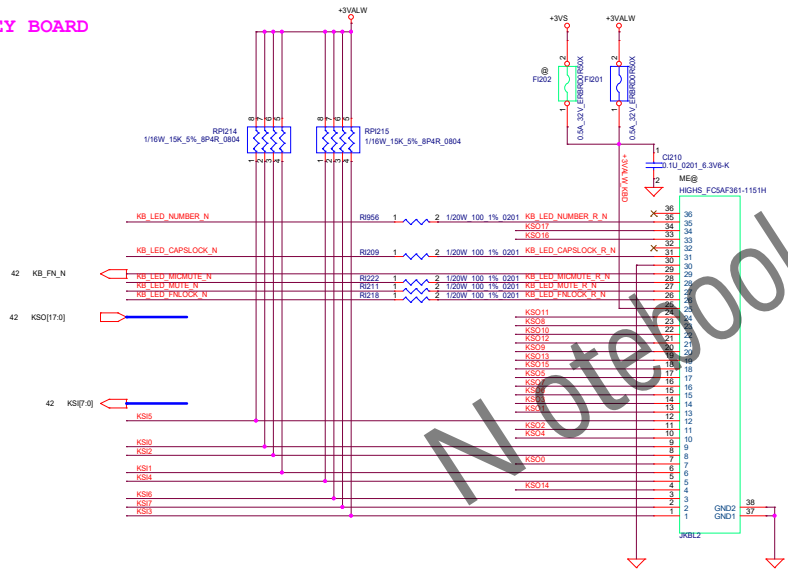
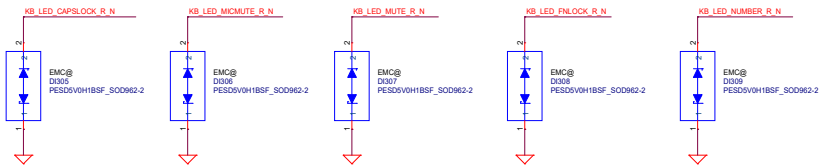
KB LED CONTROL

Track Point



KEY BOARD





TP4LEFT	EMC@	CI211	330P 50V K X7R 0201
TP4RIGHT	EMC@	CI212	330P 50V K X7R 0201
TP4MIDDLE	EMC@	CI213	330P 50V K X7R 0201
KB_FN_N	EMC@	CI214	330P 50V K X7R 0201
KSO11	EMC@	CI215	330P 50V K X7R 0201
KSO8	EMC@	CI216	330P 50V K X7R 0201
KSO10	EMC@	CI217	330P 50V K X7R 0201
KSO12	EMC@	CI218	330P 50V K X7R 0201
KSO9	EMC@	CI219	330P 50V K X7R 0201
KSO13	EMC@	CI220	330P 50V K X7R 0201
KSO15	EMC@	CI221	330P 50V K X7R 0201
KSO5	EMC@	CI222	330P 50V K X7R 0201
KSO7	EMC@	CI223	330P 50V K X7R 0201
KSO6	EMC@	CI224	330P 50V K X7R 0201
KSO3	EMC@	CI225	330P 50V K X7R 0201
KSO1	EMC@	CI226	330P 50V K X7R 0201
KSO2	EMC@	CI227	330P 50V K X7R 0201
KSO4	EMC@	CI228	330P 50V K X7R 0201
KSO0	EMC@	CI229	330P 50V K X7R 0201
KSO14	EMC@	CI230	330P 50V K X7R 0201
KSI5	EMC@	CI231	330P 50V K X7R 0201
KSI0	EMC@	CI232	330P 50V K X7R 0201
KSI2	EMC@	CI233	330P 50V K X7R 0201
KSI1	EMC@	CI234	330P 50V K X7R 0201
KSI4	EMC@	CI911	330P 50V K X7R 0201
KSI6	EMC@	CI912	330P 50V K X7R 0201
KSI7	EMC@	CI913	330P 50V K X7R 0201
KSI3	EMC@	CI914	330P 50V K X7R 0201
KBD_BL_PWM		CI313	220P 0201 25V7-K
KB_FN_N	EMC_NS@	CI204	0.01U_0201_6.3V7-K
KB_LED_FNLOCK_R_N	EMC_NS@	CI208	0.1U 25V K X5R 0201
KB_LED_MUTE_R_N	EMC_NS@	CI202	0.1U 25V K X5R 0201
KB_LED_MICMUTE_R_N	EMC_NS@	CI203	0.1U 25V K X5R 0201
KB_LED_CAPSLOCK_R_N	EMC_NS@	CI206	0.1U 25V K X5R 0201
KBD_BL_DET_N	EMC_NS@	CI312	0.1U 25V K X5R 0201
KB_LED_NUMBER_R_N	EMC_NS@	CI921	0.1U 25V K X5R 0201

CLOSE TO CONN

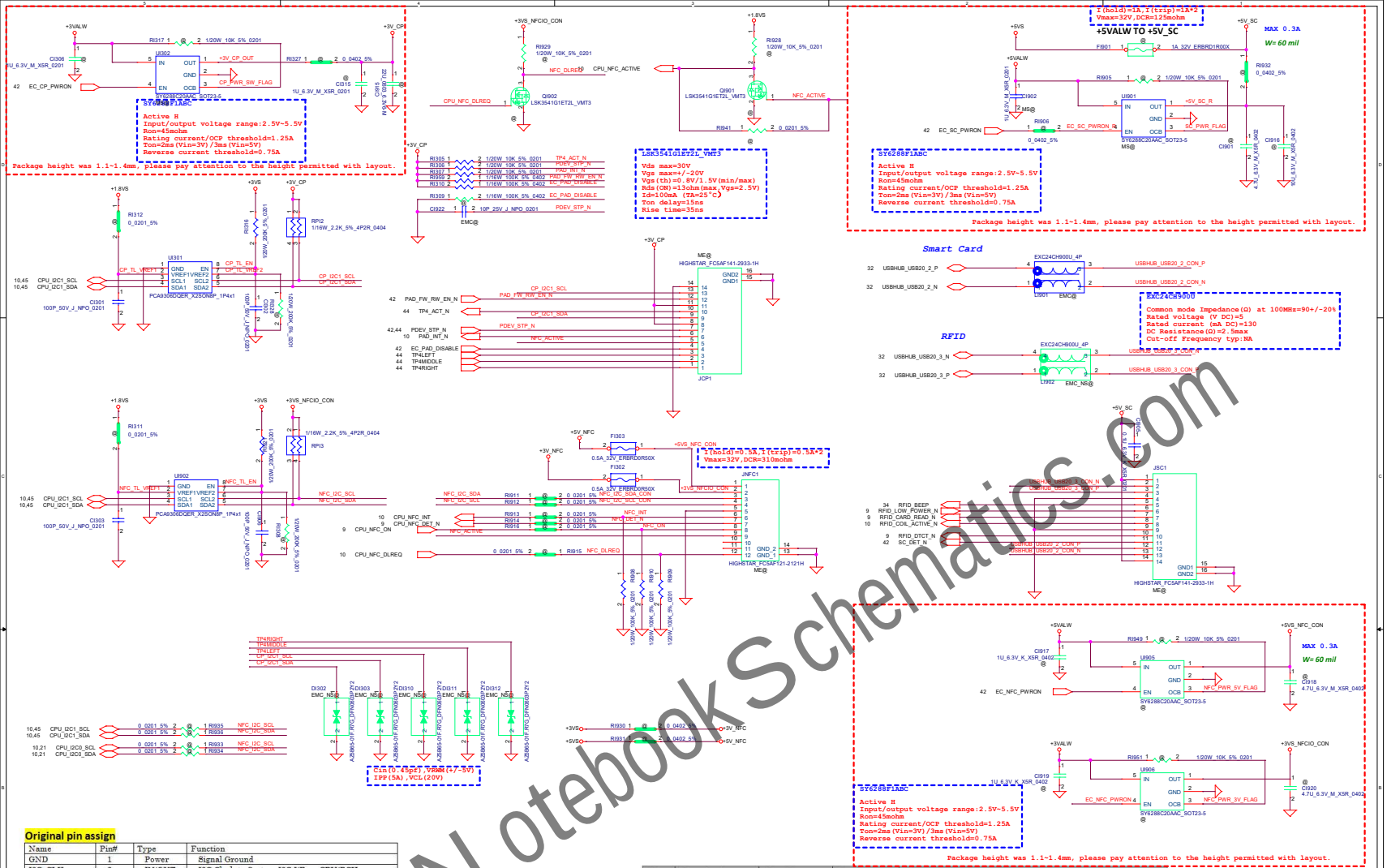
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: KB/KBBL CONN

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

Date: Wednesday, March 02, 2022 | Sheet 44 of 61



Original pin assign

Name	Pin#	Type	Function
GND	1	Power	Signal Ground
I2C_CLK	2	IN/OUT	I2C Clock to System I2C I/F on CPU/PCH
IPD_GND	3	IN	TrackPoint ground
NC	4		
TP4_ACT	5	IN	TrackPoint Activity status. Please refer to "4.2.8"
I2C_DAT	6	IN/OUT	I2C Data to System I2C I/F on CPU/PCH
VDD	7	Power	Supply power from system. Power is not supplied when system is in S3, S4, S5 and G5 state. (Refer to electrical requirement)
PDEV_STP	8	IN	This signal is used to disable to report button status and finger status to system when system LCD lid is closed or is in Tent /Stand /Tablet modes (Yoga case). Please refer to "4.2.5 PDEV_STP"
I2C_INT	9	OUT	Interrupt for I2C communication
NFC_Active	10	IN	This signal should use if NFC Antenna is implemented under touch pad PCBA. This signal should be NC or not be used in touch pad PCBA if NFC antenna is not implemented under touch pad PCBA. Please refer to "4.2.6 NFC_Active"
PAD_DISABLE	11	IN	This signal is used to disable touch pad. Please refer to "4.2.4 PAD_DISABLE".
TP4LEFT	12	IN	TrackPoint button signal
TP4MIDDLE	13	IN	TrackPoint button signal
TP4RIGHT	14	IN	TrackPoint button signal

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: TouchPad CONN

LCFC

Size: Custom | Document Number: Griffin & Roc AMD | Rev: 0.1

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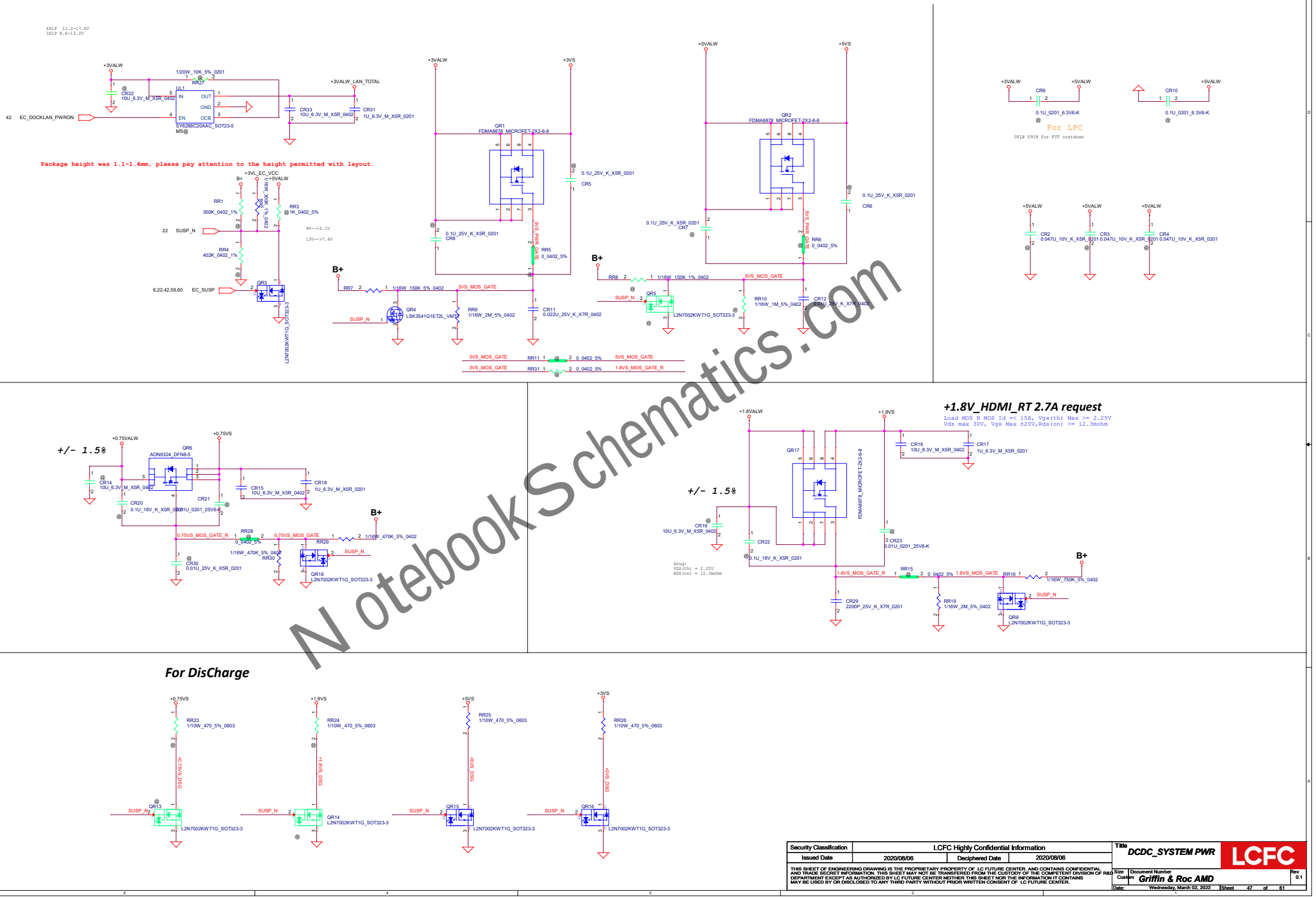
Security Classification	LC Future Center Secret Data		
Issued Date	2020/9/15	Deciphered Date	2020/7/6

Title: ***MEDIA CARD CONTROLLER***

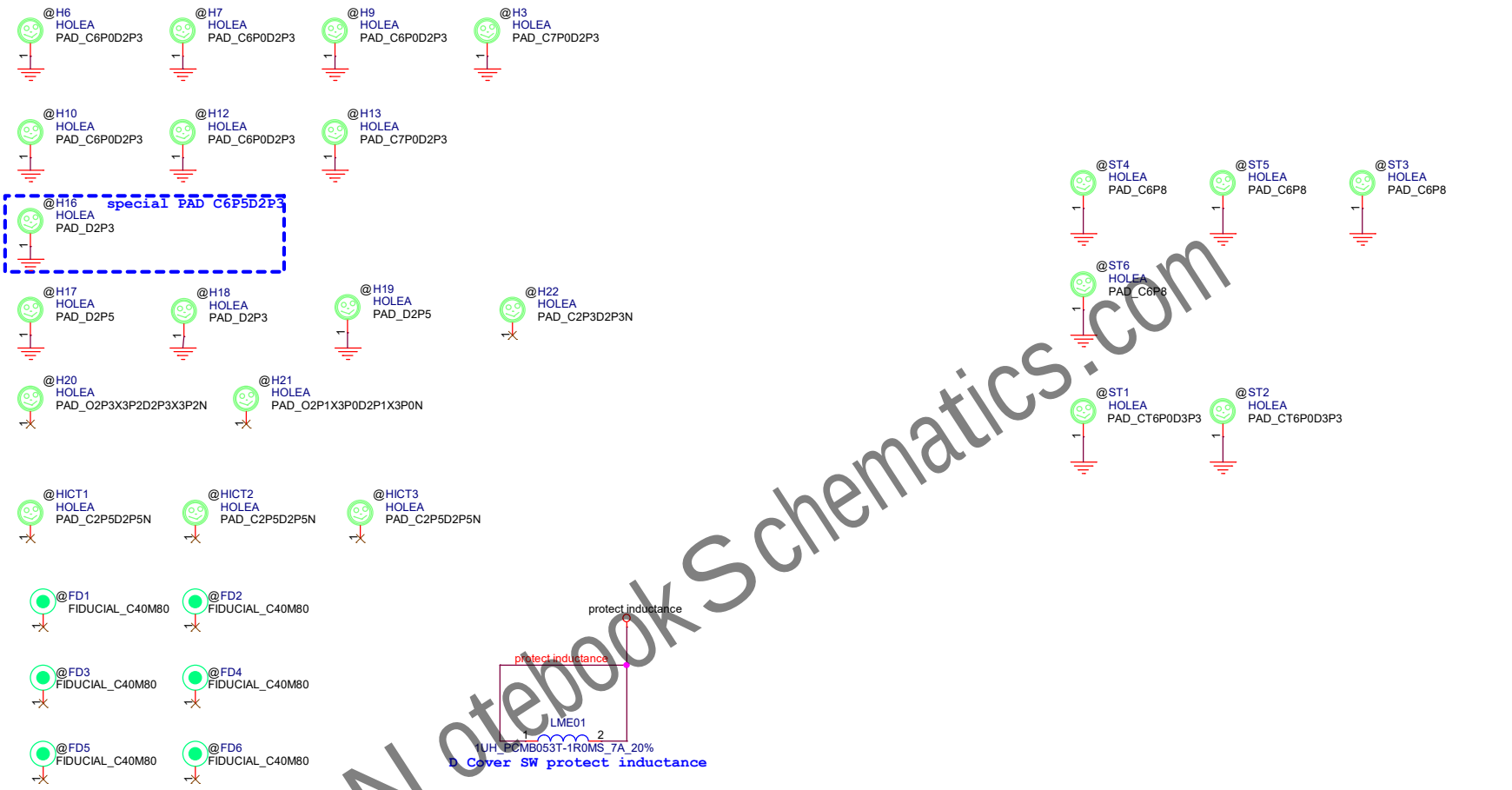
Size	Document Number	Rev
Custom	Griffin & Roc AMD	0.2

Date: Wednesday, March 02, 2022 Sheet 46 of 68



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	DCDC_SYSTEM PWR	LCFC	
Size	Custom	Document Number	Griffin & Roc AMD
Rev	0.1		
Date:	Wednesday, March 02, 2022	Sheet	47 of 61



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: ***Hole/Shielding***

LCFC

Size	Document Number	Rev
B	***Griffin & Roc AMD***	0.1

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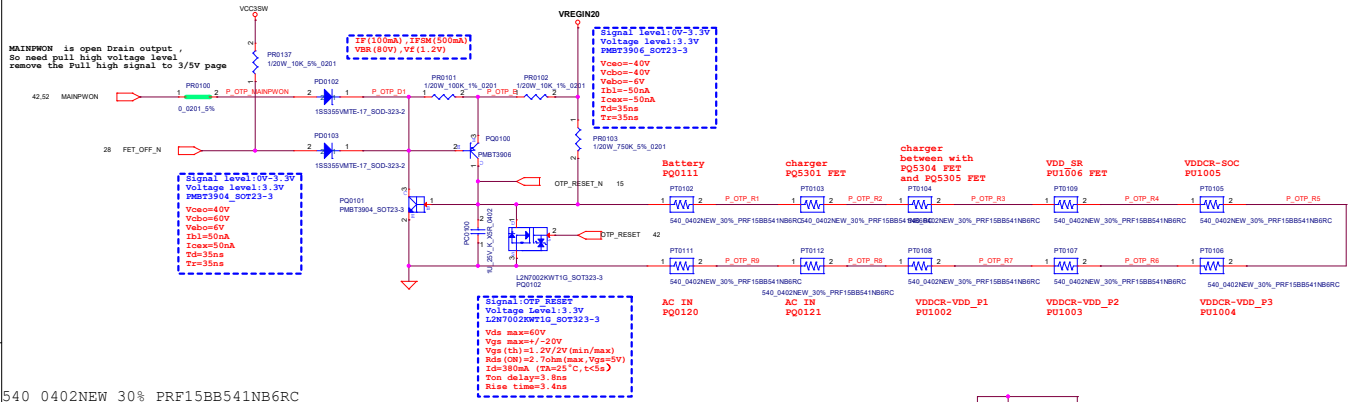
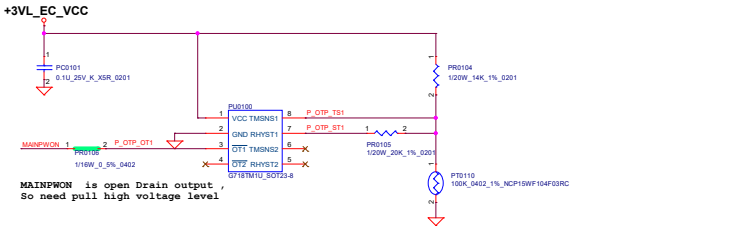
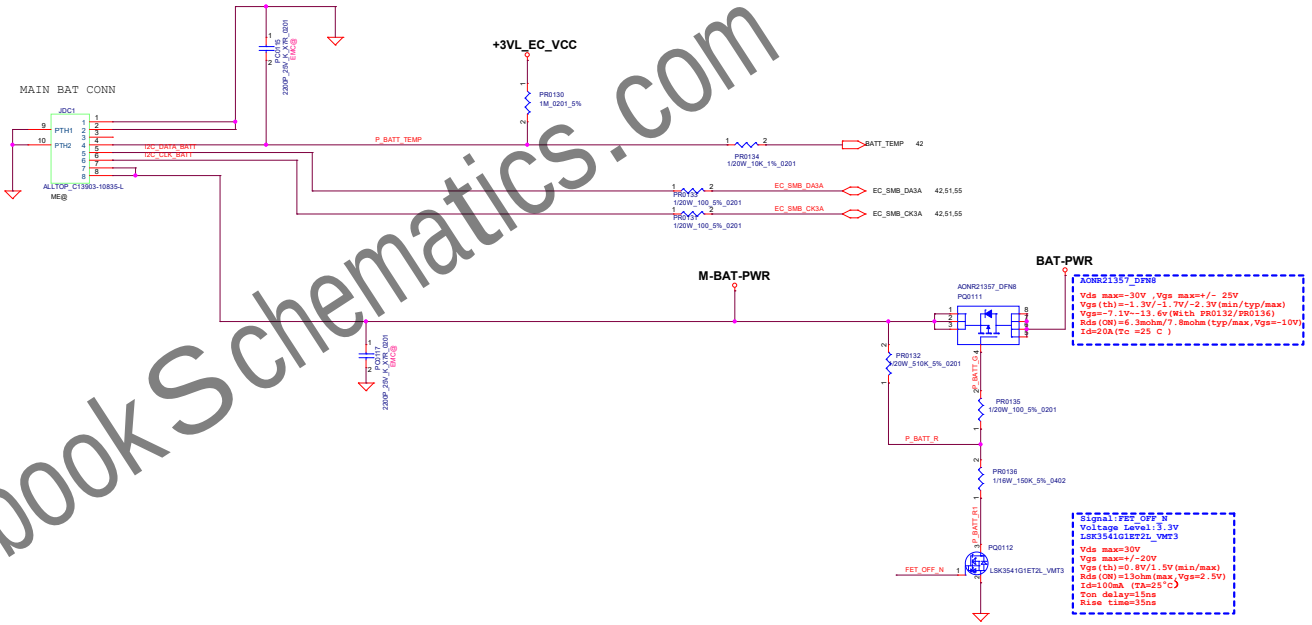


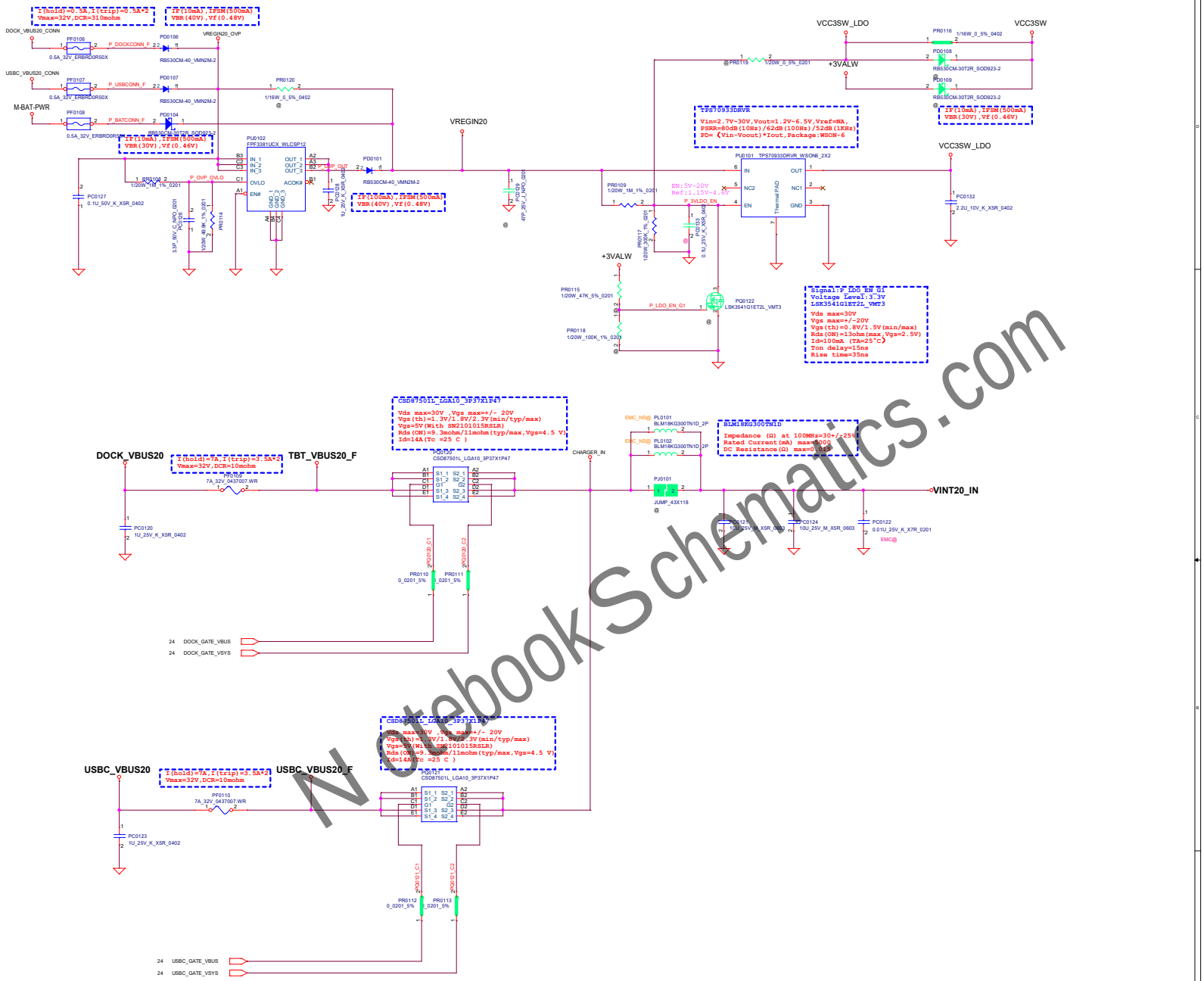


540_0402NEW_30%_PRF15BB541NB6RC
25~100Degree
0.54@25 Degree
1.2*0.54*k@85Degree
2*0.54 k@100 Degree
20*0.54 k@120Degree
100*0.54 k@130Degree
350*0.54 k@140Degree
Vbattrey min =9V,Vbattery max =12.6V
Vthreshold min=0.65V,Vthreshold min=0.85V,
TotalR (PTC)*(VBatt-1.25)/(TotalR (PTC)+750)=0.65V
TotalR (PTC)max=59.8K~==110 times 0.54 k
TotalR (PTC)min=43.72K~==80times 0.54 k
Normal run 3Dmark
the max T maybe 85 Degree
the total R PTC= 1.2*0.54*10=12*0.54 k
if only one PTC over 130 degree,
the total PTC is 100*0.54K+11*0.54k,>80*0.54K
and over the min Vthreshold,and active the OTP
if only one PTC over 140 degree,
the total PTC is 350*0.54K>>80*0.54K
,can over the min Vthreshold
and active the OTP
so,the OTP function is ok



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PWR_DCIN/RTC	LCFC	
Size: Custom	Document Number: Serval 2/Phoenix AMD	Rev: 0.1	
Date: Wednesday, March 02, 2022	Sheet 49 of 62		



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

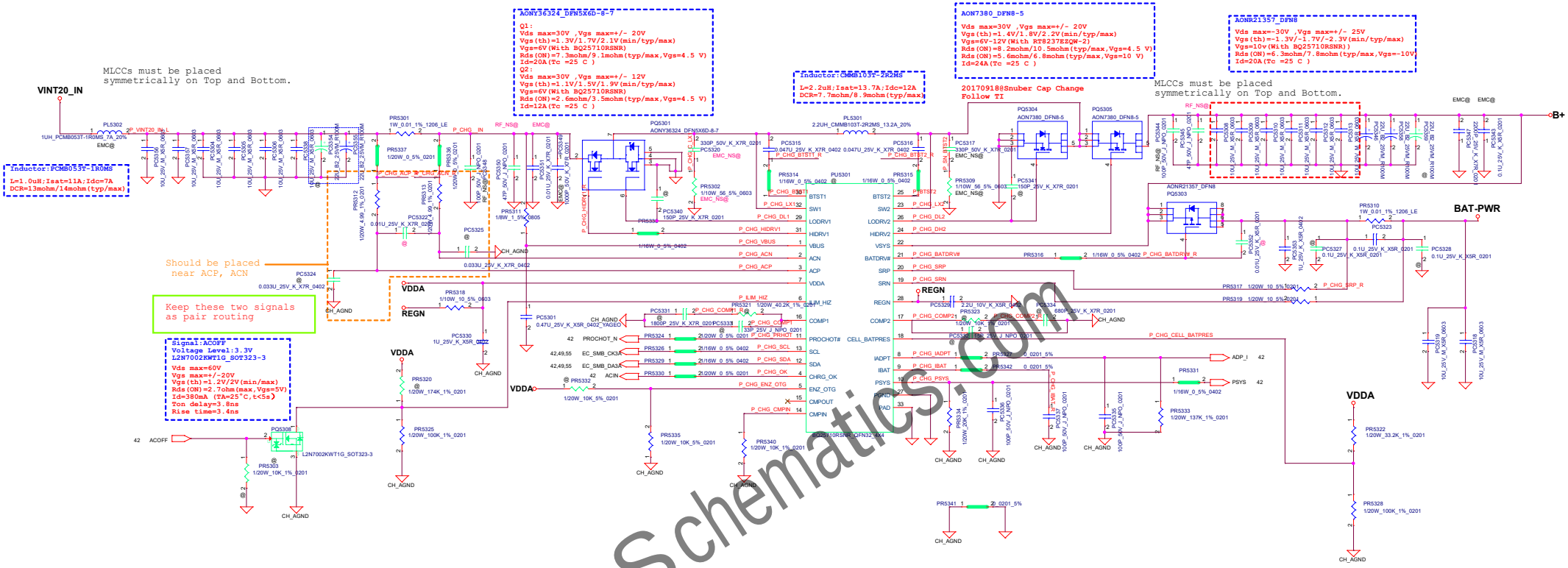
Title: PWR_ACIN

LCFC

Size: Custom | Document Number: Serval 2/Phoenix AMD | Rev: 0.1

Date: Wednesday, March 02, 2022 | Sheet 50 of 62

Part Reference:
PX5301~PX53**



CHGTI@: Install for BQ25710RSNR
CHGSOUTHA: Install for SC8885LQDER

IDPM	V(ILIM)	PR5320
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

LOGIC

TABLE of Main/2nd

IC	PU5301	TI BQ25710RSNR (1st)	Southchip SC8885LQDER (2nd)
ACP	PC5324	0.033U_25V_K_X7R_0402	NO_ASM
ACN	PC5325	0.033U_25V_K_X7R_0402	NO_ASM
COMP1	PR5321	40.2K_1%_0201	100K +-1% 0201
COMP1	PC5331	1800P_25V_K_X7R_0201	1000P 25V K X7R 0201
COMP1	PC5333	33P_25V_J_NPO_0201	10P 25V J NPO 0201
COMP2	PR5323	10K_1%_0201	330K +-1% 0201
COMP2	PC5332	15P_25V_J_NPO_0201	220P 25V K X7R 0201
COMP2	PC5334	680P_25V_K_X7R_0201	1000P 25V K X7R 0201
LIM_HZ	PR5320	174K_1%_0201	137K +-1% 0201

TABLE of PU5301

	Vendor	P/N	LCFC P/N
1st	TI	BQ25710RSNR	SA00009K300
2nd	Southchip	SC8885LQDER	SA0000CTY00

# of CELL	VCELL_PRES	PR5322
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

LOGIC

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PWR_CHARGER

LCFC

Size: Custom | Document Number: Commercial AMD Griffin and Roc | Rev: 0.1

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Part Reference:
PX6001~PX60**

TABLE of PU6001			
	Vendor	P/N	LCFC P/N
1st	TI	TPS51393RJER	SA0000APB00
2nd	SILERGY	SYV768BRAC	SA0000CHC00

TABLE of Main/2nd			
IC	PU6001	TI TPS51393RJER (1st)	Silergy SYV768BRAC (2nd)
VCC	PC6004	1U_25V_K_X5R_0402	4.7U_6.3V_M_X5R_0402
VCC	PR6009	NO_ASM	0_5%_0603
LDO	PR6010	0_5%_0603	NO_ASM
LDO	PC6005	4.7U_6.3V_M_X5R_0402	NO_ASM
BST	PC6001	0.22U_25V_K_X5R_0402	0.1U 25V K X7R 0402
FB	PR6011	240K_1%_0201	1K +-1% 0201
FB	PC6003	470P_50V_K_X7R_0201	1000P 50V K X7R 0201

3VTI@: Install for TPS51393
3VSILERGY@: Install for SYV768B

+3VALW
TDC = 7.5A

B+ 3A PJ6003 JUMP_43X79 @

EMC@ PC6017 0.1U_25V_K_X5R_0201
EMC@ PC6018 2200P_25V_K_X7R_0201
PC6019 10U_25V_M_X5R_0603
PC6020 10U_25V_M_X5R_0603
PC6024 10U_25V_M_X5R_0603
PC6025 10U_25V_M_X5R_0603
PC6021 22U_B2_25VM_R100M
RF_NS@ PC6022 47P_25V_J_NPO_0201
RF_NS@ PC6023 100P_50V_J_NPO_0201

+3VL
PR6009 1/10W_0_5%_0603 @
P_3VALW_VCC

+3VALW
PR6002 1/20W_100K_1%_0201
PR6014 0_0201_5%
3VALW_PWRG 42

PC6004 @ 1U_25V_K_X5R_0402
@ PU6001
TPS51393RJER_VQFN20_3X3
VCC PGOOD P_3VALW_PG
P_3VALW_VCC
P_3VALW_VIN VIN1 VIN2 VIN3 VIN4
SW1 SW2 SW3 P_3VALW_SW
BST P_3VALW_BST
P_3VALW_BST_R PC6001 0.22U_25V_K_X5R_0402 @
PR6008 1/16W_0_5%_0402
EN P_3VALW_EN
VOUT
ENLDO P_3VALW_ENLDO
FB P_3VALW_FB
PR6011 1/20W_240K_1%_0201 @
PC6003 470P_50V_K_X7R_0201 @
LDO
NC1 NC2
PGND1 PGND2 PGND3 THERMAL PAD

Inductor:CMLE053T-1R5MS
L=1.5uH;Isat=8.0A;Idc=7.2A
DCR=14.7mohm/17mohm(typ/max)
PL6001 1.5UH_CMLE053T-1R5MS_8.2A_20%

PR6006 1/20W_10K_1%_0201
42 EC_ON_3V
@PR6007 1/20W_0_5%_0201

+3VL_EC_VCC
PC6002 0.1U_25V_K_X5R_0201 @
PR6012 1/20W_100K_1%_0201
PR6013 1/20W_100K_1%_0201
PQ6001A NTJD5121NT1G_SC88-6
PQ6001B NTJD5121NT1G_SC88-6
42,49 MAINPWON
@PR6003 1/20W_47K_5%_0201
6V_EN2_GATE 53

NTJD5121NT1G_SC88-6
Vds max=60V
Vgs max=+/-20V
Vgs(th)=1V/2.5V(min/max)
Rds(ON)=2.5ohm(max,Vgs=4.5V)
Id=295mA (TA=25°C)
Ton delay=22ns

B+
PR6001 1/20W_1M_5%_0201
Ven 2.1V ~4.1V
PR6005 1/20W_300K_1%_0201

+3VL
PR6010 1/10W_0_5%_0603 @
P_3VALW_LDO
PC6005 4.7U_6.3V_M_X5R_0402 @

P_3VALW_SW
EMC_NS@ PR6004 1/4W_2.2_5%_0603
P_3VALW_SNB
EMC_NS@ PC6006 1000P_50V_K_X7R_0201

P_3VALW
EMC_NS@ PC6007 2200P_25V_K_X7R_0201
EMC@ PC6008 0.1U_25V_K_X5R_0201
PC6010 22U_6.3V_M_X5R_0603
PC6009 22U_6.3V_M_X5R_0603
PC6001 22U_6.3V_M_X5R_0603
PC6012 22U_6.3V_M_X5R_0603
PC6014 22U_6.3V_M_X5R_0603
PC6013 22U_6.3V_M_X5R_0603
RF_NS@ PC6015 100P_50V_J_NPO_0201
RF_NS@ PC6016 47P_25V_J_NPO_0201

+3VALW
PJ6001 JUMP_43X118 @

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: +3VALW
LCFC
Size: Custom | Document Number: Serval 2/Phoenix AMD | Rev: 0.1
Date: Wednesday, March 02, 2022 | Sheet 52 of 62

Part Reference:
PX5701~PX57**

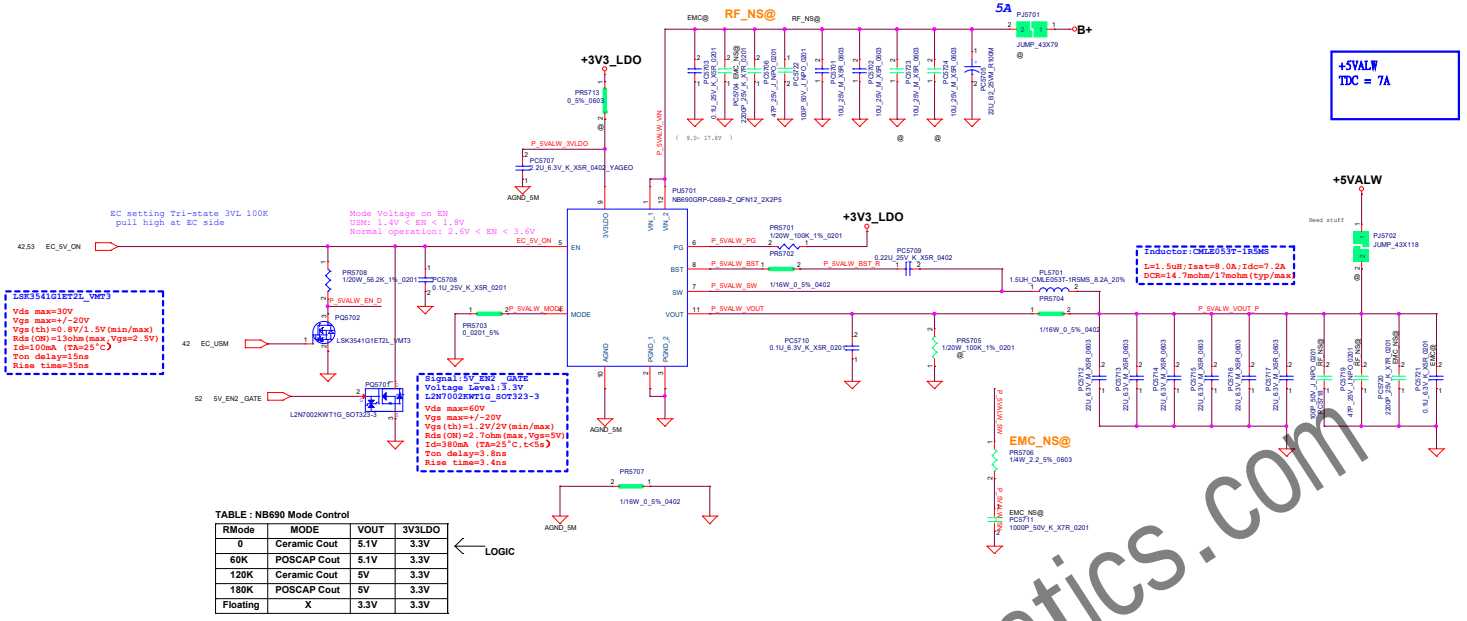


TABLE : NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

LOGIC

Part Reference:
PX8001~PX80**

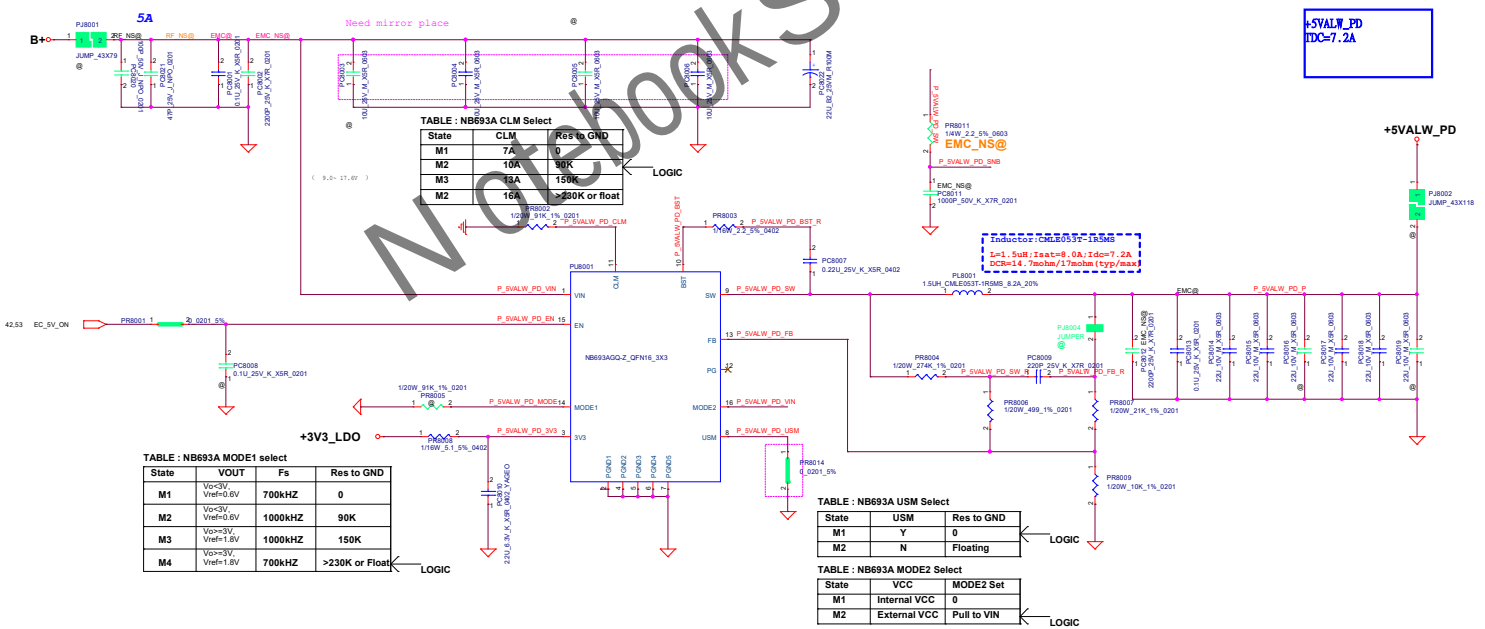


TABLE : NB693A CLM Select

State	CLM	Res to GND
M1	7A	0
M2	10A	90K
M3	13A	150K
M2	16A	>230K or float

LOGIC

TABLE : NB693A MODE1 select

State	VOUT	Fs	Res to GND
M1	Vo<3V, Vref=0.6V	700kHZ	0
M2	Vo<3V, Vref=0.6V	1000kHZ	90K
M3	Vo>=3V, Vref=1.8V	1000kHZ	150K
M4	Vo>=3V, Vref=1.8V	700kHZ	>230K or Float

LOGIC

TABLE : NB693A USM Select

State	USM	Res to GND
M1	Y	0
M2	N	Floating

LOGIC

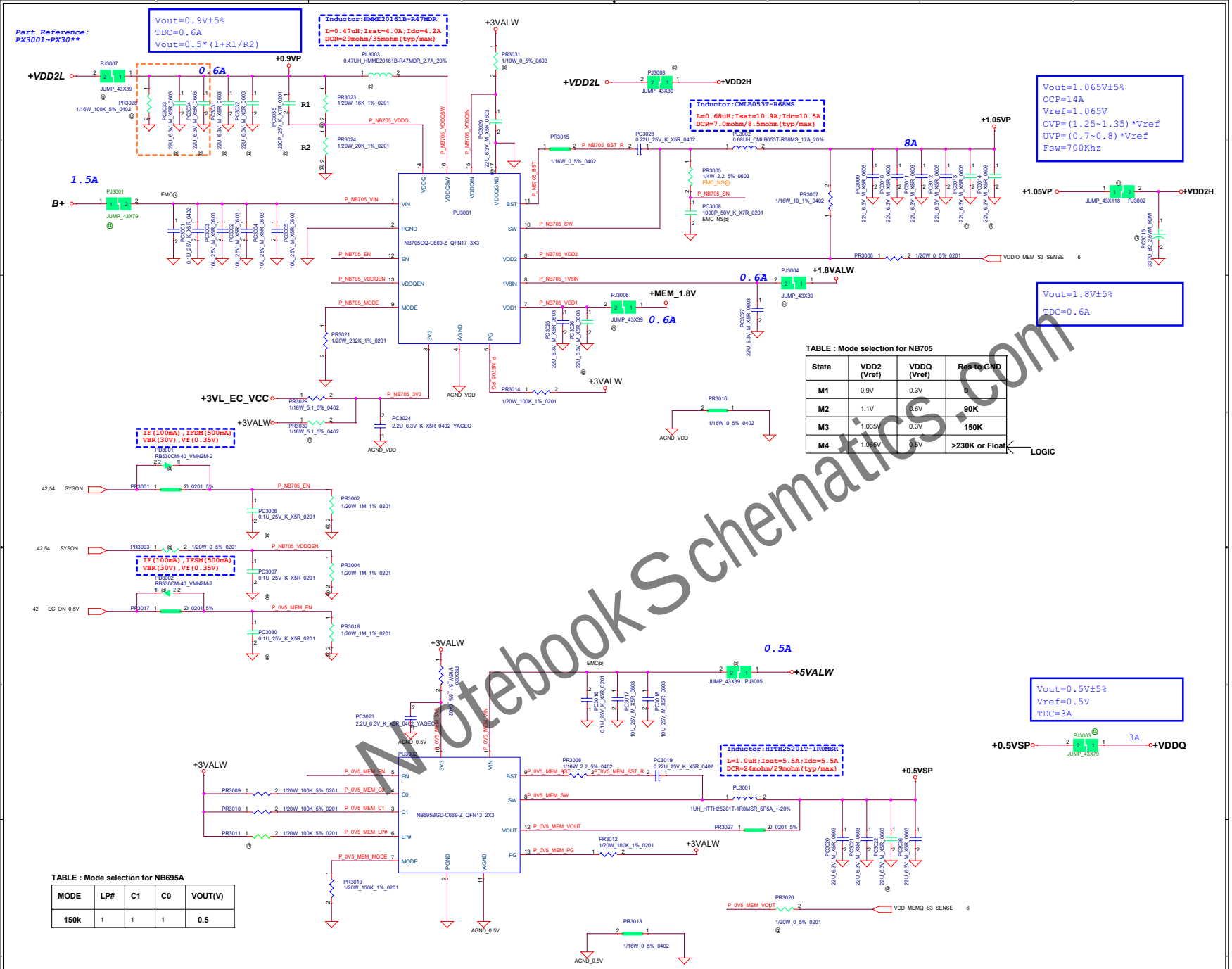
TABLE : NB693A MODE2 Select

State	VCC	MODE2 Set
M1	Internal VCC	0
M2	External VCC	Pull to VIN

LOGIC

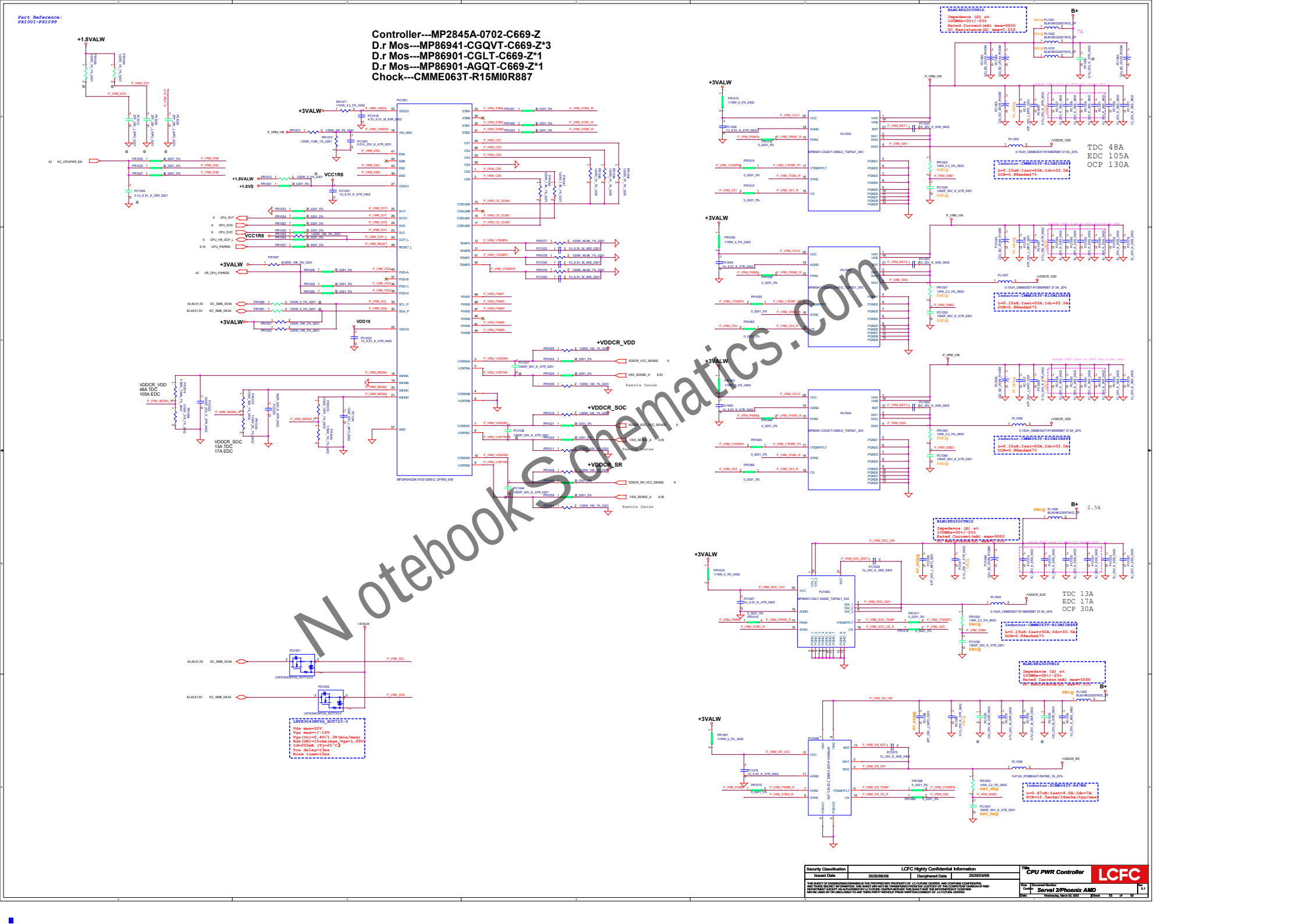
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	5VALW&+5VALW_PD	LCFC
Size	Document Number	Rev 0.1
Custom	Serval 2/Phoenix AMD	
Date:	Wednesday, March 02, 2022	Sheet 53 of 62



Part Reference:
PX1001-PX1099

Controller---MP2845A-0702-C669-Z
D.r Mos---MP86941-CGQVT-C669-Z*3
D.r Mos---MP86901-CGLT-C669-Z*1
D.r Mos---MP86901-AGQT-C669-Z*1
Chock---CMME063T-R15MI0R887



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	CPU PWR Controller	LCFC	
Size	Document Number	Rev	
Custom	Serval 2/Phoenix AMD	0.5	
Date:	Wednesday, March 02, 2022	Sheet	55 of 62

Part Reference:
PX1100~PX12**

+VDDCR_VDD

Place on Bot side

Place on TOP side

Note--Rembrandt
470uF/4.5mohm*7pcs D2+220uF/6mohm D2*4
22uF/0603*12pcss
22uF/0402*40pcs

Place on VR side

All BU(on bot side beside CPU)

+VDDCR_SOC

Rembrandt
470uF/4.5mohm*2pcs D2+220uF/6mohm D2*1
22uF/0603*6pcs
22uF/0402*20 pcs

All BU(on bot side beside CPU)

+VDDCR_VDD

All BU(on top side under CPU)

+VDDCR_SOC

All BU(on top side under CPU)

Place on VR side

+VDDCR_SR

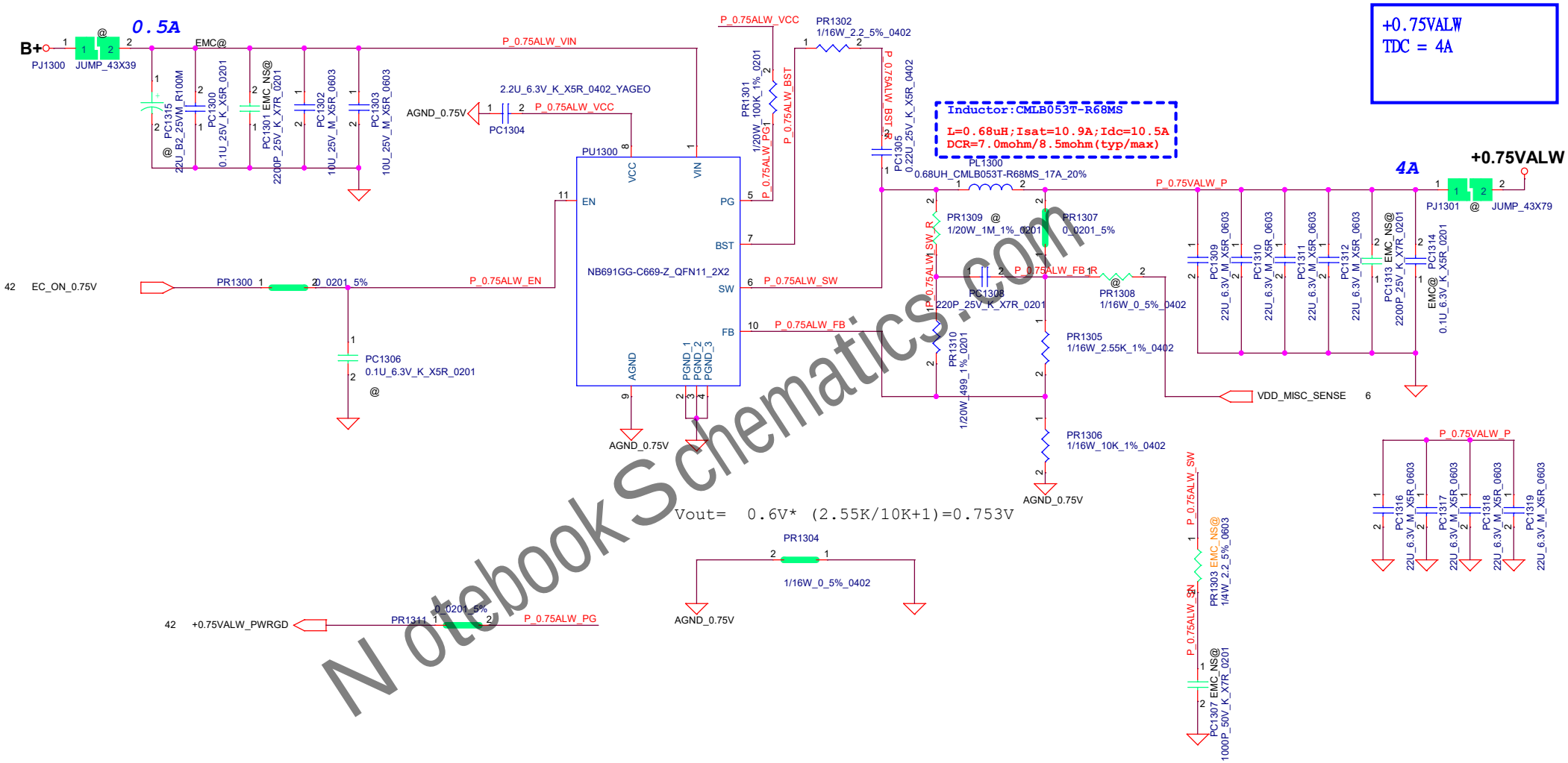
Rembrandt
22uF/0603*8pcs
10uF/0402*2pcs

Place on VR side

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PWR Decoupling	LCFC	
Size C	Document Number Serval 2/Phoenix AMD		Rev 0.1
Date: Wednesday, March 02, 2022	Sheet 56 of 62		

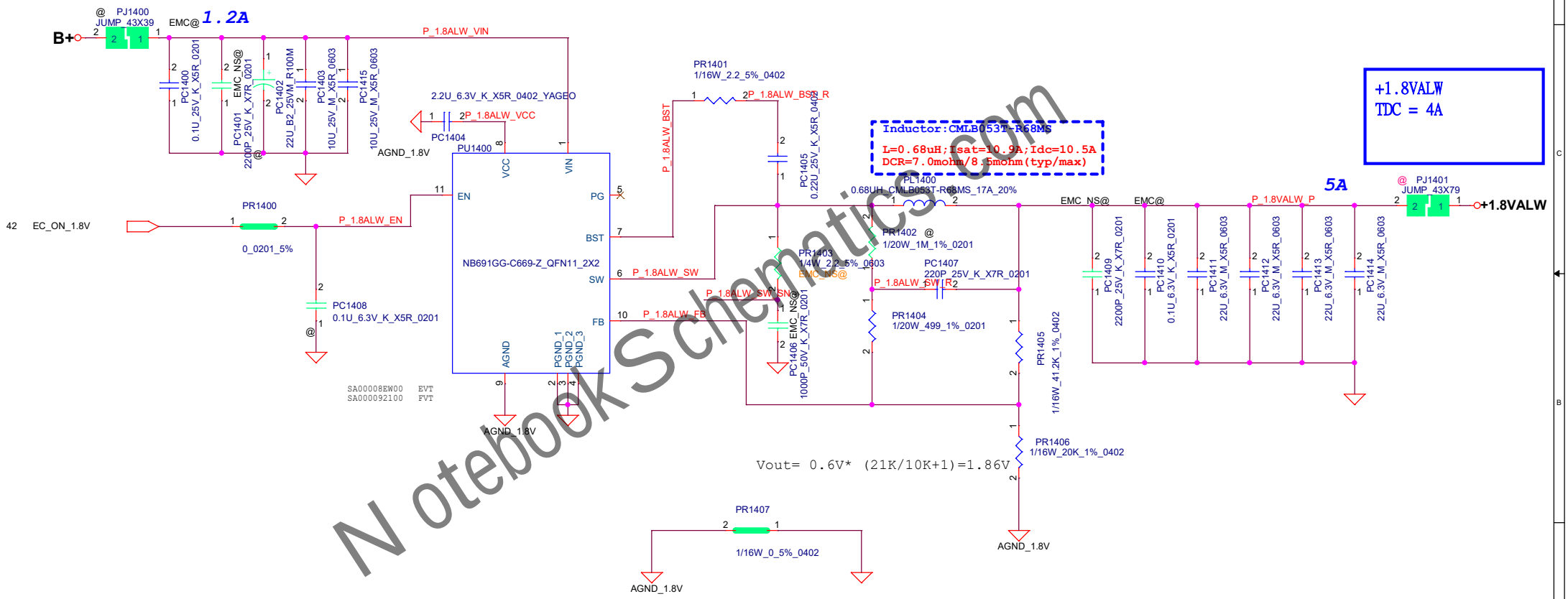
Part Reference:
PX1300~PX1399



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PWR1_+0.75VALW		LCFC
Size	Document Number		Rev
B	Serval 2/Phoenix AMD		0.1
Date:	Wednesday, March 02, 2022	Sheet 57 of 62	

Part Reference:
PX1400~PX1499



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PWR2_+1.8VALW		
Size	Document Number		Rev
B	Serval 2/Phoenix AMD		0.1
Date:	Wednesday, March 02, 2022	Sheet	58 of 62

Part Reference:
PX1500~PX1599

+VDD_11
IDC=5A
Vout =1.1V

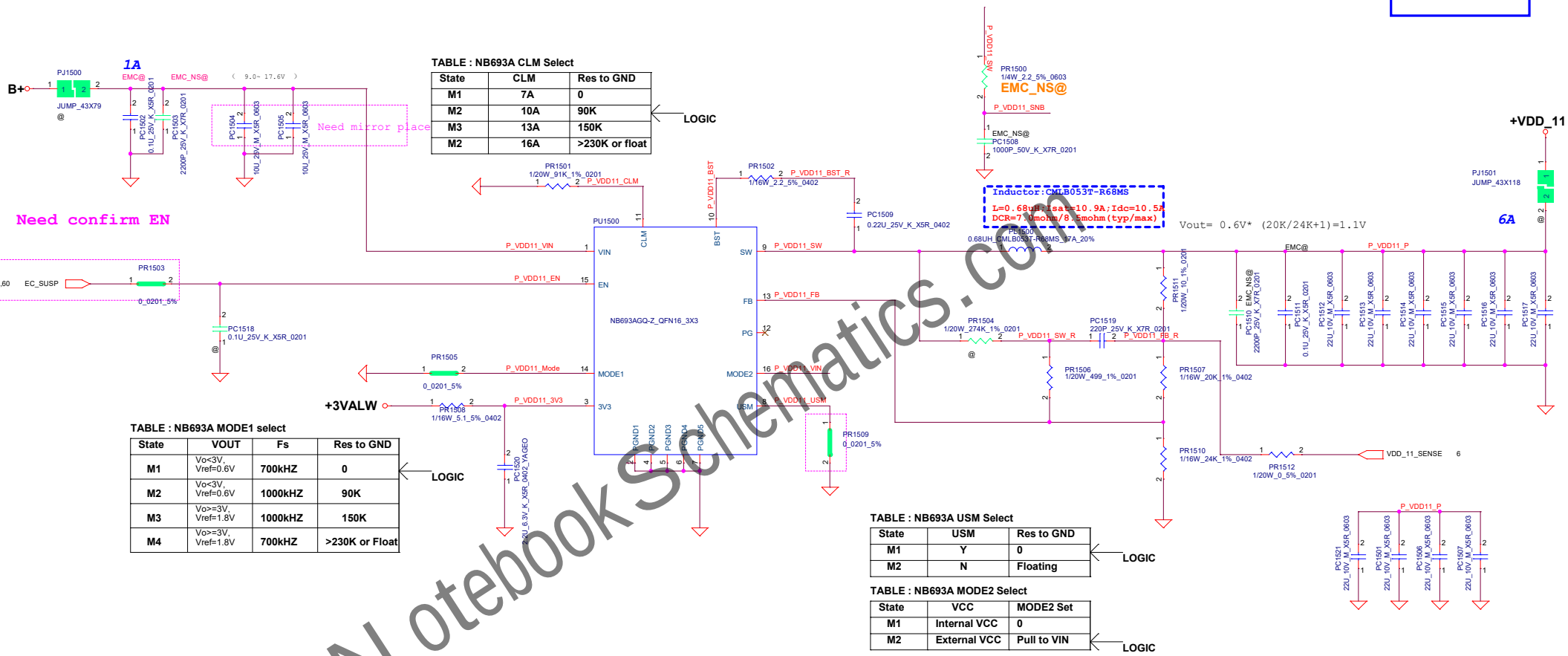


TABLE : NB693A CLM Select

State	CLM	Res to GND
M1	7A	0
M2	10A	90K
M3	13A	150K
M2	16A	>230K or float

LOGIC

TABLE : NB693A MODE1 select

State	VOUT	Fs	Res to GND
M1	Vo<3V, Vref=0.6V	700kHZ	0
M2	Vo<3V, Vref=0.6V	1000kHZ	90K
M3	Vo>=3V, Vref=1.8V	1000kHZ	150K
M4	Vo>=3V, Vref=1.8V	700kHZ	>230K or Float

LOGIC

TABLE : NB693A USM Select

State	USM	Res to GND
M1	Y	0
M2	N	Floating

LOGIC

TABLE : NB693A MODE2 Select

State	VCC	MODE2 Set
M1	Internal VCC	0
M2	External VCC	Pull to VIN

LOGIC

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PWR3_+VDD_11

LCFC

Size: Custom | Document Number: Serval 2/Phoenix AMD | Rev: 0.1

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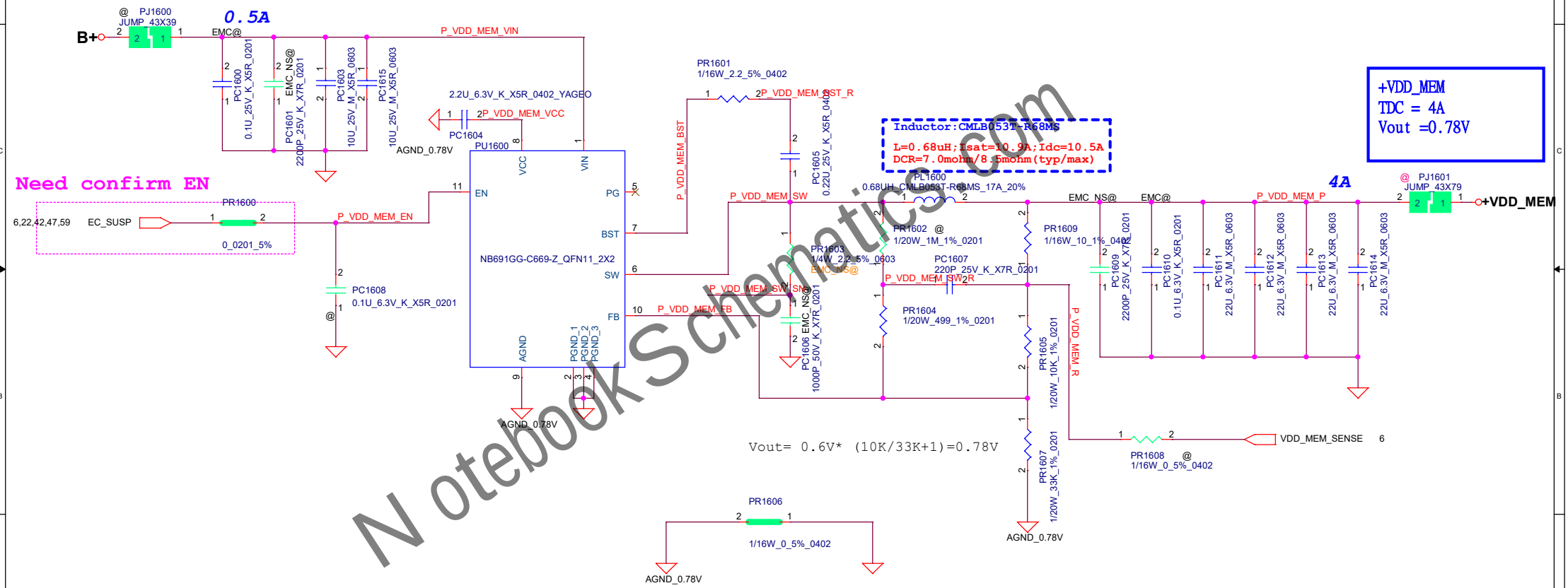
Part Reference:
PX1600~PX1699



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PWR4_+VDD_MEM		LCFC
Size	Document Number		Rev
B	Serval 2/Phoenix AMD		0.1
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Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *Change List_EE*

LCFC

Size	Document Number	Rev
C	*Serval 2/Phoenix AMD*	0.1

Date: Wednesday, March 02, 2022 Sheet 61 of 62

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

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Title: Notes_For BOM

LCFC

Size: Custom	Document Number: Serval 2/Phoenix AMD	Rev: 0.1
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