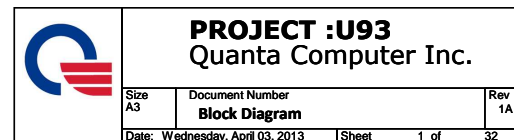
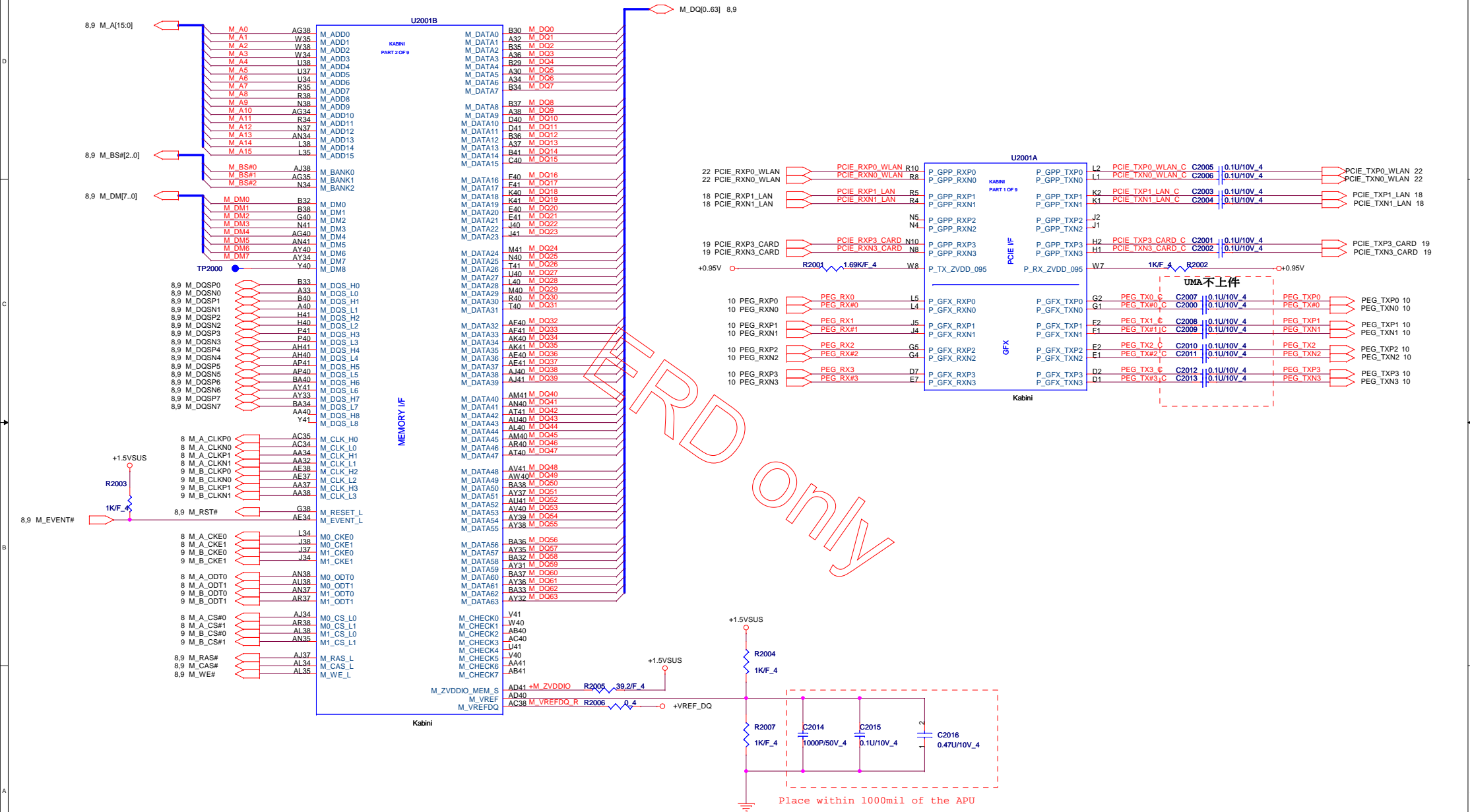
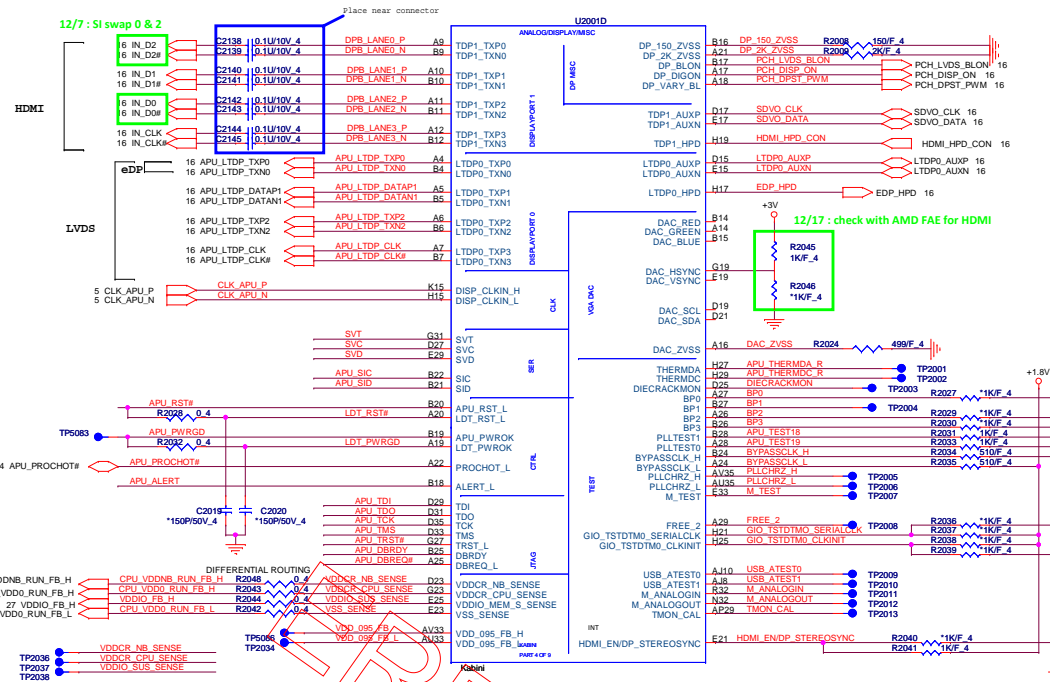
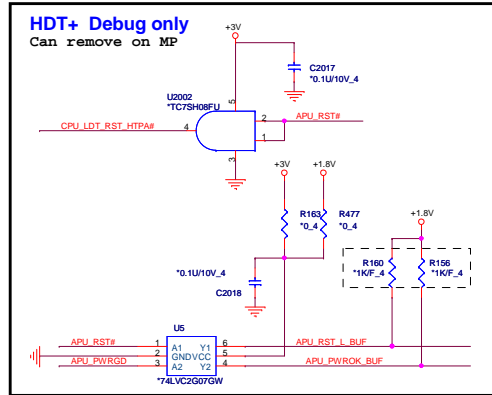
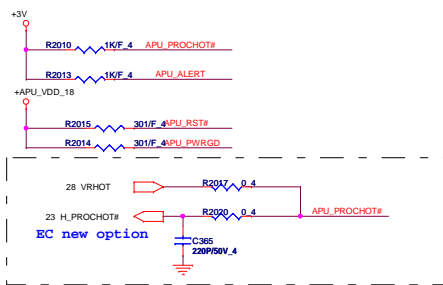


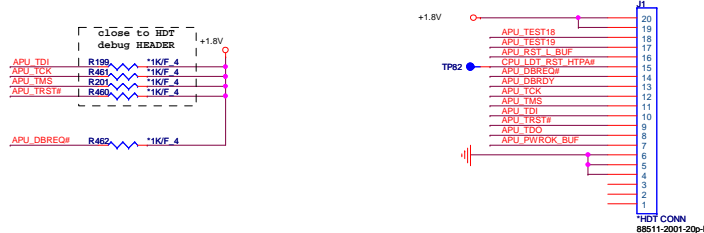
Ultra/Slim⁰¹



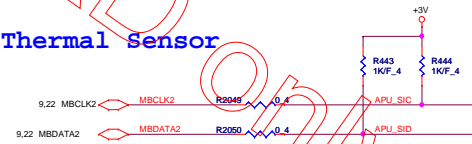




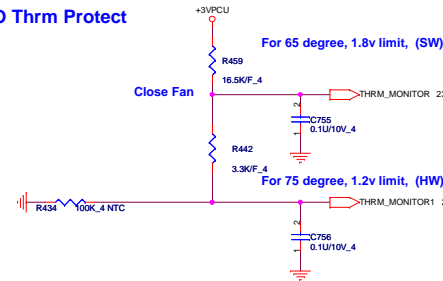
HDT+ Connector for Debug only



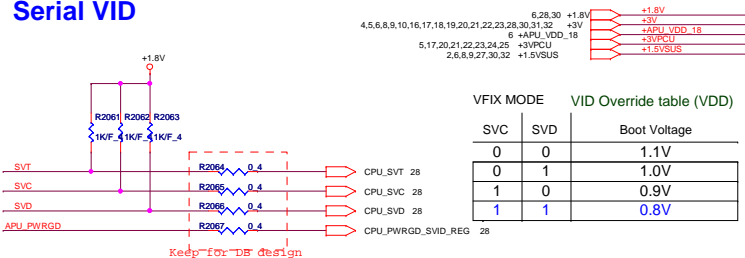
Thermal Sensor

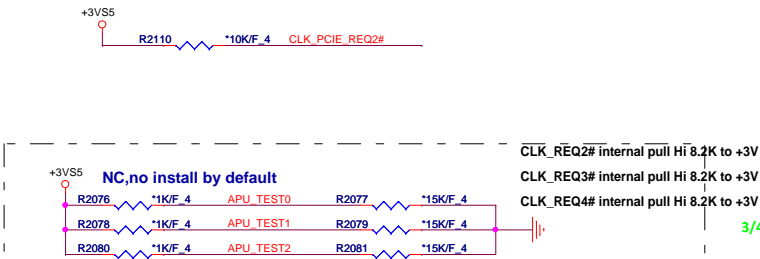
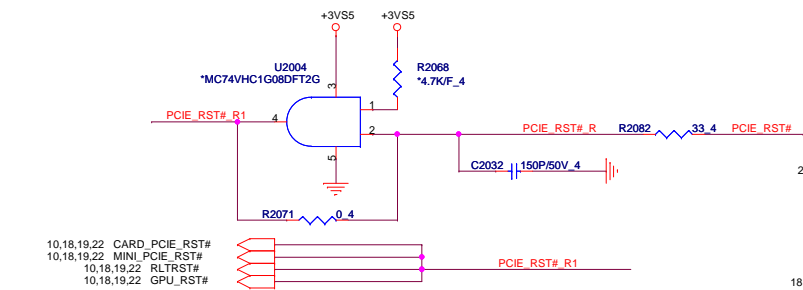


IO Thrm Protect

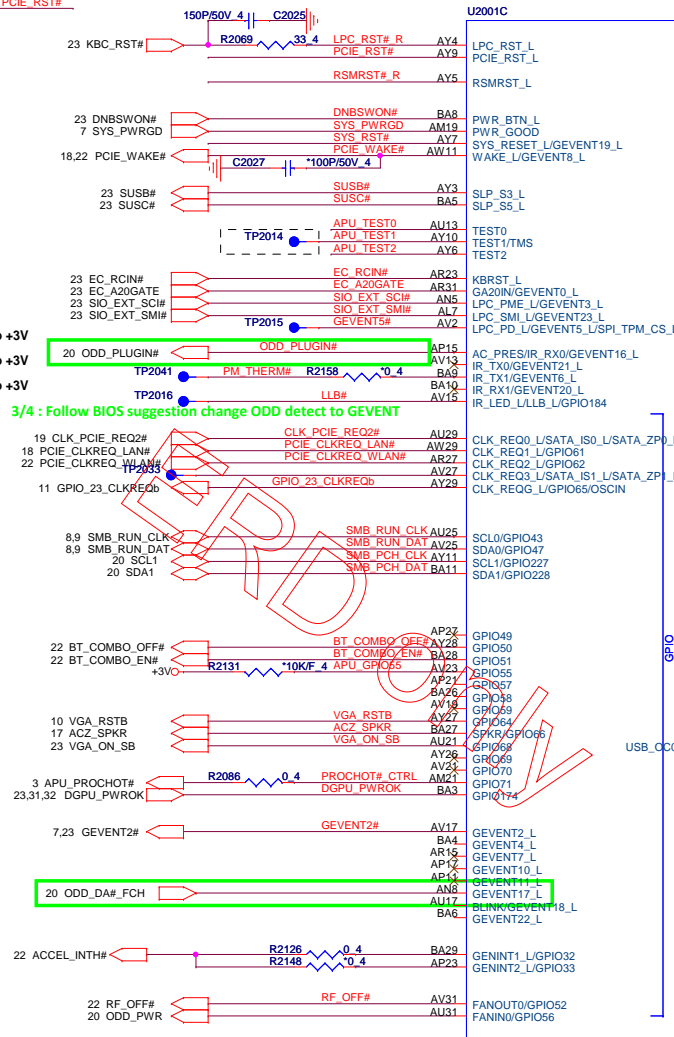
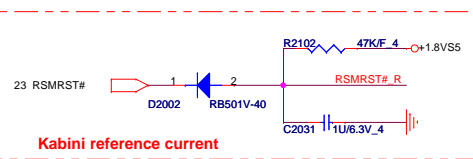
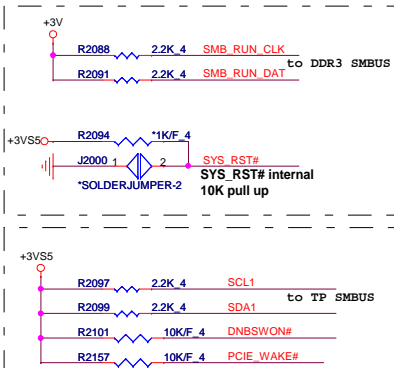


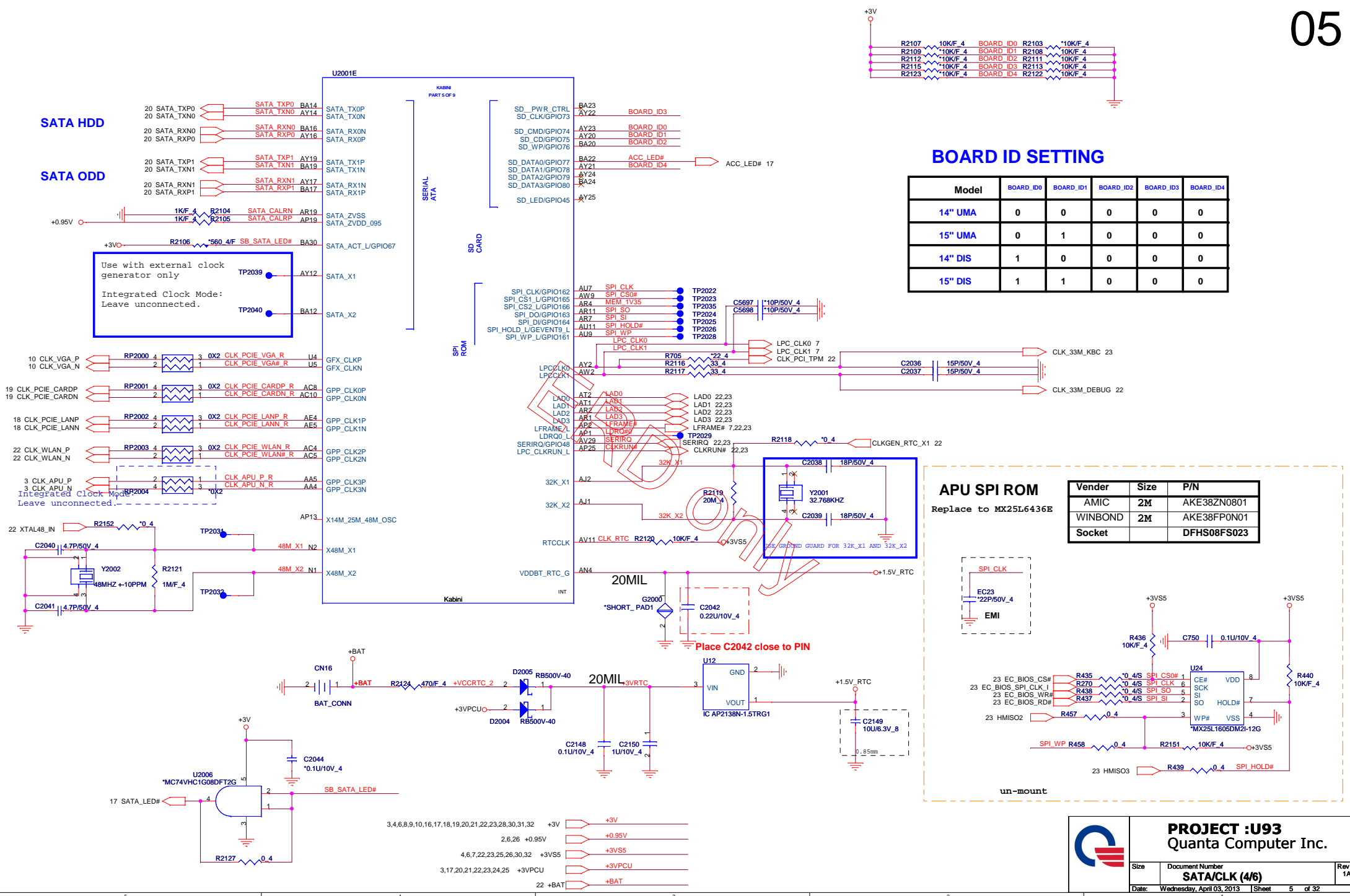
Serial VID

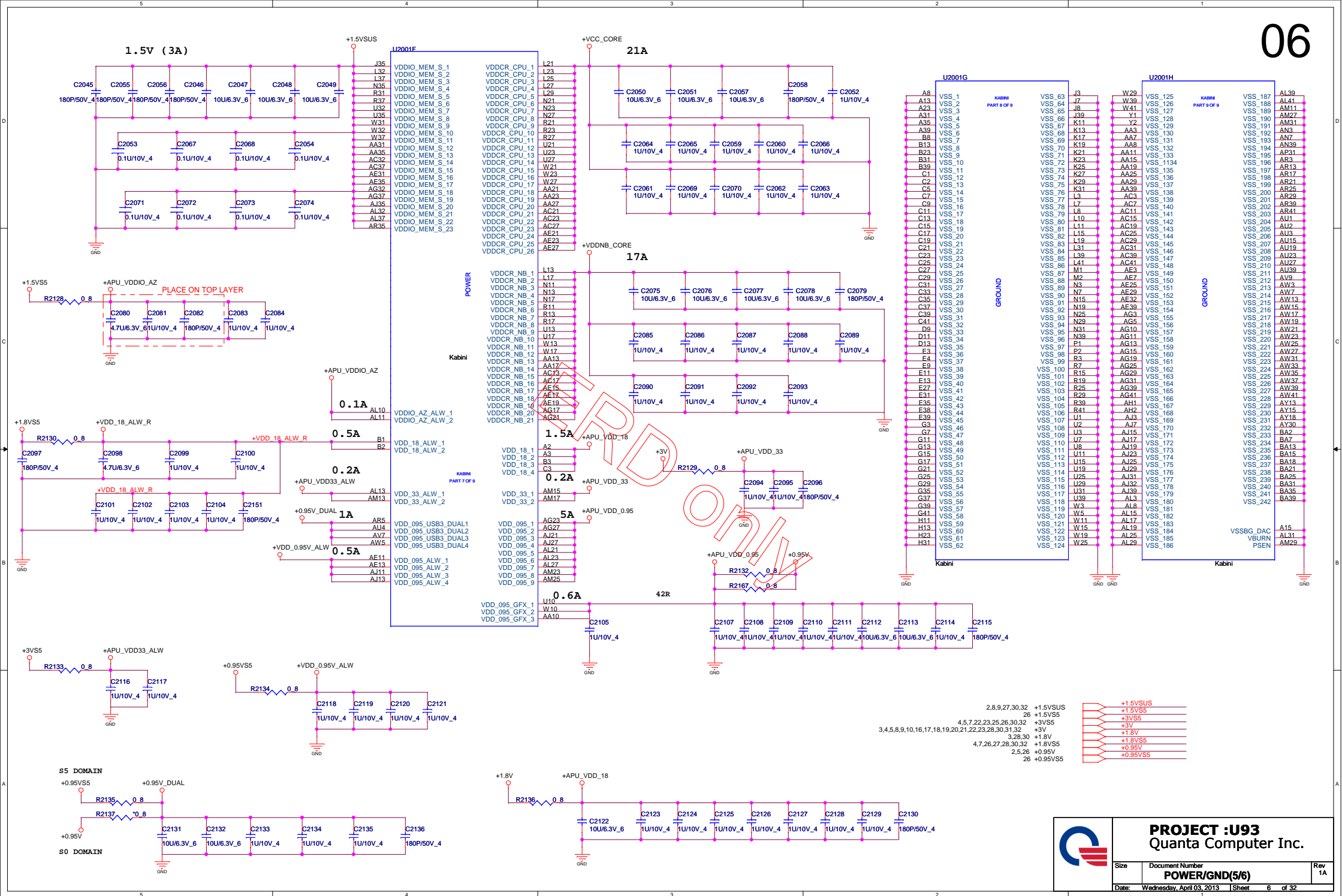




TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



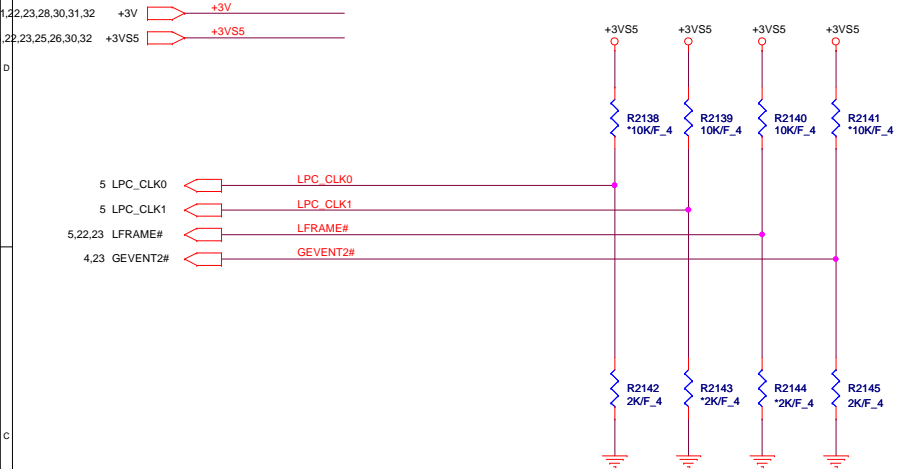




RAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

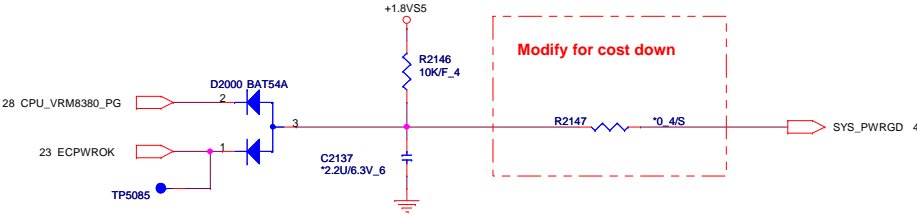
DEBUG STRAPS

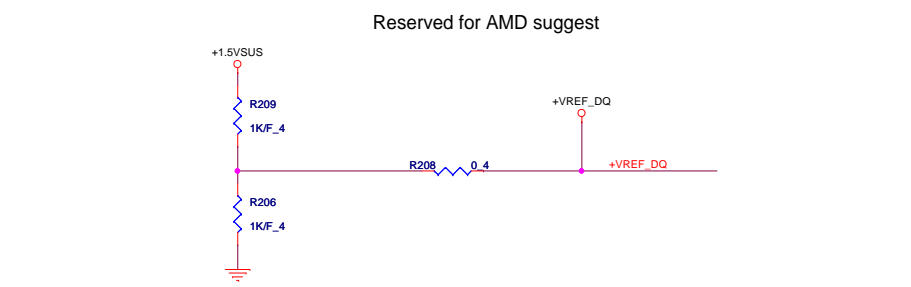
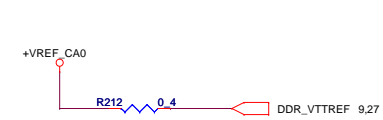


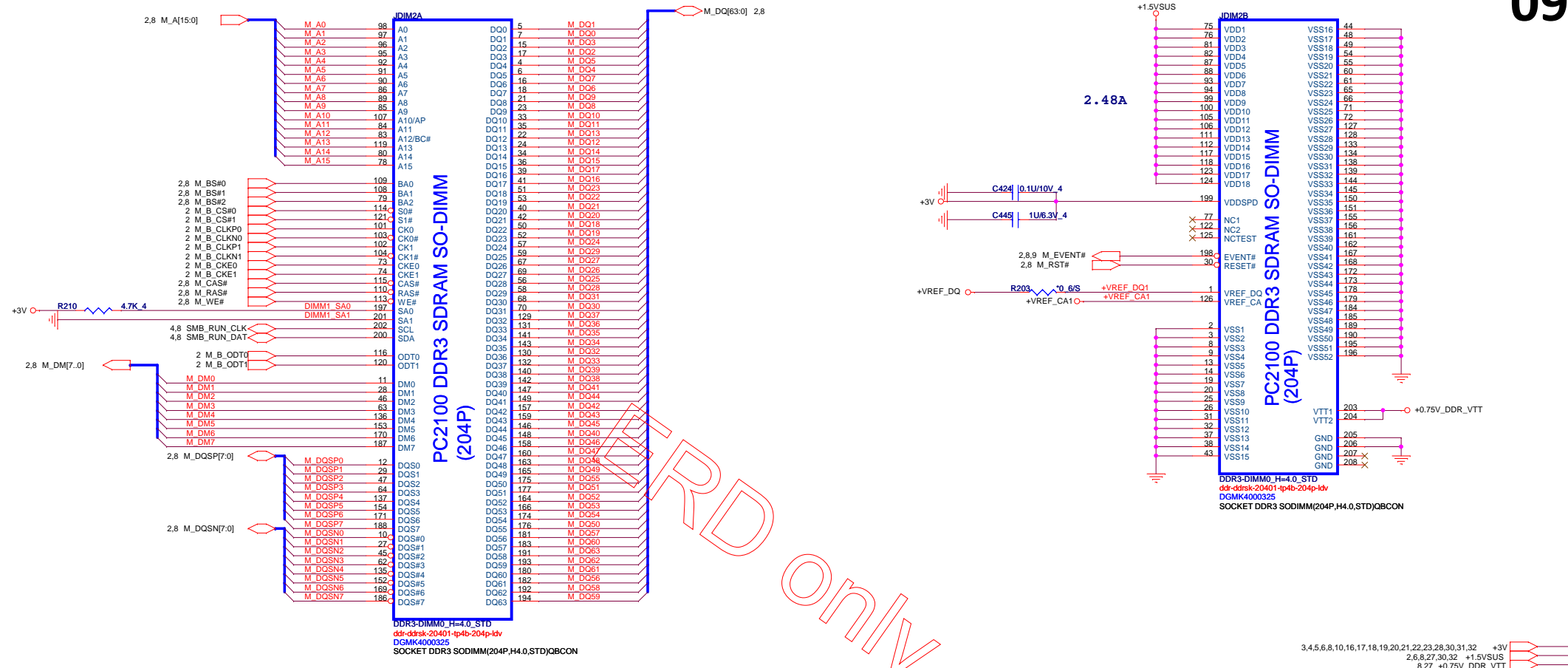
REQUIRED STRAPS

					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

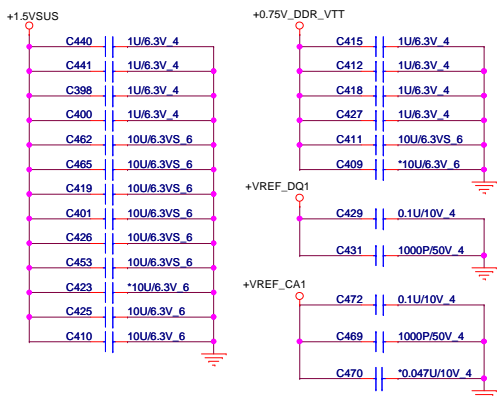
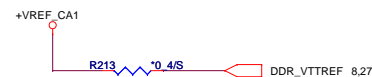
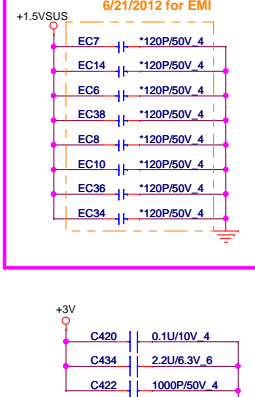
SYS_PWRGD





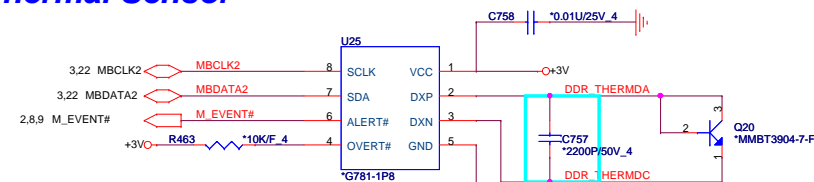


Place these Caps near So-Dimm1.

For EMI RESERVE
6/21/2012 for EMI

Local Thermal Sensor

DDR3 Thermal Sensor

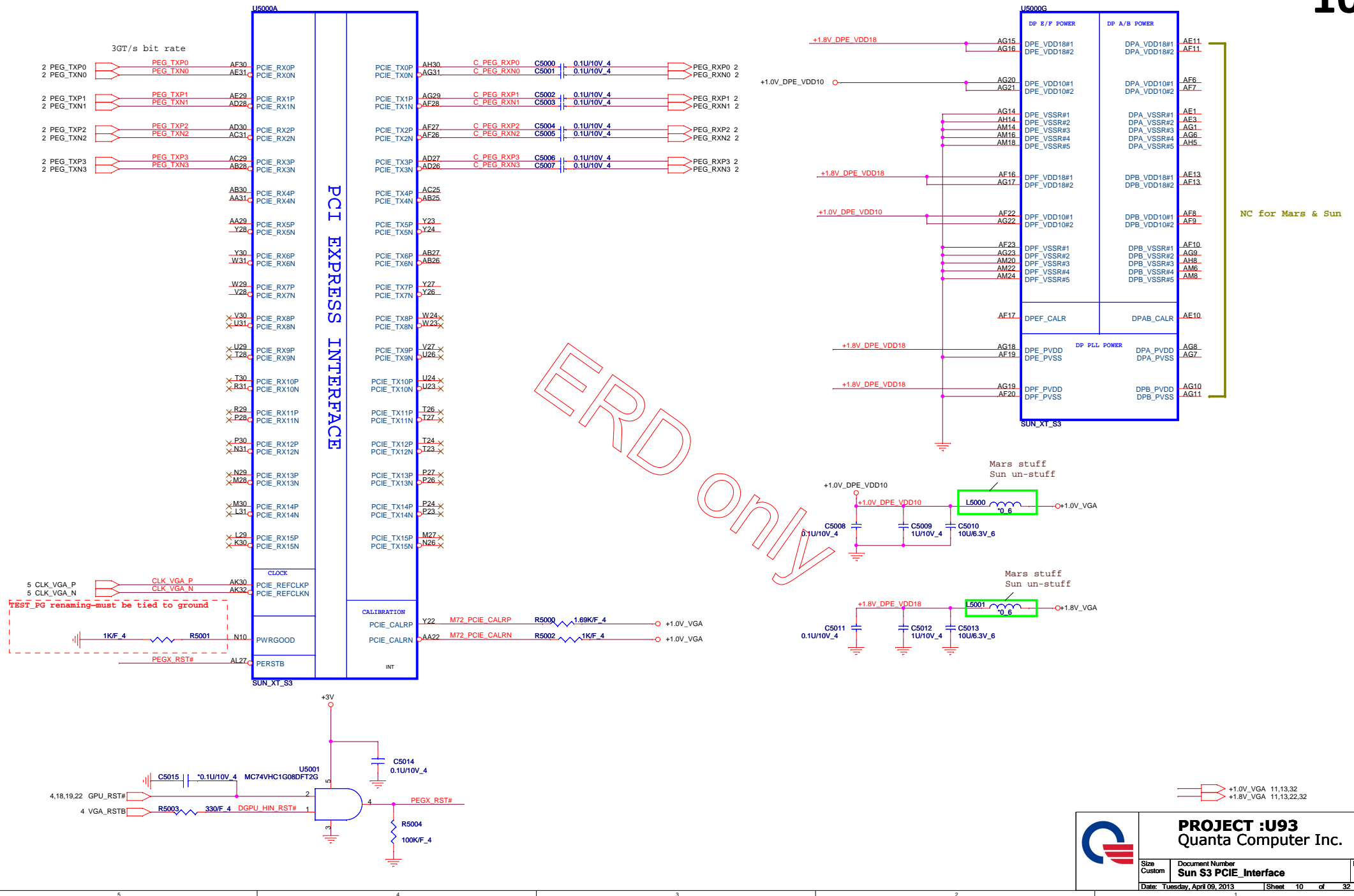


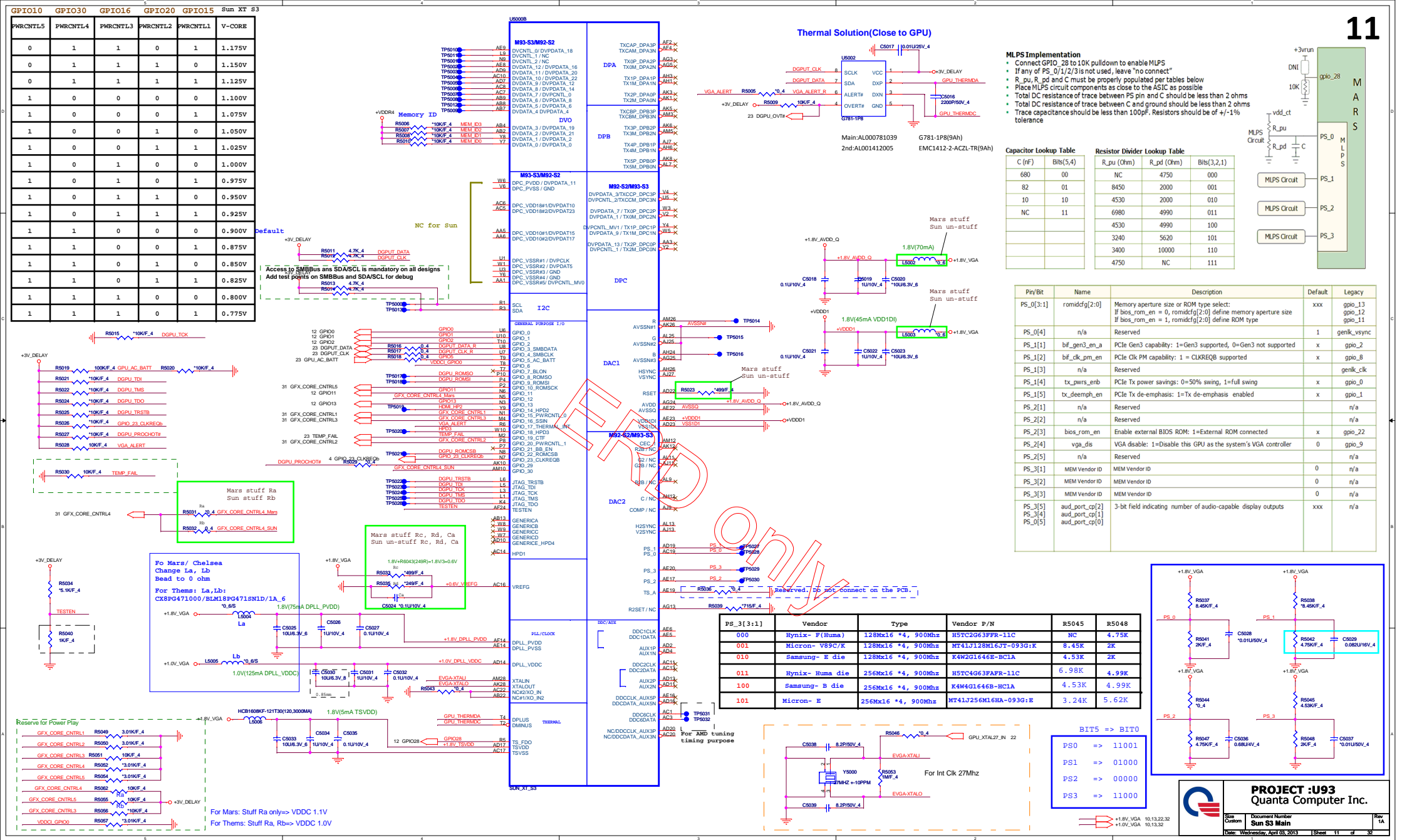
If use internal thermal IC, C9007 use 0ohm.

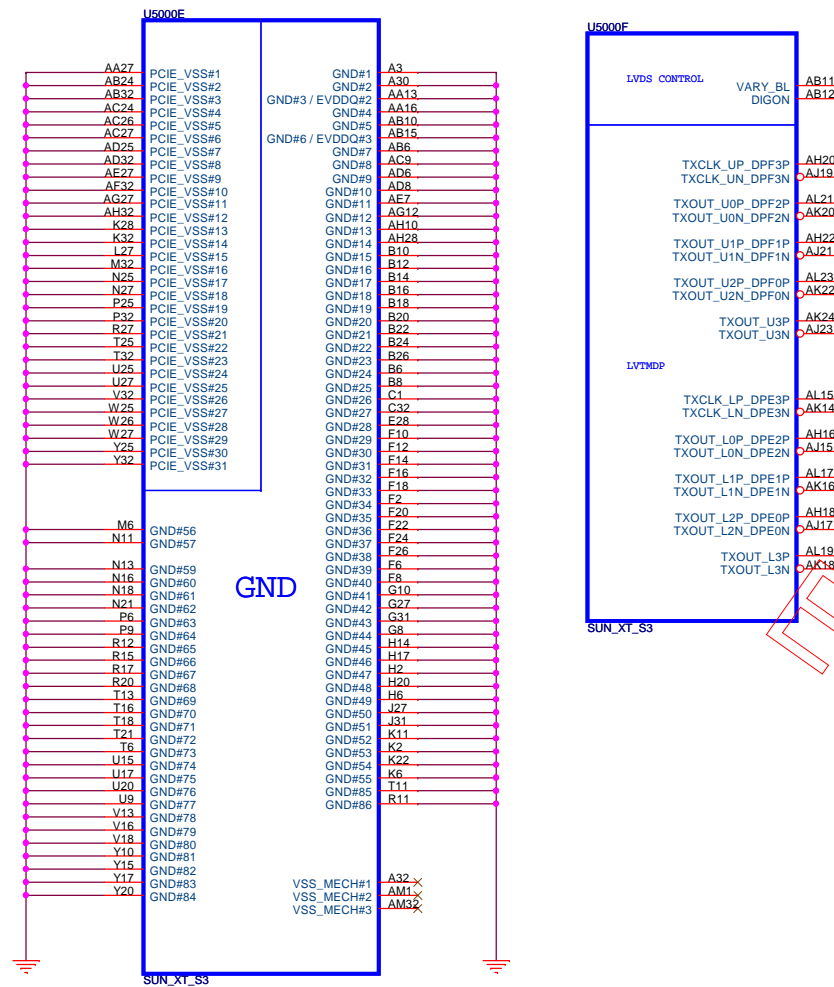
Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

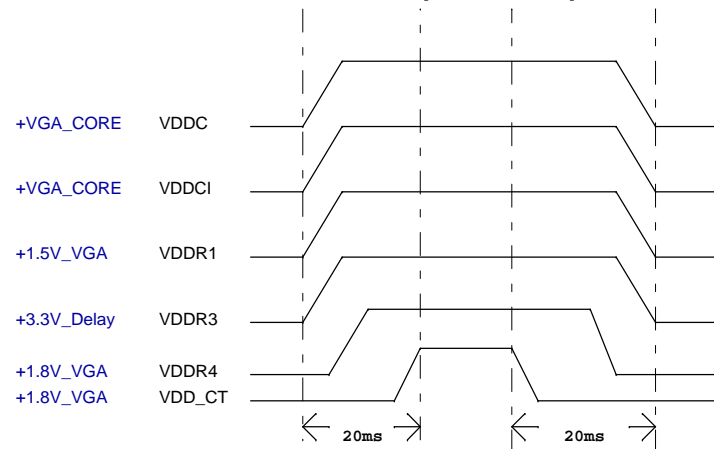
PROJECT :U93 Quanta Computer Inc.		
Size Custom	Document Number System Memory 2/2 (9.2H)	Rev 1A
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Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

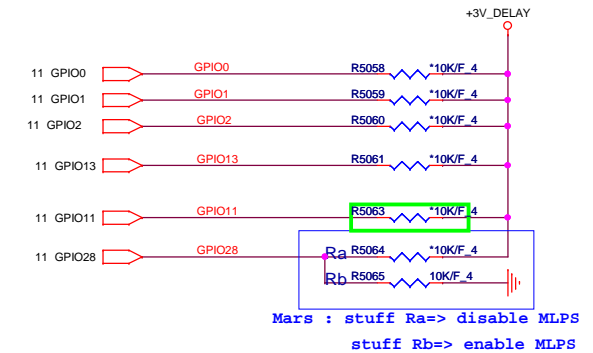
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

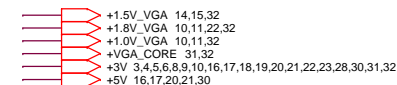
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

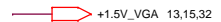
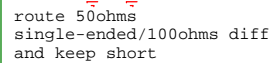
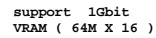
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

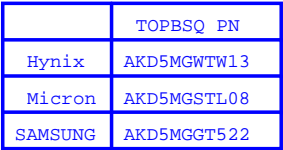


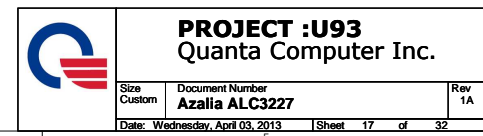
PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	Sun S3 GND / LVDS/ Straps	
Date: Wednesday, April 03, 2013	Sheet 12 of 32	



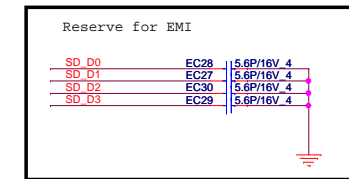




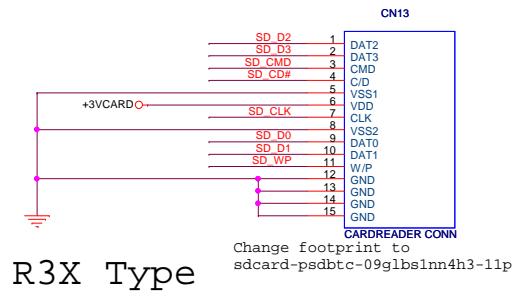


SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

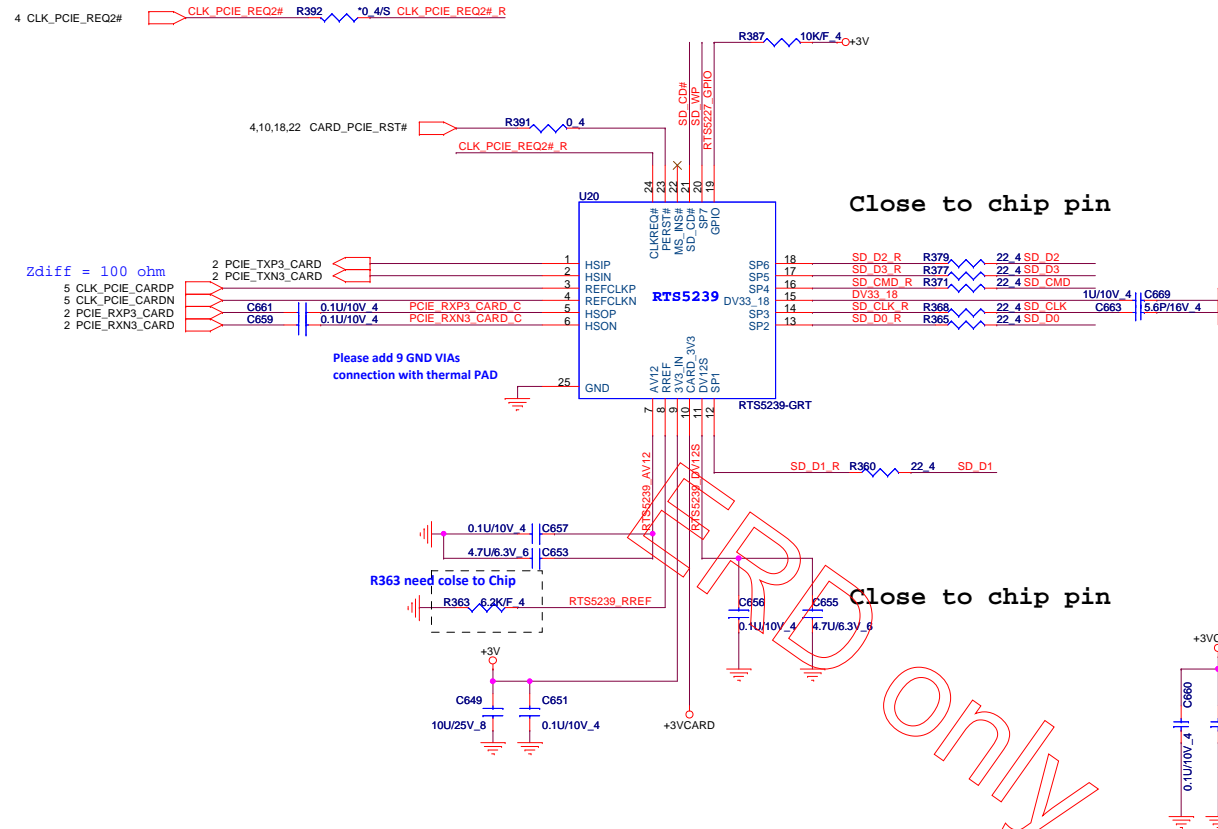
Share Pin



SD / MMC
CARD READER

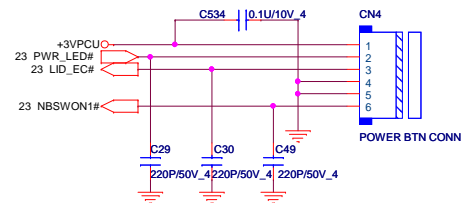


R3X Type

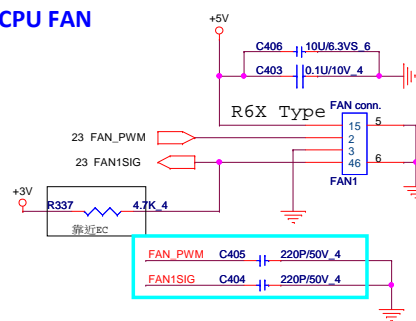


Power Button Connector

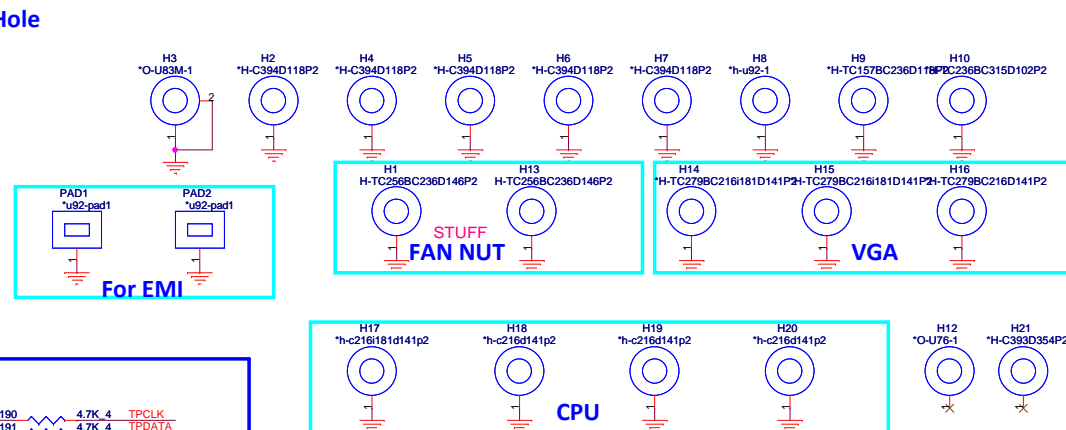
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



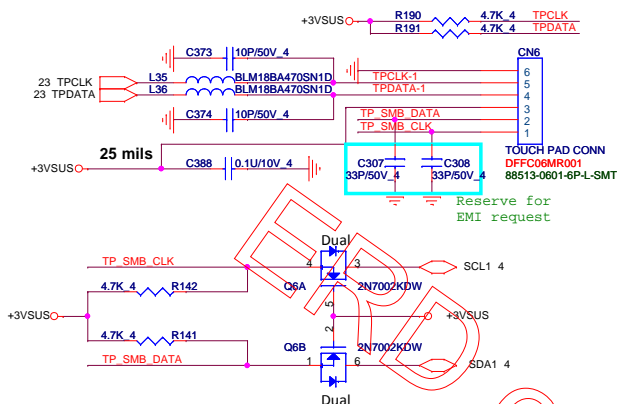
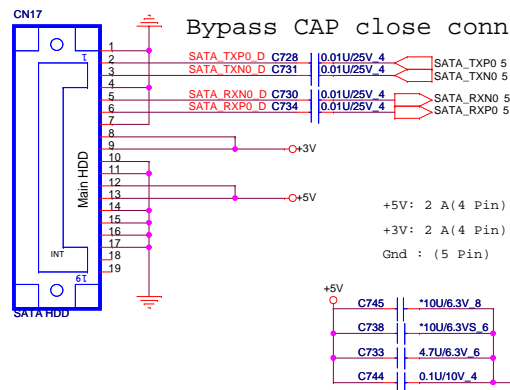
CPU FAN



Hole

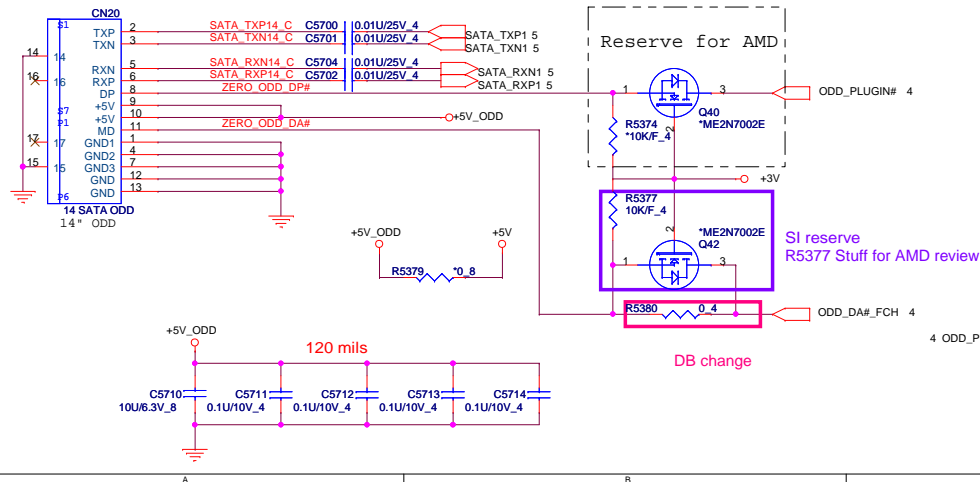


SATA HDD Connector(Cable type)



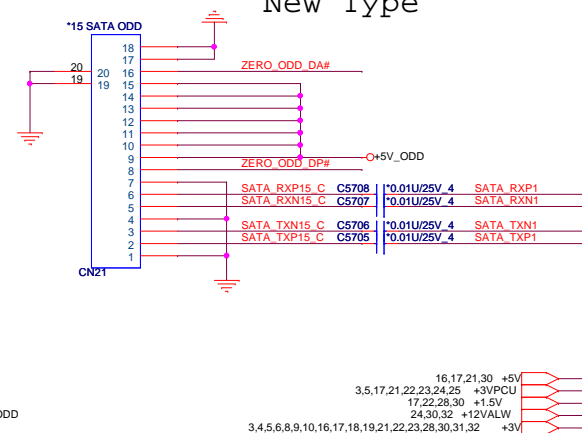
SATA ODD CONNECTOR

14" SATA ODD Bypass CAP close conn

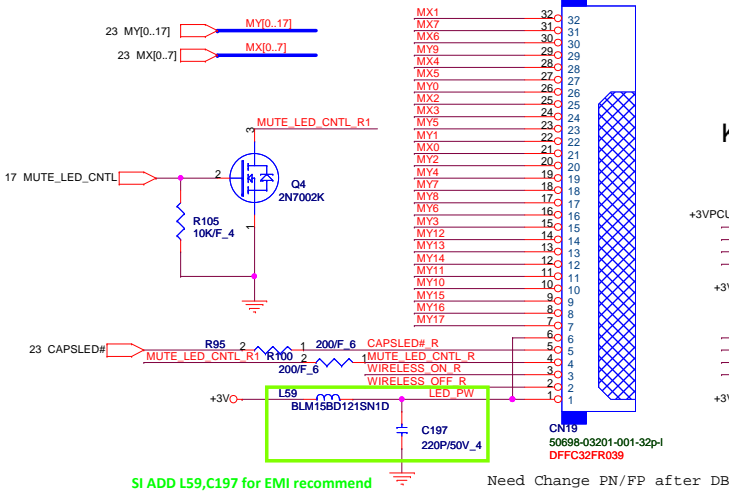


15" SATA ODD

New Type

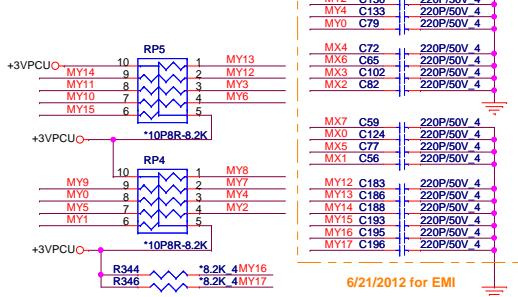


KEYBOARD Con.



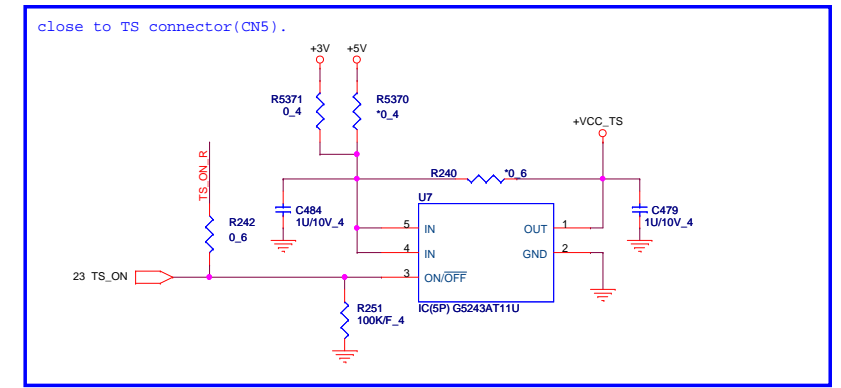
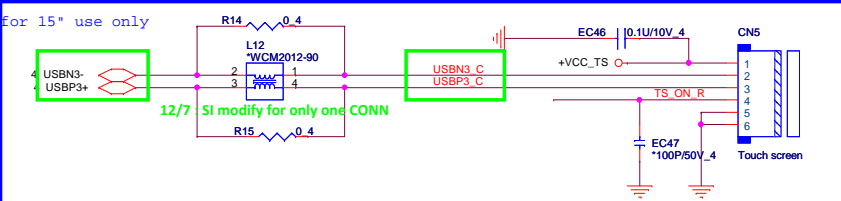
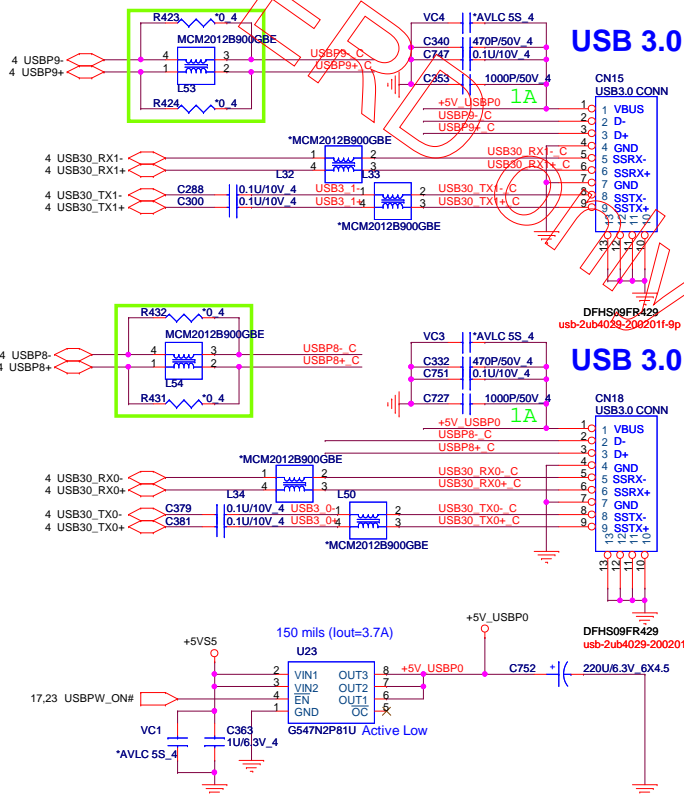
NM9 Type

KEYBOARD PULL-UP

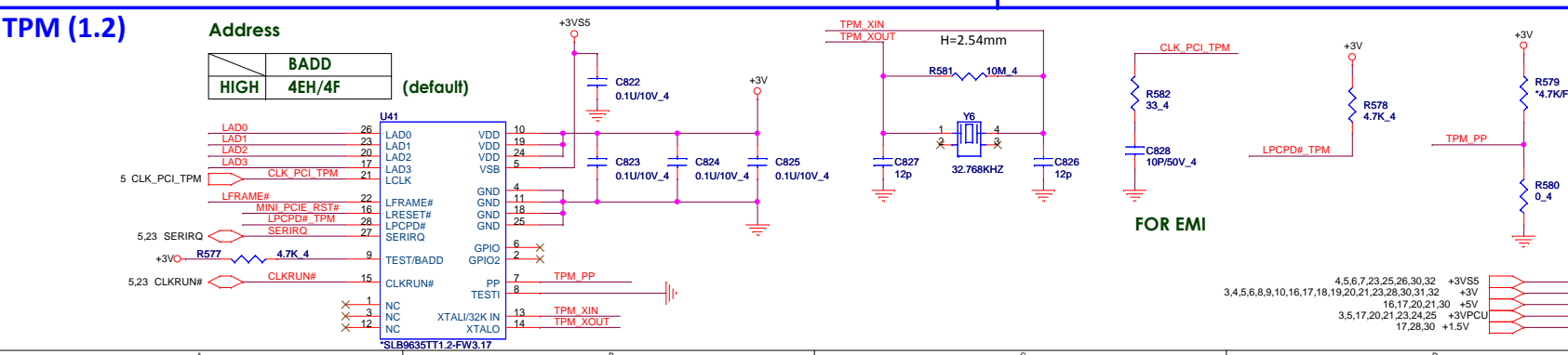
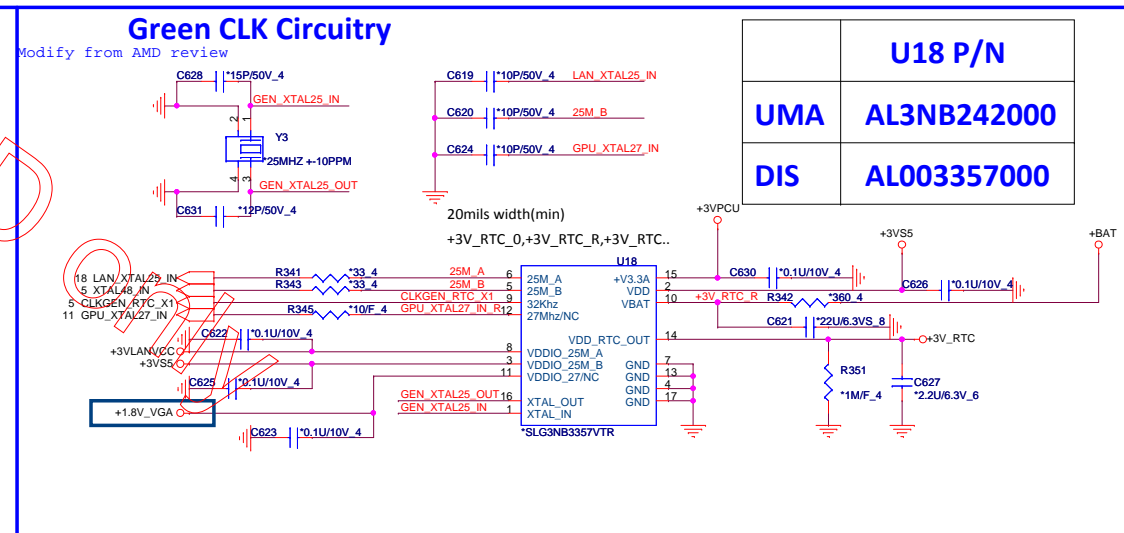
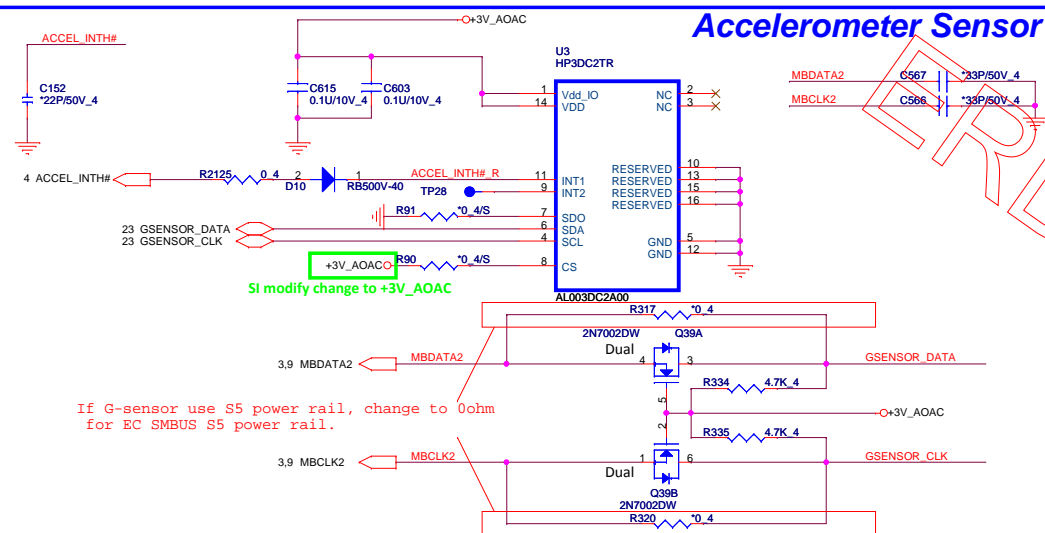
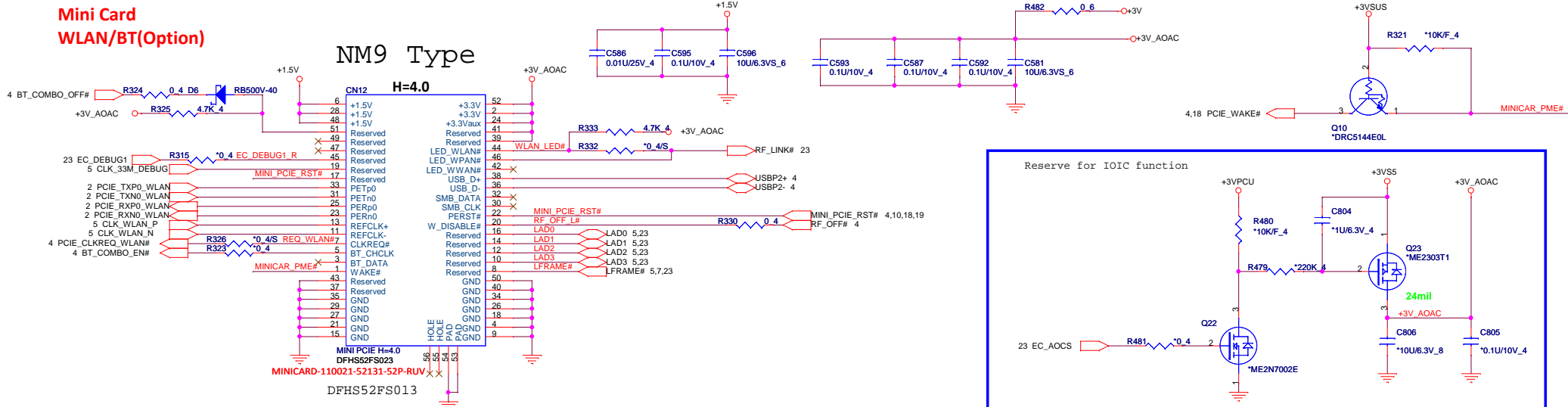



SPS Type

USB 3.0

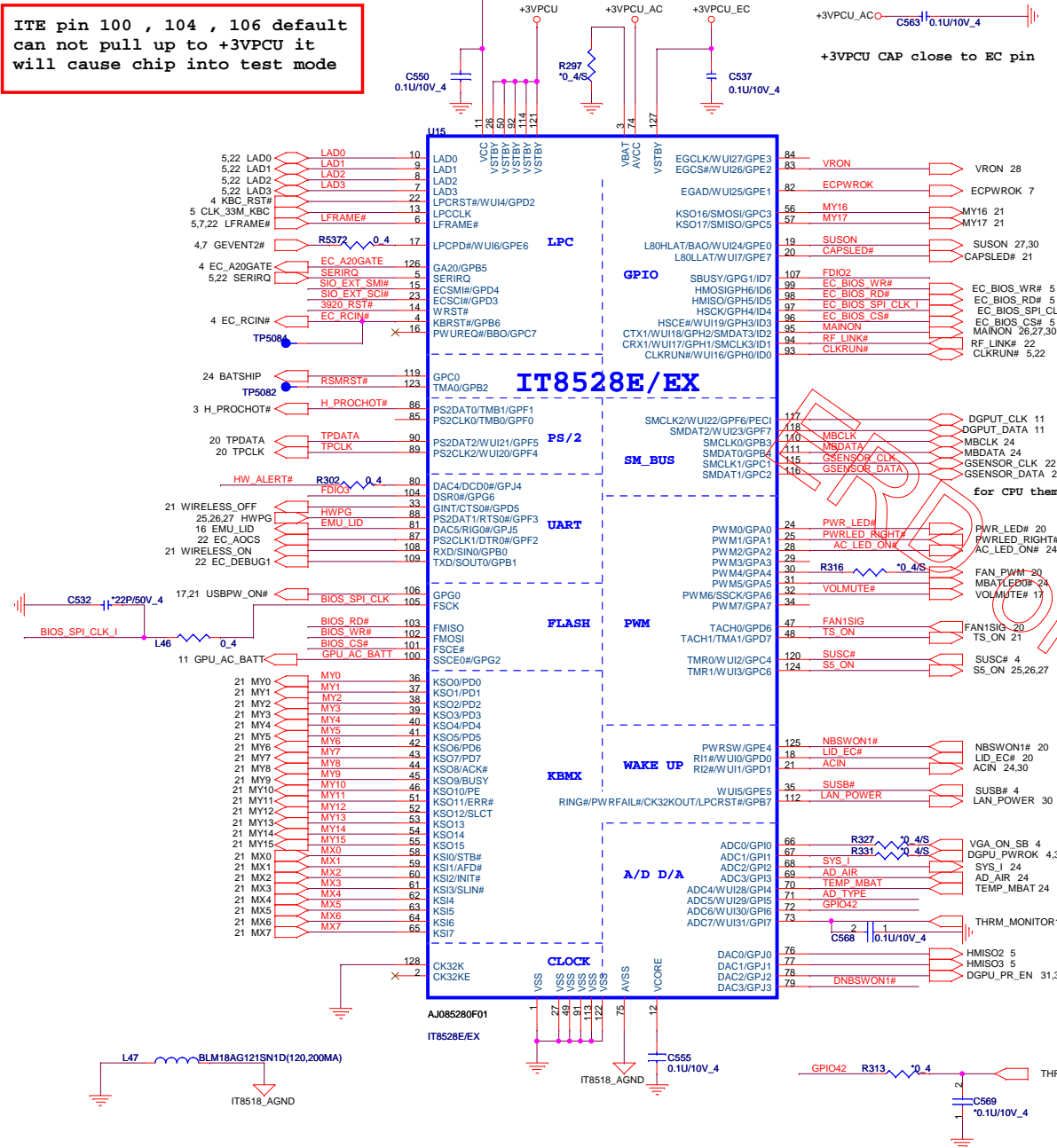


**Mini Card
WLAN/BT(Optional)**



	PROJECT :U93 Quanta Computer Inc.		
	Size Custom	Document Number MINI-PCIE/LED	Rev 1A
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ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode



Smart adapter Type check

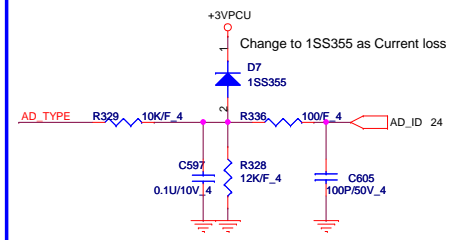


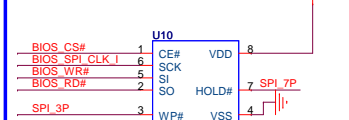
Diagram illustrating the power plane connections and decoupling capacitors:

- C549**: $0.1\mu/10V_4$ (connected to HWPG)
- C600**: $0.1\mu/10V_4$ (connected to FAN1SIG)
- C539**: $0.1\mu/10V_4$ (connected to DGPU_PR_EN)
- C546**: $100P/50V_4$ (connected to SERIRQ)

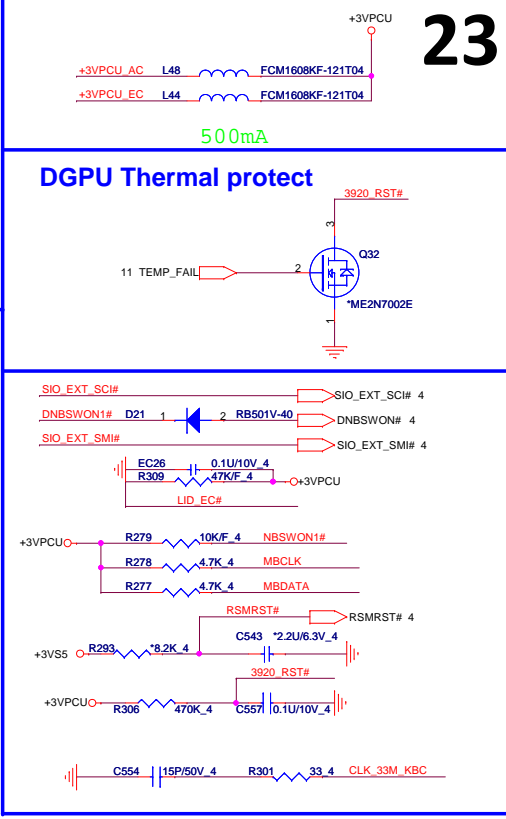
For +VIN noise

Vender	Size	P/N
AIT	4M	AKE392N0800
GGD	4M	AKE39GN0Q01
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

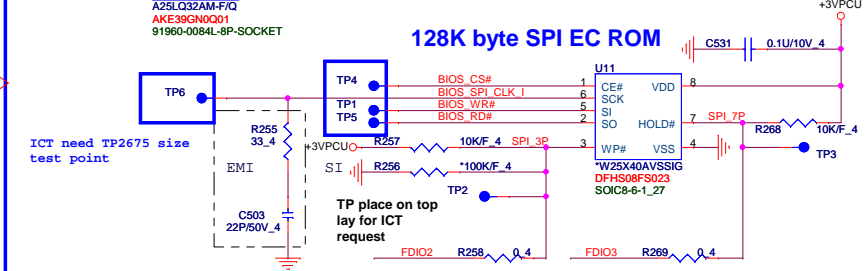
4M SPI EC ROM



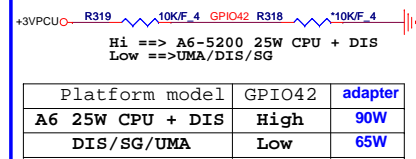
DGPU Thermal protect




128K byte SPI EC ROM

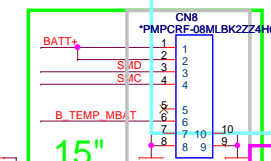


Adapter select



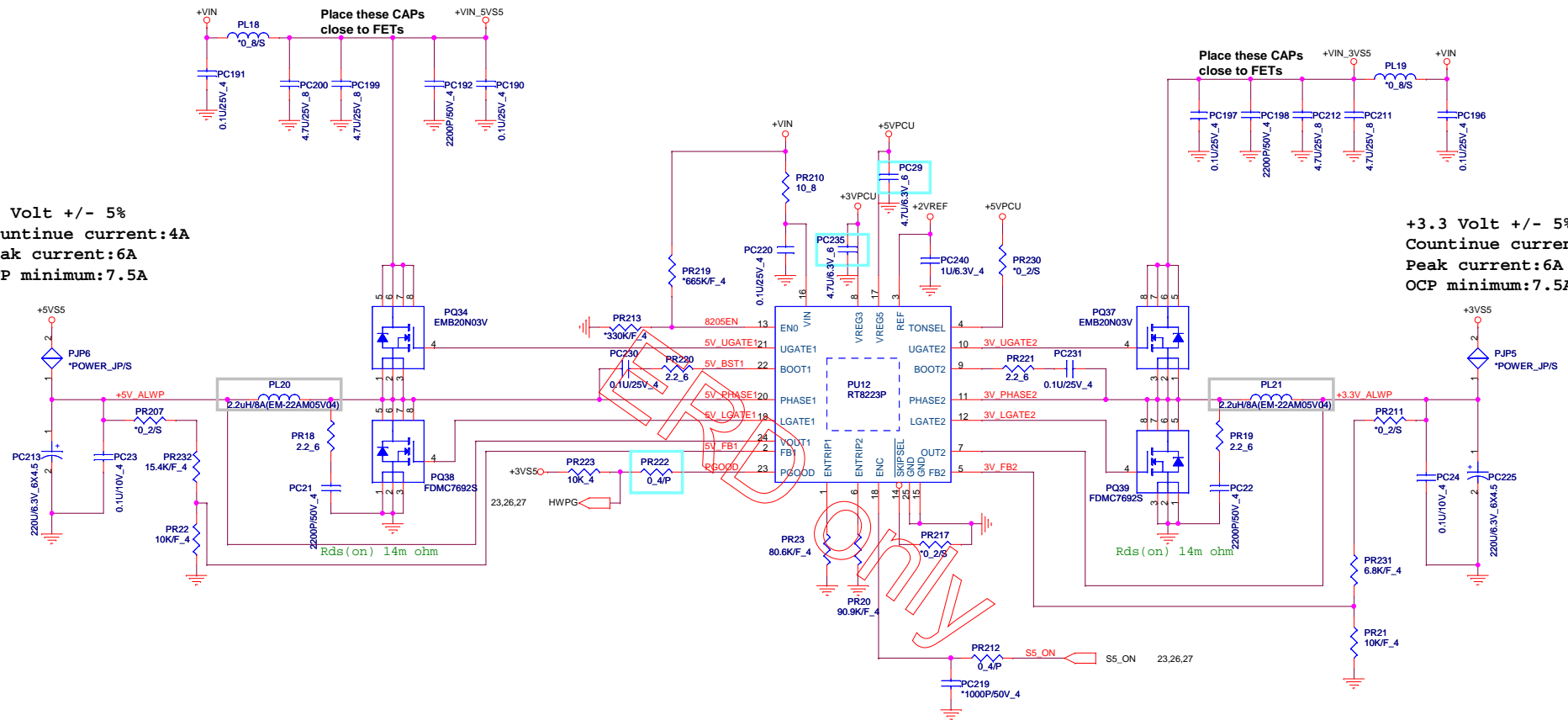
	PROJECT :U93 Quanta Computer Inc.		
	Size Custom	Document Number EC (IT8528E)/ROM	Rev 1A
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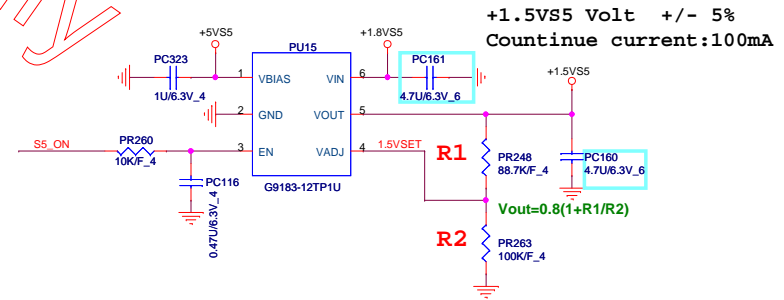
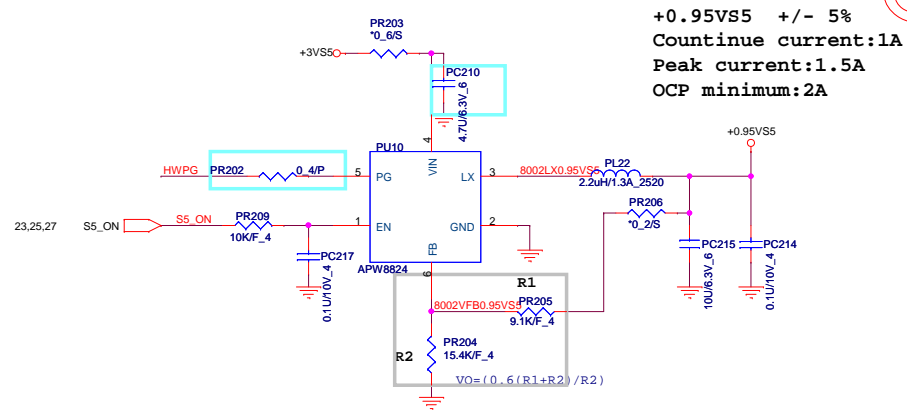
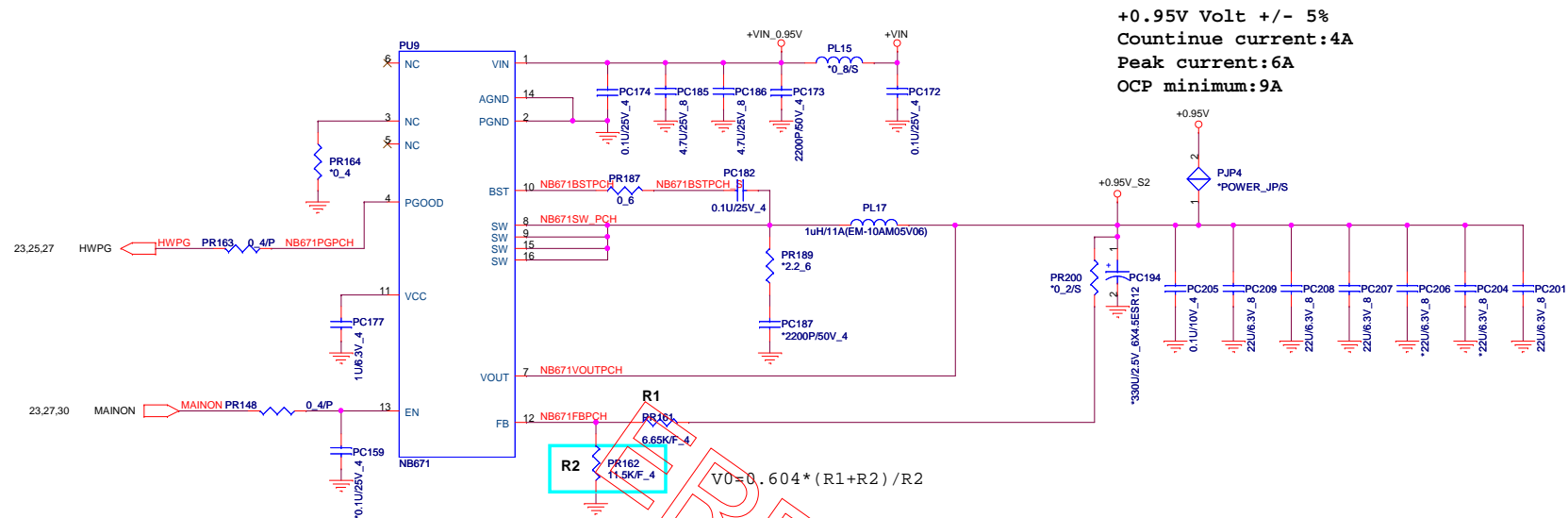
ADD VGA TEMP_FAIL function is active Hi

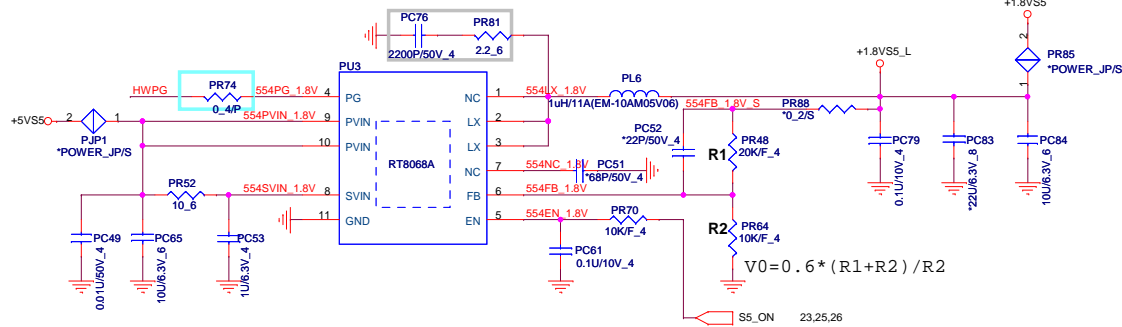
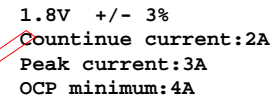


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

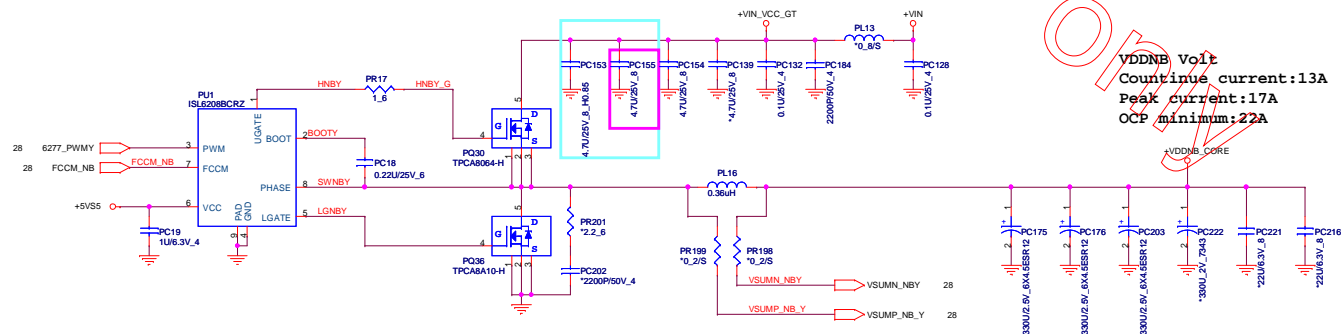
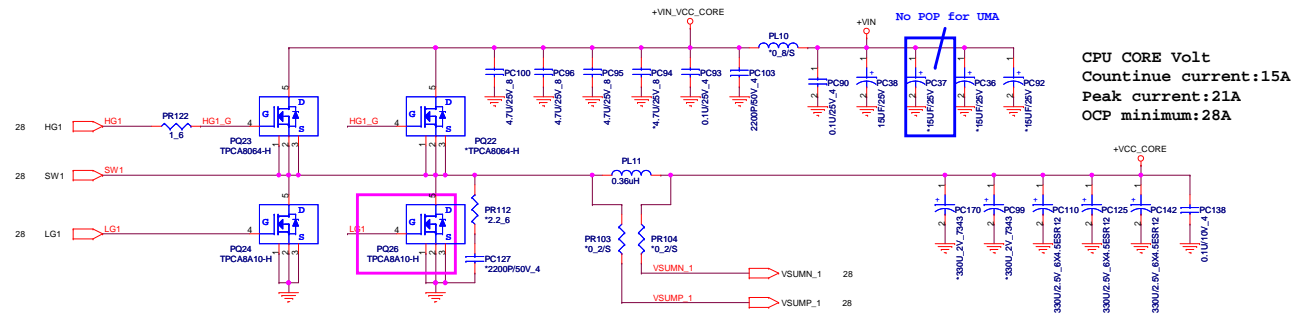






Size Custom	Document Number DDR3 (TP551216)	Rev 1A
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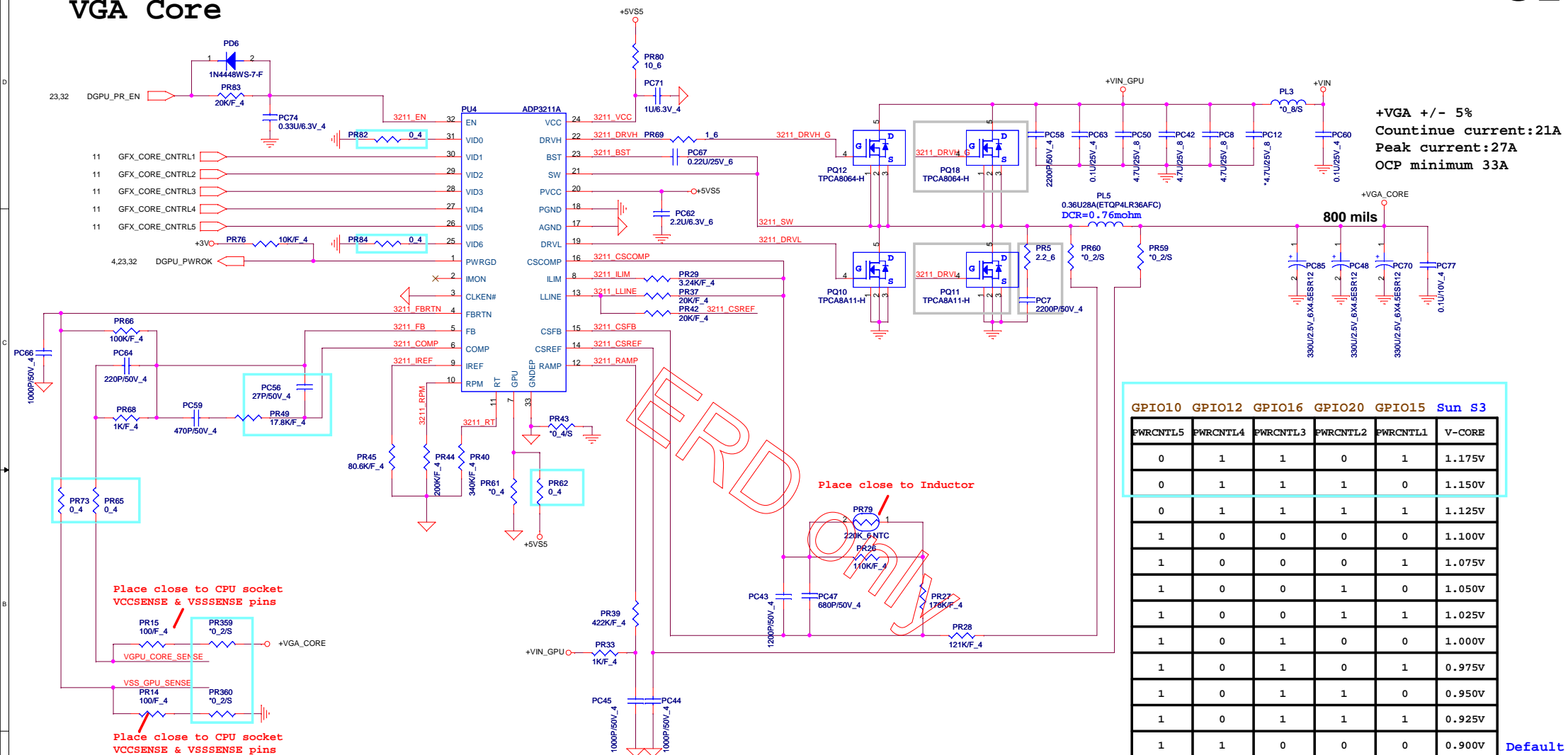




PROJECT :U76
Quanta Computer Inc.

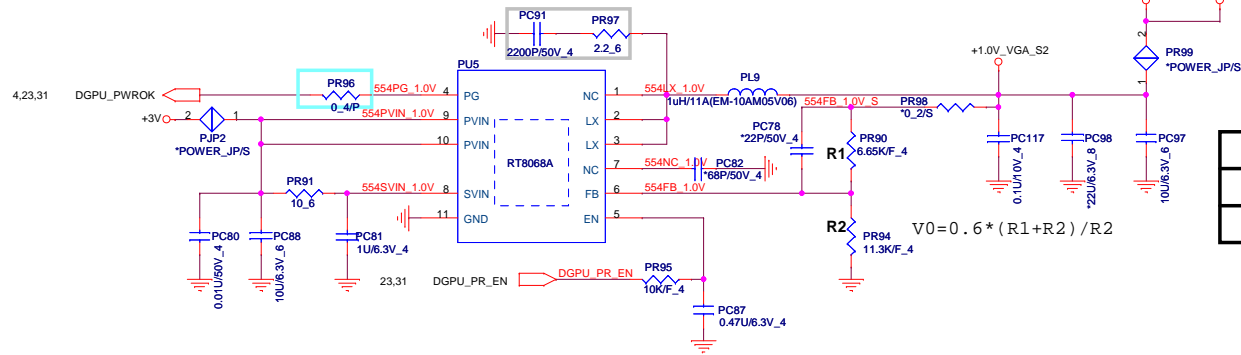
Site Custom	Document Number ISL6208	Rev 1A
Date: Wednesday, April 03, 2013 Sheet 29 of 32		

VGA Core

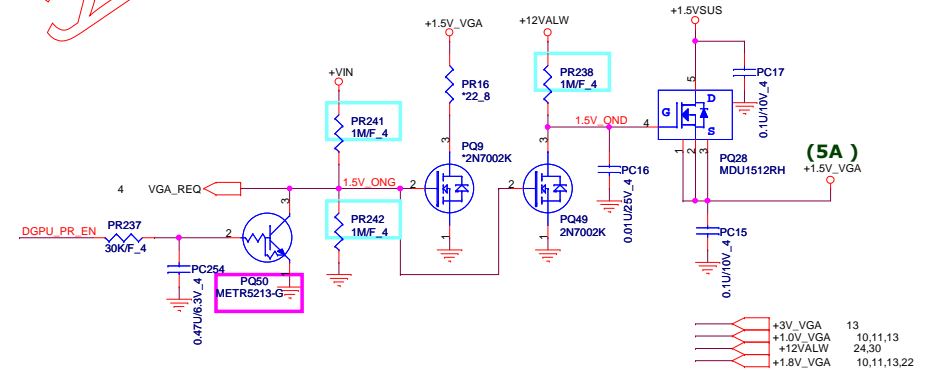
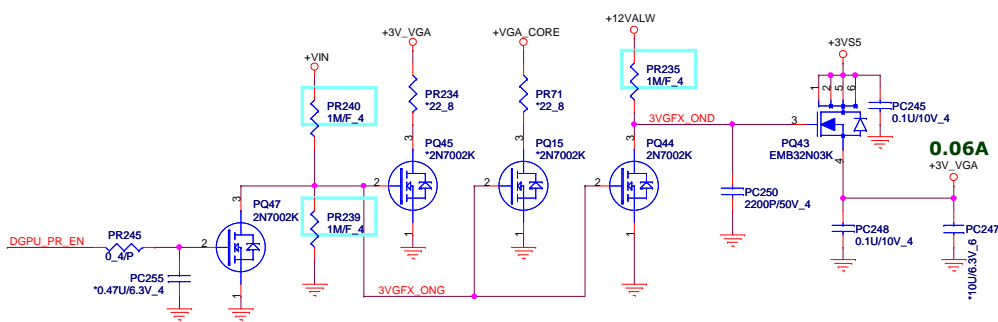
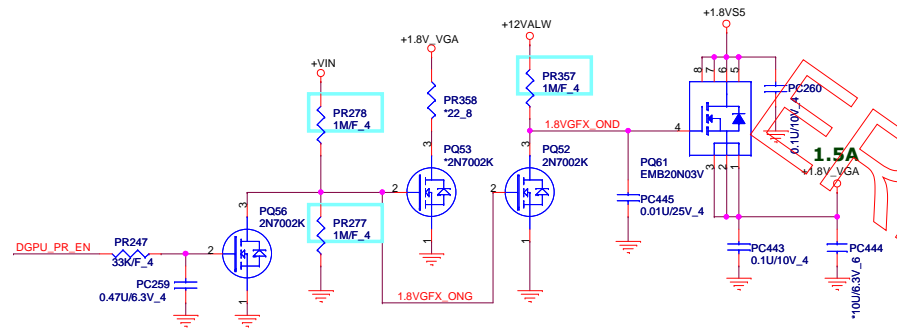


Default

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V



+3V_VGA 13
 +1.0V_VGA 10,11,13
 +12V_VALW 24,30
 +1.8V_VGA 10,11,13,22



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