1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000734528	PRODUCTION RELEASED	2009-06-04

K24 MLB SCHEMATIC

6/12/2009

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K24

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

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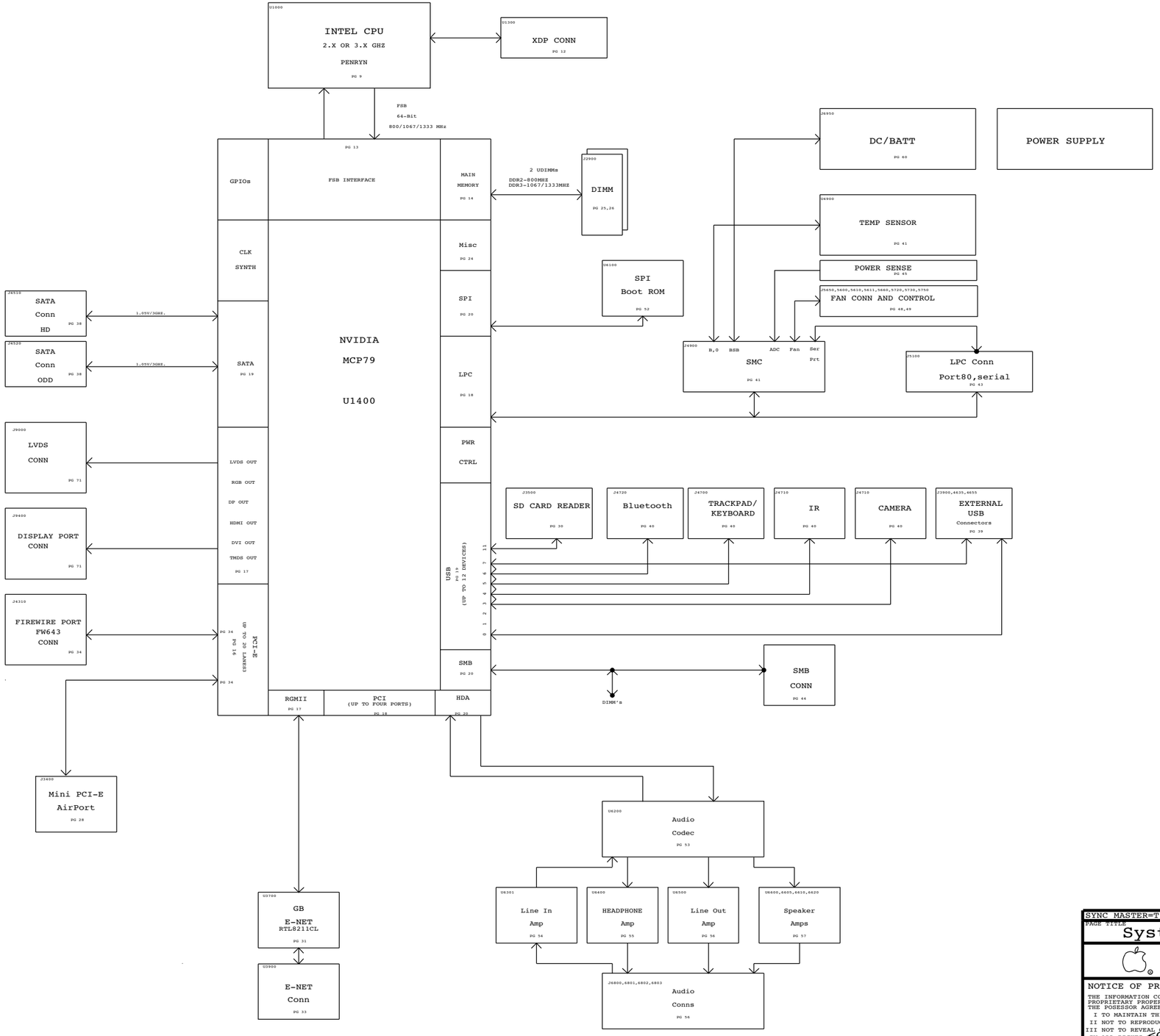

SYNC MASTER=T18 MLB SYNC DATE=12/12/2007

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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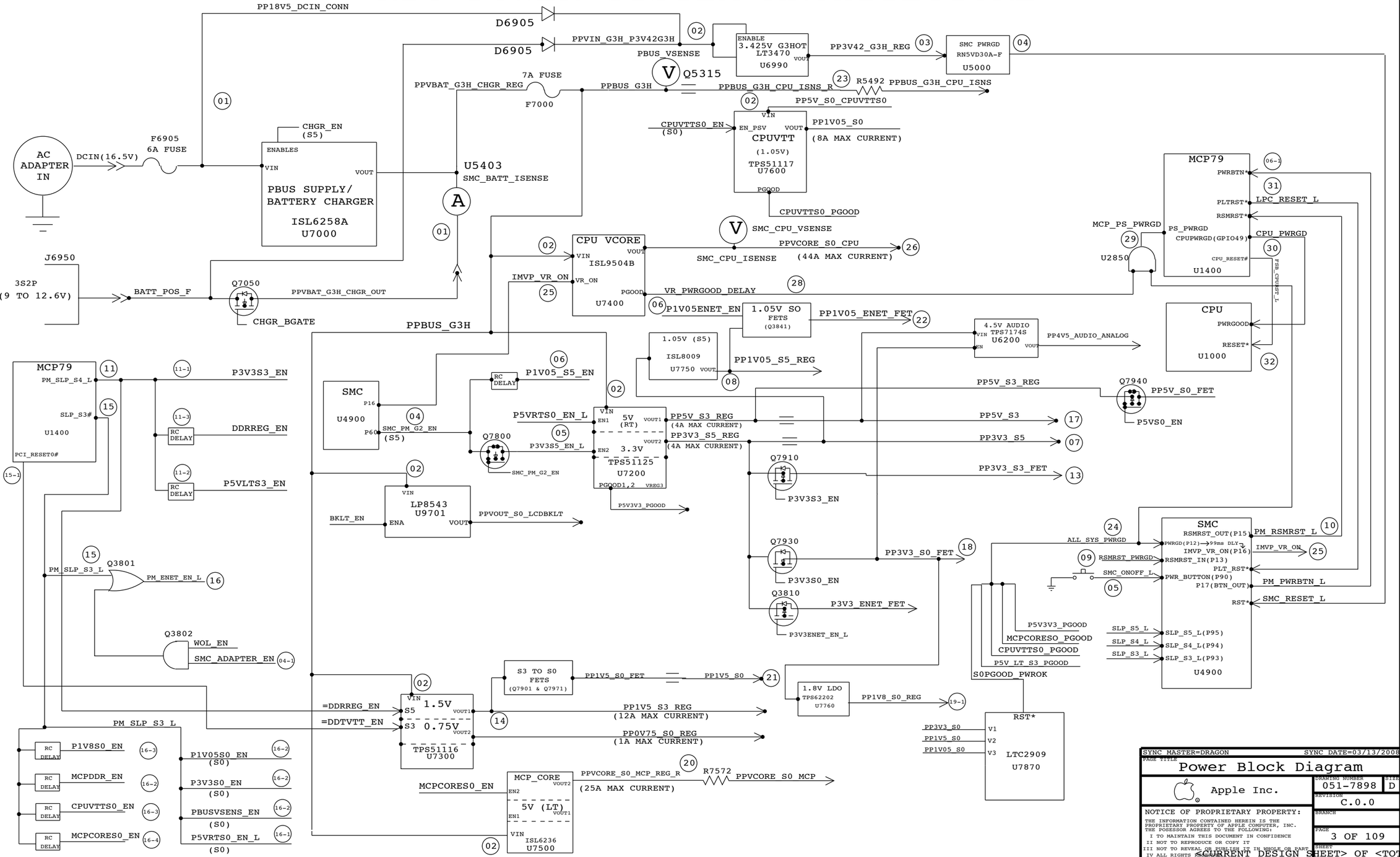
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

K24 POWER SYSTEM ARCHITECTURE



SYNC MASTER=DRAGON SYNC DATE=03/13/2008

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SLGBE,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGRM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERSIL AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K24 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC MASTER=M97 MLB

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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Revision History

SYNC MASTER=M97 MLB

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SHEET

Functional Test Points

Fan Connectors

F42	TRUE	PP5V_S0	(NEED 3 TP) 6D3 7D5
F43	TRUE	FAN_RT_PWM	47B4
F44	TRUE	FAN_RT_TACH	47C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

F2HD	TRUE	BI_MIC_LO	56C2 57B1
F2HE	TRUE	BI_MIC_HI	56C2 57B1
F2HF	TRUE	BI_MIC_SHIELD	56C2 57B1

SPEAKER FUNC_TEST

F42	TRUE	SPKRAMP_L_N_OUT	55A2 56B2
F42	TRUE	SPKRAMP_L_P_OUT	55B2 56B2
F42	TRUE	SPKRAMP_R_N_OUT	55C2 56A2
F42	TRUE	SPKRAMP_R_P_OUT	55C2 56B2
F43	TRUE	SPKRAMP_SUB_N_OUT	55B2 56B2
F42	TRUE	SPKRAMP_SUB_P_OUT	55C2 56B2

THERMAL FUNC_TEST

F43	TRUE	MCPTHMSNS_D2_P	46B5 80D3
F43	TRUE	MCPTHMSNS_D2_N	46B5 80D3

LVDS FUNC_TEST

F4D0	TRUE	PP3V3_LCDVDD_SW_F	6C3 68C2
F4D0	TRUE	PP3V3_S0_LCD_F	68C3
F4D0	TRUE	PPVOUT_S0_LCDBKLT	6C3 68B2 71C1
F4D0	TRUE	LVDS_IG_DDC_CLK	17B3 69C5
F4D0	TRUE	LVDS_IG_DDC_DATA	17A3 69C5
F4D0	TRUE	LVDS_IG_A_DATA_N<0>	17B3 68C2 75B3
F4D0	TRUE	LVDS_IG_A_DATA_P<0>	17B3 68C2 75B3
F4D0	TRUE	LVDS_IG_A_DATA_N<1>	17B3 68C2 75B3
F4D0	TRUE	LVDS_IG_A_DATA_P<1>	17B3 68C2 75B3
F4D0	TRUE	LVDS_IG_A_DATA_N<2>	17B3 68C2 75B3
F4D0	TRUE	LVDS_IG_A_DATA_P<2>	17B3 68C2 75B3
F4D0	TRUE	LVDS_IG_A_CLK_F_N	68C2 75B3
F4D0	TRUE	LVDS_IG_A_CLK_F_P	68C2 75B3
F4D0	TRUE	LED_RETURN_1	68B3 71B1
F4D0	TRUE	LED_RETURN_2	68B3 71B1
F4D0	TRUE	LED_RETURN_3	68B3 71B1
F4D0	TRUE	LED_RETURN_4	68B3 71B1
F4D0	TRUE	LED_RETURN_5	68B3 71B1
F4D0	TRUE	LED_RETURN_6	68B3 71A1
F4D0	TRUE	TP_BKL_SYNC	68C2

(NEED TO ADD 5 GND TP)

SATA ODD CONN

F2G0	TRUE	PP5V_SW_ODD	(NEED 4 TP) 6C3 37D3
F2G0	TRUE	SMC_ODD_DETECT	37C7 40B8
F2G0	TRUE	SATA_ODD_D2R_C_P	37C6 75A3
F2G0	TRUE	SATA_ODD_D2R_C_N	37C6 75A3
F2G0	TRUE	SATA_ODD_R2D_P	37C6 75A3
F2G0	TRUE	SATA_ODD_R2D_N	6A7 37C6 75A3

(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

F31	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP) 6C3 37B6
F31	TRUE	SATA_HDD_R2D_P	37A5 75A3
F31	TRUE	SATA_HDD_R2D_N	37A5 75A3
F31	TRUE	SATA_HDD_D2R_C_P	37B5 75A3
F31	TRUE	SATA_HDD_D2R_C_N	37B5 75A3
F30	TRUE	SYS_LED_ANODE_R	37A7
F30	TRUE	IR_RX_OUT	37A7 39D4
F31	TRUE	PP5V_S3_IR_R	37A7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

F2G0	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
F2G1	TRUE	SMBUS_SMC_BSA_SDA	43C5 79D3
F2G0	TRUE	SYS_DETECT_L	58A8
F2G0	TRUE	BATT_POS_F	(NEED 3 TP) 58A7 58B8 59A3

(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

F2G4	TRUE	PP3V42_G3H	(NEED 3 TP) 6B5 6D3 7D1
F2G4	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
F2G4	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
F2G5	TRUE	SMC_BTL_BUTTON_L	40C5 58C4
F2G0	TRUE	SMC_LID_R	58C2

(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

F30	TRUE	PP5V_S3_BTCAMERA_F	29C7
F301	TRUE	PCIE_MINI_D2R_P	14B6 29C7 75D3
F302	TRUE	PCIE_MINI_D2R_N	14B6 29C7 75D3
F303	TRUE	PCIE_MINI_R2D_P	29C7 75D3
F304	TRUE	PCIE_MINI_R2D_N	29C7 75D3
F2Q2	TRUE	PCIE_CLK100M_MINI_CONN_P	29C7 75D3
F2Q2	TRUE	PCIE_CLK100M_MINI_CONN_N	29C7 75D3
F2Q2	TRUE	USB_CAMERA_CONN_P	29B7 76C3
F2Q2	TRUE	USB_CAMERA_CONN_N	29B7 76C3
F2Q2	TRUE	PP5V_WLAN	(NEED 2 TP) 6C3 29C5
F2B8	TRUE	PCIE_WAKE_L	14B6 29C7
F292	TRUE	SMBUS_SMC_A_S3_SCL	6C5 43D2 79D3
F296	TRUE	SMBUS_SMC_A_S3_SDA	6C5 43D2 79D3
F293	TRUE	CONN_USB2_BT_P	29B7 76C3
F295	TRUE	CONN_USB2_BT_N	29B7 76B3
F297	TRUE	MINI_CLKREQ_O_L	29C7
F2B9	TRUE	MINI_RESET_CONN_L	29A7

(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

F370	TRUE	PP3V3_S3_LDO	6C3 49B4 49C3
F371	TRUE	PP18V5_S3	6C3 49C1 49D3
F372	TRUE	Z2_CS_L	48C8 49C3
F373	TRUE	Z2_DEBUG3	48C8 49C3
F374	TRUE	Z2_MOSI	48C8 49C3
F375	TRUE	Z2_MISO	48C8 49C3
F376	TRUE	Z2_SCLK	48C8 49C3
F377	TRUE	Z2_BOOST_EN	49C3 49C5
F378	TRUE	Z2_HOST_INTN	48D8 49C3
F379	TRUE	Z2_CLKIN	48C6 49C3
F380	TRUE	Z2_KEY_ACT_L	48C8 49C1
F381	TRUE	Z2_RESET	48C8 49C1
F382	TRUE	PSOC_MISO	48C8 49C1
F383	TRUE	PSOC_MOSI	48C8 49C1
F384	TRUE	PSOC_SCLK	48C8 49C1
F385	TRUE	SMBUS_SMC_A_S3_SDA	6D5 43D2 79D3
F386	TRUE	SMBUS_SMC_A_S3_SCL	6D5 43D2 79D3
F387	TRUE	PSOC_F_CS_L	48C8 49C1
F388	TRUE	PICKB_L	48D8 49C1

KEYBOARD CONN

F354	TRUE	PP3V3_S3	6D3 7D3
F355	TRUE	PP3V42_G3H	6A7 6D3 7D1
F324	TRUE	WS_KBD1	48C6 48D2
F325	TRUE	WS_KBD2	48C6 48D2
F326	TRUE	WS_KBD3	48C6 48D2
F327	TRUE	WS_KBD4	48C6 48D2
F328	TRUE	WS_KBD5	48C6 48D2
F329	TRUE	WS_KBD6	48C6 48D2
F32A	TRUE	WS_KBD7	48C6 48D2
F32B	TRUE	WS_KBD8	48C6 48D2
F32C	TRUE	WS_KBD9	48C6 48D2
F32D	TRUE	WS_KBD10	48C6 48D2
F32E	TRUE	WS_KBD11	48C6 48D2
F32F	TRUE	WS_KBD12	48C6 48D2
F330	TRUE	WS_KBD13	48C6 48D2
F331	TRUE	WS_KBD14	48C2 48C6
F332	TRUE	WS_KBD15_CAP	48C2
F333	TRUE	WS_KBD16_NUM	48C2
F334	TRUE	WS_KBD17	48C2 48D6
F335	TRUE	WS_KBD18	48C2 48D7
F336	TRUE	WS_KBD19	48C2 48D7
F337	TRUE	WS_KBD20	48C2 48D7
F338	TRUE	WS_KBD21	48C2 48D7
F339	TRUE	WS_KBD22	48C2 48D7
F33A	TRUE	WS_KBD23	48C2 48D7
F33B	TRUE	WS_KBD_ONOFF_L	48C2
F33C	TRUE	WS_LEFT_SHIFT_KBD	48B3 48B5 48C2
F33D	TRUE	WS_LEFT_OPTION_KBD	48B3 48B5 48C2
F33E	TRUE	WS_CONTROL_KBD	48B3 48B5 48C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

F35C	TRUE	KBDLED_ANODE	(NEED 2 TP) 49A4
F3F2	TRUE	SMC_KDBLED_PRESENT_L	49A4 49A6

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

F2F7	TRUE	PPVCORE_S0_CPU	7D7
F2F8	TRUE	PPVCORE_S0_MCP	7C7
F2F9	TRUE	PP0V75_S0	7C7
F2FA	TRUE	PP1V05_S0	7D7
F2FB	TRUE	PP1V5_S0	7C6
F2FC	TRUE	PP1V8_S0	7B6
F2FD	TRUE	PP5V_S0	6D7 7D5
F2FE	TRUE	PP3V3_S0	7D5
F2FF	TRUE	PP1V5_S3	7D3
F2G0	TRUE	PP3V3_S3	6B5 7D3
F2G1	TRUE	PP5V_S3	7C3
F2G2	TRUE	PP1V1R1V05_S5	7B3
F2G3	TRUE	PP3V3_S5	7B3
F2G4	TRUE	PP3V42_G3H	6A7 6B5 7D1
F2G5	TRUE	PPBUS_G3H	7C1
F2G6	TRUE	PP3V3_ENET_PHY	7B5
F2G7	TRUE	PP1V2R1V05_ENET	7B5
F2G8	TRUE	PP3V3_G3_RTC	20C8 21A5 24D4
F2G9	TRUE	PP5V_WLAN	6D5 29C5
F2GA	TRUE	PP5V_SW_ODD	6B7 37D3
F2GB	TRUE	PP5V_S0_HDD_FLT	6B7 37B6
F2GC	TRUE	PP3V3_S5_AVREF_SMC	40D4 41C6
F2GD	TRUE	PP18V5_S3	6C5 49C1 49D3
F2GE	TRUE	PP3V3_S3_LDO	6C5 49B4 49C3
F2GF	TRUE	PP3V3_LCDVDD_SW_F	6C7 68C2
F2H0	TRUE	PPVOUT_S0_LCDBKLT	6C7 68B2 71C1
F2H1	TRUE	PP4V5_AUDIO_ANALOG	52A5 52D2 52D7
F2H2	TRUE	SMC_PM_G2_EN	40D5 60C5 66D8
F2H3	TRUE	PM_SLP_S4_L	20C3 40C5 41A2 66C8
F2H4	TRUE	PM_SLP_S3_L	20C3 32B7 35A5 40C5 66D5 70D8

(NEED TO ADD 4 GND TP)

DC POWER CONN

F2H5	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 58D6
F2H6	TRUE	ADAPTER_SENSE	58D7

(NEED TO ADD 4 GND TP)

SYNC MASTER=M97 MLB

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-7898 | SIZE: D

REVISION: C.0.0

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

"S0,S0M" RAILS

62D1 =PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
PPVCORE_S0_CPU 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 10B5 10D6 11D6
=PPVCORE_S0_CPU_VSENSE 44D8

64C2 =PPCPUVTT_S0_REG
PP1V05_S0 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 9D5 10C6 11B6 12D6
=PP1V05_S0_MCP_FSB 13A2 13B7 21D3 22C8
=PP1V05_S0_SMC_LS
=PP1V05_S0_MCP_PEX_DVDD 7A8 22D8
=PP1V05_S0_MCP_AVDD_UF 22D4
=PP1V05_S0_MCP_SATA_DVDD 7A8 22D6
=PP1V05_S0_MCP_HDMI_VDD 17A6 23D7
=PP1V05_S0_VMON 46A8
=PP1V05_S0_MCP_PLL_UF_R 65B3
=PP1V05_FW_P1V05FWFET 35C6
=PP1V05_FWPWRCTL 35B4

63C7 63C1 63B8 =PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 21D5 22D8
=PPVCORE_S0_MCP_VSENSE 44D8

61C9 =PP0V75_S0_REG
PP0V75_S0 6D3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP 67B3
=PP0V75_S0_MEM_VTT_A 26A4
=PP0V75_S0_MEM_VTT_B 27A4

67D1 =PP1V5_S0_FET
PP1V5_S0 6D3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 10B6 11B6
=PP1V5_S0_VMON 46A8
=PP1V8R1V5_S0_MCP_MEM 15C3 15C7 22C8
=PP1V5_S0_MEM_MCP 27B3
=PP1V5_S0_MCP_PLL_VLDO 65B6

65C5 =PP1V8_S0_REG
PP1V8_S0 6D3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD 17B6 23D7
=PP1V8_S0_AUDIO 52D7

65B1 22C4 =PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

67B4 =PP5V_S0_FET
PP5V_S0 6D3 6D7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_HDD 37B3
=PP5V_S0_LPCPLUS 42D5
=PP5V_S0_FAN_RT 47C5
=PP5V_S0_CPU_IMVP 42D8
=PP5V_S0_KBDLED 49A5
=PP5V_S0_DP_AUX_MUX 49B6
=PP5V_S0_CPUVTTS0 64C8
=PP5V_S0_BKL 71D4
=PP5V_S0_MCPREG 63D4
=PP5V_S0_VMON 64B5

67C4 =PP3V3_S0_FET
PP3V3_S0 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP 12D6
=PP3V3_S0_MCP 20C2 21B3 22B8
=PP3V3_S0_MCP_DAC_UF 23D4
=PP3V3_S0_MCP_VPLL_UF 23C7
=PP3V3_S0_ODD 37C7 37D6
=PP3V3_S0_SMBUS_SMC_0_S0 43D5
=PP3V3_S0_SMBUS_SMC_B_S0 43C3
=PP3V3_S0_SMBUS_MCP_0 43D8
=PP3V3_S0_FAN_RT 47C5
=PP3V3_S0_AUDIO 52A8 52D2 56D8 57B8 57D3
=PP3V3_S0_IMVP 62D8
=PP3V3_S0_LCD 68C5
=PP3V3_S0_MCP_GPIO 17C1 18D1 20A4
=PP3V3_S0_MCP_PLL_UF 22B6
=PP3V3R1V5_S0_MCP_HDA 20D3 20D8 22A8
=PP3V3_S0_SMC 41A1 41D3
=PP3V3_S0_MCPTHMSNS 46B6
=PP3V3_S0_CPUTHMSNS 46D6
=PP3V3_S0_DPCONN 70B8 70C8
=PPSPD_S0_MEM_A 26A8
=PPSPD_S0_MEM_B 27A8
=PP3V3_S0_PWRCTL 46A5
=PP3V3_S0_VMON 46A8
=PP3V3_S0_CPUVTTISNS 45C7
=PP3V3_S0_TPAD 49A6
=PP3V3_S0_SMBUS_MCP_1 43C8
=PP3V3_S0_P1V8S0 65D8
=PP3V3_S0_BKL_VDDIO 71C7
=PP3V3_S0_MCPDDRISNS 45D8
=PP3V3_S0_MCP_PLL_VLDO 65C6
=PP3V3_S0_P3V3FWFET 35D6
=PP3V3_S0_FWPWRCTL 35B1 35D2

"S3" RAILS

61C1 =PP1V5_S3_REG
PP1V5_S3 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_P1V5S0FET 67D3
=PP1V5_S3_MEM_A 26D7
=PP1V5_S3_MEM_B 27D7
=PP1V5_S3_MEMRESET 28C6
=PP1V5_S3_HDD 37B8

67D6 =PP3V3_S3_FET
PP3V3_S3 6B5 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 43D3
=PP3V3_S3_PDCISENS 61B3
=PP3V3_S3_SMBUS_SMC_MGMT 43B5
=PP3V3_S3_VREFMRGN 25D8
=PP3V3_S3_WLAN 29A6
=PP3V3_S3_MCP_GPIO 20A3
=PP3V3_S3_TPAD 48A6 48B5 48C5 48D2
=PP3V3_S3_SMS 50B7
=PP3V3_S3_CARDREADER 30D7

60B8 =PP5V_S3_REG
PP5V_S3 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB 38C7
=PP5V_S3_IR 37A8 39D7
=PP5V_S3_BTCAMERA 29C3
=PP5V_S3_VTTCLAMP 67A3
=PP5V_S3_MCPDDRFET 67D4
=PP5V_S3_SYSLED 41B8
=PP5V_S3_TPAD 49B6 49D7
=PP5V_S3_WLAN 29C1
=PP5V_S3_1V5S30V75S0 61C5
=PP5V_S3_AUDIO 52A8 52D2 54D5 56B6
=PP5V_S3_AUDIO_AMP 55B7 55C7 55D7
=PP5V_S3_P5VS0FET 67B8
=PP5V_S3_ODD 37D5

61D8 25D5 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

"G3H" RAILS

58B4 =PP3V42_G3H_REG
PP3V42_G3H 6A7 6B5 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF 41C8
=PP3V42_G3H_SMBUS_SMC_BSA 43C5
=PP3V42_G3H_PWRCTL 66B3 66C8 66D8
=PP3V42_G3H_CHGR 59A8 59C6 59D5
=PP3V42_G3H_SMCUSBMUX 38B8
=PP3V42_G3H_TPAD 48B5 48C2 48C3 48C5
=PP3V42_G3H_BATT 58C2 58C4
=PP3V3_S5_SMC 40D4 41C1 41C3 41C7 41D8
=PP3V3_S5_LPCPLUS 42C7 42C8 42D5
=PP3V42_G3H_RTC_D 24D8
=PP3V42_G3H_BMON_ISNS 45B8
=PP3V42_G3H_ONEWIRE 58D2
=PP3V42_G3H_AUDIO 56B6

58D1 58C8 =PP18V5_DCIN_CONN
PP18V5_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PP18V5_G3H_CHGR 59D8

59C1 =PPBUS_G3H
PPBUS_G3H 6C3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT 72D8
=PPVIN_S0_MCPCORE 63D5
=PPVIN_S5_1V5S30V75S0 61C2
=PPVIN_S5_3V3S5 60C3
=PPVIN_S3_5VS3 60C6 60C7
=PPBUS_G3HRS5 44B8
=PPBUS_S5_FWPWRSW 35B7
=PPCPUVCORE_VTT_ISNS_R 45B8
(BEFORE HIGH SIDE SENSING RES.)

45B7 =PPCPUVCORE_VTT_ISNS
(AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
PPBUS_G3H_CPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 64C6
=PPVIN_S5_CPU_IMVP 62C3 62D4 62D8

"ENET" RAILS

32D2 =PP3V3_ENET_FET
PP3V3_ENET_PHY 6C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 17D3 17D7 22A5 22B6
=PP3V3_ENET_PHY 31D7

32B2 =PP1V05_ENET_FET
PP1V2R1V05_ENET 6C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC 22A8
=PP1V05_ENET_MCP_RMGT 17D3 22D6
=PP1V05_ENET_PHY 31D2

"S5" RAILS

65A5 =PP1V05_S5_REG
PP1V1R1V05_S5 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC 21A3 22D8
=PP1V05_ENET_P1V05ENETFET 32C4

60B1 =PP3V3_S5_REG
PP3V3_S5 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO 17C7 19C1
=PP3V3_S5_ROM 42B5 42C7 51C6
=PP3V3_S5_LCD 68C8
=PP3V3_S5_MCP 21B3 22B8
=PP3V3_S5_MCPPWRGD 24B8
=PP3V3_S5_PWRCTL 46B3
=PP3V3_S5_P1V05ENETFET 32C5
=PP3V3_S5_P3V3S3FET 67D8
=PP3V3_S5_P3V3S0FET 67C8
=PP3V3_S5_P1V05S5 65B8
=PP3V3_S5_MEMRESET 28C4
=PP3V3_S5_P3V3ENETFET 32D5
=PP3V3_S5_DP_PORT_PWR 70D8
=PP3V3_FW_LATEVG 36A7
=PP3V3_FW_LATEVG_ACTIVE 35A8
=PP3V3_S5_P1V05FWFET 35C7

"FIREWIRE" RAILS

35D4 =PP3V3_FW_FET
PP3V3_FW
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_FW_FWPHY 34D5 34B6 34D8 34D3
=PP3V3_S0_P1V05FWFET 35C7

35B1 =PPBUS_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVP_FW_PORT1 34C3
=PPVP_FW_PHY_CPS_FET 34C6

35C5 =PP1V0_FW_FET
PP1V05_FW
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V0_FW_FWPHY 34D6 35D3

PEX & SATA AVDD/DVDD aliases

22D1 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0 16B3
=PP1V05_S0_MCP_PEX_AVDD1 16A3
206 mA (A01)

22D8 7D7 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 16B6
=PP1V05_S0_MCP_PEX_DVDD1 16A6
57 mA (A01)

22D2 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
127 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0 19B6
=PP1V05_S0_MCP_SATA_AVDD1 19B6
127 mA (A01)

22D6 7D7 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0 19B6
=PP1V05_S0_MCP_SATA_DVDD1 19B6
43 mA (A01)

SYNC MASTER=BEN	SYNC DATE=04/21/2008
PAGE TITLE	Power Aliases
Apple Inc.	DRAWING NUMBER 051-7898
	SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 8 OF 109
	SHEET

HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.5OD.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

Z0905
STDOFF-4.5OD.98H-1.1-3.48-TH
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT
Z0906
3R2P5

OMIT
Z0907
3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT
Z0908
3R2P5

OMIT
Z0909
3R2P5

OMIT
Z0910
3R2P5

OMIT
Z0911
3R2P5

OMIT
Z0912
3R2P5

PCI-E ALIASES

UNUSED GPU LANES

16D6 16C6	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D6 16C6	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16C6	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
16C3	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
16C3	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

16B6	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
16B6	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
16C6	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
16C6	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

FIREWIRE PRESENT SIGNALS

35D3 16C6 PCIE_FW_PRSNT_L — R0950 0 5% 1/16W MF-LF 402 — NOSTUFF

USB ALIASES

UNUSED USB PORTS

19C3	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
19C3	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
19D3	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
19D3	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
19C3	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
19C3	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
19D3	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
19D3	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

17C6	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

17B3	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC MCP79 ALIASES

13B6	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE

LAN ALIASES

17D4 =MCP_MII_RXER — MCP_MII_PD (MAKE_BASE=TRUE)
17D4 =MCP_MII_COL
17D4 =MCP_MII_CRS
R0930 47K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

17B4 =DVI_HPD_GMUX_INT — HPLUG_DET2 (MAKE_BASE=TRUE)
R0940 20K 5% 1/16W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

26D5	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
27D5	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32C5	=P3V3ENET_EN	PM_SLP_RMGT_L 29C3	MAKE_BASE=TRUE
32B5	=P1V05ENET_EN		
31C2	=PP3V3_ENET_PHY_VDDREG	TP_PP3V3_ENET_PHY_VDDREG	MAKE_BASE=TRUE
31C2	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31C6	=RTL8211_ENSWREG		MAKE_BASE=TRUE
31B6	TP_RTL8211_CLK125		

R0931 22 5% 1/16W MF-LF 402

FW ALIASES

18B7	FW_PME_L	FW_PLUG_DET_L 35B1 35D7	MAKE_BASE=TRUE
35C8 34B2	=FW_PME_L	FW643_WAKE_L	MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

73C3 9B4 IN CPU_BSEL<0:2> — =MCP_BSEL<0:2> OUT 13A7 (MAKE_BASE=TRUE)

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

EMI IO POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0902 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0903 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0908 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0909 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN,SHORT,EMI,MLB,K19/K24	ZS0900,ZS0901,ZS0902,ZS0903,ZS0908,ZS0909	CRITICAL	

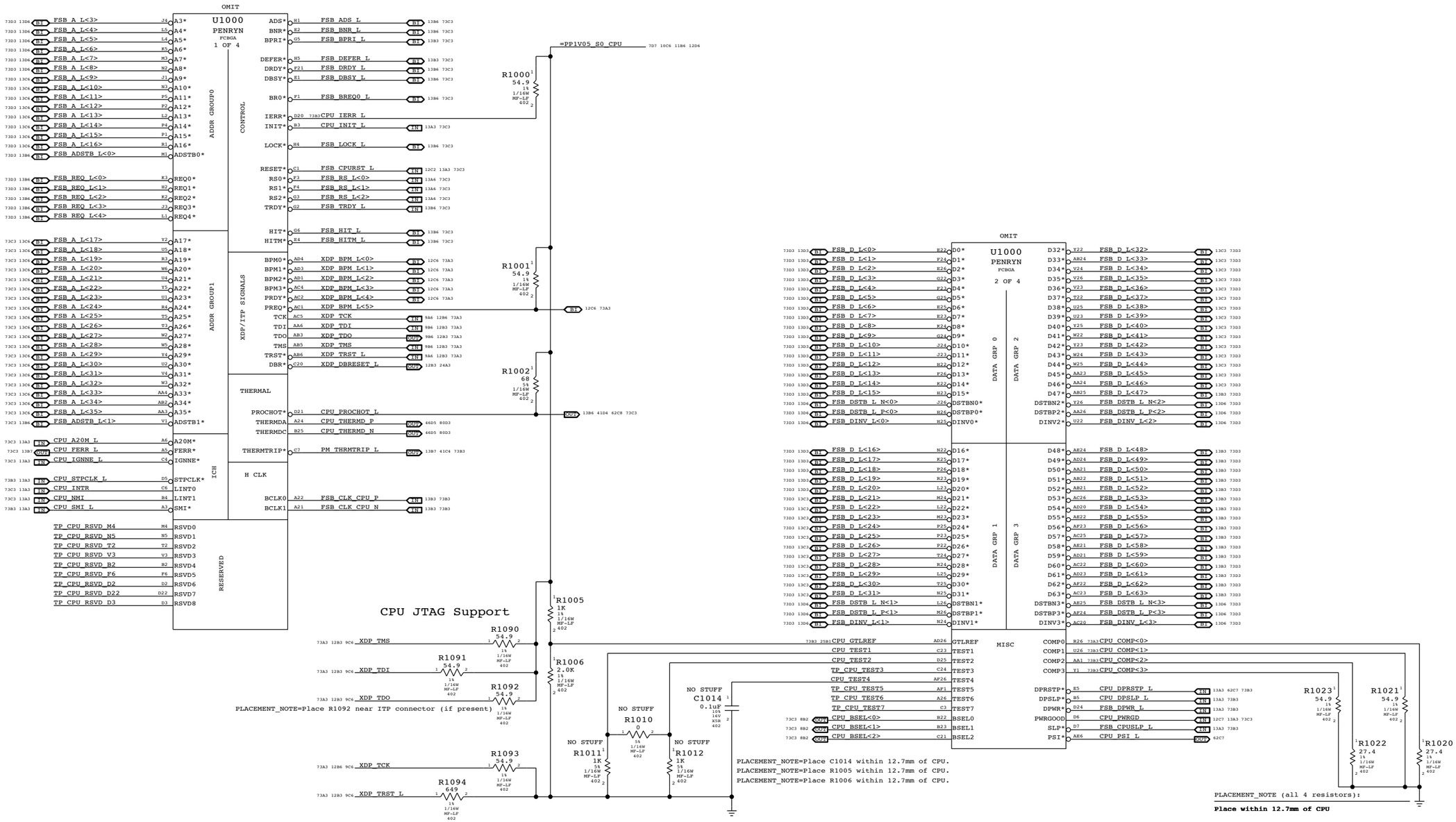
EMI POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

SYNC MASTER=M97 MLB
PAGE TITLE: SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 9 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



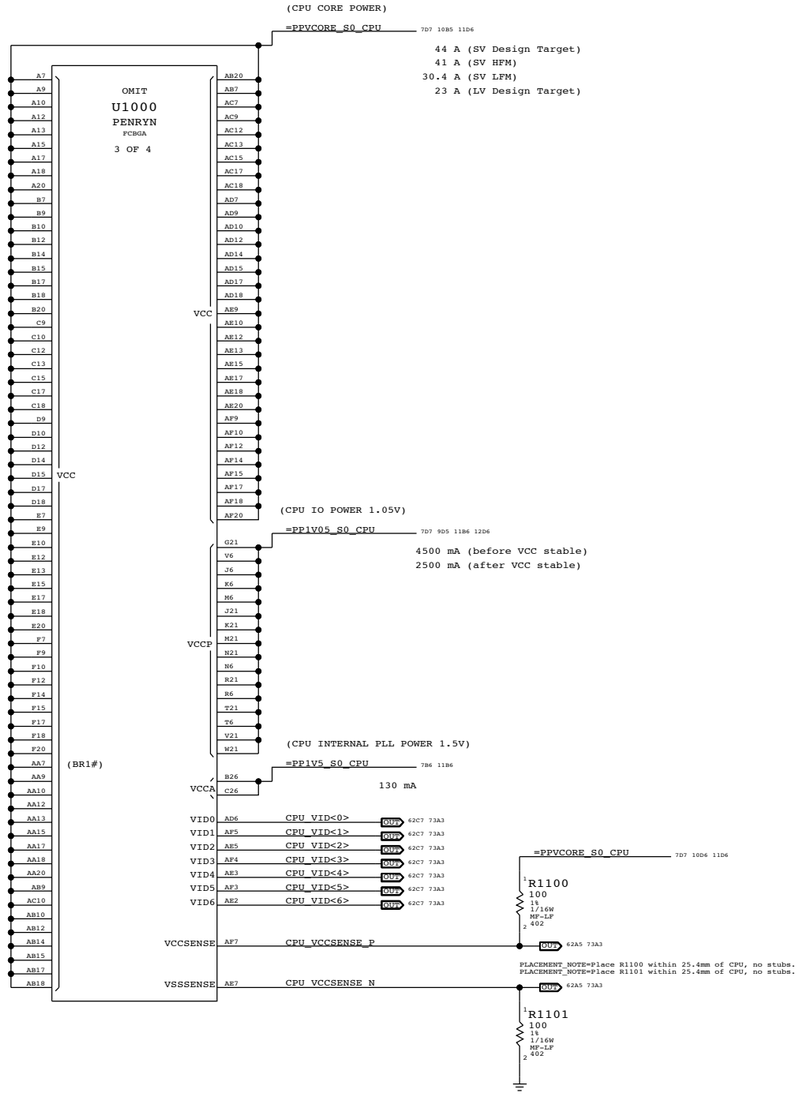
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

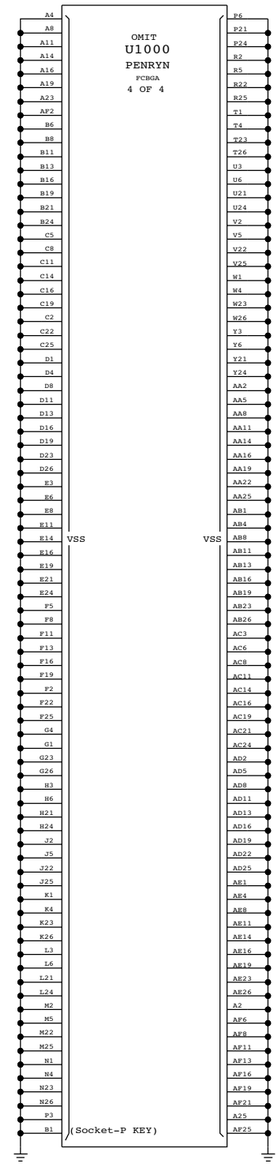
SYNC MASTER=T18 MLB | SYNC DATE=12/12/2007

PAGE TITLE: CPU FSB

Apple Inc.

DRAWING NUMBER: 051-7898 | SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 10 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=T18 MLB	SYNC DATE=12/12/2007
PAGE TITLE: CPU Power & Ground	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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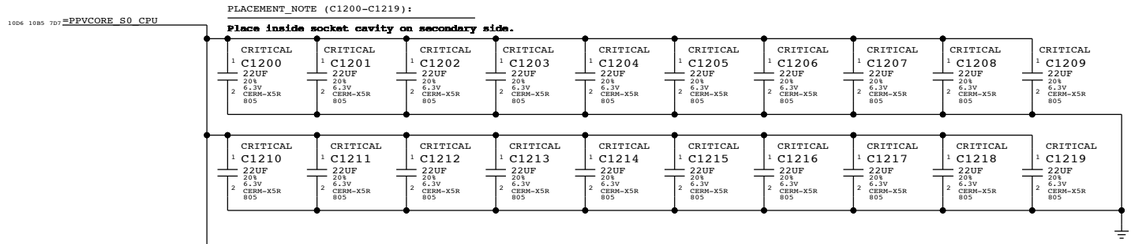
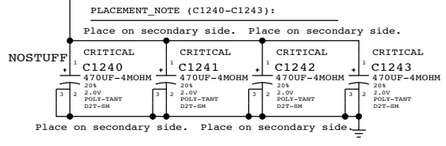
	PAGE: 11 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU VCore HF and Bulk Decoupling

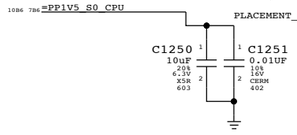
4X 330UF. 20X 22UF 0805





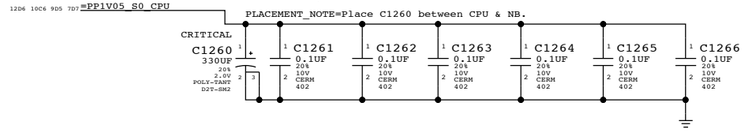
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC MASTER=RAYMOND SYNC DATE=03/31/2008

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 12 OF 109

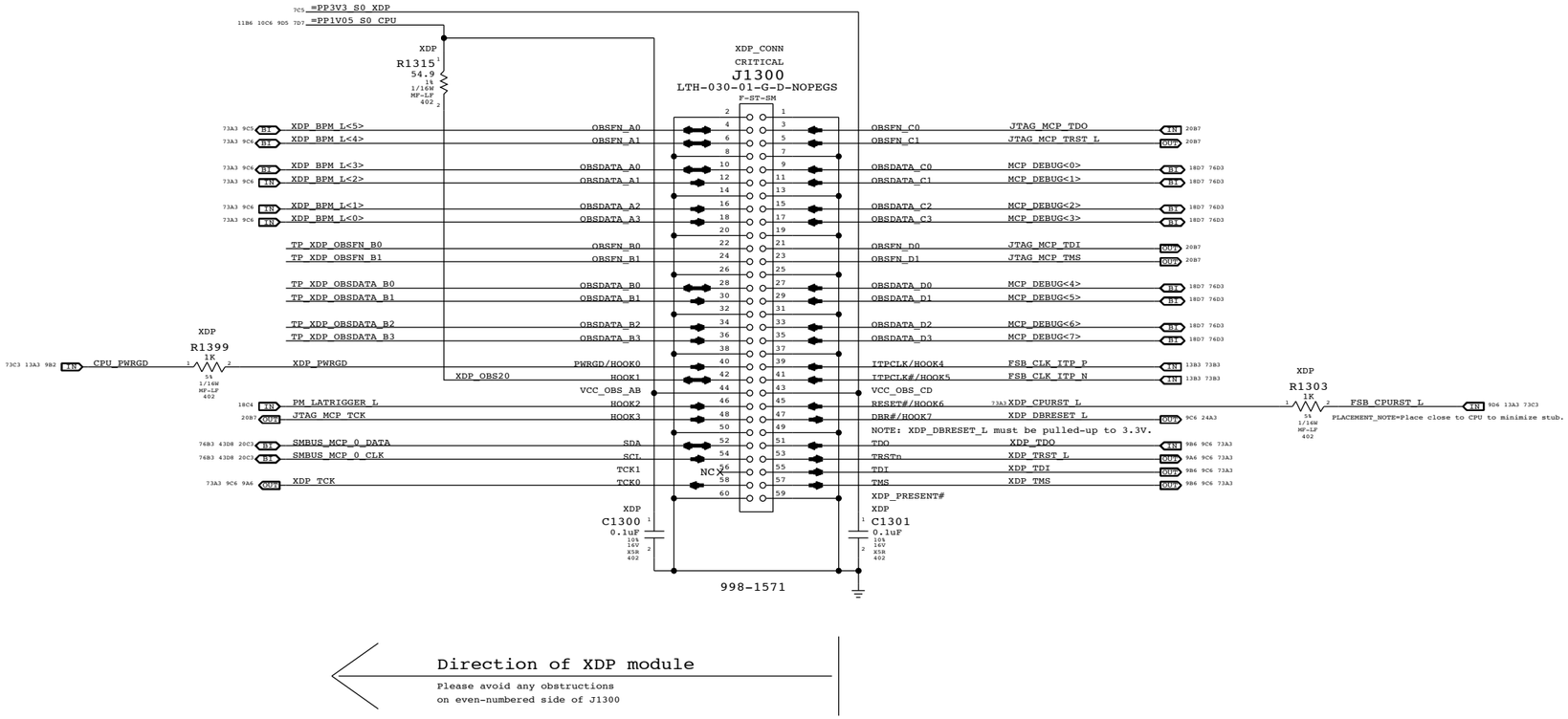
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

SYNC MASTER=K19 MLB	SYNC DATE=11/07/2008
PAGE TITLE: eXtended Debug Port(MiniXDP)	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 13 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

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BGA
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FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	K40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	K41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	K43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
CPU_D61#	J40	FSB_D_L<61>	
CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		

Loop-back clock for delay matching.

CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	B38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

22C8 21D3 13A2 7D7 =PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

73B3 41C4 9C6 PM_THRMTRIP_L
73C3 9C8 CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

8B1 =MCP_BSEL<2>
8B1 =MCP_BSEL<1>
8B1 =MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

22C7 PP1V05_S0_MCP_PLL_FSB
270 mA (A01)

206 mA	AG27	+V_DLL_DLCELL_AVDD
20 mA	AH27	+V_PLL_MCLK
29 mA	AG28	+V_PLL_FSB
15 mA	AH28	+V_PLL_CPU

73B3 MCP_BCLK_VML_COMP_VDD — AM39 BCLK_VML_COMP_VDD
73B3 MCP_BCLK_VML_COMP_GND — AM40 BCLK_VML_COMP_GND
73B3 MCP_CPU_COMP_VCC — AM43 CPU_COMP_VCC
73B3 MCP_CPU_COMP_GND — AM42 CPU_COMP_GND

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

SYNC MASTER=T18_MLB	SYNC DATE=04/04/2008
PAGE TITLE	MCP CPU Interface
Apple Inc.	DRAWING NUMBER 051-7898
	SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 14 OF 109
	SHEET

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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MEMORY PARTITION 0

MEM_A_DQ<63>	AL8	MDQ0_63	MDQS0_7_P	AL10	MEM_A_DQS_P<7>		
MEM_A_DQ<62>	AL9	MDQ0_62	MDQS0_7_N	AL11	MEM_A_DQS_N<7>		
MEM_A_DQ<61>	AP9	MDQ0_61	MDQS0_6_P	AR8	MEM_A_DQS_P<6>		
MEM_A_DQ<60>	AN9	MDQ0_60	MDQS0_6_N	AR9	MEM_A_DQS_N<6>		
MEM_A_DQ<59>	AL6	MDQ0_59	MDQS0_5_P	AM7	MEM_A_DQS_P<5>		
MEM_A_DQ<58>	AL7	MDQ0_58	MDQS0_5_N	AM8	MEM_A_DQS_N<5>		
MEM_A_DQ<57>	AN6	MDQ0_57	MDQS0_4_P	AP13	MEM_A_DQS_P<4>		
MEM_A_DQ<56>	AN7	MDQ0_56	MDQS0_4_N	AR13	MEM_A_DQS_N<4>		
MEM_A_DQ<55>	AR6	MDQ0_55	MDQS0_3_P	AV25	MEM_A_DQS_P<3>		
MEM_A_DQ<54>	AR7	MDQ0_54	MDQS0_3_N	AW25	MEM_A_DQS_N<3>		
MEM_A_DQ<53>	AV6	MDQ0_53	MDQS0_2_P	AU30	MEM_A_DQS_P<2>		
MEM_A_DQ<52>	AW5	MDQ0_52	MDQS0_2_N	AU29	MEM_A_DQS_N<2>		
MEM_A_DQ<51>	AN10	MDQ0_51	MDQS0_1_P	AT35	MEM_A_DQS_P<1>		
MEM_A_DQ<50>	AR5	MDQ0_50	MDQS0_1_N	AU35	MEM_A_DQS_N<1>		
MEM_A_DQ<49>	AU6	MDQ0_49	MDQS0_0_P	AU39	MEM_A_DQS_P<0>		
MEM_A_DQ<48>	AV5	MDQ0_48	MDQS0_0_N	AT39	MEM_A_DQS_N<0>		
MEM_A_DQ<47>	AU7	MDQ0_47					
MEM_A_DQ<46>	AU8	MDQ0_46					
MEM_A_DQ<45>	AW9	MDQ0_45					
MEM_A_DQ<44>	AP11	MDQ0_44					
MEM_A_DQ<43>	AW6	MDQ0_43					
MEM_A_DQ<42>	AY5	MDQ0_42	MRAS0#	AV17	MEM_A_RAS_L		
MEM_A_DQ<41>	AU9	MDQ0_41	MCAS0#	AP17	MEM_A_CAS_L		
MEM_A_DQ<40>	AV9	MDQ0_40	MWE0#	AR17	MEM_A_WE_L		
MEM_A_DQ<39>	AU11	MDQ0_39					
MEM_A_DQ<38>	AV11	MDQ0_38					
MEM_A_DQ<37>	AV13	MDQ0_37					
MEM_A_DQ<36>	AW13	MDQ0_36					
MEM_A_DQ<35>	AR11	MDQ0_35					
MEM_A_DQ<34>	AT11	MDQ0_34	MBA0_2	AP23	MEM_A_BA<2>		
MEM_A_DQ<33>	AR14	MDQ0_33	MBA0_1	AP19	MEM_A_BA<1>		
MEM_A_DQ<32>	AU13	MDQ0_32	MBA0_0	AW17	MEM_A_BA<0>		
MEM_A_DQ<31>	AR26	MDQ0_31					
MEM_A_DQ<30>	AU25	MDQ0_30					
MEM_A_DQ<29>	AT27	MDQ0_29					
MEM_A_DQ<28>	AU27	MDQ0_28					
MEM_A_DQ<27>	AP25	MDQ0_27	MA0_14	AR23	MEM_A_A<14>		
MEM_A_DQ<26>	AR25	MDQ0_26	MA0_13	AU15	MEM_A_A<13>		
MEM_A_DQ<25>	AP27	MDQ0_25	MA0_12	AN23	MEM_A_A<12>		
MEM_A_DQ<24>	AR27	MDQ0_24	MA0_11	AN21	MEM_A_A<11>		
MEM_A_DQ<23>	AP29	MDQ0_23	MA0_10	AN19	MEM_A_A<10>		
MEM_A_DQ<22>	AR29	MDQ0_22	MA0_9	AV21	MEM_A_A<9>		
MEM_A_DQ<21>	AP31	MDQ0_21	MA0_8	AR22	MEM_A_A<8>		
MEM_A_DQ<20>	AR31	MDQ0_20	MA0_7	AU21	MEM_A_A<7>		
MEM_A_DQ<19>	AV27	MDQ0_19	MA0_6	AP21	MEM_A_A<6>		
MEM_A_DQ<18>	AN29	MDQ0_18	MA0_5	AR21	MEM_A_A<5>		
MEM_A_DQ<17>	AV29	MDQ0_17	MA0_4	AN21	MEM_A_A<4>		
MEM_A_DQ<16>	AN31	MDQ0_16	MA0_3	AV19	MEM_A_A<3>		
MEM_A_DQ<15>	AU31	MDQ0_15	MA0_2	AU19	MEM_A_A<2>		
MEM_A_DQ<14>	AR33	MDQ0_14	MA0_1	AT19	MEM_A_A<1>		
MEM_A_DQ<13>	AV37	MDQ0_13	MA0_0	AR19	MEM_A_A<0>		
MEM_A_DQ<12>	AN37	MDQ0_12					
MEM_A_DQ<11>	AT31	MDQ0_11					
MEM_A_DQ<10>	AV31	MDQ0_10					
MEM_A_DQ<9>	AT37	MDQ0_9					
MEM_A_DQ<8>	AU37	MDQ0_8					
MEM_A_DQ<7>	AW39	MDQ0_7					
MEM_A_DQ<6>	AV39	MDQ0_6					
MEM_A_DQ<5>	AR37	MDQ0_5					
MEM_A_DQ<4>	AR38	MDQ0_4					
MEM_A_DQ<3>	AV38	MDQ0_3					
MEM_A_DQ<2>	AW38	MDQ0_2					
MEM_A_DQ<1>	AR35	MDQ0_1					
MEM_A_DQ<0>	AP35	MDQ0_0					
MEM_A_DM<7>	AN5	MDQM0_7					
MEM_A_DM<6>	AU5	MDQM0_6					
MEM_A_DM<5>	AR10	MDQM0_5					
MEM_A_DM<4>	AN13	MDQM0_4	MODT0A_1	AP15	MEM_A_ODT<1>		
MEM_A_DM<3>	AW27	MDQM0_3	MODT0A_0	AV15	MEM_A_ODT<0>		
MEM_A_DM<2>	AW29	MDQM0_2					
MEM_A_DM<1>	AV35	MDQM0_1	MCKE0A_1	AU23	MEM_A_CKE<1>		
MEM_A_DM<0>	AR34	MDQM0_0	MCKE0A_0	AT23	MEM_A_CKE<0>		

MEMORY CONTROL 0A

MCLK0A_2_P	AW33	TP_MEM_A_CLK2P
MCLK0A_2_N	AV33	TP_MEM_A_CLK2N
MCLK0A_1_P	BA24	MEM_A_CLK_P<1>
MCLK0A_1_N	AY24	MEM_A_CLK_N<1>
MCLK0A_0_P	BB20	MEM_A_CLK_P<0>
MCLK0A_0_N	BC20	MEM_A_CLK_N<0>
MCS0A_1#	AT15	MEM_A_CS_L<1>
MCS0A_0#	AR18	MEM_A_CS_L<0>

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MEMORY PARTITION 1

MEM_B_DQ<63>	AT4	MDQ1_63	MDQS1_7_P	AT2	MEM_B_DQS_P<7>		
MEM_B_DQ<62>	AT3	MDQ1_62	MDQS1_7_N	AT1	MEM_B_DQS_N<7>		
MEM_B_DQ<61>	AV2	MDQ1_61	MDQS1_6_P	AY2	MEM_B_DQS_P<6>		
MEM_B_DQ<60>	AV3	MDQ1_60	MDQS1_6_N	AY1	MEM_B_DQS_N<6>		
MEM_B_DQ<59>	AR4	MDQ1_59	MDQS1_5_P	BB6	MEM_B_DQS_P<5>		
MEM_B_DQ<58>	AR3	MDQ1_58	MDQS1_5_N	BA6	MEM_B_DQS_N<5>		
MEM_B_DQ<57>	AU2	MDQ1_57	MDQS1_4_P	BA10	MEM_B_DQS_P<4>		
MEM_B_DQ<56>	AU3	MDQ1_56	MDQS1_4_N	AY11	MEM_B_DQS_N<4>		
MEM_B_DQ<55>	AY4	MDQ1_55	MDQS1_3_P	BB33	MEM_B_DQS_P<3>		
MEM_B_DQ<54>	AY3	MDQ1_54	MDQS1_3_N	BA33	MEM_B_DQS_N<3>		
MEM_B_DQ<53>	BB3	MDQ1_53	MDQS1_2_P	BB37	MEM_B_DQS_P<2>		
MEM_B_DQ<52>	BC3	MDQ1_52	MDQS1_2_N	BA37	MEM_B_DQS_N<2>		
MEM_B_DQ<51>	AW4	MDQ1_51	MDQS1_1_P	BA43	MEM_B_DQS_P<1>		
MEM_B_DQ<50>	AW3	MDQ1_50	MDQS1_1_N	AY42	MEM_B_DQS_N<1>		
MEM_B_DQ<49>	BA3	MDQ1_49	MDQS1_0_P	AT42	MEM_B_DQS_P<0>		
MEM_B_DQ<48>	BB2	MDQ1_48	MDQS1_0_N	AT43	MEM_B_DQS_N<0>		
MEM_B_DQ<47>	BB5	MDQ1_47					
MEM_B_DQ<46>	BA5	MDQ1_46					
MEM_B_DQ<45>	BA8	MDQ1_45					
MEM_B_DQ<44>	BC8	MDQ1_44					
MEM_B_DQ<43>	BB4	MDQ1_43					
MEM_B_DQ<42>	BC4	MDQ1_42	MRAS1#	AW16	MEM_B_RAS_L		
MEM_B_DQ<41>	BA7	MDQ1_41	MCAS1#	BA15	MEM_B_CAS_L		
MEM_B_DQ<40>	AY8	MDQ1_40	MWE1#	BA16	MEM_B_WE_L		
MEM_B_DQ<39>	BA9	MDQ1_39					
MEM_B_DQ<38>	BB10	MDQ1_38					
MEM_B_DQ<37>	BB12	MDQ1_37					
MEM_B_DQ<36>	AW12	MDQ1_36					
MEM_B_DQ<35>	BB8	MDQ1_35					
MEM_B_DQ<34>	BB9	MDQ1_34	MBA1_2	BB29	MEM_B_BA<2>		
MEM_B_DQ<33>	AY12	MDQ1_33	MBA1_1	BB18	MEM_B_BA<1>		
MEM_B_DQ<32>	BA12	MDQ1_32	MBA1_0	BB17	MEM_B_BA<0>		
MEM_B_DQ<31>	BC32	MDQ1_31					
MEM_B_DQ<30>	AW32	MDQ1_30					
MEM_B_DQ<29>	BA35	MDQ1_29					
MEM_B_DQ<28>	AY36	MDQ1_28					
MEM_B_DQ<27>	BA32	MDQ1_27	MA1_14	BA29	MEM_B_A<14>		
MEM_B_DQ<26>	BB32	MDQ1_26	MA1_13	BA14	MEM_B_A<13>		
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MEM_B_DQ<8>	AW41	MDQ1_8					
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MEM_B_DQ<5>	AP41	MDQ1_5					
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MEM_B_DQ<3>	AU40	MDQ1_3	MCLK1A_1_N	BA22	MEM_B_CLK_N<1>		
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MEM_B_DM<7>	AT5	MDQM1_7					
MEM_B_DM<6>	BA2	MDQM1_6					
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MEM_B_DM<1>	AY43	MDQM1_1	MODT1A_0	AV15	MEM_B_ODT<0>		
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			MCKE1A_0	BB30	MEM_B_CKE<0>		

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
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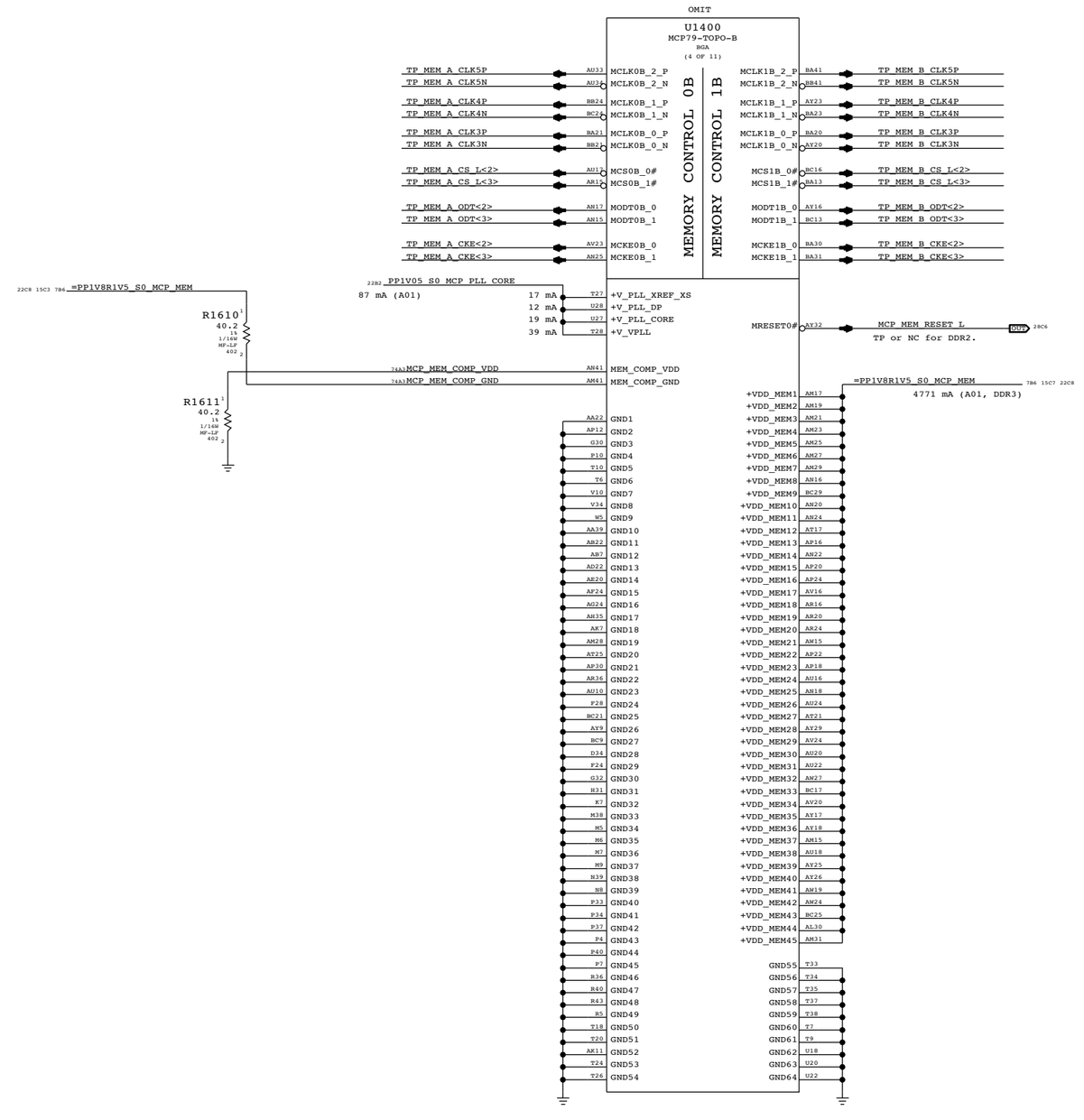
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=T18 MLB	SYNC DATE=04/04/2008
PAGE TITLE: MCP Memory Misc	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 16 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

8D6	IN	=PEG_D2R_P<0>	F7	PE0_RX0_P	PE0_TX0_P	C5	=PEG_R2D_C_P<0>
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8D6	IN	=PEG_D2R_P<10>	L9	PE0_RX10_P	PE0_TX10_P	H1	=PEG_R2D_C_P<10>
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				Int PU	PE0_REFCLK_P	E11	PEG_CLK100M_P
8D6	IN	PEG_PRSNT_L	C9	PE0_PRSNT_16#	PE0_REFCLK_N	D11	PEG_CLK100M_N
				Int PU			
29D7	IN	MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49	PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P
29D7	IN	PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N
				Int PU			
35D3	IN	FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50	PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P
35D3 8C6	IN	PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N
				Int PU			
8D6	IN	EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51	PE3_REFCLK_P	G13	PCIE_CLK100M_EXCARD_P
8D6	IN	PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	PE3_REFCLK_N	F13	PCIE_CLK100M_EXCARD_N
				Int PU			
		TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16	PE4_REFCLK_P	J13	TP_PCIE_CLK100M_PE4P
		TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46	PE4_REFCLK_N	B13	TP_PCIE_CLK100M_PE4N
				Int PU			
57A4		AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17	PE5_REFCLK_P	L14	TP_PCIE_CLK100M_PE5P
8C4	OUT	GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47	PE5_REFCLK_N	E14	TP_PCIE_CLK100M_PE5N
				Int PU			
30B7	OUT	CARDREADER_RESET	M17	PEG_CLKREQ#/GPIO_18	PE6_REFCLK_P	N14	TP_PCIE_CLK100M_PE6P
8C4	IN	GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48	PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N
				Int PU			
29C7 6D5	IN	PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	PEX_RST0#	E11	PCIE_RESET_L

75D3 29C7 6D5	IN	PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8	PCIE_MINI_R2D_C_P
75D3 29C7 6D5	IN	PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8	PCIE_MINI_R2D_C_N
75D3 34C1	IN	PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8	PCIE_FW_R2D_C_P
75D3 34C1	IN	PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8	PCIE_FW_R2D_C_N
8D6	IN	PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	PE1_TX2_P	A7	PCIE_EXCARD_R2D_C_P
8D6	IN	PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	PE1_TX2_N	B7	PCIE_EXCARD_R2D_C_N
		TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP
		TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6	TP_PCIE_PE4_R2D_CN

7A6	=PP1V05_S0_MCP_PEX_DVDD0		T17	+DVDD0_PEX1	+AVDD0_PEX1	Y12	=PP1V05_S0_MCP_PEX_AVDD0 7A6
	57 mA (A01, DVDD0 & 1)		W19	+DVDD0_PEX2	+AVDD0_PEX2	AA12	206 mA (A01, AVDD0 & 1)
			U17	+DVDD0_PEX3	+AVDD0_PEX3	AB12	
			V19	+DVDD0_PEX4	+AVDD0_PEX4	M12	
			W16	+DVDD0_PEX5	+AVDD0_PEX5	P12	
			W17	+DVDD0_PEX6	+AVDD0_PEX6	R12	
			W18	+DVDD0_PEX7	+AVDD0_PEX7	N12	
			U16	+DVDD0_PEX8	+AVDD0_PEX8	T12	
					+AVDD0_PEX9	U12	
7A6	=PP1V05_S0_MCP_PEX_DVDD1		T19	+DVDD1_PEX1	+AVDD0_PEX10	AC12	
			U19	+DVDD1_PEX2	+AVDD0_PEX11	AD12	
					+AVDD0_PEX12	V12	
					+AVDD0_PEX13	W12	
22C2	PP1V05_S0_MCP_PLL_PEX		T16	+V_PLL_PEX			=PP1V05_S0_MCP_PEX_AVDD1 7A6
	84 mA (A01)				+AVDD1_PEX1	M13	
75C3	MCP_PEX_CLK_COMP		A11	PEX_CLK_COMP	+AVDD1_PEX2	N13	
					+AVDD1_PEX3	P13	

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

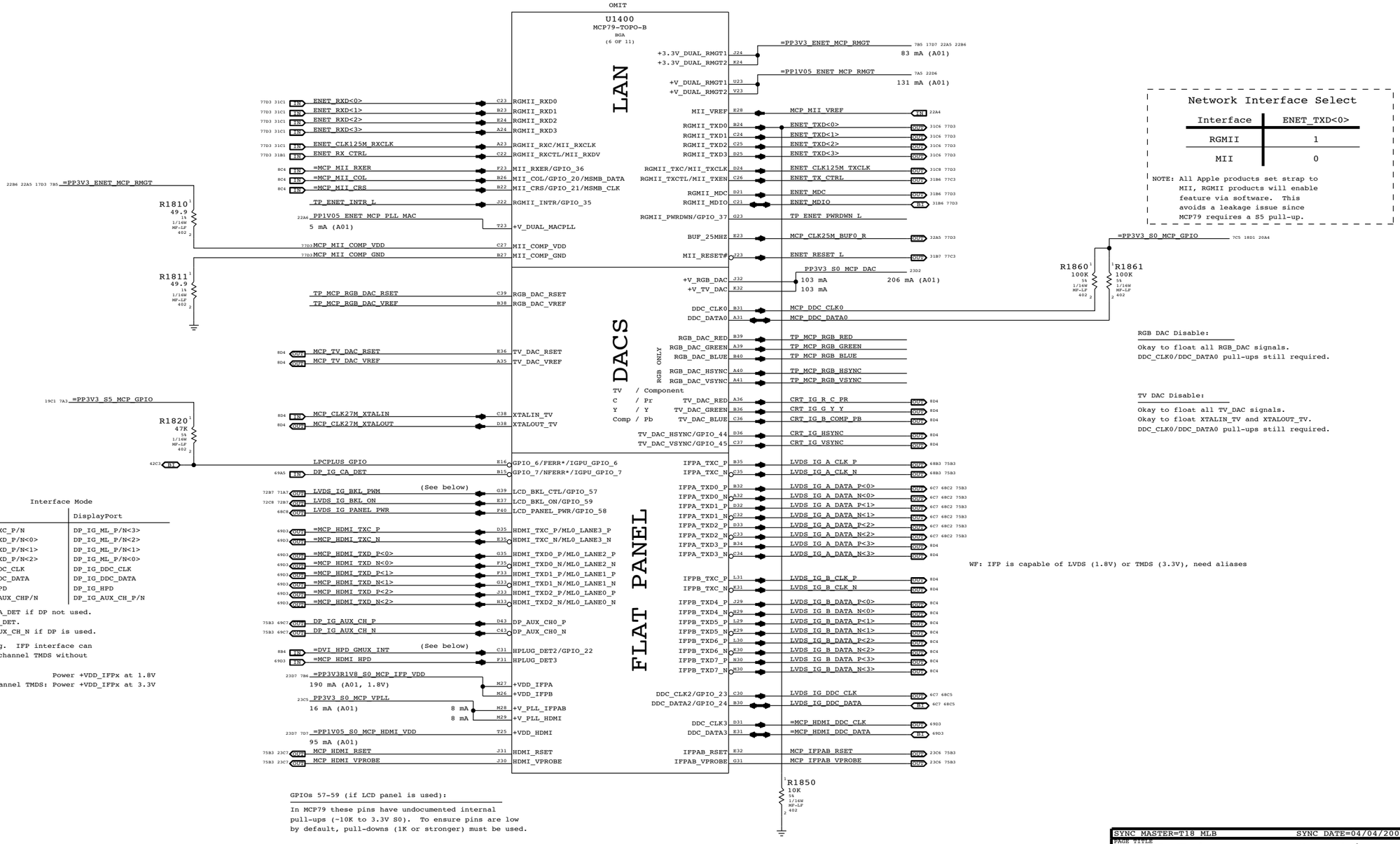
SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 17 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).


OMIT
U1400
MCP79-TOPO-B
BGA
(6 OF 11)
LAN
DACS
FLAT PANEL
ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_CLK125M_RXCLK
ENET_RX_CTRL
=MCP_MII_RXER
=MCP_MII_COL
=MCP_MII_CRS
TP_ENET_INTR_L
PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
MCP_MII_COMP_VDD
MCP_MII_COMP_GND
TP_MCP_RGB_DAC_RSET
TP_MCP_RGB_DAC_VREF
MCP_TV_DAC_RSET
MCP_TV_DAC_VREF
MCP_CLK27M_XTALIN
MCP_CLK27M_XTALOUT
LPCPLUS_GPIO
DP_IG_CA_DET
LVDS_IG_BKL_PWM
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
=MCP_HDMI_TXC_P
=MCP_HDMI_TXC_N
=MCP_HDMI_TXD_P<0>
=MCP_HDMI_TXD_N<0>
=MCP_HDMI_TXD_P<1>
=MCP_HDMI_TXD_N<1>
=MCP_HDMI_TXD_P<2>
=MCP_HDMI_TXD_N<2>
DP_IG_AUX_CH_P
DP_IG_AUX_CH_N
=DVI_HPD_GMUX_INT
=MCP_HDMI_HPD
=PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)
=PP3V3_S0_MCP_VPLL
16 mA (A01)
8 mA
8 mA
=PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)
MCP_HDMI_RSET
MCP_HDMI_VPROBE
(See below)
(See below)
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RGMII_RXC/MII_RXCLK
RGMII_RXCTL/MII_RXDV
MII_RXER/GPIO_36
MII_COL/GPIO_20/MSMB_DATA
MII_CRS/GPIO_21/MSMB_CLK
RGMII_INTR/GPIO_35
+V_DUAL_MACPLL
MII_COMP_VDD
MII_COMP_GND
RGB_DAC_RSET
RGB_DAC_VREF
TV_DAC_RSET
TV_DAC_VREF
XTALIN_TV
XTALOUT_TV
GPIO_6/FERR*/IGPU_GPIO_6
GPIO_7/NFERR*/IGPU_GPIO_7
LCD_BKL_CTL/GPIO_57
LCD_BKL_ON/GPIO_59
LCD_PANEL_PWR/GPIO_58
HDMI_TXC_P/ML0_LANE3_P
HDMI_TXC_N/ML0_LANE3_N
HDMI_TXD0_P/ML0_LANE2_P
HDMI_TXD0_N/ML0_LANE2_N
HDMI_TXD1_P/ML0_LANE1_P
HDMI_TXD1_N/ML0_LANE1_N
HDMI_TXD2_P/ML0_LANE0_P
HDMI_TXD2_N/ML0_LANE0_N
DP_AUX_CH0_P
DP_AUX_CH0_N
HPLUG_DET2/GPIO_22
HPLUG_DET3
+VDD_IFPA
+VDD_IFPB
+V_PLL_IFPAB
+V_PLL_HDMI
+VDD_HDMI
HDMI_RSET
HDMI_VPROBE
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
+3.3V_DUAL_RMGT1
+3.3V_DUAL_RMGT2
+V_DUAL_RMGT1
+V_DUAL_RMGT2
MII_VREF
RGMII_TXD0
RGMII_TXD1
RGMII_TXD2
RGMII_TXD3
RGMII_TXC/MII_TXCLK
RGMII_TXCTL/MII_TXEN
RGMII_MDC
RGMII_MDIO
RGMII_PWRDWN/GPIO_37
BUF_25MHZ
MII_RESET#
PP3V3_S0_MCP_DAC
+V_RGB_DAC
+V_TV_DAC
103 mA
103 mA
206 mA (A01)
DDC_CLK0
DDC_DATA0
RGB_DAC_RED
RGB_DAC_GREEN
RGB_DAC_BLUE
RGB_DAC_HSYNC
RGB_DAC_VSYNC
RGB ONLY
TV / Component
C / Pr
Y / Y
Comp / Pb
TV_DAC_RED
TV_DAC_GREEN
TV_DAC_BLUE
TV_DAC_HSYNC/GPIO_44
TV_DAC_VSYNC/GPIO_45
IFPA_TXC_P
IFPA_TXC_N
IFPA_TXD0_P
IFPA_TXD0_N
IFPA_TXD1_P
IFPA_TXD1_N
IFPA_TXD2_P
IFPA_TXD2_N
IFPA_TXD3_P
IFPA_TXD3_N
IFPB_TXC_P
IFPB_TXC_N
IFPB_TXD4_P
IFPB_TXD4_N
IFPB_TXD5_P
IFPB_TXD5_N
IFPB_TXD6_P
IFPB_TXD6_N
IFPB_TXD7_P
IFPB_TXD7_N
DDC_CLK2/GPIO_23
DDC_DATA2/GPIO_24
DDC_CLK3
DDC_DATA3
IFPAB_RSET
IFPAB_VPROBE
MCP_MII_VREF
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ENET_TXD<2>
ENET_TXD<3>
ENET_CLK125M_TXCLK
ENET_TX_CTRL
ENET_MDC
ENET_MDIO
TP_ENET_PWRDWN_L
MCP_CLK25M_BUF0_R
ENET_RESET_L
MCP_DDC_CLK0
MCP_DDC_DATA0
TP_MCP_RGB_RED
TP_MCP_RGB_GREEN
TP_MCP_RGB_BLUE
TP_MCP_RGB_HSYNC
TP_MCP_RGB_VSYNC
CRT_IG_R_C_PR
CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB
CRT_IG_HSYNC
CRT_IG_VSYNC
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LVDS_IG_A_CLK_N
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LVDS_IG_B_CLK_N
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LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>
LVDS_IG_B_DATA_N<2>
LVDS_IG_B_DATA_P<3>
LVDS_IG_B_DATA_N<3>
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
=MCP_HDMI_DDC_CLK
=MCP_HDMI_DDC_DATA
MCP_IFPAB_RSET
MCP_IFPAB_VPROBE
R1810
49.9
1% 1/16W MF-LF 402
R1811
49.9
1% 1/16W MF-LF 402
R1820
47K
5% 1/16W MF-LF 402
R1850
10K
5% 1/16W MF-LF 402
R1860
100K
5% 1/16W MF-LF 402
R1861
100K
1% 1/16W MF-LF 402
=PP3V3_S0_MCP_GPIO
Network Interface Select
Interface | ENET_TXD<0>
RGMII | 1
MII | 0
NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.
RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.
TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.
Interface Mode
MCP Signal | TMDS/HDMI | DisplayPort
=MCP_HDMI_TXC_P/N | TMDS_IG_TXC_P/N | DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0> | TMDS_IG_TXD_P/N<0> | DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1> | TMDS_IG_TXD_P/N<1> | DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2> | TMDS_IG_TXD_P/N<2> | DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK | TMDS_IG_DDC_CLK | DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA | TMDS_IG_DDC_DATA | DP_IG_DDC_DATA
=MCP_HDMI_HPD | TMDS_IG_HPD | DP_IG_HPD
DP_IG_AUX_CH_P/N | TP_DP_IG_AUX_CHP/N | DP_IG_AUX_CH_P/N
NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V
WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases
GPIOs 57-59 (if LCD panel is used):
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.
=DVI_HPD_GMUX_INT:
Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.
SYNC MASTER=T18 MLB
SYNC DATE=04/04/2008
PAGE TITLE
MCP Ethernet & Graphics
Apple Inc.
DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 18 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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OMIT

U1400
MCP79-TOPO-B
BGA
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PCI

76D3 18D3 PCI_REQ0_L	T2	PCI_REQ0#	
76D3 18D7 PCI_REQ1_L	V5	PCI_REQ1#/FANRPM2	
35D6 35C7 35C4 35A4 18D7 FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT2#/GPIO_41/RS232_DTR# R4
57D7 OUT AUD_IPHS_SWITCH_EN	U5	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT3#/GPIO_39/RS232_RTS# U11
18D2 IN MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT4#/GPIO_53/RS232_SOUT# P3

76D3 12C3 MCP_DEBUG<0>	AC3	PCI_AD0	
76D3 12C3 MCP_DEBUG<1>	AE10	PCI_AD1	
76D3 12C3 MCP_DEBUG<2>	AC4	PCI_AD2	
76D3 12C3 MCP_DEBUG<3>	AE11	PCI_AD3	
76D3 12C3 MCP_DEBUG<4>	AB3	PCI_AD4	
76D3 12C3 MCP_DEBUG<5>	AC6	PCI_AD5	
76D3 12C3 MCP_DEBUG<6>	AB2	PCI_AD6	
76D3 12C3 MCP_DEBUG<7>	AC7	PCI_AD7	
TP_PCI_AD<8>	AC8	PCI_AD8	
TP_PCI_AD<9>	AA2	PCI_AD9	
TP_PCI_AD<10>	AC9	PCI_AD10	
TP_PCI_AD<11>	AC10	PCI_AD11	
TP_PCI_AD<12>	AC11	PCI_AD12	
TP_PCI_AD<13>	AA1	PCI_AD13	
TP_PCI_AD<14>	AA5	PCI_AD14	
TP_PCI_AD<15>	Y5	PCI_AD15	
TP_PCI_AD<16>	W3	PCI_AD16	
TP_PCI_AD<17>	W6	PCI_AD17	
TP_PCI_AD<18>	W4	PCI_AD18	
TP_PCI_AD<19>	W7	PCI_AD19	
TP_PCI_AD<20>	V3	PCI_AD20	
TP_PCI_AD<21>	W8	PCI_AD21	
TP_PCI_AD<22>	V2	PCI_AD22	
TP_PCI_AD<23>	W9	PCI_AD23	
TP_PCI_AD<24>	U3	PCI_AD24	
TP_PCI_AD<25>	W11	PCI_AD25	
TP_PCI_AD<26>	U2	PCI_AD26	
TP_PCI_AD<27>	U5	PCI_AD27	
TP_PCI_AD<28>	U1	PCI_AD28	
TP_PCI_AD<29>	U6	PCI_AD29	
TP_PCI_AD<30>	T5	PCI_AD30	
TP_PCI_AD<31>	U7	PCI_AD31	

TP_PCI_INTW_L	P2	PCI_INTW#	
TP_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
TP_PCI_INTZ_L	N1	PCI_INTZ#	
TP_PCI_TRDY_L	Y3	PCI_TRDY#	
42D5 40C5 IN PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
8C2 IN FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU	
TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU	
42D3 40C8 BI LPC_SERIRQ	AE6	LPC_SERIRQ Int PU	

PCI_GNT0#	R3	TP_PCI_GNT0_L	
PCI_GNT1#/PANCTL2	U10	TP_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	OUT 8C4
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	OUT 8C4
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	OUT 18D2

PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	
PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	

PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	
PCI_FRAME#	Y4	TP_PCI_FRAME_L	
PCI_IRDY#	AA10	TP_PCI_IRDY_L	
PCI_PAR	Y1	TP_PCI_PAR	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L	
PCI_SERR#	AA7	TP_PCI_SERR_L	
PCI_STOP#	Y2	TP_PCI_STOP_L	
PCI_PME#/GPIO_30 Int PU (S5)	P1	PM_LATRIGGER_L	OUT 12C6

PCI_RESET0#	R10	MEM_VTT_EN_R	OUT 24C4
PCI_RESET1#	R11	TP_PCI_RESET1_L	

PCI_CLK0	R6	TP_PCI_CLK0	
PCI_CLK1	R7	TP_PCI_CLK1	
PCI_CLK2	R8	76C3 PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	76C3 PCI_CLK33M_MCP	

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402 LPC_FRAME_L OUT 40C8 42D5 76C3
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L	OUT 40C5 42D3
LPC_RESET#	AE5	LPC_RESET_L	OUT 24D4 76C3
LPC_AD0	AD3	LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402 LPC_AD<0> BI 40C8 42D5 76C3
LPC_AD1	AD2	LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402 LPC_AD<1> BI 40C8 42D5 76C3
LPC_AD2	AD1	LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402 LPC_AD<2> BI 40C8 42D3 76C3
LPC_AD3	AD5	LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402 LPC_AD<3> BI 40C8 42D3 76C3
LPC_CLK0	AE9	LPC_CLK33M_SMC_R	OUT 24B4 76C3

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

20A4 17C1 7C5 =PP3V3_S0_MCP_GPIO

18D4 MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
76D3 18D7 PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
76D3 18D7 PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
35D6 35C7 35C4 35A4 18D7 FW_PWR_EN	R1992	8.2K	5% 1/16W MF-LF 402
18D7 MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE: MCP PCI & LPC

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
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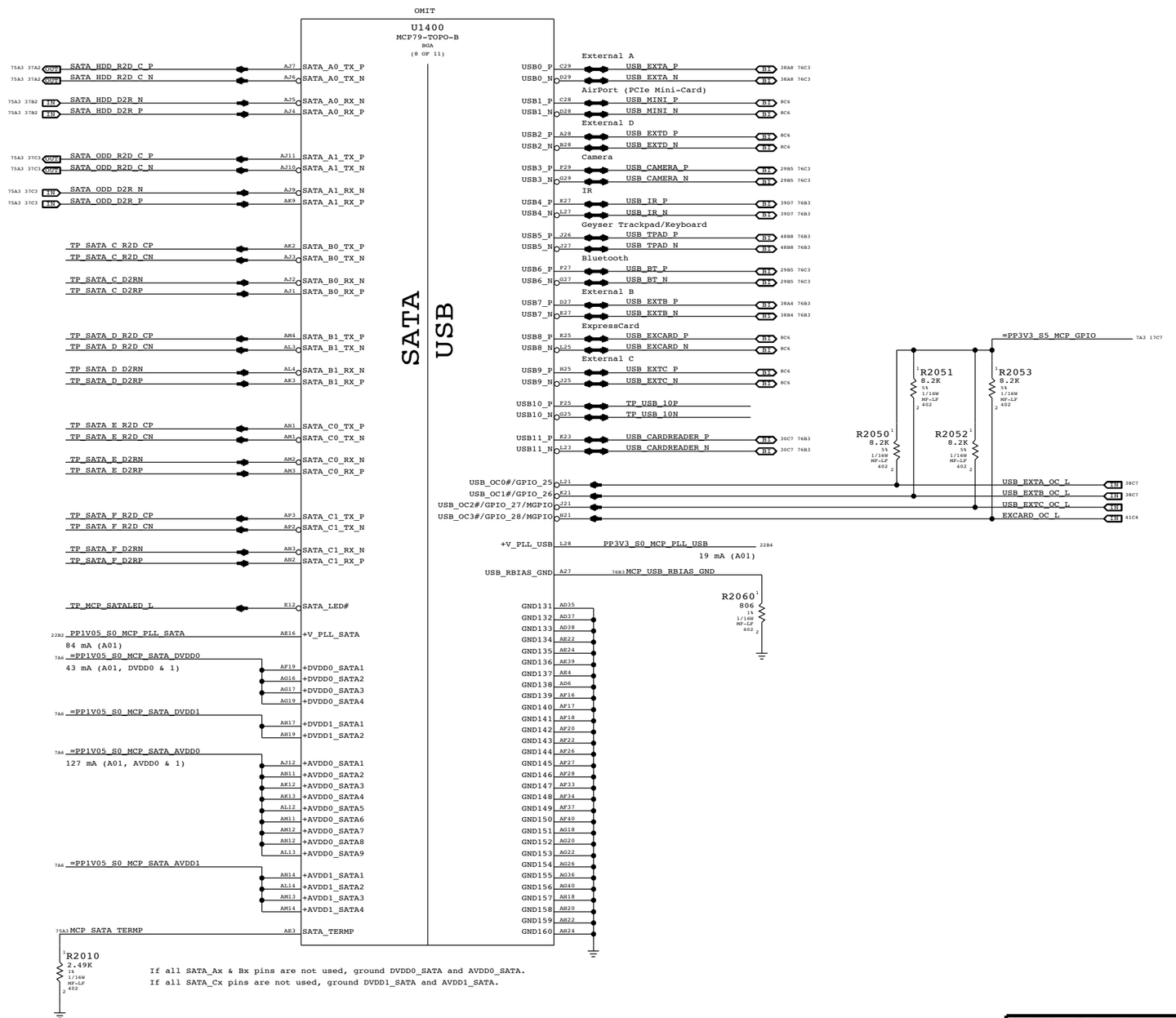
PAGE: 19 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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SYNC MASTER=T18 MLB | SYNC DATE=04/04/2008

PAGE TITLE: MCP SATA & USB

Apple Inc.

DRAWING NUMBER: 051-7898 | SIZE: D

REVISION: C.0.0

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PAGE: 20 OF 109

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OMIT

U1400
MCP79-TOPO-B
BGA
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HDA

HDA_SDIN0	G15	HDA_SDATA_IN0	Int PD
TP_MLB_RAM_SIZE	J14	HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK	Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems)	J15	HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA	Int PD
MCP_HDA_PULLDN_COMP	A15	HDA_PULLDN_COMP	
+V_PLL_NV_H	AE18		20 mA
+V_PLL_SP_SPREF	AE17		17 mA
=SPI_CS1_R_L_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1	
SMC_ADAPTER_EN	L26	GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L	
TP_SB_A20GATE	K13	A20GATE	Int PU
TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN*	Int PU
SMC_WAKE_SCI_L	C19	SIO_PME*	Int PU (S5)
SMC_RUNTIME_SCI_L	C18	EXT_SMI/GPIO_32*	Int PU (S5)
SM_INTRUDER_L	B20	INTRUDER*	
TP_MCP_LID_L	M25	LID*	Int PU (S5)
PM_BATLOW_L	M24	LLB*	Int PU (S5)
PM_DPRSLPVR	M22	CPU_DPRSLPVR	
PM_PWRBTN_L	C16	PWRBTN*	Int PU (S5)
PM_SYSRST_DEBOUNCE_L	D16	RSTBTN*	Int PU
RTC_RST_L	C20	RTC_RST*	
PM_RSMRST_L	D20	PWRGD_SB	
MCP_PS_PWRGD	E20	PS_PWRGD	
MCP_CPU_VLD	C17	CPU_VLD	
JTAG_MCP_TDI	E19	JTAG_TDI	Int PU
JTAG_MCP_TDO	F19	JTAG_TDO	
JTAG_MCP_TMS	J19	JTAG_TMS	Int PU
JTAG_MCP_TRST_L	J18	JTAG_TRST*	
JTAG_MCP_TCK	G19	JTAG_TCK	
MCP_CLK25M_XTALIN	A16	XTALIN	
MCP_CLK25M_XTALOUT	B16	XTALOUT	
RTC_CLK32K_XTALIN	A19	XTALIN_RTC	
RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC	

=PP3V3R1V5_S0_MCP_HDA — 7 mA (A01)

R2160 8.2K 5% 1/16W MF-LF 402

+V_DUAL_HDA1	J16		
+V_DUAL_HDA2	K16		
HDA_SDATA_OUT	F15	HDA_SDOUT_R	R2170 22
HDA_BITCLK	E15	HDA_BIT_CLK_R	R2171 22
HDA_RESET*	K15	HDA_RST_R_L	R2172 22
HDA_SYNC	L15	HDA_SYNC_R	R2173 22

R2170 HDA_SDOUT_R → HDA_SDOUT (OUT) 52C7 76A3
R2171 HDA_BIT_CLK_R → HDA_BIT_CLK (OUT) 52C7 76B3
R2172 HDA_RST_R_L → HDA_RST_L (OUT) 52C7 76A3
R2173 HDA_SYNC_R → HDA_SYNC (OUT) 52C7 76B3

=PP3V3R1V5_S0_MCP_HDA → R2110 49.9 1% 1/16W MF-LF 402 → MCP_HDA_PULLDN_COMP

PP1V05_S0_MCP_PLL_NV — 37 mA (A01) → +V_PLL_NV_H

=PP3V3_G3_RTC → R2120 49.9K 1% 1/16W MF-LF 402 → R2121 49.9K 1% 1/16W MF-LF 402

MISC

HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK	K17	MCP_GPIO_4	20A4
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA	L17	AUD_I2C_INT_L	IN 20A4 57D3
SLP_S3*	G17	PM_SLP_S3_L	OUT 6C3 32B7 35A5 40C5 66D5 70D8
SLP_RMGT*	J17	PM_SLP_RMGT_L	OUT 8D1
SLP_S5*	H17	PM_SLP_S4_L	OUT 6C3 40C5 41A2 66C8
THERM_DIODE_P	B11	MCP_THMDIODE_P	OUT 46B5 80D3
THERM_DIODE_N	C11	MCP_THMDIODE_N	OUT 46B5 80D3
MCP_VID0/GPIO_13	L20	MCP_VID<0>	OUT 20A3 63D8
MCP_VID1/GPIO_14	M20	MCP_VID<1>	OUT 20A3 63C8
MCP_VID2/GPIO_15	M21	MCP_VID<2>	OUT 20A3 63C8
SPKR	C13	MCP_SPKR	OUT 41C5
SMB_CLK0	L19	SMBUS_MCP_0_CLK	OUT 12B6 43D8 76B3
SMB_DATA0	K19	SMBUS_MCP_0_DATA	BI 12B6 43D8 76B3
SMB_CLK1/MSMB_CLK	G21	SMBUS_MCP_1_CLK	OUT 43B8 76B3
SMB_DATA1/MSMB_DATA	F21	SMBUS_MCP_1_DATA	BI 43B8 76B3
SMB_ALERT*/GPIO_64	M23	AP_PWR_EN	OUT 20A3 29D5 32C7
(MGPIO2) FANRPM0/GPIO_60	B12	MEM_EVENT_L	IN 20A4 26A5 27A5 40B8
FANCTL0/GPIO_61	A12	ODD_PWR_EN_L	OUT 37D6
(MGPIO3) FANRPM1/GPIO_63	D12	SMC_IG_THROTTLE_L	IN 20A4 41D4
FANCTL1/GPIO_62	C12	ARB_DETECT	20A4
CPUVDD_EN	D17	MCP_CPUVDD_EN	OUT 24A8
SPI_CS0/GPIO_10	C14	SPI_CS0_R_L	OUT 42B7 76A3
SPI_CLK/GPIO_11	D13	SPI_CLK_R	OUT 42A5 42C8 76A3
SPI_DI/GPIO_8	C15	SPI_MISO	IN 42A5 42B7 76A3
SPI_DO/GPIO_9	B14	SPI_MOSI_R	OUT 42A5 42C7 76A3
SUS_CLK/GPIO_34	B18	PM_CLK32K_SUSCLK_R	OUT 24B4 76A3
BUF_SIO_CLK	AE7	TP_MCP_BUF_SIO_CLK	
TEST_MODE_EN	K22	MCP_TEST_MODE_EN	
PKG_TEST	L22		

R2163 10K 5% 1/16W MF-LF 402
R2190 1K 1% 1/16W MF-LF 402
R2150 10K 5% 1/16W MF-LF 402
R2151 100K 5% 1/16W MF-LF 402

=PP3V3_S0_MCP
BOOT_MODE_SAFE
R2180 10K 5% 1/16W MF-LF 402 → OUT 41C5 BOOT_MODE_USER
R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R 20D4 76A3
HDA_BIT_CLK_R 20D4 76B3
HDA_RST_R_L 20D4 76A3
HDA_SYNC_R 20D4 76B3

C2170 10PF 5% 50V CERM 402
C2172 10PF 5% 50V CERM 402
C2171 10PF 5% 50V CERM 402
C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO 7C5 17C1 18D1

R2140 10K 5% 1/16W MF-LF 402
R2141 10K 5% 1/16W MF-LF 402
R2142 10K 5% 1/16W MF-LF 402
R2143 10K 5% 1/16W MF-LF 402

MCP_GPIO_4 20C3
AUD_I2C_INT_L 20C3 57D3
MEM_EVENT_L 20B3 26A5 27A5 40B8
SMC_IG_THROTTLE_L 20B3 41D4

ARB_DETECT 20B3
R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO 7D3
R2154 100K 5% 1/16W MF-LF 402
AP_PWR_EN 20C3 29D5 32C7

MCP_VID<0> 20C3 63D8
MCP_VID<1> 20C3 63C8
MCP_VID<2> 20C3 63C8

R2155 22K 5% 1/16W MF-LF 402
R2156 22K 5% 1/16W MF-LF 402
R2157 22K 5% 1/16W MF-LF 402

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SYNC MASTER=T18 MLB — SYNC DATE=06/26/2008

PAGE TITLE: MCP HDA & MISC

Apple Inc.

DRAWING NUMBER 051-7898 — SIZE D
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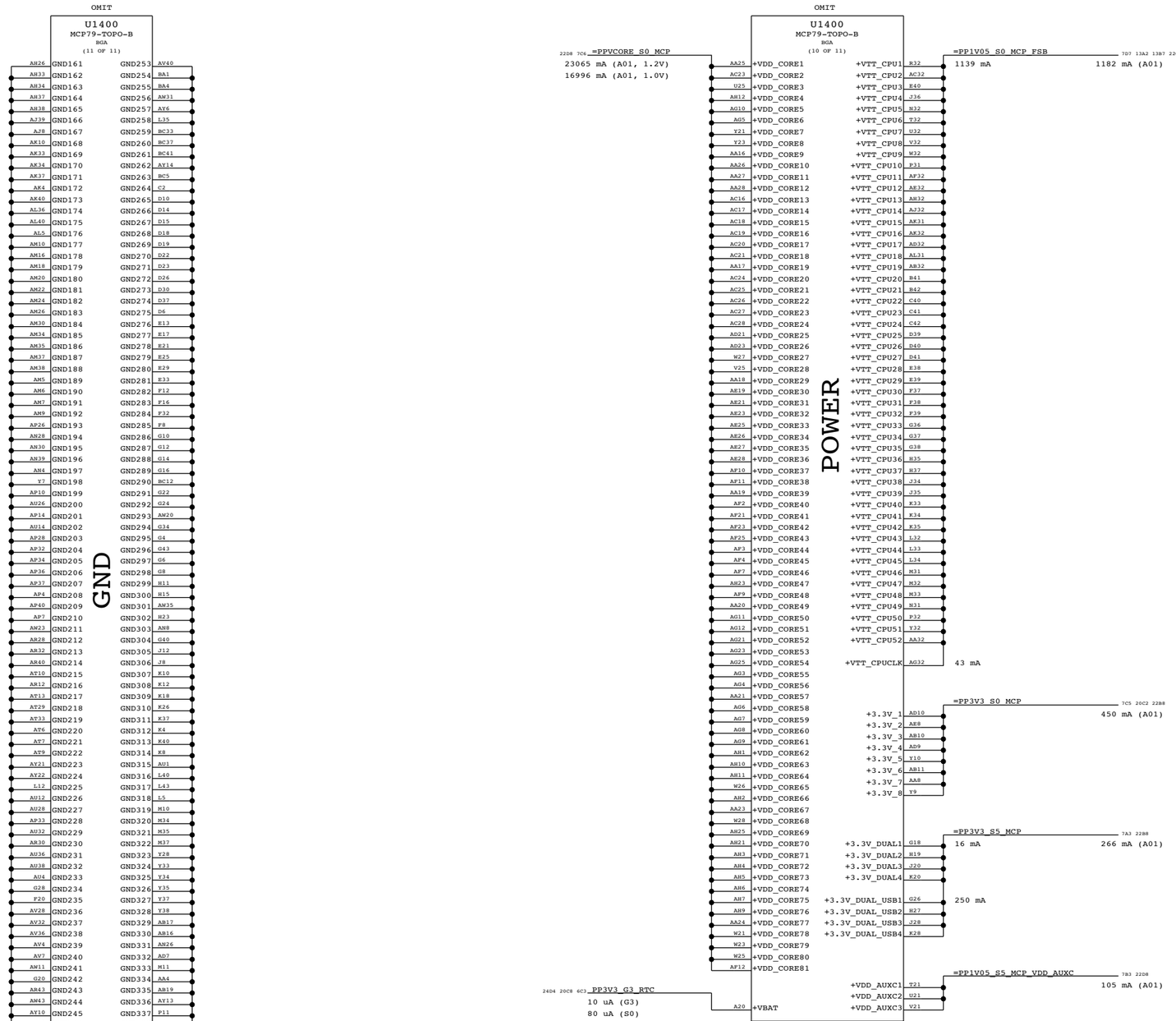

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SYNC MASTER=T18_MLB SYNC DATE=04/04/2008

PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

21D5 7C4 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R-1 402
C2501 4.7UF 20% 4V X5R-1 402
C2502 4.7UF 20% 4V X5R-1 402
C2503 4.7UF 20% 4V X5R-1 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

7D7 7A8 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R-1 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

7D7 7A8 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R-1 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

21A3 7B9 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1uF 20% 10V CERM 402
C2526 0.1uF 20% 10V CERM 402

MCP 1.05V RMGT Power

17D3 7A5 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

21D3 13B7 13A2 7D7 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

15C7 15C3 7B4 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R-1 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

21B3 20C2 7C5 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

7C5 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_S0_MCP_PLL_USB 19C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21B3 7A5 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22A5 17D7 17D3 7B9 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

20D8 20D3 7C5 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

2286 17D7 17D3 7B9 =PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF OUT 17D3
C2591 0.1UF 20% 10V CERM 402

7B8 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC 17C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R-1 402
C2596 0.1UF 20% 10V CERM 402

7D7 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

PP1V05_S0_MCP_PEX_AVDD 7A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP1V05_S0_MCP_SATA_AVDD 7A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

65B1 7B8 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB 13A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2592 10UF 20% 6.3V X5R 603
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX 16A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R-1 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA 19B6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R-1 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE 15C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R-1 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV 20C7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R-1 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

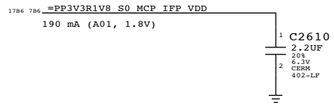
PAGE TITLE
MCP Standard Decoupling

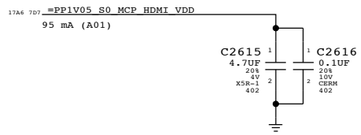
Apple Inc.

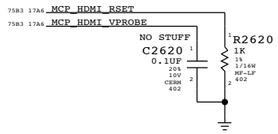
DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 25 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

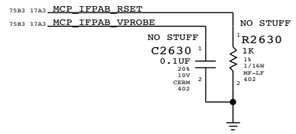
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

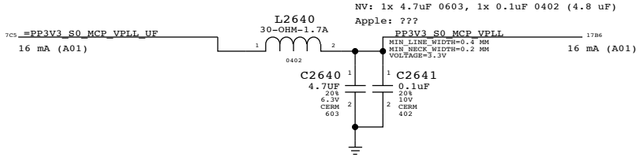




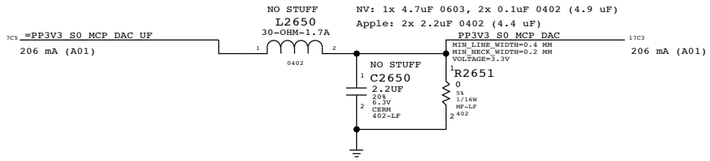




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

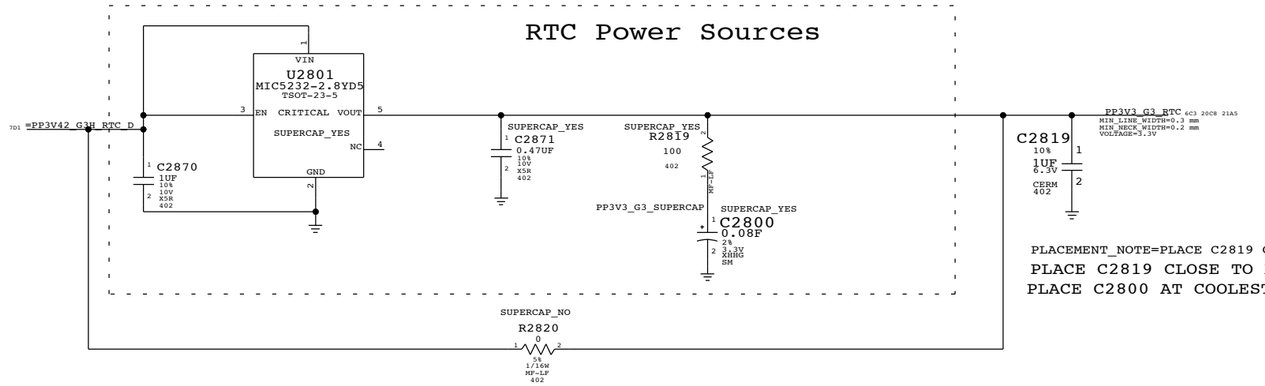
SYNC MASTER=T18 MLB SYNC DATE=12/12/2007

PAGE TITLE
MCP Graphics Support

Apple Inc.

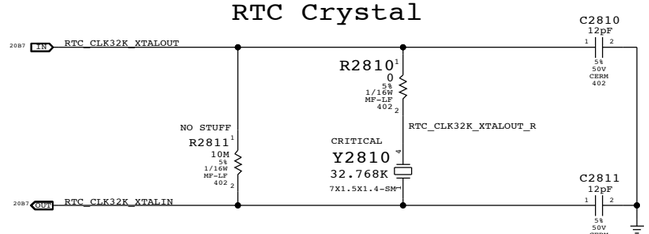
DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 26 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

RTC Power Sources



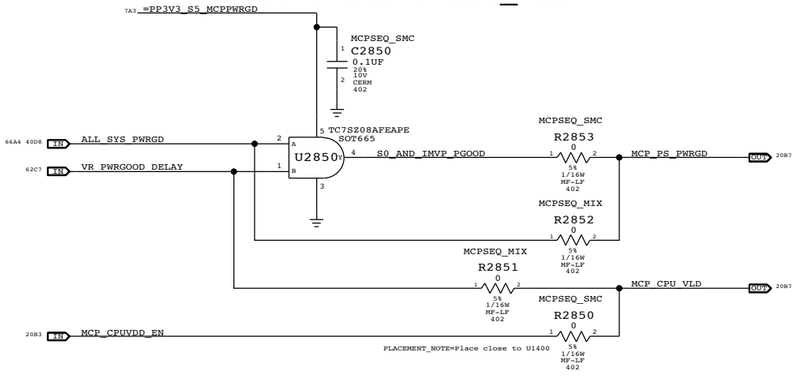
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

RTC Crystal



MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

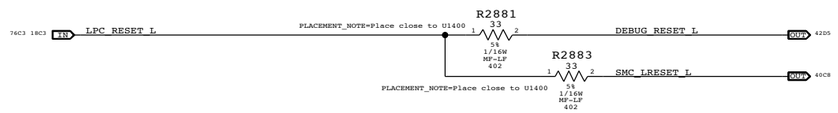
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

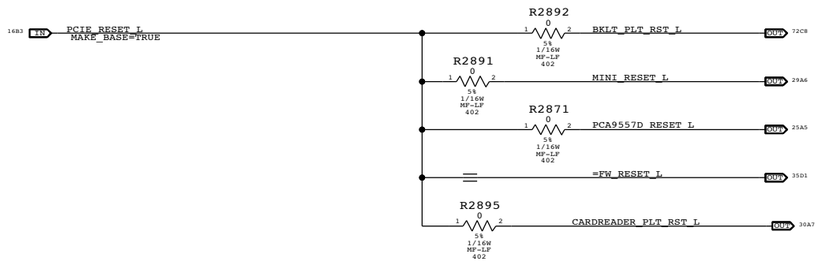
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

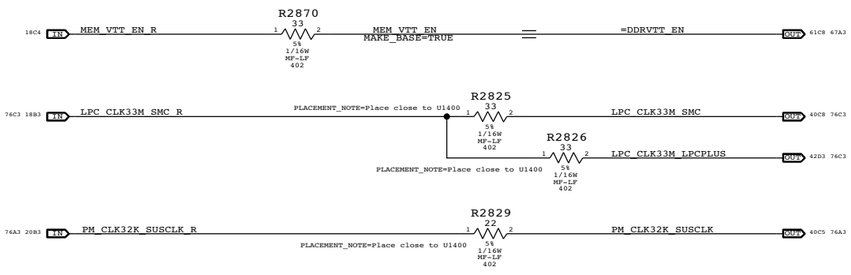
Platform Reset Connections

LPC Reset (Unbuffered)

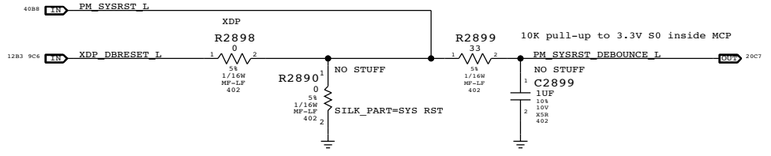


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC MASTER=RAYMOND SYNC DATE=04/05/2008

PAGE TITLE
SB Misc

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 28 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

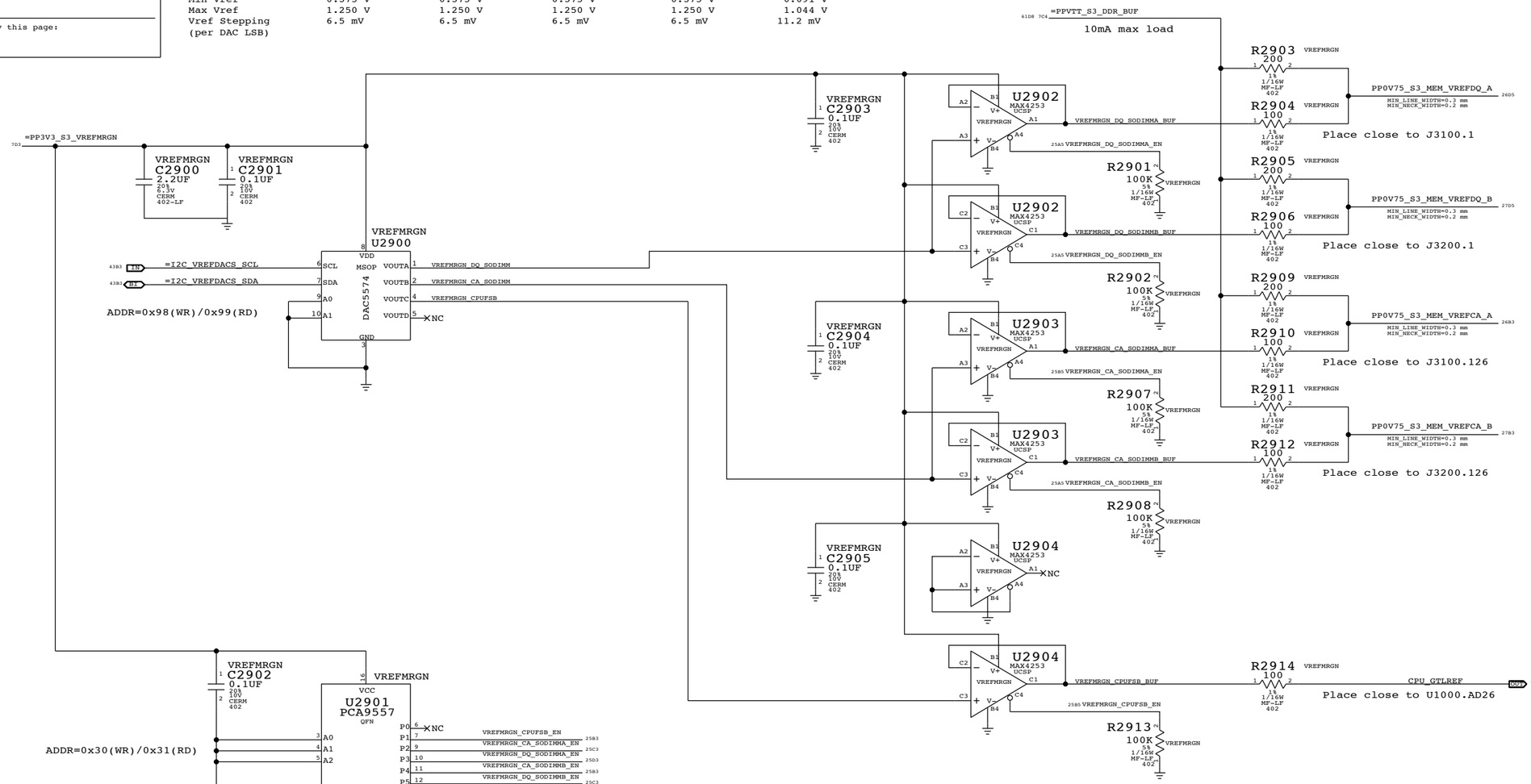
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC MASTER=BEN SYNC DATE=03/31/2008

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 29 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

7D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3111 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3112 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3113 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3114 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3115 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3116 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3117 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

74D3 14A5	IN	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>
			75	VDD	VDD	76	
	NCX		77	NC	A15	78	MEM_A_A<15>
74D3 14C5	IN	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>
			81	VDD	VDD	82	
74D3 14C5	IN	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>
74D3 14C5	IN	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>
			87	VDD	VDD	88	
74D3 14C5	IN	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>
74D3 14B5	IN	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>
			93	VDD	VDD	94	
74D3 14B5	IN	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>
74D3 14B5	IN	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>
			99	VDD	VDD	100	
74D3 14B5	IN	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>
74D3 14B5	IN	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>
			105	VDD	VDD	106	
74D3 14C5	IN	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>
74D3 14C5	IN	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L
			111	VDD	VDD	112	
74D3 14C5	IN	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>
74D3 14C5	IN	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>
			117	VDD	VDD	118	
74D3 14C5	IN	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>
74D3 14B5	IN	MEM_A_CS_L<1>	121	S1*	NC	122	NC
			123	VDD	VDD	124	
	NCX		125	TEST	VREFCA	126	
			127	VSS	VSS	128	
74D3 14C7	B1	MEM_A_DQ<32>	129	DQ32	DQ36	130	MEM_A_DQ<37>
74D3 14C7	B1	MEM_A_DQ<33>	131	DQ33	DQ37	132	MEM_A_DQ<36>
			133	VSS	VSS	134	
74C3 14B5	B1	MEM_A_DQS_N<4>	135	DQS4*	DM4	136	MEM_A_DM<4>
74C3 14B5	B1	MEM_A_DQS_P<4>	137	DQS4	VSS	138	
74D3 14C7	B1	MEM_A_DQ<34>	139	VSS	DQ38	140	MEM_A_DQ<35>
74D3 14C7	B1	MEM_A_DQ<38>	141	DQ34	DQ39	142	MEM_A_DQ<39>
			143	DQ35	VSS	144	
74D3 14C7	B1	MEM_A_DQ<44>	145	VSS	DQ44	146	MEM_A_DQ<40>
74D3 14C7	B1	MEM_A_DQ<45>	147	DQ40	DQ45	148	MEM_A_DQ<41>
			149	DQ41	VSS	150	
74C3 14B7	IN	MEM_A_DM<5>	151	VSS	DQS5*	152	MEM_A_DQS_N<5>
			153	DM5	DQS5	154	MEM_A_DQS_P<5>
			155	VSS	VSS	156	
74D3 14D7	B1	MEM_A_DQ<47>	157	DQ42	DQ46	158	MEM_A_DQ<43>
74D3 14D7	B1	MEM_A_DQ<46>	159	DQ43	DQ47	160	MEM_A_DQ<42>
			161	VSS	VSS	162	
74D3 14D7	B1	MEM_A_DQ<49>	163	DQ48	DQ52	164	MEM_A_DQ<53>
74D3 14D7	B1	MEM_A_DQ<52>	165	DQ49	DQ53	166	MEM_A_DQ<48>
			167	VSS	VSS	168	
74C3 14D5	B1	MEM_A_DQS_N<6>	169	DQS6*	DM6	170	MEM_A_DM<6>
74C3 14D5	B1	MEM_A_DQS_P<6>	171	DQS6	VSS	172	
			173	VSS	DQ54	174	MEM_A_DQ<55>
74D3 14D7	B1	MEM_A_DQ<54>	175	DQ50	DQ55	176	MEM_A_DQ<50>
74D3 14D7	B1	MEM_A_DQ<51>	177	DQ51	VSS	178	
			179	VSS	DQ60	180	MEM_A_DQ<57>
74D3 14D7	B1	MEM_A_DQ<61>	181	DQ56	DQ61	182	MEM_A_DQ<56>
74D3 14D7	B1	MEM_A_DQ<60>	183	DQ57	VSS	184	
			185	VSS	DQS7*	186	MEM_A_DQS_N<7>
74C3 14B7	IN	MEM_A_DM<7>	187	DM7	DQS7	188	MEM_A_DQS_P<7>
			189	VSS	VSS	190	
74D3 14D7	B1	MEM_A_DQ<58>	191	DQ58	DQ62	192	MEM_A_DQ<62>
74D3 14D7	B1	MEM_A_DQ<59>	193	DQ59	DQ63	194	MEM_A_DQ<63>
			195	VSS	VSS	196	
		MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L
			199	VDDSPD	SDA	200	=I2C_SODIMMA_SDA
		MEM_A_SA<1>	201	SA1	SCL	202	=I2C_SODIMMA_SCL
			203	VTT	VTT	204	

74D3 14A5 MEM_A_CKE<0> — 74D3 14A5 MEM_A_CKE<1>
NCX — J3100 F-RT-THB DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2) — 8D2
74D3 14C5 MEM_A_BA<2> — 14C5 74D3 MEM_A_A<14>
74D3 14C5 MEM_A_A<12> — 14C5 74D3 MEM_A_A<11>
74D3 14C5 MEM_A_A<9> — 14C5 74D3 MEM_A_A<7>
74D3 14C5 MEM_A_A<8> — 14B5 74D3 MEM_A_A<6>
74D3 14B5 MEM_A_A<5> — 14B5 74D3 MEM_A_A<4>
74D3 14B5 MEM_A_A<3> — 14B5 74D3 MEM_A_A<2>
74D3 14B5 MEM_A_A<1> — 14B5 74D3 MEM_A_A<0>
74D3 14B5 MEM_A_CLK_P<0> — 14B5 74D3 MEM_A_CLK_P<1>
74D3 14B5 MEM_A_CLK_N<0> — 14B5 74D3 MEM_A_CLK_N<1>
74D3 14C5 MEM_A_A<10> — 14C5 74D3 MEM_A_BA<1>
74D3 14C5 MEM_A_BA<0> — 14C5 74D3 MEM_A_RAS_L
74D3 14C5 MEM_A_WE_L — 14B5 74D3 MEM_A_CS_L<0>
74D3 14C5 MEM_A_CAS_L — 14B5 74D3 MEM_A_ODT<0>
74D3 14C5 MEM_A_A<13> — 14B5 74D3 MEM_A_ODT<1>
74D3 14B5 MEM_A_CS_L<1>
NCX
74D3 14C7 MEM_A_DQ<32> — 14C7 74D3 MEM_A_DQ<37>
74D3 14C7 MEM_A_DQ<33> — 14C7 74D3 MEM_A_DQ<36>
74C3 14B5 MEM_A_DQS_N<4> — 14B7 74C3 MEM_A_DM<4>
74C3 14B5 MEM_A_DQS_P<4>
74D3 14C7 MEM_A_DQ<34> — 14C7 74D3 MEM_A_DQ<35>
74D3 14C7 MEM_A_DQ<38> — 14C7 74D3 MEM_A_DQ<39>
74D3 14C7 MEM_A_DQ<44> — 14C7 74D3 MEM_A_DQ<40>
74D3 14C7 MEM_A_DQ<45> — 14C7 74D3 MEM_A_DQ<41>
74C3 14B7 MEM_A_DM<5>
74D3 14D7 MEM_A_DQ<47> — 14C7 74D3 MEM_A_DQ<43>
74D3 14D7 MEM_A_DQ<46> — 14C7 74D3 MEM_A_DQ<42>
74D3 14D7 MEM_A_DQ<49> — 14D7 74D3 MEM_A_DQ<53>
74D3 14D7 MEM_A_DQ<52> — 14D7 74D3 MEM_A_DQ<48>
74C3 14D5 MEM_A_DQS_N<6> — 14B7 74C3 MEM_A_DM<6>
74C3 14D5 MEM_A_DQS_P<6>
74D3 14D7 MEM_A_DQ<54> — 14D7 74D3 MEM_A_DQ<55>
74D3 14D7 MEM_A_DQ<51> — 14D7 74D3 MEM_A_DQ<50>
74D3 14D7 MEM_A_DQ<61> — 14D7 74D3 MEM_A_DQ<57>
74D3 14D7 MEM_A_DQ<60> — 14D7 74D3 MEM_A_DQ<56>
74C3 14B7 MEM_A_DM<7> — 14D5 74C3 MEM_A_DQS_N<7>
14D5 74C3 MEM_A_DQS_P<7>
74D3 14D7 MEM_A_DQ<58> — 14D7 74D3 MEM_A_DQ<62>
74D3 14D7 MEM_A_DQ<59> — 14D7 74D3 MEM_A_DQ<63>
MEM_A_SA<0>
MEM_A_SA<1>
MEM_EVENT_L — 20A4 20B3 27A5 40B8
=I2C_SODIMMA_SDA — 43D6
=I2C_SODIMMA_SCL — 43D6

7C5 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

			1	VREFDQ	VSS	2	
			3	VSS	DQ4	4	MEM_A_DQ<4>
74D3 14B7	B1	MEM_A_DQ<0>	5	DQ0	DQ5	6	MEM_A_DQ<5>
74D3 14B7	B1	MEM_A_DQ<1>	7	DQ1	VSS	8	
			9	VSS	DQS0*	10	MEM_A_DQS_N<0>
74D3 14A7	IN	MEM_A_DM<0>	11	DM0	DQS0	12	MEM_A_DQS_P<0>
			13	VSS	VSS	14	
74D3 14B7	B1	MEM_A_DQ<6>	15	DQ2	DQ6	16	MEM_A_DQ<3>
74D3 14B7	B1	MEM_A_DQ<7>	17	DQ3	DQ7	18	MEM_A_DQ<2>
			19	VSS	VSS	20	
74D3 14B7	B1	MEM_A_DQ<8>	21	DQ8	DQ12	22	MEM_A_DQ<9>
74D3 14B7	B1	MEM_A_DQ<12>	23	DQ9	DQ13	24	MEM_A_DQ<13>
			25	VSS	VSS	26	
74C3 14D5	B1	MEM_A_DQS_N<1>	27	DQS1*	DM1	28	MEM_A_DM<1>
74C3 14D5	B1	MEM_A_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L
			31	VSS	VSS	32	
74D3 14B7	B1	MEM_A_DQ<10>	33	DQ10	DQ14	34	MEM_A_DQ<11>
74D3 14B7	B1	MEM_A_DQ<15>	35	DQ11	DQ15	36	MEM_A_DQ<14>
			37	VSS	VSS	38	
74D3 14C7	B1	MEM_A_DQ<25>	39	DQ16	DQ20	40	MEM_A_DQ<29>
74D3 14C7	B1	MEM_A_DQ<24>	41	DQ17	DQ21	42	MEM_A_DQ<28>
			43	VSS	VSS	44	
74C3 14D5	B1	MEM_A_DQS_N<3>	45	DQS2*	DM2	46	MEM_A_DM<3>
74C3 14D5	B1	MEM_A_DQS_P<3>	47	DQS2	VSS	48	
			49	VSS	DQ22	50	MEM_A_DQ<27>
74D3 14C7	B1	MEM_A_DQ<26>	51	DQ18	DQ23	52	MEM_A_DQ<31>
74D3 14C7	B1	MEM_A_DQ<30>	53	DQ19	VSS	54	
			55	VSS	DQ28	56	MEM_A_DQ<18>
74D3 14C7	B1	MEM_A_DQ<20>	57	DQ24	DQ29	58	MEM_A_DQ<17>
74D3 14C7	B1	MEM_A_DQ<21>	59	DQ25	VSS	60	
			61	VSS	DQS3*	62	MEM_A_DQS_N<2>
74C3 14B7	IN	MEM_A_DM<2>	63	DM3	DQS3	64	MEM_A_DQS_P<2>
			65	VSS	VSS	66	
74D3 14C7	B1	MEM_A_DQ<23>	67	DQ26	DQ30	68	MEM_A_DQ<19>
74D3 14B7	B1	MEM_A_DQ<16>	69	DQ27	DQ31	70	MEM_A_DQ<22>
			71	VSS	VSS	72	

CRITICAL
J3100 F-RT-THB DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
KEY
516-0201

74D3 14B7 MEM_A_DQ<0> — 14B7 74D3 MEM_A_DQ<4>
74D3 14B7 MEM_A_DQ<1> — 14B7 74D3 MEM_A_DQ<5>
74D3 14A7 MEM_A_DM<0> — 14D5 74C3 MEM_A_DQS_N<0>
14D5 74C3 MEM_A_DQS_P<0>
74D3 14B7 MEM_A_DQ<6> — 14B7 74D3 MEM_A_DQ<3>
74D3 14B7 MEM_A_DQ<7> — 14B7 74D3 MEM_A_DQ<2>
74D3 14B7 MEM_A_DQ<8> — 14B7 74D3 MEM_A_DQ<9>
74D3 14B7 MEM_A_DQ<12> — 14B7 74D3 MEM_A_DQ<13>
74C3 14D5 MEM_A_DQS_N<1> — 14A7 74C3 MEM_A_DM<1>
74C3 14D5 MEM_A_DQS_P<1> — 27C2 28C5 MEM_RESET_L
74D3 14B7 MEM_A_DQ<10> — 14B7 74D3 MEM_A_DQ<11>
74D3 14B7 MEM_A_DQ<15> — 14B7 74D3 MEM_A_DQ<14>
74D3 14C7 MEM_A_DQ<25> — 14C7 74D3 MEM_A_DQ<29>
74D3 14C7 MEM_A_DQ<24> — 14C7 74D3 MEM_A_DQ<28>
74C3 14D5 MEM_A_DQS_N<3> — 14A7 74C3 MEM_A_DM<3>
74C3 14D5 MEM_A_DQS_P<3>
74D3 14C7 MEM_A_DQ<26> — 14C7 74D3 MEM_A_DQ<27>
74D3 14C7 MEM_A_DQ<30> — 14C7 74D3 MEM_A_DQ<31>
74D3 14C7 MEM_A_DQ<20> — 14B7 74D3 MEM_A_DQ<18>
74D3 14C7 MEM_A_DQ<21> — 14B7 74D3 MEM_A_DQ<17>
74C3 14B7 MEM_A_DM<2> — 14D5 74C3 MEM_A_DQS_N<2>
14D5 74C3 MEM_A_DQS_P<2>
74D3 14C7 MEM_A_DQ<23> — 14B7 74D3 MEM_A_DQ<19>
74D3 14B7 MEM_A_DQ<16> — 14C7 74D3 MEM_A_DQ<22>

PP0V75_S3_MEM_VREFCA_A — 25C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

=PP0V75_S0_MEM_VTT_A — 7C7

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

"Factory" (top) slot

SYNC MASTER=BEN SYNC DATE=06/30/2008
PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 31 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

7D3 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3211 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3212 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3213 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3214 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3215 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3216 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3217 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25C1 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

74B3 14A1 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 14A1 74B3
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 8D2
74B3 14C1 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 14C1 74B3
		81	VDD	VDD	82		
74B3 14C1 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 14C1 74B3
74B3 14C1 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 14C1 74B3
		87	VDD	VDD	88		
74B3 14C1 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 14B1 74B3
74B3 14B1 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 14B1 74B3
		93	VDD	VDD	94		
74B3 14B1 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 14B1 74B3
74B3 14B1 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 14B1 74B3
		99	VDD	VDD	100		
74C3 14B1 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 14B1 74C3
74C3 14B1 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 14B1 74C3
		105	VDD	VDD	106		
74B3 14C1 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 14C1 74B3
74B3 14C1 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 14C1 74B3
		111	VDD	VDD	112		
74B3 14C1 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 14B1 74B3
74B3 14C1 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 14B1 74B3
		117	VDD	VDD	118		
74B3 14C1 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 14B1 74B3
74B3 14B1 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
74B3 14C2 BI	MEM_B_DQ<37>	129	DQ32	DQ36	130	MEM_B_DQ<36>	BI 14C3 74B3
74B3 14C2 BI	MEM_B_DQ<32>	131	DQ33	DQ37	132	MEM_B_DQ<33>	BI 14C3 74B3
		133	VSS	VSS	134		
74A3 14D1 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 14B3 74B3
74A3 14D1 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 14C3 74B3
74B3 14C2 BI	MEM_B_DQ<35>	141	DQ34	DQ39	142	MEM_B_DQ<34>	BI 14C3 74B3
74B3 14C2 BI	MEM_B_DQ<39>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<40>	BI 14C3 74B3
74B3 14C2 BI	MEM_B_DQ<45>	147	DQ40	DQ45	148	MEM_B_DQ<44>	BI 14C3 74B3
74B3 14C2 BI	MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 14D1 74A3
74B3 14B3 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 14D1 74A3
		155	VSS	VSS	156		
74B3 14D2 BI	MEM_B_DQ<46>	157	DQ42	DQ46	158	MEM_B_DQ<42>	BI 14C3 74B3
74B3 14D2 BI	MEM_B_DQ<47>	159	DQ43	DQ47	160	MEM_B_DQ<43>	BI 14C3 74B3
		161	VSS	VSS	162		
74B3 14D2 BI	MEM_B_DQ<53>	163	DQ48	DQ52	164	MEM_B_DQ<52>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<48>	BI 14D3 74B3
		167	VSS	VSS	168		
74A3 14D1 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 14B3 74B3
74A3 14D1 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<51>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<55>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<63>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<59>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<58>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 14D1 74A3
74B3 14B3 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 14D1 74A3
		189	VSS	VSS	190		
74B3 14D2 BI	MEM_B_DQ<61>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<60>	193	DQ59	DQ63	194	MEM_B_DQ<57>	BI 14D3 74B3
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 20A4 20B3 26A5 40B8
7C5 =PPSPD_S0_MEM_B		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 43C6
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 43C6
		203	VTT	VTT	204		=PP0V75_S0_MEM_VTT_B 7C7
		MTG PINS					
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

PP0V75_S3_MEM_VREFCA_B 25C1

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	MEM_B_DQ<4>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<0>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 14D1 74A3
74B3 14A3 IN	MEM_B_DM<0>	11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 14D1 74A3
		13	VSS	VSS	14		
74B3 14B3 BI	MEM_B_DQ<3>	15	DQ2	DQ6	16	MEM_B_DQ<7>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<6>	17	DQ3	DQ7	18	MEM_B_DQ<2>	BI 14B3 74B3
		19	VSS	VSS	20		
74B3 14B3 BI	MEM_B_DQ<13>	21	DQ8	DQ12	22	MEM_B_DQ<12>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<14>	23	DQ9	DQ13	24	MEM_B_DQ<9>	BI 14B3 74B3
		25	VSS	VSS	26		
74A3 14D1 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28	MEM_B_DM<1>	IN 14A3 74B3
74A3 14D1 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 26C2 28C5
		31	VSS	VSS	32		
74B3 14B3 BI	MEM_B_DQ<15>	33	DQ10	DQ14	34	MEM_B_DQ<8>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<10>	35	DQ11	DQ15	36	MEM_B_DQ<11>	BI 14B3 74B3
		37	VSS	VSS	38		
74B3 14C3 BI	MEM_B_DQ<20>	39	DQ16	DQ20	40	MEM_B_DQ<16>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<17>	41	DQ17	DQ21	42	MEM_B_DQ<21>	BI 14C3 74B3
		43	VSS	VSS	44		
74A3 14D1 BI	MEM_B_DQS_N<2>	45	DQS2*	DM2	46	MEM_B_DM<2>	IN 14B3 74B3
74A3 14D1 BI	MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<18>	BI 14B3 74B3
74B3 14C3 BI	MEM_B_DQ<22>	51	DQ18	DQ23	52	MEM_B_DQ<23>	BI 14C3 74B3
74B3 14B3 BI	MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<29>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<24>	57	DQ24	DQ29	58	MEM_B_DQ<25>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<28>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<3>	BI 14D1 74A3
74B3 14B3 IN	MEM_B_DM<3>	63	DM3	DQS3	64	MEM_B_DQS_P<3>	BI 14D1 74A3
		65	VSS	VSS	66		
74B3 14C3 BI	MEM_B_DQ<26>	67	DQ26	DQ30	68	MEM_B_DQ<30>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<31>	69	DQ27	DQ31	70	MEM_B_DQ<27>	BI 14C3 74B3
		71	VSS	VSS	72		

516S0706

DDR3 GROUND RETURN CAPS (MCP SIDE)

7B6 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3223 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3224 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3225 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3226 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3227 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3228 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3229 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

"Expansion" (bottom) slot

SYNC MASTER=BEN SYNC DATE=05/09/2008
PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
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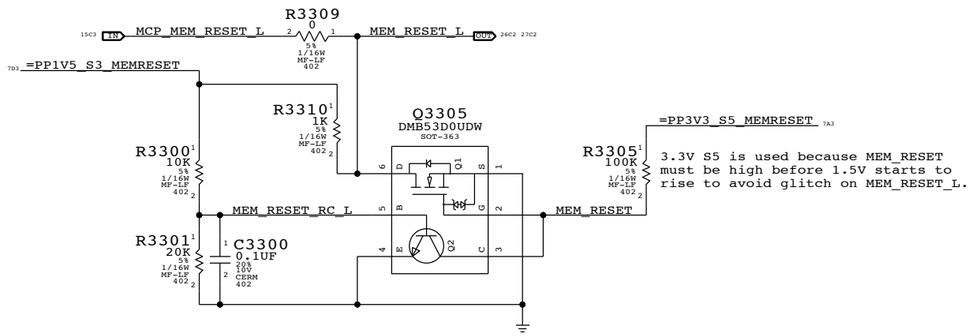
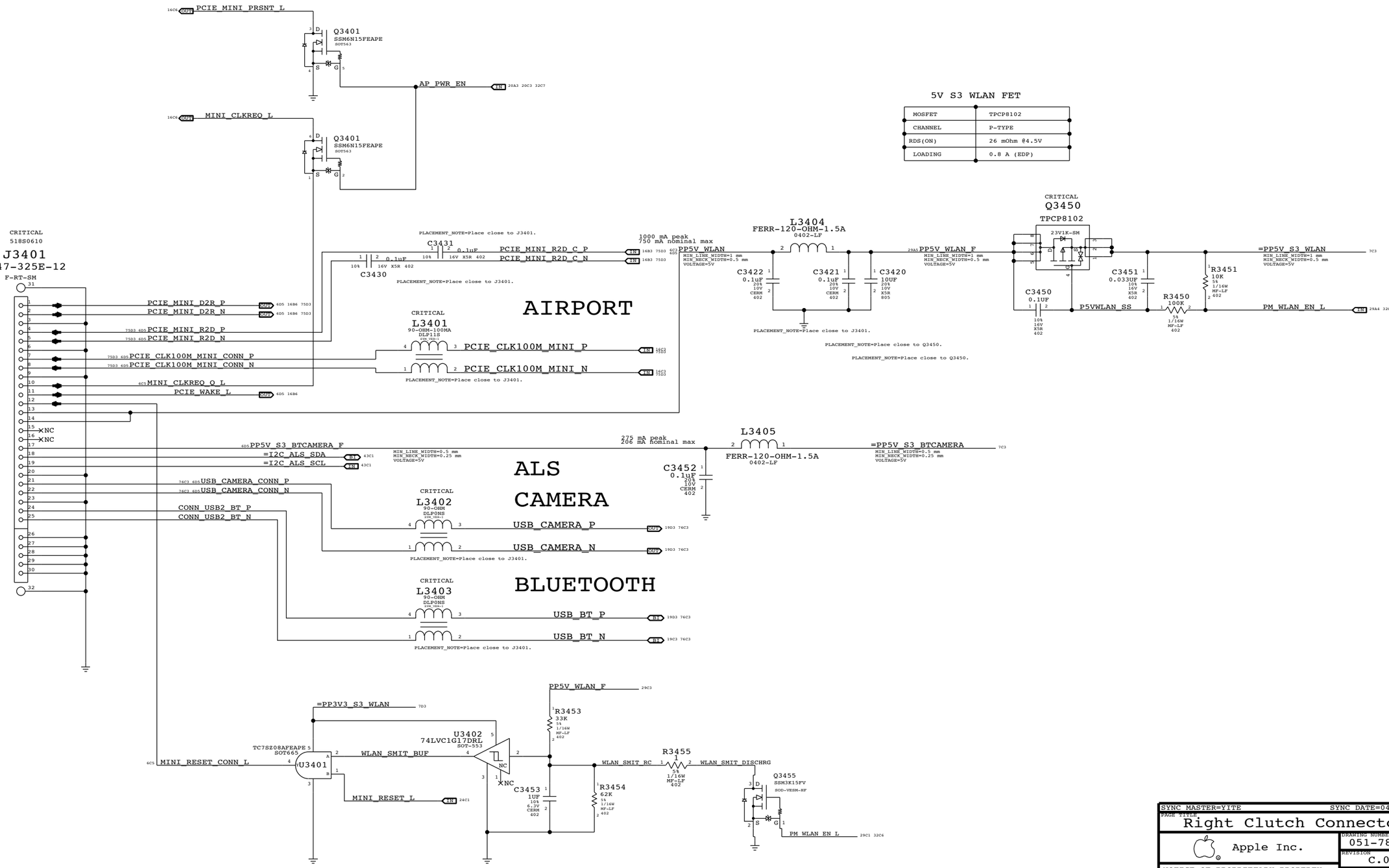
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC MASTER=T18 MLB	SYNC DATE=04/04/2008
PAGE TITLE: DDR3 Support	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 33 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=YITE	SYNC DATE=04/22/2008
PAGE TITLE	Right Clutch Connector
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
	BRANCH
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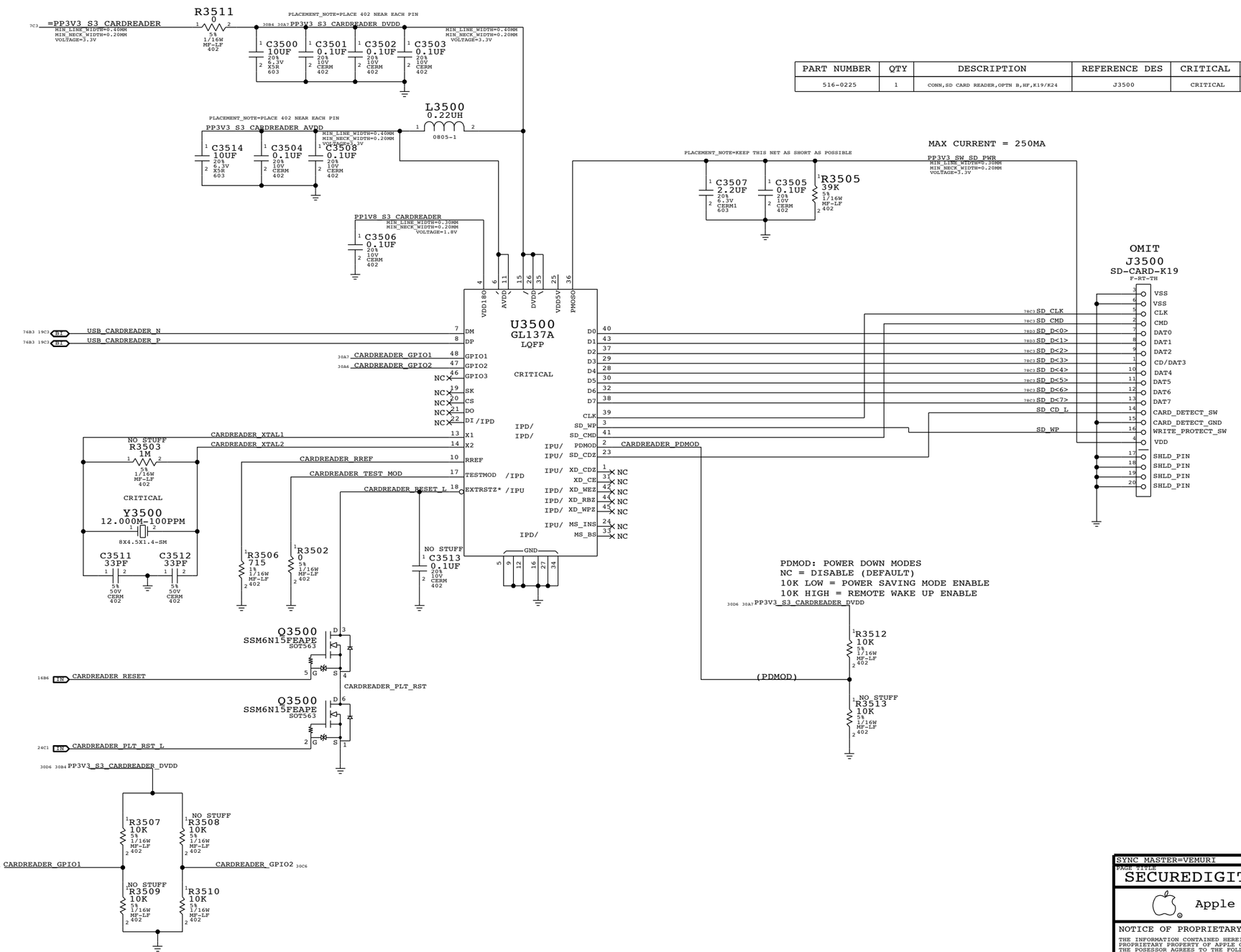
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,K19/K24	J3500	CRITICAL	



SYNC MASTER=VEMURI SYNC DATE=01/30/2009

PAGE TITLE

SECUREDIGITAL CARD READER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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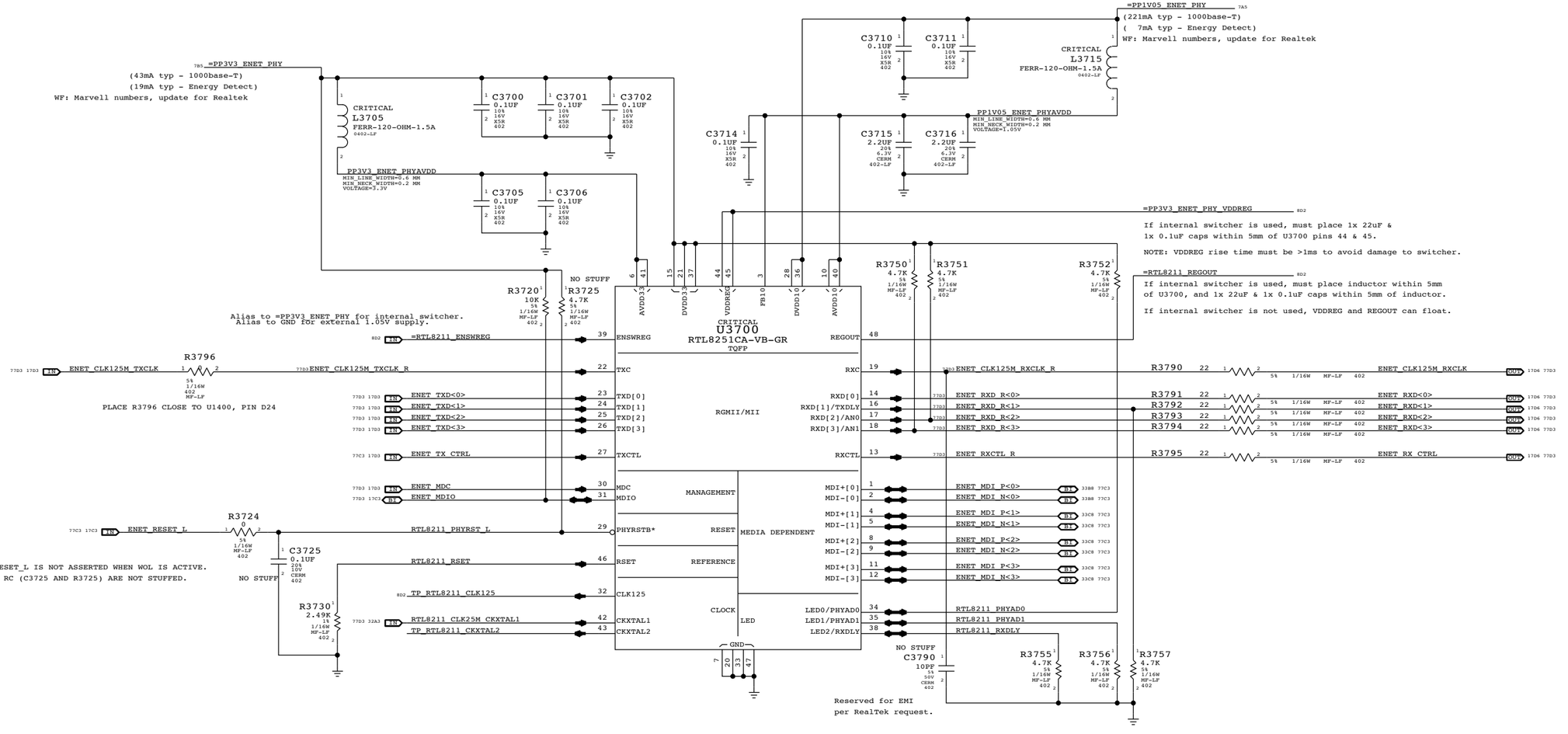
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=SUMA SYNC DATE=05/23/2008

PAGE TITLE
Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
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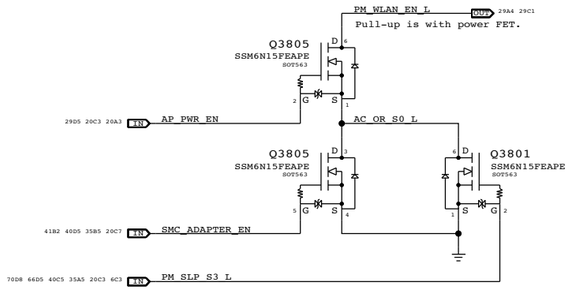
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

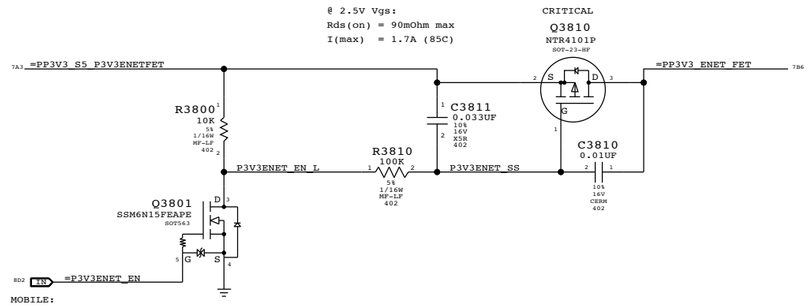
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL



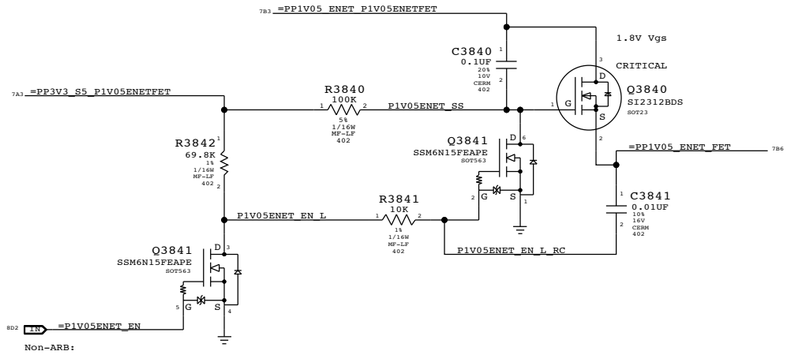
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

1.8V Vgs

CRITICAL



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PLACEMENT_NOTE=Place close to U1400

SYNC MASTER=SUMA SYNC DATE=07/01/2008

PAGE TITLE

Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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SHEET

<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-M97-3
F-RT-TH

514-0636

CRITICAL
T3901
SM
TX
RX
TLA-6T213HF

CRITICAL
T3902
SM
TX
RX
TLA-6T213HF

77C3 31B3 BI ENET_MDI_P<1>
77C3 31B3 BI ENET_MDI_N<1>
77C3 31B3 BI ENET_MDI_P<3>
77C3 31B3 BI ENET_MDI_N<3>
77C3 31B3 BI ENET_MDI_N<2>
77C3 31B3 BI ENET_MDI_P<2>
77C3 31B3 BI ENET_MDI_N<0>
77C3 31B3 BI ENET_MDI_P<0>

77C3 ENET_MDI_TRAN_P<1>
77C3 ENET_MDI_TRAN_N<1>
77C3 ENET_MDI_TRAN_P<3>
77C3 ENET_MDI_TRAN_N<3>
77C3 ENET_MDI_TRAN_N<2>
77C3 ENET_MDI_TRAN_P<2>
77C3 ENET_MDI_TRAN_N<0>
77C3 ENET_MDI_TRAN_P<0>

ENET_CENTER_TAP<1>
ENET_CENTER_TAP<3>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<0>

R3903 75 1% 1/16W MF-LF 402
R3902 75 1% 1/16W MF-LF 402
R3901 75 1% 1/16W MF-LF 402
R3900 75 1% 1/16W MF-LF 402

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

C3911 10PF 5% 50V CERM 402-1 CRITICAL
C3912 10PF 5% 50V CERM 402-1 CRITICAL
C3913 10PF 5% 50V CERM 402-1 CRITICAL
C3914 10PF 5% 50V CERM 402-1 CRITICAL
C3915 10PF 5% 50V CERM 402-1 CRITICAL
C3916 10PF 5% 50V CERM 402-1 CRITICAL
C3917 10PF 5% 50V CERM 402-1 CRITICAL
C3918 10PF 5% 50V CERM 402-1 CRITICAL

PLACEMENT_NOTE=PLACE C3911-C3918 ON MDI LINES WITHOUT ANY STUBS

SYNC MASTER=SUMA SYNC DATE=04/04/2008

PAGE TITLE: ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 39 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	

OMIT
R4100
0
5%
1/16W
MF-LF
402

35D3 7A1 =PP1V0_FW_FWPHY
135 mA
PP1V0_FW_R

L4110
120-OHM-0.3A-EMI
0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402

=PP3V3_FW_FWPHY
7B1 34B1 35D8 36B6 36D5
138 mA

114 mA FireWire PHY
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

L4130
120-OHM-0.3A-EMI
0402-LF

17 mA PCIe SerDes
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

L4135
120-OHM-0.3A-EMI
0402-LF

0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

CRITICAL
U4100
FW643E
BGA

NC ATBUSB
NC ATBUSH
NC ATBUSN
36D2 =FW_PHY_DS0 DS0 (IPD) NT-19
36D2 =FW_PHY_DS1 DS1 (IPD) NT-20
36D2 =FW_PHY_DS2 DS2 (IPD) NT-21

78D3 36C4 FW_P0_TPA_N TPA0N
78D3 36C4 FW_P0_TPA_P TPA0P
78D3 36B6 FW_P1_TPA_N TPA1N
78D3 36B6 FW_P1_TPA_P TPA1P
36C4 FW_P2_TPA_N TPA2N
36C4 FW_P2_TPA_P TPA2P
78D3 36C4 FW_P0_TPB_N TPB0N
78D3 36C4 FW_P0_TPB_P TPB0P
78D3 36B6 FW_P1_TPB_N TPB1N
78D3 36B6 FW_P1_TPB_P TPB1P
36C4 FW_P2_TPB_N TPB2N
36C4 FW_P2_TPB_P TPB2P

36D4 FW_P0_TPBIAS TPBIAS0
36C8 35A4 FW_P1_TPBIAS TPBIAS1
36D4 FW_P2_TPBIAS TPBIAS2

FW643_R0 R0
FW643_TPCPS TPCPS

36C4 =PPVP_FW_PHY_CPS
R4160 200K 1% 1/16W MF-LF 402

TP_FW643_NAND_TREE NAND_TREE NT-OUT
FW643_REXT REXT
FW_CLK24P576M_XO_R XO
FW_CLK24P576M_XI XI NT-9

NOTE: NT-xx notes show NAND tree order.

TP_FW643_SE SE (IPD)
TP_FW643_SM SM (IPD)
TP_FW643_MODE_A MODE_A (IPD) NT-18
TP_FW643_CE CE (IPD)
TP_FW643_FW620_L FW620*(IPU)
TP_FW643_JASI_EN JASI_EN (IPD) NT-11
TP_FW643_AVREG AVREG
TP_FW643_VBUF VBUF
FW643_PU_RST_L FW_RESET* (IPU) NT-8

TP_FW643_OCR10_CTL OCR_CTL_V10
NC OCR_CTL_V12 (Reserved)

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150
24.576MHZ
8M-3.2X2.5MM
R4150 412 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

VSS VREG_VSS

MISCELLANEOUS

PCI EXPRESS PHY

PCIE_RXD0N PCIE_FW_R2D_N
PCIE_RXD0P PCIE_FW_R2D_P
PCIE_TXD0N PCIE_FW_D2R_C_N
PCIE_TXD0P PCIE_FW_D2R_C_P
REFCLKN PCIE_CLK100M_FW_N
REFCLKP PCIE_CLK100M_FW_P

PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000

1394 PHY

TEST CONTROLLER
NT-4 (IPU) TCK TP_FW643_TCK
NT-3 (IPU) TDI TP_FW643_TDI
(IPU) TDO TP_FW643_TDO
NT-1 (IPU) TMS TP_FW643_TMS
NT-2 (IPU) TRST* FW643_TRST_L

POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* =FW_PME_L
REGCLT FW643_REGCTL
VAUX_DETECT FW643_VAUX_DETECT
NT-12 (IPD) VAUX_DISABLE TP_FW643_VAUX_ENABLE
NT-13 (OD) CLKREQN =FW_CLKREQ_L

SCIF
NT-16 (IPD) SCIFCLK TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN TP_FW643_SCIFDAIN
NT-17 SCIFDOUT TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL FW643_SCL
NT-6 SDA TP_FW643_SDA

CHIP RESET
NT-5 PERST* FW_RESET_L

=PP3V3_FW_FWPHY
7B1 34D2 35D8 36B6 36D5
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402

SYNC MASTER=K19 MLB	SYNC DATE=11/02/2008
PAGE TITLE	FireWire LLC/PHY (FW643)
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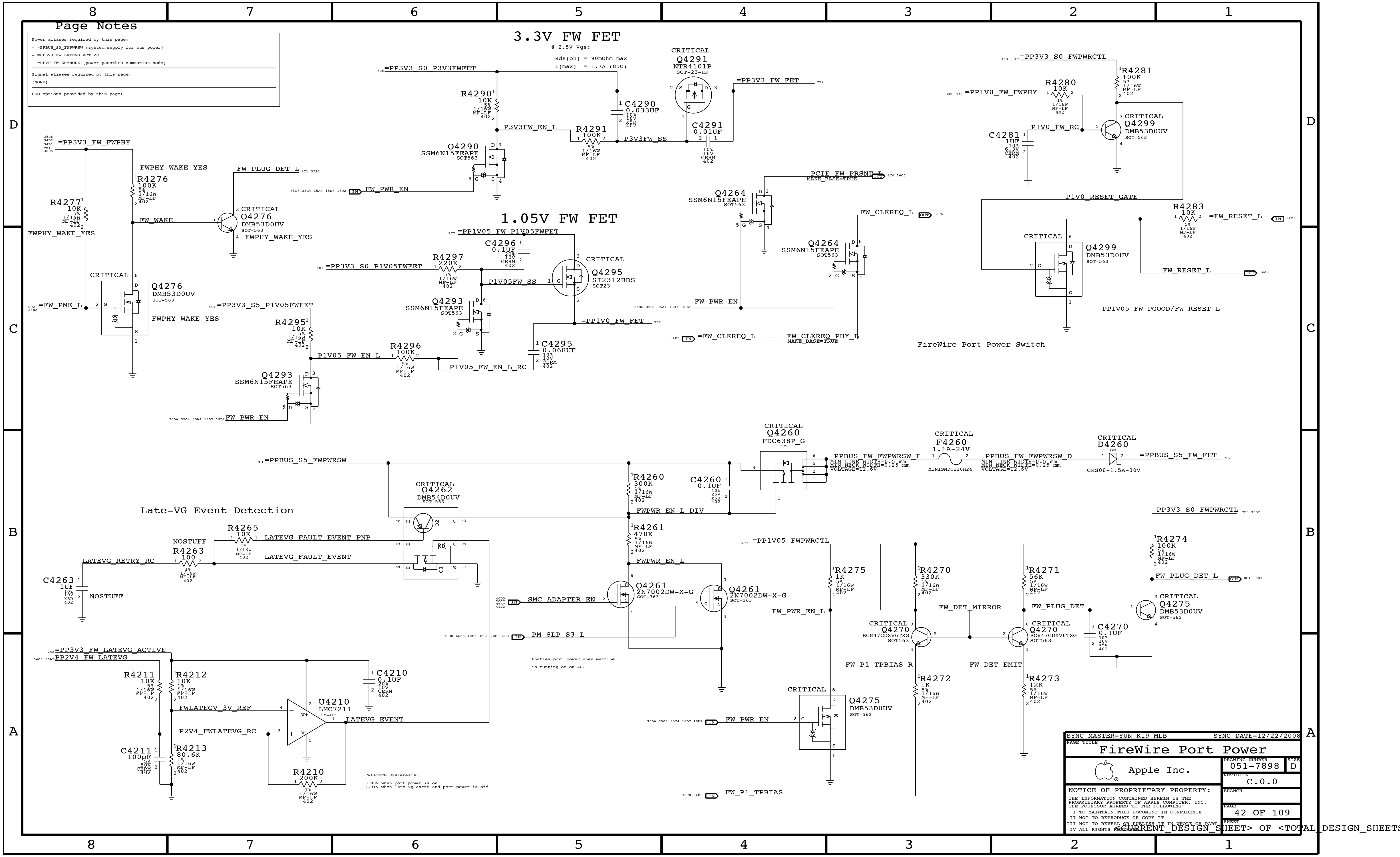
Page Notes
Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
3.3V FW FET
@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)
1.05V FW FET
FireWire Port Power Switch
PP1V05_FW PGOOD/FW_RESET_L
Late-VG Event Detection
Enables port power when machine is running or on AC.
FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off
SYNC_MASTER=YUN_K19_MLB
SYNC_DATE=12/22/2008
FireWire Port Power
Apple Inc.
051-7898
D
C.0.0
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<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

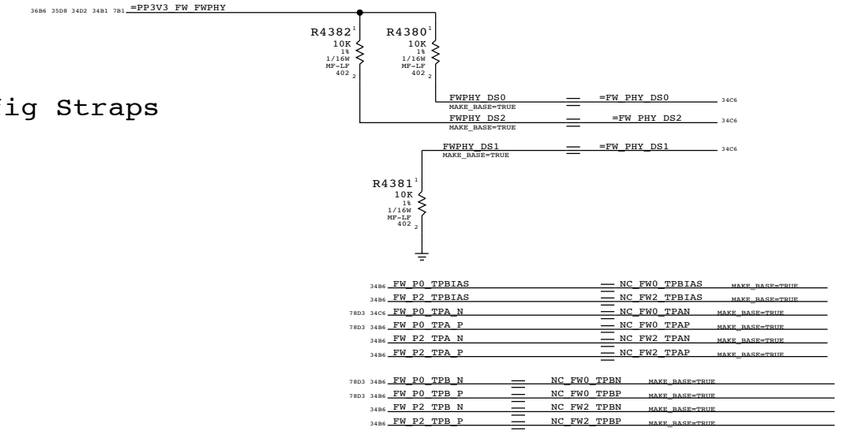
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

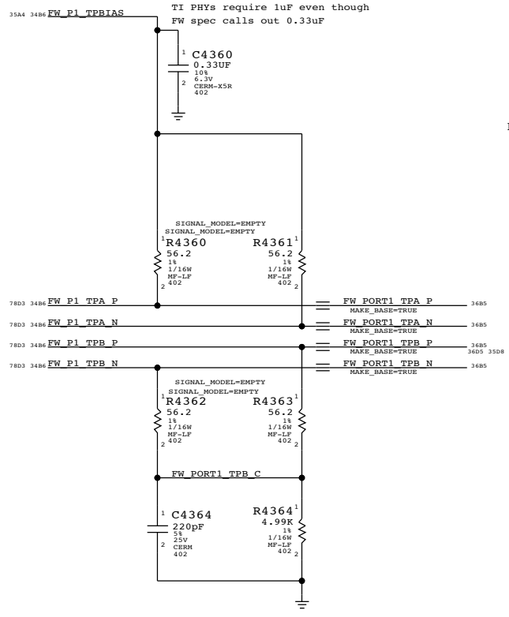
- 1-port Portable Power Class (0)

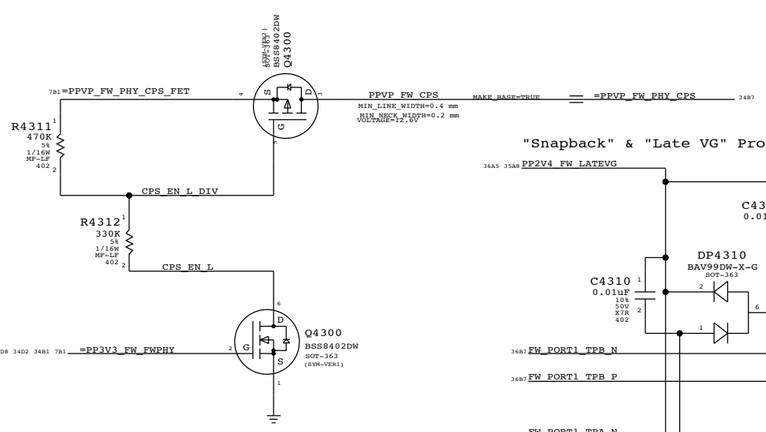
- Port "1" Bilingual (1394B)



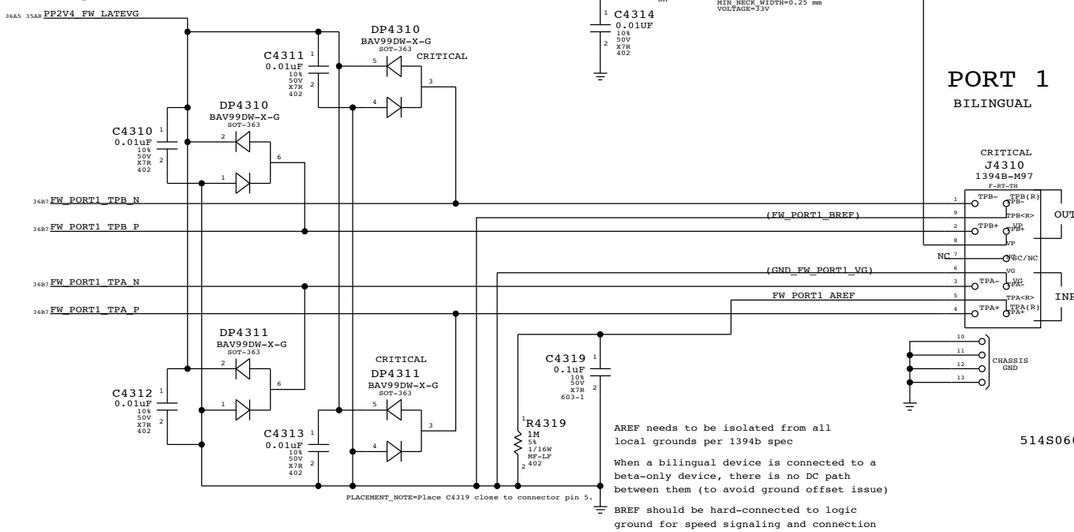
Termination

Place close to FireWire PHY

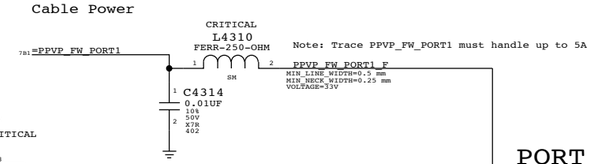




"Snapback" & "Late VG" Protection



Cable Power



PORT 1

BILINGUAL

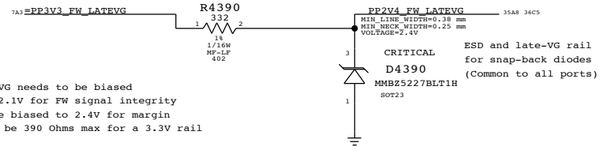
AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

Late-VG Protection Power



PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

SYNC MASTER=K19 MLB SYNC DATE=11/02/2008

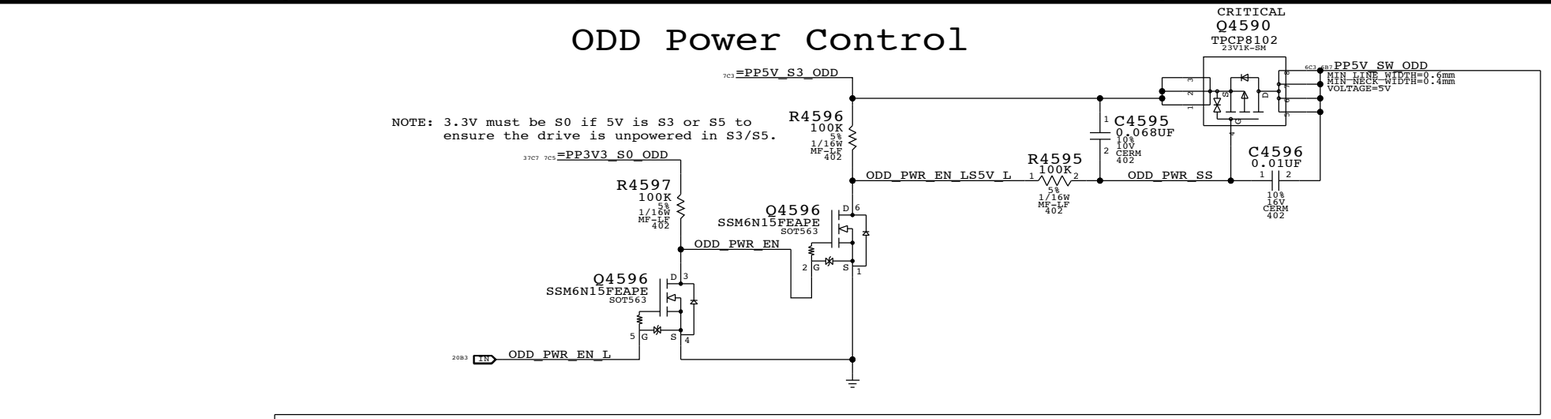
PAGE TITLE: FireWire Ports

Apple Inc.

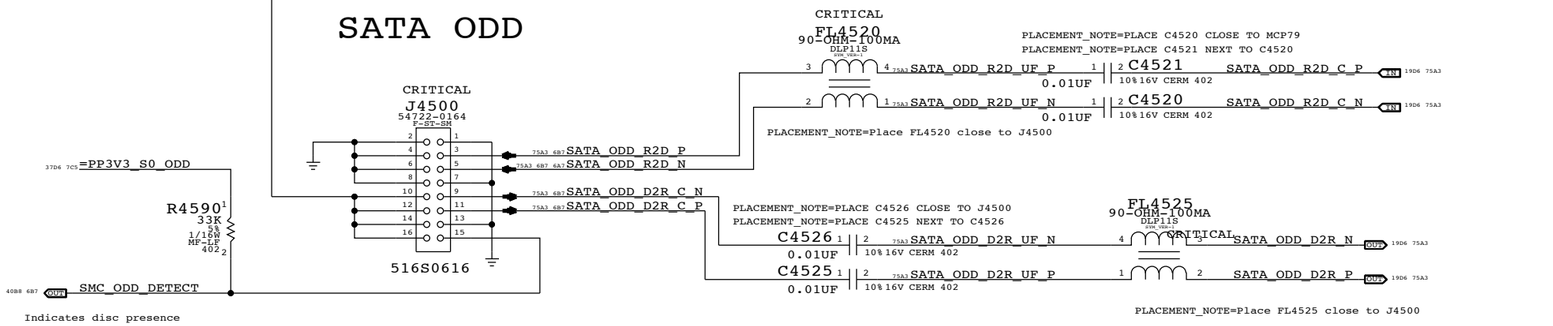
DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 43 OF 109
SHEET:

<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

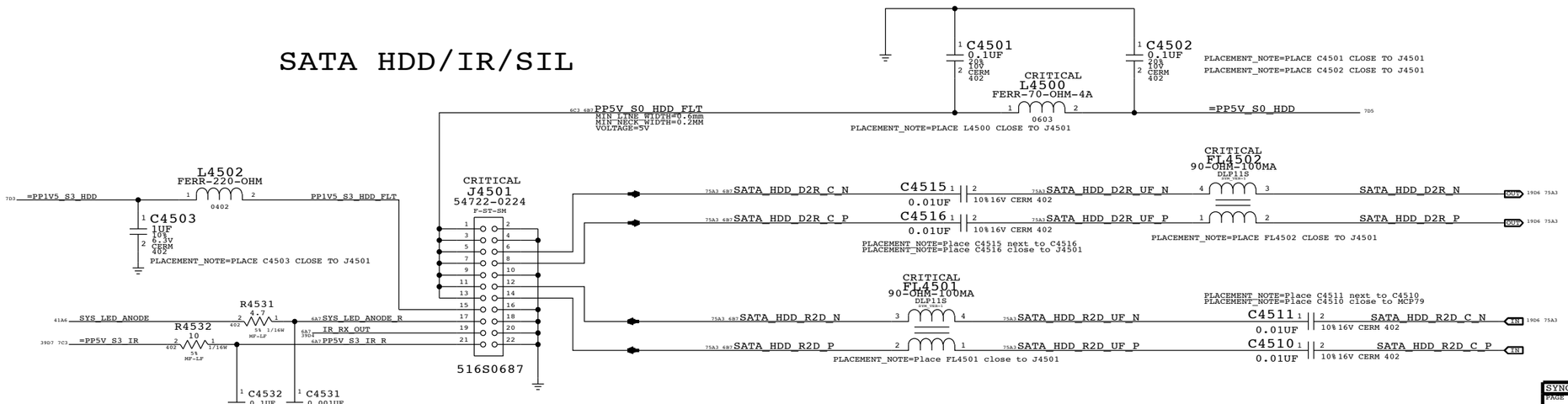
ODD Power Control



SATA ODD



SATA HDD/IR/SIL



SYNC MASTER=K19 MLB SYNC DATE=12/04/2008

PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

BRANCH

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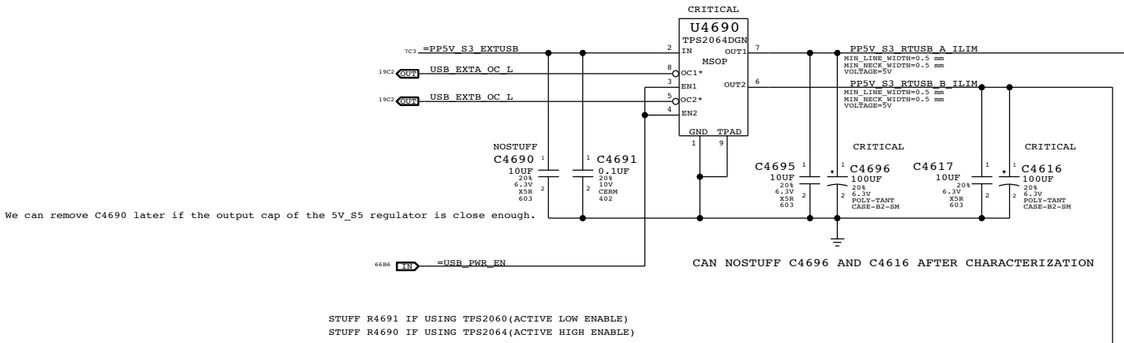
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

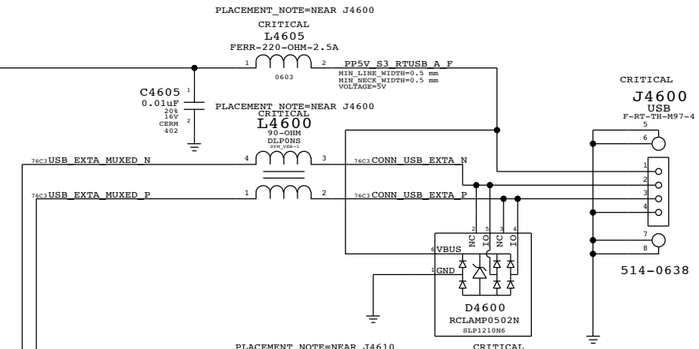
Port Power Switch



We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

STUFF R4691 IF USING TPS2060(ACTIVE LOW ENABLE)
STUFF R4690 IF USING TPS2064(ACTIVE HIGH ENABLE)

USB PORT A (FRONT PORT)

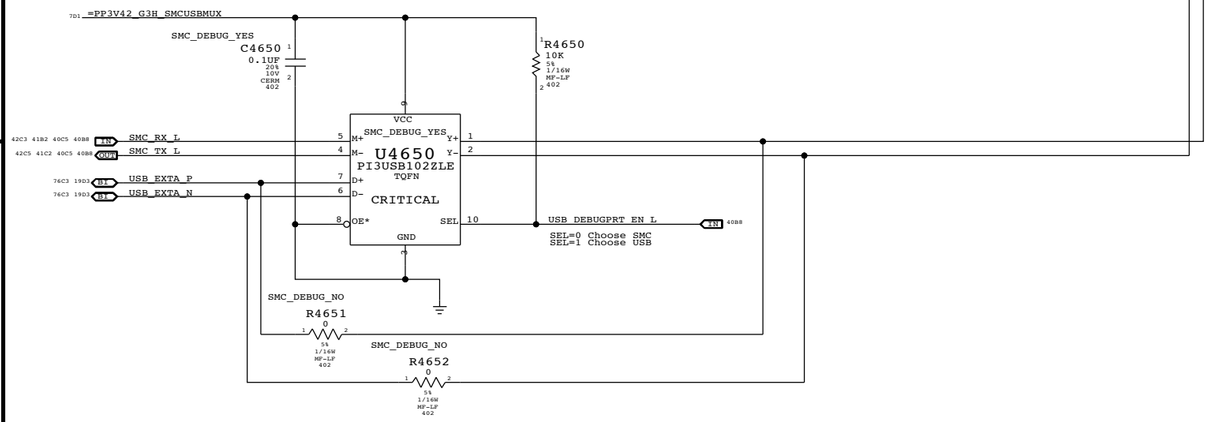


PLACEMENT_NOTE=NEAR J4610
CRITICAL
L4615
FERR-220-OHM-2.5A
0603
C4615
0.01uF
20%
16V
CERM
402
PP5V_S3_RTUSB_B_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

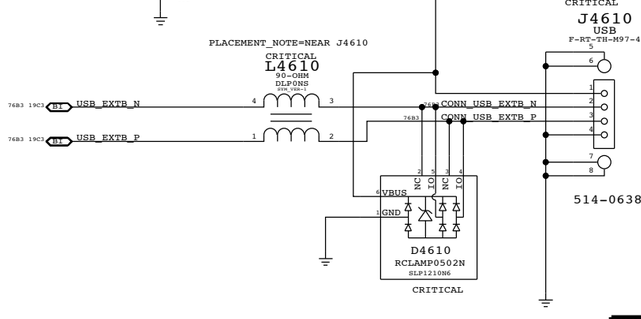
We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

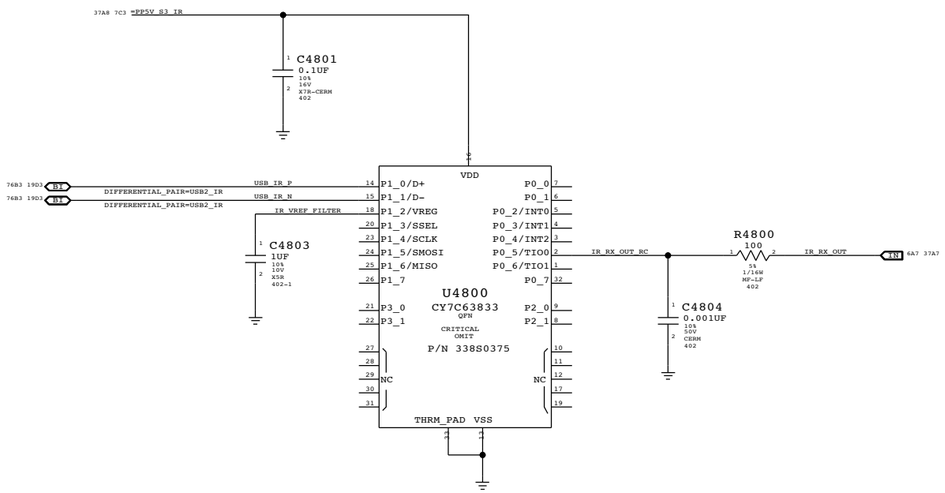
USB/SMC Debug Mux



USB PORT B (BACK PORT)



SYNC MASTER=YUAN.MA	SYNC DATE=01/18/2008
PAGE TITLE: External USB Connectors	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 46 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



CYPRESS 'ENCORE II' USB CONTROLLER

SYNC MASTER=YUAN.MA SYNC DATE=05/28/2008

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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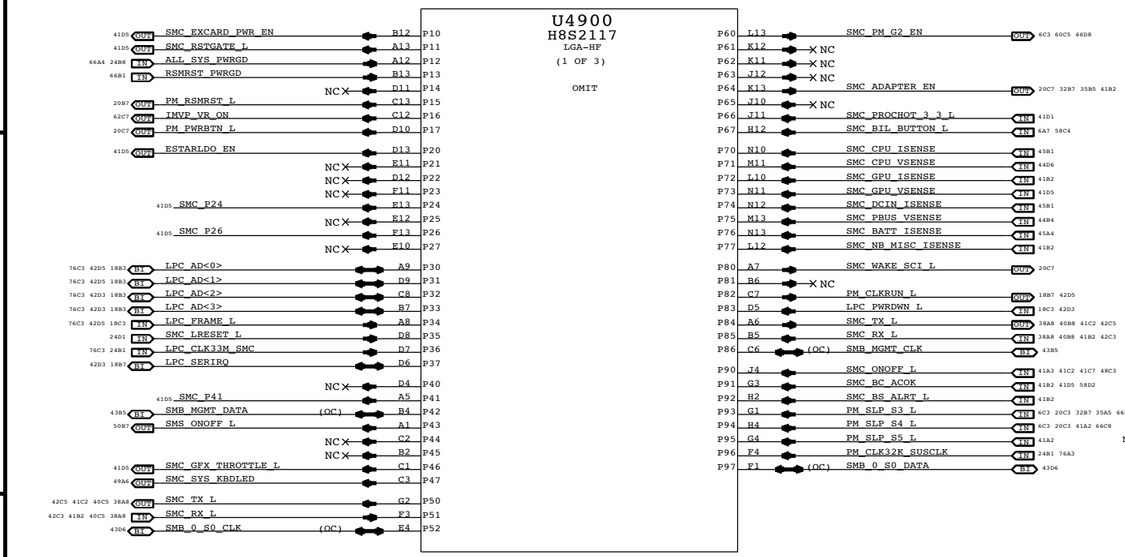
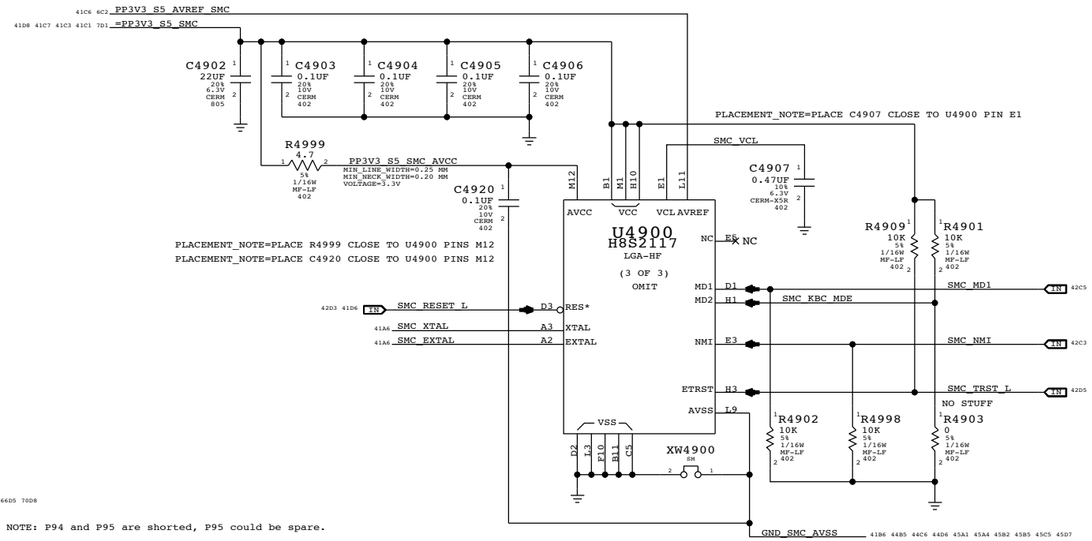
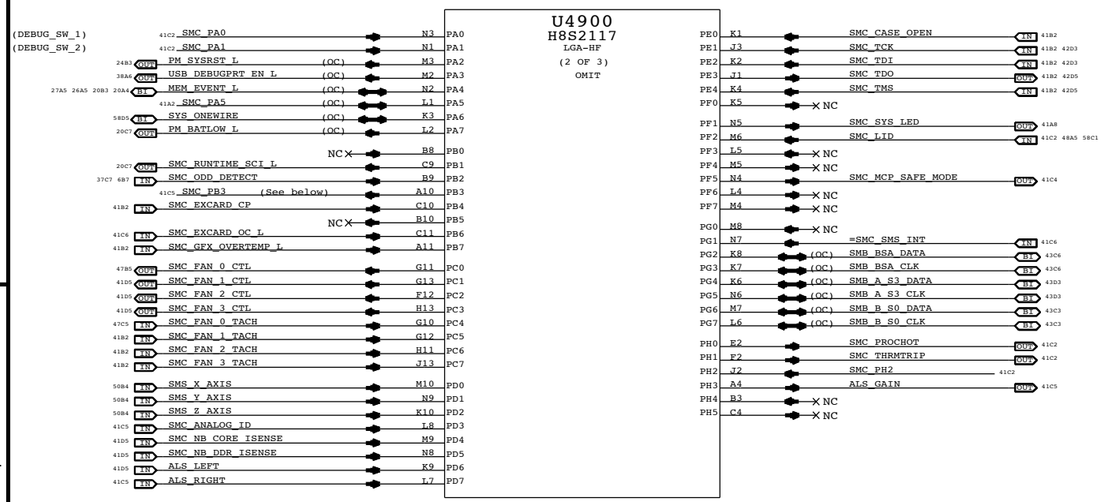
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

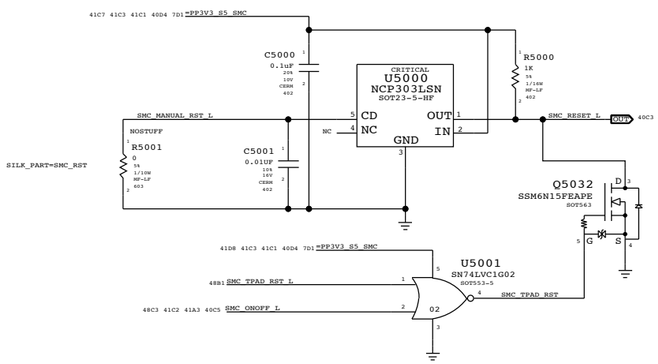
SYNC MASTER=T18_MLB SYNC DATE=06/26/2008

PAGE TITLE: SMC

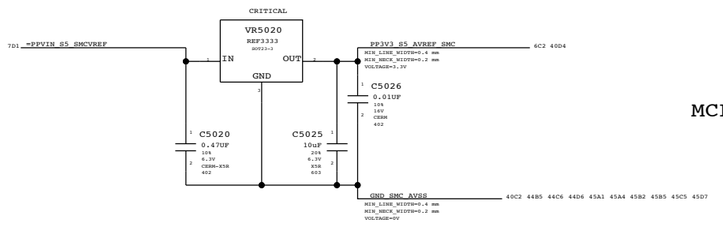
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 49 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SMC Reset "Button" / Brownout Detect

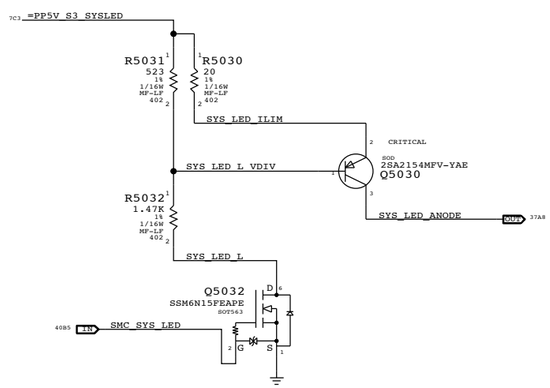


SMC AVREF Supply

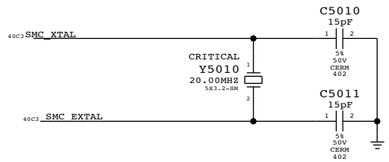


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

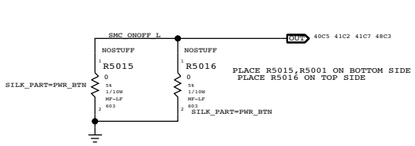
System (Sleep) LED Circuit



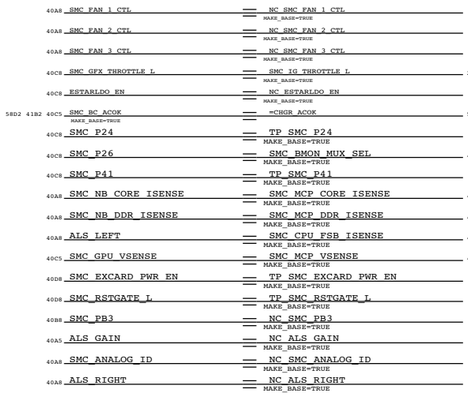
SMC Crystal Circuit



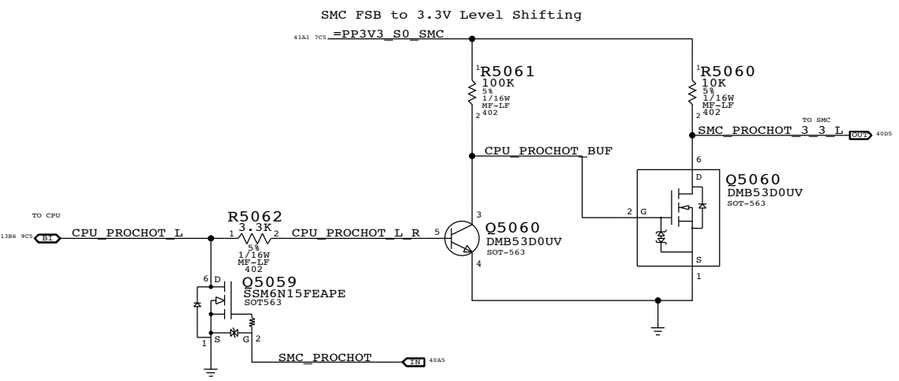
Debug Power "Button"



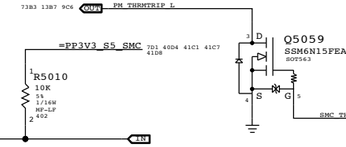
SMC FAN / GFX / BC / P24 / P26 / P41 / NB / GPU / EXCARD / RSTGATE / PB3 / ALS / ANALOG_ID



SMC FSB to 3.3V Level Shifting

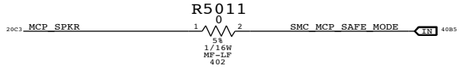


SMC THERMTRIP



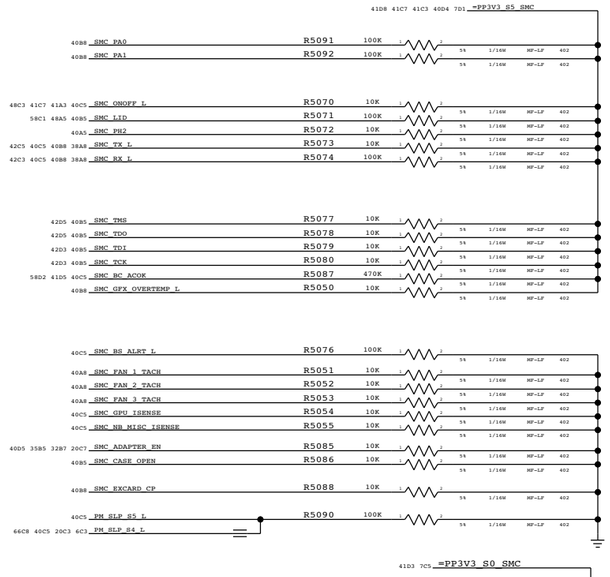
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345



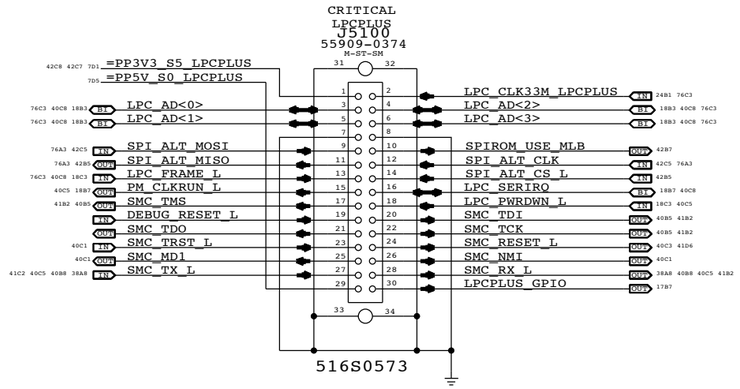
R5095 / R5010 / SMC_SMS_INT

R5091–R5074 / R5077–R5087 / R5076–R5090 / R5089

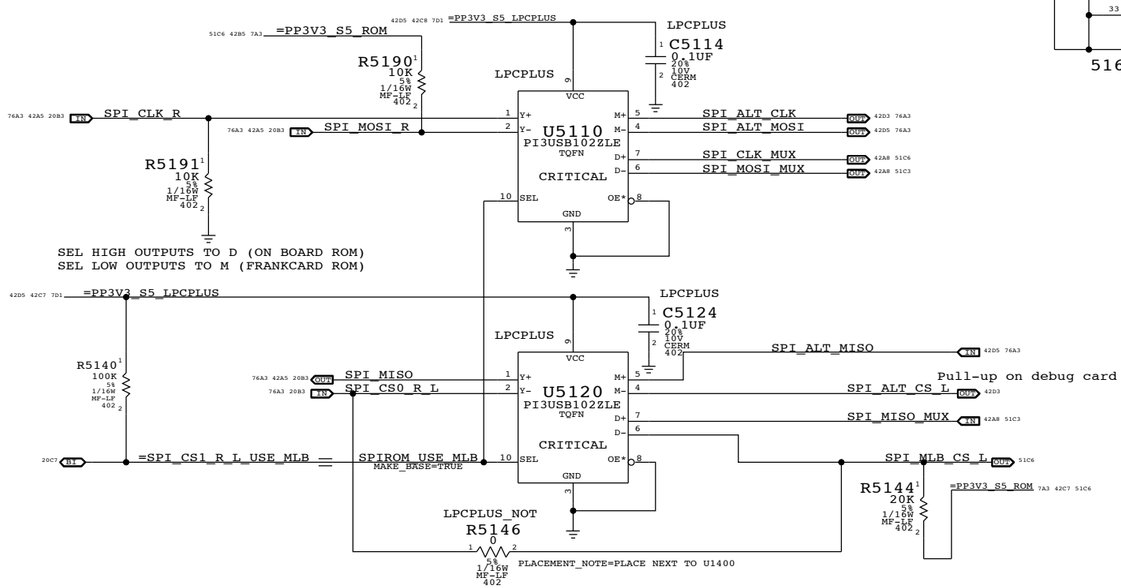


SYNC MASTER=YUAN.MA	SYNC DATE=05/28/2008
PAGE TITLE: SMC Support	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION: C.0.0 BRANCH: PAGE: 50 OF 109 SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

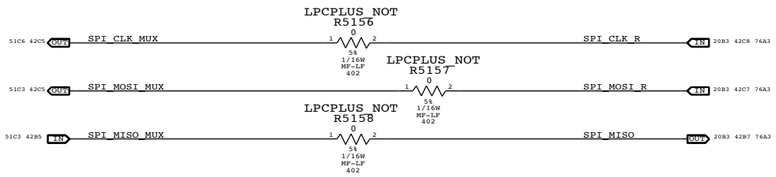
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



SYNC MASTER=CHANGZHANG SYNC DATE=05/09/2008

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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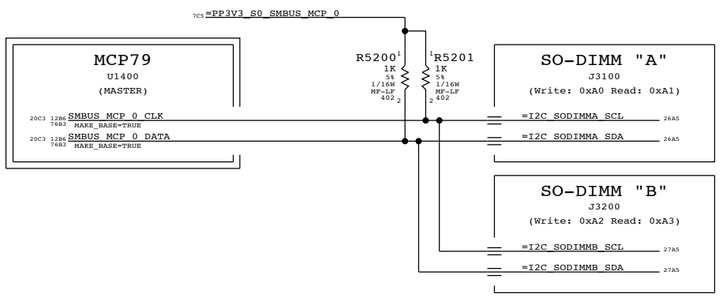
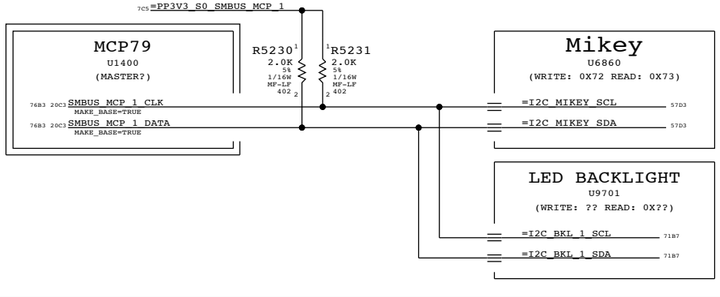
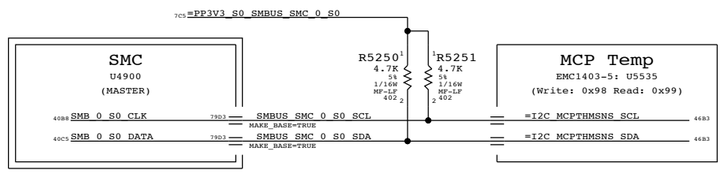
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS

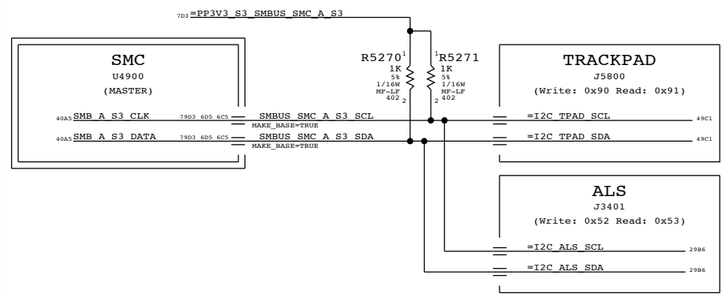


SMC "0" SMBus Connections

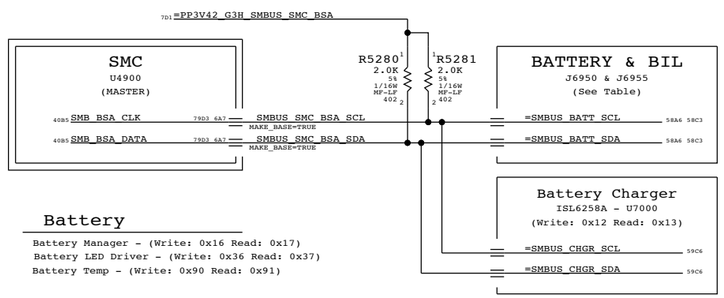


SMC "A" SMBus Connections

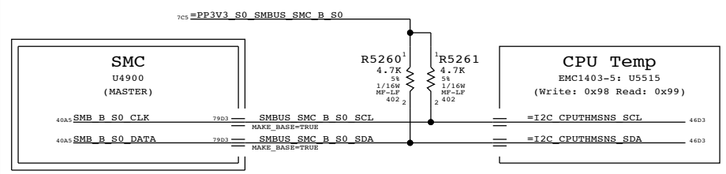
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections

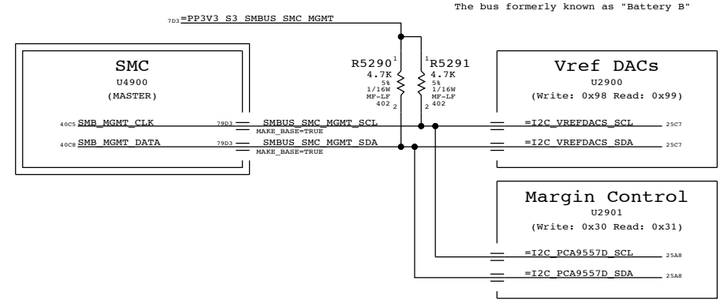


SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SYNC MASTER=BEN SYNC DATE=04/21/2008

PAGE TITLE

K24 SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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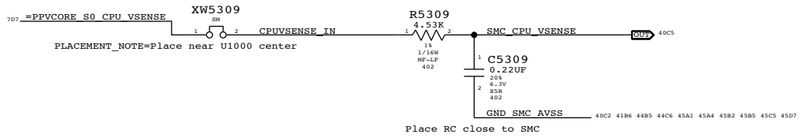
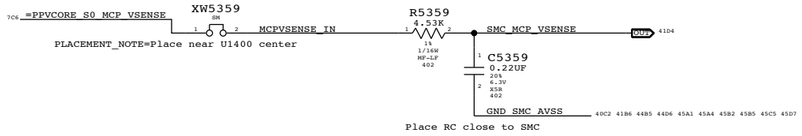
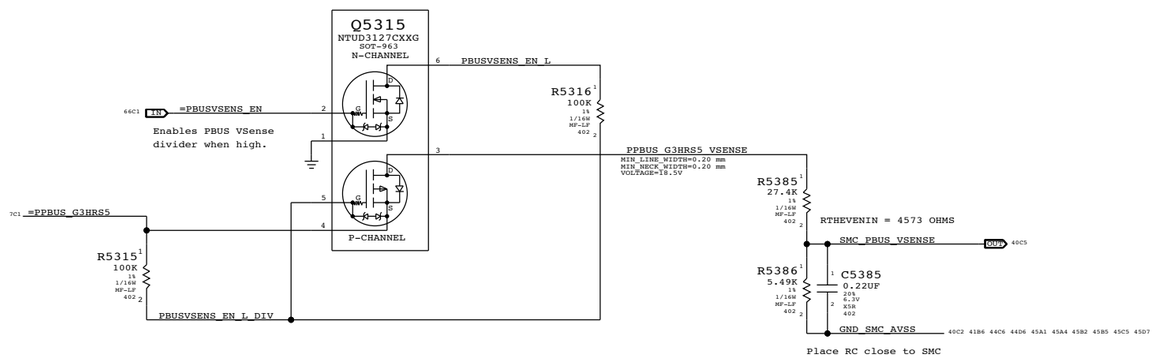
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=YUNWU SYNC DATE=02/04/2008

PAGE TITLE

VOLTAGE SENSING

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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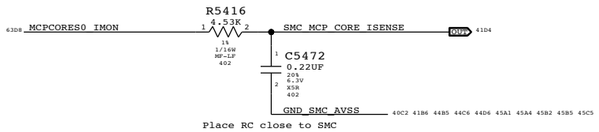
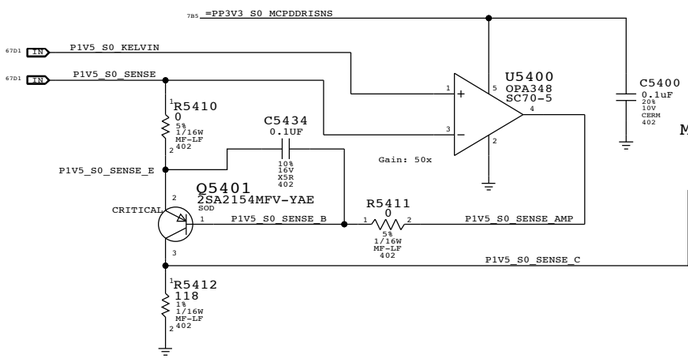
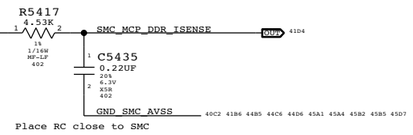
MCP VCore Current Sense Filter



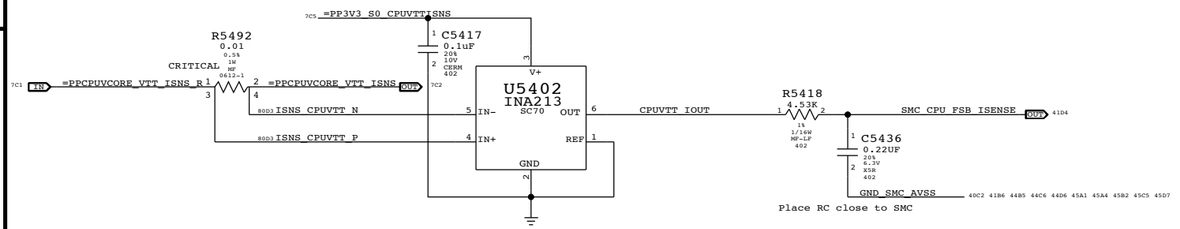
MCP MEM VDD Current Sense



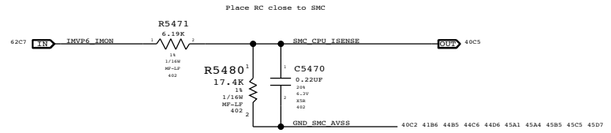
MCP MEM VDD Current Sense Filter



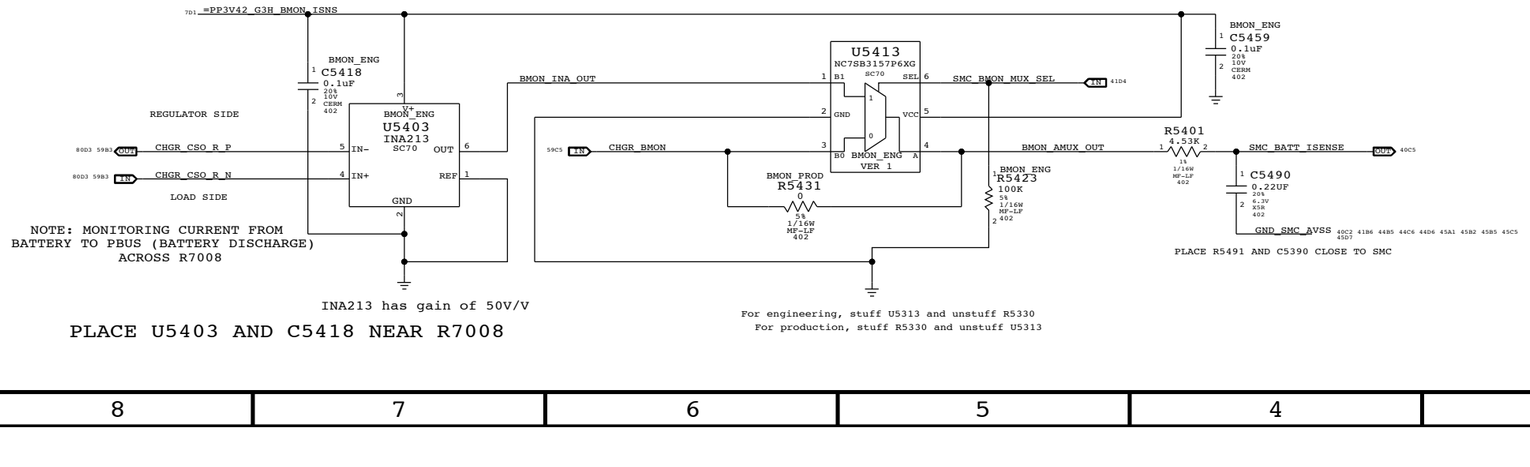
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



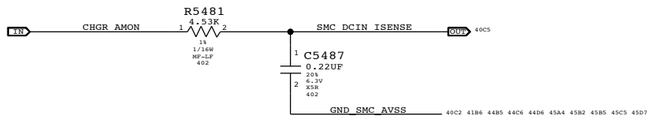
CPU VCore Load Side Current Sense / Filter



BMON CURRENT SENSE



DC-IN (AMON) CURRENT SENSE



SYNC MASTER=YUNWU SYNC DATE=12/17/2008

PAGE TITLE

Current Sensing

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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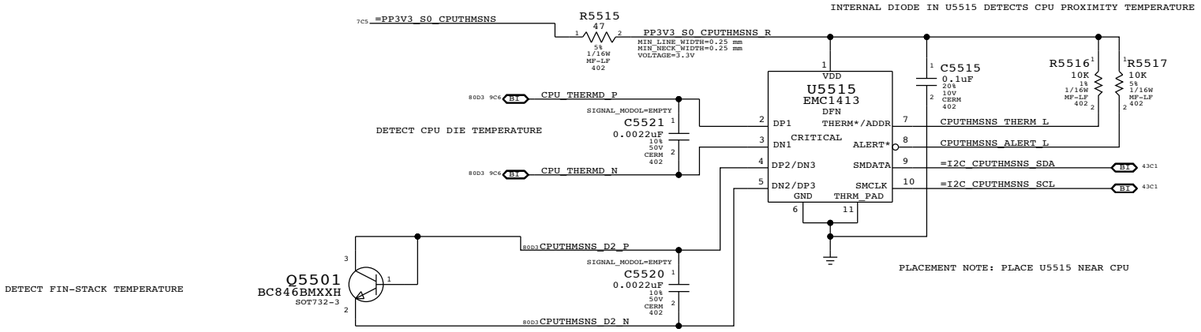
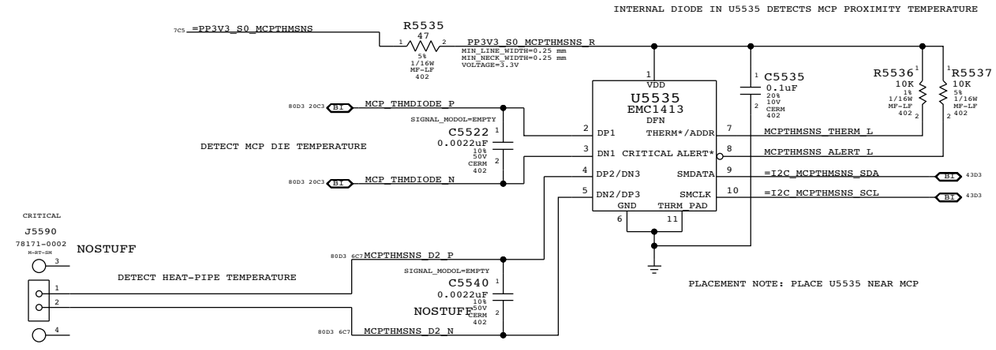
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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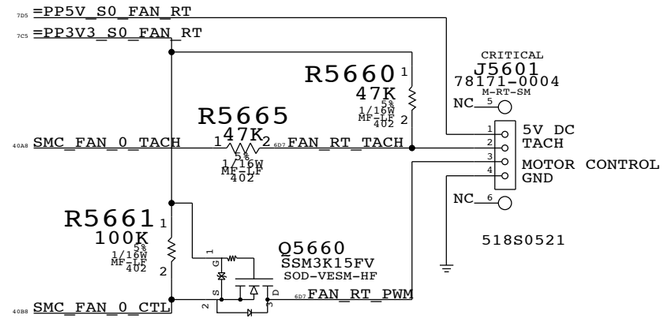

SYNC MASTER=CHANGZHANG SYNC DATE=01/18/2008

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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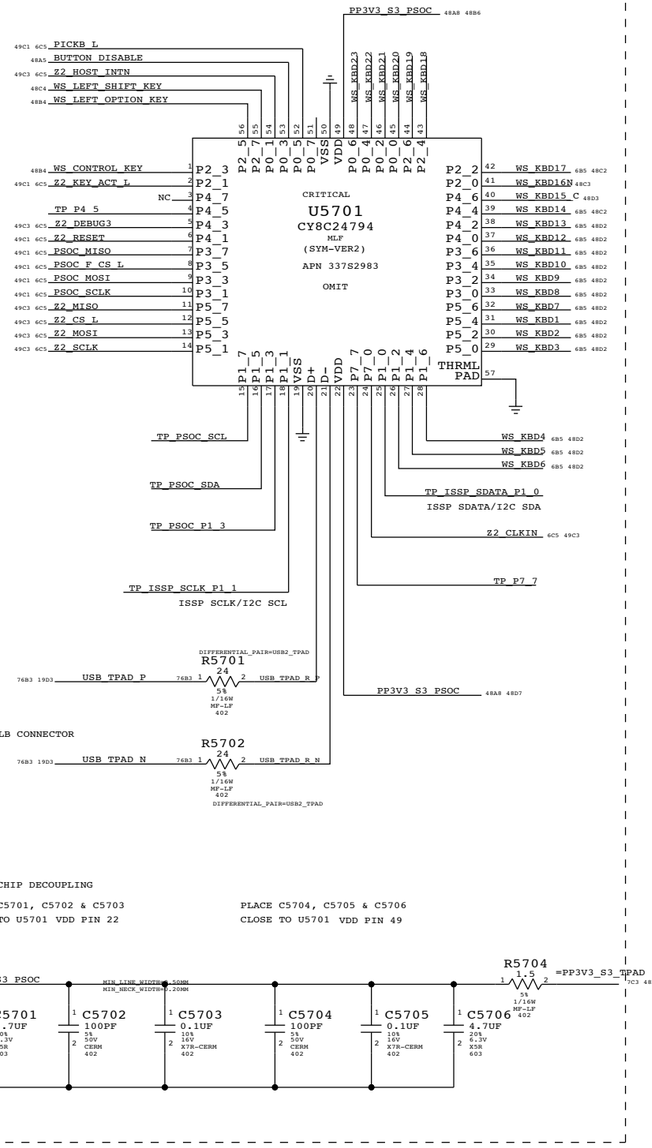
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



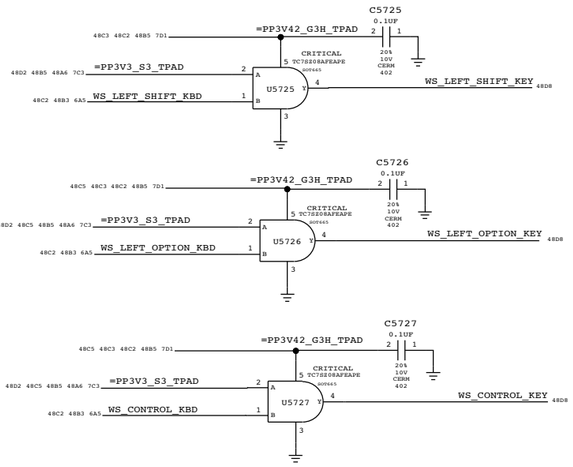
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

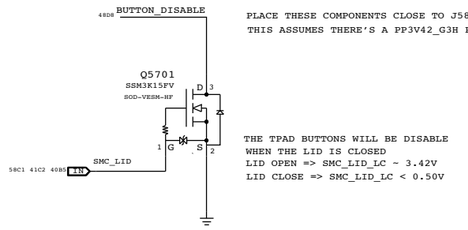
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



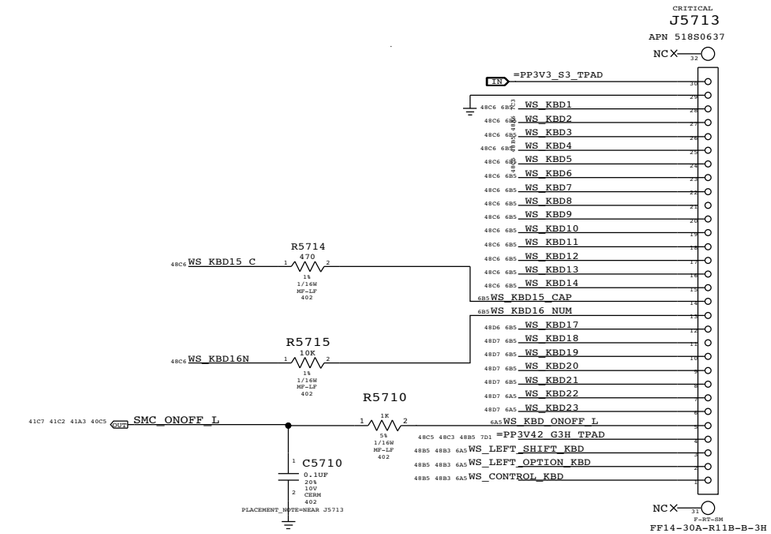
TPAD BUTTONS DISABLE



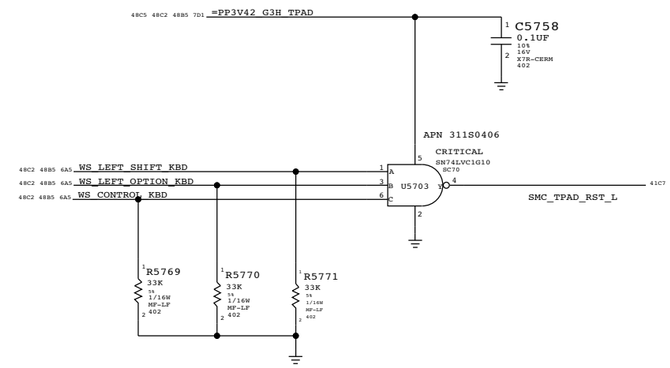
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC MASTER=YUAN.MA SYNC DATE=04/22/2008

PAGE TITLE: WELLSPRING 1

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 57 OF 109
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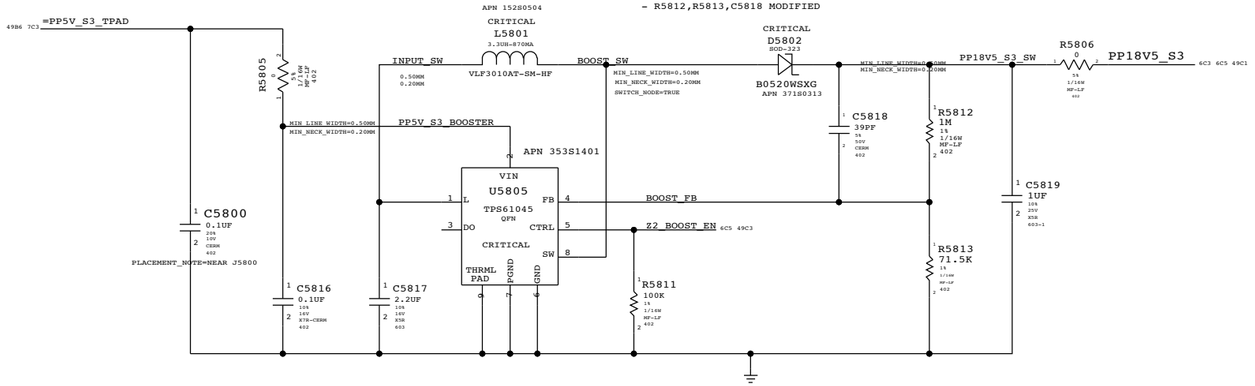
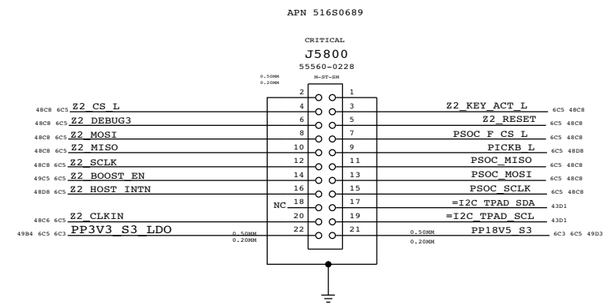
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

BOOSTER +18.5VDC FOR SENSORS

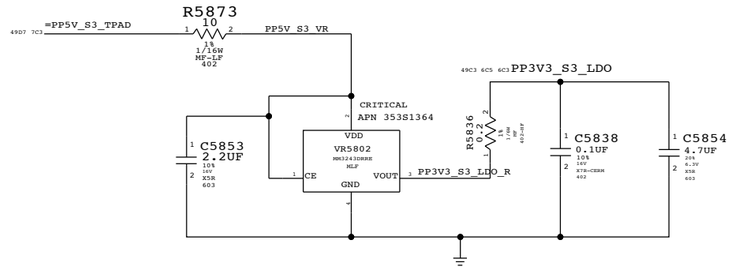
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

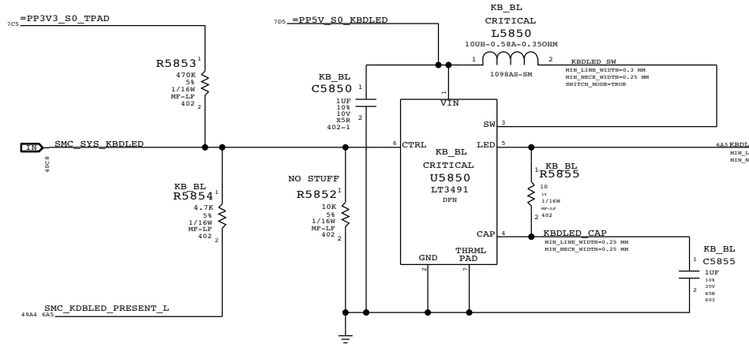
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

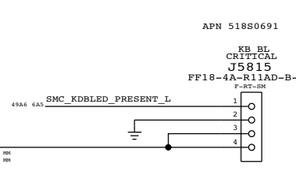
BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



APN 518S0691

J5815 pin 1 is grounded on keyboard backlight flex



KBD BACKLIGHT CONNECTOR

SYNC MASTER=YUAN.MA SYNC DATE=05/09/2008

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

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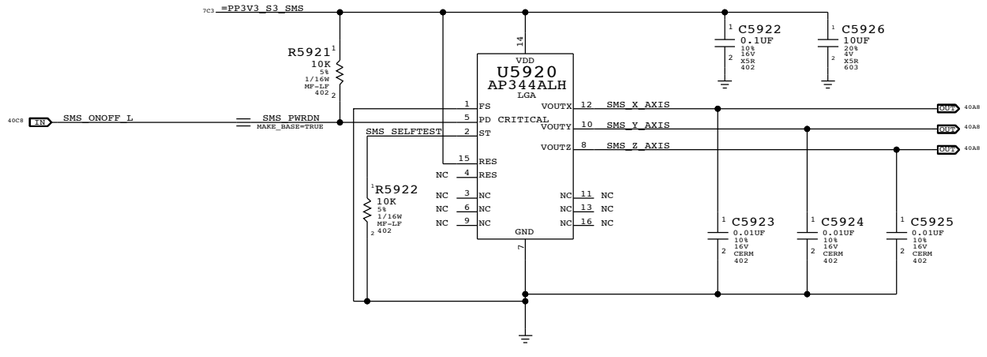
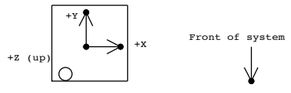
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

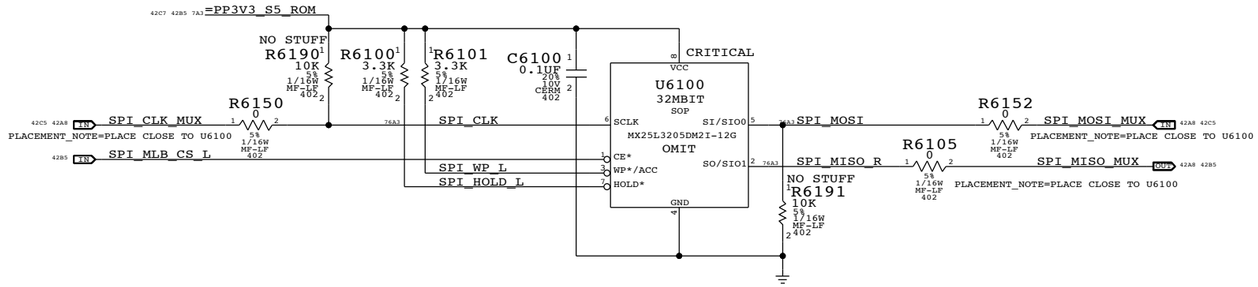


Desired orientation when
placed on board top-side:



Circle indicates pin 1 location when placed
in correct orientation

SYNC MASTER=YUNWU	SYNC DATE=06/26/2008
PAGE TITLE: SMS	
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 59 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

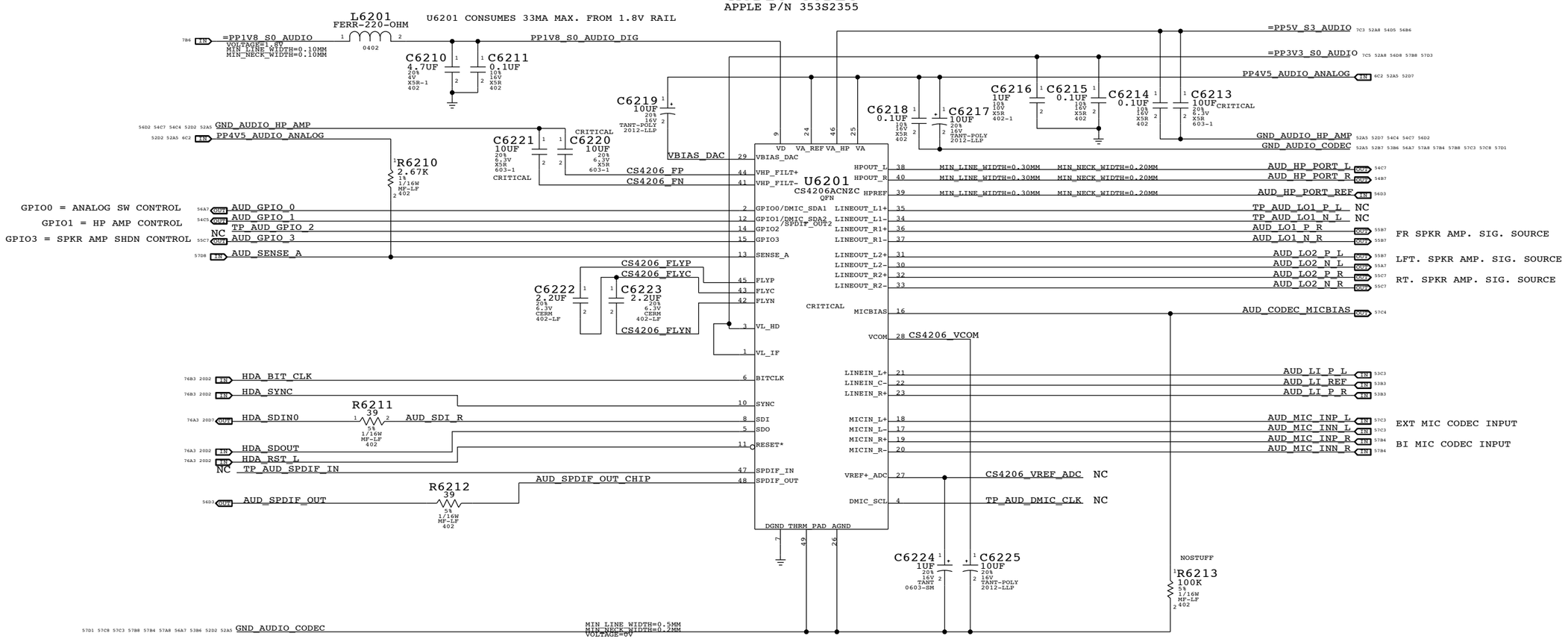
SYNC MASTER=CHANGZHANG SYNC DATE=05/02/2008

PAGE TITLE: SPI ROM

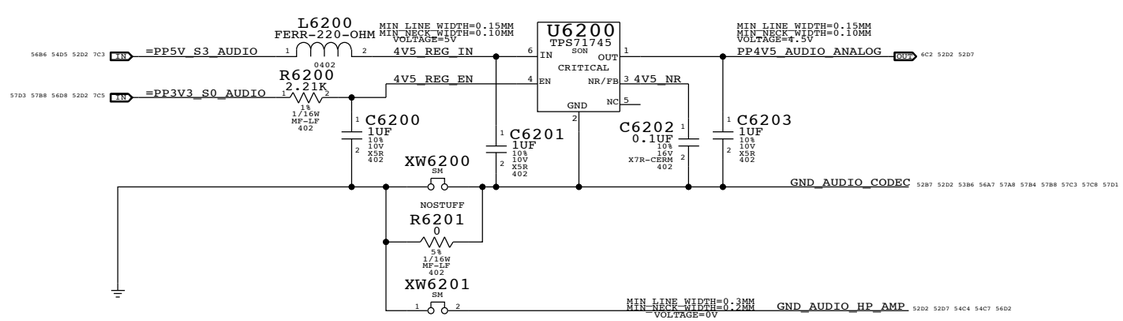
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 61 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=AUDIO
SYNC DATE=03/04/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7898
SIZE: D
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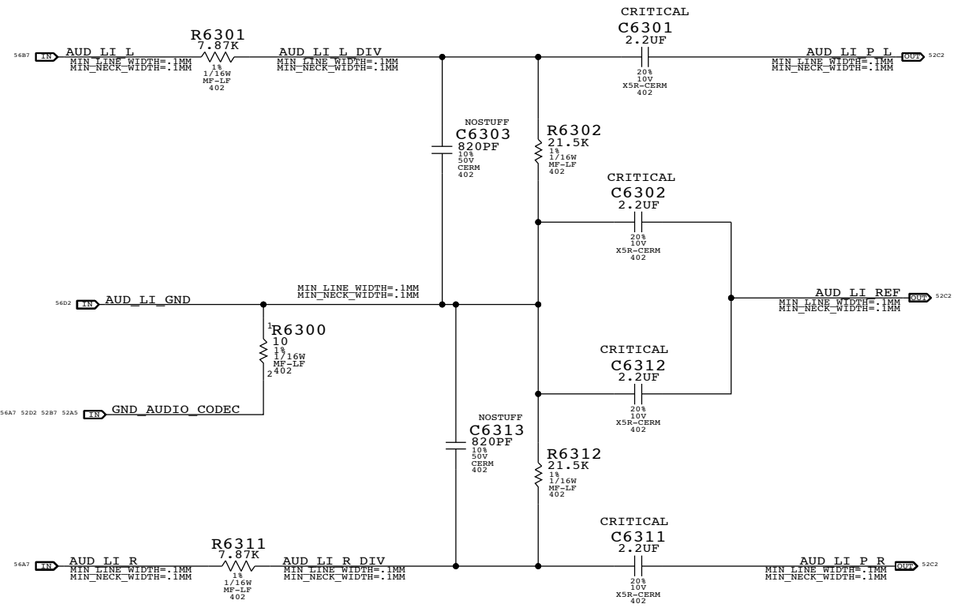
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

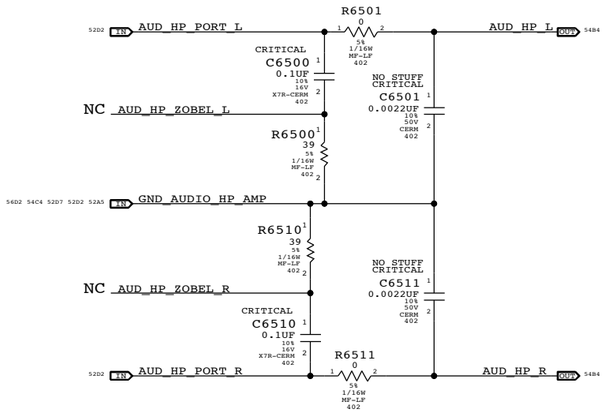


SYNC MASTER=AUDIO SYNC DATE=01/31/2009
PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

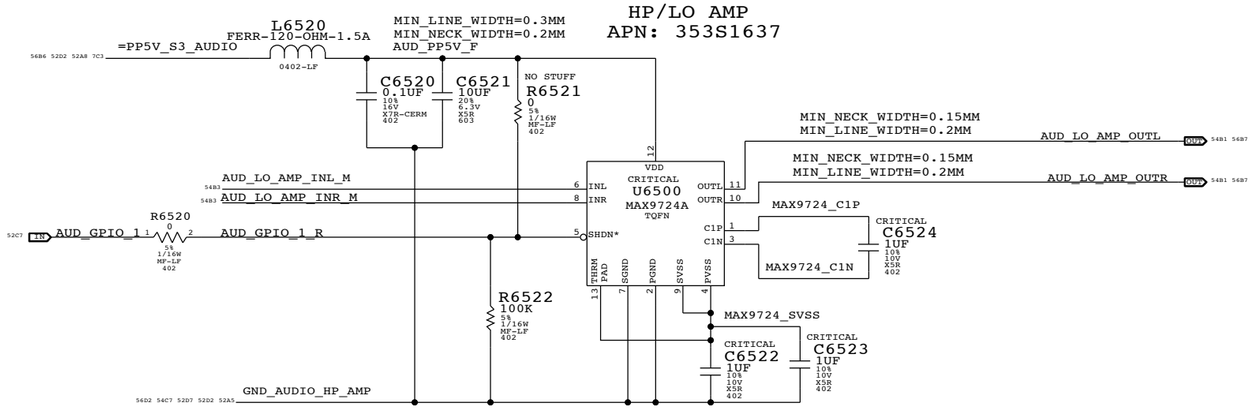
DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 63 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

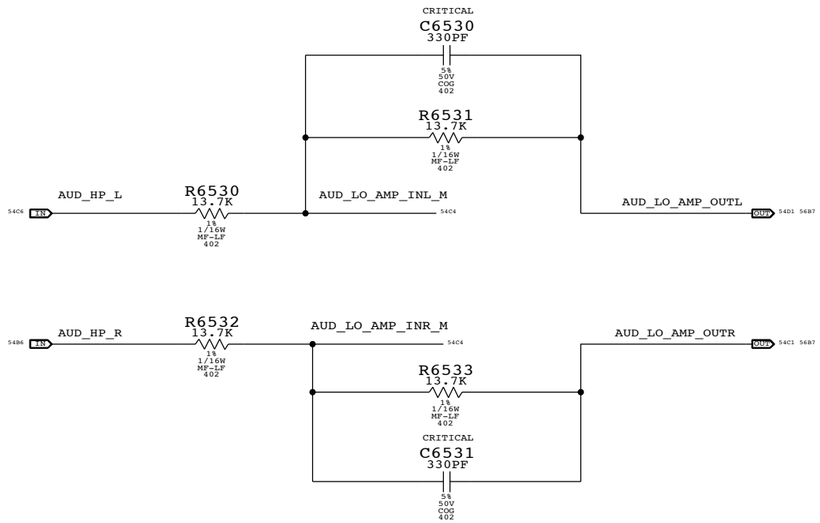


FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC MASTER=AUDIO SYNC DATE=02/03/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
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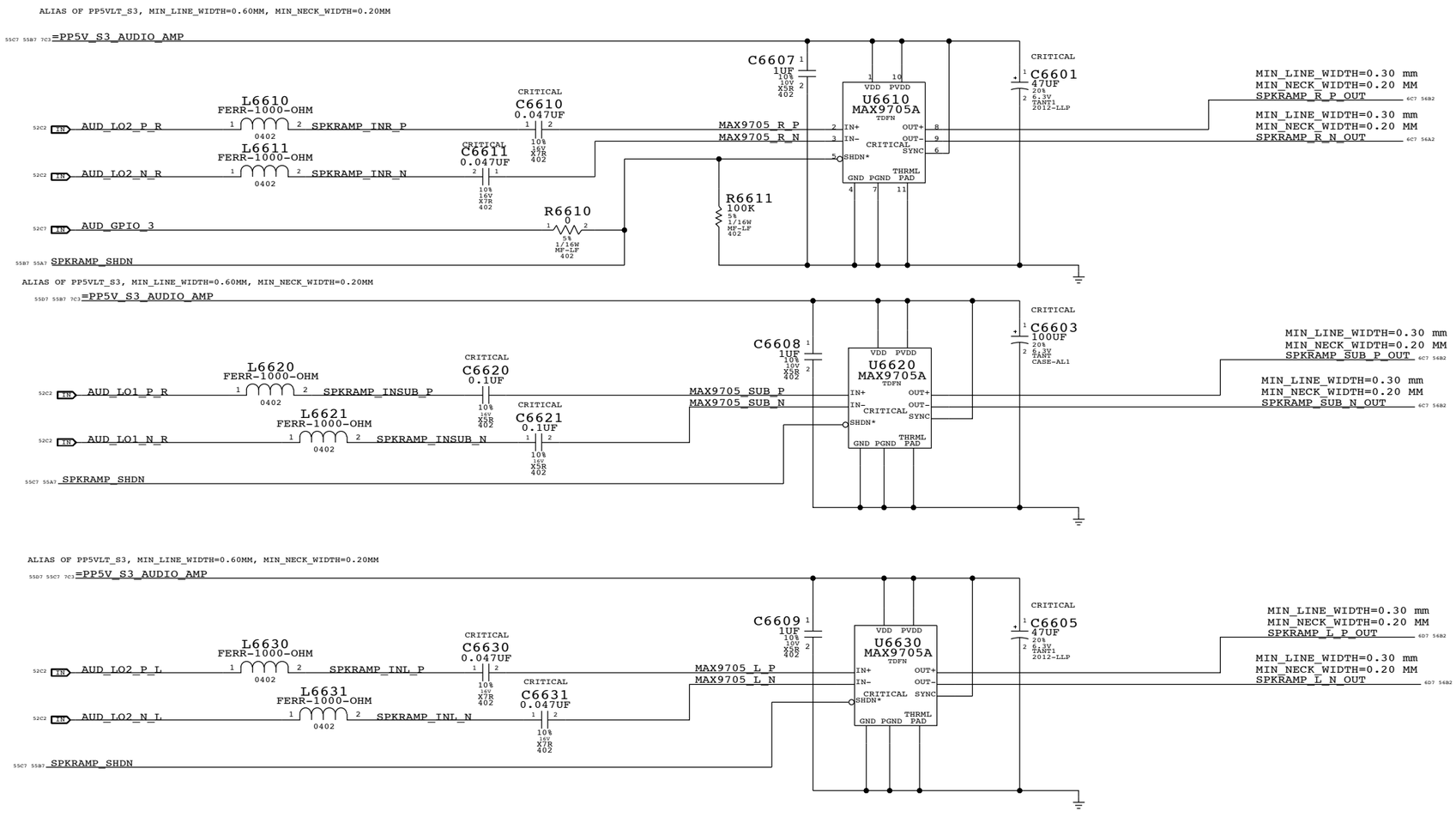
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC MASTER=AUDIO SYNC DATE=12/18/2008

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

AUD_SPDIF_OUT

=PP3V3_S0_AUDIO

APN:514-0671
J6700
SPDIF-TXRX-K24
F-RT-TH
CRITICAL

MIC 6
DETECT 5
SWITCH 2
LEFT 1
RIGHT 3
GND 4
AUDIO

A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL 10
SHIELD PINS 11 12 13

C6700 1UF 10% 6.3V CERM 402

AUD_CONNJ1_MIC
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING

L6701 FERR-1000-OHM 0402 — HS_MIC_HI
L6702 FERR-1000-OHM 0402 — HS_MIC_LO
L6706 CRITICAL FERR-220-OHM 0402 — AUD_HP_PORT_REF
L6703 CRITICAL FERR-120-OHM-1.5A 0402-LF
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONN_GND
L6704 CRITICAL FERR-220-OHM 0402 — AUD_CONN_L
L6705 CRITICAL FERR-220-OHM 0402 — AUD_CONN_R

R6700 10K 5% 1/16W MF-LF 402 — AUD_J1_SLEEVEDET_R
R6701 4.7 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_R

XW6700 SM — GND_AUDIO_HP_AMP
XW6701 SM — AUD_LI_GND
AUD_CONN_GND

DZ6701 CRITICAL 6.8V-100PF 402
DZ6704 CRITICAL 6.8V-100PF 402
DZ6705 CRITICAL 6.8V-100PF 402
DZ6703 CRITICAL 6.8V-100PF 402
DZ6700 CRITICAL 6.8V-100PF 402

C6701 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK

CHASSIS GND STITCHES
XW6710 SM
XW6711 SM
R6760 0 5% 1/16W MF-LF 402

NOSTUFF R6723 0 5% 1/16W MF-LF 402
NOSTUFF R6722 0 5% 1/16W MF-LF 402
NOSTUFF R6725 0 5% 1/16W MF-LF 402
=PP3V42_G3H_AUDIO

R6724 0 5% 1/16W MF-LF 402
=PP5V_S3_AUDIO
PP_MAX14504_VCC

C6710 1UF 10% 10V X5R 402

NOSTUFF R6726 0 5% 1/16W MF-LF 402

APN: 353S2536

U6700
MAX14504
WLP
CRITICAL

VCC A3
C4 NC1
C1 NC2
A4 NO1
A1 NO2
C2 CB
A2 NEG
COM1 B4
COM2 B1
EN* B2
GND B3 C3

AUD_LO_AMP_OUTL — R6716 0 5% 1/16W MF-LF 402 — AUD_LO_AMP_OUTL_SWITCH
AUD_LO_AMP_OUTR — R6717 0 5% 1/16W MF-LF 402 — AUD_LO_AMP_OUTR_SWITCH
AUD_LI_L — R6718 0 5% 1/16W MF-LF 402 — AUD_LI_L_SWITCH
AUD_LI_R — R6719 0 5% 1/16W MF-LF 402 — AUD_LI_R_SWITCH
AUD_GPIO_0 — R6720 0 5% 1/16W MF-LF 402 — AUD_SWITCH_CTRL

SWITCH_CP
C6711 0.0033UF 10% 50V CERM 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
R6712 24K 5% 1/16W MF-LF 402 — AUD_CONN_L
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
R6713 24K 5% 1/16W MF-LF 402 — AUD_CONN_R

R6721 100K 5% 1/16W MF-LF 402

AUD_CONN_GND — R6715 0 5% 1/16W MF-LF 402 — AUD_SWITCH_GND

GND STUFFING OPTIONS FOR CMOS SWITCH
GND_AUDIO_CODEC — R6714 0 5% 1/16W MF-LF 402

NOSTUFF R6727 0 5% 1/16W MF-LF 402

ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

MIC CONNECTOR

APN:518S0520

CRITICAL
J6701
78171-0003
M-RT-SM

BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI

SPEAKER CONNECTOR

APN:518S0519

CRITICAL
J6702
78171-0002
M-RT-SM

SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
SPKRAMP_SUB_P_OUT

C6760 33PF 5% 50V CERM 402
C6761 33PF 5% 50V CERM 402
C6762 33PF 5% 50V CERM 402
C6763 33PF 5% 50V CERM 402

CRITICAL
J6703
78171-0004
M-RT-SM

SPKRAMP_SUB_N_OUT
SPKRAMP_R_P_OUT
SPKRAMP_R_N_OUT

APN:518S0521

C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

SYNC MASTER=AUDIO — SYNC DATE=03/20/2009
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Apple Inc.
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REVISION: C.0.0
BRANCH:
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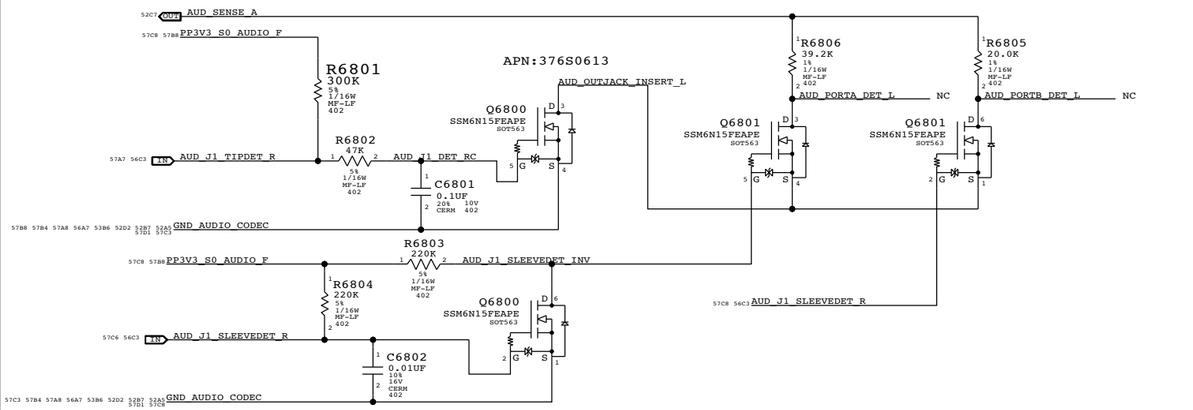
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

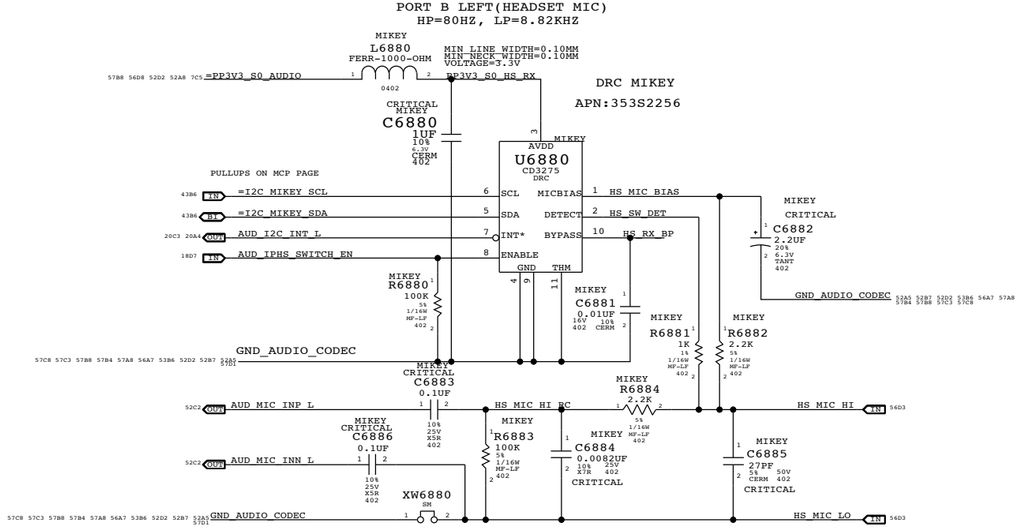
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

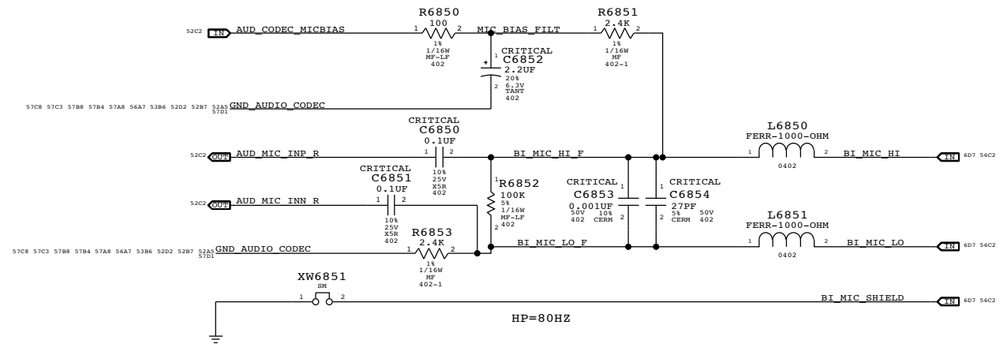
PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



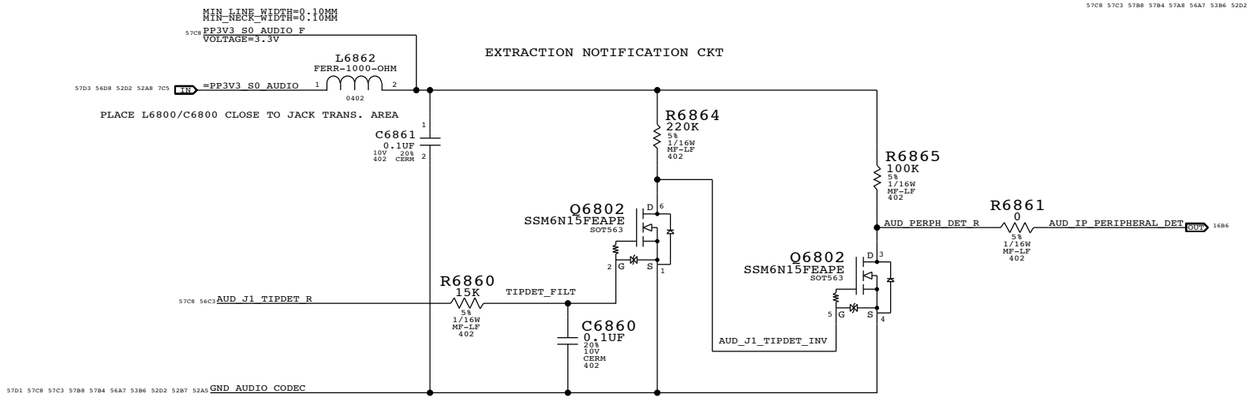
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)

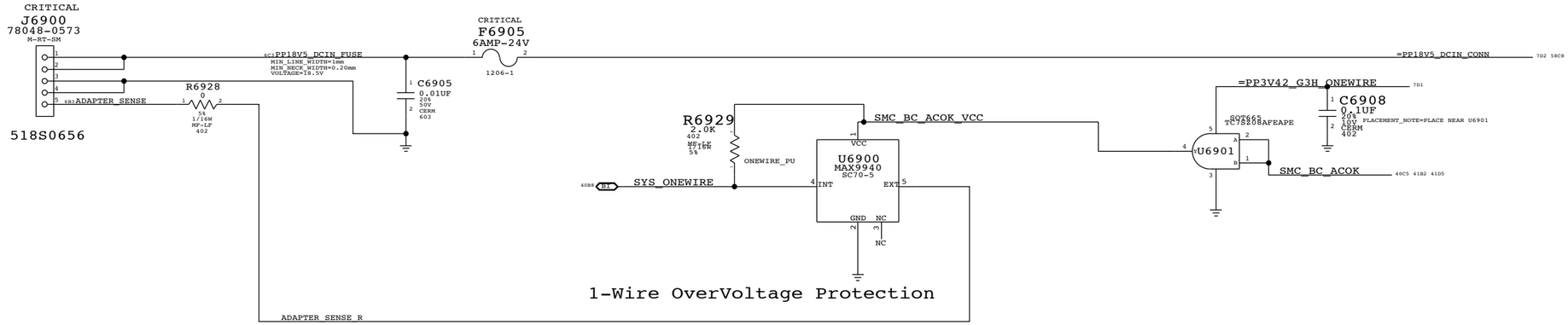


EXTRACTION NOTIFICATION CKT



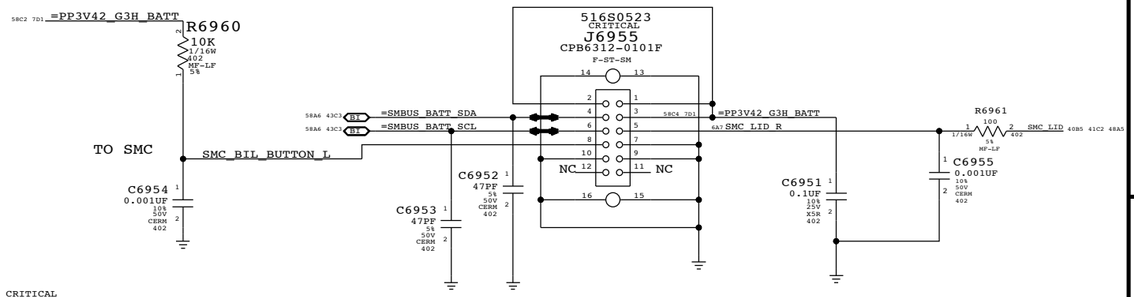
SYNC MASTER=AUDIO	SYNC DATE=03/20/2009
PAGE TITLE: AUDIO: JACK TRANSLATORS	
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 68 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MagSafe DC Power Jack



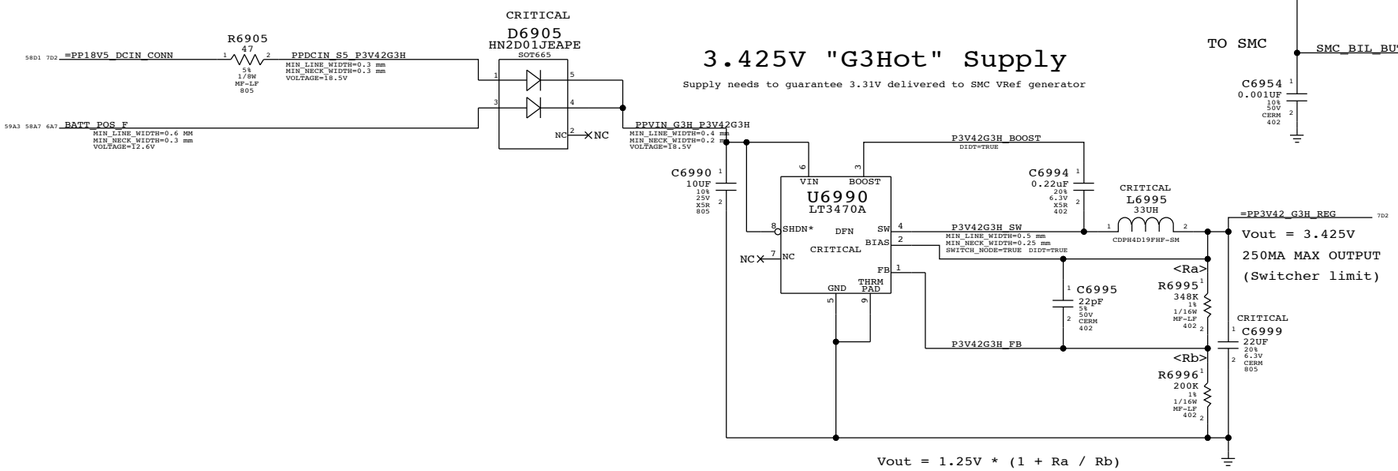
1-Wire OverVoltage Protection

BIL CONNECTOR



3.425V "G3Hot" Supply

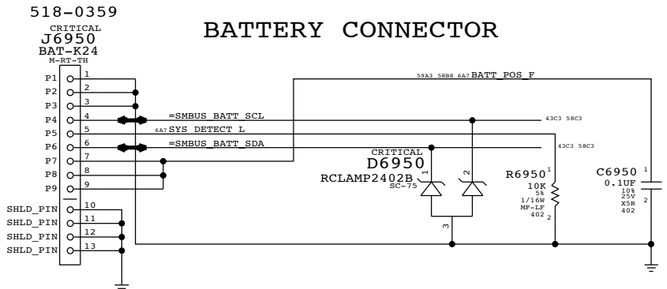
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

518-0359

BATTERY CONNECTOR



SYNC MASTER=YUNWU	SYNC DATE=12/11/2008
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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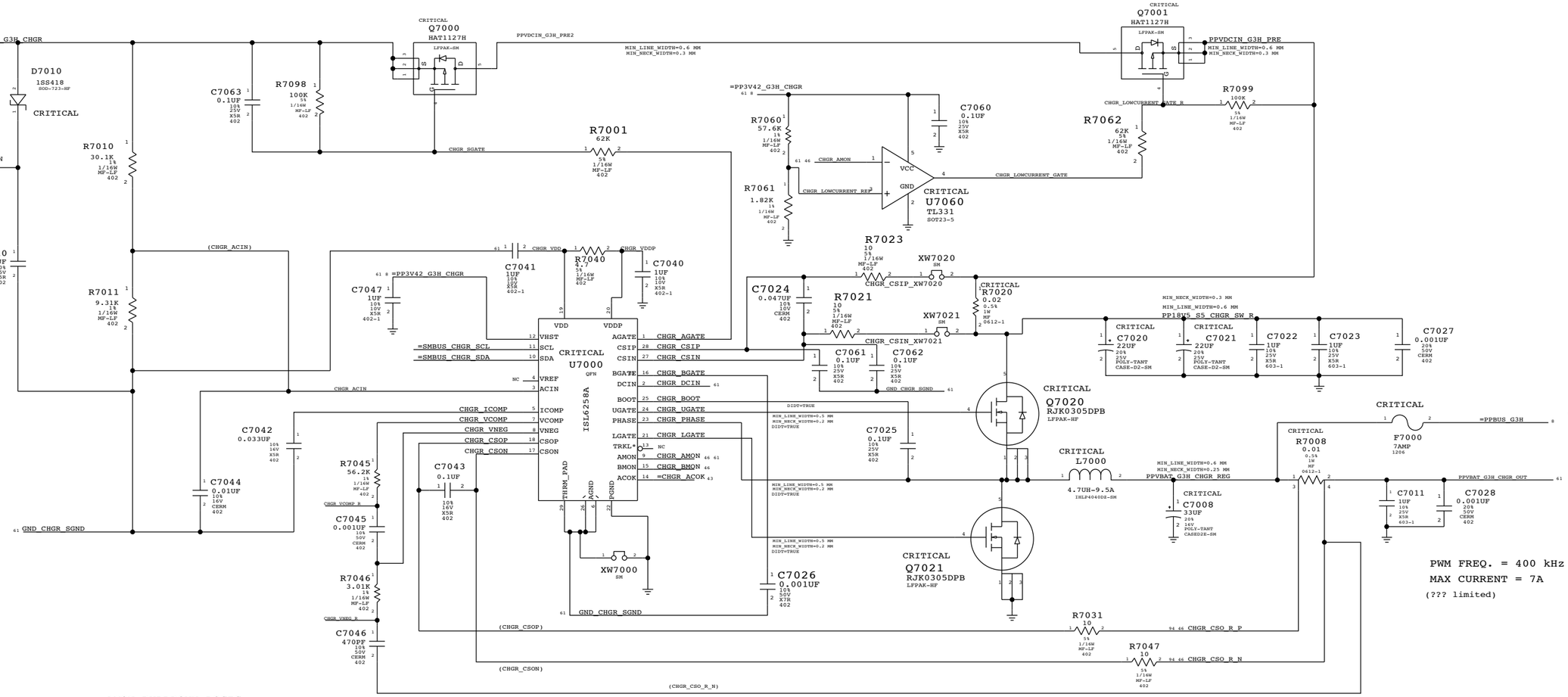
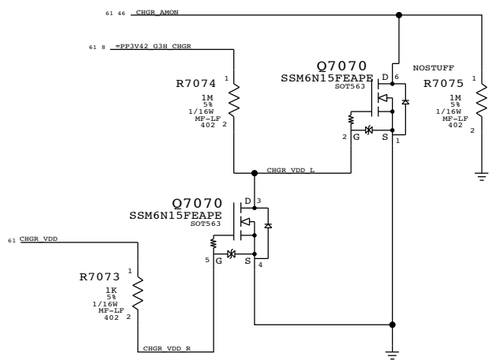
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PBUS SUPPLY / BATTERY CHARGER

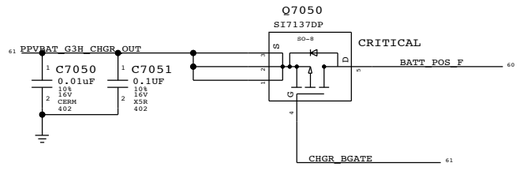


PWM FREQ. = 400 kHz
MAX CURRENT = 7A
(??? limited)

AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS

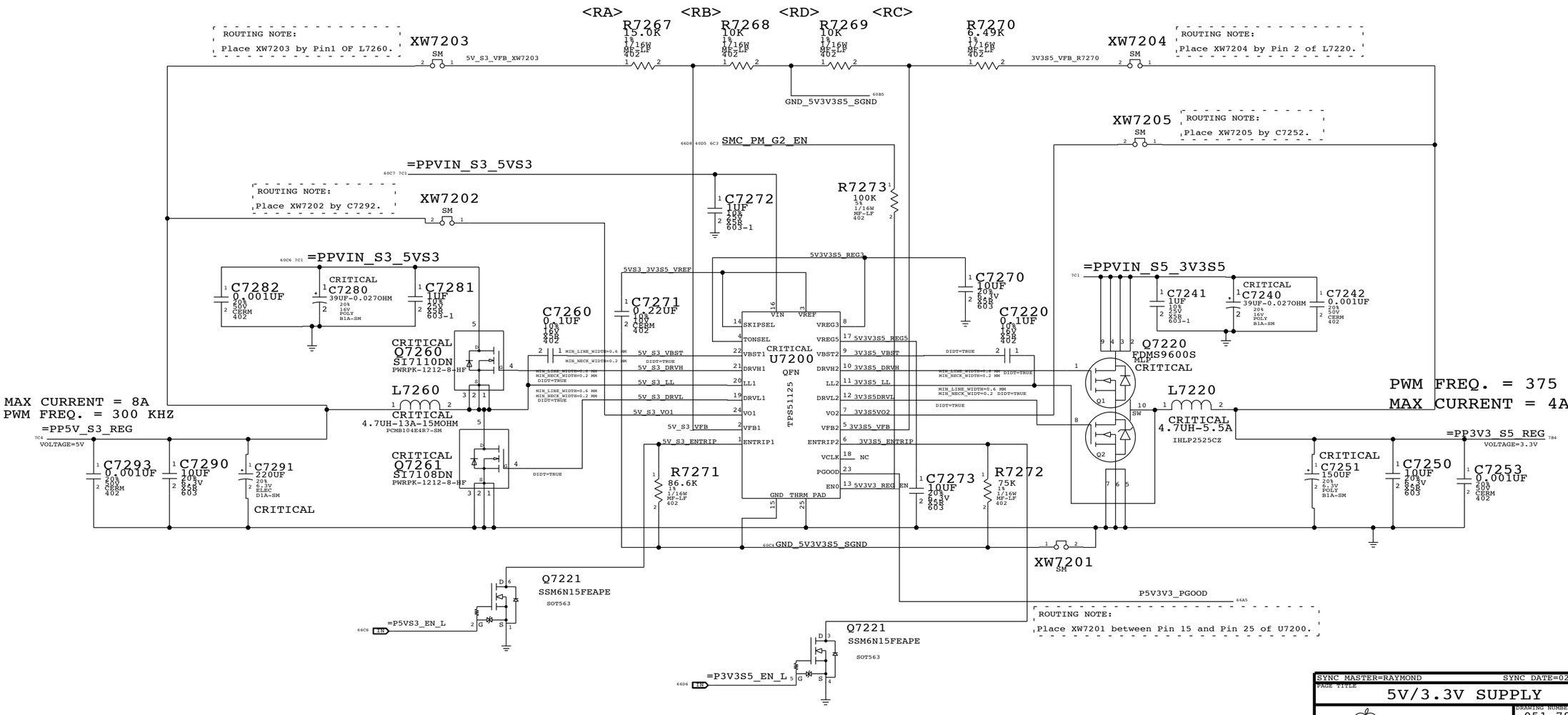


SYNC MASTER=K24_MLB	SYNC DATE=05/20/2009
PAGE TITLE	PBUS Supply/Battery Charger
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 70 OF 109
	SHEET

5V_S3/3.3V_S5 POWER SUPPLY

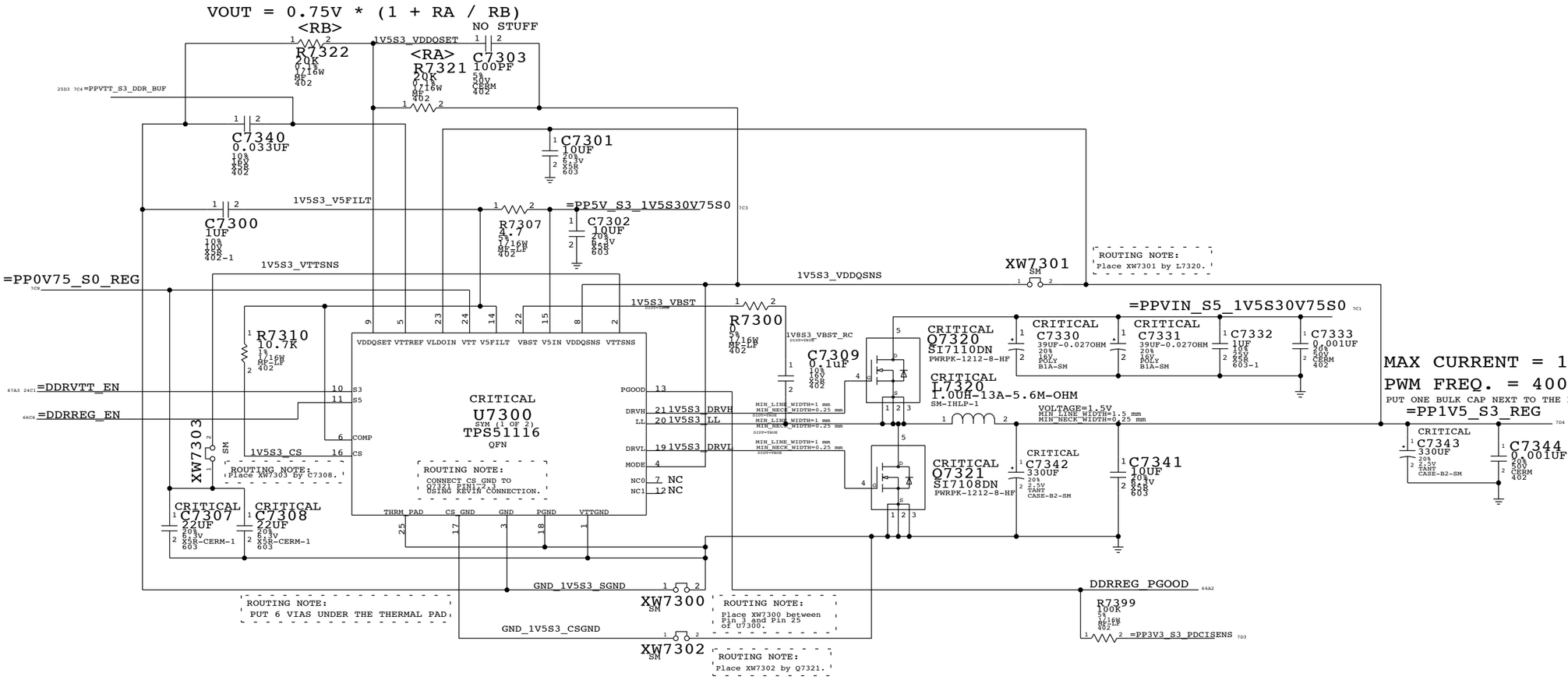
VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SYNC MASTER=RAYMOND	SYNC DATE=02/08/2008
PAGE TITLE	5V/3.3V SUPPLY
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE 72 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC MASTER=RAYMOND SYNC DATE=01/31/2008

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

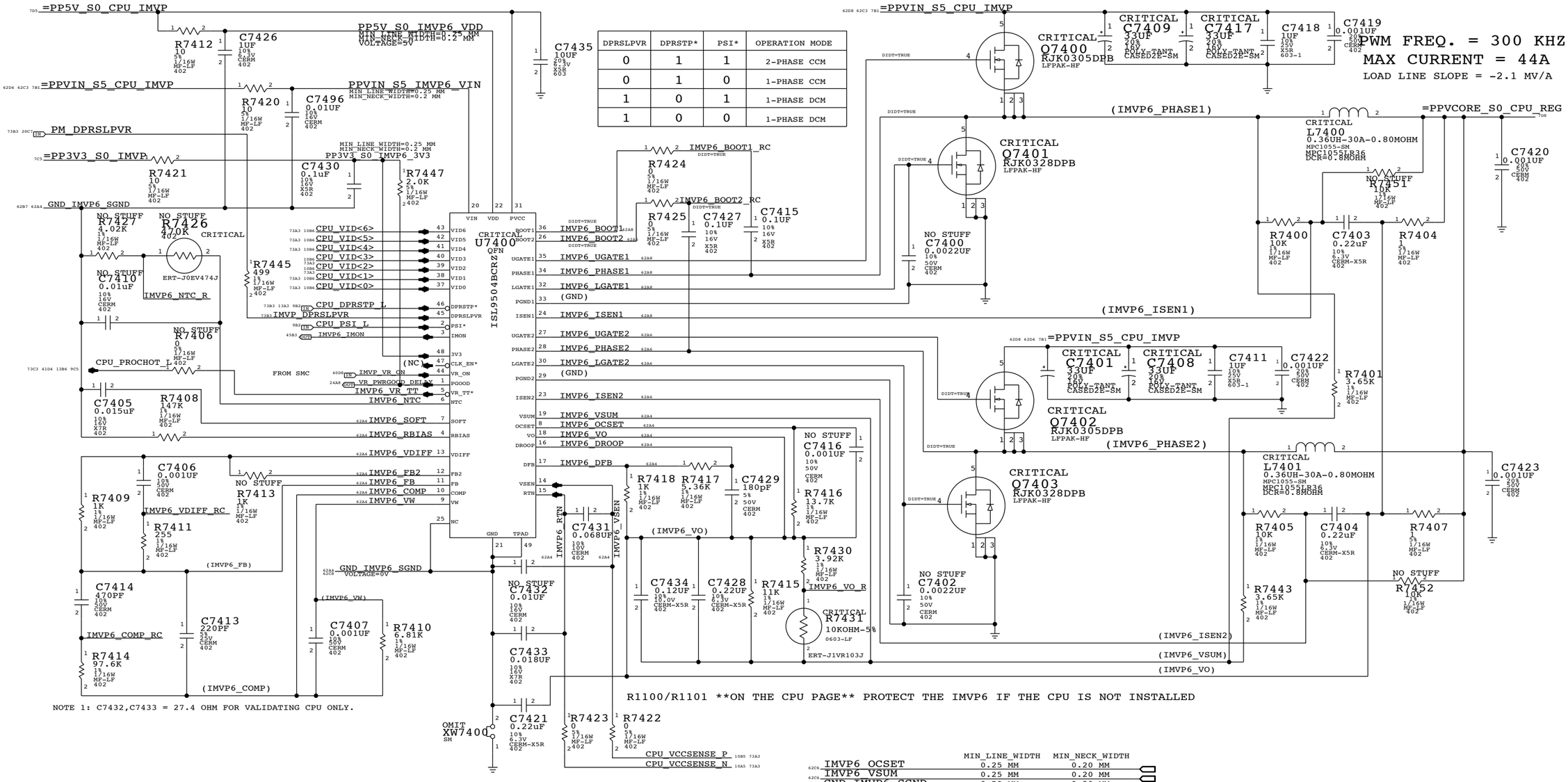
DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 73 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC MASTER=RAYMOND SYNC DATE=01/31/2008

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

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BRANCH:

PAGE: 74 OF 109

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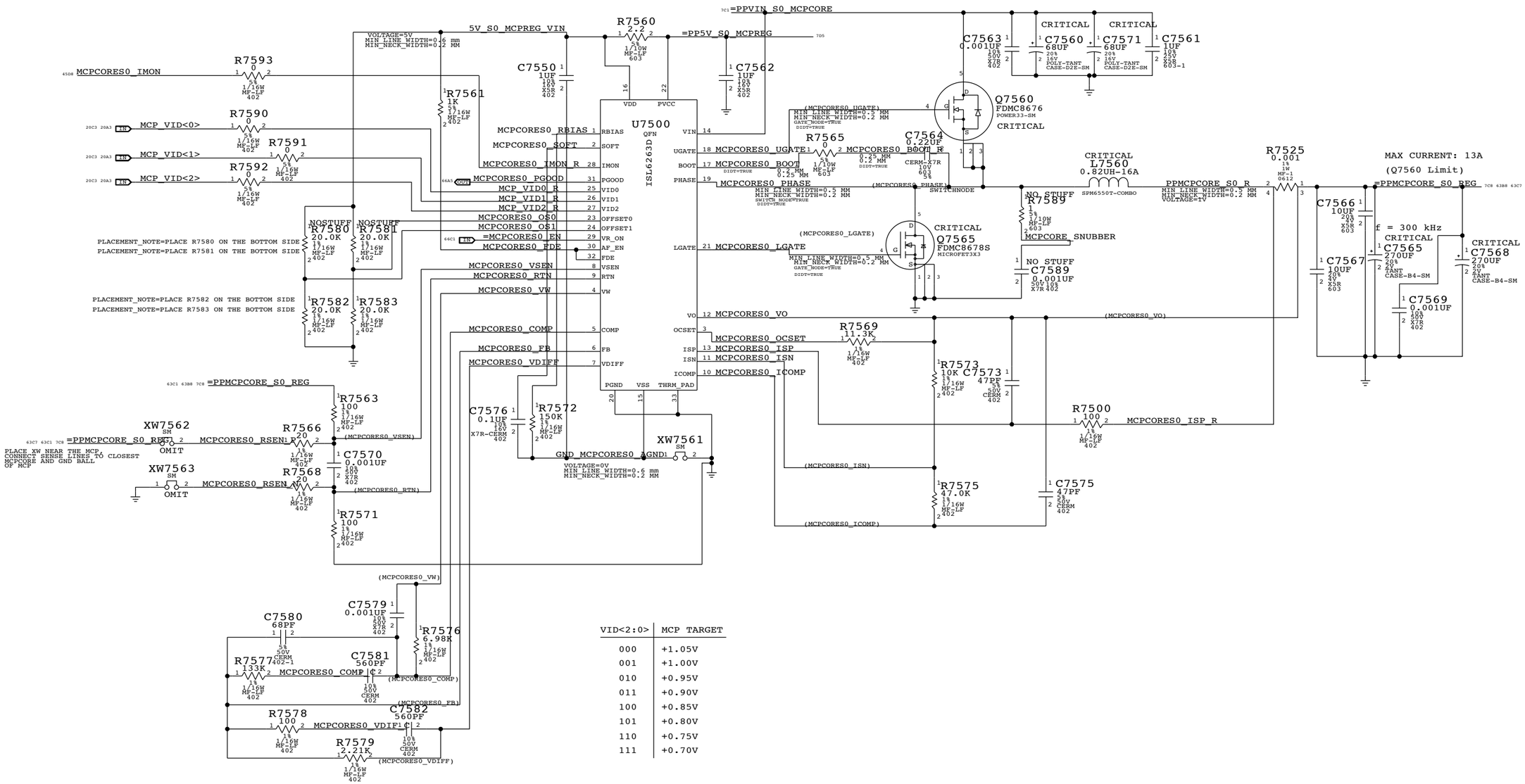
MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

SYNC MASTER=K19 MLB SYNC DATE=12/10/2008

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

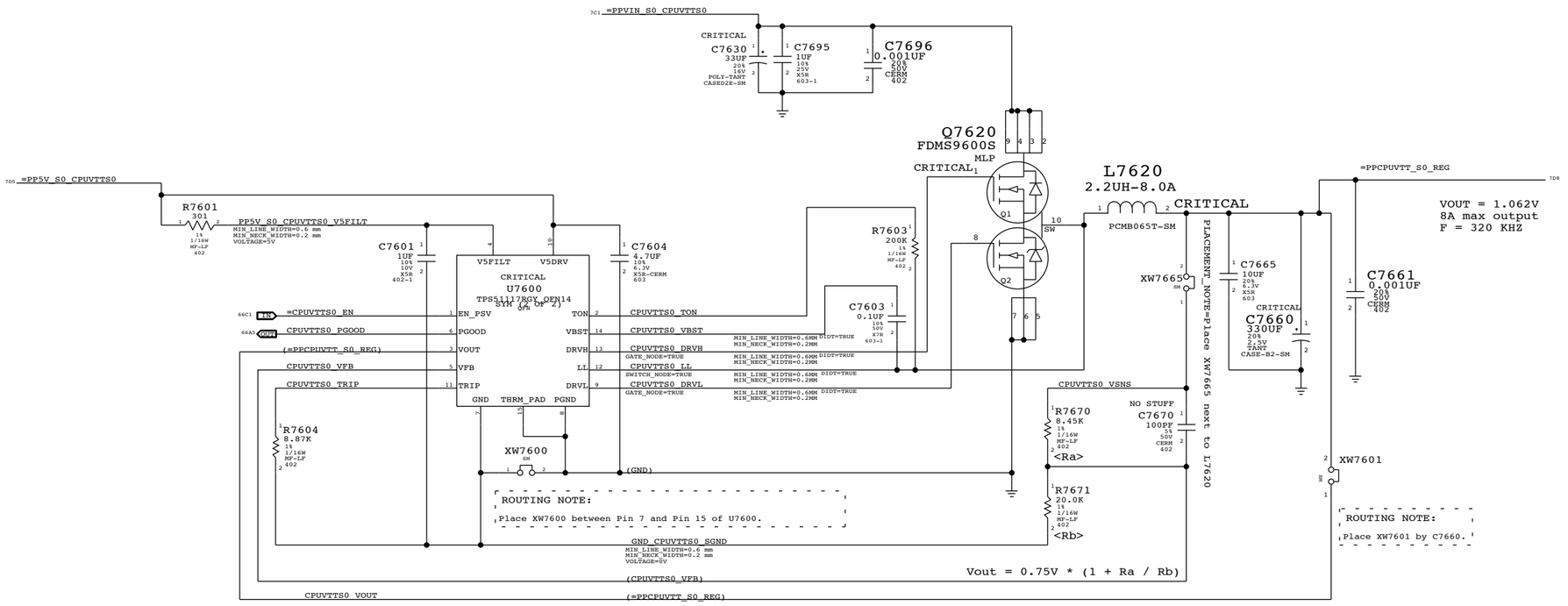
REVISION: C.0.0

BRANCH:

PAGE: 75 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPUVTT POWER SUPPLY



SYNC MASTER=RAYMOND SYNC DATE=02/08/2008

PAGE TITLE

CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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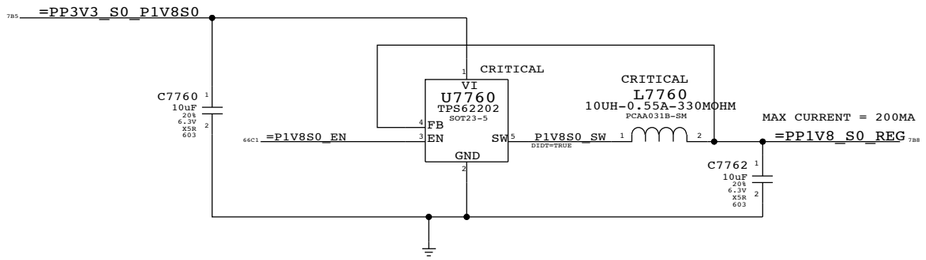
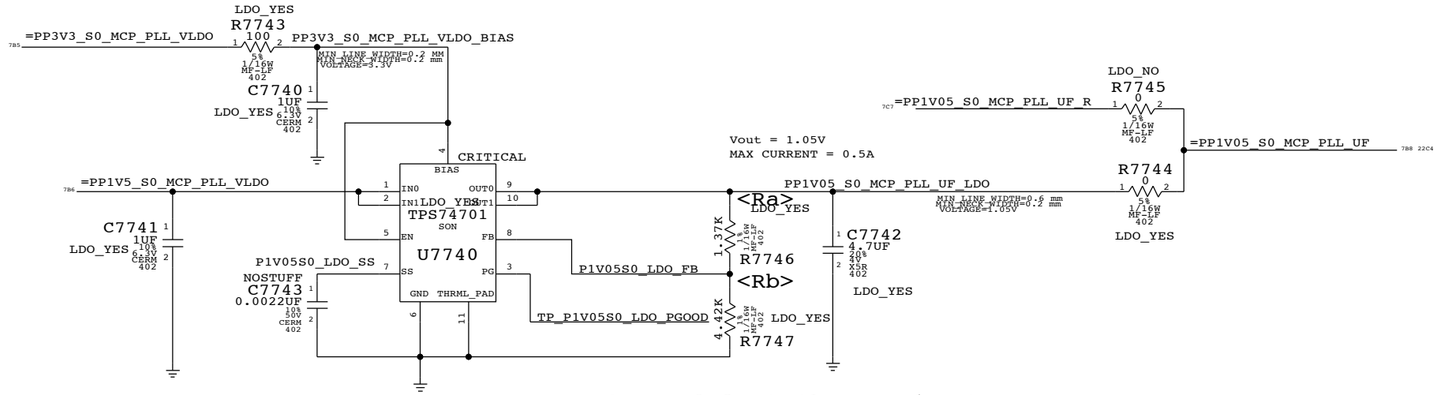
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.8V S0 SWITCHER

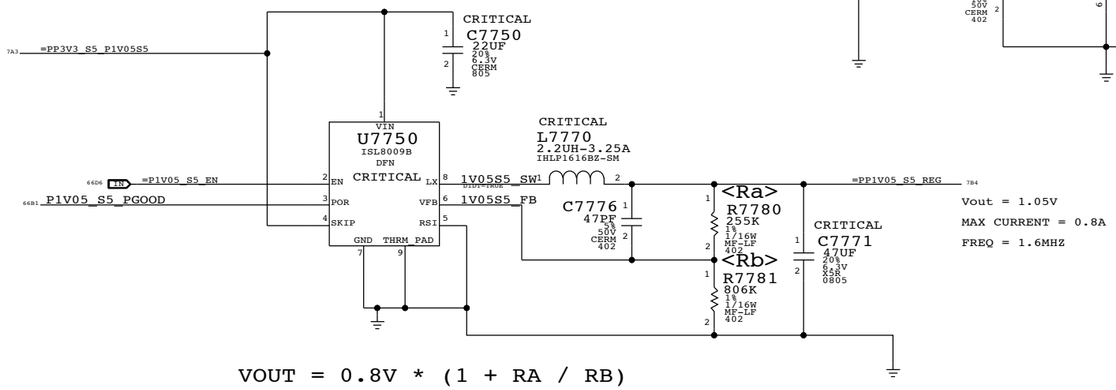


1.05V S0 PLL LDO



VOUT = 0.8V * (1 + RA / RB)

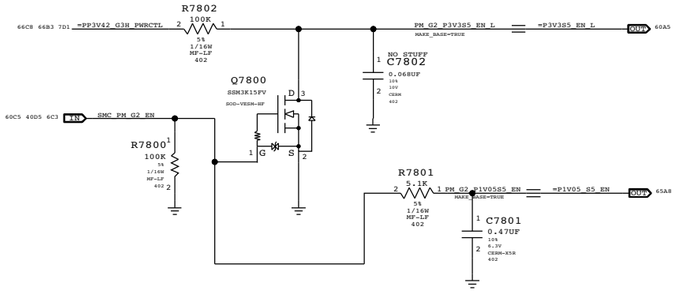
MCP 1.05V S5 (AUXC) SUPPLY



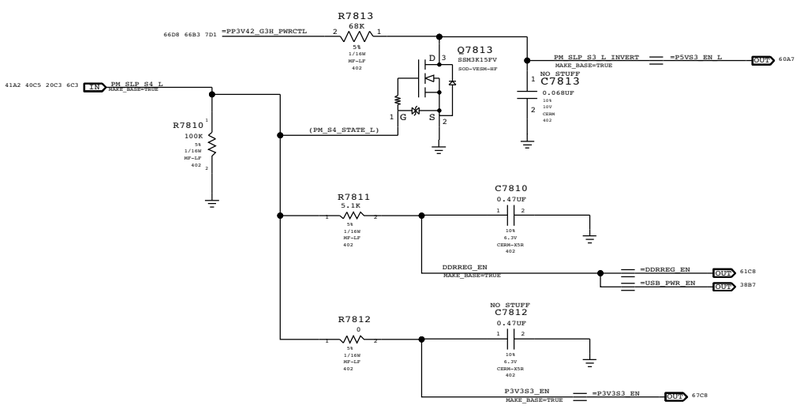
VOUT = 0.8V * (1 + RA / RB)

SYNC MASTER=RAYMOND	SYNC DATE=01/23/2008
PAGE TITLE: MISC POWER SUPPLIES	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 77 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3.3V 1.05V S5 ENABLE

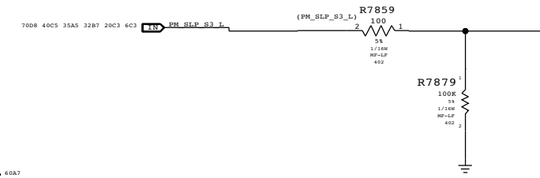


S3 ENABLE

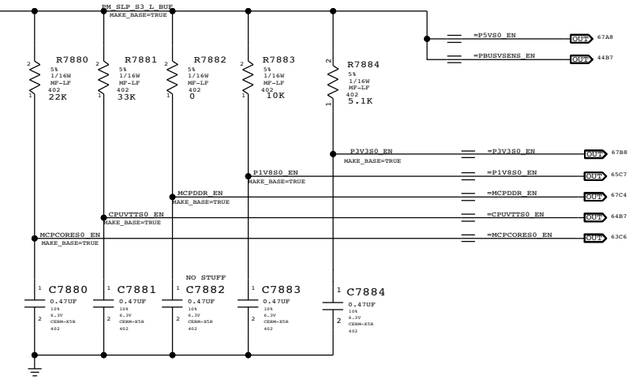


Power Control Signals

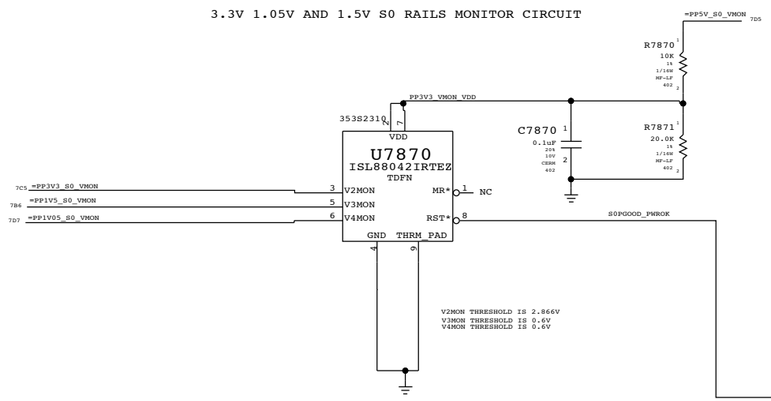
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



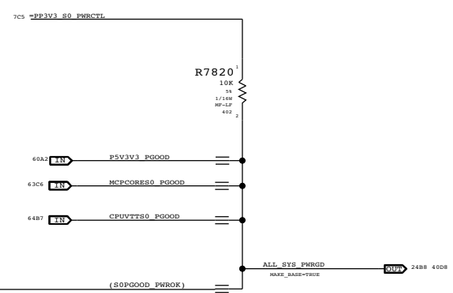
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



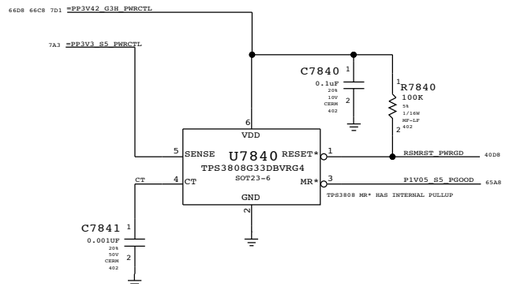
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



VOLTAGE MONITOR



Unused PGOOD signal

SYNC MASTER=YUAN.MA SYNC DATE=12/11/2008

PAGE TITLE

POWER SEQUENCING

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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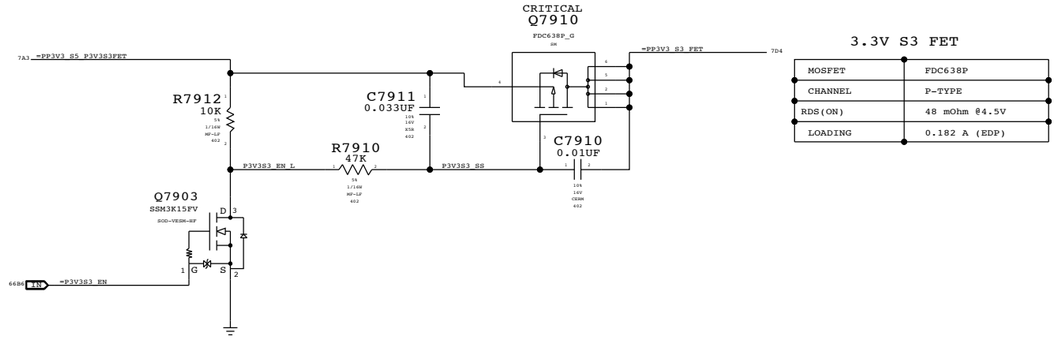
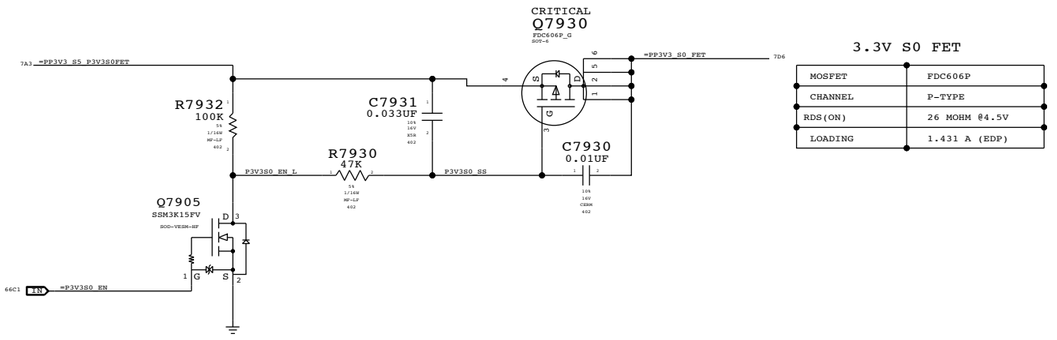
3.3V S3 FET



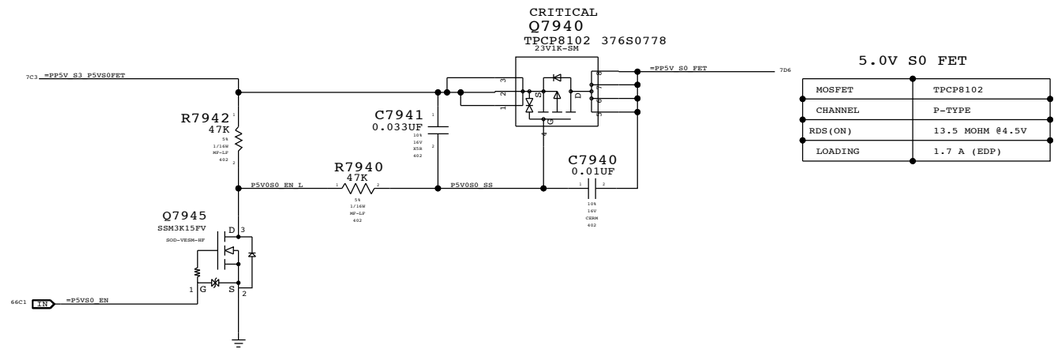
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

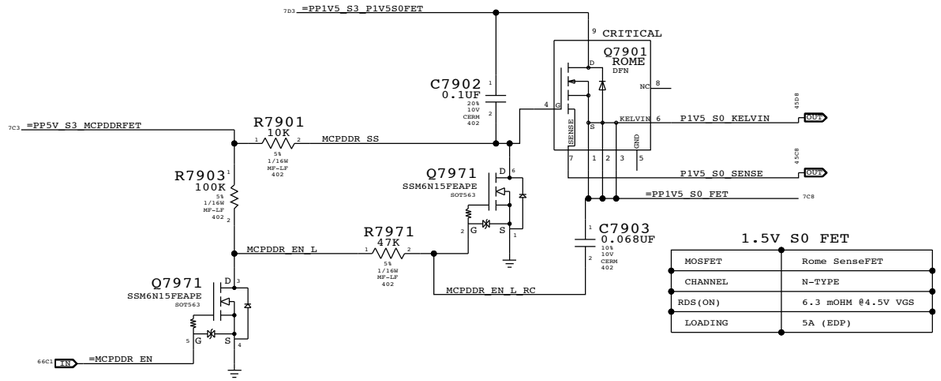
5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

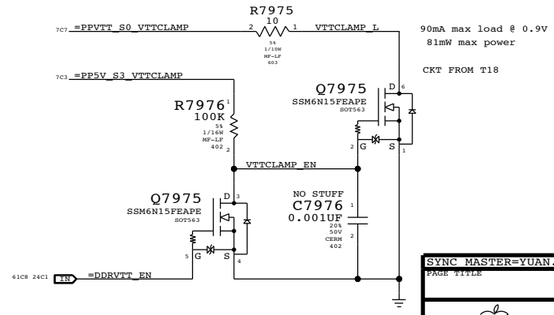
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC MASTER=YUAN.MA SYNC DATE=12/11/2008

PAGE TITLE: POWER FETS

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

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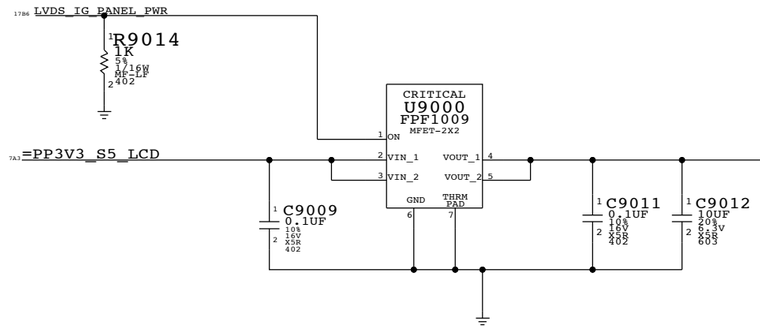
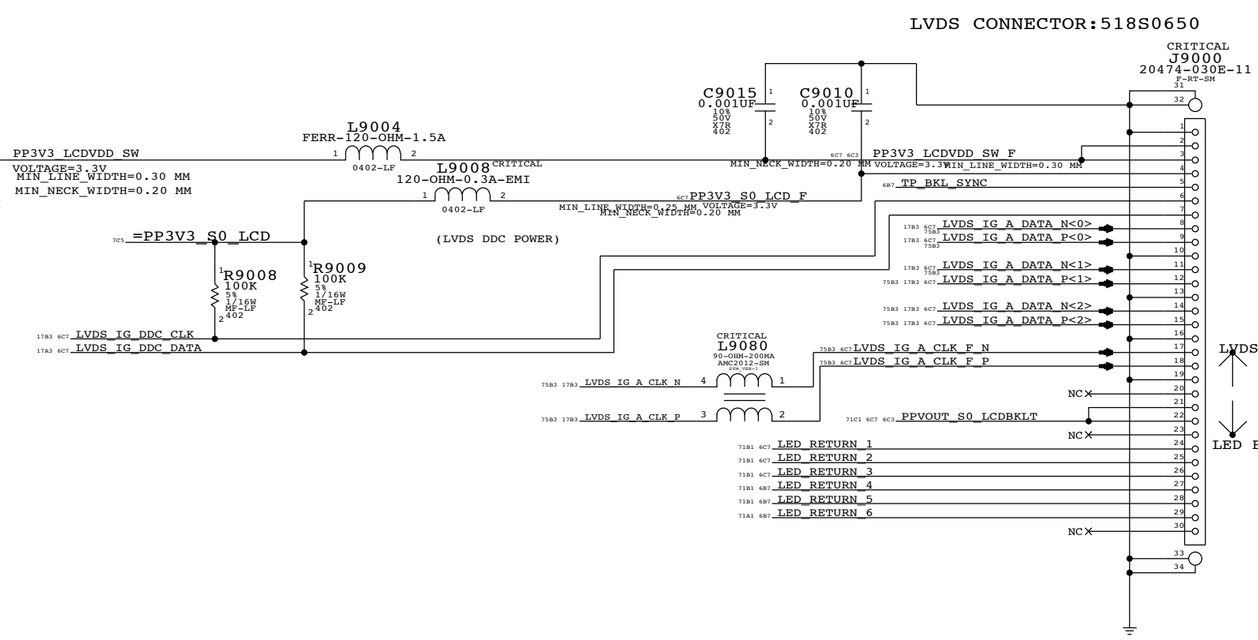
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP





LCD CONNECTOR

LVDS CONNECTOR:518S0650

SYNC MASTER=NMARTIN SYNC DATE=04/04/2008

PAGE TITLE

LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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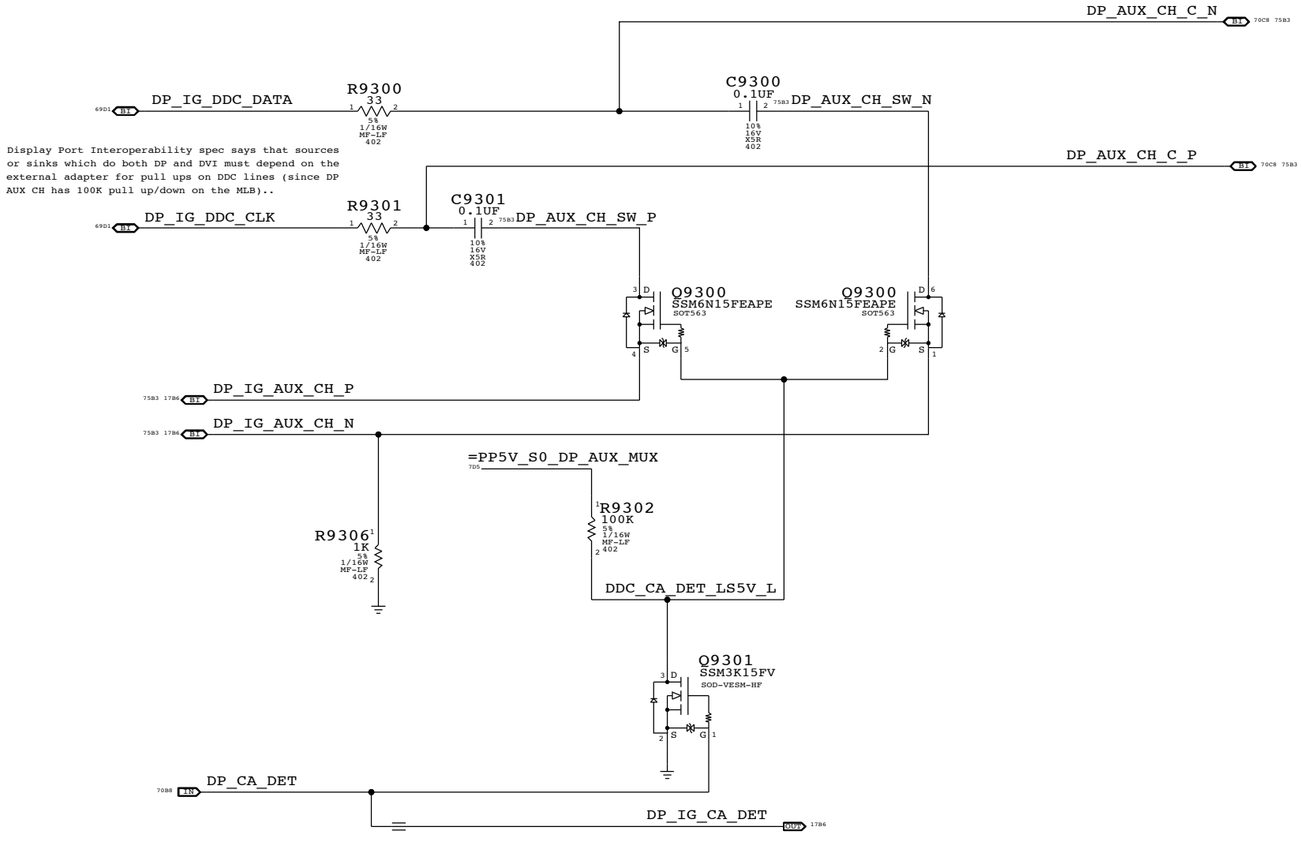
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

17B6 =MCP_HDMI_TXC_P — DP_ML_P<3> — 70C8 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXC_N — DP_ML_N<3> — 70C8 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXD_P<0> — DP_ML_P<2> — 70C1 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXD_N<0> — DP_ML_N<2> — 70C1 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXD_P<1> — DP_ML_P<1> — 70C1 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXD_N<1> — DP_ML_N<1> — 70C1 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXD_P<2> — DP_ML_P<0> — 70C1 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_TXD_N<2> — DP_ML_N<0> — 70C1 75C3 MAKE_BASE=TRUE
17B6 =MCP_HDMI_HPD — DP_HPD — 70A8 MAKE_BASE=TRUE
17A3 =MCP_HDMI_DDC_CLK — DP_IG_DDC_CLK — 69C8 MAKE_BASE=TRUE
17A3 =MCP_HDMI_DDC_DATA — DP_IG_DDC_DATA — 69C8 MAKE_BASE=TRUE



SYNC MASTER=AMASON SYNC DATE=04/18/2008

PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
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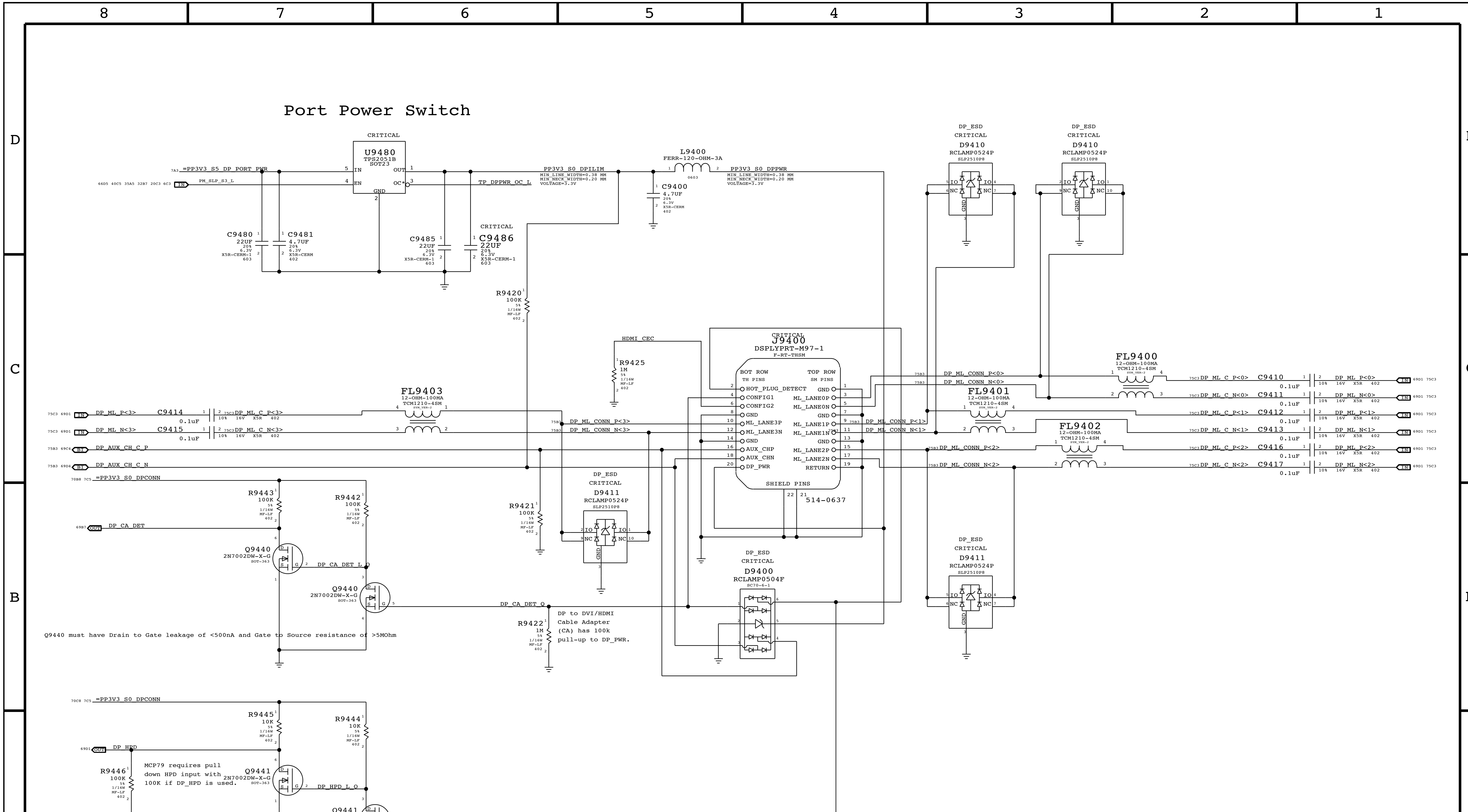
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>


Port Power Switch
CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
PP3V3_S0_DPILIM
TP_DPPWR_OC_L
L9400
FERR-120-OHM-3A
PP3V3_S0_DPPWR
C9400
4.7UF
C9480
22UF
C9481
4.7UF
C9485
22UF
C9486
22UF
R9420
100K
HDMI_CEC
R9425
1M
CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM
BOT ROW
TOP ROW
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0637
FL9403
FL9400
FL9401
FL9402
12-OHM-100MA
TCM1210-4SM
C9414
C9415
C9410
C9411
C9412
C9413
C9416
C9417
0.1uF
DP_ML_P<3>
DP_ML_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N
DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
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DP_ML_CONN_N<0>
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DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>
DP_ML_P<0>
DP_ML_N<0>
DP_ML_P<1>
DP_ML_N<1>
DP_ML_P<2>
DP_ML_N<2>
DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8
D9411
D9400
RCLAMP0504F
SC70-6-1
=PP3V3_S0_DPCONN
R9443
100K
R9442
100K
DP_CA_DET
Q9440
2N7002DW-X-G
DP_CA_DET_L_Q
DP_CA_DET_Q
R9421
100K
R9422
1M
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
R9445
10K
R9444
10K
DP_HPD
R9446
100K
MCP79 requires pull down HPD input with 100K if DP_HPD is used.
Q9441
2N7002DW-X-G
DP_HPD_L_Q
DP_HPD_Q
R9423
100K
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC_MASTER=AMASON SYNC_DATE=06/30/2008

PAGE TITLE

DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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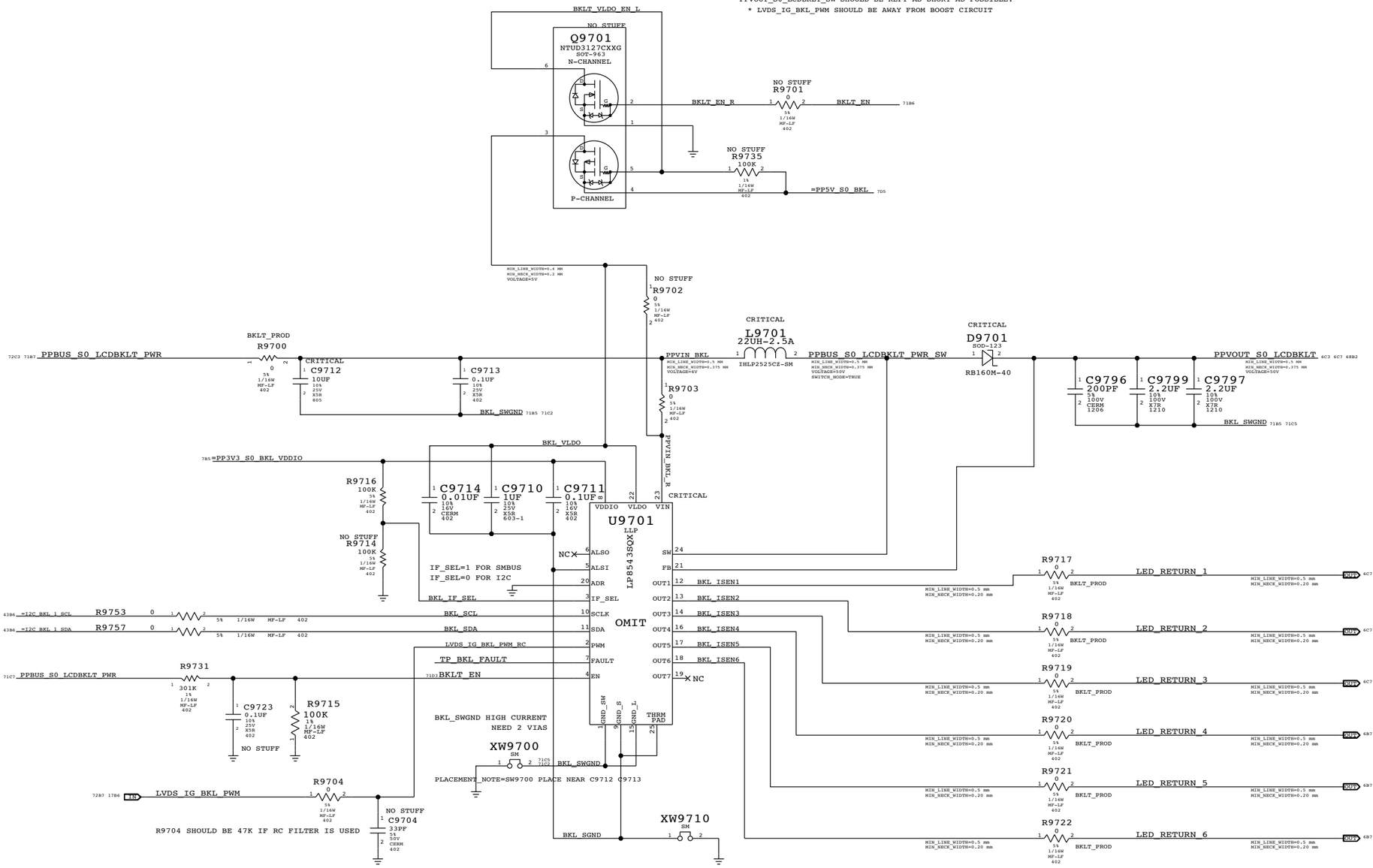
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

SYNC MASTER=KIRAN SYNC DATE=12/05/2008

PAGE TITLE
LCD BACKLIGHT DRIVER

Apple Inc.

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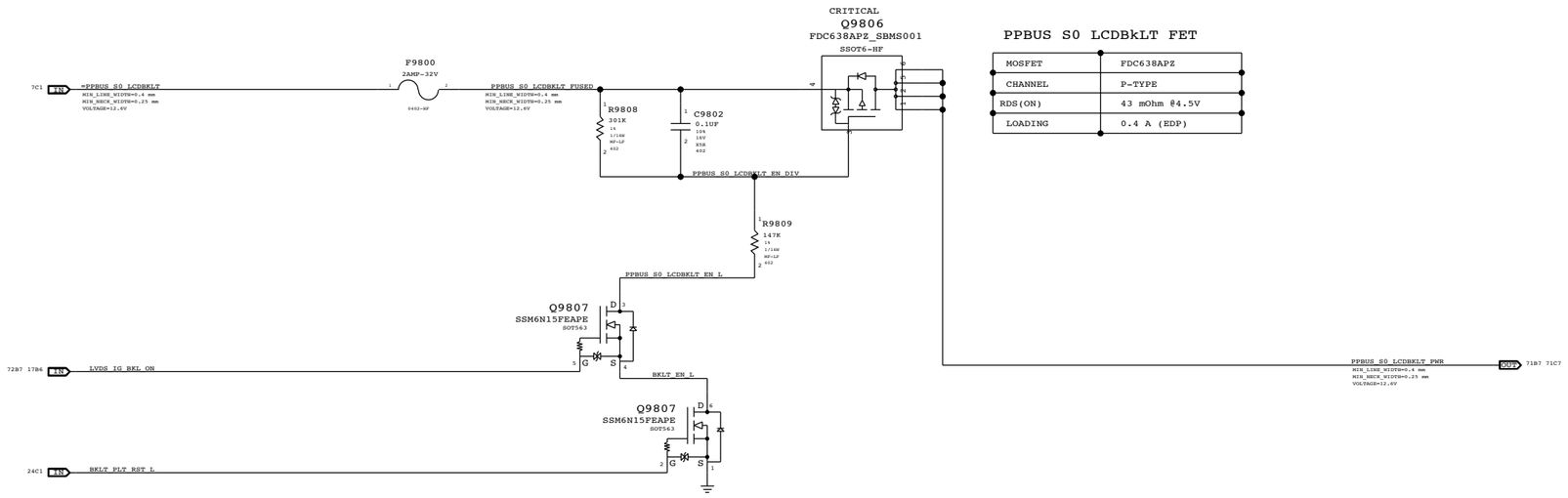
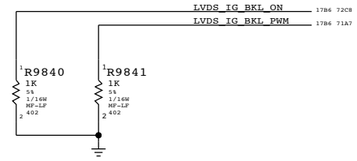
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC MASTER=YITE SYNC DATE=06/30/2008

PAGE TITLE

LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

BRANCH

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0> 9C4 13D3
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0> 9C4 13D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0> 9C4 13D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0> 9C4 13D6
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16> 9B4 9C4 13C3 13D3
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1> 9B4 13D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1> 9B4 13D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1> 9B4 13D6
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32> 9C2 13B3 13C3
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2> 9C2 13D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2> 9C2 13D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2> 9C2 13D6
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48> 9B2 9C2 13B3
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3> 9B2 13D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3> 9B2 13D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3> 9B2 13D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3> 9D8 13C6 13D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0> 9D8 13B6
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0> 9D8 13B6
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17> 9C8 9D8 13C6
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1> 9C8 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L 9D6 13B6
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L 9D6 13B6
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L 9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L 9D6 13B3
FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L 9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L 9D6 13B3
FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L 9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L 9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L 9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L 9D6 13B6
FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L 9D6 13C2 13A3
FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0> 9D6 13A4
FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L 9D6 13B6
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L 9C8 13A3
CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0> 8B2 9B4
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L 9C8 13B7
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L 9C8 13A3
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L 9D6 13A3
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR 9C8 13A3
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI 9B8 13A3
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L 9C5 13B6 41D4 62C8
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD 9B2 12C7 13A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L 9B8 13A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L 9C8 13A3
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L 9C6 13B7 41C4
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L 9B2 13A3
CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L 9B2 13A3
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L 9B2 13A3 62C7
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L 9B2 13A3
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD 13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND 13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC 13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND 13A6
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P 9B6 13B3
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N 9B6 13B3
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P 12C3 13B3
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N 12C3 13B3
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P 13A4
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N 13A4
CPU_IERR_L	CPU_50S		CPU_IERR_L 9D6
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR 20C7 62D8
(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR 62C7
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF 9B4 25B1
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 9B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 9B3
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 9B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 9B3
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI 9B6 9C6 12B3
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO 9B6 9C6 12B3
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS 9B6 9C6 12B3
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK 9A6 9C6 12B6
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L 9A6 9C6 12B3
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0> 9C6 12C6
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5> 9C5 12C6
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L 12C4
	CPU_50S	CPU_8MIL	CPU_VID<6..0> 10B6 62C7
	CPU_50S	CPU_8MIL	IMVP6_VID<6..0>
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 10B5 62A5
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 10A5 62A5
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N

FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

SYNC MASTER=T18 MLB SYNC DATE=01/04/2008

PAGE TITLE: CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14B5 26C5 26C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14A5 26D5 26D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14B5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14B5 14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14C5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14C5 26C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14B7 26C2 26C4 26D2 26D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14B7 26C2 26C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14B7 14C7 26B2 26B4 26C2 26C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14C7 26C2 26C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14C7 26B5 26B7 26C5 26C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14C7 14D7 26B5 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14D7 26B5 26B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14D7 26A5 26A7 26B5 26B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14A7 26C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14A7 26C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14B7 26B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14B7 26C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14B7 26B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14B7 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14B7 26B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14B7 26A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14D5 26C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14D5 26D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14D5 26C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14D5 26C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14D5 26B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14D5 26C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14D5 26C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14D5 26C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14D5 26B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14D5 26B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14D5 26B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14D5 26B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14D5 26B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14D5 26B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14D5 26A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14D5 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14B1 27C5 27C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14A1 27D5 27D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14B1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14B1 14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14C1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14C1 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14C1 27C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14B3 27C2 27C4 27D2 27D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14B3 27C2 27C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14B3 14C3 27C2 27C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14C3 27B2 27B4 27C2 27C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14C3 27B5 27B7 27C5 27C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14C3 14D3 27B5 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14D3 27B5 27B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14D3 27A5 27A7 27B5 27B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14A3 27C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14A3 27C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14B3 27C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14B3 27B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14B3 27B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14B3 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14B3 27B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14B3 27A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14D1 27C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14D1 27D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14D1 27C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14D1 27C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14D1 27B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14D1 27C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14D1 27B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14D1 27B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14D1 27B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14D1 27B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14D1 27B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14D1 27B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14D1 27A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14D1 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15C6

SYNC MASTER=T18_MLB SYNC_DATE=01/04/2008
PAGE TITLE: Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6D5 29C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6D5 29C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16B3 29C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16B3 29C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34C3
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16B3 34C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16B3 34C1
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6D5 29C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6D5 29C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	70C2 70C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	70C2 70C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17B6 69C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17B6 69C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	69C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	69C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	69C4 70C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	69D4 70C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17A6 23C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17A6 23C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6C7 68C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6C7 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6C7 17B3 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6C7 17B3 68C2
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	70C3 70C4 70C5
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	70C3 70C4 70C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17A3 23C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17A3 23C6
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	37A4
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	37A4
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	37B4
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	37B4
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_N	6A7 6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	37C4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19A6

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	12C3 18D7
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	18D2 18D7
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	18D2 18D7
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	18C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	18C5
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	18B3 40C8 42D3 42D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	18C3 40C8 42D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	18C3 24D4
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	18B3 24B4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	24B1 40C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	24B1 42D3
USB_EXTA	USB_90D	USB	USB_EXTA_P	19D3 38A8
	USB_90D	USB	USB_EXTA_N	19D3 38A8
	USB_90D	USB	USB_EXTA_MUXED_P	38C4
	USB_90D	USB	USB_EXTA_MUXED_N	38C4
	USB_90D	USB	CONN_USB_EXTA_P	38C3
	USB_90D	USB	CONN_USB_EXTA_N	38C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	19D3 29B5
	USB_90D	USB	USB_CAMERA_N	19D3 29B5
	USB_90D	USB	USB_CAMERA_CONN_P	6D5 29B7
	USB_90D	USB	USB_CAMERA_CONN_N	6D5 29B7
USB_BT	USB_90D	USB	USB_BT_P	19D3 29B5
	USB_90D	USB	USB_BT_N	19C3 29B5
	USB_90D	USB	CONN_USB2_BT_P	6D5 29B7
	USB_90D	USB	CONN_USB2_BT_N	6D5 29B7
USB_TPAD	USB_90D	USB	USB_TPAD_P	19D3 48B8
	USB_90D	USB	USB_TPAD_N	19D3 48B8
	USB_90D	USB	USB_TPAD_R_P	48B7
	USB_90D	USB	USB_TPAD_R_N	48B7
USB_IR	USB_90D	USB	USB_IR_P	19D3 39D7
	USB_90D	USB	USB_IR_N	19D3 39D7
USB_EXTB	USB_90D	USB	USB_EXTB_P	19C3 38A4
	USB_90D	USB	USB_EXTB_N	19C3 38B4
	USB_90D	USB	CONN_USB_EXTB_P	38B3
	USB_90D	USB	CONN_USB_EXTB_N	38B3
USB_SD	USB_90D	USB	USB_CARDREADER_P	19C3 30C7
	USB_90D	USB	USB_CARDREADER_N	19C3 30C7
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	19C4
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	12B6 20C3 43D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	12B6 20C3 43D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	20C3 43B8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	20C3 43B8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	20D2 52C7
	HDA_55S	HDA	HDA_BIT_CLK_R	20A7 20D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	20D2 52C7
	HDA_55S	HDA	HDA_SYNC_R	20A7 20D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	20A7 20D4
	HDA_55S	HDA	HDA_RST_L	20D2 52C7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	20D7 52C7
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	20D2 52C7
	HDA_55S	HDA	HDA_SDOUT_R	20A7 20D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	20C7
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	20B3 24B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24B1 40C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	20B3 42A5 42C8
	SPI_55S	SPI	SPI_CLK	51C5
	SPI_55S	SPI	SPI_ALT_CLK	42C5 42D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	20B3 42A5 42C7
	SPI_55S	SPI	SPI_MOSI	51C4
	SPI_55S	SPI	SPI_ALT_MOSI	42C5 42D5
SPI_MISO	SPI_55S	SPI	SPI_MISO	20B3 42A5 42B7
	SPI_55S	SPI	SPI_MISO_R	51C4
	SPI_55S	SPI	SPI_ALT_MISO	42B5 42D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	20B3 42B7
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17C3 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31B6 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17C3 31B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17D3 31B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17D6 31C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17D6 31C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17D6 31C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17D6 31B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17D3 31C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17D3 31B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17C3 31B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33B4 33C4 33C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33B4 33C4 33C5

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3ii_SPACING	2

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=ii_ohm_se	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	7

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	34B6 36C4
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	34C6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	34B6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	34B6 36C4
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	34B6 36B8
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	34B6 36B8

Port 2 Not Used

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
J23 SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	30C2
J24 SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	30C2
J25 SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	30C2
J26 SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	30C2
J27 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	30C2
J28 SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	30C2
J29 SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	30C2
J30 SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	30C2
J32 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	30C2
J31 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	30C2

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5V	SMB	SMBUS_SMC_A_S3_SCL	6C5 6D5 43D2
SMBUS_SMC_A_S3_SDA	SMB_5V	SMB	SMBUS_SMC_A_S3_SDA	6C5 6D5 43D2
SMBUS_SMC_B_S0_SCL	SMB_5V	SMB	SMBUS_SMC_B_S0_SCL	43C2
SMBUS_SMC_B_S0_SDA	SMB_5V	SMB	SMBUS_SMC_B_S0_SDA	43C2
SMBUS_SMC_0_S0_SCL	SMB_5V	SMB	SMBUS_SMC_0_S0_SCL	43D5
SMBUS_SMC_0_S0_SDA	SMB_5V	SMB	SMBUS_SMC_0_S0_SDA	43D5
SMBUS_SMC_BSA_SCL	SMB_5V	SMB	SMBUS_SMC_BSA_SCL	6A7 43C5
SMBUS_SMC_BSA_SDA	SMB_5V	SMB	SMBUS_SMC_BSA_SDA	6A7 43C5
SMBUS_SMC_MGMT_SCL	SMB_5V	SMB	SMBUS_SMC_MGMT_SCL	43B5
SMBUS_SMC_MGMT_SDA	SMB_5V	SMB	SMBUS_SMC_MGMT_SDA	43B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DIFFPAIR		CHGR_CSO_R_P 45A8 59B3
	DIFFPAIR		CHGR_CSO_R_N 45A8 59B3
	DIFFPAIR		CPUTHMSNS_D2_P 46C5
	DIFFPAIR		CPUTHMSNS_D2_N 46C5
	DIFFPAIR		CPU_THERMD_P 9C6 46D5
	DIFFPAIR		CPU_THERMD_N 9C6 46D5
	DIFFPAIR		ISNS_CPUVTT_P 45B7
	DIFFPAIR		ISNS_CPUVTT_N 45B7
	DIFFPAIR		ISNS_P1V5S0MCP_P
	DIFFPAIR		ISNS_P1V5S0MCP_N
	DIFFPAIR		ISNS_PVCORES0MCP_P
	DIFFPAIR		ISNS_PVCORES0MCP_N
	DIFFPAIR		MCPTHMSNS_D2_P 6C7 46B5
	DIFFPAIR		MCPTHMSNS_D2_N 6C7 46B5
	DIFFPAIR		MCP_THMDIODE_P 20C3 46B5
	DIFFPAIR		MCP_THMDIODE_N 20C3 46B5

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K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

SYNC MASTER=M97 MLB

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>