Watchmen/Cyborg AMD Schematics
Lucienne

2020-10-19
REV : X01

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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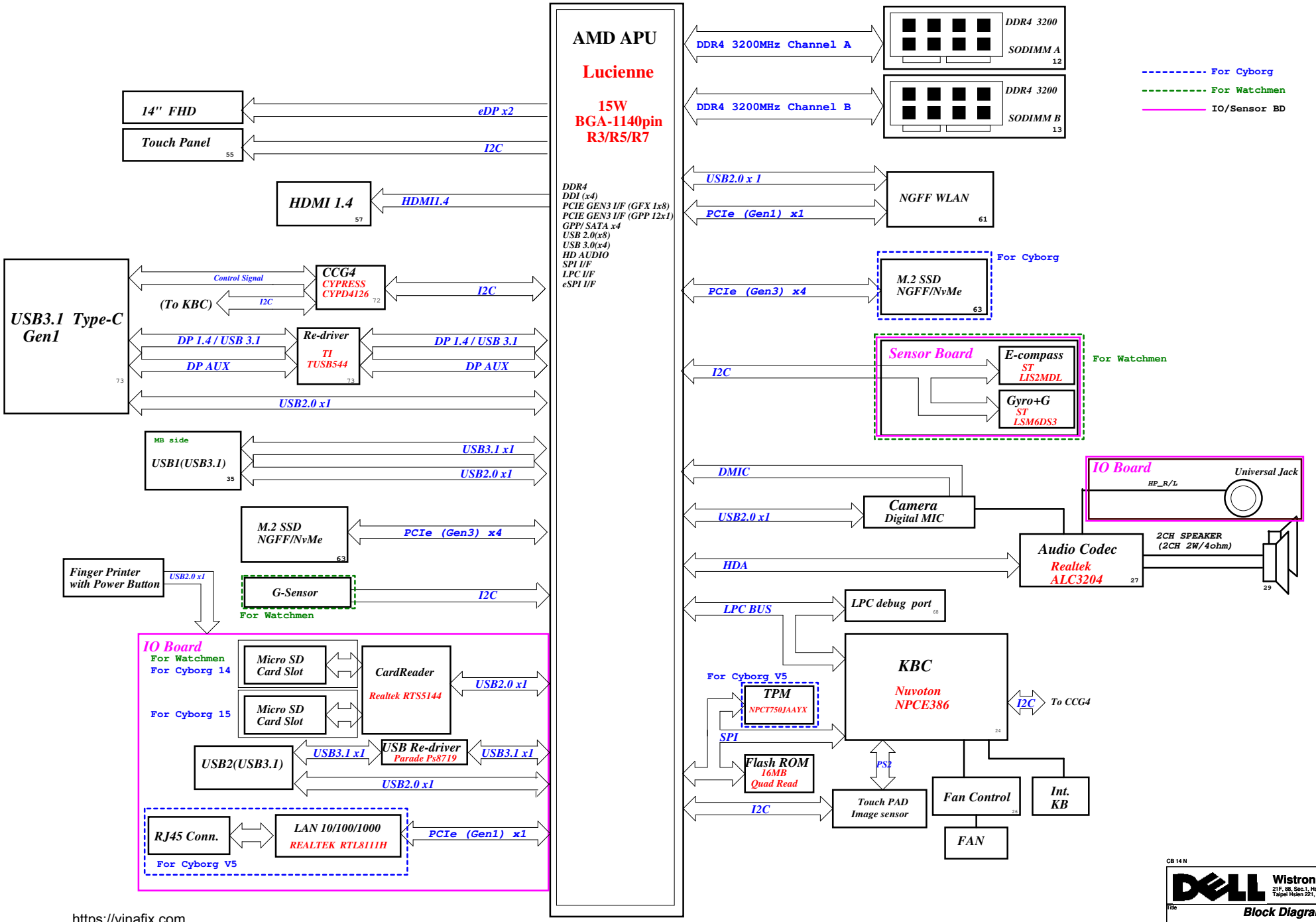
Project code:
PCB P/N:
Revision:

Watchmen/Cyborg AMD Block Diagram



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Title: Block Diagram

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SSID = PCH

SSD1 M.2 (PCIE)

[63] SSD_PCIE_RX_P0
[63] SSD_PCIE_RX_N0
[63] SSD_PCIE_RX_P1
[63] SSD_PCIE_RX_N1
[63] SSD_PCIE_RX_P2
[63] SSD_PCIE_RX_N2
[63] SSD_PCIE_RX_P3
[63] SSD_PCIE_RX_N3
[63] SSD_PCIE_TX_P0
[63] SSD_PCIE_TX_N0
[63] SSD_PCIE_TX_P1
[63] SSD_PCIE_TX_N1
[63] SSD_PCIE_TX_P2
[63] SSD_PCIE_TX_N2
[63] SSD_PCIE_TX_P3
[63] SSD_PCIE_TX_N3

SSD2 M.2 (PCIE)

[63] SSD_PCIE_RX_P8
[63] SSD_PCIE_RX_N8
[63] SSD_PCIE_RX_P9
[63] SSD_PCIE_RX_N9
[63] SSD_PCIE_RX_P10
[63] SSD_PCIE_RX_N10
[63] SSD_PCIE_RX_P11
[63] SSD_PCIE_RX_N11
[63] SSD_PCIE_TX_P8
[63] SSD_PCIE_TX_N8
[63] SSD_PCIE_TX_P9
[63] SSD_PCIE_TX_N9
[63] SSD_PCIE_TX_P10
[63] SSD_PCIE_TX_N10
[63] SSD_PCIE_TX_P11
[63] SSD_PCIE_TX_N11

LAN

[66] LAN_PCIE_RX_N
[66] LAN_PCIE_RX_P
[66] LAN_PCIE_TX_N
[66] LAN_PCIE_TX_P

WLAN

[61] WLAN_PCIE_RX_N
[61] WLAN_PCIE_RX_P
[61] WLAN_PCIE_TX_N
[61] WLAN_PCIE_TX_P

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GFX & GPP, 85Ω

CPU1B — 2 OF 13 — PCIE

G13 / F13	P_GFX_RXP0 / P_GFX_RXN0	P_GFX_TXP0 / P_GFX_TXN0	F4 / F2
J14 / H14	P_GFX_RXP1 / P_GFX_RXN1	P_GFX_TXP1 / P_GFX_TXN1	F3 / E4
G15 / F15	P_GFX_RXP2 / P_GFX_RXN2	P_GFX_TXP2 / P_GFX_TXN2	E1 / C1
J15 / K15	P_GFX_RXP3 / P_GFX_RXN3	P_GFX_TXP3 / P_GFX_TXN3	D5 / E6
H16 / J16	P_GFX_RXP4 / P_GFX_RXN4	P_GFX_TXP4 / P_GFX_TXN4	C6 / D6
F18 / G18	P_GFX_RXP5 / P_GFX_RXN5	P_GFX_TXP5 / P_GFX_TXN5	B6 / C7
J18 / K18	P_GFX_RXP6 / P_GFX_RXN6	P_GFX_TXP6 / P_GFX_TXN6	D8 / B8
H19 / G19	P_GFX_RXP7 / P_GFX_RXN7	P_GFX_TXP7 / P_GFX_TXN7	C8 / A8

M.2 SSD1 (PCIE)

Modify For Support Type 2 CPU 8/19

SSD_PCIE_RX_P0 / SSD_PCIE_RX_N0	G11 / F11	P_GPP_RXP0 / P_GPP_RXN0	P_GPP_TXP0 / P_GPP_TXN0
SSD_PCIE_RX_P1 / SSD_PCIE_RX_N1	J10 / H10	P_GPP_RXP1 / P_GPP_RXN1	P_GPP_TXP1 / P_GPP_TXN1
SSD_PCIE_RX_P2 / SSD_PCIE_RX_N2	G8 / F8	P_GPP_RXP2/SATA0_RXP / P_GPP_RXN2/SATA0_RXN	P_GPP_TXP2/SATA0_TXP / P_GPP_TXN2/SATA0_TXN
SSD_PCIE_RX_P3 / SSD_PCIE_RX_N3	G6 / F7	P_GPP_RXP3/SATA1_RXP / P_GPP_RXN3/SATA1_RXN	P_GPP_TXP3/SATA1_TXP / P_GPP_TXN3/SATA1_TXN

LAN_PCIE_RX_P / LAN_PCIE_RX_N	M9 / M8	P_GPP_RXP4 / P_GPP_RXN4	P_GPP_TXP4 / P_GPP_TXN4
WLAN_PCIE_RX_P 0R2J-2-GP 1 R301 2 WLAN_PCIE_RX_P_R / WLAN_PCIE_RX_N 0R2J-2-GP 1 R302 2 WLAN_PCIE_RX_N_R	L7 / L6	P_GPP_RXP5 / P_GPP_RXN5	P_GPP_TXP5 / P_GPP_TXN5
	K7 / K8	P_GPP_RXP6 / P_GPP_RXN6	P_GPP_TXP6 / P_GPP_TXN6
	H6 / H7	P_GPP_RXP7 / P_GPP_RXN7	P_GPP_TXP7 / P_GPP_TXN7

M.2 SSD2 (PCIE)

SSD_PCIE_RX_P8 / SSD_PCIE_RX_N8	L9 / L10	P_GPP_RXP8/SATA2_RXP / P_GPP_RXN8/SATA2_RXN	P_GPP_TXP8/SATA2_TXP / P_GPP_TXN8/SATA2_TXN
SSD_PCIE_RX_P9 / SSD_PCIE_RX_N9	K11 / J11	P_GPP_RXP9/SATA3_RXP / P_GPP_RXN9/SATA3_RXN	P_GPP_TXP9/SATA3_TXP / P_GPP_TXN9/SATA3_TXN
SSD_PCIE_RX_P10 / SSD_PCIE_RX_N10	J12 / H12	P_GPP_RXP10 / P_GPP_RXN10	P_GPP_TXP10 / P_GPP_TXN10
SSD_PCIE_RX_P11 / SSD_PCIE_RX_N11	J13 / K13	P_GPP_RXP11 / P_GPP_RXN11	P_GPP_TXP11 / P_GPP_TXN11

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PART 2 OF 13

Do Not Stuff

Do Not Stuff

M.2 SSD1 (PCIE)

L3 / L1	SSD_PCIE_TX_C_P0 / SSD_PCIE_TX_C_N0	C305 / C306	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P0 / SSD_PCIE_TX_N0
L4 / L2	SSD_PCIE_TX_C_P1 / SSD_PCIE_TX_C_N1	C307 / C308	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P1 / SSD_PCIE_TX_N1
M4 / M2	SSD_PCIE_TX_C_P2 / SSD_PCIE_TX_C_N2	C309 / C310	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P2 / SSD_PCIE_TX_N2
N3 / N1	SSD_PCIE_TX_C_P3 / SSD_PCIE_TX_C_N3	C311 / C312	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P3 / SSD_PCIE_TX_N3

LAN / WLAN

T2 / T4	LAN_PCIE_TX_C_P / LAN_PCIE_TX_C_N	C333 / C363	CB V / CB V	Do Not Stuff / Do Not Stuff	LAN_PCIE_TX_P / LAN_PCIE_TX_N
R1 / R3	WLAN_PCIE_TX_C_P / WLAN_PCIE_TX_C_N	C303 / C304	1	2 SCD1U16V2KX-3DLGP	WLAN_PCIE_TX_P / WLAN_PCIE_TX_N

M.2 SSD2 (PCIE)

K2 / K4	SSD_PCIE_TX_C_P8 / SSD_PCIE_TX_C_N8	C364 / C366	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P8 / SSD_PCIE_TX_N8
J4 / J2	SSD_PCIE_TX_C_P9 / SSD_PCIE_TX_C_N9	C365 / C368	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P9 / SSD_PCIE_TX_N9
H3 / H1	SSD_PCIE_TX_C_P10 / SSD_PCIE_TX_C_N10	C367 / C369	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P10 / SSD_PCIE_TX_N10
H4 / H2	SSD_PCIE_TX_C_P11 / SSD_PCIE_TX_C_N11	C370 / C371	1	2 SCD22U10V2KX-2-GP	SSD_PCIE_TX_P11 / SSD_PCIE_TX_N11

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Title: **CPU (PCIE/SATA)**

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(Blanking)

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Title

CPU (RSVD)

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

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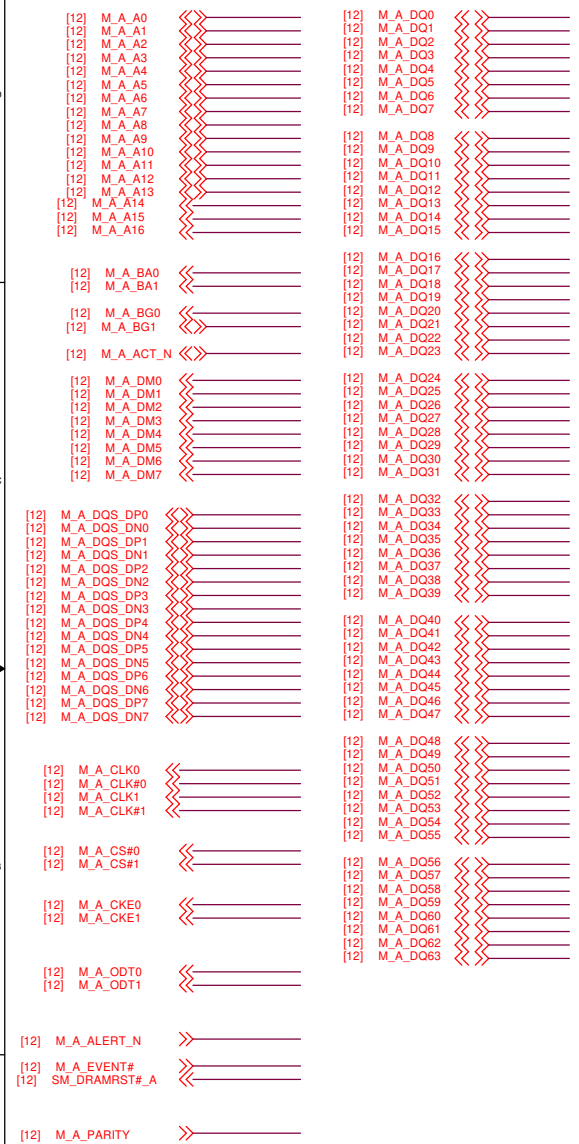
SSID = CPU



APU Type 2 does not support Channel A

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

DDR4
Channel A to SO-DIMM

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

CPU1A — MEMORY A — 1 OF 13

M_A_A0	AK26	MA_ADD0/RSVD
M_A_A1	AG24	MA_ADD1/RSVD
M_A_A2	AG23	MA_ADD2/MAB_CA0
M_A_A3	AG26	MA_ADD3/MAA_CA4
M_A_A4	AG27	MA_ADD4/MAA_CA5
M_A_A5	AF21	MA_ADD5/MAA_CA3
M_A_A6	AF22	MA_ADD6/MAA_CA2
M_A_A7	AF25	MA_ADD7/RSVD
M_A_A8	AF24	MA_ADD8/RSVD
M_A_A9	AE21	MA_ADD9/RSVD
M_A_A10	AL21	MA_ADD10/MAB_CS_L1
M_A_A11	AF27	MA_ADD11/MAA_CKE1
M_A_A12	AE23	MA_ADD12/MAA_CKE0
M_A_A13	AM23	MA_ADD13_BANK2/RSVD
M_A_A14	AM21	MA_WE_L_ADD14/MAB_CKE1
M_A_A15	AL27	MA_CAS_L_ADD15/RSVD
M_A_A16	AL24	MA_RAS_L_ADD16/MAB_CKE0
M_A_BA0	AL22	MA_BANK0/MAB_CS_L0
M_A_BA1	AK27	MA_BANK1/MAB_CA1
M_A_BG0	AE27	MA_BG0/MAA_CS_L1
M_A_BG1	AE26	MA_BG1/MAA_CS_L0
M_A_ACT_N	AD22	MA_ACT_L/RSVD
M_A_DM0	L27	MA_DM0/MAA_DM1
M_A_DM1	N23	MA_DM1/MAA_DM0
M_A_DM2	R27	MA_DM2/MAA_DM2
M_A_DM3	Y24	MA_DM3/MAA_DM3
M_A_DM4	AP27	MA_DM4/MAB_DM2
M_A_DM5	AW23	MA_DM5/MAB_DM3
M_A_DM6	AT21	MA_DM6/MAB_DM1
M_A_DM7	AV18	MA_DM7/MAB_DM0
	W24	RSVD_52
M_A_DQS_DP0	M25	MA_DQS_H0/MAA_DQS_H1
M_A_DQS_DN0	M24	MA_DQS_L0/MAA_DQS_L1
M_A_DQS_DP1	P22	MA_DQS_H1/MAA_DQS_H0
M_A_DQS_DN1	P21	MA_DQS_L1/MAA_DQS_L0
M_A_DQS_DP2	T24	MA_DQS_H2/MAA_DQS_H2
M_A_DQS_DN2	R24	MA_DQS_L2/MAA_DQS_L2
M_A_DQS_DP3	AA21	MA_DQS_H3/MAA_DQS_H3
M_A_DQS_DN3	Y21	MA_DQS_L3/MAA_DQS_L3
M_A_DQS_DP4	AP23	MA_DQS_H4/MAB_DQS_H2
M_A_DQS_DN4	AP24	MA_DQS_L4/MAB_DQS_L2
M_A_DQS_DP5	AW22	MA_DQS_H5/MAB_DQS_H3
M_A_DQS_DN5	AV22	MA_DQS_L5/MAB_DQS_L3
M_A_DQS_DP6	AT20	MA_DQS_H6/MAB_DQS_H1
M_A_DQS_DN6	AR20	MA_DQS_L6/MAB_DQS_L1
M_A_DQS_DP7	AR18	MA_DQS_H7/MAB_DQS_H0
M_A_DQS_DN7	AT18	MA_DQS_L7/MAB_DQS_L0
	Y26	RSVD_58
	Y27	RSVD_59
M_A_CLK0	AJ25	MA_CLK_H0/MAA_CKT
M_A_CLK#0	AJ24	MA_CLK_L0/MAA_CKC
M_A_CLK1	AJ22	MA_CLK_H1/MAB_CKT
M_A_CLK#1	AJ21	MA_CLK_L1/MAB_CKC
M_A_CS#0	AL25	MA_CS_L0/MAB_CA2
M_A_CS#1	AM26	MA_CS_L1/MAB_CA5
M_A_CKE0	AD24	MA_CKE0/MAA_CA1
M_A_CKE1	AD25	MA_CKE1/MAA_CA0
M_A_ODT0	AM24	MA_ODT0/MAB_CA3
M_A_ODT1	AM27	MA_ODT1/MAB_CA4
M_A_ALERT_N	AE24	MA_ALERT_L/TEST31A
M_A_EVENT#	AK23	MA_EVENT_L
SM_DRAMRST#_A	AD27	MA_RESET_L

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PART 1 OF 13

Do Not Stuff

Do Not Stuff

MA_DATA0/MAA_DATA8	K27	M_A_DQ0
MA_DATA1/MAA_DATA9	L26	M_A_DQ1
MA_DATA2/MAA_DATA13	N26	M_A_DQ2
MA_DATA3/MAA_DATA12	N27	M_A_DQ3
MA_DATA4/MAA_DATA11	G27	M_A_DQ4
MA_DATA5/MAA_DATA10	H27	M_A_DQ5
MA_DATA6/MAA_DATA15	M27	M_A_DQ6
MA_DATA7/MAA_DATA14	N24	M_A_DQ7
MA_DATA8/MAA_DATA0	L23	M_A_DQ8
MA_DATA9/MAA_DATA1	N21	M_A_DQ9
MA_DATA10/MAA_DATA5	T21	M_A_DQ10
MA_DATA11/MAA_DATA4	T22	M_A_DQ11
MA_DATA12/MAA_DATA7	M22	M_A_DQ12
MA_DATA13/MAA_DATA6	L24	M_A_DQ13
MA_DATA14/MAA_DATA2	R21	M_A_DQ14
MA_DATA15/MAA_DATA3	R23	M_A_DQ15
MA_DATA16/MAA_DATA17	P24	M_A_DQ16
MA_DATA17/MAA_DATA16	R26	M_A_DQ17
MA_DATA18/MAA_DATA21	T27	M_A_DQ18
MA_DATA19/MAA_DATA20	V27	M_A_DQ19
MA_DATA20/MAA_DATA19	P25	M_A_DQ20
MA_DATA21/MAA_DATA18	P27	M_A_DQ21
MA_DATA22/MAA_DATA23	V23	M_A_DQ22
MA_DATA23/MAA_DATA22	T25	M_A_DQ23
MA_DATA24/MAA_DATA30	W22	M_A_DQ24
MA_DATA25/MAA_DATA31	Y23	M_A_DQ25
MA_DATA26/MAA_DATA26	AC24	M_A_DQ26
MA_DATA27/MAA_DATA27	AC23	M_A_DQ27
MA_DATA28/MAA_DATA28	V21	M_A_DQ28
MA_DATA29/MAA_DATA29	W21	M_A_DQ29
MA_DATA30/MAA_DATA24	AA24	M_A_DQ30
MA_DATA31/MAA_DATA25	AA22	M_A_DQ31
MA_DATA32/MAB_DATA17	AP26	M_A_DQ32
MA_DATA33/MAB_DATA16	AN24	M_A_DQ33
MA_DATA34/MAB_DATA21	AR25	M_A_DQ34
MA_DATA35/MAB_DATA20	AU26	M_A_DQ35
MA_DATA36/MAB_DATA19	AN25	M_A_DQ36
MA_DATA37/MAB_DATA18	AN27	M_A_DQ37
MA_DATA38/MAB_DATA23	AR27	M_A_DQ38
MA_DATA39/MAB_DATA22	AU27	M_A_DQ39
MA_DATA40/MAB_DATA30	AV25	M_A_DQ40
MA_DATA41/MAB_DATA31	AW25	M_A_DQ41
MA_DATA42/MAB_DATA26	AV20	M_A_DQ42
MA_DATA43/MAB_DATA27	AW20	M_A_DQ43
MA_DATA44/MAB_DATA28	AV27	M_A_DQ44
MA_DATA45/MAB_DATA29	AW26	M_A_DQ45
MA_DATA46/MAB_DATA24	AU21	M_A_DQ46
MA_DATA47/MAB_DATA25	AW21	M_A_DQ47
MA_DATA48/MAB_DATA11	AT22	M_A_DQ48
MA_DATA49/MAB_DATA10	AP21	M_A_DQ49
MA_DATA50/MAB_DATA14	AN19	M_A_DQ50
MA_DATA51/MAB_DATA15	AN18	M_A_DQ51
MA_DATA52/MAB_DATA12	AU23	M_A_DQ52
MA_DATA53/MAB_DATA13	AR22	M_A_DQ53
MA_DATA54/MAB_DATA9	AN20	M_A_DQ54
MA_DATA55/MAB_DATA8	AP19	M_A_DQ55
MA_DATA56/MAB_DATA6	AT19	M_A_DQ56
MA_DATA57/MAB_DATA7	AW18	M_A_DQ57
MA_DATA58/MAB_DATA2	AU16	M_A_DQ58
MA_DATA59/MAB_DATA3	AW16	M_A_DQ59
MA_DATA60/MAB_DATA4	AW19	M_A_DQ60
MA_DATA61/MAB_DATA5	AU19	M_A_DQ61
MA_DATA62/MAB_DATA1	AP16	M_A_DQ62
MA_DATA63/MAB_DATA0	AT16	M_A_DQ63

RSVD_54	W27
RSVD_53	W25
RSVD_68	AC25
RSVD_69	AC27
RSVD_49	V26
RSVD_48	V24
RSVD_63	AA27
RSVD_62	AA25

MA_PAROUT/RSVD — AK24 — M_A_PARITY

1D2V_S3

M_DDR4
M_LPDDR4
AN21
AN22

CB 14 N

Follow CRB 20190423

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Title: **CPU (DDR4_CHA)**

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SSID = CPU

[13] M_B_A0
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[13] M_B_DQ60
[13] M_B_DQ61
[13] M_B_DQ62
[13] M_B_DQ63

[13] M_B_PARITY

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

DDR4
Channel B to SO-DIMM

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

CPU1I — 9 OF 13 — MEMORY B

M_B_A0	AM29	MB_ADD0/RSVD
M_B_A1	AH31	MB_ADD1/RSVD
M_B_A2	AJ30	MB_ADD2/MBB_CA0
M_B_A3	AH29	MB_ADD3/MBA_CA4
M_B_A4	AG32	MB_ADD4/MBA_CA5
M_B_A5	AG30	MB_ADD5/MBA_CA3
M_B_A6	AG31	MB_ADD6/MBA_CA2
M_B_A7	AF30	MB_ADD7/RSVD
M_B_A8	AG29	MB_ADD8/RSVD
M_B_A9	AF29	MB_ADD9/RSVD
M_B_A10	AM30	MB_ADD10/MBB_CS_L1
M_B_A11	AF31	MB_ADD11/MBA_CKE1
M_B_A12	AE32	MB_ADD12/MBA_CKE0
M_B_A13	AP30	MB_ADD13_BANK2/RSVD
M_B_A14	AP31	MB_WE_L_ADD14/MBB_CKE1
M_B_A15	AP29	MB_CAS_L_ADD15/RSVD
M_B_A16	AN29	MB_RAS_L_ADD16/MBB_CKE0
M_B_BA0	AN31	MB_BANK0/MBB_CS_L0
M_B_BA1	AM32	MB_BANK1/MBB_CA1
M_B_BG0	AD29	MB_BG0/MBA_CS_L1
M_B_BG1	AD31	MB_BG1/MBA_CS_L0
M_B_ACT_N	AD30	MB_ACT_L/RSVD
M_B_DM0	C30	MB_DM0/MBA_DM1
M_B_DM1	H32	MB_DM1/MBA_DM0
M_B_DM2	M29	MB_DM2/MBA_DM2
M_B_DM3	T29	MB_DM3/MBA_DM3
M_B_DM4	AU30	MB_DM4/MBB_DM2
M_B_DM5	BD28	MB_DM5/MBB_DM3
M_B_DM6	BB23	MB_DM6/MBB_DM1
M_B_DM7	BD20	MB_DM7/MBB_DM0
	W31	RSVD_57

DM, DQ & DQS on the same layer

M_B_DQS_DP0	E29	MB_DQS_H0/MBA_DQS_H1
M_B_DQS_DN0	D28	MB_DQS_L0/MBA_DQS_L1
M_B_DQS_DP1	J31	MB_DQS_H1/MBA_DQS_H0
M_B_DQS_DN1	J29	MB_DQS_L1/MBA_DQS_L0
M_B_DQS_DP2	N30	MB_DQS_H2/MBA_DQS_H2
M_B_DQS_DN2	M31	MB_DQS_L2/MBA_DQS_L2
M_B_DQS_DP3	T30	MB_DQS_H3/MBA_DQS_H3
M_B_DQS_DN3	T31	MB_DQS_L3/MBA_DQS_L3
M_B_DQS_DP4	AU29	MB_DQS_H4/MBB_DQS_H2
M_B_DQS_DN4	AU31	MB_DQS_L4/MBB_DQS_L2
M_B_DQS_DP5	BA27	MB_DQS_H5/MBB_DQS_H3
M_B_DQS_DN5	BB27	MB_DQS_L5/MBB_DQS_L3
M_B_DQS_DP6	BC23	MB_DQS_H6/MBB_DQS_H1
M_B_DQS_DN6	BA23	MB_DQS_L6/MBB_DQS_L1
M_B_DQS_DP7	BC20	MB_DQS_H7/MBB_DQS_H0
M_B_DQS_DN7	BA20	MB_DQS_L7/MBB_DQS_L0
	Y32	RSVD_61
	Y30	RSVD_60

M_B_CLK0	AJ31	MB_CLK_H0/MBA_CKT
M_B_CLK#0	AK30	MB_CLK_L0/MBA_CKC
M_B_CLK1	AK32	MB_CLK_H1/MBB_CKT
M_B_CLK#1	AL31	MB_CLK_L1/MBB_CKC
M_B_CS#0	AN30	MB_CS_L0/MBB_CA2
M_B_CS#1	AR31	MB_CS_L1/MBB_CA5
M_B_CKE0	AC31	MB_CKE0/MBA_CA1
M_B_CKE1	AC29	MB_CKE1/MBA_CA0
M_B_ODT0	AP32	MB_ODT0/MBB_CA3
M_B_ODT1	AR29	MB_ODT1/MBB_CA4
M_B_ALERT_N	AE30	MB_ALERT_L/TEST31B
M_B_EVENT#	AL30	MB_EVENT_L
SM_DRAMRST#_B	AC32	MB_RESET_L

FP6 REV 0.92
PART 9 OF 13

Do Not Stuff

DM, DQ & DQS on the same layer

MB_DATA0/MBA_DATA8	C27	M_B_DQ0
MB_DATA1/MBA_DATA9	A28	M_B_DQ1
MB_DATA2/MBA_DATA13	F29	M_B_DQ2
MB_DATA3/MBA_DATA12	F31	M_B_DQ3
MB_DATA4/MBA_DATA11	B27	M_B_DQ4
MB_DATA5/MBA_DATA10	D27	M_B_DQ5
MB_DATA6/MBA_DATA15	E32	M_B_DQ6
MB_DATA7/MBA_DATA14	F30	M_B_DQ7
MB_DATA8/MBA_DATA0	H31	M_B_DQ8
MB_DATA9/MBA_DATA1	H30	M_B_DQ9
MB_DATA10/MBA_DATA5	K31	M_B_DQ10
MB_DATA11/MBA_DATA4	L30	M_B_DQ11
MB_DATA12/MBA_DATA7	G30	M_B_DQ12
MB_DATA13/MBA_DATA6	H29	M_B_DQ13
MB_DATA14/MBA_DATA2	K30	M_B_DQ14
MB_DATA15/MBA_DATA3	K29	M_B_DQ15
MB_DATA16/MBA_DATA21	N32	M_B_DQ16
MB_DATA17/MBA_DATA22	N29	M_B_DQ17
MB_DATA18/MBA_DATA20	P30	M_B_DQ18
MB_DATA19/MBA_DATA19	L32	M_B_DQ19
MB_DATA20/MBA_DATA17	L31	M_B_DQ20
MB_DATA21/MBA_DATA16	M30	M_B_DQ21
MB_DATA22/MBA_DATA18	L29	M_B_DQ22
MB_DATA23/MBA_DATA23	N31	M_B_DQ23
MB_DATA24/MBA_DATA30	R30	M_B_DQ24
MB_DATA25/MBA_DATA31	R32	M_B_DQ25
MB_DATA26/MBA_DATA26	V30	M_B_DQ26
MB_DATA27/MBA_DATA27	V32	M_B_DQ27
MB_DATA28/MBA_DATA28	P29	M_B_DQ28
MB_DATA29/MBA_DATA29	P31	M_B_DQ29
MB_DATA30/MBA_DATA25	U31	M_B_DQ30
MB_DATA31/MBA_DATA24	U29	M_B_DQ31
MB_DATA32/MBB_DATA16	AT29	M_B_DQ32
MB_DATA33/MBB_DATA17	AU32	M_B_DQ33
MB_DATA34/MBB_DATA21	AW31	M_B_DQ34
MB_DATA35/MBB_DATA20	AW30	M_B_DQ35
MB_DATA36/MBB_DATA19	AR30	M_B_DQ36
MB_DATA37/MBB_DATA18	AT31	M_B_DQ37
MB_DATA38/MBB_DATA23	AV30	M_B_DQ38
MB_DATA39/MBB_DATA22	AW29	M_B_DQ39
MB_DATA40/MBB_DATA29	AY29	M_B_DQ40
MB_DATA41/MBB_DATA28	AY32	M_B_DQ41
MB_DATA42/MBB_DATA24	BC27	M_B_DQ42
MB_DATA43/MBB_DATA25	BB26	M_B_DQ43
MB_DATA44/MBB_DATA27	BC25	M_B_DQ44
MB_DATA45/MBB_DATA26	BA25	M_B_DQ45
MB_DATA46/MBB_DATA30	BB30	M_B_DQ46
MB_DATA47/MBB_DATA31	BA28	M_B_DQ47
MB_DATA48/MBB_DATA11	BA24	M_B_DQ48
MB_DATA49/MBB_DATA10	BC24	M_B_DQ49
MB_DATA50/MBB_DATA14	BC22	M_B_DQ50
MB_DATA51/MBB_DATA15	BA22	M_B_DQ51
MB_DATA52/MBB_DATA12	BB25	M_B_DQ52
MB_DATA53/MBB_DATA13	BD25	M_B_DQ53
MB_DATA54/MBB_DATA9	BB22	M_B_DQ54
MB_DATA55/MBB_DATA8	BD22	M_B_DQ55
MB_DATA56/MBB_DATA4	BA21	M_B_DQ56
MB_DATA57/MBB_DATA5	BC21	M_B_DQ57
MB_DATA58/MBB_DATA2	BC18	M_B_DQ58
MB_DATA59/MBB_DATA3	BB18	M_B_DQ59
MB_DATA60/MBB_DATA6	BB20	M_B_DQ60
MB_DATA61/MBB_DATA7	BB21	M_B_DQ61
MB_DATA62/MBB_DATA1	BB19	M_B_DQ62
MB_DATA63/MBB_DATA0	BA18	M_B_DQ63
	W30	
RSVD_56	W29	
RSVD_55	AA30	
RSVD_65	AB29	
RSVD_67	V29	
RSVD_50	V31	
RSVD_51	AA29	
RSVD_64	AA31	
RSVD_66		
MB_PAROUT/RSVD	AM31	M_B_PARITY

Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc. M_PAROUT	M_RESET_L	M_EVENT_L	M_ALERT	

Do Not Stuff

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR4_CHB)**

Size: A3 | Document Number: **Watchmen/Cyborg AMD** | Rev: **X00**

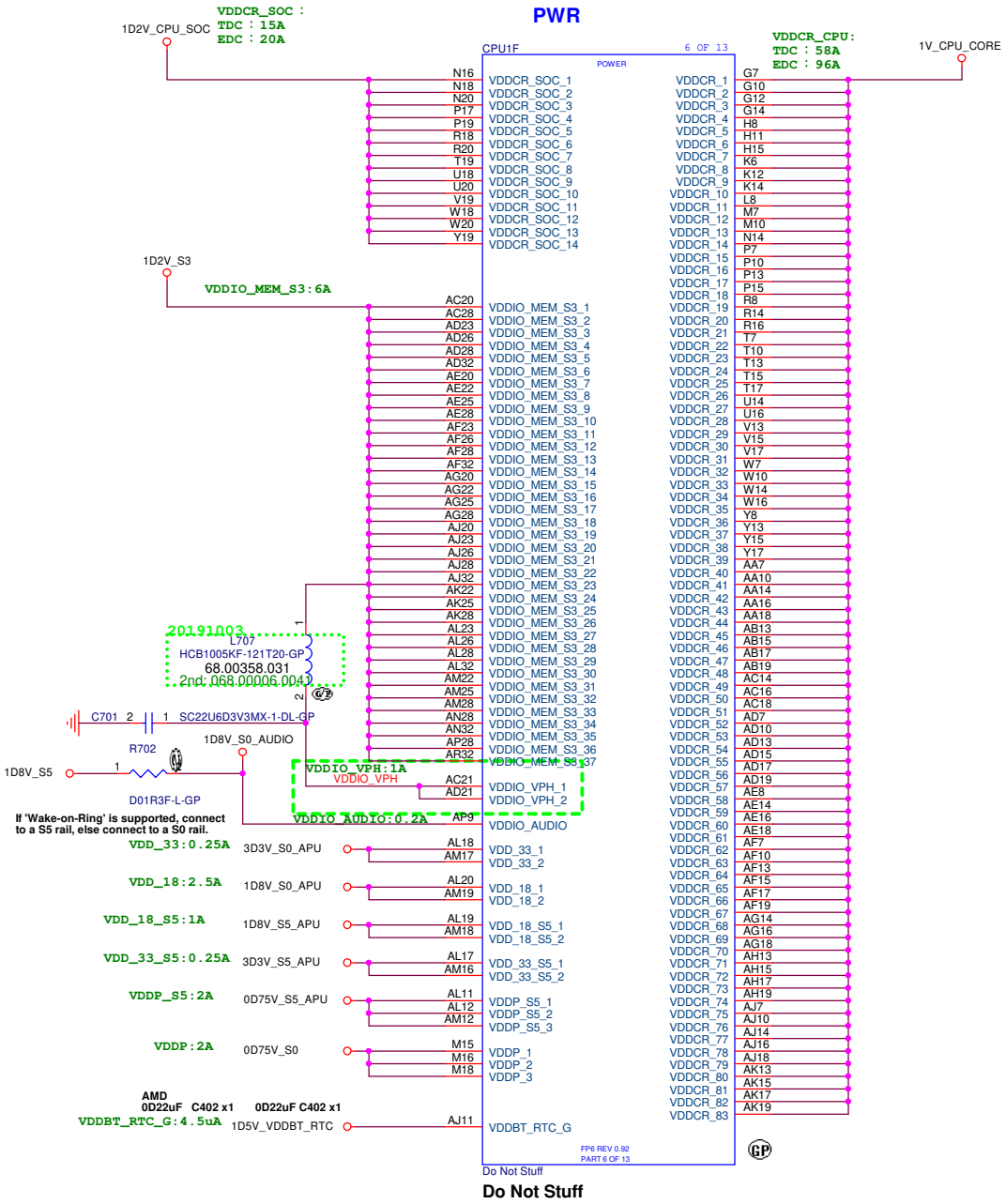
Date: Friday, October 23, 2020 | Sheet 6 of 106

Table 7. FP6 Processor Voltage Supply Currents for AMD Family 17h Models 60h-6Fh Processors

NOTICE: *To identify the proper requirements for AMD Family 17h Models 60h and AMD Family 17 Models 68h, see notes 8 and 9.*								
Supply [1]	**Nominal Voltage at Pkg Ball (V) [2]**	**Condition**	**SYSTEM_CONFIGURATION**					
			1 10 W	**2 15 W**	**3 25 W**	**4 35 W**	**5 45 W**	**6 54 W**
VDDCR_VDD	Variable (0.6-1.55) [5]	TDC [3]	20	33	44	51	58	
		EDC	34	50[8]/70[9]	70	90	96	
		Max Loadstep [4]	29	43[8]/65[9]	65	76	84	
VDDCR_SOC	Variable (0.6-1.55) [5]	TDC [3]	10	13		15		
		EDC	13	17		20		
		Max Loadstep [4]	10	13		15		
VDDIO_MEM_S3 [6]	1.10	TDC	6.00					
	1.20	TDC	6.00					
VDDIO_VPH [7]	1.20	TDC	1.00					
	1.80	TDC	1.00					
VDDP	0.75	TDC	2.00					
VDDP_S5	0.75	TDC	2.00					
VDD_18	1.80	TDC	2.50					
VDD_18_S5	1.80	TDC	1.00					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	3.00	TDC	4.5 µA					

Notes:

1. *These specifications are for the processor only. For voltage supplies that are used by other components on the platform, consult documentation for that component to ensure that both specifications are met.*
2. *A voltage supply must be capable of providing any specified nominal voltage based on processor configuration. An OPN may only support a subset of nominal voltages. Lower nominal voltages may limit performance relative to higher nominal voltages.*
3. *Current may exceed TDC for variable, limited periods of time, however the average current over any ~100 ms moving time period will be held to less than or equal to the TDC limit.*



CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (ALL POWER)***

Size: A3 | Document Number: **Watchmen/Cyborg AMD** | Rev: **X00**

Date: Friday, October 23, 2020 | Sheet 7 of 106

SSID = PCH

DISPLAY/SVI/JTAG/TEST

APU Type I(CZ): 1D8V
APU Type II(CZ-L): 3D3V

eDP

[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P1
[55] eDP_TX_CPU_N1
[24] eDP_BLON
[55] eDP_DIGON
[55] eDP_VARY_BL
[55] eDP_AUX_CPU_P
[55] eDP_AUX_CPU_N
[55] eDP_HPD_CPU

HDMI

[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N2
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P3
[57] HDMI_DDI_TX_N3
[57] HDMI_SCL_CPU
[57] HDMI_SDA_CPU
[57] HDMI_DET_CPU

TYPE-C DP

[73] DP2_AUXP
[73] DP2_AUXN
[72,73] CPU_DP_HPD

HDT

[68] APU_TDI
[68] APU_TDO
[68] APU_TCK
[68] APU_TMS
[68] APU_TRST#
[68] APU_DBREQ#
[68,72] RST#_CPU
[46,68] SVID_PWRGD
[26] THERMTRIP#_CPU
[24,44,46] H_PROCHOT#

SVID

[46] SVID_CLK_CPU
[46] SVID_DATA_CPU
[46] SVID_ALERT_N_CPU
[46] VDDNB_SENSE
[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[52] VDDP_S5_SENSE
[52] VDDP_S0_SENSE
[52] VSS_SENSEB
[24] SML1_SMBDATA
[24] SML1_SMBCLK
[24,26,44,46] VCORE_PWRGD

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Follow CRB 20190423

DisplayPort	Device
0	eDP
1	HDMI out

1D8V_S5
R838 1 2 4K7R2J-2-GP RST#_CPU
R839 1 2 4K7R2J-2-GP SVID_PWRGD
20191008

HDT&HDT+:NEED TO POP ON EV/EVT stage

1D8V_S5
HDT PIN Pull High Resistor
ASM if HDT CONN is needs of use
R815 1 2 1KR1F-GP APU_TDI
R816 1 2 1KR1F-GP APU_TCK
R817 1 2 1KR1F-GP APU_TRST#
R818 1 2 1KR1F-GP APU_DBREQ#
20191204
R805 1 1KR2J-1-GP APU_TMS

3D3V_S0
RN801
1 8 SIC_CPU
2 7 SID_CPU
3 6 ALERT#_CPU
4 5 H_PROCHOT#
SRN1KJ-4-GP

C821 1 DY 2 Do Not Stuff RST#_CPU
C822 1 DY 2 Do Not Stuff SVID_PWRGD

HDMI: High=enable

1D8V_S0
R837 1KR2F-3-GP
DP_STEREOSYNC_APU
R808 DY Do Not Stuff

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

CPU1C
3 OF 13
DISPLAY/SVI2/JTAG/TEST

eDP

eDP_TX_CPU_P0 D11 DP0_TXP0
eDP_TX_CPU_N0 B11 DP0_TXN0
eDP_TX_CPU_P1 C11 DP0_TXP1
eDP_TX_CPU_N1 A11 DP0_TXN1
D10 DP0_TXP2
B10 DP0_TXN2
D9 DP0_TXP3
B9 DP0_TXN3

DP_BLON A22 eDP_BLON
DP_DIGON D23 eDP_DIGON
DP_VARY_BL C23 eDP_VARY_BL
DP0_AUXP D12 eDP_AUX_CPU_P
DP0_AUXN B12 eDP_AUX_CPU_N
DP0_HPD C12 eDP_HPD_CPU

HDMI

HDMI_DDI_TX_P2 G23 DP1_TXP0
HDMI_DDI_TX_N2 H23 DP1_TXN0
HDMI_DDI_TX_P1 F22 DP1_TXP1
HDMI_DDI_TX_N1 G22 DP1_TXN1
HDMI_DDI_TX_P0 G21 DP1_TXP2
HDMI_DDI_TX_N0 H21 DP1_TXN2
HDMI_DDI_TX_P3 F20 DP1_TXP3
HDMI_DDI_TX_N3 G20 DP1_TXN3

DP1_AUXP J20 HDMI_SCL_CPU
DP1_AUXN K20 HDMI_SDA_CPU
DP1_HPD L21 HDMI_DET_CPU

TYPE-C DP

DP2_AUXP L19 DP2_AUXP
DP2_AUXN M19 DP2_AUXN
DP2_HPD M20 CPU_DP_HPD
DP3_AUXP M14
DP3_AUXN L14
DP3_HPD L16
DP_STEREOSYNC B23 DP_STEREOSYNC_APU
R814 1 2 100KR2J-1-GP

APU Type I 1D8V
APU Type II 3D3V

PINOUT	Description
DP_BLON	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

DisplayPort	Device
0	eDP
1	HDMI
2	
3	DP

HDT

APU_TDI AP3 TDI
APU_TDO AU1 TDO
APU_TCK AR2 TCK
APU_TMS AU3 TMS
APU_TRST# AR4 TRST_L
APU_DBREQ# AT2 DBREQ_L

HDT CONN PIN#12 RST#_CPU AW3 RESET#
HDT CONN PIN#10 SVID_PWRGD AW4 PWROK

SMB1

SIC_CPU B22 SIC
SID_CPU D22 SID
ALERT#_CPU C22 ALERT_L
THERMTRIP#_CPU AN9 THERMTRIP_L
H_PROCHOT# B25 PROCHOT_L

an output signal as overtemperature condition

SVID

SVID_CLK_CPU D25 SVC0
SVID_DATA_CPU C25 SVD0
SVID_ALERT_N_CPU A25 SVT0

FP6 REV 0.92
PART 3 OF 13

Do Not Stuff

C879 DY Do Not Stuff
C889 DY Do Not Stuff
C890 DY Do Not Stuff

3D3V_S0
Q808
SID_CPU 1 6 SML1_SMBDATA
2 5
SIC_CPU 3 4
2N7002KDW-1-GP SML1_SMBCLK

75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C
4th = 075.07002.0A7C

TEST4 BB6 TEST4 1 TP808 Do Not Stuff
TEST5 BD5 TEST5 1 TP807 Do Not Stuff
TEST6 AG12
TEST14 G25 TEST14_APU 1 TP810 Do Not Stuff
TEST15 K25 TEST15_APU 1 TP811 Do Not Stuff
TEST16 F25 TEST16_APU 1 TP812 Do Not Stuff
TEST17 F26 TEST17_APU 1 TP813 Do Not Stuff
TEST31 H26 TEST31_APU 1 TP802 Do Not Stuff
TEST41 AK9 TEST41 1 TP809 Do Not Stuff
ANALOGIO_0 AK21
ANALOGIO_1 AG21

0D75V_S0
SMU_ZVDDP P3 SMU_ZVDDP R812 1 2 196R2F-GP SMU_ZVDD

VDDP_S5_SENSE AK7 VDDP_S5_SENSE
VDDP_SENSE AK12 VDDP_S0_SENSE
VDDCR_SOC_SENSE J23 VDDNB_SENSE_APU R806 1 2 0R2J-2-GP VDDNB_SENSE
VDDCR_SENSE K22 VCCCORE_SENSE_APU R807 1 2 0R2J-2-GP VCCCORE_SENSE
VDDIO_MEM_S3_SENSE J21 VDDIO_MEM_S3_SENSE TP896
A00 Change 0 ohm to short pad
VSS_SENSE_A J22 VSS_SENSE_APU R809 1 2 0R2J-2-GP VSSCORE_SENSE
VSS_SENSE_B AJ12 VSS_SENSEB TP801 Do Not Stuff

VDDNB_SENSE R801 1 DY 2 Do Not Stuff 1D2V_CPU_SOC
VCCCORE_SENSE R802 1 DY 2 Do Not Stuff 1V_CPU_CORE
VSSCORE_SENSE R804 1 DY 2 Do Not Stuff

CB 14 N

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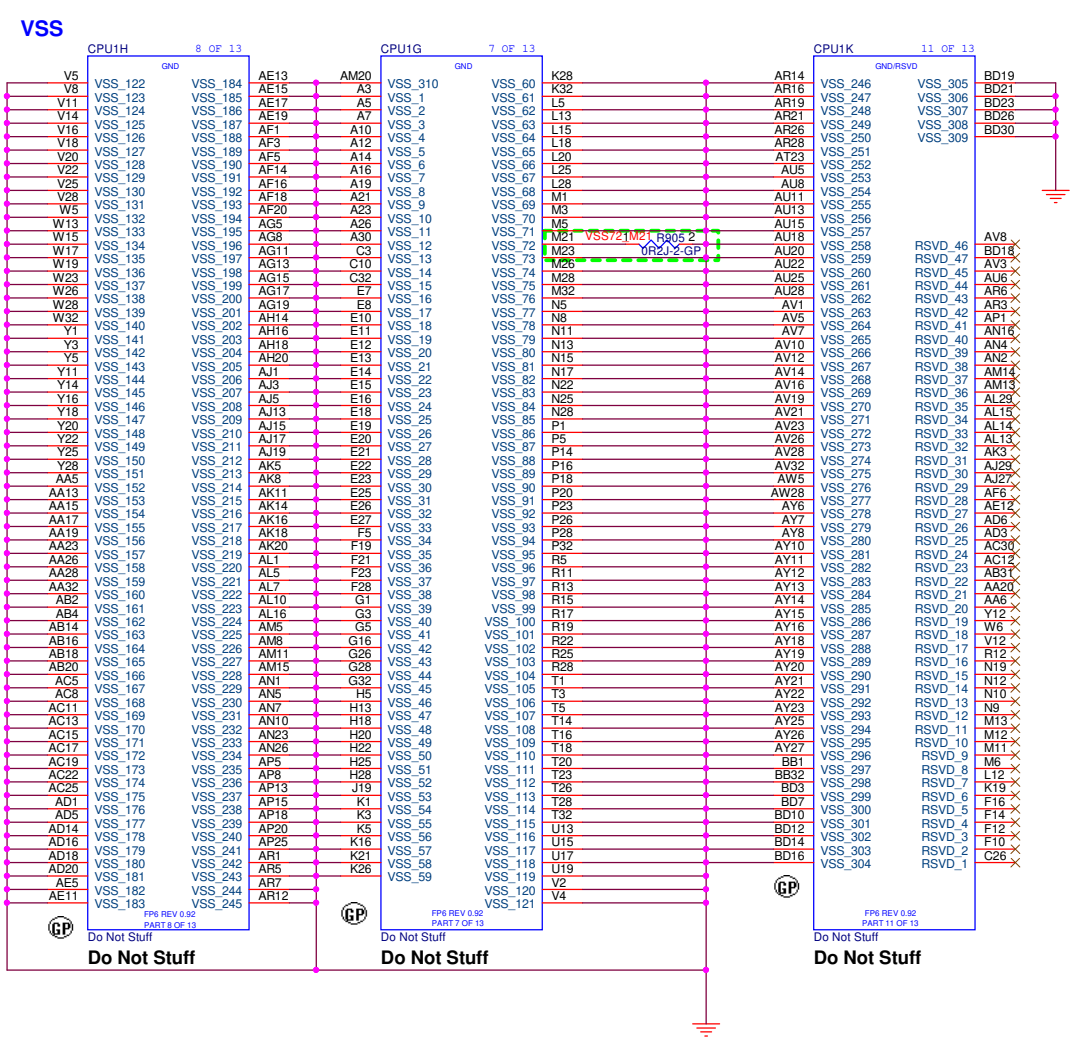
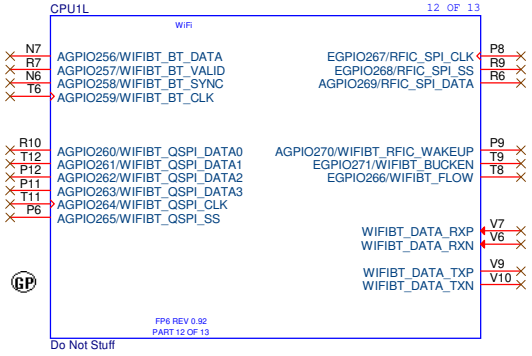
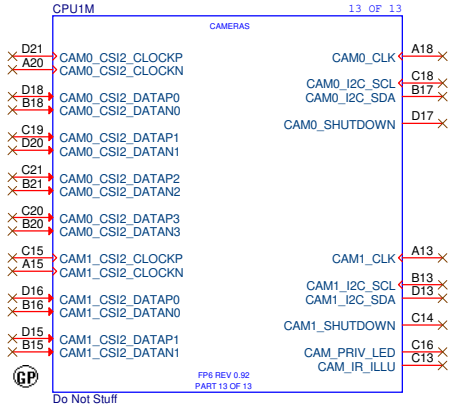
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DP/SVID/HDT/TEST)
Size: A3
Document Number: Watchmen/Cyborg AMD
Rev: X00
Date: Friday, October 23, 2020
Sheet 8 of 106







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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 9 of 106

APU Caps

SSID = PWR.Plane.Regulator_CPU CAP

1V_CPU_CORE

AMD
VDDCR
22uF C603 x30
180pF C402 x1

Follow Eva request add 22u to 20 pcs

PC1001 SC47U6D3V3MX-2-GP
PC1002 SC47U6D3V3MX-2-GP
PC1003 SC47U6D3V3MX-2-GP
PC1004 SC47U6D3V3MX-2-GP
PC1005 SC47U6D3V3MX-2-GP
PC1006 SC47U6D3V3MX-2-GP
PC1008 SC47U6D3V3MX-2-GP
PC1010 SC47U6D3V3MX-2-GP
PC1011 SC47U6D3V3MX-2-GP

PC1012 SC47U6D3V3MX-2-GP
PC1013 SC47U6D3V3MX-2-GP
PC1014 SC47U6D3V3MX-2-GP
PC1015 SC47U6D3V3MX-2-GP
PC1016 SC47U6D3V3MX-2-GP
PC1019 SC47U6D3V3MX-2-GP
PC1020 SC47U6D3V3MX-2-GP
PC1021 SC47U6D3V3MX-2-GP

SPACE LIMIT DELETE

DY PC1083 Do Not Stuff

PC1023 SC47U6D3V3MX-2-GP
PC1024 SCD1U25V2KX-1-DL-GP
PC1025 SCD1U25V2KX-1-DL-GP

SPACE LIMIT DELETE

DY PC1081 Do Not Stuff
DY PC1082 Do Not Stuff

C1018 SC220P50V2KX-3DLGP
PC1084 SC47U6D3V3MX-2-GP
PC1085 SC47U6D3V3MX-2-GP
DY PC5462 Do Not Stuff
DY PC5463 Do Not Stuff

20200930

1V_CPU_CORE

Stitching Caps

C1050 SCD01U25V2KX-3DLGP
C1051 SCD01U25V2KX-3DLGP
C1052 SCD01U25V2KX-3DLGP

AMD
VDDCR_SOC
22uF C603 x15
1uF C402 x1
180pF C402 x1

Follow Eva request add 22u to 12 pcs

1D2V_CPU_SOC

C1001 SC1U10V2KX-1DLGP
C1046 SC220P50V2KX-3DLGP

20200930

PC1047 SC22U6D3V3MX-1-DL-GP
PC1048 SC22U6D3V3MX-1-DL-GP
PC1049 SC22U6D3V3MX-1-DL-GP
PC1050 SC22U6D3V3MX-1-DL-GP
PC1055 SC22U6D3V3MX-1-DL-GP
PC1057 SC22U6D3V3MX-1-DL-GP
PC1056 SC22U6D3V3MX-1-DL-GP
PC1064 SC22U6D3V3MX-1-DL-GP
PC1063 SC22U6D3V3MX-1-DL-GP
PC1065 SC22U6D3V3MX-1-DL-GP

PC1066 SC22U6D3V3MX-1-DL-GP
PC1067 SC22U6D3V3MX-1-DL-GP
PC1017 SC47U6D3V3MX-2-GP
PC1018 SC47U6D3V3MX-2-GP
PC1007 SC47U6D3V3MX-2-GP

20191018

DY PC5459 Do Not Stuff
DY PC5460 Do Not Stuff
DY PC5461 Do Not Stuff

1D2V_S3

AMD
VDDIO_MEM_S3
22uF C603 x9
1uF C402 x2
0D22uF C402 x4
180pF C402 x2

PC1051 SC22U6D3V3MX-1-DL-GP
PC1052 Do Not Stuff
PC1053 Do Not Stuff
PC1054 Do Not Stuff
C1055 SCD22U10V2KX-2-GP
C1056 SCD22U10V2KX-2-GP
C1057 SCD22U10V2KX-2-GP
C1058 SCD22U10V2KX-2-GP
PC1060 Do Not Stuff
PC1061 Do Not Stuff

WM CB15

PC1058 SC22U6D3V3MX-1-DL-GP
PC1059 SC22U6D3V3MX-1-DL-GP
PC1062 Do Not Stuff

WM CB15

C1002 SC1U10V2KX-1DLGP
C1003 SC1U10V2KX-1DLGP
C1068 SC220P50V2KX-3DLGP
C1072 SC220P50V2KX-3DLGP
C1088 SC220P50V2KX-3DLGP

20200930
20200930
20200930

0D75V_S0

AMD
VDDP
22uF C603 x2
1uF C402 x8
180pF C402 x1

C1005 SC1U10V2KX-1DLGP
C1004 SC1U10V2KX-1DLGP
C1007 SC1U10V2KX-1DLGP
C1006 SC1U10V2KX-1DLGP
C1009 SC1U10V2KX-1DLGP
C1008 SC1U10V2KX-1DLGP
C1011 SC1U10V2KX-1DLGP
C1010 SC1U10V2KX-1DLGP

PC1078 SC22U6D3V3MX-1-DL-GP
PC1080 SC22U6D3V3MX-1-DL-GP
C1078 SC220P50V2KX-3DLGP

20200930

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER CAP1)

Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 10 of 106

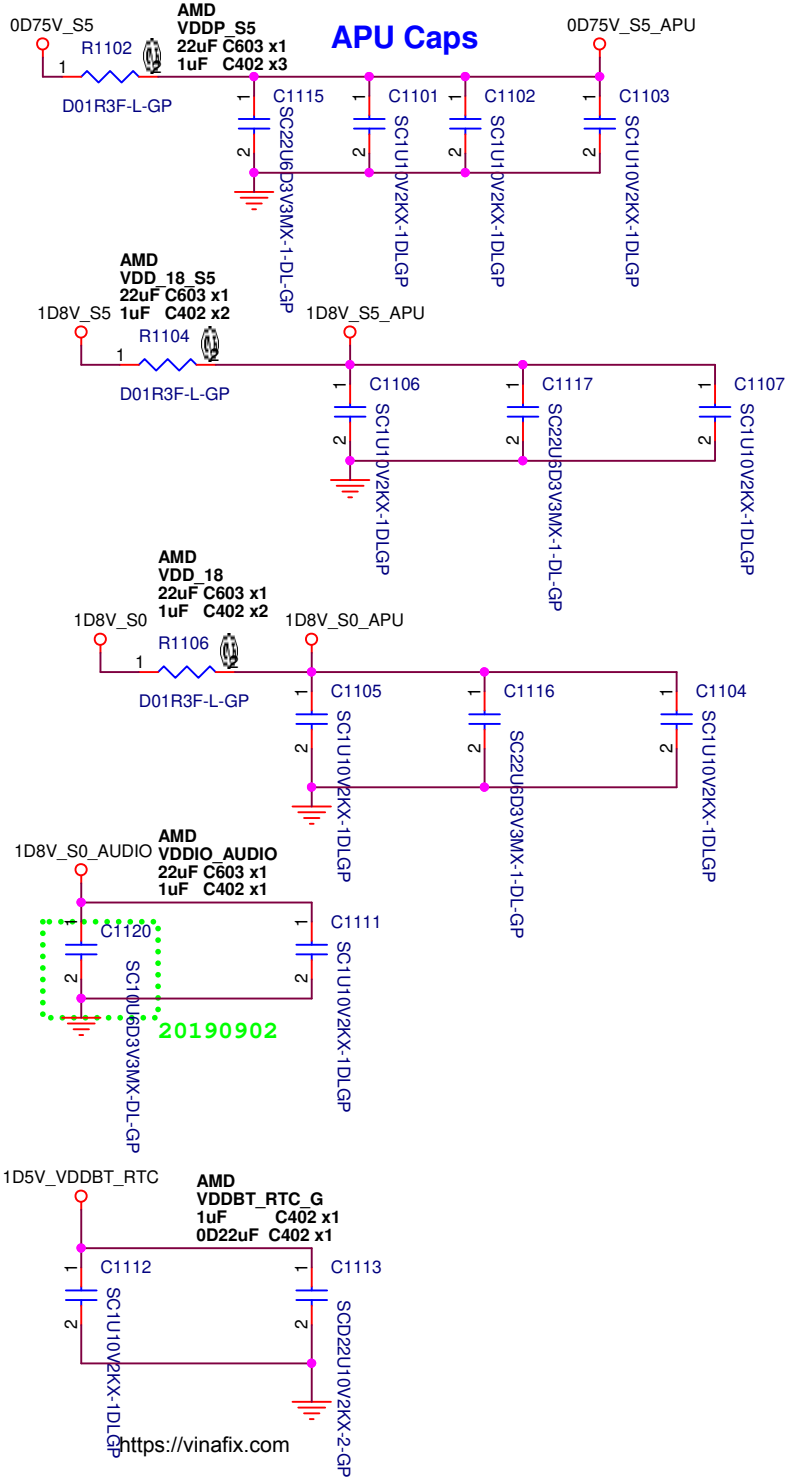


Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3[1, 2]	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 µF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 µF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 µF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

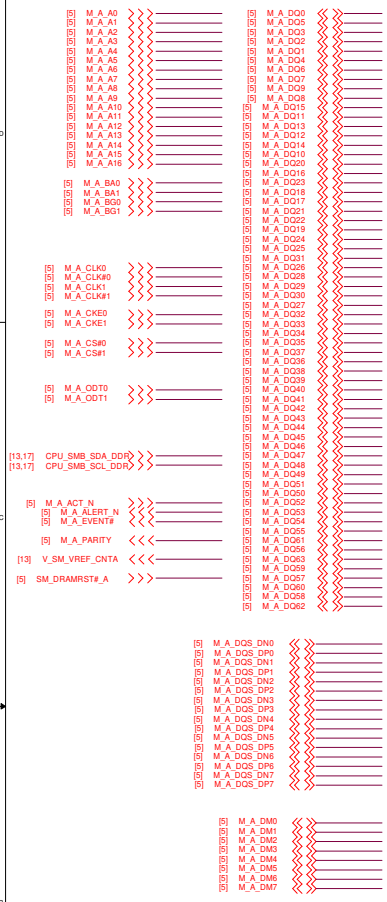
Title: ***CPU (POWER CAP2)***

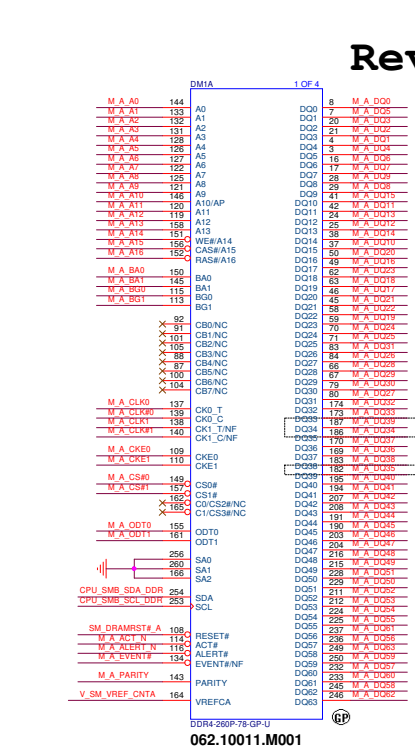
Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

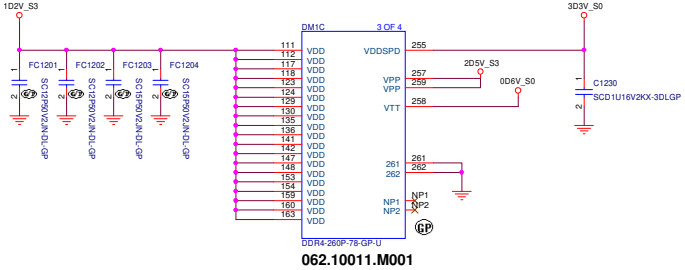
Date: Friday, October 23, 2020 Sheet 11 of 106

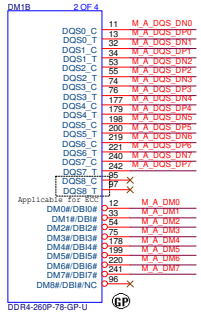
Main Func = DDR4 SODIMM

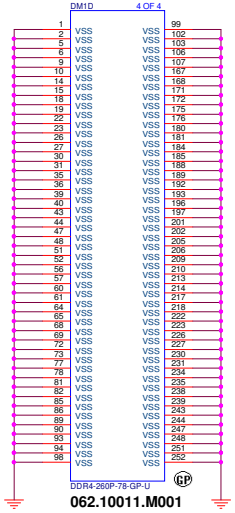
Reverse Type

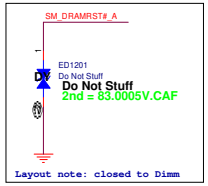


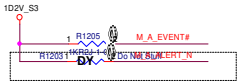


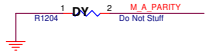






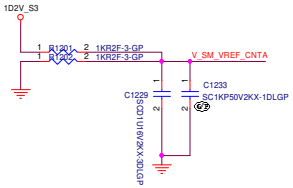






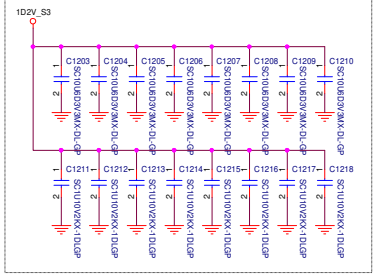
DIMM_VREFCA

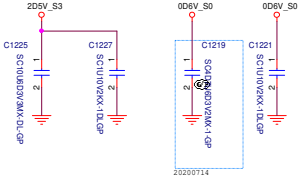
Layout Note :
VREFCA traces should
have width=20 mil;
spacing=20 mil



Layout Note :
Place these Caps near DIMM1

10uF x8
1uF x8





SPD Address of DIMMA

SPD SA2	0
SPD SA1	0
SPD SA0	0

CB 14 N

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Taipei Hsien 221, Taiwan, R.O.C.

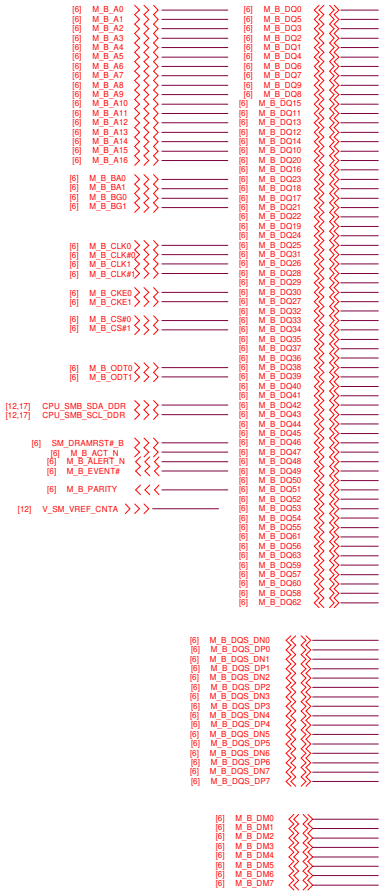
Title: DDR (DDR4-SODIMM1_CHA)

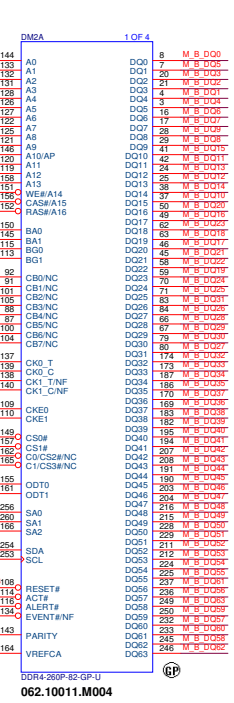
Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

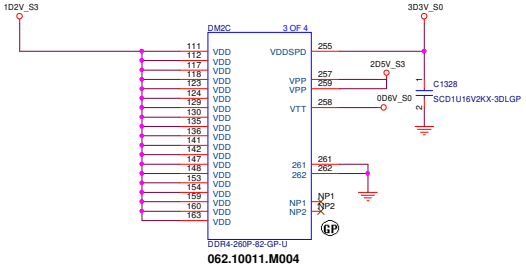
Date: Friday, October 23, 2020 | Sheet 12 of 106

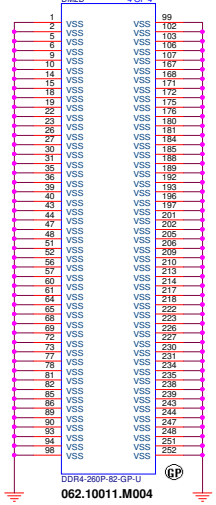
Main Func = DDR4 SODIMM

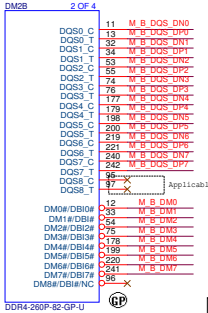
Standard Type

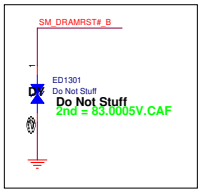


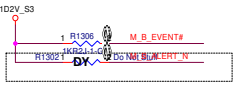








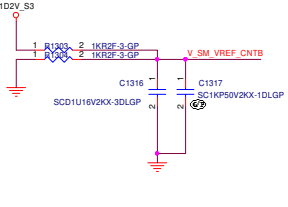




Layout note: closed to Dimm

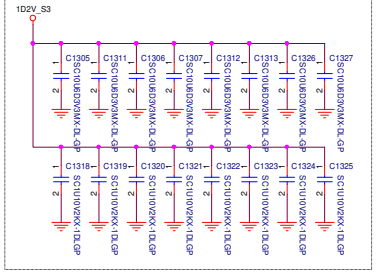
DIMM_VREFCA

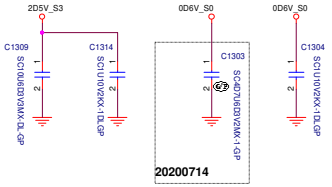
Layout Note :
VREFCA traces should have width=20 mil; spacing=20 mil



Layout Note :
Place these Caps near DIMM2

10uF x8
1uF x8





SPD Address of DIMMB

SPD SA2	0
SPD SA1	1
SPD SA0	0

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-SODIMM2_CHB)

Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 13 of 106

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CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR (RSVD)*

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 14 of 106

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR (RSVD)*

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

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SSD

[63] SSD_CLK_CPU_P
[63] SSD_CLK_CPU_N
[63] SSD_CLKREQ_CPU_N

SSD2

[63] SSD2_CLK_CPU_P
[63] SSD2_CLK_CPU_N
[63] SSD2_CLKREQ_CPU_N

WLAN

[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] WLAN_CLKREQ_CPU_N

LAN

[66] LAN_CLK_CPU_P
[66] LAN_CLK_CPU_N
[66] LAN_CLKREQ_CPU_N

SPI

[20,25] SPI_CLK_ROM
[24,25,91] SPI_SO_ROM
[24,25,91] SPI_SI_ROM
[25] SPI_WP_ROM
[25] SPI_HOLD_ROM
[24,25] SPI_CS_ROM_N0
[91] SPI_CS_ROM_N2

LPC

[24] ECSMI#_KBC
[24,68] LPC_AD_CPU_P0
[24,68] LPC_AD_CPU_P1
[24,68] LPC_AD_CPU_P2
[24,68] LPC_AD_CPU_P3
[24] LPC_CLK_KBC
[24] LPC_CLKRUN#_CPU
[68] LPC_CLK_DBG
[24] LPC_SERIRQ_CPU
[24,68] LPC_FRAME#_CPU
[24,68,91] LPC_RST#

[17,55] DBC_PANEL_EN
[24] ECSCI#_KBC

[24] KBRST#
[24] SPI_Q1601

[65] KB_DET#

[17] UMA_ID2

HC WLAN

[61] APU_UART_PTX_DRX
[61] APU_UART_PRX_DTX
[61] APU_UART_PTX_DRX_RTS#
[61] APU_UART_PRX_DTX_CTS#

[61] SUS_CLK_CPU

CLK/SATA/USB/SPI/LPC

P_GPP CLK port	Device
0	SSD
1	WLAN
2	NC
3	GPU
4	LAN
5	SSD2
6	NC

LPCCLK1/EGPIO75
CLK_REQ5_L
If unused,
enable internal pull up or pull down by software.

GFX & GPP CLK, 85Ω
SATA & USB, 90Ω

CPU1E — 5 OF 13 — CLK/LPC/EMMC/SD/SPI/eSPI/UART

SSD_CLKREQ_CPU_N AR13 — CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
WLAN_CLKREQ_CPU_N AP10 — CLK_REQ1_L/AGPIO115
UMA_ID2 AR15 — CLK_REQ2_L/AGPIO116
PEG_CLKREQ0_CPU_N AT14 — CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
LAN_CLKREQ_CPU_N AN11 — CLK_REQ4_L/OSCIN/EGPIO132
SSD2_CLKREQ_CPU_N AN13 — CLK_REQ5_L/EGPIO120
EGPIO121 AN15 — CLK_REQ6_L/EGPIO121

SSD: SSD_CLK_CPU_P AF11 — GPP_CLK0P; SSD_CLK_CPU_N AF12 — GPP_CLK0N
WLAN: WLAN_CLK_CPU_P AG4 — GPP_CLK1P; WLAN_CLK_CPU_N AG2 — GPP_CLK1N
AG3 — GPP_CLK2P; AG1 — GPP_CLK2N
AF2 — GPP_CLK3P; AF4 — GPP_CLK3N
LAN: LAN_CLK_CPU_P AH2 — GPP_CLK4P; LAN_CLK_CPU_N AH4 — GPP_CLK4N
SSD2: SSD2_CLK_CPU_P AJ2 — GPP_CLK5P; SSD2_CLK_CPU_N AJ4 — GPP_CLK5N
AF8 — GPP_CLK6P/WIFIBT_CLKP; AF9 — GPP_CLK6N/WIFIBT_CLKN
AK1 — X48M_OSC
XTL_48M_X1_CPU BB3 — X48M_X1
XTL_48M_X2_CPU BA5 — X48M_X2
AG10 — RSVD_71; AG9 — RSVD_70
SUS_CLK_CPU AW10 — RTCCLK
XTL_32K_X1_CPU AY1 — X32K_X1
XTL_32K_X2_CPU AY4 — X32K_X2

EGPIO70
LPC_PD_L/AGPIO21
LAD0/ESPI1_DATA0/EGPIO104
LAD1/ESPI1_DATA1/EGPIO105
LAD2/ESPI1_DATA2/EGPIO106
LAD3/ESPI1_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
LPC_RST_L/AGPIO32
AGPIO68
LPC_PME_L/AGPIO22
SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/EGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108
SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DATA
SPI_DO
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29
EGPIO141/UART0_RXD
EGPIO143/UART0_TXD
EGPIO142/UART0_RTS_L/UART1_RXD
EGPIO140/UART0_CTS_L/UART1_TXD
AGPIO144/SHUTDOWN_L/UART0_INTR

FP6 REV 0.92
PART 5 OF 13

Do Not Stuff

3D3V_S0

ECSMI#_KBC 1 R1606 10KR2J-3-GP

AW14 EGPIO70 — TP1601 Do Not Stuff
BB13 EC_SMI_APU 1 R1602 0R2J-2-GP ECSMI#_KBC
BA16 LPC_AD_CPU_P0_R1 R1625 10R2F-L-GP LPC_AD_CPU_P0
BA15 LPC_AD_CPU_P1_R1 R1627 10R2F-L-GP LPC_AD_CPU_P1
BC13 LPC_AD_CPU_P2_R1 R1626 10R2F-L-GP LPC_AD_CPU_P2
BB14 LPC_AD_CPU_P3_R1 R1629 10R2F-L-GP LPC_AD_CPU_P3
BB15 LPC_CLK_CPU_P0 1 R1605 2 22R2J-2-GP LPC_CLK_KBC
BD13 LPC_CLKRUN#_CPU
BA12 LPC_CLK_CPU_P1 1 R1609 2 22R2J-2-GP LPC_CLK_DBG
BC15 LPC_SERIRQ_CPU
BA13 LPC_FRAME#_CPU
BC12 A_RST#_APU 1 R1612 2 33R2J-2-GP LPC_RST#
AU12 DBC_PANEL_EN
AP4 EC_SCI#_R R16161 20R2J-2-GP ECSCI#_KBC

to KBC

BA11
BB11
AT15 KBRST#
BC11 LDRQ0#
BC10 SPI_CLK_CPU
BA10 SPI_SO_CPU R16131 2 0R2J-2-GP SPI_SO_ROM
BB8 SPI_SI_CPU R16141 2 0R2J-2-GP SPI_SI_ROM
BA9 SPI_WP_CPU R16211 2 0R2J-2-GP SPI_WP_ROM
BC8 SPI_HOLD_CPU R16221 2 0R2J-2-GP SPI_HOLD_ROM
BD11 SPI_CS_CPU_N0 R16071 2 0R2J-2-GP SPI_CS_ROM_N0
BC9 AGPIO30
BB10
BD8 SPI_CS_ROM_N2

BA17 APU_UART_PRX_DTX_R R16401 2 0R2J-2-GP APU_UART_PRX_DTX
BC16 APU_UART_PTX_DRX_R R16411 2 0R2J-2-GP APU_UART_PTX_DRX
BD15 APU_UART_PTX_DRX_RTS#_R R16421 2 0R2J-2-GP APU_UART_PTX_DRX_RTS#
BC17 APU_UART_PRX_DTX_CTS#_R R16431 2 0R2J-2-GP APU_UART_PRX_DTX_CTS#
BB16 KB_DET# R16201 10KR2J-3-GP 3D3V_S0

DB_170410
Follow BIOS request for AMD
LPC interface debug

3D3V_S0
R1631 1 10KR2J-3-GP LAN_CLKREQ_CPU_N
R1630 1 DY Do Not Stuff PEG_CLKREQ0_CPU_N
R1604 1 10KR2J-3-GP LPC_CLKRUN#_CPU
R1634 1 10KR2J-3-GP SSD_CLKREQ_CPU_N
R1653 1 10KR2J-3-GP SSD2_CLKREQ_CPU_N
R1633 1 10KR2J-3-GP WLAN_CLKREQ_CPU_N
R1698 1 10KR2J-3-GP LDRQ0#
R1646 1 DY Do Not Stuff EGPIO121

1D8V_S5
DY R1632 Do Not Stuff SPI_SI_ROM

Remove R1635 R1636 for layout space

DY R1688 Do Not Stuff AGPIO30
Close to R1612
C1603 1 2 SC150P50V1KX-1-GP LPC_RST#
EC1614 1 DY 2 Do Not Stuff LPC_CLK_KBC
0201>>0402 20200714
EC1615 1 DY 2 Do Not Stuff LPC_CLK_DBG
20201005
C1616 1 DY 2 Do Not Stuff LPC_SERIRQ_CPU

Q1601 PJA138KA-GP
SPI_CLK_ROM → D; S → SPI_CLK_CPU; G → SPI_Q1601
084.00138.0A31
2nd = 084.00138.0A31

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1615 1 20MR2J-GP
X1602
XTAL-32D768KHZ-98-GP
082.30003.0301
2nd = 082.30003.0191
C1601 SC12P50V2JN-DL-GP
C1602 SC15P50V2JN-DL-GP

Note:
C1612 and C1613 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.

XTL_48M_X1_CPU R1623 33R1J-GP XTL_48M_X1
R1618 1MR2F-GP
C1612 SC8D2P50VCN-2-GP
1st = 82.30026.371
2nd = 082.30028.0091
X1601 XTAL-48MHZ-36-GP
XTL_48M_X2_CPU R1624 33R1J-GP XTL_48M_X2
C1613 SC8D2P50VCN-2-GP

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/LPC/SPI/UART)
Size: A3
Document Number: Watchmen/Cyborg AMD
Rev: X00
Date: Friday, October 23, 2020
Sheet 16 of 106

SSID = PCH

CLK/SATA/USB/SPI/LPC

SO-DIMM

[12,13] CPU_SMB_SCL_DDR

[12,13] CPU_SMB_SDA_DDR

Panel

[55] CPU_I2C_SCL_TS_R

[55] CPU_I2C_SDA_TS_R

Touch Pad

[65,66] CPU_I2C_SCL_P3

[65,66] CPU_I2C_SDA_P3

[27] HDA_SDIN0_CPU

[27] HDA_BITCLK_CODEC_R

[27] HDA_SYNC_CODEC

[27] HDA_SDOUT_CODEC

[24] KB_DISABLE

[45,52,54] 3V_5V_PWRGD

[61] WAKE_L

[24,51,66] APU_SLP_S5#

[24,40,51,52] APU_SLP_S3#

[61] UART_WAKE#_APU

[24,61,63,91] PLT_RST#

[24] PM_PWRBTN#

[24,40] SYS_PWRGD

[20] SYS_RST#_CPU

[29] SPK_ID

[24] AC_PRES_KBC

[16,24] ECSMI#_KBC

[24] PSP_2

[24] PSP_1

[65] TP_WAKE_CPU#

[91] PRQA#

[64] SATA_ACT#

[27] SPKR

[65] KB_LED_BL_DET

[55] TOUCH_PANEL_PD#

[55] TOUCH_PANEL_INTR#

[63] PCIE_SSD_RST

[55] TOUCH_PANEL_DET#

[16] UMA_ID2

[16,55] DBC_PANEL_EN

[70] GSENSOR_INT_R

[55] DMIC_CLK_EDP

[55] DMIC_DATA_EDP

[61] DOUT_BT_M2

[61] BCLK_BT_M2

[61] LRCLK_BT_M2

[61] SDIN_BT_M2

to PCIE

20190802

Sensor INT

3D3V_S5

1.8V/3.3V_S0

1.8V/3.3V_S5

AGPIO:1.8V/3.3V_S5 /DEVSJP :3.3V_S5

SATA_ACT:3.3V/AGPIO:1.8V/3.3V_S5

A00 Change 0 ohm to short pad 20181219

A00 Change 0 ohm to short pad 20181219

A00 Change 0 ohm to short pad 20181219

SMB0 PU S0 PWR Rail (to SO-DIMM)

SMB1 PU S5 PWR Rail (to Touch PAD)

Straps	
	LFRAME_L LPCCLK0/EGPIO74 LPCCLK1/EGPIO75 RTCCLK SYS_RESET_L/AGPIO1 BLINK/USB_OC7_L/AGPIO11 AGPIO3
S5 PWR Rail S0 PWR Rail	AGPIO0 - EGPIO42 AGPIO64 - EGPIO148
SMB0, 3D3V_S0 SMB1, 3D3V_S5	DIMM KBC 3D3V_S5 Thermal 3D3V_S0 GSENSOR for HDD Protect
APU Type I only APU type II only	AGPIO8 AGPIO40

PCIE_RST1_L/EGPIO27
AGPIO40
LPC_PD_L/SD_CMD/AGPIO21
If unused,
enable internal pull up or pull down by software.

Cyborg N / Cyborg V

DIS/UMA

2IN1/CLAMSHELL

APU I2C port 0 RR=3.3V

INTERNAL DEBUG PURPOSE ONLY

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (I2C/GPIO/RTC/SMBS/HDA)

Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 17 of 106

Main Func = USB

USB3.0 Port1

[35] USB1_USB30_RX_N
[35] USB1_USB30_RX_P
[35] USB1_USB30_TX_N
[35] USB1_USB30_TX_P

[35] USB1_USB20_N
[35] USB1_USB20_P

USB3.0 Port2

[66] USB2_USB30_RX_N
[66] USB2_USB30_RX_P
[66] USB2_USB30_TX_N
[66] USB2_USB30_TX_P

[66] USB2_USB20_N
[66] USB2_USB20_P

Finger Printer

[66] FP1_USB20_N
[66] FP1_USB20_P

IR Camera

[55] CCD_USB20_N
[55] CCD_USB20_P

Card Reader EVT 0510

[66] CARD1_USB20_N
[66] CARD1_USB20_P

Type C USB20

[73] TYPEC_USB20_N
[73] TYPEC_USB20_P

DP Type-C 20180416

[73] USB3_USB30_TX_P0
[73] USB3_USB30_TX_N0
[73] USB3_USB30_RX_P0
[73] USB3_USB30_RX_N0

[73] USB3_USB30_TX_P1
[73] USB3_USB30_TX_N1
[73] USB3_USB30_RX_P1
[73] USB3_USB30_RX_N1

20180418

[74] USB_OC0#
[35] USB_OC1#

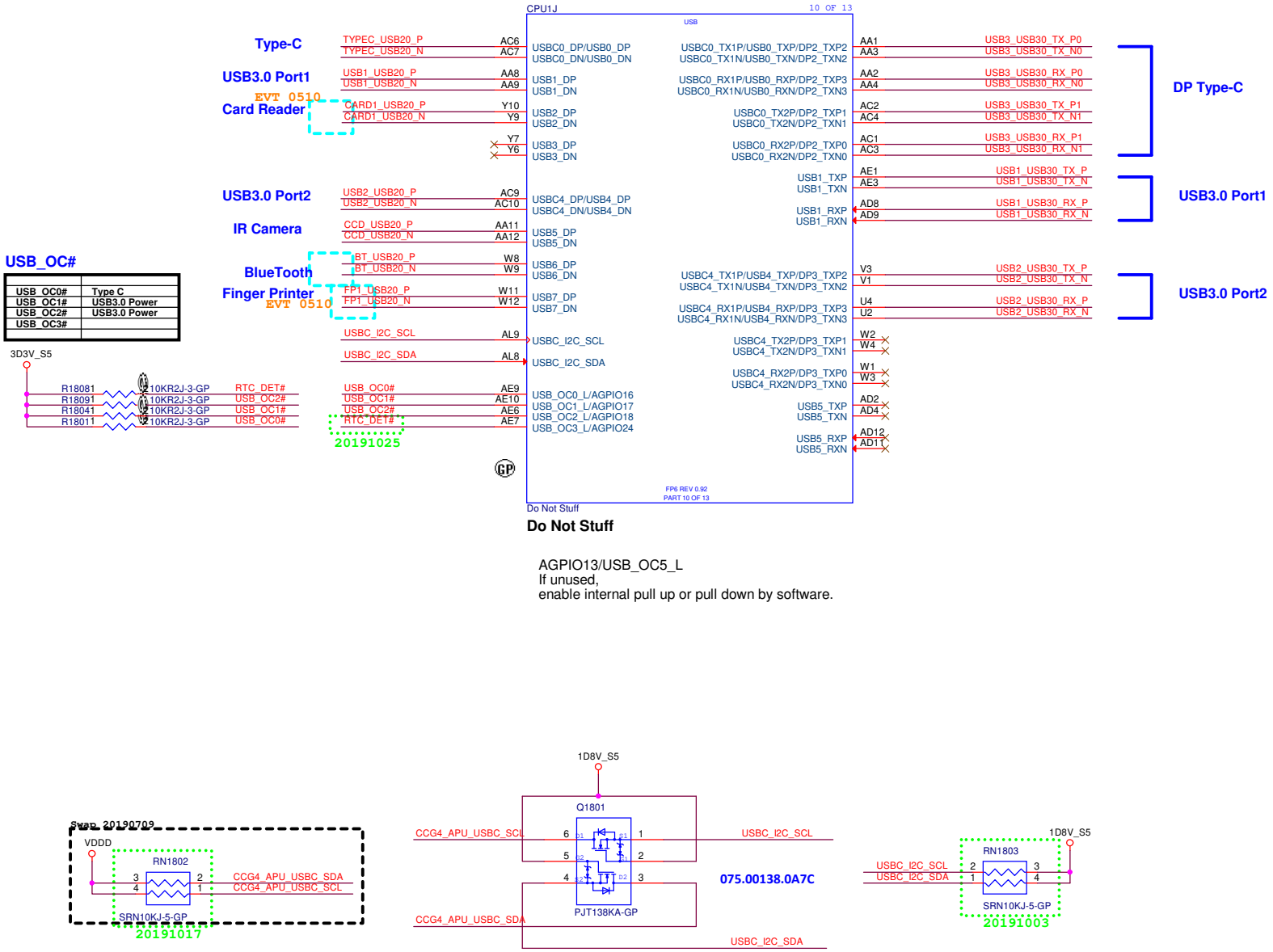
[35] USB_OC2#

[72,73] CCG4_APU_USBC_SCL
[72,73] CCG4_APU_USBC_SDA

BT

[61] BT_USB20_P
[61] BT_USB20_N

[25] RTC_DET#



Do Not Stuff

AGPIO13/USB_OC5_L
If unused,
enable internal pull up or pull down by software.

USB_OC#

USB_OC0#	Type C
USB_OC1#	USB3.0 Power
USB_OC2#	USB3.0 Power
USB_OC3#	

20191025

20191017

075.00138.0A7C

20191003

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (USB)*

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 18 of 106

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CB 14 N

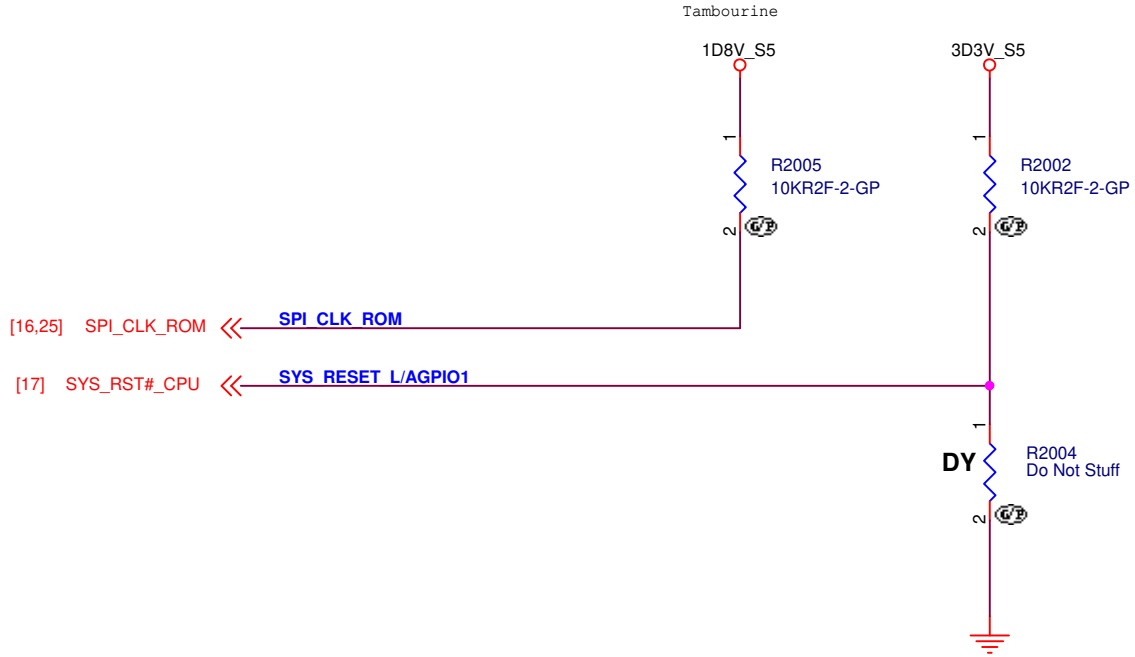
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (RSVD)*

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 19 of 106

STRAP PINS



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10KΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (Strap)*

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 20 of 106

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CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (RSVD)*

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 21 of 106

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (RSVD)*

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 22 of 106

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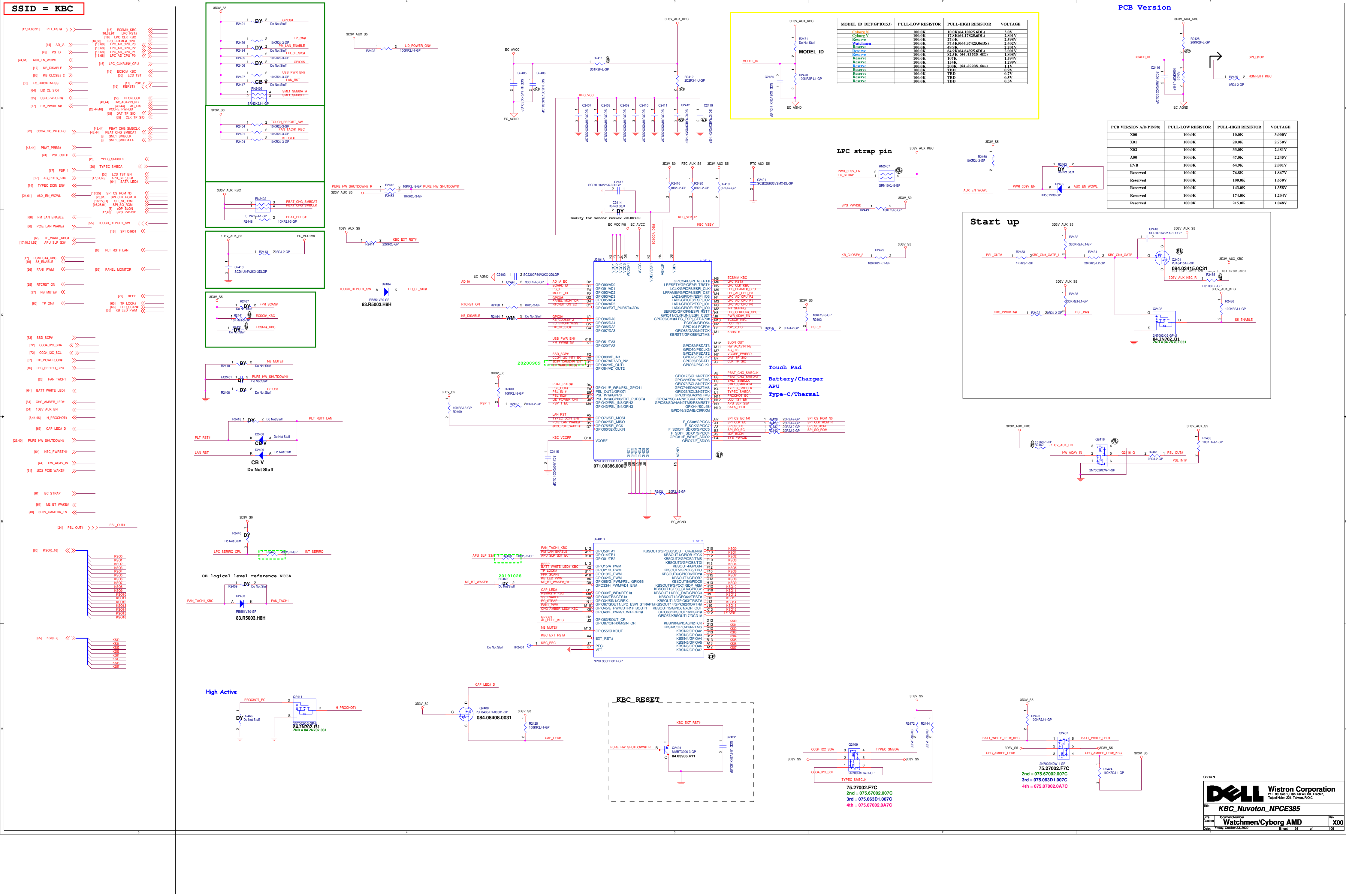
CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (RSVD)*

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 23 of 106



MODEL_ID_DET(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Cyborg N	100.0K	10.0K(64.10025.6DL)	3.0V
Cyborg V	100.0K	17.8K(64.17825.6DL)	2.801V
Reserve	100.0K	27.0K	2.598V
Watchmen	100.0K	37.4K(064.37425.06DS)	2.402V
Reserve	100.0K	49.9K	2.201V
Reserve	100.0K	64.9K(64.64925.6DL)	2.001V
Reserve	100.0K	82.5K (64.82525.6DL)	1.808V
Reserve	100.0K	107K	1.594V
Reserve	100.0K	154K	1.299V
Reserve	100.0K	200K (64.20035.6DL)	1.1V
Reserve	100.0K	TBD	0.9V
Reserve	100.0K	TBD	0.7V
Reserve	100.0K	TBD	0.5V
Reserve	100.0K	TBD	0.3V

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.000V
X01	100.0K	20.0K	2.750V
X02	100.0K	33.0K	2.481V
A00	100.0K	47.0K	2.245V
EVB	100.0K	64.9K	2.001V
Reserved	100.0K	76.8K	1.867V
Reserved	100.0K	100.0K	1.650V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_Nuvoton_NPCE385

Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 24 of 106

https://vinafix.com

SSID = Flash.ROM

[16,24] SPI_CS_ROM_N0
[16,24,91] SPI_SO_ROM
[16] SPI_WP_ROM
[16] SPI_HOLD_ROM
[16,24,91] SPI_SI_ROM
[24,91] SPI_CLK_ROM_R
[16,20] SPI_CLK_ROM

1D8V_VCCSPI

R25011 10KR2J-3-GP SPI_SO_ROM
R25021 10KR2J-3-GP SPI_CS_ROM_N0
R25031 10KR2J-3-GP SPI_WP_ROM
R25041 10KR2J-3-GP SPI_HOLD_ROM

BIOS1 **16MByte**

SPI_CS_ROM_N0 → CS#
SPI_SO_ROM → DO/IO1
SPI_WP_ROM → WP#/IO2
GND
VCC ← 1D8V_VCCSPI
HOLD#/RESET#/IO3 → SPI_HOLD_ROM
CLK → SPI_CLK_ROM
DI/IO0 → SPI_SI_ROM

W25Q128JWSIQ-GP
072.25128.0AF1
2nd = 072.25128.0A91
EVT BOM USE 072.25128.0I01 20200730

C2502 SC1U10V2KX-1DLGP
R2506 33R2J-2-GP
SPI_CLK_ROM_R
C2504 SC33P50V2JN-3DLGP

1D8V_VCCSPI C2503 SC1U10V2KX-1DLGP
1D8V_S5 C2509 SCD1U16V2KX-3DLGP

SSID = RBAT

[24] RTCRST_ON
[18] RTC_DET#

+RTC_VCC
3D3V_AUX_S5
RTC_AUX_S5

D2502 BAT54C-12-GP
75.00054.A7D

R2507 1KR2J-1-GP
RTC_PWR

DY C2505 Do Not Stuff
20200714

R2509 10MR2J-L-GP

Q2505 PJE8408-R1-00001-GP
084.08408.0031

RTC_DET#_R
R2505 0R2J-2-GP
RTC_DET#

1D8V_S5 — R2508 D01R2J-L-GP — 1D8V_VCCSPI

RTC_AUX_S5

Q2506 PJA3415AE-GP
084.03415.0C31

C2511 SC1U10V2KX-1DLGP
VBAT_SB_N
C2512 SC1U10V2KX-1DLGP
R2511 1KR2F-3-GP
1D5V_VDDBT_RTC
C2513 SC1U10V2KX-1DLGP
G2501 Do Not Stuff

R2512 DY Do Not Stuff
RTCRST_ON

Q2511 PJE8408-R1-00001-GP
084.08408.0031
Q701_S
R2513 100R2J-2-GP
R2515 10KR2F-2-GP

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

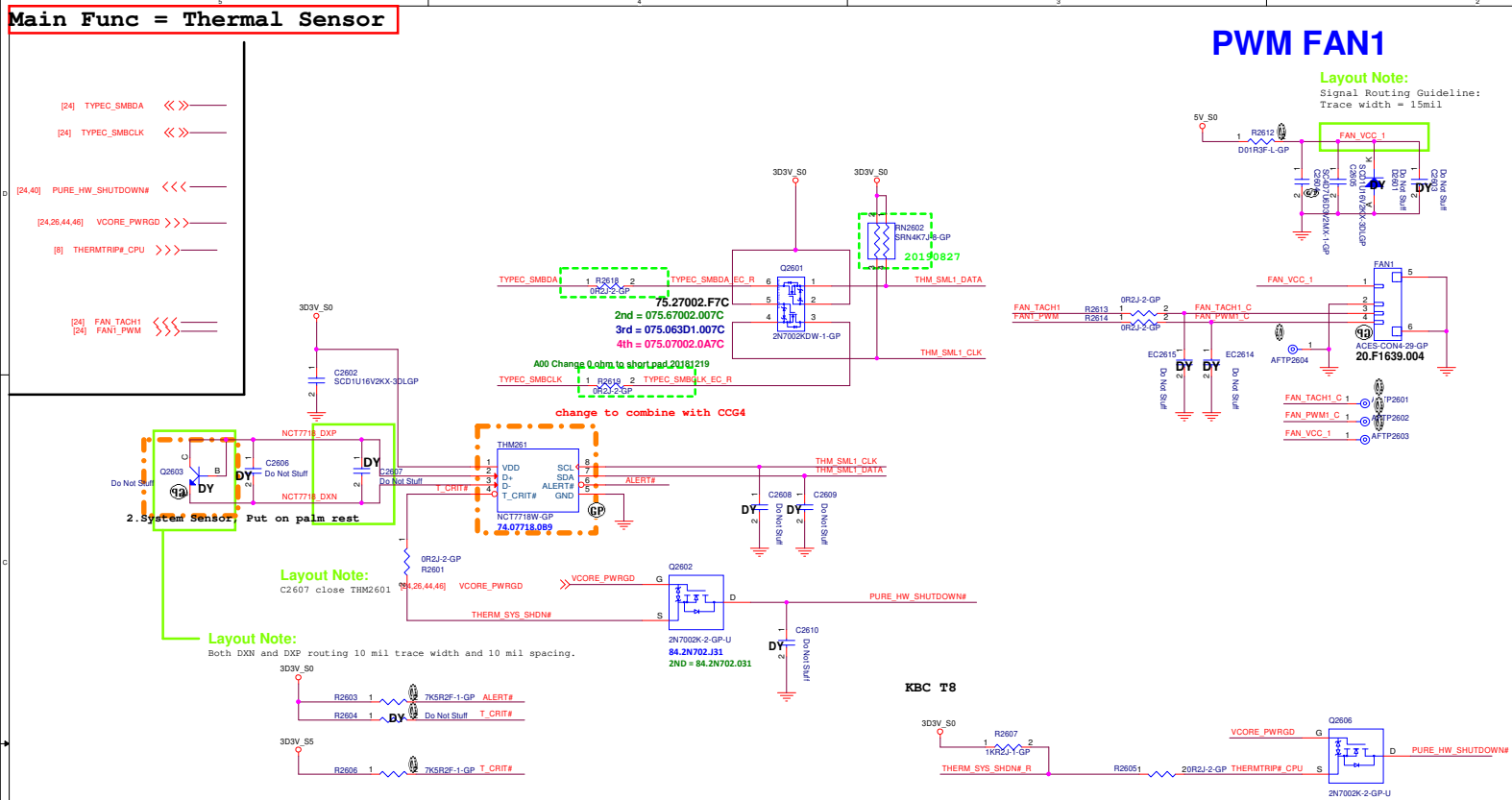
Title: **FLASH / RTC**

Size: A3 | Document Number: **Watchmen/Cyborg AMD** | Rev: **X00**

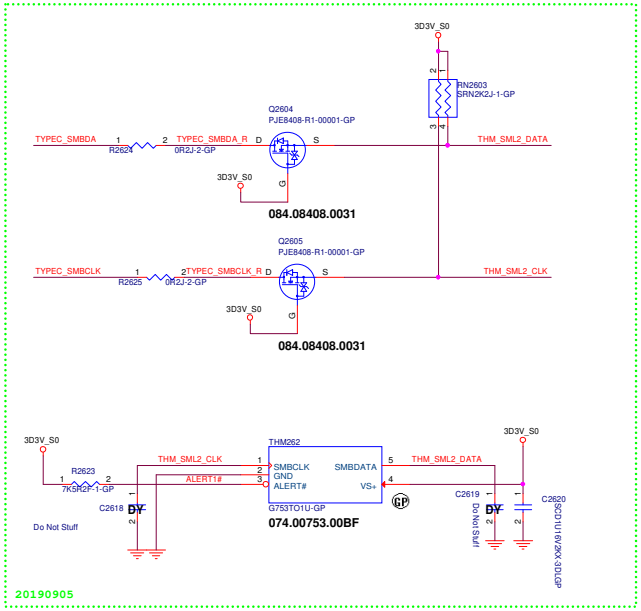
Date: Friday, October 23, 2020 | Sheet 25 of 106

Main Func = Thermal Sensor

PWM FAN1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



CB 14 N

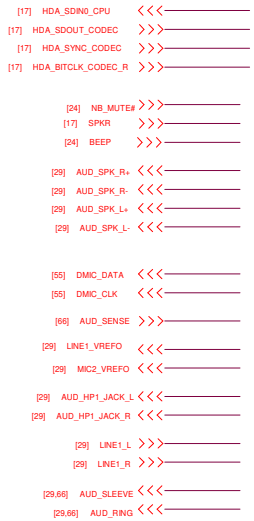
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

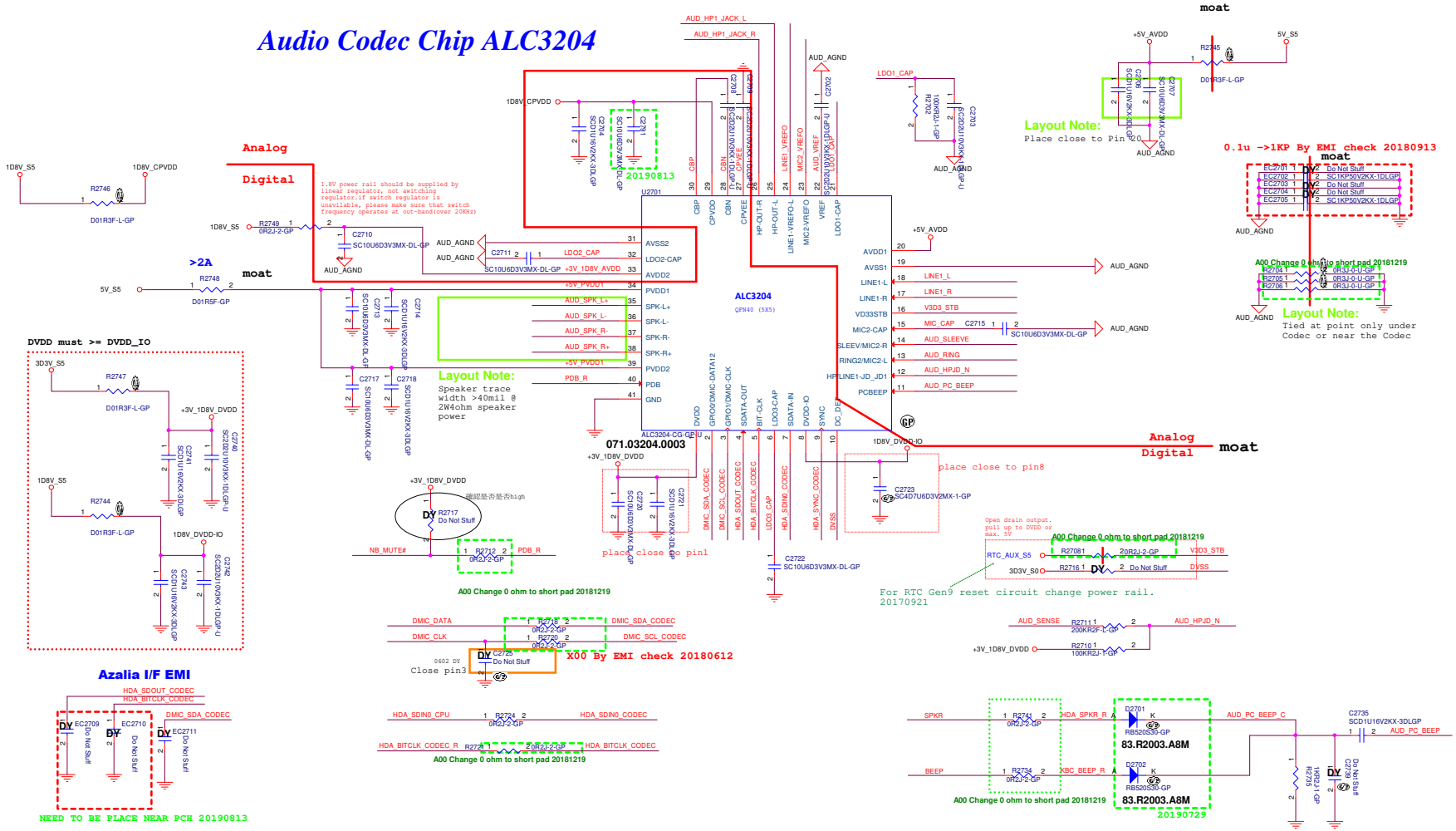
Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 28 of 106

Main Func = Audio



Audio Codec Chip ALC3204



CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204

Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 27 of 106

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CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 28 of 106

Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[17] SPK_ID

AUD_SPK_L-_C 1
AUD_SPK_L+_C 1
AUD_SPK_R-_C 1
AUD_SPK_R+_C 1
AFTP2901
AFTP2902
AFTP2903
AFTP2904

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L-
Pin4	SPK_L+

AUD_SPK_L+ R2904 1 0R3J-0-U-GP
AUD_SPK_L- R2903 1 0R3J-0-U-GP
AUD_SPK_R- R2901 1 0R3J-0-U-GP
AUD_SPK_R+ R2902 1 0R3J-0-U-GP

AUD_SPK_L+_C
AUD_SPK_L-_C
AUD_SPK_R-_C
AUD_SPK_R+_C
SPK_ID

SPK1
ACES-CON6-20-GP-U
20.F1639.006
2nd = 20.F1804.006

EC2902 SC1KP50V2KX-1DLGP
EC2901 SC1KP50V2KX-1DLGP
EC2903 SC1KP50V2KX-1DLGP
EC2904 SC1KP50V2KX-1DLGP

D2904 Do Not Stuff
D2905 Do Not Stuff
D2906 Do Not Stuff
D2907 Do Not Stuff
D2908 Do Not Stuff

in >LC >out
SPK_ID:接哪種喇叭:high/low來判斷

From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

Universal Jack (Moved to I/O Board)

MIC2_VREFO 2 RN2901 4 SRN2K2J-1-GP

AUD_HP1_JACK_L
LINE1_L C2907 1 2 LINE1-L_C SC10U6D3V3MX-DL-GP
R2922 1 2 1KR2J-1-GP
R2908 1 10R2F-L-GP
AUD_RING
AUD_HP1_JACK_L1

LINE1_R C2908 1 2 LINE1-L_R SC10U6D3V3MX-DL-GP
AUD_HP1_JACK_R
R2921 1 2 1KR2J-1-GP
R2910 1 10R2F-L-GP
AUD_HP1_JACK_R1
AUD_SLEEVE

D2902 RB520S30-GP
LINE1_VREFO_D1
R2912 1 2 4K7R2J-2-GP
83.R2003.A8M

LINE1_VREFO
D2903 RB520S30-GP
LINE1_VREFO_D2
R2913 1 2 4K7R2J-2-GP
83.R2003.A8M

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3
Document Number: Watchmen/Cyborg AMD
Rev: X00
Date: Friday, October 23, 2020
Sheet 29 of 106

Main Func = Audio

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 30 of 106

Main Func = LAN

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN (Reserved)*

Size	Document Number	Rev
A3	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 31 of 106

Main Func = LAN

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45 (Reserved)

Size: A3 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 32 of 106

Main Func = Card Reader

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5170

Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 33 of 106

Main Func = USB2.0

CB 14 N

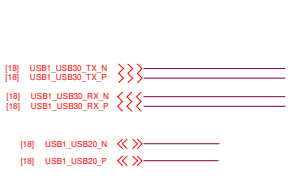
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

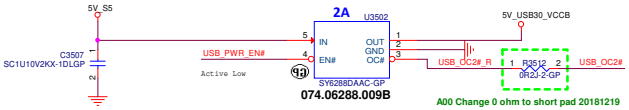
Title
USB Charger

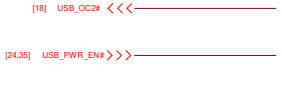
Size	Document Number	Rev
A4	***Watchmen/Cyborg AMD***	***X00***

Date: Friday, October 23, 2020 Sheet 34 of 106

Main Func = USB3.0 Port1

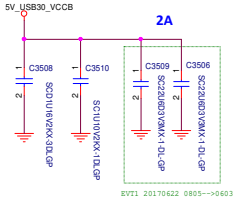


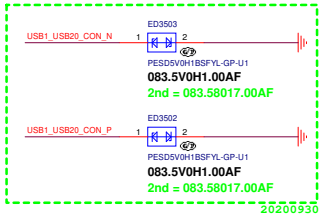


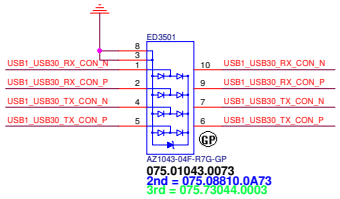


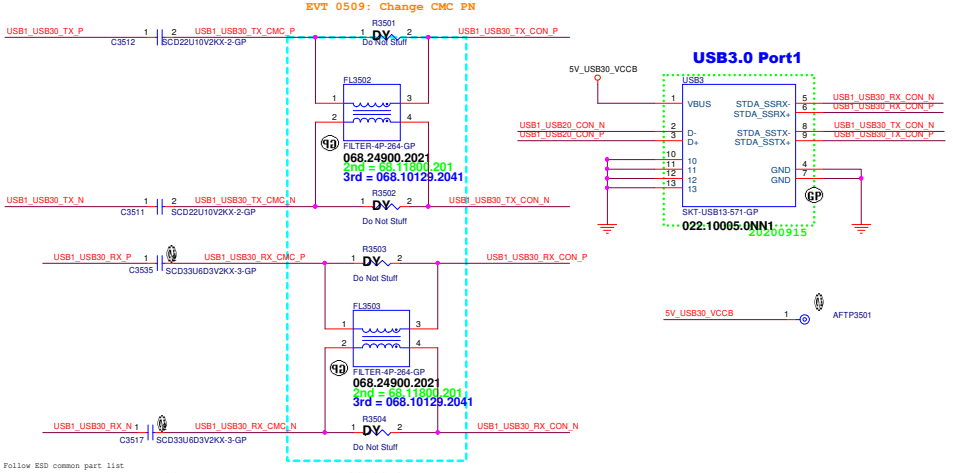
USB3.0 Port 1

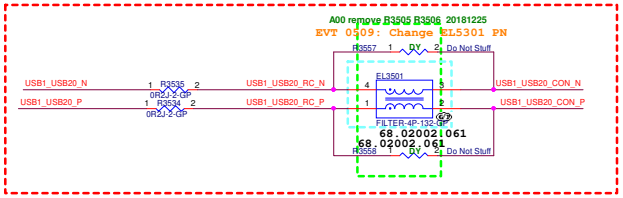
Layout Note: Close USB3





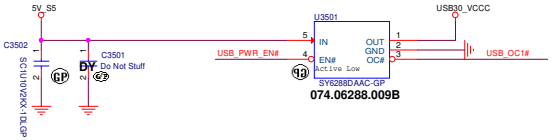




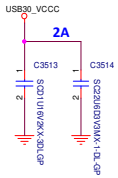


Main Func = USB3.0 Port2

Pin define by follow layout routing



USB3.0 Port 1



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Title: **USB3.0 CONN**

Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 35 of 106

Main Func = USB Charger

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Title

USB Charger

Size	Document Number	Rev
A4	***Watchmen/Cyborg AMD***	***X00***

Date: Friday, October 23, 2020 Sheet 36 of 106

(Blanking)

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Title: *Reserved*

Size	Document Number	Rev
A3	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 37 of 106

Main Func = USB HUB

CB 14 N

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Title

USB HUB

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 38 of 106

Main Func = USB3.0 Port1

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Title: (Reserved)

Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 39 of 106

Power Sequence

[17,24,51,52] APU_SLP_S3#

[45] 3V_5V_EN

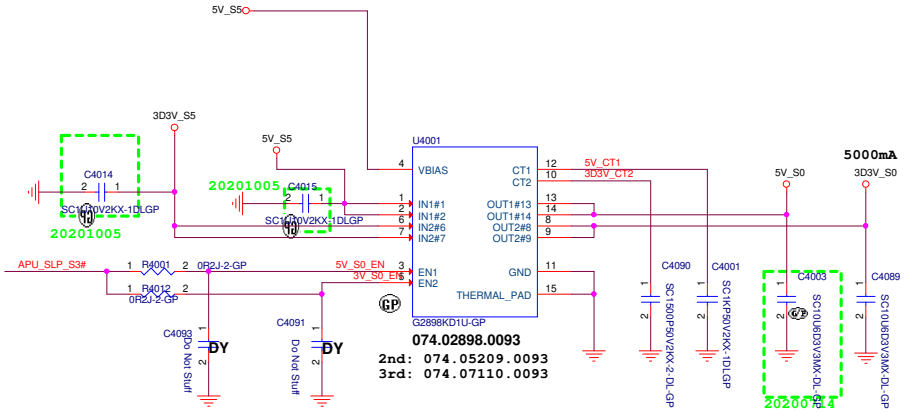
[24,26] PURE_HW_SHUTDOWN#

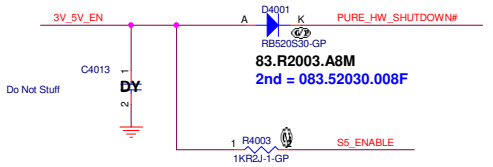
[24] S5_ENABLE

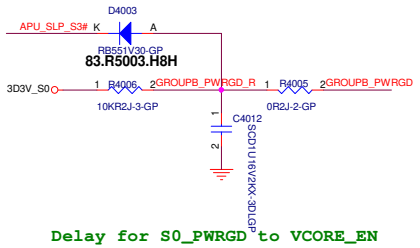
[17,24] SYS_PWRGD

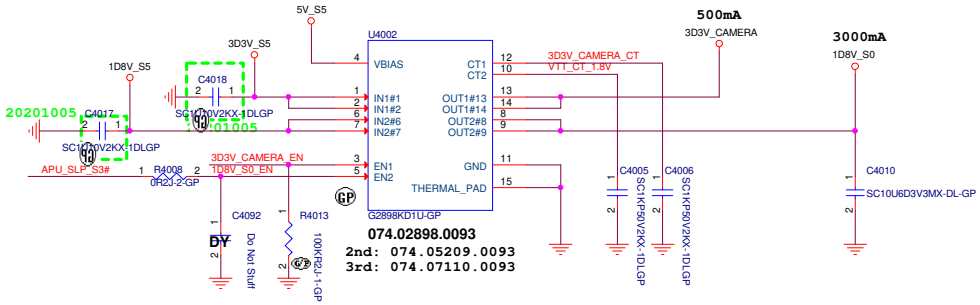
[44,46] GROUPB_PWRGD

[24] 3D3V_CAMERA_EN









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Title: Power Plane Enable&Sequence

Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 40 of 106

Main Func = Power Plane & Sequence

(Blanking)

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Title: *Connected_Standby(1/2)+DS3*

Size	Document Number	Rev
A4	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 41 of 106

(Blanking)

CB 14 N

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 42 of 106

Main Func = ADT Input

[24,44] AC_DIS
[24] PS_ID
[24,44] HW_ACAVIN_NB

Layout Note:
PSID Layout width > 25mil

84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11

75.00099.O7D
2nd = 75.00099.E7D
3rd = 75.00099.B7D
4th = 075.00099.0E7D

084.08438.0A31

75.05125.07D
2nd = 075.52215.007D

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

20.F2120.008

083.00624.00AM

S1
084.21321.0037

084.05112.001K
2nd = 84.00124.K1K
3rd = 084.00024.0A1K

84.05212.B11
2nd = 84.00124.H1K
3rd = 084.00024.0B1K

Main Func = M-BAT Input

[24,44] PBAT_CHG_SMBCLK
[24,44] PBAT_CHG_SMBDAT
[24,44] PBAT_PRES#

Batt Connecter

020.F1198.0010

084.08408.0031

20200922
20201005

Placement: Close to Batt Connector

20191218

2nd = 75.00099.K7D	2nd = 75.00099.K7D	2nd = 75.00099.K7D
3rd = 75.00099.Q7D	3rd = 75.00099.Q7D	3rd = 75.00099.Q7D
4th = 75.00099.D7D	4th = 75.00099.D7D	4th = 75.00099.D7D

Barrel Adapter Plug-in Detect
Follow Bandon

74.00331.H2F

20200929

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Title: DCIN

Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 43 of 106

SSID = PWR.Plane.Regulator_Charger

ISL9538C For Charger

OFFPAGE

20180526 check

From RKF ACK

Prochot

TypeC Prochot

Barrel Prochot

S2

20190606

20190711

DCR=6.6m~7mohm,
Idc=12A, Isat=27A
11.5mm x 10mm x 4.0mm

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)						
MIN	TYP ±1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLim/I.S. Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	0.476
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

PU +VCCSTG - 1.0 V on CPU side

TypeC Prochot

Follow custormer circuits.

Barrel Prochot

Follow custormer circuits.

Barrel input

TypeC input

+3D3V_VDD_DCIN

Vcore_OVP

Location	Gen11	Gen10
PR44A0	DY	Stuff
PR44D6	DY	Stuff
PR44D7	DY	Stuff
PR44D8	DY	Stuff
PC44D0	Stuff	DY
PC44D1	Stuff	DY
PQ44D1	Stuff	DY
PR44D0	Stuff	DY
PR44D1	Stuff	DY
PR44D2	Stuff	DY
PR44D3	Stuff	DY
PR44D4	Stuff	DY
PR44D5	Stuff	DY
PR44A7	Stuff	Stuff
PR44A8	DY	Stuff
PQ44D0	Stuff	Stuff

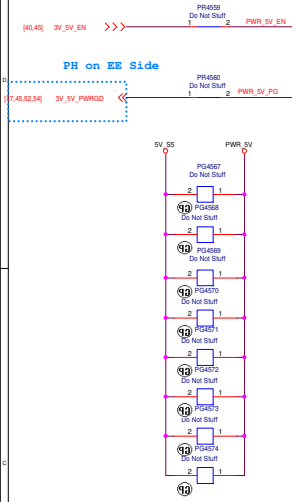
Wistron Corporation

Power (Charger_ISL9538)

Watchmen/Cyborg AMD

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal



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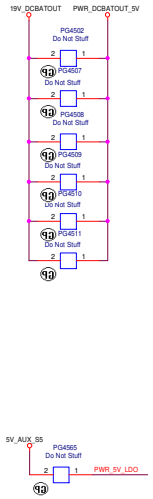
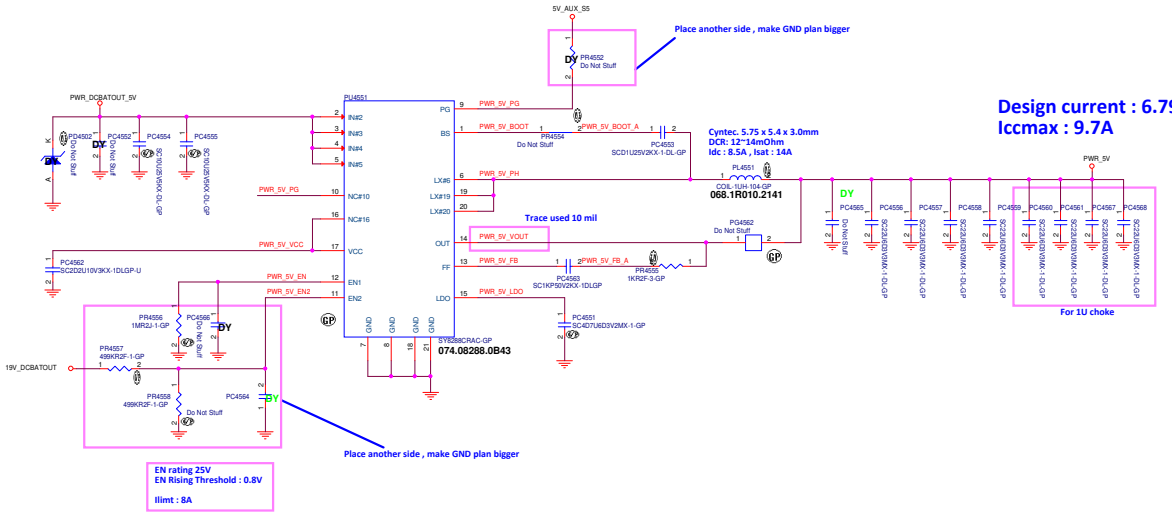
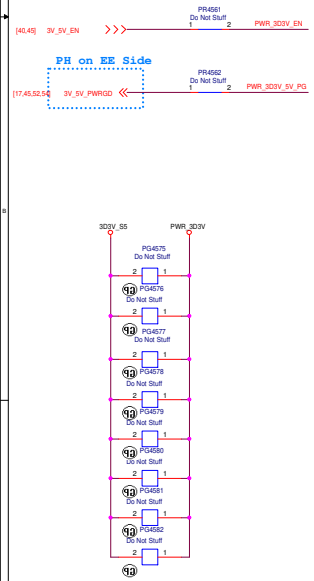


SY8288C For 5V

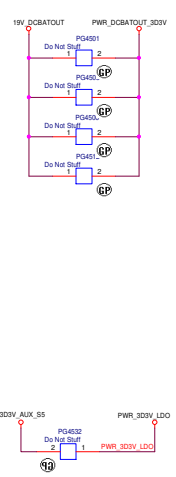


SSID = PWR.Plane.Regulator_3D3V

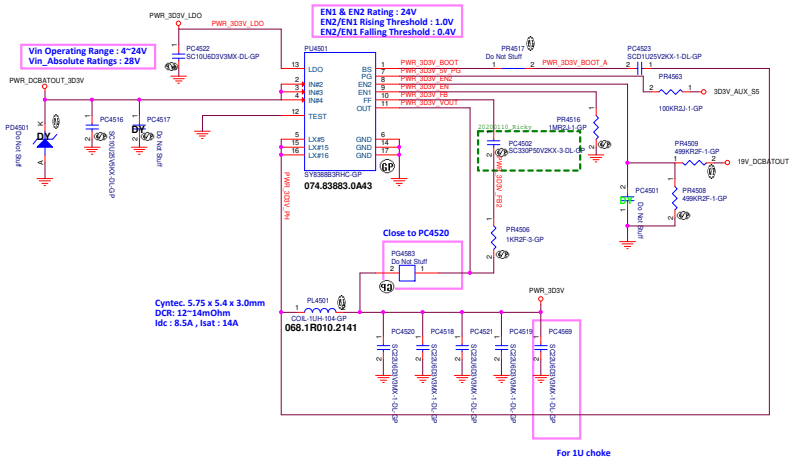
OFFPAGE-Signal



OFFPAGE-GAP



SY8388B3 For 3D3V



FPR S5 SSO 20191209 REMOVE ALL

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Title: POWER (SY8288_5V/3D3V)

Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 28, 2020 | Sheet 45 of 106

OFFPAGE

[8,24,44] H_PROCHOT#
[8] SVID_ALERT_N_CPU
[8] SVID_CLK_CPU
[8] SVID_DATA_CPU
[24,26,44] VCORE_PWRGD
[40,44] GROUPB_PWRGD
[8,68] SVID_PWRGD
[8] VSSCORE_SENSE
[8] VCCCORE_SENSE
[8] VDDNB_SENSE

1D8V_S5 — PR4616 2D2R3J-2-GP — PWR_VCORE_VDDIO

H_PROCHOT# — PG4602 Do Not Stuff — PWR_VCORE_VRHOTL
SVID_ALERT_N_CPU — PR4617 0R2J-2-GP — PWR_VCORE_SVT
SVID_CLK_CPU — PR4618 0R2J-2-GP — PWR_VCORE_SVC
SVID_DATA_CPU — PR4619 0R2J-2-GP — PWR_VCORE_SVD
VCORE_PWRGD — PG4620 Do Not Stuff — PWR_VCORE_VR_READY
GROUPB_PWRGD — PG4621 Do Not Stuff — PWR_VCORE_VR_EN
SVID_PWRGD — PG4638 — PWR_SVID_PWRGD Do Not Stuff
VSSCORE_SENSE — PG4640 — PWR_VCORE_RGND Do Not Stuff

074.03662.0B73

PU4601 RT3662AMGQW-GP-U

PWR_VCORE_VREF_PINSET — PR4633 62KR2F-GP — PR4671 249KR2F-GP — PR4636 37K4R2F-1-GP — PWR_VCORE_VREF_PINSET_G — PR4653 4K32R2F-GP — PR4652 10KR2F-2-GP — PWR_VCORE_VREF_PINSET_H
5V_S5 — PR4601 4D7R3J-L1-GP — PWR_VCORE_VCC — PC4601 SC2D2U10V3KX-1DLGP-U
PR4666 Do Not Stuff — PWR_VCORE_PVCC — PC4636 SC2D2U10V3KX-1DLGP-U
1st = 69.60011.221
2nd = 69.60013.201
NTC-100K-12-GP-U PR4630
PWR_VCORE_SET1
PR4634 6K49R2F-1-GP — PWR_VCORE_RNTC2P — 62KR2F-GP PR4635 — PWR_VCORE_TSEN
PR4632 32K4R2F-1-GP — PWR_VCORE_RNTC2P_NB — 62KR2F-GP PR4639 — PWR_VCORE_TSEN_NB
PR4637 24K3R2F-1-GP — PWR_VCORE_TSEN_B
NTC-100K-12-GP-U PR4626
PR4655 1K18R2F-GP — PR4654 100R2F-L1-GP-U — PWR_VCORE_TSEN_NB_B
1st = 69.60011.221
2nd = 69.60013.201

Pin	Net
17	VCC
34	PVCC
13	SET1
12	TSEN
23	TSEN_NB
41	GND
29	EN
22	VDDIO
18	PWROK
19	SVC
20	SVD
21	SVT
3	PGOOD
11	VRHOT#
16	IMON_NB
15	VREF_PINSET
27	COMP_NB
26	FB_NB

PWR_VCORE_SVT — PC4610 Do Not Stuff
PWR_VCORE_SVC — PC4611 Do Not Stuff
PWR_VCORE_SVD — PC4612 Do Not Stuff
3D3V_S0 — PC4646 Do Not Stuff — PR4643 Do Not Stuff — PC4647 SCD1U16V2KX-3DLGP — PR4668 10KR2J-3-GP
PC4608 Do Not Stuff
PC4635 SC1U10V2KX-1DLGP
PWR_SVID_PWRGD
PWR_VCORE_SVC
PWR_VCORE_SVD
PWR_VCORE_SVT
PWR_VCORE_VR_READY
PWR_VCORE_VRHOTL
PR4651 1K4R2F-1-GP — PWR_VCORE_IMON
PWR_VCORE_VREF_PINSET_C
PR4650 14KR2F-GP — PWR_VDDNB_IMON
PWR_VCORE_VREF_PINSET_E
PR4670 374R2F-1-GP — PR4615 Do Not Stuff — PR4631 Do Not Stuff
PWR_VCORE_VREF_PINSET_F — PR4629 — PWR_VCORE_VREF_PINSET_D — PWR_VCORE_VREF_PINSET_B — PWR_VCORE_VREF_PINSET_A
PR4667 9K09R2F-GP — PR4669 16K9R2F-GP — PR4609 16KR2F-GP
NTC-100K-12-GP-U 1st = 69.60011.221 2nd = 69.60013.201
NTC-100K-12-GP-U 1st = 69.60011.221 2nd = 69.60013.201
PR4608 10K5R2F-GP
3D9R2F-GP PR4644 — PWR_VCORE_VREF_PINSET
PC4629 SCD47U25V3KX-1-DL-GP — PWR_VCORE_VREF_PINSET

Remote Vsense
VDDNB_SENSE — PC4644 SC220P50V2KX-3DLGP — PWR_VCORE_FB_NB — PC4645 SC100P50V2JN-3DLGP — PWR_VCORE_COMP_NB
1D2V_CPU_SOC — PR4645 10R2F-L-GP — PR4626 52K3R2F-L-GP — PWR_VCORE_FB_NB
PR4625 10KR2F-2-GP
PR4676 Do Not Stuff — PWR_VCORE_FB_NB_A — PC4668 Do Not Stuff
Local Vsense

PWR_DCBATOUT_VCCCORE — PR4607 4D7R2F-GP — PD4601 Do Not Stuff
PWR_DCBATOUT_VCCCOREA_1 — PC4607 SCD1U25V2KX-1-DL-GP

Pin	Net	Out
28	VIN	
38	BOOT1	PWR_VCORE_BOOTA [47]
37	UGATE1	PWR_VCORE_HGA [47]
36	PHASE1	PWR_VCORE_PHA [47]
35	LGATE1	PWR_VCORE_LGA [47]
9	ISEN1P	PWR_VCORE_ISEN1P [47]
10	ISEN1N	PWR_VCORE_ISEN1N [47]
2	BOOT2	PWR_VCORE_BOOTB [47]
1	UGATE2	PWR_VCORE_HGB [47]
40	PHASE2	PWR_VCORE_PHB [47]
39	LGATE2	PWR_VCORE_LGB [47]
7	ISEN2P	PWR_VCORE_ISEN2P [47]
8	VSEN	PWR_VCORE_VSEN_1
5	COMP	PWR_VCORE_COMP
6	FB	PWR_VCORE_FB
4	RGND	PWR_VCORE_RGND
30	BOOT_NB	PWR_VDDNB_BOOT [48]
31	UGATE_NB	PWR_VDDNB_HG [48]
32	PHASE_NB	PWR_VDDNB_PH [48]
33	LGATE_NB	PWR_VDDNB_LG [48]
25	ISENP_NB	PWR_VCORE_ISENP_NB [48]
24	ISENN_NB	PWR_VCORE_ISENN_NB [48]

PR4627 Do Not Stuff
PC4634 SCD1U25V2KX-1-DL-GP
PC4604 SC100P50V2JN-3DLGP — PR4614 47KR2F-GP — PC4603 SC220P50V2KX-3DLGP — PR4603 10KR2F-2-GP
PR4675 Do Not Stuff — PWR_VCORE_FB_A — PC4667 Do Not Stuff
SA 0424
PC4642 SCD1U25V2KX-1-DL-GP

Remote Vsense
VCCCORE_SENSE
PR4647 10R2F-L-GP — 1V_CPU_CORE
PR4648 10R2F-L-GP
Local Vsense
PWR_VCORE_RGND
Remote Vsense

CB 14 N

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT3662A CPUCORE
Size: A2 | Document Number: ROSA NB STD POWER | Rev: SA
Date: Friday, October 23, 2020 | Sheet 46 of 106

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19V_DCBATOUT — PWR_DCBATOUT_VCCCORE

PG4701 Do Not Stuff
PG4702 Do Not Stuff
PG4703 Do Not Stuff
PG4704 Do Not Stuff
PG4705 Do Not Stuff

19V_DCBATOUT — PWR_DCBATOUT_VCCCORE

PG4706 Do Not Stuff
PG4707 Do Not Stuff
PG4708 Do Not Stuff
PG4713 Do Not Stuff
PG4714 Do Not Stuff

PWR_DCBATOUT_VCCCORE

PC4701 ST100U25VDM-1-GP

For acoustic noice

PWR_DCBATOUT_VCCCORE

PC4702 SC10U25V5KX-DL-GP
PC4704 SC10U25V5KX-DL-GP
PC4715 SC10U25V5KX-DL-GP
PD4701 Do Not Stuff

PU4701 AOE6932-GP 075.06932.0A73

[46] PWR_VCORE_LGA — PWR_VCORE_LGA
[46] PWR_VCORE_HGA
[46] PWR_VCORE_PHA
[46] PWR_VCORE_BOOTA — PR4701 2D2R3-1-U-GP — PWR_VCORE_BOOTA_A — PC4701 SCD1U25V2KX-1-DL-GP

PR4713 Do Not Stuff (DY) — PWR_VCORE_SNBA
PC4716 Do Not Stuff (DY)

Cyntec. 7.6mm x6.8mmx3.0mm
DCR: 0.9m Ohm+/-5%
Idc : 35A , Isat : 41A
PL4701 IND-D15UH-59-GP 068.R1510.2191

1V_CPU_CORE

PT4701 PT4702 PT4703 PT4704 T60U2DVM-GP

PG4709 Do Not Stuff — PG4710 Do Not Stuff

PWR_VCORE_ISEN1P_1A — PR4715 2K15R2F-1-GP — PWR_VCORE_ISEN1P_2A
PR4702 2K15R2F-1-GP — PC4709 SCD1U25V2KX-1-DL-GP — PWR_VCORE_ISEN1P_A

[46,47] PWR_VCORE_ISEN1P — PR4703 Do Not Stuff (DY)
[46,47] PWR_VCORE_ISEN1N — PR4704 1R2F-GP
[46,47] PWR_VCORE_ISEN2P — PR4705 3K9R2F-GP

TDC=45A
Imax=70A

VCORE :330uF/6m ohm * 6pcs+22uF * 30pcs

PWR_DCBATOUT_VCCCORE

PC4708 SC10U25V5KX-DL-GP
PC4707 SC10U25V5KX-DL-GP
PC4714 SC10U25V5KX-DL-GP
PD4702 Do Not Stuff

PU4702 AOE6932-GP 075.06932.0A73

[46] PWR_VCORE_LGB — PWR_VCORE_LGB
[46] PWR_VCORE_HGB
[46] PWR_VCORE_PHB
[46] PWR_VCORE_BOOTB — PR4712 2D2R3-1-U-GP — PWR_VCORE_BOOTB_A — PC4713 SCD1U25V2KX-1-DL-GP

PR4714 Do Not Stuff (DY) — PWR_VCORE_SNBB
PC4717 Do Not Stuff (DY)

Cyntec. 7.6mm x6.8mmx3.0mm
DCR: 0.9m Ohm+/-5%
Idc : 35A , Isat : 41A
PL4702 IND-D15UH-59-GP 068.R1510.2191

1V_CPU_CORE

PG4712 Do Not Stuff — PG4711 Do Not Stuff

PWR_VCORE_ISEN2P_1B — PR4716 2K15R2F-1-GP — PWR_VCORE_ISEN2P_2B
PR4706 2K15R2F-1-GP — PC4711 SCD1U25V2KX-1-DL-GP — PWR_VCORE_ISEN1P_B

[46,47] PWR_VCORE_ISEN2P — PR4707 Do Not Stuff (DY)
[46,47] PWR_VCORE_ISEN1N — PR4709 1R2F-GP — PC4710 SCD1U25V2KX-1-DL-GP
[46,47] PWR_VCORE_ISEN1P — PR4708 3K9R2F-GP

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT3662A CPUCORE
Size: Custom
Document Number: ROSA NB STD POWER
Rev: SA
Date: Friday, October 23, 2020
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OFFPAGE_GAP

19V_DCBATOUT
PWR_DCBATOUT_VDDNB
PG4801 Do Not Stuff
PG4802 Do Not Stuff
PG4803 Do Not Stuff
PG4804 Do Not Stuff

PWR_DCBATOUT_VDDNB
TC4801 ST100U25VDM-1-GP
077.C1071.0071

TDC=13A
Imax=17A

SB1101.2Ray:Add PQ4801 2ND

PU4801
[46] PWR_VDDNB_HG
[46] PWR_VDDNB_LG
FDMS3600-02-RJK0215-COLAY-GP

1st = 075.36356.0073
2nd = 075.00630.0073

PWR_DCBATOUT_VDDNB
PC4803 SC10U25V5KX-DL-GP
PC4802 SC10U25V5KX-DL-GP
PD4801 Do Not Stuff

Cyntec. 7.6mm x6.8mmx3.0mm
DCR: 0.9m Ohm+/-5%
Idc : 35A , Isat : 41A

NB : 330uF /9mohm* 2pcs+22uF * 12pcs

[46] PWR_VDDNB_PH
[46] PWR_VDDNB_BOOT
PR4801 2D2R3-1-U-GP
PWR_VDDNB_BOOT_A
PC4805 SCD1U25V2KX-1-DL-GP

PL4801 IND-D15UH-59-GP
068.R1510.2191

1D2V_CPU_SOC
PT4801 ST330U2D5VBM-4-GP
PT4802 ST330U2D5VBM-4-GP

close to PL4801
PWR_VDDNB_PH
PR4804 Do Not Stuff DY
PWR_VDDNB_SNB
PC4806 Do Not Stuff DY

PG4805 Do Not Stuff
PWR_VCORE_ISENP_NB_B
PG4806 Do Not Stuff
PR4805 1K8R2F-GP
PWR_VCORE_ISENP_NB_A
PR4802 1K8R2F-GP
PC4801 SCD1U25V2KX-1-DL-GP

[46] PWR_VCORE_ISENP_NB
PWR_VCORE_ISENP_NB
PR4803 5K49R2F-GP
[46] PWR_VCORE_ISENN_NB
PWR_VCORE_ISENN_NB

CB 14 N

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT3662A CPUCORE
Size: A3
Document Number: ROSA NB STD POWER
Rev: SA
Date: Friday, October 23, 2020
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TBD

CB 14 N

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Power (RSVD)***
Size: A2	Document Number: **Watchmen/Cyborg AMD** Rev: **X00**
Date: Friday, October 23, 2020	Sheet 49 of 106

TBD

CB 14 N

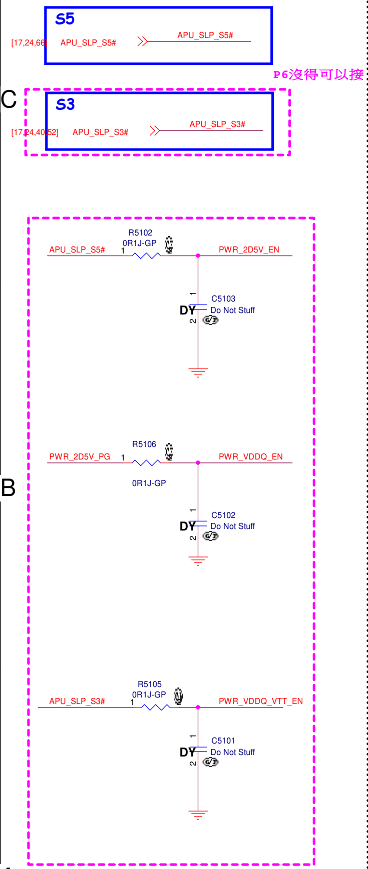
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power (RSVD)*

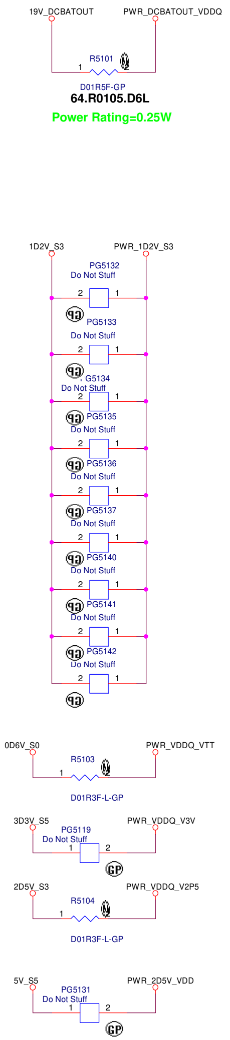
Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 50 of 106

OFFPAGE



OFFPAGE_GAP



NB685GQ for VDDQ & VTT

TDC : 8.75A
OCP : 13A

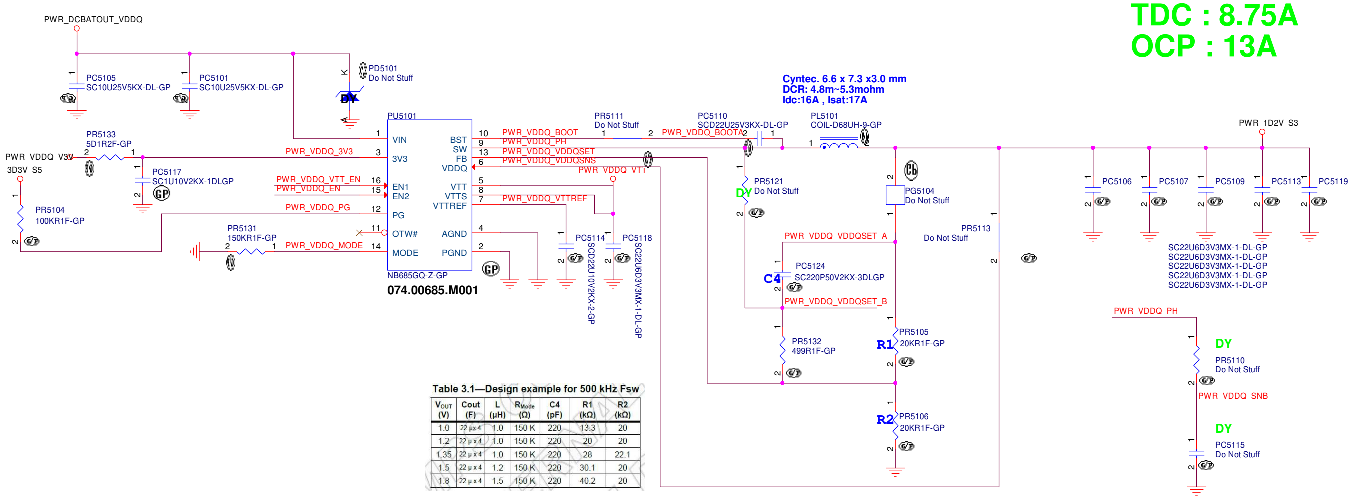
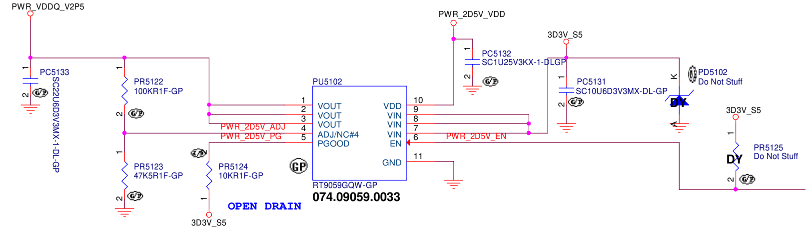


Table 3.1—Design example for 500 kHz Fsw

V_{OUT} (V)	Cout (F)	L (μH)	R_{Mode} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)
1.0	22 μx 4	1.0	150 K	220	13.3	20
1.2	22 μ x 4	1.0	150 K	220	20	20
1.35	22 μ x 4	1.0	150 K	220	28	22.1
1.5	22 μ x 4	1.2	150 K	220	30.1	20
1.8	22 μ x 4	1.5	150 K	220	40.2	20

Design Current = 0.7A

RT9059GQW for 2D5V



Vout = 0.8*(1+R1/R2)=2.48V

https://vinafix.com

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC VCCSA(NCP302035)	
Size A2	Document Number: Watchmen/Cyborg AMD	Rev X00
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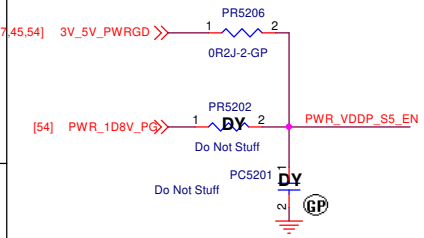
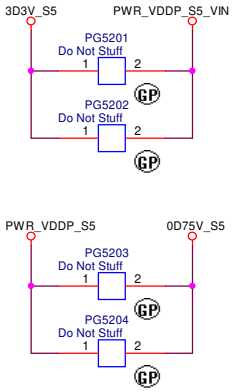
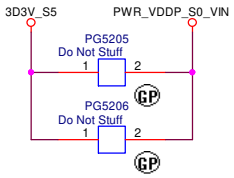
SSID = PWR.Plane.Regulator_VDDP

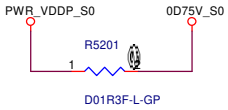
OFFPAGE-Signal



OFFPAGE-GAP

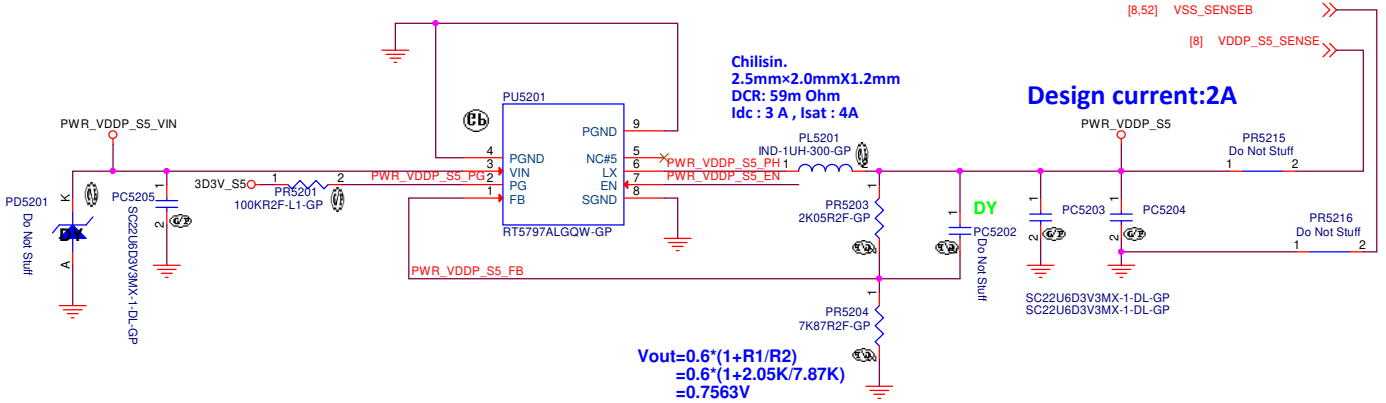




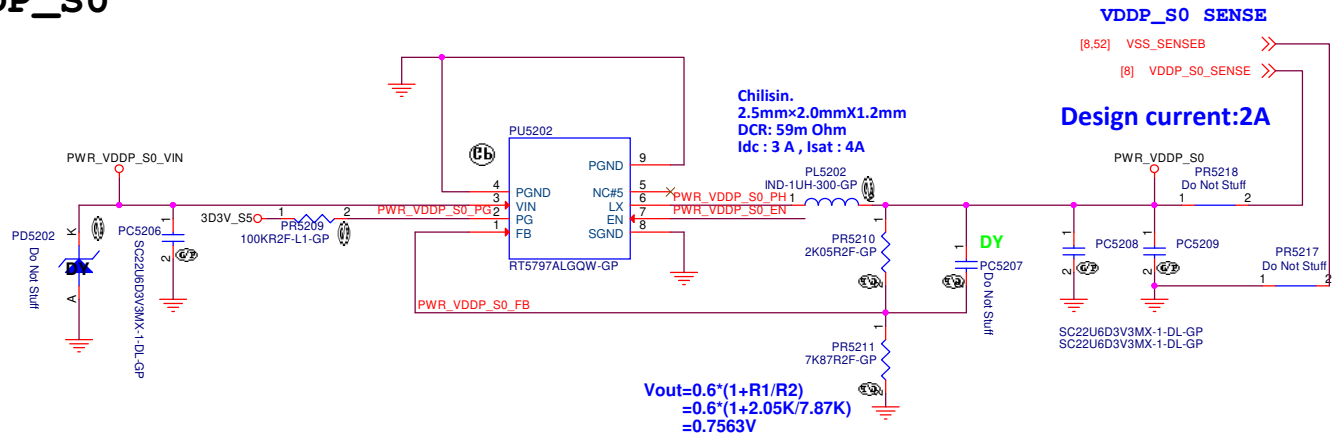


https://vinafix.com

VDDP_S5



VDDP_S0



CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT5797_VDDP)

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

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CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	***Watchmen/Cyborg AMD***	*X00*

Date: Friday, October 23, 2020 Sheet 53 of 106

SSID = PWR.Plane.Regulator_1D8V

SY8386RHC for 1D8V_VDD

OFFPAGE-Signal

PH on EE Side

[52] PWR_1D8V_PG

20180430 follow starload

[17,45,52] 3V_5V_PWRGD

PR5455 20KR2J-L2-GP

PWR_1D8V_EN

[24] 1D8V_AUX_EN

OFFPAGE-GAP

19V_DCBATOUT PWR_DCBATOUT_1D8V

PG5401 Do Not Stuff

1D8V_S5 PWR_1D8V

PG5402 Do Not Stuff

PG5403 Do Not Stuff

PG5404 Do Not Stuff

PG5407 Do Not Stuff

1D8V_PWR 1D8V_AUX_S5

PG5406 Do Not Stuff

IDC : 2.82A
Iccmax : 4.03A

Cyntec 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

PL5401 COIL-1UH-34-GP-U1

Trace used 10 mil

PU5401 SY8386RHC-GP

DY

Place another side , make GND plan bigger

Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 20K/10K)
= 0.6 x 3 = 1.8 V

RT9078-18GJ5 for 1D8V_AUX_S5

2017/08/03 change 074.09078.003F from 074.01339.0D3F

PU5451 RT9078-18GJ5-GP 074.09078.003F

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8386RHC_1D8V)

Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 54 of 106

Main Func = LCD

[8] eDP_AUX_CPU_N
[8] eDP_AUX_CPU_P
[8] eDP_TX_CPU_N0
[8] eDP_TX_CPU_P0
[8] eDP_TX_CPU_N1
[8] eDP_TX_CPU_P1
[16,17] DBC_PANEL_EN
[24] LCD_TST
[24] BLON_OUT
[8] eDP_HPD_CPU
[17] TOUCH_PANEL_DET#
[17] CPU_I2C_SCL_TS_R
[17] CPU_I2C_SDA_TS_R
[24] EC_BRIGHTNESS
[24] LCD_TST_EN
[24] TOUCH_REPORT_SW
[8] eDP_VARY_BL
[8] eDP_DIGON
[17,70] SENSOR_I2C_SDA
[17,70] SENSOR_I2C_SCL
[7] GSEN_INT1_C

0513

INVERTER POWER

19V_DCBATOUT → 800mA → F5503 POLYSW-1D1MSV-2-GP-U 69.50007.A31 → DCBATOUT_LCD_R → R5514 0R7R2F-1-GP → DCBATOUT_LCD
C5515 10U/25V/X5R/K/0805 ×2 (20200714)
C5516 0.1U/50V/X7R/K/0603 ×2 (20200714)

LCDVDD

Layout Note:
Trace width = 80mil

3D3V_LCDVDD_S0 → R5521 0R2J-2-GP → 3D3V_LCDVDD_R
C5503 Do Not Stuff (20191227)
Hi:2.9V Lo:0.8V
LCDVDD Layout 80 mil
U5301 RT9742CGJ5-GP 074.09742.0A9F
20180419 follow Common part
3D3V_S5 → C5504 SCR7C1E0X226KX-1-GP (20200714)
eDP_PWR_EN → Q5502 BAT54C-1E-GP 75.00054.A7D → R5506 100KR2J-1-GP → LCDVDD_EN

EC (BIST MODE)

Brightness
A00 Change R to 0ohm to short pad 20181220
EC_BRIGHTNESS → R5226 0R2J-2-GP → EC_BRIGHTNESS_R
R5504 Do Not Stuff
R5224 1 DY 2 Do Not Stuff
D5501 BAT54C-1E-GP 75.00054.A7D
LCD_TST → R5505 100KR2J-1-GP
BLON_OUT_C → R5503 100KR2J-1-GP
eDP_BKLT_CTRL → R5504 100KR2J-1-GP
Swap 20180725
SRN100J-3-GP: LCD_BRIGHTNESS / BKLT_CTRL
SRN100J-3-GP: LCD_TST_C / EDP_HPD_CONN

20200728

3D3V_S0 → R5574 Do Not Stuff → R5563 470R2J-2-GP → R5564 10R2F-3-GP 2018091 4.7R->10R
eDP_BKLT_CTRL → Q5503 2N7002KDW-1-GP
eDP_VARY_BL → R5582 2K2R2J-2-GP → Q5503_C
Q5501_R → Q5501 UM6T3904LTTG-GP
1st = 84.T3904.H11
2nd = 84.03904.J11
3rd = 84.03904.T11

3D3V_S0 → R5575 Do Not Stuff → R5566 470R2J-2-GP → R5567 1KR7R2J-2-GP
eDP_PWR_EN → Q5505_C
eDP_DIGON → R5571 10KR2F-2-GP → R5585 2K2R2J-2-GP → Q5504_R
Q5504 UM6T3904LTTG-GP
1st = 84.T3904.H11
2nd = 84.03904.J11
3rd = 84.03904.T11

Camera DMIC / LCD / Touch Panel

LCD1 → 5V_TPAN_VDD, 3D3V_CAMERA_S5, LCD_BRIGHTNESS_CON_N, LCD_BRIGHTNESS_CON_P, DMIC_DATA_EDP_CONN, DMIC_CLK_EDP_CONN, SENSOR_I2C_SDA, SENSOR_I2C_SCL, CAMERA_RST_C, 3D3V_S0_SENSOR, DBC_PANEL_EN_N, eDP_TX_CON_N1, eDP_TX_CON_P1, eDP_TX_CON_N0, eDP_TX_CON_P0, eDP_AUX_CON_N, eDP_AUX_CON_P, 3D3V_LCDVDD_S0, LCD_TST_C, EDP_HPD_CONN, BLON_OUT_C, LCD_BRIGHTNESS, TOUCH_PANEL_DET#, TOUCH_REPORT_SW, I2C_SCL_TS_C, I2C_SDA_TS_C, TOUCH_PANEL_INT#, TOUCH_PANEL_PD#, DCBATOUT_LCD, 3D3V_TPAN_VDD
F5501 POLYSW-1D1MSV-9-GP-U 69.48001.081
R5518 100R2J-2-GP
C5534 SCD1U16V2KX-3DLGP
C5537 SCD1U16V2KX-3DLGP
C5508 SCD1U16V2KX-3DLGP
C5532 SCD1U16V2KX-3DLGP
C5531 SCD1U16V2KX-3DLGP
C5533 SCD1U16V2KX-3DLGP
EC5504 2 DY 1 Do Not Stuff
STAR-CON45-6-GP 020.F0847.0040 (20200806)

3D3V_LCDVDD_S0

Trace width = 80mil
C5599 SCD1U10V2KX-GP
C5536 SCD1U10V2KX-GP
C5538 SCD1U10V2KX-GP
(20200714)
Layout notes: Close to LCD1

PU/PD FOR AUX CHANNEL

SKL PDG (#543016):
Recomends having a pull-up resistor of 100 kΩ for AUXN
and a pull-down resistor of 100 kΩ for AUXP
between the AC capacitor and the connector,

eDP_AUX_CON_P → R5528 1 DY 2 Do Not Stuff → 3D3V_S0
eDP_AUX_CON_N → R5529 1 DY 2 Do Not Stuff → 3D3V_S0

TOUCH_PANEL_PD# / TOUCH_PANEL_INT#

TOUCH_PANEL_PD# → TOUCH_PANEL_PD# (CN)
TOUCH_PANEL_INT# → TOUCH_PANEL_INT# (CN)
CPU_I2C_SDA_TS_R → R5577 1 2 33R2J-2-GP → CPU_I2C_SDA_TS
CPU_I2C_SCL_TS_R → R5576 1 2 33R2J-2-GP → CPU_I2C_SCL_TS
EC5505 CPU_I2C_SDA_TS / CPU_I2C_SCL_TS
XD104/24P-RTG-GP 075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003
(20200807)

Main Func = CAMERA

[24] PANEL_MONITOR

Need to define U2401support :PANEL_MONITOR

[18] CCD_USB20_N
[18] CCD_USB20_P
[27] DMIC_DATA
[27] DMIC_CLK
[17] DMIC_DATA_EDP
[17] DMIC_CLK_EDP

CAMERA POWER

3D3V_S5 → D5702 D01FR2J-L-GP → R5573 → 3D3V_CAMERA_R → F5504 POLYSW-1D1A6V-9-GP-U 69.48001.081 → 3D3V_CAMERA_S5
R5519 1 DY 2 Do Not Stuff
EC5503 (20200714)

CCD_USB20_N / CCD_USB20_P → EL5501 FLT6R-4P-1-GP 68.02002.061 → CCD_USB20_CON_N / CCD_USB20_CON_P
R5585 1 DY 2 Do Not Stuff
R5556 1 DY 2 Do Not Stuff

PANEL_PWRGD CIRCUIT

3D3V_LCDVDD_S0 → R5517 100KR2J-1-GP → PANEL_PWRGD_R → R5515 0R2J-2-GP → PANEL_MONITOR
3D3V_S5 → R5513 1MR2J-1-GP → BL_PWR_MONITOR
Q5505 L2N7002KDW1T1G-GP
R5516 Do Not Stuff
DCBATOUT_LCD → Q5502 L2N7002KDW1T1G-GP
C5507 SCD1U25V2KX-1-DL-GP
(20200707)

Codec
DMIC_DATA → R5502 1 DY 2 Do Not Stuff → DMIC_DATA_EDP
DMIC_CLK → R5503 1 DY 2 Do Not Stuff → DMIC_CLK_EDP
Layout Note: Reduce the stubs.

DMIC_DATA_EDP / DMIC_CLK_EDP → EL5502 BLM15AG121SN1-1GP → DMIC_DATA_EDP_CONN / DMIC_CLK_EDP_CONN
EL5503 BLM15AG121SN1-1GP
EC5502 (if S/I PN'd)
EC5501 Do Not Stuff

Layout Note: Close to LCD1
Need to define U2401support :PANEL_MONITOR

Main Func = Touch panel

[17] TOUCH_PANEL_INT#
[17] TOUCH_PANEL_PD#
[17,24,40,51,52] APU_SLP_S3#

Touch Panel

TOUCH_PANEL_INT# → C5541 Do Not Stuff
TOUCH_PANEL_PD# → C5540 Do Not Stuff
Touch Panel PR internally.
R5599 1 DY 2 Do Not Stuff → TOUCH_PANEL_INT#
(20190802)

TOUCH PANEL POWER

5V_S0 → F5506 Do Not Stuff → 5V_TPAN_VDD
Do Not Stuff
(20200807)

5V_S0 → R5512 0R2J-2-GP → C5
3D3V_S0 → R5507 Do Not Stuff → C5
3V5V_TPAN_VDD → R5501 0R2J-2-GP → 3V5V_TPAN_VDD_R → F5505 POLYSW-1D1A6V-9-GP-U 69.48001.081 → 3D3V_TPAN_VDD
C5501 SCD1U10V2KX-3DLGP
C5502 SCD1U10V2KX-3DLGP
(20200915)

CB 14 N

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00
Date: Friday, October 23, 2020 | Sheet 55 of 106

(Blanking)

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 56 of 106

Main Func = HDMI

[8] HDMI_DDI_TX_N0
[8] HDMI_DDI_TX_P0
[8] HDMI_DDI_TX_N1
[8] HDMI_DDI_TX_P1
[8] HDMI_DDI_TX_N2
[8] HDMI_DDI_TX_P2
[8] HDMI_DDI_TX_N3
[8] HDMI_DDI_TX_P3

[8] HDMI_DET_CPU

[8] HDMI_SCL_CPU
[8] HDMI_SDA_CPU

HDMI_DDI_TX_N3 C5714 1 2 SCD1U16V2KX-3DLGP HDMI_CLK#_R_C
HDMI_DDI_TX_P3 C5709 1 2 SCD1U16V2KX-3DLGP HDMI_CLK_R_C
HDMI_DDI_TX_P2 C5707 1 2 SCD1U16V2KX-3DLGP HDMI_DATA2_R_C
HDMI_DDI_TX_N2 C5710 1 2 SCD1U16V2KX-3DLGP HDMI_DATA2#_R_C
HDMI_DDI_TX_N1 C5715 1 2 SCD1U16V2KX-3DLGP HDMI_DATA1#_R_C
HDMI_DDI_TX_P1 C5712 1 2 SCD1U16V2KX-3DLGP HDMI_DATA1_R_C
HDMI_DDI_TX_P0 C5711 1 2 SCD1U16V2KX-3DLGP HDMI_DATA0_R_C
HDMI_DDI_TX_N0 C5708 1 2 SCD1U16V2KX-3DLGP HDMI_DATA0#_R_C

3D3V_S0

R5717 499R2F-2-GP
R5718 499R2F-2-GP
R5720 499R2F-2-GP
R5732 499R2F-2-GP
R5706 499R2F-2-GP
R5707 499R2F-2-GP
R5713 499R2F-2-GP
R5714 499R2F-2-GP

R5719 DY Do Not Stuff
Q5701 PJE8408-R1-00001-GP
084.08408.0031
20191211
HDMI_PLL_GND

R5708 DY Do Not Stuff

Change to 150 ohm by EMI 20180507

HDMI_CLK_R_C → R5705 150R2F-1-GP → HDMI_CLK#_R_C
HDMI_DATA2#_R_C → R5702 150R2F-1-GP → HDMI_DATA2_R_C
HDMI_DATA0#_R_C → R5703 150R2F-1-GP → HDMI_DATA0_R_C
HDMI_DATA1_R_C → R5704 150R2F-1-GP → HDMI_DATA1#_R_C

HDMI CONN

5V_HDMI_S0
C5713 SCD1U16V2KX-3DLGP

HDMI1
+5V_POWER
HDMI_DATA0_R_C / HDMI_DATA0#_R_C
HDMI_DATA1_R_C / HDMI_DATA1#_R_C
HDMI_DATA2_R_C / HDMI_DATA2#_R_C
TMDS_DATA0+ TMDS_DATA0- TMDS_DATA1+ TMDS_DATA1- TMDS_DATA2+ TMDS_DATA2-
TMDS_DATA0_SHIELD TMDS_DATA1_SHIELD TMDS_DATA2_SHIELD
HDMI_CLK_R_C / HDMI_CLK#_R_C
TMDS_CLOCK_SHIELD TMDS_CLOCK+ TMDS_CLOCK-
SCL SDA
CEC DDC/CEC_GROUNG HOT_PLUG_DETECT
RESERVED#14
GND GND GND GND
DDC_CLK_HDMI DDC_DATA_HDMI HPD_HDMI_CON
HDMI (A_Type)
SKT-HDMI23-260-GP
022.10025.0831
20200915

5V_S0
D5702 BAW56-9-GP-U
75.00056.07D
20200713
Swap 20191218

3D3V_S0
Swap 20180725
RN5704 SRN4K7J-8-GP
HDMI_SCL_CPU
HDMI_SDA_CPU
Q5705 2N7002KDW-1-GP
Vgs=2.5V
DDC_CLK_PH1
DDC_DATA_PH2
RN5702 SRN2K2J-1-GP
DDC_CLK_HDMI
DDC_DATA_HDMI

84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11

3D3V_S0
Q5703 LMBT3904LT1G-GP
HDMI_DET_CPU
R5712 0R2J-2-GP
HDMI_HPD_E
HDMI_HPD_B
R5710 150KR2F-L-GP
R5711 200KR2F-L-GP
R5709 100KR2J-1-GP
HPD_HDMI_CON

5V_S0
F5701 POLYSW-1D1A6V-9-GP-U
5V_HDMI_S0
20190807
69.48001.081
2nd = 69.50011.081

ED5701 AZ1043-04F-R7G-GP
HDMI_DATA2_R_C / HDMI_DATA2#_R_C
HDMI_DATA1_R_C / HDMI_DATA1#_R_C
075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003

ED5702 AZ1043-04F-R7G-GP
HDMI_CLK#_R_C / HDMI_CLK_R_C
HDMI_DATA0#_R_C / HDMI_DATA0_R_C
075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003

ED5703 AZ1043-04F-R7G-GP
HPD_HDMI_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003

20200714

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Title: HDMI
Size: A3
Document Number: Watchmen/Cyborg AMD
Rev: X00
Date: Friday, October 23, 2020
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(Blanking)

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Title
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Size	Document Number	Rev
A3	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 58 of 106

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Title
(Reserved)

Size	Document Number	Rev
A3	***Watchmen/Cyborg AMD***	*X00*

Date: Friday, October 23, 2020 Sheet 59 of 106

Main Func = HDD

(Blanking)

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Title: SATA IF_HDD/ODD

Size: A3 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 60 of 106

Main Func = WLAN

PCIE

[3] WLAN_PCIE_TX_N
[3] WLAN_PCIE_TX_P
[3] WLAN_PCIE_RX_N
[3] WLAN_PCIE_RX_P

PCIE_CLK

[16] WLAN_CLK_CPU_N
[16] WLAN_CLK_CPU_P
[16] WLAN_CLKREQ_CPU_N

USB2.0

[18] BT_USB20_P
[18] BT_USB20_N

[17] WAKE_L
[17,24,63,91] PLT_RST#
[17] UART_WAKE#_APU
[16] SUS_CLK_CPU

Power EN

[24] AUX_EN_WOWL
[24] EC_STRAP
[24] JIO3_PCIE_WAKE#

UART

[16] APU_UART_PTX_DRX
[16] APU_UART_PRX_DTX
[16] APU_UART_PTX_DRX_RTS#
[16] APU_UART_PRX_DTX_CTS#

[24] M2_BT_WAKE#
[17] DOUT_BT_M2
[17] BCLK_BT_M2
[17] LRCLK_BT_M2
[17] SDIN_BT_M2

3D3V_WLAN
2A
C6110
C6108
C6109
SCD1U16V2KX-1DL-GP
20180912 0603->0805

3D3V_S5
R6101
JIO3_PCIE_WAKE#
10KR2J-3-GP

3D3V_WLAN
R6108
DY
M2_BT_WAKE#_R
Do Not Stuff

3D3V_S5
1A
C6103
SCD1U16V2KX-3DLGP
R6137
10KR2J-3-GP
C6104
SCD1U16V2KX-3DLGP
R6138
20KR2J-L2-GP
WLAN_EN_R#
WLAN_EN#
Q6101
PJA3415AE-GP
084.03415.0C31
C6101
SCS150V2KX-4GP
FC6101

3D3V_WLAN_R
3D3V_WLAN
R6143
D01R3F-L-GP

AUX_EN_WOWL
R6136
0R2J-2-GP
3D3V_WLAN_EN
Q6102
2N7002K-2-GP-U
84.2N702.I31
2ND = 84.2N702.031
3rd = 84.07002.I31
2017.10.25
Change Location
Connector list v8

3D3V_WLAN
R6107
10KR1J-GP
UART_WAKE#_APU
UART_WAKE#
Q6103
PJE8408-R1-00001-GP
084.08408.0031

20190723
3D3V_WLAN
U6103
SUS_CLK_CPU
SUS_CLK
DY
Do Not Stuff
GP
Do Not Stuff
2nd = 073.74134.0A0G

Note:pin 76 and pin 77 need contact to GND
R6105 can be no load for QC NFA564 only.
C6111
Do Not Stuff
C6112
Do Not Stuff
WLAN1
WIFI_RF_EN_R
BLUETOOTH_EN_R
PLT_RST#_WLAN
SUS_CLK_R
R6105
Do Not Stuff
M2_BT_WAKE#
R6121
0R1J-GP
M2_BT_WAKE#_R
UART_PTX_DRX_RTS#
UART_PRX_DTX_CTS#
UART_PTX_DRX
UART_PRX_DTX
UART_WAKE#
R6120
0R1J-GP
UART_WAKE#_R1
DOUT_BT_M2
SDIN_BT_M2
LRCLK_BT_M2
BCLK_BT_M2
NGFF_KEY_E_75P
SKT-NGFF75P-164-GP
062.10003.0B11
3.3V
JIO3_PCIE_WAKE#
WLAN_CLKREQ_CPU_N
WLAN_CLK_CPU_N_R
WLAN_CLK_CPU_P_R
R6104
0R2J-2-GP
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
20190813
WLAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_TX_N
WLAN_PCIE_TX_P
BT_USB20_CON_N
BT_USB20_CON_P

BT_USB20_CON_P
R6111
0R2J-2-GP
BT_USB20_P
EL6101
DY
Do Not Stuff
Do Not Stuff
BT_USB20_CON_N
R6110
0R2J-2-GP
BT_USB20_N

3D3V_WLAN
R6126
10KR2J-3-GP
R6127
DY
Do Not Stuff
PLT_RST#_WLAN
PLT_RST#
D6105
RB551V30-GP
EC_STRAP
D6106
RB551V30-GP

Do Not Stuff AFTP6101 3D3V_WLAN
Do Not Stuff AFTP6105 WLAN_CLKREQ_CPU_N
Do Not Stuff AFTP6106 WIFI_RF_EN_R
Do Not Stuff AFTP6107 BLUETOOTH_EN_R
Do Not Stuff AFTP6108 PLT_RST#
Do Not Stuff AFTP6109 WAKE_L

3D3V_S0
20190820
U6120
APU_UART_PTX_DRX
UART_PTX_DRX
SN74LVC1G07DRLR-GP
73.01G07.02G

1D8V_S0
20190820
U6122
UART_PRX_DTX
APU_UART_PRX_DTX
SN74LVC1G07DRLR-GP
73.01G07.02G

3D3V_S0
20190820
U6121
APU_UART_PTX_DRX_RTS#
UART_PTX_DRX_RTS#
SN74LVC1G07DRLR-GP
73.01G07.02G

1D8V_S0
20190820
U6123
UART_PRX_DTX_CTS#
APU_UART_PRX_DTX_CTS#
SN74LVC1G07DRLR-GP
73.01G07.02G

1D8V_S0
UART_PTX_DRX
R6154
1KR2J-1-GP
UART_PTX_DRX_RTS#
R6155
1KR2J-1-GP
UART_PRX_DTX
R6156
100KR2J-1-GP
UART_PRX_DTX_CTS#
R6157
100KR2J-1-GP

3D3V_S0
APU_UART_PRX_DTX
R6158
1KR2J-1-GP
APU_UART_PRX_DTX_CTS#
R6159
1KR2J-1-GP
20190902
APU_UART_PTX_DRX
R6160
DY
Do Not Stuff
APU_UART_PTX_DRX_RTS#
R6161
DY
Do Not Stuff
DY ON AMD CKT

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Taipei Hsien 221, Taiwan, R.O.C.
Title
NGFF_WLAN CONN
Size A2
Document Number Watchmen/Cyborg AMD
Rev X00
Date: Friday, October 23, 2020
Sheet 61 of 106

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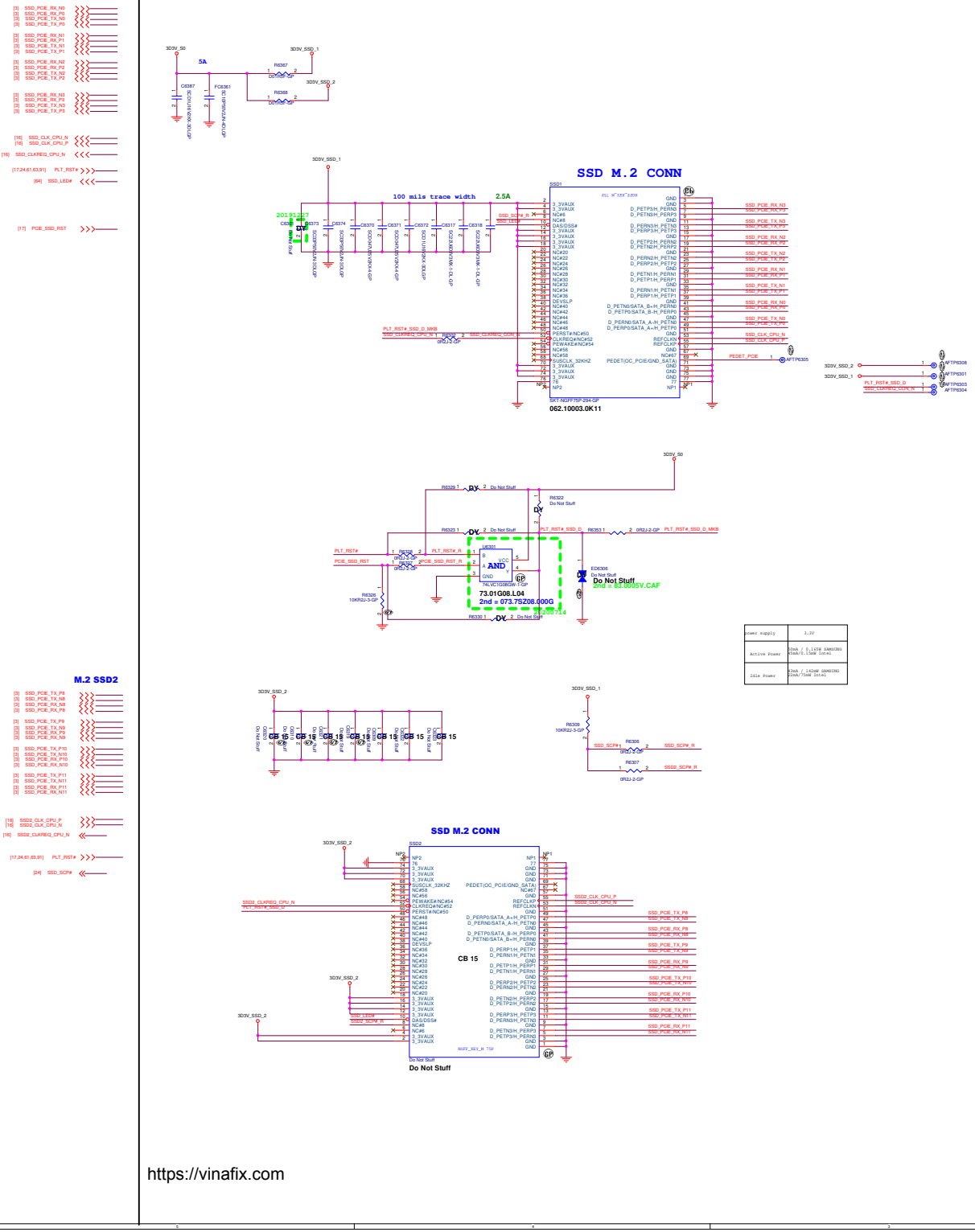
Title

Reserved

Size	Document Number	Rev
A4	***Watchmen/Cyborg AMD***	*X00*

Date: Friday, October 23, 2020 Sheet 62 of 106

SSD = M.2



power supply	3.3V
Active Power	45mA / 0.145W SAMSUNG 45mA/0.15mW Intel
Idle Power	43mA / 142mW SAMSUNG 22mA/75mW Intel

CB 14 N

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File:

INT IO (SSD M.2)

Size	Document Number	Rev
A1	Watchmen/Cyborg AMD	X00

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Main Func = Power BTN

[24] LID_CL_SIO#
[24] KBC_PWRBTN#
[67] LID_CLOSE#_MR1
[66] KBC_PWRBTN#_R

Low actived from KBC GPIO

0.1u->1KP By EMI check 20180808

For EMI Reserved

LID_CLOSE#_MR1 EC6401 1 DY 2 Do Not Stuff

Power button

Layout note:
G6401 place to buttom
G6402 place to top

RN6401 20190829
LID_CL_SIO# 2
KBC_PWRBTN# 1
4
SRN0J-6-GP
LID_CLOSE#_MR1
KBC_PWRBTN#_R
swap 20180808

EC6403 Do Not Stuff DY
ED6402 DY
ED6401 Do Not Stuff DY
Do Not Stuff
2nd = 83.0005V.CAF
G6401 Do Not Stuff
C6401 Do Not Stuff DY
3D3V_S5

83.05725.0A0
2nd = 83.0005V.CAF

Main Func = Battery LED

[24] CHG_AMBER_LED#
[24] BATT_WHITE_LED#

Low actived from KBC GPIO

Q6403 LDTA114EET1G-GP
CHG_AMBER_LED# 1 R6405 2 CHG_AMBER_LED_R#
0R2J-2-GP
B E C
5V_S5
AMBER_LED_BAT
20191211
084.00114.0013

A00 Change 0 ohm to short pad 20181220

EC6402 Do Not Stuff DY
0.1u->1KP By EMI 20180808

Q6404 LDTA114EET1G-GP
BATT_WHITE_LED# 1 R6404 2 BATT_WHITE_LED_R#
0R2J-2-GP
B E C
5V_S5
WHITE_LED_BAT
20191211
084.00114.0013

Low actived from KBC GPIO

EC6404 Do Not Stuff DY
0.1u->1KP By EMI 20180808

Battery LED1 (AMBER_LED)

Follow Bucky 20180816

R6407
1 2 BAT_AMBER
499R2F-2-GP

LED1
LED-YW-5-GP
083.1212A.0070

Battery LED2(WHITE_LED)

R6406
1 2 BAT_WHITE
549R2F-GP

Main Func = HDD LED

[24] SATA_LED#
[17] SATA_ACT#
[63] SSD_LED#

https://vinafix.com

SATA HDD LED
LOW actived from PCH GPIO

EVT 0509 :Copy Intel

3D3V_S0
R6401
10KR2J-3-GP
SATA_LED#

D6401
SATA_ACT# 1
SSD_LED# 2
3
BAT54A-11-GP
75.BAT54.07D

SATA_LED#_D
Q6401
PJE8438-GP
S D G
BATT_WHITE_LED#
084.08438.0A31

Add SSD LED function_20170920

Layout note:
G6401 place to buttom
G6402 place to top

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Title: LED Board&Power Button
Size: A3
Document Number: Watchmen/Cyborg AMD
Rev: X00
Date: Friday, October 23, 2020
Sheet 64 of 106

Main Func = KB

20180402

[24] CAP_LED#_D

[24] KSI[0..7]

[24] KSO[0..16]

[16] KB_DET#

[17] KB_LED_BL_DET

[24] KB_LED_PWM

Keyboard Backlight (Reserved)

5V_S0 → F6502 69.48001.081 POLYSW-1D1A6V-9-GP-U → +5V_KB_BL

C6501 SCD1U16V2KX-3DLGP

KBBL1 → ACES-CON4-90-GP-U 020.K0298.0004 → AFTP6565

KB_LED_BL_DET → R6503 51KR2J-1-GP → KB_LED_DET_C

KB_BL_CTRL# → R6507 100KR2J-1-GP DY Do Not Stuff → C6502

Q6501 PJA138KA-GP
084.00138.0A31
2nd = 084.00138.0C31
20200914

KB Backlight Power Consumption: 285mA max.

KB_LED_PWM → R6505 Do Not Stuff

+5V_KB_BL → AFTP6605

KB_LED_BL_DET → AFTP6606

KB_BL_CTRL# → AFTP6607

CAP LED Control

LOW actived from KBC GPIO

CAP_LED#_D → R6508 0R2J-2-GP → CAP_LED#_R → Q6502 LDTA114EET1G-GP → CAP_LED_Q → R6506 1KR2J-1-GP → CAP_LED

5V_S0

084.00114.0013

EC6505 DY Do Not Stuff

Internal Keyboard Connector

KB1 → ACES-CON30-29-GP 020.K0254.0030

CAP_LED

AFTP6532 CAP_LED
AFTP6503 KSO10
AFTP6506 KSO11
AFTP6516 KSO9
AFTP6539 KSO14
AFTP6535 KSO13
AFTP6515 KSO15
AFTP6508 KSO16
AFTP6538 KSO12
AFTP6520 KSO0
AFTP6510 KSO2
AFTP6517 KSO1
AFTP6518 KSO3
AFTP6505 KSO8
AFTP6512 KSO6
AFTP6534 KSO7
AFTP6522 KSO4
AFTP6536 KSO5
AFTP6507 KSI0
AFTP6502 KSI3
AFTP6540 KSI1
AFTP6513 KSI5
AFTP6533 KSI2
AFTP6521 KSI4
AFTP6511 KSI6
AFTP6523 KSI7
AFTP6519 KB_DET#

Main Func = TPAD

[24] TP_WAKE_KBC#

[17] TP_WAKE_CPU#

[24] TP_ON#

[24] TP_LOCK#

[24] CLK_TP_SIO

[24] DAT_TP_SIO

[17,66] CPU_I2C_SCL_P3

[17,66] CPU_I2C_SDA_P3

BOM SELECT TP_WAKE — NO STUFF NON TP_WAKE

3D3V_S5 → R6521 D01R2J-L-GP → 3D3V_TP_VDD

Q6504 PJA3415AE-GP
084.03415.0C31

C6503 SCD1U16V2KX-3DLGP

TP_ON# → R6516 1KR2J-1-GP → TP_ON#_GATE

TP_ON#_GATE → Q6505 PJE8408-R1-00001-GP
084.08408.0031

R6522 100R3J-4-GP → Q6205_Q

TP_VDD Discharge Circuit

Follow RR

3D3V_TP_VDD, 3D3V_TP_VDD, 3D3V_S5

R6511 10KR2J-3-GP

R6515 10KR2J-3-GP

Q6506 PJE8408-R1-00001-GP
084.08408.0031

TP_WAKE_KBC# → TP_WAKE_CPU#

R6523 DY Do Not Stuff

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

3D3V_TP_VDD → R6509 100KR2J-1-GP → TP_LOCK#

Precision Touch Pad Connector

PIN DEFINE

3D3V_TP_VDD

C6504 SCD1U16V2KX-3DLGP

R6513 DY Do Not Stuff

AFTP6531

TP1 → PTWO-CON8-16-GP 020.K0255.0008

CPU_I2C_SDA_TP
CPU_I2C_SCL_TP
TP_WAKE_KBC#
TP_LOCK#
TPDATA_C
TPCLK_C

3D3V_TP_VDD
TPCLK_C → AFTP6529
TPDATA_C → AFTP6530
CPU_I2C_SCL_TP → AFTP6524
CPU_I2C_SDA_TP → AFTP6528
TP_WAKE_KBC# → AFTP6527
TP_LOCK# → AFTP6525
AFTP6526

Support PTP

PS2

3D3V_TP_VDD

RN6504 SRN10KJ-5-GP

CLK_TP_SIO
DAT_TP_SIO

RN6503 SRN33J-5-GP-U → TPCLK_C, TPDATA_C

Need to check with SW.

EC6503 DY Do Not Stuff

EC6504 DY Do Not Stuff

Follow RR

I2C

APU

device

3D3V_TP_VDD, 3D3V_S5

A00 Change 0 ohm to short pad 20181220

R6512 0R2J-2-GP

RN6502 SRN2K2J-1-GP

RN6505 SRN2K2J-1-GP

Q6204_G

Q6503 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.67002.007C

CPU_I2C_SCL_P3 → CPU_I2C_SCL_TP

CPU_I2C_SDA_P3 → CPU_I2C_SDA_TP

EC6504 DY Do Not Stuff

EC6502 DY Do Not Stuff

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Title: Key Board&Touch Pad

Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 65 of 106

Main Func = IO Connector

AUDIO

[27,29] AUD_RING
[27,29] AUD_SLEEVE
[29] AUD_HP1_JACK_L1
[29] AUD_HP1_JACK_R1
[27] AUD_SENSE

CRD

[18] CARD1_USB20_N
[18] CARD1_USB20_P

USB3.0

PORT1

[18] USB2_USB30_RX_N
[18] USB2_USB30_RX_P
[18] USB2_USB30_TX_N
[18] USB2_USB30_TX_P
[18] USB2_USB20_N
[18] USB2_USB20_P
[24] KB_CLOSE#_2

I2C

[17,65] CPU_I2C_SCL_P3
[17,65] CPU_I2C_SDA_P3

LAN

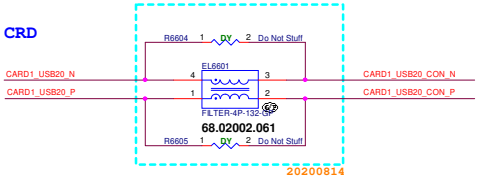
[3] LAN_PCIE_RX_N
[3] LAN_PCIE_RX_P
[3] LAN_PCIE_TX_N
[3] LAN_PCIE_TX_P
[16] LAN_CLK_CPU_N
[16] LAN_CLK_CPU_P
[16] LAN_CLKREQ_CPU_N
[24] PM_LAN_ENABLE
[24] PCIE_LAN_WAKE#

FP

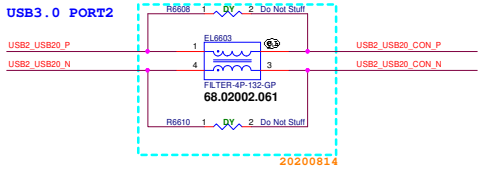
[18] FP1_USB20_N
[18] FP1_USB20_P
[24] FPR_SCAN#
[24,64] LID_CL_SIO#
[64] KBC_PWRBTN#_R

[17,24,51] APU_SLP_S5#
[24] PLT_RST#_LAN
[44] PWR_CHG_VBATIN
[17,24,61,83,91] PLT_RST#
[67] LID_C1_NB#

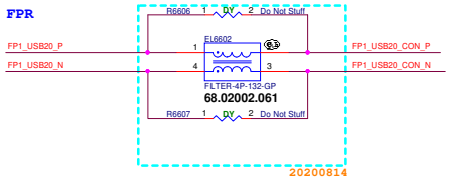
CRD



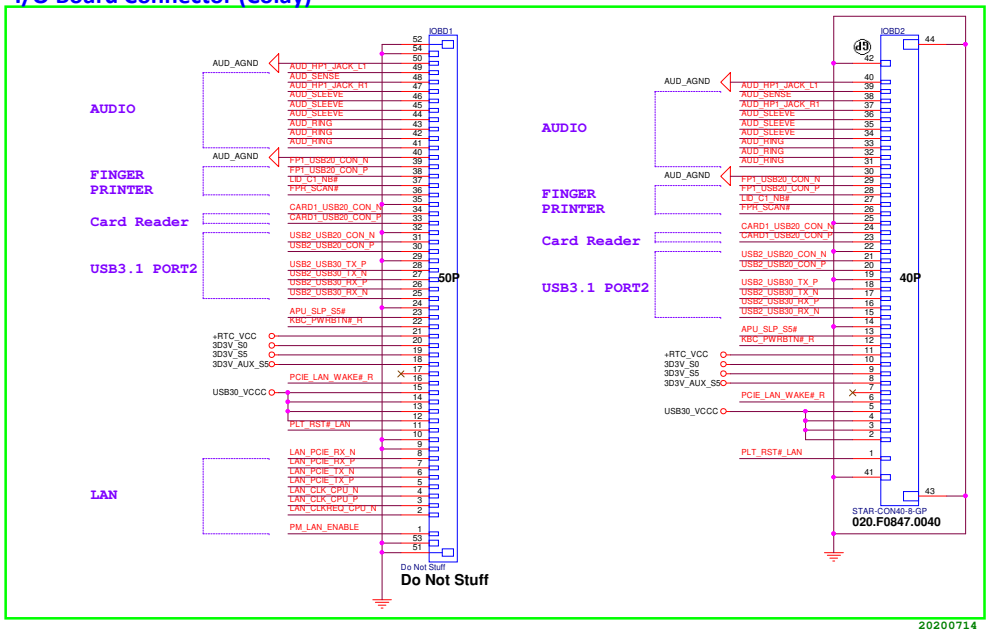
USB3.0 PORT2



FPR

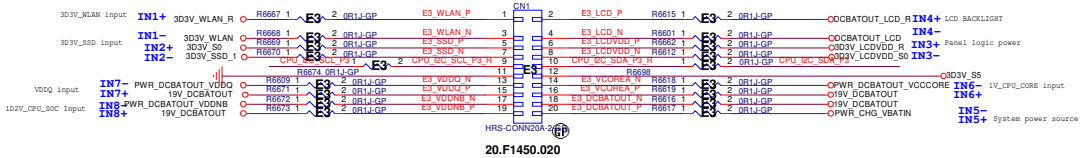


I/O Board Connector (Colay)



E3

4mil for trace width and trace to trace .



20.F1450.020

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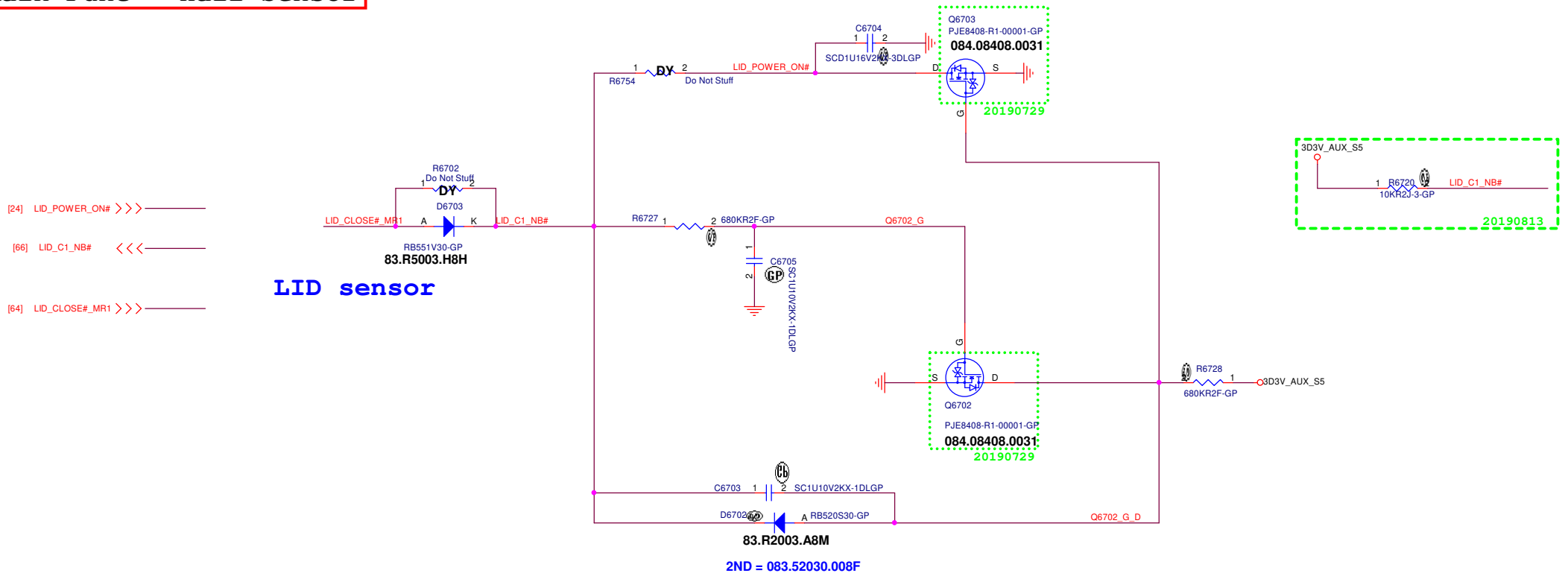
Title: IO Board Connector

Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 66 of 106

Main Func = Hall Sensor



CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LID Sensor

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 67 of 106

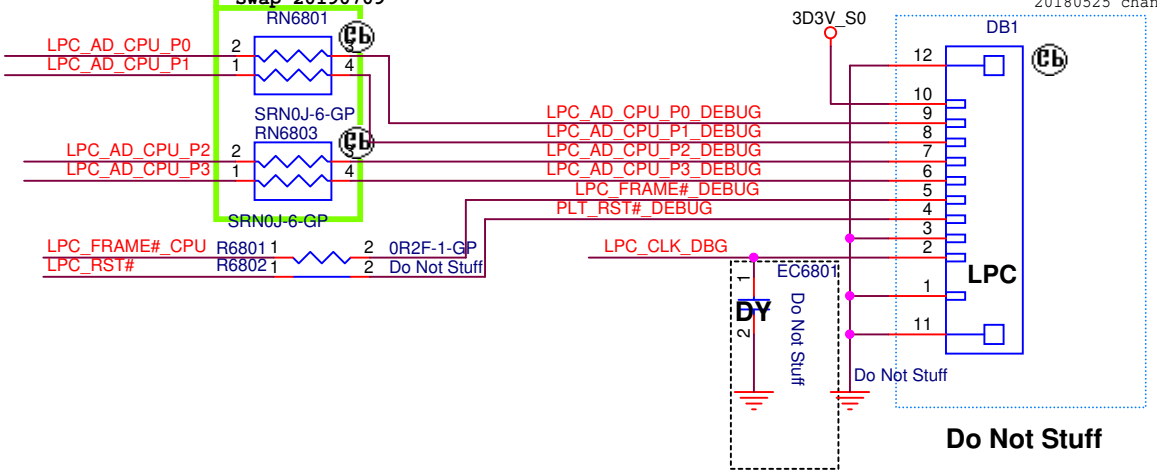
SSID = DEBUG PORT

[16,24] LPC_AD_CPU_P0
[16,24] LPC_AD_CPU_P1
[16,24] LPC_AD_CPU_P2
[16,24] LPC_AD_CPU_P3
[16,24] LPC_FRAME#_CPU
[16,24,91] LPC_RST#
[16] LPC_CLK_DBG
[8] APU_TCK
[8] APU_TMS
[8] APU_TDI
[8] APU_TDO
[8,46] SVID_PWRGD
[8,72] RST#_CPU
[8] APU_DBREQ#
[8] APU_TRST#

Layout Note:
Place near trace separated point.
Swap 20190709

Debug Connector

20180525 change to conn



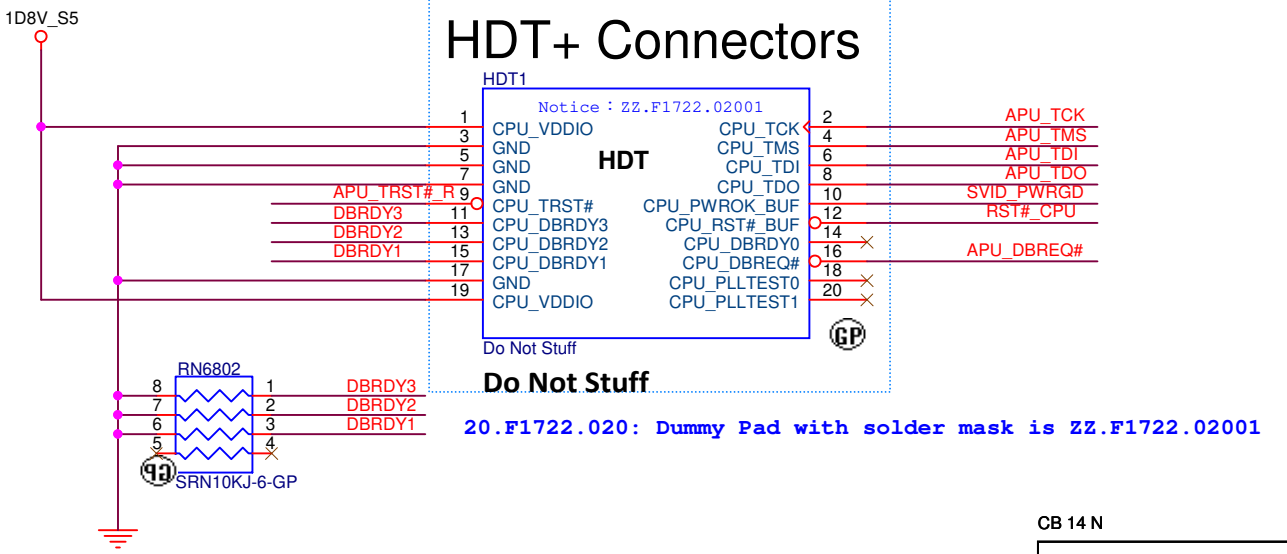
Do Not Stuff

RF request 2017/11/08 modify

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.
20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

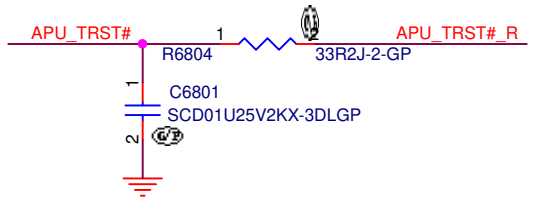
20180525 change to conn

HDT+ Connectors



Do Not Stuff

20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001



CB 14 N

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Title: Dubug connector

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 68 of 106

Sensor HUB

(Blanking)

CB 14 N

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor HUB

Size: A3 | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 69 of 106

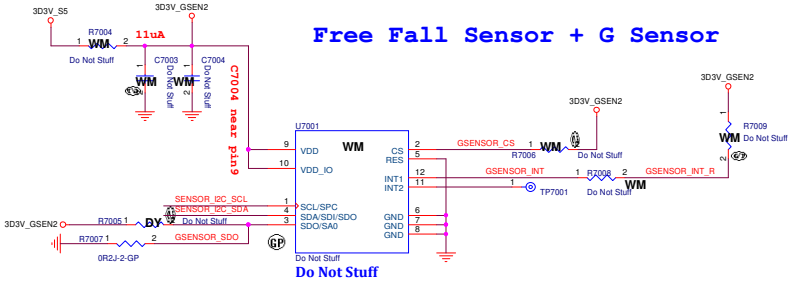
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

[17,55] SENSOR_I2C_SCL
[17,55] SENSOR_I2C_SDA
[17] GSENSOR_INT_R

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I^2C lines.

Free Fall Sensor + G Sensor



Do Not Stuff

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

CB 14 N

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Title: Free Fall Sensor

Size	Document Number	Rev
A2	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 70 of 106

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Type C PD (CCG4)***

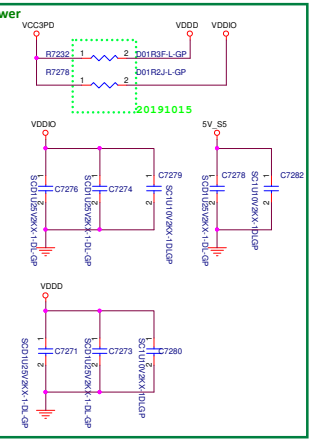
Size	Document Number	Rev
A3	***Watchmen/Cyborg AMD***	***X00***

Date: Friday, October 23, 2020 Sheet 71 of 106

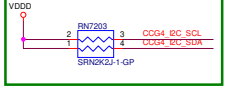
Main Func = CCG4

[24] CCG4_I2C_INT#_EC
[24] CCG4_I2C_SCL
[24] CCG4_I2C_SDA
原本24pin有
[74] FAST_ON_TP1
[73] TUSB544_EN#
[8,73] CPU_DP_HPD
[73] USBC1_CC2_CONN
[73] USBC1_CC1_CONN
[72,74] PD_VBUS_C_CTRL1
[18,73] CCG4_APU_USBC_SDA
[18,73] CCG4_APU_USBC_SCL
[8,68] RST#_CPU

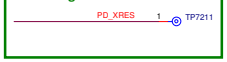
Power



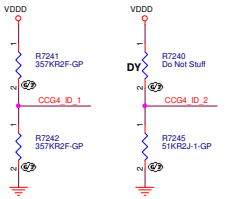
I2C to KBC

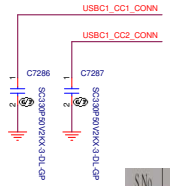


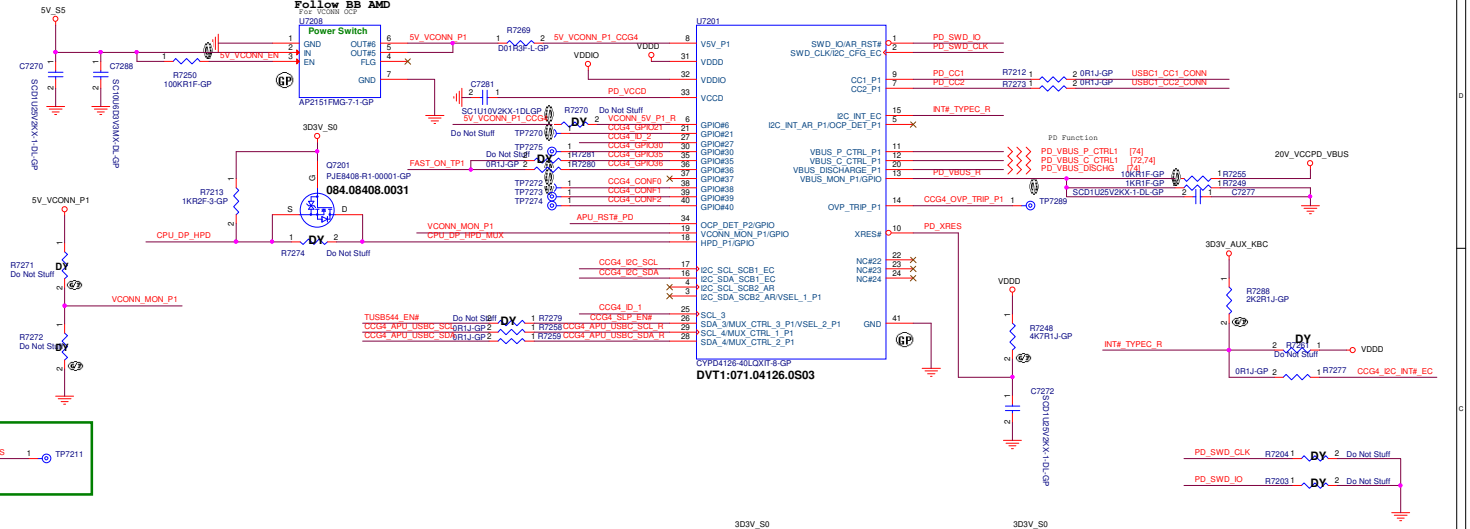
For Debug

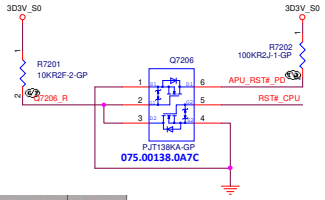


Platform Detect Pin



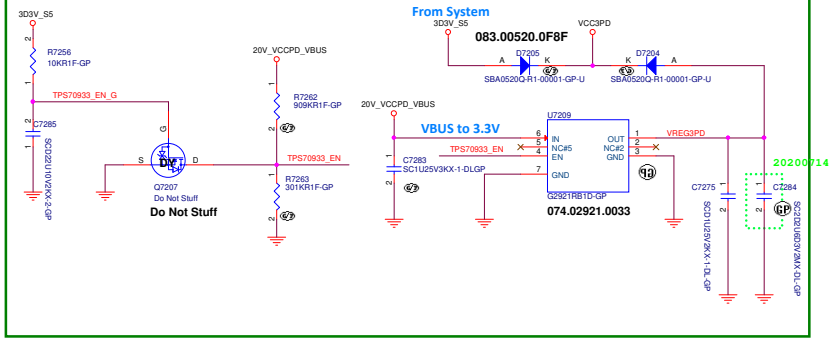






S.No	Project Name	ODM	CCG4_ID_1	Single/ Dual Port	Port 1 Configuration	Port 2 Configuration	Voltage level	Voltage value
1	Bucky/BenSolo AMD	Wistron	L0	Single	USB+DP+Charging	N/A	L0	0V

For Dead Battery modify



CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB PD(CYPD5126)
Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00
Date: Friday, October 23, 2020 | Sheet 72 of 106

Main Func = TYPEC MUX

From CPU

[18] USB3_USB30_TX_P0
[18] USB3_USB30_TX_N0
[18] USB3_USB30_RX_P0
[18] USB3_USB30_RX_N0

[18] USB3_USB30_TX_P1
[18] USB3_USB30_TX_N1
[18] USB3_USB30_RX_P1
[18] USB3_USB30_RX_N1

DisplayPort AUX

[8] DP2_AUXP
[8] DP2_AUXN

MUX I2C

[18,72] CCG4_APU_USBC_SCL
[18,72] CCG4_APU_USBC_SDA

Re-Driver ctrl

Need a GPIO from CCG5

[72] TUSB544_EN#

HPD

[8,72] CPU_DP_HPD

I2C/USB MUX

TypeC CC

[72] USBC1_CC1_CONN
[72] USBC1_CC2_CONN

Type C USB20

[18] TYPEC_USB20_N
[18] TYPEC_USB20_P

3D3V_S5 3D3V_TUSB R7301 0R1R5F-L-GP

U7301 TUSB544IRNJR-GP 071.00544.0003

20V_VCCPD_VBUS 3A

20171214 Change to short pad

20191022 REMOVE CMC POP RESISTOR

20191023

Q7301 2N7002KDW-1-GP 75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C
4th = 075.07002.0A7C

R7333 100KR2J-1-GP
R7332 100KR2J-1-GP

R7355 Do Not Stuff
EVT 0509: Change EL7301 EL7302 PN
EL7301 FILTER-4P-1SG-GP 68.02002.061
R7356 Do Not Stuff

USB1 SKT-USB28-1-GP 062.10009.0681

ED7301 AZ1043-04F-R7G-GP 075.01043.0073
2nd = 075.06810.0A73
3rd = 075.73044.0003
20200714

ED7302 AZ1043-04F-R7G-GP 075.01043.0073
2nd = 075.06810.0A73
3rd = 075.73044.0003
20200714

ED7306 AZ1043-04F-R7G-GP 075.01043.0073
20200805

ED7303 PESD5V0H1BSFYL-GP-U1 083.5V0H1.00AF
2nd = 083.58017.00AF
ED7304 PESD5V0H1BSFYL-GP-U1 083.5V0H1.00AF
2nd = 083.58017.00AF
20200930

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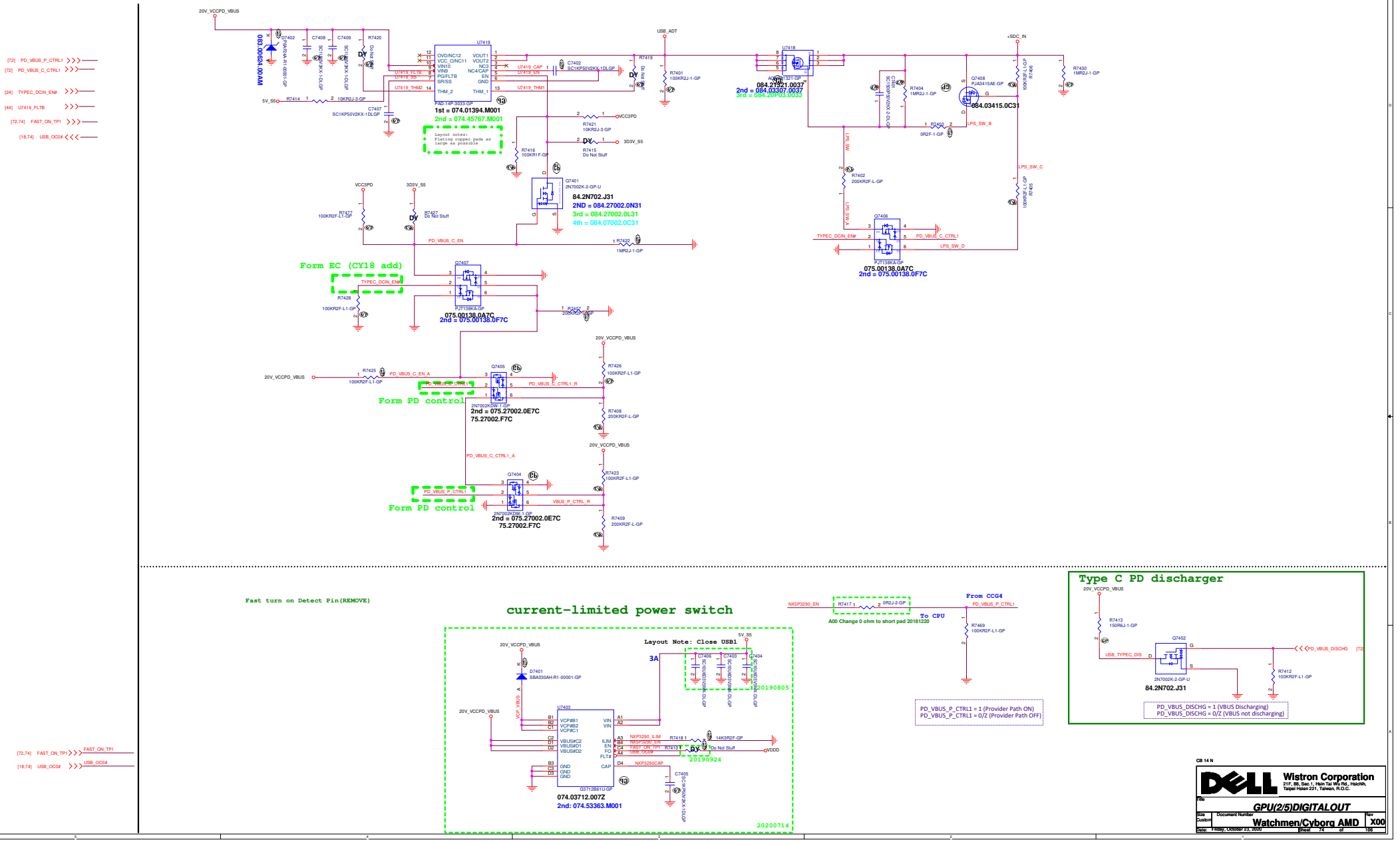
File: USB Type-C&MUX(TUSB546)
Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00
Date: Friday, October 23, 2020 | Sheet 73 of 108



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 75 of 106

Main Func = dGPU

Reserve

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (1/5) PEG

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 76 of 106

Reserve

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (2/5) DIGITALOUT

Size	Document Number	Rev
Custom	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 77 of 106

Reserve

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5) VRAM I/F

Size	Document Number	Rev
Custom	Watchmen/Cyborg AMD	X00

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Reserve

CB 14 N

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU (4/5) GPIO/STRAP		
Size: C	Document Number: Watchmen/Cyborg AMD	Rev: X00
Date: Friday, October 23, 2020	Sheet 79 of 106	

Reserve

CB 14 N

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (5/5) PWR/GND***

Size	Document Number	Rev
A4	**Watchmen/Cyborg AMD**	X00

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Reserve

CB 14 N

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU VRAM1,2 (1/4)*

Size	Document Number	Rev
C	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 81 of 106

Reserve

CB 14 N

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU (BOMACO)	
Size: C	Document Number: Watchmen/Cyborg AMD	Rev: X00
Date: Friday, October 23, 2020	Sheet 82 of 106	

Main Func = dGPU

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CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 83 of 106

Main Func = dGPU

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CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Watchmen/Cyborg AMD | Rev: X00

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OFFPAGE

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5F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

dGPU_VDDC

Watchmen/Cyborg AMD

X00

Friday, October 24, 2014

Reserve

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D875V/VDD1D8V/1D35V

Size: Custom | Document Number: Watchmen/Cyborg AMD | Rev: X00

Date: Friday, October 23, 2020 | Sheet 86 of 106

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CB 14 N

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
GPU DISCHARGE

Size	Document Number	Rev
A4	Watchmen/Cyborg AMD	X00

Date: Friday, October 23, 2020 Sheet 87 of 106

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CB 14 N

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 88 of 106

Main Func = UnusedParts

H1 Do Not Stuff — Do Not Stuff
H2 Do Not Stuff — Do Not Stuff
H3 Do Not Stuff — Do Not Stuff
H4 Do Not Stuff — Do Not Stuff

CPU SKREW HOLE

H8 Do Not Stuff — Do Not Stuff
H10 Do Not Stuff — Do Not Stuff
H12 Do Not Stuff — Do Not Stuff

HS1 STF237R113H91-GP
434.0HH0K.0001
20191209

H13 Do Not Stuff
Do Not Stuff
PCB Footprint = HT12X12B10X10R45
20200820 ME Request

CB 14 CLIP1 SPRING-39-GP-U
34.49U01.001
20201007 ME Request

Main Func = EMI Capacitors

Mind the voltage rating of the caps.

19V_DCBATOUT
EC8917 SC1K50V2KX-1DLGP
EC8919 DY Do Not Stuff
EC8925 DY Do Not Stuff
EC8962 SC1K50V2KX-1DLGP
EC8928 SC1K50V2KX-1DLGP
EC8929 SC1K50V2KX-1DLGP
19V_DCBATOUT
EMI 20181002
EC8957 SC1K50V2KX-1DLGP
EC8963 SC1K50V2KX-1DLGP
EC8954 SC1K50V2KX-1DLGP
EC8958 DY Do Not Stuff

by EMI 20180928
1D2V_S3
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909 EC8910
DY Do Not Stuff; SC1K50V2KX-1DLGP; SC1K50V2KJ-3DLGP
EC8978 EC8979 EC8980 EC8981 EC8911 EC8912 EC8913 EC8914 EC8915
DY Do Not Stuff; SC1K50V2KX-1DLGP
UPDATE 7/25

3D3V_S0
EC8952 EC8950 EC8951 EC8953 EC8975 EC8976 EC8977 EC8985 EC8986 EC8995
SC1K50V2KX-1DLGP; DY Do Not Stuff
UPDATE 7/25
20200813

0.1u->1KP by EMI 20180928
5V_S5
EC8949 EC8947 EC8948
SC1K50V2KX-1DLGP; DY Do Not Stuff
EMI 20181002
EC8959 EC8960 EC8969 EC8970 EC8971 EC8987
SC1K50V2KX-1DLGP; SCD1U16V2KX-3DLGP; DY Do Not Stuff

3D3V_S5
EC8961 EC8964 EC8965 EC8966
DY Do Not Stuff; SCD1U16V2KX-3DLGP
20200813

3D3V_S5
EC8962 EC8963 EC8984 EC8955 EC8956
SCD1U16V2KX-3DLGP; DY Do Not Stuff
20200813

1D8V_S5
EC8988 EC8989 EC8990 EC8991 EC8992 EC8993 EC8994
SCD1U16V2KX-3DLGP; DY Do Not Stuff
20200813

Main Func = RF Capacitors

Mind the voltage rating of the caps.

0.1uF:FC8903 FC8904
4.7pF:FC8905 FC8941 FC8942
10 pF:FC8943 FC8944
1uF:FC8901 FC8902

3D3V_S5
FC8901 SCD1U10V2KX-1DLGP
FC8902 SCD1U16V2KX-1DLGP
FC8903 SCD1U16V2KX-3DLGP
FC8904 SCD1U16V2KX-3DLGP
FC8905 SCD1U16V2KX-3DLGP
FC8941 SCD1U16V2KX-3DLGP
FC8942 SCD1U16V2KX-3DLGP
FC8943 SC10P50V2JN-4DLGP
FC8944 SC10P50V2JN-4DLGP

20181012 1uF:FC8906 FC8907
4.7pF:FC8910 FC8937 FC8938
0.1uF:FC8908 FC8909
10 pF:FC8939 FC8940

5V_S5
FC8906 SCD1U10V2KX-1DLGP
FC8907 SCD1U10V2KX-1DLGP
FC8908 SCD1U16V2KX-3DLGP
FC8909 SCD1U16V2KX-3DLGP
FC8910 SC4D7P50V2BN-2GP
FC8937 SC4D7P50V2BN-2GP
FC8938 SC4D7P50V2BN-2GP
FC8939 SC10P50V2JN-4DLGP
FC8940 SC10P50V2JN-4DLGP
20201012

19V_DCBATOUT
FC8916 SC1U25V3KX-1DLGP
FC8917 SC1U25V3KX-1DLGP
FC8918 SC1U25V2KX-1DLGP
FC8919 SC1U25V2KX-1DLGP
FC8920 SC1U25V2KX-1DLGP
FC8921 SC1U25V2KX-1DLGP
FC8922 SC4D7P50V2BN-2GP
FC8923 SC4D7P50V2BN-2GP
FC8924 SC4D7P50V2BN-2GP
FC8925 SC4D7P50V2BN-2GP
FC8926 SC10P50V2JN-4DLGP
FC8927 SC1U25V3KX-1DLGP
FC8928 SC6P50V2CN-1NLGP
FC8929 SC6P50V2CN-1NLGP
FC8930 SC1U25V2KX-1DLGP
FC8931 SC10P50V2JN-4DLGP
FC8932 SC10P50V2JN-4DLGP
FC8933 SC10P50V2JN-4DLGP
FC8934 SC12P50V2JN-4DLGP
FC8935 SC12P50V2JN-4DLGP
FC8936 SC12P50V2JN-4DLGP
20201012

1uF:FC8916 FC8917 FC8918 FC8927
0.1uF:FC8919 FC8920 FC8921 FC8930
4.7pF:FC8922 FC8923 FC8924 FC8925
6pF:FC8928 FC8929

12pF:FC8934 FC8935 FC8936
10pF: FC8926 FC8931 FC8932 FC8933

CB 14 N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: Watchmen/Cyborg AMD | Rev: X00
Date: Friday, October 23, 2020 | Sheet 89 of 106

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CB 14 N

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Watchmen/Cyborg AMD*	*X00*

Date: Friday, October 23, 2020 Sheet 90 of 106

Main Func = TPM

[16,24,68] LPC_RST#
[17,24,61,63] PLT_RST#

[24,25] SPI_CLK_ROM_R
[16,24,25] SPI_SI_ROM
[16,24,25] SPI_SO_ROM
[16] SPI_CS_ROM_N2

[17] PIRQA#

1D8V_S5 — R9149 TPM 2 Do Not Stuff — 1D8V_S0 — R9150 1 DY 2 Do Not Stuff — 1D8V_TPM
20200914

1D8V_TPM — C9109 Do Not Stuff TPM — C9112 Do Not Stuff TPM — C9113 Do Not Stuff TPM

1D8V_TPM — R9151 Do Not Stuff TPM — Q9101 Do Not Stuff TPM — R9155 Do Not Stuff TPM — 3D3V_S5
SPI_IRQ#_TPM2 — S D — PIRQA#
Do Not Stuff
20200915
R9157 1 DY 2 Do Not Stuff

1D8V_TPM — R9148 Do Not Stuff DY — SPI_CS2#_IC
1D8V_S5 — R9158 Do Not Stuff TPM — SPI_CS2#_IC

1D8V_TPM — 5mA — C9104 Do Not Stuff TPM

1D8V_S5 — 40mA — C9106 Do Not Stuff TPM — C9108 Do Not Stuff TPM

20200909: Change U9101 PN

U9101 TPM

8	VHIO	SDA/GPIO0	29
22	VHIO	SCL/GPIO1	30
1	VSB	PIRQ#/GPIO2	18
		GPIO3	6
		GPIO4	13
		PP/GPIO6	4
	MOSI/GPIO7	NC#7	7
	MISO	NC#9	9
20	SCS#/GPIO5	NC#10	10
19	SCLK	NC#11	11
17	PLTRST#	NC#12	12
		NC#14	14
16	GND	NC#15	15
23	GND	NC#25	25
33	GND	NC#26	26
		NC#27	27
		NC#28	28
2	NC#2	NC#31	31
3	NC#3	NC#32	32
5	NC#5		

Do Not Stuff
Do Not Stuff

TP9101 — TPM_GPIO0
TPM_GPIO1 — TP9102
SPI_IRQ#_TPM2
TPM_GPIO3 — TP9103
TPM_GPIO4 — R9118 1 DY 2 Do Not Stuff — SPI_CS_ROM_N2
TPM_GPIO6_PP — TP9104

SPI_SI_ROM — R9133 1 TPM 2 Do Not Stuff — SPI_SI_ROM_TPM
SPI_SO_ROM — R9132 1 TPM 2 Do Not Stuff — SPI_SO_ROM_TPM
SPI_CS_ROM_N2 — R9130 1 TPM 2 Do Not Stuff — SPI_CS2#_IC
SPI_CLK_ROM_R — R9138 1 TPM 2 Do Not Stuff — SPI_CLK_ROM_TPM

K TPM A — D9101 Do Not Stuff — TPM_PLT_RST#

PLT_RST# — R9101 1 DY 2 Do Not Stuff — PLT_RST#_TPM
R9159 1 DY 2 Do Not Stuff

LPC_RST# — R9102 1 TPM 2 Do Not Stuff

U9101_2_GND — R9152 Do Not Stuff DY

1D8V_TPM — R9156 1 TPM 2 Do Not Stuff — TPM_PLT_RST#

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Title: INT IO (TPM)		
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Size: A3 | Document Number: *Watchmen/Cyborg AMD* | Rev: *X00*

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Title	*LVDS_Switch*	
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Title	*CRT_Switch*	
Size: A3	Document Number: Watchmen/Cyborg AMD	Rev: X00
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Main Func = Debug

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Title: CPU_XDP;PCH_XDP

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Title: CLK Block Diagram

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Change notes -

Phase	Date	Sch Page	Location	Reason of change	Owner
DVT1	2018/9/13	24	Add D2409 ,R2489 to KBC_GPI005 for Mods about Lan function.	Follow AMD's suggestion	EE
DVT1	2018/9/18	16	R1623/R1624 0R 0402->0201	Add layout spacing	EE
DVT1	2018/9/20	40	ADD R4014	For break down easily	EE
DVT1	2018/9/20	30	R4637 change to 340 ohm,PR4601 change to 187 ohm, and PR4601 change to 187 ohm	Follow AMD's stardust test result	PWR
DVT1	2018/9/21	46	PR4625 change 9.53K/0402 for VR HOT	For VR HOT	PWR
DVT1	2018/9/21	16	R1609 change 33ohm and EC1615 change 33P	Reduce noise	EMC
DVT1	2018/9/27	24	R2428	20K for PCB_VERSION_DVT1	EE
DVT2	2019/11/13	44,48	TC4801 PT4402	DY by acoustic test	EE
DVT2	2019/11/15	24	R2428	33K for PCB_VERSION_DVT2	EE
DVT2	2019/11/16	74	C7493 DY,C7491 C7492 10U change to 22U	Follow Factory suggestion	EE
A00	2018/12/3	8	R806,R807,R809	short PAD for MP	EE
A00	2018/12/3	9	R901,R902,R903,R904	short PAD for MP	EE
A00	2018/12/5	11	R1102,R1103,R1104,R1105,R1106	short PAD for MP	EE
A00	2018/12/5	16	R1613,R1614,R1621,R1622,R1607,R1616	short PAD for MP	EE
A00	2018/12/7	17	R1772,R1722,R1723,R1773,R1712,R1706	short PAD for MP	EE
A00	2018/12/21	18	R1807	short PAD for MP	EE
A00	2018/12/21	24	R2411,R2416,R2419,R2420,R2413,R2445,R2468,R2422,R2457,R2456,R2421,R2426,R2427,R2437,R2443	short PAD for MP	EE
A00	2018/12/21	24	R2428	47K for PCB_VERSION_A00	EE
A00	2018/12/21	25	R2508	short PAD for MP	EE
A00	2018/12/21	26	R2618,R2619,R2615,R2605,R2613,R2614,R2612	short PAD for MP	EE
A00	2018/12/24	27	R2741,R2734,R2721,R2718,R2712,R2720,R2704,R2705,R2706,R2708	short PAD for MP	EE
A00	2018/12/24	29	R2901,R2902,R2903,R2904,R2906,R2907,R2909,R2911,R2923,R2914	short PAD for MP	EE
A00	2018/12/24	34	R3432	short PAD for MP	EE
A00	2018/12/24	35	R3501,R3502,R3503,R3504,R3512,R3524,R3533,R3521,R3522	short PAD for MP	EE
A00	2018/12/24	38	R3805,R3806,R3821,R3822,R3803	short PAD for MP	EE
A00	2018/12/25	40	R4001,R4013,R4012,R4008,R4007,R4005	short PAD for MP	EE
A00	2018/12/25	40	R4014	remove R4014,short	EE
A00	2018/12/25	43	EL4301,EL4302,EL4303,EL4304,R4380	short PAD for MP	EE
A00	2018/12/25	55	R5514,R5523,R5508,R5531,R5502,R5537,R5538	short PAD for MP	EE
A00	2018/12/25	57	R5712,R5715	short PAD for MP	EE
A00	2018/12/25	60	R6001,R6016	short PAD for MP	EE
A00	2018/12/25	61	R6143,R6110,R6111	short PAD for MP	EE
A00	2018/12/25	63	R6328,R6327	short PAD for MP	EE
A00	2018/12/25	63	R6321,R6331	改成兩個 0805 Short PAD	EE
A00	2018/12/25	64	R6404,R6405	short PAD for MP	EE

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Title: Change History

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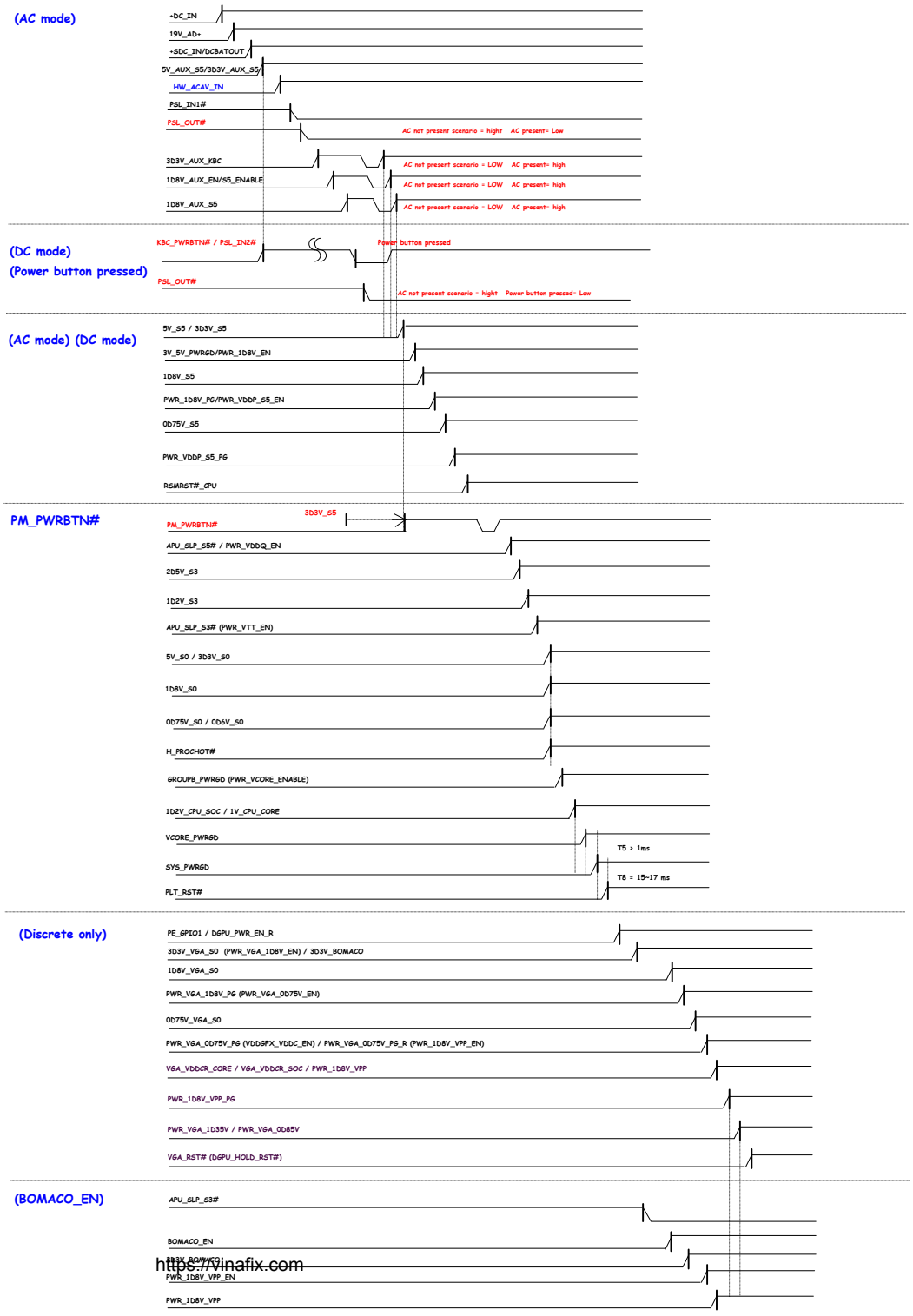
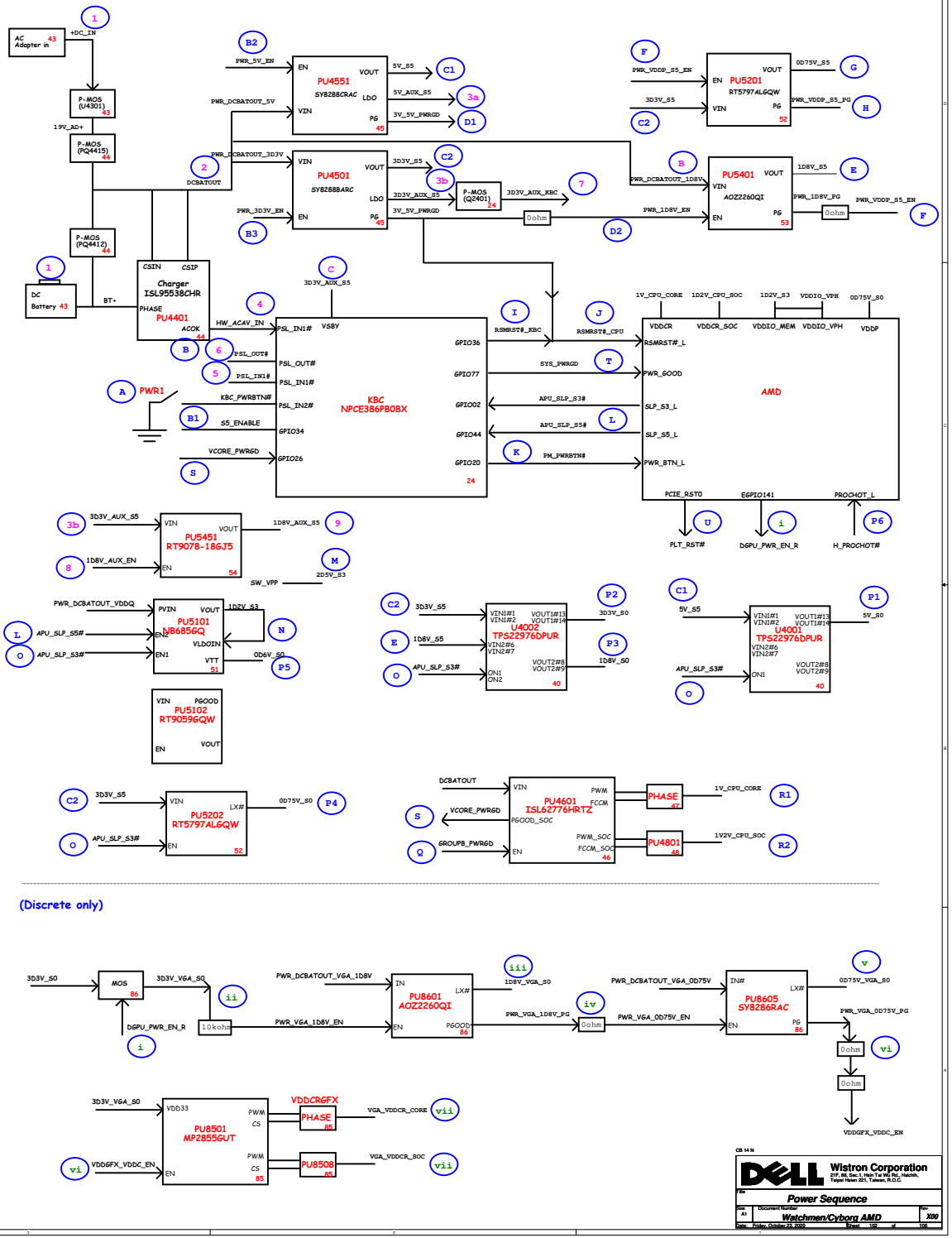
Power Up Sequence





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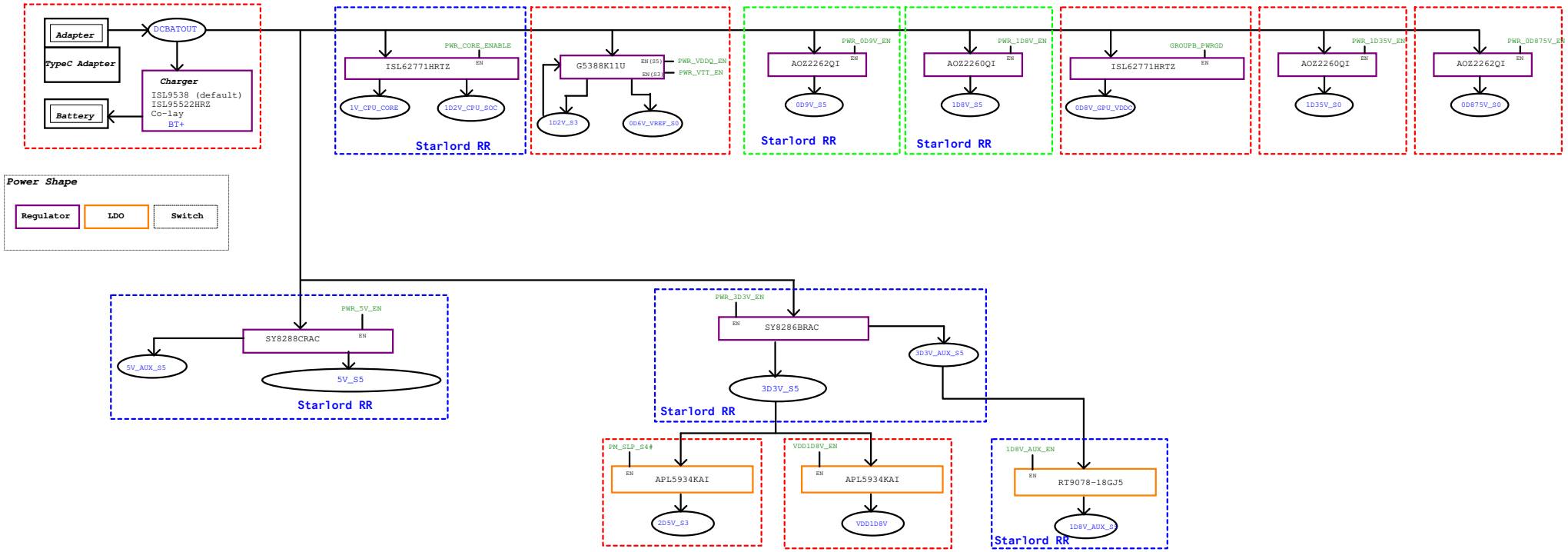
Power Sequence

Watchmen/Cyborg AMD

X00

Date: Friday, October 23, 2020



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Title: **Power Block Diagram**

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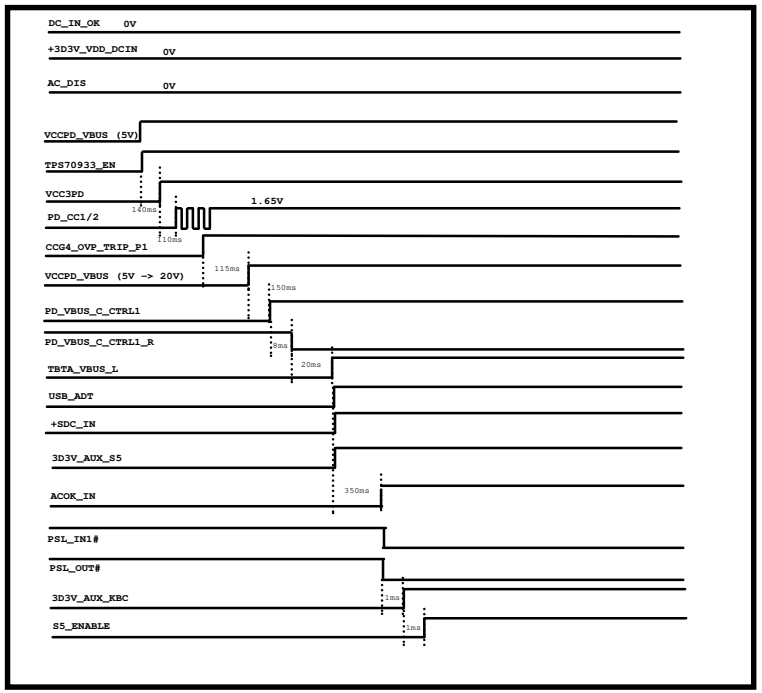
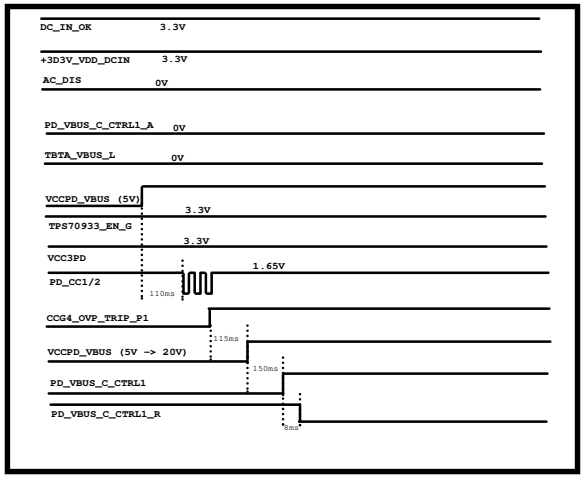
Type-C Adapter sequence

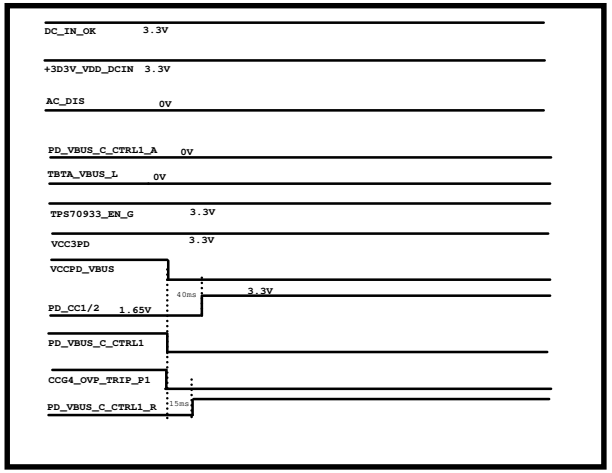
Type-C ADP IN without Barrel ADP (DC mode)



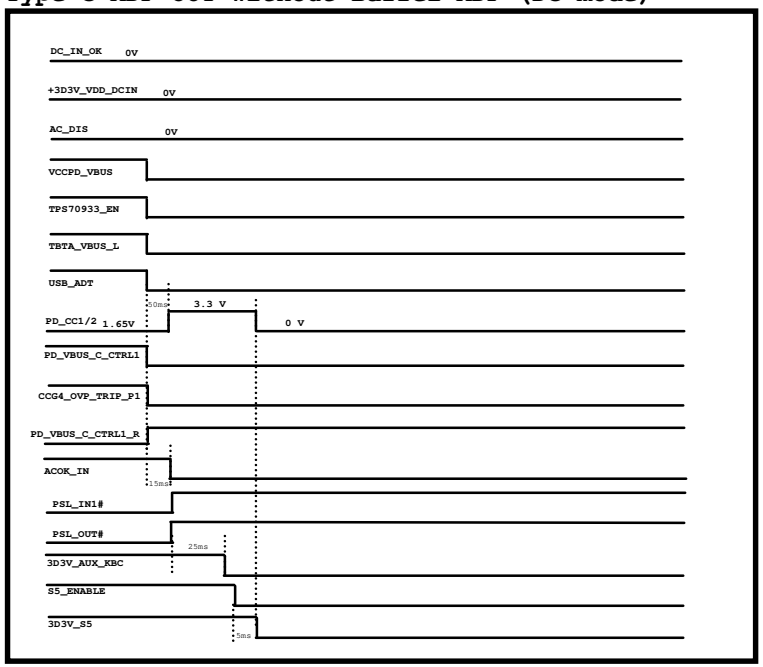
Type-C ADP IN after Barrel ADP in



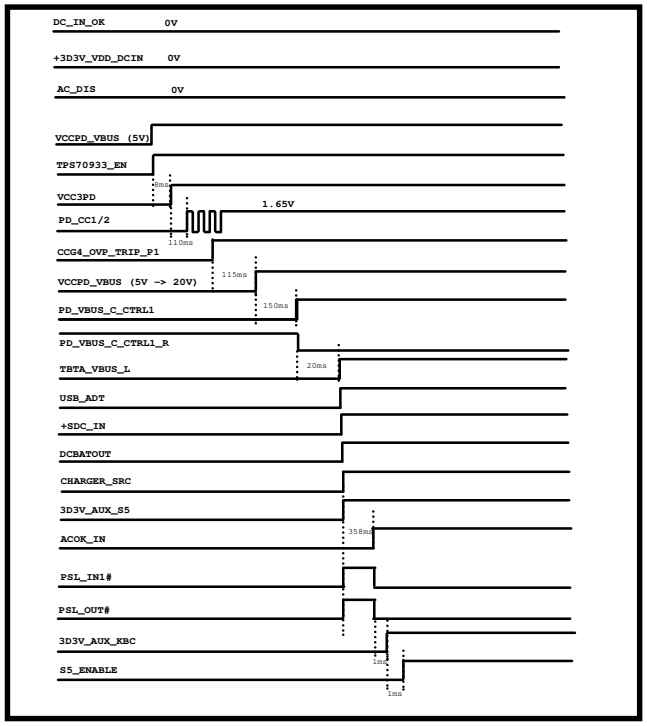
Type-C ADP OUT after Barrel ADP in



Type-C ADP OUT without Barrel ADP (DC mode)



Type-C ADP IN without battery (Dead Battery)



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Title: SMBUS Block Diagram

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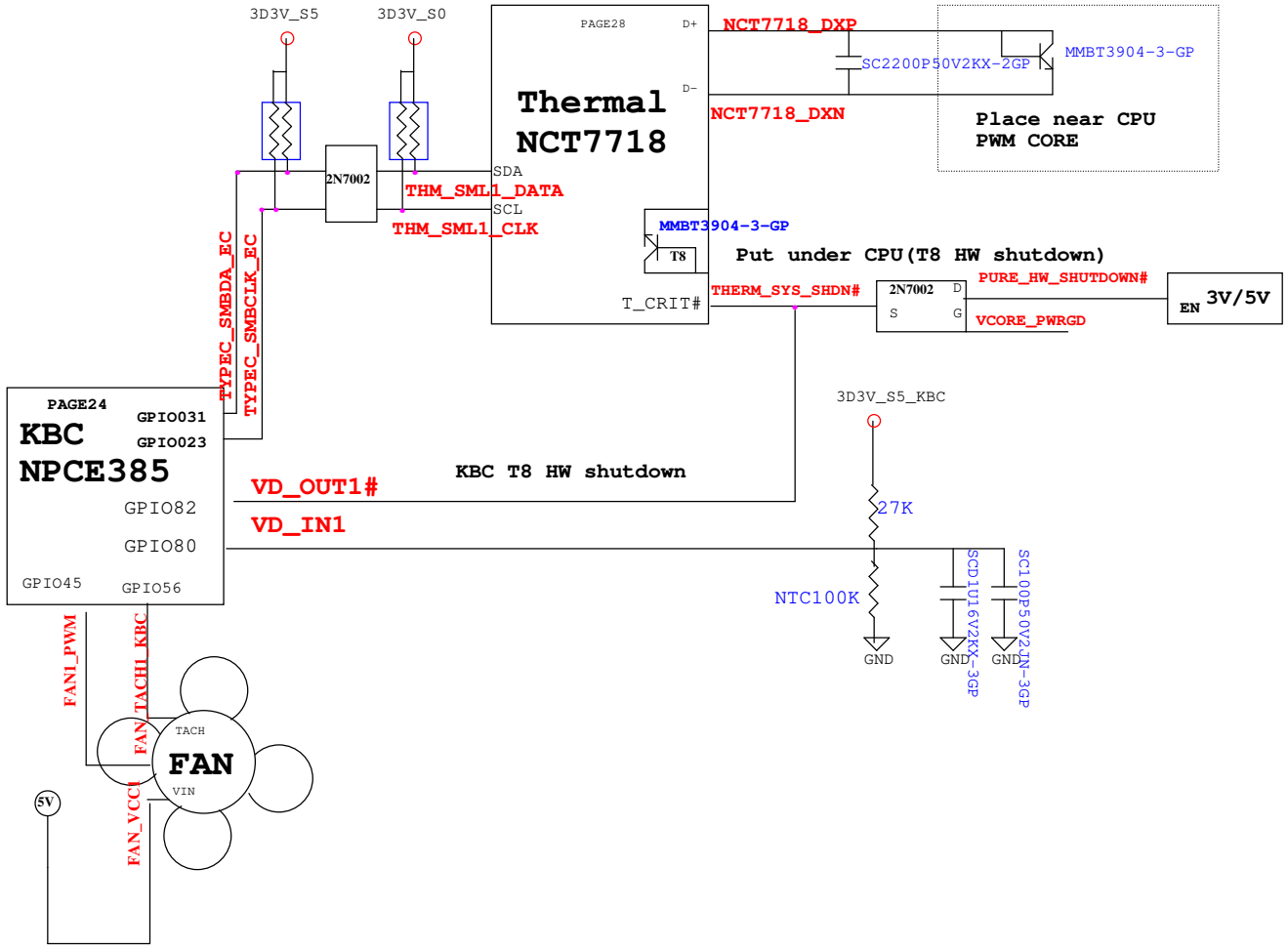
Thermal Block Diagram



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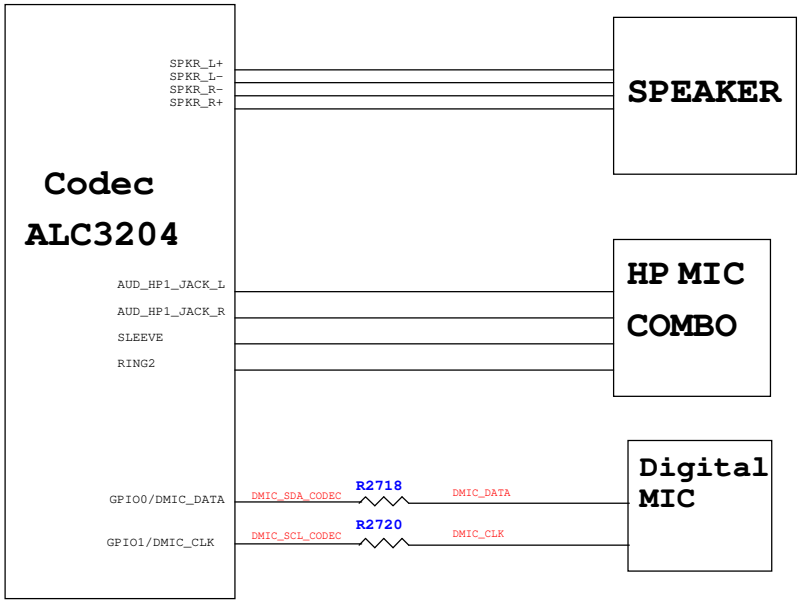
Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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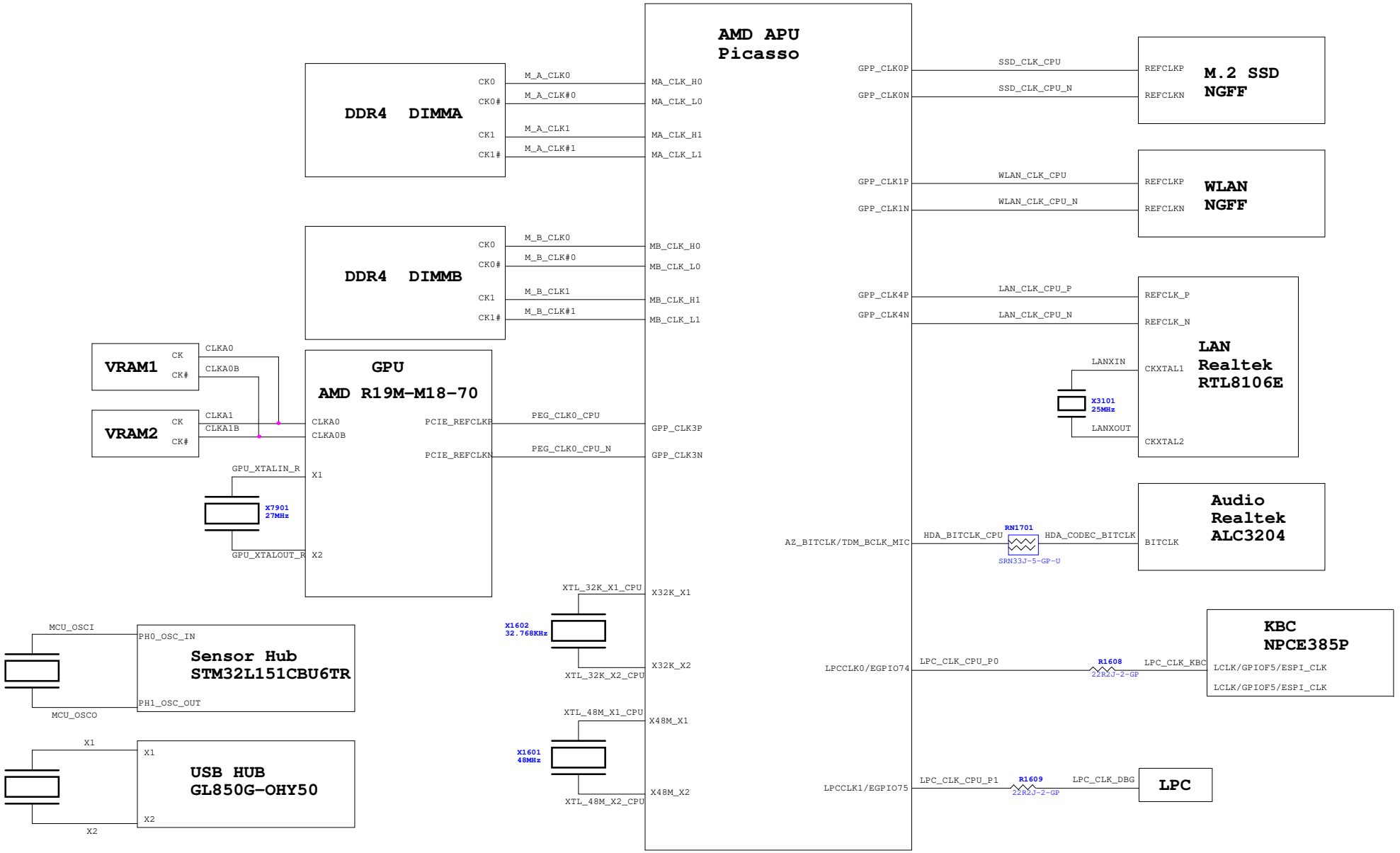
CLK Block Diagram



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Title: CLK Block Diagram

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