LCFC Confidential

Y550 M/B Schematics Document

Comet Lake H-Processor with DDR4 + NV N18P-G61/G62 GPU

2019-12-16

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Cover Page		
Size: Custom	Document Number: Y550		Rev: 1.0
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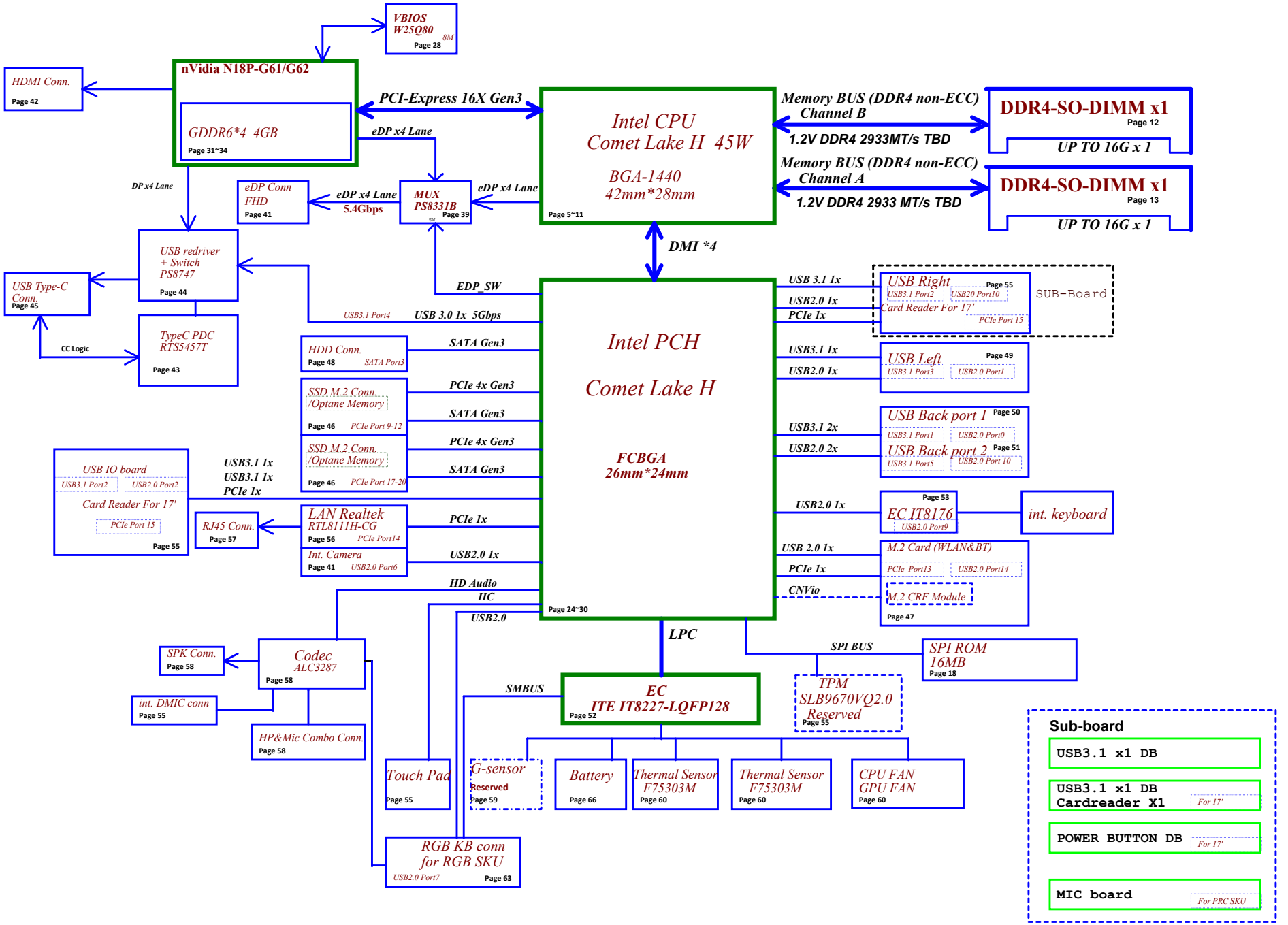

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Block Diagram**

Size	Document Number	Rev
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Date: Tuesday, January 14, 2020 Sheet 2 of 83

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
i5@i7@i9@	CPU Part
PRC@	PRC
WW@	Worldwide
OPT@	NV GPU part
M4GX4@S4GX4@	VRAM part
N18PG61@	N18PG61 PART
N18PG62@	N18PG62 PART
GYSNC@	GSYNC support part
DDS@	Dynamic Display Switch part
MUX@	EDP MUX Switch part
MUX1@	Colay DDS and MUX
HDMI@	HDMI logo
CNVI@	CNVi support part
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
EMC_8111H@	LAN 8111H EMC Part
AG@	Anti-ghost Part
BL@	BL Part
RGB@	RGB Part
MP@	Mass Production Stage Part

BOM Structure	BTO Item
USB@	USB2.0 port1 for USB Port
NPI@	NPI stage stuff
DCI@	DCI
Debug@	USB2.0 port 1for Debug
TPM@	For support TPM sku part
GS@	Reserved for G-sensor
OPTANE@	For Optane SKU stuff
MIRROR@	MIRROR
NOMIRROR@	No MIRROR
ME@	ME part(connector)
EMC@	EMC part
EMC_NS@	EMC not stuff
RF@	RF part
RF-NS@	RF No part
CD@	Cost down part
UP9632_@	UP9632 part stuff

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7	RGB
8	NA
9	AG
10	Back USB3.0
11:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Right USB3.0(DB)
3	Left USB3.0
4	Type-C Port
5	Back USB3.0
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	NA
1B	NA
2	NA
3	HDD Gen3
4	NA
5	NA
7	NA

PCIE Port table	
Port	Function
1:8	NA
9:12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15	Card Reader
17:20	M.2 SSD/Optane

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Title: **Notes List**

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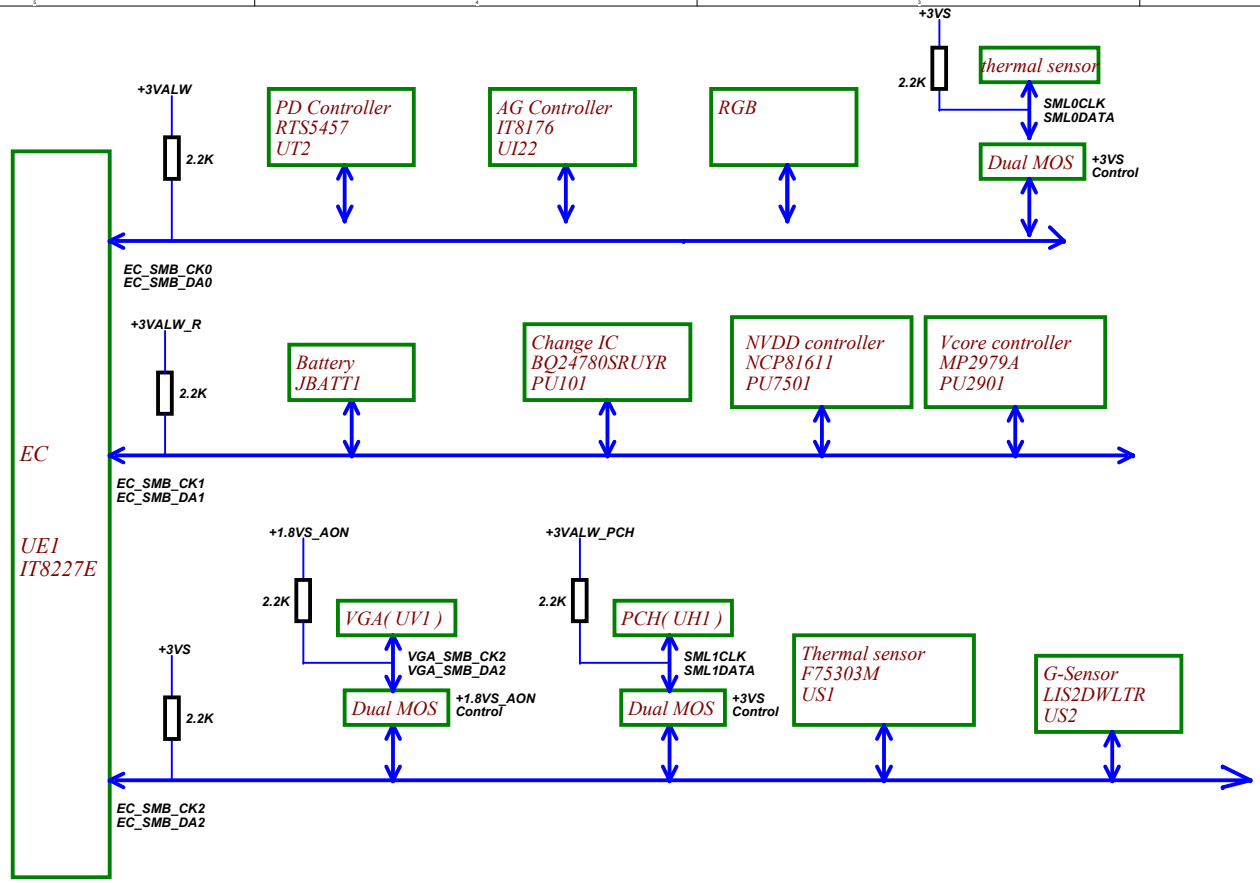


SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio	Anti-ghost
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

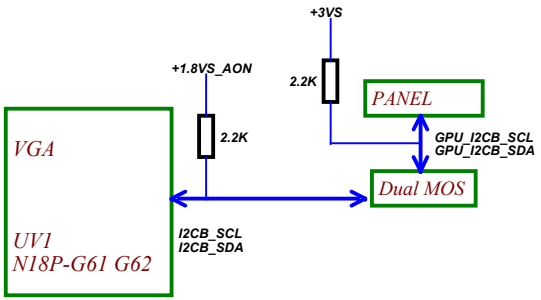
Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update
Thermal Sensor NCT7718M	1001100xb

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update



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Title	I2C Block		
Size	D	Document Number	¥550
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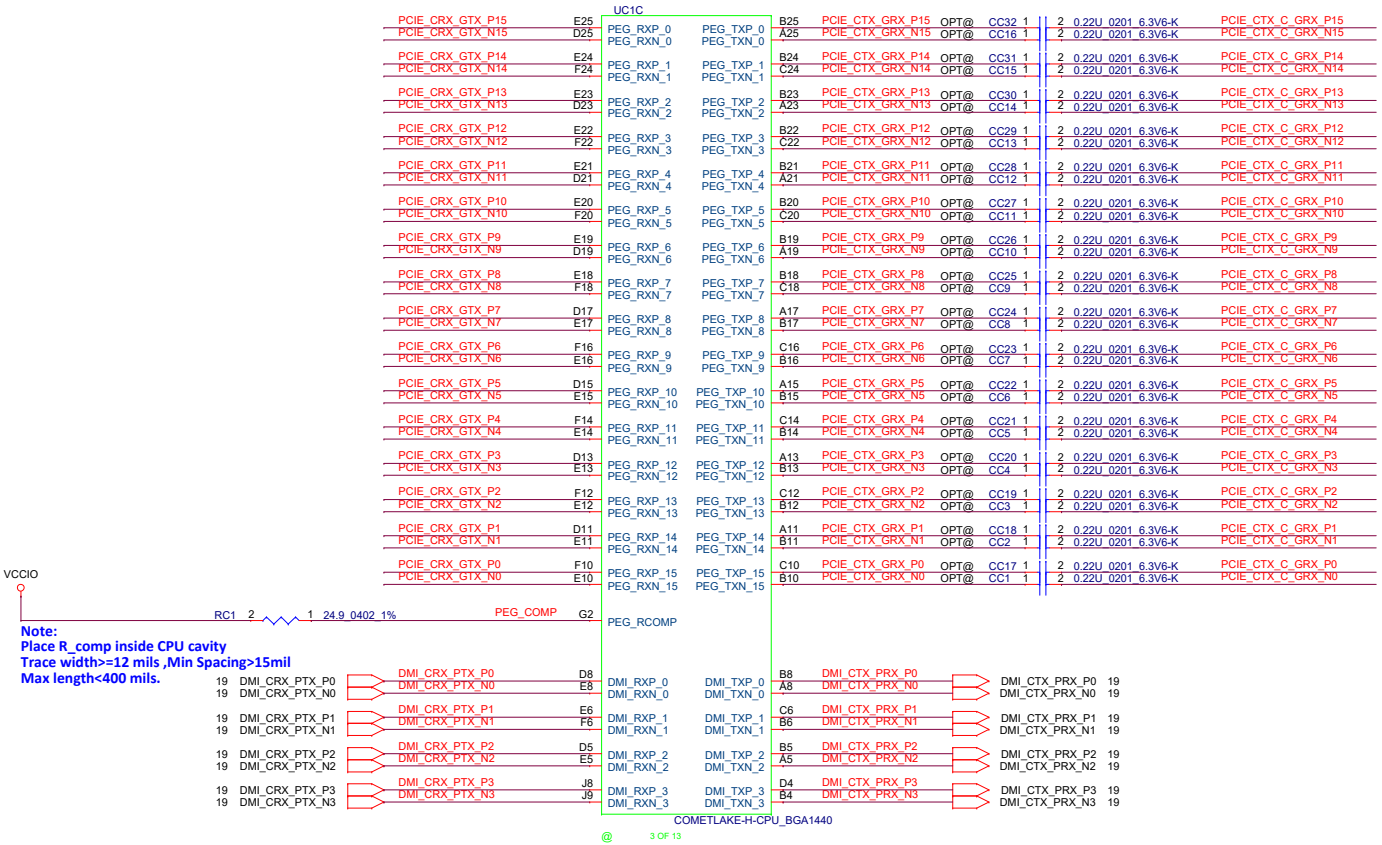
25 PCIE_CRX_GTX_N[0..15]

25 PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] 25

PCIE_CTX_C_GRX_P[0..15] 25



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (1/7) DMI,PEG

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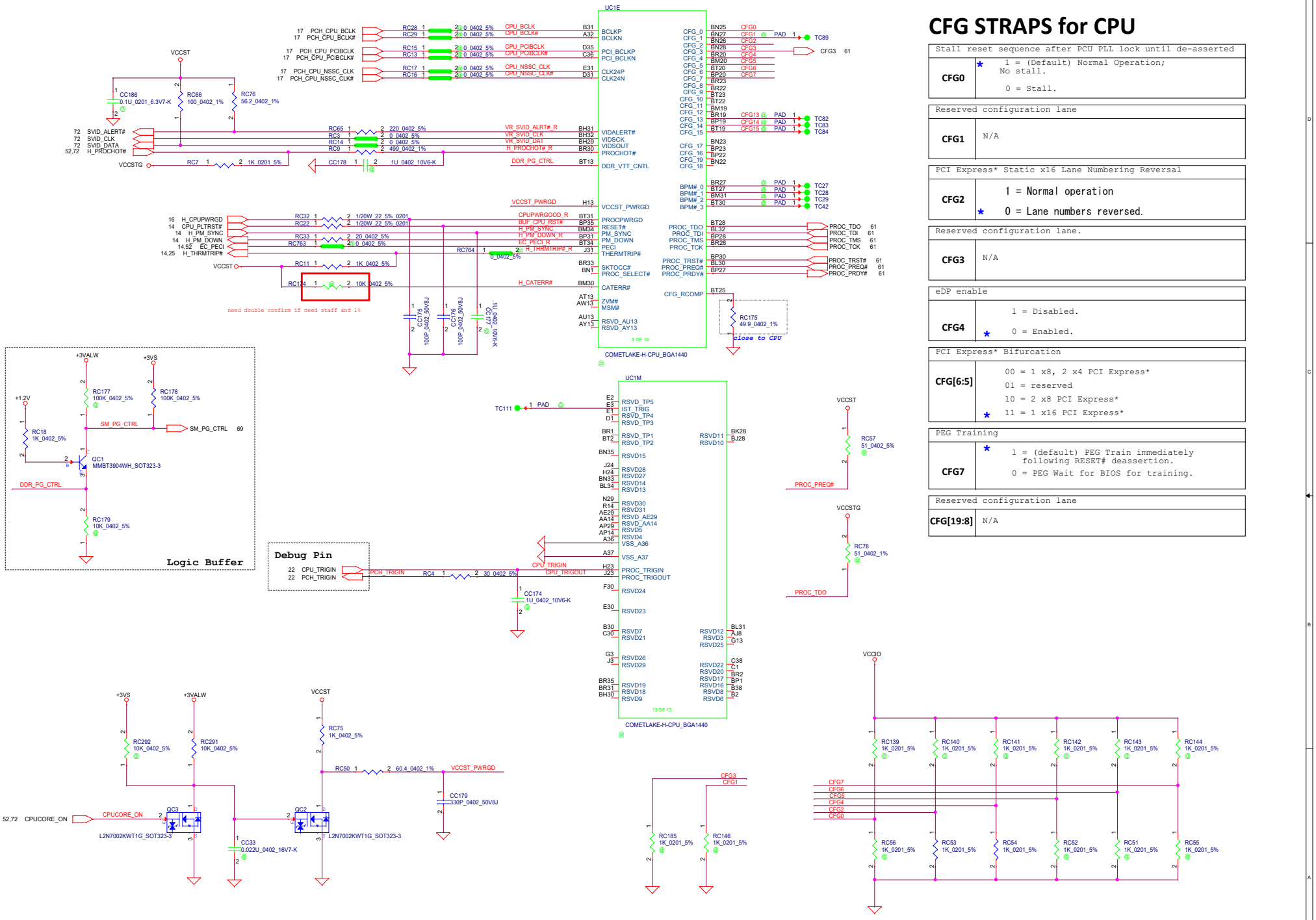

CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.
Reserved configuration lane	
CFG1	N/A
PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed.
Reserved configuration lane.	
CFG3	N/A
eDP enable	
CFG4	1 = Disabled. * 0 = Enabled.
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* * 11 = 1 x16 PCI Express*
PEG Training	
CFG7	* 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.
Reserved configuration lane	
CFG[19:8]	N/A

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (2/7) PM, XDP, CLK, CFG

Size	Document Number	Rev
Custom	Y550	1.0

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	Y550	1.0

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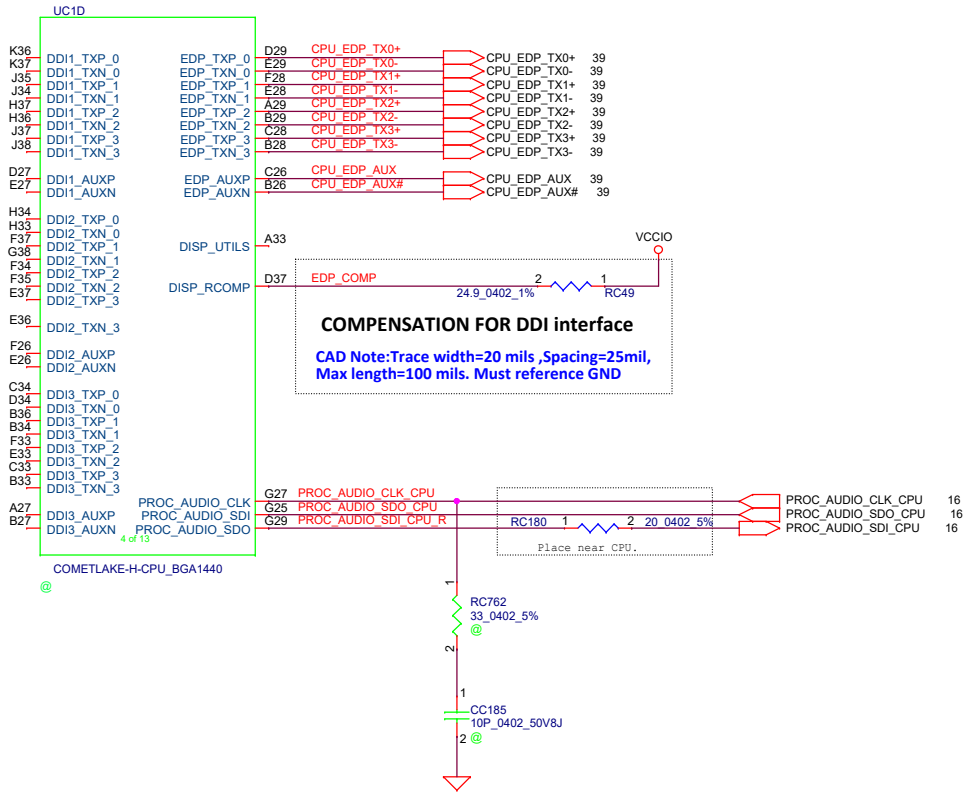

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
A3	¥550	1.0

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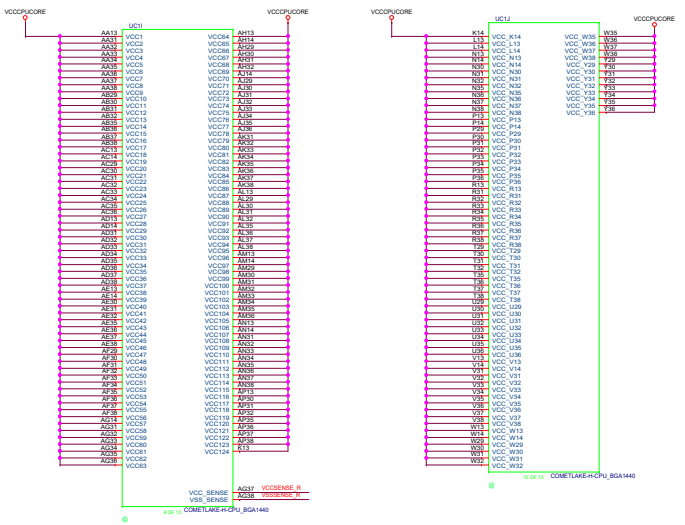
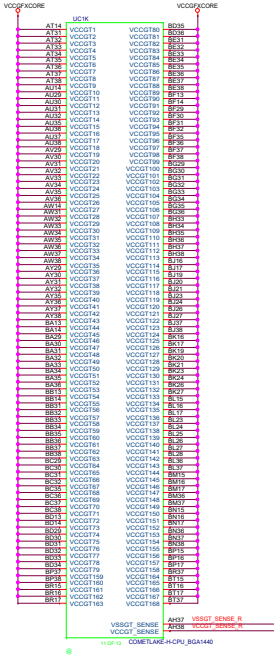
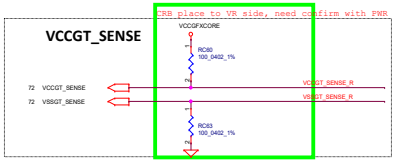
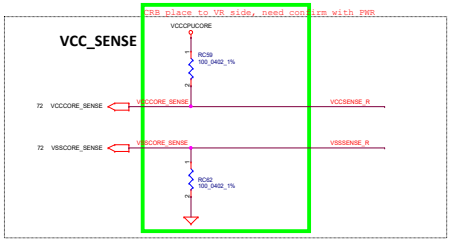
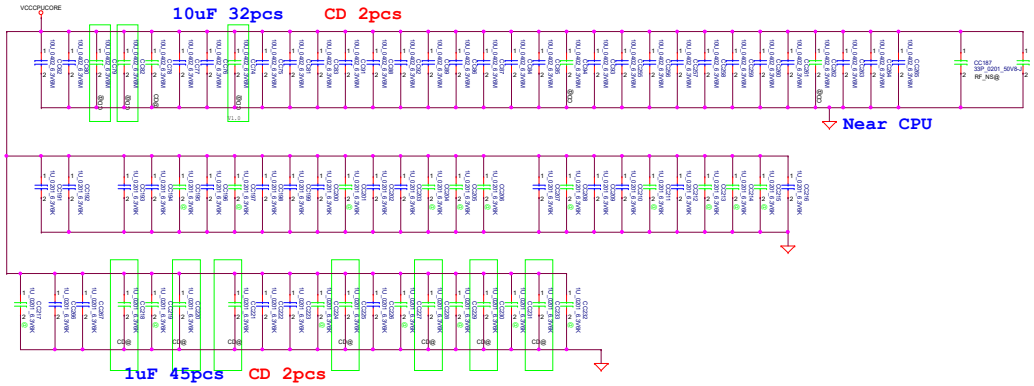




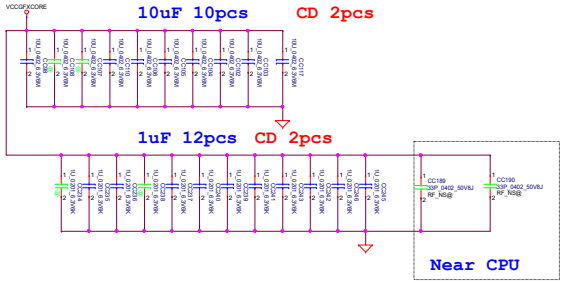




PDG near: 470uf*4 47uf*20
backside:10uf*32 1uf*45



PDG near: 470uf*4 47uf*20
backside:10uf*32 1uf*45



Security Classification	LC Future Center Secret Data		Title: CPU (5/7) PWR, BYPASS
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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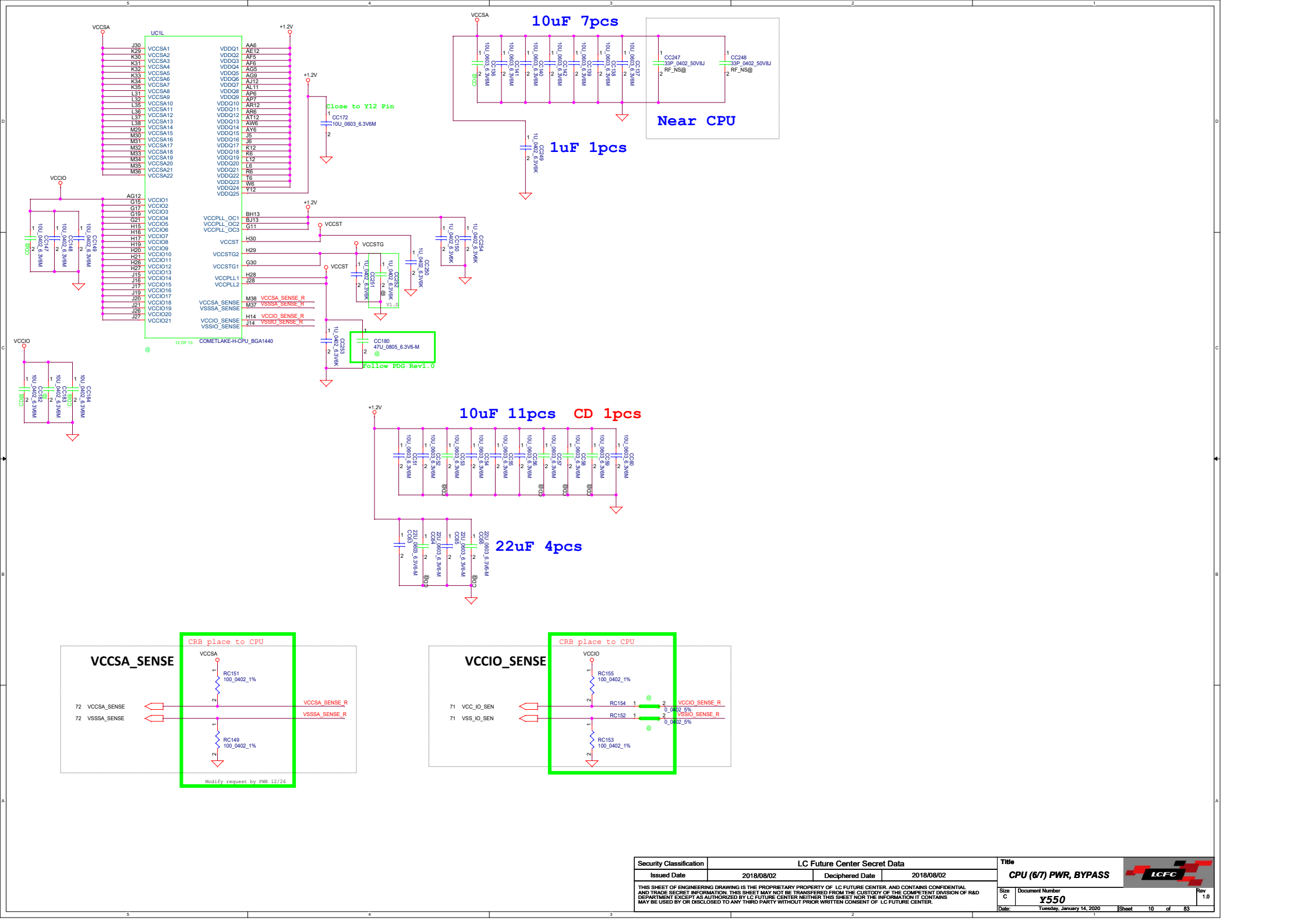

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (6/7) PWR, BYPASS

Size	Document Number	Rev
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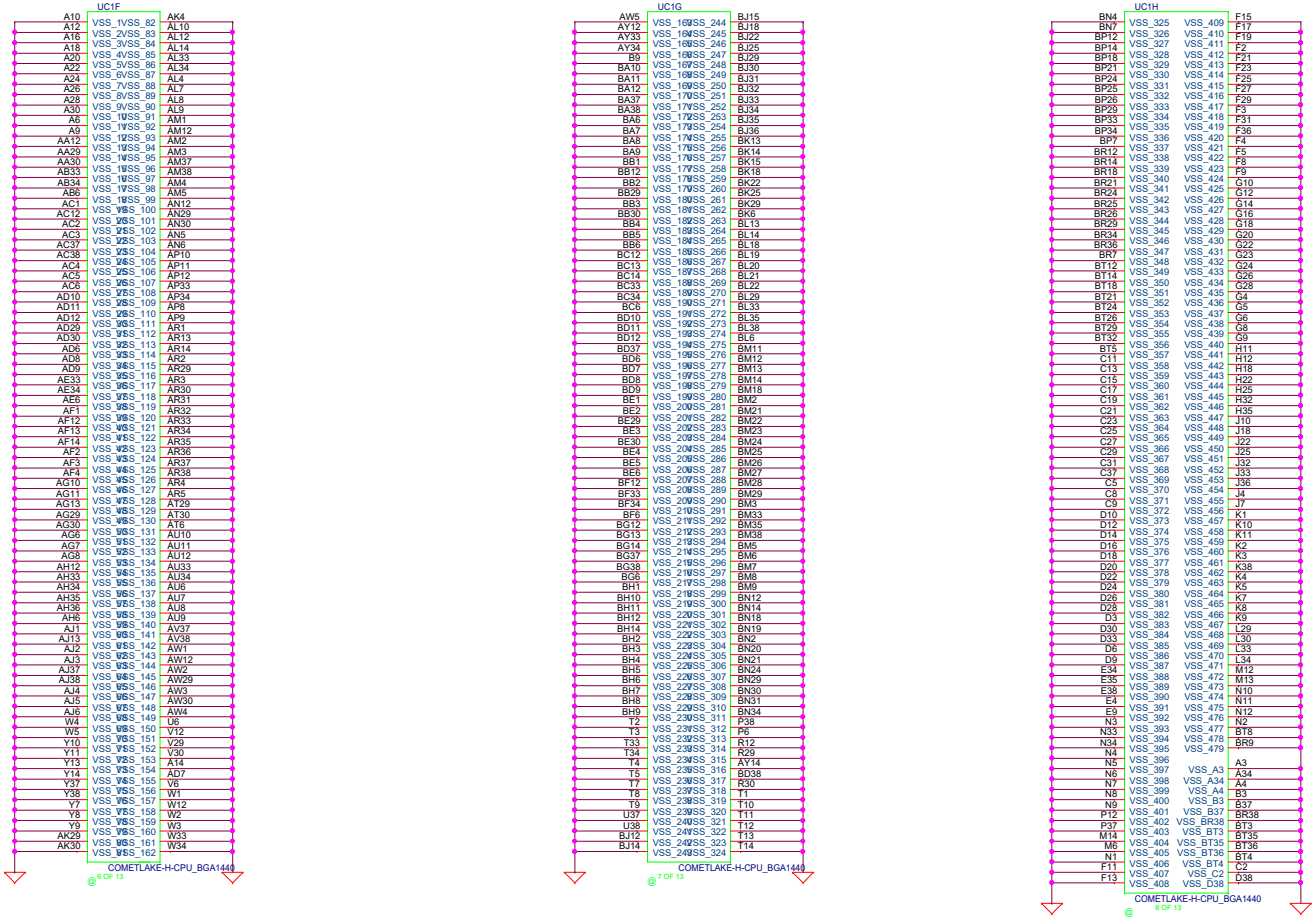

Title: **CPU (6/7) PWR, VSS**

Size	Document Number	Rev
C	Y550	1.0

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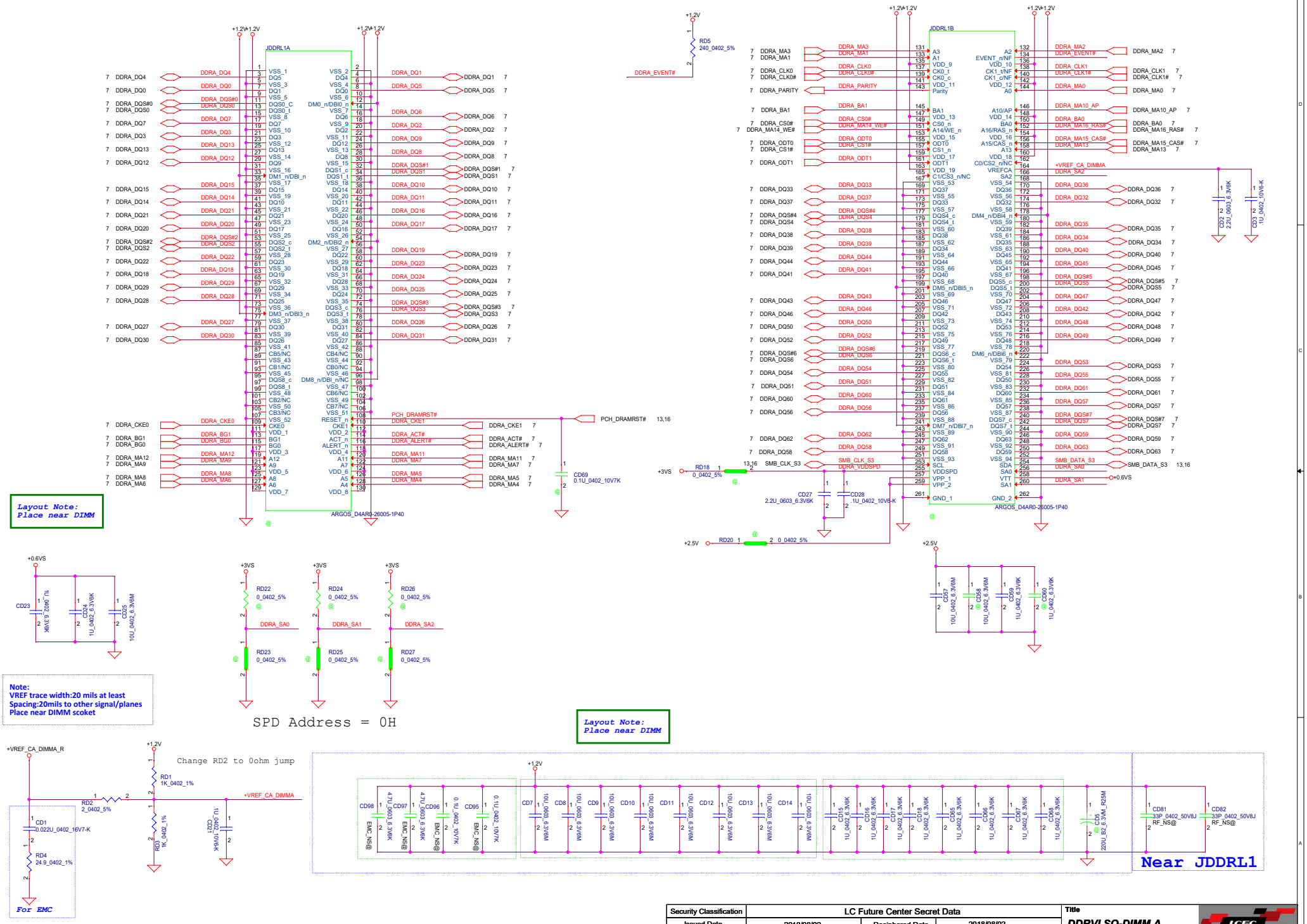
DDR4 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDRVI SO-DIMM A		
Size	Document Number		Rev
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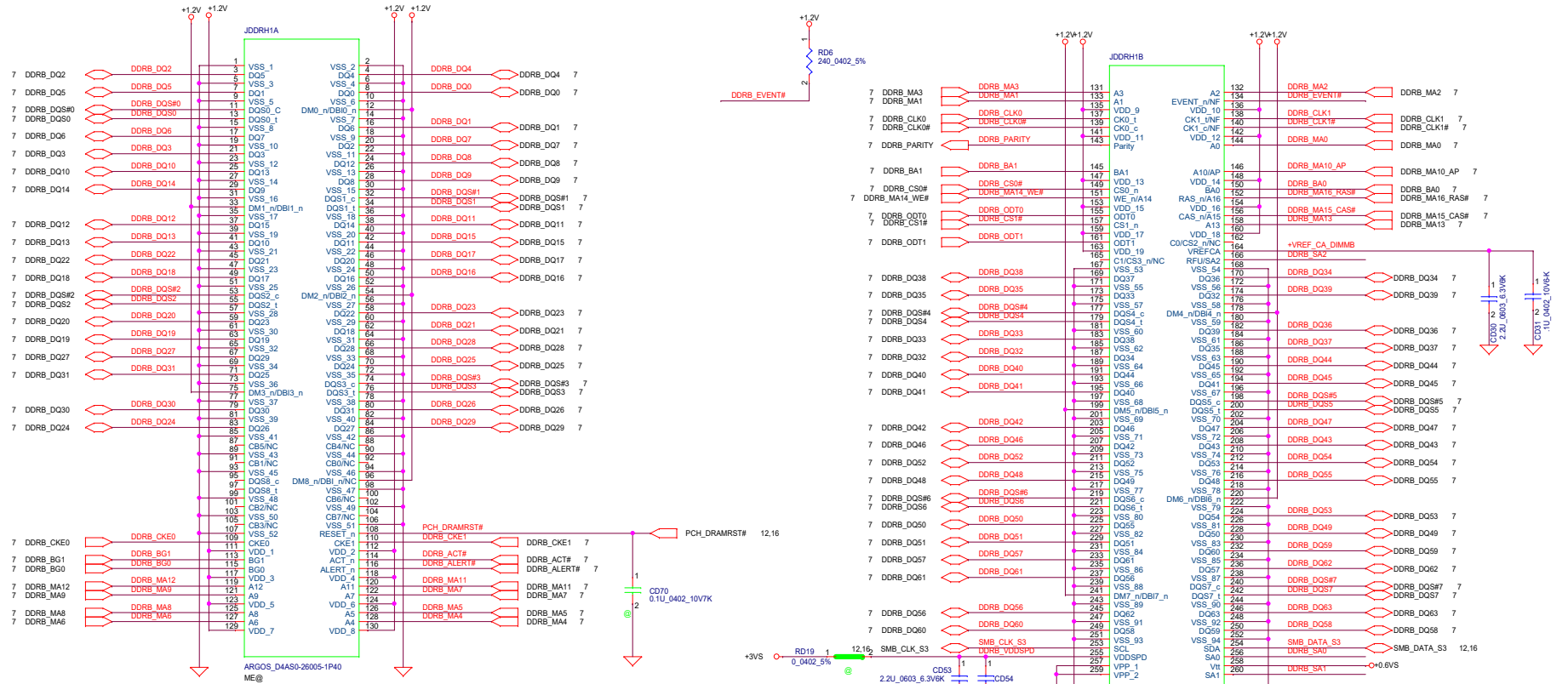
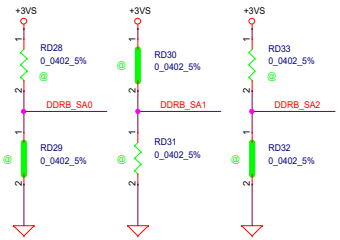
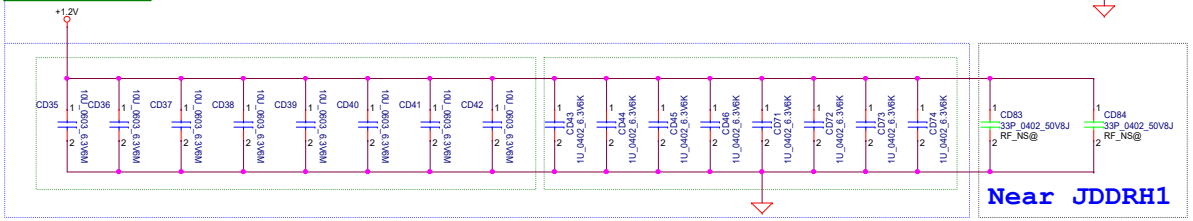
DDR4 SO-DIMM B

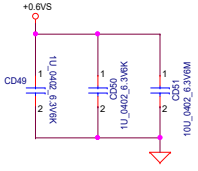


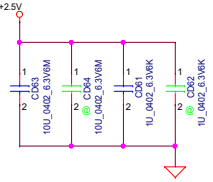


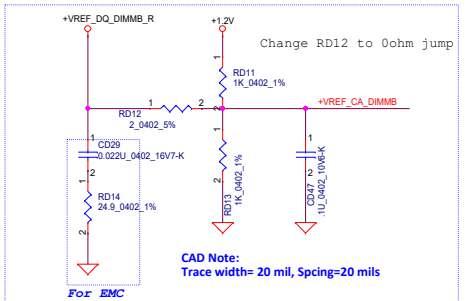
SPD Address = 2H

Layout Note:
Place near DIMM









Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDRVI SO-DIMM B		
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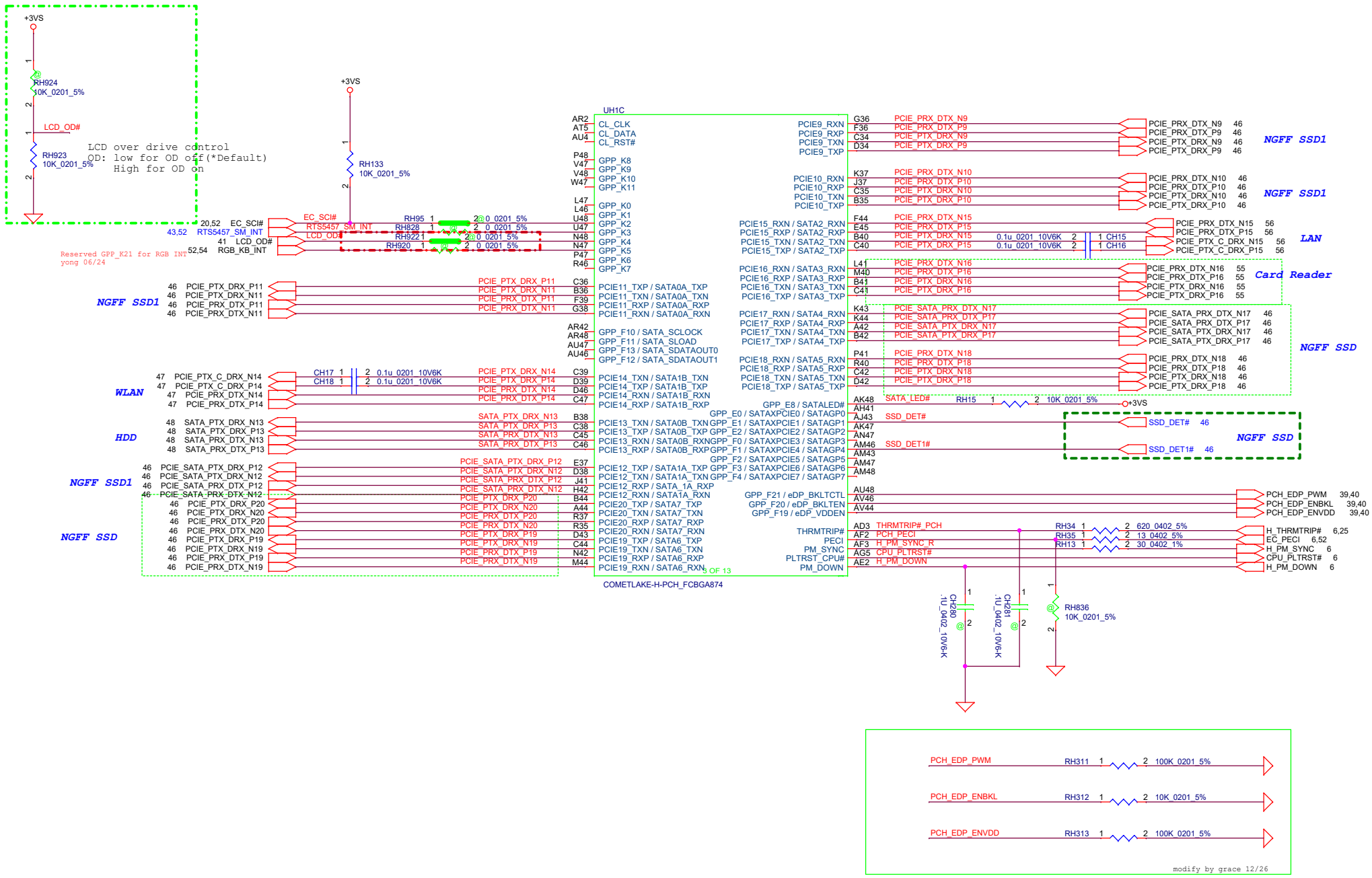

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PCH (1/9) PCIe/SATA/GPPFG**

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NEED close to PCH

EMC_NS@ 33P_0201_50V8-J 2 1 CH296 LPC_AD3
EMC_NS@ 33P_0201_50V8-J 2 1 CH293 LPC_AD2
EMC_NS@ 33P_0201_50V8-J 2 1 CH294 LPC_AD1
EMC_NS@ 33P_0201_50V8-J 2 1 CH295 LPC_AD0

HuiH request Reserved Cap 11/12

Back USB (3.0)

Right USB (3.0) DB

Back USB (3.0)

LEFT USB (3.0) MB(AOU)

TYPE-C USB (3.0)

UH1F

50 USB30_TX_N1 USB30_TX_N1 F9 USB31_1_TXN
50 USB30_TX_P1 USB30_TX_P1 F7 USB31_1_TXP
50 USB30_RX_N1 USB30_RX_N1 D11 USB31_1_RXN
50 USB30_RX_P1 USB30_RX_P1 C11 USB31_1_RXP
55 USB30_TX_N2 USB30_TX_N2 C3 USB31_2_TXN
55 USB30_TX_P2 USB30_TX_P2 D4 USB31_2_TXP
55 USB30_RX_N2 USB30_RX_N2 B9 USB31_2_RXN
55 USB30_RX_P2 USB30_RX_P2 C9 USB31_2_RXP

C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP

51 USB30_TX_N5 USB30_TX_N5 C15 USB31_5_TXN
51 USB30_TX_P5 USB30_TX_P5 B15 USB31_5_TXP
51 USB30_RX_N5 USB30_RX_N5 J13 USB31_5_RXN
51 USB30_RX_P5 USB30_RX_P5 K13 USB31_5_RXP

49 USB30_TX_P3 USB30_TX_P3 G12 USB31_3_TXP
49 USB30_TX_N3 USB30_TX_N3 F11 USB31_3_TXN
49 USB30_RX_P3 USB30_RX_P3 C10 USB31_3_RXP
49 USB30_RX_N3 USB30_RX_N3 B10 USB31_3_RXN

44 TYPE-C_USB3_TX_P4 TYPE-C_USB3_TX_P4 C14 USB31_4_TXP
44 TYPE-C_USB3_TX_N4 TYPE-C_USB3_TX_N4 B14 USB31_4_TXN
44 TYPE-C_USB3_RX_P4 TYPE-C_USB3_RX_P4 J15 USB31_4_RXP
44 TYPE-C_USB3_RX_N4 TYPE-C_USB3_RX_N4 K16 USB31_4_RXN

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COMETLAKE-H-PCH_FCBGA874

GPP_A1 / LAD0 / ESPI_IO0 BB39 LPC_AD0_R RH128 1 2@0_0201_5% LPC_AD0 52
GPP_A2 / LAD1 / ESPI_IO1 AW37 LPC_AD1_R RH130 1 2@0_0201_5% LPC_AD1 52
GPP_A3 / LAD2 / ESPI_IO2 AV37 LPC_AD2_R RH131 1 2@0_0201_5% LPC_AD2 52
GPP_A4 / LAD3 / ESPI_IO3 BA38 LPC_AD3_R RH132 1 2@0_0201_5% LPC_AD3 52

+3VS

10K_0201_5% RH104
10K_0201_5% RH113

GPP_A5 / LFRAME# / ESPI_CS0# BE38 LPC_FRAME# LPC_FRAME# 52
GPP_A6 / SERIRQ / ESPI_CS1# AW35 SERIRQ SERIRQ 52
GPP_A7 / PIRQA# / ESPI_ALERT0# BA36 TPM_SPI_IRQ# 55
GPP_A0 / RCIN# / ESPI_ALERT1# BE39 KBRST# KBRST# 52
GPP_A14 / SUS_STAT# / ESPI_RESET# BF38

For LPC_CLK
R: 0Ω to 22Ω

GPP_A9 / CLKOUT_LPC0 / ESPI_CLK BB36 CLK_PCI_EC_R RH84 1 2 22_0402_5% CLK_PCI_EC CLK_PCI_EC 52
GPP_A10 / CLKOUT_LPC1 BB34

GPP_K19 / SMI# T48 PCH_SMI# RH821 1 2 0_0201_5% EC_SMI# 18,52
GPP_K18 / NMI# T47 RH129 1 2 10K_0201_5% +3VS

CH265 33P_0402_50V8J EMC@

V0.4

GPP_E6 / SATA_DEVSLP2 AH40
GPP_E5 / SATA_DEVSLP1 AH35 DEVSLP DEVSLP 46
GPP_E4 / SATA_DEVSLP0 AL48
GPP_F9 / SATA_DEVSLP7 AP47
GPP_F8 / SATA_DEVSLP6 AN37
GPP_F7 / SATA_DEVSLP5 AN46
GPP_F6 / SATA_DEVSLP4 AR47 DEVSLP1 DEVSLP1 46
GPP_F5 / SATA_DEVSLP3 AP48

NGFF SSD

change DEVSLP to SATA Port1 by Bing 0621
change DEVSLP1 to SATA Port7 by Bing 0621
H: Sleep Mode
L: Active Mode

UH1E

44 TYPE-C_DP_HPD AT6 GPP_I0 / DDPB_HPD0 / DISP_MISC0
42 HDMI_HPD AN10 GPP_I1 / DDPC_HPD1 / DISP_MISC1
AP9 GPP_I2 / DDPD_HPD2 / DISP_MISC2
47 CNVI_EN# CNVI_EN# AL15 GPP_I3 / DDPF_HPD3 / DISP_MISC3

GPP_I5 / DDPB_CTRLCLK AL13 DDPB_CLK PAD1 @IT37
GPP_I6 / DDPB_CTRLDATA AR8 DDPB_DATA
GPP_I7 / DDPC_CTRLCLK AN13 DDPC_CLK PAD 1 @IT28
GPP_I8 / DDPC_CTRLDATA AL10 DDPC_DATA
GPP_I9 / DDPD_CTRLCLK AL9 DDPD_CLK PAD 1 @IT36
GPP_I10 / DDPD_CTRLDATA AR3 DDPD_DATA
GPP_F23 / DDPF_CTRLDATA AN40
GPP_F22 / DDPF_CTRLCLK AT49

GPP_F14 / PS_ON# AP41

39 PCH_EDP_HPD PCH_EDP_HPD AN6 GPP_I4 / EDP_HPD / DISP_MISC4

RH310 100K_0201_5% @

GPP_K23 / IMGCLKOUT1 M45
GPP_K22 / IMGCLKOUT0 L48
GPP_K21 T45
GPP_K20 T46
GPP_H23 / TIME_SYNC0 AJ47

5 OF 13

COMETLAKE-H-PCH_FCBGA874

+3VS

DDPB_DATA RH834 1 @ 2 2.2K_0201_5%
DDPC_DATA RH33 1 @ 2 2.2K_0201_5%
DDPD_DATA RH835 1 @ 2 2.2K_0201_5%

DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
* L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
* L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
* L Port D is not detected. (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (2/9) USB3/GPPAEFGHI

Size	Document Number	Rev
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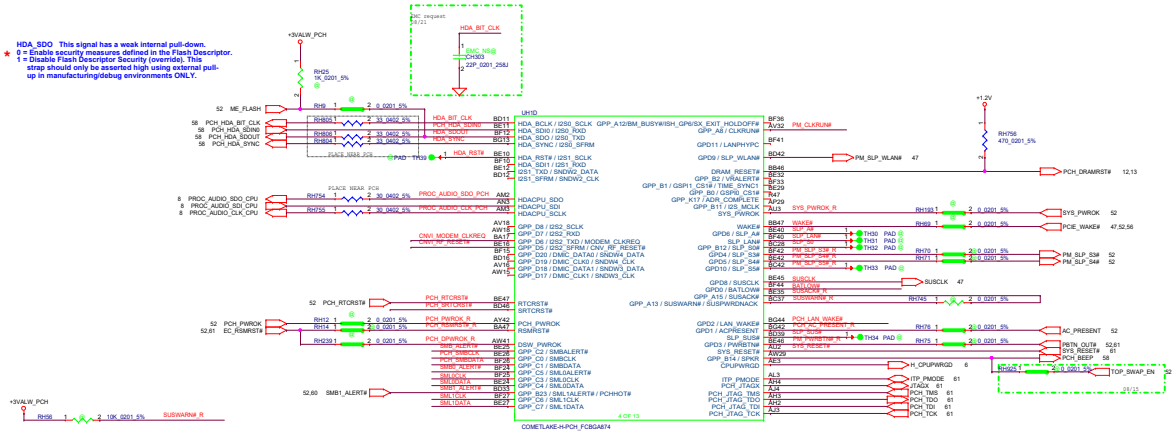
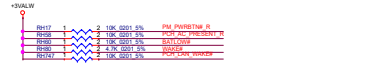
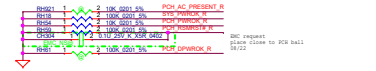
HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.







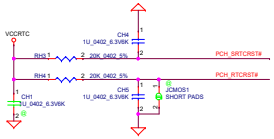
Strap

GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS (Default)

GPP_C5 /SML0ALERT#
This Signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

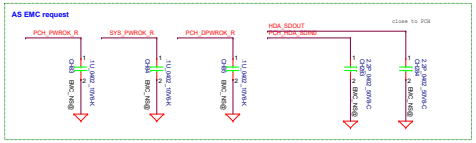
GPP_B23 /SML1ALERT#/PCHHOT#
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Note:When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

CMOS

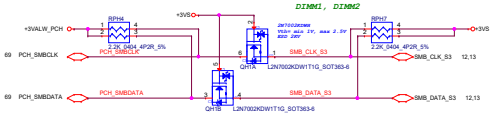


SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable _Top Swap= mode. (Default)
1 = Enable _Top Swap= mode.

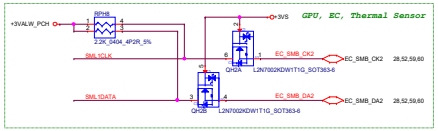
AS EMC request

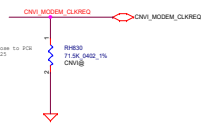


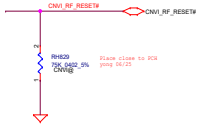
DIMM1, DIMM2

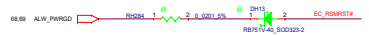


GPU, EC, Thermal Sensor





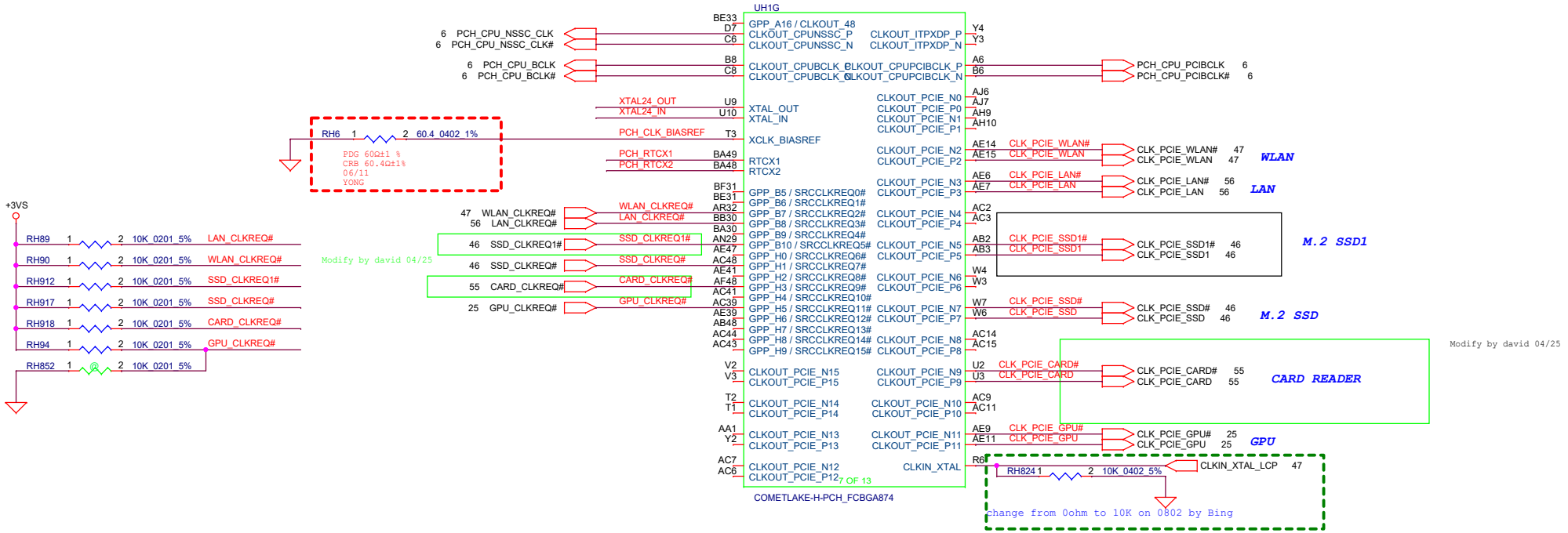


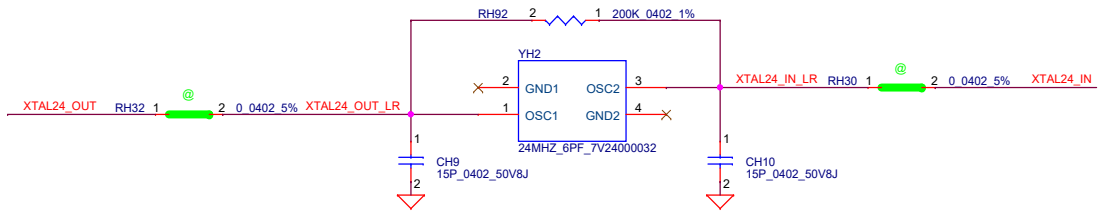


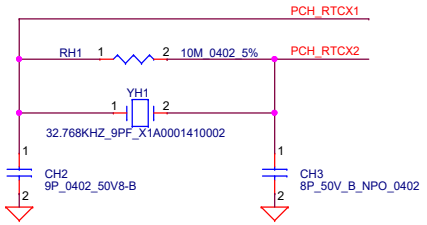
RSMRST# sequence control circuit

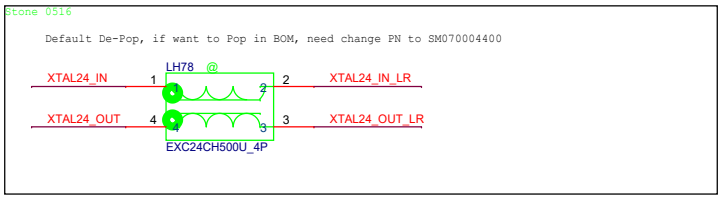
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PCH (3/9) HDA,RTC,SMBUS,PM		
Size D	Document Number ¥550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 16 of 83		









Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PCH (3/9) CLOCK,GPPBH**

Size	Document Number	Rev
A3	Y550	1.0

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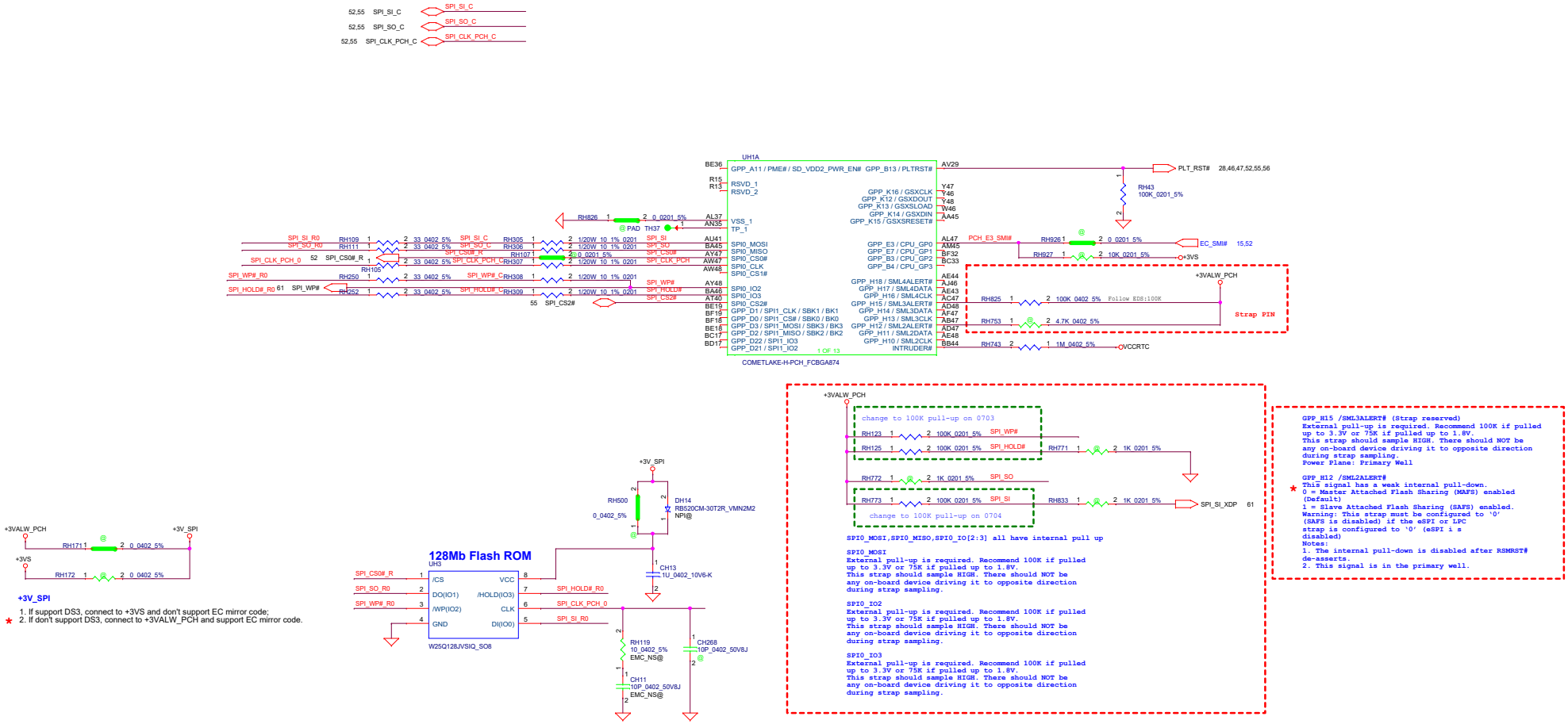

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
A2	Y550	1.0

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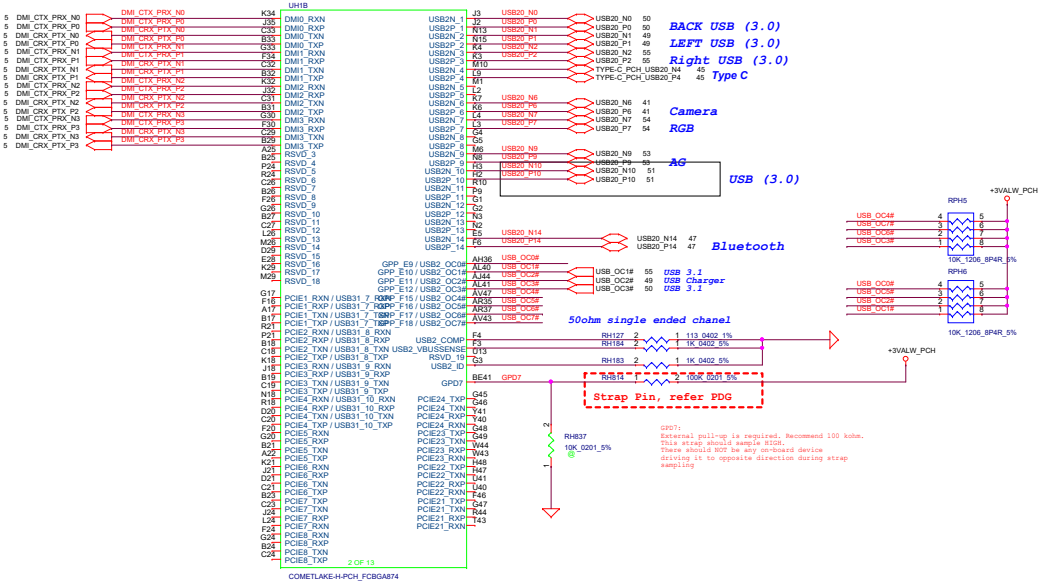

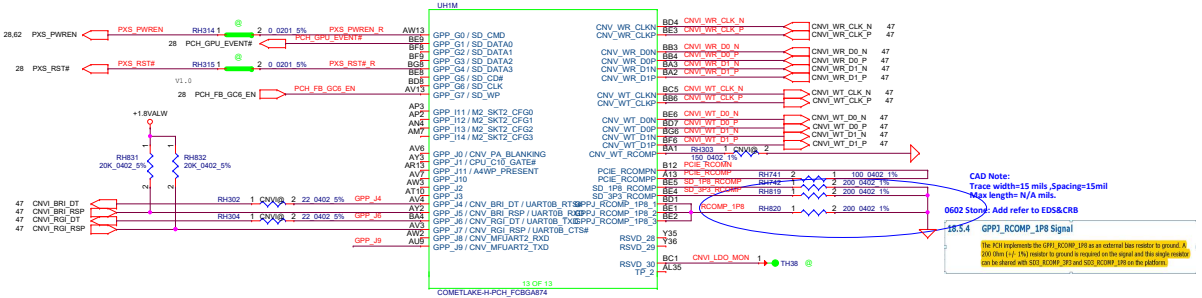

Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Blank		
Size	Document Number		Rev
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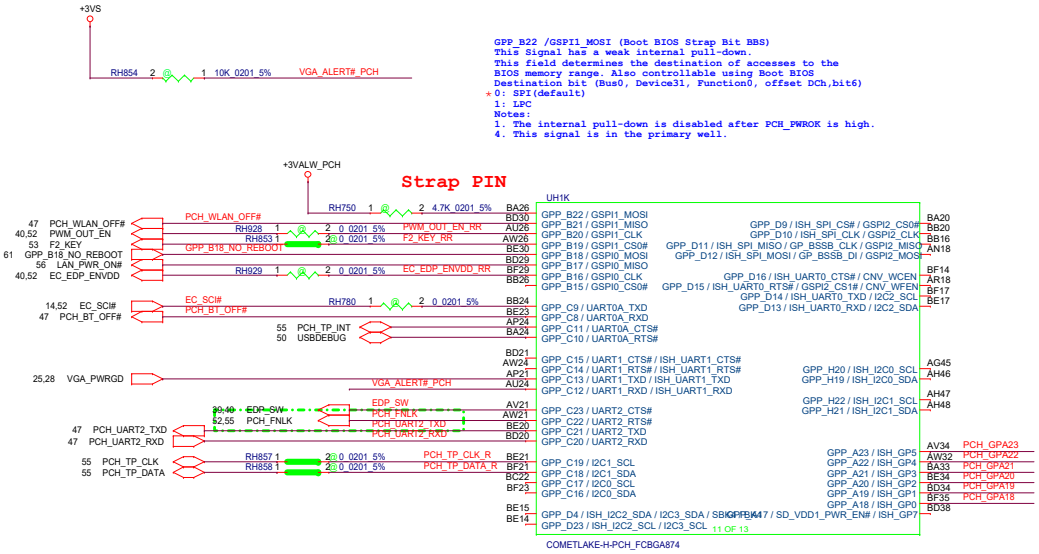
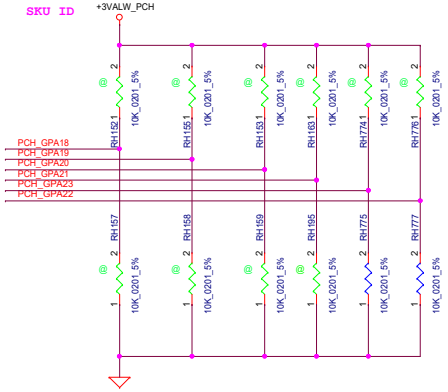
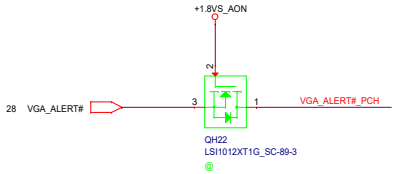
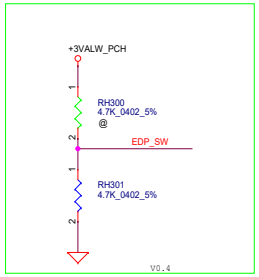


Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC





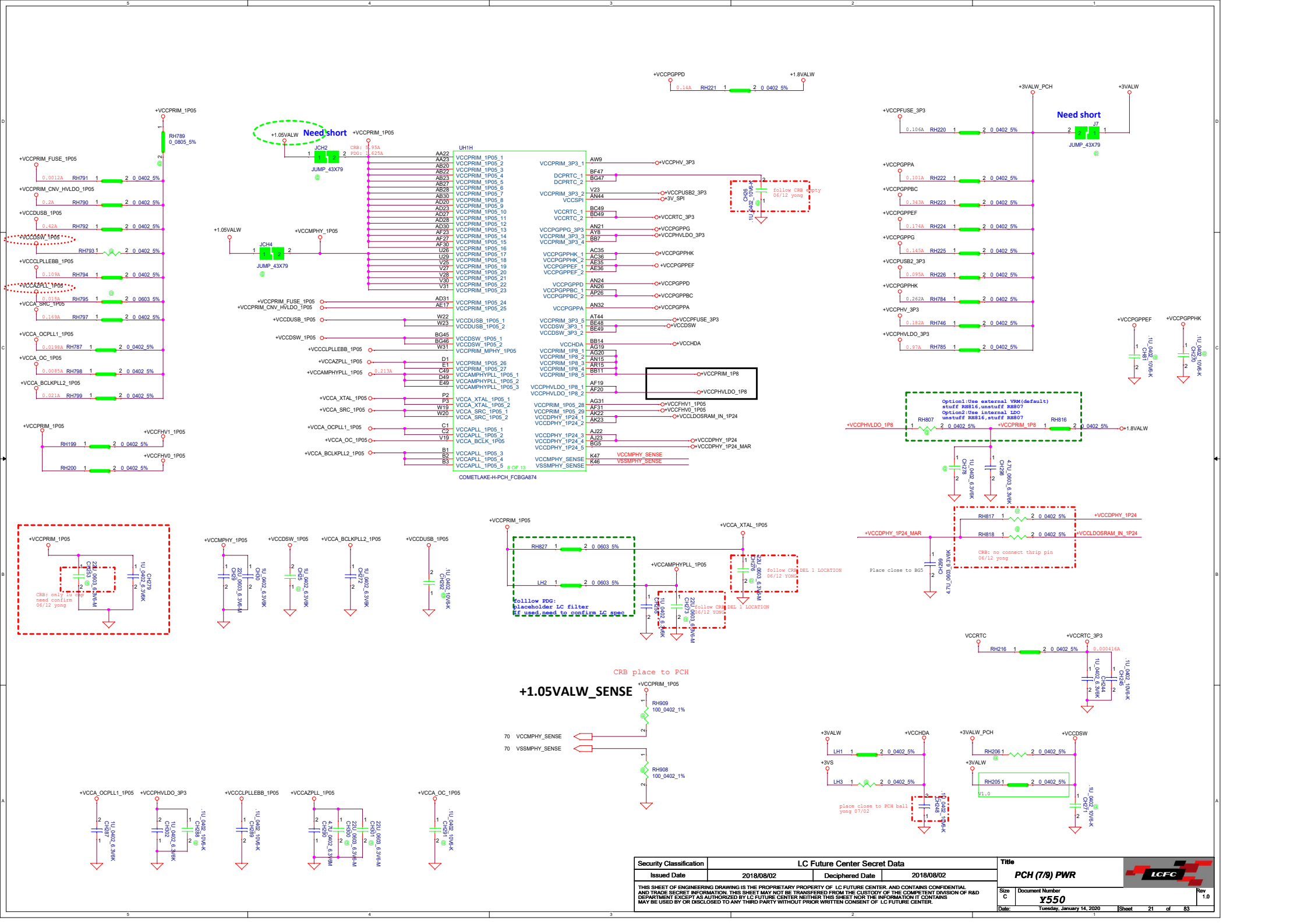


Board ID table need modify
yong 07/10

PCH_GPA22 add for distinguish
L350: H
Y550:L
yong 07/11

Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22 (L340: H Y550: L)	PCH_GPA23 (Reserved)
Y550-15-N18E G0	0	0	0	0	0	0
Y550-15-N18E G1	0	0	0	1	0	0
Y550-15-N18P G61	0	0	1	0	0	0
Y550-15-N18P G62	0	0	1	1	0	0
Y540-17-N18E G0	0	1	0	0	0	0
Y540-17-N18E G1	0	1	0	1	0	0
Y540-17-N18P G61	0	1	1	0	0	0
Y540-17-N18P G62	0	1	1	1	0	0

Title			
PCH (6/9) GPPPABCD, I2C			
Size C	Document Number Y550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 20 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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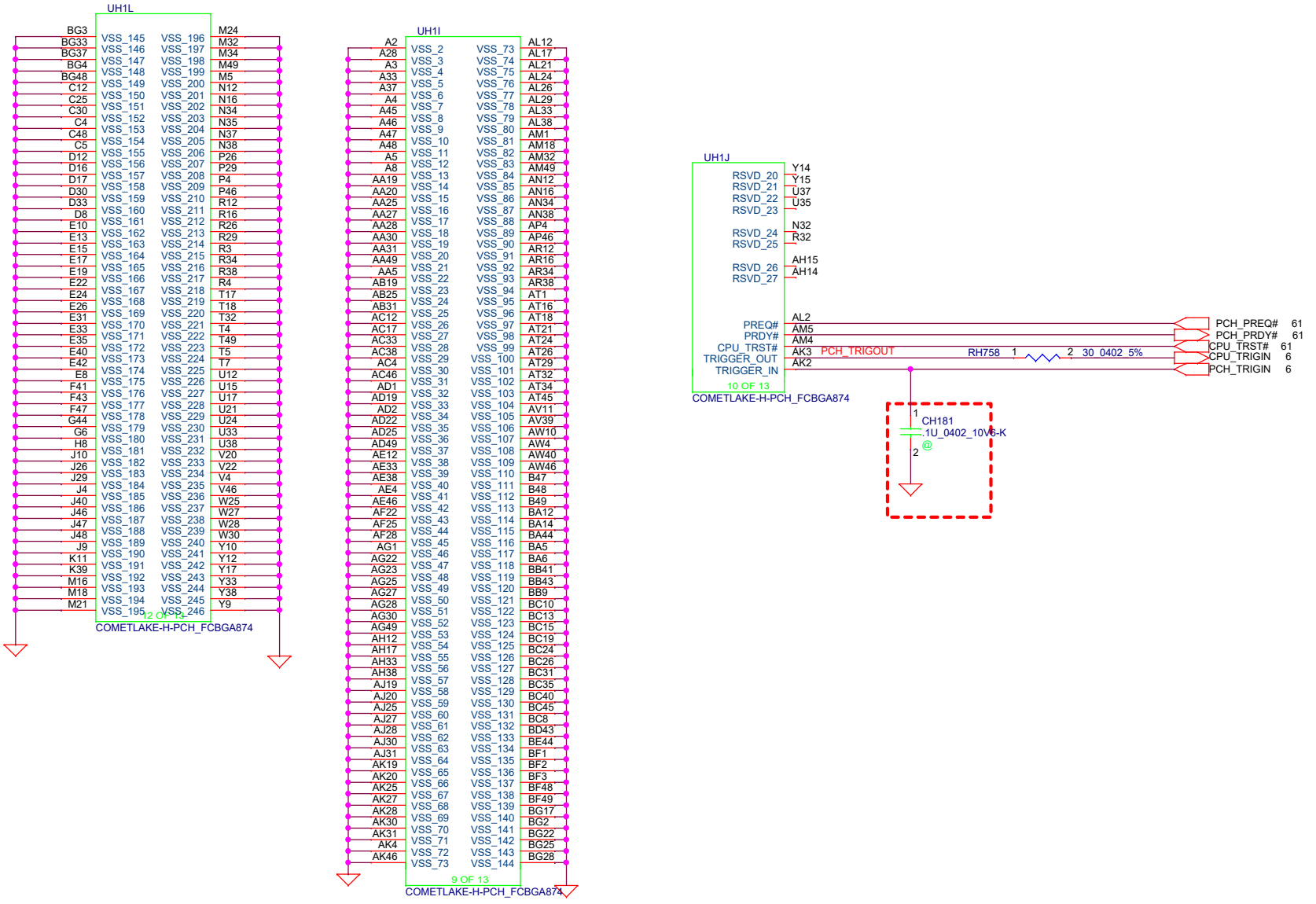
Title	PCH (7/9) PWR		
Size	Document Number		Rev
C	Y550		1.0
Date:	Tuesday, January 14, 2020	Sheet	21 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
B	Y550	1.0

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Security Classification	LC Future Center Secret Data		
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Title

Blank

LCFC

Size	Document Number	Rev
B	*Y550*	1.0

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N18P-G61 G62 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU EVENT	
GPIO3	OUT	-	GPU MUX controler	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight (PWM)enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power (LCD_VDD)enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	IN	N/A	IGPU Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA(TYPE-C)	
GPIO15	IN	N/A	Hot Plug Detect for IFPB(NA)	
GPIO16	OUT	-	DGPU PWM switch select	
GPIO17	IN	N/A	Hot Plug Detect for IFPD(DGPU eDP HPD)	
GPIO18	IN	N/A	Hot Plug Detect for IFPE(NA)	
GPIO19		N/A	NA	
GPIO20		N/A	GC6_MODE	
GPIO21	O	N/A	DGPU Backlight Enable	
GPIO22	O	N/A	ADC MUX select	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24		N/A	NA	
GPIO25			FVDDQ_PSI	
GPIO26		N/A	FP-FUSE	
GPIO27	IN	N/A	Hot Plug Detect for IFPC(HDMI)	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

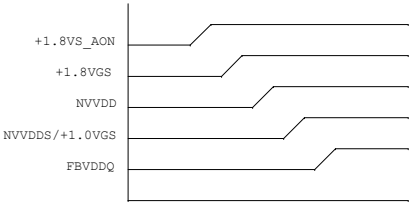
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N18P-G61 G62 Power Sequence

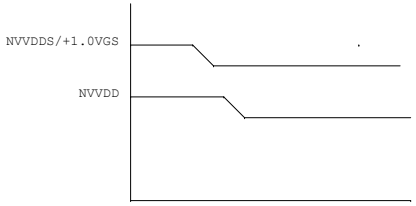


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data		
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Title: VGA Notes List

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C	¥550	1.0

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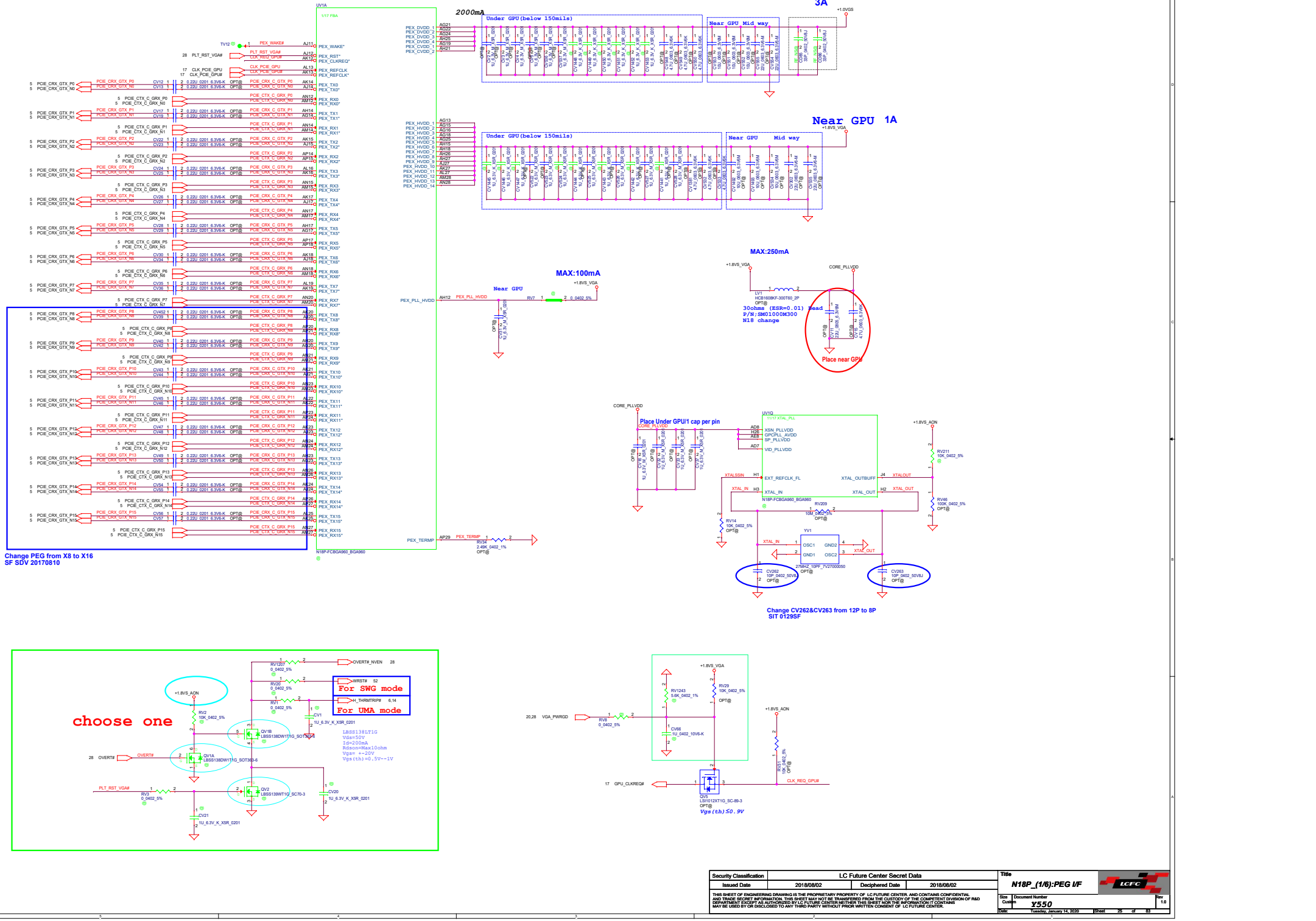

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18P_(1/6):PEG I/F

Size	Document Number	Rev
Custom	Y550	1.0
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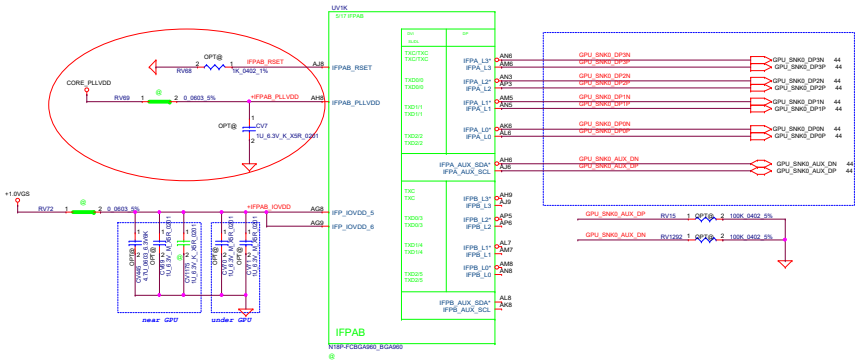
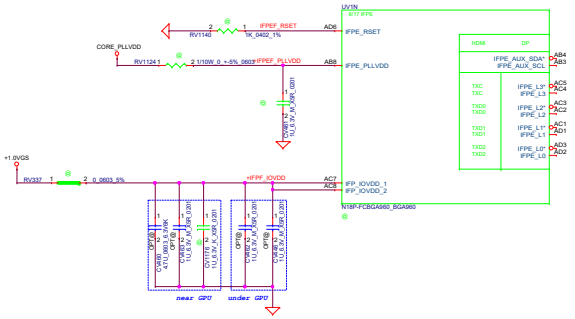
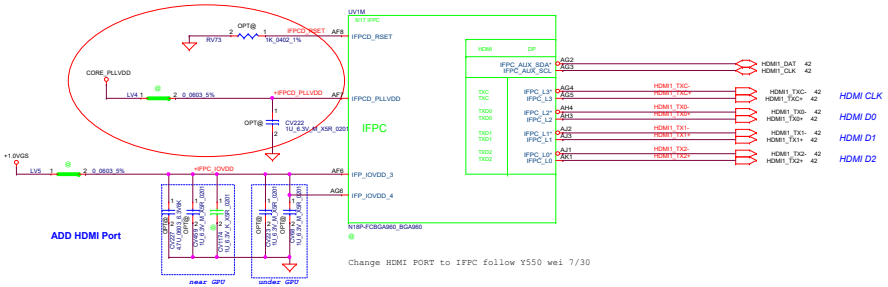
Ref NV DG-08780-001
If an IFP link is unused, in general it should be left unconnected.
This includes Main and Aux links.
IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF)
can be left unconnected if neither of IFPx /IFPy is in use



for Type-C DP





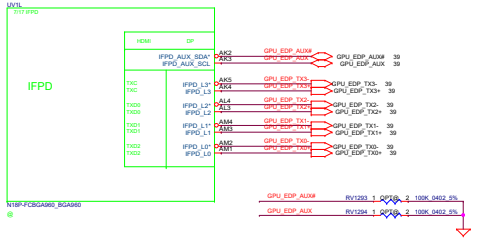
For HDMI

ADD HDMI Port

Change HDMI PORT to IFPC follow Y550 wei 7/30

Decouling Value

MLCC	N18	N17	location
CV7	1uf	0.1uf	Under
CV222	1uf	0.1uf	Under
CV461	1uf	0.1uf	Under
CV70	1uf	0.1uf	Under
CV71	1uf	0.1uf	Under
CV223	1uf	0.1uf	Under
CV68	1uf	0.1uf	Under
CV462	1uf	0.1uf	Under
CV484	1uf	0.1uf	Under



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *N18P_(3/6):VRAM I/F*

Size	Document Number	Rev
D	*Y550*	1.0

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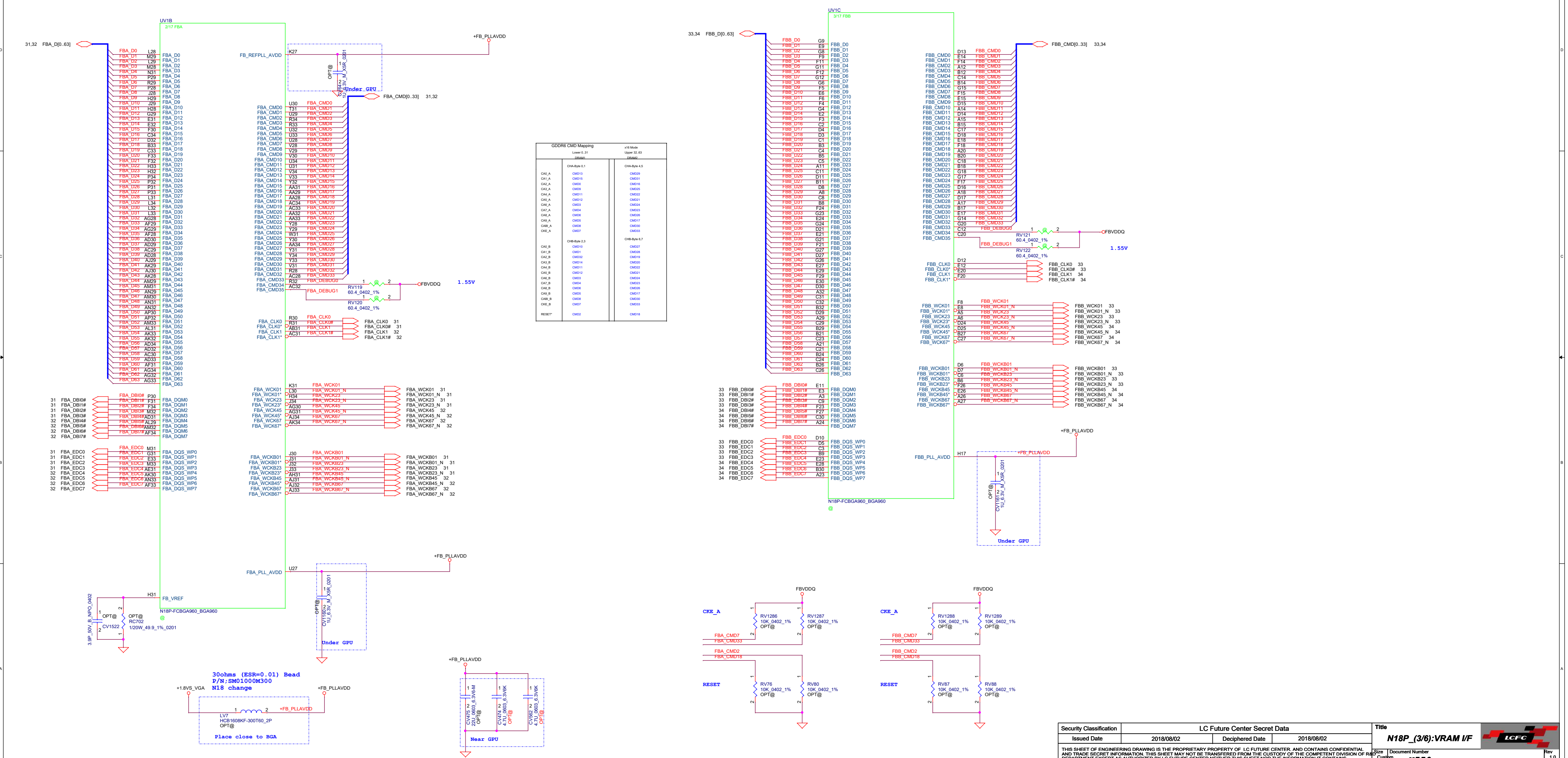
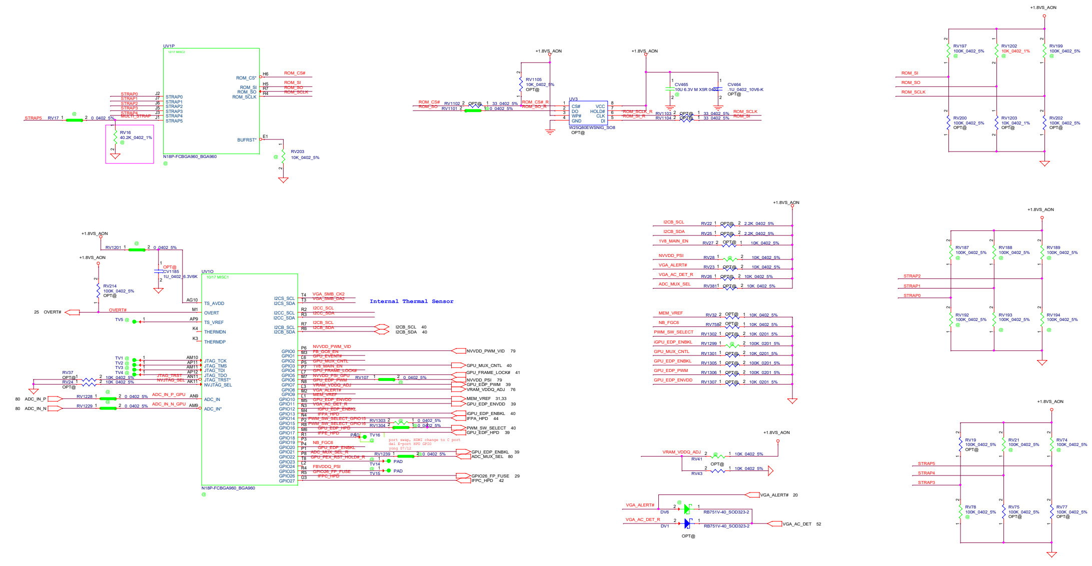


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18P_(3/6):VRAM I/F

Size: Custom | Document Number: Y550 | Rev: 1.0

Date: Tuesday, January 14, 2020 |



1:ENABLE 0:DISABLE
SOR0 DISABLE
SOR1/2/3 ENABLE

GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N18P	L	L	L	ENABLE

VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
4GB	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H

VGA_DEVICE

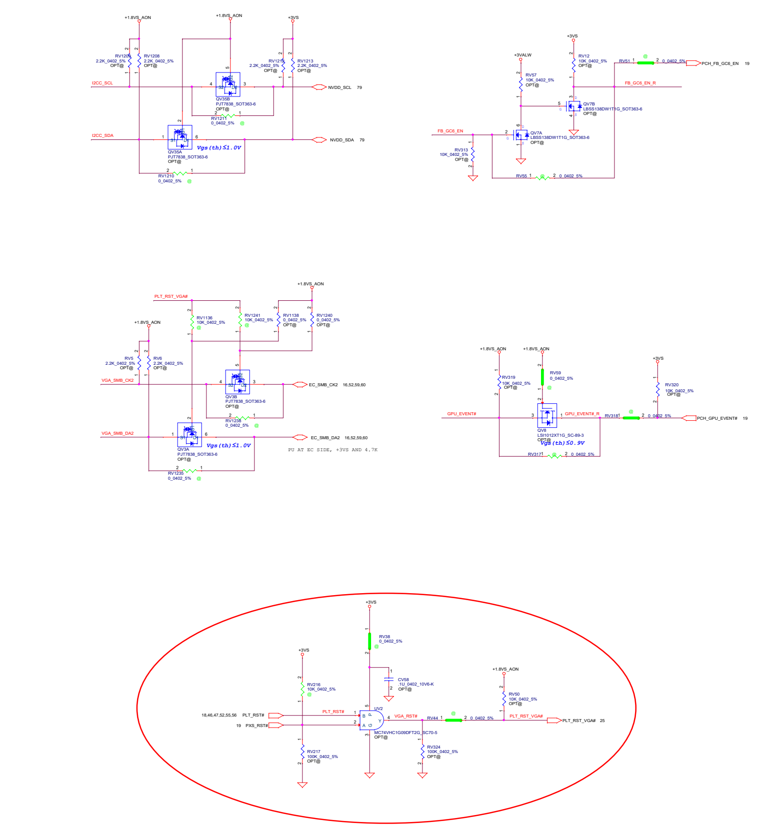
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

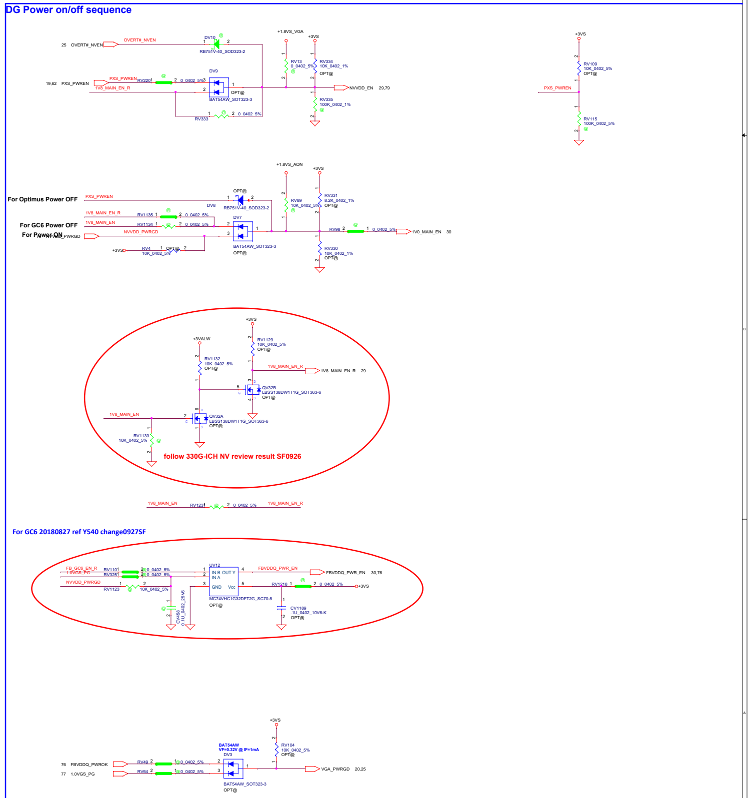
1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



DG Power on/off sequence



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18P_(4/6):GPIO
Size: Custom — Document Number: Y550 — Rev 1.0
Date: Thursday, January 16, 2020

5A Peak 8A

Cost down list:
1U 4Pcs

Partition A Under GPU(below 150mils)

Partition B Under GPU(below 150mils)

Under GPU(below 150mils)

Near GPU

Near GPU

1.8V Total 1A (AON+MAIN)

0.5A

under GPU

near GPU

FP_FUSE_GPU

CALIBRATION PIN	N18P
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	40.2Ohm

RV94 40.2ohm 60.4ohm

Place near balls

PLACE MIDWAY BETWEEN FBA AND FBB

only for N18P

Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

AG26,AJ28 NC pin,
only for under GPU 1.8VS_VGA layout trace

2A

V20B+

AON7408L
Vds=30V
Ids=15A
Rdson=28mohm@Vgs=4.66V
=20mohm@Vgs=6V
=18mohm@Vgs>10V
Vgs=+-20V
Vgsth=1~3V

Vg=16.4V@AC
Vg=7.38V@Battery

+1.8V_MAIN discharger circuit

Reserve PD3/PR4/PR5/CV38 for NV sequence requirement

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Title: N18P_(5/6):PWR

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BOTH GP107 AND N18P-G5 NEED
NC AF30,AF32,AK31,AM34,E34,H30,M30,M34,
A30,A9,B2,B23,D22,D28,D9,E4

UV1D
UV1F
UV1G
UV1E
NVVDD
N18P-FCBGA960_BGA960

trace width: 16mils
differential voltage sensing.
differential signal routing.

VDD_SENSE L4 NVVDD_VDD_SENSE NVVDD_VDD_SENSE 79
GND_SENSE L5 NVVDD_VSS_SENSE NVVDD_VSS_SENSE 79

UNDER GPU

NEAR GPU

Add RV332 for NVVDDS discharge Hai Y520 SVT

Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725

+5VALW
+1.0VGS
RV60 47K_0402_5%
QV11 LBSS139WT1G_SC70-3
QV29 AO3402_SOT-23-3
QV12 AO3402_SOT-23-3
28,77 1V0_MAIN_EN

Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT

FBVDDQ
RV61 470_0603_5%
RV48 47K_0402_5%
QV6B 2N7002KDWH_SOT363-6
QV6A 2N7002KDWH_SOT363-6
28,76 FBVDDQ_PWR_EN

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18P_(6/6):PWR,VSS
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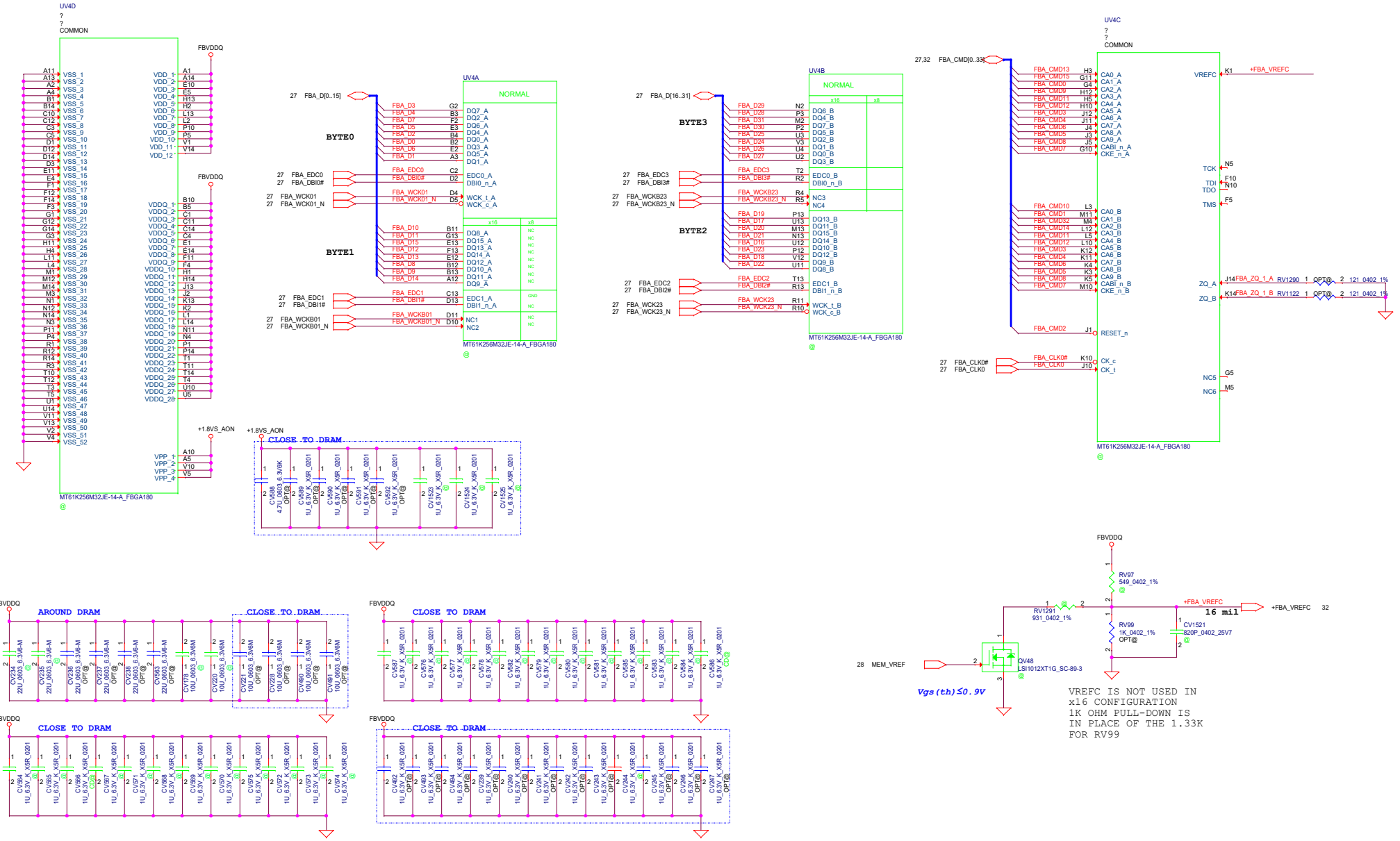
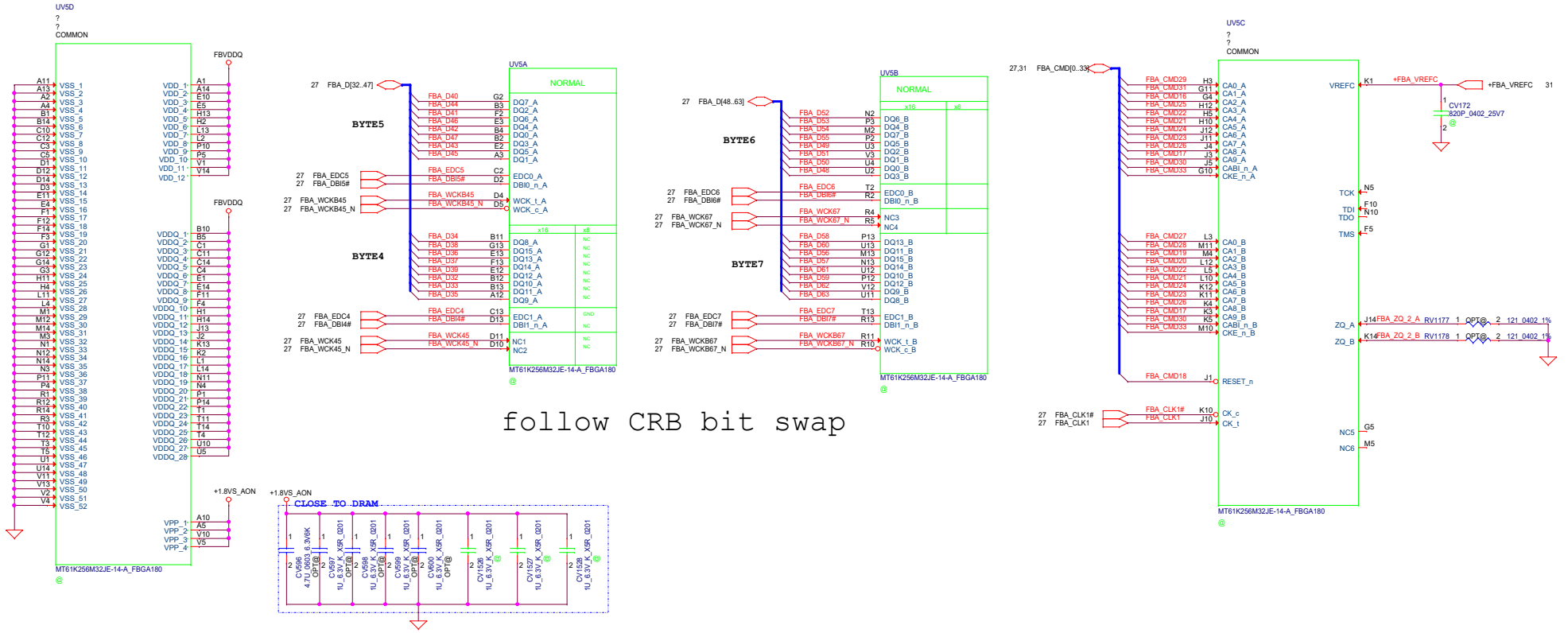
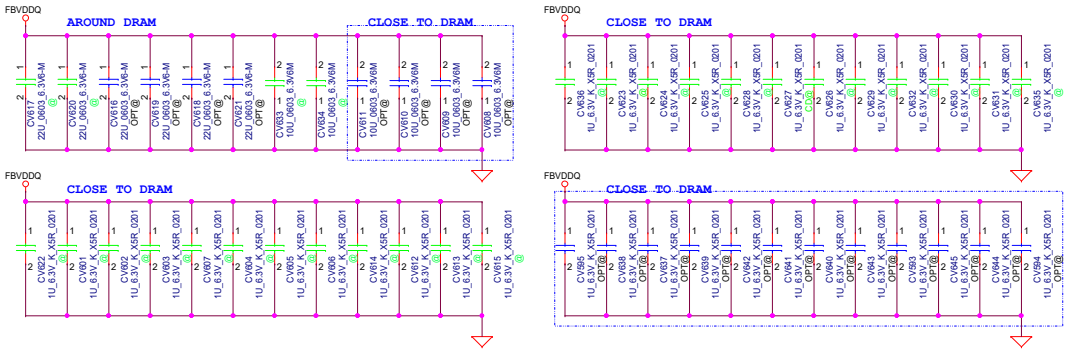
Date: Tuesday, January 14, 2020 | Sheet 30 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_GDDR6_A_[31_0]		
Size C	Document Number Y550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 31 of 83		



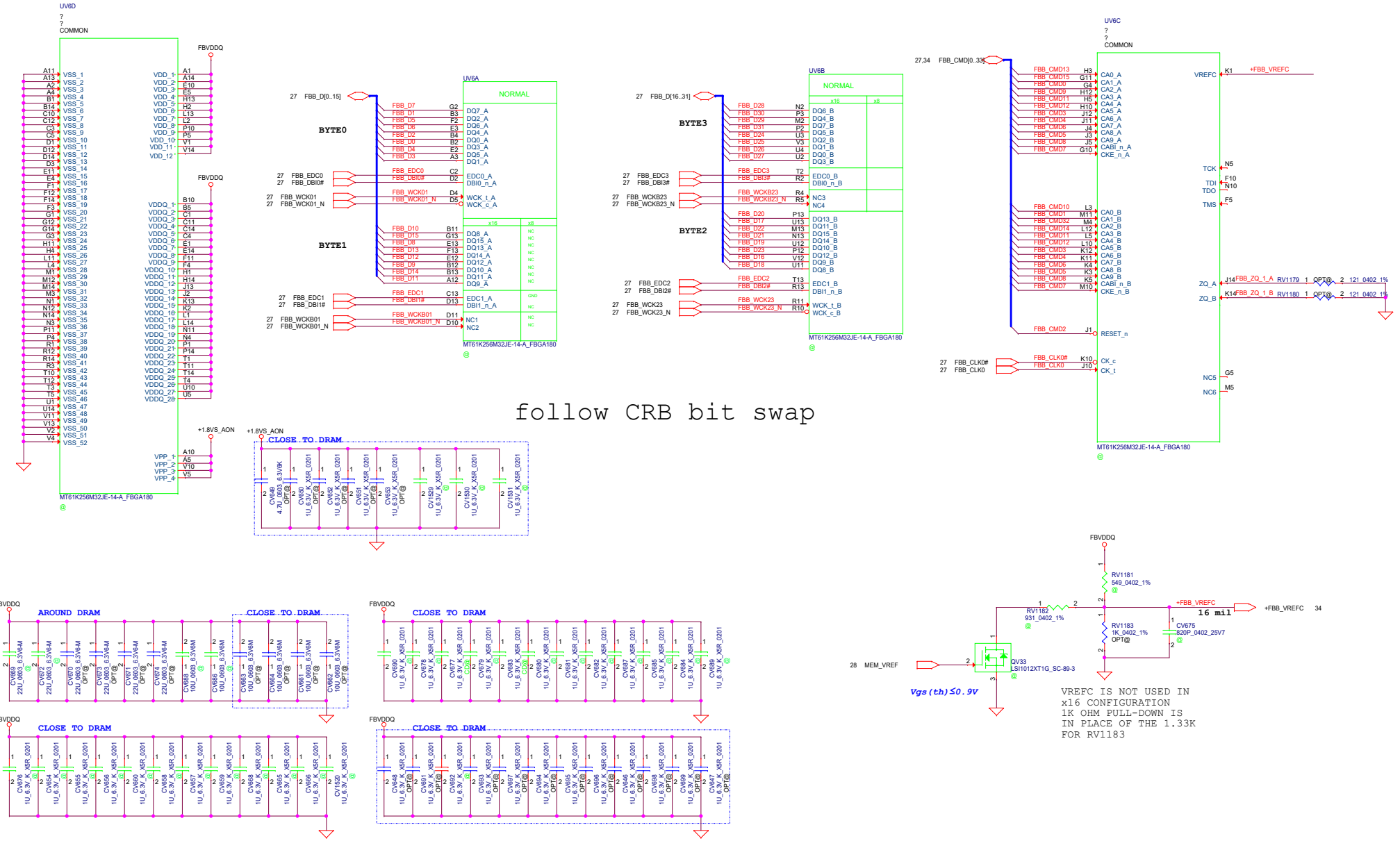


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18P_GDDR6_A_[63_32]

Size	Document Number	Rev
C	Y550	1.0

Date: Tuesday, January 14, 2020 | Sheet 32 of 83



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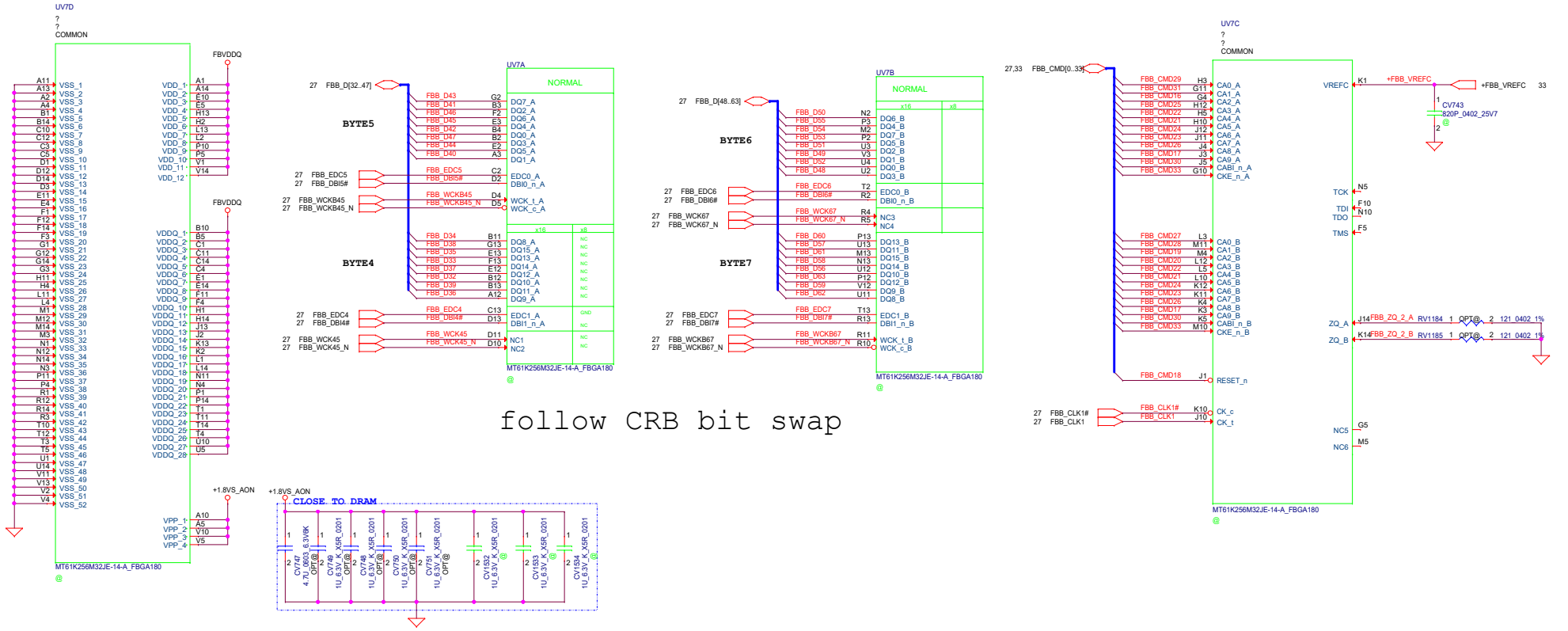
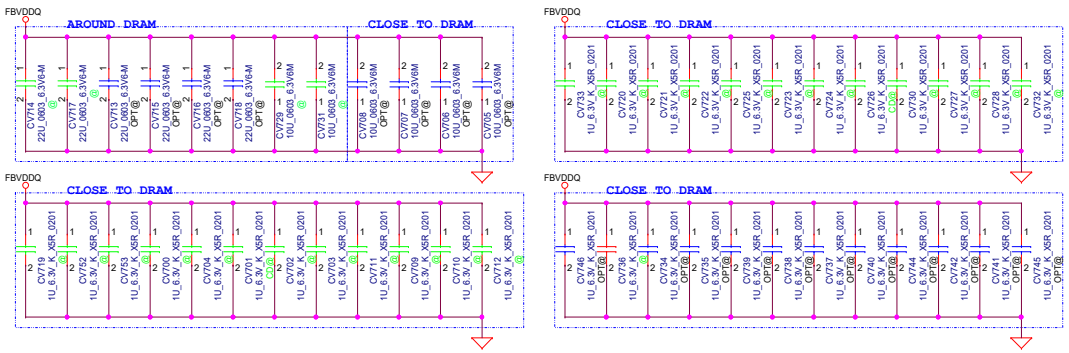
Title: N18P_GDDR6_B_[31_0]

Size: C | Document Number: ¥550 | Rev: 1.0

Date: Tuesday, January 14, 2020 | Sheet 33 of 83





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18P_GDDR6_B_[63_32]

Size	Document Number	Rev
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Title

Blank

Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
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Title

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Size	Document Number	Rev
B	Y550	1.0

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Security Classification	LC Future Center Secret Data		
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Title

Blank

Size	Document Number	Rev
B	Y550	1.0

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Title

Blank

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SA000060U00, S IC PS8331BQFN60GTR-A2 QFN 60P DP SWITCH symbol & footprint apply

UR2

PS8331BQFN60GTR-A1_QFN60_5X9

need fine tune RR59/RR60/RR61
BOM structure
08/08

UR3 CB3257ABQ_DHVQFN16_2P5X3P5

UR4 UR5 UR6 M74VHC1GT125DF2G_SC70-5

QR5822 MMBT3904WH_SOT323-3

QR5821 L2N7002KWT1G_SOT323-3

QR28A QR28B PJT7838_SOT363-6

Vgs(th)≤1.0V

EDP_SW :Port switching control configuration; Internal pull down at ~150KΩ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected

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Title: EDP MUX

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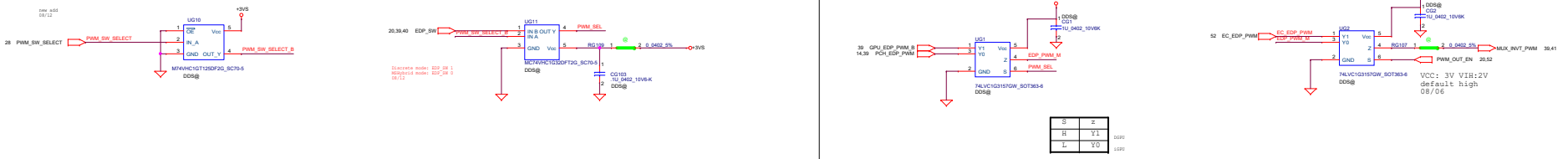
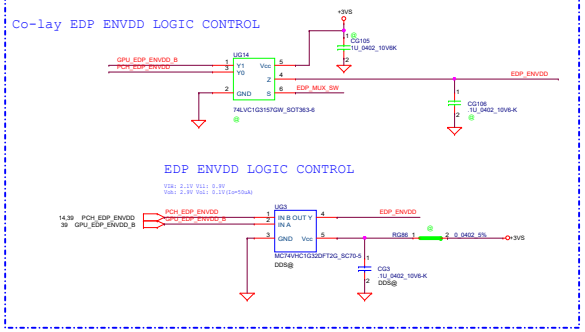
need fine tune RG107 RG108 RG88 BOM structure
08/08

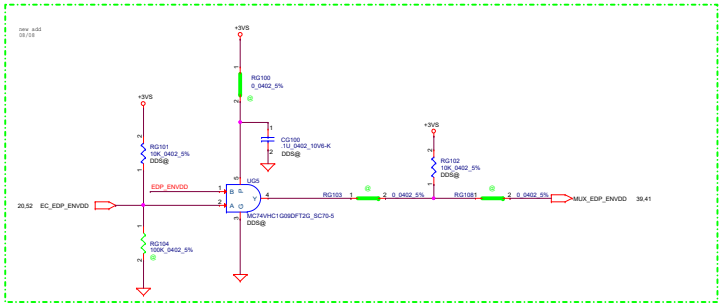
EDP PWM LOGIC CONTROL

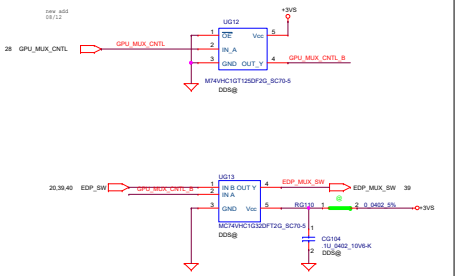


S	z
H	Y1
L	Y0

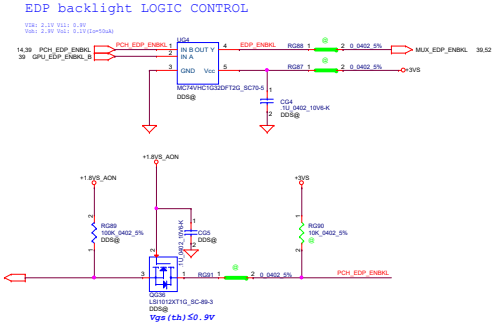
Co-lay EDP ENVDD LOGIC CONTROL



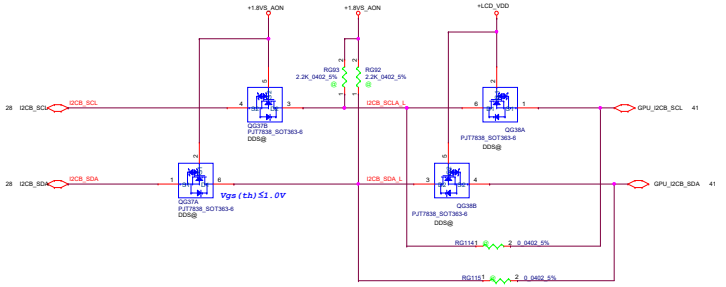




EDP backlight LOGIC CONTROL



level shift for I2C



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Title		
DC V TO VS INTERFACE		
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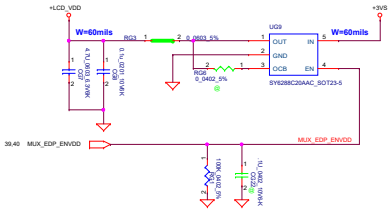
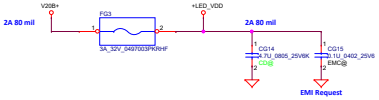
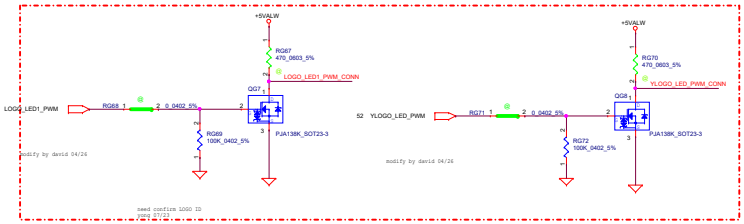
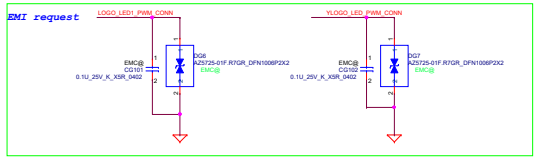
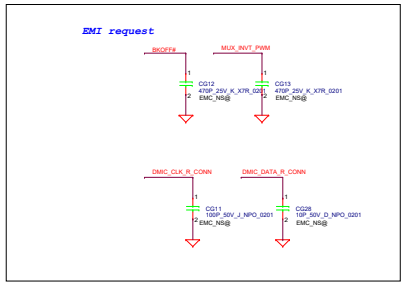
LCD POWER CIRCUIT

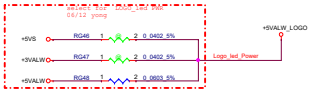


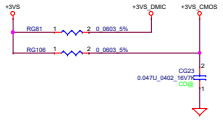


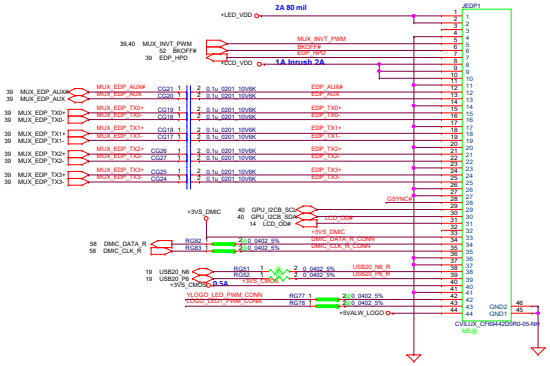


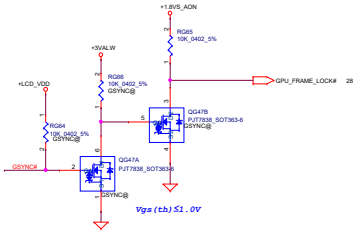


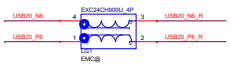












Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	eDP/ CMOS/Touch screen		
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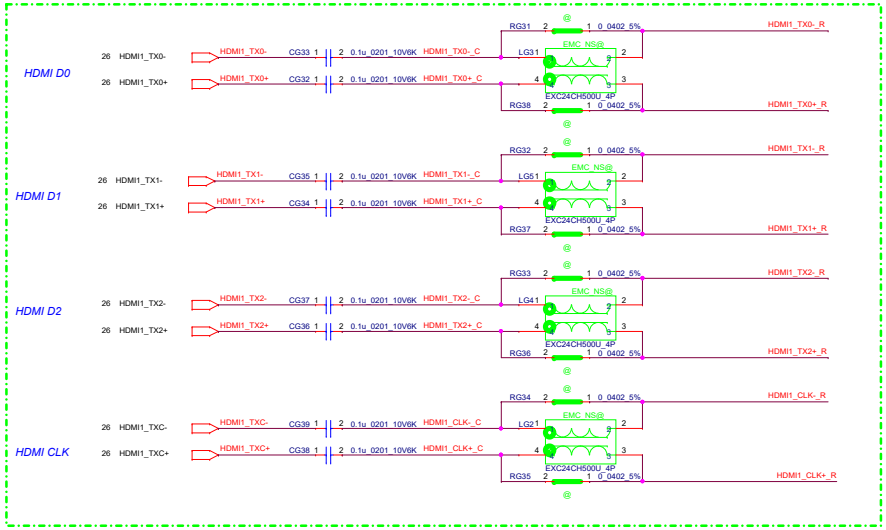

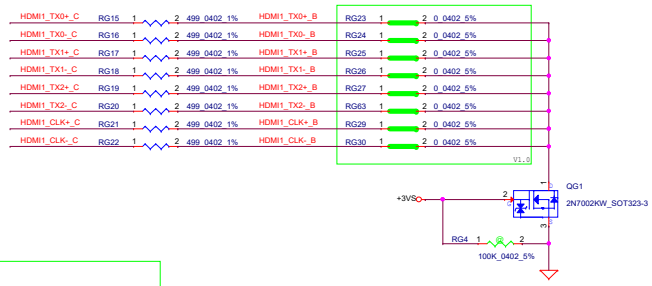

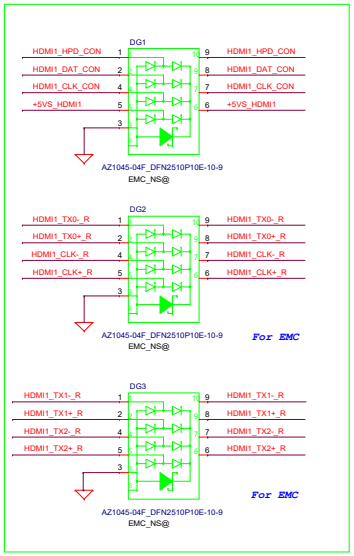

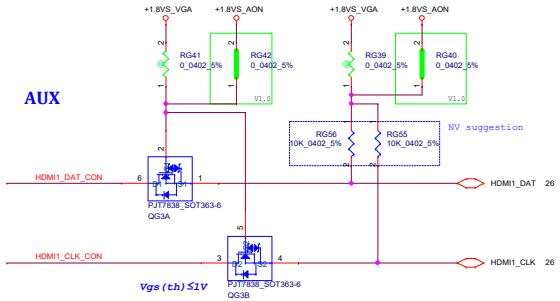

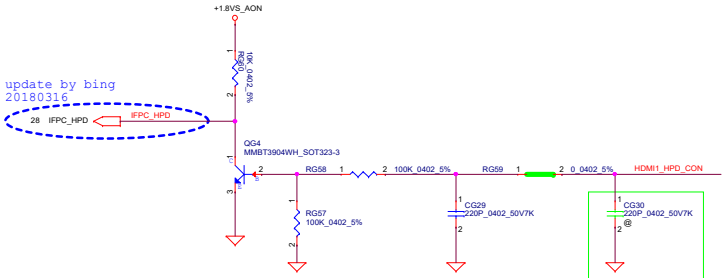

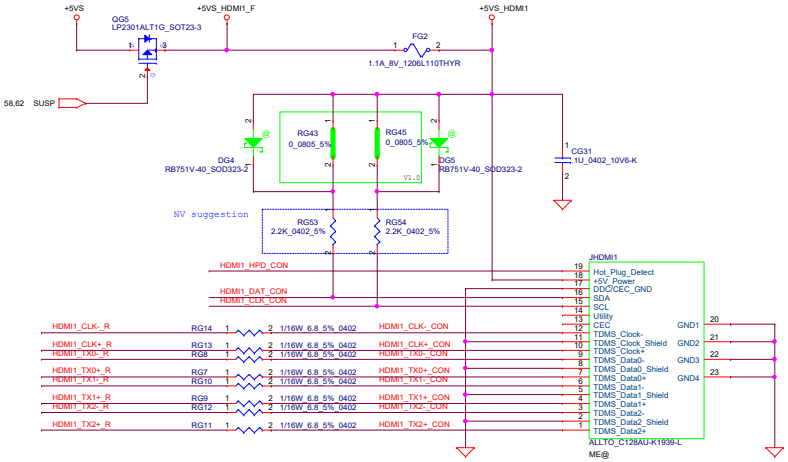

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Title	HDMI_CONN		
Size	Document Number		Rev
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Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

VMON:
Used to monitor VBUS voltage.
Divide the VBUS voltage down to ADC full-scale input of 1.2V.
Then connect the divided voltage to this pin.

+VBUS_P0 — RT45 200K_0402_1% — VMON — RT40 10K_0402_1%

+5VALW — RT41 590K_0402_1% — LOC_PWR_MON — RT46 10K_0402_1%

+LDO_3V3 — RT42@ 0_0402_5% — RT47 10K_0402_1%

RA=RT42

RB=RT47

+3VALW — RT11 0_0402_5%

EC

52,53,54,60,72 EC_SMB_CK0 — QT1A 2N7002KDWH_SOT363-6 — SM_CK

52,53,54,60,72 EC_SMB_DA0 — QT1B 2N7002KDWH_SOT363-6 — SM_SDA

2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV

RT9 2 0_0402_5%

RT10 2 0_0402_5%

+VCON_IN — 500mA — CT102 10U_0805_10V6K — CT101 .1U_0402_10V6-K

place close to pin13

+5VALW — RT48 2 0_0603_5% — +VCON_IN

CT1 10U_0603_10V6K

QT2 AO3413_SOT23-3 SB93413000J

VDS=-20
VGS=+-8V
Id=3A
Vth=-1v

I2C1_IRQ# — RT55 2 47K_0402_5%

100mA — +5VALW — RT103 2 0_0603_5%

100mA — +5V_IN

+5V_IN — CT2 4.7U_10V_K_X5R_0402 — CT3 10U_0603_10V6K

+LDO_3V3 — CT4 4.7U_0402_6.3V6M — CT103 0.1U_6.3V_K_X5R_0201

for redriver pin control mode used
this pin can be fonfigured as digital GPIO via F/W
in some applications
06/13 yong

RT14 1 2 0_0402_5% — PS8747_FLIP_C1 44

for redriver pin control mode used
06/13 yong

44 PS8747_USB_MODE_C1 — RT16 1 2 0_0402_5%
44 PS8747_DP_MODE_C1 — RT15 1 2 0_0402_5%

UT2

AUX_N/MGPIO5
AUX_P/MGPIO4
SBU2/MGPIO7
SBU1/MGPIO6
VCON_IN
5V_IN
LDO_3V3
BB_DM/MGPIO1
BB_DP/MGPIO0
CC2
CC1

PS8747_FLIP_C1_R — VBUS_DSCHG — VBUS_DSCHG 45

EMC@ CT51 2 220P_0402_50V_X7R_0402

USBC_CC2_CONN — USBC_CC2_CONN 45
USBC_CC1_CONN — USBC_CC1_CONN 45

EMC@ CT61 2 220P_0402_50V_X7R_0402

45 VBUS_EN — I2C_EN/GPIO10

I2C1_IRQ# — I2C_INT/GPIO9

REPETER_SDA_L RT17 1 2 0_0402_5% REPETER_SDA_R — I2C_SDA/GPIO8

REPETER_SCL_L RT18 1 2 0_0402_5% REPETER_SCL_R — I2C_SCL/GPIO7

LOC_PWR_MON — LOC_PWR_MON

45 TYPE_C_OCP# — IMON_MGPIO8

VMON — VMON_MGPIO9

RTS5457T-GR

SM_INT/GPIO4
SM_SDA/GPIO6
SM_SCL/GPIO5
REXT
DB_CFG
HPD/GPIO3
E-PAD

INT#_TYPEC_R — RT58 1 @ 2 0_0402_5% — RTS5457_SM_INT — RTS5457_SM_INT 14,52

SM_SDA_R — RT2151 @ 2 0_0402_5% — SM_SDA

SM_CK_R — RT2161 @ 2 0_0402_5% — SM_CK

RT59 1 2 1/16W_6.2K_1%_0402

RT60 1 2 0_0402_5%

RT60 for dead battery
Stuff: disable
unStuff: Enable

TYPE-C_DP_RE_HPD — TYPE-C_DP_RE_HPD 44

RTS5457T-GR_QFN24_4X4

follow stone request
08/21

+3VS_RE1 — RT984 0_0402_5%

44 REPETER_SDA — QT4A 2N7002KDWH_SOT363-6 — REPETER_SDA_L

44 REPETER_SCL — QT4B 2N7002KDWH_SOT363-6 — REPETER_SCL_L

+3VALW

INT#_TYPEC_R — RT978 4.7K_0402_5%

SM_CK — RT977 4.7K_0402_5%

SM_SDA — RT979 4.7K_0402_5%

+LDO_3V3

I2C1_IRQ# — RT980 4.7K_0402_5%

REPETER_SDA_L — RT981 4.7K_0402_5%

REPETER_SCL_L — RT982 4.7K_0402_5%

RTS5457_SM_INT — RT983 4.7K_0402_5%

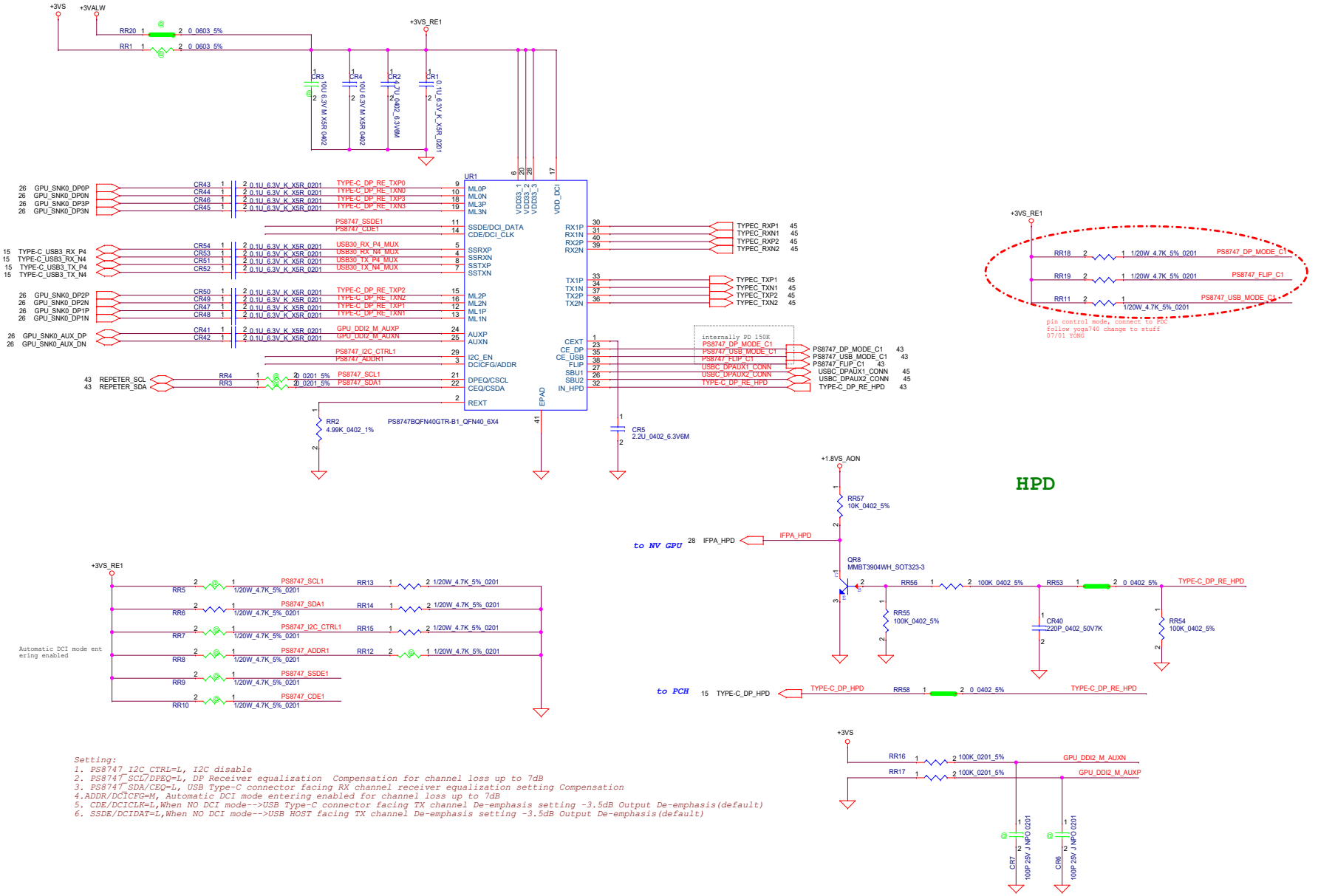
Modify by Yong808/21

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: USB TYPE-C Controller

Size: Custom | Document Number: Y550 | Rev: 1.0

Date: Monday, January 20, 2020 | Sheet 43 of 83



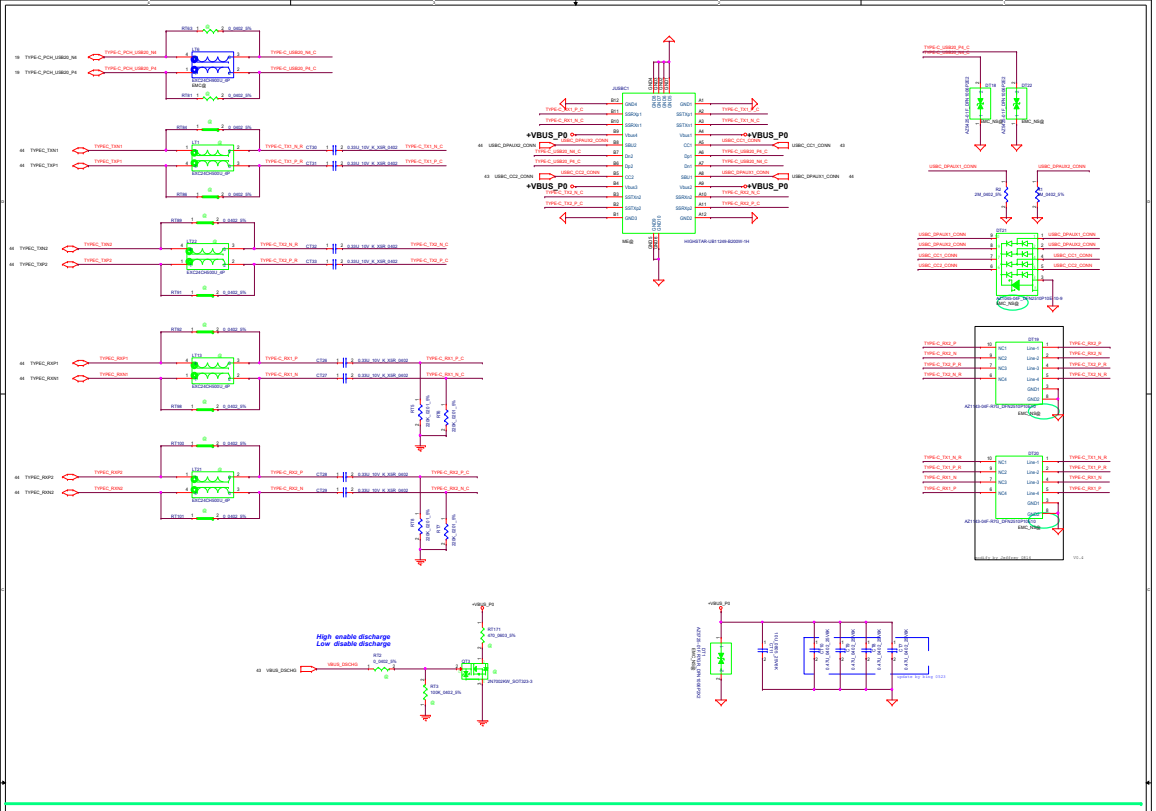
Setting:
1. PS8747_I2C_CTRL=L, I2C disable
2. PS8747_SCL/DPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB
3. PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation
4.ADDR/DCICFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB
5. CDE/DCICLK=L,When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)
6. SSDE/DCIDAT=L,When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *DDI Redriver PS8330*

Size	Document Number	Rev
C	*Y550*	1.0

Date: Tuesday, January 14, 2020 | Sheet 44 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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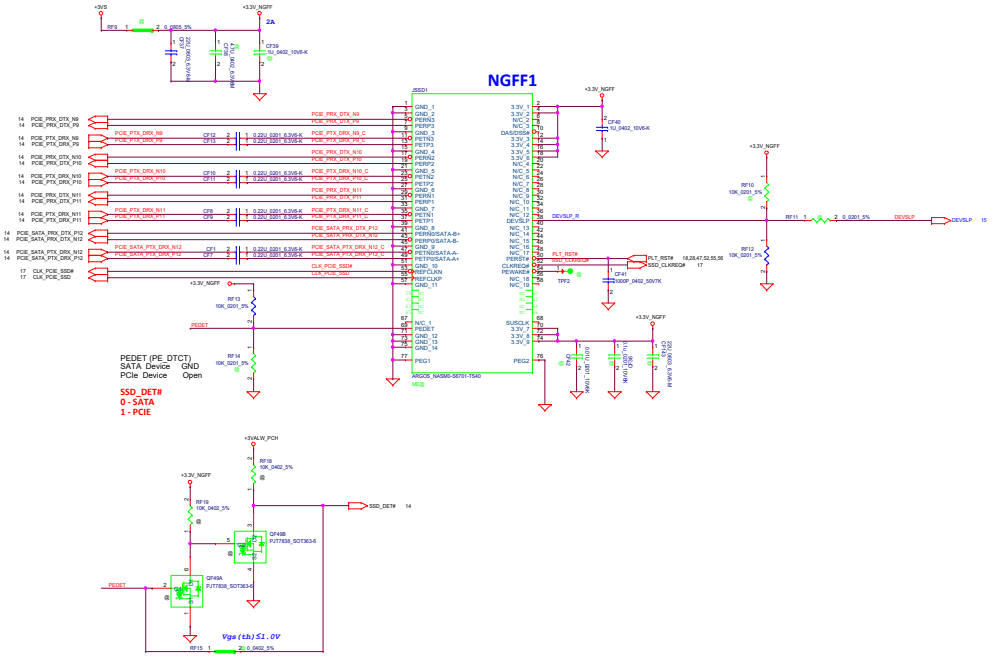
Title: USB TYPE-C Port

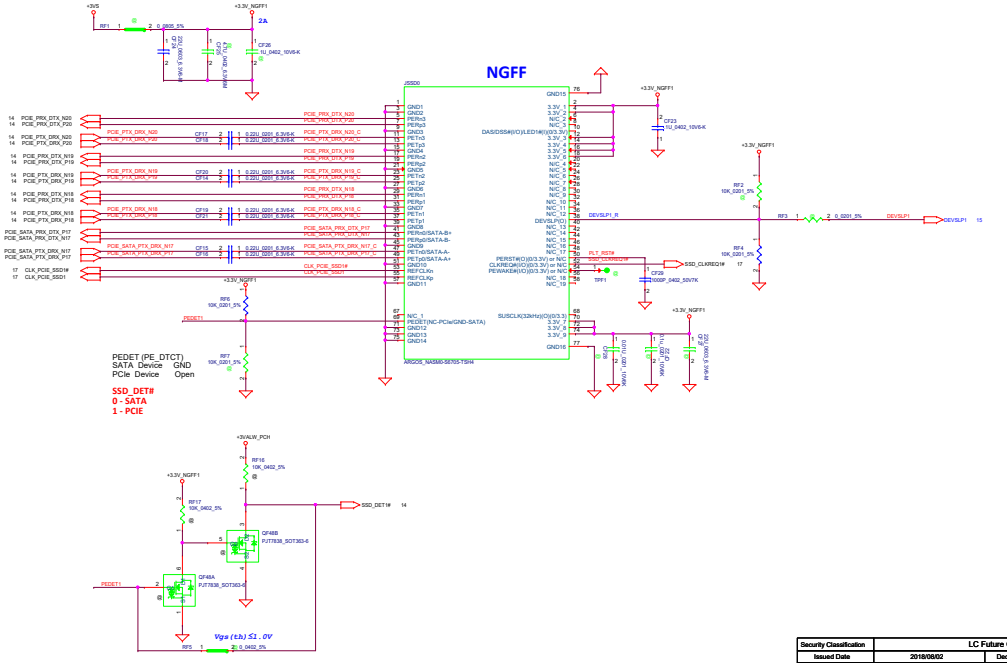
Size: B | Document Number: Y550 | Rev: 1.0

Date: Friday, January 11, 2019 | Sheet 46 of 53

M.2 SSD(SATA/PCIE)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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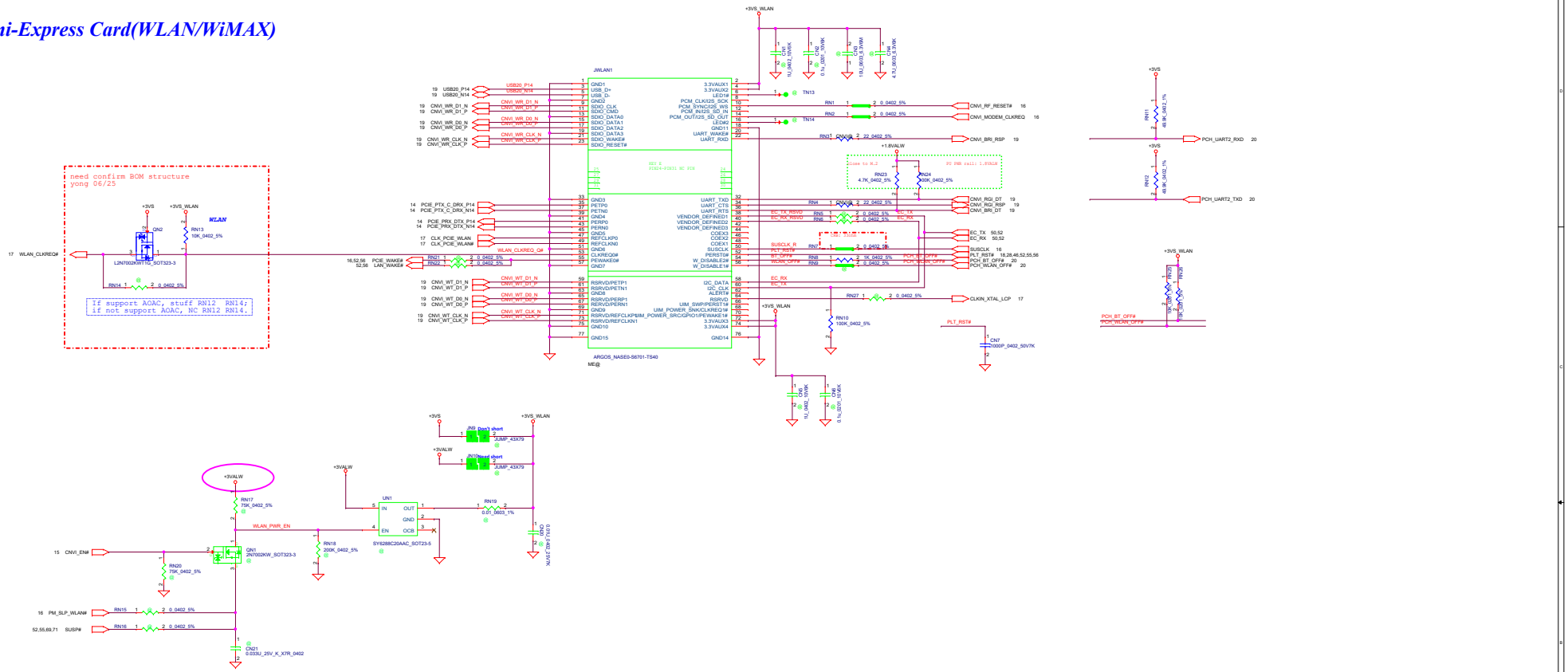
Title	NGFF WLAN	LCFC
Size	Document Number	Rev
Date	Y550	1.0
Date: Wednesday, January 15, 2020	Sheet 46 of 53	

Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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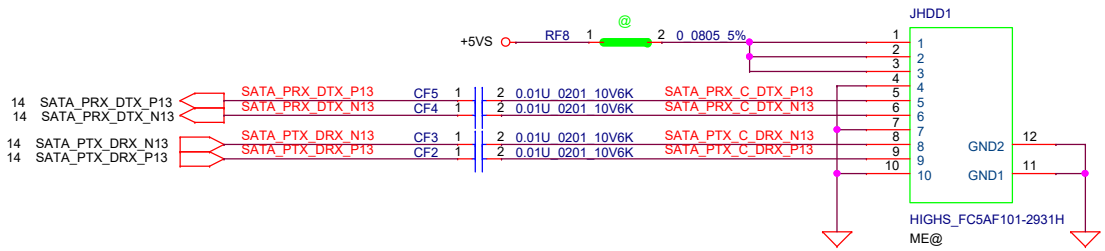
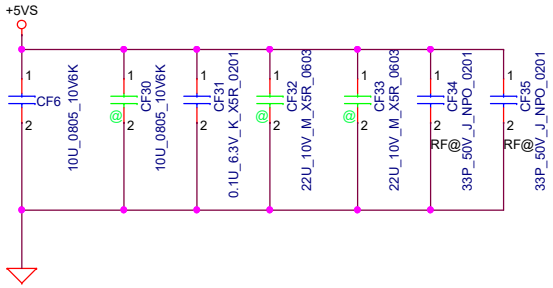
Title	CNVI		
Size D	Document Number ¥550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 47 of 83		

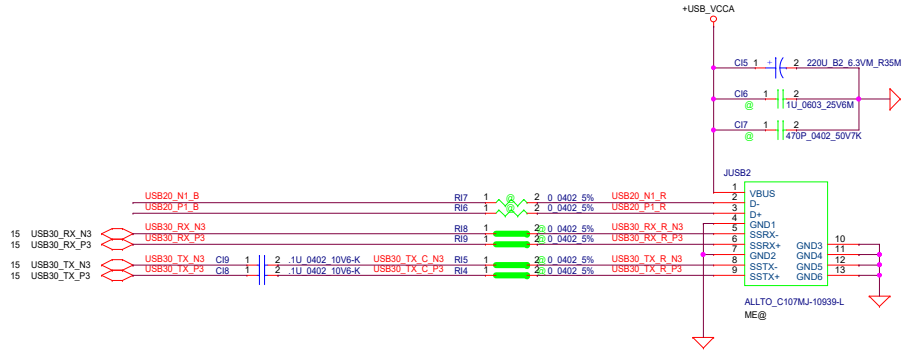
SATA HDD Conn.

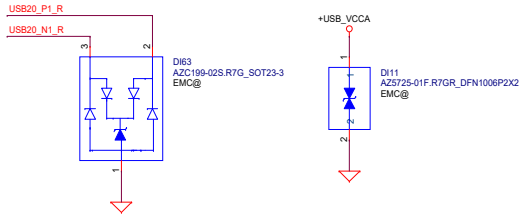


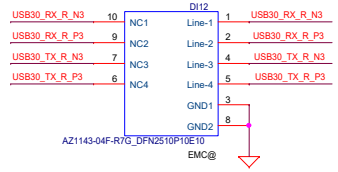


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

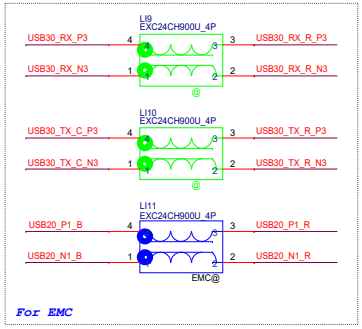
Title	HDD/XBOX CONN		
Size B	Document Number Y550		Rev 1.0
Date:	Wednesday, January 15, 2020	Sheet 48 of 83	





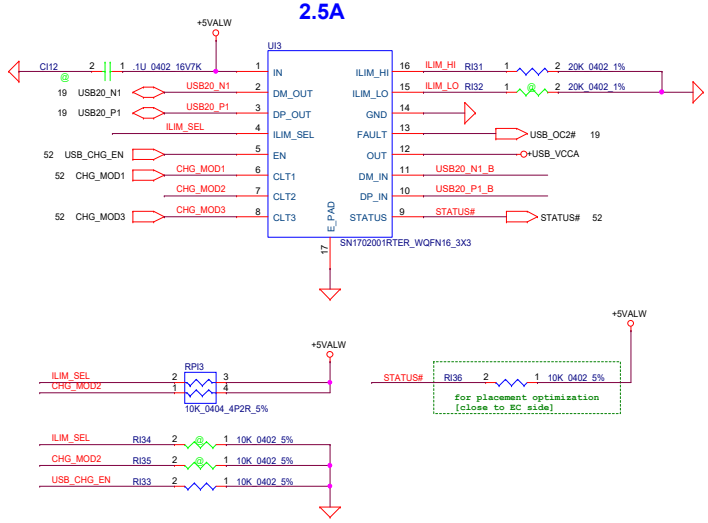


For EMC



For EMC

USB charger
2.5A



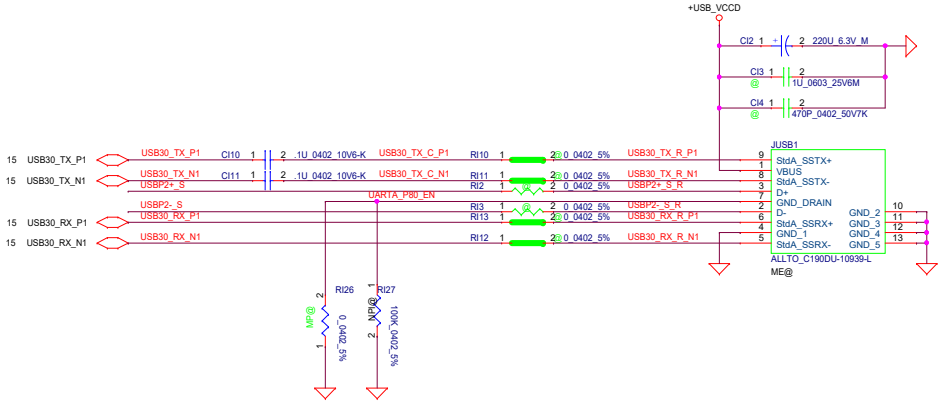
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

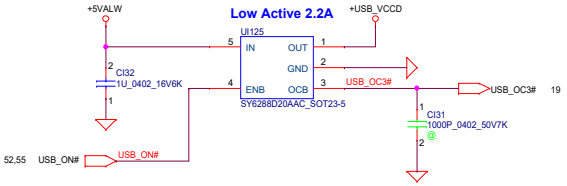
Title: **USB2.0/USB3.0 PORT (LEFT)**

Size	Document Number	Rev
C	¥550	1.0

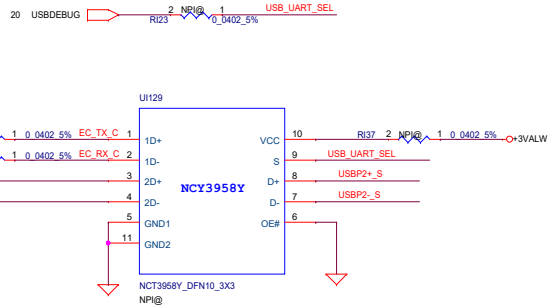
Date: Tuesday, January 14, 2020 | Sheet 49 of 83

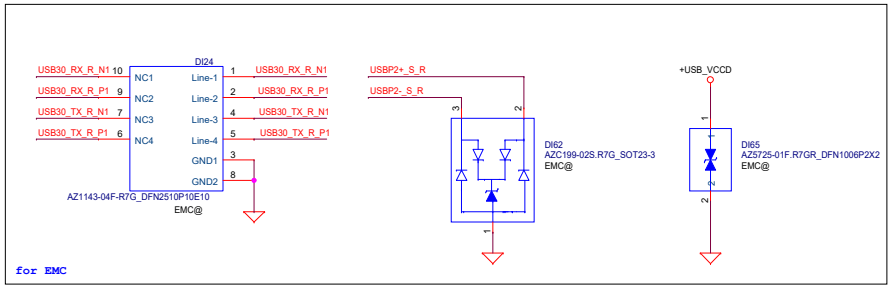


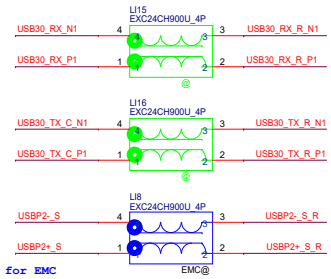
USB3.1 PORT x2



For USB Debug Function



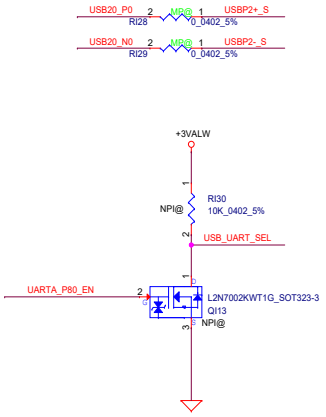




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

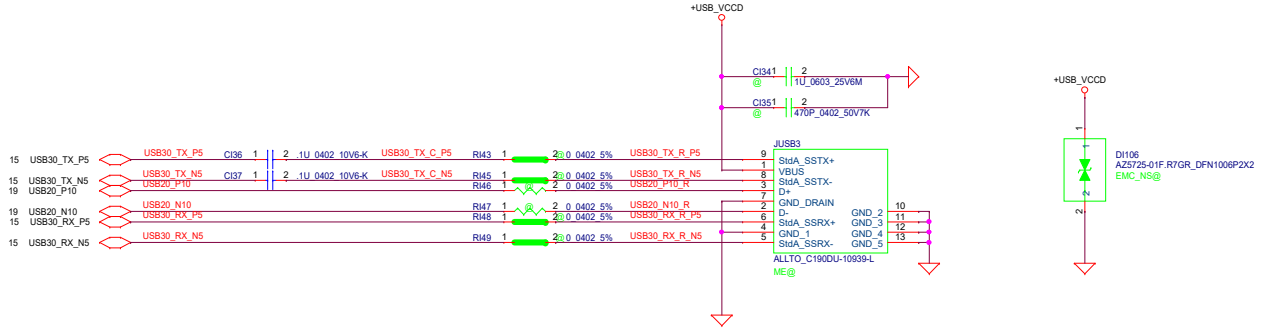


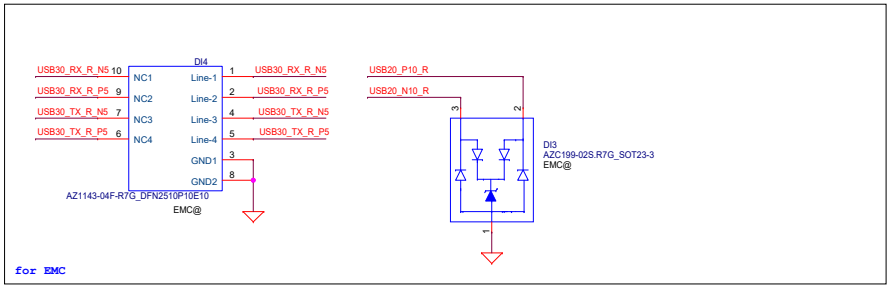
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

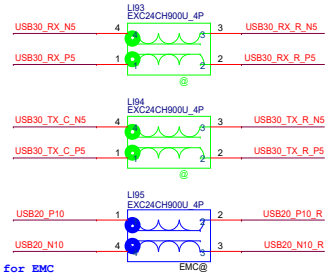
Title: **USB2.0**

Size	Document Number	Rev
C	Y550	1.0

Date: Tuesday, January 14, 2020 Sheet 50 of 83





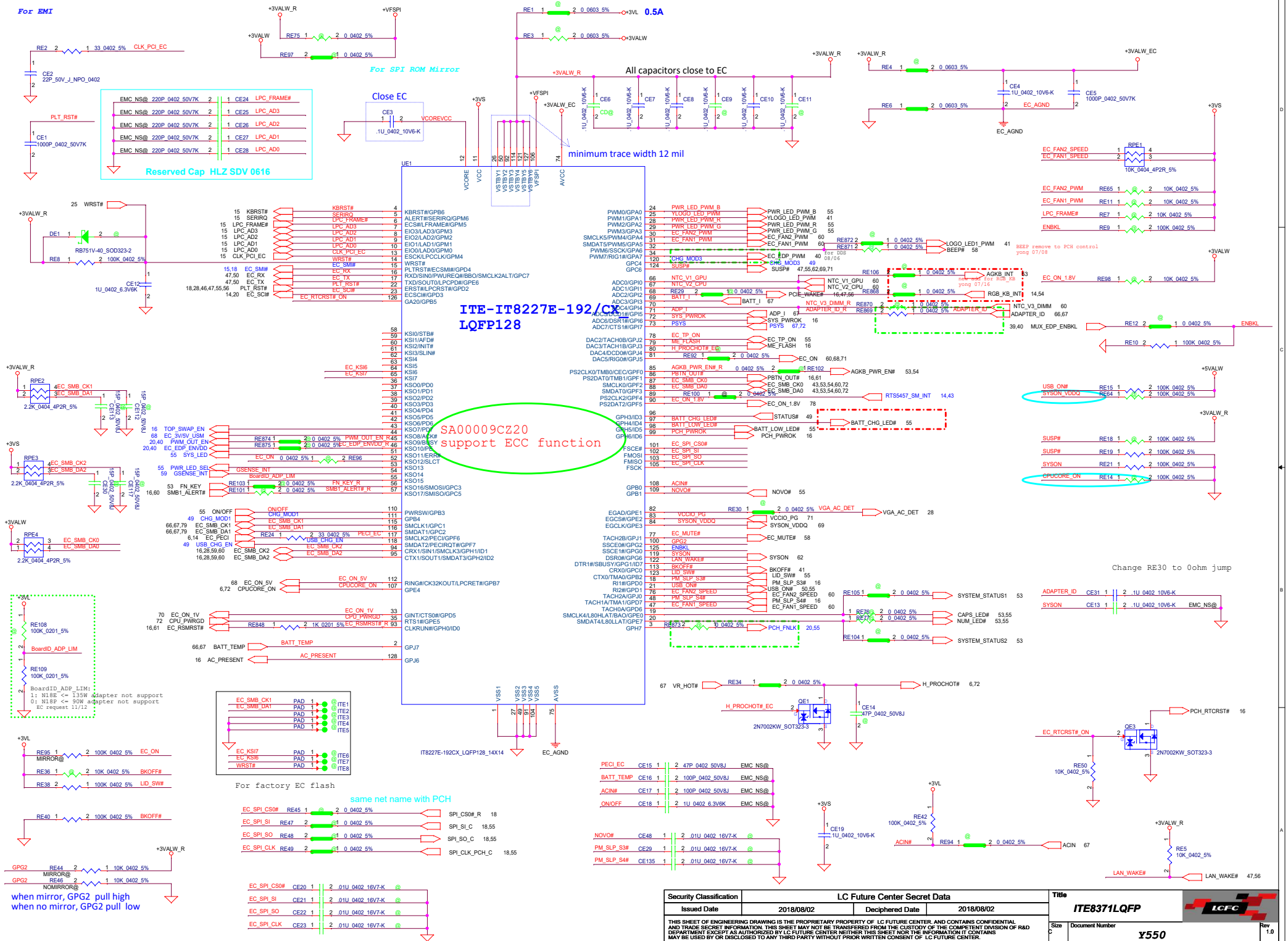


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB2.0**

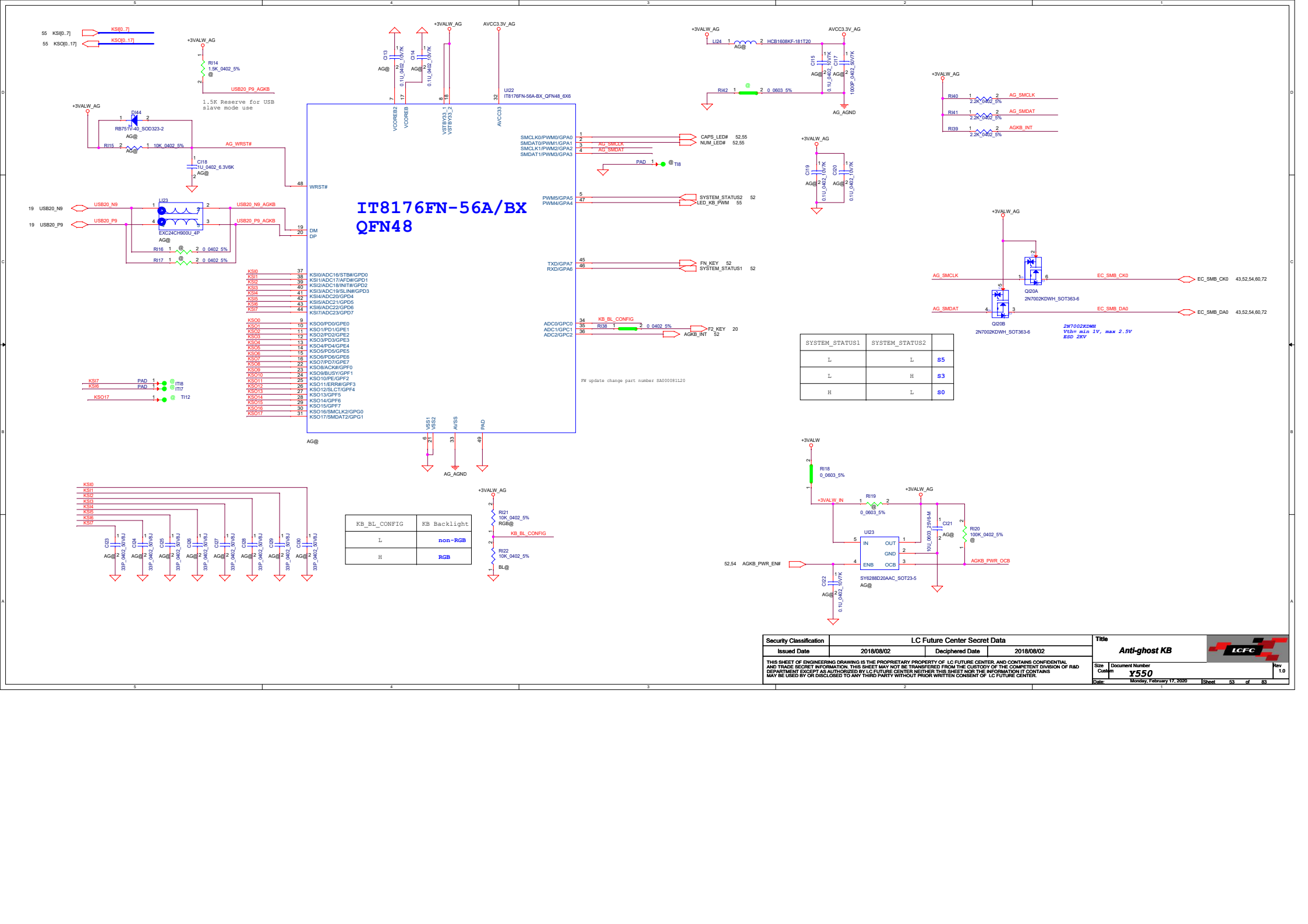
Size	Document Number	Rev
C	Y550	1.0

Date: Tuesday, January 14, 2020 Sheet 51 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	ITE8371LQFP		
Size	Document Number		Rev
C	Y550		1.0
Date:	Wednesday, January 15, 2020	Sheet	52 of 83


IT8176FN-56A/BX
QFN48
1.5K Reserve for USB slave mode use
FW update change part number SA000081L20
2N7002KDWH Vth= min 1V, max 2.5V ESD 2KV
SY8288D20AAC_SOT23-5
EXC24CH900U_4P
RB751V-40_SOD323-2
2N7002KDWH_SOT363-6
SYSTEM_STATUS1 | SYSTEM_STATUS2 |
L | L | S5
L | H | S3
H | L | S0
KB_BL_CONFIG | KB Backlight
L | non-RGB
H | RGB
Security Classification | LC Future Center Secret Data
Issued Date | 2018/08/02 | Deciphered Date | 2018/08/02
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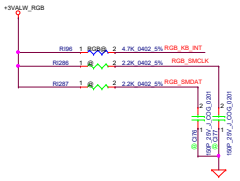
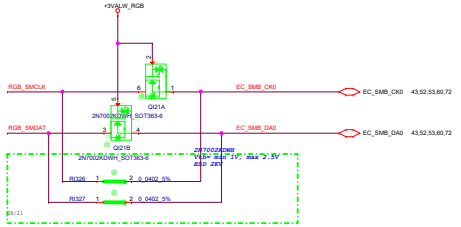
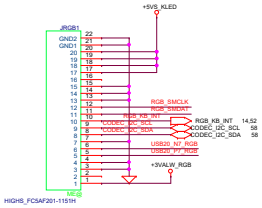
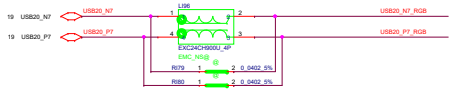
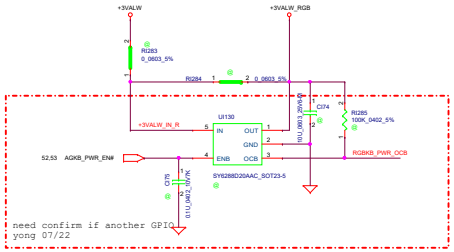
Title: Anti-ghost KB
Size: Custom | Document Number: Y550 | Rev: 1.0
Date: Monday, February 17, 2020 | Sheet 53 of 83











Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	RGB KB		
Size D	Document Number		Rev 1.0
	Y550		
Date: Monday, January 20, 2020	Sheet 54 of 83		

ON/OFF switch

No function field

Charger LED

K/B Connector

PWR LED

TP/B Connector

USB3.1 PORT x1

Low Active 1.8A

system LED

MIC board

17" Power DB Conn del LID yong 0619

for 15" USB board

for 17" USB board

modify by david 24/26

need confirm pin 1 yong 07/22

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title: KBD/PWR/IO/LED/TP Conn.

Size: D | Document Number: ¥550 | Rev: 1.0

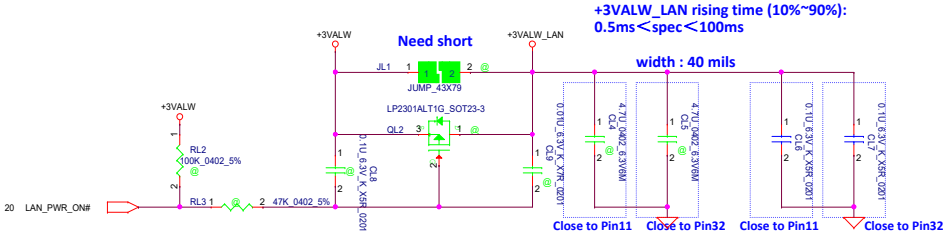
Date: Tuesday, March 03, 2020 | Sheet 55 of 85

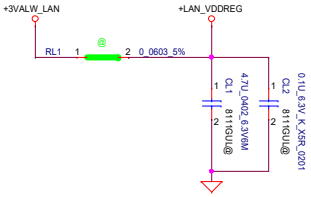
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

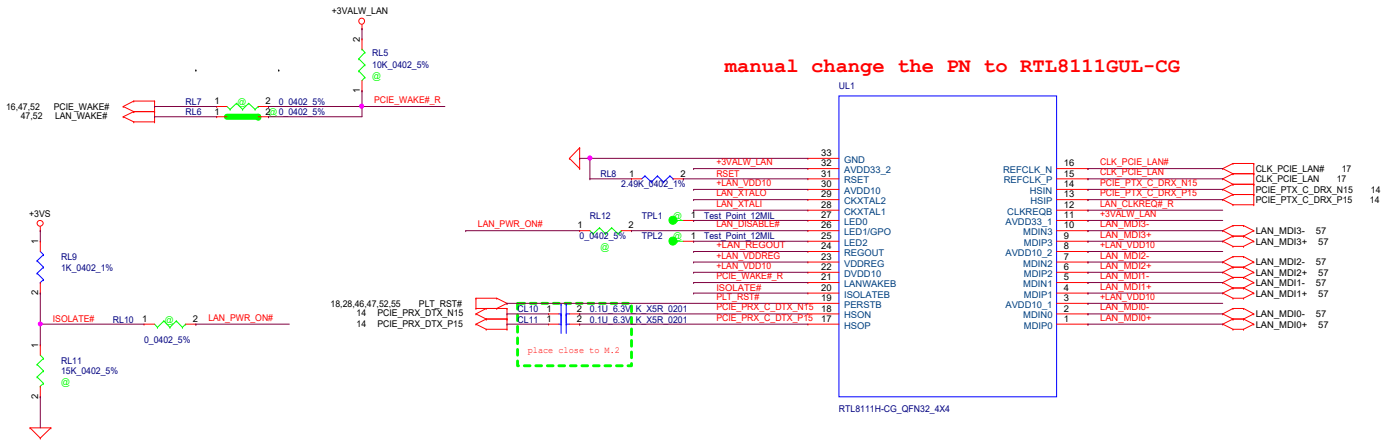
Need short

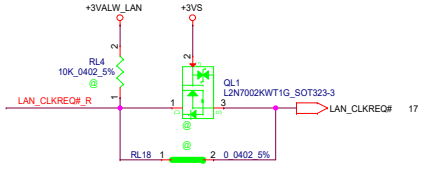
width : 40 mils



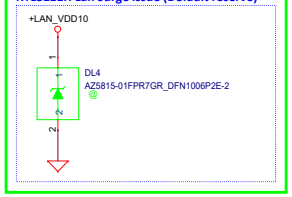


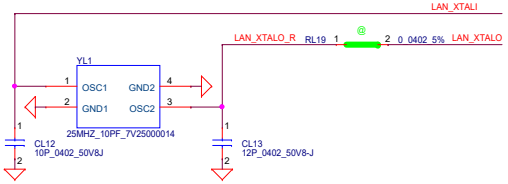
manual change the PN to RTL8111GUL-CG



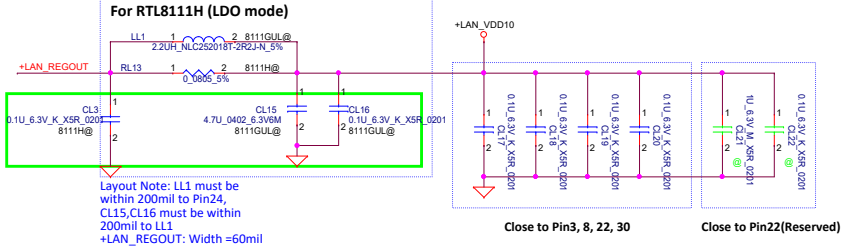


2018/01/24: add AZ5815-01F.R7GR for RTL8111H Lan Surge issue (Default reserve)





For RTL8111GUL(SWR mode)
For RTL8111H (LDO mode)



Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

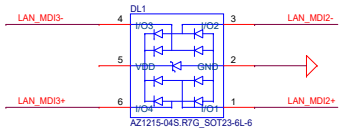
Close to Pin3, 8, 22, 30

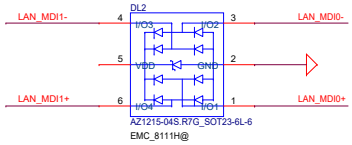
Close to Pin22(Reserved)

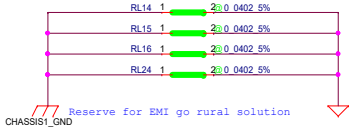
Security Classification	LC Future Center Secret Data		
Issued Date	2019/02/13	Deciphered Date	2019/02/13

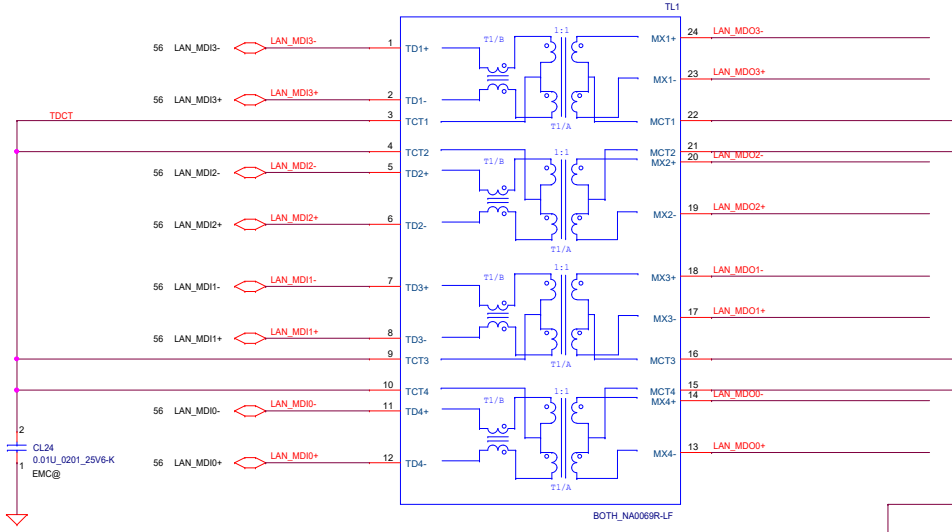
Title	LAN_RTL8111GUL_H		
Size	Document Number		Rev
C	¥550		1.0
Date:	Tuesday, January 14, 2020	Sheet	56 of 83

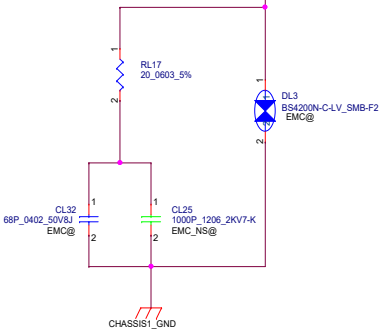
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

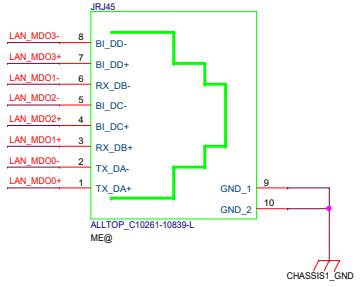






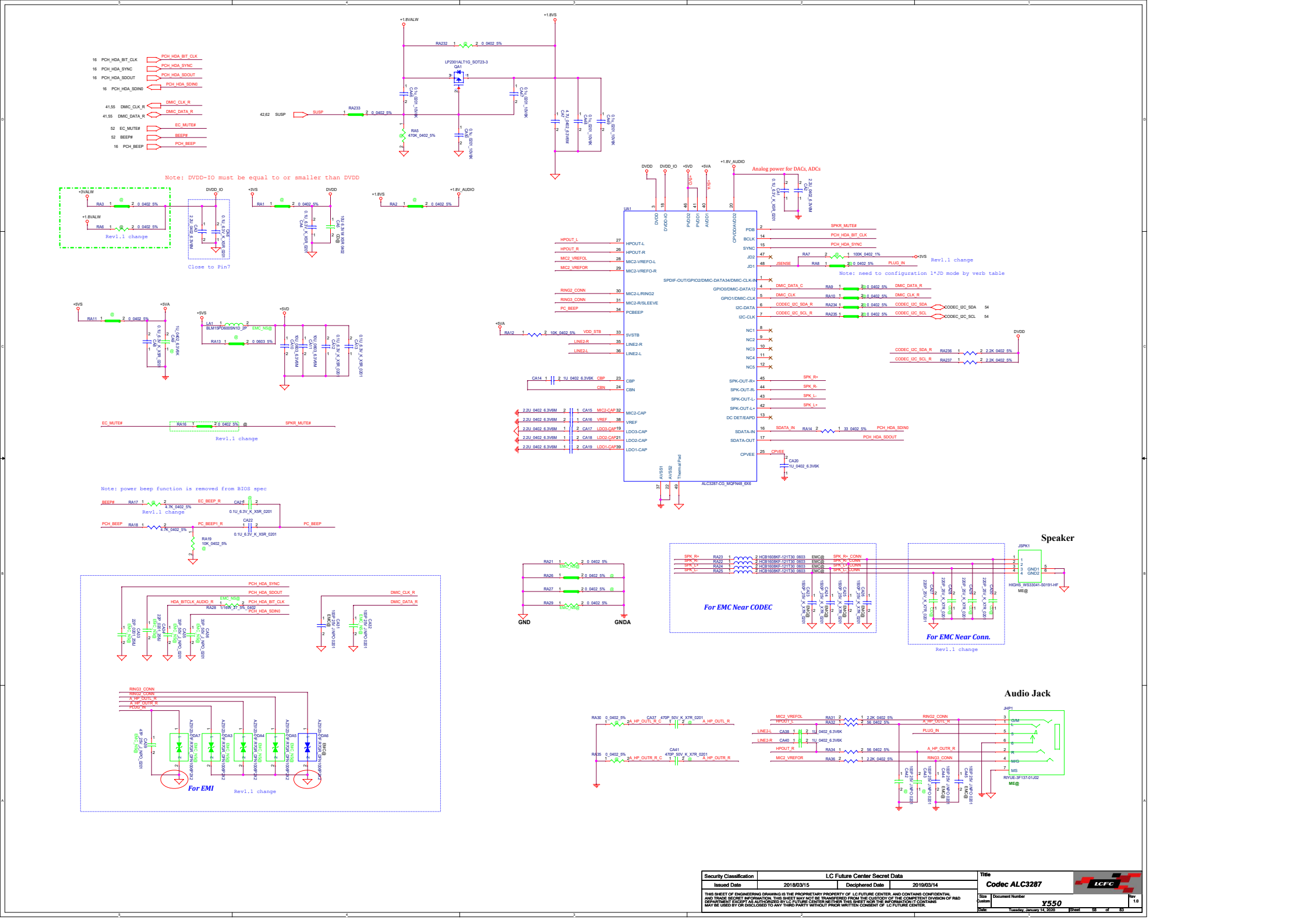






Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	LAN_Transformer		
Size	Document Number		Rev
C	Y550		1.0
Date:	Tuesday, January 14, 2020	Sheet	57 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/03/15	Deciphered Date	2019/03/14

Title	Codec ALC3287		
Size: Custom	Document Number: Y550		Rev: 1.0
Date: Tuesday, January 14, 2020	Sheet 58 of 83		

APS G-Sensor

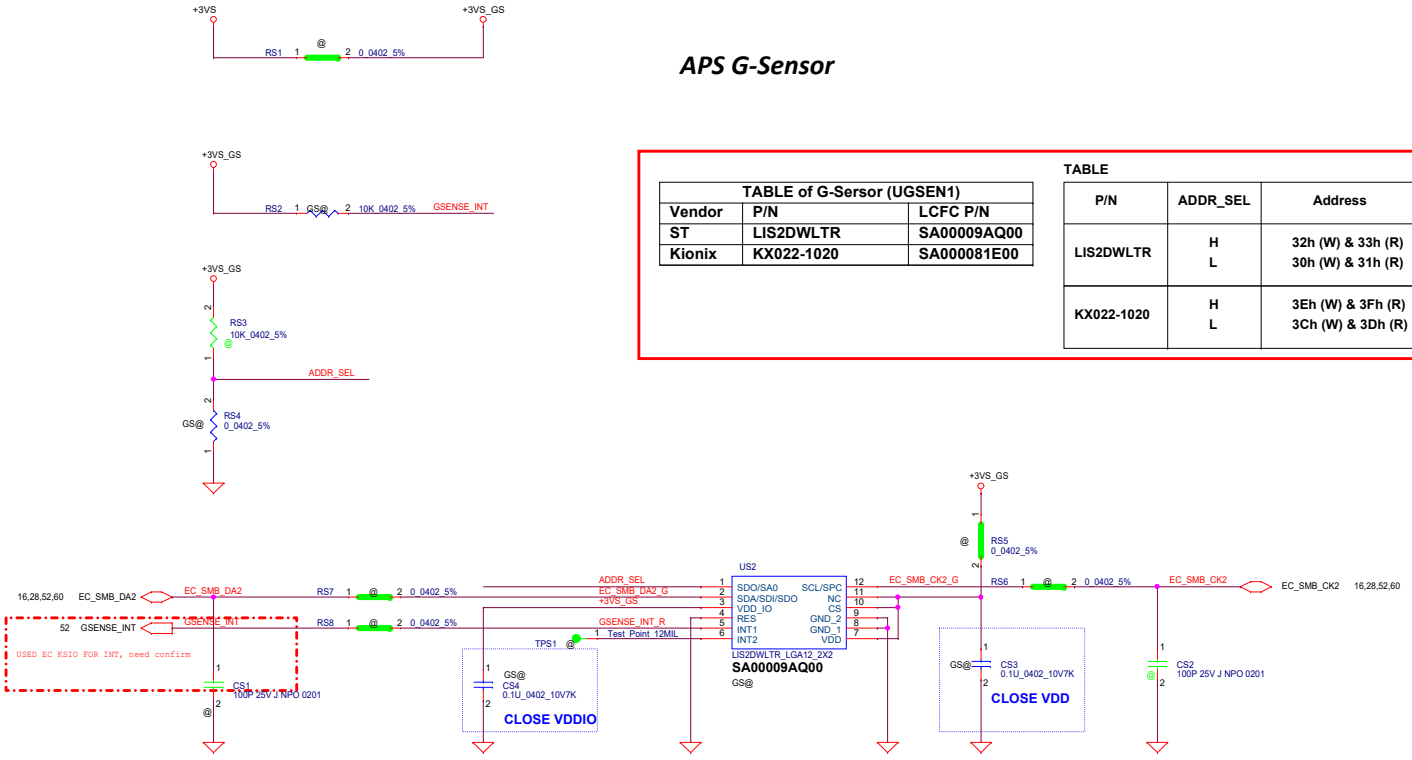


TABLE of G-Sersor (UGSEN1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00

TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

Title: USB2.0

Size	Document Number	Rev
C	Y550	1.0

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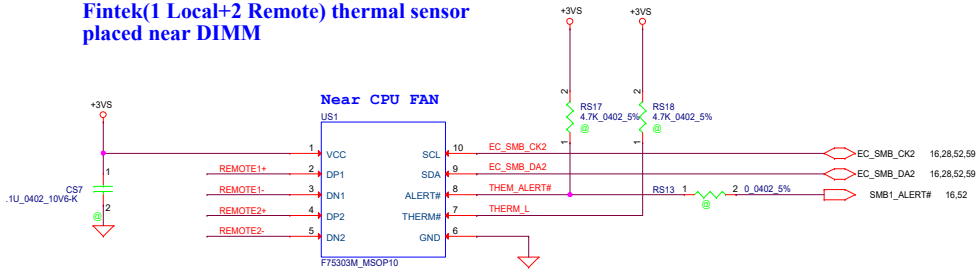
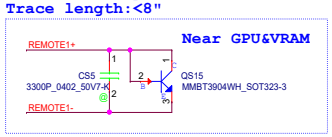
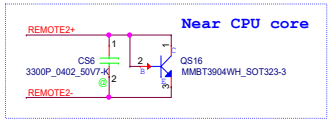
Fintek(1 Local+2 Remote) thermal sensor placed near DIMM

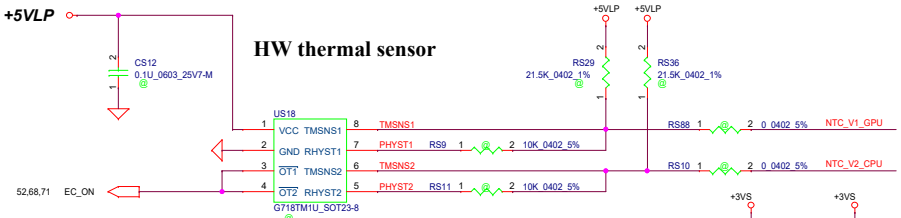


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

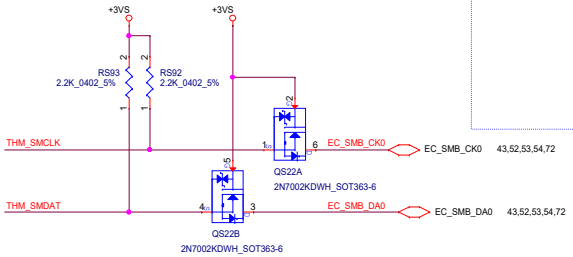


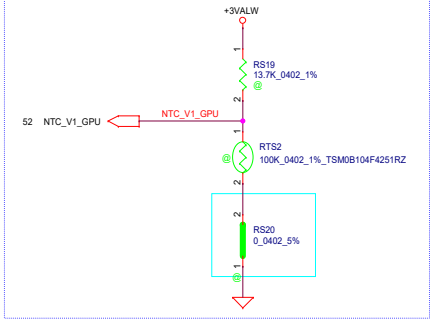


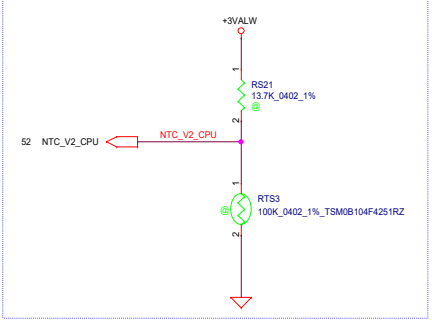
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

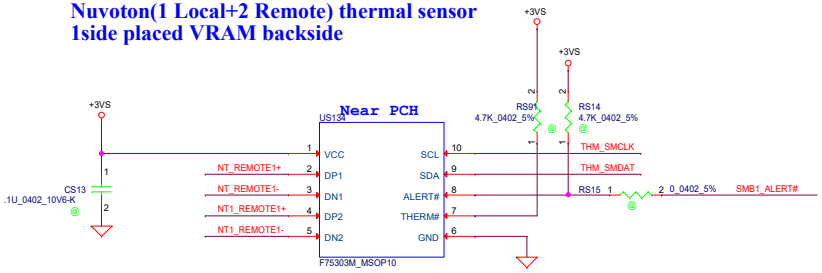


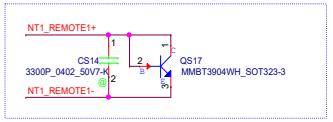


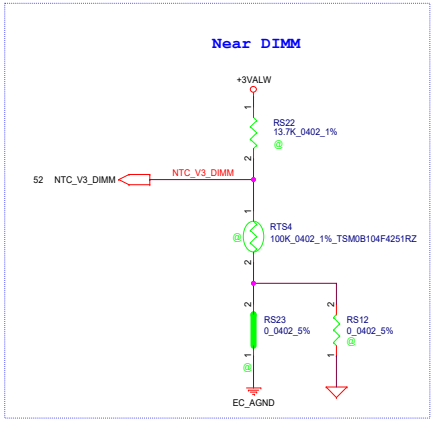


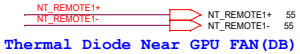
for layout optimized, change the EC_AGND to GND

Nuvoton(1 Local+2 Remote) thermal sensor 1side placed VRAM backside







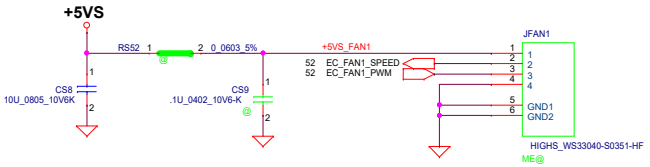


Thermal Diode Near GPU FAN(DB)

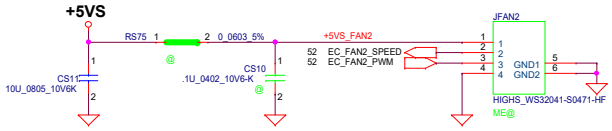
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb

FAN Conn Right



FAN Conn LEFT



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Thermal sensor/FAN CONN		
Size C	Document Number Y550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 60 of 83		

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

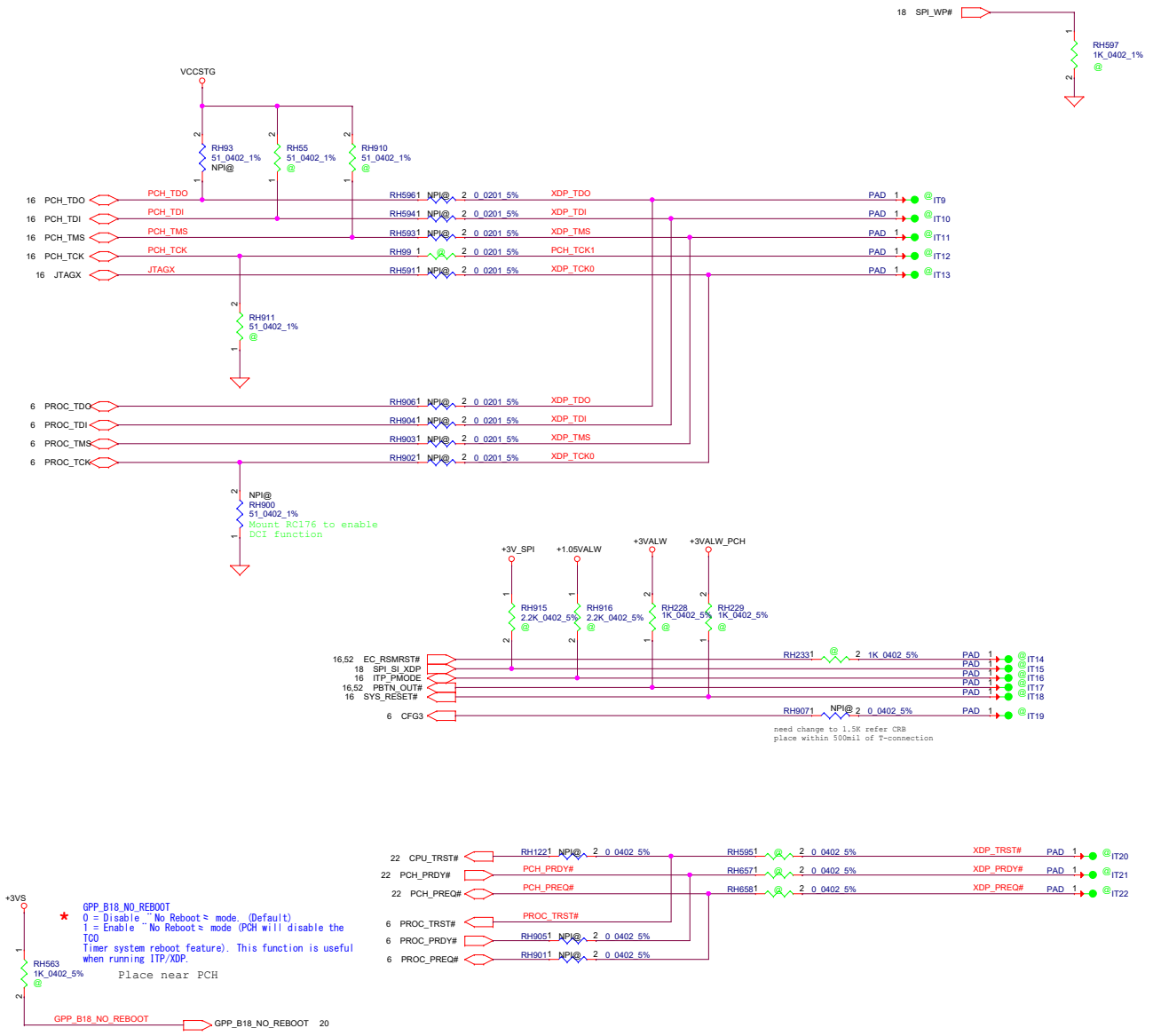
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



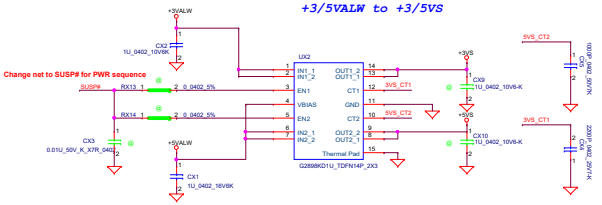
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

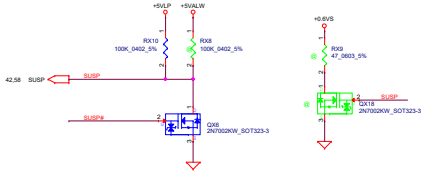
Title: XDP

Size: Custom | Document Number: Y550 | Rev: 1.0

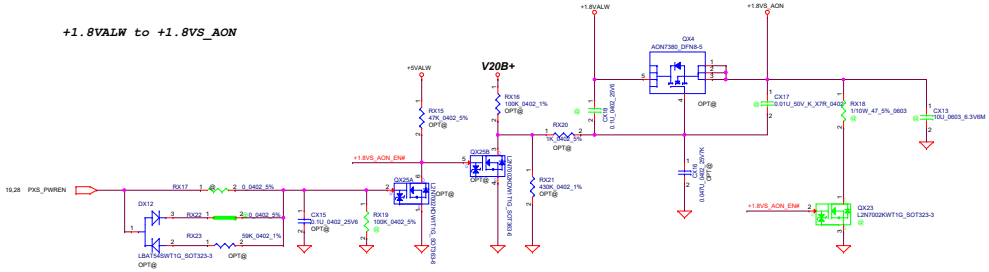
Date: Tuesday, January 14, 2020 | Sheet 61 of 83

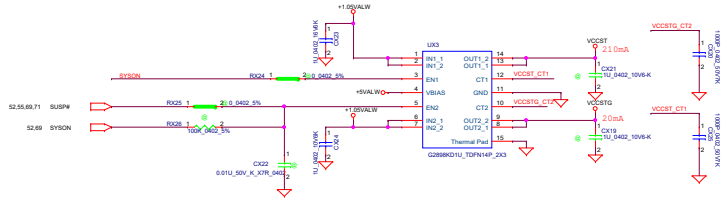
+3/5VALW to +3/5VS





+1.8VALW to +1.8VS_AON





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

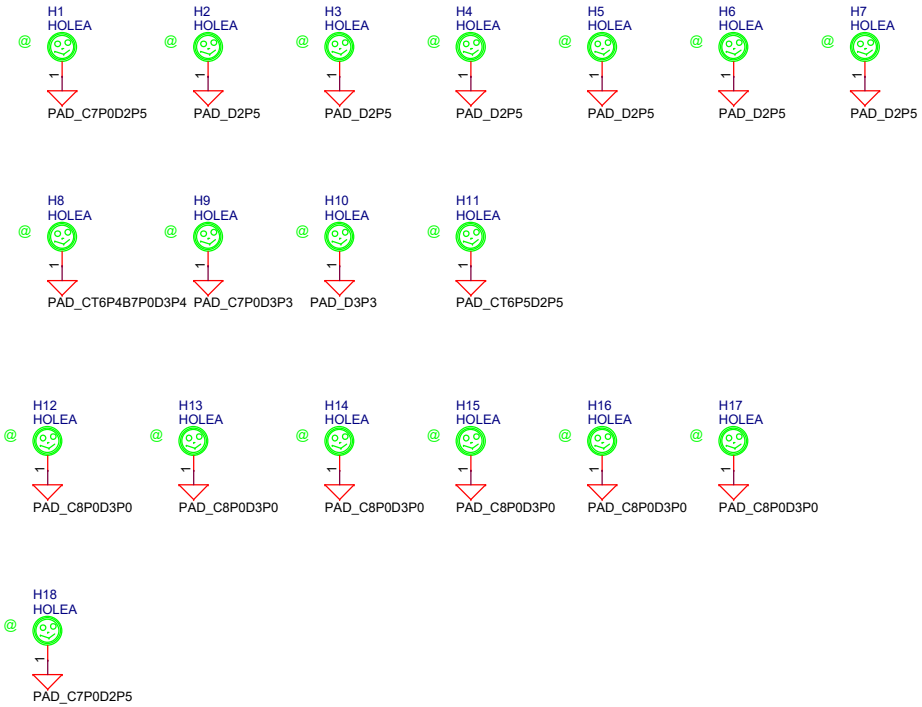
Title	DC V TO VS INTERFACE		
Size D	Document Number ¥550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 62 of 83		

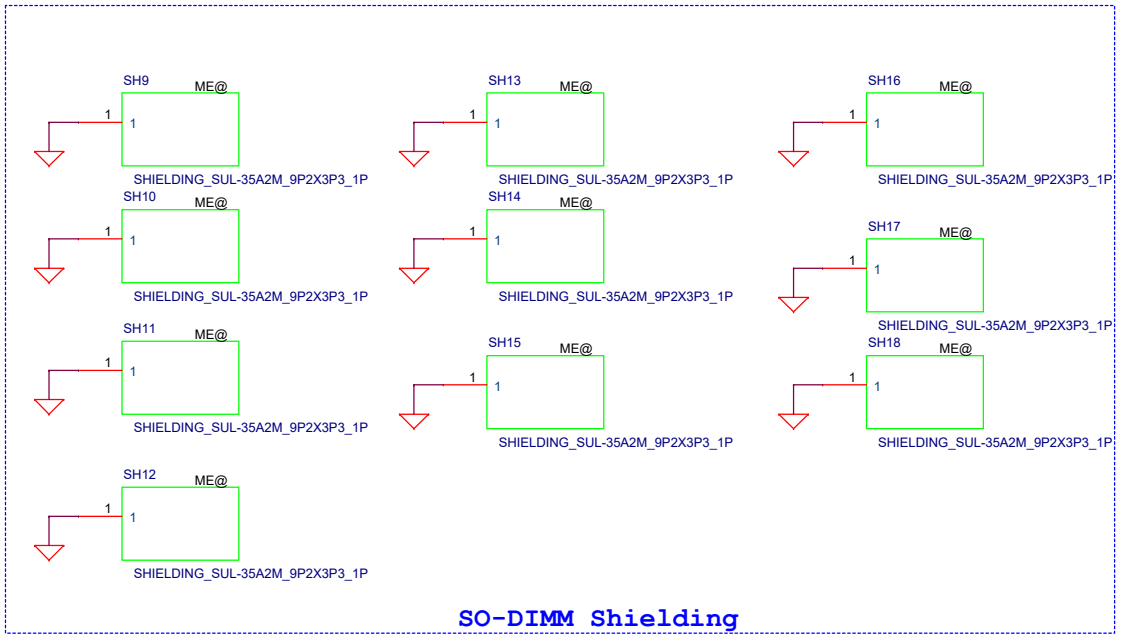
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

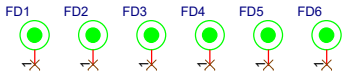
Title: *Virtual symbol*

Size	Document Number	Rev
C	¥550	0.1

Date: Friday, February 21, 2020 Sheet 63 of 83





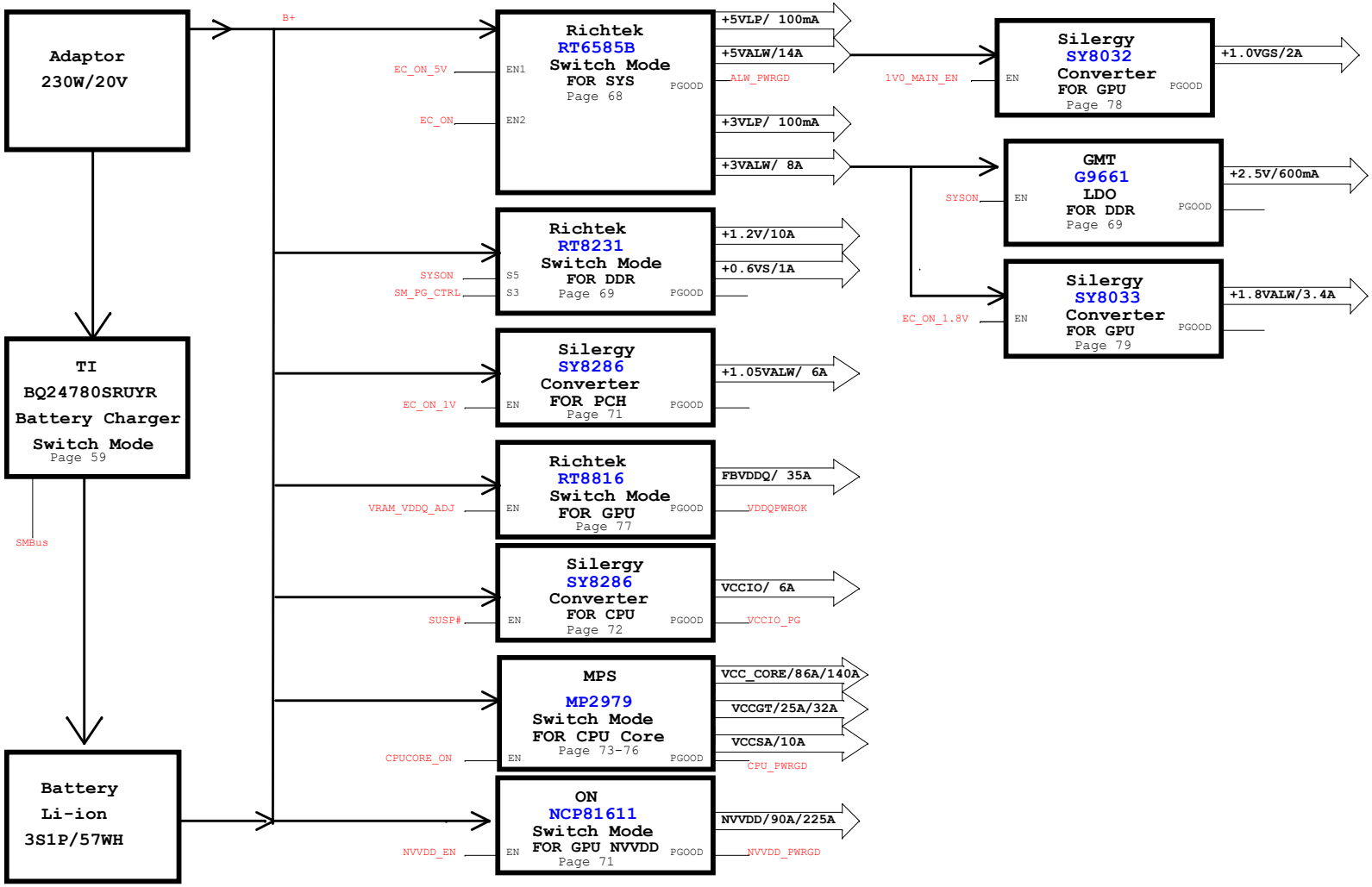


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Hole**

Size	Document Number	Rev
B	Y550	1.0

Date: Monday, February 10, 2020 Sheet 64 of 83

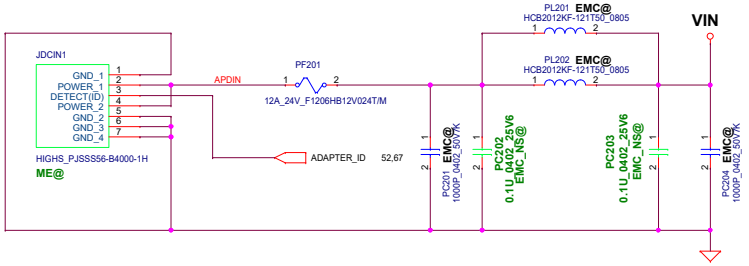


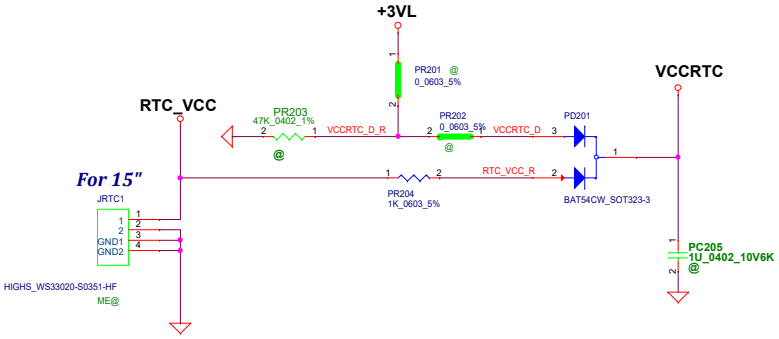
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

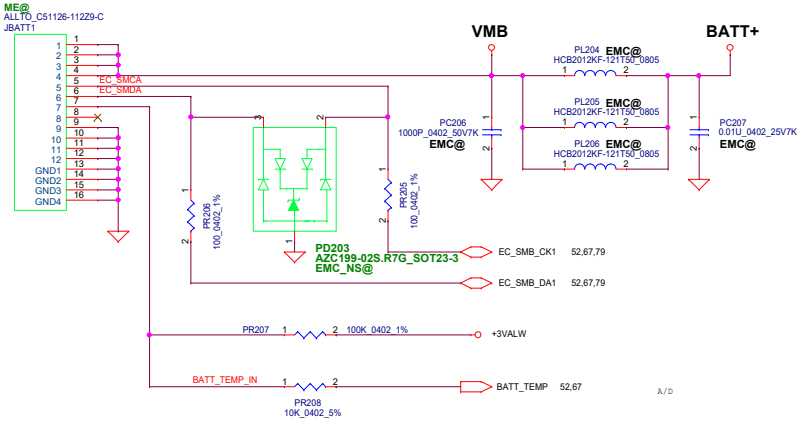
Title: **Power Diagram**

Size	Document Number	Rev
Custom	Y550	1.0

Date: Wednesday, February 19, 2020 Sheet 65 of 83

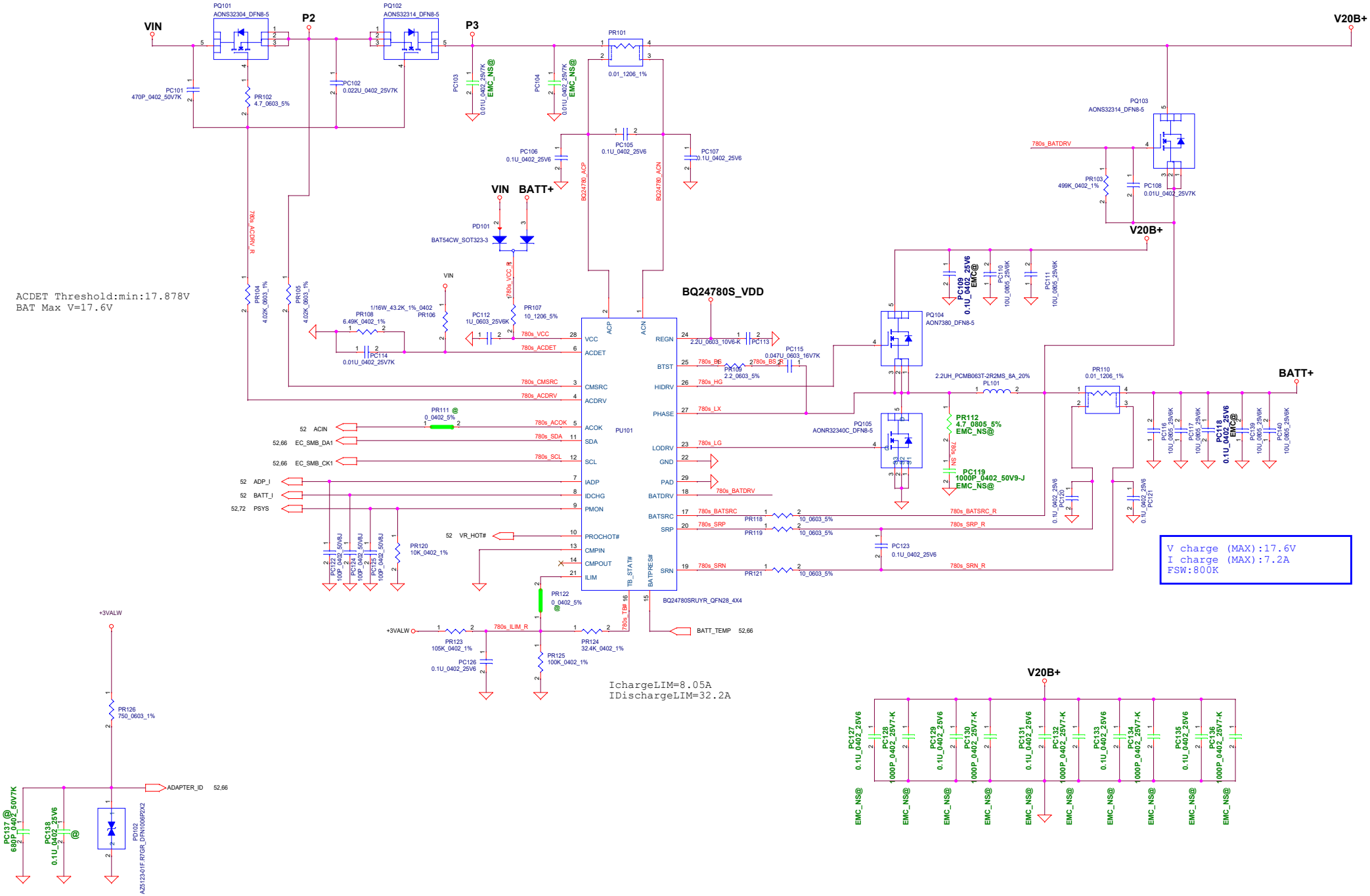






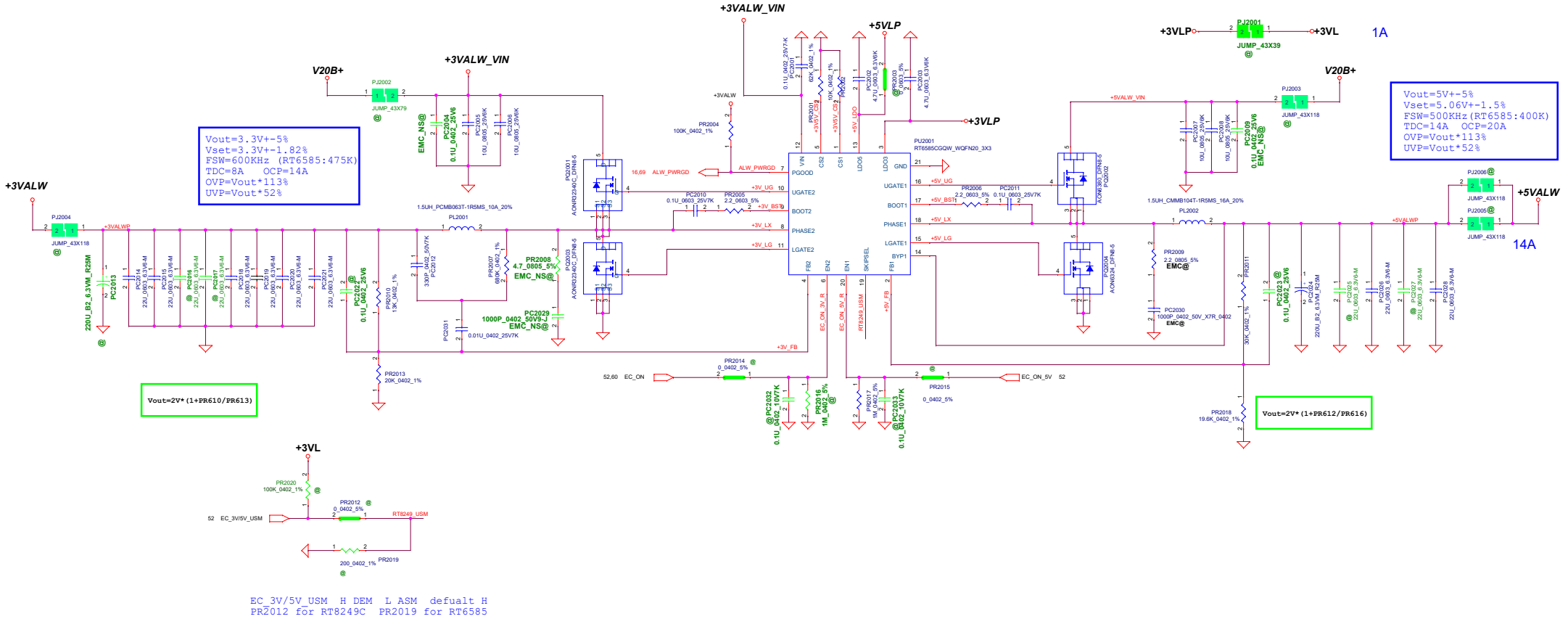
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN/BATT/RTC		
Size C	Document Number Y550		Rev 1.0
Date: Wednesday, February 19, 2020	Sheet 66 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-charger		
Size	Custom	Document Number	Y550
Rev	1.0		
Date:	Wednesday, February 19, 2020	Sheet	67 of 83


+3VALW_VIN
+5VLP
+3VLP
+3VL
1A
V20B+
+3VALW_VIN
Vout=3.3V+-5%
Vset=3.3V+-1.82%
FSW=600KHz (RT6585:475K)
TDC=8A OCP=14A
OVP=Vout*113%
UVP=Vout*52%
Vout=5V+-5%
Vset=5.06V+-1.5%
FSW=500KHz(RT6585:400K)
TDC=14A OCP=20A
OVP=Vout*113%
UVP=Vout*52%
+3VALW
+5VALW
14A
PU2001
RT6585CGQW_WQFN20_3X3
VIN
PGOOD
UGATE2
BOOT2
PHASE2
LGATE2
FB2
EN2
EN1
SKIPSEL
FB1
BYP1
LGATE1
PHASE1
BOOT1
UGATE1
GND
LDO3
LDO5
CS1
CS2
PL2001
1.5UH_PCMB063T-1R5MS_10A_20%
PL2002
1.5UH_CMMB104T-1R5MS_16A_20%
Vout=2V*(1+PR610/PR613)
Vout=2V*(1+PR612/PR616)
+3VL
EC_3V/5V_USM H DEM L ASM defualt H
PR2012 for RT8249C PR2019 for RT6585
Security Classification
LC Future Center Secret Data
Issued Date
2018/08/02
Deciphered Date
2018/08/02
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Title
PWR-3/5VALW
Size
Custom
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Y550
Rev
1.0
Date:
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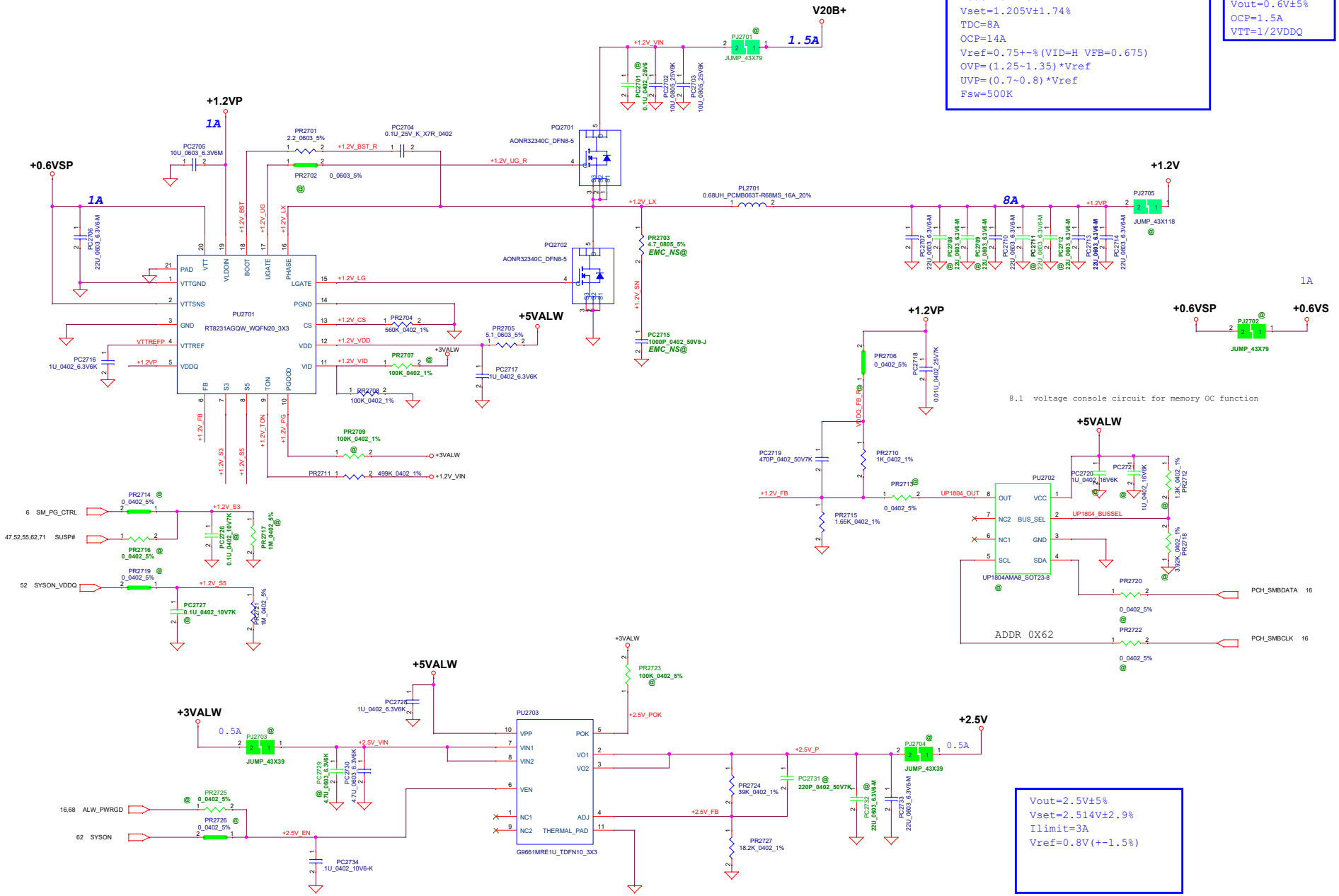


STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

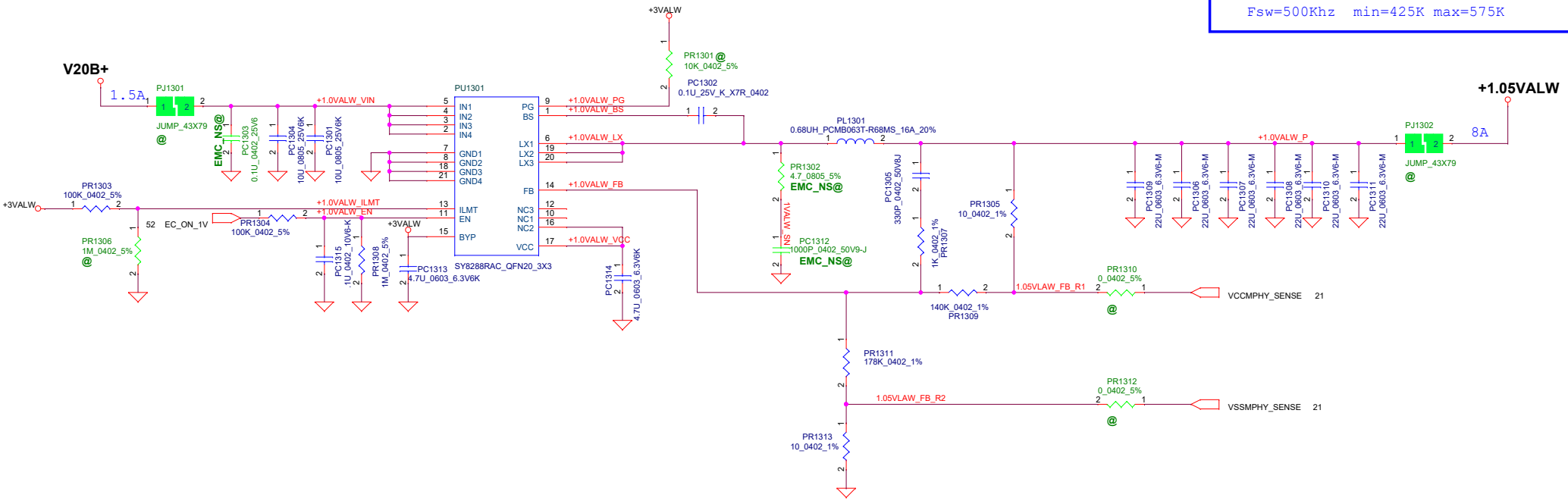
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VDDQ/VTT

Size: Custom | Document Number: Y550 | Rev: 1.0

Date: Wednesday, February 19, 2020 | Sheet 69 of 83

Vout=1.05V±5%
Vset=1.072V±1.87%
Vref=0.6V(+-1%)
TDC=8A
OCP=16A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K

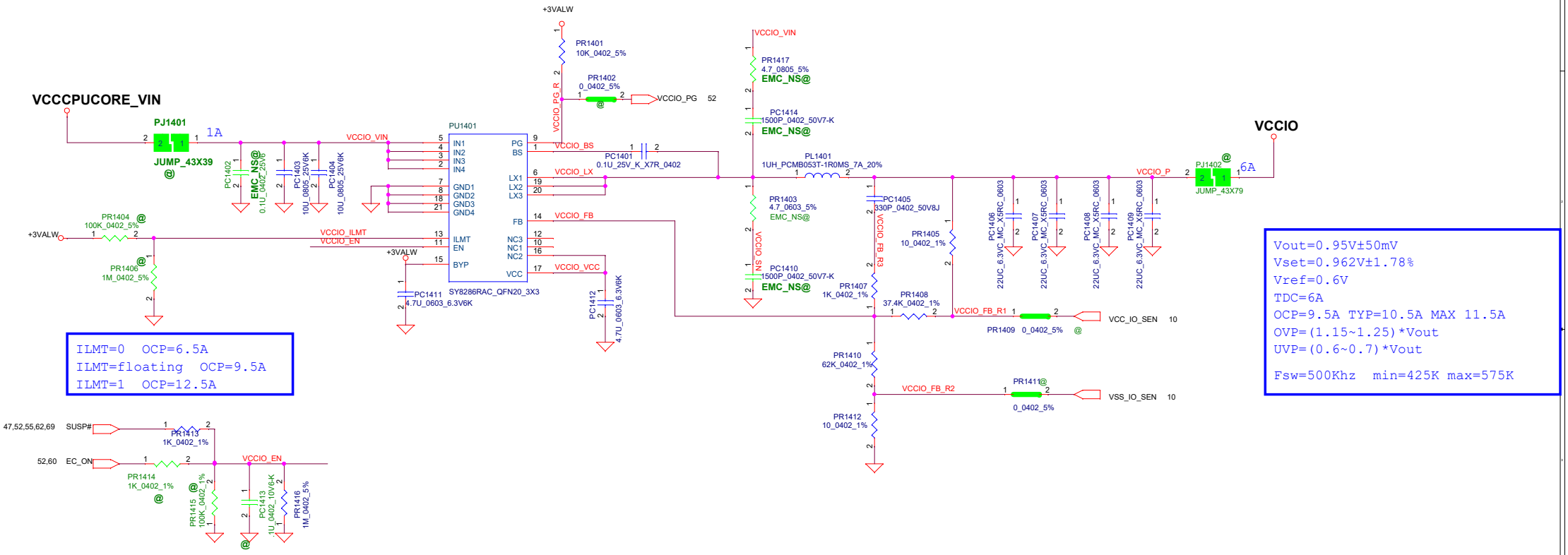


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.0VALW**

Size	Document Number	Rev
Custom	Y550	1.0

Date: Wednesday, February 19, 2020 Sheet 70 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCIO**

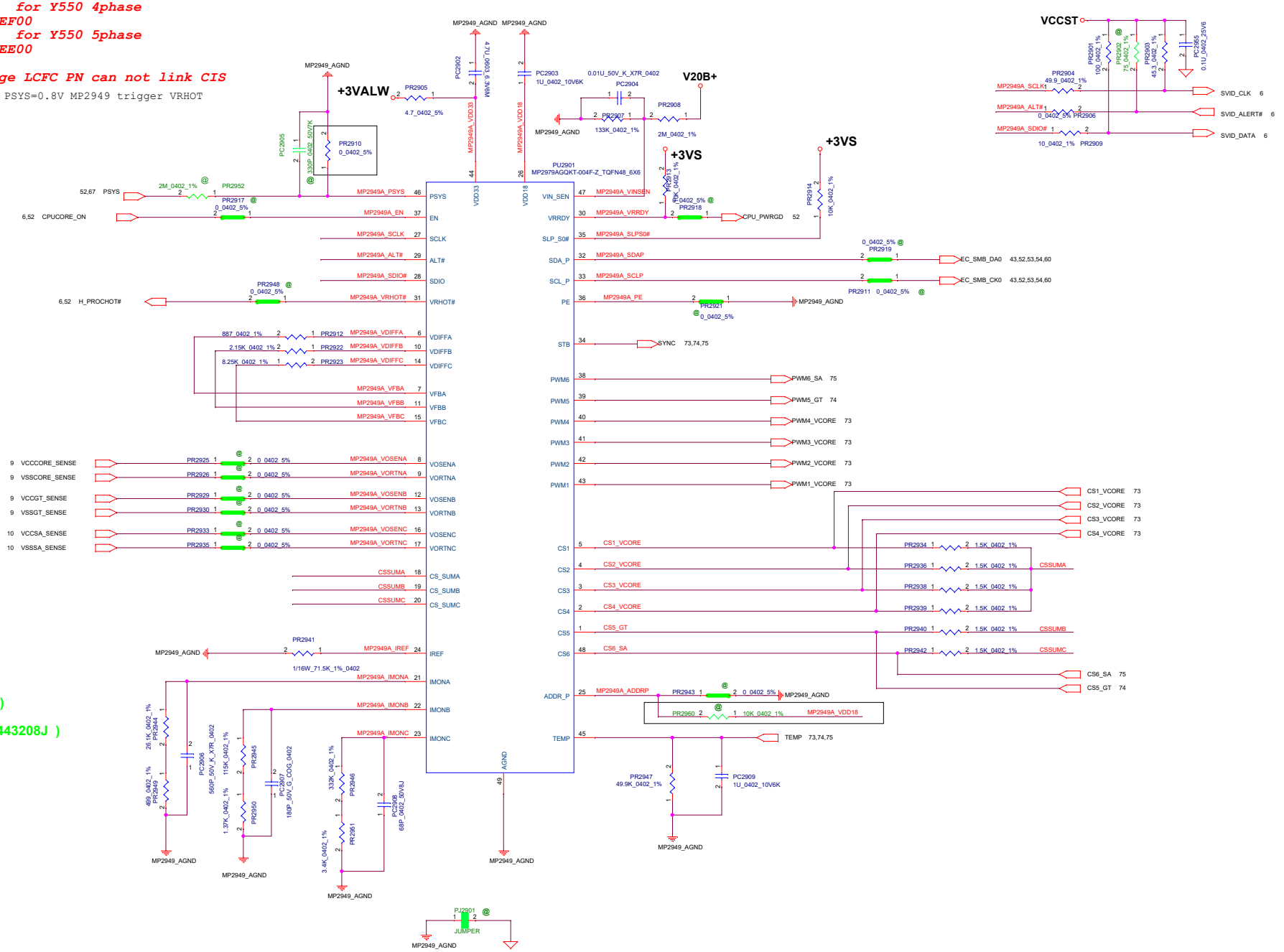
Size	Document Number	Rev
Custom	Y550	1.0

Date: Wednesday, February 19, 2020 Sheet 71 of 83

MP2979AGQKT-004F for Y550 4phase
LCFC PN: SA0000AEF00
MP2979AGQKT-004E for Y550 5phase
LCFC PN: SA0000AEE00

PU2901 only change LCFC PN can not link CIS

PSYS=0.8V MP2949 trigger VRHOT



5Phase
PR2912=887ohm(SD00000XK8J)
PR2944+PR2949=22.567K
(22.1K SD03422128J+432 SD03443208J)
PC2907=180pF(SE000017A00)
PR2939=750ohm(SD03475008J)

Security Classification	LC Future Center Secret Data		
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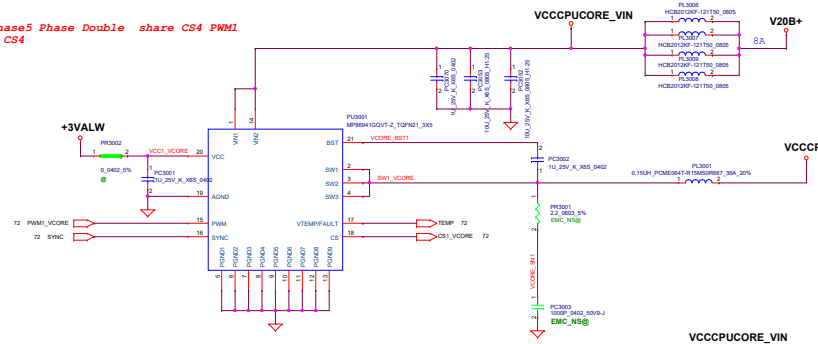
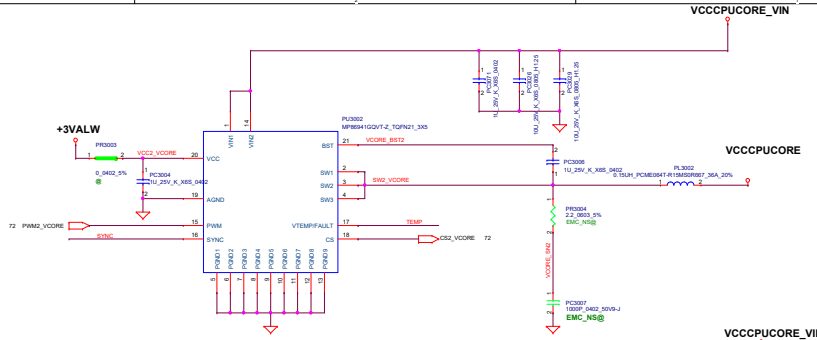
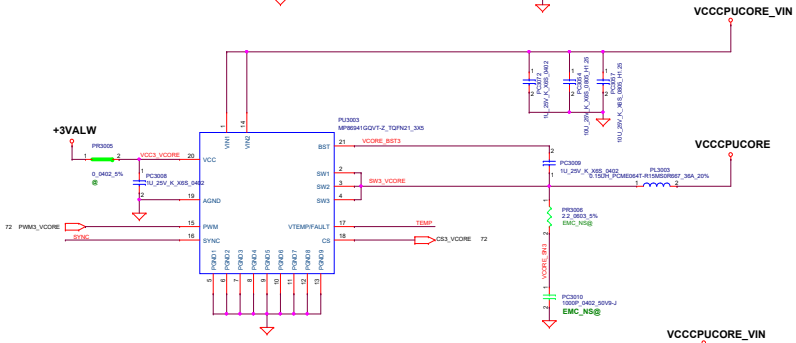
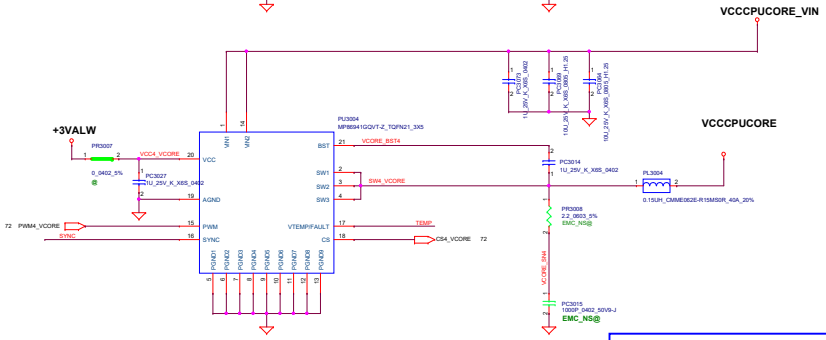
Phase4 Phase5 Phase Double share CS4 PWM1
CS share CS4

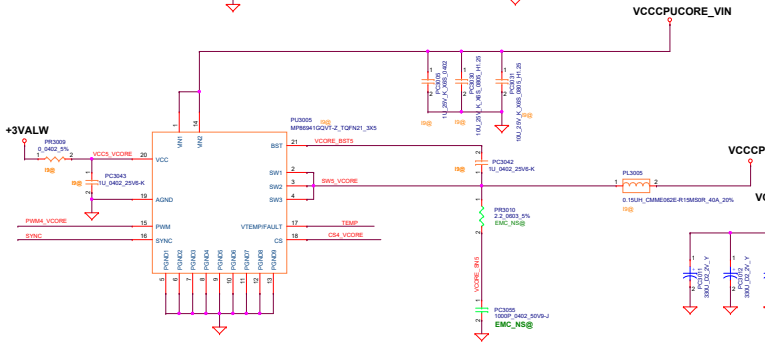




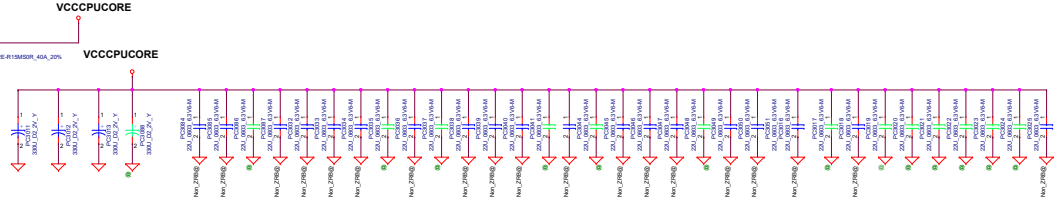


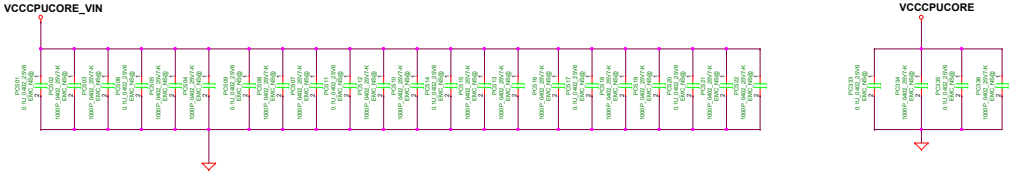


Vboot=0V Loadline=1.1mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=±10mV(0.5A-TDC)
Ripple=±15mV(TDC-Iccmax)
TDC=125A Performance Line(5phase) Iccmax=165A
TDC=86A Base Line(4phase) Iccmax=140A
OVP=VID+400mV
OVP=2V(during SS)
UVP=VID-300mV
Fsw=500Khz



Y540:330u*2PCS+22u*19PCS
Y550:follow Y540 Vendor
PDG:470uF*4pcs+47uF*33pcs
Actual:330u*3PCS+22u*19PCS





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title	PWR-VCCCPUCORE		
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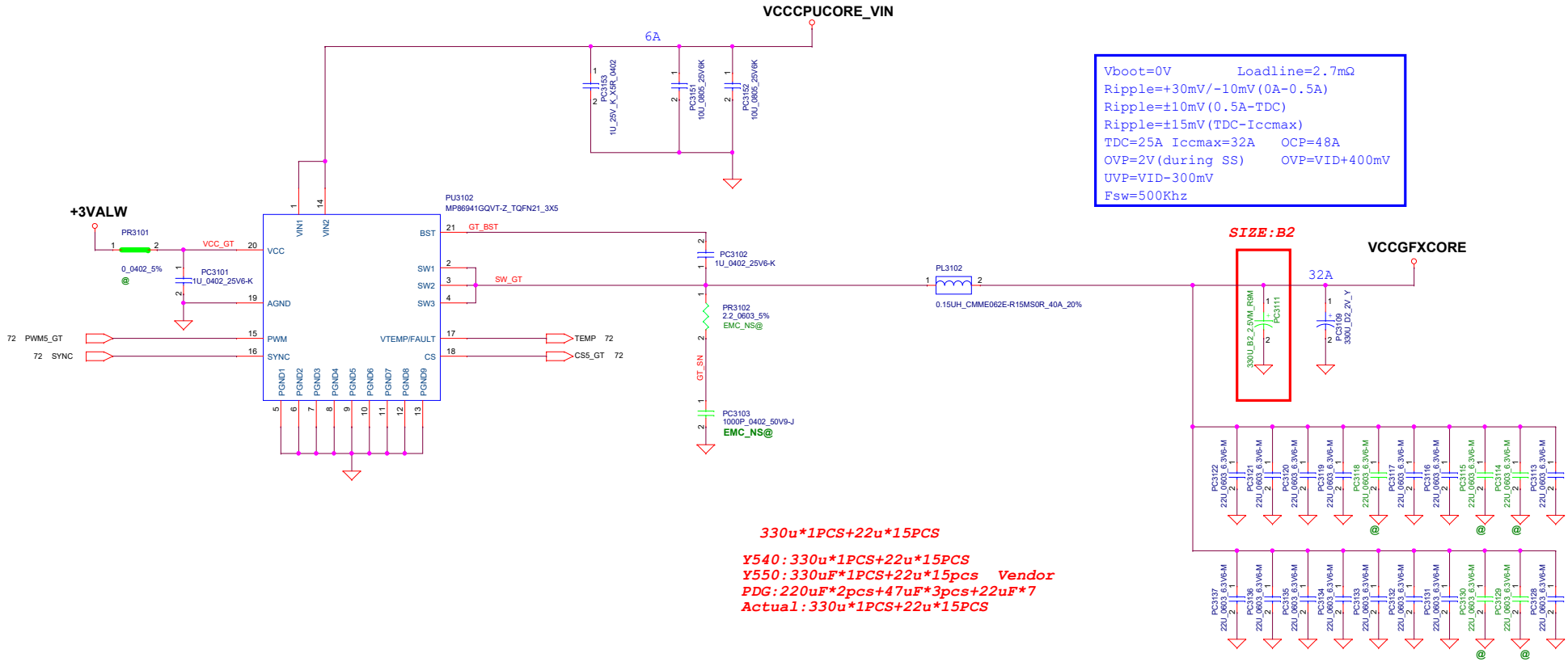

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCGFXCORE

Size: Custom | Document Number: Y550 | Rev: 1.0

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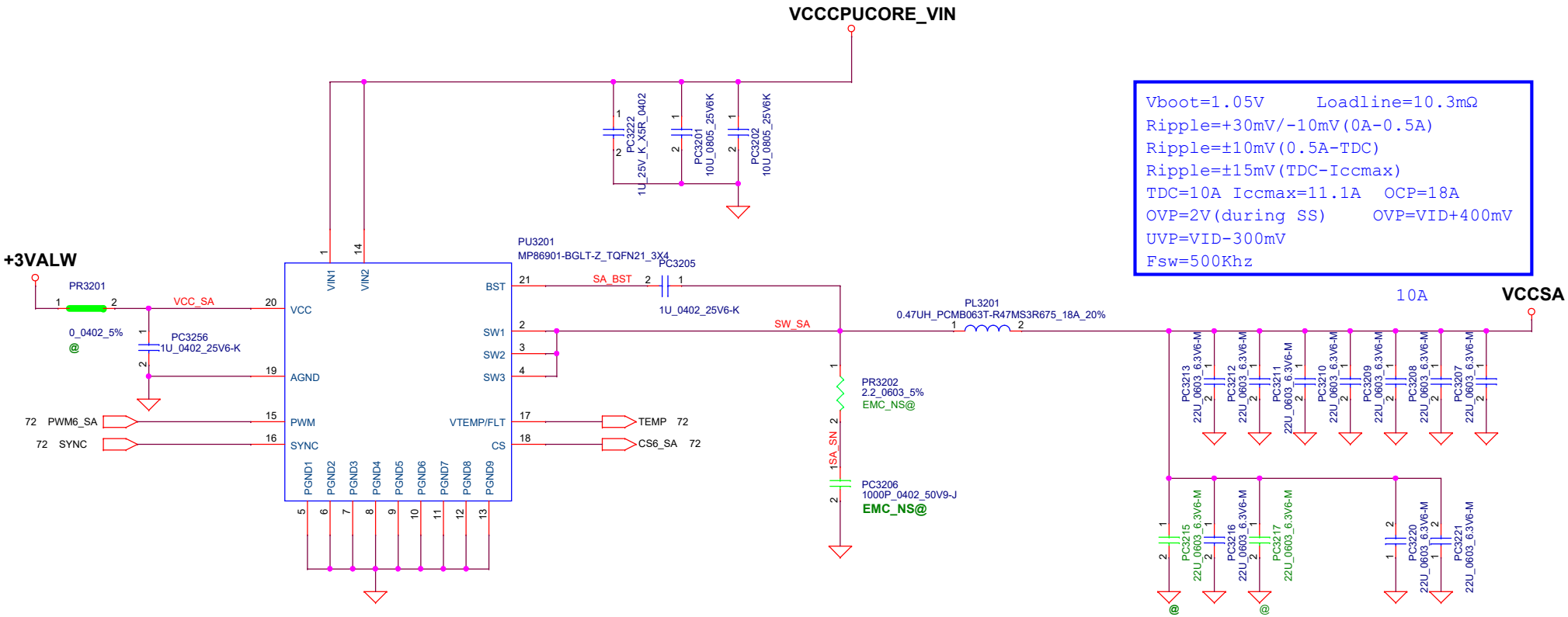
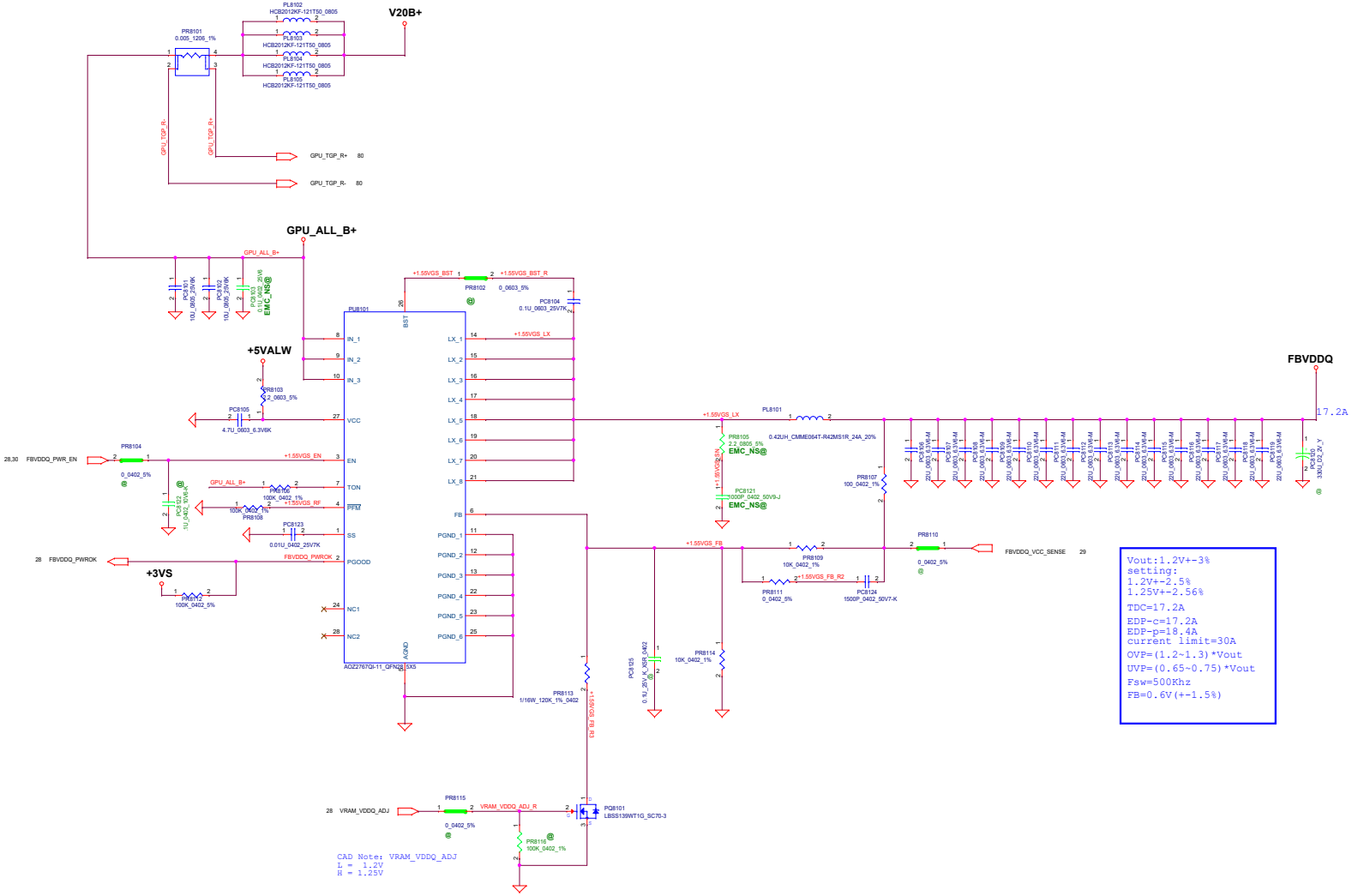


Y540:22u*10PCS
Y550:22u*10pcs Vendor
PDG:220uF*1pcs+47uF*4pcs+22uF*4
Actual:22u*10PCS

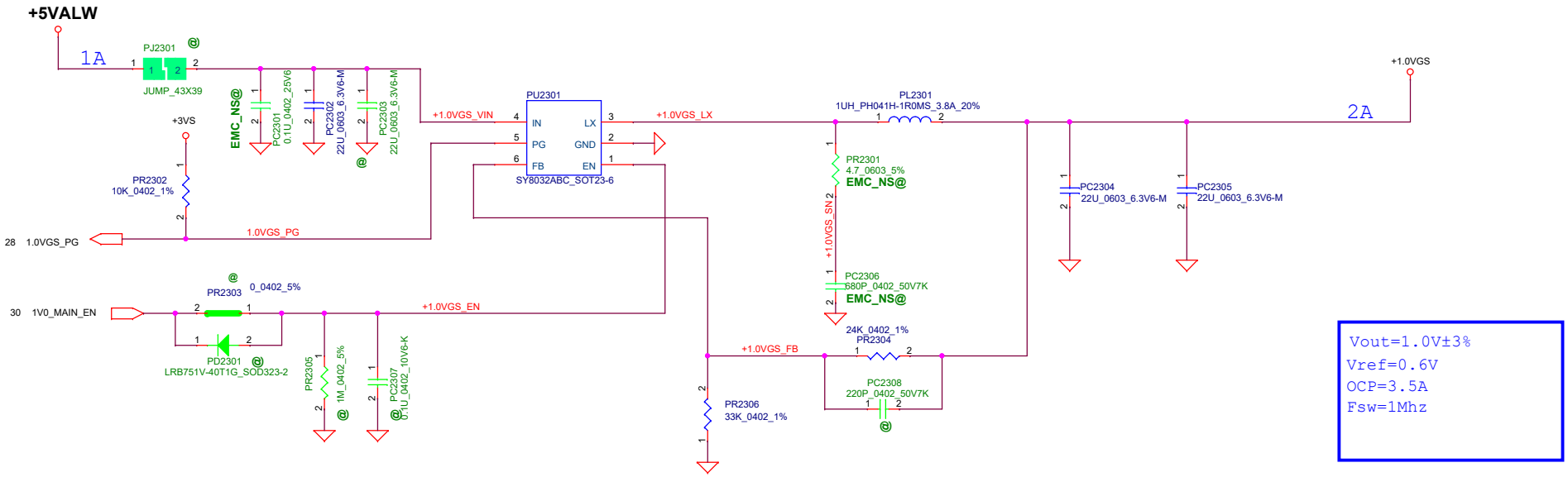
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-VCCSA		
Size B	Document Number	Y550	Rev 1.0
Date:	Wednesday, February 19, 2020	Sheet 75 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

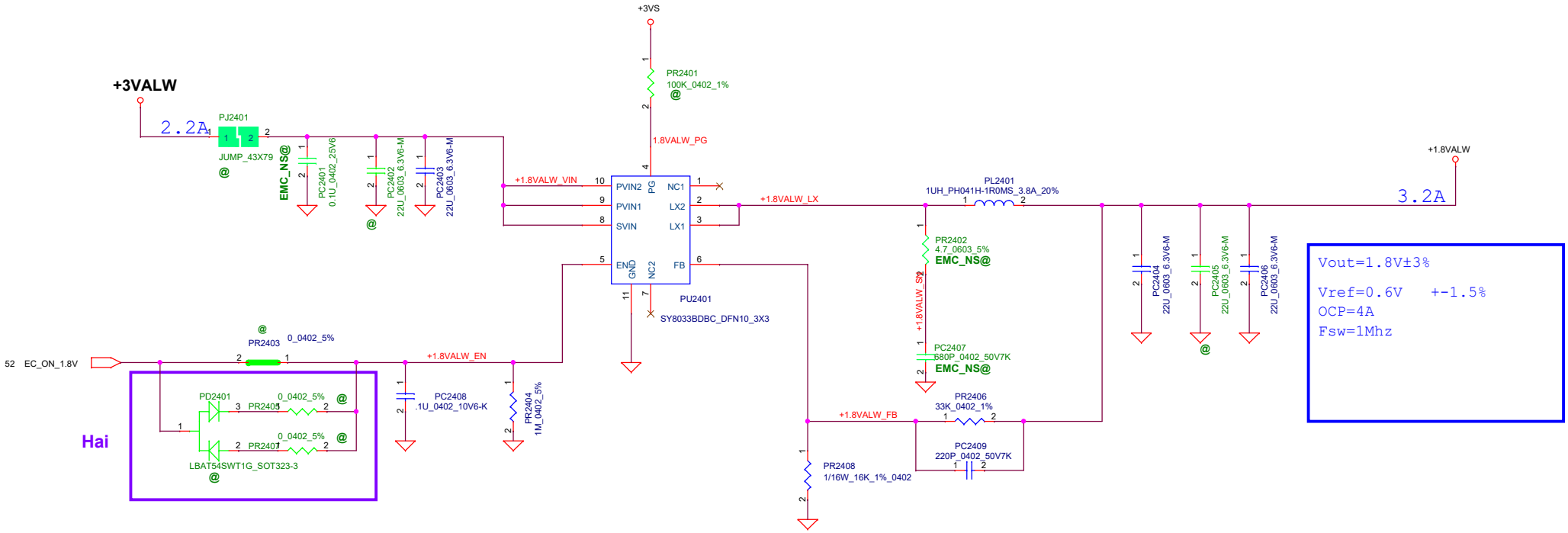
Title	PWR-FBVDDQ		
Size	Document Number	Rev	
Custom	Y550	1.0	
Date:	Wednesday, February 19, 2020	Sheet 76 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.8/1.0VGS**

Size: Custom	Document Number: Y550	Rev: 1.0
Date: Wednesday, February 19, 2020	Sheet 77 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.8/1.0VGS**

Size: Custom	Document Number: Y550	Rev: 1.0
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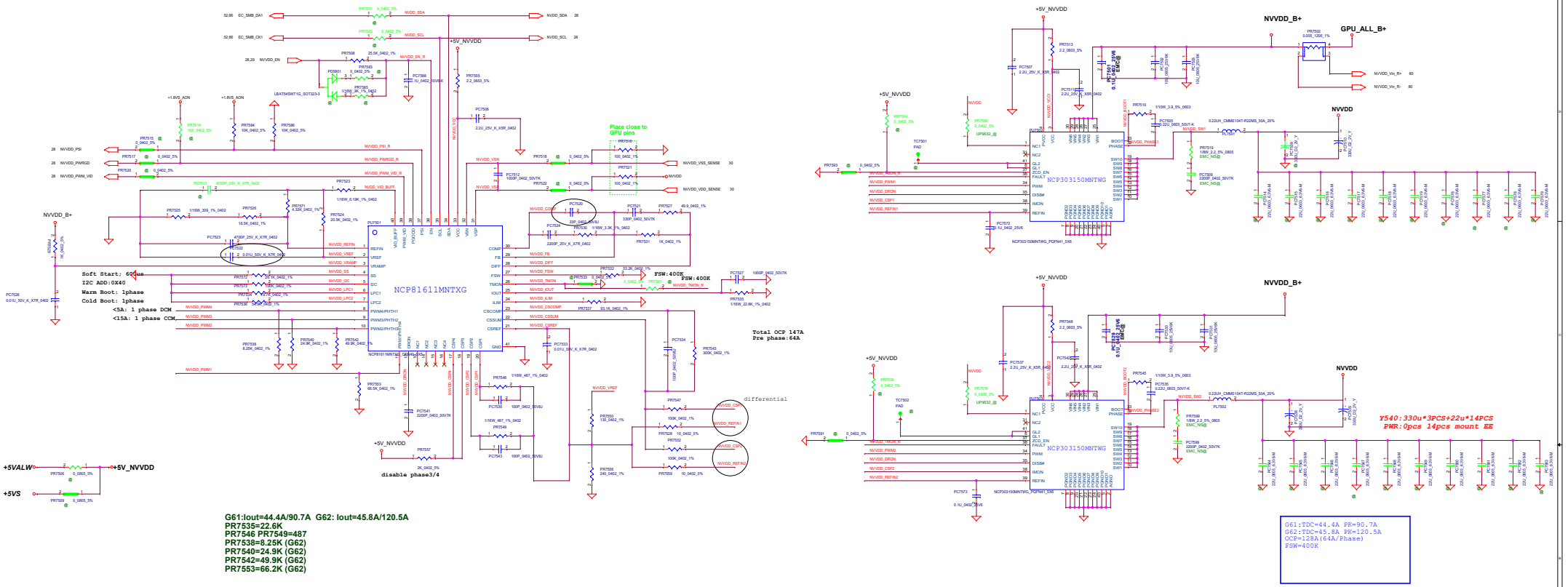

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-NVVDD

Size: Custom | Document Number: Y550 | Rev: 1.0

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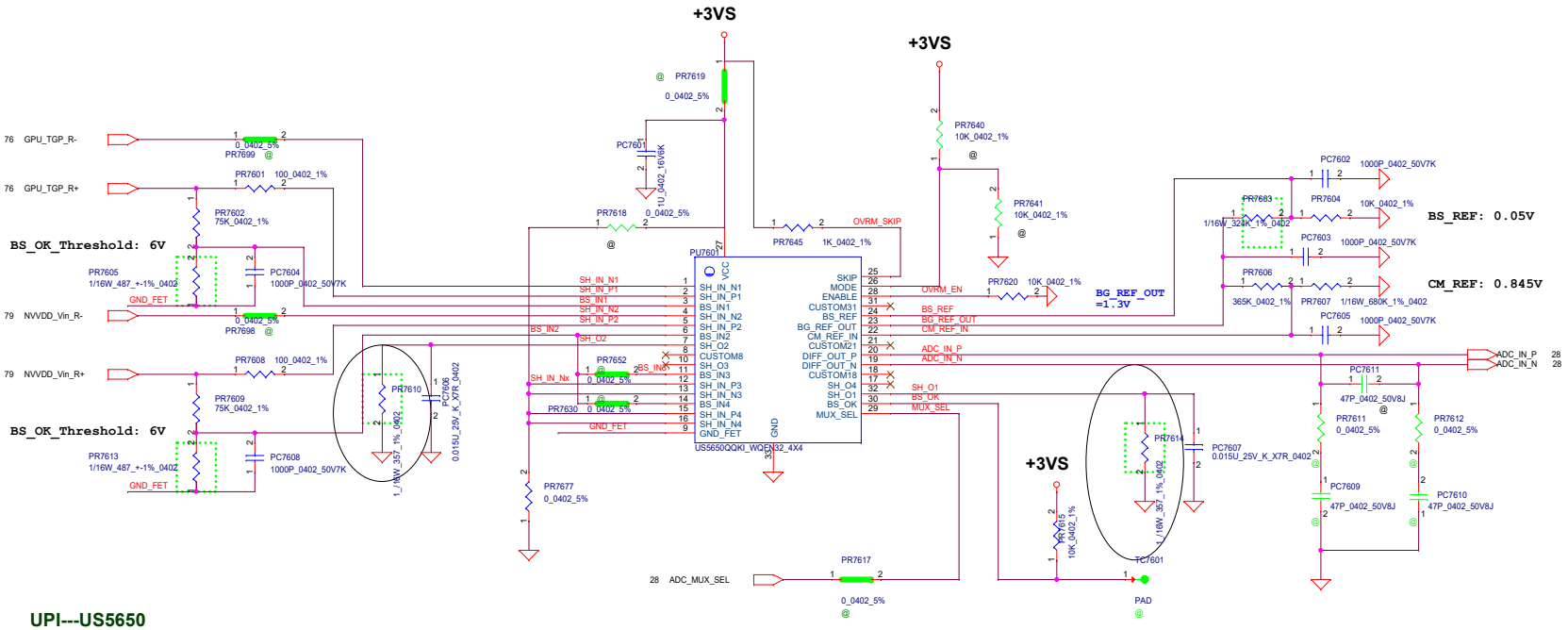

UPI---US5650
PR7605=487
PR7613=487
PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7603=324K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

ON---NCP45491
PR7605=649
PR7613=649
PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7603=243K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-NVVDDS		
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Security Classification	LC Future Center Secret Data		
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Title

Virtual symbol

Size	Document Number	Rev
C	***¥550***	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

Blank

Size	Document Number	Rev
C	***¥550***	1.0

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Security Classification	LC Future Center Secret Data		
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Title
Blank

Size	Document Number	Rev
C	***¥550***	1.0

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