LCFC NM-B112

NANO G AST CG512 M/B Schematics Document

AMD FT4 Stoney SOC with DDRIIII

AMD R16M-M1-30

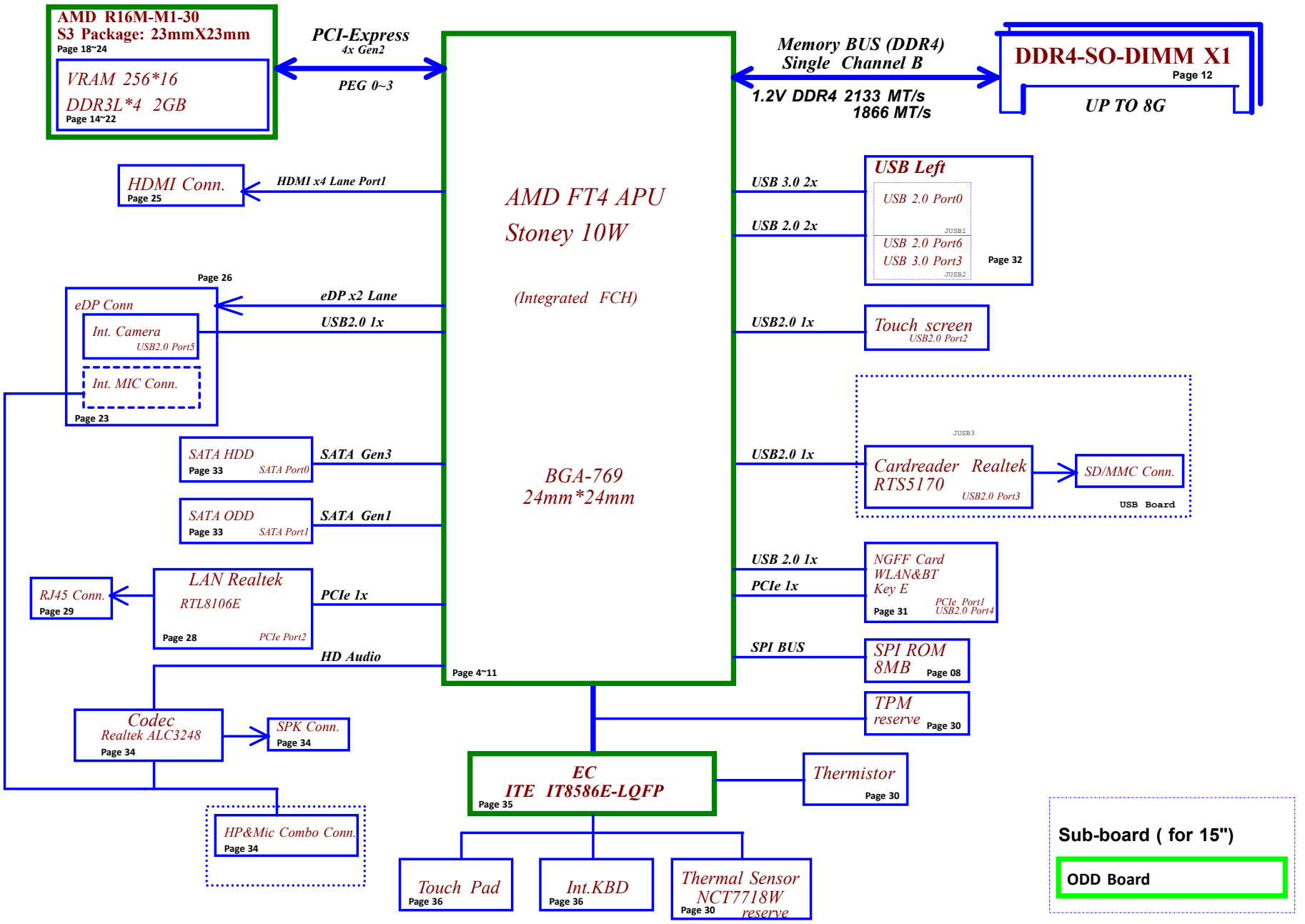
REV:0.2

2016-5-18

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: Cover Page			
Size: Custom	Document Number: CG521		Rev: 0.1
Date: Monday, August 08, 2016	Sheet 1 of 48		

File Name : German



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: Block Diagram

Size	Document Number	Rev
Custom	CG521	0.1

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Voltage Rails (O --> Means ON , X --> Means OFF)

power plane / State	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+2.5V +1.2V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOARD Config.	BOARD_ID0	BOARD_ID1	BOARD_ID2	Function
	0: 14''	0: Dis		
	1: 15''	1: UMA		

USB Port Table for Stoney FT4

USB 2.0	USB 3.0	Port	Port device
EHCI		0	Left USB (2.0)
		1	Blue Tooth
		2	Camera
		3	Touch screen
xHCI		4	Card Reader
		5	LEFT USB (3.0)
	2	6	N/A
		7	N/A

PCIE PORT LIST

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	DIS GPU
	1	
	2	
	3	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_PX@	EMC GPU part
EMC_CZ@	EMC Carrizo APU part
EMC_15@	EMC 15 part
RF_NS@	RF reserve Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
AOAC@	AOAC support part
HDT@	HDT Debug part
TS@	Touch screen part
CZ@	Carrizo Part
CZL@	CarrizoL part
CZPX@	Carrizo Discrete Part
CZLPX@	CarrizoL Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2GX4@	X76 SAMSUNG 1G
M2GX4@	X76 MICRON 1G
H2GX4@	X76 HYNIX 1G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
S1G@	SAMSUNG 1G
M1G@	MICRON 1G
H1G@	HYNIX 1G
CZLUMA@	CarrizoL UMA Part
CZUMA@	Carrizo UMA Part
SIVCD@	SIV COST down material
HDMI@	HDMI Logo

VRAM

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	HDMI Convert reserve
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VS_VGA	X		X	X	V	V APU_SIC APU_SID 3VS for AST	X	V
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

EC SM Bus1 address

Device	Address
Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_100xb(reserve)
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting
HDMI Convert	RSVD

APU SM Bus address

Device	Address
DDR DIMMA	0xA0h
DDR DIMMB	0xA2h
WLAN	RSVD

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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **Notes List**

Size	Document Number	Rev
Custom	BMWQ3	0.1

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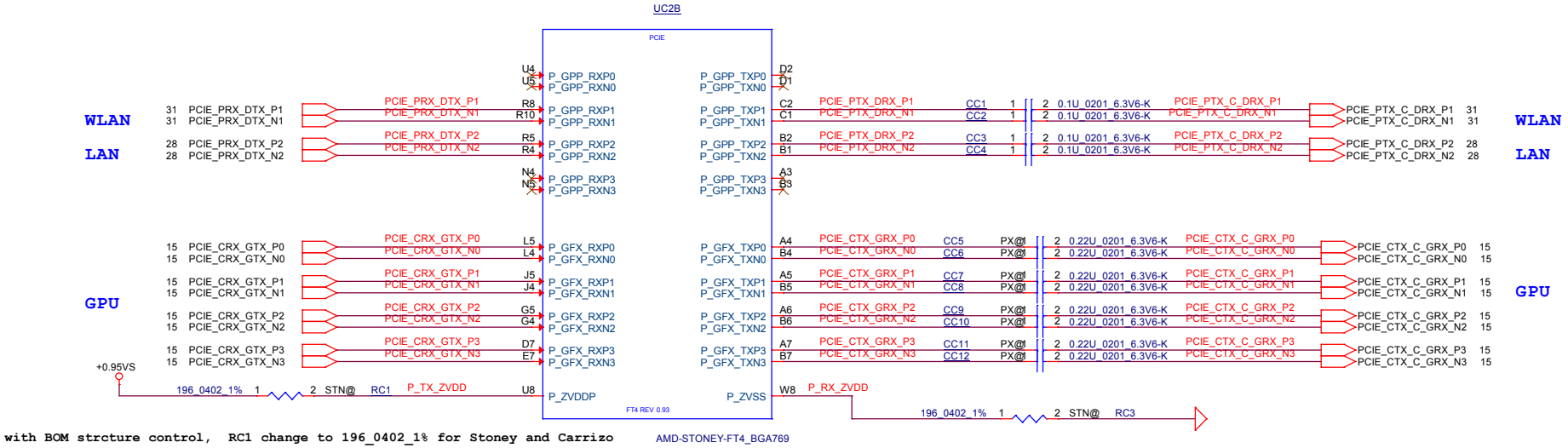

with BOM strcture control, RC1 change to 196_0402_1% for Stoney and Carrizo @

CarrizoL not support GFX4-GFX7

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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FP4 (PCIE I/F)

Size	Document Number	Rev
Custom	CG521	0.1

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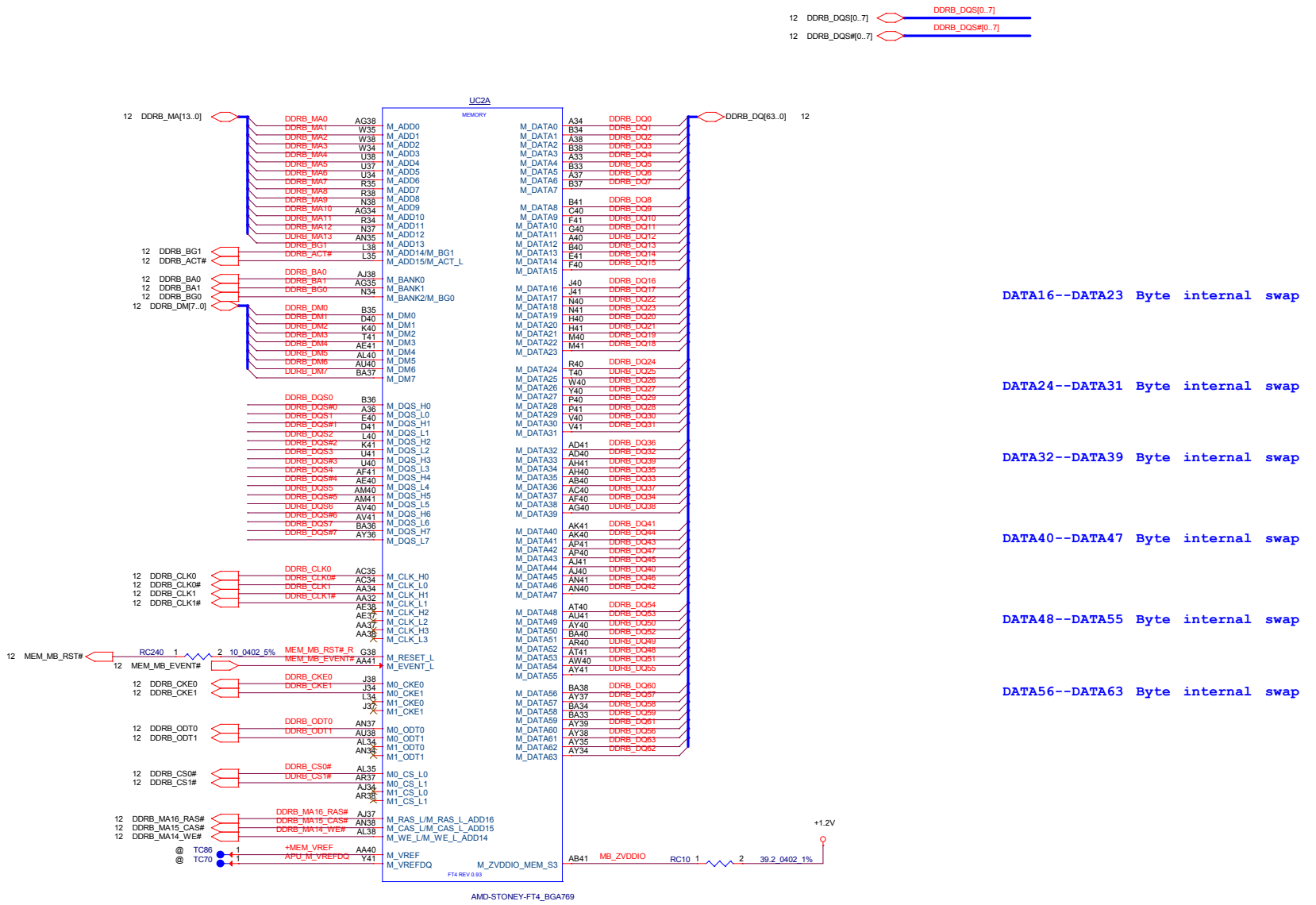

Title: **FP4 (MEM)**

Size	Document Number	Rev
Custom	CG521	0.1

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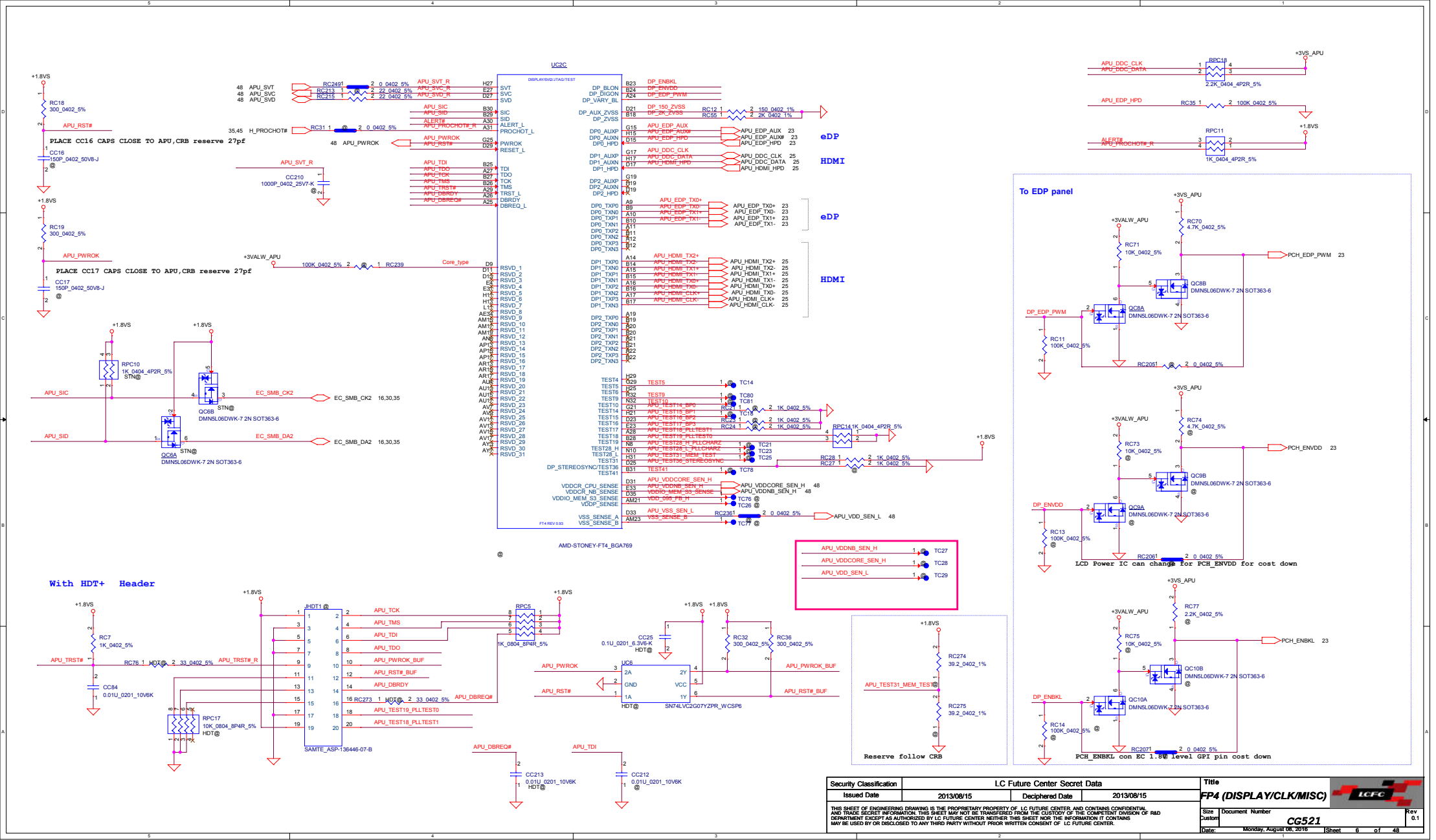
UC2C
AMD-STONEY-FT4_BGA769
eDP
HDMI
eDP
HDMI
PLACE CC16 CAPS CLOSE TO APU,CRB reserve 27pf
PLACE CC17 CAPS CLOSE TO APU,CRB reserve 27pf
To EDP panel
LCD Power IC can change for PCH_ENVDD cost down
PCH_ENBKL con EC 1.8V level GPI pin cost down
With HDT+ Header
Reserve follow CRB
SAMTE_ASP-136446-07-B
SN74LVC2G07YZPR_WCSP6
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
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FP4 (DISPLAY/CLK/MISC)
Size
Custom
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Rev
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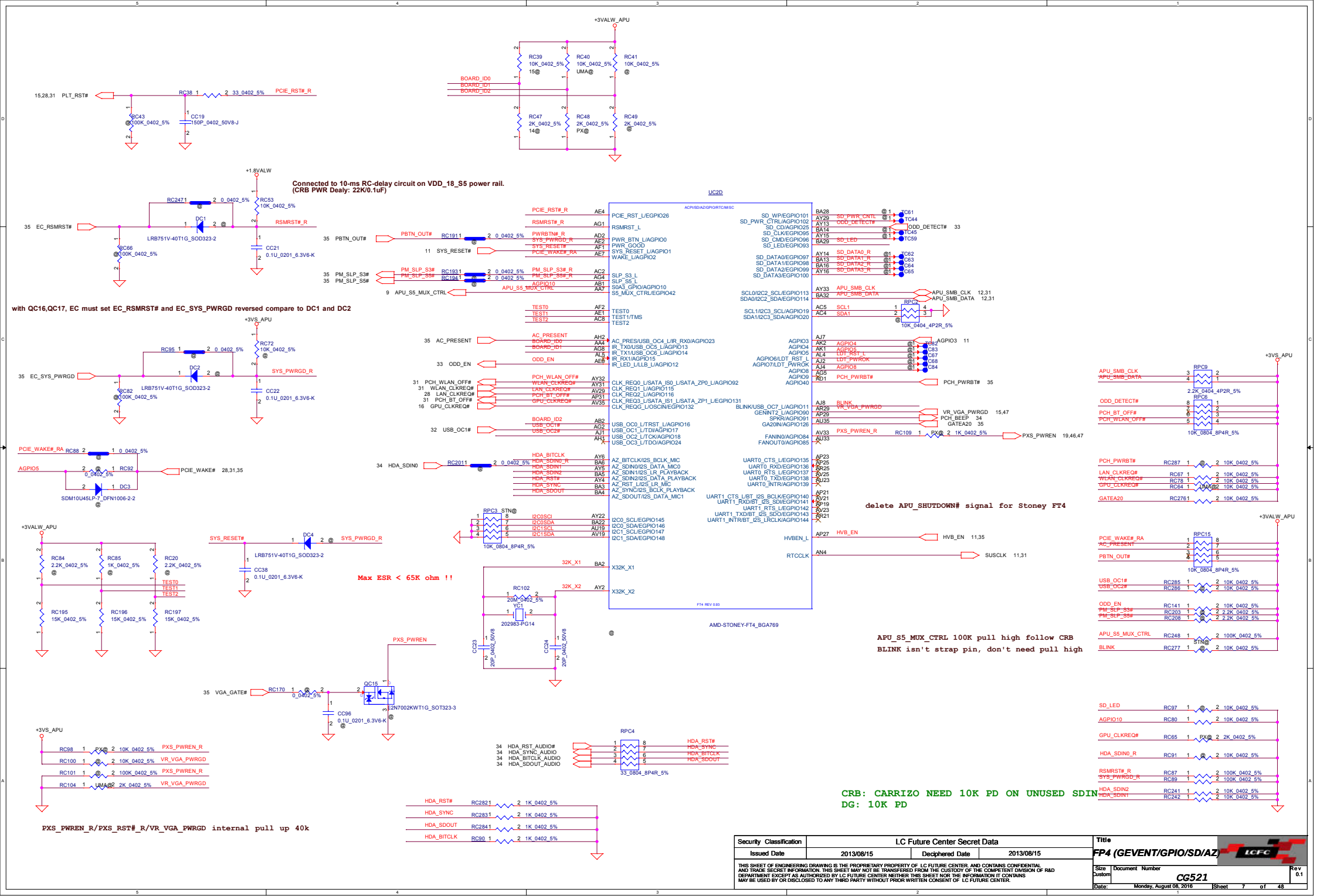

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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FP4 (GEVENT/GPIO/SD/AZ)

Size	Document Number	Rev
Custom	CG521	0.1

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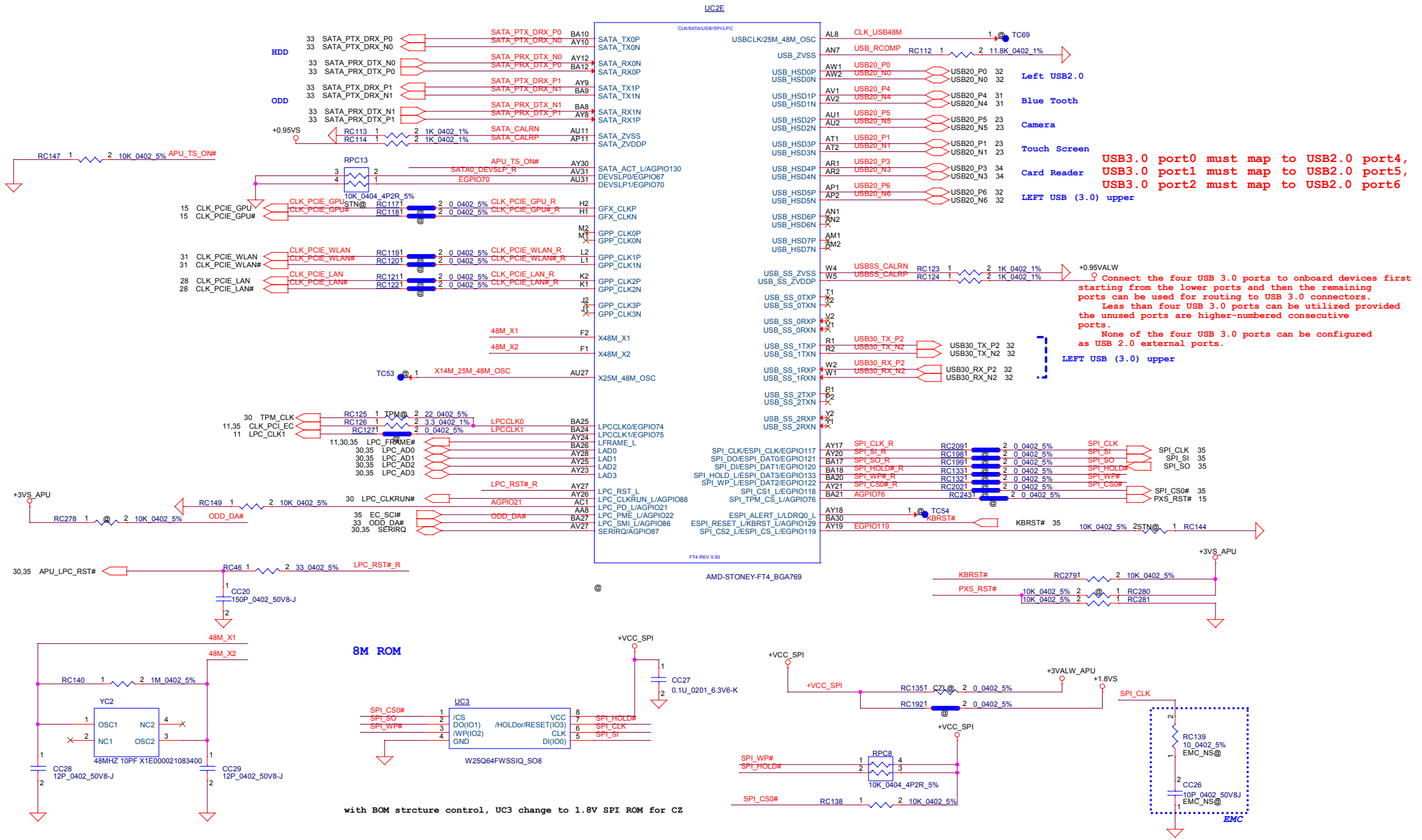

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	FP4 (SATA/USB/LPC/SPI)		
Size Custom	Document Number CG521		Rev 0.1
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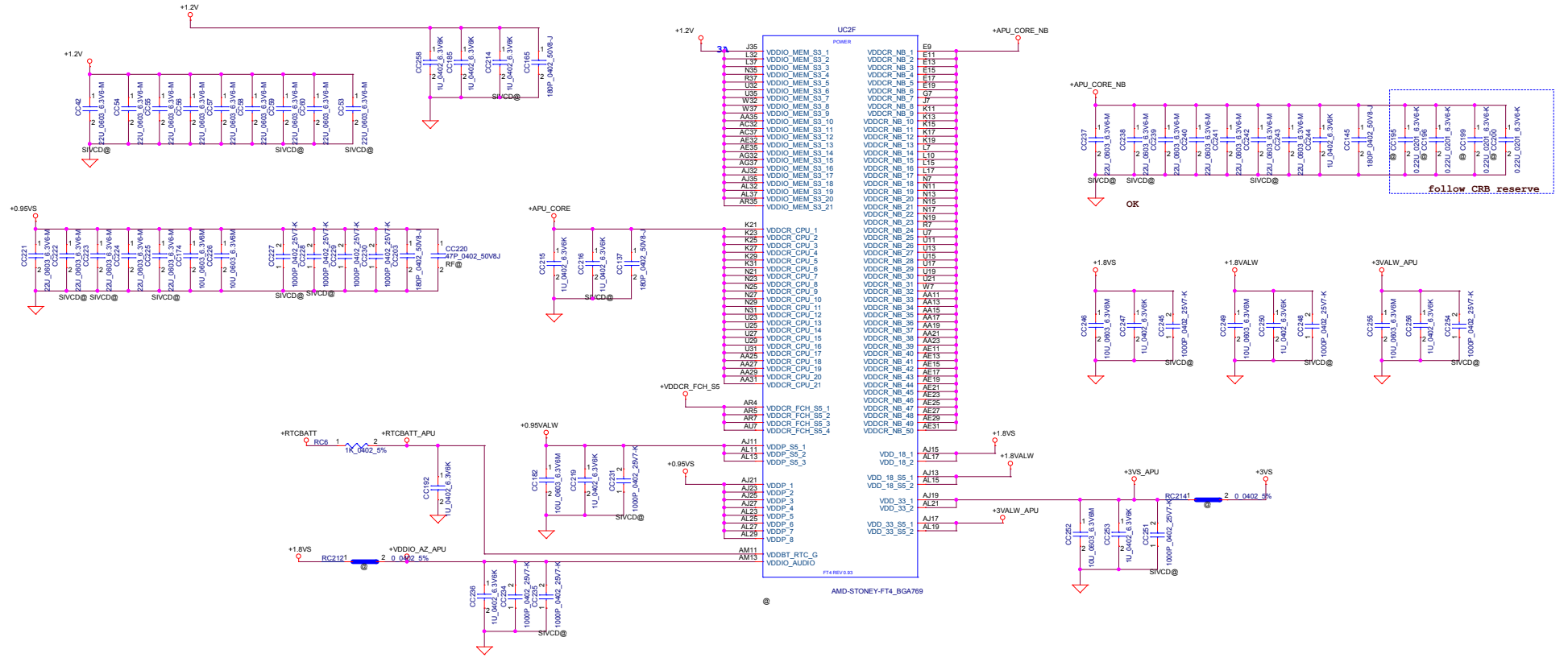

Vinafix.com

	Design Guide	G FT4	CRB
VDDCR_CPU	7*22uf 0603 2*1uf 0402 1*180pf 0402	11*22uf 0805 2*1uf 0402 1*180pf 0402	11*22uf 0603 1*1uf 0402 1*180pf 0402
VDDCR_NB	11*22uf 0603 1*1uf 0402 1*180pf 0402	11*22uf 0603 1*1uf 0402 1*180pf 0402	15*22uf 0603 8*0.22uf 0402 split *5 1*180pf 0402
VDDCR_GFX			
VDDIO_MEM_S3	9*22uf 0603 3*1uf 0402 3*180pf 0402	9*22uf 0603 2*1uf 0402 split*4 0.22uf 0402 1*180pf 0402 split*2	9*22uf 0603 2*1uf 0402 split*4 0.22uf 0402 1*180pf 0402 split*2
VDDCR_FCH_S5	1*10uf 0402 2*1uf 0402 2*1000pf 0402	1*10uf 0402 2*1uf 0402 2*1000pf 0402	2*10uf 0603 1*0.22uf 0402
VDDP	5*22uf 0603 2*10uf 0603 4*1000pf 0402 1*180pf 0402	5*22uf 0603 2*10uf 0603 4*1000pf 0402 1*180pf 0402	4*10uf 0603 1*0.22uf 0402 1*180pf 0402
VDDP_GFX			
VDDP_S5	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603 1*0.22uf 0402
VDD_18	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*22uf 0603 1*10uf 0603
VDD_18_S5	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603 1*0.22uf 0402
VDD_33	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603
VDD_33_S5	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603 1*0.22uf 0402
VDDIO_AUDIO	1*10uf 0402 2*1000pf 0402	1*10uf 0402 2*1000pf 0402	3*1uf 0402
VDDBT_RTC_G	1*1000pf 0402	1*1000pf 0402	1*0.22uf 0402

Security Classification	LC Future Center Secret Data		
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Title: FP4 (POWER&DECOUPLING)

Size: Custom	Document Number: BMWQ3	Rev: 0.1
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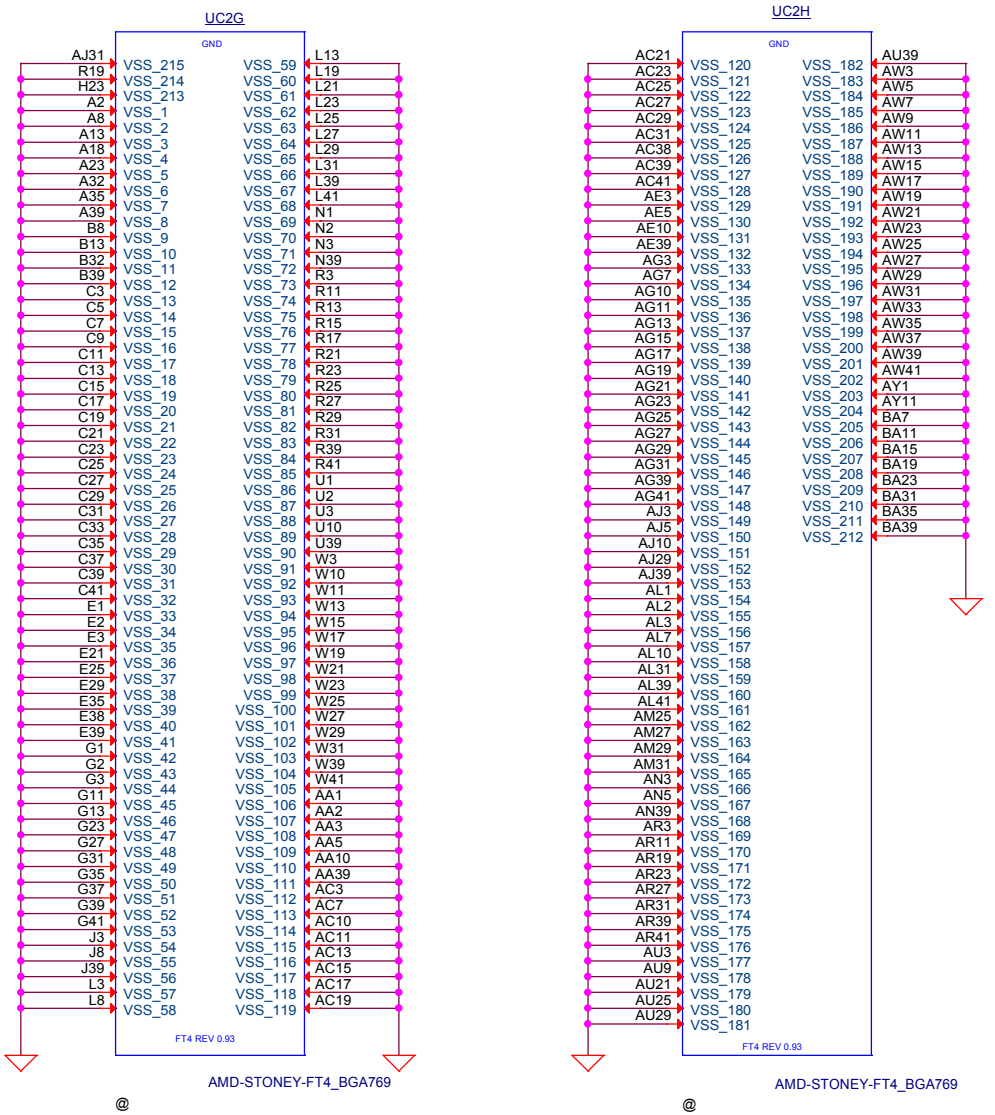

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title

FT4 (VSS)

Size	Document Number	Rev
Custom	CG521	0.1
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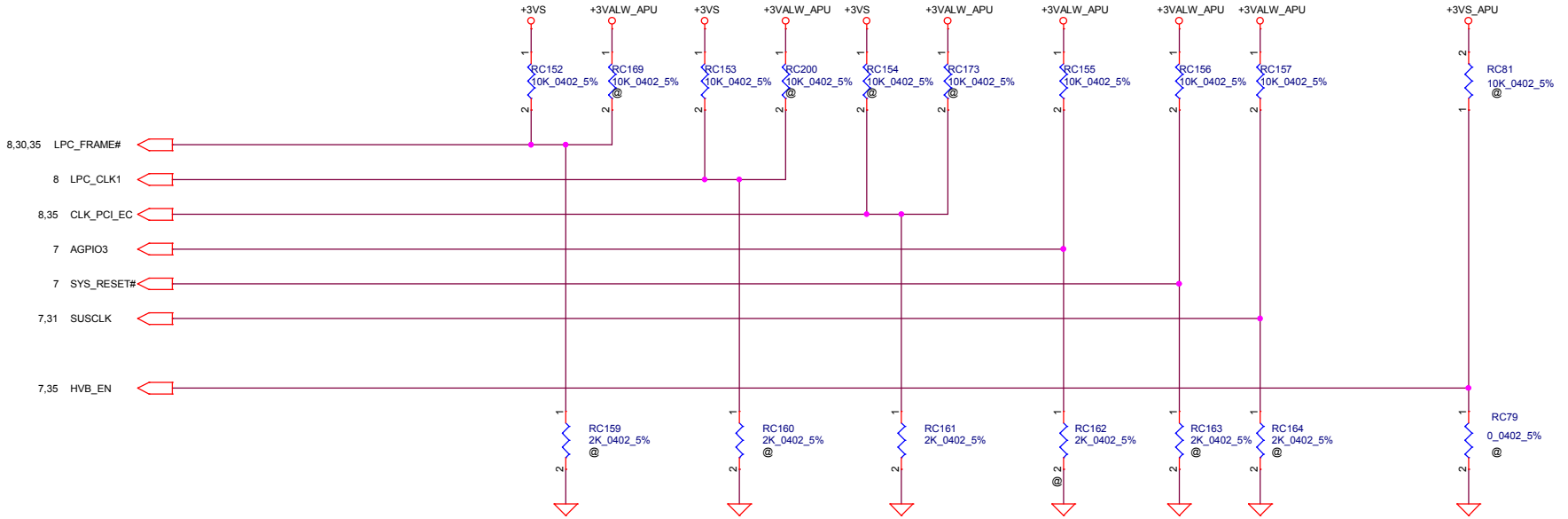

STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	RTCCLK Int pull-up	SYS_RESET_L Int pull-up	AGPIO3 Int pull-up	HVB_EN
Type	II	II	II	I	I	I	
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	RTC Coin Battery is implemented Default	Normal Power Up &Reset Timing Default	Enhanced reset logic (for quicker S5 resume) Default	floating Disable HVB on FT4 platforms Default
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	RTC Coin Battery is not implemented	Reserved	traditional reset logic	connected to VSS Enable HVB on FT4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

Type II straps become valid after PWR_GOOD is asserted,straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.
Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to ' 1' for ℄ AGPIO3

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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FP4 (STRAPS)

Size	Document Number	Rev
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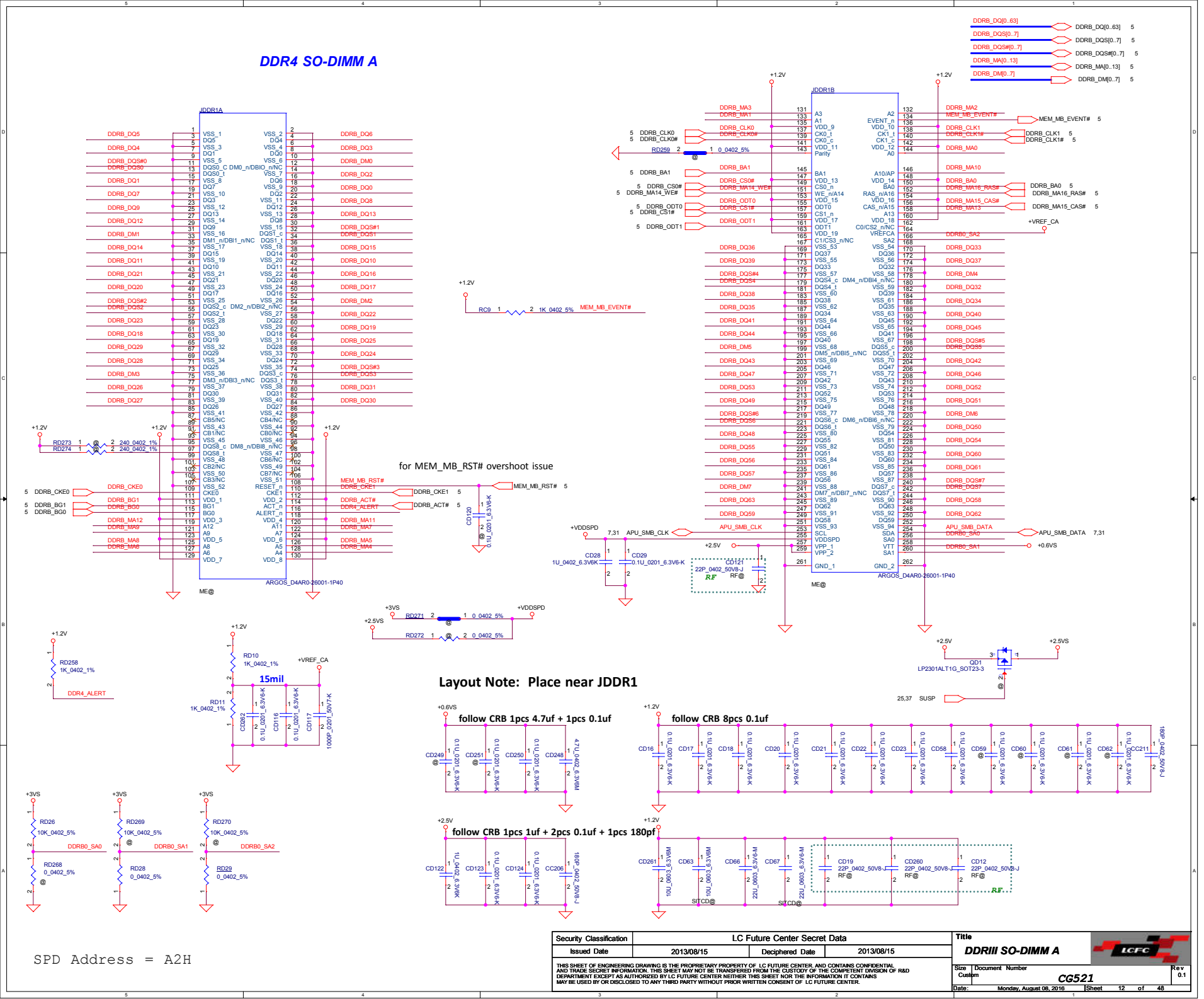
DDR4 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	DDRIII SO-DIMM A		
Size	Document Number		Rev
Custom	CG521		0.1
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Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **DDRIII SO-DIMM B**

Size	Document Number	Rev
D	CG521	0.1

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

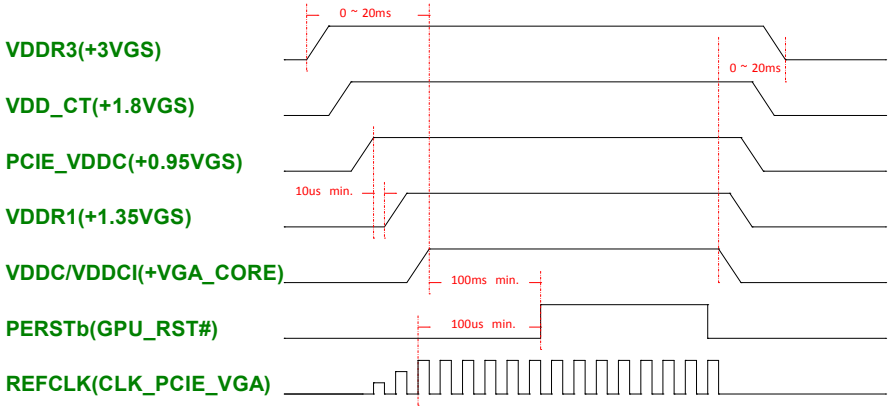
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).

For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Title: VGA Notes List

Size: Custom | Document Number: CG521 | Rev: 0.1

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4 PCIE_CTX_C_GRX_P[3..0]
4 PCIE_CTX_C_GRX_N[3..0]

PCIE_CTX_C_GRX_P[3..0]
PCIE_CTX_C_GRX_N[3..0]

PCIE_CRX_GTX_P[3..0]
PCIE_CRX_GTX_N[3..0]

PCIE_CRX_GTX_P[3..0] 4
PCIE_CRX_GTX_N[3..0] 4

UV1A

PCIE_CTX_C_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_CRX_C_GTX_P0	0.22U_0201_6.3V6-K	1	2 PX@	CV1	PCIE_CRX_GTX_P0
PCIE_CTX_C_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_CRX_C_GTX_N0	0.22U_0201_6.3V6-K	1	2 PX@	CV2	PCIE_CRX_GTX_N0
PCIE_CTX_C_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIE_CRX_C_GTX_P1	0.22U_0201_6.3V6-K	1	2 PX@	CV3	PCIE_CRX_GTX_P1
PCIE_CTX_C_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_CRX_C_GTX_N1	0.22U_0201_6.3V6-K	1	2 PX@	CV4	PCIE_CRX_GTX_N1
PCIE_CTX_C_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_CRX_C_GTX_P2	0.22U_0201_6.3V6-K	1	2 PX@	CV5	PCIE_CRX_GTX_P2
PCIE_CTX_C_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_CRX_C_GTX_N2	0.22U_0201_6.3V6-K	1	2 PX@	CV6	PCIE_CRX_GTX_N2
PCIE_CTX_C_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_CRX_C_GTX_P3	0.22U_0201_6.3V6-K	1	2 PX@	CV7	PCIE_CRX_GTX_P3
PCIE_CTX_C_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_CRX_C_GTX_N3	0.22U_0201_6.3V6-K	1	2 PX@	CV8	PCIE_CRX_GTX_N3

AB30	PCIE_RX4P	PCIE_TX4P	AC25	
AA31	PCIE_RX4N	PCIE_TX4N	AB25	
AA29	PCIE_RX5P	PCIE_TX5P	Y23	
Y28	PCIE_RX5N	PCIE_TX5N	Y24	
Y30	PCIE_RX6P	PCIE_TX6P	AB27	
W31	PCIE_RX6N	PCIE_TX6N	AB26	
W29	PCIE_RX7P	PCIE_TX7P	Y27	
V28	PCIE_RX7N	PCIE_TX7N	Y26	
V30	NC#V30	NC#W24	W24	
U31	NC#U31	NC#W23	W23	
U29	NC#U29	NC#V27	V27	
T28	NC#T28	NC#U26	U26	
T30	NC#T30	NC#U24	U24	
R31	NC#R31	NC#U23	U23	
R29	NC#R29	NC#T26	T26	
P28	NC#P28	NC#T27	T27	
P30	NC#P30	NC#T24	T24	
N31	NC#N31	NC#T23	T23	
N29	NC#N29	NC#P27	P27	
M28	NC#M28	NC#P26	P26	
M30	NC#M30	NC#P24	P24	
L31	NC#L31	NC#P23	P23	
L29	NC#L29	NC#M27	M27	
K30	NC#K30	NC#N26	N26	

PCI EXPRESS INTERFACE

CLOCK

8 CLK_PCIE_GPU
8 CLK_PCIE_GPU#
CLK_PCIE_GPU
CLK_PCIE_GPU#
AK30 PCIE_REFCLKP
AK32 PCIE_REFCLKN

CALIBRATION

PCIE_CALR_TX Y22 RV3 1 PX@ 2 1.69K_0402_1%
PCIE_CALR_RX AA22 RV5 1 PX@ 2 1K_0402_1%
+0.95VGS

1K_0402_1% 1 PX@ 2 RV4 N10 TEST_PG

16 GPU_RST#
GPU_RST#
AL27 PERSTB

AMD R16M-M1-30
EXO@

RV6 100K_0402_5% PX@

RV7 1 @ 2 0_0402_5%
+3VGS

UV2
8 PXS_RST#
7,28,31 PLT_RST#
IN1 IN2 VCC GND OUT
GPU_RST#
MC74VHC1G08DFT2G_SC70-5
PX@

7,47 VR_VGA_PWRGD
GPU_RST#
VR_VGA_PWRGD
DV3 PX@
VGA_PWROK
VGA_PWROK 47
BAT54AWT1G_SOT323-3

with BOM strcture control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok

11/4 change to PC sample SA000074V10

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_PCIE

Size	Document Number	Rev
Custom	CG521	0.1

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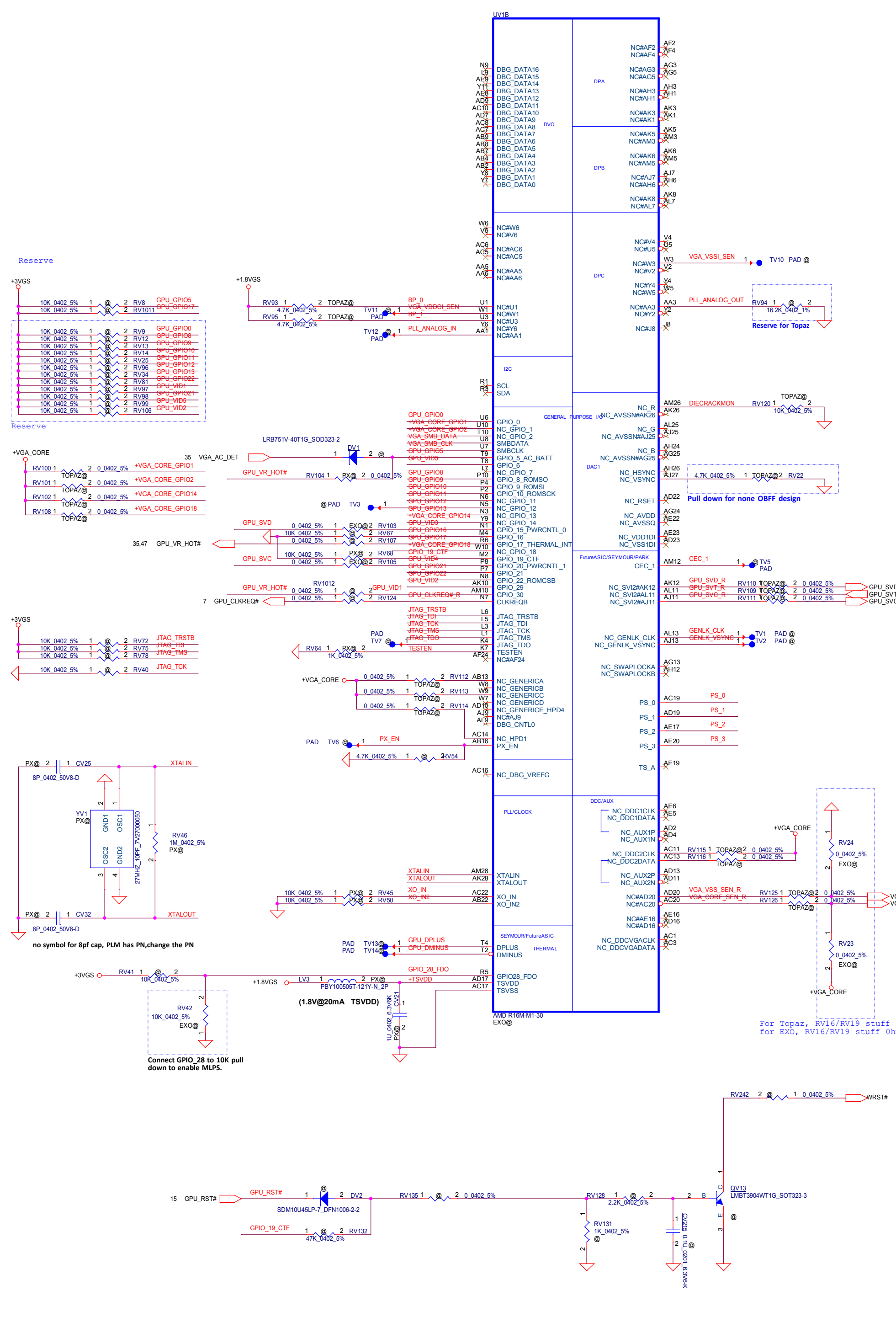
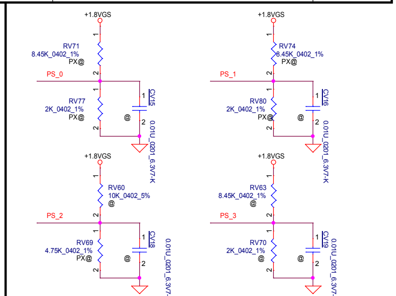


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1, Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_ PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	X
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_ FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	NA
PS_2[2]	N/A	Reserved.	NA
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	0
PS_2[5]	N/A	Reserved	NA
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 1G 000 = Hynix 2G 111 = Micron 1G 010 = Micron 2G 110 = Samsung 1G 001 = Samsung 2G	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable. 111= No usable endpoints.	X



MLPS	Bit					BOM		
	5	4	3	2	1	R_pu( )	R_pd( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45k	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	0	RV74=NC	RV77=4.75K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=X76

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

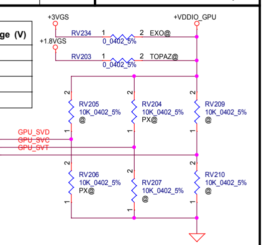
with BOM strcture control,
when config PEG3
RV74 change to 8.45K,
RV80 change to 2K

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

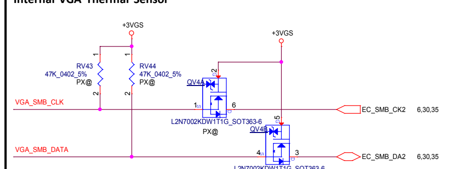
Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



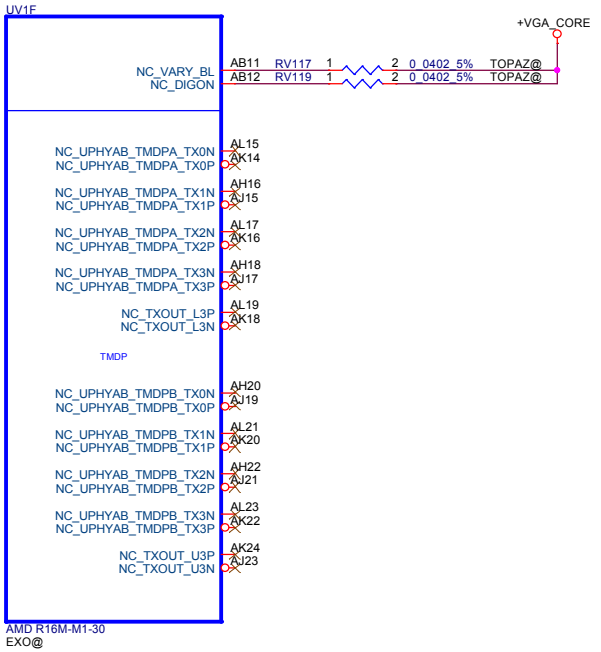
Internal VGA Thermal Sensor



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **ATI_JET-LE_Main_MSIC**

Size: Custom | Document Number: CG521 | Rev: 0.1



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_TMDP

Size	Document Number	Rev
Custom	CG521	0.1

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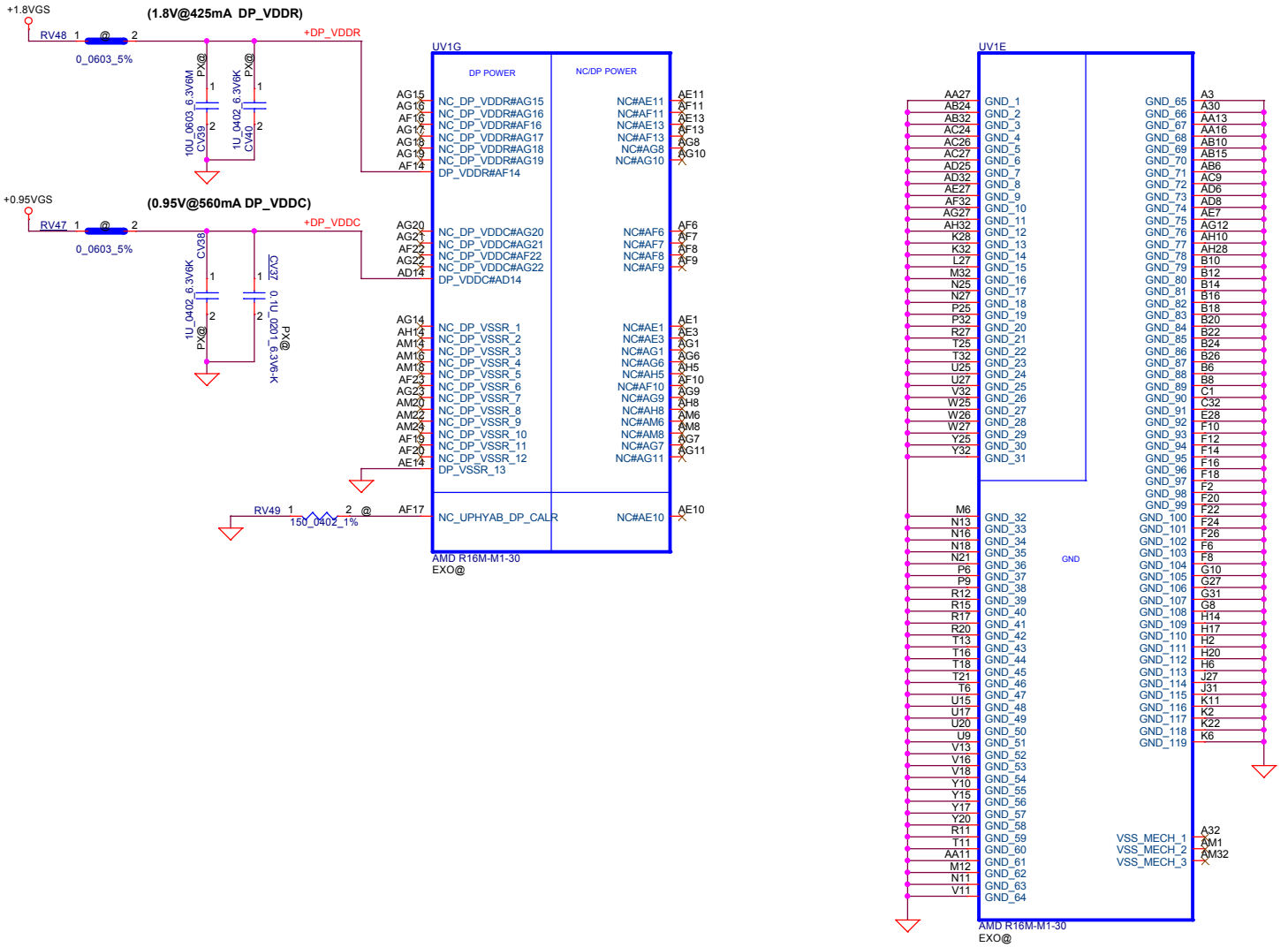
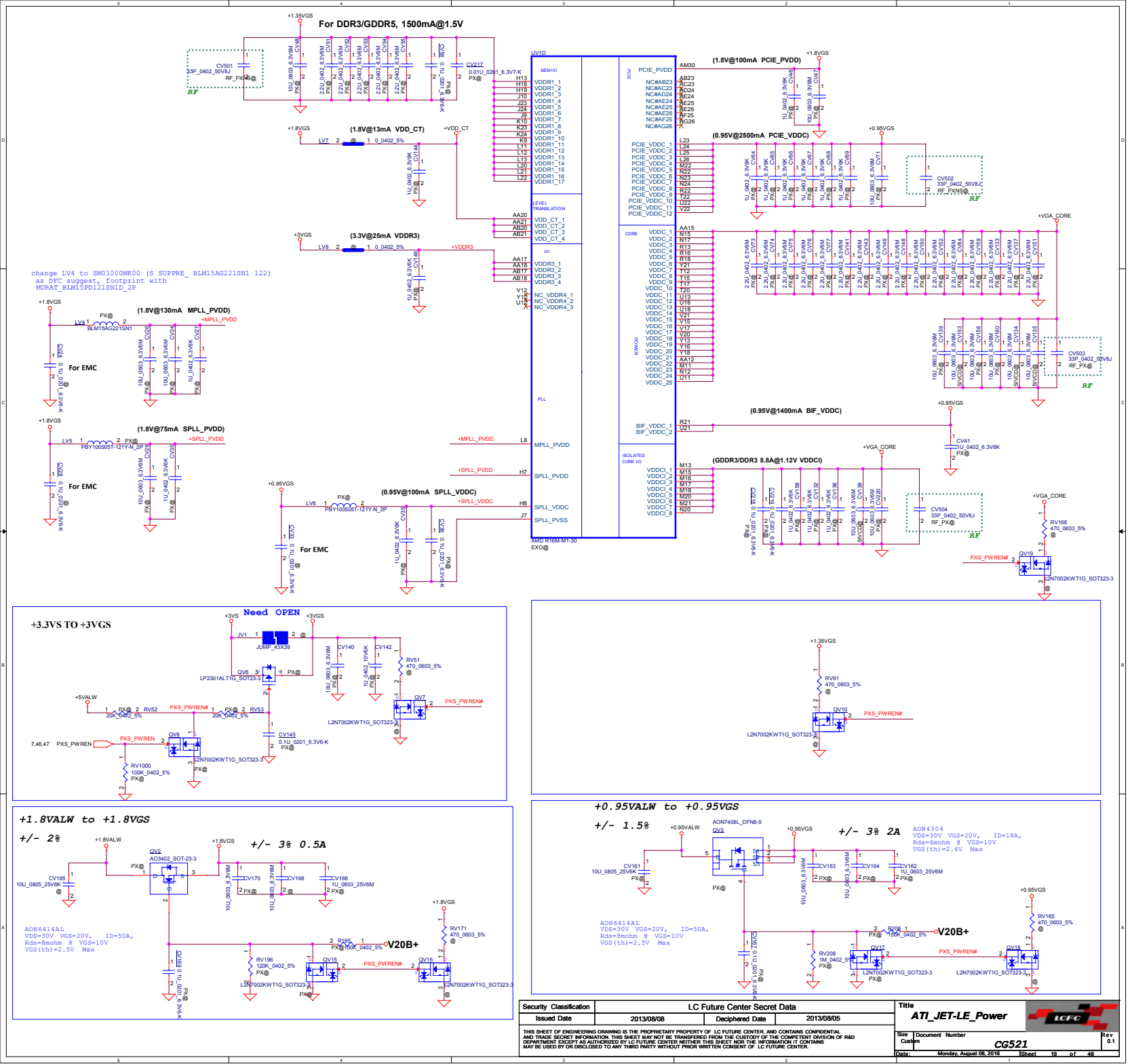


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_DP Power

Size	Document Number	Rev
Custom	CG521	0.1

Date: Monday, August 08, 2016 Sheet 18 of 48


For DDR3/GDDR5, 1500mA@1.5V
(1.8V@100mA PCIE_PVDD)
(0.95V@2500mA PCIE_VDDC)
(1.8V@13mA VDD_CT)
(3.3V@25mA VDDR3)
change LV4 to SM01000MK00 (S SUPPRE_ BLM15AG221SN1 122)
as DFC suggest, footprint with
MURAT_BLM15PD121SN1D_2P
(1.8V@130mA MPLL_PVDD)
(1.8V@75mA SPLL_PVDD)
(0.95V@100mA SPLL_VDDC)
(0.95V@1400mA BIF_VDDC)
(GDDR3/DDR3 8.8A@1.12V VDDCI)
+VGA_CORE
For EMC
Need OPEN
+3.3VS TO +3VGS
+1.8VALW to +1.8VGS
+/- 2%
+/- 3% 0.5A
+0.95VALW to +0.95VGS
+/- 1.5%
+/- 3% 2A
AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max
AON4304
VDS=30V VGS=20V, ID=18A,
Rds=6mohm @ VGS=10V
VGS(th)=2.4V Max
V20B+
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
2013/08/05
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Title
ATI_JET-LE_Power
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Custom
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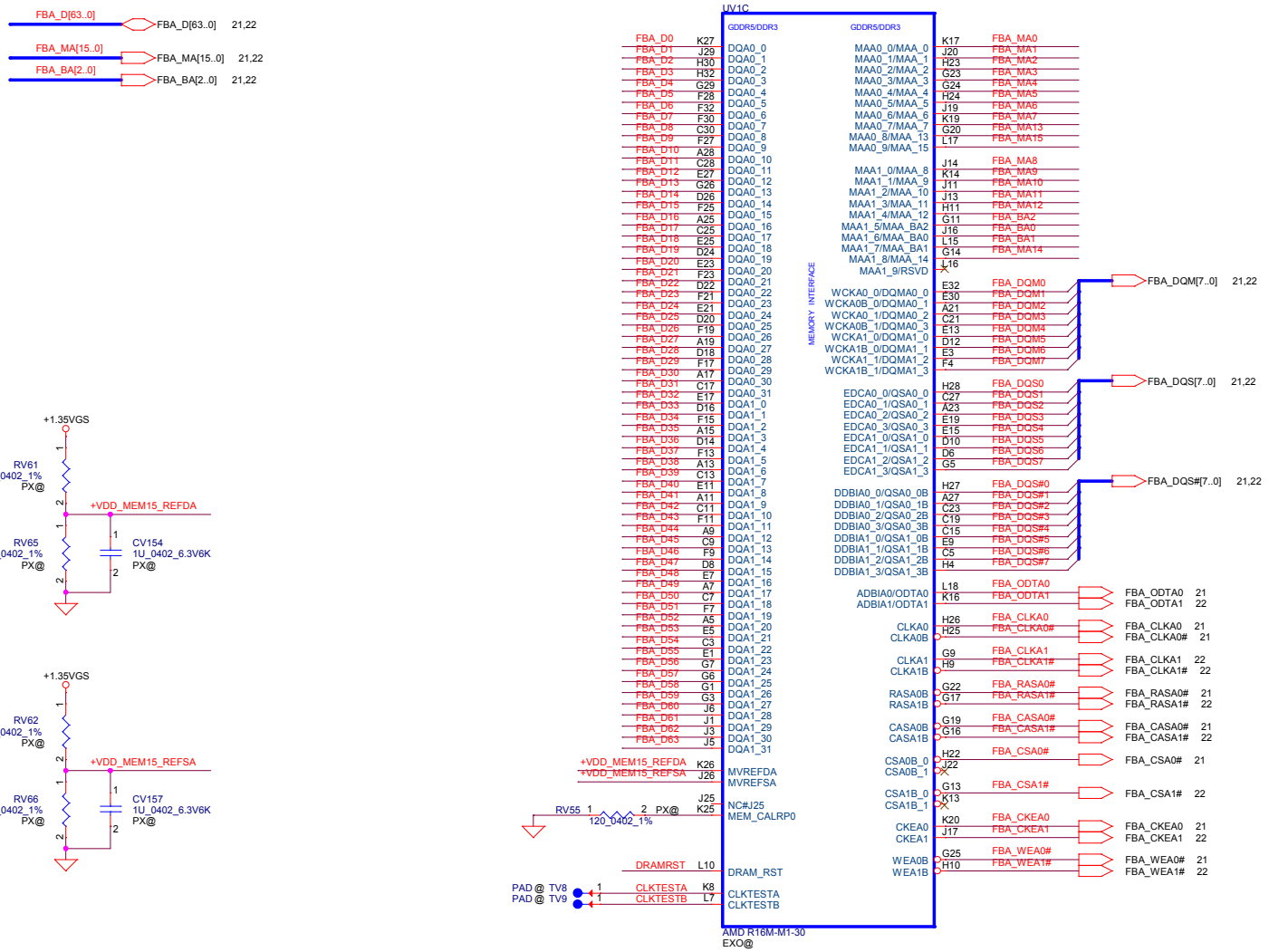

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_MEM IF

Size	Document Number	Rev
Custom	CG521	0.1

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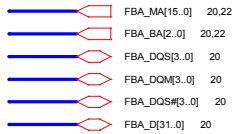
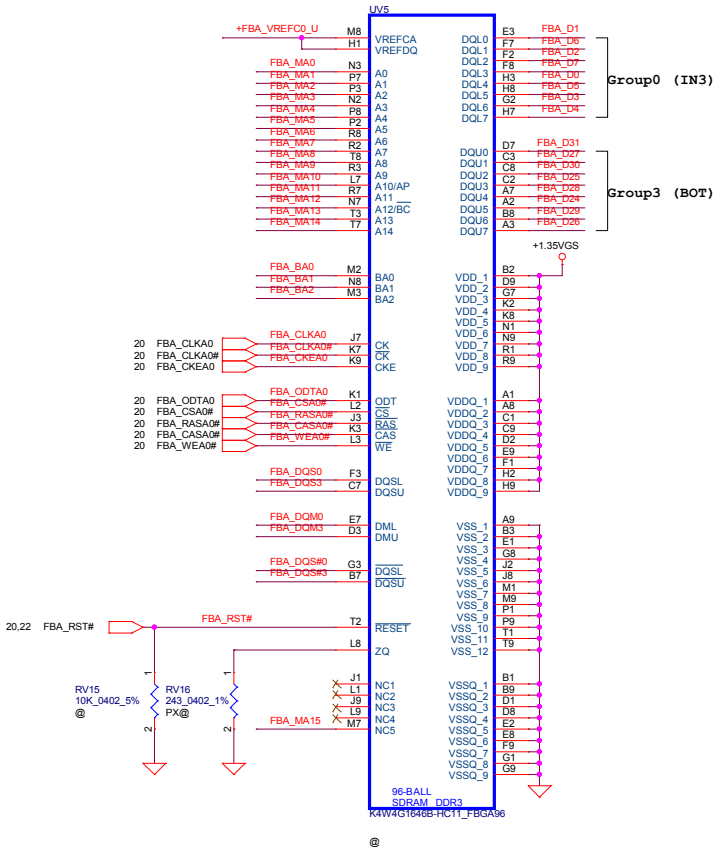
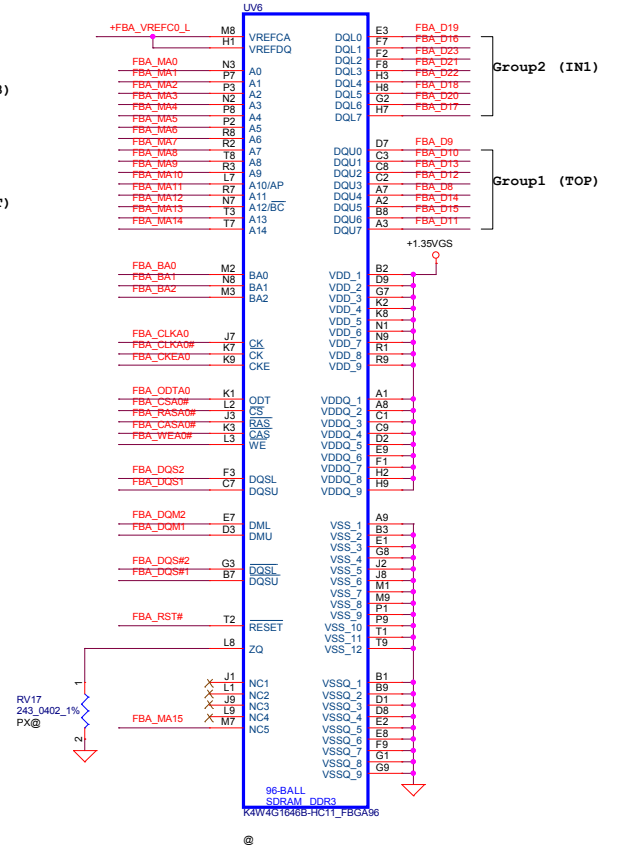
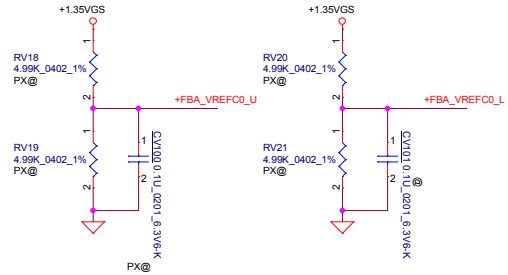
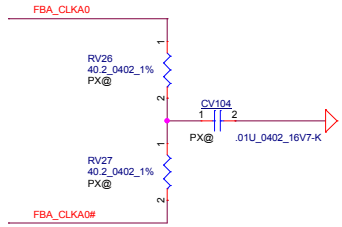
Memory Partition A - Lower 32 bits

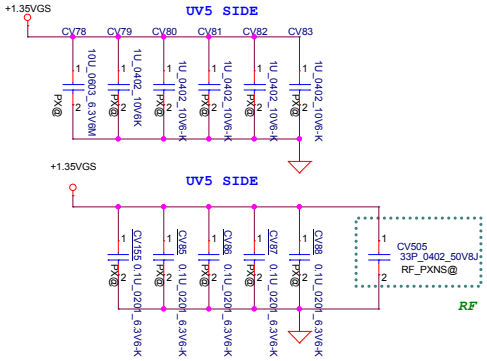


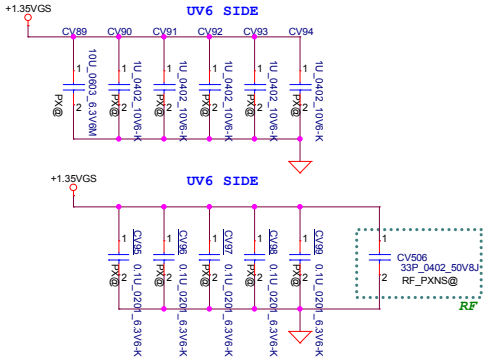












Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_A

LCFC

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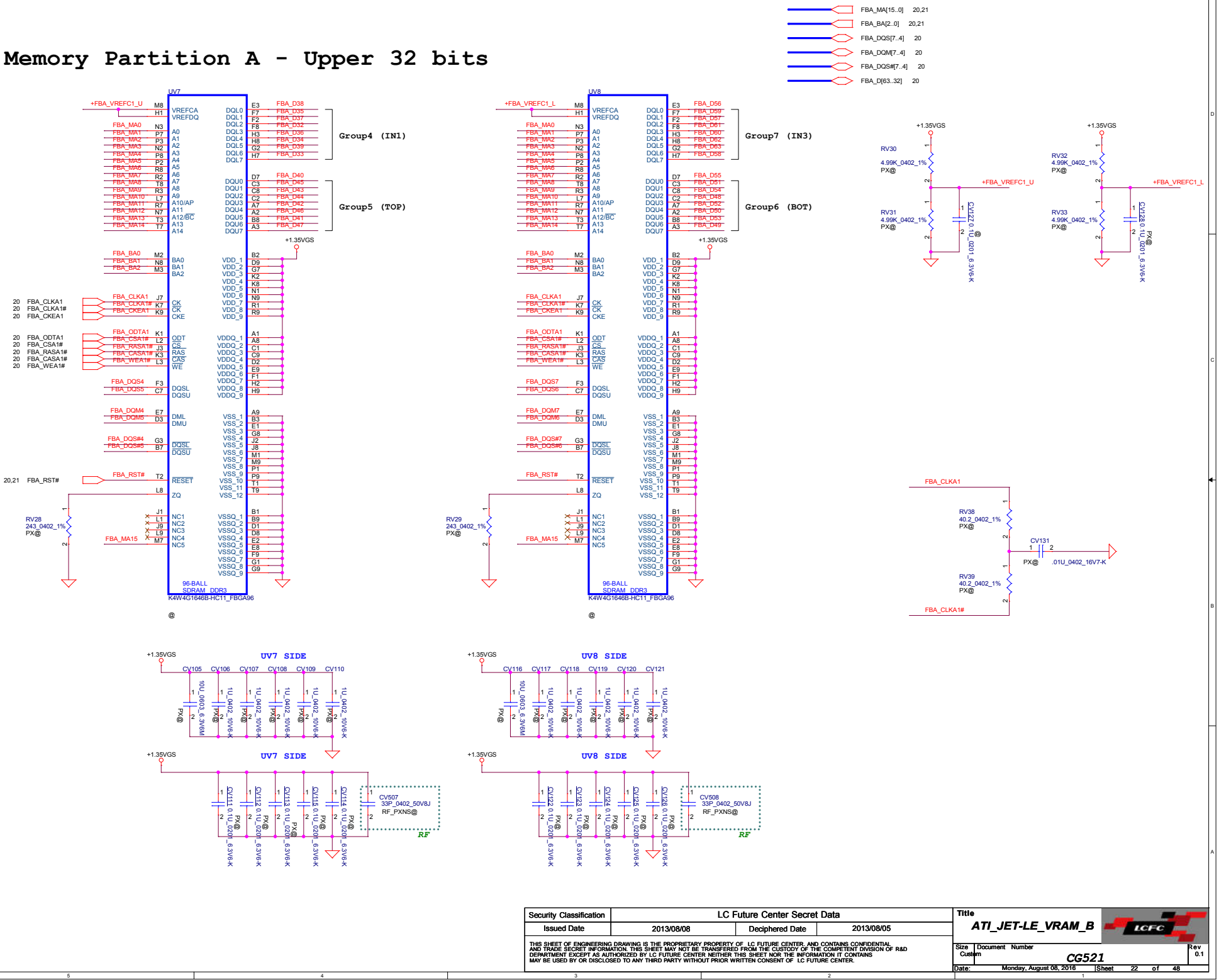
Memory Partition A - Upper 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_B

Size: Custom | Document Number: CG521 | Rev: 0.1

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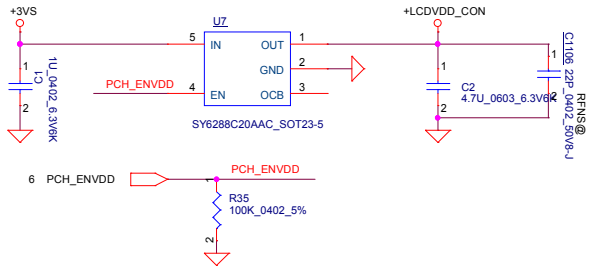
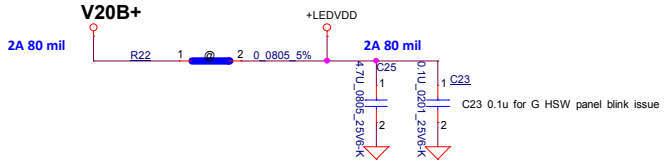
LCD POWER CIRCUIT

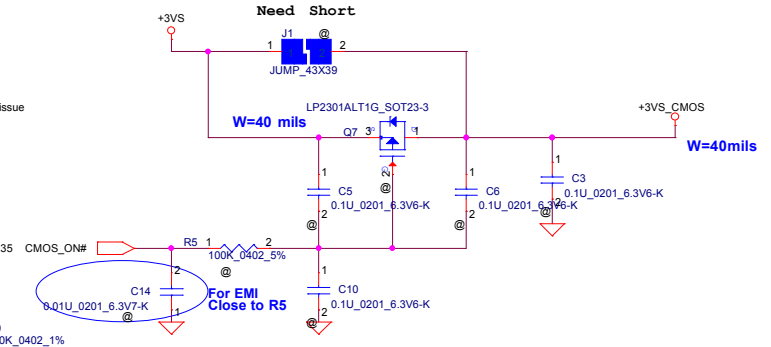


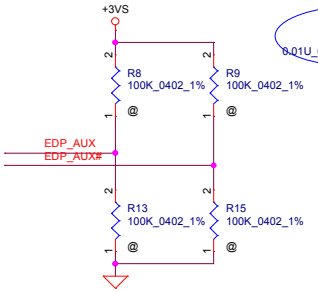
APU output enable Voh min is 1.8V-0.45V=1.35V

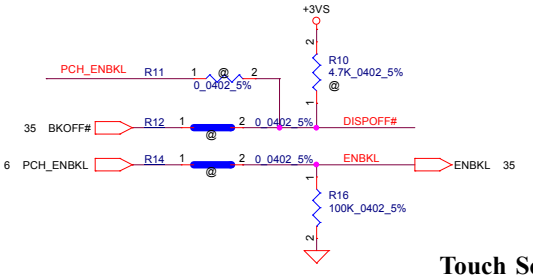
B+ to +LEDVDD POWER

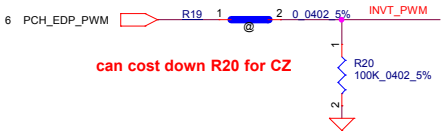


CMOS Camera

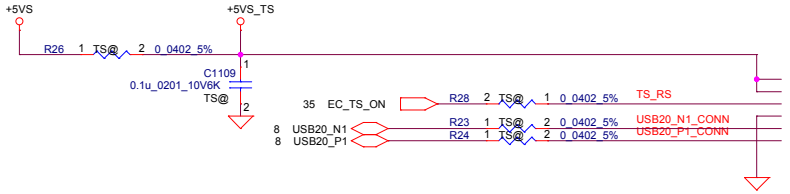


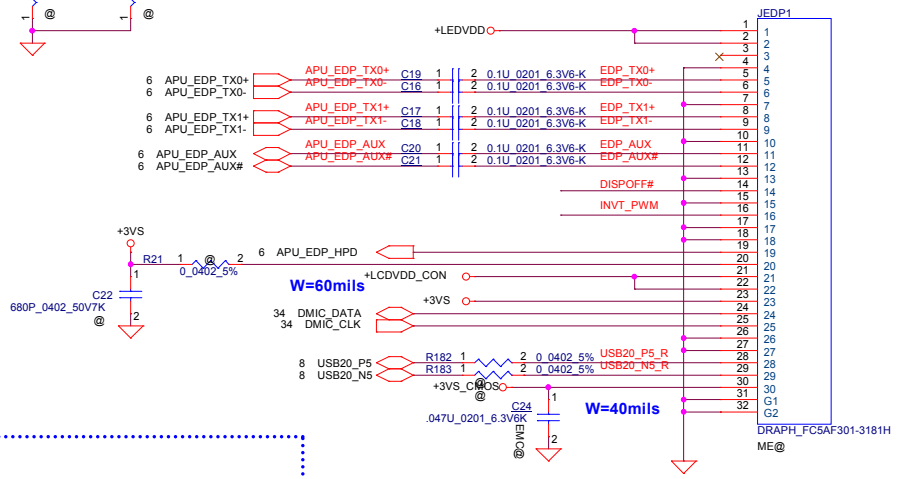




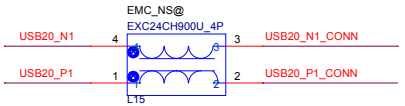


Touch Screen

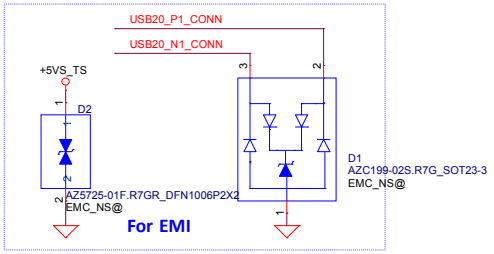


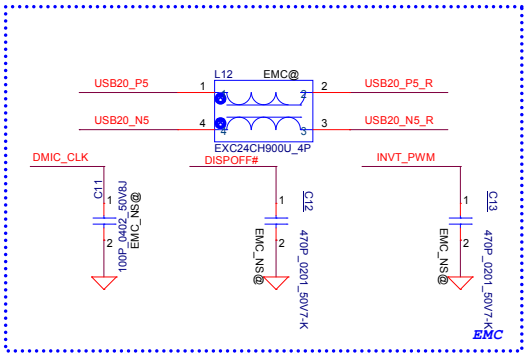


Touch Screen



For EMI





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *eDP/CMOS/Touch screen*

Size	Document Number	Rev
Custom	CG521	0.1

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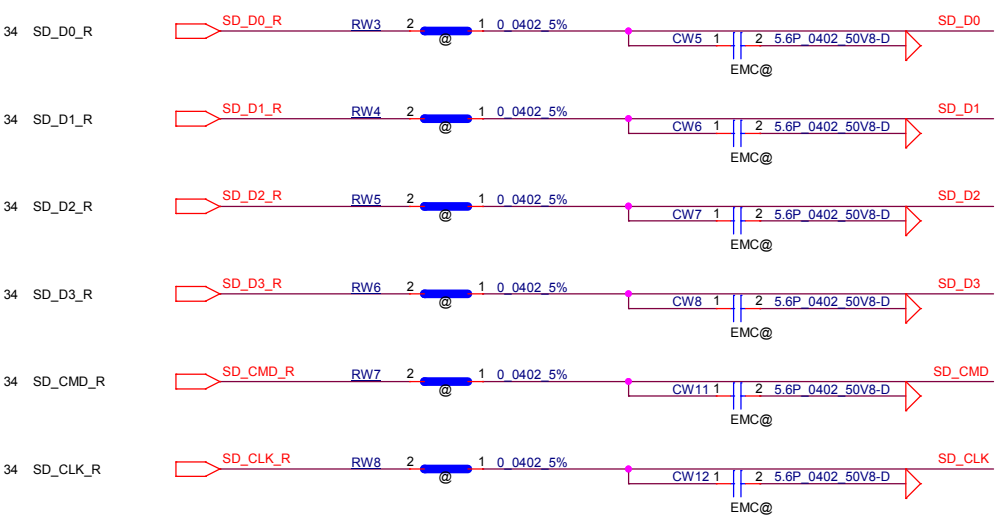
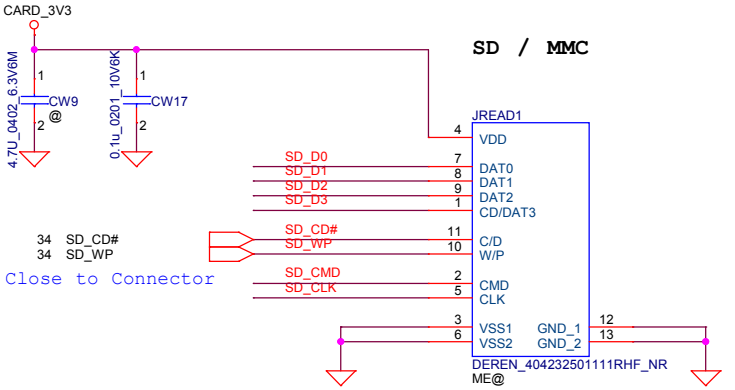
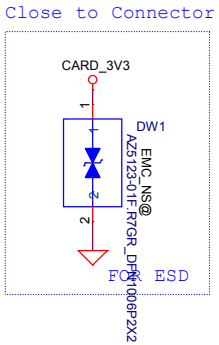




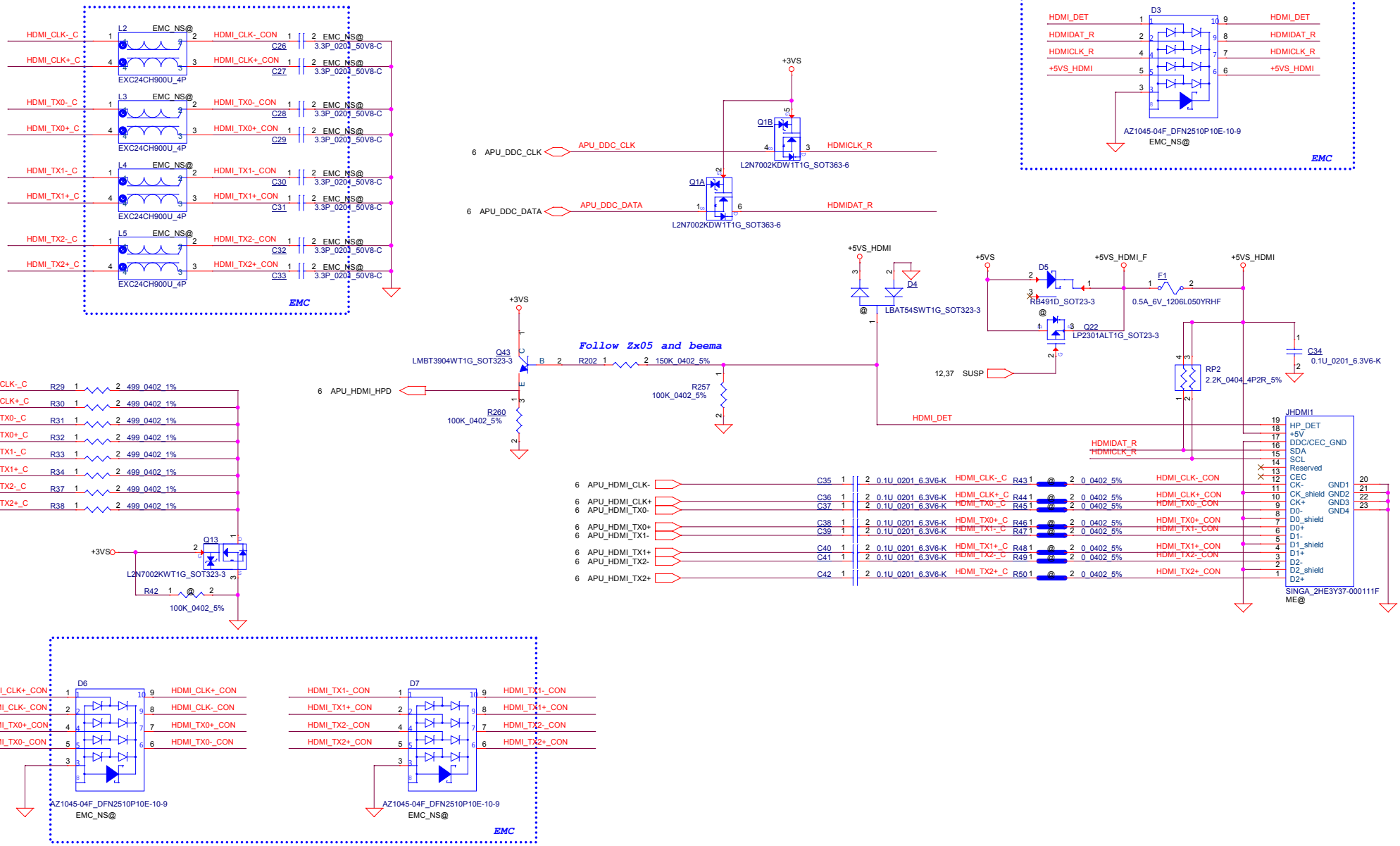


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **CardReader**

Size	Document Number	Rev
B	BMWQ3	0.1

Date: Monday, August 08, 2016 Sheet 24 of 48



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: HDMI_CONN

Size: Custom | Document Number: CG521 | Rev: 0.1

Date: Monday, August 08, 2016 | Sheet 25 of 48

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title

DP to CRT Convert(IT6515FN)

Size	Document Number	Rev
Custom	*CG521*	0.1

Date: Monday, August 08, 2016 Sheet 26 of 48

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title

CRT

Size	Document Number	Rev
Custom	***CG521***	0.1

Date: Monday, August 08, 2016 Sheet 27 of 48

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms ≤ spec ≤ 10.0ms

+3VALW
Need short
+3VALW_LAN
JL1 1 2 @
JUMP_43X79
width : 40 mils

CL4 1 2 4.7U_0603_6.3V6K
CL5 1 2 4.7U_0603_6.3V6K
SIVCD@
CL6 1 2 0.1U_0201_6.3V6K
CL7 1 2 0.1U_0201_6.3V6K

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

+3VALW_LAN
RL1 1 @ 2 0_0603_5%
+LAN_VDDREG
40mil
CL1 4700P_0603_50V7K
CL2 56P_0201_25V8-J

+3VALW_LAN
RL5 10K_0402_5%
@
7,31,35 PCIE_WAKE#
31,35 LAN_WAKE#
RL7 1 @ 2 0_0402_5%
RL10 1 @ 2 0_0402_5%
PCIE_WAKE#_R

change the Lan Chip PN to RTL8107ECG

+3VALW_LAN
+3VS
RL4 10K_0402_5%
@
LAN_CLKREQ#_R
QL1
L2N7002KWT1G_SOT323-3
RL18 1 @@ 2 0_0402_5%
LAN_CLKREQ# 7

+3VS
RL9 1K_0402_1%
ISOLATE#
RL11 15K_0402_5%
@

+3VALW_LAN
RL21 10K_0402_5%
@
LAN_DISABLE#
PLT_RST#
CL34 0.1u_0201_10V6K
EMC_NS@

UL1
RL8 1 2 2.49K_0402_1%
TL3 @ 1
TL4 @ 1
7,15,31 PLT_RST#
4 PCIE_PRX_DTX_N2
4 PCIE_PRX_DTX_P2
CL10 1 2 0.1U_0201_6.3V6-K
CL11 1 2 0.1U_0201_6.3V6-K
CL10 close to Pin18
CL11 close to Pin17

33	GND	REFCLK_N	16 CLK_PCIE_LAN# → CLK_PCIE_LAN# 8
32	AVDD33	REFCLK_P	15 CLK_PCIE_LAN → CLK_PCIE_LAN 8
31	RSET	HSIN	14 PCIE_PTX_C_DRX_N2 → PCIE_PTX_C_DRX_N2 4
30	AVDD10_1	HSIP	13 PCIE_PTX_C_DRX_P2 → PCIE_PTX_C_DRX_P2 4
29	CKXTAL2	CLKREQB	12 LAN_CLKREQ#_R
28	CKXTAL1	NC_4	11 +3VALW_LAN
27	LED0	NC_3	10 LAN_MDI3- → LAN_MDI3- 29
26	GPO	NC_2	9 LAN_MDI3+ → LAN_MDI3+ 29
25	LED1	AVDD10_0	8 +LAN_VDD10
24	NC_6	NC_1	7 LAN_MDI2- → LAN_MDI2- 29
23	DVDD33	NC_0	6 LAN_MDI2+ → LAN_MDI2+ 29
22	NC_5	MDIN1	5 LAN_MDI1- → LAN_MDI1- 29
21	LANWAKEB	MDIP1	4 LAN_MDI1+ → LAN_MDI1+ 29
20	ISOLATEB	NC_7	3 +LAN_VDD10
19	PERSTB	MDIN0	2 LAN_MDI0- → LAN_MDI0- 29
18	HSON	MDIP0	1 LAN_MDI0+ → LAN_MDI0+ 29
17	HSOP		

RTL8106E-CG_QFN32_4X4

YL1
LAN_XTALI
LAN_XTALO
OSC1 GND2
GND1 OSC2
25MHZ_10PF_7V25000014
CL12 12P_0402_50V8-J
CL13 12P_0402_50V8-J

For RTL8111H (LDO mode)

+LAN_REGOUT
60mil
CL33 0.1U_0201_6.3V6-K @
RL6 1 @@ 2 0_0805_5%
LL1 2.2UH_NLC252018T-2R2J-N_5%
60mil
CL15 4.7U_0603_6.3V6K @
CL16 0.1U_0201_6.3V6-K @

+LAN_VDD10
CL17 56P_0201_25V8-J
CL18 4700P_0201_25V7-K
CL19 0.1U_0201_6.3V6-K
CL20 0.1U_0201_6.3V6-K @
CL21 1U_0402_6.3V6K
CL22 0.1U_0201_6.3V6-K @

Close to Pin3, 8, 22, 30
Close to Pin22(Reserved)

Layout Note: RL6,CL16 must be within 200mil to Pin36,
+LAN_REGOUT: Width =60mil

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_RTL8111H_CG
Size: Custom | Document Number: BMWQ3 | Rev: 0.1
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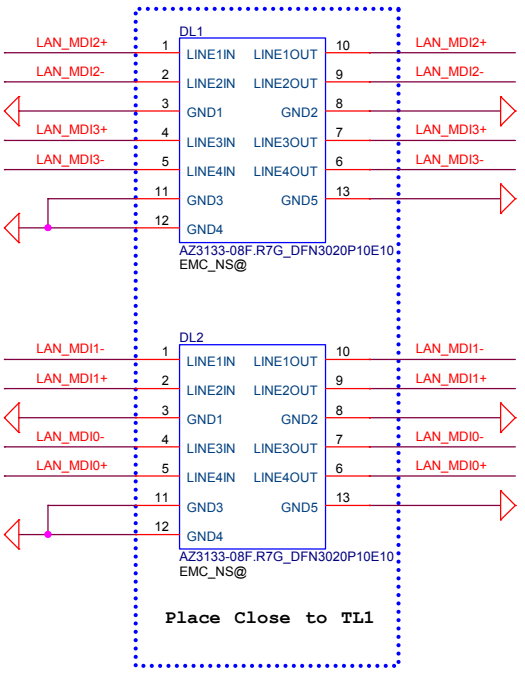
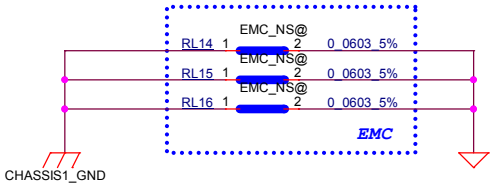
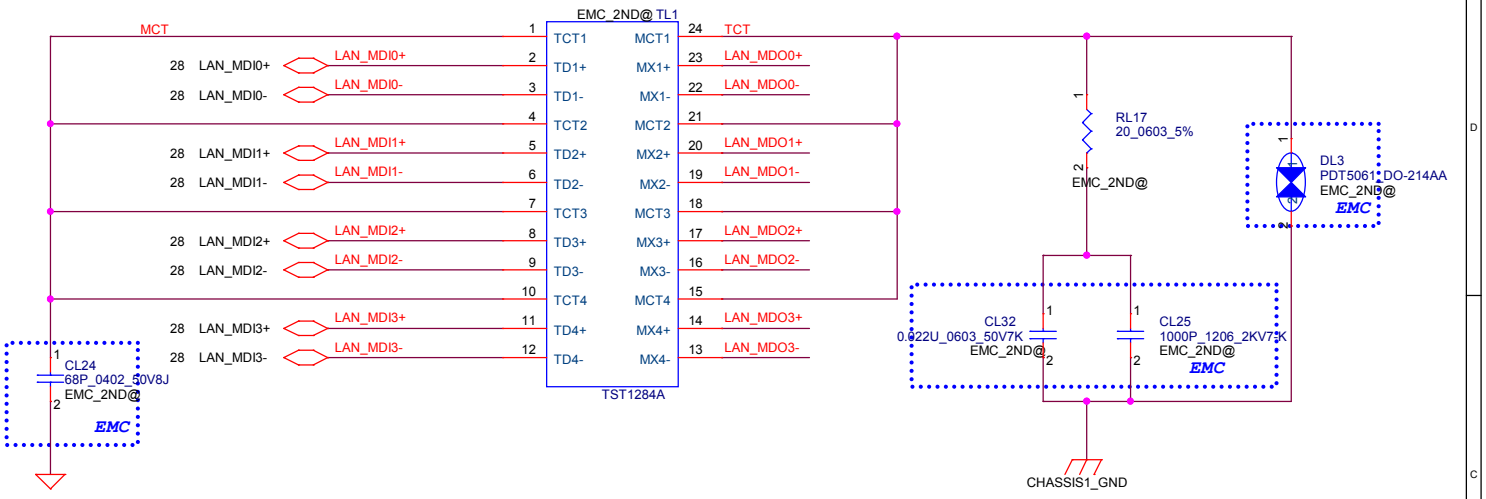
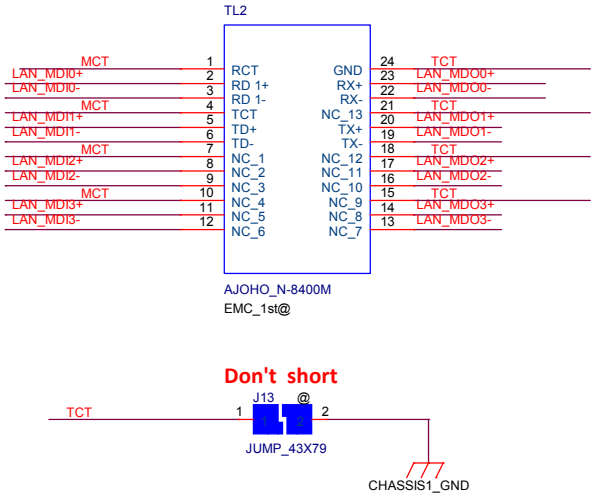
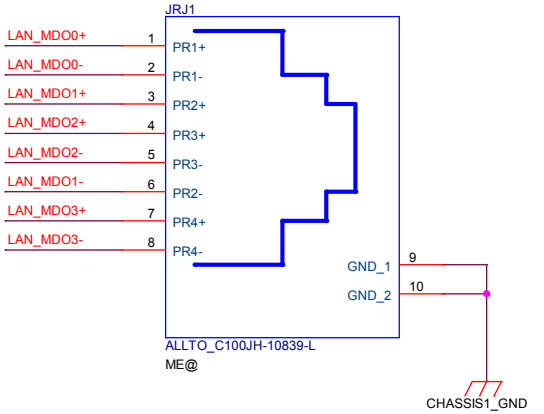
DL1/DL2
1'S PN:SC300003M00











Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_Transformer

Size	Document Number	Rev
B	CG521	0.1

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Close to U1

REMOTE+_R
C44
2200P_0402_50V7K
REMOTE-_R

R175 1 @ 2 0_0402_5% REMOTE1+
REMOTE+_R
R176 1 @ 2 0_0402_5% REMOTE2+
REMOTE-_R
R177 1 @ 2 0_0402_5% REMOTE2-
R178 1 @ 2 0_0402_5% REMOTE1-

REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Near GPU&VRAM

REMOTE1+
C45
100P_0402_50V8J
@
Q15
LMBT3904WT1G_SOT323-3
REMOTE1-

Near CPU core

REMOTE2+
C46
100P_0402_50V8J
@
Q16
LMBT3904WT1G_SOT323-3
REMOTE2-

SMSC thermal sensor
placed near DIMM

+3VS
C47
0.1U_0201_6.3V6-K
R51 10K_0402_5%
U1
VDD SCL
D+ SDA
D- ALERT#
T_CRIT# GND
NCT7718W_MSOP8
EC_SMB_CK2 6,16,35
EC_SMB_DA2 6,16,35

Address 1001_101xb

+3VALW
R17
13.7K_0402_1%
NTC_V1
R1
100K_0402_1%_TSM0B104F4251RZ
PX@
R184 0_0402_5% PX@
R185 0_0402_5% @
EC_AGND

Near CPU

+3VALW
R25
13.7K_0402_1%
NTC_V2
R3
100K_0402_1%_TSM0B104F4251RZ
R191 0_0402_5%
R192 0_0402_5% @
EC_AGND

HW thermal sensor

+5VLP
C4
0.1U_0201_6.3V6-K
U4
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
G718TM1U_SOT23-8
R252 21.5K_0402_1% @
R253 21.5K_0402_1% @
R196 0_0402_5% NTC_V1
R197 0_0402_5% NTC_V2
R6 10K_0402_5%
R7 10K_0402_5%
44 EC_ON_R
NTC_V1 35
NTC_V2 35

over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

TPM

+3VS
R52 0_0603_5%
+5VS_FAN
C49
10U_0805_10V6K
C50
0.1u_0201_10V6K
35 EC_FAN_SPEED
35 EC_FAN_PWM
JFAN1
ACES_85205-04001
ME@

+3VS
RTPM11 TPM@ 0_0603_5%
CTPM1
10U_0603_6.3V6M
TPM@
+3VS_TPM
CTPM3
0.1U_0201_6.3V6K

UTPM1 TPM@
NC_1 NC_2 NC_3 PP
NC_4 VNC_1
GND_1 GND_2 GND_3
NC_5 VNC_2 NC_6 NC_7 NC_8
VPS_1 VPS_2
LPCPD# SERIRQ
LAD0 LAD1 LFRAME# LAD2 LAD3
NC_11 LCLK NC_10 NC_9
LRESET#
ST33ZP24AR28PVSP_TSSOP28
RTPM2 TPM@ 4.7K_0402_5%
SERIRQ 8,35
LPC_AD0 8,35
LPC_AD1 8,35
LPC_FRAME# 8,11,35
LPC_AD2 8,35
LPC_AD3 8,35
RTPM3 TPM@ 0_0402_5%
TPM_CLK 8
RTPM4 TPM@ 0_0402_5%
RTPM16 TPM@ 0_0402_5%
LPC_CLKRUN# 8
APU_LPC_RST# 8,35

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: Thermal sensor/FAN CONN/TPM

Size: Custom | Document Number: CG521 | Rev: 0.1

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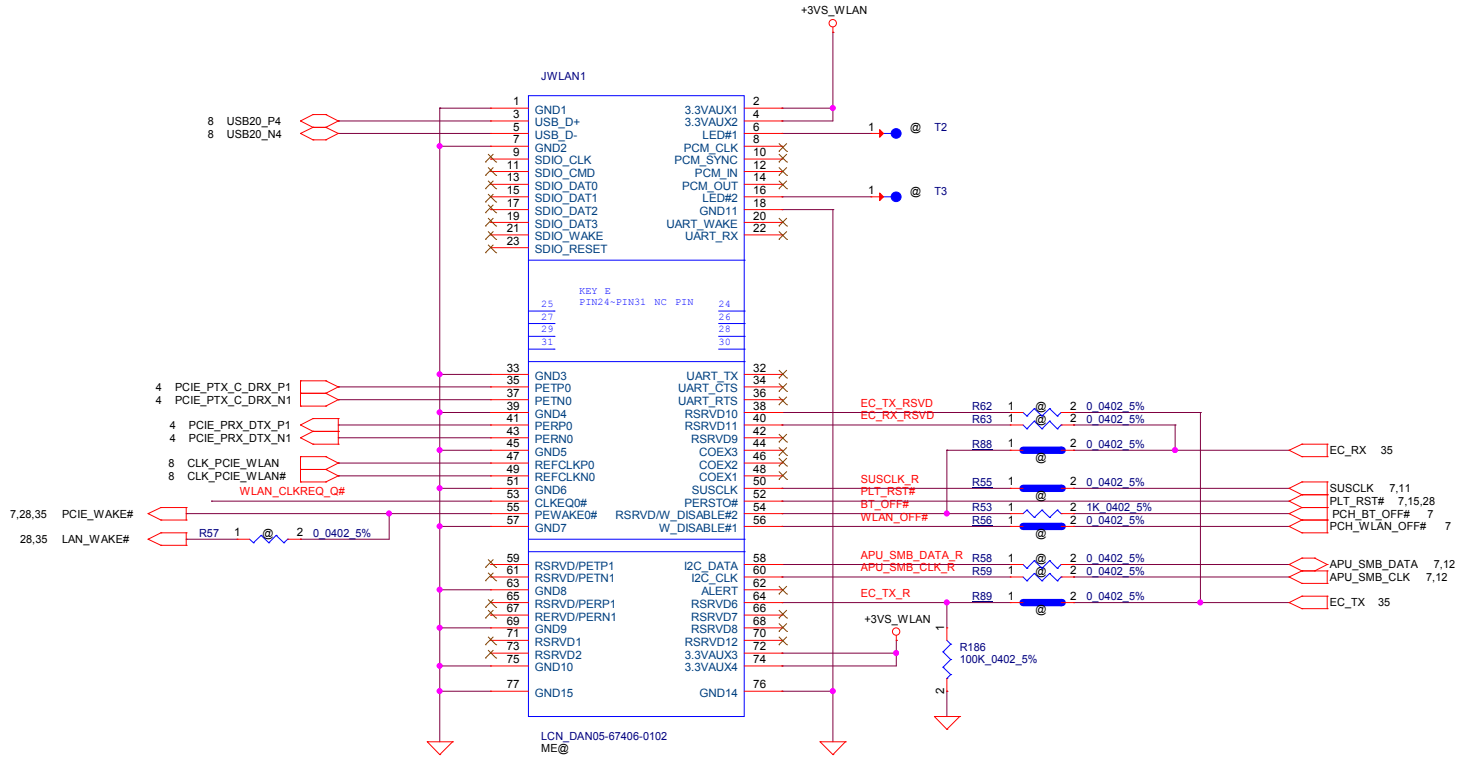
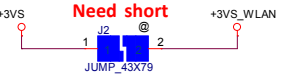
Mini-Express Card(WLAN/WiMAX)



Not support AOAC, delete AOAC power circuit 1015



7 WLAN_CLKREQ# R61 0_0402_5% WLAN_CLKREQ_Q#

If support AOAC, NC R61;
if not support AOAC, stuff R61.

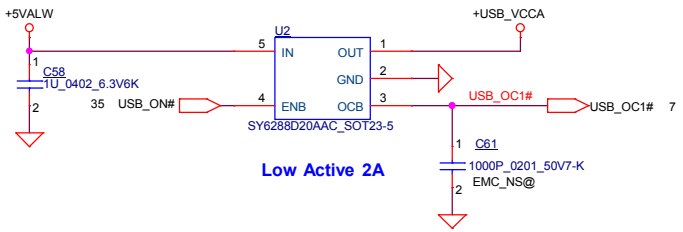
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

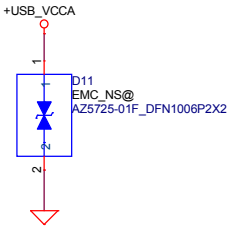
Title: NGFF WLAN

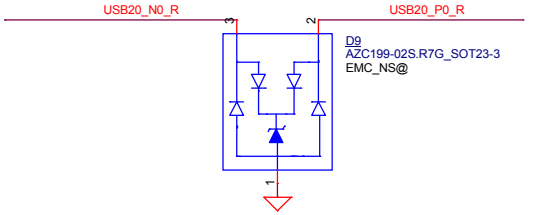
Size: Custom | Document Number: CG521 | Rev: 0.1

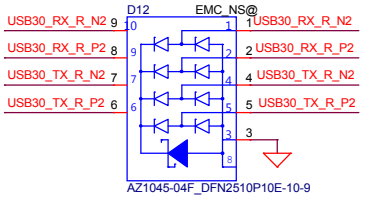
Date: Monday, August 08, 2016 | Sheet 31 of 48

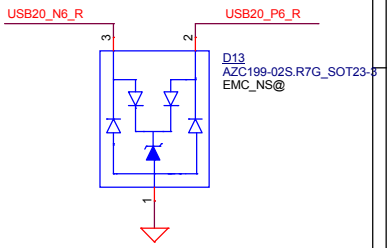
LEFT SIDE USB PORT X2



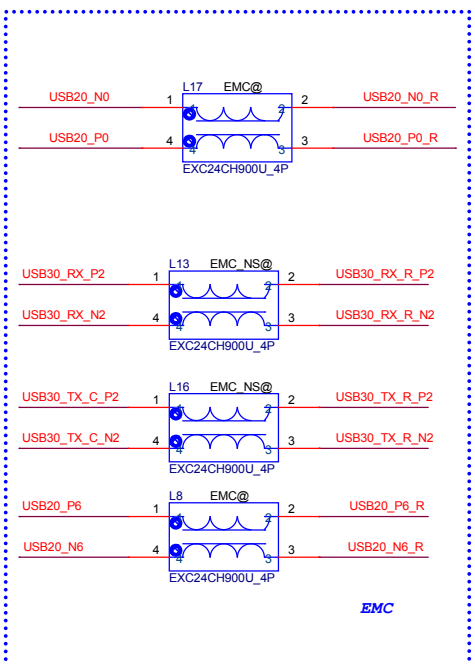


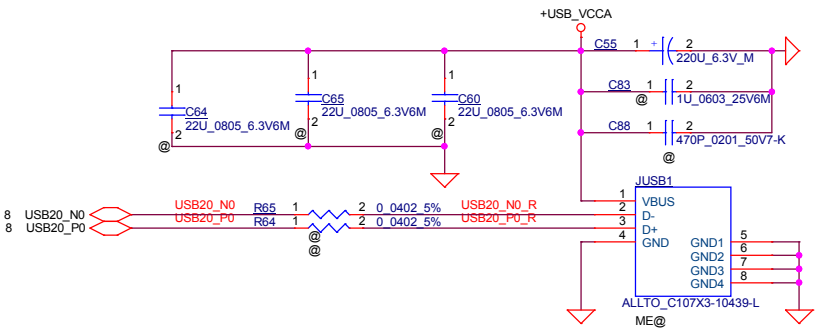


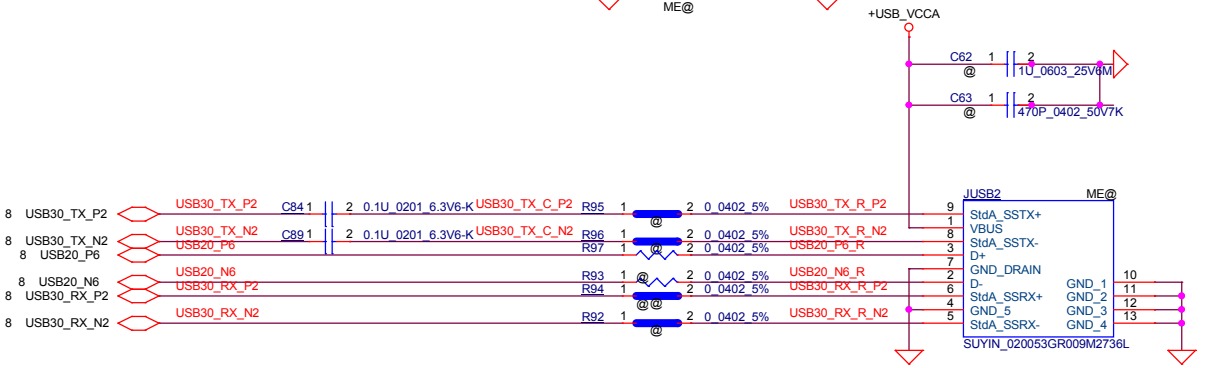




EMC solution need double check 1015







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **P32-USB3.0 PORT (LEFT)**

Size	Document Number	Rev
Custom	CG521	0.1

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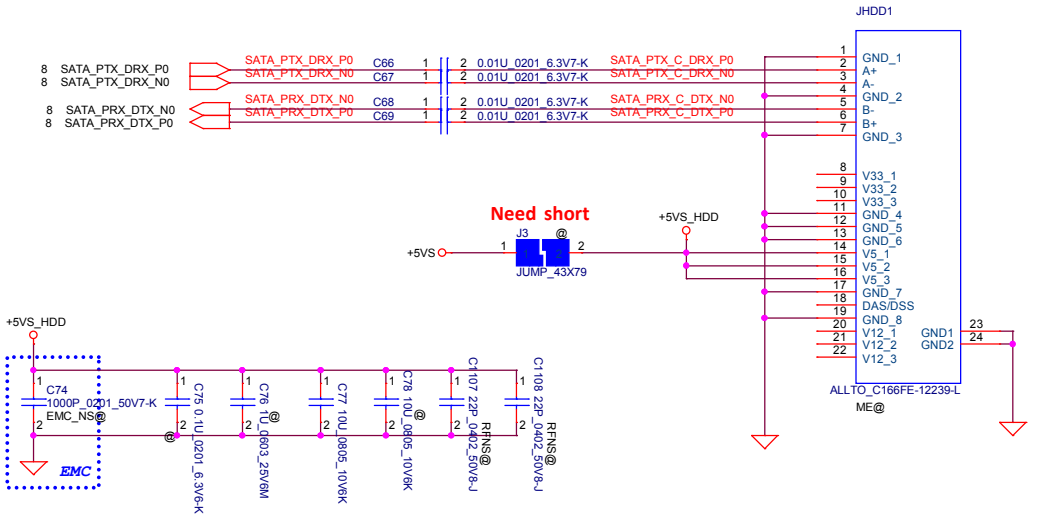
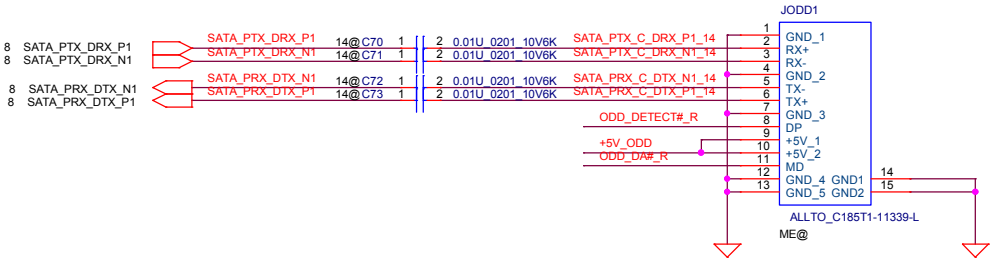
SATA HDD Conn.



FOR 14"

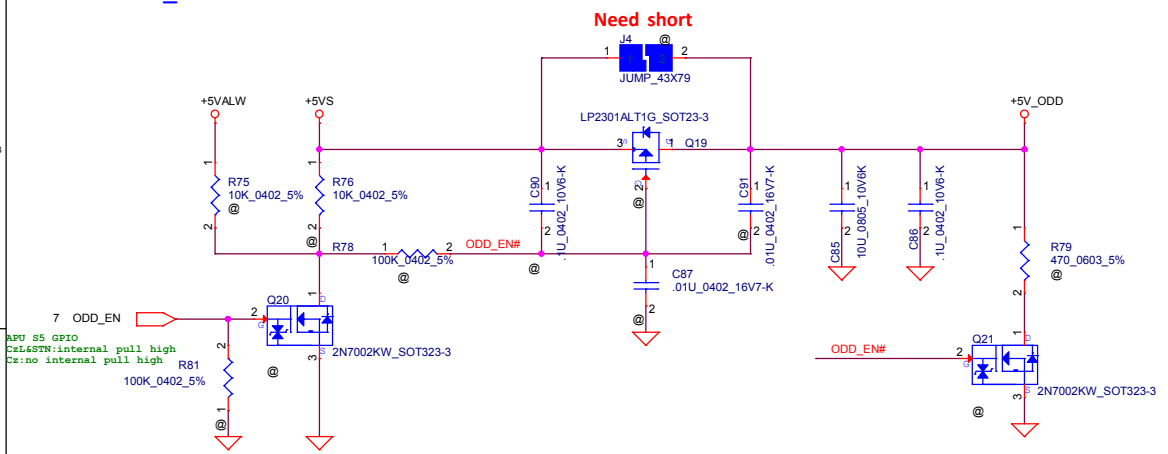
SATA ODD Conn.



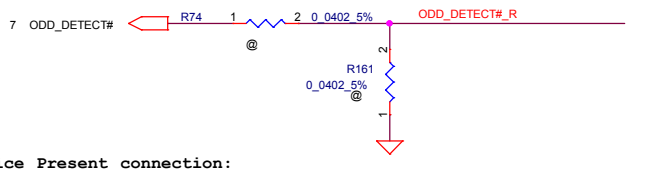
FOR 15"

SATA ODD FFC Conn

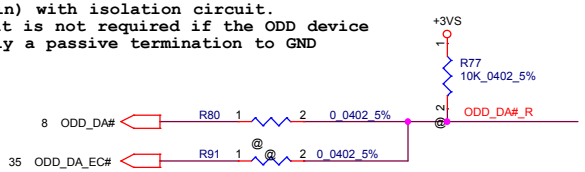
+5VS to +5V_ODD



SATA ODD power regulator control
FCH GPIO (S5 domain) with integrated pull-up
FCH GPIO (S0 domain) with isolation circuit to filter glitches during S5 to S0 transition



SATA ODD Device Present connection:
FCH GEVENT (S0 domain) or
FCH GEVENT (S5 domain) with isolation circuit.
The isolation circuit is not required if the ODD device present pin has only a passive termination to GND



SATA ODD Device Attention connection:
FCH GEVENT (S0 domain) or
FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: HDD/ODD CONN

Size: Custom | Document Number: BMWQ3 | Rev: 0.1

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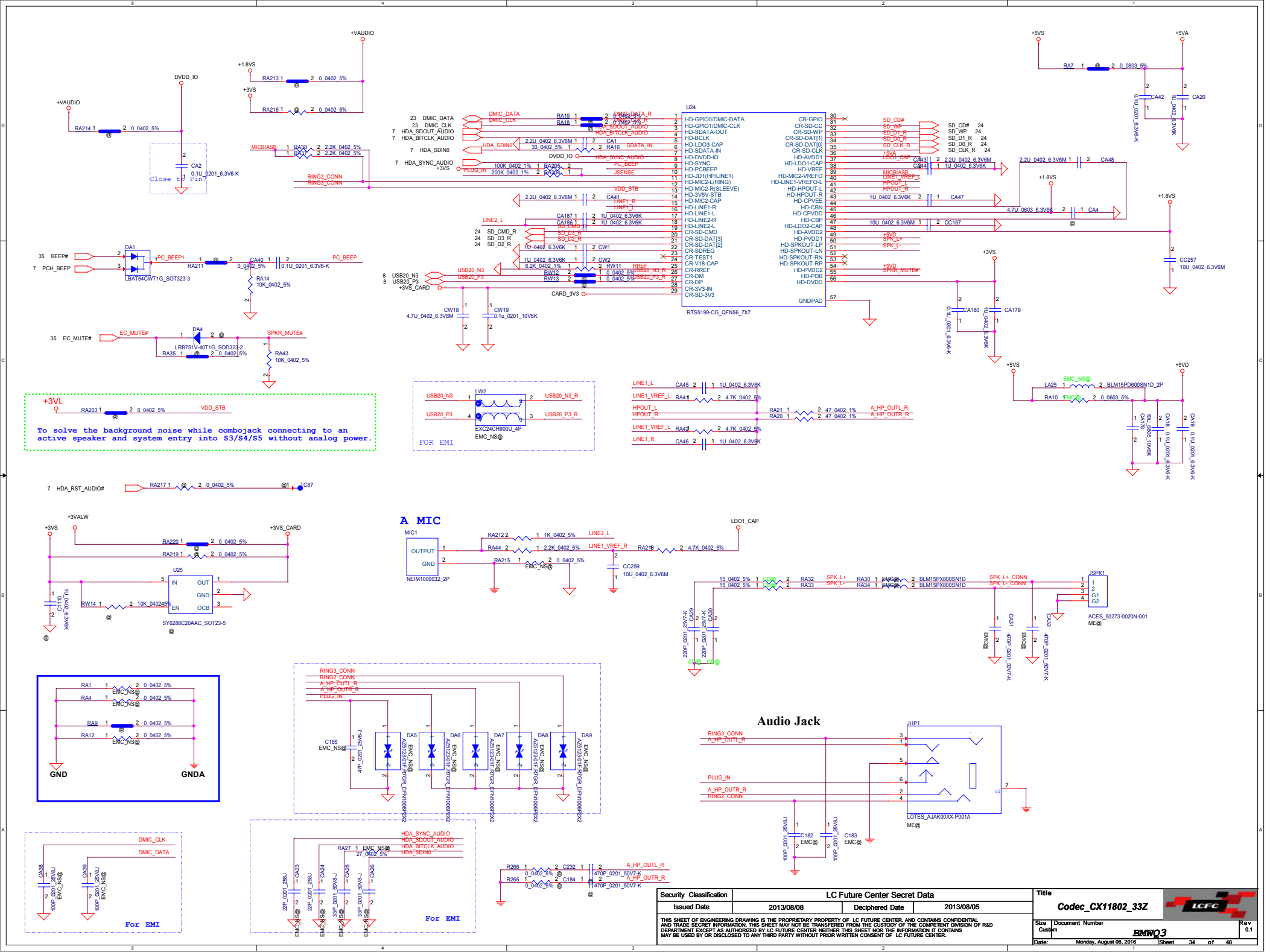

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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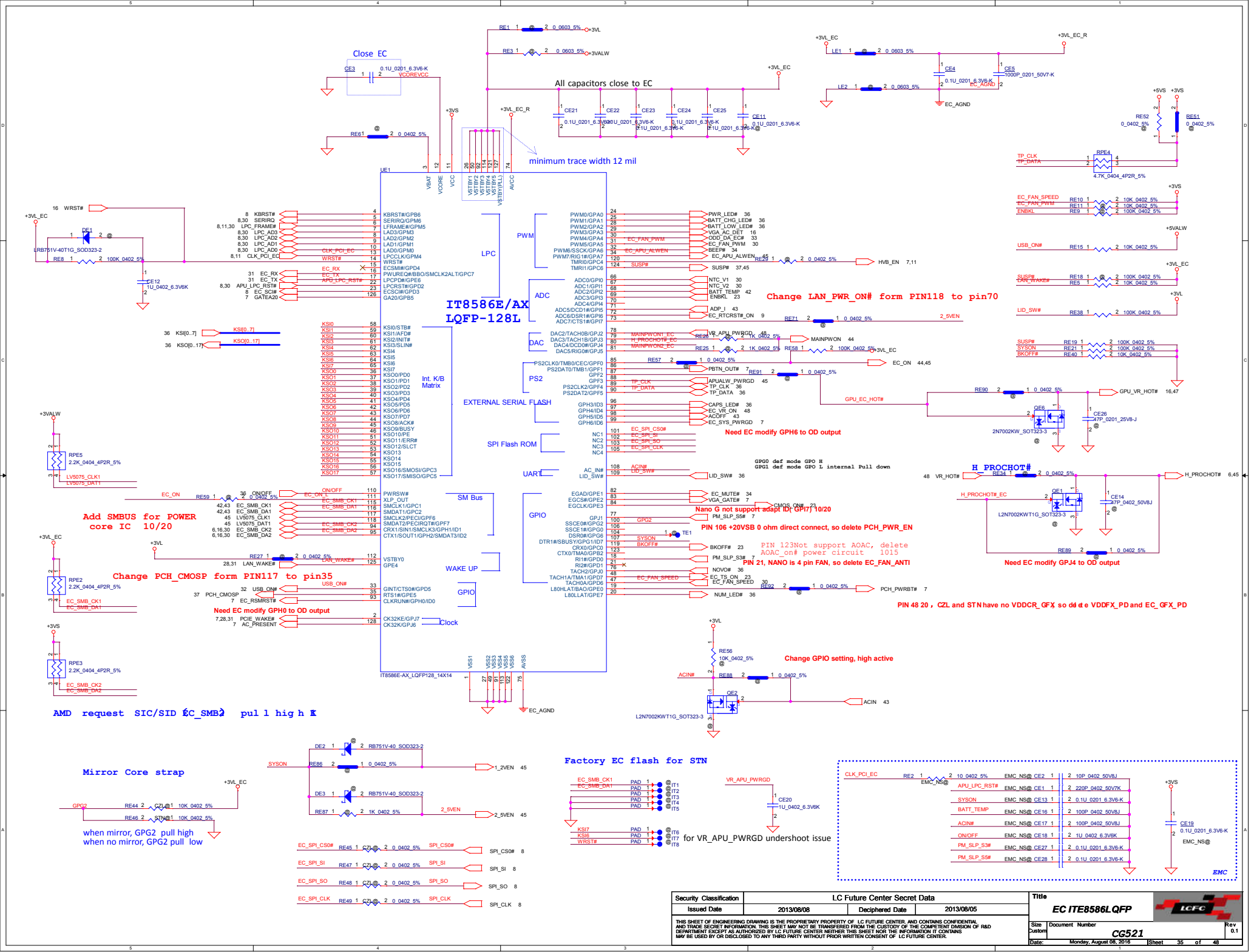
Title	Codec_CX11802_33Z		
Size	Document Number		Rev
Custom	BMWQ3		0.1
Date:	Monday, August 08, 2016	Sheet	34 of 48


Close EC
All capacitors close to EC
minimum trace width 12 mil
IT8586E/AX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
GPIO
SM Bus
WAKE UP
Clock
Int. K/B Matrix
Change LAN_PWR_ON# form PIN118 to pin70
Need EC modify GPH6 to OD output
GPG0 def mode GPO H
GPG1 def mode GPO L internal Pull down
Add SMBUS for POWER core IC 10/20
Change PCH_CMOSP form PIN117 to pin35
Need EC modify GPH0 to OD output
Nano G not support adapt ID(GPI7) 10/20
PIN 106 +20VSB 0 ohm direct connect, so delete PCH_PWR_EN
PIN 123Not support AOAC, delete AOAC_on# power circuit 1015
PIN 21, NANO is 4 pin FAN, so delete EC_FAN_ANTI
PIN 48 20 , CZL and STN have no VDDCR_GFX so delete VDDFX_PD and EC_GFX_PD
H_PROCHOT#
Need EC modify GPJ4 to OD output
Change GPIO setting, high active
AMD request SIC/SID EC_SMB2 pull high
Mirror Core strap
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Factory EC flash for STN
for VR_APU_PWRGD undershoot issue
EMC
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
2013/08/05
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Title
EC ITE8586LQFP
Size
Custom
Document Number
CG521
Rev
0.1
Date:
Monday, August 08, 2016
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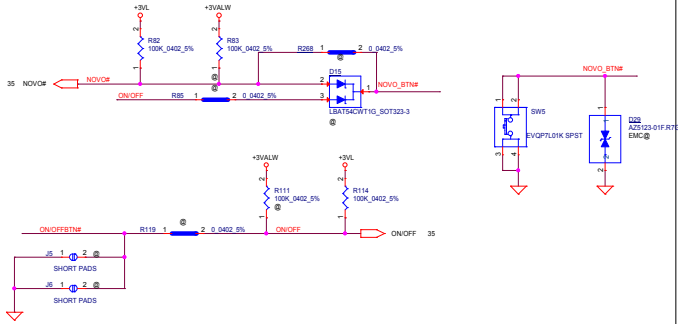
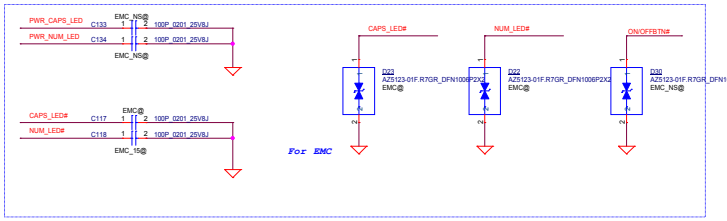
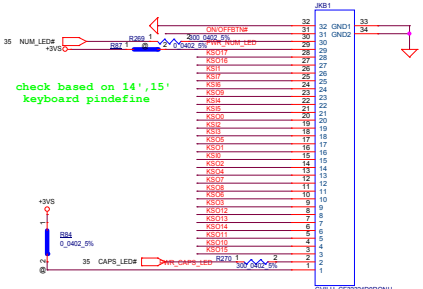
ON/OFF switch



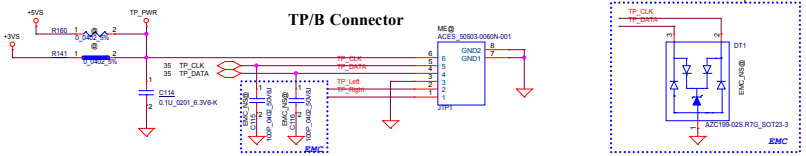
K/B Connector

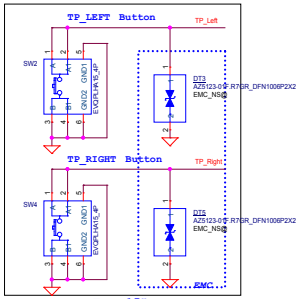




check based on 14'',15' keyboard pindefine

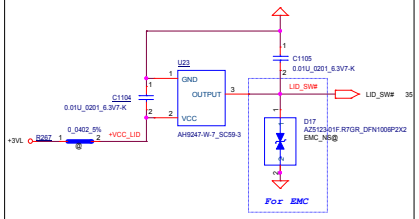
TP/B Connector





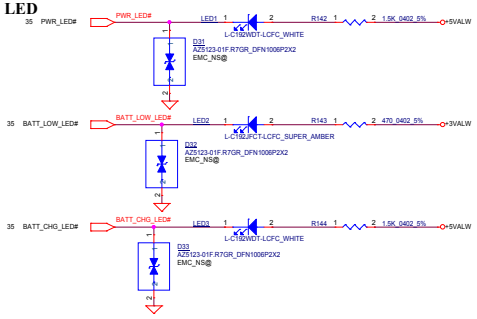
For 14"

PWR/B Connector

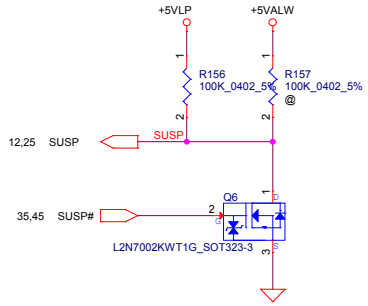


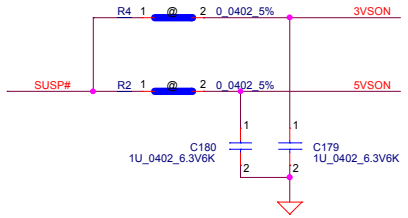
USB I/O Connector

LED



Title	Size	Document Number	Rev
KBD/PWR/IO/LED/TP Conn.	Custom	CG521	0.1
	Date: Monday, August 08, 2016	Sheet 36 of 48	



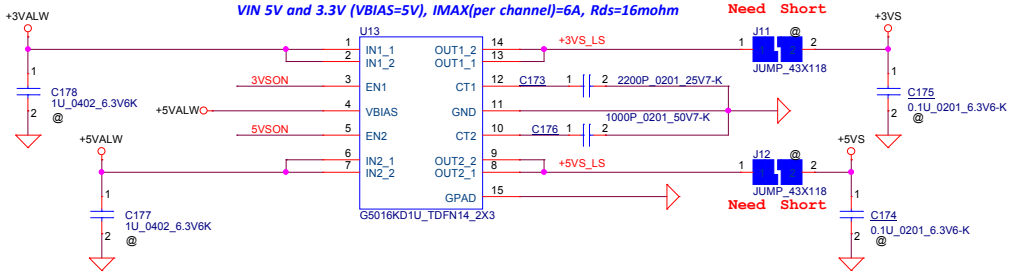


Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

Need Short

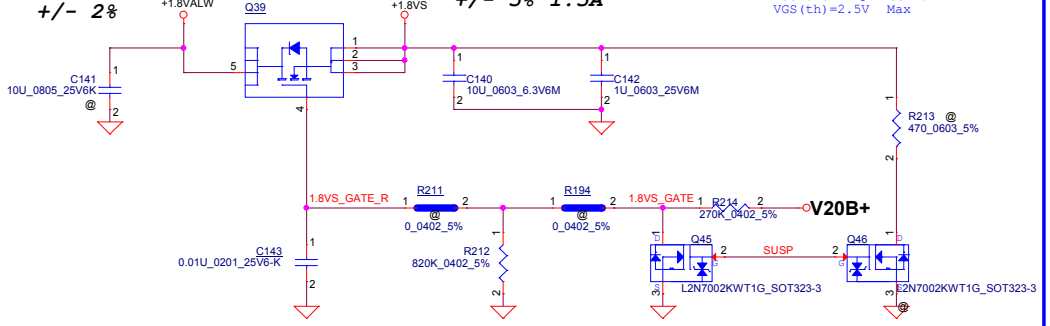


+1.8VALW to +1.8VS

+/- 2%

+/- 5% 1.5A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

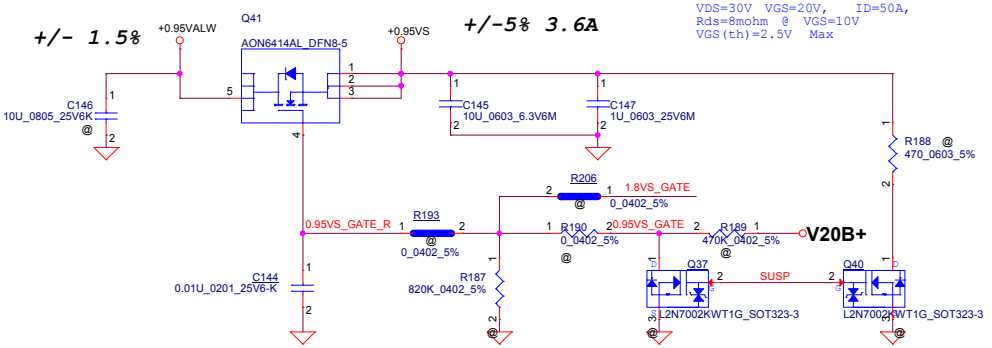


+0.95VALW to +0.95VS

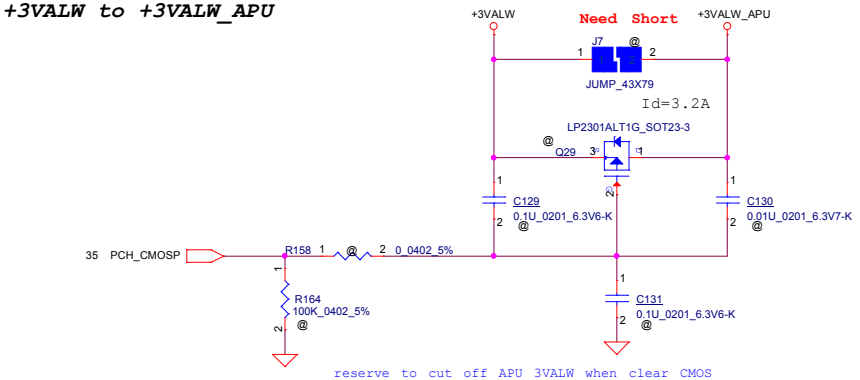
+/- 1.5%

+/-5% 3.6A

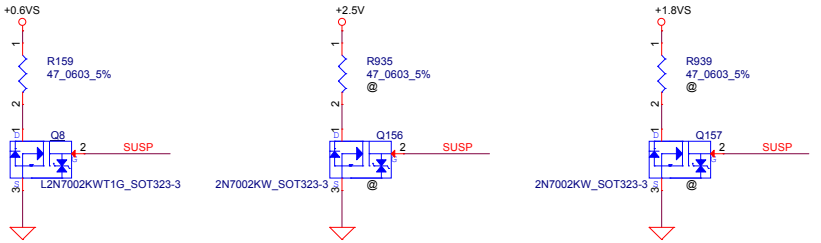
AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max



+3VALW to +3VALW_APU



For DisCharge



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
Custom	CG521	0.1

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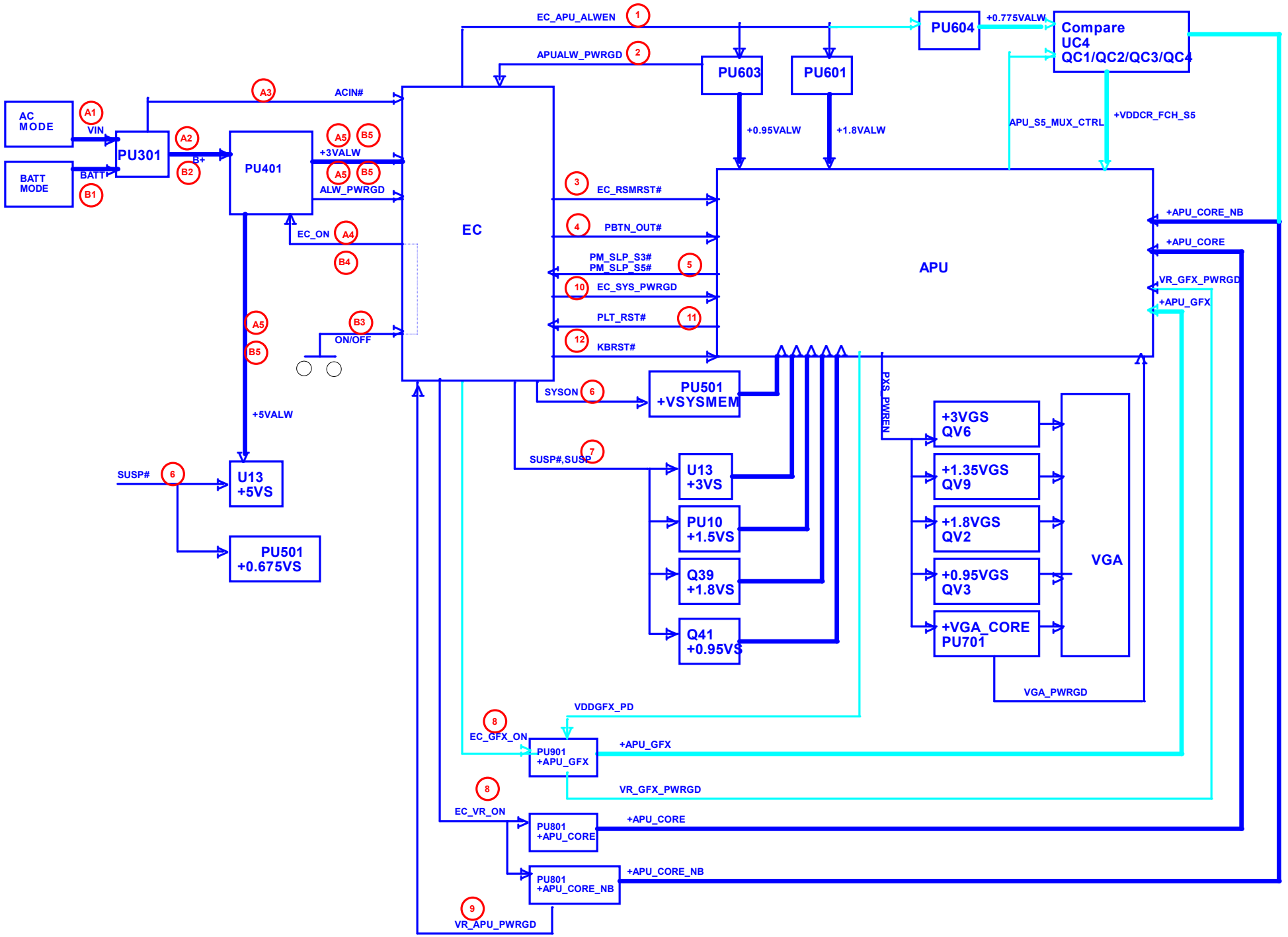

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **Power sequence Block**

Size	Document Number	Rev
Custom	CG521	0.1

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VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

H1 HOLEA
1
@
pad_ct8p0d2p3

H2 HOLEA
1
pad_ct8p0b6p0d2p3
@

H3 HOLEA
1
pad_ct8p0b6p0d2p3
@

H4 HOLEA
1
pad_ct8p0b6p0d2p3
@

H5 HOLEA
1
pad_c8p0d2p3
@

H6 HOLEA
1
pad_c8p0d2p3
@

H7 HOLEA
1
pad_c8p0d2p3
@

H8 HOLEA
1
CHASSIS1_GND
pad_c8p0d2p3
@

H9 HOLEA
1
pad_c8p0d2p3
@

H10 HOLEA
1
pad_c8p0d2p3
@

H16 HOLEA
1
PAD_C2P8D2P8N
@

H18 HOLEA
1
PAD_O3P3X2P8D3P3X2P8N
@

H11 HOLEA
1
PAD_CB6p0D3P7
@

H12 HOLEA
1
PAD_CB6p0D3P7
@

H13 HOLEA
1
PAD_CB6p0D3P7
@

H14 HOLEA
1
PAD_CB6p0D3P7
@

H15 HOLEA
1
pad_ct8p0b6p0d3p2
@

PCB Fedical Mark PAD

FD1 1 @
FD2 1 @
FD3 1 @
FD4 1 @
FD5 1 @
FD6 1 @

For EMC

+VGA_CORE
1
C168
0.1U_0201_6.3V6-K
2
@

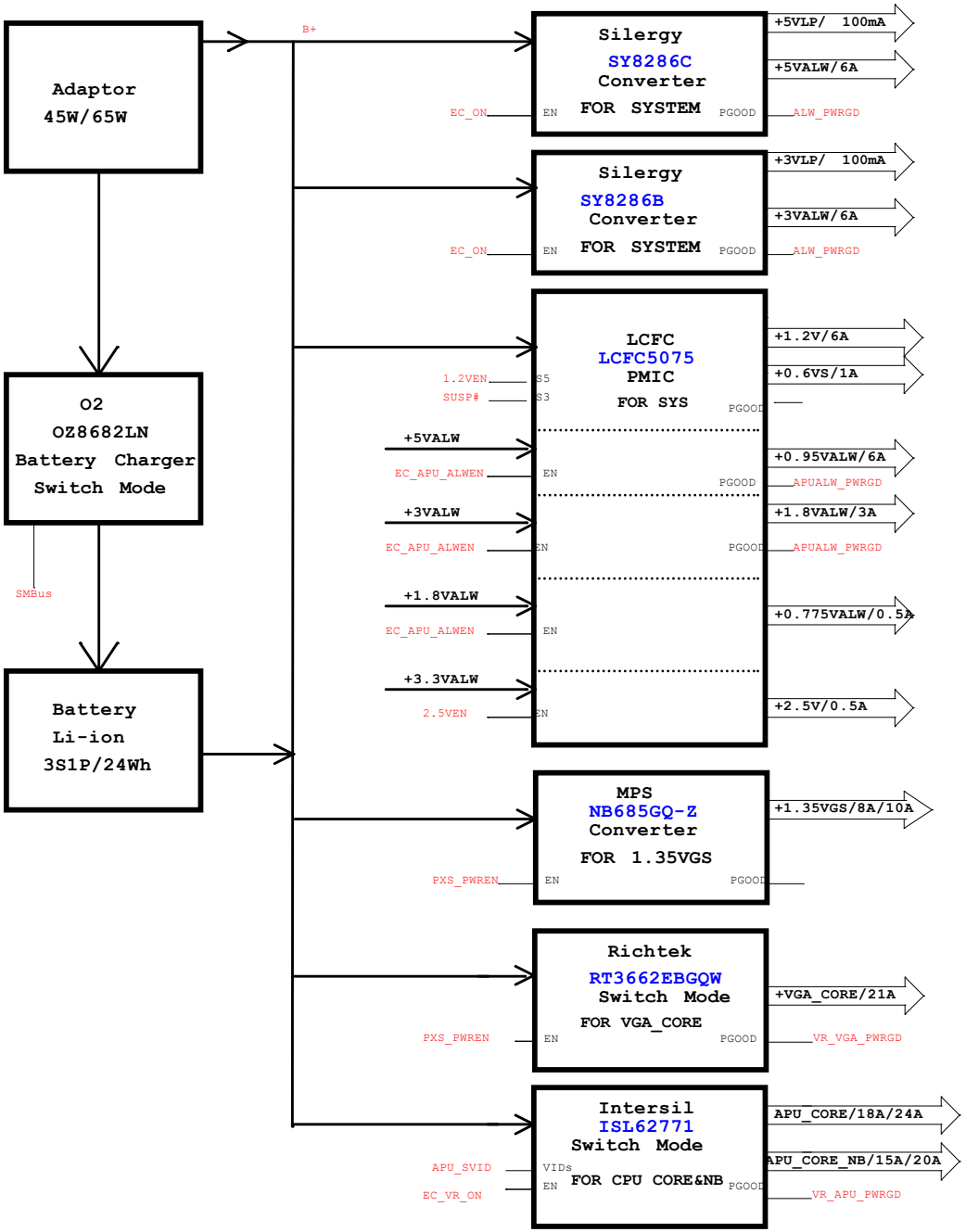
+3VS
1
C169
0.1U_0201_6.3V6-K
2
@

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ***Hole***

LCFC

Size B	Document Number ***CG521***	Rev 0.1
Date: Monday, August 08, 2016	Sheet 40 of 48	

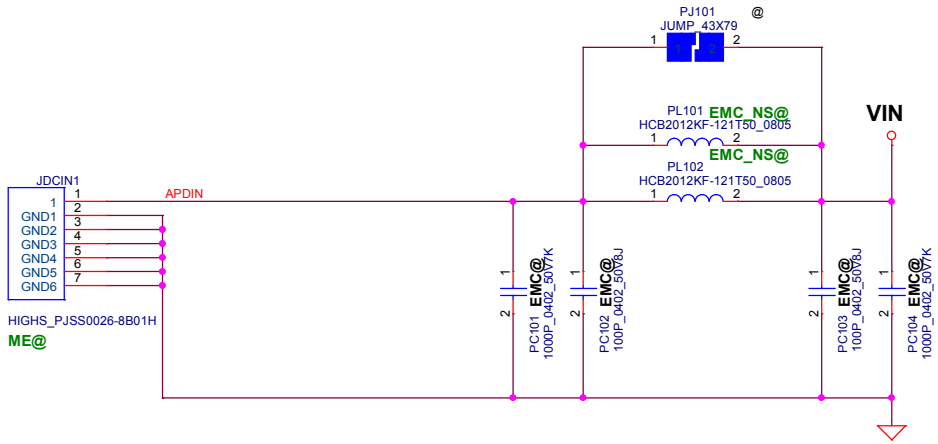


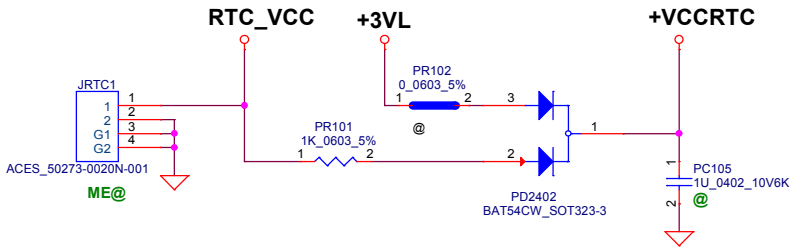
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

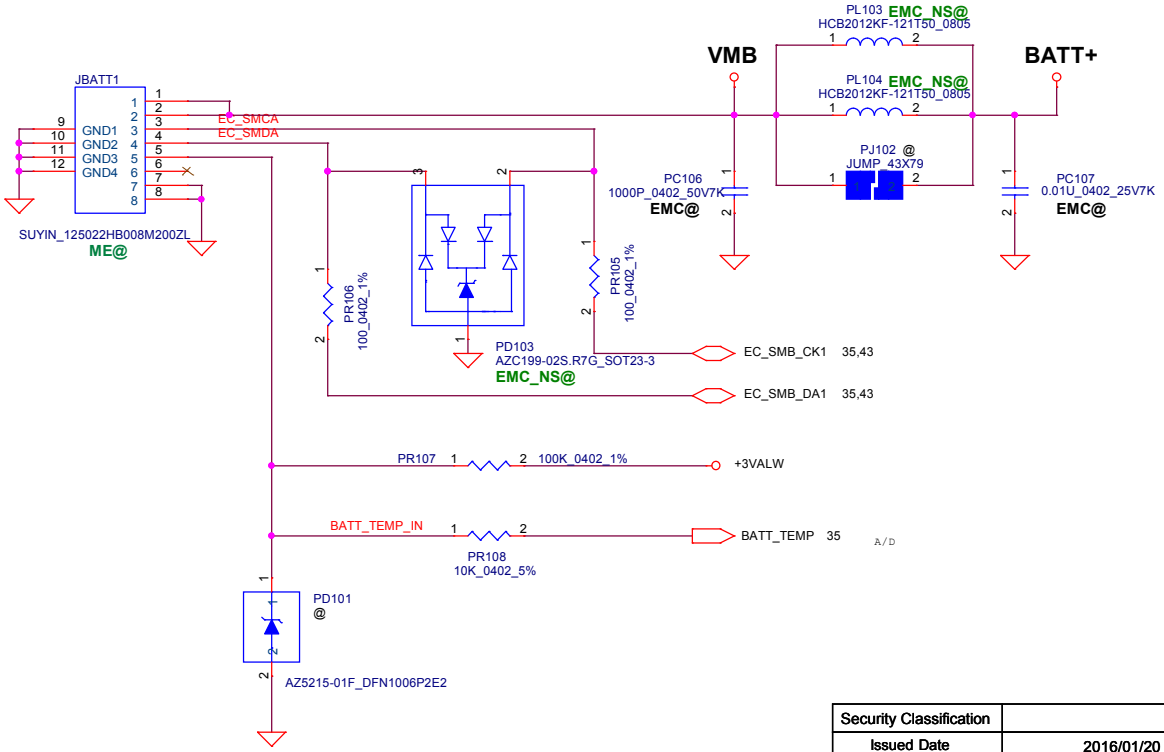
Title: **Power Diagram**

Size	Document Number	Rev
Custom	CG412	0.3

Date: Monday, August 08, 2016 Sheet 41 of 48





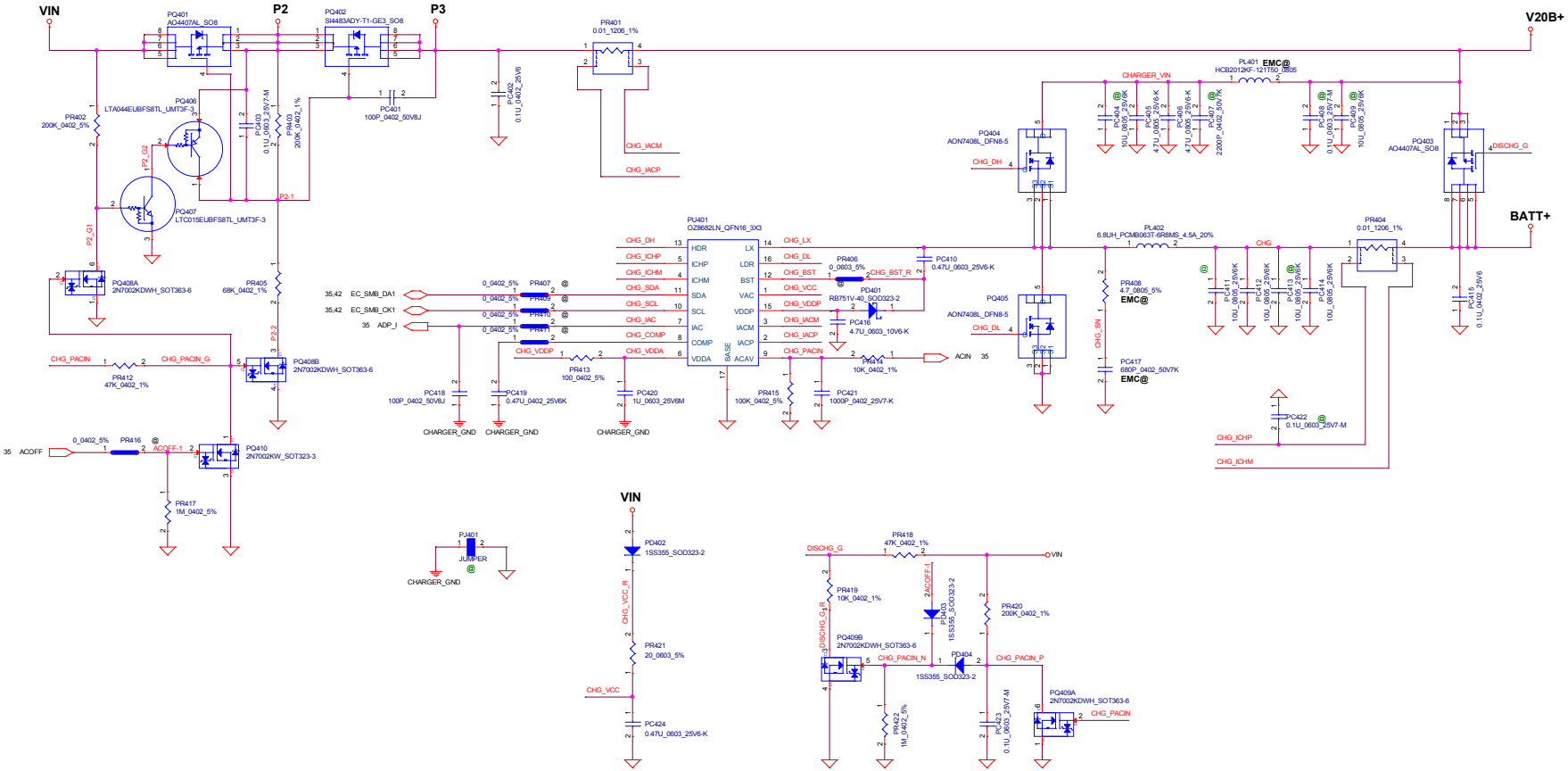


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **DCIN /BATT/ RTC**

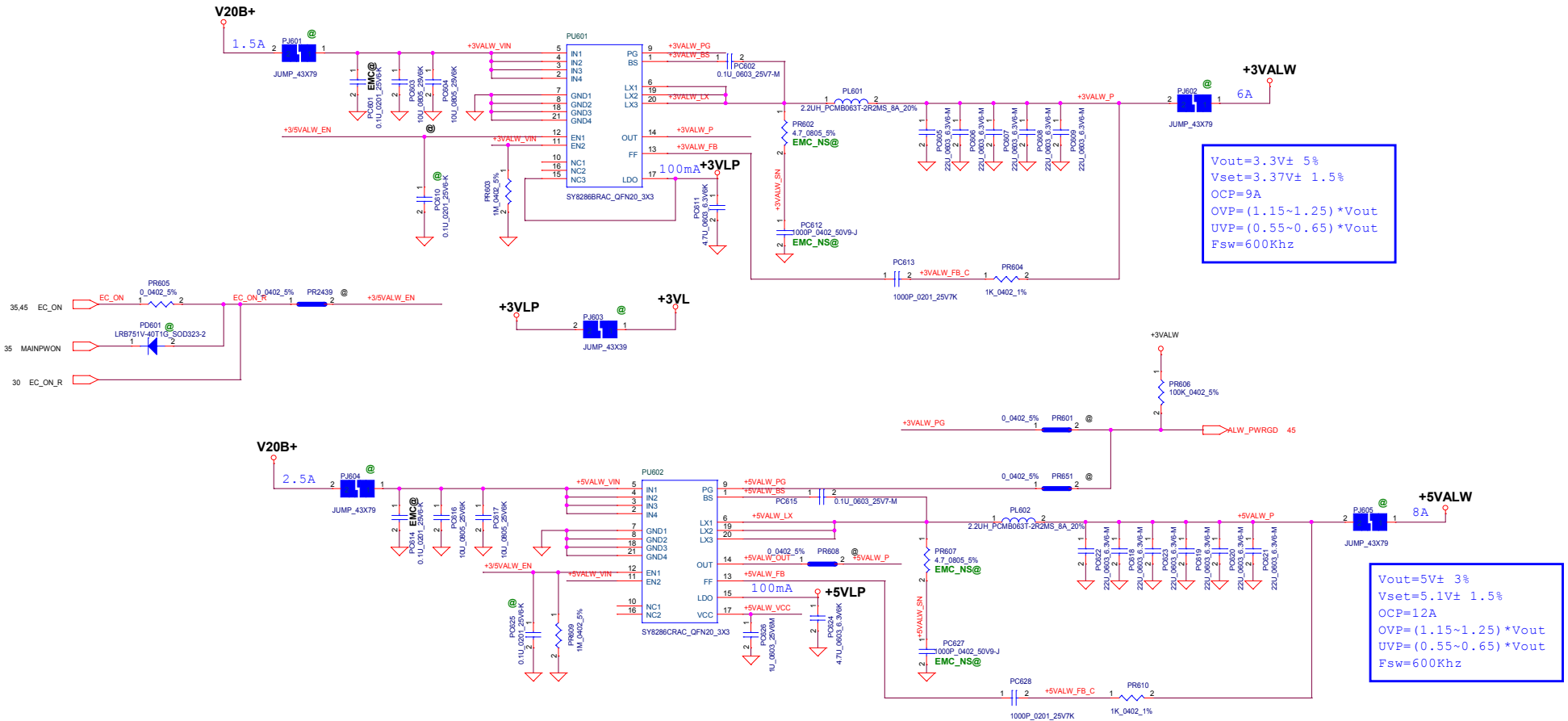
Size	Document Number	Rev
Custom	CG512	1.0

Date: Monday, August 08, 2016 Sheet 42 of 48



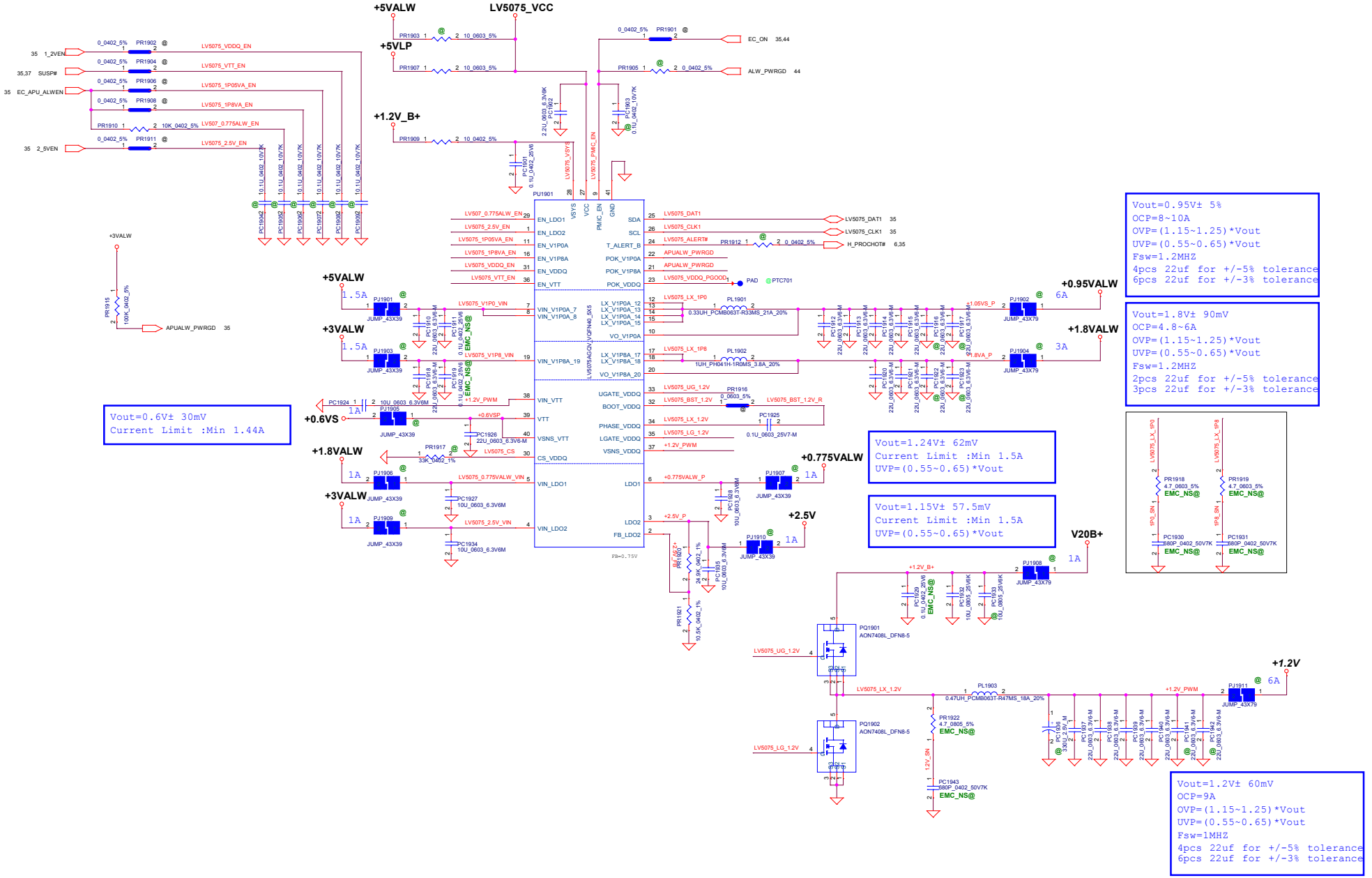
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR--Charger		
Size: Custom	Document Number: CG512		Rev: 1.0
Date: Monday, August 08, 2016	Sheet 43 of 48		



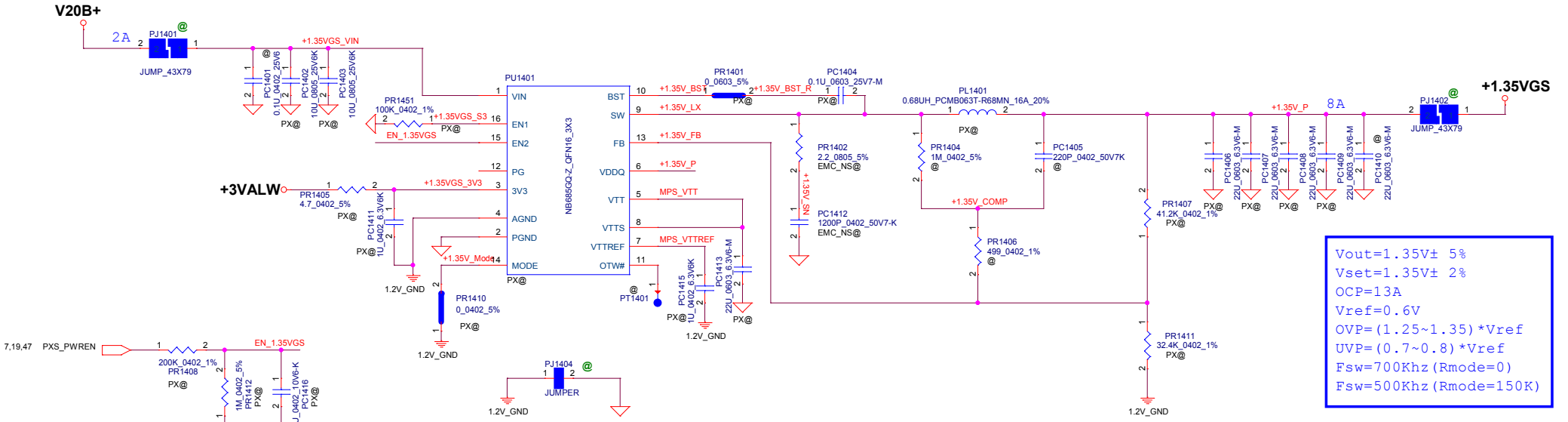
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-3V/5V SY8286B/C		
Size	Document Number	CG512	Rev
C			1.0
Date:	Monday, August 08, 2016	Sheet	44 of 48

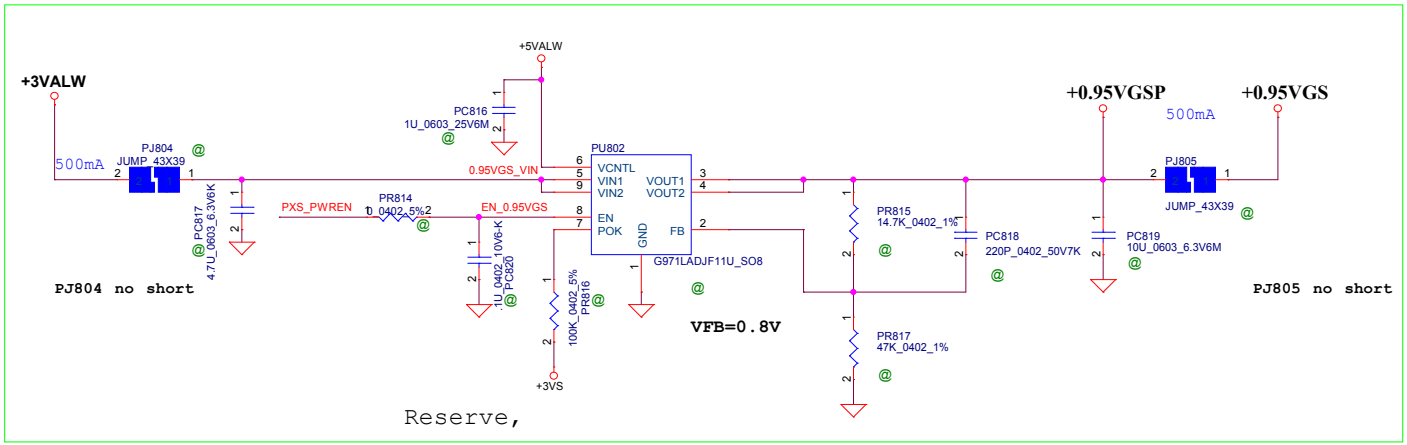


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-XXXX		
Size Custom	Document Number XXXX		Rev 1.0
Date: Monday, August 08, 2016	Sheet 45 of 48		



Vout=1.35V± 5%
Vset=1.35V± 2%
OCP=13A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz(Rmode=0)
Fsw=500Khz(Rmode=150K)



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: VRAM PWR-MPS_NB685

Size	Document Number	Rev
Custom	CG512	1.0

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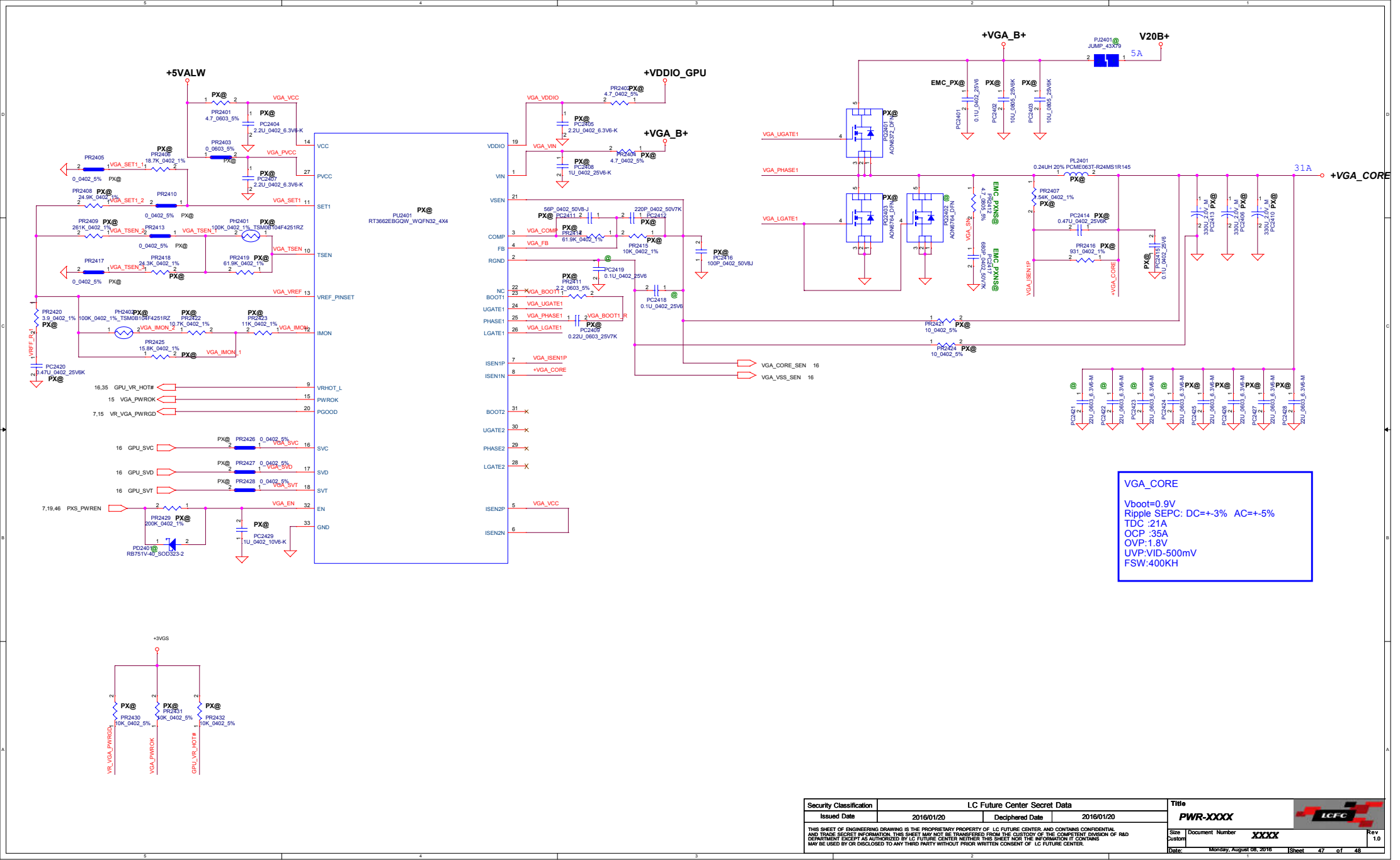
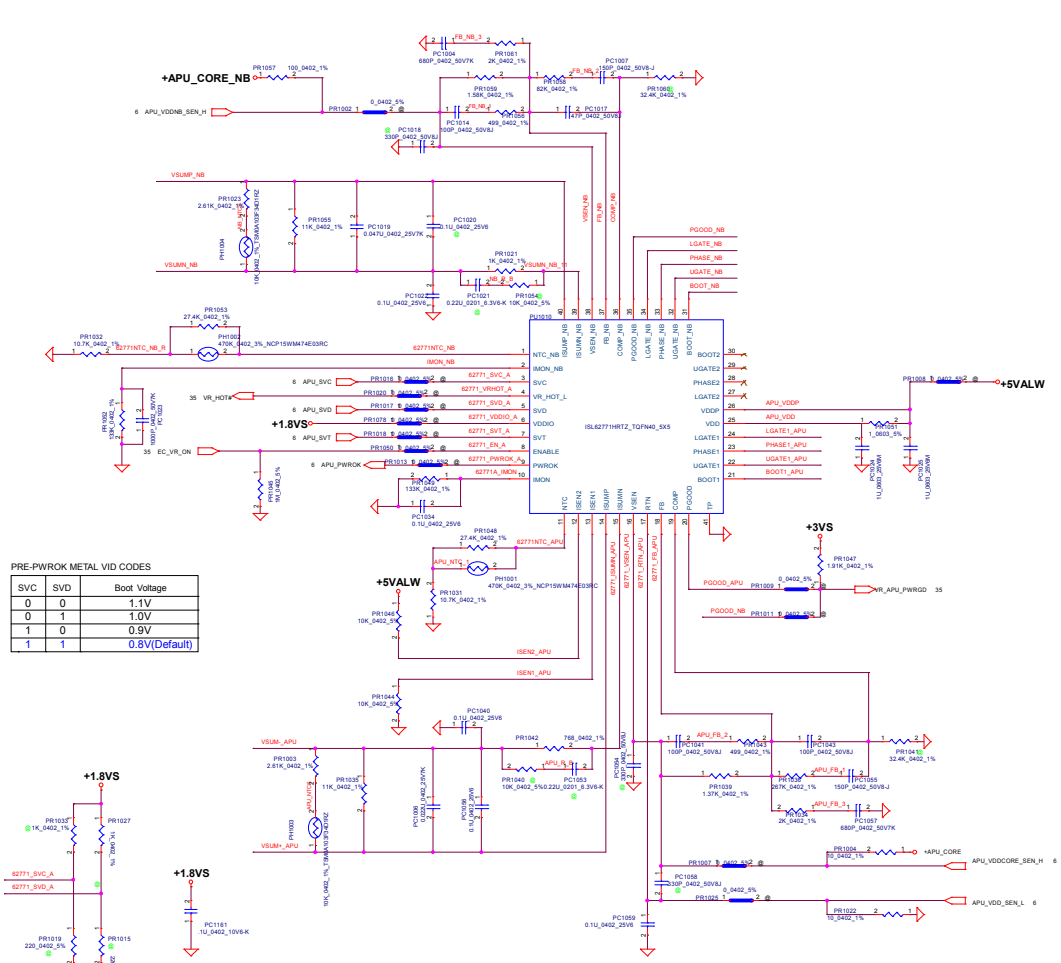


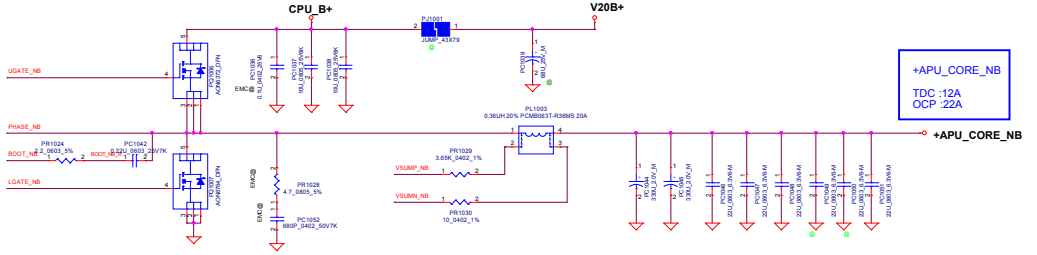
VGA_CORE

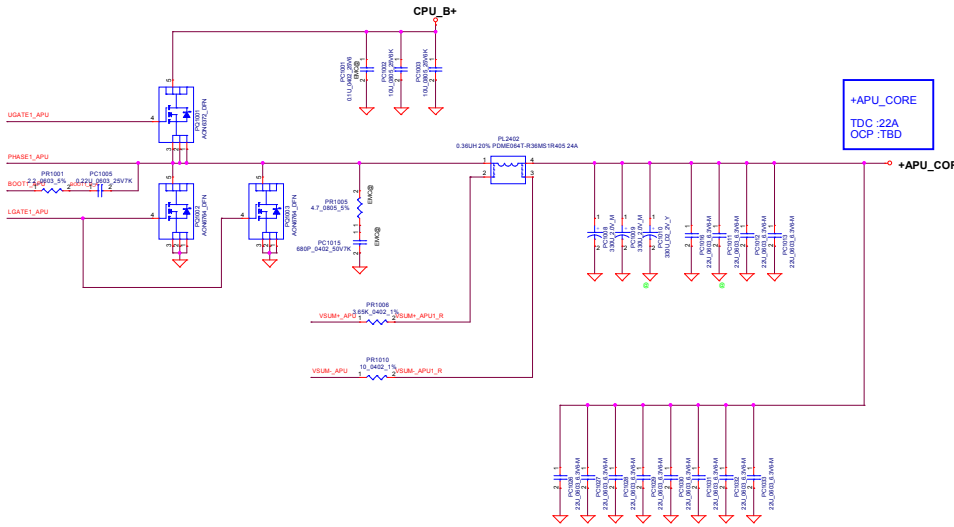
Vboot=0.9V
Ripple SEPC: DC=+-3% AC=+-5%
TDC :21A
OCP :35A
OVP:1.8V
UVP:VID-500mV
FSW:400KH

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-XXXX		
Size: Custom	Document Number: XXXX		Rev: 1.0
Date: Monday, August 08, 2016	Sheet 47 of 48		







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: PWR_CPU Core

Size: D | Document Number: CG512 | Rev: 0.3

Date: Monday, August 05, 2013 | Sheet 48 of 48