PAGE	TITLE	Quantity
01	COVER PAGE	
02	BLOCK DIAGRAM	
03	CPU (PCIE/DMI)	
04	CPU (THERMAL/CLOCK/PM/CFG)	
05	CPU (DDR4 CHANNEL A)	
06	CPU (DDR4 CHANNEL B)	
07	CPU (DDI/EDP)	
08	CPU (CPU Power)	
09	CPU (VSS)	
10	CPU (Power CAP)	
11	DDR4 DIMM_1	
12	DDR4 DIMM_2	
13	DDR4 DIMM_3 (R)	
14	DDR4 DIMM_4 (R)	
15	PCH (SPI/UART/I2C)	
16	PCH (DMI/PCI-E/USB)DDI GP	
17	PCH (PCI-E/SATA)	
18	PCH (CLOCK/CL)	
19	PCH (USB/ESPI)	
20	PCH(GPIO/CPU/SMBUS/IHDA/JTAG)	
21	PCH (POWER1)	
22	PCH (POWER2)_PCH Strap	
23	PCH Power CAP	
24	SIO ITE8732F_CX	
25	Flash&RTC	
26	Thermal&FAN	
27	Audio Codec_ALC269	
28	Audio_MUTE	
29	Audio IO_Combo HP_MIC	
30	Audio IO_Rear (R)	
31	LAN RTL8111GA	
32	RJ45&Transformer	
33	Card reader RTS5229	
34	USB Charger_APL3524	
35	USB_Front Port	
36	USB_REAR PORT	
37	USB20_FRONT HEADER (R)	
38	USB30_REAR PORT (R)	
39	USB30 (R)	
40	Power Plane EN Sequence	
41	Dual Power	
42	Switch power	
43	DCIN JACK(BATT Conn)	
44	OZ554A LED Converter (R)	
45	5V/3D3V(RT6575D)	
46	CPU_CORE(NCP81203)	
47	CPU_CORE_OUTPUT_(NCP81151)	
48	CPU_VCCGTUS (NCP81151)	
49	DCDC_12V (NCP1589A)	
50	CPU_VCCSA (RT8237C)	
51	MEM_MEMVTT (RT8207P)	
52	PCH_1D0V (RT8237C)	
53	VCC_IO (RT8237C)	
54	DCDC_2D5V (APL5930)	

PAGE	TITLE	Quantity
55	LVDS Connector (R)	
56	HDMI IN (R)	
57	HDMI OUT (R)	
58	VGA	
59	DP/HDMI	
60	HDD/ODD	
61	Mini PCIE Card TV Tuner (R)	
62	WLAN and BT--NGFF	
63	SSD-NGFF	
64	PWR BT/Side Key/LED	
65	Stand off&EMI Cap&DUMMY BOM	
66	IO Board (R)	
67	COM PORT	
68	Debug	
69	LPT (R)	
70	G sensor (R)	
71	Thunderbolt (R)	
72	Thunderbolt (R)	
73	Thunderbolt (R)	
74	Thunderbolt (R)	
75	Thunderbolt (R)	
76	GPU (1/5): PEG (R)	
77	GPU (2/5): DIGITALOUT (R)	
78	GPU (3/5): VRAM I/F (R)	
79	GPU (4/5): GPIO/STRAP (R)	
80	GPU (5/5): PWR/GND (R)	
81	VRAM1 (1/2) (R)	
82	VRAM2 (3/4) (R)	
83	VRAM3 (5/6) (R)	
84	VRAM4 (7/8) (R)	
85	PWR_GPU_CORE (R)	
86	DISCRETE VGA POWER (R)	
87	GPU Switch (R)	
88	GPU Switch (R)	
89	GPU others (R)	
90	NFC (R)	
91	TPM	
92	PS2 (R)	
93	Express Card_PCIEx16	
94	Smart Card (R)	
95	Scalar-RTD2486VRD (R)	
96	Scalar Power (R)	
97	Inter LAN_WGI219LM	
98	LAN Switch (R)	
99	XDP&ITP	
100	Table of Content	
101	GPIO table	
102	POWER SEQUENCE	
103	Power Block Diagram	
104	SMBUS table	
105	CLOCK MAP	
106	RESET Flow CHART	
107	Change History	

PCB BOARD SIZE
8 Layers
198mmX184mm
Thickness: 1.6mm

BOM Configuration
Unmount:(R_)
XDP:(X_)
OCP:(O_)
Q170 SKU:(Q_)
DP:(DP_)
USB_TYPE C:(TYPEC_)
USB_TYPE A:(TYPEA_)
3L 前掀式 SATA CONN:(SF_)
3L 後掀式 SATA CONN:(SB_)

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

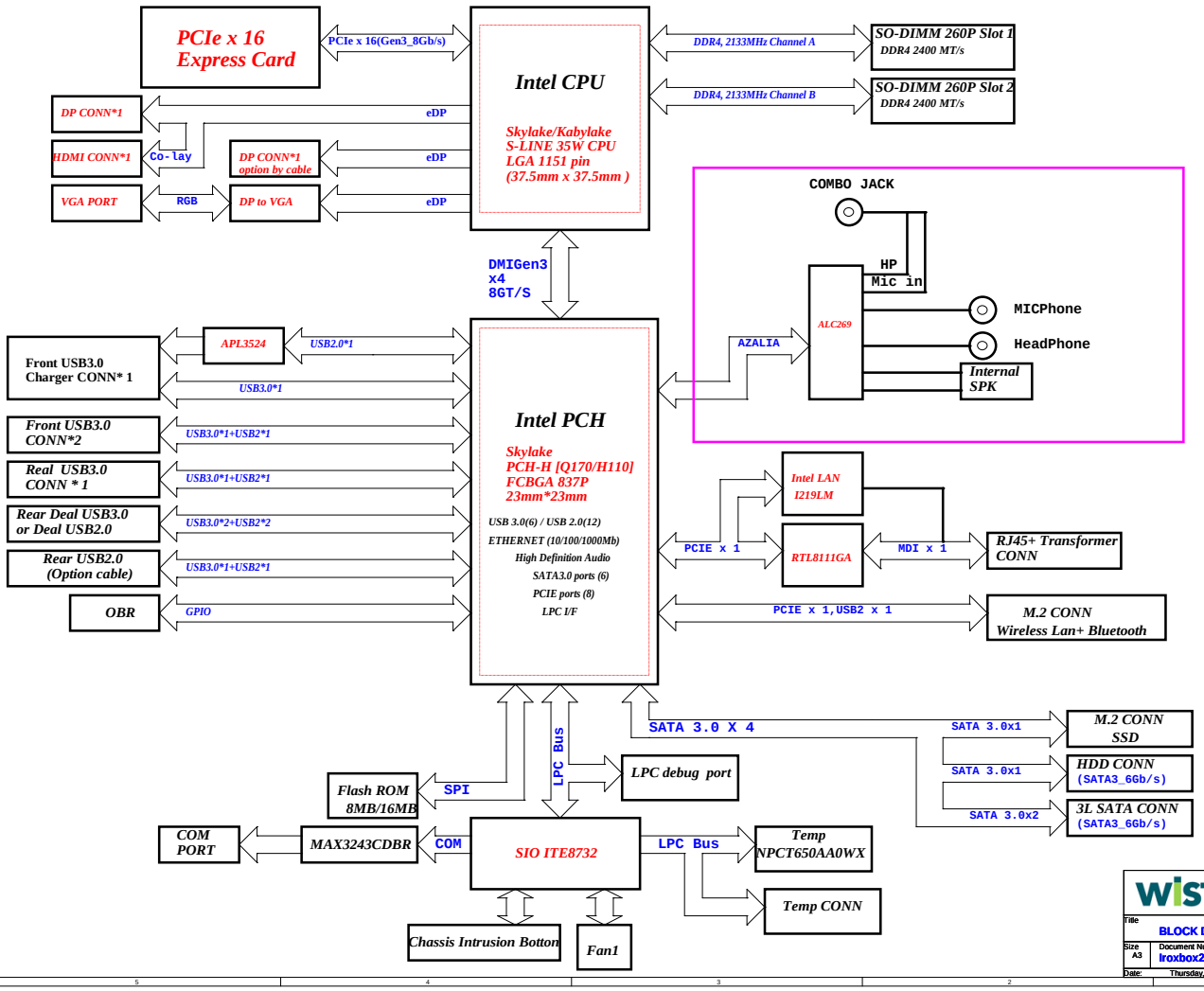
Title: COVER PAGE

Size	Document Number	Rev
C	lroxbox2	-1

Date: Thursday, March 02, 2017 Sheet 1 of 107

Ironbox Block Diagram

PCB:16531
Project Code: 3PD08F010001



5V/3D3V DC/DC RT6575DGQW

INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3D3V_A

CPU/GT DC/DC NCP81203

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE GFX_CORE

VCCSA DC/DC RT8237C

INPUTS	OUTPUTS
DCBATOUT	VCC_SA

VCCIO DC/DC RT8237C

INPUTS	OUTPUTS
DCBATOUT	VCC_IO

12V DC/DC NCP1589AMNTWG

INPUTS	OUTPUTS
3D3V_S0	12V_S0

MEM/MEMVTT DC/DC RT8207P

INPUTS	OUTPUTS
DCBATOUT	VDDQ

1D0V DC/DC RT8237C

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

2D5V_VPP DC/DC APL5930KAI

INPUTS	5V_CHARGER
DCBATOUT	2D5V_VPP

PCB LAYER

L1:Top	L5:GND
L2:GND	L6:Signal
L3:Signal	L7:Signal
L4:Signal	L8:Bottom

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Iroxbox2 | Rev: -1
Date: Thursday, March 09, 2017 | Sheet 2 of 107

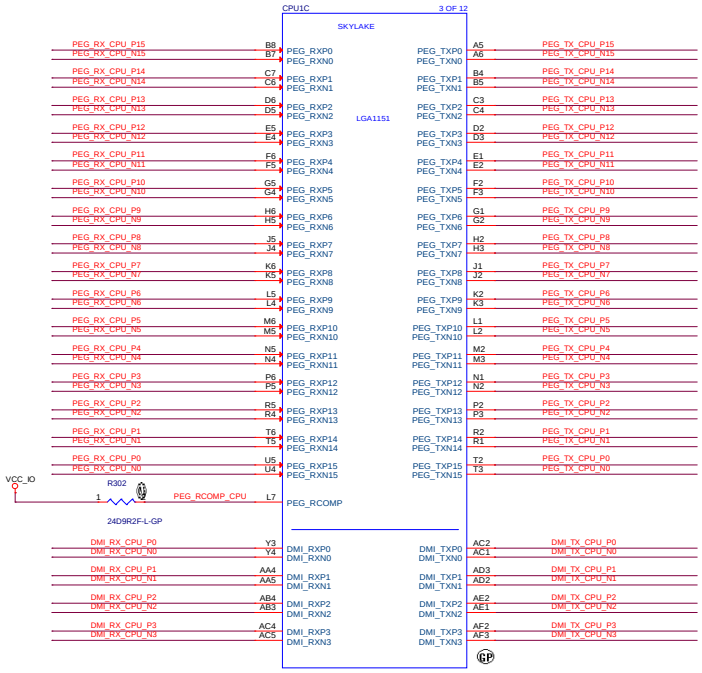
2014/8/5
Change CPU P/N to 062.10015.0081

PEG

93 PEG_TX_CPU_P[0..15]
93 PEG_TX_CPU_N[0..15]
93 PEG_RX_CPU_P[0..15]
93 PEG_RX_CPU_N[0..15]

DMI

16 DMI_RX_CPU_P[0..3]
16 DMI_RX_CPU_N[0..3]
16 DMI_TX_CPU_P[0..3]
16 DMI_TX_CPU_N[0..3]



SKYLAKE-1

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU(PCIE/DMI)

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 3 of 107

CPU XDP

20 H_TDO
20 H_TDI
20 H_TMS
20 H_TCK
65 H_TRST_N
99 H_PREQ_N
99 H_PRDY_N

SVID

46 VIDSCK_VR1
46 VIDSOUT_VR1
46 VIDALERT#_VR1

CLOCK

18 CPU_BCLK_PCH
18 CPU_BCLK_PCH#
18 CPU_PCIBCLK_PCH
18 CPU_PCIBCLK_PCH#
18 CPU_CLK24M_PCH
18 CPU_CLK24M_PCH#

CONTROL

65 CPU_VCCST_PWRGD_R
24,46 PROCHOT#_R
51 DDR_VTT_CNTL
40 CPU_VCCST_PWRGD
20,65 H_PWRGD
17,65 PLTRST_CPU_N
17 PM_SYNC_CPU
17 PM_DOWN_PCH
17,24 PECI_CPU
17 THERMTRIP#_CPU_R
16 H_SKTOCC_N

20 PCH_JTAG_TDO
20 PCH_JTAG_TDI
20 PCH_JTAG_TMS
21 H_TRST_N_R

VIDSCK
VIDSOUT
VIDALERT#
Need to add Pull UP on both CPU and VR side.

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	WS1 [inches]	WS2 [inches]	R_{PU} [Ω]	R_{PD} [Ω]	R_{ST} [Ω]	VCC_{fs} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

2014/9/29
reserve R21 as Rosa D7

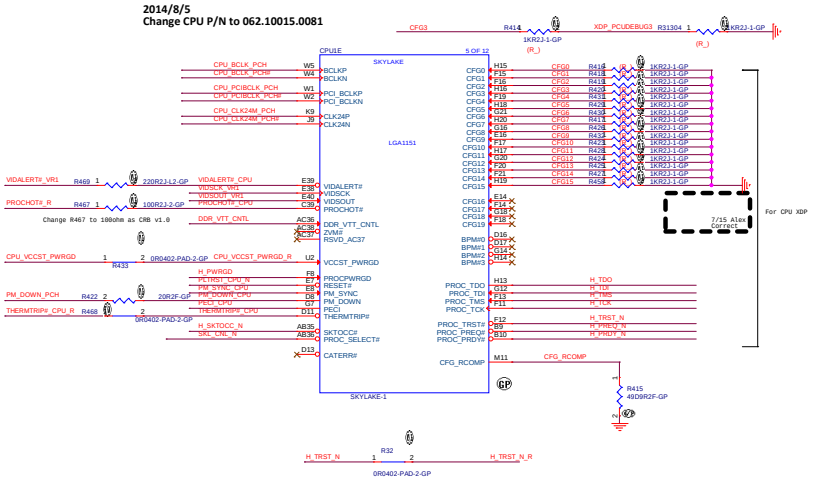
SKL_CNL_N R402 2 1 10KR2J-3-GP VCC_IO
0 this RES Value unconfirm.

1V_VCCST_VCCPLL_S3
VIDSCK_VR1 R17 1 2 45D3R3F-L-GP
VIDALERT#_VR1 R470 1 2 56R2F-1-GP
VIDSOUT_VR1 R471 1 2 100R2J-2-GP
PROCHOT#_CPU R421 1 2 75R2F-2-GP
Change R421 to 75ohm as CRB v1.0

3D3V_S5
H_SKTOCC_N R477 1 10KR2J-3-GP

H_TCK TERMINATION
PLACE NEAR CPU WITHIN 1.1 INCH
H_TCK R403 1 51R2F-2-GP
Place on Bottom
H_TRST_N R407 1 51R2F-2-GP

2014/8/5
Change CPU P/N to 062.10015.0081



- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_(THERMAL/CLOCK/PM/CFG)
Size: Custom | Document Number: Iroxbox2 | Rev: -1
Date: Thursday, March 02, 2017 | Sheet 4 of 107

CHANNEL A DIMM0

11 M_A_DQ[63..0]

11 M_A_A[13..0]

11 M_A_DQS_DP[7..0]

11 M_A_DQS_DN[7..0]

11 M_A_BA[1..0]

11 M_A_BG[1..0]

11 M_A_CLK0
11 M_A_CLK#0

11 M_A_CLK1
11 M_A_CLK#1

11 M_A_CS#[1..0]

11 M_A_ACT#

11 M_A_ODT0
11 M_A_ODT1

11 M_A_CKE0
11 M_A_CKE1

11 M_A_CAS#
11 M_A_WE#
11 M_A_RAS#

11 M_A_ALERT#
11 M_A_PAR

2014/8/5
Change CPU P/N to 062.10015.0081

CPU1A — 1 OF 12 — SKYLAKE — LGA1151

M_A_DQ0	AE38	DDR0_DQ0	
M_A_DQ1	AE37	DDR0_DQ1	
M_A_DQ2	AD38	DDR0_DQ2	
M_A_DQ3	AD37	DDR0_DQ3	
M_A_DQ4	AE39	DDR0_DQ4	
M_A_DQ5	AE40	DDR0_DQ5	
M_A_DQ6	AD39	DDR0_DQ6	
M_A_DQ7	AD40	DDR0_DQ7	
M_A_DQ8	A38	DDR0_DQ8	
M_A_DQ9	A37	DDR0_DQ9	
M_A_DQ10	AL38	DDR0_DQ10	
M_A_DQ11	AL37	DDR0_DQ11	
M_A_DQ12	AJ40	DDR0_DQ12	
M_A_DQ13	AJ39	DDR0_DQ13	
M_A_DQ14	AL39	DDR0_DQ14	
M_A_DQ15	AL40	DDR0_DQ15	
M_A_DQ16	AN38	DDR0_DQ16/DDR0_DQ32	
M_A_DQ17	AN40	DDR0_DQ17/DDR0_DQ33	
M_A_DQ18	AR38	DDR0_DQ18/DDR0_DQ34	
M_A_DQ19	AR37	DDR0_DQ19/DDR0_DQ35	
M_A_DQ20	AN39	DDR0_DQ20/DDR0_DQ36	
M_A_DQ21	AN37	DDR0_DQ21/DDR0_DQ37	
M_A_DQ22	AR39	DDR0_DQ22/DDR0_DQ38	
M_A_DQ23	AR40	DDR0_DQ23/DDR0_DQ39	
M_A_DQ24	AW37	DDR0_DQ24/DDR0_DQ40	
M_A_DQ25	AU38	DDR0_DQ25/DDR0_DQ41	
M_A_DQ26	AV35	DDR0_DQ26/DDR0_DQ42	
M_A_DQ27	AW35	DDR0_DQ27/DDR0_DQ43	
M_A_DQ28	AU37	DDR0_DQ28/DDR0_DQ44	
M_A_DQ29	AV37	DDR0_DQ29/DDR0_DQ45	
M_A_DQ30	AT35	DDR0_DQ30/DDR0_DQ46	
M_A_DQ31	AU35	DDR0_DQ31/DDR0_DQ47	
M_A_DQ32	AY8	DDR0_DQ32/DDR1_DQ0	
M_A_DQ33	AW8	DDR0_DQ33/DDR1_DQ1	
M_A_DQ34	AV6	DDR0_DQ34/DDR1_DQ2	
M_A_DQ35	AU6	DDR0_DQ35/DDR1_DQ3	
M_A_DQ36	AU8	DDR0_DQ36/DDR1_DQ4	
M_A_DQ37	AV8	DDR0_DQ37/DDR1_DQ5	
M_A_DQ38	AW6	DDR0_DQ38/DDR1_DQ6	
M_A_DQ39	AY6	DDR0_DQ39/DDR1_DQ7	
M_A_DQ40	AY4	DDR0_DQ40/DDR1_DQ8	
M_A_DQ41	AV4	DDR0_DQ41/DDR1_DQ9	
M_A_DQ42	AT1	DDR0_DQ42/DDR1_DQ10	
M_A_DQ43	AT2	DDR0_DQ43/DDR1_DQ11	
M_A_DQ44	AV3	DDR0_DQ44/DDR1_DQ12	
M_A_DQ45	AW4	DDR0_DQ45/DDR1_DQ13	
M_A_DQ46	AT4	DDR0_DQ46/DDR1_DQ14	
M_A_DQ47	AT3	DDR0_DQ47/DDR1_DQ15	
M_A_DQ48	AP2	DDR0_DQ48/DDR1_DQ32	
M_A_DQ49	AM4	DDR0_DQ49/DDR1_DQ33	
M_A_DQ50	AP3	DDR0_DQ50/DDR1_DQ34	
M_A_DQ51	AM3	DDR0_DQ51/DDR1_DQ35	
M_A_DQ52	AP4	DDR0_DQ52/DDR1_DQ36	
M_A_DQ53	AM2	DDR0_DQ53/DDR1_DQ37	
M_A_DQ54	AP1	DDR0_DQ54/DDR1_DQ38	
M_A_DQ55	AM1	DDR0_DQ55/DDR1_DQ39	
M_A_DQ56	AK3	DDR0_DQ56/DDR1_DQ40	
M_A_DQ57	AH1	DDR0_DQ57/DDR1_DQ41	
M_A_DQ58	AK4	DDR0_DQ58/DDR1_DQ42	
M_A_DQ59	AK2	DDR0_DQ59/DDR1_DQ43	
M_A_DQ60	AH4	DDR0_DQ60/DDR1_DQ44	
M_A_DQ61	AK2	DDR0_DQ61/DDR1_DQ45	
M_A_DQ62	AH3	DDR0_DQ62/DDR1_DQ46	
M_A_DQ63	AK1	DDR0_DQ63/DDR1_DQ47	

AU33	DDR0_ECC0	DDR0_DQSP2/DDR0_DQSP4
AT33	DDR0_ECC1	DDR0_DQSP3/DDR0_DQSP5
AW33	DDR0_ECC2	DDR0_DQSP4/DDR1_DQSP0
AV31	DDR0_ECC3	DDR0_DQSP5/DDR1_DQSP1
AU31	DDR0_ECC4	DDR0_DQSP6/DDR1_DQSP4
AT31	DDR0_ECC5	DDR0_DQSP7/DDR1_DQSP5
AW31	DDR0_ECC6	DDR0_DQSP8
AY31	DDR0_ECC7	DDR0_DQSN8

AW18	M_A_CLK0	DDR0_CKP0
AV18	M_A_CLK#0	DDR0_CKN0
AW17	M_A_CLK1	DDR0_CKP1
AY17	M_A_CLK#1	DDR0_CKN1
AW16		DDR0_CKP2
AV16		DDR0_CKN2
AT18		DDR0_CKP3
AU18		DDR0_CKN3
AY24	M_A_CKE0	DDR0_CKE0
AW24	M_A_CKE1	DDR0_CKE1
AY25		DDR0_CKE2
AV25		DDR0_CKE3
AW12	M_A_CS#0	DDR0_CS#0
AU11	M_A_CS#1	DDR0_CS#1
AV13		DDR0_CS#2
AT13		DDR0_CS#3
AW11	M_A_ODT0	DDR0_ODT0
AU14	M_A_ODT1	DDR0_ODT1
AU12		DDR0_ODT2
AT16		DDR0_ODT3
AY13	M_A_BA0	DDR0_BA0/DDR0_CA8/DDR0_BA0
AV15	M_A_BA1	DDR0_BA1/DDR0_CA9/DDR0_BA1
AW23	M_A_BG0	DDR0_BA2/DDR0_CA4/DDR0_BG0
AW13	M_A_RAS#	DDR0_RAS#/DDR0_CA3/DDR0_MA16
AV14	M_A_WE#	DDR0_WE#/DDR0_CA2/DDR0_MA14
AY11	M_A_CAS#	DDR0_CAS#/DDR0_CA1/DDR0_MA15
AW15	M_A_A0	DDR0_MA0/DDR0_CA9/DDR0_MA0
AU18	M_A_A1	DDR0_MA1/DDR0_CA8/DDR0_MA1
AU17	M_A_A2	DDR0_MA2/DDR0_CA5/DDR0_MA2
AV19	M_A_A3	DDR0_MA3
AT19	M_A_A4	DDR0_MA4
AU20	M_A_A5	DDR0_MA5/DDR0_CA4/DDR0_MA5
AV20	M_A_A6	DDR0_MA6/DDR0_CA2/DDR0_MA6
AU21	M_A_A7	DDR0_MA7/DDR0_CA4/DDR0_MA7
AT20	M_A_A8	DDR0_MA8/DDR0_CA3/DDR0_MA8
AT22	M_A_A9	DDR0_MA9/DDR0_CA1/DDR0_MA9
AY14	M_A_A10	DDR0_MA10/DDR0_CA8/7/DDR0_MA10
AU22	M_A_A11	DDR0_MA11/DDR0_CA7/DDR0_MA11
AY22	M_A_A12	DDR0_MA12/DDR0_CA6/DDR0_MA12
AV12	M_A_A13	DDR0_MA13/DDR0_CA8/DDR0_MA13
AY23	M_A_BG1	DDR0_MA14/DDR0_CA9/DDR0_BG1
AU24	M_A_ACT#	DDR0_MA15/DDR0_CA8/DDR0_ACT#
AY15	M_A_PAR	DDR0_PAR
AY23	M_A_ALERT#	DDR0_ALERT#

AF39	M_A_DQS_DN0	DDR0_DQSN0
AK39	M_A_DQS_DN1	DDR0_DQSN1
AP39	M_A_DQS_DN2	DDR0_DQSN2/DDR0_DQSN4
AU36	M_A_DQS_DN3	DDR0_DQSN3/DDR0_DQSN5
AW7	M_A_DQS_DN4	DDR0_DQSN4/DDR1_DQSN0
AU3	M_A_DQS_DN5	DDR0_DQSN5/DDR1_DQSN1
AN3	M_A_DQS_DN6	DDR0_DQSN6/DDR1_DQSN4
AJ3	M_A_DQS_DN7	DDR0_DQSN7/DDR1_DQSN5
AF38	M_A_DQS_DP0	DDR0_DQSP0
AK38	M_A_DQS_DP1	DDR0_DQSP1
AP38	M_A_DQS_DP2	DDR0_DQSP2/DDR0_DQSP4
AV36	M_A_DQS_DP3	DDR0_DQSP3/DDR0_DQSP5
AV7	M_A_DQS_DP4	DDR0_DQSP4/DDR1_DQSP0
AU2	M_A_DQS_DP5	DDR0_DQSP5/DDR1_DQSP1
AN2	M_A_DQS_DP6	DDR0_DQSP6/DDR1_DQSP4
AJ2	M_A_DQS_DP7	DDR0_DQSP7/DDR1_DQSP5

DDR CHANNEL A

SKYLAKE-1

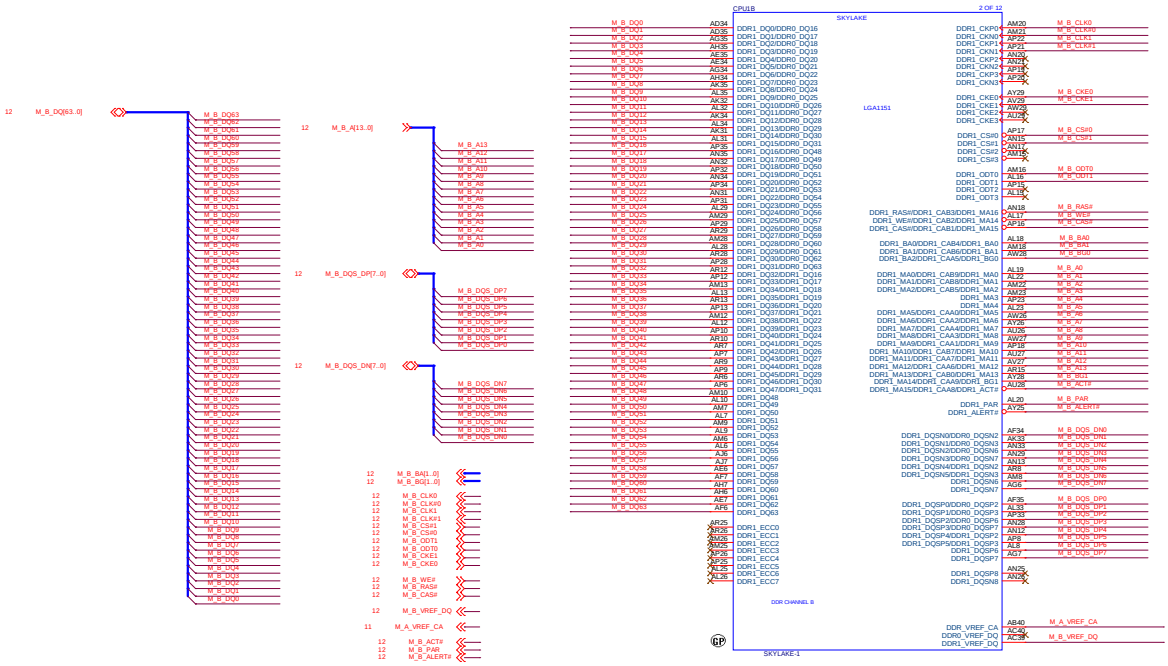
<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_(DDR4 CHANNEL A)

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 5 of 107



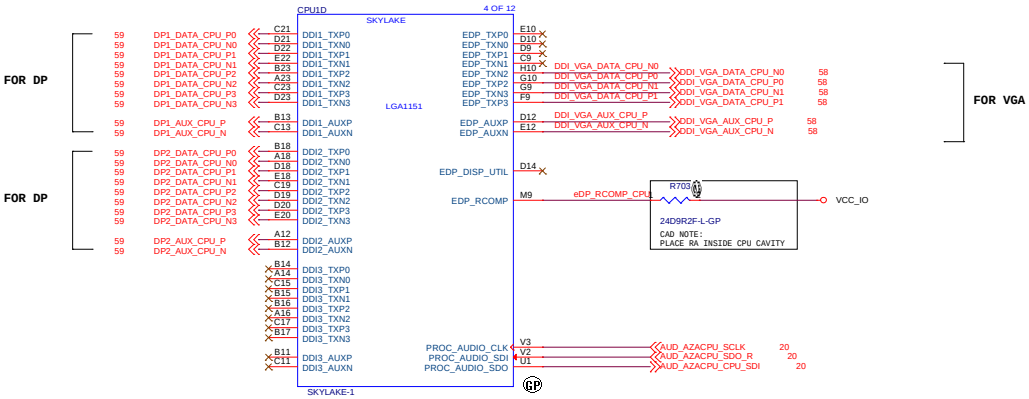
<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: CPU (DDR_CHB)		
Size: C	Document Number: Iroxbox2	Rev: -1
Date: Wednesday, March 08, 2017	Sheet 6 of 107	

2014/8/5
Change CPU P/N to 062.10015.0081

VBIOS set as DP

Note:
1. When using eDP bifurcation:
   — x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1])
   — x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

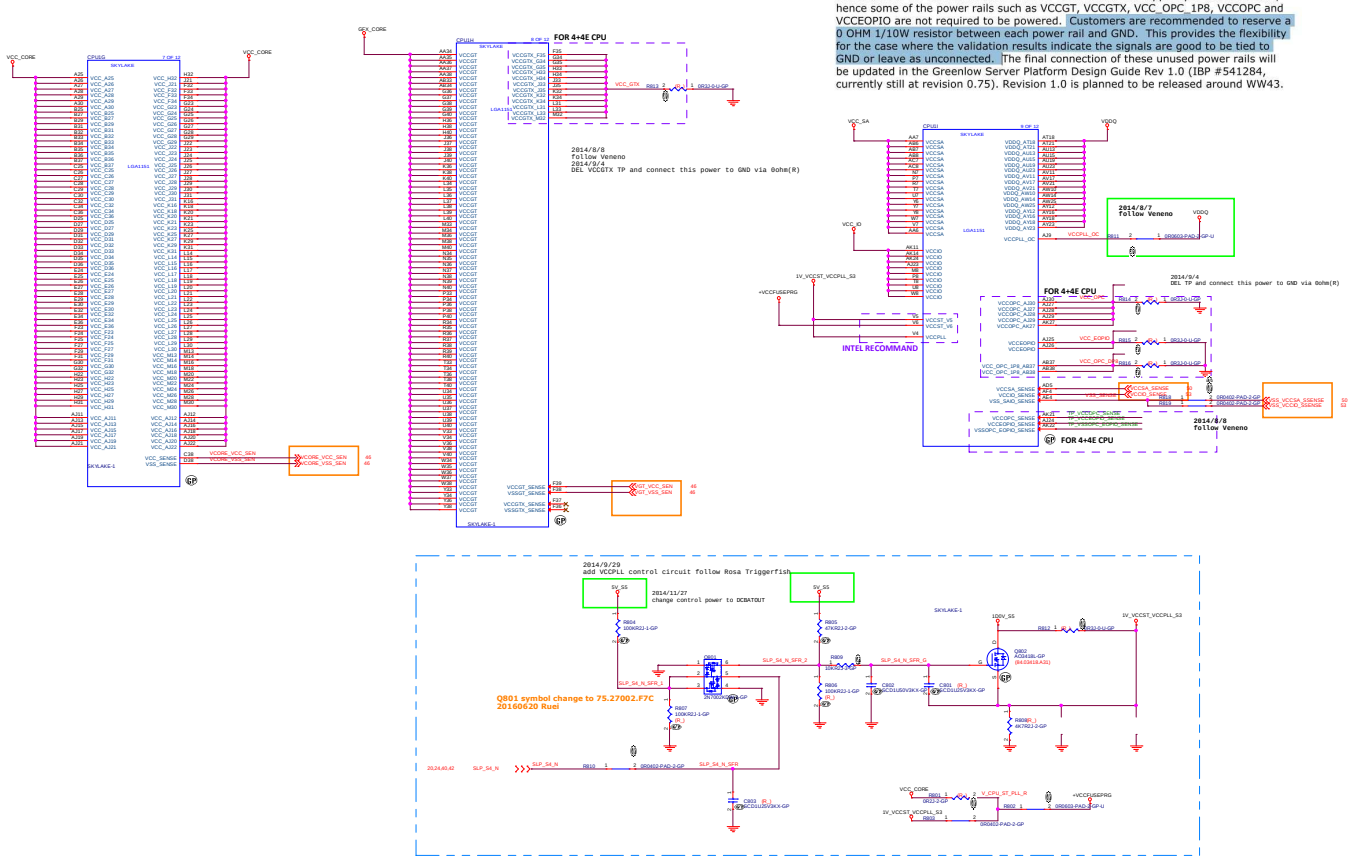
Title: CPU (DDI/EDP)

Size: Custom | Document Number: Iroxbox2 | Rev: -1

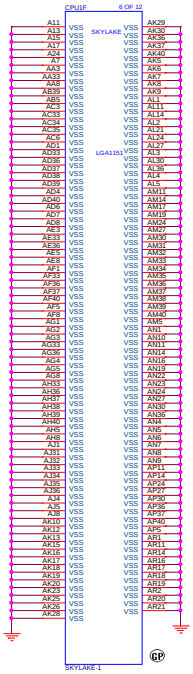
Date: Thursday, March 02, 2017 | Sheet 7 of 107

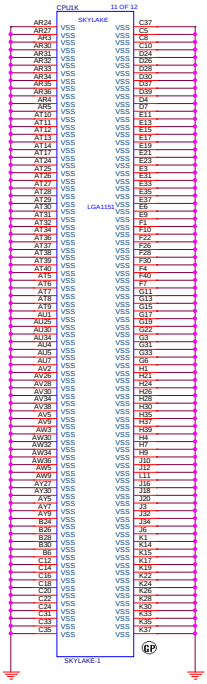
Greenlow Server Reference Circuit: Unused Power Pins Handling

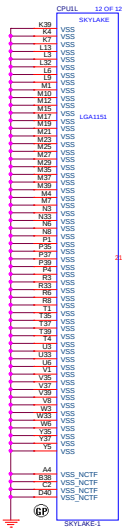
Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGT, VCCGTX, VCC_OPC_1P8, VCCOPC and VCCEOPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.

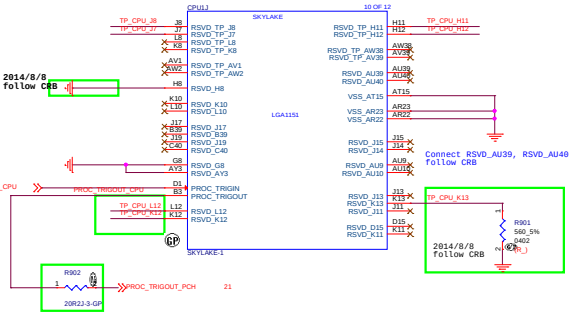


2014/8/5
Change CPU P/N to 062.10015.0081









<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: CPU (VSS)		
Size: C	Document Number: lroxbox2	Rev: -1
Date: Thursday, March 02, 2017	Sheet 9 of 107	

2014/8/8
DEL VCCOPC and VCCEOPIO power cap

PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

2014/8/8
add VCC_SA cap

CAPS FOR DIMM

2014/8/8
add 1D2V_S3 cap

PLACE ALL CAPS SOCKET EDGE TOP

PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

2014/8/8
add VCC_IO cap

PLACE ALL CAPS OUTSIDE CPU SOCKET CAVITY ON TOPSIDE

2014/8/15
del TC1001-TC1008

PLACE CAPS AT SOCKET EDGE 6 ON TOP & 6 ON BOTTOM

PLACE CAP ON SOCKET EDGE TOP(SLR)

PLACE CAPS ON TOP SIDE SOCKET CAVITY

PLACE CAPS ON BACKSIDE UNDER SOCKET CAVITY

PLACE CAPS ON TOP SIDE SOCKET CAVITY

PLACE CAPS AT SOCKET EDGE 6 ON TOP & 6 ON BOTTOM

<Core Design>

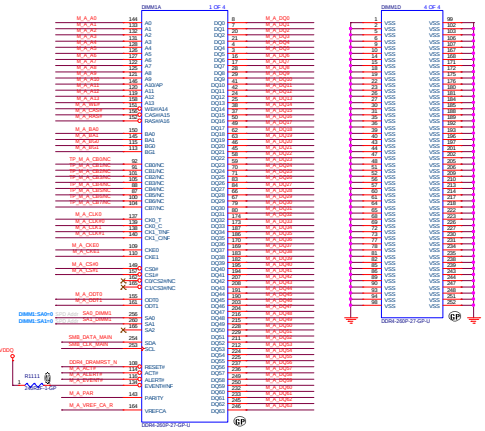
wistron

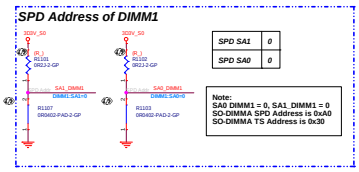
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

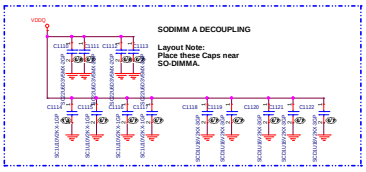
Title: CPU Power CAP

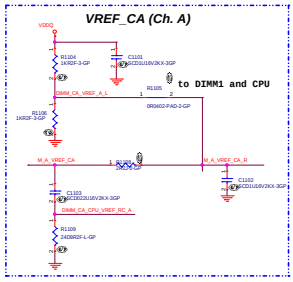
Size: Custom | Document Number: Rev: 0A | Date: Monday, March 03, 2014 | Sheet 16 of 37

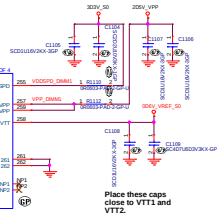
CHANNEL-A XMM1, A0, H=8mm







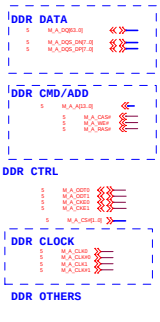




SMBus 0	
Device	8-bit Address (hex)
DIMM A0	A0
DIMM A1	A4
DIMM B0	A2
DIMM B1	A6

1 0 1 0 0 x x 0

Note:0,7 Bit as default



Wistron Incorporated
21F, 88, Sec.,Lihsin Tai Wu Rd
Hsichih, Taipei Hsien

Title	DDR4 DIMM_1		
Size	Document Number		Rev
C	Custom	ironbox2	-1
Date:	Tuesday, March 28, 2017	Sheet 11 of 307	

CHANNEL-B DIMM2, A2, H=4mm

DDR DATA
6 M_B_DQ63..0
6 M_B_DQS_DP[7..0]
6 M_B_DQS_DN[7..0]

DDR CMD/ADD
6 M_B_A[13..0]
6 M_B_WE#
6 M_B_RAS#
6 M_B_CAS#
6 M_B_BA[2..0]
6 M_B_BS0..1

DDR CTRL
6 M_B_CS#1
6 M_B_CS#0
6 M_B_CKE1
6 M_B_CKE0
6 M_B_ODT1
6 M_B_ODT0

DDR CLOCK
6 M_B_CLK1
6 M_B_CLK0#
6 M_B_CLK1
6 M_B_CLK1#

DDR OTHERS
11,20,65 DDRA_DRAMRST_N
11,20,58,63 SMB_DATA_MAIN
11,20,58,63 SMB_CLK_MAIN
6 M_B_ACT#
6 M_B_PAR
6 M_B_ALERT#
6 M_B_VREF_DQ

DIMM2A 1 OF 4
DIMM2D 4 OF 4
DIMM2B 2 OF 4
DIMM2C 2 OF 4

DDR4-260P-1D-GP-U (662.10011.030P1)

SPD Address of DIMM2

SPD SA1	1
SPD SA0	0

Note:
SA0 DIMM2 = 0, SA1_DIMM2 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM B DECOUPLING
Layout Note:
Place these Caps near SO-DIMMA.

VREF_DQ (Ch. B)
to DIMM2 and CPU

Place these caps close to VTT1 and VTT2.

SMBus 0	
Device	8-bit Address (hex)
DIMM A0	A0
DIMM A1	A4
DIMM B0	A2
DIMM B1	A6

1	0	1	0	0	x	x	0

Note: 0,1 "7 Bit as default

<Core Design>
wistron Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title: DDR4 DIMM_2
Size: Custom
Document Number: Inxbox2
Rev: -1
Date: Thursday, March 09, 2017 Sheet 12 of 37

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DDR4 DIMM_3_(R)

Size	Document Number	Rev
Custom	Inoxbox2	-1

Date: Thursday, March 02, 2017 Sheet 13 of 107

Reserved

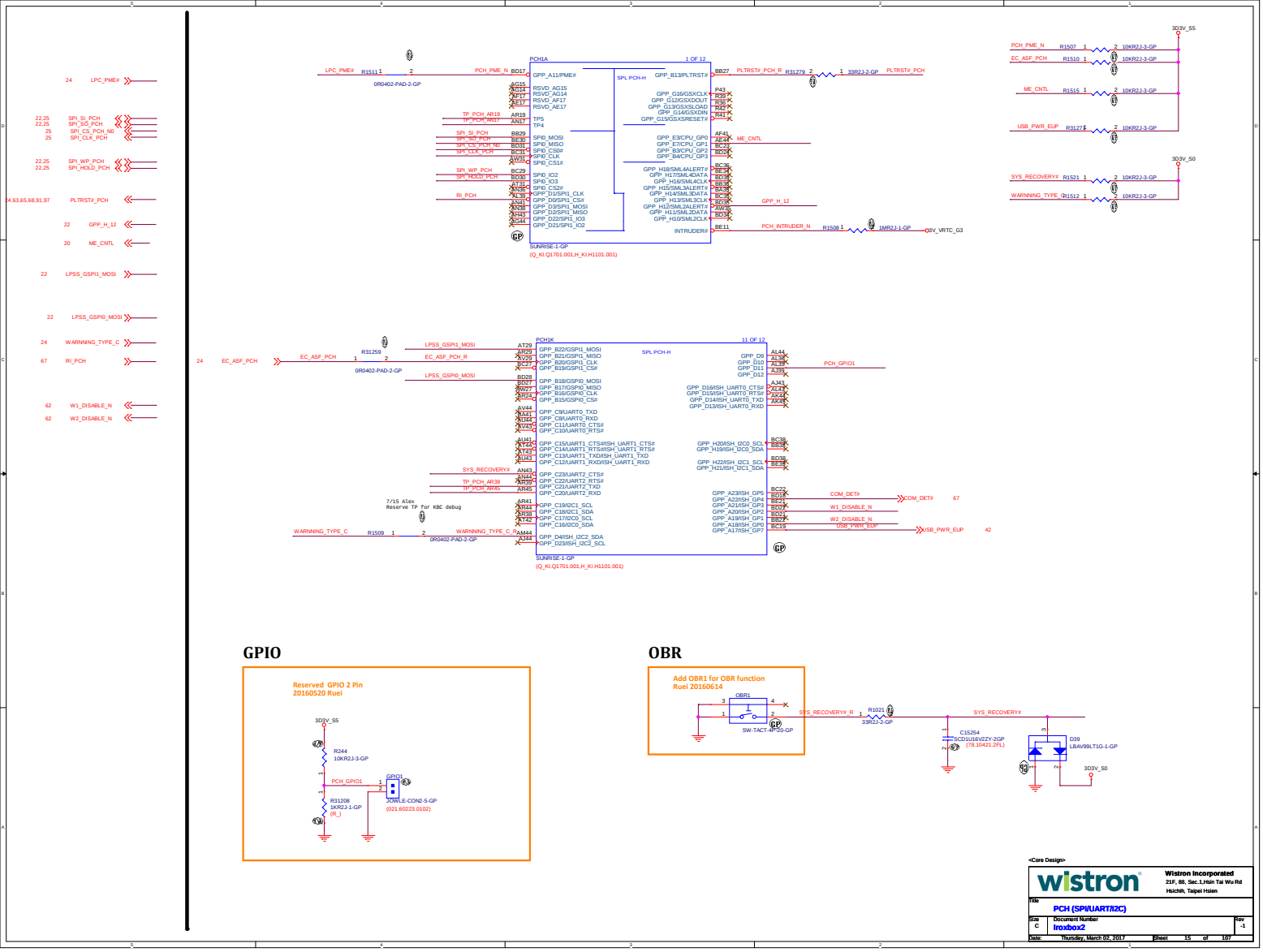
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
DDR4 DIMM_4_(R)

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 14 of 107



GPIO

OBR

<Core Design>

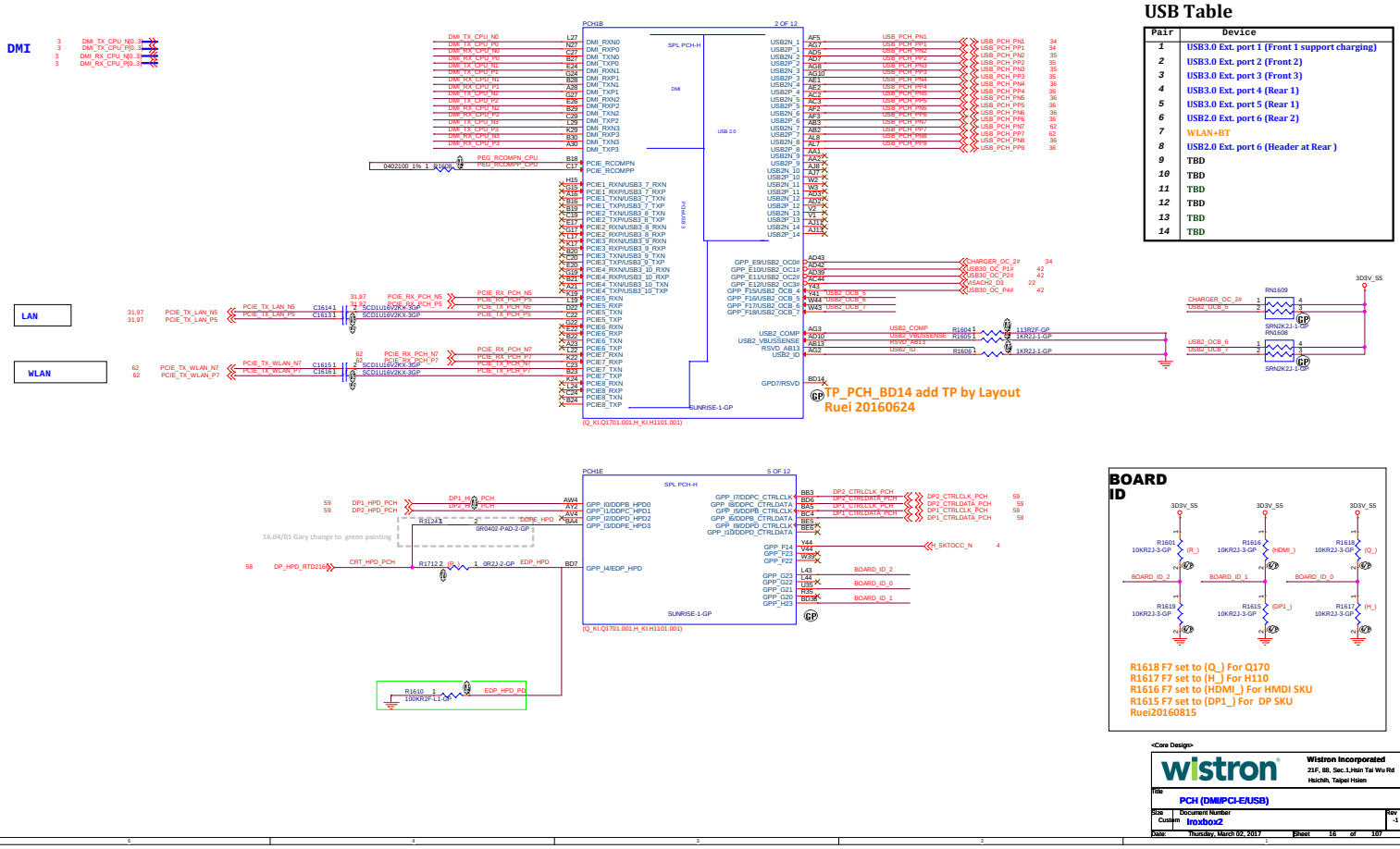
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (SPI/UART/I2C)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Thursday, March 02, 2017 Sheet 15 of 107



USB Table

Pair	Device
1	USB3.0 Ext. port 1 (Front 1 support charging)
2	USB3.0 Ext. port 2 (Front 2)
3	USB3.0 Ext. port 3 (Front 3)
4	USB3.0 Ext. port 4 (Rear 1)
5	USB3.0 Ext. port 5 (Rear 1)
6	USB2.0 Ext. port 6 (Rear 2)
7	WLAN+BT
8	USB2.0 Ext. port 6 (Header at Rear)
9	TBD
10	TBD
11	TBD
12	TBD
13	TBD
14	TBD

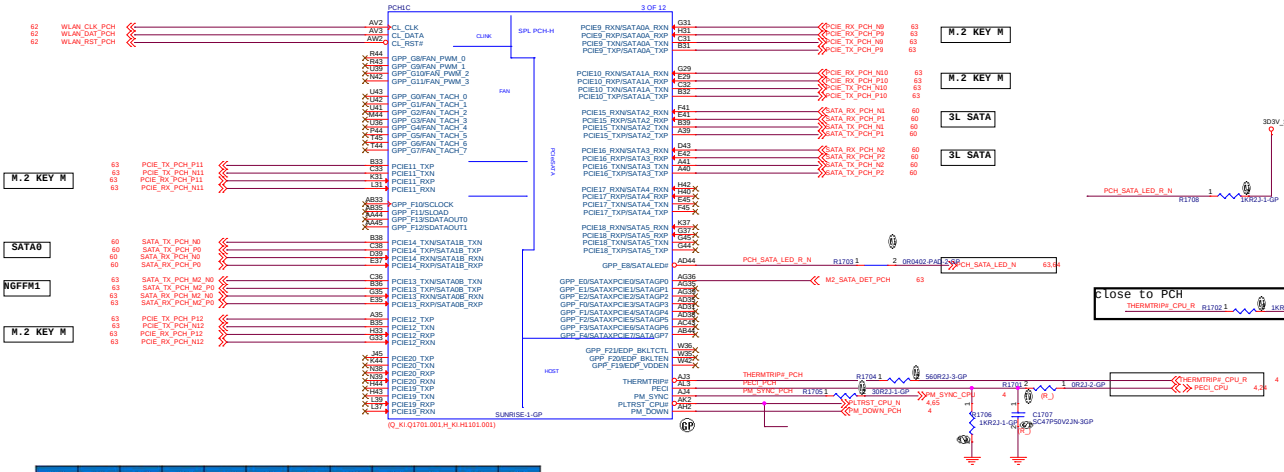
BOARD ID

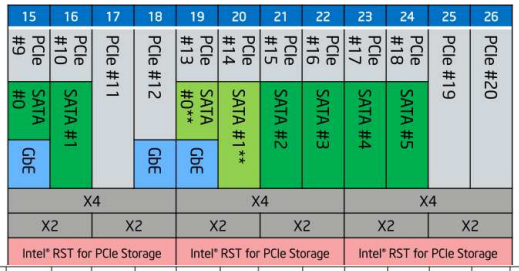
R1618 F7 set to (Q_) For Q170
R1617 F7 set to (H_) For H110
R1616 F7 set to (HDMI_) For HMDI SKU
R1615 F7 set to (DP1_) For DP SKU
Ruei20160815

<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (DMI/PCI-E/USB)
Size: Custom | Document Number: Iroxbox2 | Rev: -1
Date: Thursday, March 02, 2017 | Sheet 16 of 107





Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (PCI-E/SATA)

Size	Document Number	Rev
Custom	Inxboxz	-1

Date: Thursday, March 02, 2017 Sheet 17 of 107

6/21 Delete
CLKOUT_48 is only supported and enabled on SKL-H Server

2014/8/13 2.7K 1%
1V_VCCF24_Sx NEED CHECK
R1803 1 2K7R2F-GP
6/26 2.7K 0.5%
INTEL PDG: 2.71K 0.5%

Add PEG_CLKREQ9_M2# For M.2 SSD 20160517 Ruei
Add PEG_REQ_PCIE16# For M.2 SSD 20160517 Ruei

CLK OUT for CPU XDP
CLK OUT OF PCIE for PCIEx16
CLK OUT OF PCIE for SSD
CLK OUT OF PCIE for LAN
CLK OUT OF miniPCIEx1 for WLAN

X1801 symbol change to 82.30001.611 Ruei 20160616

082.30003.0221

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH(CLOCK/CL)
Size: Custom | Document Number: Iroxbox2 | Rev: -1
Date: Thursday, March 09, 2017 | Sheet 18 of 107

PORT1 USB30 FRONT 1 (support charging)

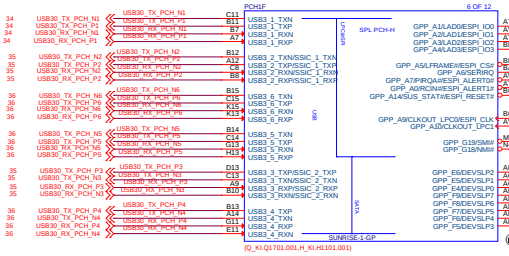
PORT2 USB30 FRONT 2

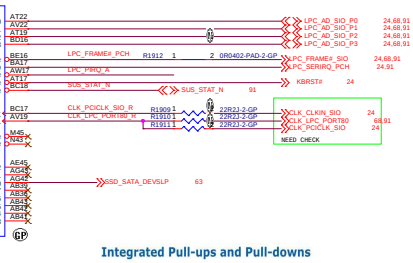
PORT4 USB30 REAR PORT 1

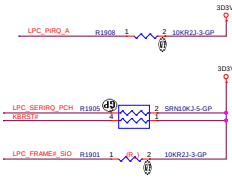
PORT4 USB30 REAR PORT 1

PORT3 USB30 FRONT 3

PORT4 USB30 REAR PORT 2



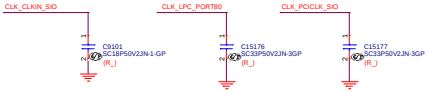




Integrated Pull-ups and Pull-downs

Signal	Resistor Type	Value	Notes
LAD[3:0]	Pull-up	15 ~ 40 KΩ	

sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe /LAN	PCIe	PCIe	PCIe



Reserve C9101, C15176, C15177 for 24MHz EMI
20160419 Ruei

<Core Design>

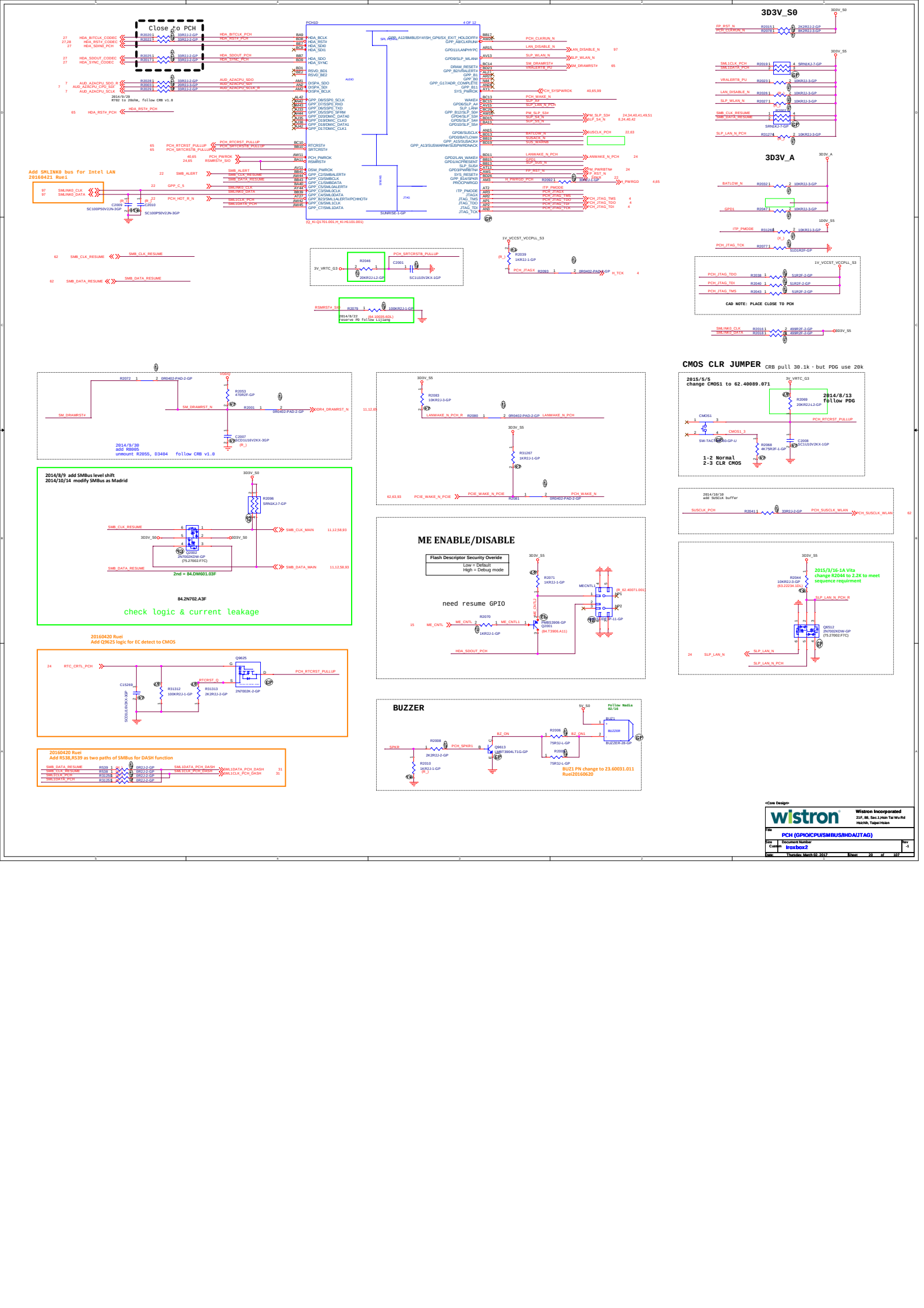
wistron

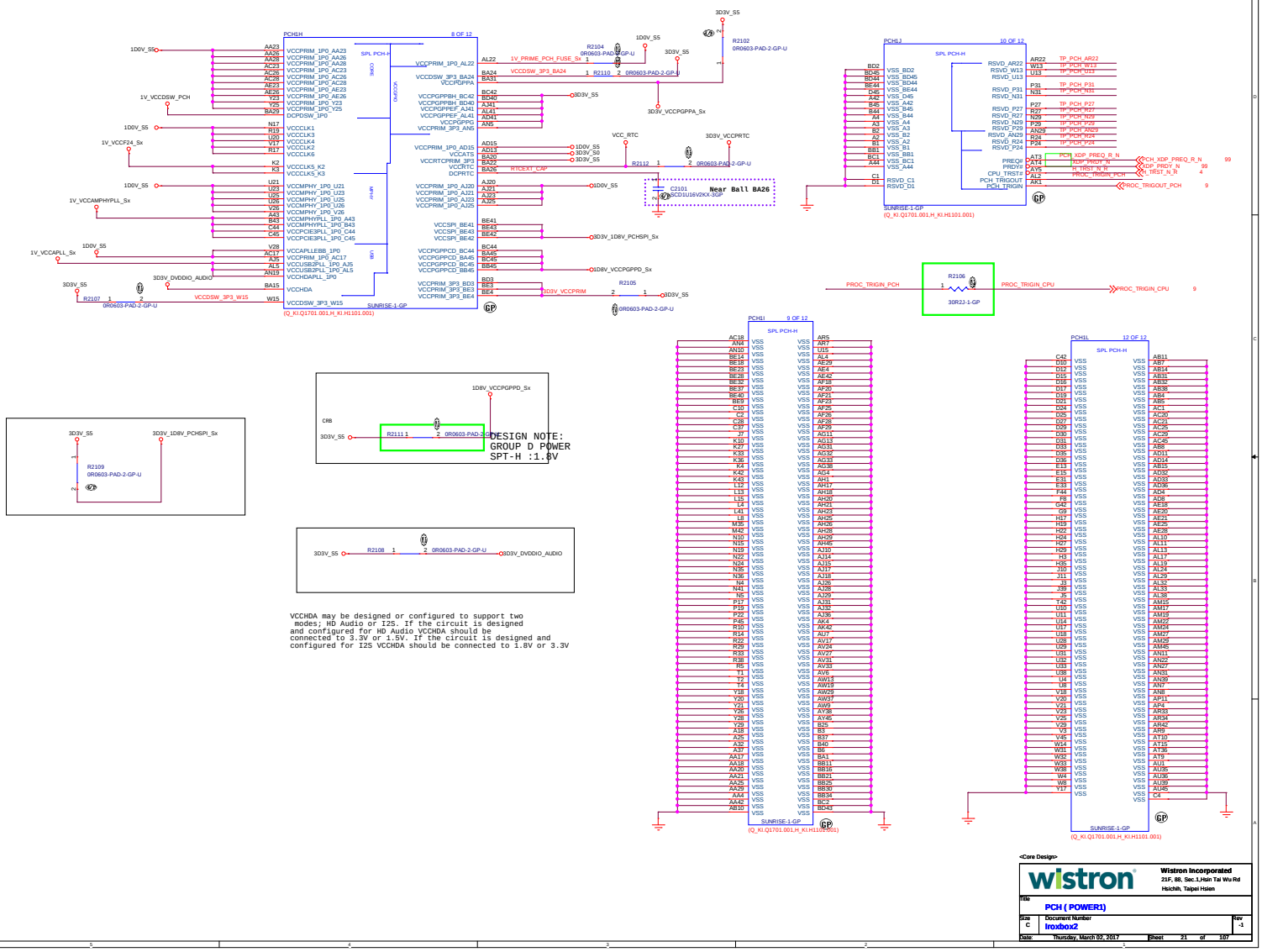
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (USB/ESPI

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 19 of 107


Close to PCH
PCH1D
4 OF 12
HDA_BITCLK_CODEC
HDA_RST#_CODEC
HDA_SDIN0_PCH
HDA_SDOUT_CODEC
HDA_SYNC_CODEC
HDA_BITCLK_PCH
HDA_RST#_PCH
HDA_SDOUT_PCH
HDA_SYNC_PCH
HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDO
HDA_SYNC
RSVD_BD1
RSVD_BE2
DISPA_SDO
DISPA_SDI
DISPA_BCLK
AUD_AZACPU_SDO_R
AUD_AZACPU_CPG_SDI
AUD_AZACPU_SCLK
AUD_AZACPU_SDO
AUD_AZACPU_SDI
AUD_AZACPU_SCLK_R
AUDIO
2014/9/29
R782 to 20ohm, follow CRB v1.0
HDA_RST#_PCH
PCH_RTCRST_PULLUP
PCH_SRTCRSTB_PULLUP
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#_SIO
DSW_PWROK
SMB_ALERT
SMB_CLK_RESUME
SMB_DATA_RESUME
GPP_C_5
PCH_HOT_R_N
SMLINK0_CLK
SMLINK0_DATA
SMLCLK_PCH
SMLDATA_PCH
GPP_C0/SMBALERT#
GPP_C1/SMBCLK
GPP_C2/SMBDATA
GPP_C3/SMLALERT#/PCHHOT#
GPP_C4/SMLCLK
GPP_C5/SMLDATA
GPP_B23/SMLALERT#/PCHHOT#
GPP_C6/SMLCLK
GPP_C7/SMLDATA
Add SMLINK0 bus for Intel LAN
20160421 Ruei
SC100P50V2JN-3GP
SUNRISE-1-GP
(Q_KI.Q1701.001.H_KI.H1101.001)
SM_DRAMRST#
DDR4_DRAMRST_N
2014/9/30
add R8005
unmount R2055, D3404 follow CRB v1.0
2014/8/9 add SMBus level shift
2014/10/14 modify SMBus as Madrid
SMB_CLK_MAIN
SMB_DATA_MAIN
2nd = 84.DM601.03F
84.2N702.A3F
check logic & current leakage
20160420 Ruei
Add Q9625 logic for EC detect to CMOS
RTC_CRTL_PCH
RTCRST_Q
PCH_RTCRST_PULLUP
2N7002K-2-GP
20160420 Ruei
Add R538,R539 as two paths of SMBus for DASH function
SMB_DATA_RESUME
SMB_CLK_RESUME
SMLCLK_PCH
SMLDATA_PCH
SMLDATA_PCH_DASH
SMLCLK_PCH_DASH
3V_VRTC_G3
PCH_SRTCRSTB_PULLUP
C2001
SC1U10V2KX-1GP
1V_VCCST_VCCPLL_S3
PCH_JTAGX
PCH_TCK
RSMRST#_SIO
2014/8/22
(64.10025.6DL)
reserve PD follow LiJiang
3D3V_S0
3D3V_S5
3D3V_A
1D0V_S5
SML1CLK_PCH
SML1DATA_PCH
VRALERTB_PU
LAN_DISABLE_N
SLP_WLAN_N
SMB_CLK_RESUME
SMB_DATA_RESUME
SLP_LAN_N_PCH
SRN1KJ-7-GP
SRN4K7J-7-GP
BATLOW_N
GPD1
ITP_PMODE
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TMS
CAD NOTE: PLACE CLOSE TO PCH
SMLINK0_CLK
SMLINK0_DATA
CMOS CLR JUMPER
CRB pull 30.1k，but PDG use 20k
2015/5/5
change CMOS1 to 62.40089.071
2014/8/13
follow PDG
1-2 Normal
2-3 CLR CMOS
2014/10/10
add SUSCLK buffer
SUSCLK_PCH
PCH_SUSCLK_WLAN
ME ENABLE/DISABLE
Flash Descriptor Security Overide
Low = Default
High = Debug mode
need resume GPIO
ME_CNTL
ME_CNTL1
HDA_SDOUT_PCH
2015/3/16-1A Vita
change R2044 to 2.2K to meet sequence requirment
BUZZER
SPKR
PCH_SPKR1
BZ_ON
BZ_ON1
BUZ1 PN change to 23.60031.011
Ruei20160620
Follow Nadia 02/16
<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
HsiChih, Taipei Hsien
Title
PCH (GPIO/CPU/SMBUS/HDA/JTAG)
Size
Custom
Document Number
Irouxbox2
Rev
-1
Date:
Thursday, March 02, 2017
Sheet
28
of
107



DESIGN NOTE:
GROUP D POWER
SPT-H :1.8V

VCCHDA may be designed or configured to support two modes; HD Audio or I2S. If the circuit is designed and configured for HD Audio VCCHDA should be connected to 3.3V or 1.5V. If the circuit is designed and configured for I2S VCCHDA should be connected to 1.8V or 3.3V

<Core Design>

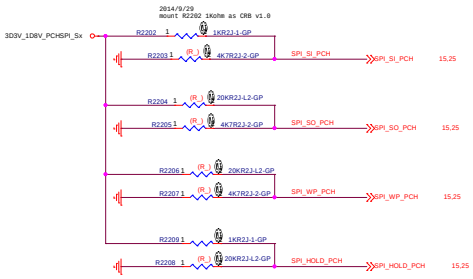
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (POWER1)

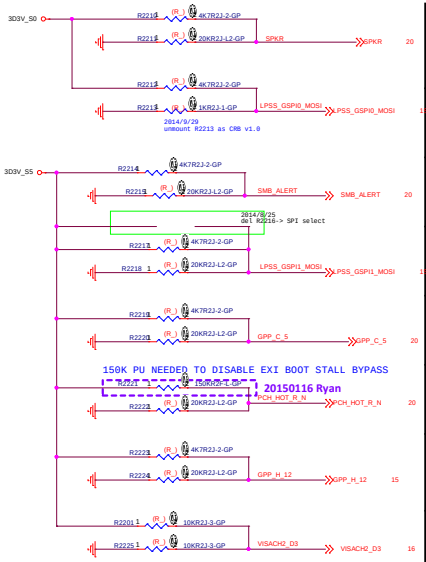
Size	Document Number	Rev
C	lroxbox2	-1

Date: Thursday, March 02, 2017 Sheet 21 of 107

PCH STRAP FUNCTIONS



SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU



SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
PCH_PORT80_LED (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistoris disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

Need check
Though CRB use LPC to connect EC
This pin doen't pull down

Follow ROSA / D7 trigerfish & Lily / M800 skylake project.

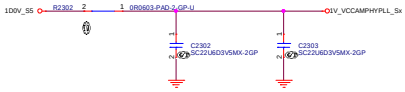
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

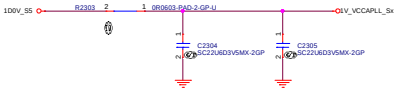
Title: PCH_(POWER2)

Size	Document Number	Rev
C	lroxbox2	-1

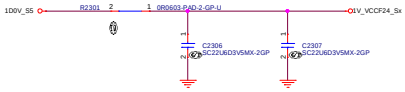
Date: Thursday, March 02, 2017 Sheet 22 of 107



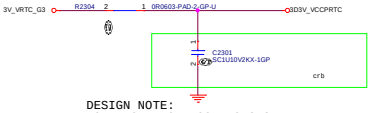
DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A42,A43, AND B43



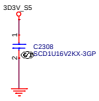
DESIGN NOTE:
PLACE HOLDER FOR VCCAUSB_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19



DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3

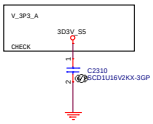


DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22

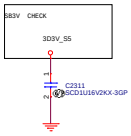


DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41

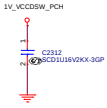
DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26



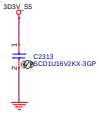
DESIGN NOTE:
EDGE CAP FOR VCCPUSBDSW_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN W15



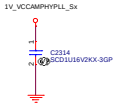
DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20



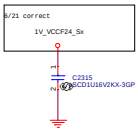
DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29



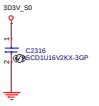
DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41



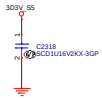
DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42,A43 AND B43



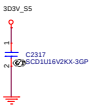
DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3



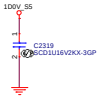
DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13



DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40



DESIGN NOTE:
BOAED CAP FOR VCCPHVC_3P3(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN15



DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26,AND AC17

<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: PCH Power CAP		
Size: C	Document Number: lroxbox2	Rev: -1
Date: Thursday, March 02, 2017	Sheet 23 of 107	

AMP

LPC

Power Manager

CLOCK

SMBUS

PECI

SPI

OTHERS

HW Monitor

VRD

PCH

PECI follow design guide--Kai 0319

Reset signals

REMINE LAYOUT

For AC OFF SEQUENCE

ECIO SPI ROM

1. layout trace is as far as possible short
2. Pull-up resistor 3K8R near SPI Flash

Add PROCHOT# Logic by EC control
Ruei 20160617

AddUSB OBL Logic by EC control
Ruei 20160721

COM

To SB 3/5 EUP control

PWRBT Signal

Power Good 3V

0.8VCC3~3.63_PWR_GOOD
SIO delay:
20ms~3.2s
000s 010s 100s
400ms / 51ms / 200ms

Add debug Header 20160630

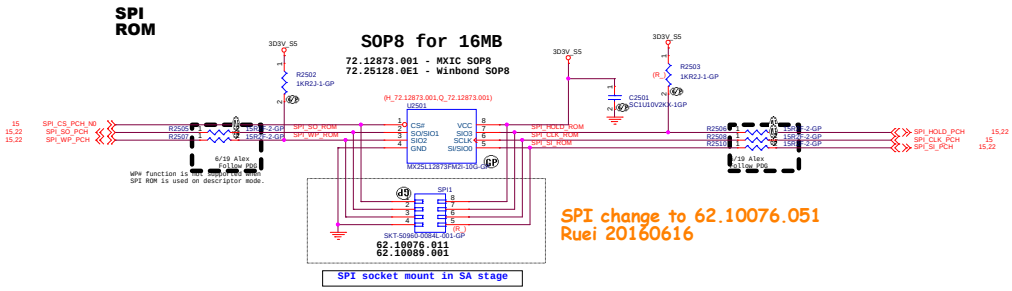
Add discharger for VCC3 Ruei 20160630

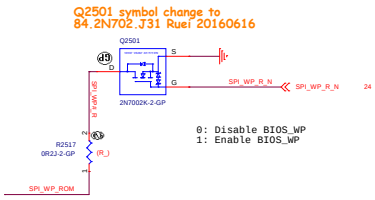
Chassis Intrusion

LPC group mdoel can pull high--Kai 0319
RN7990 change to 3D3V_S0--Kai 0328

Reserved EUP_DSW_SEL
JP1=1 EUP
JP1=0 DSW
--Kai 0315
Add pull down--Kai 0319

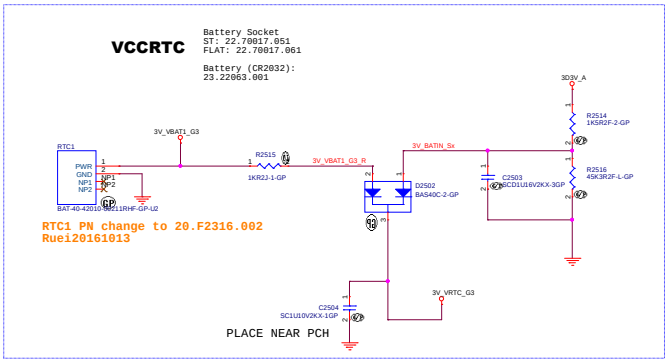
wistron
Wistron Incorporated
21F-23, No. 3,Sec Ta-Hsi Rd.
Hsichih, Taipei Hsien





2014/8/6
add SPI1 62.10076.011

Single Flash Device: 15ohom
Dual Flash Device: 33ohm



SKL Platforms – SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

An Intel internal debug strap is implemented on the SPI0_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

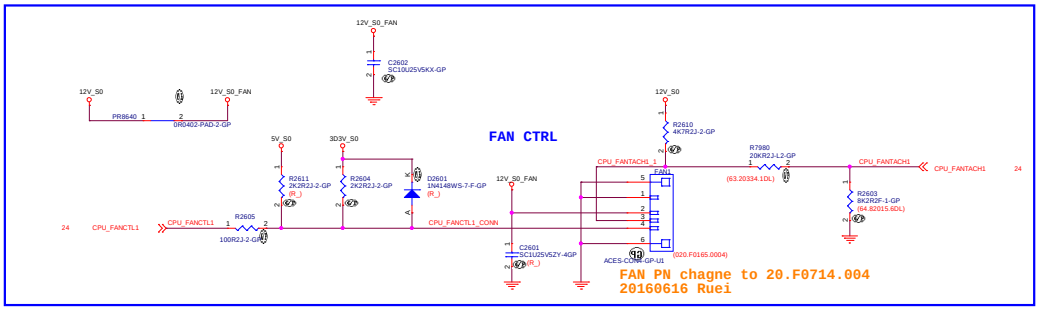
Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: Flash&RTC		
Size: C	Document Number: lroxbox2	Rev: -1
Date: Thursday, March 02, 2017	Sheet 25 of 107	

FAN design follow Hangzhou
20160623 Ruei



FAN PN chagne to 20.F0714.004
20160616 Ruei

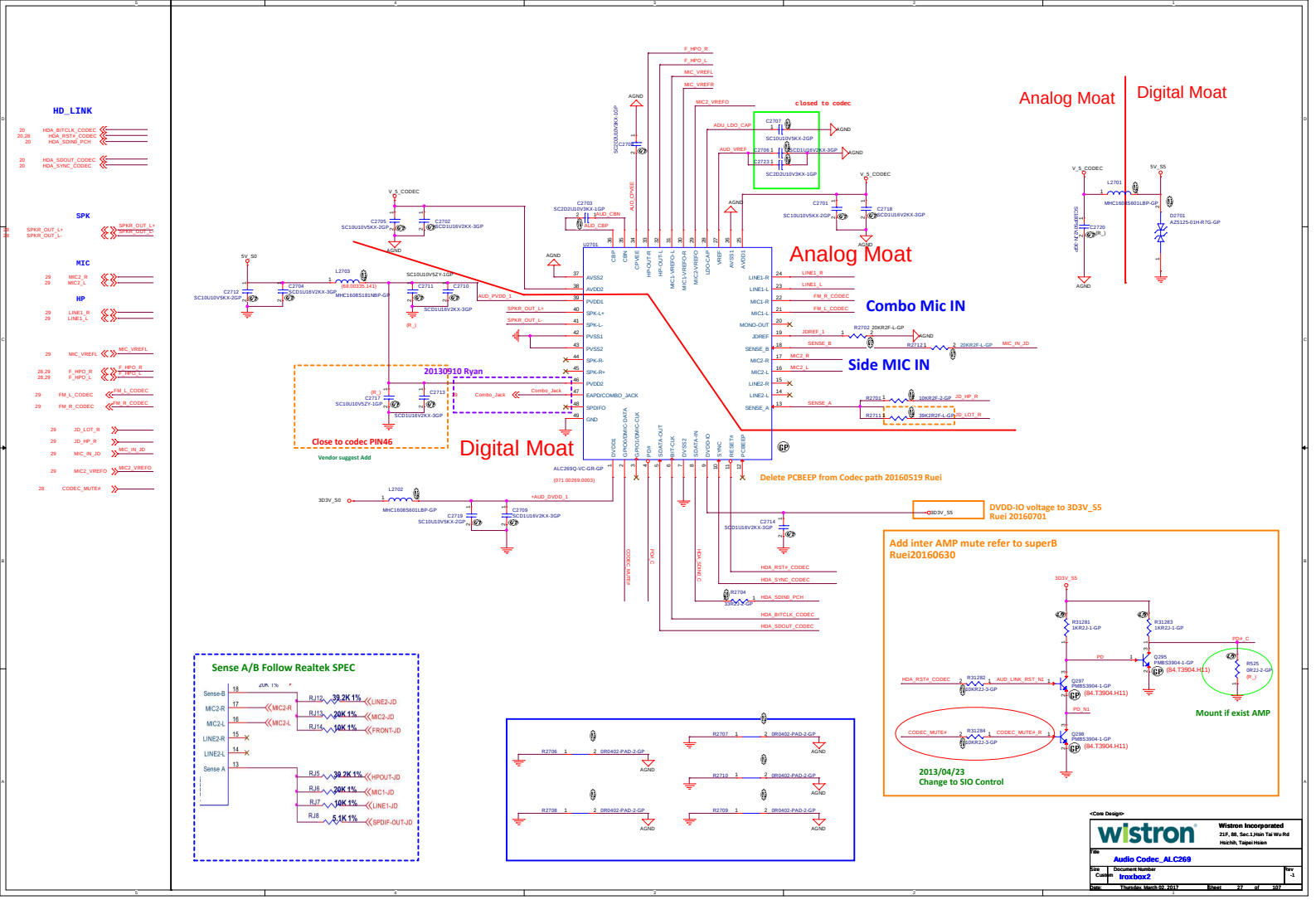
<Core Design>

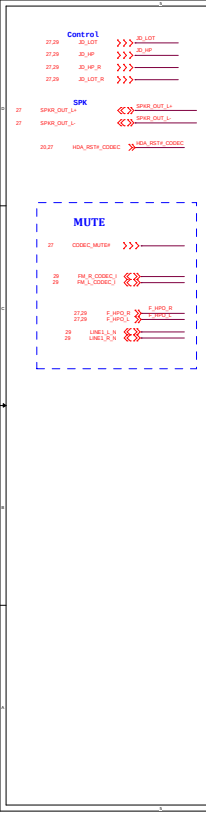
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

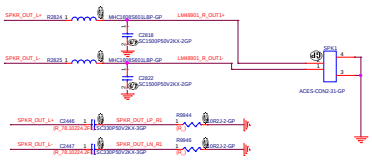
Title: Thermal & FAN

Size	Document Number	Rev
Custom	Inoxbox2	-1

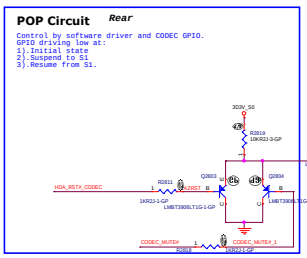
Date: Thursday, March 02, 2017 Sheet 26 of 107

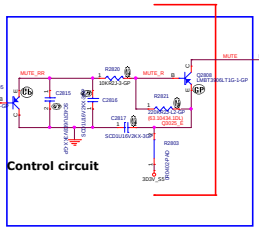

HD_LINK
SPK
MIC
HP
Analog Moat
Digital Moat
Combo Mic IN
Side MIC IN
closed to codec
20130910 Ryan
Close to codec PIN46
Vendor suggest Add
Delete PCBEEP from Codec path 20160519 Ruei
DVDD-IO voltage to 3D3V_S5
Ruei 20160701
Add inter AMP mute refer to superB
Ruei20160630
Mount if exist AMP
2013/04/23
Change to SIO Control
Sense A/B Follow Realtek SPEC
ALC269Q-VC-GR-GP
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Audio Codec_ALC269
Itoxbox2



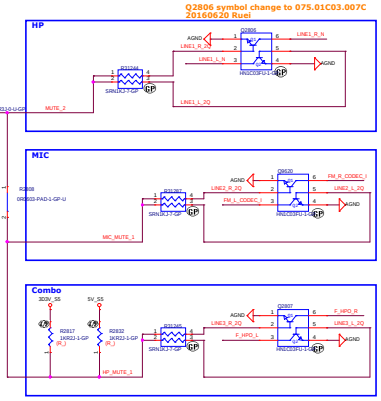


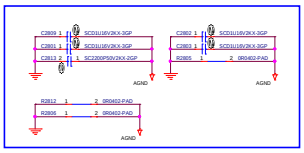
SPK1 Pn change to 20.F1606.002
20160616 Ruei

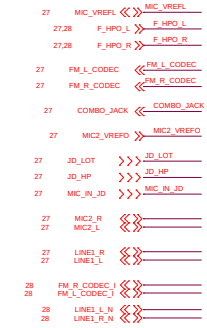


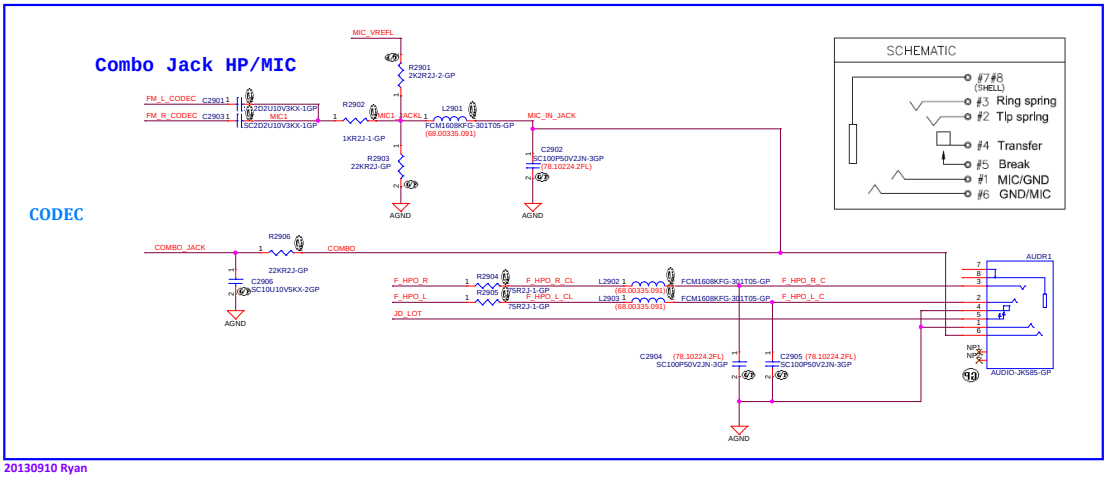


Q2806 symbol change to 075.01C03.007C
20160620 Ruei

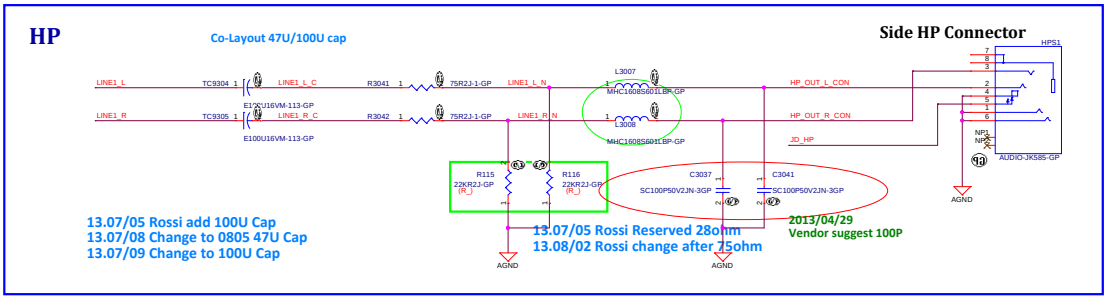


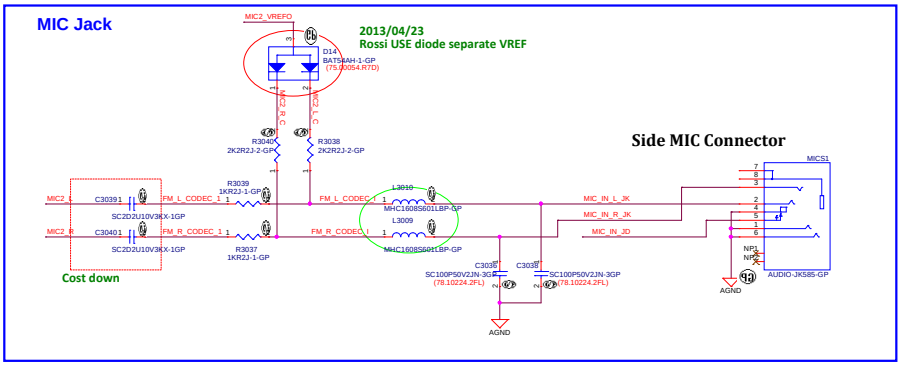


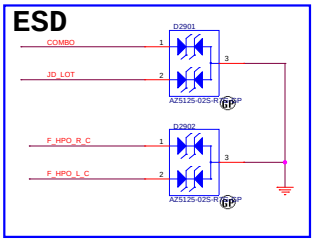


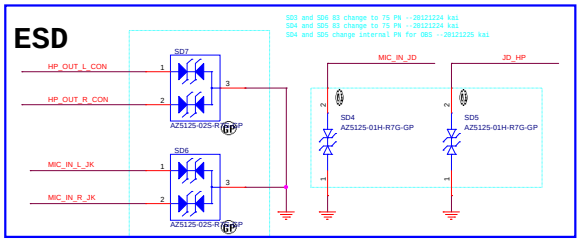


20130910 Ryan









<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: Audio IO_Combo HP_MIC

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 29 of 107

Reserved

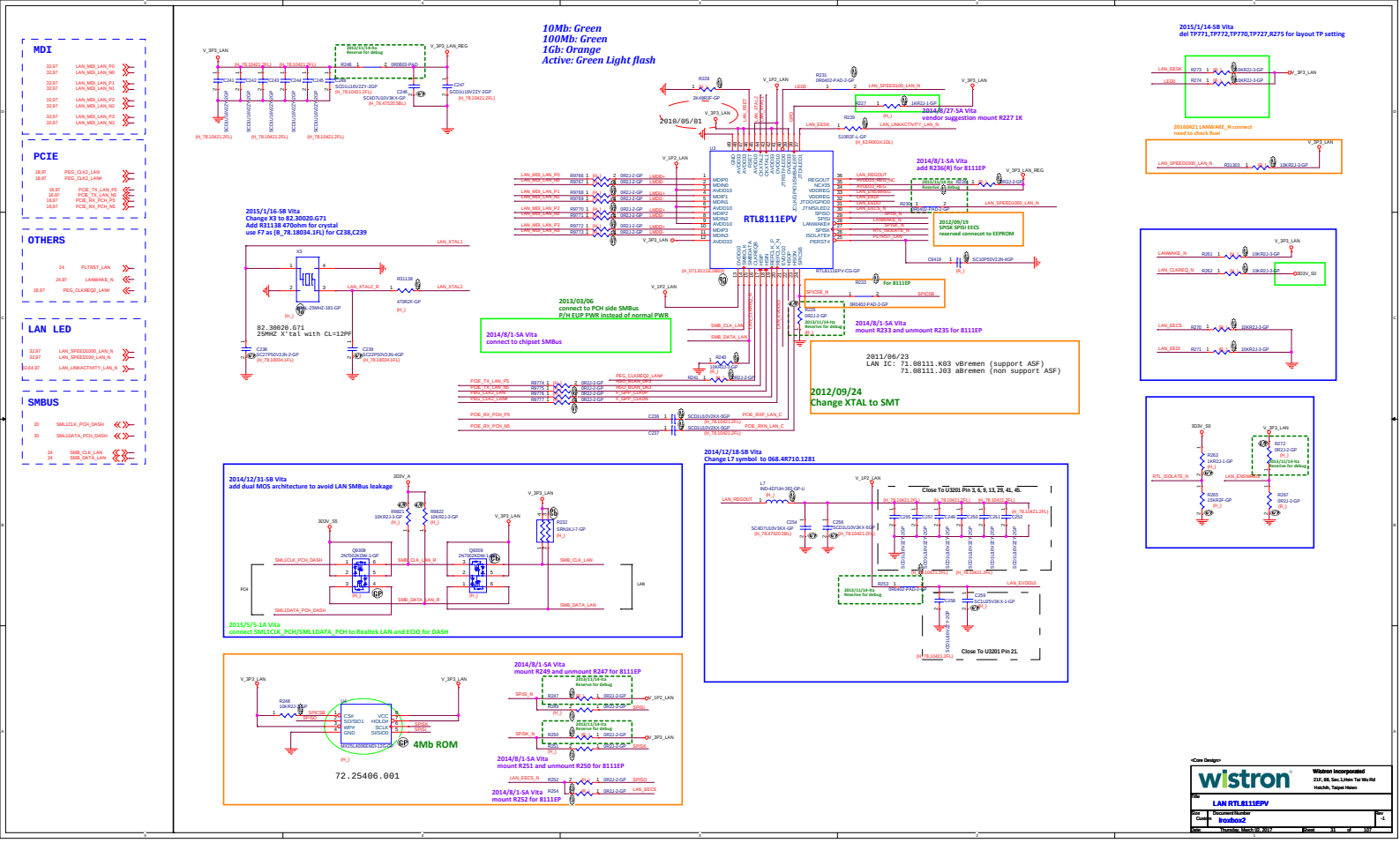
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Audio IO_Rear_(R)

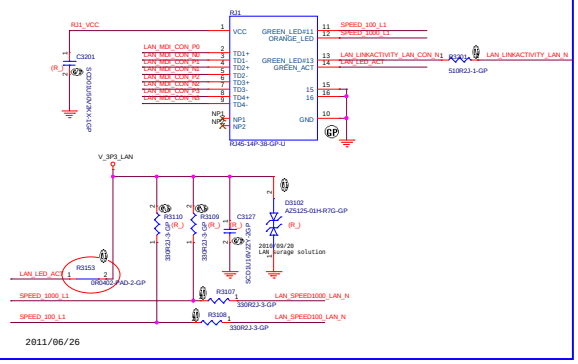
Size	Document Number	Rev
C	Iroxbox2	-1

Date: Thursday, March 02, 2017 Sheet 30 of 107


MDI
PCIE
OTHERS
LAN LED
SMBUS
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Green Light flash
RTL8111EPV
2010/05/01
2015/1/16-SB Vita
Change X3 to 82.30020.G71
Add R31138 470ohm for crystal
use F7 as (8_78.18034.1FL) for C238,C239
82.30020.671
25MHZ X'tal with CL=12PF
2013/03/06
connect to PCH side SMBus
P/H EUP PWR instead of normal PWR
2014/8/1-SA Vita
connect to chipset SMBus
2012/09/24
Change XTAL to SMT
2011/06/23
LAN IC: 71.08111.K03 vBremen (support ASF)
71.08111.J03 aBremen (non support ASF)
2014/12/31-SB Vita
add dual MOS architecture to avoid LAN SMBus leakage
2015/5/5-1A Vita
connect SML1CLK_PCH/SML1DATA_PCH to Realtek LAN and EC/O for DASH
4Mb ROM
72.25406.001
2014/8/1-SA Vita
mount R249 and unmount R247 for 8111EP
2014/8/1-SA Vita
mount R251 and unmount R250 for 8111EP
2014/8/1-SA Vita
mount R252 for 8111EP
2014/12/18-SB Vita
Change L7 symbol to 068.4R710.1281
Close To U3201 Pin 3, 6, 9, 13, 23, 41, 45.
Close To U3201 Pin 21.
2015/1/14-SB Vita
del TP771,TP772,TP770,TP727,R275 for layout TP setting
20160421 LANWAKE_N connect
need to check Rom!
2014/8/27-SA Vita
vendor suggestion mount R227 1K
2014/8/1-SA Vita
add R236(R) for 8111EP
2013/09/19
SPI5K SPI5I EECS
reserved connecot to EEPROM
2014/8/1-SA Vita
mount R233 and unmount R235 for 8111EP
For 8111EP
Reserve for debug
Reserve for EEPROM
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
LAN RTL8111EPV
Custom
Ironbox2
Thursday, March 09, 2017

31,97 LAN_SPEED100_LAN_N
31,97 LAN_MDI_LAN_P0
31,97 LAN_MDI_LAN_N0
31,97 LAN_MDI_LAN_P1
31,97 LAN_MDI_LAN_N1
31,97 LAN_MDI_LAN_P2
31,97 LAN_MDI_LAN_N2
31,97 LAN_MDI_LAN_P3
31,97 LAN_MDI_LAN_N3
31,97 LAN_SPEED1000_LAN_N
31,64,97 LAN_LINKACTIVITY_LAN_N

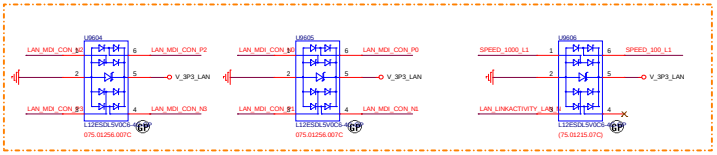
RJ1 symbol change to 022.10001.01U1



2011/06/26

	Link	Act
PCB		

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1 Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: RJ45&Transformer

Size: Custom | Document Number: lnxxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 32 of 107

Reserved

<Core Design>

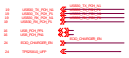
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Card reader (R_)

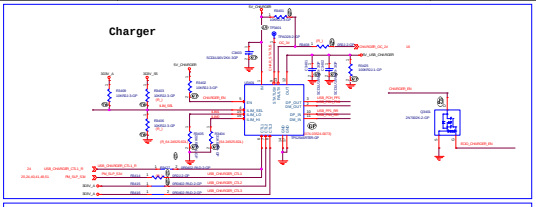
Size	Document Number	Rev
C	lroxbox2	-1

Date: Thursday, March 02, 2017 Sheet 33 of 107

USB3.0 SIDE CONNECTOR



Charger



Truth Table for TPS2540A/TPS2543/TPS2546

ACPI Control	CTL1	CTL2	CTL3	ILIM_SEL	PWR	Control Mode
S0	1	1	1	1	+5V_MAIN	CDP
S1	1	1	1	1	+5V_MAIN	CDP
S3	1	1	1	1	ATX_5VSB	CDP
S4	0	1	1	1	ATX_5VSB	DCP
S5	0	1	1	1	ATX_5VSB	DCP
S5_EuP	0	1	1	1	ATX_5VSB	DCP
G3->S5	0	1	1	1	ATX_5VSB	DCP

Pin attention to CTRL1 and CTRL3 SPIO pin selection

	CTRL1	CTRL2	CTRL3	ILIM_SEL
S0	High	High	High	High
S3	Low	High	High	High
S4	Low	High	High	High
S5	Low	High	High	High

USB 3.0 Connector Pin definition

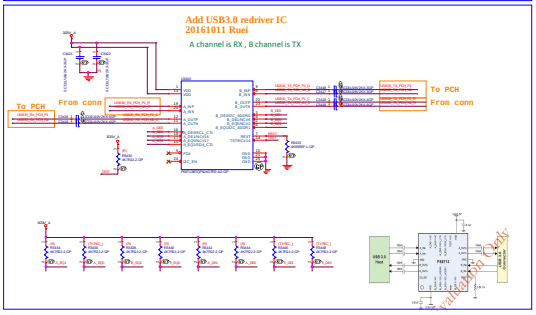
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Type A Charge Port (Front)

USB3071 PN change to 22.10339.F41
Ruel 20160602

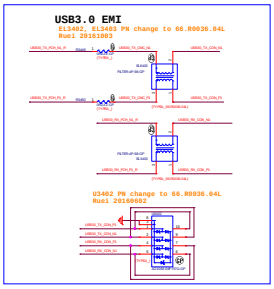
Add USB3.0 redriver IC
20161011 Ruel

A channel is RX , B channel is TX



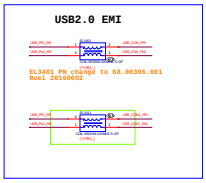
USB3.0 EMI

EL3402, EL3403 PN change to 66.R0036.04L
Ruel 20161003



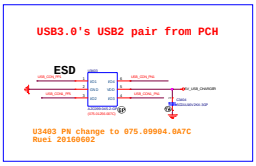
U3402 PN change to 66.R0036.04L
Ruel 20160602

USB2.0 EMI

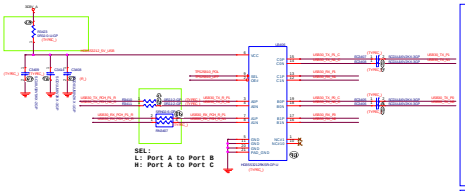


EL3401 PN change to 66.00396.001
Ruel 20160602

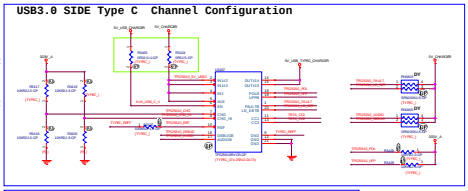
USB3.0's USB2 pair from PCH



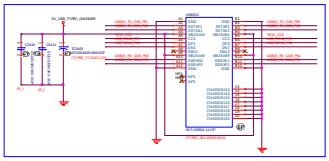
U3403 PN change to 075.09904.0A7C
Ruel 20160602



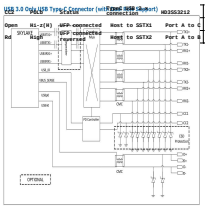
USB3.0 SIDE Type C Channel Configuration



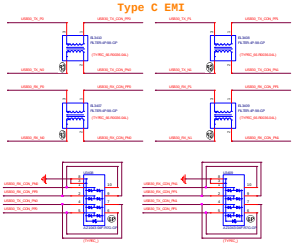
USB3.0 Type C connector change to 062.10009.0811 by F7 20161027



SEL:
L: Port A to Port B
H: Port A to Port C



Type C EMI



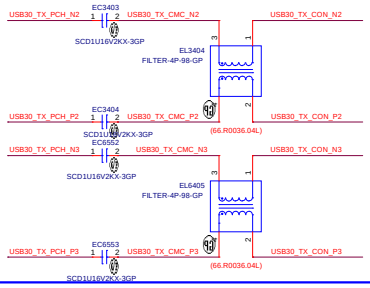
19 USB30_RX_PCH_N2
19 USB30_RX_PCH_P2
19 USB30_TX_PCH_N2
19 USB30_TX_PCH_P2

16 USB_PCH_PP2
16 USB_PCH_PN2

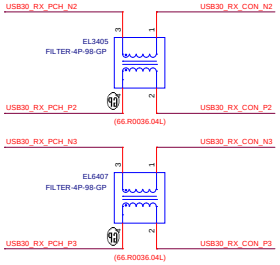
19 USB30_RX_PCH_N3
19 USB30_RX_PCH_P3
19 USB30_TX_PCH_N3
19 USB30_TX_PCH_P3

16 USB_PCH_PP3
16 USB_PCH_PN3

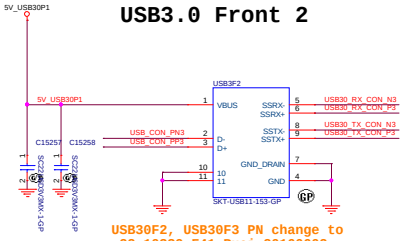
USB3.0 EMI



EL3404, EL6405, EL3405, EL6407 PN change to 66.R0036.04L Ruei 20161003

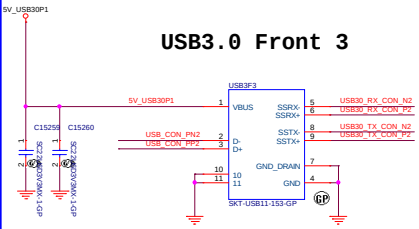


USB3.0 Front 2

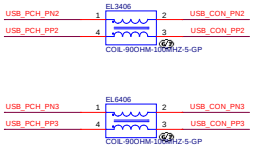


USB30F2, USB30F3 PN change to 22.10339.F41 Ruei 20160602

USB3.0 Front 3

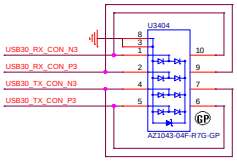


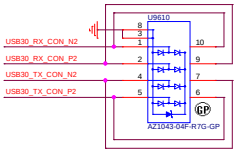
USB2.0 EMI



EL3406, EL6406 PN change to 68.00396.001 Ruei 20160603

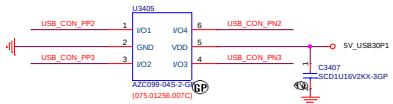
USB3.0 ESD





U3404, U9610 PN change to 075.01043.0073 Ruei 20160603

USB2.0 ESD



U3405 PN change to 075.09904.0A7C Ruei 20160603

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

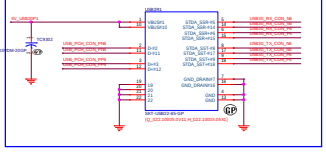
Title: USB_Front Port

Size	Document Number	Rev
Custom	Iroxbox2	-1

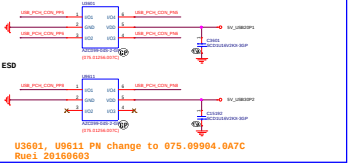
Date: Thursday, March 02, 2017 Sheet 35 of 107

USB3R1 PN change to 022.10005.0V11 refer to SophiaRuei 20160616

Dual USB3.0 REAR PORT1



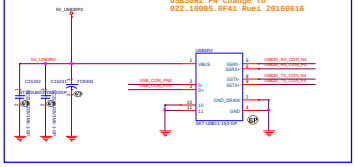
USB2.0 ESD



U3601, U9611 PN change to 075.09904.0A7C Ruei 20160603

USB3.0 REAR PORT2

USB30R2 PN change to 022.10005.0F41 Ruei 20160616

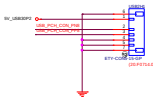


USB 3.0 Connector Pin definition

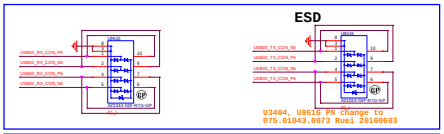
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB2.0 Rear Header(Option)

USB2H1 PN change to 20.F1868.005 Ruei 20160616

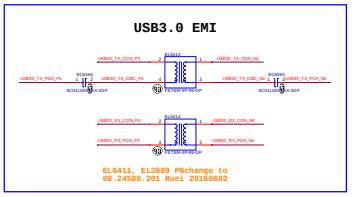


ESD



U3404, U9615 PN change to 075.01043.0073 Ruei 20160603

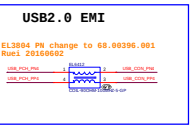
USB3.0 EMI



EL6411, EL3809 PNchange to 68.24500.201 Ruei 20160603

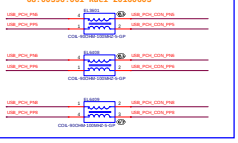
USB2.0 EMI

EL3804 PN change to 68.00396.001 Ruei 20160602



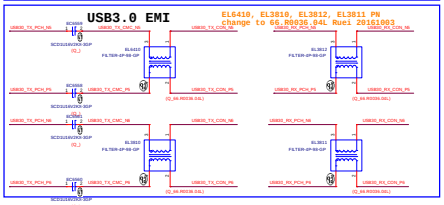
USB2.0 EMI

EL3601, EL6408, EL6409 PN change to 68.00396.001 Ruei 20160603

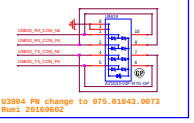


USB3.0 EMI

EL6410, EL3810, EL3812, EL3811 PN change to 68.00936.04L Ruei 20151003

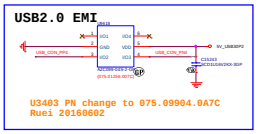


USB3.0 EMI



U3804 PN change to 075.01043.0073 Ruei 20160602

USB2.0 EMI



U3403 PN change to 075.09904.0A7C Ruei 20160602

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: USB_REAR PORT

Custom: Document Number: Irosbox2 Rev: A

Date: Thursday, March 02, 2017 Sheet 36 of 107

Reserved

Reserved

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: 937_USB30_FRONT HEADER_(R)

Size: A | Document Number: Rev: 1.0
Custom | Date: Friday, July 09, 2010 | Sheet 37 of 39

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB30_REAR PORT_(R)

Size	Document Number	Rev
C	DP Iroxbox2	-1

Date: Thursday, March 09, 2017 Sheet 38 of 107

Reserved

<Core Design>

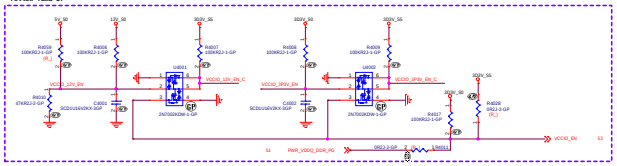
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB30_(R)

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 39 of 107

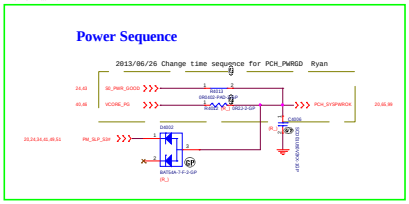
2014/9/23
VCCIO ENABLE
follow Yaha D7

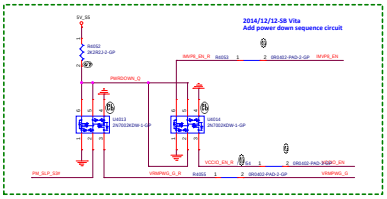


2014/8/7
follow Madrid

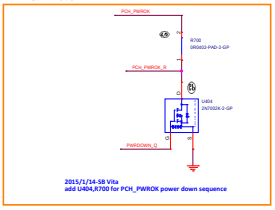
Power Sequence

2013/06/26 Change time sequence for PCH_PWRGD Ryan



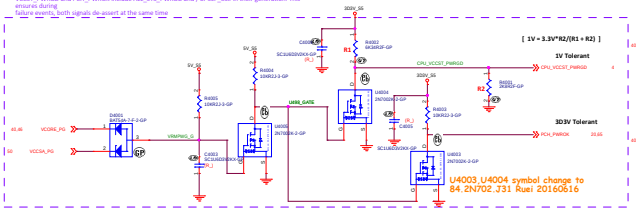


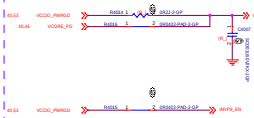
Add logic U404 for power down sequence
Ruei20160624



2014/8/7
follow Veneno

Note:
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both
VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during
failure events, both signals de-assert at the same time

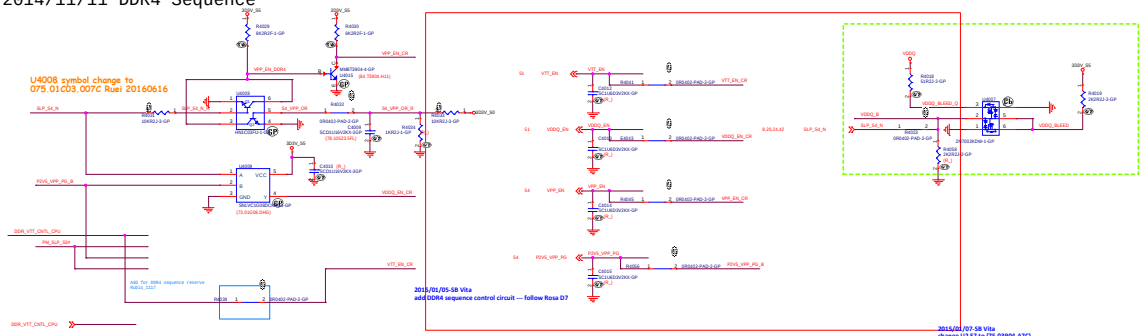


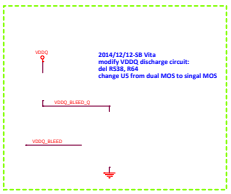


1> VCCIO -> VCORE -> VCCSA (current)
2> VCCIO -> VCORE/VCCSA both

2014/11/11 DDR4 Sequence

U4008 symbol change to
075.01C03_007C Ruei 20160616





2015/01/07-SB Vita
change U2 F7 to (75.03904.A7C)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

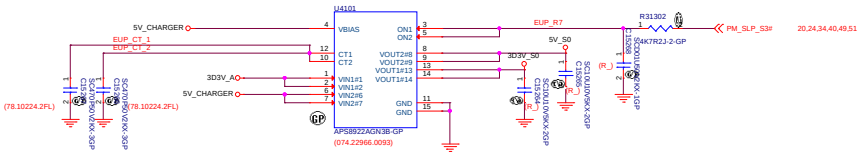
Title: Power Plane EN Sequence
Size: C | Document Number: Irqxbox2 | Rev: 1A
Date: Thursday, March 08, 2007 | Sheet: 46 of 49

ANNIE Run Power

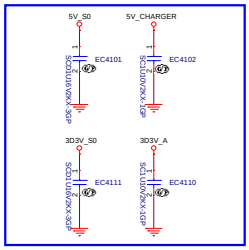
5V_S0 loading
3* 5V S0 current of 2.5" HDD = 3*1A=3A < 6A Vout spec

3D3V_S0 loading = 1A + 0.5A + 0.025A = 1.525A < 6A Vout spec
2*DP* 1A
4* SATA re-driver 4* 0.125 =0.5A
Codec 0.025A

Modify 3D3V_S0/5V_S0 Logic Control as Load Switch
Ruei20160707

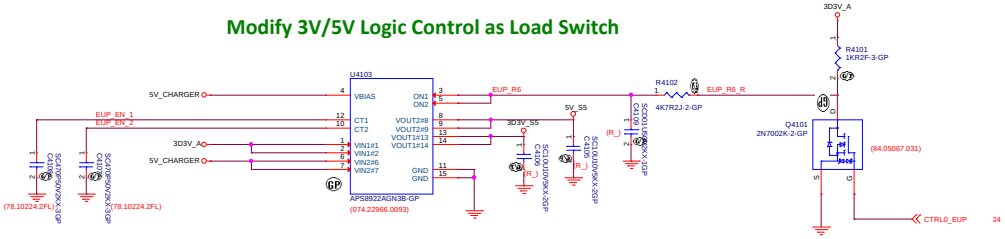


must be closed U4101

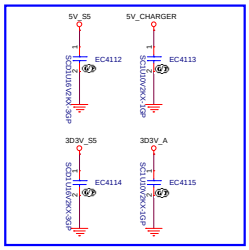


EUP Power

Modify 3V/5V Logic Control as Load Switch



must be closed U4103



<Core Design>

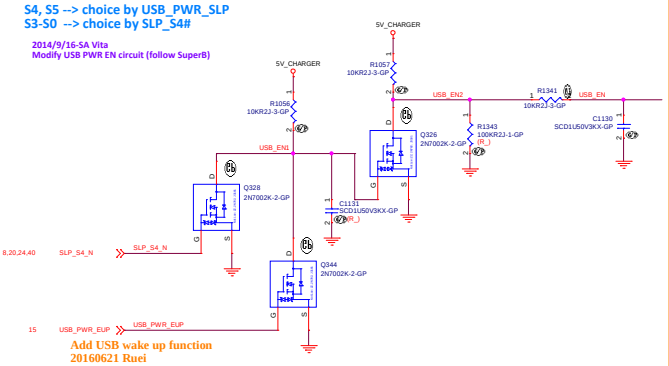
wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: Switch power_DS3		
Size: Custom	Document Number: roxbox2	Rev: -1
Date: Thursday, March 02, 2017	Sheet 41 of 107	

24 USB_PWR_EUP

	S5	S4	S3-S0		S5	S4	S3-S0	Status
USB_PWR_SLP	L	L	L	USB_EN	L	L	H	No Support S4 USB wake up
USB_PWR_SLP	L	H	L	USB_EN	L	H	L	Support S4 USB wake up

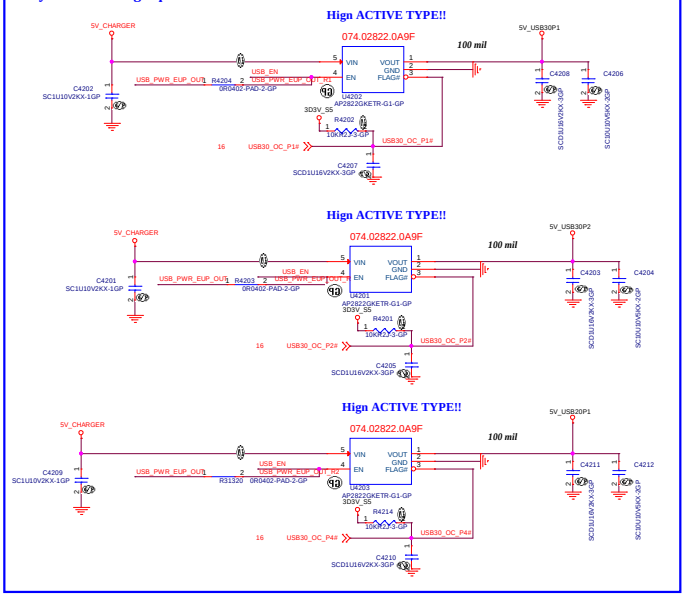
S4, S5 --> choice by USB_PWR_SLP
S3-S0 --> choice by SLP_S4#

2014/9/16-SA Vita
Modify USB PWR EN circuit (follow SuperB)



Add USB wake up function
20160621 Ruei

colay USB3S1 charger power



<Core Design>

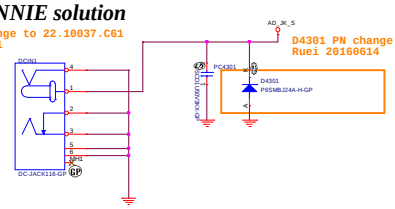
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Switch power
Size: Custom | Document Number: Iroxbox2 | Rev: -1
Date: Thursday, March 02, 2017 | Sheet 42 of 107

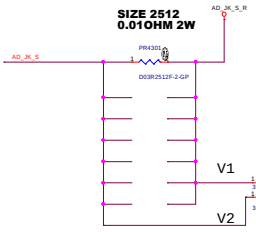
ANNIE solution

DCIN1 PN change to 22.10037.C61
Ruei 20160621

D4301 PN change to (83.P6SMB.HAG) by F7
Ruei 20160614

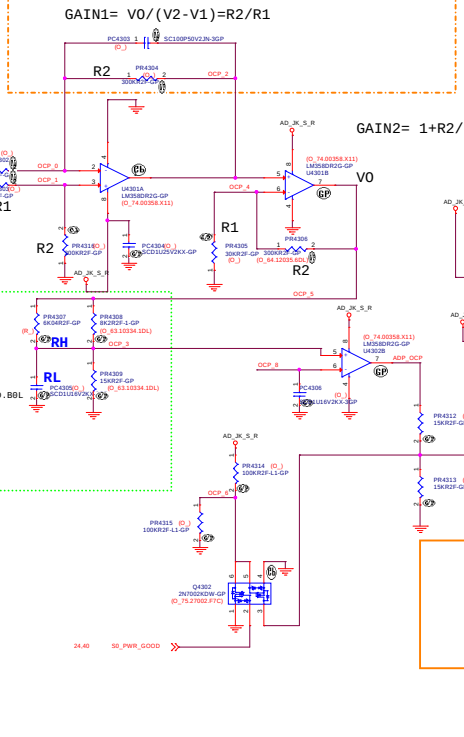


SIZE 2512
0.010HM 2W

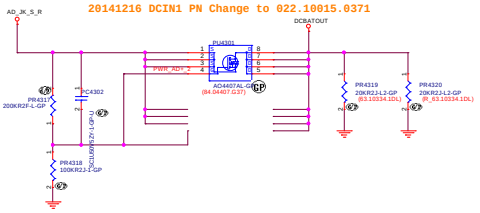


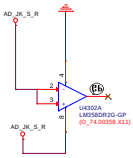
GAIN1= VO/(V2-V1)=R2/R1

GAIN2= 1+R2/R1

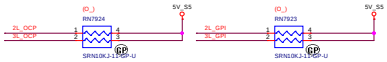


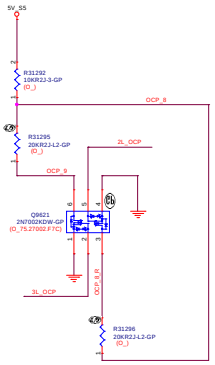
20141216 DCIN1 PN Change to 022.10015.0371





	1L	1L+2L	1L+3L	1L+2L	1L+2L+3L	1L+2L+3L
	65W	90W	90W	135W	135W	135W
	MB	VGA card +MB	MB+ extend HDD	VGA card (R7) + MB	VGA card + MB+ extend HDD	VGA card (R7) + MB+ extend HDD
(2L_GPI)	H	L	H	L	L	L
(2L_GPO)	H	L	H	L	L	L
(3L_GPI)	H	H	L	H	L	L
(3L_GPO)	H	H	L	L	L	L





<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DCIN JACK(BATT Conn)

Size: Custom | Document Number: Inxobox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 43 of 107

Reserved

<Core Design>

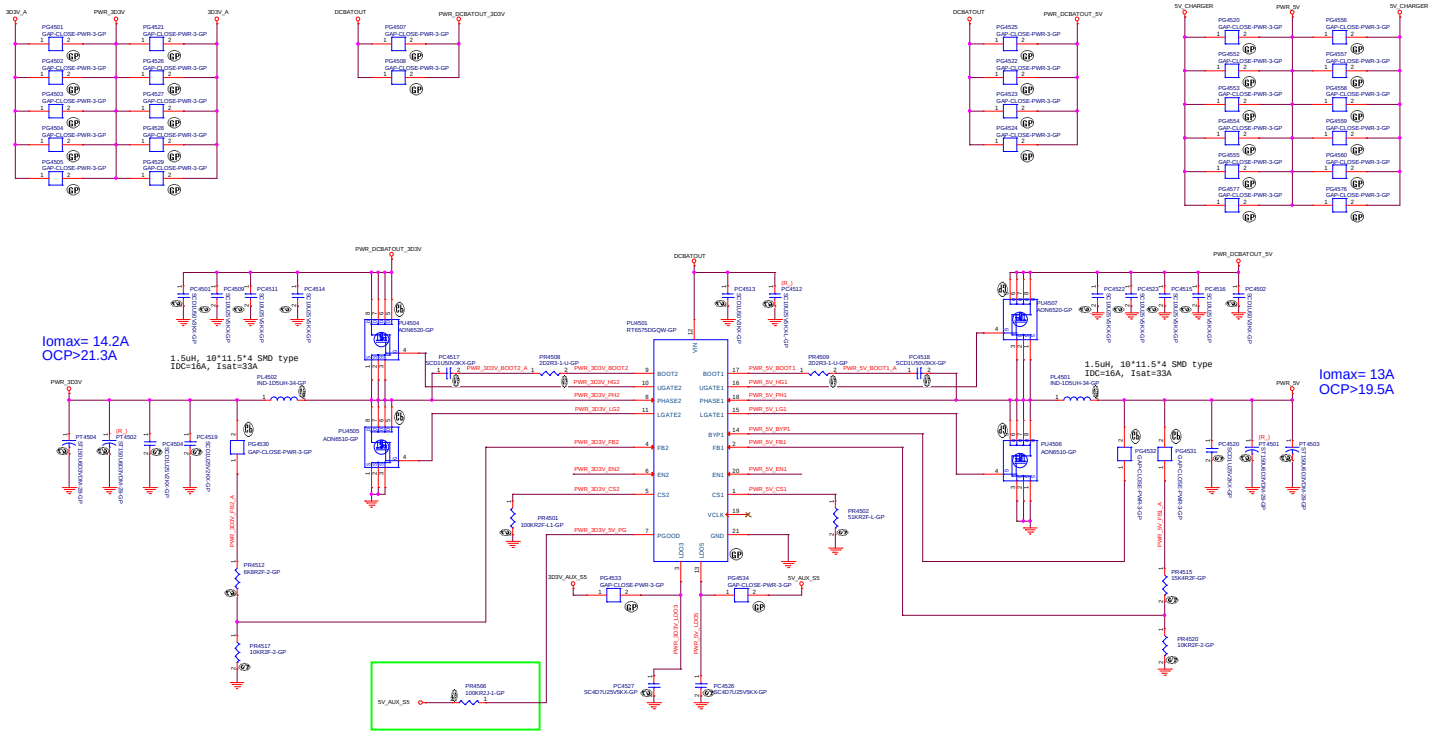
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

Title: OZ554A LED Converter_(8)

Size: A | Document Number: InsBox2 | Rev: A

Date: Tuesday, March 26, 2013 | Sheet: 23 of 28



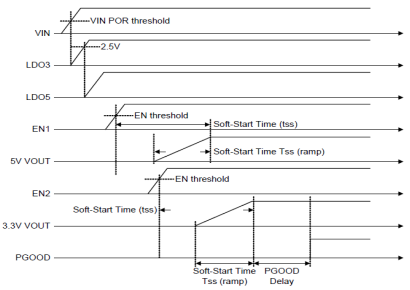
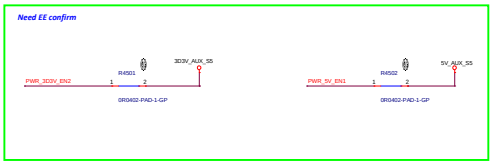


Figure 6. RT6575B Timing



<Core Design>

wistron

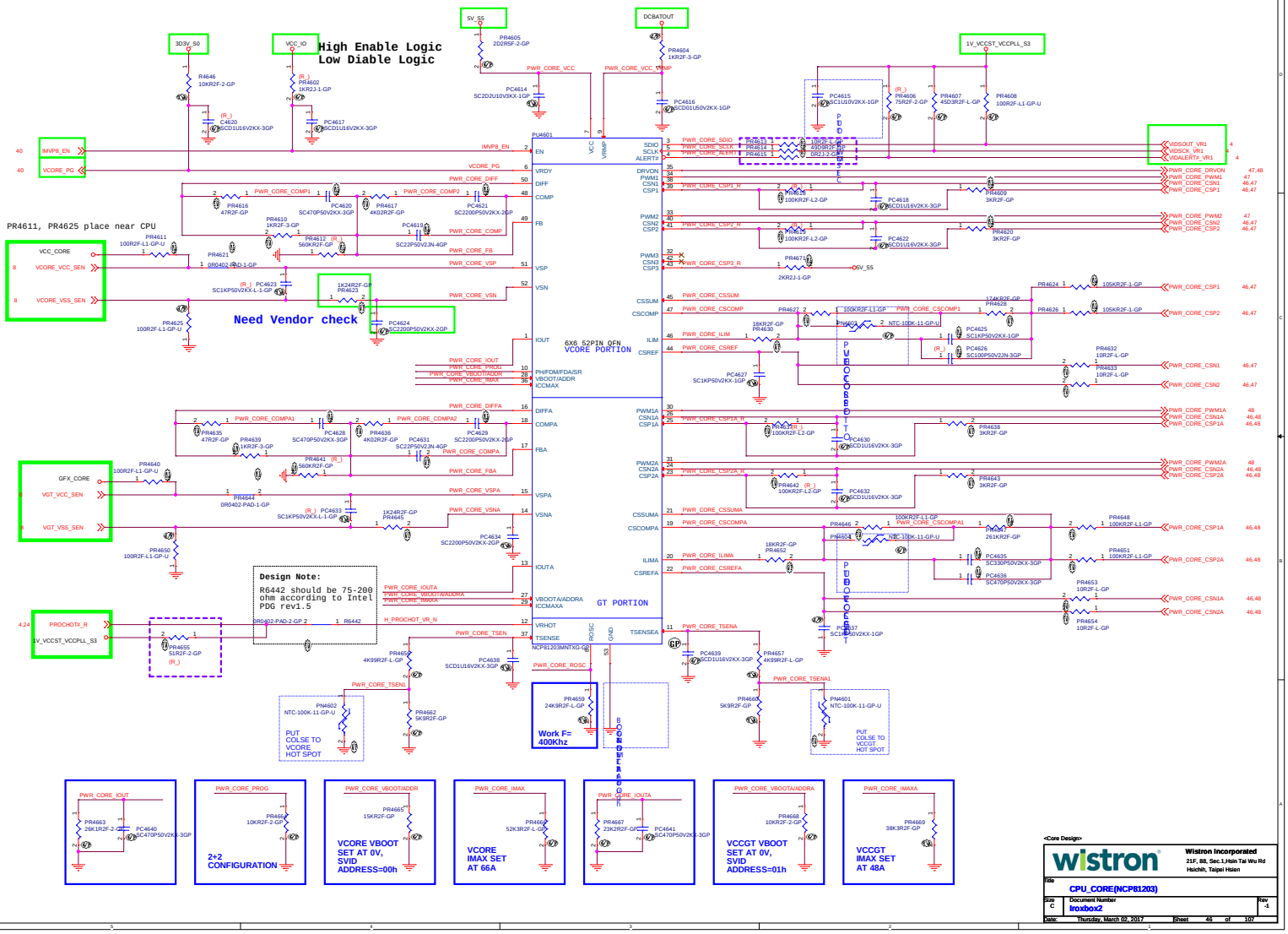
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: 5V/3D3V(RT6575D)

Size: A2 | Document Number: Inxdoc2 | Rev: A1

Date: Thursday, March 02, 2017 | Sheet 45 of 100

Intel SKYLAKE IMVP8 POWER 35W



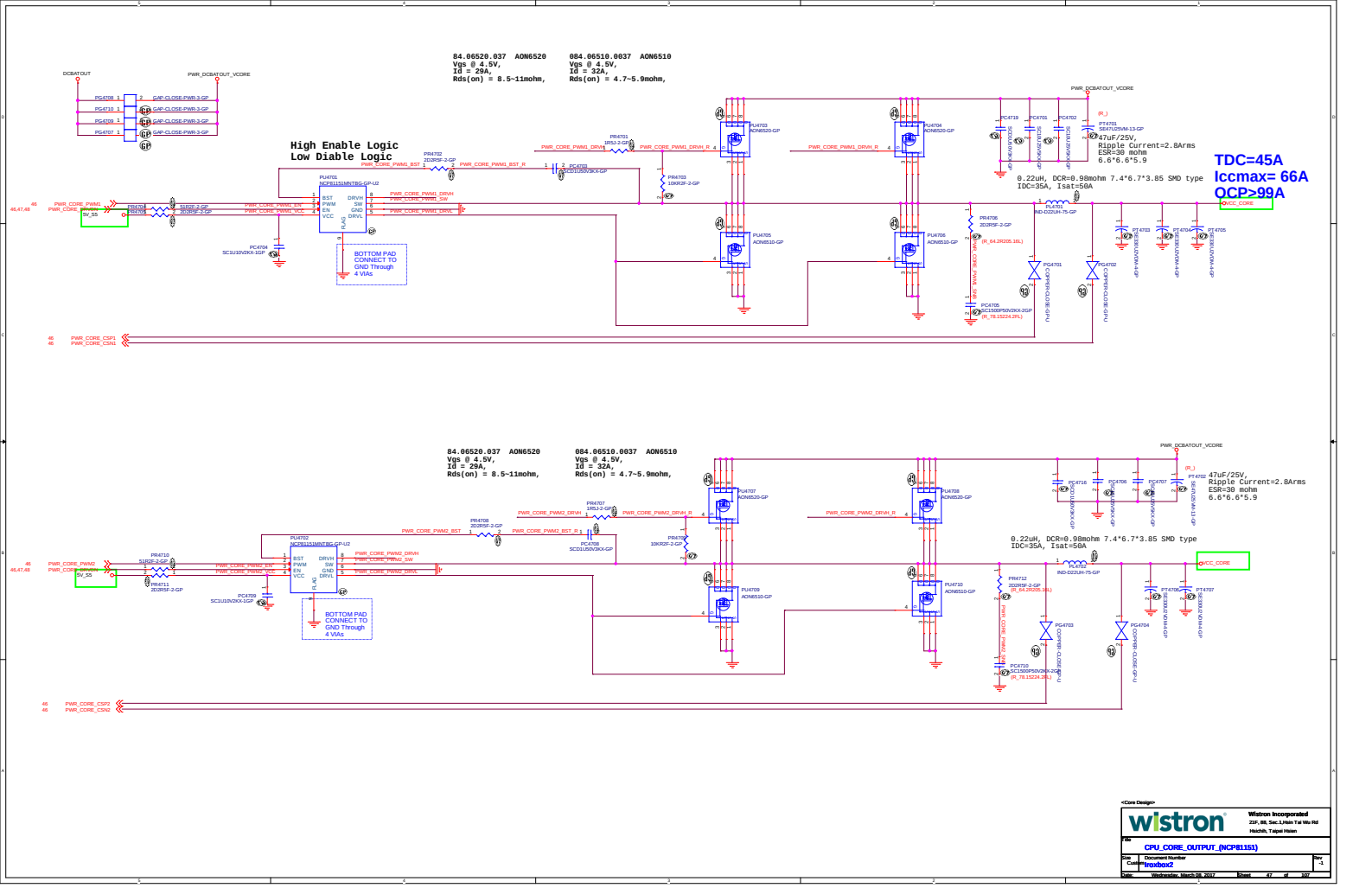
<Core Design>

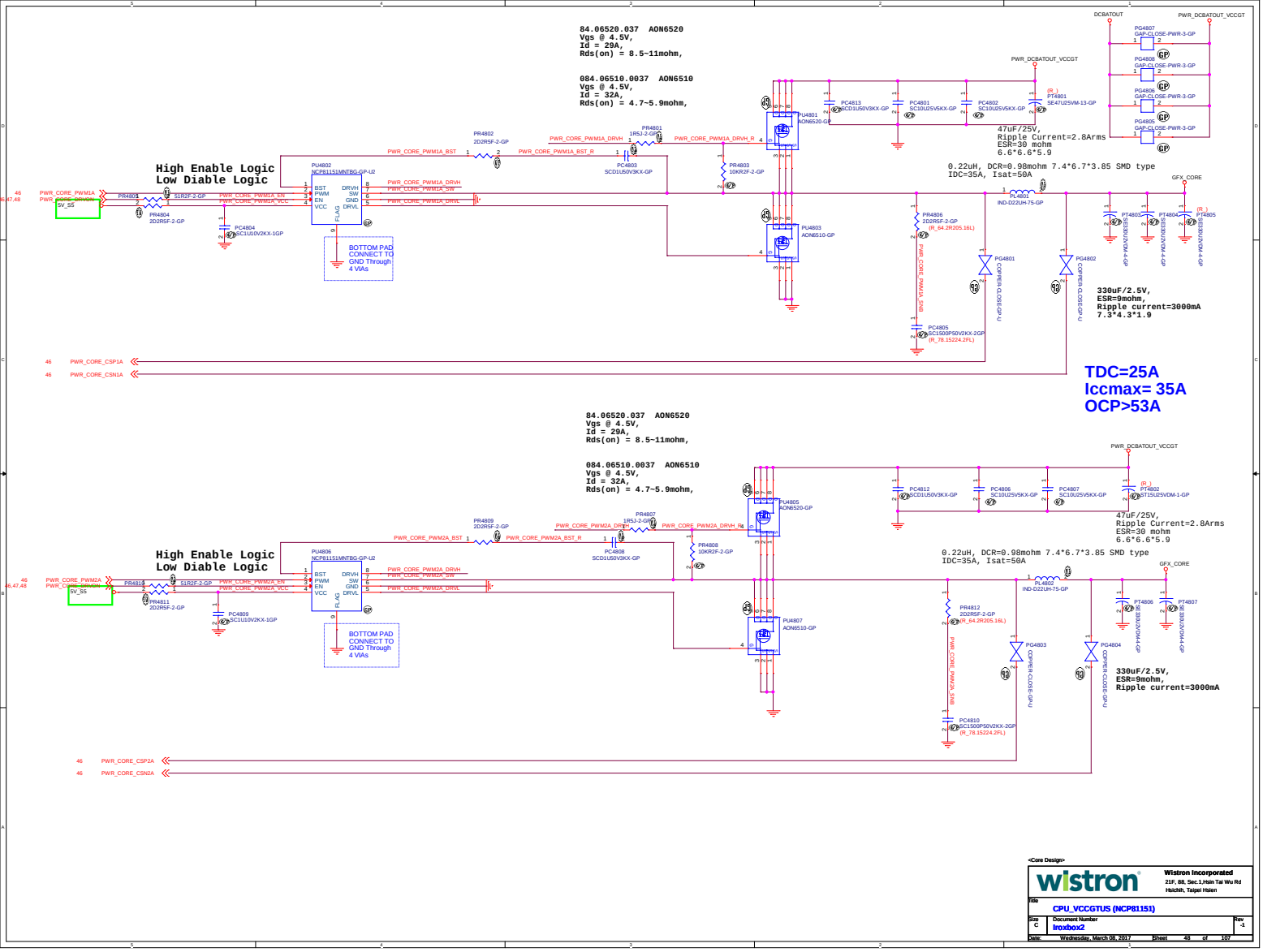
wistron Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_CORE(NCP81203)

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 46 of 107


84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,
084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,
High Enable Logic
Low Diable Logic
DCBATOUT
PWR_DCBATOUT_VCORE
PWR_CORE_PWM1
PWR_CORE_PWM1_DRVH
PWR_CORE_PWM1_DRVL
PWR_CORE_PWM1_SW
PWR_CORE_PWM1_BST
PWR_CORE_PWM1_VCC
PWR_CORE_PWM1_EN
PWR_CORE_CSP1
PWR_CORE_CSN1
BOTTOM PAD CONNECT TO GND Through 4 VIAs
47uF/25V,
Ripple Current=2.8Arms
ESR=30 mohm
6.6*6.6*5.9
0.22uH, DCR=0.98mohm 7.4*6.7*3.85 SMD type
IDC=35A, Isat=50A
TDC=45A
Iccmax= 66A
OCP>99A
VCC_CORE
PWR_CORE_PWM2
PWR_CORE_PWM2_DRVH
PWR_CORE_PWM2_DRVL
PWR_CORE_PWM2_SW
PWR_CORE_PWM2_BST
PWR_CORE_PWM2_VCC
PWR_CORE_PWM2_EN
PWR_CORE_CSP2
PWR_CORE_CSN2
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
CPU_CORE_OUTPUT_(NCP81151)
Wednesday, March 08, 2017



<Core Design>

wistron

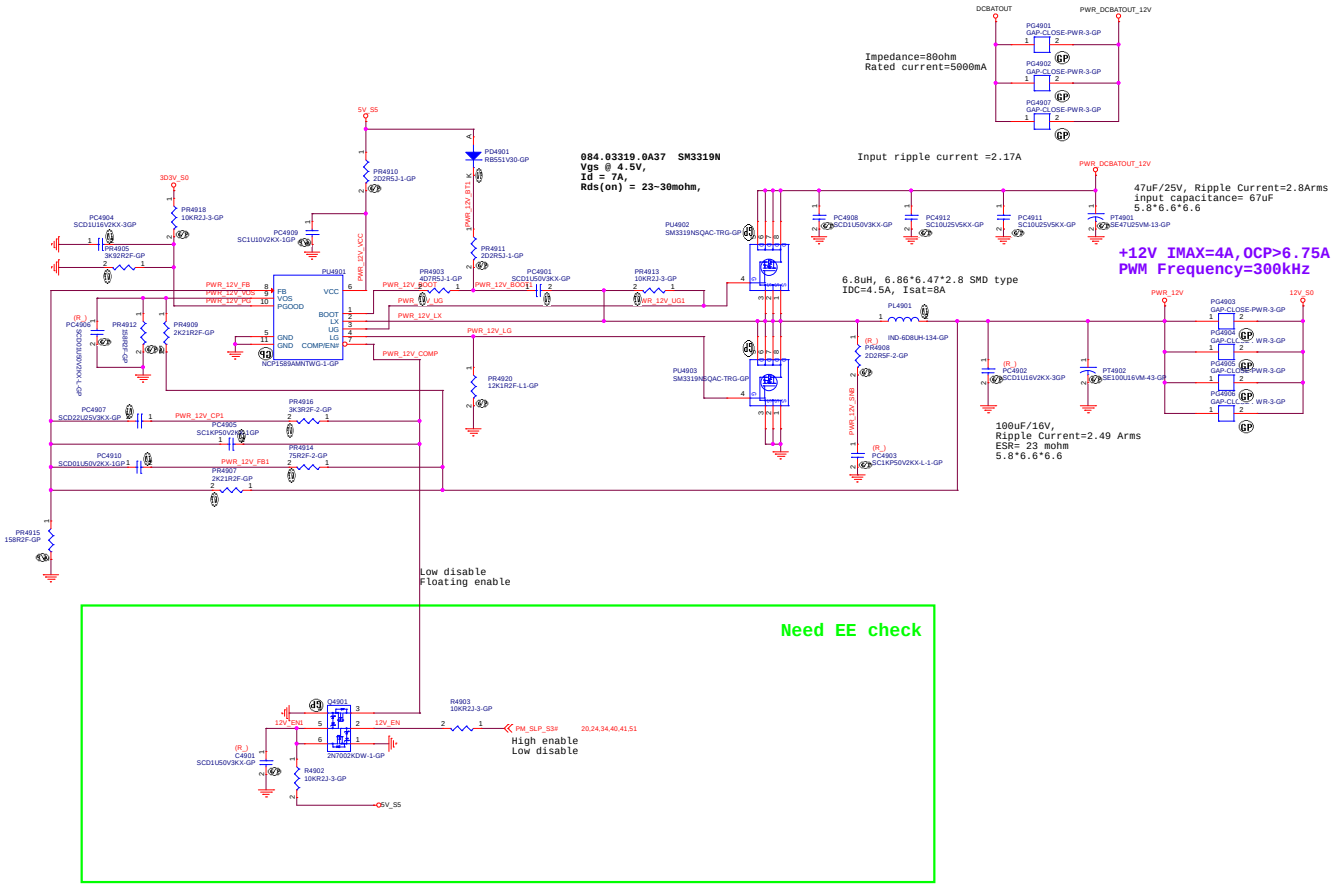
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_VCCGTUS (NCP81151)

Size: C | Document Number: Iroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 48 of 107

PWR_12V



<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title	DCDC_12V (NCP1589A)		
Size C	Document Number Inoxbox2		Rev -1
Date: Thursday, March 02, 2017		Sheet 49 of 107	

PWR_VCCSA

FOR EMI

PWR_DCBATOUT_VCCSA

PC5018 SCD1U50V3KX-GP

84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

Need EE to check

3D3V_S0

PR5022 10KR2J-3-GP

PU5001 RT8237CZQW-2-GP

VCCSA_PG

PWR_VCCSA_CS
PWR_VCCSA_SW
PWR_VCCSA_RF

PGOOD CS EN FB RF
GND BOOT UGATE PHASE VCC LGATE

PWR_VCCSA_BOOT
PWR_VCCSA_HG
PWR_VCCSA_SW
PWR_VCCSA_VCC
PWR_VCCSA_LG

PR5032 56KR2J-1-GP
PR5031 470KR2F-GP
PWM Frequency setting
OCP setting

PR5021 2D2R5J-1-GP
5V_S0

PR5006 2D2R5J-1-GP
PC5012 SCD1U25V2KX-GP
PWR_VCCSA_BOOT_A

PR5012 2D2R5J-1-GP
PWR_VCCSA_HG_A

PC5010 SC1U50V3KX-GP

PU5002 AON6520-GP
PU5003 AON6510-GP

PC5004 SC10U25V5KX-GP
PC5014 SC10U25V5KX-GP
PC5020 SC10U25V5KX-GP
(R_) PT5004 SE47U25VM-24-GP
47uF/25V, Ripple Current=2.8Arms
5.8*6.6*6.6

PWR_DCBATOUT_VCCSA
DCBATOUT
PG5001 GAP-CLOSE-PWR-3-GP
PG5002 GAP-CLOSE-PWR-3-GP

Iomax= 11A
OCP>17.25A

PL5001 IND-D47UH-35-GP-U
0.47uH,
DCR=4.0~4.2mohm,
Idc=17.5A, Isat=26A
6.86*6.47*3

PWR_VCCSA
VCC_SA

(R_) PR5014 1R5J-2-GP
PWR_VCCSA_SNB
(R_) PC5001 SC2200P50V2KX-2GP

(R_) PC5006 EC01U16V2KX-3GP
PT5001 SE560U2D5VM-14-GP
PT5002 SE560U2D5VM-14-GP
560uF/2.5V,
Ripple Current=3.5Arms
ESR= 16 mohm
5.7*6.6*6.6

8 VCCSA_SENSE
R6443
VCCSA_SENSE_1
8 VSS_VCCSA_SSENSE
0R0402-PAD-1-GP R6444
VSS_VCCSA_SENSE_1
0R0402-PAD-1-GP

VCCSA_SENSE_1
PR5026 10R2F-L-GP
R1
PR5027 16K2R2F-GP
PC5017 SC18P50V2JN-1-GP (R_)
PWR_VCCSA_FB
R2
PR5028 33KR2F-GP
VOUT=((R1+R2)/R2)*0.7
=0.7*(1+16.2/33)
=1.04V
VSS_VCCSA_SENSE_1
PR5025 10R2F-L-GP

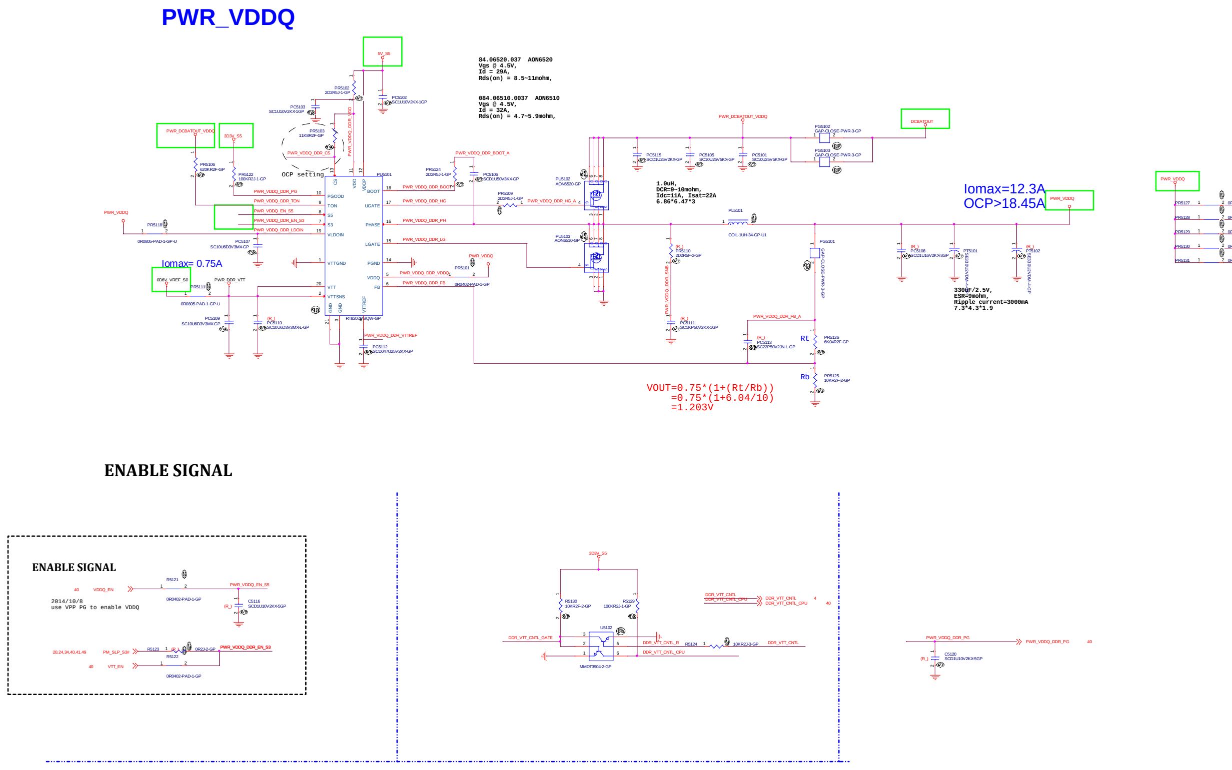
3D3V_S0
R5022 10KR2J-1-GP (R_)
40 VCCSA_EN
VCCSA_EN
R5003 10KR2J-3-GP (R_)
5V_S5
R5001 10KR2J-3-GP
EN_VCCSA_Q

3D3V_S0
R5004 10KR2J-3-GP
High :ENALBE VCCSA
Low :DISALBE VCCSA
PWR_VCCSA_EN
Q5001 2N7002DW-6-GP (75.27002.F7C)

<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1 Hsin Tai Wu Rd
Hsichih, Taipei Hsien

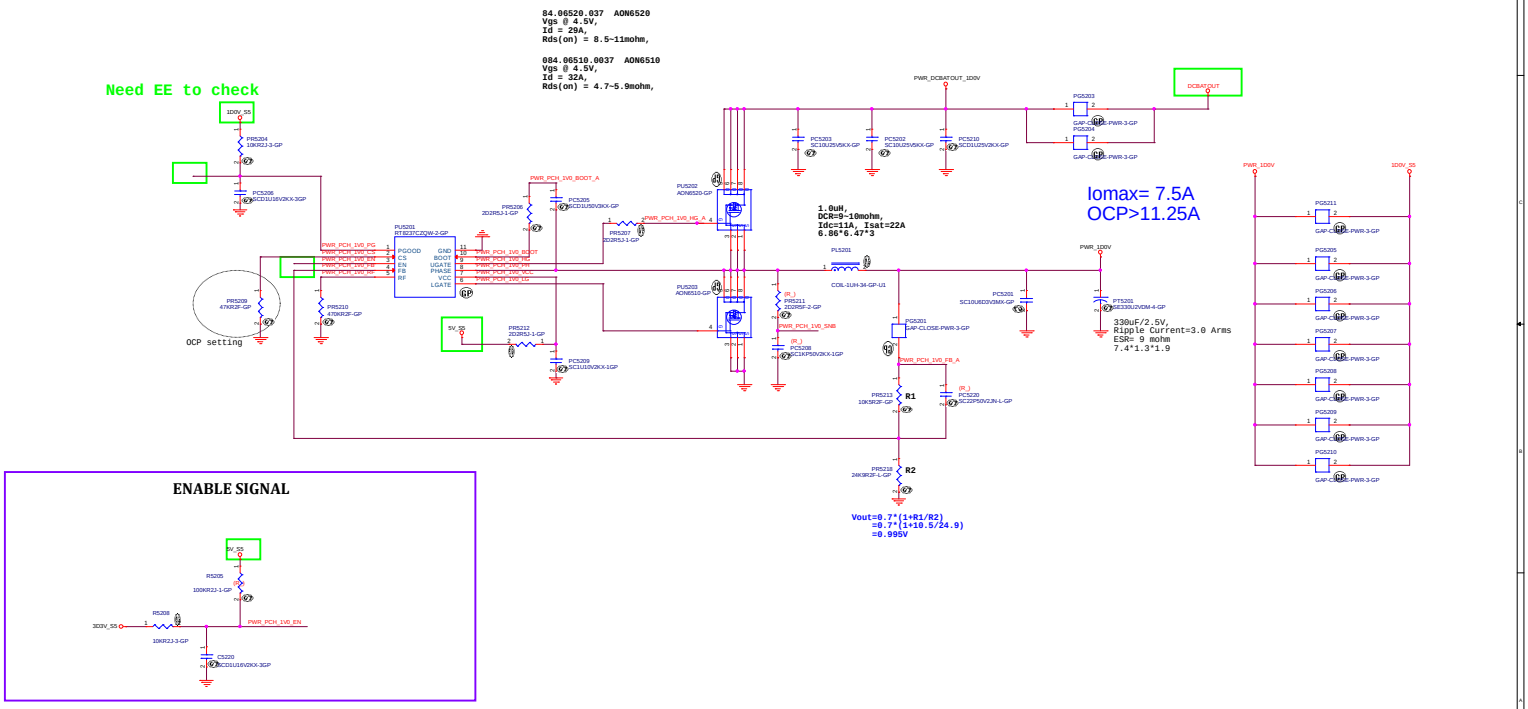
File: CPU_VCCSA (RT8237C)
Size: Custom | Document Number: Iroxbox2 | Rev: -1
Date: Thursday, March 02, 2017 | Sheet 50 of 107



<Core Design>

Wistron Incorporated	21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	MEM_MEMVTT (RT8207P)
Size: D	Document Number: Iroxbox2 — Rev: -1
Date: Thursday, March 02, 2017	Sheet 51 of 107

PWR_1D0V



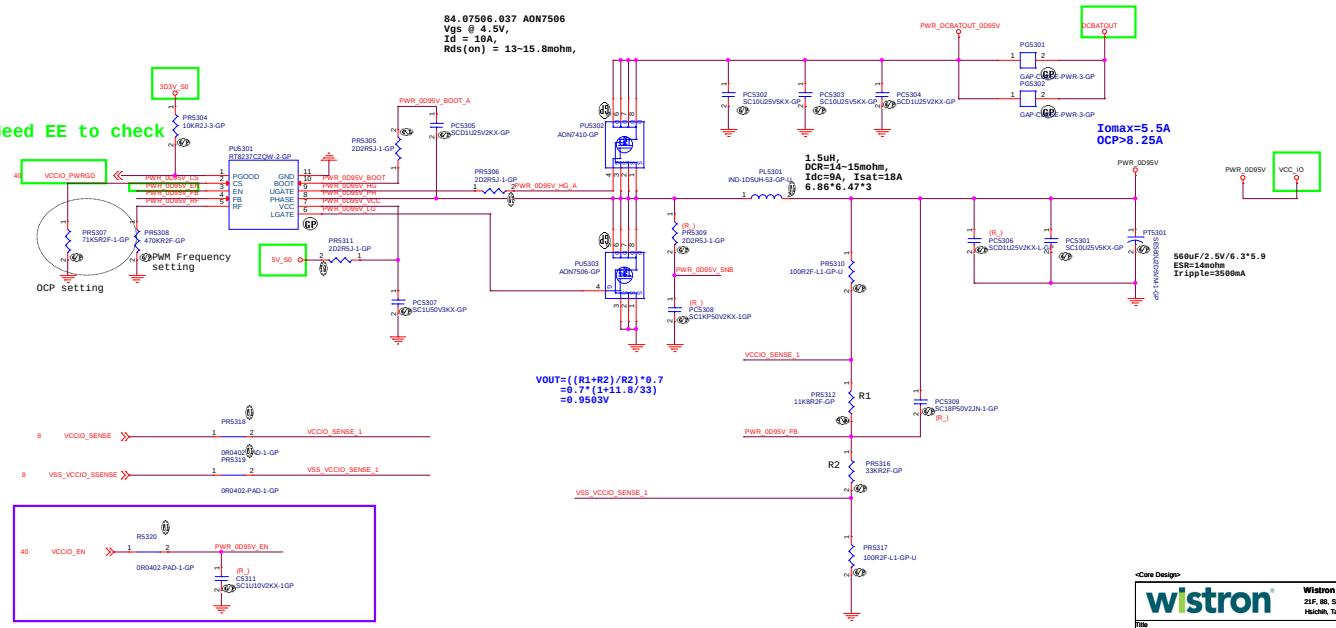
<Core Design>			
wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien		
File	PCH_1D0V (RT8237C)		
Size: Custom	Document Number: lnxsbox2		Rev: -1
Date: Thursday, March 02, 2006	Sheet: 52	of: 107	

PWR_VCCIO

84.07410.A37 SIS412DN
Vgs @ 4.5V,
Id = 7A,
Rds(on) = 24~29mohm,

84.07506.037 AON7506
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 13~15.8mohm,

Need EE to check



<Core Design>

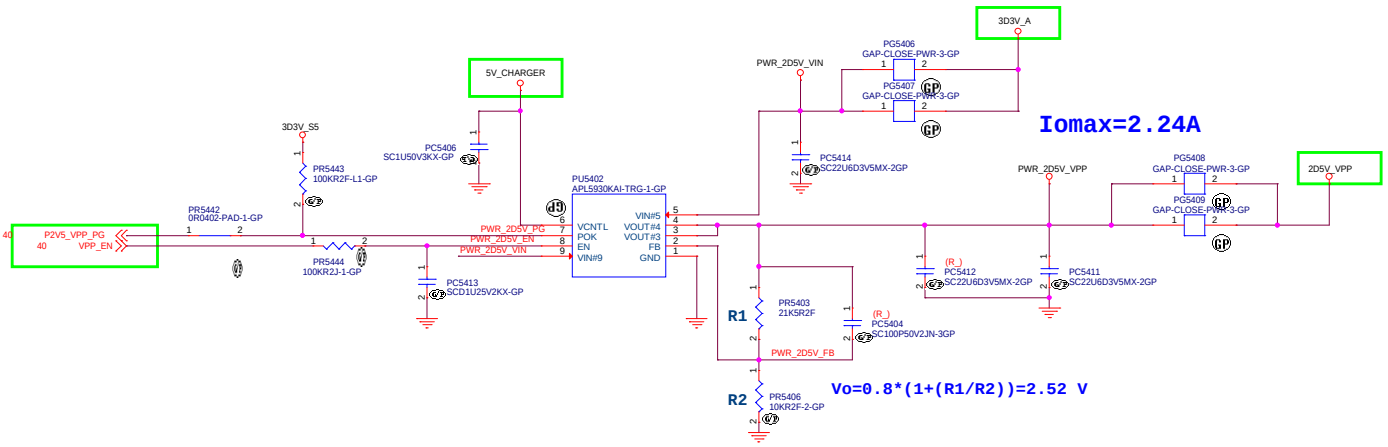
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCC_IO (RT8237C)

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Thursday, March 02, 2017 | Sheet 53 of 107

PWR_2D5V_VPP



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DCDC_2D5V (APL5930)

Size	Document Number	Rev
B	Iroxbox2	-1

Date: Thursday, March 09, 2017 Sheet 54 of 107

Reserved

Reserved

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI IN_(R)

Size: C | Document Number: Iroxbox2 | Rev: -1

Date: Friday, March 03, 2017 | Sheet 56 of 107

Reserved

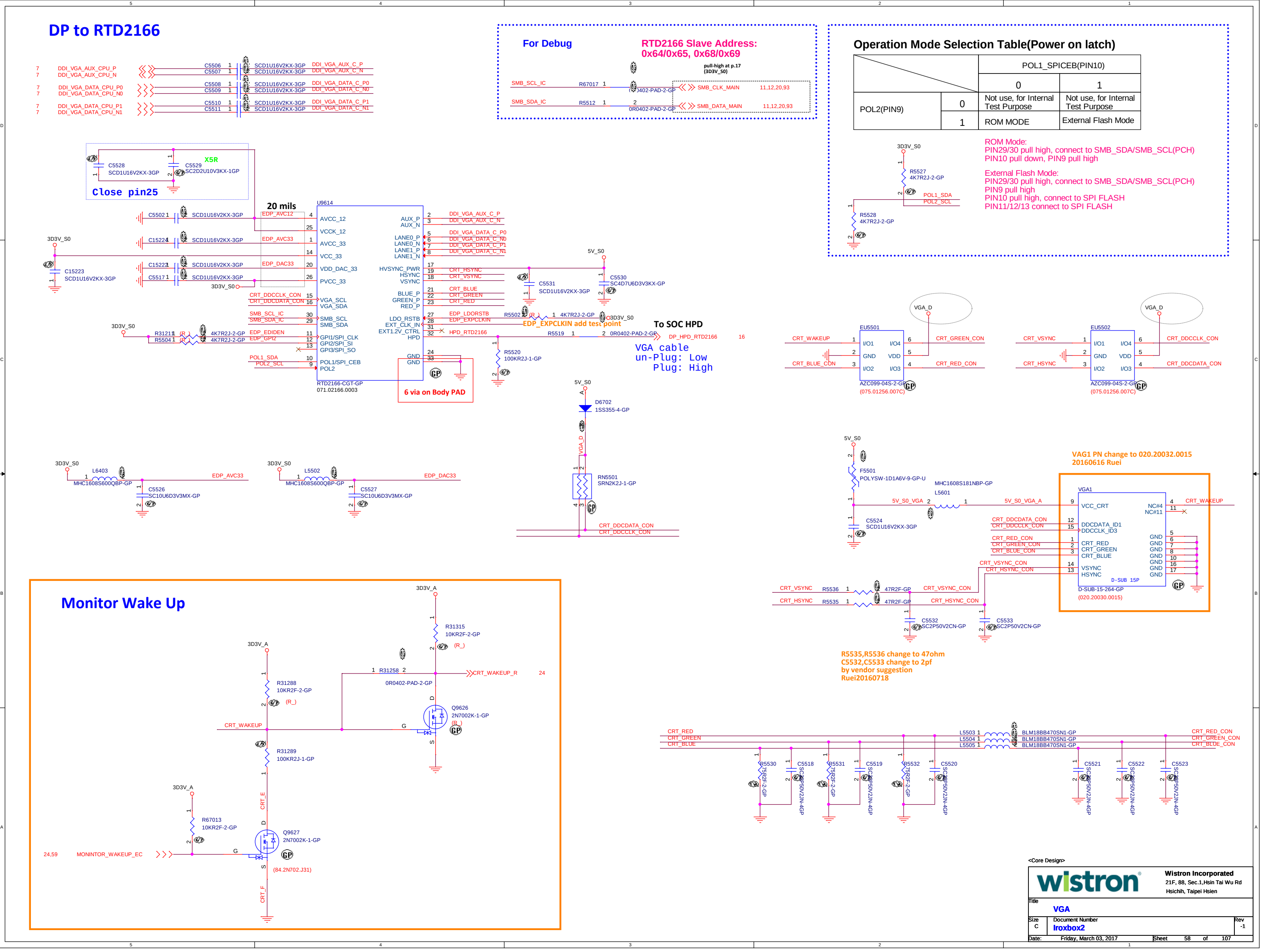
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI OUT_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Thursday, March 09, 2017 Sheet 57 of 107



		POL1_SPICEB(PIN10)	
		0	1
POL2(PIN9)	0	Not use, for Internal Test Purpose	Not use, for Internal Test Purpose
	1	ROM MODE	External Flash Mode

DP1

Place all CAP near DP Connector

DP connector

Impedance 85 ohm

Q3109 change to 84.02130.031 by F7 20160524 Ruel

DP1 PN change to 062.10006.0101 20160705 Ruel

2014/8/1 change DP2 to 22.10329.161

2015/01/21-SB Vita change FS604 symbol to 69.50007.D21

2015/01/07-SB Corree add FS604 for OC protection and use F7 as 69.41501.051

30mil 500mA (Max.)

Add Wakeup function by Pin16 Ruel 20160617

Monitor Wake Up

TR15,TR16,TR17,TR18 PN change to 66.R0036.04L by F7 Ruel 20161003

AUX

Q5706 symbolchange to 075.01C03.007C 20160620 Ruel

HPD

PLACE NEAR CONNECTOR PIN

2015/3/25-1A Vita add F7 (84.05067.031) which has Gate threshold voltage for Q5708

ESD

ED5704,ED5705, ED5706 Symbol change to 075.01043.0073 Ruel20160711

Display control line ESD Diodes

DP Cable(Option)

Place all CAP near DP Connector

DP connector (Option)

Impedance 85 ohm

Q9612 symbol change to 84.02130.031 Ruel 20160620

2015/01/07-SB Corree add FS604 for OC protection and use F7 as 69.41501.051

2015/01/21-SB Vita change FS604 symbol to 69.50007.D21

30mil 500mA (Max.)

2014/8/1 change DP2 to 22.10329.161

Add Wakeup function by Pin16 Ruel 20160617

2016/10/03-1A Ruel Change TR15 / TR16 / TR17 / TR18 F7 to 66.R0036.04L

AUX

Q9609 symbolchange to 075.01C03.007C 20160620 Ruel

HPD

PLACE NEAR CONNECTOR PIN

2015/3/25-1A Vita add F7 (84.05067.031) which has Gate threshold voltage for Q5708

ESD

ED5707,ED5708, ED5709 Symbol change to 075.01043.0073 Ruel20160711

Display control line ESD Diodes

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

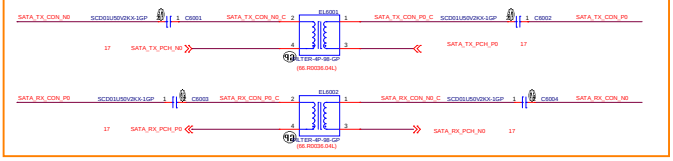
File: DP/HDMI

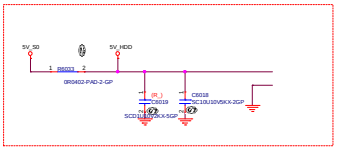
Size: Custom | Document Number: linuxbox2 | Rev: -1

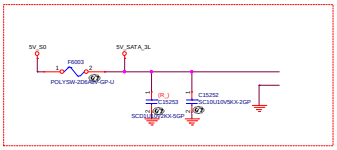
Date: Friday, March 09, 2007 | Sheet 59 of 107

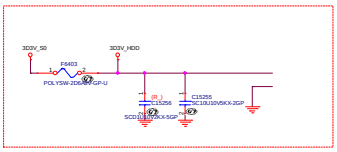
SATA Port 0

EL6001,EL6002 change to 68.24500.201 Ruei 20160614



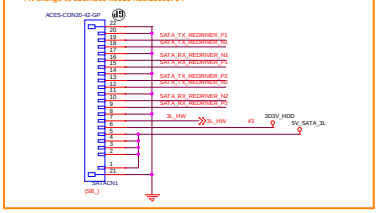


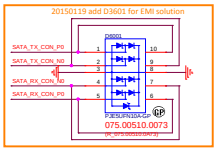




3L SATA Connector

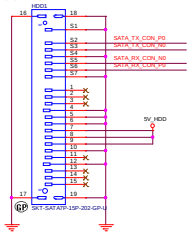
PN change to 020.K0164.0020 Ruei20160714



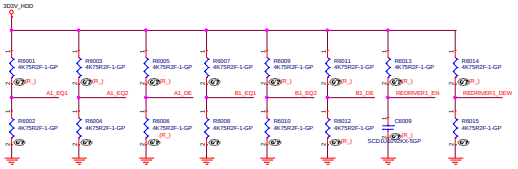


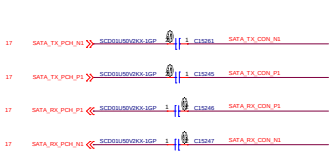
SATA HDD1 Connector

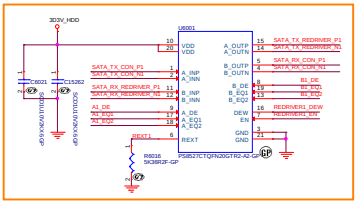
HDD1 symbol change to 020.F0928.0022
20161024 Ruei

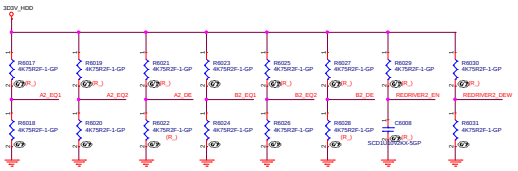


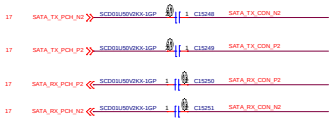
SATA Re-Driver

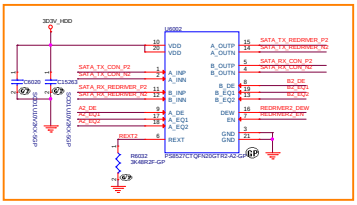












<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDD/ODD

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Friday, March 03, 2017 | Sheet 60 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Mini PCIE Card TV Tuner_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Friday, March 03, 2017 Sheet 61 of 107

M.2 2230 / 1630 Key E Type

USB

16 USB_PCH_PP7
16 USB_PCH_PN7

PCIEX1

16 PCIE_RX_PCH_N7
16 PCIE_RX_PCH_P7
16 PCIE_TX_WLAN_N7
16 PCIE_TX_WLAN_P7
18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#

OTHERS

24,62 PLT_WLAN_RST#
18 PEG_CLKREQ1_WLAN#
17 WLAN_RST_PCH
17 WLAN_DAT_PCH
17 WLAN_CLK_PCH
20 SMB_CLK_RESUME
20 SMB_DATA_RESUME
15 W1_DISABLE_N
15 W2_DISABLE_N
24,62 PLT_WLAN_RST#
20 PCH_SUSCLK_WLAN
20,63,93 PCIE_WAKE_N_PCIE

3D3V_S5

R6110 10KR2J-3-GP
R6105 10KR2J-3-GP

2014/10/1-Corree
Change to Key.E type

NGFFE1

R6116 0R2J-2-GP
R6114 0R2J-2-GP
R6115 0R2J-2-GP
R6109 0R0402-PAD-2-GP

SMB_CLK_RESUME
SMB_DATA_RESUME
W1_DISABLE_N
W2_DISABLE_N
PLT_WLAN_RST#
PCH_SUSCLK_WLAN
SMB_CLK_MINI
SMB_DATA_MINI
PLT_WLAN_RST_C

R31148 0R0402-PAD-2-GP WLAN_CLK_CON
R31150 0R0402-PAD-2-GP WLAN_DAT_CON
R31149 0R0402-PAD-2-GP WLAN_RST_CON

Controller Link interface is the Management communication link between the Skylake PCH and Intel Wireless cards

76	3_3VAUX	GND	77
74	3_3VAUX	RESERVED#73	75
72	RESERVED#70	RESERVED#71	73
70	RESERVED#68	GND	71
68	RESERVED#66	RESERVED#67/2ND_LANE_PERN1	69
66	GPIO0_NFC_RESET#/MGPIO7	RESERVED#65/2ND_LANE_PERP1	67
64	NFC_I2C_IRQ/MGPIO5	GND	65
62	NFC_I2C_SM_CLK	RESERVED#61/2ND_LANE_PETN1	63
60	NFC_I2C_SM_DATA	RESERVED#59/2ND_LANE_PETP1	61
58	W_DISABLE#1	GND	59
56	RESERVED#54/W_DISABLE#2	PEWAKE0#	57
54	PERST0#	CLKREQ0#	55
52	SUSCLK_32KHZ	GND	53
50	COEX1	REFCLKN0	51
48	COEX2	REFCLKP0	49
46	COEX3	GND	47
44	CLINK_CLK	PERN0	45
42	CLINK_DATA	PERP0	43
40	CLINK_RESET	GND	41
38	UART_CTS	PETN0	39
36	UART_RTS	PETP0	37
34	UART_TX	GND	35
32			33
22	UART_RX	SDIO_RESET	23
20	UART_WAKE	SDIO_WAKE	21
18	GND	SDIO_DAT3	19
16	LED#2	SDIO_DAT2	17
14	PCM_OUT	SDIO_DAT1	15
12	PCM_IN	SDIO_DAT0	13
10	PCM_SYNC	SDIO_CMD	11
8	PCM_CLK	SDIO_CLK	9
6	LED#1	GND	7
4	3_3VAUX	USB_D-	5
2	3_3VAUX	USB_D+	3
		GND	1
NP2	NP2	NP1	NP1

NGFF_KEY_E_75P

SKT-NGFF75P-91-GP

062.10003.0611

MINI_WAKE# R6106 0R0402-PAD-2-GP PCIE_WAKE_N_PCIE
MINI_CLKREQ#_WLAN_C R6107 0R0402-PAD-2-GP PEG_CLKREQ1_WLAN#

PEG_CLK1_WLAN#
PEG_CLK1_WLAN
PCIE_RX_PCH_N7
PCIE_RX_PCH_P7
PCIE_TX_WLAN_N7
PCIE_TX_WLAN_P7

2014/10/7
TX connect to TX, RX connect to RX due to symbol error
WLAN Module /KINGSTON,LITE-ON
Pin35 / Pin37 : PCIE_RXP / PCIE_RXN
Pin41 / Pin43: PCIE_TXP / PCIE_TXN

PLT_WLAN_RST#
C9422 (R) 4P5N1C050JSTG

3D3V_S5

USB_CON_PN7
USB_CON_PP7

2014/9/16-Vita
add EL3605 for NGFFE1 (follow Rosa Tigris)

2014/11/1-Corree
Change EL3605 to 66.R0036.04L for NGFFE1at SA
If SI concern , Change CMC PN to 068.01012.2011

M.2 SSD stand off PAD M.2 WLAN stand off

HS3
STF237R121H138-GP

Close to Pin2/4/72/74

3D3V_S5

C15184 SC10U6D3V5KX-1GE (78.10622.511)
C15183 SCD1U25V2KX-2-GP (78.10422.5FL)
C15181 SCD1U25V2KX-2-GP (78.10422.5FL)
C15182 SCD1U25V2KX-2-GP (78.10422.5FL)

2014/12/25-SB Vita
add F7 (78.10422.5FL) for C6110,C6112,C6113 -- MLCC unify

USB_CON_PP7 EL3605 USB_PCH_PP7
USB_CON_PN7 USB_PCH_PN7
MCM1012B900FBP-GP-U (66.R0036.04L)

U6201
USB_CON_PP7 I/O1 I/O4 USB_CON_PN7
GND VDD 3D3V_S5
I/O2 I/O3
AZC099-04S-2-GP (075.01256.007C)

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

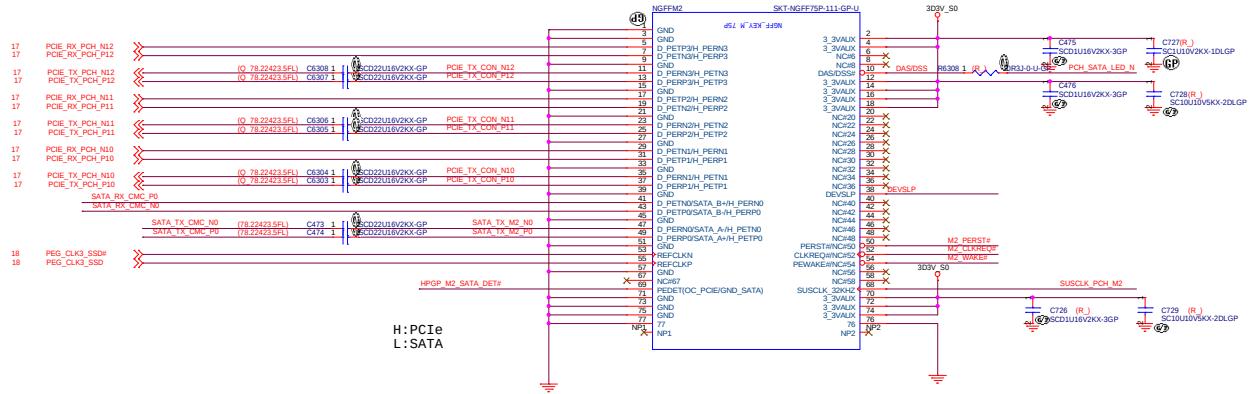
Title: WLAN and BT--NGFF

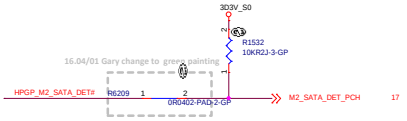
Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 62 of 107

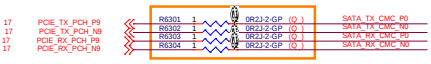
NGFF(M Key)

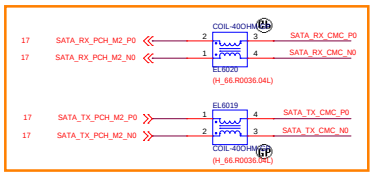
NGFFM2 PN change to 062.10003.0731
Ruei 201611230

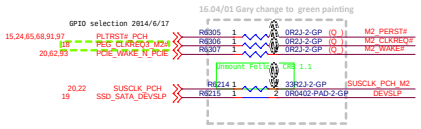




Close to CONN







<Core Design>

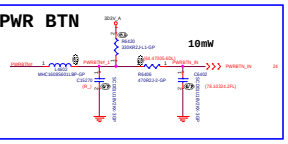
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: SSD-NGFF

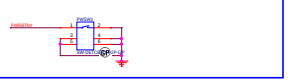
Size	Document Number	Rev
Custom	Inxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 63 of 107

PWR BTN



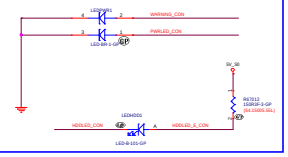
Power Button



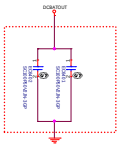
Power LAN LED

HDDLAN1 change to 83.19217.G70
Ruei 20160616

Power LED / HDD LED

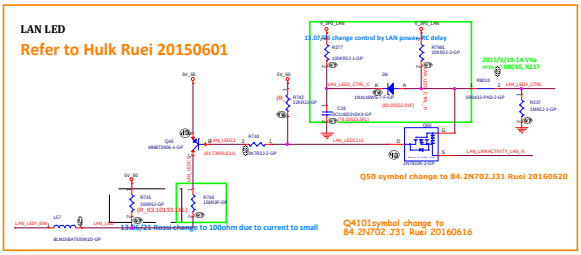


LEDPW1 PN change to 83.00195.M70
HDDLED1 PN change to 83.19217.G70
Ruei 20160616



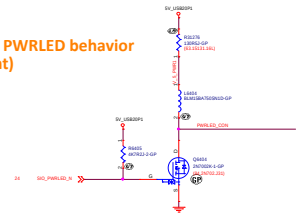
LAN LED

Refer to Hulk Ruei 20150601



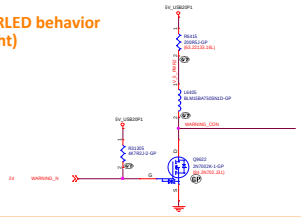
PWR LED

20160629 modify PWRLED behavior
S0: Blue(keep light)
S3: Blue(blink)

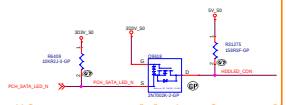


WARNING LED

20160629 modify PWRLED behavior
Normal: Blue(keep light)
Warning: Red(blink)



HDD LED



Modify HDDLED control logic,refer to Hulk
Ruei 20160628

TVS

Add ED3201 for HDDLED,PWRLED,LANLED
ESD protect Ruei 20160623

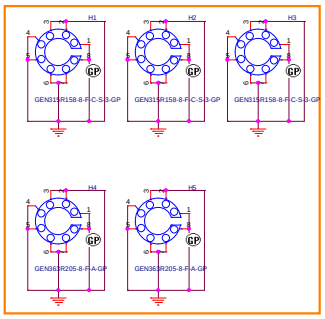
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

PWR BT/Side Key/LED

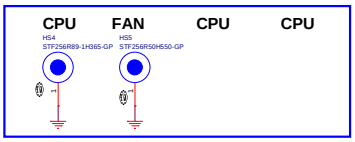
Size	Document Number	Rev
C	Irqxbox2	A

Date: Friday, March 10, 2017 Sheet 44 of 107

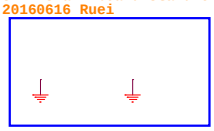
MB Screw hole



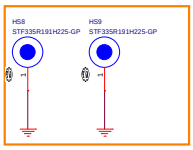
H4,H5 chagne to ZZ.SCREW.551
20160616 Ruei



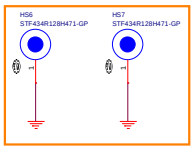
SATA Small board stand-off PAD
20160616 Ruei



SATA Small board stand-off

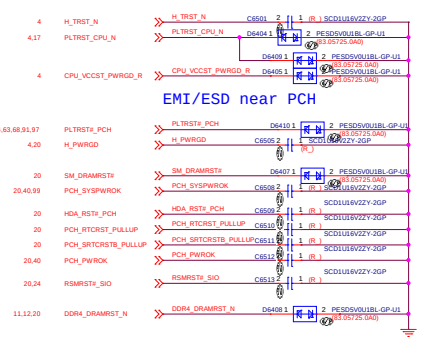


HDD cage stand-off

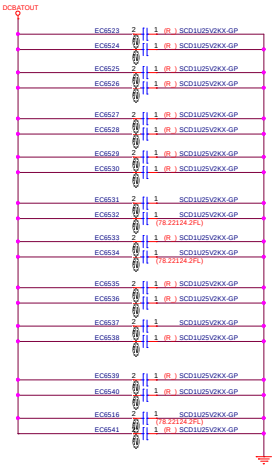


EMI CAP

EMI/ESD near CPU



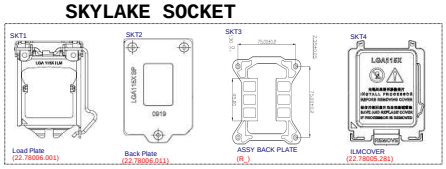
EMI/ESD near PCH



DUMMY BOM

Material part

SKYLAKE SOCKET



Battery Symbol

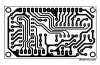
Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

Wire Length:60mm
耐高温>85C

Vendor
P/N:
23.21208.061
23.24220.612

Del PCHHS1 by Thermal--Ryan 0225

PCB Symbol



HeatSink Symbol

Vendor
P/N:
60.3MN01.011(second source)
60.3MN01.001

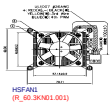
LABEL

MB serial NO# and MAC address
40.3BZ24.011 -> 30 x 15mm
40.3KP03.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
40.3BZ23.011 -> 30 x 10mm
40.3BZ24.011 -> 30 x 15mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
345.02801.0001 -> 12 x 6mm

Wire Length:30mm

Vendor
P/N:
23.21221.024
23.21212.031

HeatSink+FAN Symbol



Vendor
P/N:

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Stand off&EMI Cap&DUMMY BOM

Size	Document Number	Rev
C	lroxbox2	-1

Date: Friday, March 03, 2017 Sheet 65 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: IO Board_(R)

Size: C | Document Number: Iroxbox2 | Rev: -1

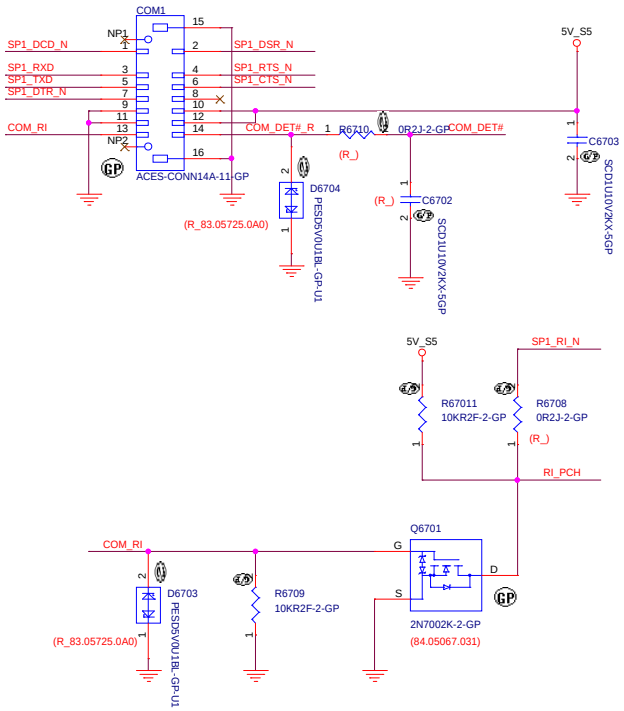
Date: Friday, March 03, 2017 | Sheet 66 of 107

SERIAL PORT

SPI

24 SP1_RTS_N
24 SP1_DTR_N
24 SP1_DSR_N
24 SP1_RXD
24 SP1_DCD_N
24 SP1_TXD
24 SP1_CTS_N
24 SP1_RI_N
15 COM_DET#
15 RI_PCH

20160802 Ruei
Delete U9609



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

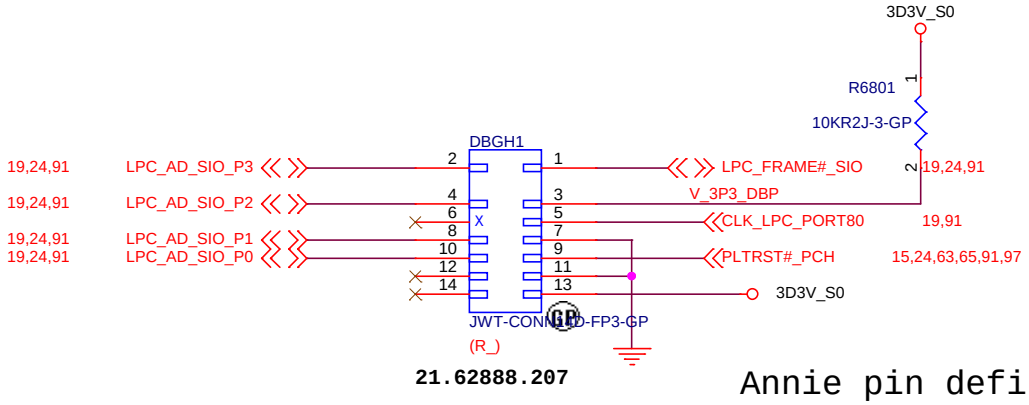
Title: COM PORT

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Friday, March 03, 2017 | Sheet 67 of 107

80 port

Layout close to SIO



21.62888.207

Annie pin define

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: **Debug**		
Size: Custom	Document Number: **Iroxbox2**	Rev: -1
Date: Wednesday, March 08, 2017	Sheet 68 of 107	

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LPT_(R)

Size: Custom | Document Number: 1roxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 69 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: G sensor_(R)

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 70 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 71 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 72 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 73 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 74 of 107

Reserved

<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	Thunderbolt_(R)
Size: C	Document Number: lroxbox2
Rev: -1	
Date: Wednesday, March 08, 2017	Sheet 75 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(1/5) PEG_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 76 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
GPU(2/5)DIGITALOUT_(R)

Size	Document Number	Rev
Custom	Iroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 77 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(3/5):VRAM I/F_(R)

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 78 of 107

Reserved

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

Title: GPU[5/6]-PWR/GND_[8]

Size: C | Document Number: Inx4box2 | Rev: A

Date: Wednesday, March 28, 2012 | Sheet 33 of 37

Reserved

<Cover Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

Title: VRAM 1.2 (1/4) (R)

Size: A3 | Document Number: insxbox2 | Rev: A

Date: Wednesday, March 28, 2007 | Sheet 31 of 37

Reserved

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

Title: VRAM 3.4 (16) (R)

Size: C | Document Number: inxbox2 | Rev: A

Date: Wednesday, March 06, 2002 | Sheet 22 of 37

Reserved

<Case Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

Title: VRAM 5.6 (24) (R)

Size: A3 | Document Number: inxbox2 | Rev: A

Date: Wednesday, March 06, 2013 | Sheet 33 of 37

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd.
Hsichih, Taipei Hsien

Title: VRAM 7.0 (DX) (R)

Size: D | Document Number: InnoBox2 | Rev: A

Date: Tuesday, March 26, 2013 | Sheet 55 of 57

Reserved

<Core Design>

wistron

Wistron Incorporated
21F., 88, Sec. 1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

PWR_GPU_CORE_PQ

Size: A | Document Number: Rev: 1A

Date: Wednesday, March 06, 2013 | Sheet 69 of 100

Reserved

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DISCRETE VGA POWER_(R)

Size: Custom | Document Number: Ironbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 88 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 87 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 88 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Others

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 89 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: NFC

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 90 of 107

15,24,63,65,68,97 PLTRST#_PCH

19,24 LPC_SERIRQ_PCH

19 SUS_STAT_N

19,24,68 LPC_AD_SIO_P0 — LPC_AD0

19,24,68 LPC_AD_SIO_P1 — LPC_AD1

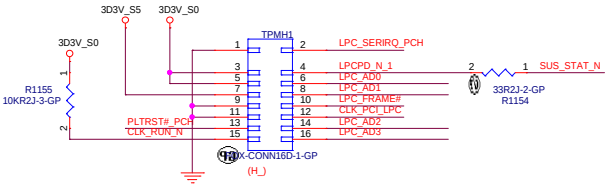
19,24,68 LPC_AD_SIO_P2 — LPC_AD2

19,24,68 LPC_AD_SIO_P3 — LPC_AD3

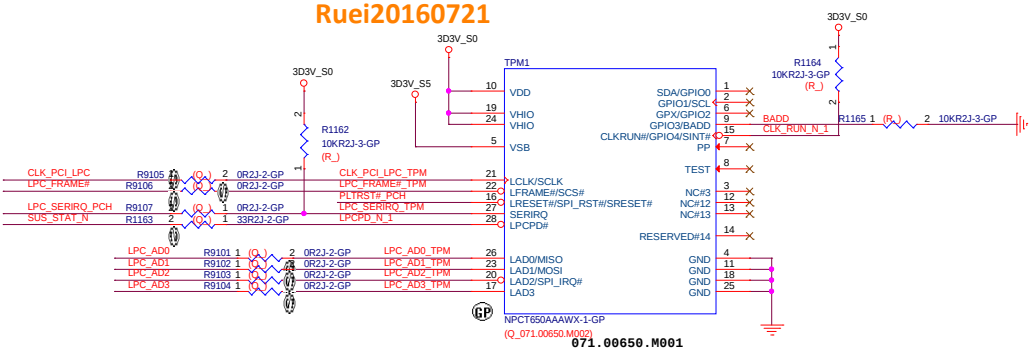
19,24,68 LPC_FRAME#_SIO — LPC_FRAME#

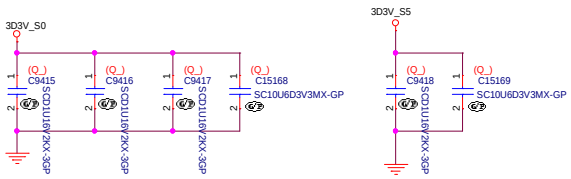
19,68 CLK_LPC_PORT80 — CLK_PCI_LPC

TPM Header (v MARR)
(refer to Superbox 2016019 Ruei)



TPM onboard chip for Q170
change TPM1 symbol to 071.00650.M001(TPM2.0)
Ruei20160721





<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: TPM

Size: Custom | Document Number: Iroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 91 of 107

Reserved

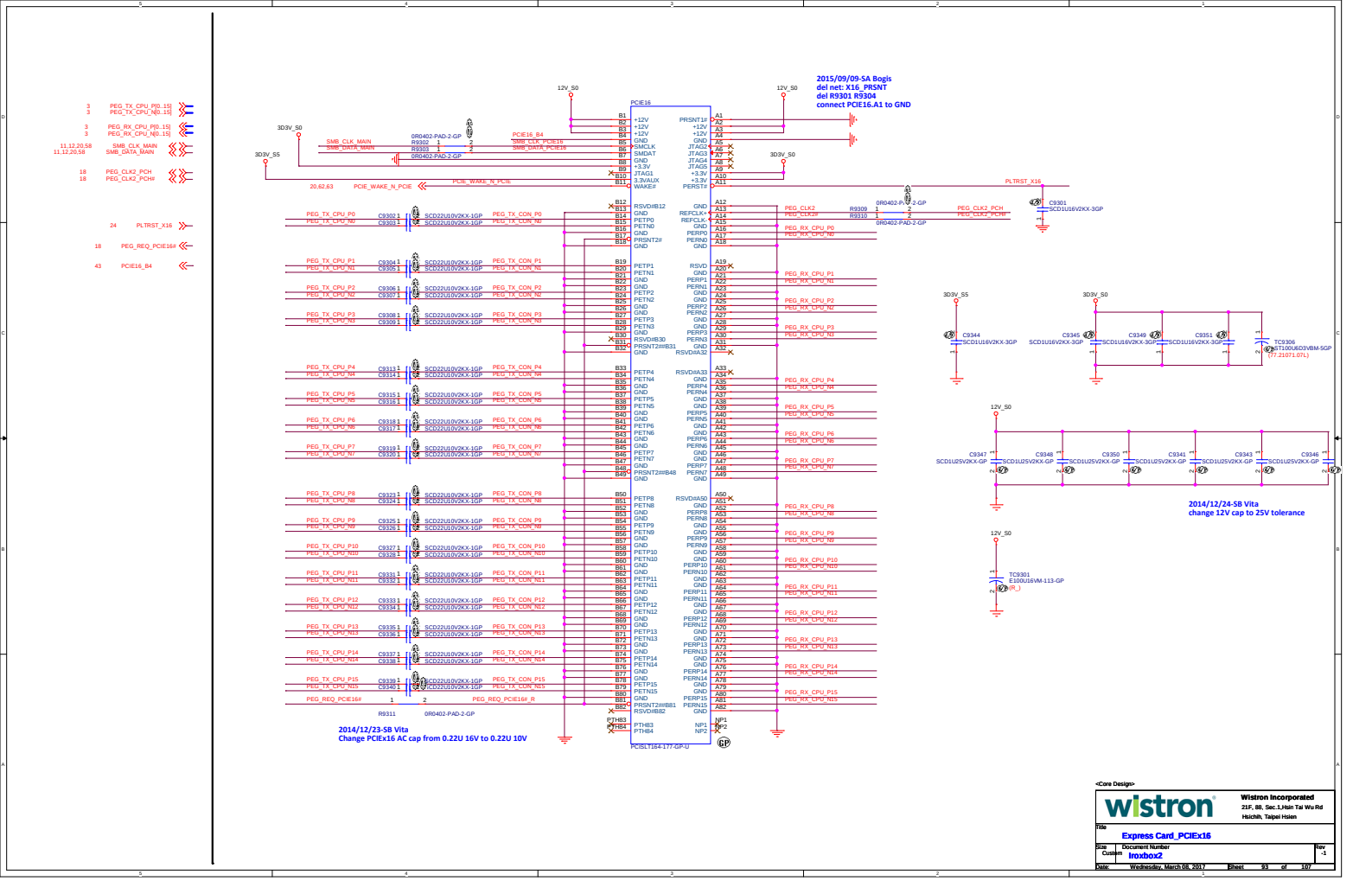
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PS2_(R)

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 92 of 107


2015/09/09-SA Bogis
del net: X16_PRSNT
del R9301 R9304
connect PCIE16.A1 to GND
2014/12/23-SB Vita
Change PCIEx16 AC cap from 0.22U 16V to 0.22U 10V
2014/12/24-SB Vita
change 12V cap to 25V tolerance
PCIE16
PCIBLT164-177-GP-U
Express Card_PCIEx16
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Inoxbox2
Wednesday, March 08, 2017

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Smart Card_(R)

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Thursday, March 09, 2017 | Sheet 84 of 107

Reserved

Reserved

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: Scalar Power_(R)

Size: Custom | Document Number: iroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 56 of 107

PCIE

18,31	PEG_CLK2_LAN	
18,31	PEG_CLK2_LAN#	
16,31	PCIE_TX_LAN_P5	
16,31	PCIE_TX_LAN_N5	
16,31	PCIE_RX_PCH_P5	
16,31	PCIE_RX_PCH_N5	

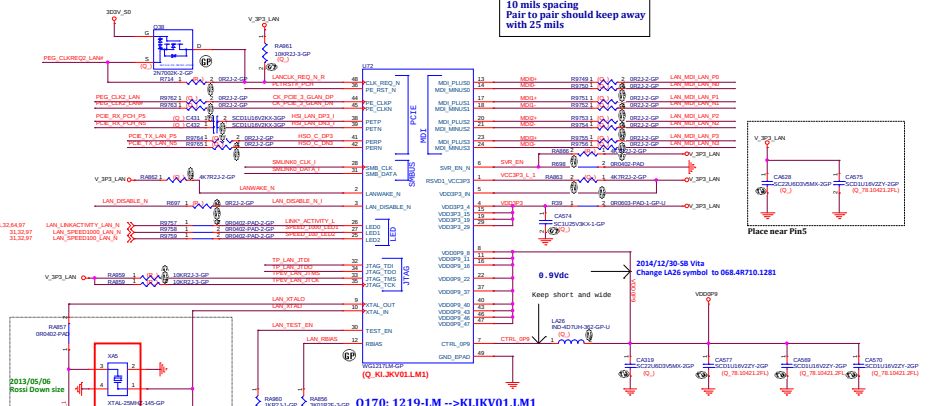
OTHERS

20	LAN_DISABLE_N	
20	SMLINK0_CLK	
20	SMLINK0_DATA	
12,24,63,65,66,91	PLTRST#_PCH	
24,31	LANWAKE_N	
18,31	PEG_CLKREQ2_LAN#	

31,32	LAN_MDI_LAN_P0	
31,32	LAN_MDI_LAN_N0	
31,32	LAN_MDI_LAN_P1	
31,32	LAN_MDI_LAN_N1	
31,32	LAN_MDI_LAN_P2	
31,32	LAN_MDI_LAN_N2	
31,32	LAN_MDI_LAN_P3	
31,32	LAN_MDI_LAN_N3	
31,32,97	LAN_SPEED1000_LAN_N	
31,32,97	LAN_SPEED100_LAN_N	
31,32,64,97	LAN_LINKACTMITY_LAN_N	
24	LAN_EN_PWR_SIO	

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,the CLK_REQ_N pull-up resistor should be connected to +V3.3S.

LAN_MDI_P / LAN_MDI_N routing guide line: 4 mils on 10 mils spacing
Pair to pair should keep away with 25 mils

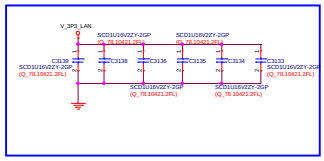


Place near Pin5

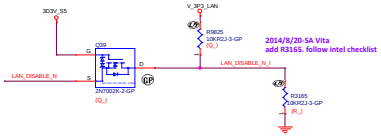
0.9Vdc POWER OPTIONS

Internal SRV	Shared with PCH's 1.05V SVR
LA36 : STUFF	LA36 : NO STUFF
RA1020 : NO STUFF	RA1020 : STUFF
R968 : STUFF	R968 : NO STUFF
RA886 : NO STUFF	RA886 : STUFF

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply (example sharing from PCH's 1.05V SVR). When sharing, make sure the 1.05V_SHARED is controlled by the SLP_LAN signal. Both +3.3V_LAN and 1.05V_SHARED rails are remained powered on during ALL Sx states, as required to support WOL.

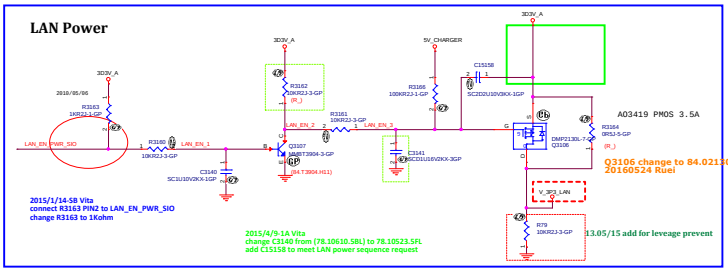


2015/3/19-1A Vita
add Q39, R9825 to control WOL under EUP



2014/8/20-SA Vita
add R316S. follow intel checklist

LAN Power



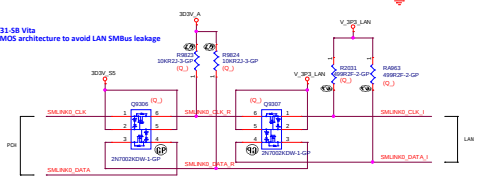
2015/1/14-SB Vita
connect R3163 PIN2 to LAN_EN_PWR_SIO
change R3163 to 1Kohm

2015/4/9-1A Vita
change C3140 from (78.10610.5BL) to 78.10523.5FL
add C15158 to meet LAN power sequence request

Q3106 change to 84.02130.031 by F7 20160524 Ruel

13.05/15 add for leveage prevent

2014/12/31-SB Vita
add dual MOS architecture to avoid LAN SMBus leakage



<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Inter LAN_WGI219LM
Size: Custom | Document Number: Inoxbox2 | Rev: -1
Date: Thursday, March 06, 2014 | Sheet 97 of 102

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LAN Switch_(R)

Size	Document Number	Rev
C	lroxbox2	-1

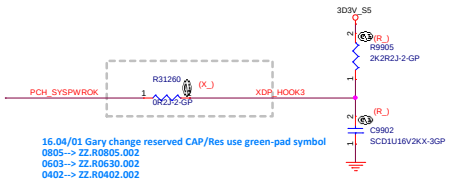
Date: Wednesday, March 08, 2017 Sheet 88 of 107

XDP for CPU

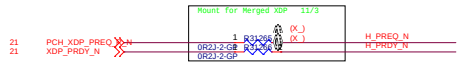
4 H_PREQ_N
4 H_PRDY_N

4,20 H_TDO
4,20 H_TDI
4,20 H_TMS

20,40,65 PCH_SYSPWROK



16.04/01 Gary change reserved CAP/Res use green-pad symbol
0805--> ZZ.R0805.002
0603--> ZZ.R0630.002
0402--> ZZ.R0402.002



PLACE ALL RA WITHIN 1.1INCH FROM CPU XDP
11/6 Javon

H_TDO → PCH_JTAG_TDO 4,20
H_TDI → PCH_JTAG_TDI 4,20
H_TMS → PCH_JTAG_TMS 4,20

<Core Design>

Wistron Incorporated
21F, 88, Sec.1.Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: XDP&ITP
Size: Custom | Document Number: Iroxbox2 | Rev: -1
Date: Wednesday, March 08, 2017 | Sheet 99 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Table of Content

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 100 of 107

Reserved

<Core Design>

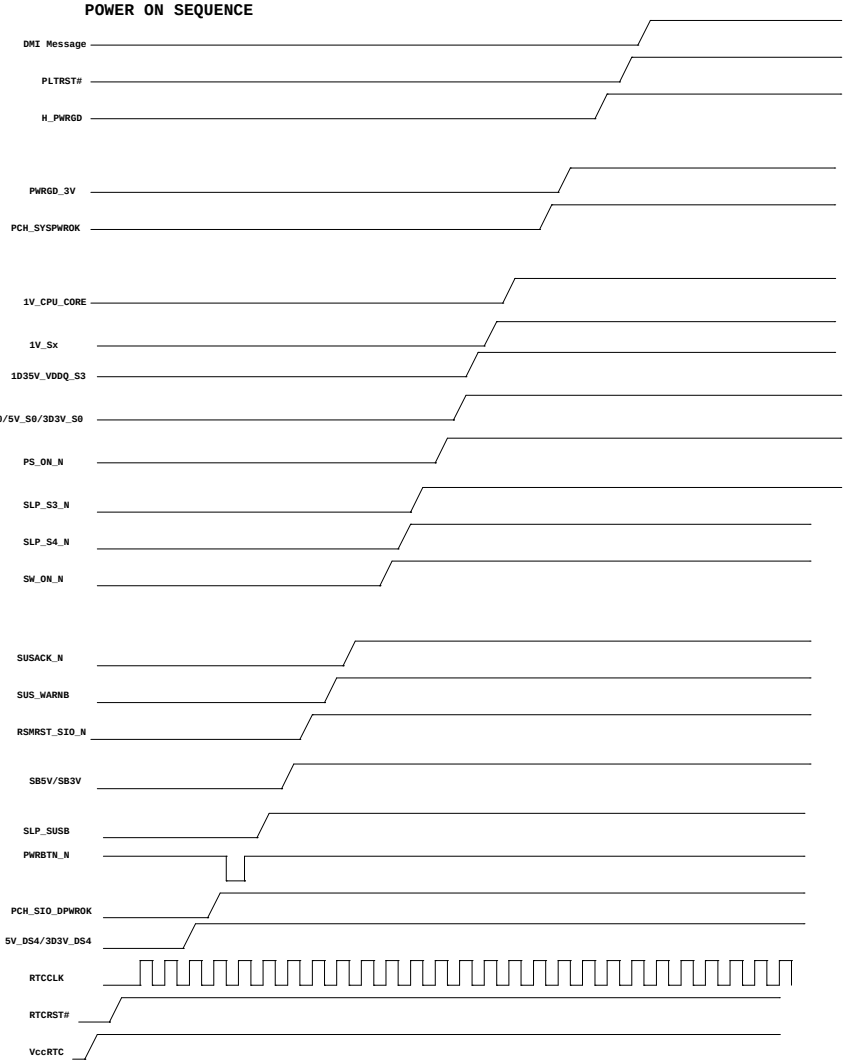
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPIO table

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 101 of 107

POWER ON SEQUENCE

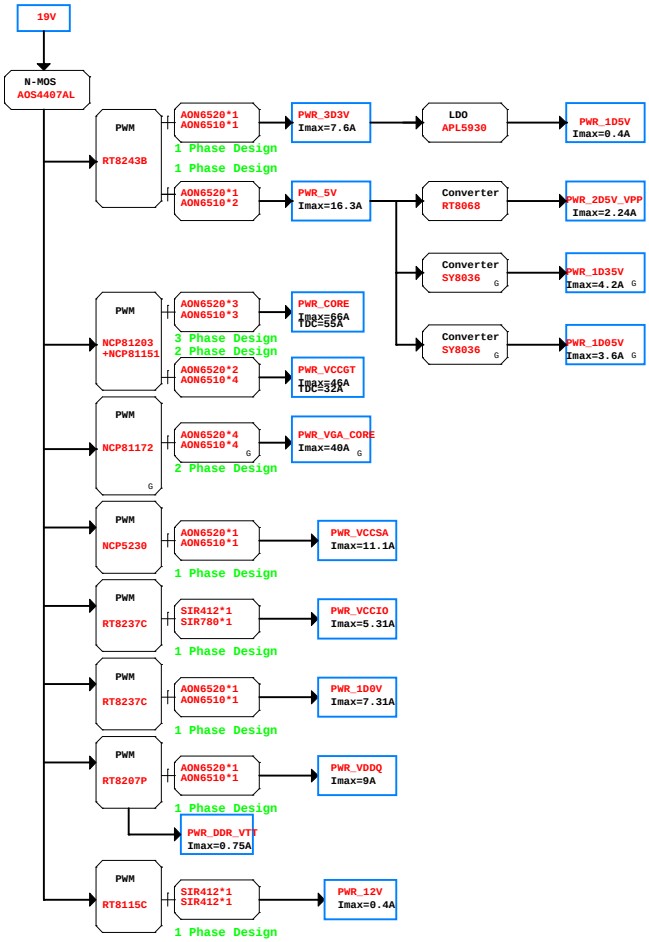


<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Power sequence

Size: C | Document Number: Imxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 100 of 102



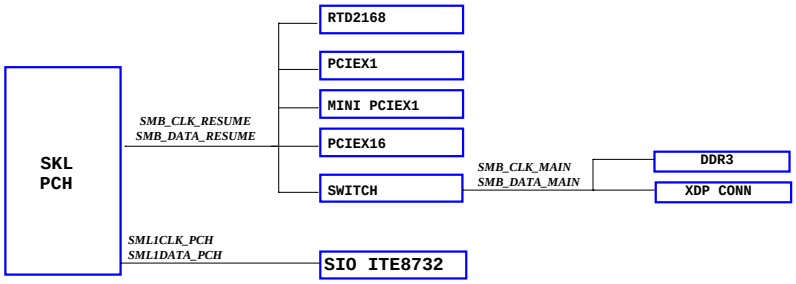
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: Power Block Diagram

Size: Custom | Document Number: inoxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 103 of 107



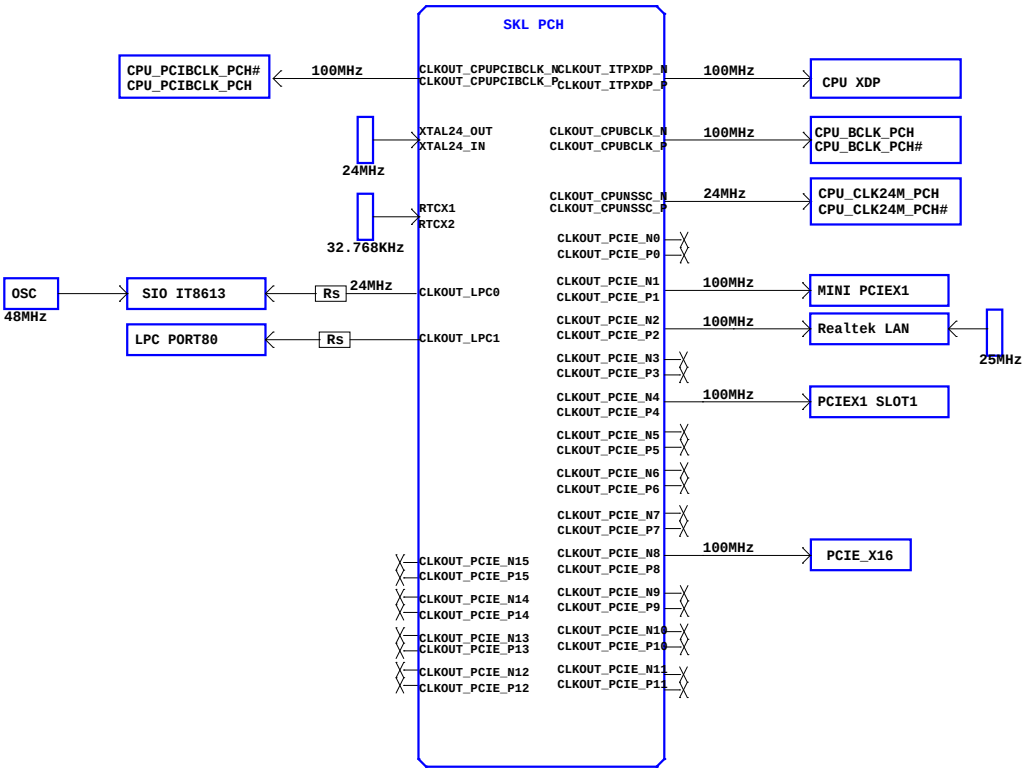
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: SMBUS Block Diagram

Size	Document Number	Rev
C	lroxbox2	-1

Date: Wednesday, March 08, 2017 Sheet 104 of 107



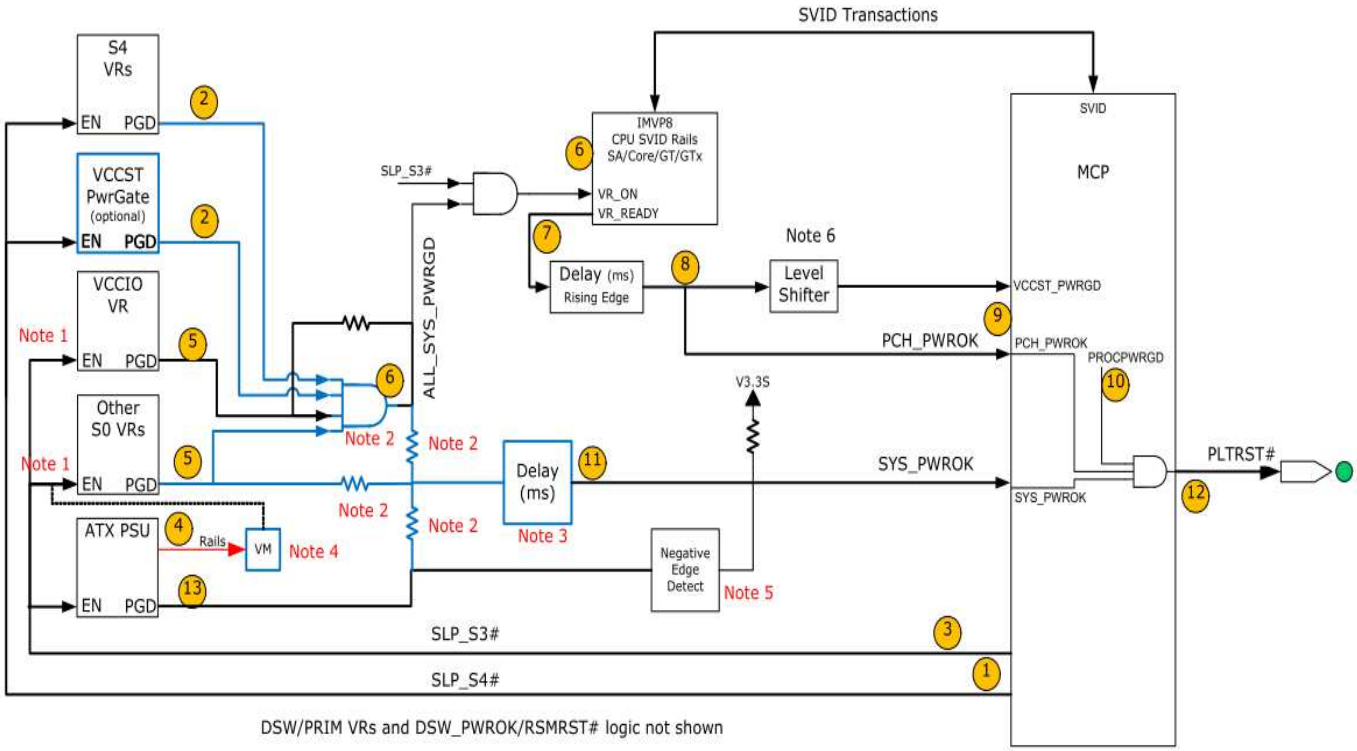
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Clock MAP

Size: C | Document Number: Iroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 105 of 107



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: RESET Flow Chart

Size: C | Document Number: Iroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 106 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Change History

Size: C | Document Number: lroxbox2 | Rev: -1

Date: Wednesday, March 08, 2017 | Sheet 107 of 107