Compal LA-K811P

GH47H MB Schematic Document

Rev : 1A

2021.01.14-B

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.		
Title: *Cover Sheet*		
Size	Document Number: *LA-K811P*	Rev: 1A
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HDMI - JHDMI1

- VGA Port C

P.39

HDMI Re-driver
- PS8419

VBIOS ROM

- SOP8
- Size : 2M

P.28

GN20E3 60W
- MAX-Q
- GDDR6 6G

P.25-37

eDP - JEDP1

- CPU eDP

P.38

DDI

PEG x 4
8GT/s

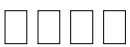
Intel Tiger Lake H35
Processor

Memory BUS

Interleaved (DDR4)

- DDR4 So-DIMM 260 pin
- Channel A

P.23



- DDR4 MD
- Channel B

P.24

USB3 - JUSB 2

- USB3 Port 2 (GEN2)
- USB2 Port 2

USB3 - JUSB 1

- USB3 Port 3 (GEN2)
- USB2 Port 3

USB3 Re-driver
- GL9901

USB3 Re-driver
- GL9901

Type C (TBT4) - JTYPEC1

- USB-C TCP0
- USB2 Port 2
- PD Ti 65992D

P.42-43

Tiger Lake PCH-LP
BGA 1499 (45.5 x 25)

SPI

SPI ROM 16M

- SOP8
- Size : 32M

P.16

LPC/eSPI BUS

P.06-22

TPM
- NPCT750

P.66

SSD - JSSD1 (PCIE/SATA)

- PCIE Port 9-12
- SATA @ Port 12

P.68

HD Audio

I2C

Touch Pad

- EC PS2
- PCH I2C3 P.63

EC KB9052

P.58

ESB/PS2

Fan Control*2
page 77

Extend IC
- ESB
- KC3810 P.59

WIFI - JNGFF1

- PCIE1.0 2.5GT/s
- PCIE Port 6

- USB2 Port 10

P.52

CCD Camera

- Port 8

P.38

Finger print
- USB2 Port 7

P.66

Tuch Screen
- USB2 Port 9
- PCH I2C5

P.38

HDA Codec
- ALC295

P.56

Int.KBD

- KSI/KSO
- 3 Zone RGB
(32pin + 12pin)

P.62&63

DMIC(Codec)

DMIC(PCH)

Int. Speaker

- ON M/B > L
- ON M/B > R

Audio Jack

- On M/B

Int. DMIC

- On CCD Module

Sub Board

TURBO/B (JTRB1) P.63

RTC CKT. (JRTC1) P.17

Power On/Off CKT. P.63

HW Circuit DC/DC P.78

Power Circuit DC/DC P.81-111

Security Classification	Compal Secret Data	
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Title: Block Diagrams

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Vcc	3.3V +/- 5%
Ra	100K +/- 1%

EC Board ID Table for AD channel

Board ID	Rb	Vmin	Vtyp	Vmax	EC AD	
0	0		0.000 V	0.300 V	0x00 – 0x13	SD028000080
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 – 0x1E	SD034120280
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F – 0x25	SD034150280
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 – 0x30	SD034200280
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 – 0x3A	SD034270280
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B – 0x45	SD034330280
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 – 0x54	SD034430280
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 – 0x64	SD034560280
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 – 0x76	SD034750280
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 – 0x87	SD034100380
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 – 0x96	SD034130380
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 – 0xA4	SD034160380
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 – 0xAF	SD034200380
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 – 0xB7	SD000001B80
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 – 0xBF	SD00000G280
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 – 0xC9	SD034330380
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA – 0xD4	SD00000WM80
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 – 0xDD	SD034560380
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE – 0xF0	SD00000AL80
19	NC		3.000 V		0xF1 – 0xFF	NC

*PCB Version
*Key board type

Board ID	PCB Revision	
0	EVT Rev 0.1	EVT@
1	EVT2 Rev 0.2	EVT2@
2	PVT Rev 1.0	PVT@ / MP@
3		
4		
5		
6		
7		
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9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		

STATE / SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
S0IX	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

Power Plane	Description	S0	S0ix	S3	S4/S5
+19V_ADPIN_P1	Adapter power supply	N/A	N/A	N/A	N/A
+20V_PDVIN	PD USB-C power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat tery power supply	N/A	N/A	N/A	N/A
+19VB	AC or bat tery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6V_VDDQ	LPDDR4x +0.6V power rail(VDDQ)	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OC	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.1V_VDDQ	LPDDR4x +1.1V power rail (VDD2)	ON	ON	ON	OFF
+1.8V	LPDDR4x +1.8V power rail(VDD1)	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
SOC_CK/DA (Port0)				
SOC_CK/DA (Port3)	TM-P3393-003 (Touch Pad)			
SOC_SMBCLK	DIMM1			
EC_CK/DA (Port0) (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_CK/DA (Port1) (+3VS) SOC_SML1CK/DA (+3VALW)	TGL-U / PCH LP	TBD		
	NV GN20E	0x9E		
	Thermal Sensor (NCT7718W)	0x98	1001_1001b	1001_1000b
	Thermal Sensor (G781)	0x9A	1001_1011b	1001_1010b
	Thermal Sensor (G753)	0x90		
EC_CK/DA (Port2)	LED Driver (59116F)	0xC0		
EC_CK/DA (Port3)	TI PD	0x40		
EC_CK/DA (Port4)	N/A (Set GPIO)			
EC_CK/DA (Port5)	KC3810	TBD		

PCB@ ZZZ
PCB
DAB0008F000

V : Must V : Options

Item (X43 / X76)	BOM Structure		Item (X43 / X76)	BOM Structure	
Unpop	@		dGPU circuit	VGA@	V
Connector	CONN@		OVEM	OVRM@	V
R Short	short@		OVRM GEN2	GEN2@	V
PCB	PCB@		OVRM-uPI	uPI_GEN2@	V
UMA (Reserved)	UMA@		OVRM-ON	ON_GEN2@	V
DIS (Reserved)	VGA@	V			
Intel design request	GLITCH@	V	Extend GPIO	KC3810@	V
PRIM Design	PREM@	V	Board ID	EVT@	V
SOC CMC	CMC@	V	Board ID	DVT@	V
SPI 1LD (WO TPM)	1LD@	V	Board ID	PVT@	V
SPI 2LD (W TPM)	2LD@	V	TPM	2LDTPM@	V
PCB	PCB@	V			
SDP	SDP@	V	TBT4	TypeC@	V
DDP	DDP@	V	TBT4 EMC	BL_EMC@	V
Memory Down	MEM@	V	TBT4 EMI	BL_EMI@	V
HYNIX 4G	X76DHYN4@	V	TBT4 ESD	BL_ESD@	V
HYNIX 8G	X76DHYN8@	V	Off-line charger	CHG@	V
HYNIX 16G	X76DHYN16@	V	Intel CNVi	CNVI@	V
MICRON 4G	X76DMIC4@	V	FOR UART debug	UART@	
MICRON 8G	X76DMIC8@	V	eDP-TS I2C	TS_I2C@	V
MICRON 16G	X76DMIC16@	V	eDP-TS USB	TS_USB@	V
SAMSUNG 4G	X76DSAM4@	V	Touch ad	TP@	V
SAMSUNG 8G	X76DSAM8@	V	Finger print	FP@	V
SAMSUNG 16G	X76DSAM16@	V	RGB Key board	3ZRGB@	V
WO Memory down	NODX76@	V	Thermal sensor	TMS@	V

43 Level	Description	BOM Structure
431AQ1BOL01		VGA@/GLITCH@/PREM@/CMC@/2LD@/2LDTPM@/MEM@/OVRM@/GEN2@/KC3810@/EVT@/TypeC@/CHG@/CNVI@/I2CTS@/TP@/FP@/3ZRGB@/TMS@/PCB@

Item (X4E)	BOM Structure	
EMI requirement	EMI@	V
EMI require reserve	XEMI@	
ESD requirement	ESD@	V
ESD require reserve	XESD@	
RF requirement	RF@	V
RF require reserve	XRF@	
FP EMI requirement	FPEMI@	V
FP ESD requirement	FPESD@	V
X4E	FOR MB EE	
X4E	FOR IO EE	

Item (X76)	BOM Structure	
OVRM-uPI	uPI_GEN2@	
OVRM-ON	ON_GEN2@	
VRAM-HYNIX	X76VHYN@	V
VRAM-MICRON	X76VMIC@	V
VRAM-SAMSUNG	X76VSAM@	V

X76 – UPI OVRM
X76 – ON OVRM

X76 – HYNIX
X76 – MICRON
X76 – SAMSUNG

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Title: Notes List

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Title: **Power MAP**

Size	Document Number	Rev
	LA-K811P	1A

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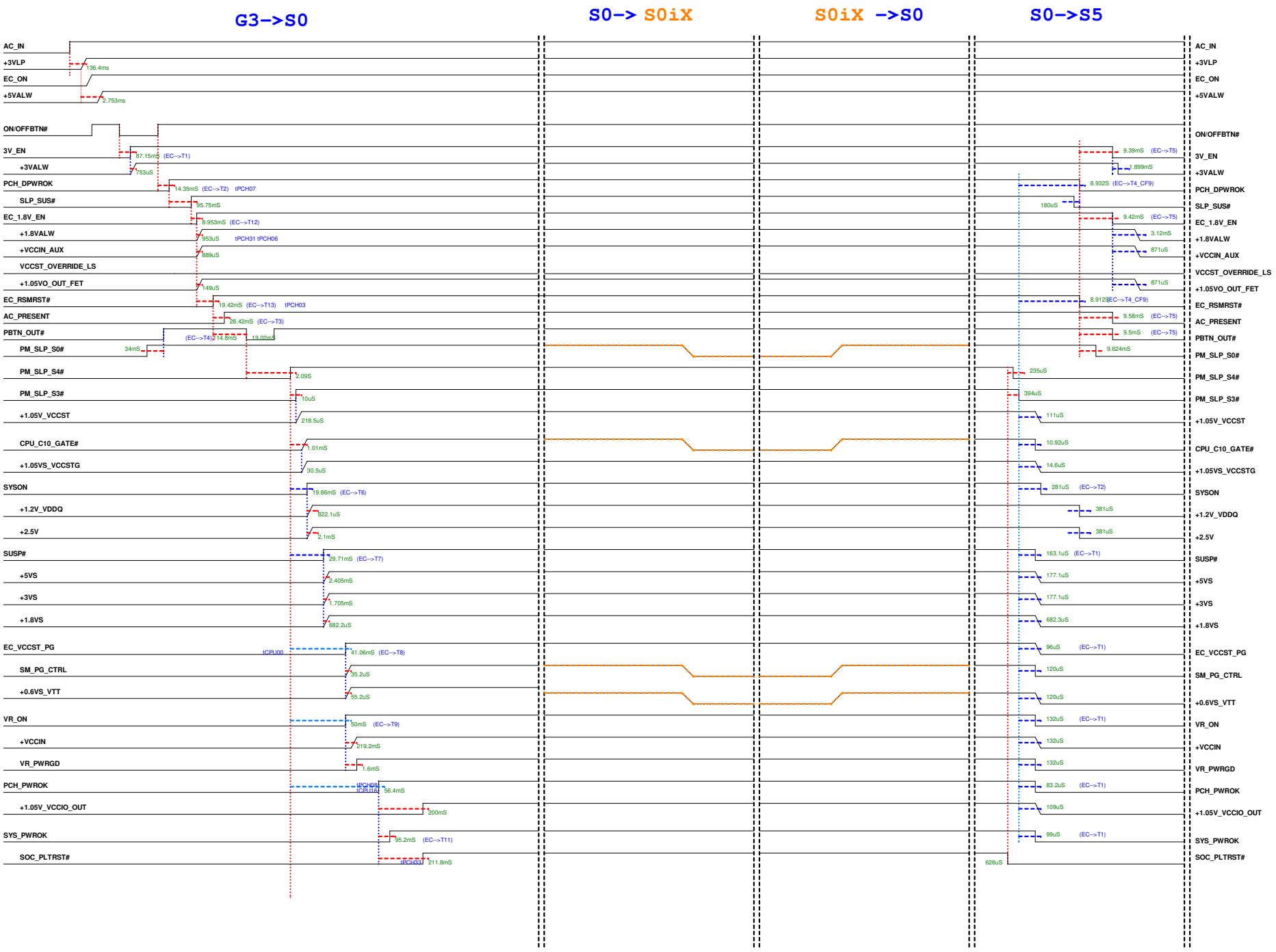
[GH47H - PWR Sequence_TGL-UP3_DDR4_S0iX]



Compal Electronics, Inc.		
Title: Power Sequence		
Size:	Document Number: LA-K811P	Rev: 1A
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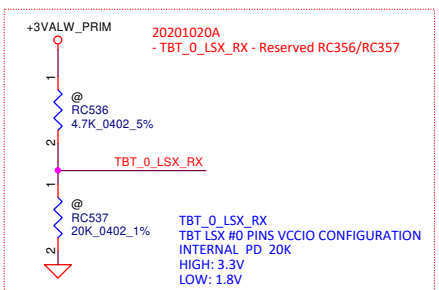

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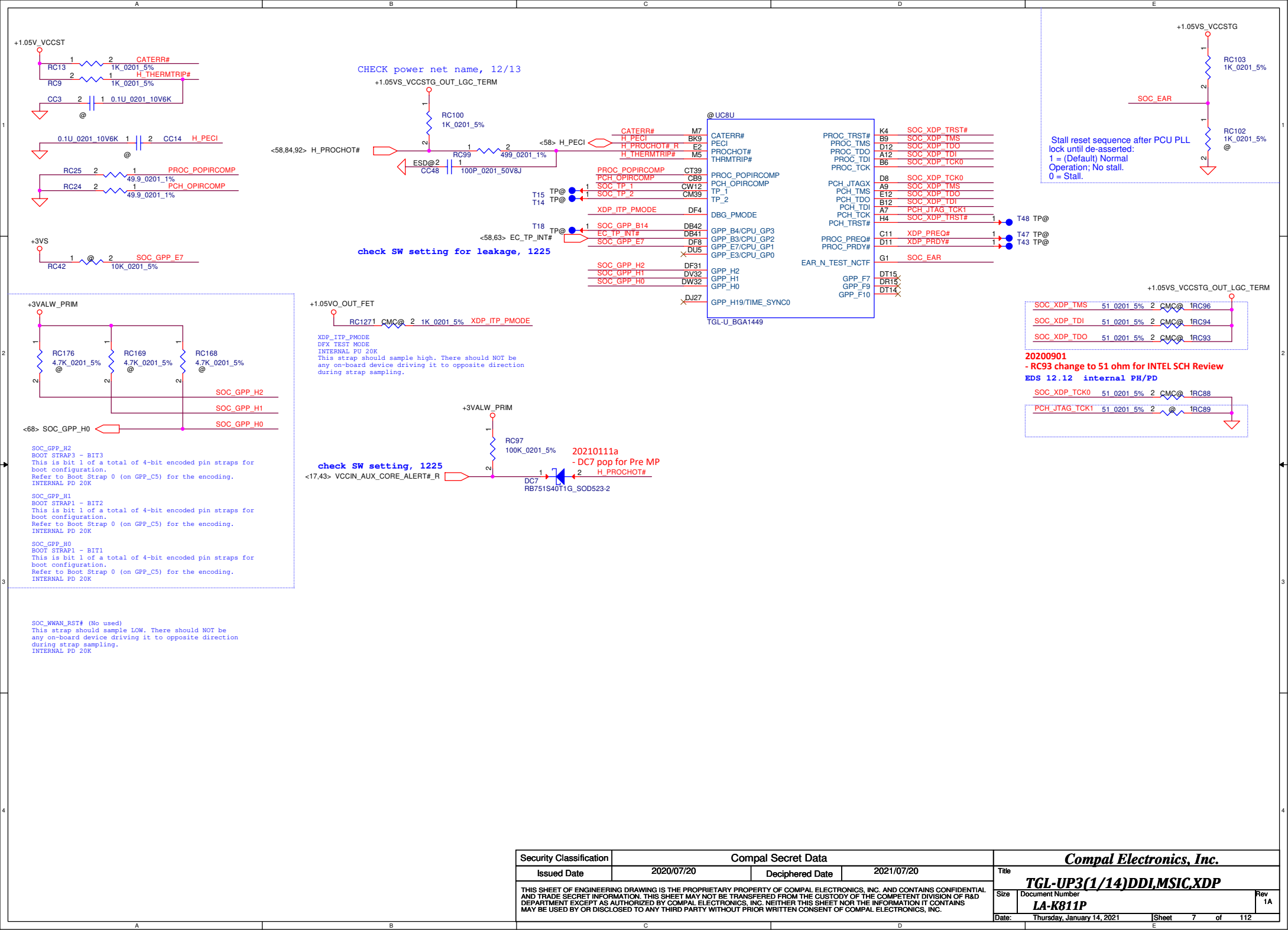
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title: TGL-UP3(1/14)DDI,EDP			
Size	Document Number: LA-K811P		Rev: 1A
Date: Thursday, January 14, 2021	Sheet 6 of 112		



Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title: TGL-UP3(1/14)DDI,MSIC,XDP			
Size	Document Number: LA-K811P		Rev: 1A
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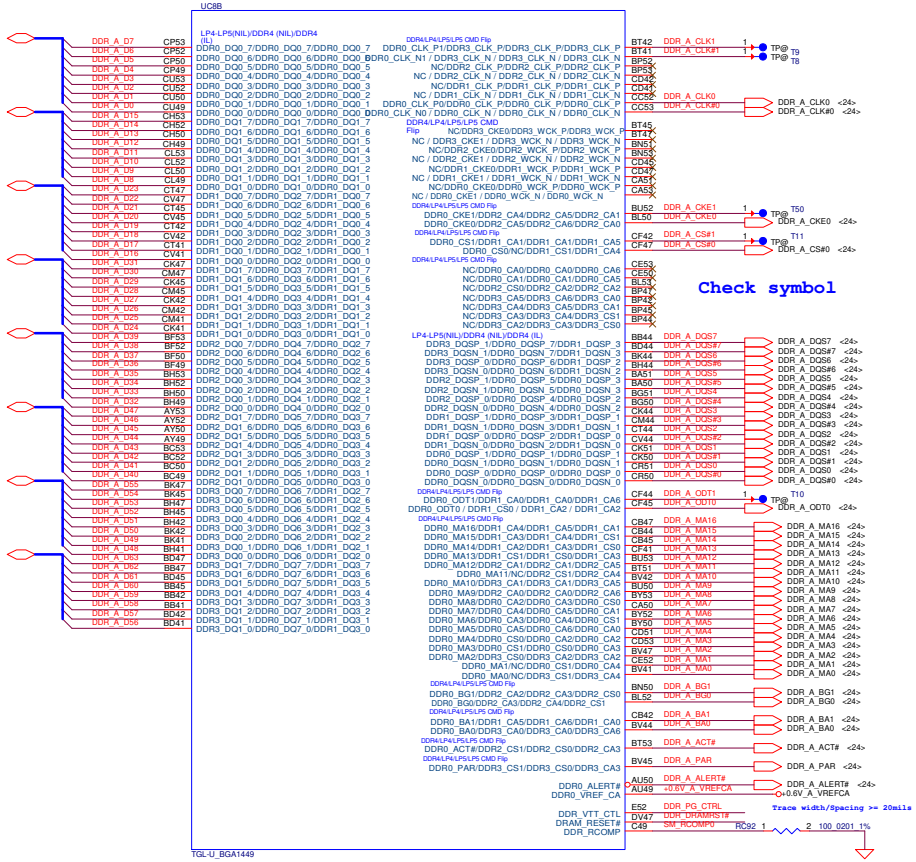
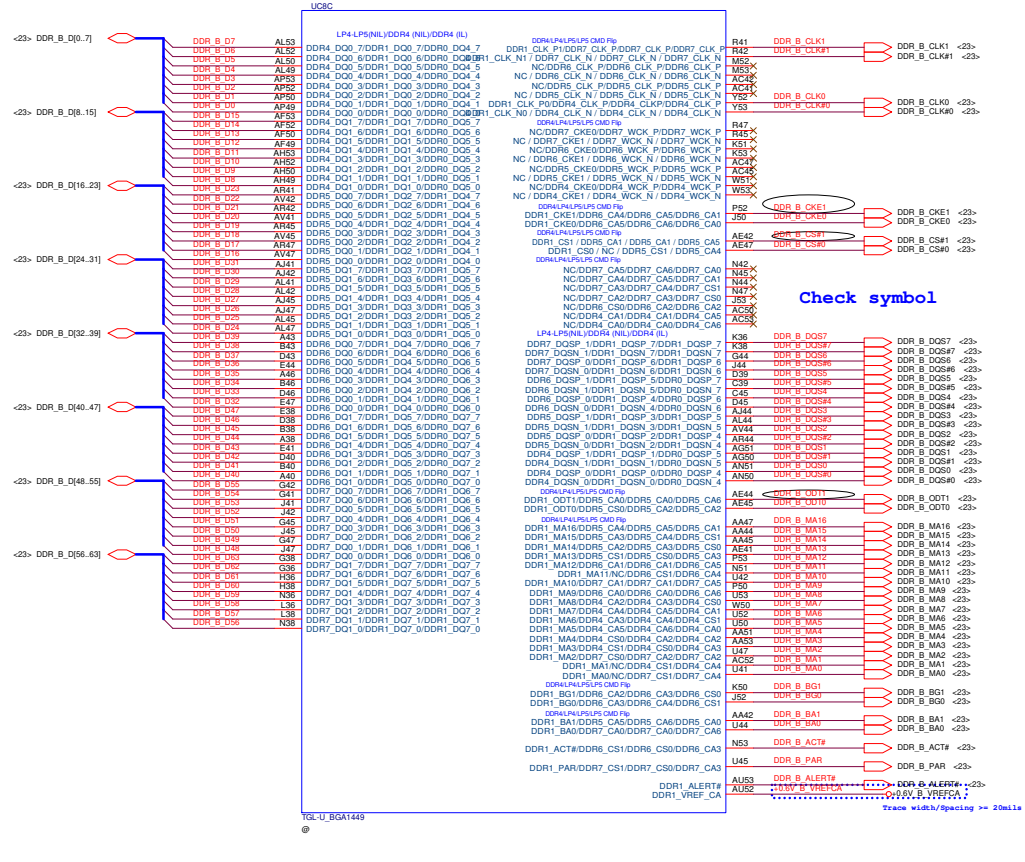
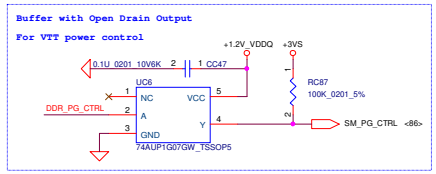
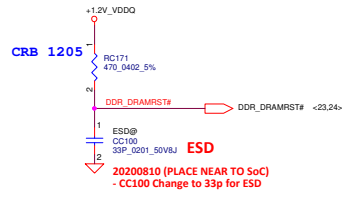
Follow Intel DDR4 NIL

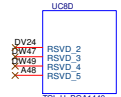
DDR4: Refer to 609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5











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Compal Electronics, Inc.

Title: **TGL-UP3(3/14)DDR4**

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	LA-K811P	1A
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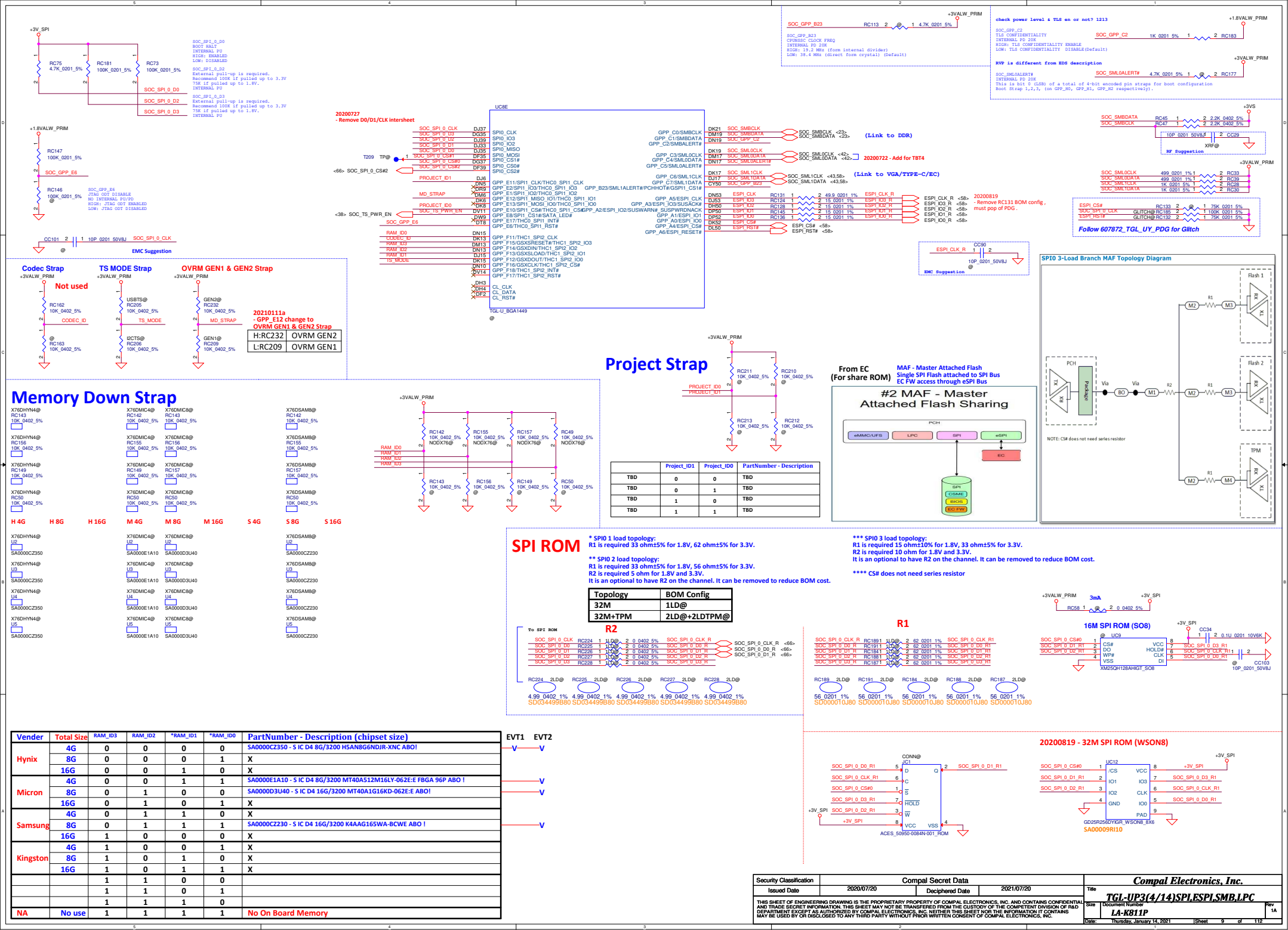

Topology	BOM Config
32M	1LD@
32M+TPM	2LD@+2LDTPM@

	Project_ID1	Project_ID0	PartNumber - Description
TBD	0	0	TBD
TBD	0	1	TBD
TBD	1	0	TBD
TBD	1	1	TBD

Vender	Total Size	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description (chipset size)	EVT1	EVT2
Hynix	4G	0	0	0	0	SA0000CZ350 - S IC D4 8G/3200 H5AN8G6NDJR-XNC ABO!	V	V
	8G	0	0	0	1	X		
	16G	0	0	1	0	X		
Micron	4G	0	0	1	1	SA0000E1A10 - S IC D4 8G/3200 MT40A512M16LY-062E:E FBGA 96P ABO !	V	V
	8G	0	1	0	0	SA0000D3U40 - S IC D4 16G/3200 MT40A1G16KD-062E:E ABO!	V	V
	16G	0	1	0	1	X		
Samsung	4G	0	1	1	0	X		
	8G	0	1	1	1	SA0000CZ230 - S IC D4 16G/3200 K4AAG165WA-BCWE ABO !	V	V
	16G	1	0	0	0	X		
Kingston	4G	1	0	0	1	X		
	8G	1	0	1	0	X		
	16G	1	0	1	1	X		
		1	1	0	0			
		1	1	0	1			
		1	1	1	0			
NA	No use	1	1	1	1	No On Board Memory		

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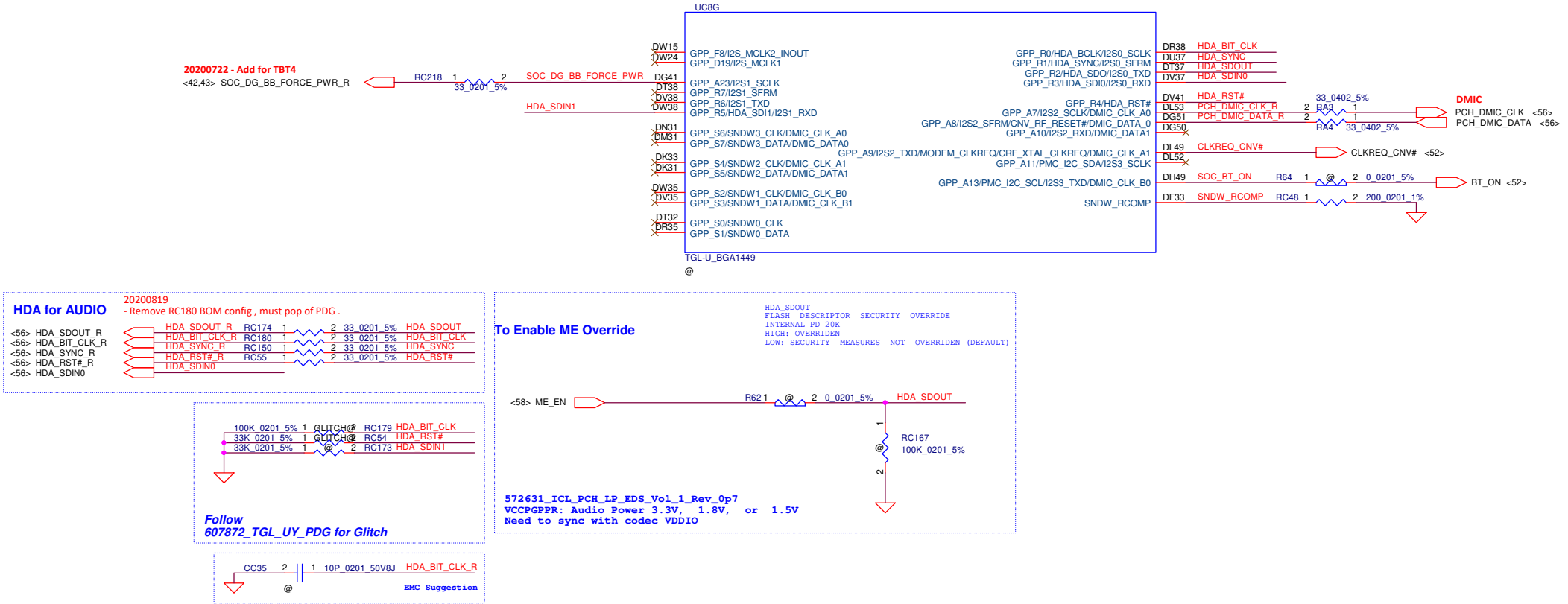

HDA for AUDIO

20200819
- Remove RC180 BOM config , must pop of PDG .

To Enable ME Override

HDA_SDOUT
FLASH DESCRIPTOR SECURITY OVERRIDE
INTERNAL PD 20K
HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

572631_ICL_PCH_LP_EDS_Vol_1_Rev_0p7
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: TGL-UP3(5/14)HDA,SNDW

Size	Document Number	Rev
	LA-K811P	1A

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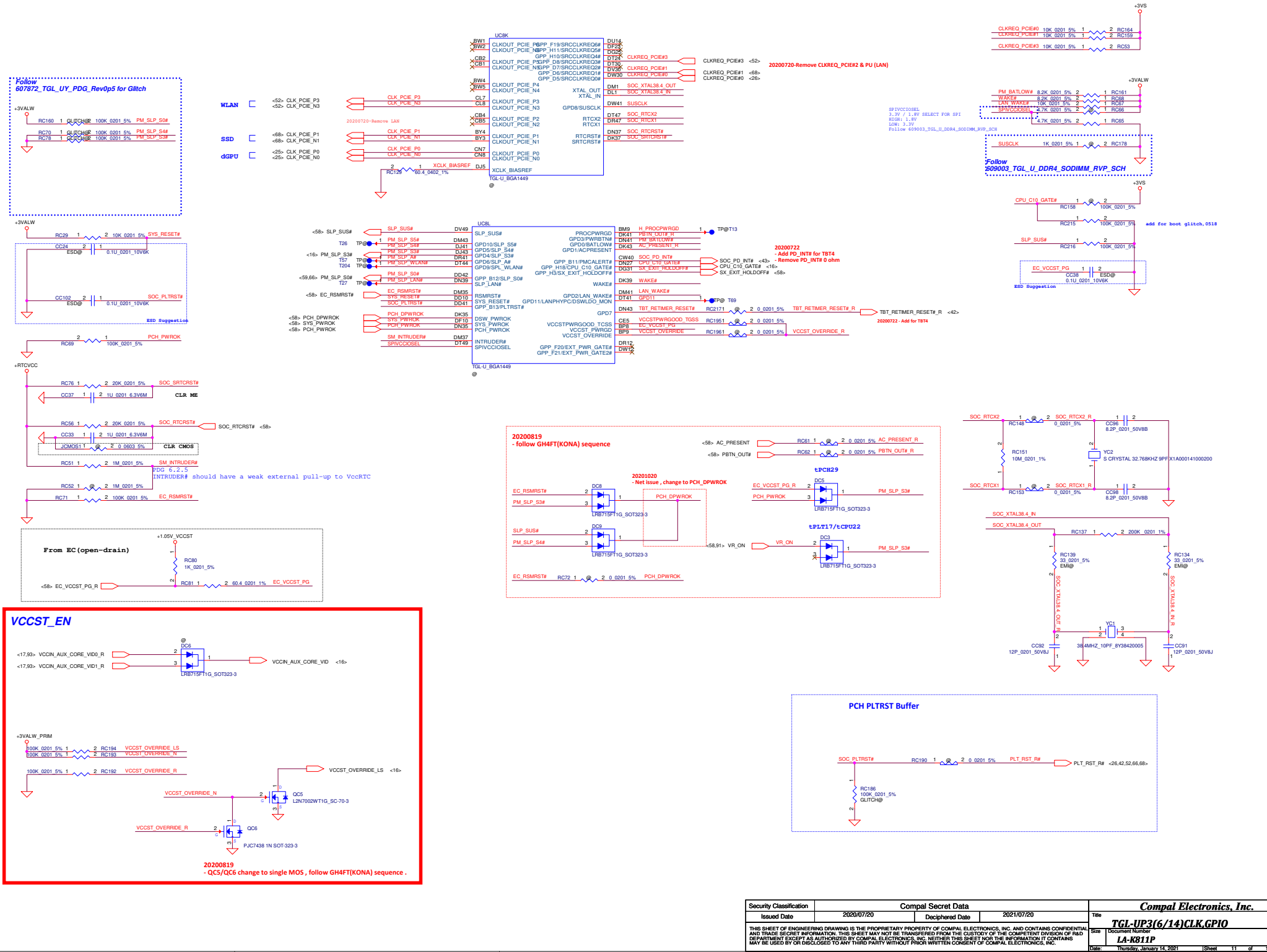

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Compal Electronics, Inc.			
Title	TGL-UP3(6/14)CLK,GPIO		
Size	Document Number		Rev
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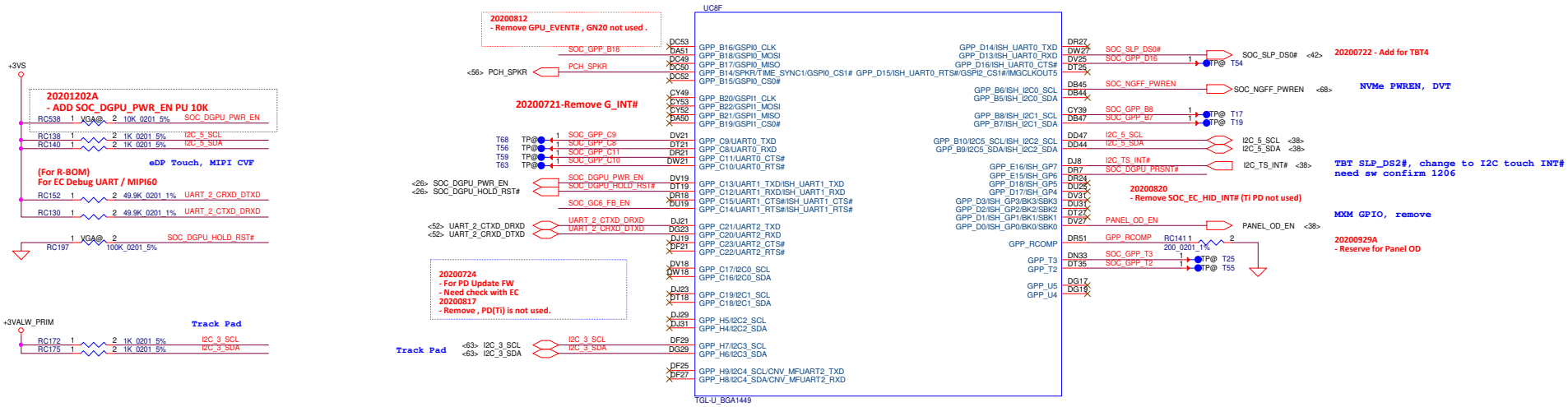

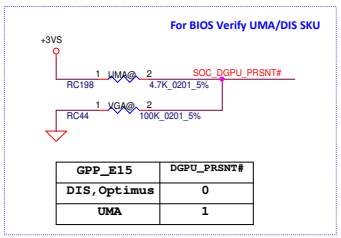

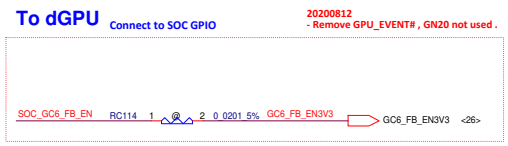

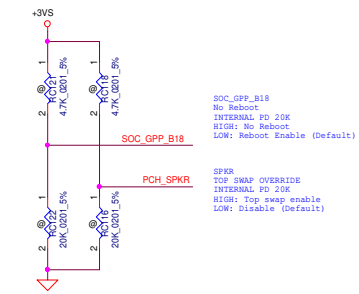

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Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: TGL-UP3(7/14)GPIO

Size	Document Number	Rev
	LA-K811P	1A

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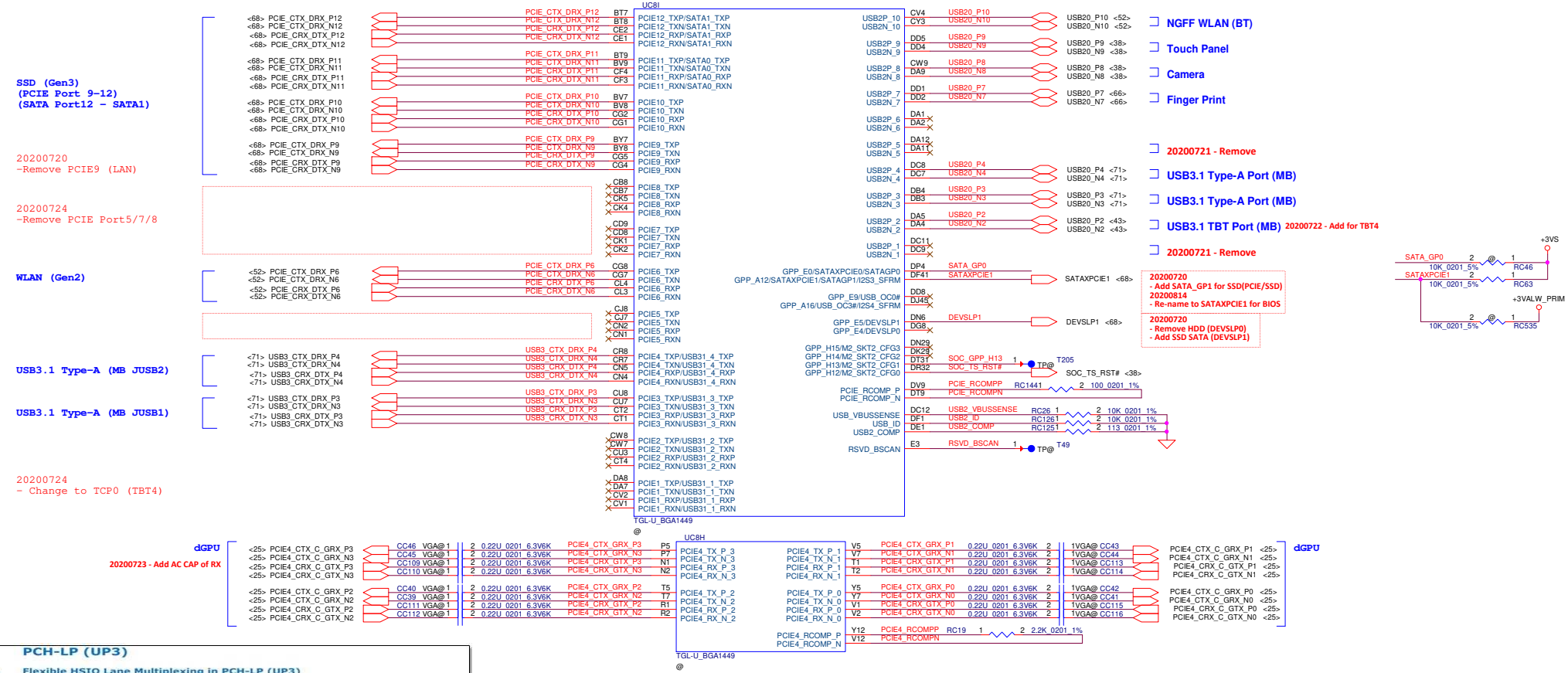

3.3 PCH-LP (UP3)

Figure 2. Flexible HSIO Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4			GbE	GbE	GbE		SATA 0	SATA 1

NOTE
Some lane multiplexing capabilities are not available on all SKUs. Refer to the PCH SKU section for specific SKU details.

Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): • CLKOUT_PCIE_P[6:0] • CLKOUT_PCIE_N[6:0] PCH-LP (Y): • CLKOUT_PCIE_P[6:1] • CLKOUT_PCIE_N[6:1]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

Figure 22. Tiger Lake PCH-LP SKU

CHIPSET SKU	Max USB 2.0 Nbr of Ports	USB 2.0 P1	USB 2.0 P2	USB 2.0 P3	USB 2.0 P4	USB 2.0 P5	USB 2.0 P6	USB 2.0 P7	USB 2.0 P8	USB 2.0 P9	USB 2.0 P10 (or CNVi BT)	USBr1	USBr2
PREMIUM-UP4	6												
PREMIUM-UP3	10												
MAINSTREAM BASE-UP3	8												

Port Disabled | Port Enabled | Port Enabled for Intel® Wireless-AC only

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Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title	TGL-UP3(8/14)PCIE,USB,SATA		
Size	Document Number		Rev
	LA-K811P		1A
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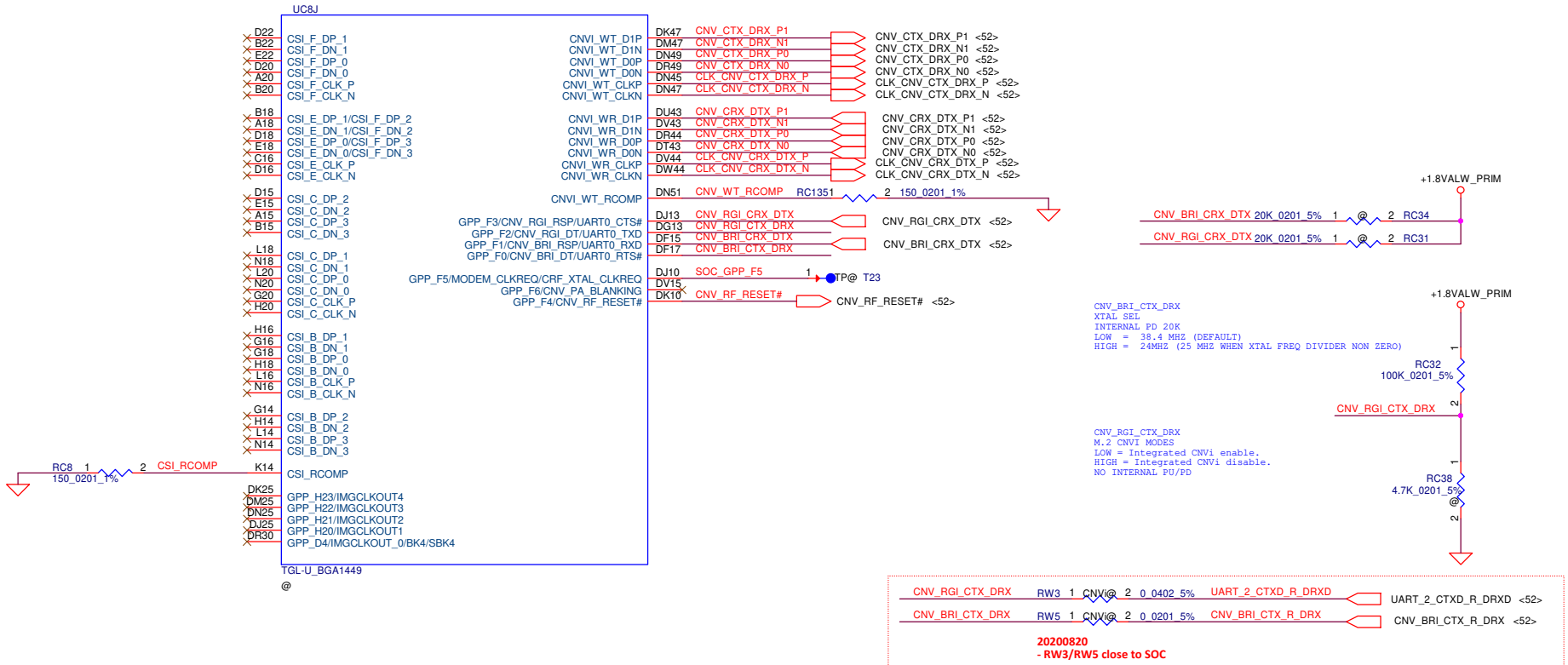

Compal Electronics, Inc.

Title: TGL-UP3(9/14)CSI,CNV

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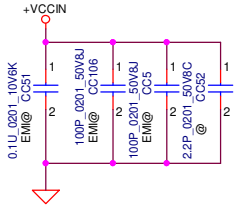
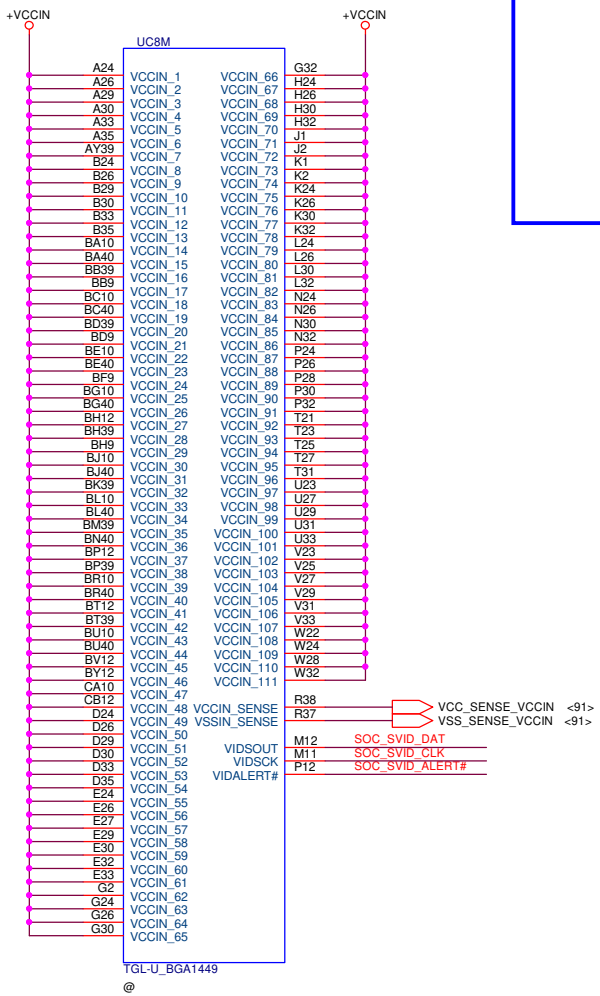
Package size?

EMC CAPS-PLACE
< 5mm from SOC VCCIN

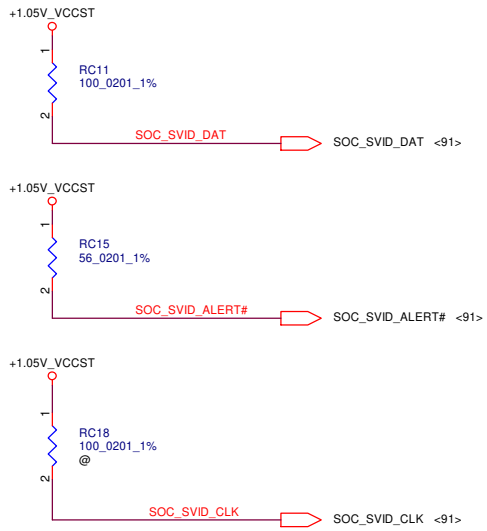




SVID DATA

SVID ALERT

SVID CLOCK



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Compal Electronics, Inc.

Title: TGL-UP3(10/14)Power, SVID

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EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)

+1.2V_VDDQ

2P_0201_6V8C CC12 EMI@
100P_0201_50V8J CC13 EMI@
2P_0201_6V8C CC15 EMI@
100P_0201_50V8J CC17 EMI@
2P_0201_6V8C CC16 EMI@
100P_0201_50V8J CC18 EMI@

UC8 TGL-U_BGA1449 @

AA39	VDDQ_1	VCCSTG_OUT_1	AF9
AB40	VDDQ_2	VCCSTG_1	AF12
AC39	VDDQ_3	VCCSTG_2	AD12
AD40	VDDQ_4	VCCSTG_OUT_2	AN10
AD51	VDDQ_5	VCCSTG_OUT_3	AM9
AD52	VDDQ_6	VCCSTG_OUT_4	AG10
AE39	VDDQ_7	VCCION_OUT	V15
AF40	VDDQ_8		M9
AG39	VDDQ_9	VCCSTG_OUT_LGC	
AH40	VDDQ_10	VCCST_1	BT2
AJ39	VDDQ_11	VCCST_2	BT1
AK40	VDDQ_12	VCCST_3	BT4
AK51	VDDQ_13	VCCSTG_3	BP2
AK52	VDDQ_14	VCCSTG_4	BP1
AL39	VDDQ_15	VCCSTG_5	BP4
AM40	VDDQ_16		
AN39	VDDQ_17		
AP40	VDDQ_18		
AP39	VDDQ_19		
AT52	VDDQ_20		
AU40	VDDQ_21		
AW40	VDDQ_22		
AW51	VDDQ_23		
AW52	VDDQ_24		
BD51	VDDQ_25		
BD52	VDDQ_26		
BK51	VDDQ_27		
BK52	VDDQ_28		
BV51	VDDQ_29		
BV52	VDDQ_30		
CA40	VDDQ_31		
CC40	VDDQ_32		
CC49	VDDQ_33		
CC50	VDDQ_34		
CE40	VDDQ_35		
CG40	VDDQ_36		
CH39	VDDQ_37		
CJ40	VDDQ_38		
CL40	VDDQ_39		
CN40	VDDQ_40		
CP47	VDDQ_41		
CP40	VDDQ_42		
D50	VDDQ_43		
E51	VDDQ_44		
F49	VDDQ_45		
T51	VDDQ_46		
T52	VDDQ_47		

+1.05VS_VCCSTG_OUT_FUSE
+1.05V_VCCIO_OUT
+1.05VS_VCCSTG_OUT_LGC
+1.05V_VCCST
+1.05VS_VCCSTG

+1.05VS_VCCSTG_OUT_LGC
+1.05VS_VCCSTG_OUT_LGC_TERM
RC101 1 @ 2 0_0402_5%

+1.05V_VCCST
+1.05VS_VCCSTG
+1.05VS_VCCSTG_OUT_FUSE
+1.05VS_VCCSTG_OUT_FUSE

1U_0201_10V6M CC73
1U_0201_10V6M CC74
1U_0201_10V6M CC69
1U_0201_10V6M CC72
1U_0201_10V6M CC59
1U_0201_10V6M CC1

clsoe AF9
clsoe AD12
clsoe AN10

VCCST_EN_LS
RC21 0_0201_5%
VCCST_EN_LS_R
1U_0201_6.3V6M CC1

+1.05VO_OUT_FET
1U_0201_6.3V6M CC2
+5VALW
CC7 0.1U_0201_10V6K @
PREM@
1U_0201_6.3V6M CC58

UC1 S IC G2894KD1U TDFN2X3
IN1 OUT1
EN1 CT1
VBIAS GND
EN2 CT2
IN2 OUT2
GND PAD

VCCST_EN_LS_R
VCCSTG_EN_LS_R
SA0000D5C00
footprint use
SA00007QK00

+1.05V_VCCST_R
Imax : 0.445 A
CC10 0.1U_0201_10V6K
RC23 1 @ 2 0_0402_5%
CC1041 2 1000P_0201_50V7K
CC1051 @ 2 1000P_0201_50V7K
@ RC104 0_0603_5%

+1.05VS_VCCSTG_R
Imax : 0.119 A
CC60 0.1U_0201_10V6K PREM@
PREM@ RC112 0_0402_5%
+1.05VS_VCCSTG

+1.05V_VCCST

VCCST
I (Max) : 0.455 A(+1.05V_VCCST)
RDS(Typ) : 3.5 mohm
V drop : 0.0016V

20200824
- Reserved for Volume Design
- VOL@ change to @

VCCSTG
I (Max) : 0.119 A(+1.05VS_VCCSTG)
RDS(Typ) : 3.5 mohm
V drop : 0.0004V

VCCSTG_EN_LS
RC111 0_0201_5%
VCCSTG_EN_LS_R
RC214 100K_0201_5% PREM@

CC105 Must be @
CPU_C10_GATE# stable to +1.05VS_VCCSTG <= 65us (tCPU26)

Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

+1.2V_VDDQ
+1.2V_VDDQ
+1.2V_VDDQ

VCCST/VCCSTG Enable

<11> PM_SLP_S3#
PM_SLP_S3# RC77 1 2 0_0201_5%
<58,78,84,86> SUSP#
SUSP# RC2081 @ 2 0_0201_5%
+3VALW_PRIM
CC36 0.1U_0201_10V6K @
<11> VCCIN_AUX_CORE_VID
<11> VCCST_OVERRIDE_LS
VCCIN_AUX_CORE_VID
VCCST_OVERRIDE_LS
UC5 MC74VHC1G32DFT2G_SC70-5-D
footprint use
SA00000OJ00
pop (SA0000C8300)
VCCST_STG_COM_EN
DC2 LRB715FT1G_SOT323-3
VCCST_EN_LS
DC1 LRB715FT1G_SOT323-3
VCCSTG_EN_LS
PREM@
RC74 1 PREM@ 2 0_0201_5%
<11> CPU_C10_GATE#
CPU_C10_GATE# RC79 1 @ 2 0_0201_5%

Figure 231. VCCST Enable Logic

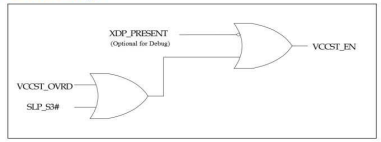
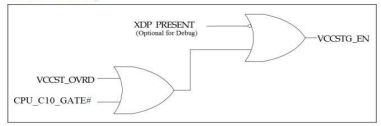


Figure 232. VCCSTG Enable Logic



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Compal Electronics, Inc.	
Title	TGL-UP3(11/14)Power
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+1.8VALW_PRIM
+1.8V_PRIM_MCP
RC60 1 @ 2 0_0603_5%
+3VALW
+3VALW_DSW
RC166 1 @ 2 0_0402_5%

+1.8V_PRIM_MCP
@
L3 1 2 4.7UH_UHP252012BF-4R7M_20%
RC59 1 2 0_0402_5%
+1.8V_VCCA_CLKLDO
RC57 0_0402_5%
CC32 47U_0603_6.3V6M

+3VALW TO +3V_PRIM

1354mA

+3VALW
JPC1 JUMP_43X39 @
+3VALW_PRIM
CC31 4.7U_0402_6.3V6M

Package size?

EMC CAPS-PLACE
< 5mm from SOC VCCIN_AUX

+VCCIN_AUX
0.1U_0201_10V6K EMI@ CC83
100P_0201_50V8J EMI@ CC81
100P_0201_50V8J EMI@ CC79
2.2P_0201_50V8C @ CC57

+VCCIN_AUX
UC8N
+1.8V_PRIM_MCP

AB12	VCCIN_AUX_1	VCCPRIM_1P8_1	CY18
AC10	VCCIN_AUX_2	VCCPRIM_1P8_2	CY20
AE10	VCCIN_AUX_3	VCCPRIM_1P8_3	CY24
AK2	VCCIN_AUX_4	VCCPRIM_1P8_4	CY26
AR10	VCCIN_AUX_5	VCCPRIM_1P8_5	DA18
AT12	VCCIN_AUX_6	VCCPRIM_1P8_6	DA20
AU10	VCCIN_AUX_7	VCCPRIM_1P8_7	DA22
AW10	VCCIN_AUX_8	VCCPRIM_1P8_8	DA24
BV1	VCCIN_AUX_9	VCCPRIM_1P8_9	DA26
BV39	VCCIN_AUX_10	VCCPRIM_1P8_10	DC18
BW40	VCCIN_AUX_11	VCCPRIM_1P8_11	DC20
BY39	VCCIN_AUX_12	VCCPRIM_1P8_12	DC22
CC1	VCCIN_AUX_13	VCCPRIM_1P8_13	DC24
CD12	VCCIN_AUX_14	VCCPRIM_1P8_14	DC26
CF10	VCCIN_AUX_15	VCCPRIM_1P8_15	DD20
CG12	VCCIN_AUX_16	VCCPRIM_1P8_16	DD22
CH10	VCCIN_AUX_17	VCCPRIM_1P8_17	DV22
CJ1	VCCIN_AUX_18		
CJ12	VCCIN_AUX_19	VCCPRIM_3P3_1	DA35
CK10	VCCIN_AUX_20	VCCPRIM_3P3_2	DC28
CL12	VCCIN_AUX_21	VCCPRIM_3P3_3	DC30
CM10	VCCIN_AUX_22	VCCPRIM_3P3_4	DD30
CP1	VCCIN_AUX_23		
CP10	VCCIN_AUX_24	DCPRTC	DV34
CR12	VCCIN_AUX_25		DV46
CT10	VCCIN_AUX_26	VCCLDOSTD_0P85	
CU12	VCCIN_AUX_27		DV16
CY1	VCCIN_AUX_28	VCCA_CLKLDO_1P8_1	DC15
AK1	VCCIN_AUX_29	VCCA_CLKLDO_1P8_2	
			DV28
AV9	VCCIN_AUX_VSSSENSE	VCCDPHY_1P24	
AT9	VCCIN_AUX_VCCSENSE		DD38
		VCCDSW_1P05	
DD17	VCC_VNNEXT_1P05_1		BR3
DD18	VCC_VNNEXT_1P05_2	VCC1P05_OUT_FET_1	BR4
		VCC1P05_OUT_FET_2	BT5
DA15	VCC_V1P05EXT_1P05_1	VCC1P05_OUT_FET_3	
DA17	VCC_V1P05EXT_1P05_2		DA31
		VCCPRIM_1P05_1	DC33
DB39	GPP_B2/VRALERT#	VCCPRIM_1P05_2	DC31
DV12	GPP_F22/VNN_CTRL	VCCPRIM_1P05_3	
DT12	GPP_F23/V1P05_CTRL		DC35
		VCCRTC	DD37
DB37	GPP_B0/CORE_VID0	VCCDSW_3P3	DA28
DB38	GPP_B1/CORE_VID1	VCCPGPPR	
			CY31
		VCCPRIM_3P3_5	CY33
		VCCPRIM_3P3_6	CY39
		VCCPRIM_1P8_18	
		RSVD_1	AP12

TGL-U_BGA1449
@

+1.05VO_VNNBYPASS
+1.05VO_EXTBYPASS
R25 @ 100K_0201_5%
R24 @ 100K_0201_5%

<93> VSS_SENSE_VCCIN_AUX
<93> VCC_SENSE_VCCIN_AUX

+3VALW_PRIM
+VO_VCCDCPRTC
+0.85VO_VCCLDOSTD
+1.8V_VCCA_CLKLDO
+1.24VO_VCCDPHY
+1.05VO_VCCDSW
+1.05VO_OUT_FET
+1.05VO_OUT_PCH
+RTCVCC
+3VALW_DSW
+3VALW_PRIM
for HDA=3V
+3VALW_PRIM
+1.8V_PRIM_MCP
+VCCANA_EHV
TP@T12

check SW function , 1225

<7,43> VCCIN_AUX_CORE_ALERT#_R
RC98 1 @ 2 0_0201_5% VCCIN_AUX_CORE_ALERT#
VNN_CTRL
V1.05P_CTRL
T203 TP@
T60 TP@

<11,93> VCCIN_AUX_CORE_VID0_R
<11,93> VCCIN_AUX_CORE_VID1_R
RC82 1 @ 2 0_0201_5% VCCIN_AUX_CORE_VID0
RC85 1 @ 2 0_0201_5% VCCIN_AUX_CORE_VID1

+3VALW_PRIM
RC83 1 2 100K_0201_5% VCCIN_AUX_CORE_VID0_R
RC84 1 2 100K_0201_5% VCCIN_AUX_CORE_VID1_R

NOTE:
576591-tgl-pch-lp-eds-vol1of2-rev0p5
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.

607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with either VCCPRIM_1P8 or VCCPRIM_3P3 depending on their operating voltage.

RTC Battery

MAX. 8000mil

+RTCBATT
W=20mil
RC86 1K_0402_5%
+CHGRTC
DC4 LRB715FT1G_SOT323-3
W=40mil
2mA
+RTCVCC
1U_0201_6.3V6M CC30
0.1U_0201_10V6K CC28
W=20mil

+RTCBATT
JRTC1 ACES_50271-0020N-001
CONN@
SP02000RO00

+3VALW_DSW
@CC99 1U_0201_10V6M
+1.05VO_VCCDSW
CC23 1U_0201_10V6M
+0.85VO_VCCLDOSTD
CC94 2.2U_0201_6.3V6M
+1.8V_PRIM_MCP
CC37 1U_0201_10V6M @
+3VALW_PRIM
CC21 0.1U_0201_10V6K
CC22 1U_0201_10V6M @
+1.24VO_VCCDPHY
CC95 4.7U_0402_6.3V6M
+VO_VCCDCPRTC
CC33 0.1U_0201_10V6K

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Compal Electronics, Inc.

Title: TGL-UP3(12/14)Power

Size	Document Number	Rev
	LA-K811P	1A

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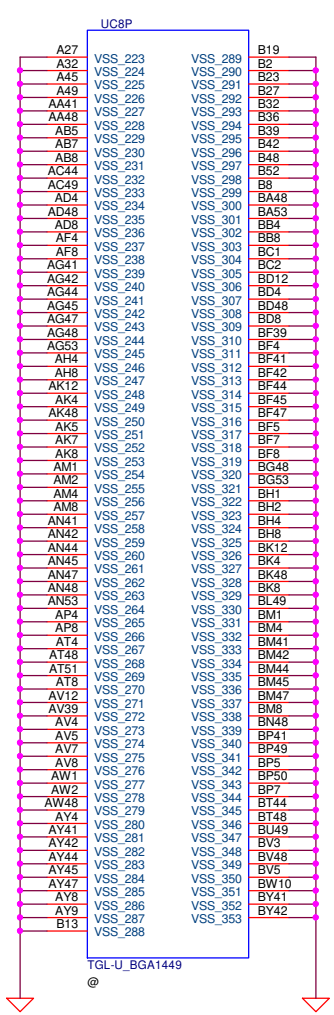

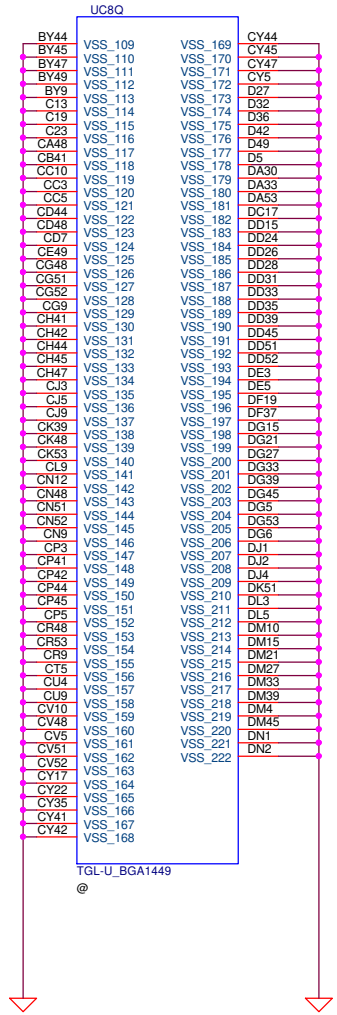

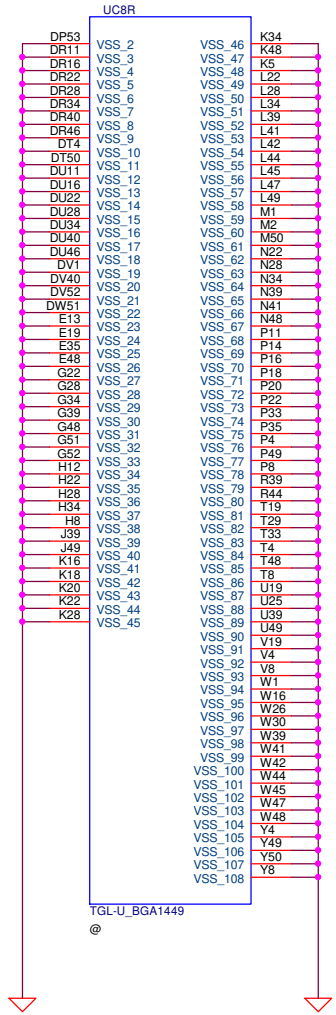

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **TGL-UP3(13/14)GND**

Size | Document Number: **LA-K811P** | Rev: 1A

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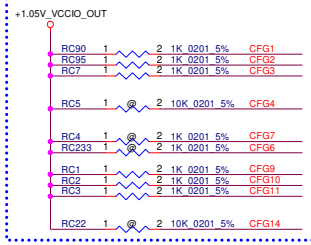
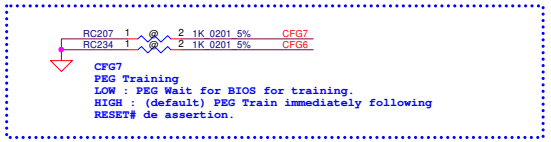
20200901
- Update Table (PDG 2.0)

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[5]	RSVD	None	1K ohm
CFG[6:7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	1K ohm
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

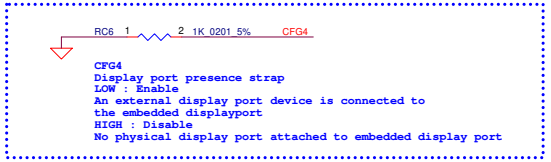
CFG Signals have int. PH 3K ohm.



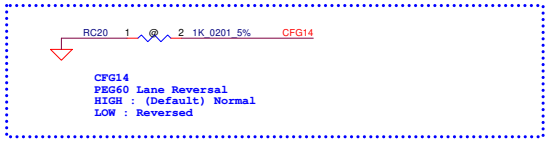
20200901
- RC4 change to 1k (CFG7) for PDG2.0 update .
- Add RC233 1K PU & C233 1K PD (CFG6) for PDG2.0 update & Intel SCH review .



CFG7
PEG Training
LOW : PEG Wait for BIOS for training.
HIGH : (default) PEG Train immediately following RESET# de assertion.

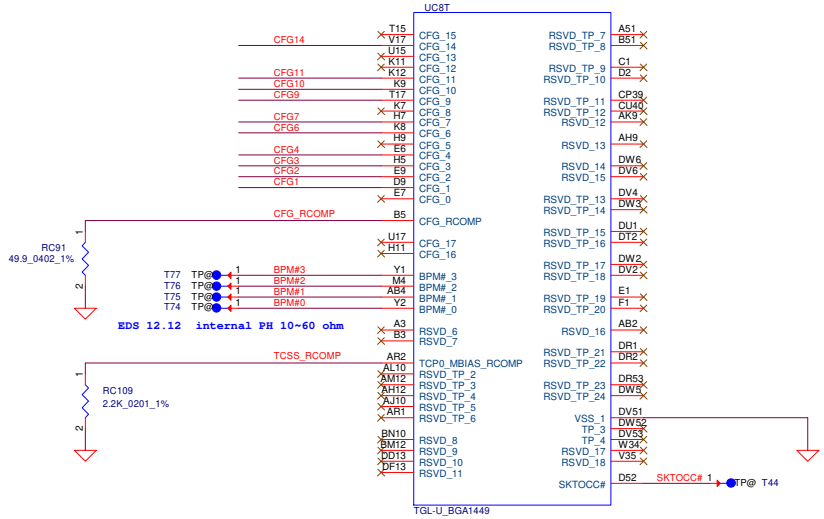


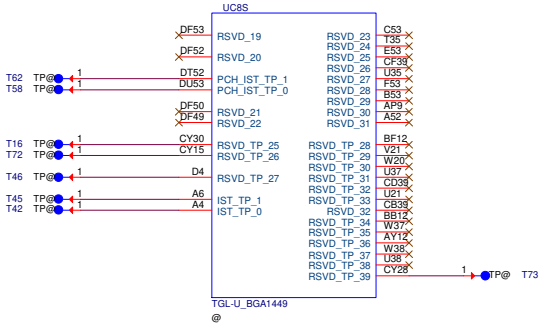
CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port



CFG14
PEG60 Lane Reversal
HIGH : (Default) Normal
LOW : Reversed

CFG Signals
(For Strap & XDP)





Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.	
Title	TGL-UP3(14/14)RSVD,CFG
Size	Document Number: LA-K811P
Rev	1A
Date:	Thursday, January 14, 2021
Sheet	19 of 112

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: **Reserve for SOC/PCH/FCH**

Size	Document Number	Rev
	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 20 of 112

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: **Reserve for SOC/PCH/FCH**

Size	Document Number	Rev
	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 21 of 112

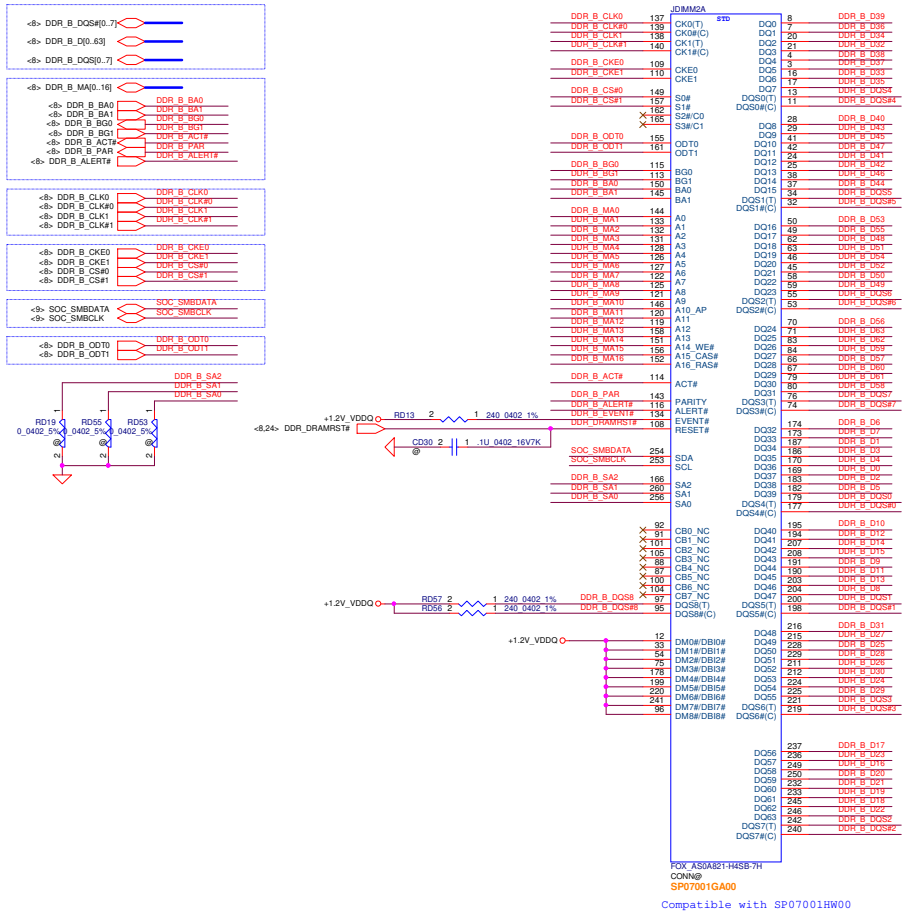
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

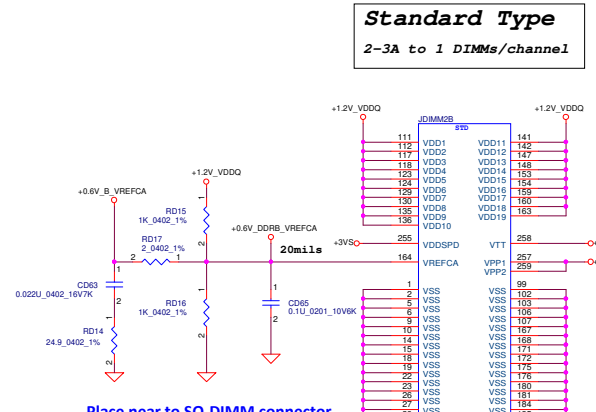
Compal Electronics, Inc.

Title: **Reserve for SOC/PCH/FCH**

Size	Document Number	Rev
	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 22 of 112

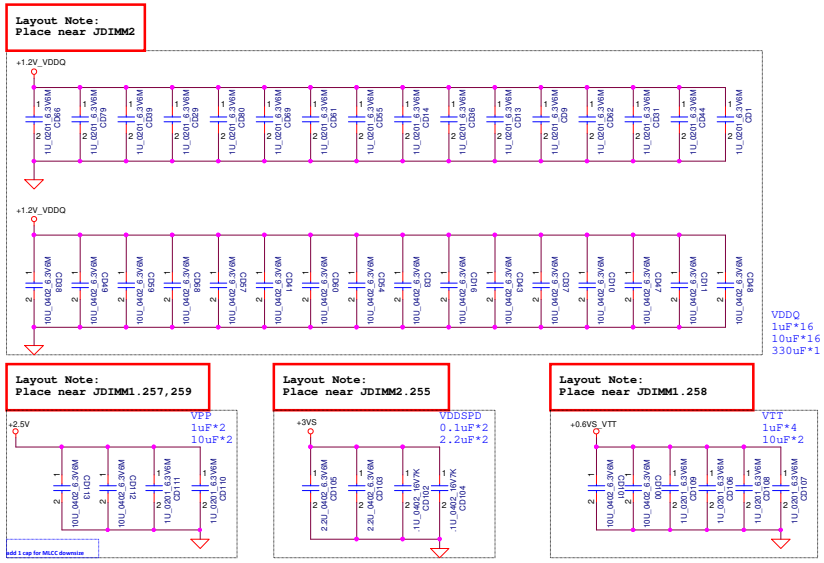




Standard Type

2-3A to 1 DIMMs/channel

Interleaved Memory



Refer for DDR4 SO-DIMM Decoupling Caps
607872_TGL_UY_PDG_Rev0p5

Table 50. DDR4 SODIMM Power Plane Decoupling

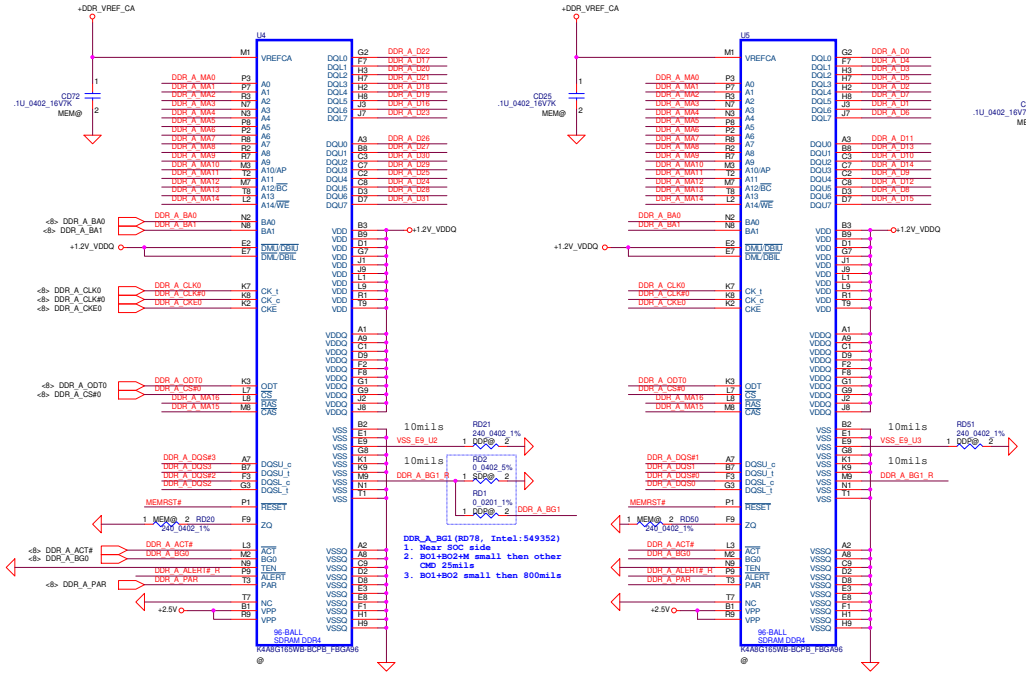
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	1 cap per DIMM. Place close to DIMM	2x 0.1µF (0402)
		1 cap per DIMM. Place close to DIMM	2x 2.2µF (0402)

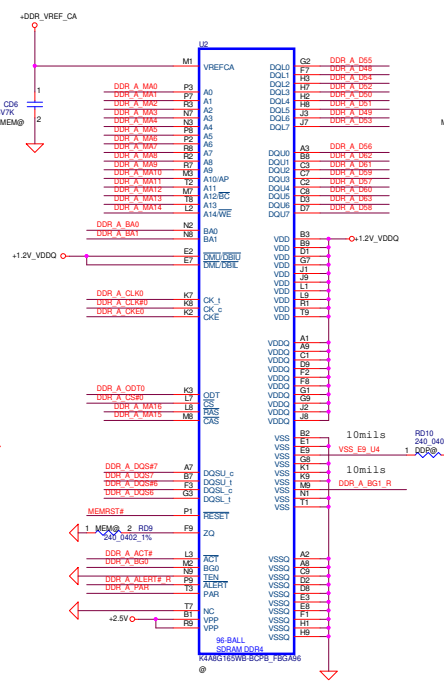
Note: 1. Total quantity is referring to 2 channels.

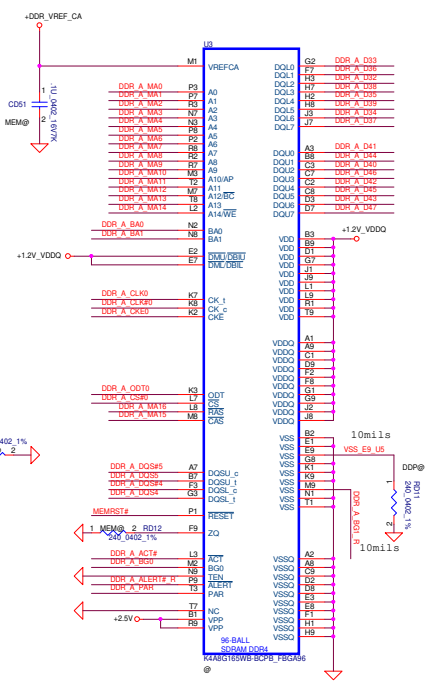
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

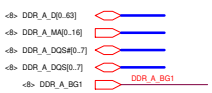
Compal Electronics, Inc.			
Title: DDR4 DIMMA			
Size: Custom	Document Number: LA-K811P		Rev: 1A
Date: Thursday, January 14, 2021		Sheet 23 of 112	

change SDP footprint







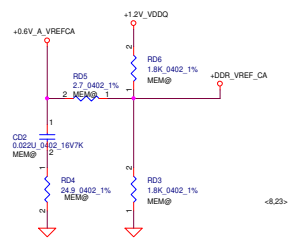


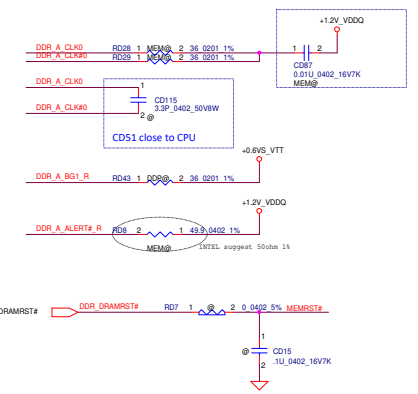
DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS
RCOMP[0] (SOC side)	200_1%	121_1%

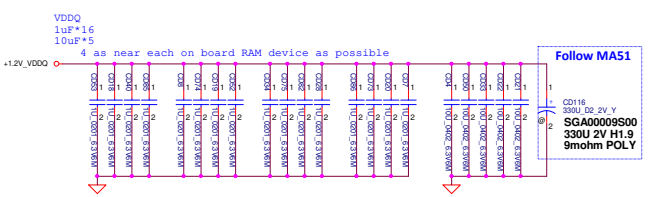
SDP@ RD21 0_0402_5% SD028000080
SDP@ RD10 0_0402_5% SD028000080
SDP@ RD51 0_0402_5% SD028000080
SDP@ RD11 0_0402_5% SD028000080

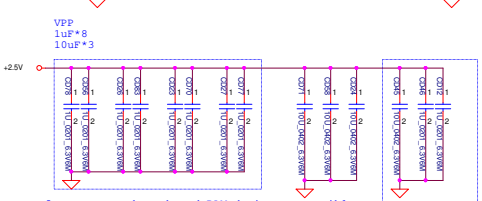
20200824
- Where ????

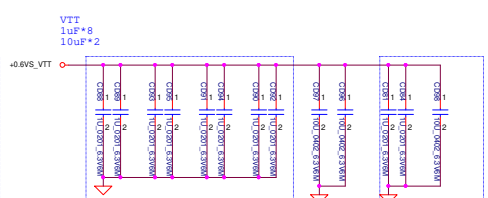
TERMINATION











Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDR4 ON BOARD CHIPS

Size: Custom | Document Number: LA-K811P | Rev: 1A

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TGL-UP3 only support x4

20200723 - Link OK

+1.8VSDGPU_AON

RV501 VGA@ 10K_0201_5%

<26> PLTRST_VGA#_1V8 → PLTRST_VGA#_1V8

<26> VGA_CLKREQ#_R → VGA_CLKREQ#_R

UV1A
GN20-E7
BGA2714
COMMON

1/24 PCI_EXPRESS

	BR31	PEX_WAKE
	BT30	PEX_RST
	BP31	PEX_CLKREQ
<11> CLK_PCIE_P0	BJ30	PEX_REFCLK
<11> CLK_PCIE_N0	BK30	PEX_REFCLK
<13> PCIE4_CRX_C_GTX_P0	BL31	PEX_TX0
<13> PCIE4_CRX_C_GTX_N0	BM31	PEX_TX0
<13> PCIE4_CTX_C_GRX_P0	BR32	PEX_RX0
<13> PCIE4_CTX_C_GRX_N0	BT32	PEX_RX0
<13> PCIE4_CRX_C_GTX_P1	BJ32	PEX_TX1
<13> PCIE4_CRX_C_GTX_N1	BK32	PEX_TX1
<13> PCIE4_CTX_C_GRX_P1	BP33	PEX_RX1
<13> PCIE4_CTX_C_GRX_N1	BR33	PEX_RX1
<13> PCIE4_CRX_C_GTX_P2	BL33	PEX_TX2
<13> PCIE4_CRX_C_GTX_N2	BM33	PEX_TX2
<13> PCIE4_CTX_C_GRX_P2	BR34	PEX_RX2
<13> PCIE4_CTX_C_GRX_N2	BT34	PEX_RX2
<13> PCIE4_CRX_C_GTX_P3	BJ34	PEX_TX3
<13> PCIE4_CRX_C_GTX_N3	BK34	PEX_TX3
<13> PCIE4_CTX_C_GRX_P3	BP35	PEX_RX3
<13> PCIE4_CTX_C_GRX_N3	BR35	PEX_RX3
	BL35	PEX_TX4
	BM35	PEX_TX4
	BR36	PEX_RX4
	BT36	PEX_RX4
	BJ36	PEX_TX5
	BK36	PEX_TX5
	BP37	PEX_RX5
	BR37	PEX_RX5
	BL37	PEX_TX6
	BM37	PEX_TX6
	BR38	PEX_RX6
	BT38	PEX_RX6
	BJ38	PEX_TX7
	BK38	PEX_TX7
	BP39	PEX_RX7
	BR39	PEX_RX7
	BL39	PEX_TX8
	BM39	PEX_TX8
	BR40	PEX_RX8
	BT40	PEX_RX8
	BJ40	PEX_TX9
	BK40	PEX_TX9
	BP41	PEX_RX9
	BR41	PEX_RX9
	BL41	PEX_TX10
	BM41	PEX_TX10
	BR42	PEX_RX10
	BT42	PEX_RX10
	BJ42	PEX_TX11
	BK42	PEX_TX11
	BP43	PEX_RX11
	BR43	PEX_RX11
	BL43	PEX_TX12
	BM43	PEX_TX12
	BR44	PEX_RX12
	BT44	PEX_RX12
	BJ44	PEX_TX13
	BK44	PEX_TX13
	BP45	PEX_RX13
	BR45	PEX_RX13
	BL45	PEX_TX14
	BM45	PEX_TX14
	BR46	PEX_RX14
	BT46	PEX_RX14
	BL47	PEX_TX15
	BM47	PEX_TX15
	BP47	PEX_RX15
	BR47	PEX_RX15

PEX_DVDD	BF32	
PEX_DVDD	BF34	
PEX_DVDD	BF35	
PEX_DVDD	BF37	
PEX_DVDD	BG32	
PEX_DVDD	BG34	
PEX_DVDD	BG35	
PEX_DVDD	BG37	
PEX_DVDD	BH32	
PEX_DVDD	BH34	
PEX_DVDD	BH35	
PEX_DVDD	BH37	
PEX_CVDD	BF31	
PEX_CVDD	BG31	
PEX_CVDD	BH31	
PEX_HVDD	BF38	
PEX_HVDD	BF40	
PEX_HVDD	BF41	
PEX_HVDD	BG38	
PEX_HVDD	BG40	
PEX_HVDD	BG41	
PEX_HVDD	BG43	
PEX_HVDD	BG44	
PEX_HVDD	BH38	
PEX_HVDD	BH40	
PEX_HVDD	BH41	
PEX_HVDD	BH43	
PEX_HVDD	BH44	
PEX_PLL_HVDD	BF43	
PEX_CVDD_SENSE	BK46	20200723 - Remove PEX_CVDD_SENSE
PEX_TERMP	BT50	PEX_TERMP

+PEX_VDD

Under GPU: CV10, CV11, CV12, CV13, CV14, CV15, CV16, CV17 — VGA@ 1U_0201_6.3V6M / 4.7U_0402_6.3V6M
1U_0402*6(X6S)
4.7U_0603*2(X6S)

Near GPU: CV18, CV19, CV20, CV21, CV22 — VGA@ 10U_0402_6.3V6M / 22U_0603_6.3V6M
10U_0805*3
22U_0805*2

+1.8VSDGPU_AON

Under GPU: CV23, CV24, CV25, CV26, CV27, CV28, CV29, CV30, CV31, CV32, CV33 — VGA@ 1U_0201_6.3V6M / 4.7U_0402_6.3V6M
1U_0402*9(X6S)
4.7U_0603*2(X6S)

Near GPU: CV34, CV2812, CV36, CV37, CV38 — VGA@ 10U_0402_6.3V6M / 22U_0603_6.3V6M
10U_0805*3
22U_0805*2

+PEX_PLL_HVDD

RV529 VGA@ 0_0402_5%

+1.8VSDGPU_AON

CV452 VGA@ 1U_0201_6.3V6M

RV11 VGA@ 2.49K_0402_1%

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: GN20E PEG

Size	Document Number	Rev
Custom	LA-K811P	1A

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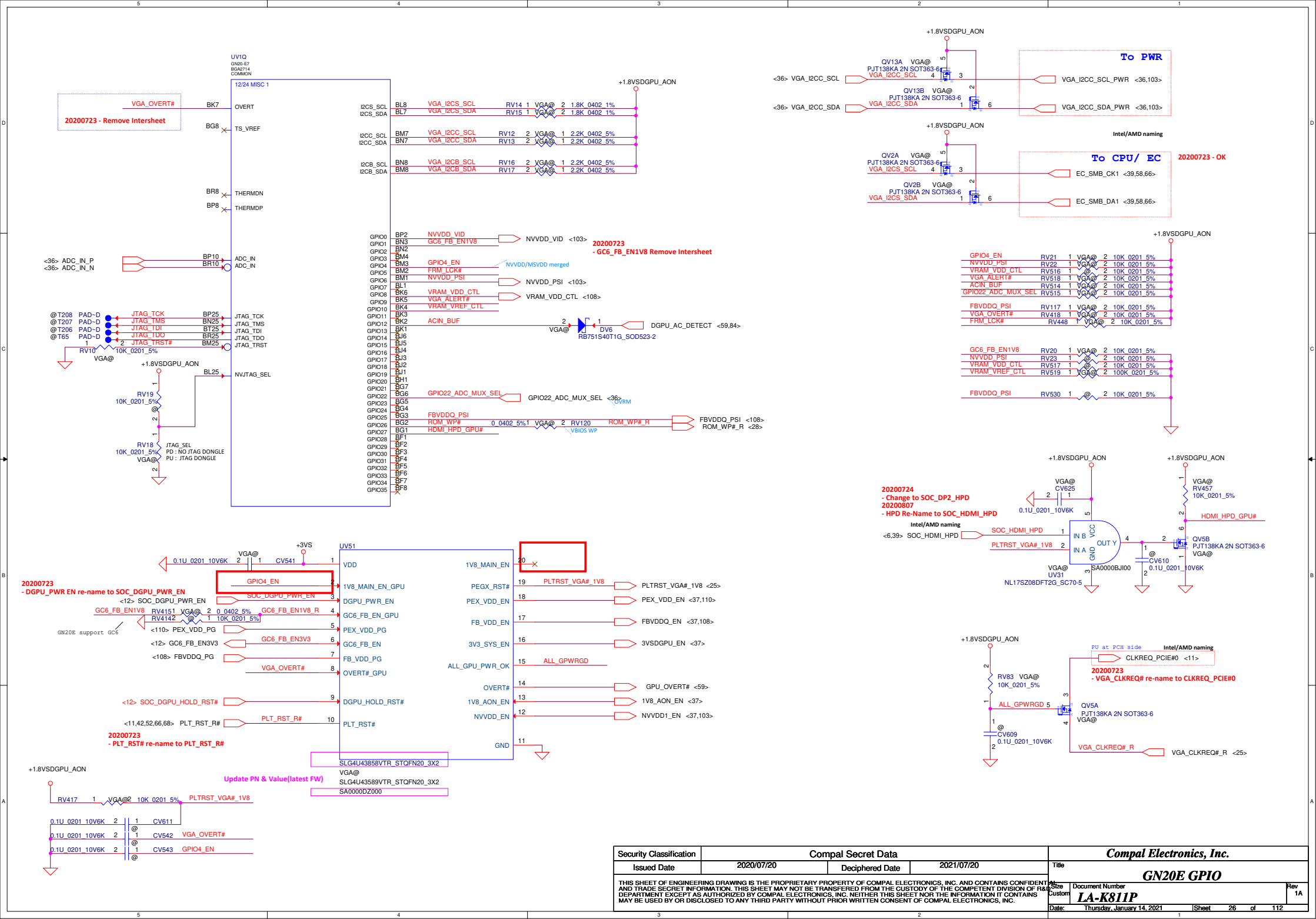
UV1Q
GN20-E7
BGA2714
COMMON
12/24 MISC 1
VGA_OVERT#
20200723 - Remove Intersheet
BK7 OVERT
BG8 TS_VREF
BR8 THERMDN
BP8 THERMDP
I2CS_SCL BL8 VGA_I2CS_SCL RV14 1 VGA@ 2 1.8K_0402_1%
I2CS_SDA BL7 VGA_I2CS_SDA RV15 1 VGA@ 2 1.8K_0402_1%
I2CC_SCL BM7 VGA_I2CC_SCL RV12 2 VGA@ 1 2.2K_0402_5%
I2CC_SDA BN7 VGA_I2CC_SDA RV13 2 VGA@ 1 2.2K_0402_5%
I2CB_SCL BN8 VGA_I2CB_SCL RV16 2 VGA@ 1 2.2K_0402_5%
I2CB_SDA BM8 VGA_I2CB_SDA RV17 2 VGA@ 1 2.2K_0402_5%
+1.8VSDGPU_AON
<36> ADC_IN_P
<36> ADC_IN_N
BP10 ADC_IN
BR10 ADC_IN
GPIO0 BP2 NVVDD_VID NVVDD_VID <103>
GPIO1 BN3 GC6_FB_EN1V8
20200723
- GC6_FB_EN1V8 Remove Intersheet
GPIO4 BM3 GPIO4_EN
FRM_LCK# NVVDD/MSVDD merged
BM2 FRM_LCK#
GPIO5 BM1 NVVDD_PSI NVVDD_PSI <103>
GPIO6 BL1
GPIO7 BK6 VRAM_VDD_CTL VRAM_VDD_CTL <108>
GPIO8 BK5 VGA_ALERT#
GPIO9 BK4 VRAM_VREF_CTL
GPIO10 BK3
GPIO11 BK2 ACIN_BUF
DV6 RB751S40T1G_SOD523-2
DGPU_AC_DETECT <59,84>
@T208 PAD~D JTAG_TCK BP25 JTAG_TCK
@T207 PAD~D JTAG_TMS BN25 JTAG_TMS
@T206 PAD~D JTAG_TDI BT25 JTAG_TDI
@T65 PAD~D JTAG_TDO BR25 JTAG_TDO
JTAG_TRST# BM25 JTAG_TRST
RV10 10K_0201_5%
VGA@
BL25 NVJTAG_SEL
RV19 10K_0201_5%
RV18 10K_0201_5%
JTAG_SEL
PD : NO JTAG DONGLE
PU : JTAG DONGLE
GPIO12 BK1
GPIO13 BJ6
GPIO14 BJ5
GPIO15 BJ4
GPIO16 BJ3
GPIO17 BJ2
GPIO18 BJ1
GPIO19 BH1
GPIO20 BG7
GPIO21 BG6 GPIO22_ADC_MUX_SEL GPIO22_ADC_MUX_SEL <36>
GPIO22 BG5
GPIO23 BG4
GPIO24 BG3 FBVDDQ_PSI
GPIO25 BG2 ROM_WP#
GPIO26 BG1 HDMI_HPD_GPU#
GPIO27 BF1
GPIO28 BF2
GPIO29 BF3
GPIO30 BF4
GPIO31 BF5
GPIO32 BF6
GPIO33 BF7
GPIO34 BF8
GPIO35
0_0402_5%1 VGA@ 2 RV120 ROM_WP#_R
VBIOS WP
FBVDDQ_PSI <108>
ROM_WP#_R <28>
DVRM
+1.8VSDGPU_AON
QV13A VGA@ PJT138KA 2N SOT363-6
<36> VGA_I2CC_SCL VGA_I2CC_SCL
QV13B VGA@ PJT138KA 2N SOT363-6
<36> VGA_I2CC_SDA VGA_I2CC_SDA
To PWR
VGA_I2CC_SCL_PWR <36,103>
VGA_I2CC_SDA_PWR <36,103>
Intel/AMD naming
QV2A VGA@ PJT138KA 2N SOT363-6
VGA_I2CS_SCL
QV2B VGA@ PJT138KA 2N SOT363-6
VGA_I2CS_SDA
To CPU/ EC
20200723 - OK
EC_SMB_CK1 <39,58,66>
EC_SMB_DA1 <39,58,66>
GPIO4_EN RV21 1 VGA@ 2 10K_0201_5%
NVVDD_PSI RV22 1 VGA@ 2 10K_0201_5%
VRAM_VDD_CTL RV516 1 @ 2 10K_0201_5%
VGA_ALERT# RV518 1 VGA@ 2 10K_0201_5%
ACIN_BUF RV514 1 VGA@ 2 10K_0201_5%
GPIO22_ADC_MUX_SEL RV515 1 VGA@ 2 10K_0201_5%
FBVDDQ_PSI RV117 1 VGA@ 2 10K_0201_5%
VGA_OVERT# RV418 1 VGA@ 2 10K_0201_5%
FRM_LCK# RV448 1 VGA@ 2 10K_0201_5%
GC6_FB_EN1V8 RV20 1 VGA@ 2 10K_0201_5%
NVVDD_PSI RV23 1 @ 2 10K_0201_5%
VRAM_VDD_CTL RV517 1 @ 2 10K_0201_5%
VRAM_VREF_CTL RV519 1 VGA@ 2 100K_0201_5%
FBVDDQ_PSI RV530 1 @ 2 10K_0201_5%
20200724
- Change to SOC_DP2_HPD
20200807
- HPD Re-Name to SOC_HDMI_HPD
Intel/AMD naming
<6,39> SOC_HDMI_HPD
SOC_HDMI_HPD
PLTRST_VGA#_1V8
VGA@ CV625 0.1U_0201_10V6K
IN B VCC
IN A GND
OUT Y
SA0000BJI00
VGA@ UV31 NL17SZ08DFT2G_SC70-5
VGA@ RV457 10K_0201_5%
HDMI_HPD_GPU#
QV5B PJT138KA 2N SOT363-6
@ CV610 0.1U_0201_10V6K
+3VS
UV51
0.1U_0201_10V6K VGA@ CV541
20200723
- DGPU_PWR EN re-name to SOC_DGPU_PWR_EN
GPIO4_EN
SOC_DGPU_PWR_EN
<12> SOC_DGPU_PWR_EN
GC6_FB_EN1V8 RV4151 VGA@ 2 0_0402_5% GC6_FB_EN1V8_R
RV4142 @ 1 10K_0201_5%
GN20E support GC6
<110> PEX_VDD_PG
<12> GC6_FB_EN3V3 GC6_FB_EN3V3
<108> FBVDDQ_PG
VGA_OVERT#
<12> SOC_DGPU_HOLD_RST#
<11,42,52,66,68> PLT_RST_R#
PLT_RST_R#
20200723
- PLT_RST# re-name to PLT_RST_R#
VDD
1V8_MAIN_EN_GPU
DGPU_PWR_EN
GC6_FB_EN_GPU
PEX_VDD_PG
GC6_FB_EN
FB_VDD_PG
OVERT#_GPU
DGPU_HOLD_RST#
PLT_RST#
1V8_MAIN_EN
PEGX_RST#
PEX_VDD_EN
FB_VDD_EN
3V3_SYS_EN
ALL_GPU_PWR_OK
OVERT#
1V8_AON_EN
NVVDD_EN
GND
PLTRST_VGA#_1V8 PLTRST_VGA#_1V8 <25>
PEX_VDD_EN <37,110>
FBVDDQ_EN <37,108>
3VSDGPU_EN <37>
ALL_GPWRGD
GPU_OVERT# <59>
1V8_AON_EN <37>
NVVDD1_EN <37,103>
SLG4U43858VTR_STQFN20_3X2
VGA@
SLG4U43589VTR_STQFN20_3X2
SA0000DZ000
Update PN & Value(latest FW)
+1.8VSDGPU_AON
RV417 1 VGA@ 2 10K_0201_5% PLTRST_VGA#_1V8
0.1U_0201_10V6K CV611
0.1U_0201_10V6K CV542 VGA_OVERT#
0.1U_0201_10V6K CV543 GPIO4_EN
+1.8VSDGPU_AON
RV83 VGA@ 10K_0201_5%
ALL_GPWRGD
QV5A PJT138KA 2N SOT363-6
VGA@
CV609 0.1U_0201_10V6K
PU at PCH side
Intel/AMD naming
CLKREQ_PCIE#0 <11>
20200723
- VGA_CLKREQ# re-name to CLKREQ_PCIE#0
VGA_CLKREQ#_R
VGA_CLKREQ#_R <25>
Security Classification
Compal Secret Data
Issued Date
2020/07/20
Deciphered Date
2021/07/20
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Compal Electronics, Inc.
Title
GN20E GPIO
Size
Custom
Document Number
LA-K811P
Rev
1A
Date:
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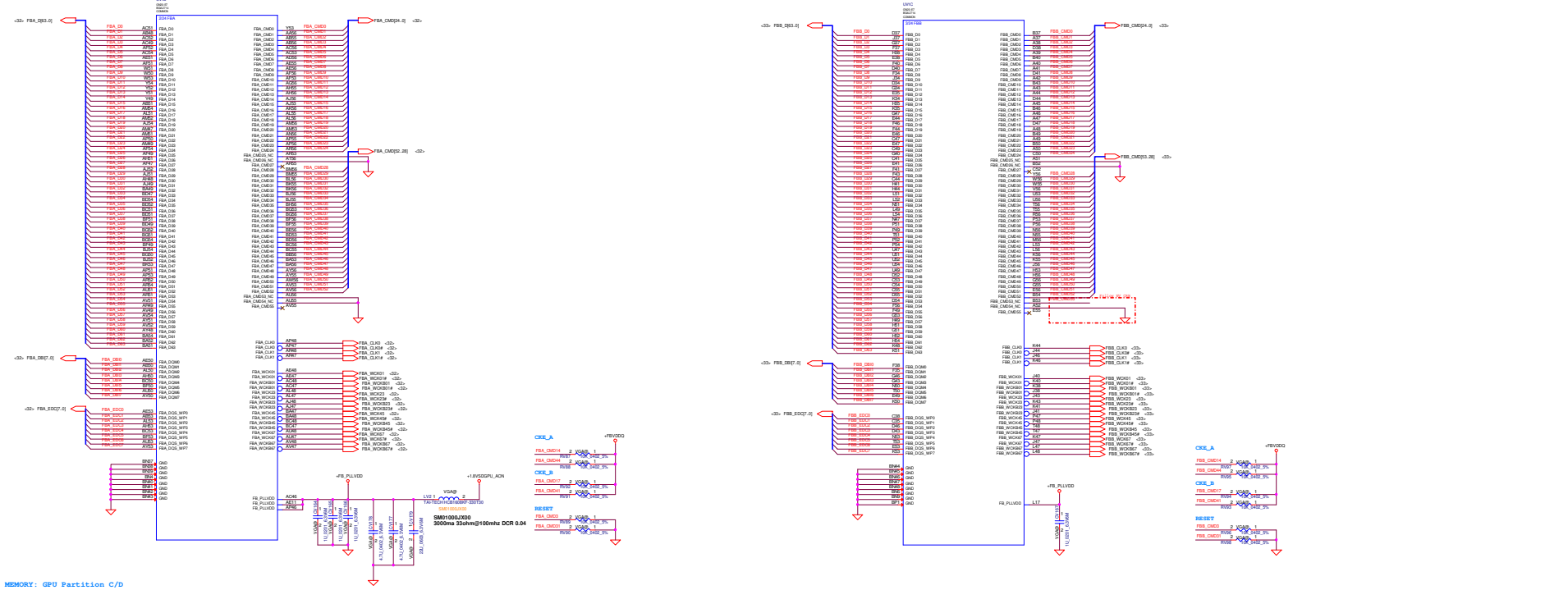
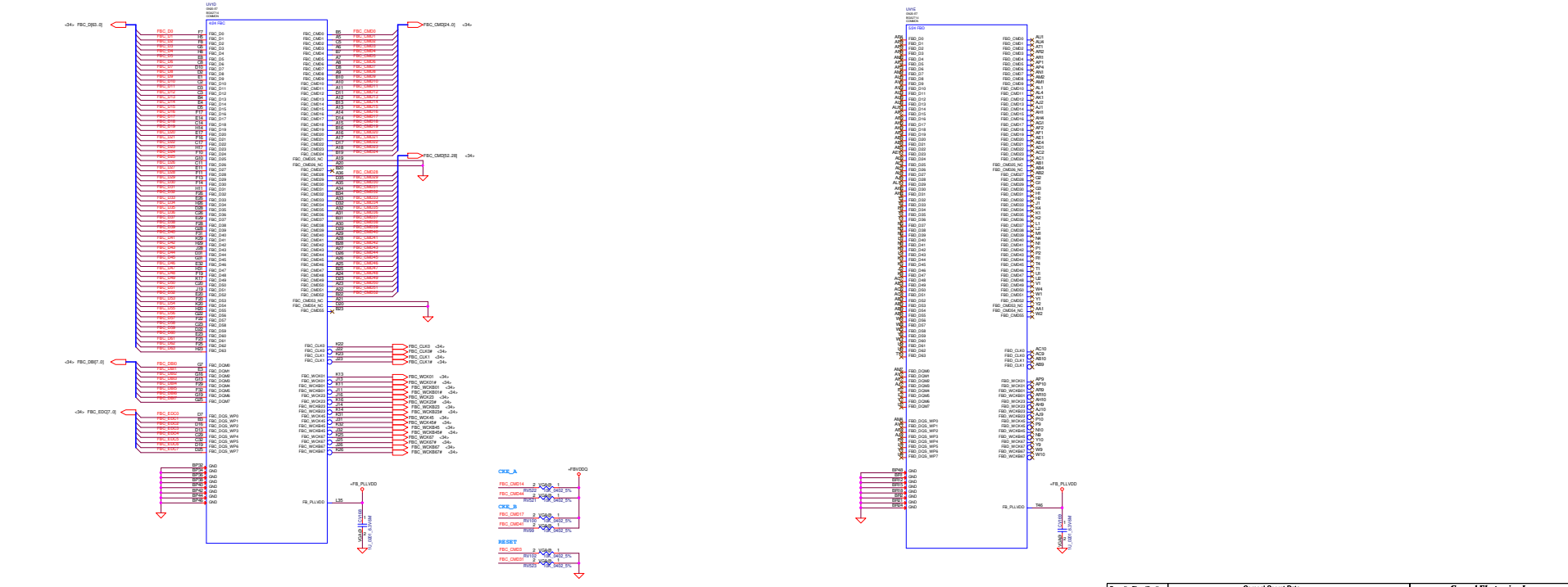
MEMORY: GPU Partition A/B



MEMORY: GPU Partition C/D



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Issued Date	2020/07/29	Deciphered Date	2021/07/29
			Title: GN20E MEM-AB
Size: Custom	Document Number: LA-K811P		Rev: 1A
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Vender	STRAP1 RV33/RV34	STRAP0 RV31/RV32	PartNumber - Description
Samsung	0 : RV34	0 : RV32	SA0000C6280 256M32 K4Z80325BC-HC14 1.2V
Micron	0 : RV34	1 : RV31	SA0000DUW20 256M32 H56C8H24AIR-S2C
Hynix	1 : RV33	0 : RV32	SA0000BND80 MT61K256M32JE-14:A 1.2V

20200824
- STRAP2 keep 0 , RV36 change VGA@
- VRAM just only 3 type .

Strap 1

X76VSAM@	X76VMIC@	X76VHYN@
RV34 100K_0402_1% SD034100380	RV34 100K_0402_1% SD034100380	RV33 100K_0402_1% SD034100380

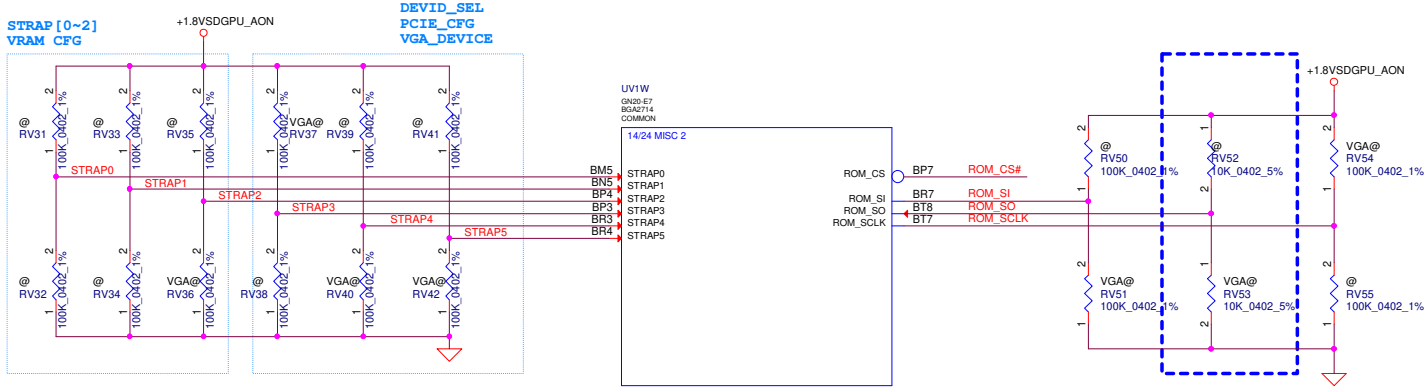
Strap 0

X76VSAM@	X76VMIC@	X76VHYN@
RV32 100K_0402_1% SD034100380	RV31 100K_0402_1% SD034100380	RV32 100K_0402_1% SD034100380

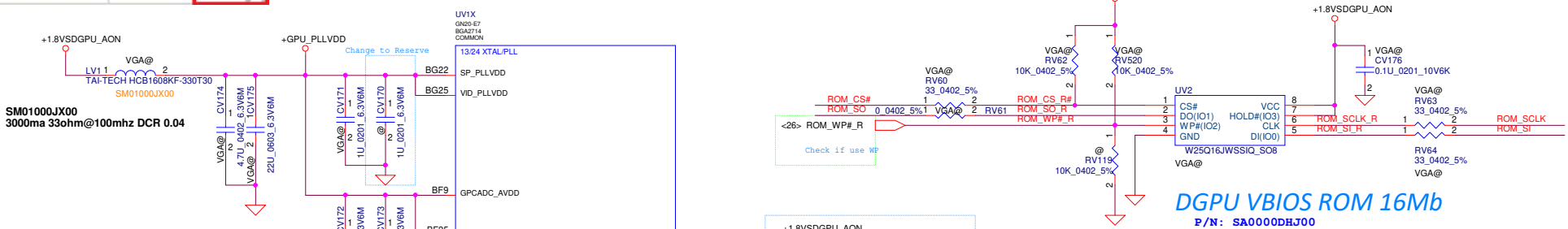
Vendor	Manufacturer Part Number	Die Revision	Strap
Samsung	K4Z80325BC-HC14	C-die	0x0
Hynix	H56C8H24AIR-S2C	A-die	0x2
Micron	MT61K256M32JE-14:A	A-die	0x1

STRAP [0~2]
VRAM CFG

STRAP [3~5]
SMB ALT_ADDR
DEVID_SEL
PCIE_CFG
VGA_DEVICE



The Strap for ROM_SO should be 10K while all others are 100K.



DGPU VBIOS ROM 16Mb

P/N: SA0000DHJ00

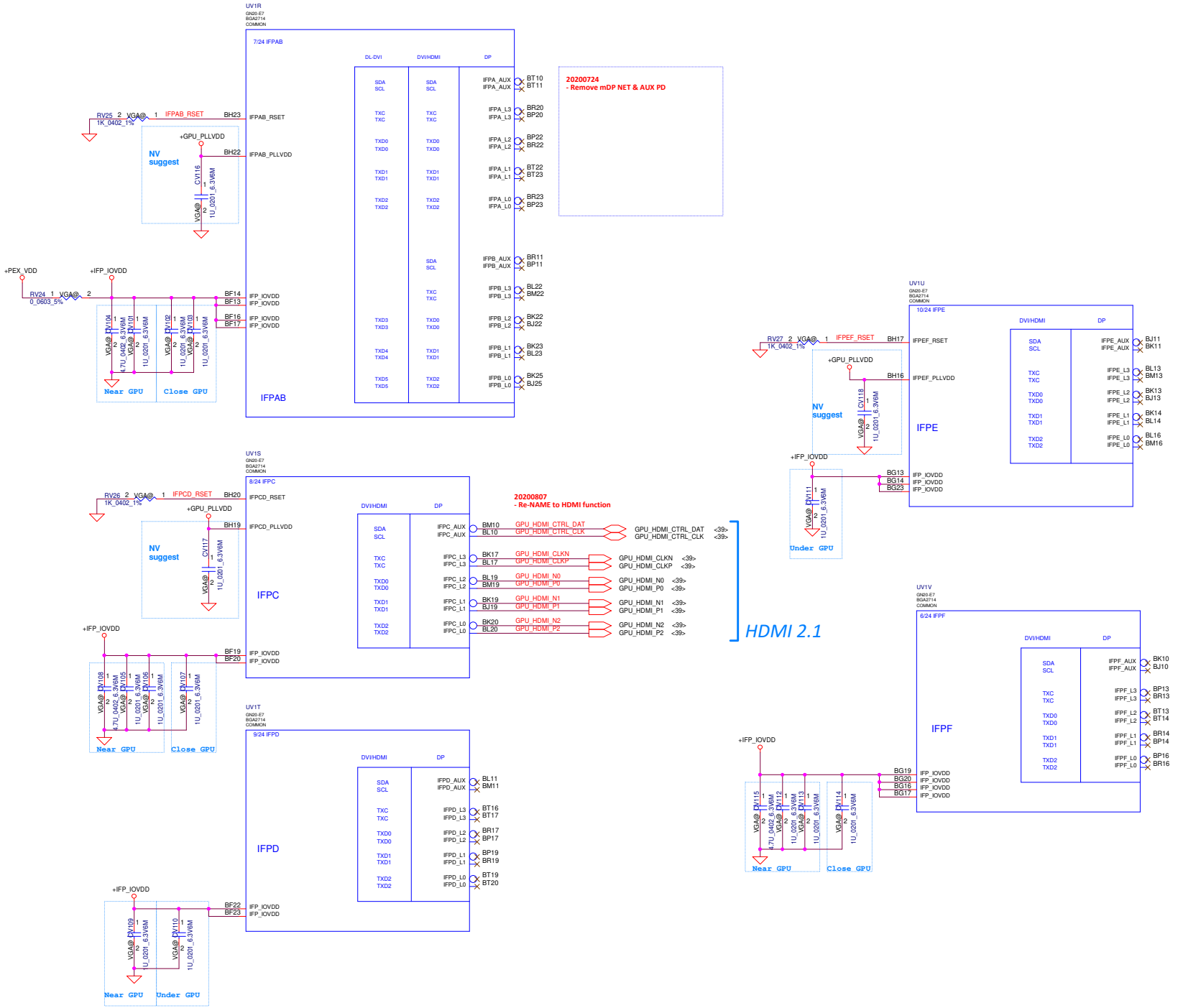
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: GN20E RON/XTAL

Size: Custom | Document Number: LA-K811P | Rev: 1A

Date: Thursday, January 14, 2021 | Sheet 28 of 112



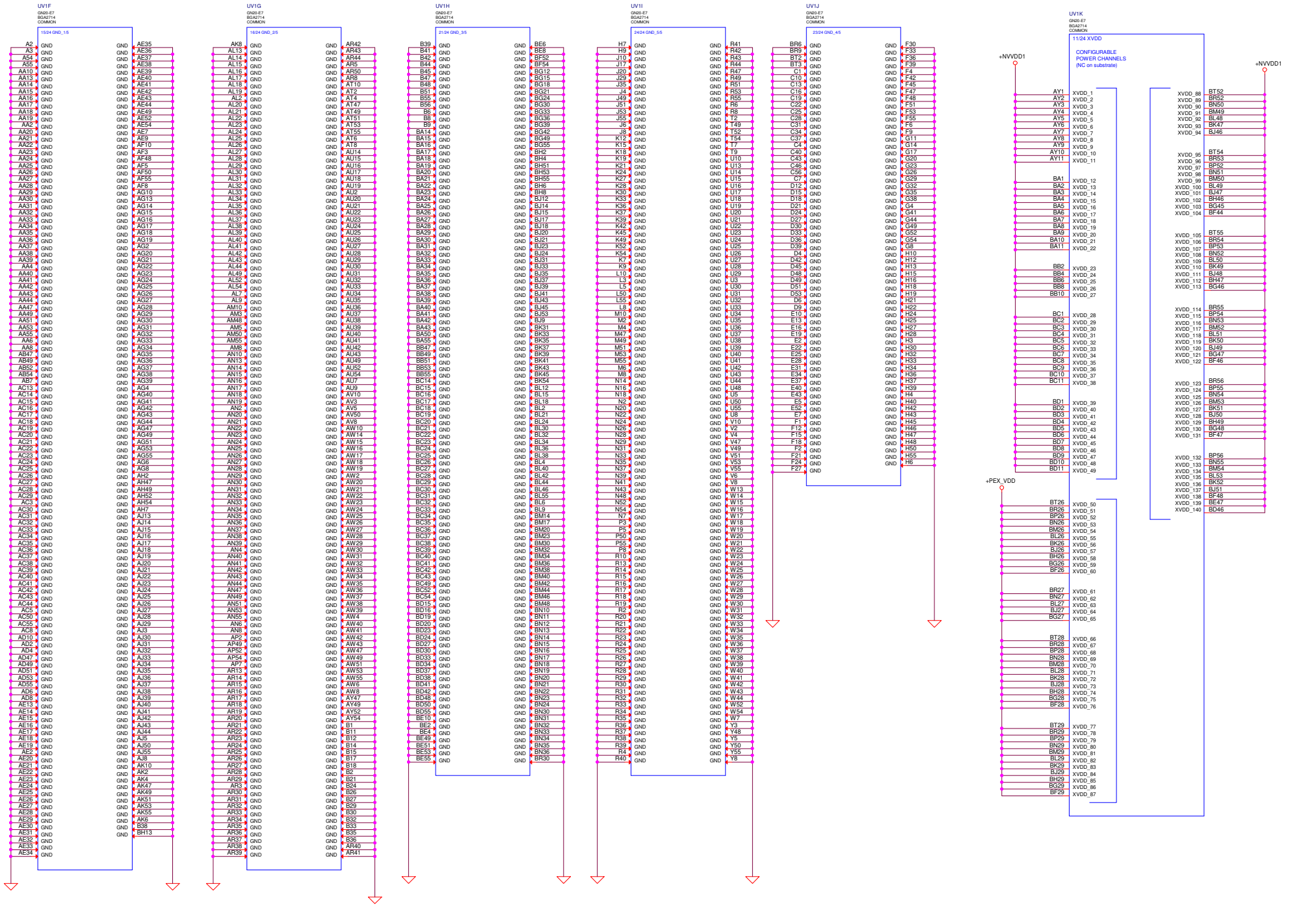
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: **GN20E DISP**

Size	Document Number	Rev
C	LA-K811P	1A

Date: Thursday, January 14, 2021 Sheet 29 of 112



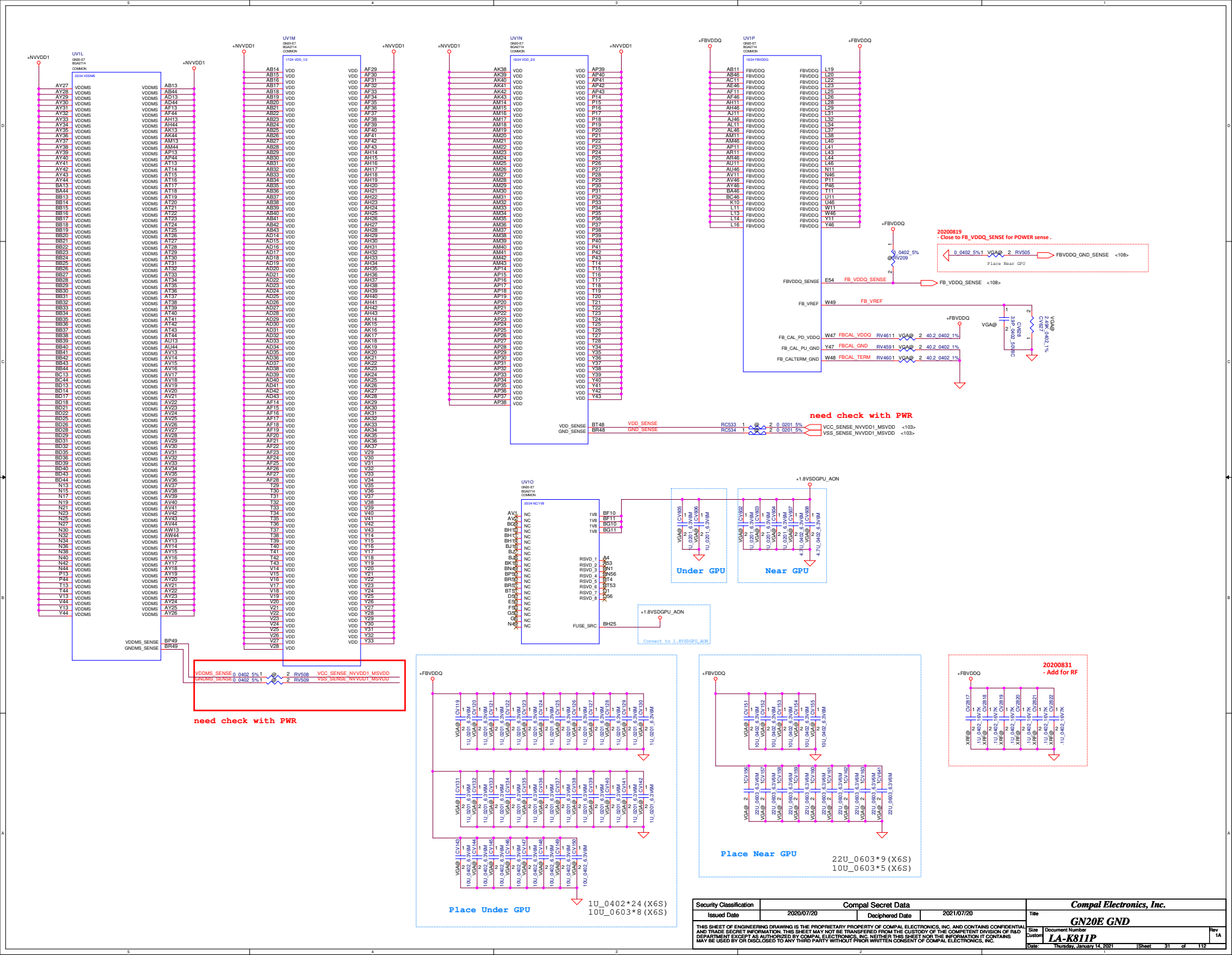
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: **GN20E PWR/GND**

Size	Document Number	Rev
C	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 30 of 112



Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

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Title	GN20E GND		
Size	Document Number		Rev
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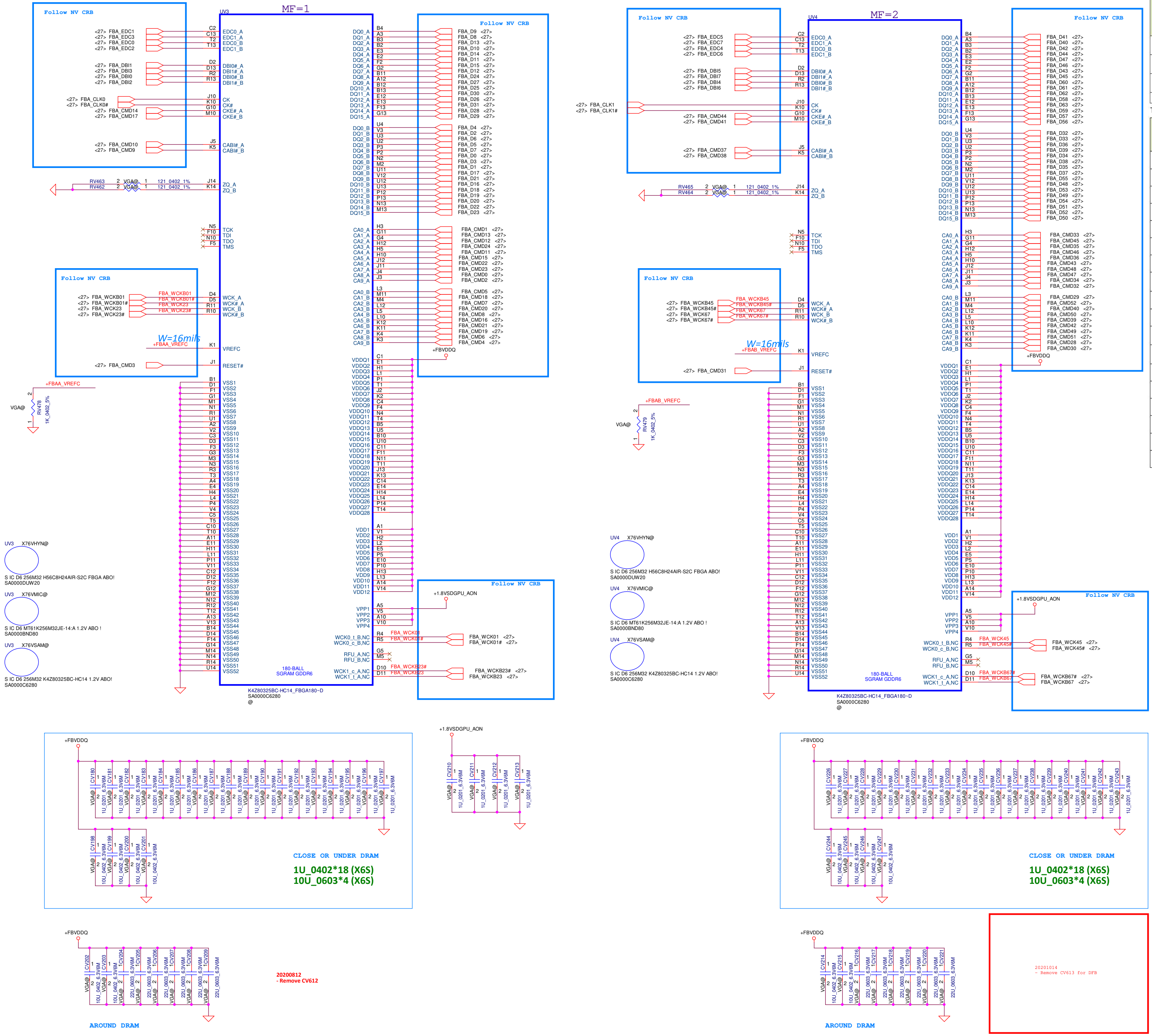

Table 6.4 GDDR6 Mode 3 Mapping, GB5-256

GB5-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB5-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0,1: CA8_A Bytes 2,3: -------	FBx_CMD28	Bytes 4,5: ------- Bytes 6,7: CA8_B
FBx_CMD1	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD29	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD2	Bytes 0-1: CA9_A Bytes 2,3: -------	FBx_CMD30	Bytes 4,5: ------- Bytes 6,7: CA9_B
FBx_CMD3	Bytes 0-3: RST*	FBx_CMD31	Bytes 4-7: RST*

Table 6.4 GDDR6 Mode 3 Mapping, GB5-256 (Continued)

GB5-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB5-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA9_B	FBx_CMD32	Bytes 4,5: CA9_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD33	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: ------- Bytes 2,3: CA8_B	FBx_CMD34	Bytes 4,5: CA8_A Bytes 6,7: -------
FBx_CMD7	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD35	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD8	Bytes 0,1: ------- Bytes 2,3: CA4_B	FBx_CMD36	Bytes 4,5: CA4_A Bytes 6,7: -------
FBx_CMD9	Bytes 0,1: ------- Bytes 2,3: CABI_B	FBx_CMD37	Bytes 4,5: CABI_A Bytes 6,7: -------
FBx_CMD10	Bytes 0,1: CABI_A Bytes 2,3: -------	FBx_CMD38	Bytes 4,5: ------- Bytes 6,7: CABI_B
FBx_CMD11	Bytes 0,1: CA4_A Bytes 2,3: -------	FBx_CMD39	Bytes 4,5: ------- Bytes 6,7: CA4_B
FBx_CMD12	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD40	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD13	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD41	Bytes 4,5: ------- Bytes 6,7: CKE_B
FBx_CMD14	Bytes 0,1: CKE_A Bytes 2,3: -------	FBx_CMD42	Bytes 4,5: ------- Bytes 6,7: CA5_B
FBx_CMD15	Bytes 0,1: CA5_A Bytes 2,3:-------	FBx_CMD43	Bytes 4,5: CA5_A Bytes 6,7: -------
FBx_CMD16	Bytes 0,1: ------- Bytes 2,3: CA5_B	FBx_CMD44	Bytes 4,5: CKE_A Bytes 6,7: -------
FBx_CMD17	Bytes 0,1: ------- Bytes 2,3: CKE_B	FBx_CMD45	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD18	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD46	Bytes 4,5: CA3_A Bytes 6,7: -------
FBx_CMD19	Bytes 0,1: ------- Bytes 2,3: CA7_B	FBx_CMD47	Bytes 4,5: CA7_A Bytes 6,7: -------
FBx_CMD20	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD48	Bytes 4,5: CA6_A Bytes 6,7: -------
FBx_CMD21	Bytes 0,1: ------- Bytes 2,3: CA6_B	FBx_CMD49	Bytes 4,5: ------- Bytes 6,7: CA6_B

Table 6.4 GDDR6 Mode 3 Mapping, GB5-256 (Continued)

GB5-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB5-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD22	Bytes 0,1: CA6_A Bytes 2,3: -------	FBx_CMD50	Bytes 4,5: ------- Bytes 6,7: CA3_B
FBx_CMD23	Bytes 0,1: CA7_A Bytes 2,3: -------	FBx_CMD51	Bytes 4,5: ------- Bytes 6,7: CA7_B
FBx_CMD24	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD52	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD25	Bytes 0,1: ------- Bytes 2,3: -------	FBx_CMD53	Bytes 4,5: ------- Bytes 6,7: -------
FBx_CMD26	Bytes 0,1: ------- Bytes 2,3: -------	FBx_CMD54	Bytes 4,5: ------- Bytes 6,7: -------
GB5-256	GPU FB Channel 0 & 1		
FBx_CMD27	DEBUG0[1]		
FBx_CMD55	DEBUG1[1]		

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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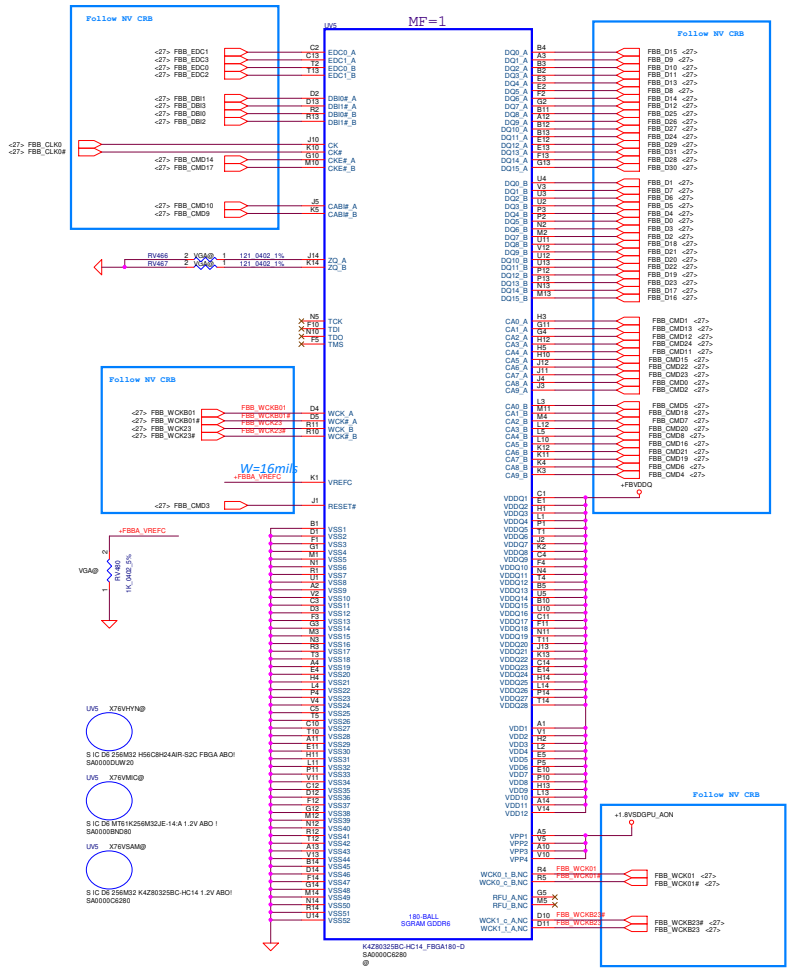
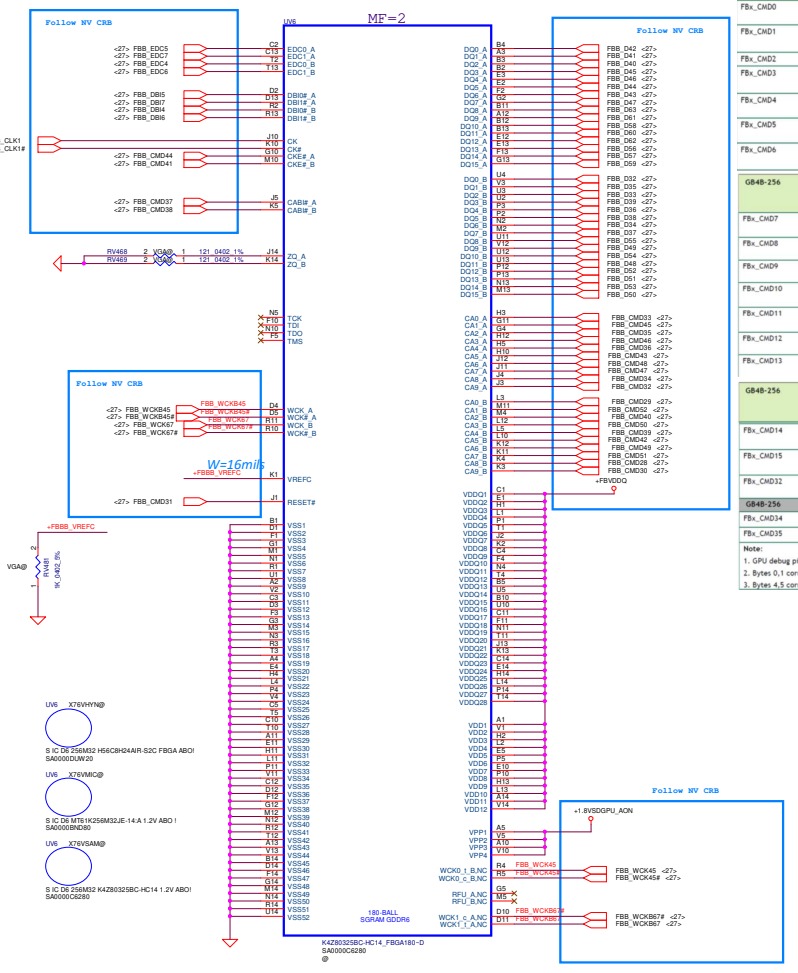
Issued Date	2020/07/20	Deciphered Date	2021/07/20	Title: GDDR6_A
				Size / Document Number: LA-K811P / Rev 1A
				Date: Thursday, January 14, 2021 / Sheet 32 of 112





GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 & 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: GDDR6_B

Size: | Document Number: LA-K811P | Rev: 1A

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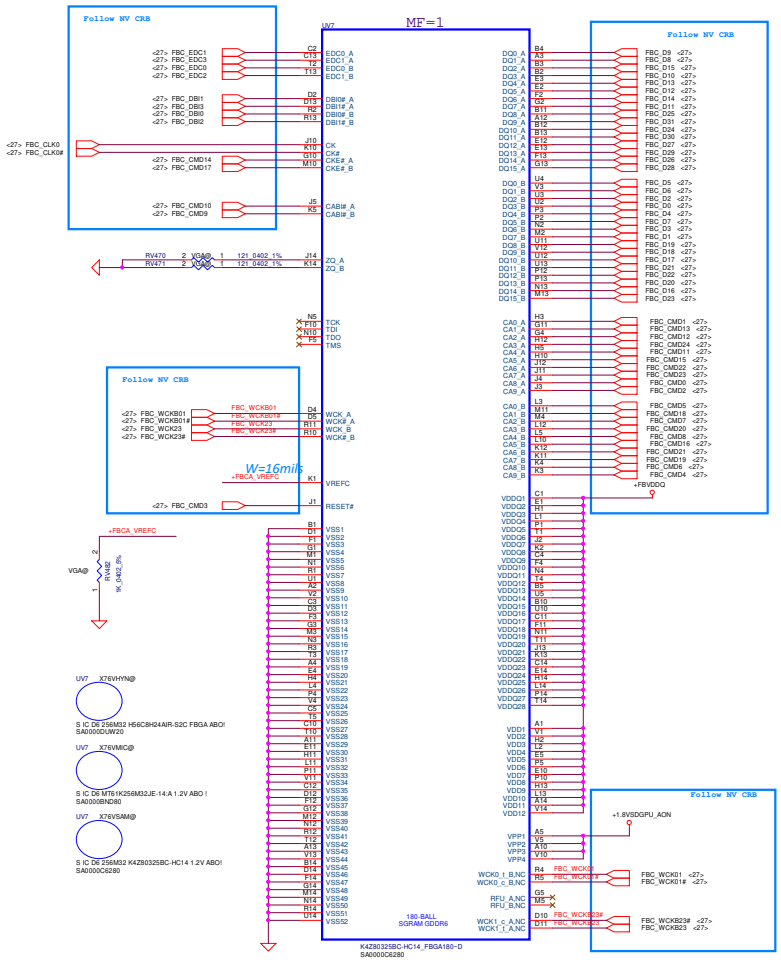
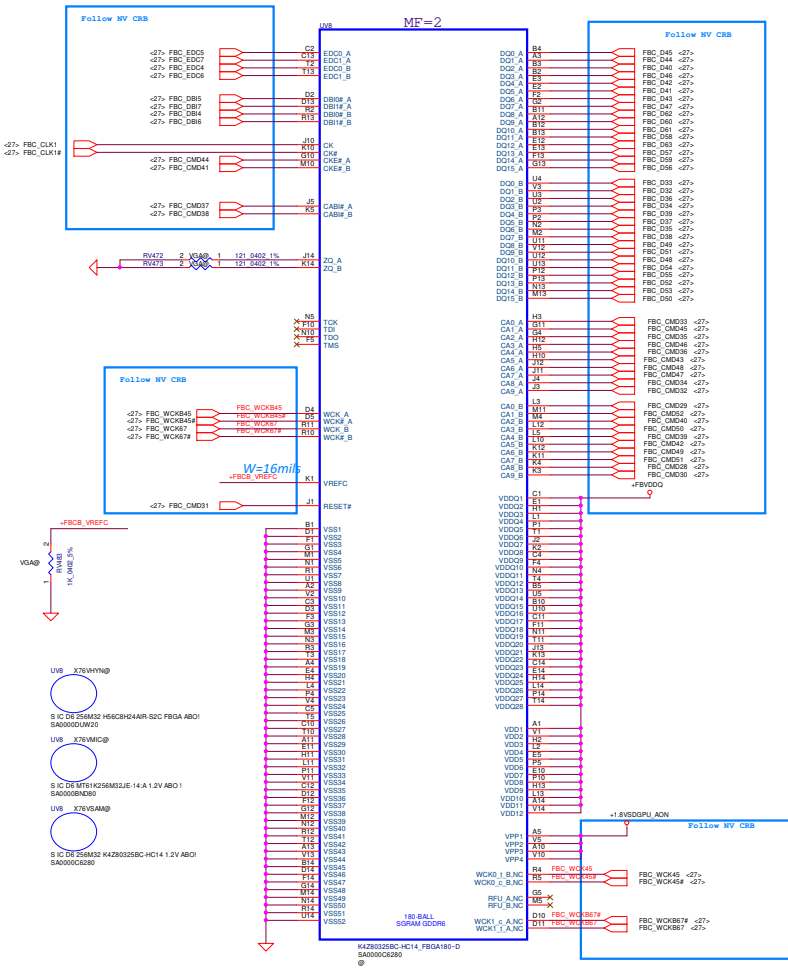




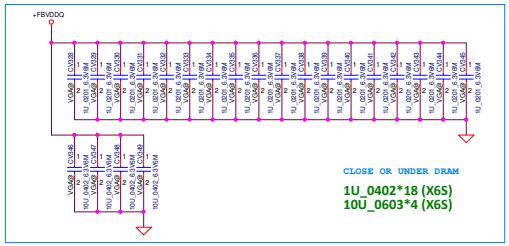
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CA8I_A Bytes 2,3: CA8I_B	FBx_CMD22	Bytes 4,5: CA8I_A Bytes 6,7: CA8I_B

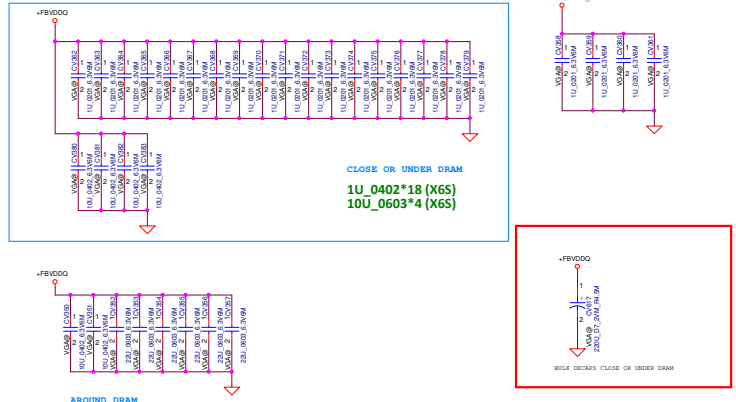
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE*_A Bytes 2,3: CKE*_B	FBx_CMD26	Bytes 4,5: CKE*_A Bytes 6,7: CKE*_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 & 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.





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Compal Electronics, Inc.

Title: GDDR6_C

Size: | Document Number: LA-K811P | Rev: 1A

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Remove VRAM channel D

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE*_A Bytes 2,3: CKE*_B	FBx_CMD26	Bytes 4,5: CKE*_A Bytes 6,7: CKE*_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B
GB4B-256	GPU FB Channel 0 & 1		
FBx_CMD34	DEBUG0[1]		
FBx_CMD35	DEBUG1[1]		

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: GDDR6_D

Size: | Document Number: LA-K811P | Rev: 1A

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20201130C

uPI_GEN2@ CV271 1000P_0402_50V7K SE074102K80

uPI_GEN2@ CV274 1000P_0402_50V7K SE074102K80

GEN2 ON-Semi no need BS_IN 1000pF Pull down

GEN2 UPI need 1000pF Pull down-->need check on 2021/01

GEN2 gain control by VBIOS

RV101 GEN2@ 0_0402_5% SD028000080

RV106 GEN2@ 0_0402_5% SD028000080

NV Suggest

*CV274/CV271 Keep NV suggest to unpop when GEN2.
PS:UPI-Semi suggest pop CV274/CV271 when GEN2.

CSSP_B+ — 75K_0402_1% GEN1@ 2 RV101 — PFM_CH1_BS_IN1

1000P_0402_50V7K 1 2 CV271 GEN1@ — 1 RV104 2 ON_GEN1@ 649_0402_1%

CSSP_FBVDD — 75K_0402_1% GEN1@ 2 RV106 — PFM_CH1_BS_IN2

1000P_0402_50V7K 1 2 CV274 GEN1@ — 1 RV108 2 ON_GEN1@ 649_0402_1%

RV114 0_0402_5% OVRM@ — RV115 0_0402_5% OVRM@

UV10

BS_IN1 BS_IN2 BS_IN3 BS_IN4 — PFM_CH1_BS_IN3 — PFM_CH1_BS_IN4

0_0402_5% 1 GEN2@ 2 RV118 — PFM_FILTER_GND_FET — GND_FET

RV122 1 2 475_0402_1% ON_GEN1@
RV123 1 2 475_0402_1% ON_GEN1@
RV124 1 2 169_0402_1%@
RV126 1 2 169_0402_1%@

SH_O1 IMON1 SH_O3 BG_REF_OUT — SH_O1 SH_O2 SH_O3 SH_O4

CV278 CV279 CV280 CV281 0.015U_0402_16V7K

RV123 uPI_GEN2@ 0_0402_5% SD028000080

NV Suggest no use IMON PIN
- uPI PD GND
- ON NC Floating

RV128 0_0402_5% 1 @ 2 PFM_ADC_MUX_SEL_R — MUX_SEL

PFM_ADC_FILTER_EN — ENABLE

PFM_SKIP_R — SKIP

PFM_ADC_FILTER_MODE — MODE_SEL

<26> GPIO22_ADC_MUX_SEL

NCP45492XMNTWG_QFN32_4X4 — SA0000CQX00 ON_GEN1@

VCC — PFM_CH1_SH_IN_P1 — SH_IN_P1 SH_IN_N1 SH_IN_P2 SH_IN_N2 SH_IN_P3 SH_IN_N3 SH_IN_P4 SH_IN_N4

ADC_IN_N <26>
ADC_IN_P <26>

DIFF_OUT_P DIFF_OUT_N — CV3088 47P_0402_50V8J — RV125 1 OVRM@ 2 0_0402_5% CV276 1 2 47P_0402_50V8J OVRM@

ADC_IN_N — PFM_PF_BSOR_R — RV127 1 OVRM@ 2 0_0402_5% CV277 1 2 47P_0402_50V8J OVRM@

BS_OK

NC NC NC NC — IMON2 BV_REF ADSR0 SYNC — TH1

RV130 0_0201_5% 1 GEN2@ 2

BG_REF_OUT BS_REF CM_REF_IN — PFM_BG_REF_OUT PFM_BS_REF

RV131 1 GEN1@ 2 0_0201_5%
RV134 1 GEN1@ 2 0_0201_5%

GND

RV132 1 2 243K_0402_1% ON_GEN1@ — PFM_BS_REF_R

RV135 1 GEN1@ 2 365K_0402_1%
RV194 1 GEN1@ 2 0_0402_5% PFM_CM_REF_IN_R

681K_0402_1% 2 GEN1@ 1 RV136

10K_0402_1% 1 OVRM@ 2 RV133

RV196 0_0201_5% uPI_GEN2@

NV Suggest no use IMON PIN
uPI PD GND
ON NC Floating

PFM_CM_REF_IN

PFM_BG_REF_OUT_R RV139 2 GEN2@ 1 0_0201_5% BG_REF_OUT

- RV139 NV Suggest POP when GEN2

20201130C

CV285 1000P_0402_50V7K OVRM@

CV4101 1000P_0402_50V7K @ — CV284 1000P_0402_50V7K GEN1@ — CV283 1000P_0402_50V7K OVRM@

NV Suggest

RV132 GEN2@ 31.6K_0402_1% SD034316280

RV132 uPI_GEN1@ 324K_0402_1% SD034324380

20201130C

RV132 @ 243K_0402_1% SD000004200

RV132 need check UPI GEN1 BOM option

OVR-M GEN1 BOM options based on GPU TGP

RV122 uPI_GEN1@ 357_0402_1% SD034357080

RV123 uPI_GEN1@ 357_0402_1% SD034357080

RV104 uPI_GEN1@ 487_0402_1% SD00000EL80

RV108 uPI_GEN1@ 487_0402_1% SD00000EL80

20201130C

20201130
- Remove RV193

OVR-M GEN1/GEN2 IC Part number

UV10 uPI_GEN1@ — S IC US5650QQKI WQFN 32P POWER MONITOR — SA0000CMA00

UV10 ON_GEN2@ — S IC NCP45495XMNTWG QFN 32P MONITOR — SA0000DUX00

UV10 uPI_GEN2@ — S IC US5651AQKI WQFN 32P POWER MONITOR — SA0000DY100

For OVRM Keep ON

+3V_OVRM — OVRM@ RV178 0_0402_5% — +3VS

OVRM@ CV272 0.1U_0201_10V6K

20201130C
- RV1935/RV1936 Reserved FOR UPI GEN2
- Must be pop for GEN1 & GEN2 Solution

RV1935 2 OVRM@1 0_0402_5% — 100_0402_1% GEN1@ 2 RV103 CSSP_B+ — CSSP_B+ <104>

ON_GEN2@ CV273 680P_0402_50V7K — uPI_GEN2@ CV273 0.1U 25V K X7R 0402 SE00000W210 20201130C

0_0402_5% 2 GEN1@ 1 RV105 — CSSN_B+ — CSSN_B+ <104>

RV1936 2 OVRM@1 0_0402_5% — 100_0402_1% GEN1@ 2 RV109 CSSP_FBVDD — CSSP_FBVDD <104>

ON_GEN2@ CV275 680P_0402_50V7K — uPI_GEN2@ CV275 0.1U 25V K X7R 0402 SE00000W210 20201130C

0_0402_5% 2 GEN1@ 1 RV116 — CSSN_FBVDD — CSSN_FBVDD <104>

GEN2 gain control by VBIOS

uPI_GEN2@ RV105 51 +-5% 0402 SD028510A80
uPI_GEN2@ RV116 51 +-5% 0402 SD028510A80
uPI_GEN2@ RV103 51 +-5% 0402 SD028510A80
uPI_GEN2@ RV109 51 +-5% 0402 SD028510A80

ON_GEN2@ RV105 0 +-5% 0402 SD028000080
ON_GEN2@ RV116 0 +-5% 0402 SD028000080
ON_GEN2@ RV103 0 +-5% 0402 SD028000080
ON_GEN2@ RV109 0 +-5% 0402 SD028000080

GEN2 NV suggest BS_IN3,4 need also connect with BS_IN2(CSSP_FBVDD)
No use SH_P/N need PU the same voltage as no use BS_IN

+3V_OVRM — GEN1@ RV1933 0_0402_5%

RV1922 GEN2@ 1 0_0402_5% CSSP_FBVDD

RV1937 2 @ 1 0_0402_5%

GEN1@ 2K_0402_5% RV110 — RV111 — RV112 — RV113

PFM_CH1_SH_IN_P3
PFM_CH1_SH_IN_N3
SNN_PFM_CH1_SH_IN_P4
SNN_PFM_CH1_SH_IN_N4

RV110 GEN2@ 0_0402_5% SD028000080
RV111 GEN2@ 0_0402_5% SD028000080
RV112 GEN2@ 0_0402_5% SD028000080
RV113 GEN2@ 0_0402_5% SD028000080

+3V_OVRM — RV148 10K_0201_5% GEN2@ — ADSR0 — RV149 10K_0201_5% @

+3V_OVRM — RV147 10K_0201_5% @ — PFM_CM_REF_IN — RV150 10K_0201_5% GEN2@

ADSR0(Pin21) ADSR1(Pin22,PFM_CM_REF_IN)

Pin23 : I2C_CLK(PFM_BG_REF_OUT)
Pin24 : I2C_DATA(PFM_BS_REF)

ON-SEMI Suggest need add RC filter.

+3V_OVRM — RV159 10K_0402_1% OVRM@ — PFM_PF_BSOK_R — RV198 24.9K_0402_1% ON_GEN2@ — CV2813 1U_0201_6.3V6M ON_GEN2@

<26> VGA_I2CC_SCL — RV531 1 GEN2@ 2 0_0201_5% — VGA_I2CC_SCL_OVRM — RV129 2 GEN2@ 10_0402_5% — PFM_BG_REF_OUT

<26> VGA_I2CC_SDA — RV532 1 GEN2@ 2 0_0201_5% — VGA_I2CC_SDA_OVRM — RV144 2 GEN2@ 10_0402_5% — PFM_BS_REF

<26,103> VGA_I2CC_SCL_PWR — RV203 1 @ 2 0_0201_5%

<26,103> VGA_I2CC_SDA_PWR — RV202 1 @ 2 0_0201_5%

Follow NV CRB, OVRM/PWR IC use same I2C power rail.

Table 3.6 OVR-M GEN1 BOM options based on GPU TGP

GPU Maximum TGP (W)1	Rsense (mohm)	Follow schematic UPI SH_IN R1	SH_IN R3, R4	SH_O R21 RV122	SH_O R25 RV123	BUS PU RV101 RV106 R22, R27	BUS PD RV104 RV108 R23, R26	Bg_ref_o R17 RV132	Follow Schematic OnSemi SH_IN R1	SH_IN R3, R4	SH_O R21 RV122	SH_O R25 RV123	BUS PU RV101 RV106 R22, R27	BUS PD RV104 RV108 R23, R26	Bg_ref_o R17 RV132
35-79	5	100Ω	49.9Ω	357Ω	357Ω	75KΩ	487Ω	324KΩ	100Ω	49.9Ω	475Ω	475Ω	75KΩ	649Ω	243KΩ
80-99	5	100Ω	49.9Ω	255Ω	475Ω	75KΩ	499Ω	316KΩ	100Ω	49.9Ω	340Ω	634Ω	75KΩ	665Ω	237KΩ
100-170+	5	100Ω	49.9Ω	196Ω	475Ω	75KΩ	499Ω	316KΩ	100Ω	49.9Ω	261Ω	634Ω	75KΩ	665Ω	237KΩ

Note: 1.GPU Maximum TGP (W)= Baseline TGP (W) + Configurable TGP Mode 2 (W) + Dynamic Boost 2.0 Maximum Power (W).
Contact NVIDIA Application Engineering for VBIOS with OVR-M Gen 1 BOM configuration.

+3V_OVRM — RV151 10K_0201_5% @ — PFM_ADC_FILTER_MODE — RV156 10K_0201_5% @

+3V_OVRM — RV152 1K_0402_1% GEN1@ — PFM_SKIP_R — RV199 30.1K_0402_1% @

NV Suggest RV152 GEN2@ 10K_0402_1% SD034100280

+3V_OVRM — RV141 10K_0201_5% @ — PFM_ADC_FILTER_EN — RV145 10K_0201_5% OVRM@

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Compal Electronics, Inc.

Title: OVRM-GEN1&2

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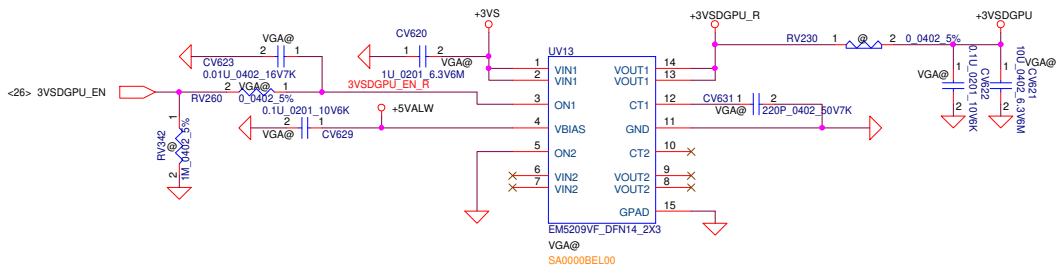
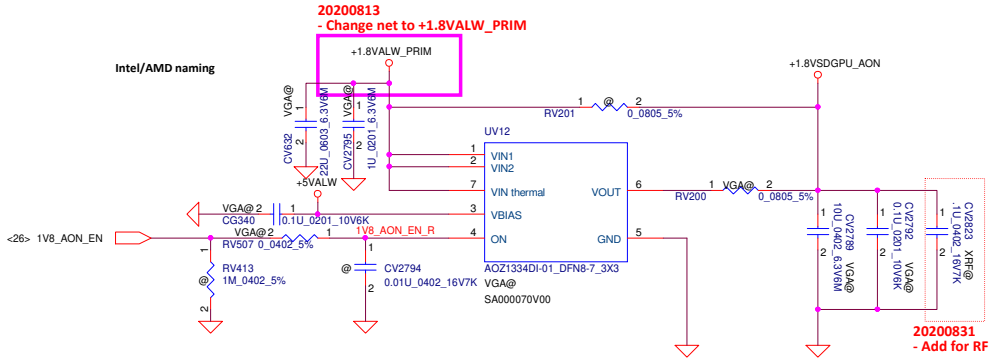
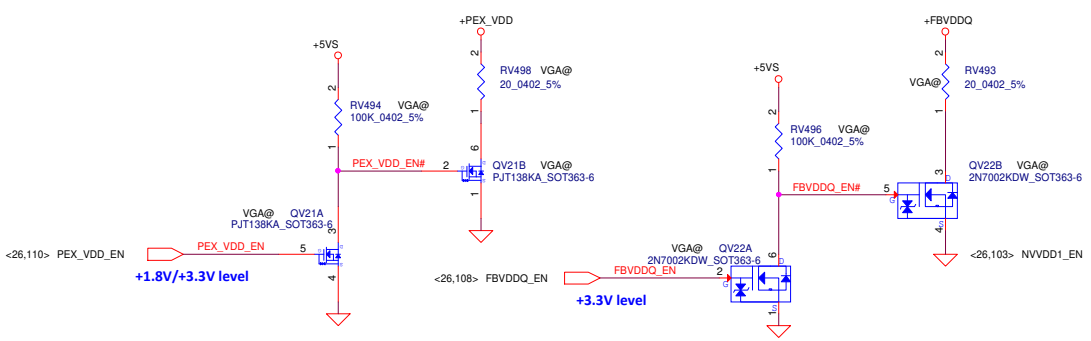




For Power down sequence



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Title: GN20E-GPU Power control

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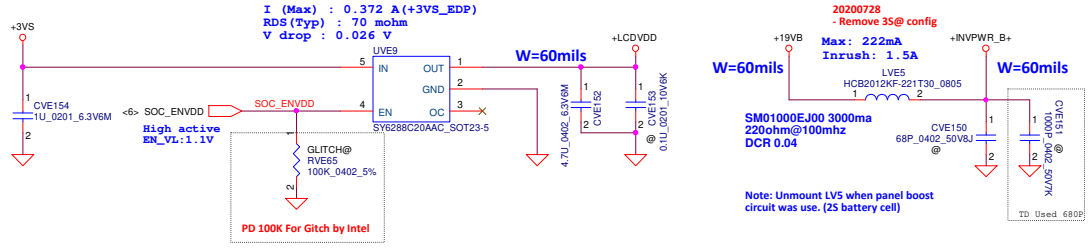
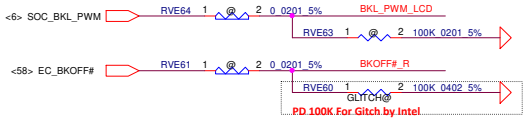
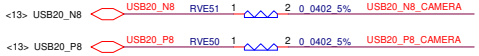
LCD POWER CIRCUIT



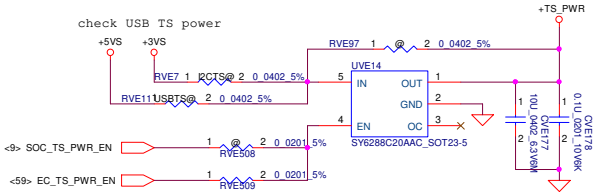
LCD enable signal



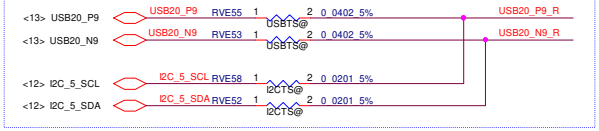
Camera

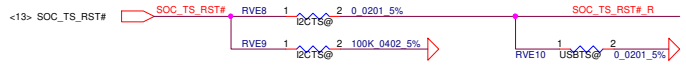


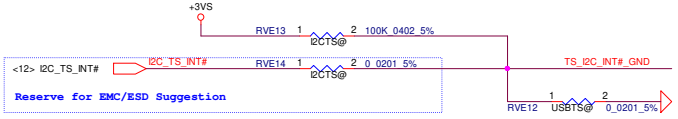
USB/I2C Touch Screen Co-Lay

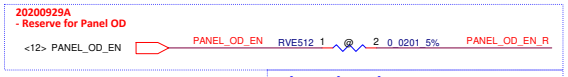


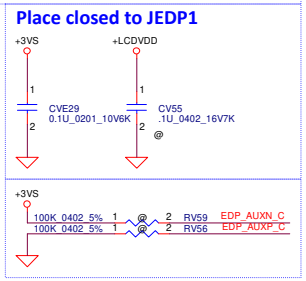
I2C / USB Touch co-lay

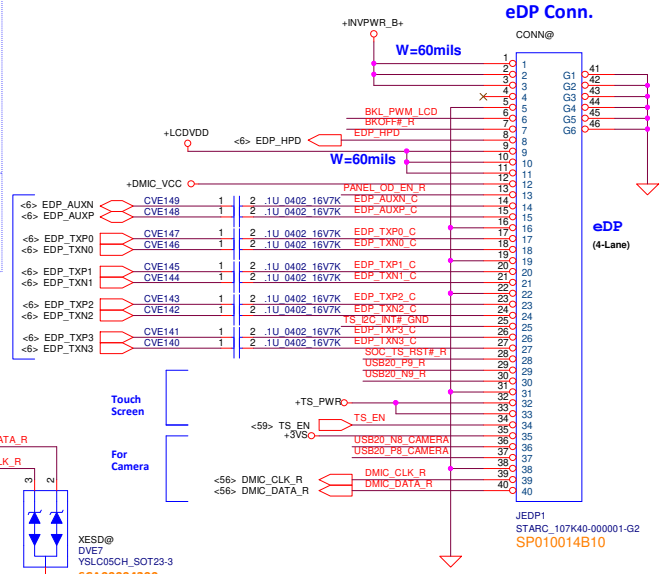


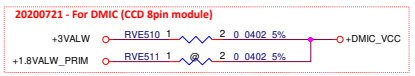


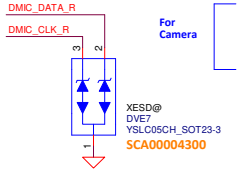












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Compal Electronics, Inc.			
Title	eDP / DMIC / IR Camera / Touch		
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HDMI

*Vout = 0.8 * ((3.83K+10K)/10K) = 1.1064V

20200826
- DVH2/DVH3 PN change to SC300005D00

SC300005D00

SC300001G00

20200807
- Re-NAME to HDMI function

*SCL/SDA can 3V3 or 1V8
20200810 (For VENDER Review)
- pop RVH11/RVH13/RVH32/RVH33

20200929A for HPD
- unpop RVH12
- Add RVH34

Placed close to REXT pin.

20200807
- For Vender debug

HDP Deterct

20200724
- Change to SOC_DP2_HPD
20200807
- HPD Re-Name to SOC_HDMI_HPD

Intel/AMD naming

20200929A
- pop RVH19/QVH1 for HPD
- Add RVH35

RY11 design guide rev2.0
use 20K pull down.

20200810 (For VENDER Review)
- unpop QVH1A/RVH19
- Pop RVH24

DDC (Reserved)

20200819
- unpop RVH20/RVH21 for Vender review

3ohm/10pF

20200807
- Re-NAME to HDMI function

EQ

EQ
L0: Pull down with 1k,
EQ=8dB
L1: Pull down with 20k
EQ=7dB
L2: Floating
EQ=5dB
L3: Pull up with 20k
EQ=3dB
L4:Pull up with 1k
EQ=1dB

I2C ADDR
L: 0x10 - 0x2F (Default)
M: 0x30 - 0x4F
H: 0x90 - 0x9f and 0xD0 - 0xDF

DC IN
L: TMDS input is AC Coupled
H: TMDS input is DC Coupled

20200806
- Change footprint to ACON_HMRB4-AK1L0C_19P

HDMI connector

DC232000Y00

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Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: HDMI CONN. (PS8419)

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Reserve Page

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Compal Electronics, Inc.		
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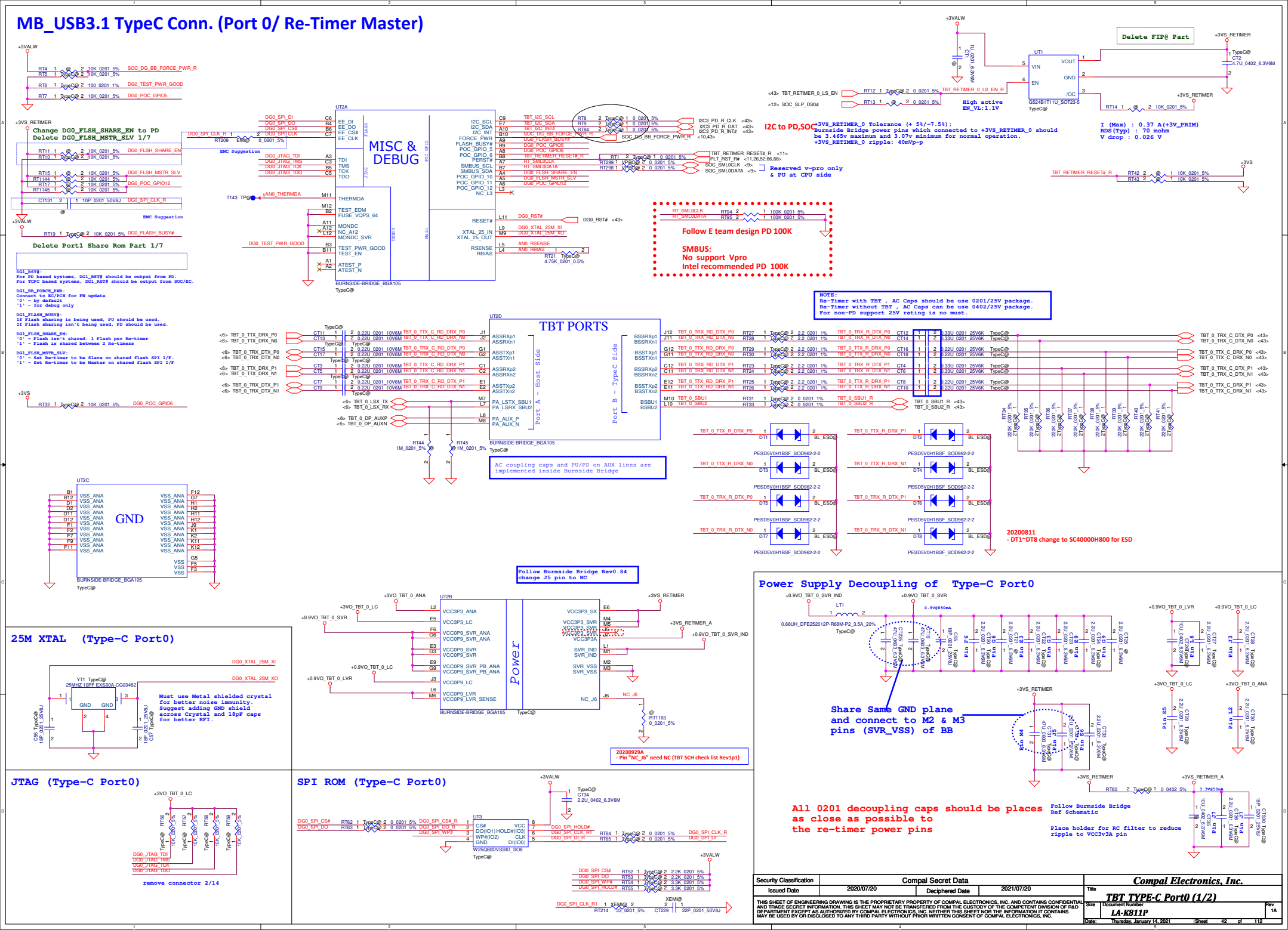
Reserve Page

MB_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)



25M XTAL (Type-C Port0)

JTAG (Type-C Port0)

SPI ROM (Type-C Port0)

Power Supply Decoupling of Type-C Port0

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.	
Title	TBT TYPE-C Port0 (1/2)
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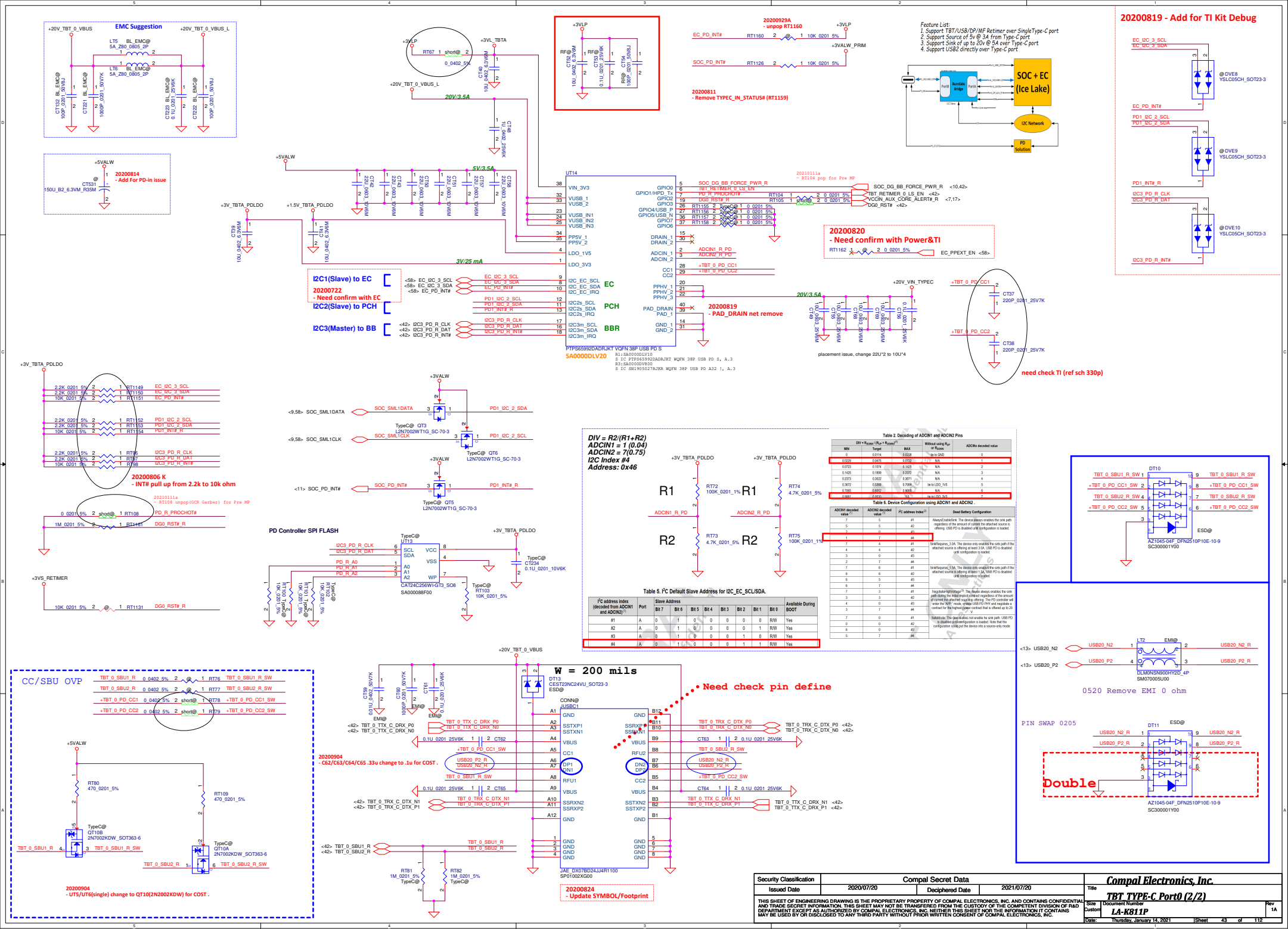

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Title: **TBT TYPE-C Port0 (2/2)**

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Compal Electronics, Inc.

Title: **Reserve_TYPE-C**

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Compal Electronics, Inc.

Title: *Reserve_TYPE-C*

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Compal Electronics, Inc.

Title: *Reserve_TYPE-C*

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Compal Electronics, Inc.

Title: *Reserve_TYPE-C*

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Compal Electronics, Inc.

Title: *Reserve_TYPE-C*

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MB_USB3.1 TypeC Conn. (Power Path)
- Remove
- TBT4 Change to TI solution

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ***TYPE-C Power Path***

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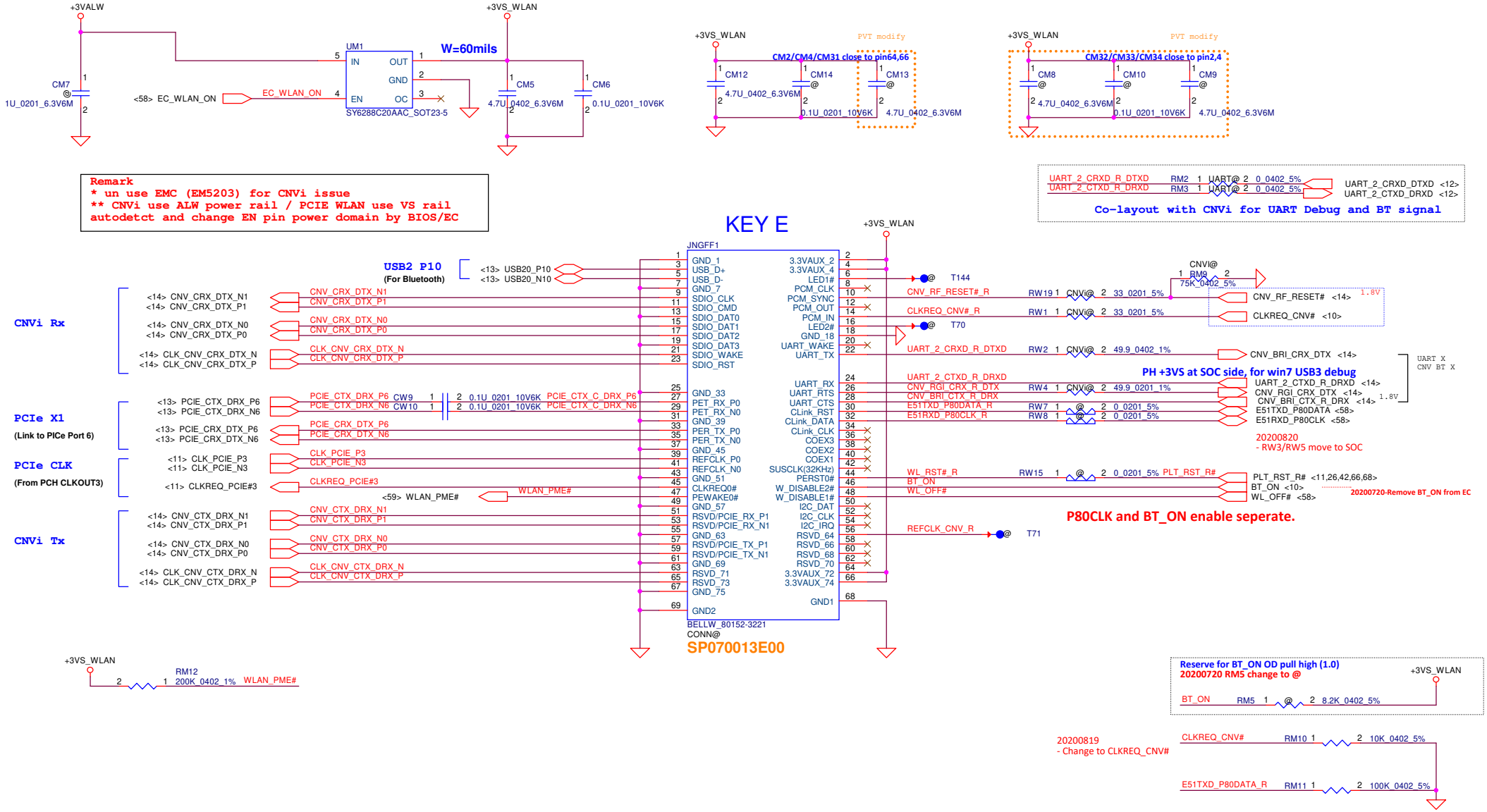
NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: NGFF WL(KEY E) / WWAN(KRY B)			
Size	Document Number: LA-K811P		Rev: 1A
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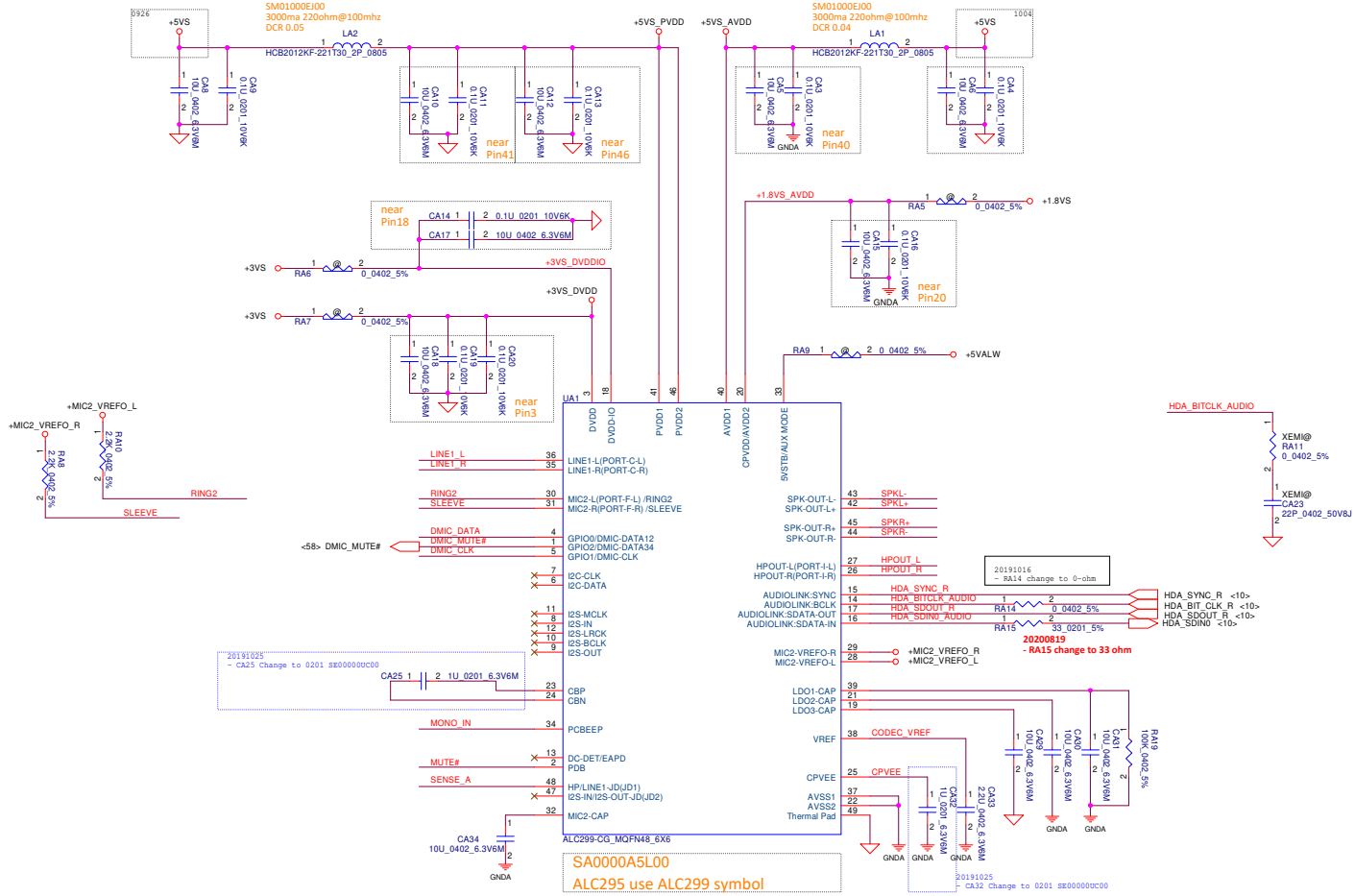
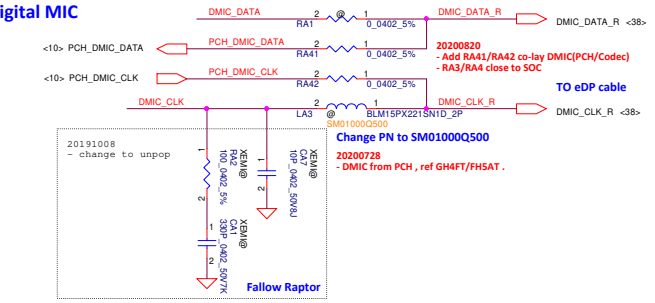
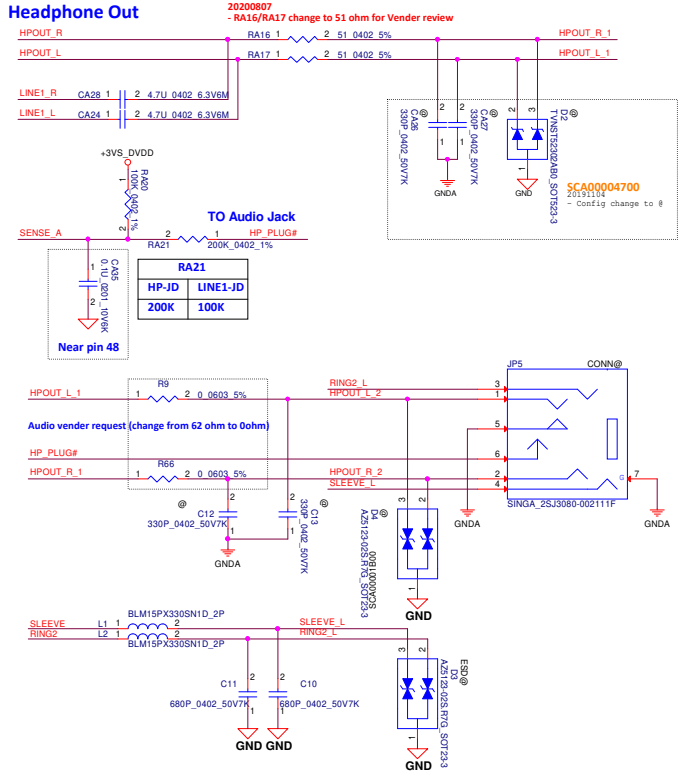
AUDIO CODEC ALC295



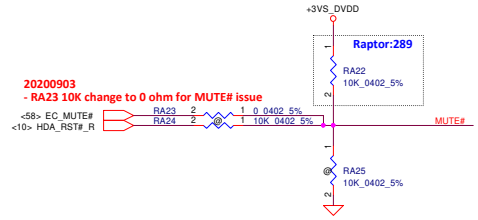
Digital MIC



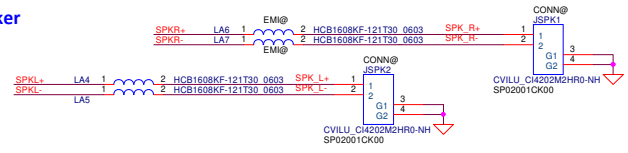
Headphone Out



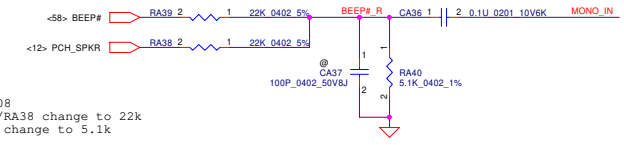
MUTE#



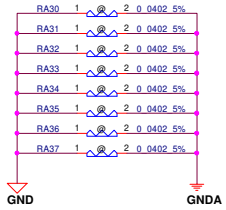
Speaker



BEEP



20191008
- RA39/RA38 change to 22k
- RA40 change to 5.1k



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Compal Electronics, Inc.			
Title: Audio Code ALC295			
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Compal Electronics, Inc.		
Title: *Audio-Reserve*		
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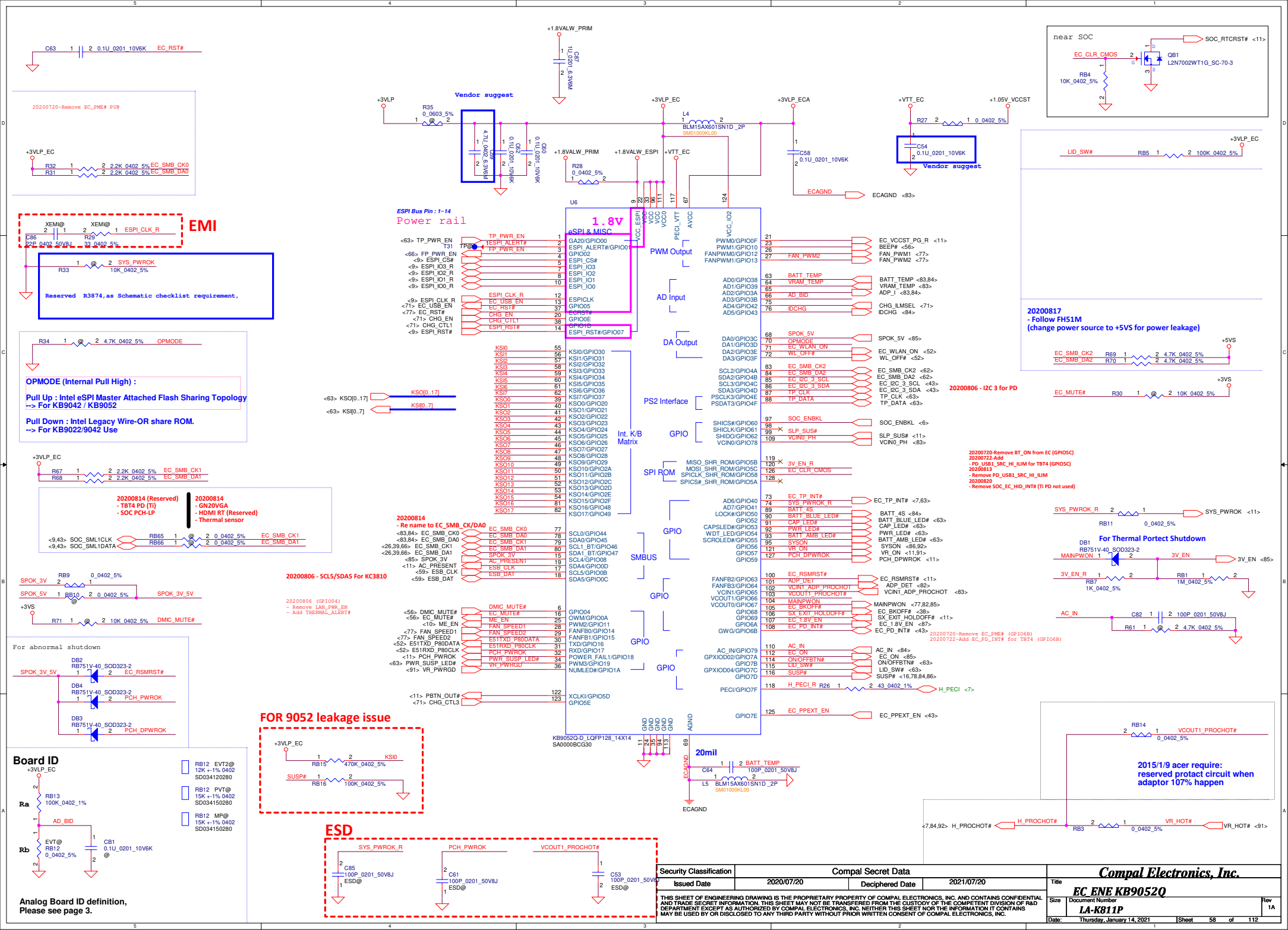

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **EC_ENE KB9052Q**

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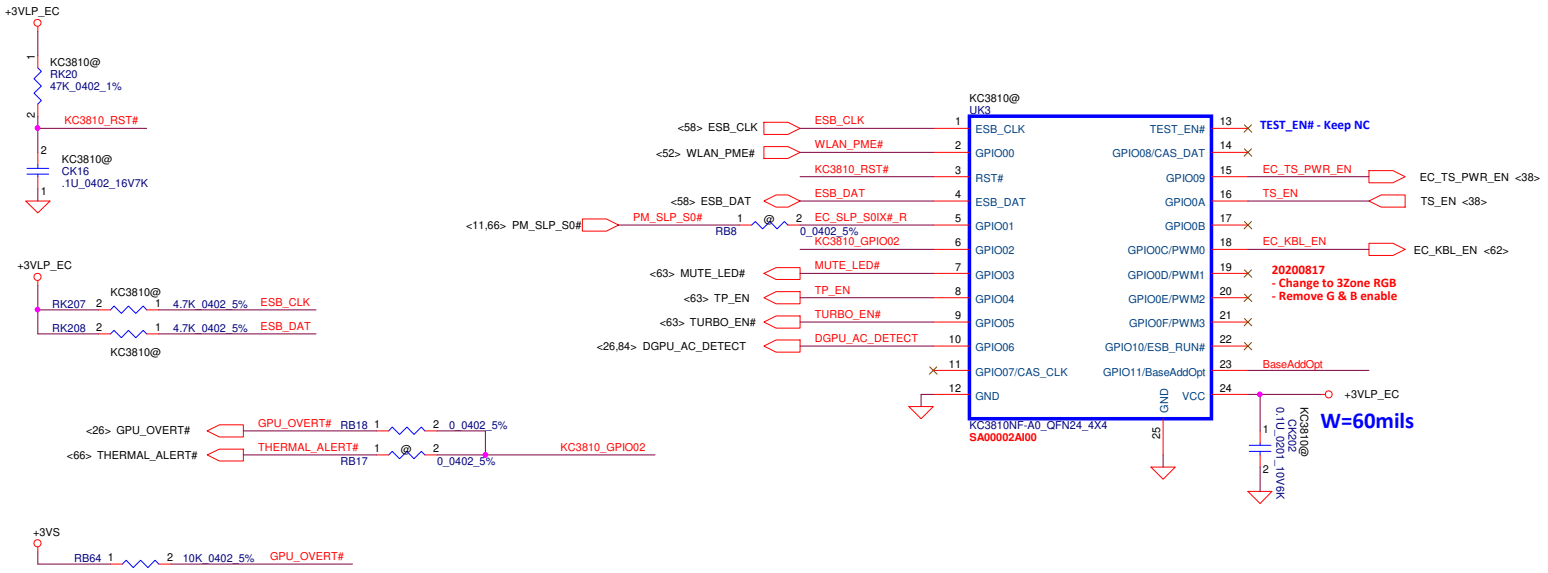
OMEN New ESB CLK&DAT for Extend I/O

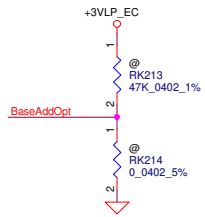
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.



Need EC confirm

[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and the other keep NC or initial High

- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08



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Compal Electronics, Inc.

Title: **Extend I/O KC3810**

Size: Document Number: **LA-K811P** Rev: 1A

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Compal Electronics, Inc.

Title: **Reserve for Secure & Reset IC**

Size	Document Number	Rev
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Compal Electronics, Inc.

Title: **Reserve for SMB/I2C Block Diagrams**

Size	Document Number	Rev
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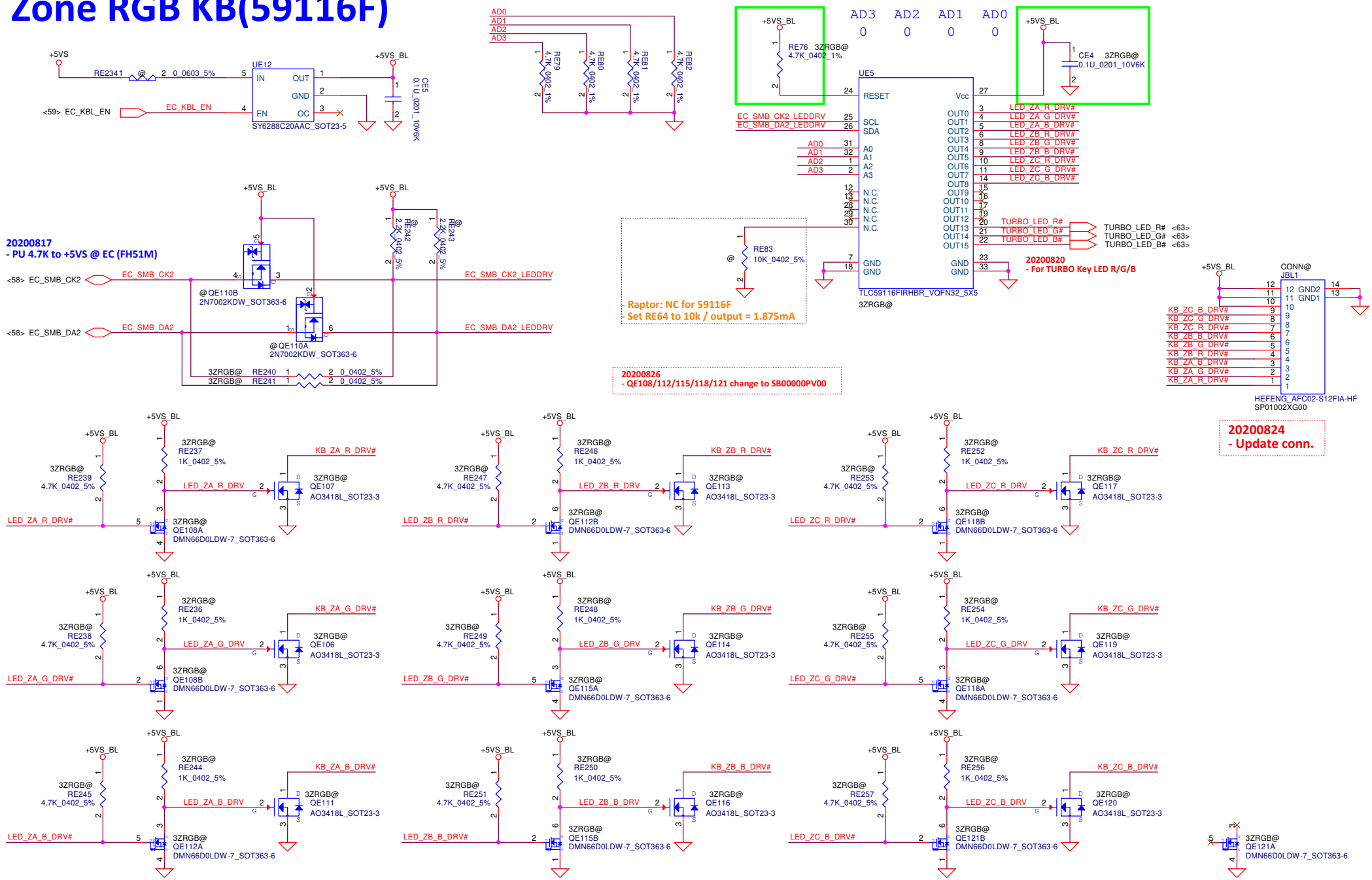
3 Zone RGB KB(59116F)



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Compal Electronics, Inc.			
Title: 3 Zone RGB KB(59116F)			
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KB Conn. 32pin

DVT: remove SWK1 switch button

ON/OFF BTN

<59> MUTE_LED#
<58> CAP_LED#
MUTE_LED#
CAP_LED#

<58> KSI[0..7]
KSI[0..7]
<58> KSO[0..17]
KSO[0..17]

RK6 100K_0402_5%
+3VLP
<58> ON/OFFBTN#
ON/OFFBTN#
SW1 EVT@ TJG-533-V-T/R_6P

20200811
- For EVT TEST

MUTE_LED# RK210 0_0402_5% MUTE_LED#_R
CAP_LED# RK211 0_0402_5% CAP_LED#_R
+3VS

20200804
- Update Footprint

CONN@ JKB1
KSO16 KSO17 KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
ON/OFFBTN#
ACES_51519-03201-001
SP01001RH00

KB BackLight (1 Zone RGB) 6pin

20200817
- Remove

Lid Switch

+3VLP
UG115 APX8132AI_TSOT-23-3
VDD OUT GND
LID_SW# LID_SW# <58>
CG2 .1U_0402_16V7K
CG1 .1U_0402_16V7K

TP/B Conn.

+3VALW
+3VS RK11 0_0402_5%
+3V_PTP
UK2 SY6288C20AAC_SOT23-5
IN OUT GND EN OC
CK4 1U_0201_6.3V6M
CK5 4.7U_0402_6.3V6M
TP_PWR_EN <58>

TP_PWR_EN follow SYSON behavior

EC PS2
PCH I2C
<7,58> EC_TP_INT#
<59> TP_EN
@ CK2 0.1U_0201_10V6K
JTP1
TP_CLK TP_DATA
I2C_3_SDA_R I2C_3_SCL_R EC_TP_INT# TP_EN
CK6 680P_0402_50V7K ESD@
GND GND
HEFEN_AFA02-S08FIA-2H CONN@
SP01002PE00

+3V_PTP
RK1 10K_0402_5%
EC_TP_INT#

+3V_PTP +3V_PTP
QK1B 2N7002KDW_SOT363-6
RK10 2.2K_0402_5%
RK7 2.2K_0402_5%
<12> I2C_3_SCL
I2C_3_SCL_R
RK9 0_0402_5%
QK1A 2N7002KDW_SOT363-6
<12> I2C_3_SDA
I2C_3_SDA_R
RK8 0_0402_5%

+3V_PTP
RK3 4.7K_0402_5%
RK2 4.7K_0402_5%
<58> TP_CLK
<58> TP_DATA
TP_CLK
TP_DATA

Battery LED

<58> BATT_AMB_LED#
BATT_AMB_LED#
RG4 1K_0402_5%
LED1
+5VALW
<58> BATT_BLUE_LED#
BATT_BLUE_LED#
RG6 560_0402_5%
LTST-C295TBKF-CA_AMBER-BLUE

Power LED

<58> PWR_SUSP_LED#
PWR_SUSP_LED#
RG11 1K_0402_5%
LED2
+5VALW
<58> PWR_LED#
PWR_LED#
RG10 560_0402_5%
LTST-C295TBKF-CA_AMBER-BLUE

Turbo Key

20200810
- Add D7 for ESD
20200820
- Add D8 for ESD

<62> TURBO_LED_G#
<62> TURBO_LED_B#
TURBO_LED_G# TURBO_LED_B# RG12 1K_0402_5%

Reserved for placement

TURBO_LED_R#
TURBO_EN#
D7 AZ5123-02S.R7G_SOT23-3 ESD@
TURBO_LED_G#
TURBO_LED_B#
D8 AZ5123-02S.R7G_SOT23-3 ESD@

+3VALW
R72 10K_0402_5%
+5VALW
CONN@ JTRB1
<59> TURBO_EN#
<62> TURBO_LED_R#
TURBO_EN#
TURBO_LED_R#
G1 G2
ACES_51570-00401-P02
SP01002LF00

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Compal Electronics, Inc.

Title: KB/TP/LED/LID

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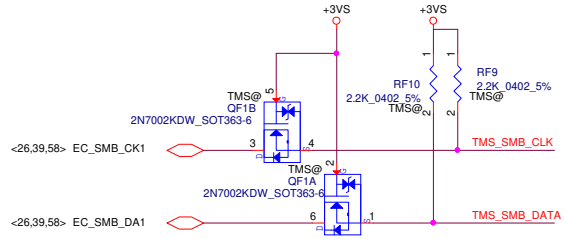
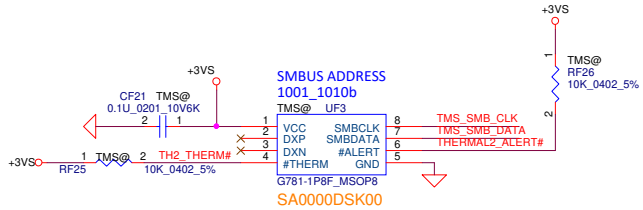
20200717
- Remove G-Sensor

THERMAL SENSOR

20200810
- Check address



Close to Thermal SKIN

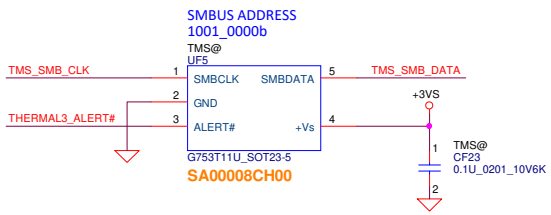


SA0000DSK00

20200929A
- change to SA0000DSK00 (S IC G788-1P81U MSOP 8P TEMP.SENSOR)

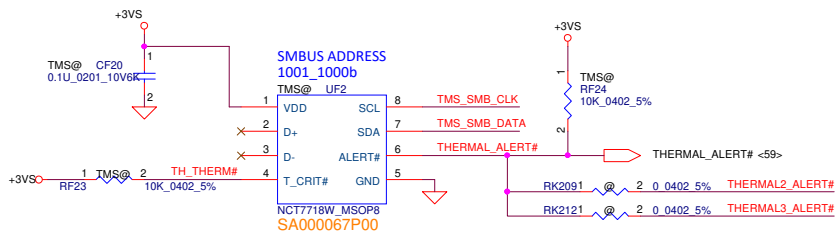
Close XXXX

20200810
- Add For Thermal solution



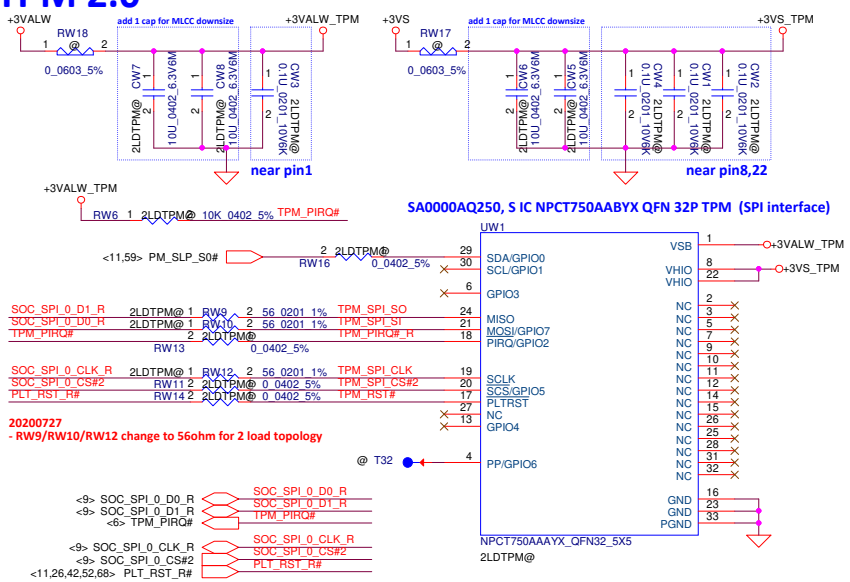
SA00008CH00

Close to SO-DIMM



SA000067P00

TPM 2.0

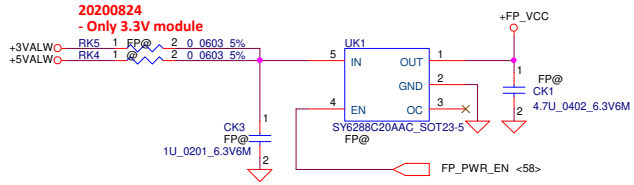


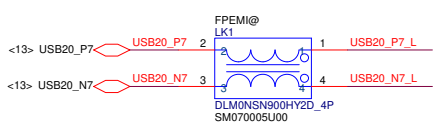
20200727
- RW9/RW10/RW12 change to 56ohm for 2 load topology

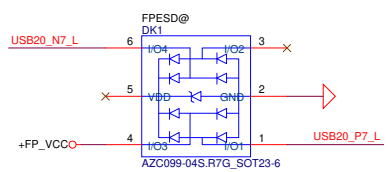
20200819
- BIOS change to 32M , Remove TPM3LD@

Finger print

20200824
- Only 3.3V module

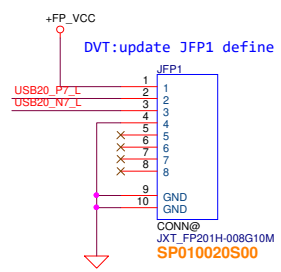






PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



SP010020S00

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Compal Electronics, Inc.

Title: TPM/FP/Sensor

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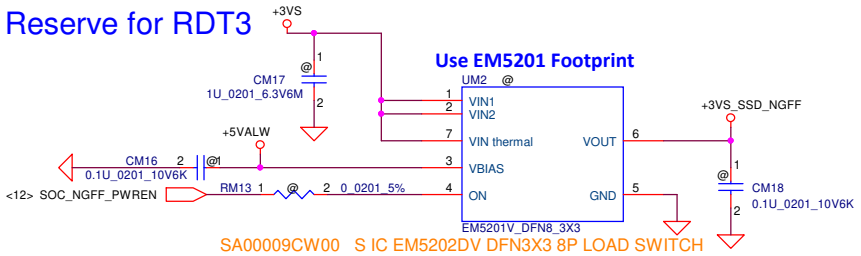
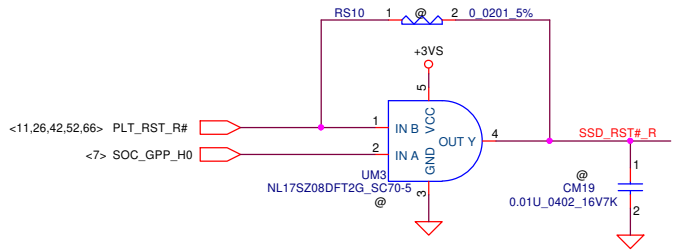
M.2 PCIE/SATA SSD

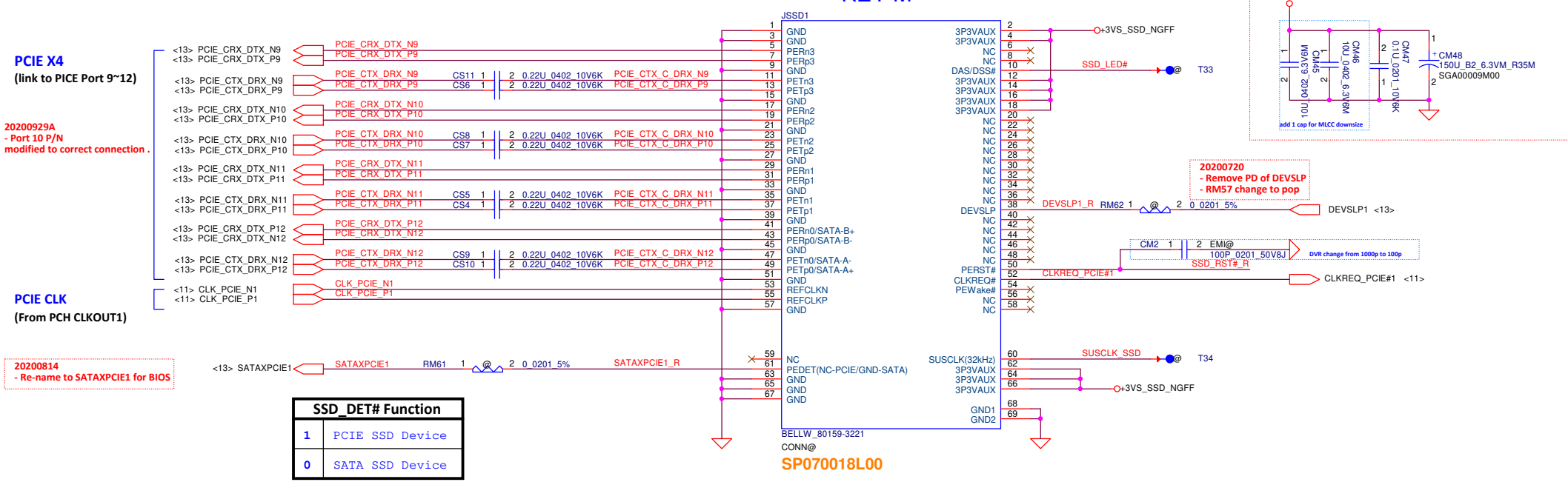
20200826
- SSD Power SCH move to P.78
- +3VS_SSD_NGFF

Reserve for RDT3





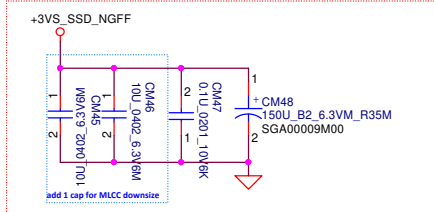
KEY M



20200929A
- Port 10 P/N
modified to correct connection .

20200814
- Re-name to SATAXPCIE1 for BIOS

20200903
- Add for M.2 SSD Power



20200720
- Remove PD of DEVSLP
- RM57 change to pop

CM2 EMI@ 100P_0201_50V8J
DVR change from 1000p to 100p
SSD_RST#_R

SSD_DET# Function	
1	PCIE SSD Device
0	SATA SSD Device

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Compal Electronics, Inc.			
Title: NGFF SSD(KEY M)			
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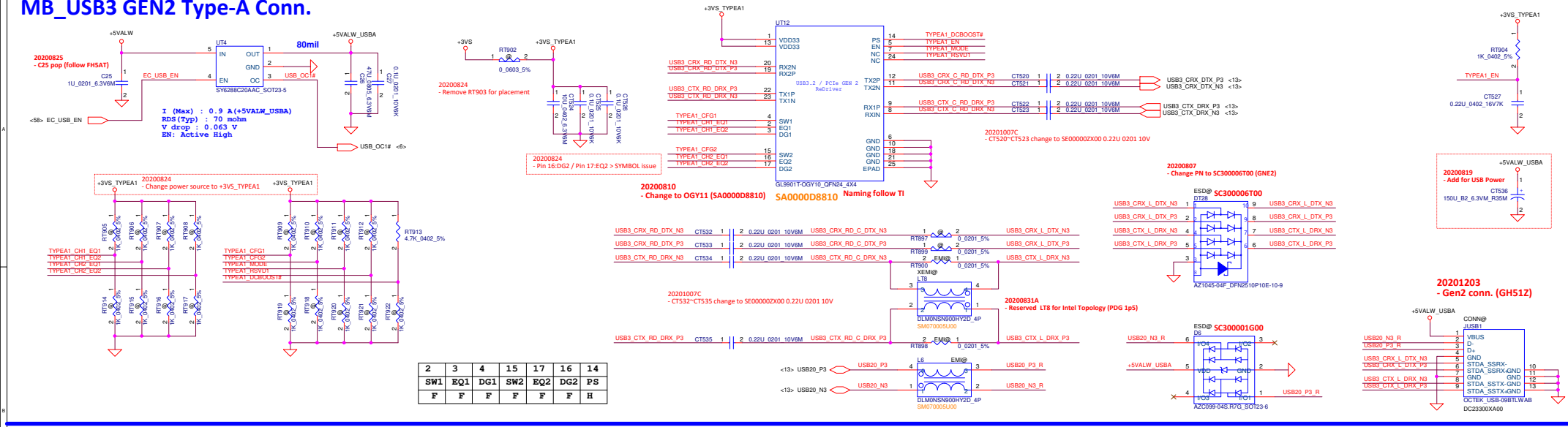
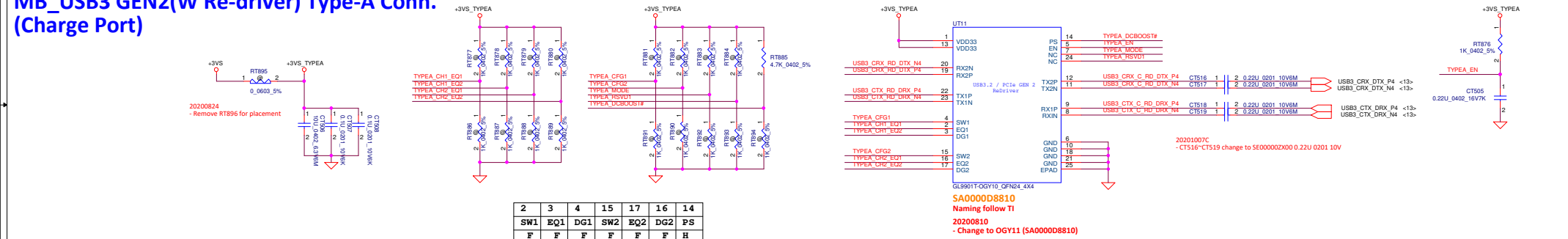
MB_USB3 GEN2 Type-A Conn.



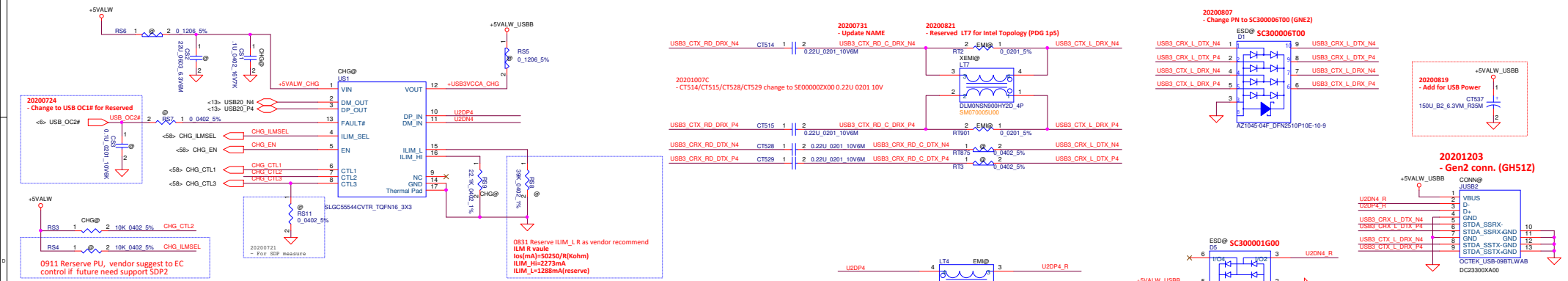
2	3	4	15	17	16	14
SW1	EQ1	DG1	SW2	EQ2	DG2	PS
F	F	F	F	F	F	H

MB_USB3 GEN2(W Re-driver) Type-A Conn. (Charge Port)



2	3	4	15	17	16	14
SW1	EQ1	DG1	SW2	EQ2	DG2	PS
F	F	F	F	F	F	H

USB Host Charger



USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title	USB2/USB3 TYPEA1&2		
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Compal Electronics, Inc.

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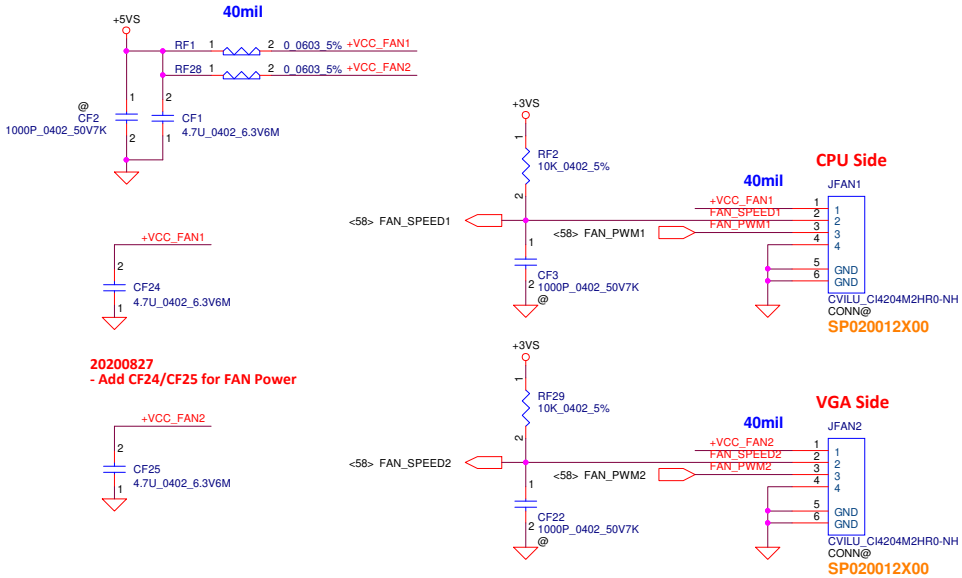
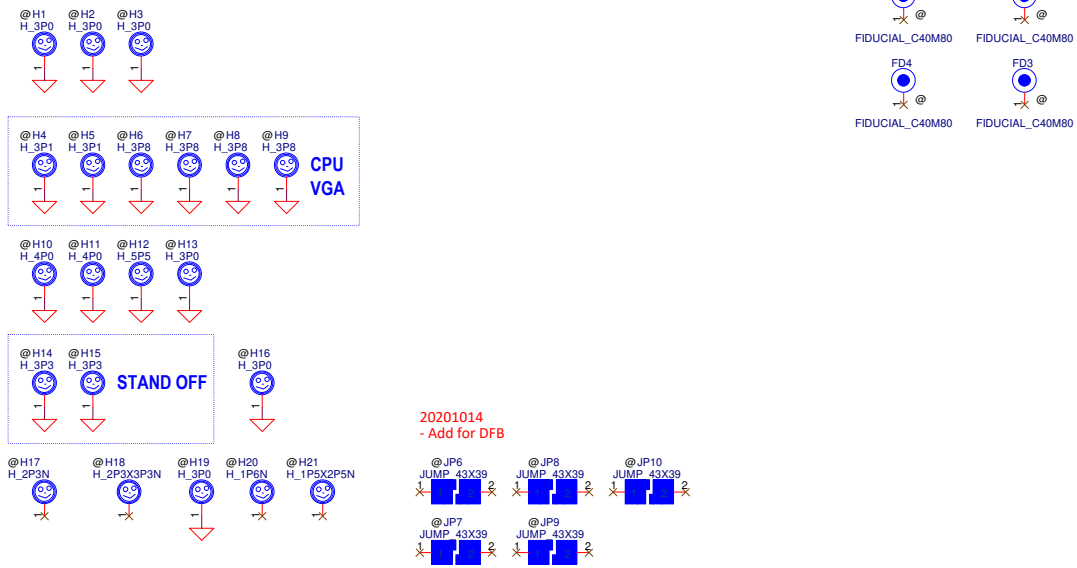
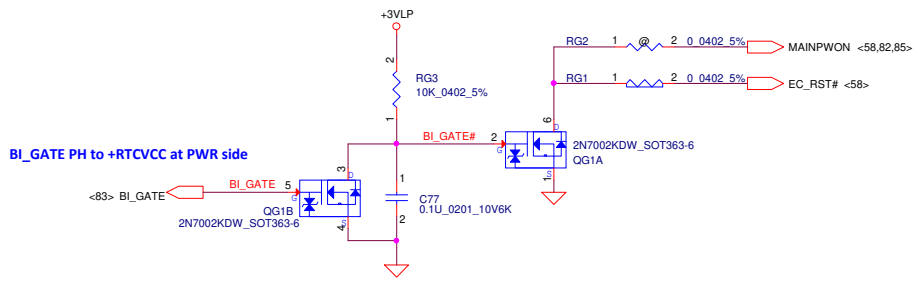
FAN1 Conn



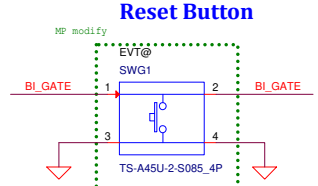
Screw Hole



Reset Circuit



Reset Button



20200728
- Need check

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

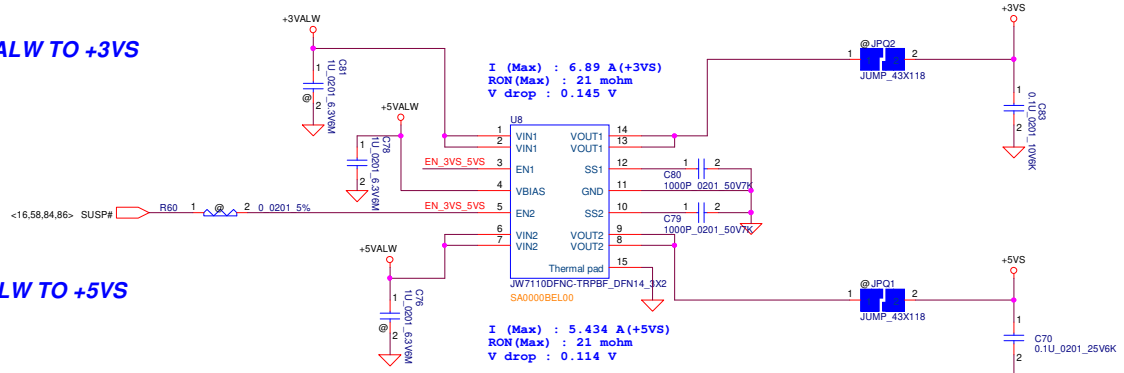
Compal Electronics, Inc.

Title: FAN & Screw Hole & Reset

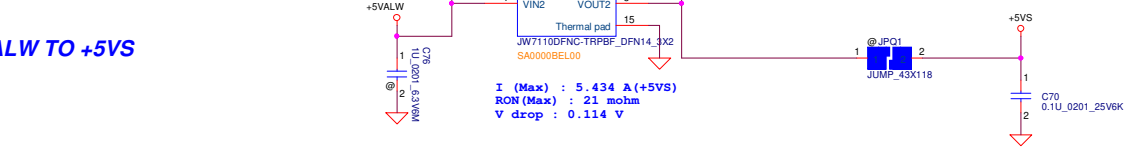
Size: Custom | Document Number: LA-K811P | Rev: 1A

Date: Thursday, January 14, 2021 | Sheet 77 of 112

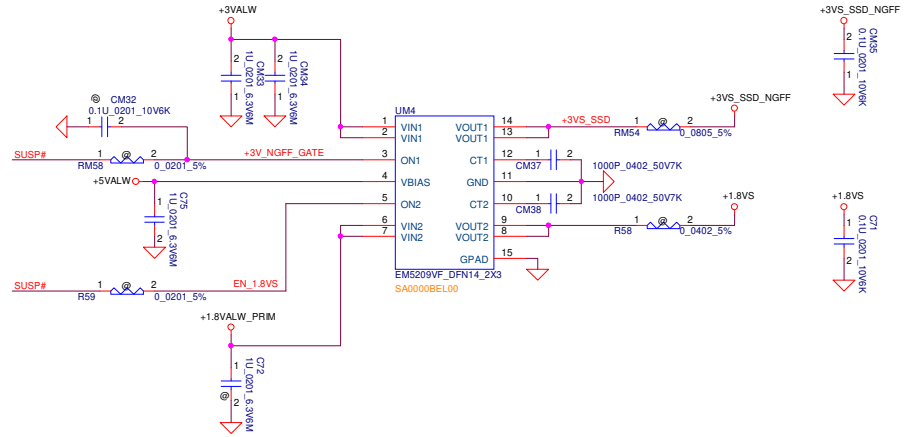
+3VALW TO +3VS



+5VALW TO +5VS



M.2 SSD Power source



+1.8VALW TO +1.8VS

20200826
- +1.8VS move to UM4

20200717
- Remove VGA Power sequence

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: **DC Interface & Sequence Logic**

Size	Document Number	Rev
	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 78 of 112

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: **XDP/CMC/APS Debug Conn**

Size	Document Number	Rev
	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 79 of 112

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

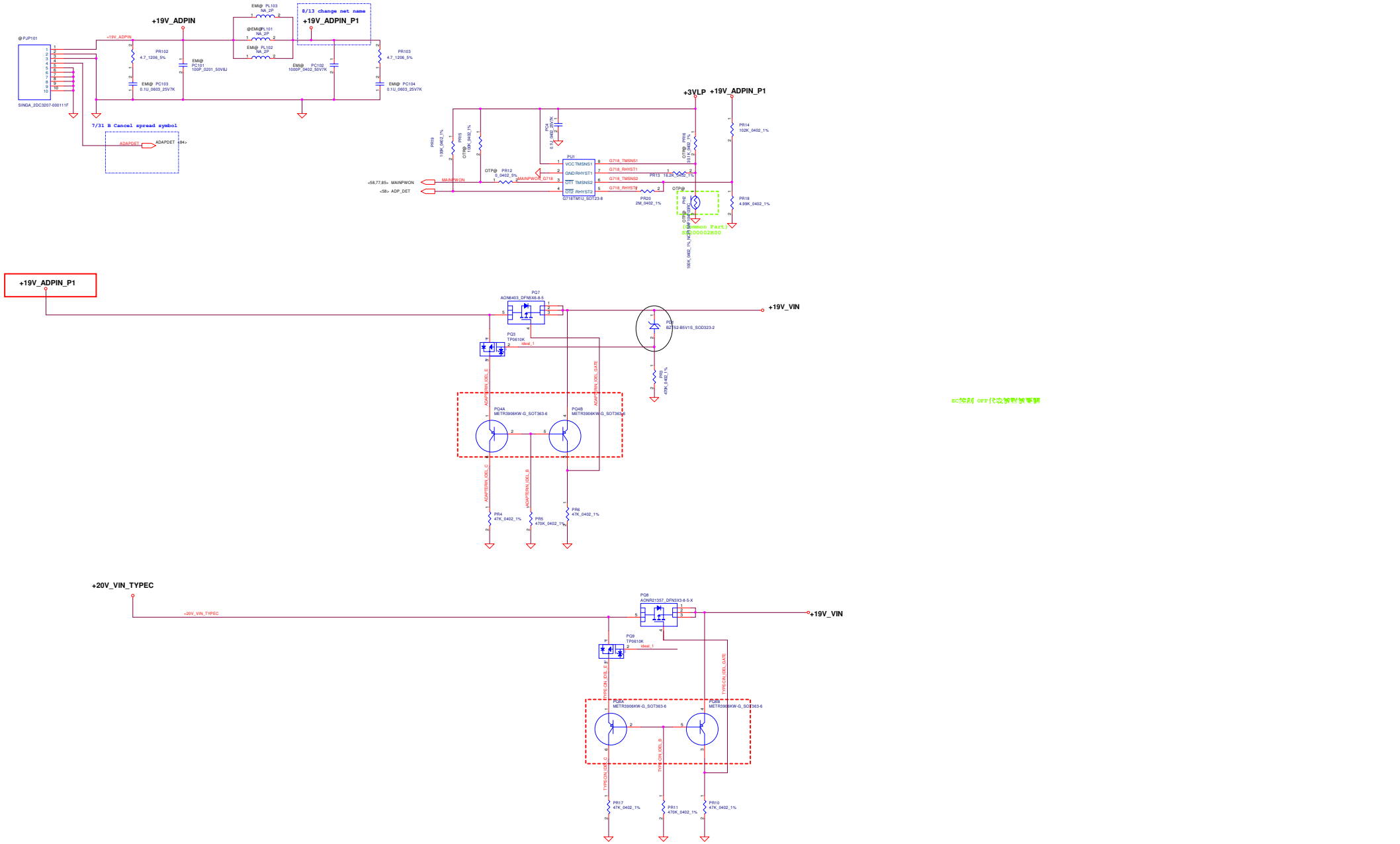
Title: **Reserve**

Size	Document Number	Rev
	LA-K811P	1A

Date: Thursday, January 14, 2021 | Sheet 80 of 112

PWR-Reserve Page

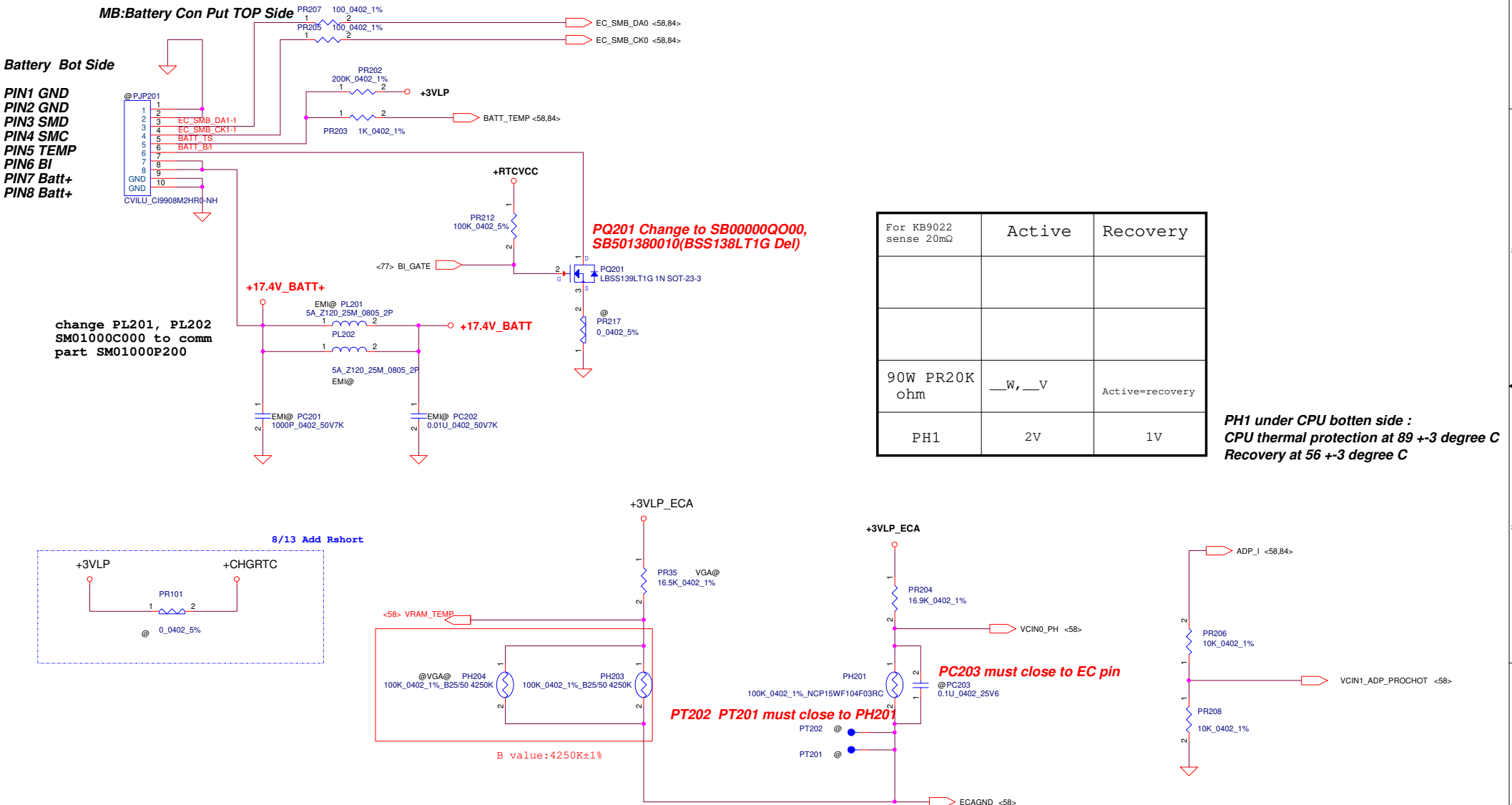
Title	<Title>	
Size A	Document Number LA-K811P	Rev 1A
Date: Thursday, January 14, 2021	Sheet 81 of 112	



EC控制 OFF切換機制

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title: PWR-DC Conn/Type-C PD selector			
Size: D	Document Number: LA-K811P		Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 82 of 112		

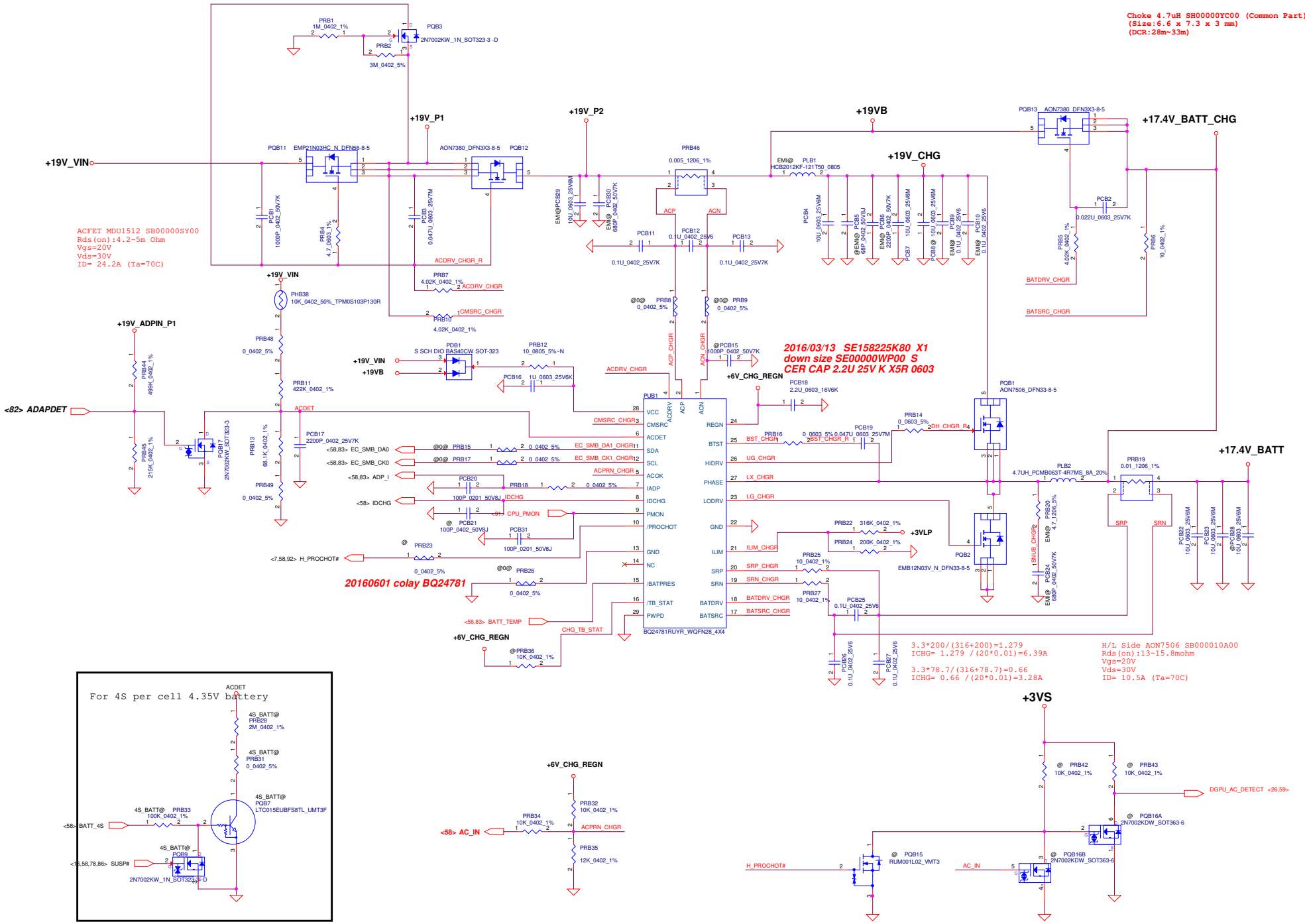


For KB9022 sense 20mΩ	Active	Recovery
90W PR20K ohm	__W,__V	Active=recovery
PH1	2V	1V

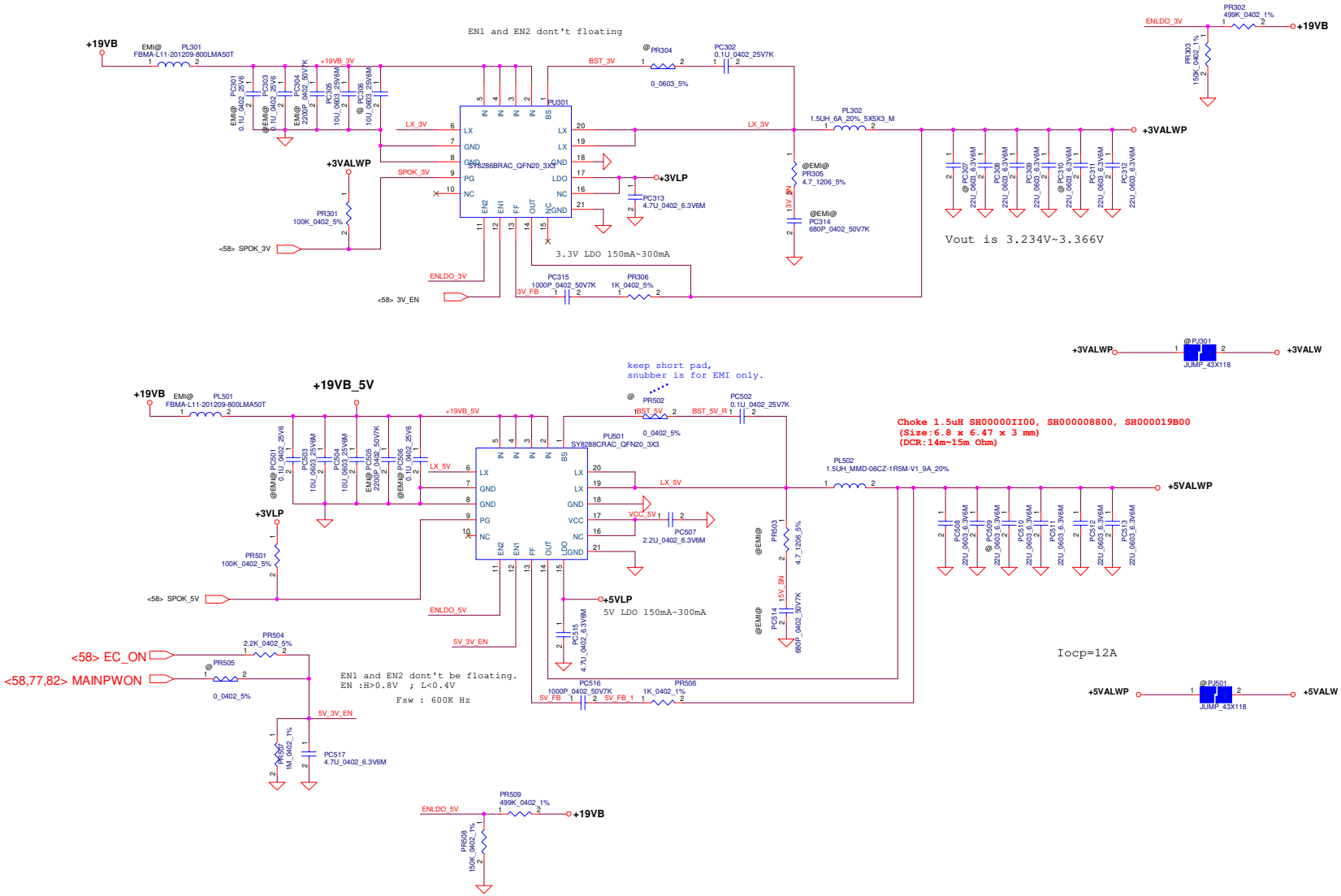
PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: LA-K811P		Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 83 of 112		



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2020/07/20	Deciphered Date	2021/07/20	Title: charger
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-K811P; Rev: 0.2
				Date: Thursday, January 14, 2021; Sheet 84 of 112



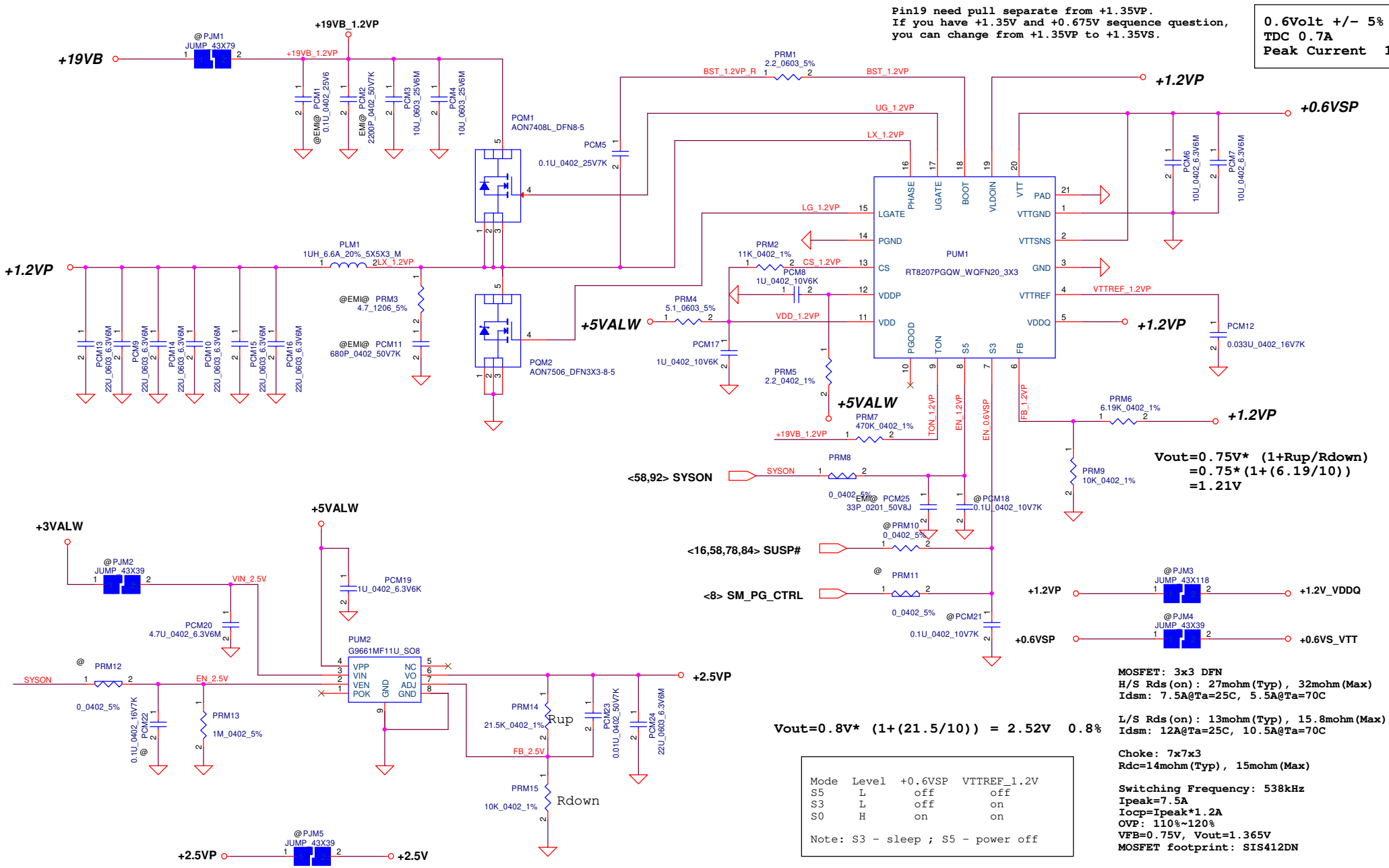
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	LA-K811P	0.2

Date: Thursday, January 14, 2021 Sheet 85 of 112



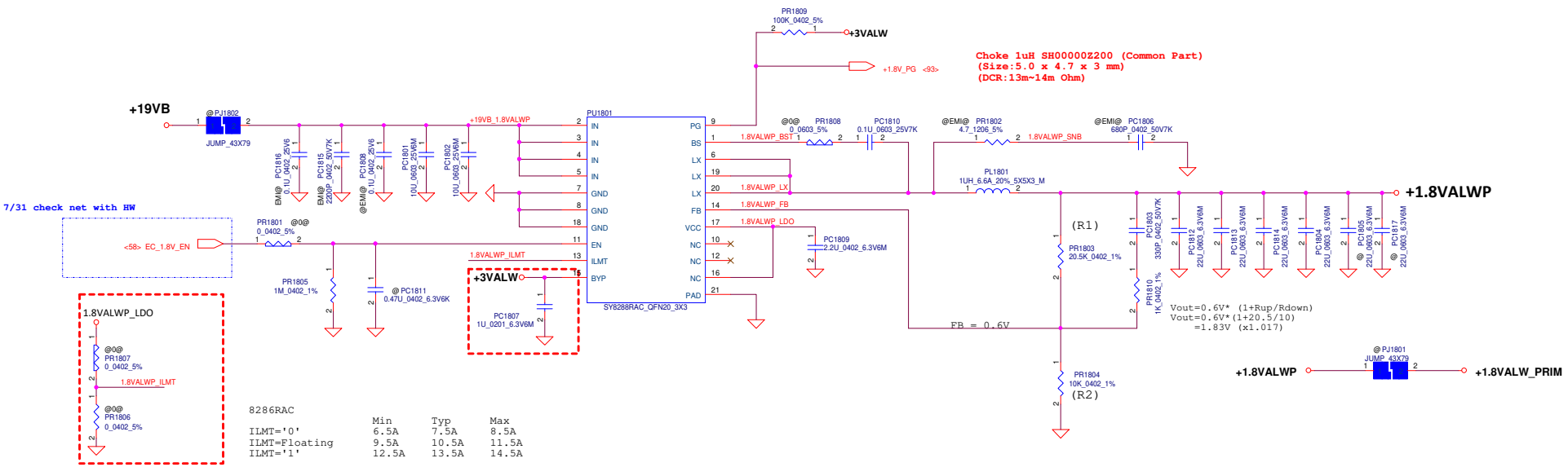
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: LA-K811P | Rev: 0.2

Date: Thursday, January 14, 2021 | Sheet 86 of 112



8286RAC

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ILMT='1'	12.5A	13.5A	14.5A

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: 1.5VS/2.5V

Size: C | Document Number: LA-K811P | Rev: 0.2

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PWR-Reserve Page

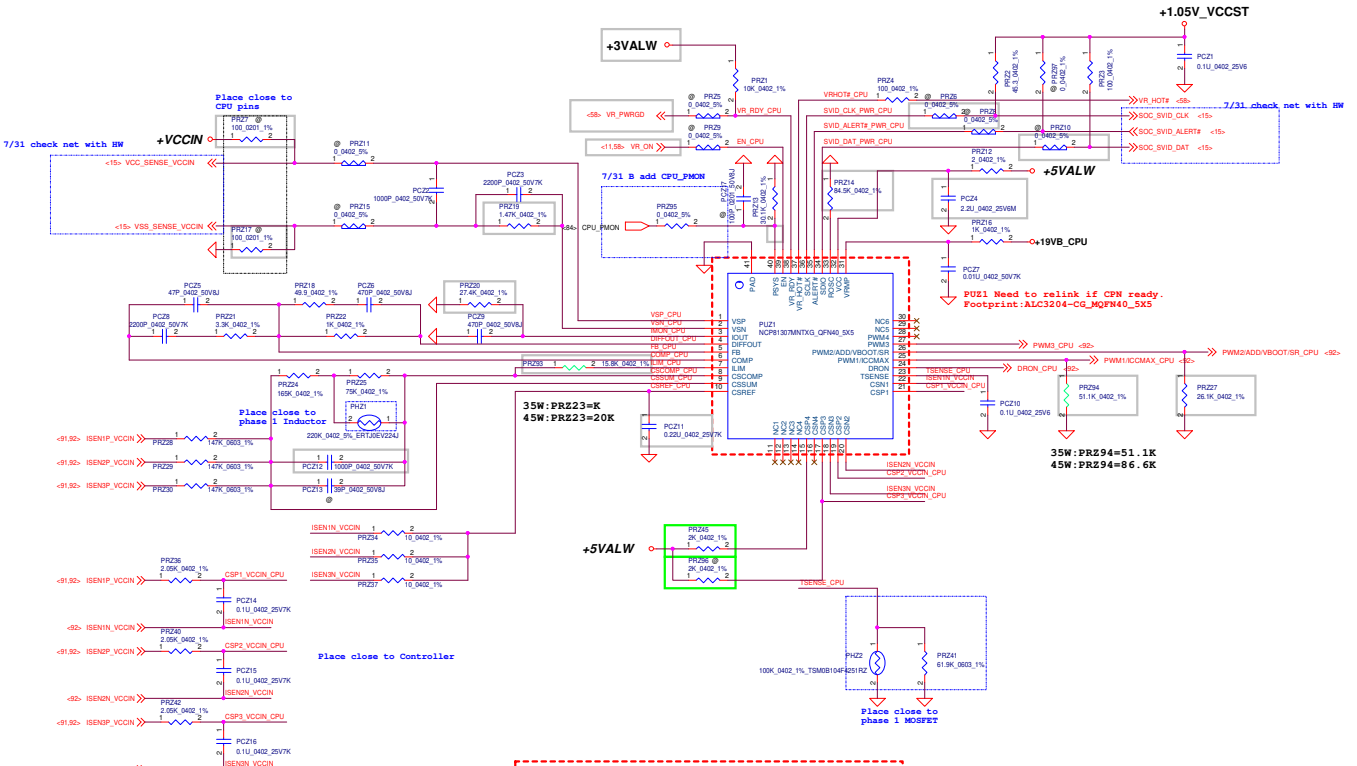
Title	<Title>	
Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 88 of 112	

PWR-Reserve Page

Title	<Title>	
Size A	Document Number LA-K811P	Rev 0.2
Date: Thursday, January 14, 2021	Sheet 89 of 112	

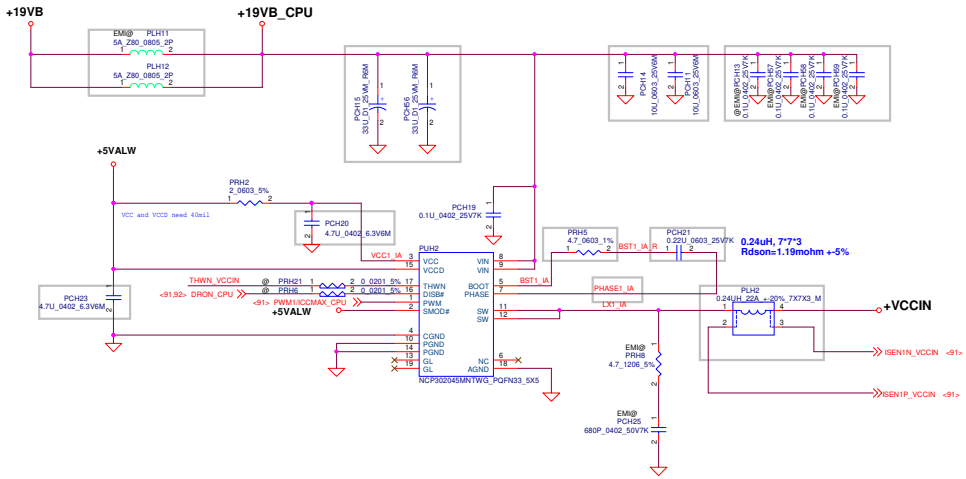
PWR-Reserve Page

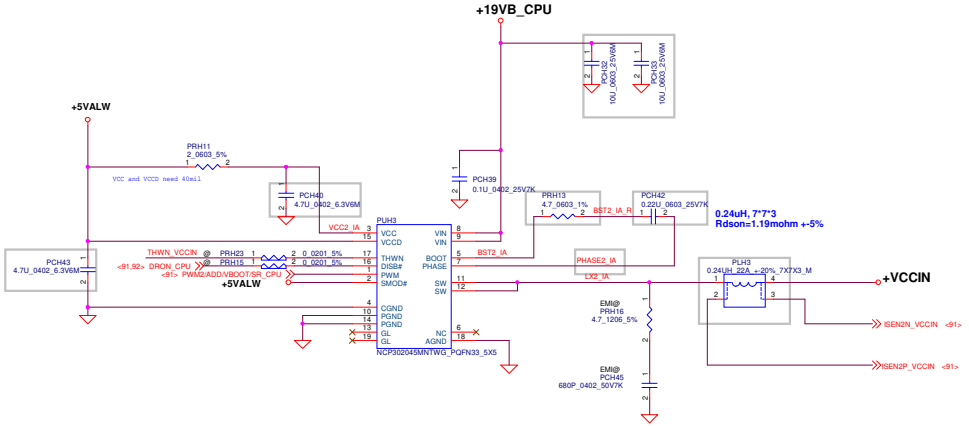
Title	<Title>	
Size A	Document Number LA-K811P	Rev 0.2
Date: Thursday, January 14, 2021	Sheet 90 of 112	

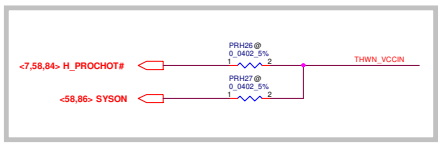


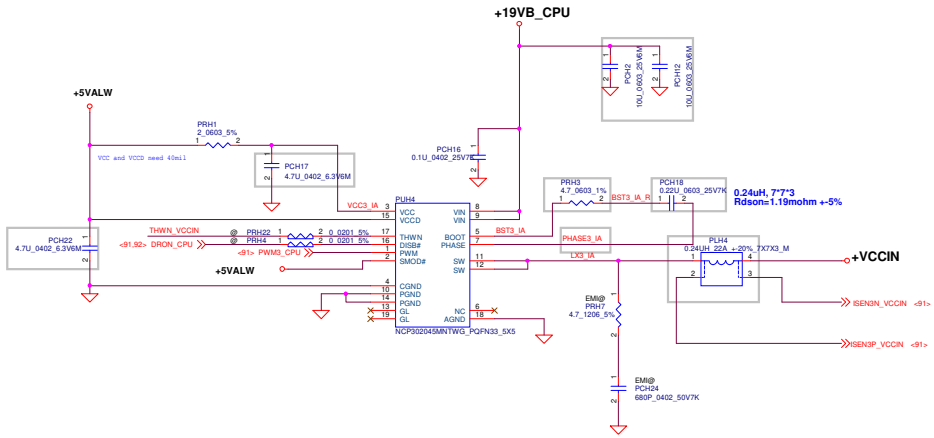
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Title	Compal Electronics, Inc.		
Size / Custom	Document Number: CPU IC TGL-H_baseline		Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 91 of 112		







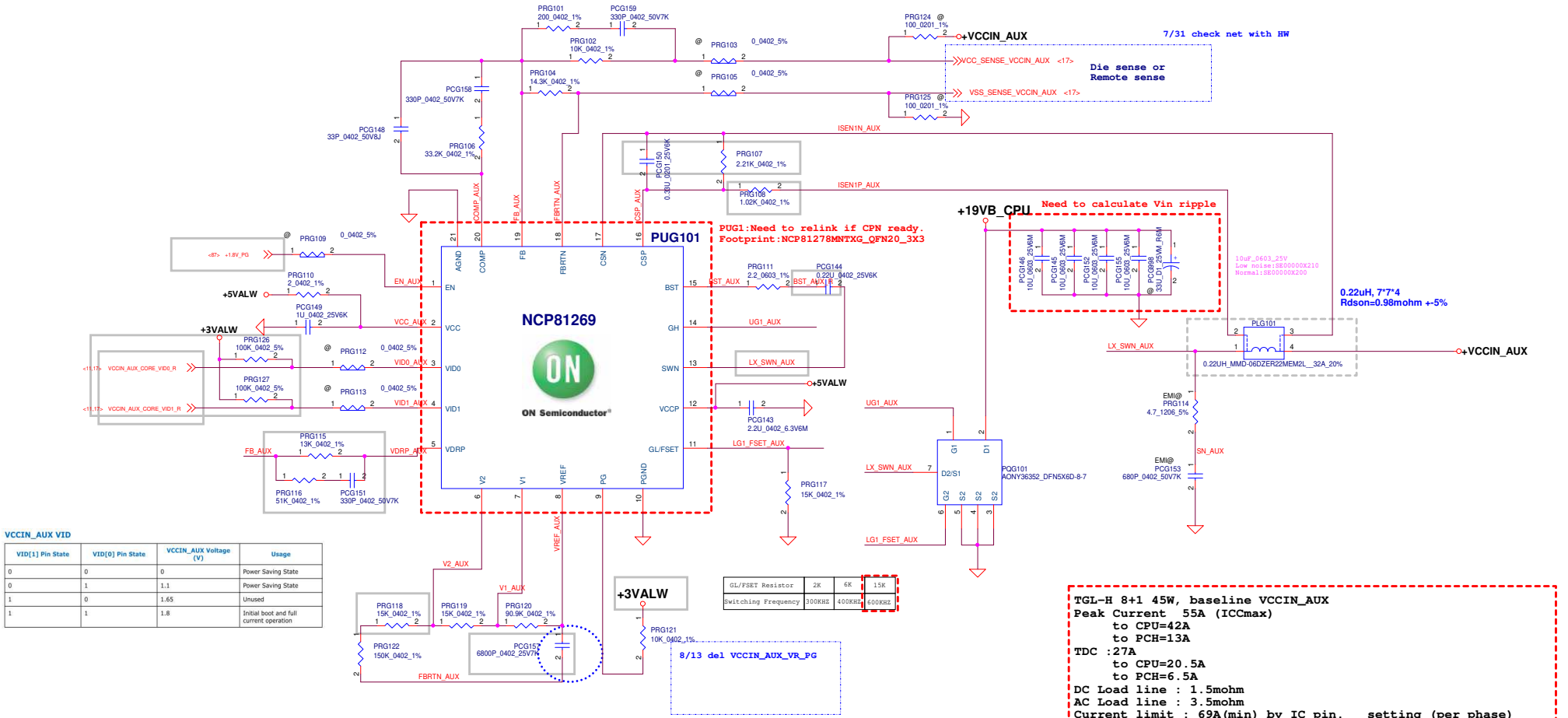


Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Title: VCCIN_SW

Size: Custom | Document Number | Rev: 0.2

Date: Thursday, January 14, 2021 | Sheet 92 of 112



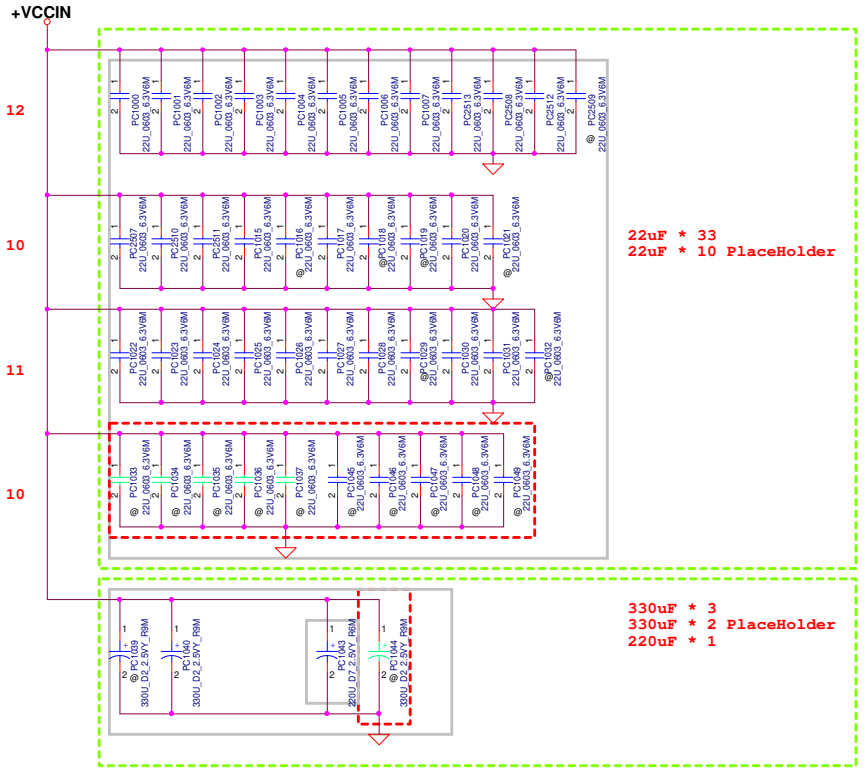
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

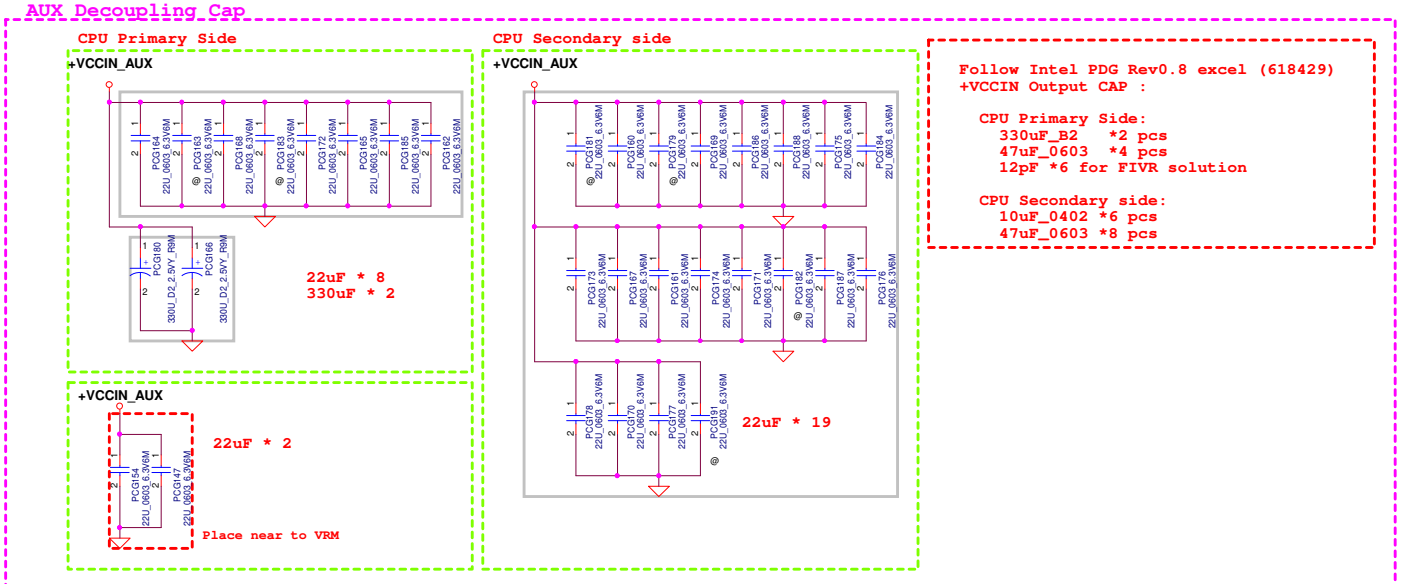
Title: VCCIN_AUX

Size | Document Number: LA-K811P | Rev: 0.2

Date: Thursday, January 14, 2021 | Sheet 93 of 112



Follow Intel PDG Rev0.8 excel (618429)
+VCCIN Output CAP :
47uF_0603 *10 pcs + reserved *2pcs
10uF_0402 *25 pcs + reserved *2pcs
220uF_D7 *4pcs + reserved *2pcs
12pF *6 for FIVR solution



Follow Intel PDG Rev0.8 excel (618429)
+VCCIN Output CAP :

CPU Primary Side:
330uF_B2 *2 pcs
47uF_0603 *4 pcs
12pF *6 for FIVR solution

CPU Secondary side:
10uF_0402 *6 pcs
47uF_0603 *8 pcs

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-K811P	0.2

Date: Thursday, January 14, 2021 Sheet 94 of 112

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 95 of 112	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 96 of 112	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 97 of 112	

PWR-Reserve Page

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Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 98 of 112	

PWR-Reserve Page

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Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 99 of 112	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K811P	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 100 of 112	

PWR-Reserve Page

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Size A	Document Number LA-K811P	Rev 0.2
Date: Thursday, January 14, 2021	Sheet 101 of 112	

PWR-Reserve Page

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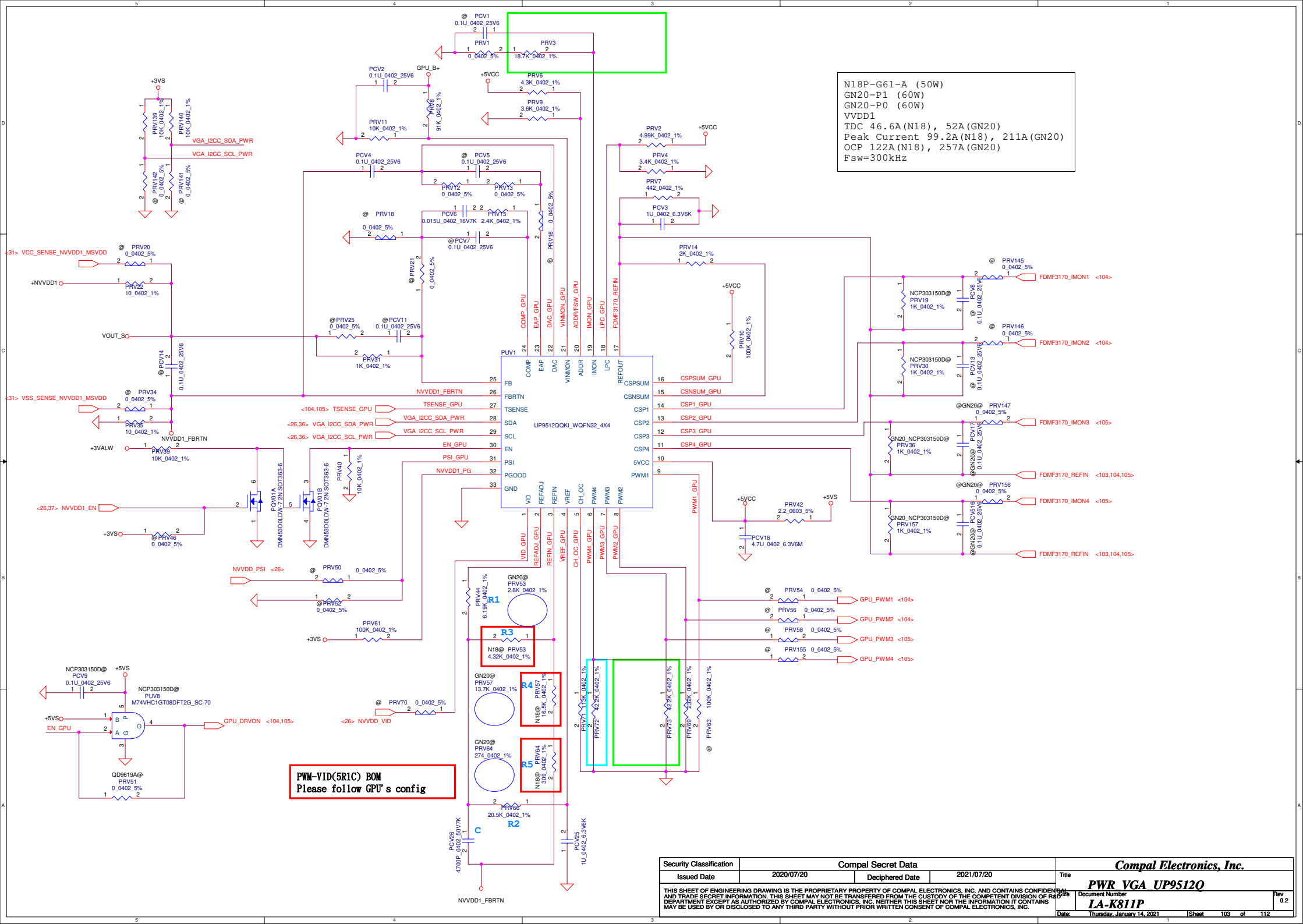
Date: Thursday, January 14, 2021	Sheet 102 of 112	



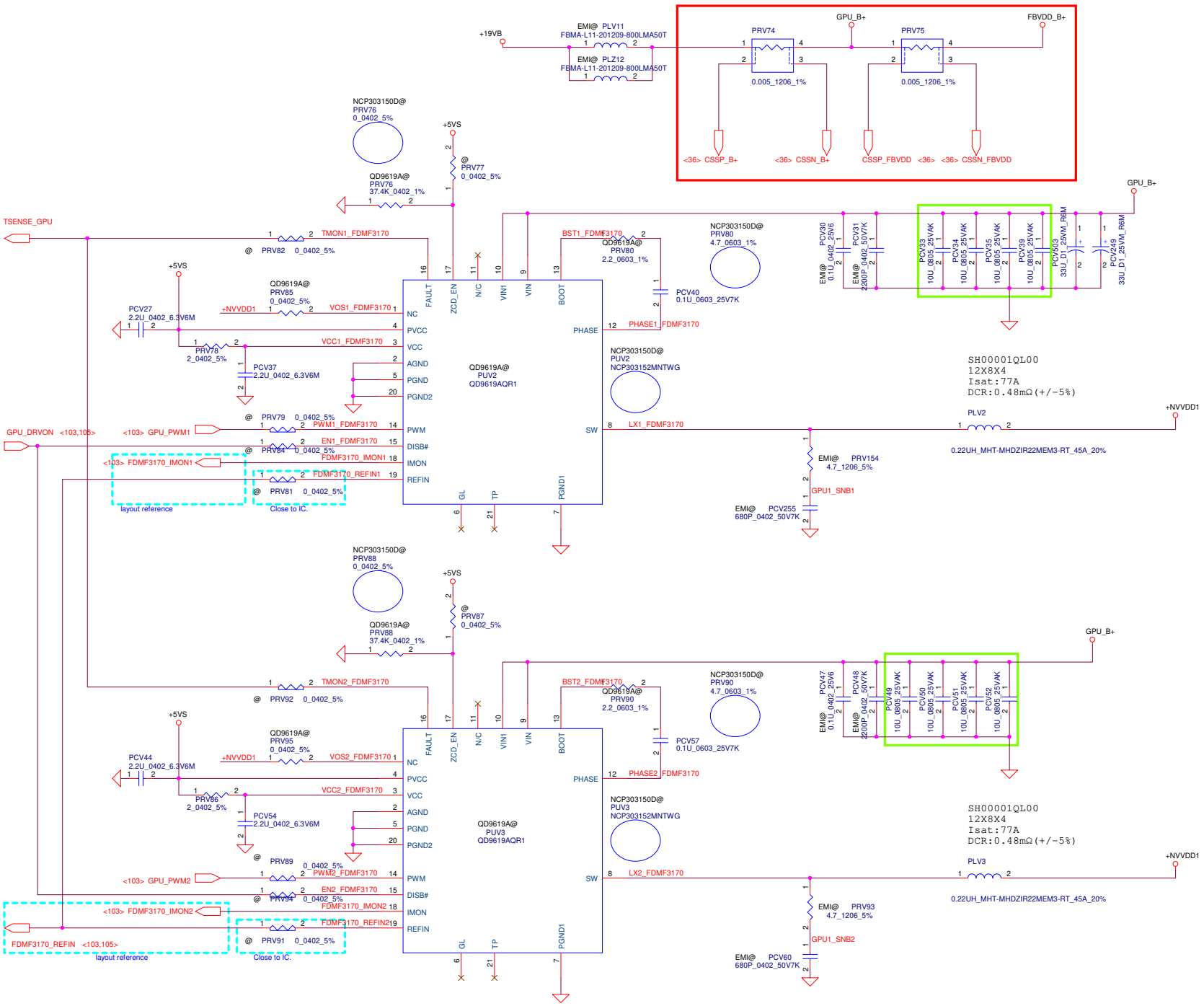
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: PWR_VGA_UP9512Q

Size: B | Document Number: LA-K811P | Rev: 0.2

Date: Thursday, January 14, 2021 | Sheet 103 of 112



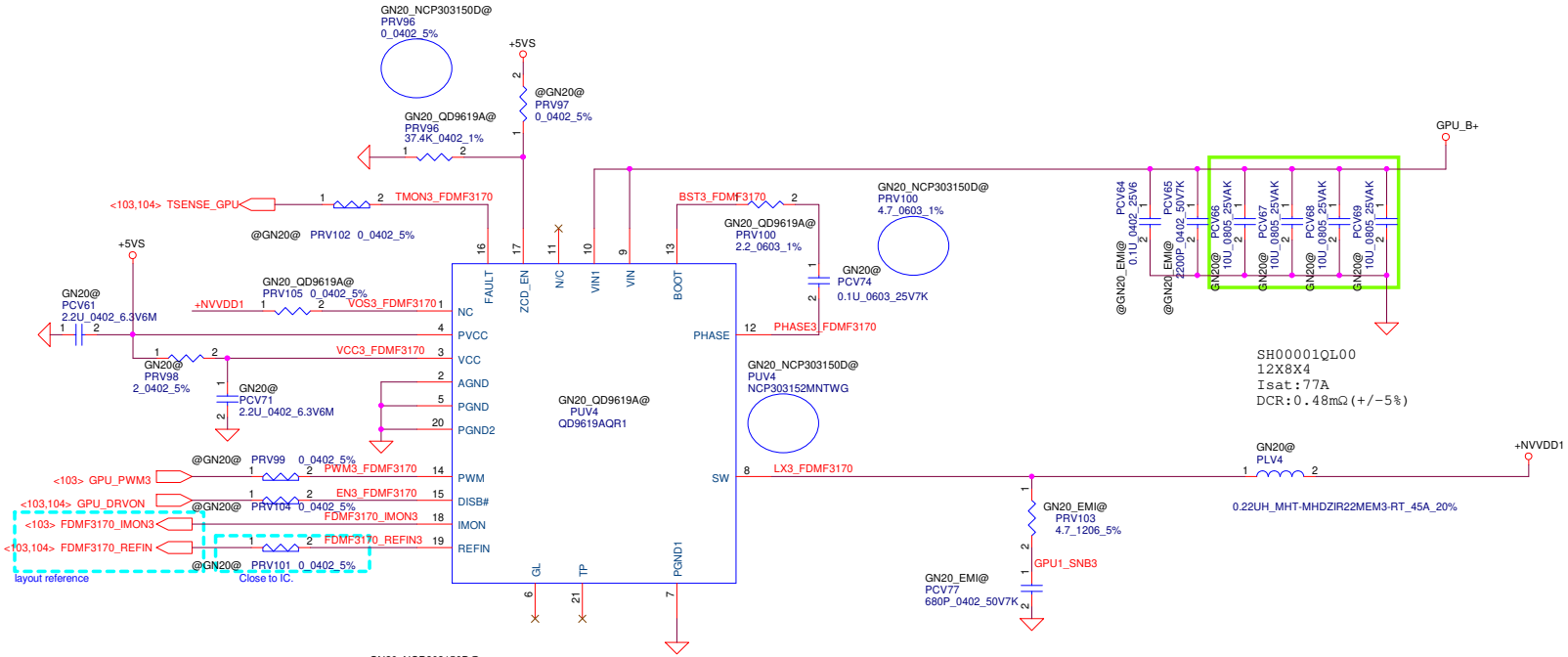
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

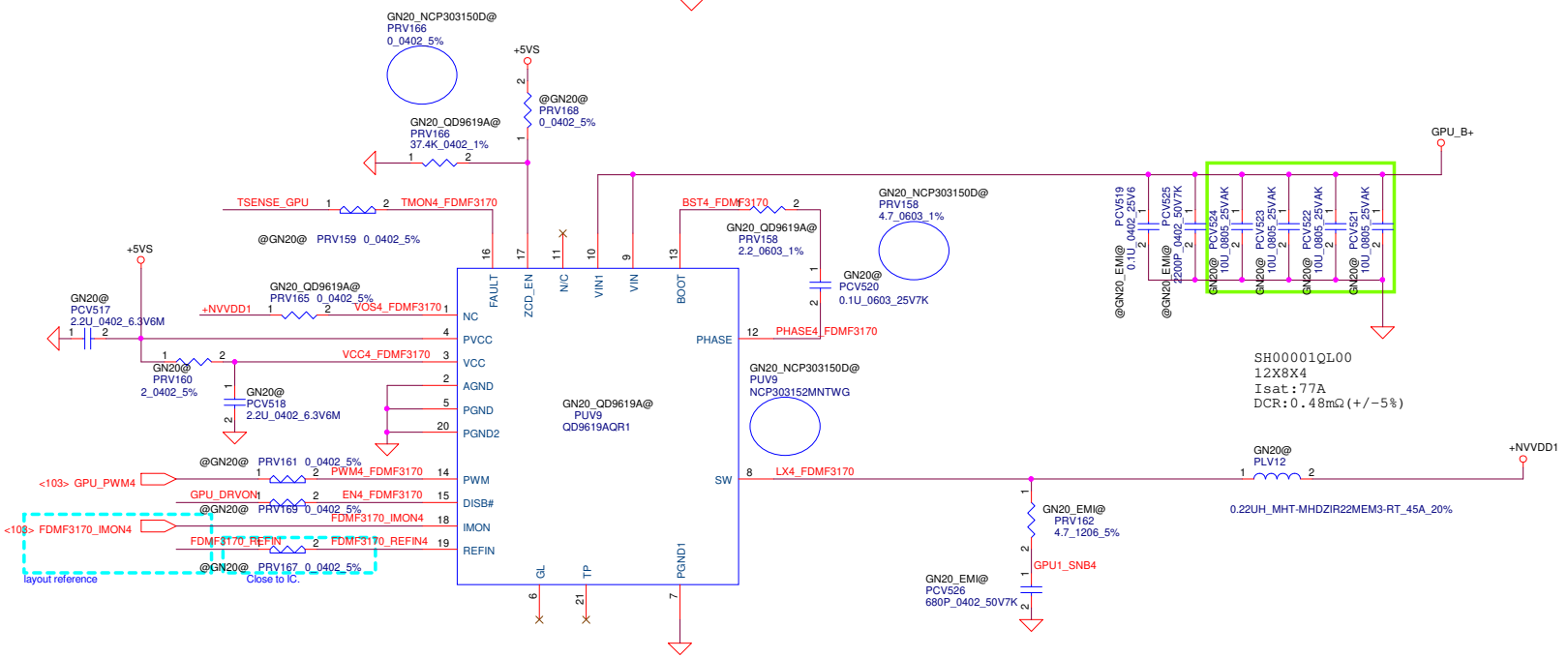
Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size | Document Number: **LA-K811P** | Rev: 0.2

Date: Thursday, January 14, 2021 | Sheet 104 of 112





Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: PWR_+NVVDD1

Size: Document Number: LA-K811P

Rev: 0.2

Date: Thursday, January 14, 2021

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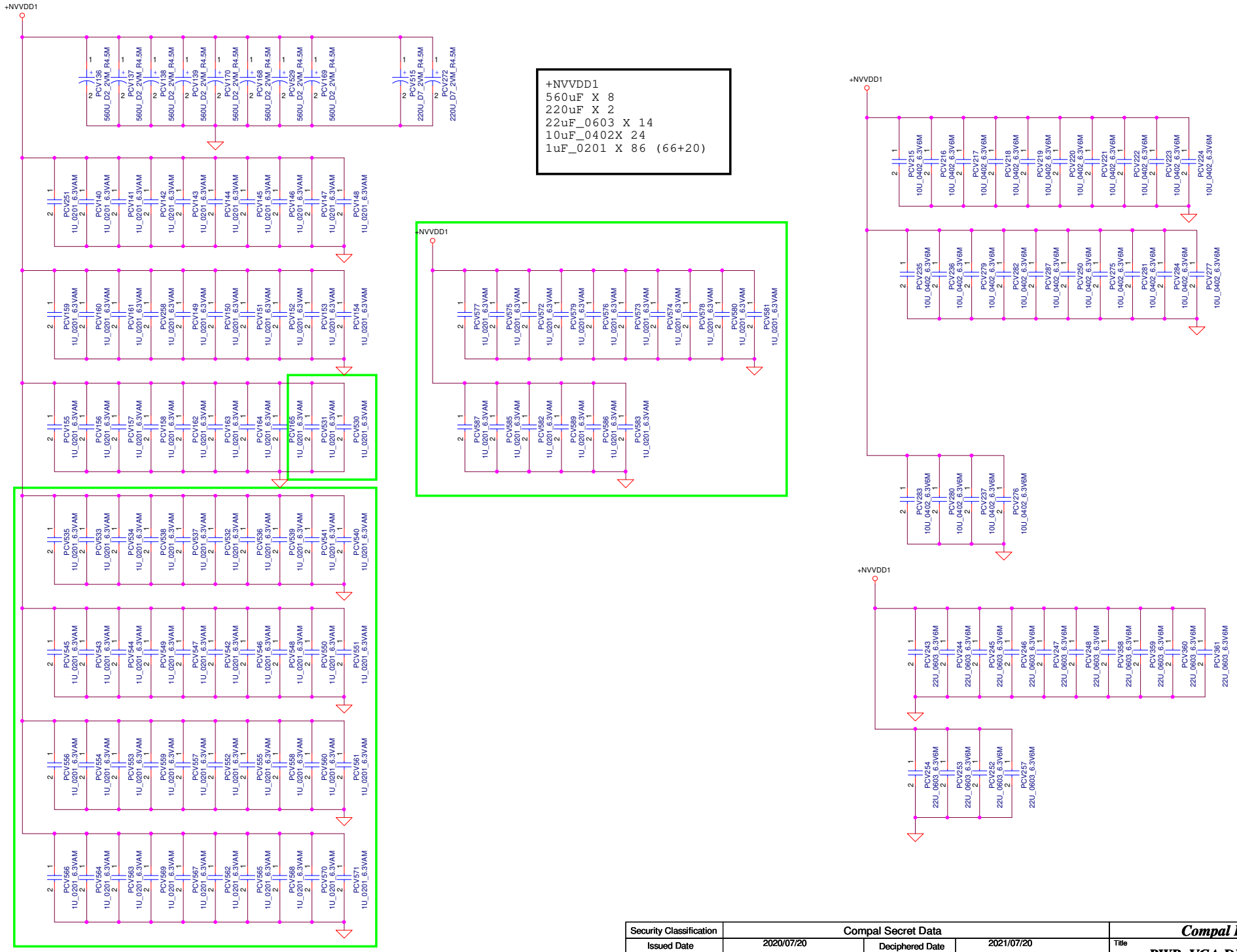
Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.		
Title: *Reserve Page*		
Size	Document Number: *LA-K811P*	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 106 of 112	



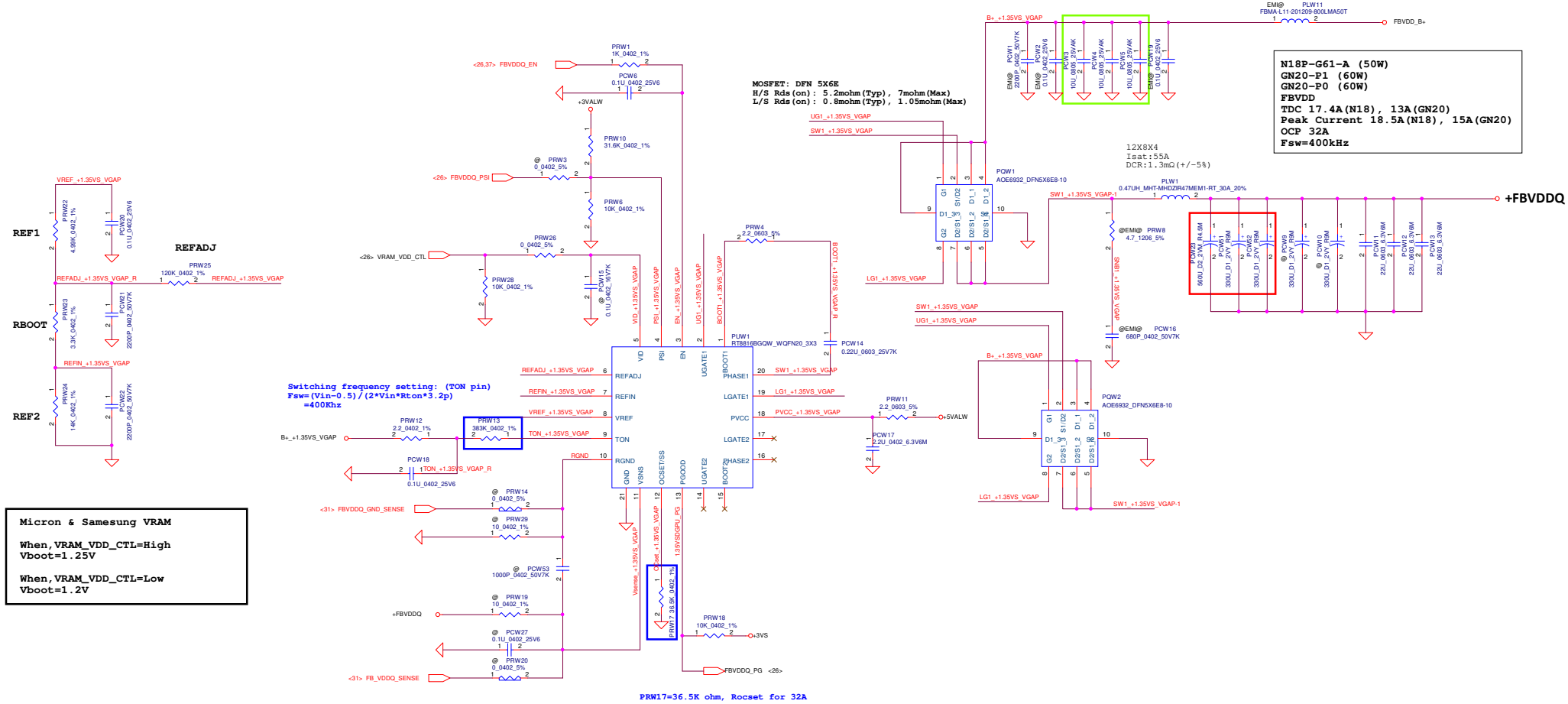
Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: PWR_VGA DECOUPLING

Size | Document Number: LA-K811P | Rev: 0.2

Date: Thursday, January 14, 2021 | Sheet 107 of 112



Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.			
Title	PWR_+VRAM		
Size	Document Number		Rev
	GH51Z LA-K851P		0.2
Date:	Thursday, January 14, 2021	Sheet	108 of 112

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

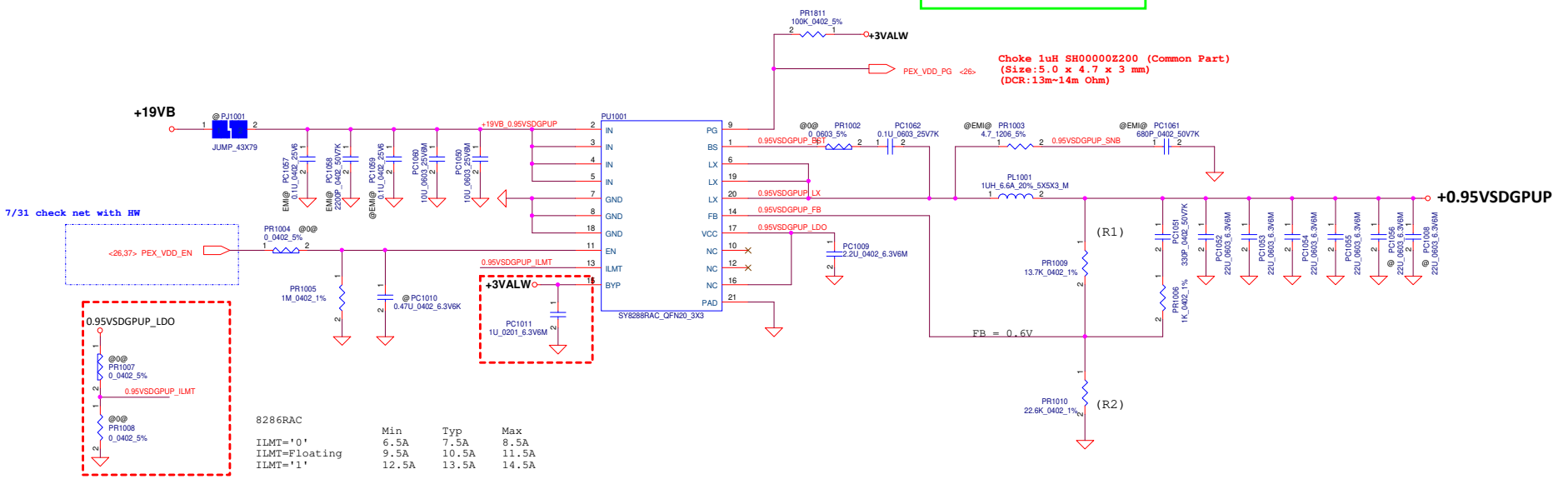
Compal Electronics, Inc.		
Title: *Reserve Page*		
Size	Document Number: *LA-K811P*	Rev: 0.2
Date: Thursday, January 14, 2021	Sheet 109 of 112	

Choke 1uH SH00000YG00 (Common Part)
(Size:3.8 x 3.8 x 1.9 mm)
Isat:3.42A
(DCR:20m~25m)
Choke: SH00000YG00 Size:4x4x2 (Common Part)
Rdc=27±20% Taiyo
Rdc=20mohm(Typ), 25mohm(Max) Cyntec
Rdc=27±20% 3L
Rdc=30±20% Tai-Tech
Rdc=32±20% Chilisin
Rdc=36mohm(Typ), Xmohm(Max) Maglayers

+0.95VSDGPUP — @PJ1003 JUMP_43X79 — +PEX_VDD

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
=0.6V* (1+13.7/22.6)
Vout=0.963V (GN20@)

Choke 1uH SH00000Z200 (Common Part)
(Size:5.0 x 4.7 x 3 mm)
(DCR:13m~14m Ohm)



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Security Classification	Compal Secret Data		
Issued Date	2020/07/20	Deciphered Date	2021/07/20

Compal Electronics, Inc.

Title: +PEX_VDD

Size	Document Number	Rev
C	LA-K811P	0.2

Date: Thursday, January 14, 2021 Sheet 110 of 112

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		design change	0.1		CHERGER IC_BQ25710->BQ24781 PCB20 PC101_SE071101J80_S CER CAP 100P 50V J NPO 0402_->_SE00000SE00_S CER CAP 100P 50V J NPO 0201 PRG114_SD001200B80_2_1206_5%_->_SD001470B80_4.7_1206_5% PCG153_SE074222K80_2200P_0402_50V7K_->_SE074681K80_680P_0402_50V7K PRH3 PRH5 PRH13_SD00001RD00_4.7_0603_1%_->_SD014220B80_2.2_0603_1% PRH3 PRH5 PRH13_SD00001RD00_4.7_0603_1%_->_SD000006T80_4.7_0603_1%	10/23	EVT1
02		design change	0.2		PRZ19SD0342101802.1K_0402_1% ->SD0000094801.47K_0402_1% PRZ20SD03425528025.5K_0402_1% ->SD03427428027.4K_0402_1% PRG115SD0344751804.75K_0402_1% ->SD03413028013K_0402_1% PC1016SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PC1018SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PC1019SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PC1021SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PC1029SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PC1032SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PC1039SGA0000E800S POLY C 330U 2.5V Y D2 ESR9M H1.9->NA PC2509SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PCG163SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PCG179SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PCG181SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PCG182SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PCG183SE00000M000S CER CAP 22U 6.3V M X5R 0603->NA PCG998SGA0000A400S POLY C 33U 25V M ESR60M D1 H1.9->NA	10/27	EVT1
09		design change	0.3		PC306SE00000X200->@ PC305SE00000X200@->@ PUZ1SA0000DOH10NCP81307MNTXG_QFN40_5X5->SA0000DOH00NCP81307MNTXG_QFN40_5X5 PCV249SGA0000C300100U_D3L_25VM_R60M->SGA0000A40033U_D1_25VM_R6M PCV590->SGA0000A40033U_D1_25VM_R6M	11/18	EVT2
10					PUV2 SA0000CUO00NCP303150DMNTWG->SA0000DIL00NCP303152MNTWG PUV3 SA0000CUO00NCP303150DMNTWG->SA0000DIL00NCP303152MNTWG PUV4 SA0000CUO00NCP303150DMNTWG->SA0000DIL00NCP303152MNTWG PUV9 SA0000CUO00NCP303150DMNTWG->SA0000DIL00NCP303152MNTWG PC1011 SE00000UC00->SE00001HM00 PC1807 SE00000UC00->SE00001HM00	11/24	PVT2
11					PRV163 SD0280000800_0402_5%->SD0280000800_0402_5% PRV166 PRV164 SD000006T804.7_0603_1%->SD000006T804.7_0603_1% PRV158 PUV10 SA0000DIL00NCP303152MNTWG->SA0000DIL00NCP303152MNTWG PUV9		
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Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
				PCB Rev 0.2			
1	9 23/24	DDR4	0922B	For INTEL PDG	MD Change to Chanel A SO-DIMM Change to Chanel B		
2	23/24	DDR4	0925A	MD / SO-DIMM pin swap			
3	6	HDMI	0929A	HDP	- Add RVH34(unpop) & RVH35(pop) for net HDMI_RT_HPD - unpop RC64 / RVH24 - pop QVH1 / RVH19		
4	43	PD	0929A	net EC_PD_INT#	unpop RT1160		
5	28	VRAM	0929A	Samsung VRAM Strap wrong	SAMSUNG pop RV34/RV32		
6	68	M.2 PCIE	0929A	Port 10 P/N is wrong	Port 10 P/N modified to correct connection .		
7	9	Memory	0929A	Memory Down strap	Add Memory Down strap (MDCHA@ & MDCHB@)		
8	42	TBT	0929A	Pin J6 need NC	Pin "NC_J6" need NC (TBT SCH check list Rev1p1) , add RT1163 (@)		
9	12/38	Panel	0929A	Panel OD	Reserve for Panel OD (SOC GPP_D0)		
10	9	WSON Socket	0929A	ROM Socket	JC1 change to WSON Socket for Debug		
11	58	BID	0929A	EVT2 Board ID	EVT2 Board ID (EVT2@)		
12	66	Thermal	0929A	Thermal sensor changed	UF3 SA00000V200 change to SA0000DSK00 (S IC G788-1P81U MSOP 8P TEMP.SENSOR)		
13		CAP	0929A	Material changed	- SE000013500 change to SE00000UC00 (6.3V) (S CER CAP 1U 6.3V M X5R 0201) - SE000013M00 change to SE00000M000 (0603) (S CER CAP 22U 6.3V M X5R 0603) - SE075223K80 change to SE068103K80 (S CER CAP 0.01UF 25V K X7R 0402) - SE00001HG00 change to SE00000V680 (S CER CAP 2.2U 10V M X5R 0402) - SE071820J80 change to SE00000SE00 (S CER CAP 100P 50V J NPO 0201)		
14	81-111	PWR SCH	0929B	POWER update	Combined Power SCH (0925) (PD-IN Solution changed - fix 20V)		
15	23/24	DDR4	1007A	MD / SO-DIMM pin swap	Combined		
16	81-111	PWR SCH	1007B	POWER update	Combined Power SCH (1006PWR) (PD-IN Solution changed - fix 20V)		
17		VGA	1007C	MD / SO-DIMM pin swap	CV613/CV616/CV617 change to SGA0000AM00 220U 2V M D7 ESR4.5M SR H1 - pop CV617 - unpop CV613/CV616		
18	71	Cap	1007D		CT520~CT523 / CT532~CT535 / CT516~CT519 / CT514/CT515/CT528/CT529 change to SE00000ZX00 0.22U 0201 10V		
19	24	DDR4	1008A	MD pin swap	DDR_A_D3 <-> DDR_A_D2		
20	77		1008A	Screw Hole	Add H20 - 1P9N		
21	62	59116F	1008A	Power net issue	Net +5V_LBPWR change to +5VS_BL		
22	43	Cap & R	1012A		- CT59 change to SE074103K80 @ EMI@ - CC7 change to SE00000SV00 & @ - CT34/CD103/CD105 change to SE000008880 - RT6 change to SD04110080 & TypeC@ - RC148/RC153/RV533/RV534/RS10/R64 change to 0_0201 R-short - R58/RK210/RK211/RV230 change to 0_0402 R-short - RT895/RT902/RW17/RW18 change to 0_0603 R-short		
23	77		1012A	Screw Hole	- Add H21 - H1P5XH2P5N - H20 change to H1P6N		
24	56/58		1012B	MIC MUTE#	- Add Net DMIC_MUTE# for Key board - Reserve R71 PU +3VS		
25	77		1012B	Screw Hole	Update H21 - H1P5XH2P5_N		
26	77		1013A	Screw Hole	Update H21 - H1P5XH2P5N		
27	39		1013A	HDMI HPD	Pop RVH34		
28	32		1014A	DFB	Remove CV613 for DFB Add JP6~JP10 for DFB		
30	77		1014A	Screw Hole	Update H21 - H_1P5XH2P5N / H20 - H_1P6N for ME H14 - H_3P3 for ME		
31	42		1016A	TBT4	Remove RT50,RT51 for Intel review		
32	77		1016A	Screw Hole	H4,H5 change to H_3P1 for Thermal		
33	11		1020A	PCH_DPWROK	DC8/DC9 Net issue , change to PCH_DPWROK .		
34	39		1020A	HDMI	- RVH1~8 change to 649_0201 (SD00002GK00) - CVH1~16 change to 0.22u_0201 (SE00000ZX00) - Add CFG 0/1/2/4 PD 1K / PU 1K & pop RVH38		
35	6		1020A	TBT4	TBT_0_LSX_RX - Reserved RC356/RC357		
36	63		1021B	TURBO KEY	Add R72 for TURBO_EN#		
37	63		1026A	FOR BOM	- QE106/107/111/113/114/116/117/119/120 SB000002N00 change to SB00001S80U		
38	13		1027A	FOR SATAXPCIE	pop RC63 & unpop RC535		
39	9		1103A	DRAM	Update DRAM config		
40			1106A	BOM (2nd list)	UM4,UV13 change to Main source : SA0000BEL00		
41	81-111	PWR SCH	1106B	POWER update	Combined Power SCH (1027PWR)		
				PCB Rev 1.0			
42	58	BID	1130A	PVT Board ID	PVT Board ID (PVT@) Update PD IC PN : SA0000DLV20		
44	81-111	PWR SCH	1130B	POWER update	Combined Power SCH (1130PWR)		
45	81-111	PWR SCH	1201A	POWER update	Combined Power SCH (1201PWR)		
46	36	OVRM	1201A	upi solution	- RV1935/RV1936 Reserved FOR UPI GEN2 (OVRM@)		
47	12	VGA	1202A	DGPU_PWR_EN	- Add PU RC538 (10K_0201) for SOC_DGPU_PWR_EN		
48	36	OVRM	1202B	OVRM GEN1/GEN2 Co-lay	Marge OVRM SCH		
49	71	USB	1203A	USB3 Conn. update	USB3 Conn. update (DC23300XA00)		
50	7 / 43	TBT	0111A	Plug sequence of Type-C	DC7 / RT104 pop , RT108 remove by GCR .		
51	9	OVRM	0111A	OVRM Strap	GPP_E12 change to OVRM GEN1 & GEN2 Strap .		
52	81-111	PWR SCH	0114B	POWER update	Combined Power SCH (1201PWR)		

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