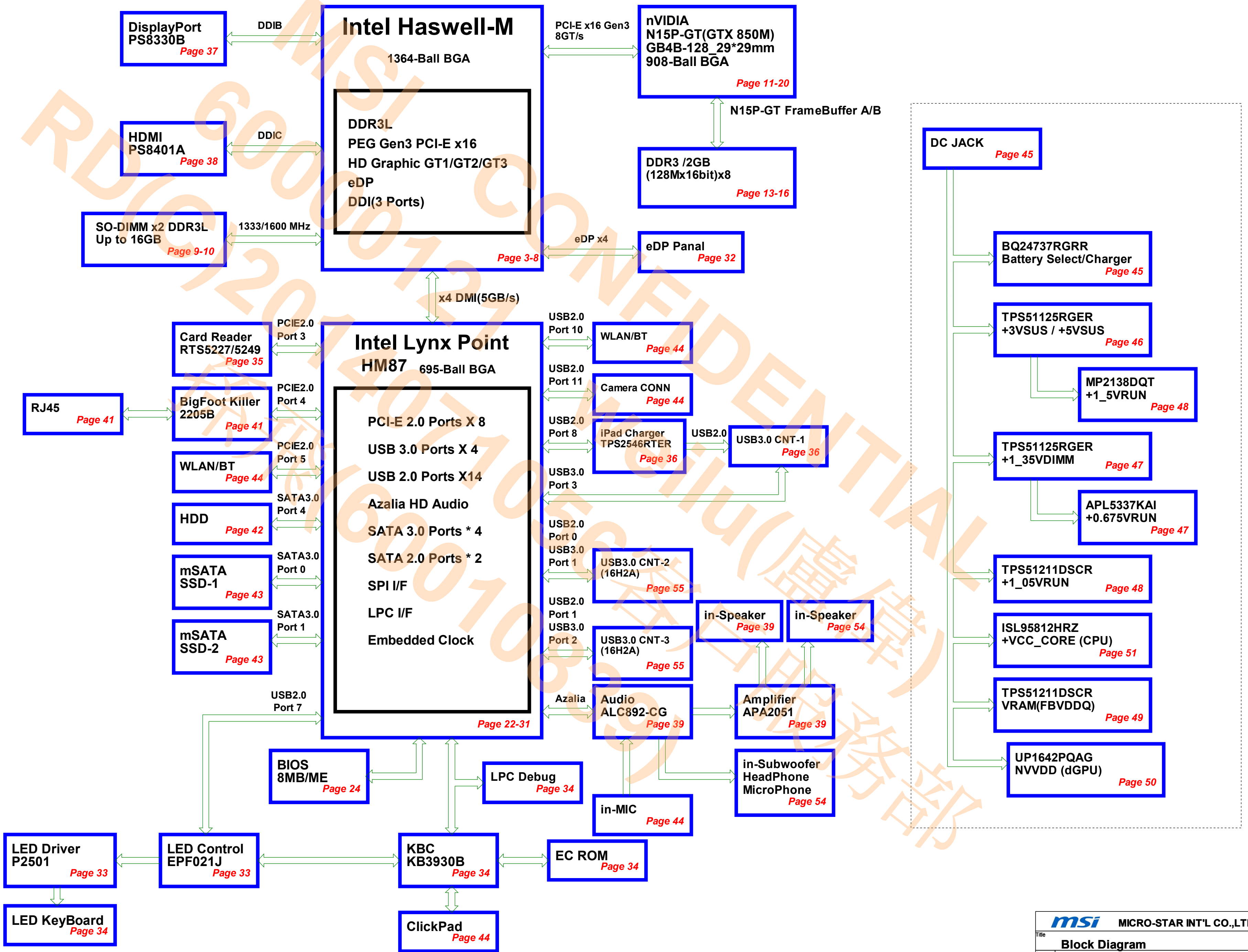
MS-16H4 Ver:0A

Shark Bay Mobile

Tuesday, March 25, 2014



MICRO-STAR INT'L CO.,LTD.

Title	Block Diagram
Size / Document Number	MS-16H4
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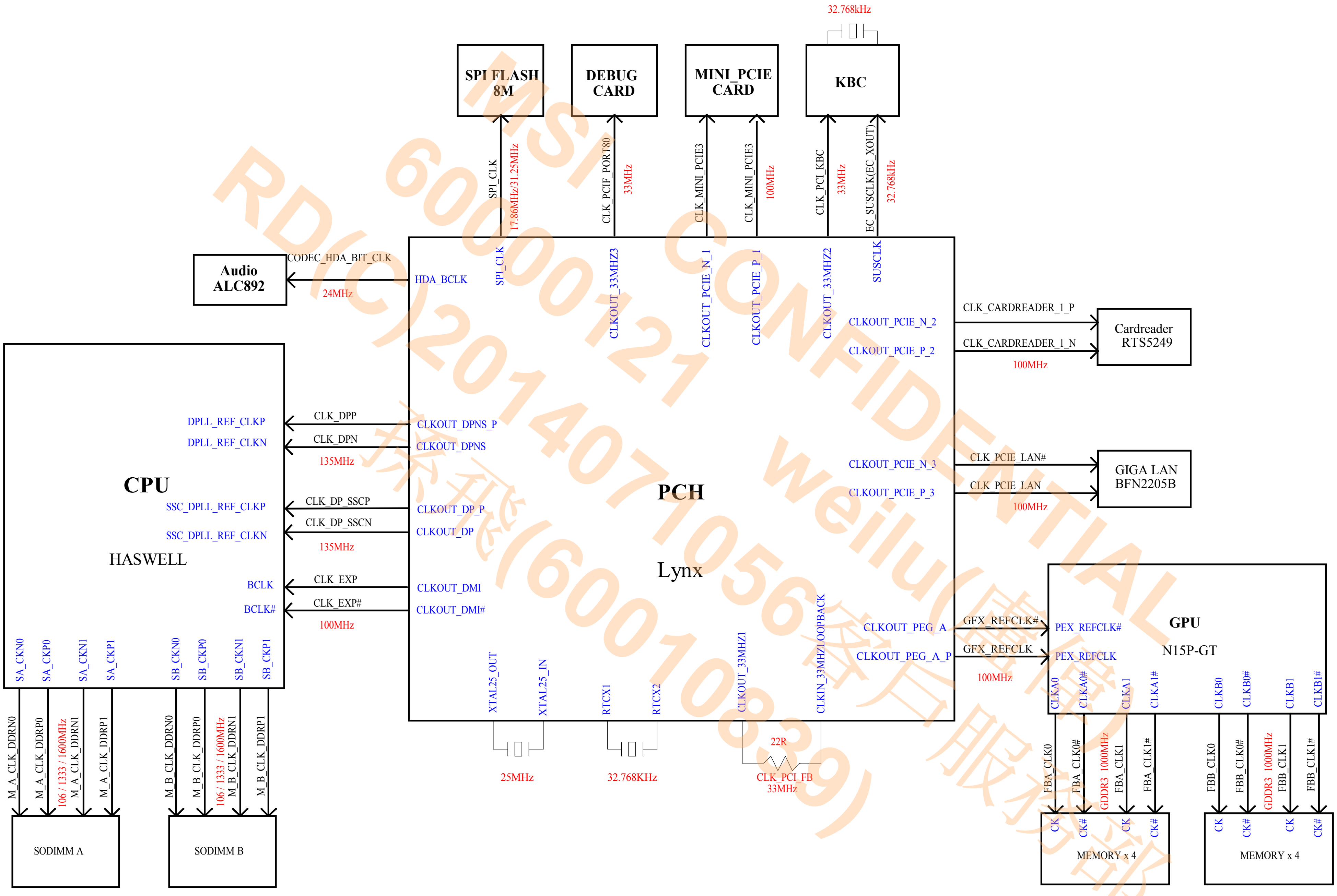
Sheet	1 of 62



MICRO-STAR INT'L CO.,LTD.

Title: CLock Delivery chart

Size | Document Number: MS-16H4 | Rev: 0A

Date: Monday, March 24, 2014 | Sheet 2 of 62

Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

U68A HASWELL_BGA_E

DMI_TXN0 25 AB2 DMI_RXN0
DMI_TXN1 25 AB3 DMI_RXN1
DMI_TXN2 25 AC3 DMI_RXN2
DMI_TXN3 25 AC1 DMI_RXN3
DMI_TXP0 25 AB1 DMI_RXP0
DMI_TXP1 25 AB4 DMI_RXP1
DMI_TXP2 25 AC4 DMI_RXP2
DMI_TXP3 25 AC2 DMI_RXP3
DMI_RXN0 25 AF2 DMI_TXN0
DMI_RXN1 25 AF4 DMI_TXN1
DMI_RXN2 25 AG4 DMI_TXN2
DMI_RXN3 25 AG2 DMI_TXN3
DMI_RXP0 25 AF1 DMI_TXP0
DMI_RXP1 25 AF3 DMI_TXP1
DMI_RXP2 25 AG3 DMI_TXP2
DMI_RXP3 25 AG1 DMI_TXP3
DMI

FDI_CSYNC 25 F11 FDI_CSYNC
FDI_INT 25 F12 DISP_INT
FDI

PEG_RCOMP AH6 PEG_COMP R206 24.9R1%0402 +VCCIOA_OUT

PEG_RXN0	E10	PEG_RXN0	11
PEG_RXN1	C10	PEG_RXN1	11
PEG_RXN2	B10	PEG_RXN2	11
PEG_RXN3	E9	PEG_RXN3	11
PEG_RXN4	D9	PEG_RXN4	11
PEG_RXN5	B9	PEG_RXN5	11
PEG_RXN6	L5	PEG_RXN6	11
PEG_RXN7	L2	PEG_RXN7	11
PEG_RXN8	M4	PEG_RXN8	11
PEG_RXN9	L4	PEG_RXN9	11
PEG_RXN10	M2	PEG_RXN10	11
PEG_RXN11	V5	PEG_RXN11	11
PEG_RXN12	V4	PEG_RXN12	11
PEG_RXN13	V1	PEG_RXN13	11
PEG_RXN14	Y3	PEG_RXN14	11
PEG_RXN15	Y2	PEG_RXN15	11
PEG_RXP0	F10	PEG_RXP0	11
PEG_RXP1	D10	PEG_RXP1	11
PEG_RXP2	A10	PEG_RXP2	11
PEG_RXP3	F9	PEG_RXP3	11
PEG_RXP4	C9	PEG_RXP4	11
PEG_RXP5	A9	PEG_RXP5	11
PEG_RXP6	M5	PEG_RXP6	11
PEG_RXP7	L1	PEG_RXP7	11
PEG_RXP8	M3	PEG_RXP8	11
PEG_RXP9	L3	PEG_RXP9	11
PEG_RXP10	M1	PEG_RXP10	11
PEG_RXP11	Y5	PEG_RXP11	11
PEG_RXP12	V3	PEG_RXP12	11
PEG_RXP13	V2	PEG_RXP13	11
PEG_RXP14	Y4	PEG_RXP14	11
PEG_RXP15	Y1	PEG_RXP15	11
PEG_TXN0	B6	PEG_TXN0	11
PEG_TXN1	C5	PEG_TXN1	11
PEG_TXN2	E6	PEG_TXN2	11
PEG_TXN3	D4	PEG_TXN3	11
PEG_TXN4	G4	PEG_TXN4	11
PEG_TXN5	E3	PEG_TXN5	11
PEG_TXN6	J5	PEG_TXN6	11
PEG_TXN7	G3	PEG_TXN7	11
PEG_TXN8	J3	PEG_TXN8	11
PEG_TXN9	J2	PEG_TXN9	11
PEG_TXN10	T6	PEG_TXN10	11
PEG_TXN11	R6	PEG_TXN11	11
PEG_TXN12	R2	PEG_TXN12	11
PEG_TXN13	R4	PEG_TXN13	11
PEG_TXN14	T4	PEG_TXN14	11
PEG_TXN15	T1	PEG_TXN15	11
PEG_TXP0	C6	PEG_TXP0	11
PEG_TXP1	B5	PEG_TXP1	11
PEG_TXP2	D6	PEG_TXP2	11
PEG_TXP3	E4	PEG_TXP3	11
PEG_TXP4	G5	PEG_TXP4	11
PEG_TXP5	E2	PEG_TXP5	11
PEG_TXP6	J6	PEG_TXP6	11
PEG_TXP7	G2	PEG_TXP7	11
PEG_TXP8	J4	PEG_TXP8	11
PEG_TXP9	J1	PEG_TXP9	11
PEG_TXP10	T5	PEG_TXP10	11
PEG_TXP11	R5	PEG_TXP11	11
PEG_TXP12	R1	PEG_TXP12	11
PEG_TXP13	R3	PEG_TXP13	11
PEG_TXP14	T3	PEG_TXP14	11
PEG_TXP15	T2	PEG_TXP15	11

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Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil

U68B HASWELL_BGA_E

MISC
C51 PROC_DETECT
G50 CATERR
G51 PECI
34 H_PECI
H_PROCHOT# R E50 PROCHOT
27 H_THRMTRIP# D53 THERMTRIP
THERMAL

DDR3
SM_RCOMP0 BB51 SM_RCOMP0_JNC R219 100R1%0402 GND
SM_RCOMP1 BB53 SM_RCOMP1_JNC R215 75R1%0402
SM_RCOMP2 BB52 SM_RCOMP2_JNC R218 100R1%0402
SM_DRAMRST BE51 CPUDRAMRST#

25 H_PM_SYNC D52 PM_SYNC
F50 PWRGOOD
PM_DRAM_PWRGD_R AP48 SM_DRAMPWROK
27 PCH_PLTRST_CPU L54 PLTRSTIN
27 H_CPUPWRGD
PWR

JTAG
PRDY N53
PREQ N52
TCK N54 XDP_TCLK
TMS M51
TRST M53 XDP_TRST#
TDI N49
TDO M49
DBR F53

R194 10KR1%0402 GND

CLOCK
23 CLK_DPN AC6 DPLL_REF_CLKN
23 CLK_DPP AE6 DPLL_REF_CLKP
23 CLK_DP_SSCN V6 SSC_DPLL_REF_CLKN
23 CLK_DP_SSCP Y6 SSC_DPLL_REF_CLKP
23 CLK_EXP# AB6 BCLKN
23 CLK_EXP AA6 BCLKP

BPM#0 R51
BPM#1 R50
BPM#2 P49
BPM#3 N50
BPM#4 R49
BPM#5 P53
BPM#6 U51
BPM#7 P51

2 OF 12

H_CPUPWRGD EC8 X_C15p50N0402 GND

p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.

XDP_TCLK R34 X_51R1%0402
XDP_TRST# R36 X_51R1%0402
GND

+1_35VDIMM
Not Support Deep S3
R41 1.8K1%0402-HF
1.35V
25 PM_DRAM_PWRGD R39 X_0402 PM_DRAM_PWRGD_R
R40 3.3KR1%0402
GND

1K on CRB , 0R on DG

R,C Close SO-DIMM
9,10 DDR3_DRAMRST# R50 X_0402 CPUDRAMRST#
EC1 X_C0.1u50X70402
GND

EC Sink current 2 mA

+VCCIO_OUT
R193 681R1%0402
34 EC_PROCHOT# R192 56R0402 H_PROCHOT# R
51 IMVP_PROCHOT# 1 2 JNC9 X_0402

47P close PWM

MICRO-STAR INT'L CO.,LTD.

Title	CPU-1 (Host Bus)	
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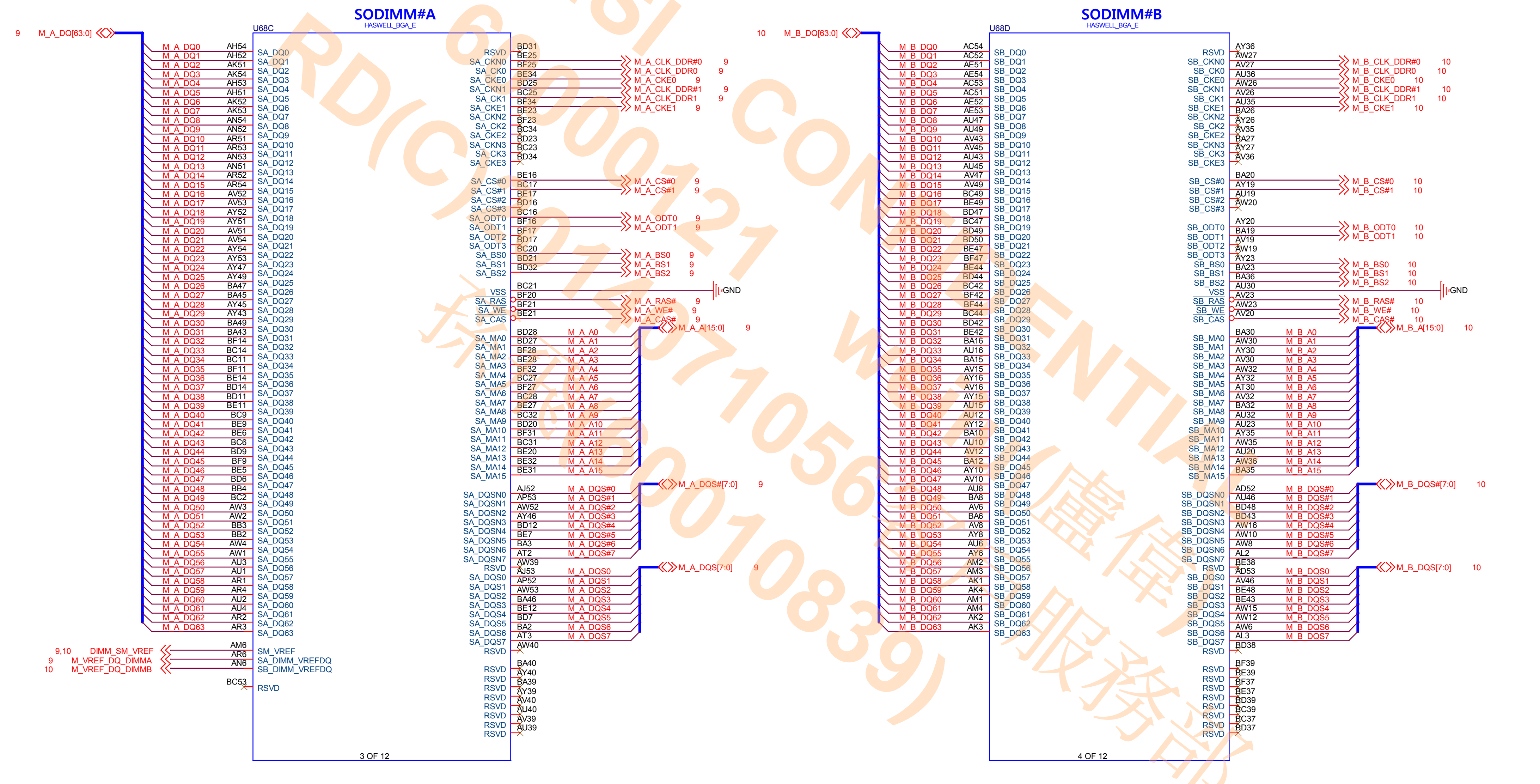
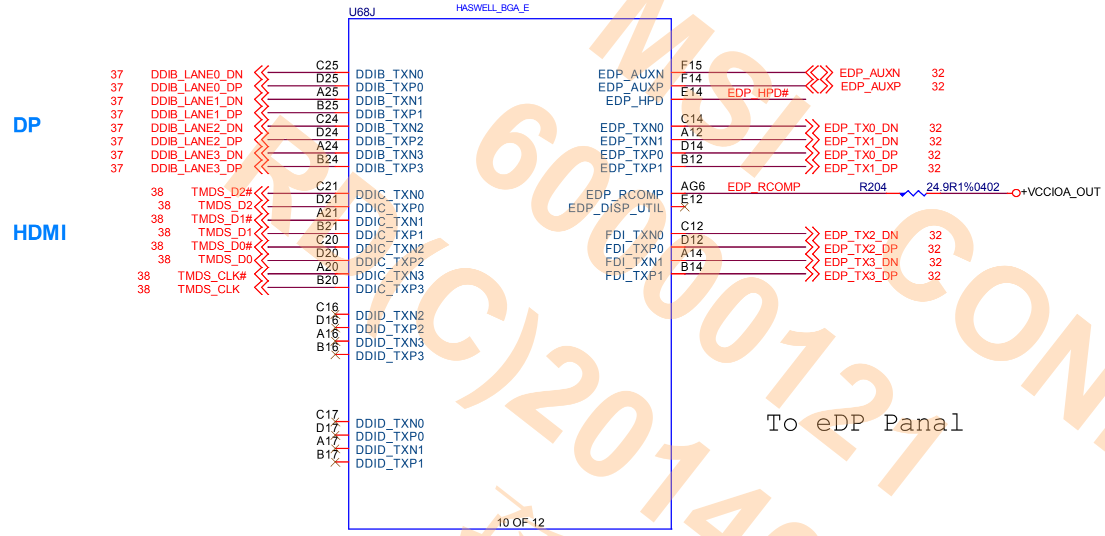
Haswell (DDR3L)



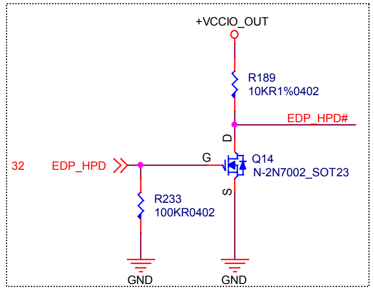
MICRO-STAR INT'L CO.,LTD.

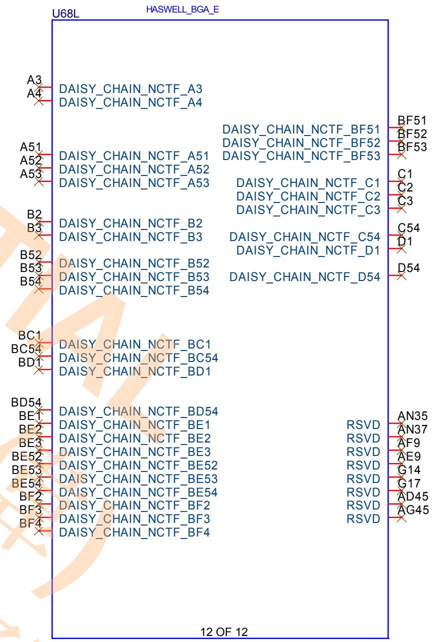
Title	CPU-2 (DDR3L)	
Size	Document Number: MS-16H4	Rev 0A
Date: Monday, March 24, 2014	Sheet 4 of 62	

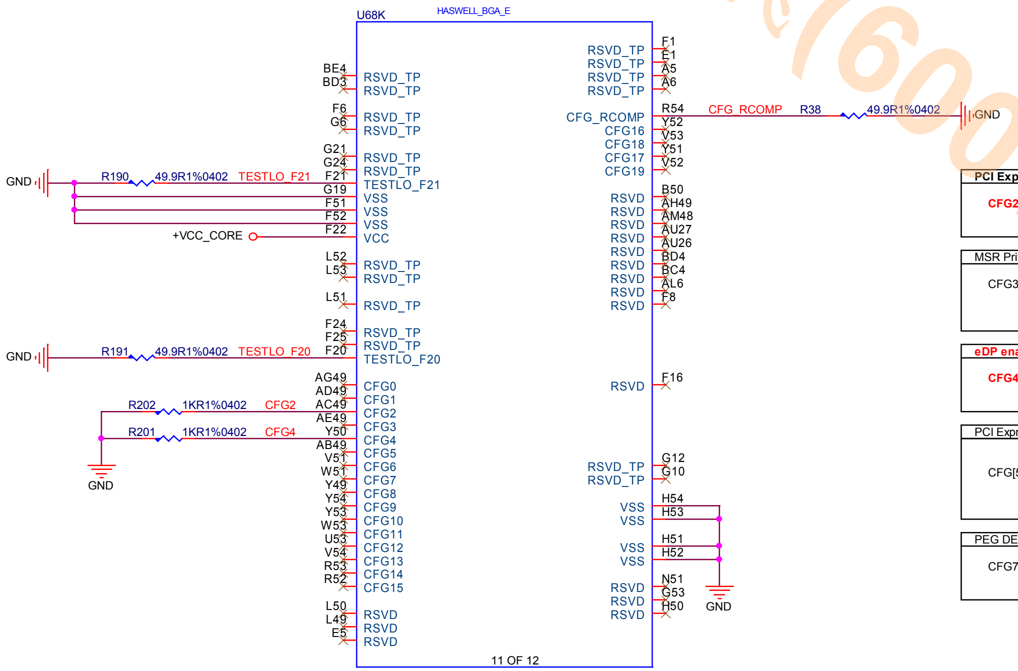
Display/Reserved



To eDP Panal







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

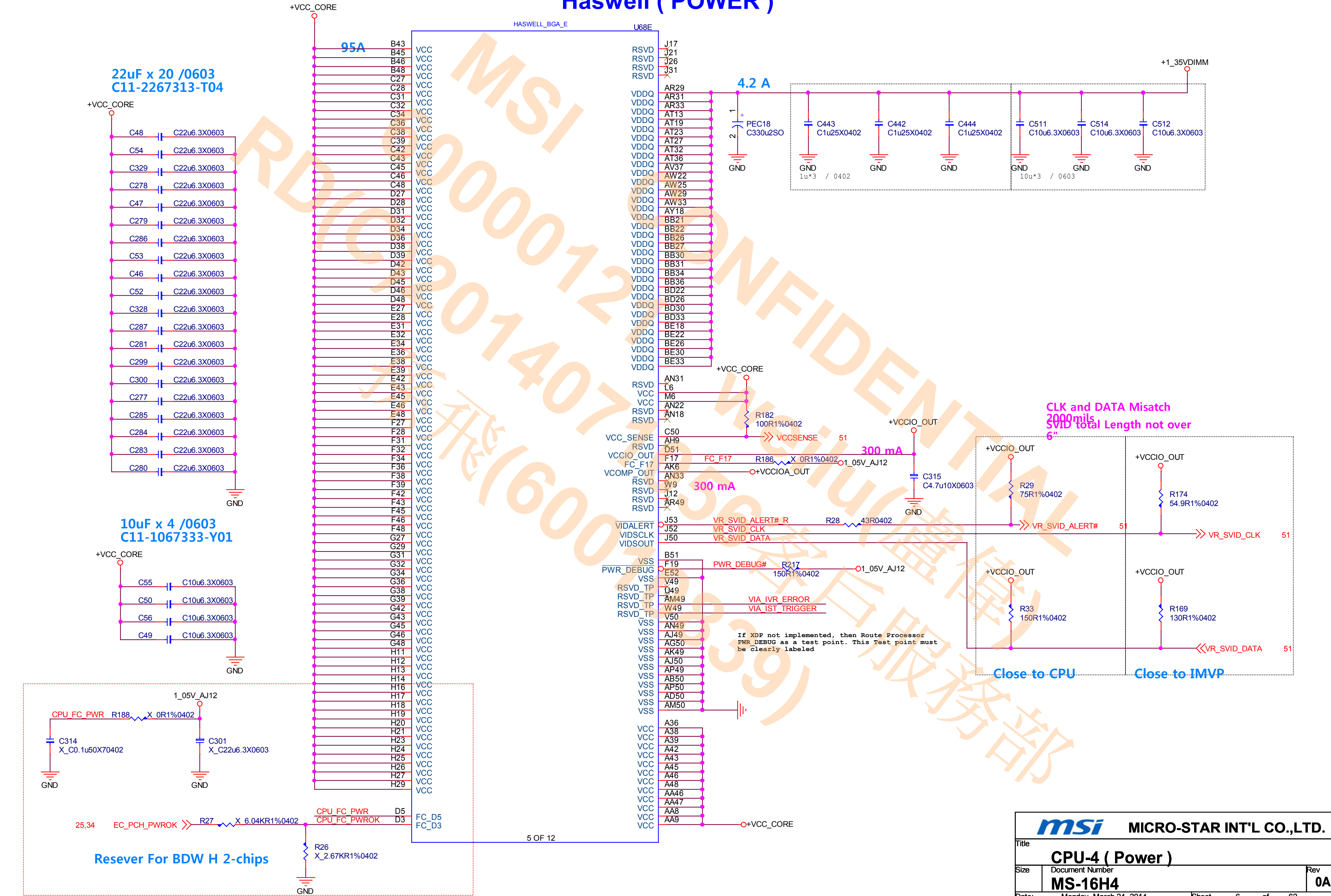
eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

msi	MICRO-STAR INT'L CO.,LTD.	
Title	CPU-3 (Display/Reserved)	
Size	Document Number MS-16H4	Rev 0A
Date: Monday, March 24, 2014	Sheet 5 of 62	

Haswell (POWER)



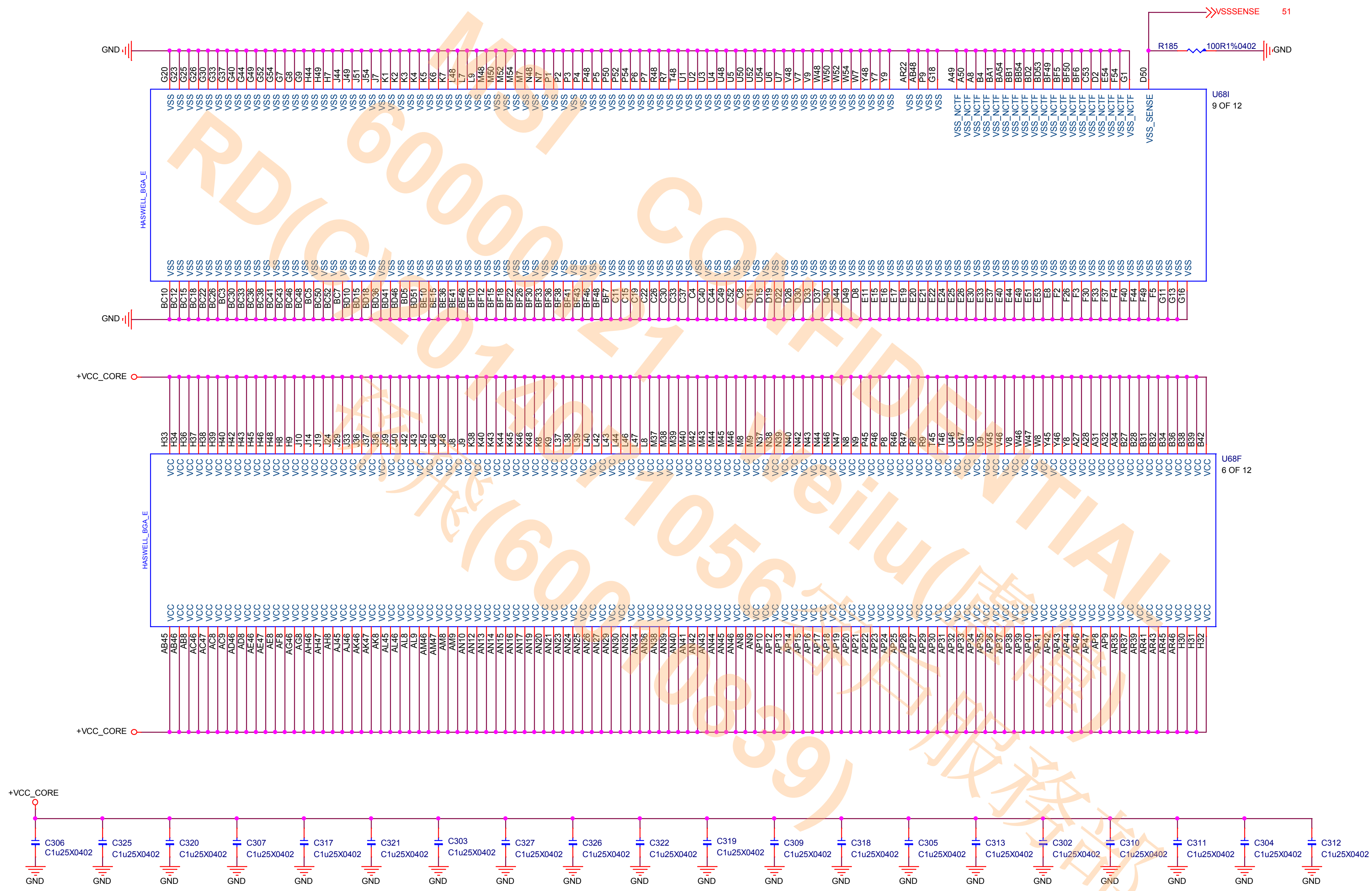
MICRO-STAR INT'L CO.,LTD.

Title: CPU-4 (Power)

Size | Document Number: MS-16H4 | Rev: 0A

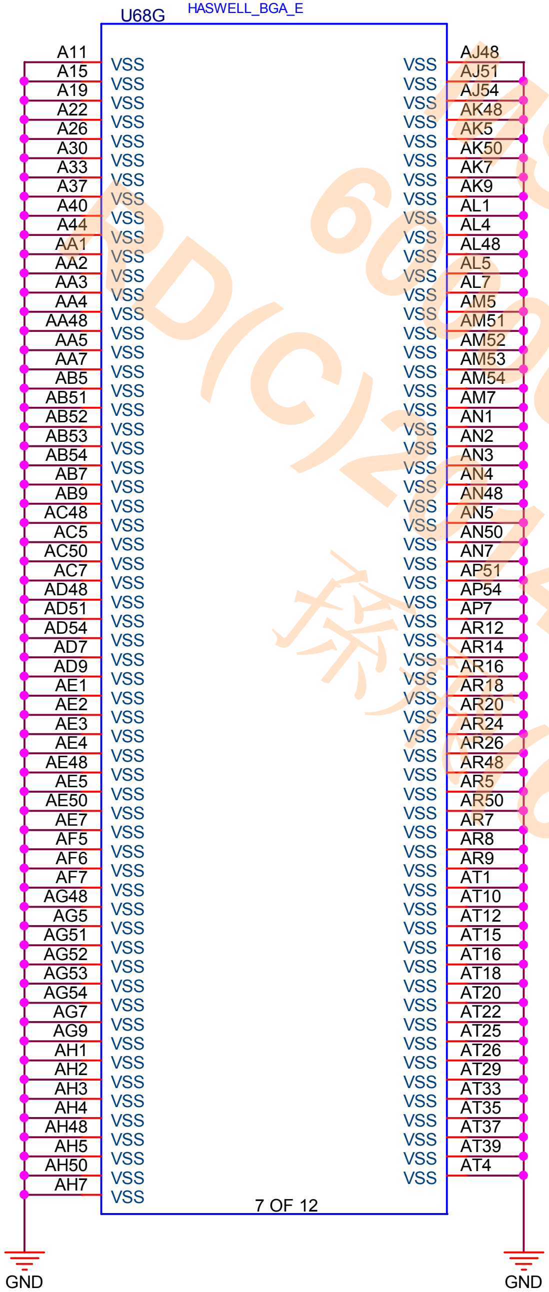
Date: Monday, March 24, 2014 | Sheet 6 of 62

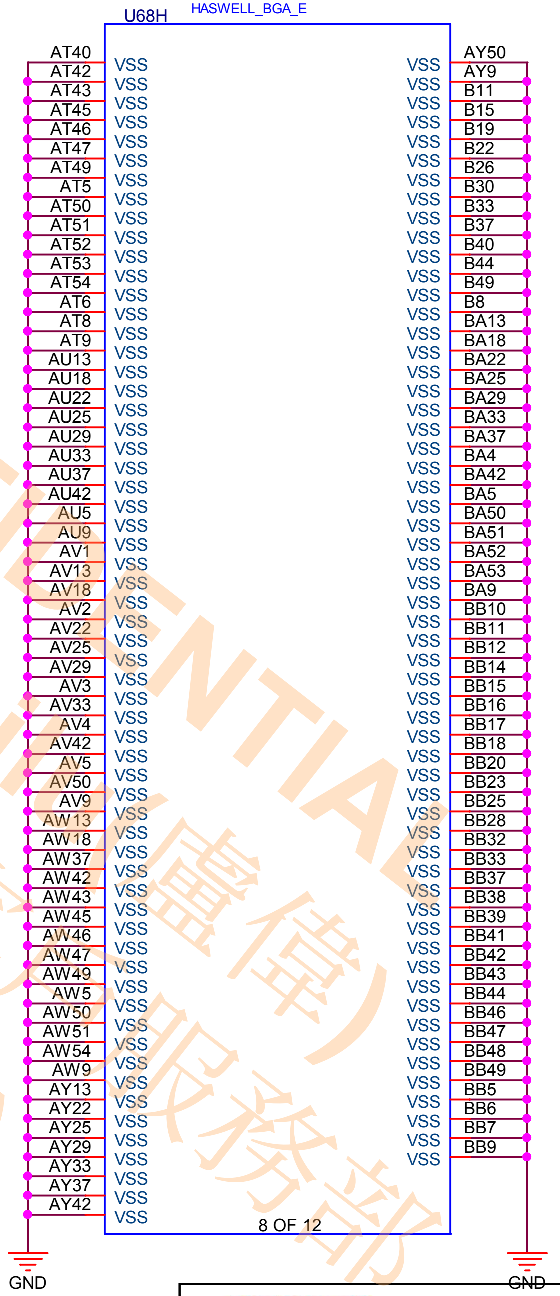
Haswell (Power & GND)



msi	MICRO-STAR INT'L CO.,LTD.	
Title	CPU-6 (Power & GND)	
Size	Document Number MS-16H4	Rev 0A
Date: Monday, March 24, 2014	Sheet 7 of 62	

Haswell (GND)





MICRO-STAR INT'L CO.,LTD.

Title: CPU-5 (GND)

Size	Document Number	Rev
	MS-16H4	0A

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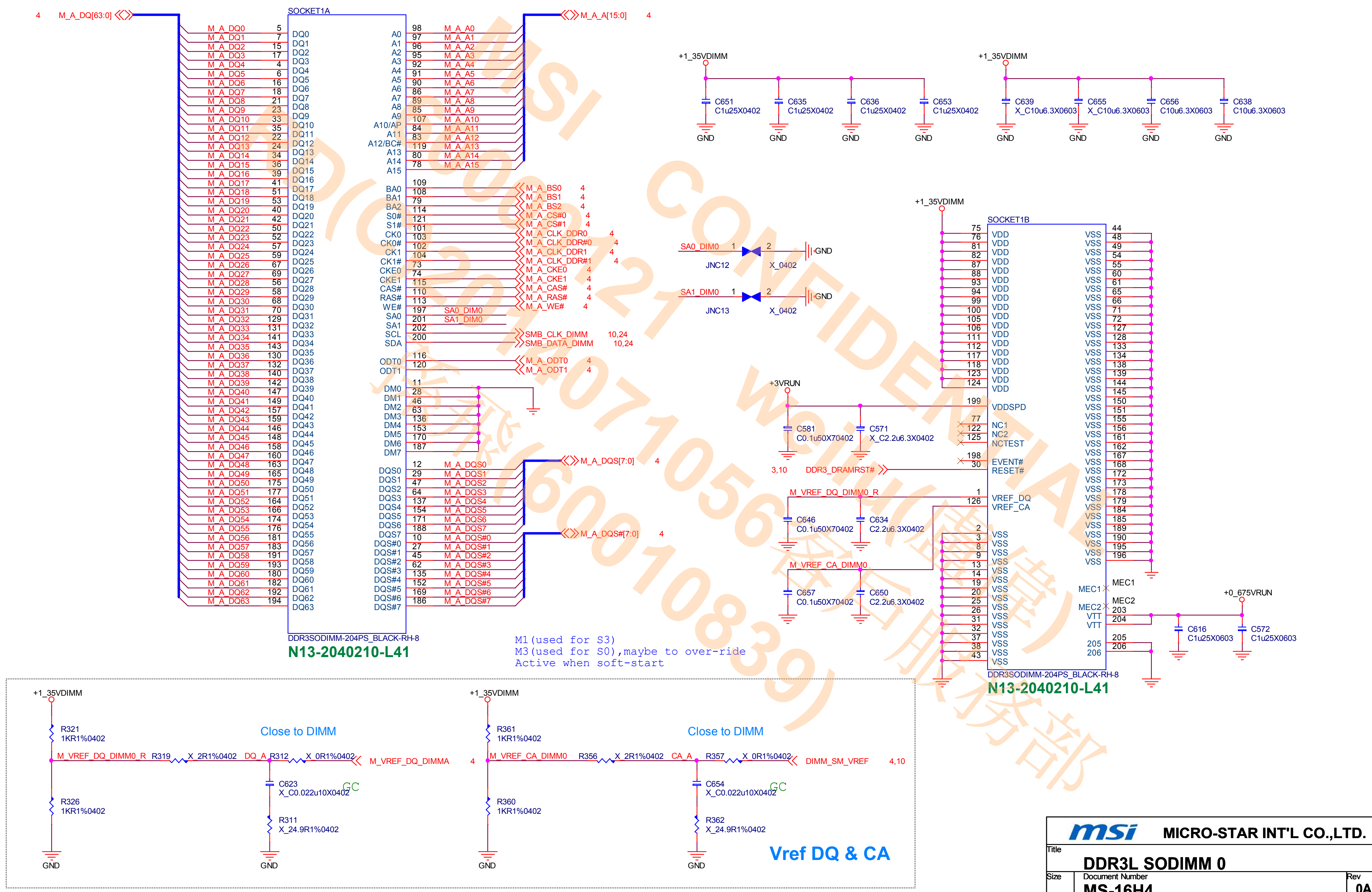
SODIMM#A



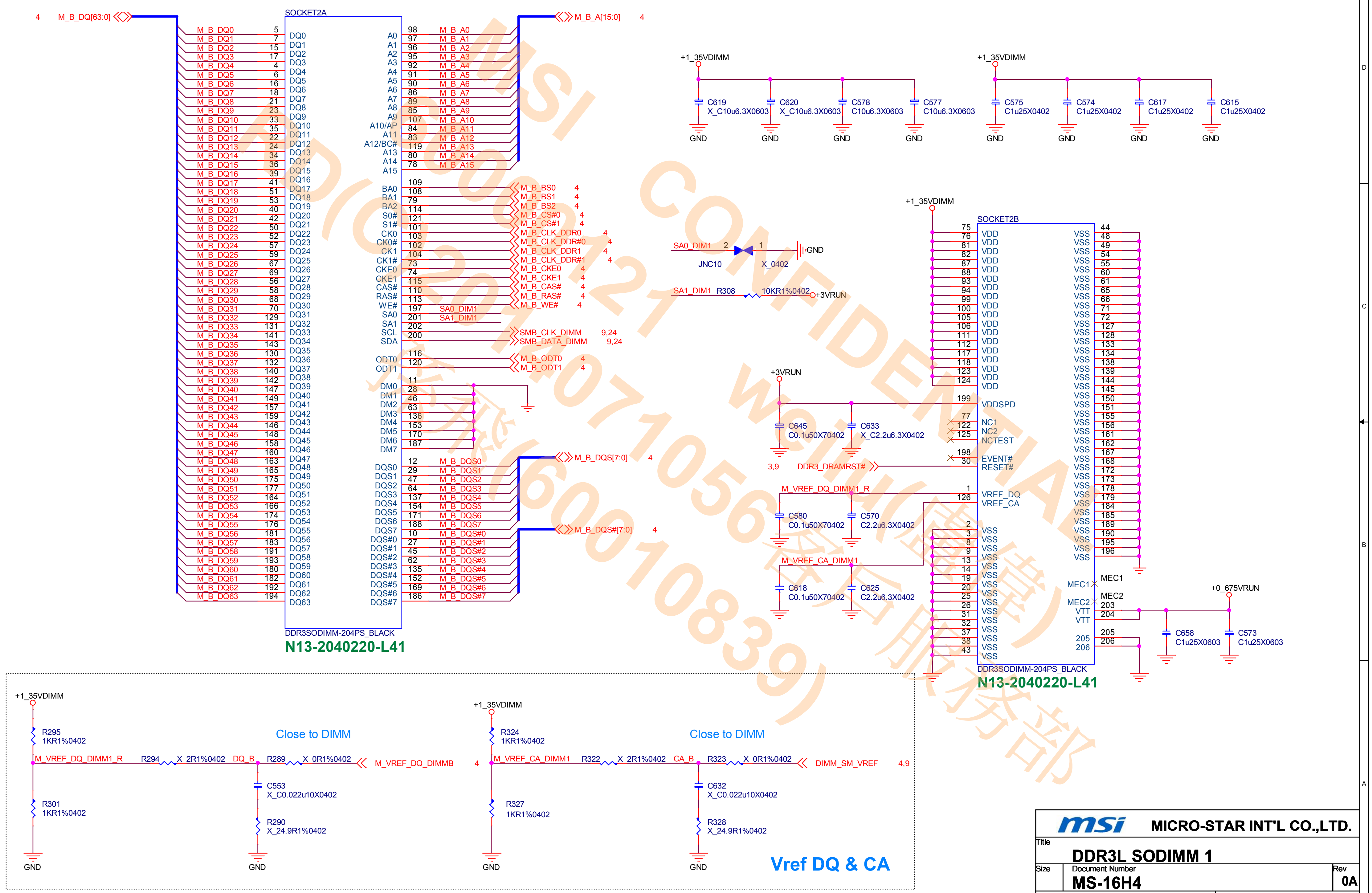
MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 0

Size | Document Number: MS-16H4 | Rev: 0A

Date: Monday, March 24, 2014

SODIMM#B



MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 1

Document Number: MS-16H4 | Rev: 0A

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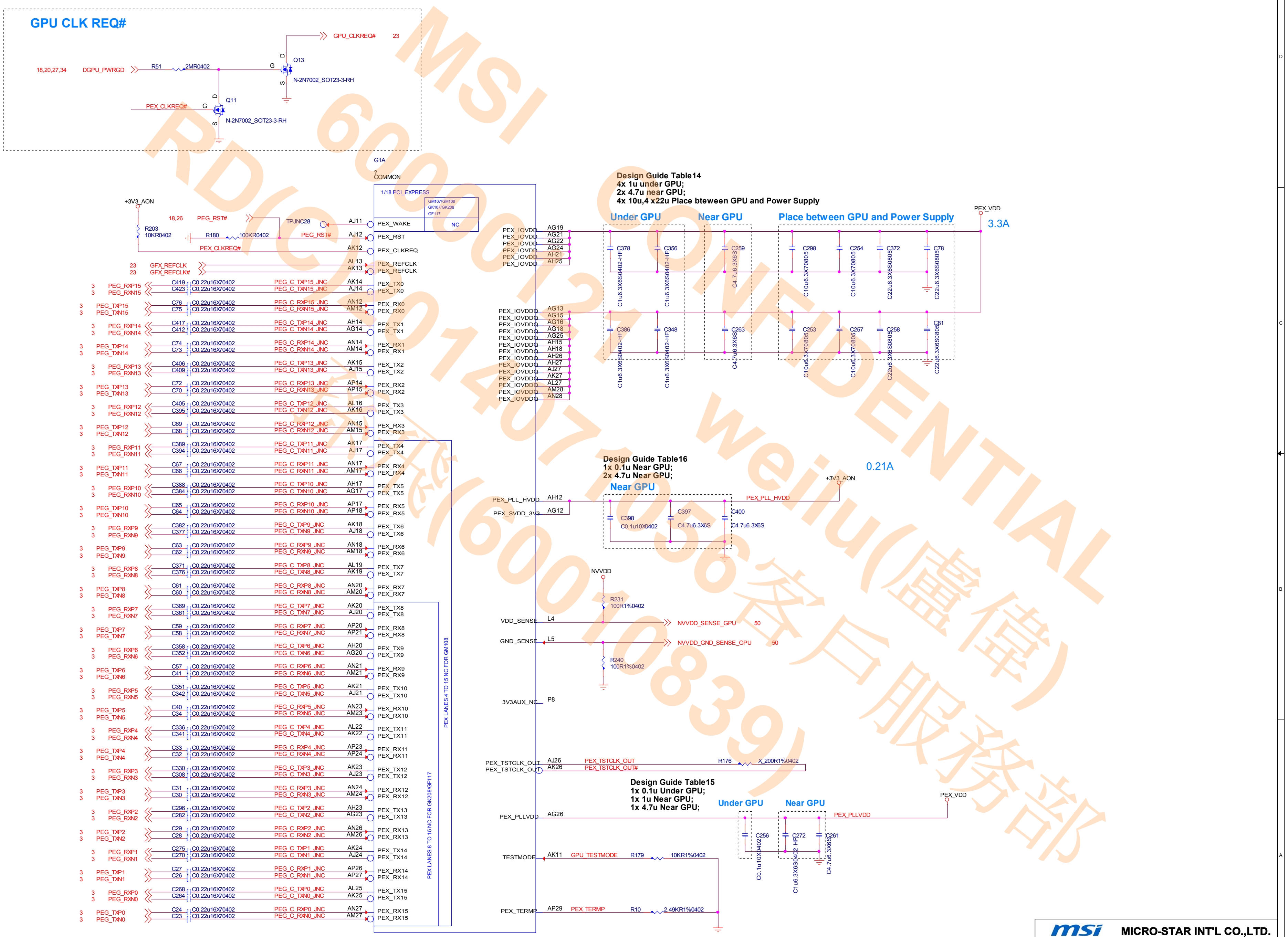
PCI-Express Gen3 x16 Interface



msi MICRO-STAR INT'L CO.,LTD.

Title: DGPU_PCI-E Host

Size | Document Number: MS-16H4 | Rev: 0A

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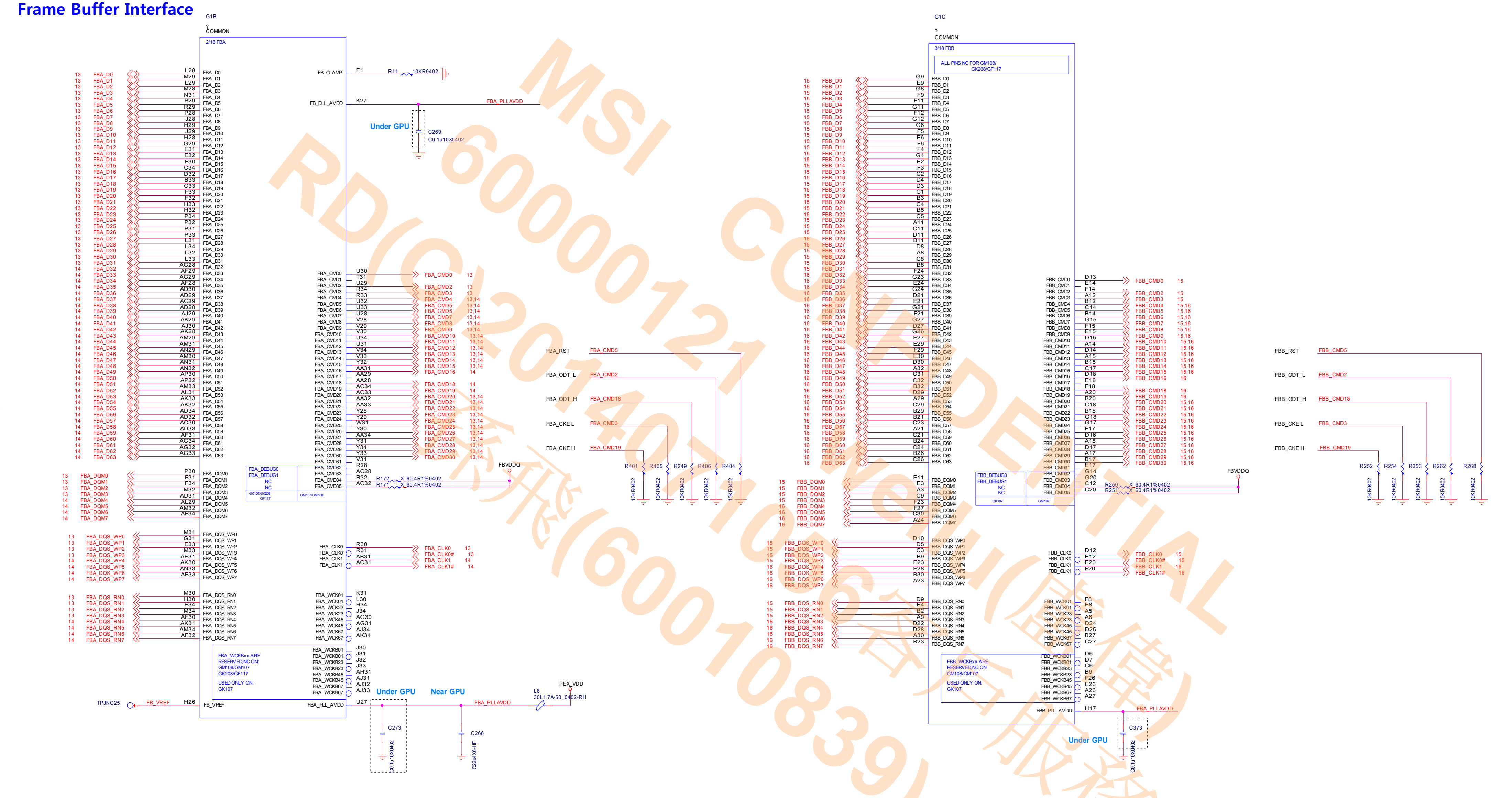
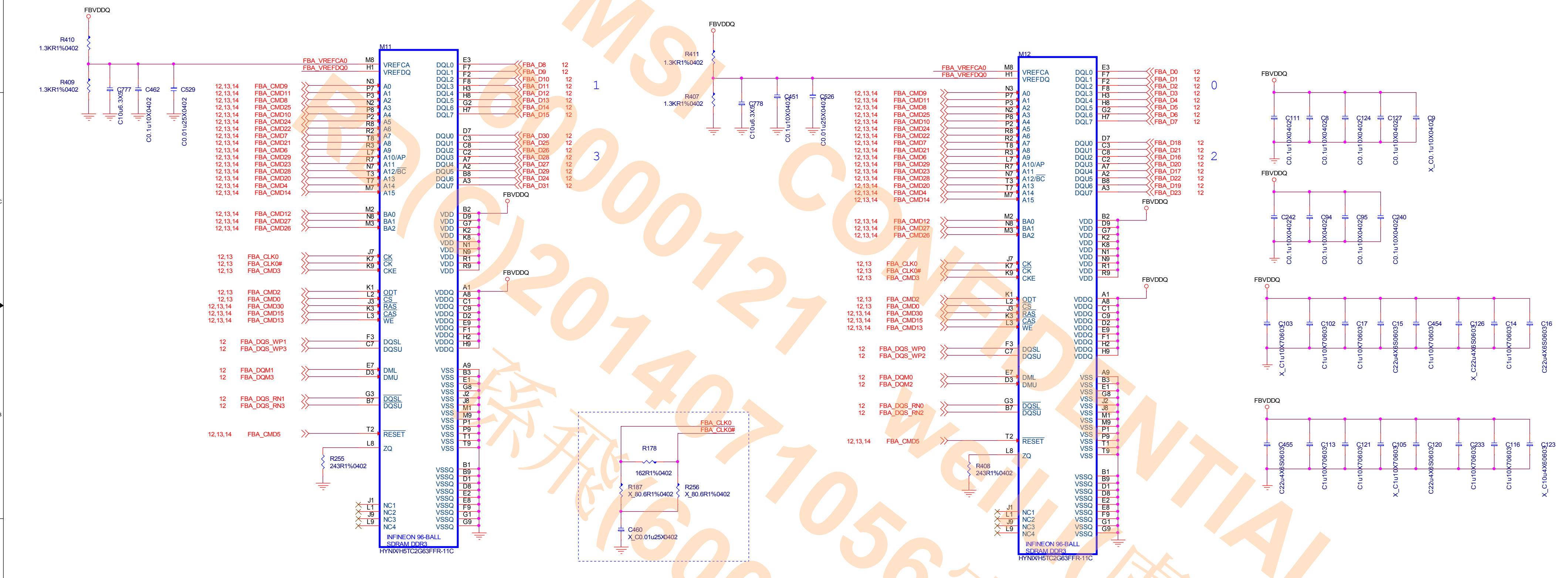
Frame Buffer Interface



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_MEM IF A/B	
Size	Document Number: MS-16H4	Rev: 0A
Date: Monday, March 24, 2014	Sheet 12 of 62	

DDR3 Frame A-1



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_DDR3 FrameBuffer A1
Size / Document Number	MS-16H4
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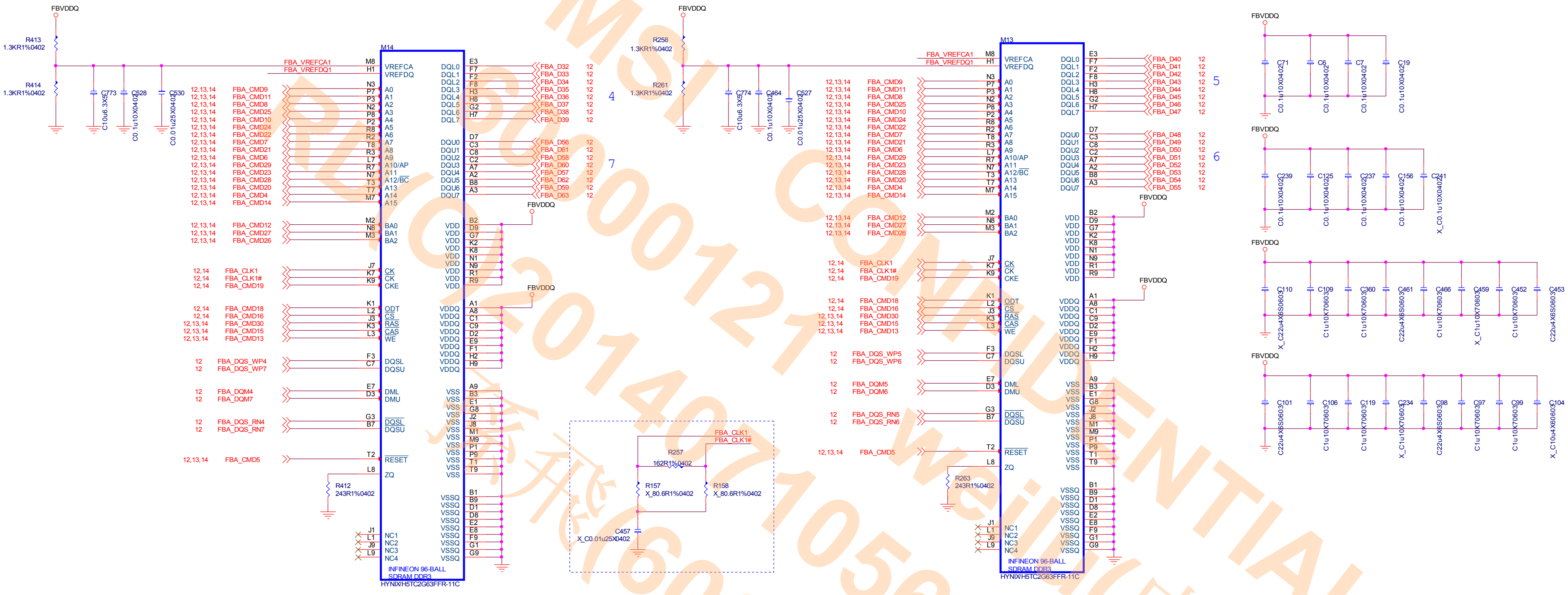
DDR3 Frame A-2



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_DDR3 FrameBuffer A2	
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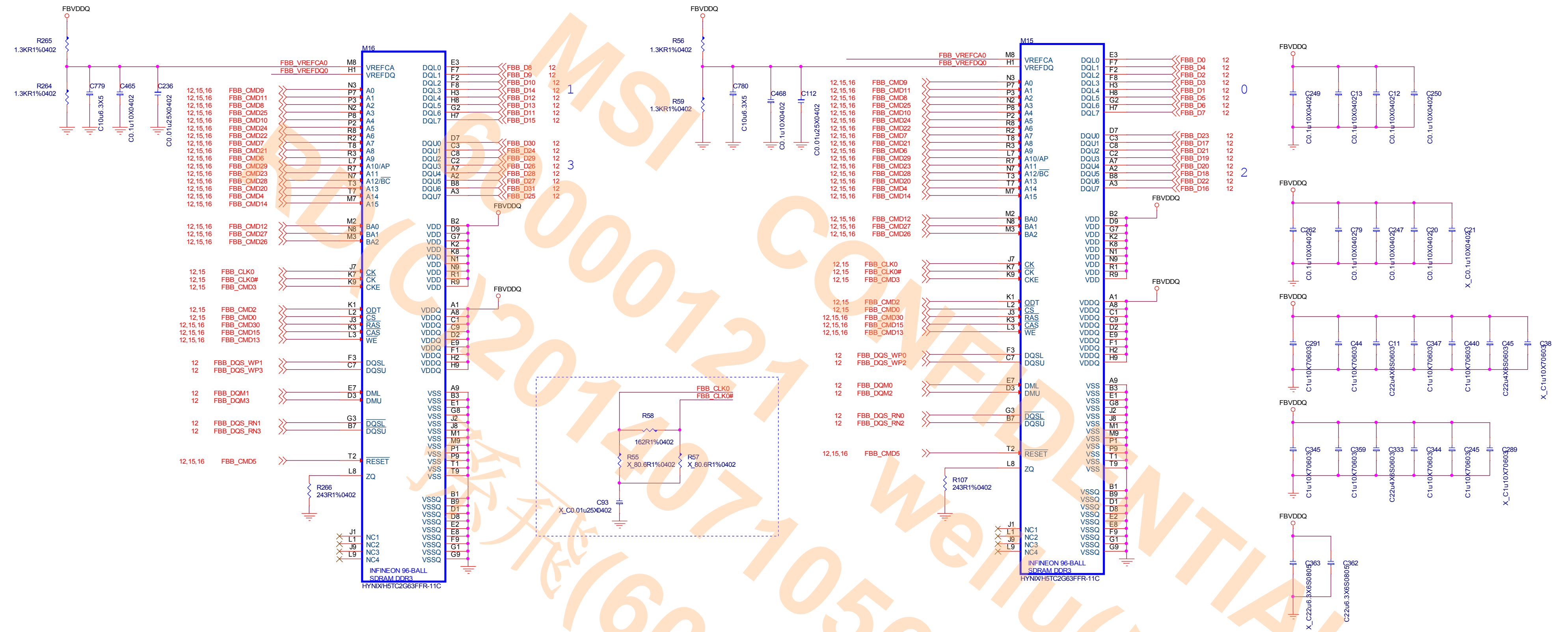
DDR3 Frame B-1



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_DDR3 FrameBuffer B1	
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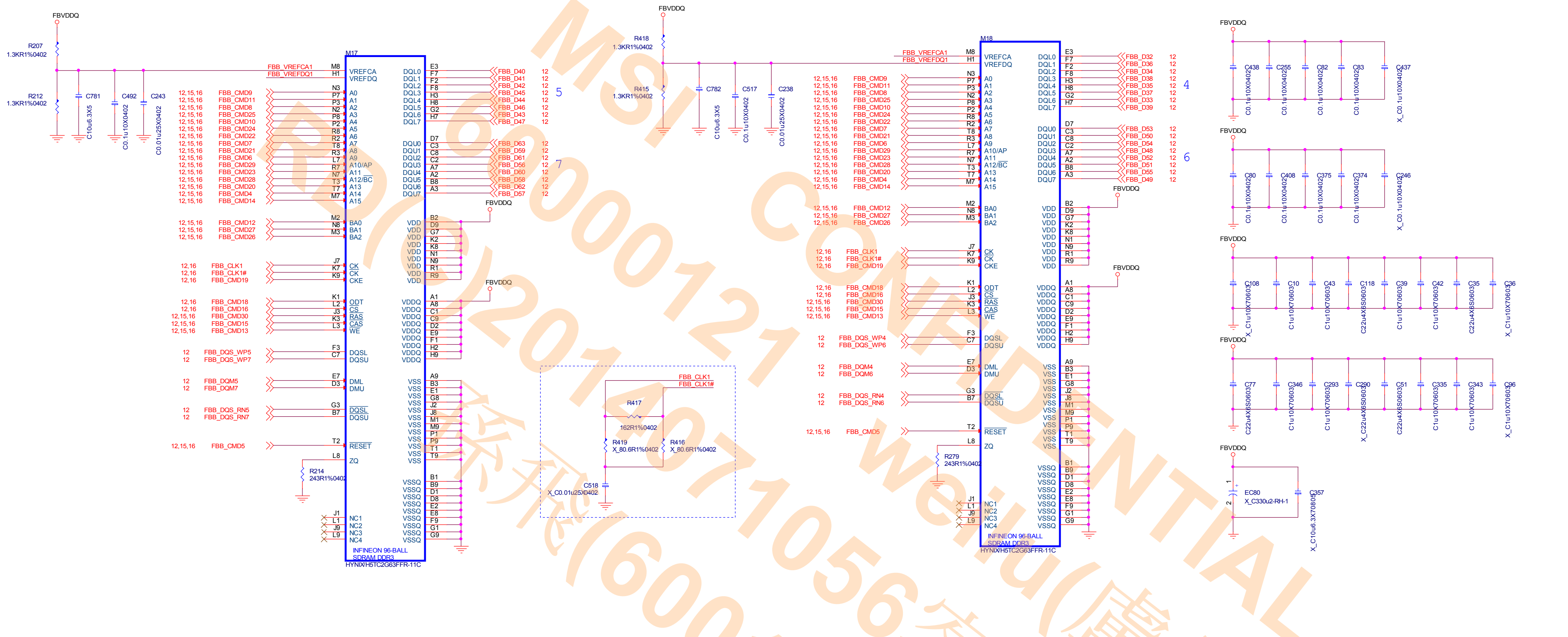
DDR3 Frame B-2



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_DDR3 FrameBuffer B2	
Size	Document Number: MS-16H4	Rev: 0A
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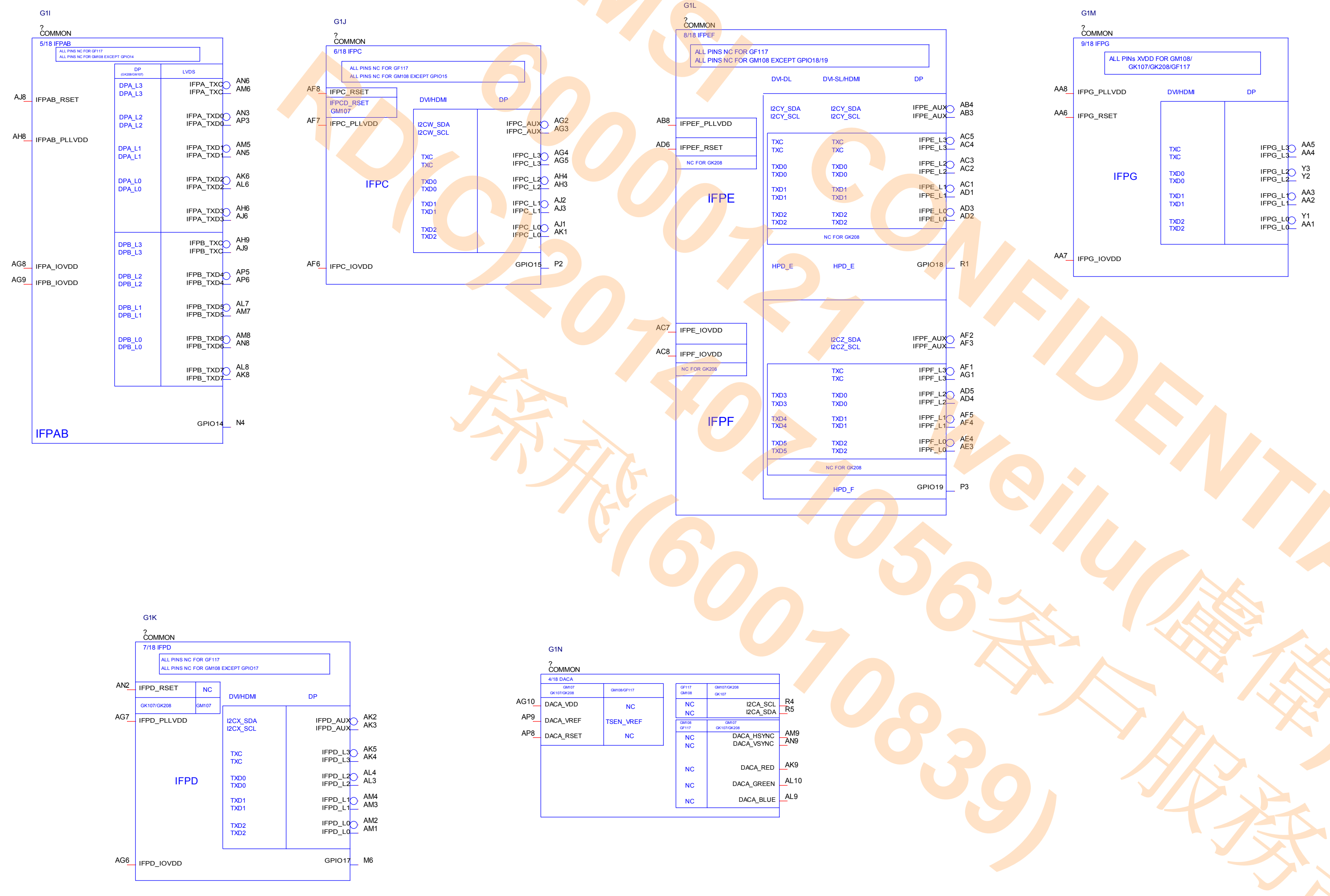
Display IF

IFP A/B LVDSDual Link | **IFP C Native HDMI OR DP** | **IFP E/F Dual Link TMDS DVI-I** | **DAC A VGA**



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_Display IF	
Size	Document Number: MS-16H4	Rev: 0A
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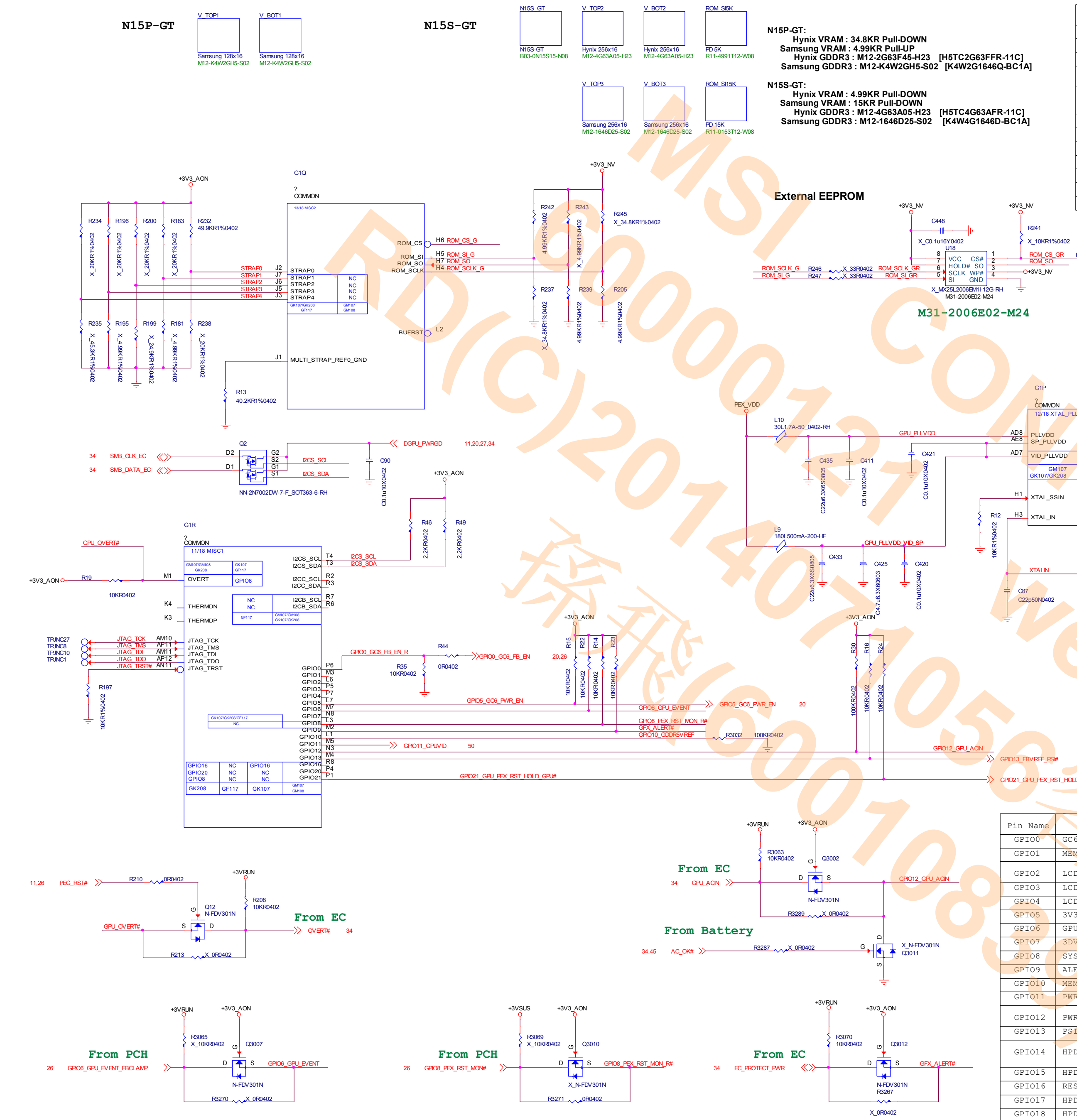


N15P-GT:
Hynix VRAM : 34.8KR Pull-DOWN
Samsung VRAM : 4.99KR Pull-UP
Hynix GDDR3 : M12-2G63F45-H23 [H5TC2G63FFR-11C]
Samsung GDDR3 : M12-K4W2GH5-S02 [K4W2G1646Q-BC1A]

N15S-GT:
Hynix VRAM : 4.99KR Pull-DOWN
Samsung VRAM : 15KR Pull-DOWN
Hynix GDDR3 : M12-4G63A05-H23 [H5TC4G63AFR-11C]
Samsung GDDR3 : M12-1646D25-S02 [K4W4G1646D-BC1A]

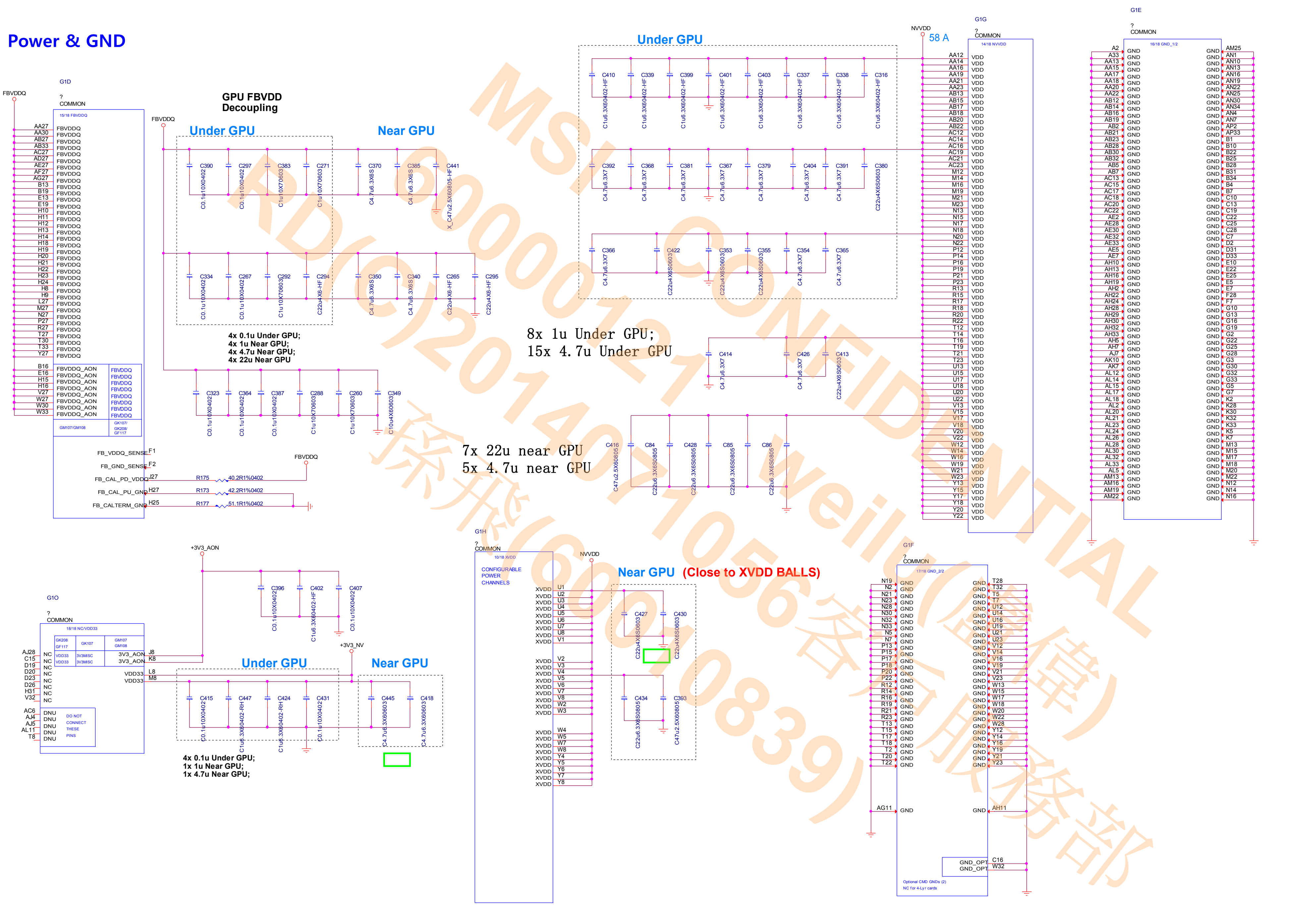
External EEPROM

M31-2006E02-M24

Item	Location	N15P-GT	N15S-GT
Device ID		0x1391	0x1341
Package		GB4-128	GB4-128
Memory Type		DDR3	DDR3
Device Specific Strap Mode Selection	R13	Multi_Strap_Ref0_GND,40.2K PD to GND	Multi_Strap_Ref0_GND,40.2K PD to GND
ROM_SI	R237	0x6, Hynix 2G, 34.8kohm pull down	0x0, Hynix 2G, 4.99kohm pull down
	R242	0x8, Samsung 2G, 4.99Kohm pull up	0x2, Samsung 2G, 15Kohm pull down
ROM_SO	R329	4.99Kohm pull down	4.99Kohm pull down
ROM_SCLK	R305	4.99Kohm pull down	4.99Kohm pull down
Strap0	R232	49.9Kohm pull up	49.9Kohm pull up
Strap1		NC	NC
Strap2		NC	NC
Strap3		NC	NC
Strap4		NC	NC

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GC6_FB_EN(GPIO0_GC6_FB_EN)	O	FB Enable for GC6 2.0	10K pull-down
GPIO1	MEM_VDD_CTL(NC)	O	Memory VDD VID	
GPIO2	LCD_BL_PWM(NC)	O	Panel Backlight PWM Brighteness Control	
GPIO3	LCD_VCC(NC)	O	Panel Power Enable	
GPIO4	LCD_BLEN(NC)	O	Panel Backlight Enable	
GPIO5	3V3_MAIN_EN(GPIO5_GC6_PWR_EN)	O	GPU POWER Sequencing	10K pull-up to 3V3 _AON
GPIO6	GPU_EVENT#(GPIO6_GPU_EVENT_FBCLAMP)	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3 _AON
GPIO7	3DVision(NC)	O	3D Vision L/R signal	
GPIO8	SYS_PEX_RST_MON#(GPIO8_PEX_RST_MON#)	I	System side PCI reset Monitor	10K pull-up to 3V3 _AON
GPIO9	ALERT(EC_PROTECT_PWR)	I/O	Active Low Thermal Alert	10K pull-up to 3V3 _AON
GPIO10	MEM_VREF_CTL(GPIO10_GDDR5VREF)	O	Memory VREF Control	100K pull-down
GPIO11	PWR_VID(GPIO11_GPUVID)	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL(GPIO12_GPU_ACIN)	I	AC power detect or power supply overdraw input	100K pull-up to 3V3 _AON
GPIO13	PSI(GPIO13_FBVREF_PSI#)	O	Phase shedding	10K pull-up to 3V3 _AON
GPIO14	HPD_A(NC)	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	
GPIO15	HPD_C(NC)	I	Hot Plug Detect for IFPC	
GPIO16	RESERVED			
GPIO17	HPD_D(NC)	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E(NC)	I	Hot Plug Detect for IFPE	
GPIO19	HPD_F or HPD_B(NC)	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	
GPIO20	RESERVED			
GPIO21	GPU_PEX_RST_HOLD (GPIO21_GPU_PEX_RST_HOLD_GPU#)	O	GPU PCIE self-reset control	10K pull-up to 3V3 _AON
OVERT	OVERT(OVERT#)	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3 _AON

Power & GND



msi	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_Power & GND
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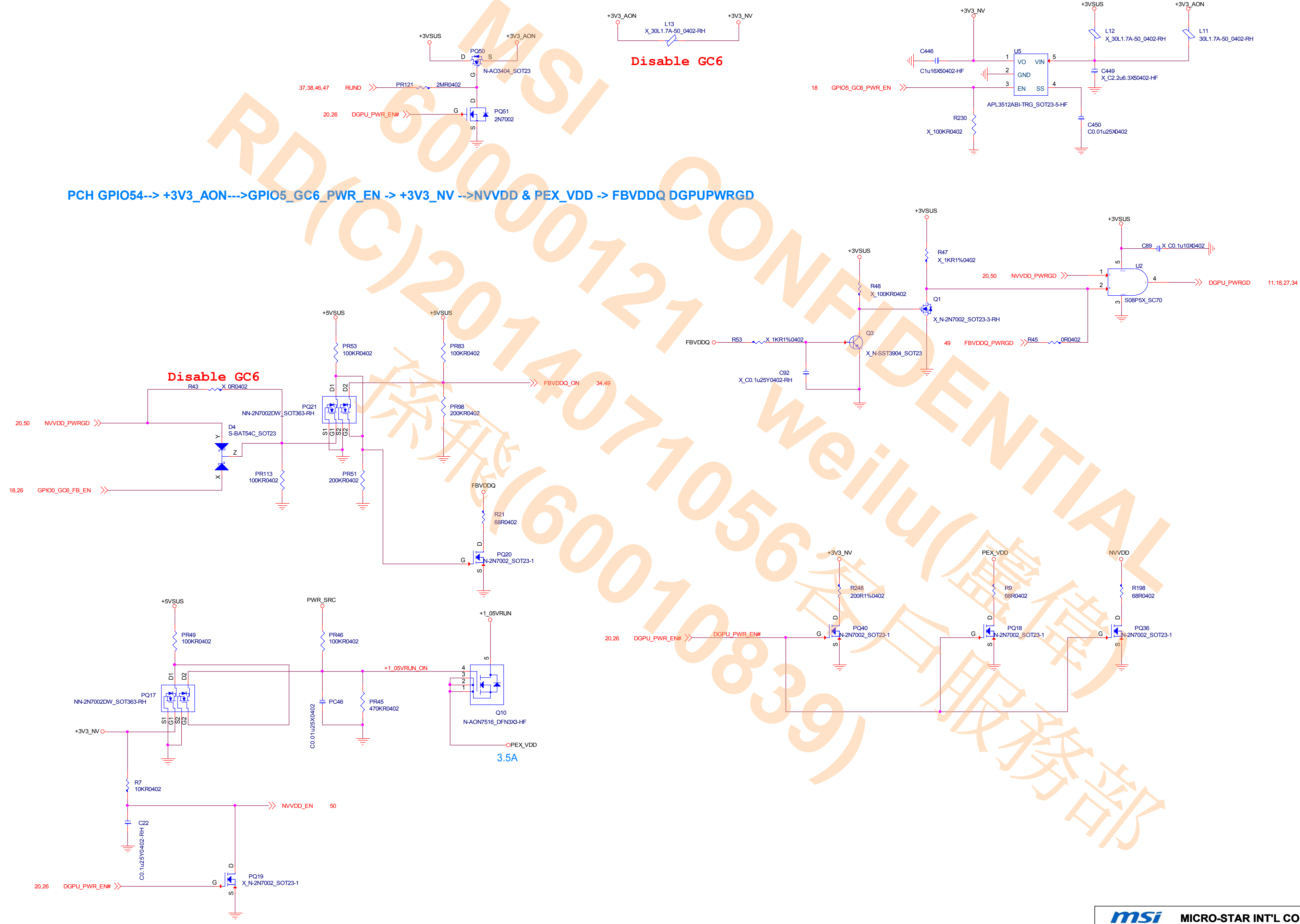
Power Control



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_Power Control	
Size	Document Number MS-16H4	Rev 0A
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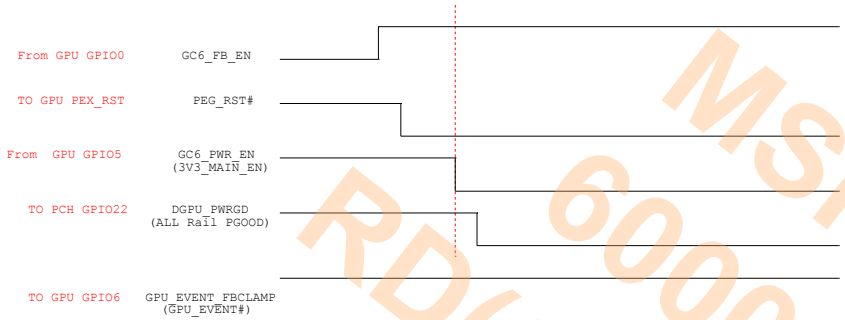
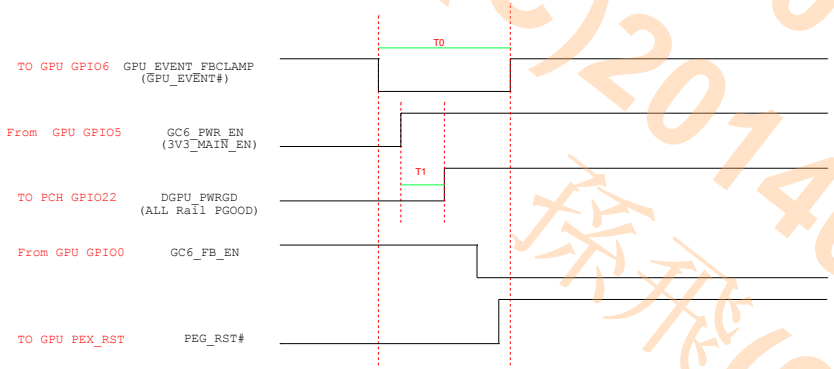
GC6 2.0 ENTRY SEQUENCE



GC6 2.0 EXIT SEQUENCE



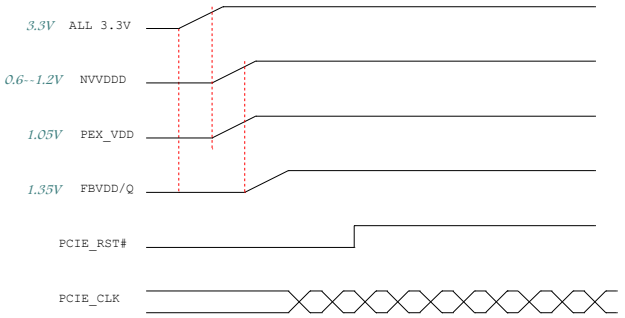
GC6 2.0 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
   If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

GPU POWER ON SEQUENCE



NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltagr.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up.
   NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_POWER SEQUENCE

Size | Document Number: MS-16H4 | Rev: 0A

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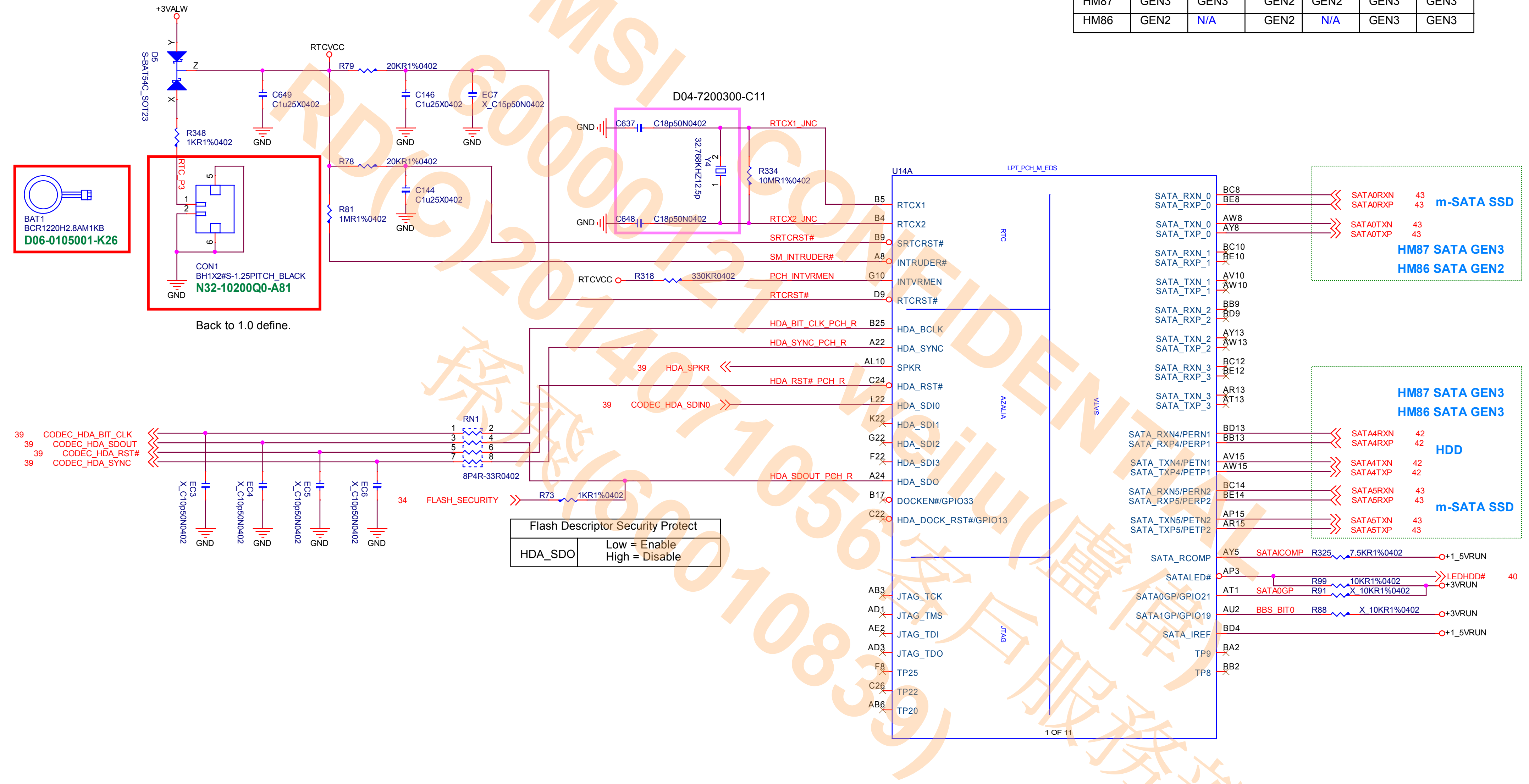
Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-1 (HDA/JTAG/SATA)		
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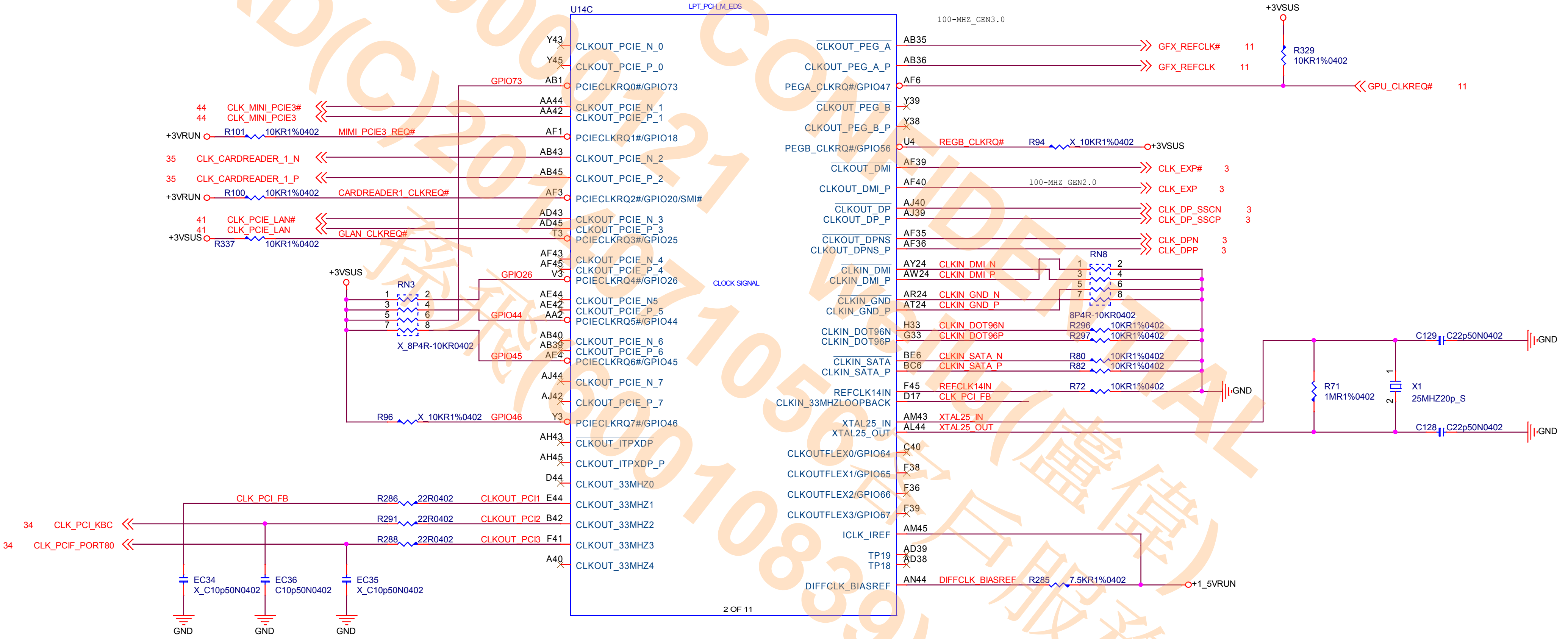
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k ∮10% external pull-up resistor instead of No Connect.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.

Title	PCH-2 (CLK)	
Size	Document Number: MS-16H4	Rev: 0A
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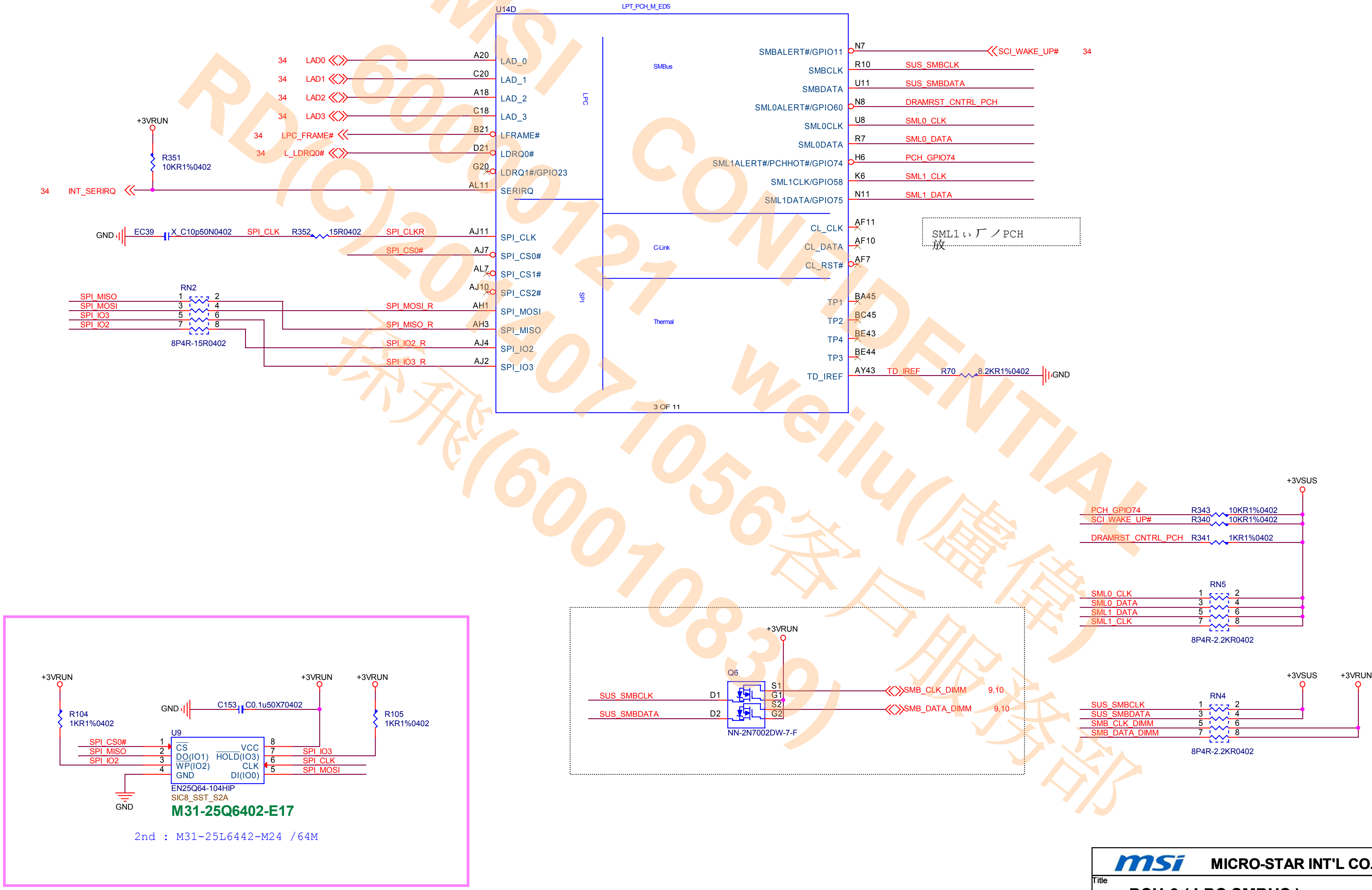
Lynx Point (LPC,SMBUS)



MSI MICRO-STAR INT'L CO.,LTD.

Title	PCH-3 (LPC,SMBUS)	
Size	Document Number MS-16H4	Rev 0A
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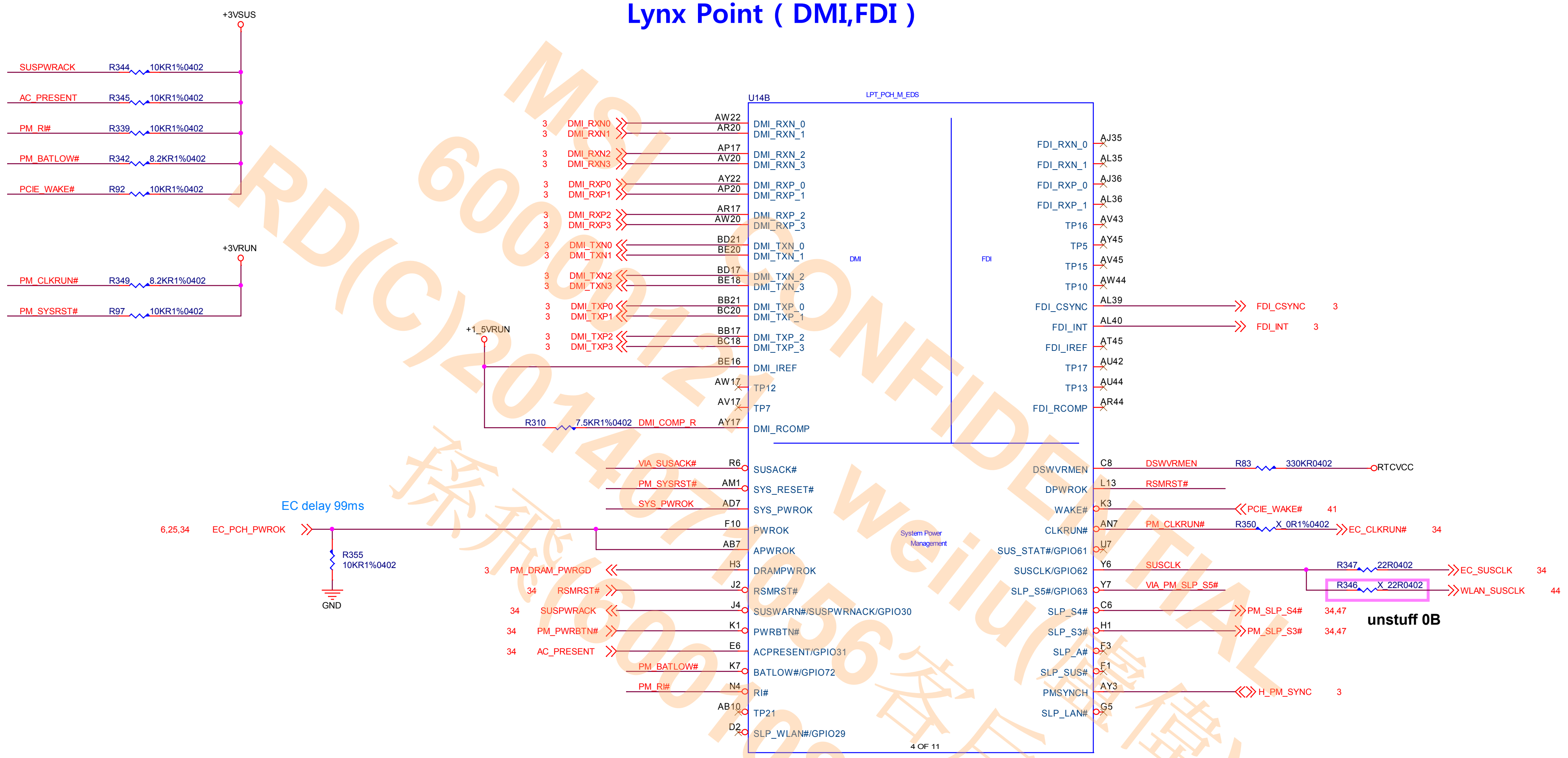
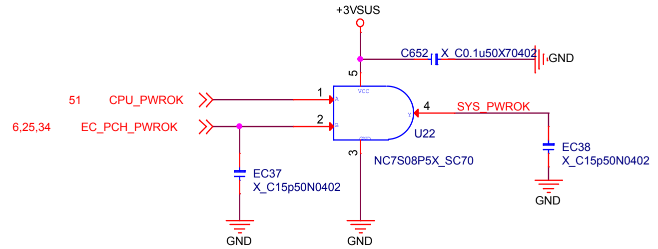
Lynx Point (DMI,FDI)



GPIO Setting : Ref 486708_LPT_EDS Section2.18



APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

msi	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-4 (DMI,FDI)	
Size	Document Number MS-16H4	Rev 0A
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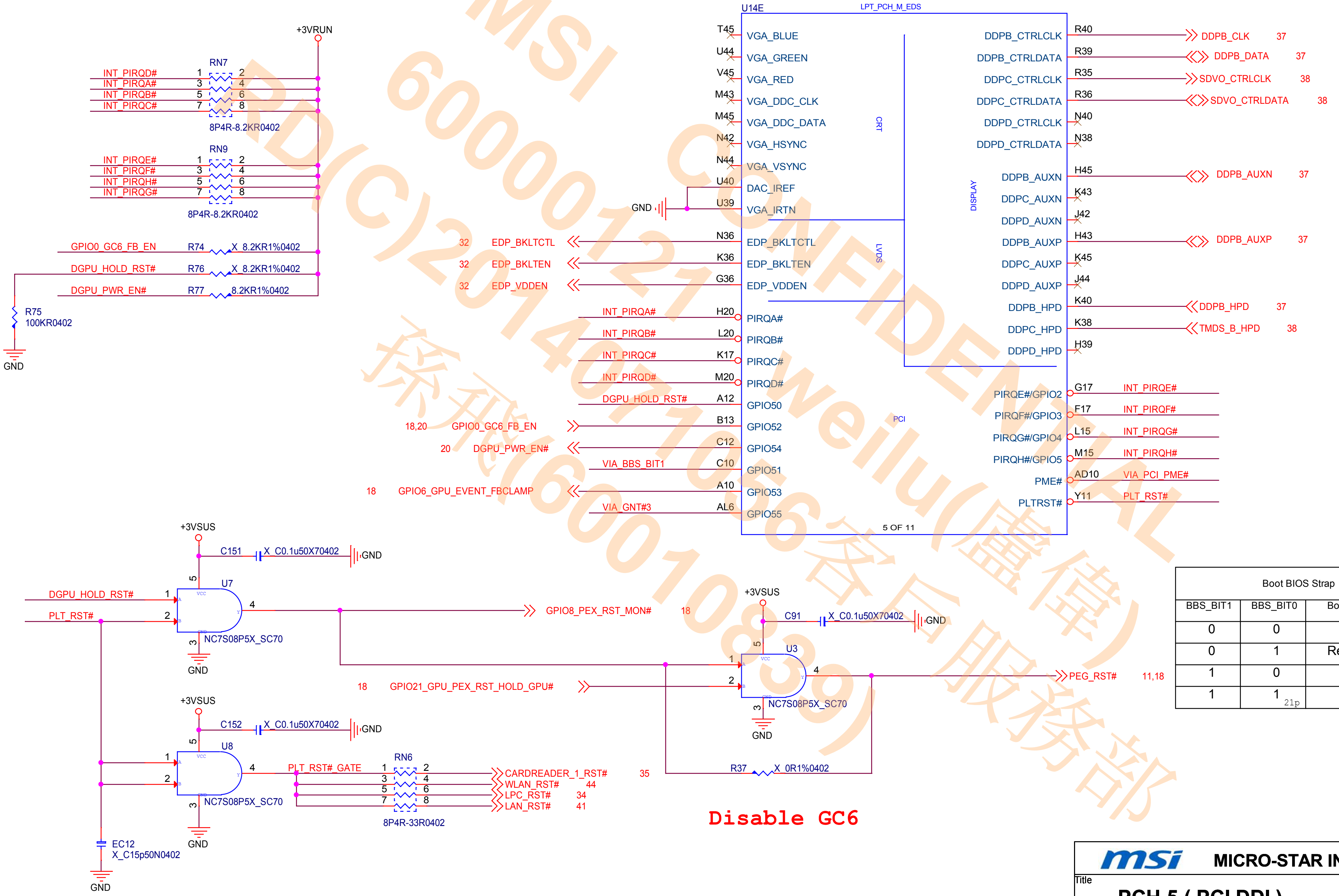
Lynx Point (PCI,DDI)



DDI-B : DP
DDI-C : HDMI

Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

Disable GC6

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

Size | Document Number: MS-16H4 | Rev: 0A

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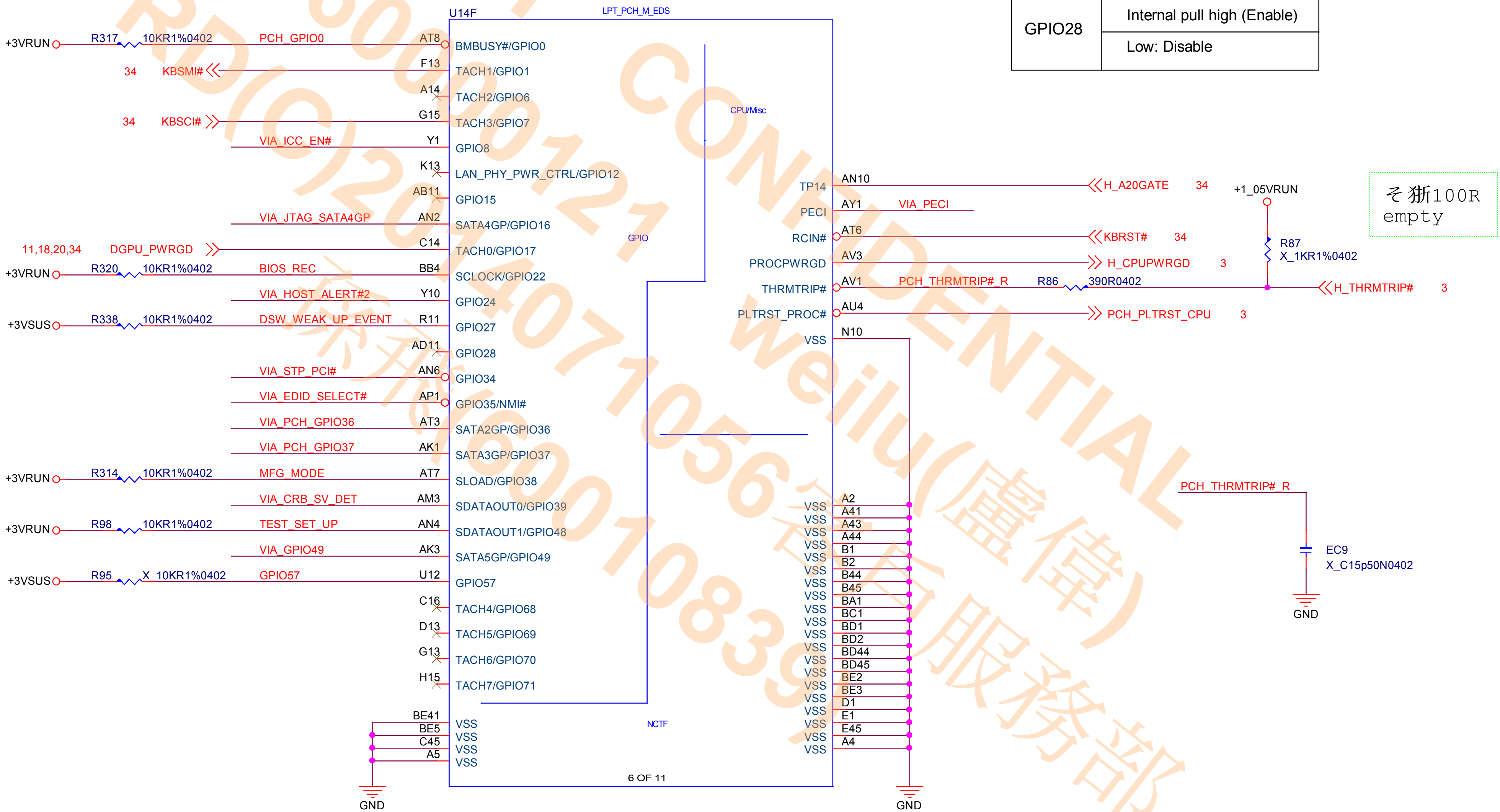
Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

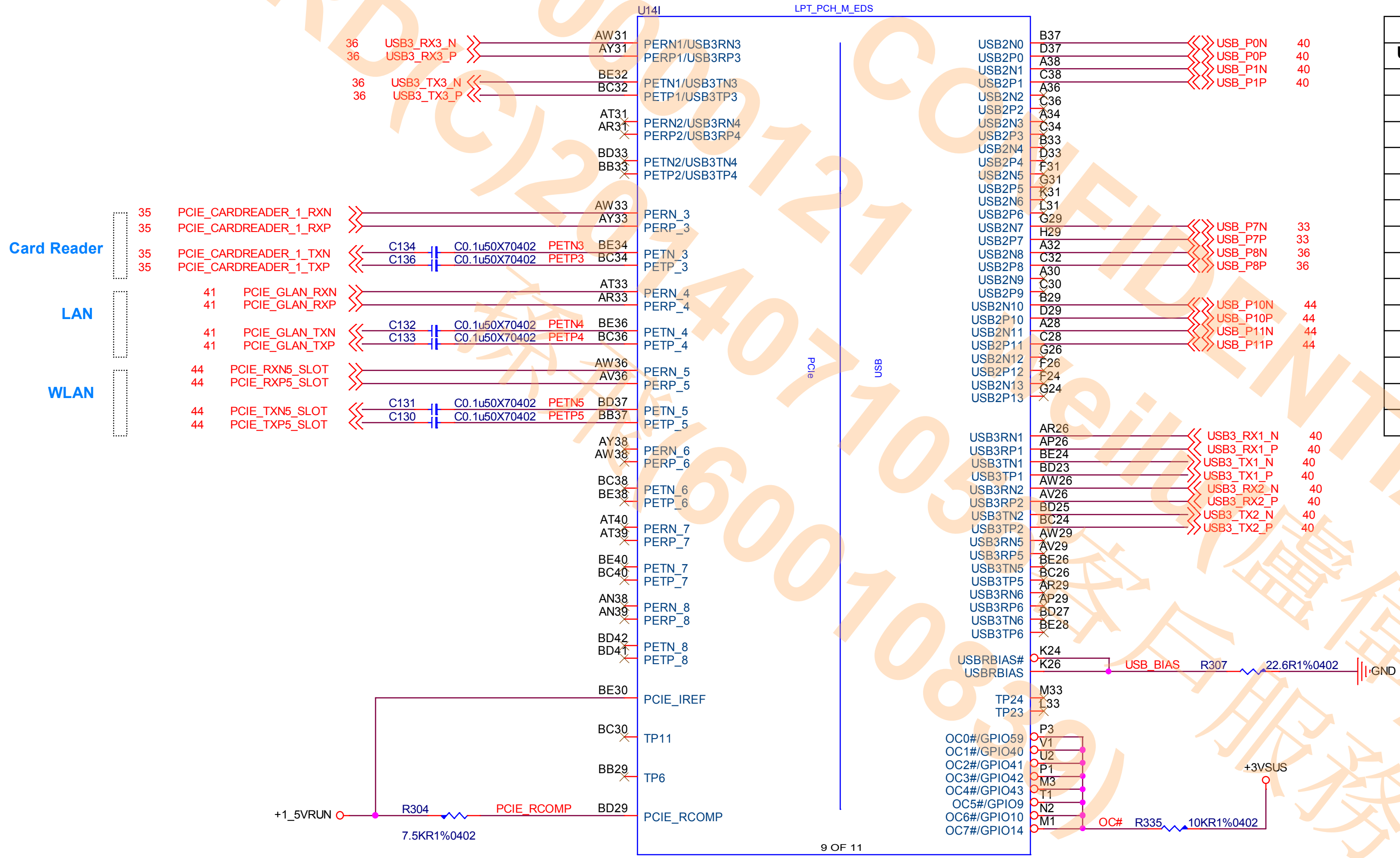
PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



MICRO-STAR INT'L CO.,LTD.		
Title: PCH-6 (GPIO,MISC)		
Size	Document Number: MS-16H4	Rev: 0A
Date: Monday, March 24, 2014		Sheet 27 of 62

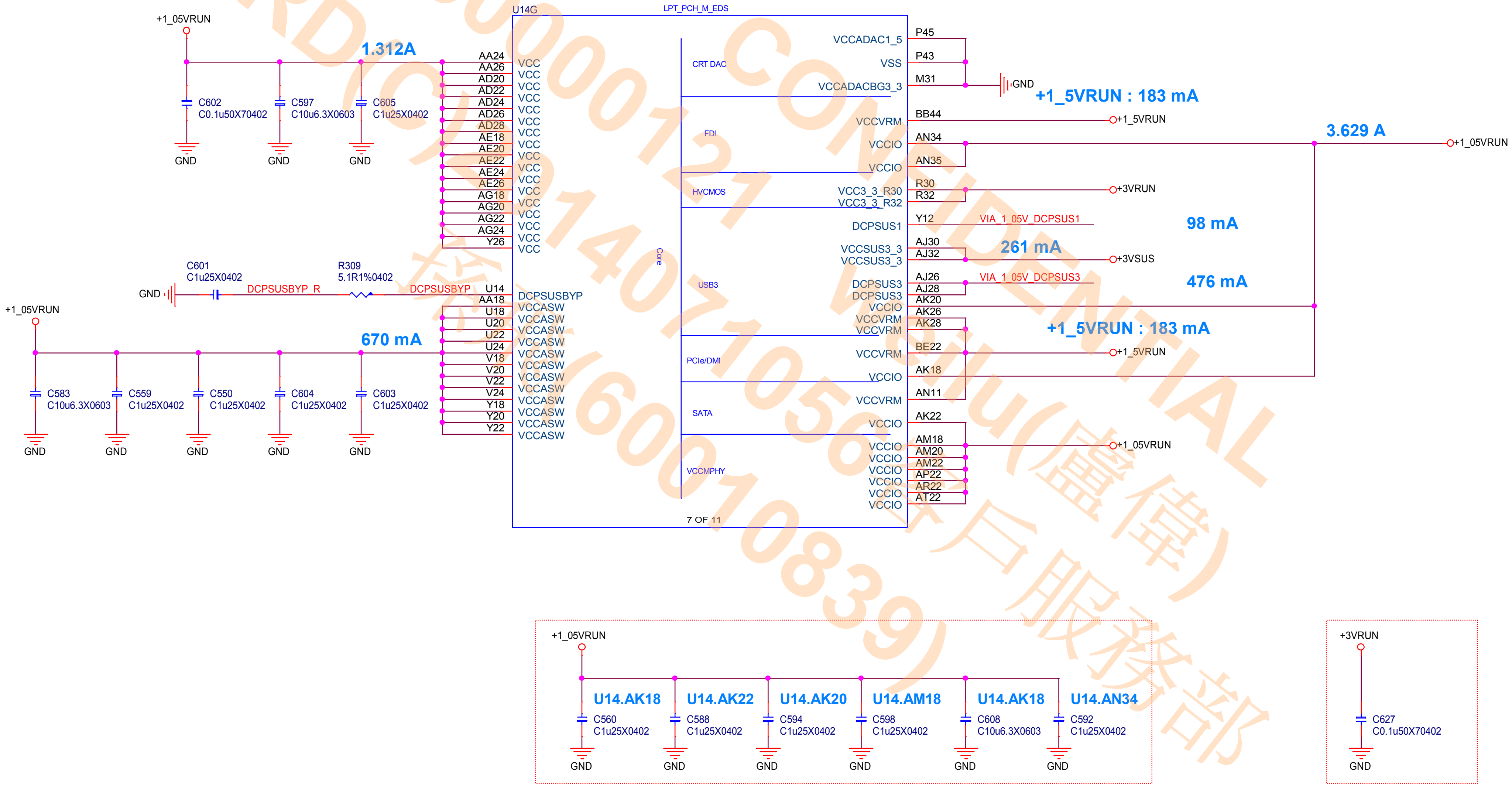
Lynx Point (PCIE,USB)

SKU	USB3.0					
	Port-1	Port-2	Port-3	Port-4	Port-5	Port-6
HM87	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0
HM86	USB3.0	USB3.0	USB3.0	USB3.0	N/A	N/A



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H4A
1	2	USB 3.0 Port 2	16H4A
2			NC
3			NC
4			NC
5			NC
6			NC
7		EPF021	
8	3	USB 3.0 Port 3	16H41
9			NC
10		WLAN	
11		WebCam	
12			NC
13			NC

Lynx Point (Power)



MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

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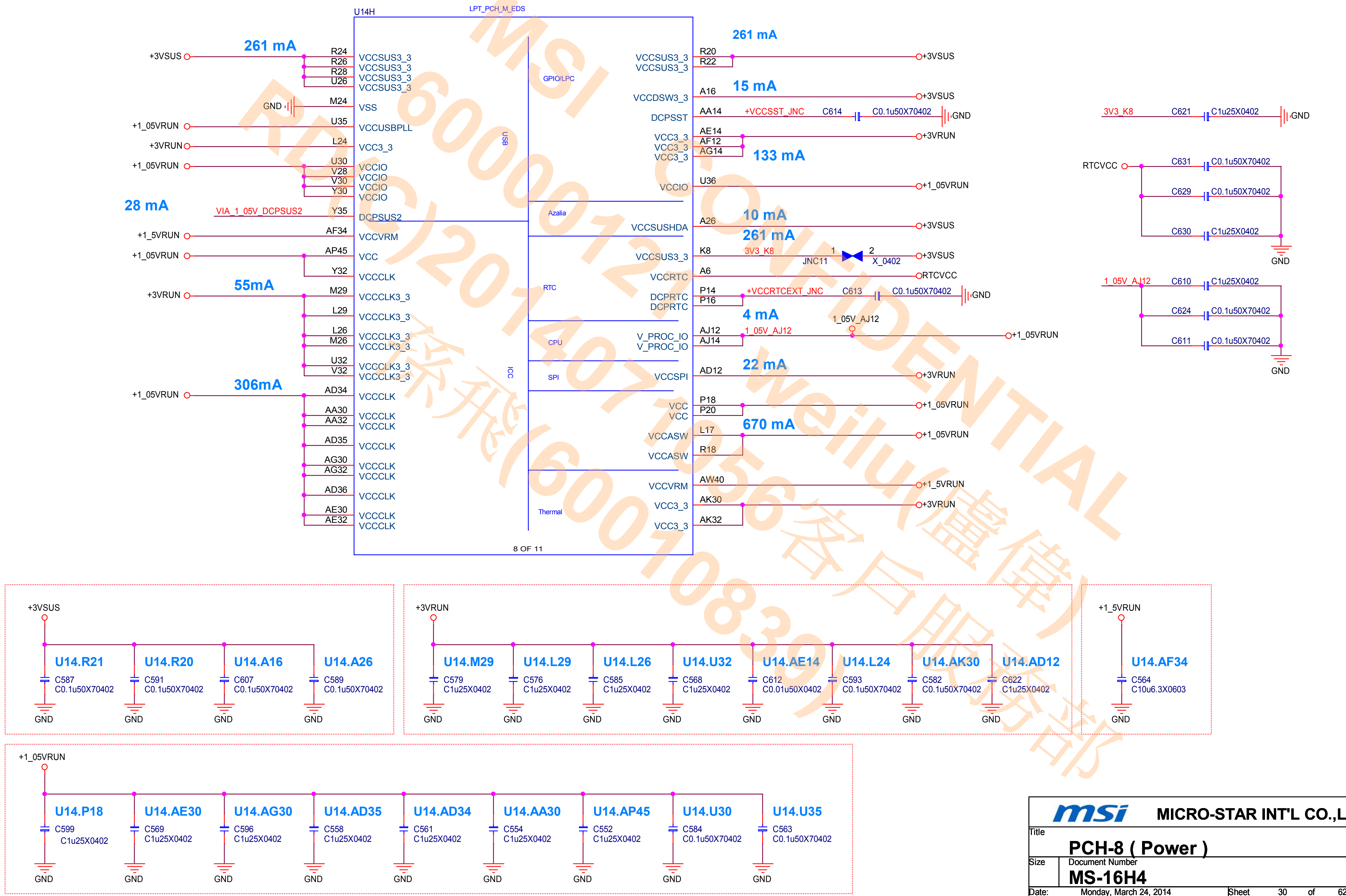
Lynx Point (Power)



msi	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-8 (Power)	
Size	Document Number MS-16H4	Rev 0A
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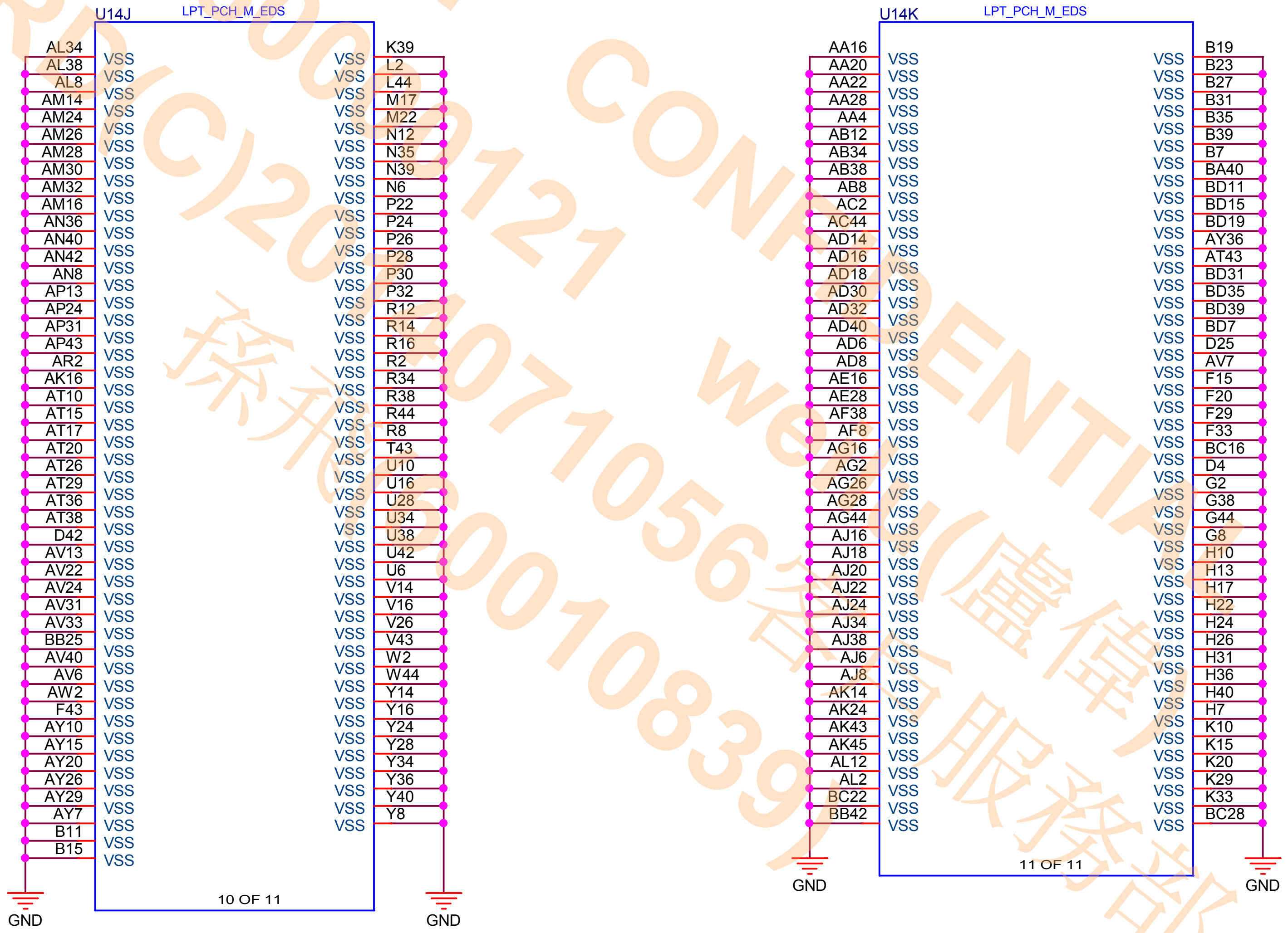
Lynx Point (GND)



MICRO-STAR INT'L CO.,LTD.

Title: **PCH-8 (GND)**

Size | Document Number: **MS-16H4** | Rev: **0A**

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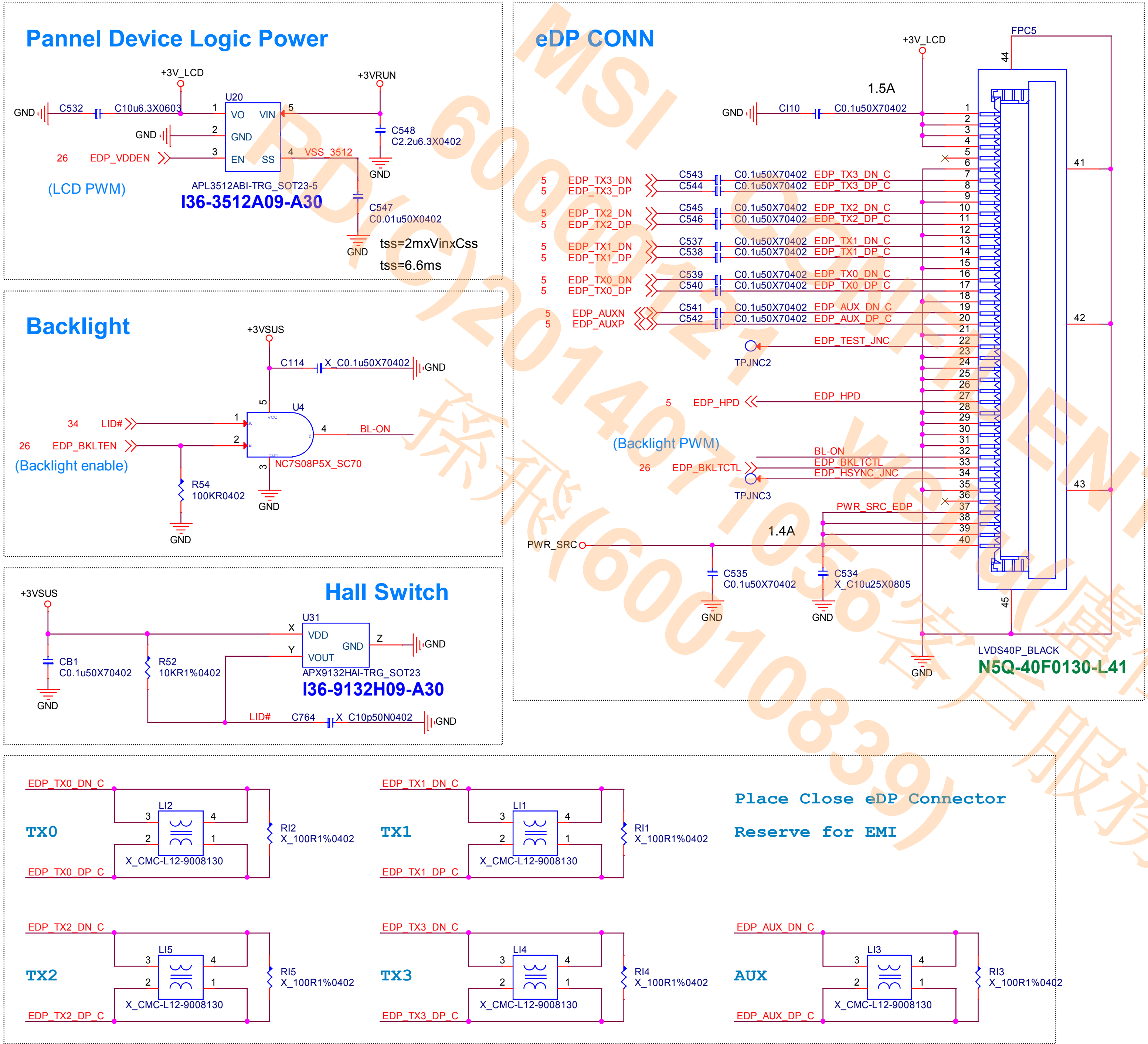
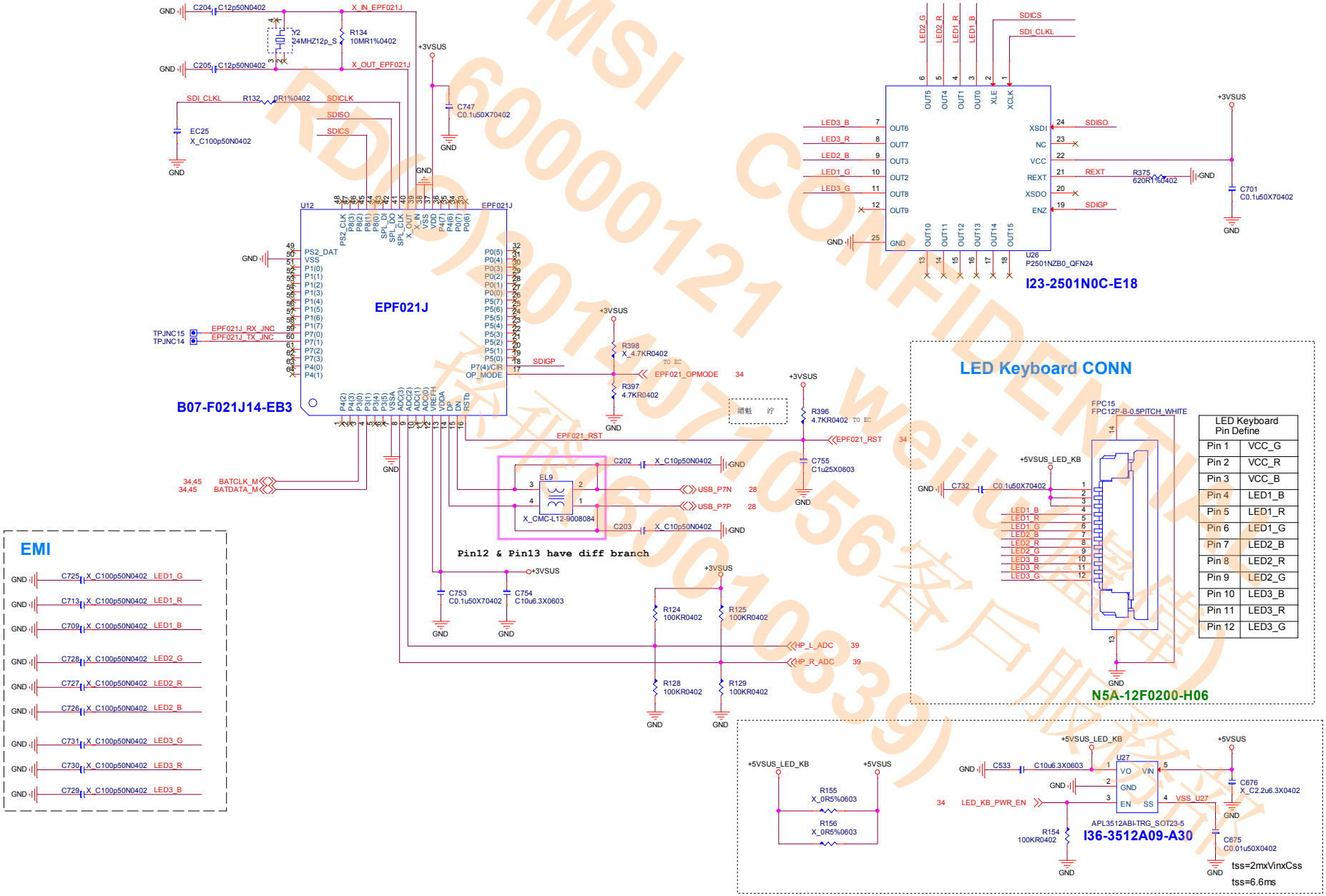
eDP Connector



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

LED 8051 Controller



msi	MICRO-STAR INT'L CO.,LTD.	
Title	LED Driver IC/LED_8051	
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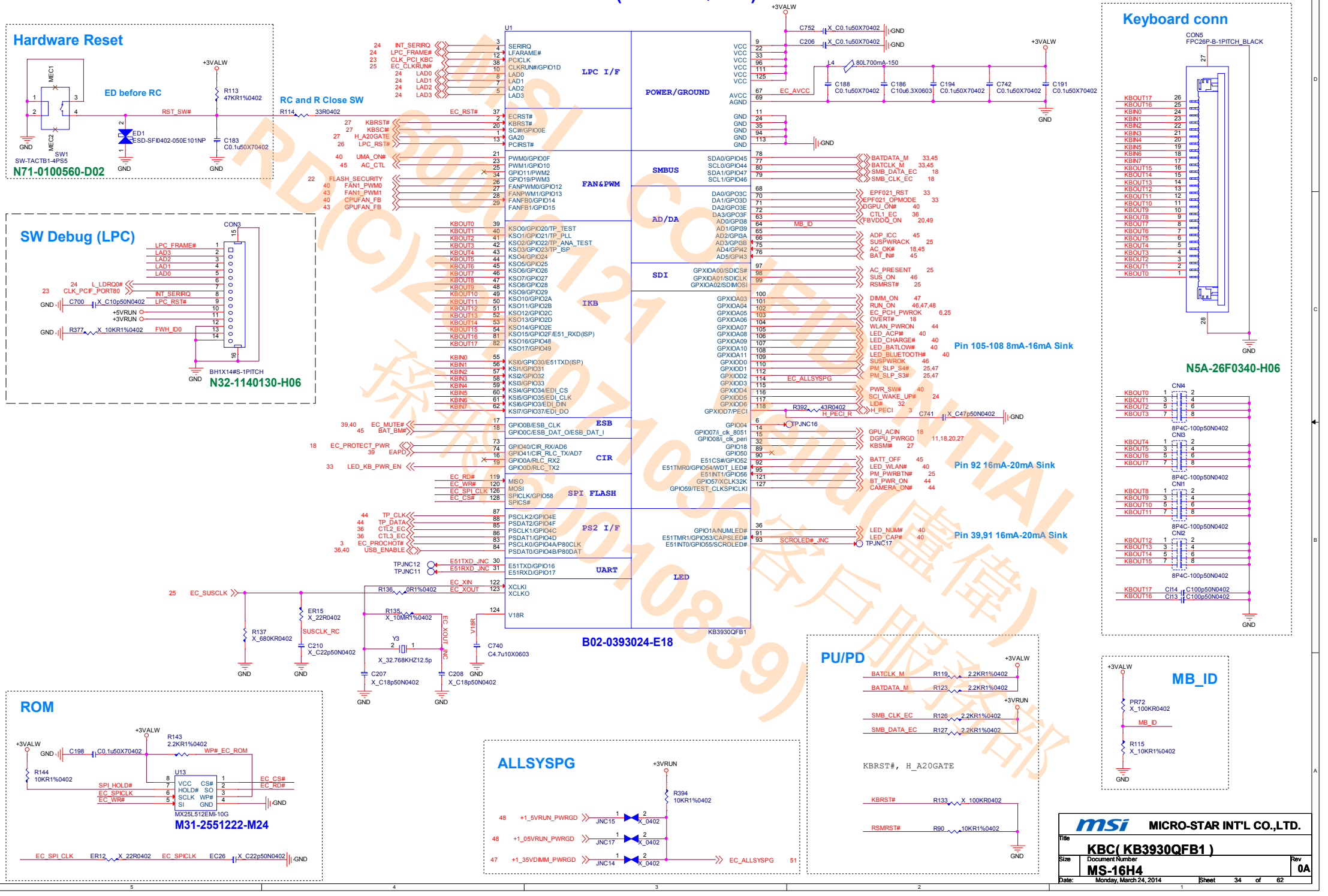
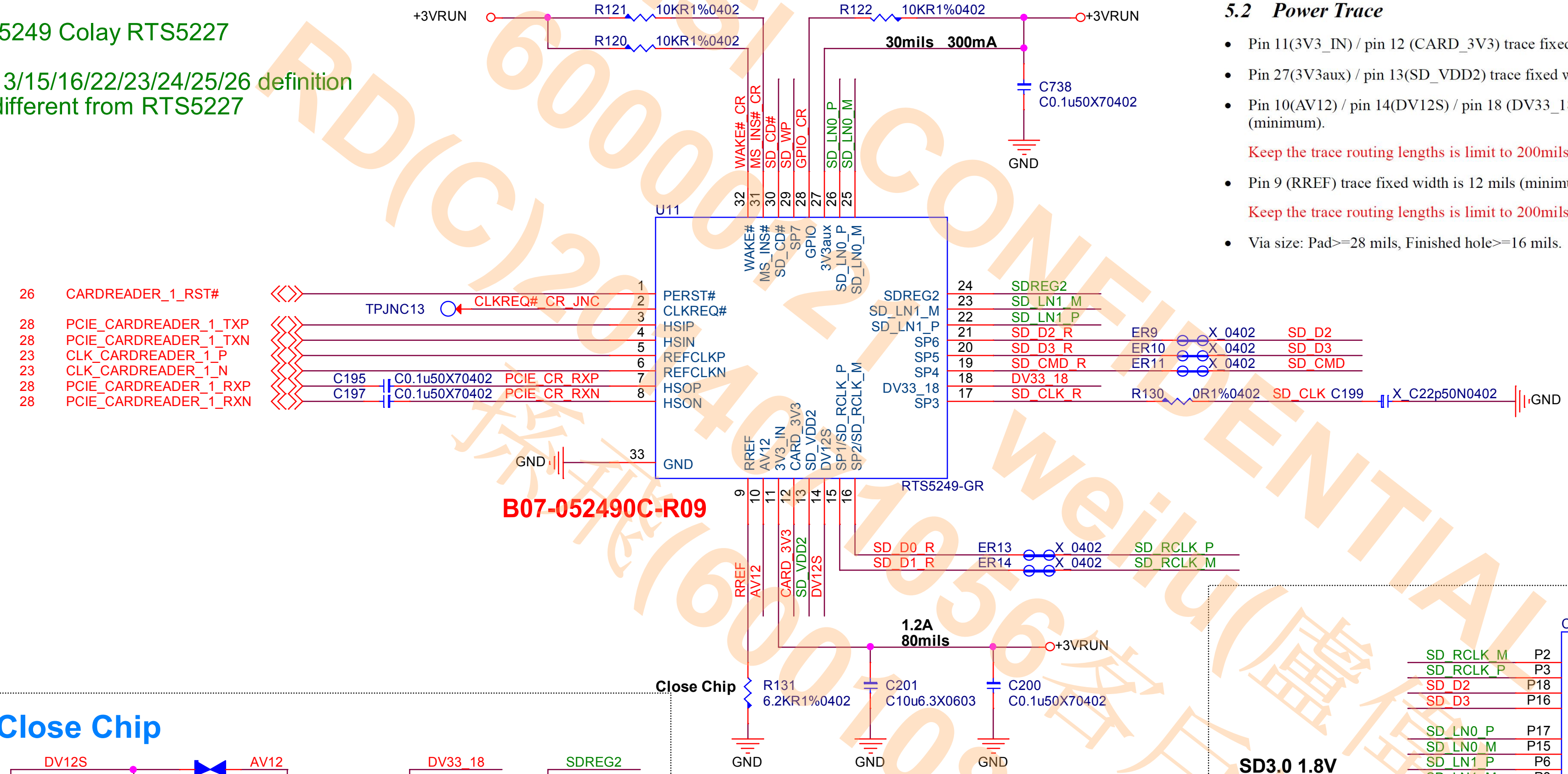
KBC(KB3930QFB1)



CardReader (RTS5249)

RTS5249 Colay RTS5227

Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227



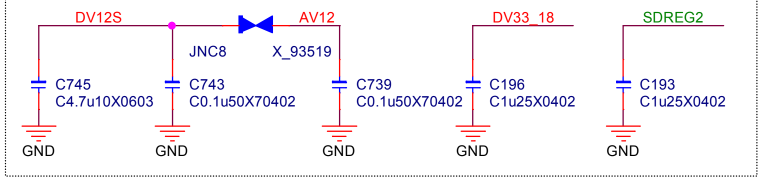
5.2 Power Trace

- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace fixed width is 40 mils (minimum).
- Pin 27(3V3aux) / pin 13(SD_VDD2) trace fixed width is 30 mils (minimum).
- Pin 10(AV12) / pin 14(DV12S) / pin 18 (DV33_18) / pin 24(SDREG2) trace fixed width is 20 mils (minimum).

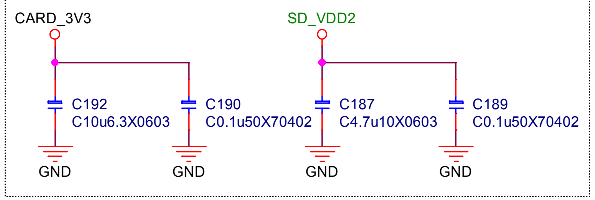
  Keep the trace routing lengths is limit to 200mils.
- Pin 9 (RREF) trace fixed width is 12 mils (minimum).

  Keep the trace routing lengths is limit to 200mils.
- Via size: Pad>=28 mils, Finished hole>=16 mils.

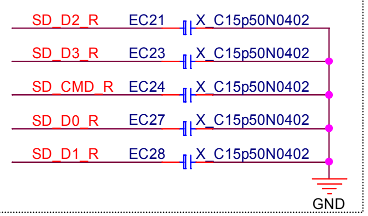
Close Chip

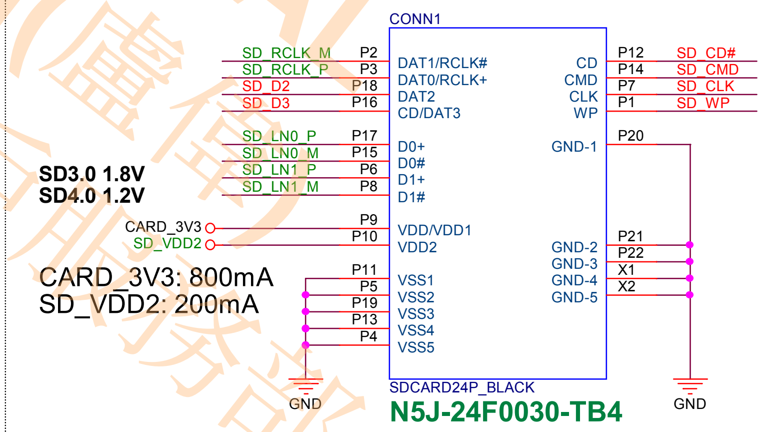


Close Connector



EMI

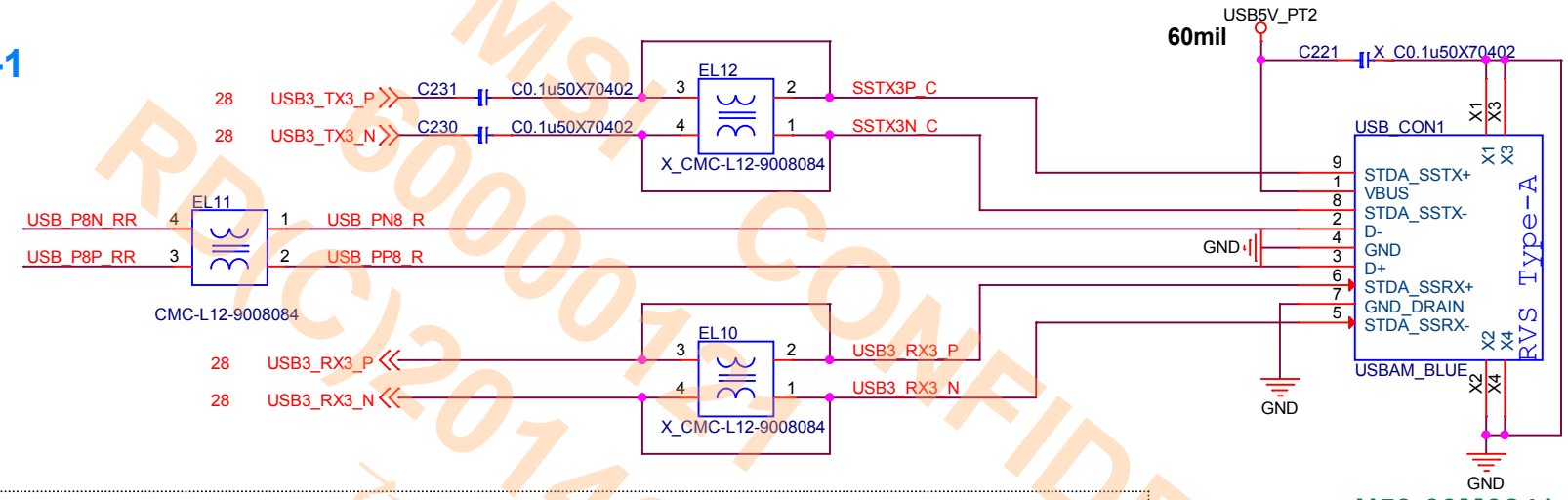




USB 3.0 / iCharger

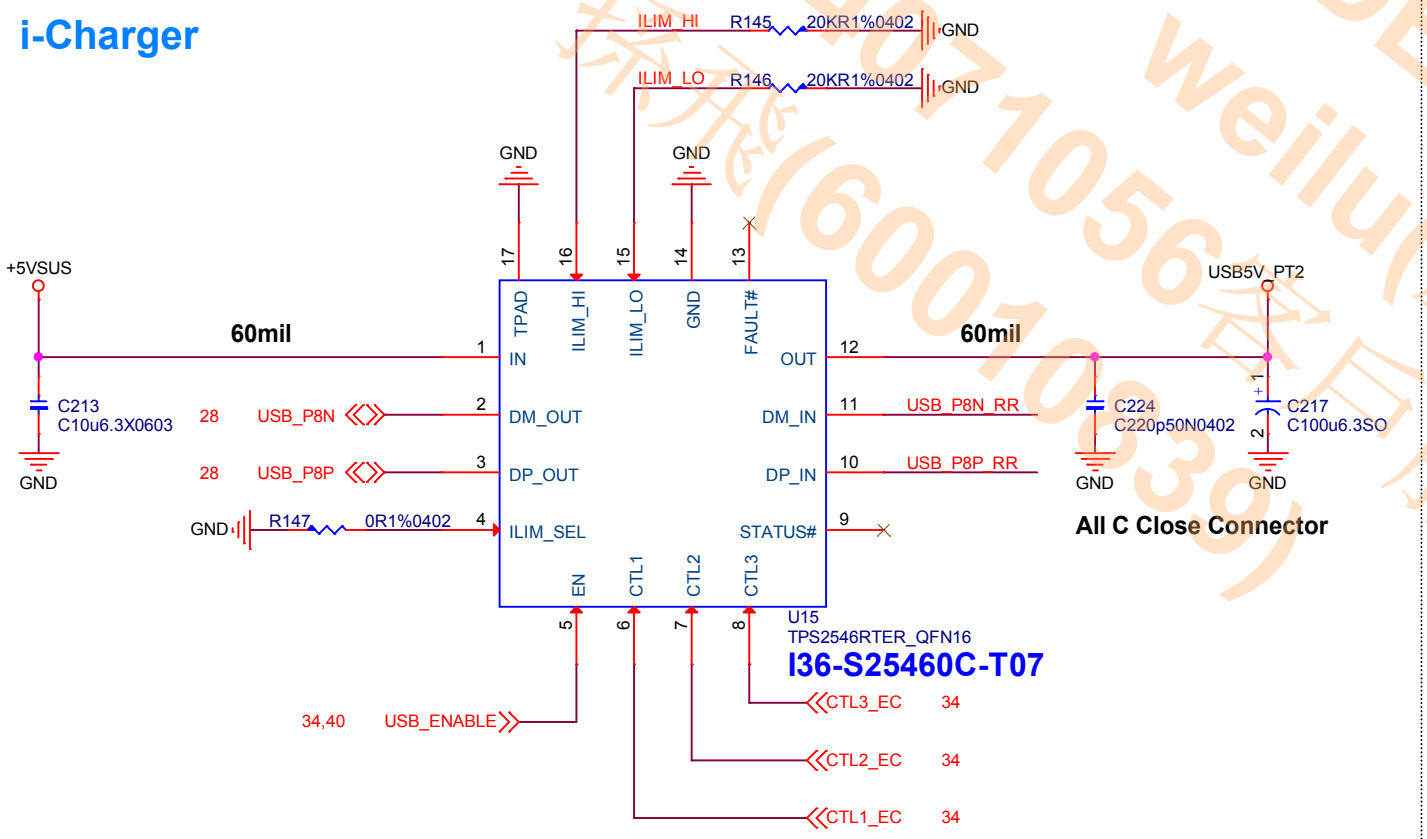
USB3.0 CNT-1

USB3.0 Port-6
USB2.0 Port-9

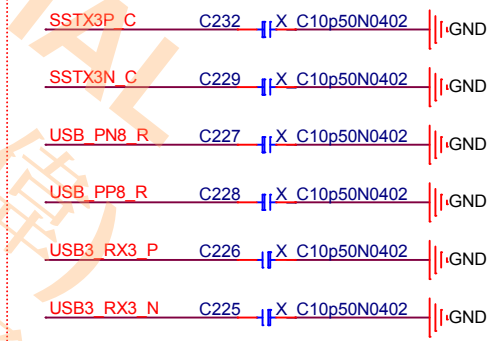


N53-09M0241-AF2

i-Charger



EMI



MICRO-STAR INT'L CO.,LTD.		
Title: USB 3.0 / iCharger		
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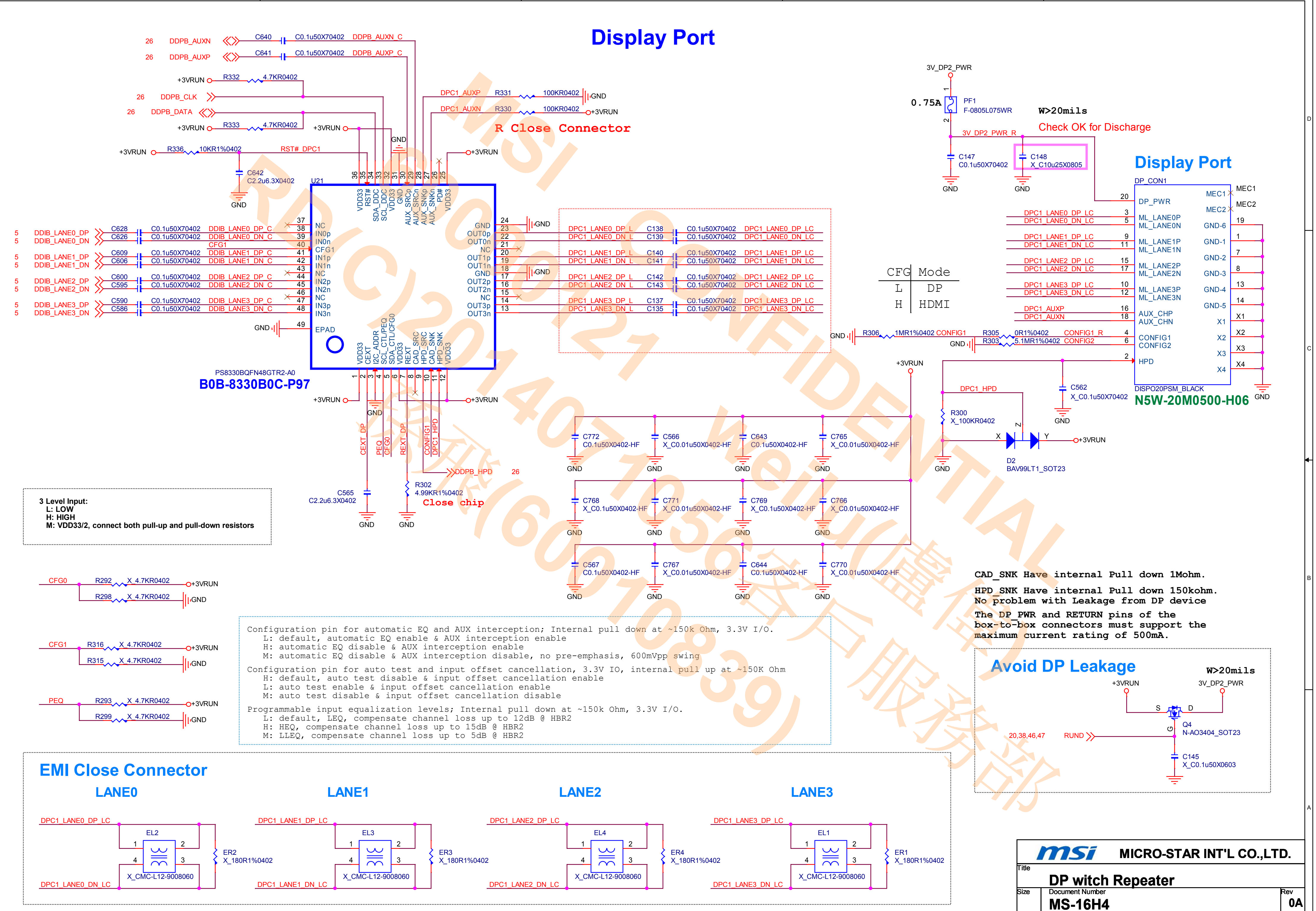
Display Port




```
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
    L: default, automatic EQ enable & AUX interception enable
    H: automatic EQ disable & AUX interception enable
    M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
    H: default, auto test disable & input offset cancellation enable
    L: auto test enable & input offset cancellation enable
    M: auto test disable & input offset cancellation disable
Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
    L: default, LEQ, compensate channel loss up to 12dB @ HBR2
    H: HEQ, compensate channel loss up to 15dB @ HBR2
    M: LLEQ, compensate channel loss up to 5dB @ HBR2
```

MICRO-STAR INT'L CO.,LTD.

Title	DP witch Repeater	
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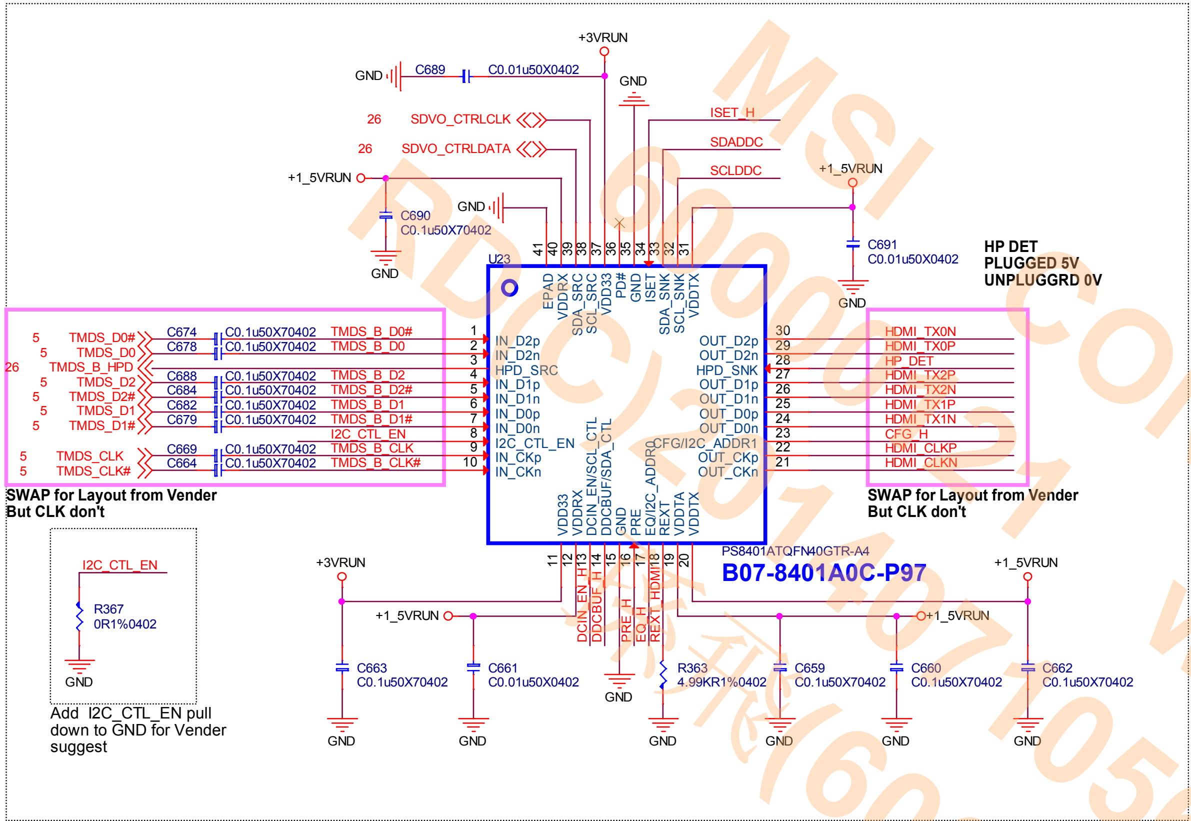
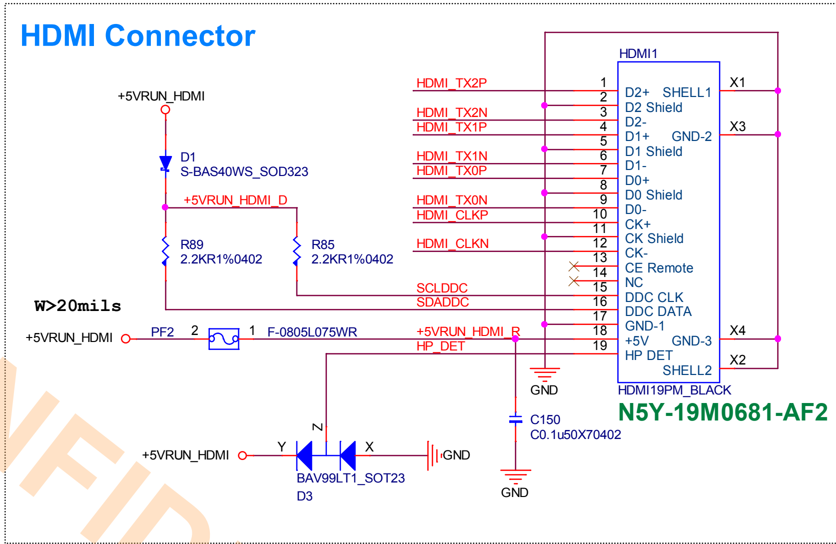
HDMI Repeater



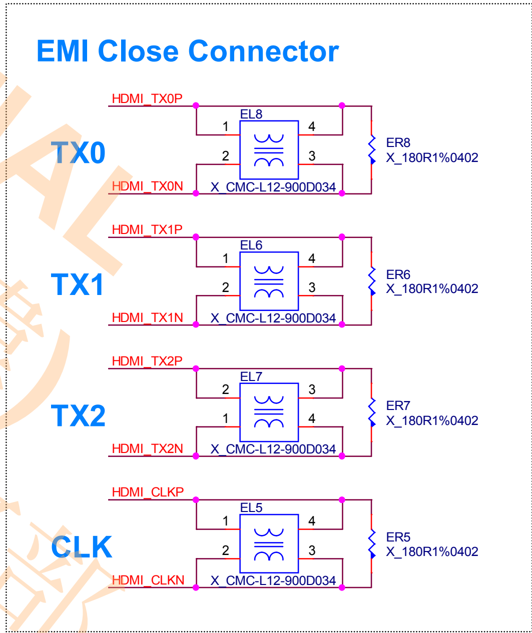
HDMI Connector

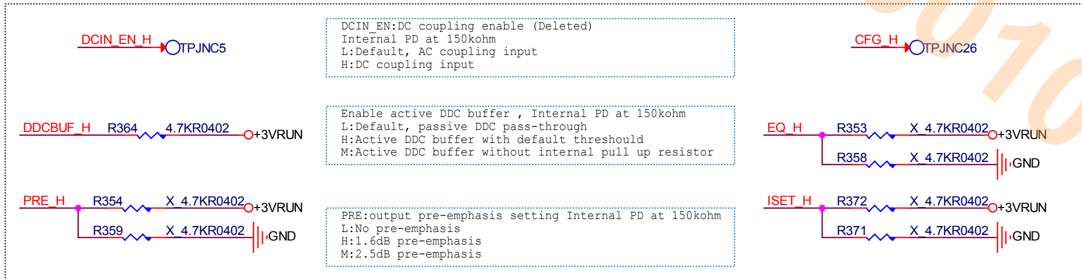


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

EMI Close Connector





DCIN_EN:DC coupling enable (Deleted)
Internal PD at 150kohm
L:Default, AC coupling input
H:DC coupling input

Configuation pin (Deleted)
Internal PD at 150kohm
L:HDMI ID disable
H:HDMI ID enable

Enable active DDC buffer , Internal PD at 150kohm
L:Default, passive DDC pass-through
H:Active DDC buffer with default threshold
M:Active DDC buffer without internal pull up resistor

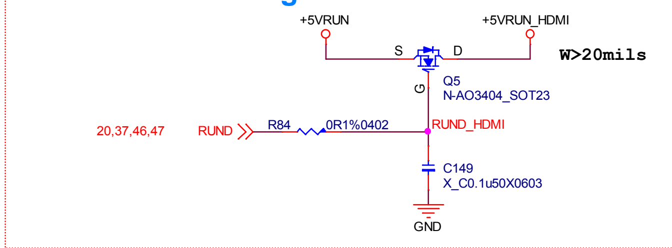
Receiver equalization setting
Internal PD at 150kohm
L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 48.6dB

PRE:output pre-emphasis setting Internal PD at 150kohm
L:No pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis

TMDS output swing adjustment
Internal PD at 150kohm
L:Default
H:Increase +13%
M:reduce -13%

ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150k , 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage



MICRO-STAR INT'L CO.,LTD.

Title: HDMI Repeater

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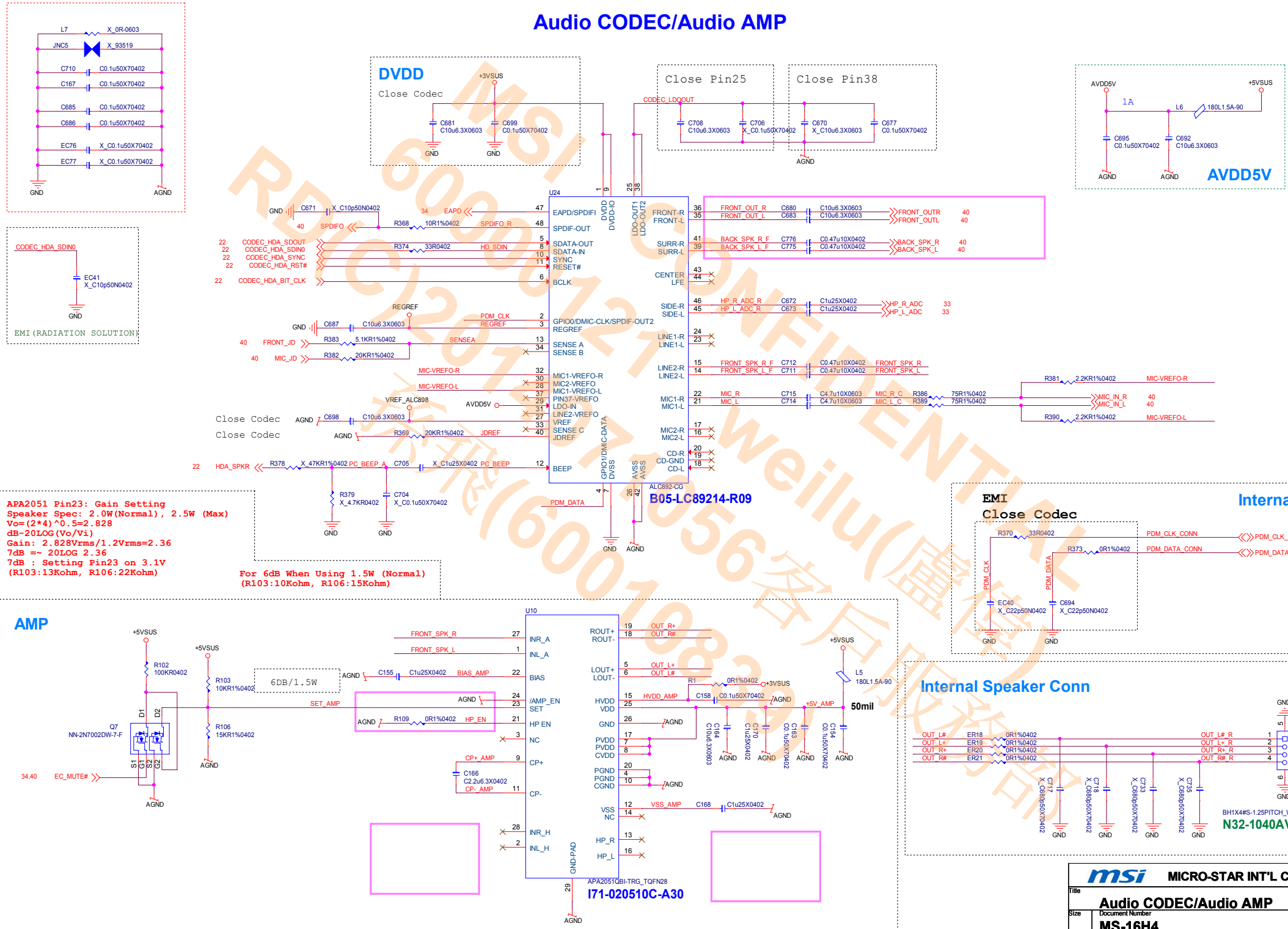
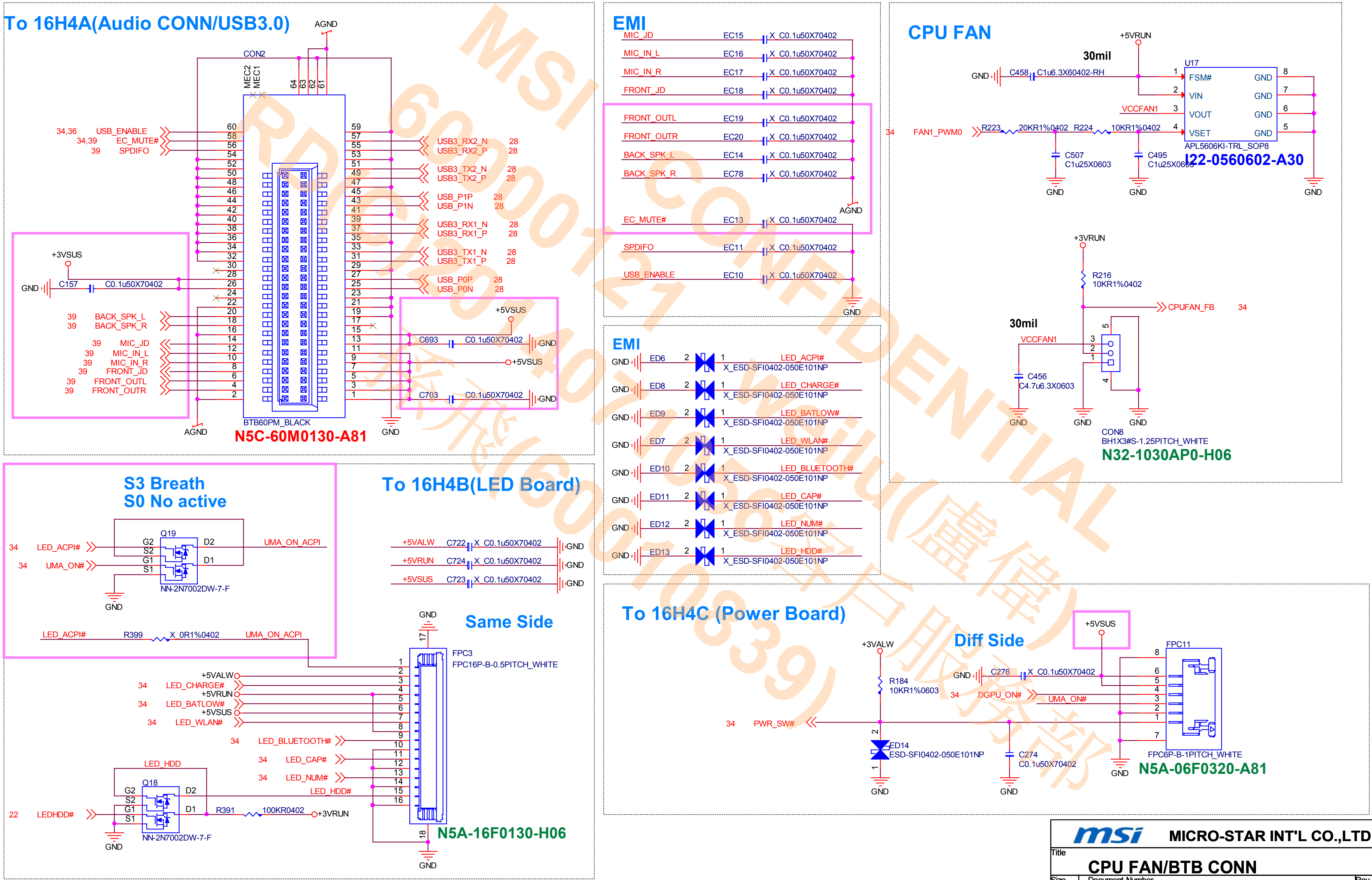
Audio CODEC/Audio AMP



CPU FAN/BTB CONN



MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN/BTB CONN

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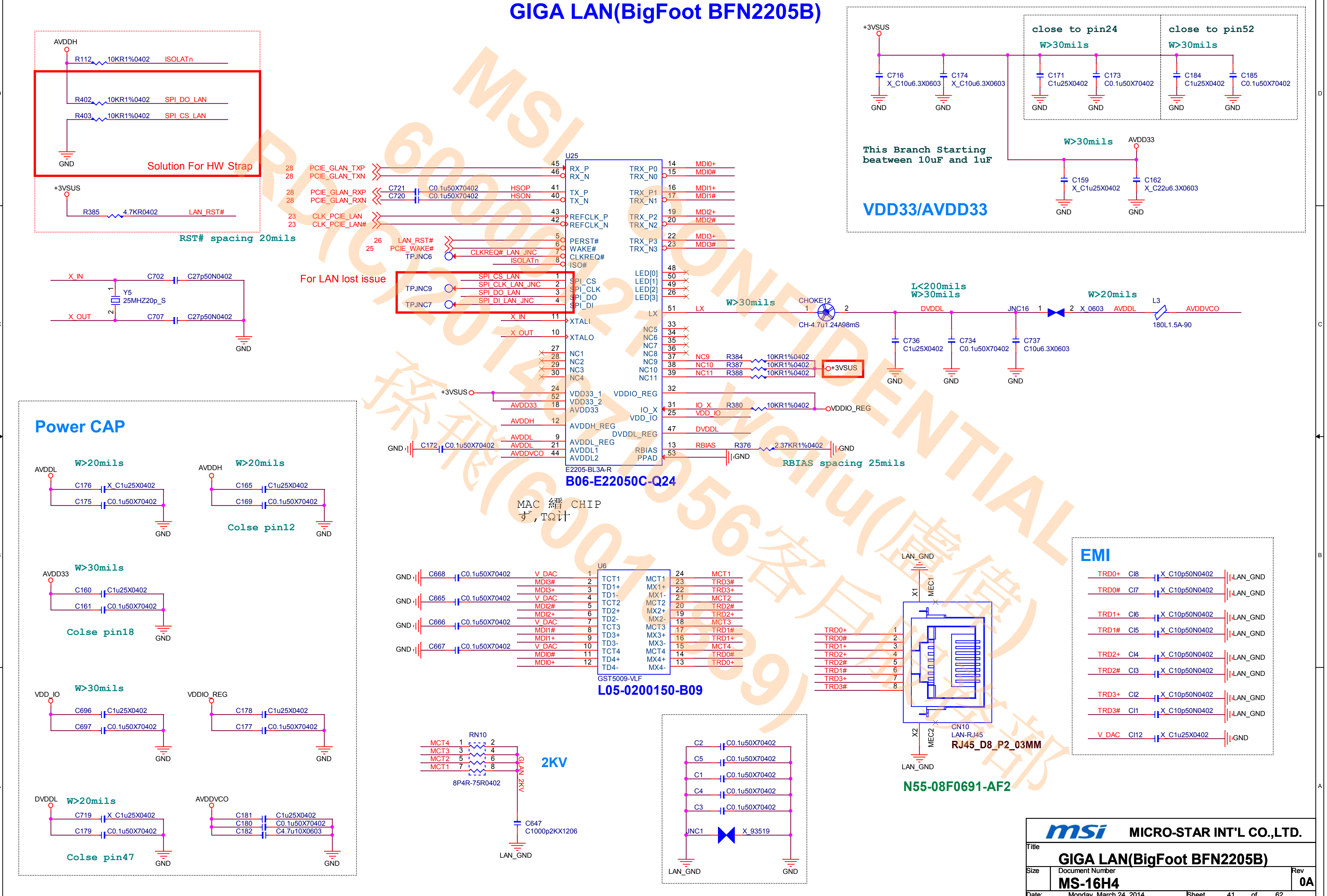
GIGA LAN(BigFoot BFN2205B)



MICRO-STAR INT'L CO.,LTD.

Title	GIGA LAN(BigFoot BFN2205B)
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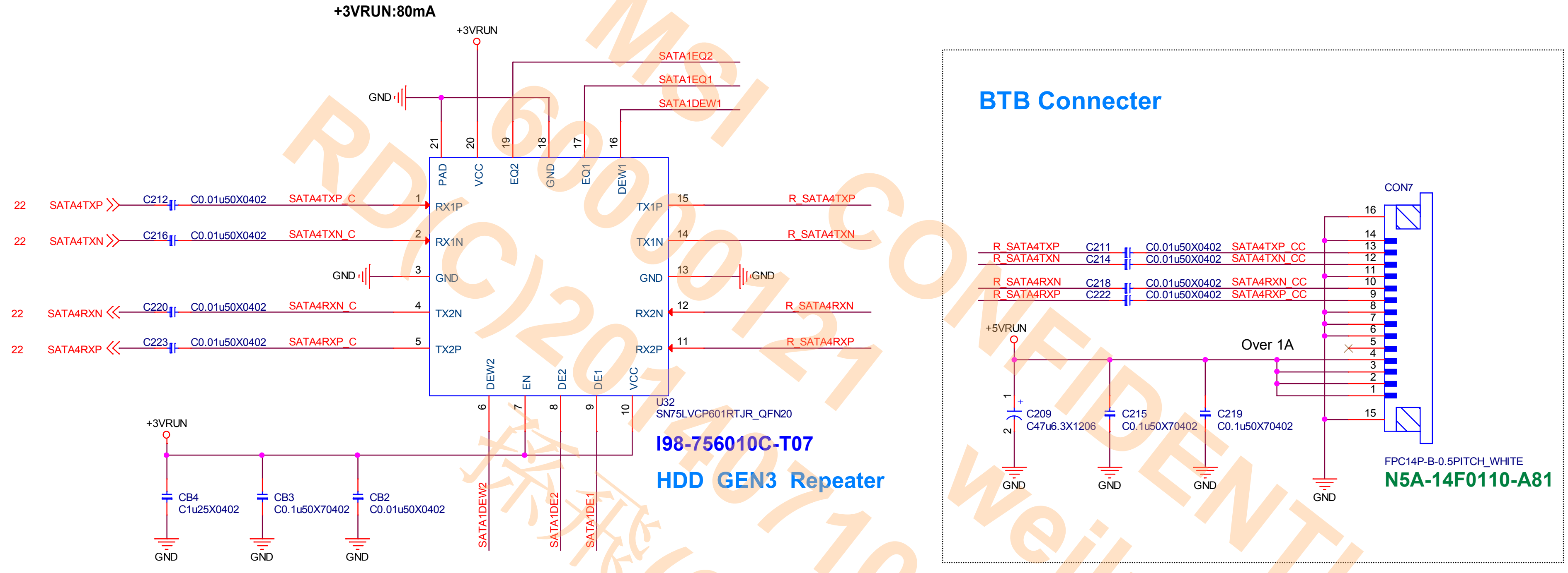
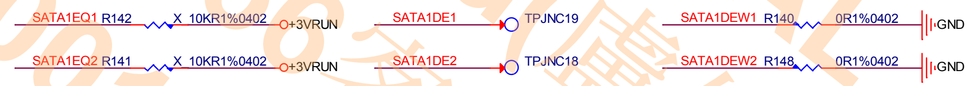
HDD (With Repeater)



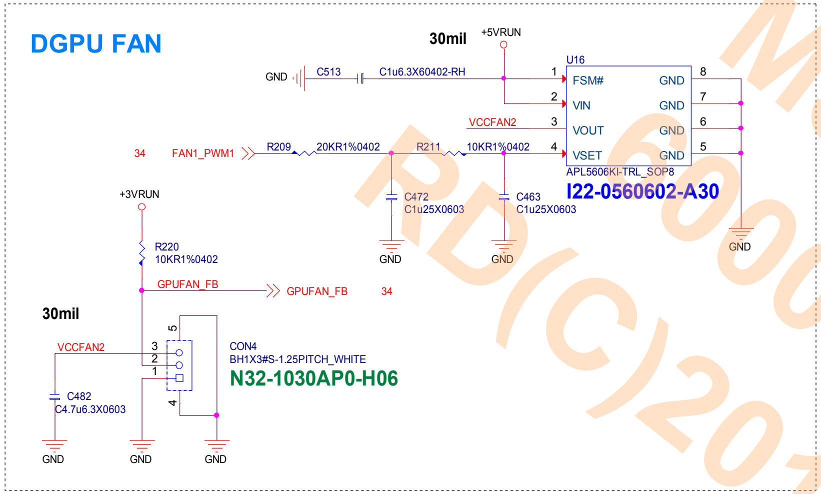


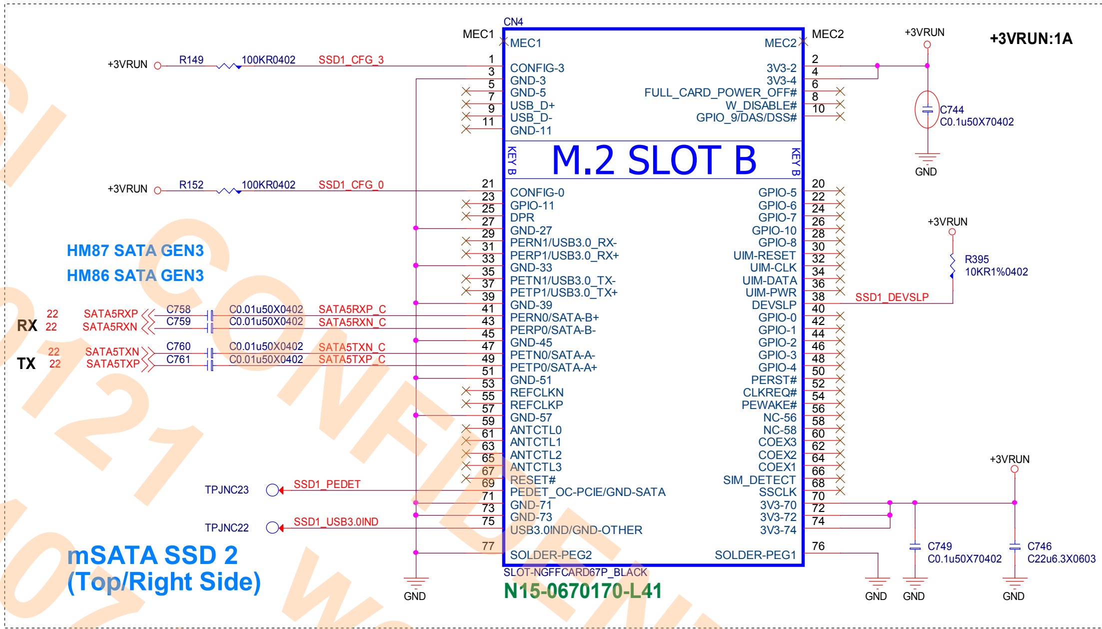
TI SN75LVCP601RTJR HW Setting

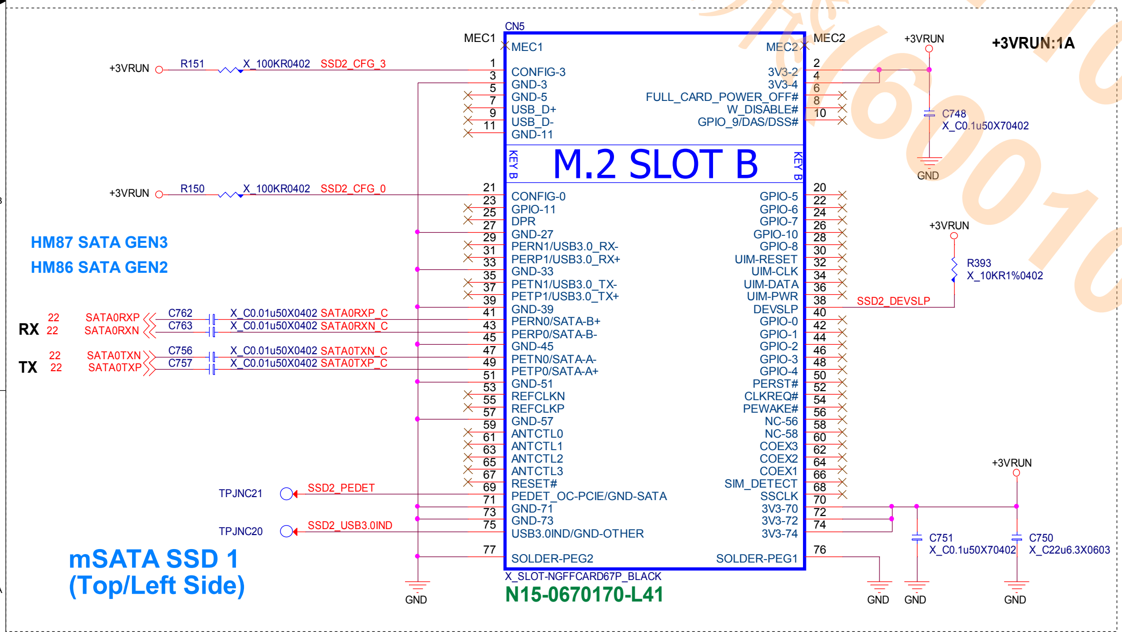
DE1/DE2	CH1/CH2De-Emphasis dB(at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB(at 6Gbps)
NC(default)	-4	NC(default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1(default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

SSD/ DGPU FAN







40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential singal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential singal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential singal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host Transmitter differential singal pair

MICRO-STAR INT'L CO.,LTD.

Title: SSD/ DGPU FAN

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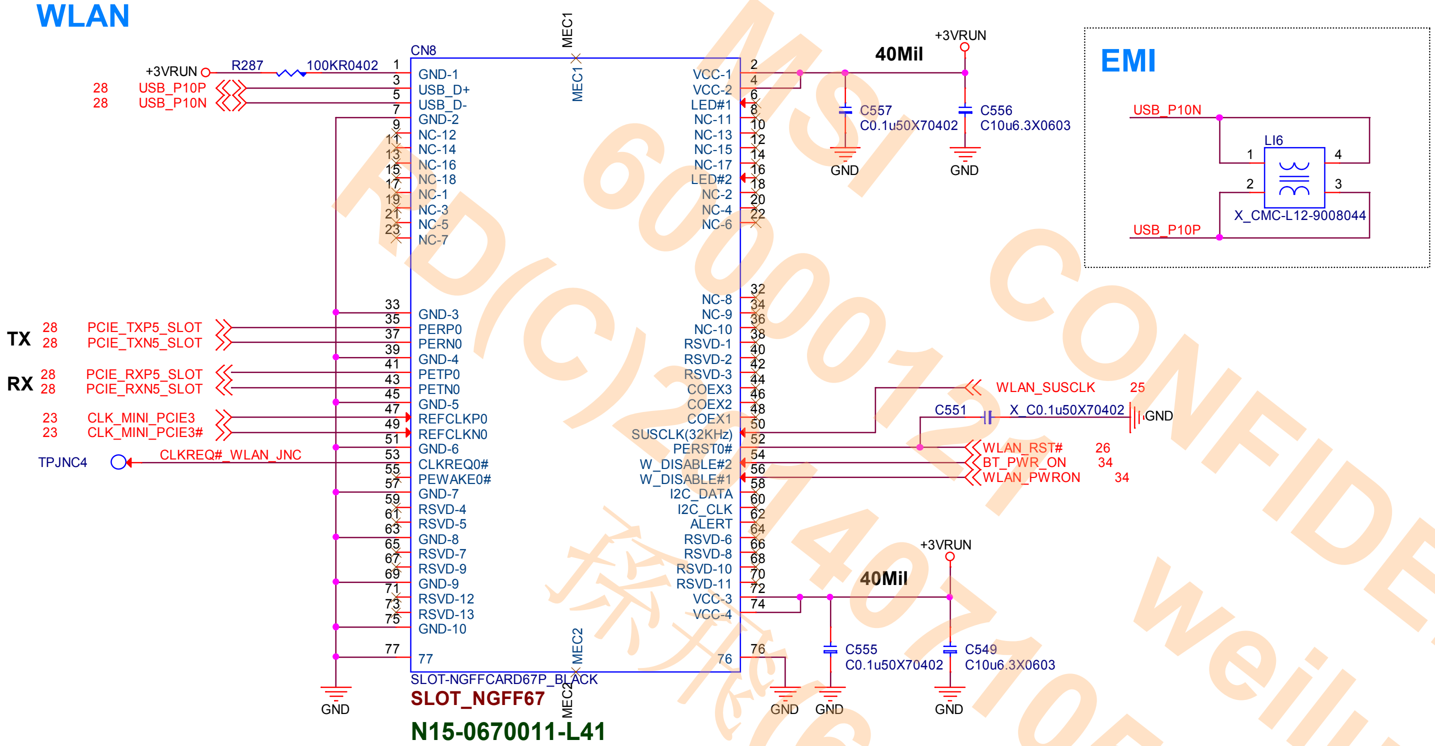
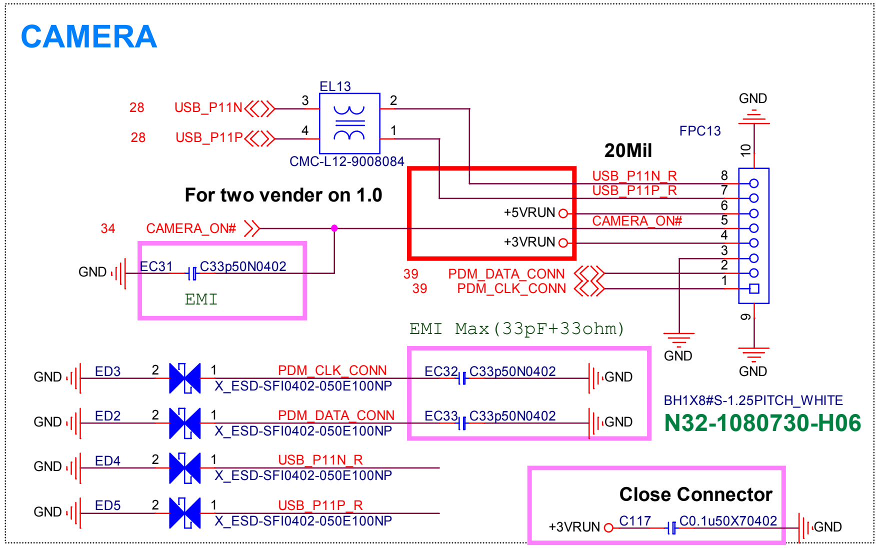
WLAN /Camera/ClickPad/FP

WLAN

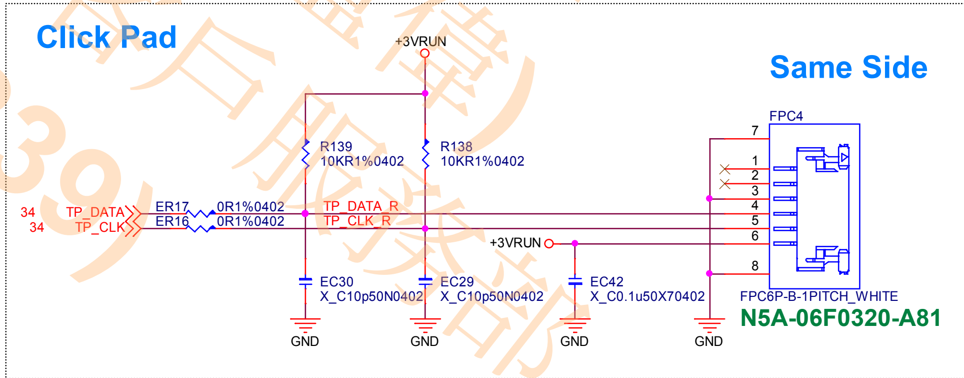


Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA



Click Pad



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Title: WLAN /Camera/ClickPad/FP

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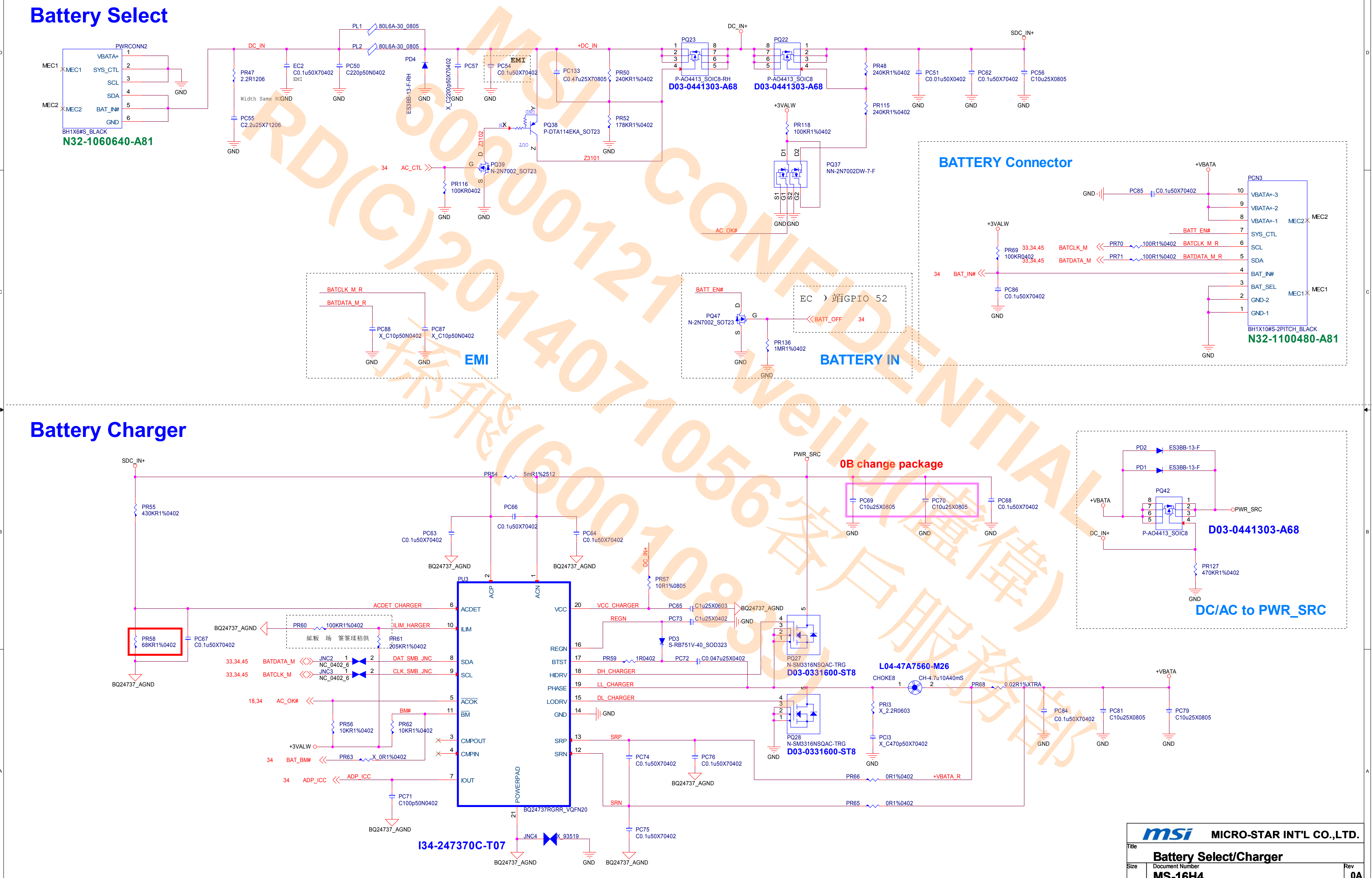
Date: Monday, March 24, 2014 | Sheet 44 of 62

Battery Select/Charger



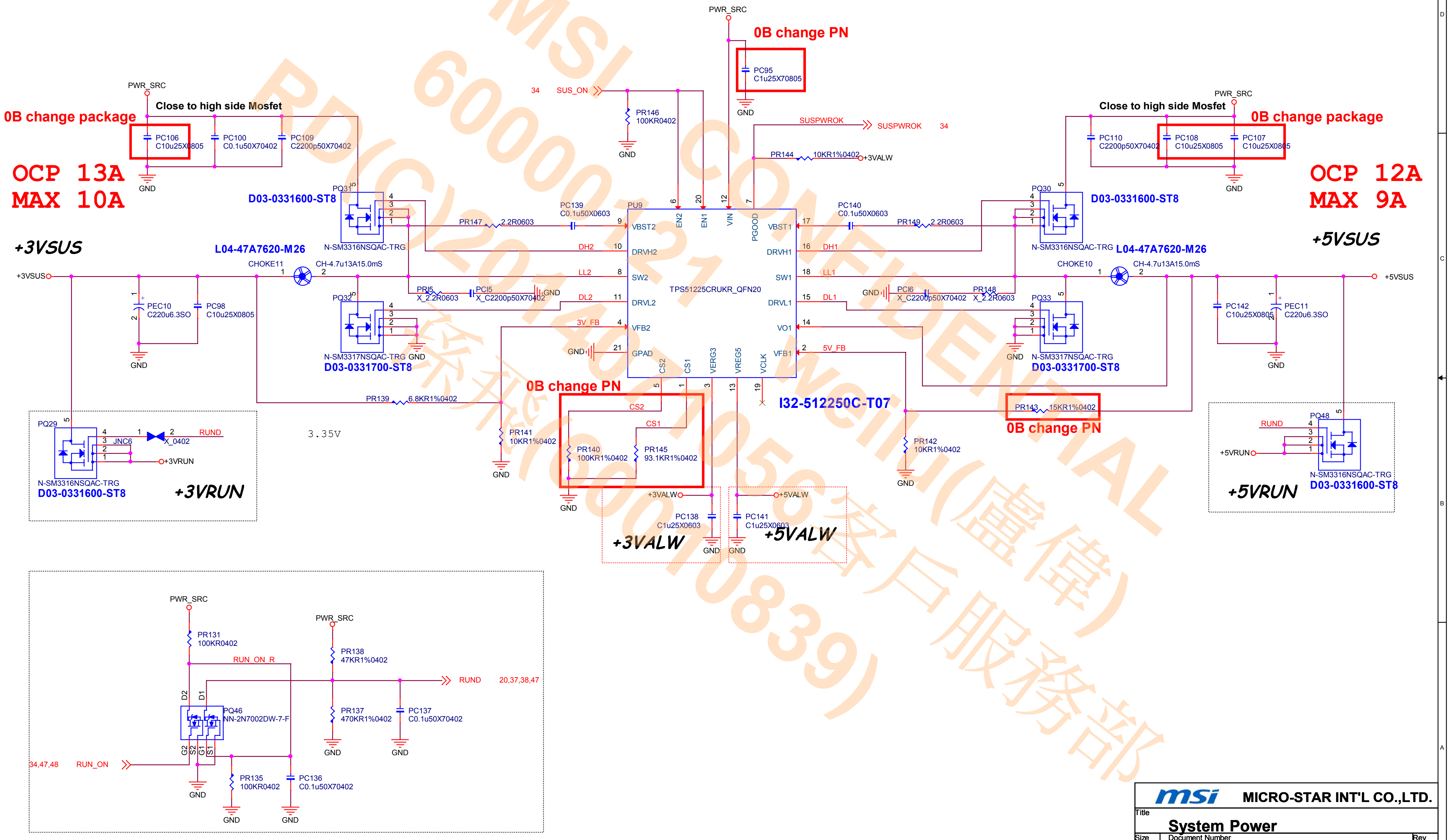
msi MICRO-STAR INT'L CO.,LTD.

Title: Battery Select/Charger

Size | Document Number: MS-16H4 | Rev: 0A

Date: Monday, March 24, 2014 | Sheet 45 of 62

System Power



MICRO-STAR INT'L CO.,LTD.

Title	System Power	
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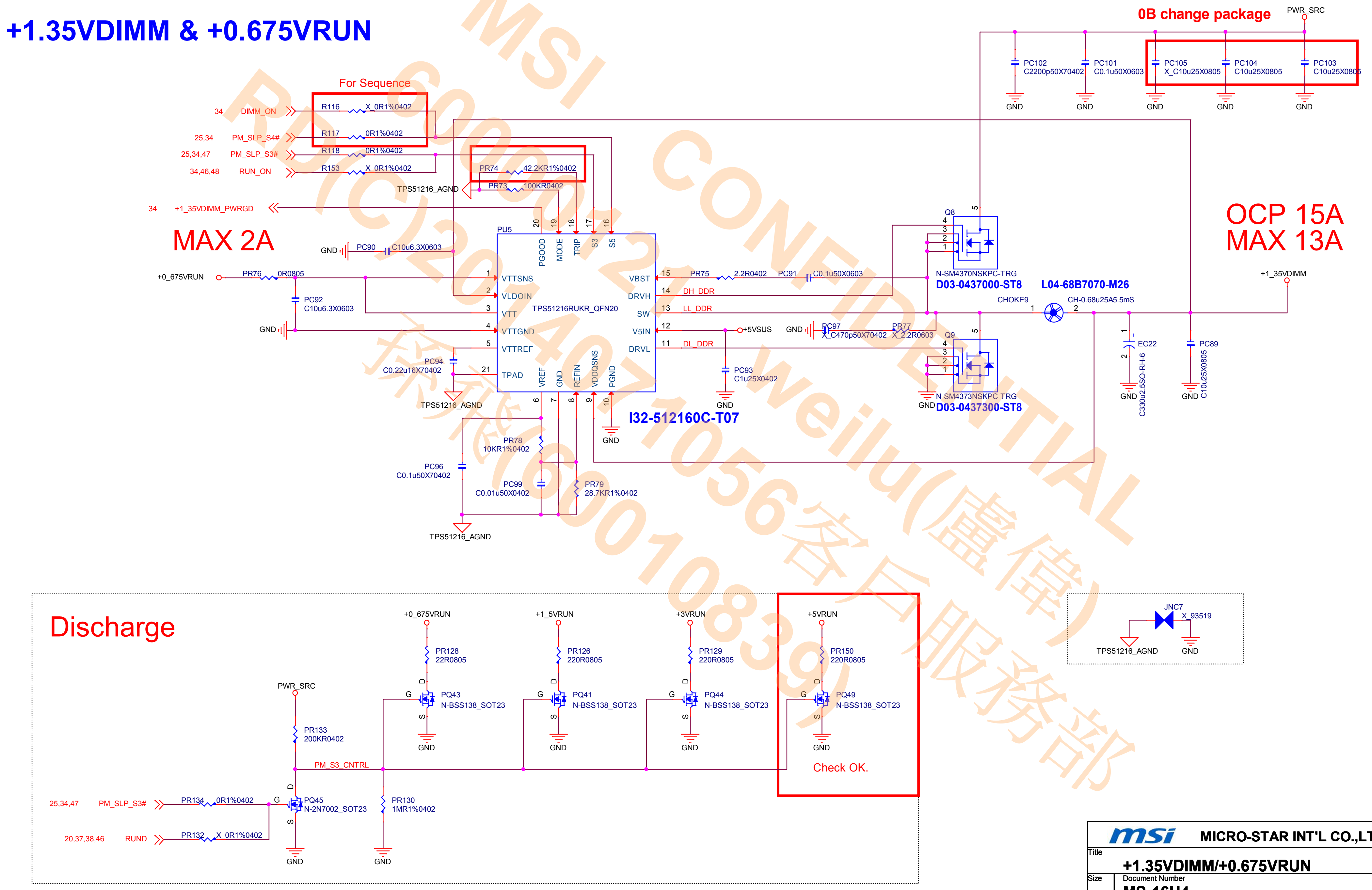
+1.35VDIMM/+0.675VRUN



MICRO-STAR INT'L CO.,LTD.

Title: +1.35VDIMM/+0.675VRUN

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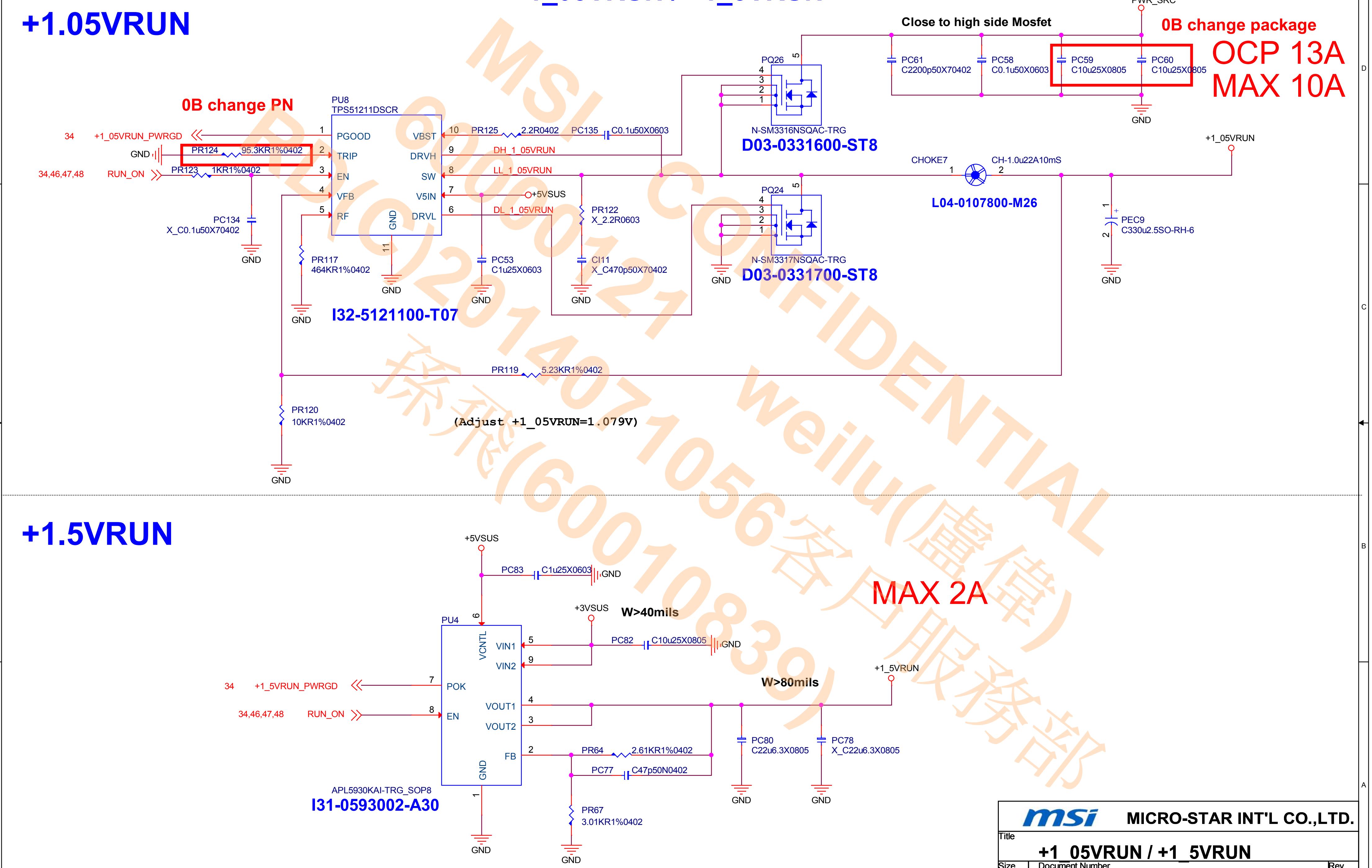
+1_05VRUN / +1_5VRUN



MICRO-STAR INT'L CO.,LTD.

Title	+1_05VRUN / +1_5VRUN
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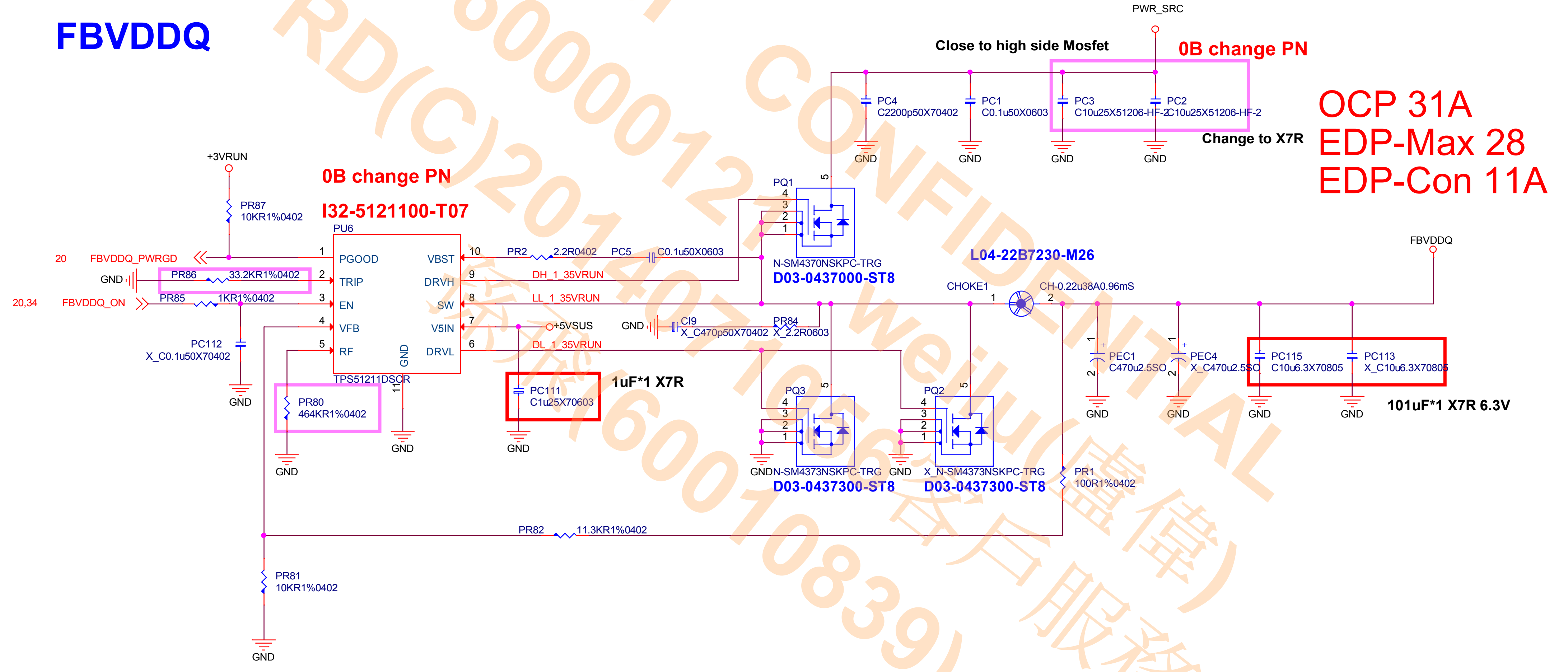
DGPU POWER FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER FBVDDQ

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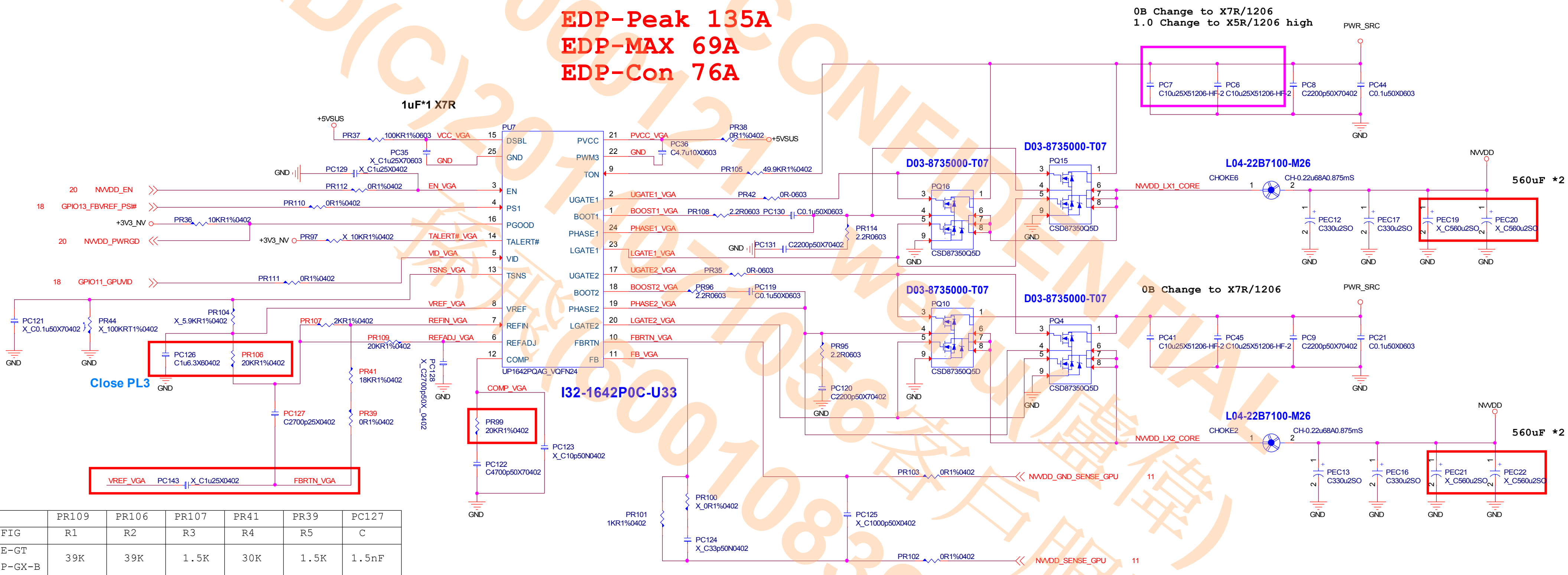
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 135A
EDP-MAX 69A
EDP-Con 76A

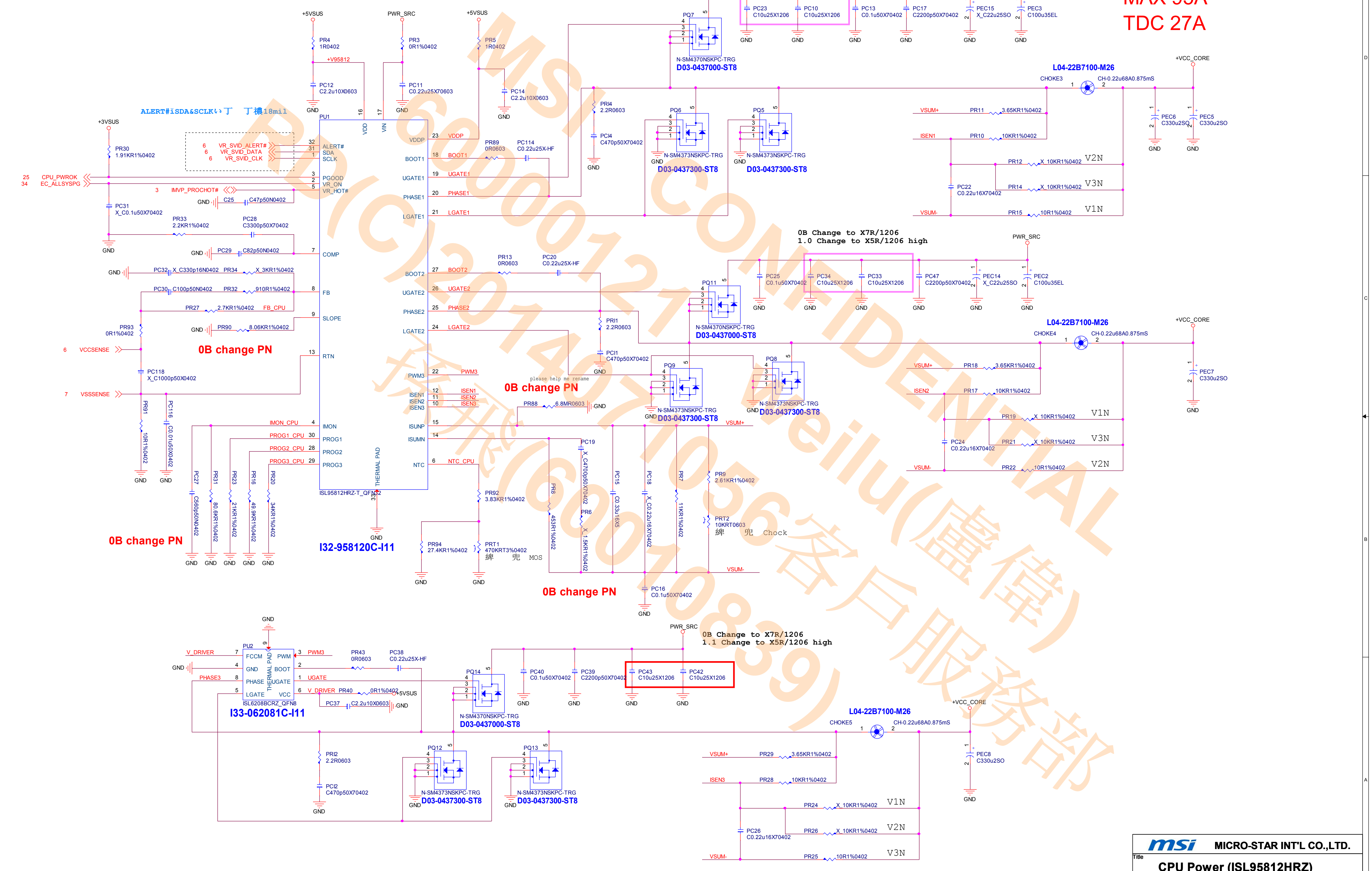


	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
N15E-GT N15P-GX-B	39K	39K	1.5K	30K	1.5K	1.5nF
N15P-GT	20K	20K	2K	18K	0K	2.7nF

CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)

MAX 95A
TDC 27A



MICRO-STAR INT'L CO.,LTD.

Title	CPU Power (ISL95812HRZ)
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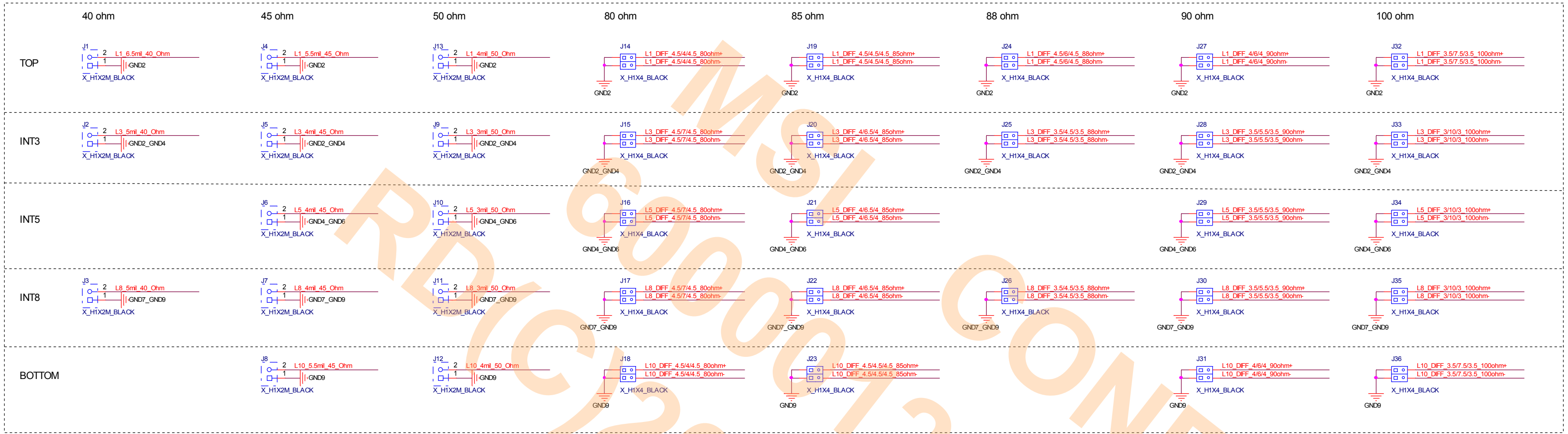
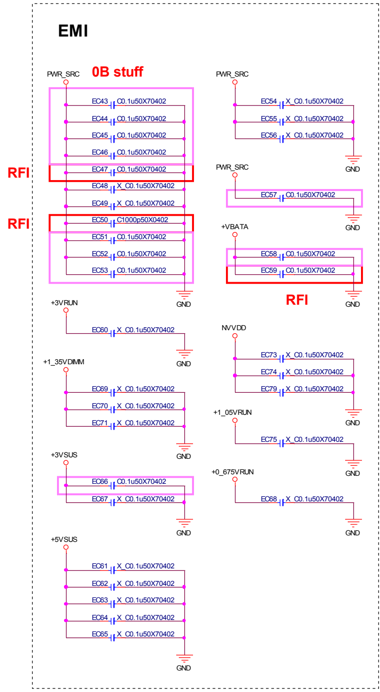
Impedence Connector No PN



EMI/ Impedence



msi	MICRO-STAR INT'L CO.,LTD.
Title	EMI/ Impedence
Size / Document Number	MS-16H4
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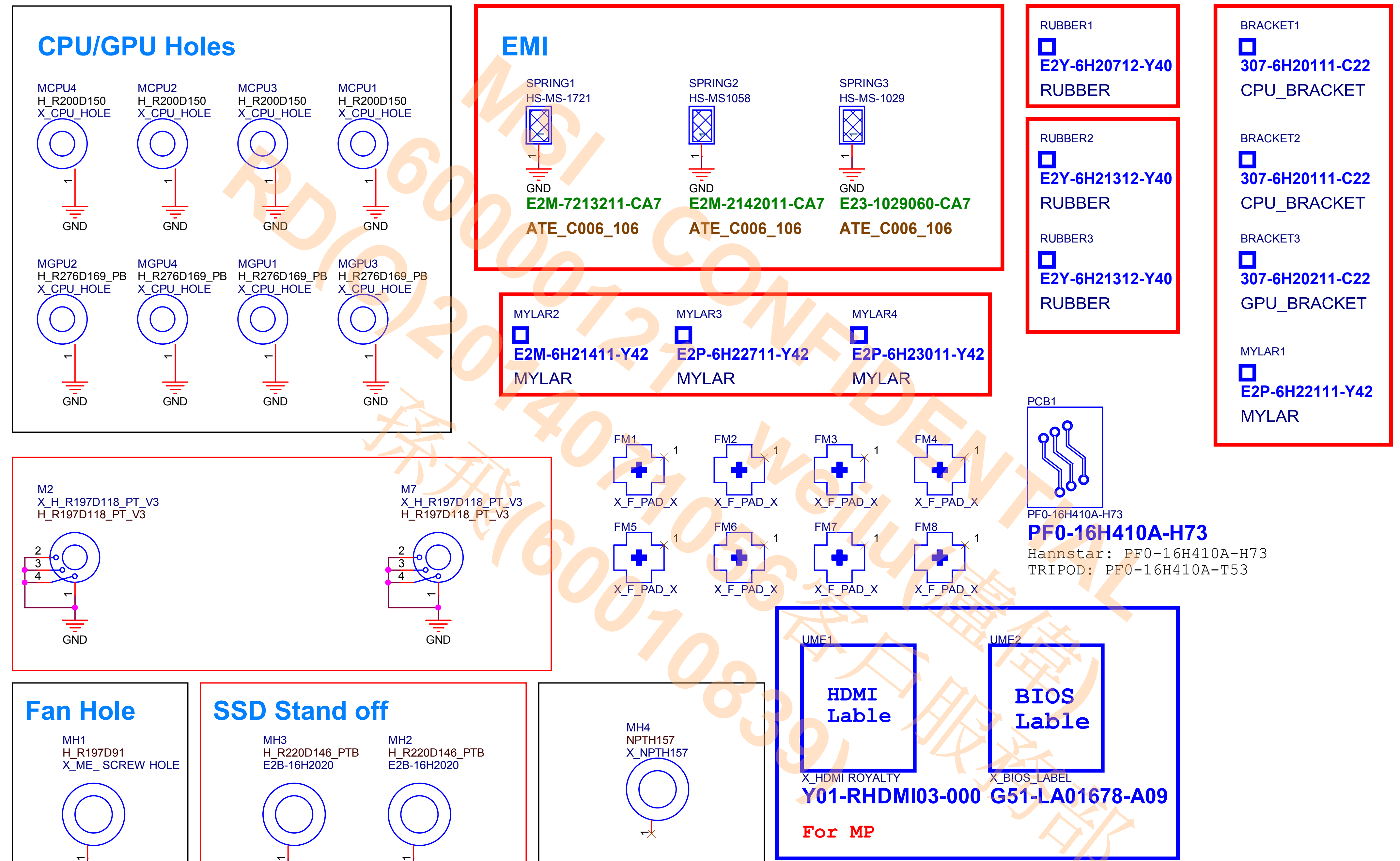
CPU/GPU Holes
MCPU4 H_R200D150 X_CPU_HOLE
MCPU2 H_R200D150 X_CPU_HOLE
MCPU3 H_R200D150 X_CPU_HOLE
MCPU1 H_R200D150 X_CPU_HOLE
GND
MGPU2 H_R276D169_PB X_CPU_HOLE
MGPU4 H_R276D169_PB X_CPU_HOLE
MGPU1 H_R276D169_PB X_CPU_HOLE
MGPU3 H_R276D169_PB X_CPU_HOLE
EMI
SPRING1 HS-MS-1721 GND E2M-7213211-CA7 ATE_C006_106
SPRING2 HS-MS1058 GND E2M-2142011-CA7 ATE_C006_106
SPRING3 HS-MS-1029 GND E23-1029060-CA7 ATE_C006_106
RUBBER1 E2Y-6H20712-Y40 RUBBER
RUBBER2 E2Y-6H21312-Y40 RUBBER
RUBBER3 E2Y-6H21312-Y40 RUBBER
BRACKET1 307-6H20111-C22 CPU_BRACKET
BRACKET2 307-6H20111-C22 CPU_BRACKET
BRACKET3 307-6H20211-C22 GPU_BRACKET
MYLAR1 E2P-6H22111-Y42 MYLAR
MYLAR2 E2M-6H21411-Y42 MYLAR
MYLAR3 E2P-6H22711-Y42 MYLAR
MYLAR4 E2P-6H23011-Y42 MYLAR
FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8 X_F_PAD_X
PCB1 PF0-16H410A-H73
PF0-16H410A-H73
Hannstar: PF0-16H410A-H73
TRIPOD: PF0-16H410A-T53
M2 X_H_R197D118_PT_V3 H_R197D118_PT_V3
M7 X_H_R197D118_PT_V3 H_R197D118_PT_V3
Fan Hole
MH1 H_R197D91 X_ME_ SCREW HOLE
SSD Stand off
MH3 H_R220D146_PTB E2B-16H2020
MH2 H_R220D146_PTB E2B-16H2020
MH4 NPTH157 X_NPTH157
UME1 HDMI Lable X_HDMI ROYALTY Y01-RHDMI03-000
UME2 BIOS Lable X_BIOS_LABEL G51-LA01678-A09
For MP

MICRO-STAR INT'L CO.,LTD.

Title	Screw/ME
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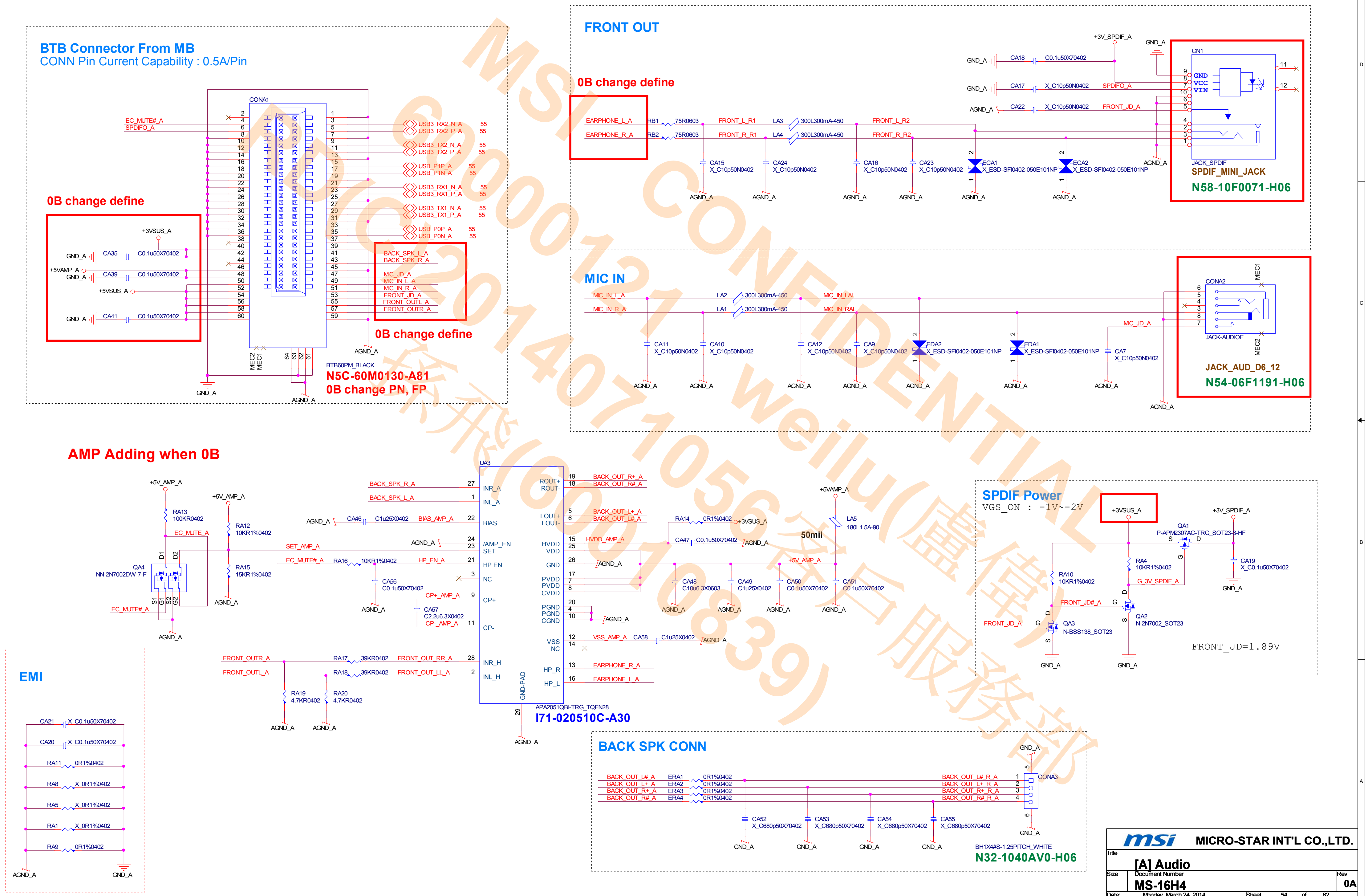
16H4-A Board (Audio CONN)



MICRO-STAR INT'L CO.,LTD.

Title	[A] Audio	
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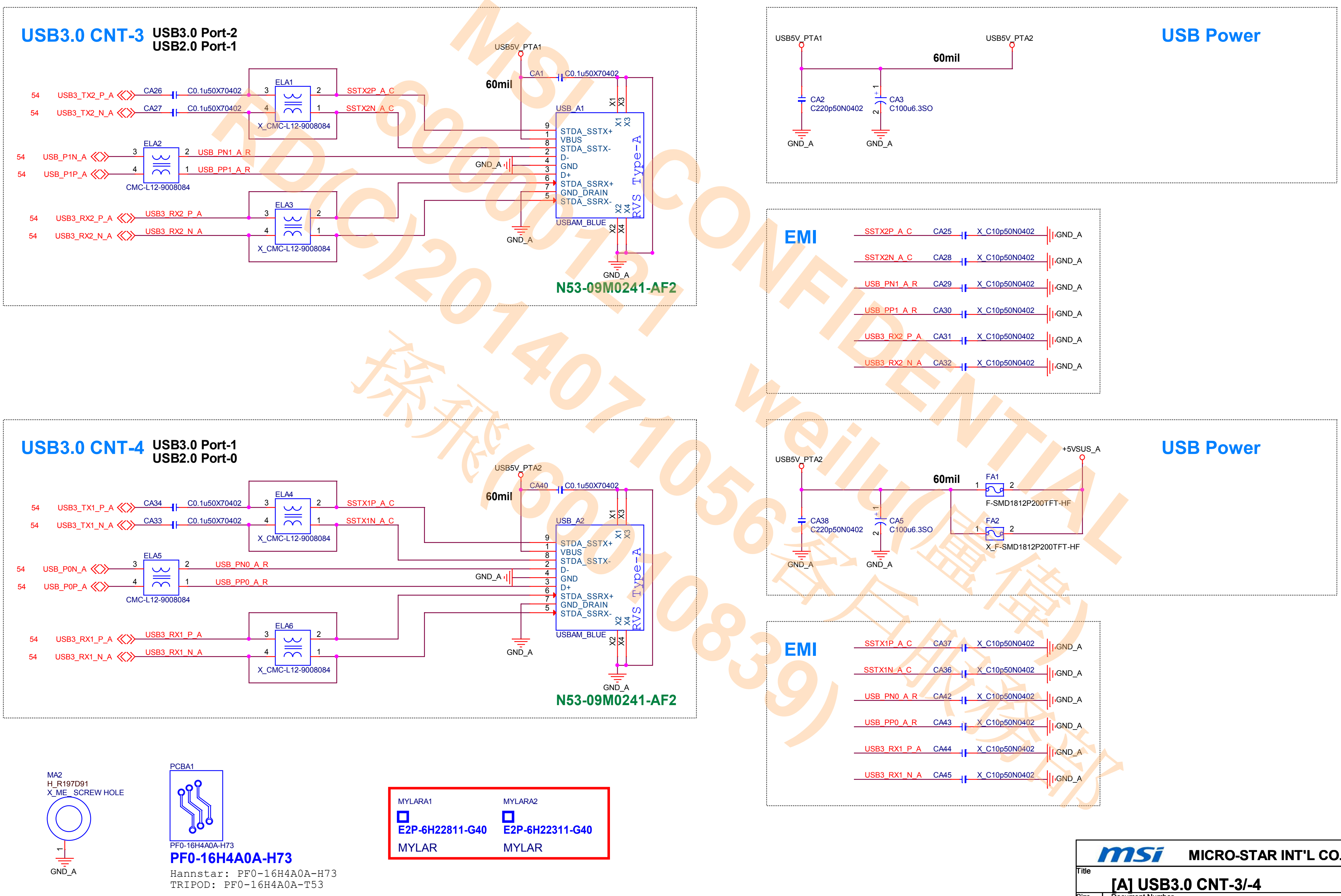
[A] USB3.0 CNT-2/-3



MICRO-STAR INT'L CO.,LTD.

Title: [A] USB3.0 CNT-3/-4

Size | Document Number: MS-16H4 | Rev: 0A

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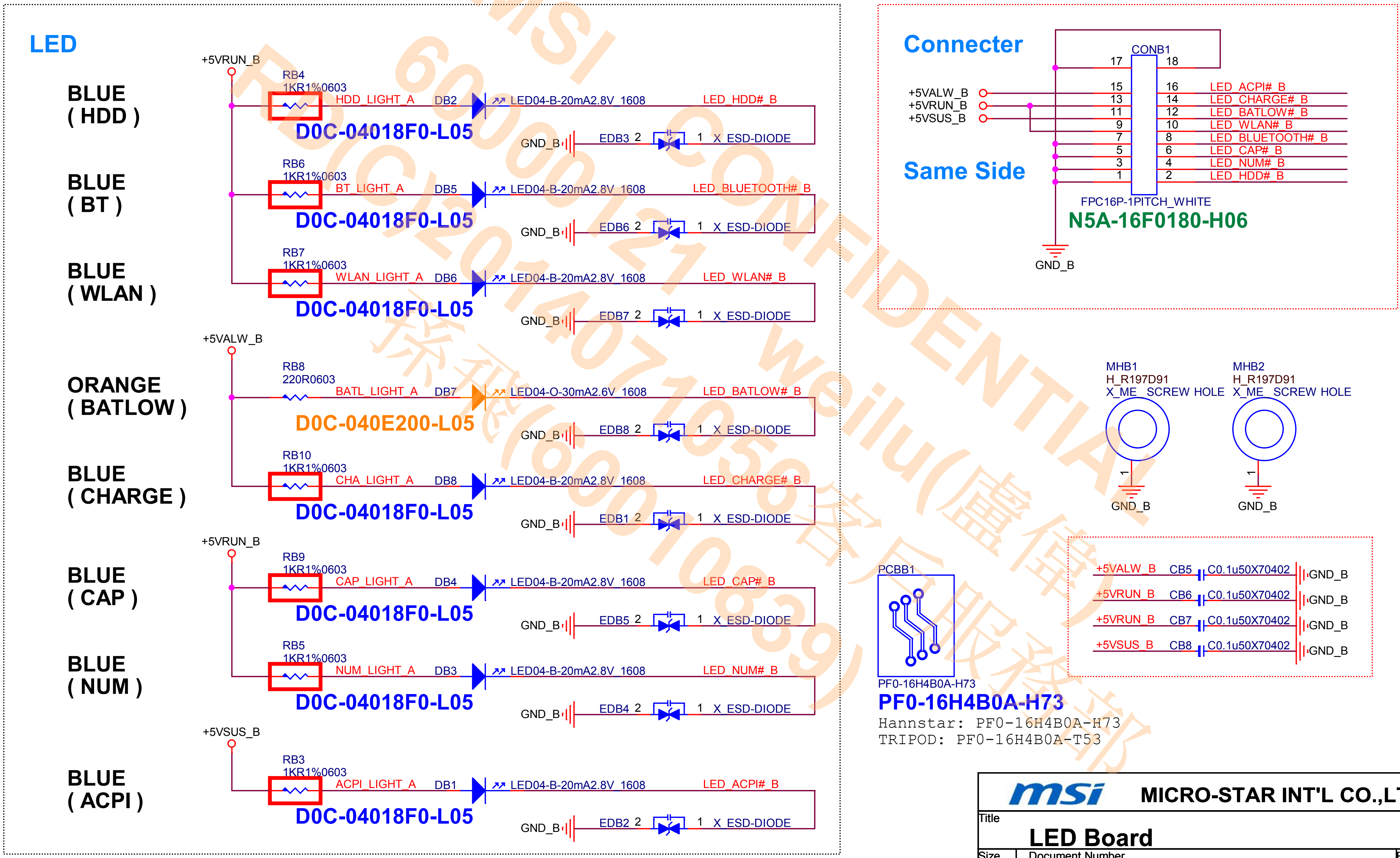
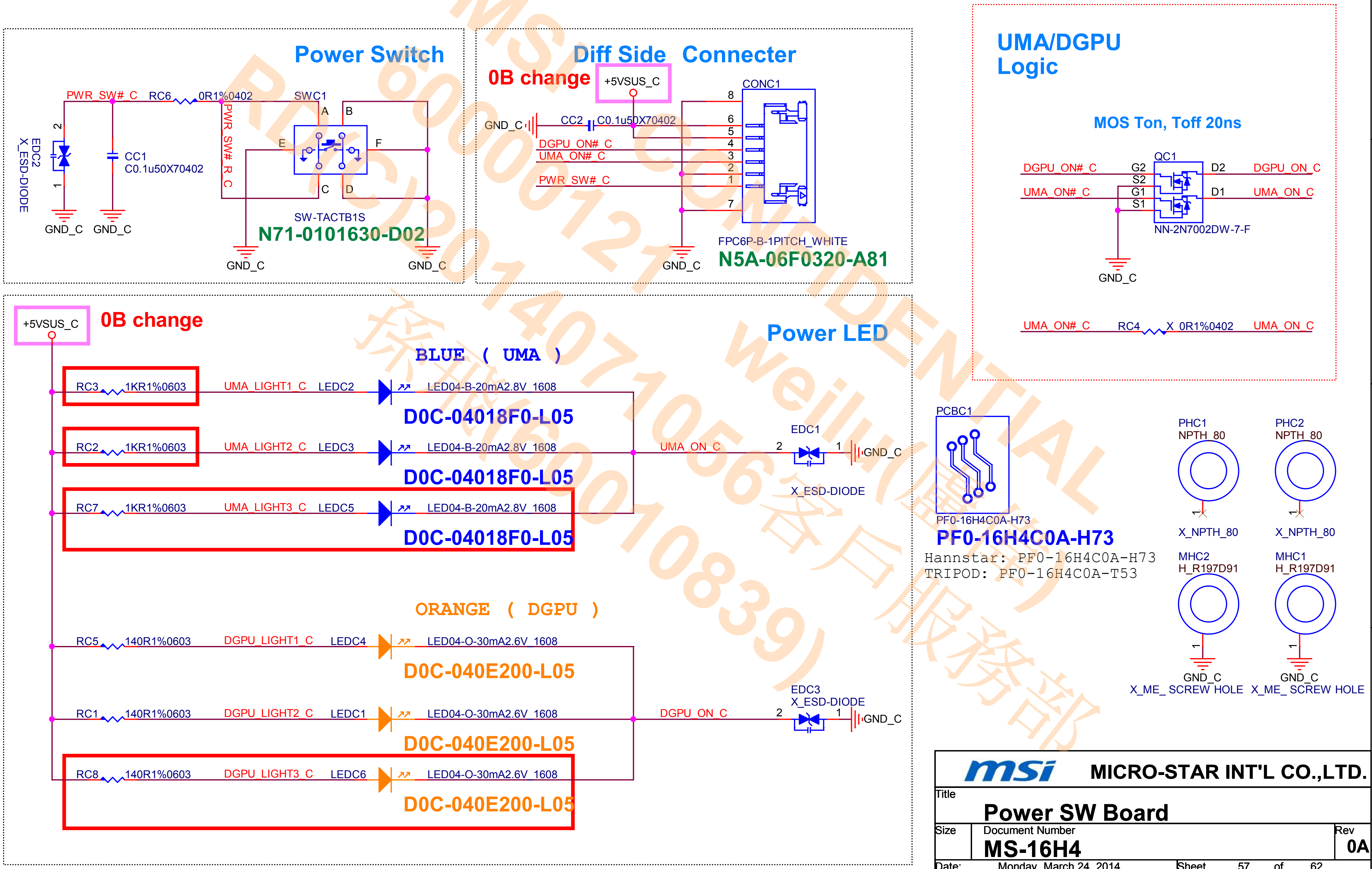
16H4-B Board (LED Board)



MICRO-STAR INT'L CO.,LTD.

Title	LED Board	
Size	Document Number: MS-16H4	Rev: 0A
Date: Monday, March 24, 2014	Sheet 56 of 62	

16H4-C Board (Power SW Board)

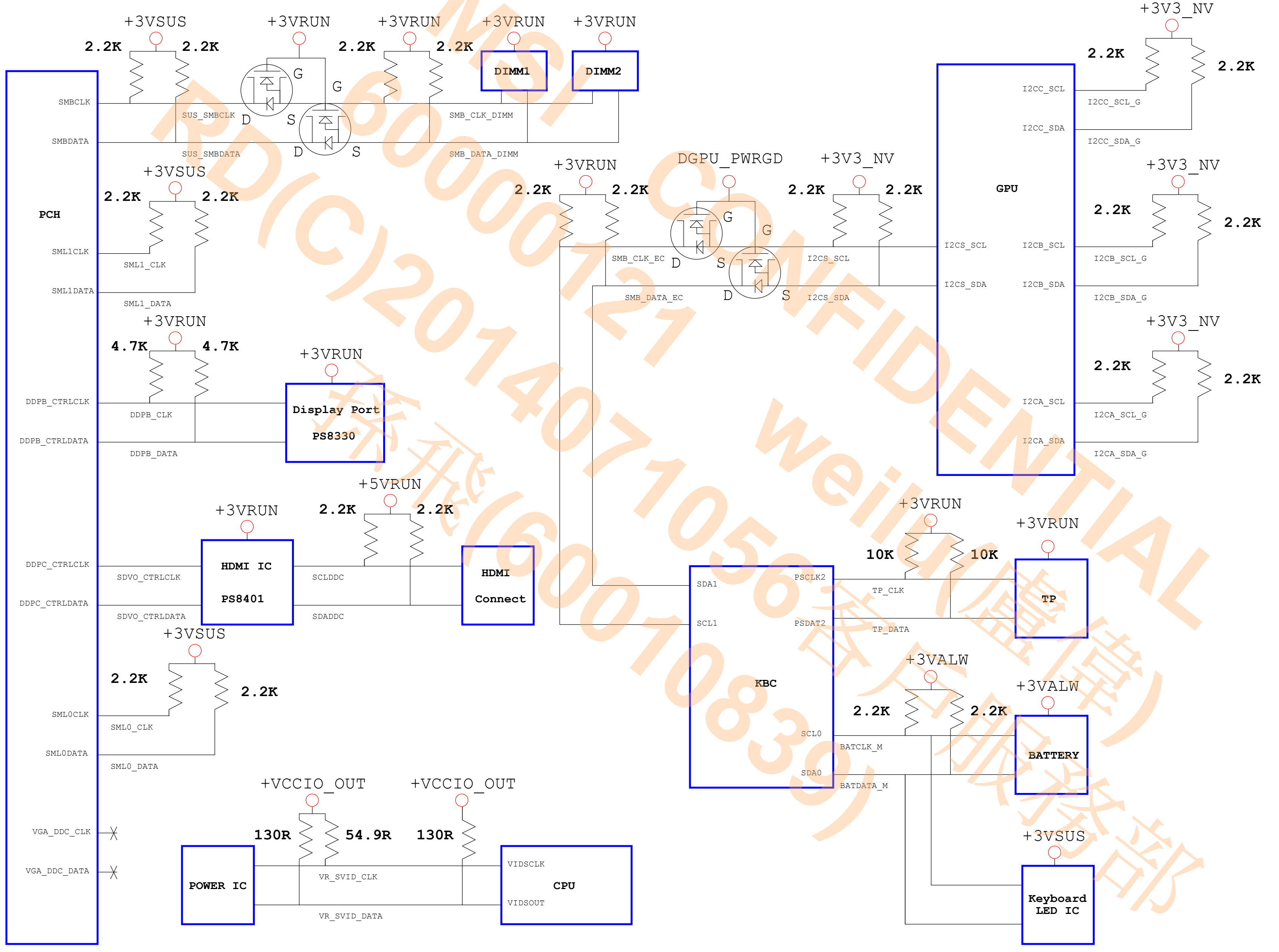


MICRO-STAR INT'L CO.,LTD.

Title: **Power SW Board**

Size | Document Number: **MS-16H4** | Rev: **0A**

Date: Monday, March 24, 2014 | Sheet 57 of 62



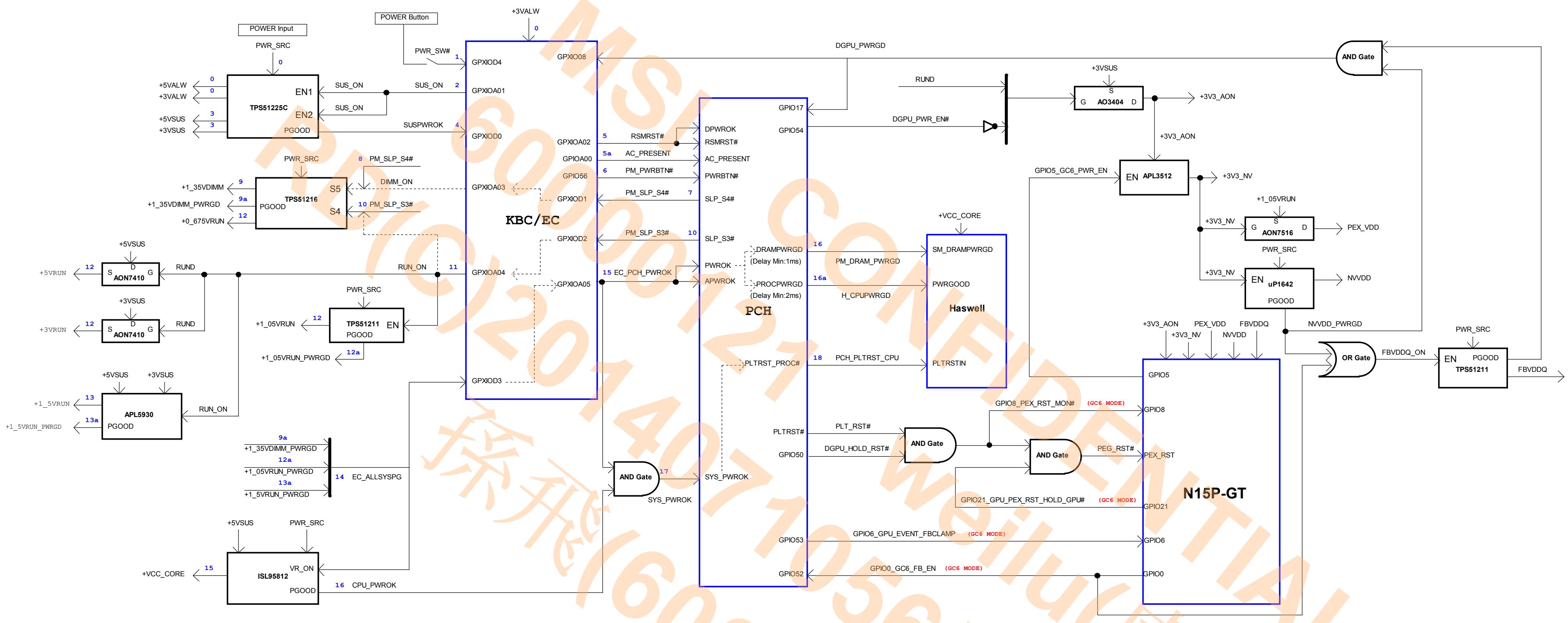
MICRO-STAR INT'L CO.,LTD.

Title: SMB Topology

Size | Document Number: MS-16H4 | Rev: 0A

Date: Monday, March 24, 2014 | Sheet 58 of 62

MS-16H4 Power on Block Diagram



MICRO-STAR INT'L CO.,LTD.

Title	Power on Block Diagram	
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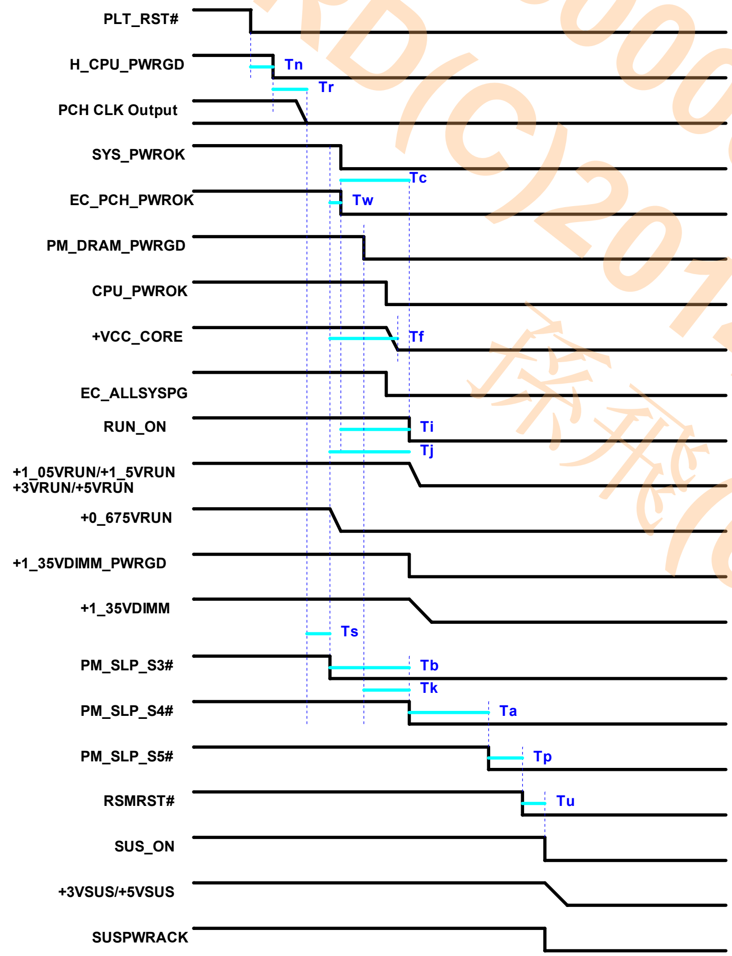
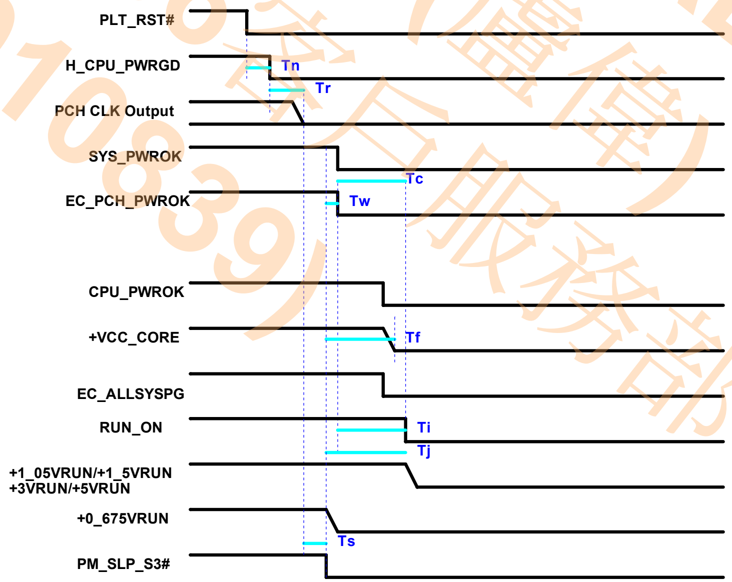
Power down Sequence

	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> G3



S0 -> S3



msi MICRO-STAR INT'L CO.,LTD.
Title: Power down Sequence
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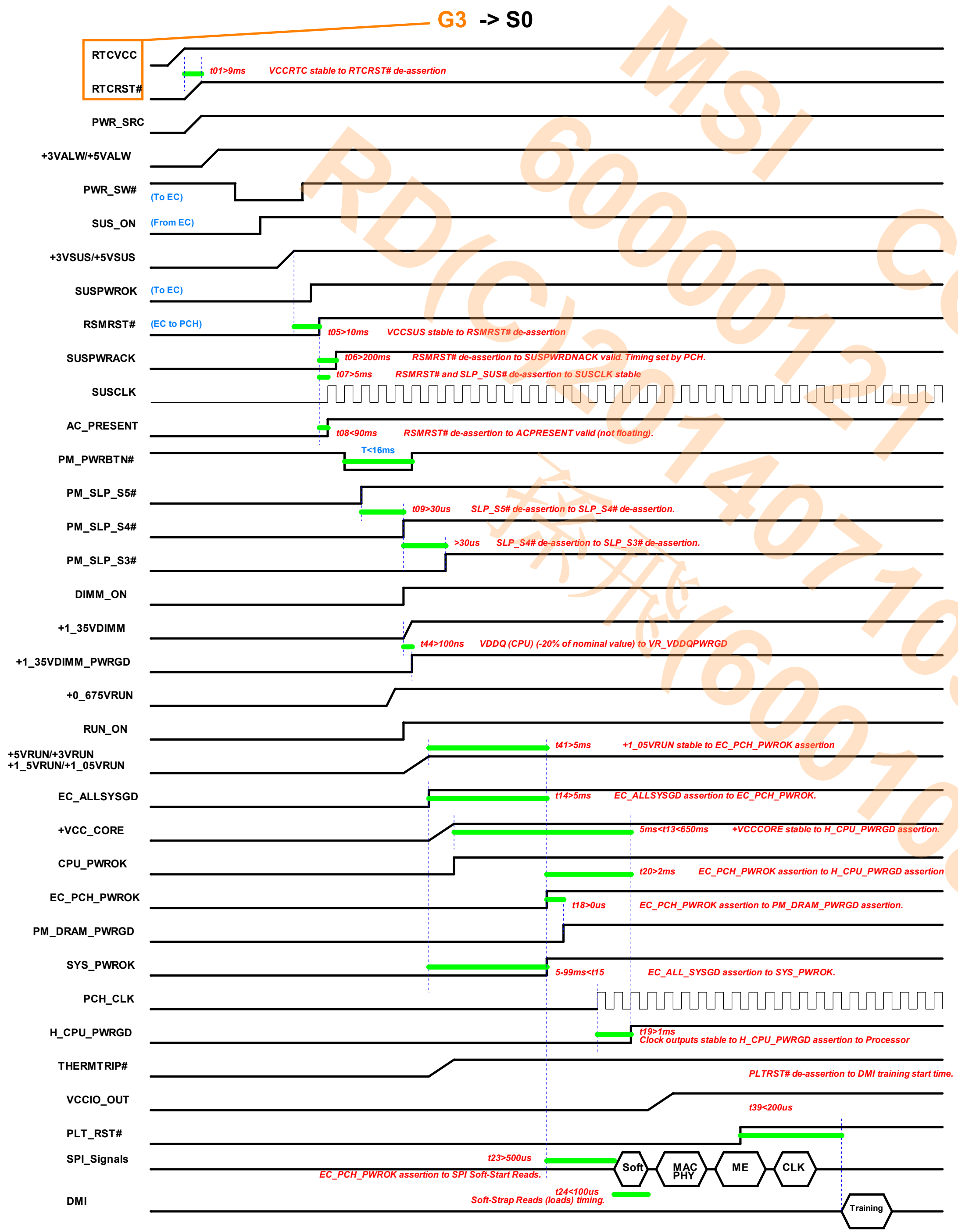
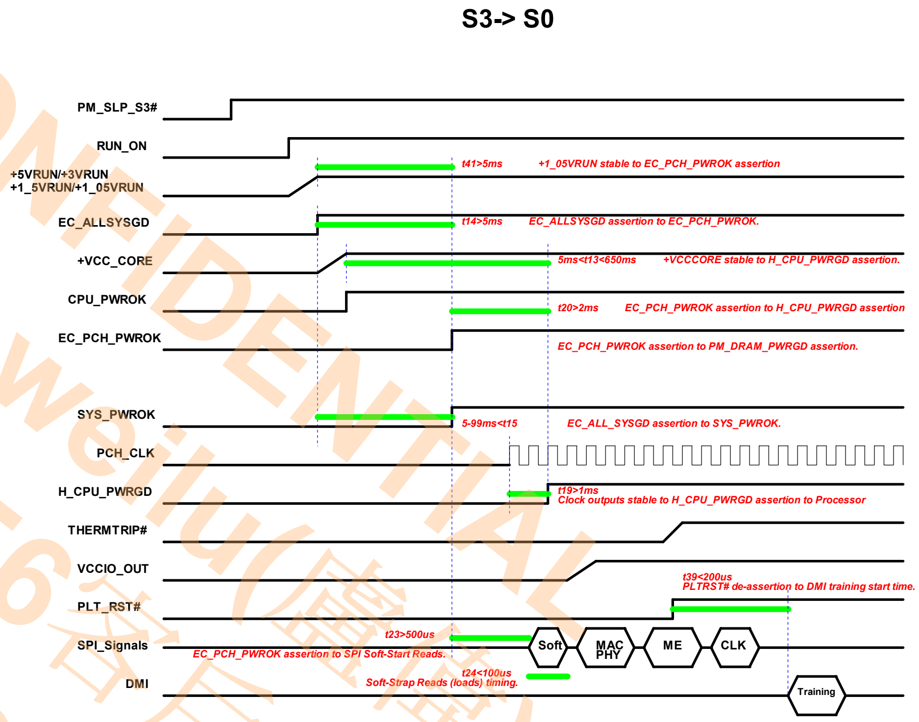
Power on Sequence





msi MICRO-STAR INT'L CO.,LTD.
Title: Power on Sequence
Size | Document Number: MS-16H4 | Rev: 0A
Date: Monday, March 24, 2014 | Sheet 61 of 62

History

0A: 2014/2/17

01. P11 NVVDD_SENSE change NVVDD_SENSE_GPU TO GPU VDD_SENSE
    NVVDD_GND_SENSE change NVVDD_GND_SENSE_GPU TO GPU GND_SENSE
    PCIE_RST# change PEG_RST# TO GPU PEX_RST

02. P17 ADD R3106 R3092 TO +3V3_AON

03. P18 ADD C3236 TO Q3006 PIN G2
    ADD R3289 TO Q3002 PIN D
    ADD R3288 TO Q3001 PIN D
    change R3011 R3094 R3086 R3108 TO +3V3_AON
    change R3105 R3091 TO +3V3_AON
    ADD R3110 R3093 R3111 R3100 TO +3V3_AON
    PCIE_RST# change PEG_RST# TO R3073

04. P20 ADD R3210 FBVDDQ_PWRGD TO U3006 PIN 2
    ADD R3067 C3073 PQ3037 TO PQ3007 PIN G1
    ADD PR3087 TO D3003 PIN Z
    DEL PQ3016 PC3064 TO PQ3015 PIN D2
    PR3088 470K change 200K
    PWR_SRC change +5VSUS TO PR3091
    PWR_SRC change +5VSUS TO PR3086

05. P24 U9 Footprint SPIFLASH8 change SIC8_SST_S2A

06. P26 DGPU_SELECT# change GPIO0_GC6_FB_EN TO PCH GPIO52
    ADD GPIO6_GPU_EVENT_FBCLAMP TO PCH GPIO53
    ADD R400 R401 U18 TO U7 PIN 4
    ADD GPIO8_PEX_RST_MON# TO U7 PIN4
    ADD GPIO21_GPU_PEX_RST_HOLD_GPU# TO U18 PIN2
    PCIE_RST# change PEG_RST# TO R93

07. P34 GPU_ACIN1 change GPU_ACIN TO EC GPIO07
    ADD OVERT# TO EC GPXIOA06
    EC_PROTECT_PWR TO EC GPIO40
    DEL FB_CLAMP TO EC GPIO0D
    DEL FB_CLAMP_REQ# TO EC GPIO0A

08. P45 DEL PQ40

09. P47 ADD R153 RUN_ON TO PU5 S3

10. P49 DEL PR83 FB_VDDQ_SENSE TO PR1
    DGPU_PWRGD change FBVDDQ_PWRGD TO PU6 PGOOD
    PWR_SRC_FBVDDQ change PWR_SRC TO PQ1 PIN 5

11. P50 DEL PR113 PS1_NVVDD_EN_INA TO PU7 EN
    3V3_NV change +3V3_NV TO PR36
    3V3_NV change +3V3_NV TO PR97
    PWR_SRC_NVVDD change PWR_SRC TO PQ15 PIN1
    PWR_SRC_NVVDD change PWR_SRC TO PQ4 PIN1

12. P52 PWR_SRC_NVVDD change PWR_SRC TO EC54
    PWR_SRC_FBVDDQ change PWR_SRC TO EC57

2014/2/18

1. P50 PR109 39K change 20K
   PR106 36K change 20K
   PR107 1.5K change 2K
   PR41 30K change 18K
   PR39 1.5K change 0
   PC127 1.5nF change 2.7nF

2014/2/19

1. P33 ADD R155 R156 TO +5VSUS_LED_KB
   +5VSUS change +5VSUS_LED_KB TO FPC15 PIN 1
   ADD U27
   ADD C533 TO U27 VO
   ADD C676 TO U27 VIN
   ADD C675 TO U27 SS
   ADD R154 TO U27 EN
   ADD LED_KB_PWR_EN TO U27 EN

2. P34 ADD LED_KB_PWR_EN TO EC GPIO0D

2014/2/20

1. P12 ADD R3183 TO G3000 PIN FBA_CMD34
   ADD R3184 TO G3000 PIN FBA_CMD35

2. P18 ADD C3093 TO G3000 PIN SP_PLLVDD
   ADD Q3007 R3065 R3270 TO G3000 PIN GPIO6
   ADD Q3010 R3069 R3271 TO G3000 PIN GPIO8
   ADD Q3012 R3070 R3267 TO G3000 PIN GPIO9

3. P45 ADD PD4 TO +DC_IN

2014/2/21

1. P13 ADD C3296 C3320 C3322 C3323 TO FBVDDQ

2. P14 ADD C3326 C3327 C3324 C3325 TO FBVDDQ

3. P15 ADD C3078 C3084 C3094 C3107 TO FBVDDQ

4. P15 ADD C3328 C3329 C3330 C3331 C3332 TO FBVDDQ

2014/2/25

1. P32 ADD R260 TO FPC5 PIN 40

2. P37 ADD C767 C765 C768 C766 C772 C770 C771 C769 TO +3RUN

3. P11-- P20 Rename

2014/2/26

1. P51 PC20 Footprint F_C0402 change N_C0603_NB
   PC38 Footprint F_C0402 change N_C0603_NB
   PC114 Footprint F_C0402 change N_C0603_NB
   PR13 Footprint F_R0402 change N_R0603_NB
   PR43 Footprint F_R0402 change N_R0603_NB
   PR89 Footprint F_R0402 change N_R0603_NB

2014/3/3

1. P03 R39 Footprint F_R0402 change NC_0402_6
   R50 Footprint F_R0402 change NC_0402_6

2. P26 DEL R400
   DEL R42

3. P32 DEL R260
   DEL R259
   UB1 change U31

4. P33 DEL R366
   DEL R365

5. P35 ER9 Footprint F_R0402 change NC_0402_6
   ER10 Footprint F_R0402 change NC_0402_6
   ER11 Footprint F_R0402 change NC_0402_6
   ER13 Footprint F_R0402 change NC_0402_6
   ER14 Footprint F_R0402 change NC_0402_6

6. P41 DEL L1
   DEL L2
   ADD JNC16 TO DVDDL

7. P42 UB2 change U32

8. P54 DEL USB_ENABLE_A

9. P55 DEL UA2
   DEL UA1
   DEL CA6
   DEL CA4
   DEL USB_ENABLE_A
   ADD FA1 TO +5VSUS_A

2014/3/5

1. P52 L12_DIFF_4.5/4.5/4.5_85OHM-changeL10_DIFF_4.5/4.5/4.5_85OHM-
   L12_DIFF_4.5/4.5/4.5_85OHM+changeL10_DIFF_4.5/4.5/4.5_85OHM+
   L12_DIFF_4.5/4/4.5_80OHM-changeL10_DIFF_4.5/4/4.5_80OHM-
   L12_DIFF_4.5/4/4.5_80OHM+changeL10_DIFF_4.5/4/4.5_80OHM+
   L12_DIFF_4/6/4_90OHM- changeL10_DIFF_4/6/4_90OHM-
   L12_DIFF_4/6/4_90OHM+ changeL10_DIFF_4/6/4_90OHM+
   L12_DIFF_3.5/7.5/3.5_100OHM-changeL10_DIFF_3.5/7.5/3.5_100OHM-
   L12_DIFF_3.5/7.5/3.5_100OHM+changeL10_DIFF_3.5/7.5/3.5_100OHM+
   L12_5.5MIL_45_OHM changeL10_5.5MIL_45_OHM
   L12_4MIL_50_OHM changeL10_4MIL_50_OHM
   L10_DIFF_4.5/7/4.5_80OHM-changeL8_DIFF_4.5/7/4.5_80OHM-
   L10_DIFF_4.5/7/4.5_80OHM+changeL8_DIFF_4.5/7/4.5_80OHM+
   L10_DIFF_4/6.5/4_85OHM-changeL8_DIFF_4/6.5/4_85OHM-
   L10_DIFF_4/6.5/4_85OHM+changeL8_DIFF_4/6.5/4_85OHM+
   L10_DIFF_3.5/5.5/3.5_90OHM-changeL8_DIFF_3.5/5.5/3.5_90OHM-
   L10_DIFF_3.5/5.5/3.5_90OHM+changeL8_DIFF_3.5/5.5/3.5_90OHM+
   L10_DIFF_3.5/4.5/3.5_88OHM-changeL8_DIFF_3.5/4.5/3.5_88OHM-
   L10_DIFF_3.5/4.5/3.5_88OHM+changeL8_DIFF_3.5/4.5/3.5_88OHM+
   L10_DIFF_3/10/3_100OHM-changeL8_DIFF_3/10/3_100OHM-
   L10_DIFF_3/10/3_100OHM+changeL8_DIFF_3/10/3_100OHM+
   L10_5MIL_40_OHM changeL8_5MIL_40_OHM
   L10_4MIL_45_OHM changeL8_4MIL_45_OHM
   L10_3MIL_50_OHM changeL8_3MIL_50_OHM
   GND11 changeGND9
   GND9_GND11 changeGND7_GND9

2014/3/6

1. P22 SATA1TXP change SATA5TXP TOU14 PINSATA_TXP5
   SATA1TXN change SATA5TXN TOU14 PINSATA_TXN5
   SATA1RXP change SATA5RXP TOU14 PINSATA_RXP5
   SATA1RXN change SATA5RXN TOU14 PINSATA_RXN5

2. P28 USB3_TX5_P change USB3_TX3_PTO U14 PIN USB3TP3
   USB3_TX5_N change USB3_TX3_NTO U14 PIN USB3TN3
   USB3_RX5_P change USB3_RX3_PTO U14 PIN USB3RP3
   USB3_RX5_N change USB3_RX3_NTO U14 PIN USB3RN3

3. P36 USB3_TX5_P change USB3_TX3_PTO C231
   USB3_TX5_N change USB3_TX3_NTO C230
   USB3_RX5_P change USB3_RX3_PTO USB_CON1 PIN6
   USB3_RX5_N change USB3_RX3_NTO USB_CON1 PIN5
   SSTX5P_C change SSTX3P_CTO C231
   SSTX5N_C change SSTX3N_CTO C230

4. P43 SATA1RXN change SATA5RXNTO C759
   SATA1RXP change SATA5RXPTO C758
   SATA1TXN change SATA5TXNTO C760
   SATA1TXP change SATA5TXPTO C761
   SATA1RXN_C change SATA5RXN_CTO C759
   SATA1RXP_C change SATA5RXP_CTO C758
   SATA1TXN_C change SATA5TXN_CTO C760
   SATA1TXP_C change SATA5TXP_CTO C761

2014/3/7

1. P06 DEL TPJNC24
   ADD R217 TO U68 PIN PWR_DEGUG

2014/3/7

1. P03 DEL NET VIA_H_CATERR# TO U68 PIN G50
   DEL NET VIA_XDP_PREQ# TO U68 PIN N52
   DEL NET VIA_XDP_TMS TO U68 PIN M51
   DEL NET VIA_XDP_TDI TO U68 PIN N49
   DEL NET VIA_XDP_TDO TO U68 PIN M49
   DEL NET VIA_XDP_DBRESET# TO U68 PIN F53

2. P22 DEL NET VIA_JTAG_TMS TO U14 PIN AD1
   DEL NET VIA_JTAG_TDO TO U14 PIN AD3
   DEL NET VIA_JTAG_TDI TO U14 PIN AE2
   DEL NET VIA_JTAG_TCK TO U14 PIN AB3

3. P23 DEL NET VIA_TP_CLK_FLEX0 TO U14 PIN C40
   DEL NET VIA_TP_CLK_FLEX3 TO U14 PIN F39

4. P55 ADD FA2