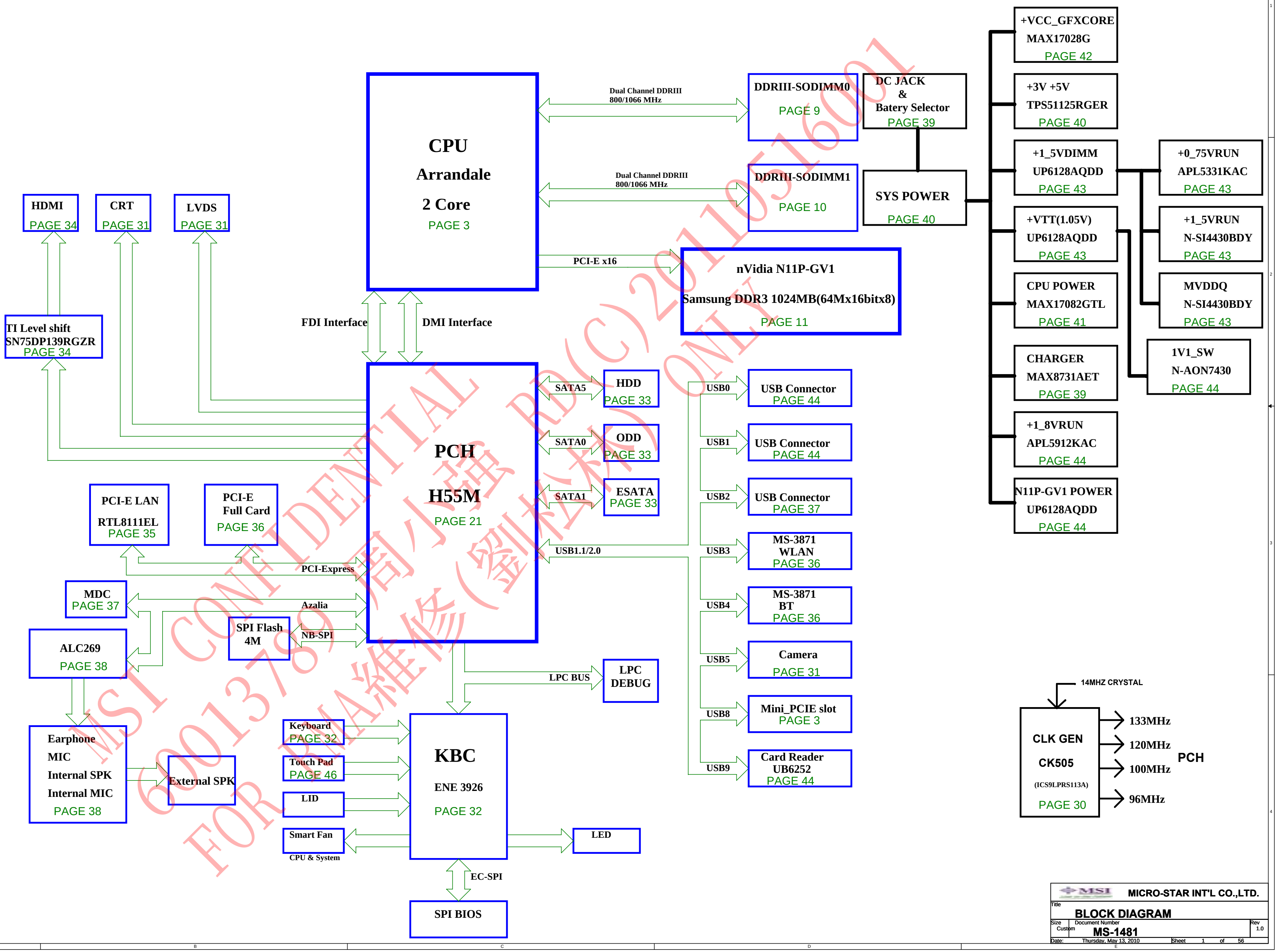
MS-1481 Ver : 1.0

Calpella Platform

Release Date :2010/05/13

Table of Contents



CPU
Arrandale
2 Core
PAGE 3
Dual Channel DDRIII 800/1066 MHz
DDRIII-SODIMM0
PAGE 9
Dual Channel DDRIII 800/1066 MHz
DDRIII-SODIMM1
PAGE 10
DC JACK & Batery Selector
PAGE 39
SYS POWER
PAGE 40
+VCC_GFXCORE
MAX17028G
PAGE 42
+3V +5V
TPS51125RGER
PAGE 40
+1_5VDIMM
UP6128AQDD
PAGE 43
+0_75VRUN
APL5331KAC
PAGE 43
+VTT(1.05V)
UP6128AQDD
PAGE 43
+1_5VRUN
N-SI4430BDY
PAGE 43
CPU POWER
MAX17082GTL
PAGE 41
MVDDQ
N-SI4430BDY
PAGE 43
CHARGER
MAX8731AET
PAGE 39
1V1_SW
N-AON7430
PAGE 44
+1_8VRUN
APL5912KAC
PAGE 44
N11P-GV1 POWER
UP6128AQDD
PAGE 44
PCI-E x16
nVidia N11P-GV1
Samsung DDR3 1024MB(64Mx16bitx8)
PAGE 11
HDMI
PAGE 34
CRT
PAGE 31
LVDS
PAGE 31
TI Level shift
SN75DP139RGZR
PAGE 34
FDI Interface
DMI Interface
PCH
H55M
PAGE 21
SATA5
HDD
PAGE 33
SATA0
ODD
PAGE 33
SATA1
ESATA
PAGE 33
USB1.1/2.0
USB0
USB Connector
PAGE 44
USB1
USB Connector
PAGE 44
USB2
USB Connector
PAGE 37
USB3
MS-3871
WLAN
PAGE 36
USB4
MS-3871
BT
PAGE 36
USB5
Camera
PAGE 31
USB8
Mini_PCIE slot
PAGE 3
USB9
Card Reader
UB6252
PAGE 44
PCI-E LAN
RTL8111EL
PAGE 35
PCI-E
Full Card
PAGE 36
PCI-Express
MDC
PAGE 37
Azalia
SPI Flash
4M
NB-SPI
ALC269
PAGE 38
LPC BUS
LPC
DEBUG
Earphone
MIC
Internal SPK
Internal MIC
PAGE 38
External SPK
Keyboard
PAGE 32
Touch Pad
PAGE 46
LID
Smart Fan
CPU & System
KBC
ENE 3926
PAGE 32
LED
EC-SPI
SPI BIOS
14MHZ CRYSTAL
CLK GEN
CK505
(ICS9LPRS113A)
PAGE 30
133MHz
120MHz
100MHz
96MHz
PCH

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	BLOCK DIAGRAM	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 1 of 56	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

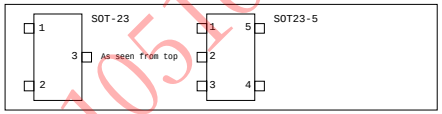
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
N11P_VDD_CORE	0.85V	S0	GPU core power
MVDDQ	1.5V	S0	GPU DDR3 power
1V1_SW	1.05V	S0	GPU PCIE power
+3VRUN_N11P	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

Suffix
\# = Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

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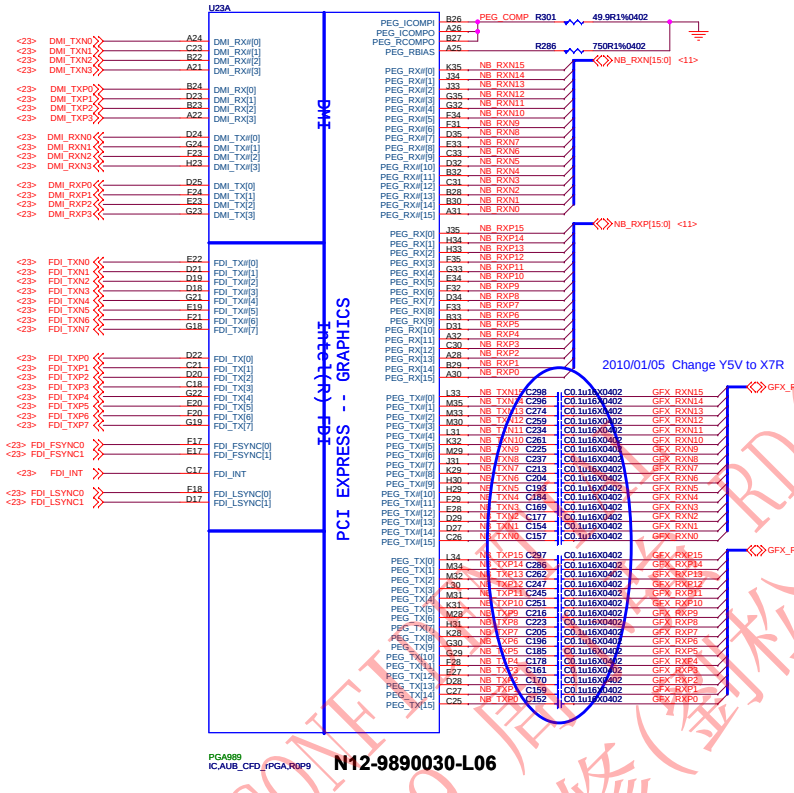
Title: PLATFORM
Size: Custom | Document Number: MS-1481 | Rev: 1.0
Date: Thursday, May 13, 2010 | Sheet 2 of 56

ARRANDALE PROCESSOR (CLK,MISC,JTAG)

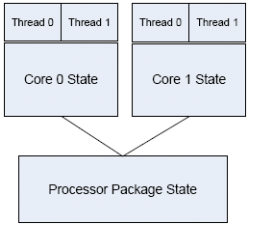


Westmere (formerly Nehalem-C) is the name given to the 32 nm die shrink of Nehalem.

Brand Name	Model (list)	L3 Cache size	Thermal Design Power
Intel Core i3	i3-3xxM	3 MB	35 W
Intel Core i5	i5-4xxM	3 MB	35 W
	i5-5xxM	3 MB	35 W
Intel Core i7	i7-6xxUM	4 MB	18 W
	i7-6xxLM	4 MB	25 W
	i7-6xxM	4 MB	35 W

The Core i3-3xx will be similar to the Core i5-4xx series but running at lower clock speeds and without Turbo Boost

Brand							
Segment	POP1	POP2	POP3	ULV1	ULV2	LV1	LV2
TDP	35W	35W	35W	18W	18W	25W	25W
Cores/ Threads	2/4	2/4	2/4	2/4	2/4	2/4	2/4
CPU Base Freq (GHz)	2.40	2.53	2.66	1.06	1.2	2.00	2.13
Intel® Turbo Boost Technology Max 8C Turbo (GHz)	2.93	3.06	3.33	2.13	2.26	2.80	2.93
DDR3 (MHz)	1066MHz	1066MHz	1066MHz	800MHz	800MHz	1066MHz	1066MHz
L3 Cache	3MB	3MB	4MB	4MB	4MB	4MB	4MB
Integrated Gfx	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Gfx Base Render Frequency	500MHz	500MHz	500MHz	166MHz	166MHz	266MHz	266MHz
Intel® Turbo Boost Technology Max Gfx Render (MHz)	766MHz	766MHz	766MHz	500MHz	500MHz	566MHz	566MHz
Intel® Hyper-threading /VT/TXT/Intel® vPro	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package	BGA/rPGA	BGA/rPGA	BGA/rPGA	BGA	BGA	BGA	BGA

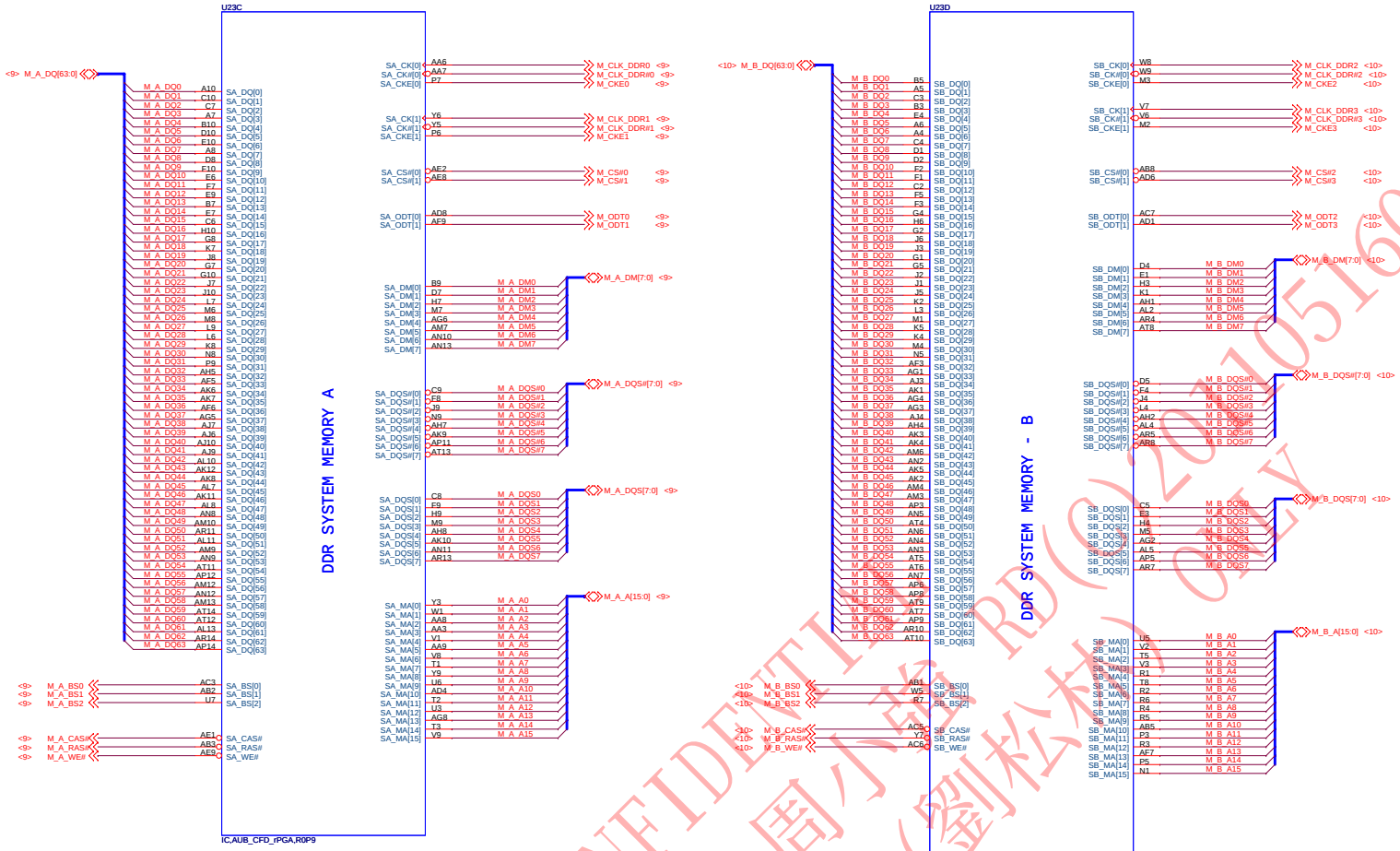


Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1			
		C0	C1	C3	C6
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	PROCESSOR(HOST BUS)	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 3 of 56	

ARRANDALE PROCESSOR (DDR3)



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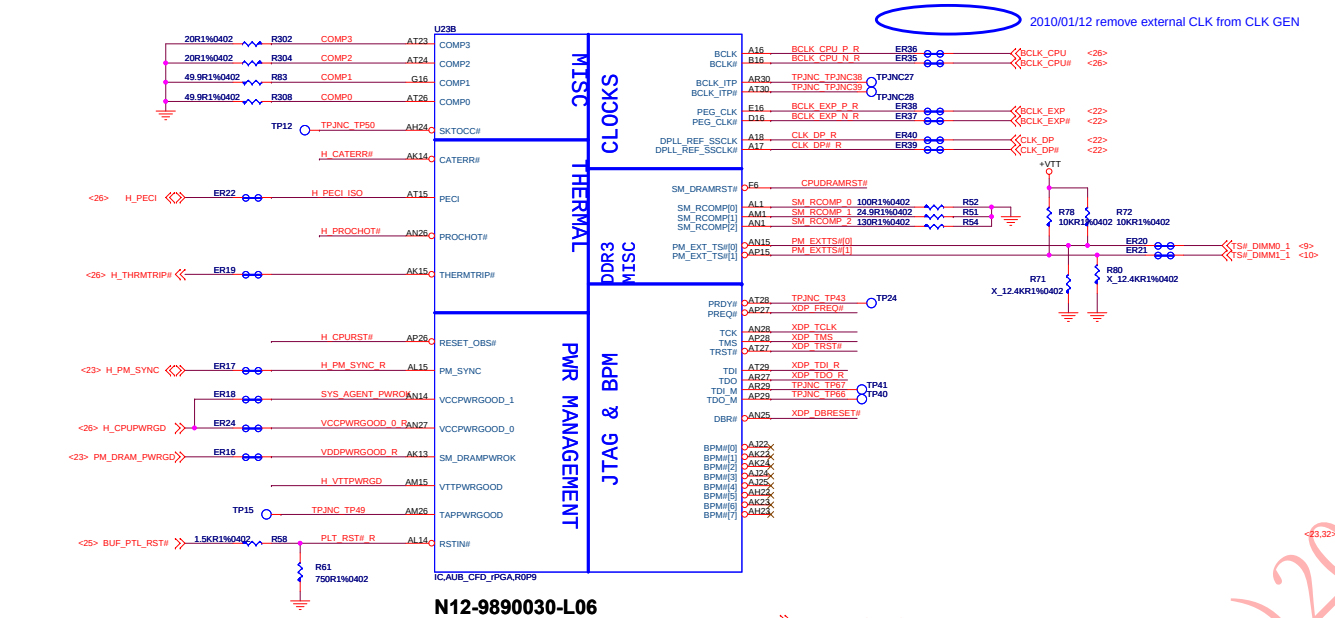
N12-9890030-L06

MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR(DDR3)

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 4 of 56



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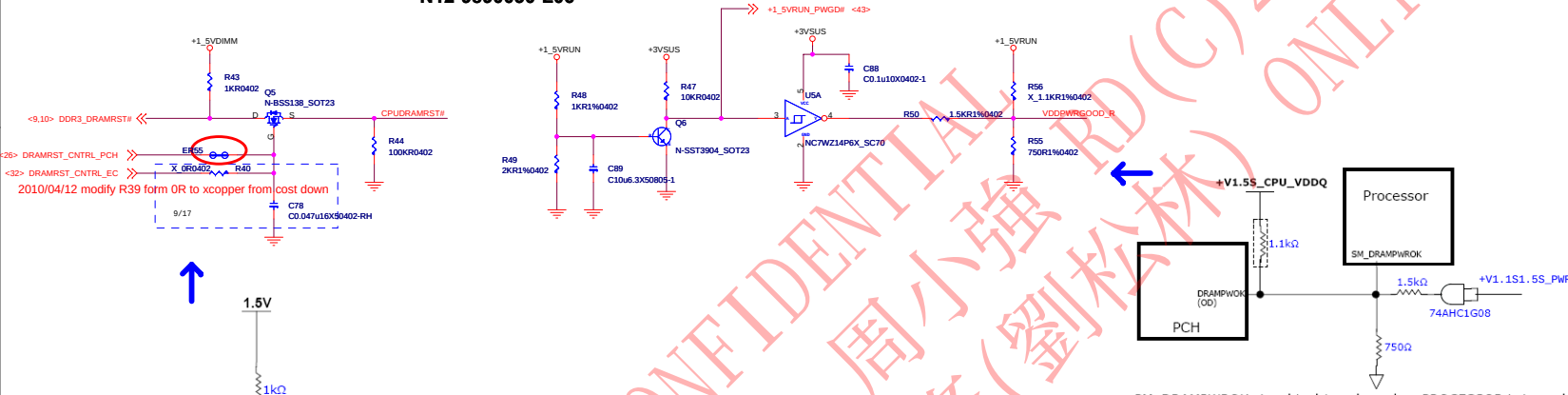
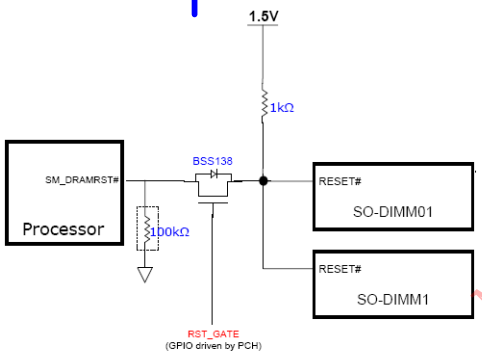




When Processor V_{DDQ} power is turned off in S3, SM_DRAMRST# will also go low with processor power. To avoid SM_DRAMRST# going low, a FET (e.g., BSS138) is added which is controlled using a PCH GPIO (RST_GATE). A Pull-up resistor of 1 kΩ to +1.5V_DIMM is added at SM_DRAMRST#_pin of SO-DIMM. Before system enters S3 (Before SLP_S3# going low), RST_GATE is driven low and FET is turned off. With a 1-kΩ PU on the SO-DIMM side, SM_DRAMRST# is maintained high during S3. When exiting S3, the FET will remain off until the integrated memory controller is reinitialized to drive the SM_DRAMRST# signal to a high level after the Processor V_{DDQ} power is restored.

SM_DRAMPWROK signal is driven low when PROCESSOR is turned off in S3 entry. During S3 exit, this signal is driven high only after +V1.5S_CPU_VDDQ stable. There is no timing requirement between and 0.75-V V_{TT} rail.

+V1.1S1.5S_PWRGD signal is an open-drain signal driven from +V1.5S_CPU_VDDQ PWRGOOD logic. It should go high only after +V1.5S_CPU_VDDQ to processor is stable.

DRAMPWROK behavior in S5/S4 to S0:

During S5/S4 to S0, DRAMPWROK is driven low by PCH until PCH_PWROK becomes high provided SLP_S4# is high. Even though DRAMPWROK derived from PWRGOOD of +V1.5S_CPU_VDDQ comparator, it is overdriven to low by PCH until PCH_PWROK goes high. This implementation ensures that S5 to S0 timings are maintained.

DRAMPWROK behavior in S0 to S3:

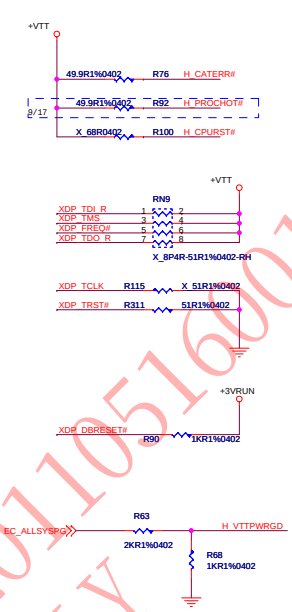
This signal is driven low as the +V1.1S1.5S_PWRGD becomes low when +V1.5S_CPU_VDDQ ramps down. To maintain this signal low, this AND gate is powered using SUS rail (+V3.3A). Any buffer/AND gate of 4 mA should work fine in the given circuit.

DRAMPWROK behavior in S3 to S0:

This signal is driven high when +V1.5S_CPU_VDDQ to the processor is stable

DRAMPWROK is 1.1-V/1.05-V signal to processor; hence a resistor divider is implemented to level translate the signal.

Refer to the latest Intel CRB schematics for more details on +V1.1S1.5S_PWRGD generation.

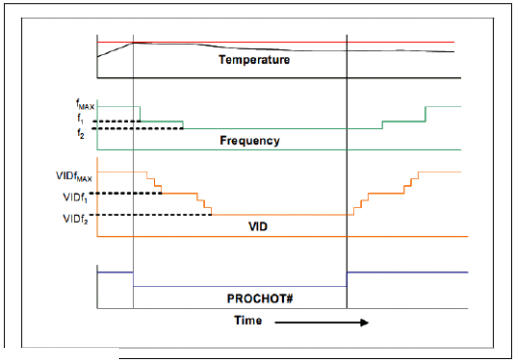


Arrandale Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory/Graphics
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI/Intel® FDI
DPLL_REF_SSCLK/DPLL_REF_SSCLK#	120 MHz	Embedded DisplayPort (eDP)

Signal Name	Description	Direction/Buffer Type
VCCPWRGOOD_0 VCCPWRGOOD_1	**VCCPWRGOOD_0 and VCCPWRGOOD_1 (Power Good) Processor Input:** The processor requires these signals to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. Both signals must then transition monotonically to a high state. VCCPWRGOOD_0 and VCCPWRGOOD_1 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of these signals. VCCPWRGOOD_0 and VCCPWRGOOD_1 should be tied together and connected to the PROCPWRGD output signal of the PCH.	I Asynchronous CMOS

Frequency and Voltage Ordering



MICRO-STAR INT'L CO.,LTD.
Title: PROCESSOR(CLK,THRM,PM,MSIC)
Size: Custom | Document Number: MS-1481 | Rev: 1.0
Date: Thursday, May 13, 2010 | Sheet 5 of 56

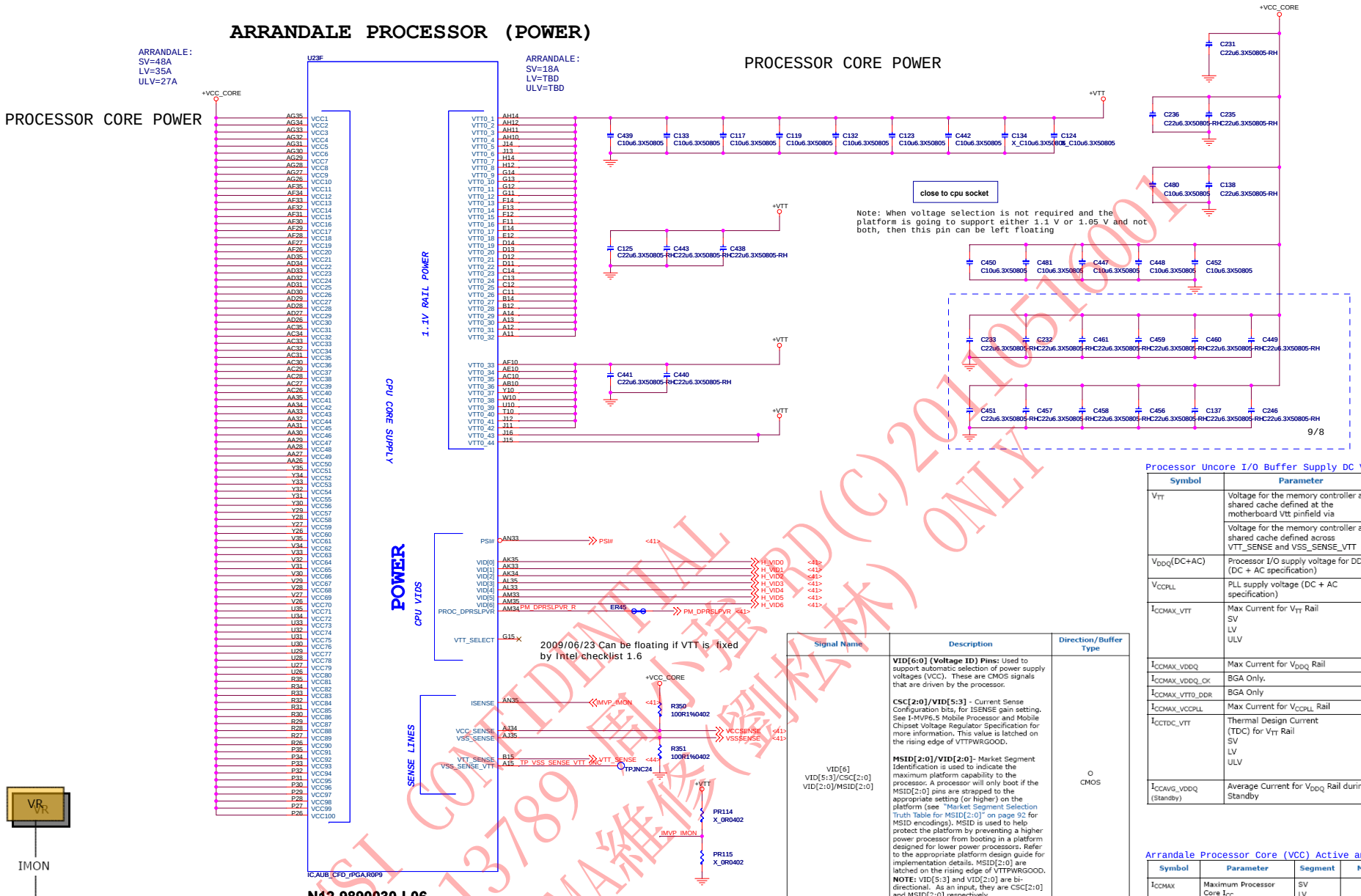
ARRANDALE PROCESSOR (POWER)

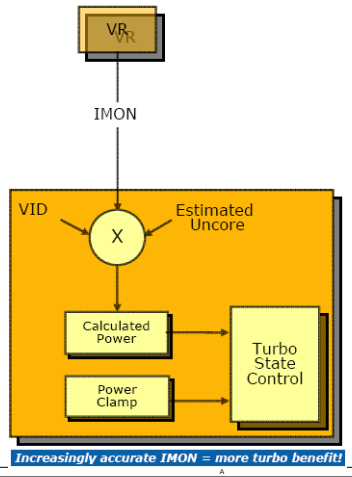
ARRANDALE:
SV=48A
LV=35A
ULV=27A

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER

PROCESSOR CORE POWER





Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{TT}	Voltage for the memory controller and shared cache defined at the motherboard Vtt pinfield via	0.9975	1.05	1.1025	V
	Voltage for the memory controller and shared cache defined across VTT_SENSE and VSS_SENSE_VTT	0.9765	1.05	1.1235	V
V_{DDQ}(DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	1.425	1.5	1.575	V
V_{CCPLL}	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V
I_{CCMAX_VTT}	Max Current for V_{TT} Rail SV LV ULV		-	 18 16 16	A
I_{CCMAX_VDDQ}	Max Current for V_{DDQ} Rail		-	3	A
$I_{CCMAX\_VDDQ\_CK}$	BGA Only.			0.2	A
$I_{CCMAX\_VTT0\_DDR}$	BGA Only			2.6	A
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail		-	1.35	A
I_{CCTDC_VTT}	Thermal Design Current (TDC) for V_{TT} Rail SV LV ULV		-	 18 16 16	A
I_{CCAVG_VDDQ} (Standby)	Average Current for V_{DDQ} Rail during Standby		-	0.33	A

Signal Name	Description	Direction/Buffer Type
VID[6] VID[5:3]/CSC[2:0] VID[2:0]/MSID[2:0]	**VID[6:0] (Voltage ID) Pins:** Used to support automatic selection of power supply voltages (VCC). These are CMOS signals that are driven by the processor. **CSC[2:0]/VID[5:3]** - Current Sense Configuration bits, for ISENSE gain setting. See I-MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulator Specification for more information. This value is latched on the rising edge of VTTPWRGOOD. **MSID[2:0]/VID[2:0]**- Market Segment Identification is used to indicate the maximum platform capability to the processor. A processor will only boot if the MSID[2:0] pins are strapped to the appropriate setting (or higher) on the platform (see "Market Segment Selection Truth Table for MSID[2:0]" on page 92 for MSID encodings). MSID is used to help protect the platform by preventing a higher power processor from booting in a platform designed for lower power processors. Refer to the appropriate platform design guide for implementation details. MSID[2:0] are latched on the rising edge of VTTPWRGOOD. **NOTE:** VID[5:3] and VID[2:0] are bi-directional. As an input, they are CSC[2:0] and MSID[2:0] respectively.	O CMOS

Arrandale Processor Core (VCC) Active and Idle Mode DC Voltage and Current

Symbol	Parameter	Segment	Min	Typ	Max	Unit
I_{CCMAX}	Maximum Processor Core I_{CC}	SV LV ULV			48 35 27	A
I_{CC_TDC}	Thermal Design I_{CC}	SV LV ULV			32 22 16	A
I_{CC_LFM}	I_{CC} at LFM	SV LV ULV			18 12 8	A
I_{C6}	I_{CC} at C6 Idle-state	SV LV ULV			0.3 0.3 0.3	A

Table 17. IA Core I_{MAX} and Gain Definition – Defined Relative to CPU Core Maximum Current

CPU SKU, $I_{CC\_CORE\text{-}MAX}$ Maximum CPU Core Current	I_{MAX} (IMON=900 mV min) [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
$I_{CC\_CORE\text{-}MAX}$ ≤20 A	20	001	45.0
20A< $I_{CC\_CORE\text{-}MAX}$ ≤30 A	30	010	30.0
30A< $I_{CC\_CORE\text{-}MAX}$ ≤40 A	40	011	22.5
40A< $I_{CC\_CORE\text{-}MAX}$ ≤50 A	50	100	18.0
50A< $I_{CC\_CORE\text{-}MAX}$ ≤60 A	60	101	15.0
60A< $I_{CC\_CORE\text{-}MAX}$ ≤70 A	70	110	12.9
70A< $I_{CC\_CORE\text{-}MAX}$ ≤90 A	90	111	10.0

Table 43. Market Segment Selection Truth Table for MSID[2:0]

MSID[2]	MSID[1]	MSID[0]	Description[1,2]
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Arrandale Standard Voltage (SV) 35W Supported
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR(POWER)

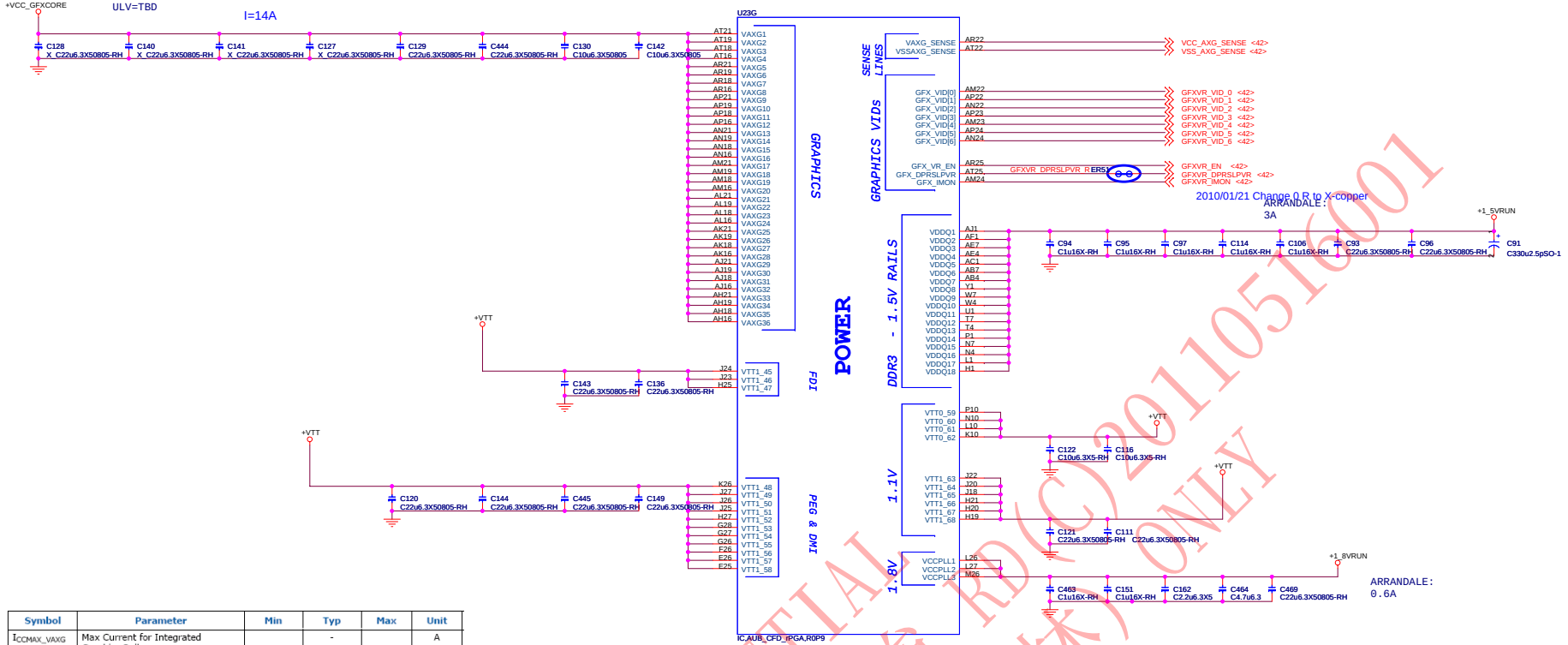
Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 6 of 56

ARRANDALE PROCESSOR (GRAPHICS POWER)

ARRANDALE:
SV=15A
LV=TBD
ULV=TBD

I=14A

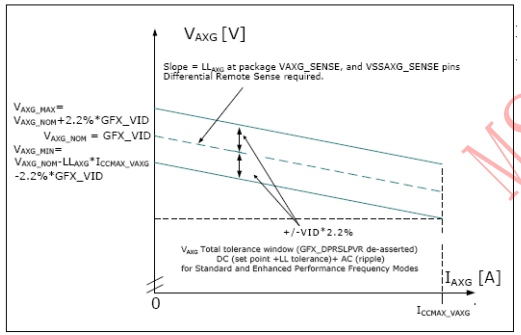


N12-9890030-L06

Symbol	Parameter	Min	Typ	Max	Unit
I_{CCMAX_VAXG}	Max Current for Integrated Graphics Rail SV LV ULV		-	 22 15 12	A
I_{CCTDC_VAXG}	Thermal Design Current (TDC) for Integrated Graphics Rail SV LV ULV		-	 12 7 6	A

Symbol	Parameter	Min	Typ	Max	Unit
V_{AXG}	Graphics core voltage		See Figure 15		

V_{AXG}/I_{AXG} Static and Ripple Voltage Regulation



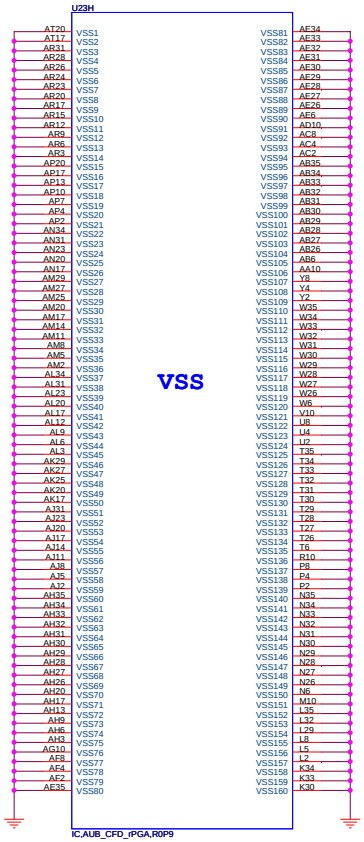
MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR(GRAPHICS POWER)

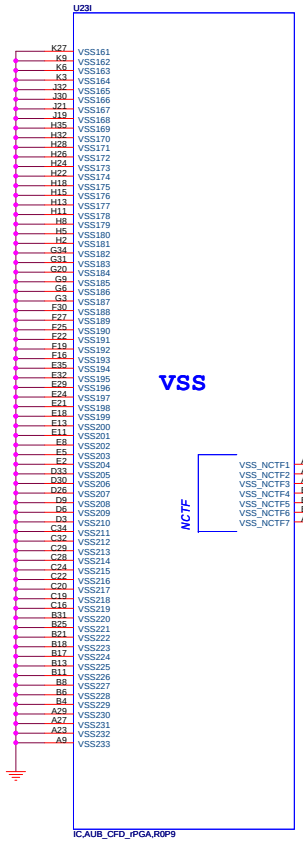
Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 7 of 56

ARRANDALE PROCESSOR (GND)

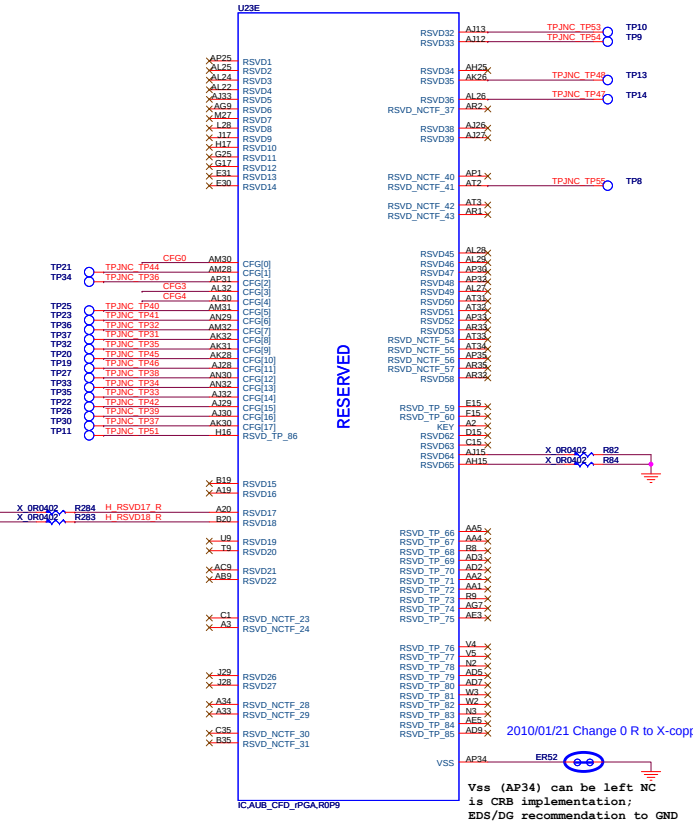


N12-9890030-L06



N12-9890030-L06

ARRANDALE PROCESSOR (RESERVED)



N12-9890030-L06

Processor Core/Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C1E	AutoHALT state with lowest frequency and voltage operating point.
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.

DMI States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

Integrated Memory Controller States

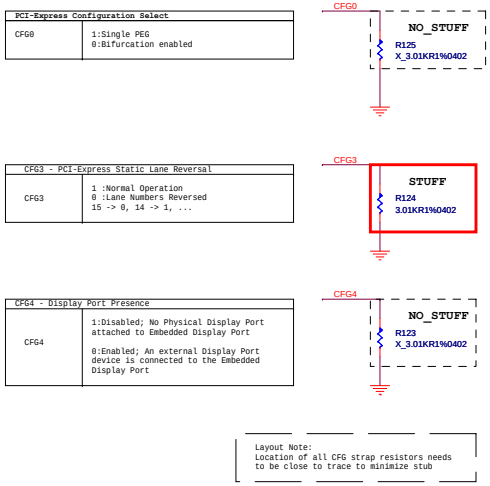
State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed.
Active Power down	CKE deasserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE deasserted using device self-refresh.

Integrated Graphics Controller States

State	Description
D0	Full on, display active.
D3 Cold	Power-off.

PCIe Link States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.



CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.

- 1: No lane reversal
- 0: Reversal

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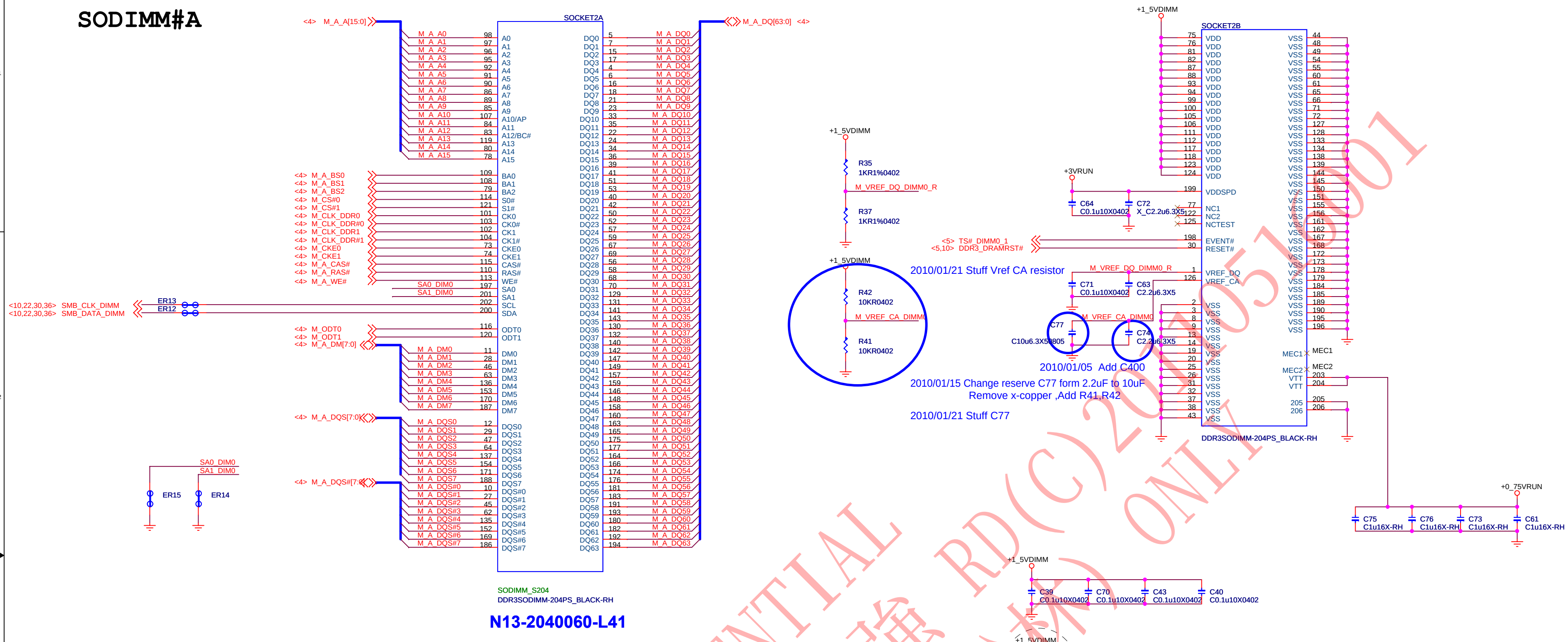
Title	PROCESSOR (GND)		
Size: Custom	Document Number: MS-1481		Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 8 of 56		

SODIMM#A



DDR3 SDRAM,2GB,667(1333)MHz,TRANSCEND/TS256MSK64V3U

IDD Specification parameters Definition
(IDD values are for full operating range of voltage and Temperature)

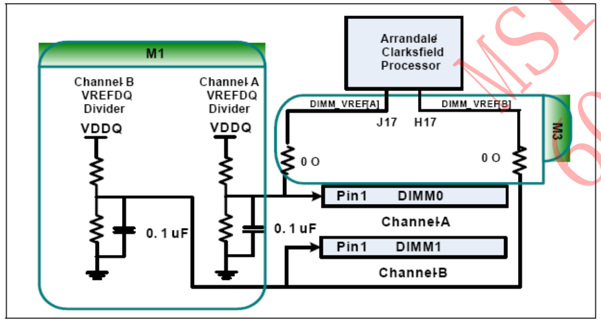
Parameter	Symbol	Max.	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1,200	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	1,360	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	800	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	960	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	960	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	800	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	1,000	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	2,120	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	2,320	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	2,240	mA
Self refresh current; CK and /CKat 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R	IDD7	3,400	mA

2.5.4 DDR3 VREFDQ Design Implementation

Intel is requesting that customers implement two methods (M1 and M3) to generate and control the DDR3 SO-DIMM Reference voltage for Data/Strobe inputs (V_{REFDQ}) on Arrandale- and Clarksfield-based platforms. For Arrandale, M1 should be used. For Clarksfield only designs and common motherboard designs (which support both Arrandale and Clarksfield processors), both M1 and M3 methods should be concurrently implemented.

Note: DDR3 V_{REFDQ} recommendation outlined above in this document, V_{REFCA} and V_{REFDQ} on SO-DIMM cannot be tied together any more for Clarksfield only and Common motherboard designs in order to support M3 and M1/M3 co-existence.

Figure 33. Clarksfield DDR3 SO-DIMM VREF_DQ Design Requirements



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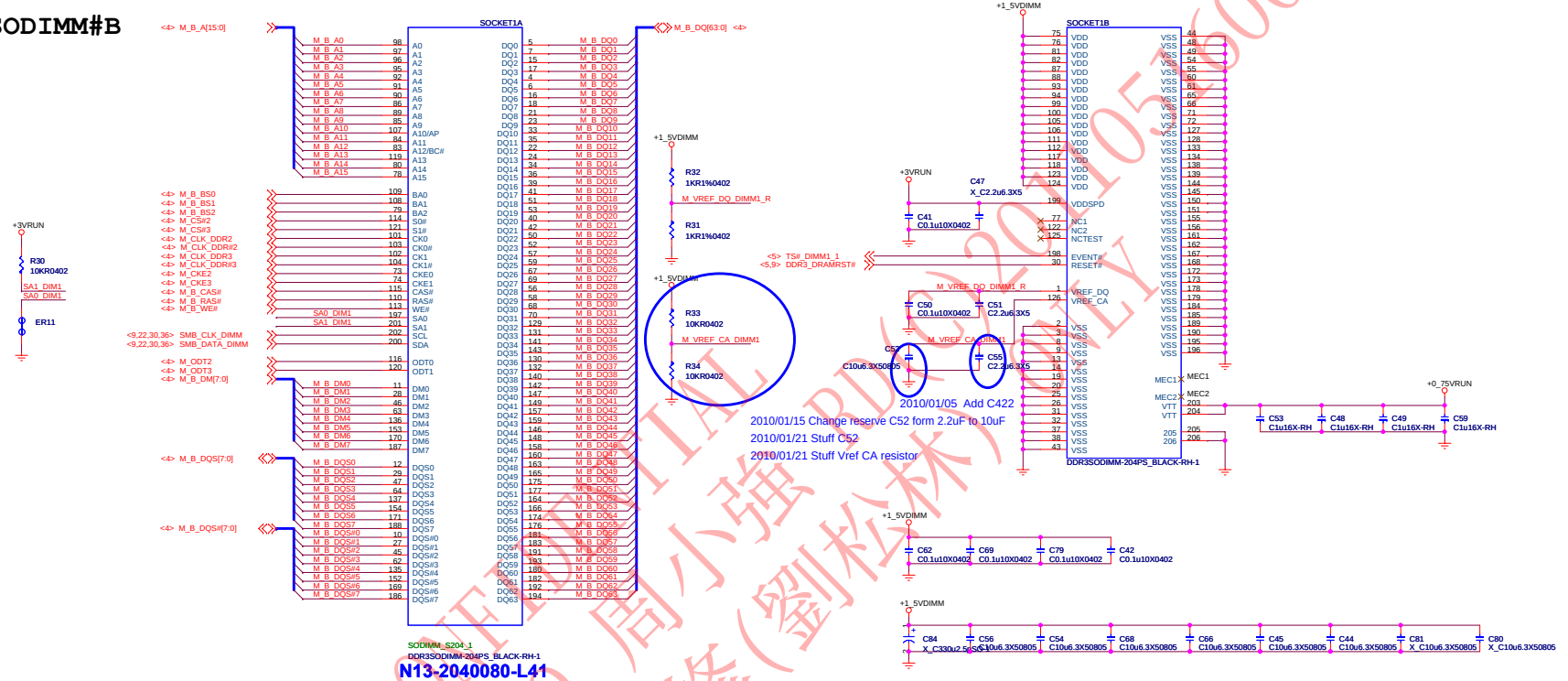
Title: DDR3 SODIMM0			
Size: Custom	Document Number: MS-1481		Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 9 of 56		

SODIMM#B



Title	DDR3 SODIMM1
Size	Custom
Document Number	MS-1481
Rev	1.0
Date:	Thursday, May 13, 2010
Sheet	10 of 56

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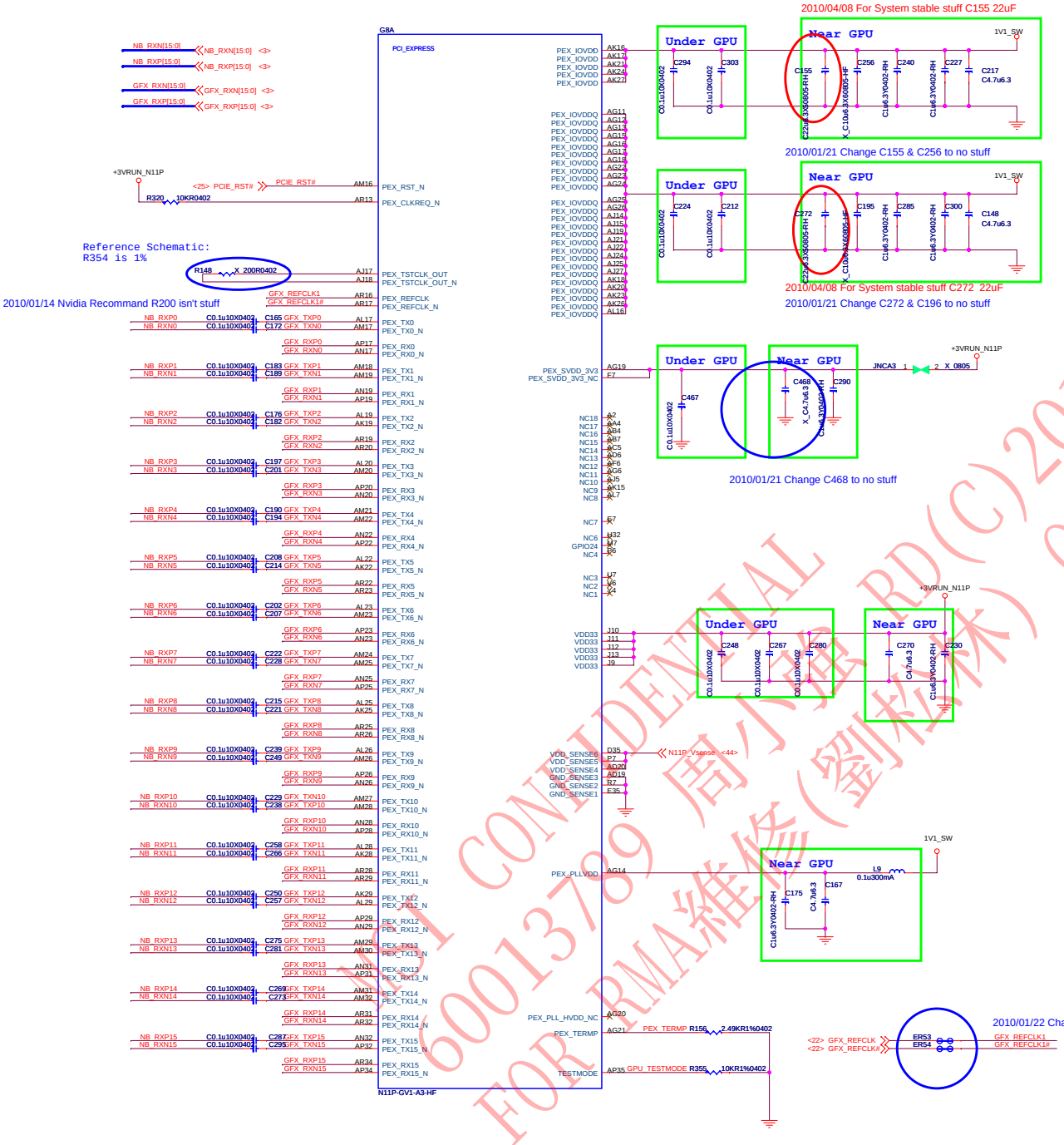

Optimus Software Design for Arrandale Platforms

At POST, the system BIOS should initialize the IGP as the primary graphics adapter. As the OS initializes, both the IGP driver and GPU driver will load. Up to this point the platform is similar to any multiple graphics adapter system-such as a desktop system with more than one graphics card installed. However, the GPU in an Optimus system typically has no physical display outputs. It is purely a graphics rendering and compute device. Then Optimus software will determine when the GPU's capabilities are needed and will enable the GPU as needed, and will host work for individual applications on the GPU as needed.

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_TX	90DIFF	1
PEX_TX	90DIFF	1

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_RX	90DIFF	1
PEX_RX	90DIFF	1

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_CLK_OUT	90DIFF	1
PEX_CLK_OUT	90DIFF	1

SOURCE POWER NETS

	NET	MIN_LINE_WIDTH	MAX_CURRENT	VOLTAGE	NV_SOURCE POWER_NET
3V3	3V3	16.00	4A	3.30000V	TRUE
12V	12V	25.00	8A	18.00000V	TRUE

Features	N11P-GE1	N11P-LP1	N11P-GS1
Host Platform	PCIE 2.0 x 16		
Memory Interface	128-bit DDR3 GDDR3		128-bit DDR3 GDDR3 GDDR5
Process Technology	40nm		
Device ID	0x0A29	0x0A2B	0x0CAF
Package	969-ball BGA 29nm x 29nm package BG1-128		
Display	DVII DVID 1920 x1200 @ 60Hz		DVII DVID 2560 x 1600 @ 60Hz

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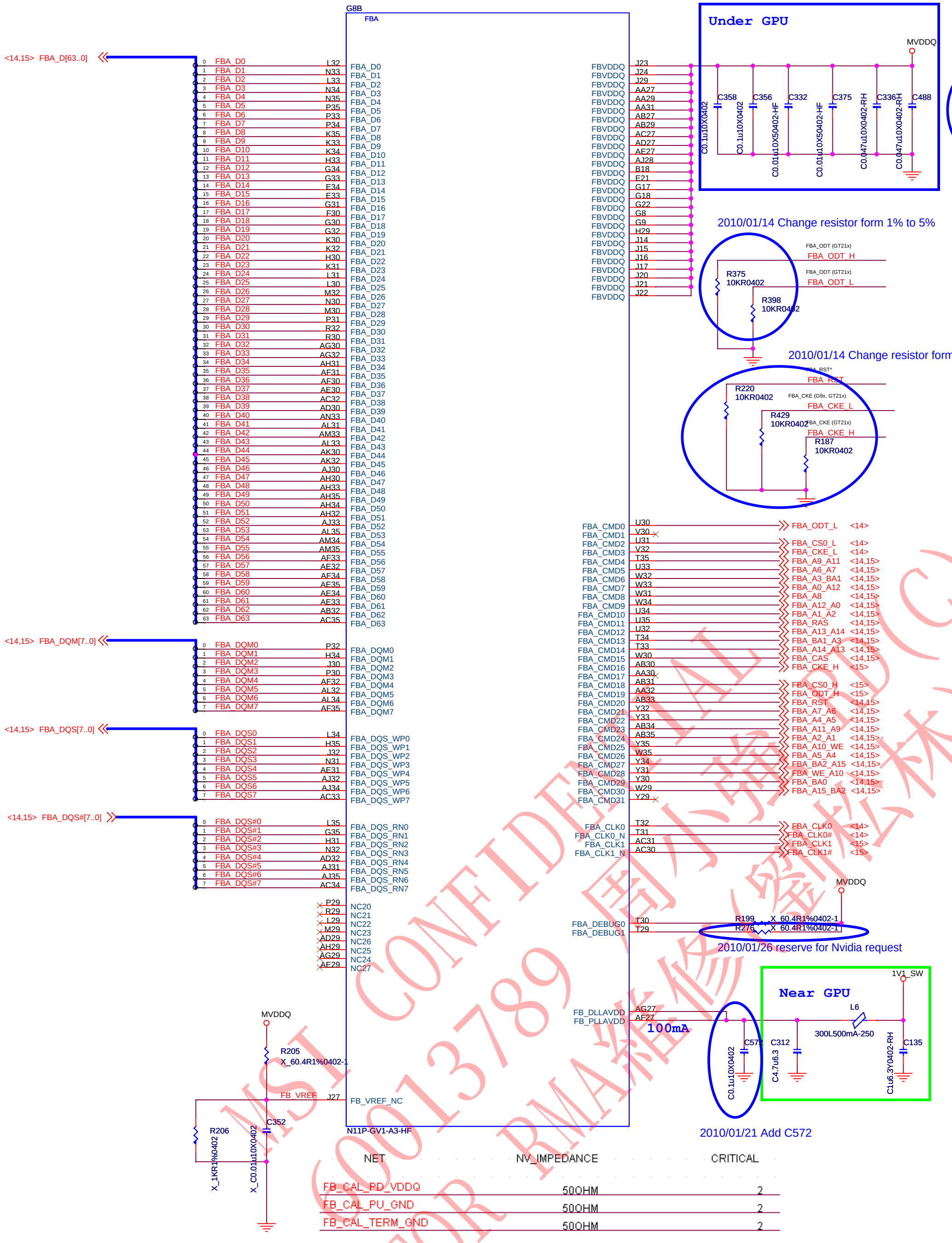
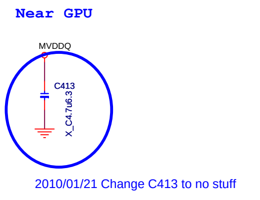
Title: N11P-GV1 PCIE Host

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 11 of 56



G8B
FBA
<14,15> FBA_D[63..0]
<14,15> FBA_DQM[7..0]
<14,15> FBA_DQS[7..0]
<14,15> FBA_DQS#[7..0]
Under GPU
MVDDQ
C358 C356 C332 C375 C336 C488
2010/01/14 Change resistor form 1% to 5%
R375 10KR0402
R398 10KR0402
FBA_ODT_H
FBA_ODT_L
R220 10KR0402
R429 10KR0402
R187 10KR0402
FBA_RST
FBA_CKE_L
FBA_CKE_H
R199 X_60.4R1%0402-1
R276 X_60.4R1%0402-1
2010/01/26 reserve for Nvidia request
Near GPU
1V1_SW
L6 300L500mA-250
C572 C312 C135
100mA
2010/01/21 Add C572
R205 X_60.4R1%0402-1
FB_VREF
R206 X_1KR1%0402
C352 X_C0.01u10X0402
N11P-GV1-A3-HF
NET NV_IMPEDANCE CRITICAL
FB_CAL_PD_VDDQ 50OHM 2
FB_CAL_PU_GND 50OHM 2
FB_CAL_TERM_GND 50OHM 2



GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD0	FBx_CMD3	CKE	
FBx_CMD1	FBx_CMD8	A8	A8
FBx_CMD2	FBx_CMD2	CS0#	
FBx_CMD3	FBx_CMD21	A7	A6
FBx_CMD4	FBx_CMD24	A2	A1
FBx_CMD5	FBx_CMD23	A11	A9
FBx_CMD6	FBx_CMD26	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD8	FBx_CMD15	CAS#	CAS#
FBx_CMD9	FBx_CMD13	BA1	A3
FBx_CMD10	FBx_CMD4	A9	A11
FBx_CMD11	FBx_CMD18		CS0#
FBx_CMD12	FBx_CMD29	BA0	BA0
FBx_CMD13	FBx_CMD27	BA2	A15
FBx_CMD14	FBx_CMD6	A3	BA1
FBx_CMD15	FBx_CMD17		CS1#
FBx_CMD16	FBx_CMD19		ODT
FBx_CMD17	FBx_CMD22	A4	A5
FBx_CMD18	FBx_CMD12	A13	A14
FBx_CMD19	FBx_CMD28	WE#	A10
FBx_CMD20	FBx_CMD10	A1	A2
FBx_CMD21	FBx_CMD25	A10	WE#
FBx_CMD22	FBx_CMD9	A12	A0
FBx_CMD23	FBx_CMD1	CS1#	
FBx_CMD24	FBx_CMD11	RAS#	RAS#
FBx_CMD25	FBx_CMD0	ODT	

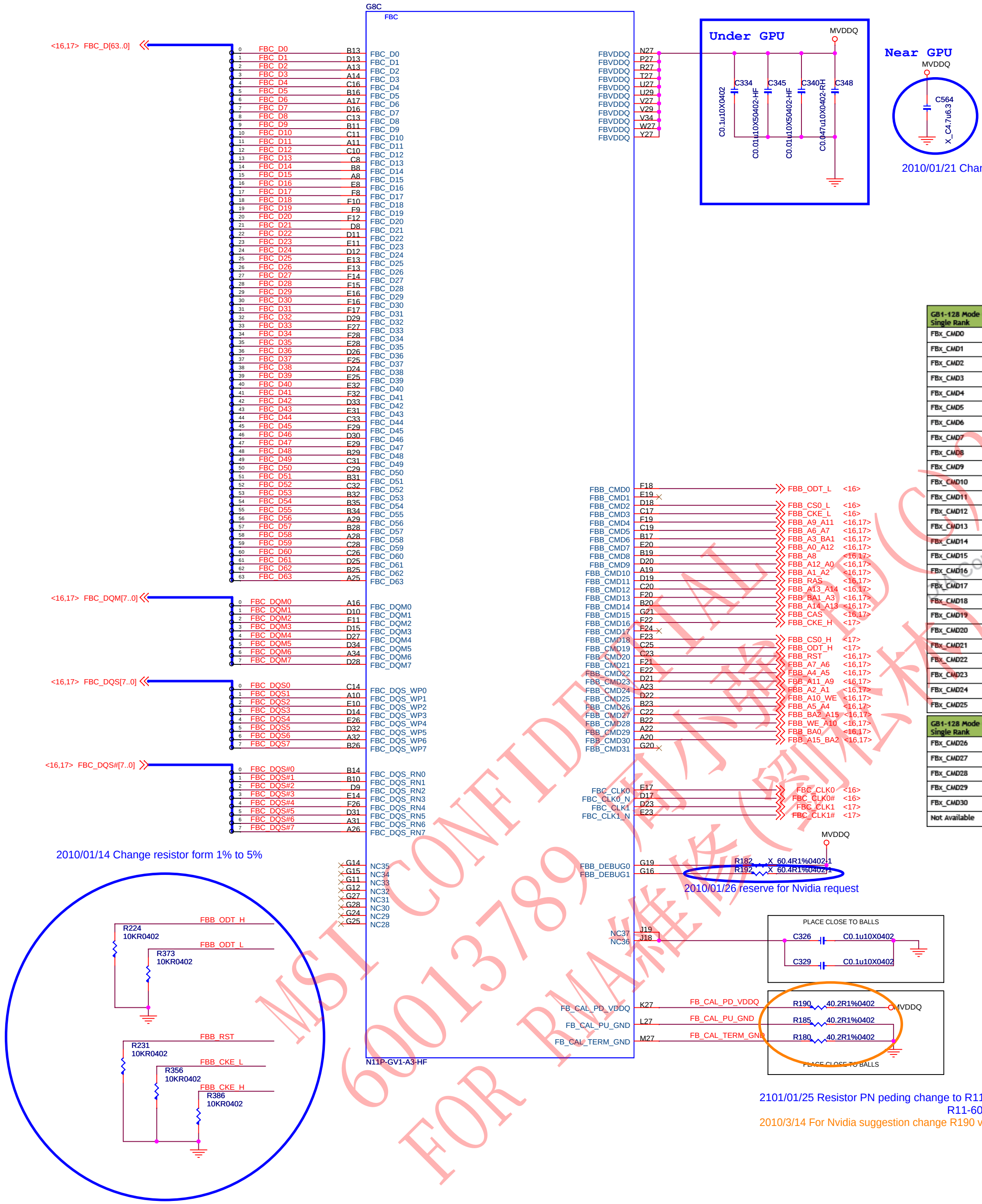
GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD26	FBx_CMD5	A6	A7
FBx_CMD27	FBx_CMD16		CKE
FBx_CMD28	FBx_CMD20	RST	RST
FBx_CMD29	FBx_CMD14	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
Not Available	FBx_CMD31		

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1_MEM Interface A

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 12 of 56



G8C
FBC
FBC_D[63..0]
FBC_DQM[7..0]
FBC_DQS[7..0]
FBC_DQS#[7..0]
FBVDDQ
Under GPU
MVDDQ
C334
C345
C340
C348
Near GPU
C564
2010/01/21 Change C564 to no stuff
FBB_ODT_L
FBB_CS0_L
FBB_CKE_L
FBB_CS0_H
FBB_ODT_H
FBB_RST
FBC_CLK0
FBC_CLK0#
FBC_CLK1
FBC_CLK1#
2010/01/14 Change resistor form 1% to 5%
FBB_ODT_H
FBB_ODT_L
FBB_RST
FBB_CKE_L
FBB_CKE_H
R224 10KR0402
R373 10KR0402
R231 10KR0402
R356 10KR0402
R386 10KR0402
FBB_DEBUG0
FBB_DEBUG1
R182
R192
2010/01/26 reserve for Nvidia request
PLACE CLOSE TO BALLS
C326 C0.1u10X0402
C329 C0.1u10X0402
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R190 40.2R1%0402
R185 40.2R1%0402
R180 40.2R1%0402
N11P-GV1-A3-HF
2101/01/25 Resistor PN peding change to R11-402AT12-W08
R11-604AT12-W08
2010/3/14 For Nvidia suggestion change R190 value form 60R to 40R

GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD0	FBx_CMD3	CKE	
FBx_CMD1	FBx_CMD8	A8	A8
FBx_CMD2	FBx_CMD2	CS0#	
FBx_CMD3	FBx_CMD21	A7	A6
FBx_CMD4	FBx_CMD24	A2	A1
FBx_CMD5	FBx_CMD23	A11	A9
FBx_CMD6	FBx_CMD26	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD8	FBx_CMD15	CAS#	CAS#
FBx_CMD9	FBx_CMD13	BA1	A3
FBx_CMD10	FBx_CMD4	A9	A11
FBx_CMD11	FBx_CMD18		CS0#
FBx_CMD12	FBx_CMD29	BA0	BA0
FBx_CMD13	FBx_CMD27	BA2	A15
FBx_CMD14	FBx_CMD6	A3	BA1
FBx_CMD15	FBx_CMD17		CS1#
FBx_CMD16	FBx_CMD19		ODT
FBx_CMD17	FBx_CMD22	A4	A5
FBx_CMD18	FBx_CMD12	A13	A14
FBx_CMD19	FBx_CMD28	WE#	A10
FBx_CMD20	FBx_CMD10	A1	A2
FBx_CMD21	FBx_CMD25	A10	WE#
FBx_CMD22	FBx_CMD9	A12	A0
FBx_CMD23	FBx_CMD1	CS1#	
FBx_CMD24	FBx_CMD11	RAS#	RAS#
FBx_CMD25	FBx_CMD0	ODT	

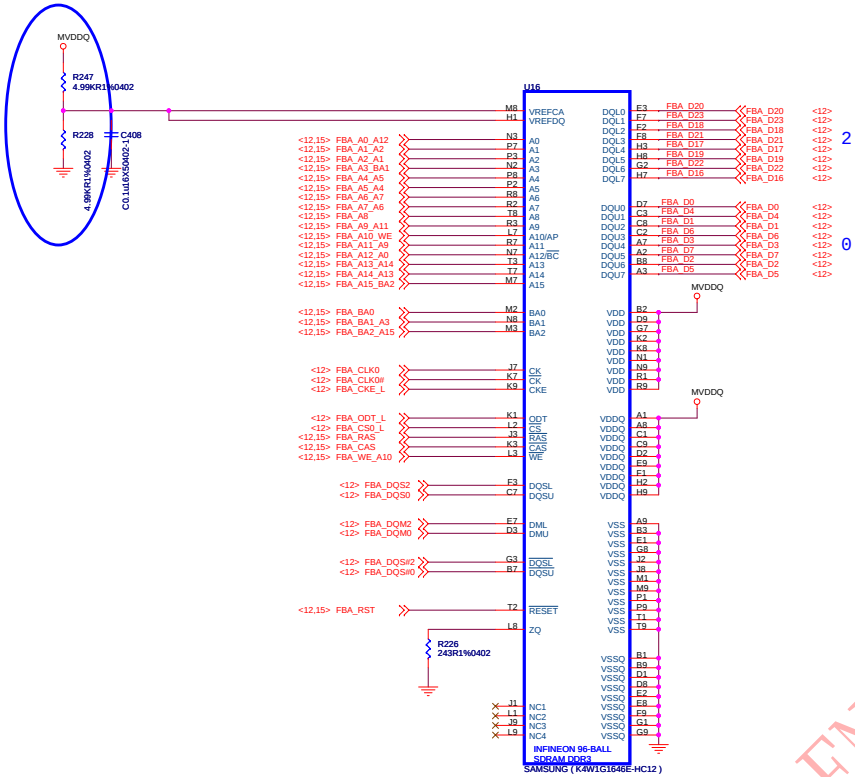
GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD26	FBx_CMD5	A6	A7
FBx_CMD27	FBx_CMD16		CKE
FBx_CMD28	FBx_CMD20	RST	RST
FBx_CMD29	FBx_CMD14	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
Not Available	FBx_CMD31		

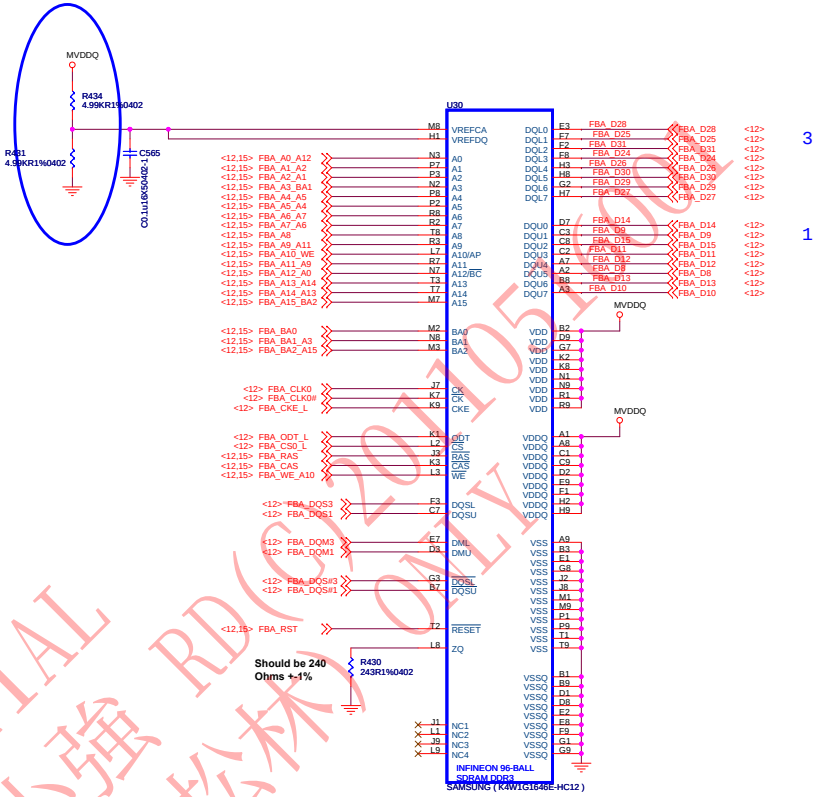
NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2

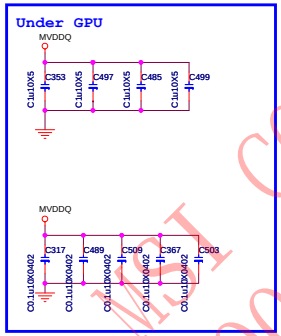
NV Check those value is correct

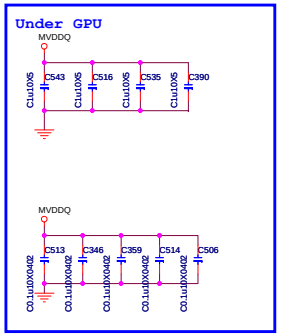
MICRO-STAR INT'L CO.,LTD.

Title	N11P-GV1_MEM Interface C	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 13 of 56	









11.0 1Gb gDDR3 SDRAM E-die IDD Spec Table

[Table 44] IDD Specification for 1Gb gDDR3 E-die

Symbol	64Mx16 (K4W1G1646E)					Unit
	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	
	7-7-7	9-9-9	11-11-11	12-12-12	13-13-13	
IDD0	65	70	80	TBD	TBD	mA
IDD1	85	90	105	TBD	TBD	mA
IDD2P-F	25	25	25	TBD	TBD	mA
IDD2P-S	10	10	10	TBD	TBD	mA
IDD2N	30	35	35	TBD	TBD	mA
IDD2Q	30	35	35	TBD	TBD	mA
IDD3P-F	25	27	30	TBD	TBD	mA
IDD3N	45	50	55	TBD	TBD	mA
IDD4R	130	160	200	TBD	TBD	mA
IDD4W	130	155	195	TBD	TBD	mA
IDD5	150	160	160	TBD	TBD	mA
IDD6	10	10	10	TBD	TBD	mA
IDD7	200	240	290	TBD	TBD	mA

NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V

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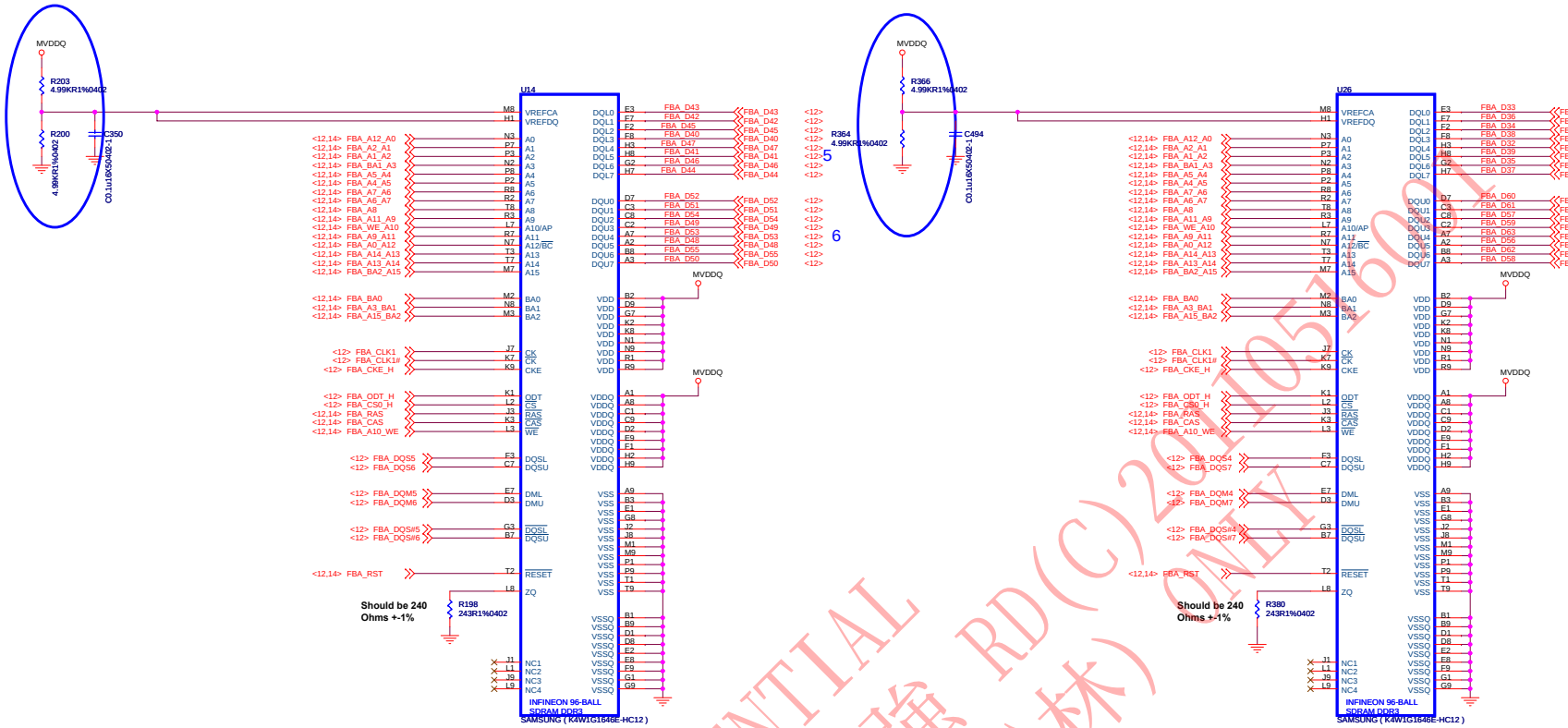
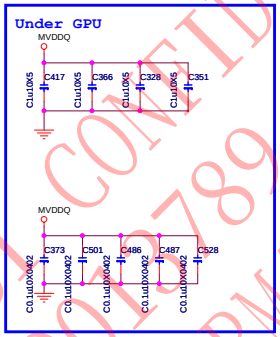
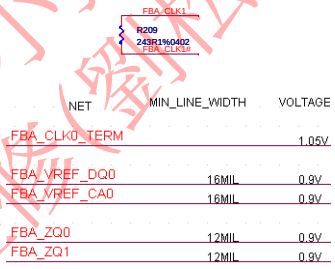
Title: N11P-GV1_FrameA DDR3 I

Size: Custom | Document Number: MS-1481 | Rev: 1.0

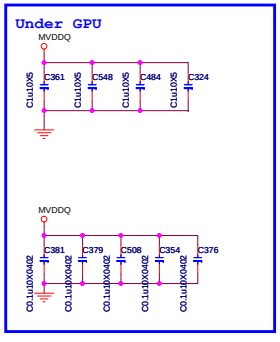
Date: Thursday, May 13, 2010 | Sheet 14 of 56







NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V



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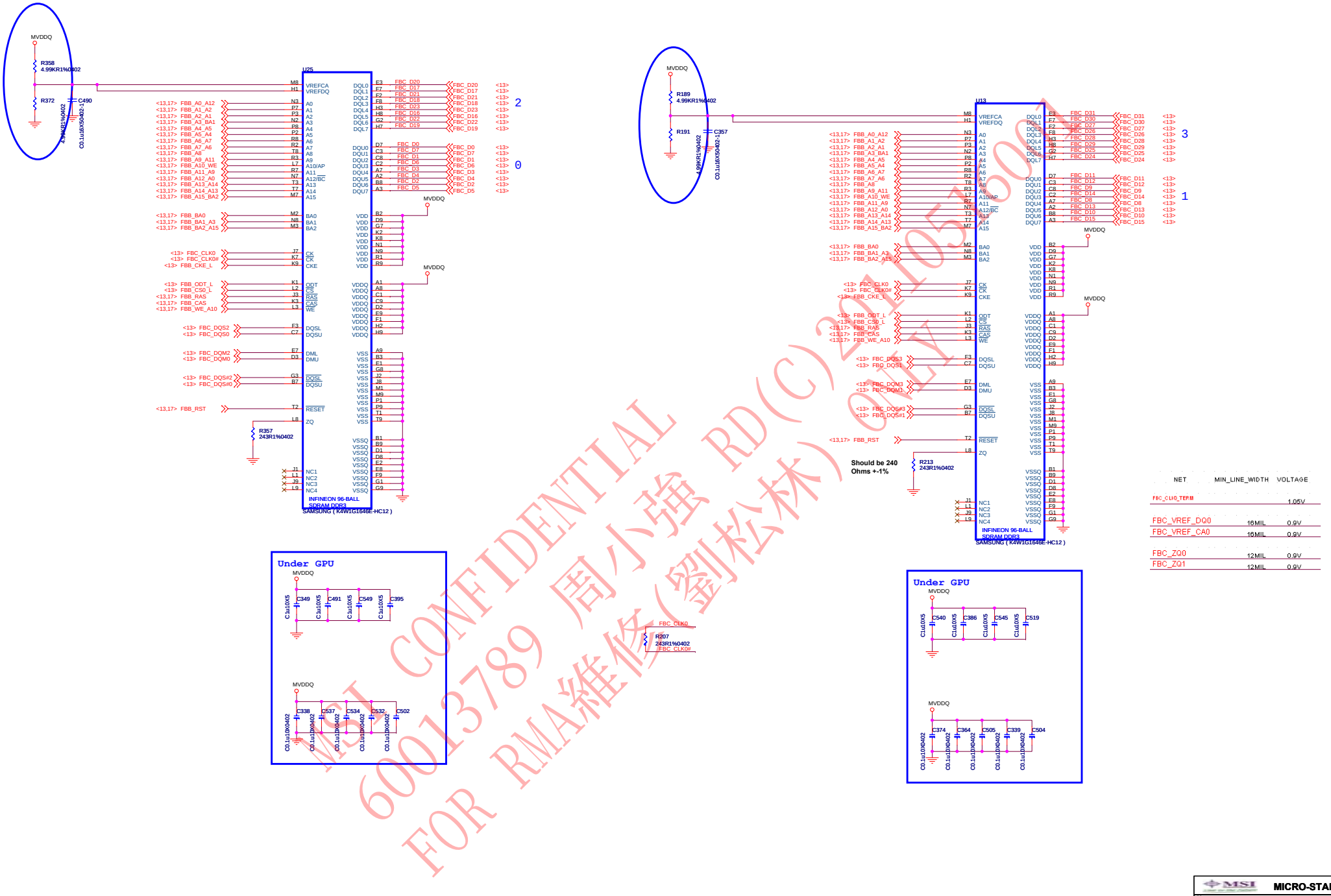
Title: N11P-GV1_FrameA DDR3 II

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 15 of 56



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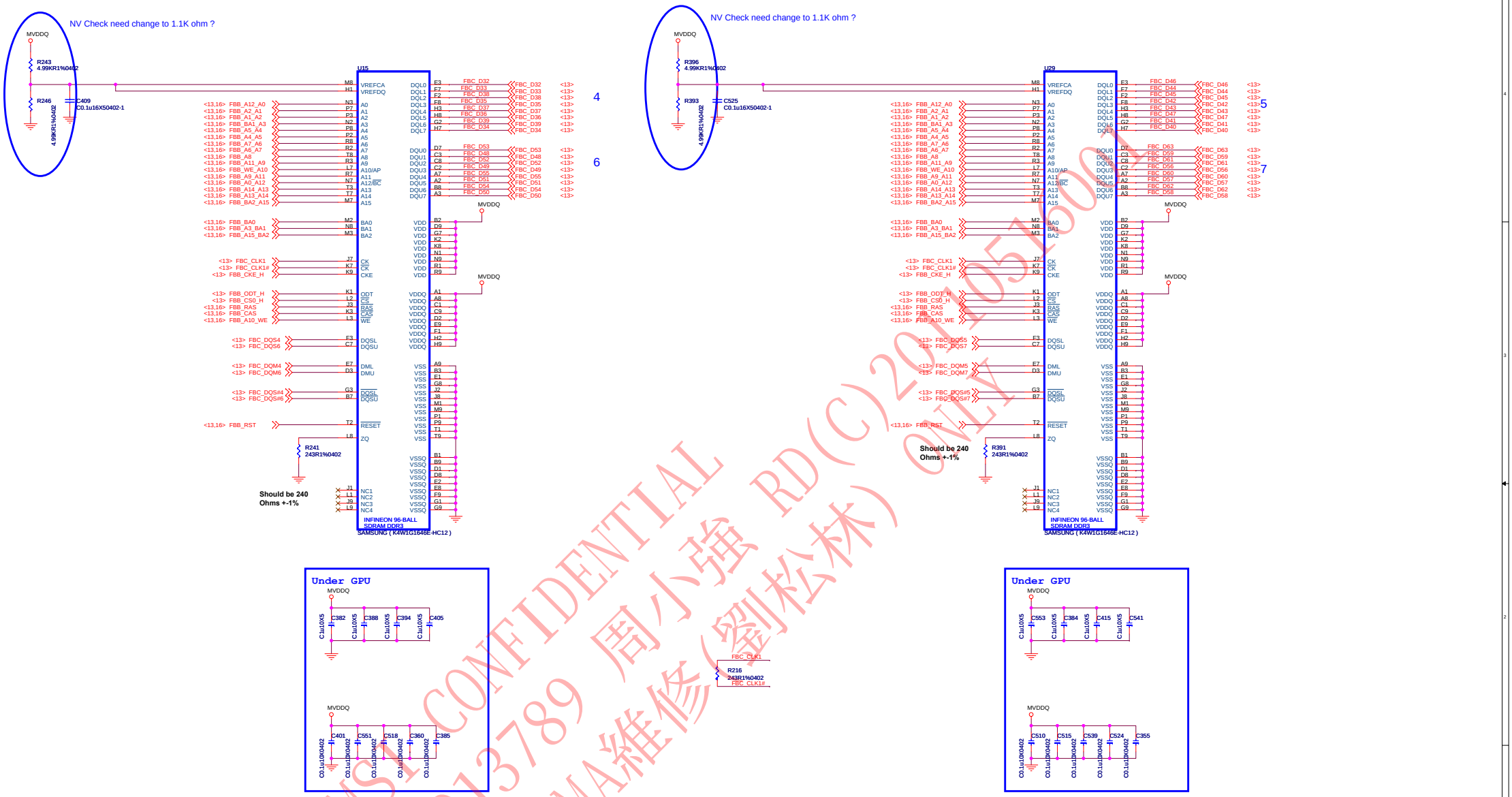
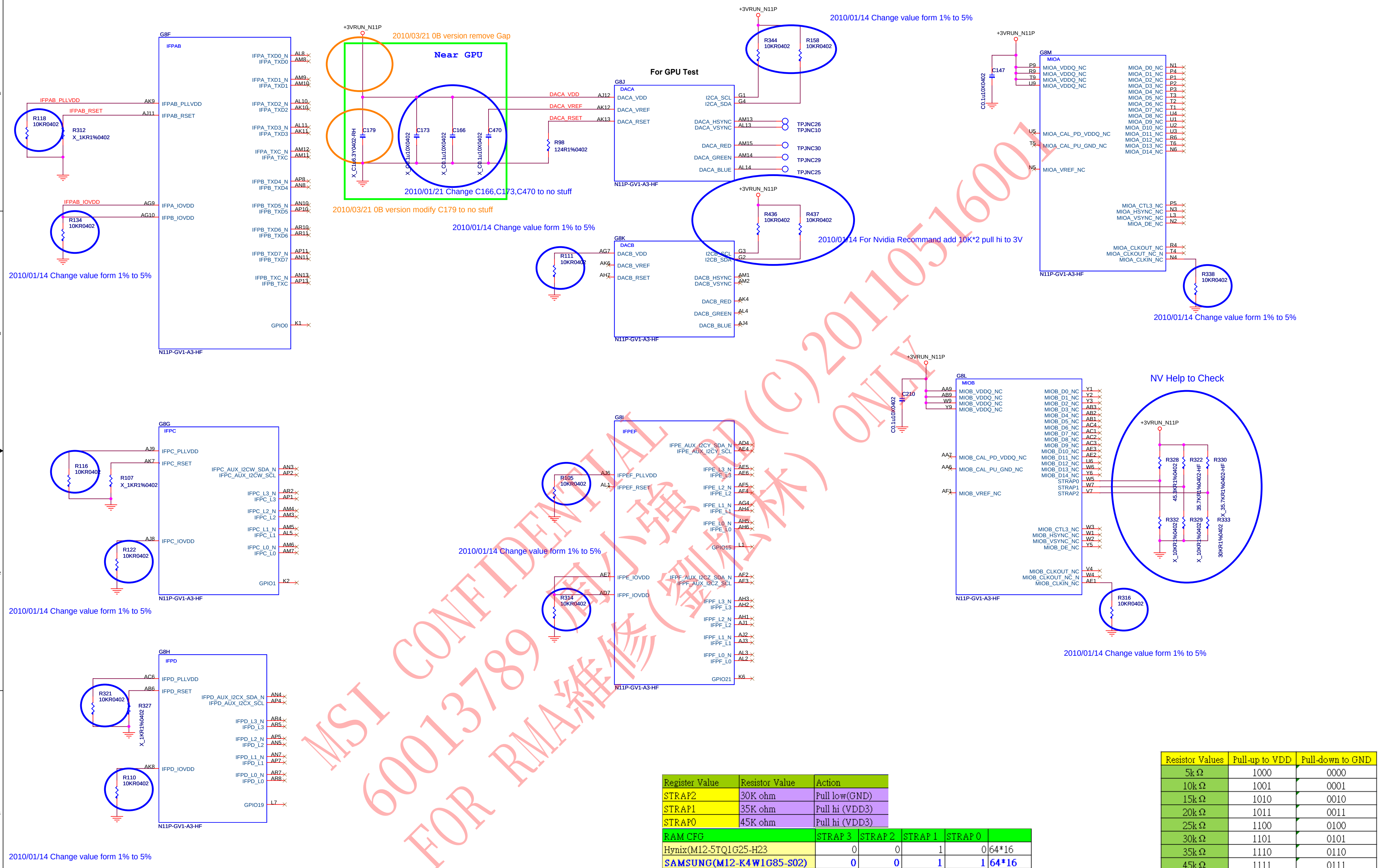
Title: N11P-GV1_FrameB DDR3 I

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 16 of 56



MSI	MICRO-STAR INT'L CO.,LTD.
Title	N11P-GV1_FrameB DDR3 II
Size: Custom	Document Number: MS-1481
Rev	1.0
Date: Thursday, May 13, 2010	Sheet 17 of 56



Register Value	Resistor Value	Action
STRAP2	30K ohm	Pull low(GND)
STRAP1	35K ohm	Pull hi (VDD3)
STRAP0	45K ohm	Pull hi (VDD3)

RAM CFG	STRAP 3	STRAP 2	STRAP 1	STRAP 0	
Hynix(M12-5TQ1G25-H23	0	0	1	0	64*16
SAMSUNG(M12-K4W1G85-S02)	**0**	**0**	**1**	**1**	**64*16**

Resistor Values	Pull-up to VDD	Pull-down to GND
5k Ω	1000	0000
10k Ω	1001	0001
15k Ω	1010	0010
20k Ω	1011	0011
25k Ω	1100	0100
30k Ω	1101	0101
35k Ω	1110	0110
45k Ω	1111	0111

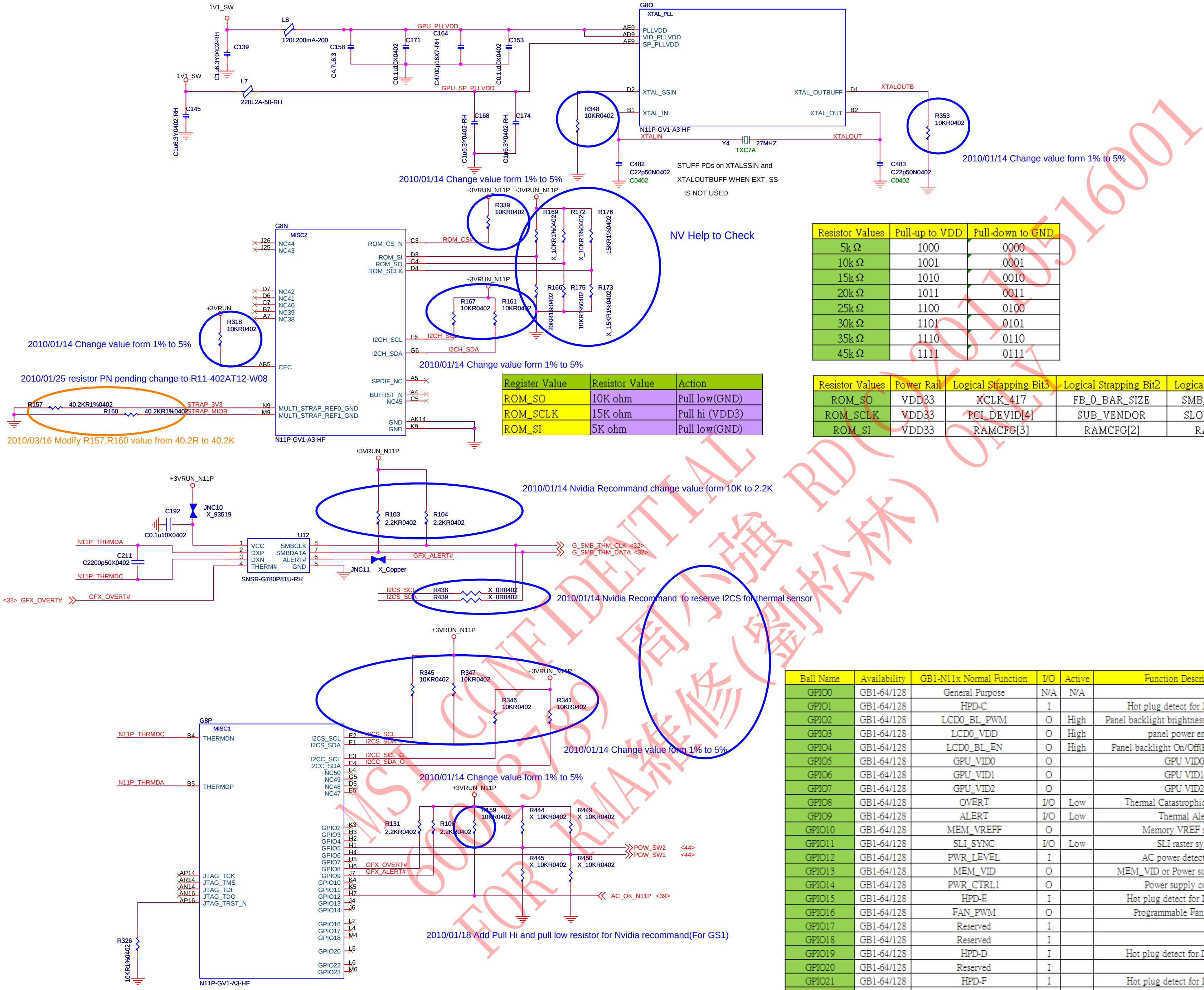
Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1_Display Interface

Size: Custom | Document Number: MS-1481 | Rev 1.0

Date: Thursday, May 13, 2010 | Sheet 18 of 56



Resistor Values	Pull-up to VDD	Pull-down to GND
5k Ω	1000	0000
10k Ω	1001	0001
15k Ω	1010	0010
20k Ω	1011	0011
25k Ω	1100	0100
30k Ω	1101	0101
35k Ω	1110	0110
45k Ω	1111	0111

Register Value	Resistor Value	Action
ROM_SO	10K ohm	Pull low(GND)
ROM_SCLK	15K ohm	Pull hi (VDD3)
ROM_SI	5K ohm	Pull low(GND)

Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]

Ball Name	Availability	GB1-N11x Normal Function	I/O	Active	Function Description
GPIO0	GB1-64/128	General Purpose	N/A	N/A	
GPIO1	GB1-64/128	HPD-C	I		Hot plug detect for IFP link C
GPIO2	GB1-64/128	LCD0_BL_PWM	O	High	Panel backlight brightness(PWM capable)
GPIO3	GB1-64/128	LCD0_VDD	O	High	panel power enable
GPIO4	GB1-64/128	LCD0_BL_EN	O	High	Panel backlight On/Off(PWM capable)
GPIO5	GB1-64/128	GPU_VID0	O		GPU VID0
GPIO6	GB1-64/128	GPU_VID1	O		GPU VID1
GPIO7	GB1-64/128	GPU_VID2	O		GPU VID2
GPIO8	GB1-64/128	OVERT	I/O	Low	Thermal Catastrophic Overtemp
GPIO9	GB1-64/128	ALERT	I/O	Low	Thermal Alert
GPIO10	GB1-64/128	MEM_VREFF	O		Memory VREF switch
GPIO11	GB1-64/128	SLI_SYNC	I/O	Low	SLI raster sync
GPIO12	GB1-64/128	PWR_LEVEL	I		AC power detect input
GPIO13	GB1-64/128	MEM_VID	O		MEM_VID or Power supply control
GPIO14	GB1-64/128	PWR_CTRL1	O		Power supply control
GPIO15	GB1-64/128	HPD-E	I		Hot plug detect for IFP Link E
GPIO16	GB1-64/128	FAN_PWM	O		Programmable Fan Control
GPIO17	GB1-64/128	Reserved	I		
GPIO18	GB1-64/128	Reserved	I		
GPIO19	GB1-64/128	HPD-D	I		Hot plug detect for IFP Link D
GPIO20	GB1-64/128	Reserved	I		
GPIO21	GB1-64/128	HPD-F	I		Hot plug detect for IFP Link F
GPIO22	GB1-64/128	SWAPRDY	I		SLI swap ready signal
GPIO23	GB1-64/128	STEREO	I/O		

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1_Thermal, GPIOs

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 |

DA-04661-001_v04
DA-04882-001

Products	GPU (W)	Mem (W)	NVCLK/MCLK (MHz)
N11P-GE1 1024MB DDR3	22.98	5.07	575/790
N11P-LP1 1024MB DDR3	14.81	4.78	475/700
N11P-GS1 1024MB DDR3	22.85	4.97	450/790

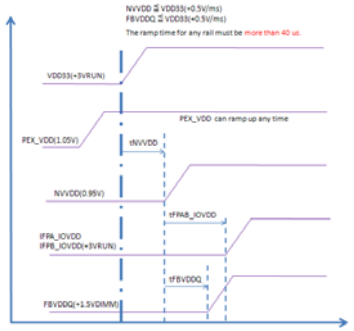
Products	NVVDD		
N11P-GE1 1024MB DDR3	0.95V	21.4A	20.33W
N11P-LP1 1024MB DDR3	0.85V	14.37A	12.22W
N11P-GS1 1024MB DDR3	0.9V	22.19A	19.97W

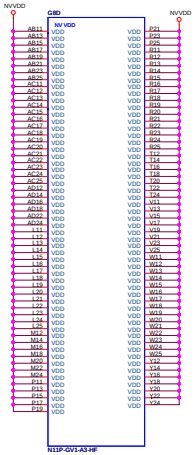
Products	FBVDD 1.5V		FBVDDQ GPU+Mem 1.5V	
N11P-GE1 1024MB DDR3	1.84A	2.76W	2.56A	3.84W
N11P-LP1 1024MB DDR3	1.69A	2.54W	2.48A	3.73W
N11P-GS1 1024MB DDR3	1.52A	2.28W	2.98A	4.48W

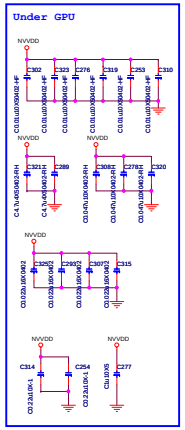
Products	PCI Expeess 1.05V		I/O PLLVDD 1.05V	
N11P-GE1 1024MB DDR3	599.27mA	0.63W	186.77mA	0.2W
N11P-LP1 1024MB DDR3	581.74mA	0.61W	186.77mA	0.2W
N11P-GS1 1024MB DDR3	578mA	0.61W	186mA	0.2W

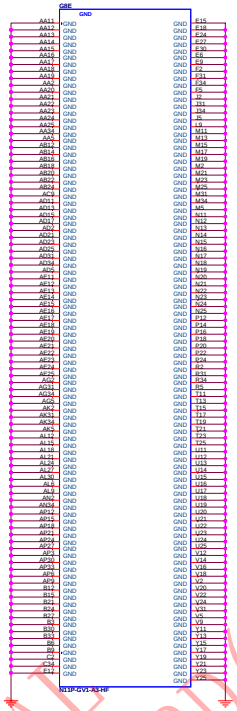
Products	I/O PLLVDD 1.8V	
N11P-GE1 1024MB DDR3	88.5mA	0.16W
N11P-LP1 1024MB DDR3	88.5mA	0.16W
N11P-GS1 1024MB DDR3	87mA	0.16W

Products	Other 3.3V	
N11P-GE1 1024MB DDR3	39.97mA	0.13W
N11P-LP1 1024MB DDR3	39.97mA	0.13W
N11P-GS1 1024MB DDR3	39mA	0.13W



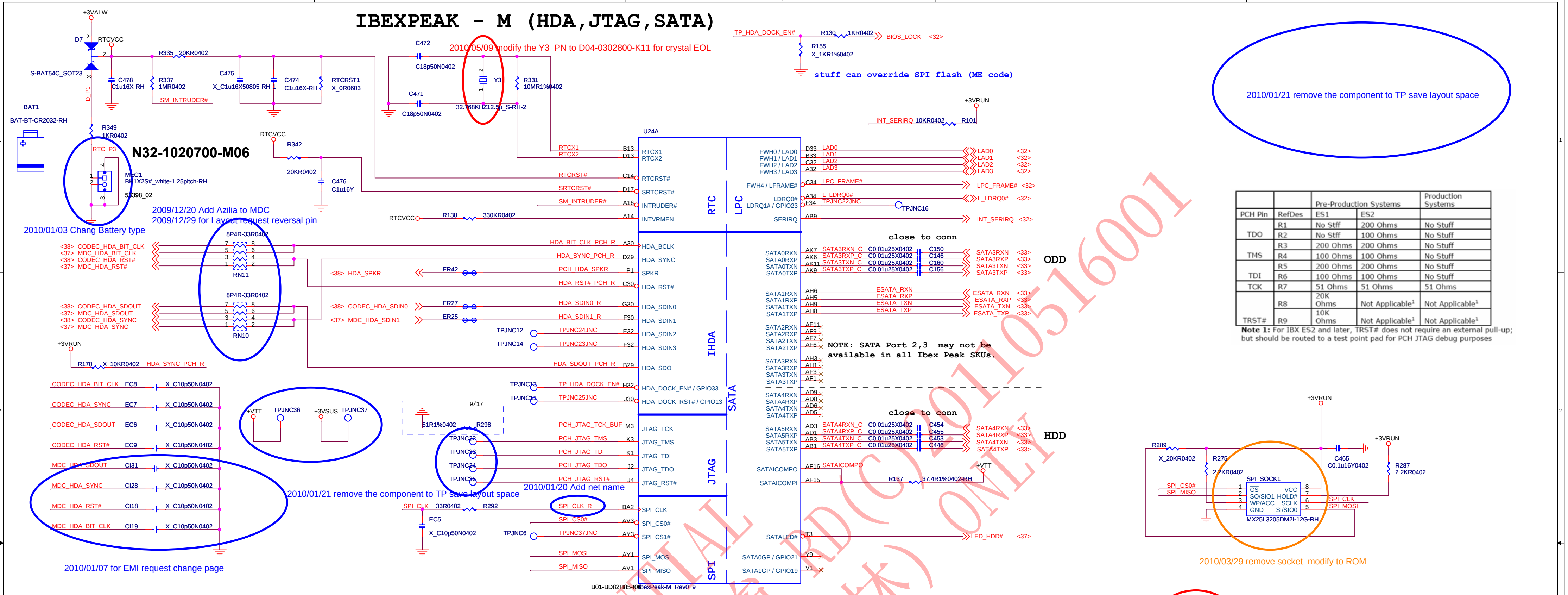






MICRO-STAR INT'L CO.,LTD.
Title: N11P-GV1 Power & GND
Size: D | Document Number: MS-1481 | Rev: 1.0
Date: Thursday, May 13, 2010 | Sheet 20 of 56

IBEXPEAK - M (HDA,JTAG,SATA)



PCH Pin	RefDes	Pre-Production Systems ES1	ES2	Production Systems
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor
Disable iTPM: Left floating, no pull-down required.

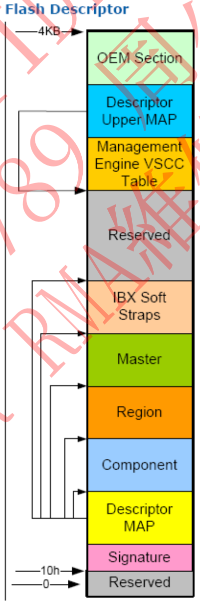
Boot Flow for Ibex Peak

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x0. The descriptor fetch is triggered whichever comes first, the assertion of MEPWROK or deassertion of LAN_RST#. If the signature is present and valid, then the PCH controller will boot in Descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the GNT0# and SPI_CS1#1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from Firmware hub or SPI flash.

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Ibex Peak based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.

Flash Descriptor

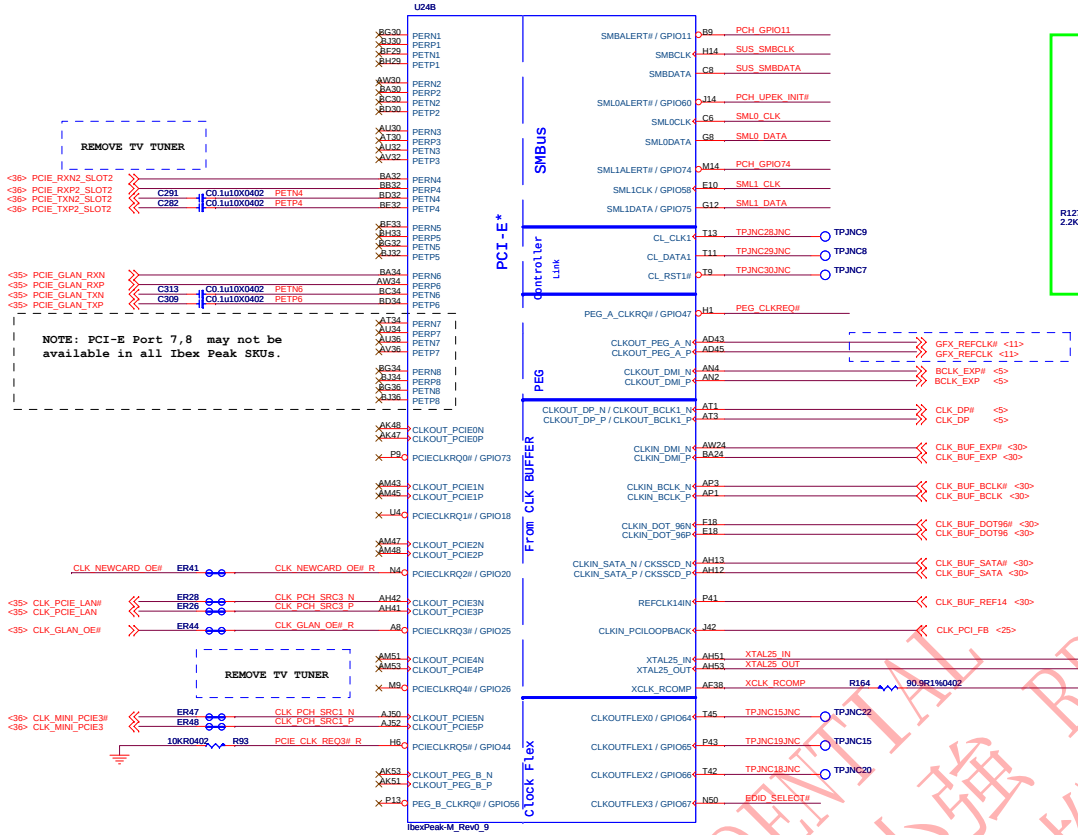


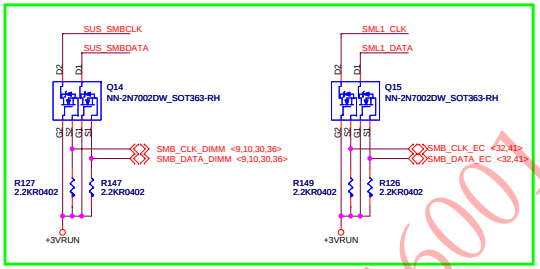
- The Flash signature at the bottom of the flash (offset 0) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. This table is NOT used by Intel® ME Ignition FW only. BIOS and GbE write and erase capabilities depend on LVSCC and UVSCC registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

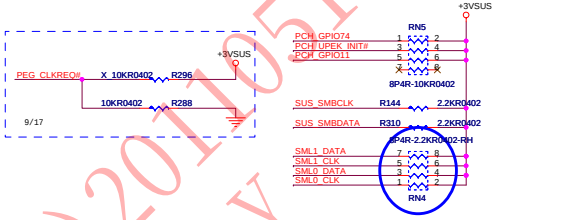
Region Access Control Table

	Master Read/Write Access		
Region	CPU and BIOS	ME	GbE Controller
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Management Engine	Read / Write	ME can always read from and write to ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

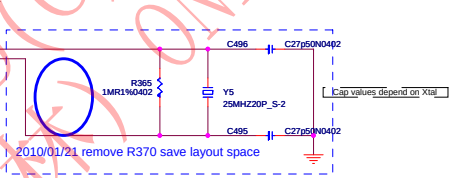
IBEXPEAK - M (PCI-E,SMBUS,CLK)



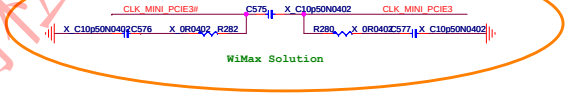




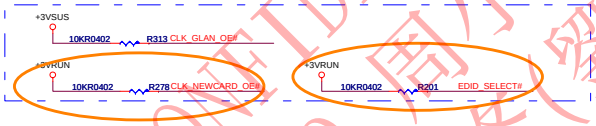
2009/12/29 RN8 reversal for layout request



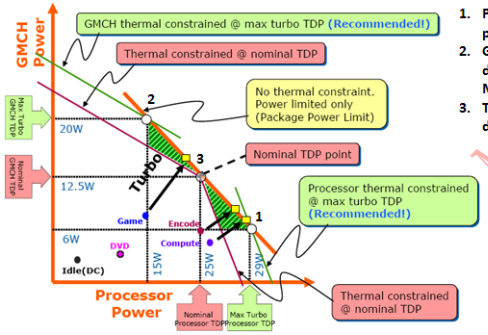
2010/01/21 remove R370 save layout space



2010/03/23 Resever Wimax solution

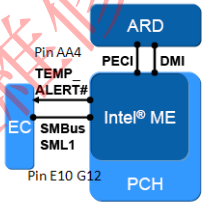


PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well



1. Processor turbo – Most challenging in terms of power density, drives Heat Exchanger design
2. GFX turbo – Doesn't affect Heat Exchanger design, just ensures that Thermal Interface Material is capable
3. TDP (Legacy) – Slightly relaxed Heat Exchanger design

- The system can be maximized turbo benefit by: Thermal design for package turbo limits
- Caution: Designs managing only the nominal TDP point will be under-designed for package turbo!
- Cooling component TDPs ≠Enabling Package Turbo



- Turbo Boost control– EC passes parameters through PCH to host software for real-time Turbo Boost control.
- PCH can be programmed to notify EC when a device is outside of limits via TEMP_ALERT# signal– No SW alert in PCH.

- EC can read from PCH via SMBus:
  - Temperatures
    - CPU, GMCH
  - Sequence number
  - Host status
- EC can write to PCH via SMBus:
  - Disable and enable power sharing
  - CPU and package power clamps
  - Biasing preference
  - Upper and lower temperature limits
    - CPU, MCH
    - TEMP_ALERT# trip points
- PCH can alert EC to out of range temperature conditions
  - TEMP_ALERT# signal assertion
- EC can monitor Intel® ME health by checking "Sequence Number"
  - Increments each time the Intel ME refreshes data

Indicates optional usage with Turbo Boost

Block Read Data Structure

Byte	Data	Format	Units	Range
0	Max Package Temperature	Unsigned byte	1°C/bit	0-255°C
1	PCH Temperature	Unsigned byte	1°C/bit	0-255°C
3:2	CPU Temperature	10.6 Format	1/64°C/bit	0-256°C
4	MCH Temperature	Unsigned byte	1°C/bit	0-255°C
5	DIMM0 Temperature	Unsigned byte	1°C/bit	0-255°C
6	DIMM1 Temperature	Unsigned byte	1°C/bit	0-255°C
7	DIMM2 Temperature	Unsigned byte	1°C/bit	0-255°C
8	DIMM3 Temperature	Unsigned byte	1°C/bit	0-255°C
9	Sequence Number	Unsigned byte	Count	0-255
11:10	CPU Energy Counter	16 int:16frac	0.1253J/bit	
19:14	Host Status	Status register	N/A	N/A

EC-PCH Write Commands

Commands	Format	Units
SMBus Turbo Status (STS)	Register	
CPU Temperature Limits	10.6 Format	1/64°C/bit
MCH Temperature Limits	Unsigned byte	1°C/bit
IBX Temperature Limits	Unsigned byte	1°C/bit
DIMM Temperature Limits	Unsigned byte	1°C/bit
Processor Power Clamp	Unsigned word	0.1W/bit

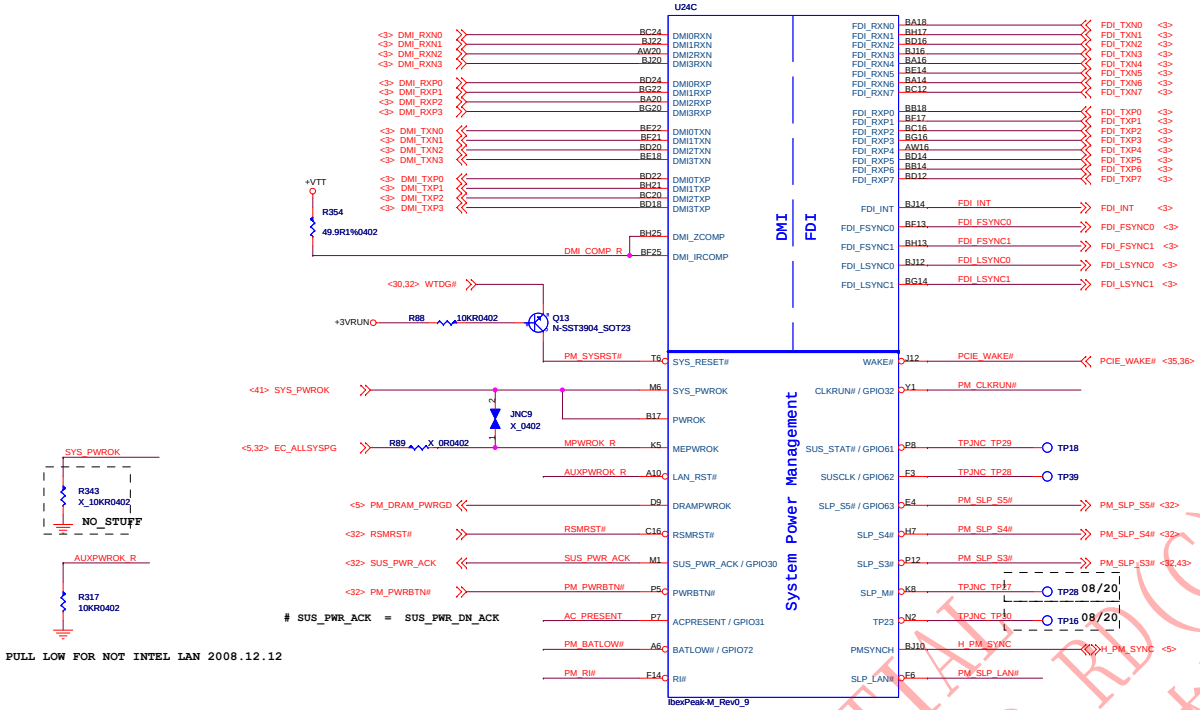
MICRO-STAR INT'L CO.,LTD.

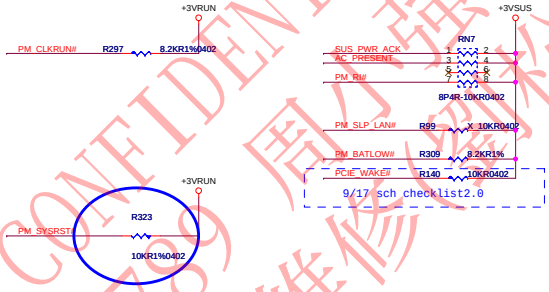
Title: IBEXPEAK - M (PCI-E,SMBUS,CLK)

Size: Custom | Document Number: MS-1481 | Rev: 1.0

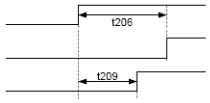
Date: Thursday, May 13, 2010 | Sheet 22 of 56

IBEXPEAK - M (DMI,FDI,GPIO)





Source	Dest	Signal Name
Board	PCH	PWROK
PCH	Processor	DRAMPWRGD
PCH	Processor	PROCPWRGD



Sym	Parameter	Min	Max	Units	Notes
t209	PWROK active to PROCPWRGD active	See Note 7	—	ms	7
t206	PWROK deglitch time	1	—	ms	6

6. Ensure PWROK is a solid logic '1' before proceeding with the boot sequence. Note: If PWROK drops after t206 it will be considered a power failure.
7. t209 minimum timing selectable as 1 ms (recommended), 5 ms, 50 ms, or 100 ms using bits 9:8 of PCHSTRP15.

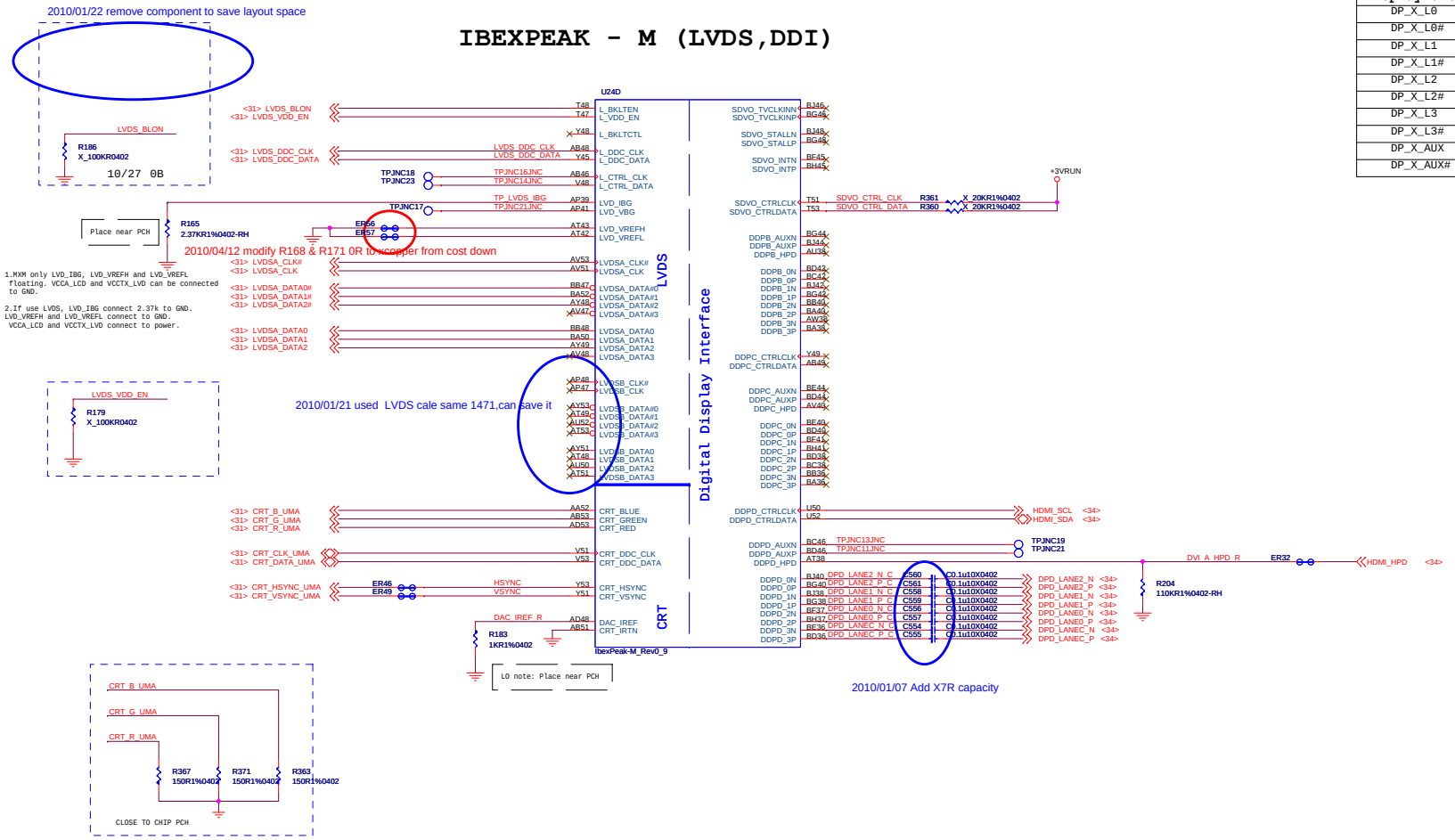
Flexible Display Interface

The Flexible Display Interface (Intel® FDI) is a bus technology that utilizes differential signaling to transport display data from a pixel source Havendale to a sink Ibex Peak. There are two Flexible Display Interface channels- A and B which are independently controlled. Each channel from Havendale include 4 Tx differential pairs comprising the data link, used for transporting pixel and framing data from the display engine. Two single-ended LineSync and FrameSync inputs. Single-ended DISP_INT is used for interrupts from sink (Ibex Peak) to source (Havendale).

MICRO-STAR INT'L CO.,LTD.	
Title	IBEXPEAK - M (DMI,FDI,GPIO)
Size: Custom	Document Number: MS-1481
Rev	1.0
Date: Thursday, May 13, 2010	Sheet 23 of 56

IBEXPEAK - M (LVDS,DDI)

DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA



MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (LVDS,DDI)

Size: Custom | Document Number: MS-1481 | Rev: 1.0

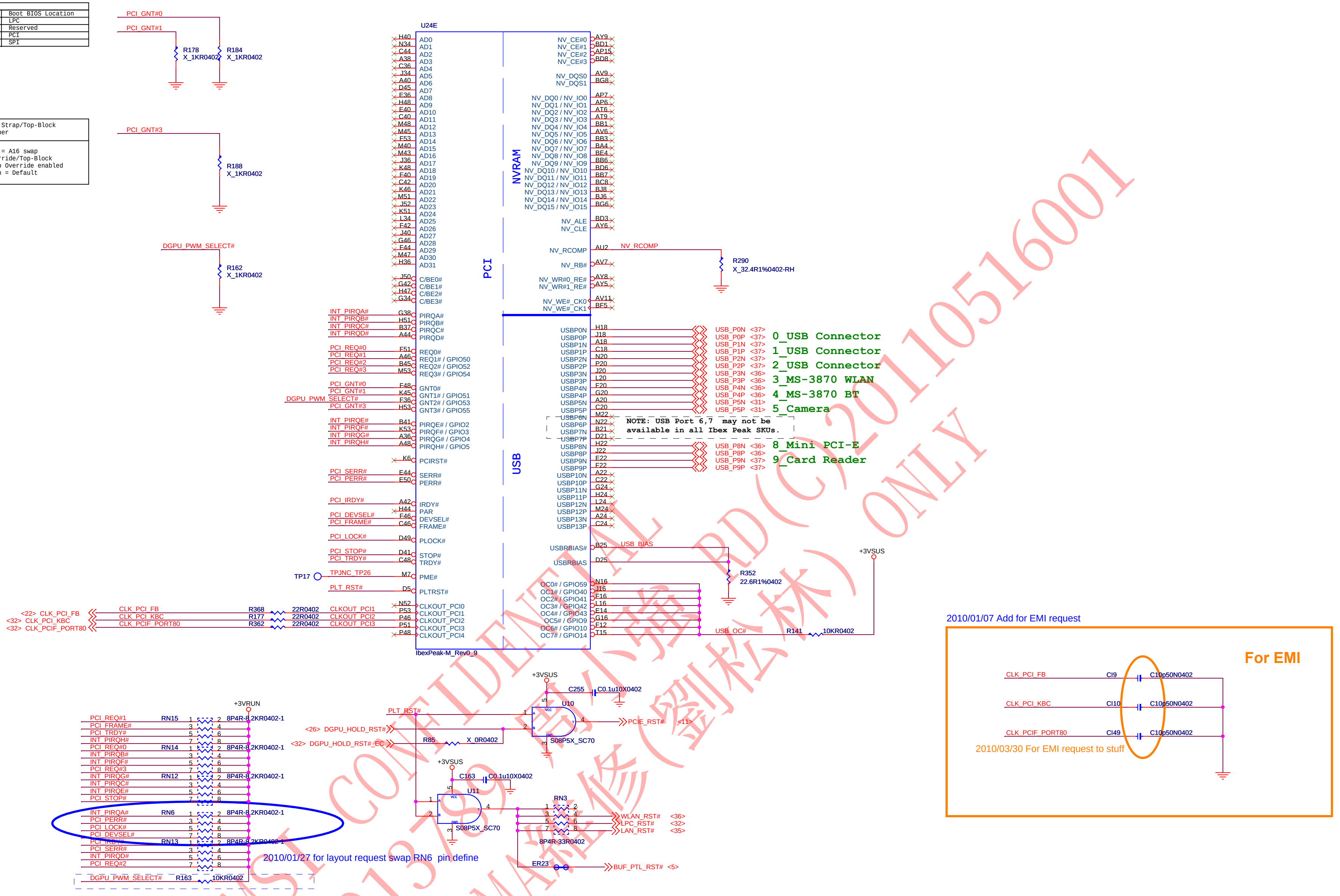
Date: Thursday, May 13, 2010 | Sheet 24 of 56

IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

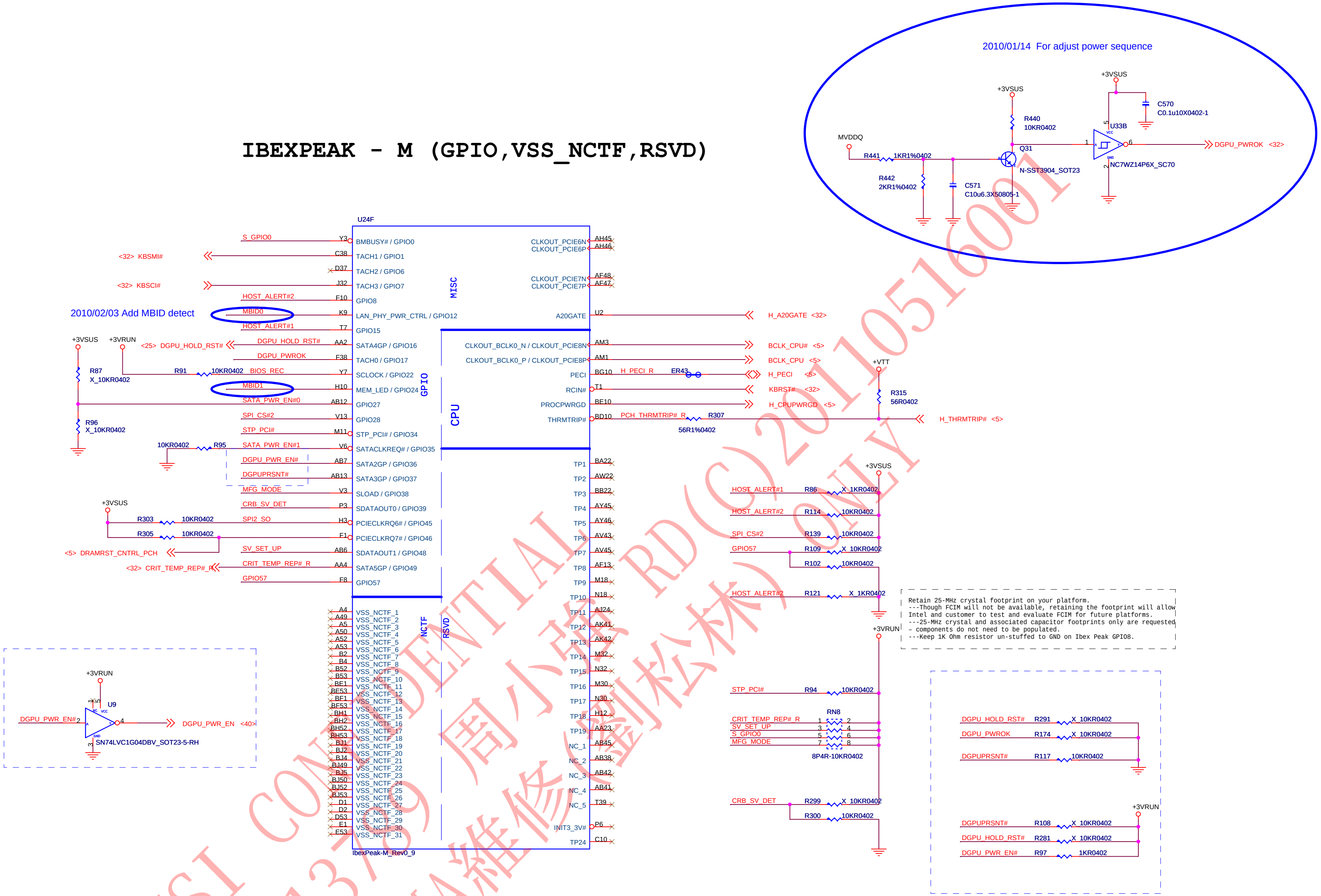
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



U24E
PCI
NVRAM
USB
IbexPeak-M_Rev0_9
PCI_GNT#0
PCI_GNT#1
PCI_GNT#3
DGPU_PWM_SELECT#
R178 X_1KR0402
R184 X_1KR0402
R188 X_1KR0402
R162 X_1KR0402
R290 X_32.4R1%0402-RH
R352 22.6R1%0402
NV_RCOMP
USB_BIAS
+3VSUS
USB_OC#
R141 10KR0402
0_USB Connector
1_USB Connector
2_USB Connector
3_MS-3870 WLAN
4_MS-3870 BT
5_Camera
NOTE: USB Port 6,7 may not be available in all Ibex Peak SKUs.
8_Mini PCI-E
9_Card Reader
TP17
<22> CLK_PCI_FB
<32> CLK_PCI_KBC
<32> CLK_PCIF_PORT80
R368 22R0402
R177 22R0402
R362 22R0402
+3VRUN
RN15 8P4R-8.2KR0402-1
RN14 8P4R-8.2KR0402-1
RN12 8P4R-8.2KR0402-1
RN6 8P4R-8.2KR0402-1
RN13 8P4R-8.2KR0402-1
R163 10KR0402
2010/01/27 for layout request swap RN6 pin define
PLT_RST#
<26> DGPU_HOLD_RST#
<32> DGPU_HOLD_RST#_EC
R85 X_0R0402
C255 C0.1u10X0402
U10 S08P5X_SC70
PCIE_RST# <11>
C163 C0.1u10X0402
U11 S08P5X_SC70
RN3 8P4R-33R0402
WLAN_RST# <36>
LPC_RST# <32>
LAN_RST# <35>
ER23
BUF_PTL_RST# <5>
2010/01/07 Add for EMI request
For EMI
CLK_PCI_FB CI9 C10p50N0402
CLK_PCI_KBC CI10 C10p50N0402
CLK_PCIF_PORT80 CI49 C10p50N0402
2010/03/30 For EMI request to stuff

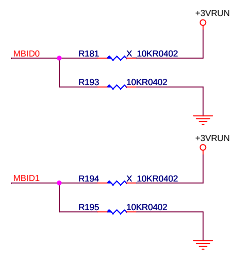
MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (PCI,USB,NVRAM)	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 25 of 56	

IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



2010/01/14 For adjust power sequence
+3VSUS
MVDDQ
R441 1KR1%0402
R442 2KR1%0402
R440 10KR0402
Q31 N-SST3904_SOT23
C571 C10u6.3X50805-1
U33B NC7WZ14P6X_SC70
C570 C0.1u10X0402-1
DGPU_PWROK <32>
U24F
S_GPIO0
<32> KBSMI#
<32> KBSCI#
HOST_ALERT#2
2010/02/03 Add MBID detect
MBID0
HOST_ALERT#1
+3VSUS
+3VRUN
<25> DGPU_HOLD_RST#
DGPU_PWROK
R87 X_10KR0402
R91 10KR0402 BIOS_REC
MBID1
SATA_PWR_EN#0
R96 X_10KR0402
SPI_CS#2
STP_PCI#
10KR0402 R95 SATA_PWR_EN#1
DGPU_PWR_EN#
DGPUPRSNT#
MFG_MODE
CRB_SV_DET
R303 10KR0402 SPI2_SO
R305 10KR0402
<5> DRAMRST_CNTRL_PCH
SV_SET_UP
<32> CRIT_TEMP_REP#_R
CRIT_TEMP_REP#_R
GPIO57
BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
MEM_LED / GPIO24
GPIO27
GPIO28
STP_PCI# / GPIO34
SATACLKREQ# / GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
SDATAOUT1 / GPIO48
SATA5GP / GPIO49
GPIO57
MISC
GPIO
CPU
NCTF
RSVD
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
H_A20GATE <32>
CLKOUT_BCLK0_N / CLKOUT_PCIE8N
CLKOUT_BCLK0_P / CLKOUT_PCIE8P
BCLK_CPU# <5>
BCLK_CPU <5>
PECI
H_PECI_R ER43
H_PECI <5>
RCIN#
KBRST# <32>
PROCPWRGD
H_CPUPWRGD <5>
THRMTRIP#
PCH_THRMTRIP#_R R307 56R1%0402
+VTT
R315 56R0402
H_THRMTRIP# <5>
VSS_NCTF_1 … VSS_NCTF_31
TP1 … TP24
NC_1 NC_2 NC_3 NC_4 NC_5
INIT3_3V#
IbexPeak-M_Rev0_9
+3VSUS
HOST_ALERT#1 R86 X_1KR0402
HOST_ALERT#2 R114 10KR0402
SPI_CS#2 R139 10KR0402
GPIO57 R109 X_10KR0402
R102 10KR0402
HOST_ALERT#2 R121 X_1KR0402
+3VRUN
STP_PCI# R94 10KR0402
RN8
CRIT_TEMP_REP#_R
SV_SET_UP
S_GPIO0
MFG_MODE
8P4R-10KR0402
CRB_SV_DET R299 X_10KR0402
R300 10KR0402
+3VRUN
U9
DGPU_PWR_EN#
DGPU_PWR_EN <40>
SN74LVC1G04DBV_SOT23-5-RH
DGPU_HOLD_RST# R291 X_10KR0402
DGPU_PWROK R174 X_10KR0402
DGPUPRSNT# R117 10KR0402
+3VRUN
DGPUPRSNT# R108 X_10KR0402
DGPU_HOLD_RST# R281 X_10KR0402
DGPU_PWR_EN# R97 1KR0402

Retain 25-MHz crystal footprint on your platform.
---Though FCIM will not be available, retaining the footprint will allow Intel and customer to test and evaluate FCIM for future platforms.
---25-MHz crystal and associated capacitor footprints only are requested - components do not need to be populated.
---Keep 1K Ohm resistor un-stuffed to GND on Ibex Peak GPIO8.



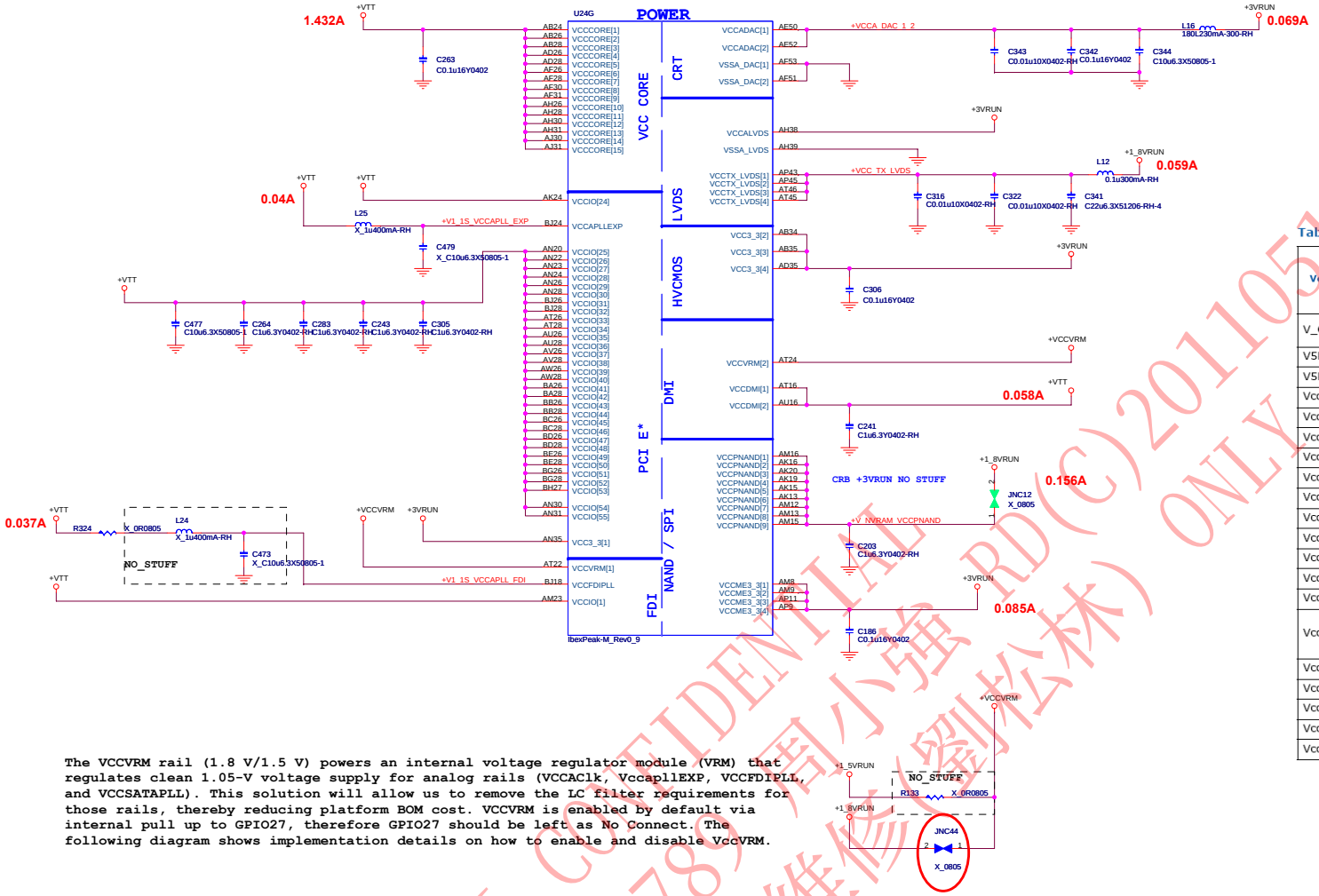
CFG	MBID0(GPIO12)	MBID1(GPIO24)	Remark
None OC	0	0	Default
TDB	0	1	
TDB	1	0	
OC	1	1	

MBID0 & MBID1 are for OC and none OC detect

2010/02/03 Add MBID detect

MICRO-STAR INT'L CO.,LTD.
Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)
Size: Custom | Document Number: MS-1481 | Rev: 1.0
Date: Thursday, May 13, 2010 | Sheet 26 of 56

IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

Mobile Thermal Design Power

SKU	Thermal Design Power (TDP)	Notes
QM57	3.5 W	1
HM57	3.5 W	1
HM55	3.5 W	1
PM55	3.5 W	1
QS57	3.4 W	1

Table 8-4. Measured I_{CC} (Mobile Only)

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
V_CPU_IO	1.1/ 1.05	.001	.001	.001	.001			—
V5REF	5	.001	.001	.001	.001			—
V5REF_Sus	5	.001	.001	.001	.001	.001		—
Vcc3_3	3.3	.305	.305	.0176	.0176			—
VccADAC	3.3	.075	.0011	.0011	.0011			—
VccADPLLA	1.05	.088	.0176	.825	.0044			—
VccADPLLB	1.05	.088	.0176	.0044	.0044			—
VccCore	1.05	1.43	1.254	.3685	.2805			—
VccDMI	1.1	.055	.055	.0011	.0011			—
VccIO	1.05	3.23	2.628	.463	.285			—
VccLAN	1.05	.220	.220	.066	.066	.132		—
VccME	1.05	1.2	1.2	.186	.186	.98	.0044	—
VccME3_3	3.3	.031	.031	.0022	.0022	.0154	.0022	—
VccpNAND	1.8	.0055	.0055	.0022	.0022			—
VccRTC	3.3	.0011	.0011	.0011	.0011	.0011	.0011	6 uA See notes 1, 2
VccSus3_3	3.3	.087	.087	.0132	.0132	.133	.0297	—
VccSusHDA	3.3	.0088	.0088	.001	.001	.001	.001	—
VccVRM	1.8/1.5	.156	.114	.113	.045			—
VccALVDS	3.3	.0011	.0011	.0011	.0011			
VccTX_LVDS	1.8	.066	.0011	.0198	.0011			

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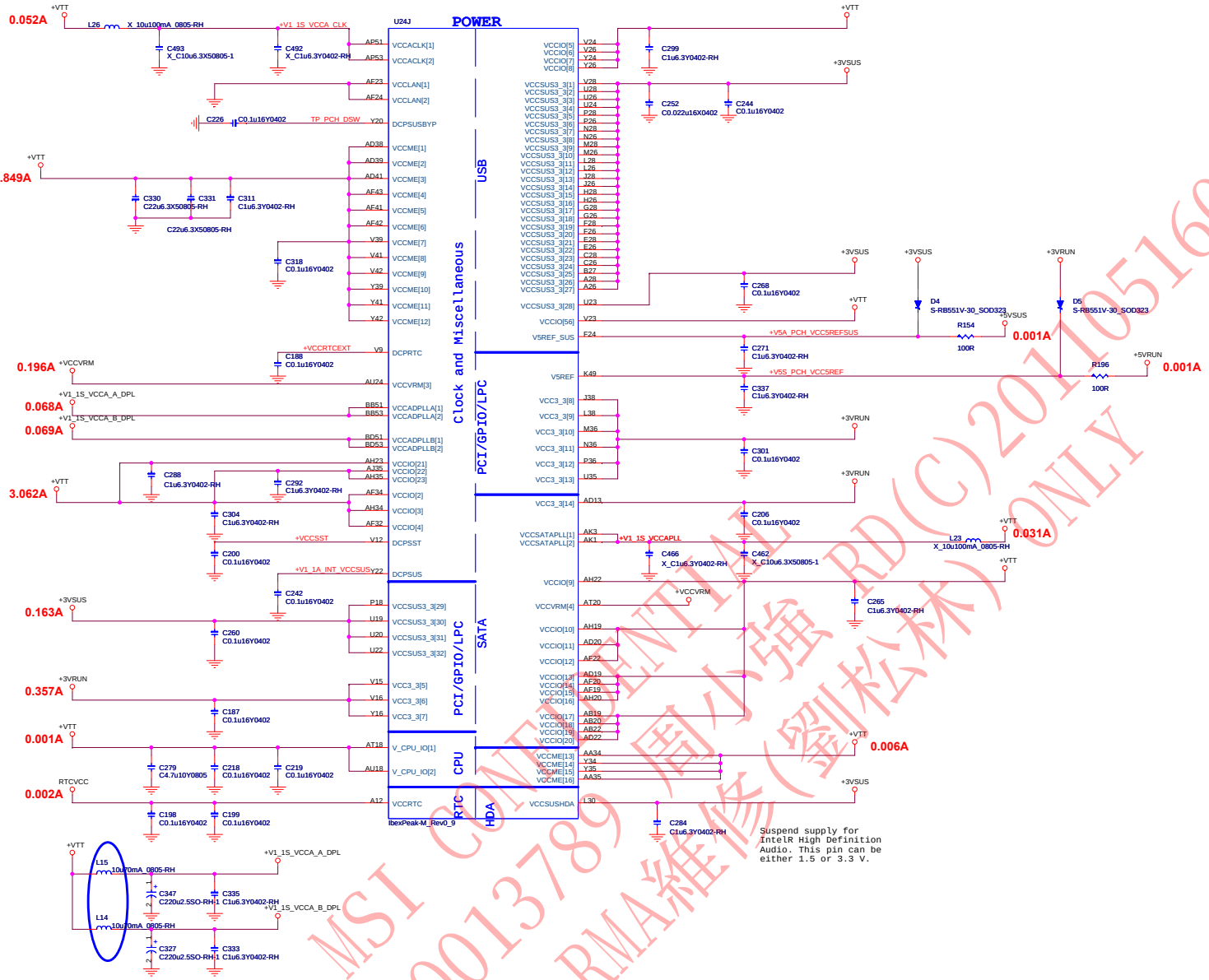
Size: Custom	Document Number: MS-1481		Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 27 of 56		

VccLAN may be grounded if Intel LAN is disabled.

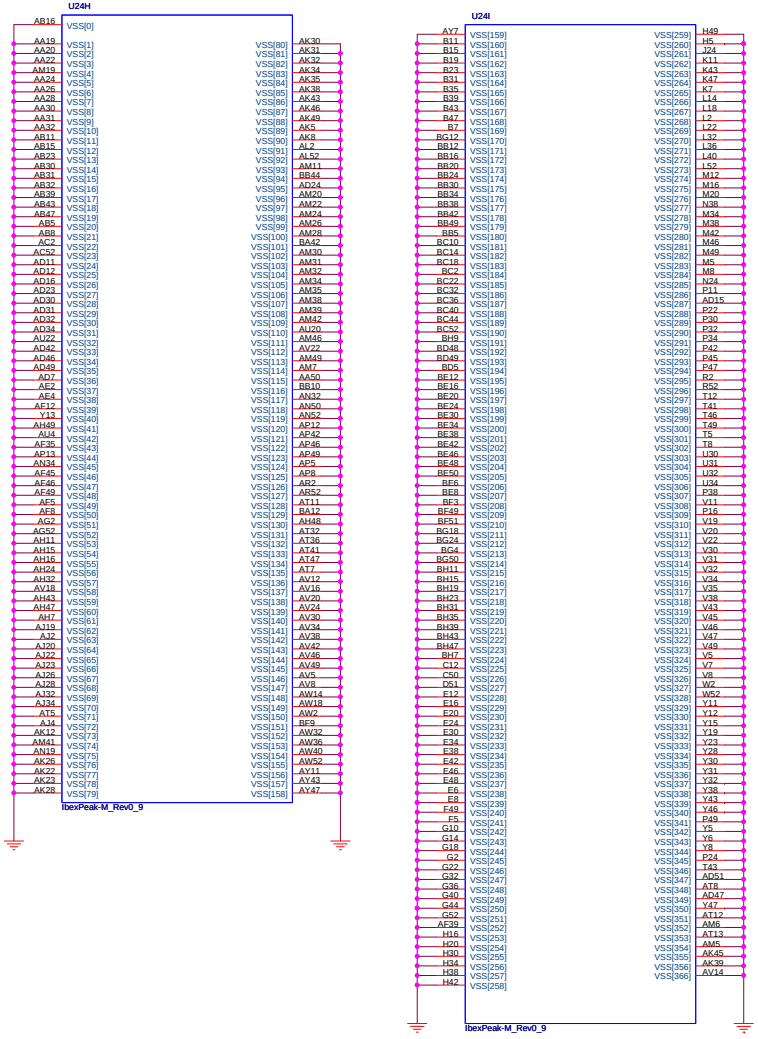
IBEXPEAK - M (POWER)



2101/01/25 Bead PN pending PN change to :L01-1006084-T19

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (POWER)		
Size: Custom	Document Number: MS-1481	Rev: 1.0	
Date: Thursday, May 13, 2010	Sheet 28 of 56		

IBEXPEAK - M (GND)



Intel® 5 Series Chipset Mobile SKUs

Feature Set		SKU Name(s)				
		QM57	HM57	PM55	HM55	QS57
PCI Express* 2.0 Ports		8	8	8	6[5]	8
USB* 2.0 Ports		14	14	14	12[4]	14
SATA Ports		6	6	6	4[6]	6
HDMI/DVI/VGA/SDVO/DisplayPort		Yes	Yes	No	Yes	Yes
LVDS		Yes	Yes	No	Yes	Yes
Graphics Support with PAVP 1.5		Yes	Yes	No	Yes	Yes
FIS Based Port Multiplier Support		Yes	Yes	Yes	No	Yes
Intel® Quiet System Technology		No	No	No	No	No
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	Raid 0/1/5/10 Support	Yes	Yes	Yes	No	Yes
Intel® ME Ignition FW only		No	No	Yes	No	No
Intel® AT		Yes	Yes	No	Yes	Yes
Intel® AMT 6.0		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Business		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Consumer		No	Yes	No	No	No
Intel® Remote Wake Technology		No	No	No	No	No

Figure 2-6. Platform Power Block Diagram—S3, M-Off, with WoL, No WoWLAN

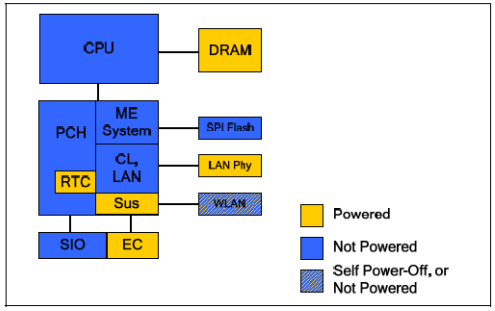


Figure 2-9. Platform Power Block Diagram—S4-5, M-Off, with WoL, No WoWLAN

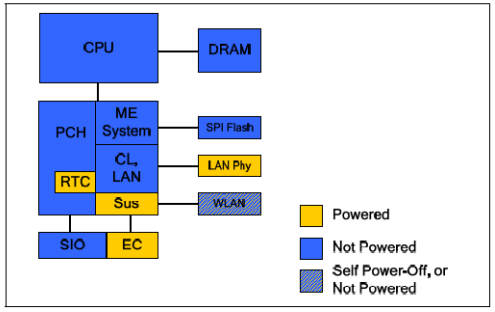


Table 113. Power Delivery Summary for Intel Management Engine SubSystem (Sheet 1 of 2)

What It Powers	Rail	Sx[1]/M3	Sx/Moff[2]	Sx/Moff/WOL[3]	Source	Enabled By	Power OK indicator
Platform 5-V Rail	V5.0A	On	On	On	5 V Always (Sx)		
DRAM VDD	V1.5U	On in S3	On in S3	On in S3	V1.5U	SLP_S4#	
DRAM VTT	V0.75S or V0.75U	Off[4]	Off[4]	Off[4]	V0.75S or V0.75U	SLP_S3#	
CK505	3.3 CK505	Off[5]	Off[5]	Off[5]	V3.3S	CKPWRGD	
Mobile Intel® 5 Series Chipset	1.05 VCORE	Off[5]	Off[5]	Off[5]	V1.05S		PWROK
WLAN	V3.3A	On	On	On	3.3 V Always		
	M3 Support + Intel® 82577 GbE LAN						
Intel® ME Local RAM	V1.05M	On	Off	Off	V1.05M	SLP_M#[6]	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	On	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	On	Off	Off[7]	V3.3M	SLP_M#[6]	MEPWROK
Integrated LAN controller	VCCLAN	On	Off	Off	V1.05M	SLP_M#[6]	
	No M3 Support + Intel® 82577 GbE LAN						
Intel ME Local RAM	V1.05M	Off	Off	Off	V1.05M	SLP_M#[6]	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	Off	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off[7]	V3.3M	SLP_M#[6]	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	V1.05M	SLP_M#[6]	
	No M3 Support + No Intel® 82577 GbE LAN						
Intel ME Local RAM	V1.05M/1.1M	Off	Off	Off	V1.05M	SLP_M#[6]	MEPWROK
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off[7]	V3.3M	SLP_M#[6]	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	Grounded		

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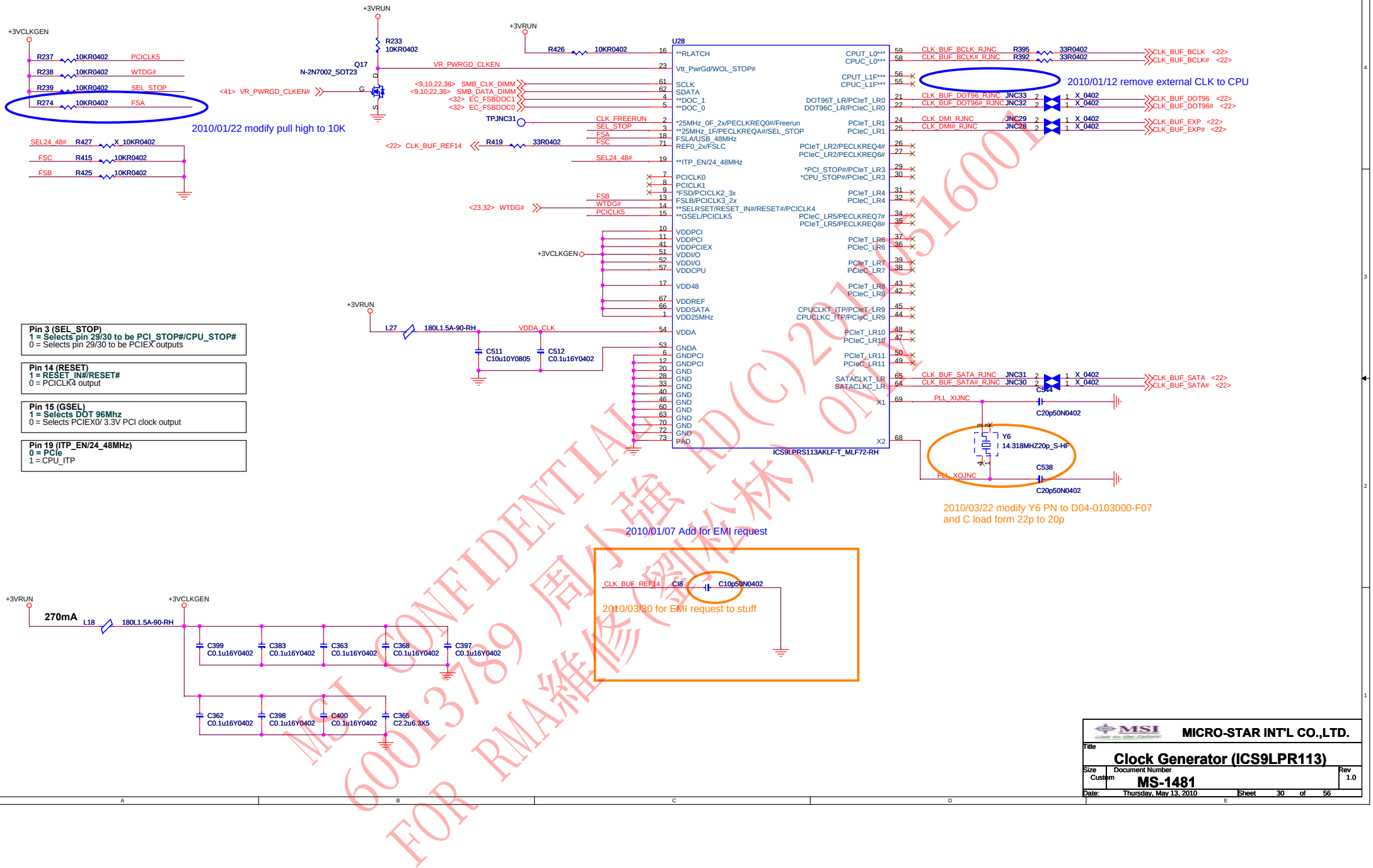
Title: IBEXPEAK - M (GND)

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 29 of 56



MSI MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator (ICS9LPR113)

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 30 of 56

CRT

2010/03/07 Add fuse for safety request(near Connector)

2010/03/29 for EMI suggestion modify bead to indutor 120nH

2010/01/22 modify R369,R359 to stuff

2010/03/29 for EMI suggestion C92,C104,C108 to stuff

2010/01/05 Add CRT HSYNC &VSYN level shift

N59-15F0751-A10

LVDS

2010/01/21 Change Pin define and remove resver component for layout space save and save cost(common used 1471 LVDS cable)

2010/01/21 remove resver component for layout space

N32-2200270-A81

Title	CRT,LVDS,CAMERA
Size	Custom
Document Number	MS-1481
Rev	1.0
Date:	Sheet 31 of 56

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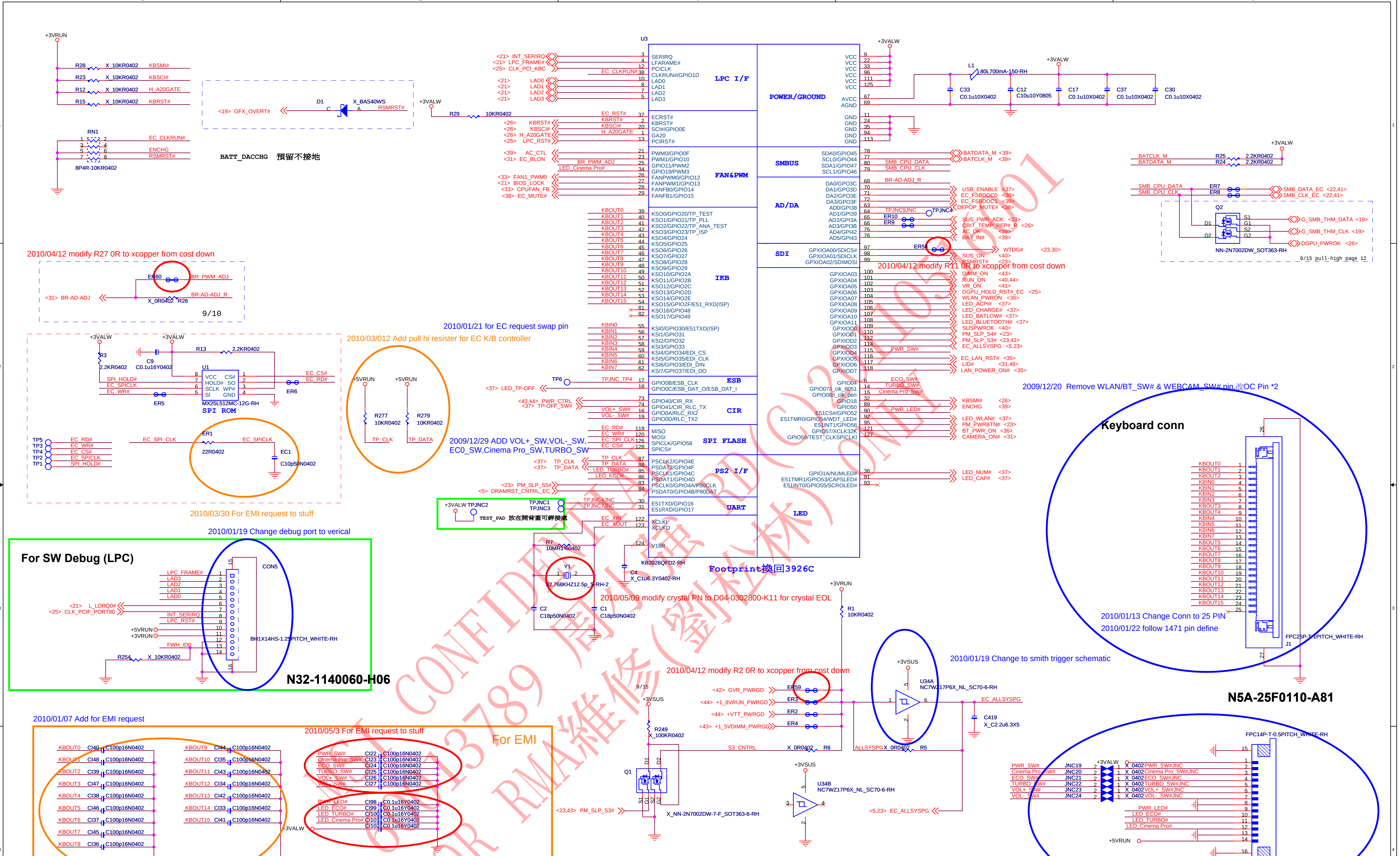


U3
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
KB3926QFD2-RH
Footprint換回3926C
BATT_DACCHG 預留不接地
SPI ROM
MX25L512MC-12G-RH
2010/04/12 modify R27 0R to xcopper from cost down
9/10
2010/03/012 Add pull hi resister for EC K/B controller
2010/01/21 for EC request swap pin
2009/12/29 ADD VOL+_SW,VOL-_SW, EC0_SW,Cinema Pro_SW,TURBO_SW
2010/03/30 For EMI request to stuff
2010/01/19 Change debug port to verical
TEST_PAD 放在開背蓋可焊接處
For SW Debug (LPC)
CON5
BH1X14HS-1.25PITCH_WHITE-RH
N32-1140060-H06
2010/04/12 modify R11 0R to xcopper from cost down
2009/12/20 Remove WLAN/BT_SW# & WEBCAM_SW# pin,改OC Pin *2
Keyboard conn
2010/01/13 Change Conn to 25 PIN
2010/01/22 follow 1471 pin define
FPC25P-1.0PITCH_WHITE-RH
J1
N5A-25F0110-A81
2010/05/09 modify crystal PN to D04-0302800-K11 for crystal EOL
2010/01/19 Change to smith trigger schematic
2010/04/12 modify R2 0R to xcopper from cost down
NC7WZ17P6X_NL_SC70-6-RH
X_NN-2N7002DW-7-F_SOT363-6-RH
NN-2N7002DW_SOT363-RH
9/15 pull-high page 12
2010/01/07 Add for EMI request
2010/05/3 For EMI request to stuff
For EMI
2010/05/3 For EMI request add CI98,CI99,CI100,CI101,CI102
2010/03/30 For EMI request to stuff
2010/01/25 for Layout request rechange to capacity
FPC14P-T-0.5PITCH_WHITE-RH
CON1
2010/01/18 Change pin define to 14 pin
N5A-14F0070-A81

Symbol	Parameter	Limits	Unit
		Typ	
Icc	Typical current consumption in operating state under Windows environment. All clock domains are running, and no keyboard/mouse activities.	20	mA

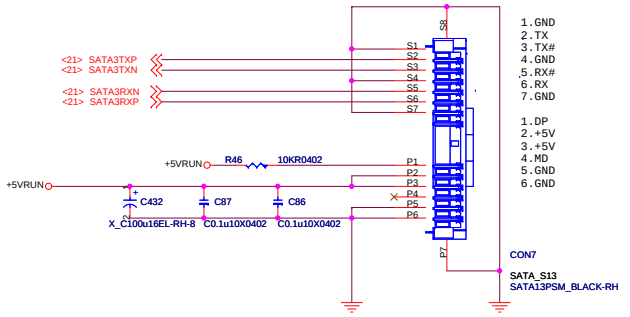
MICRO-STAR INT'L CO.,LTD.

Title: KBC/EC/uP(KB3926)

Size: Custom | Document Number: MS-1481 | Rev 1.0

Date: | Sheet 32 of 56

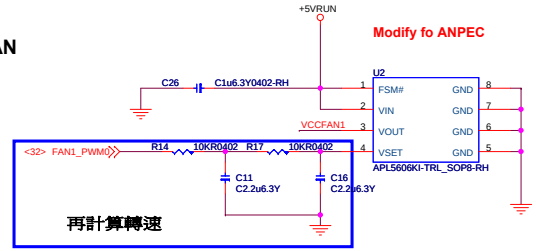
SATA ODD

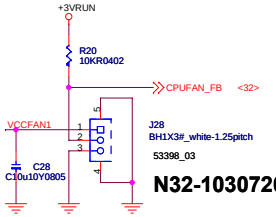


N5N-13M0010-A81

CPU FAN

Modify fo ANPEC

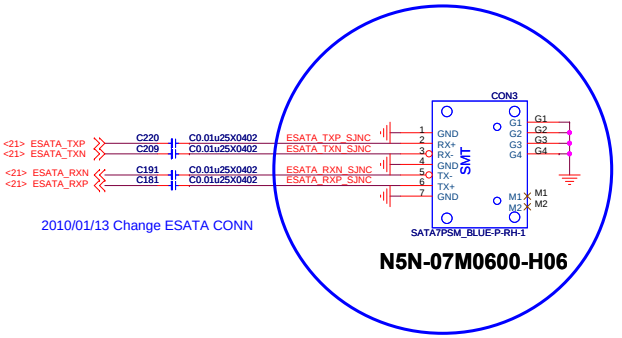




9/10 chage footprint

N32-1030720-A81

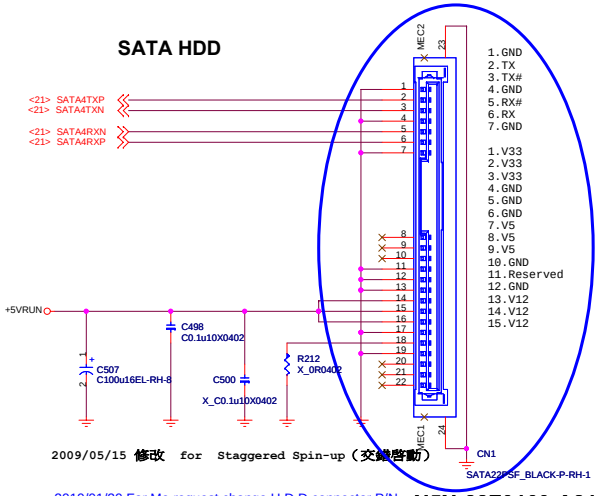
ESATA



2010/01/13 Change ESATA CONN

N5N-07M0600-H06

SATA HDD



2009/05/15 修改 for Staggered Spin-up（交錯啓動）

2010/01/20 For Me request change H.D.D connector P/N

N5N-22F0160-A81

MSI MICRO-STAR INT'L CO.,LTD.

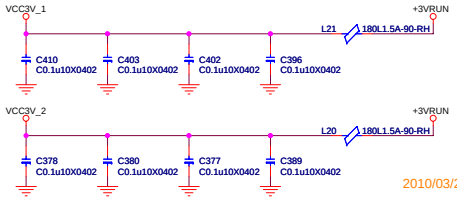
Title: ODD,HDD,ESATA,FAN

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: | Sheet 33 of 56

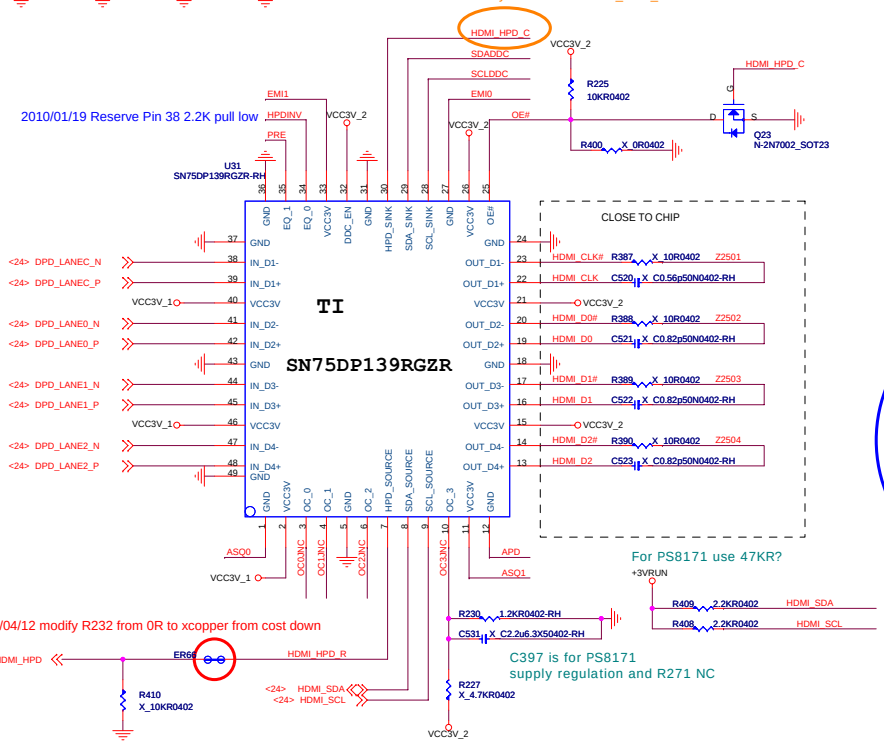
HDMI Switch

	HP_DET	OE#
UNPLUG	0	1 (HIGH Z)
PLUG	1	0 (ACTIVE)



2010/03/26 modify net name to HDMI_HPD_C

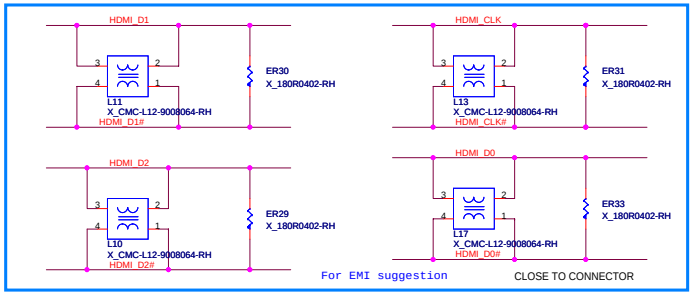
2010/01/19 Reserve Pin 38 2.2K pull low



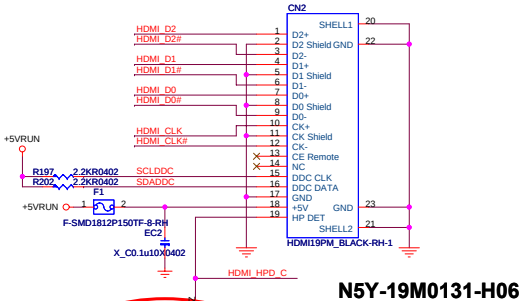
For PS8171 use 47KR?

2010/04/12 modify R232 from 0R to xcopper from cost down

C397 is for PS8171
supply regulation and R271 NC

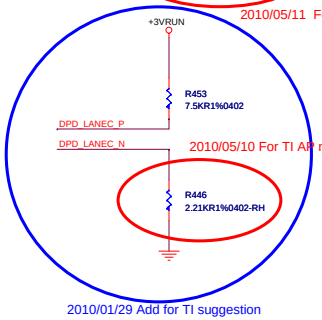


HDMI connector



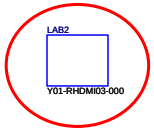
N5Y-19M0131-H06

2010/05/11 For Q23 damage risk to stuff D6 protection



2010/05/10 For TI APP note modfiy resister from 9.1KR to 2.2KR

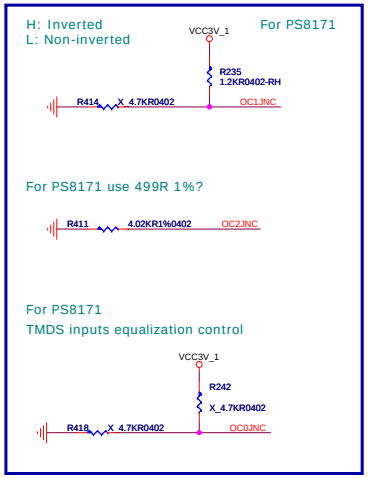
2010/01/29 Add for TI suggestion



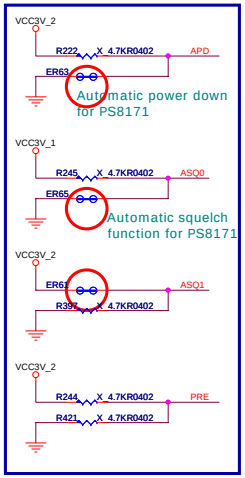
2010/05/11 For MVT version to stuff the HDMI lable

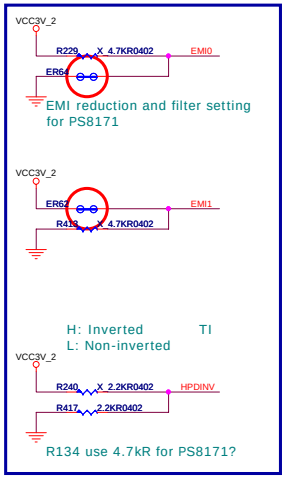
SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500KΩ) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down~500kΩ) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.9V	Pin 4
GND VCC	[ASQ1,ASQ0] = HL: No automatic squelch (Internal pull down~500kΩ) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.65K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up~500kΩ) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND VCC	EMI reduction and filter setting. (EMI1 internal pull up~500KΩ; EMI0 internal pull down~500KΩ) [EMI1,EMI0] = HL: No EMI reduction EMI0 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (internal pull-down~500KΩ) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500KΩ) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

Note2: High is HPD logic inverted, Low is HPD logic non-inverted



2010/04/12 modify R223,R234,R394,,R407,R422 from 0R to xcopper form cost down





MSI	MICRO-STAR INT'L CO.,LTD.	
Title	HDMI & LEVEL SHIFT	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date:	Sheet 34 of 56	

Note: add 0.1u cap at each power pin of LAN, please don't save.

Use External 1.05V Supply When Disable Switch Regulator.
If Using External 1.2V Supply Pls. Contact With FAE.

2010/01/08 remove it,If used jump write

2010/03/03 modify CHOKE1 form 2.2uH to 4.7uH for Realtek request

For RTL8105E
* C1841 to C1844 are for VDD10 pins-- 3, 13, 29, 45.

For RTL8111E
* C1841 to C1848 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

Part Reference	Choke1	C1840	C1846	R1662	R1668
Enable Switch Regulator					
Disable Switch Regulator	X	X	X	X	X

2010/04/14 modify R21 from 0R to xcopper for cost down

Pls. refer to 8111E Layout Guide for L1, C1, C2 selection criteria.

Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

2010/04/14 modify R8 from 0R to xcopper for cost down

2010/04/12 modify R256 from 0R to xcopper for cost down

2010/03/26 modify Xcopper to 0R

2010/04/14 modify R454 from 0R to xcopper for cost down

For RTL8105E
* C1851 to C1855 are for VDD33 pins-- 27, 39, 42, 47, 48.

For RTL8111E
* C1851 to C1856 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

VDD33 power on rise time >1ms

C1851 to C1856 Close To LAN chip

2010/01/03 Change the net name

2010/01/17 Chnge Digital GND to Analog GND

Please close to LAN Chip

2010/01/01 Change name net

2010/01/22 Add for LAN ECO

2010/04/14 modify R18 from 0R to xcopper for cost down

Remove For Disable Switch Regulator

2010/01/03 follow reference schematic remover 3 capacity

2010/01/04 follow reference schematic add 10K pull low

2010/04/12 modify R16 from 0R to xcopper for cost down

N55-08F0491-SH4

EEPROM Select

For RTL 8105E

VDD33

R11 1K GPO

2.When using EFuse/BIOS Patch.

FOR RTL 8111E

VDD33

R11 1K GPO

R19 10K SMBDATA

3.When using EFuse/BIOS Patch without ASF function.

For EMI

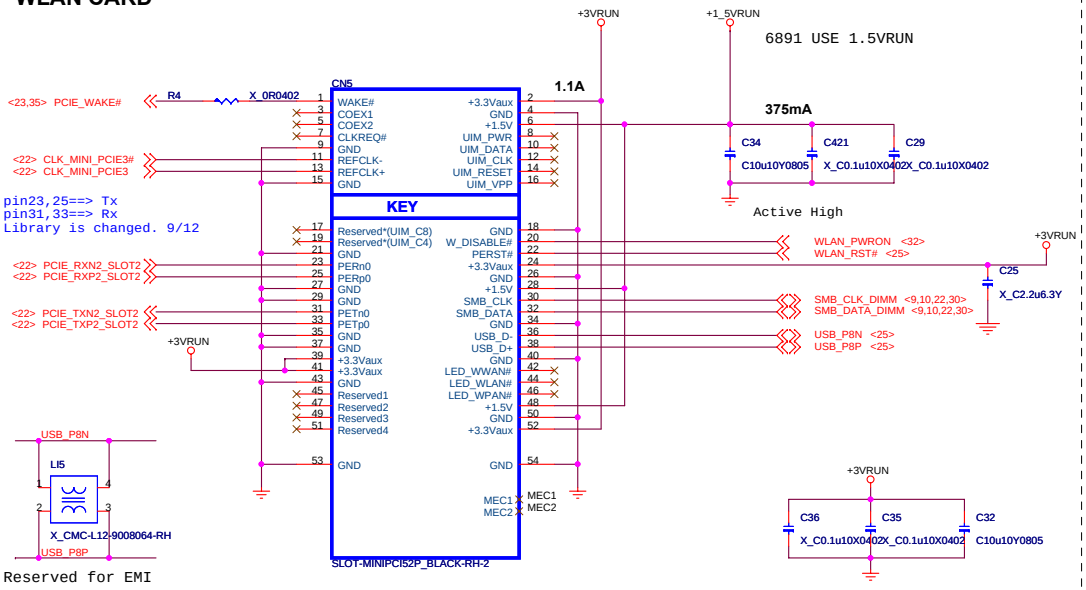
2010/03/26 reserve 0.1uF *4 for EMI

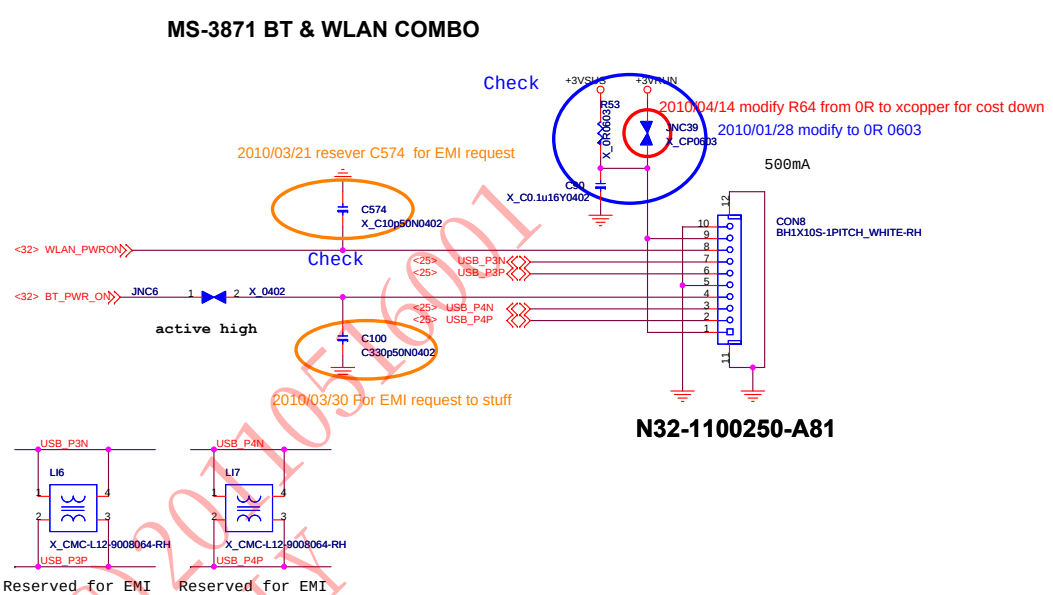
MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(RTL 8111EL)

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: | Sheet 35 of 56





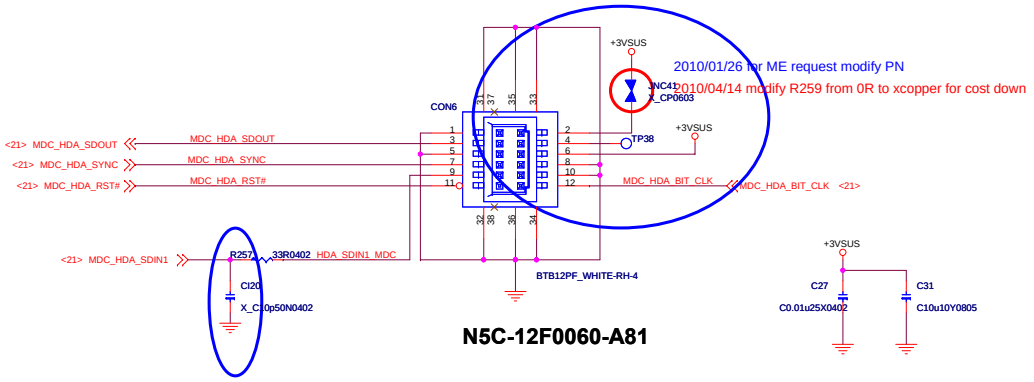
MICRO-STAR INT'L CO.,LTD.

Title: WLAN,BT,Combo ,3G SIM CARD

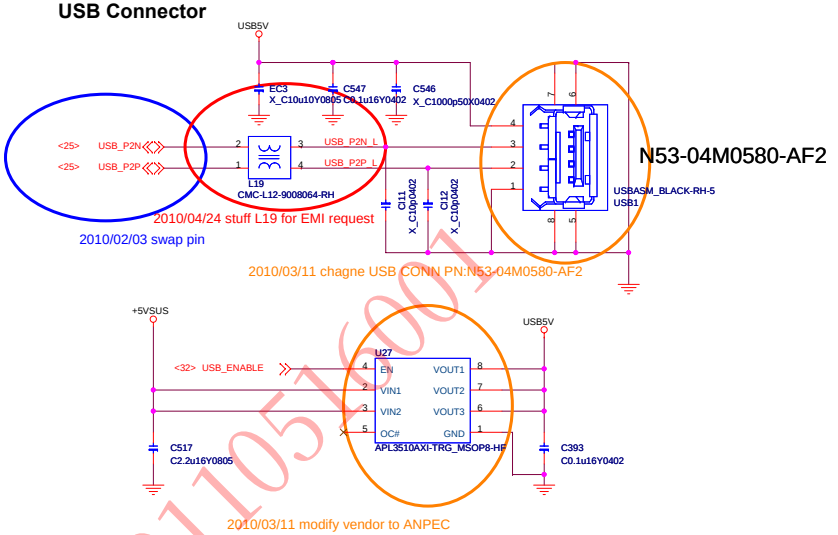
Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 36 of 56

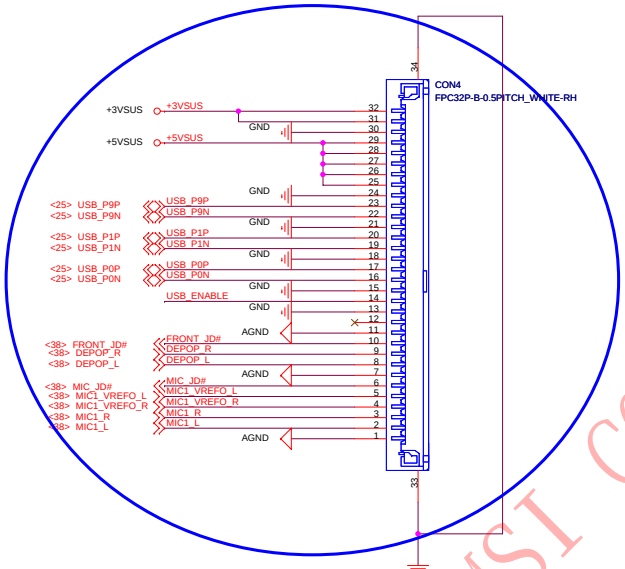
MDC



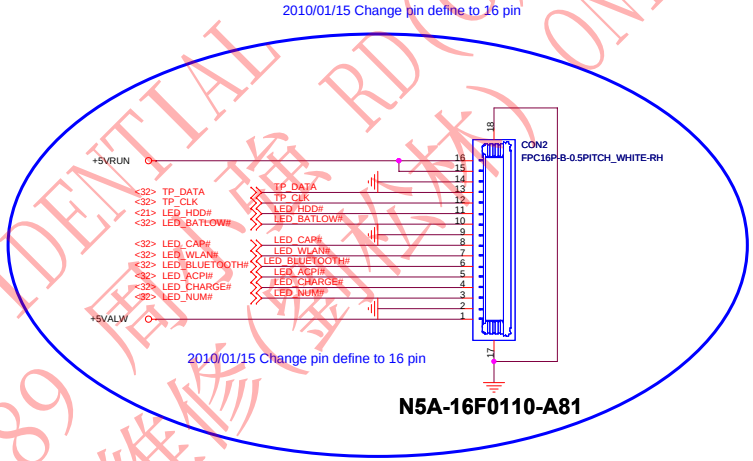
USB Connector



2010/01/15 Change pin define to 32 pin



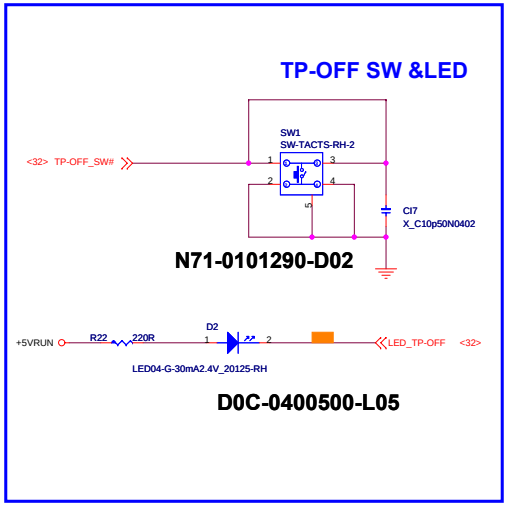
2010/01/15 Change pin define to 16 pin

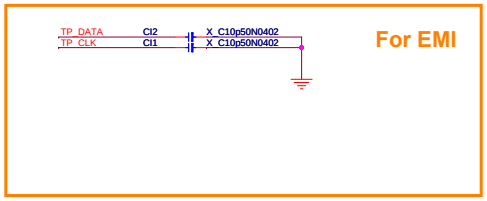


Connector to P.44 Board A

Connector to P.46 Board C

TP-OFF SW &LED



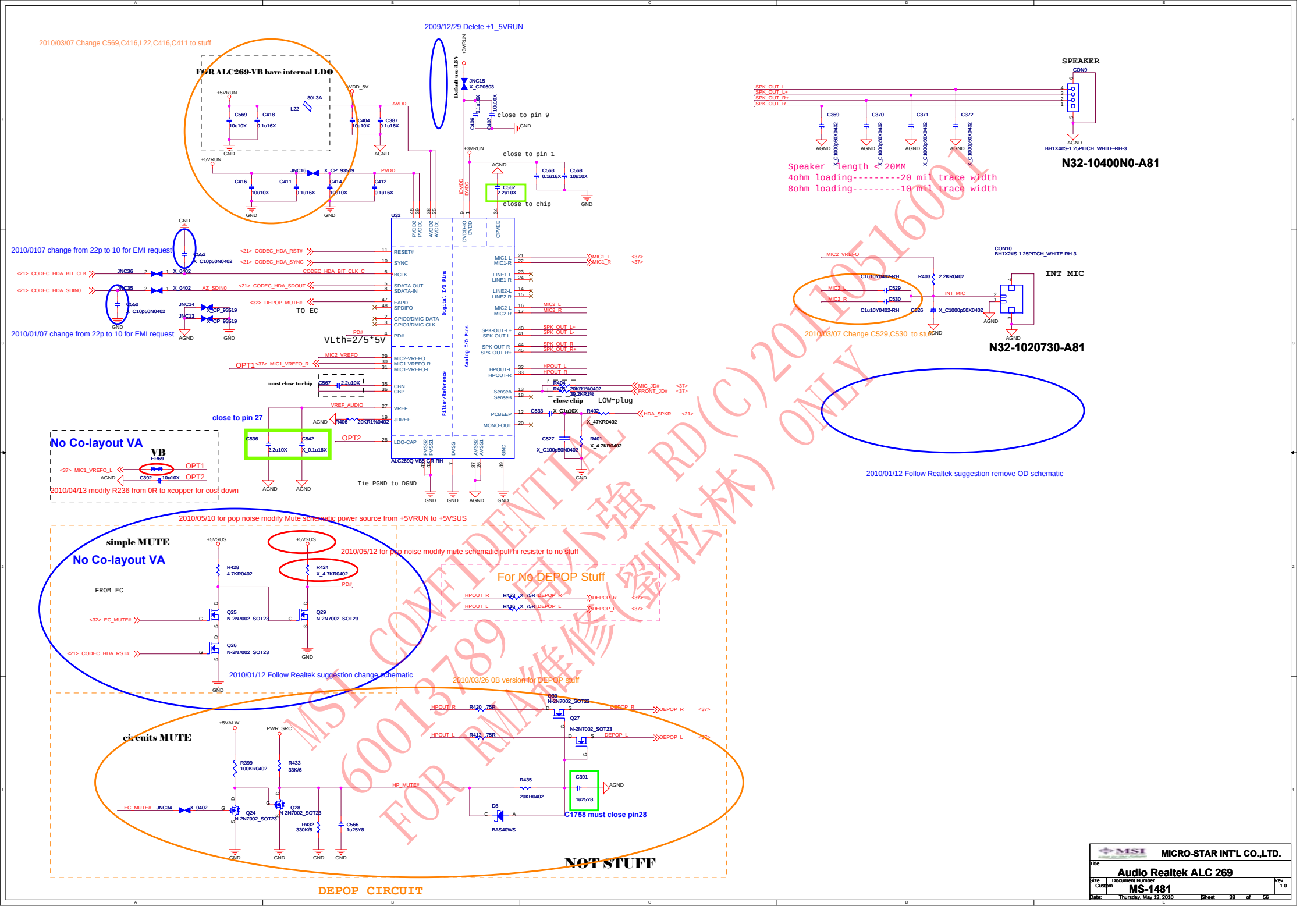


MICRO-STAR INT'L CO.,LTD.

Title: MDC,USB,CONN

Size: Custom | Document Number: MS-1481 | Rev: 1.0

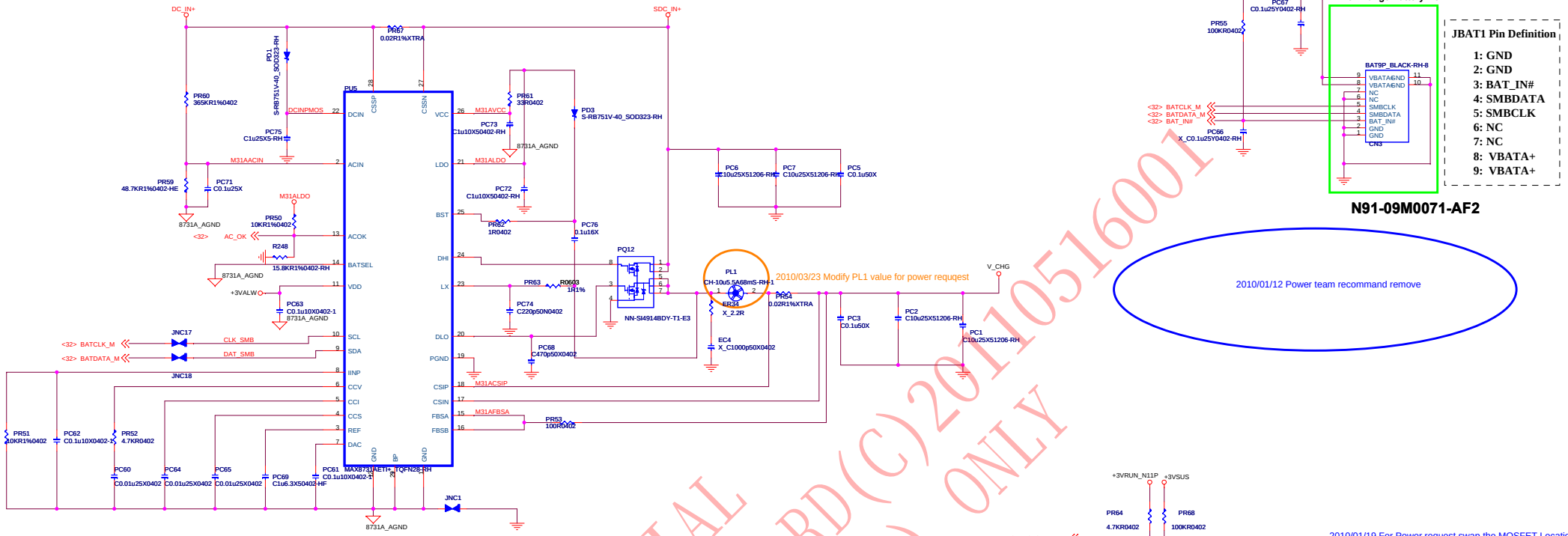
Date: Thursday, May 13, 2010 | Sheet 37 of 56



Title	Audio Realtek ALC 269
Size	Custom
Document Number	MS-1481
Rev	1.0
Date:	Thursday, May 13, 2010
Sheet	38 of 56

MICRO-STAR INT'L CO.,LTD.

Adapter input voltage set 19 Voltage



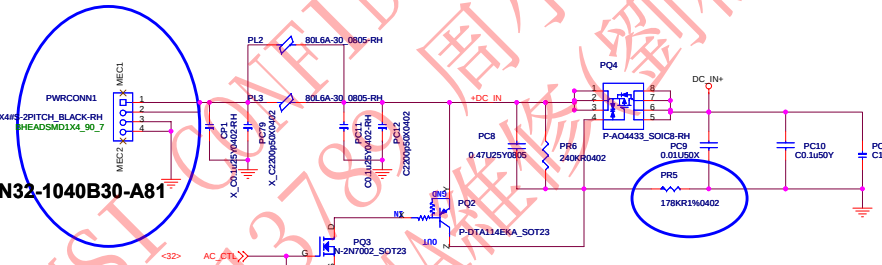
2010/03/23 Modify PL1 value for power requqest

2010/01/12 Power team recommand remove

N91-09M0071-AF2

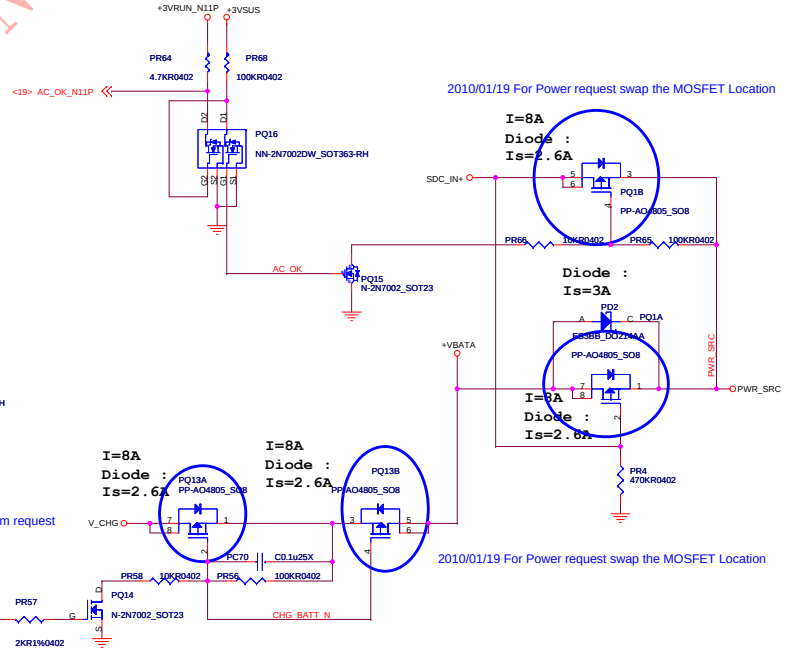
IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. V_IINP = IINPUT x RS1 x 3mA/V x PR25

2009/12/31 更換power connector
2010/01/12 Chage connector same the 16G1



N32-1040B30-A81

2010/01/12 modify from 0603 174K to 0402 178K for power team request

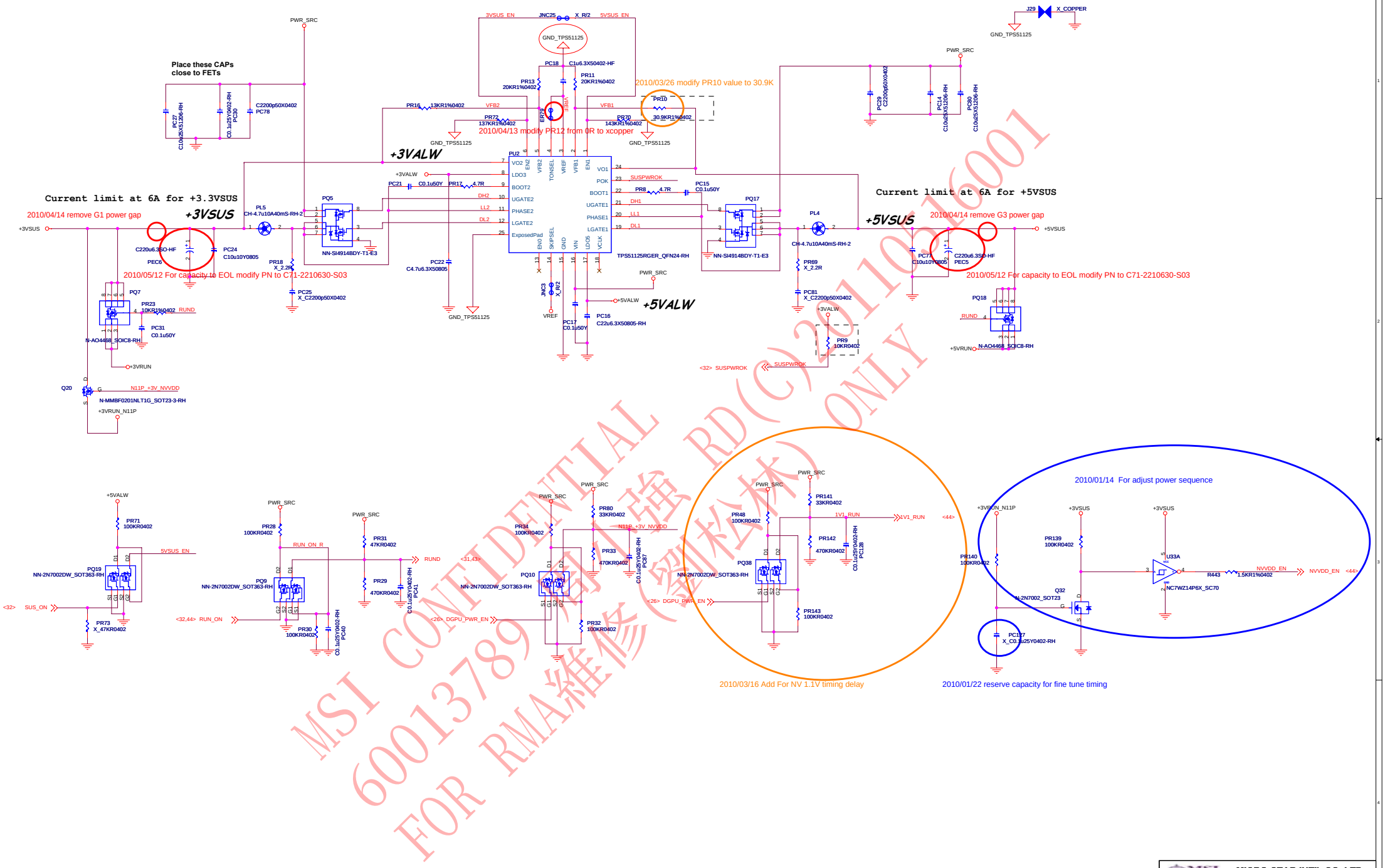


MICRO-STAR INT'L CO.,LTD.

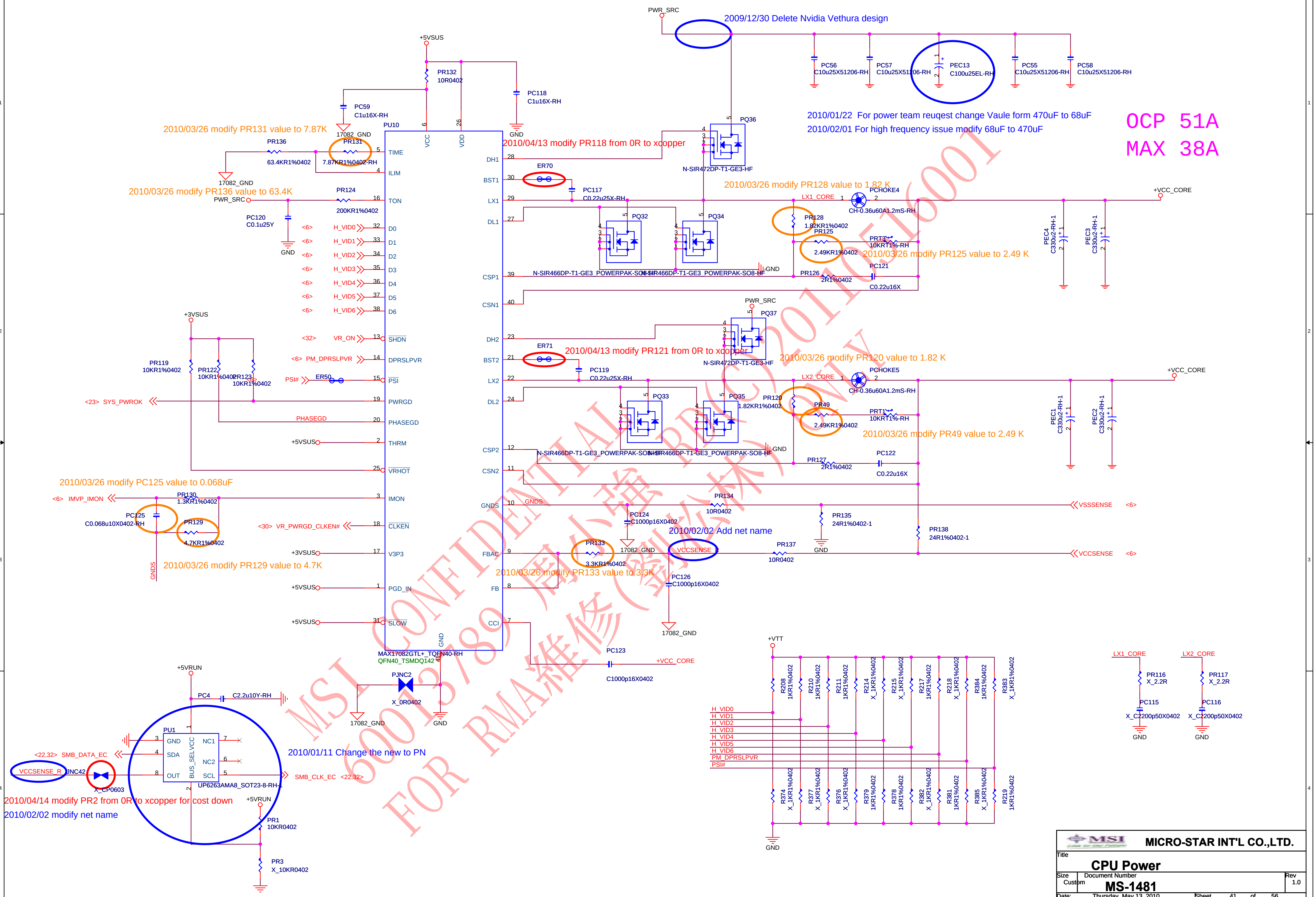
Title: Battery Select & Charger

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 39 of 56



MICRO-STAR INT'L CO.,LTD.	
Title	System power
Size: Custom	Document Number: MS-1481
Rev	1.0
Date: Thursday, May 13, 2010	Sheet 40 of 56



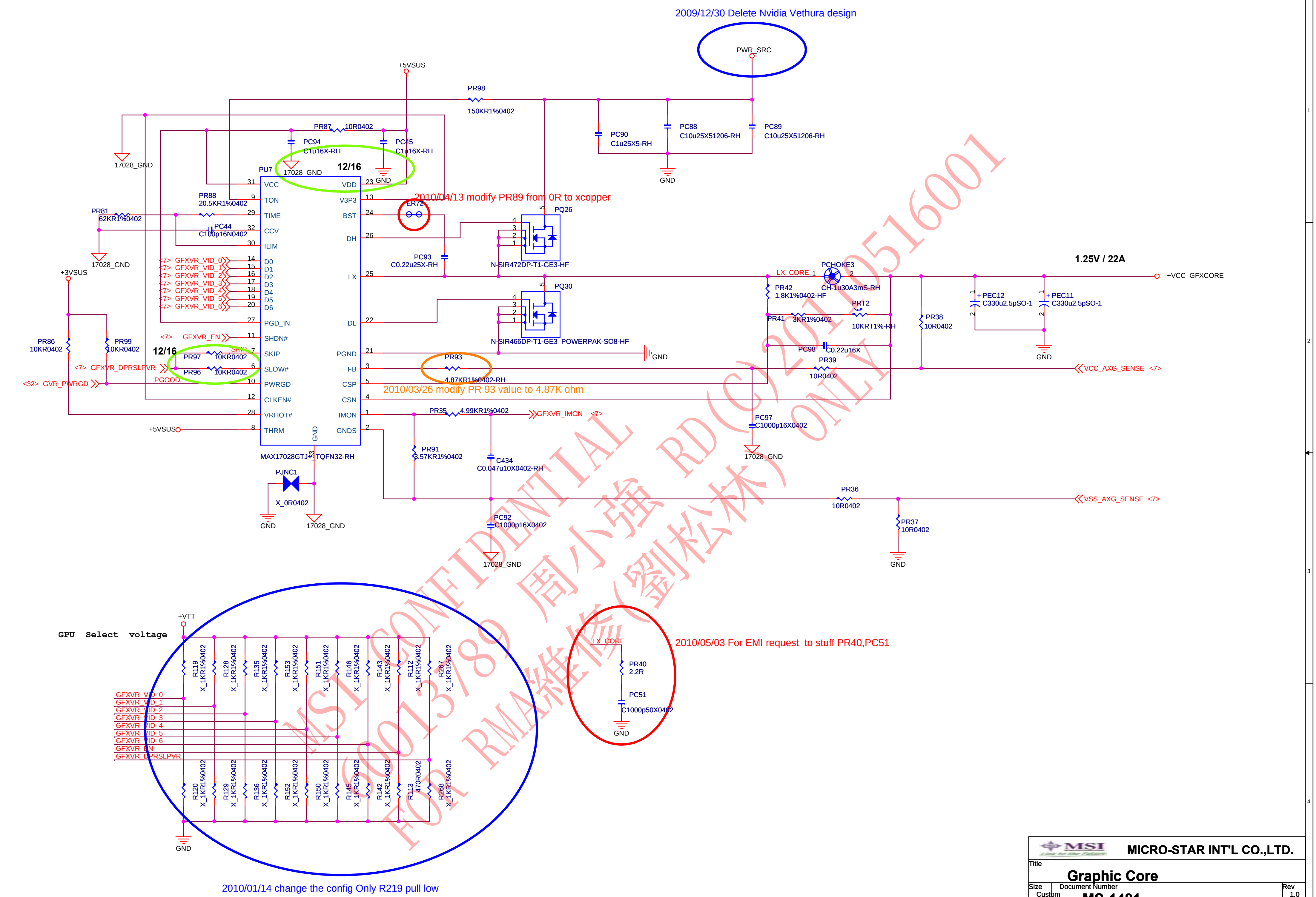
2009/12/30 Delete Nvidia Vethura design
2010/01/22 For power team reuqest change Vaule form 470uF to 68uF
2010/02/01 For high frequency issue modify 68uF to 470uF
OCP 51A
MAX 38A
2010/03/26 modify PR131 value to 7.87K
2010/04/13 modify PR118 from 0R to xcopper
2010/03/26 modify PR136 value to 63.4K
2010/03/26 modify PR128 value to 1.82 K
2010/03/26 modify PR125 value to 2.49 K
2010/04/13 modify PR121 from 0R to xcopper
2010/03/26 modify PR120 value to 1.82 K
2010/03/26 modify PR49 value to 2.49 K
2010/03/26 modify PC125 value to 0.068uF
2010/03/26 modify PR129 value to 4.7K
2010/02/02 Add net name
2010/03/26 modify PR133 value to 3.3K
2010/01/11 Change the new to PN
2010/04/14 modify PR2 from 0R to xcopper for cost down
2010/02/02 modify net name
PU10
MAX17082GTL+_TQFN40-RH
QFN40_TSMDQ142
PU1
UP6263AMA8_SOT23-8-RH-1
PWR_SRC
+5VSUS
+3VSUS
+VCC_CORE
+5VRUN
+VTT
LX1_CORE
LX2_CORE
VSSSENSE
VCCSENSE
VCCSENSE_R
SMB_DATA_EC
SMB_CLK_EC
IMVP_IMON
VR_PWRGD_CLKEN#
SYS_PWROK
PM_DPRSLPVR
VR_ON
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PSI#

MICRO-STAR INT'L CO.,LTD.

Title: CPU Power

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 41 of 56

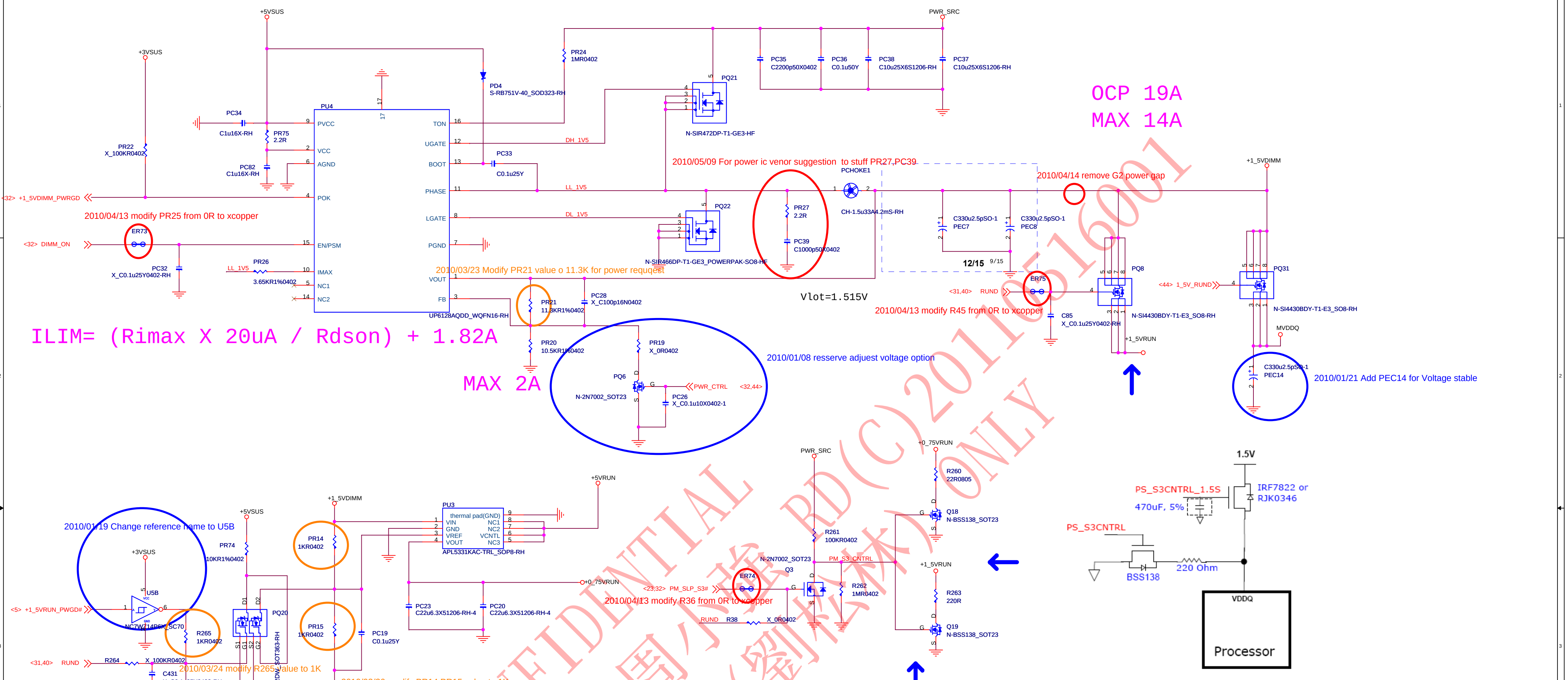

2009/12/30 Delete Nvidia Vethura design
PWR_SRC
+5VSUS
PR98
150KR1%0402
PC90
C1u25X5-RH
PC88
C10u25X51206-RH
PC89
C10u25X51206-RH
GND
PR87
10R0402
PC94
C1u16X-RH
PC45
C1u16X-RH
17028_GND
12/16
PU7
VCC
TON
TIME
CCV
ILIM
D0
D1
D2
D3
D4
D5
D6
PGD_IN
SHDN#
SKIP
SLOW#
PWRGD
CLKEN#
VRHOT#
THRM
VDD
V3P3
BST
DH
LX
DL
PGND
FB
CSP
CSN
IMON
GNDS
MAX17028GTJ+TQFN32-RH
2010/04/13 modify PR89 from 0R to xcopper
ER72
PQ26
N-SIR472DP-T1-GE3-HF
PQ30
N-SIR466DP-T1-GE3_POWERPAK-SO8-HF
PC93
C0.22u25X-RH
PR88
20.5KR1%0402
PR81
62KR1%0402
PC44
C100p16N0402
<7> GFXVR_VID_0
<7> GFXVR_VID_1
<7> GFXVR_VID_2
<7> GFXVR_VID_3
<7> GFXVR_VID_4
<7> GFXVR_VID_5
<7> GFXVR_VID_6
+3VSUS
PR86
10KR0402
PR99
10KR0402
<7> GFXVR_EN
PR97
10KR0402
PR96
10KR0402
<7> GFXVR_DPRSLPVR
<32> GVR_PWRGD
PGOOD
1.25V / 22A
LX_CORE
PCHOKE3
CH-1u30A3mS-RH
+VCC_GFXCORE
PR42
1.8K1%0402-HF
PR41
3KR1%0402
PRT2
10KRT1%-RH
PEC12
C330u2.5pSO-1
PEC11
C330u2.5pSO-1
PR38
10R0402
PC98
C0.22u16X
PR39
10R0402
VCC_AXG_SENSE <7>
PR93
4.87KR1%0402-RH
2010/03/26 modify PR 93 value to 4.87K ohm
PR35
4.99KR1%0402
GFXVR_IMON <7>
PC97
C1000p16X0402
PR91
3.57KR1%0402
C434
C0.047u10X0402-RH
PJNC1
X_0R0402
PR36
10R0402
VSS_AXG_SENSE <7>
PR37
10R0402
PC92
C1000p16X0402
GPU Select voltage
+VTT
R119 X_1KR1%0402
R128 X_1KR1%0402
R135 X_1KR1%0402
R153 X_1KR1%0402
R151 X_1KR1%0402
R146 X_1KR1%0402
R143 X_1KR1%0402
R112 X_1KR1%0402
R267 X_1KR1%0402
GFXVR_VID_0
GFXVR_VID_1
GFXVR_VID_2
GFXVR_VID_3
GFXVR_VID_4
GFXVR_VID_5
GFXVR_VID_6
GFXVR_EN
GFXVR_DPRSLPVR
R120 X_1KR1%0402
R129 X_1KR1%0402
R136 X_1KR1%0402
R152 X_1KR1%0402
R150 X_1KR1%0402
R145 X_1KR1%0402
R142 X_1KR1%0402
R113 470R0402
R268 X_1KR1%0402
2010/01/14 change the config Only R219 pull low
2010/05/03 For EMI request to stuff PR40,PC51
PR40
2.2R
PC51
C1000p50X0402

MICRO-STAR INT'L CO.,LTD.

Title: **Graphic Core**

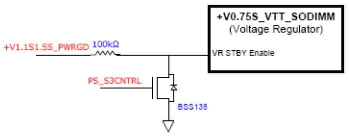
Size	Document Number	Rev
Custom	MS-1481	1.0

Date: Thursday, May 13, 2010 Sheet 42 of 56



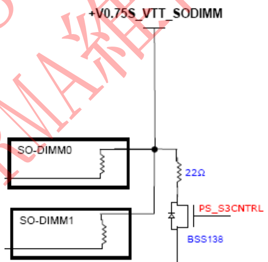
In current designs, Processor V_{DDQ} is powered with +V1.5, which is "ON" in S3. This is changed to a switching rail which is "OFF" during S3. A power FET is required to control the Processor V_{DDQ} (1.5 V) power. For N-FET (e.g., IRF7822 or RJK0346), gate voltage of FET (PS_S3CNTRL_1.5S) is derived from SLP_S3# and at 12-V logic. RDS(ON) of the FET used in CRB is in the range of 5 mΩ. Every design is different and designer should select an appropriate FET so that the required voltage rail specification is maintained at the Processor V_{DDQ} pins.

Signal Name	Source	Voltage Level	Comments
PS_S3CNTRL	Inverted SLP_S3# signal	In CRB, it is a 3.3-V signal.	Voltage should be high enough to turn ON or OFF the MOSFET. When selecting the MOSFET, insure $V_{gs}>V_{gsth}$.
PS_S3CNTRL_1.5S	Buffered SLP_S3# signal	In Intel CRB it is a 12-V signal.	Voltage should be high enough to turn ON or OFF the Power MOSFET. When selecting the MOSFET, insuree $V_{gs}>V_{gsth}$.

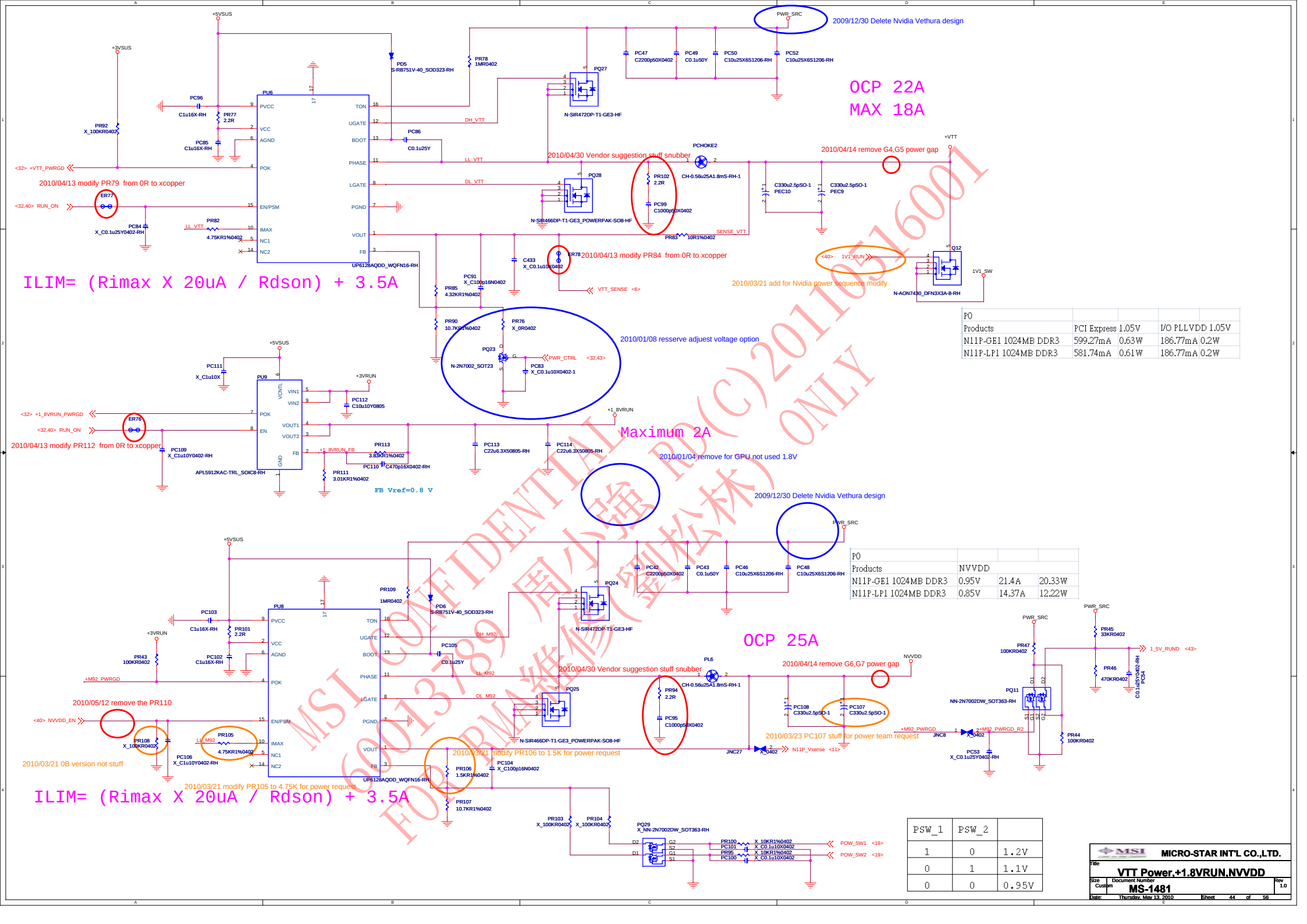


+V0.75S_VTT_DIMM should ramp up later than +V1.5S_CPU_VDDQ. Circuit shown above is used to delay +V0.75V_VTT_SODIMM ramp with respect to +V1.5S_CPU_VDDQ.

100-kΩ isolation resistor is used in reference design so that when gate is turned on, it does not pull +V1.1S1.5S_PWRGD signal to low which may impact other functionality on the board. To ensure +V1.1S1.5S_PWRGD signal levels maintained, comparator pull-up has been changed from 100 kΩ to 1 kΩ (R2F2 in Intel CRB schematic).



CKE is driven low by the processor to put the memory in self refresh while entering S3. When the processor +V1.5_CPU_VDDQ power is turned off, the discharge path on +V0.75S ensures CKE stays low during S3. To avoid any glitch on CKE signals during S3 entry, faster (22 Ω) discharge circuitry ensures +V0.75 ramps down before processor +V1.5S_CPU_VDDQ is turned off.



P0			
Products	PCI Express 1.05V	I/O PLLVDD 1.05V	
N11P-GE1 1024MB DDR3	599.27mA	0.63W	186.77mA 0.2W
N11P-LP1 1024MB DDR3	581.74mA	0.61W	186.77mA 0.2W

P0			
Products	NVVDD		
N11P-GE1 1024MB DDR3	0.95V	21.4A	20.33W
N11P-LP1 1024MB DDR3	0.85V	14.37A	12.22W

PSW_1	PSW_2	
1	0	1.2V
0	1	1.1V
0	0	0.95V

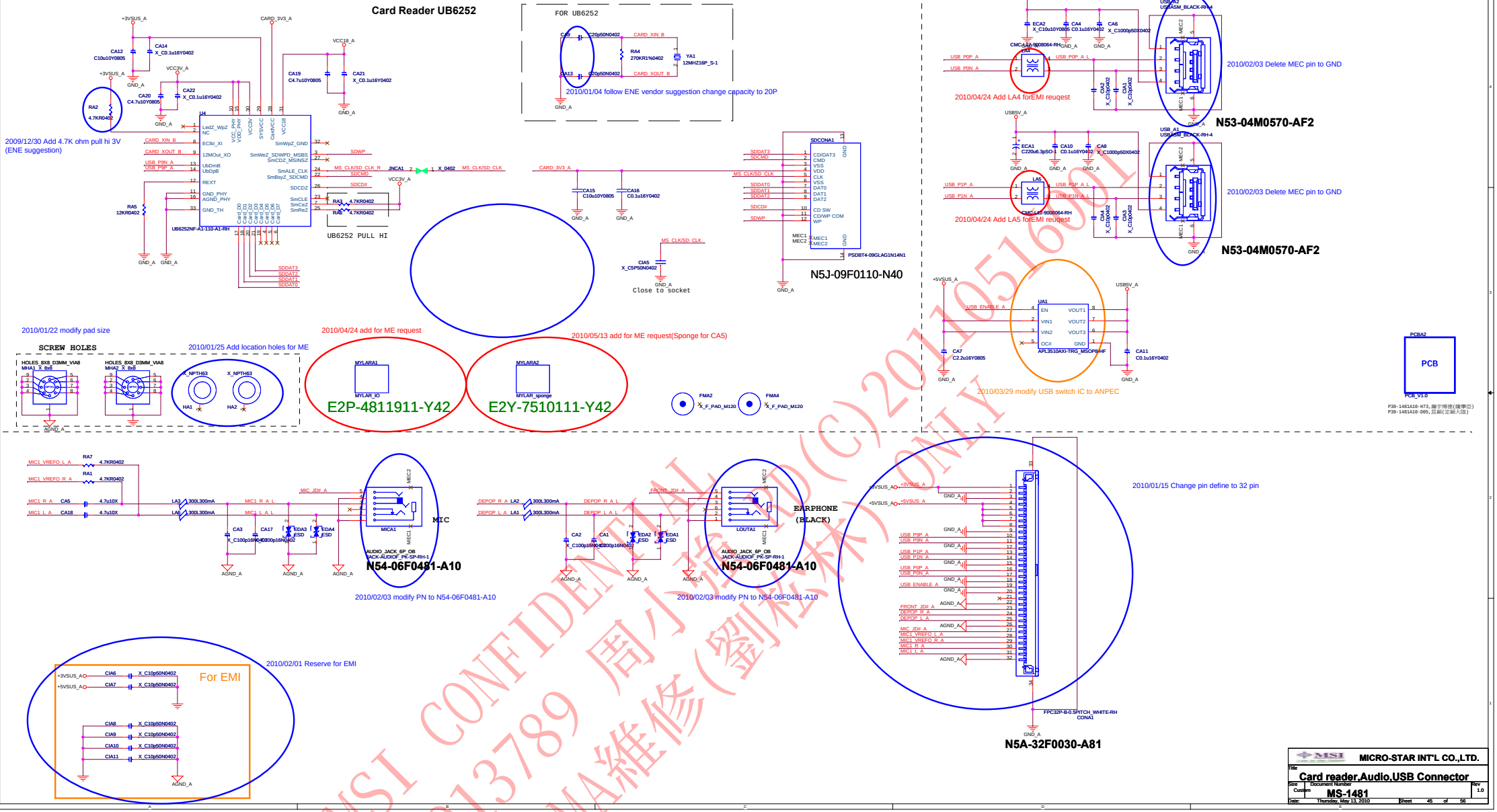
MICRO-STAR INT'L CO.,LTD.

Title: VTT Power,+1.8VRUN,NVVDD

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 44 of 56

Card Reader UB6252



MICRO-STAR INT'L CO.,LTD.

Title: Card reader,Audio,USB Connector

Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 45 of 56

PCBA3

PCB

PCB_V1.0

P30-1481B10-H73,瀚宇博德(薩摩亞),
P30-1481B10-D05,昆精(定穎大陸)

+3VALW_B

DB1 X_S-RB551V-30_SOD323

RB3 10KR

PWR_SW#_B

CB1 C0.1u10X0402

GND_B

2009/12/29 ADD VOL+_SW,VOL-_SW,EC0_SW,HIQ_SW,TURBO_SW

VOL+_SW#_B JNCB6 X_0402 SWB3 SW-TACT-1B CIB6 X_C0.1u16Y0402 N71-0100900-D02

VOL-_SW#_B JNCB4 X_0402 SWB4 SW-TACT-1B CIB4 X_C0.1u16Y0402 N71-0100900-D02

TURBO_SW#_B JNCB5 X_0402 SWB5 SW-TACT-1B CIB5 X_C0.1u16Y0402 N71-0100900-D02

Cinema Pro_SW#_B JNCB2 X_0402 SWB1 SW-TACT-1B CIB1 X_C0.1u16Y0402 N71-0100900-D02

ECO_SW#_B JNCB3 X_0402 SWB6 SW-TACT-1B CIB3 X_C0.1u16Y0402 N71-0100900-D02

PWR_SW#_B JNCB1 X_0402 SWB2 SW-TACT-1B CIB2 X_C0.1u16Y0402 N71-0100900-D02

FMB3 X_F_PAD_M120

FMB2 X_F_PAD_M120

FMB1 X_F_PAD_M120

FMB4 X_F_PAD_M120

SCREW HOLES

MHB1 X_R6.2D2.7 holes_r244d106

MHB2 X_R6.2D2.7 holes_r244d106

X_NPTH63

X_NPTH63

HB1

HB2

2010/01/25 Add Location holes for ME

2010/03/29 Add launch baord Mylar for ME

MYLARB1 MYLAR_Launch

E2P-4811711-Y42

N5A-14F0090-A81

FPC14P-T-0.5PITCH_WHITE-RH

+3VALW_B

PWR_SW#_B

Cinema Pro_SW#_B

ECO_SW#_B

VOL+_SW#_B

VOL-_SW#_B

LED_PWR#B

LED_ECO#B

LED_TURBO#B

LED_Cinema Pro#_B

+5VRUN_B

CONB1

2010/004/30 modify connector PN for ME request

LED

+5VRUN_B

RNB1 8P4R-220R0402

DB5 LED04-B-20mA3.8V_3216-RH LED_PWR#B BLUE D0C-0405230-L05

DB3 X_LED04-B-20mA3.8V_3216-RH LED_ECO#B BLUE D0C-0405230-L05 (WLAN)

DB4 LED04-O-30mA2.0V_320160-HF LED_TURBO#B Amber D0C-0409300-L05 (P1)

DB2 X_LED04-B-20mA3.8V_3216-RH LED_Cinema Pro#_B BLUE D0C-0405230-L05

LED

+5VRUN_B

RNB2 8P4R-220R0402

DB9 LED04-B-20mA3.8V_3216-RH LED_PWR#B BLUE D0C-0405230-L05

DB7 X_LED04-B-20mA3.8V_3216-RH LED_ECO#B BLUE D0C-0405230-L05 (WLAN)

DB6 LED04-O-30mA2.0V_320160-HF LED_TURBO#B BLUE D0C-0409300-L05 (P1)

DB8 X_LED04-B-20mA3.8V_3216-RH LED_Cinema Pro#_B BLUE D0C-0405230-L05

2010/03/26 modify DB4 & DB6 color to Amber
modify DB2,DB3,DB7,DB8 to no stuff for ID request

For EMI

LED_PWR#B CIB8 X_C100p16N0402

LED_ECO#B CIB9 X_C100p16N0402

LED_TURBO#B CIB10 X_C100p16N0402

LED_Cinema Pro#_B CIB7 X_C100p16N0402

+5VRUN_B CIB11 X_C100p16N0402

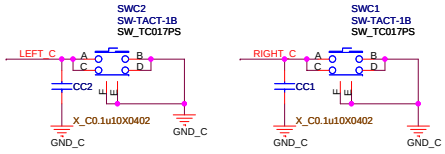
GND_B

MSI MICRO-STAR INT'L CO.,LTD.

Title: Launch Board

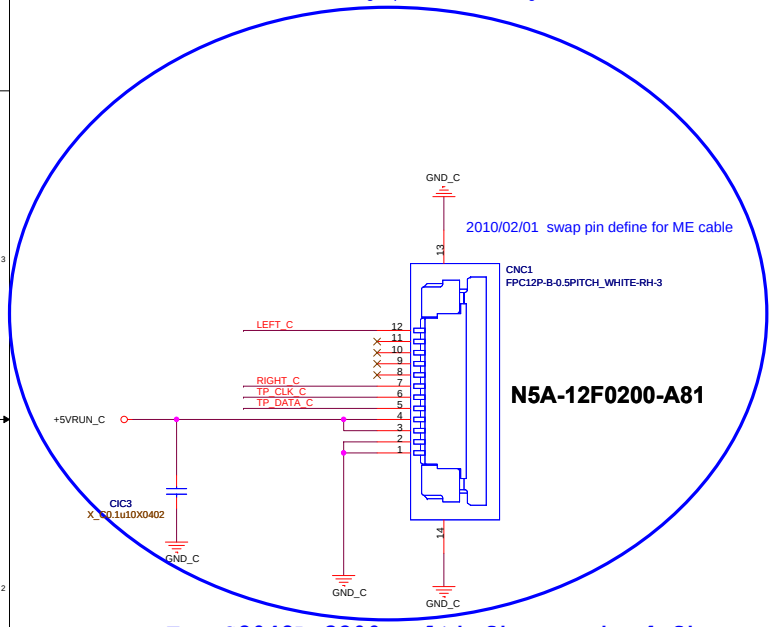
Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 46 of 56



N71-0100900-D02 **N71-0100900-D02**

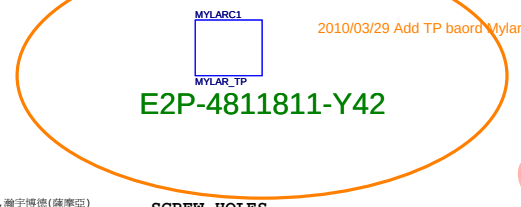
2010/01/14 Chagne pin define for multi finger



N5A-12F0200-A81

2010/02/01 swap pin define for ME cable

For S8048D-3200 multi finger pin define

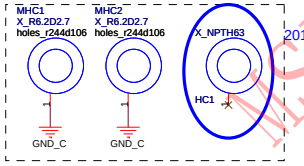


E2P-4811811-Y42

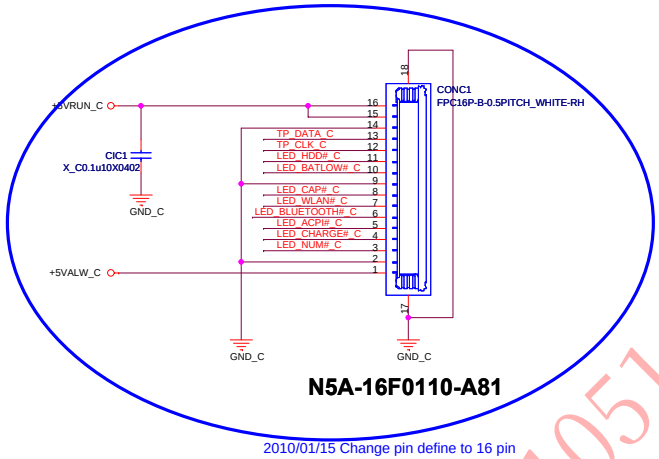
2010/03/29 Add TP baord Mylar for ME

P30-1481C10-H73,迪宇博德(薩摩亞)
P30-1481C10-D0S,昆精(定精大陸)

SCREW HOLES



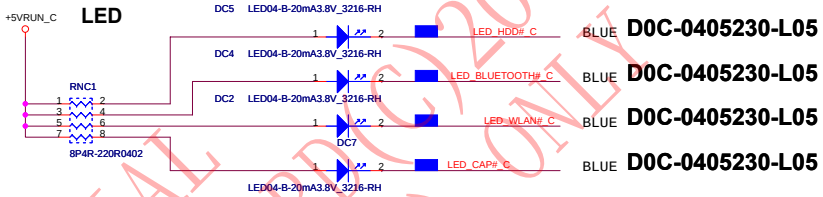
2010/01/25 Add location holes for ME



N5A-16F0110-A81

2010/01/15 Change pin define to 16 pin

2010/01/05 remove HDD signal MOSFET

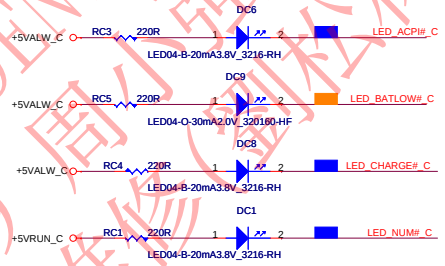


BLUE **D0C-0405230-L05**

BLUE **D0C-0405230-L05**

BLUE **D0C-0405230-L05**

BLUE **D0C-0405230-L05**



BLUE **D0C-0405230-L05**

ORANG **D0C-0409300-L05**

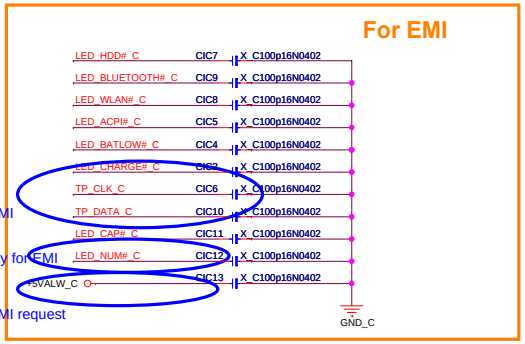
BLUE **D0C-0405230-L05**

BLUE **D0C-0405230-L05**

2010/01/26 reserve for EMI

2010/01/27 reserve LED capacity for EMI

2010/02/01 reserve for EMI request

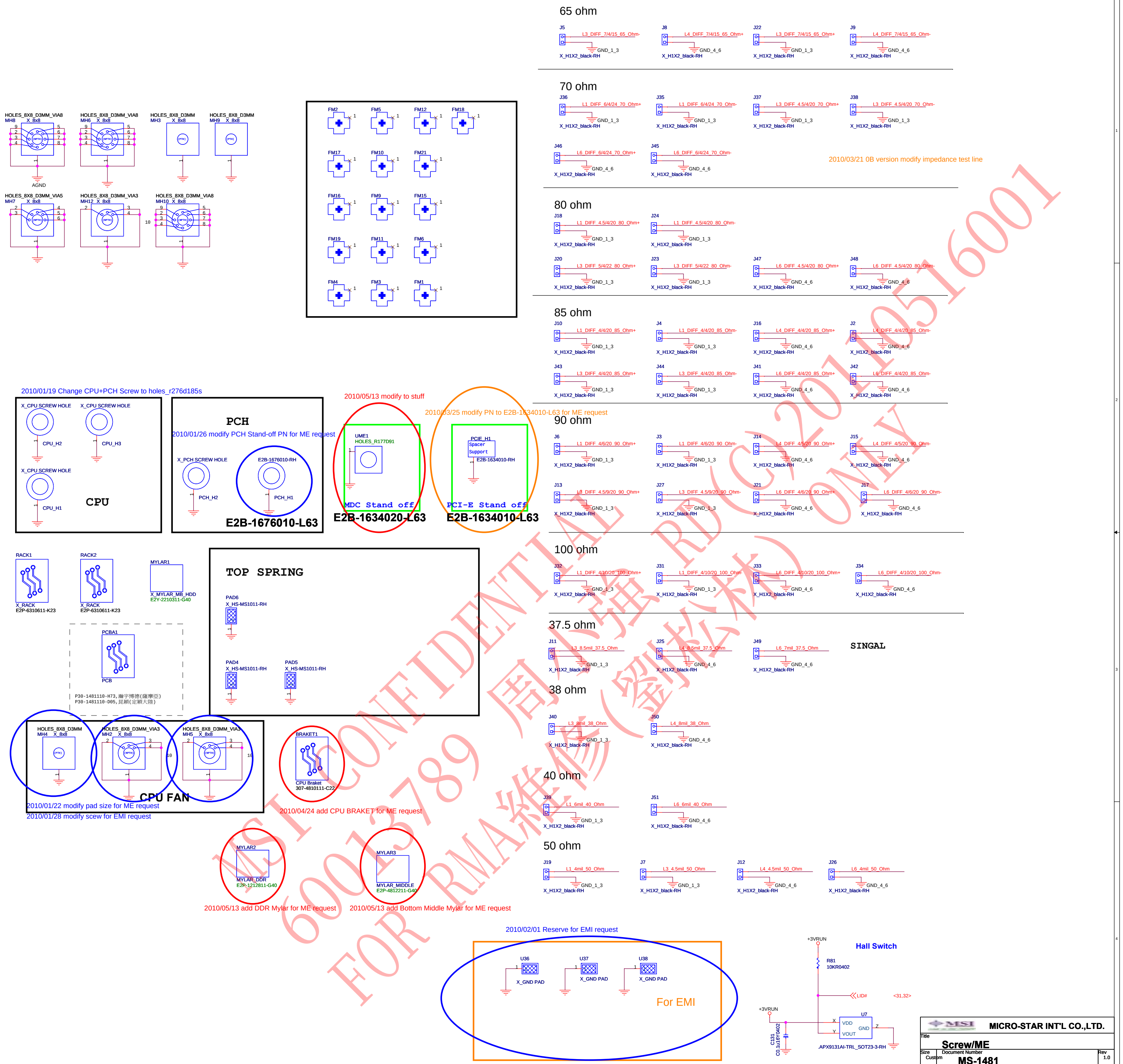


MSI MICRO-STAR INT'L CO.,LTD.

Title: TP,LEDBOARD

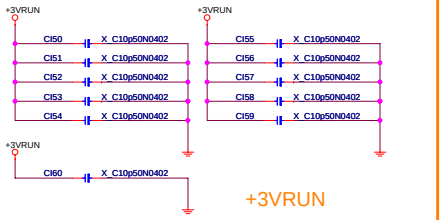
Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 47 of 56

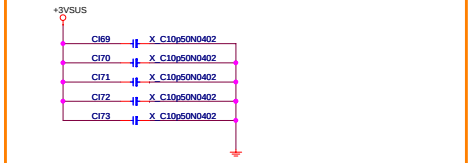

65 ohm
70 ohm
2010/03/21 0B version modify impedance test line
80 ohm
85 ohm
90 ohm
100 ohm
37.5 ohm
SINGAL
38 ohm
40 ohm
50 ohm
2010/01/19 Change CPU+PCH Screw to holes_r276d185s
CPU
PCH
2010/01/26 modify PCH Stand-off PN for ME request
E2B-1676010-L63
2010/05/13 modify to stuff
MDC Stand off
E2B-1634020-L63
2010/03/25 modify PN to E2B-1634010-L63 for ME request
PCI-E Stand off
E2B-1634010-L63
TOP SPRING
CPU FAN
2010/01/22 modify pad size for ME request
2010/01/28 modify scew for EMI request
2010/04/24 add CPU BRAKET for ME request
2010/05/13 add DDR Mylar for ME request
2010/05/13 add Bottom Middle Mylar for ME request
2010/02/01 Reserve for EMI request
For EMI
Hall Switch

MICRO-STAR INT'L CO.,LTD.

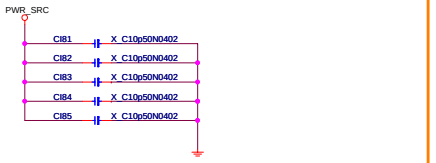
Title	Screw/ME	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 48 of 56	



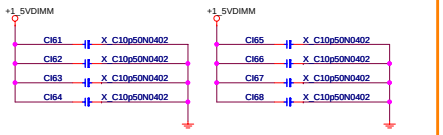
+3VRUN



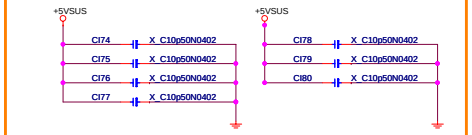
+3VSUS



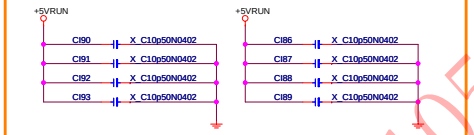
PWR_SRC



+1_5VDIMM

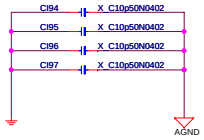


+5VSUS



+5VRUN

2010/02/01 Reserve power by pass capacity for EMI request



GND to AGND

MICRO-STAR INT'L CO.,LTD.

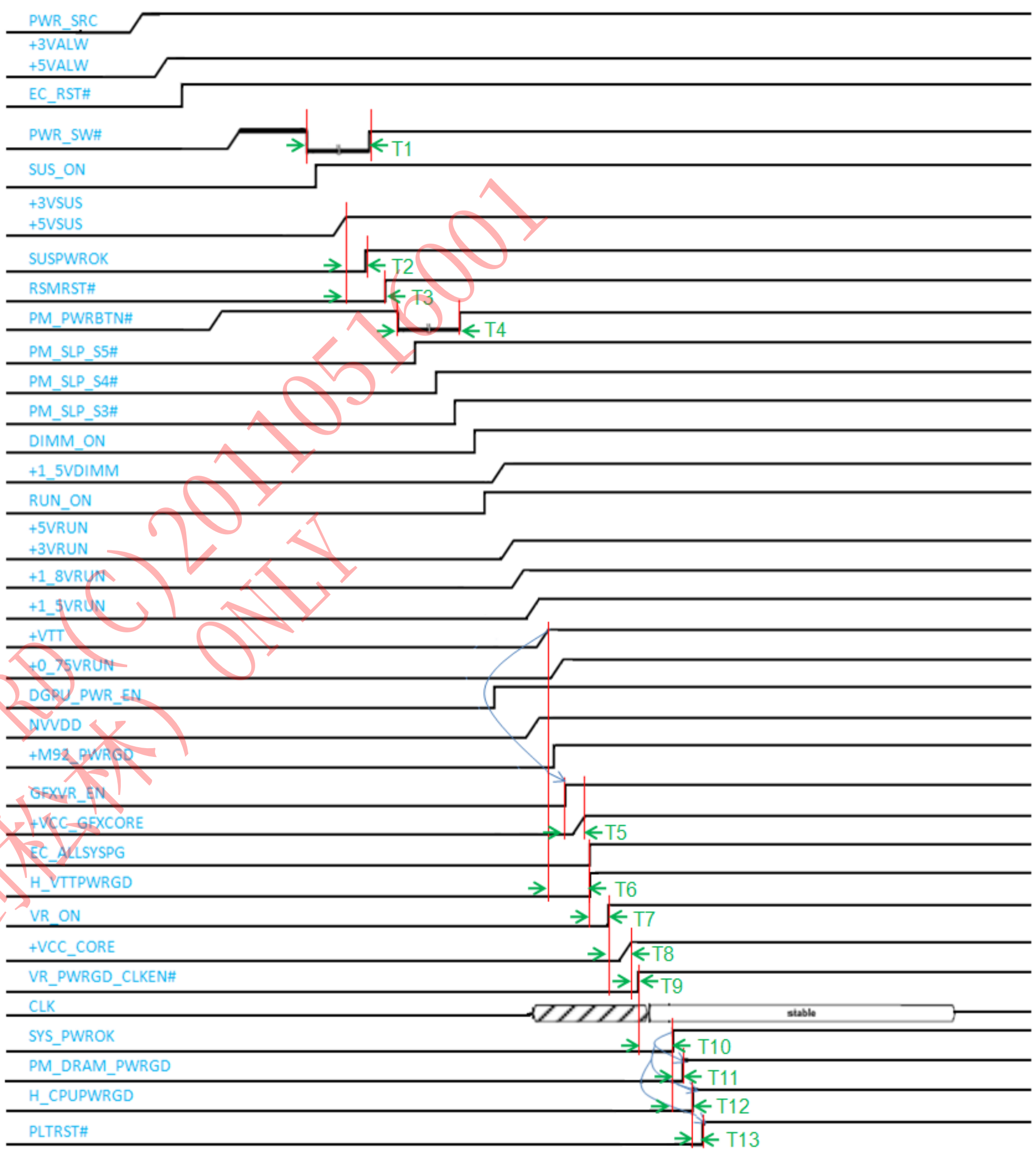
Title: EMI

Size: Custom | Document Number: MS-1481 | Rev: 1.0

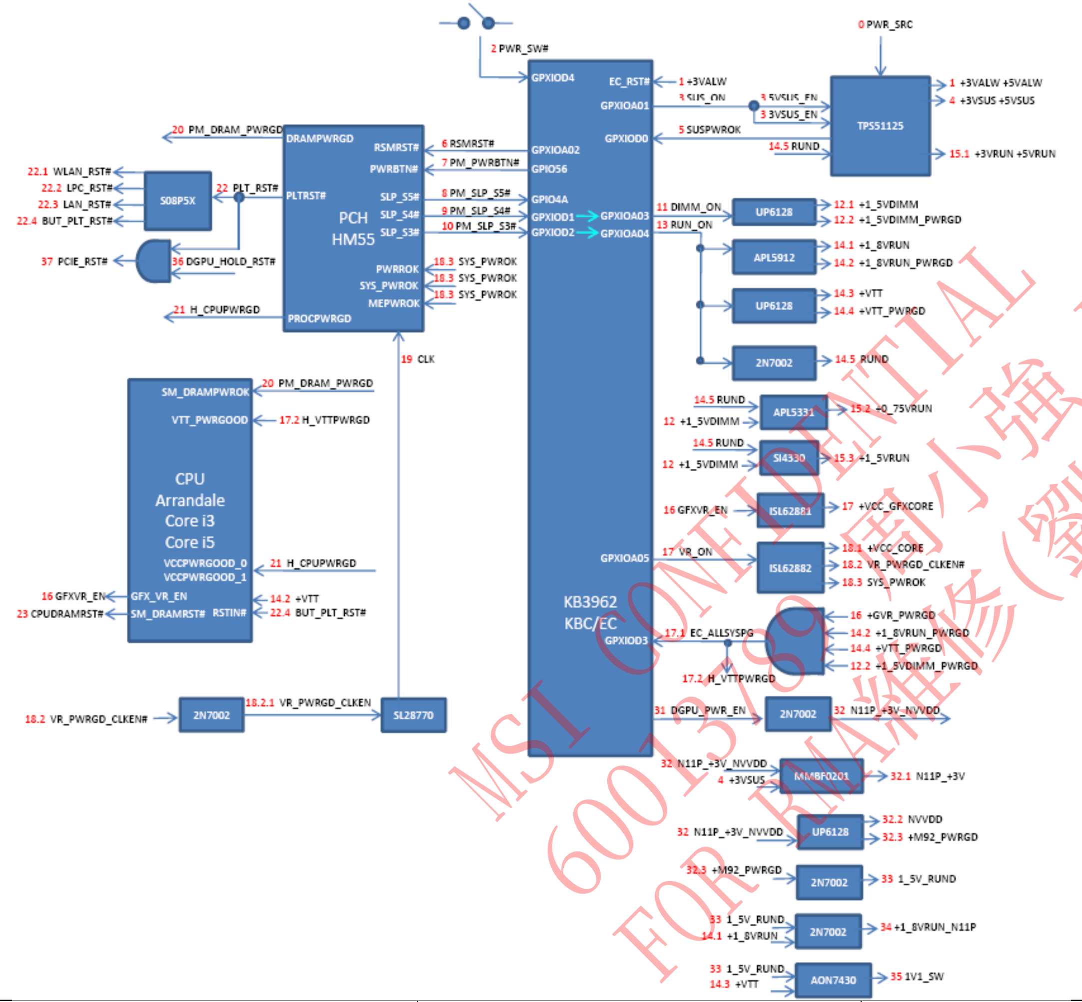
Date: Thursday, May 13, 2010 | Sheet 49 of 56

Label	Min	Max	Units	Description
T1	150		ms	
T2	2	2.5	ms	The powergood function is activated with 2 ms internal delay after SUSPWROK goes high. If the output voltage becomes within +/-5% of the target value, PGOOD goes high around 2.5 ms after SUSPWROK goes high.
T3	10		ms	Vcc_SUS stable to RSMRST# deassertion.
T4	150		ms	
T5		1	us	CPU will drive Gfx_VR_EN when VTT ramps. Gfx_VR_EN to Gfx_VID stable. Timing set by Processor.
T6		500	ms	VTT stable to VTTPWRGOOD assertion to the processor.
T7	99		ms	ALL_SYS_PWRGD assertion to IMVP_VR_EN. This timing is generated by EC.
T8		3	ms	
T9	10	100	us	
T10	3	20	ms	IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
T11	1		ms	SYS_PWROK/PCH_PWROK assertion to DRAMPWROK assertion. Timing set by PCH.
T12	1		ms	SYS_PWROK/PCH_PWROK assertion to VCCPWRGOOD0/VCCPWRGOOD_1 assertion. Timing set by PCH.
T13	1		ms	VCCPWRGOOD_0/VCCPWRGOOD_1 assertion to PLTRST# deassertion

Calpella System Power on Sequence DC mode



PWR_SRC
+3VALW
+5VALW
EC_RST#
PWR_SW#
T1
SUS_ON
+3VSUS
+5VSUS
SUSPWROK
T2
RSMRST#
T3
PM_PWRBTN#
T4
PM_SLP_S5#
PM_SLP_S4#
PM_SLP_S3#
DIMM_ON
+1_5VDIMM
RUN_ON
+5VRUN
+3VRUN
+1_8VRUN
+1_5VRUN
+VTT
+0_75VRUN
DGPU_PWR_EN
NVVDD
+M92_PWRGD
GFXVR_EN
+VCC_GFXCORE
T5
EC_ALLSYSPG
H_VTTPWRGD
T6
VR_ON
T7
+VCC_CORE
T8
VR_PWRGD_CLKEN#
T9
CLK
stable
SYS_PWROK
T10
PM_DRAM_PWRGD
T11
H_CPUPWRGD
T12
PLTRST#
T13



2 PWR_SW#
0 PWR_SRC
GPXIOD4
EC_RST#
GPXIOA01
GPXIOD0
GPXIOA02
GPIO56
GPIO4A
GPXIOD1
GPXIOD2
GPXIOA03
GPXIOA04
GPXIOA05
GPXIOD3
KB3962
KBC/EC
TPS51125
1 +3VALW
3 SUS_ON
3 5VSUS_EN
3 3VSUS_EN
5 SUSPWROK
14.5 RUND
1 +3VALW +5VALW
4 +3VSUS +5VSUS
15.1 +3VRUN +5VRUN
20 PM_DRAM_PWRGD
DRAMPWRGD
RSMRST#
PWRBTN#
PLTRST#
SLP_S5#
SLP_S4#
SLP_S3#
PCH
HM55
PWROK
SYS_PWROK
MEPWROK
PROCPWRGD
6 RSMRST#
7 PM_PWRBTN#
8 PM_SLP_S5#
9 PM_SLP_S4#
10 PM_SLP_S3#
18.3 SYS_PWROK
19 CLK
21 H_CPUPWRGD
22 PLT_RST#
S08P5X
22.1 WLAN_RST#
22.2 LPC_RST#
22.3 LAN_RST#
22.4 BUT_PLT_RST#
37 PCIE_RST#
36 DGPU_HOLD_RST#
11 DIMM_ON
13 RUN_ON
UP6128
12.1 +1_5VDIMM
12.2 +1_5VDIMM_PWRGD
APL5912
14.1 +1_8VRUN
14.2 +1_8VRUN_PWRGD
14.3 +VTT
14.4 +VTT_PWRGD
2N7002
14.5 RUND
APL5331
15.2 +0_75VRUN
SI4330
15.3 +1_5VRUN
12 +1_5VDIMM
16 GFXVR_EN
ISL62881
17 +VCC_GFXCORE
17 VR_ON
ISL62882
18.1 +VCC_CORE
18.2 VR_PWRGD_CLKEN#
16 +GVR_PWRGD
17.1 EC_ALLSYSPG
17.2 H_VTTPWRGD
31 DGPU_PWR_EN
32 N11P_+3V_NVVDD
MMBF0201
4 +3VSUS
32.1 N11P_+3V
32.2 NVVDD
32.3 +M92_PWRGD
33 1_5V_RUND
34 +1_8VRUN_N11P
AON7430
35 1V1_SW
SM_DRAMPWROK
VTT_PWRGOOD
17.2 H_VTTPWRGD
CPU
Arrandale
Core i3
Core i5
VCCPWRGOOD_0
VCCPWRGOOD_1
GFX_VR_EN
SM_DRAMRST#
RSTIN#
16 GFXVR_EN
23 CPUDRAMRST#
14.2 +VTT
22.4 BUT_PLT_RST#
18.2 VR_PWRGD_CLKEN#
18.2.1 VR_PWRGD_CLKEN
SL28770

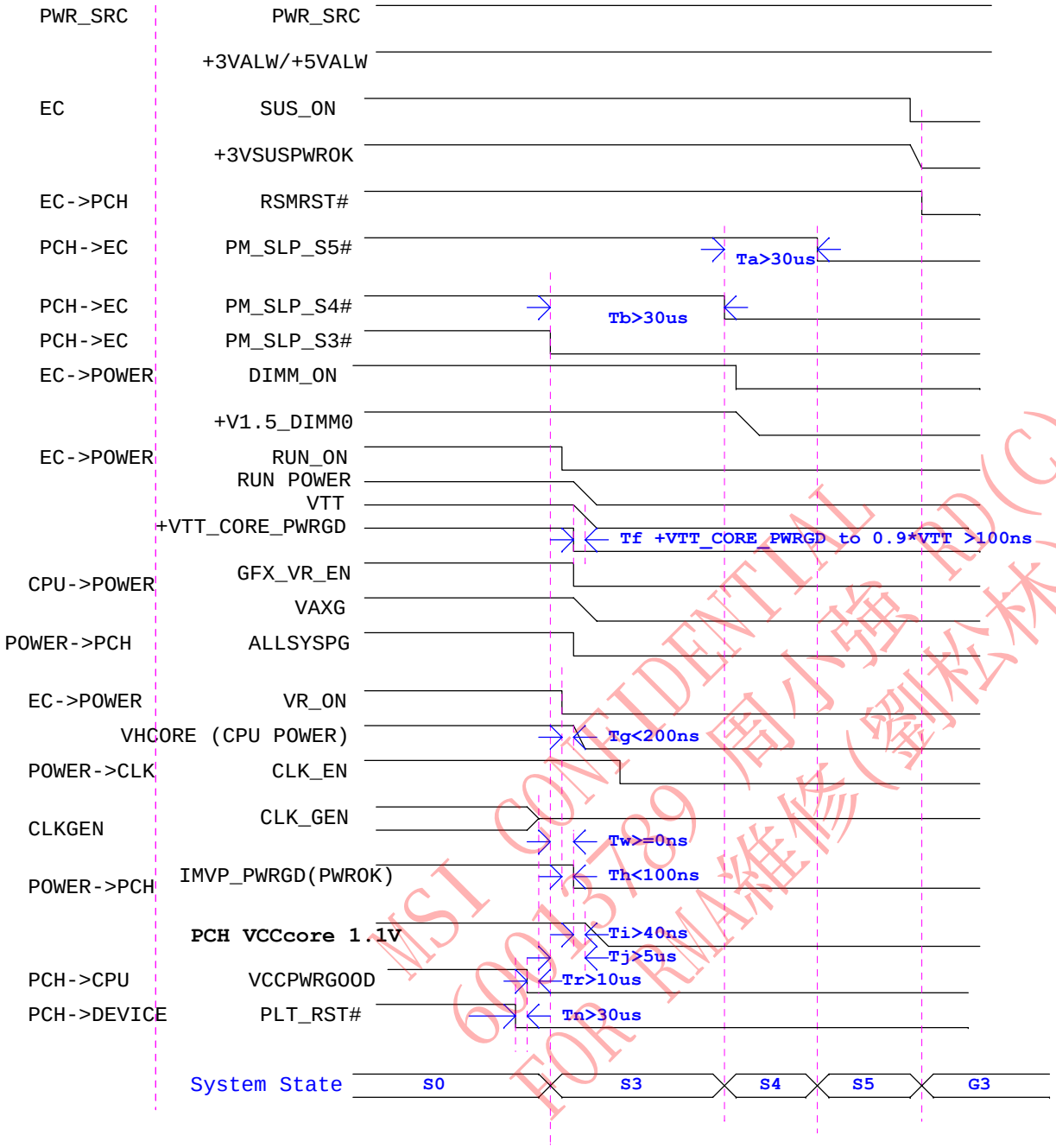
MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequency

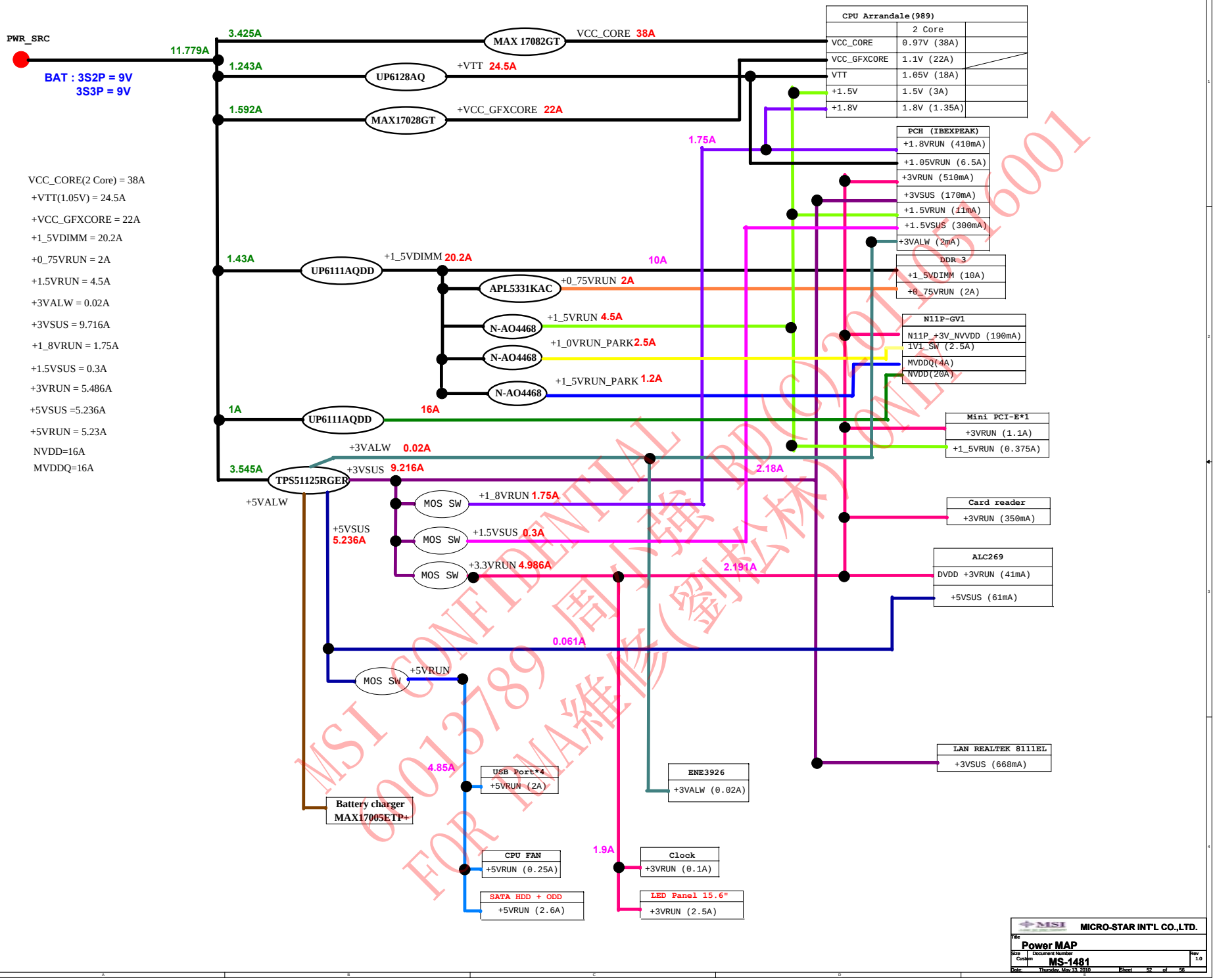
Size: Custom | Document Number: MS-1481 | Rev: 1.0

Date: Thursday, May 13, 2010 | Sheet 50 of 56

Power down Sequence DC mode S0 to G3



MSI	MICRO-STAR INT'L CO.,LTD.	
Title: Power on Sequency		
Size: A3	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 51 of 56	



MICRO-STAR INT'L CO.,LTD.

Power MAP

MS-1481

Rev 1.0

Thursday, May 13, 2010

Sheet 52 of 56

0A NOTE

2009/12/25

1.Change Aduio codec form ALC 888 to ALC 269
2.Change LAN Chip from RTL 8111DL to RTL 8111EL

2009/12/29

1.For Power team request change the power page(P.38~P.43) to same the 16G1
2. Page 21 For Layout request reversal the PCH Azialia arry resistor sequency
3. Page 22 For Layout request reversal the PCH SMbus arry resistor sequency
4. Page 5 Remove PROCHOT# line, Add test point
5. Page 45 ADD VOL+_SW,VOL-_SW,EC0_SW,HIQ_SW,TURBO_SW

2009/12/30

1.For Card reader ENE suggestion add 4.7K ohm pull hi to 3V
2. P40,P41,P43 delete Nvidia Venthura power desgin

2009/12/31

1. Page 38 Change power connector

2010/01/03

1. Page 46 Add TP board
2. Page 12, 13 modify off page symbol
3. Page 35 follow reference schematic remover 3 capacity

2010/01/04

1. Page 35 follow reference schematic add 10K pull low
2. Page 44 Remove NV I/O 1.8V
3. Page 45 follow ENE suggestion change the capacity to 20P

2010/01/05

1. Page 3 Change decoupling capacity from X5R to X7R
2. Page 31 Add CRT HSYNC &VSYN level shift
3. Page 47 remove HDD LED MOSFET

2010/01/07

1. Page 38 For EMI request change capacity from 22p to 10p

2010/01/08

1. Page 43 For OC reserve adjust voltage schemaitc
2. Page 44 For OC reserve adjust voltage schemaitc

2010/01/12

1.Page 38 follow Realtek suggestion modify PD# schematic
2.Page 39 Remove power schematic for power team request
3.Page 40 Chagne R1230 from 174K(0603) to 178K(0402) for power team request
4.Page 38 remove OD schematic for Realtek suggestion
5.Page 38 Add and change pull hi resistor to 4.7K
6.Page 38 Change power connector same the 16G1

2010/01/13

1.Page 32 Change keyboard Connector for 87 Keys
2.Page 33 Change ESATA CONN PN

2010/01/14

1.Page 47 Change TP Pin define for multi finger
2.Page 42 reserve GFX VID pull & low resistor
3.Page 11 Nvidia Recommand R200 isn't stuff
4.Page 12 Change pull low resistor value form 1% to 5%
5.Page 13 Change pull low resistor value form 1% to 5%
6.Page 18 Change pull low resistor value form 1% to 5%
7.Page 19 Change pull low resistor value form 1% to 5%
8.Page 19 Nvidia recommend change R103 & R104 value from 10K to 2,2K ohm
9.Page 19 Nvidia recommend reserve I2CS for thermal sensor
10.Page 40 For adjust power sequence modify schematic

2010/01/15

1.Page 9.10 Change reserve capacity value form 2.2uF to 10uF
2.Page 9.10 Remove the x-copper, add verf_ca resistor 10K*2

2010/01/18

1.Page 19 Add reserve pull hi and pull low resistor for Nvidia recommend
2.Page 32 & 46 Change Connector from 16 pin to 14 pin

2010/01/19

1.Page 36 Fro EMI request change reserve capacity location
2.Page 39 Fro power team request swap the MOSFET location
3.Page 32 Change the smith trigger unit at schematic
4.Page 43 Change smith trigger part reference
5.Page 34 Reserve Level shift IC pin 38 add 2.2K pull low
6.Page 48 Change CPU+PCH Screw to holes_r276d185s

2010/01/20

1.Page 33 For Me request change H.D.D connector P/N
2.Page 19 Add GPIO 5 & 6 Pull hi & Pull low resistor for Nvidia request
3.Page 48 Change PCH-Stand-off PN E2B-1431010-L63

2010/01/21

1.Page 07 Change 0R to X-copper
2.Page 08 Change 0R to X-copper
3.Page 9 Stuff C77 & Stuff Vref CA resister
4.Page 9 Stuff C52 & Stuff Vref CA resister
5.Page 11 Change C155,C256,C272,C196,C268 to no stuff
6.Page 12 Change C413 to no stuff and Add C572
7.Page 18 Change C166,C173,C470 to no stuff
8.Page 21 remove resistor to TP point save for layout space
9.Page 31 Change Pin define and remove reserve component for layout space save and save cost (common used 1471 LVDS cable)
10.Page 24 used LVDS cable same the 1471,can save other LVDS write
11.Page 38 Add capacity for voltage stable
12.Page 33 Remove component to save layout space

2010/01/22

1.Page 35 Add Q33,R45,C573,U35 for LAN ECO
2.Page 11 Change 0R to x-copper tosave component
3.Page 32 Change array capacity to save layout space
4.Page 46 For ID request Add LED *4
5.Page 41 For power team request modify capacity value from 470uF t0 68uF
6.Page 45 modify screw size for ME
7.Page 23 modify resistor 1K to 10K
8.Page 31 modify R369,R359 to stuff
9.Page 24 remove component to save layout space
10.Page 40 Reserve capacity for fine tune timing
11.Page 30 modify FSA pull high to 10KR
12.Page 30 modify Crystal(Y6) for ME height limit
13.Page 32 Key board follow 1471 pin define

2010/01/25

1.Page 32 Rechange array capacity to capacity
2.Page 45 Add location holes for ME
3.Page 46 Add location holes for ME
4.Page 47 Add location holes for ME
5.Page 21 BIOS PN pending change to M31-25L3203-M24
6.Page 13 Resistor PN peding change to R11-402AT12-W08
7.Page 19 Resistor PN peding Change to R11-402AT12-W08
8.Page 28 Bead PN pending change to L01-1006084-T19
9.Page 48 For EMI suggestion change MH8 GND to AGND

2010/01/26

1.Page 48 modify stand-off for ME request
2.Page 12 reserve pull hi resister for Nvidia request
3.Page 13 reserve pull hi resister for Nvidia request
4.Page 47 Add TP CLK & DATA pull hi resistor
4.Page 37 for ME request modify the MDC connecotr PN

2010/01/27

1.Page 48 modify stand-off for ME request
2.Page 25 for layout request swap RN6 pin define
3.Page 37 & 45 connector pin define
4.Page 47 reserve capacity for EMI request

2010/01/28

1.Page 48 modify screw for EMI request

2010/01/29

1.Page 34 Add resistor for TI suggestion

2010/02/01

1.Page 47 Swap TP connector pin define for ME cable
2.Page 45 no stuff USB EMI common choke
3.Page 37 no stuff USB EMI common choke
4.Page 45 Reserve capacity for EMI request
5.Page 47 Reserve capacity for EMI request
6.Page 47 Reserve capacity for EMI request
7.Page 49 Reserve power by pass capacity for EMI request
8.Page 48 Reserve GND Pad for EMI request
9.Page 41 For high frequency issue modify 68uF to 100uF

2010/02/02

1.Page 41 Change net and add net name for vendor suggestion
2.Page 41 Reserve 330uF capacity for high frequency issue

2010/02/03

1.Page 37 USB Pin 2 & Pin 3 Pin 2 swap
2.Page 45 Delete USB MEC pin to GND
3.Page 45 Delete USB MEC pin to GND

2010/02/09

Note for 0B CN4,VGA1,CN2,USB1,MICA1,LOUT1 fot 產線製程改爲60階,0B需改回原本階層

Begging to now total adding components :81

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	0A NOTE	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 53 of 56	

2010/02/09

Note 1 CN4,VGA1,CN2,USB1,MICA1,LOUT1 for SMTchange to 60 status,remind 0B version must change to default status

Note 2. remind 0B version msut change 14.318MHz & 25MHz crystal to mainstream source

2010/03/03

1.Page 35 modify CHOKE1 form 2.2uH to 4.7uH for Realtek request

2010/03/07

1.Page 31 Add CRT fuse for safety request

1.Page 38 Change C569,C416,L22,C416,C411 ,C529,C530 t0 stuff

2010/03/11

1.Page 37 modify USB connector PN:N53-04M0580-AF2

2.Page 32 remove TP baord pull hi resistor to mainboad

2010/03/11

1.Page 13 modify R190 value form 60R to 40R for NV suggestion

2.Page 37 for ME modify USB1 Connector PN to N53-04M0580-AF2

2010/03/16

1.Page 19 modify R157,R160 value form 40.2R to 40.2K

2.Page 40 Add NV 1.1V timing delay schematic

2010/03/21

1.Page 18 remove JNCA2 at 0B version

2.Page 18 modify C179 to no stuff at 0B versionn

2010/03/22

1.Page 30 modify Y6 PN:D04-0100900-F07
c load value form 22p to 20p

2010/03/22

1.Page 22 Resever Wimax solution

2.Page 42 Resever for EMI request

2010/03/24

1.Page 39 modify PL1 PN to L04-1007340-M26

2.Page 43 modify PR21 PN to R11-1132T12-W08

3.Page 44 modify PC107 stuff

4.Page 43 modify R265 to stuff

5.Page 44 modify PR105 to 4.75K

6.Page 44 modify PR106 to 1.5K

2010/03/25

1.Page 48 modify Mini PCI-E Solt for ME request

1.Page 48 modify Mini PCI-E Stand off for ME request

2010/03/26

1.Page 42 modify PR 93 value to 4.87K ohm

2.Page 48 modify Mini PCI-E Stand off for ME request

3.Page 35 reserve 0.1uF *4 for EMI

4.Page 35 modify Xcopper to 0R

5.Page 41 modify PR120,Pr128 to 1.82KR

6.Page 41 modify PR125,PR49 to 2.49KR

7.Page 41 modify PR133 to 3.3KR

8.Page 41 modify PR131 to 7.87 KR

9.Page 41 modify PR136 to 63.4KR

10.Page 41 modify PC125 value to 0.068uF

11.Page 40 modify PR10value to 30.9K

12.Page 38 for DEPOP function stuff DEPOP schematic

13.Page 43 modify PR14,PR15 value to 1K

14.Page 46 modify DB4 & DB6 color to Amber
modify DB2,DB3,DB7,DB8 to no stuff for ID request

2010/03/29

1.Page 37 modify USB switch IC to ANPEC

2.Page 45 modify USB switch IC to ANPEC

3.Page 21 remove BIOS socket modify to ROM

4.Page 31 modify L3,L4,L5 to indutor 120nH for EMI suggestion

5.Page 31 modify C92,C104,C108 to stuff

6.Page 46 Add Launch board Mylar for ME

7.Page 47 Add TP board Mylar for ME

2010/03/30

1.Page 36 For EMI request to stuff C100

2.Page 32 For EMI request to stuff KB capacity(CI40、CI48、CI39、CI47、CI38、CI46、CI37、CI45、CI36、CI44、CI35、CI43、CI34、CI42、CI33、CI41)

3.Page 32 For EMI request to stuff ER1 & EC1

4.Page 30 For EMI request to stuff CI8

5.Page 25 For EMI request to stuff CI9,CI10,CI49

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	0B NOTE	
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 54 of 56	

2010/04/08

1.Page 11 For System stable stuff C155 & C272 22uF

2010/04/12

1.Page 05 modify R39 from 0R to xcopper for cost down
2.Page 24 modify R168 & R171 from 0R to xcopper for cost down
3.Page 32 modify R11 for 0R to xcopper from cost down
4.Page 32 modify R2 for 0R to xcopper from cost down
5.Page 32 modify R27 for 0R to xcopper from cost down
6.Page 34 modify R223,R234,R394,,R407,R422 from 0R to xcopper for cost down
7.Page 35 modify R16,R256 for 0R to xcopper from cost down

2010/04/13

1.Page 38 modify R236 from 0R to xcopper for cost down
2.Page 41 modify RR118 ,PR121 from 0R to xcopper for cost down
3.Page 42 modify RR89 from 0R to xcopper for cost down
4.Page 43 modify RR25,R36,R45 from 0R to xcopper for cost down

2010/04/14

1.Page 35 modify R18 from 0R to xcopper for cost down
2.Page 35 modify R8 from 0R to xcopper for cost down
3.Page 36 modify R64 from 0R to xcopper for cost down
4.Page 36 modify R21 from 0R to xcopper for cost down
5.Page 37 modify R259 from 0R to xcopper for cost down
6.Page 41 modify PR2 from 0R to xcopper for cost down
7.Page 35 modify R454 from 0R to xcopper for cost down
8.Page 27 modify R132 from 0R to xcopper for cost down
9.Page 40 remove G1,G3 power gap
10.Page 43 remove G2 power gap

2010/04/24

1.Page 45 stuff LA4,LA5 for EMI request
2.Page 33 stuff L19 for EMI request
3.Page 45 Add Mylar for ME request
4.Page 48 Add CPU BRACKET for ME request

2010/04/30

1.Page 46 modify the launch board connector for ME request
2.Page 44 stuff 6128(VTT) snubber 2.2R+1000P for vendor suggestion
3.Page 44 stuff 6128(NVDD) snubber 2.2R+1000P for vendor suggestion
4.Page 38 modify speaker & mic connector for ME request

2010/05/03

1.Page 32 Fro EMI request stuff CI22,CI23,CI24,CI25,CI26,CI27
2.Page 32 Add CI98,CI99,CI100,CI101,CI102 for EMI request
3.Page 42 Fro EMI request stuff the snubber(PR40,PC51)

2010/05/09

1.Page 43 Fro power IC vendor suggestion to stuff 6128 snubber(1.5VDIMM) PR27,PC39
2.Page 21 modify Y3 from D04-0300220-S35 to D04-0302800-K11 for crystal EOL
3.Page 32 modify Y1 from D04-0300220-S35 to D04-0302800-K11 for crystal EOL

2010/05/10

1.Page 38 For pop noise modify the PD# power source form +5VRUN to +5VSUS
2.Page 34 For TI AP note modify the R446 from 9.1Kr to 2.2KR

2010/05/11

1.Page 34 For MVT version to stuff the HDMI label
2.Page 34 For Q23 damage risk to stuff D6 protection

2010/05/12

1.Page 38 for pop noise modify mute schematic pull hi resister(R424) to no stuff
2.Page 44 remove the PR110 at 1.0 version
3.Page 40 For capacity PN EOL modify the PEC5 & PEC6 PN to C71-2210630-S03

2010/05/13

1.Page 48 for ME request to stuff modem stand off
2.Page 45 add Mylar for ME request(Sponge for CA5)
3.Page 48 add DDR Mylar for ME request
4.Page 48 add bottom_middle Mylar for ME request

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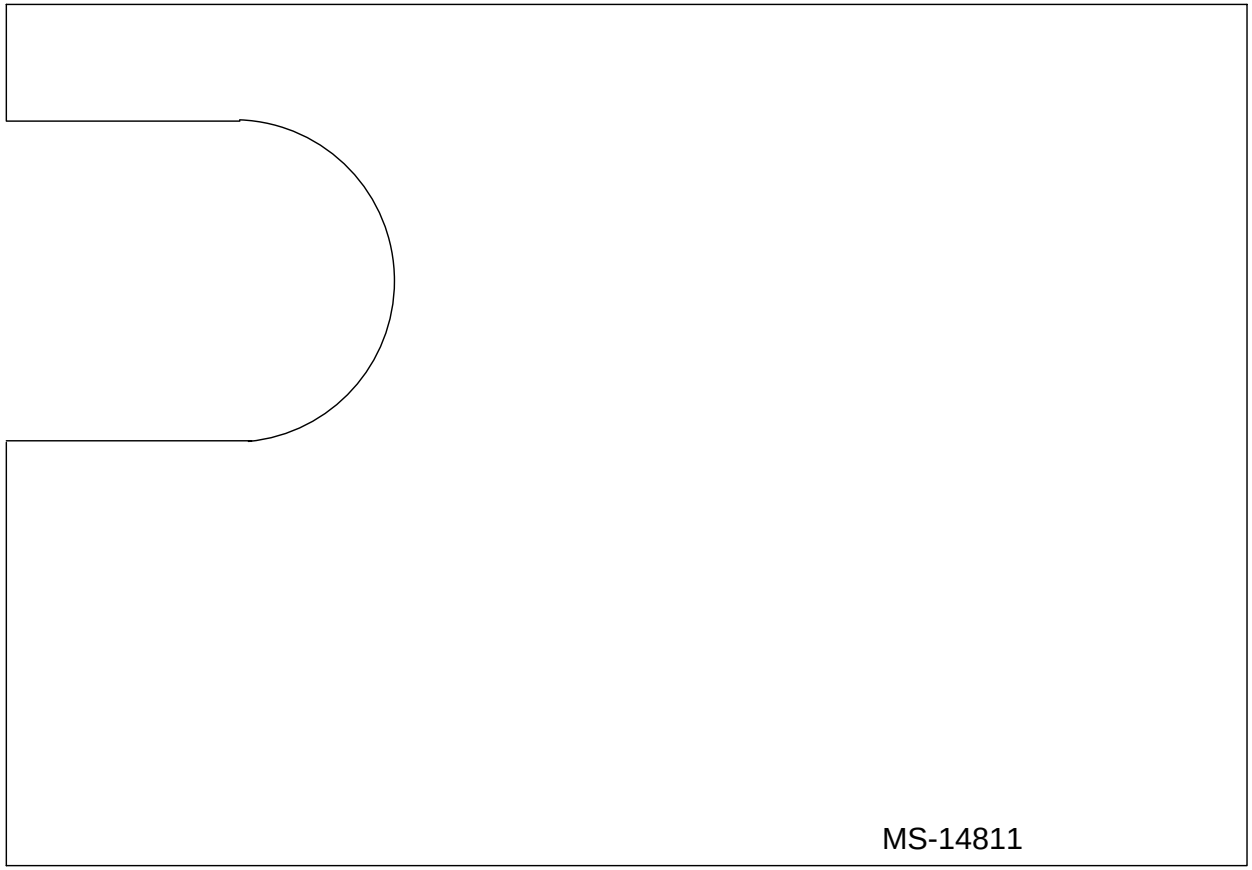
Title: 1.0 NOTE		
Size: Custom	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 55 of 56	

MS-1481B



MS-1481A

MS-1481C

TP

MSI MICRO-STAR INT'L CO.,LTD.		
Title: TOPOLOGY		
Size: B	Document Number: MS-1481	Rev: 1.0
Date: Thursday, May 13, 2010	Sheet 56 of 56	