DELL/COMPAL

MODEL NAME : FDV42

PCB NO : LA-J272P

BOM P/N :

GPIO MAP: X11_CMLH_GPIO map Rev0.4_20190927

PWR Circuit : BHMLK_CMLH_14DSC_X01_PWR_20191022C

Brook Hollow MLK 14 DSC (TBT)

Comet Lake H

2019-10-24

REV : 0.2 (X01)

X76@ :
2GSAMX76@
2GMICRX76@
2GHYNX76@

@ : Nopop Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESD Component
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
VPRO@ : VPRO support
NVPRO@ : non VPRO support
JUMP@ : Jump solder and short
@JUMP@ : Jump no solder
XDP@ : XDP Component
@XDP@
CONN@ : Connector Component
WWAN@ : WWAN Component
WWANRF@ : WWAN RF Component

ESPI@ : eSPI interface
DS3@ : Deep sleep support
NDS3@ : non Deep sleep support
@NDS3@ : non Deep sleep Nopop Component
RTD3@ : RTD3 support
NRTD3@ : non RTD3 support
5107ES@ :
5107NES@ :
2GSAM@
2GMICR@
2GHYN@

MB PCB

Part Number	Description
DAB00063000	PCB 2VW LA-J272P REV0 M/B 1 S

Layout Dell logo

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REV:X00
PWB:

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Title
Cover Sheet

Size	Document Number	Rev
A	*LA-J272P*	0.2

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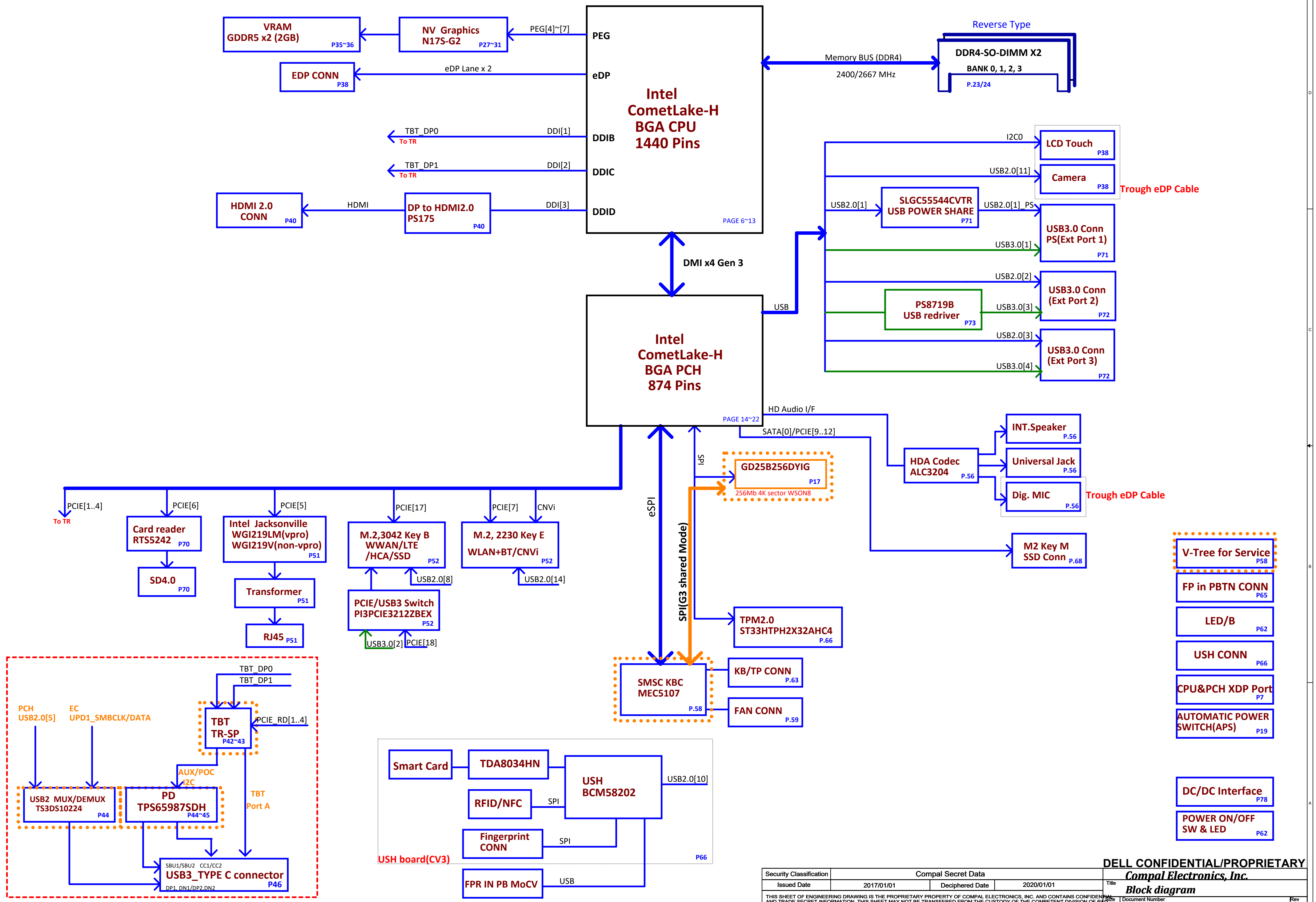
Brook Hollow MLK 14 DSC TBT Block Diagram



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Title *Block diagram*

Size C | Document Number *LA-J272P* | Rev 0.2

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

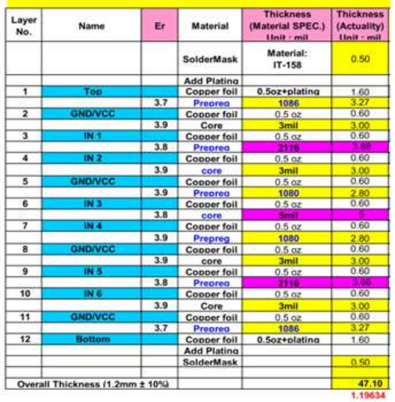
power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->RIGHT
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		Titan Ridge - SP
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		LOM
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-0A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	NA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	
		PCIE-19	SATA-6	NA
		PCIE-20	SATA-7	NA

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 ->LEFT
3	JUSB3-->RIGHT
4	FP IN PB
5	TI PD
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	NA
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO

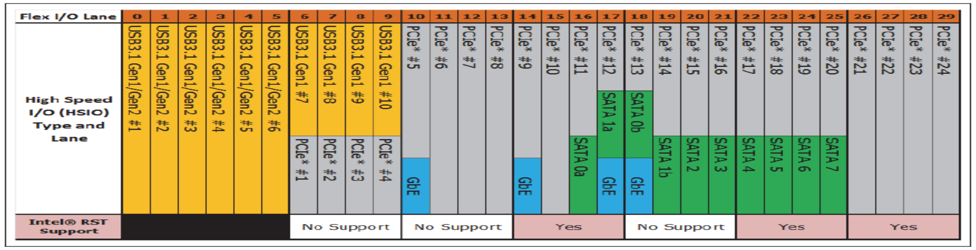
VIDEO	DESTINATION
eDP	LCD
DDI-B	Titan Ridge - SP (Port 0)
DDI-C	Titan Ridge - SP (Port 1)
DDI-D	PS175 --> JHDMI1



Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	Material: IT-158	0.50
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.60
		3.7	Prepreg	1086	3.27
2	GND/VCC		Copper foil	0.5 oz	0.60
		3.9	Core	3mil	3.00
3	IN 1		Copper foil	0.5 oz	0.60
		3.8	Prepreg	2116	3.88
4	IN 2		Copper foil	0.5 oz	0.60
		3.9	core	3mil	3.00
5	GND/VCC		Copper foil	0.5 oz	0.60
		3.9	Prepreg	1080	2.80
6	IN 3		Copper foil	0.5 oz	0.60
		3.8	core	5mil	5
7	IN 4		Copper foil	0.5 oz	0.60
		3.9	Prepreg	1080	2.80
8	GND/VCC		Copper foil	0.5 oz	0.60
		3.9	core	3mil	3.00
9	IN 5		Copper foil	0.5 oz	0.60
		3.8	Prepreg	2116	3.88
10	IN 6		Copper foil	0.5 oz	0.60
		3.9	Core	3mil	3.00
11	GND/VCC		Copper foil	0.5 oz	0.60
		3.7	Prepreg	1086	3.27
12	Bottom		Copper foil	0.5oz+plating	1.60
			Add Plating		
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)					47.10

1.19634

Figure 110. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7 PCIe* #1	USB3.1 Gen1 #8 PCIe* #2	USB3.1 Gen1 #9 PCIe* #3	USB3.1 Gen1 #10 PCIe* #4	PCIe* #5 GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 GbE
Intel® RST Support							No Support				No Support				Yes

Flex I/O Lane	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	PCIe* #10	PCIe* #11 SATA 0a	PCIe* #12 SATA 1a GbE	PCIe* #13 SATA 0b GbE	PCIe* #14 SATA 1b	PCIe* #15 SATA 2	PCIe* #16 SATA 3	PCIe* #17 SATA 4	PCIe* #18 SATA 5	PCIe* #19 SATA 6	PCIe* #20 SATA 7	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support				No Support				Yes				Yes			

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Size A

Document Number ***LA-J272P***

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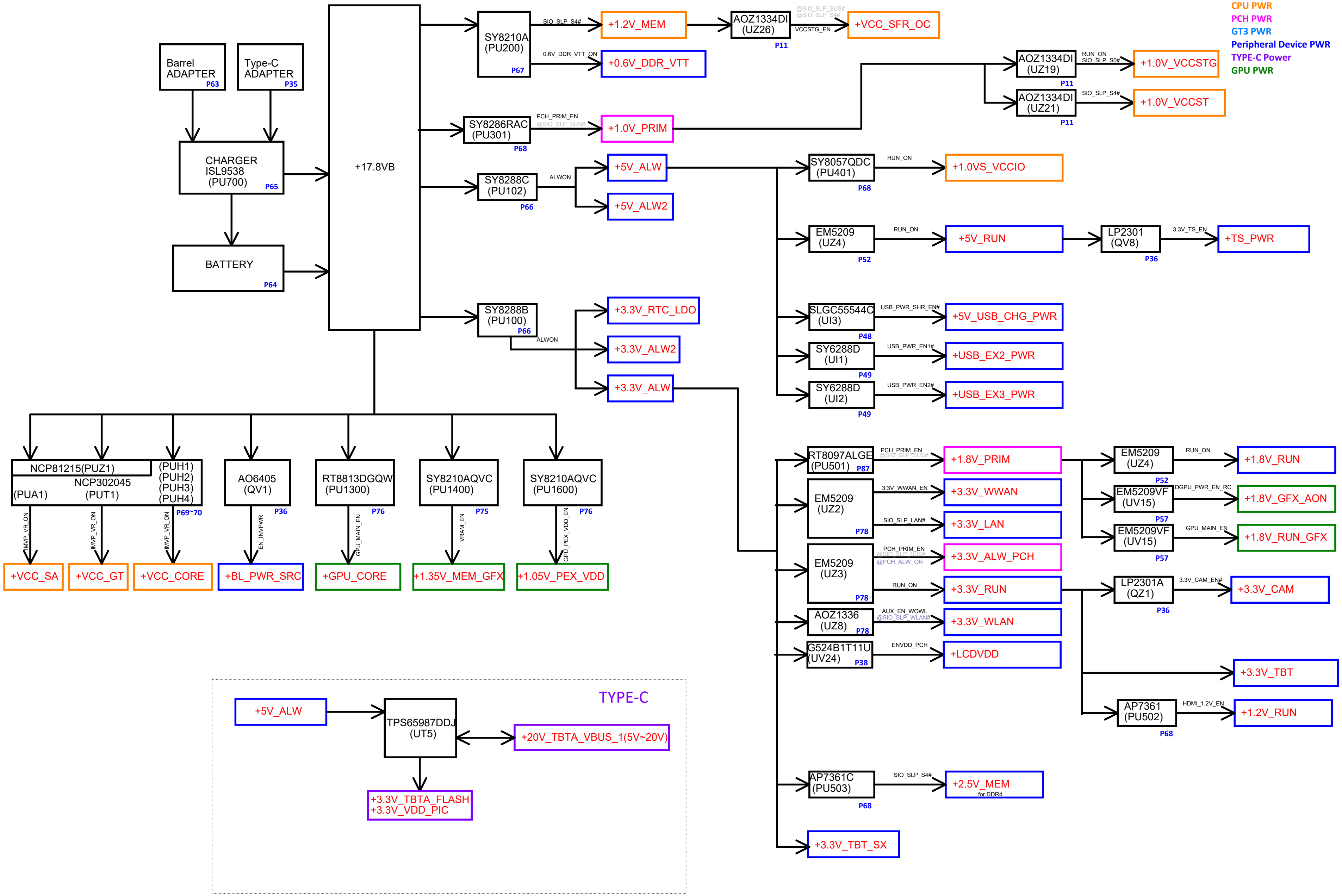

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Size C	Document Number ***LA-J272P***	Rev 0.2
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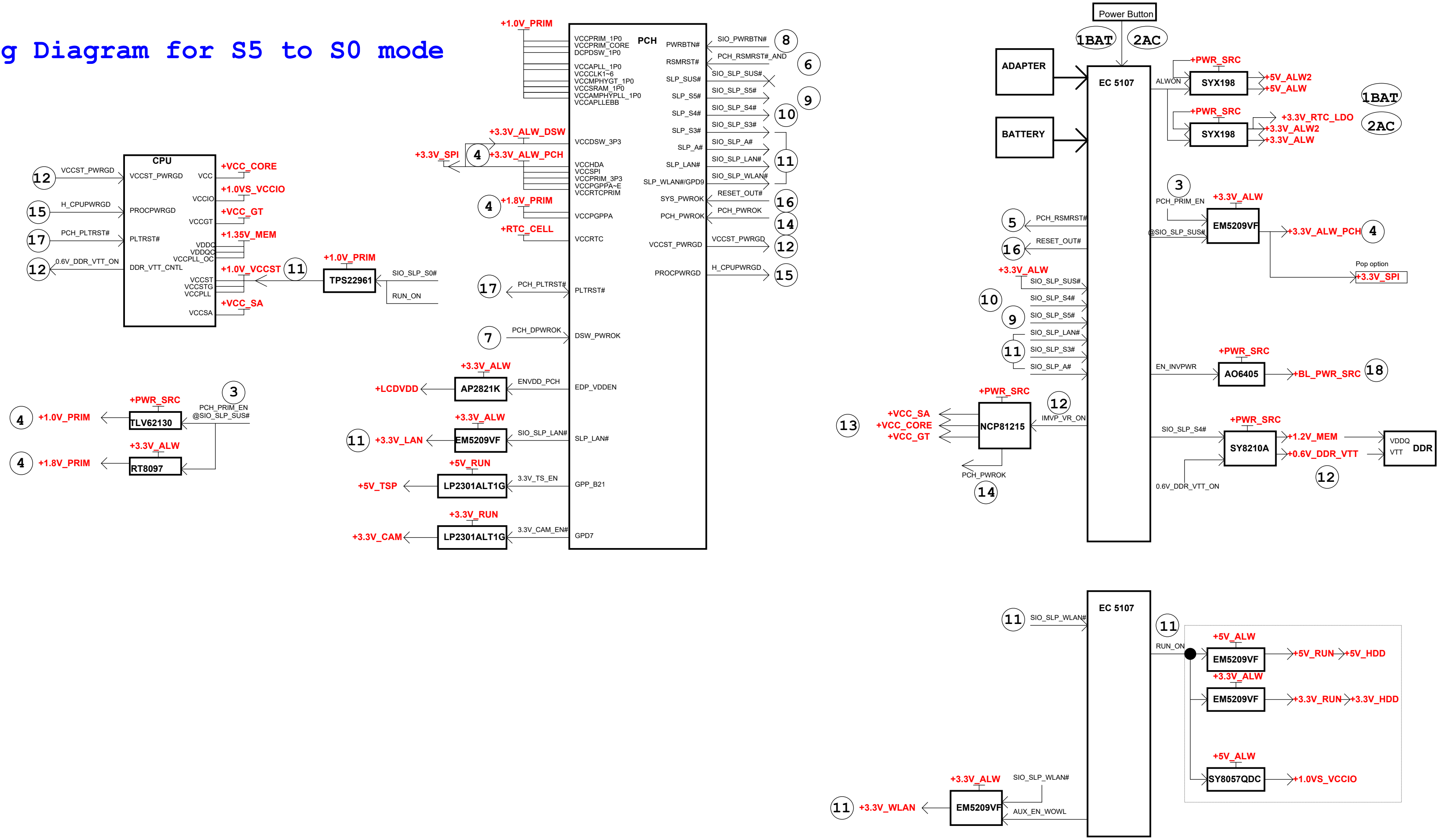
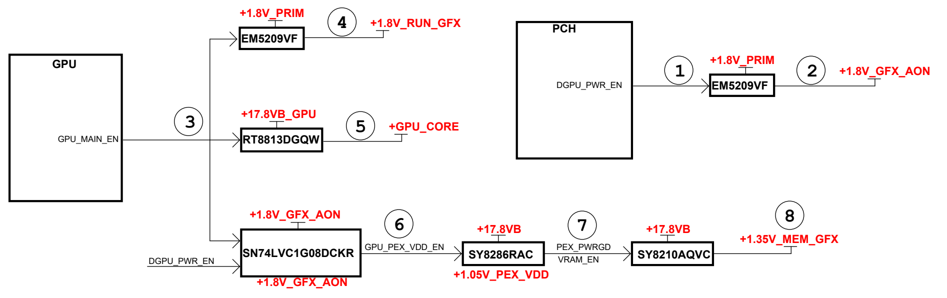
Timing Diagram for S5 to S0 mode



GPU power-on Timing Diagram during win10



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Title *Power Sequence*

Size Custom Document Number *LA-J272P* Rev 0.2

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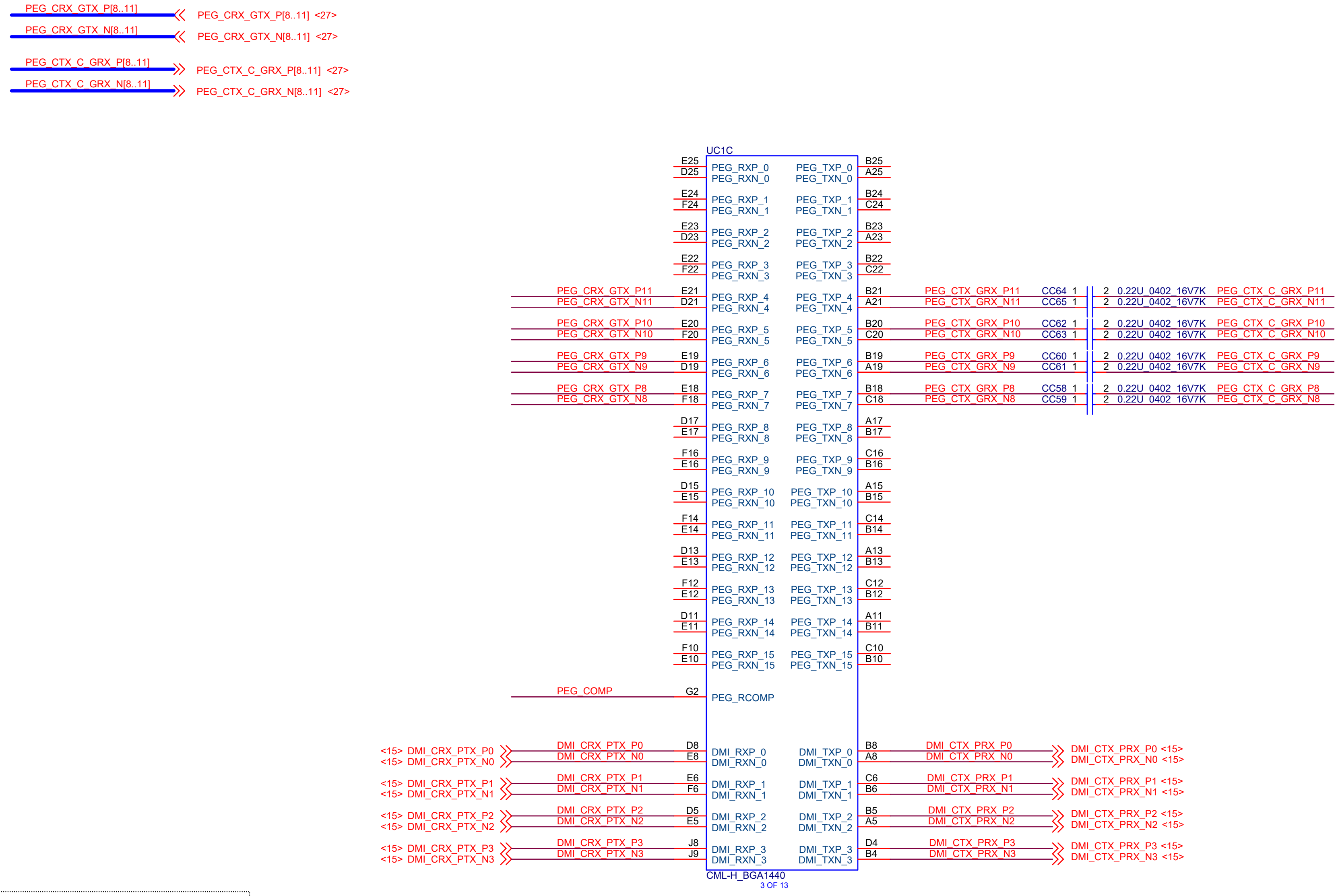

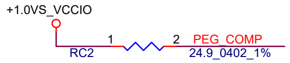

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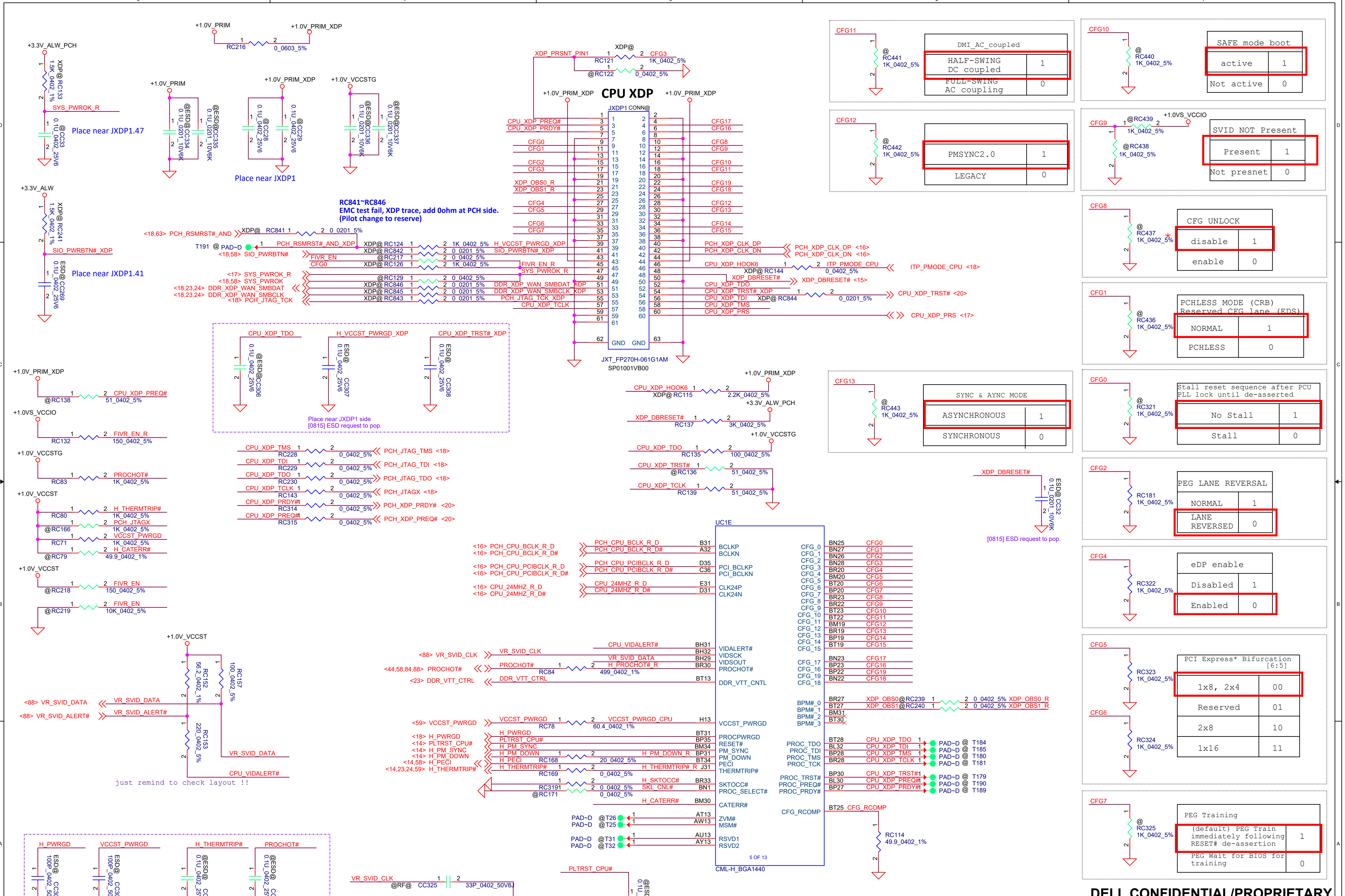

CFG11

DMI_AC_coupled	
HALF-SWING DC coupled	1
FULL-SWING AC coupling	0

CFG12

PMSYNC2.0	1
LEGACY	0

CFG10

SAFE mode boot	
active	1
Not active	0

CFG9

SVID NOT Present	
Present	1
Not presnet	0

CFG8

CFG UNLOCK	
disable	1
enable	0

CFG1

PCHLESS MODE (CRB) Reserved CFG lane (EDS)	
NORMAL	1
PCHLESS	0

CFG13

SYNC & AYNC MODE	
ASYNCHRONOUS	1
SYNCHRONOUS	0

CFG0

Stall reset sequence after PCU PLL lock until de-asserted	
No Stall	1
Stall	0

CFG2

PEG LANE REVERSAL	
NORMAL	1
LANE REVERSED	0

CFG4

eDP enable	
Disabled	1
Enabled	0

CFG5 / CFG6

PCI Express* Bifurcation [6:5]	
1x8, 2x4	00
Reserved	01
2x8	10
1x16	11

CFG7

PEG Training	
(default) PEG Train immediately following RESET# de-assertion	1
PEG Wait for BIOS for training	0

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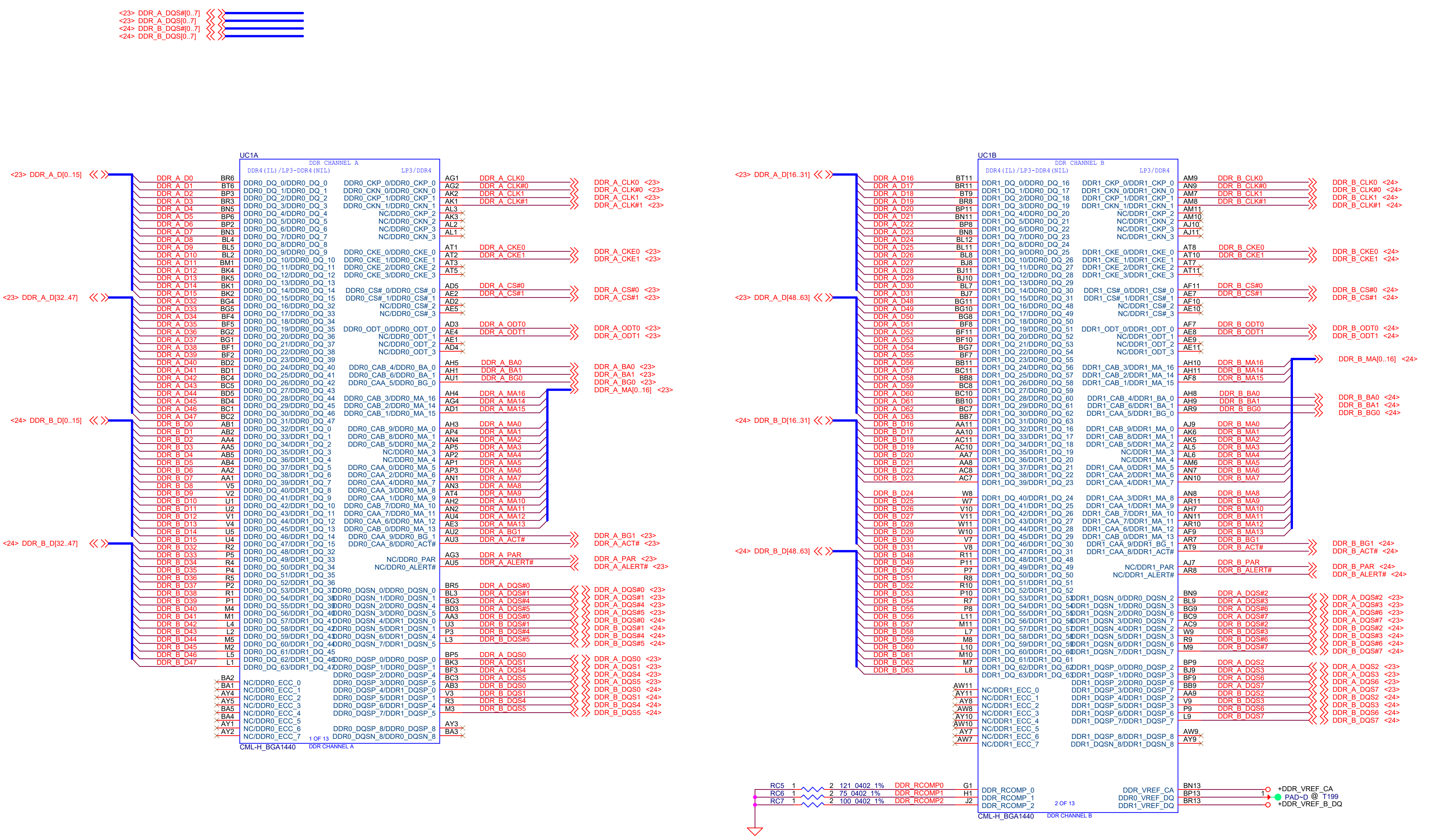

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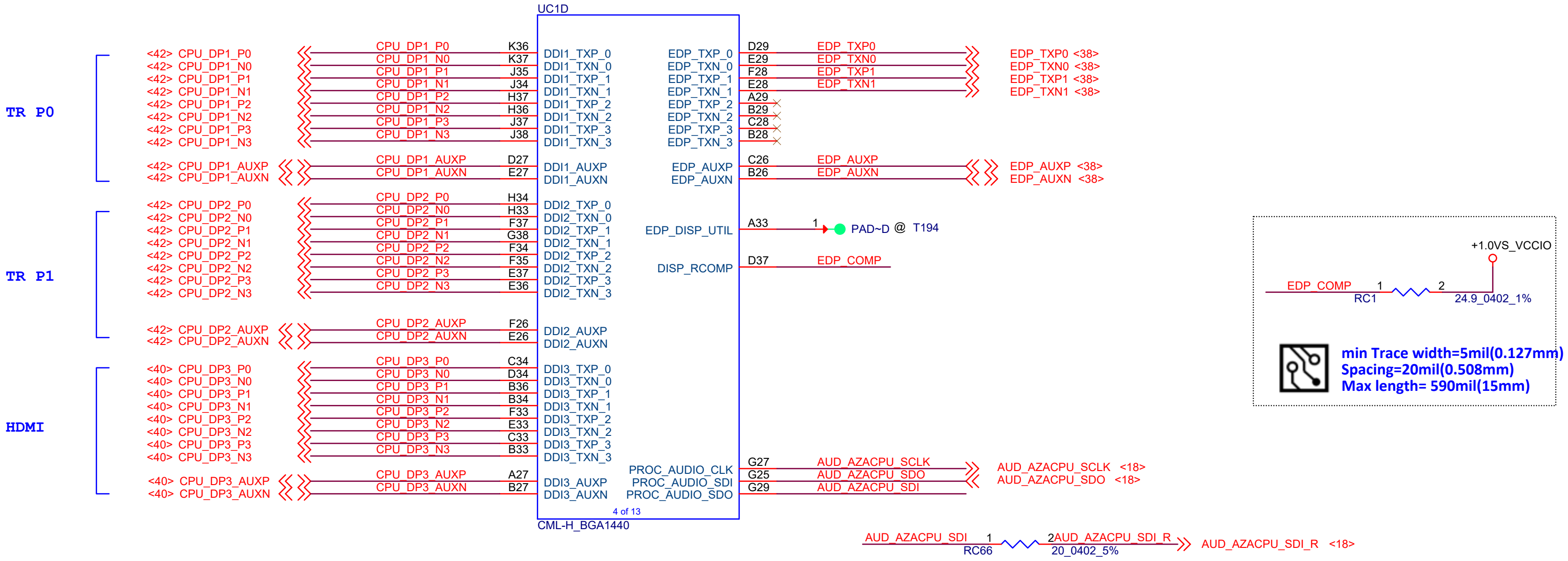

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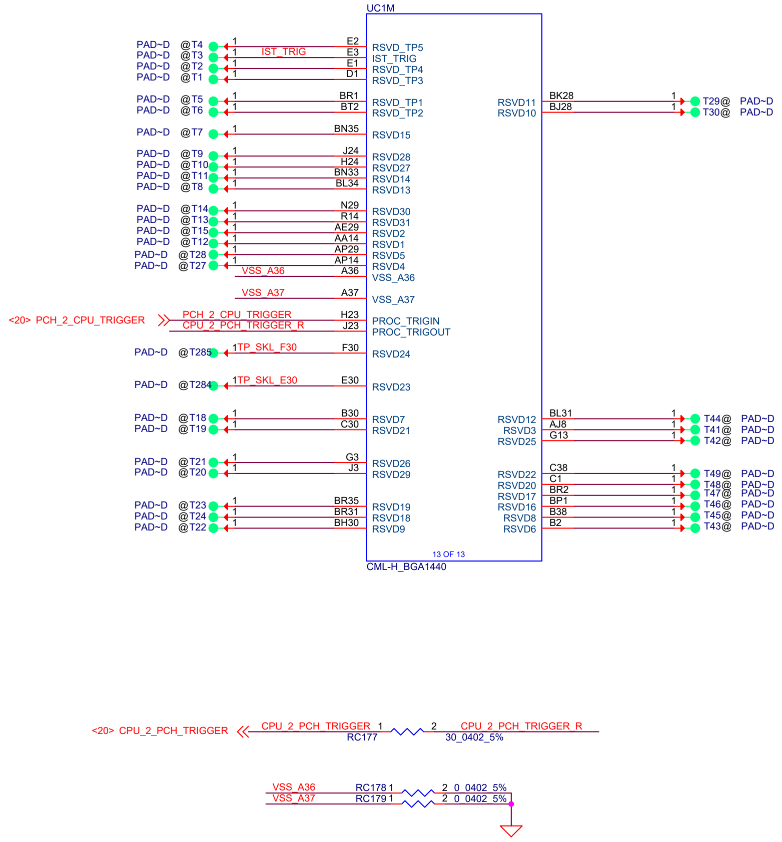

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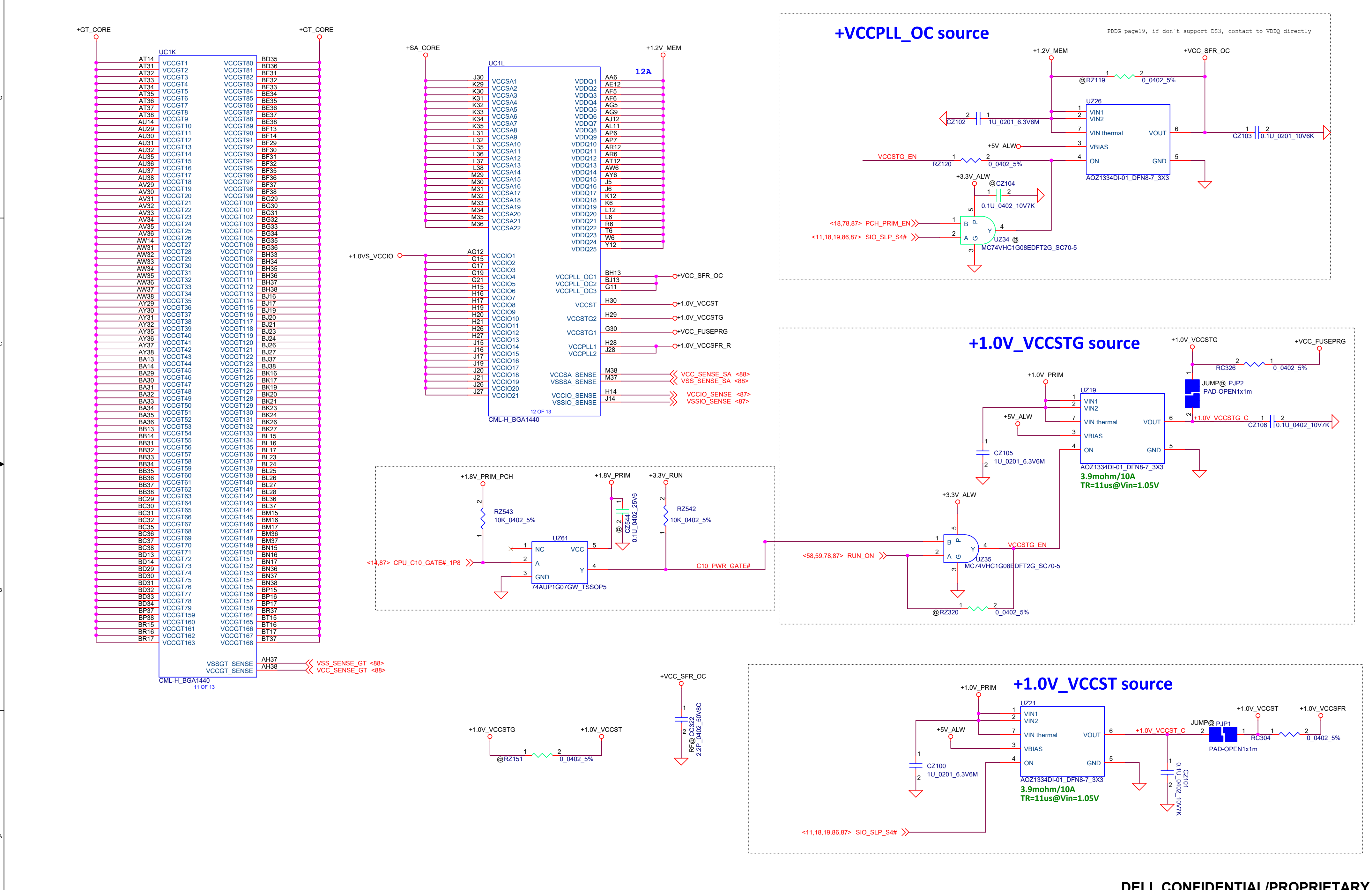

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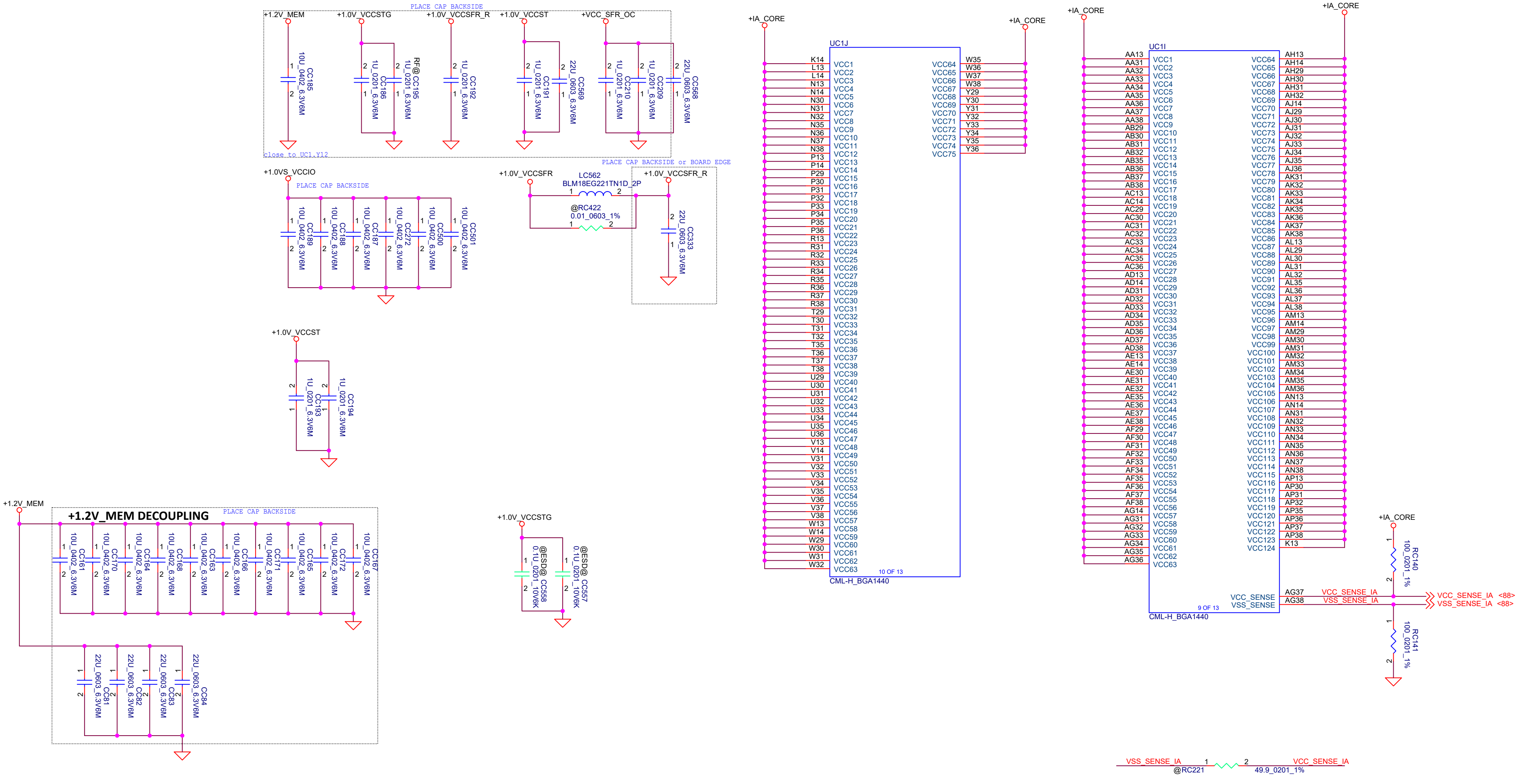
CPU Decoupling CAP Follow 611586_CML_H_PDG_Rev0p7
page. 592 ,593 Table 326. CML H 8+2 Processor Decoupling Requirements



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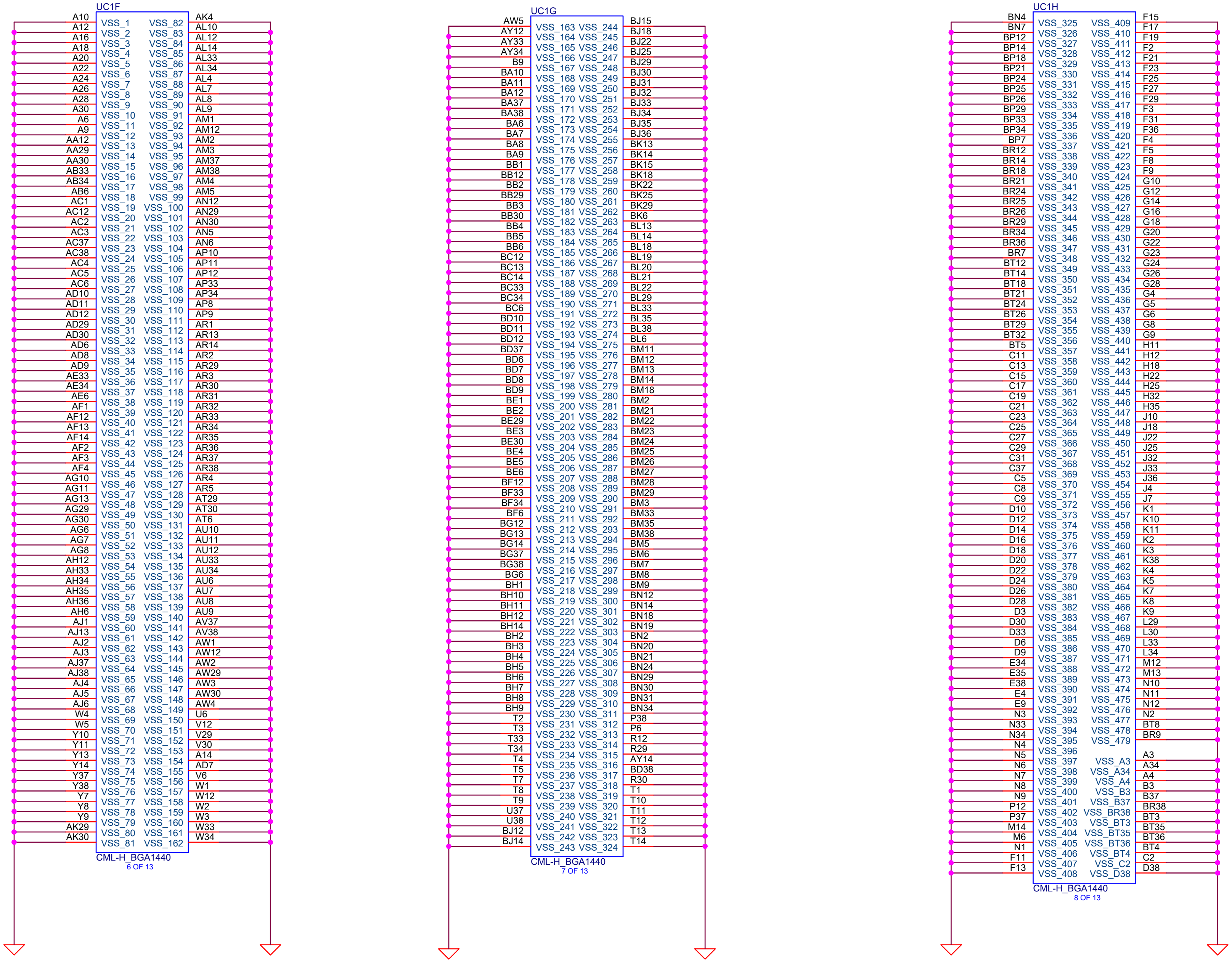

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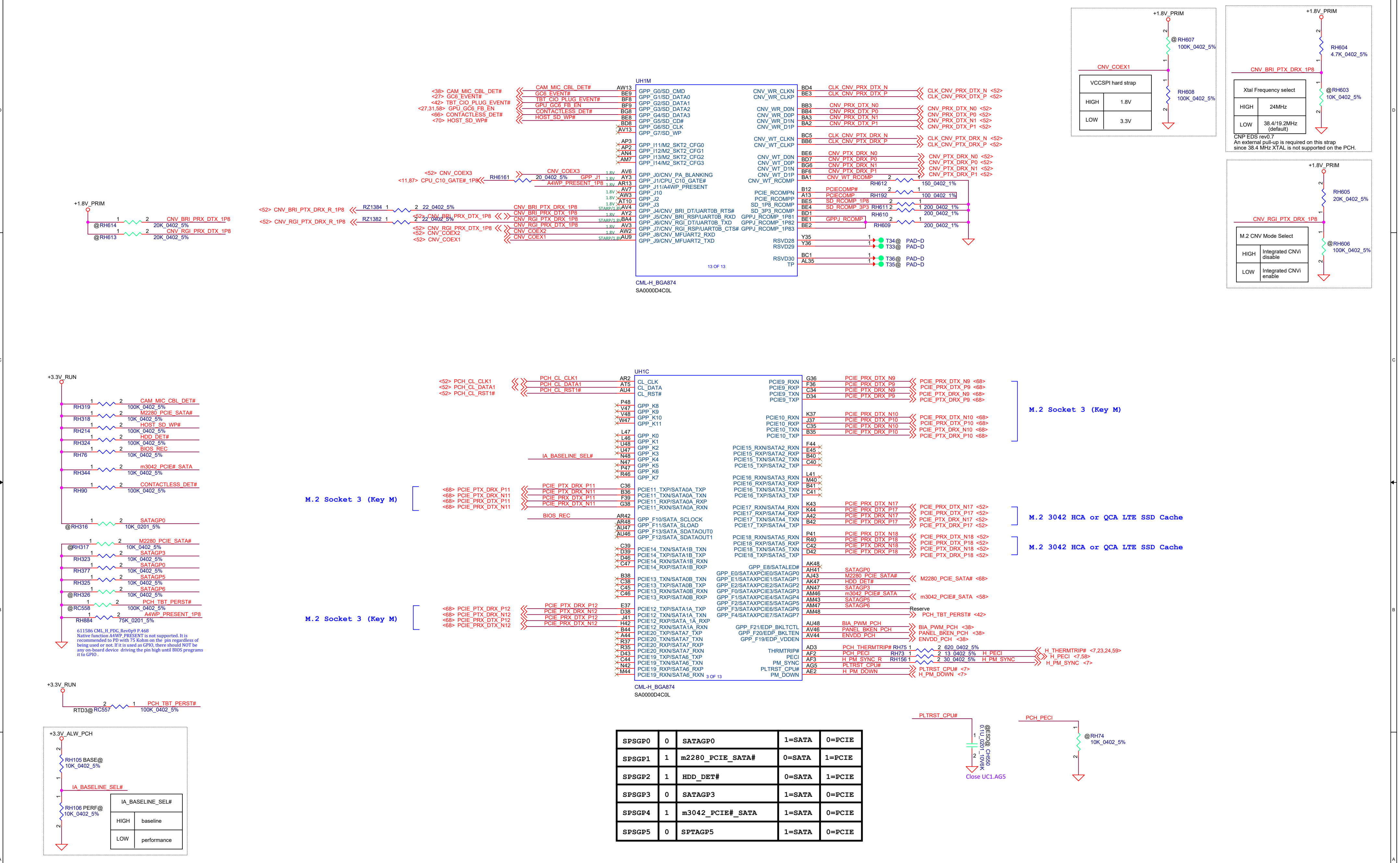

VCCSPI hard strap	
HIGH	1.8V
LOW	3.3V

Xtal Frequency select	
HIGH	24MHz
LOW	38.4/19.2MHz (default)

M.2 CNV Mode Select	
HIGH	Integrated CNVi disable
LOW	Integrated CNVi enable

IA_BASELINE_SEL#	
HIGH	baseline
LOW	performance

SPSGP0	0	SATAGP0	1=SATA	0=PCIE
SPSGP1	1	m2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	m3042_PCIE#_SATA	1=SATA	0=PCIE
SPSGP5	0	SPTAGP5	1=SATA	0=PCIE

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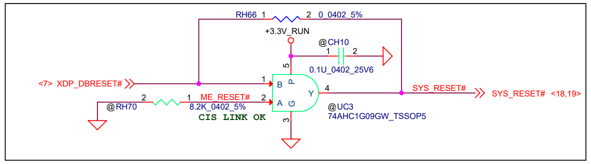
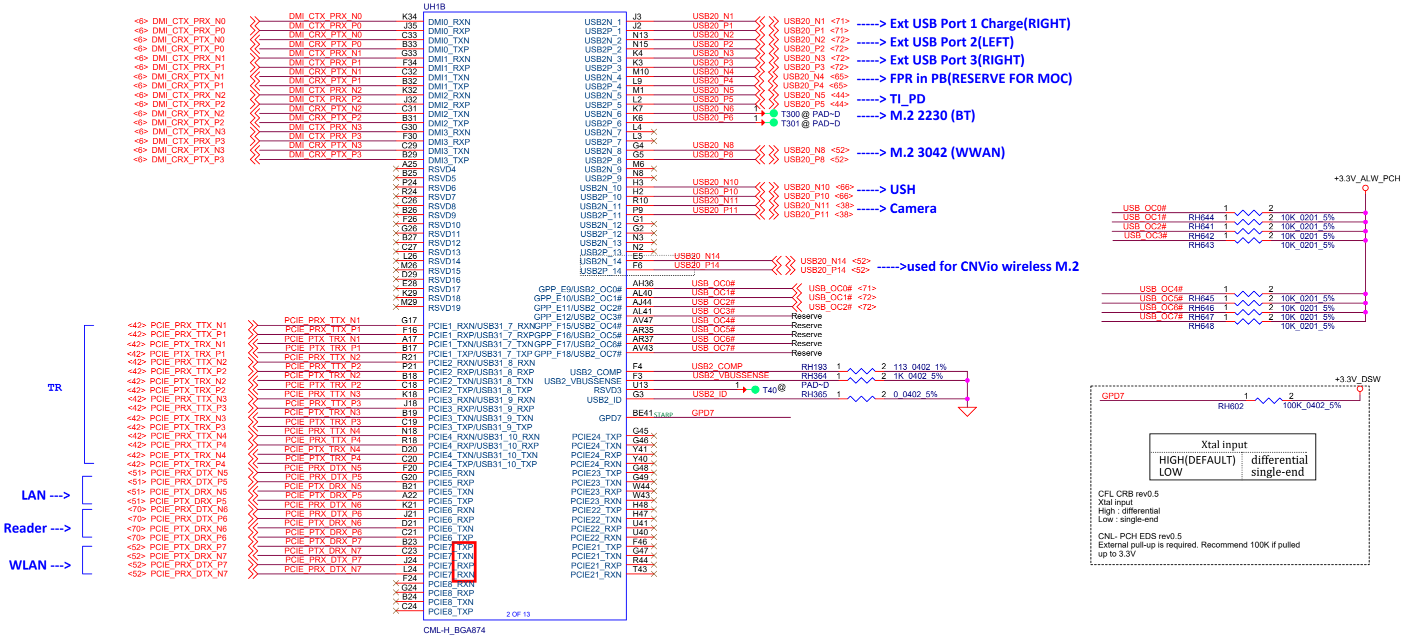
Title *CometLake PCH-H (1/9)*

Size C Document Number *LA-J272P* Rev 0.2





Xtal input	
HIGH(DEFAULT)	differential
LOW	single-end

CFL CRB rev0.5
Xtal input
High : differential
Low : single-end

CNL- PCH EDS rev0.5
External pull-up is required. Recommend 100K if pulled up to 3.3V

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Title
CometLake PCH-H (2/9)

Size C
Document Number *LA-J272P*
Rev 0.2

Date: Friday, October 25, 2019
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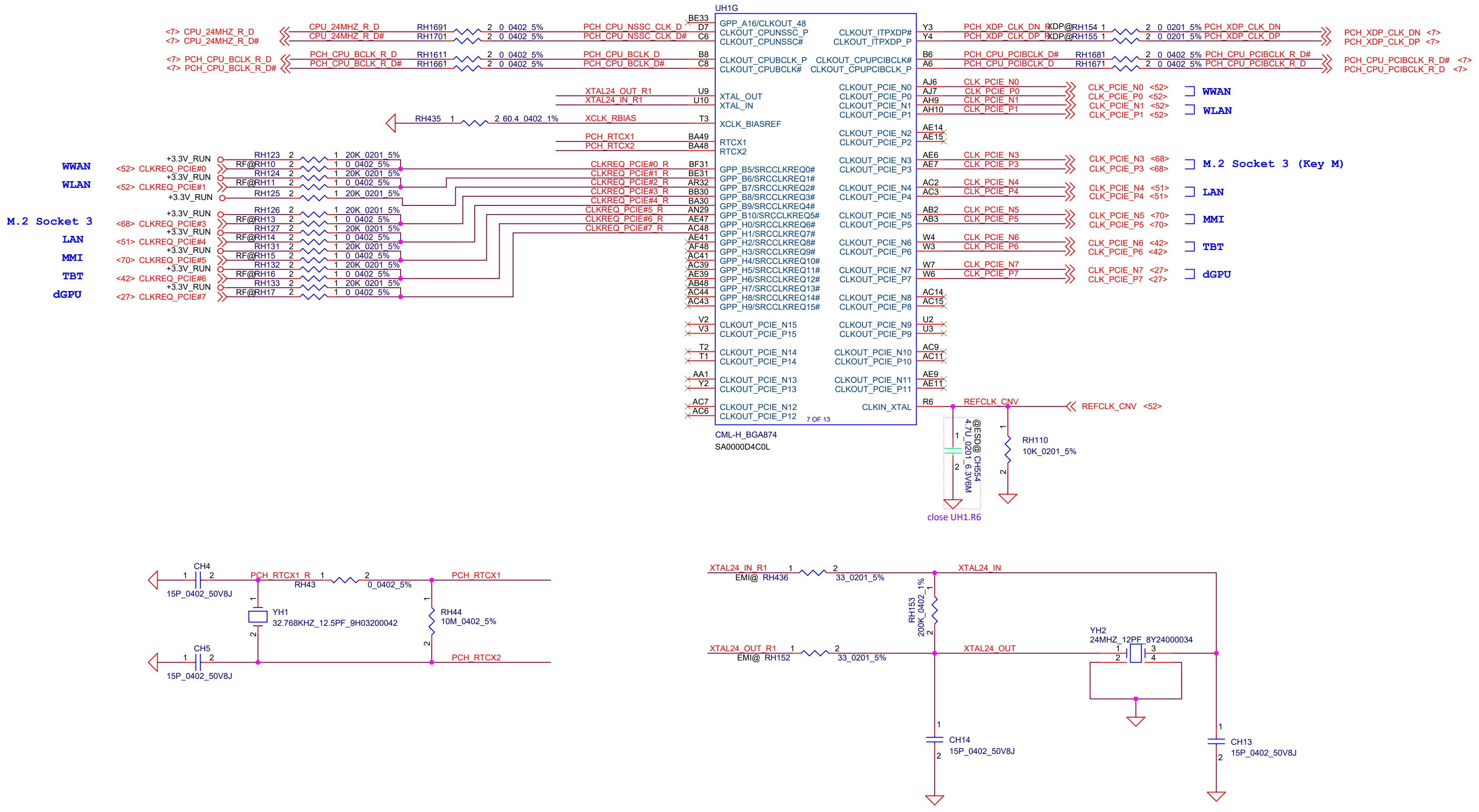

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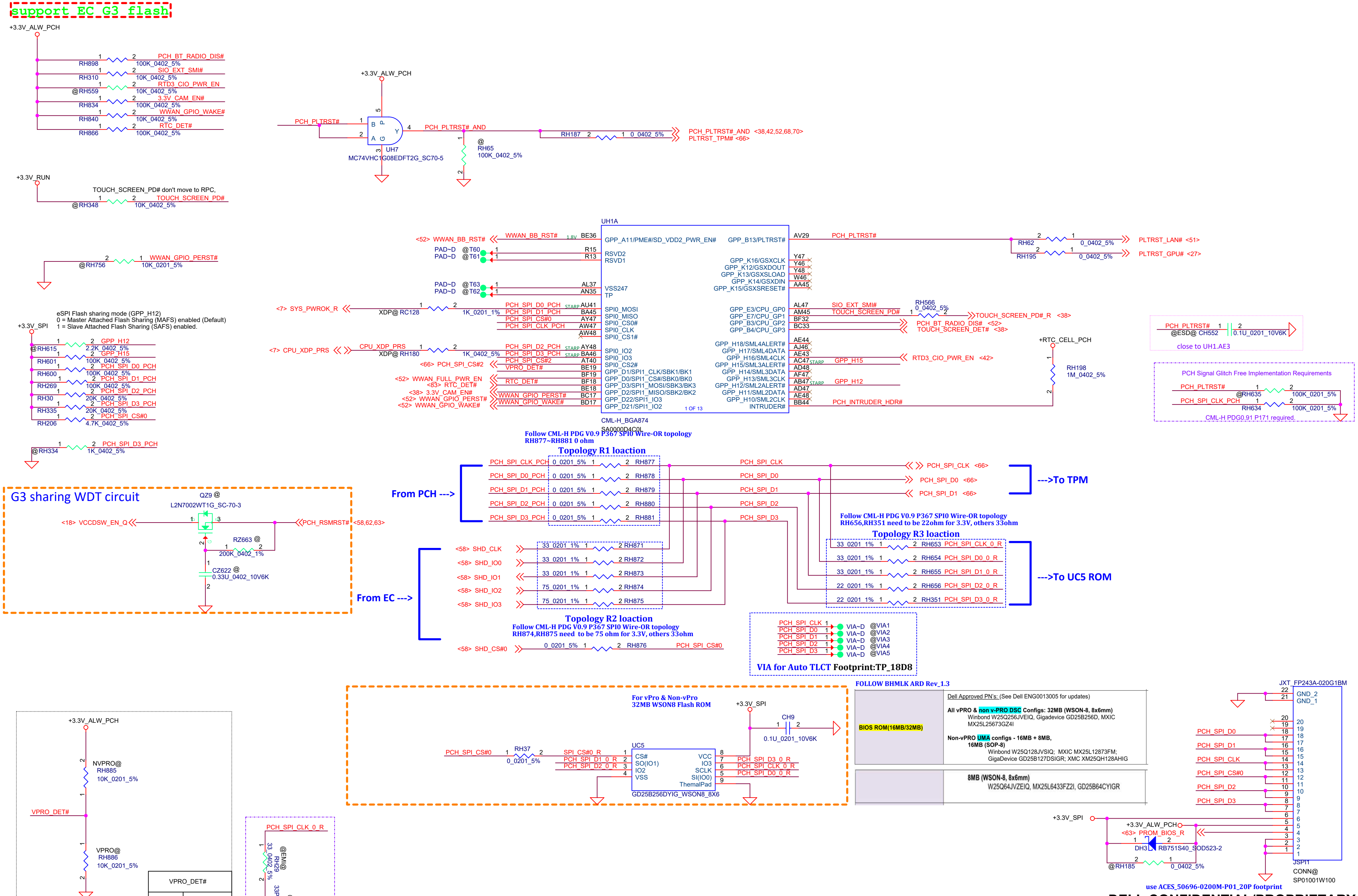
Title *CometLake PCH-H (3/9)*

Size	Document Number	Rev
B	*LA-J272P*	0.2

Date: Friday, October 25, 2019 Sheet 16 of 108



VPRO_DET#	
HIGH	NON VPRO
LOW	VPRO

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CometLake PCH-H (4/9)

Size	Document Number	Rev
B	LA-J272P	0.2

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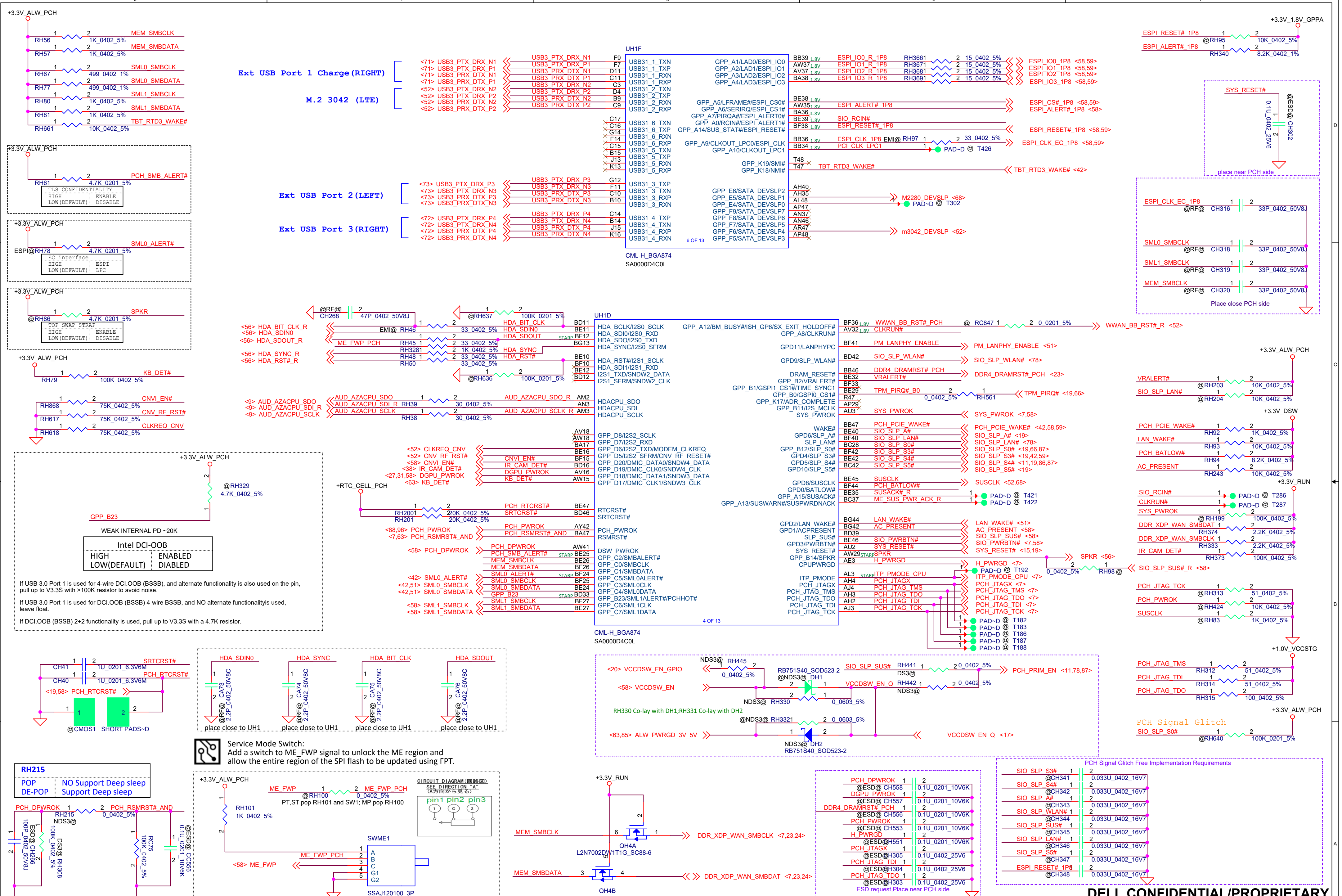

Intel DCI-OOB

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

If USB 3.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.

If USB 3.0 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionalityis used, leave float.

If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD.
(suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE

LOW = ENABLE (DEFAULT) -->Pin2 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin1 & Pin2 short

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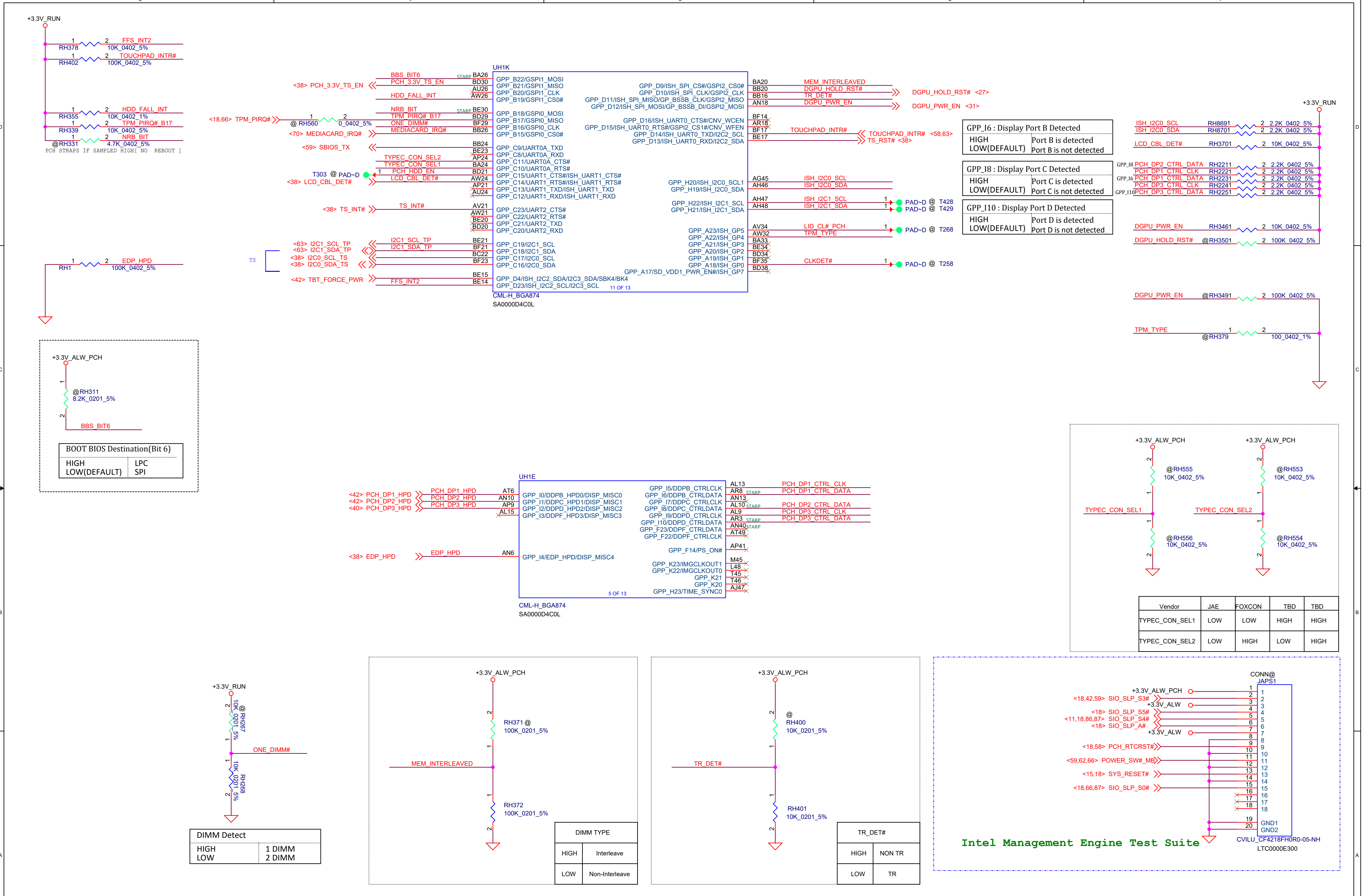
Size B
Document Number LA-J272P
Rev 0.2



GPP_I6 : Display Port B Detected	
HIGH	Port B is detected
LOW(DEFAULT)	Port B is not detected

GPP_I8 : Display Port C Detected	
HIGH	Port C is detected
LOW(DEFAULT)	Port C is not detected

GPP_I10 : Display Port D Detected	
HIGH	Port D is detected
LOW(DEFAULT)	Port D is not detected

BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

TR_DET#	
HIGH	NON TR
LOW	TR

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Title *CometLake PCH-H (6/9)*

Size B Document Number *LA-J272P* Rev 0.2

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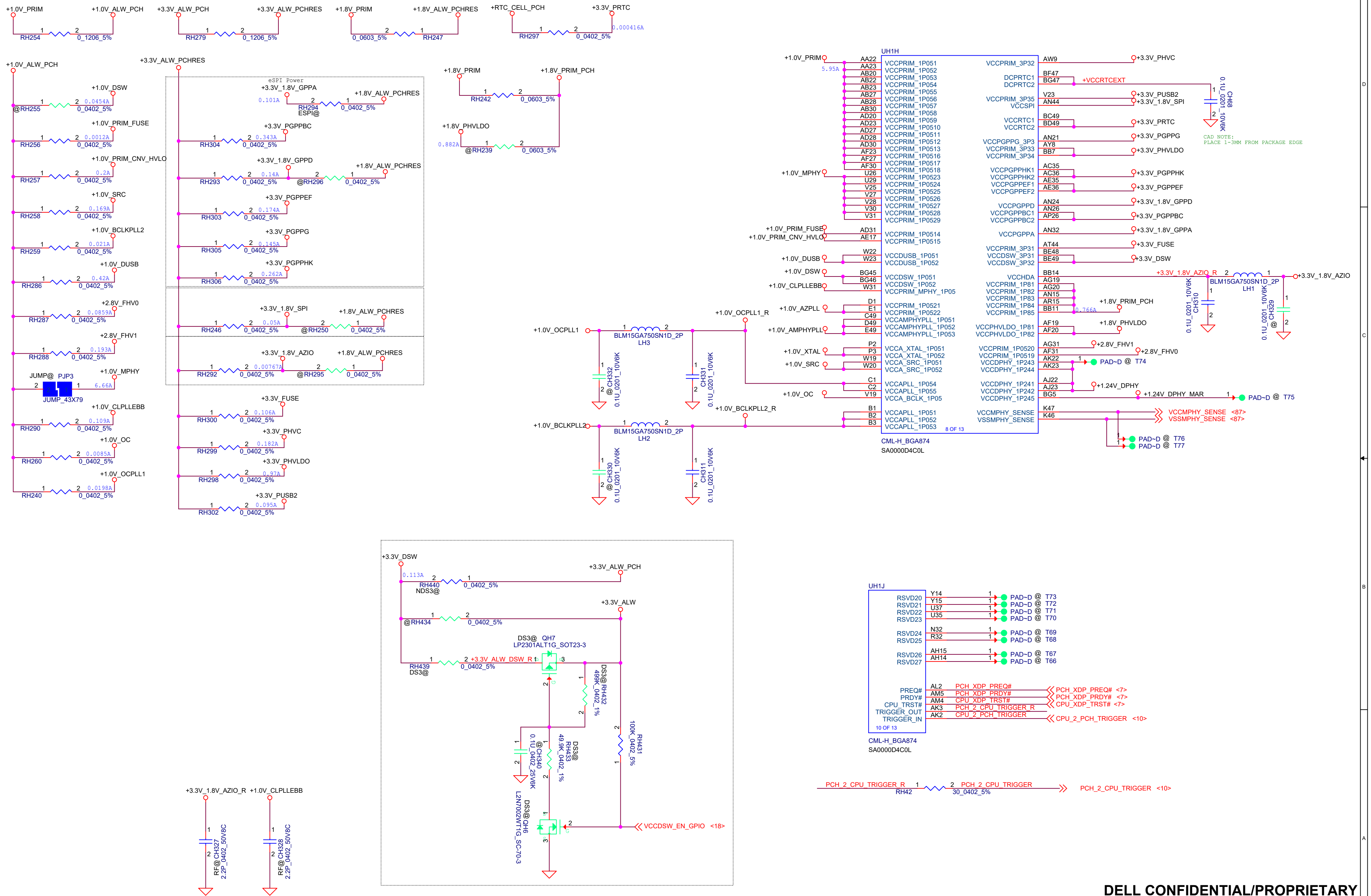

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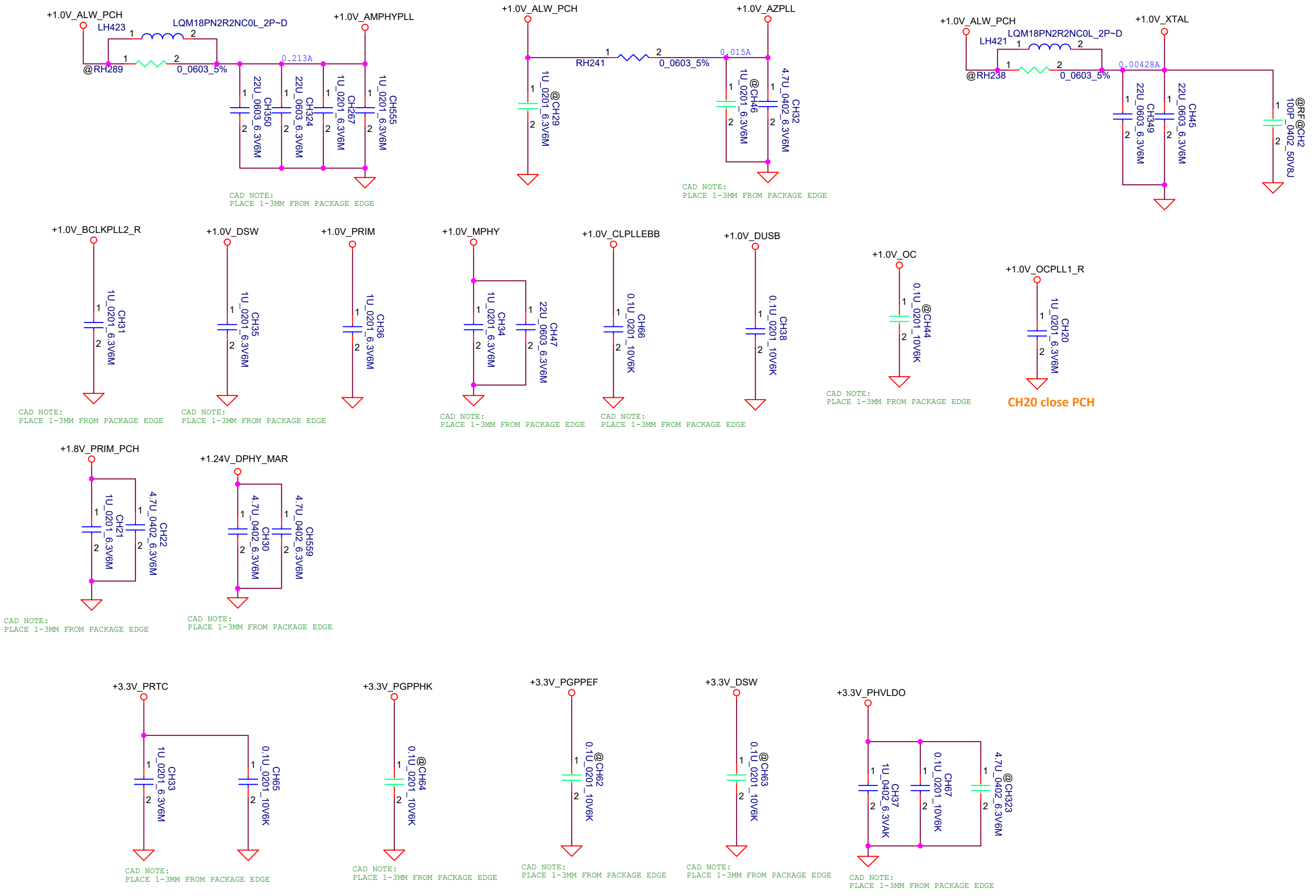
Size: B
Document Number: **LA-J272P**
Rev: 0.2

Date: Friday, October 25, 2019
Sheet 20 of 108

PCH Decoupling cap Follow 611586_CML_H_PDG_Rev0p7
page. 598 Table 329. Decoupling and Power Connection Requirements for PCH-H



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Size B
Document Number *LA-J272P*
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Date: Friday, October 25, 2019
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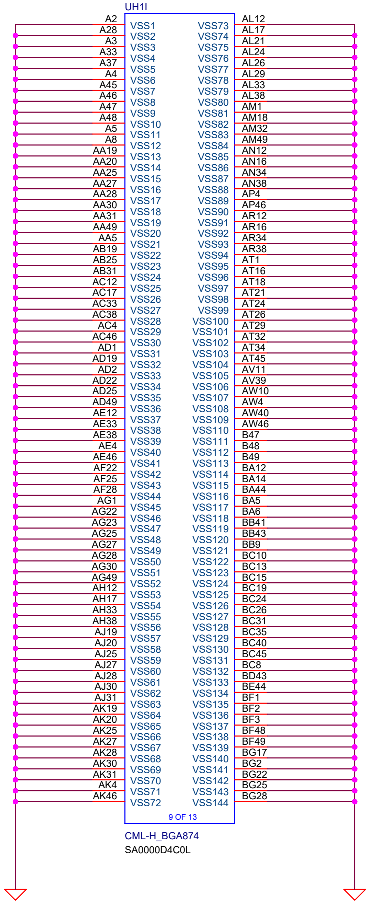

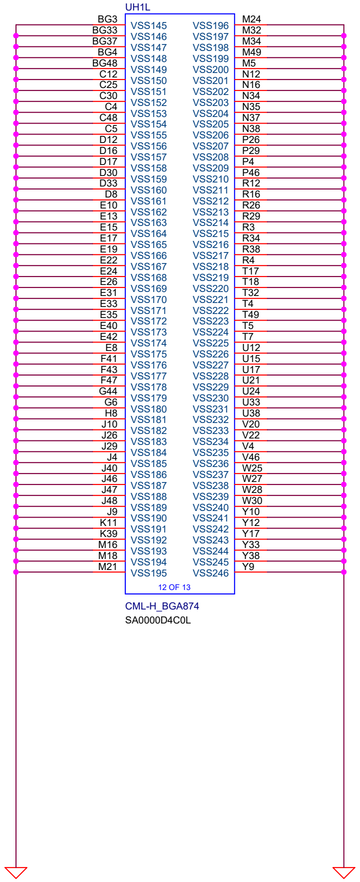

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Size B
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Rev 0.2

Date: Friday, October 25, 2019
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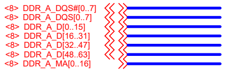
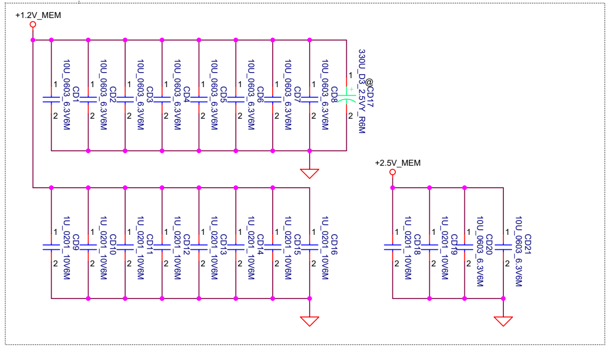
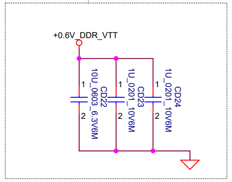


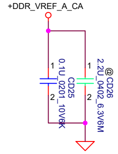
Layout Note:
Place near JDIMM1

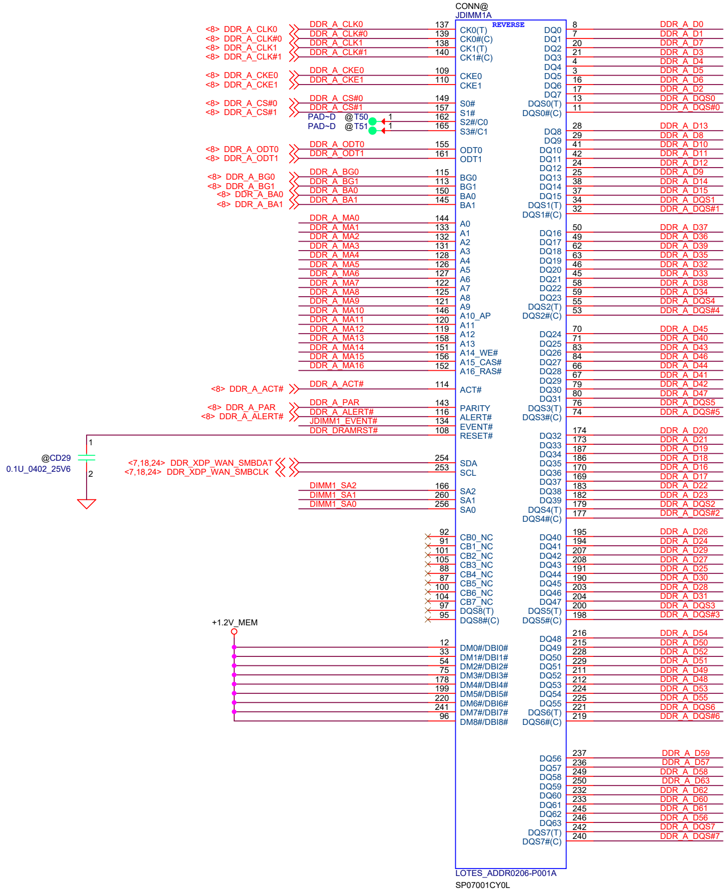
SODIMM Decoupling cap Follow 611586_CML_H_PDG_Rev0p7 page. 126 Table 28. DDR4 SODIMM Power Plane Decoupling

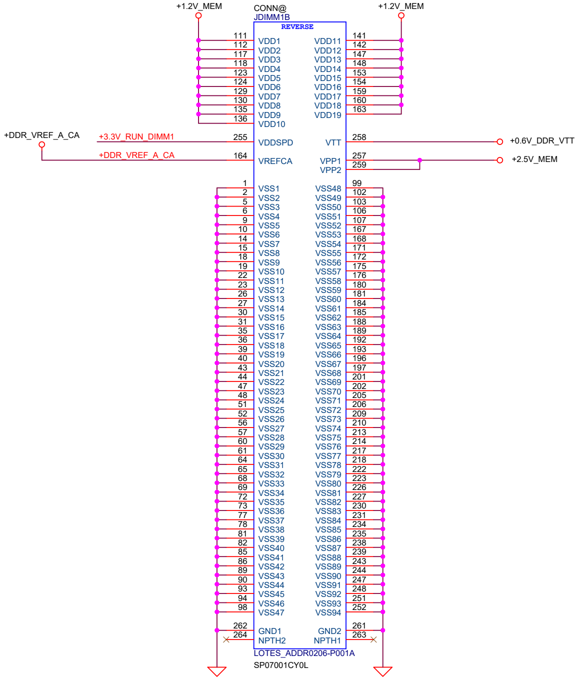


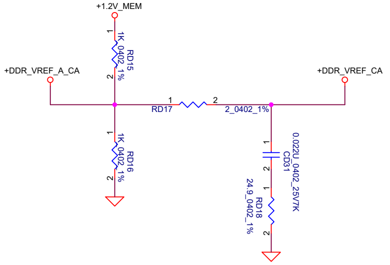
Layout Note:
Place near
JDIMM1.258





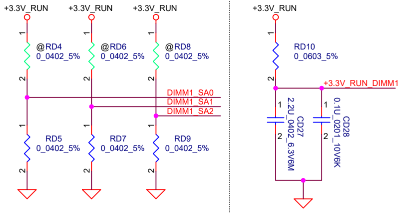


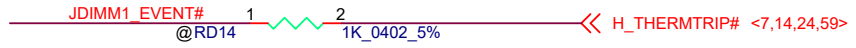




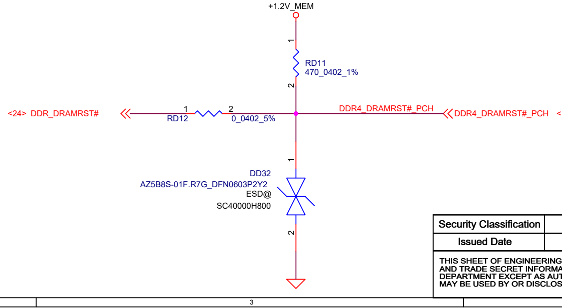
DIMM Select

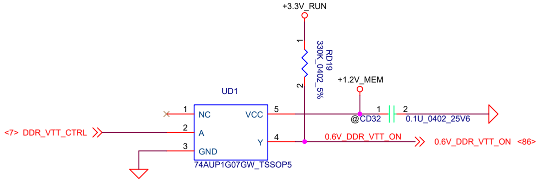
	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0





Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
* **Byte[3]**	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
* **Byte[5]**	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]





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Title ***DDR4-SODIMM SLOT1***

Size C Document Number ***LA-J272P*** Rev 0.2

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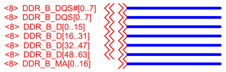
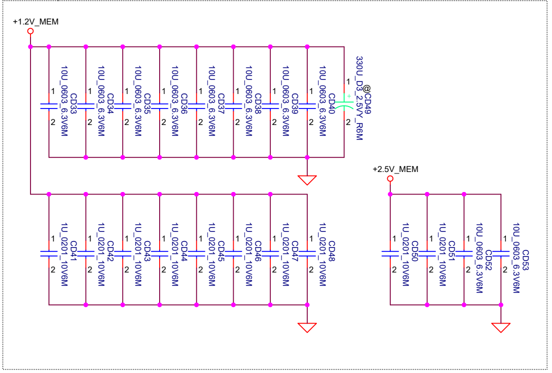


Layout Note:
Place near JDIMM2

SODIMM Decoupling cap Follow 611586_CML_H_PDG_Rev0p7 page. 126 Table 28. DDR4 SODIMM Power Plane Decoupling



Layout Note:
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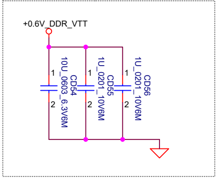
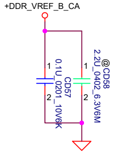
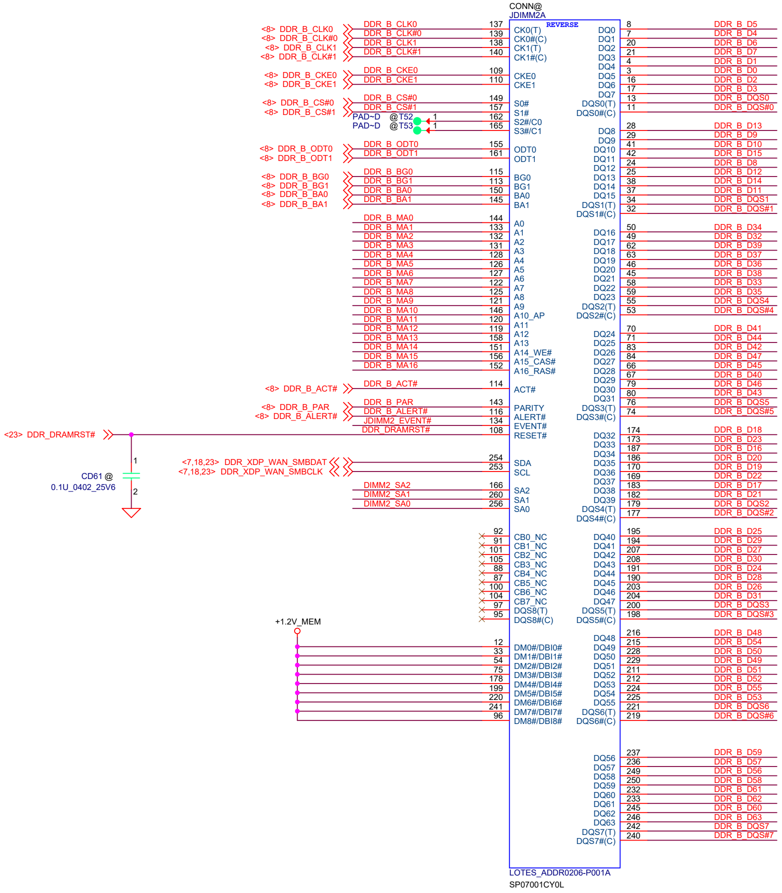
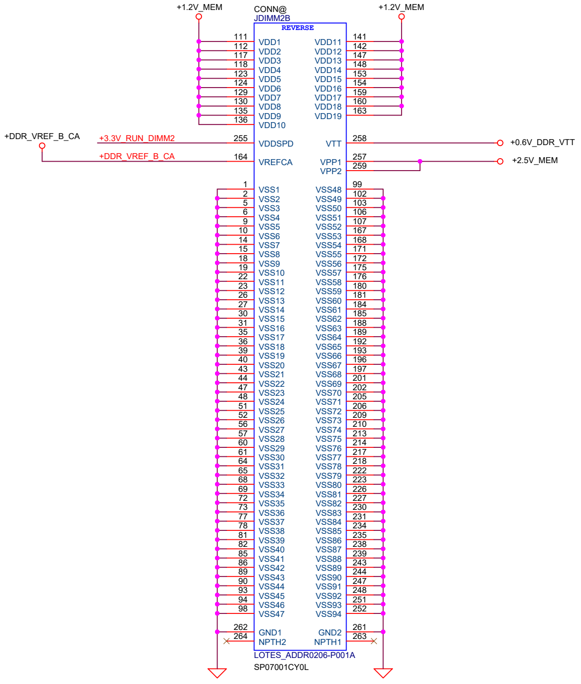
JDIMM2.258



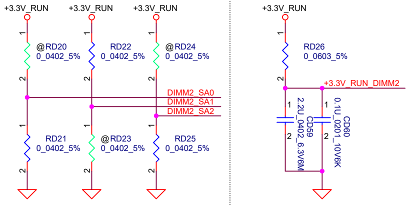


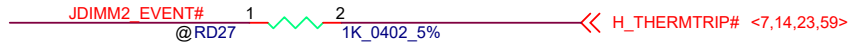


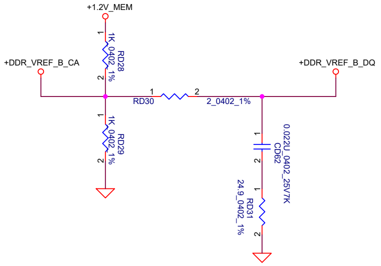


DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0







Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
* Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
* Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

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Compal Electronics, Inc.

Title
DDR4-SODIMM SLOT2

Size C
Document Number *LA-J272P*
Rev 0.2

Date: Friday, October 25, 2019
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Reserve

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Title	DDR_2	
Size	Document Number LA-J272P	Rev 0.2
Date:	Friday, October 25, 2019	Sheet 25 of 108

Reserve

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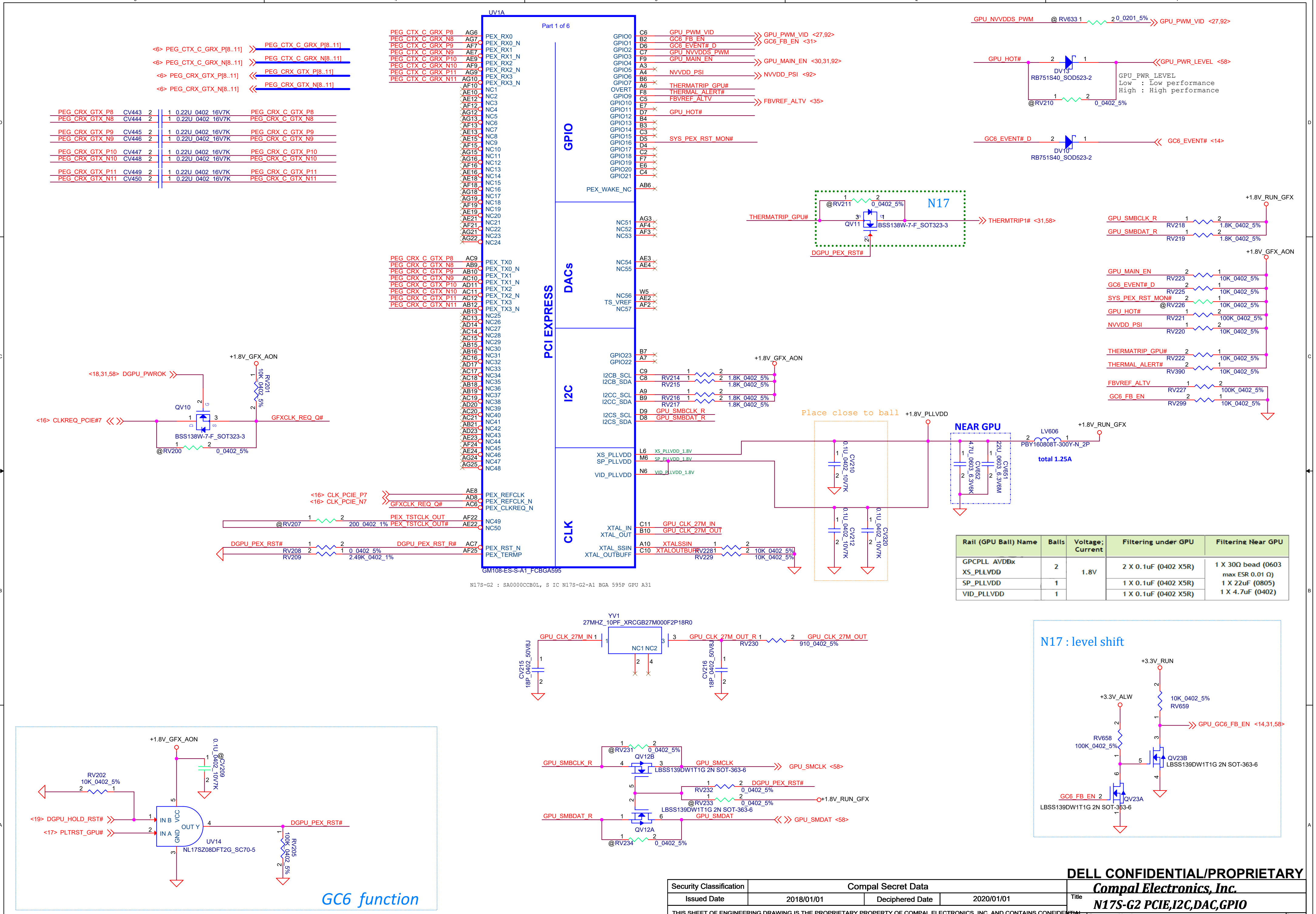

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
GPCPLL_AVDDx XS_PLLVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	

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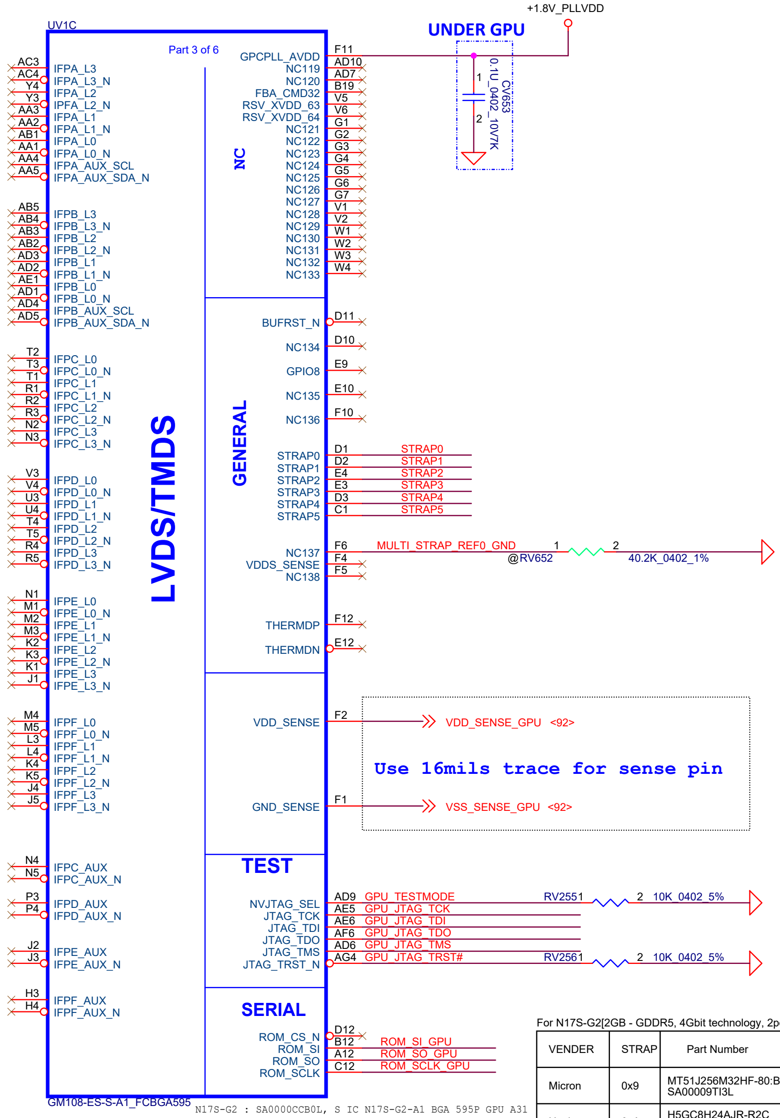
Compal Electronics, Inc.

Title
N17S-G2 PCIE,I2C,DAC,GPIO

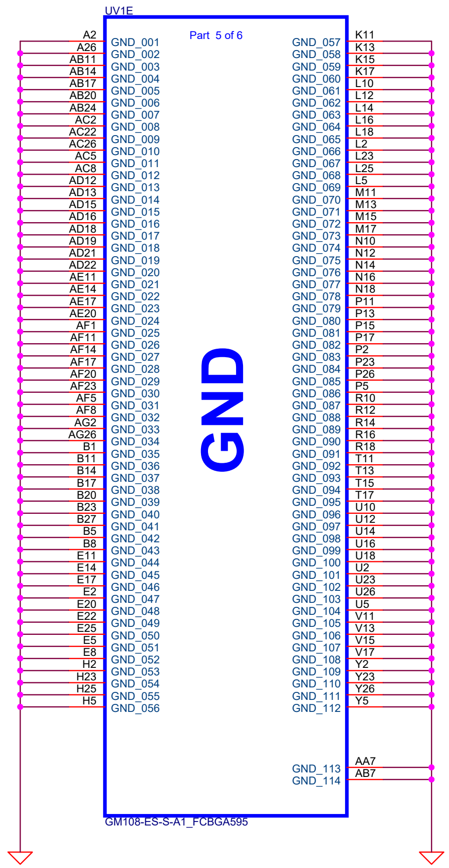
Size Custom
Document Number **LA-J272P**
Rev 0.2

Date: Friday, October 25, 2019

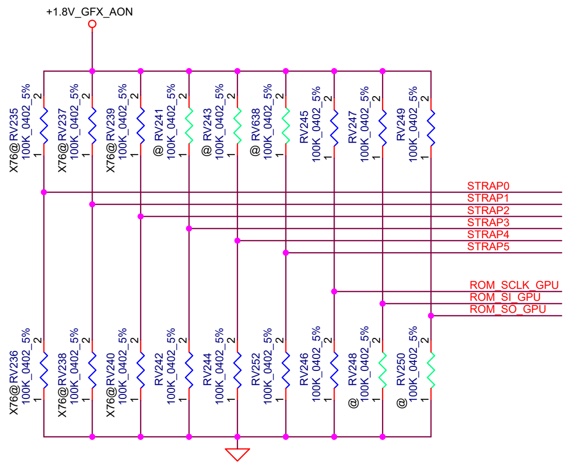


Use 16mils trace for sense pin

N17S-G2 : SA0000CCB0L, S IC N17S-G2-A1 BGA 595P GPU A31



N17S-G2 Decive ID 0x1D13



Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Daniel YS Cheng Compal - Dell Notebook

For N17S-G2[2GB - GDDR5, 4Gbit technology, 2pcs x 32]

VENDER	STRAP	Part Number	Note (Strap2,Strap1,Strap0)
Micron	0x9	MT51J256M32HF-80:B SA00009TI3L	(L, M, L)
Hynix	0xA	H5GC8H24AJR-R2C SA0000C171L	(L, M, H)
Samsung	0x3	K4G80325FC-HC25 SA00009TA3L	(L, H, H)

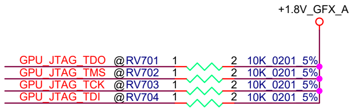


Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post production ready

Notes:

1. For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

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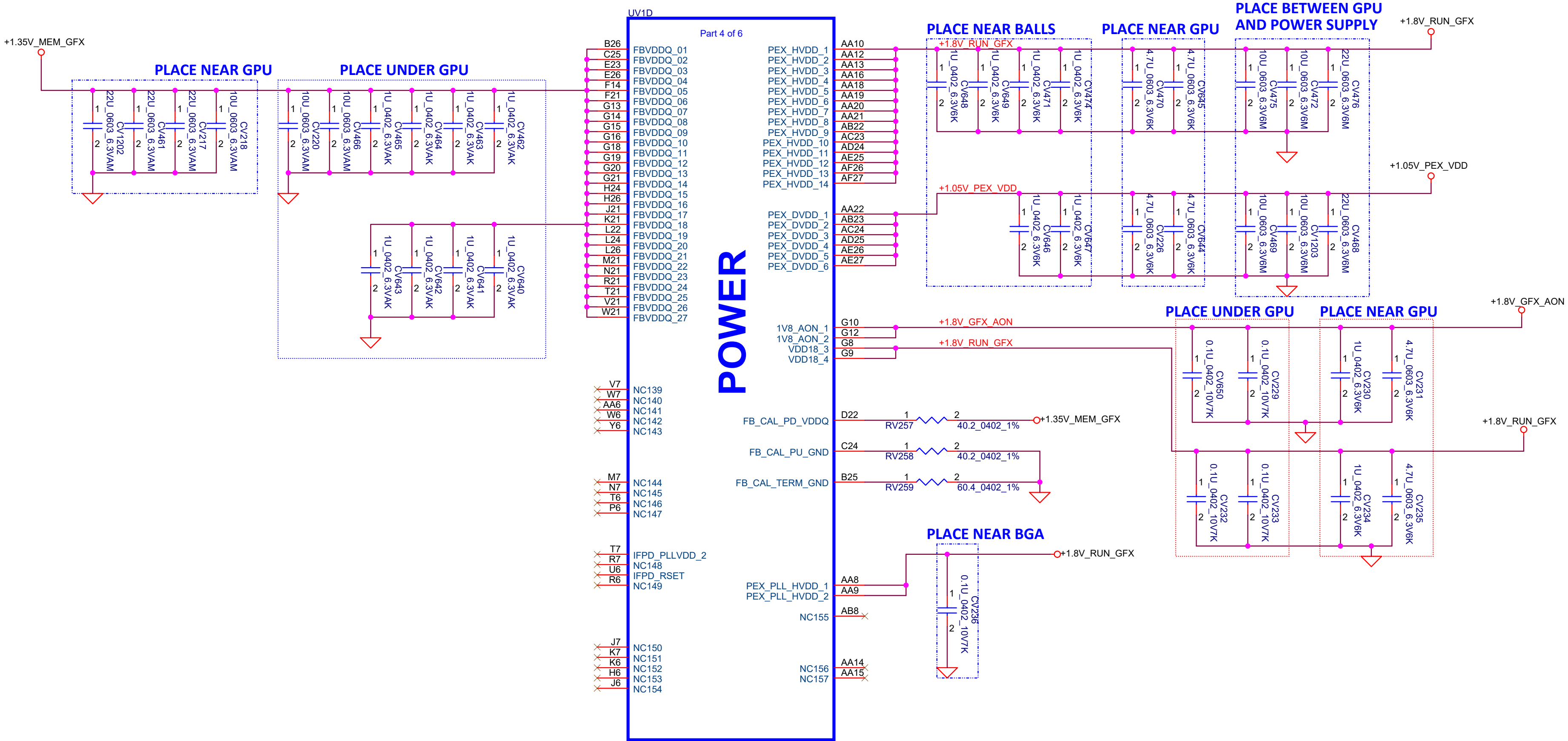

N17S-G2 : SA0000CCB0L, S IC N17S-G2-A1 BGA 595P GPU A31

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

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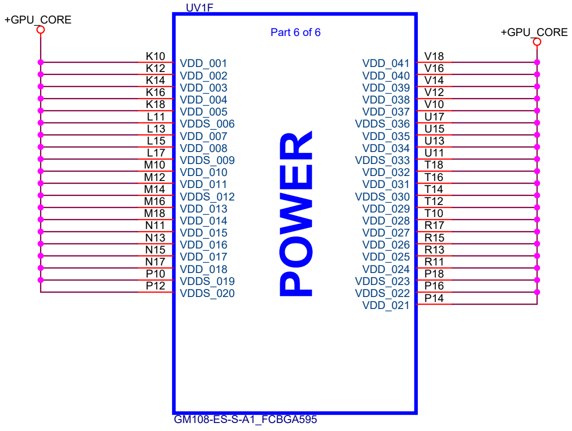
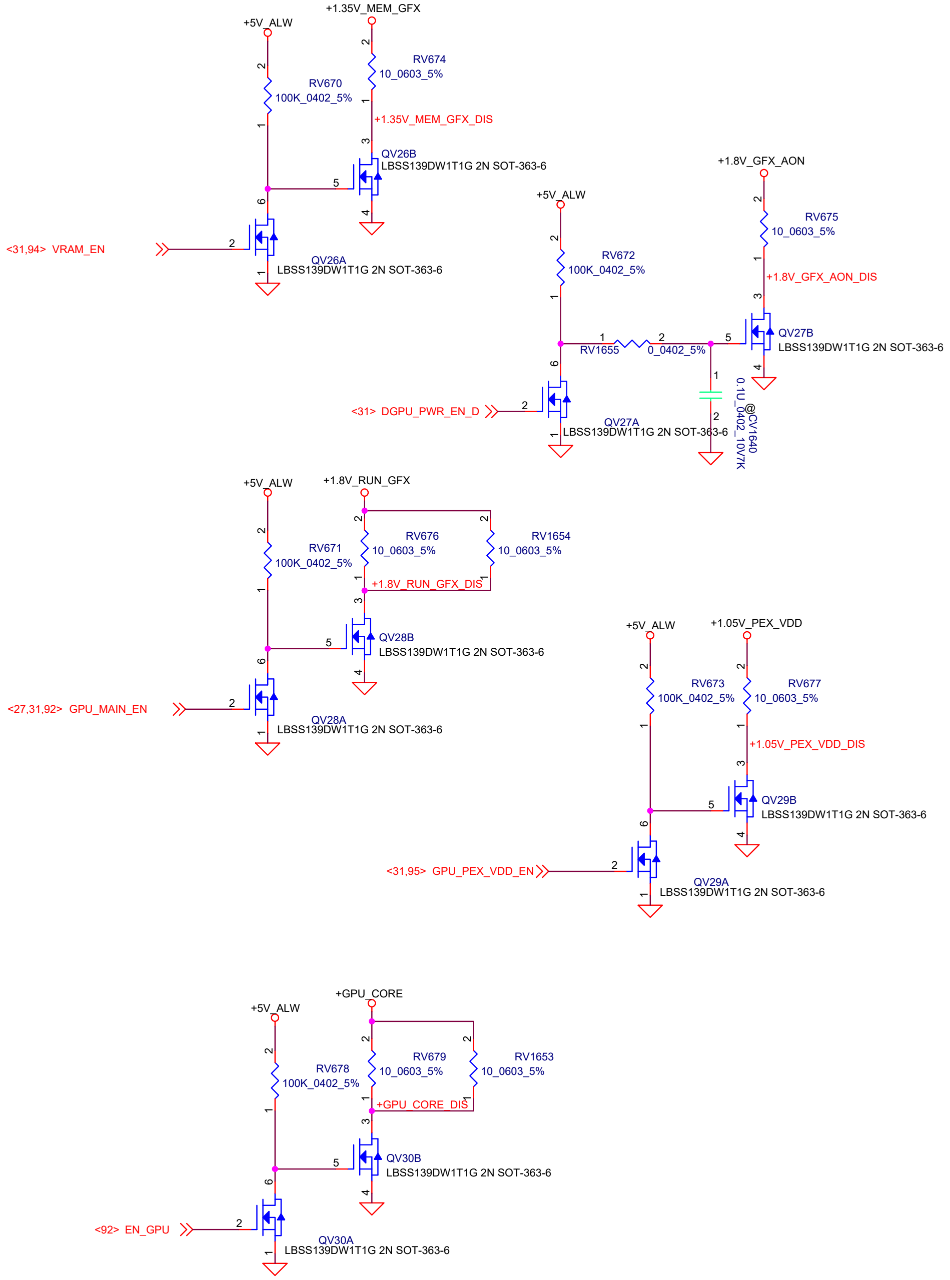


N17S-G2 : SA0000CCB0L, S IC N17S-G2-A1 BGA 595P GPU A31



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Title
N17S-G2 PCIE,I2C,DAC,GPIO

Size: Custom
Document Number: ***LA-J272P***
Rev: 0.2

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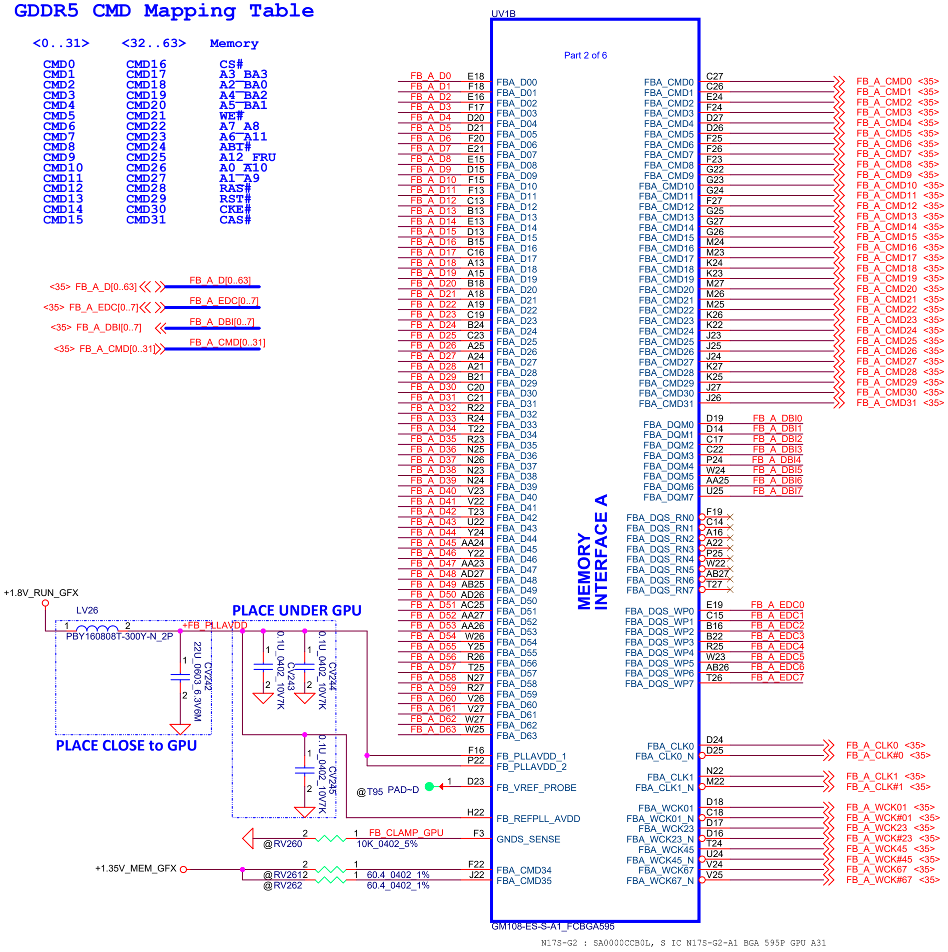
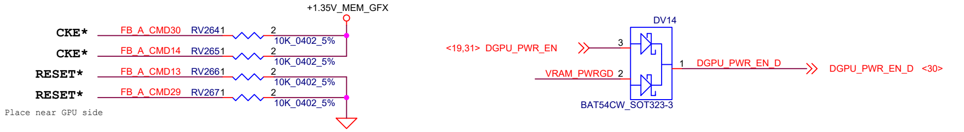
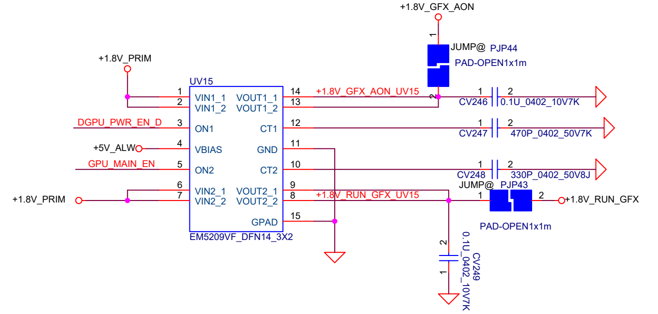
GDDR5 CMD Mapping Table

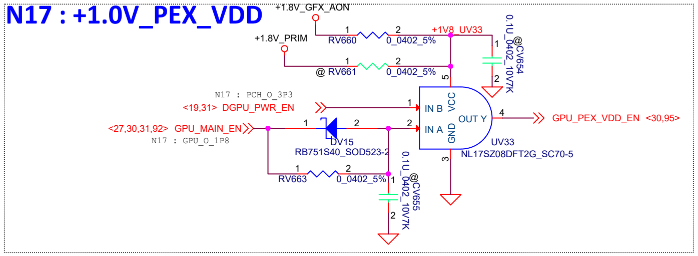
<0..31>	<32..63>	Memory
CMD0	CMD16	CS#
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_FRU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

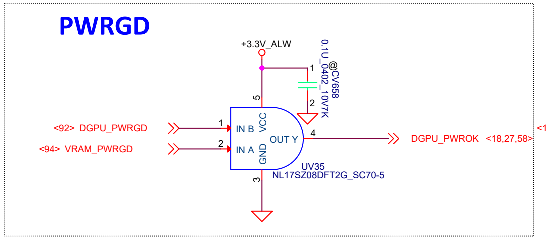


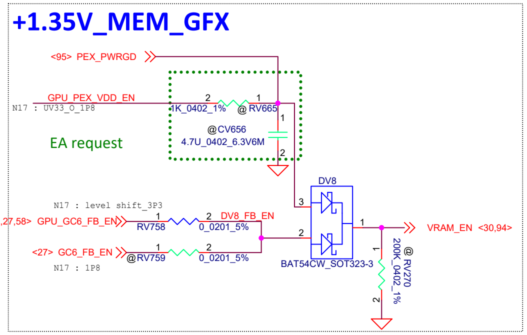
Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 30Ω bead (0603 max ESR 10 mΩ) 1 X 22uF (0805)
FBB_PLL_AVDD	1			
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	

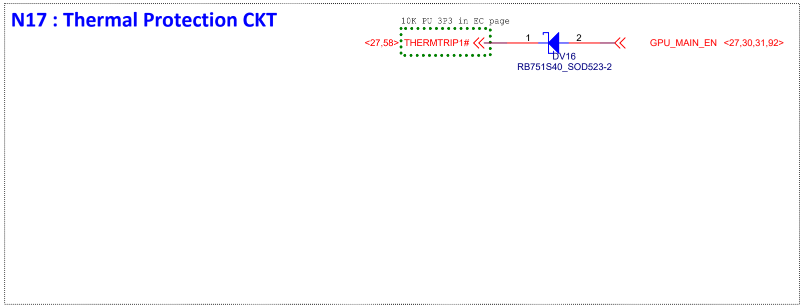





N17 : +1.0V_PEX_VDD


PWRGD


+1.35V_MEM_GFX


N17 : Thermal Protection CKT

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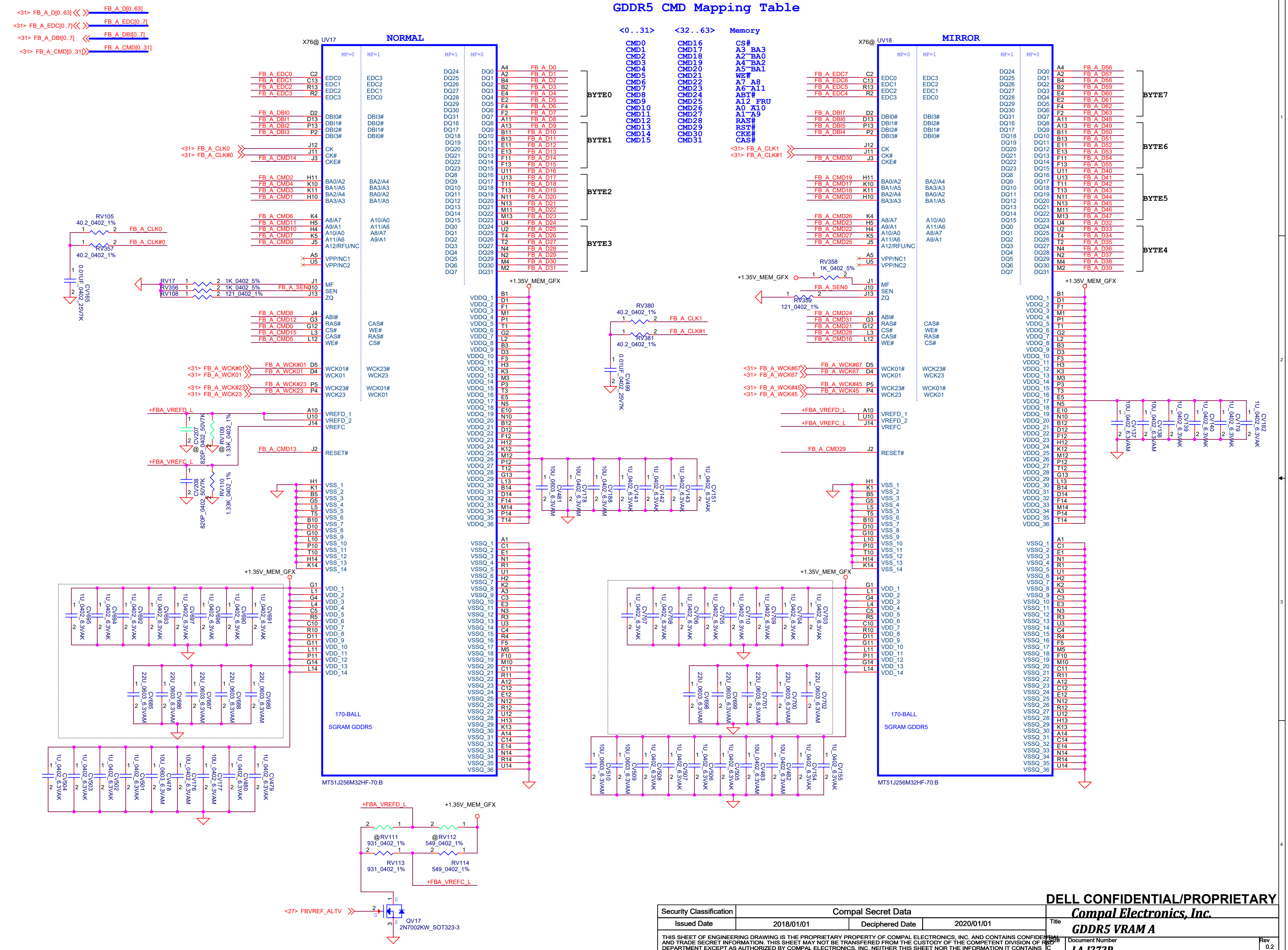

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
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CMD3	CMD19	A4_BA2
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CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_FRU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

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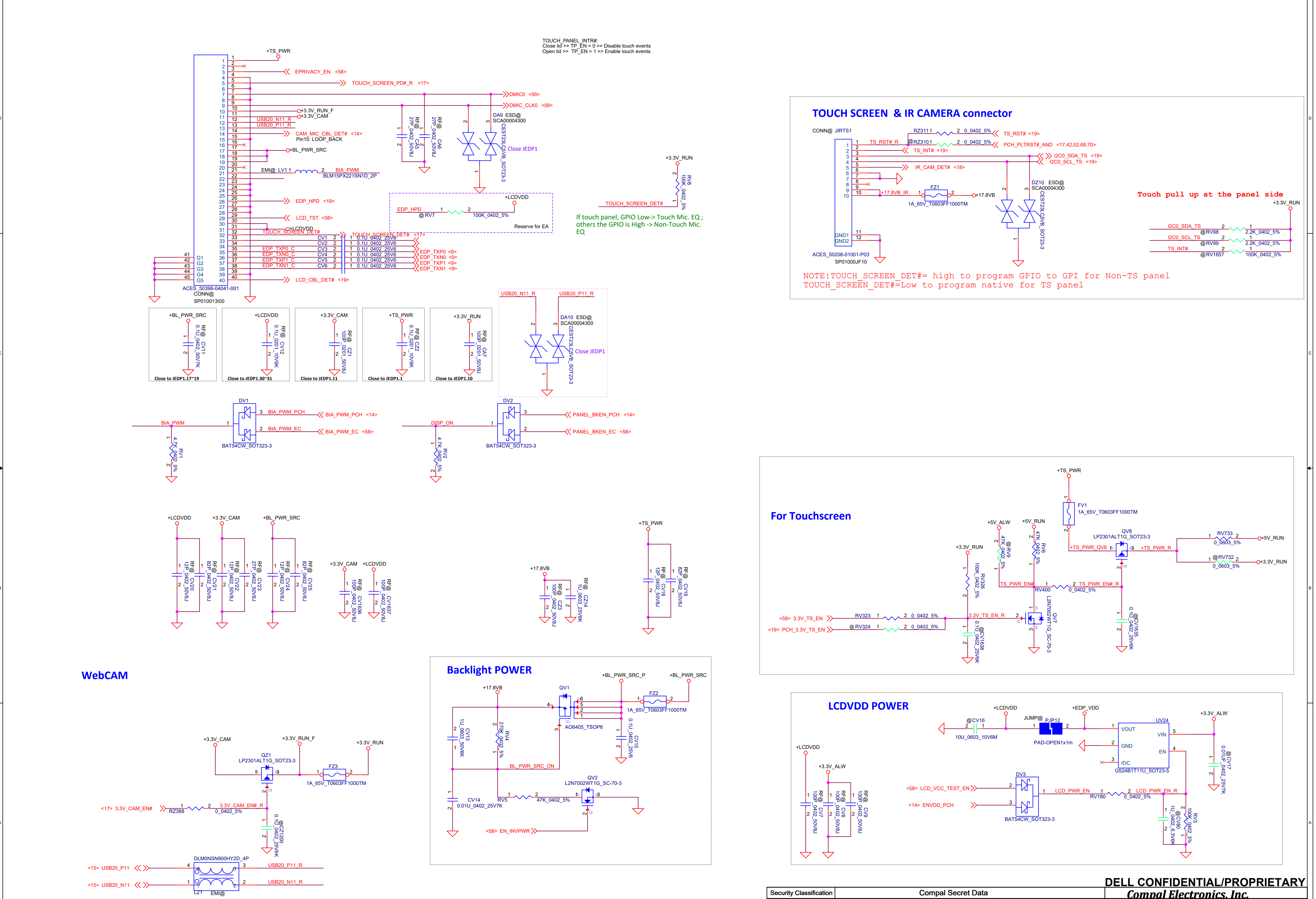

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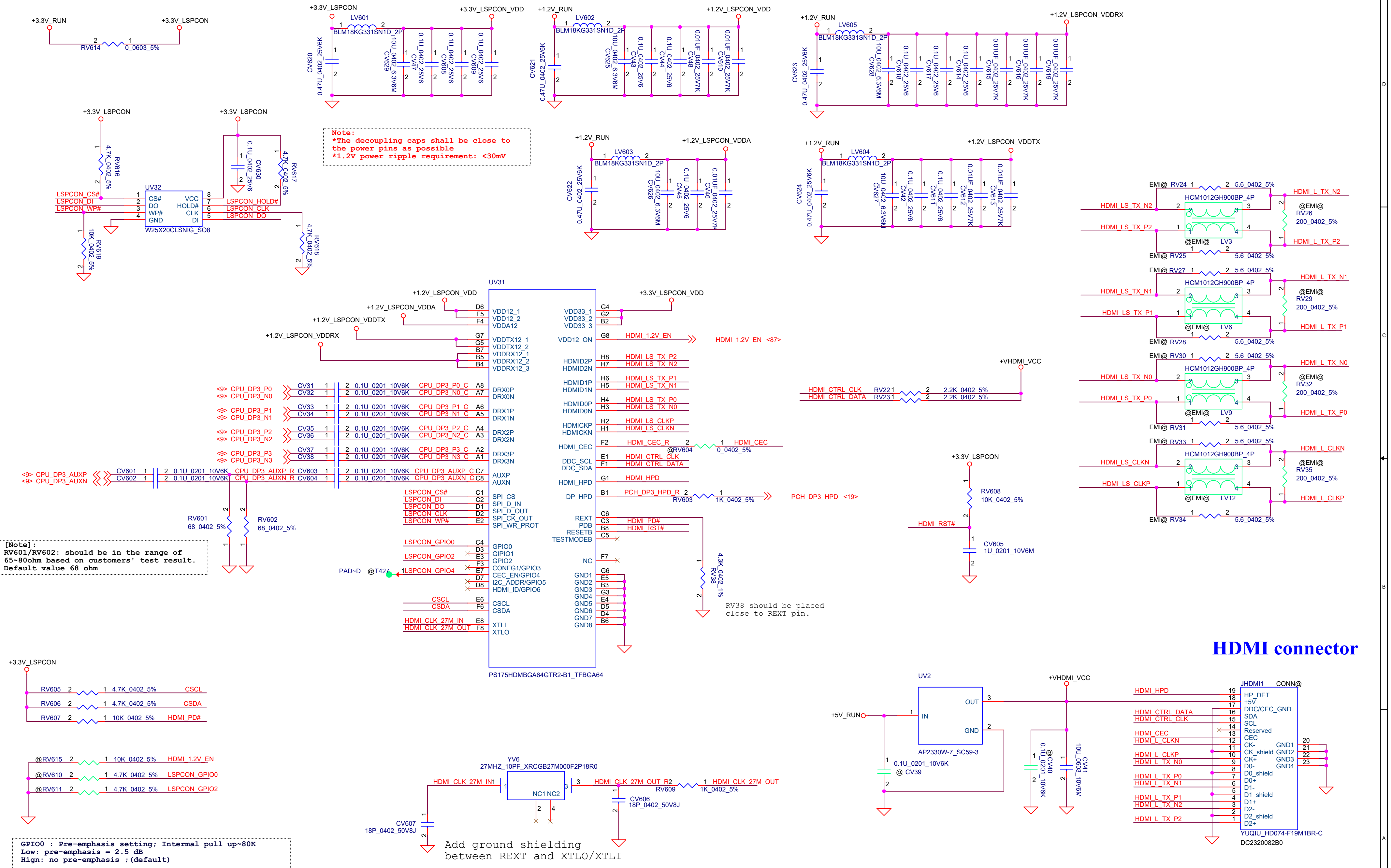

Note:
*The decoupling caps shall be close to the power pins as possible
*1.2V power ripple requirement: <30mV

[Note]:
RV601/RV602: should be in the range of 65~80ohm based on customers' test result.
Default value 68 ohm

RV38 should be placed close to REXT pin.

Add ground shielding between REXT and XTLO/XTLI

HDMI connector

GPIO0 : Pre-emphasis setting; Internal pull up~80K
Low: pre-emphasis = 2.5 dB
Hign: no pre-emphasis ;(default)

GPIO2:Firmware initial address, internal pull-up~80K
Low: Start from Bank 7
High: Start from Bank 3 ;(default)

CEC_EN/GPIO4: For debug purpose

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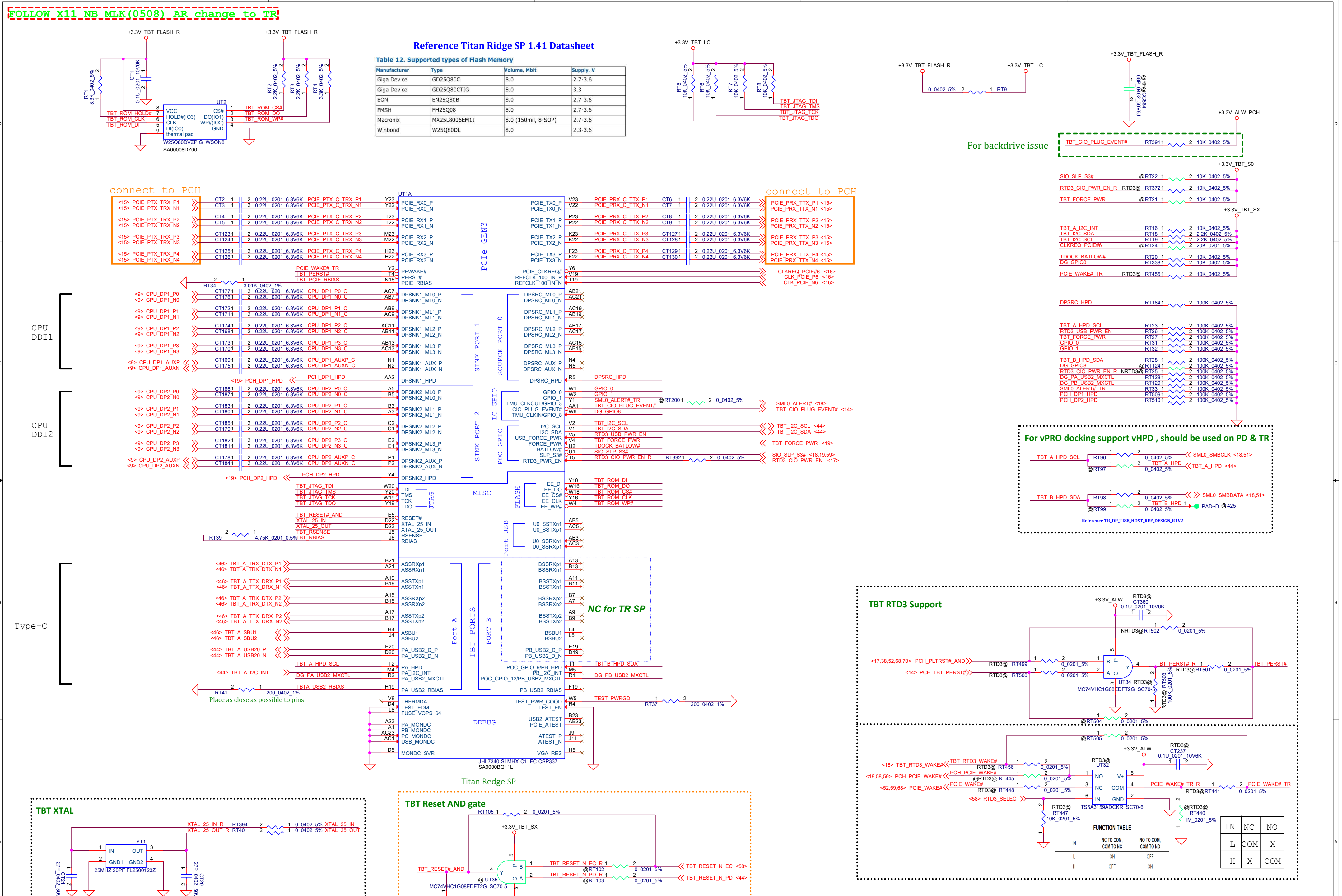

Reference Titan Ridge SP 1.41 Datasheet

Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
Giga Device	GD25Q80C	8.0	2.7-3.6
Giga Device	GD25Q80CTIG	8.0	3.3
EON	EN25Q80B	8.0	2.7-3.6
FMSH	FM25Q08	8.0	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Winbond	W25Q80DL	8.0	2.3-3.6

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

IN	NC	NO
L	COM	X
H	X	COM

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Size: Custom

Document Number: LA-J272P

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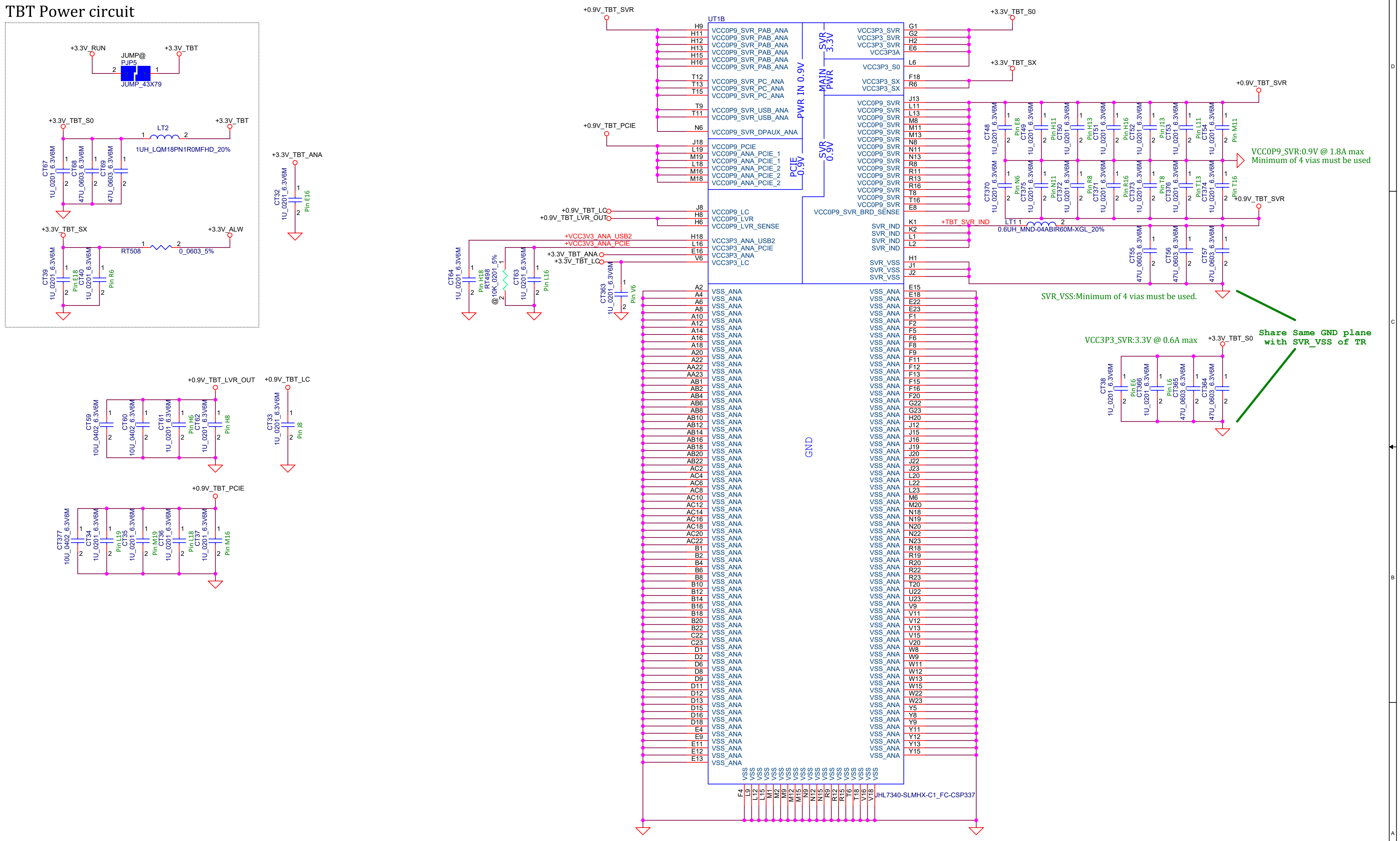
TBT Power circuit



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Title
TBT-TR-SP(2/2)PWR,VSS

Size B
Document Number *LA-J272P*
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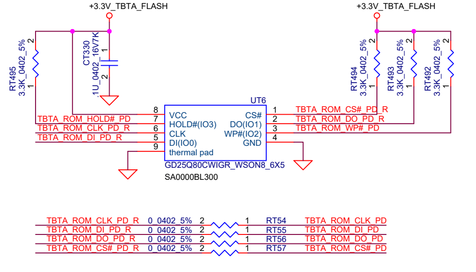
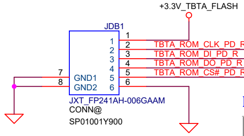
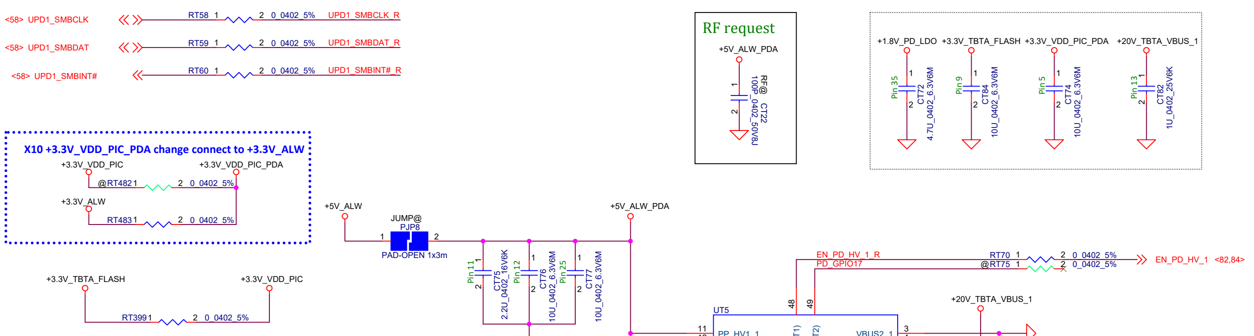
FOLLOW X11 NB MLK(0508) PD 65982DD change to 65987DD

For TR Config

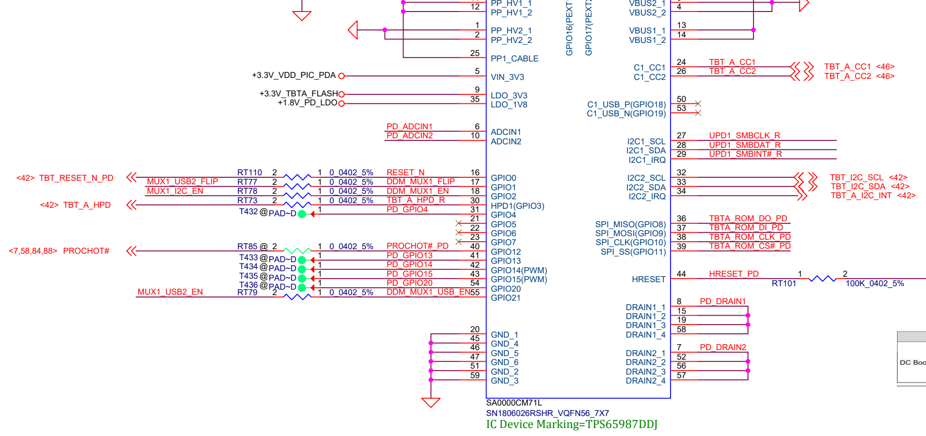




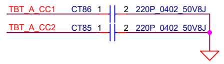


PD GPIO define

GPIO	Pin #	Package Pin Name	TPS65988 (Dual Port) CML-TR	TPS65987S (Single Port) CML-TR		NOTES
0	16	GPIO0 (RESETZ)	TR_RESETZ	TR_RESETZ		
1	17	GPIO1	DDM_MUX1_FLIP	DDM_MUX1_FLIP		GPIO for I2C/USB2.0 Mux control
2	18	GPIO2	DDM_MUX1_EN	DDM_MUX1_EN		
3	30	GPIO3 (HPD1)	TR_PA_HPD	TR_PA_HPD		HPD/SMBus_vPro
4	31	GPIO4 (HPD2)	TR_PB_HPD	-		
5	21	GPIO5	-	-		Resv I2C3/GPIO for external DP-USB3 Mux control
6	22	GPIO6	-	-		
7	23	GPIO7	-	-		
8	36	SPI_MISO (Boot Mode)	SPI_MISO	SPI_MISO		Backup SPI Flash
9	37	SPI_MOSI (GPIO9)	SPI_MOSI	SPI_MOSI		
10	38	SPI_CLK (GPIO10)	SPI_CLK	SPI_CLK		
11	39	SPI_SS (GPIO11)	SPI_SS	SPI_SS		
12	40	GPIO12 (SWD)	PROCHOT#	PROCHOT#		PD configs as OD for shared use
13	41	GPIO13 (SWD)	-	-		Resv for DDM_MUX2_USB_EN
14	42	GPIO 14 (PWM)	DDM_MUX2_FLIP	DDM_MUX2_FLIP		GPIO for I2C/USB2.0 Mux control
15	43	GPIO 15 (PWM)	DDM_MUX2_EN	DDM_MUX2_EN		
16	48	GPIO16 (PP_EXT1)	PP3_HVE_EN	PP3_HVE_EN		
17	49	GPIO17 (PP_EXT2)	PP4_HVE_EN	-		
18	50	GPIO18 (C1_USB_P)	-	-		Resv I2C3/GPIO for external DP-USB3 Mux control
19	53	GPIO19 (C1_USB_N)	-	-		
20	54	GPIO20 (C2_USB_P)	-	-		
21	55	GPIO21 (C2_USB_N)	-	-		Resv for DDM_MUX1_USB_EN
	24	C1_CC1	Port1 CC	Port1 CC		Port 1 CC
	26	C1_CC2	Port1 CC	Port1 CC		
	45	C2_CC1	Port2 CC			Port 2 CC
	47	C2_CC2	Port2 CC			
-	6	ADCIN1	Buspower Config	Buspower Config		
-	10	ADCIN2 (I2C Add)	Pull Dn (0x20, 0x24)	Pull Dn (0x20, 0x24)		I2C Address config
-	27	I2C1_SCL (Master/Slave)	I2C1 for EC	I2C1 for EC		
-	28	I2C1_SDA (M/S)				
-	29	I2C1_IRQ (M/S)				
-	32	I2C2_SCL (Slave Only)	I2C2 for TR	I2C2 for TR		
-	33	I2C2_SDA (Slave)				
-	34	I2C2_IRQ (Slave)				



IC Device Marking=TPS65987DDJ

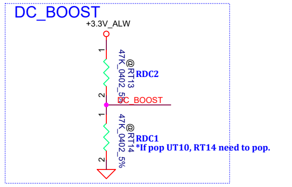


PARAMETER			VALUE
VCC (3.0V to 3.6V)			3.3 V
I²C support required in system (Yes/No)			No
AC Boost	R_{EQ}	Level	AC Boost Level 2: R_{EQ} = 3.83 K
	0 Ω	0	
	1.69 k ±1%	1	
	3.83 k ±1%	2	
	DNI	3	

Table 3. Design Parameters (continued)

PARAMETER				VALUE
DC Boost	R_{DC1}	R_{DC2}	Level	Mid DC Level: R_{DC1} = DNI R_{DC2} = DNI
	22 kΩ - 47 kΩ	Do Not Install (DNI)	40 mV Low DC Boost	
	DNI	DNI	60 mV Mid DC Boost	
	DNI	22 kΩ - 47 kΩ	80 mV High DC Boost	

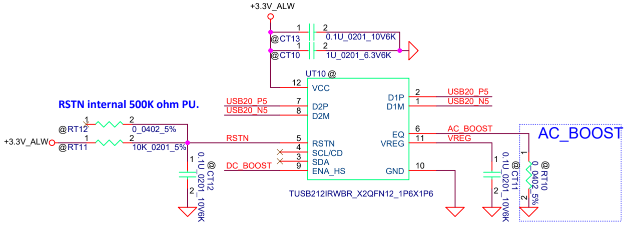
DC_BOOST



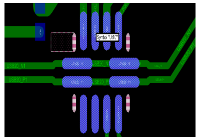
*If pop UT10, RT14 need to pop.

RSTN internal 500K ohm PU.

AC_BOOST

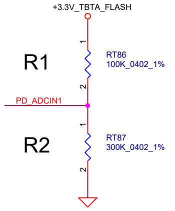


UT10 layout placement



BUSPOWER Config

BP_NoWait value 0.7~0.78



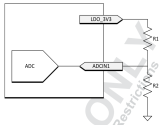
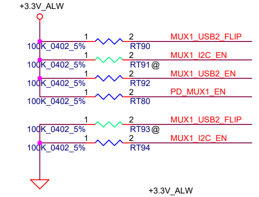


Figure 20. ADCIN1 Resistor Divider

Table 5. Boot Mode Pin Strapping

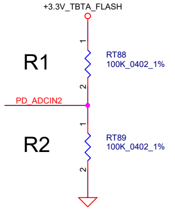
SPI_MISO	ADCIN1 DIV = R2/(R1+R2)(1)		Dead Battery Mode	Device Configuration
	DIV MIN	DIV MAX		
1	0.00	0.18	BP_NoResponse	Safe Configuration
1	0.20	0.28	BP_WaitFor3V3_Internal	Safe Configuration
1	0.30	0.38	BP_ECWait_Internal	Infinite Wait
1	0.40	0.48	BP_WaitFor3V3_External	Safe Configuration
1	0.50	0.58	BP_ECWait_External	Infinite Wait
1	0.60	1.00	BP_NoWait	Safe Configuration
0	0.10	0.18	BP_NoResponse	Configuration 1
0	0.20	0.28	BP_NoWait	Configuration 2
0	0.30	0.38	BP_ECWait_Internal	Infinite Wait
0	0.40	0.48	BP_NoWait	Configuration 3
0	0.50	0.58	BP_ECWait_External	Infinite Wait
0	0.60	0.68	BP_NoWait	Configuration 4
0	0.70	0.78	BP_NoWait	Reserved
0	0.80	0.88	BP_NoResponse	Reserved
0	0.90	1.00	BP_NoWait	Configuration 5

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.



Need CHECK

I2C Address Divider:010b



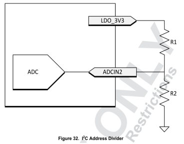


Figure 32. I²C Address Divider

Table 4. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]
DIV_min	DIV_max	I2C_ADDR_DECODE
Short ADCIN2 to GND		000b
0.20	0.38	001b
0.40	0.58	010b
Short ADCIN2 to LDO_3V3		011b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

INA/B ,OUTA/B ports are I / O

I2C to PD for DELL docking fireware program

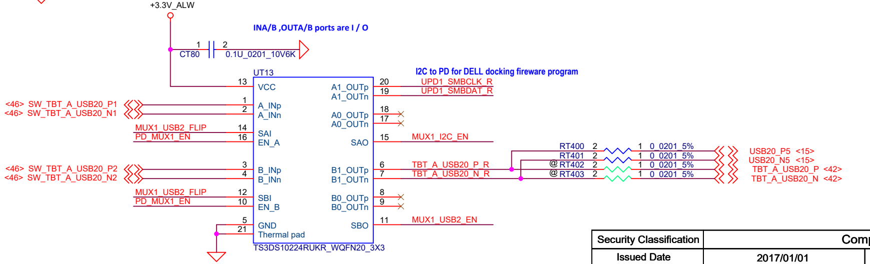


Table 1. Enable and Disable Function Table

ENA	ENB	INA	INB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Enabled	Hi-Z	Hi-Z	Enabled	Enabled
1	0	Enabled	Hi-Z	Enabled	Enabled	Hi-Z	Hi-Z
1	1	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

Table 6. Complete Function Table

SAI	SBI	SA0	SBO	OUTA0	OUTA1	OUTB0	OUTB1	FUNCTIONAL MODE	
0	0	0	0	INB	—	INA	—	Crosspoint, 1-channel 1:4 mux	
0	0	0	1	INB	—	—	INA	1-channel 1:4 mux	USB only on SW_TBT_A_USB20_P1/N1
0	0	1	0	—	INB	INA	—	1-channel 1:4 mux	
0	0	1	1	—	INB	—	INA	1-channel 1:4 mux	USB on SW_TBT_A_USB20_P1/N1 DDM on SW_TBT_A_USB20_P2/N2
0	1	0	0	INB	—	INA	—		
0	1	0	1	INB	—	—	INA		
0	1	1	0	—	INB	INB	—		
0	1	1	1	—	INB	—	INB		
1	0	0	0	INA	—	INA	—	Fan-out 1:2 configuration	
1	0	0	1	INA	—	—	INA	Fan-out 1:2 configuration	
1	0	1	0	—	INA	INA	—	Fan-out 1:2 configuration	
1	0	1	1	—	INA	—	INA	Fan-out 1:2 configuration	
1	1	0	0	INA	—	INB	—	Crosspoint, 2-channel 1:2 mux, 1-channel 1:4 mux	
1	1	0	1	INA	—	—	INB	2-channel 1:2 mux,1-channel 1:4 mux	USB only on SW_TBT_A_USB20_P2/N2
1	1	1	0	—	INA	INB	—	2-channel 1:2 mux,1-channel 1:4 mux	
1	1	1	1	—	INA	—	INB	2-channel 1:2 mux,1-channel 1:4 mux	USB on SW_TBT_A_USB20_P2/N2 DDM on SW_TBT_A_USB20_P1/N1

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Size	Document Number	Rev
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Title *Reserve Type-C_PD Power*

Size B Document Number *LA-J272P* Rev 0.2

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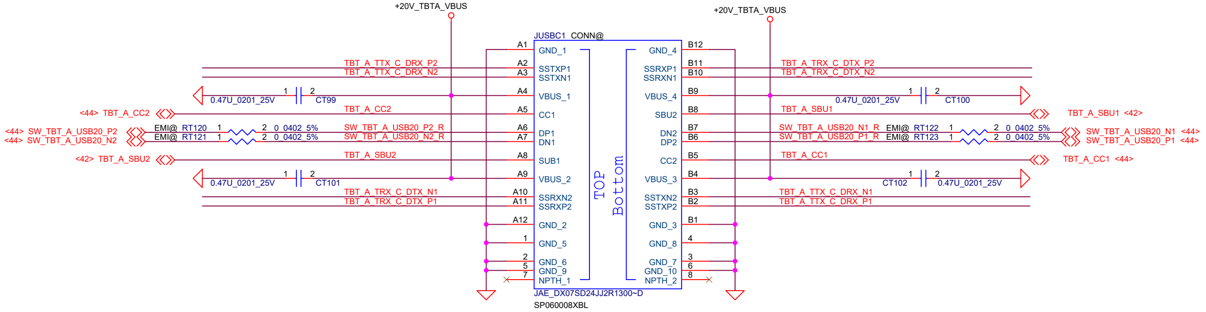
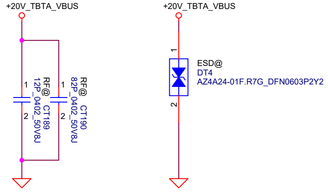


to be change to LTCX0095NBL

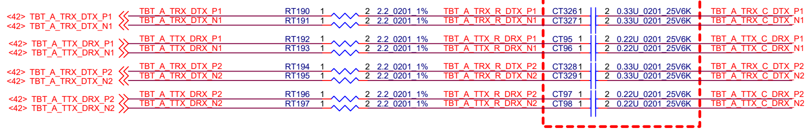
DX07SD24JJ4R1100

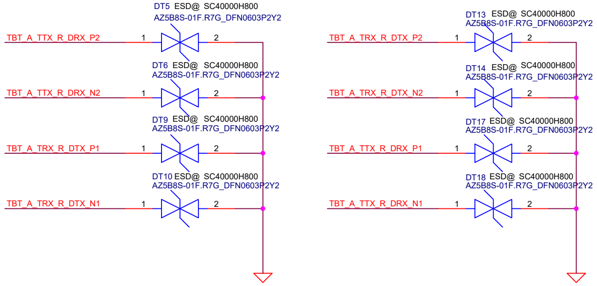
Vinafix.com



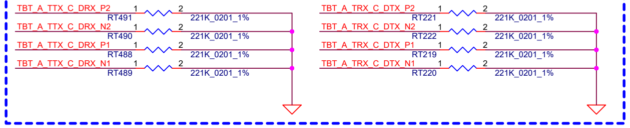
Place holder for future VBUS-short fix (reduce current surge)

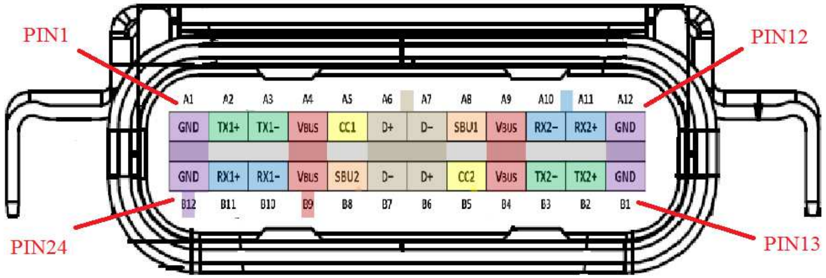
AC coupling is recommended for VBUS-short protection on SSTX/SSRX lines. If not needed, place 0 Ohm resistor instead.





Discharge SSTX/SSRX resistors - must be placed if 330nF cap is being used.





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TYPE-C_Port2 (2/2)

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D

C

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B

A

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Size
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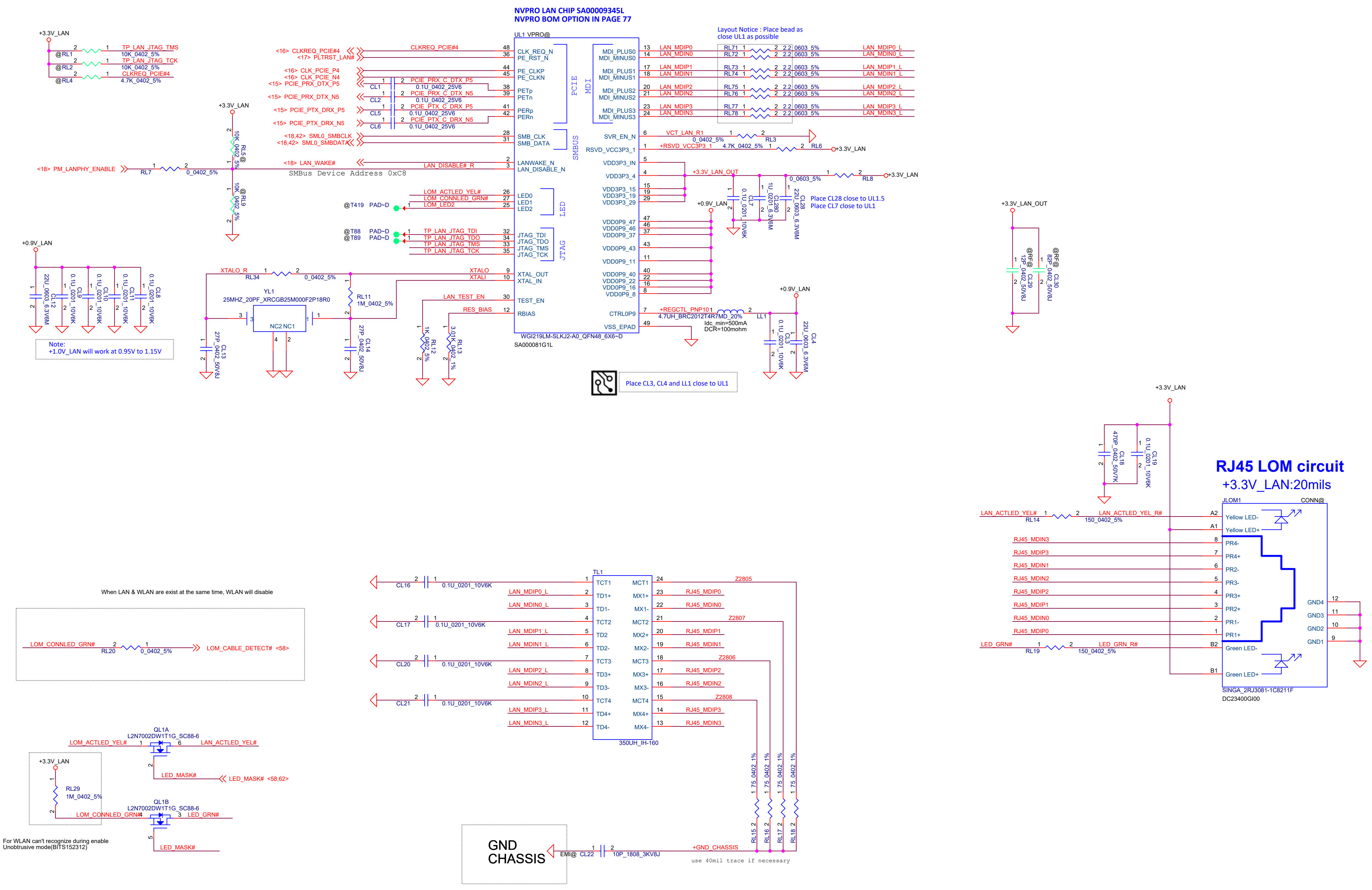

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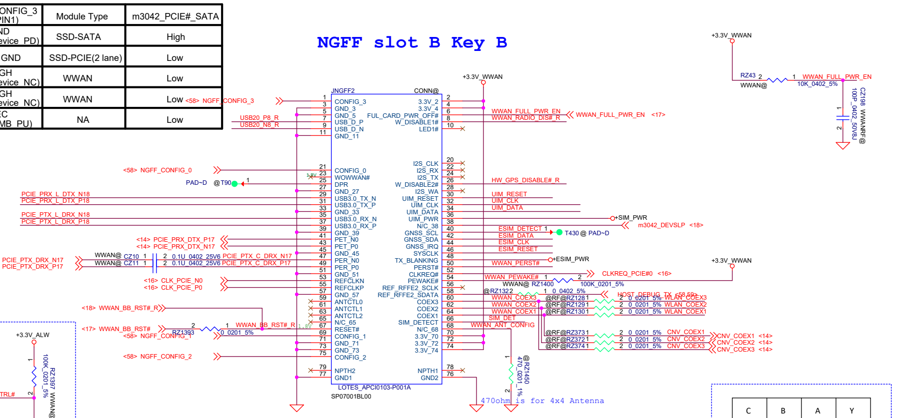
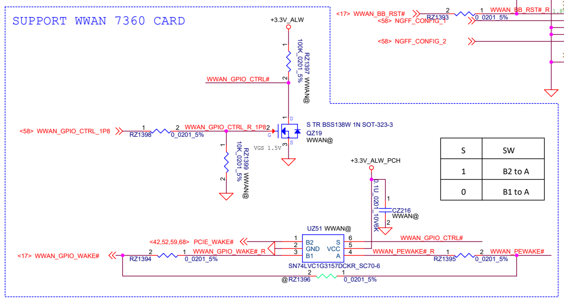
STATE #	CONFIG_0 (PIN21)	CONFIG_1 (PIN69)	CONFIG_2 (PIN75)	CONFIG_3 (PIN1)	Module Type	m3042_PCIE#_SATA
0	GND	GND (PEDET_PD)	GND	GND (device_PD)	SSD-SATA	High
1	GND	HIGH (PEDET_NC)	GND	GND	SSD-PCIE(2 lane)	Low
8	GND (device_PD)	GND (device_PD)	HIGH (device_NC)	HIGH (device_NC)	WWAN	Low
	GND (device_PD)	GND (device_PD)	GND (device_PD)	HIGH (device_NC)	WWAN	Low
15	EC (MB_PU)	EC (MB_PU)	EC (MB_PU)	EC (MB_PU)	NA	Low

NGFF slot B Key B

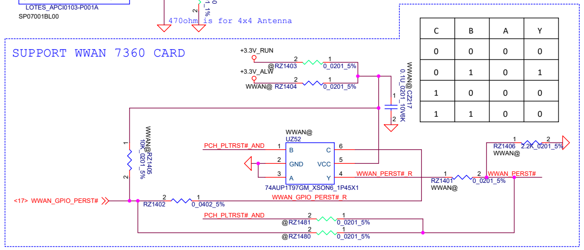


SUPPORT WWAN 7360 CARD



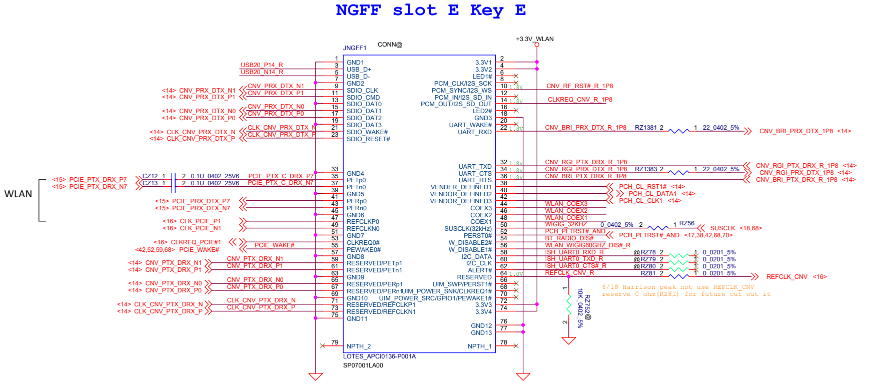
S	SW
1	B2 to A
0	B1 to A

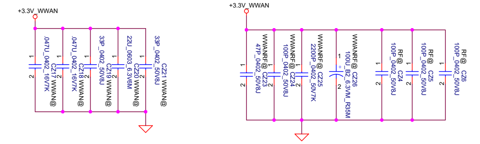
SUPPORT WWAN 7360 CARD

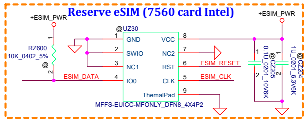


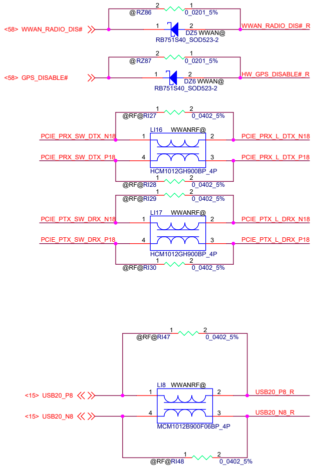
C	B	A	Y
0	0	0	0
0	1	0	1
1	0	0	0
1	1	0	0

NGFF slot E Key E

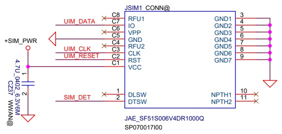


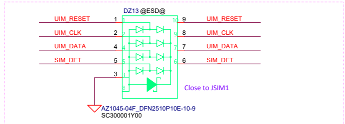


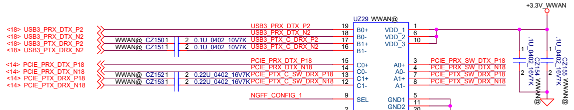




SIM Card Push-Push

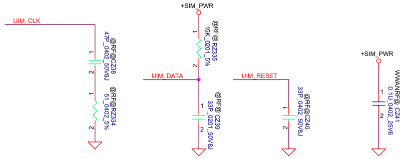


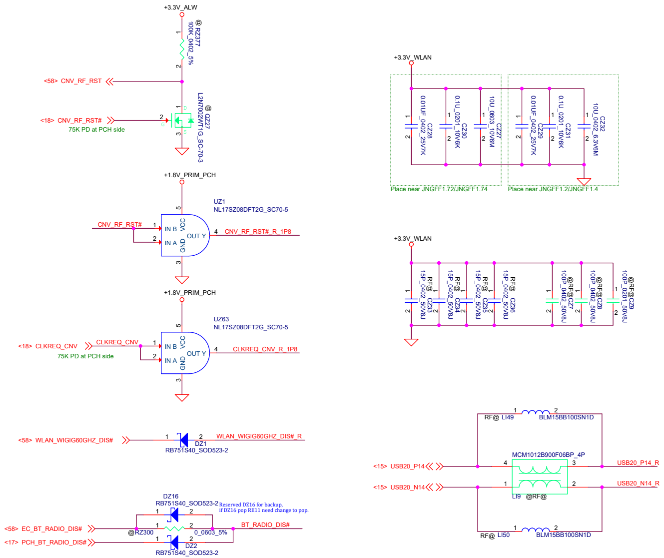




Function	SEL	OEn
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

main PERICOM SA00006EJ00
S IC PI3PCIE3212ZBEX TQFN 20P MUX SW
2nd TI SA00009A100
S IC HD3SS3212RKSR VQFN 20P MUX/DEMUX SW





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Title ***NGFF Card***

Size D Document Number ***LA-J272P*** Rev 0.2

Date: Friday, October 25, 2019 Sheet 52 of 108

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Date: Friday, October 25, 2019
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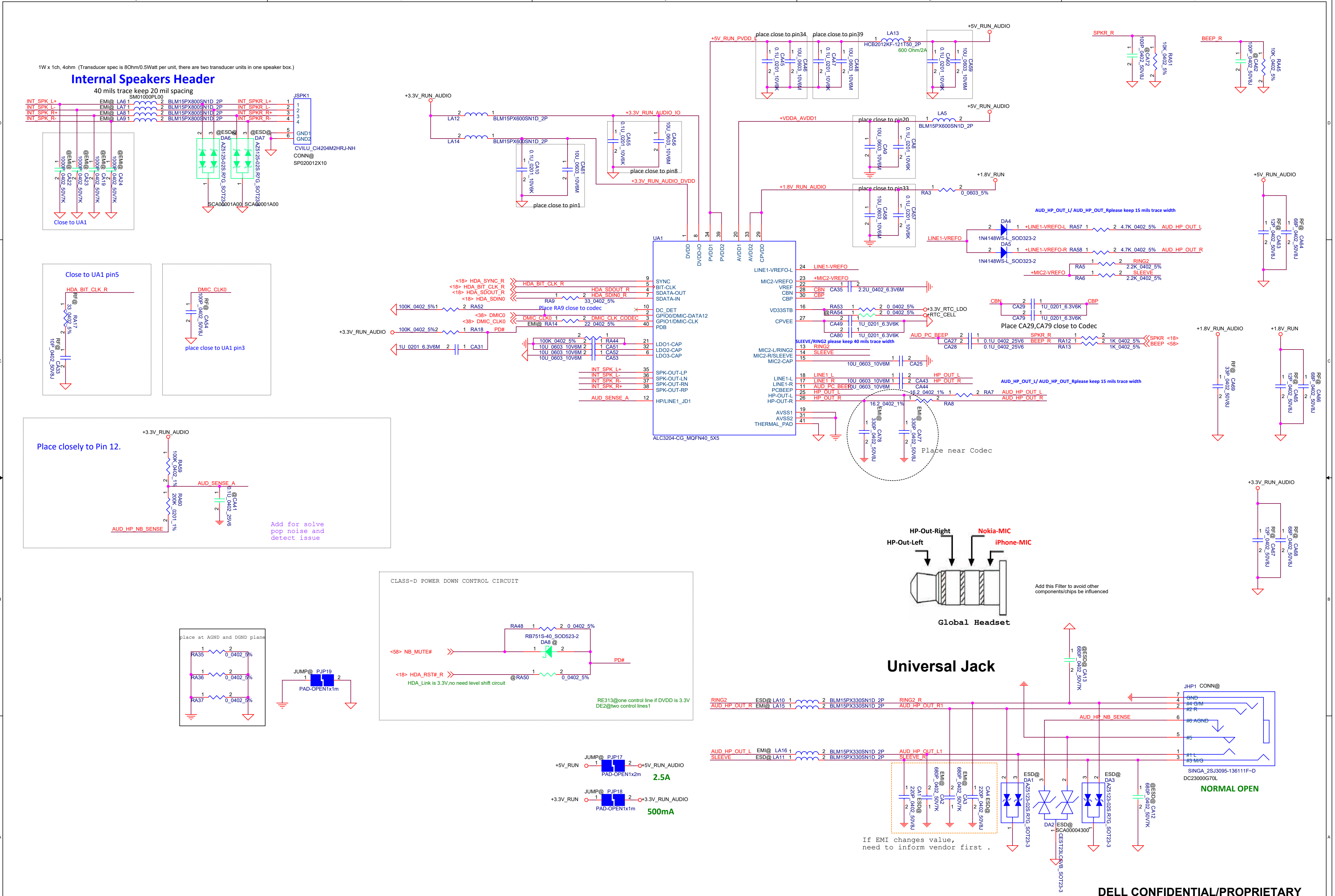

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Title	Codec ALC3204		
Size	Document Number LA-J272P		Rev 0.2
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Title
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Size
Document Number
LA-J272P
Rev
0.2

Date: Friday, October 25, 2019
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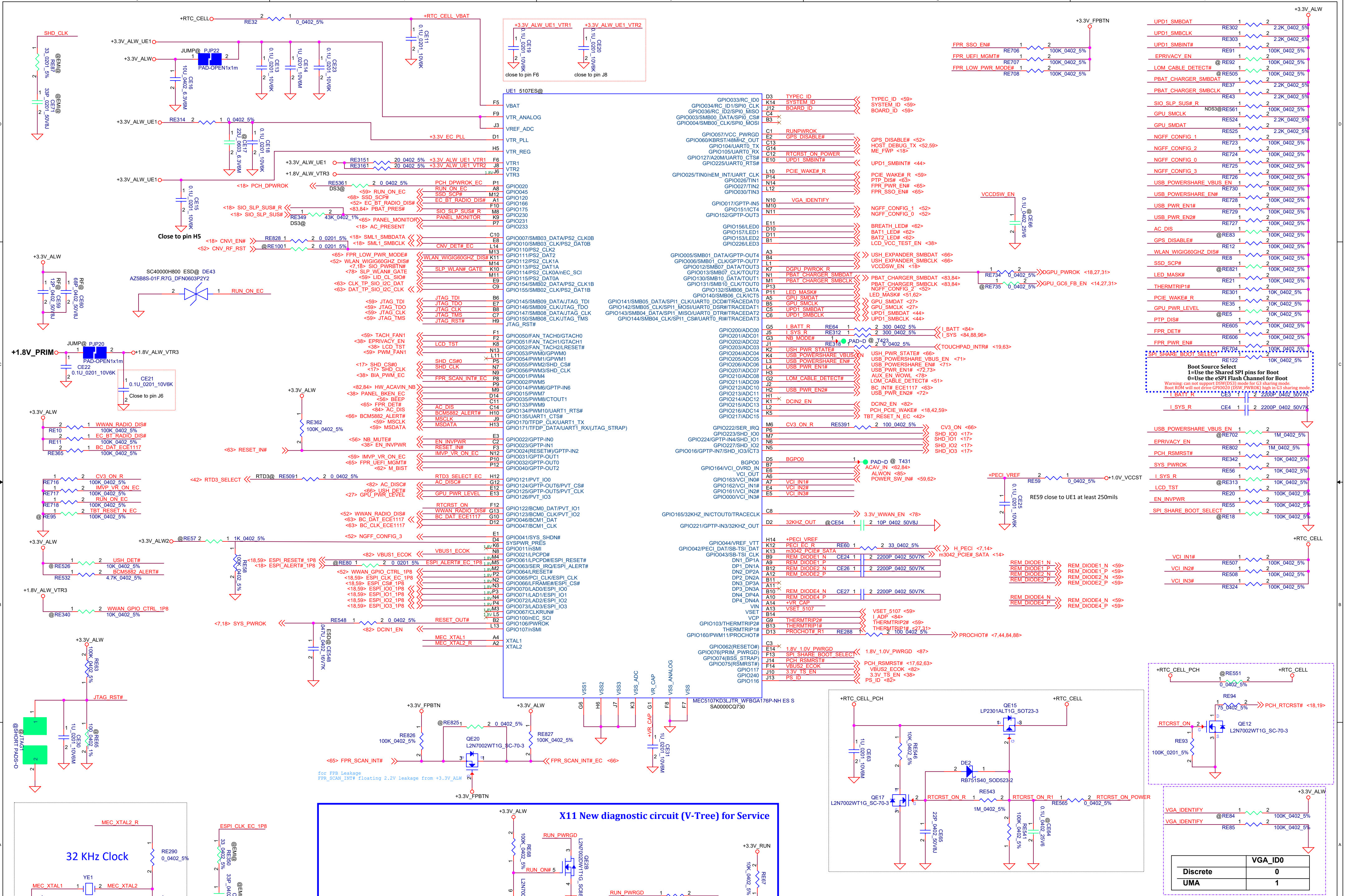

Boot Source Select
1=Use the Shared SPI pins for Boot
0=Use the eSPI Flash Channel for Boot
Warning: can not support DSW(DS3) mode for G3 sharing mode.
Boot ROM will not drive GPIO020 (DSW_PWROK) high in G3 sharing mode.

	VGA_ID0
Discrete	0
UMA	1

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Compal Electronics, Inc.

Title: *EC MEC5107*

Size: Custom | Document Number: *LA-J272P* | Rev: 0.2

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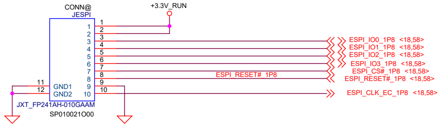
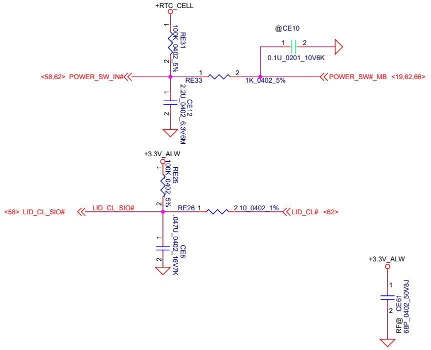
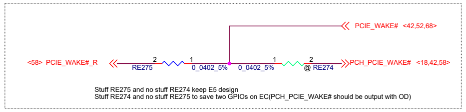
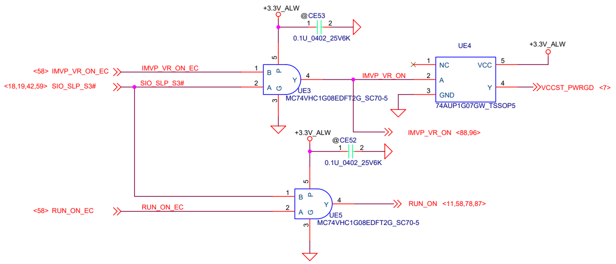
For BHMLK DSC

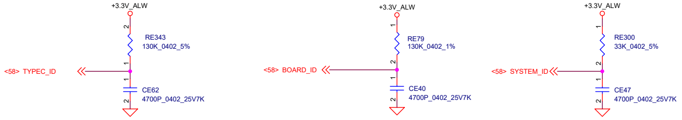






Stuff RE275 and no stuff RE274 keep E5 design
Stuff RE274 and no stuff RE275 to save two GPIOs on EC(PCH_PCIE_WAKE# should be output with OD)





	RE343	CE62	REV
	240K	4700p	Single Port ACE w/o TR
*	130K	4700p	Single Port ACE w/TR
	62K	4700p	Dual Port ACE w/o TR
	33K	4700p	Dual Port ACE w/TR
	8.2K	4700p	Dual Port ACE (w/TR +w/o TR)
	4.3K	4700p	
	2K	4700p	
	1K	4700p	

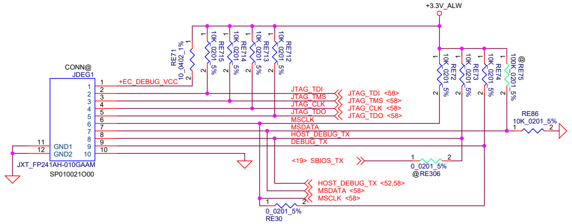
	RE79	CE40	REV
	240K	4700p	X00
*	130K	4700p	X01
	62K	4700p	X02
	33K	4700p	X03
	8.2K	4700p	
	4.3K	4700p	A00
	2K	4700p	
	1K	4700p	

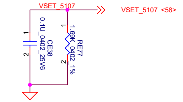
	RE300	**CE47**	**PANEL SIZE**
	240K	**4700p**	**11"**
	130K	**4700p**	**12"**
	62K	**4700p**	**13"**
*	**33K**	**4700p**	**14"**
	8.2K	**4700p**	**BR15 H**
	4.3K	**4700p**	**17"**
	2K	**4700p**	**BR15 P**
	1K	**4700p**	

PD_ACE_DET# rise time is measured from 5%~68%.

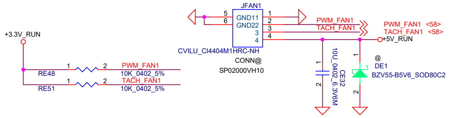
BOARD_ID rise time is measured from 5%~68%.

PANEL_ID rise time is measured from 5%~68%.





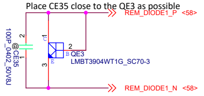
Rest=1.69K , Tp=97 degree

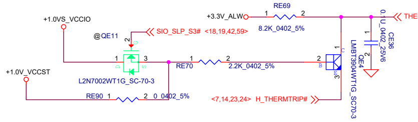


Thermal diode mapping

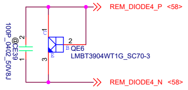
5107 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	2280 (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

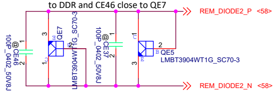




DP4/DN4 for Skin on
QE6, place QE6 close to
Vcore VR choke.



DN2a/DP2a for DDR on QE7, place QE7 close
to DDR and CE46 close to QE7



DP2/DN2 for 2280 on QE5, place QE5 close
to JNGFF3 and CE37 close to QE5

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Title *MEC5105 SUPPORT*

Size Custom Document Number *LA-J272P* Rev 0.2

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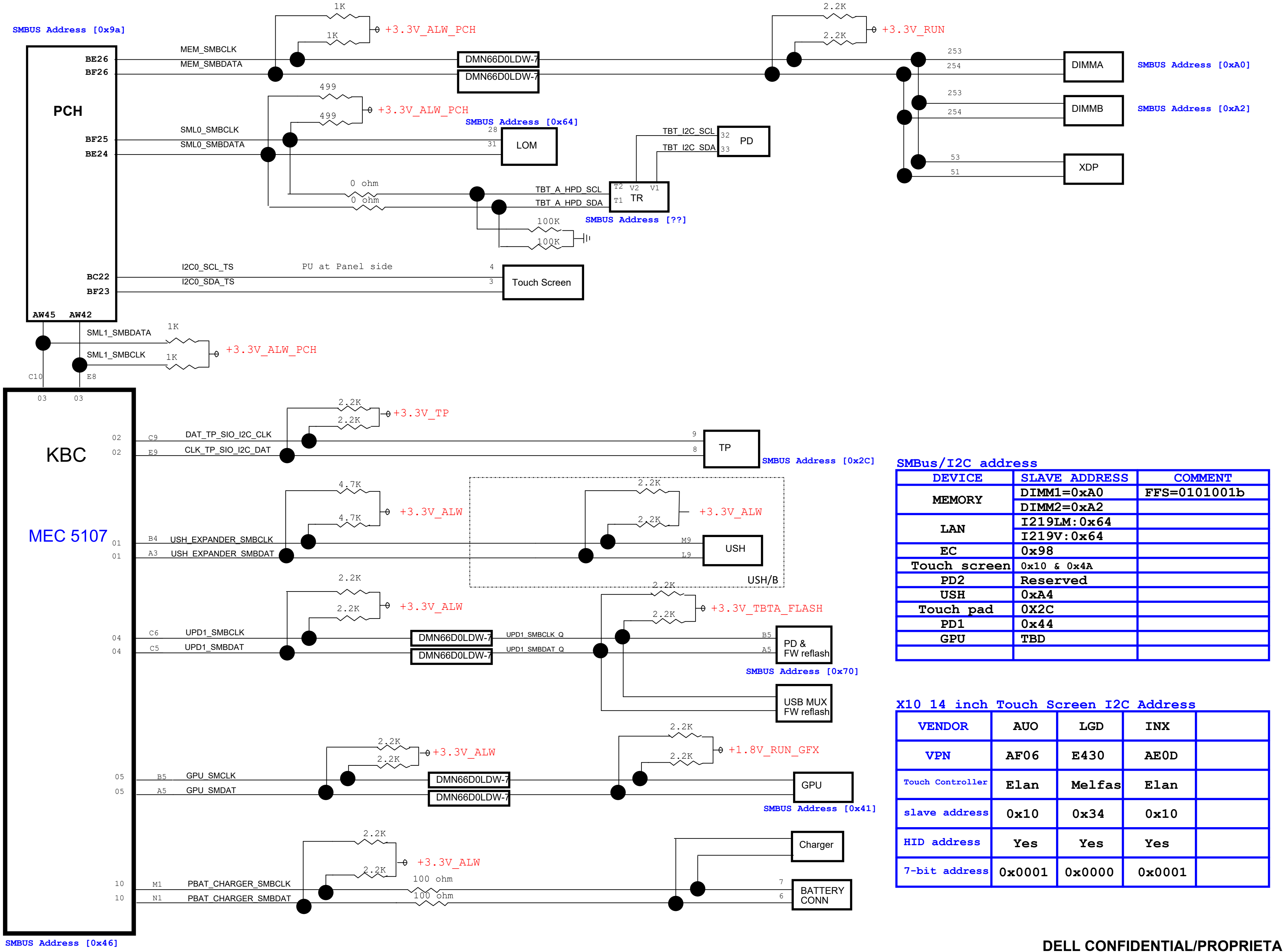

SMBus/I2C address

DEVICE	SLAVE ADDRESS	COMMENT
MEMORY	DIMM1=0xA0	FFS=0101001b
	DIMM2=0xA2	
LAN	I219LM:0x64	
	I219V:0x64	
EC	0x98	
Touch screen	0x10 & 0x4A	
PD2	Reserved	
USH	0xA4	
Touch pad	0X2C	
PD1	0x44	
GPU	TBD	

X10 14 inch Touch Screen I2C Address

VENDOR	AUO	LGD	INX	
VPN	AF06	E430	AE0D	
Touch Controller	Elan	Melfas	Elan	
slave address	0x10	0x34	0x10	
HID address	Yes	Yes	Yes	
7-bit address	0x0001	0x0000	0x0001	

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Title *SMbus Block Diagram*

Size B

Document Number *LA-J272P*

Rev 0.2

Date: Friday, October 25, 2019

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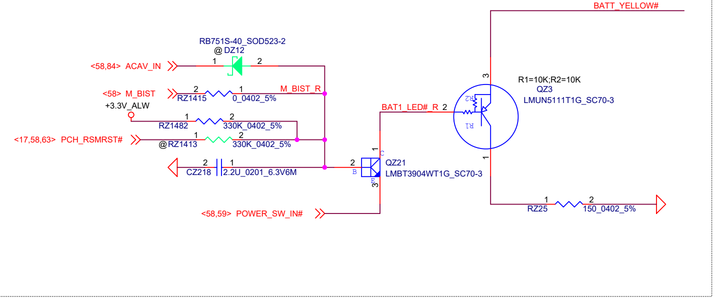
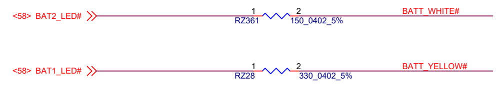
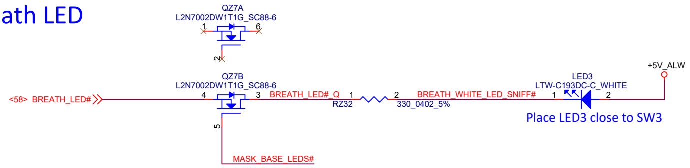


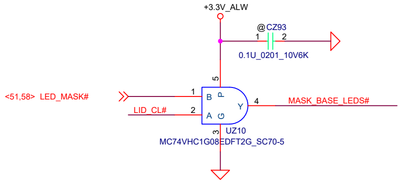
Battery LED



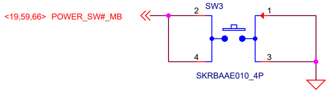
Breath LED



Place LED3 close to SW3

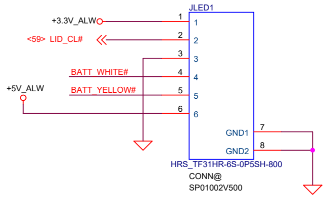


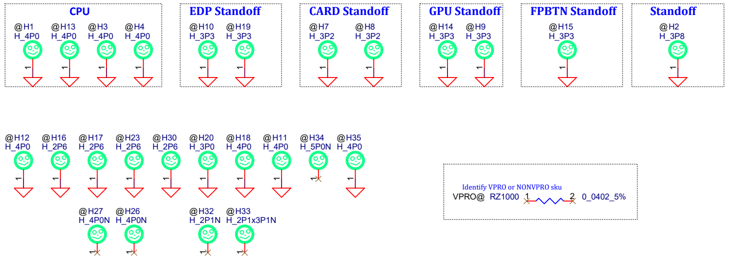
POWER & INSTANT ON SWITCH



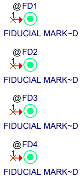
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

LED board CONN

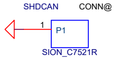




Fiducial Mark



TR crystal shielding can



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Title *PAD, LED*

Size C Document Number *LA-J272P* Rev 0.2

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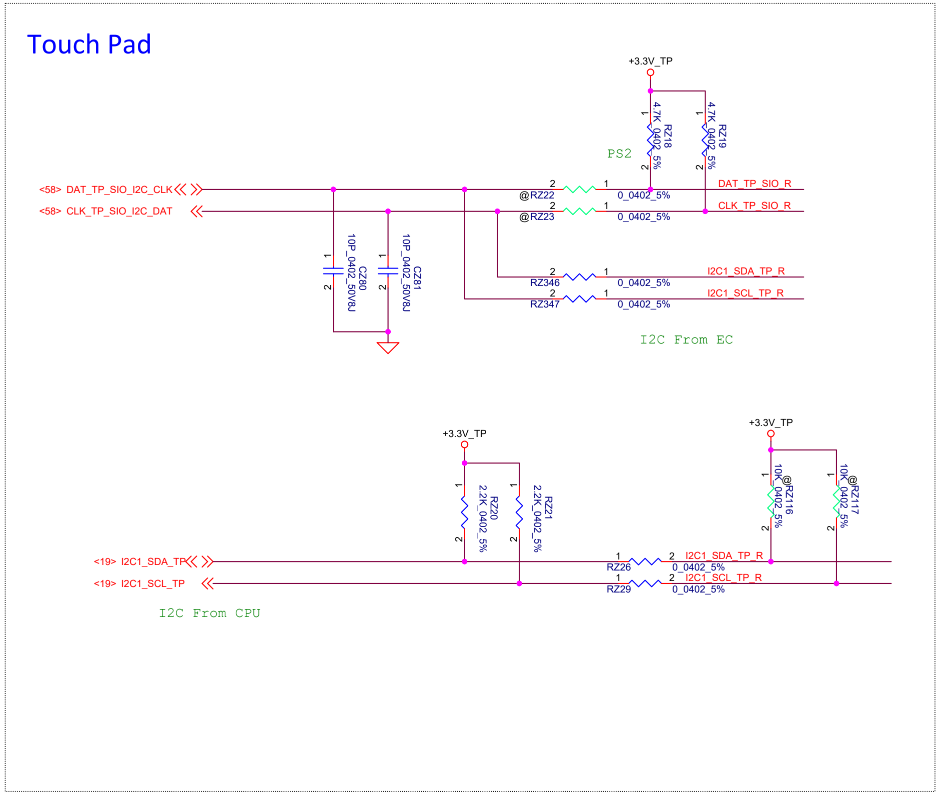
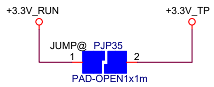
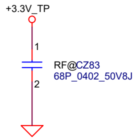
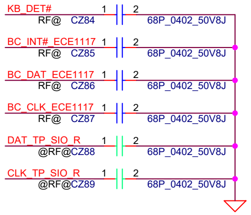
Touch Pad

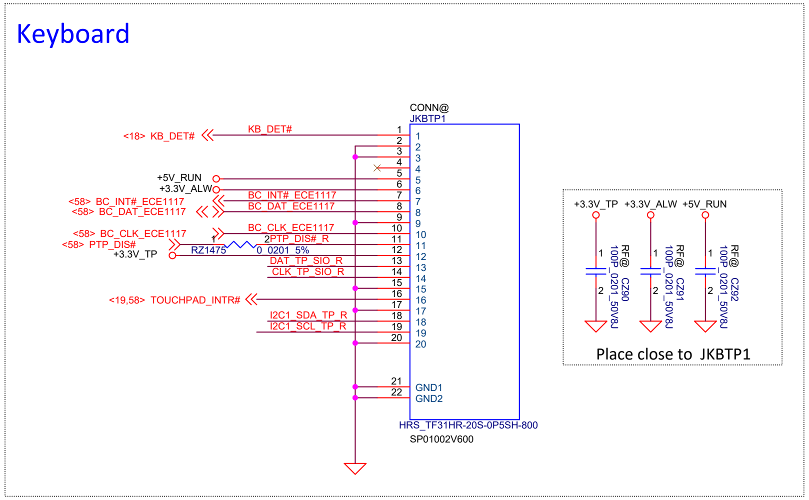




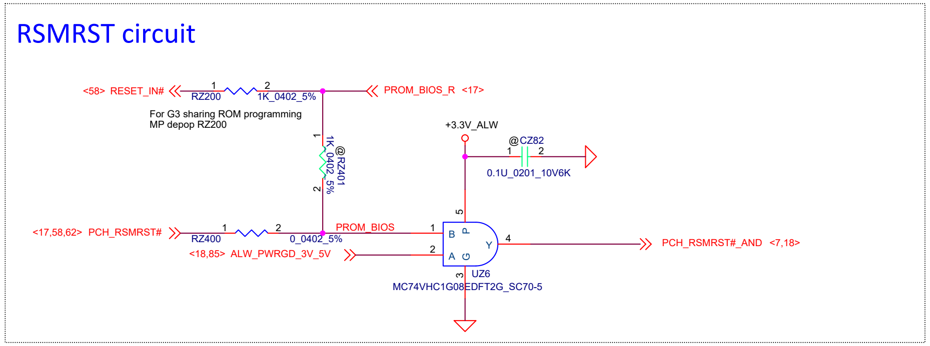




Keyboard



RSMRST circuit



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Title *Keyboard*

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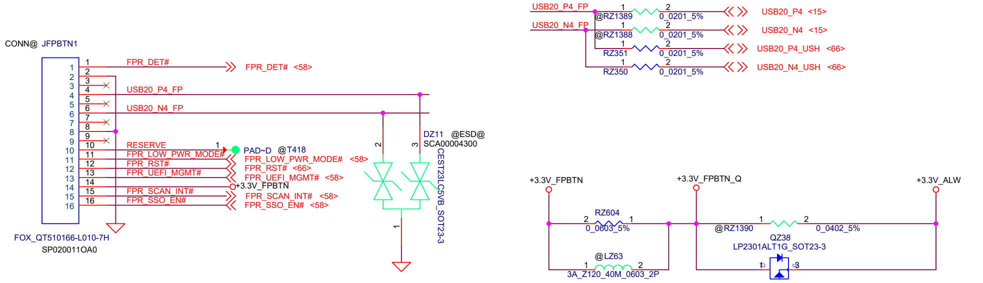
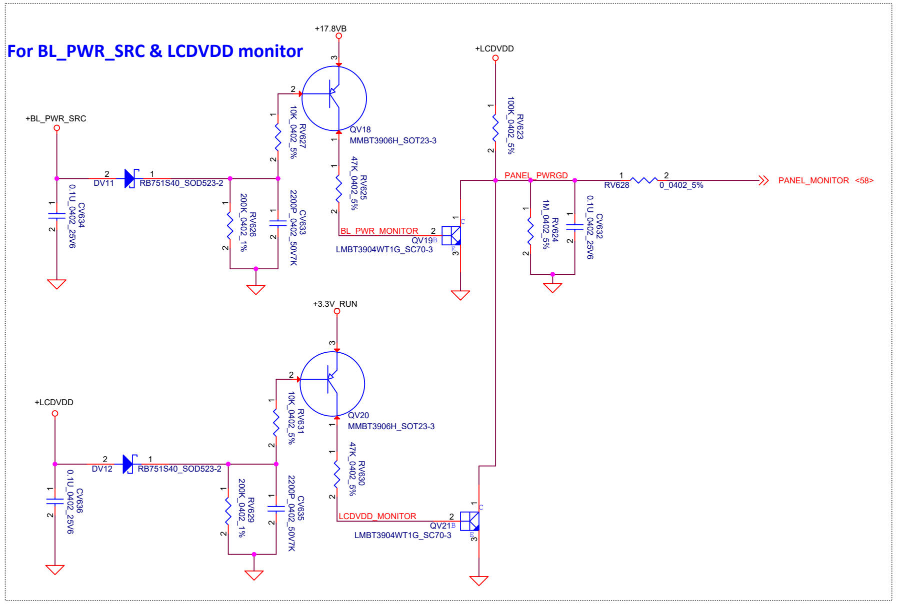
FP in PWR BUTTON connector



Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR DET(GND)	16

For BL_PWR_SRC & LCDVDD monitor



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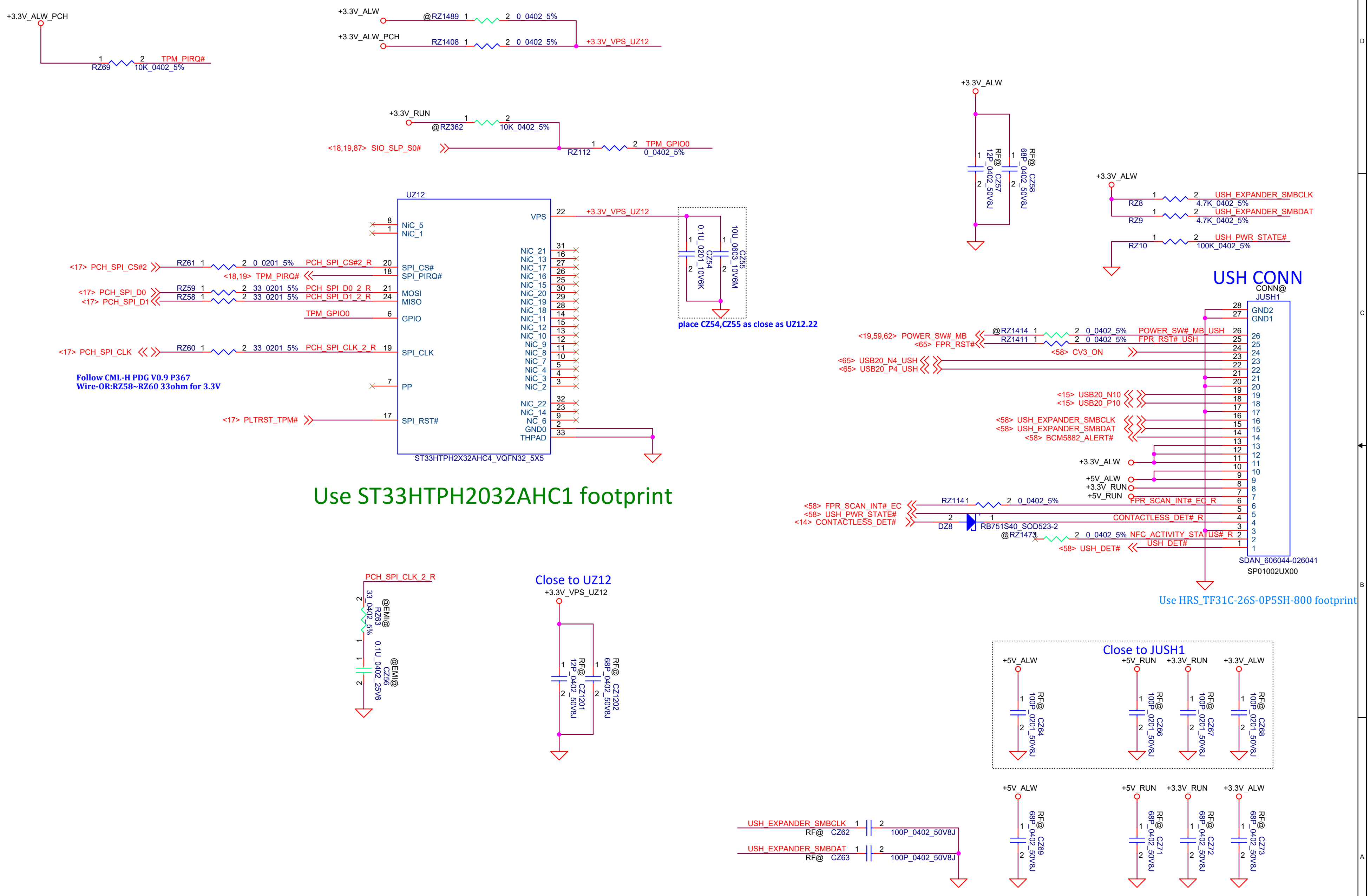

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Title	***USH & TPM***		
Size Custom	Document Number ***LA-J272P***		Rev 0.2
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Compal Electronics, Inc.

Title *Reserve HDD CONN*

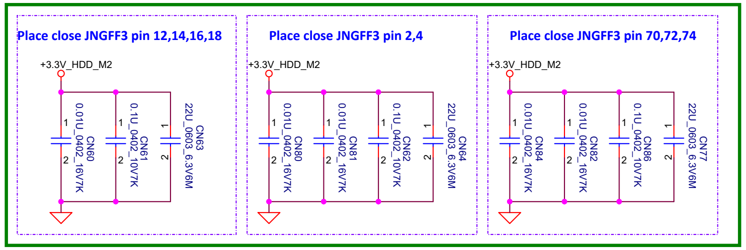
Size B

Document Number *LA-J272P*

Rev 0.2

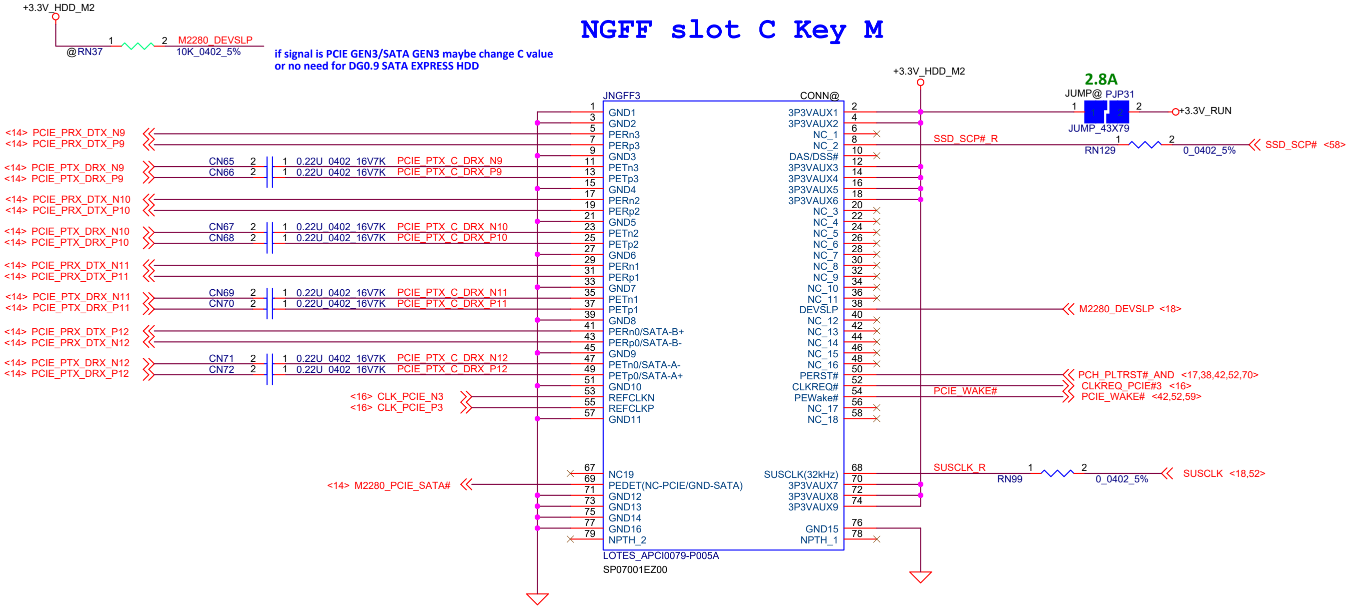
Date: Friday, October 25, 2019

Add Power Decoupling for support Intel Teton Glacier



2280 SSD

NGFF slot C Key M



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Compal Electronics, Inc.

Title
M2 2280 Socket

Size B
Document Number ***LA-J272P***
Rev 0.2

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Reserve

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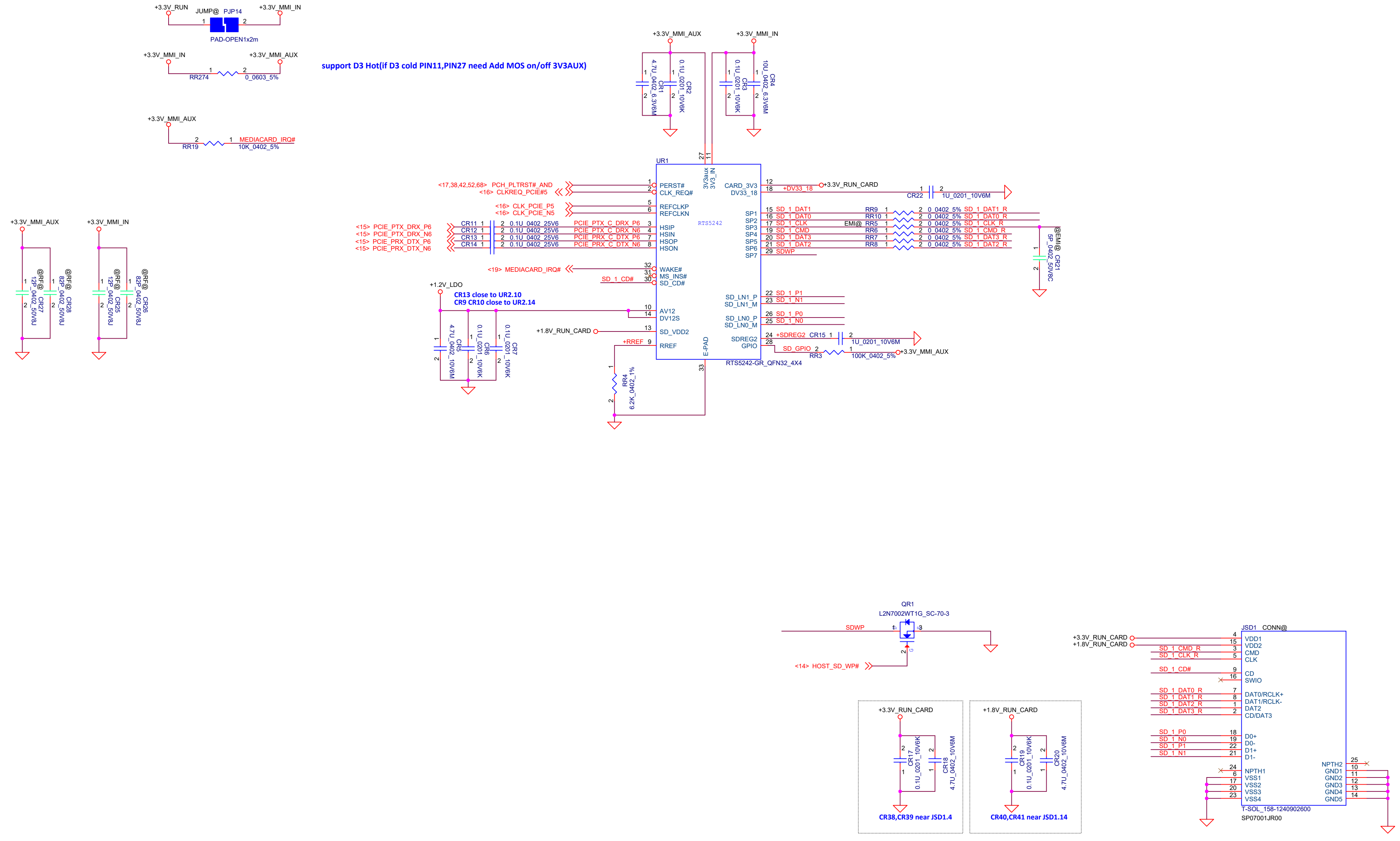

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Compal Electronics, Inc.

Title ***Card Reader***

Size	Document Number	Rev
C	***LA-J272P***	0.2

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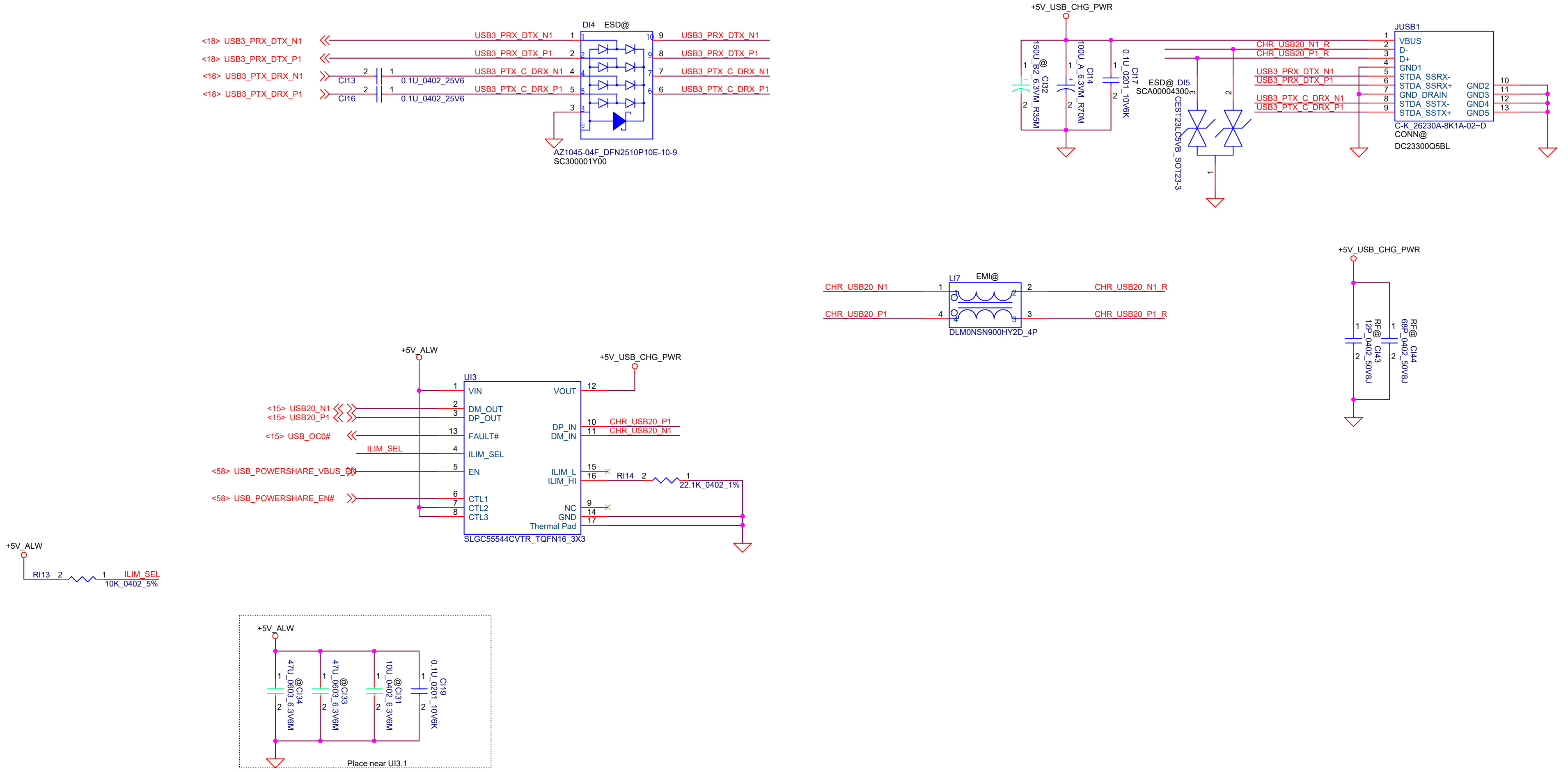
For PWR SW + Charger combine IC



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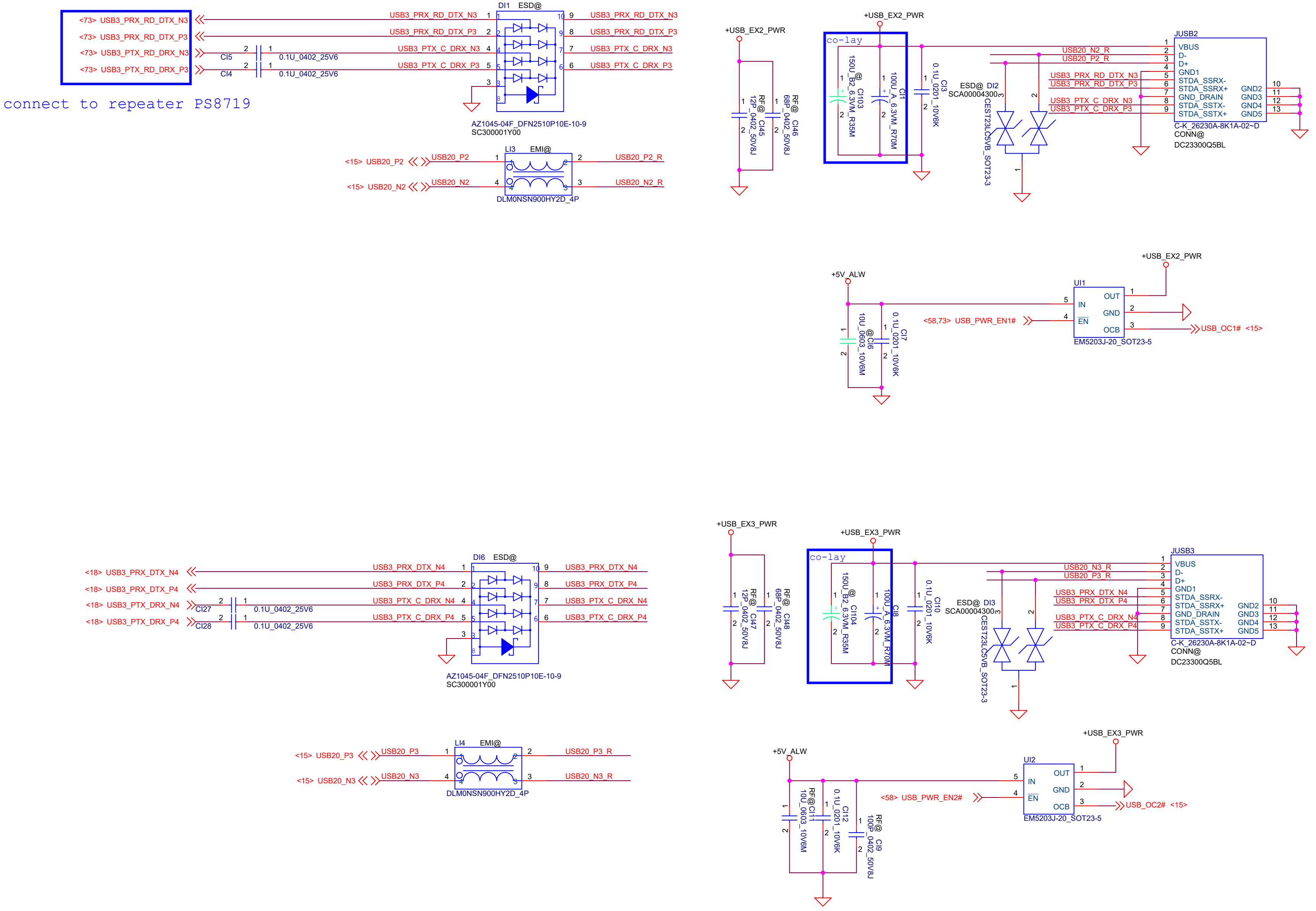
Compal Electronics, Inc.

Title ***USB SW***

Size	Document Number	Rev
B	***LA-J272P***	0.2

Date: Friday, October 25, 2019



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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title ***JUSB2&JUSB3***

Size B | Document Number ***LA-J272P*** | Rev 0.2

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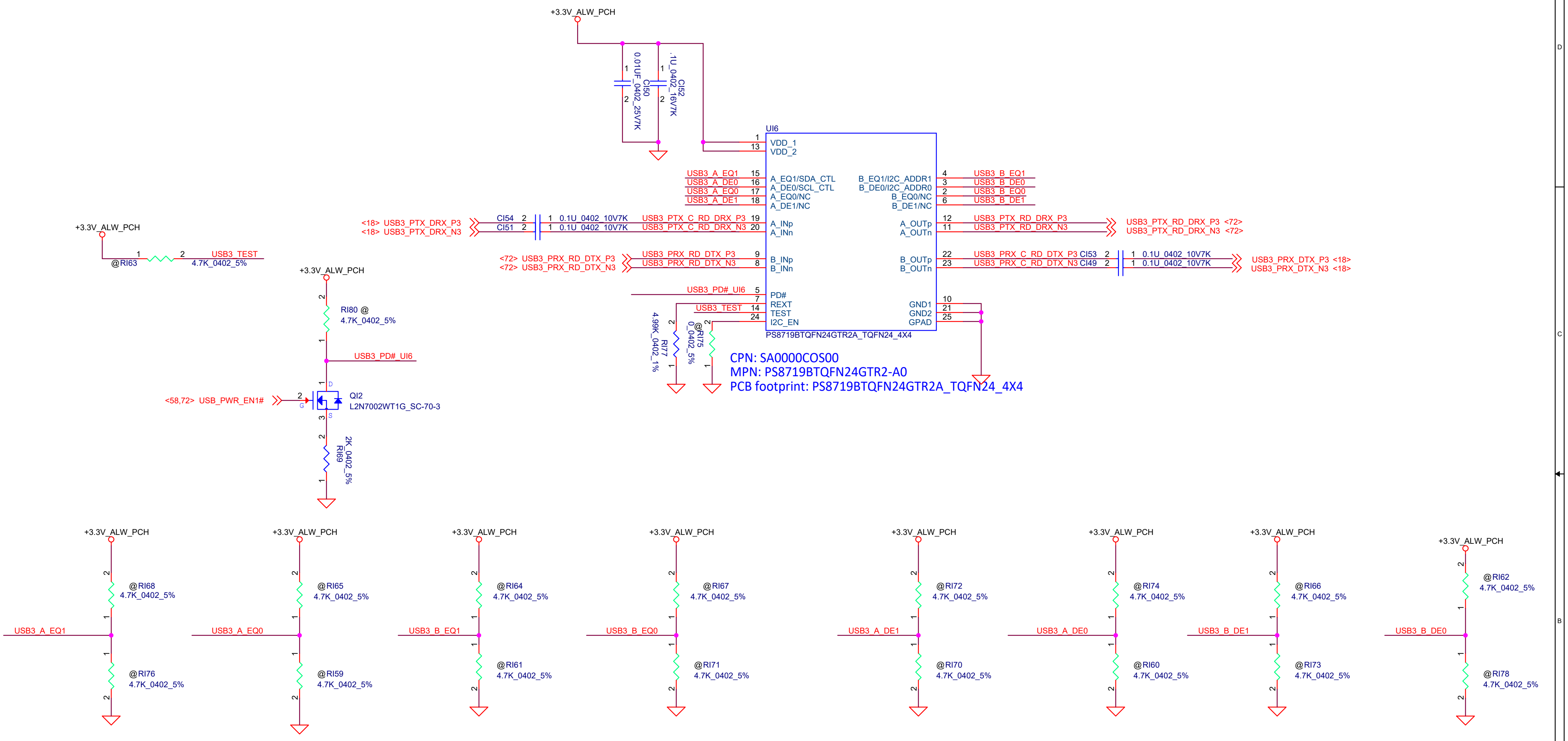
USB3_repeater_from_PS8713B_change_to_PS8719B

FOR LEFT JUSB2 USE



CPN: SA0000COS00
MPN: PS8719BTQFN24GTR2-A0
PCB footprint: PS8719BTQFN24GTR2A_TQFN24_4X4

Parade_PS8719B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A_DE&B_DE have internal pull-down 150k

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Compal Electronics, Inc.

Title
USB3.0 Repeater for JUSB3

Size: Custom
Document Number: ***LA-J272P***
Rev: 0.2
Date: Friday, October 25, 2019
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Compal Electronics, Inc.

Title

Reserve for USB

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FOR NVPRO LAN chip BOM OPTION

NVPRO@ UL1
WGI219V SLKJ4 A0 QFN
SA00009345L

EC Chip

5107NES@ UE1
MEC5107KD4LJTR_WFBGA176P-NH
SA0000CQ740

FOR 14HD VRAM BOM OPTION

VENDER	STRAP	Part Number			(Strap2,Strap1,Strap0)	H:RV239 L:RV240	H:RV237 L:RV238	H:RV235 L:RV236	
Samsung	0x3	K4G80325FC-HC25 SA00009TA3L	2GSAM@ UV17 K4G80325FC-HC25	2GSAM@ UV18 K4G80325FC-HC25	(L, H, H)	2GSAM@ RV240 100K_0402_5%	2GSAM@ RV237 100K_0402_5%	2GSAM@ RV235 100K_0402_5%	
Micron	0x9	MT51J256M32HF-80:B SA00009TI3L	2GMICR@ UV17 MT51J256M32HF-80:B	2GMICR@ UV18 MT51J256M32HF-80:B	(L, M, L)	2GMICR@ RV240 100K_0402_5%	2GMICR@ RV237 100K_0402_5%	2GMICR@ RV238 100K_0402_5%	2GMICR@ RV236 100K_0402_5%
Hynix	0xA	H5GC8H24AJR-R2C SA0000C171L	2GHYN@ UV17 H5GC8H24AJR-R2C	2GHYN@ UV18 H5GC8H24AJR-R2C	(L, M, H)	2GHYN@ RV240 100K_0402_5%	2GHYN@ RV237 100K_0402_5%	2GHYN@ RV238 100K_0402_5%	2GHYN@ RV235 100K_0402_5%

FOR 14HD VRAM X76

2GSAMX76@ ZZZ
ALT. GROUP PARTS VRAM SAM EDC42
X7670231LC3

2GMICRX76@ ZZZ
ALT. GROUP PARTS VRAM MICRON EDC42
X7670231LB1

2GHYNX76@ ZZZ
ALT. GROUP PARTS VRAM HYNIX EDC42
X7670231LB2

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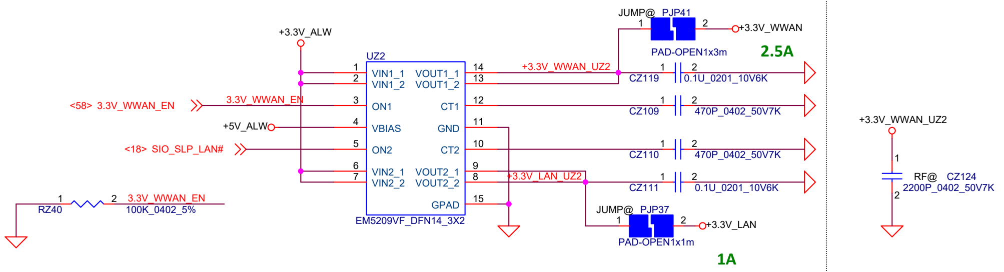
+3.3V_WWAN/+3.3V_LAN source



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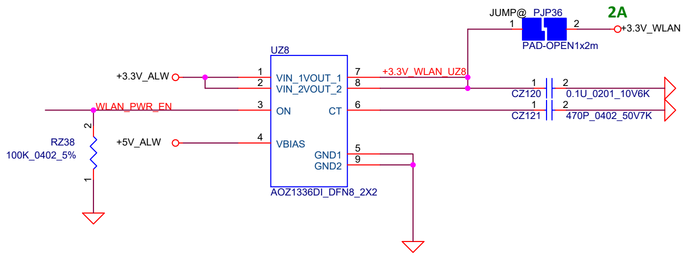
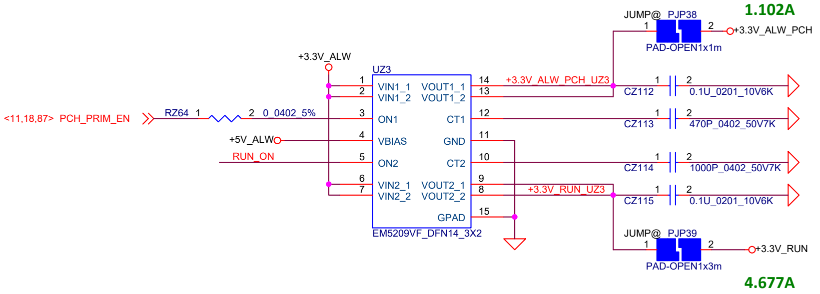
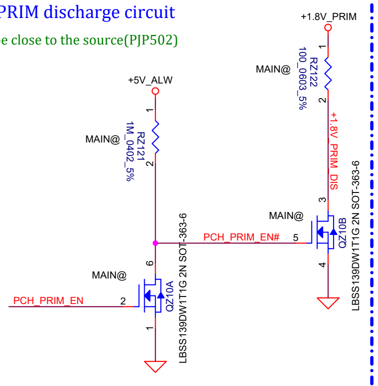


+3.3V_ALW_PCH/+3.3V_RUN source

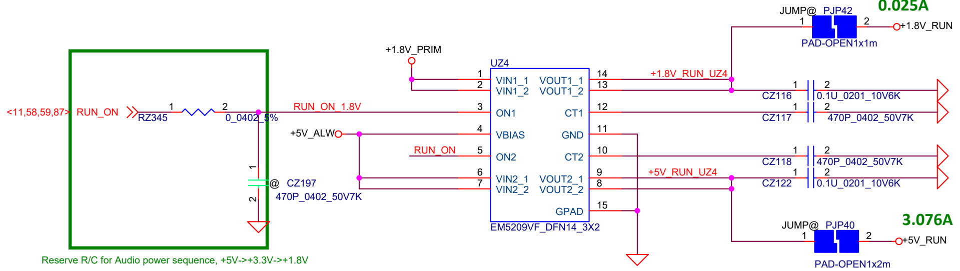


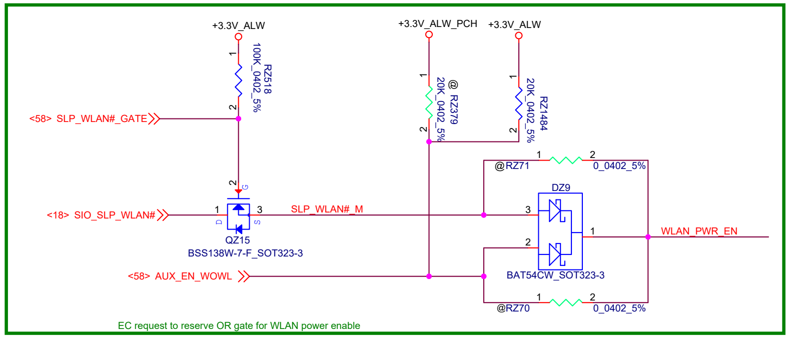
+1.8V_PRIM discharge circuit

Need to be close to the source(PJP502)



+5V_RUN/+1.8V_RUN source





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Compal Electronics, Inc.

Title ***Power control***

Size B

Document Number ***LA-J272P***

Rev 0.2

Date: Friday, October 25, 2019

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D D

C C

Reserve

B B

A A

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Title
Reserve for XDP/CMC/APS

Size
Document Number
LA-J272P
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D

C

Reserve

B

A

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Title
Google Debug & INAs

Size
Document Number
LA-J272P
Rev
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Date: Friday, October 25, 2019
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Compal Electronics, Inc.

Title
PWR-Block Diagram

Size
Document Number
LA-J272P
Rev
0.2

Date: Friday, October 25, 2019
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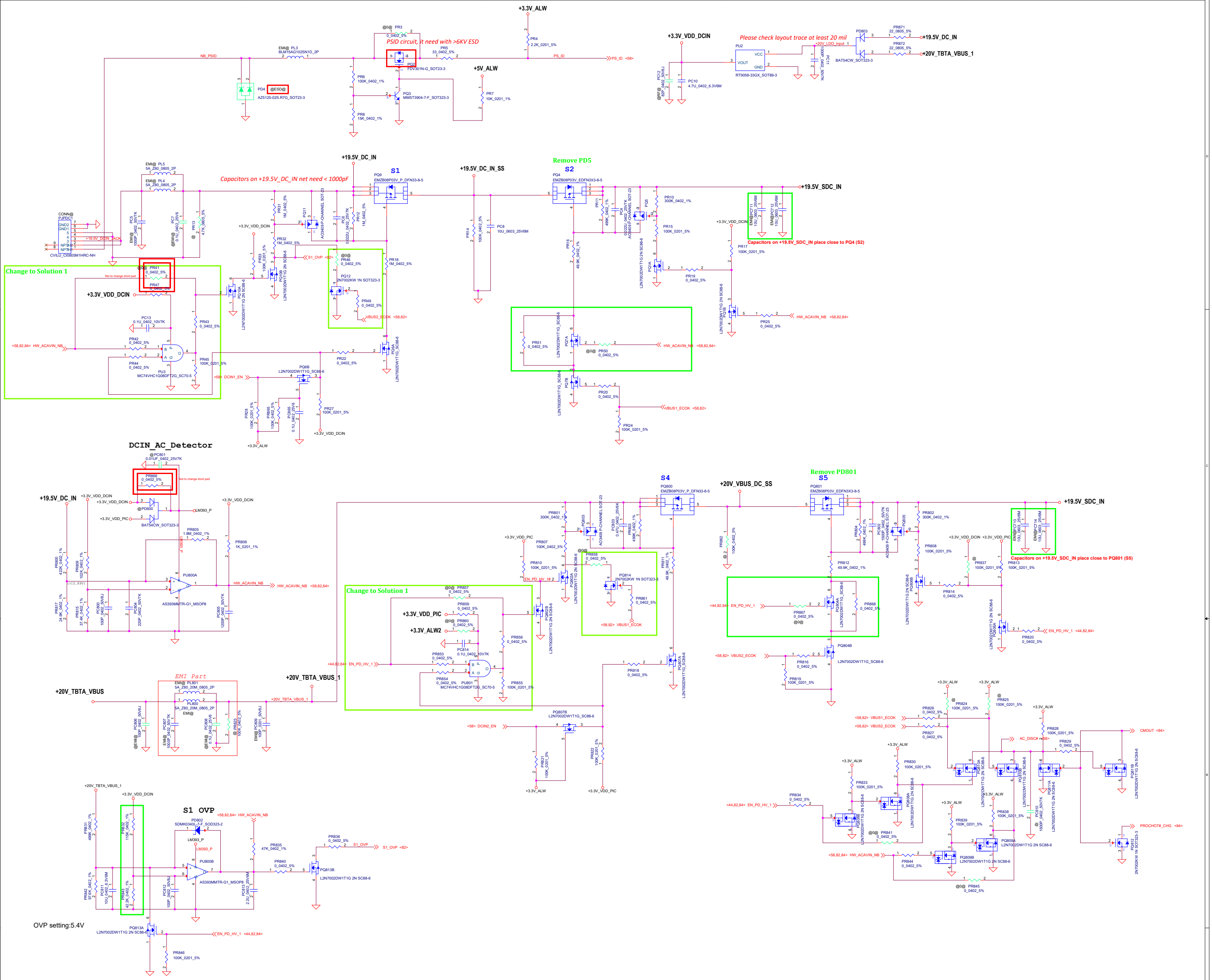

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	Compal Electronics, Inc.
Title	DC Connector/1Type-C PD Selector
Size	Document Number LA-J272P
Rev	0.2
Date:	Friday, October 25, 2019
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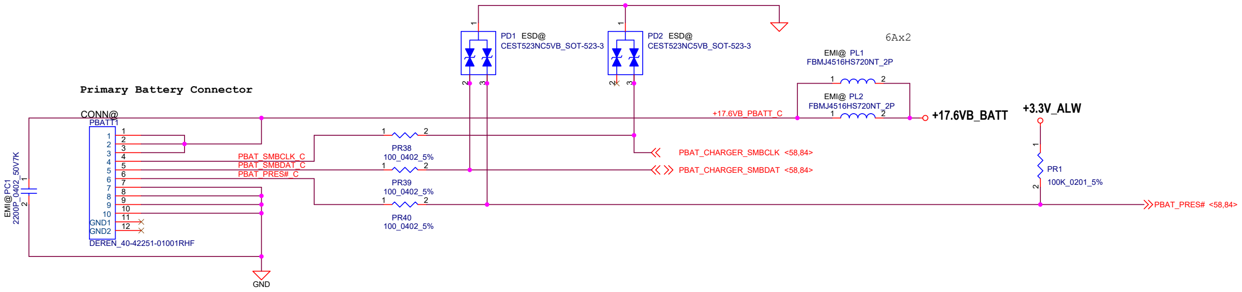
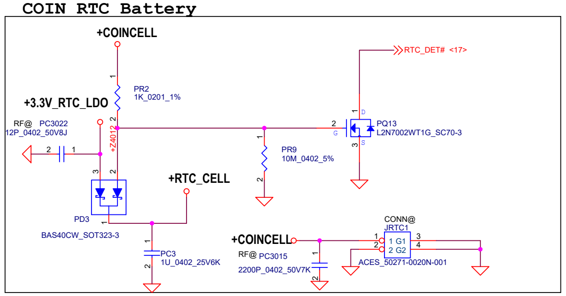
Primary Battery Connector



COIN RTC Battery



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Compal Electronics, Inc.

Title
Battery Connector/ RTC

Size
Document Number
LA-J272P
Rev
0.2

Date: Friday, October 25, 2019
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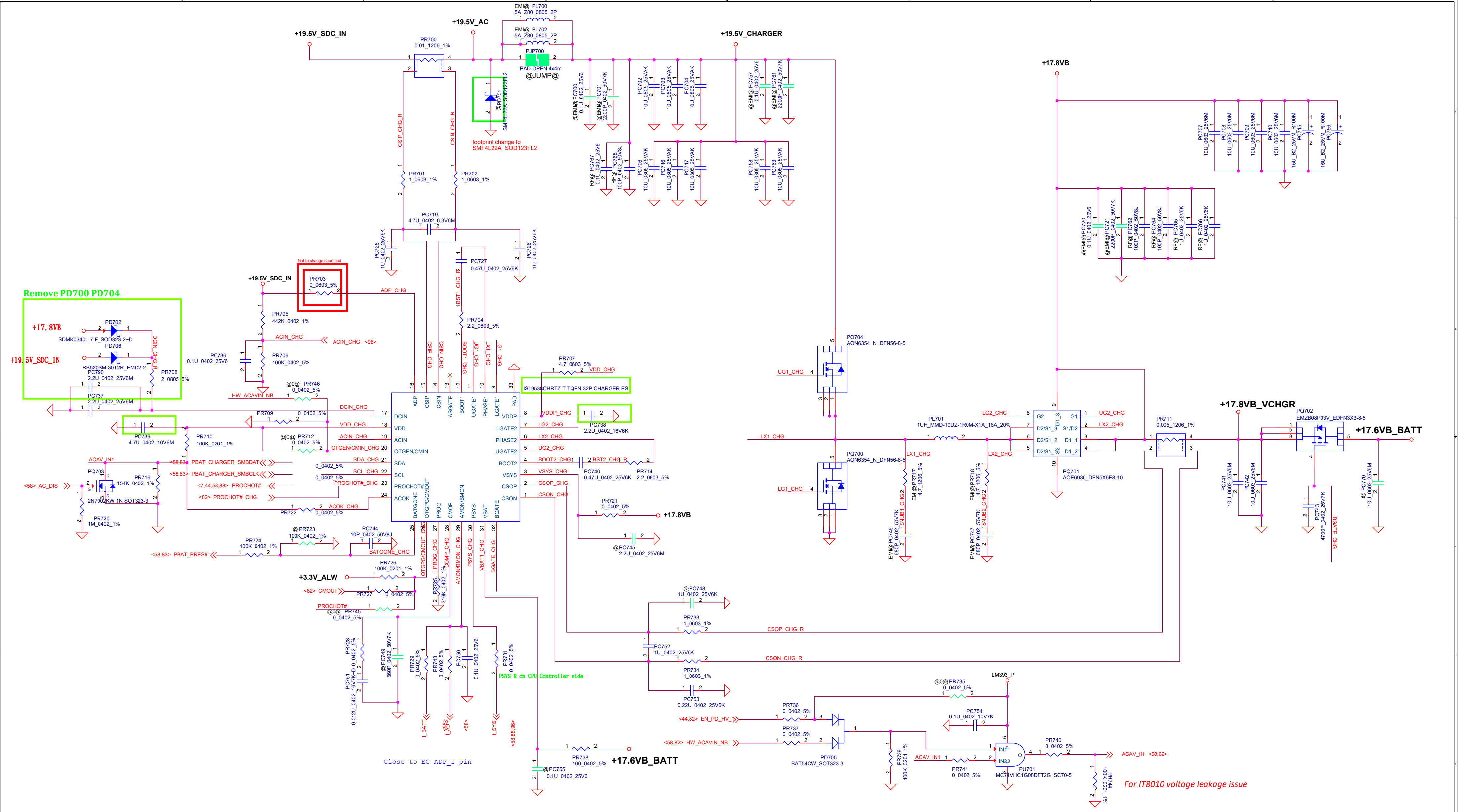

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Compal Electronics, Inc.

Title
Charger

Size
Document Number
LA-J272P
Rev
0.2

Date: Friday, October 25, 2019
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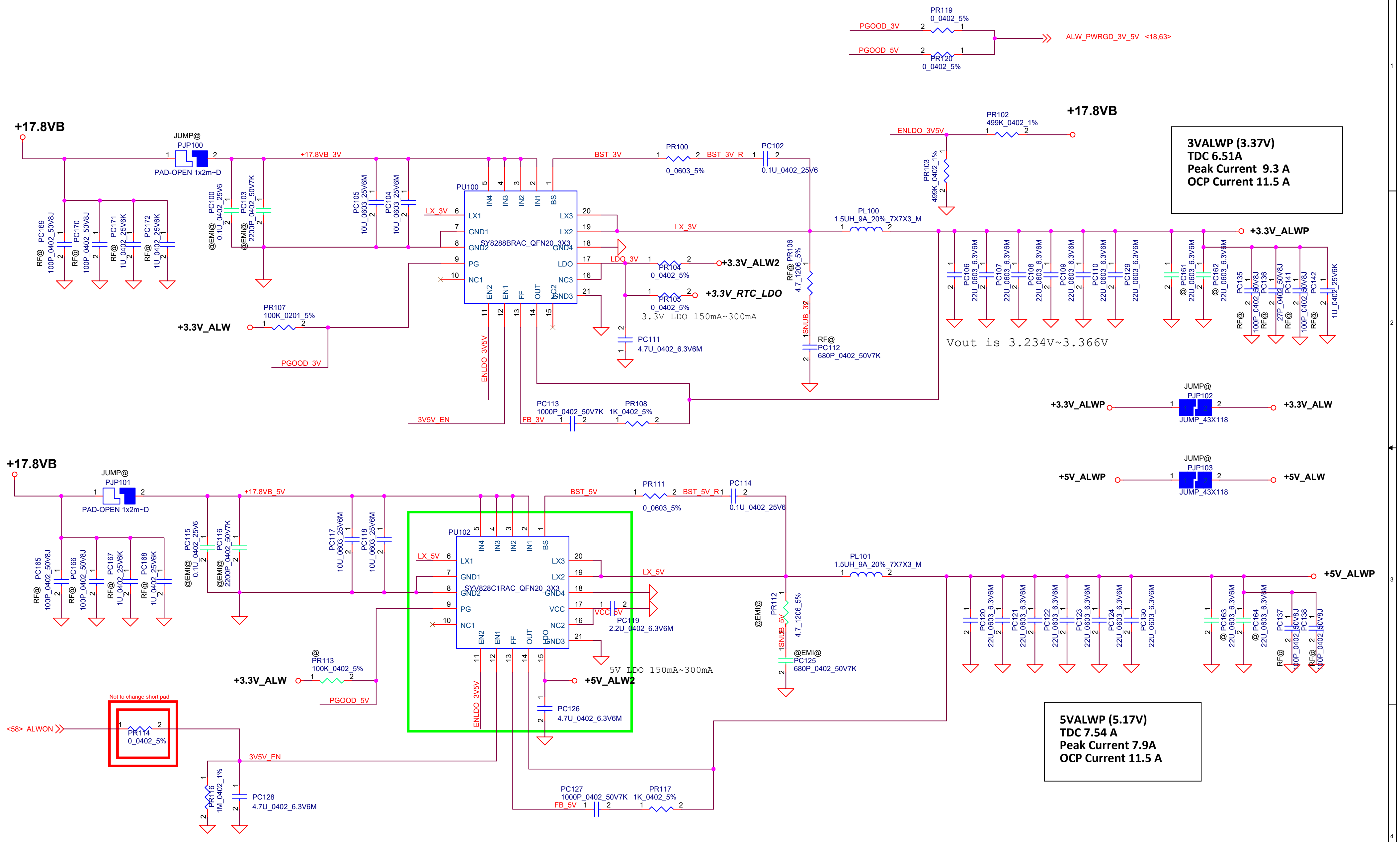

3VALWP (3.37V)
TDC 6.51A
Peak Current 9.3 A
OCP Current 11.5 A

5VALWP (5.17V)
TDC 7.54 A
Peak Current 7.9A
OCP Current 11.5 A

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Compal Electronics, Inc.

Title	+5V_ALW/3.3V_ALW		
Size	Document Number LA-J272P		Rev 0.2
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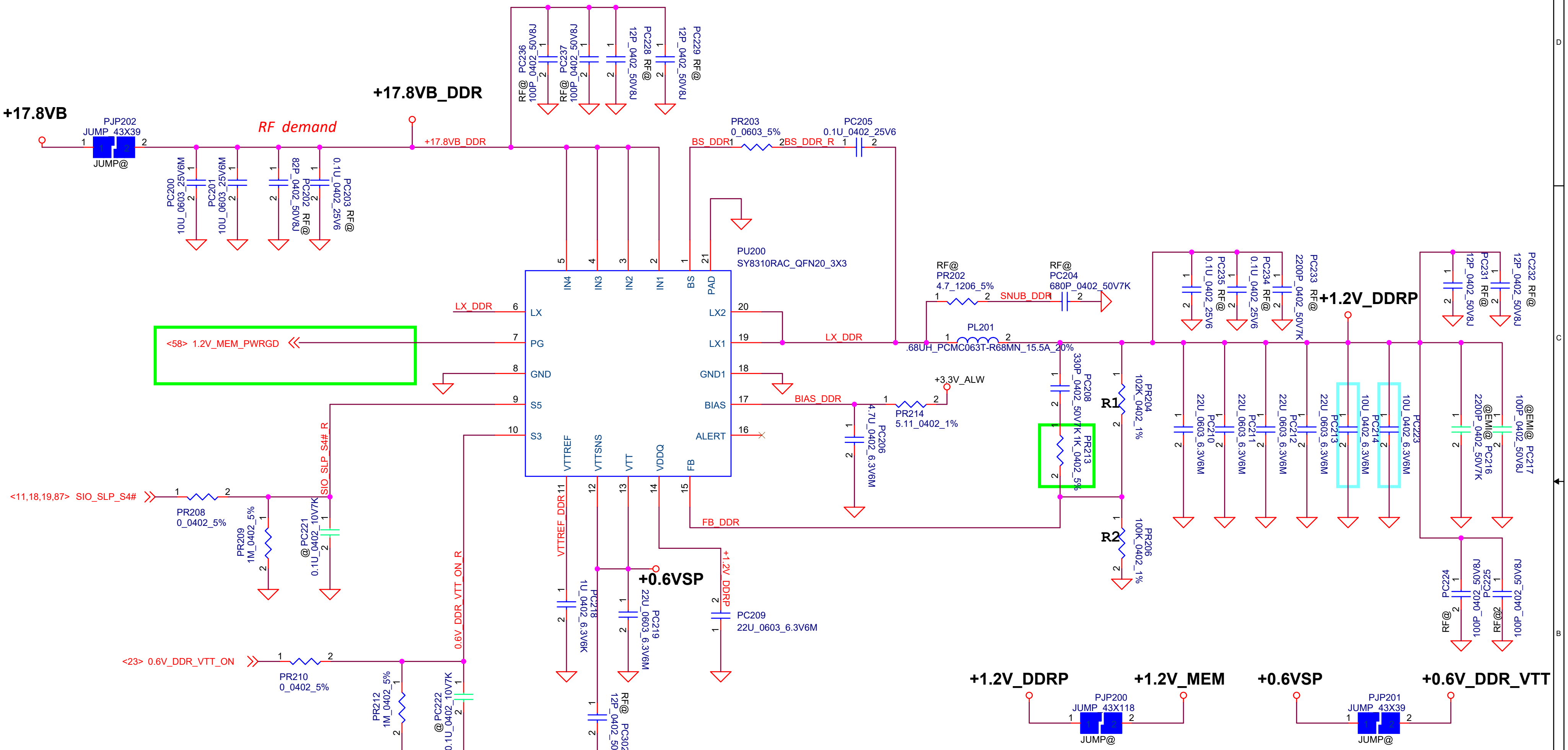

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 7.91A
Peak Current 11.3A
OCP Current 16A Fix by IC

0.6Volt +/- 5%
TDC 0.787A
Peak Current 1.125A
OCP Current 2A (fix)

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Compal Electronics, Inc.

Title
+1.2V_MEN/+0.6V_DDR_VTT

Size
Document Number
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Rev
0.2

Date: Friday, October 25, 2019
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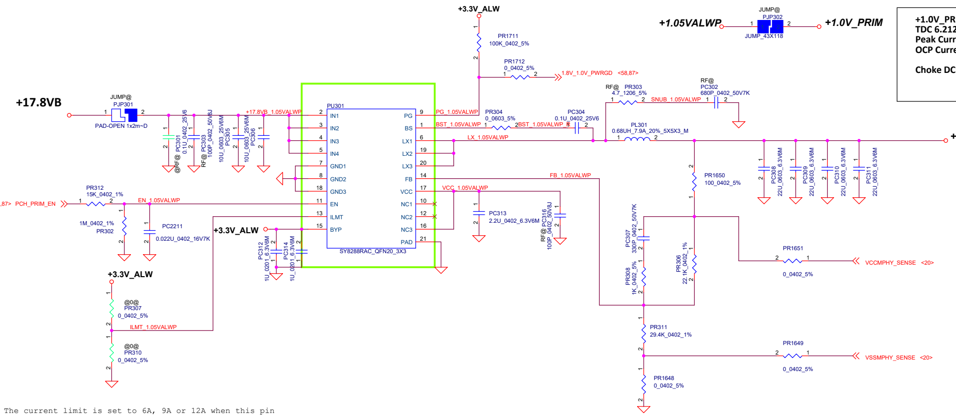
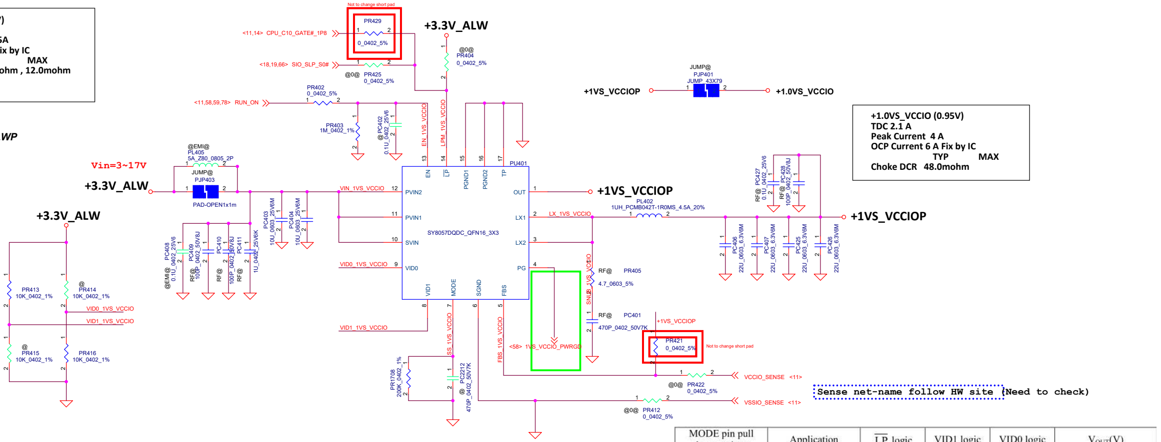


+1.0V_PRIM (1.05V)
TDC 6.212A
Peak Current 8.875A
OCP Current 12 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

The current limit is set to 6A, 9A or 12A when this pin
is pull low, float or pull high

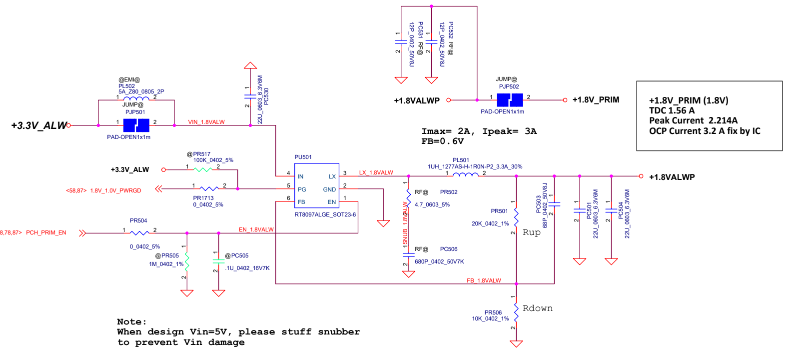


+1.0VS_VCCIO (0.95V)
TDC 2.1 A
Peak Current 4 A
OCP Current 6 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

Sense net-name follow HW site (Need to check)

MODE pin pull down resistor	Application	$\overline{LP}$ logic	VID1 logic	VID0 logic	V_{OUT}(V)
200k	Vcc_IO	0	x	x	0.000(LPM)
		1	0	0	0.850
		1	0	1	0.875
		1	1	0	0.950
		1	1	1	0.975
>500k or floating	Vcc_PRIM_CORE	0	x	x	0.700(LPM)
		1	0	0	0.850
		1	0	1	0.900
		1	1	0	0.950
		1	1	1	1.000
0	Vcc_EDRAM	0	x	x	0.000(LPM)
		1	0	0	0.800(MSM)
		1	0	1	0.950
		1	1	0	1.000
		1	1	1	1.050

Prepared for Compal

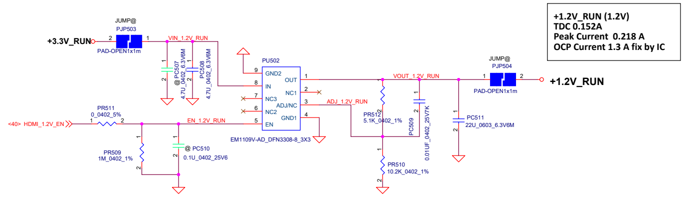


+1.8V_PRIM (1.8V)
TDC 1.56 A
Peak Current 2.214A
OCP Current 3.2 A fix by IC

Imax= 2A, Ipeak= 3A
FB=0.6V

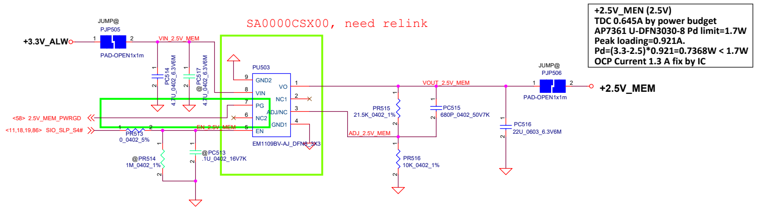
Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)



+1.2V_RUN (1.2V)
TDC 0.152A
Peak Current 0.218 A
OCP Current 1.3 A fix by IC

SA0000CSX00, need relink



+2.5V_MEN (2.5V)
TDC 0.645A by power budget
AP7361 U-DFN3030-8 Pd limit=1.7W
Peak loading=0.921A.
Pd=(3.3-2.5)*0.921=0.7368W < 1.7W
OCP Current 1.3 A fix by IC

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Title
+1VALWP/VCCIO/PRIM_CORE/1.8V/2.5V/1.2V
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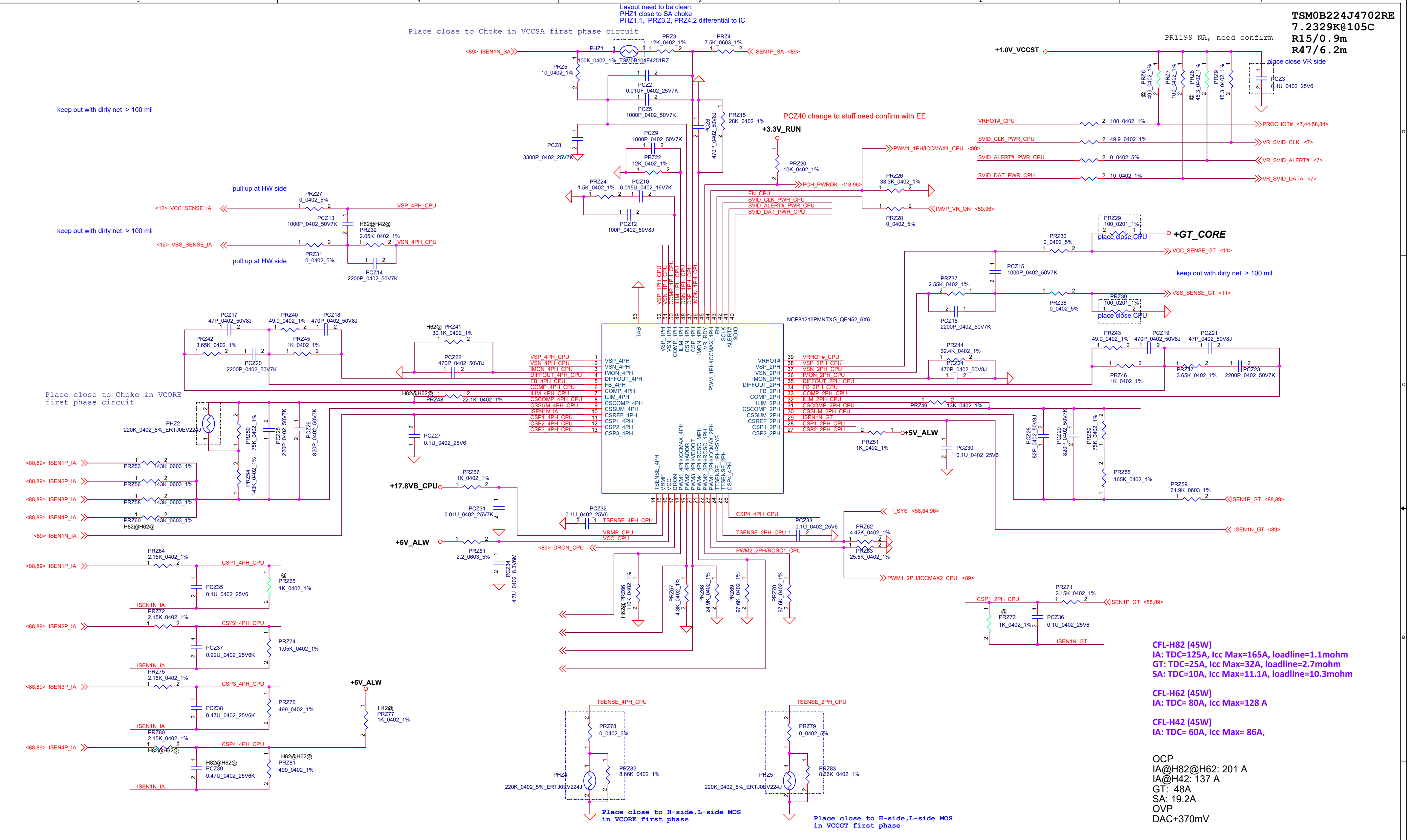
TSM0B224J4702RE
7.2329K@105C
R15/0.9m
R47/6.2m



CFL-H82 (45W)
IA: TDC=125A, Icc Max=165A, loadline=1.1mohm
GT: TDC=25A, Icc Max=32A, loadline=2.7mohm
SA: TDC=10A, Icc Max=11.1A, loadline=10.3mohm

CFL-H62 (45W)
IA: TDC= 80A, Icc Max=128 A

CFL-H42 (45W)
IA: TDC= 60A, Icc Max= 86A,

OCP
IA@H82@H62: 201 A
IA@H42: 137 A
GT: 48A
SA: 19.2A
OVP
DAC+370mV

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Title		
CPU_CORE		
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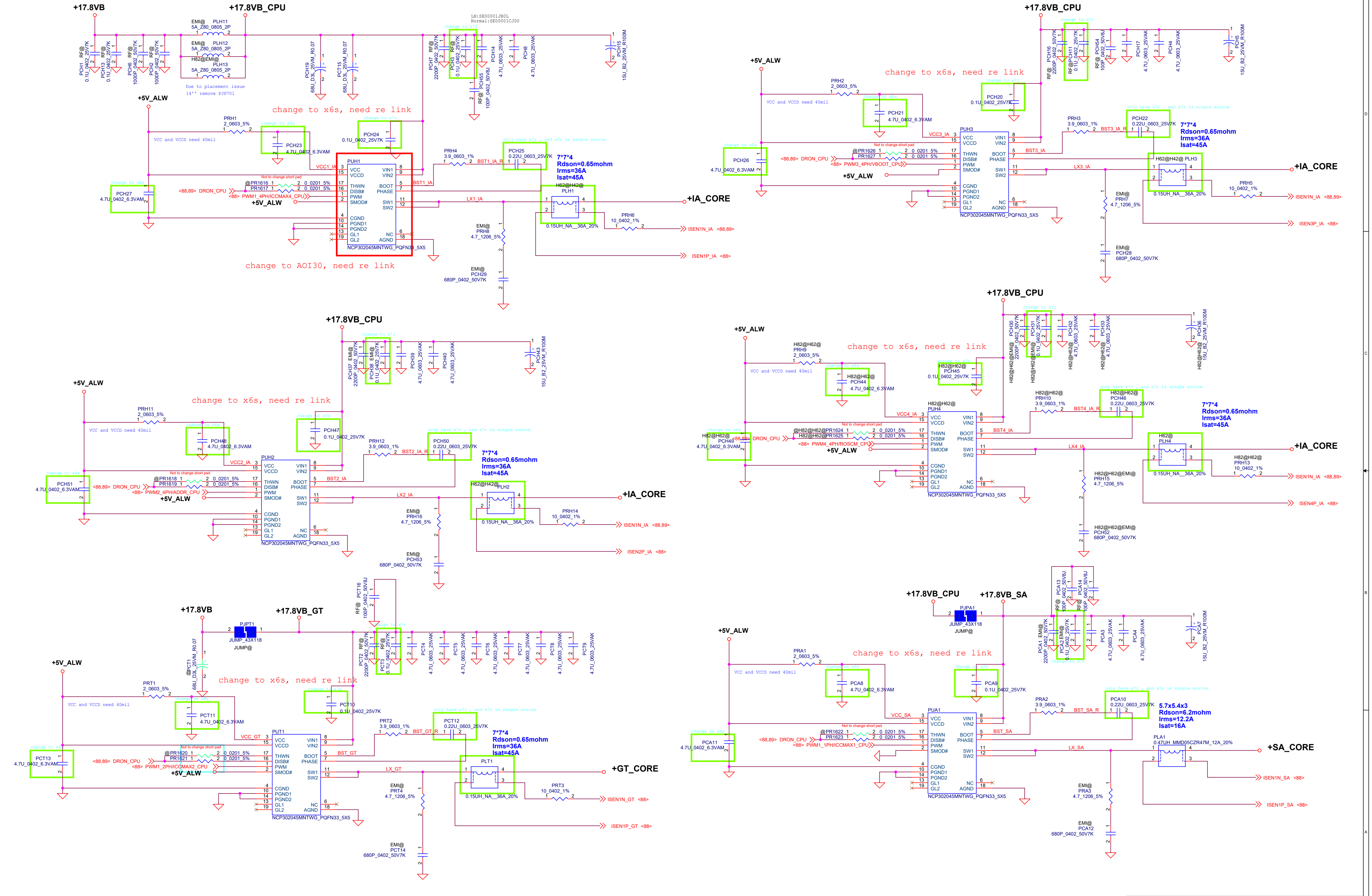

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Compal Electronics, Inc.
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CPU_CORE
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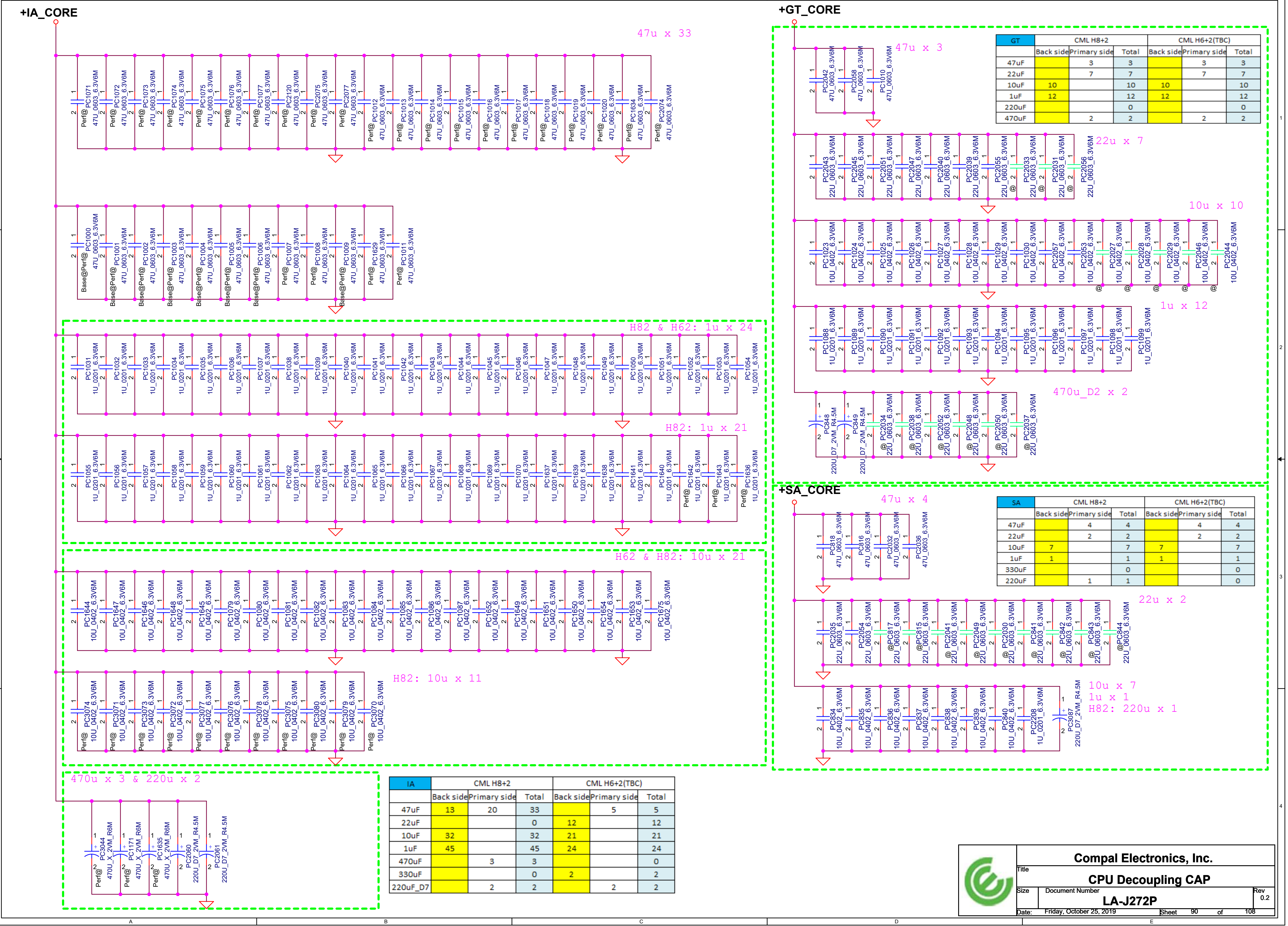

IA	CML H8+2			CML H6+2(TBC)		
	Back side	Primary side	Total	Back side	Primary side	Total
47uF	13	20	33		5	5
22uF			0	12		12
10uF	32		32	21		21
1uF	45		45	24		24
470uF		3	3			0
330uF			0	2		2
220uF_D7		2	2		2	2

GT	CML H8+2			CML H6+2(TBC)		
	Back side	Primary side	Total	Back side	Primary side	Total
47uF		3	3		3	3
22uF		7	7		7	7
10uF	10		10	10		10
1uF	12		12	12		12
220uF			0			0
470uF		2	2		2	2

SA	CML H8+2			CML H6+2(TBC)		
	Back side	Primary side	Total	Back side	Primary side	Total
47uF		4	4		4	4
22uF		2	2		2	2
10uF	7		7	7		7
1uF	1		1	1		1
330uF			0			0
220uF		1	1			0

Compal Electronics, Inc.

Title
CPU Decoupling CAP

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Compal Electronics, Inc.

Title
Reserve for PWR

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			N16S-GTR			N17x
		Config A	Config B	Config C	Config D	N18M-Q3
Vmin	V	0.6	0.6	0.65	0.9	0.3
Vmax	V	1.2	1.2	1.15	1.15	1.3
Vboot	V	0.875	0.9	0.9	1.028	0.8
Voltage Step Vstep	mV	6.25	6.25	25	12.5	6.25
Number of Voltage Levels N	Level	96	96	20	20	160
PWM Frequency Fpwm	MHz	1.125	1.125	0.676	0.676	0.675
PWM Minimum Pulse Width Tdmin	ns	9.26	9.26	74	74	9.26
VID Transient Time T	us	<100	<100	<100	<100	<100
EDP-Continue			26.5A			30A
EDP-Peak			53A			64A
Component Value						
R1(1%)	KΩ	39	20	39	27	6.19
R2(1%)	KΩ	39	20	30	7.5	20.5
R3(1%)	KΩ	1.5	2	3	0	4.32
R4(1%)	KΩ	30	18	24	6.2	16.5
R5(1%)	KΩ	1.5	0	3	1.74	0.309
C	nF	1.5	2.7	1.8	5.6	4.7

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.8V to 1V
Active phase with CCM	1.4V to 5.5V

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)

Rt=Rrefadj // (Rboot+Rref2)

Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]

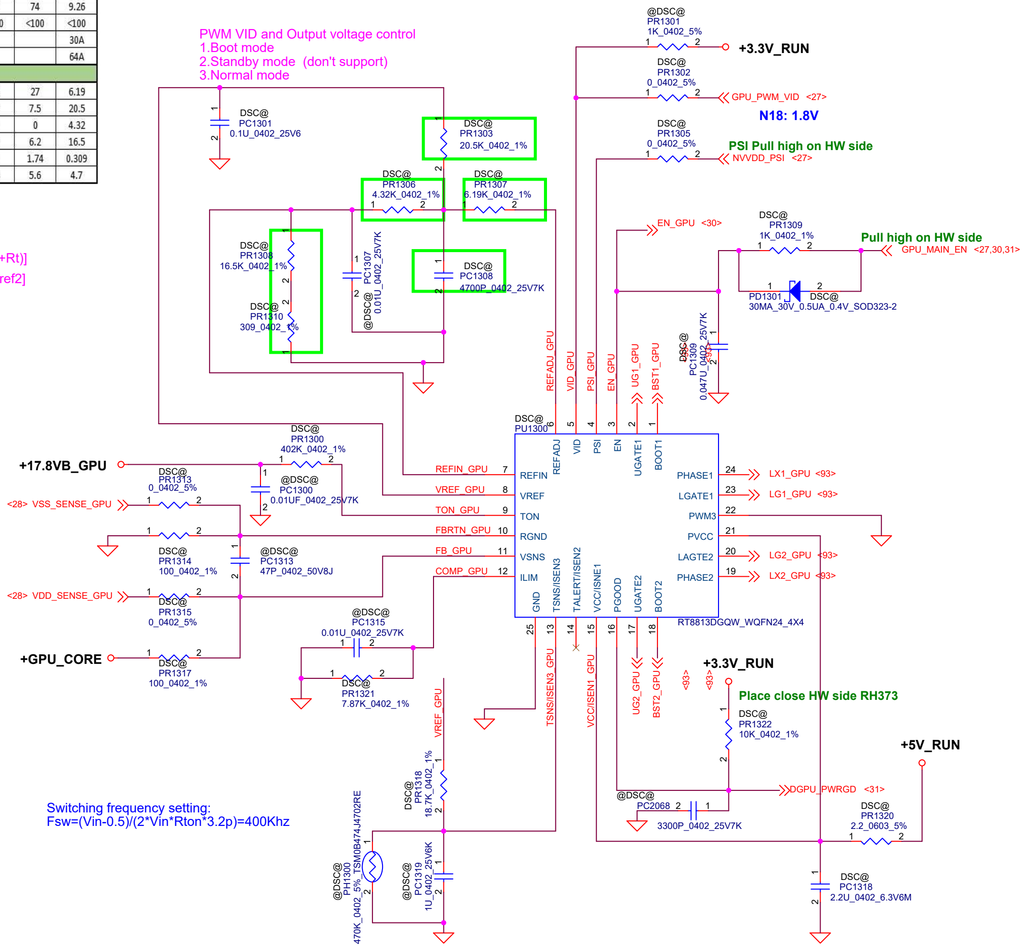
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]

Vout=Vmin+N*Vstep

Vstep=(Vmax-Vmin)/Nmax

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

14HD: N17S-G1 (GB2C-64)
15HD: N17S-G1-B (GB4C-128)
15HP:N19M-Q3



PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

N18: 1.8V

PSI Pull high on HW side

Pull high on HW side

Place close HW side RH373

Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=400Khz

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Compal Electronics, Inc.		
Title **GPU_CORE**		
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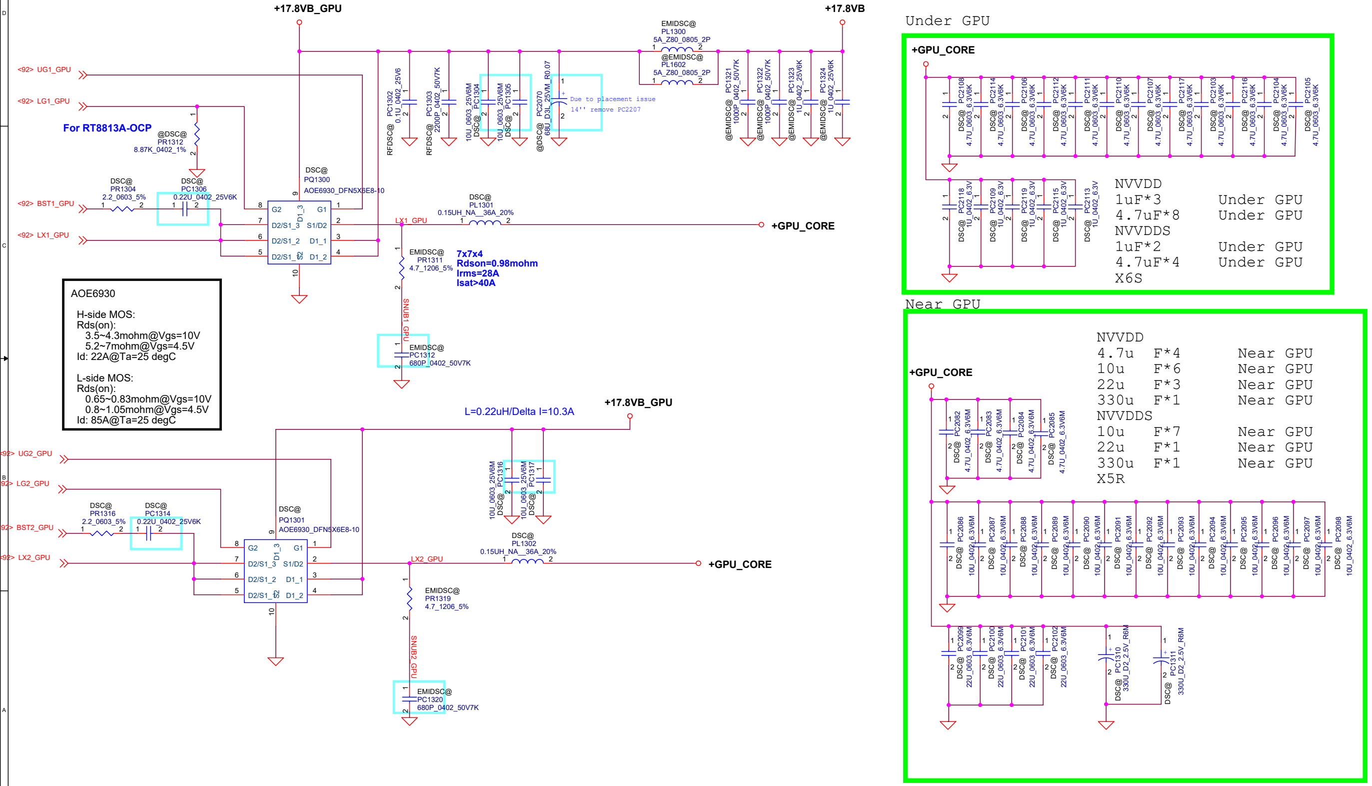
+VGA_CORE(N18M-Q3)
TDC=30 A
Peak 64 A (NVDD=54A, NVDDS=10A)
OCP=78.8 A

C=1*330uF (6mohm)=330uF
Vripple=Iripple*ESR(min)=12.78A*6mohm=76.69mV



AOE6930

H-side MOS:
Rds(on):
3.5~4.3mohm@Vgs=10V
5.2~7mohm@Vgs=4.5V
Id: 22A@Ta=25 degC

L-side MOS:
Rds(on):
0.65~0.83mohm@Vgs=10V
0.8~1.05mohm@Vgs=4.5V
Id: 85A@Ta=25 degC

Under GPU:

NVVDD	
1uF*3	Under GPU
4.7uF*8	Under GPU
NVVDDS	
1uF*2	Under GPU
4.7uF*4	Under GPU
X6S	

Near GPU:

NVVDD		
4.7u	F*4	Near GPU
10u	F*6	Near GPU
22u	F*3	Near GPU
330u	F*1	Near GPU
NVVDDS		
10u	F*7	Near GPU
22u	F*1	Near GPU
330u	F*1	Near GPU
X5R		

BH X10		15HD		14HD	
		N17S-G1-B		N17S-G1	
power rail	cap(uF)	Under	Near	Under	Near
NVVDD	1	8		3	
	4.7	16		8	4
	10		9		6
	22		7		3
	330		1		1
NVVDDS	1	5		2	
	4.7			4	
	10	5	2		7
	22		3		1
	330				1
Total		798.2		958.2	

N18M-Q3-A1(GB4c-128)
NVVDD
1uF*8 Under GPU
4.7uF*16 Under GPU
10uF*9 Near GPU
22uF*7 Near GPU
330uF*1 Near GPU
NVVDDS
1uF*5 Under GPU
10uF*5 Under GPU
10uF*2 Near GPU
22uF*3 Near GPU

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Compal Electronics, Inc.					
Title	GPU_decoupling				
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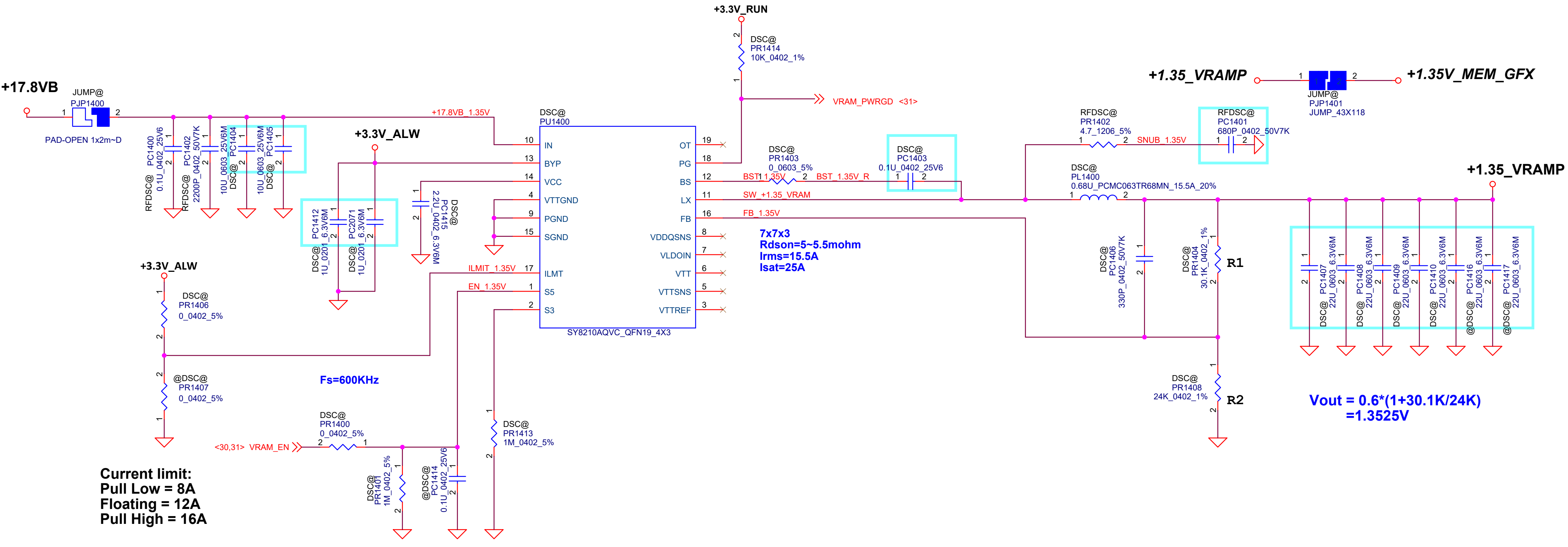
+1.35_VRAM (1.3525V)
TDC=7.7A
Peak Current=11A
OCP=16A



7x7x3
Rdson=5~5.5mohm
Irms=15.5A
Isat=25A

Fs=600KHz

Vout = 0.6*(1+30.1K/24K)
=1.3525V

Current limit:
Pull Low = 8A
Floating = 12A
Pull High = 16A

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Title
GPU_VRAM
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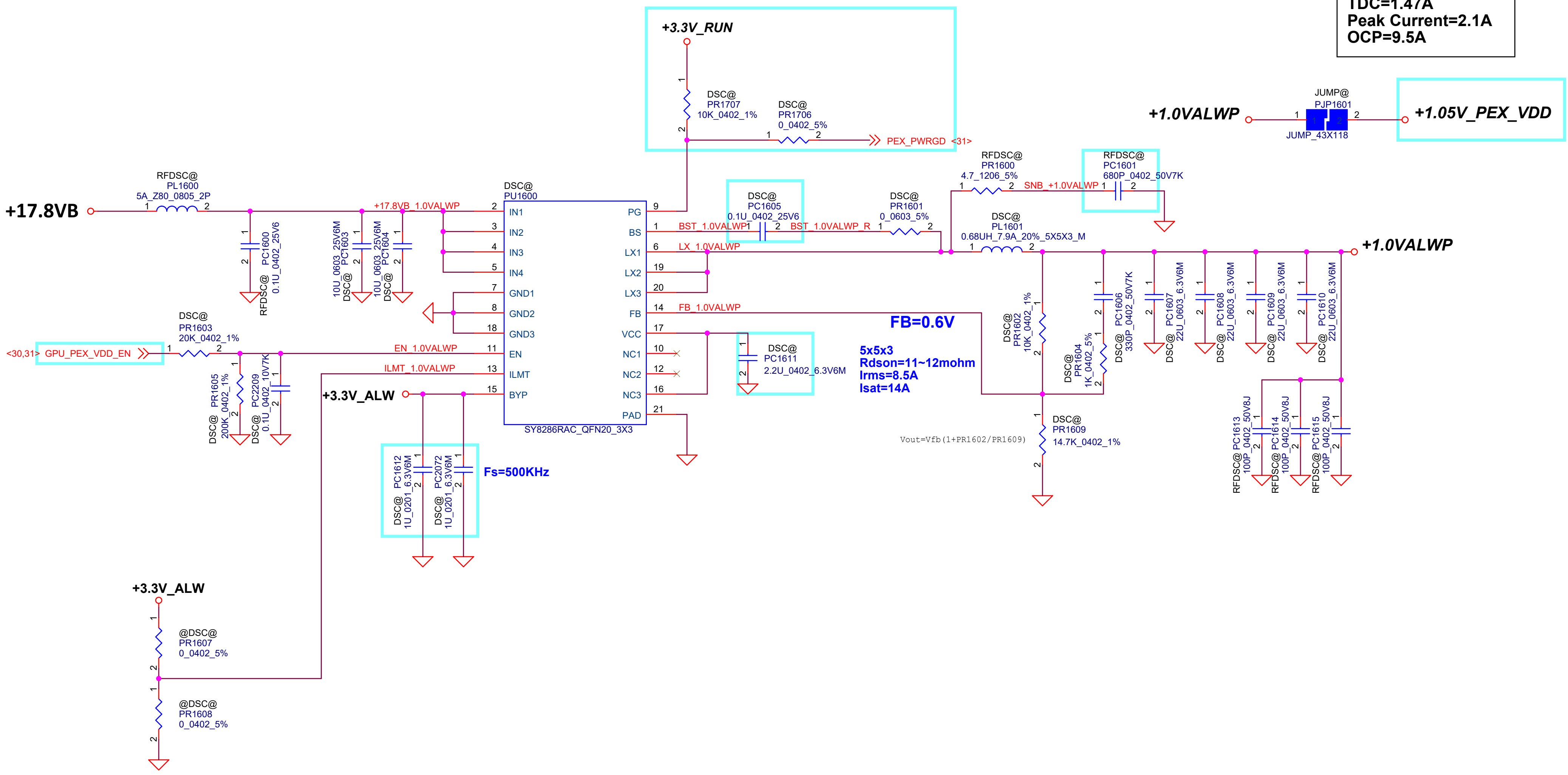
+1.05V_PRIM (1.0V)
TDC=1.47A
Peak Current=2.1A
OCP=9.5A



Current limit:
Pull Low = 6.5~8.5A
Floating = 9.5~11.5A
Pull High = 12.5~14.5A

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Title	**+1.05V_PEX_VDD**
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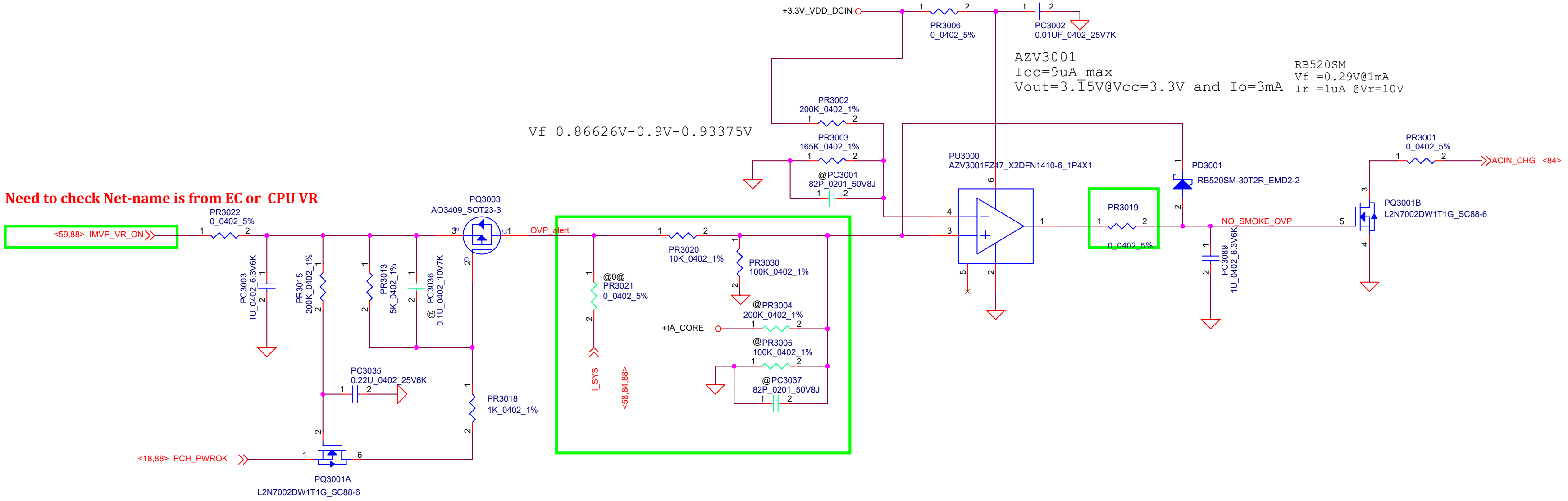

Need to check Net-name is from EC or CPU VR

Vf 0.86626V-0.9V-0.93375V

AZV3001
Icc=9uA_max
Vout=3.15V@Vcc=3.3V and Io=3mA

RB520SM
Vf =0.29V@1mA
Ir =1uA @Vr=10V

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Title
VCORE OVP

Size
Document Number
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Title
Reserve for PWR

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CPU

H82@ PRZ84 25.5K_0402_1%	H42@ PRZ66 82.5K_0402_1%	H42@ PRZ48 15K_0402_1%	H82@ PRZ66 130K_0402_1%	H42@ PRZ41 28K_0402_1%	H82@ PRZ32 2.74K_0402_1%

CPU choke

H82@ PLH1 0.15UH_MMD06DZER15MEM2L_36A_20%	H82@ PLH2 0.15UH_MMD06DZER15MEM2L_36A_20%	H82@ PLH3 0.15UH_MMD06DZER15MEM2L_36A_20%
H82@ PLH4 0.15UH_MMD06DZER15MEM2L_36A_20%		

OUTPUT CAPS

Base@ PC3090 220U_D7_2VM_R4.5M	Base@ PC3092 220U_D7_2VM_R4.5M				
Base@ PC3093 22U_0603_6.3V6M	Base@ PC3091 22U_0603_6.3V6M	Base@ PC3095 22U_0603_6.3V6M	Base@ PC3094 22U_0603_6.3V6M	Base@ PC3096 22U_0603_6.3V6M	
Base@ PC3097 22U_0603_6.3V6M	Base@ PC3098 22U_0603_6.3V6M	Base@ PC3099 22U_0603_6.3V6M	Base@ PC3100 22U_0603_6.3V6M	Base@ PC3101 22U_0603_6.3V6M	
Base@ PC3102 22U_0603_6.3V6M	Base@ PC3104 22U_0603_6.3V6M	Base@ PC3106 22U_0603_6.3V6M	Base@ PC3107 22U_0603_6.3V6M	Base@ PC3110 22U_0603_6.3V6M	Base@ PC3113 22U_0603_6.3V6M
Base@ PC3103 22U_0603_6.3V6M	Base@ PC3105 22U_0603_6.3V6M	Base@ PC3109 22U_0603_6.3V6M	Base@ PC3108 22U_0603_6.3V6M	Base@ PC3111 22U_0603_6.3V6M	Base@ PC3112 22U_0603_6.3V6M

GPU
IC

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Version Change List (P. I. R. List)

Item	*Page#*	*Date*	*Issue Description*	*Solution Description*	*Rev.*

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Compal Electronics, Inc.

Title: **PWR P.I.R**

Size
Document Number: **LA-J272P**
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Date: Friday, October 25, 2019

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay Time (ps/inch)	DK	DF(1GHz)	35 ± 3.5 ohm single-end	40 ± 4 ohm single-end	42 ± 4.2 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm single-end	80 ± 8 ohm Diff	85 ± 8.5 ohm Diff	88 ± 8.8 ohm Diff	90 ± 9 ohm Diff	100 ± 10 ohm Diff	REF	90 ± 9 ohm Diff	85 ±8.5 ohm Diff	REF	100 ± 10 ohm Diff	REF
		3.7	SolderMask	GA-150LL	0.50		3.70	0.03	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	
			Add Plating		0.95																			
1	Top		Copper foil	0.5oz	0.65				8.5	6.6	6	5.3	4.3	5/4.5	4.2/4	3.9/4.1	4/5	3.5/7	L2	7.1/4	8.5/4	L3	10.5/4.5	No REF
		3.7	Prepreg	1086 or 1080	2.70	152.90	3.70	0.0195	34.7	40.3	42.48	45.36	50.26	80.67	85.22	88.24	90.62	100.84		90.66	85.15		99.63	
2	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Core	3mil	3.00		*3.70*	0.0187																
3	Sig1		Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L2/L4				9/5	No REF
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					99.19	
4	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Core	3mil	3.00		3.70	0.0187																
5	Sig2		Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L4/L6				9/5.5	No REF
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					10.16	
6	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Core	3mil	3.00		3.70	0.0187																
7	Sig3		Copper foil	0.5oz	0.65				7.5	5.8	5.5	4.7	3.8	4.5/3.5	4.2/4	4/4.5	4/5	3.5/7.5	L6/L9				9/5.5	No REF
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.48	40.3	41.55	45.29	50.47	80.59	85.13	88.67	90.14	100.62					99.68	
8	Sig4		Copper foil	0.5oz	0.65				7.5	5.8	5.5	4.7	3.8	4.5/3.5	4.2/4	4/4.5	4/5	3.5/7.5	L6/L9				9/5.5	No REF
		3.7	Core	3mil	3.00		3.70	0.0187																
9	GND/PWR		Copper foil	0.5oz	0.65																			
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176																
10	Sig5		Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L9/L11				9/5	No REF
		3.7	Core	3mil	3.00		3.70	0.0187	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					99.19	
11	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Prepreg	1086 or 1080	2.70	152.90	3.70	0.0195																
12	Bottom		Copper foil	0.5oz	0.65				8.5	6.6	6	5.3	4.3	5/4.5	4.2/4	3.9/4.1	4/5	3.5/7	L11	7.1/4	8.5/4	L10	10.5/4.5	No REF
			Add Plating		0.95				34.7	40.3	42.48	45.36	50.26	80.67	85.22	88.24	90.62	100.84		90.66	85.15		99.63	
		3.7	SolderMask		0.50		3.70	0.03																
Overall Thickness (1.2mm ± 10%)					47.90000																			
					1.21666																			
	Reference GCE RD data																							

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PROCHOT# Topology

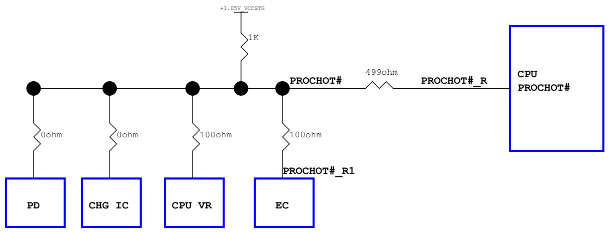


Figure 228. SPI0 3-Load(2 Flash and 1 TPM) EC G3 Flash Sharing with Wire-OR Topology

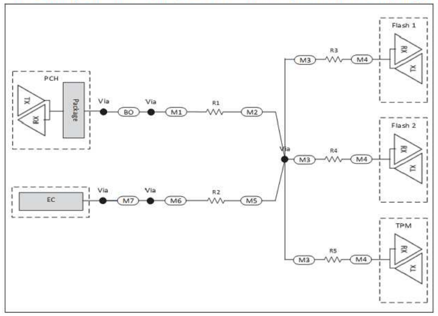
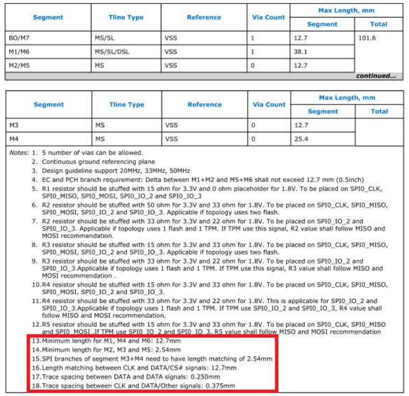


Table 222. SPI0 3-Load(2 Flash and 1 TPM) EC G3 Flash Sharing with Wire-OR Topology Routing Guidelines



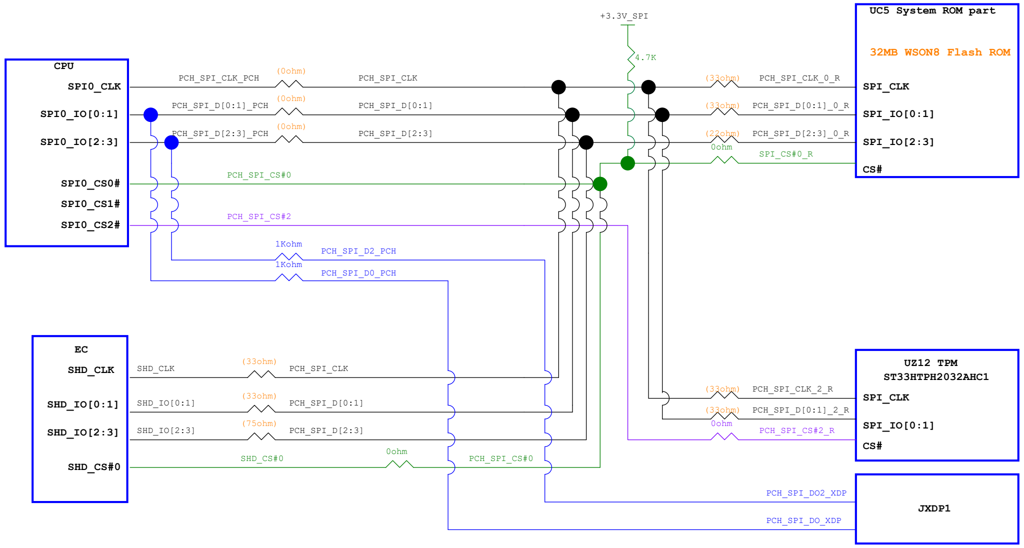
Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
BO/M7	MS/SL	VSS	1	12.7	101.6
M1/M6	MS/SL/DSL	VSS	1	38.1	
M2/M5	MS	VSS	0	12.7	

continued...

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
M3	MS	VSS	0	12.7	
M4	MS	VSS	0	25.4	

Notes:
1. 5 number of vias can be allowed.
2. Continuous ground referencing plane
3. Design guideline support 20MHz, 33MHz, 50MHz
4. EC and PCH branch requirement: Delta between M1+M2 and M5+M6 shall not exceed 12.7 mm (0.5inch)
5. R1 resistor should be stuffed with 15 ohm for 3.3V and 0 ohm placeholder for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3
6. R2 resistor should be stuffed with 50 ohm for 3.3V and 33 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses two flash.
7. R2 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses 1 flash and 1 TPM. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.
8. R3 resistor should be stuffed with 15 ohm for 3.3V and 33 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses two flash.
9. R3 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_IO_2 and SPI0_IO_3.Applicable if topology uses 1 flash and 1 TPM. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation .
10. R4 resistor should be stuffed with 15 ohm for 3.3V and 33 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3.
11. R4 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. This is applicable for SPI0_IO_2 and SPI0_IO_3.Applicable if topology uses 1 flash and 1 TPM. If TPM use SPI0_IO_2 and SPI0_IO_3, R4 value shall follow MISO and MOSI recommendation.
12. R5 resistor should be stuffed with 15 ohm for 3.3V and 33 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI .If TPM use SPI0_IO_2 and SPI0_IO_3, R5 value shall follow MISO and MOSI recommendation
13. Minimum length for M1, M4 and M6: 12.7mm
14. Minimum length for M2, M3 and M5: 2.54mm
15. SPI branches of segment M3+M4 need to have length matching of 2.54mm
16. Length matching between CLK and DATA/CS# signals: 12.7mm
17. Trace spacing between DATA and DATA signals: 0.250mm
18. Trace spacing between CLK and DATA/Other signals: 0.375mm

EC G3 SPI Flash Sharing with Wire-OR Topology



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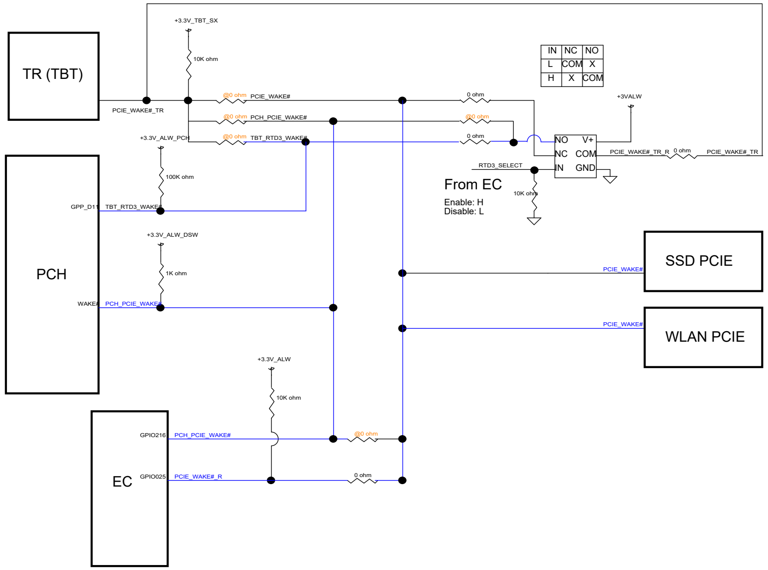
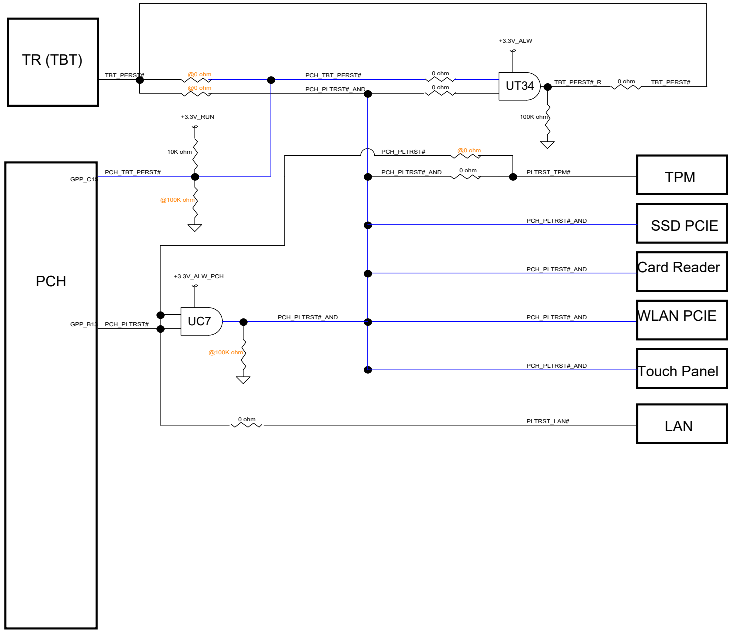
PCH_PCIE_WAKE# Topology



PCH_PLTRST# Topology



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Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.
1	38	2019/9/20	Reserve RC delay on +LCDVDD enable for LCD sequence adjustment flexibility(X11 platform)	add RV180 SD028000080(S RES 1/16W 0 +-5% 0402) and CV80(non-pop) SE000000K80(S CER CAP 1U 6.3V K X5R 0402) on DV3.1	0.2(X01)
2	19 38	2019/9/20	Spyglass lesson learn, reserve PCH GPIO for TS_RST# control(X11 platform)	P19 add net TS_RST# on UH1.BE17(GPP_D13) with offpage P38 add two control path RZ311(SD028000080(S RES 1/16W 0 +-5% 0402, pop) & RZ310(SD028000080(S RES 1/16W 0 +-5% 0402, no-pop)on JIRTS1.1(TS_RST#_R) by PCH & EC(PCH_PLTRST#_AND) respectively,	0.2(X01)
3	52	2019/10/9	CML-H not light up LCD with AX201 installed, implement new push-pull and-gate as level shift for CNVi RF_RESET & CLKREQ_CNV(Aligned with Rialto and Fiorano, X11 platform)	add UZ1,UZ63 SA00003R000(S IC NL17SZ08DFT2G SC70 5P AND GATE) between PCH & WLAN NGFF	0.2(X01)
4	52 58	2019/10/9	Dell request BT_RADIO_DIS# controlled by both EC & PCH(X11 platform)	P52 add two control path DZ16,DZ2 SCS00003700(S SCH DIO RB751S40 SOD523) on JNGFF1.54 BT_RADIO_DIS# by both PCH & WLAN NGFF P58 change RE11 SD028100380(S RES 1/16W 100K +-5% 0402) form no-pop to pop	0.2(X01)
5	59	2019/10/9	DVT1.0 PCB revision, Board_ID change to X01 (X11 platform)	change RE79 from SD000001B80(S RES 1/16W 240K +-1% 0402) to SD034130380(S RES 1/16W 130K +-1% 0402)	0.2(X01)
6	17	2019/10/15	MEC5107 D4 ver has fixed load code issue, depop WDT circuit(X11 platform)	change QZ9,RZ663,CZ622 from pop to no-pop	0.2(X01)
7	44	2019/10/15	1) Dell PW SA request to disconnect PD PROHOT# control (X11 platform) 2) TI request, for TypeC disable feature(X11 platform)	1) change RT85 (SD028000080(S RES 1/16W 0 +-5% 0402, pop) from pop to no-pop(X11 platform) 2) change RT79 (SD028000080(S RES 1/16W 0 +-5% 0402, pop) from no-pop to pop(X11 platform)	0.2(X01)
8	14	2019/10/15	MLCC reduction for baseline sku	add net IA_BASELINE_SEL# on UH1.N48(GPP_K4), and PU/PD RES R105,R106 SD028100280(S RES 1/16W 10K +-5% 0402), PU stands for baseline sku	0.2(X01)
9					

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