COMPAL

MODEL NAME : Bullseye TGL

PCB NO : DA8001QB000

PCB 2X2 LA-K036P REVO M/B 1 S

TGL-U+N17S-G3+MEC1515 (DSC)

2021-03-08

REV : 1.0 (A00)

TGL CPU QS

UC1 SA0000DRS1L QS_I3@
S IC A31 FH8069004531502 QVBG B1 3G S

UC1 SA0000DRR1L QS_I5@
S IC A31 FH8069004530601 QVBD B1 2.4G S

UC1 SA0000DRG1L QS_I7@
S IC A31 FH8069004529905 QVBA B1 2.8G S

TGL CPU Base-U

UC1 SA0000DXG0L PENTIUM@
S IC A31 FH8069004531802 QVBK B1 2G S

UC1 SA0000DXH0L CELERON@
S IC A31 FH8069004531901 QVBS B1 1.8G S

TGL CPU R3

UC1 SA0000DTU2L R3_I5@
S IC FH8069004531301 SRK05 B1 2.4G A31 !

UC1 SA0000DTT2L R3_I7@
S IC FH8069004530104 SRK02 B1 2.8G A31 !

DAZ part number

DAZ2X500101 - GCE

DAZ2X500102 - TRIPOD

DAZ2X500103 - HSB

DAZ2X500104 - TMT

@ : Un-pop Component
DIS@/DISRF@ : GPU Surpport
M_STRAP@/H_STRAP@/S_STRAP@ : VRAM strap pin
2G_G5@/4G_G5@ : 2G GDDR5 / 4G GDDR5 VRAM
UMA@ : not Support external Graphic card
N3@/V3@ : Inspiron/Vostro
MSFT@/NMSFT@ : MSFT SKU / Normal SKU
G3@ : Support G3 sharing SPI topology
CNV@ : Support CNVi function
S5LID@/LID@ : Support S5 LID power up Function/Normal LID close
ES_I3@/ES_I5A@/ES_I5B@/ES_I7@ : TGL-U QS Sample
STG@ : C10_gate control VCCSTG
I2CTCH@/USBTCH@ : Touch Screen support I2C signal / USB signal
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7
I2CPAD@/PS2PAD@ : EC use I2C touch PAD signal(or PS2)
JP@/JUMP@/PJP@ : JUMP
100@/1000@ : 10/100 LAN / Giga-LAN
PRO@/ICPRO@ : only LCDVDD protection/Hinge up protection Support
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/NTPM@ : HW TPM/SW TPM
750_CTPM@ : 750 and china TPM
CTPM@/ST_CTPM@ : China TPM/ST China TPM
FFS@ : Free Fall Sensor
TYPEC@/NTYPEC@ : Support TypeC/non-TypeC
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component
LBIST@/LBIST@RF@ : LBIST for LCD monitor
N17S_G3_R3@/N17S_G3_R1@ : N17S-G3-A1_BGA_595P GPU
TP@/CMC@TP@ : Test Point/XDP Test Point
DISPCB@/UMAPCB@ : PCB MB

Layout Dell logo

REV: X01
PWB: 9HTP8

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

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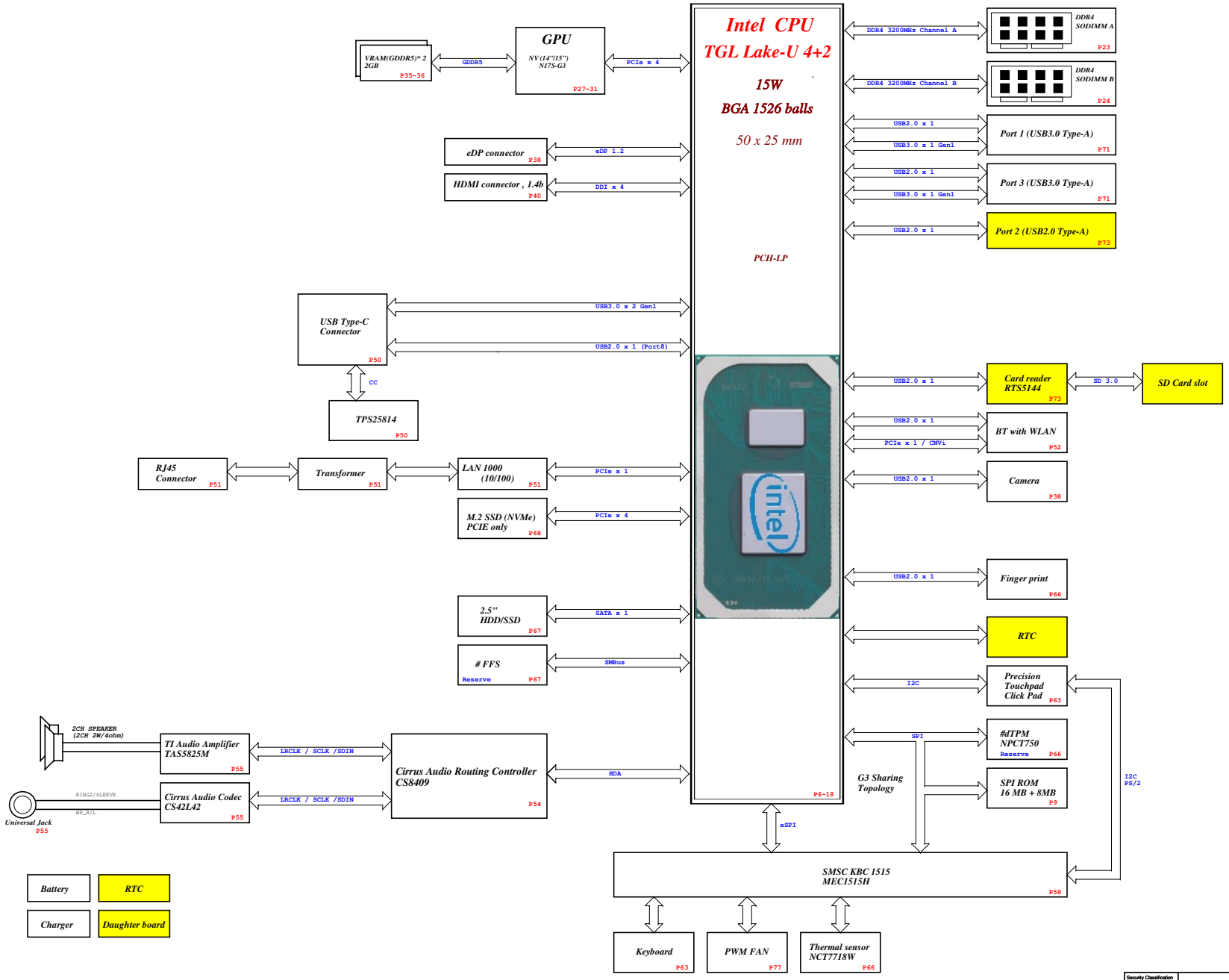
Title: **Cover Page**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 Sheet 1 of 101

Block Diagram



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Title: Block Diagram

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Date: Monday, March 08, 2021 | Sheet 2 of 103

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	Typec-C
5	Finger printer
6	CCD
7	Card reader , IO/B
8	Touch screen
9	Reserved
10	BT

Board ID & Model ID Table

Bullseye TGL			
	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
NBDR	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve RE1 PU-64.9K -Pilot RE1 PU-82.5K -Reserve
	DSC - N17S-G3	RE3 PU-17.8K	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5	G3	
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A	N/A	
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A	
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A	
+RTC_SOC	RTC power	ON	ON	ON	ON	
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF	
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF	
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF	
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF	
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF	
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF	
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF	
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF	
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF	
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF	
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF	
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF	
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF	
+3VALW_DSW	+19VB to DSW power rail for suspend power	ON	ON	ON	OFF	
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF	
+5VS	System +5VS power rail	ON	OFF	OFF	OFF	
+3VS	System +3VS power rail	ON	OFF	OFF	OFF	
+1.35V_MEM_GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF	
+3VGS	+3V power rail for GPU	ON	OFF	OFF	OFF	
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF	OFF	
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF	

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

RE: ICL N3V3 MLK High Power Consumption on VCCIN_AUX Under S3/S5
Wu, Eddie <eddie.wu@intel.com>
寄件日期: 2019/6/6 (週四) 下午 09:41
收件者: Chin. David (TPE); Chen. Johnny (TPE); Hung. Henry (TPE); Chang, Jay Sj; Liu. Joe (TPE); Lai. Carol (TPE); Kenny.Lu@dell.com
副本: Chen. AlexCL (TPE); Cheng, Gary1; Hsiao, Jimmy

Hi David,
VCCIN_AUX only down to 0V while SLP_S0# is asserted.
On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,
Eddie Wu +886-2-66221110

10.12.4 Power States

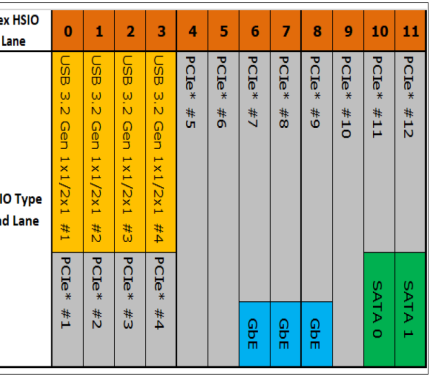
Table 207. System with M3 State Supported

Rails	SKUs	S0/M03	C102	S0ix/M-off[4]	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON [13]	ON [13]	OFF[6]	OFF[6]	OFF	No Power
VCCSTG	All	ON	ON	OFF [2]	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	ON	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON	ON[11]	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON	ON[11]	OFF[14]	OFF[14]	OFF[14]	OFF[14]	No Power

Note : VCCIN_AUX only down to 0V while SLP_S0# is asserted. On S3 mode, it only can down to 1.1V.

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIE-3		USB3.0 (Type-C)
USB3.0-4	PCIE-4		USB3.0 (Type-C)
	PCIE-5		PCIE SSD
	PCIE-6		PCIE SSD
	PCIE-7		PCIE SSD
	PCIE-8		PCIE SSD
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1	NC
	PCIE4 - 0		GPU
	PCIE4 - 1		GPU
	PCIE4 - 2		GPU
	PCIE4 - 3		GPU

Figure 77. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)



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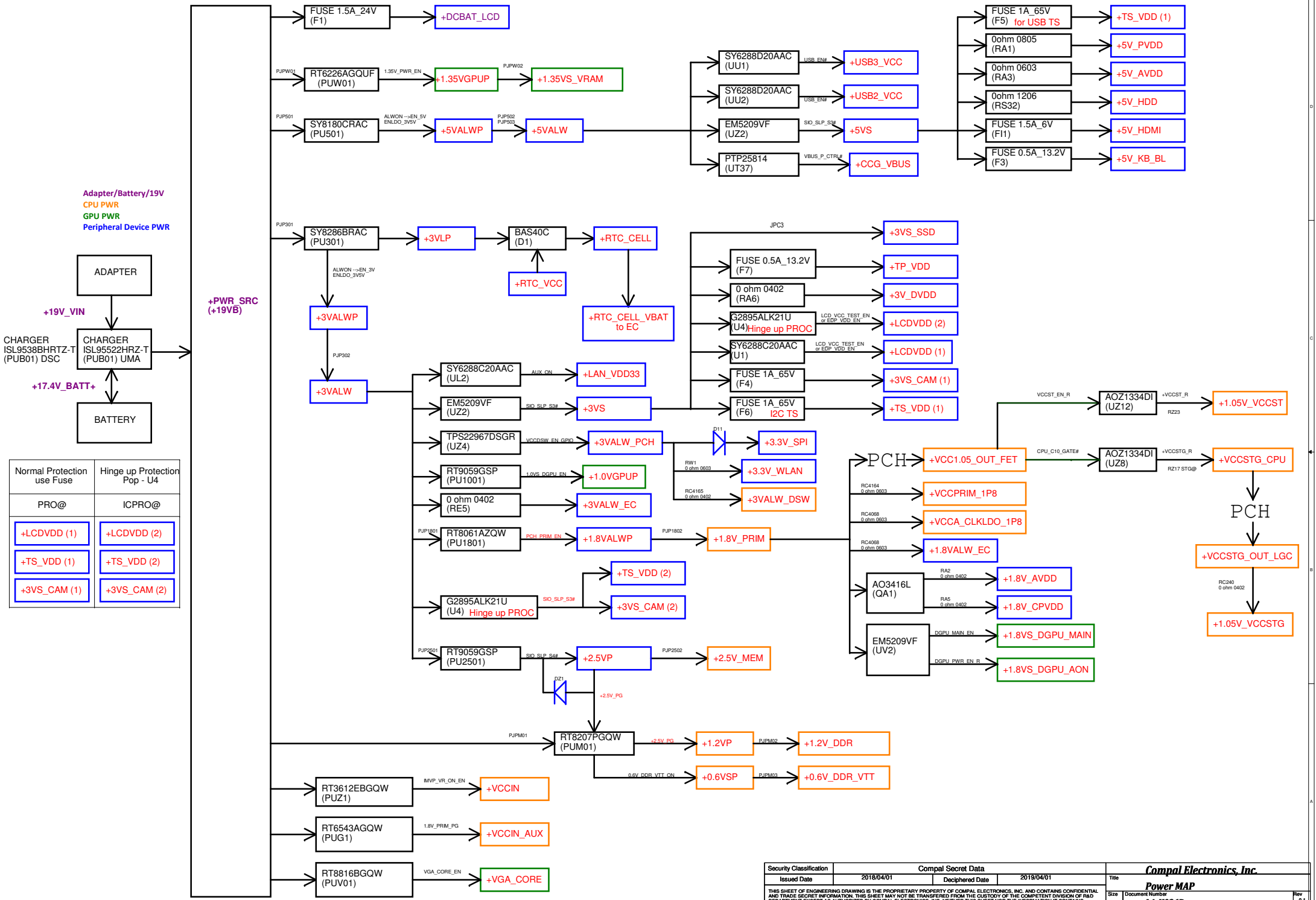
			Date: Monday, March 08, 2021, Sheet 3 of 101



Normal Protection use Fuse	Hinge up Protection Pop - U4
PRO@	ICPRO@
+LCDVDD (1)	+LCDVDD (2)
+TS_VDD (1)	+TS_VDD (2)
+3VS_CAM (1)	+3VS_CAM (2)

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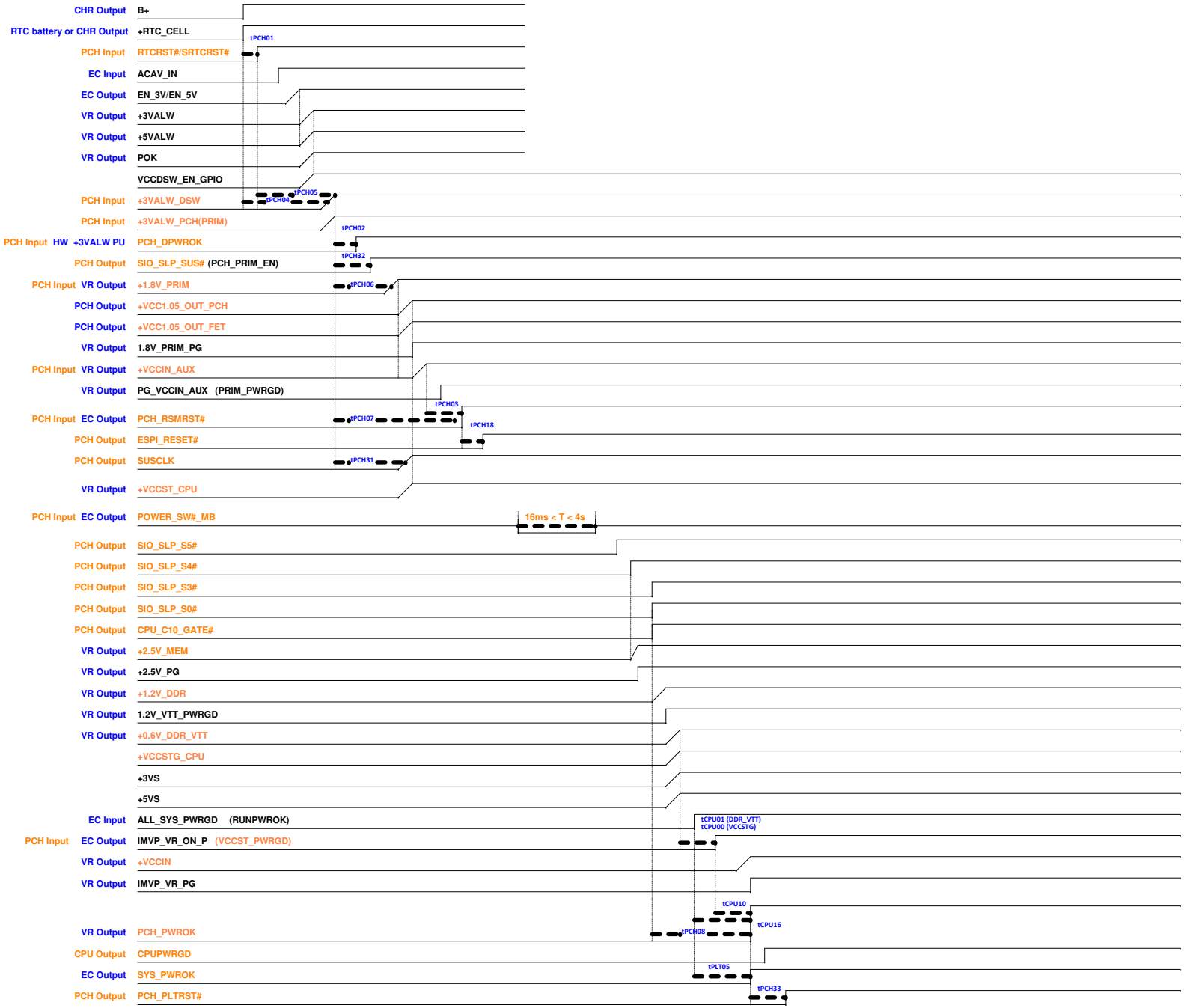
Compal Electronics, Inc.			
Title	Power MAP		
Size	Document Number	LA-K036P	Rev 0.1
Date:	Monday, March 08, 2021	Sheet 4 of 101	

Power Up Sequence
G3 to S0



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Compal Electronics, Inc.			
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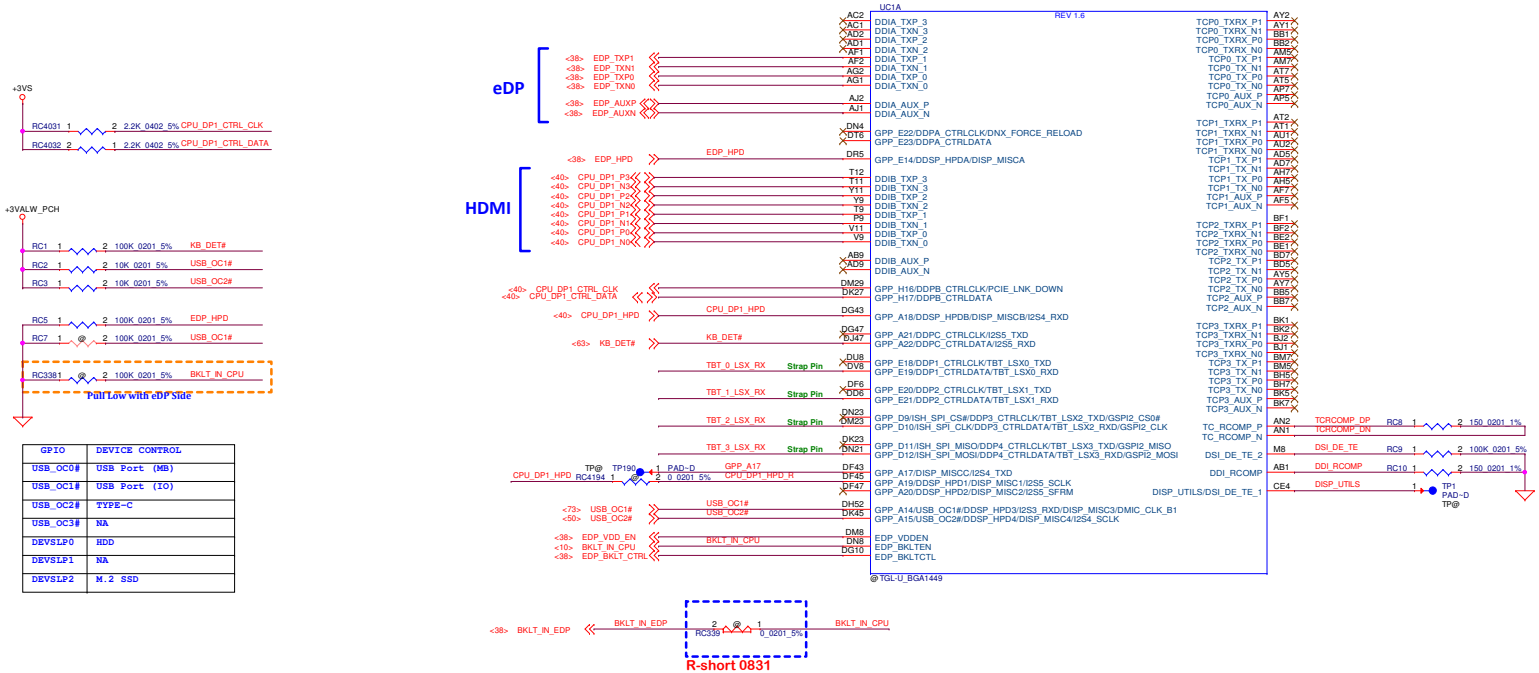
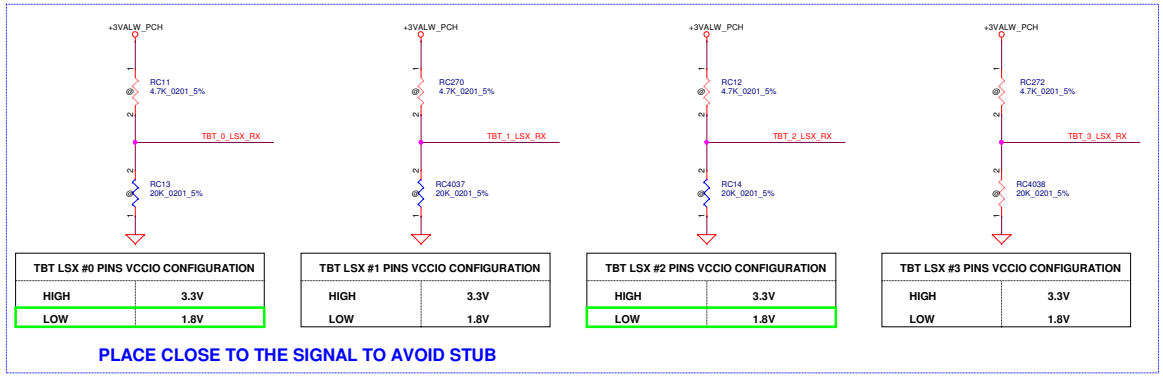
Size	Document Number LA-K036P		Rev 0.1
Date: Monday, March 08, 2021	Sheet 5 of 101		





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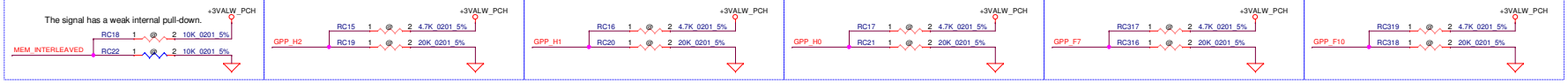
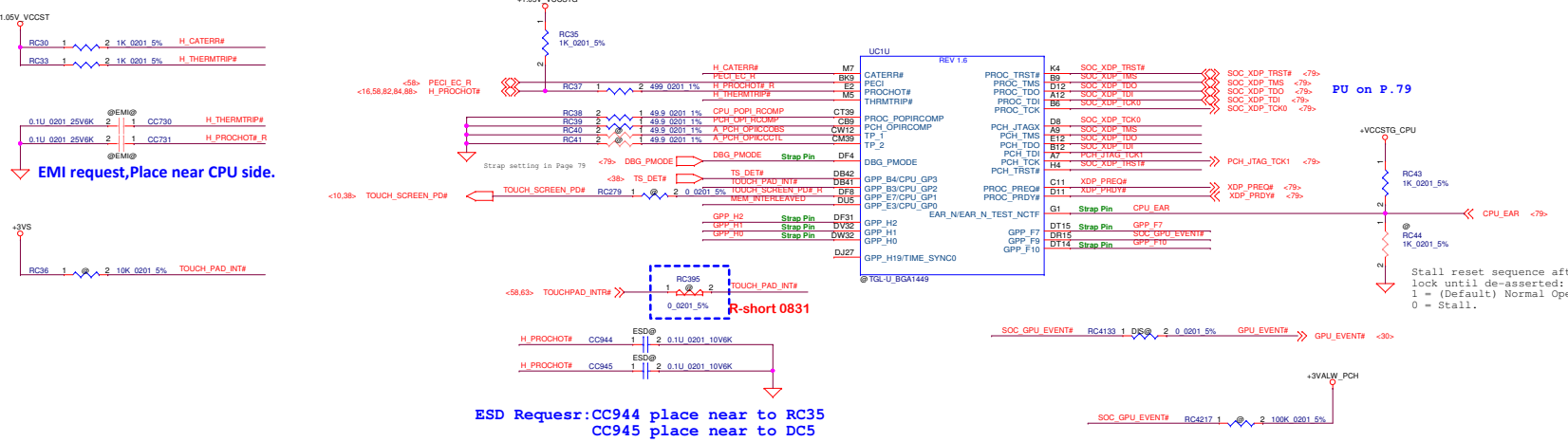
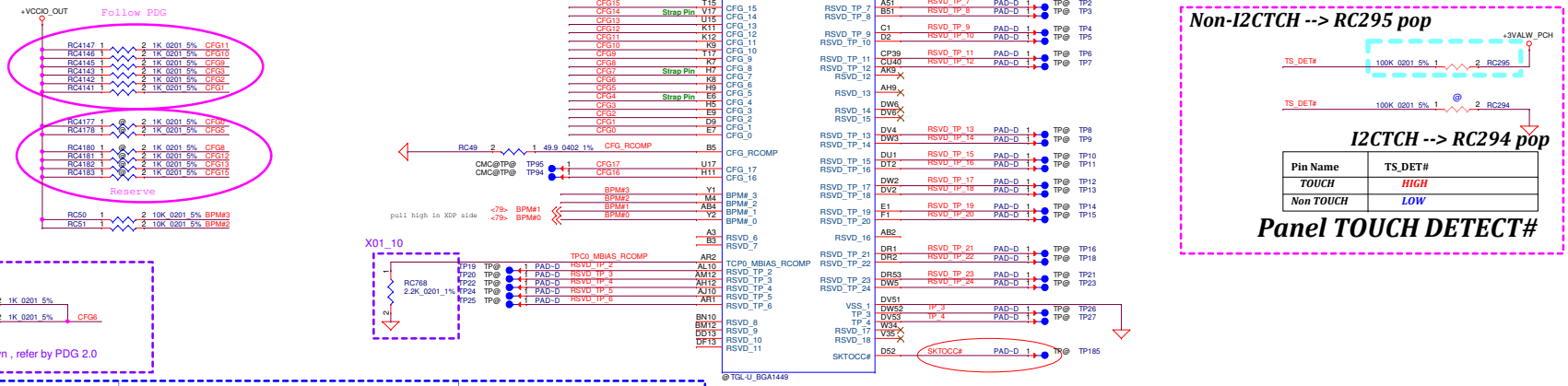
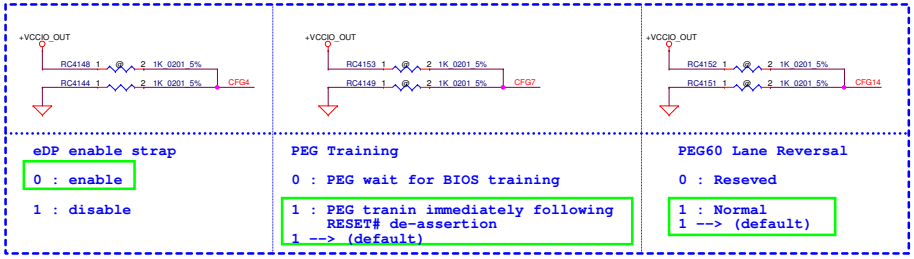
Compal Electronics, Inc.			
Title	P006 - TGL-U(1/13)TCSS,EDP		
Size	Document Number		Rev
	LA-K036P		0.1
Date:	Monday, March 08, 2021	Sheet	6 of 100

DIMM TYPE	BOOT STRAP 3	BOOT STRAP 2	BOOT STRAP 1	Reserved	Reserved
1 : Interleave 0 : Non-Interleave	GPP_H2 (Weak internal PD 20K) This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.	GPP_H1 (Weak internal PD 20K) This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.	GPP_H0 (Weak internal PD 20K) This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.	GPP_F7 (Weak internal PD 20K)	GPP_F10 (Weak internal PD 20K)









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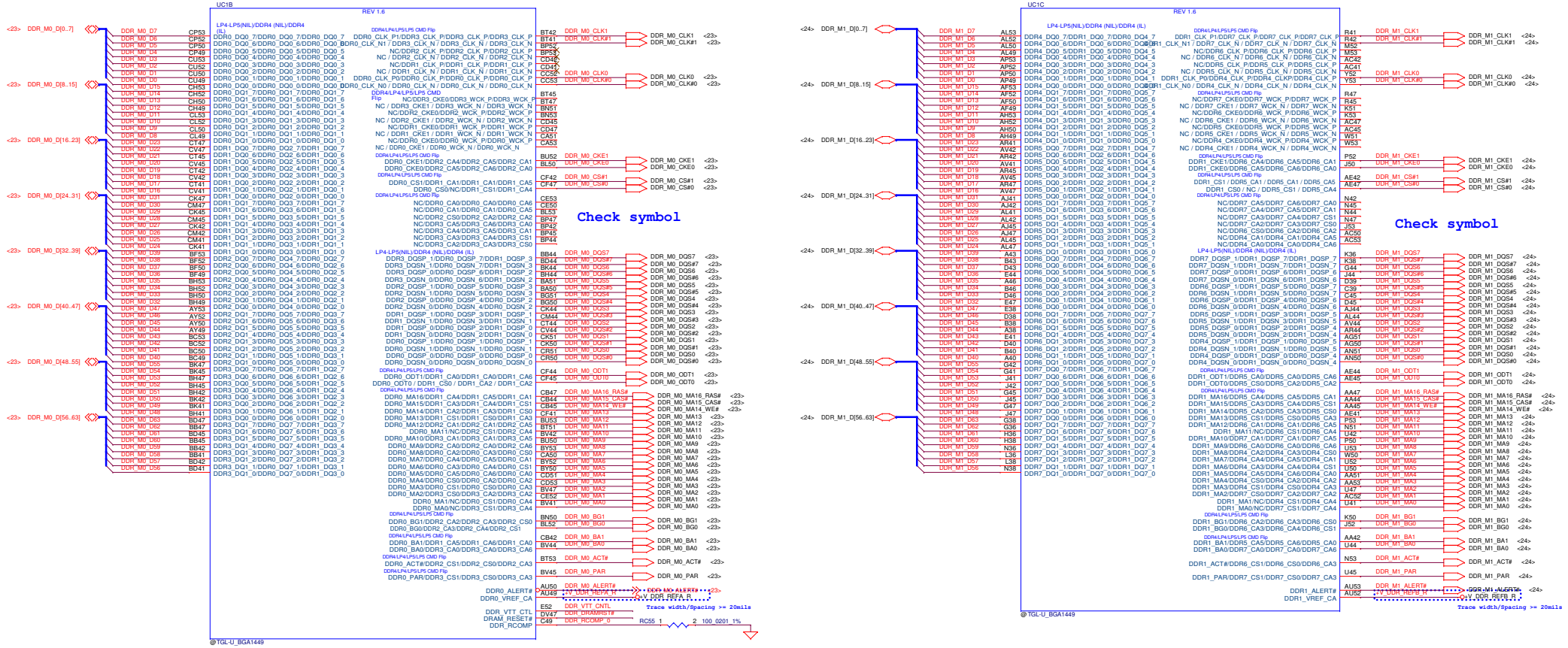
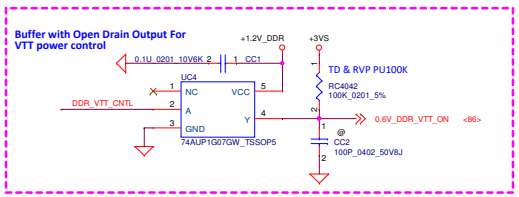
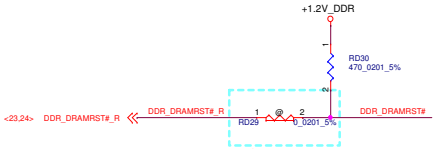
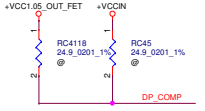
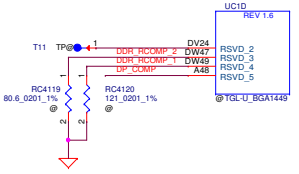
			Size: LA-K036P; Document Number; Rev 0.1
			Date: Monday, March 08, 2021; Sheet 7 of 100











Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	P008 - TGL-U(3/13)LPDDR4/x
Size	Document Number: LA-K036P
Rev	0.1
Date:	Monday, March 08, 2021
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BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

A0 PERSONALITY STRAP

SPI0_IO3

0 = Enable

1 = Disable

TLS CONFIDENTIALITY

GPP_C2 (Weak internal PD 20K)

0 = TLS CONFIDENTIALITY DISABLE

1 = TLS CONFIDENTIALITY ENABLE

no need this security for CSME (internal PD)

CPUNSSC CLOCK FREQ

GPP_B23 (Weak internal PD 20K)

0 = 38.4 MHz clock direct from crystal (default)

1 = 19.2 MHz clock from divider (Device from 38.4MHz crystal)

ESPI OR EC LESS

GPP_C5 (Weak internal PD 20K)

0 = Enable eSPI. (Default)

1 = Disable eSPI.

This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). <--use this

1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI.
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved.

Reserved

GPP_E6 (External pull-up is required)

To TPM

Can set GPIO to 1.8V to cost down level shift circuit

Didn't support C-Link

DDR4,XDP

GPU,THM.EC

Type-C , TBT

ESPI 1.8V

Check!!
AEP pop RC91/RC93
RVP unpop RC91/RC93

PCH R1 R3 SPI1-64Mb
R4 SPI2-128Mb
EC R2 R5 TPM

PCH Side

From EC

R2 should place near P.58 UE1 (EC side)

To SPI ROM 1

To SPI ROM 2

R5 should place near P.66 UX1 (TPM side)

To TPM

For 2 Flash + 1 TPM

R2	R3	R4
RC24 TPM@ 49.9 0201 1% SD00000TO00		
RC25 TPM@ 49.9 0201 1% SD00000TO00		

NPI pop D11
MP pop RC56

For EC Auto Load Code

64Mb Flash ROM
ROM_1

Use X76 control UC5 and UC6
X7687131184 - Winbond
X7687131185 - Gigadevice
X7687131186 - XMC

128Mb Flash ROM
ROM_2

FLASH ROM

RF@ SML1_SMBCLK CC4 @RF@ 33P 0201 50V8J RF Request

EMI@ SPI_CLK_ROM RC405 @EMI@ 33_0402_5% CC72 @EMI@ 33P_0402_50V8J

place colse to UC5

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Issued Date	2020/10/01	Deciphered Date 2018/10/01

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Title: P009 - TGL-U(4/13)SPI,SMB,ESPI

Size: Document Number: LA-K036P Rev: 0.1

Date: Monday, March 08, 2021 Sheet 9 of 100

TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

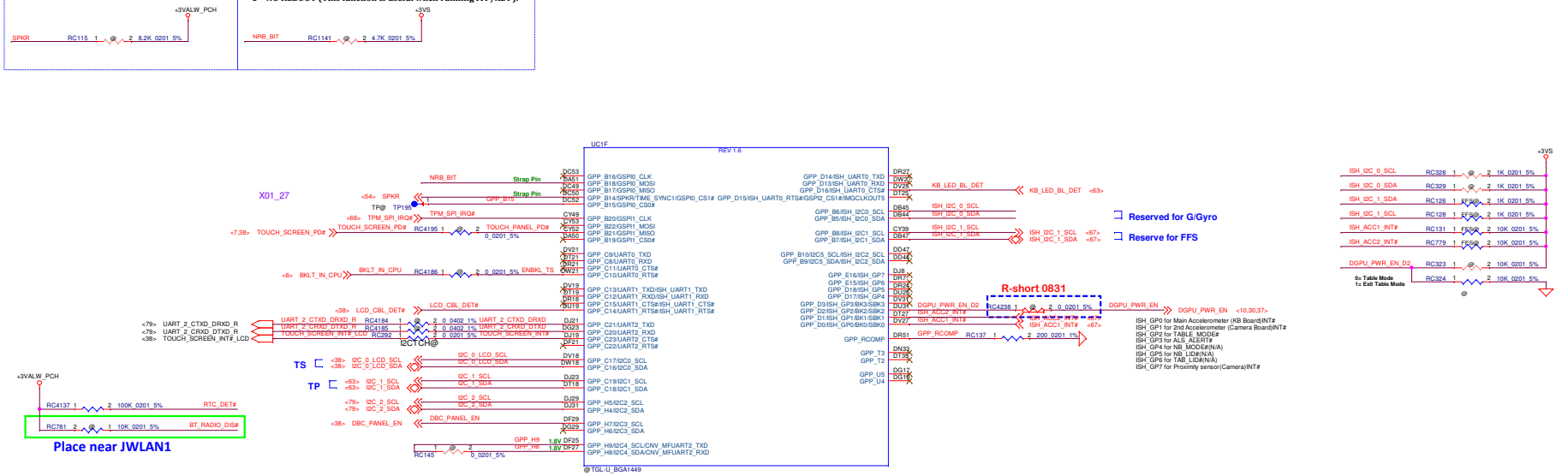
1 = Enable "Top Swap" mode.

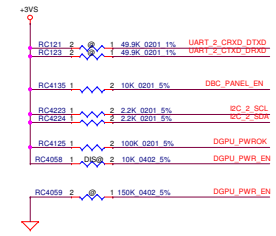
NO REBOOT

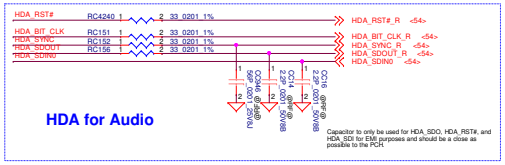
GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = REBOOT ENABLED

1 = NO REBOOT (This function is useful when running ITP/XDP).





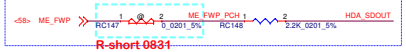


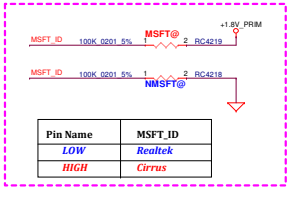
FLASH DESCRIPTOR SECURITY OVERRIDE

GPP_R2/HDA_SDO (Internal 20 K Pull Down)

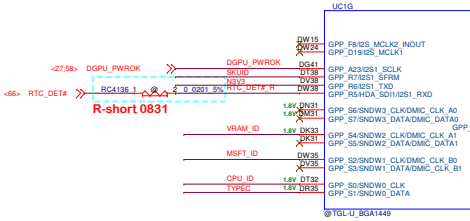
0 = ENABLE (DEFAULT)

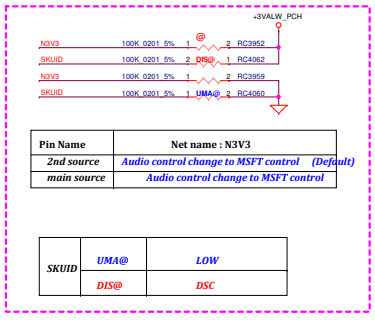
1 = DISABLE (ME can update)





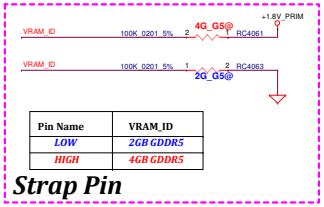
Pin Name	MSFT_ID
LOW	Realtek
HIGH	Cirrus





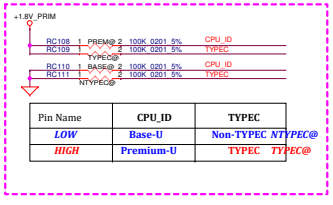
Pin Name	Net name : N3V3
2nd source	Audio control change to MSFT control (Default)
main source	Audio control change to MSFT control

SKUID	UMA@	LOW
	DIS@	DSC



Pin Name	VRAM_ID
LOW	2GB GDDR5
HIGH	4GB GDDR5

Strap Pin



Pin Name	CPU_ID	TYPEC
LOW	Base-U	Non-TYPEC NTYPEC@
HIGH	Premium-U	TYPEC TYPEC@

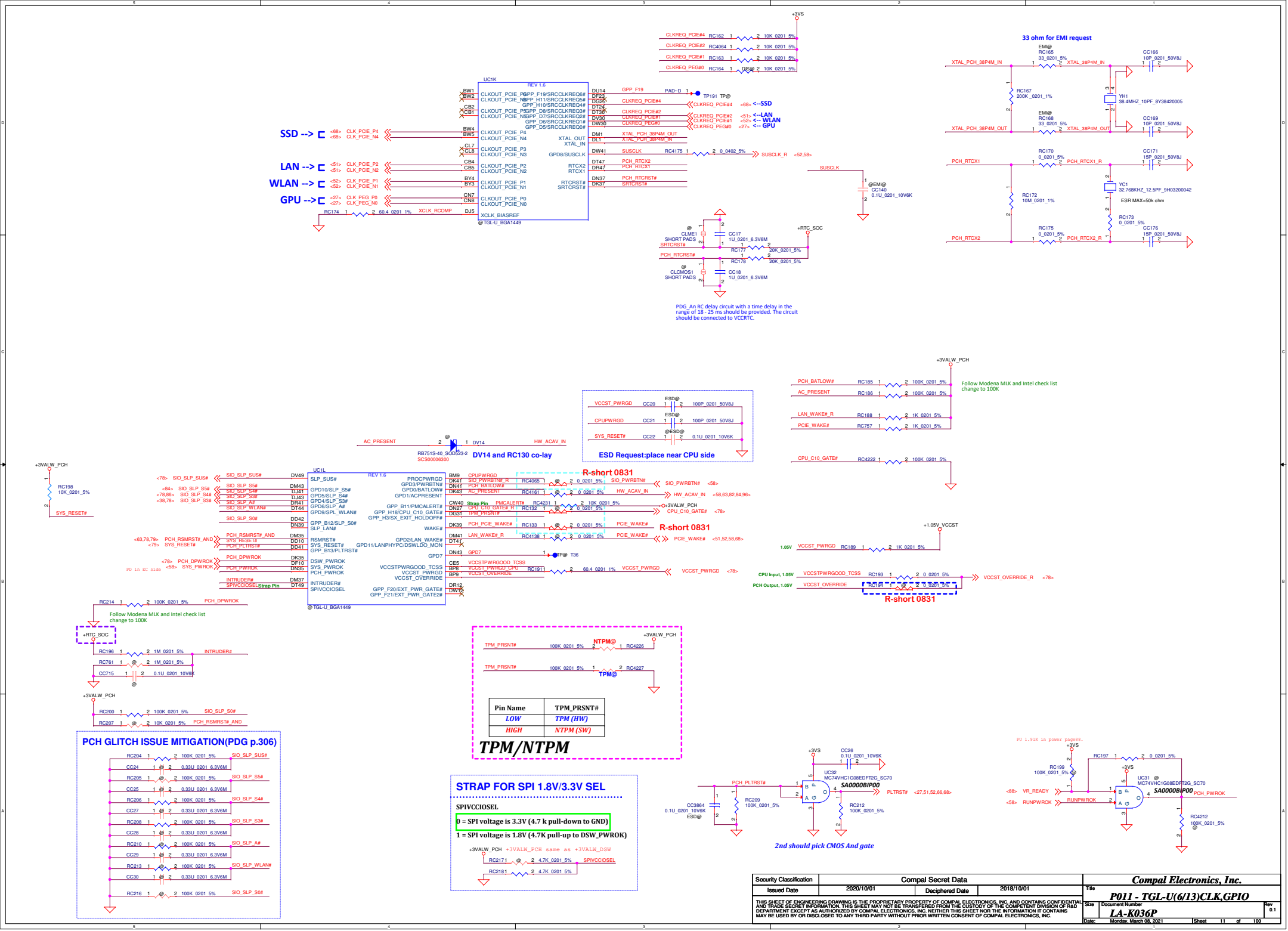
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

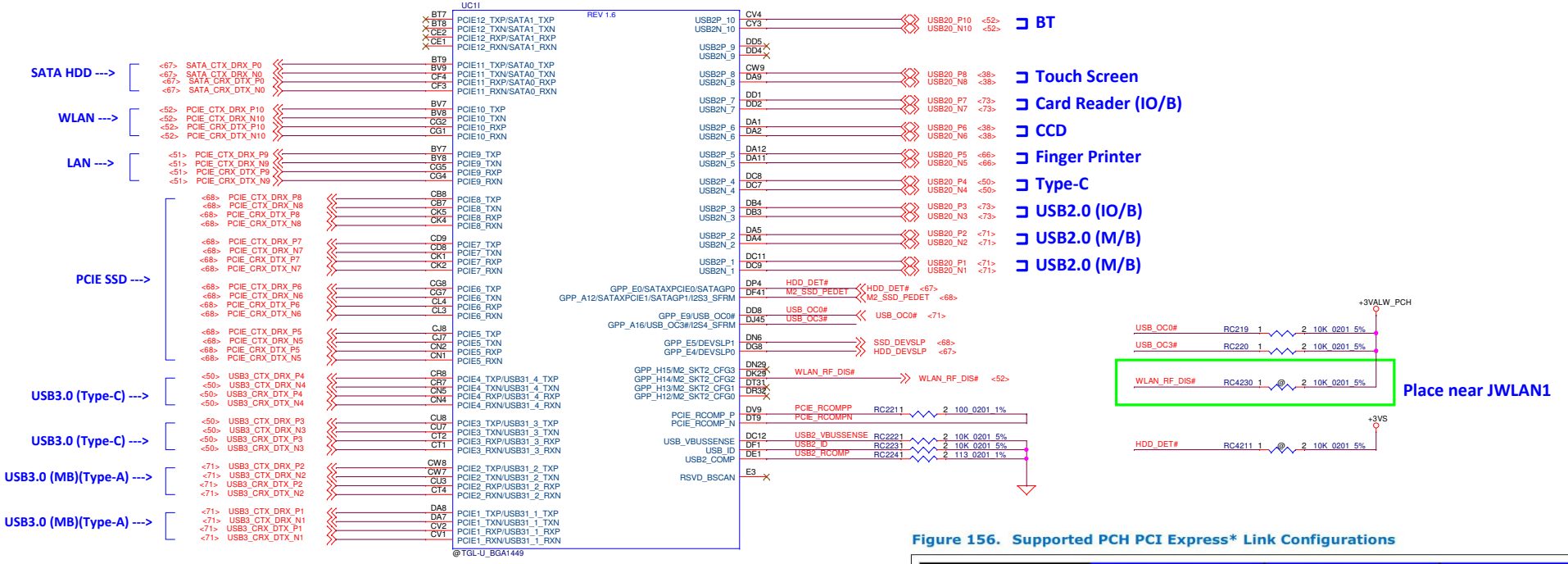
Compal Electronics, Inc.

Title: P010 - TGL-U(5/13)HDA,I2C,ISH

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 10 of 100


33 ohm for EMI request
SSD --> CLK_PCIE_P4 CLK_PCIE_N4
LAN --> CLK_PCIE_P2 CLK_PCIE_N2
WLAN --> CLK_PCIE_P1 CLK_PCIE_N1
GPU --> CLK_PEG_P0 CLK_PEG_N0
UC1K
REV 1.6
@TGL-U_BGA1449
<--SSD
<--LAN
<--WLAN
<--GPU
PDG_An RC delay circuit with a time delay in the range of 18 - 25 ms should be provided. The circuit should be connected to VCCRTC.
DV14 and RC130 co-lay
ESD Request:place near CPU side
R-short 0831
R-short 0831
R-short 0831
Follow Modena MLK and Intel check list change to 100K
Follow Modena MLK and Intel check list change to 100K
PCH GLITCH ISSUE MITIGATION(PDG p.306)
STRAP FOR SPI 1.8V/3.3V SEL
SPIVCCIOSEL
0 = SPI voltage is 3.3V (4.7 k pull-down to GND)
1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWROK)
+3VALW_PCH same as +3VALW_DSW
TPM/NTPM
Pin Name | TPM_PRSNT#
LOW | TPM (HW)
HIGH | NTPM (SW)
2nd should pick CMOS And gate
Compal Secret Data
Issued Date 2020/10/01
Deciphered Date 2018/10/01
Compal Electronics, Inc.
P011 - TGL-U(6/13)CLK,GPIO
LA-K036P
Rev 0.1
Monday, March 08, 2021
Sheet 11 of 100



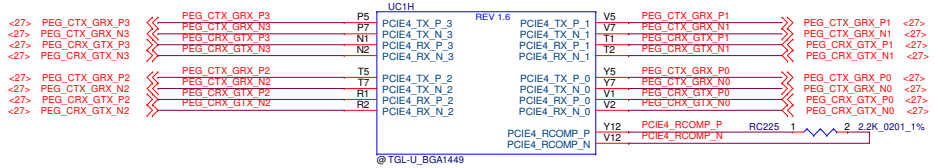


Figure 156. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12
Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1	0	1	0	1
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0
	4x1	0	0	0	0	0	0	0	0	0	0	0	0
Base-U	1x4					RP5				RP9			
	1x4 LR					RP5				RP9			
	2x2					RP5		RP7		RP9		RP11	
	1x2+2x1					RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2					RP8	RP7	RP5		RP12	RP11	RP9	
	4x1					RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-Y	1x4	RP1								RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3				RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4			RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4			RP7	RP8	RP9	RP10	RP11	RP12

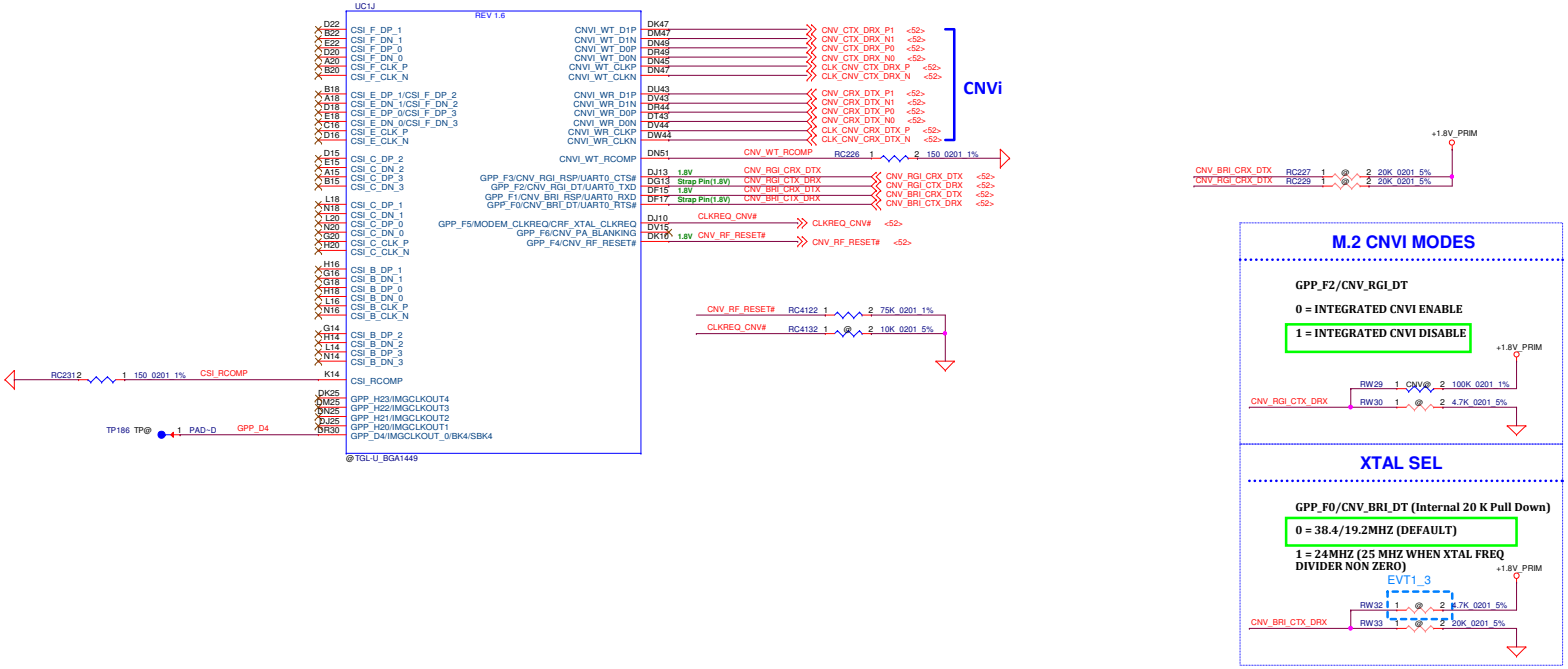
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: P012 - TGL-U(7/13)PCIE,USB

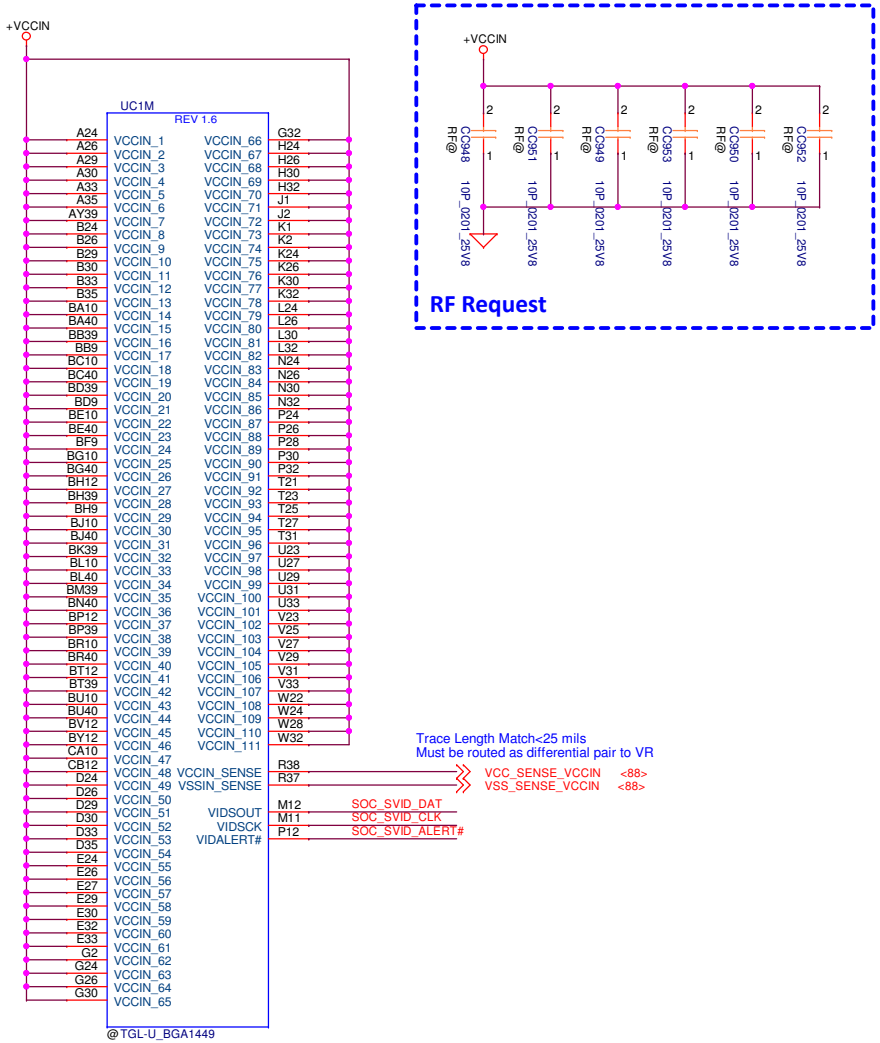
Size: | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 12 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.	
Title	P013 - TGL-U(8/13)CSI,CNVi
Size	Document Number: LA-K033P
Rev	0.1
Date:	Monday, March 08, 2021
Sheet	13 of 100



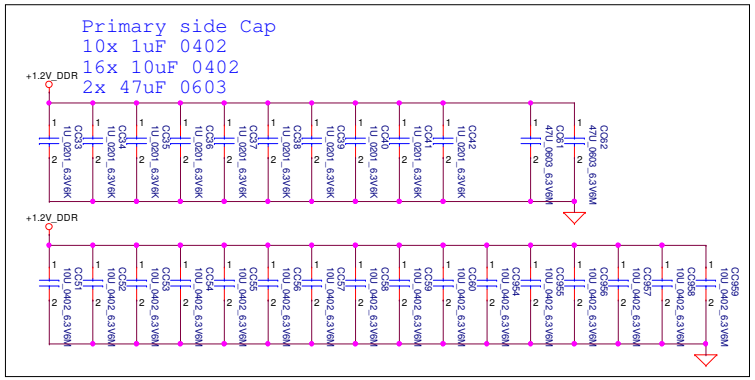
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

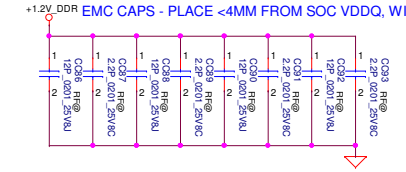
Compal Electronics, Inc.

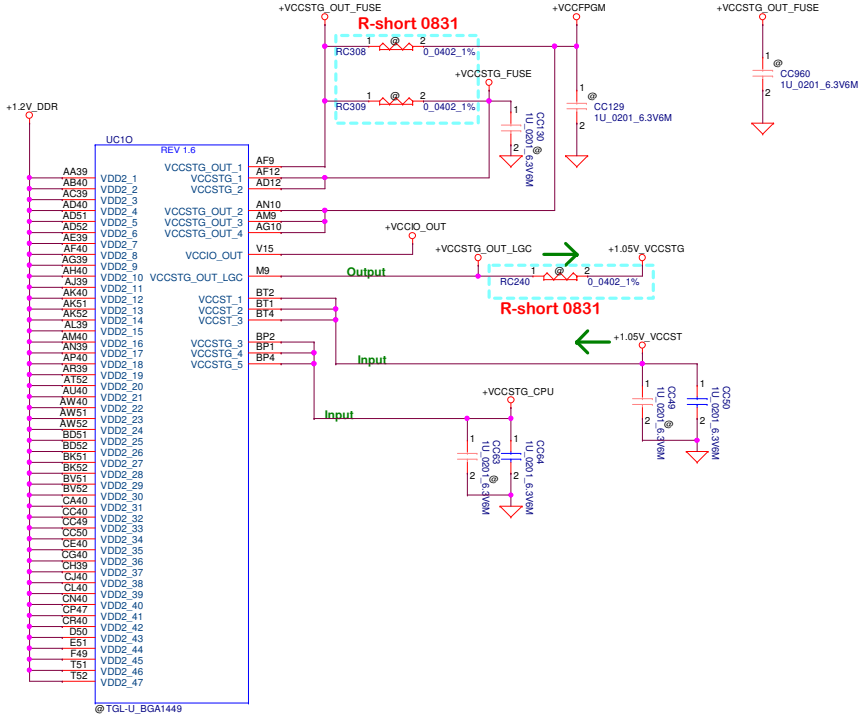
Title: P014 - TGL-U(9/13)CPU PWR,SVID

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 Sheet 14 of 100







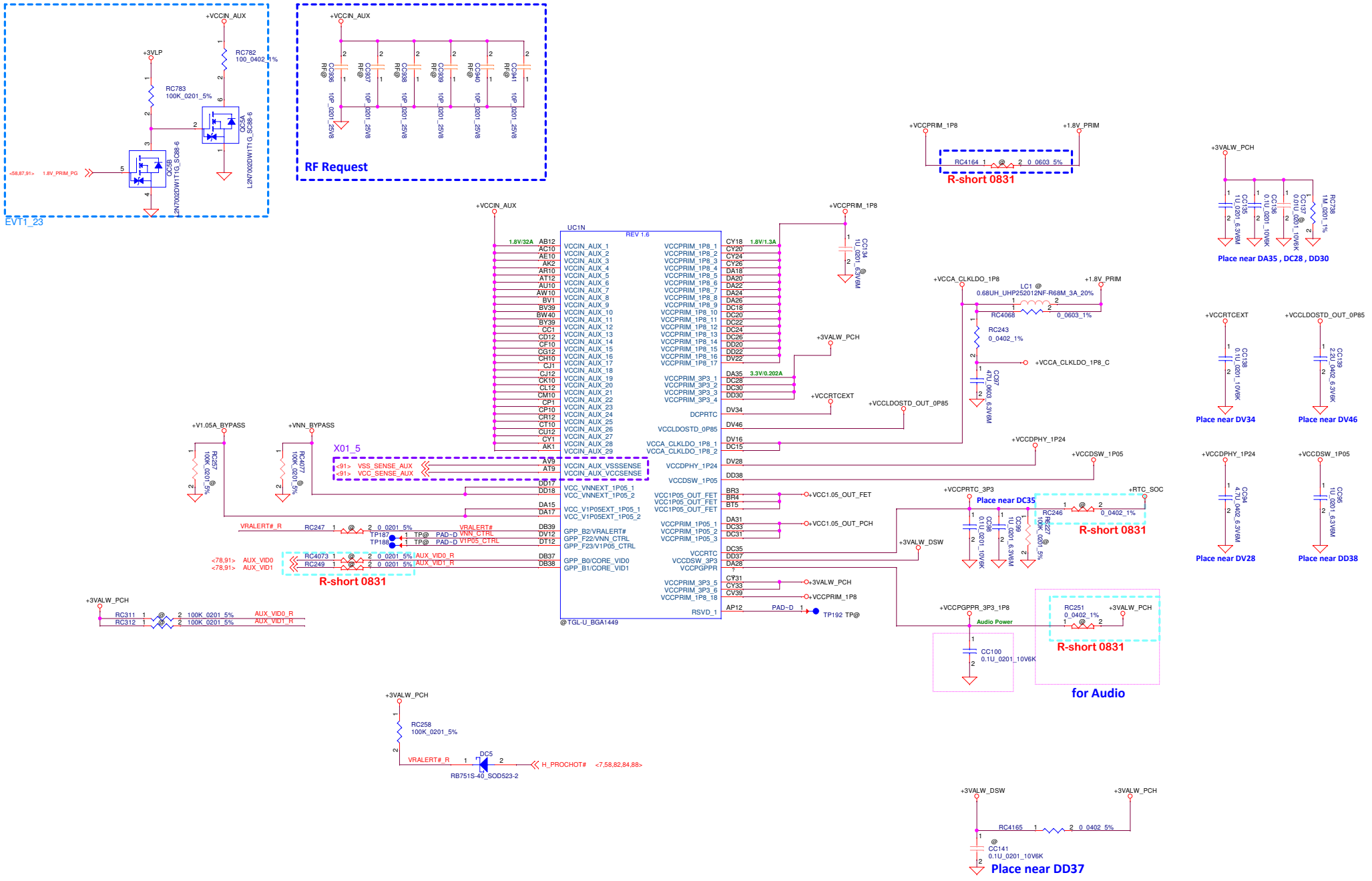
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P015 - TGL-U(10/13)CPU PWR**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 15 of 100



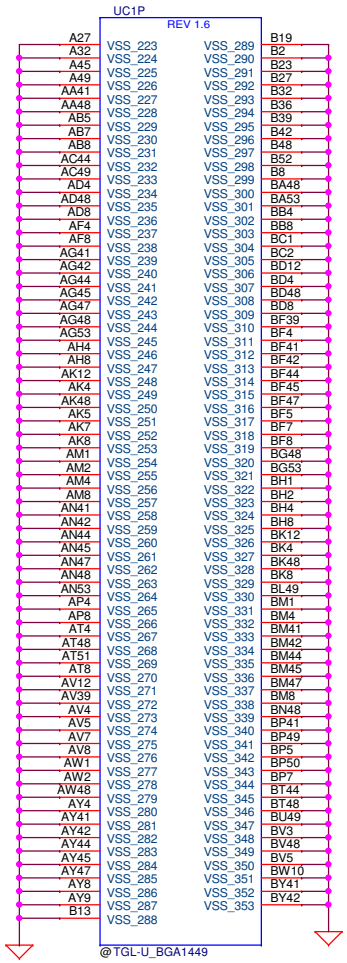
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

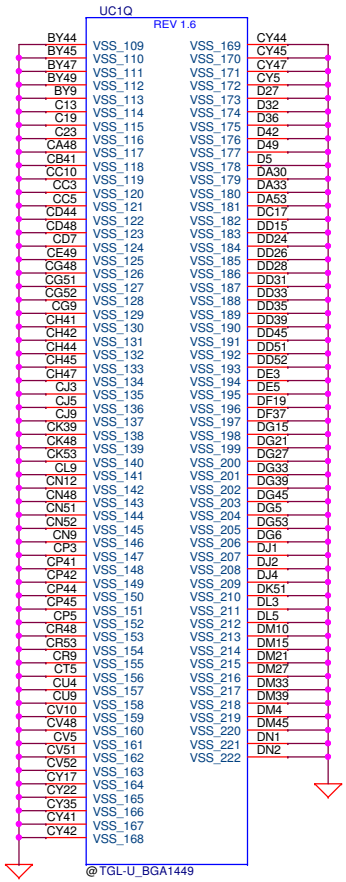
Compal Electronics, Inc.

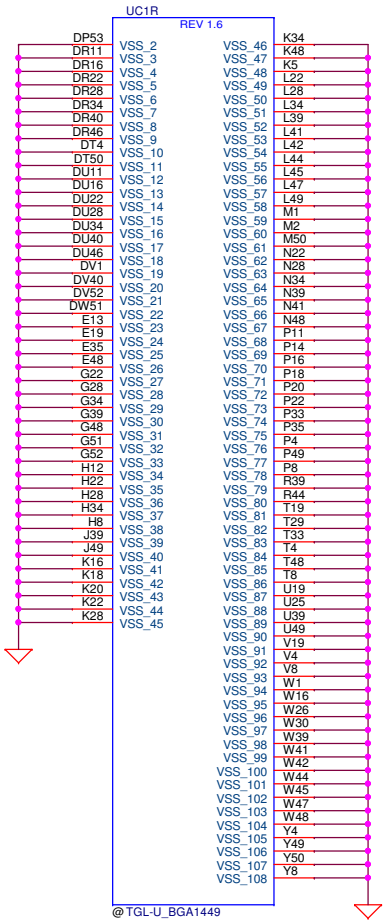
Title: **P016 - TGL-U(11/13)PCH Power**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 16 of 100







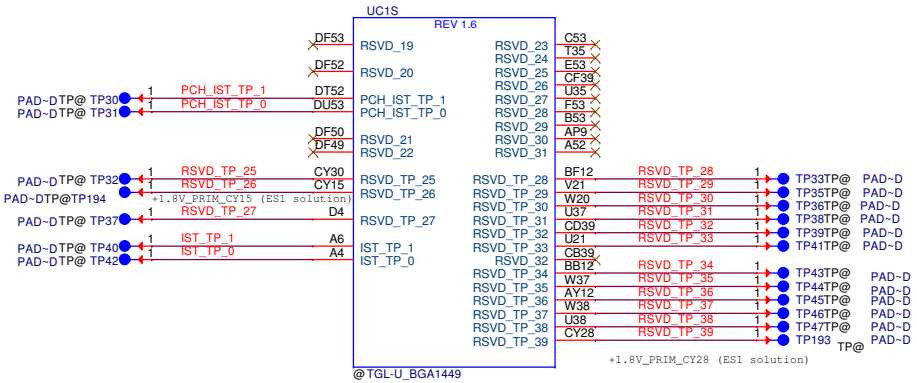
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P017 - TGL-U(12/13)GND**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 17 of 100



ES1 Workaround Circuit
Intel Document Number: 614056

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P018 - TGL-U(13/13)RSVD**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 Sheet 18 of 100

Main Function:

Reserve

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 19 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 20 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 21 of 101

Main Function:

Reserve

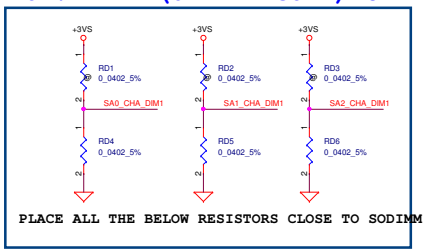
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: (RSVD)		
Size	Document Number: LA-K036P	Rev: 0.1
Date: Monday, March 08, 2021	Sheet 22 of 101	

Main Func = DDR4(1/2)

CHANNEL-M0

BOT: DIMM1(JDIMM2 CONN)Non-ECC DIMM



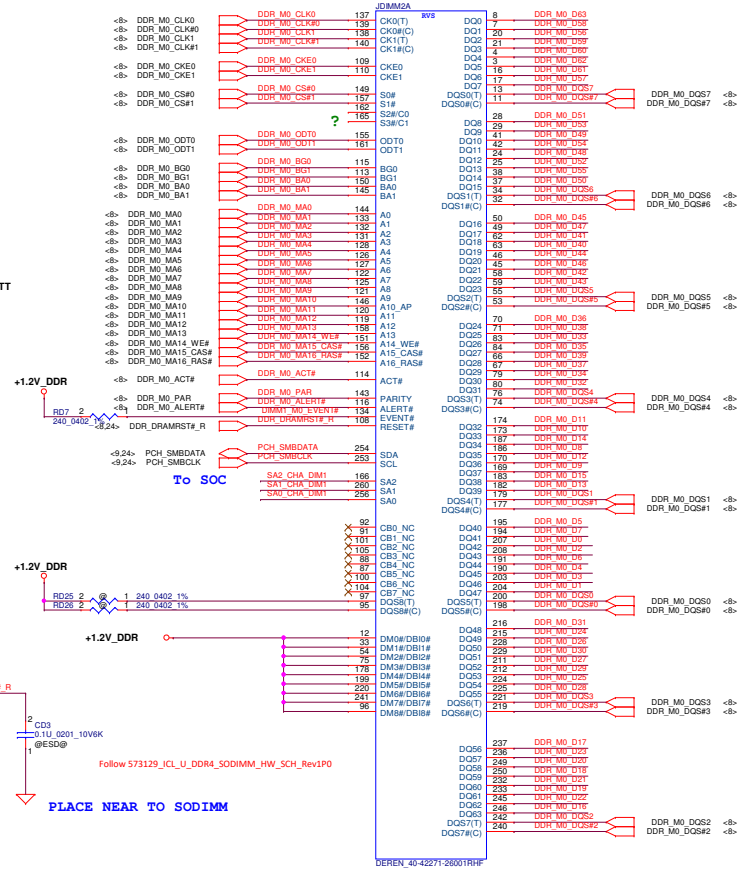
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

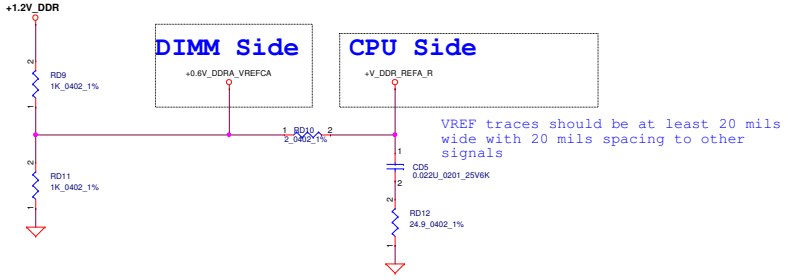
SPD ADDRESS FOR CHANNEL A :

SA0 = 0; SA1 = 0; SA2 = 0.

Non-Interleaved Memory

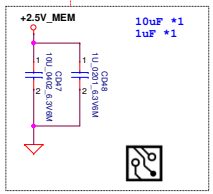
REVERSE TYPE (5.2 mm)



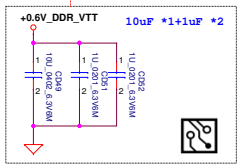


Decoupling Cap._Channel A

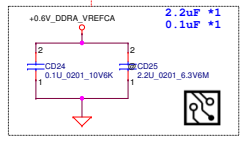
Layout Note:
Place near JDIMM2.257,259



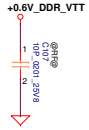
Layout Note:
Place near JDIMM2.258

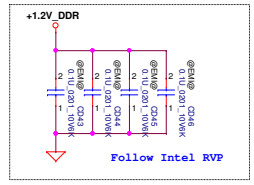


Layout Note:
PLACE THE CAP near JDIMM2. 164



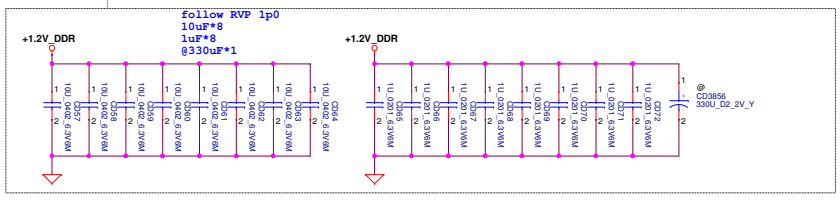
C107 place near JDIMM2



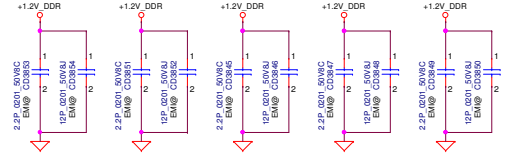


Part Number:SP07001JH00
Part Value:S SOCKET LOTES ADDR0208-P001A 260P DDR4

Layout Note:
Place near JDIMM2



EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



POP
EMI@
UNPOP
@EMI@\@ESD@\@RF@\CONN@\@

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: DDR4 CHM0: DIMM0			
Size	Document Number: LA-K036P		Rev: 0.1
Date: Monday, March 08, 2021	Sheet 23 of 101		

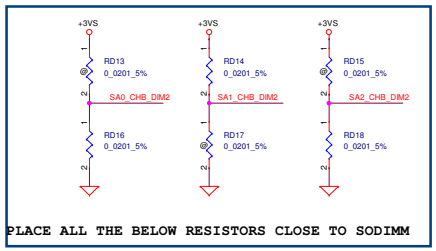
Main Func = DDR4(2/2)

CHANNEL-M1

BOT: DIMM2(JDIMM1 CONN)Non-ECC DIMM

Non-Interleaved Memory

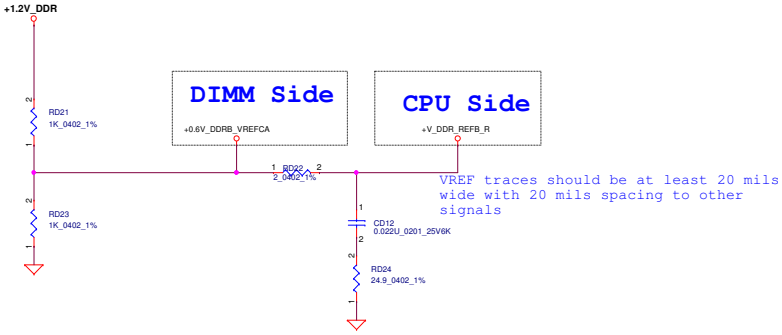
STD (5.2 mm)

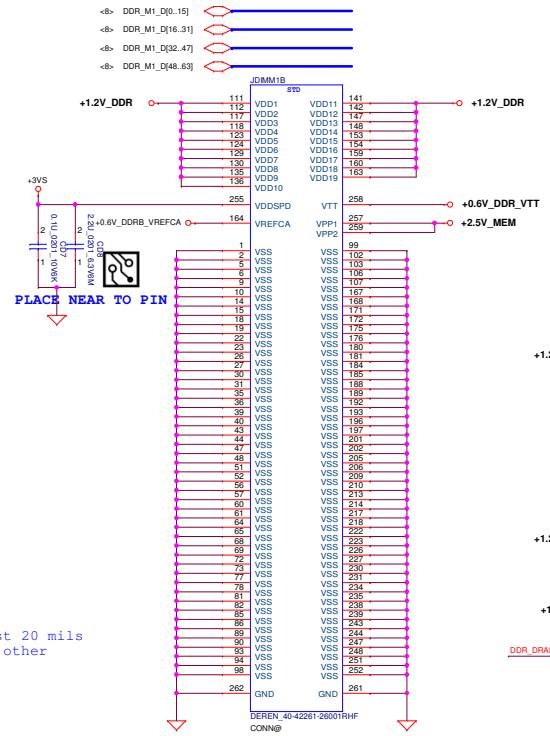


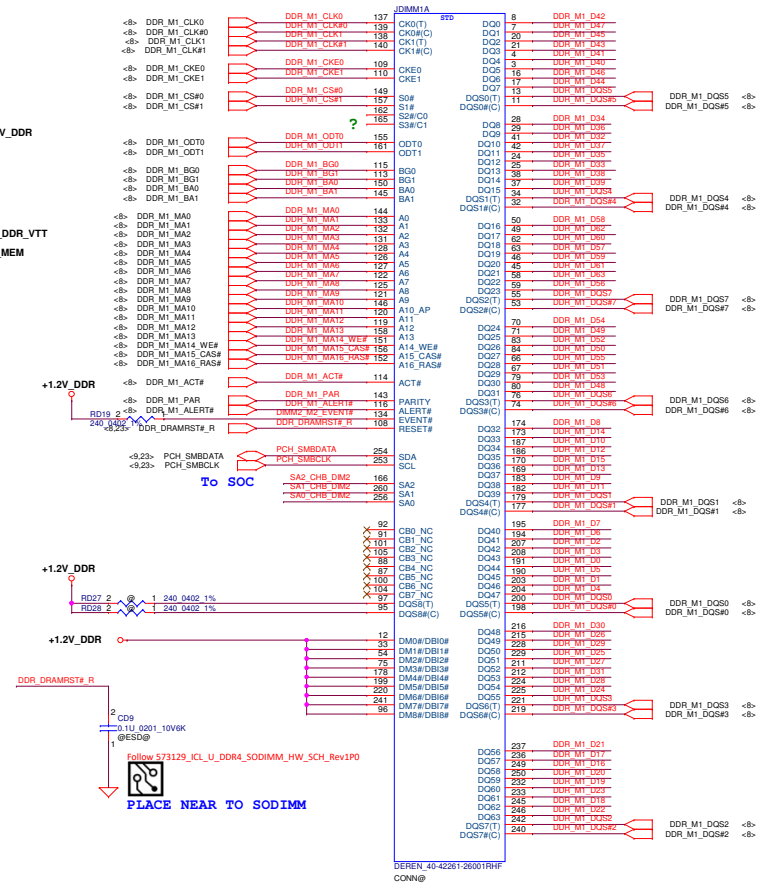
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :

SA0 = 0; SA1 = 1; SA2 = 0.

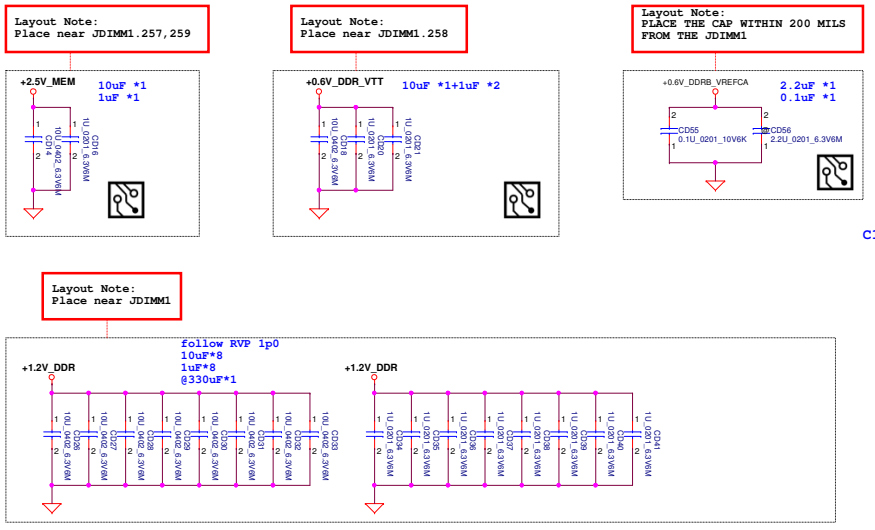




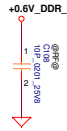


Part Number:SP07001HY00
Part Value:S SOCKET LOTES ADDR0207-P001A 260P DDR4

Decoupling Cap._Channel B



C108 place near JDIMM1



08/30
Update Table 4-26 for DDR4 SO-DIMM Decoupling Caps
572907_ICL_UY_PDG_Rev0p7 Page.99

Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)
		Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

Compal Electronics, Inc.			
Title: DDR4 CHM1: DIMM1			
Size	Document Number: LA-K036P		Rev: 0.1
Date: Monday, March 08, 2021	Sheet 24 of 101		

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 25 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 26 of 101

Main Func = GPU

PCIE X4 Bus

<12> PEG_CRX_GTX_N[0..3] — PEG_CRX_GTX_N[0..3]
<12> PEG_CRX_GTX_P[0..3] — PEG_CRX_GTX_P[0..3]
<12> PEG_CTX_GRX_N[0..3] — PEG_CTX_GRX_N[0..3]
<12> PEG_CTX_GRX_P[0..3] — PEG_CTX_GRX_P[0..3]

PCIE CLK

<11> CLKREQ_PEG#0 — CLKREQ_PEG#0
<11> CLK_PEG_P0 — CLK_PEG_P0
<11> CLK_PEG_N0 — CLK_PEG_N0

<11,51,52,66,68> PLTRST# — PLTRST#
<9,30> DGPU_HOLD_RST# — DGPU_HOLD_RST#

<30> PLT_RST_VGA# — PLT_RST_VGA#

<30,66,85> T_CRIT# — T_CRIT#
<9,31> GC6_FB_EN3V3 — GC6_FB_EN3V3

<30,37> DGPU_MAIN_EN — DGPU_MAIN_EN

<92> GPU_CORE_PG — GPU_CORE_PG
<37,94> +1.35VGS_PGOOD — +1.35VGS_PGOOD

<10,58> DGPU_PWROK — DGPU_PWROK

GPIO
Pull High with CPU Side

Reset Control

1.8V AND GATE

+1.8VS_DGPU_AON
UV12
(From PCH) PLTRST# — IN B
DGPU_HOLD_RST# — IN A
VCC, GND, OUT Y
PLT_RST_VGA#
RV378 @ 100K_0201_5%
NL17SZ08EDFT2G SOT-353
DIS@
SA0000BJI00

+1.8VS_DGPU_AON
RV4998 DIS@ 10K_0201_5%
CV757 DIS@ 0.1U_0201_6.3V6K
UV26
PLT_RST_VGA#
+1.8VS_DGPU_AON_UV26
QV150B DIS@ PJT138KA 2N SOT363-6 SB000016K00
GC6_FB_EN3V3
NL17SZ08EDFT2G SOT-353 DIS@ SA0000BJI00

+3VS
RV4996 DIS@ 100K_0201_5%
T_CRIT# — DV12 DIS@ — T_CRIT#_D — DV11 DIS@ — DGPU_MAIN_EN
RB751S-40_SOD523-2 SCS00006300
RB751S-40_SOD523-2 SCS00006300
PLT_RST_VGA#_UV26
QV150A
PJT138KA 2N SOT363-6 DIS@ SB000016K00
+3VS
RV4997 @ 10K_0201_5%
Full High with PWR Side
GPU_CORE_PG

+3VS
GPU_CORE_PG
+1.35VGS_PGOOD
UV11
DGPU_PWROK
MC74VHC1G09DFT2G_SC70-5
DIS@
Pull High with CPU Side
Open Drain

CLK_REQ

+1.8VS_DGPU_AON
RV68 DIS@ 10K_0201_5%
DGPU_PWROK
RV5001 0_0201_5% DIS@
CLKREQ_PEG#0_R — CLKREQ_PEG#0 (To SOC)
BSS138W 1N SOT-323-3
QV3
DIS@

VGS(Max) : 1.2 V

UV1A COMMON — 1/14 PCI_EXPRESS

PLT_RST_VGA#			+1.8V_AON	AB6	PEX_WAKE#	
CLKREQ_PEG#0_R			+1.8V_AON	AC7	PEX_RST#	
CLK_PEG_P0				AC6	PEX_CLKREQ#	
CLK_PEG_N0				AE8	PEX_REFCLK	
				AD8	PEX_REFCLK#	
PEG_CRX_GTX_P0	CV11	DIS@	PEG_CRX_C_GTX_P0	AC9	PEX_TX0	
PEG_CRX_GTX_N0	CV12	DIS@	PEG_CRX_C_GTX_N0	AB9	PEX_TX0#	
PEG_CTX_GRX_P0	CV1	DIS@	PEG_CTX_C_GRX_P0	AG6	PEX_RX0	
PEG_CTX_GRX_N0	CV6	DIS@	PEG_CTX_C_GRX_N0	AG7	PEX_RX0#	
PEG_CRX_GTX_P1	CV13	DIS@	PEG_CRX_C_GTX_P1	AB10	PEX_TX1	
PEG_CRX_GTX_N1	CV14	DIS@	PEG_CRX_C_GTX_N1	AC10	PEX_TX1#	
PEG_CTX_GRX_P1	CV7	DIS@	PEG_CTX_C_GRX_P1	AF7	PEX_RX1	
PEG_CTX_GRX_N1	CV8	DIS@	PEG_CTX_C_GRX_N1	AE7	PEX_RX1#	
PEG_CRX_GTX_P2	CV15	DIS@	PEG_CRX_C_GTX_P2	AD11	PEX_TX2	
PEG_CRX_GTX_N2	CV16	DIS@	PEG_CRX_C_GTX_N2	AC11	PEX_TX2#	
PEG_CTX_GRX_P2	CV19	DIS@	PEG_CTX_C_GRX_P2	AE9	PEX_RX2	
PEG_CTX_GRX_N2	CV20	DIS@	PEG_CTX_C_GRX_N2	AF9	PEX_RX2#	
PEG_CRX_GTX_P3	CV17	DIS@	PEG_CRX_C_GTX_P3	AC12	PEX_TX3	
PEG_CRX_GTX_N3	CV18	DIS@	PEG_CRX_C_GTX_N3	AB12	PEX_TX3#	
PEG_CTX_GRX_P3	CV21	DIS@	PEG_CTX_C_GRX_P3	AG9	PEX_RX3	
PEG_CTX_GRX_N3	CV22	DIS@	PEG_CTX_C_GRX_N3	AG10	PEX_RX3#	

All caps: 0.22U_0201_6.3V6M

AB13 PEX_TX4 / AC13 PEX_TX4#
AF10 PEX_RX4 / AE10 PEX_RX4#
AD14 PEX_TX5 / AC14 PEX_TX5#
AE12 PEX_RX5 / AF12 PEX_RX5#
AC15 PEX_TX6 / AB15 PEX_TX6#
AG12 PEX_RX6 / AG13 PEX_RX6#
AB16 PEX_TX7 / AC16 PEX_TX7#
AF13 PEX_RX7 / AE13 PEX_RX7#
NC FOR GM108

AD17 PEX_TX8 / AC17 PEX_TX8#
AE15 PEX_RX8 / AF15 PEX_RX8#
AC18 PEX_TX9 / AB18 PEX_TX9#
AG15 PEX_RX9 / AG16 PEX_RX9#
AB19 PEX_TX10 / AC19 PEX_TX10#
AF16 PEX_RX10 / AE16 PEX_RX10#
AD20 PEX_TX11 / AC20 PEX_TX11#
AE18 PEX_RX11 / AF18 PEX_RX11#
AC21 PEX_TX12 / AB21 PEX_TX12#
AG18 PEX_RX12 / AG19 PEX_RX12#
AD23 PEX_TX13 / AE23 PEX_TX13#
AF19 PEX_RX13 / AE19 PEX_RX13#
AF24 PEX_TX14 / AE24 PEX_TX14#
AE21 PEX_RX14 / AF21 PEX_RX14#
AG24 PEX_TX15 / AG25 PEX_TX15#
AG21 PEX_RX15 / AG22 PEX_RX15#
NC FOR GF117/GK208/GM108

N17S-G2-A1_FCBGA_595P
@

Power rails

PEX_IOVDD — AA22, AB23, AC24, AD25, AE26, AE27
Place near balls: AA22, AE27
Place near BGA
Midway GPU & VR
+1.0VS_DGPU
CV202 DIS@ 1U_0201_6.3V6M
CV222 DIS@ 1U_0201_6.3V6M
CV205 DIS@ 4.7U_0402_6.3V6M
CV2 DIS@ 4.7U_0402_6.3V6M
CV393 DIS@ 4.7U_0402_6.3V6M
CV199 DIS@ 10U_0603_6.3V6M
CV204 DIS@ 10U_0603_6.3V6M
CV9 DIS@ 22U_0603_6.3V6M
CV767 DISRF@ 100P_0201_25V8J
CV768 DISRF@ 0.1U_0201_6.3V6K
CV931 DISRF@ 10P_0201_25V8

PEX_IOVDDQ — AA10, AA12, AA13, AA16, AA18, AA19, AA20, AA21, AB22, AC23, AD24, AE25, AF26, AF27
Place near balls: AA10, AA16, AB22, AF27
Place near BGA
Midway GPU & VR
+1.8VS_DGPU_MAIN
+PEX_IOVDDQ
CV201 DIS@ 1U_0201_6.3V6M
CV200 DIS@ 1U_0201_6.3V6M
CV390 DIS@ 1U_0201_6.3V6M
CV391 DIS@ 1U_0201_6.3V6M
CV392 DIS@ 4.7U_0402_6.3V6M
CV3 DIS@ 4.7U_0402_6.3V6M
CV198 DIS@ 10U_0402_6.3V6M
CV203 DIS@ 10U_0402_6.3V6M
CV10 DIS@ 22U_0603_6.3V6M
CV770 DISRF@ 100P_0201_25V8J
CV769 DISRF@ 0.1U_0201_6.3V6K
RV4970 1 DIS@ 2 0_0402_5%

NC FOR GF119
PEX_PLL_HVDD — AA8, AA9
+PEX_PLL_HVDD
RV4976 1 DIS@ 2 0_0402_5%
CV207 DIS@ 0.1U_0201_6.3V6K
Place near ball
PEX_SVDD_3V3 — AB8

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	

VDD_SENSE — F2 — VDD_SENSE_GPU — VDD_SENSE_GPU <92>
GND_SENSE — F1 — GND_SENSE_GPU — GND_SENSE_GPU <92>
To POWER
trace width: 16mils
differential voltage sensing.
differential signal routing.

PEX_TSTCLK_OUT — AF22
PEX_TSTCLK_OUT# — AE22

PEX_PLLVDD — AA14
PEX_PLLVDD — AA15

TESTMODE — AD9 — GPU_TESTMODE — GPU_TESTMODE <30>

PEX_TERMP — AF25 — PEX_TERMP
RV376 DIS@ 2.49K_0201_1%

UV1 — SA0000D2G1L — N17S_G3_R3@
S IC N17S-G3-A1 BGA 595P GPU A31 !

UV1 — SA0000D2G0L — N17S_G3_R1@
S IC N17S-G3-A1 BGA 595P GPU

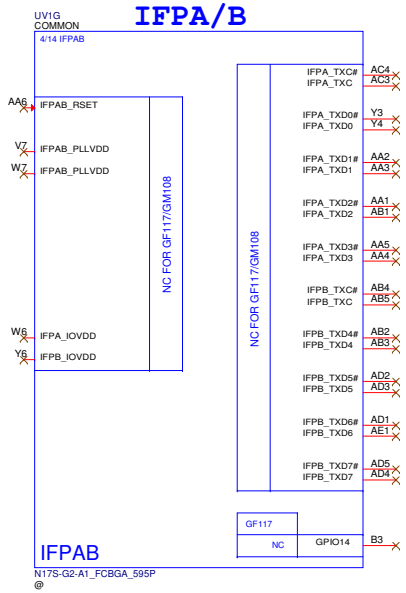
Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

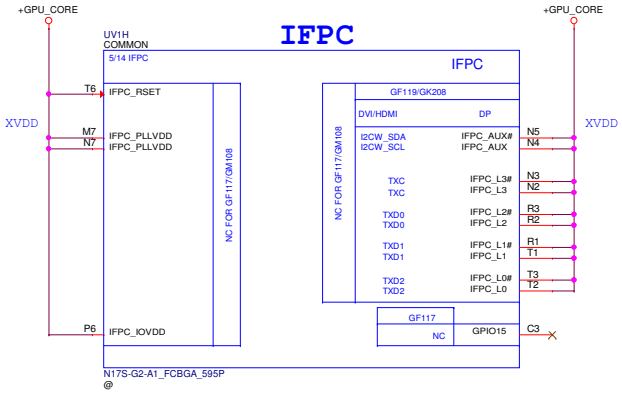
Title: NV(1/5)-PCIE
Size: — Document Number: LA-K036P — Rev: 0.1
Date: Monday, March 08, 2021 — Sheet 27 of 101

Main Func = GPU

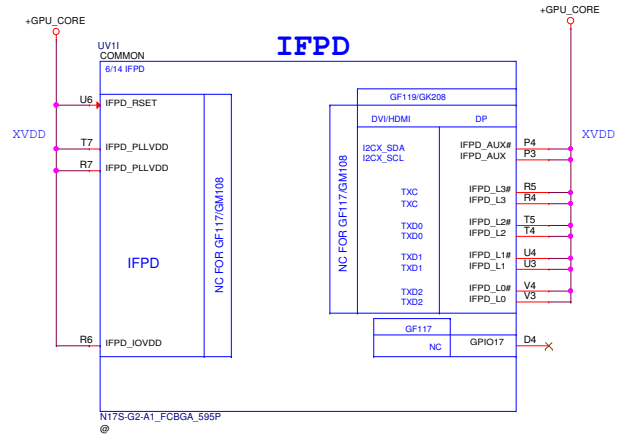
IFPA/B



IFPC

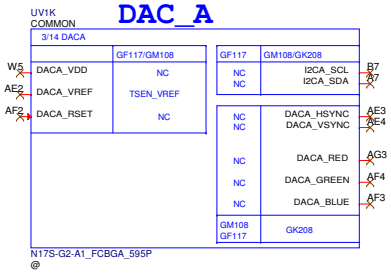


IFPD



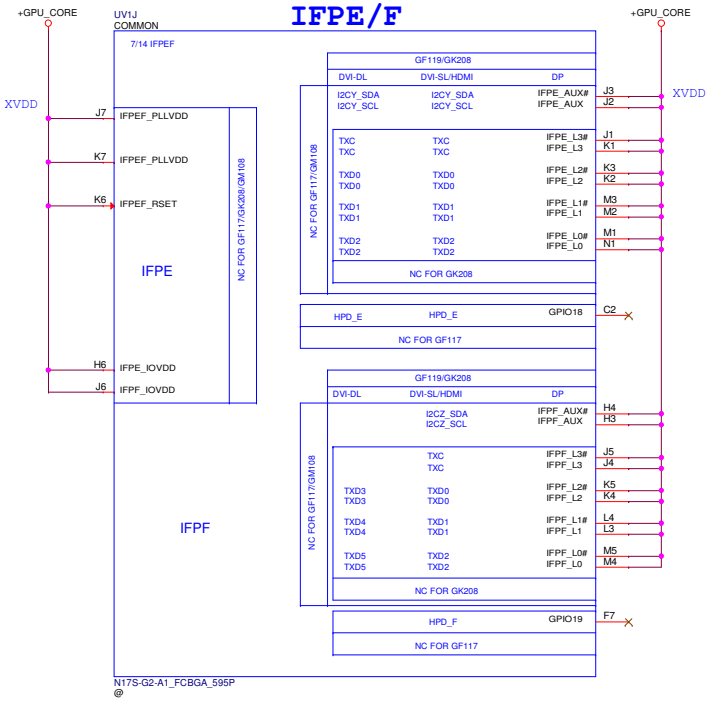
Note:
IFPC/D/E/F interface are XVDDs pin for N17S GPU, and connect them to NVVDD power for improving NVVDD power rail routing

DAC_A



Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
GPCPLL_AVDDx XS_PLLVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 22uF (0805)
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 4.7uF (0402)

IFPE/F



X'TAL

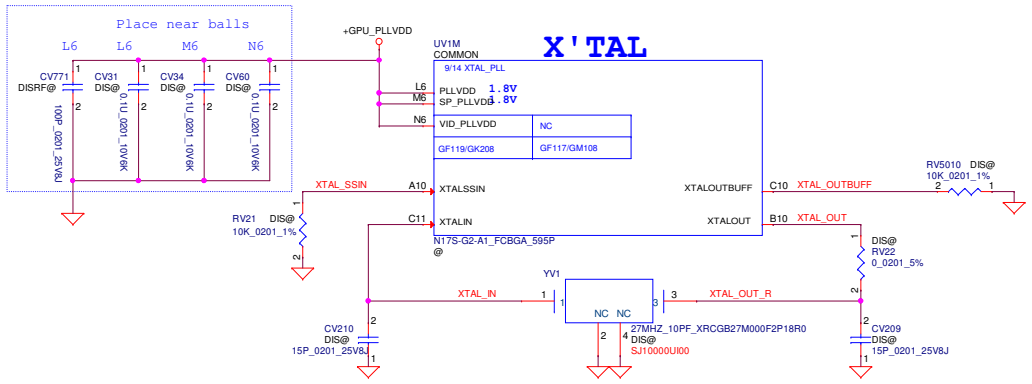


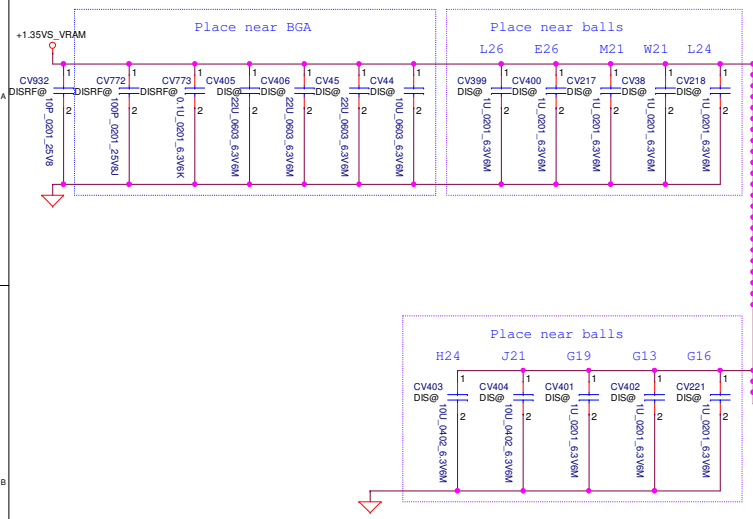
Table 11-1. Crystal Specifications

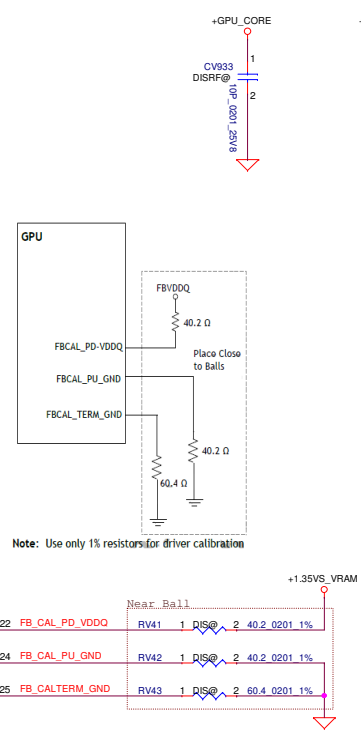
Parameter/Description	Tolerance
Nominal Frequency	27.0000 MHz
Oscillation Type	Fundamental
Operating Temperature	0 to 85°C
Absolute accuracy with respect to frequency at room temperature (25° C)	± 30 ppm
Variation over temperature range (From 0 degrees C to 70 degrees C)	± 30 ppm
Variation over time (typically 1 year)	± 5 ppm
Note: Crystal load capacitors should have 5% accuracy for best results, the value of the capacitors should be chosen according to manufacturer's specification.	

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

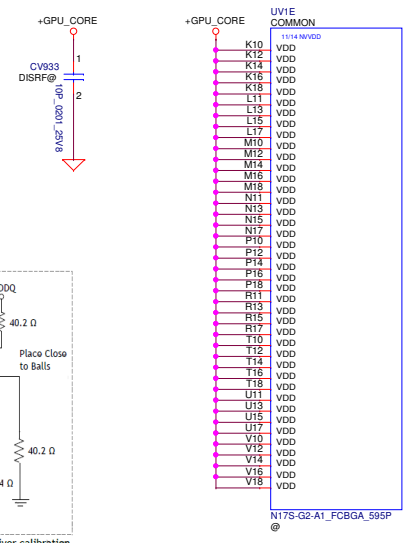
Compal Electronics, Inc.	
Title	NV(2/5)-IFP_ABCDEF_DAC_XTAL
Size	Document Number: LA-K036P
Rev	0.1
Date: Monday, March 08, 2021	Sheet 28 of 101

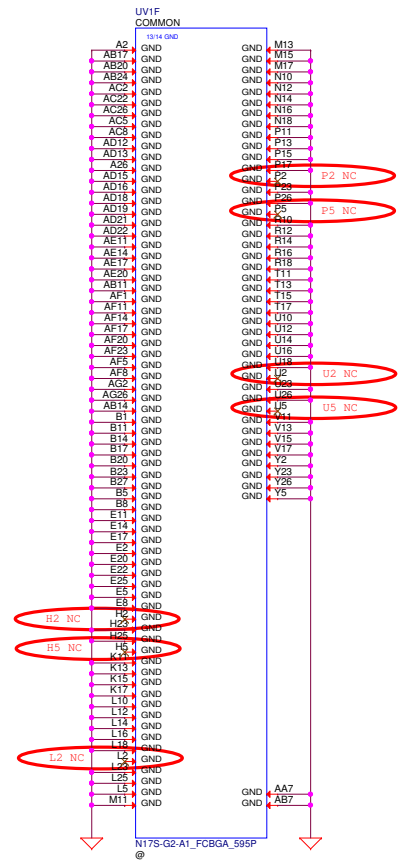
Main Func = GPU





Note: Use only 1% resistors for driver calibration



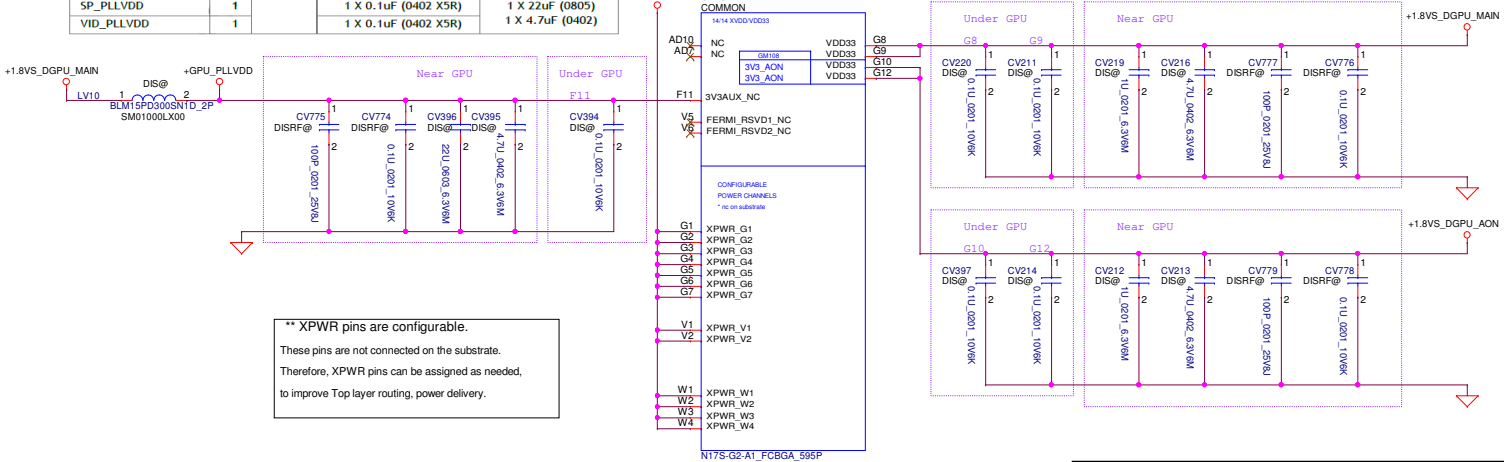


Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)

Voltage by GPU SKU

GPU_Decoupling CAPs @ Power Page

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
GPCPLL AVDDx XS_PLLVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	



** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed,

to improve Top layer routing, power delivery.

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: NV(3/5)-POWER

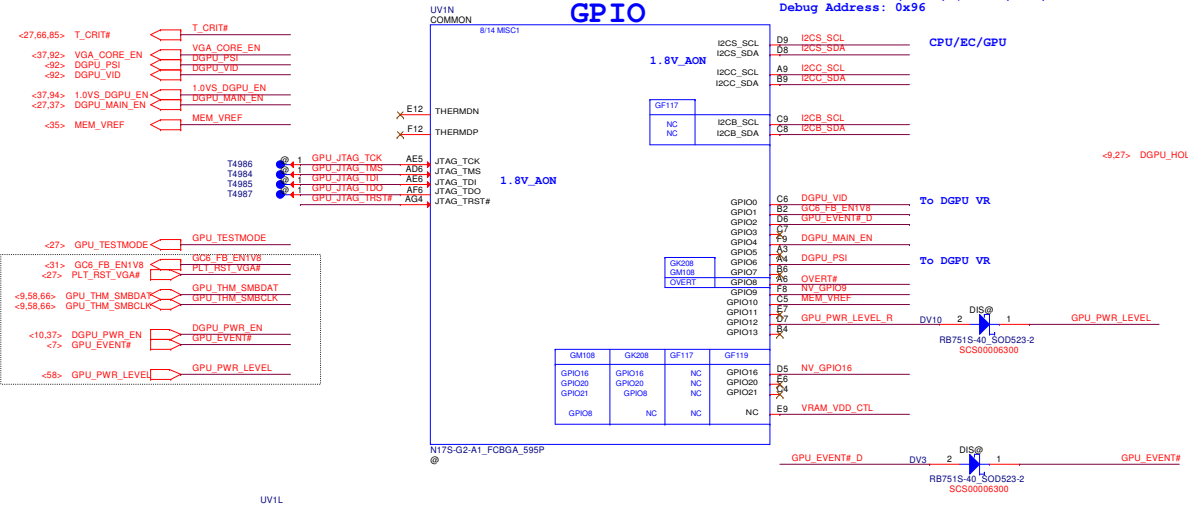
Size: | Document Number: LA-K036P | Rev: 0.1

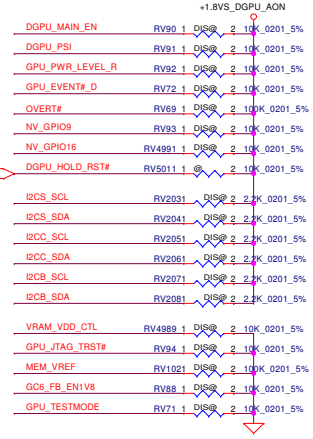
Date: Monday, March 08, 2021 | Sheet 29 of 101

Main Func = GPU

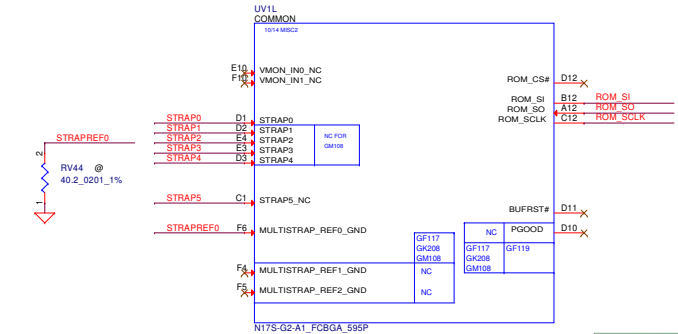
GPIO

I2CS SMBUS: 0x9E(write) , 0x9F(read) -->default
0x9C(write) , 0x9D(read) -->alternate for dual GPU
Debug Address: 0x96





GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT*/ WAKE*	I	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AOH, unless driven actively.
GPIO3	NVVDDS_PWM	I/O	PWM output to control the NVVDDS power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO5	FRM_LCK*	I	Active low Frame Lock	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO6	NVVDD_PSI*/ NVVDDS_PSI*	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AOH to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD_EN / Quadro:Power_Brake*	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AOH
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB*	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON*	I	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AOH unless actively driven
GPIO17	UNUSED	I/O		
GPIO18	UNUSED	I/O		
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO21	MEM_VDD_CTL	O	Frame Buffer VDD select	Open Drain; Pull-up/pull-down to set the FBVDD/Q power-on voltage at boot up
GPIO22	UNUSED	I/O		
GPIO23	GC6M: GPU_PEX_RST_HOLD*	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to gated 3V3



EXPOSED STRAP

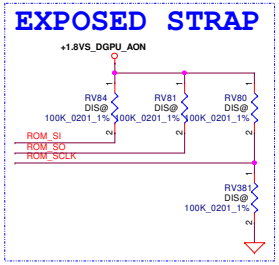
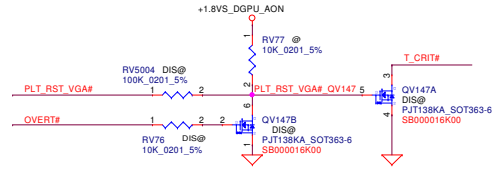
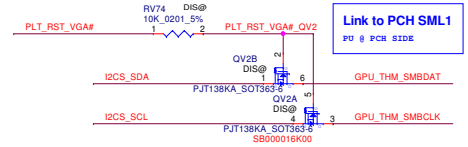


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

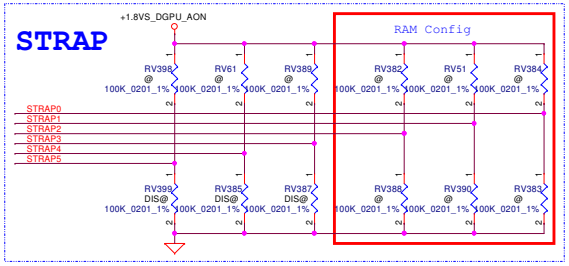
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			



Internal Thermal Sensor



STRAP



Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

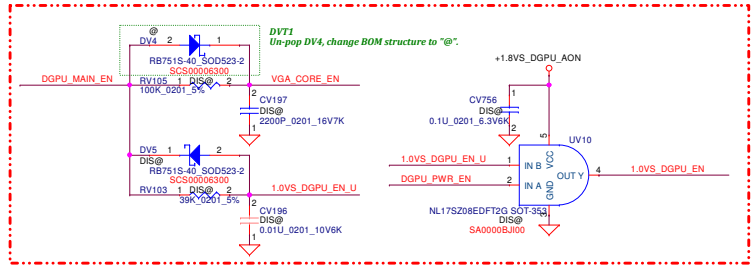


Table 6. N17S-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production ready

Notes:
1. For N17S-G0/G2/G3/G4, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

RAM_CFG	STRAP2	STRAP1	STRAP0
0x09 (LML) M2G	RV388 M_STRAP@	RV390 M_STRAP@ RV51 M_STRAP@	RV383 M_STRAP@
0x0A (LMH) H2G	RV388 H_STRAP@	RV390 H_STRAP@ RV51 H_STRAP@	RV384 H_STRAP@
0x03 (LHH) S2G	RV388 S_STRAP@	RV51 S_STRAP@	RV384 S_STRAP@

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

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Title: NV(4/5)-GPIO/Strap

Size: | Document Number: LA-K036P | Rev: 0.1

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Main Func = GPU

For GC6

<30> GC6_FB_EN1V8 → GC6_FB_EN1V8
<9,27> GC6_FB_EN3V3 → GC6_FB_EN3V3

<94> +1.0VS_DGPU_PGOOD → +1.0VS_DGPU_PGOOD
<37,94> 1.35V_PWR_EN → 1.35V_PWR_EN

Can set GPIO to 1.8V to cost down level shift circuit
if pop RV5012 need check double PU

GC6_FB_EN1V8 RV5012 1 @ 2 0_0201_5% GC6_FB_EN3V3

UV1B
COMMON
2/14 FBA

<35> FB_A_D[0..31]
<36> FB_A_D[32..63]

FB_A_D0	E18	FBA_D0
FB_A_D1	F18	FBA_D1
FB_A_D2	E16	FBA_D2
FB_A_D3	F17	FBA_D3
FB_A_D4	D20	FBA_D4
FB_A_D5	D21	FBA_D5
FB_A_D6	F20	FBA_D6
FB_A_D7	E21	FBA_D7
FB_A_D8	E15	FBA_D8
FB_A_D9	D15	FBA_D9
FB_A_D10	F15	FBA_D10
FB_A_D11	F13	FBA_D11
FB_A_D12	C13	FBA_D12
FB_A_D13	B13	FBA_D13
FB_A_D14	E13	FBA_D14
FB_A_D15	D13	FBA_D15
FB_A_D16	B15	FBA_D16
FB_A_D17	C16	FBA_D17
FB_A_D18	A13	FBA_D18
FB_A_D19	A15	FBA_D19
FB_A_D20	B18	FBA_D20
FB_A_D21	A18	FBA_D21
FB_A_D22	A19	FBA_D22
FB_A_D23	C19	FBA_D23
FB_A_D24	B24	FBA_D24
FB_A_D25	C23	FBA_D25
FB_A_D26	A25	FBA_D26
FB_A_D27	A24	FBA_D27
FB_A_D28	A21	FBA_D28
FB_A_D29	B21	FBA_D29
FB_A_D30	C20	FBA_D30
FB_A_D31	C21	FBA_D31
FB_A_D32	R22	FBA_D32
FB_A_D33	R24	FBA_D33
FB_A_D34	T22	FBA_D34
FB_A_D35	R23	FBA_D35
FB_A_D36	N25	FBA_D36
FB_A_D37	N26	FBA_D37
FB_A_D38	N23	FBA_D38
FB_A_D39	N24	FBA_D39
FB_A_D40	V23	FBA_D40
FB_A_D41	V22	FBA_D41
FB_A_D42	T23	FBA_D42
FB_A_D43	U22	FBA_D43
FB_A_D44	Y24	FBA_D44
FB_A_D45	AA24	FBA_D45
FB_A_D46	Y22	FBA_D46
FB_A_D47	AA23	FBA_D47
FB_A_D48	AD27	FBA_D48
FB_A_D49	AB25	FBA_D49
FB_A_D50	AD26	FBA_D50
FB_A_D51	AC25	FBA_D51
FB_A_D52	AA27	FBA_D52
FB_A_D53	AA26	FBA_D53
FB_A_D54	W26	FBA_D54
FB_A_D55	Y25	FBA_D55
FB_A_D56	R26	FBA_D56
FB_A_D57	T25	FBA_D57
FB_A_D58	N27	FBA_D58
FB_A_D59	R27	FBA_D59
FB_A_D60	V26	FBA_D60
FB_A_D61	V27	FBA_D61
FB_A_D62	W27	FBA_D62
FB_A_D63	W25	FBA_D63

NC / GF119 → FB_CLAMP F3

FBA_CMD0 C27 FB_A_CMD0 → FB_A_CMD[0..15] <35>
FBA_CMD1 C26 FB_A_CMD1
FBA_CMD2 E24 FB_A_CMD2
FBA_CMD3 F24 FB_A_CMD3
FBA_CMD4 D27 FB_A_CMD4
FBA_CMD5 D26 FB_A_CMD5
FBA_CMD6 F25 FB_A_CMD6
FBA_CMD7 F26 FB_A_CMD7
FBA_CMD8 F23 FB_A_CMD8
FBA_CMD9 G22 FB_A_CMD9
FBA_CMD10 G23 FB_A_CMD10
FBA_CMD11 G24 FB_A_CMD11
FBA_CMD12 F27 FB_A_CMD12
FBA_CMD13 G25 FB_A_CMD13
FBA_CMD14 G27 FB_A_CMD14
FBA_CMD15 G26 FB_A_CMD15 → FB_A_CMD[16..31] <36>
FBA_CMD16 M24 FB_A_CMD16
FBA_CMD17 M23 FB_A_CMD17
FBA_CMD18 K24 FB_A_CMD18
FBA_CMD19 K23 FB_A_CMD19
FBA_CMD20 M27 FB_A_CMD20
FBA_CMD21 M26 FB_A_CMD21
FBA_CMD22 M25 FB_A_CMD22
FBA_CMD23 K26 FB_A_CMD23
FBA_CMD24 K22 FB_A_CMD24
FBA_CMD25 J23 FB_A_CMD25
FBA_CMD26 J25 FB_A_CMD26
FBA_CMD27 J24 FB_A_CMD27
FBA_CMD28 K27 FB_A_CMD28
FBA_CMD29 K25 FB_A_CMD29
FBA_CMD30 J27 FB_A_CMD30
FBA_CMD31 J26 FB_A_CMD31

GDDR5_BGA170_MIRR COMMAND MAP

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

+3VS
RV111 100K_0201_5% DIS@
RV113 100K_0201_5% DIS@
GC6_FB_EN3V3
GC6_FB_EN3V3_Q
QV8A DIS@ PJT138KA 2N SOT363-6 SB000016K00
GC6_FB_EN1V8
QV8B DIS@ PJT138KA 2N SOT363-6 SB000016K00

+1.8VS_DGPU_AON
GC6_FB_EN3V3
+1.0VS_DGPU_PGOOD
UV23 FBVDD/Q_EN
1.35V_PWR_EN
74LVC1G32GW_TSSOP5 SA000014S00 DIS@
1.8V OR GATE

From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

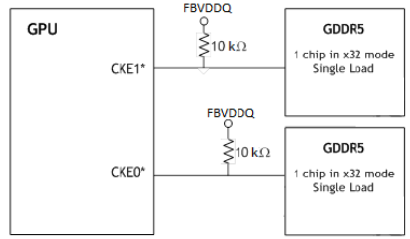

Figure 7-4. Clock Enable (CKE*) Signal Connection, ×32 Mode

<35> FB_A_DBI0 FB_A_DBI0 D19 FBA_DQM0
<35> FB_A_DBI1 FB_A_DBI1 D14 FBA_DQM1
<35> FB_A_DBI2 FB_A_DBI2 C17 FBA_DQM2
<35> FB_A_DBI3 FB_A_DBI3 C22 FBA_DQM3
<36> FB_A_DBI4 FB_A_DBI4 P24 FBA_DQM4
<36> FB_A_DBI5 FB_A_DBI5 W24 FBA_DQM5
<36> FB_A_DBI6 FB_A_DBI6 AA25 FBA_DQM6
<36> FB_A_DBI7 FB_A_DBI7 U25 FBA_DQM7

GF117/GF119/GK208
NC
FBA_DEBUG0
FBA_DEBUG1
FBA_CMD32 B19
FBA_CMD34 F22
FBA_CMD35 J22
T20 @
T21 @

FBVDDQ_GPU
1.35V

GDDR5 design
FBA_CKE_L / FBA_CKE_H
FB_A_CMD14 RV2439 1 DIS@ 2 10K_0201_1%
FB_A_CMD30 RV2440 1 DIS@ 2 10K_0201_1%
FBA_RST_L / FBA_RST_H
FB_A_CMD13 RV2437 1 DIS@ 2 10K_0201_1%
FB_A_CMD29 RV2438 1 DIS@ 2 10K_0201_1%
+1.35VS_VRAM

<35> FB_A_EDC0 FB_A_EDC0 E19 FBA_DQS_WP0
<35> FB_A_EDC1 FB_A_EDC1 C15 FBA_DQS_WP1
<35> FB_A_EDC2 FB_A_EDC2 B16 FBA_DQS_WP2
<35> FB_A_EDC3 FB_A_EDC3 B22 FBA_DQS_WP3
<36> FB_A_EDC4 FB_A_EDC4 R25 FBA_DQS_WP4
<36> FB_A_EDC5 FB_A_EDC5 W23 FBA_DQS_WP5
<36> FB_A_EDC6 FB_A_EDC6 AB26 FBA_DQS_WP6
<36> FB_A_EDC7 FB_A_EDC7 T26 FBA_DQS_WP7

F19 FBA_DQS_RN0
C14 FBA_DQS_RN1
A16 FBA_DQS_RN2
A22 FBA_DQS_RN3
P23 FBA_DQS_RN4
W22 FBA_DQS_RN5
AB27 FBA_DQS_RN6
T27 FBA_DQS_RN7

FBA_CLK0 D24 FB_A_CLK0 → FB_A_CLK0 <35>
FBA_CLK0# D25 FB_A_CLK#0 → FB_A_CLK#0 <35>
FBA_CLK1 N22 FB_A_CLK1 → FB_A_CLK1 <36>
FBA_CLK1# M22 FB_A_CLK#1 → FB_A_CLK#1 <36>

FBA_WCK01 D18 FB_A_WCK0 → FB_A_WCK0 <35>
FBA_WCK01# C18 FB_A_WCK#0 → FB_A_WCK#0 <35>
FBA_WCK23 D17 FB_A_WCK1 → FB_A_WCK1 <35>
FBA_WCK23# D16 FB_A_WCK#1 → FB_A_WCK#1 <35>
FBA_WCK45 T24 FB_A_WCK2 → FB_A_WCK2 <36>
FBA_WCK45# U24 FB_A_WCK#2 → FB_A_WCK#2 <36>
FBA_WCK67 V24 FB_A_WCK3 → FB_A_WCK3 <36>
FBA_WCK67# V25 FB_A_WCK#3 → FB_A_WCK#3 <36>

GF119
NC
FB_PLLAVDD F16
FB_PLLAVDD P22
FB_PLLAVDD H22
GF117
FB_DLLAVDD

Place near balls
CV55 DIS@ 0.1U_0201_10V6K
CV52 DIS@ 0.1U_0201_10V6K
CV53 DIS@ 0.1U_0201_10V6K
CV398 DIS@ 0.1U_0201_10V6K
CV51 DIS@ 220U_0603_6.3V6M
CV781 DISRF@ 10P_0201_25V8
CV780 DIS@ 0.1U_0201_6.3V6K
CV783 DISRF@ 100P_0201_25V8J
CV782 DISRF@ 100P_0201_25V8J
CV784 DISRF@ 100P_0201_25V8J
CV785 DISRF@ 2200P_0201_16V7K
+FB_PLLAVDD
LV7 DIS@ BLM15PD300SN1D_2P SM01000LX00
+1.8VS_DGPU_MAIN

For VRAM DEBUG using
T4988 @ 1 FB_VREF D23 FB_VREF_PROBE

N17S-G2-A1_FCBGA_595P
@

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 kΩ pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

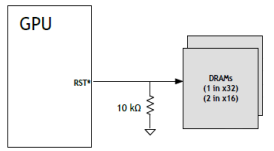

Figure 7-3. Reset Signal Connection

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 30Ω bead (0603 max ESR 10 mΩ) 1 X 22uF (0805)
FBB_PLL_AVDD	1			
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	

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Issued Date	2018/08/31	Deciphered Date	2019/08/06

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Title: NV(5/5)-MEMORY FBA
Size: | Document Number: LA-K036P | Rev: 0.1
Date: Monday, March 08, 2021 | Sheet 31 of 101

Reserve

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Issued Date	2018/08/31	Deciphered Date	2019/08/06

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Title: **Reserve**

Size | Document Number: **LA-K036P** | Rev: 0.1

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Reserve

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Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: **SMbus Block Diagram**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 Sheet 33 of 101

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: **SMbus Block Diagram**

Size	Document Number	Rev
	LA-K036P	0.1

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Main Func = VRAM

Memory Partition A

<31> FB_A_CMD[0..15] — FB_A_CMD[0..15]
<31> FB_A_D[0..31] — FB_A_D[0..31]
<36> +FBA_VREFC0 — +FBA_VREFC0
<30> MEM_VREF — MEM_VREF

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to DRAM, see section 7.1.13.

UV6 MF=0

FB_A_EDC0 C2 EDC0 EDC3
FB_A_EDC1 C13 EDC1 EDC2
FB_A_EDC2 R13 EDC2 EDC1
FB_A_EDC3 R2 EDC3 EDC0

FB_A_DBI0 D2 DBI0# DBI3#
FB_A_DBI1 D13 DBI1# DBI2#
FB_A_DBI2 P13 DBI2# DBI1#
FB_A_DBI3 P2 DBI3# DBI0#

FB_A_CLK0 J12 CK
FB_A_CLK#0 J11 CK#
FB_A_CMD14 J3 CKE#

FB_A_CMD2 H11 BA0/A2 BA2/A4
FB_A_CMD4 K10 BA1/A5 BA3/A3
FB_A_CMD3 K11 BA2/A4 BA0/A2
FB_A_CMD1 H10 BA3/A3 BA1/A5

FB_A_CMD6 K4 A8/A7 A10/A0
FB_A_CMD11 H5 A9/A1 A11/A6
FB_A_CMD10 H4 A10/A0 A8/A7
FB_A_CMD7 K5 A11/A6 A9/A1
FB_A_CMD9 J5 A12/RFU/NC

A5 VPP/NC_2
U5 VPP/NC_1

RV116 DIS@ 1 — 2 1K_0201_1% — FB_A_MF J1 MF
RV118 DIS@ 1 — 2 1K_0201_1% — FB_A_SEN J10 SEN
RV120 DIS@ 2 — 1 121_0201_1% — FB_A_ZQ J13 ZQ

FB_A_CMD8 J4 ABI#
FB_A_CMD12 G3 RAS# CAS#
FB_A_CMD0 G12 CS# WE#
FB_A_CMD15 L3 CAS# RAS#
FB_A_CMD5 L12 WE# CS#

<31> FB_A_WCK#0 — FB_A_WCK#0 D5 — WCK01# WCK23#
<31> FB_A_WCK0 — FB_A_WCK0 D4 — WCK01 WCK23
<31> FB_A_WCK#1 — FB_A_WCK#1 P5 — WCK23# WCK01#
<31> FB_A_WCK1 — FB_A_WCK1 P4 — WCK23 WCK01

A10 VREFD_1
U10 VREFD_2
+FBA_VREFC0 J14 VREFC

FB_A_CMD13 J2 RESET#

H1 K1 B5 G5 L5 T5 B10 D10 G10 L10 P10 T10 H14 K14 VSS

G1 L1 G4 L4 C5 R5 C10 R10 D11 G11 L11 P11 G14 L14 VDD

170-BALL
SGRAM GDDR5
H5GC4H24MFR-T2C
@

DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7

A4 FB_A_D0
A2 FB_A_D1
B4 FB_A_D2
B2 FB_A_D3
E4 FB_A_D4
E2 FB_A_D5
F4 FB_A_D6
F2 FB_A_D7 — BYTE0
A11 FB_A_D8
A13 FB_A_D9
B11 FB_A_D10
B13 FB_A_D11
E11 FB_A_D12
E13 FB_A_D13
F11 FB_A_D14
F13 FB_A_D15 — BYTE1
U11 FB_A_D16
U13 FB_A_D17
T11 FB_A_D18
T13 FB_A_D19
N11 FB_A_D20
N13 FB_A_D21
M11 FB_A_D22
M13 FB_A_D23 — BYTE2
U4 FB_A_D24
U2 FB_A_D25
T4 FB_A_D26
T2 FB_A_D27
N4 FB_A_D28
N2 FB_A_D29
M4 FB_A_D30
M2 FB_A_D31 — BYTE3

+1.35VS_VRAM

VDDQ: B1 D1 F1 M1 P1 T1 G2 L2 B3 D3 F3 H3 K3 M3 P3 T3 E5 N5 E10 N10 B12 D12 F12 H12 K12 M12 P12 T12 G13 L13 B14 D14 F14 M14 P14 T14

VSSQ: A1 C1 E1 N1 R1 U1 H2 K2 A3 C3 E3 N3 R3 U3 C4 F4 F5 M5 F10 M10 C11 R11 A12 C12 E12 N12 R12 U12 H13 K13 A14 C14 E14 N14 R14 U14

+1.35VS_VRAM

RV125 DIS@ 549_0201_1%
Place near pin J14 of each VRAM
W=16mils
+FBA_VREFC0
RV200 DIS@ 931_0201_1%
RV127 DIS@ 1.33K_0201_1%
CV158 DIS@ 820P_0201_25V7K
CV159 DIS@ 820P_0201_25V7K
MEM_VREF
QV50 BSS138W 1N SOT-323-3 DIS@

Near to UV6
FB_A_CLK0 — RV11 DIS@ 40.2_0201_1% — FB_A_CLK0_R — RV21 DIS@ 40.2_0201_1% — FB_A_CLK#0
CV4 DIS@ 0.01U_0201_10V6K

+1.35VS_VRAM

Near VRAM
CV601 DIS@ 22U_0603_6.3V6M
CV602 DIS@ 22U_0603_6.3V6M
CV603 DIS@ 10U_0603_6.3V6M
CV604 DIS@ 10U_0603_6.3V6M

Near ball
CV605 DIS@ 10U_0603_6.3V6M
CV606 DIS@ 10U_0603_6.3V6M
CV607 DIS@ 10U_0603_6.3V6M
CV608 DIS@ 10U_0603_6.3V6M

+1.35VS_VRAM

Near ball
CV609 DIS@ 1U_0201_6.3V6M
CV610 DIS@ 1U_0201_6.3V6M
CV611 DIS@ 1U_0201_6.3V6M
CV612 DIS@ 1U_0201_6.3V6M
CV613 DIS@ 1U_0201_6.3V6M
CV614 DIS@ 1U_0201_6.3V6M
CV615 DIS@ 1U_0201_6.3V6M
CV616 DIS@ 1U_0201_6.3V6M
CV617 DIS@ 1U_0201_6.3V6M
CV618 DIS@ 1U_0201_6.3V6M
CV765 DIS@ 1U_0201_6.3V6M
CV766 DIS@ 1U_0201_6.3V6M
CV764 DIS@ 1U_0201_6.3V6M
CV763 DIS@ 1U_0201_6.3V6M

Hynix 2G

UV6 SA0000C171L H2G_R3@ — S IC D5 256M32 H5GC8H24AJR-R2C BGA A31!
UV8 SA0000C171L H2G_R3@ — S IC D5 256M32 H5GC8H24AJR-R2C BGA A31!

Micron 2G

UV6 SA00009TI3L M2G_R3@ — S IC D5 256M32 MT51J256M32HF-80:B A31!
UV8 SA00009TI3L M2G_R3@ — S IC D5 256M32 MT51J256M32HF-80:B A31!

Samsung 2G

UV6 SA00009TA3L S2G_R3@ — S IC D5 256M32 K4G80325FC-HC25 FBGA A31!
UV8 SA00009TA3L S2G_R3@ — S IC D5 256M32 K4G80325FC-HC25 FBGA A31!

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: N17S_GDDR5_A

Size: — Document Number: LA-K036P — Rev: 0.1

Date: Monday, March 08, 2021 — Sheet 35 of 101

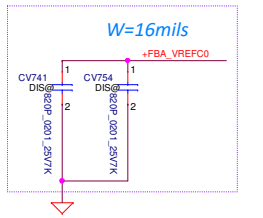
Main Func = VRAM

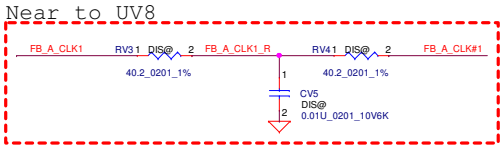
Memory Partition B

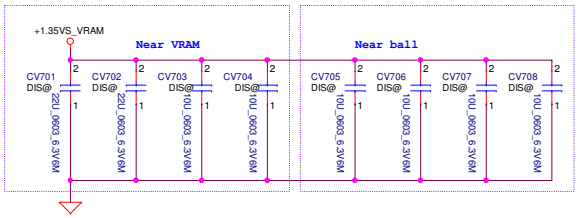
Table 7-4. GDDR5 Mode H Mapping

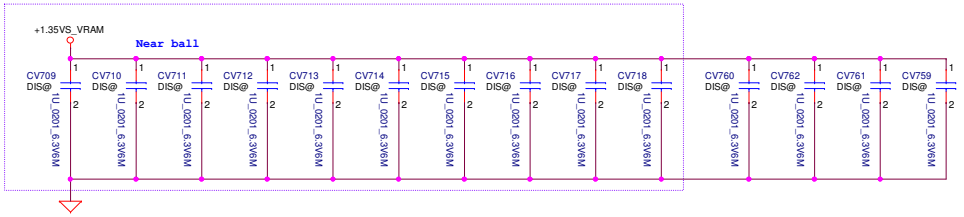
GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

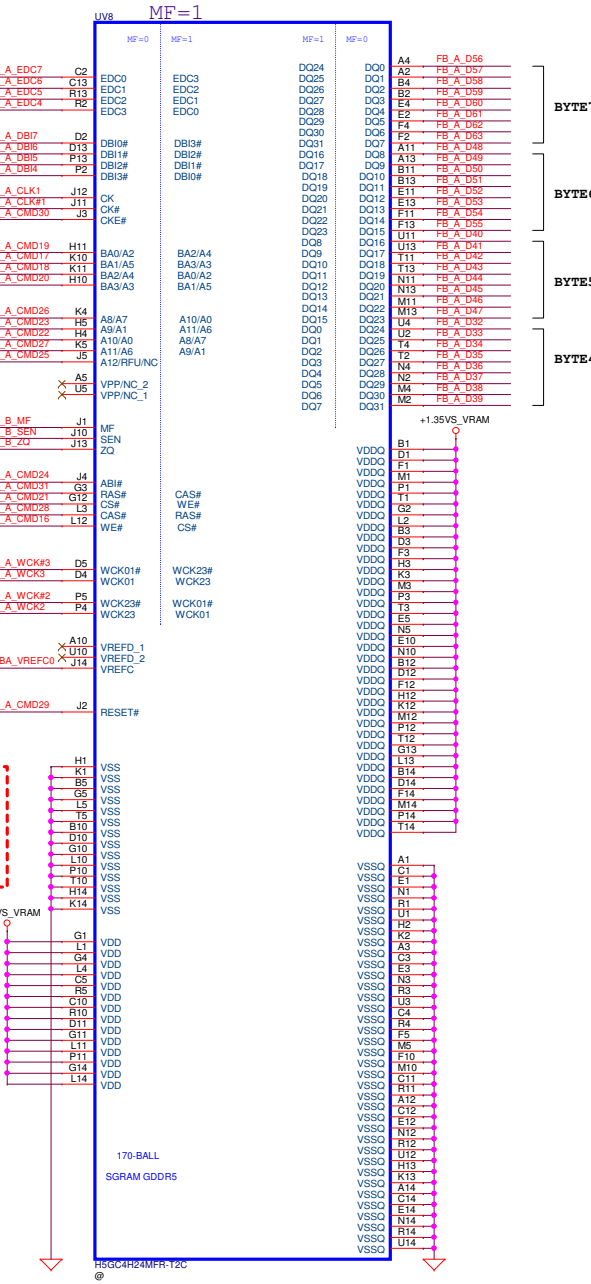
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to DRAM, see section 7.1.13.







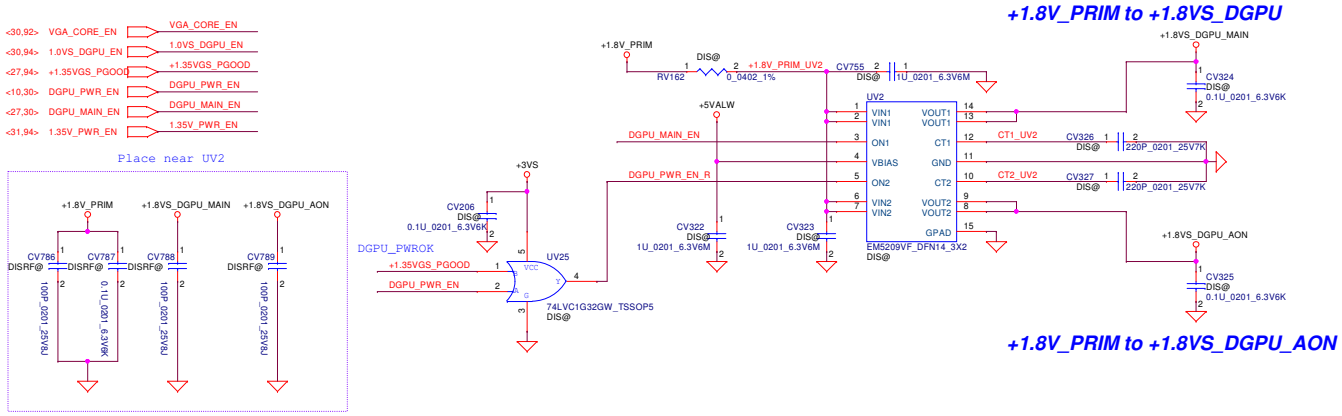


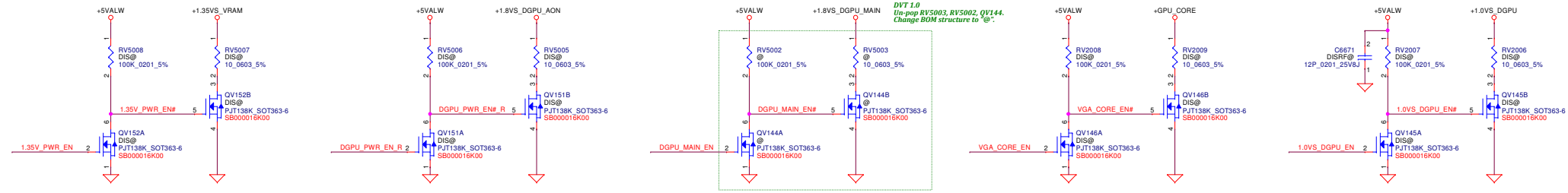


Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

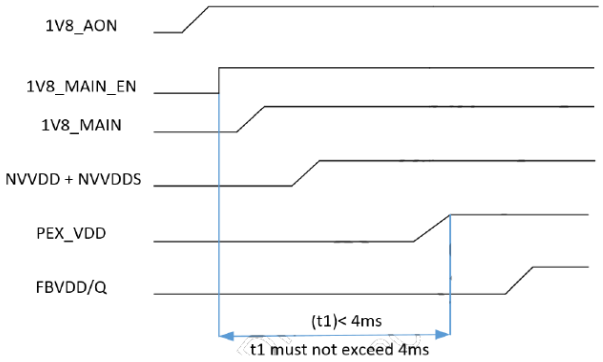
Compal Electronics, Inc.	
Title	N17S_GDDR5_B
Size	Document Number: LA-K036P
Rev	0.1
Date: Monday, March 08, 2021	Sheet 36 of 101

Main Func = GPU DC

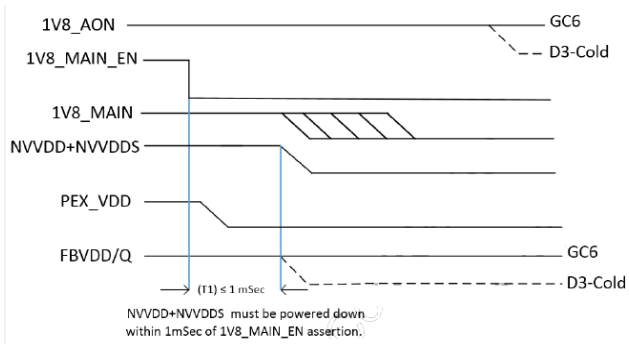




Power-Up Sequence



Power-Down Sequence



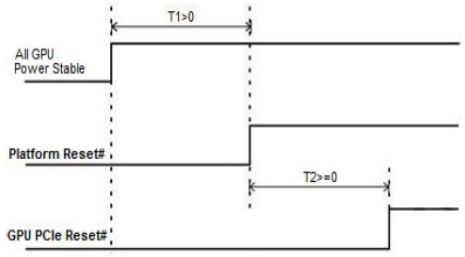
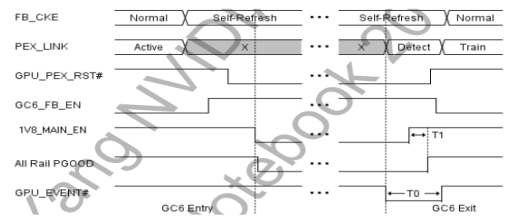
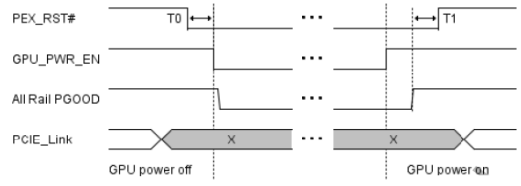


Figure 8.4 Cold Reset Sequence Requirement for Optimus



Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms



Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.
Title: DGPU_DC/DC Interface
Size: Document Number: LA-K036P
Rev: 0.1
Date: Monday, March 08, 2021 Sheet 37 of 101

Main Func = LCD

Pin 5,6,9 Cable side NC
Pin 4 for 17" CAMERA

JEDP1 CONN@
ACES_51540-04001-P01
SP010029F00

R96 close JEDP! @ 08/15

60 mils

+3VS
R90 LCD_CBL_DET# 10K_0402_5%

+DCBAT_LCD
+LCDVDD_LCD
+3VS_CAM
+MIC_VCC
+TS_VDD

LCD_TST_C
DBC_PANEL_EN_R
EDP_HPD <6>
LCD_CBL_DET# <10>
EDP_AUXP_C
EDP_AUXN_C
EDP_TXN0_C
EDP_TXP0_C
EDP_TXN1_C
EDP_TXP1_C
TOUCH_SCREEN_INT# LCD <10>
TOUCH_SCREEN_RST_LCD <10>
LCD_BRIGHTNESS
BLON_OUT_C
DMIC_DATA_EDP
DMIC_CLK_EDP
USB20_N6_R
USB20_P6_R
USB20_N8_R
USB20_P8_R
TS_DET# <7>
TS_EN

C1 1U_0402_16V7K
C3 1U_6.3V_MX5R_0201
C2 10P_0402_50V8J

INVERTER POWER

+19VB
F1 1.5A_24V_SMD1812P150TF-24
+DCBAT_LCD
60 mils
C105 place near JEDP1
C105 100U_0805_25V8
C5 @
C6 0.1U_0402_50V7K 100P_0402_50V7K

DMIC_CLK_EDP
DMIC_DATA_EDP
ED4 CEST523NC5VB_SOT-523-3 @ESD@

+LCDVDD_LCD
+LCDVDD
R8 0_0603_5%

EE note: Never change R8 to short pad after MP

DMIC_DATA_EDP
DMIC_CLK_EDP
R6243 0_0201_5%
R6244 0_0201_5%
DMIC_DATA_CODEC <54>
DMIC_CLK_CODEC <54>
to Codec
R6245 0_0201_5%
R6246 0_0201_5%
DMIC_PCH_DATA <10>
DMIC_PCH_CLK <10>
to PCH

R75 100K_0402_5%
R76 100K_0402_5%
BKLT_CTRL
BLON_OUT_D9

LCD_BRIGHTNESS R79 100_0402_5%
LCD_TST_C R80 100_0402_5%
LCD_TST
R11 0_0201_5%
D2 BAT54C_SOT23-3-D
Brightness
EDP_BKLT_CTRL <6>
LCD_TST <58>

R790 0_0201_5%
BLON_OUT_C R78 100_0402_5%
D9 BAT54C_SOT23-3-D
Backlight
PANEL_BKEN_EC <58>
BKLT_IN_EDP <6>

R-short 0831
<10> DBC_PANEL_EN
R13 @ 0_0201_5%
DBC_PANEL_EN_R

<6> EDP_TXN0
<6> EDP_TXP0
C12 0.1U_0201_16V6K
C13 0.1U_0201_16V6K
EDP_TXN0_C
EDP_TXP0_C

<6> EDP_TXN1
<6> EDP_TXP1
C14 0.1U_0201_16V6K
C15 0.1U_0201_16V6K
EDP_TXN1_C
EDP_TXP1_C

<6> EDP_AUXN
<6> EDP_AUXP
C17 0.1U_0201_16V6K
C19 0.1U_0201_16V6K
EDP_AUXN_C
EDP_AUXP_C

<6> EDP_VDD_EN
<58> LCD_VCC_TEST_EN
D4 BAT54C_SOT23-3-D
R17 100K_0402_5%
EC (BIST MODE)

+3VS
PRO@ C16 1U_0201_6.3V6M
U1 PRO@ SY6288C20AAC_SOT23-5
IN OUT GND OC EN
LCDVDD_EN
+LCDVDD
40mil
R15 PRO@ 10K_0402_5%
High Active

Main Func = CAM&MIC, TS

TCH@ -->Touch Screen
@RF@ --> RF
I2CTCH@ --> I2C Touch Screen
USBTCH@ --> USB Touch Screen

+3VS
F4 PRO@ 1A_65V_T0603FF1000TM
+3VS_CAM

+TS_VDD
+5VSO
F5 USBTCH@ 1A_65V_T0603FF1000TM
+3VS
F6 I2CTCH@ 1A_65V_T0603FF1000TM

+MIC_VCC
R83 @ 0_0402_5%
C39 @ 1U_0201_6V3M
C36 0.1U_0402_10V7K
+3VS_CAM
@RF@ C102 10P_0201_25V8

C36: colse to JEDP1.29
C102: colse to JEDP1

Non-TCH -->R81, R82, F5 unpop

D3 RB551V-30_SOD323-2
<59,77> NB_LID#
TOUCH_SCREEN
TS_EN
R14 33_0402_5%
TOUCH_SCREEN_PD# <7,10>
C18 @ 10P_0402_50V8J

Main Func = Hinge up protection

+3VS
+LCDVDD
C955 1U_0201_6.3V6M
ICPRO@
C350 10U_0402_6.3V6M
CABLE2_OCP# <58>

+3VALW
LCDVDD_EN
U4 ICPRO@ G2895ALK21U_TDFN10_2X2
IN1 EN1 VB EN2 IN2 OUT1 GND FLAG1 FLAG2 OUT2 EPAD
CABLE1_OCP# R331 0_0201_5%
to EC
CABLE2_OCP# R_R341 0_0201_5%

<11,78> SIO_SLP_S3#
C956 1U_0201_6.3V6M
R105 100K_0201_5%
C954 1U_0201_6.3V6M

+3VS_CAM_TS R99 0_0402_5%
+TS_VDD
R100 0_0402_5%
C351 10U_0402_6.3V6M
C352 10U_0402_6.3V6M

For BL_PWR_SRC & LCDVDD monitor

+19VB
RF Request
LBIST@RF@
CV75 47P_0201_25V8J
CV76 100P_0201_25V7K
CV77 0.1U_0201_25V6K
place as close as QV18

+DCBAT_LCD_DV13_R
SB00000W600 MMDT3906_SOT363-6 QV18A LBIST@
+DCBAT_LCD
DV16 LBIST@ RB751S-40_SOD523-2 SCS00006300
+DCBAT_LCD_DV13
R621 LBIST@ 10K_0201_5%
R624 200K_0201_5% LBIST@
CV633 LBIST@ 2200P_0201_25V7K

BL_PWR_MONITOR_R
R627 LBIST@ 47K_0201_5%
BL_PWR_MONITOR
QV19 LBIST@ LMBT3904WT1G_SC70-3

+3VS
+LCDVDD_LCD_DV14_R
SB00000W600 MMDT3906_SOT363-6 QV18B LBIST@
+LCDVDD_LCD
DV15 LBIST@ RB751S-40_SOD523-2 SCS00006300
+LCDVDD_LCD_DV14
R622 LBIST@ 10K_0201_5%
R623 200K_0201_5% LBIST@
CV651 LBIST@ 2200P_0201_16V7K

LCDVDD_MONITOR_R
R626 LBIST@ 47K_0201_5%
LCDVDD_MONITOR
QV21 LBIST@ LMBT3904WT1G_SC70-3

+LCDVDD_LCD
R658 LBIST@ 100K_0201_5%
PANEL_MONITOR <58>
R677 LBIST@ 1M_0201_5%

I2C Touch Screen (Reserved)

Close to JEDP1

<10> I2C_0_LCD_SDA
<10> I2C_0_LCD_SCL
R84 I2CTCH@ 0201_5%
R85 I2CTCH@ 0201_5%
USB20_N8_R
USB20_P8_R

R86 I2CTCH@ 10K_0402_5%
R87 I2CTCH@ 10K_0402_5%
R88 I2CTCH@ 10K_0402_5%
TOUCH_SCREEN_RST_LCD

USB20_N8_R
USB20_P8_R
ED2 CEST523NC5VB_SOT-523-3 @ESD@

USB20_P6_R
USB20_N6_R
ED3 CEST523NC5VB_SOT-523-3 @ESD@

USBTCH@
R18 0_0201_5%
L4 DLM0NSN900HY2D_4P @EMI@
USB20_P8 <12>
USB20_N8 <12>
R19 USBTCH@ 0_0201_5%

R-short 0831
R10 0_0201_5%
L3 @EMI@ DLM0NSN900HY2D_4P
USB20_P6 <12>
USB20_N6 <12>
R12 0_0201_5%
R-short 0831

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.
Title: LCD/Cam/MIC/T.Panel
Size: B
Document Number: LA-K036P
Rev: 0.1
Date: Monday, March 06, 2021
Sheet 38 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

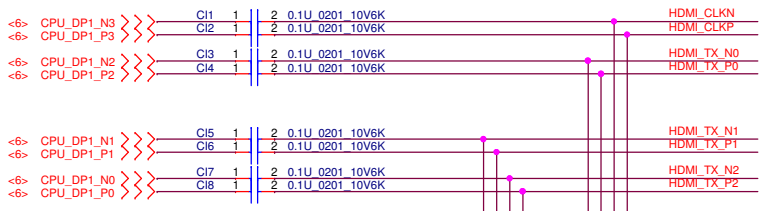
Compal Electronics, Inc.

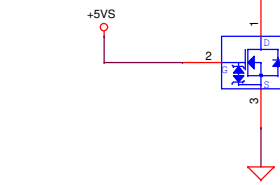
Title: (RSVD)

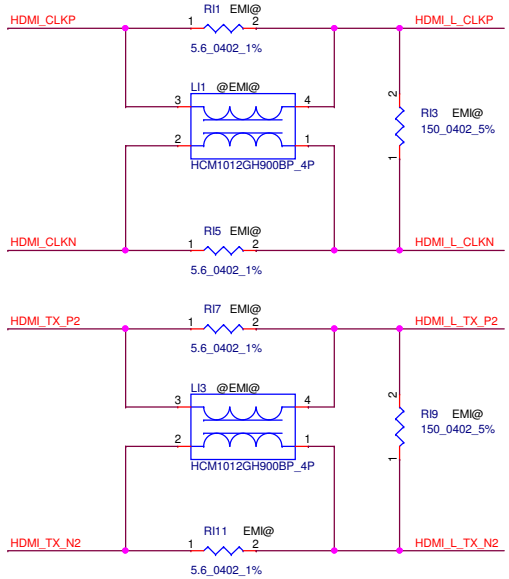
Size | Document Number: LA-K036P | Rev: 0.1

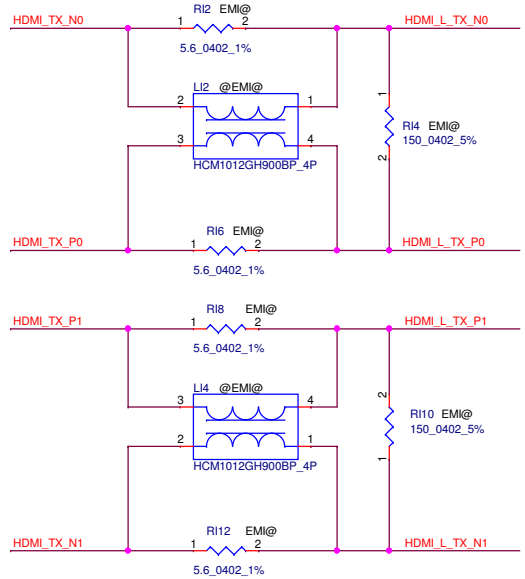
Date: Monday, March 08, 2021 | Sheet 39 of 101

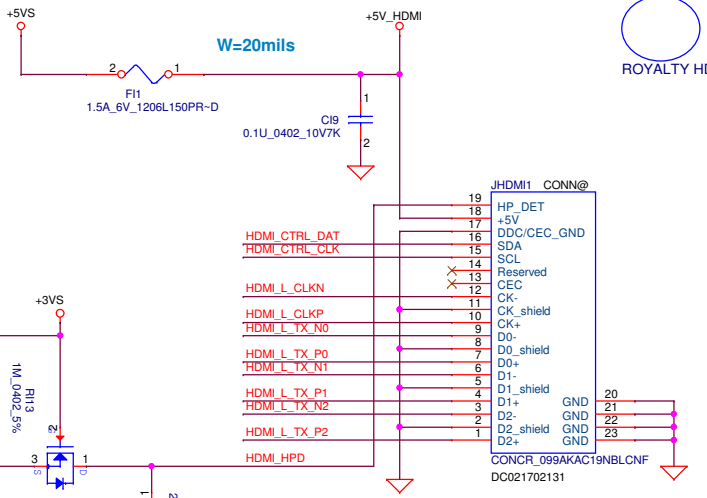
Main Func = HDMI

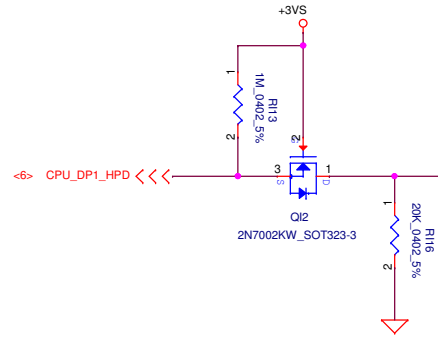












Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: HDMI L.Shifter/Conn

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 40 of 101

Main Function:

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 41 of 101

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port0 (1/2)**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 42 of 101

Main Func =

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.		
Title: TBT TYPE-C Port0 (2/2)		
Size	Document Number: LA-K036P	Rev: 0.1
Date: Monday, March 08, 2021	Sheet 43 of 101	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.		
Title: *TBT TYPE-C Port1 (1/2)*		
Size	Document Number: *LA-K036P*	Rev: 0.1
Date: Monday, March 08, 2021	Sheet 44 of 101	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: *TBT_TYPE-C Port1 (2/2)*

Size | Document Number: *LA-K036P* | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 45 of 101

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT_TYPE-C Port2 (1/2)**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 Sheet 46 of 101

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port2 (2/2)**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 47 of 101

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: TBT TYPE-C Port3 (1/2)

Size: | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 48 of 101

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **Reserve for TBT_TYPE-C Port3 (2/2)**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 49 of 101

MB_USB3.1 TypeC Conn. (Power Path)

POP
TYPEC@

UNPOP
CCG5C@/TBT@

5V@3A

R-short 0831

W=120 mils

20 mils

need to ask EC , low active for TPS25814

CHG_HI PD set for 3A
(replay by TI FAE)

low Active

CDP mode

Can be floating , if no need

R-short 0831

for EC inform Type-C port has device plugging

PTPS25814AARSMR_QFN32_4X4

POP
EMI@/TYPEC@/TYPEC@EMI@/TYPEC@ESD@
UNPOP
CCG5C@/@EMI@/CCG5C@EMI@/@ESD@/CCG5C@RF@

Cross Moat Cap
DSC Only

TYPE-C

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title: TYPE-C Power Path

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 50 of 101

Main Func = LAN

LAN CHIP 10/100/1000

Layout:
For RTL8111H-CG
* Place CL3,CL4,CL5,CL6 close to each VDD10 pin 8, 30, 3, 22
For RTL8106E
* Place CL3,CL4 close to each VDD10 pin 8, 30

CL3: close to Pin8
CL4: close to Pin30
CL5: close to Pin3
CL6: close to Pin22

CL2,RL1: Only for RTL8111 LDO mode.

1000@ R-short 0831

40 mils

Layout:
For RTL8111H-CG
* Place CL10 and CL11 and CL12 close to each VDD33 pin 11, 23 , 32
For RTL8106E
* Place CL11 and CL12 close to each VDD33 pin 23, 32

40 mils R-short 0831

CL12: close to Pin23
CL10: close to Pin11
CL11: close to Pin32

Layout:
CL15: close to Pin32
CL17: close to Pin11

+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

JP5
Always Open

W=40mils W=40mils

High Active

	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M

UL1 1000@ RTL8111H-CG_QFN32_4X4 SA000080P00

UL1 100@ RTL8106E-CG_QFN32_4X4 SA000065Y00

25MHZ_10PF_XRCGB25M000F2P34R0

CL8, CL9 close to UL1 Pin 17, 18
CL13, CL14 close to UL1 Pin 13, 14

"PCIE_WAKE#" PU 1k on CPU side

R-short 0831

Main Func = LAN LAN TransFormer 10/100M x2

TL1 TOP, TL2 BOT

Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF

Main:
SP0500006H00, SX'FORM_ NS0014 LF LAN
2nd:
W00, SX'FORM_ HD-245 10/100 PC CARD LAN

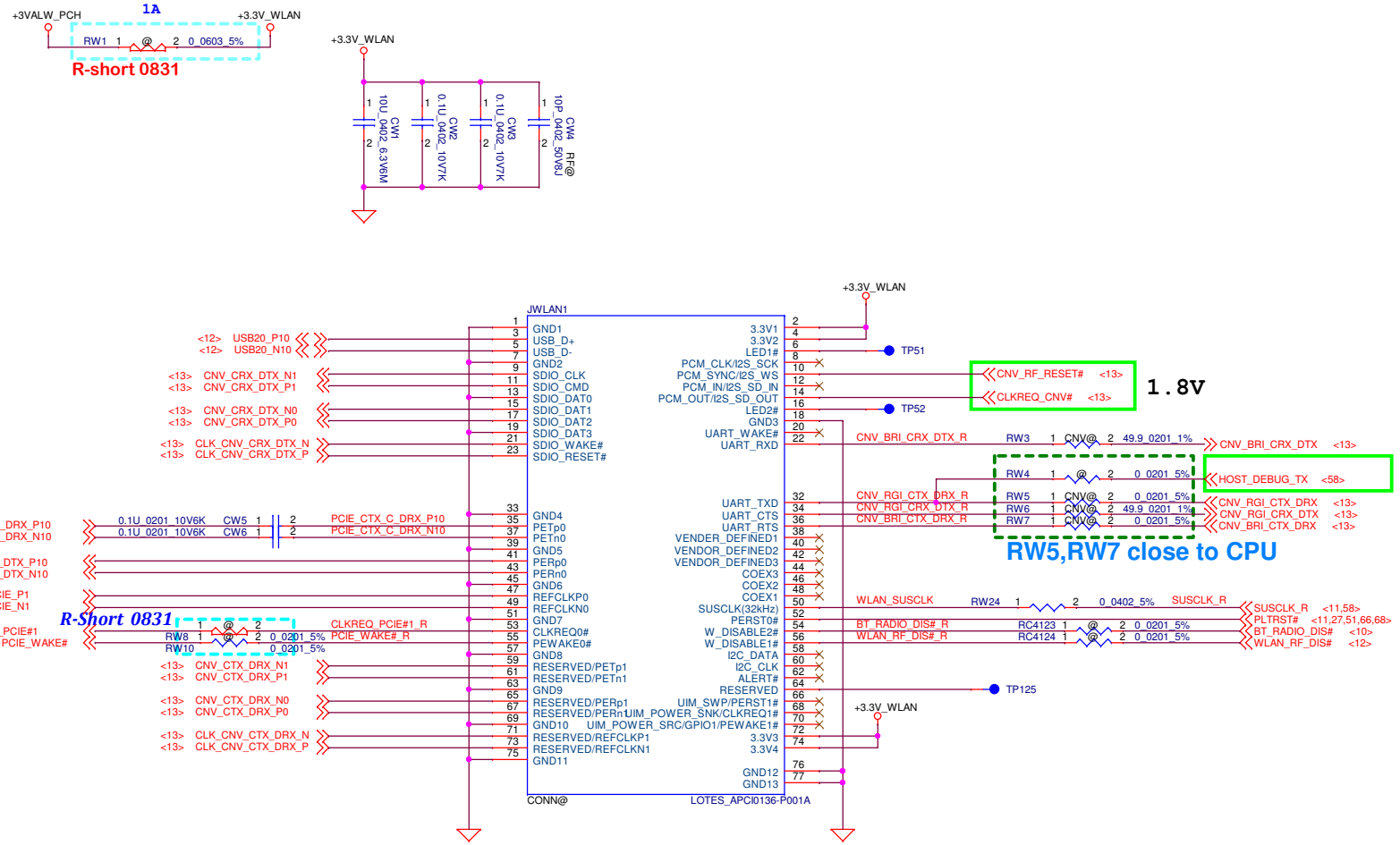
Both 100 and 1000 use 10P

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.
Title: LAN RTL8111/RTL8106
Size: Custom
Document Number: LA-K036P
Rev: 0.1
Date: Monday, March 08, 2021
Sheet 51 of 101

Main Func = WLAN

E Key CONN



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	NGFF WLAN CONN		
Size	Document Number		Rev
	LA-K036P		0.1
Date:	Monday, March 08, 2021	Sheet	52 of 101

Main Function: WIGIG / WIDI

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

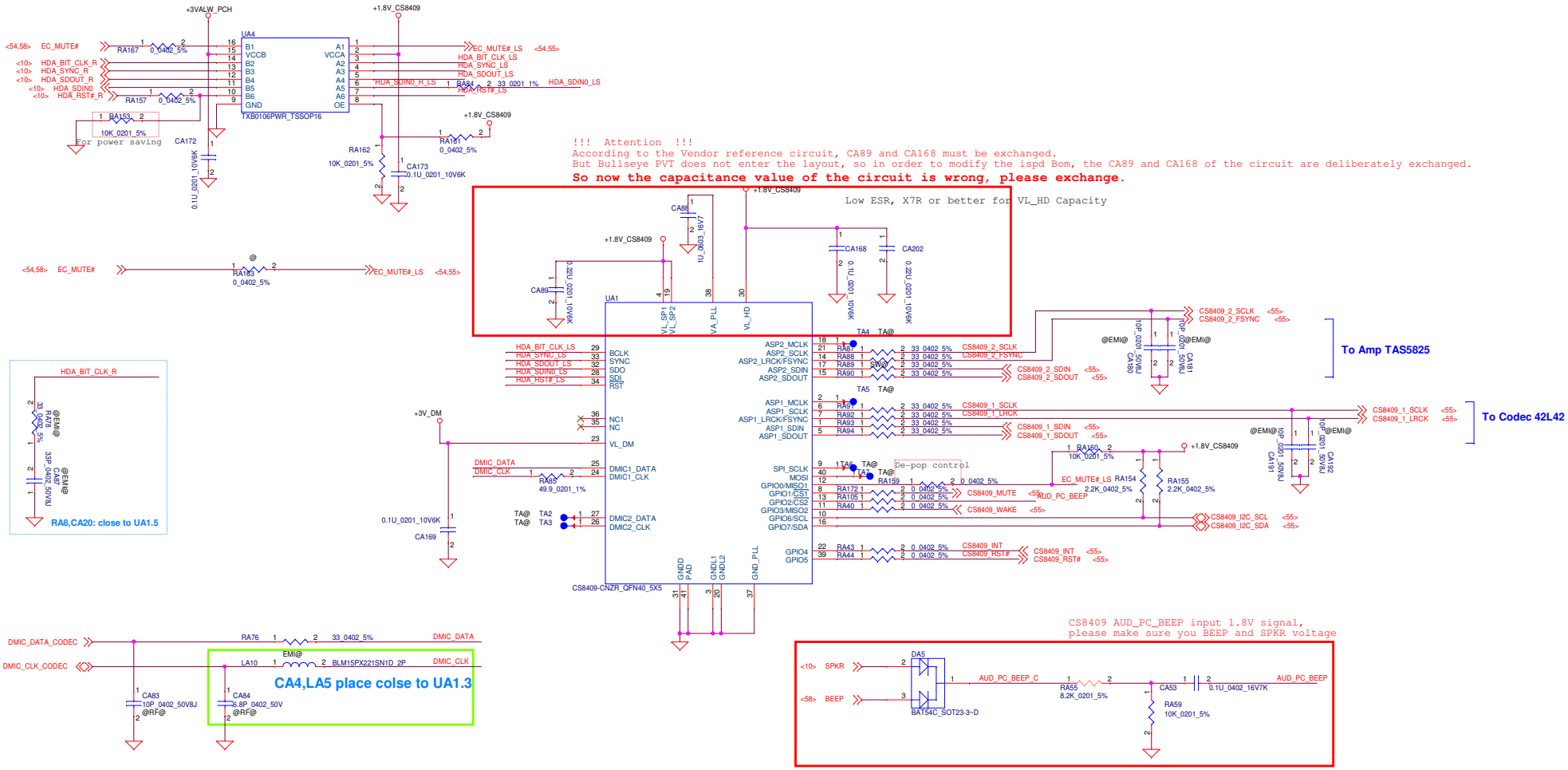
Compal Electronics, Inc.

Title: WIGIG / WIDI(RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 53 of 101

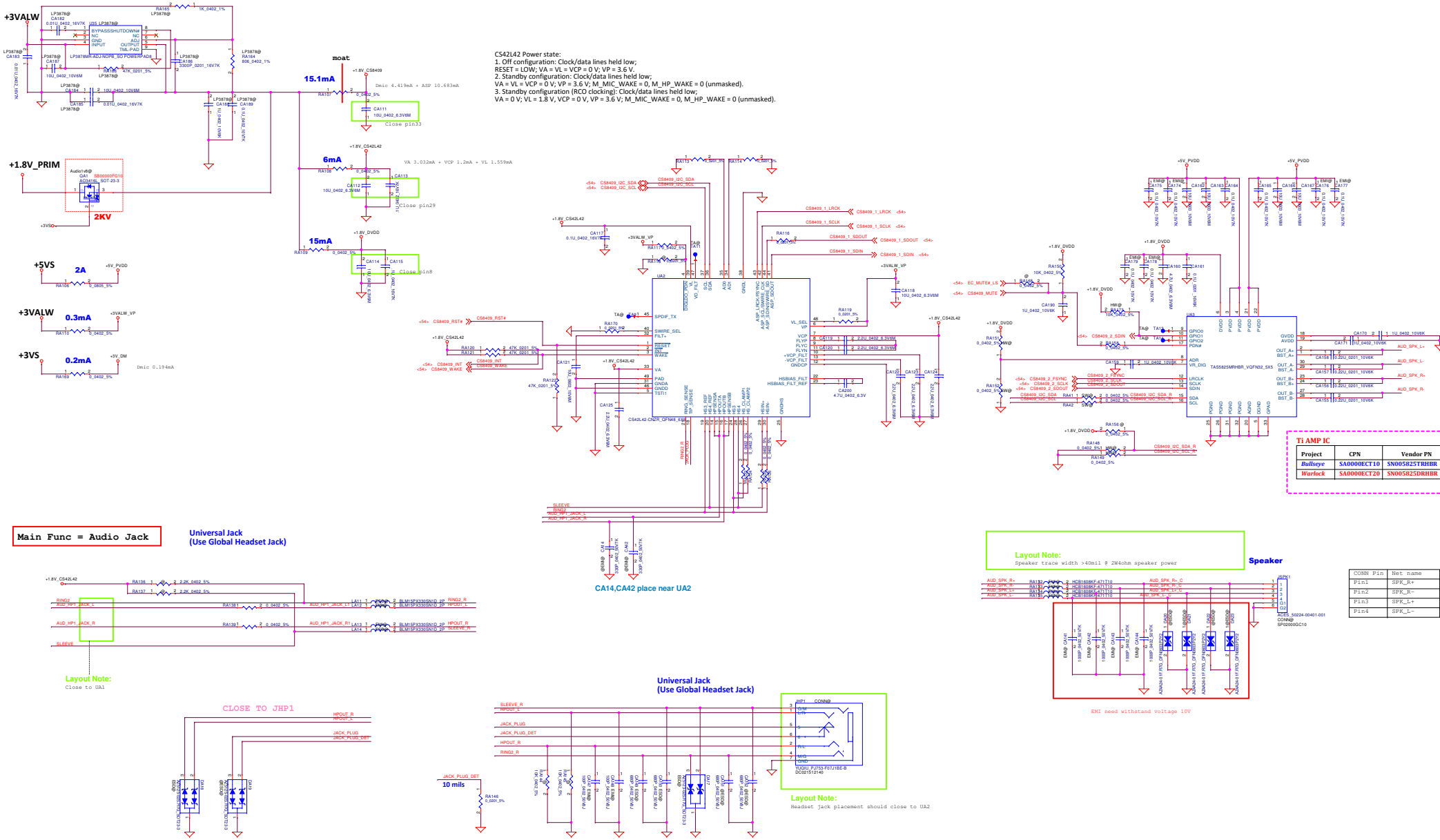
Main Function:



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	(RSVD)		
Size	Document Number	LA-K036P	Rev 0.1
Date:	Monday, March 08, 2021	Sheet 54 of 101	

Main Function:



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

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Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 55 of 101

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **Audio Codec ALC3204**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 Sheet 56 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: (RSVD)		
Size	Document Number: LA-K036P	Rev: 0.1
Date: Monday, March 08, 2021	Sheet 57 of 101	

Main Func = EC

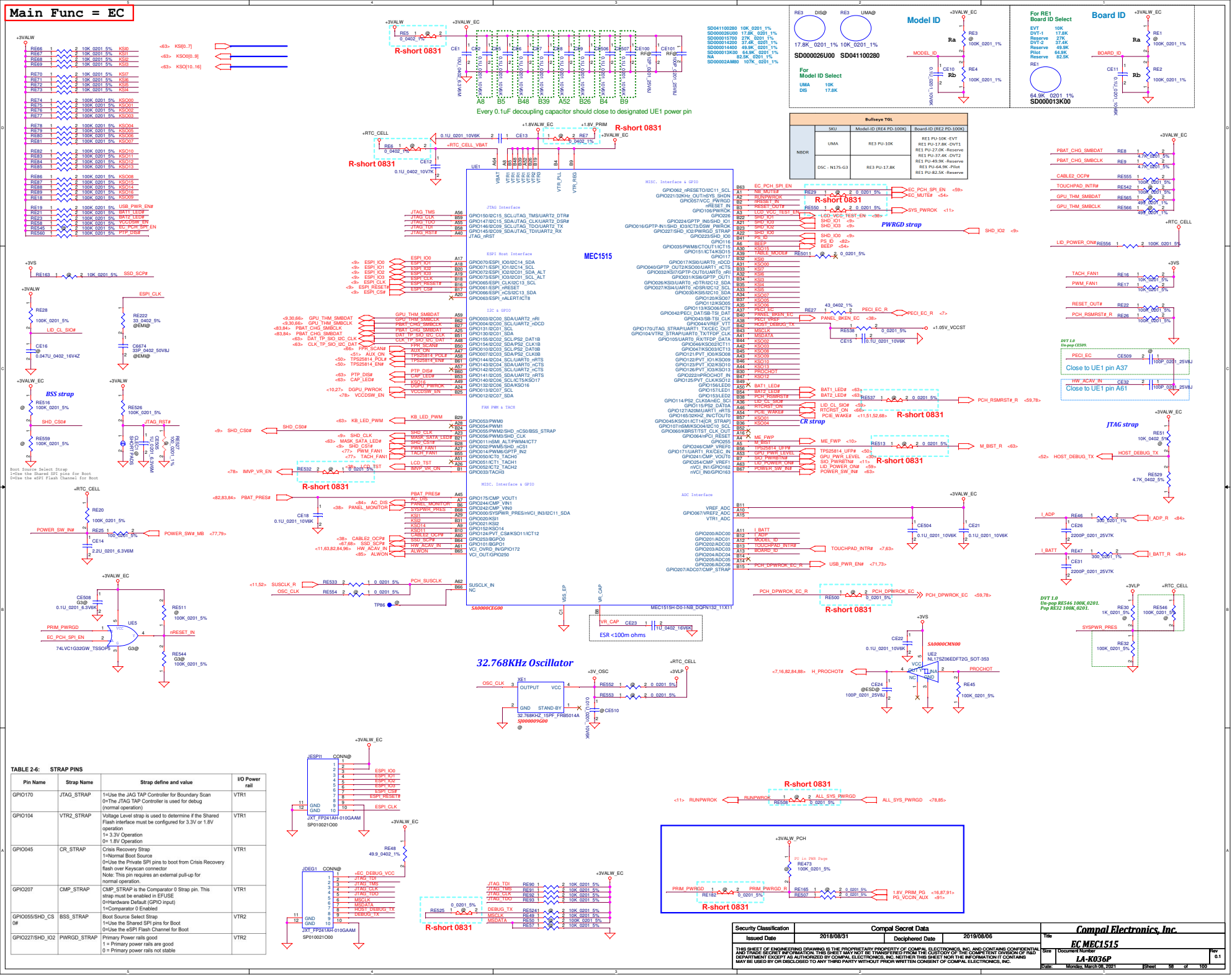


TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPIO104	VTR2_STRAP	Voltage Level strap is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VTR1
GPIO045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keyscan connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPIO207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE 0=Hardware Default (GPIO input) 1=Comparator 0 Enabled	VTR1
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VTR2
GPIO227/SHD_IO2	PWRGD_STRAP	Primary Power rails good 1 = Primary power rails are good 0 = Primary power rails not stable	VTR2

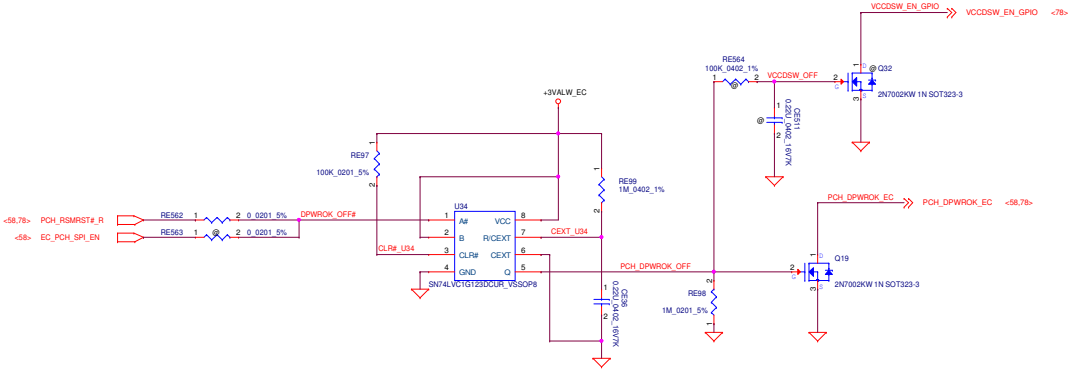
Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Title	Compal Electronics, Inc.
	EC MEC1515
Size	Document Number: LA-K036P
Rev	0.1
Date:	Monday, March 08, 2021
Sheet	58 of 100

Main Function: WDT circuit

FUNCTION TABLE

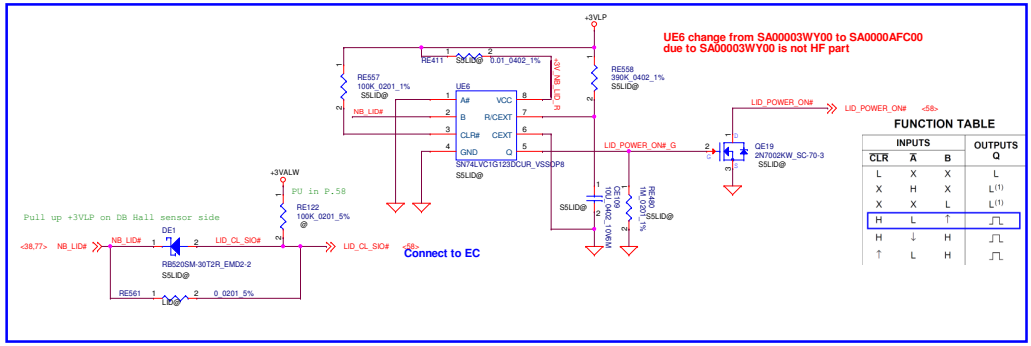
INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍



t_w OUT(2)		Q	C_{ext} = 28 pF, R_{ext} = 2 kΩ	225	600	190	220	170	200	150	180	ns
			C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	100	110	100	110	100	110	100	110	µs
			C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	1	1.1	1	1.1	1	1.1	1	1.1	ms

Main Function: S5 LID

S5 LID OPEN POWER ON



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

Compal Electronics, Inc.			
Title	(RSVD)		
Size	Document Number		Rev
	LA-K036P		0.1
Date:	Monday, March 08, 2021	Sheet 59 of 101	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

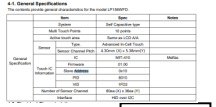
Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 60 of 101

Main Function:SMB/I2C Block Diagrams



I2C Address:0x10

JeDP CONN
For Touch Screen

USB20_P8_R
USB20_N8_R
0 ohm
I2C_0_LCD_SCL
I2C_0_LCD_SDA
4.7k ohm
+3VS
@ 2.2k ohm
I2C_0_SCL
I2C_0_SDA
DV18
DW18

I2C Address: 0x2C
0b0101 100 + R/W

JTP CONN
Touch PAD
I2C

+TP_VDD (+3VS)
I2C_1_SCL_R
I2C_1_SDA_R
2.2k ohm
I2C_1_SCL
I2C_1_SDA
DJ23
DT18

Power Monitor
CONN

I2C_2_SCL
I2C_2_SDA

JTP CONN
Touch PAD
PS2

DAT_TP_SIO_R
CLK_TP_SIO_R
DAT_TP_SIO_I2C_CLK
CLK_TP_SIO_I2C_DAT

- I²C

The I²C interface complies with I²C Bus Specification, Version 2.1.
The device address is 0x2C.
I²C clock rate: 400KHz

TGL-U

I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA

KBC
MEC 1515

GPIO155
GPIO154
GPIO004
GPIO003
GPIO131
GPIO130

ISH_I2C_0_SCL
ISH_I2C_0_SDA
DB45 ISH_I2C_0_SCL
DB44 ISH_I2C_0_SDA
@ 1k ohm
Reserved

ISH_I2C_1_SCL
ISH_I2C_1_SDA
CY39 ISH_I2C_1_SCL
DB47 ISH_I2C_1_SDA
1k ohm
FreeFall Sensor
LNG2DMTR LGA

FreeFall Sensor reserved
SMBus Address: 0101001b

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

SMBCLK
SMBDATA
DK21 MEM_SMBCLK
DM19 MEM_SMBDATA
+3VALW_PCH
2N7002KDW
QC6
PCH_SMBCLK
PCH_SMBDAT
2.2k ohm
+3VS
DIMMA
DDR4
DIMMB
DDR4
XDP CONN

SMBus Address: 000
SMBus Address: 010

SML0CLK
SML0DATA
DK19 SML0_SMBCLK
DM17 SML0_SMBDATA
499 ohm
GPU_THM_SMBCLK
GPU_THM_SMBDAT
2N7002KDW
Q11
THM_SML1_CLK
THM_SML1_DATA
Thermal Sensor
NCT7718W

SML1CLK
SML1DATA
DK17 SML1_SMBCLK
DJ17 SML1_SMBDATA
Reserved for Type-C , TBT
PJT138KA
QV2
I2CS_SCL
I2CS_SDA
GPU
N17S-G3
+1.8VS_DGPU_AON

PBAT_CHG_SMBCLK
PBAT_CHG_SMBDAT
+3VALW_EC
100 ohm
CLK_SMB
DAT_SMB
BATT CONN

7-bit Address:0x0B
0001011x x is R/W

Charger
ISL95522
PUB01

SMBus Address:0b00010011(resd)
0b00010010 (write)

6.3 Address Setting

NCT7718W I²C/ SMBus™ address is 1001100xb (x is R/W bit).

SMBus Address: 1001100xb (x is R/W bit)

I2CS SMBUS: 0x9E(write) , 0x9F(read)
Debug Address: 0x96

13.3.2.1 I2CS Slave Address

The default I2CS address is 0x9E. This address can not be used by another device on the same bus. The GPU has an alternative I2CS address (0x9C) which is used when a second GPU is placed on the board. This alternative address is enable by using the SMB_ALT_ADDR strap. See Chapter "GPU Straps" for information regarding this strap. By using this alternative I2CS address, two GPUs on the board can be placed on the same I2CS bus.

Specification	Description
Base Address	• BAR0: 16 MB • BAR1: 256 MB • BAR2: 32 MB • I/O BAR: 4 KB
PCI Class Code	0x03 - 3D Controller
PCI Sub-Class Code	0x02 - 3D Controller
ECC Support	Not Supported
SMBus (8-Bit Address)	0x9E (write), 0x9F (read) or 0x9C (write), 0x9D (read)

System Management Bus (SMBus) Specification Version 3.0

Appendix C. SMBus Device Address Assignments

Table 17 lists the pre-assigned and reserved SMBus device assignments.

Table 17. Reserved and pre-assigned SMBus addresses

Slave Address Bits [7:1]	R/W# Bit [0]	Description	Specification
0000 000	0	General Call Address	I²C-Bus Specification And User Manual [9821]
0000 000	1	START byte	I²C-Bus Specification And User Manual [9821]
0000 001	X	CBUS address	I²C-Bus Specification And User Manual [9821]
0000 010	X	Address reserved for different bus format	I²C-Bus Specification And User Manual [9821]
0000 011	X	Reserved for future use	I²C-Bus Specification And User Manual [9821]
0000 1XX	X	Hs Mode Master Code	I²C-Bus Specification And User Manual [9821]
0001 000	X	SMBus Host	System Management Bus Specification V 1.1, December 1998
0001 001	X	Smart Battery Charger	Smart Battery Charger Specification V 1.1, December 1998
0001 010	X	Smart Battery Selector Smart Battery System Manager	Smart Battery Selector Specification V 1.1, December 1998 Smart Battery System Manager Specification V 1.0B, August 1999
0001 011	X	Smart Battery	Smart Battery Data Specification V 1.1, December 1998
0001 100	X	SMBus Alert Response Address	System Management Bus Specification V 1.1, December 1998
0100 000	1	PMBus™ ZONE READ	PMBus Power System Management Protocol Specification, Part I, Revision 1.3
0101 100	X	Reserved for previous versions of the	

The ISL95522 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL95522 uses the SMBus Read Word and Write Word protocols shown in Figure 33 on page 32 to communicate with the host system and a smart battery. The ISL95522 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_:

Read address = 0b00010011(0X13H)
Write address = 0b00010010(0X12H)

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: SMB/I2C Block Diagrams

Size: Document Number: LA-K036P Rev: 0.1

Date: Monday, March 08, 2021 Sheet 81 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

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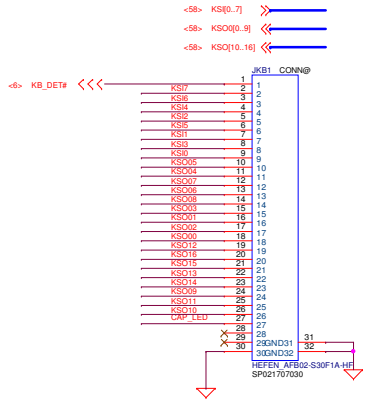
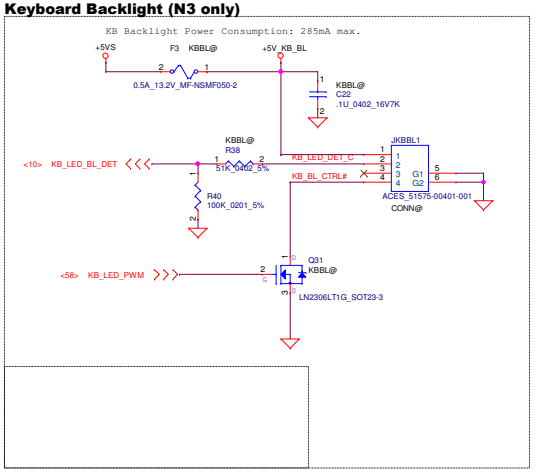
Main Func = KB

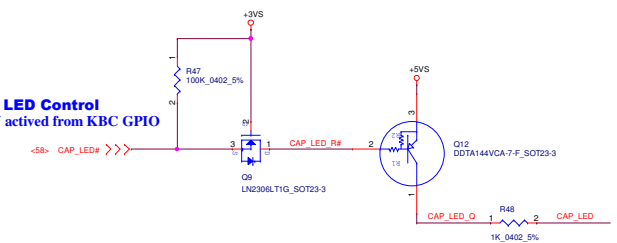


Keyboard Backlight (N3 only)

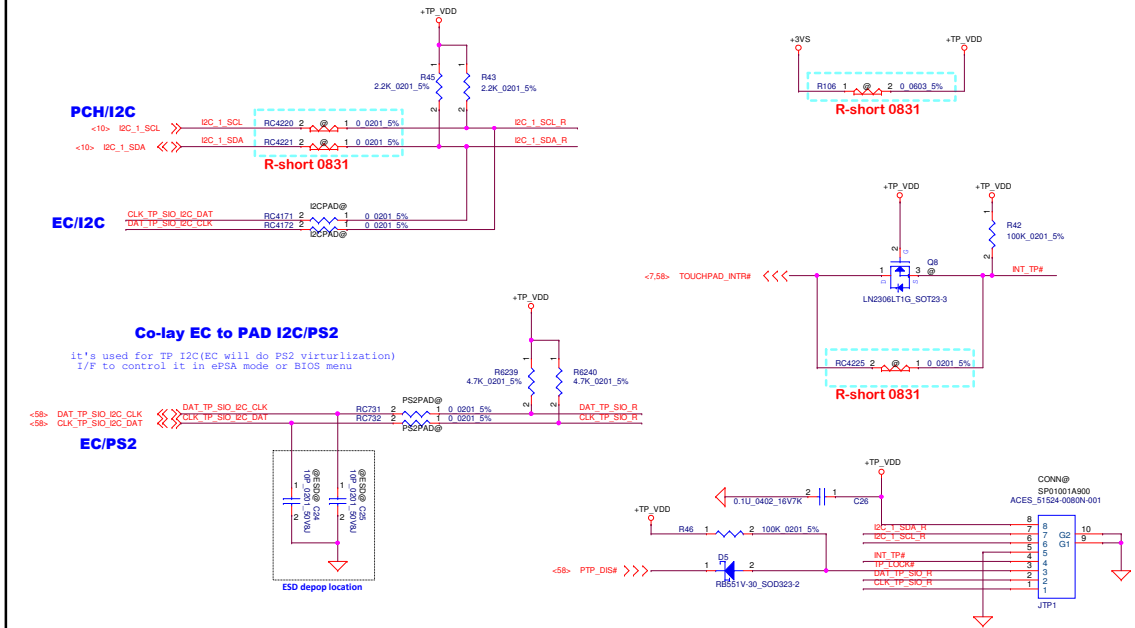


CAP LED Control

LOW actived from KBC GPIO



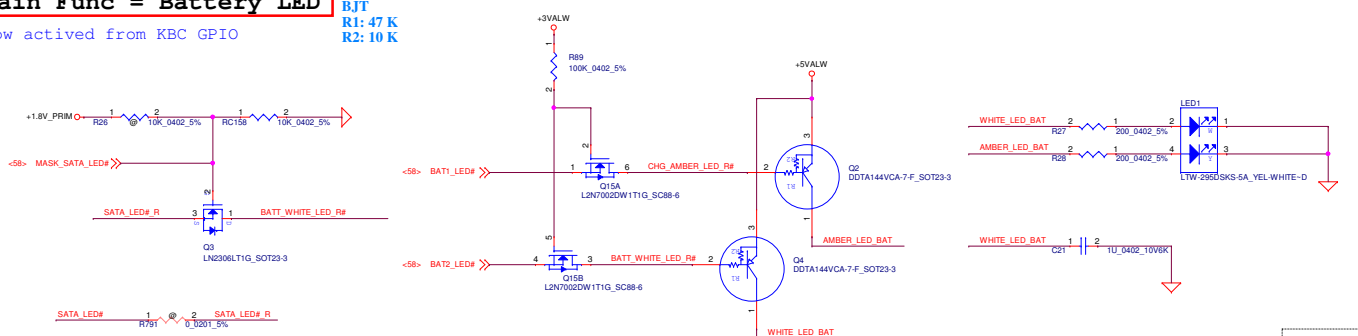
Main Func = TPAD

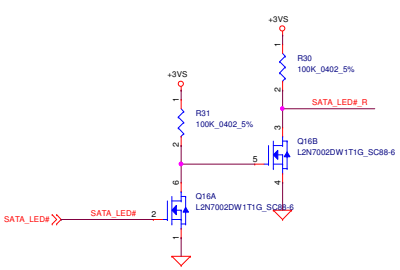


Main Func = Battery LED

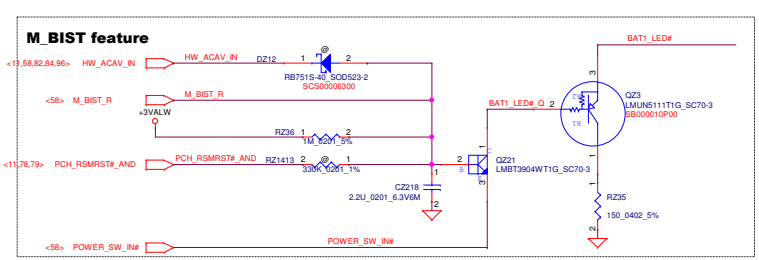
Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K





M_BIST feature



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	Keyboard/Touch Pad/Thermal/FAN		
Size	Document Number	LA-K036P	Rev 0.1
Date: Monday, March 08, 2021	Sheet 63 of 101		

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 64 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

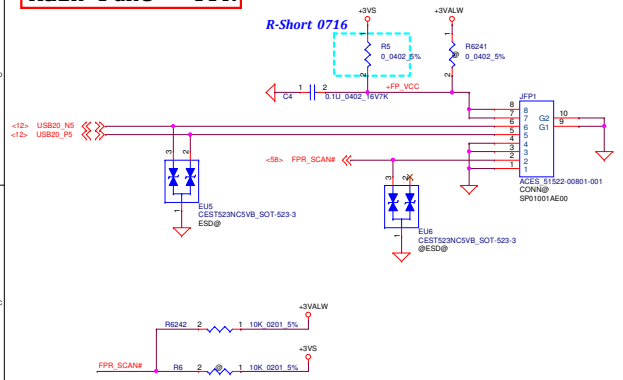
Compal Electronics, Inc.

Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

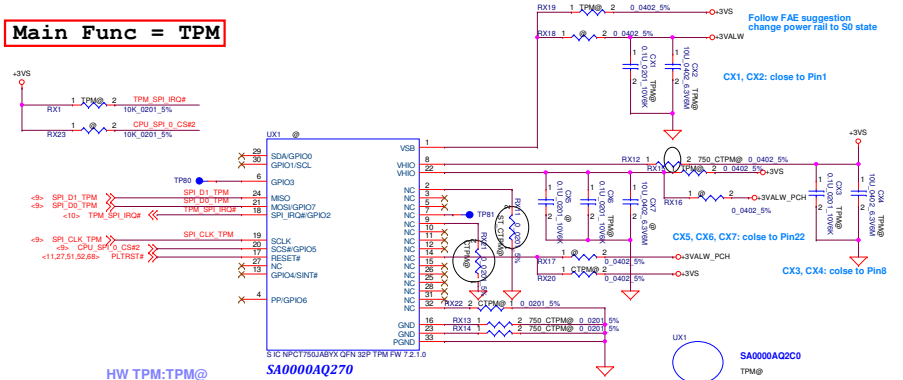
Date: Monday, March 08, 2021 | Sheet 65 of 101

Main Func = FPR

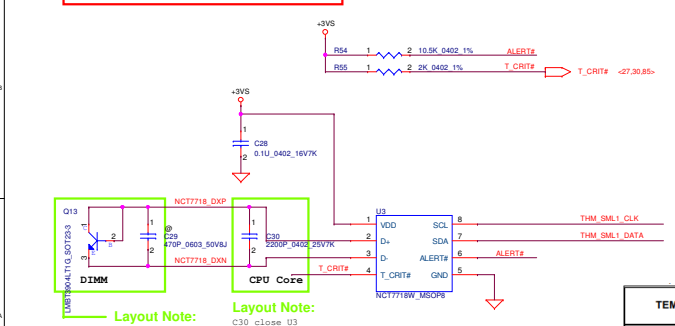


Main Func = OTP

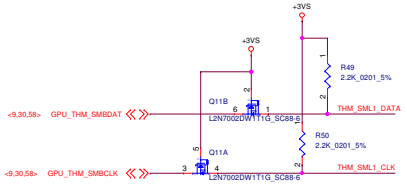
Main Func = TPM



Main Func = Thermal

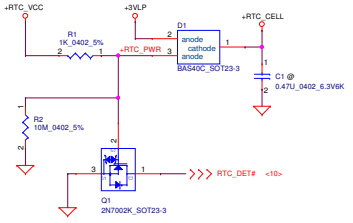


DXN and DXP routing width and spacing is 10 mil / 10 mil.

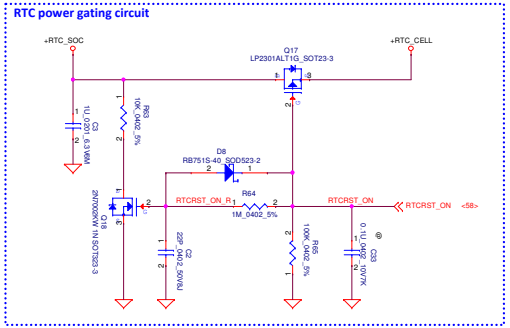


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = RTC



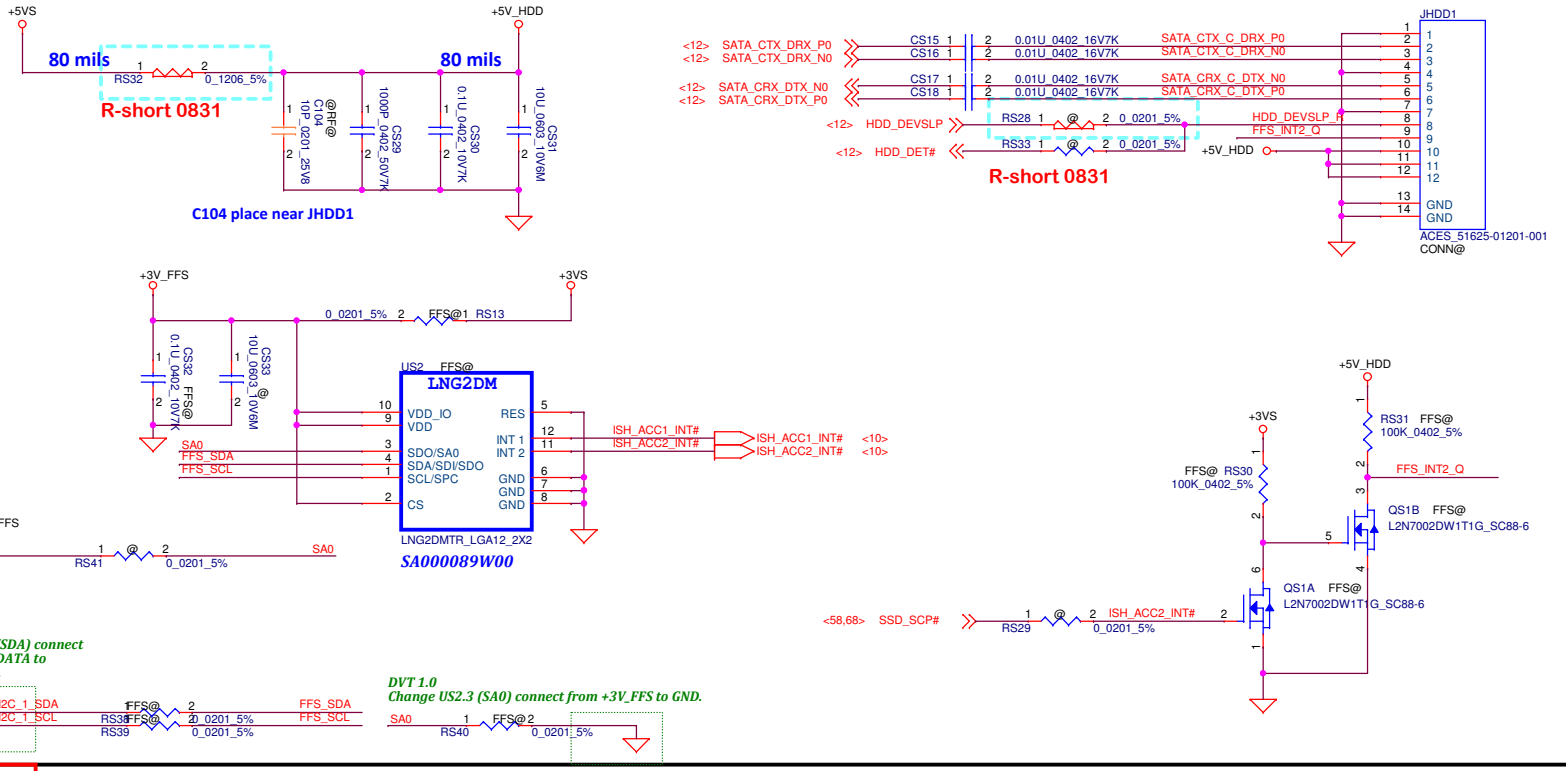
RTC power gating circuit



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.	
Title	TPM/RTC/Screw hole
Size	Document Number: LA-K036P
Rev	0.1
Date: Monday, March 08, 2021	Sheet 66 of 101

Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

Main Func = ODD

Cancel ODD

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: HDD/FFS/ODD

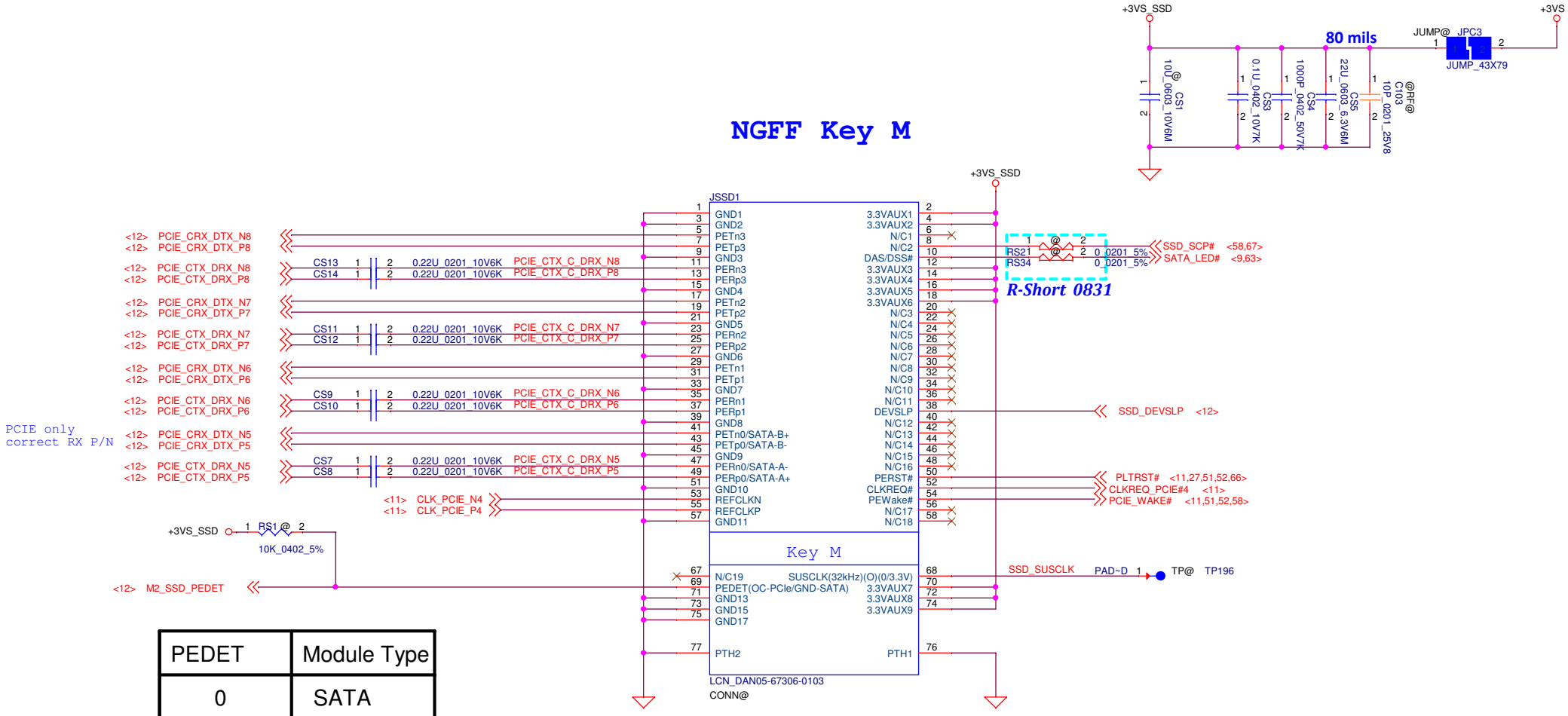
Size: Custom | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 67 of 101

Main Func = SSD

M Key CONN

NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: NVME SSD

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 68 of 101

Main Func = eMMC

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **eMMC (RSVD)**

Size	Document Number	Rev
	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 69 of 101

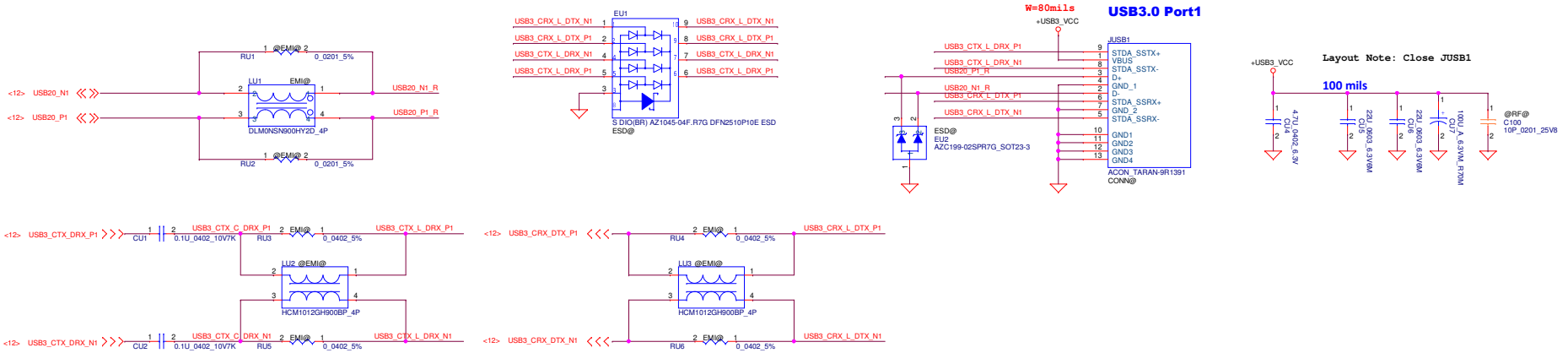
Main Function:

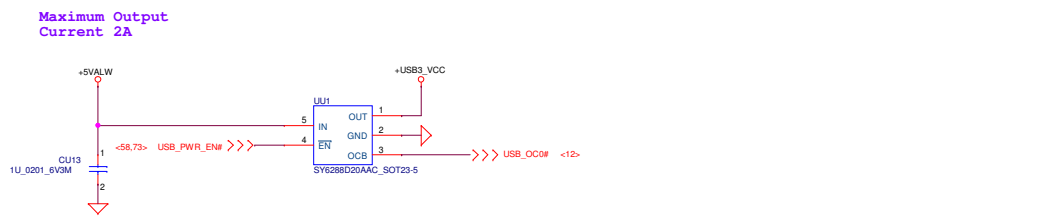
Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: (RSVD)		
Size	Document Number: LA-K036P	Rev: 0.1
Date: Monday, March 08, 2021	Sheet 70 of 101	

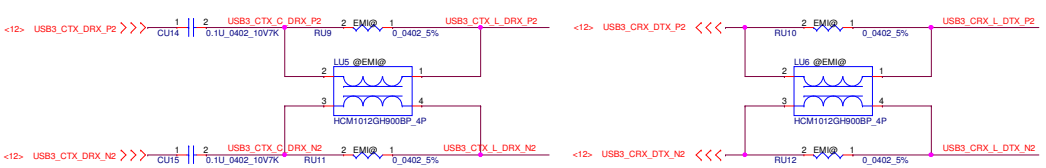
Main Func = USB3.0 Port1





Maximum Output
Current 2A

Main Func = USB3.0 Port2



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Title	USB3.0		
Size	Document Number		Rev
	LA-K036P		0.1
Date:	Monday, March 08, 2021	Sheet	71 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

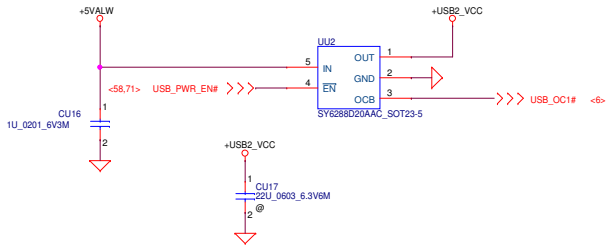
Compal Electronics, Inc.

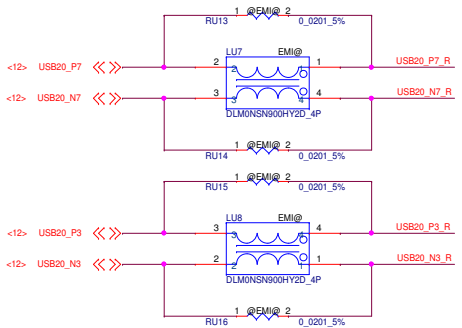
Title: *(RSVD)*

Size | Document Number: *LA-K036P* | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 72 of 101

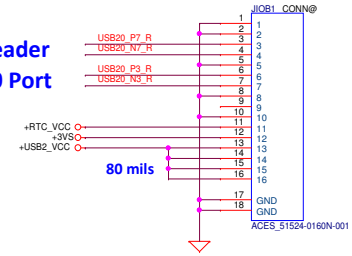
Main Func = USB2.0 Port3 + Card Reader on IO/B





USB2.0/Card Reader connector

CardReader
USB2.0 Port



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: Finger Print & I/O CONN			
Size	Document Number: LA-K036P		Rev: 0.1
Date: Monday, March 08, 2021		Sheet 73 of 101	

Main Function:

Reserve

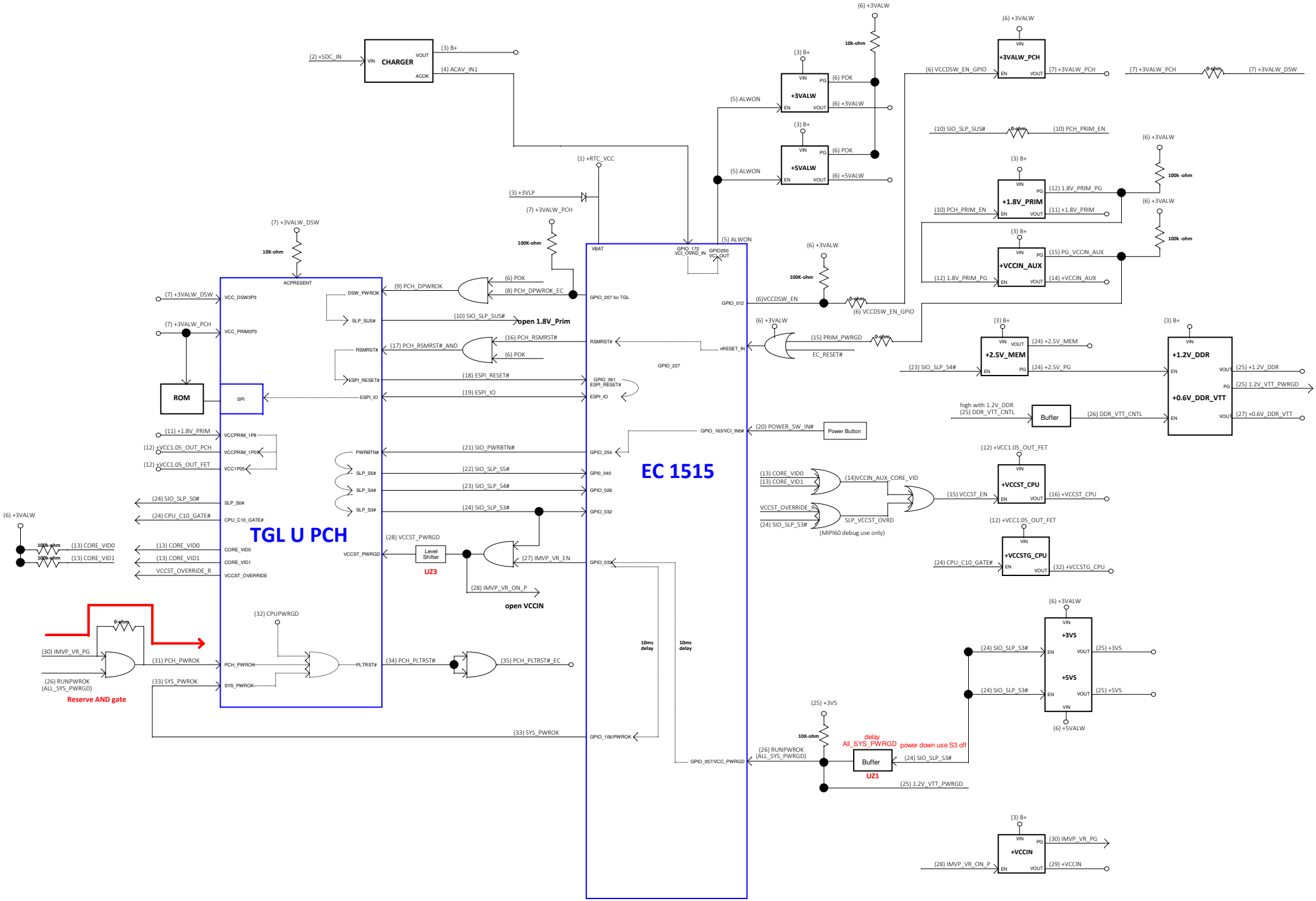
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: DOCK(RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 74 of 101



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date 2019/04/01	Title (RSVD)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Document Number LA-K036P Rev 0.1
			Date: Monday, March 08, 2021 Sheet 25 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

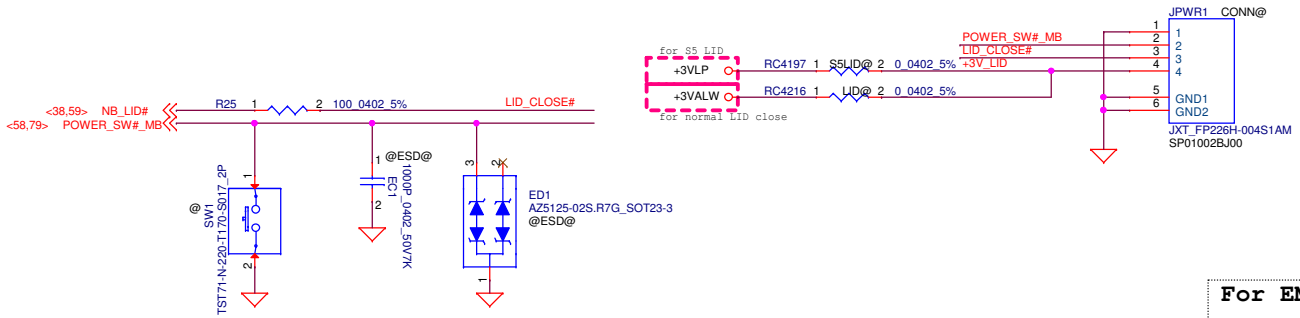
Title: (RSVD)

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 76 of 101

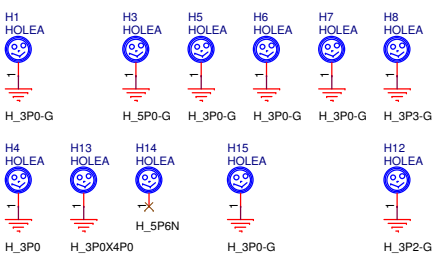
Main Func = Power BTN

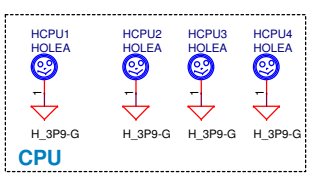
Low actived from KBC GPIO

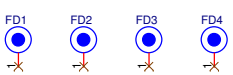


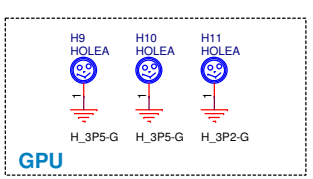
For EMI Reserved

Screw hole/FD

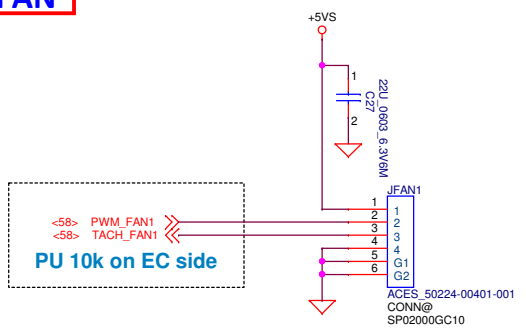




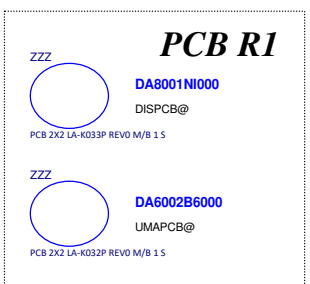




FAN



PCB PN



PCB R3

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: PWRBTN/PCB PN//SCREW/FAN

Size | Document Number: LA-K036P | Rev: 0.1

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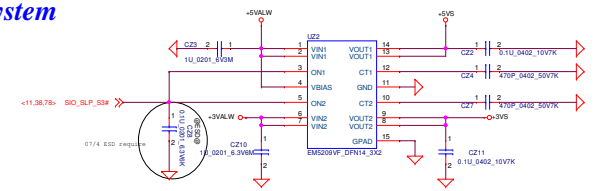
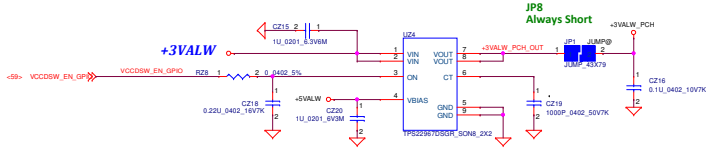
Main Func = DC/DC

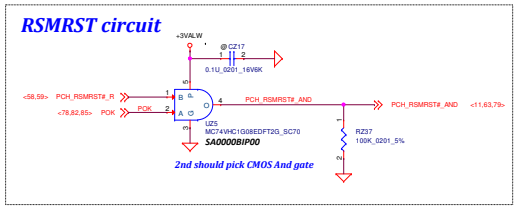
+5VS / +3VS for System



+3VALW TO +3VALW_PCH

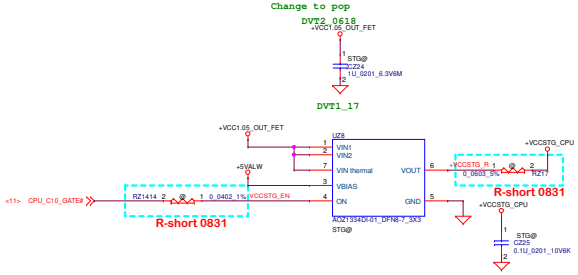


RSMRST circuit



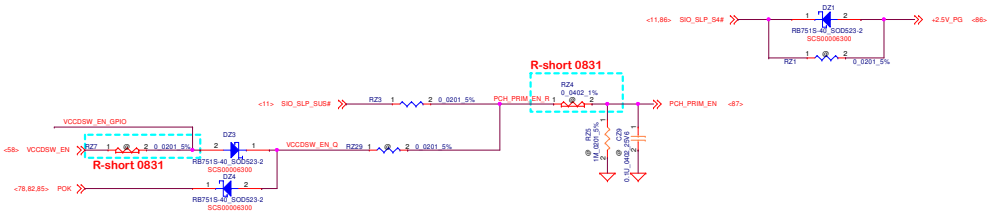
Change to pop

VCCSTG

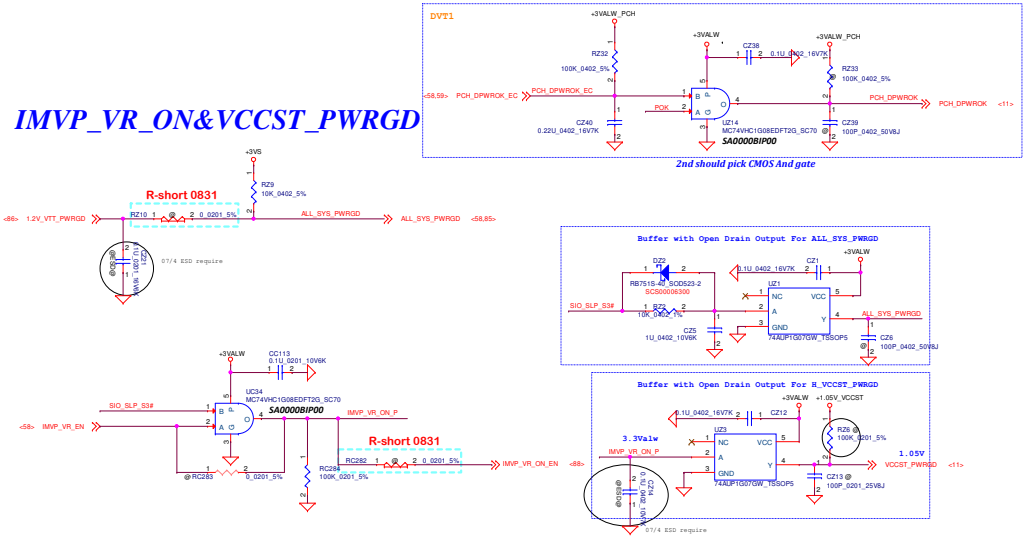


+1.2V_VDDQ TO +1.2V_VCCPLL_OC

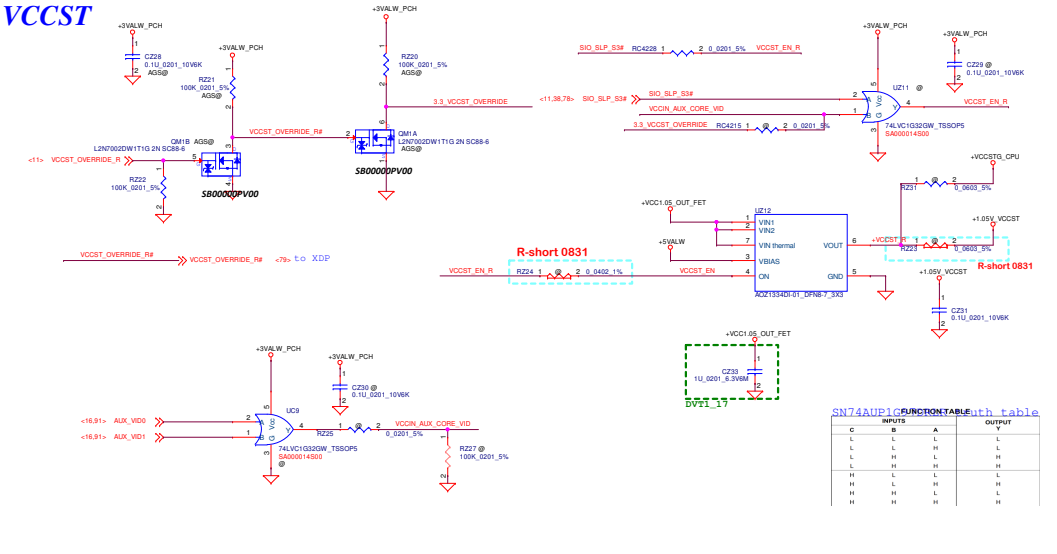
Sequence Logic



IMVP_VR_ON&VCCST_PWRGD



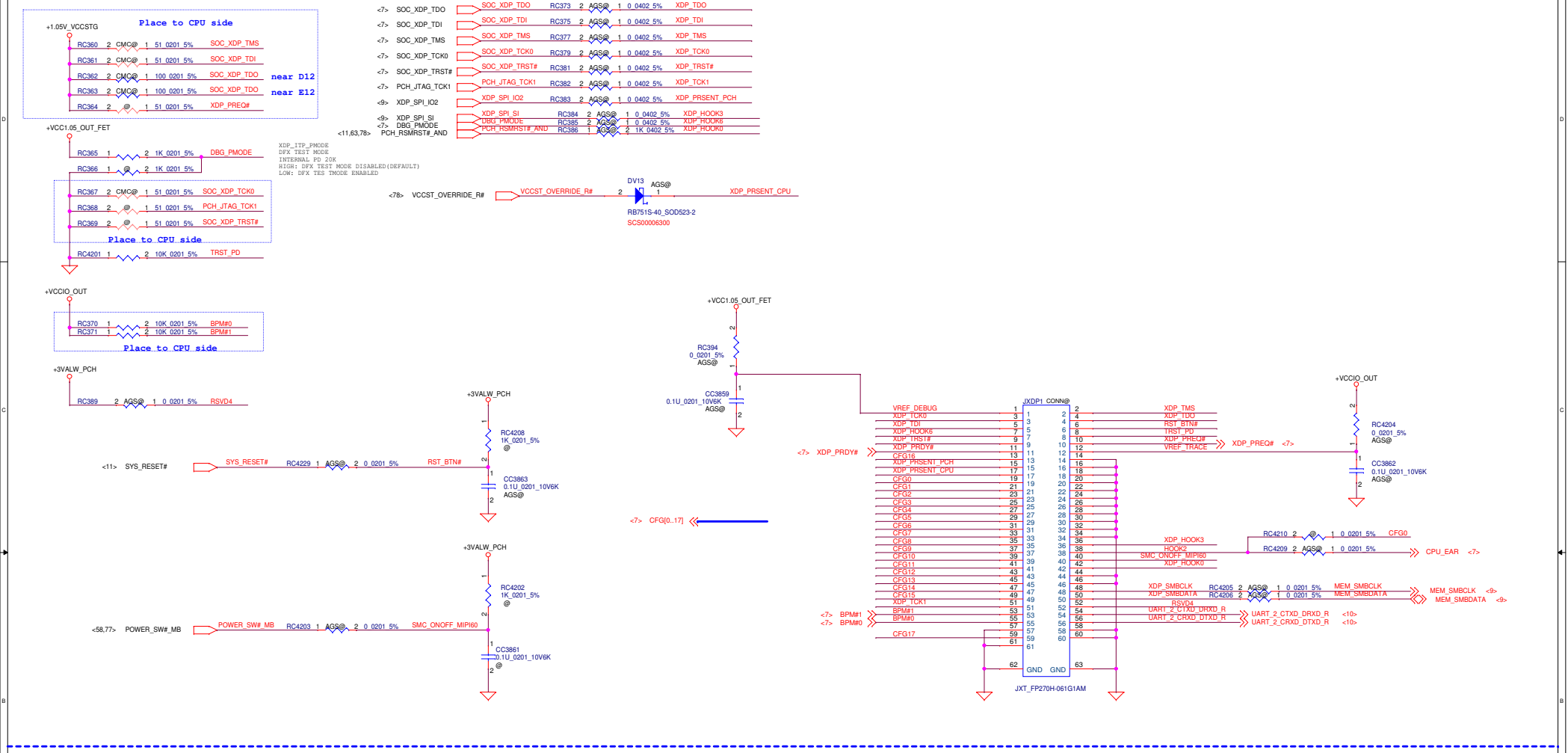
VCCST



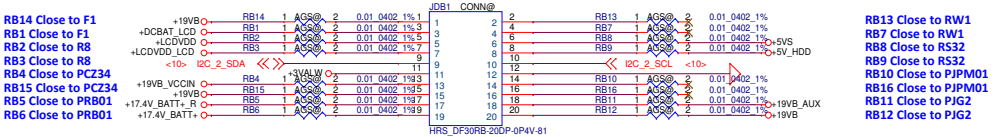
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2018/04/01

Compal Electronics, Inc.			
Title: DC/DC			
Size	Document Number: LA-K036P		Rev: 0.1
Date: Monday, March 08, 2021		Sheet 78 of 101	

Main Func = Debug connector



Power Monitor



2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: Debug connector

Size | Document Number: LA-K036P | Rev: 0.1

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Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **XDP**

Size	Document Number	Rev
B	LA-K036P	0.1

Date: Monday, March 08, 2021 | Sheet 80 of 101

Reserve

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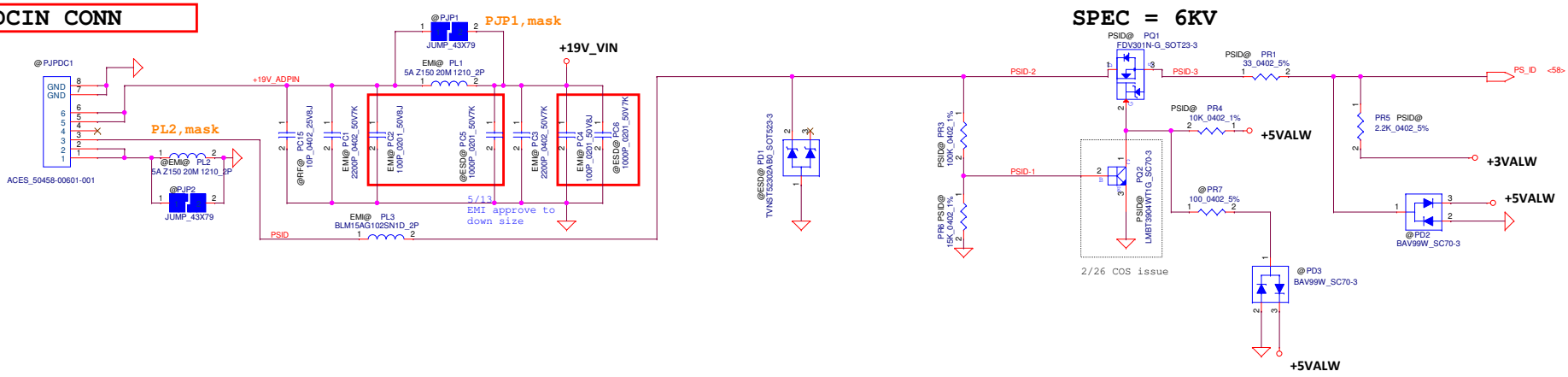
Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.			
Title	Reserve for PWR		
Size	Document Number	LA-K036P	Rev 0.1
Date: Monday, March 08, 2021	Sheet 81 of 101		

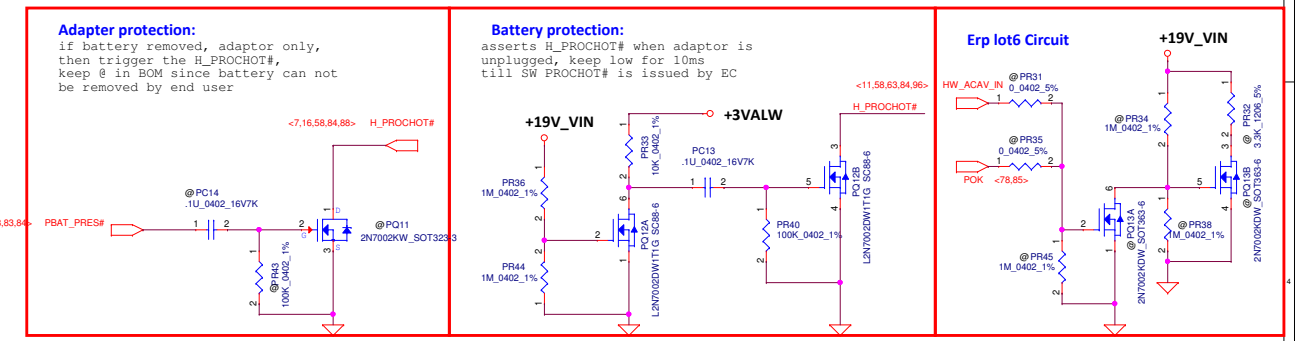
Main Func = DCIN CONN



Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: ***PWR_DCIN CONN***

Size | Document Number: ***LA-K036P*** | Rev: 0.1

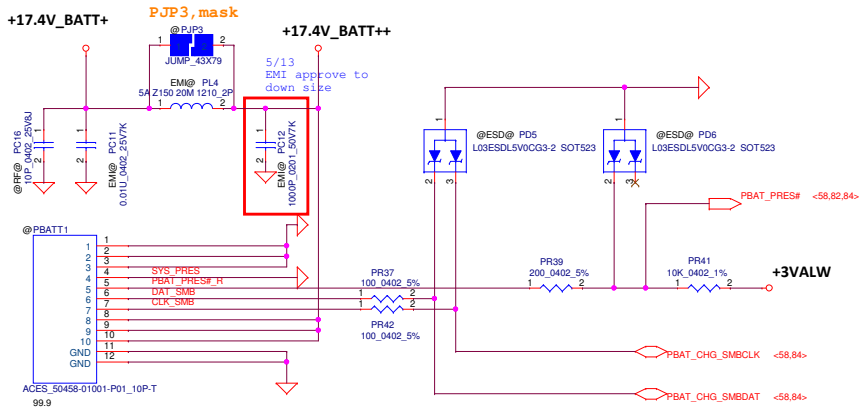
Date: Monday, March 08, 2021 | Sheet 82 of 101

Main Func = BATT CONN

Battery Bot Side

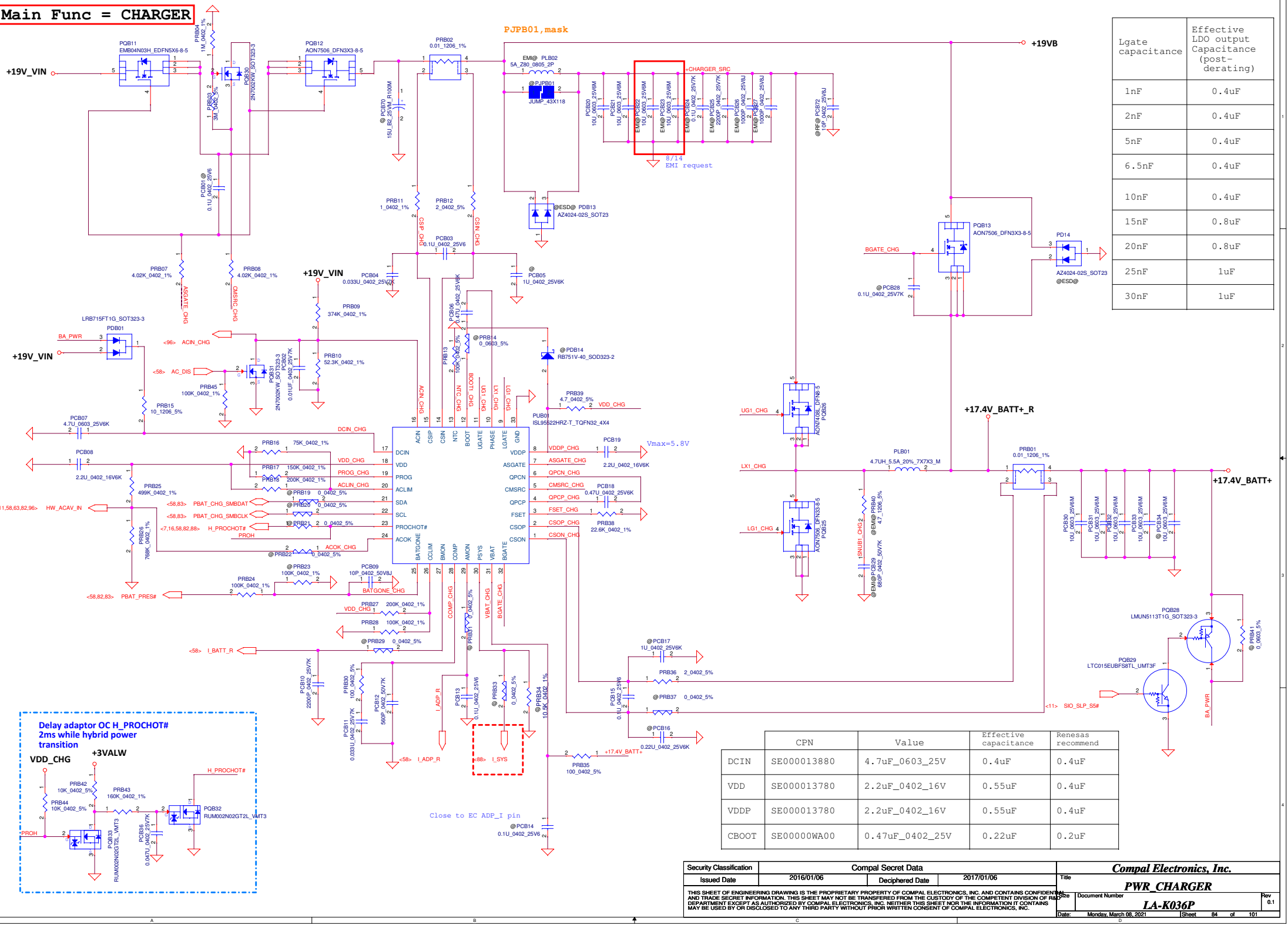
PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T



Compal Electronics, Inc.		
Title: PWR_BATT CONN		
Size	Document Number: LA-K036P	Rev: 0.1
Date: Monday, March 08, 2021	Sheet 83 of 101	

Main Func = CHARGER



Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

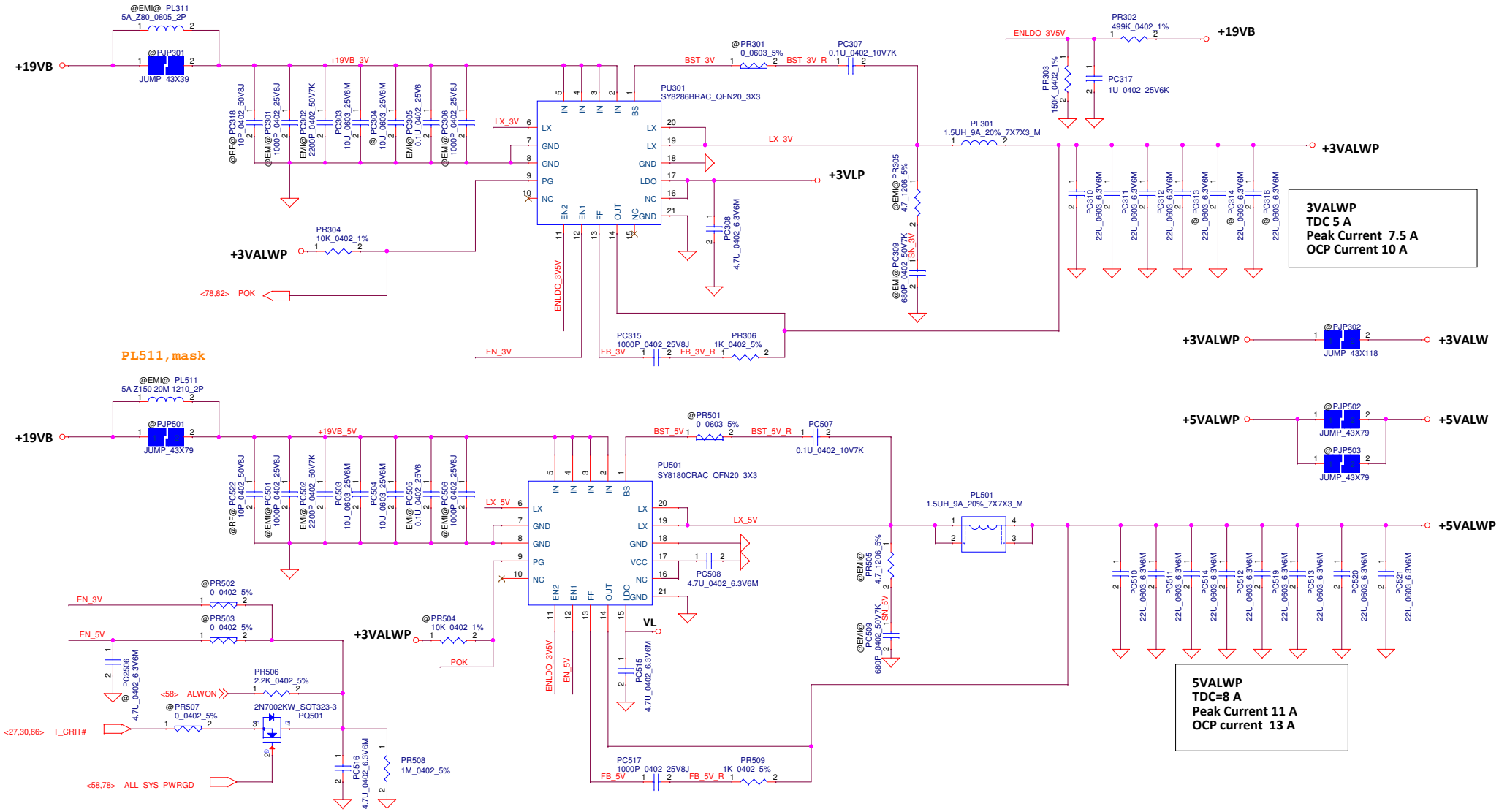
Compal Electronics, Inc.

Title: PWR_CHARGER

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 84 of 101

Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

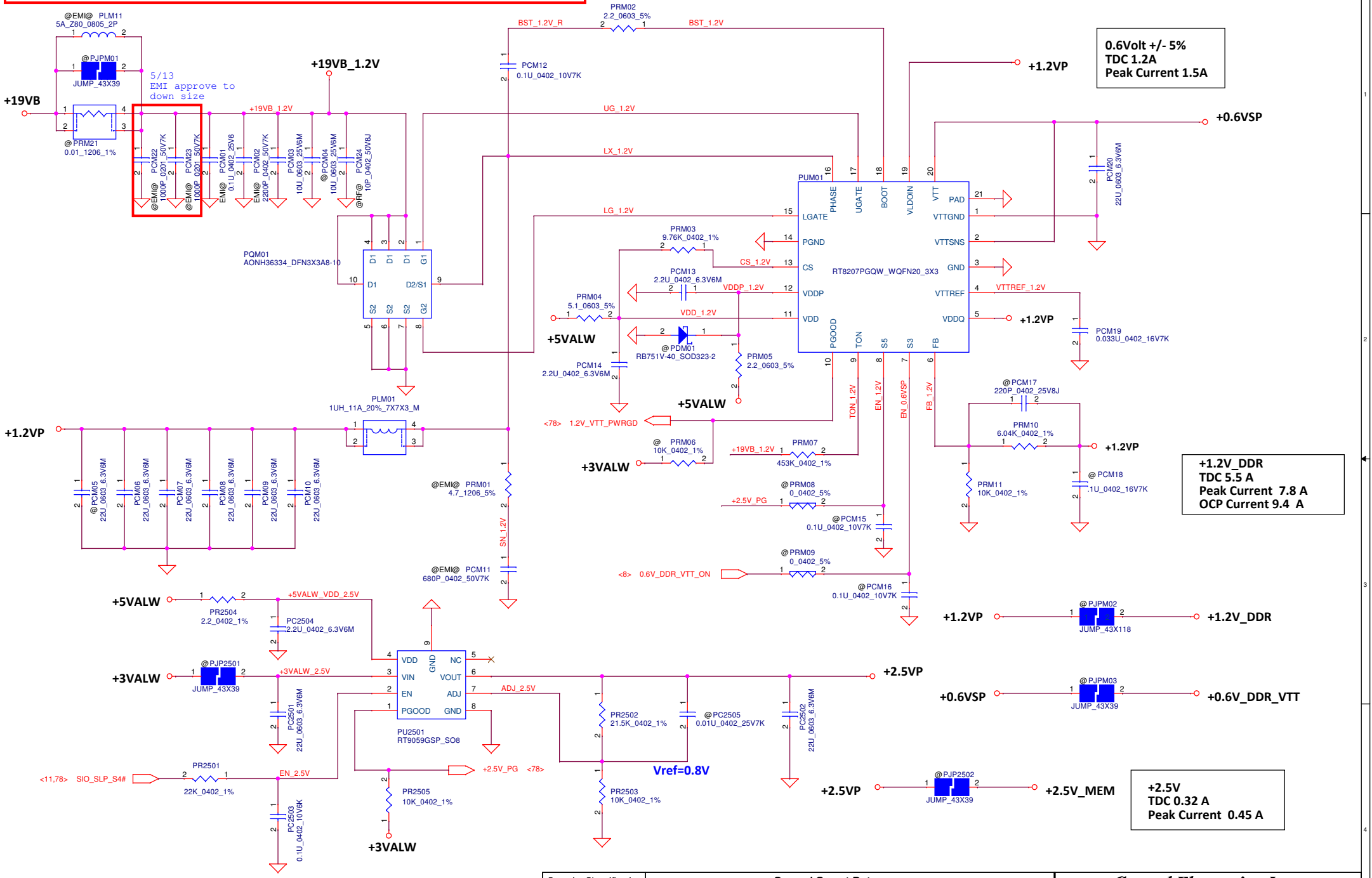
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size: B | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 85 of 101

Main Func = +1.2V_DDR/+0.6V_DDR_VTT/+2.5VP



Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

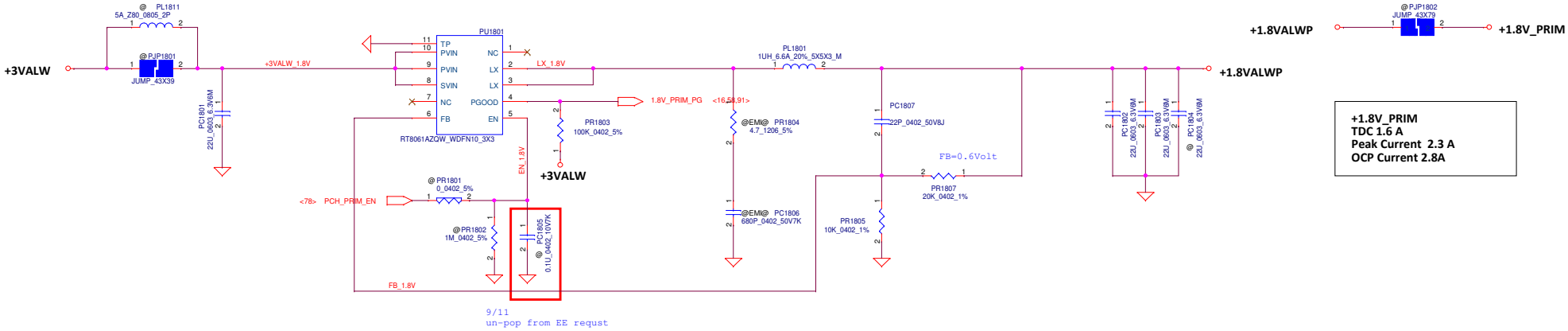
Compal Electronics, Inc.

Title: PWR_+1.2V_MEN/+0.6V_/+2.5VP

Size: | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 86 of 101

Main Func = +1.8VALWP / +1.05VALWP



9/11
un-pop from EE requst

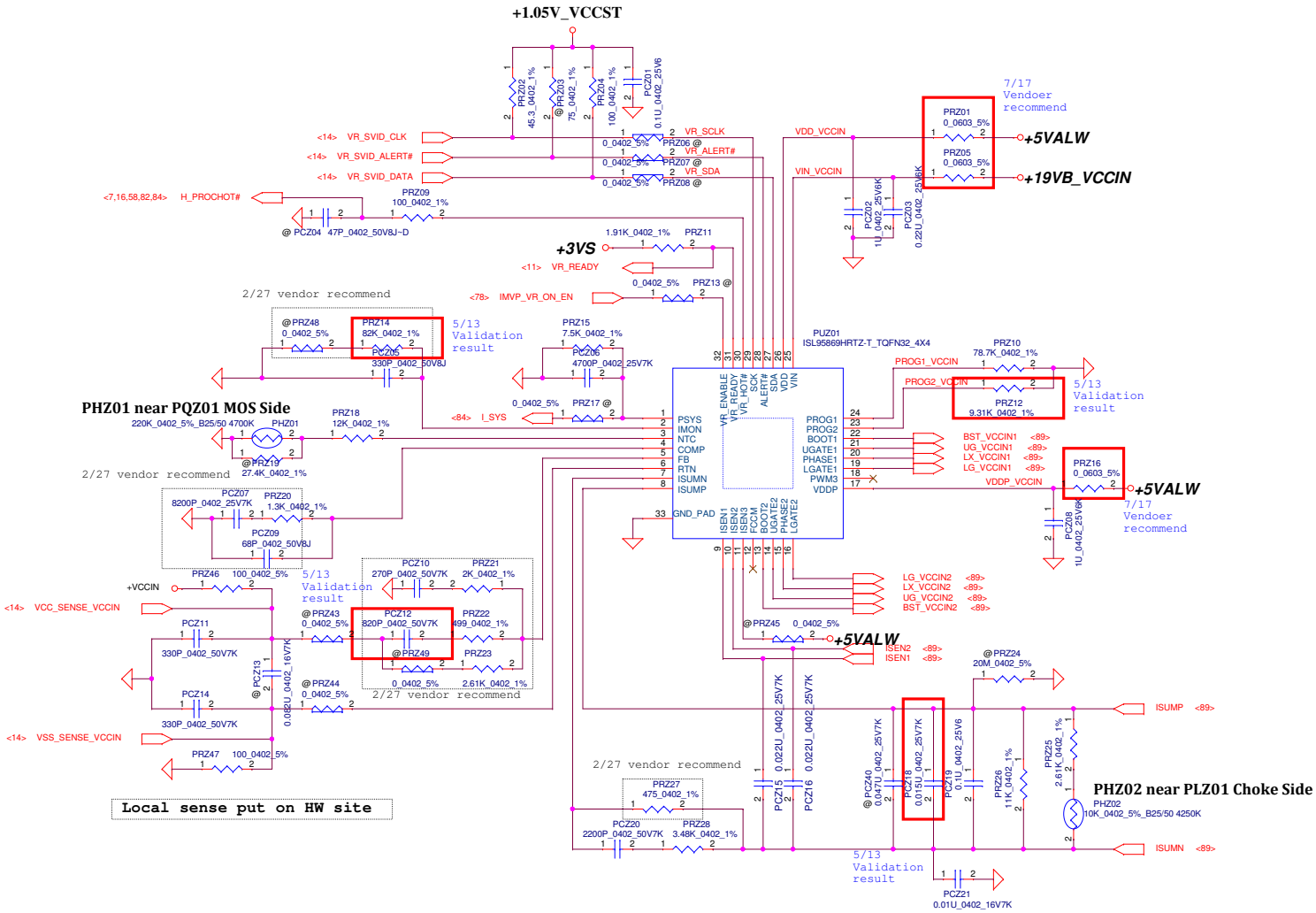
Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.

Title: PWR_+1.8VALWP

Size | Document Number: LA-K036P | Rev: 0.1

Date: Monday, March 08, 2021 | Sheet 87 of 101



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/11/05	Deciphered Date 2014/12/15	Title PWR_VCCIN
Size	Document Number LA-K036P		Rev 0.1
Date: Monday, March 08, 2021	Sheet 88 of 101		

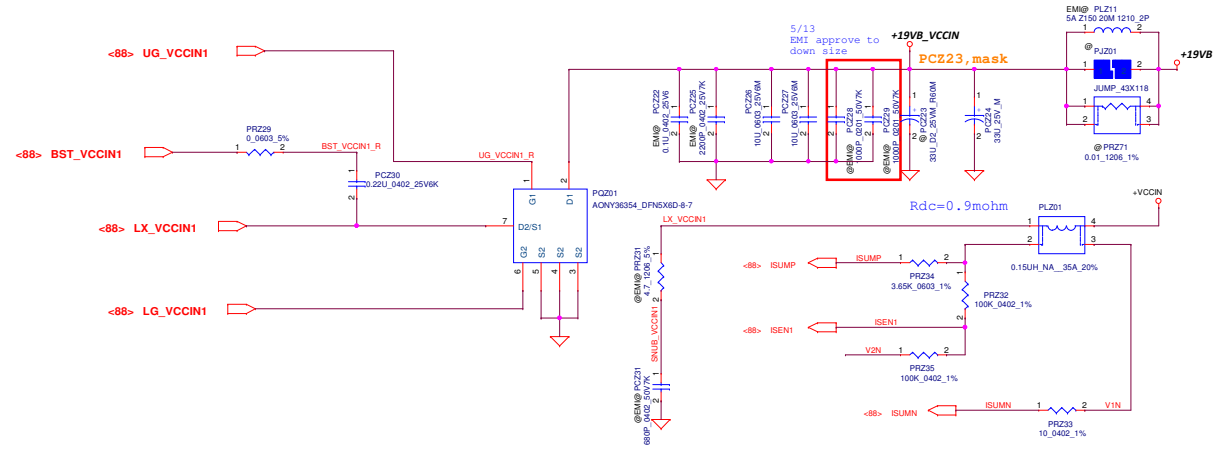
Baseline
UP3_4+2 15W (U42)

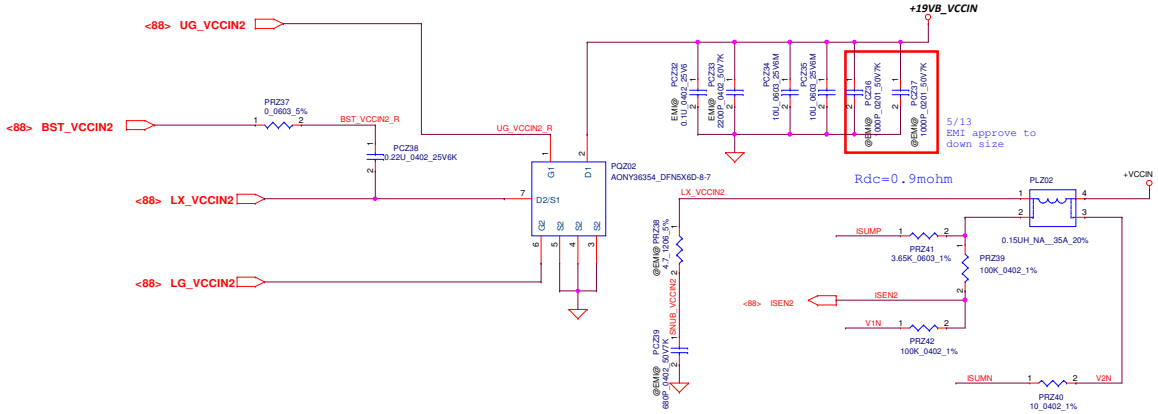
ICCMAX=47A
TDC=30A

Baseline
UP3_4+2 28W (U42)

ICCMAX=55A
TDC=36A

Frequency 750KHz





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	PWR_VCCIN		
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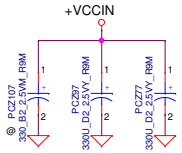
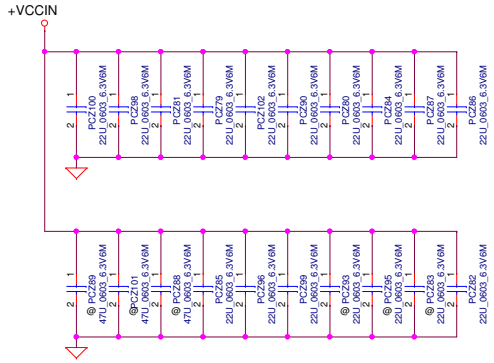
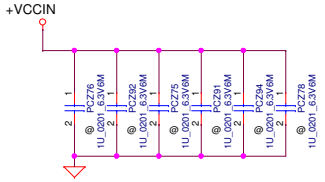
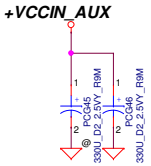
Main Func = VCCIN/ VCCIN_AUX



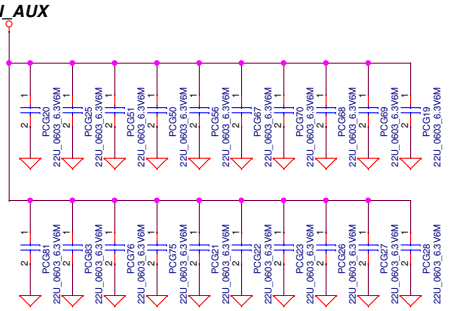
Primary side :
330U_R9 *2
22U_0603 *14

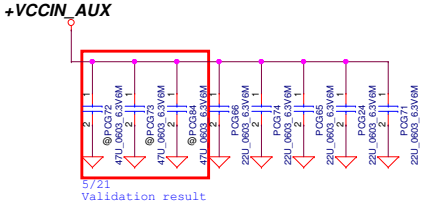






330U_R9 *1
22U_0603 *25





5/21
Validation result

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Compal Electronics, Inc.

Title: PWR_VCCIN/ VCCIN_AUX

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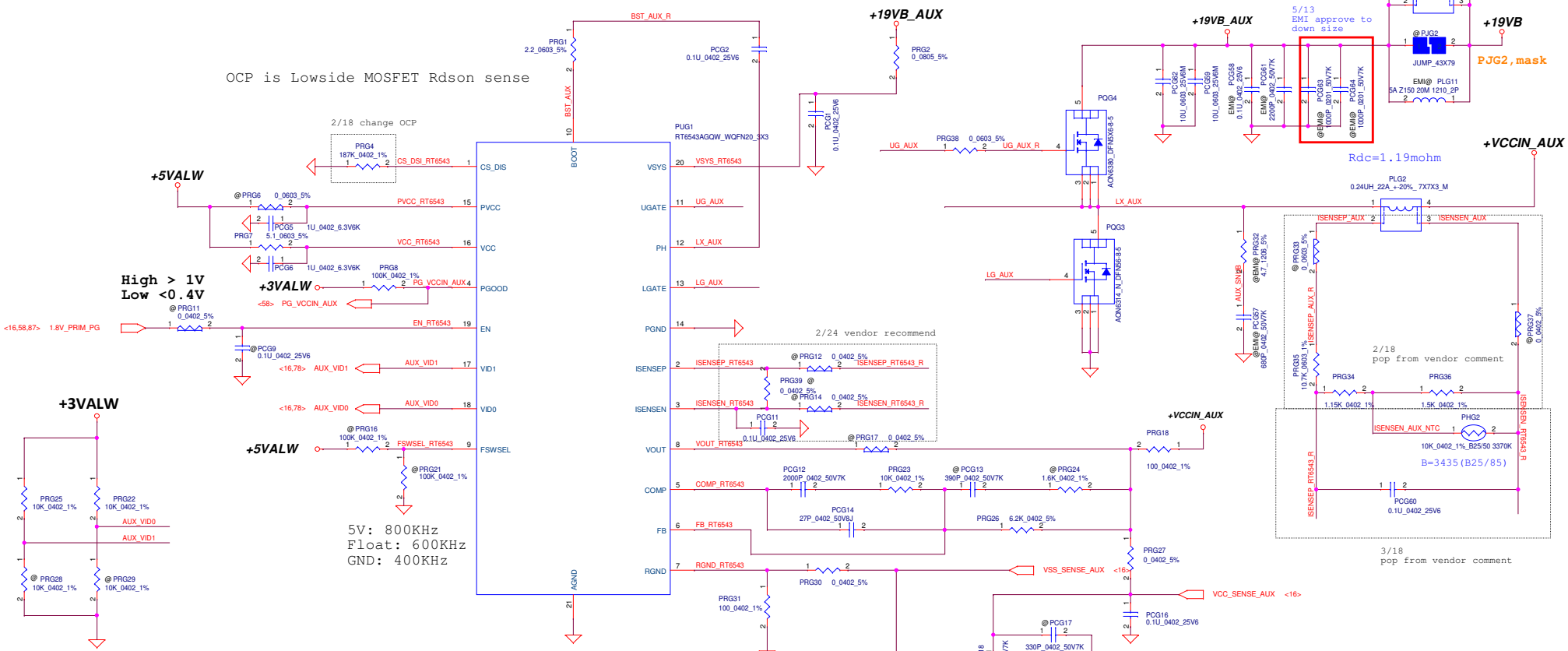
Main Func = VCCIN_AUX

ICCMAX=27A
TDC=14A
DC LL=1.8m(mV/A)
AC LL=TBD



VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

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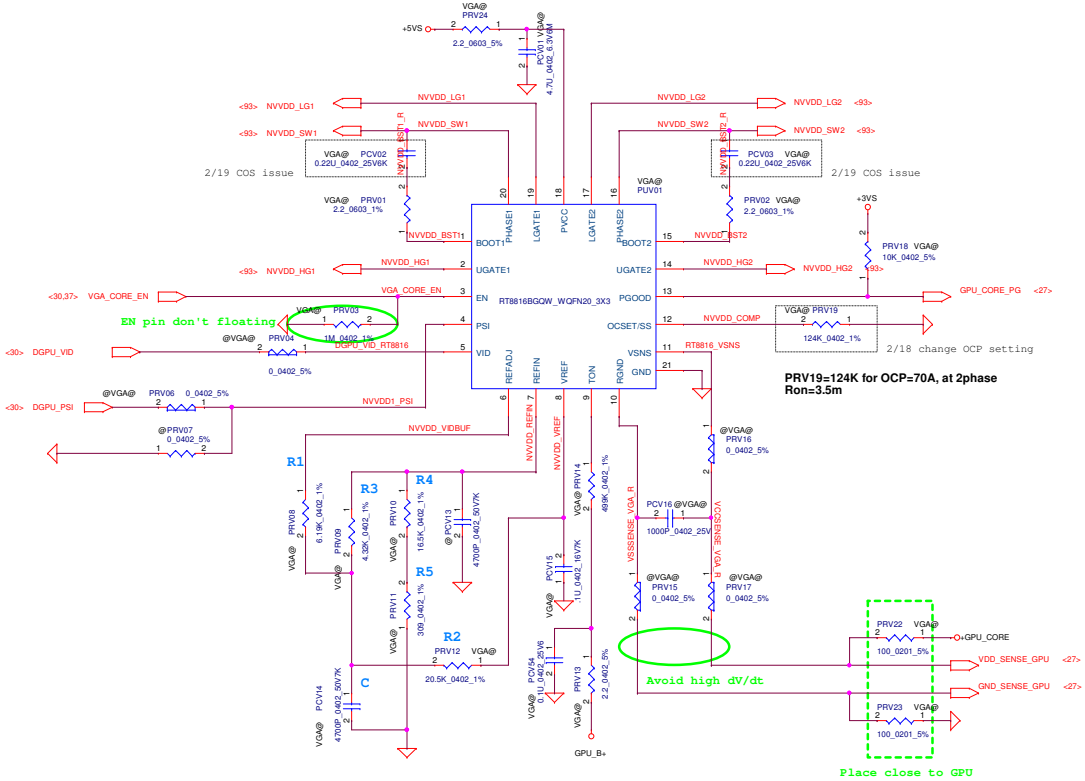
Main Func = VGA CORE



Operation Phase Number PSI Voltage Setting

1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

```
+GPU_CORE (N17S-G3)
TDC=29.8A
Peak Current 58.7A
OCP=  70A
DCR:0.98mohm +-5%
            TYP        MAX
H/SRds(on): 8.2mohm   10.5mohm
L/SRds(on): 2.8mohm    3.5mohm
```

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Compal Electronics, Inc.			
Title	PWR_VGA_CORE		
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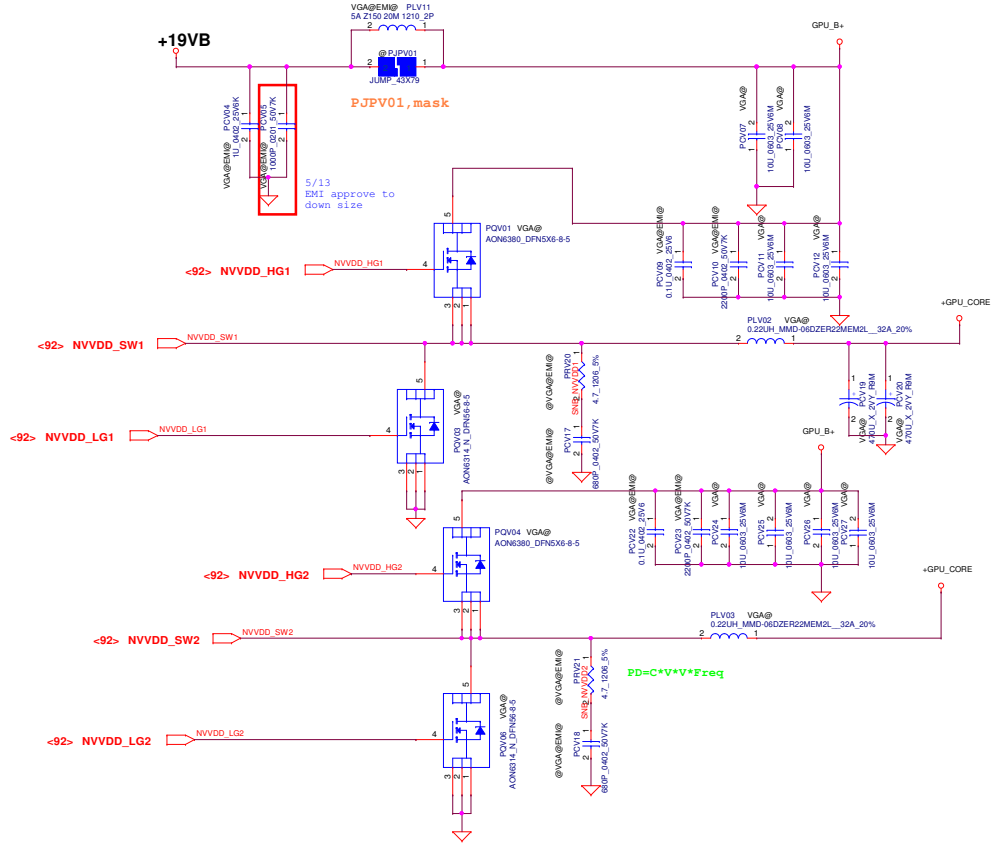
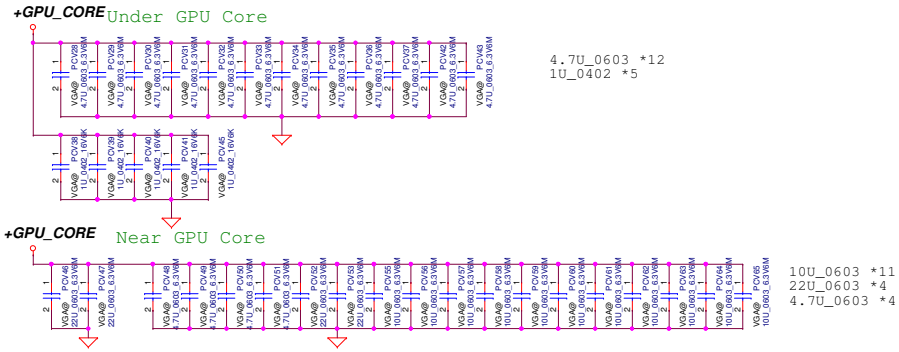
Main Func = VGA CORE





Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.			
Title	GPU_Decoupling		
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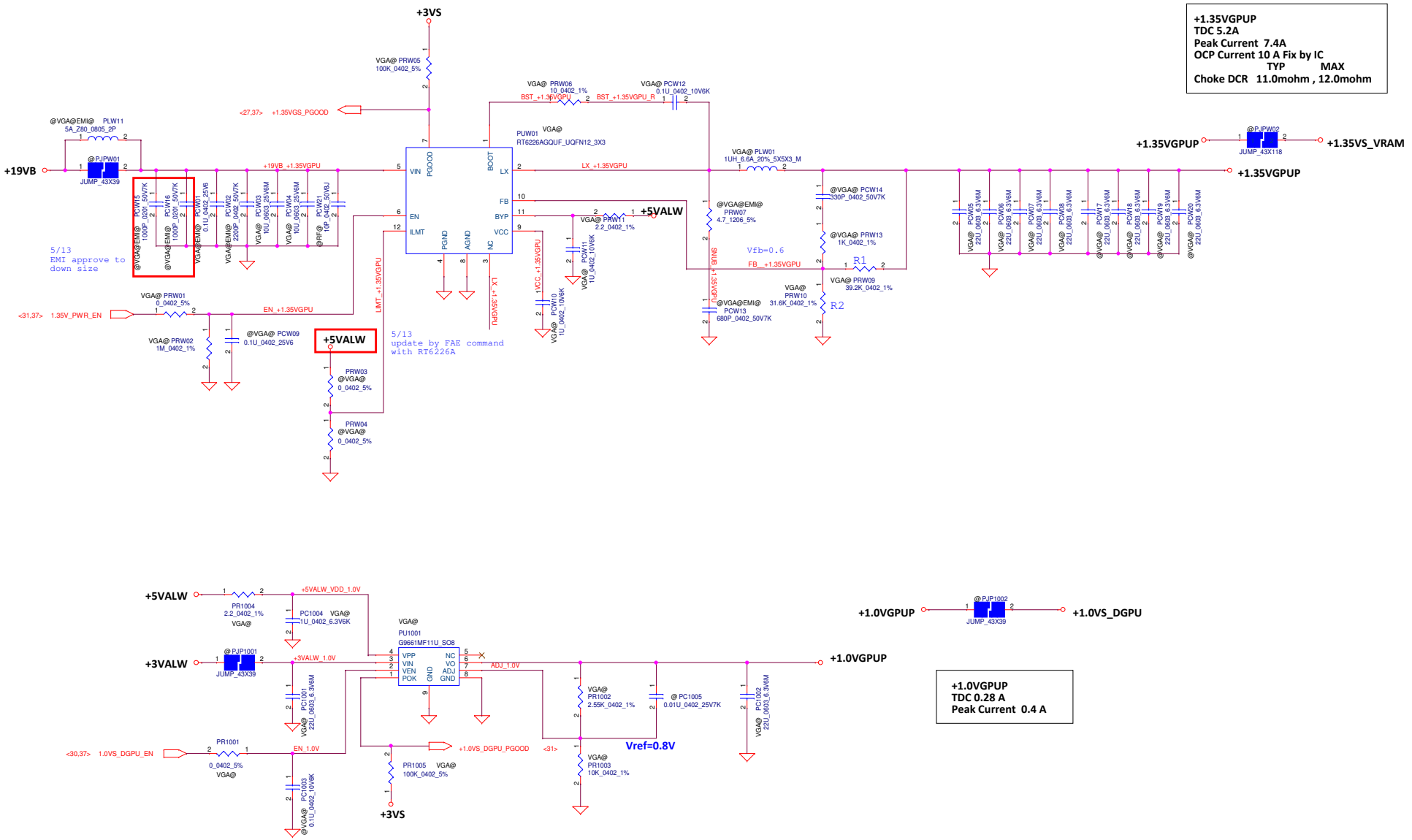
Main Func = +1.35VGPUP



Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.			
Title	PWR_+1.35VGPUP		
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Reserve

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Compal Electronics, Inc.		
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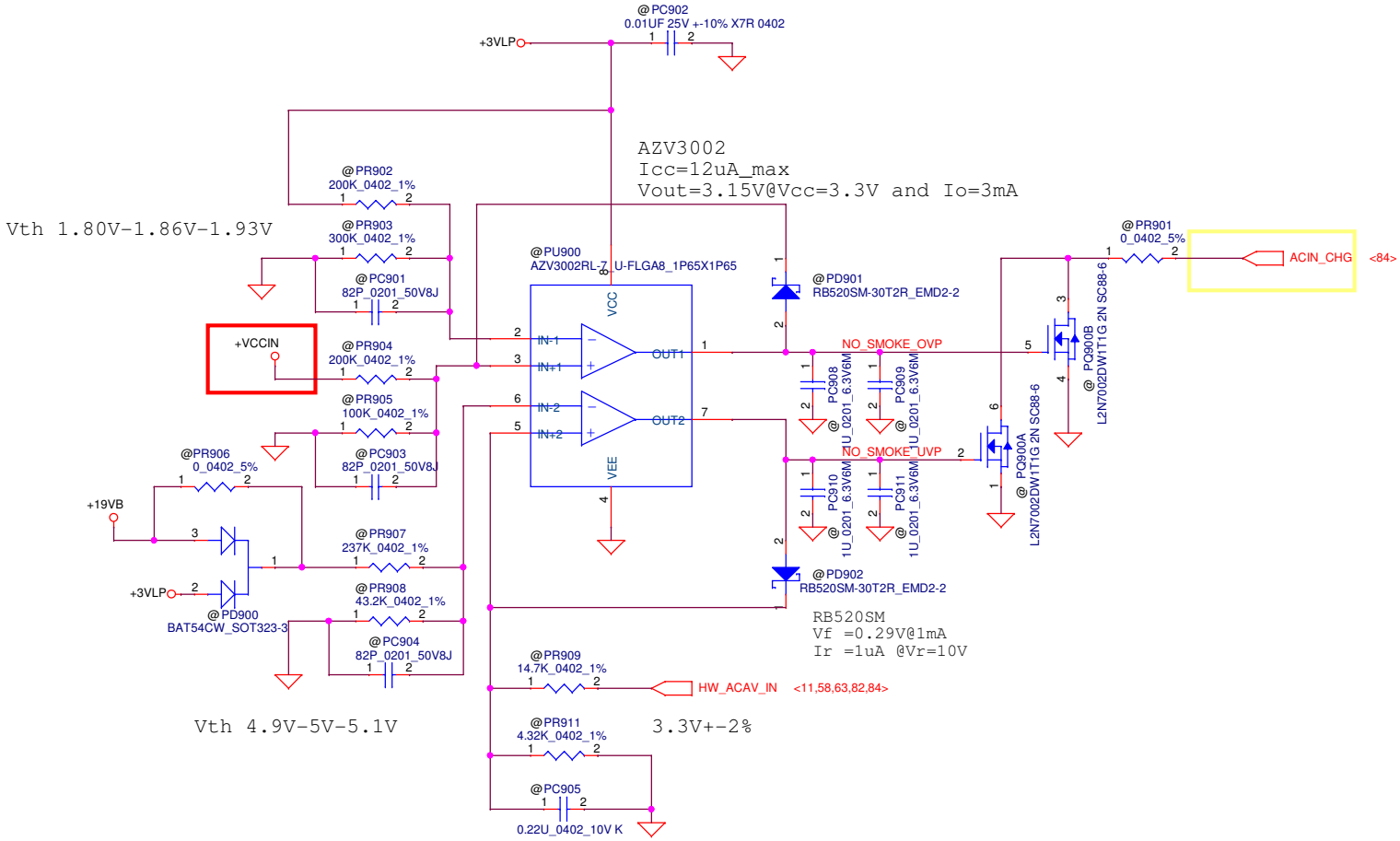

Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.

Title: **NO SMOKE**

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Reserve

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Reserve

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Compal Electronics, Inc.		
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Reserve

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Version Change List (P. I. R. List)

Item	Page #	Date	Request Owner	Issue Description	Solution Description	Rev.
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
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Version Change List (P. I. R. List)

DVT1 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 05/15								
1	2018/5/17	8		Add RC207, CPU_SPI_0_CS#1	For 2nd ROM	Y	N	Y
2	2018/5/17	66		Del JP7, short +5VS and +5VS_ODD	Optimal B+ routing	Y	N	Y
3	2018/5/17	14		CC52,CC48,CC51,C5 change to 0402	meet purchase requirement	Y	Y	Y
4	2018/5/17	29		CV73~CV78, CV100~CV109 change to 0402	meet purchase requirement	Y	Y	Y
5	2018/5/17	71		del CU3,CU8 CU4,CU9 1U change to 4.7U	meet purchase requirement	Y	Y	Y
6	2018/5/20			Del CS6,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize	Y	Y	Y
7	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch	Y	N	Y
8	2018/6/4	38		Connect UC1.CC30 to R72, Add RC208,RC209	For 17" Touch	Y	N	Y
9	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize	Y	Y	Y
10	2018/6/4	31		CV161,CV162,CV163,CV164,CV165,CV166,CV167,CV168,CV169,CV170,CV182,CV183, CV184,CV185,CV186,CV187,CV188,CV189,CV190,CV191,CL16 change to 0201	MLCC downsize	Y	Y	Y
11	2018/6/13	56		CA16 change to 0402	MLCC downsize	Y	Y	Y
12	2018/7/4	65		add Rx10~14	co-lay ST TPM	Y	N	Y
13	2018/7/4			add CC75(pop),CZ41,CC76,CC77,CC78,CC79	For ESD requirement	Y	Y	Y
14	2018/7/6	65		add Rx15~RX19	co-lay China TPM	Y	N	Y

DVT2 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 07/16								
1	2018/8/14	66	RX20,RX21,RX22	reserve 0 ohm 0402	reserve for china TPM	Y	N	Y
2	2018/8/15	38	R96	reserve 0 ohm 0201	disconnet B+	Y	N	Y
3			EU1,EU3,EU8,EU9	SC300002C00=>SC300001Y00	ESD require	Y	Y	N
4		71	RE1	SD034178280=>SD034270280 17.8K change to 27K	EC board ID	Y	Y	N
5			CC54,CC57		fixed 1.05 OVP(BITS382716)	Y	Y	N
6			UZ2	SA00007XR00=>SA00008R600(Vccio load switch)	fixed 1.05 OVP(BITS382716)	Y	Y	N
7				Remove Typec configuration	Dell PCR	N	Y	N
8			CC64,CC52,CC59,CC17,CC15,CC18,CC19	0402 1u =>0201 1u	MLCC downsize	Y	Y	Y
9			R52	7.15K =>6.49K	Fixed OTP issue(BITS383003)	Y	Y	N