Octopus_A/B (Gemini Lake)

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Quanta Computer Inc.

PROJECT : ZBA/ZBB

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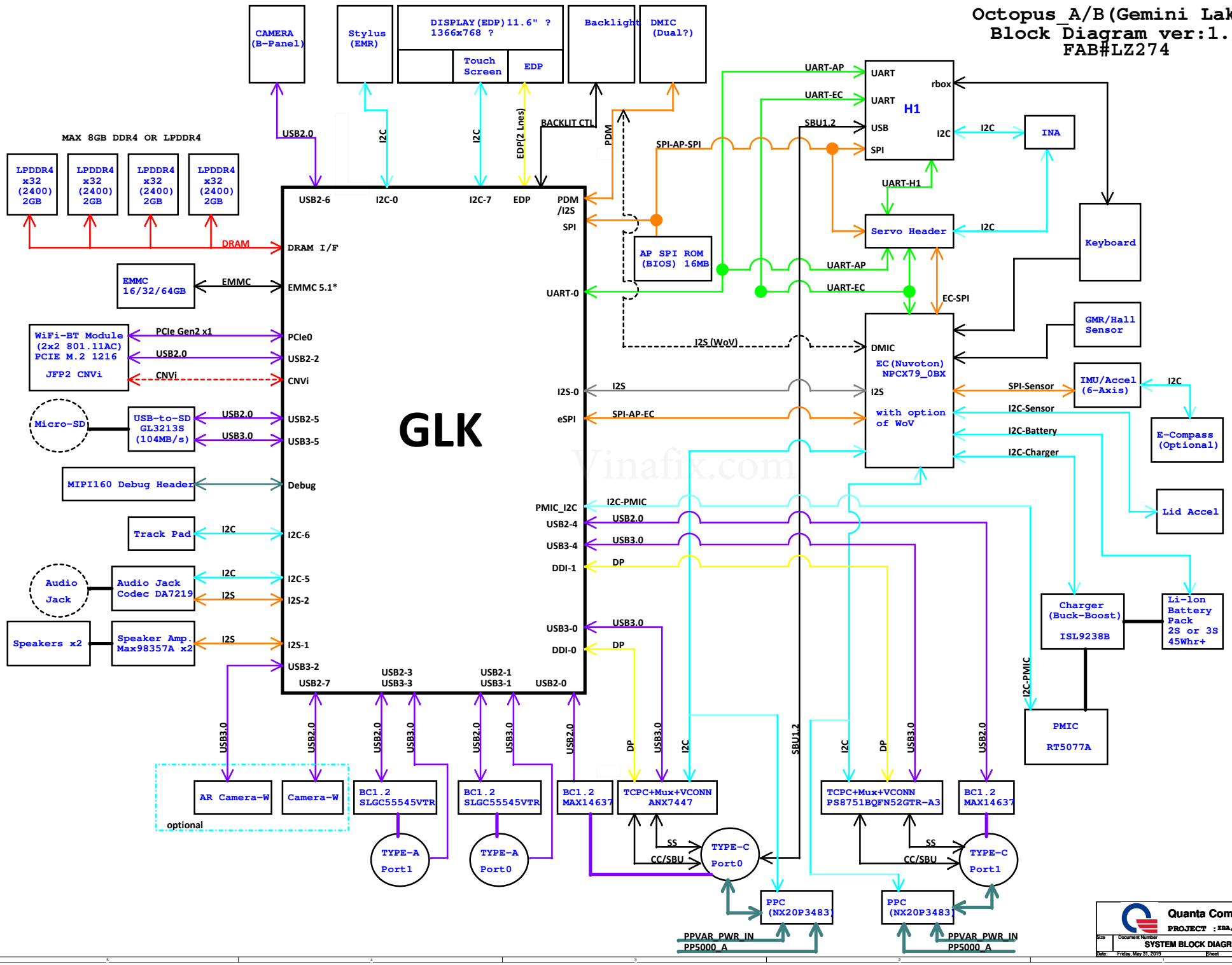
Octopus_A/B(Gemini Lake)
Block Diagram ver:1.0
FAB#LZ274
CAMERA (B-Panel)
Stylus (EMR)
DISPLAY(EDP)11.6" ? 1366x768 ?
Touch Screen
EDP
Backlight
DMIC (Dual?)
MAX 8GB DDR4 OR LPDDR4
LPDDR4 x32 (2400) 2GB
LPDDR4 x32 (2400) 2GB
LPDDR4 x32 (2400) 2GB
LPDDR4 x32 (2400) 2GB
DRAM
EMMC 16/32/64GB
EMMC
WiFi-BT Module (2x2 801.11AC) PCIE M.2 1216
JFP2 CNVi
PCIe Gen2 x1
USB2.0
CNVi
Micro-SD
USB-to-SD GL3213S (104MB/s)
USB2.0
USB3.0
MIPI160 Debug Header
Track Pad
I2C
Audio Jack
Audio Jack Codec DA7219
I2S
Speakers x2
Speaker Amp. Max98357A x2
GLK
USB2-6
I2C-0
I2C-7
EDP
PDM /I2S
SPI
DRAM I/F
EMMC 5.1*
PCIe0
USB2-2
CNVi
USB2-5
USB3-5
Debug
I2C-6
I2C-5
I2S-2
I2S-1
USB3-2
USB2-7
USB2-3
USB3-3
USB2-1
USB3-1
USB2-0
UART-0
I2S-0
eSPI
PMIC_I2C
USB2-4
USB3-4
DDI-1
USB3-0
DDI-0
USB2.0
I2C
I2S
EDP(2 Lines)
BACKLIT CTL
PDM
SPI-AP-SPI
AP SPI ROM (BIOS) 16MB
UART-AP
UART-EC
SBU1.2
H1
UART
rbox
USB
SPI
UART-H1
Servo Header
INA
Keyboard
EC-SPI
GMR/Hall Sensor
I2S (WoV)
DMIC
EC(Nuvoton) NPCX79_0BX
with option of WoV
SPI-Sensor
IMU/Accel (6-Axis)
I2C-Sensor
I2C-Battery
I2C-Charger
E-Compass (Optional)
Lid Accel
I2C-PMIC
Charger (Buck-Boost) ISL9238B
Li-Ion Battery Pack 2S or 3S 45Whr+
PMIC RT5077A
AR Camera-W
Camera-W
optional
BC1.2 SLGC55545VTR
BC1.2 SLGC55545VTR
BC1.2 MAX14637
TCPC+Mux+VCONN ANX7447
TCPC+Mux+VCONN PS8751BQFN52GTR-A3
BC1.2 MAX14637
TYPE-A Port1
TYPE-A Port0
SS
CC/SBU
TYPE-C Port0
TYPE-C Port1
PPC (NX20P3483)
PPC (NX20P3483)
PPVAR_PWR_IN
PP5000_A
PPVAR_PWR_IN
PP5000_A
Quanta Computer Inc.
PROJECT : ZBA/ZBB
SYSTEM BLOCK DIAGRAM
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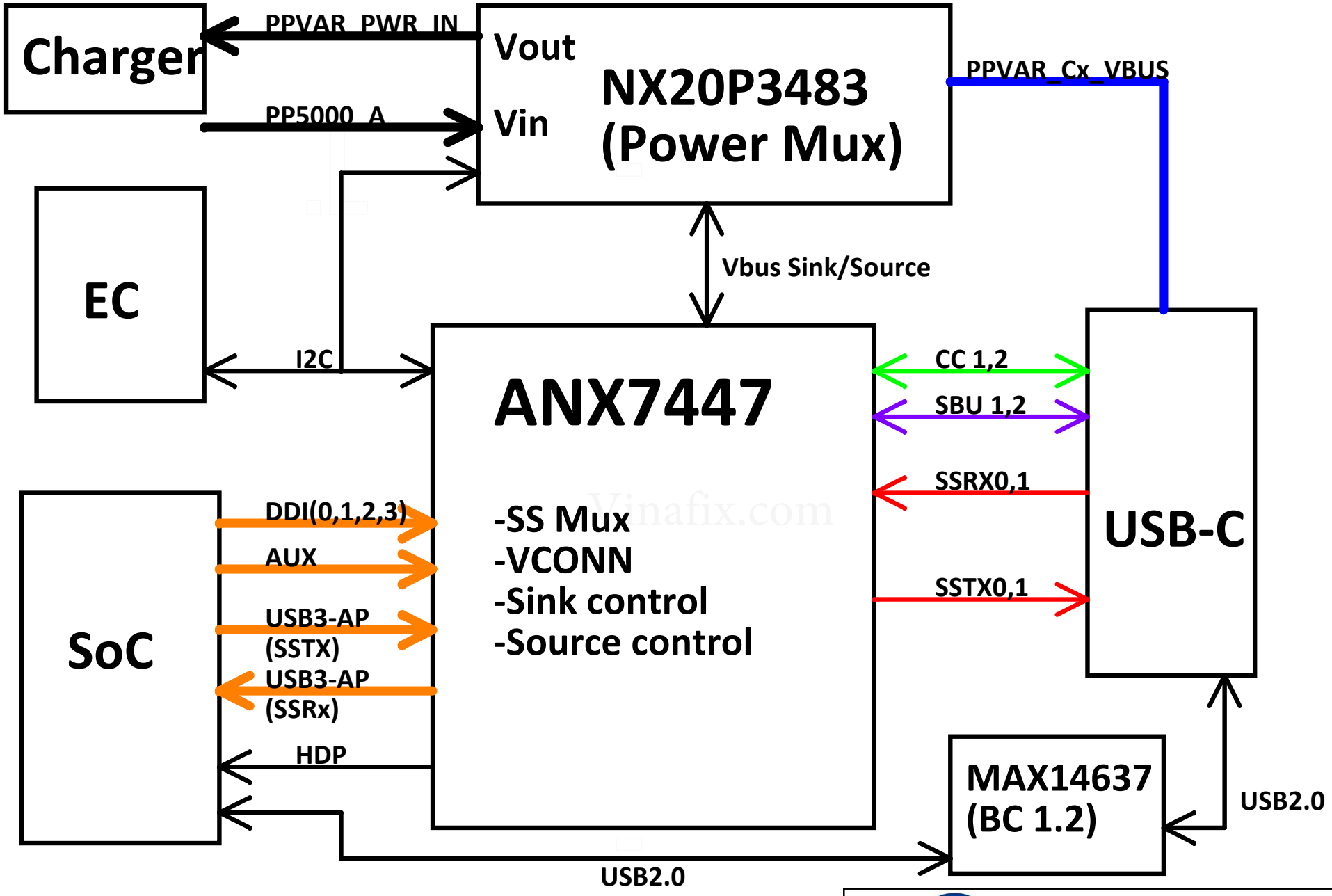

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PROJECT : ZBA/ZBB

Size	Document Number	Rev
	USB TYPE-C BLOCK DIAGRAM	1A

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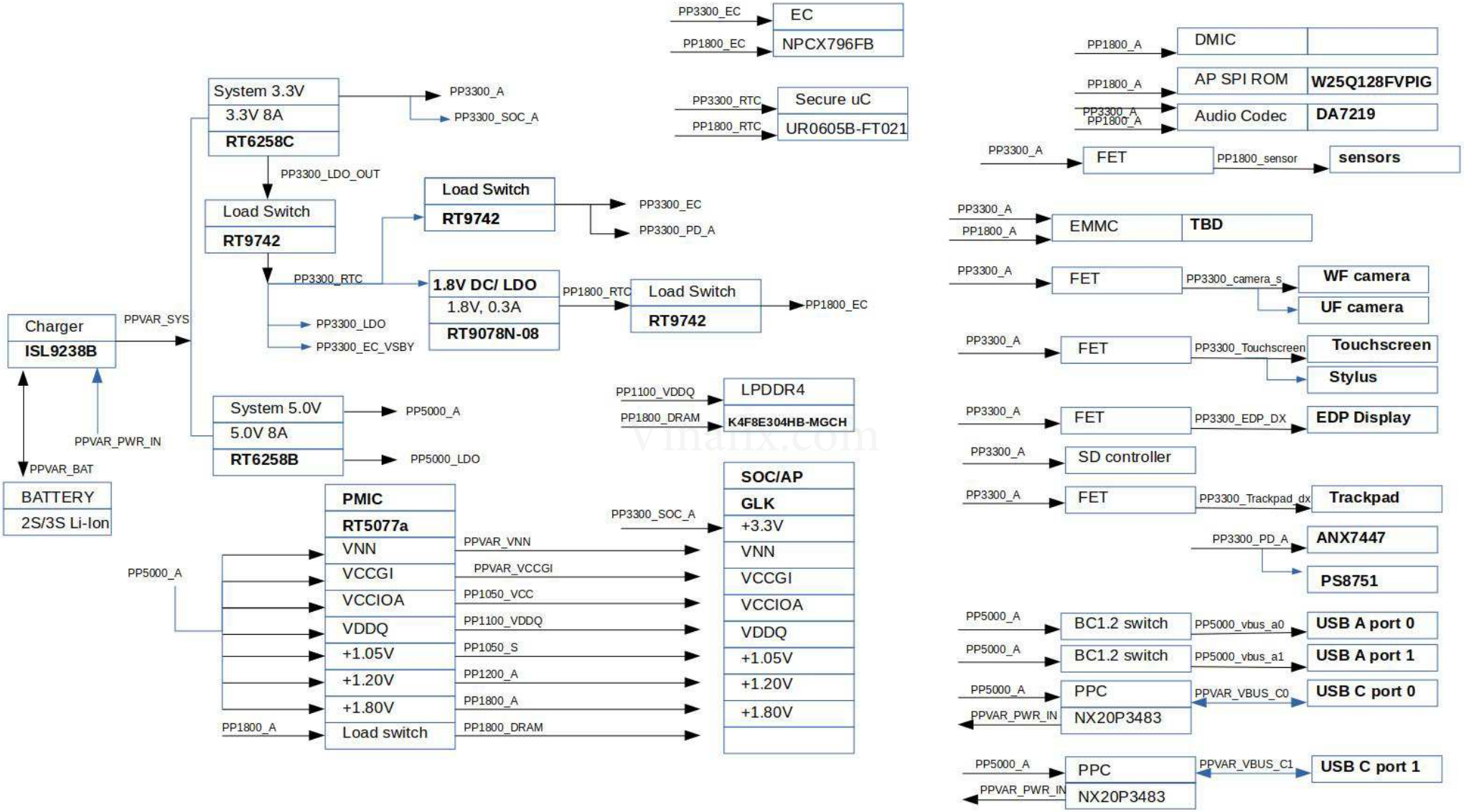
Power Tree



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Size	Document Number	Rev
	Power Tree	1A

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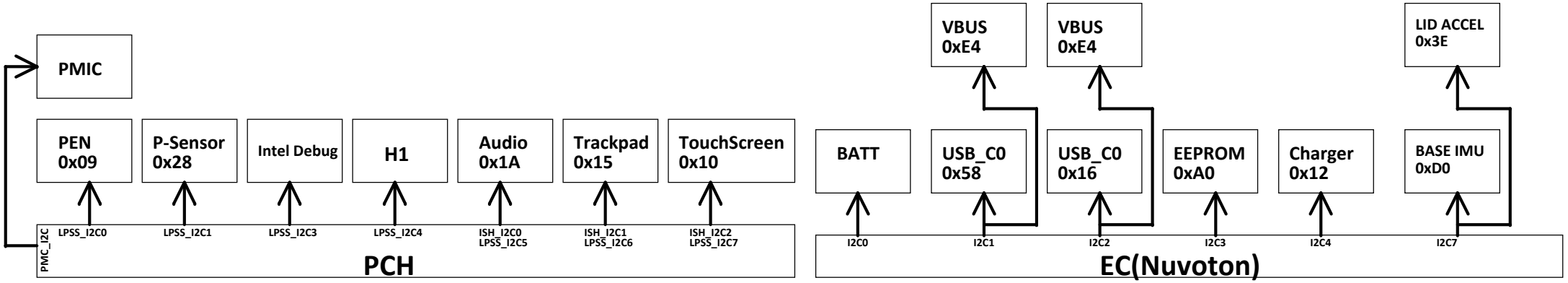
Master	Port	Net Name	Slave Device(S)	Speed
EC	I2C0_0	EC_I2C_BATTERY_3V3	BATTERY (TBD)	100KHZ
EC	I2C1_0	EC_I2C_USB_C0_MUX	ANX7447, NX20P3483	100KHZ
EC	I2C2_0	EC_I2C_USB_C1_MUX	*Check subboard*	100KHZ
EC	I2C3_0	EC_I2C_EEPROM_SCL	M34E02	100KHZ
EC	I2C4_1	EC_I2C_CHARGER_3V3	ISL9238B	100KHZ
EC	I2C5_0	-		
EC	I2C7_0	EC_I2C_SENSOR_U	LSM6DS3TR, LIS2MDLTR	400KHZ
AP	LPSS_I2C0	PCH_I2C_PEN	STYLUS (TBD)	400KHZ
AP	LPSS_I2C1	PCH_I2C_P_SENSOR	TBD	100KHZ
AP	LPSS_I2C2	-		
AP	LPSS_I2C3	DBG_PCH_I2C	TBD	TBD
AP	LPSS_I2C4	PCH_I2C_H1	H1 (not used)	100KHZ
AP	LPSS_I2C5	PCH_I2C_AUDIO	DA7219	100KHZ
AP	LPSS_I2C6	PCH_I2C_TRACKPAD	TRACKPAD (TBD)	100KHZ
AP	LPSS_I2C7	PCH_I2C_TOUCHSCREEN	TOUCHSCREEN (TBD)	100KHZ
AP	PMC_I2C	PCH_PMIC_I2C	RT5077A	100KHZ



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Size	Document Number	Rev
	I2C MAP	1A
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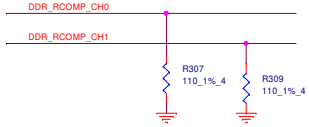
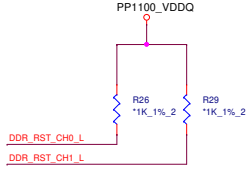
(CPU)



PLACE AS CLOSE TO SOC AS POSSIBLE



Quanta Computer Inc.			
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	SOC DRAM I/F		1A
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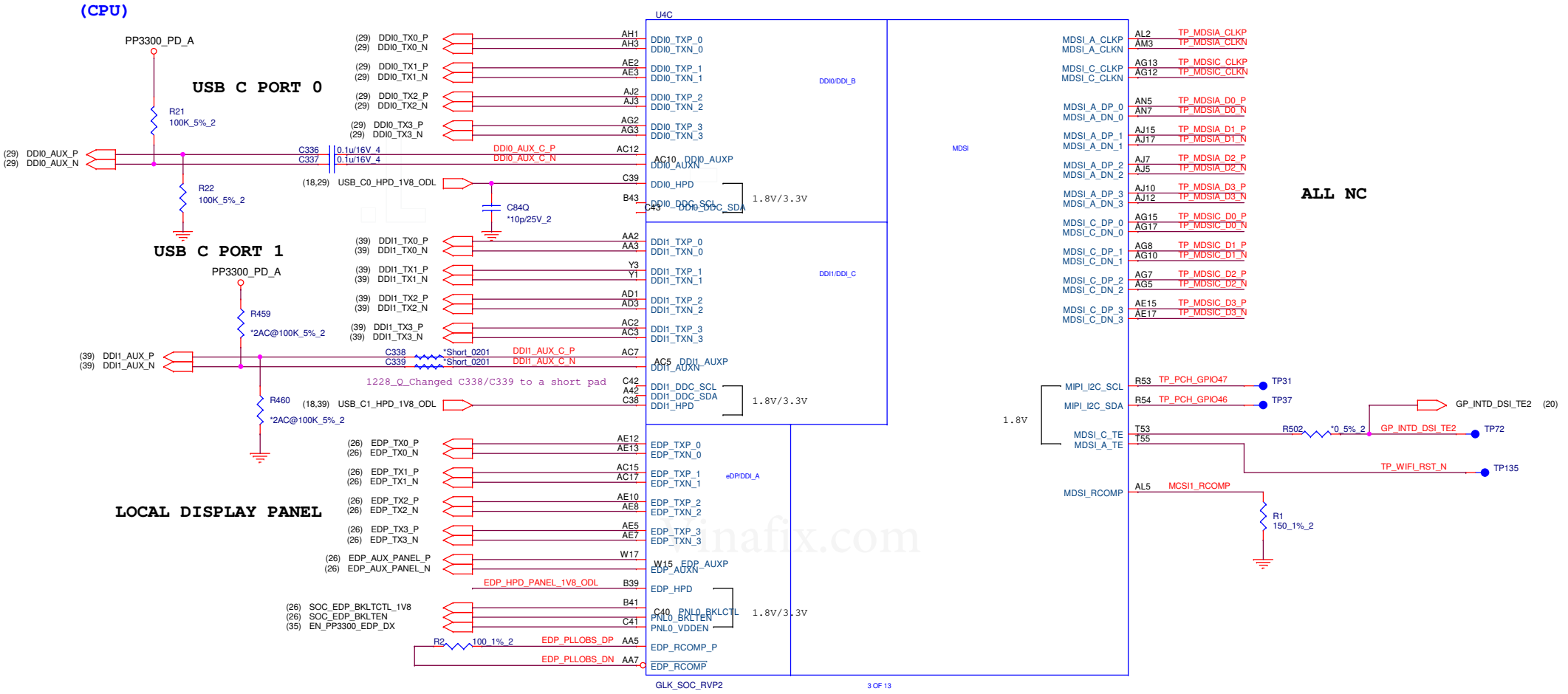
Gemini lake (DISPLAY,eDP)



Quanta Computer Inc.			
PROJECT : ZBA/ZBB			
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	SOC EDP/MIPI/DDI		1A
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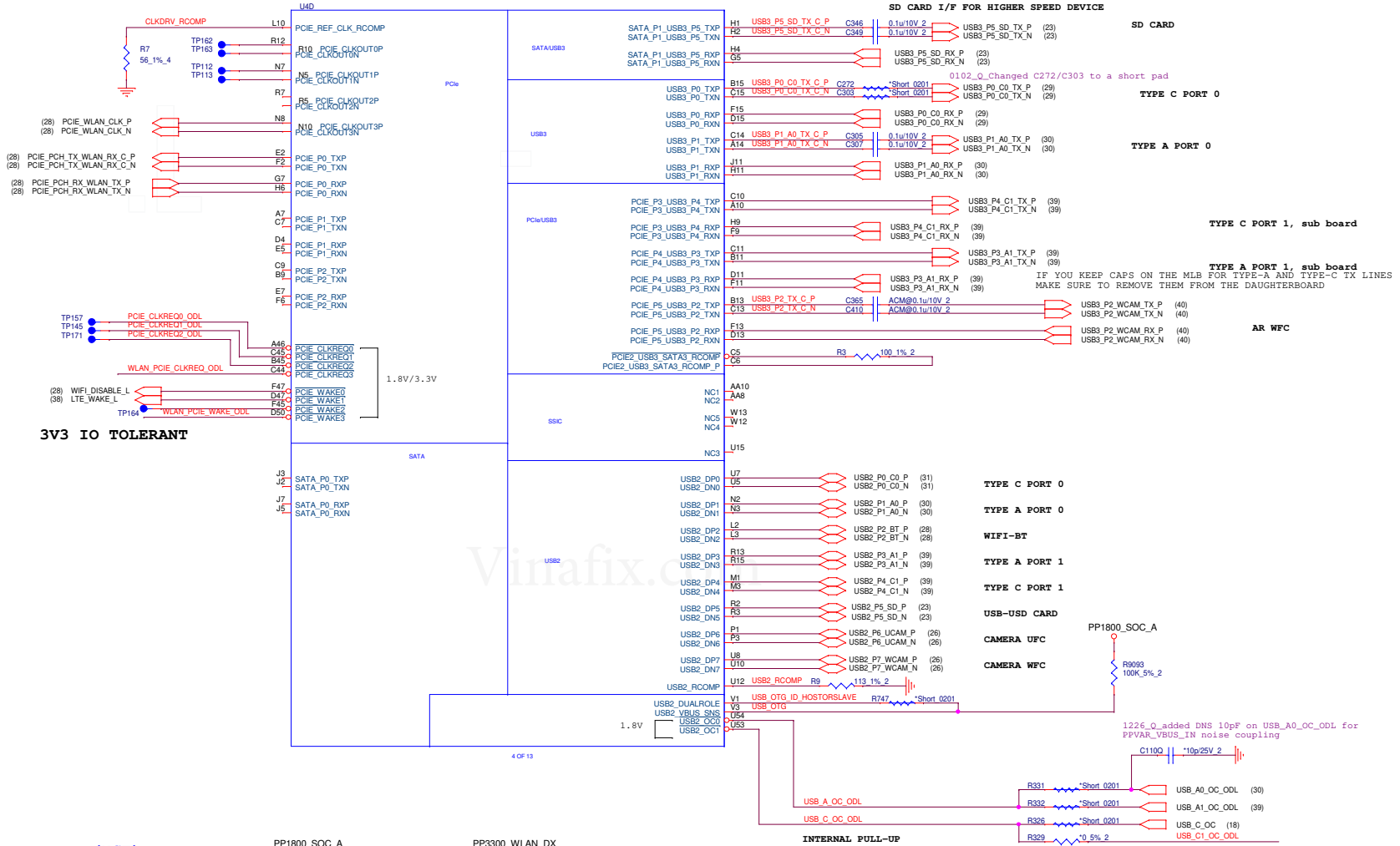
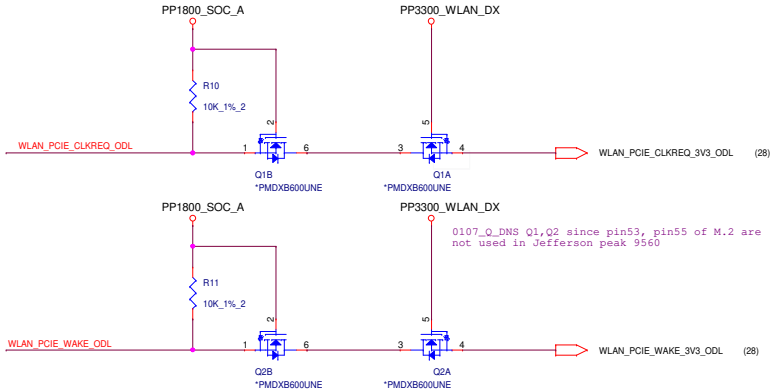
Gemini lake (SATA , ODD, CLK ,USB,PCIE)

(CPU)



(NGF)



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PROJECT : ZBA/ZBB
Size | Document Number: SOC PCIE/USB/SATA | Rev 1A
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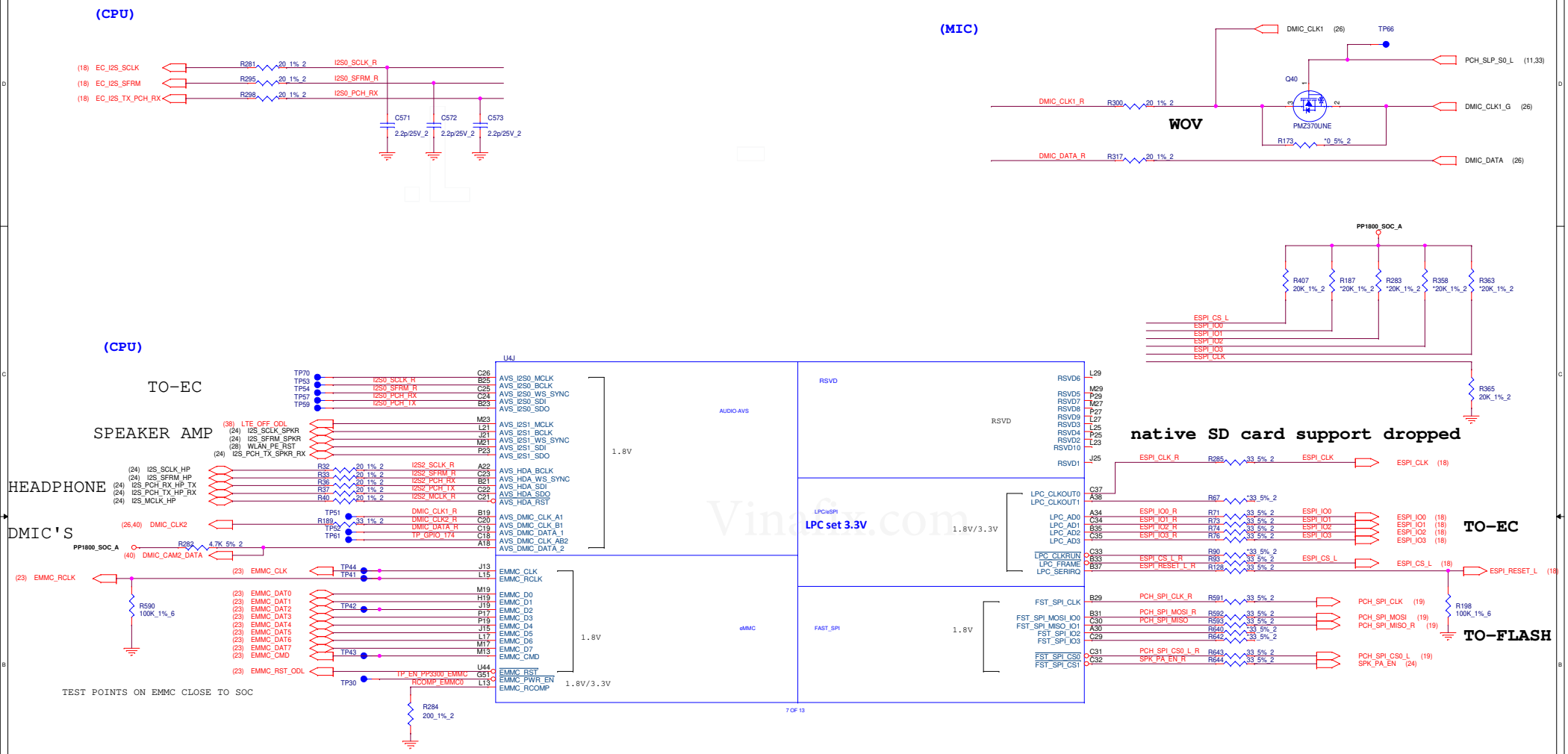
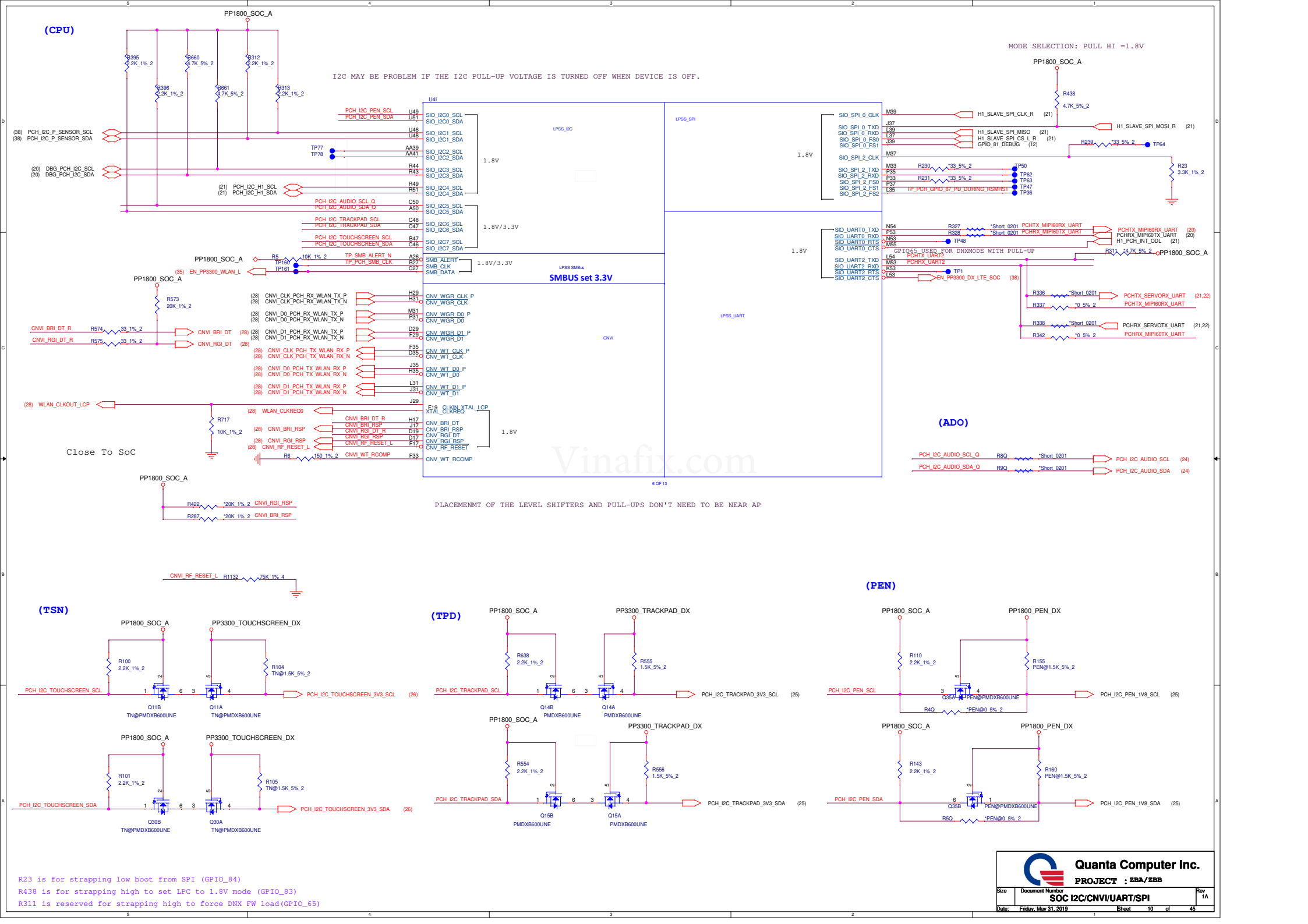
Gemini lake (EMMC/LPC/I2C/GPIO/HDA)




(CPU)
PP1800_SOC_A
I2C MAY BE PROBLEM IF THE I2C PULL-UP VOLTAGE IS TURNED OFF WHEN DEVICE IS OFF.
MODE SELECTION: PULL HI =1.8V
SMBUS set 3.3V
PLACEMENMT OF THE LEVEL SHIFTERS AND PULL-UPS DON'T NEED TO BE NEAR AP
Close To SoC
(ADO)
(TSN)
(TPD)
(PEN)
PP3300_TOUCHSCREEN_DX
PP3300_TRACKPAD_DX
PP1800_PEN_DX
R23 is for strapping low boot from SPI (GPIO_84)
R438 is for strapping high to set LPC to 1.8V mode (GPIO_83)
R311 is reserved for strapping high to force DNX FW load(GPIO_65)
Quanta Computer Inc.
PROJECT : ZBA/ZBB
SOC I2C/CNVI/UART/SPI
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Vendor	Dram PartNumber	RAM ID	Memory	Rank Density	Dual Rank
Micron	MT53B256M32D1NP-062	0 (0000)	4GiB	8Gb	N
Hynix	H9HCNNN8KUMLHR-NME	0 (0000)	4GiB	8Gb	N
Samsung	K4F8E304HB-MGCJ	0 (0000)	4GiB	8Gb	N
Nanya	NT6AN256T32AV-J2	0 (0000)	4GiB	8Gb	N
Micron	MT53E512M32D2NP-046	1 (0001)	8GiB	16Gb	N
Samsung	K4F6E3S4HM-MGCJ	1 (0001)	8GiB	16Gb	N
Kingston	B5116PC2WDGPKR	1 (0001)	8GiB	16Gb	N
Micron	MT53B512M32D2NP-062	2 (0010)	8GiB	8Gb	Y
Hynix	H9HCNNNBPUMLHR-NME	2 (0010)	8GiB	8Gb	Y
Samsung	K4F6E304HB-MGCJ	2 (0010)	8GiB	8Gb	Y

Gemini lake (PMU/PMIC/RTC)

(CPU)

PP1800_SOC_A

R371 100K_5%_2 DRAM_ID0
R376 *100K_5%_2 DRAM_ID1
R382 100K_5%_2 DRAM_ID2
R399 *100K_5%_2 DRAM_ID3
R373 *100K_5%_2
R378 100K_5%_2
R385 *100K_5%_2
R402 100K_5%_2

PP3300_SOC_A

R557 100K_5%_2
R276 100K_5%_2

PP1050_VCCRAM_S

R56 *68_1%_2
R58 *169_1%_4
R63 *84.5_1%_4

(18) SUSPWRDNACK

U4E

(33) PCH_PMIC_I2C_SCL → R46 → PMC_I2C_SCL
(33) PCH_PMIC_I2C_SDA → R48 → PMC_I2C_SDA
TP_AP_PMC_SPI_CLK → L48 PMC_SPI_CLK
DRAM_ID0 → N48 PMC_SPI_FS0
DRAM_ID1 → N44 PMC_SPI_FS1
DRAM_ID2 → L49 PMC_SPI_FS2
DRAM_ID3 → L51 PMC_SPI_RXD
TP_AP_PMC_SPI_TX → N49 PMC_SPI_TXD
1.8V
PMC

PLT_RST_L → D54 PMU_PLTRST
(12,18) EC_PCH_PWR_BTN_ODL → E53 PMU_PWRBTN
(9,33) PCH_SLP_S0_L → C52 PMU_SLP_S0
(33) PCH_SLP_S3_L → D51 PMU_SLP_S3
(33) PCH_SLP_S4_L → J49 PMU_SLP_S4
SUSPWRDNACK → F54 SUSPWRDNACK
PMU_BATLOW_L → J48 PMU_BATLOW
(12,18,21,22) SYS_RST_ODL → C51 PMU_RSTBTN
(28) PCH_SUSCLK → G49 PMU_SUSCLK
(28) BT_DISABLE_L → E52 SUS_STAT
1.8V/3.3V
PMU

TP81 TP82 TP83 → TP_PCH_GPIO_78 F55 SVID0_CLK
TP_PCH_GPIO_77 G53 SVID0_DATA
TP_PCH_GPIO_76 G54 SVID0_ALERT
1.05V
SVID

TP87 TP88 → DEBUG_OBS_PORT_A0 D1 DEBUG_PORT_A0
DEBUG_OBS_PORT_A1 D2 DEBUG_PORT_A1
A54 NC2
C54 NC11
Misc

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RTC is 3.3V
PMU set 3.3V
1.8V

iCLK
1.8V OSC_CLK_OUT_0 B17
OSC_CLK_OUT_1 C17
OSCIN U2 PCH_OSCIN
OSCOUT T1 PCH_OSCOUT

RTC
D23 RTC_X1 PCH_RTC_X1
F23 RTC_X2 PCH_RTC_X2
J23 VCC_RTC_EXTPAD RTC_EXPAD
H25 INTRUDER INTRUDER
D25 SOC_PWROK EC_PCH_PWROK
F27 RSM_RST PCH_RSMRST_L
F25 RTC_TEST PCH_RTEST_ODL
D27 RTC_RST PCH_RTCRST_ODL

Thermal
1.8V
THERMTRIP J53
PROCHOT J54
NC3 H53
NC15 AG44
NC4 H55
NC16

Spare
NC1 A4
NC5 BH1
SKTOCC A53
NC14 F37
NC6 BL2
NC7 BL3
NC8 BL53
NC9 C2
NC10 C3
NC17 R41

EC_IN_RW_OD (21) → PCH_WP_OD (19)
EC_PCH_PWROK (18) → PCH_RSMRST_L (12,18)
THERMTRIP_L (33) → PCH_PROCHOT_ODL (18,37)

PP3300_RTC
R8 100K_5%_2
C360 0.1u/10V_2
R735 *Short_0201
R46 100K_5%_2

SEL BOM: 9H03280012
Quanta suggested 20ppm/12.5pF
PCH_RTC_X2
PCH_RTC_X1
X2 32.768KHZ/20ppm/12.5pF
9H03200031
R45 1M_1%_2
C2 18p/25V_2
C3 18p/25V_2
TXC/9H03200031
2nd source:
EPSON/FC-135

SEL BOM: CS325-19.200MABJ-UT
Quanta suggested 20ppm/12pF
PCH_OSCOUT
PCH_OSCIN
X3 19.2MHZ/20ppm1/12pF
7V19200001
R722 200K_1%_2
C1 15p/25V_2
C4 15p/25V_2
TXC/7V19200001
2nd source:
Hosonic/E3FB19E0X0008E
Interquip/5YEA19200122SF50Q2

PP3300_A

R190 100K_1%_2
R191 1K_1%_2
R120Q *100K_1%_2
C120Q *1u/6.3V_2
PLT_RST_L
PCH_SLP_S3_L → Q56 PJE138K → SLP_S3 → Q57 PJE138K
0109_Q_added DNS resistor/cap on PLT_RST_L for potential issue

PCH_RSMRST_L
R587 100K_1%_2

PP3300_A
R508 499K_1%_2
PCH_RSMRST_OD
PCH_RSMRST_L → Q80 PJE138K
C447 *1u/6.3V_2

CHECK RTCRST SIGNAL

PP3300_RTC
R50 20K_1%_2
PCH_RTCRST_ODL
EC_PCH_RTCRST → Q7 PJE138K
C5 1u/25V_4

CHECK RTCRST SIGNAL

PP3300_RTC
R740 20K_1%_2
PCH_RTEST_ODL
(18) EC_PCH_RTCRST → EC_PCH_RTCRST
R739 100K_1%_2
Q86 PJE138K
C582 1u/25V_4

PCH_RSMRST_OD
PCH_SLP_S0_L → Q79 PMZB670UPE → SLP_S0_L → SLP_S0_L (18)
R516 *0_5%_2
R507 499K_1%_2

PCH_RSMRST_OD
PCH_SLP_S3_L → Q81 PMZB670UPE → SLP_S3_L → SLP_S3_L (18,35)
R517 *0_5%_2
R509 499K_1%_2

PCH_RSMRST_OD
PCH_SLP_S4_L → Q82 PMZB670UPE → SLP_S4_L → SLP_S4_L (18,35)
R518 *0_5%_2
R510 499K_1%_2

Quanta Computer Inc.
PROJECT : ZBA/ZBB

Size	Document Number	Rev
	SOC PMU/RTC/SVID/THERMAL/MISC	1A

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LAYOUT NOTE: PLACE THE R62, 65, 55, 57, R393 WITHIN 1" OF J5 MIPI60 CONNECTOR.

(CPU)

PP1800_SOC_A

R65 51_1%_2 R393 150_1%_2 R62 51_1%_2

TP_GPIO5

(20) TCK (20) TDI (20) TDO (20) TMS (20) TRST_L

R57 *51_1%_2 R55 51_1%_2

PP1800_SOC_A

R397 150_1%_2 R394 51_1%_2

(20) CX_PRDY_L (20) CX_PREQ_L

U4H

JTAG

AH53 AM53 AJ54 AL53 AL54 AK53 — JTAGX JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TRST

AH55 AJ53 — JTAG_PRDY JTAG_PREQ

1.8V

ITP

PP1800_A PP3300_A

R380 *4.7K_5%_2 R391 1K_5%_2 R392 1K_5%_2

R391,R392,R341,R352 can't be un-stuffed in MP even if removing debugging related stuffs from MP

(10) GPIO_81_DEBUG R340 1K_5%_2 BOOT_HALT_L (20)

(11,18,21,22) SYS_RST_ODL R341 *Short_0201 DBG_PMU_RSTBTN_L (20)

(11,18) EC_PCH_PWR_BTN_ODL R352 *Short_0201 DBG_PMU_PWRBTN_L (20)

(11,18,21,23,28) PLT_RST_L R361 1K_5%_2 DBG_PMU_PLTRST_L (20)

(11,18) PCH_RSMRST_L R379 *1K_5%_2 DBG_RSMRST_L (20)

GPIO

1.8V

1.8V/3.3V

1.8V

GPIO_8 GPIO_9 GPIO_10 GPIO_11 GPIO_12 GPIO_13 GPIO_14 GPIO_15 GPIO_16 — AG53 AG54 AE54 AE53 AD55 AD53 AC54 AC53 AB53 — DBG_PTI_CLK0 (20) DBG_PTI_DATA_0 (20) DBG_PTI_DATA_1 (20) DBG_PTI_DATA_2 (20) DBG_PTI_DATA_3 (20) DBG_PTI_DATA_4 (20) DBG_PTI_DATA_5 (20) DBG_PTI_DATA_6 (20) DBG_PTI_DATA_7 (20)

GPIO_17 GPIO_18 GPIO_19 GPIO_20 GPIO_21 GPIO_22 GPIO_23 GPIO_24 GPIO_25 — AA49 AC48 AC46 AE51 AE49 AC51 AC49 AA51 AA46 — DBG_PTI_CLK1 (20) DBG_PTI_DATA_8 (20) DBG_PTI_DATA_9 (20) DBG_PTI_DATA_10 (20) CNVI_MFUART2_RXD_PTI_11 CNVI_MFUART2_TXD_PTI_12 CNVI_GNSS_PA_BLANKING_PTI_13 DBG_PTI_DATA_14 (20) DBG_PTI_DATA_15 (20)

GPIO_26 GPIO_27 GPIO_28 GPIO_29 GPIO_30 GPIO_31 GPIO_32 GPIO_33 GPIO_34 — AE41 AE39 AE46 AE44 AC41 AC39 AC44 AC43 AA44 — DBG_PTI_CLK2 (20) DBG_PTI_DATA_16 (20) DBG_PTI_DATA_17 (20) DBG_PTI_DATA_18 (20) DBG_PTI_DATA_19 (20) DBG_PTI_DATA_20 (20) DBG_PTI_DATA_21 (20) DBG_PTI_DATA_22 (20) DBG_PTI_DATA_23 (20)

GPIO_35 GPIO_36 GPIO_37 GPIO_38 GPIO_39 GPIO_40 GPIO_41 — AA54 AA53 Y55 Y53 W54 W53 V53 — DCI_CLK_PTICLK3 (20) DCI_DATA_PTITRACE3_0 (20) DBG_PTI_DATA_TRACE3_1 (20) DBG_PTI_DATA_TRACE3_2 (20) DBG_PTI_DATA_TRACE3_3 DBG_PTI_DATA_TRACE3_4 DBG_PTI_DATA_TRACE3_5

GPIO_105 GPIO_134 GPIO_135 GPIO_136 GPIO_137 GPIO_138 GPIO_139 GPIO_140 GPIO_141 GPIO_142 GPIO_143 GPIO_144 GPIO_145 GPIO_146 GPIO_210 GPIO_212 GPIO_213 GPIO_214 — L46 H45 H47 L43 M43 H37 H43 J43 D43 F43 H41 F39 L41 F41 R27 U43 U41 U39 — EC_AP_INT_ODL TRACKPAD_INT1_1V8_ODL PMIC_PCH_INT_1V8_ODL EC_PCH_WAKE_1V8_ODL TRACKPAD_INT2_1V8_ODL PEN_EJECT PEN_EJECT TP_GPIO210 TP_AP_GPIO213

TOUCHSCREEN_RST (26) TP65 EC_AP_INT_ODL (18)

C85Q *10p/25V_2

HP_INT_ODL (24) PEN_PDCT_ODL (25) PEN_INT_ODL (25) PEN_RESET (25)

PP1800_SOC_A

LTE_SAR_ODL (38) TP49 TP74 R558 *Short_0201 TP68 TP172 TP69

R289 100K_5%_2 PEN_EJECT (25)

EN_PP3300_TOUCHSCREEN (25,35) EN_PP3300_CAMERA (35) TOUCHSCREEN_INT_ODL (26) P_SENSOR_INT_L (38)

1226_Q_made R289 stuffed for no matter internal PU is available or not

PEN_EJECT C86Q *10p/25V_2

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PP1800_SOC_A

DBG_PTI_DATA_16 R362 1K_5%_2 R28973 20K_1%_2 EC_AP_INT_ODL

(18,25) TRACKPAD_INT_1V8_ODL TRACKPAD_INT_1V8_ODL R524 *Short_0201 TRACKPAD_INT1_1V8_ODL R531 *Short_0201 TRACKPAD_INT2_1V8_ODL

0102_Q_Changed R531 to a short pad

CNVI_GNSS_PA_BLANKING_PTI_13 R14 *Short_0201 R16 *0_5%_2 CNVI_GNSS_PA_BLANKING (28) DBG_PTI_DATA_13 (20)

(PMC)

PP1800_SOC_A

R880 10K_2

PMIC_PCH_INT_1V8_ODL R887 *Short_0201 PMIC_PCH_INT_ODL (33)

CNVI_MFUART2_RXD_PTI_11 R17 *Short_0201 R24 *0_5%_2 CNVI_MFUART2_RXD (28) DBG_PTI_DATA_11 (20)

CNVI_MFUART2_TXD_PTI_12 R25 *Short_0201 R61 *0_5%_2 CNVI_MFUART2_TXD (28) DBG_PTI_DATA_12 (20)

(CPU)

PP1800_SOC_A

R881 *10K_2

EC_PCH_WAKE_1V8_ODL R888 *Short_0201 EC_PCH_WAKE_ODL (18)

R380 is reserved for strapping high (GPIO_81)

R877 is for strapping low to not allow eMMC as a boot source (GPIO_27)

No extermal PU/PD on GPIO_28, using internal PD for allowing SPI as a boot source

Quanta Computer Inc.

PROJECT : ZBA/ZBB

Size	Document Number	Rev
	SOC JTAG/GPIO/ITP	1A

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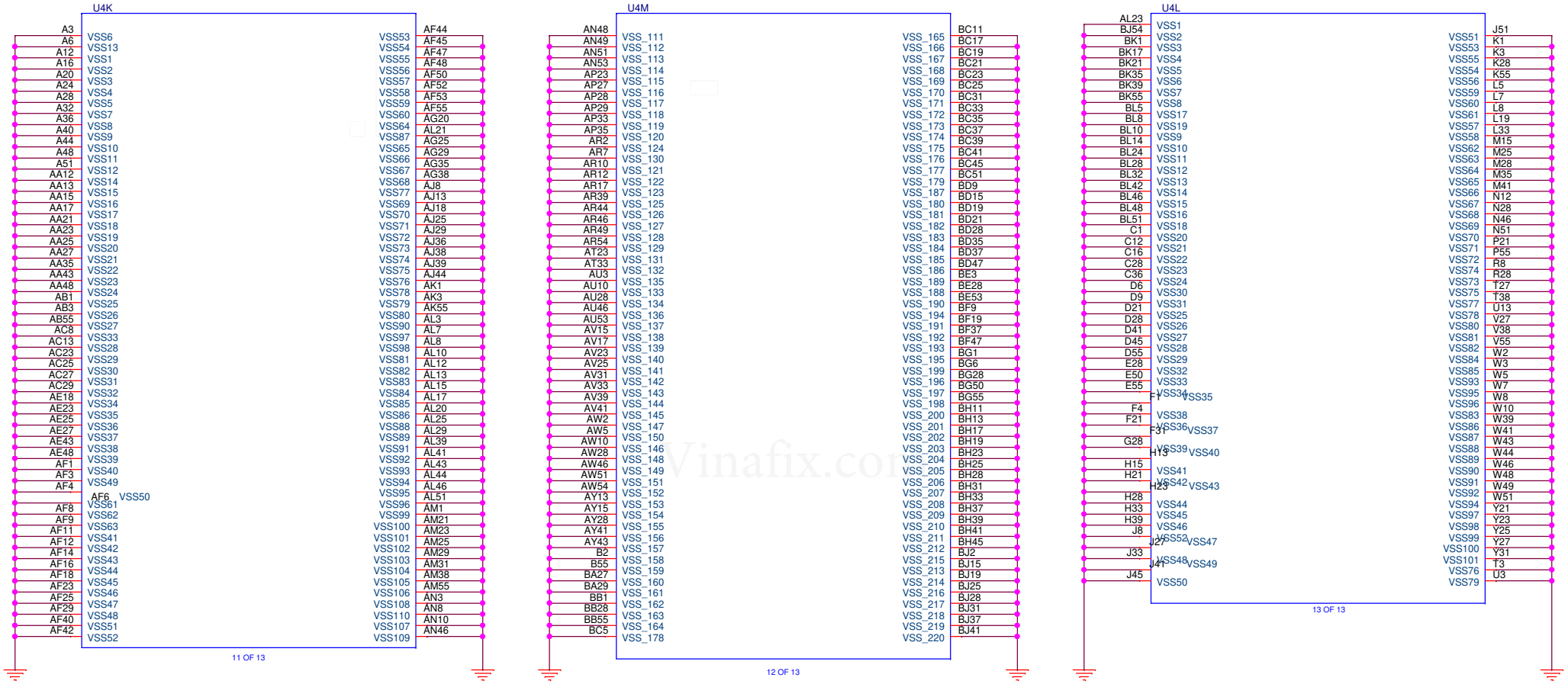
GLK ULT (GND)

(CPU)



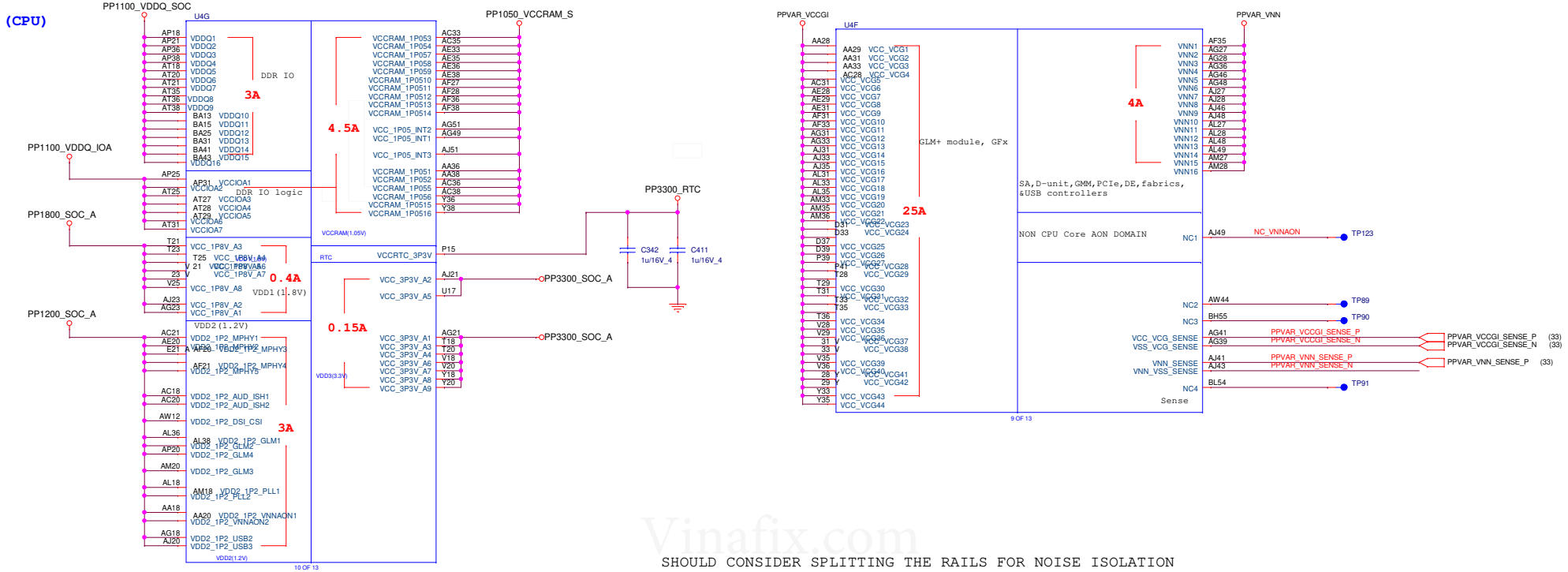
Quanta Computer Inc.

PROJECT : ZBA/ZBB

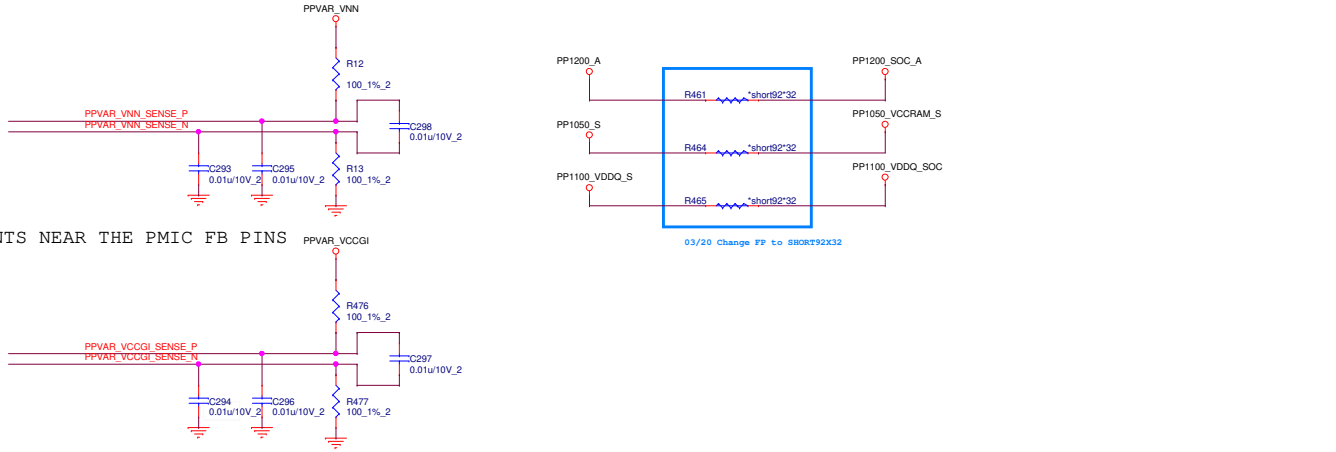
Size	Document Number	Rev
	SOC GROUND	1A
Date: Friday, May 31, 2019	Sheet 13 of 45	

SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION

Gemini (POWER)



SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION



PLEASE THESE COMPONENTS NEAR THE PMIC FB PINS

Quanta Computer Inc.		
PROJECT : ZBA/ZBB		
Size	Document Number: SOC POWER	Rev: 1A
Date: Friday, May 31, 2019	Sheet 14 of 45	

(CPU)

PPVAR_VNN

DECOUPLING VALUES AND NUMBER BASED ON THE REFERENCE DOC

C28 1u/6.3V_4 C37 1u/6.3V_4 C46 1u/6.3V_4 C129 1u/6.3V_4 C29 1u/6.3V_4 C83 22u/6.3V_6 C38 22u/6.3V_6 C47 22u/6.3V_6 C51 22u/6.3V_6

PPVAR_VNN: 5 X 1UF_0402_6.3V, 4 X 22UF_0603_6.3V

PPVAR_VNN

C277 1u/6.3V_4

PPVAR_VCCGI

C6 1u/6.3V_4 C10 1u/6.3V_4 C95 1u/6.3V_4 C101 1u/6.3V_4 C105 1u/6.3V_4 C130 1u/6.3V_4 C156 1u/6.3V_4 C199 22u/6.3V_6 C200 22u/6.3V_6 C201 22u/6.3V_6 C204 22u/6.3V_6

PPVAR_VCCGI: 12 X 1UF_0402_6.3V, 8 X 22UF_0603_6.3V, 2 X 0.1UF_0402_16V

PPVAR_VCCGI

C9 1u/6.3V_4 C94 1u/6.3V_4 C99 1u/6.3V_4 C104 1u/6.3V_4 C115 1u/6.3V_4 C155 22u/6.3V_6

PPVAR_VCCGI

C203 22u/6.3V_6 C205 22u/6.3V_6 C206 22u/6.3V_6

PPVAR_VCCGI

C207 0.1u/16V_4 C278 0.1u/16V_4

PP1050_VCCRAM_S: 1uF_0402x10 , 22uF_0603 x3

PP1050_VCCRAM_S

C79 1u/6.3V_4 C84 1u/6.3V_4

PP1050_VCCRAM_S

C33 1u/6.3V_4 C42 1u/6.3V_4

PP1050_VCCRAM_S

C80 1u/6.3V_4 C85 1u/6.3V_4 C419 1u/6.3V_4 C88 22u/6.3V_6

PP1050_VCCRAM_S

C34 1u/6.3V_4 C43 1u/6.3V_4 C437 1u/6.3V_4 C57 22u/6.3V_6 C61 22u/6.3V_6

PP1200_SOC_A

C144 22u/6.3V_6

PP1200_SOC_A

C440 1u/6.3V_4 C493 1u/6.3V_4 C496 22u/6.3V_6

PP1200_SOC_A

C441 1u/6.3V_4 C494 1u/6.3V_4 C497 22u/6.3V_6 C499 22u/6.3V_6

PP1200_SOC_A

C89 1u/6.3V_4

PP1200_SOC_A

C438 1u/6.3V_4 C465 1u/6.3V_4 C495 1u/6.3V_4 C498 1u/6.3V_4 C500 22u/6.3V_6 C501 22u/6.3V_6 C502 22u/6.3V_6

PP1200_SOC_A: 1uF_0402x9 , 22uF_0603 x7

PP1100_VDDQ_SOC

C31 1u/6.3V_4 C40 1u/6.3V_4

PP1100_VDDQ_SOC

EDGE CAP FOR EXPOSED POWER PLANES

C322 0.1u/16V_4 C327 0.1u/16V_4 C334 0.1u/16V_4 C335 0.1u/16V_4

PP1100_VDDQ_SOC

C30 1u/6.3V_4 C39 1u/6.3V_4 C52 22u/6.3V_6 C56 22u/6.3V_6

PP1100_VDDQ_SOC

C60 22u/6.3V_6 C64 22u/6.3V_6 C67 22u/6.3V_6 C69 22u/6.3V_6 C332 1u/6.3V_4 C333 1u/6.3V_4

PP1100_VDDQ_S PP1100_VDDQ_IOA

W1 *short92*32

03/20 Change FP to SHORT92X32

C288 1u/6.3V_4 C289 1u/6.3V_4 C291 1u/6.3V_4 C304 22u/6.3V_6 C313 22u/6.3V_6 C319 22u/6.3V_6

VDDQI: 1uF_0402x8 , 22uF_0603 x10 , 0.1uF_0402x4

PP1800_SOC_A: 1uF_0402x4 , 22uF_0603 x1

PP1800_SOC_A

C97 1u/6.3V_4 C100 1u/6.3V_4 C98 1u/6.3V_4 C102 1u/6.3V_4 C106 22u/6.3V_6

PP3300_SOC_A

C414 1u/6.3V_4 C416 1u/6.3V_4 C417 1u/6.3V_4 C418 1u/6.3V_4 C432 22u/6.3V_6

PP3300_SOC_A

C90 1u/6.3V_4

PP3300_SOC_A: 1uF_0402x8 , 22uF_0603 x2

PP3300_SOC_A

C91 1u/6.3V_4 C92 1u/6.3V_4 C103 22u/6.3V_6

PP3300_SOC_A

C107 1u/6.3V_4

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PROJECT : ZBA/ZBB

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	SOC DECOUPLING	1A
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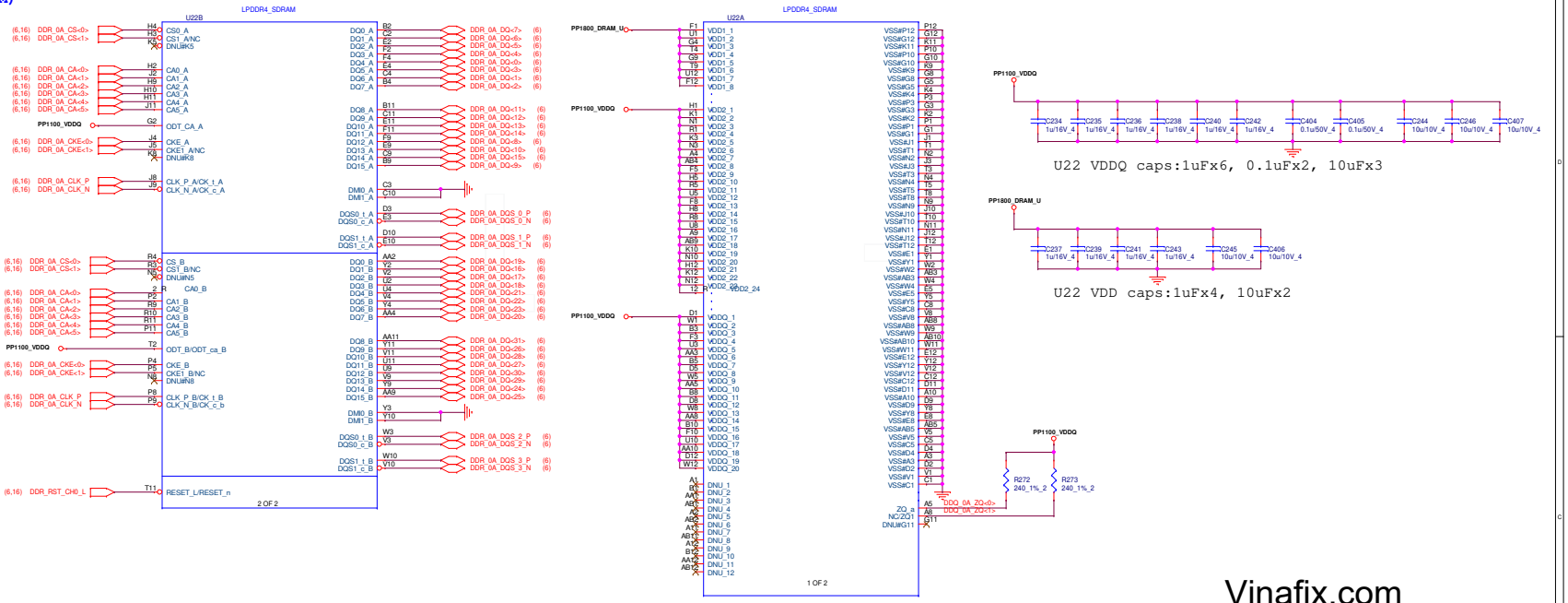
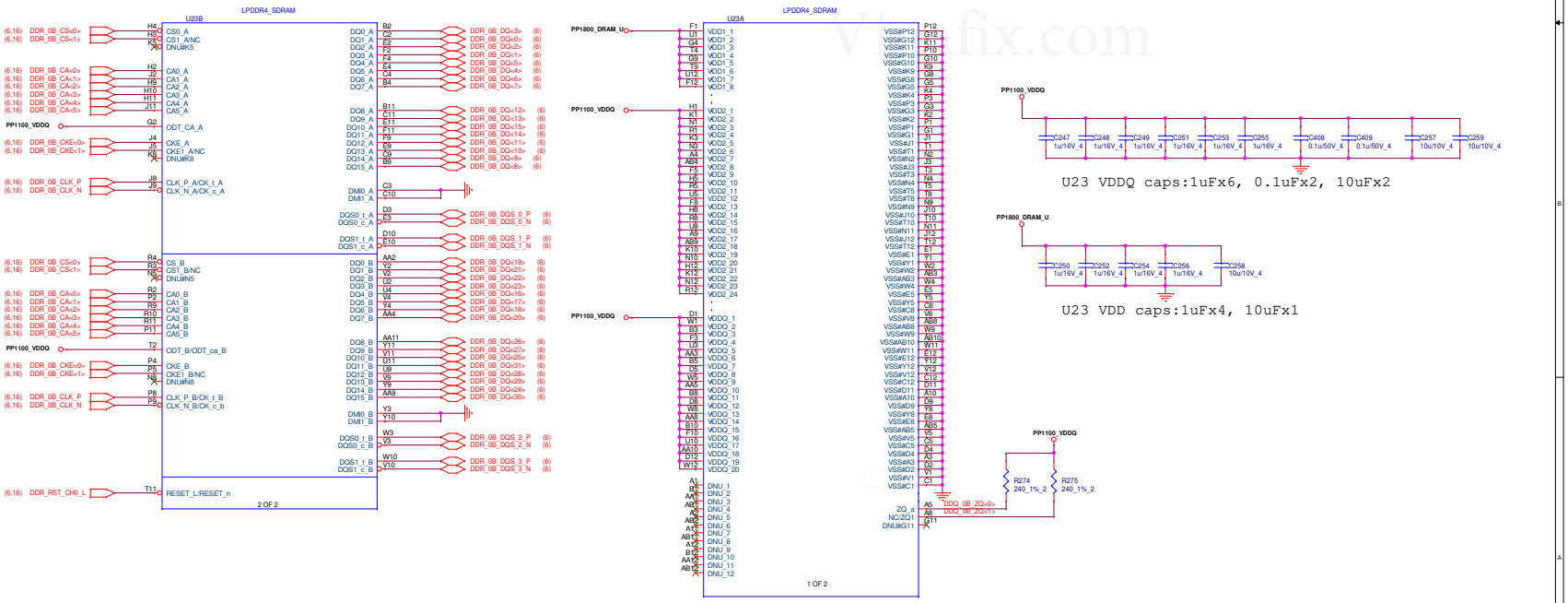
(OBM)





Quanta Computer Inc.			
PROJECT : ZBA/ZBB			
Size	Document Number		Rev
	MEMORY CH 00/01 LPDDR4		1A
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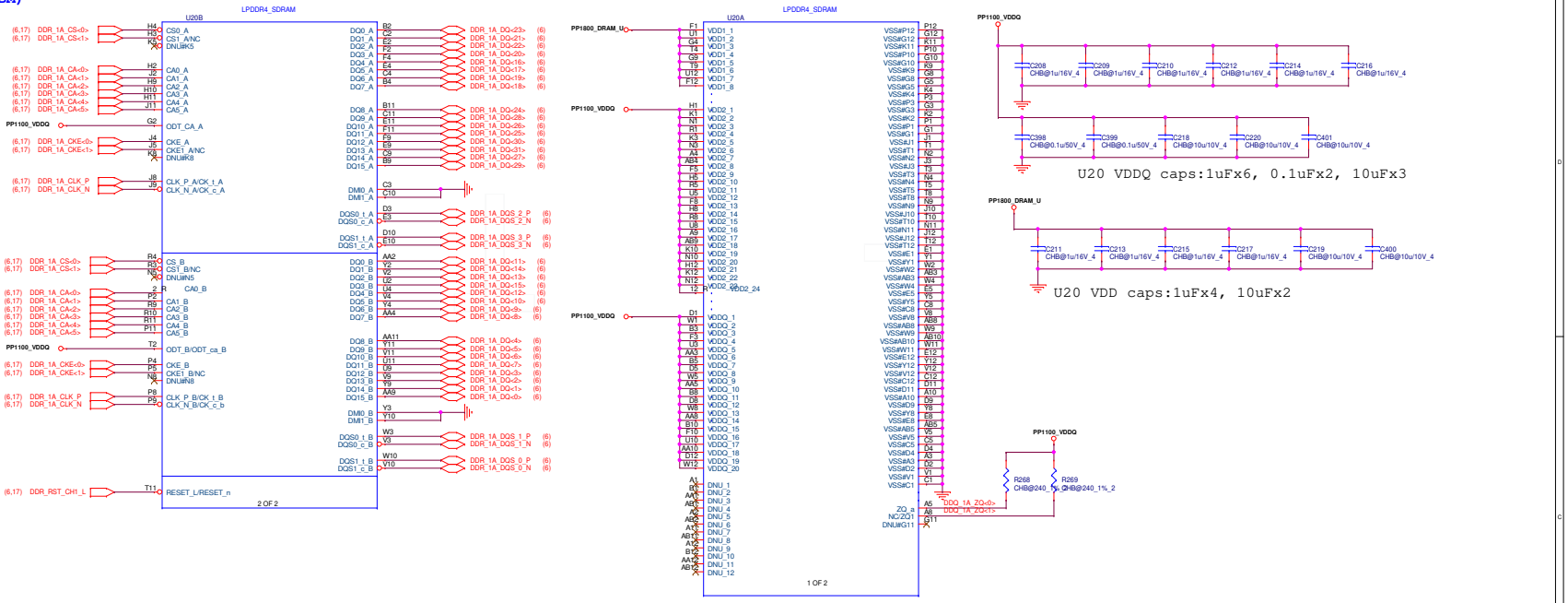
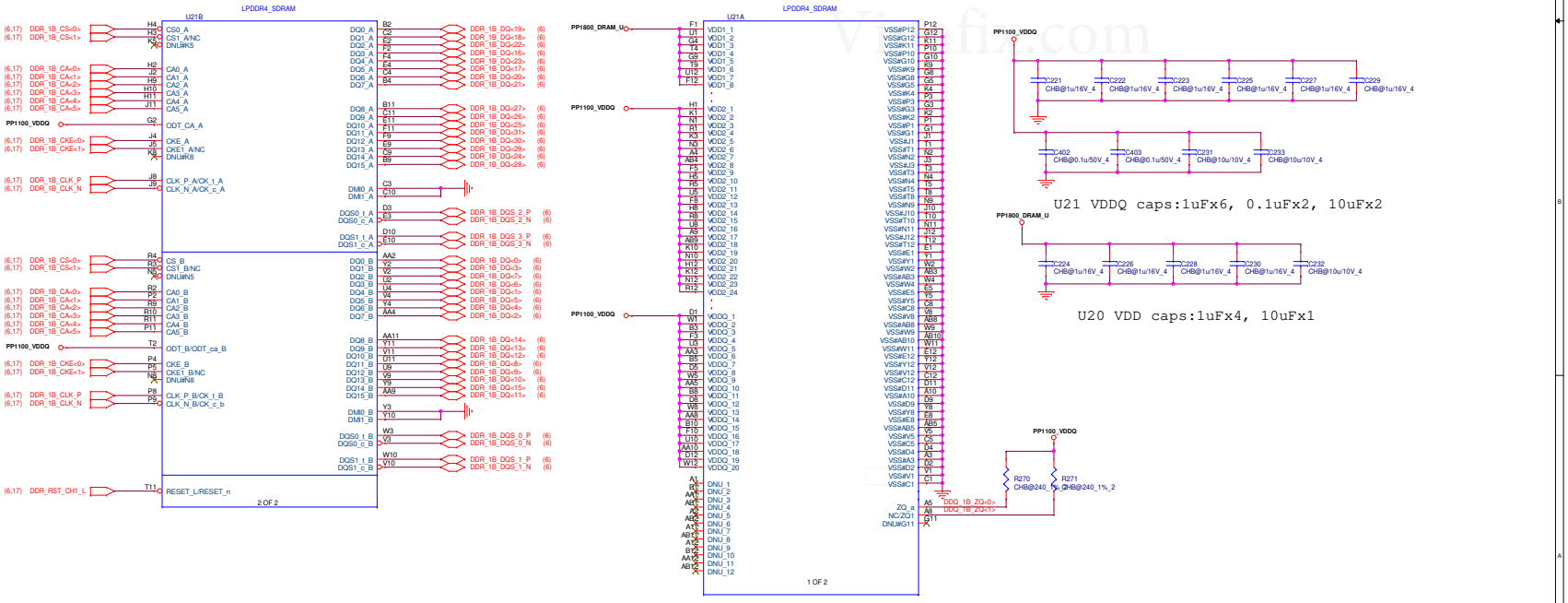
(OBM)





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PROJECT : ZBA/ZBB

Size	Document Number	Rev
	MEMORY CH 10/11 LPDDR4	1A

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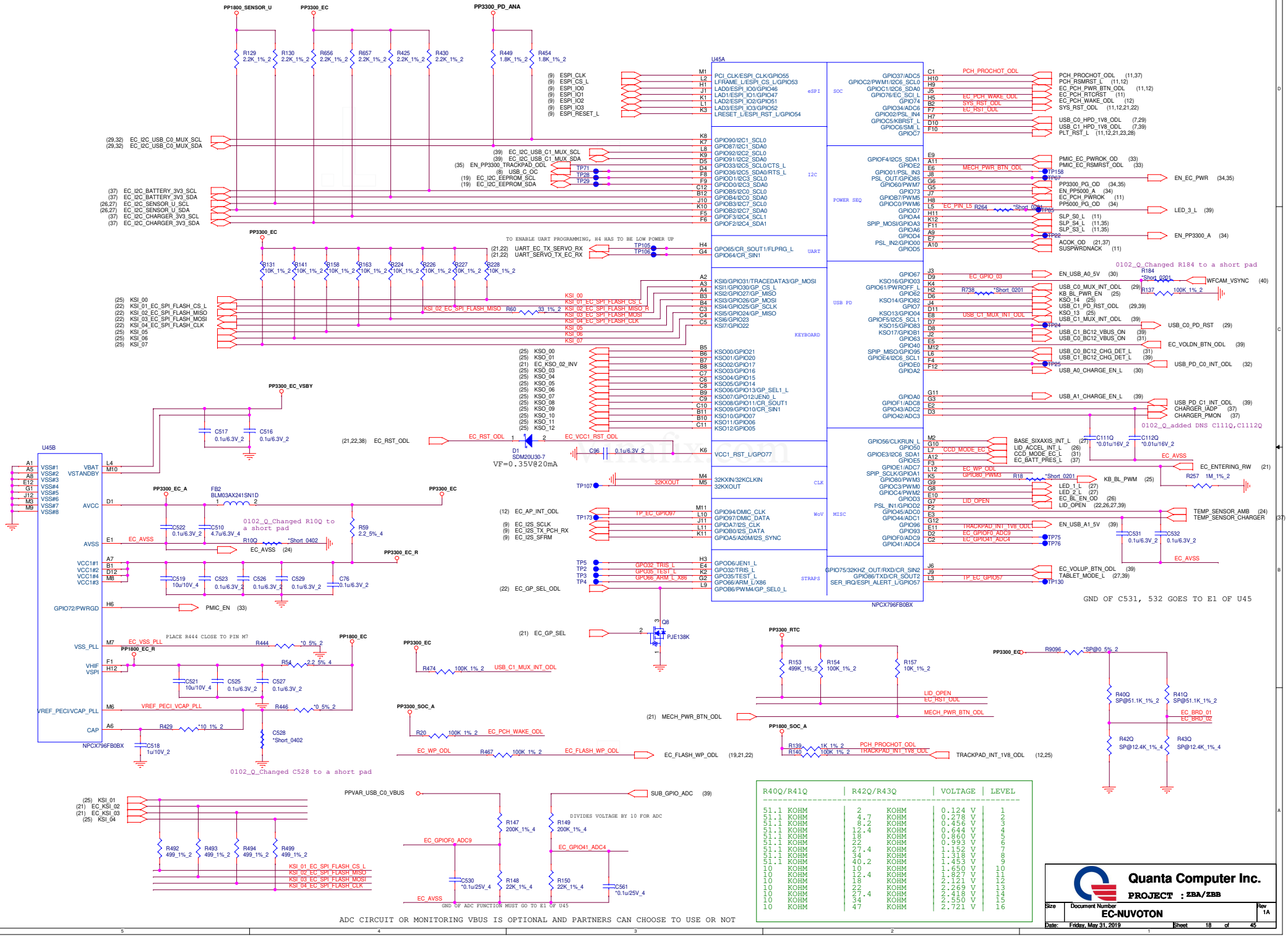
(KBC)


U45A
NPCX796FB0BX
U45B
NPCX796FB0BX
PP1800_SENSOR_U
PP3300_EC
PP3300_PD_ANA
PP3300_EC_VSBY
PP3300_EC_A
PP3300_EC_R
PP1800_EC
PP1800_EC_R
PP3300_RTC
PP1800_SOC_A
PP3300_SOC_A
PP3300_EC_VSBY
TO ENABLE UART PROGRAMMING, H4 HAS TO BE LOW POWER UP
0102_Q_Changed R184 to a short pad
0102_Q_added DNS C111Q,C1112Q
0102_Q_Changed R10Q to a short pad
0102_Q_Changed C528 to a short pad
GND OF C531, 532 GOES TO E1 OF U45
PLACE R444 CLOSE TO PIN M7
VF=0.35V@20mA
DIVIDES VOLTAGE BY 10 FOR ADC
GND OF ADC FUNCTION MUST GO TO E1 OF U45
ADC CIRCUIT OR MONITORING VBUS IS OPTIONAL AND PARTNERS CAN CHOOSE TO USE OR NOT
R40Q/R41Q | R42Q/R43Q | VOLTAGE | LEVEL
51.1 KOHM | 2 KOHM | 0.124 V | 1
51.1 KOHM | 4.7 KOHM | 0.278 V | 2
51.1 KOHM | 8.2 KOHM | 0.456 V | 3
51.1 KOHM | 12.4 KOHM | 0.644 V | 4
51.1 KOHM | 18 KOHM | 0.860 V | 5
51.1 KOHM | 22 KOHM | 0.993 V | 6
51.1 KOHM | 27.4 KOHM | 1.152 V | 7
51.1 KOHM | 34 KOHM | 1.318 V | 8
51.1 KOHM | 40.2 KOHM | 1.453 V | 9
10 KOHM | 10 KOHM | 1.650 V | 10
10 KOHM | 12.4 KOHM | 1.827 V | 11
10 KOHM | 18 KOHM | 2.121 V | 12
10 KOHM | 22 KOHM | 2.269 V | 13
10 KOHM | 27.4 KOHM | 2.418 V | 14
10 KOHM | 34 KOHM | 2.550 V | 15
10 KOHM | 47 KOHM | 2.721 V | 16
Quanta Computer Inc.
PROJECT : ZBA/ZBB
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EC-NUVOTON
Rev 1A
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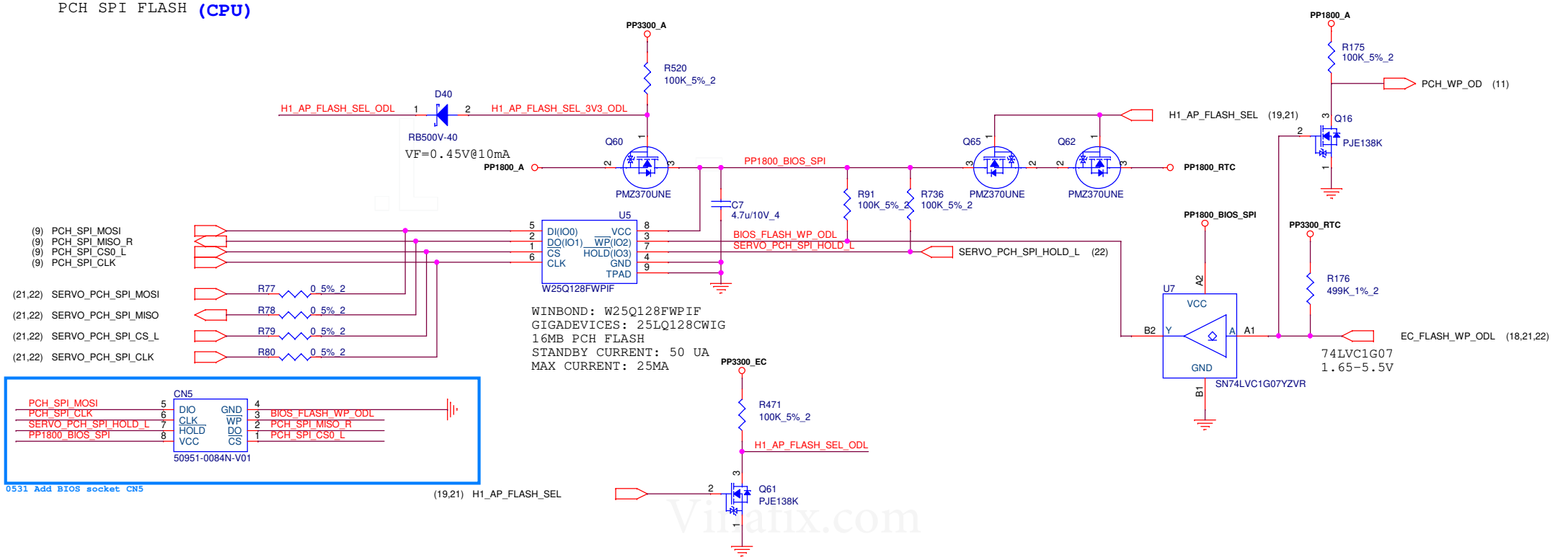
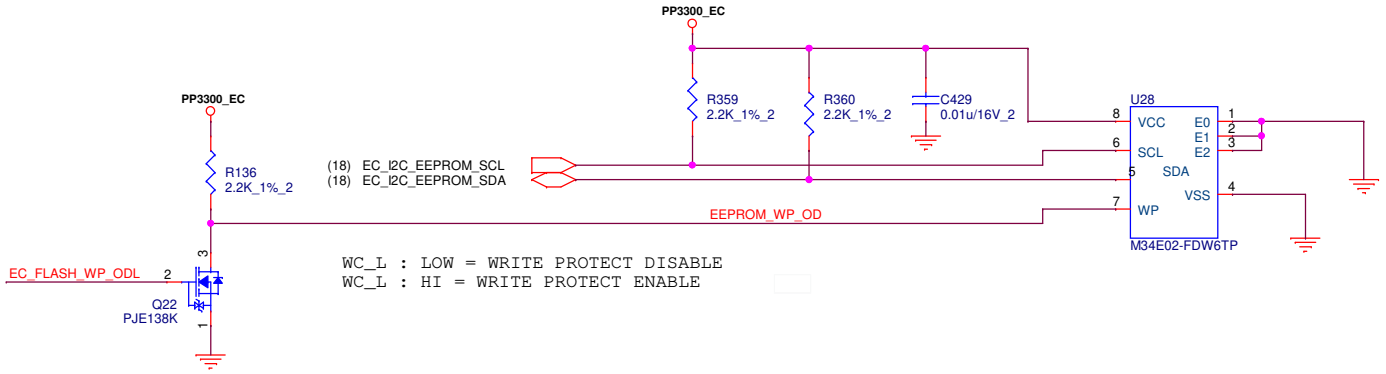
PCH SPI FLASH (CPU)



(KBC)

SKU EEPROM



Quanta Computer Inc.

PROJECT : ZBA/ZBB

Size	Document Number	Rev
	SPI ROM	1A
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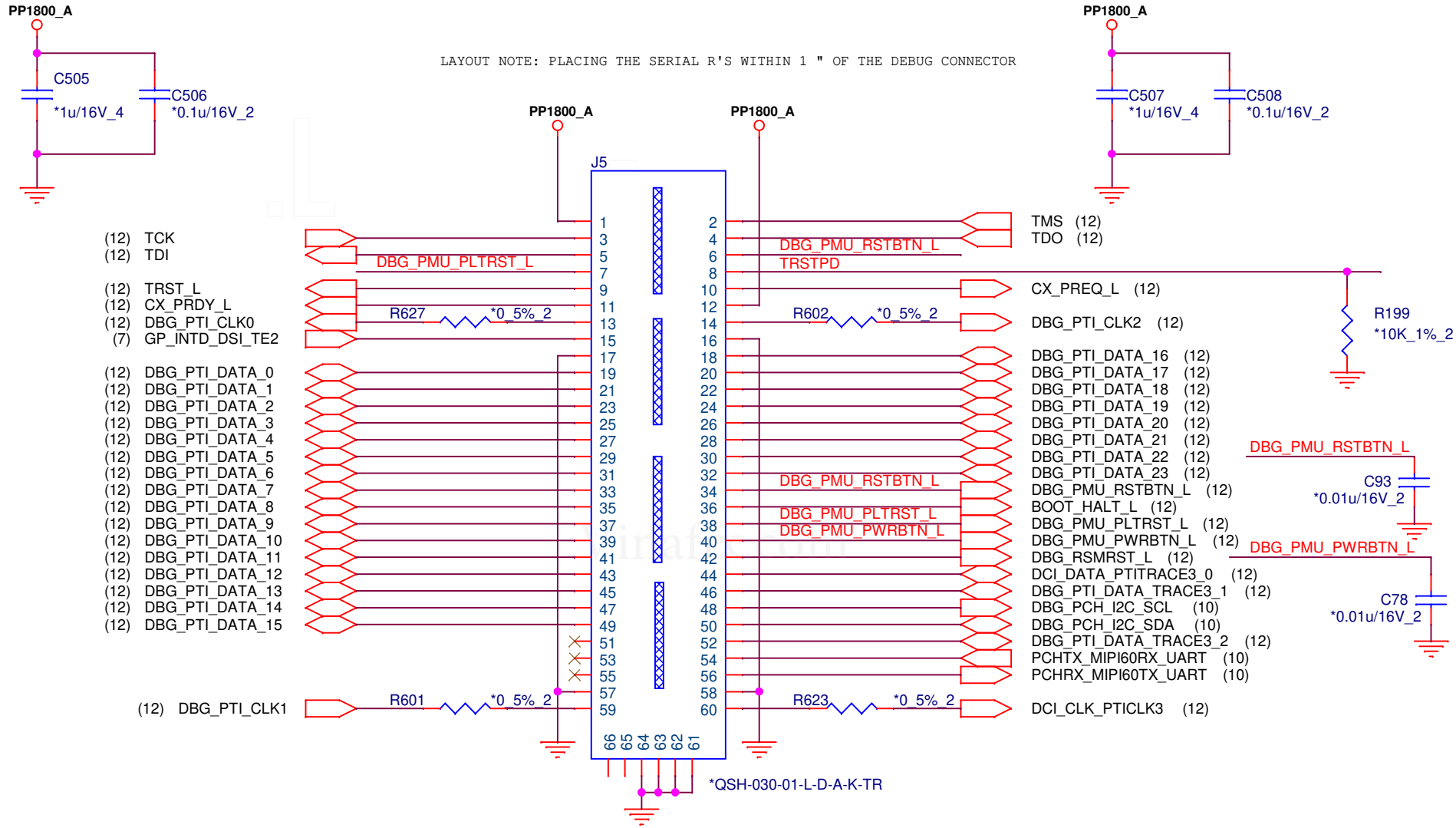
(INT)



Quanta Computer Inc.		
PROJECT : ZBA/ZBB		
Size	Document Number: MIPI60 DEBUG HEADER	Rev: 1A
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(H1C)

KEEP NEAR TPM/SPI ROM TO MINIMIZE SPI STUBS
PLACE TERMINATION NEAR DIVIDE

(10) H1_SLAVE_SPI_MOSI_R — R782 33_5% 2 — H1_SLAVE_SPI_MOSI
(10) H1_SLAVE_SPI_CLK_R — R792 33_5% 2 — H1_SLAVE_SPI_CLK
(10) H1_SLAVE_SPI_CS_L_R — R793 33_5% 2 — H1_SLAVE_SPI_CS_L
(10) H1_SLAVE_SPI_MISO — R794 33_5% 2 — H1_SLAVE_SPI_MISO_R

PP3300_RTC — R813 *Short_0603 — PP3300_VDDIOM
R450 *Short_0603 — PP3300_VDDIOB
PP1800_RTC — R451 *Short_0603 — C386 0.1u/10V_2 — PP1800_VDDIOA
PP3300_VDDIOM — R857 30.9K_1%_2 — C439 0.1u/10V_2
ADDED TO MATCH 3MS DELAY
C382 0.1u/10V_2
C378 4.7u/6.3V_4 — C387 0.1u/10V_2 — C388 0.1u/10V_2 — C389 0.1u/10V_2

PP3300_VDDIOM
1226_Q_added 499K PU to PP3300_VDDIOM on H1_BATT_PRES_L as in 2.82 change list
R90Q 499K_1%_2

PP1800_SOC_A — R443 10K_5%_2 — D33 SDM20U30-7 — VF=0.35V@20mA — (10) H1_PCH_INT_ODL
PP1800_VDDIOA — R445 10K_5%_2 — R501 10K_5%_2

U37 RESETB

(22) RESET_H1_ODL — G1
(22) H1_BOOT_UART_TX — TP60 — R334 *0_5%_2 — DIOA1 — B9
(10) PCH_I2C_H1_SDA — H1_SLAVE_SPI_MOSI — D8
(10,22) PCHTX_SERVORX_UART — H1_SPI_MOSI — C9
H1_PCH_INT_L — E8
H1_SLAVE_SPI_CLK — D9
(10,22) PCHRX_SERVOTX_UART — H1_SPI_CLK — F8
(10) PCH_I2C_H1_SCL — R335 *0_5%_2 — DIOA9 — F9
H1_SLAVE_SPI_MISO_R — G8
H1_SPI_MISO — H8
H1_SLAVE_SPI_CS_L — H9
H1_BOOT_UART_RX — J9
H1_SPI_CS_L — J8
(22) H1_BOOT_UART_RX — TP58 — H7
J7

DIOA0 DIOA1 DIOA2 DIOA3 DIOA4 DIOA5 DIOA6 DIOA7 DIOA8 DIOA9 DIOA10 DIOA11 DIOA12 DIOA13 DIOA14 — 1.8V

(22,36) DEBUG_I2C_SCL — J6
(22,36) DEBUG_I2C_SDA — H6
EC_GP_SEL — J5
H1_AP_FLASH_SEL — H5
H1_BOOT_CONFIG — J3
(18,22) UART_SERVO_TX_EC_RX — H4
(18,22) UART_EC_TX_SERVO_RX — J2
(36) EN_PP3300_INA_H1_ODL — J1

DIOB0 DIOB1 DIOB2 DIOB3 DIOB4 DIOB5 DIOB6 DIOB7 — 3.3V

(18) EC_GP_SEL
(19) H1_AP_FLASH_SEL
(22) H1_BOOT_CONFIG
R472 10K_5%_2 — R473 10K_5%_2 — R203 10K_5%_2

DIOB4 - GND, BUT HAD INTERNAL PD - TIE MAY NOT BE NECESSARY

R304 *0_5%_2 — E1
R308 *0_5%_2 — F1
USBAN USBAP
(31) USB_C0_SBU1 — R855 *Short_0201 — H1_USB_C0_SBU1
(31) USB_C0_SBU2 — R856 *Short_0201 — H1_USB_C0_SBU2
R310 *Short_0201 — E2
R306 *Short_0201 — F2
USBBN USBBP

0102_Q_Changed R306,R310 to a short pad

R169 2M_1%_2 — R204 2M_1%_2 — R172 2M_1%_2 — R178 2M_1%_2

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11

UR0605B-FT021

DIOM0 DIOM1 DIOM2 DIOM3 DIOM4 — 1.8V

C1 DIOM0 — R873 *Short_0201 — SYS_RST_ODL (11,12,18,22)
B1 DIOM1 — R874 *Short_0201 — CCD_MODE_ODL (31)
A1 DIOM2 — R875 *Short_0201 — H1_BATT_PRES_L (37)
A2 DIOM3 — R876 *Short_0201 — PLT_RST_L (11,12,18,23,28)
A3 DIOM4

PP3300_VDDIOM — R561 10K_5%_2

DIOR0 DIOR1 DIOR2 DIOR3 DIOR4 DIOR5 DIOR6 DIOR7 DIOR8 DIOR9 DIOR10 DIOR11

B3 — EC_RST_ODL (18,22,38)
A4 — MECH_PWR_BTN_IN_ODL (22,25)
B4 DIOR2
A5
B5 — EC_KSO_02_INV (18)
A6 — EC_ENTERING_RW (18)
ACOK_OD
B6 — R999 1K_1%_2 — EC_FLASH_WP_ODL (18,19,22)
B7 — MECH_PWR_BTN_ODL (18)
A8 DIOR8
B8 — KSO_02 (25)
A9 — EC_IN_RW_OD
C8 — BAT_DISABLE_ODL (37)

PP3300_VDDIOM — R529 100K_1%_2 — PP1800_SOC_A — R448 100K_5%_2
ACOK_OD (18,37)
EC_IN_RW_OD (11)

RDCC1 RDCC2
D1 H1_RDCC1 — R859 *0_5%_2 — USB_C0_CC1 — USB_C0_CC1 (29,31)
D2 H1_RDCC2 — R860 *0_5%_2 — USB_C0_CC2 — USB_C0_CC2 (29,31)

NC#1 NC#2 NC#3 NC#4 NC#5 NC#6 NC#7 NC#8 NC#9 NC#10 NC#11 NC#12 NC#13 NC#14 NC#15

PP5000_LDO — C577 0.1u/10V_2

U8 TLV8802DGKR
VDD — OUT2 — OUT1 — VSS — IN2_N — IN2_P — IN1_N — IN1_P
R718 10K_1%_2 — OP_OUT2 — 6 OP_OUT2 — 5 R720 100K_1%_2 — USB_C0_CC2
R719 10K_1%_2 — OP_OUT1 — 2 OP_OUT1 — 3 R721 100K_1%_2 — USB_C0_CC1

FOR EC FLASH PROGRAMMING

H1_SPI_CS_L — R417 33_5%_2 — SERVO_PCH_SPI_CS_L
H1_SPI_MISO — R409 33_5%_2 — SERVO_PCH_SPI_MISO
H1_SPI_MOSI — R410 33_5%_2 — SERVO_PCH_SPI_MOSI
H1_SPI_CLK — R413 33_5%_2 — SERVO_PCH_SPI_CLK

PP1800_VDDIOA — C445 *0.1u/10V_2 — U56 *SN74LVC126ARGYRG4

H1_AP_FLASH_SEL — 1OE
H1_SPI_CS_L — 1A — 1Y — 3 — SERVO_PCH_SPI_CS_L — SERVO_PCH_SPI_CS_L (19,22)
2OE
H1_SPI_MOSI — 2A — 2Y — 6 — SERVO_PCH_SPI_MOSI — SERVO_PCH_SPI_MOSI (19,22)
3OE
H1_SPI_CLK — 3A — 3Y — 8 — SERVO_PCH_SPI_CLK — SERVO_PCH_SPI_CLK (19,22)
4OE
(19,22) SERVO_PCH_SPI_MISO — 4A — 4Y — 11 — H1_SPI_MISO
VCC VIA#1 VIA#2 VIA#3 VIA#4 OE_O GND

stuffing option for different KB

DIOR2 — R565 0_5%_2 — KSI_02 — KSI_02 (25)
R566 *0_5%_2 — KSI_03 — KSI_03 (25)
EC_KSI_03 — R5671 0_5%_2 — KSI_03
EC_KSI_02 — R567 *0_5%_2 — KSI_02
DIOR8 — R568 0_5%_2 — EC_KSI_02 — EC_KSI_02 (18)
R569 *0_5%_2 — EC_KSI_03 — EC_KSI_03 (18)

PP1800_VDDIOA
R412 *1M_1%_2 — R414 1M_1%_2 — R416 1M_1%_2 — R419 *4.7K_1%_2
H1_SLAVE_SPI_CLK
DIOA1
DIOA9
H1_SLAVE_SPI_CS_L
R162 1M_1%_2 — R165 *1M_1%_2 — R166 *1M_1%_2 — R432 1M_1%_2
STRAPS : SPI FOR CONVERTIBLE/CLAMPSHELL

Quanta Computer Inc.
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Size | Document Number: H1 SECURE MICROCONTROLLER | Rev 1A
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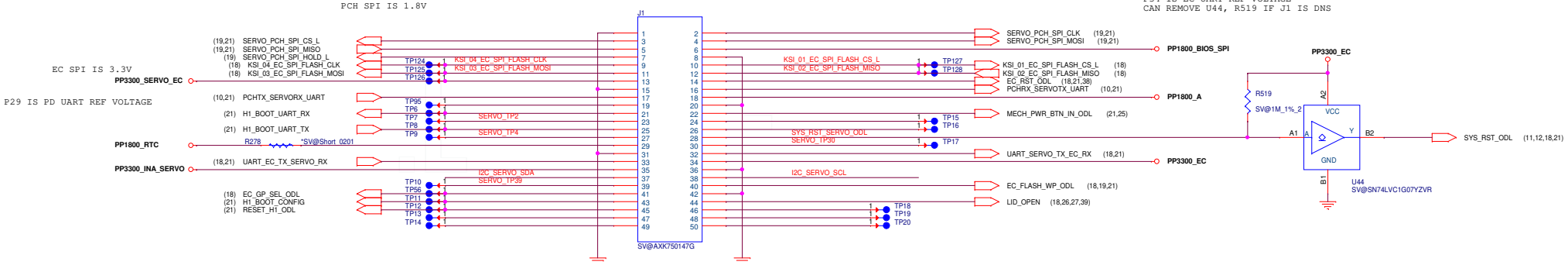
(GOG)

PCH SPI IS 1.8V

P18 IS PCH UART REF VOLTAGE
P34 IS EC UART REF VOLTAGE
CAN REMOVE U44, R519 IF J1 IS DNS

EC SPI IS 3.3V

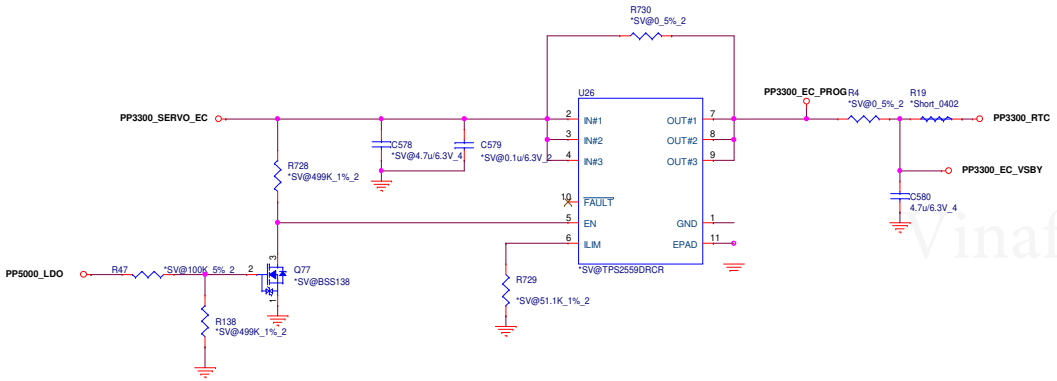
P29 IS PD UART REF VOLTAGE



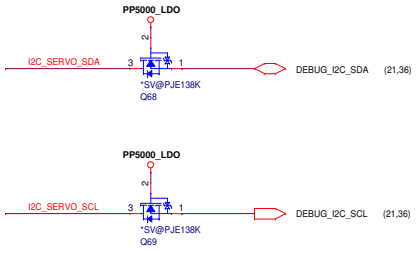
SERVO HEADER (H1C)

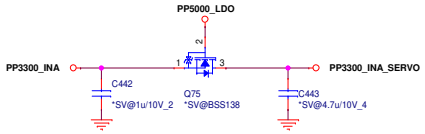
POWER FOR FLASHING EC THROUGH SERVO

CAN REMOVE U44, U26, Q77, C578, C579, R128, R47, R138 R519 IF J1 IS DNS



CAN REMOVE Q68, Q69 IF J1 IS DNS





0103_Q_DNS Q68,Q69,C442,Q75,C443 no matter servo board is stuffed or not, the INA feasrure was removed from DVT build

Quanta Computer Inc.
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Size	Document Number	Rev
	SERVO	1A
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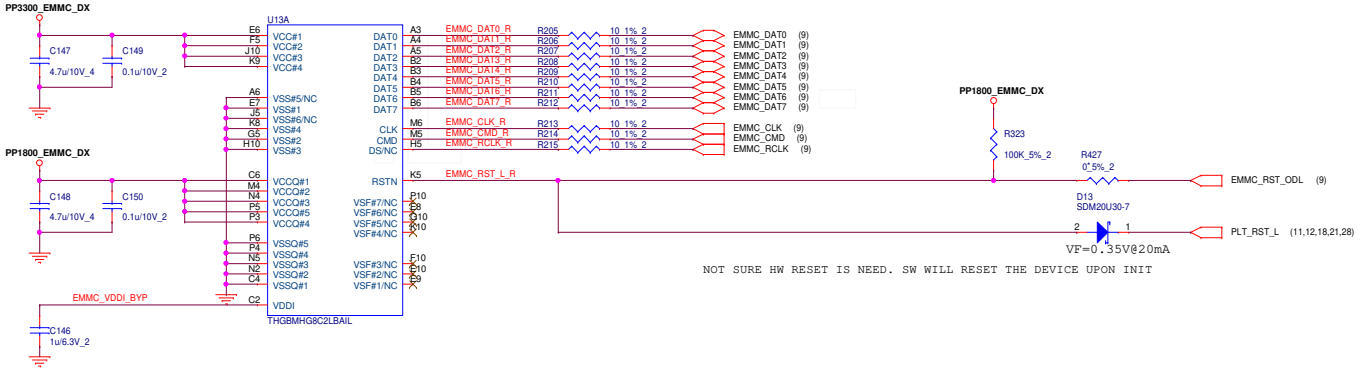
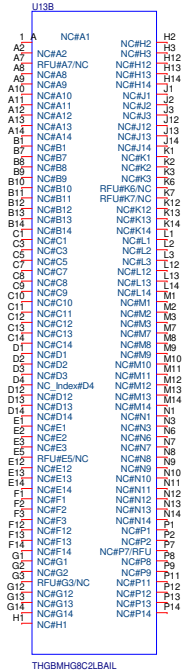
(MMC)

32 GB EMMC STORAGE

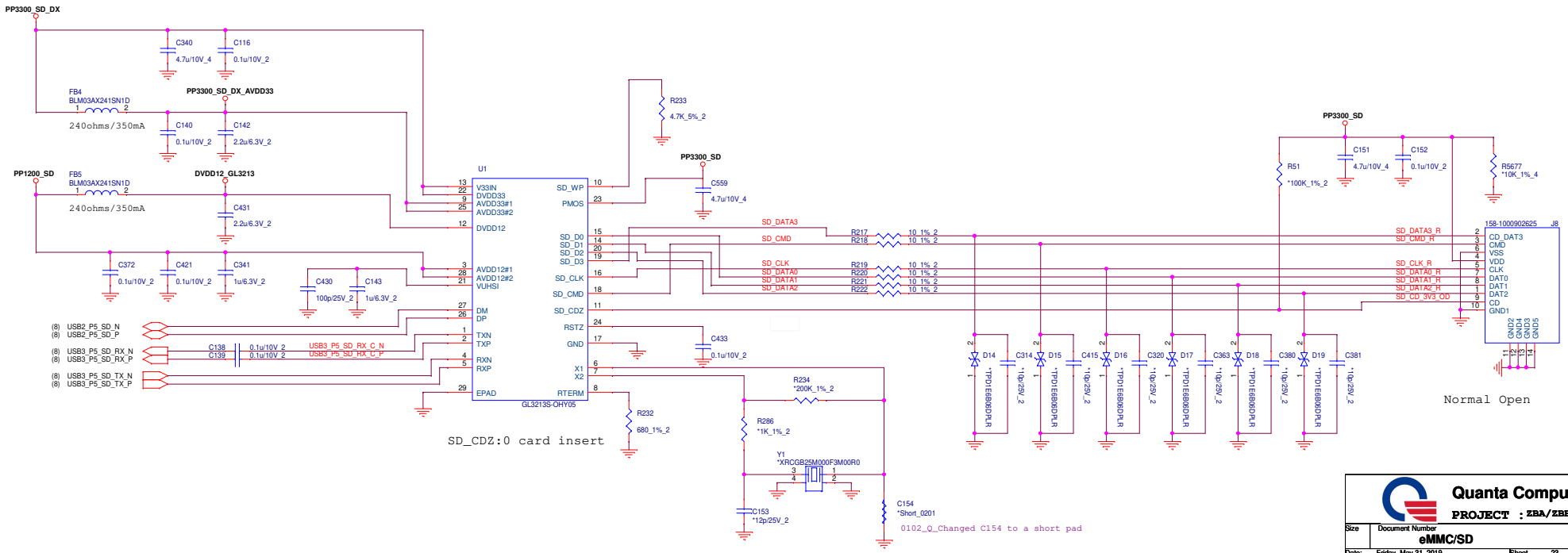
150 UA SLEEP CURRENT





(CRD)

MICRO SD CARD



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PROJECT : ZBA/ZBB

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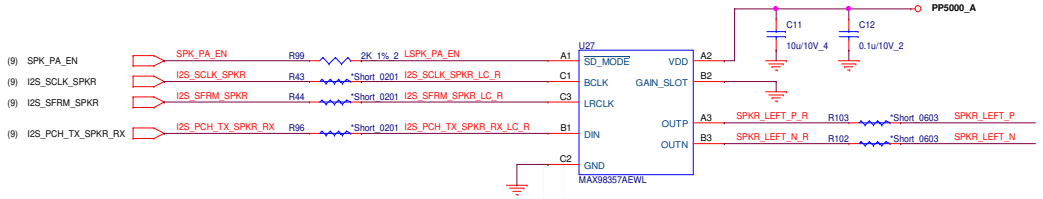
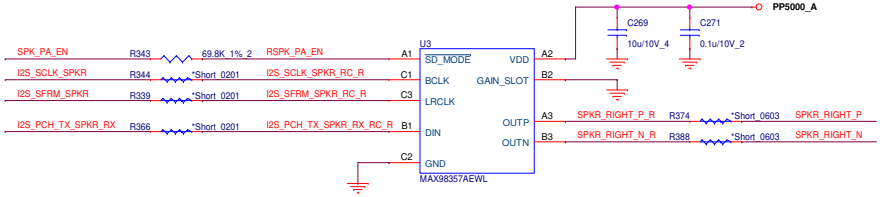
(AMP)

LEFT CHANNEL



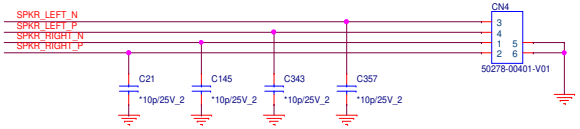
LEFT CHANNEL = SHORT (OR 2K FOR SAFETY) TO 1.8V
GAIN_SLOT: 100K TO GND = 15 DB GAIN
GAIN_SLOT: 0 TO GND = 12 DB GAIN
GAIN_SLOT: UNCONNECTED = 9 DB GAIN
GAIN_SLOT: 0 TO VDD = 6 DB GAIN
GAIN_SLOT: 100K TO VDD = 3 DB GAIN

RIGHT CHANNEL



RIGHT CHANNEL = 69.8K TO 1.8V
GAIN_SLOT: GND = 12 DB GAIN

(ADO)

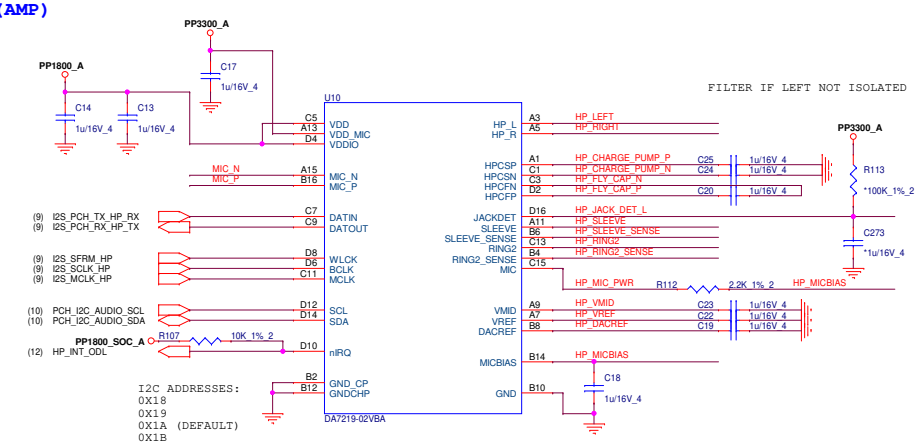


(THM)

Note for placement, it
needs to be placed near CPU
requested by thermal team

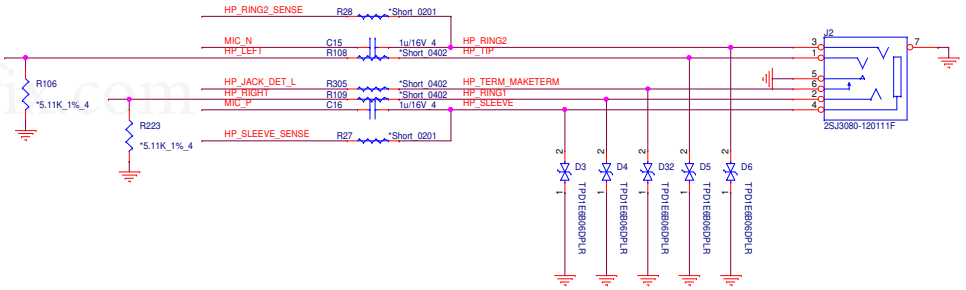
CSP PACKAGE, BUT CAN BE ROUTED ON TYPE-3
<10UA IN DEEP SLEEP

(AMP)



(ADO)

5K TO FILTER LEFT IF NOT ISOLATED



CHANGED MIC SERIES CAPS TO 1UF TO MATCH 10HZ 3DB
FREQUENCY RECOMMENDED IN THE DA7219 DATASHEET

THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL
THE SAME APPLIES TO HP_SLEEVE AND HP_SLEEVE_SENSE SIGNALS
ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

Quanta Computer Inc.
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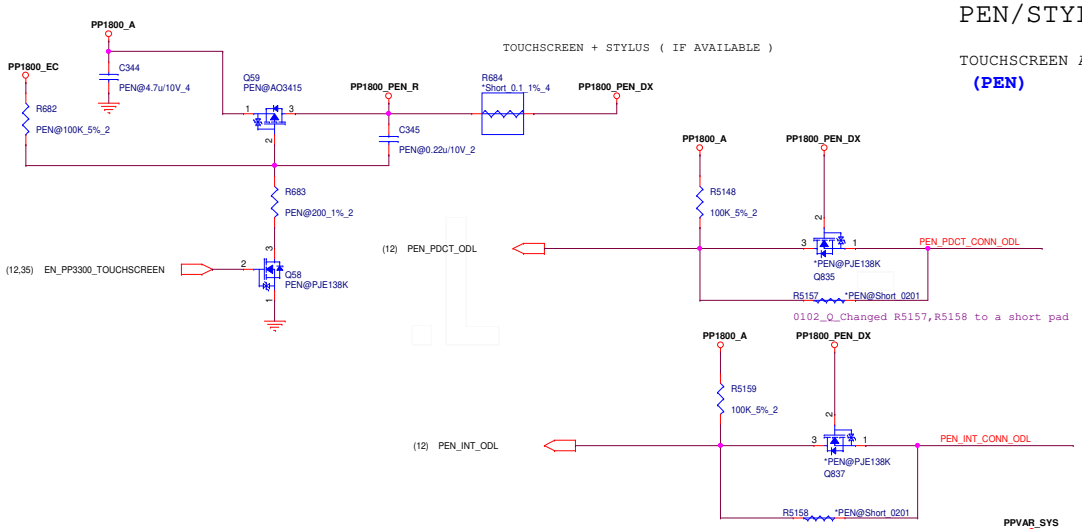
PEN/STYLUS CONNECTOR

TOUCHSCREEN AND PEN/STYLUS POWER TOGETHER

PEN 7-BIT I2C ADDRESS = 0X09
~ 100 MA

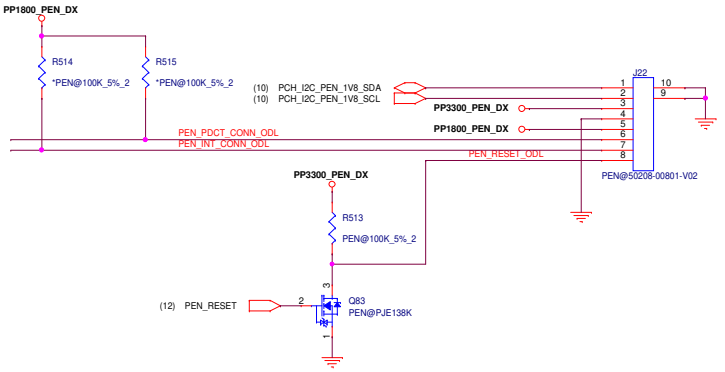
(PEN)

TOUCHSCREEN + STYLUS (IF AVAILABLE)

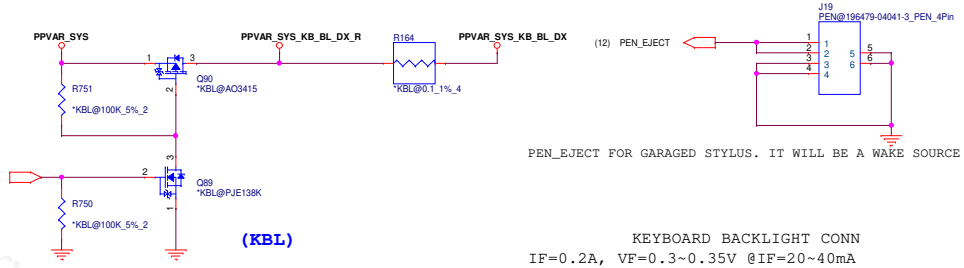


STUFF R5148,R5159,R5157,R5158 DEFAULT
IF LEAKAGE FOUND, STUFF Q835,Q837,R514,R515
AND DEPOP R5157,R5158,R5148,R5159

(PEN)



(KBL)

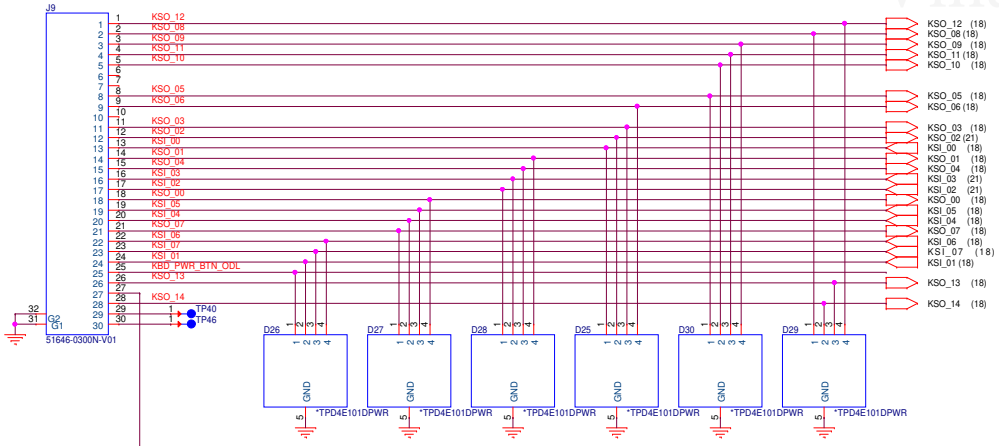


PEN_EJECT FOR GARAGED STYLUS. IT WILL BE A WAKE SOURCE

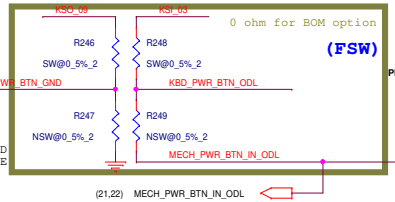
(KBC)

KEYBOARD

CM TO CHOOSE CONNECTOR- THIS ONE WILL SUPPORT THE KEYPAD SO THE PINOUT MAY NEED TO CHANGE



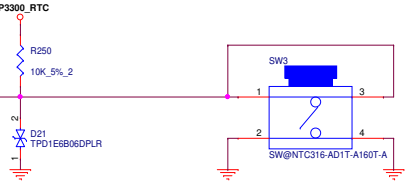
STUFF THESE FOR KEYBOARD LOCK BUTTON



THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHELL SKU

(21,22) MECH_PWR_BTN_IN_ODL

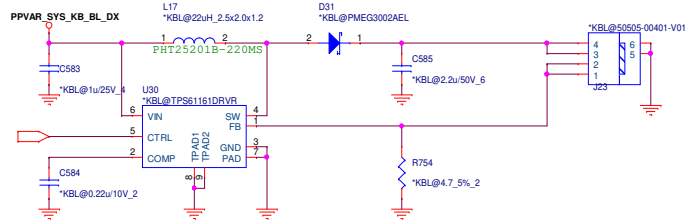
STUFF THESE FOR KEYBOARD POWER BUTTON



Convertible	R246,R248,SW3 STUFF ; R247,R249 NC
Clamshell	R247,R249 STUFF ; R246,R248,SW3 NC

(KBL)

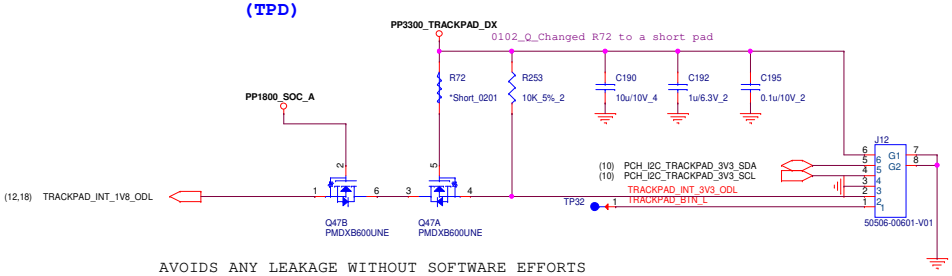
KEYBOARD BACKLIGHT CONN
IF=0.2A, VF=0.3~0.35V @IF=20~40mA



TRACKPAD CONNECTOR

CM TO CHOOSE CONNECTOR

(TPD)



AVOIDS ANY LEAKAGE WITHOUT SOFTWARE EFFORTS

Quanta Computer Inc.
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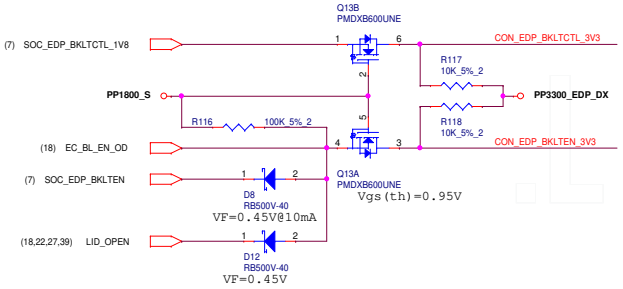
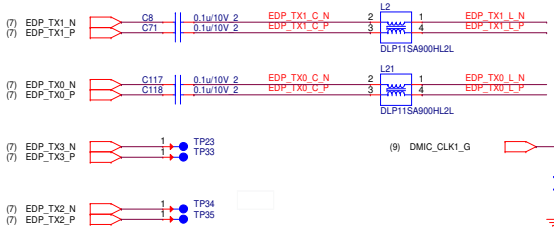
(LDS)

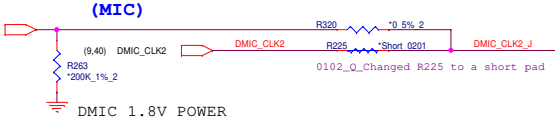


EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR

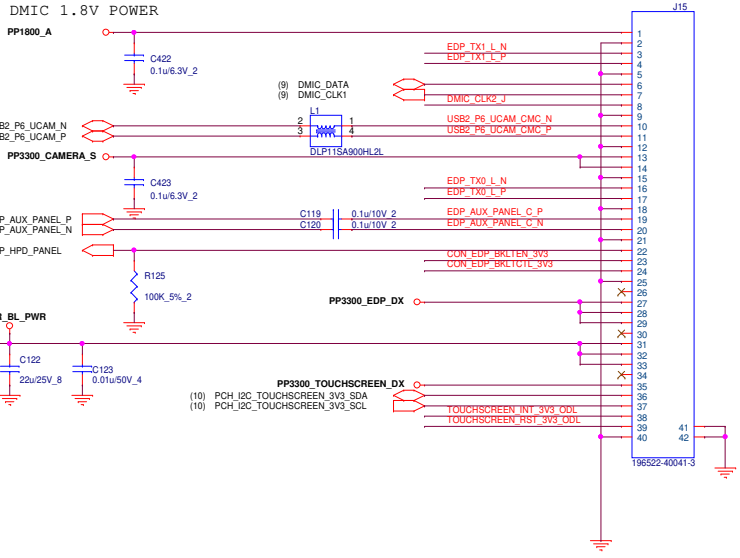


EDP + MIC + SENSOR +CAMERA CONNECTOR

(MIC)

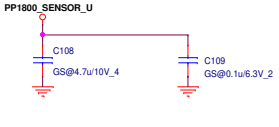


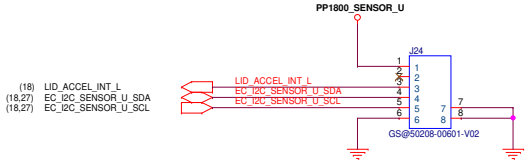
DMIC 1.8V POWER



LID ACCEL-CORAL

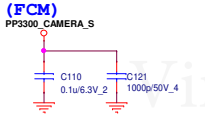
(ACS)



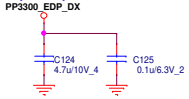


I2C MODE: (SET BY NCS TIE TO VDDIO)
I2C 8bit ADDRESS: 0X3E (SDO_ADDR = VDDIO)
I2C MAX SPEED = 3.4MHZ

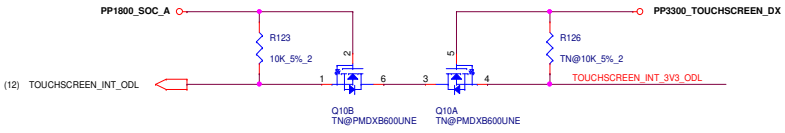
(FCM)



(LDS)



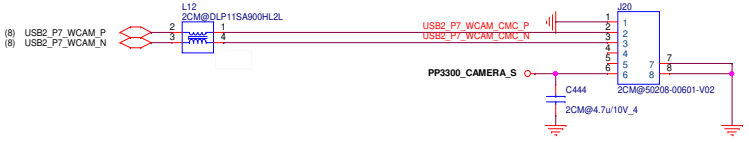
(TSN)



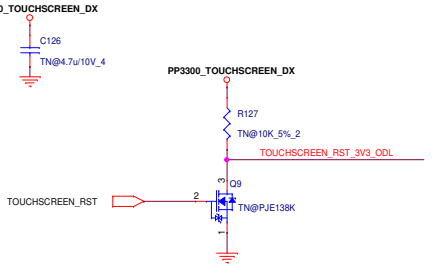
WFC CAMERA

(RCM)

WFC INTERFACE PINOUT TBD. PENDING CHANGE



(TSN)



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	LID(eDP/CAM/TOUCH/SENSOR)	1A
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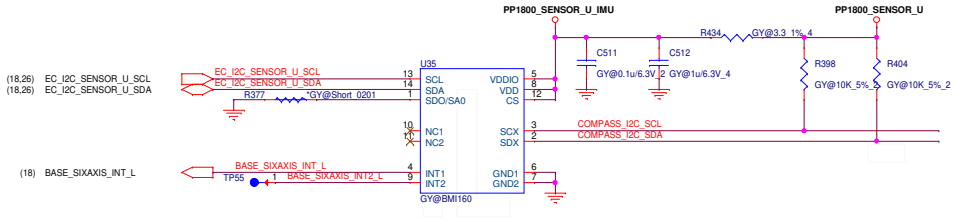
(GRS)



IMU

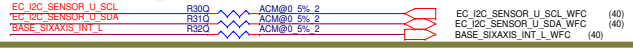
MODE 2 (SLAVE TO EC, MASTER TO MAG)

I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 7'0X68 (LSB SET BY SD0/SA0) -->8'0xD0h

(ACM)

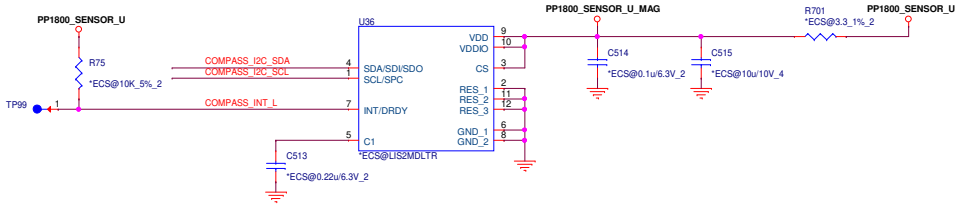
0 ohm for BOM option

R30Q~R32Q place near to IMU U35



for AR Camera, IMU can be DNS, but R30Q,R31Q,R32Q need to be stuffed

(ECS)



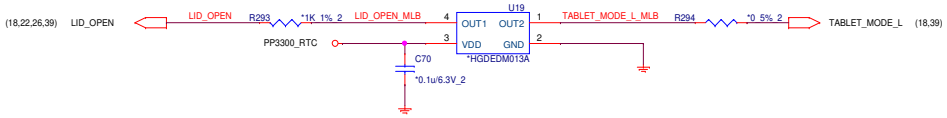
MAGNETOMETER

SLAVE TO IMU SENSOR

I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 0X1E

GMR SENSOR (RESERVED FOR ON BOARD SITUATIOM

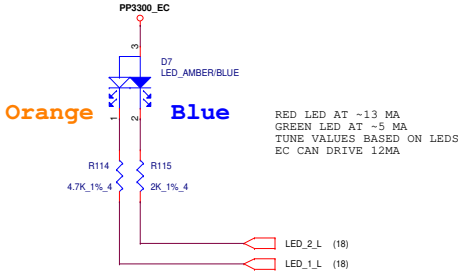
(GMR_MLB) **For on board GMR**



MAKE SURE TO CHECK THE POLARITY OF MAGNET TO ASSIGN THE PIN LID-OPEN AND TABLET-MODE
IF THE GMR SENSOR IS NOT PLACED ON THE MLB, PLEASE CAREFULLY PLAN THE PINOUT ON THE SUB-BOARD INTERFACE.

(UIF)

CHARGE/BATTERY LED



RED LED AT ~13 MA
GREEN LED AT ~5 MA
TUNE VALUES BASED ON LEDS
EC CAN DRIVE 12MA

Quanta Computer Inc.
PROJECT : ZBA/ZBB

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	SENSOR(COMPASS/GYRO)(OP1)	1A
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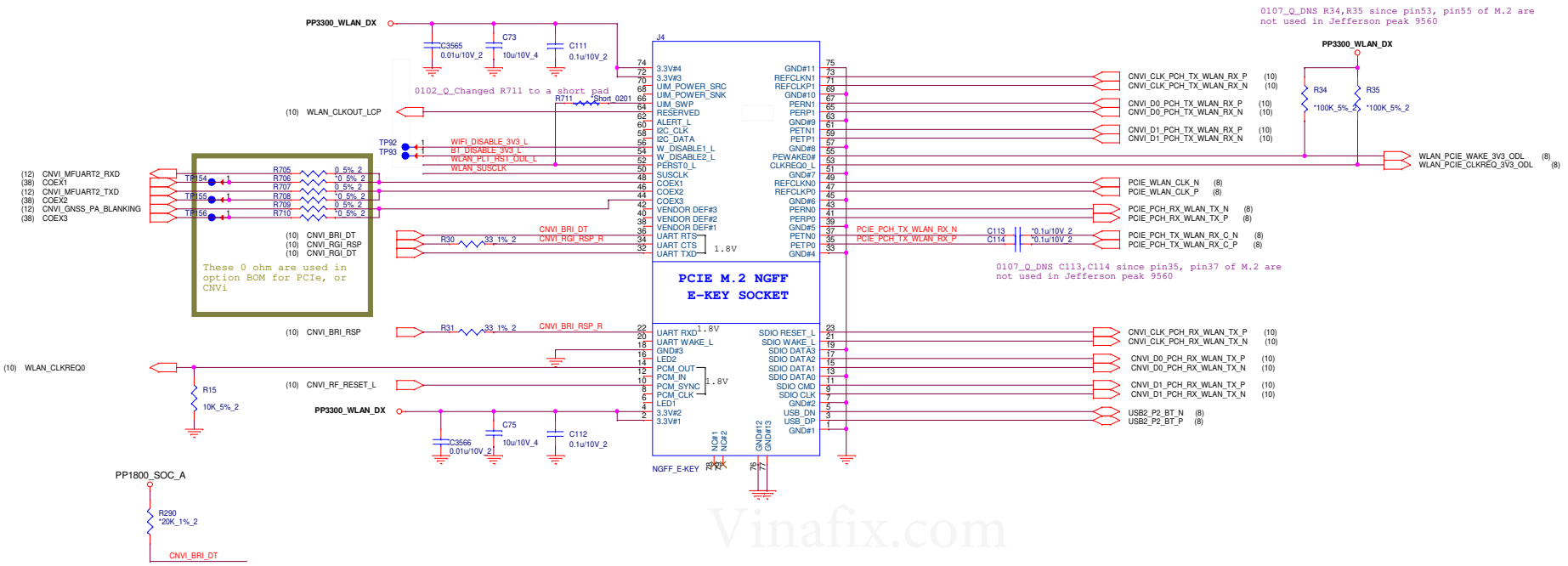
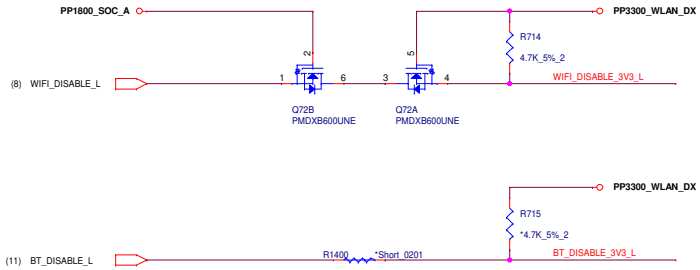
WIFI

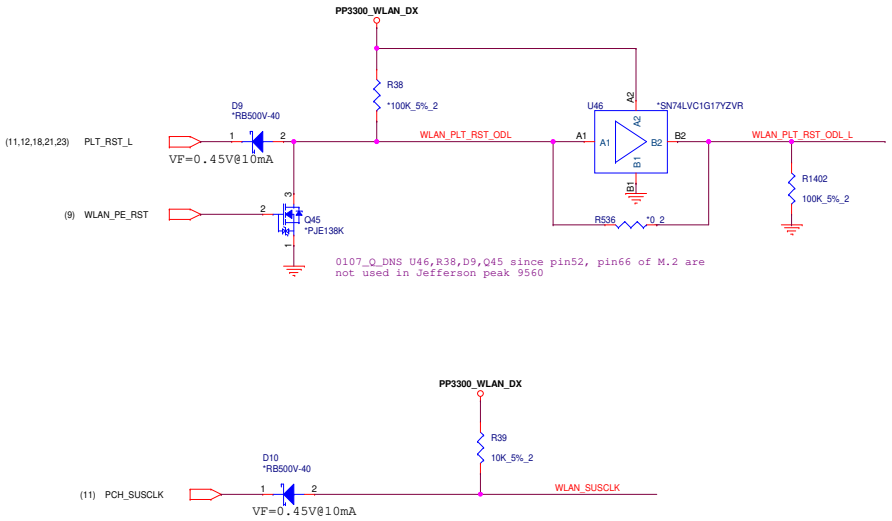
CM TO CHOOSE CONNECTOR

(NGF)



PLACE THE PULL-UP R CLOSE TO M.2. (FOR DEBUG)





U46,R38,D9,Q45,C113,C114,R34,R35,Q1,Q2 need to be stuffed for WiFi flexible design

Quanta Computer Inc.

PROJECT : ZBA/ZBB

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	WIFI/BT CONNECTOR	1A
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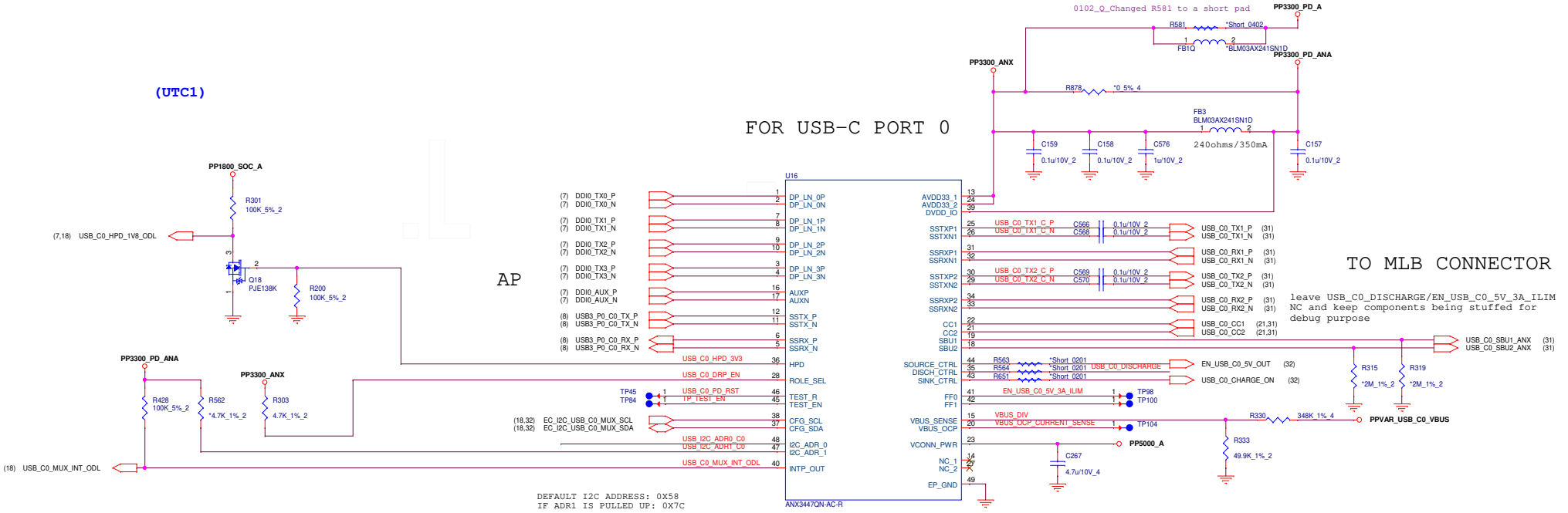
(UTC1)

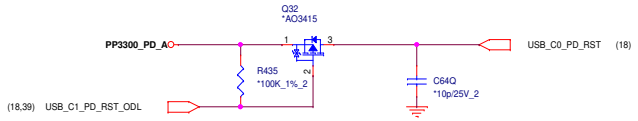
FOR USB-C PORT 0



TO MLB CONNECTOR

leave USB_C0_DISCHARGE/EN_USB_C0_5V_3A_ILIM NC and keep components being stuffed for debug purpose

WITH THE NX20P3483, THE VBUS DISCHARGE CAN BE SW CONTROL



USB_C0_PD_RST IS ACTIVE HIGH WITH 100K INTERNAL PD

Quanta Computer Inc.		
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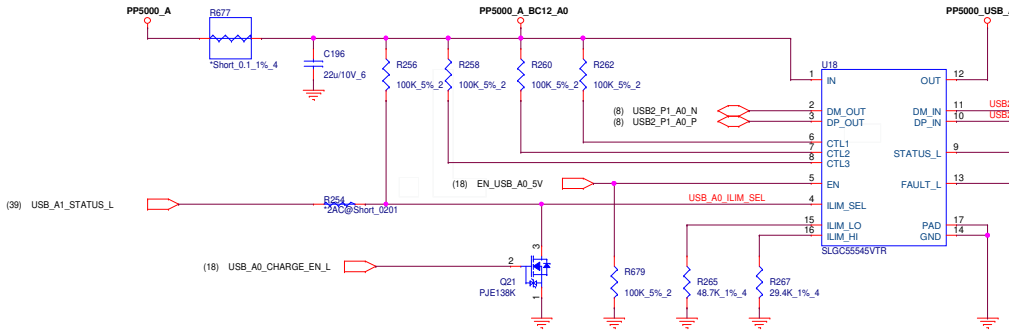
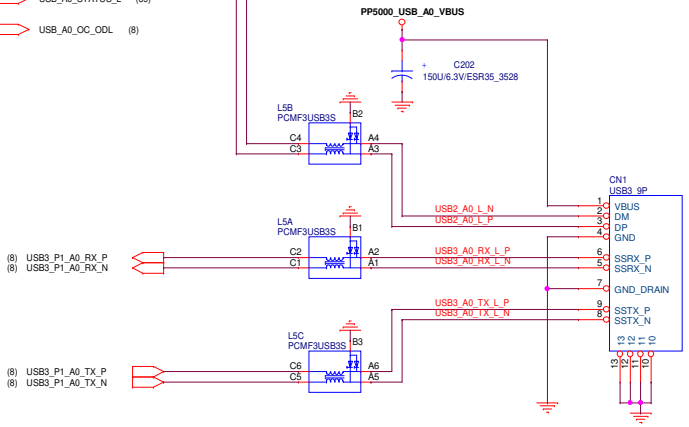
BC 1.2 FOR THE TYPE-A PORT A0

(UBC1)



(UB31)

CM TO CHOOSE CONNECTOR



Quanta Computer Inc.		
PROJECT : ZBA/ZBB		
Size	Document Number: USB A CONNECTIONS(MLB)	Rev: 1A
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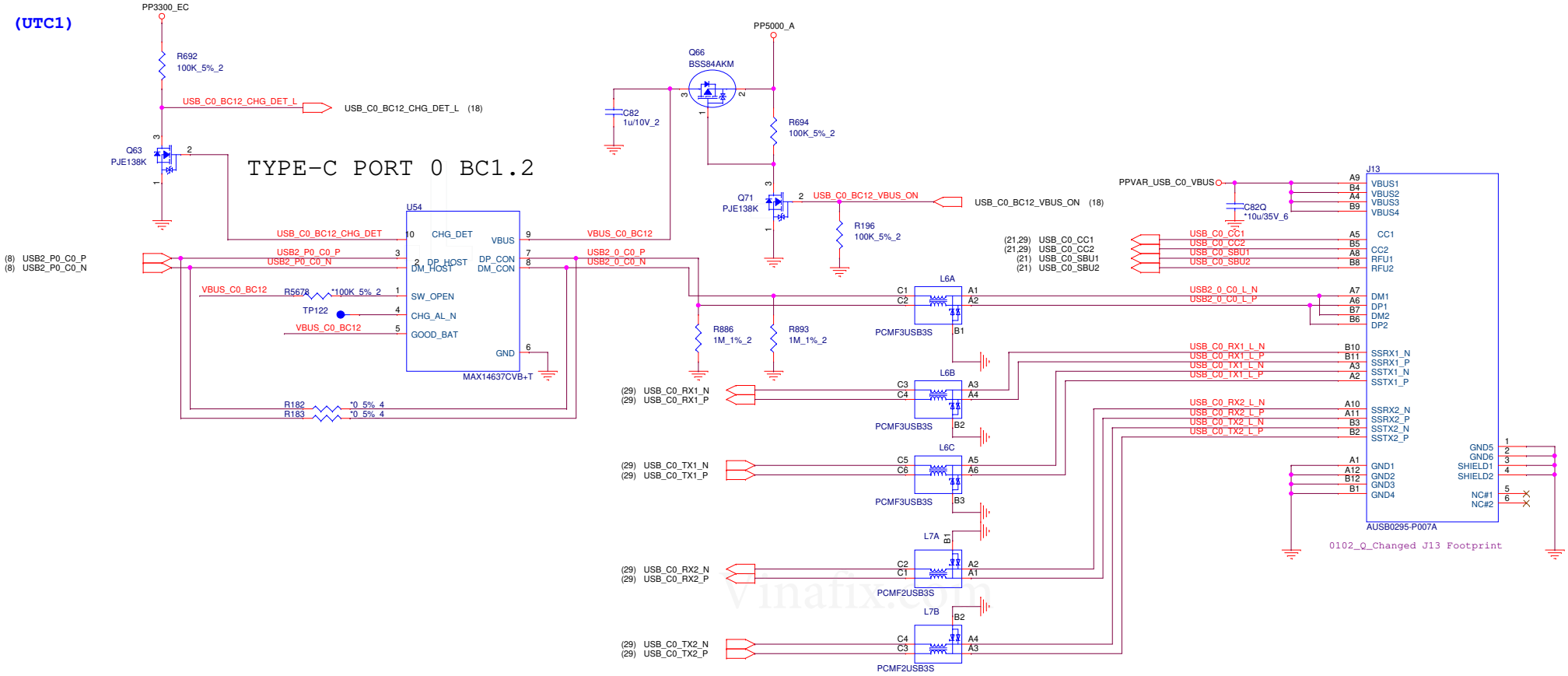
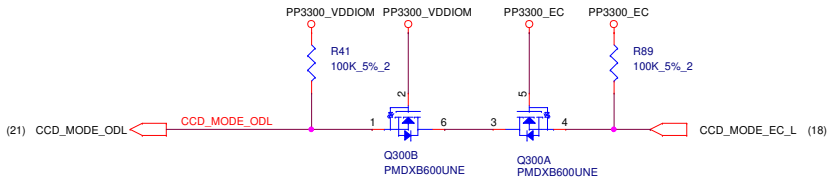
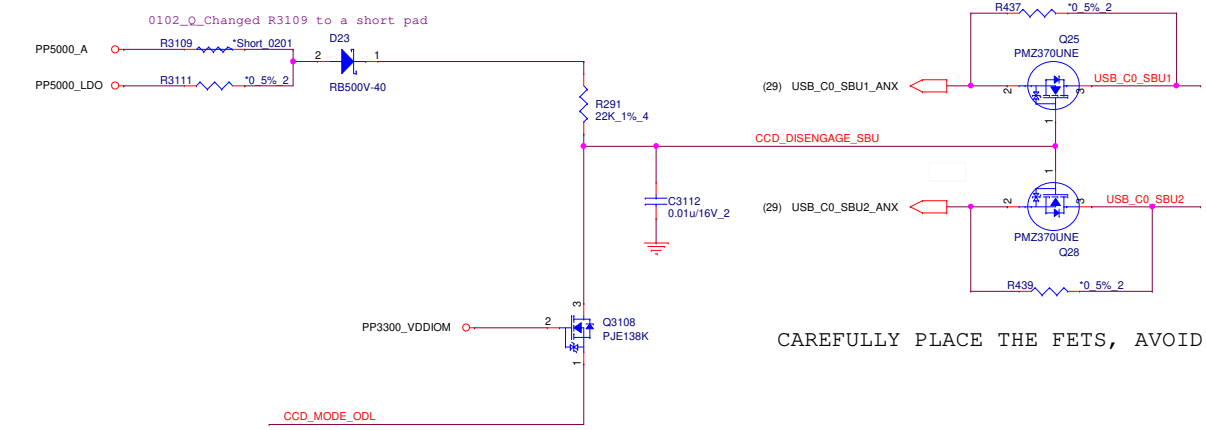
(UTC1)

TYPE-C PORT 0 BC1.2



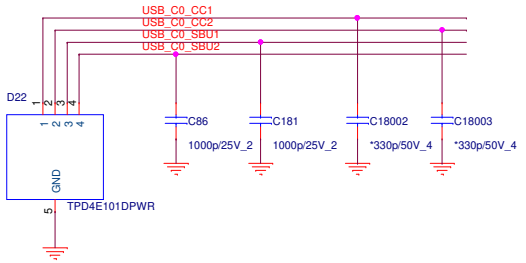


ONLY TIME CCD_DISENGAGE_SBU IS HIGH WHEN CCD_MODE IS INACTIVE AN THERE IS POWER TO THE TCPC



CAREFULLY PLACE THE FETS, AVOID LONG STUB

(UTC1)



Quanta Computer Inc.

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	USB C CONNECTOR (MLB)	1A

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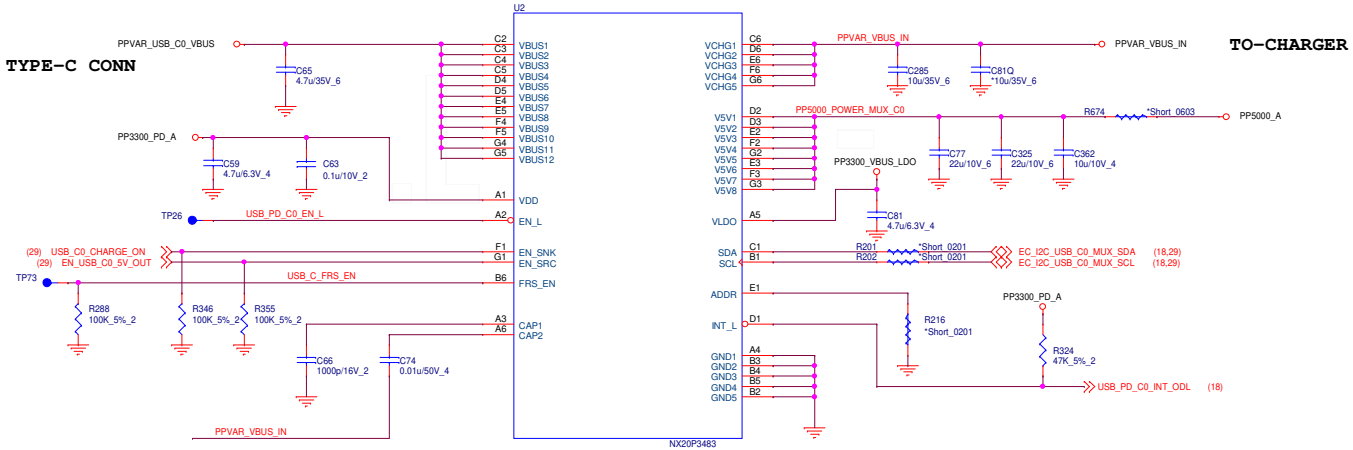
PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR

(PUB1)



Quanta Computer Inc.		
PROJECT : ZBA/ZBB		
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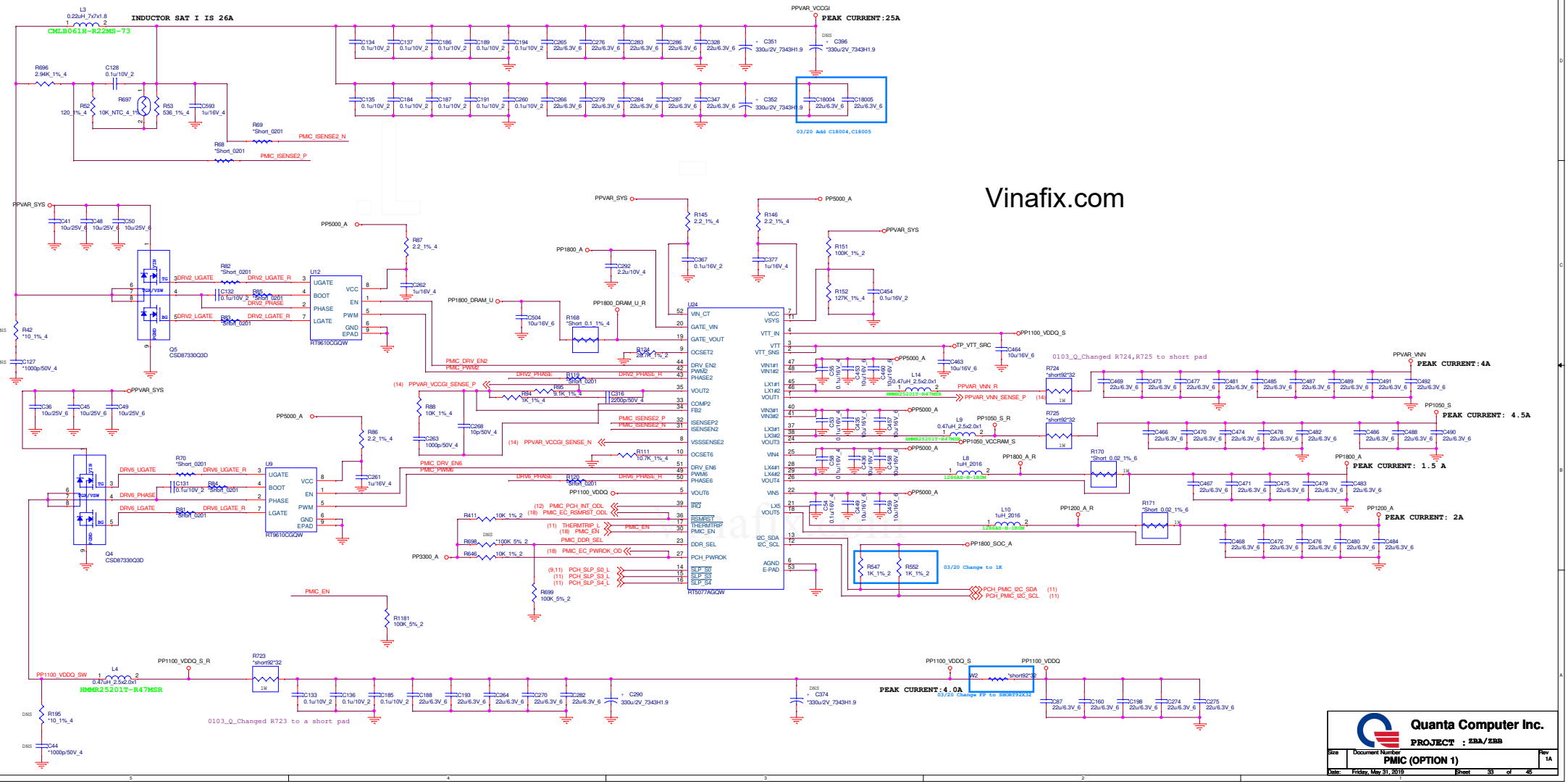
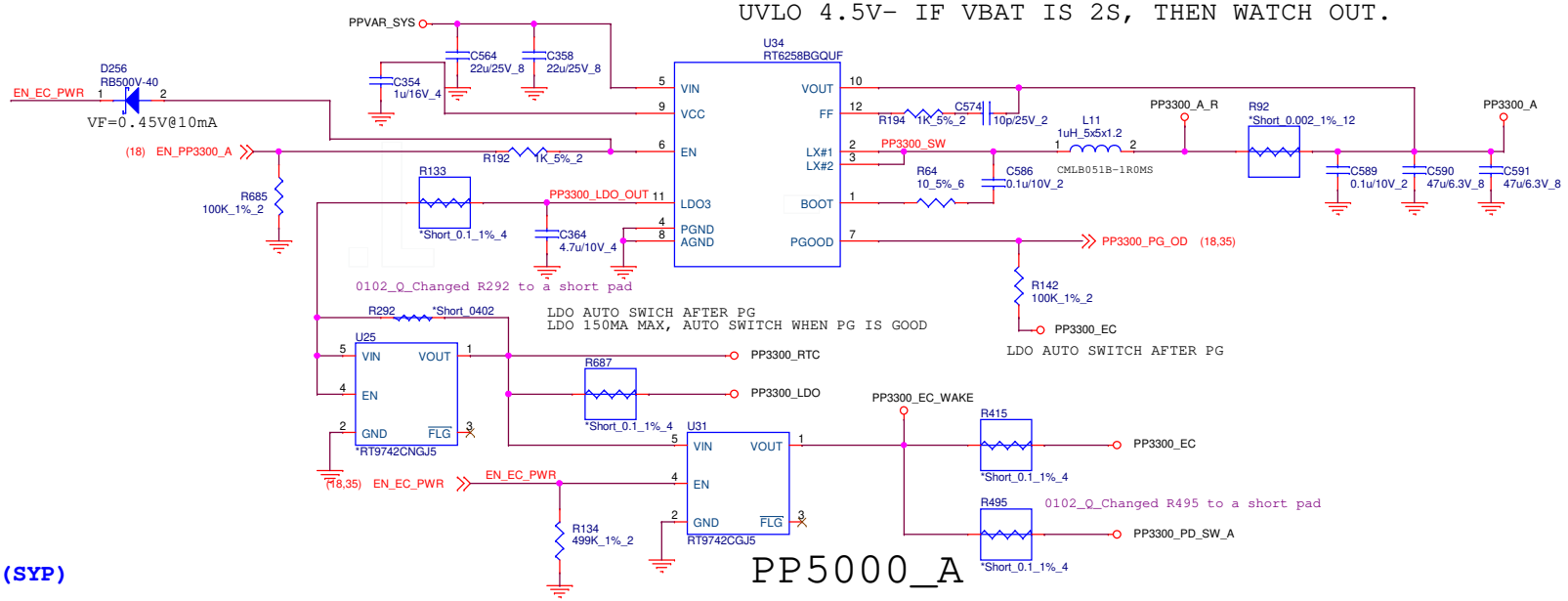


(SYP)

PP3300_A

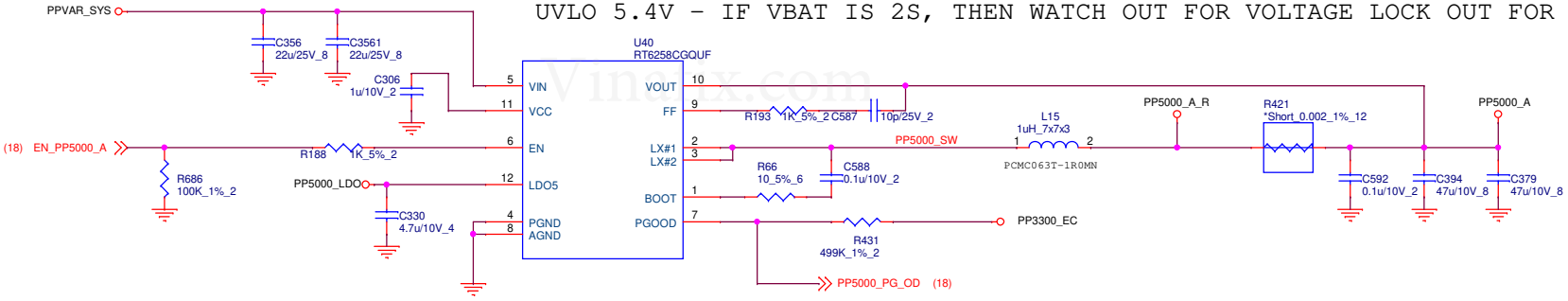
UVLO 4.5V- IF VBAT IS 2S, THEN WATCH OUT.



(SYP)

PP5000_A

UVLO 5.4V - IF VBAT IS 2S, THEN WATCH OUT FOR VOLTAGE LOCK OUT FOR 1.8V



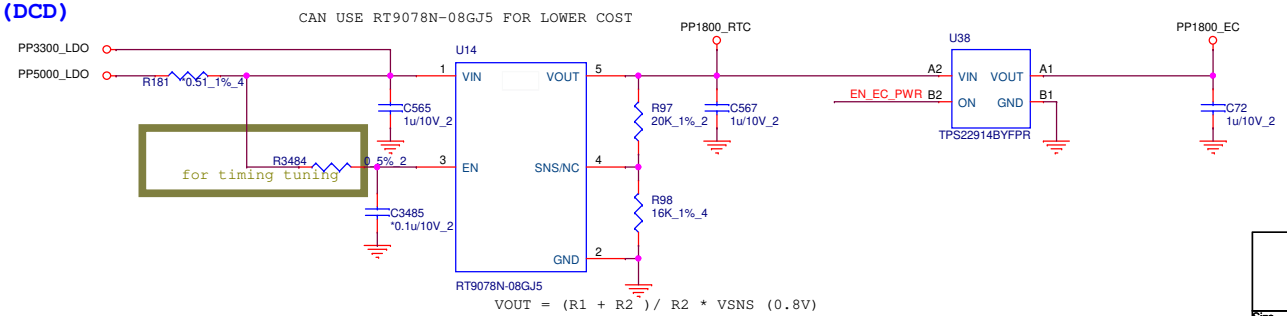
PP1800_RTC, PP1800_EC

(DCD)

PP1800_RTC CAN BE GENERATED BY A SEPARATE DC-DC R

CAN USE RT9078N-08GJ5 FOR LOWER COST

PP1800_EC CAN BE GENERATED BY A SEPARATE REGULATOR



VOUT = (R1 + R2)/ R2 * VSNS (0.8V)

CHOICES FOR THE REGULATORS CAN BE SUBSTITUE AFTER CONFIRM THE FUNCTIONALITY.

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PROJECT : ZBA/ZBB

Size	Document Number	Rev
	POWER: 1.8V(EC) 3.3V AND 5V	1A
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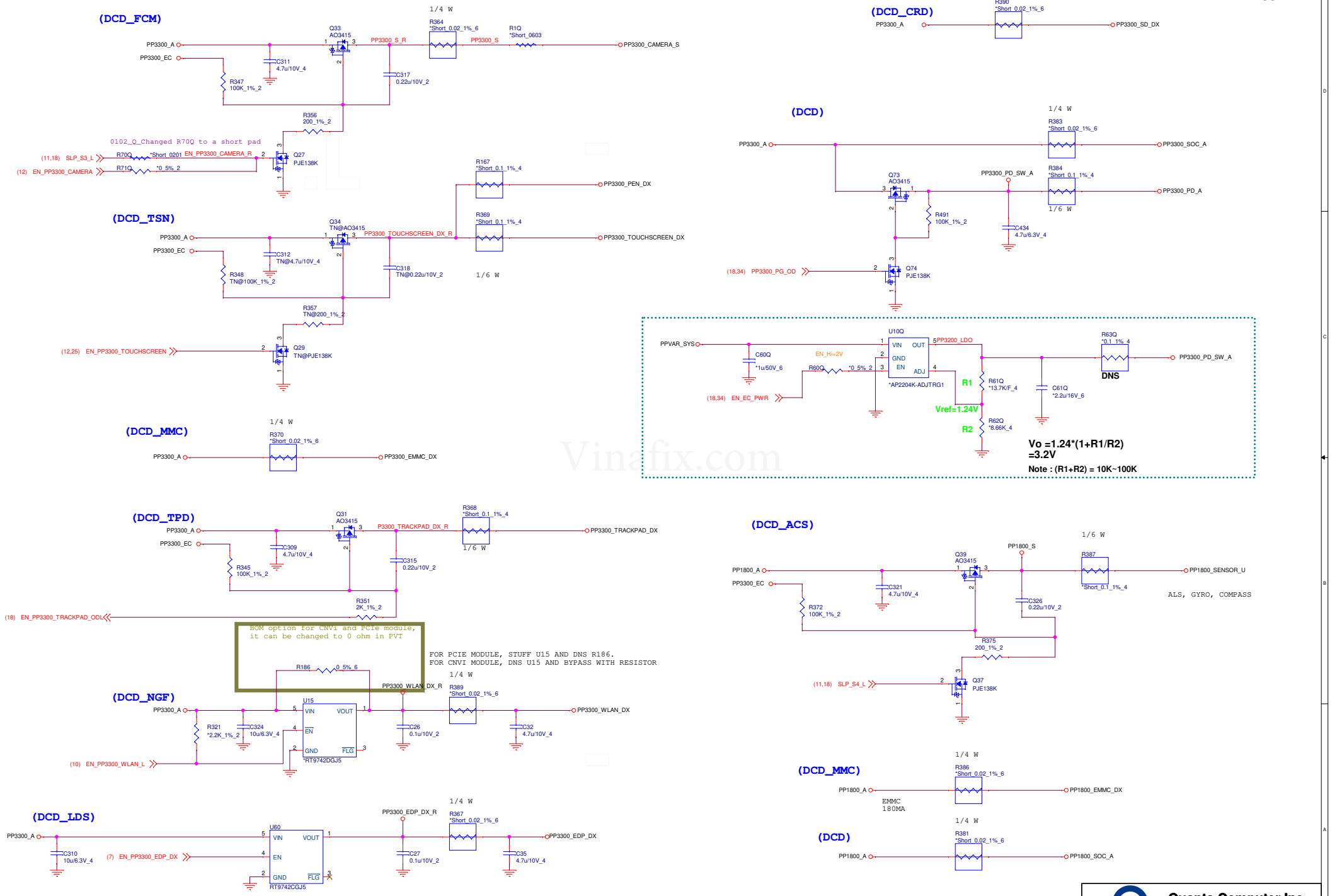

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PROJECT : ZBA/ZBB

Size	Document Number	Rev
	POWER - LOAD SWITCHES	1A
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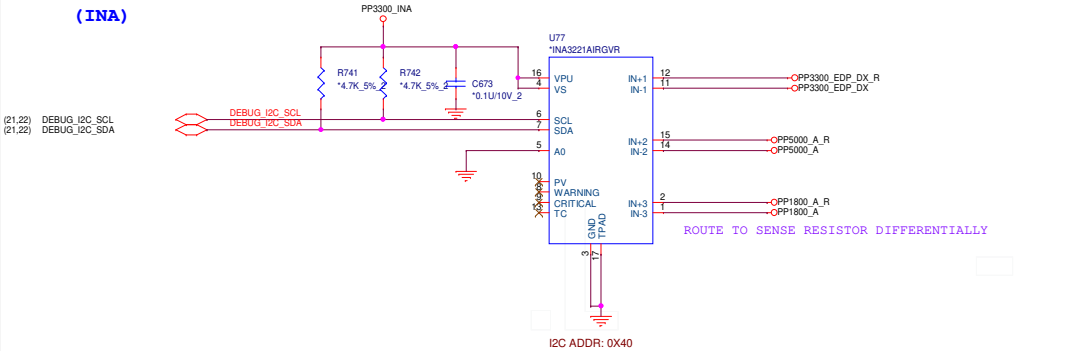
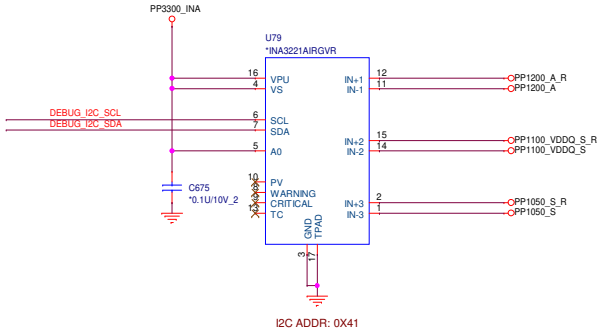
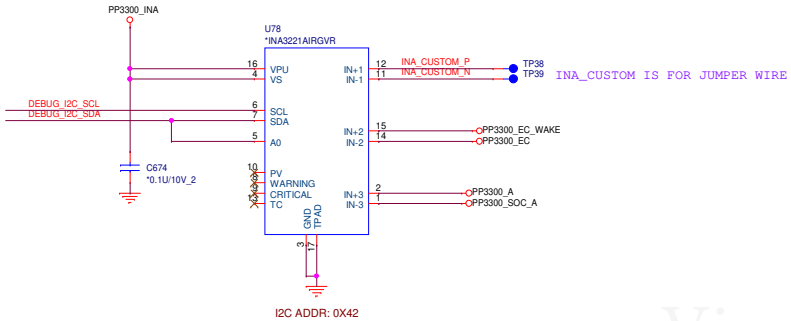
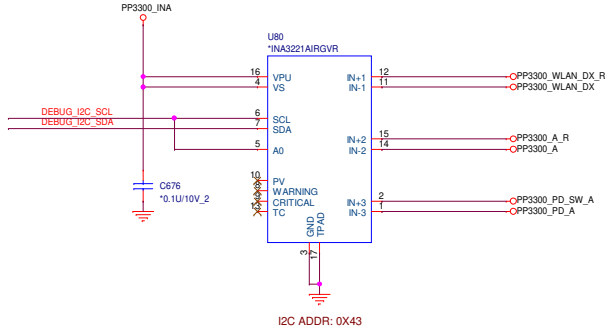
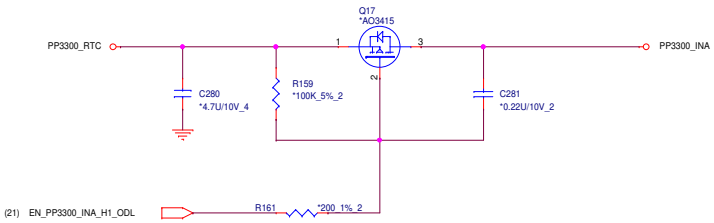
(INA)



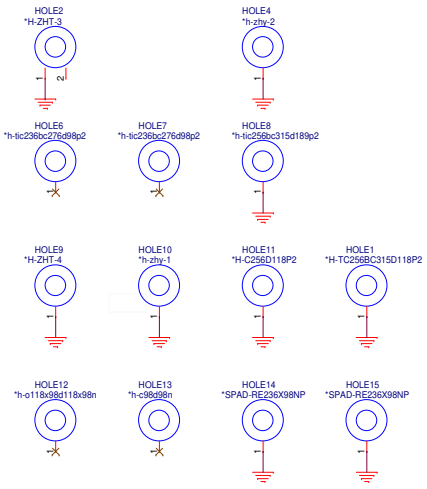




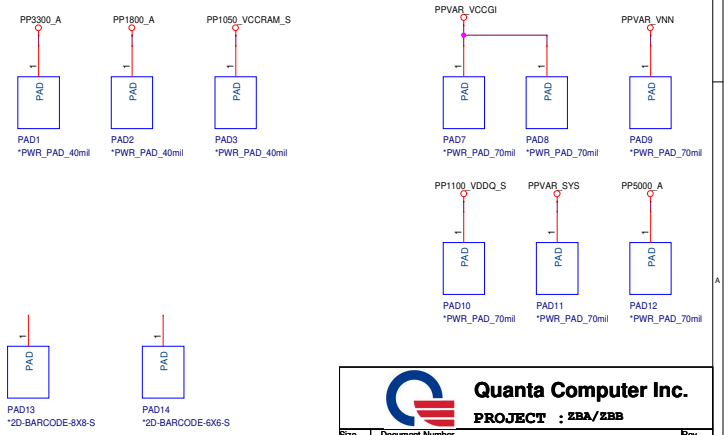




HOLES (OTH)



POWER TEST PAD (OTH)



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	INAs	1A
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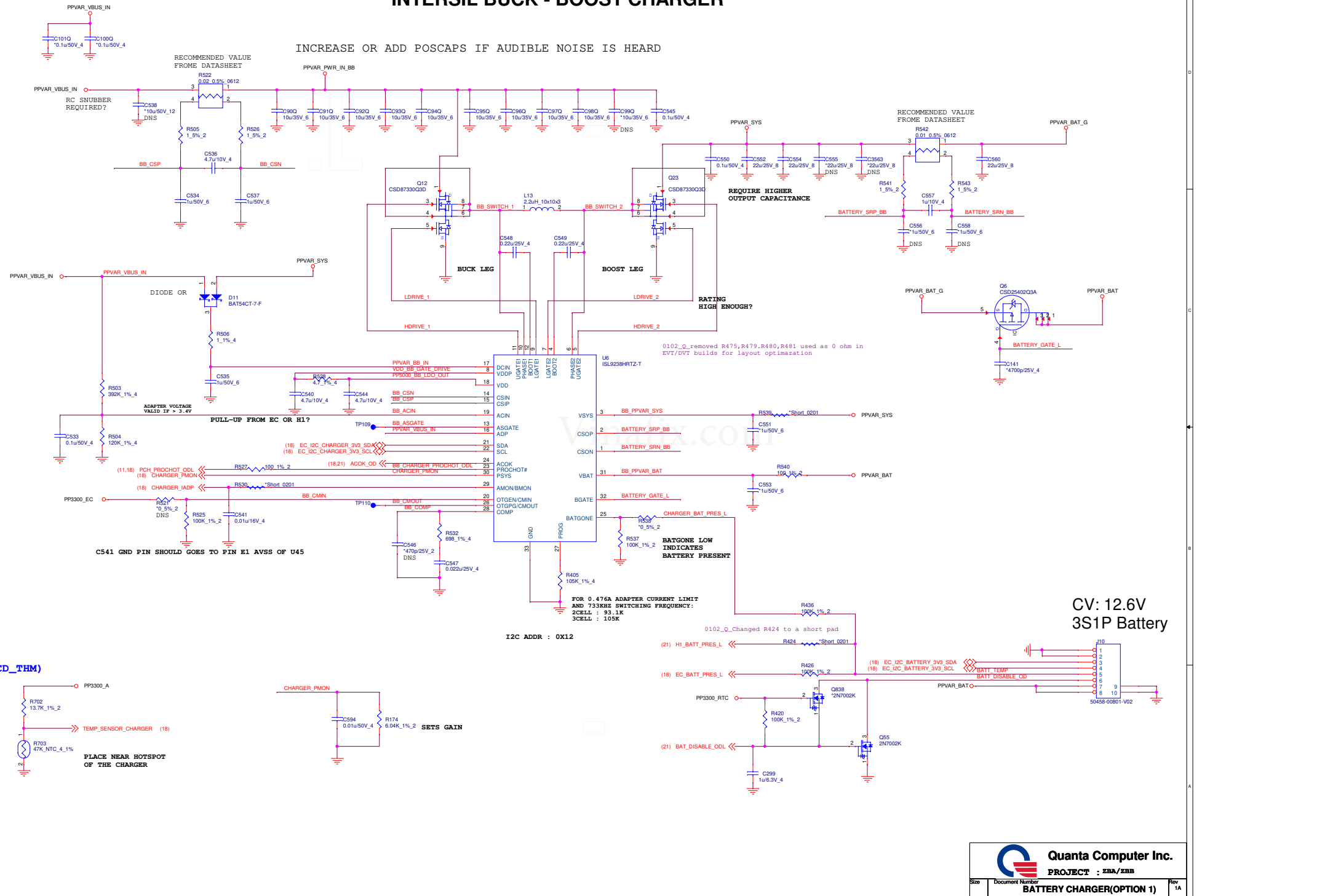
INTERSIL BUCK - BOOST CHARGER



Quanta Computer Inc.			
PROJECT : ZBA/ZBB			
Size	Document Number		Rev
	BATTERY CHARGER(OPTION 1)		1A
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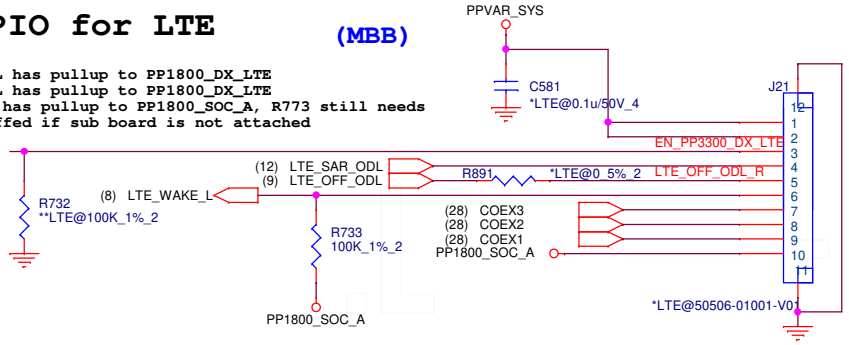
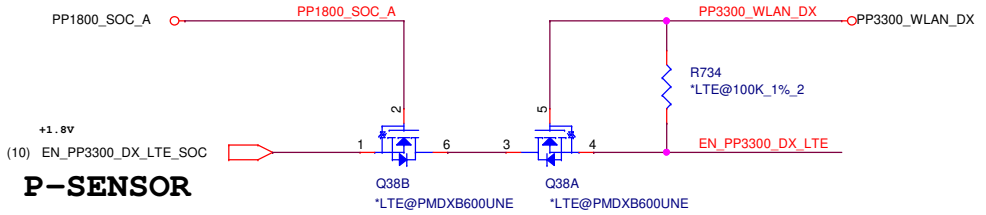
GPIO for LTE

(MBB)

Coral sub board
-LTE_SAR_ODL has pullup to PP1800_DX_LTE
-LTE_OFF_OFL has pullup to PP1800_DX_LTE
-LTE_WAKE_L has pullup to PP1800_SOC_A, R773 still needs to be stuffed if sub board is not attached

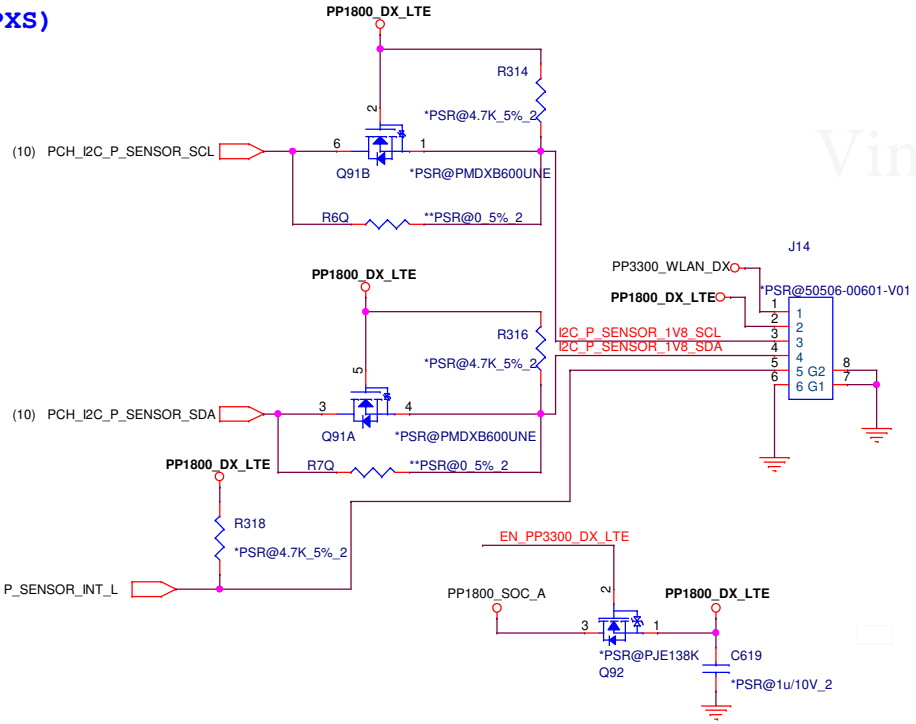


LEVERAGING CORAL BOARD!



P-SENSOR

(PXS)

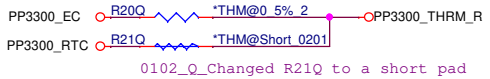


(SYS_THM)

Thermal Protector

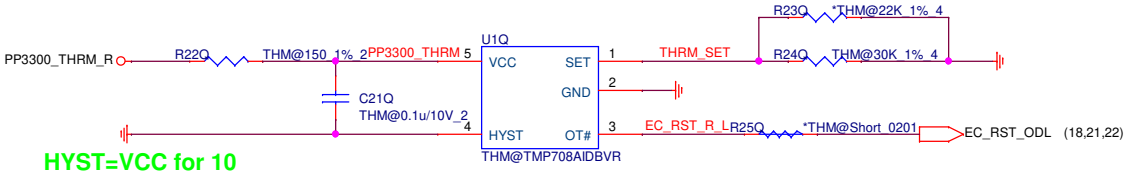
Need fine tune
for thermal protect point
Note placement position

TEMP=76.3C



0102_Q_Changed R21Q to a short pad

Rset(Kohm)=0.0012T*T-0.9308T+96.147



HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

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	LTE,STEST	1A
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(UTC2)

(18,22,26,27) LID_OPEN
(18) LED_3_L
R132 *Short_0201
R255 *0_5%_2
EC_GPIO_1
R197 *100K_5%_2

(18,27) TABLET_MODE_L
R322 *Short_0201
EC_GPIO_2

EC_GPIO1,2 CAN BE USED FOR CONNECTING THE GMR SENSOR ON THESUB-BOARD
OR IT CAN BE USED TO CONNECT AN SPARE EC GPIO PINS FOR ADDITIONAL CONTROL FROM EC

PPVAR_VBUS_IN
C87Q *10u/50V_12
C80Q *10u/35V_6
C62 10u/35V_6
C68 2AC@0.1u/50V_4
J6 2AC@51288-0060N-001

PULL-DOWN RESISTORS TO AVOID
FLOATING INPUT W/O SUB-BOARD

PP3300_RTC
C424 0.1u/16V_4
PP3300_PD_A
R48 1.8K_1%_2
R49 1.8K_1%_2
R259 100K_5%_2
C425 2AC@0.1u/16V_4

(18) USB_PD_C1_INT_ODL
(18) EC_I2C_USB_C1_MUX_SCL
(18) EC_I2C_USB_C1_MUX_SDA
(18,29) USB_C1_PD_RST_ODL
C3562 *2AC@1u/6.3V_2

PP3300_EC
R229 100K_5%_2
R185 100K_5%_2
R693 100K_5%_2
USB_C1_BC12_CHG_DET_L
EC_VOLUP_BTN_ODL
EC_VOLDN_BTN_ODL

J17
(7) DDI1_AUX_P
(7) DDI1_AUX_N
DDI1_AUX_P
DDI1_AUX_N
EC_GPIO_1
USB_PD_C1_INT_ODL
EC_I2C_USB_C1_MUX_SCL
EC_I2C_USB_C1_MUX_SDA
EC_GPIO_2
USB_C1_HPD_3V3
USB_C1_PD_RST_ODL
(18) EC_VOLUP_BTN_ODL
(18) EC_VOLDN_BTN_ODL
(30) USB_A0_STATUS_L
EC_VOLUP_BTN_ODL
EC_VOLDN_BTN_ODL
USB_C1_CC1
USB_C1_CC2
TP79
TP80
USB_C1_BC12_CHG_DET_L
(18) USB_C1_BC12_CHG_DET_L
(18) USB_C1_BC12_VBUS_ON
(18) USB_C1_MUX_INT_ODL
(18) USB_A1_CHARGE_EN_L
(18) EN_USB_A1_5V
(8) USB_A1_OC_ODL
(30) USB_A1_STATUS_L
PP5000_A
C426 2AC@0.1u/16V_4
(18) SUB_GPIO_ADC
R135 *2AC@Short_0201
0102_Q_Changed R135 to a short pad
FH34SRJ-40S-0.5SH(50)

CC1, CC2 ARE FOR BIP INTERFACE

(8) USB3_P4_C1_TX_P
(8) USB3_P4_C1_TX_N
(8) USB2_P3_A1_N
(8) USB2_P3_A1_P
(8) USB3_P4_C1_RX_P
(8) USB3_P4_C1_RX_N
(8) USB2_P4_C1_P
(8) USB2_P4_C1_N
(7) DDI1_TX3_N
(7) DDI1_TX3_P
(7) DDI1_TX2_N
(7) DDI1_TX2_P
(7) DDI1_TX1_N
(7) DDI1_TX1_P
(7) DDI1_TX0_N
(7) DDI1_TX0_P
(8) USB3_P3_A1_TX_N
(8) USB3_P3_A1_TX_P
(8) USB3_P3_A1_RX_N
(8) USB3_P3_A1_RX_P
J18
2AC@FH34SRJ-30S-0.5SH(50)

SELECT PER SEL SI TEAM

SUB_GPIO_ADC GOES TO AN ADC PIN OF EC WITH STUFFING OPTIONS
THE PIN CAN BE USED FOR VBUS DETECT OR FOR BOARD ID DETECT, OR USE AS A GENERAL GPIO FROM EC

SELECT PER SEL SI TEAM
CM TO ADJUST PINOUT/PIN COUNT

PP1800_SOC_A
R240 100K_5%_2
(7,18) USB_C1_HPD_1V8_ODL
USB_C1_HPD_1V8_ODL
Q19 2AC@PJE138K
USB_C1_HPD_3V3
R1401 2AC@499K_1%_2

MOTHER BOARD INTERFACE

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PROJECT : ZBA/ZBB

Size	Document Number	Rev
	CONNECTORS TO SUB BOARD	1A
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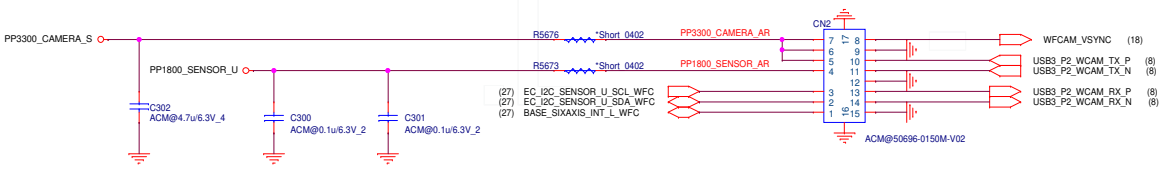
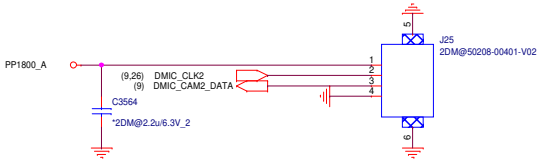
AR CAMERA CONN
(ACM)



DMIC CONN
(MIC2)



PREFERRED DMIC CHANNEL CONFIG
INTERFACE 1: STRAP MIC TO LEFT=CHANNEL 0
INTERFACE 2: STRAP MIC TO RIGHT=CHANNEL 3

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PROJECT : ZBA/ZBB
Size | Document Number: AR CONNECTORS | Rev: 1A
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	Blank	1A

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	Blank	1A

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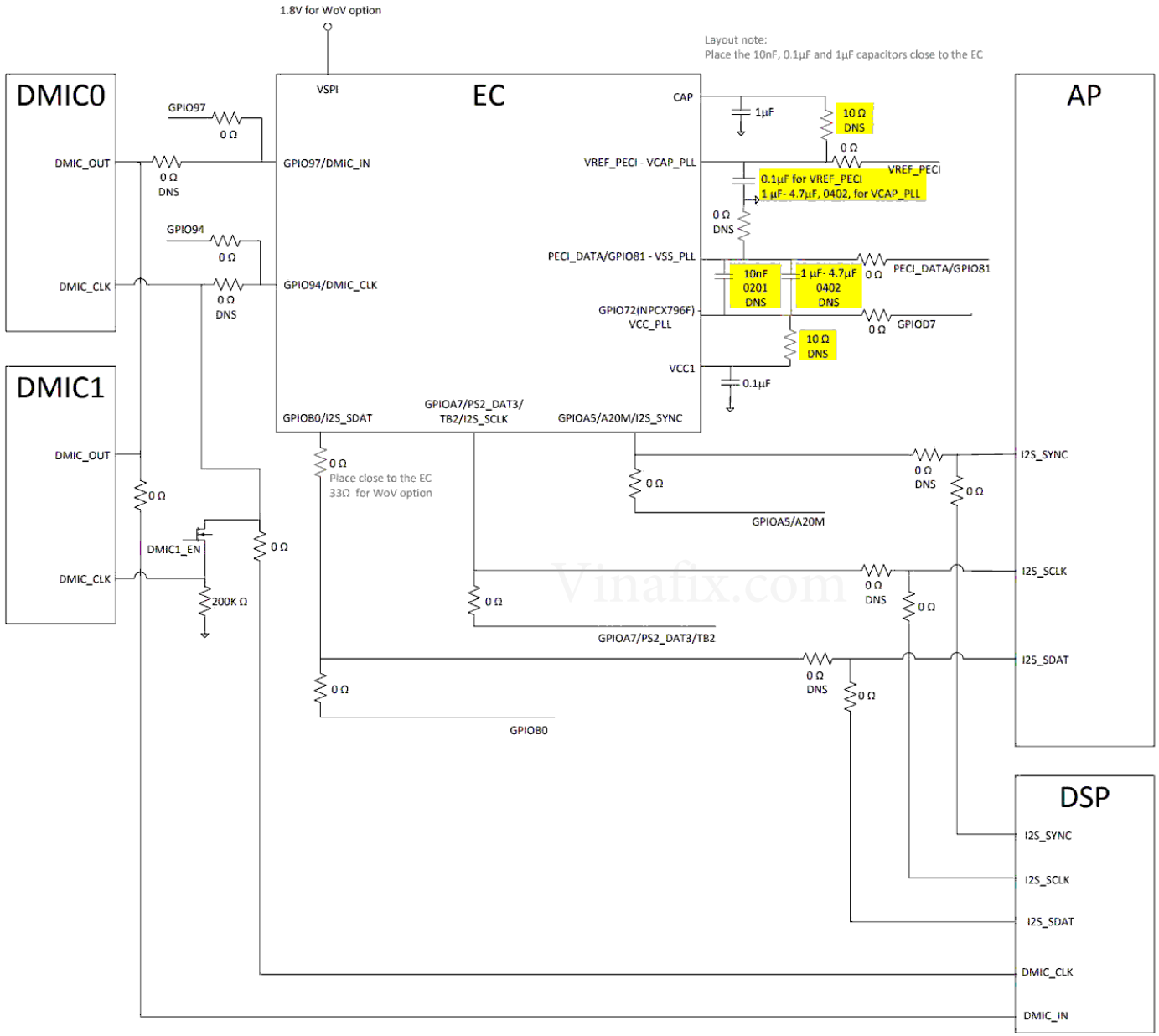

Quanta Computer Inc.		
PROJECT : ZBA/ZBB		
Size	Document Number: WOV DIAGRAM	Rev 1A
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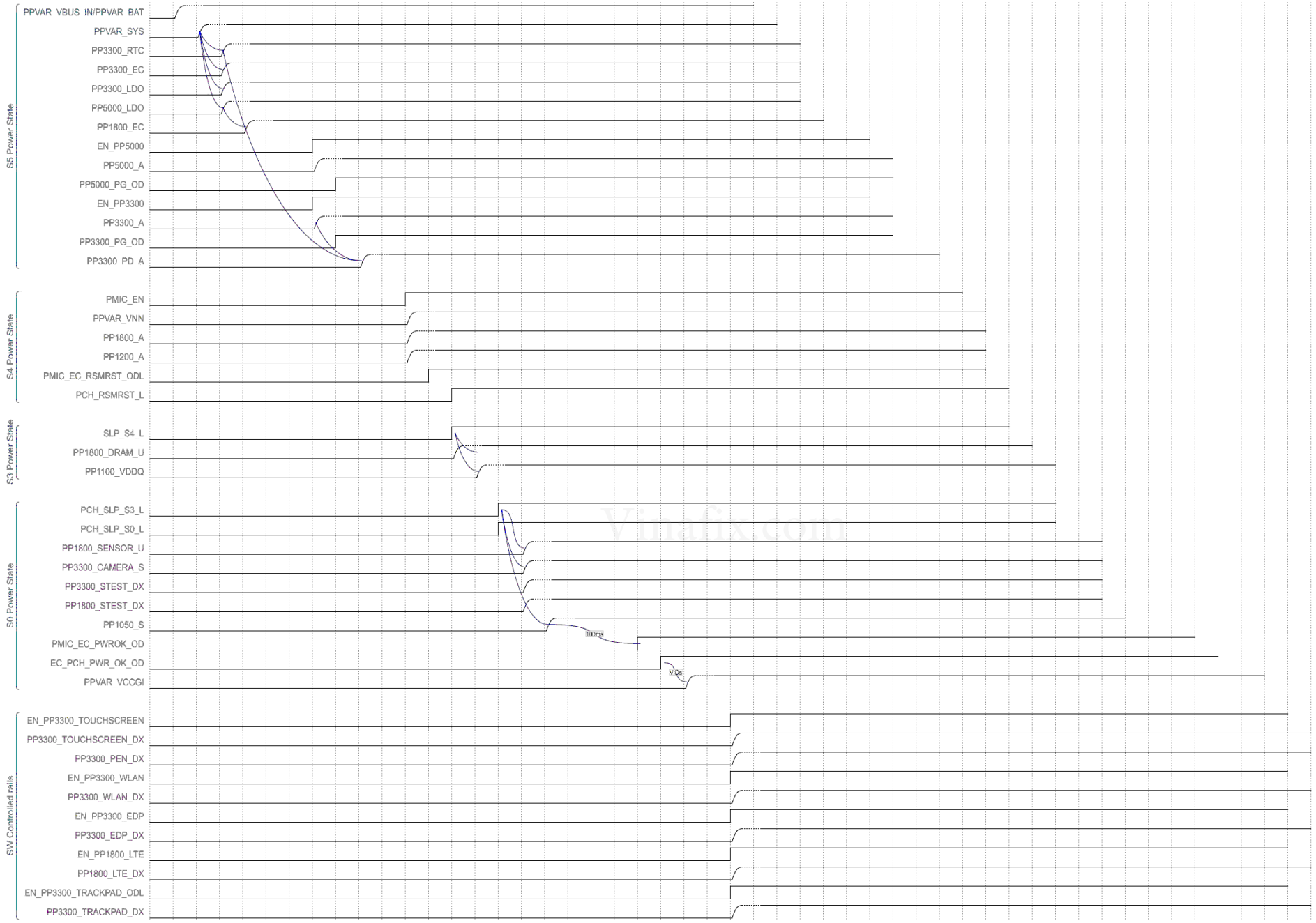

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PROJECT : ZBA/ZBB

Size	Document Number	Rev
	POWER SEQUENCE	1A

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GPIO #	Bump Name	Voltage	Bootstrap Termination	Default Termination	Bootstrap Purpose	Bootstrap Usage	Bootstrap	Octopus Signal Name
GPIO_27	GPIO_27	1.8V	20K PU	20K PD	eMMC as boot Source 20K PU internal	1 = enable (default) 0 = disable	eMMC Boot	DBG_PTI_DATA_16
GPIO_28	GPIO_28	1.8V	20K PU	20K PD	SPI as boot Source 20K PU internal	1 = enable (default) 0 = disable	SPI Boot	DBG_PTI_DATA_17
GPIO_42	GP_INTD_DSI_TE1	1.8V	20K PD	20K PD	Flash Descriptor Override for SPI security features	1 = Override 0 = No Override (default)	Flash Descriptor	TP_WIFI_RST_N, TP135
GPIO_43	GP_INTD_DSI_TE2	1.8V	20K PU	20K PD	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GP_INTD_DSI_TE2
GPIO_44	USB_OC0_B	1.8V	20K PD	20K PU	RVSD	1 = Do Not Use 0 = disable (default)	RSVD	USB_A_OC_ODL
GPIO_45	USB_OC1_B	1.8V	20K PD	20K PU	Top Swap Override. Have core look for BIOS code in SPI ROM	1 = Enable 0 = disable (default)	Top Swap	USB_C_OC_ODL
GPIO_61	LPSS_UART0_TXD	1.8V	20K PD	20K PU	TXE to bypass ROM in SoC and go to patch space	1 = enable bypass 0 = disable (default)	TXE ROM Bypass	PCHTX_MIPI60RX_UART
GPIO_62	LPSS_UART0_RTS_	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_INT_L
GPIO_65	LPSS_UART2_TXD	1.8V	20K PD	20K PU	TXE to perform DnX for new FW Image over USB.	1 = Force DnX 0 = Do Not Force (default)	DnX FW Load	PCHTX_UART2
GPIO_66	LPSS_UART2_RTS_	1.8V	20K PD	20K PU	LPC Boot BIOS strap	1 = LPC Boot 0 = No LPC Boot (default)	LPC Boot	LTE_OFF_ODL
GPIO_79	LPSS_SPI_0_CLK	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	H1_SLAVE_SPI_CLK_R
GPIO_80	LPSS_SPI_0_FS0	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = No halt (default)	RSVD	H1_SLAVE_SPI_CS_L_R
GPIO_81	LPSS_SPI_0_FS1	1.8V	20K PU	20K PU	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GPIO_81_DEBUG (Boot halt)
GPIO_83	LPSS_SPI_0_TXD	1.8V	20K PD	20K PD	Sets the LPC buffer to 1.8V or 3.3V mode	1 = 1.8V mode 0 = 3.3V mode (default)	LPC Voltage Select	H1_SLAVE_SPI_MOSI_R
GPIO_84	LPSS_SPI_2_CLK	1.8V	20K PU	20K PD	SPI Boot BIOS Strap	1 = Don't SPI Boot (default) 0 = SPI Boot Debug if Secure boot fuse is set to 0	SPI Boot Source	stest_SPI1_CLK_R
GPIO_85	LPSS_SPI_2_FS0	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_SPI_CS_L_R
GPIO_86	LPSS_SPI_2_FS1	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = enable (default)	RSVD	stest_CNTRL
GPIO_87	LPSS_SPI_2_FS2	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	TP_PCH_GPIO_87_PD
GPIO_89	LPSS_SPI_2_TXD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	stest_SPI1_MOSI_R
GPIO_159	AVS_I2S0_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 =Default	RSVD	I2S0_PCH_RX
GPIO_163	AVS_I2S1_WS_SYN	1.8V	20K PD	20K PD	SMBus 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	Buffers 1.8V/3.3V	I2S_SFRM_SPKR
GPIO_164	AVS_I2S1_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	WLAN_PE_RST
GPIO_168	AVS_HDA_SDI	1.8V	20K PD	20K PD	PMU 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	PMU 1.8V/3.3V	I2S2_PCH_RX
GPIO_172	AVS_M_CLK_B1	1.8V	20K PD	20K PD	SMBus No Reboot. Handled by PMC	1 = Enable 0 = disable (default)	SMBus Reboot	DMIC_CLK2_R
GPIO_174	AVS_M_CLK_AB2	1.8V	20K PD	20K PD	VDD2 Voltage Select	1 = 1.24V 0 = 1.20V (default)	VDD2 Voltage	(Open, TP_GPIO_174)
GPIO_175	AVS_M_DATA_2	1.8V	20K PD	20K PD	eSPI vs. LPC	1 = eSPI mode 0 = LPC mode (default)	eSPI/LPC mode	DMIC_CAM2_DATA
GPIO_177	SMB_CLK	1.8V/3.3V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	(Open, TP160)
GPIO_191	CNV_BRI_DT	1.8V	20K PD	None	eSPI Flash Sharing Mode. Set to 0 if GPIO_175 is set to 0	1 = Slave attached Share 0 = Master attached (default)	Flash Sharing	CNVI_BRI_DT_R
GPIO_192	CNV_BRI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_BRI_RSP
GPIO_193	CNV_RGI_DT	1.8V	20K PU	None	RSVD	1 = Normal Operation 0 = Do not use	RSVD	CNVI_RGI_DT_R
GPIO_194	CNV_RGI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_RGI_RSP
GPIO_195	CNV_RF_RESET_B	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_RF_RESET_L
GPIO_196	XTAL_CLKREQ	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	(Not available)