LCFC Confidential

Y540 M/B Schematics Document

NM-C541

Coffee Lake H-Processor with DDR4 + NV N18P-G0 GPU

2019-02-28

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: Cover Page			
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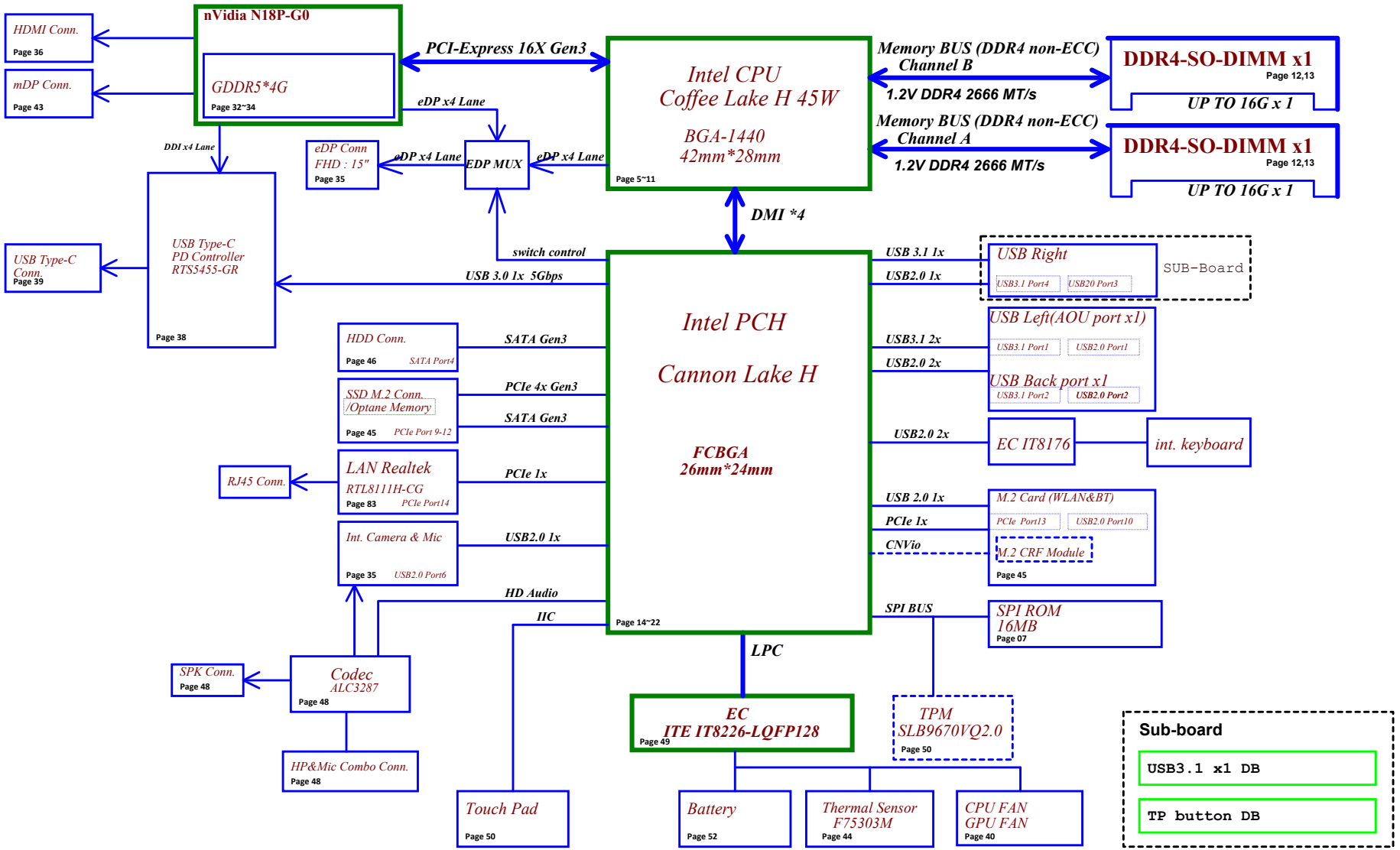

Security Classification	LC Future Center Secret Data		
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Title	Block Diagram		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD NVVDDS +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
AOAC@	AOAC support part
CNVI@	CNVi support part
ME@	ME part(connector, hole)
OPT@	For NV GPU part
OPTANE@	Optane memory support part
TPM@	For support TPM sku part
OPT17@	For NV N17P GPU part
OPT18@	For NV N18P GPU part
NPI@	For NPI use
MP@	For MP use
PS8713@	only mount for PS8713 redriver
CD@	Cost down part

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:8	NA
14	BT
9	AG
10:13	NA

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	NA
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	M.2 SSD Gen3
1B	NA
2	HDD Gen3
3	NA
4	NA
5	NA

PCIE Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15:24	NA

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Title: **Notes List**

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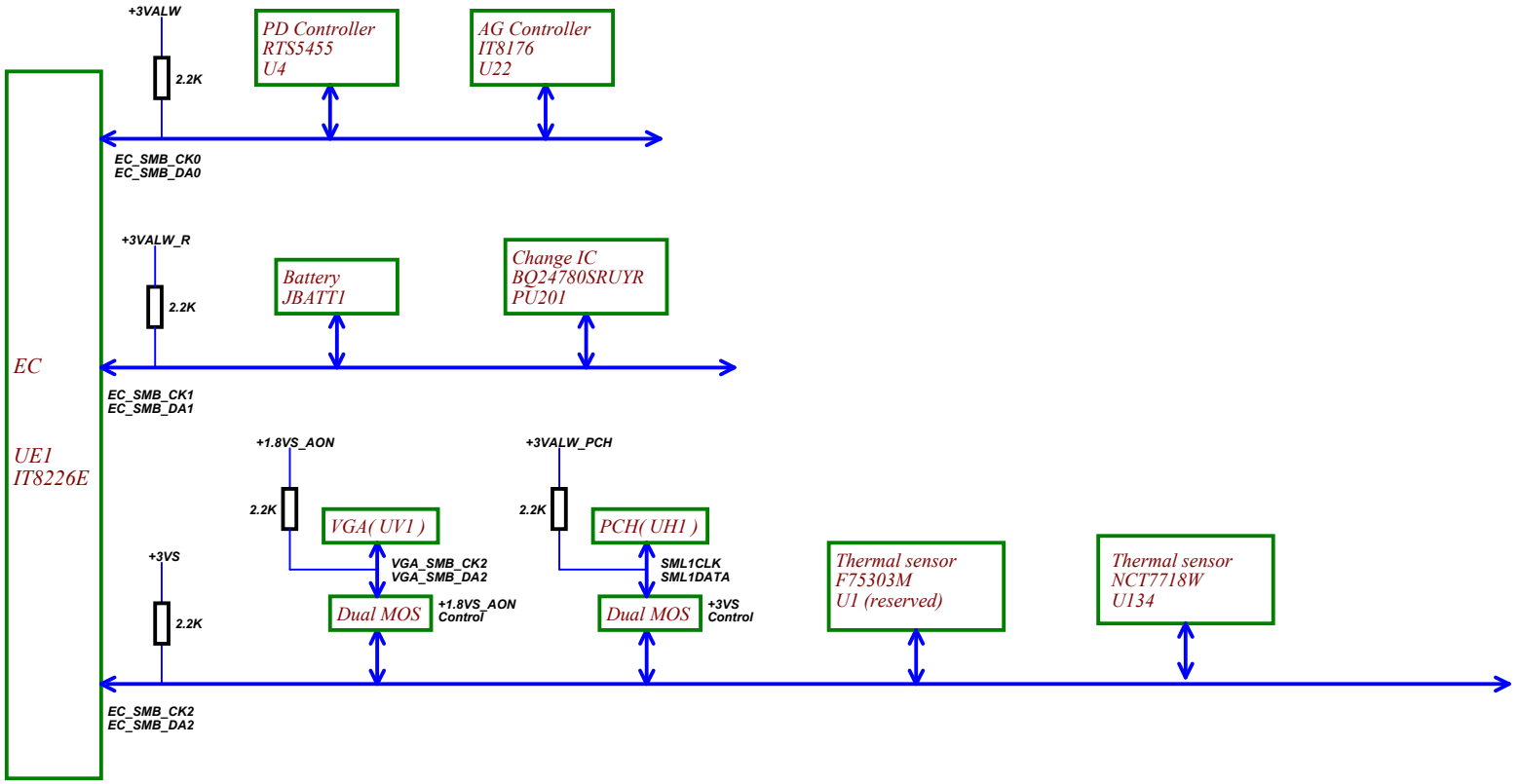

SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS Reserve	X	V +3VALW_PCH	V +3VS	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update
Thermal Sensor NCT7718M	1001100xb

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update

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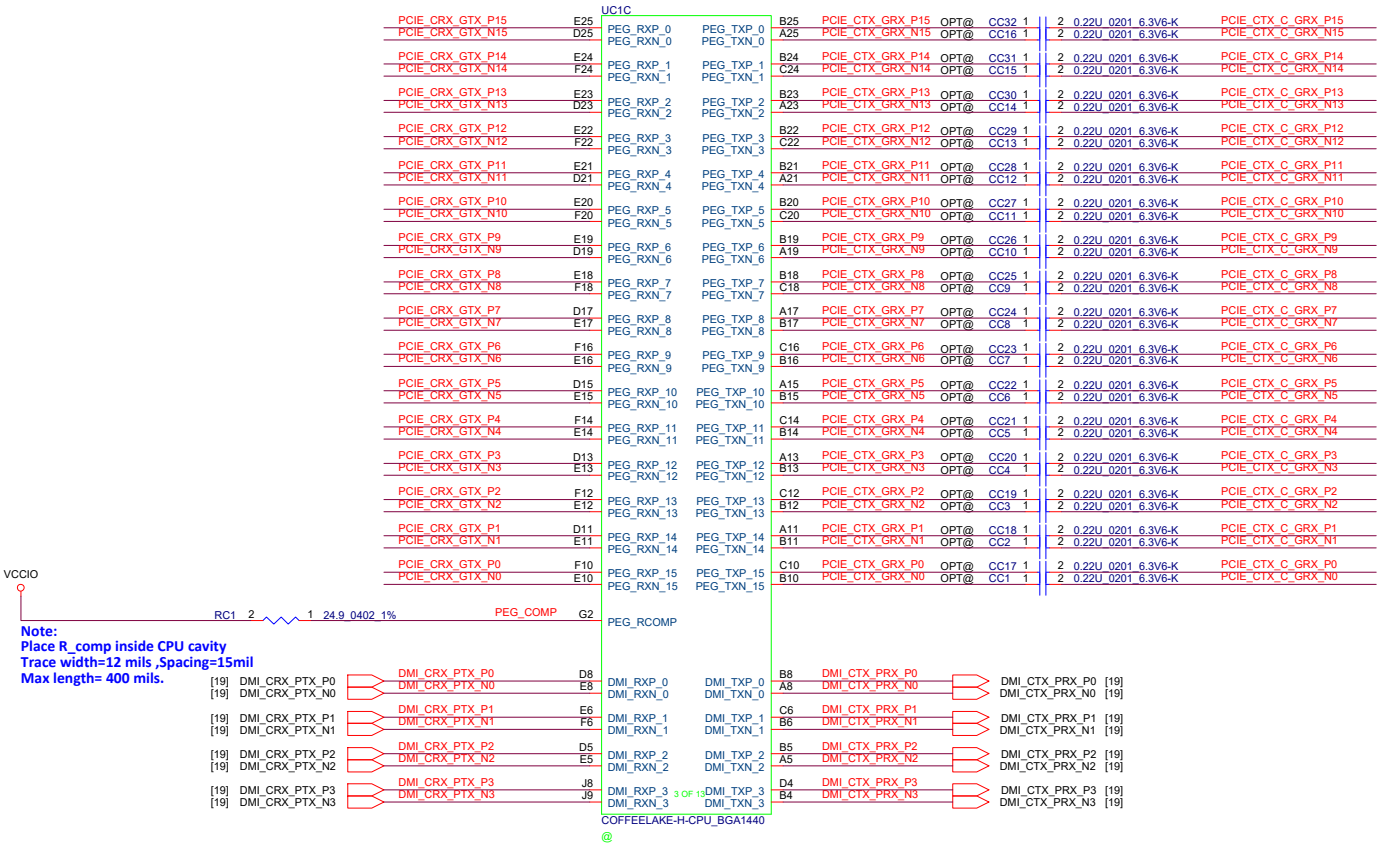
Title: Blank4

[24] PCIE_CRX_GTX_N[0..15]
[24] PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] [24]
PCIE_CTX_C_GRX_P[0..15] [24]



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (1/7) DMI,PEG

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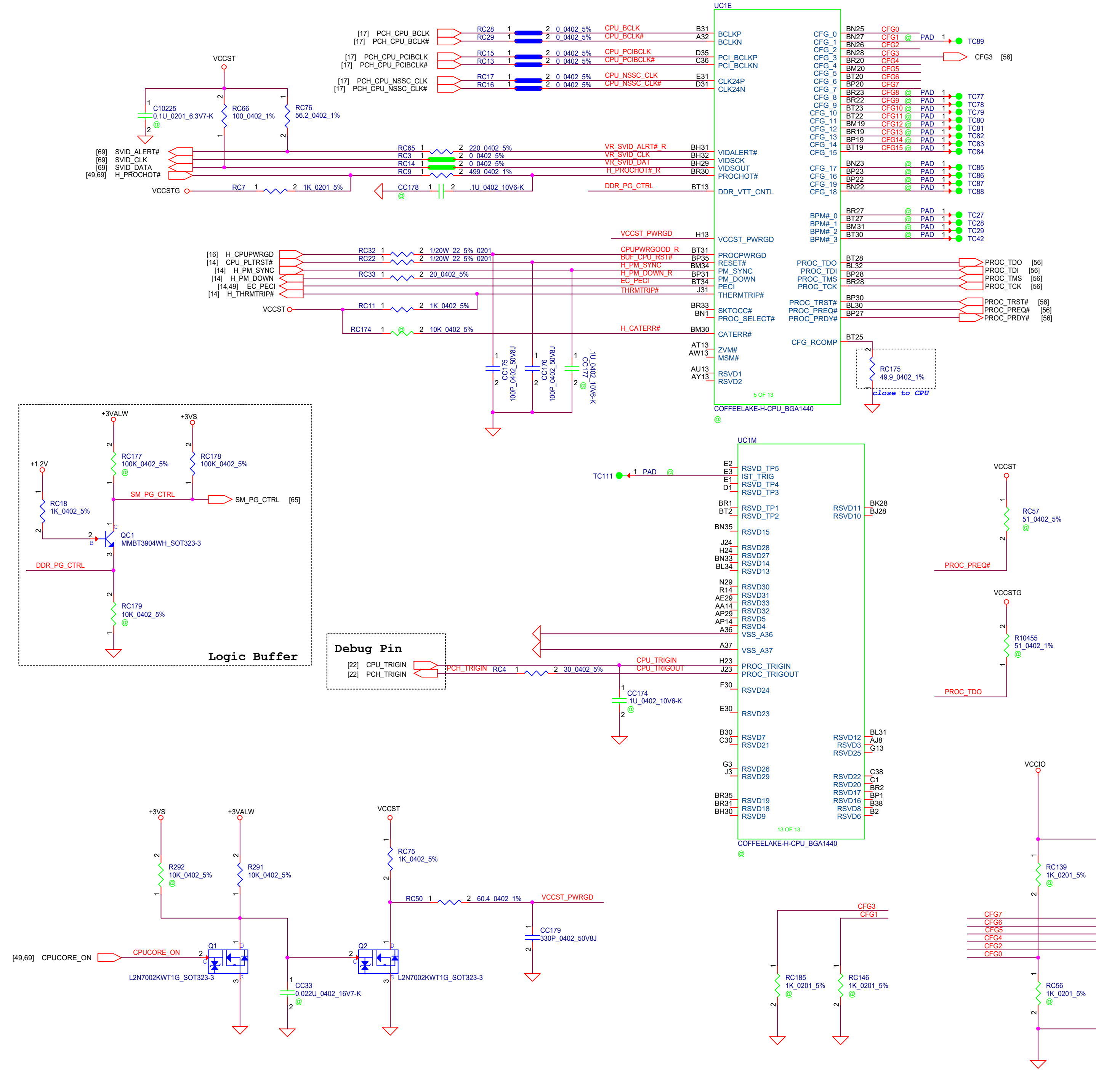
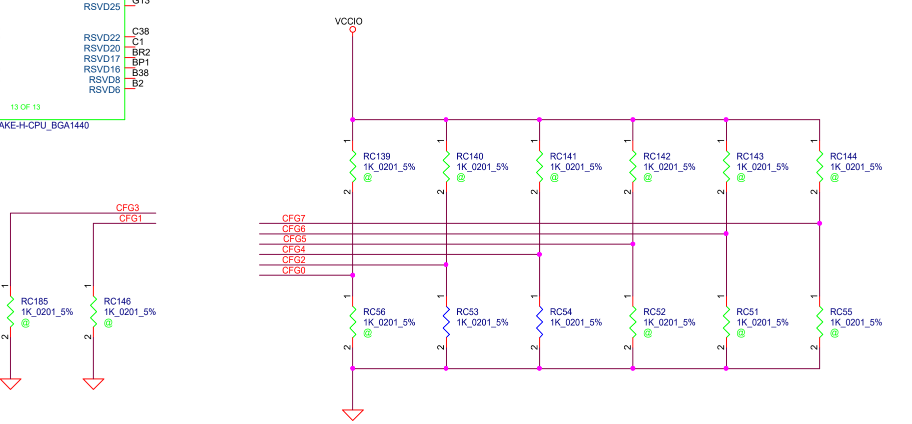


CFG STRAPS for CPU

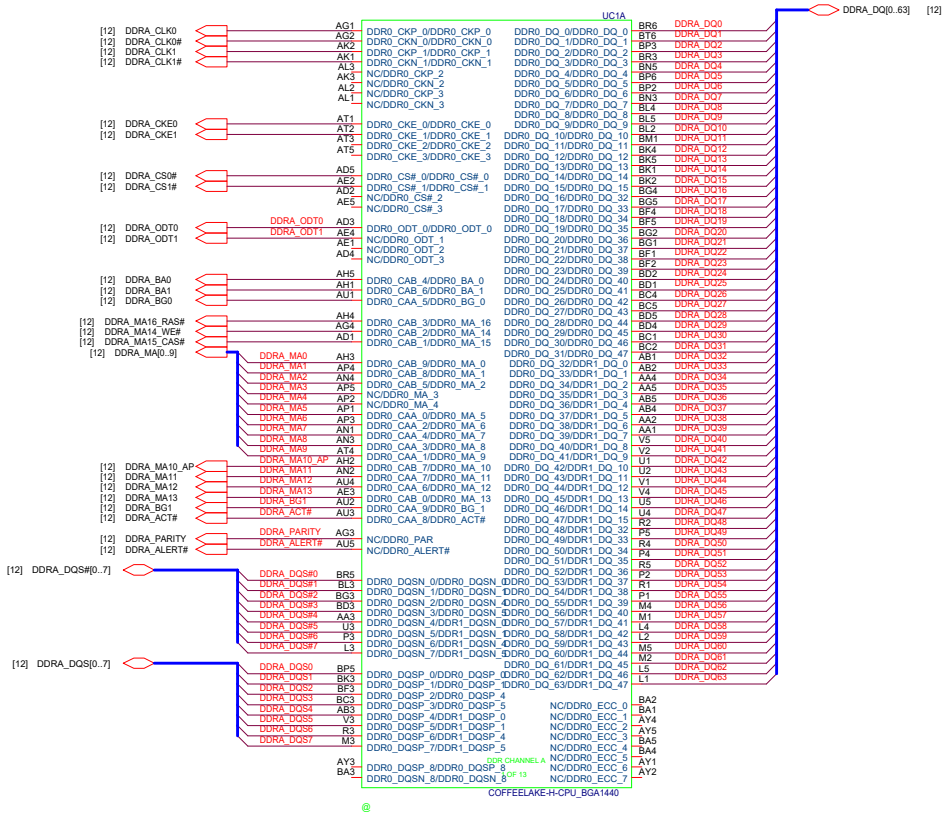
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 (Default) Normal peration; No stall. 0 Stall.
Reserved configuration lane	
CFG1	N/A
PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed
Reserved configuration lane.	
CFG3	N/A
eDP enable	
CFG4	1 Disabled. * 0 Enabled.
PCI Express* Bifurcation	
CFG[6:5]	00 1 x8, PCI press* 01 reserved 10 x8 PCI press* * 11 1 x16 PCI press*
PEG Training	
CFG7	* 1 (default) PEG Train immediately following RESET# deassertion. 0 PEG Wait for BIOS for training.
Reserved configuration lane	
CFG[19:8]	N/A

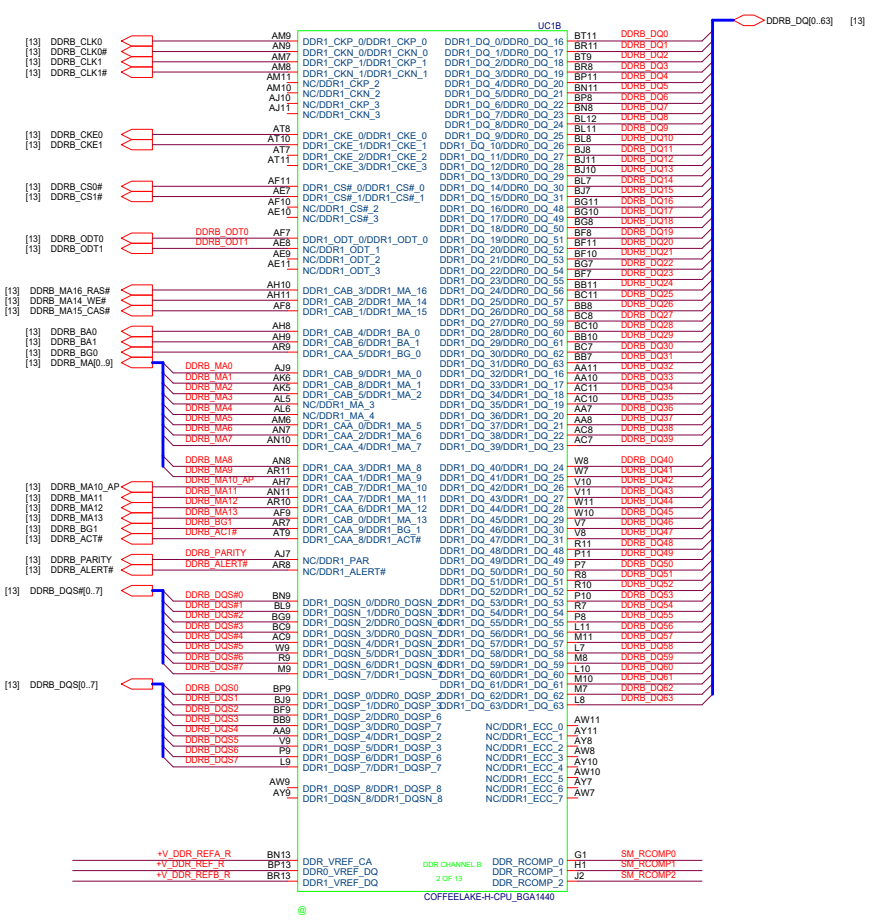


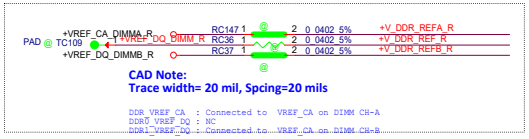
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (2/7) PM, XDP, CLK, CFG

Size: Custom | Document Number: Y540 | Rev: 0.1







DDR4 COMPENSATION SIGNALS

Security Classification	LC Future Center Secret Data		
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Title: *CPU (3/7) DDRVI*

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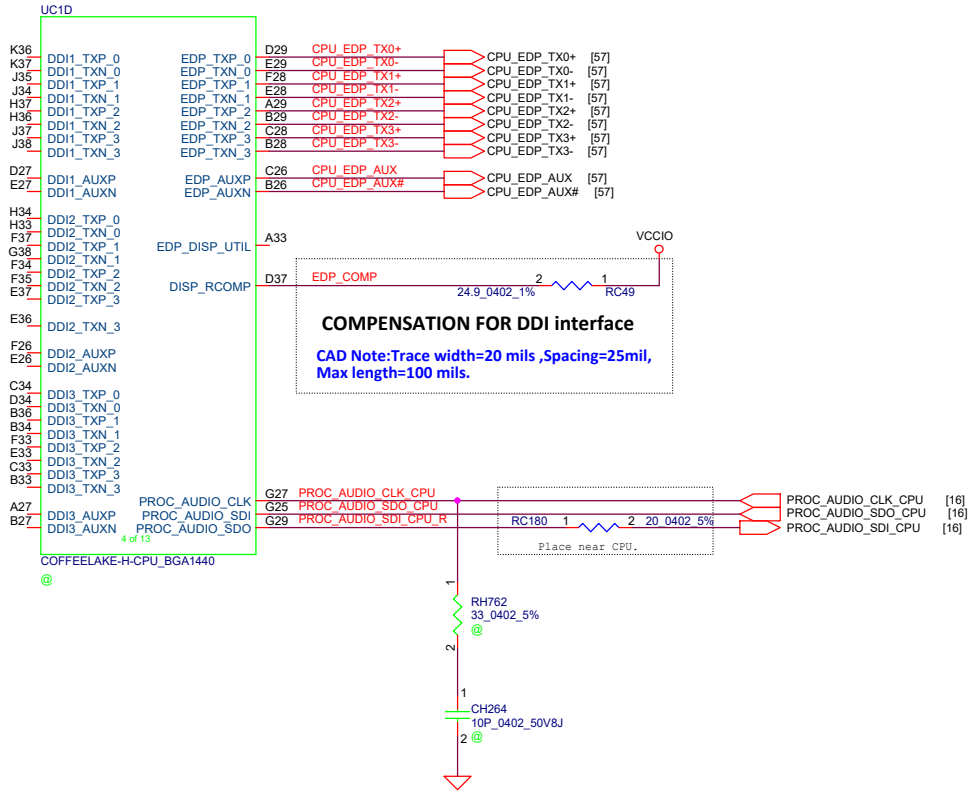

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **CPU (4/7) eDP, DDI**

Size	Document Number	Rev
A3	Y540	0.1

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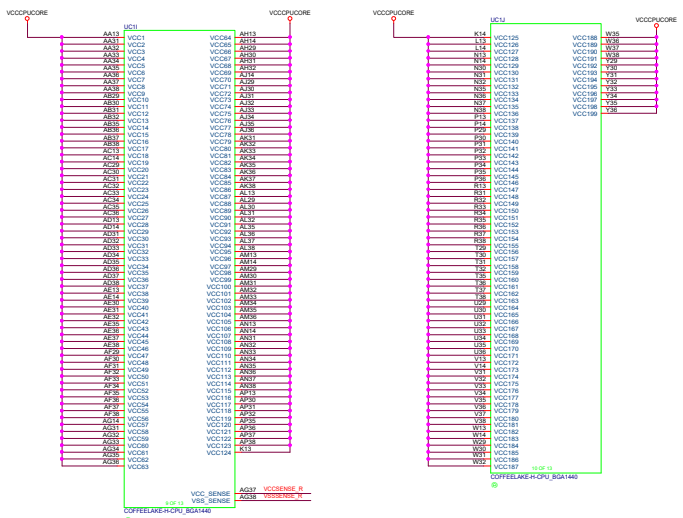

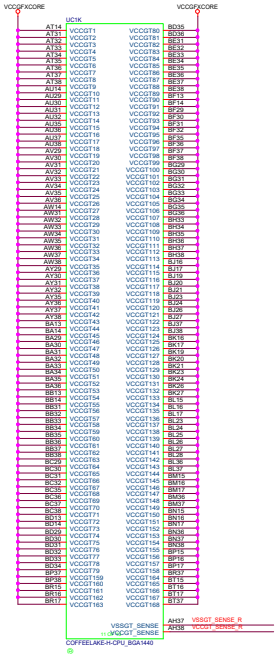

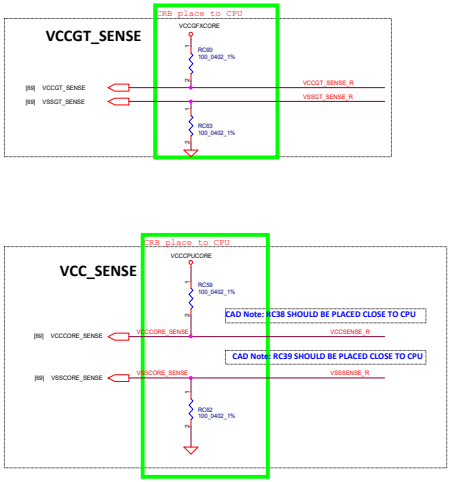

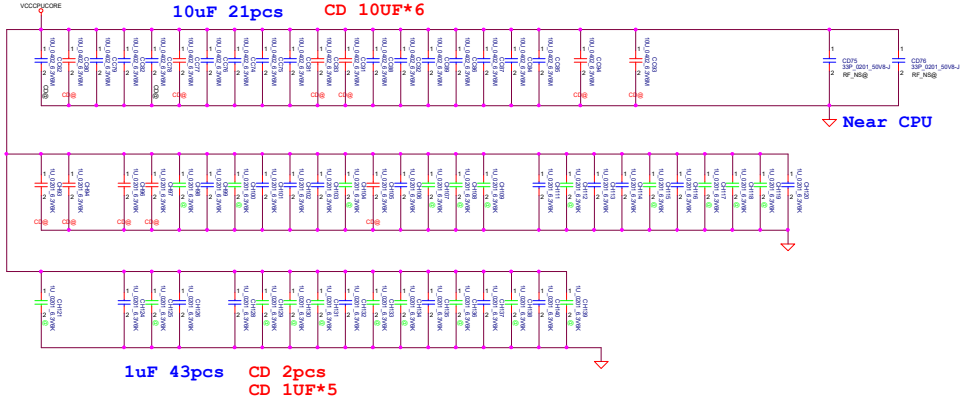

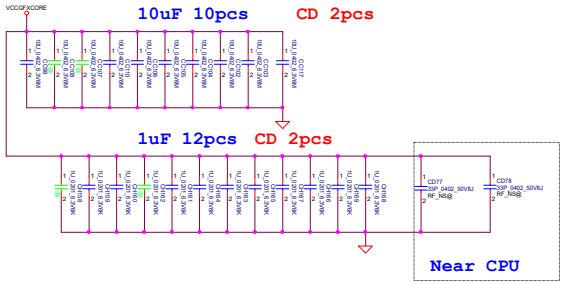

Security Classification	LC Future Center Secret Data		Title: CPU (5/7) PWR, BYPASS
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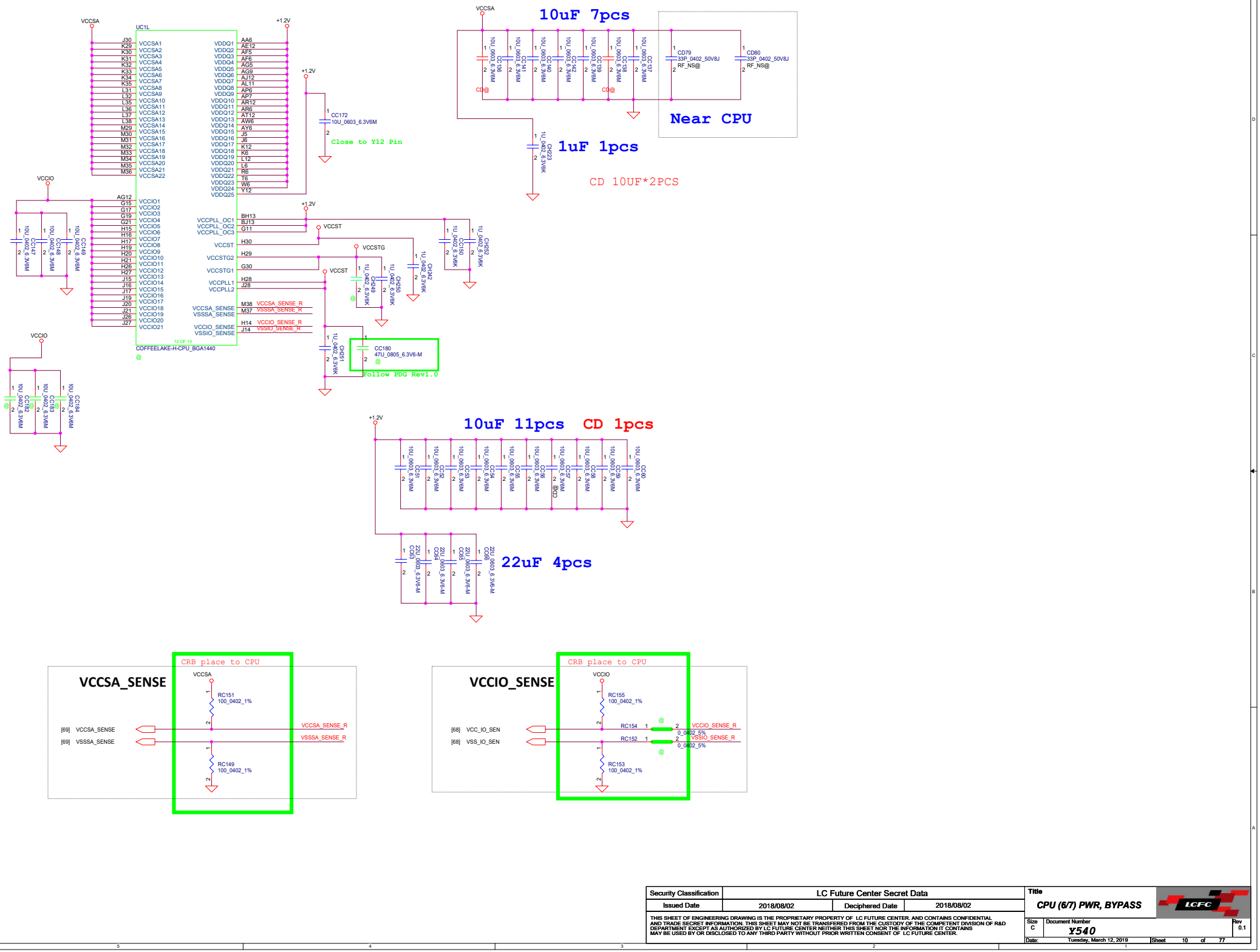

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	CPU (6/7) PWR, BYPASS		
Size C	Document Number Y540		Rev 0.1
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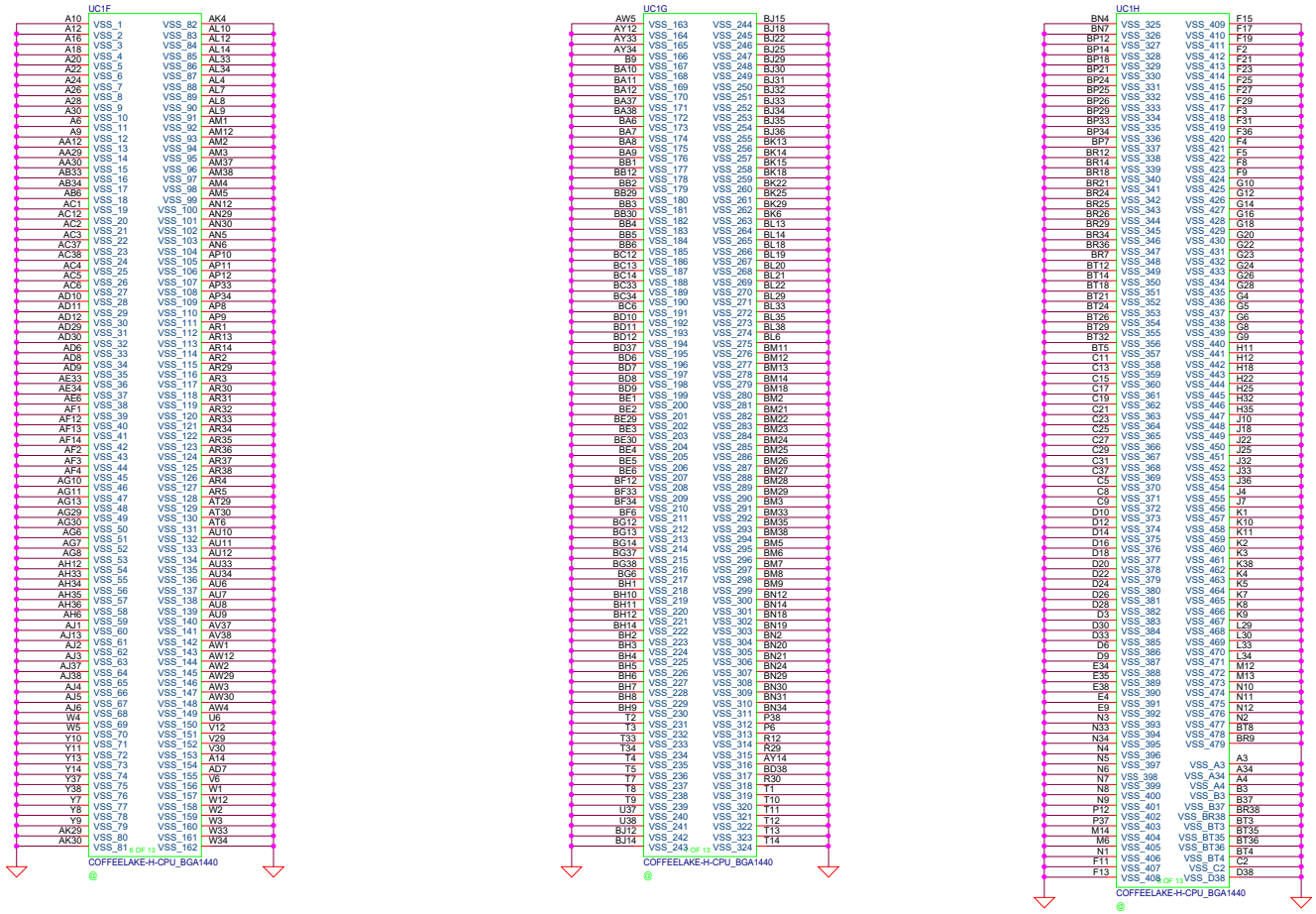

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (6/7) PWR, VSS

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C	Y540	0.1

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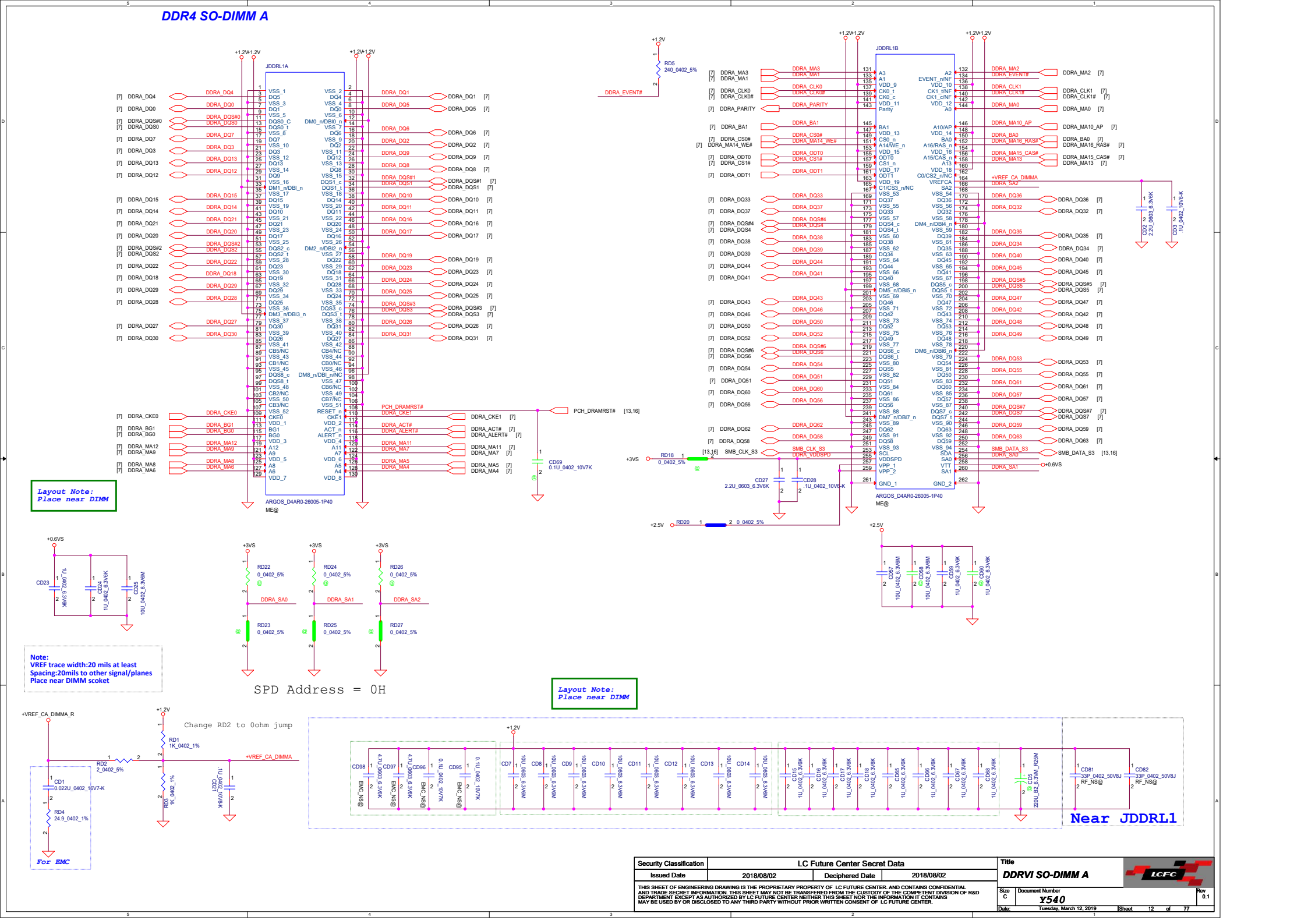
DDR4 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDRVI SO-DIMM A		
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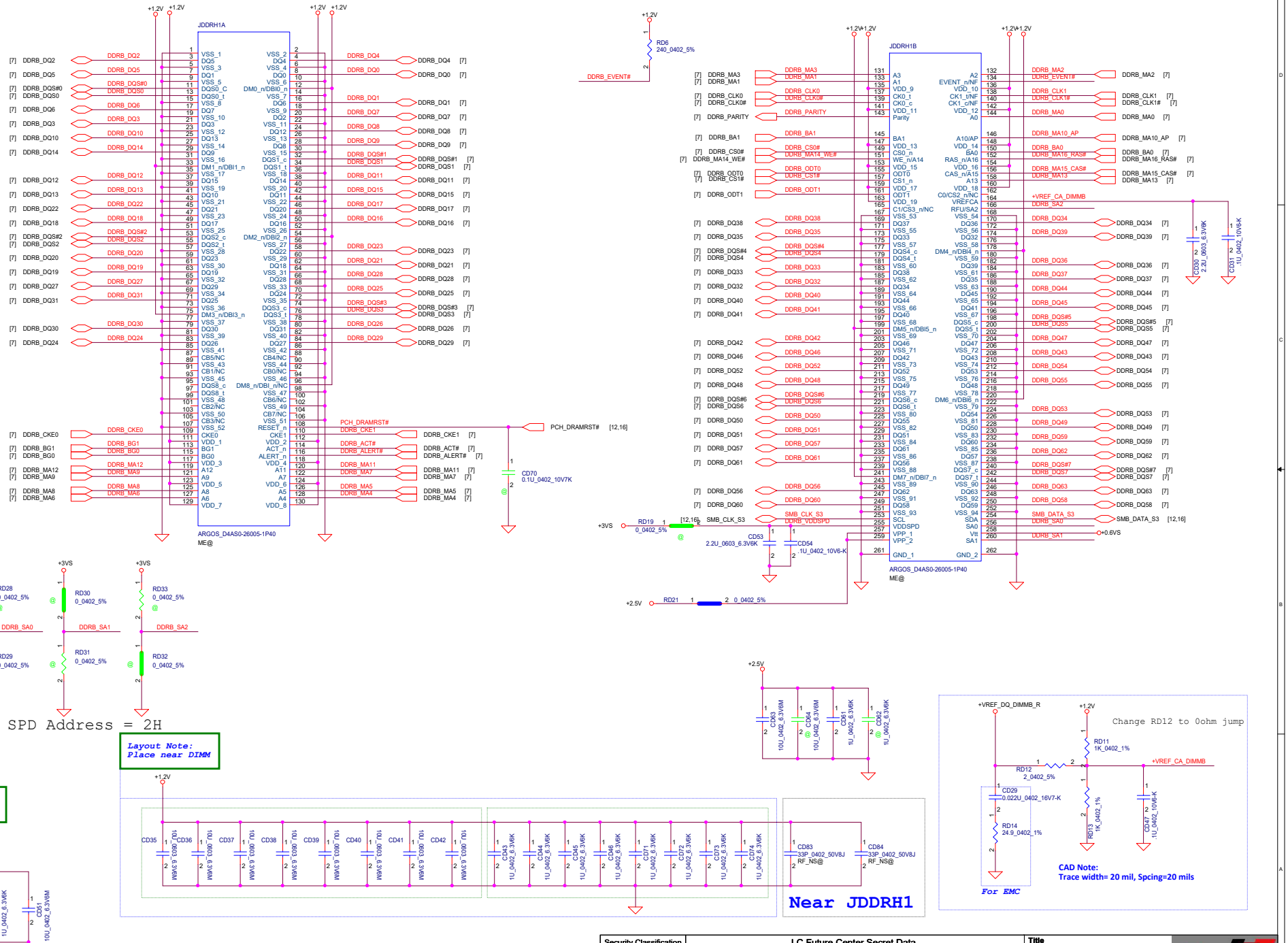
DDR4 SO-DIMM B



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDRVI SO-DIMM B		
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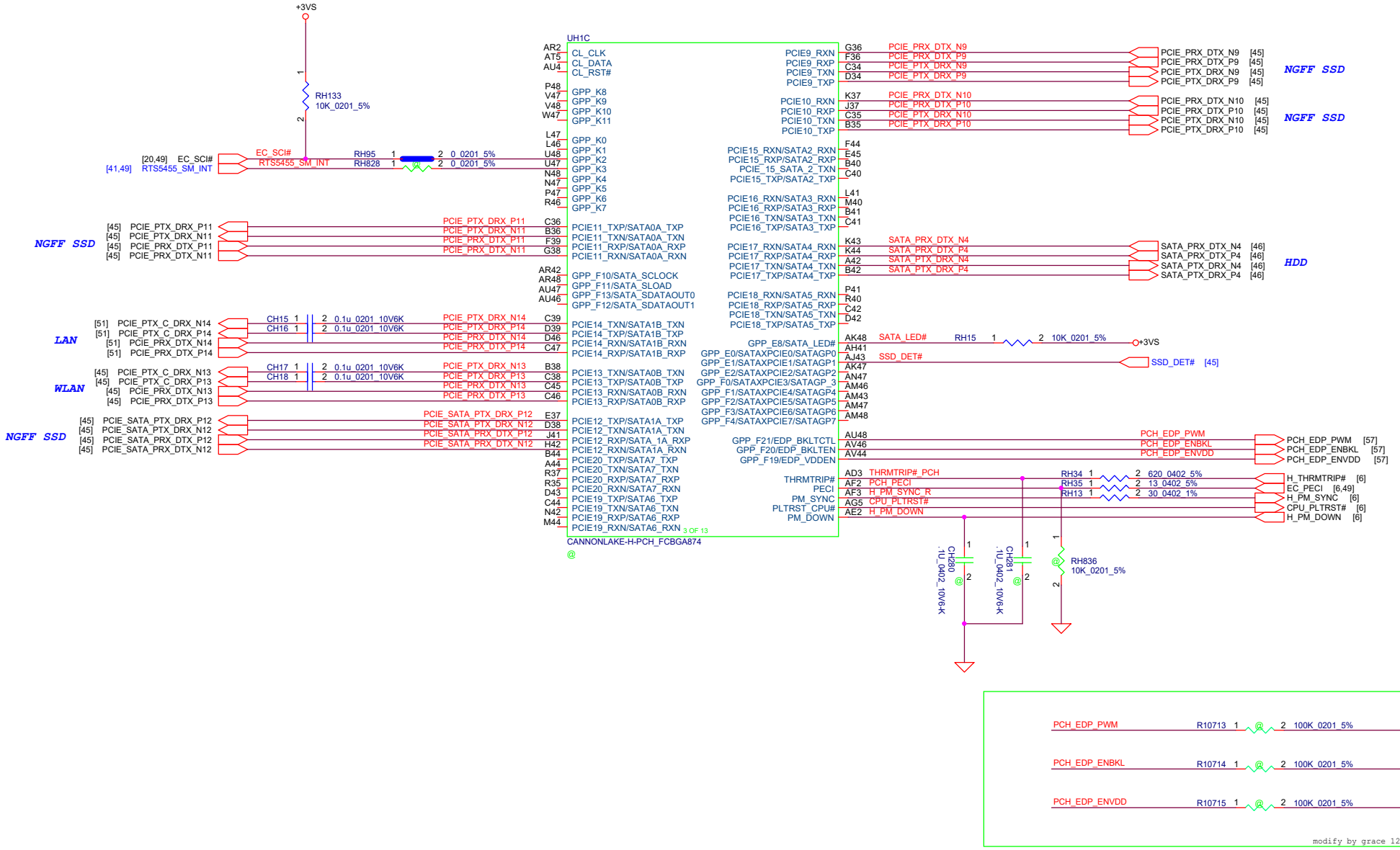

Security Classification	LC Future Center Secret Data		
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Title: PCH (1/9) PCIe/SATA/GPPFG

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NEED close to PCH

EMC_NS@ 33P_0201_50V8-J 2 — 1 CH296 LPC_AD3
EMC_NS@ 33P_0201_50V8-J 2 — 1 CH293 LPC_AD2
EMC_NS@ 33P_0201_50V8-J 2 — 1 CH294 LPC_AD1
EMC_NS@ 33P_0201_50V8-J 2 — 1 CH295 LPC_AD0

HuiH request Reserved Cap 11/12

HM370 only have 4(#1-#4) USB3.1 GEN2 port

Back USB (3.0)

TYPE-C USB (3.0)

LEFT USB (3.0) MB(AOU)

Right USB (3.0) DB

UH1F

[48] USB30_TX_N1 → USB30_TX_N1 → F9 USB31_1_TXN
[48] USB30_TX_P1 → USB30_TX_P1 → F7 USB31_1_TXP
[48] USB30_RX_N1 → USB30_RX_N1 → D11 USB31_1_RXN
[48] USB30_RX_P1 → USB30_RX_P1 → C11 USB31_1_RXP

[40] TYPE-C_USB3_TX_N2 → TYPE-C_USB3_TX_N2 → C3 USB31_2_TXN
[40] TYPE-C_USB3_TX_P2 → TYPE-C_USB3_TX_P2 → D4 USB31_2_TXP
[40] TYPE-C_USB3_RX_N2 → TYPE-C_USB3_RX_N2 → B9 USB31_2_RXN
[40] TYPE-C_USB3_RX_P2 → TYPE-C_USB3_RX_P2 → C9 USB31_2_RXP

C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP

C15 USB31_5_TXN
B15 USB31_5_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP

[47] USB30_TX_P3 → USB30_TX_P3 → G12 USB31_3_TXP
[47] USB30_TX_N3 → USB30_TX_N3 → F11 USB31_3_TXN
[47] USB30_RX_P3 → USB30_RX_P3 → C10 USB31_3_RXP
[47] USB30_RX_N3 → USB30_RX_N3 → B10 USB31_3_RXN

[50] USB30_TX_P4 → USB30_TX_P4 → C14 USB31_4_TXP
[50] USB30_TX_N4 → USB30_TX_N4 → B14 USB31_4_TXN
[50] USB30_RX_P4 → USB30_RX_P4 → J15 USB31_4_RXP
[50] USB30_RX_N4 → USB30_RX_N4 → K16 USB31_4_RXN

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GPP_A1/LAD0/ESPI_IO0 — BB39 LPC_AD0_R — RH128 1 2 0_0201_5% → LPC_AD0 [49]
GPP_A2/LAD1/ESPI_IO1 — AW37 LPC_AD1_R — RH130 1 2 0_0201_5% → LPC_AD1 [49]
GPP_A3/LAD2/ESPI_IO2 — AV37 LPC_AD2_R — RH131 1 2 0_0201_5% → LPC_AD2 [49]
GPP_A4/LAD3/ESPI_IO3 — BA38 LPC_AD3_R — RH132 1 2 0_0201_5% → LPC_AD3 [49]

+3VS
RH104 10K_0201_5%
RH113 10K_0201_5%

GPP_A5/LFRAME#/ESPI_CS0# — BE38 LPC_FRAME# → LPC_FRAME# [49]
GPP_A6/SERIRQ/ESPI_CS1# — AW35 SERIRQ → SERIRQ [49]
GPP_A7/PIRQA#/ESPI_ALERT0# — BA36 → TPM_SPI_IRQ# [50]
GPP_A0/RCIN#/ESPI_ALERT1# — BE39 KBRST# → KBRST# [49]
GPP_A14/SUS_STAT#/ESPI_RESET# — BF38

GPP_A9/CLKOUT_LPC0/ESPI_CLK — BB36 CLK_PCI_EC_R — RH84 1 2 22_0402_5% → CLK_PCI_EC → CLK_PCI_EC [49]
GPP_A10/CLKOUT_LPC1 — BB34

For LPC_CLK
R: 0Ω to 2Ω

GPP_K19/SMI# — T48 PCH_SMI# — RH821 1 @ 2 0_0201_5% → EC_SMI# [49]
GPP_K18/NMI# — T47 — RH129 1 @ 2 10K_0201_5% → +3VS

CH265 33P_0402_50V8J EMC@

AH40
GPP_E6/SATA_DEVSLP2 — AH35 DEVSLP1 → DEVSLP1 [45] *NGFF SSD*
GPP_E5/SATA_DEVSLP1 — AL48
GPP_E4/SATA_DEVSLP0 — AP47
GPP_F9/SATA_DEVSLP7 — AN37
GPP_F8/SATA_DEVSLP6 — AN46
GPP_F7/SATA_DEVSLP5 — AR47
GPP_F6/SATA_DEVSLP4 — AP48
GPP_F5/SATA_DEVSLP3

Change DEVSLP to SATA Port1 by Bing 0621
H: Sleep Mode
L: Active Mode

CANNONLAKE-H-PCH_FCBGA874
@

UH1E

[41] TYPE-C_DP_HPD → RH23 1 2 0_0201_5% → AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
[44] HDMI_HPD → RH26 1 2 0_0201_5% → AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
[43] DP_HPD → RH27 1 2 0_0201_5% → AP9 GPP_I2/DDPD_HPD2/DISP_MISC2
[45] CNVI_EN# → CNVI_EN# → AL15 GPP_I3/DPPE_HPD3/DISP_MISC3

GPP_I5/DDPB_CTRLCLK — AL13 DDPB_CLK — PAD1 @IT37
GPP_I6/DDPB_CTRLDATA — AR8 DDPB_DATA
GPP_I7/DDPC_CTRLCLK — AN13 DDPC_CLK — PAD 1 @IT28
GPP_I8/DDPC_CTRLDATA — AL10 DDPC_DATA
GPP_I9/DDPD_CTRLCLK — AL9 DDPD_CLK — PAD 1 @IT36
GPP_I10/DDPD_CTRLDATA — AR3 DDPD_DATA
GPP_F23/DDPF_CTRLDATA — AN40
GPP_F22/DDPF_CTRLCLK — AT49

GPP_F14/EXT_PWR_GATE#/PS_ON# — AP41

[57] PCH_EDP_HPD → PCH_EDP_HPD → AN6 GPP_I4/EDP_HPD/DISP_MISC4

R10712 @ 100K_0201_5%

GPP_K23/IMGCLKOUT1 — M45
GPP_K22/IMGCLKOUT0 — L48
GPP_K21 — T45
GPP_K20 — T46
GPP_H23/TIME_SYNC0 — AJ47

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CANNONLAKE-H-PCH_FCBGA874
@

+3VS
DDPB_DATA — RH834 1 @ 2 2.2K_0201_5%
DDPC_DATA — RH33 1 @ 2 2.2K_0201_5%
DDPD_DATA — RH835 1 @ 2 2.2K_0201_5%

DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
* L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
* L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
* L Port D is not detected. (Default)

Security Classification	LC Future Center Secret Data		
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Title: PCH (2/9) USB3/GPPAEFGHI

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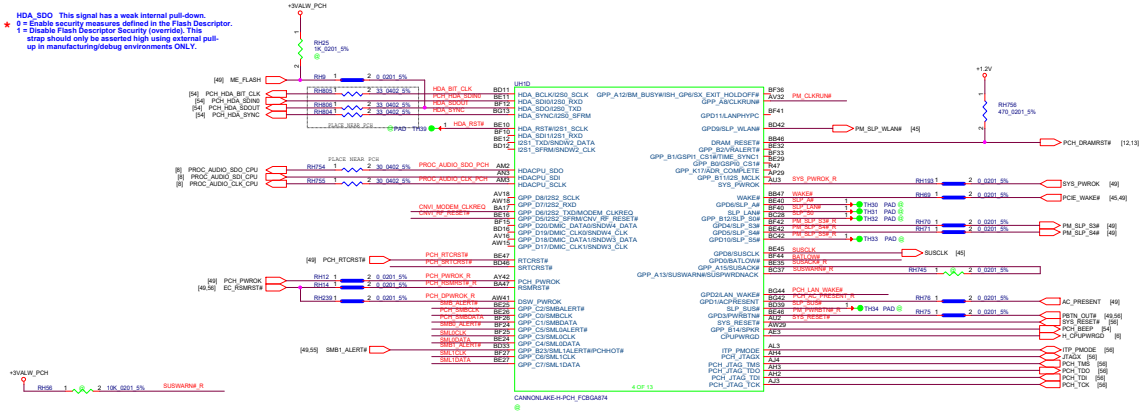
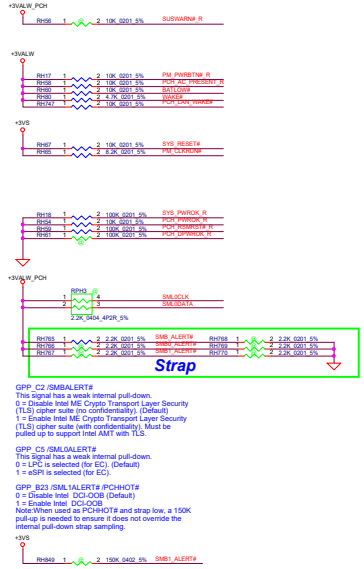
HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

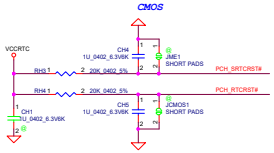


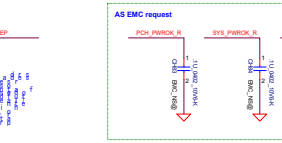


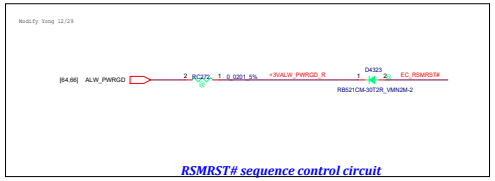
GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

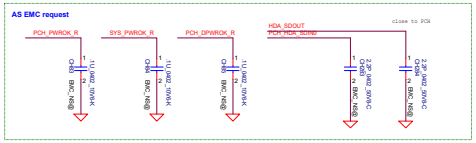
GPP_C5 /SML0ALERT#
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

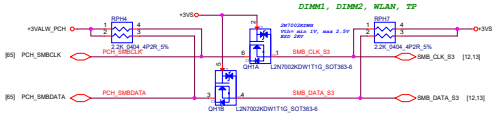
GPP_B23 /SML1ALERT# /PCHHOT#
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Note:When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

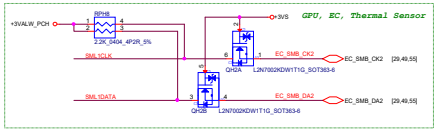


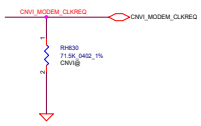


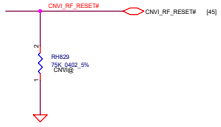






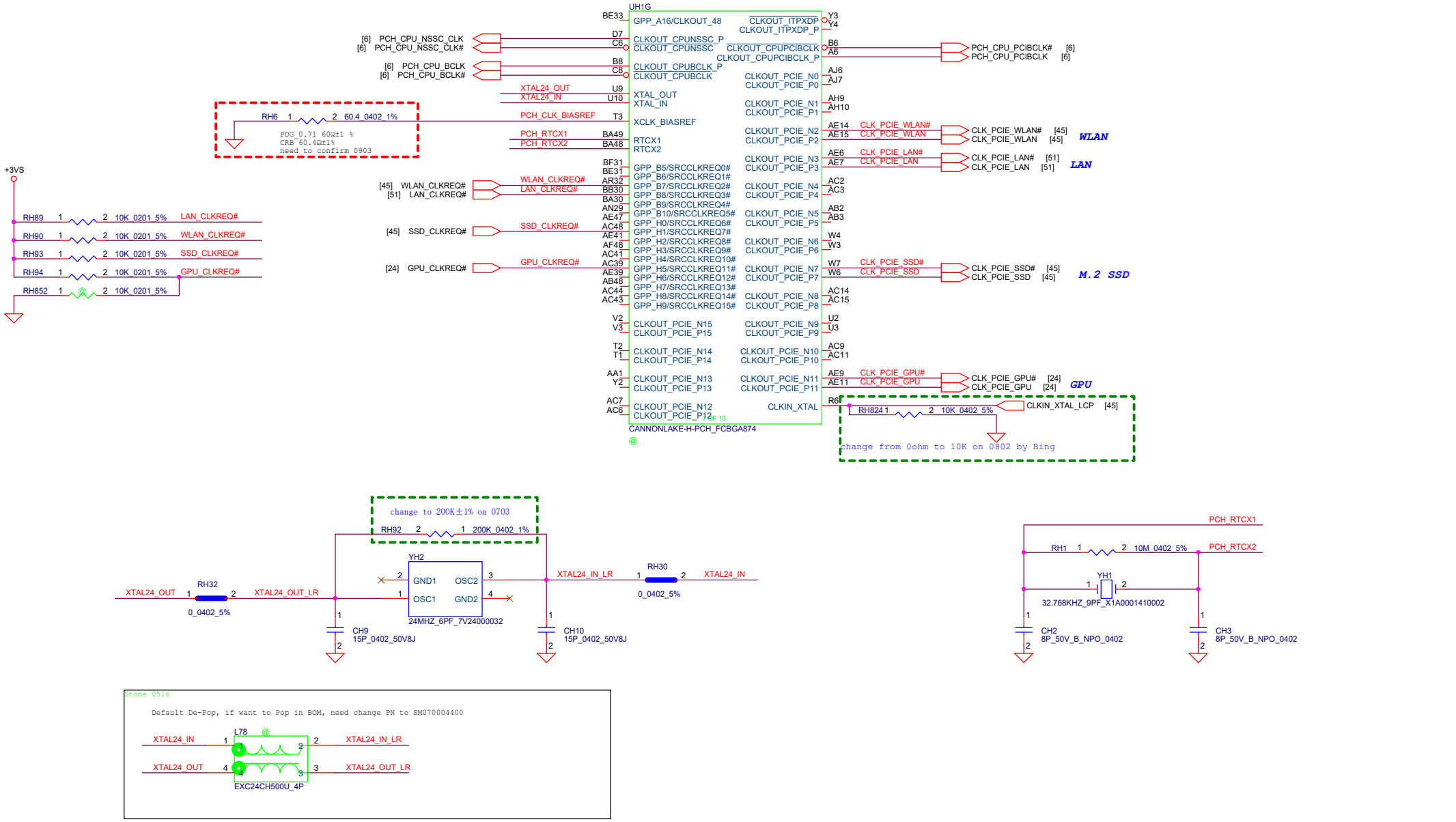






Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PCH (3/9) HDA,RTC,SMBUS,PM		
Size D	Document Number Y540		Rev 0.1
Date: Tuesday, March 12, 2019		Sheet 16 of 77	

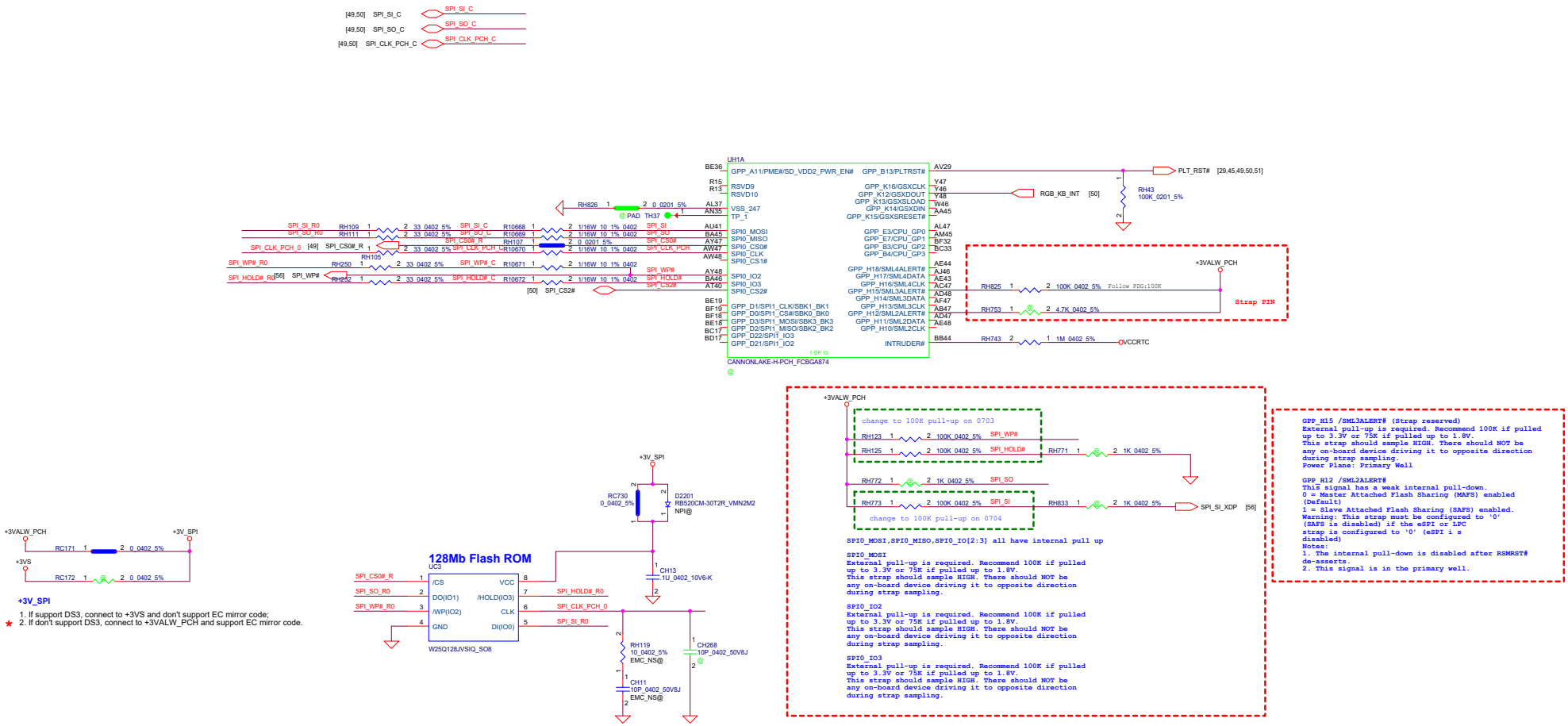


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PCH (3/9) CLOCK,GPPBH**

Size	Document Number	Rev
A3	Y540	0.1

Date: Tuesday, March 12, 2019 Sheet 17 of 77



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
A2	Y540	0.1

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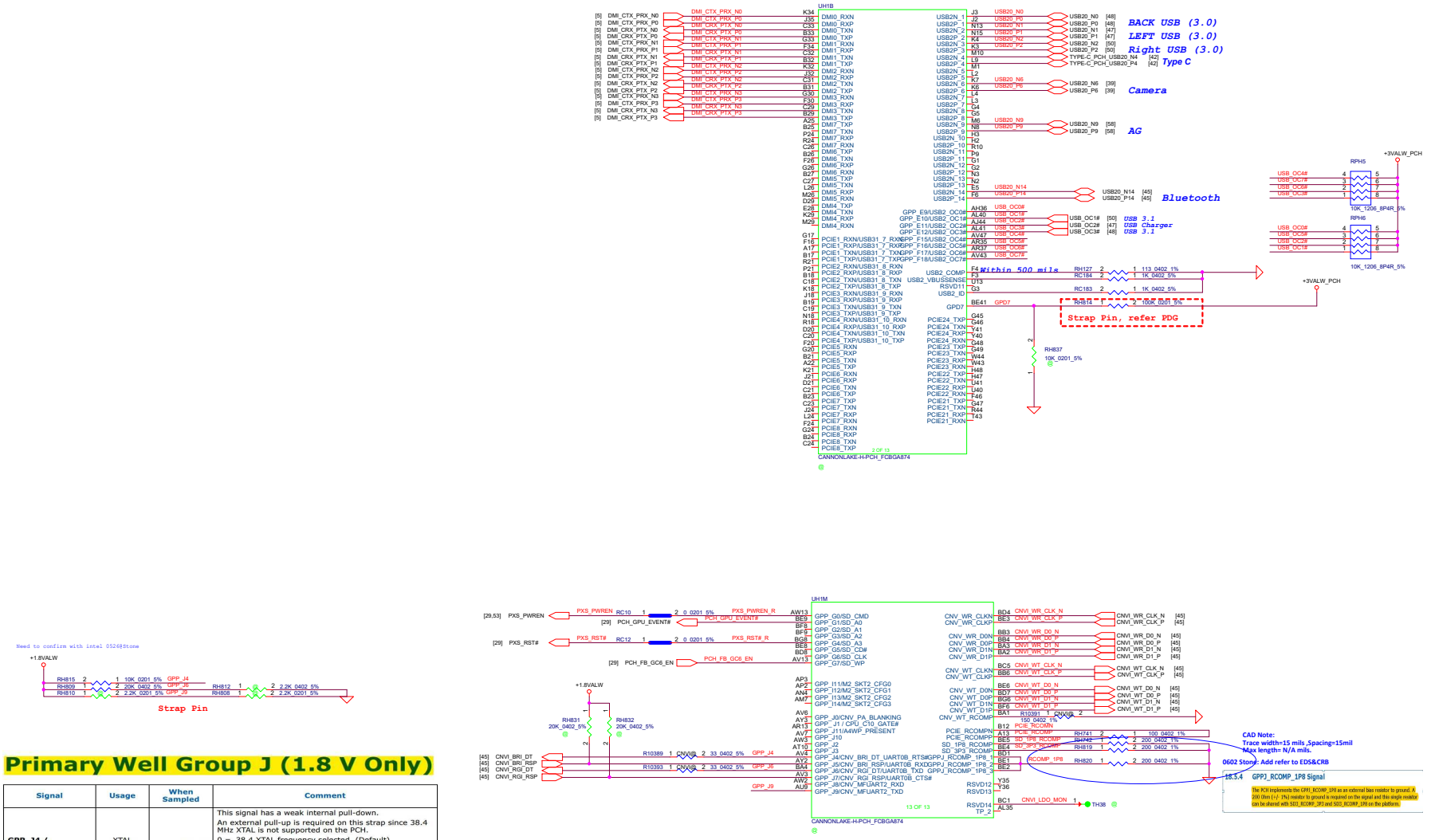

Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Blank		
Size: Custom	Document Number: Y540		Rev: 0.1
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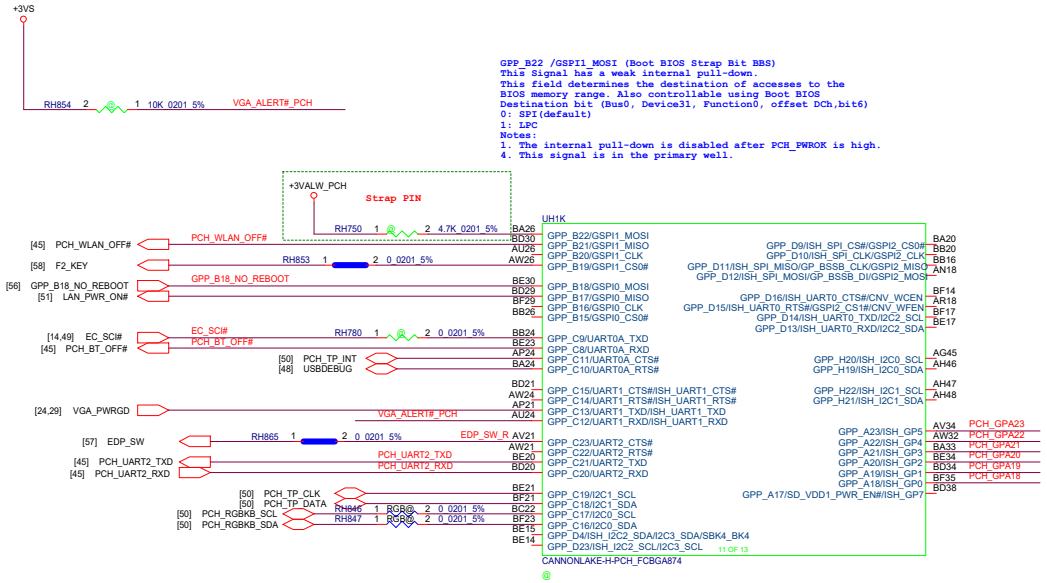
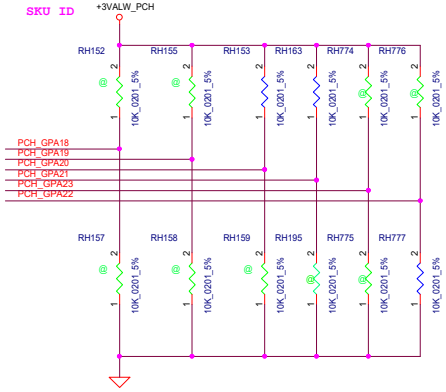
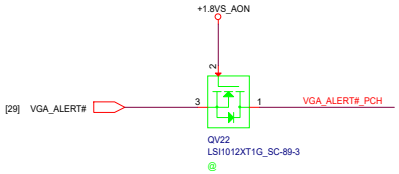
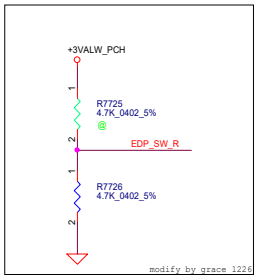


Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC







01/09: GPA22 add for MUX sku

Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22	PCH_GPA23
Y540-15-N17P MUX	0	0	0	0	0	x
Y540-15-N18E G0 MUX	0	0	0	1	0	x
Y540-15-N18E G1 MUX	0	0	1	0	0	x
Y540-15-N18P MUX	0	0	1	1	0	x
Y7000P-15-N17P MUX	0	1	0	0	0	x
Y7000P-15-N18E G0 MUX	0	1	0	1	0	x
Y7000P-15-N18E G1 MUX	0	1	1	0	0	x
Y7000P-15-N18P MUX	0	1	1	1	0	x
Y540-17-N17P MUX	1	0	0	0	0	x
Y540-17-N18E G0 MUX	1	0	0	1	0	x
Y540-17-N18E G1 MUX	1	0	1	0	0	x
Y540-17-N18P MUX	1	0	1	1	0	x

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (6/9) GPPPABCD, I2C

Size	Document Number	Rev
C	Y540	0.1

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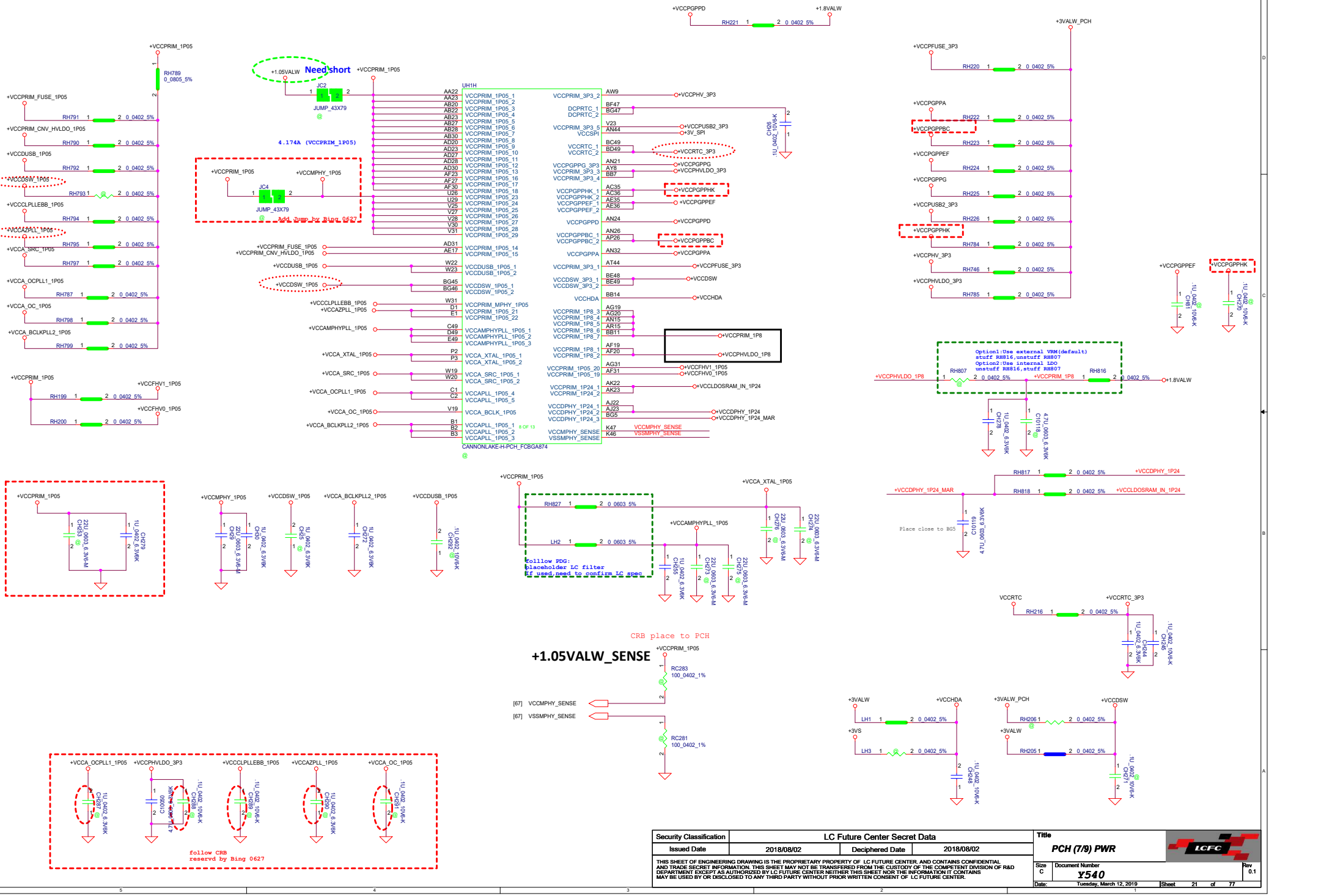

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (7/9) PWR

Size	Document Number	Rev
C	Y540	0.1

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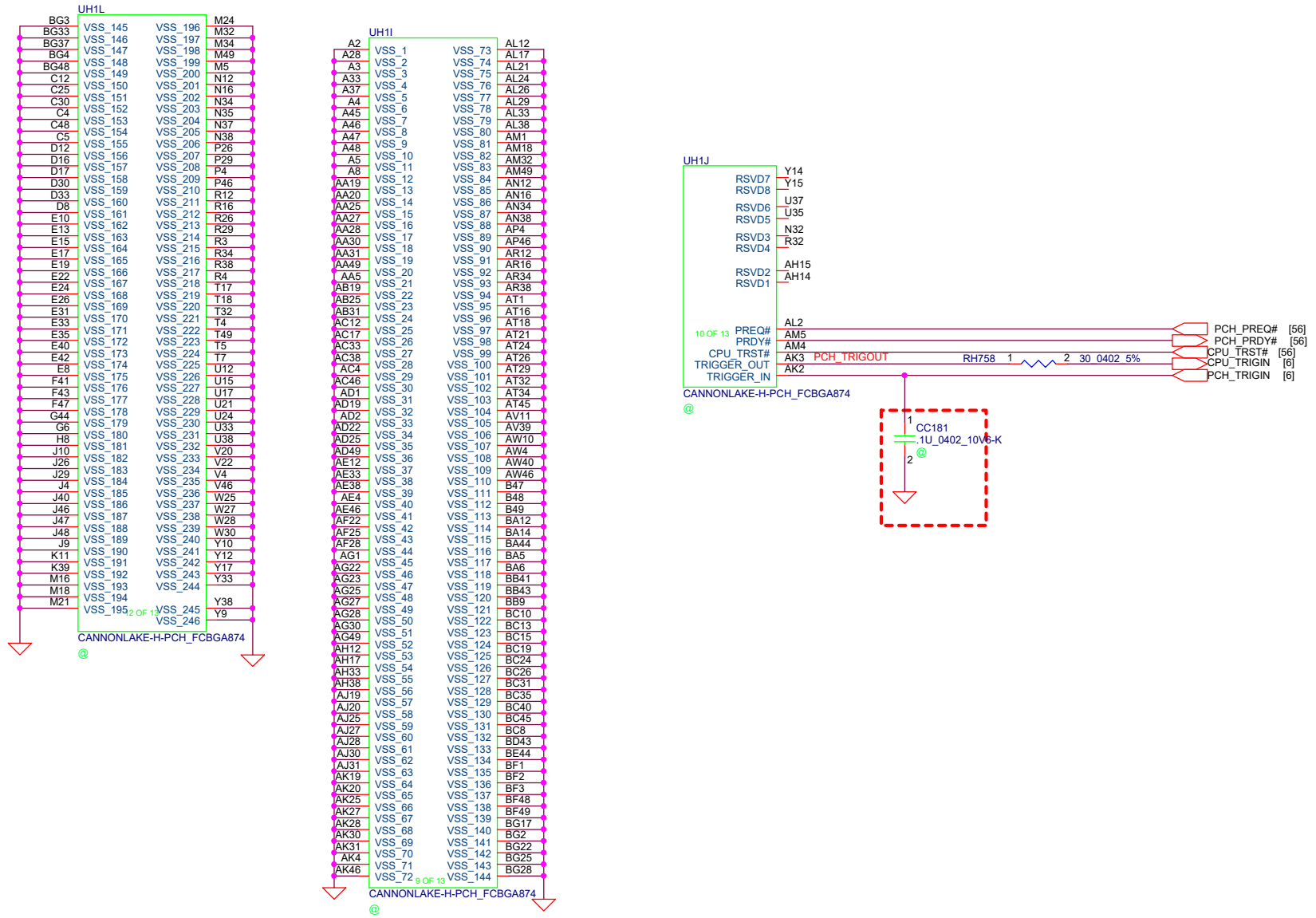

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (9/9) VSS

Size	Document Number	Rev
B	Y540	0.1

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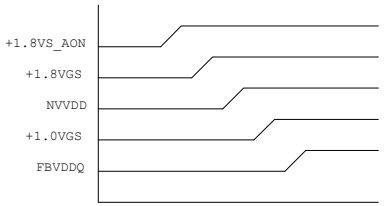
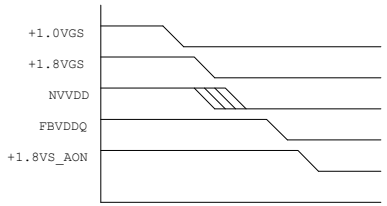
N18P-G0 GPIO

GPIO	I/O	N18P GPIO Name	N17P GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	GC6:GC6_FB_EN	GC6 FRAME BUFFER ENABLE	FB_GC6_EN	(10K pull down)
GPIO2	IN	GC6:GPU_EVENT*	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K pull High)
GPIO3	OUT	UNUSED	NVVDDS_PWM	UNUSED	UNUSED	
GPIO4	OUT	GC6:1V8_MAIN_EN	GC6:1V8_MAIN_EN	GPU power sequencing for GC6 --- 1V8_MAIN_EN	V8_MAIN_EN	(10K pull High)
GPIO5	IN	FRAME_LOCK*	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(10K pull High)
GPIO7	OUT	LCD_BL_PWM	LCD_BL_PWM	LCD Panel Backlight PWM	UNUSED	
GPIO8	OUT	MEM_VDD_CTL	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K pull down)
GPIO9	I/O	THERM_ALERT*	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K pull High)
GPIO10	OUT	MEM_VREF_CTL	MEM_VREF_CTL	Memory VREF Control	MEM_VREF	(10K pull down)
GPIO11	OUT	LCD_VCC	LCD_VCC	LCD Panel VOLTAGE	UNUSED	
GPIO12	IN	PWR_LEVEL	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K pull High)
GPIO13	OUT	UNUSED	LCD back light EN	UNUSED	UNUSED	
GPIO14	IN	HPD_IFPA*	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K pull High)
GPIO15	IN	HPD_IFPB*	HPD_IFPB*	Hot Plug Detect for IFPB	UNUSED	
GPIO16	OUT	UNUSED	UNUSED	UNUSED	UNUSED	
GPIO17	IN	HPD_IFPD*	HPD_IFPD*	Hot Plug Detect for IFPD	UNUSED	
GPIO18	IN	HPD_IFPE*	HPD_IFPE*	Hot Plug Detect for IFPE	IFPE_HPD	(10K pull High)
GPIO19	OUT	Reserved	3D VISION	UNUSED	UNUSED	
GPIO20	OUT	GC6:NB_FGC6	unused	Low Power States Fast CG6	NB_FGC6	(10K pull down)
GPIO21	OUT	LCD_BLEN	unused	LCD Panel Backlight Enable	UNUSED	
GPIO22		INA_HT*/ADC_MUX_SEL	unused	OVRM MUX SEL	ADC_MUX_SEL_R	(10K pull High)
GPIO23		UNUSED	UNUSED	UNUSED	RASTER_SYNC1	(100K pull down)
GPIO24		UNUSED	UNUSED	UNUSED	UNUSED	
GPIO25	OUT	FBVDD_PSI	unused	Turns off phases of the Frame buffer power supply	UNUSED	(5.1K pull High)
GPIO26		FP_FUSE	unused	Field-programming of select fuses	GPIO26_FP_FUSE	(10K pull down)
GPIO27	IN	HPD_IFPC*	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K pull High)

N18E-G1 Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. Delay from 1V8_MAIN_EN to PEXVDD/NVVDD_PGOOD must NOT exceed 4ms.
3. It is recommended that the delay from 1V8_AON on to PEXVDD/NVVDD_PGOOD assertion not exceed 20ms.
4. Power up NVVDD must be 90% before PEXVDD can start ramp-up.
5. All 3.3V devices that connect to the GPU must be powered after 1V8_AON;GPU cannot have any 3.3V leakage paths before 1V8_AON is present.
6. Refer to the JEDEC Memory SPEC for memory-related power sequencing.
7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6



1. PEXVDD must power down before NVVDD,
2. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed
3. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.
4. Power down of PEXVDD must be less than 10% before NVVDD can start ramp-down..

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

VRAM CFG Table

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	N18P-G0 VRAM
L	L	L	0 (0x0000)	?
L	L	H	1 (0x0001)	?
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

FS_OVERT# function only N18P

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	L	FS_OVERT# function ENABLE
L	L	H	FS_OVERT# function DISABLED Reserved; do not configure
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

Strap pin function differences between N17P &N18P

Strap pin	N18P	N17P
ROM_SI	FS_OVERT* NEED PULL LOW	SOR_EXPOSED[3..0]
ROM_SO		
ROM_CLK		
STRAP5	SMB_ALT_ADDR DEVID_SEL PCIE_CFG VGA_DEVICE	SMB_ALT_ADDR DEVID_SEL PCIE_CFG VGA_DEVICE
STRAP4		
STRAP3		
STRAP2	RAMCFG[4:0]	RAMCFG[4:0]
STRAP1		
STRAP0		

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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Title: *N18E VGA Notes List*

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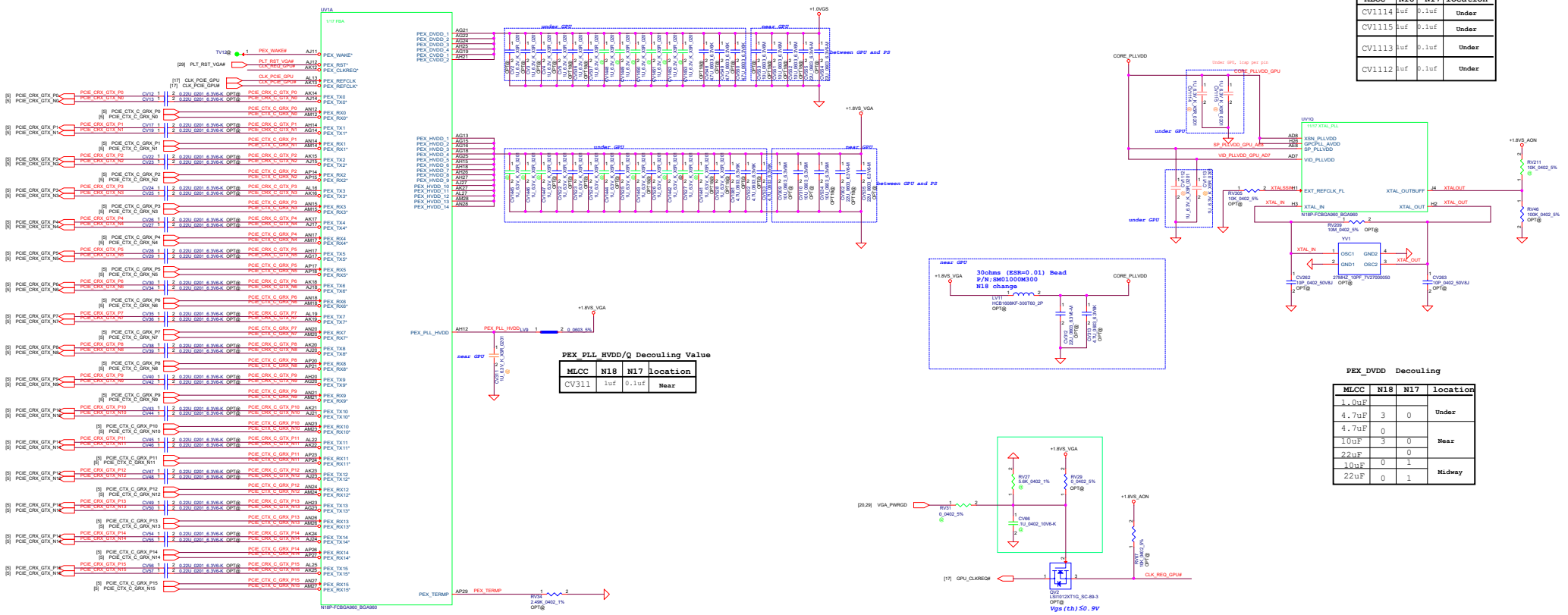
UV1A
1/17 FBA
N18P-FCBGA960_BGA960
PEX_WAKE#
PLT_RST_VGA#
CLK_PCIE_GPU
CLK_PCIE_GPU#
PEX_PLL_HVDD
PEX_TERMP
RV34 2.49K_0402_1% OPT@
under GPU
near GPU
between GPU and PS
+1.8VGS
+1.8VS_VGA
PEX_PLL_HVDD/Q Decoupling Value
MLCC N18 N17 location
CV311 1uf 0.1uf Near
Core_PLLVDD Decouling Value
MLCC N18 N17 location
CV1114 1uf 0.1uf Under
CV1115 1uf 0.1uf Under
CV1113 1uf 0.1uf Under
CV1112 1uf 0.1uf Under
CORE_PLLVDD
UV1Q
1/17 XTAL_PLL
XTAL_OUTBUFF
XTAL_IN
XTAL_OUT
N18P-FCBGA960_BGA960
RV211 10K_0402_5%
RV146 100K_0402_5%
30ohms (ESR=0.01) Bead
P/N:SM01000M300
N18 change
LV11 HCB1608KF-300T80_2P
PEX_DVDD Decouling
MLCC N18 N17 location
1.0uF Under
4.7uF 3 0
4.7uF 0 Near
10uF 3 0
22uF 0
10uF 0 1 Midway
22uF 0 1
VGA_PWRGD
GPU_CLKREQ#
CLK_REQ_GPU#
QV23 LBSS12XT1G_SC-89-3
Vgs(th)≤0.9V
choose one
For SWG mode
OVERT#_NVEN
WRST# [49]
QV24A LBSS138DW1T1G_SOT363-6
QV24B LBSS138DW1T1G_SOT363-6
QV16 LBSS139WT1G_SC70-3
+1.0VGS Discharge
QV14 LBSS139WT1G_SC70-3
QV15 AO3402_SOT-23-3
Vgs(th)≤1.5V
u dated by bing.gu 20180308
Security Classification
LC Future Center Secret Data
Issued Date 2018/08/02
Deciphered Date 2018/08/02
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N16P-GX_PEG I/F
Size D
Document Number
Y540
Rev 0.1
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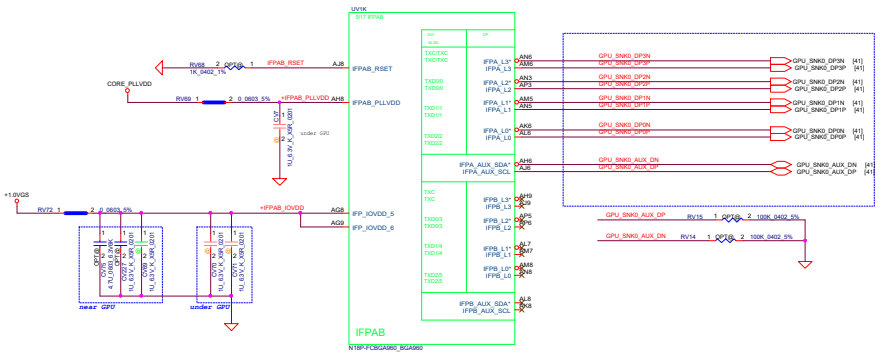
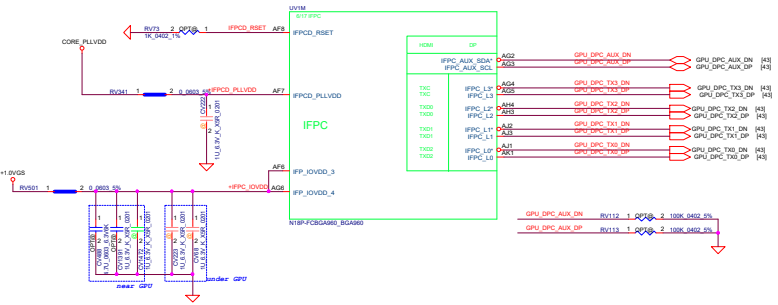
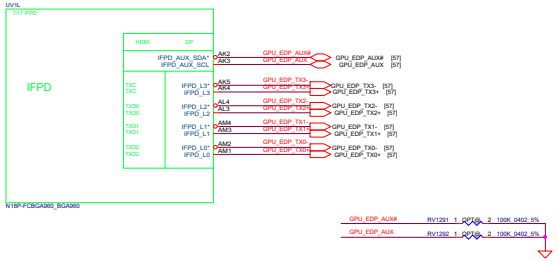


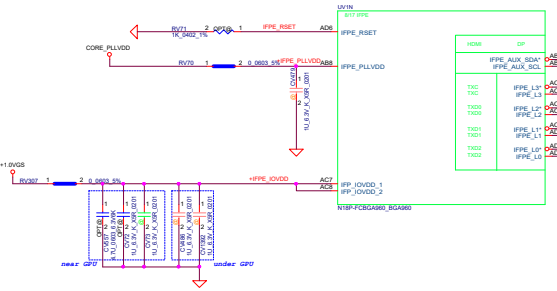
for Type-C DP



Decouling Value

MLCC	N18	N17	location
CV7	1uf	0.1uf	Under
CV222	1uf	0.1uf	Under
CV479	1uf	0.1uf	Under
CV70	1uf	0.1uf	Under
CV71	1uf	0.1uf	Under
CV223	1uf	0.1uf	Under
CV68	1uf	0.1uf	Under
CV486	1uf	0.1uf	Under
CV1392	1uf	0.1uf	Under





HDMI CLK
HDMI D0
HDMI D1
HDMI D2

For HDMI

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N16P-GX_DIGITAL OUT I/F
Size	D
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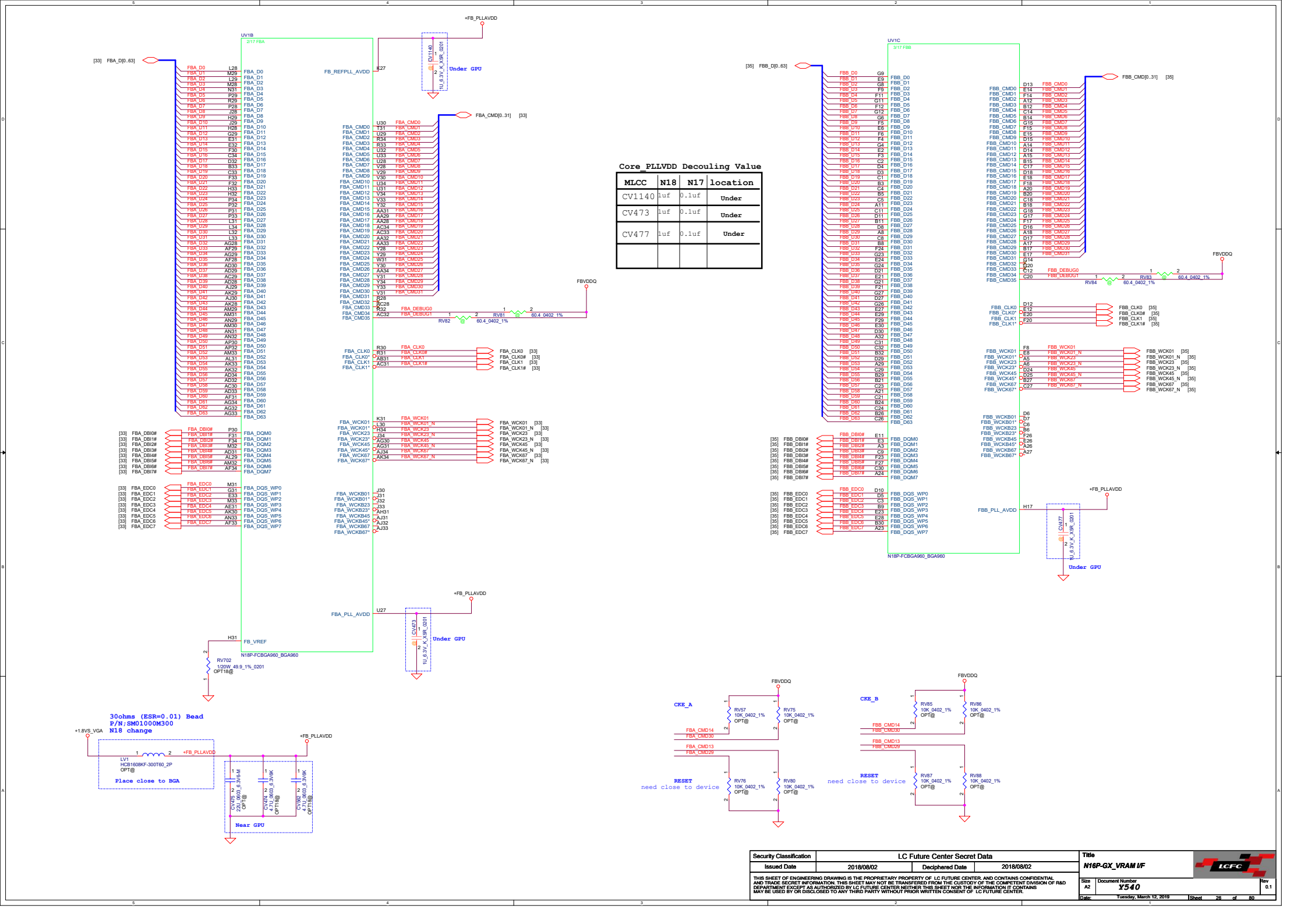

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N16P-GX_VRAM I/F

Size: A2 | Document Number: Y540 | Rev: 0.1

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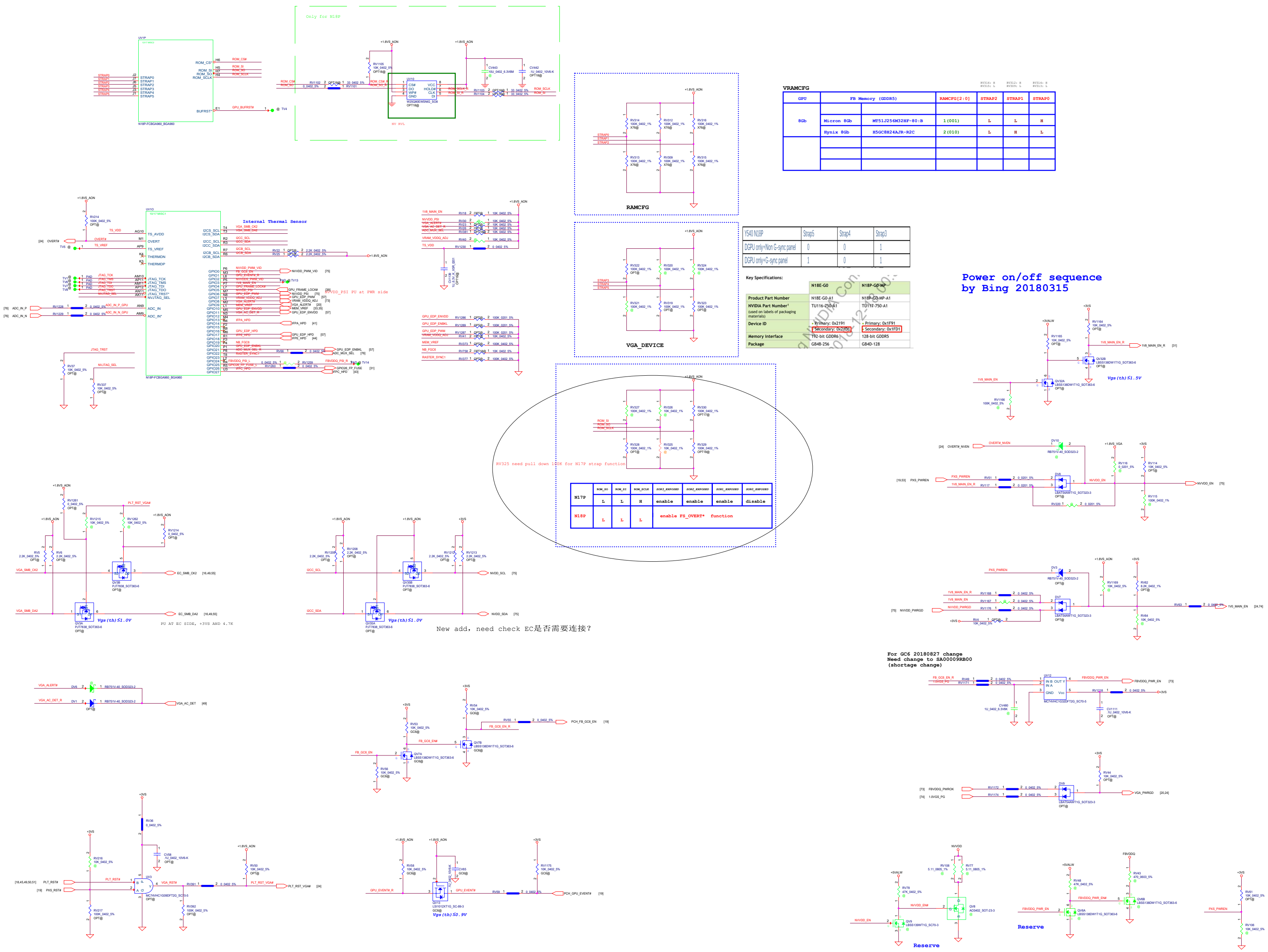

VRAMCFG

RV316: H / RV315: L — RV312: H / RV309: L — RV314: H / RV313: L

GPU	FB Memory (GDDR5)		RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
8Gb						
	Micron 8Gb	MT51J256M32HF-80:B	1(001)	L	L	H
	Hynix 8Gb	H5GC8H24AJR-R2C	2(010)	L	H	L

Y540 N18P	Strap5	Strap4	Strap3
DGPU only+Non G-sync panel	0	0	1
DGPU only+G-sync panel	1	0	1

Key Specifications:

	N18E-G0	N18P-G0-MP
Product Part Number	N18E-G0-A1	N18P-G0-MP-A1
NVIDIA Part Number[1] (used on labels of packaging materials)	TU116-750-A1	TU117-750-A1
Device ID	• Primary: 0x2191 • Secondary: 0x21D1	• Primary: 0x1F91 • Secondary: 0x1FD1
Memory interface	192-bit GDDR6	128-bit GDDR5
Package	GB4B-256	GB4D-128

	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
N17P	L	L	H	enable	enable	enable	disable
N18P	L	L	L	enable FS_OVERT* function			

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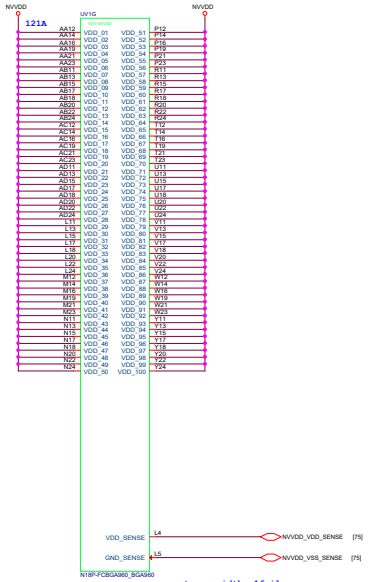
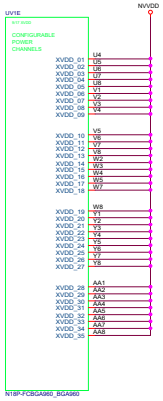
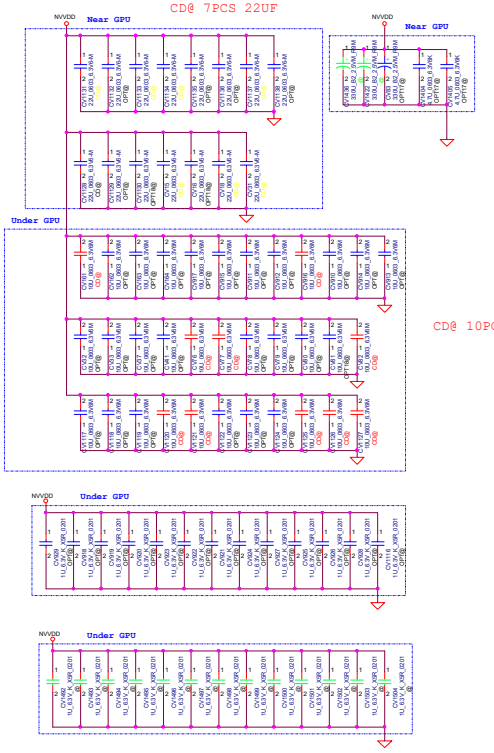
Title: N16P-GX_PEG I/F

Size: A0 — Document Number: Y540 — Rev: 0.1



trace width: 16mils
differential voltage sensing.
differential signal routing.





NVVDD/Q Decouling

MLCC	N18P	N17P	location
10uF	34	21	Under
1.0uF	13	13	
			Near
10uF	0	11	
22uF	15	10	
4.7uF	0		
330uF	0	1	

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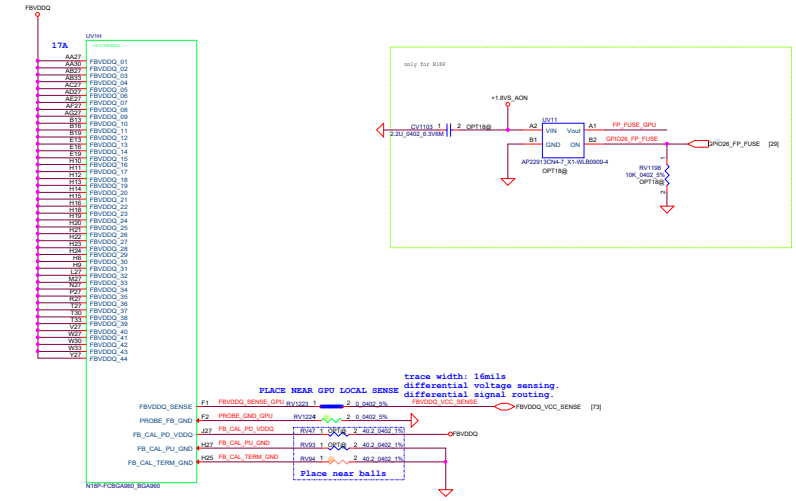
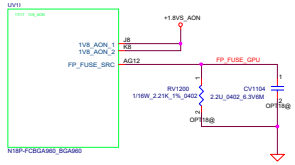
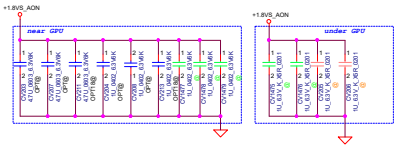
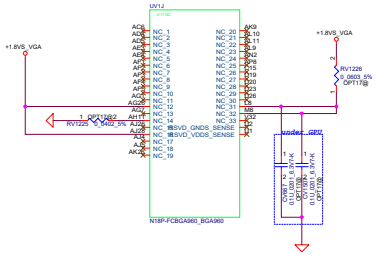






1.8VS_AON Decouling Value

MLCC	N18	N17	location
CV205	1uf	0.1uf	Under
CV206	1uf	0.1uf	Under
CV1475	@	@	Under
CV1476	@	@	Under



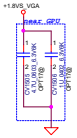
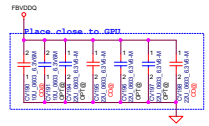
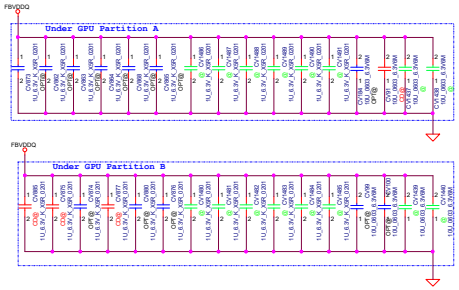


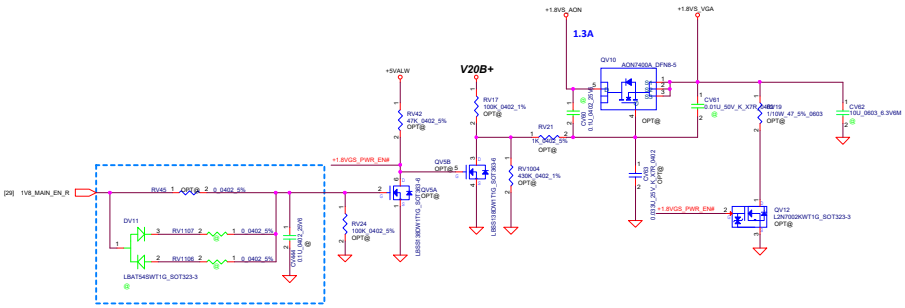
Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm





+1.8VS_AON TO +1.8VS_VGA



Reserve PD3,RV1107,RV1106,CV444 for NV sequence requirement-Harry 10/20

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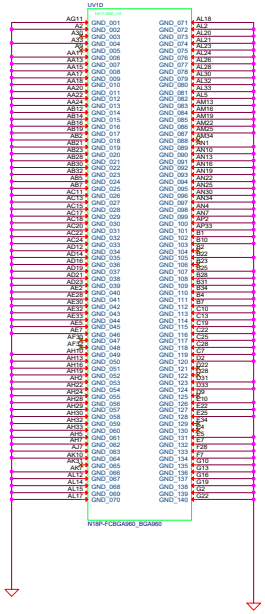
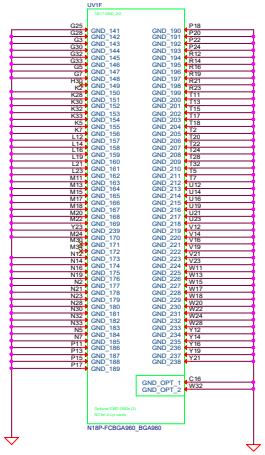
BOTH GP107 AND N18P-G5 NEED
NC AF30,AF32,AK31,AM34,E34,H30,M30,M34,
A30,A6,B2,B23,D22,D28,D9,E4





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Title	GND		
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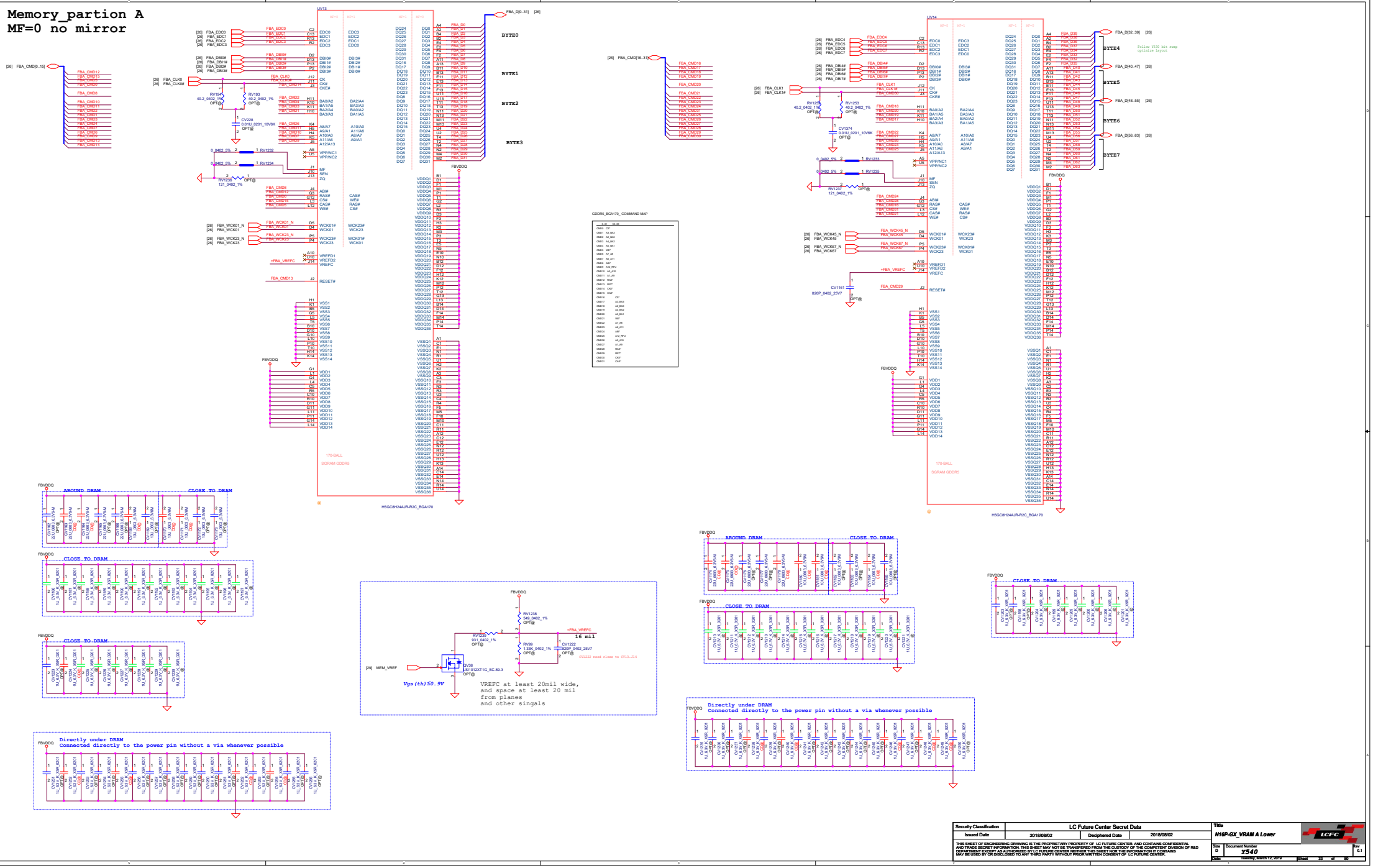
Memory_partion A
MF=0 no mirror



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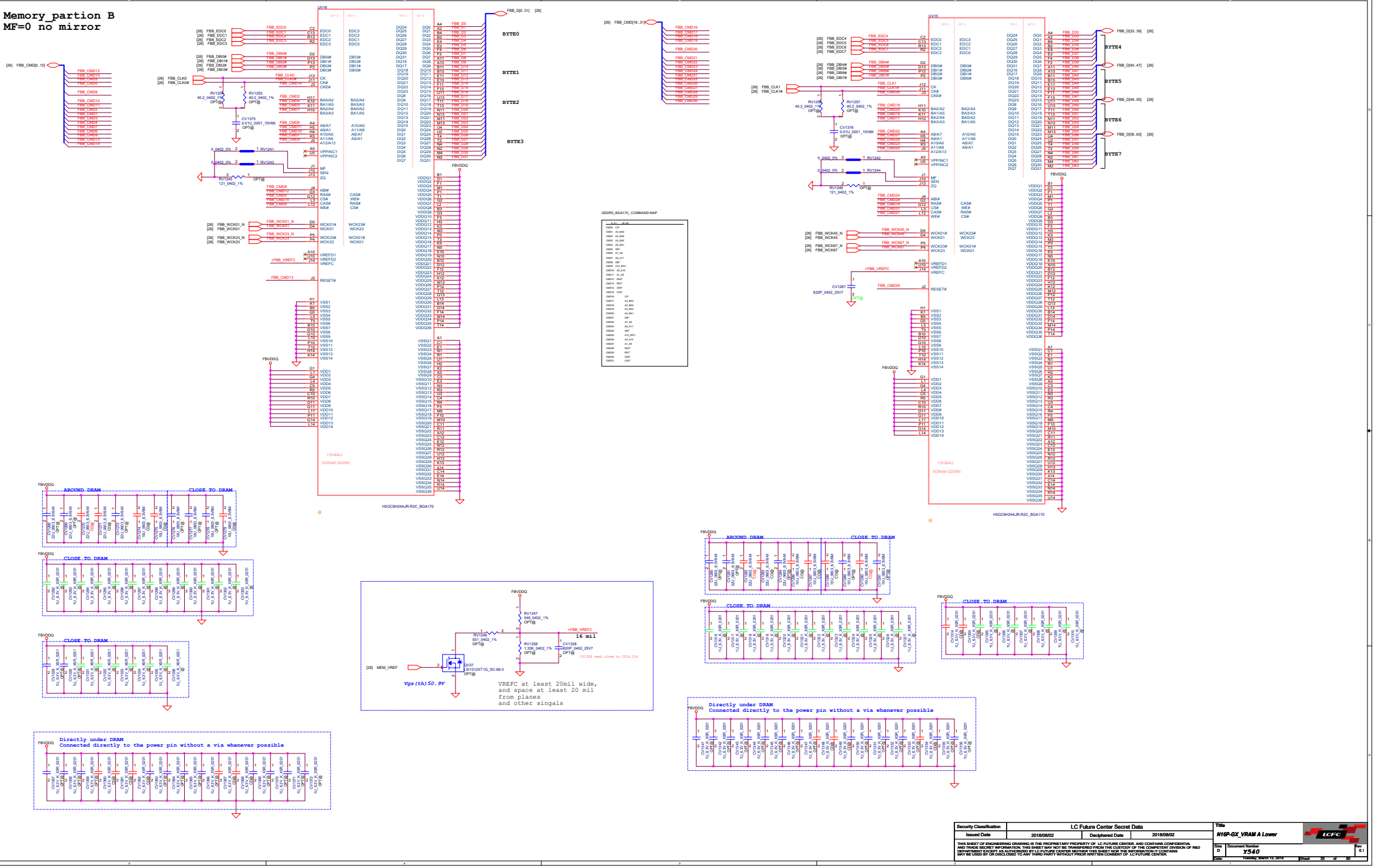
Memory_partion B
MF=0 no mirror



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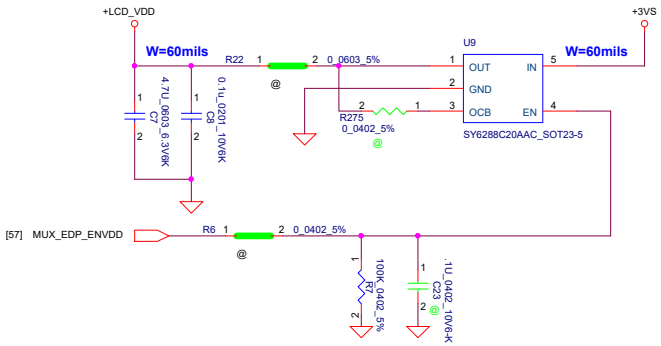
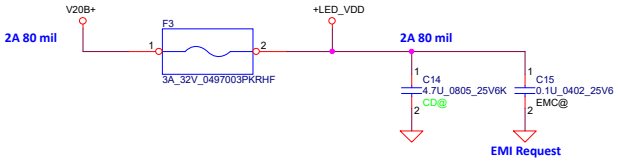
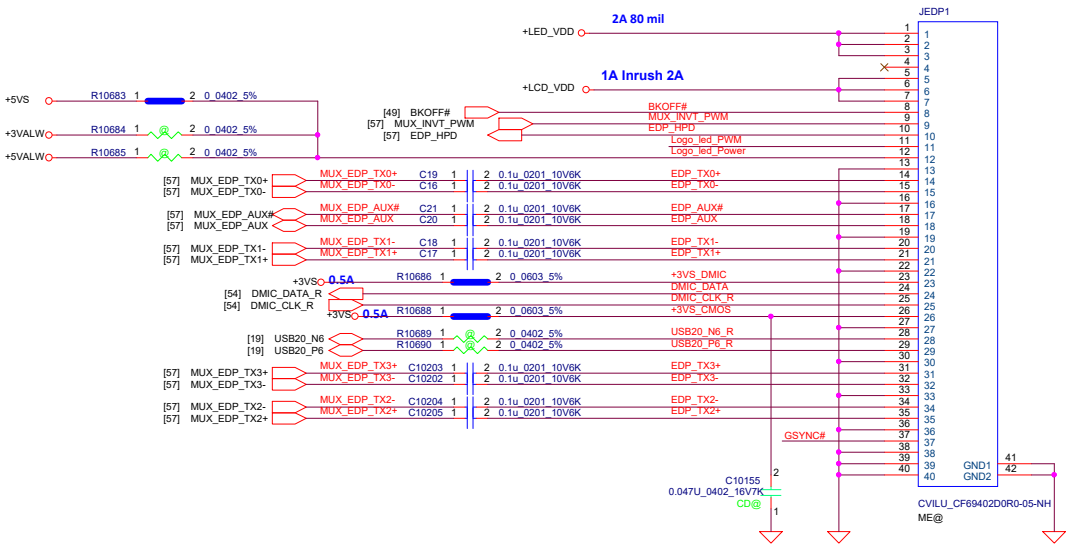
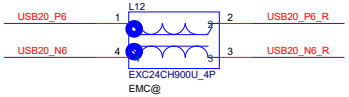
LCD POWER CIRCUIT

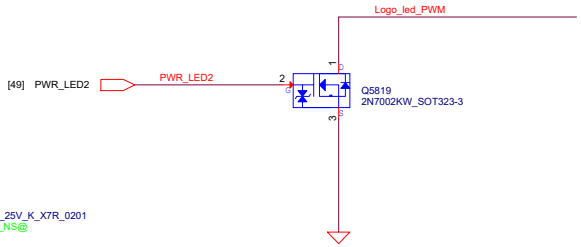




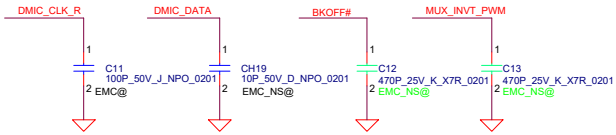


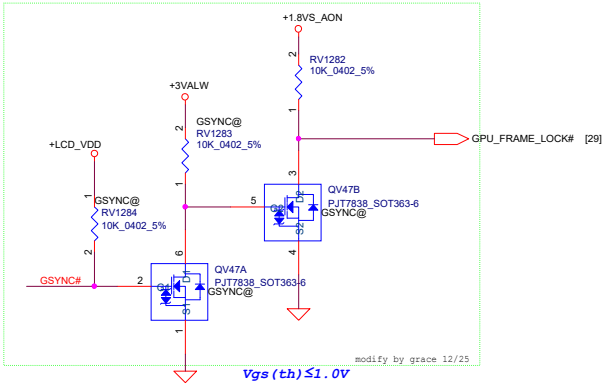
For EMI





EMI request





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Title: eDP/ CMOS/Touch screen

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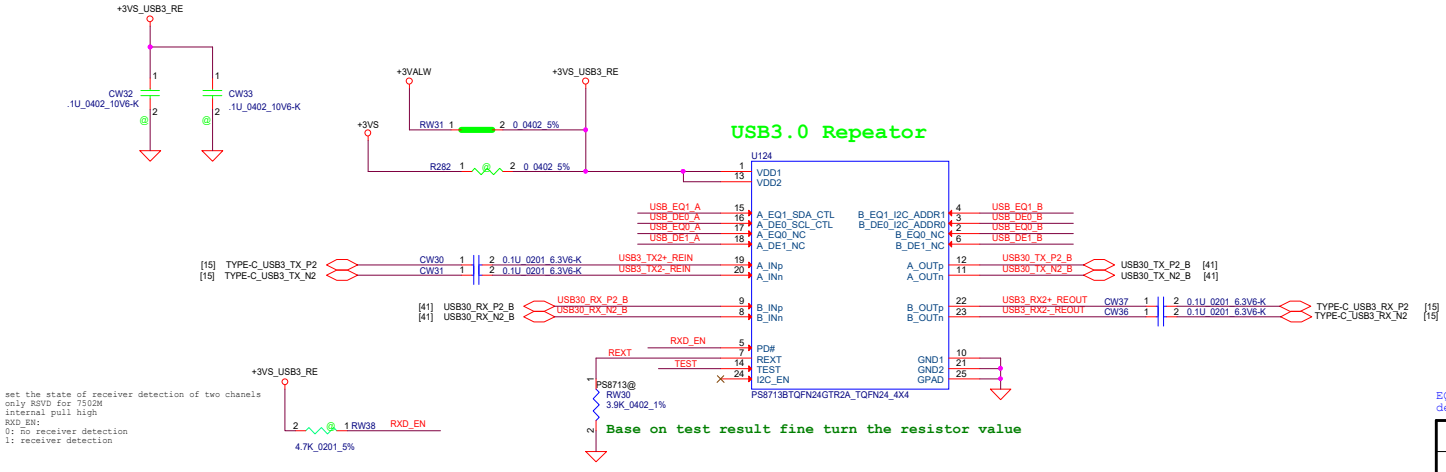
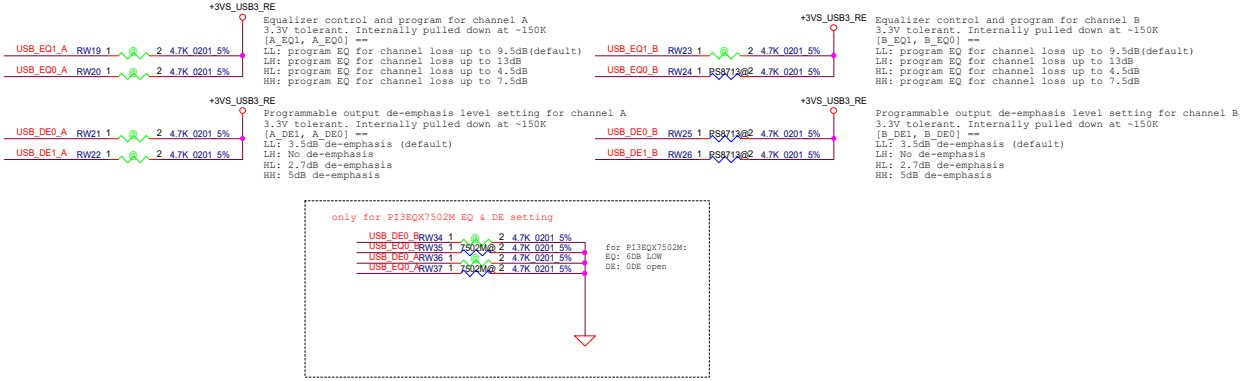


EQ & DE setting BOM structure
default setting, need fine tune

Location	PS8713BT	PI3EQX7502M
RW38	@ no need use	@ internal PU only for 7502M
RW34 RW35 RW36 RW37	@ internal pull down no need external resistance	@ default setting EQ_A/B: floating for EQ=3dB DE_A/B: floating for DE=0dB need fine tune
RW30 RW27	PS8713@	@ floating without external connection
RW19 RW22 RW23 RW26	Used for EQ&DE setting base on fine tune result	@ NC pin no need use
RW20 RW21 RW24 RW25	Used for EQ&DE setting base on fine tune result	Used for EQ&DE setting base on fine tune result



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Title: DDI Redriver PS8330

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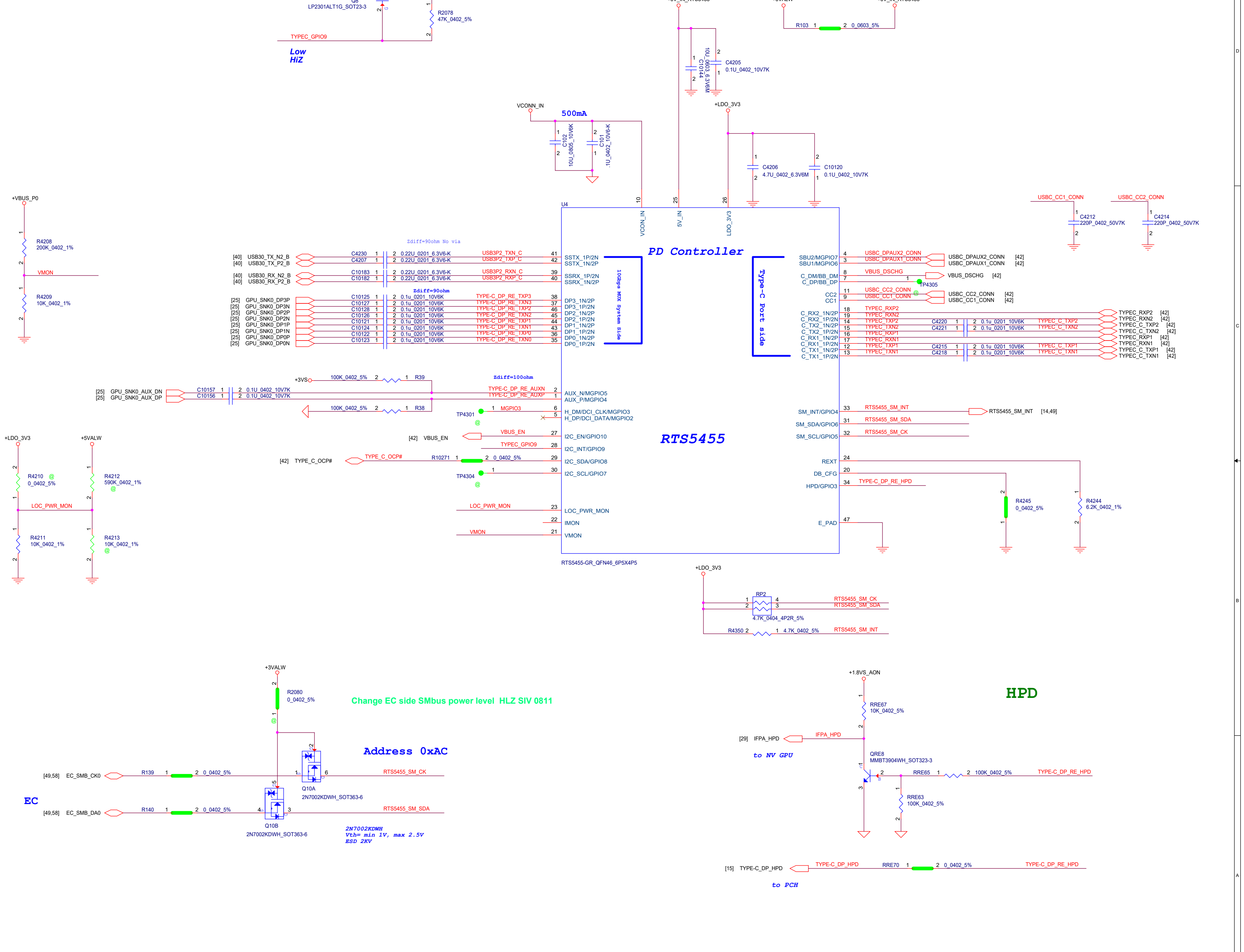
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



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Title: **USB TYPE-C Controller**

LCFC

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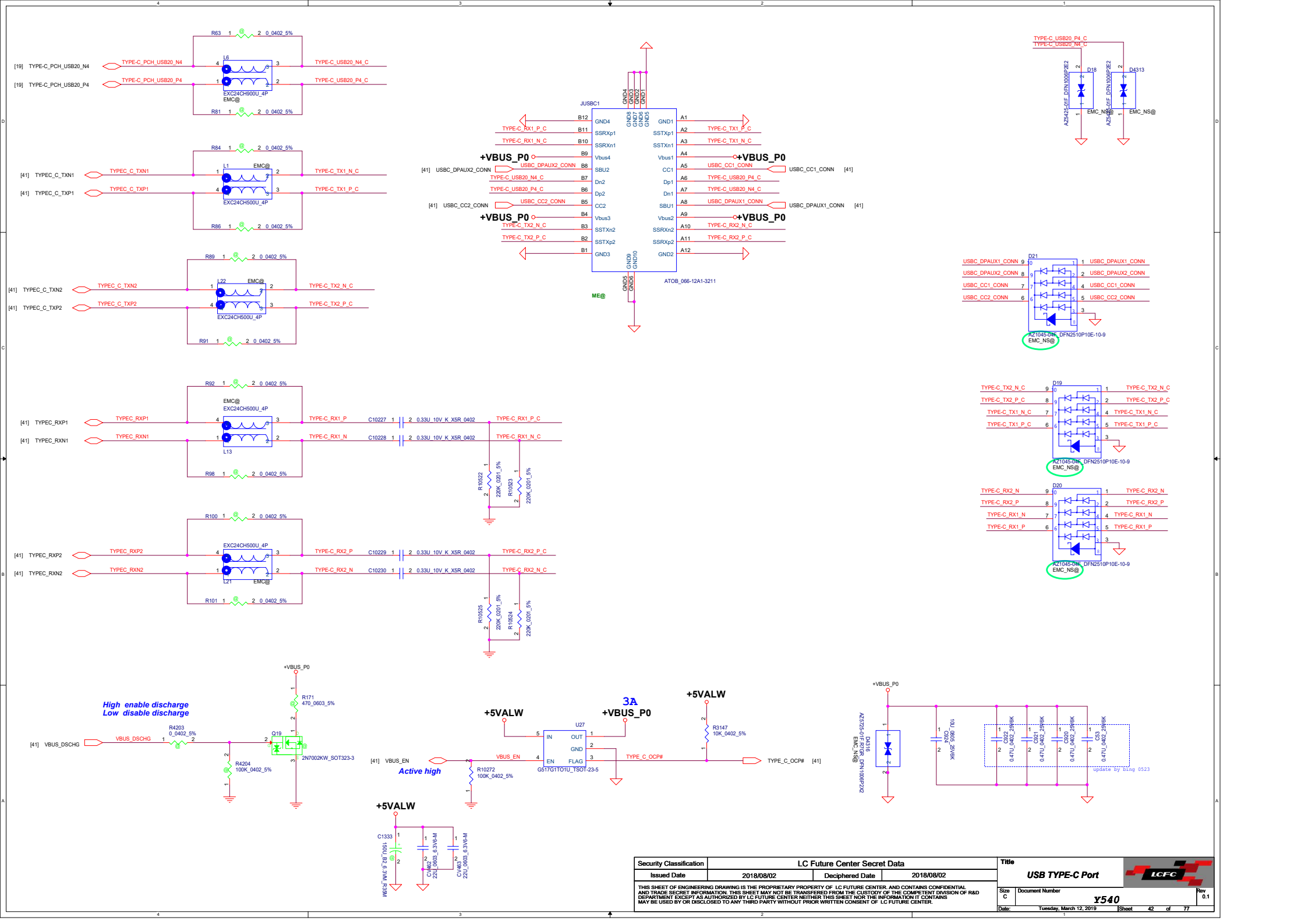

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB TYPE-C Port**

Size	Document Number	Rev
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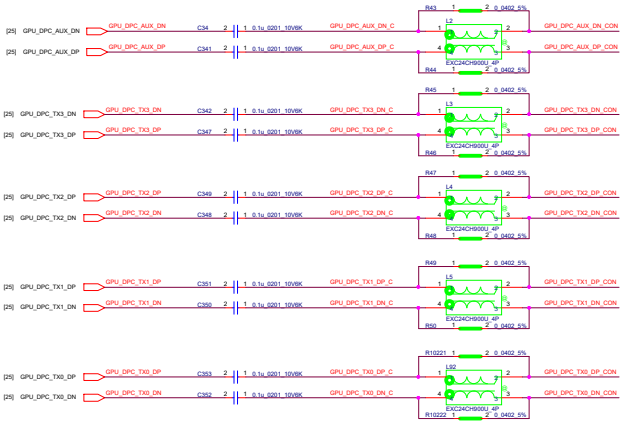

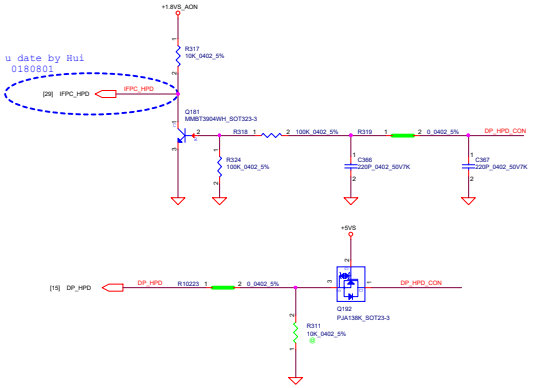

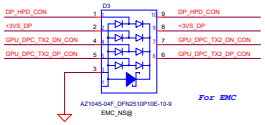

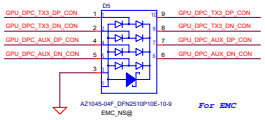

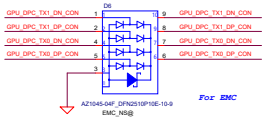

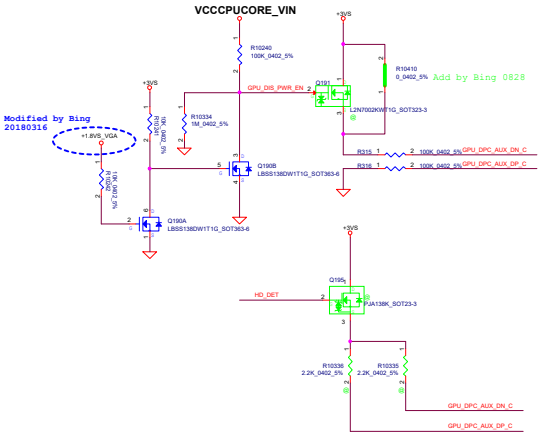

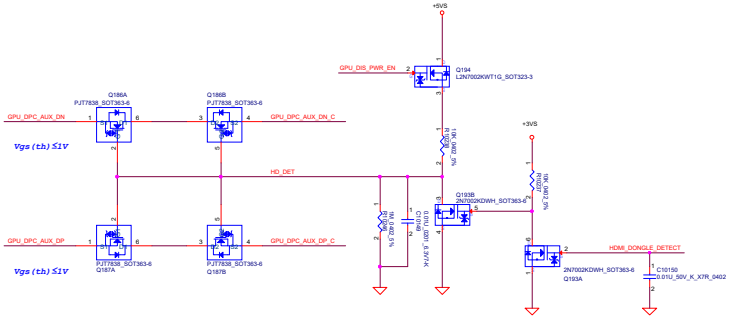

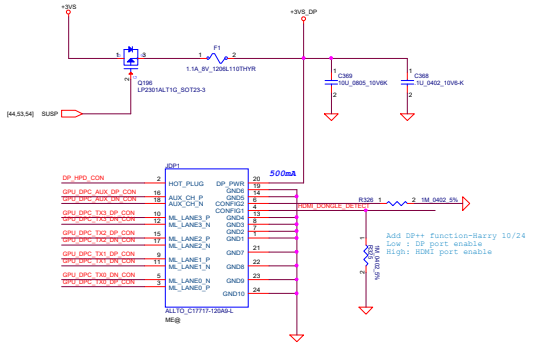

Security Classification	LC Future Center Secret Data		
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Title	DP		
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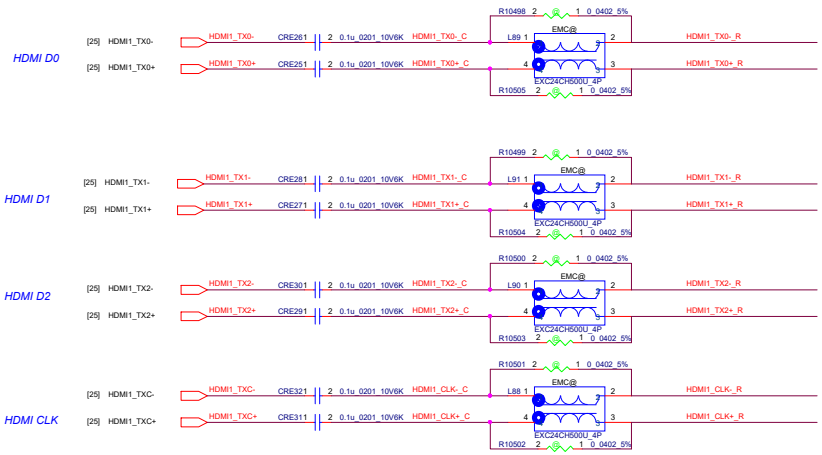

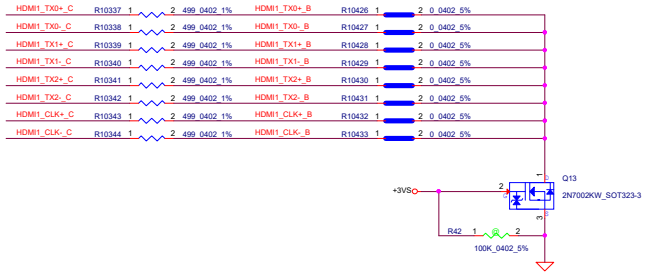

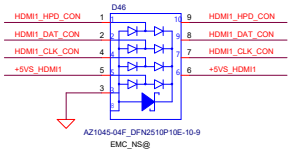

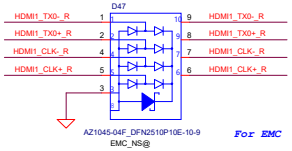

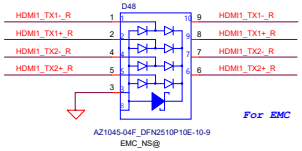

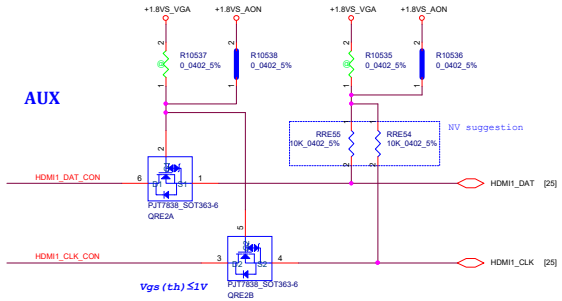

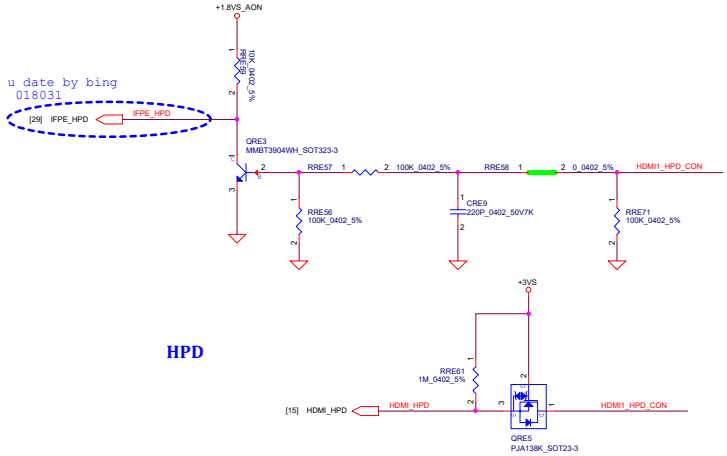

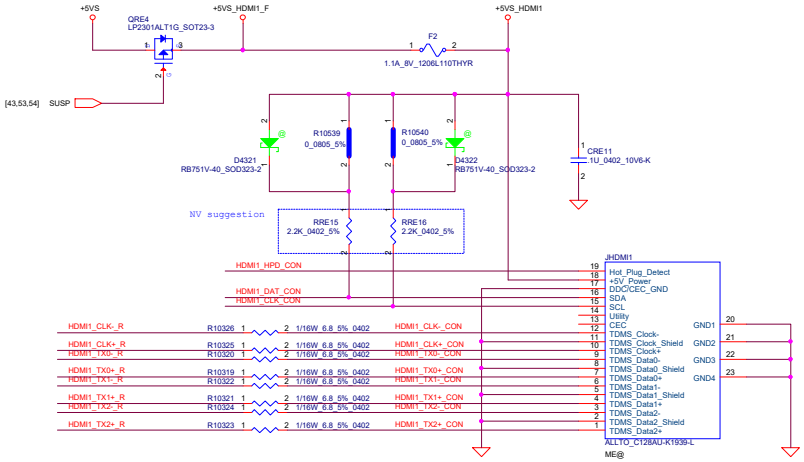

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	HDMI_CONN		
Size	Document Number		Rev
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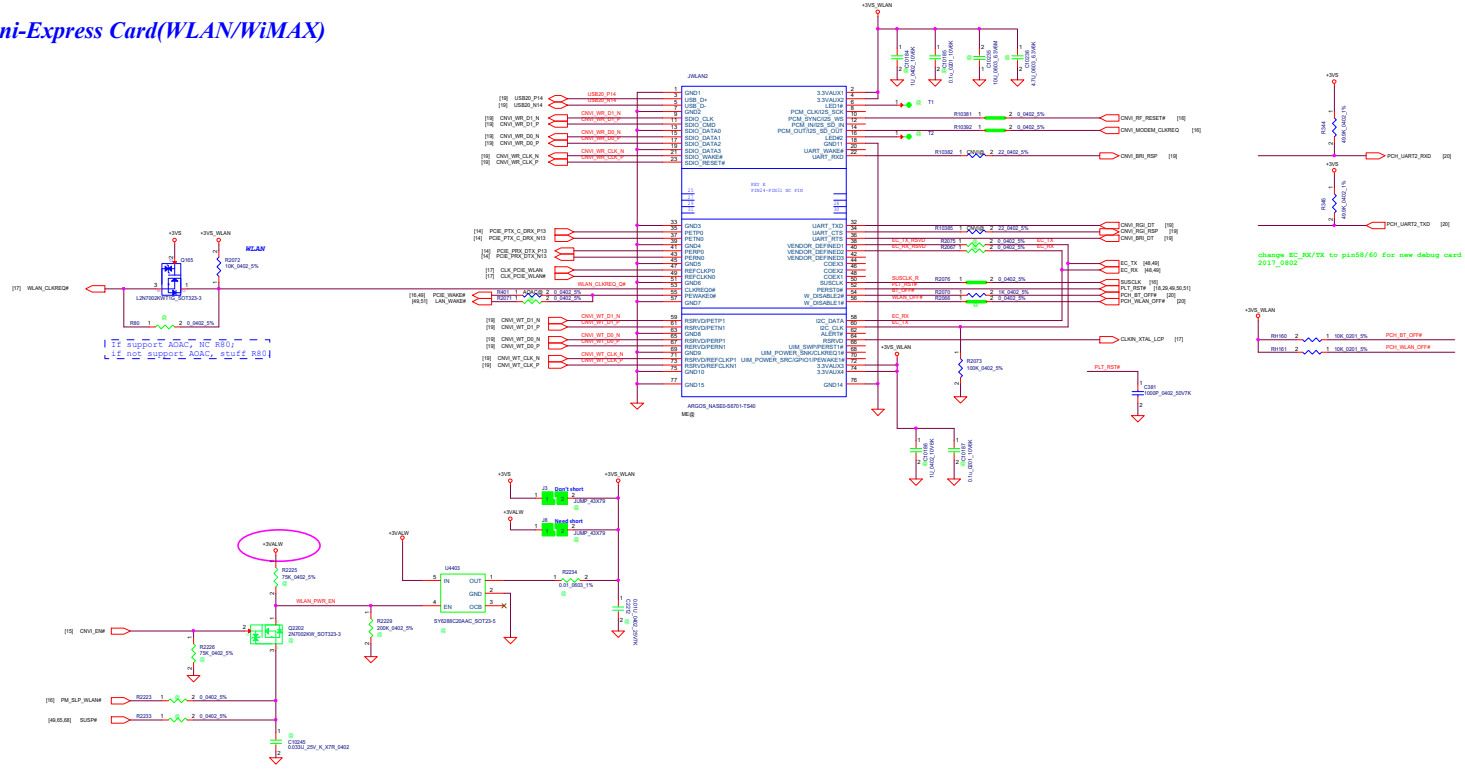
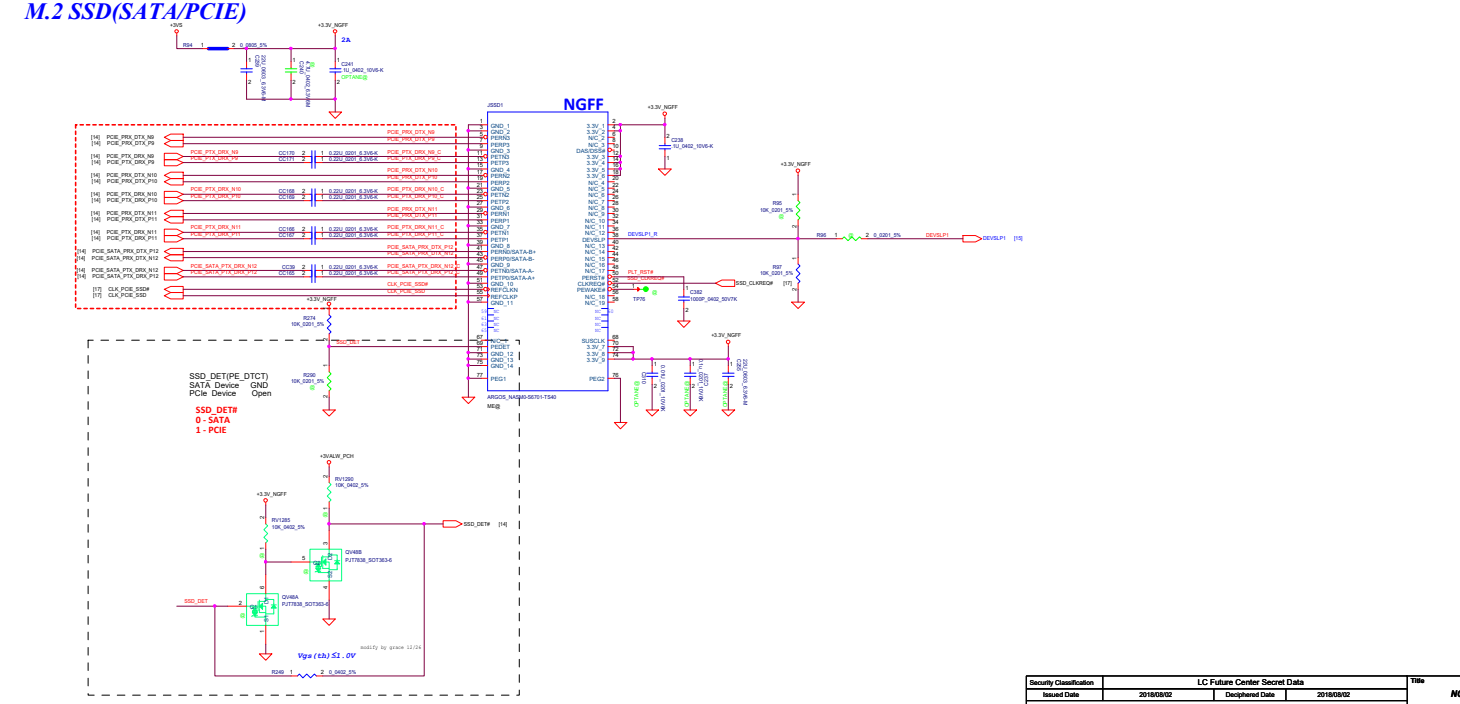
Mini-Express Card(WLAN/WiMAX)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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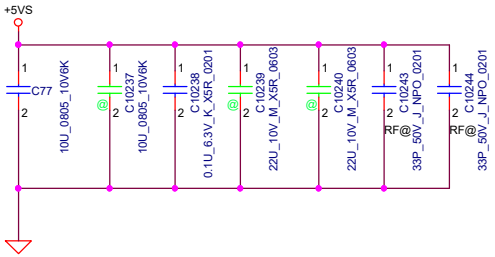
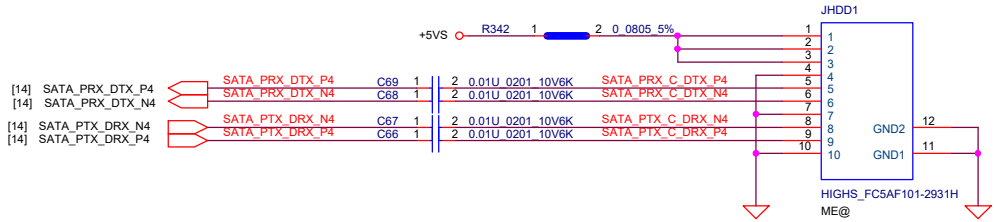
Title: NGFF WLAN

Size: C | Document Number: Y540 | Rev: 0.1

Date: Tuesday, March 14, 2017 | Sheet 45 of 77

SATA HDD Conn.



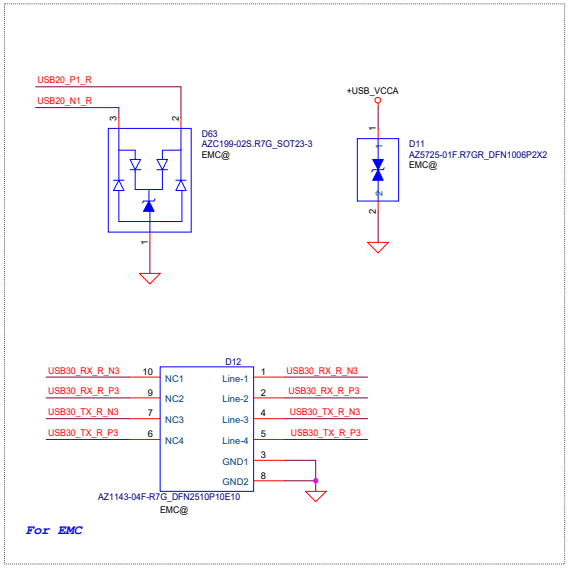


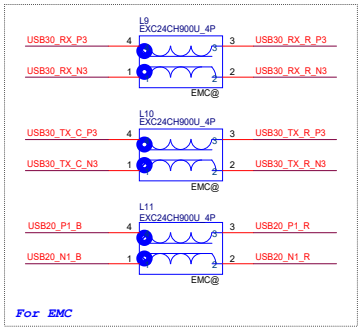
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

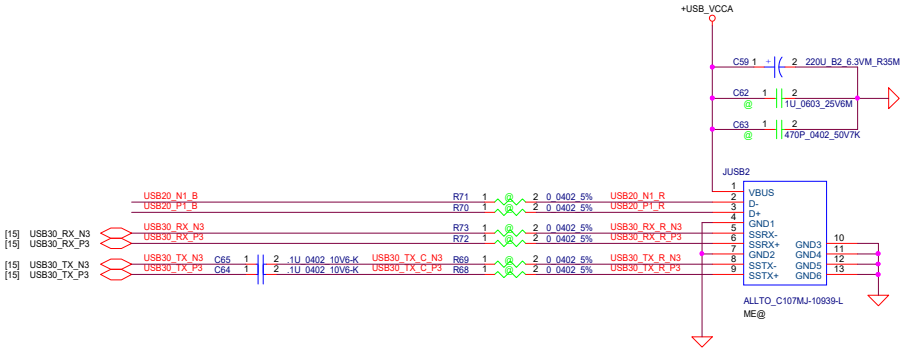
Title: **HDD/XBOX CONN**

Size	Document Number	Rev
Custom	Y540	0.1

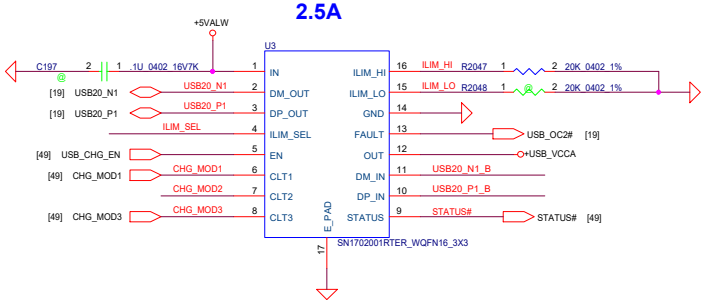
Date: Tuesday, March 12, 2019 Sheet 46 of 77

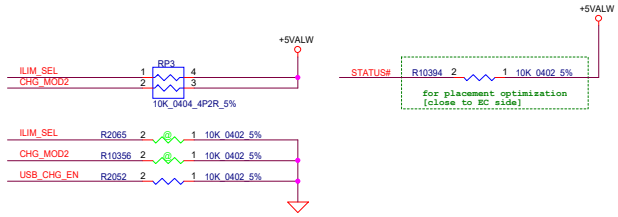






USB charger
2.5A

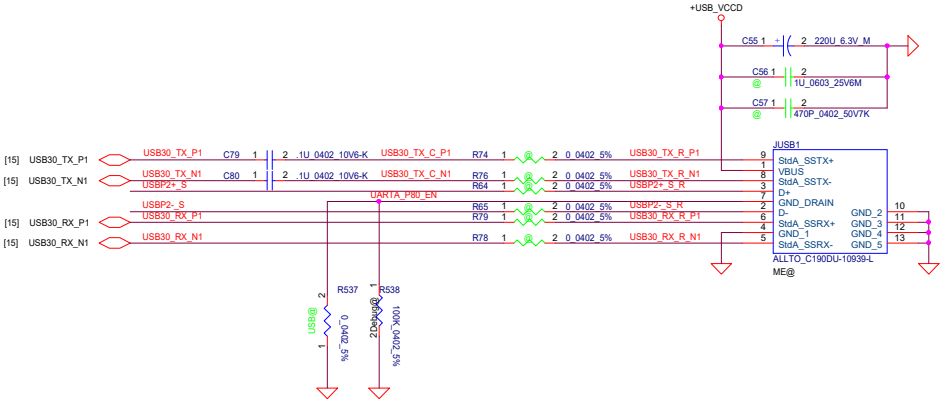




CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

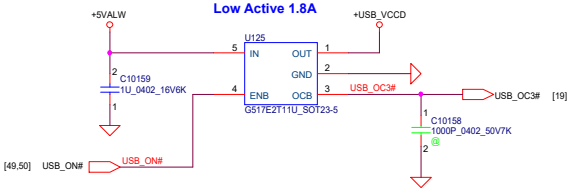
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	USB2.0/USB3.0 PORT (LEFT)		
Size C	Document Number Y540		Rev 0.1
Date: Tuesday, March 12, 2019	Sheet 47 of 77		

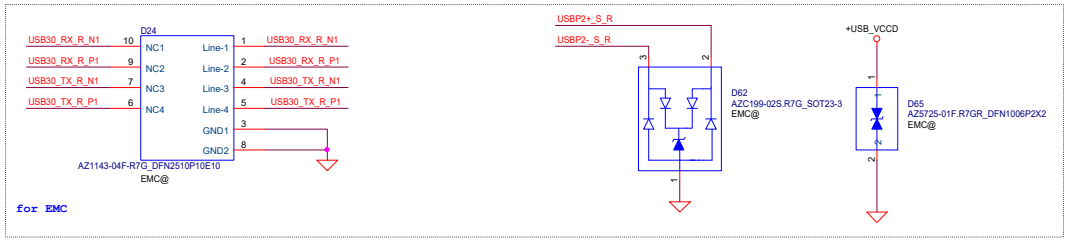


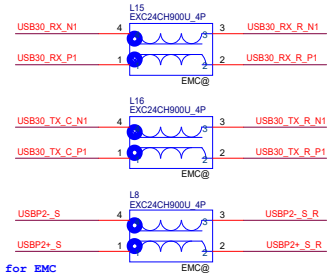
USB3.1 PORT x1

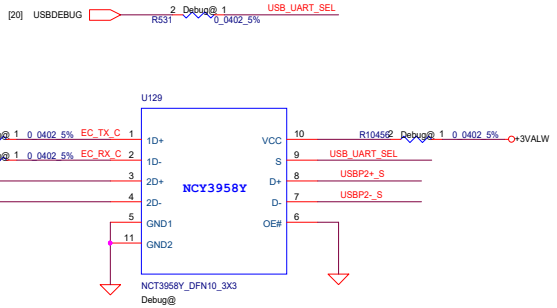
Low Active 1.8A

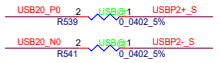


For USB Debug Function





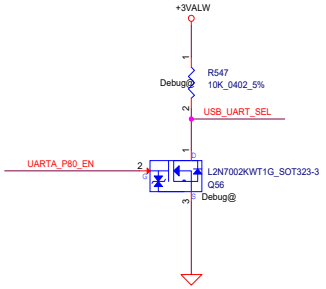




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

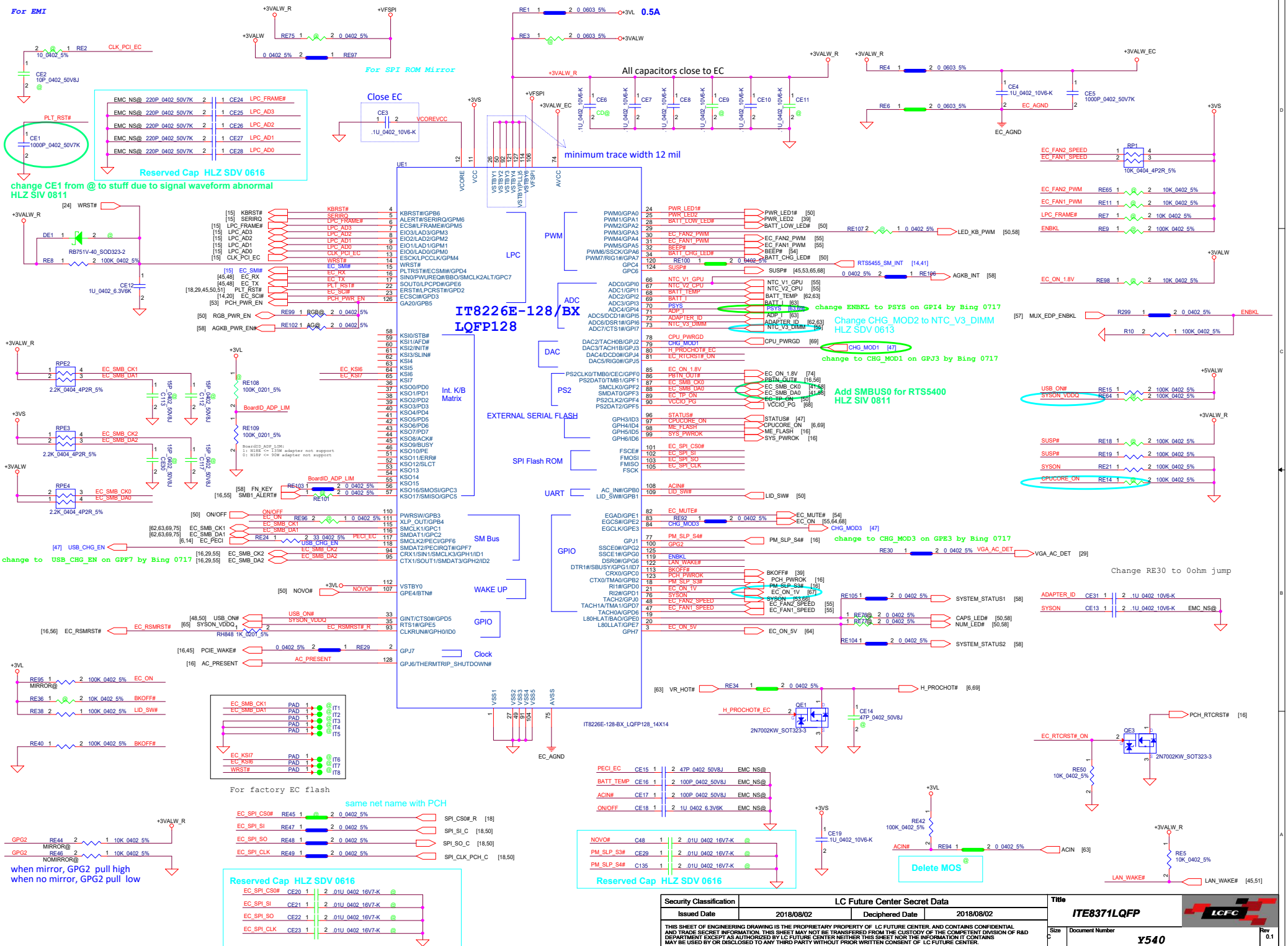


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: USB2.0

Size	Document Number	Rev
C	Y540	0.1

Date: Tuesday, March 12, 2019 Sheet 48 of 77



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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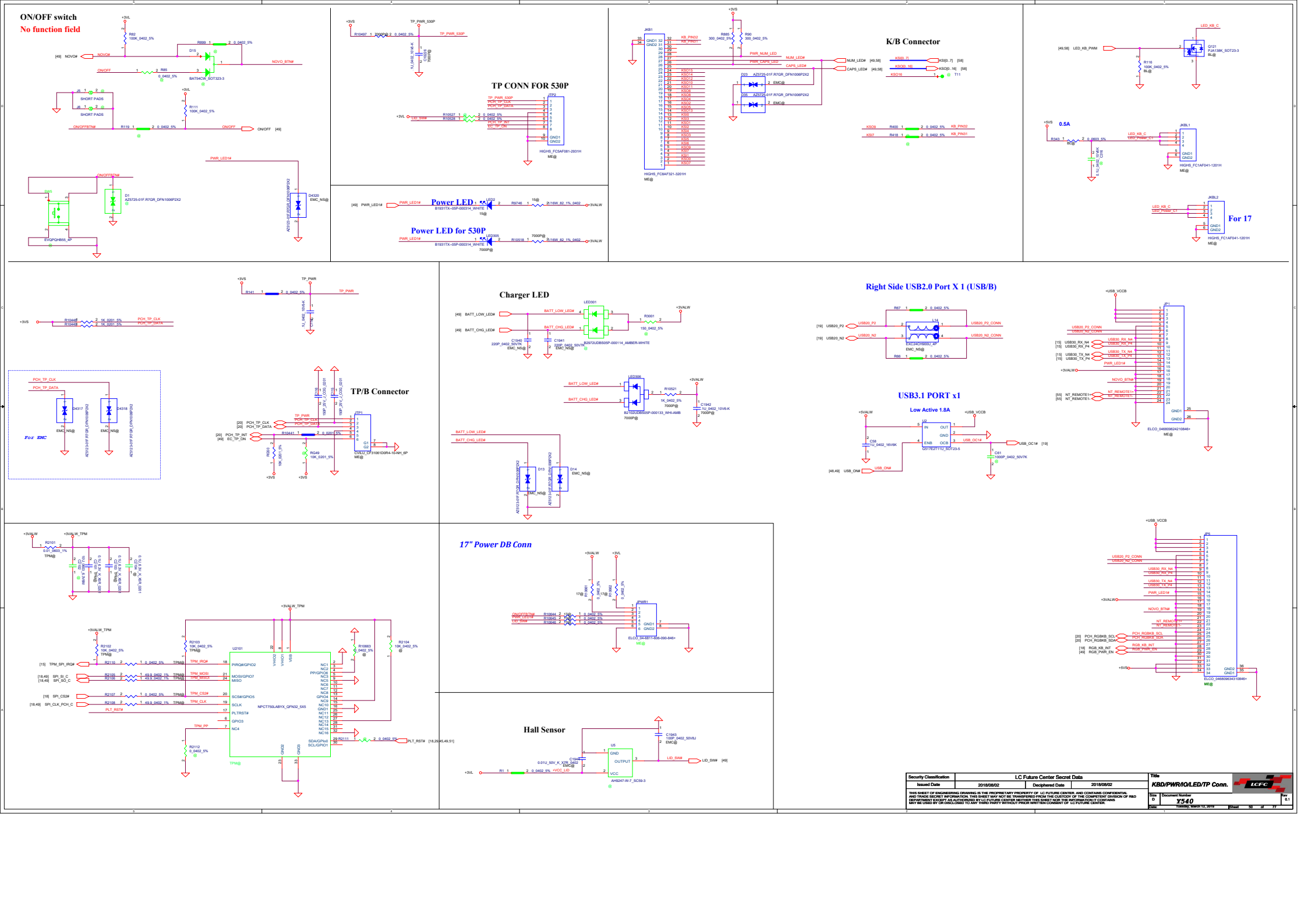
Title: ITE8371LQFP

Size	Document Number	Rev
C	Y540	0.1

Date: Tuesday, March 12, 2019 Sheet 49 of 77

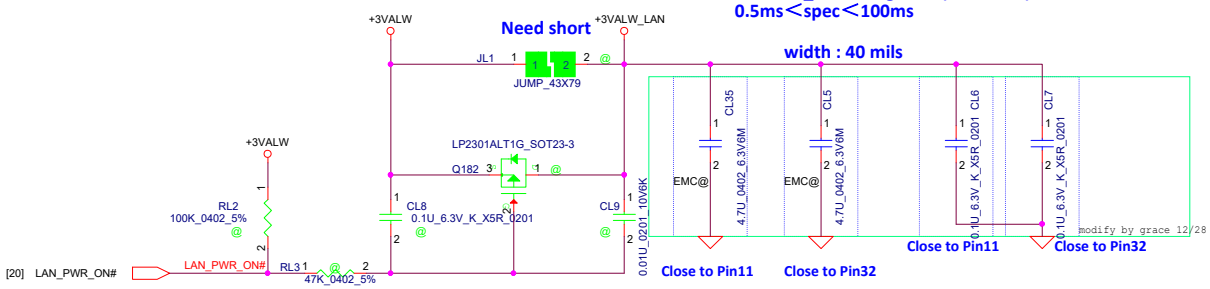

ON/OFF switch
No function field
TP CONN FOR 530P
Power LED :
Power LED for 530P
K/B Connector
For 17
TP/B Connector
For EMC
Charger LED
Right Side USB2.0 Port X 1 (USB/B)
USB3.1 PORT x1
Low Active 1.8A
17" Power DB Conn
Hall Sensor
LC Future Center Secret Data
KBD/PWR/IO/LED/TP Conn.
Issued Date
2018/08/02
Deciphered Date
2018/08/02
Tuesday, March 12, 2019

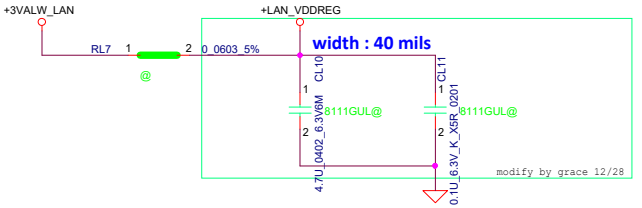
+3VALW TO +3VALW_LAN

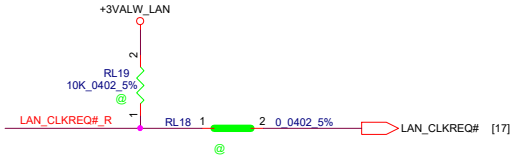
+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

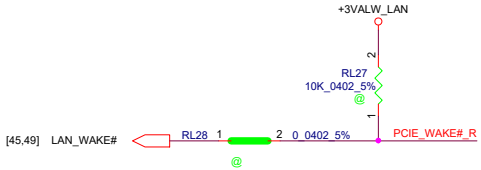
Need short

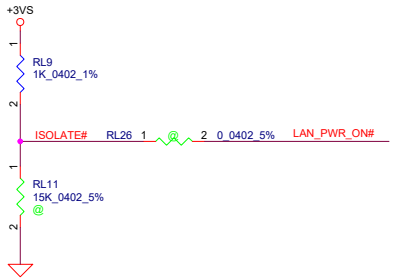
width : 40 mils

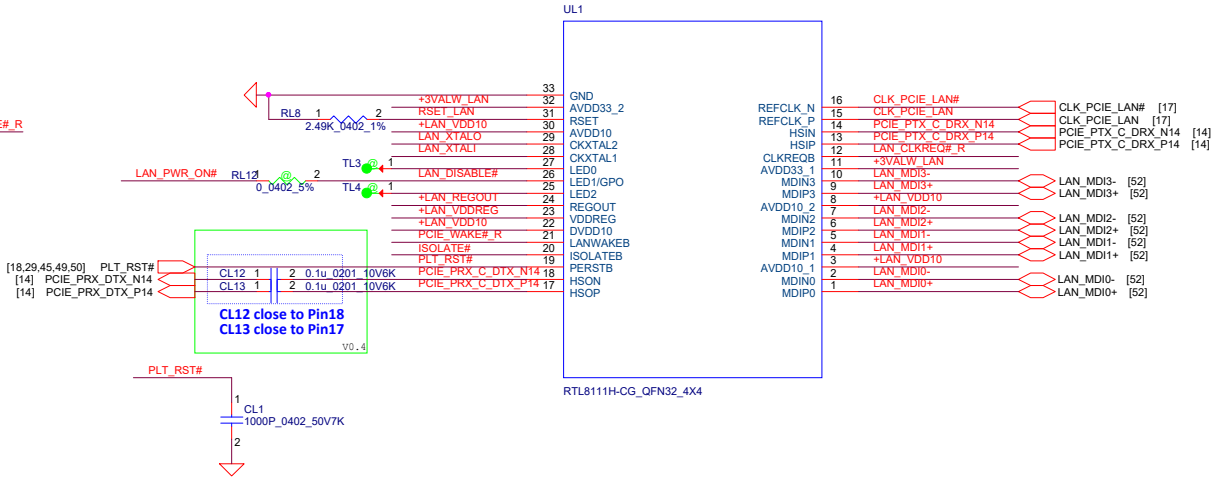


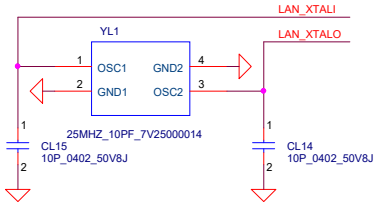


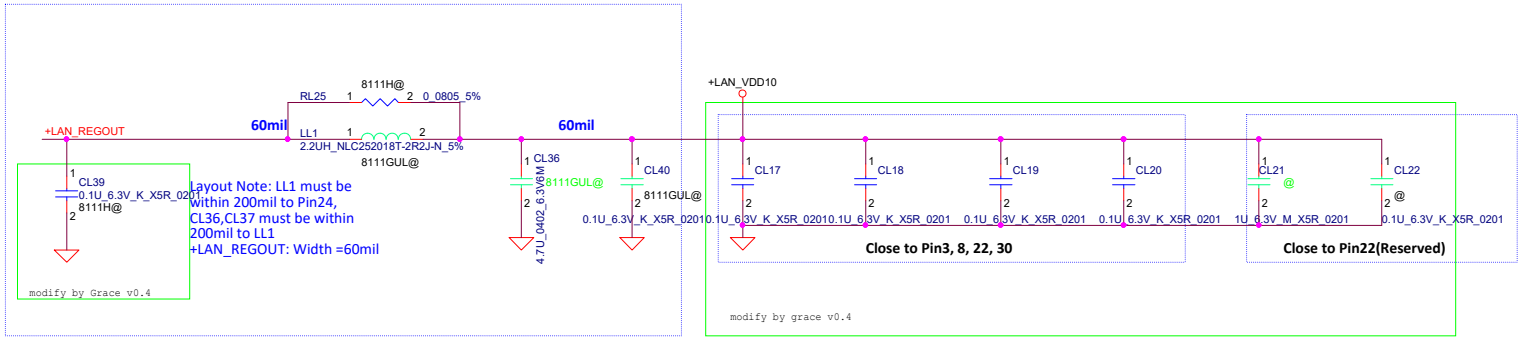












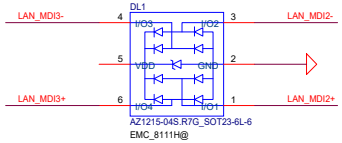
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

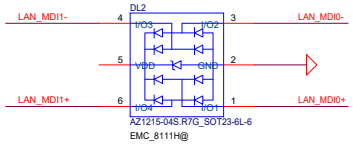
Title: **LAN_RTL8111**

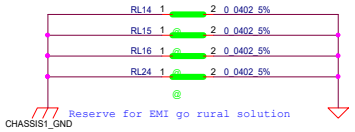
Size	Document Number	Rev
Custom	Y540	0.4

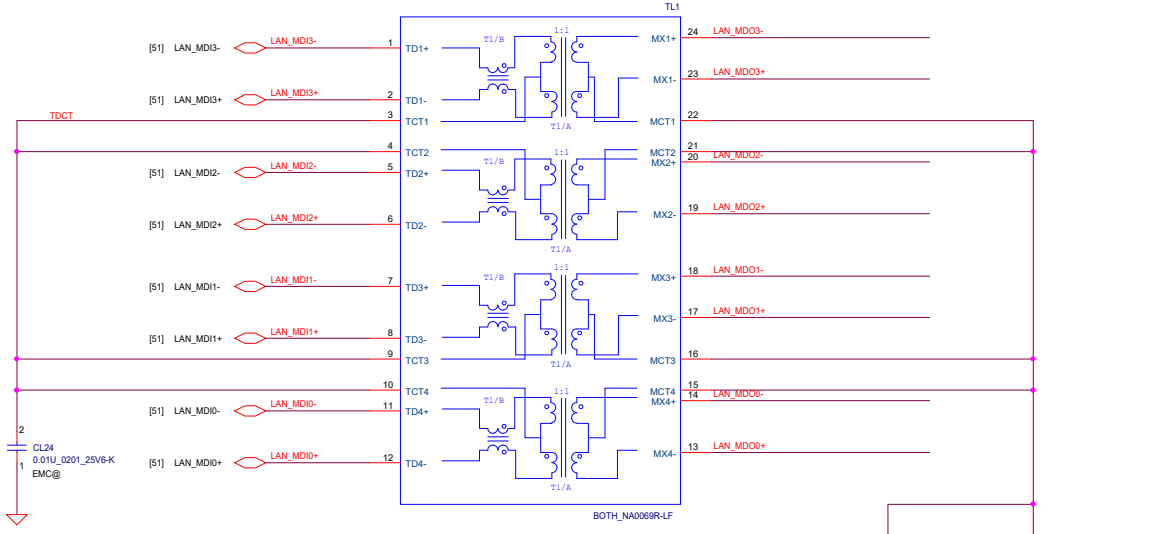
Date: Tuesday, March 12, 2019 Sheet 51 of 77

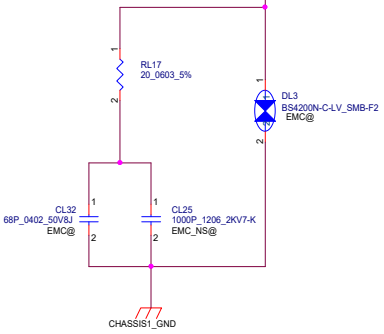
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

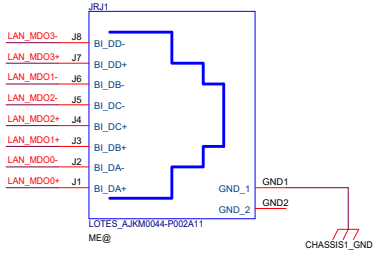






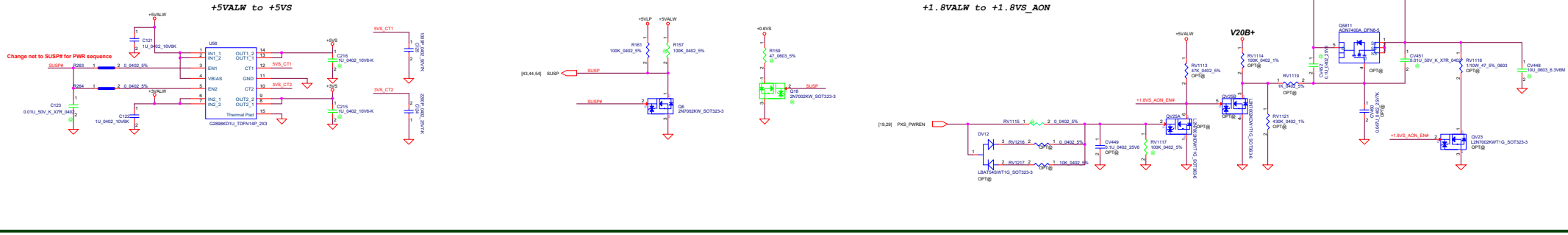


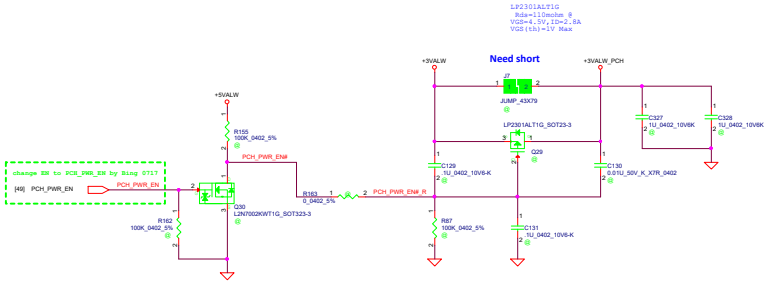


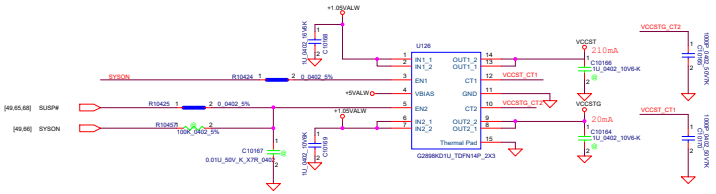


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	LAN_Transformer		
Size	Document Number		Rev
C	Y540		0.1
Date:	Tuesday, March 12, 2019	Sheet	52 of 77







Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DC V TO VS INTERFACE		
Size D	Document Number Y540		Rev 0.1
Date: Tuesday, March 12, 2019		Sheet 53 of 77	

Digital power for HDA link

Digital power for digital I/O circuit

Analog power for DACs, ADCs

Analog power for mixers, & IO ports

Power supply for full-bridge left/Right channel

HP/MIC Jack

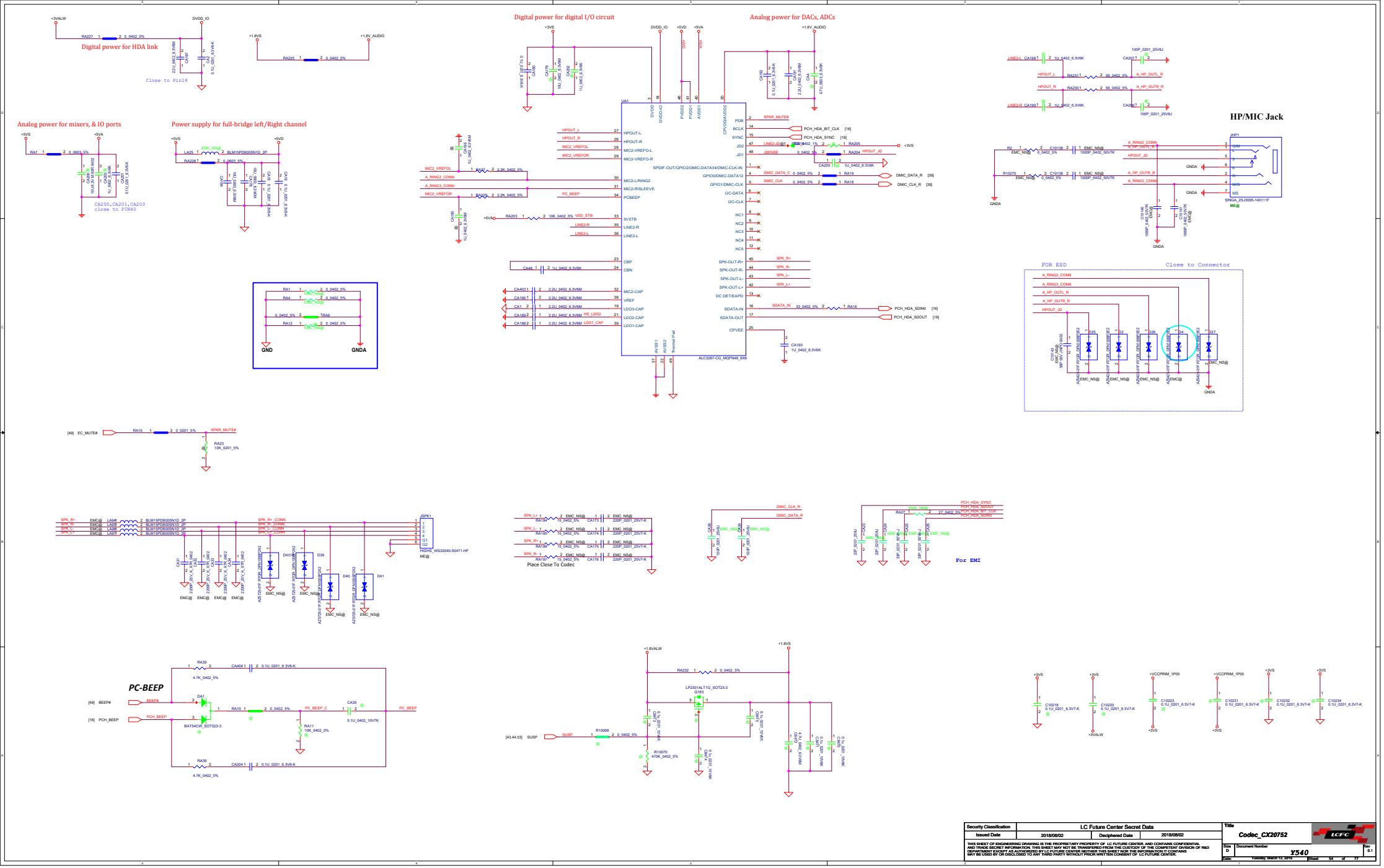
FOR ESD

Close to Connector

Place Close To Codec

For EMI

PC-BEEP



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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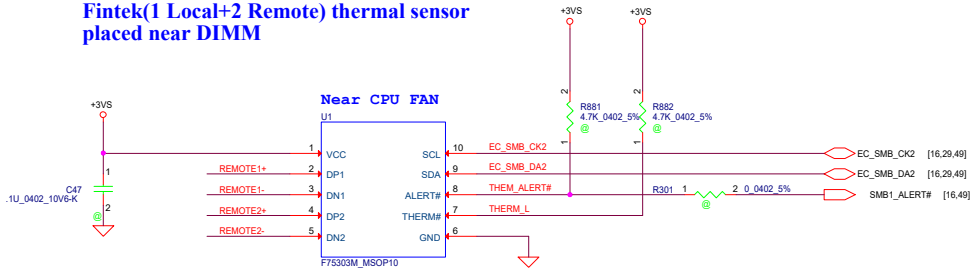
Title: Codec_CX20752

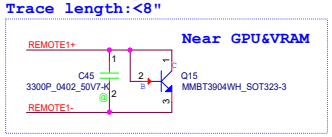
Size: D | Document Number: X540 | Rev: 0.1

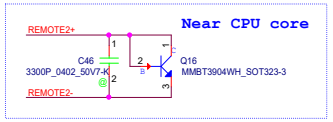
Date: Tuesday, March 12, 2019 | Sheet 54 of 77

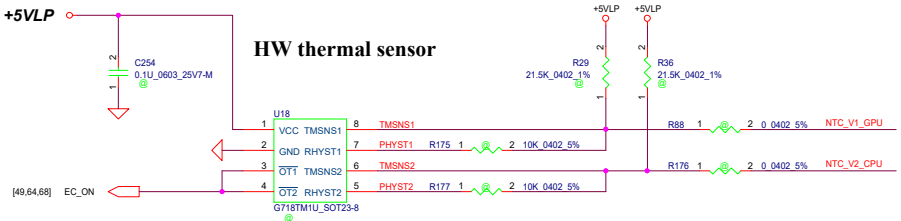
Fintek(1 Local+2 Remote) thermal sensor placed near DIMM



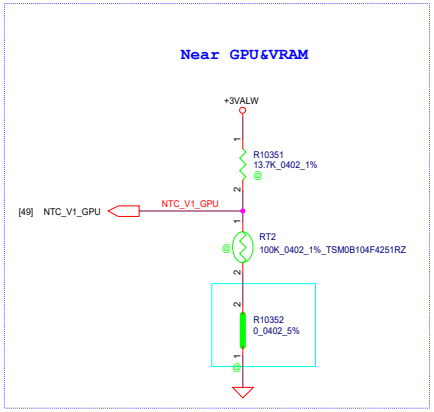
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

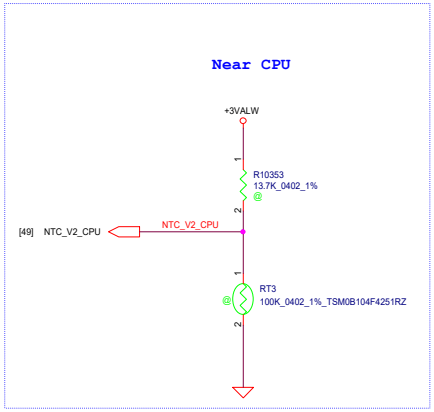






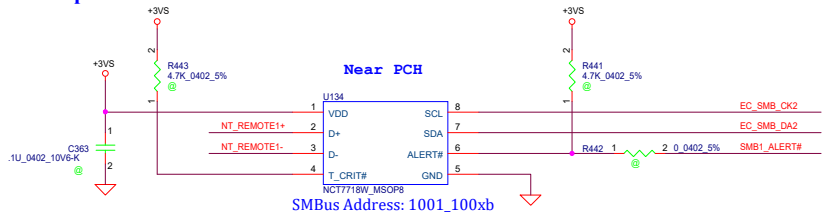
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



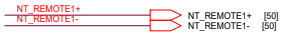


for layout optimized, change the EC_AGND to GND

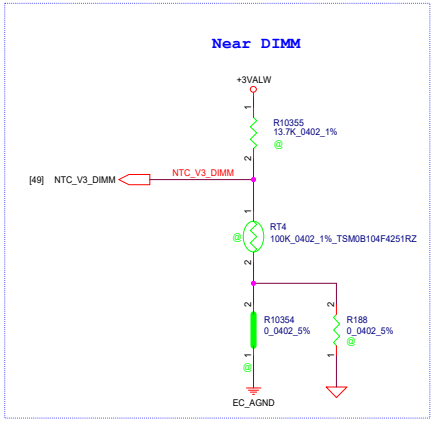
Nuvoton(1 Local+1 Remote) thermal sensor placed near TBD



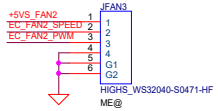
SMBus Address: 1001_100xb



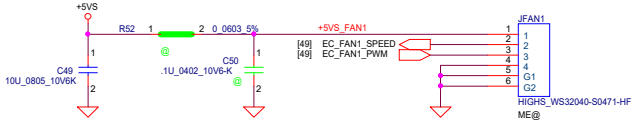
Thermal Diode Near GPU FAN(DB)
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

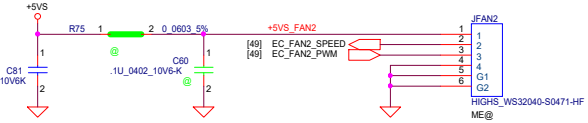


FAN Conn



Address 1001_101xb





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Thermal sensor/FAN CONN		
Size C	Document Number Y540		Rev 0.1
Date: Tuesday, March 12, 2019		Sheet 55 of 77	

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

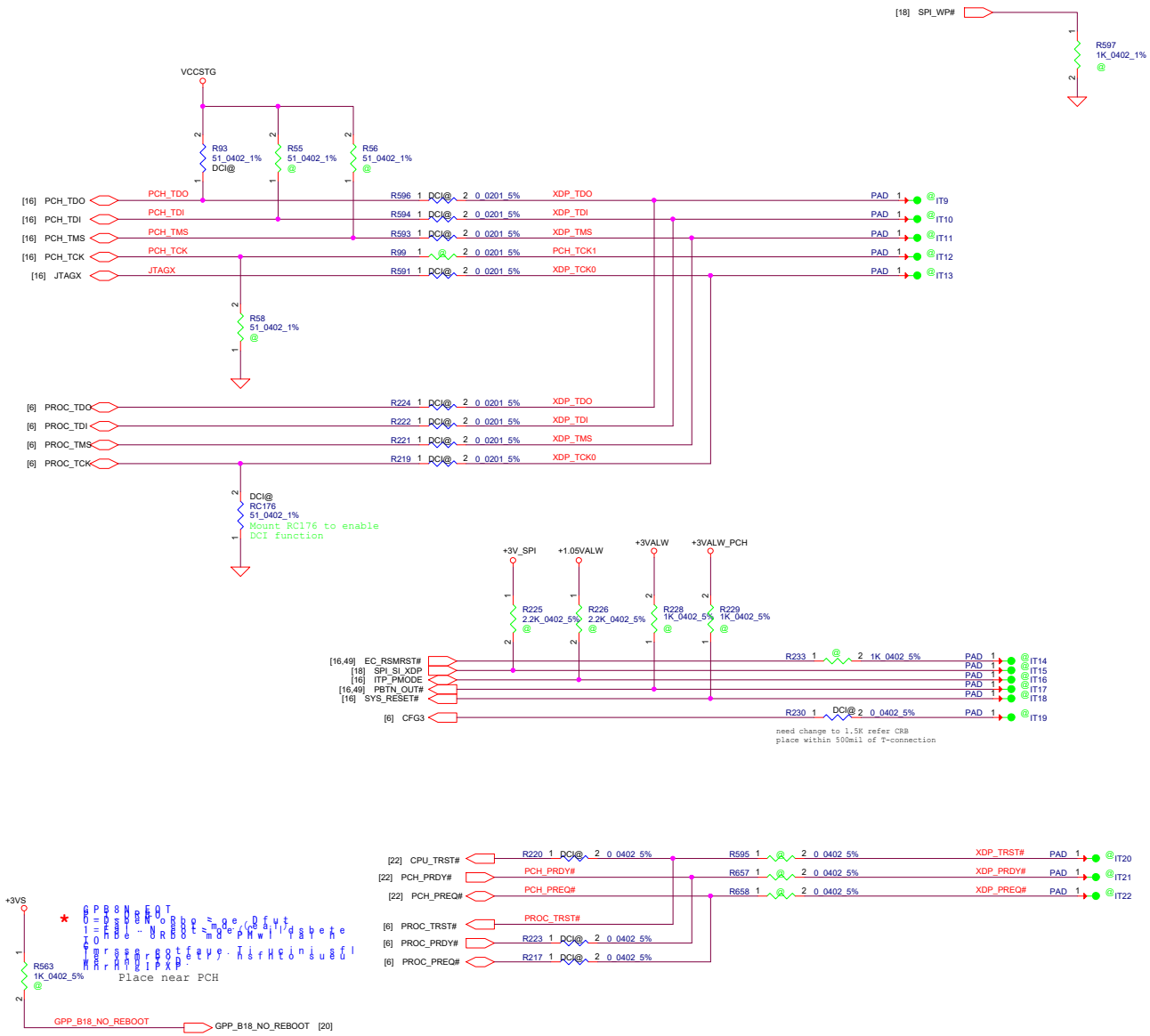
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: XDP

Size: Custom | Document Number: Y540 | Rev: 0.1

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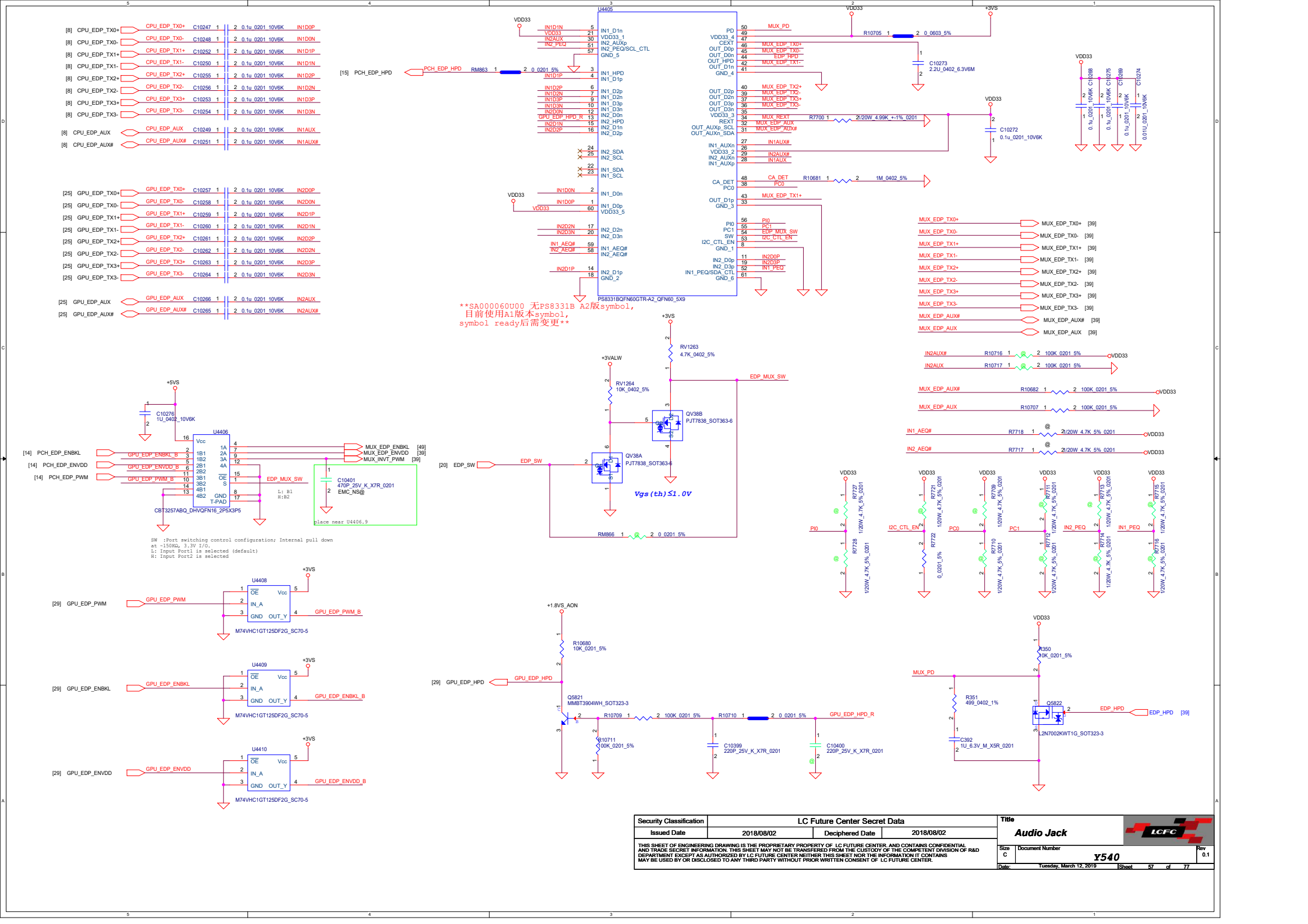
U4405
PS8331BQFN60GTR-A2_QFN60_5X9
**SA000060U00 无PS8331B A2版symbol,
目前使用A1版本symbol,
symbol ready后需变更**
U4406
CBT3257ABQ_DHVQFN16_2P5X3P5
SW :Port switching control configuration; Internal pull down
at ~150KΩ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected
U4408
U4409
U4410
M74VHC1GT125DF2G_SC70-5
Vgs(th)≤1.0V
Security Classification
LC Future Center Secret Data
Issued Date
2018/08/02
Deciphered Date
2018/08/02
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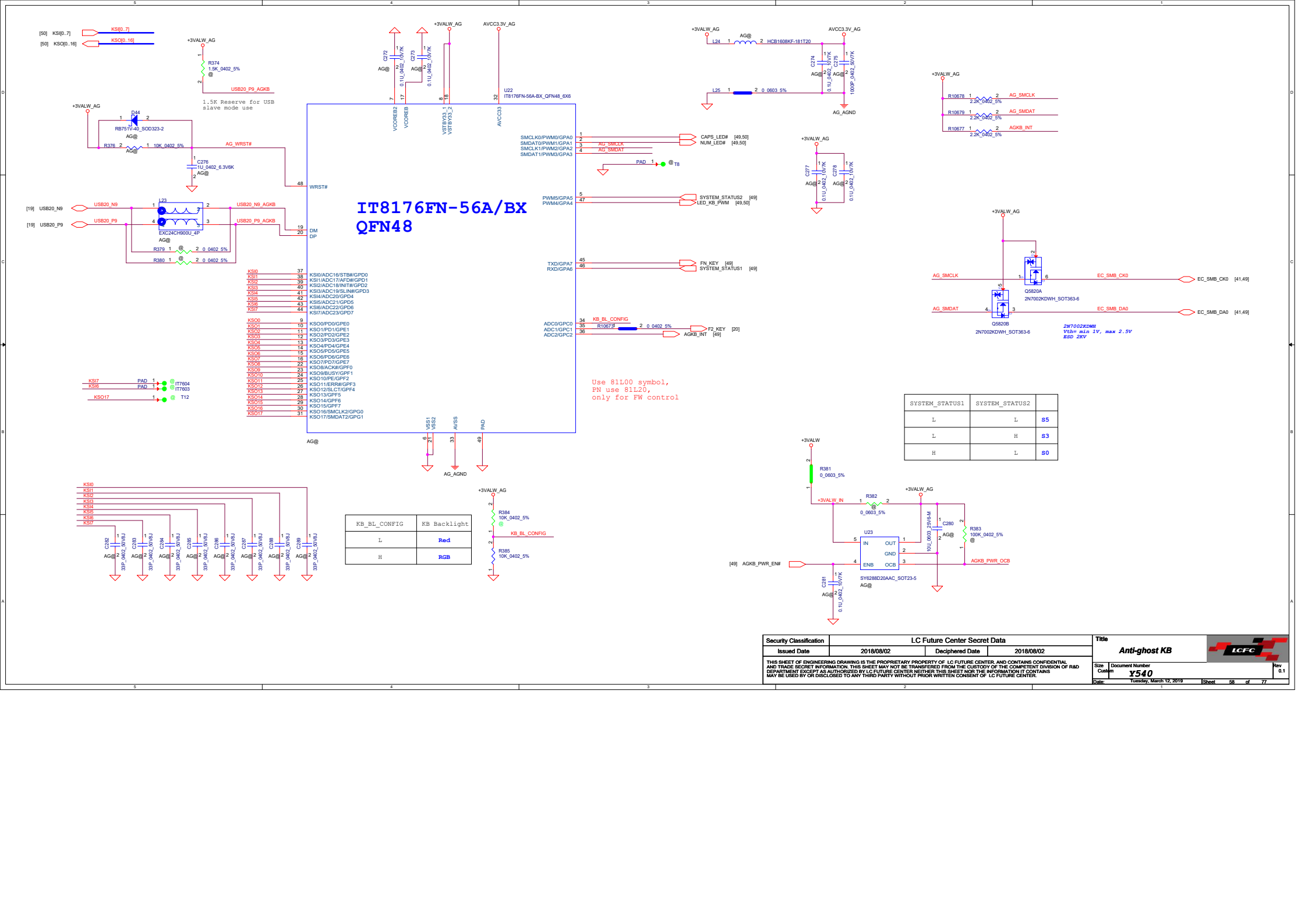
IT8176FN-56A/BX
QFN48
U22
IT8176FN-56A-BX_QFN48_6X6
1.5K Reserve for USB slave mode use
Use 81L00 symbol, PN use 81L20, only for FW control
EXC24CH900U_4P
SY8288D20AAC_SOT23-5
2N7002KDWH_SOT363-6
2N7002KDWH Vth= min 1V, max 2.5V ESD 2KV
KB_BL_CONFIG | KB Backlight
L | Red
H | RGB
SYSTEM_STATUS1 | SYSTEM_STATUS2
L | L | S5
L | H | S3
H | L | S0
Security Classification | LC Future Center Secret Data
Issued Date | 2018/08/02 | Deciphered Date | 2018/08/02
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HDMI Logo

ZZZ1 HDMI@

HDMI Logo
RO00000040J

PCB MB

ZZZ2

PCB FY715 NM-C541 NS-C541/C542/C543/C544
DAZ1EW00100

GPU

UV1

OPT18@
S IC N18P-G0-MP-A1 BGA 960P GPU 12 !
SA00009YG00

CPU

UC1 i5@

S IC CL8068404121905 QRR5 U0 2.4G BGA 1440
SA0000A0P10

UC1 i7@

S IC CL8068404121817 QRR2 U0 2.6G BGA 1440
SA0000A0N10

PCH

UH1

S IC FH82HM370 SR40B B0 BGA 874P PCH 12!
SA00009AG00

MICRON 4GB VRAM

ZZZ4 M4GX4@

Micron_4GB_VRAM
X7646R12001

HYNIX 4GB VRAM

ZZZ5 H4GX4@

HYNIX_4GB_VRAM
X7646R12002

SKU ID

RH157 15@
S RES 1/20W 10K +-5% 0201
SD04310028J

RH158 15@
S RES 1/20W 10K +-5% 0201
SD04310028J

RH157 7000P@
S RES 1/20W 10K +-5% 0201
SD04310028J

RH155 7000P@
S RES 1/20W 10K +-5% 0201
SD04310028J

RH152 17@
S RES 1/20W 10K +-5% 0201
SD04310028J

RH158 17@
S RES 1/20W 10K +-5% 0201
SD04310028J

GPU STRAP

RV325 OPT18@
10K_0402_1%
SD03410028J

RV325 OPT17@
100K_0402_1%
SD0341T0038J

GPU FB_CAL_TERM_GND

RV94 OPT18@
40.2_0402_1%
SD0340402A8J

RV94 OPT17@
60.4_0402_1%
SD0340604A8J

UV13 X76@
MT51J256M32HF-80:B
SA00007Z930

UV14 X76@
MT51J256M32HF-80:B
SA00007Z930

UV15 X76@
MT51J256M32HF-80:B
SA00007Z930

UV16 X76@
MT51J256M32HF-80:B
SA00007Z930

UV13 X76@
H5GC8H24AJR-R2C
SA00009FV00

UV14 X76@
H5GC8H24AJR-R2C
SA00009FV00

UV15 X76@
H5GC8H24AJR-R2C
SA00009FV00

UV16 X76@
H5GC8H24AJR-R2C
SA00009FV00

SW5 15@
SW EVQPQHB55
SN100006P00

D1 15@
AZ5725-01F
SC400008K00

U5 15@
AH9247-W-7
SA00007RN00

LED301 15@
B2972UDBS05P-000114
SC50000FR00

R3001 15@
150_0402_5%
SD02815008J

SW5 7000P@
SW EVQPQHB55
SN100006P00

D1 7000P@
AZ5725-01F
SC400008K00

U5 7000P@
AH9247-W-7
SA00007RN00

LED301 17@
B2972UDBS05P-000114
SC50000FR00

R3001 17@
150_0402_5%
SD02815008J

for N18P decoupling

CV1113 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV205 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV1140 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV68 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV1112 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV70 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV1114 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV311 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV7 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV222 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV479 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV486 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV477 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV71 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV473 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV206 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV223 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV1392 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

CV1115 OPT18@
1U_6.3V_K_X5R_0201
SE00000Z700

for N17P decoupling

CV1140 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV223 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV222 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV1113 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV68 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV479 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV1114 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV206 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV1115 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV70 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV473 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV311 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV1112 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV7 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV486 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV477 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV1392 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV205 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

CV71 OPT17@
0.1UC_6.3VC_KC_X7RC_0201
SE00001BL00

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Virtual symbol*

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H1
HOLEA
PAD_CT8P0B6P0D2P3

H3
HOLEA
PAD_CT8P0D2P5

H5
HOLEA
PAD_CT8P0B6P0D2P3

NH6
HOLEA
PAD_C5P0D5P0N

H7
HOLEA
PAD_ST8P0CB6P0D2P3

H8
HOLEA
PAD_ST8P0D2P5

H9
HOLEA
PAD_ST8P0D2P5
CHASSIS1_GND

H10
HOLEA
PAD_ST8P0CB8P0D2P5

NH11
HOLEA
PAD_O2P5X3P1D2P5X3P1N

H12
HOLEA
PAD_ST8P0D2P5

H13
HOLEA
PAD_ST8P0D2P5

H14
HOLEA
PAD_CB6P0D2P3

H15
HOLEA
PAD_CT5P5D3P2

H16
HOLEA
PAD_CT5P5D3P2

H17
HOLEA
PAD_CT5P5D3P0

H18
HOLEA
PAD_CT5P5D3P0

H19
HOLEA
PAD_CT5P5D3P2

H20
HOLEA
PAD_CT5P5D3P2

H21
HOLEA
PAD_CT5P5D3P2

H22
HOLEA
PAD_C8P0D4P5

NH23
HOLEA
PAD_C2P5D2P5N

NH24
HOLEA
PAD_O2P5X3P1D2P5X3P1N

H23
HOLEA
PAD_CT8P0D2P5

H24
HOLEA
PAD_CT8P0D2P5

add by Bing 04/08

SH9 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH13 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH16 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH10 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH14 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH17 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH11 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH15 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SH12 ME@
SHIELDING_SUL-35A2M_9P2X3P3_1P

SO-DIMM Shielding

FD1 FD2 FD3 FD4 FD5 FD6

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Blank*

Size: C	Document Number: Y540	Rev: 0.1
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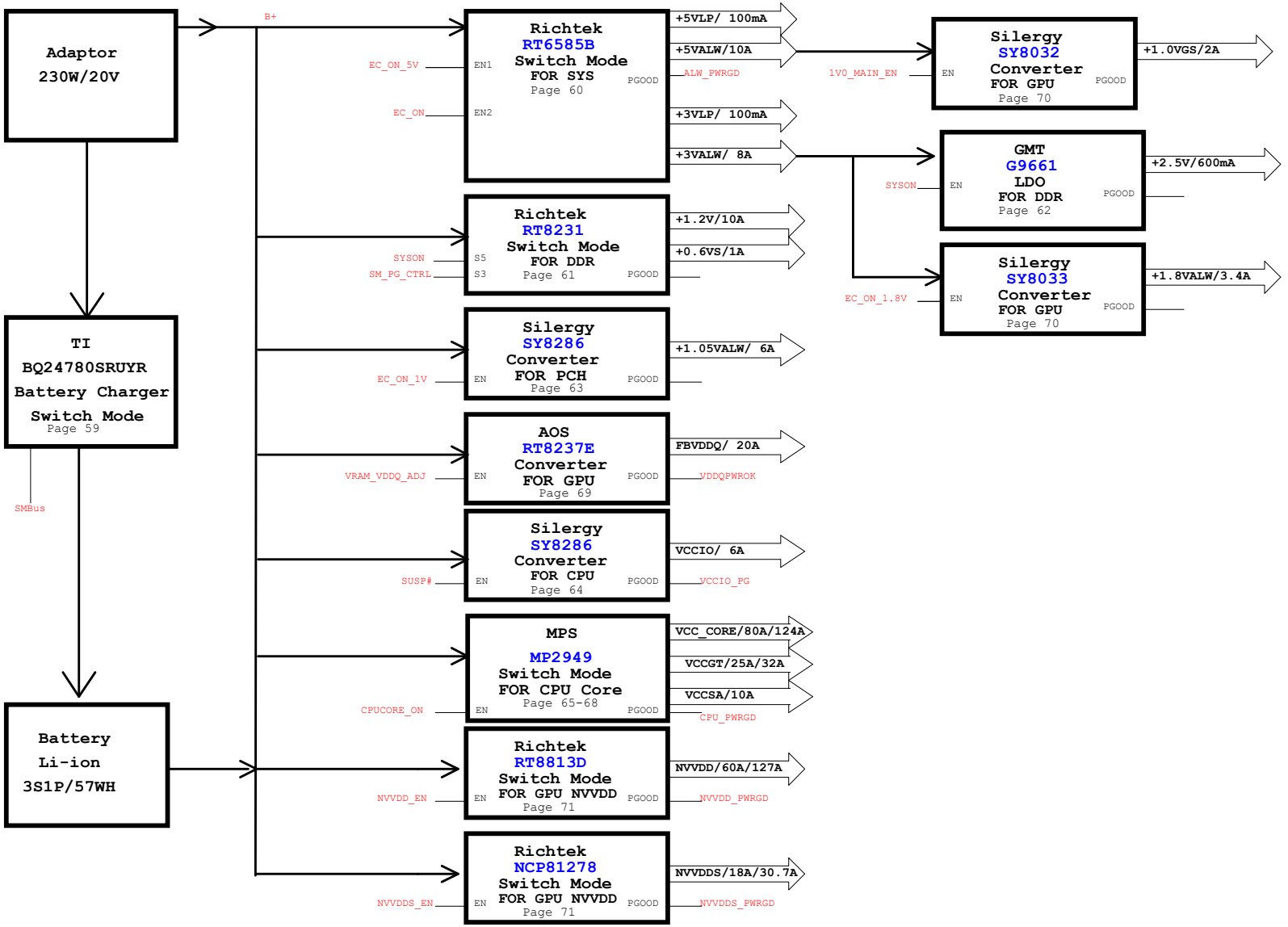
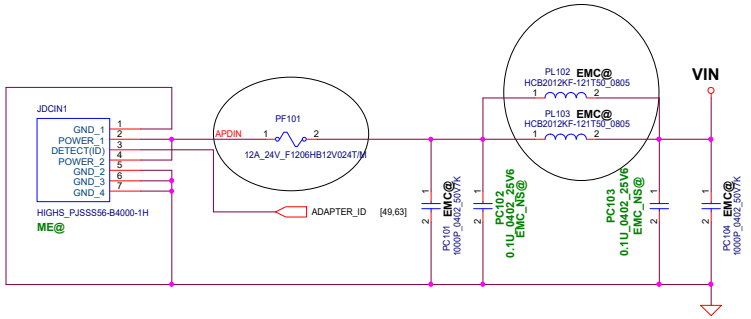


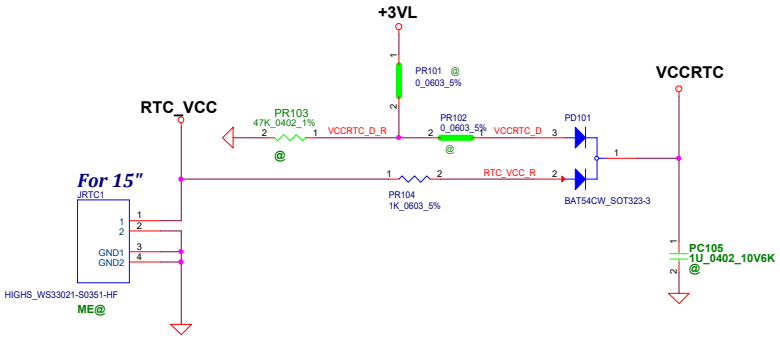
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

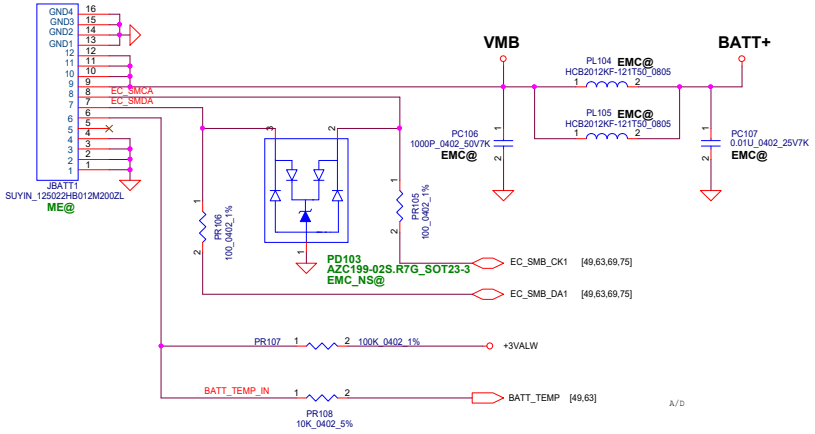
Title: **Power Diagram**

Size	Document Number	Rev
Custom	Y540	0.1

Date: Tuesday, March 12, 2019 Sheet 61 of 80







Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN/BATT/RTC		
Size C	Document Number Y540		Rev 0.1
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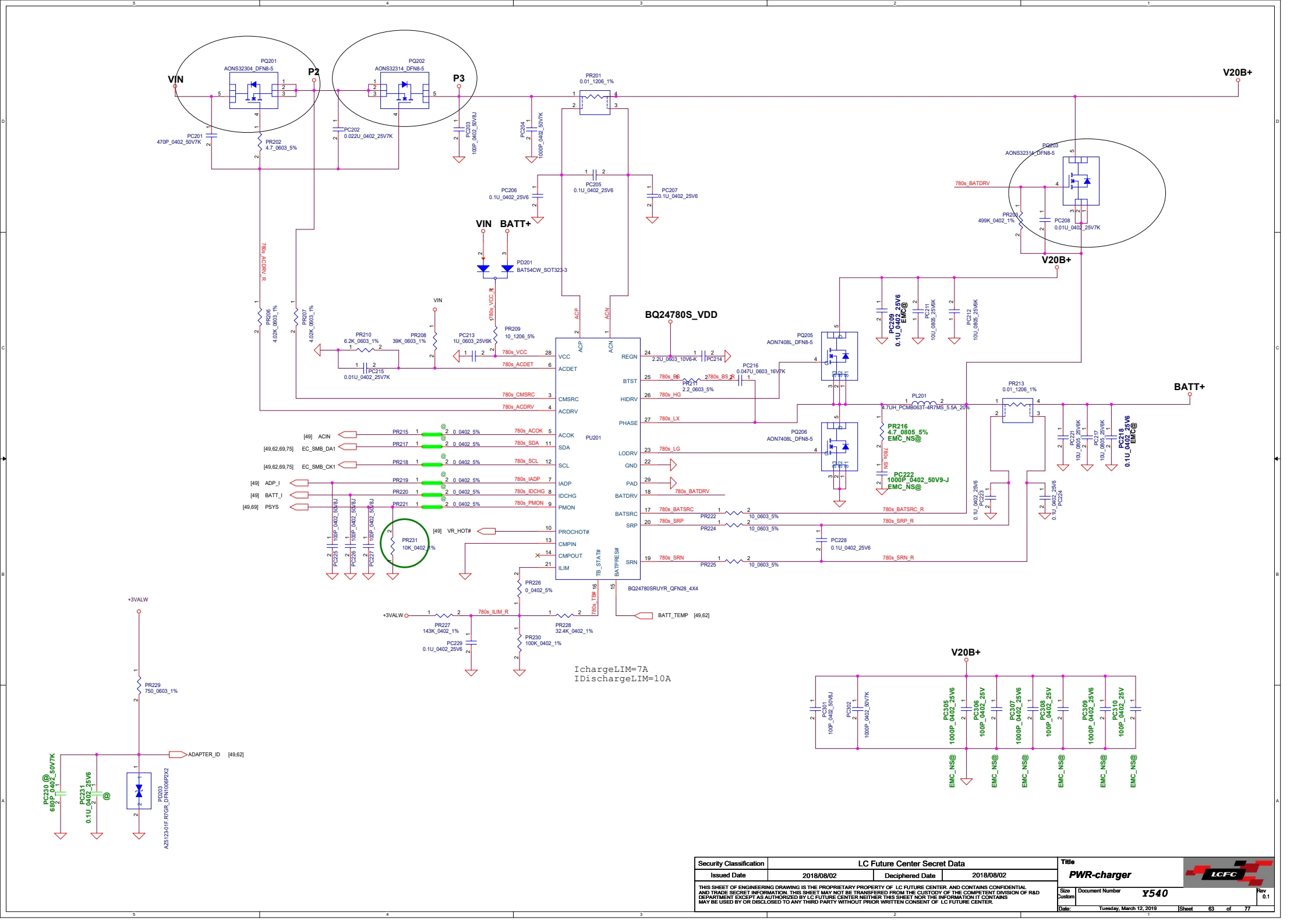
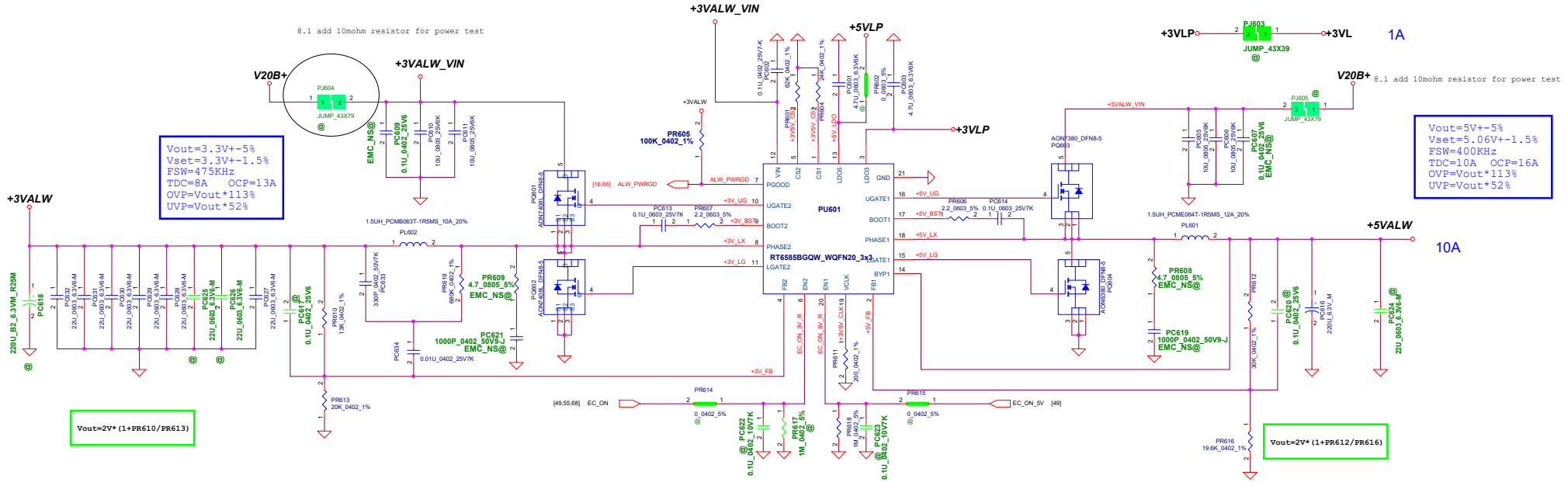


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-charger		
Size: Custom	Document Number: Y540		Rev: 0.1
Date: Tuesday, March 12, 2019	Sheet 63 of 77		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-3/5VALW

Size: Custom | Document Number: Y540 | Rev: 0.1

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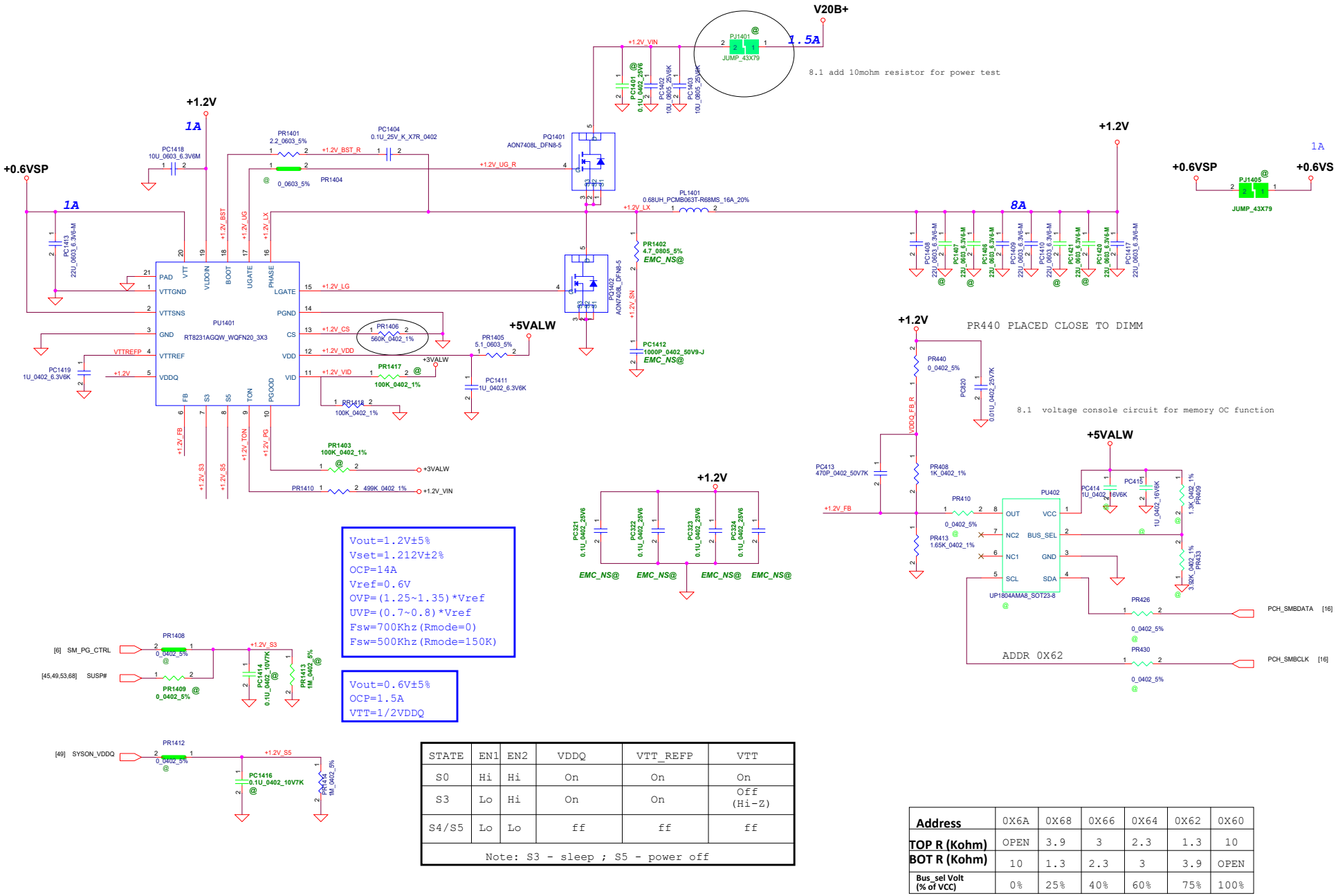

Vout=1.2V±5%
Vset=1.212V±2%
OCP=14A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz(Rmode=0)
Fsw=500Khz(Rmode=150K)

Vout=0.6V±5%
OCP=1.5A
VTT=1/2VDDQ

STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	ff	ff	ff

Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VDDQ/VTT

Size	Document Number	Rev
C	Y540	0.1

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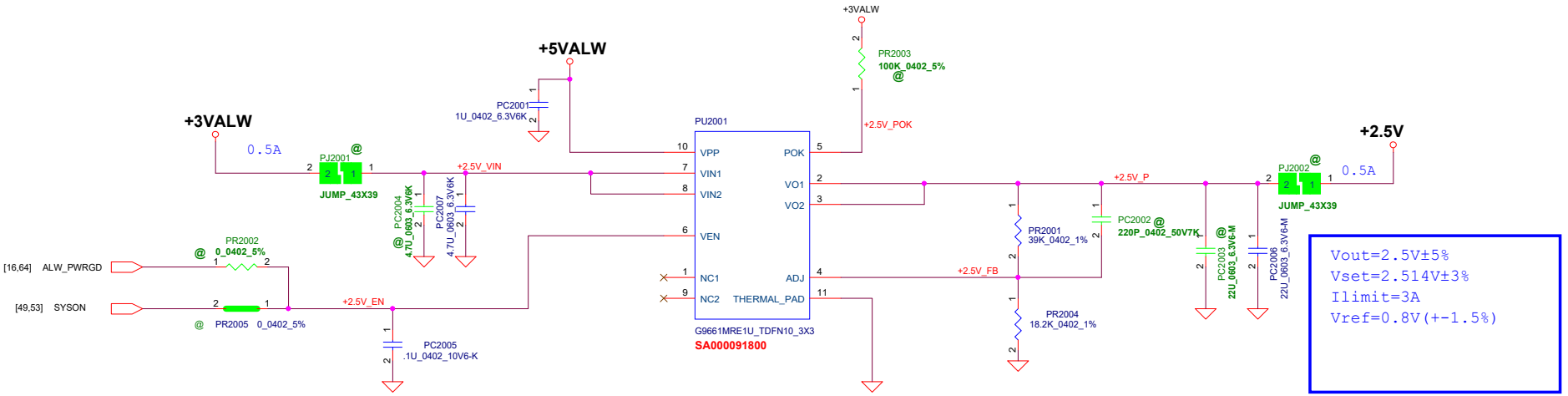

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-2.5V**

Size: Custom	Document Number: Y540	Rev: 0.1
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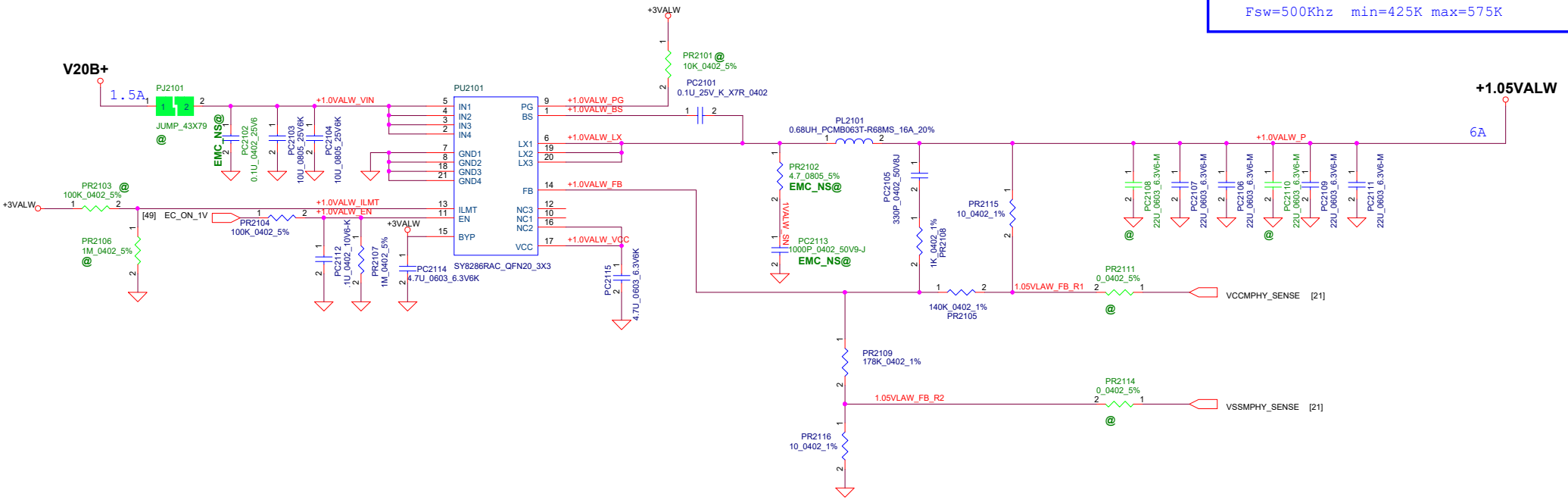
Vout=1.05V±5%
Vset=1.051V±1.81%
Vref=0.6V(+-1%)
TDC=8A
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.0VALW**

Size: Custom	Document Number: Y540		Rev: 0.1
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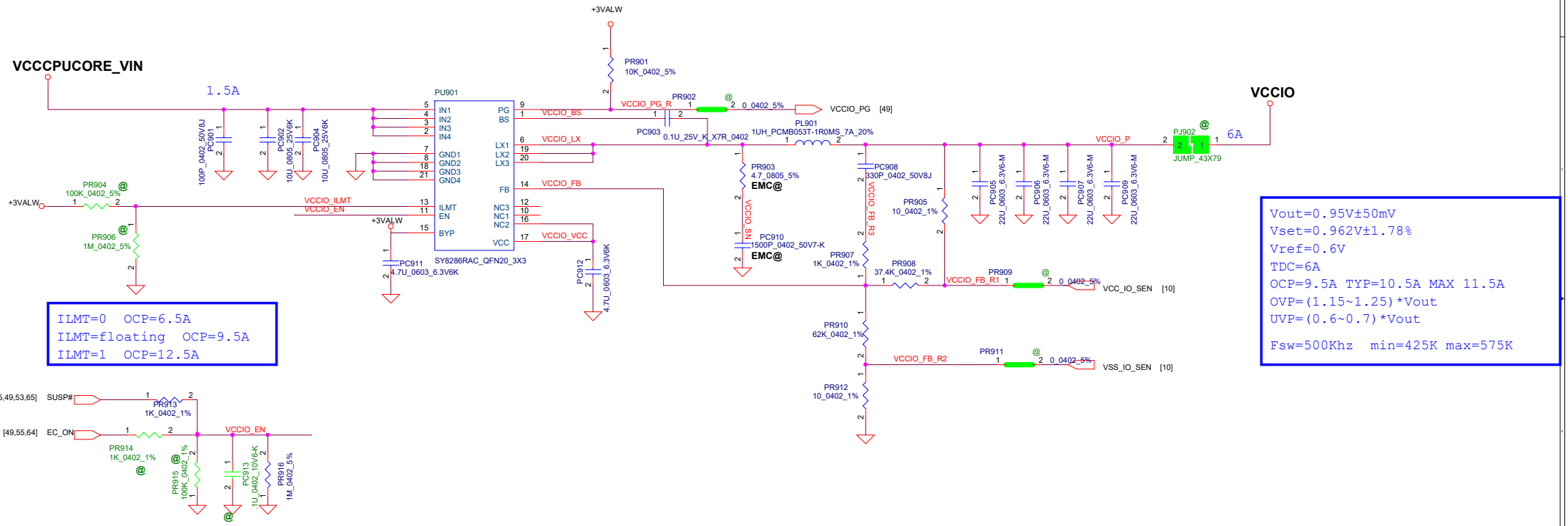
VCCIO 20VB+ change to Core VIN for layout



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCIO

Size	Document Number	Rev
Custom	Y540	0.1

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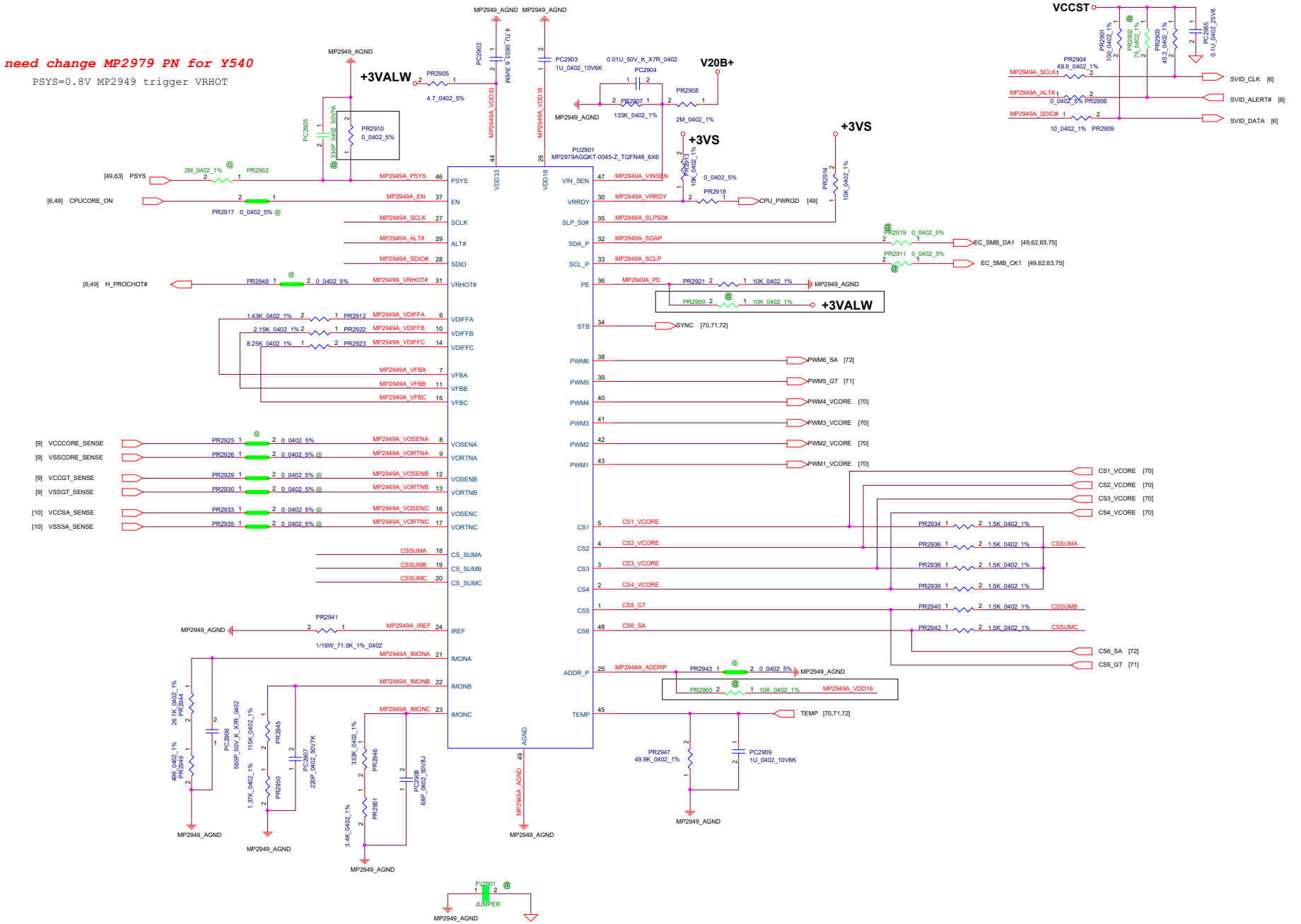

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Issued Date	2016/01/20	Deciphered Date	2016/01/20

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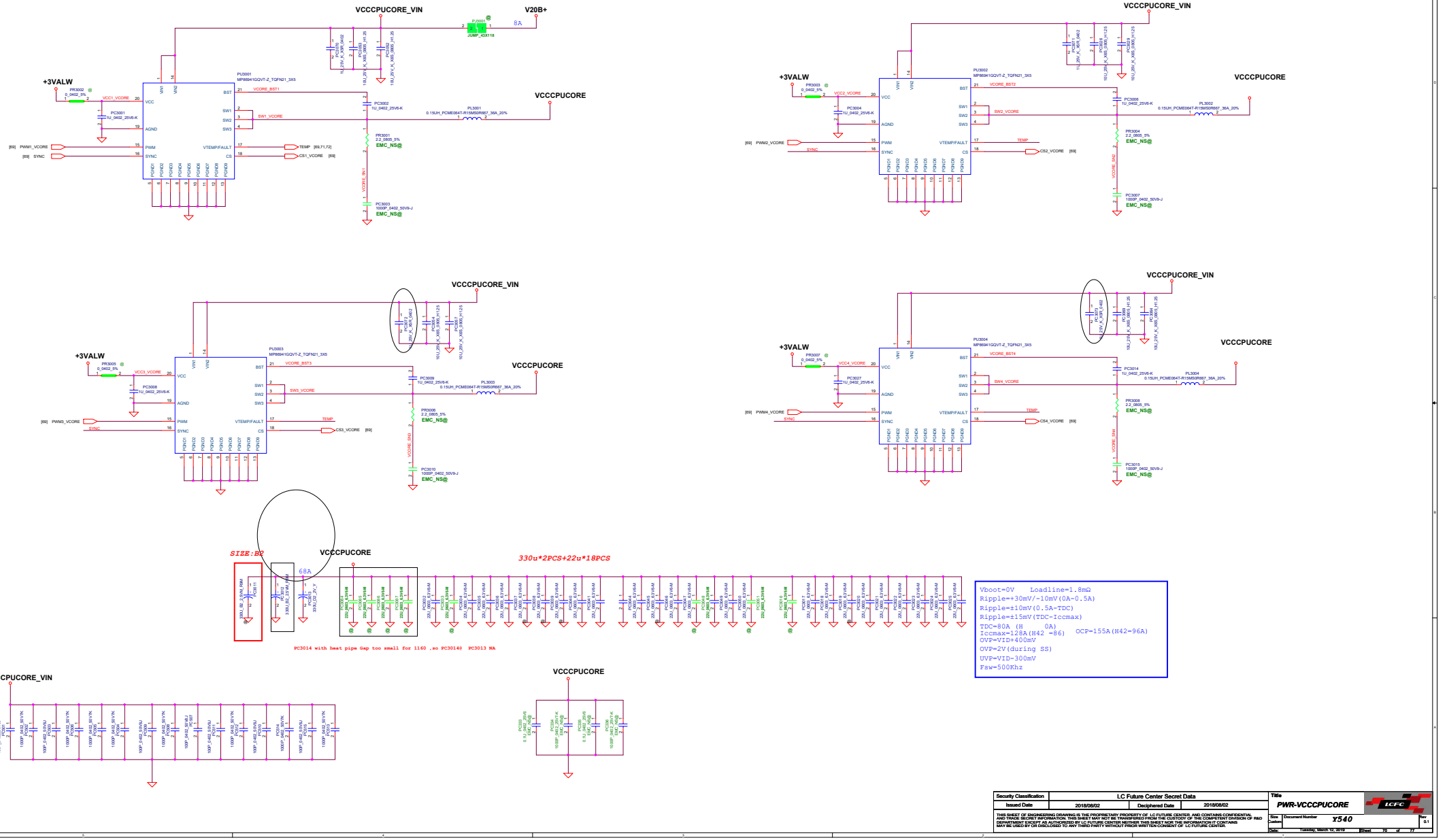
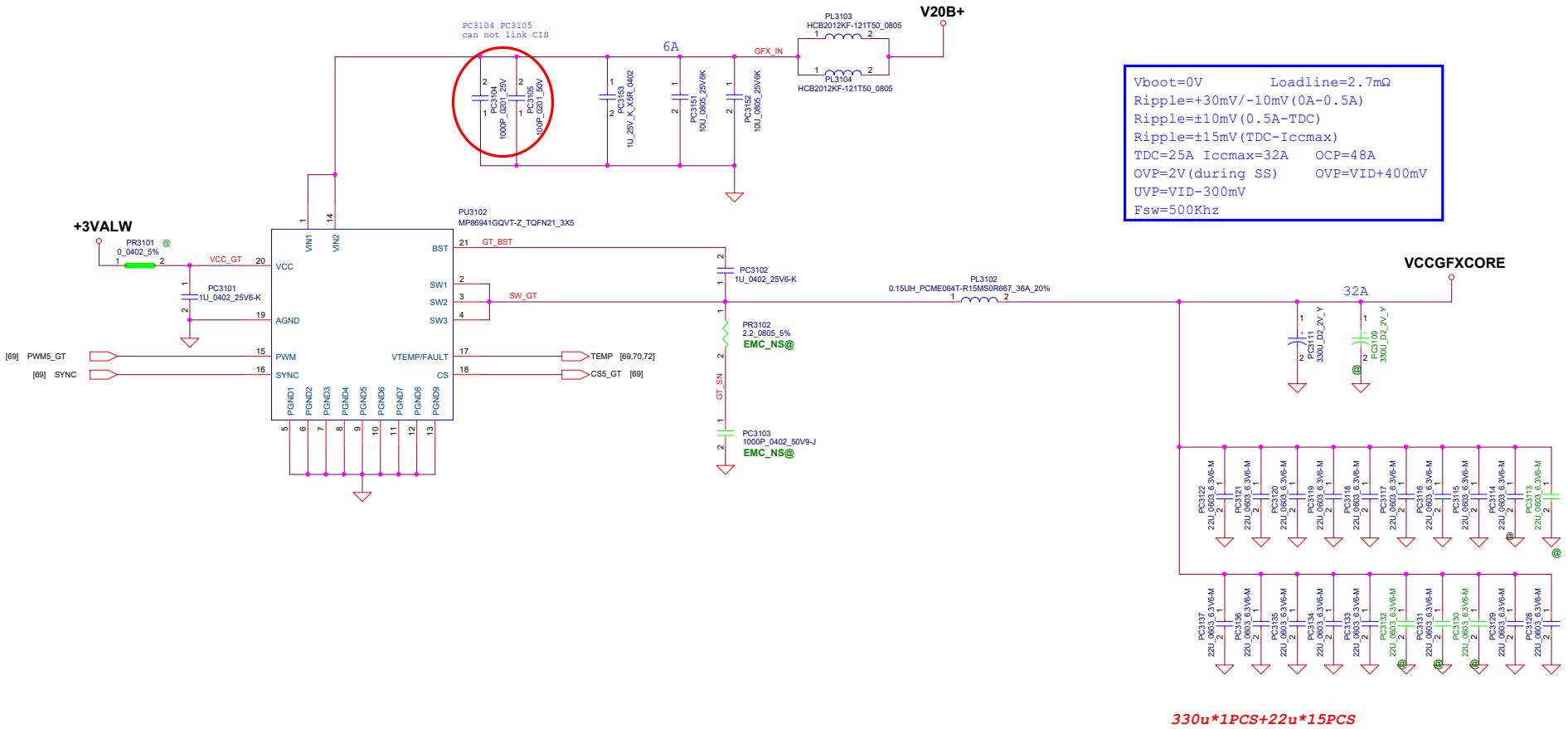
Title	PWR-IMVP8_MP2949		
Size: Custom	Document Number: EY52U		Rev: 0.1
Date: Tuesday, March 12, 2019	Sheet 69 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-VCCCPUCORE		
Size: Custom	Document Number: ¥540		Rev: 0.1
Date: Tuesday, March 12, 2019	Sheet 79 of 77		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCGFXCORE

Size: Custom	Document Number: Y540	Rev: 0.1
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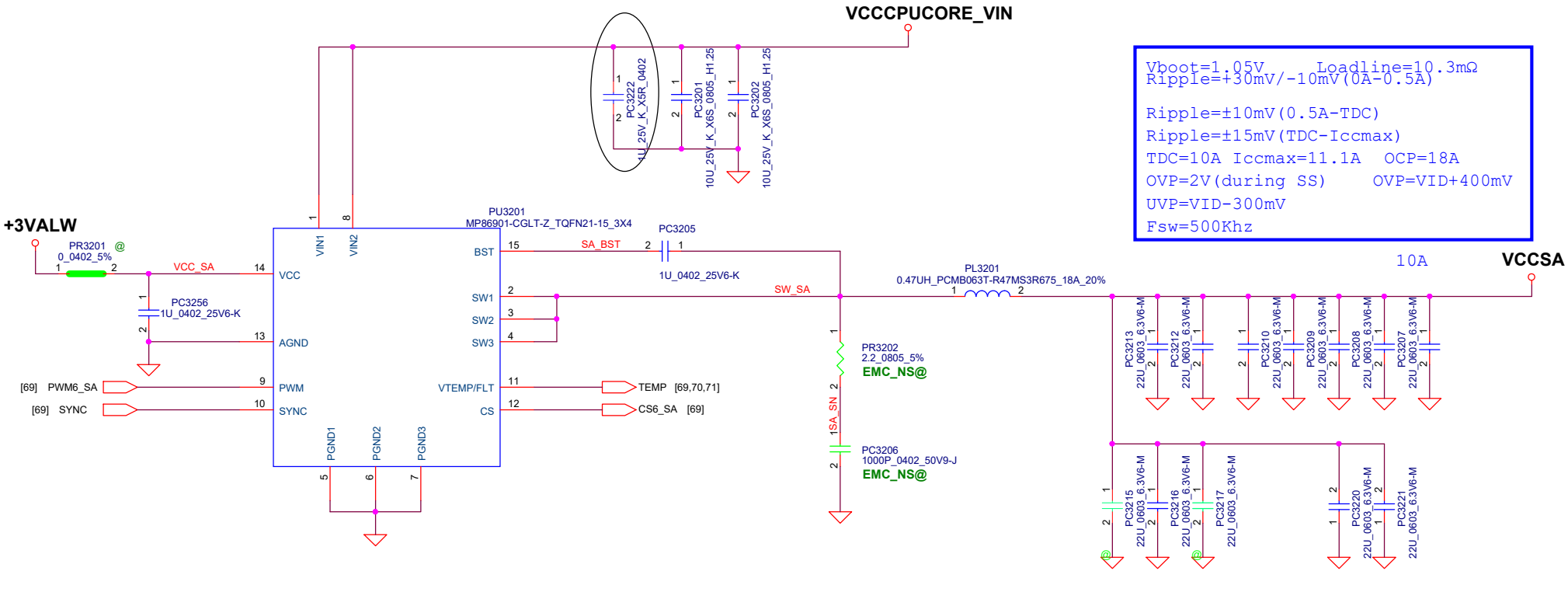

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCSA**

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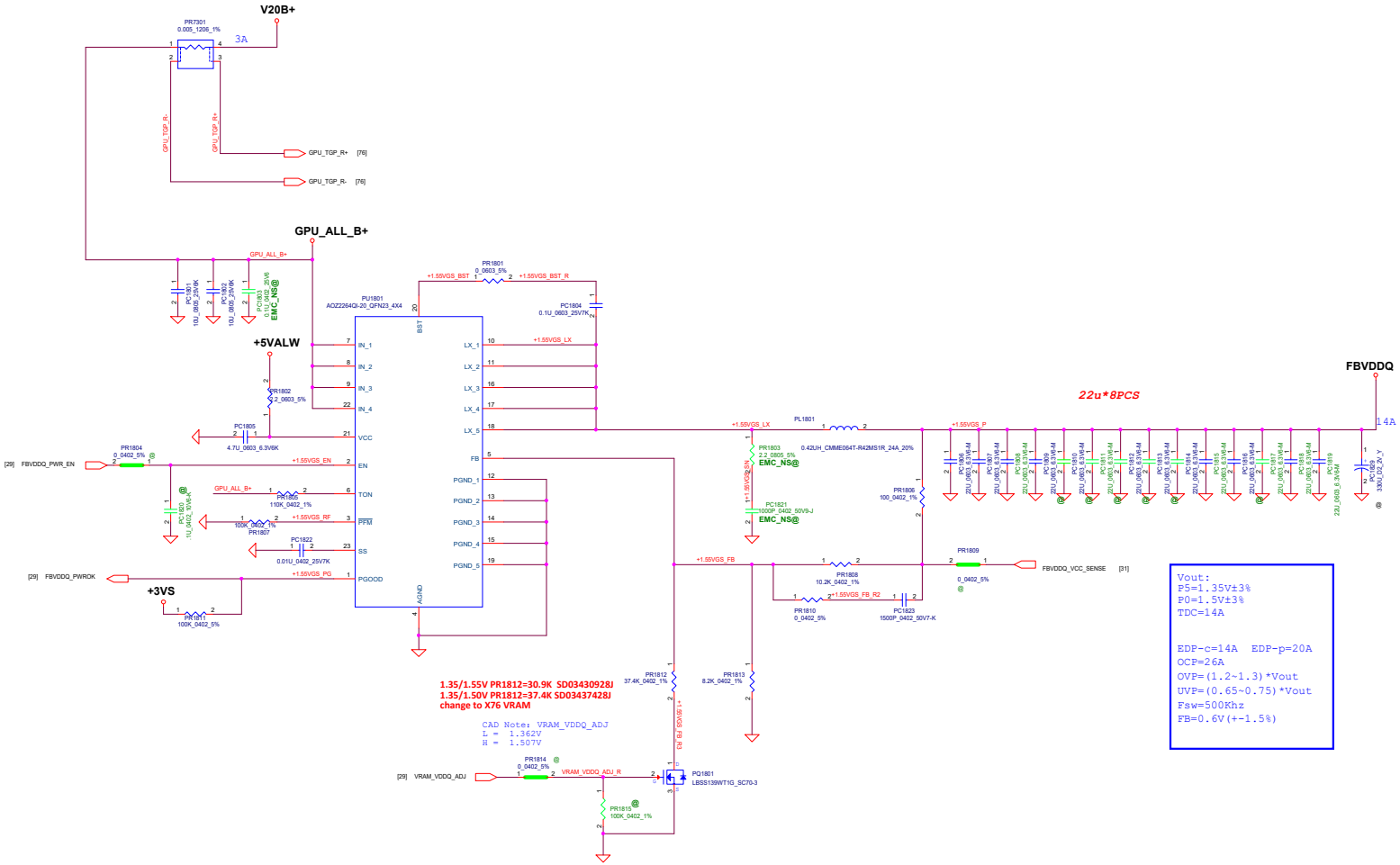

Title			
PWR-FBVDDQ			
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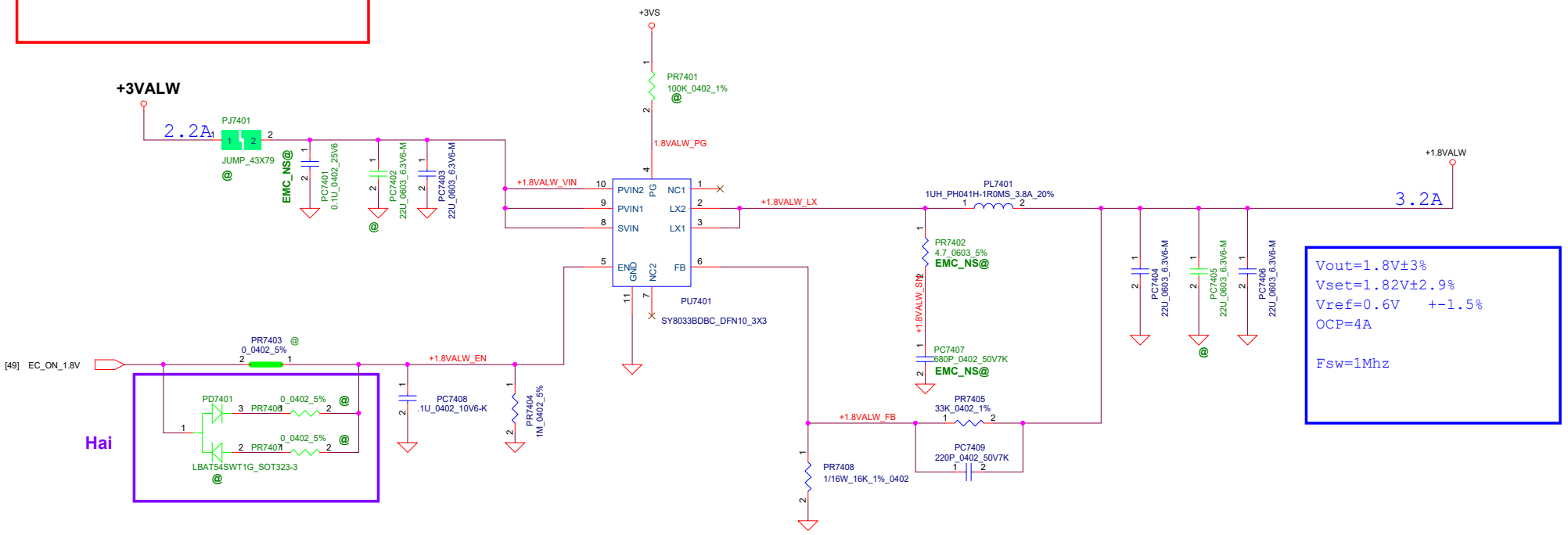
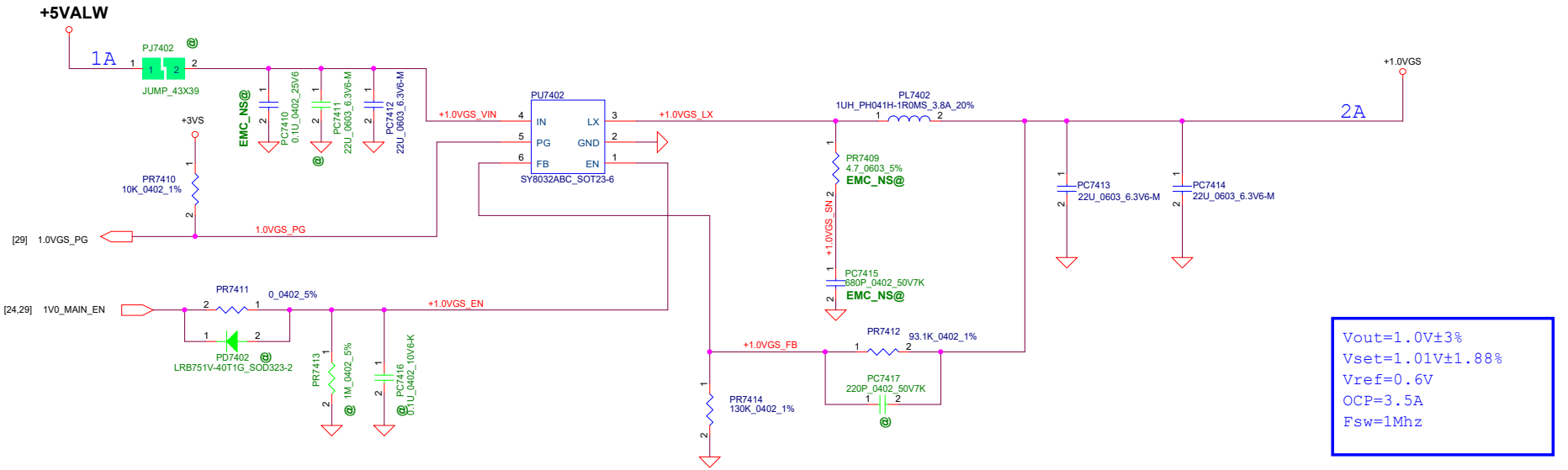
1.8V VIN change to 3.3V





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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.8/1.0VGS**

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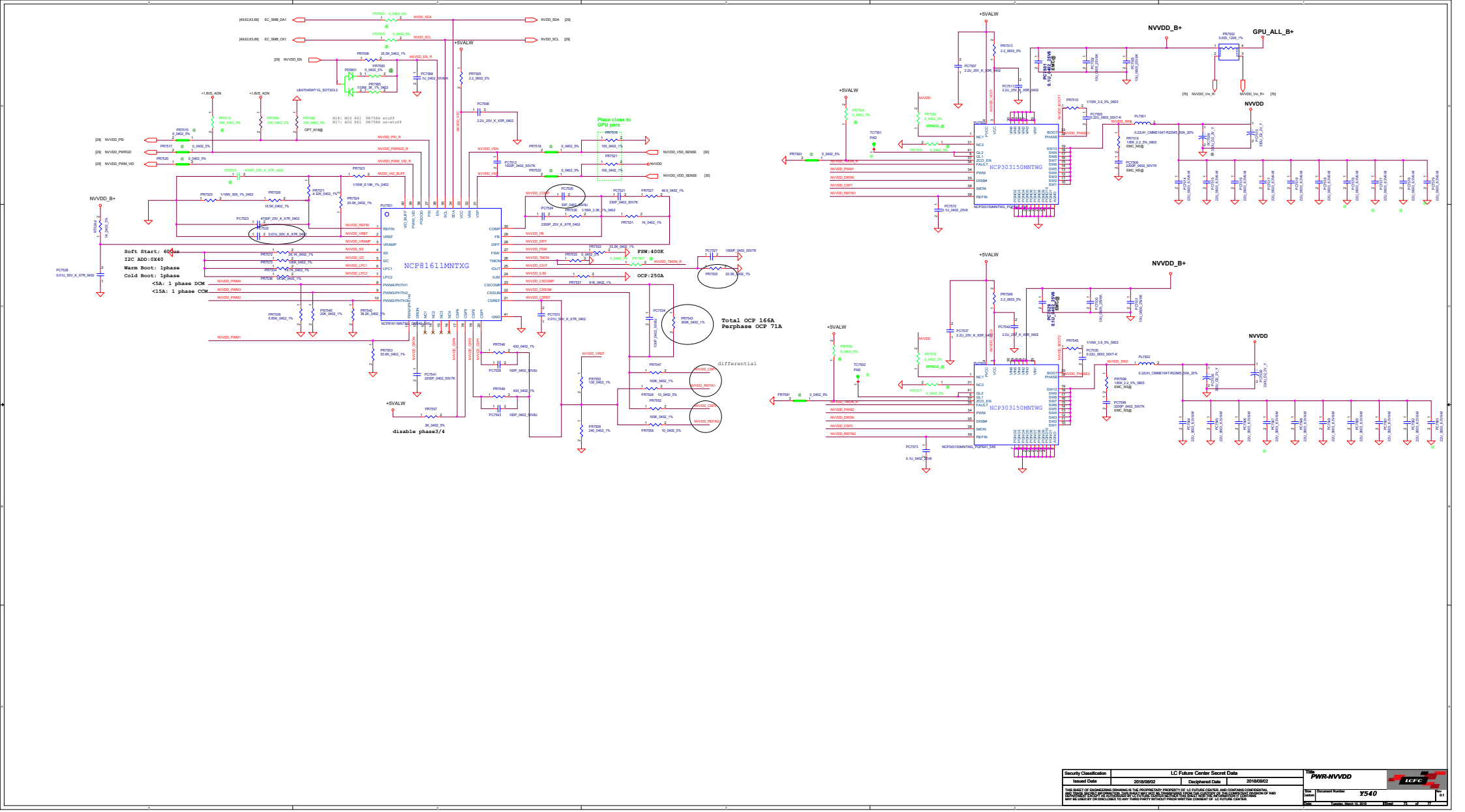

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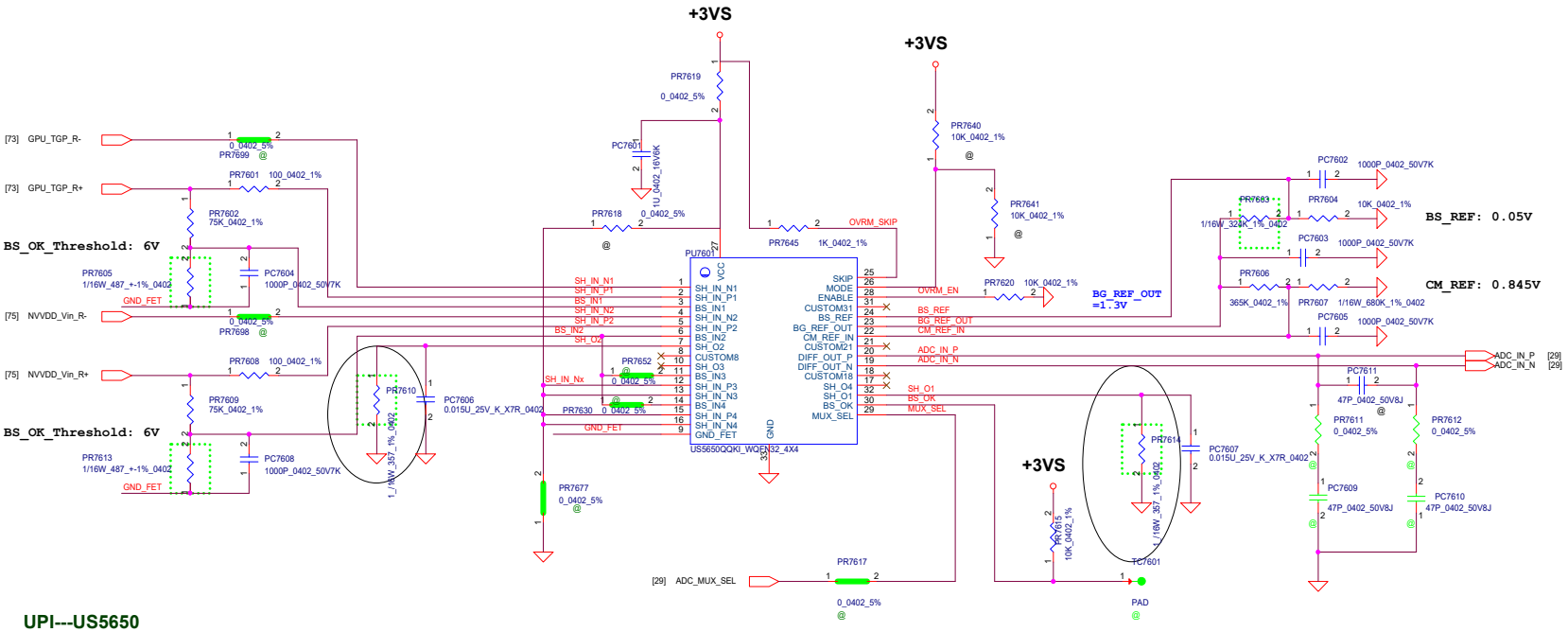

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Title: *Virtual symbol*

Size	Document Number	Rev
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