Compal Confidential

DIS M/B Schematics Document

AMD Raven Ridge FP5 APU with DDR4

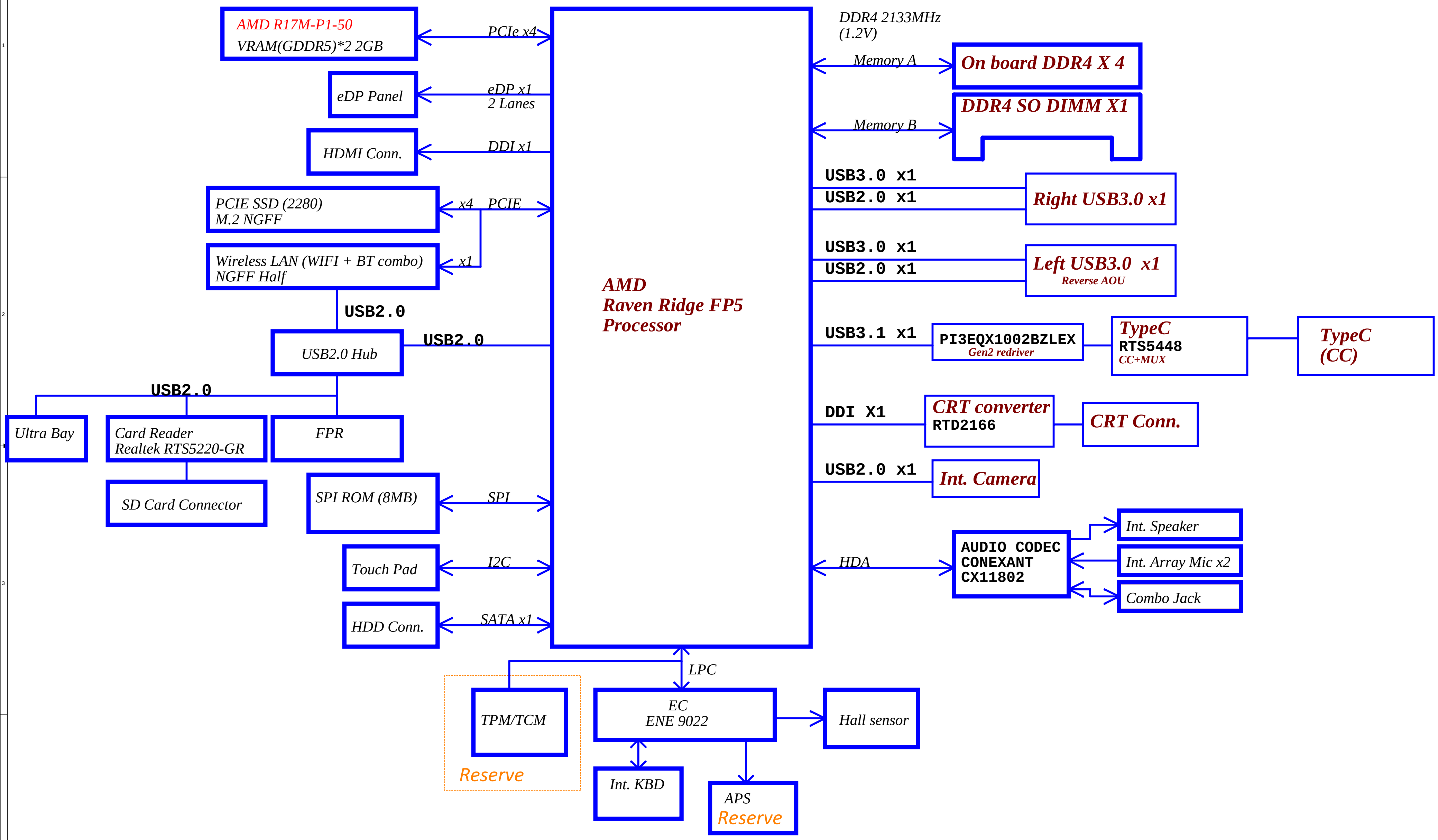
AMD R17M-P1-50

2017-09-12

LA-F485PR02

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: Cover Page
				Size: C; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 1 of 54

20141107B



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: Cover Page	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: C / Document Number: LA-F485P	Rev: 0.2
				Date: Monday, December 18, 2017	Sheet 2 of 54

Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.8VALW	0.95V always on power rail	ON	ON	ON
+0.8VS	0.95V switched power rail	ON	OFF	OFF
+1.2V_DDR	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V_MEM	2.5V power rail for DDR	ON	ON	OFF
+0.6VS_VTT	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VS_VRAM	1.35V switched power rail for VGA DDR	ON	OFF	OFF
+VDDCI	0.8V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON

STATE / SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

CPU

UC1
SA0000ASA10
RAVEN7 YM2700C4T4MFB 2G
RAVEN7@

UC1
SA0000A8R10
RAVEN5 YM2500C4T4MFB 1.8G
RAVEN5@

UC1
SA0000BIT10
RAVEN3 YM2300C4T4MFB 2G
RAVEN3@

DDR X76

ZZZ
X76DDR4H@
1G HYNIX
X7675138L21

ZZZ
X76DDR4M@
1G MICRON
X7675138L22

ZZZ
X76DDR4S@
1G SAMSUNG
X7675138L23

PCB

ZZZ
DA8001DB000
PCB 267 LA-F485P REV0 M/B

EMC X4E

ZZZ
X4ED@
X4E DIS
X4EA9638L01

ZZZ
X4EU@
X4E Ultra
X4EA9638L02

dGPU

UV1
DIS@
S IC 216-0905018 A1 R17M-P1-50 FCBGA 769P 0FA
SA0000ALV10

VRAM X76

X7675138L25 X7675138L24 X7675138L26

ZZZ
X7675138L25
M2G@

ZZZ
X7675138L24
H2G@

ZZZ
X7675138L26
S2G@

Card Reader X76

ZZZ
X7675138L61
X76RT@
RTS5146

ZZZ
X7675138L62
X76GL@
GL835

BOM Structure Table

BOM Structure	Item	BOM Structure	Item
UMA@	For UMA	X76RT@	Card Reader Realtek
DIS@	For DIS	X76GL@	Card Reader GENESYS
ME@	ME part	X76DDR4H@	Onboard RAM HYNIX
EMI@	EMI pop componemt	X76DDR4M@	Onboard RAM MICRON
@EMI@	EMI Unpop component	X76DDR4S@	Onboard RAM SAMSUNG
ESD@	ESD pop component	H2G@	For HYNIX 2G VRAM
@ESD@	ESD Unpop component	S2G@	For SAMSUNG 2G VRAM
ULTESD@	ESD Ultra Bay pop componemt	M2G@	For MICRON 2G VRAM
RF@	RF pop component	X4ED@	EMC component for DIS
@RF@	RF Unpop component	X4EU@	EMC component for UMA
@	Unpop	X76@	X76 part
VGA@	VGA component		
HDT@	For HDT Debug used		
FP@	Finger Print Component		
KBL@	KeyBoard Backlight component		
NOTPM@	No TPM/TCM Component		
TPM@	TPM Component		
TCM@	TCM Component		
AOU@	AOU Component		
NONAOU@	NONAOU Component		
APS@	APS Component		
NONAPS@	No APS Component		
BATT2@	Ultra bay Component		
NONBATT2@	Non Ultra bay Component		
SBATT@	2nd BATT SKU		
NONSBATT@	Non 2nd BATT SKU		
STE@	Stereo SPK		
MONO@	Mono SPK		
SDP@	DDR SDP Component		
DDP@	DDR DDP Component		
RAVEN7@	RAVEN7 CPU		
RAVEN5@	RAVEN5 CPU		
RAVEN3@	RAVEN3 CPU		
8M@	BIOS 8M		
16M@	BIOS 16M		

SMBUS Control Table

	SOURCE	VGA	BATT	EC	SODIMM	WLAN	APU
EC_SMB_CK1 EC_SMB_DA1	9022 +3VALW	X	V +3VALW	V +3VALW	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X
EC_SMB_CK2 EC_SMB_DA2	9022 +3VS	X	X	V +3VALW	X	X	V +1.8VS (+3VS)

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	GPU	0x41/0x41	
Charger	0001 0010 b	12H	APS	3Dh/3Ch	
			VGA Converter	0x64/0x65	

USB OC MAPPING

OC#	USB Port	
0	USB20_0_port2	
1	USB20_1_port0	
2	USB HUB	
3		

APU SM Bus address

	Device	Address	HEX
SM Bus 0	DDR DIMM1	1010 001Xb	A2H

APU I2C Bus address

	Device	Address
I2C 3	Touch Pad (Synaptics) Touch Pad (Elan)	$2C 0X15

GPP Port Table

Port	Device
GPP0	SSD (PCIE)
GPP1	
GPP2	
GPP3	
GPP4	LAN (PCIE)
GPP5	WLAN (PCIE)
GPP6	HDD (SATA)
GPP7	

DisplayPort Table

Port	Device
0	eDP
1	HDMI
3	DisplayPort -> CRT
2	

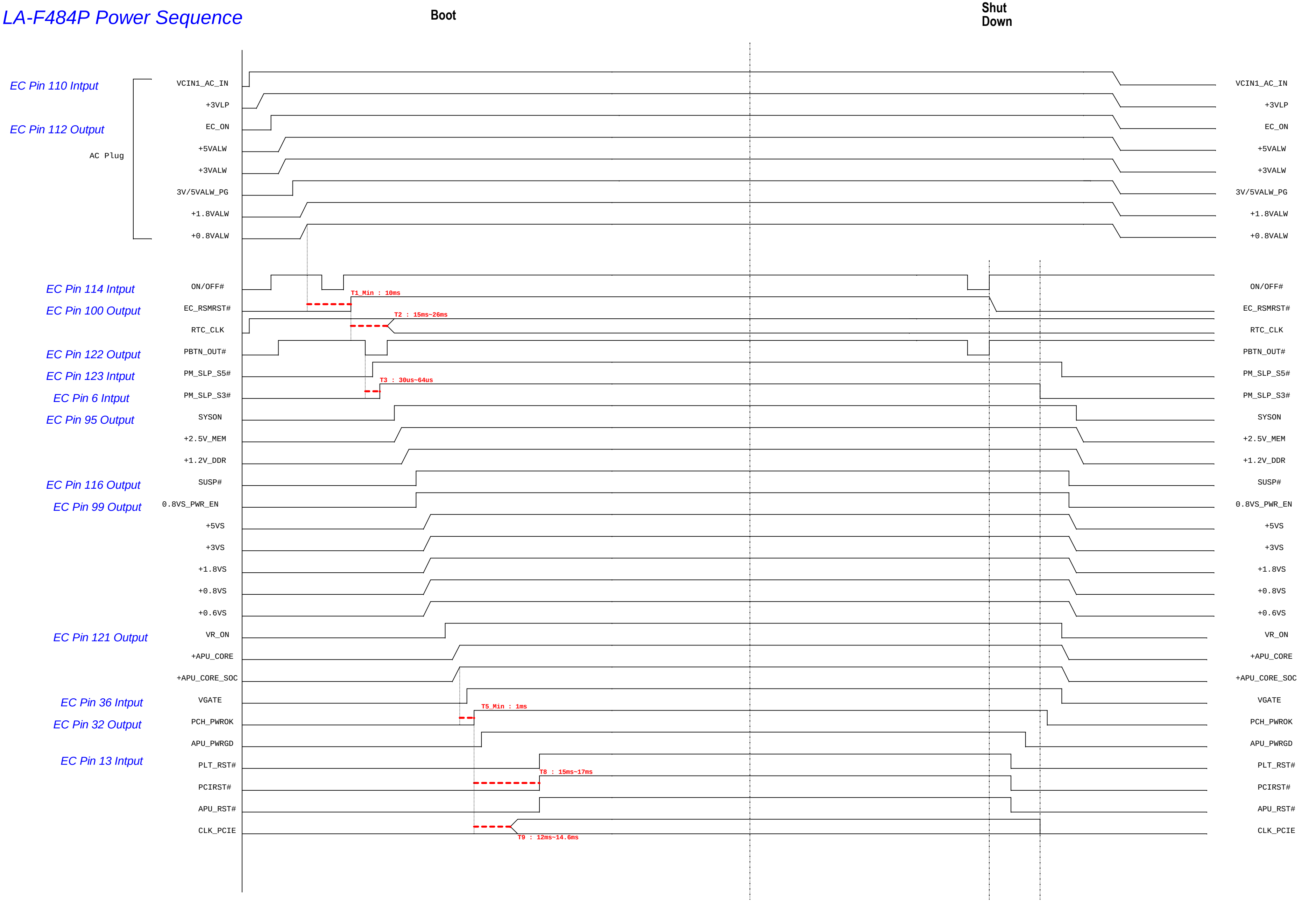
USB3.0 Port Table

Port	Device
0	
1	Type C Right
2	USB3.0 Left
3	USB3.0 Right
4	

USB2.0 Port Table

Port	Device
0	Camera
1	Type C Right
2	USB3.0 Left
3	USB3.0 Right
4	
5	USB Hub
5-1	Card Reader
5-2	BT
5-3	Ultra Bay
5-4	FP

LA-F484P Power Sequence



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

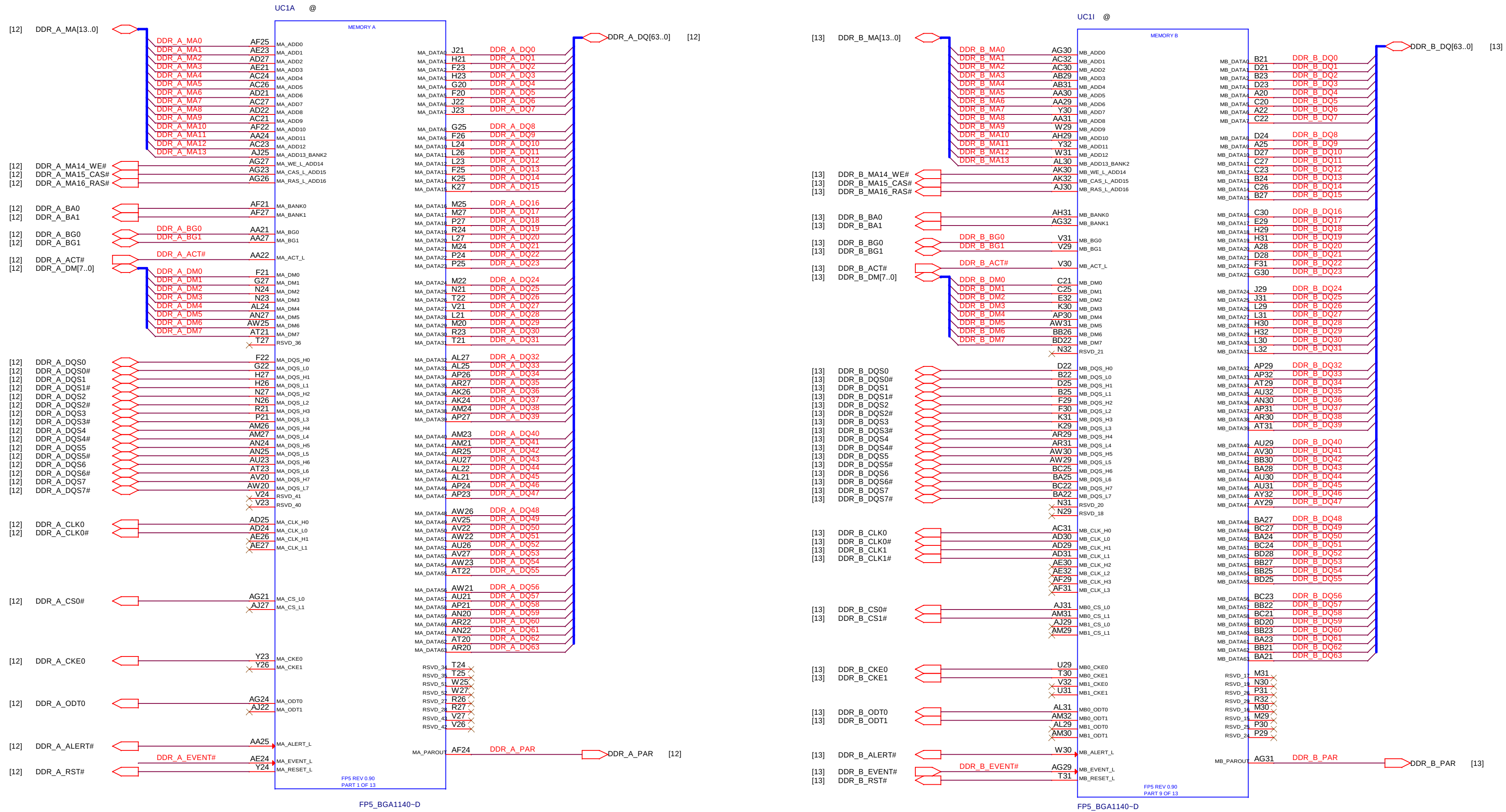
Compal Electronics, Inc.

Title: Power Sequence

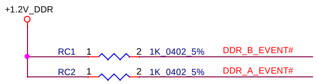
Size: C | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017 | Sheet 4 of 54

Main Func = CPU



EVENT# pull high

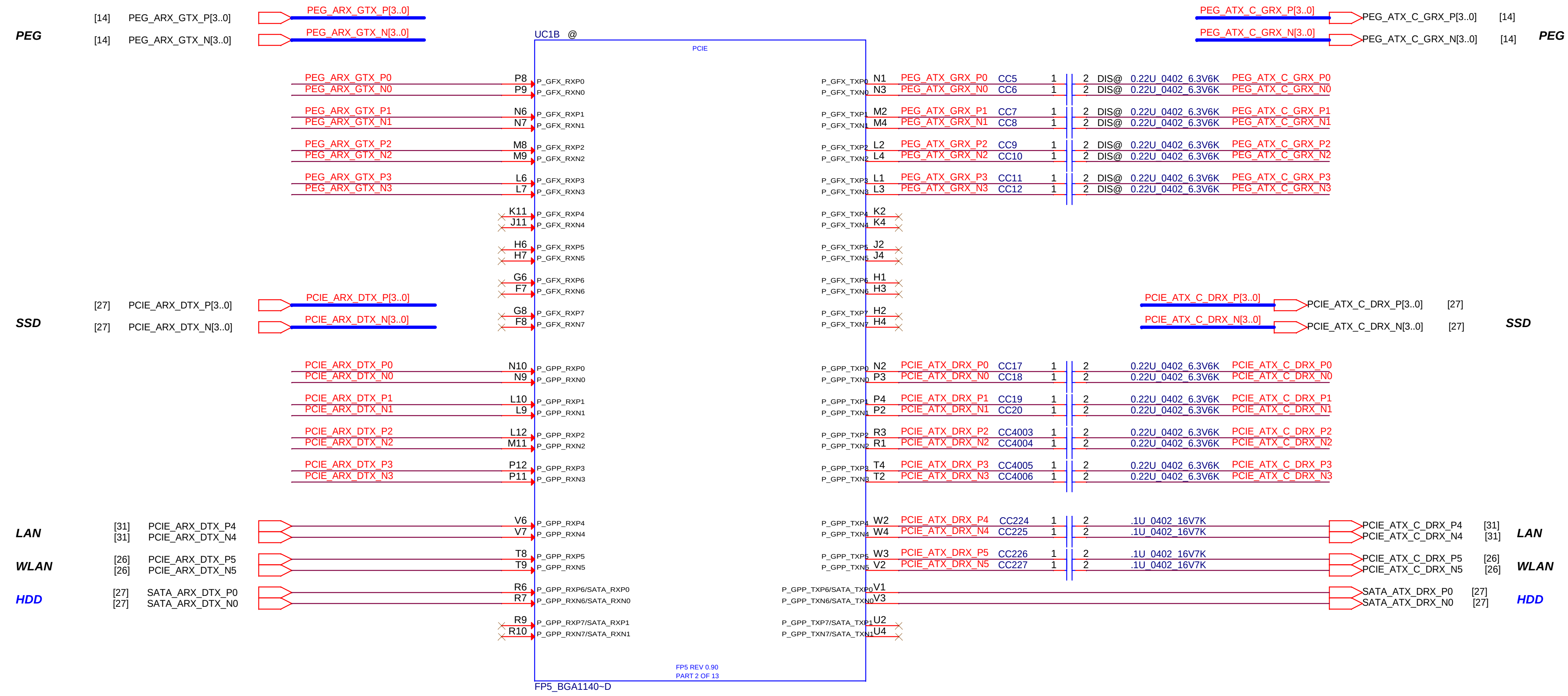


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date 2017/01/07	Title: FP5 DDR4 MEMORY I/F

Size	Document Number	Rev
Custom	LA-F485P	0.2

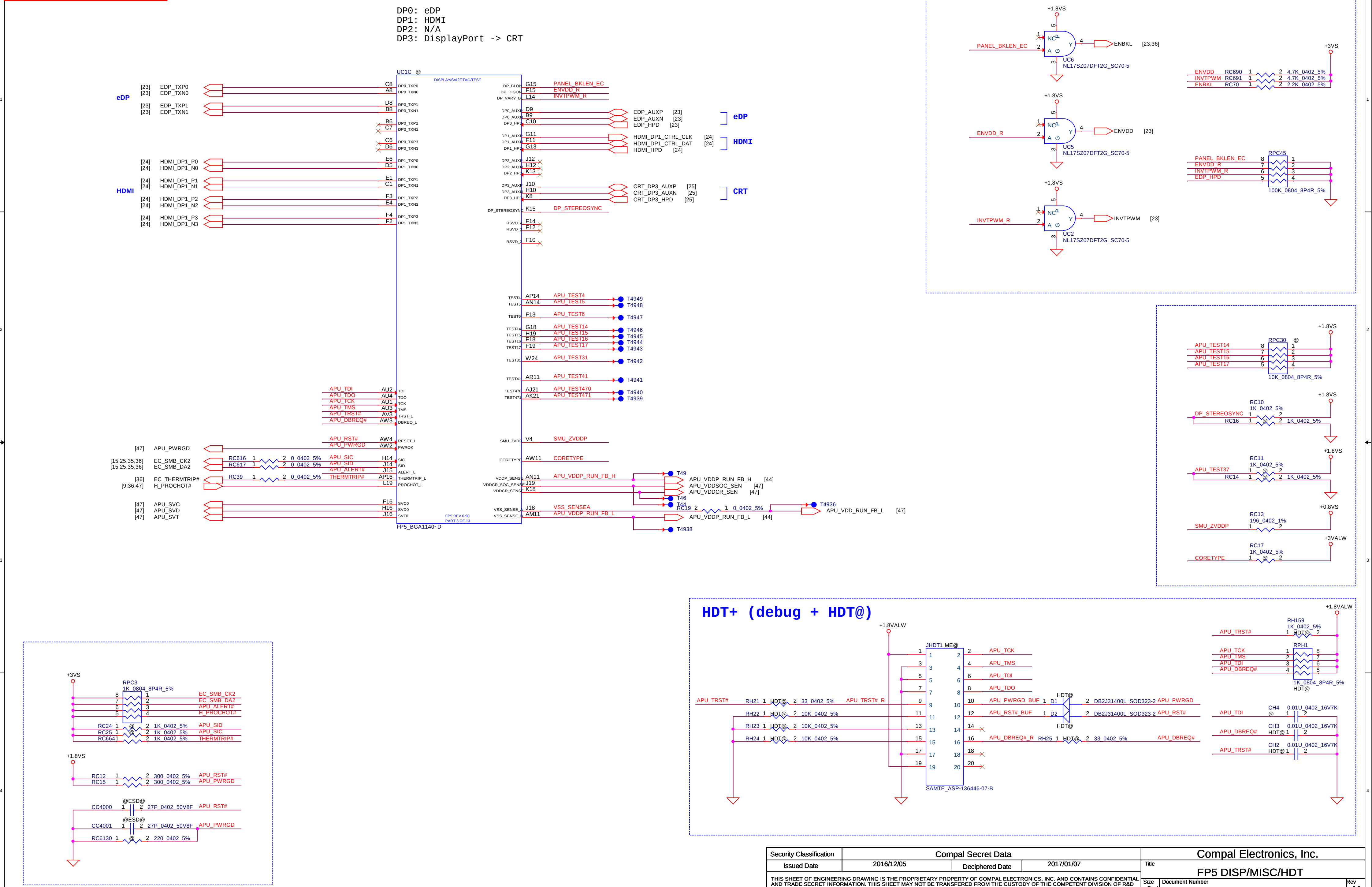
Date: Monday, December 18, 2017 | Sheet 5 of 54

Main Func = CPU



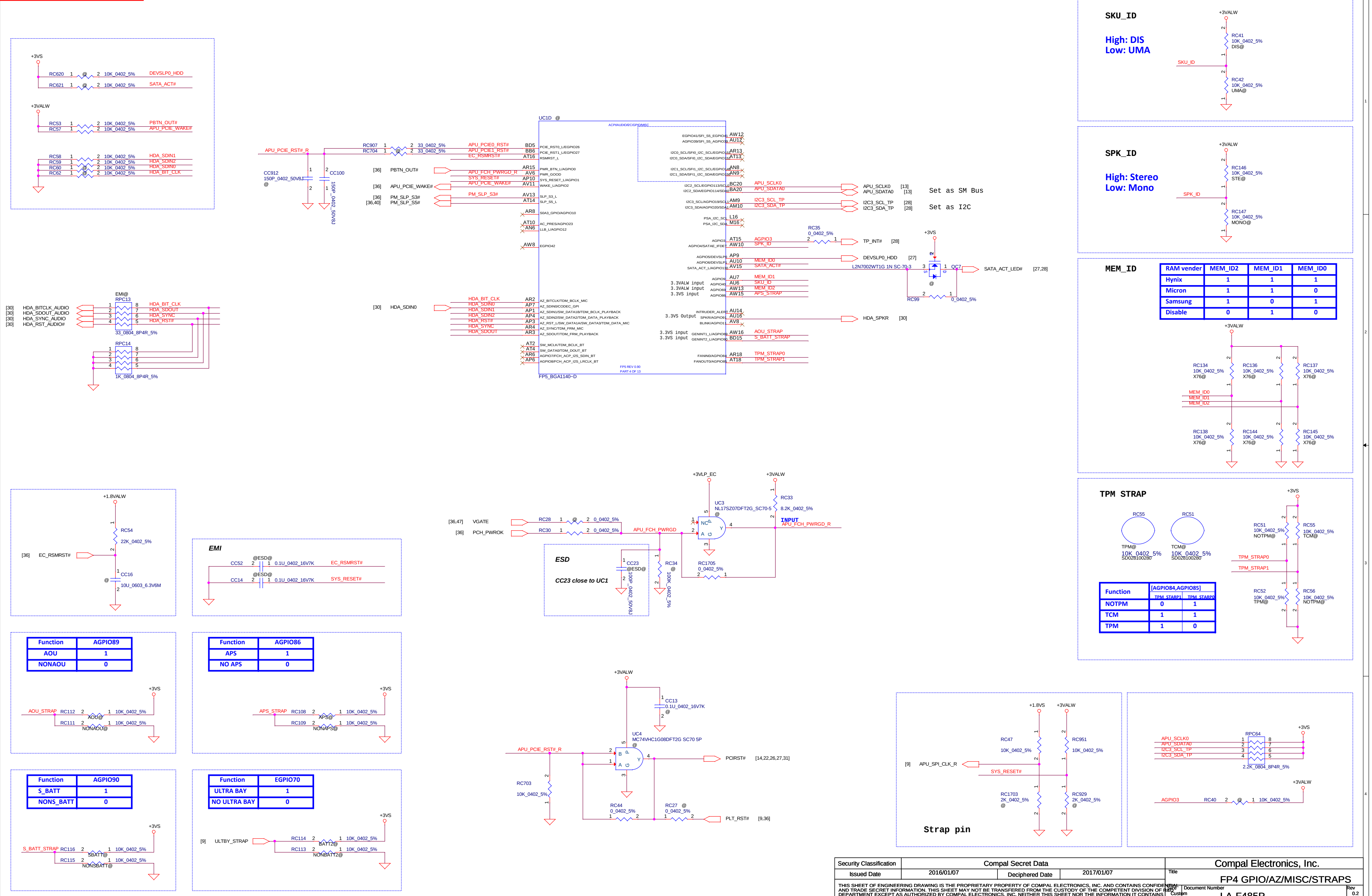
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/01/07	Title: FP5 PCIE/UMI
				Size: Custom; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 6 of 54

Main Func = CPU



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date 2017/01/07	Title: FP5 DISP/MISC/HDT
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Custom; Document Number: LA-F485P; Rev: 0.2
			Date: Monday, December 18, 2017; Sheet 7 of 54

Main Func = CPU



RAM vender	MEM_ID2	MEM_ID1	MEM_ID0
Hynix	1	1	1
Micron	1	1	0
Samsung	1	0	1
Disable	0	1	0

Function	[AGPIO84,AGPIO85]	
	TPM_STARP1	TPM_STARP0
NOTPM	0	1
TCM	1	1
TPM	1	0

Function	AGPIO89
AOU	1
NONAOU	0

Function	AGPIO86
APS	1
NO APS	0

Function	AGPIO90
S_BATT	1
NONS_BATT	0

Function	EGPIO70
ULTRA BAY	1
NO ULTRA BAY	0

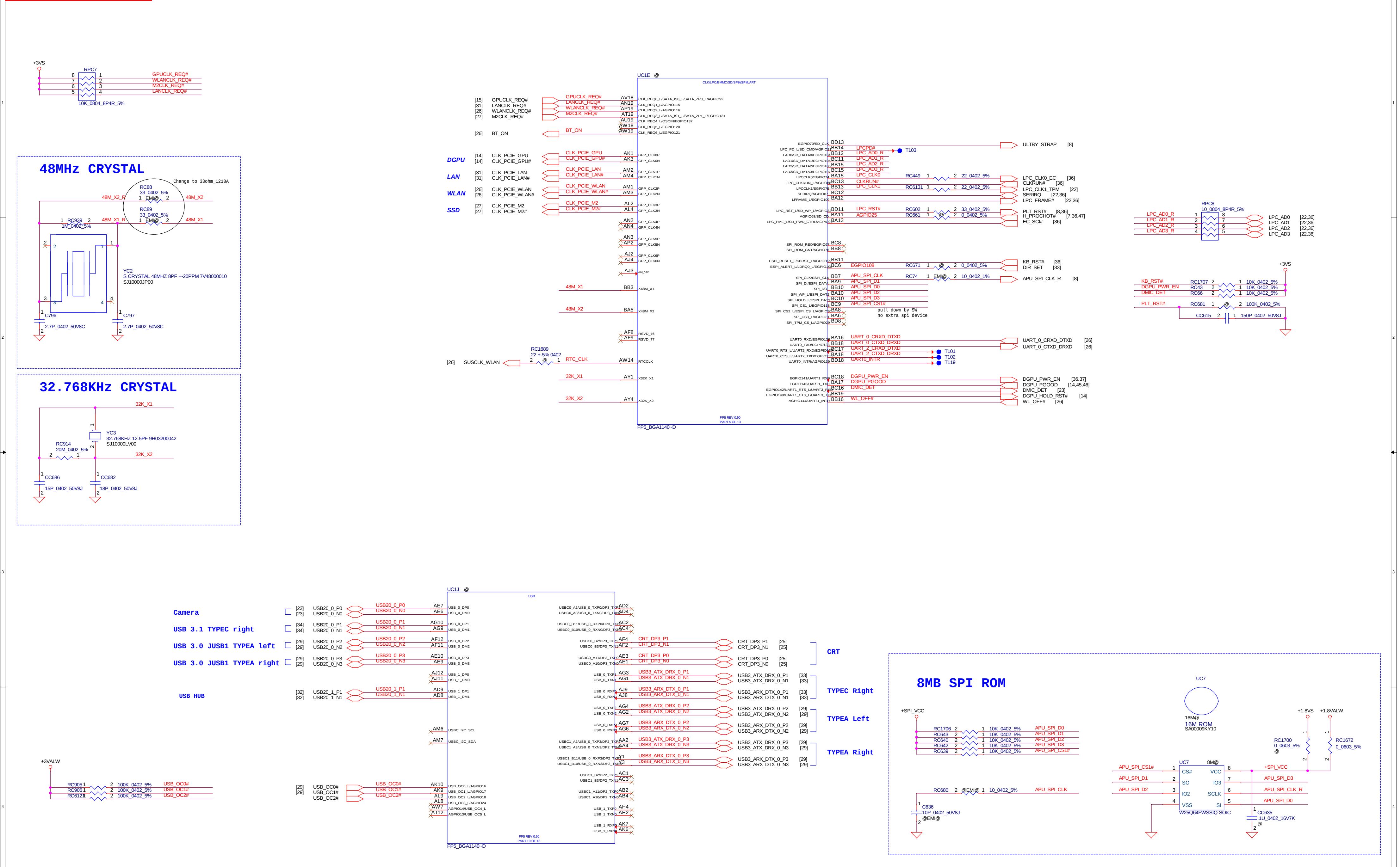
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: FP4 GPIO/AZ/MISC/STRAPS

Size: Custom | Document Number: LA-F485P | Rev: 0.2

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/01/07

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

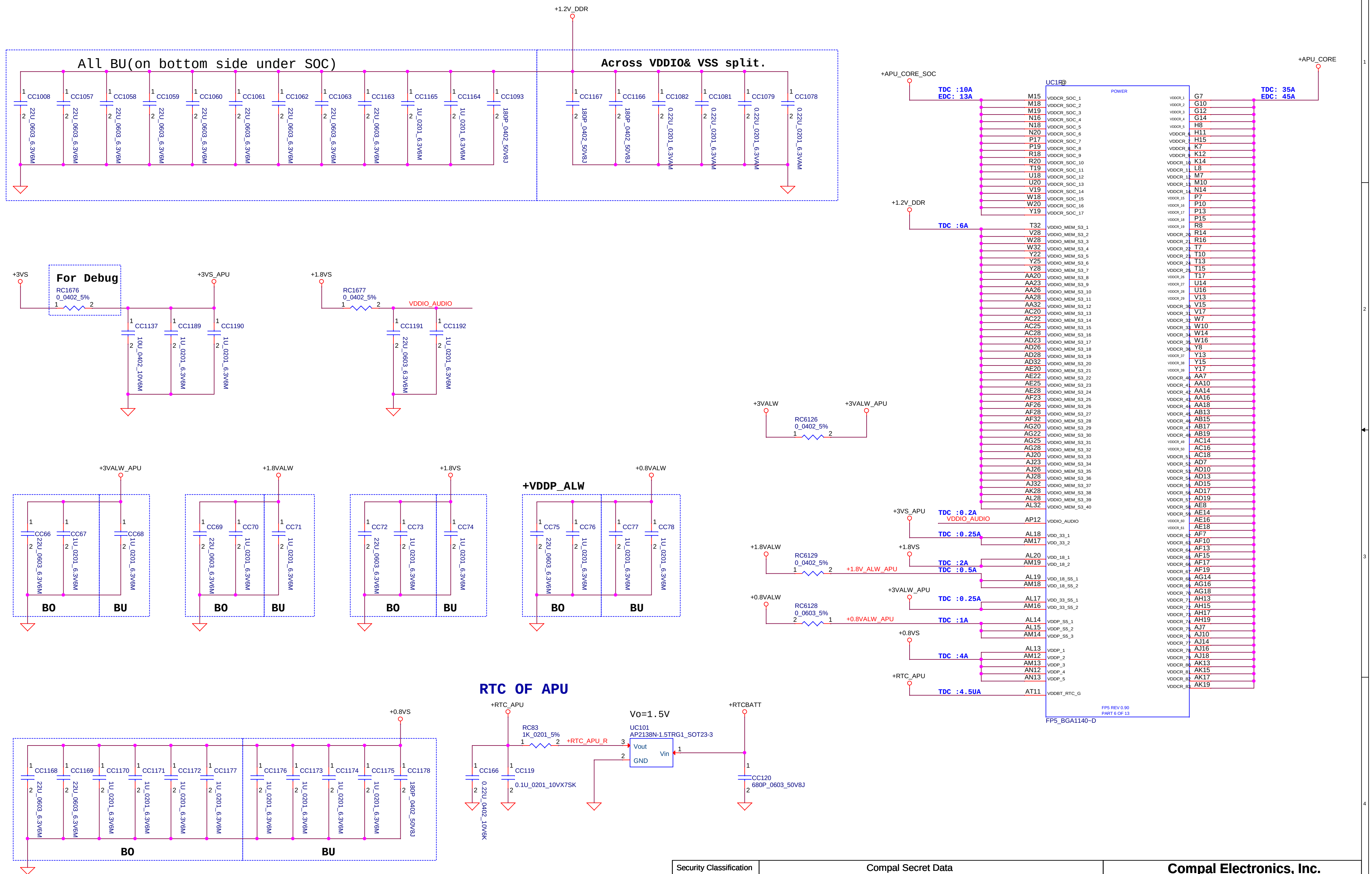
Compal Electronics, Inc.

Title: FP5 SATA/CLK/USB/SPI

Size: Custom | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017 | Sheet 9 of 54

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

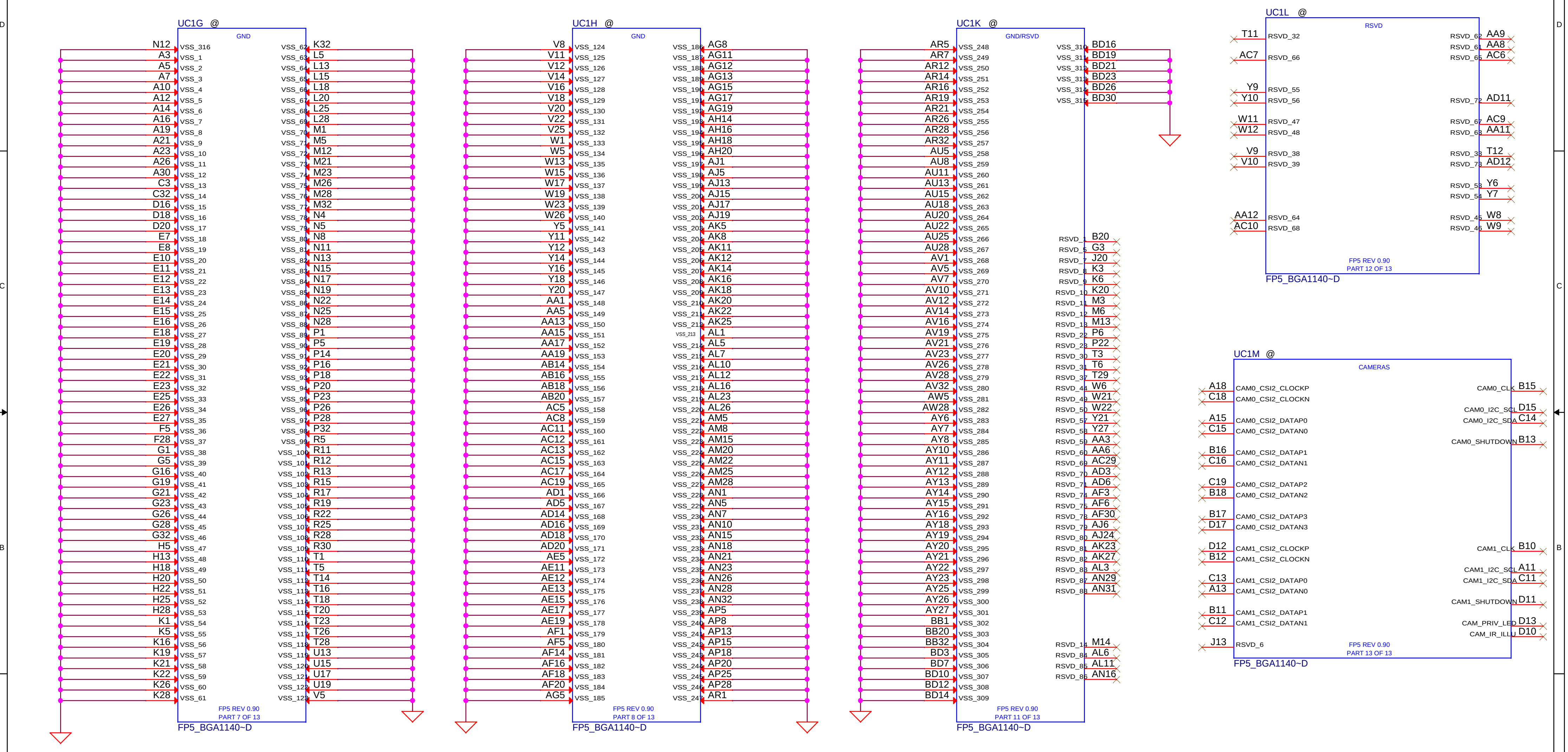
Compal Electronics, Inc.

Title: FP4 PWR

Size: Custom | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017 | Sheet 10 of 54

Main Func = CPU



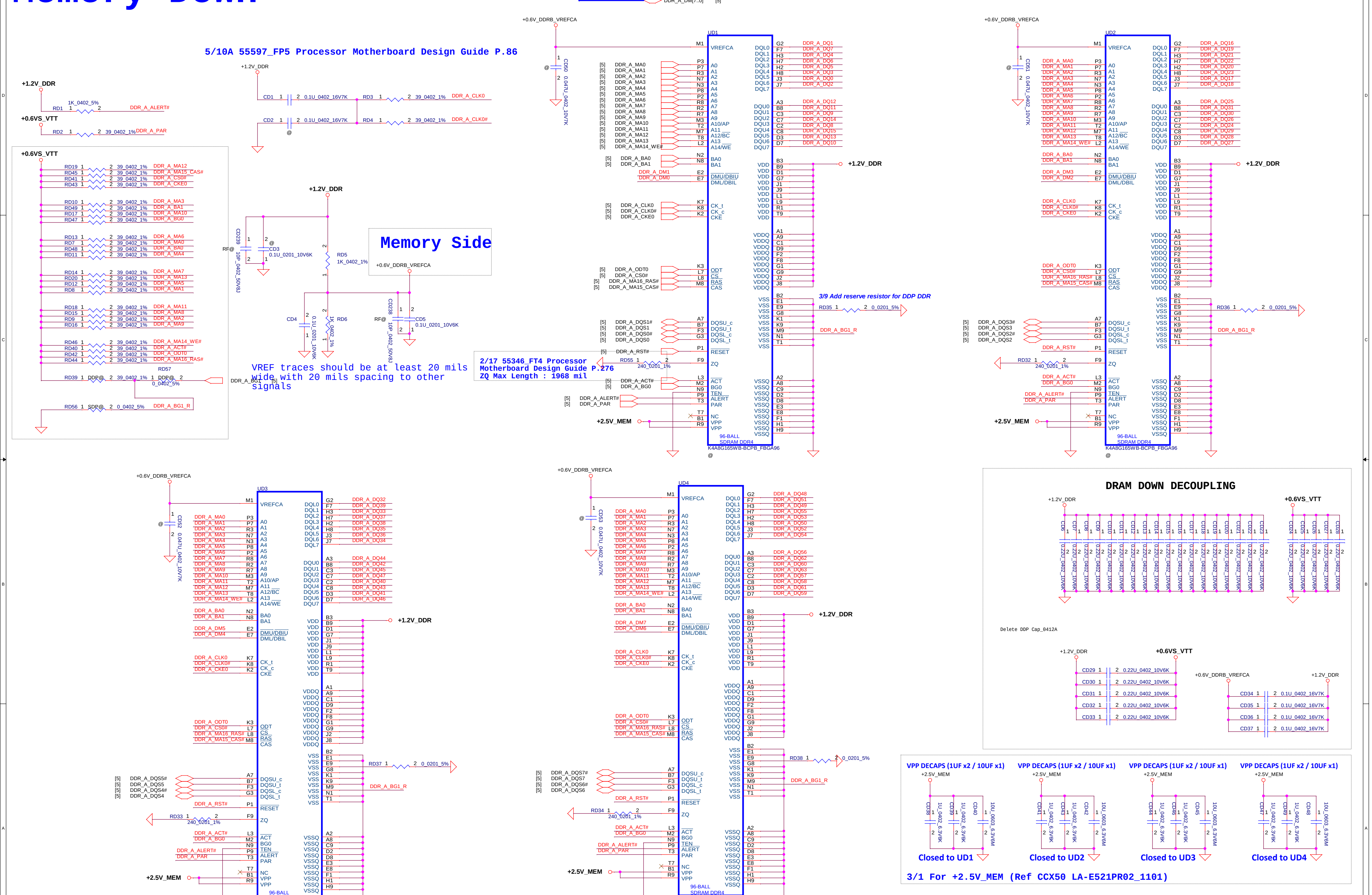
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/01/07	Title: FP5 GND

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size	Document Number	Rev
Custom	LA-F485P	0.2

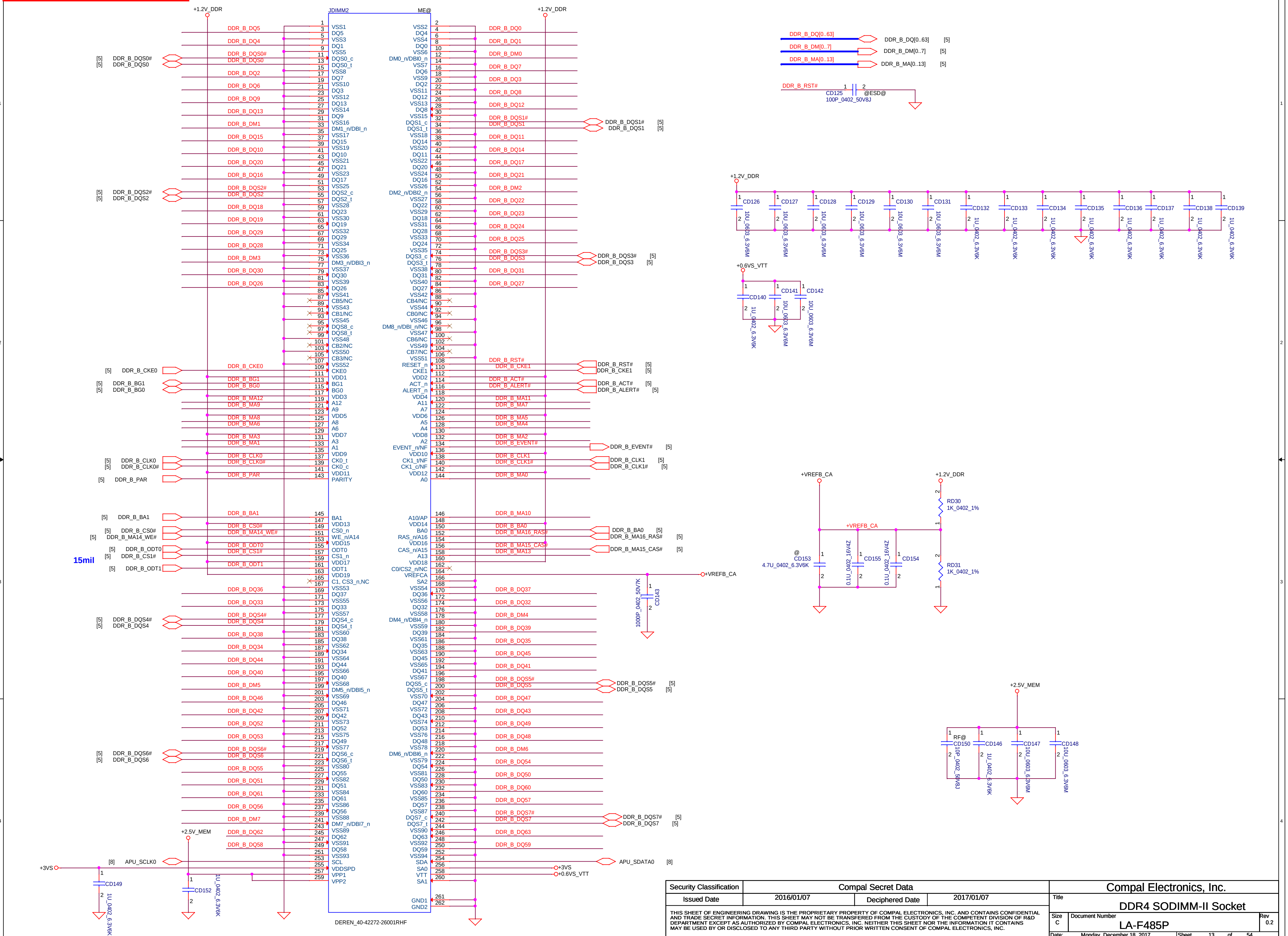
Date: Monday, December 18, 2017 | Sheet 11 of 54

Memory Down



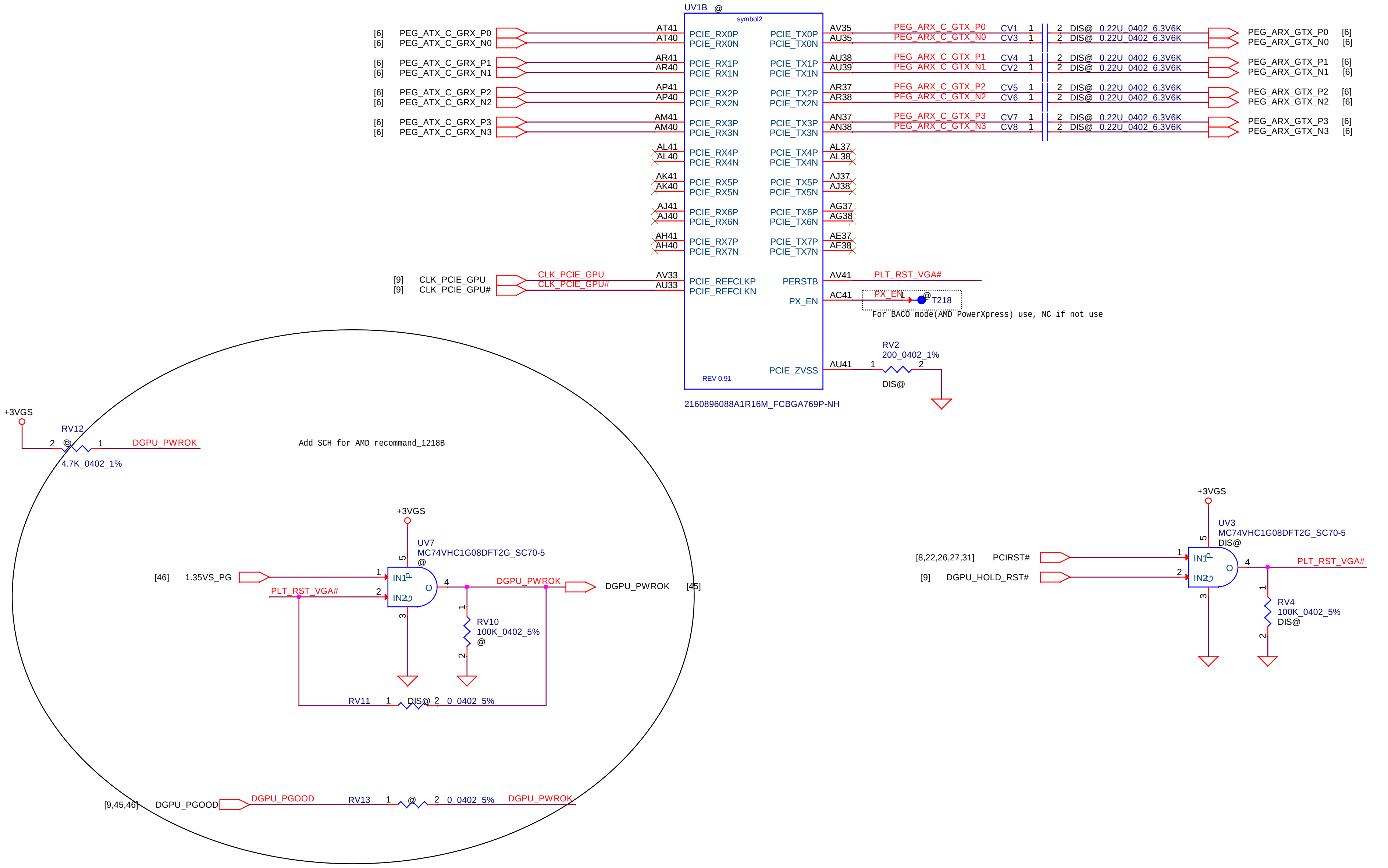
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: DDR4_CHA SO-DIMM
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-F485P / Rev 0.2
				Date: Monday, December 18, 2017 / Sheet 12 of 54

Main Func = DIMM2



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title: DDR4 SODIMM-II Socket
				Size: C; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 13 of 54

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



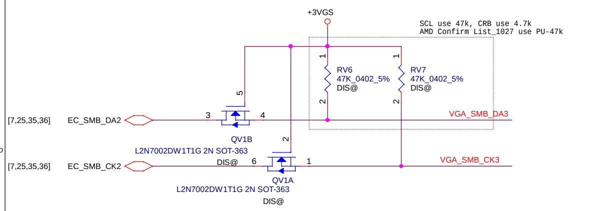
Security Classification	Compal Secret Data		
Issued Date	2017/04/18	Deciphered Date	2019/04/18

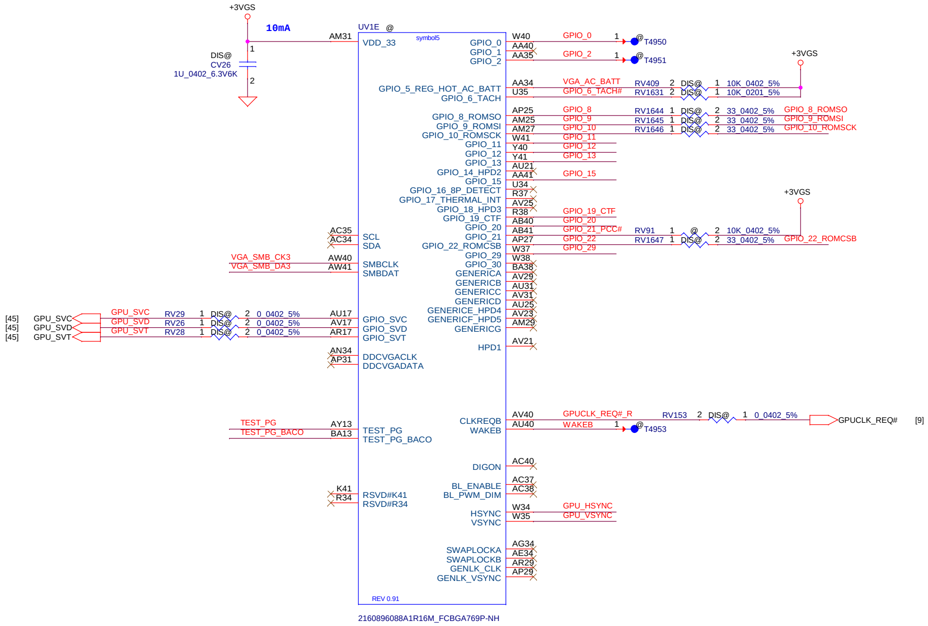
Compal Electronics, Inc.

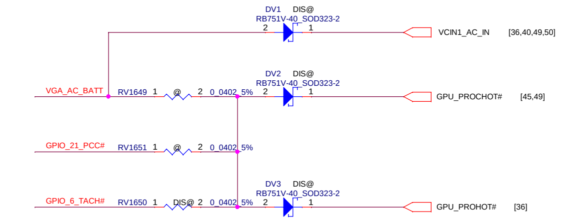
Title: R17M-P1-50/70_(1/9)_PCIE

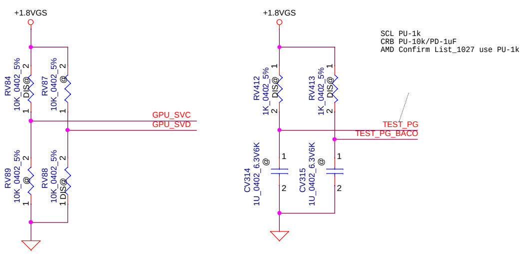
Size: Custom | Document Number: LA-F485P | Rev: 0.2

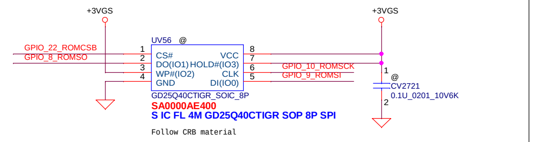
Date: Monday, December 18, 2017 | Sheet 14 of 54





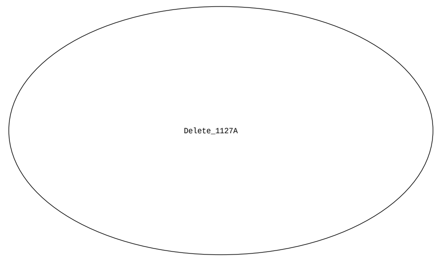


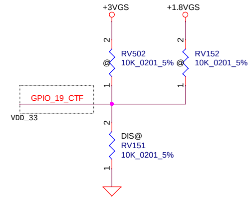




Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8





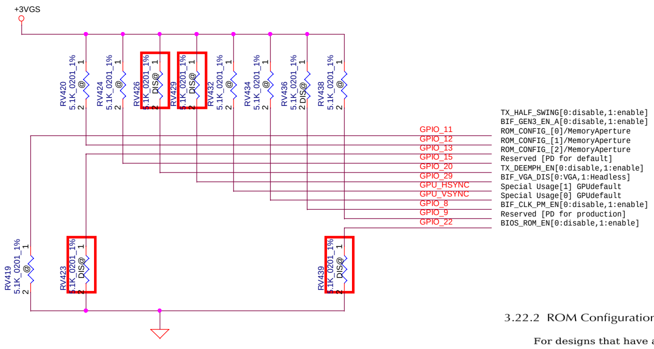


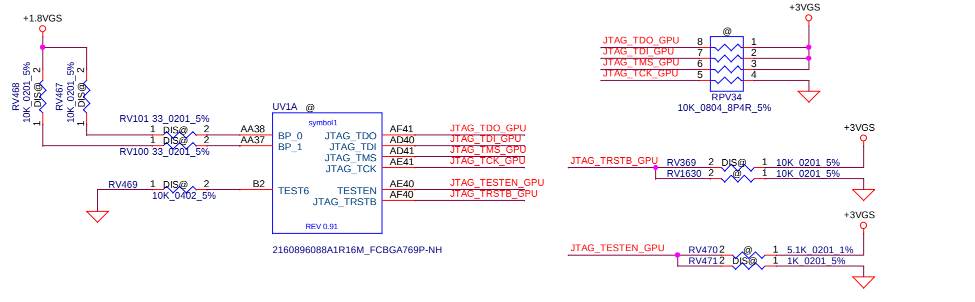
Table 3–27 Primary Memory Aperture Sizes Requested at PCI Configuration

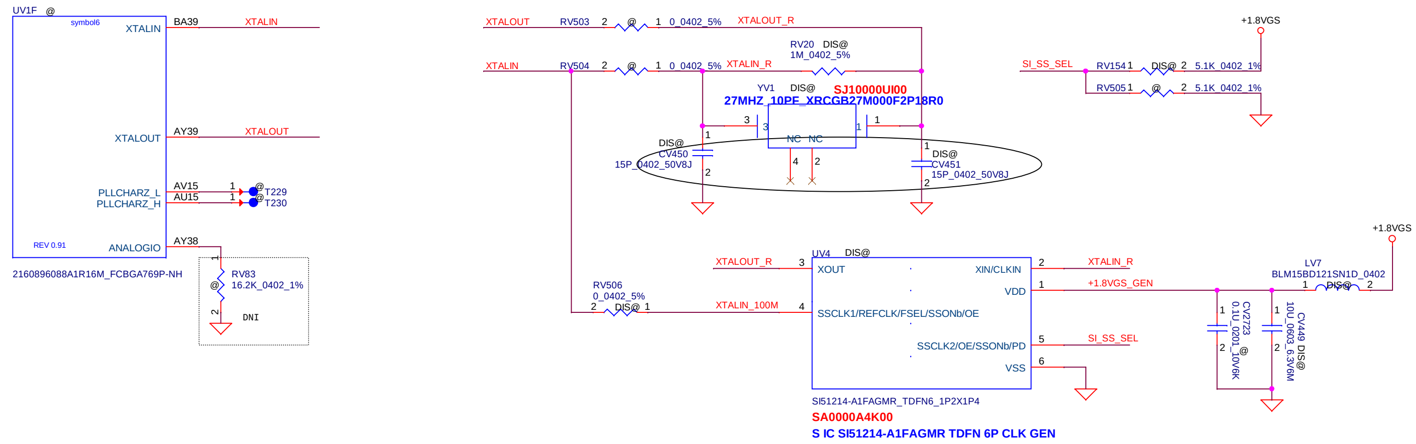
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

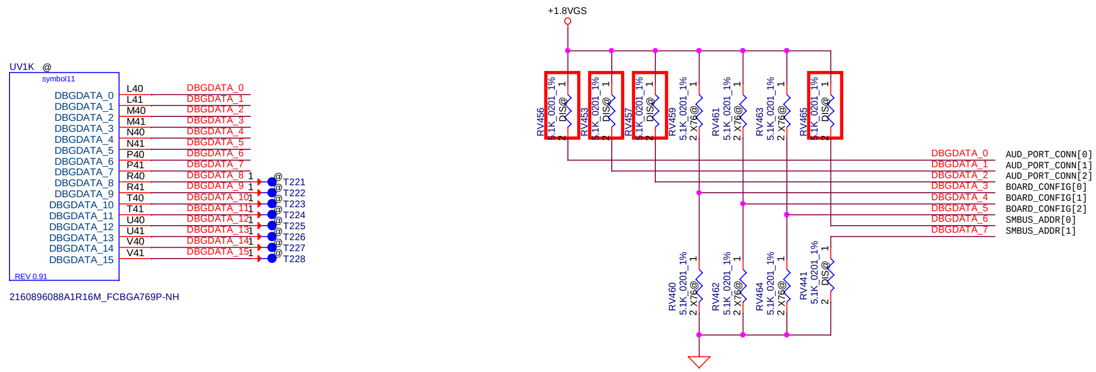
3.22.2 ROM Configurations

For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).







AUD_PORT_CONN[2:0]

111: No usable endpoints
110: One usable endpoint
101: Two usable endpoints
100: Three usable endpoints
011: Four usable endpoints
010: Five usable endpoints
001: Six usable endpoints
000: All endpoints are usable

BOARD_CONFIG[2:0]

000:SAM 256Mx32
001:HYN 256Mx32
010:MIC 256Mx32
011:
100:
101:
110:
111:

DBGDATA_[7:6]

00: 0×40
01: 0×41
10: 0×42
11: 0×43

MLPS Memory ID setting:

BOARD_CONFIG[2:0]		Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor P/N	SMT quantity
ID	[2:0]	ex: Samsung-GDDR5	64M x 32 4PCS,		1GB		4 pcs
0	000	Samsung-GDDR5	256M*32 2PCS, 1 RANK		2GB	K4G80325FB-HC28	2 pcs
1	001	Hynix-GDDR5	256M*32 2PCS, 1 RANK		2GB	H5GC8H24MJR-R0C	2 pcs
2	010	Micron-GDDR5	256M*32 2PCS, 1 RANK		2GB	MT51J256M32HF	2 pcs
3	011						
4	100						
5	101						
6	110						
7	111						

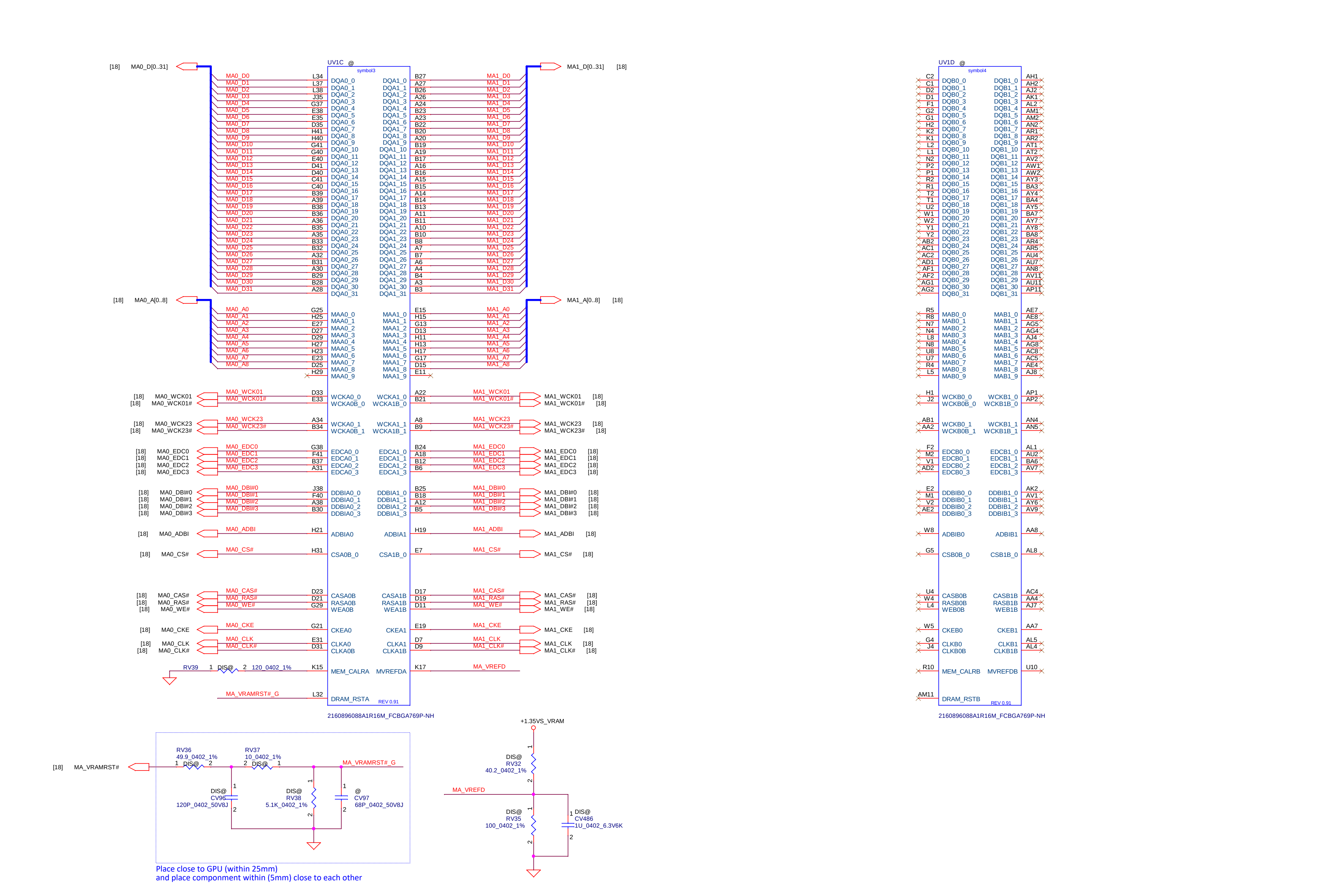
Security Classification	Compal Secret Data		
Issued Date	2017/04/18	Deciphered Date	2019/04/18

Compal Electronics, Inc.

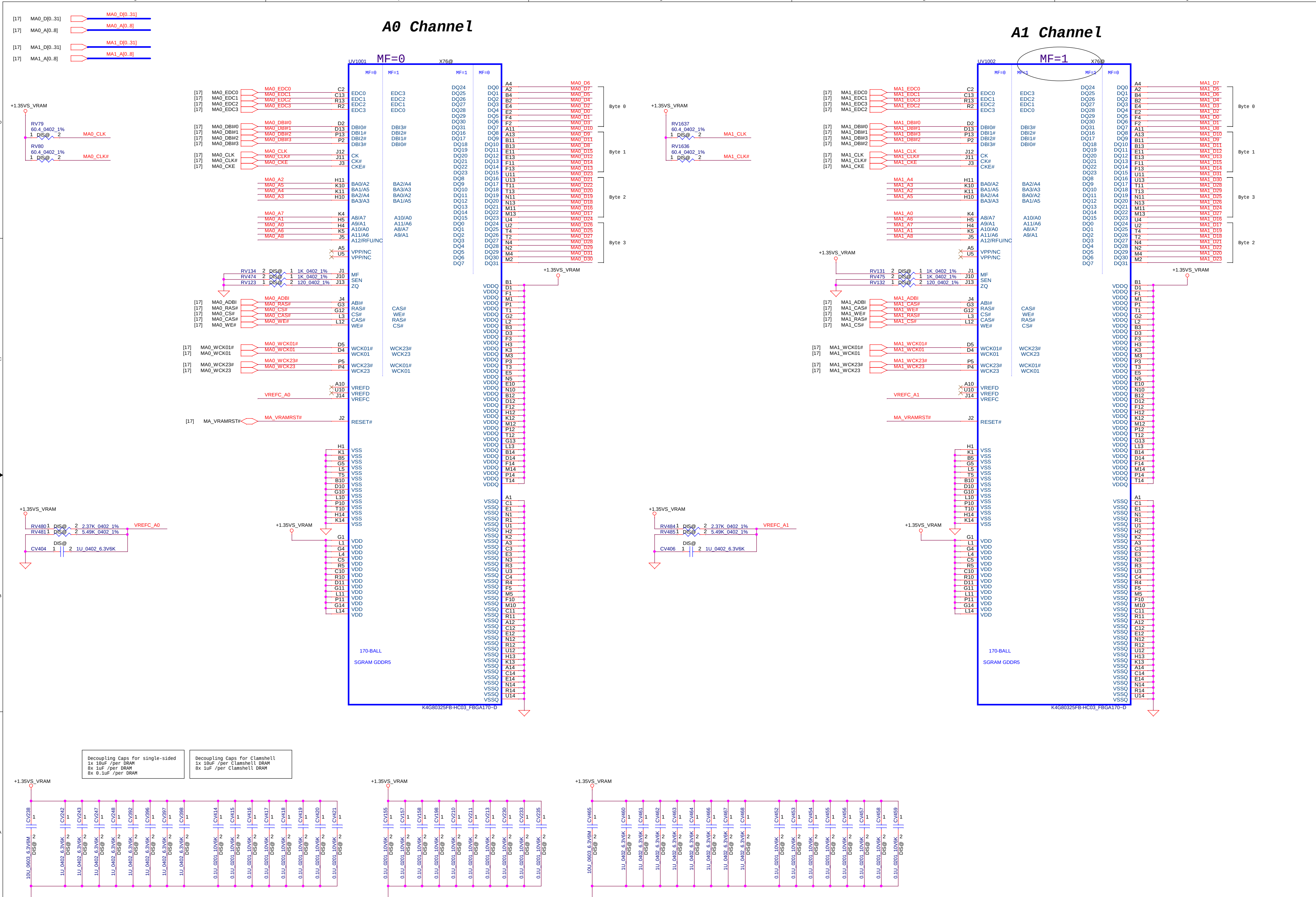
Title: R17M-P1-50/70_(3/9)_MSIC-2

Size: Custom | Document Number: LA-F485P | Rev 0.2

Date: Monday, December 18, 2017 | Sheet 16 of 54



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/04/18	Deciphered Date	2019/04/18	Title: R17M-P1-50/70_(4/9)_MEM
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 17 of 54

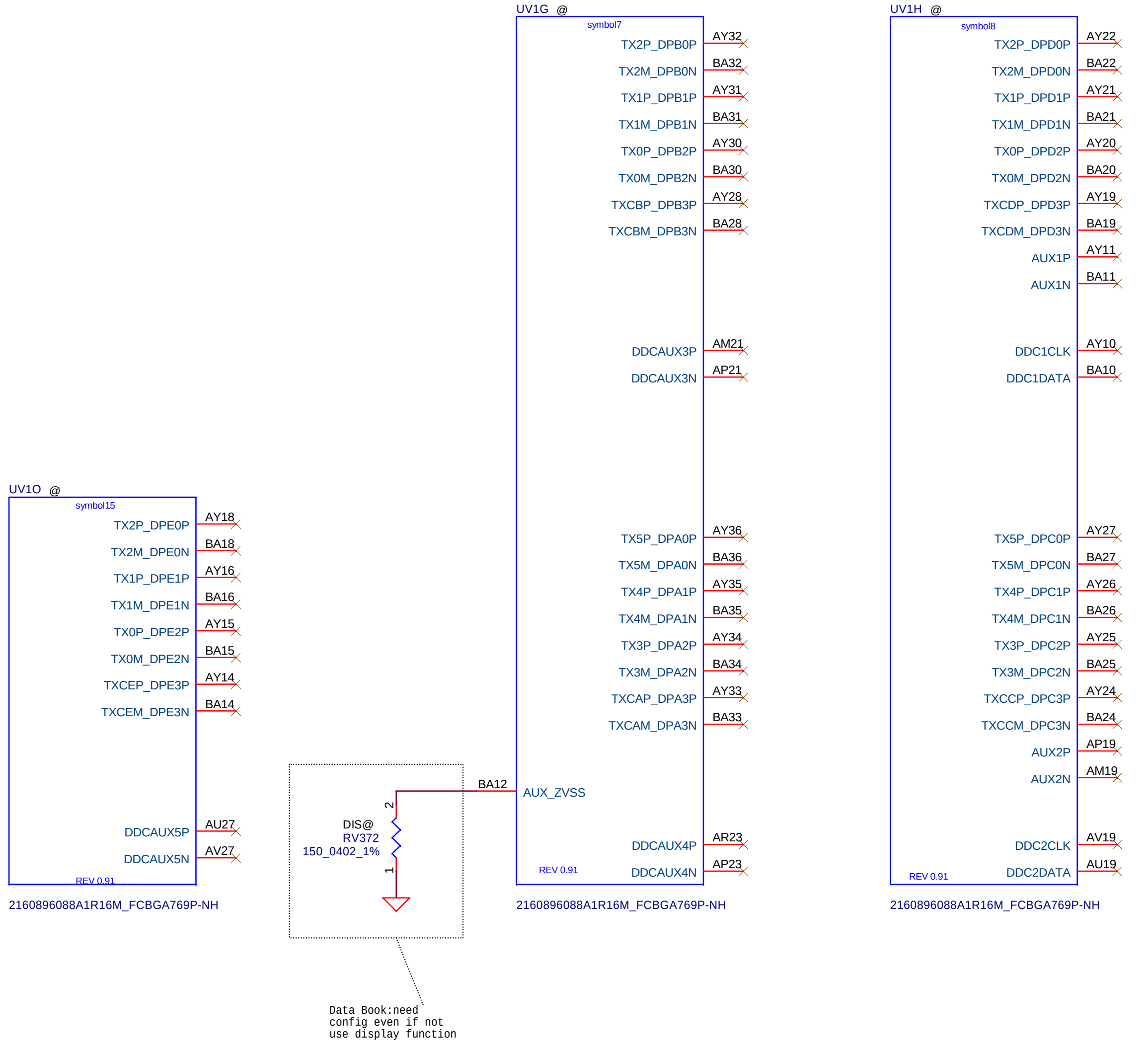


Security Classification	Compal Secret Data		
Issued Date	2017/04/18	Deciphered Date	2019/04/18

Compal Electronics, Inc.

Title: R17M-P1-50/70_(5/9)_CH A

Size: Custom | Document Number: LA-F485P | Rev: 0.2



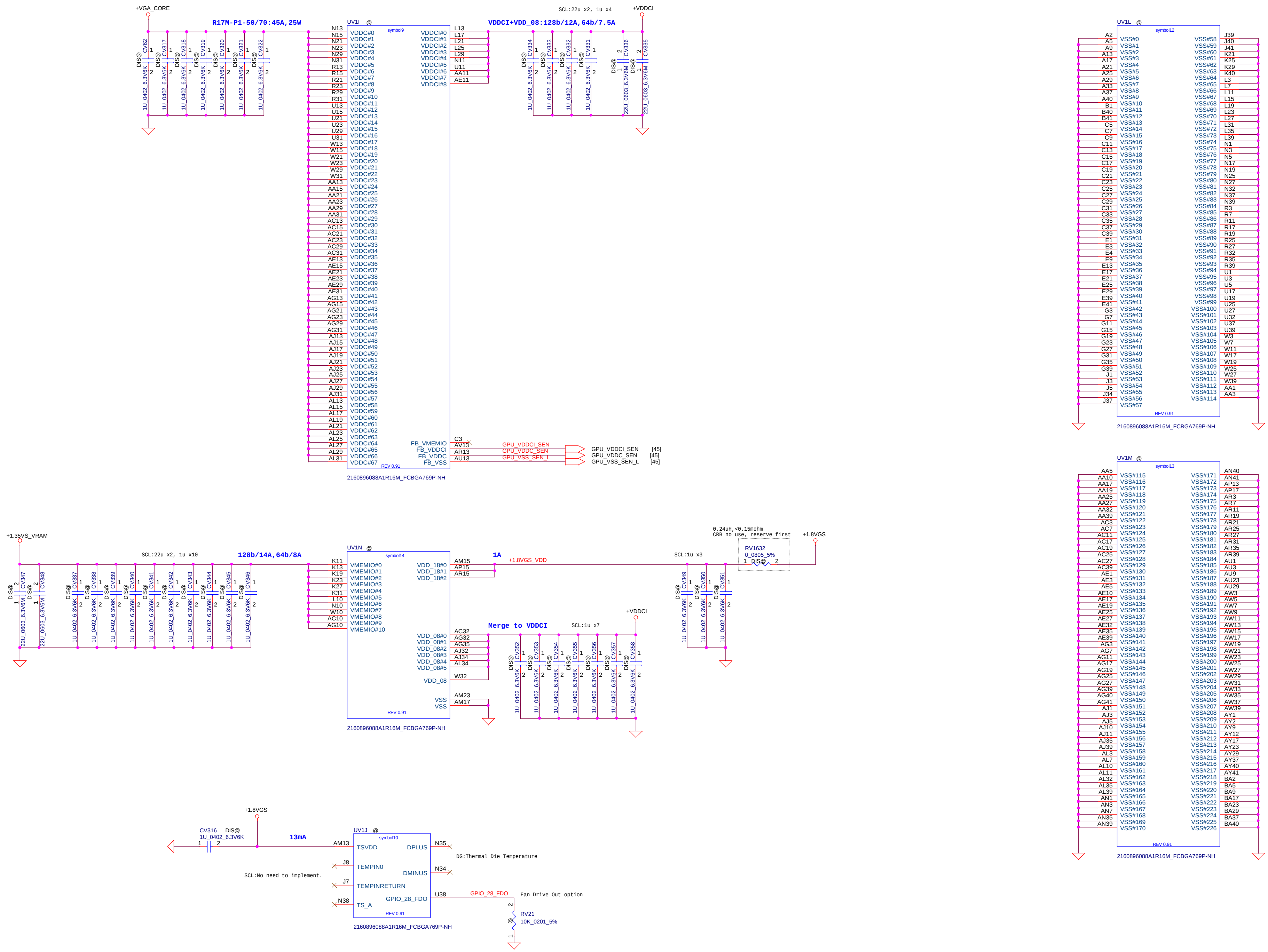
Security Classification	Compal Secret Data		
Issued Date	2017/04/18	Deciphered Date	2019/04/18

Compal Electronics, Inc.

Title: R17M-P1-50/70_(7/9)_DISPLAY

Size: Custom | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017



Security Classification	Compal Secret Data		
Issued Date	2017/04/18	Deciphered Date	2019/04/18

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: R17M-P1-50/70_(8/9)_PWR/GND

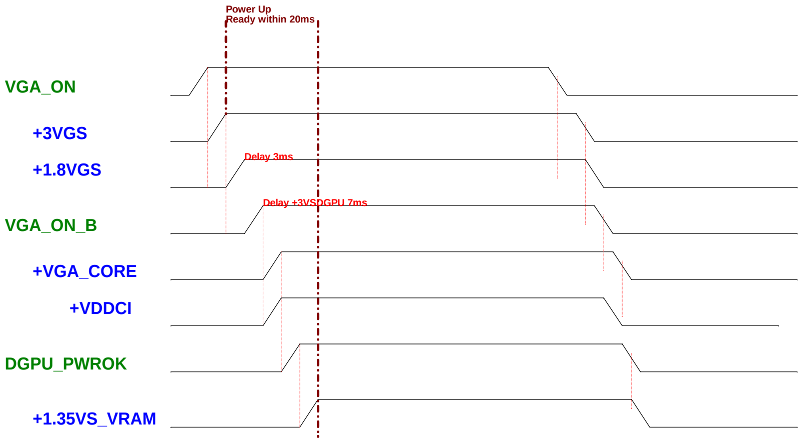
Size: Custom | Document Number: LA-F485P | Rev: 0.2

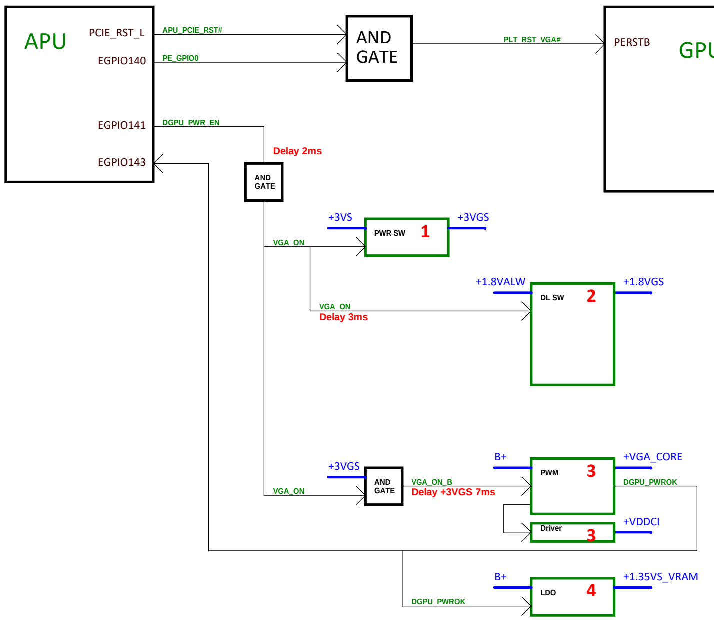
Date: Monday, December 18, 2017 | Sheet 20 of 54

5.3 Power-up/down Sequence

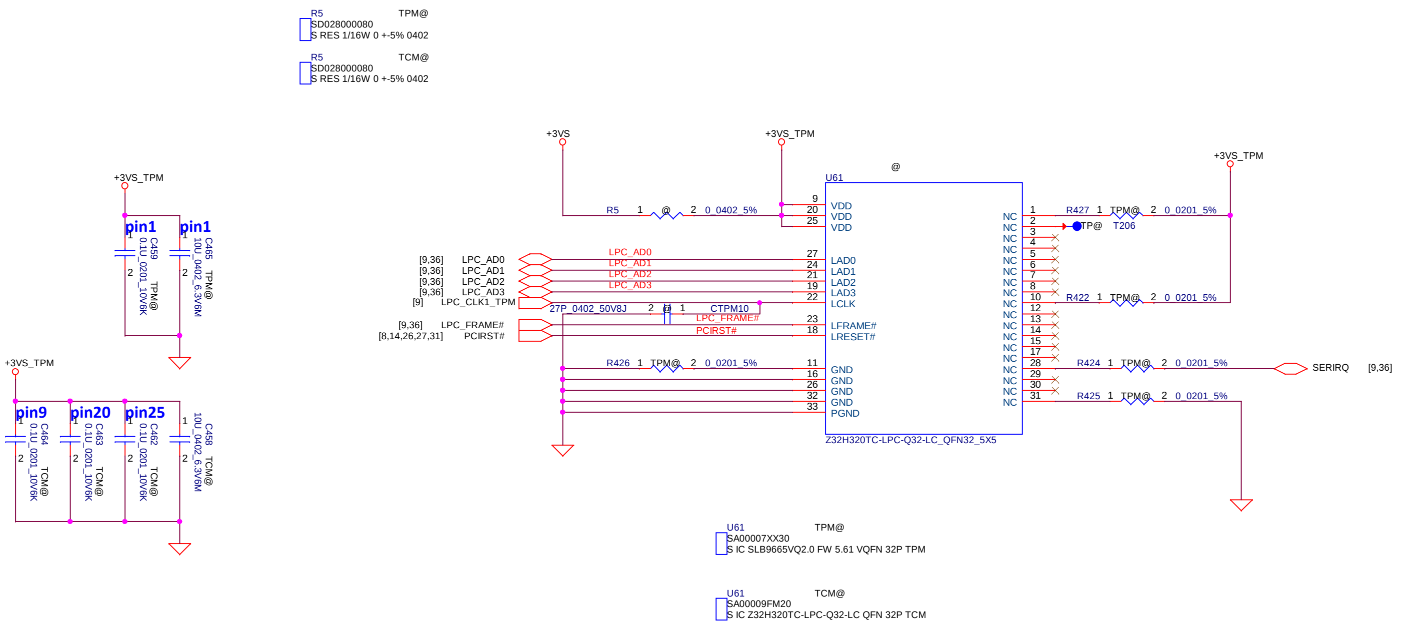
"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

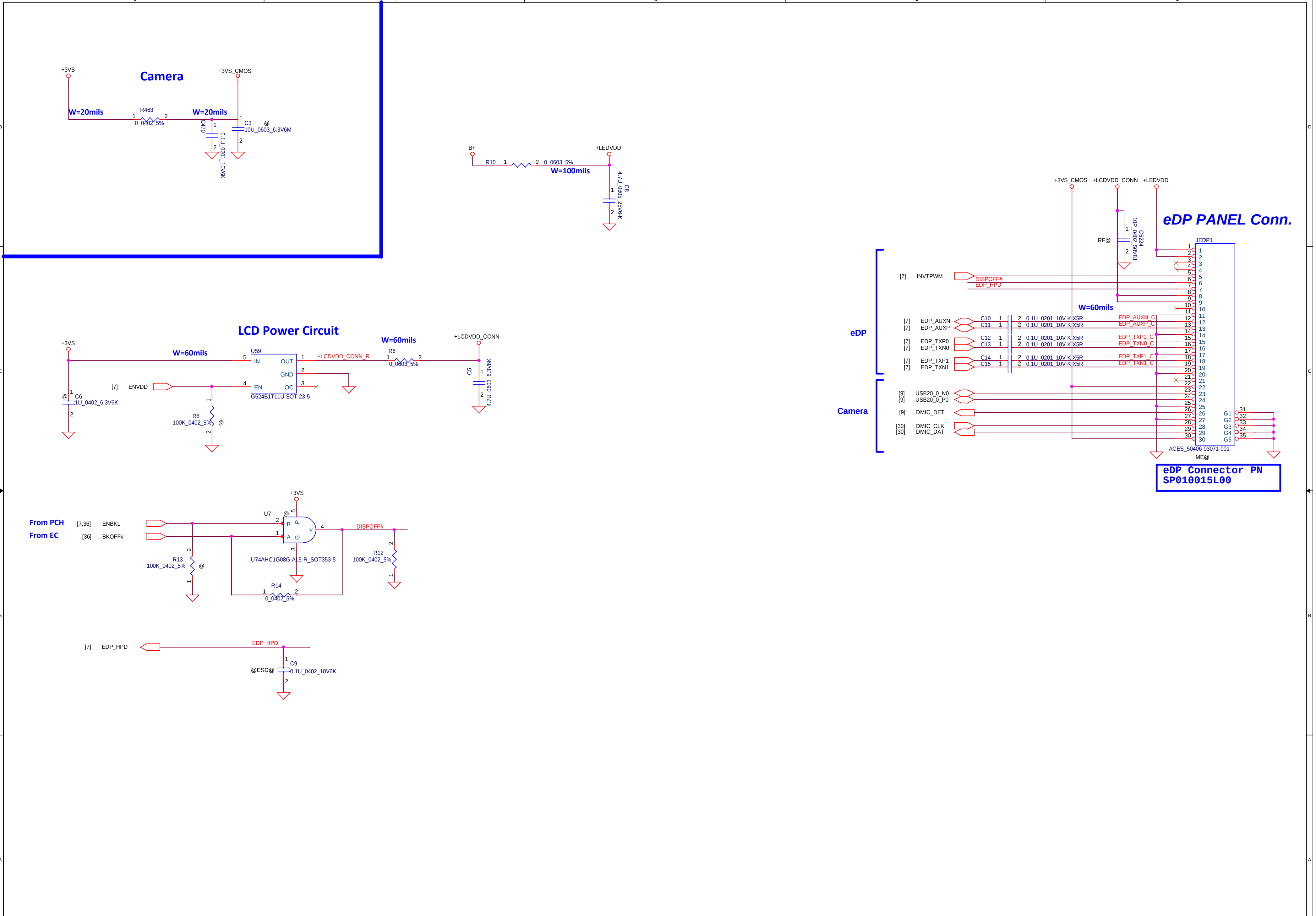




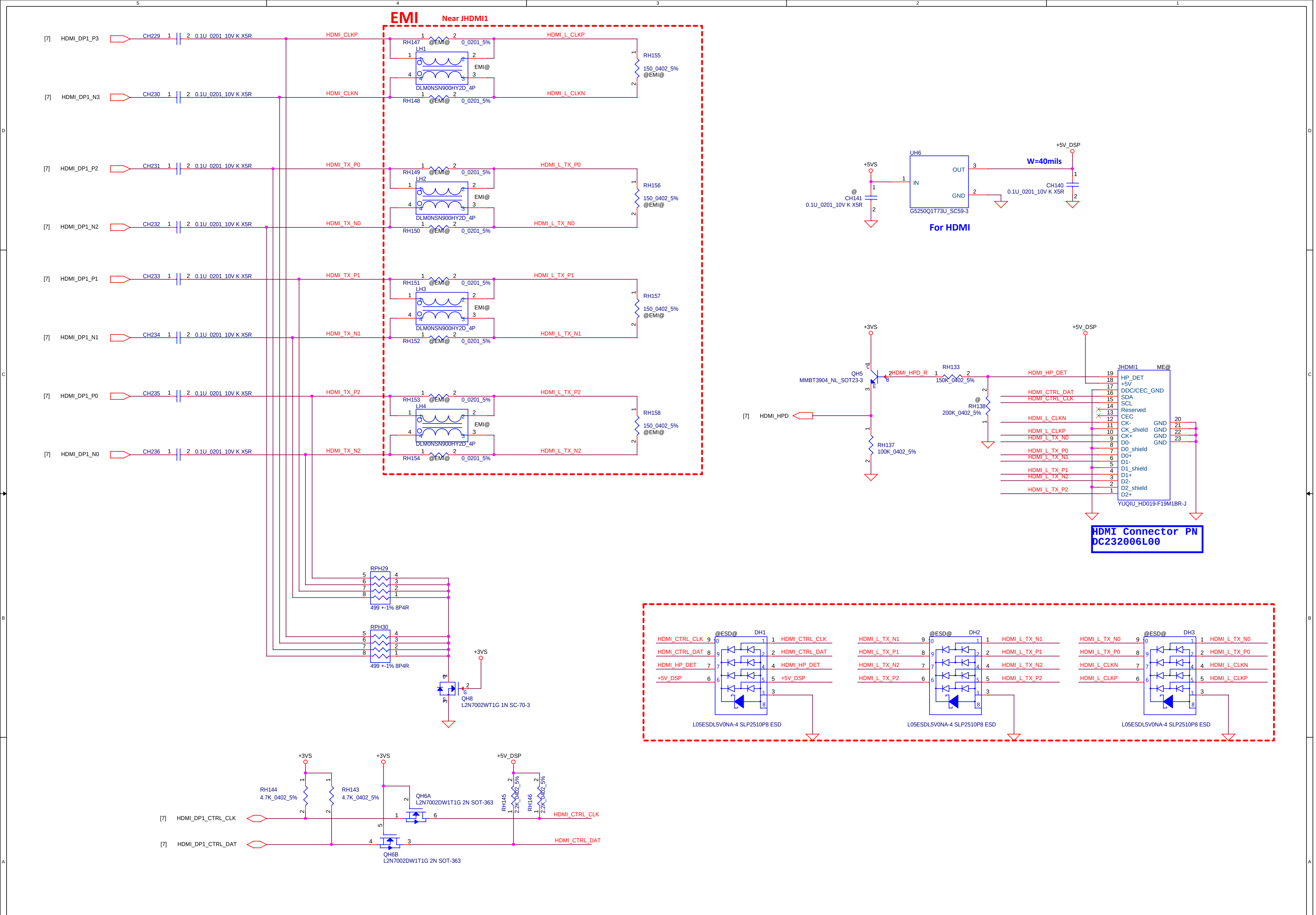
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/04/18	Deciphered Date	2019/04/18	Title: R17M-P1-50/70_(9/9)_NOTE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-F485P / Rev 0.2
				Date: Monday, December 18, 2017 / Sheet 21 of 54



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: TPM/TCM
				Size / Document Number: LA-F485P / Rev 0.2
				Date: Monday, December 18, 2017 / Sheet 22 of 54



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: eDP/CAMERA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: C; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 23 of 54

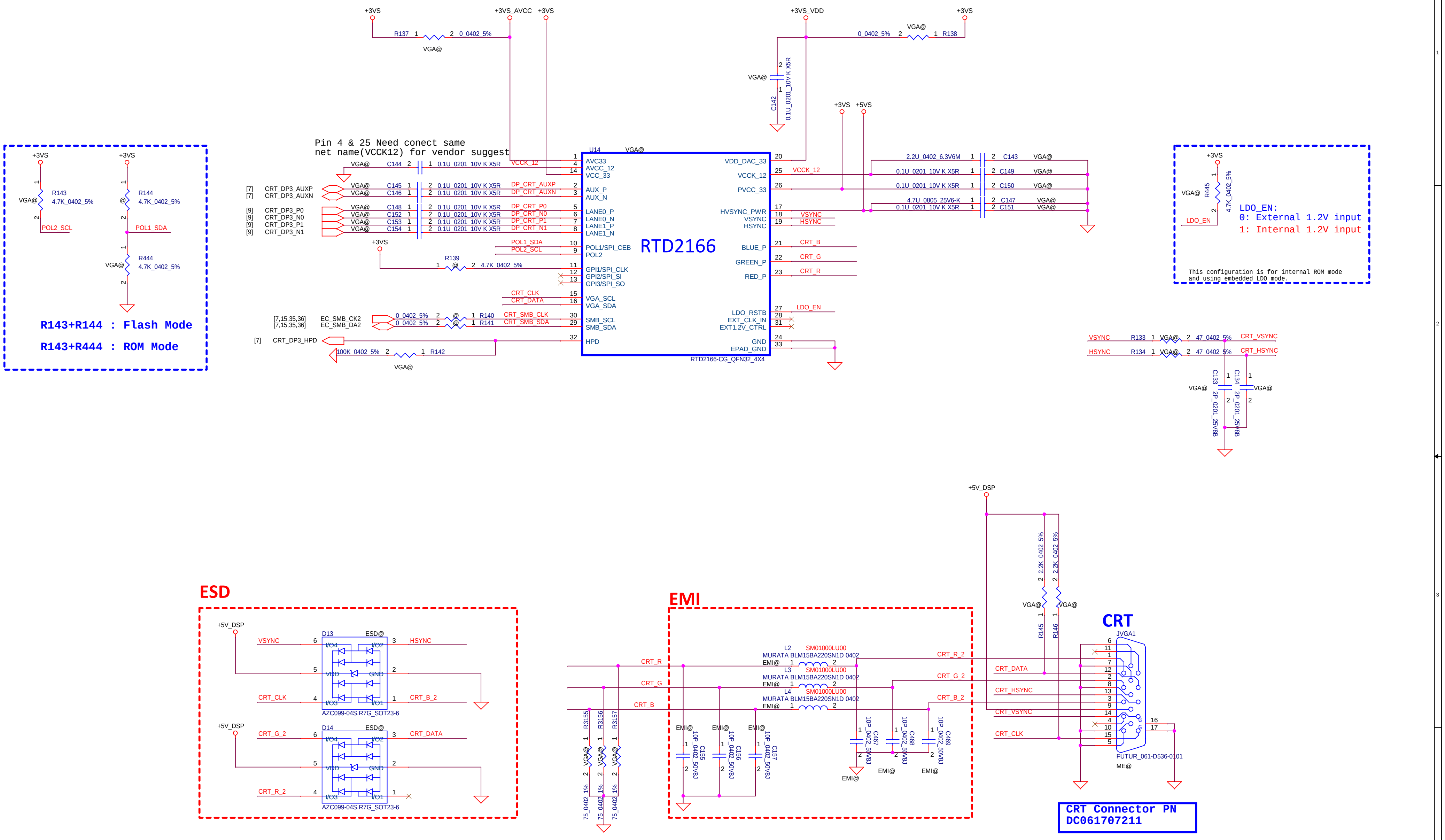


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: HDMI

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size	Document Number	Rev
C	LA-F485P	0.2

Date: Monday, December 18, 2017 Sheet 24 of 54



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

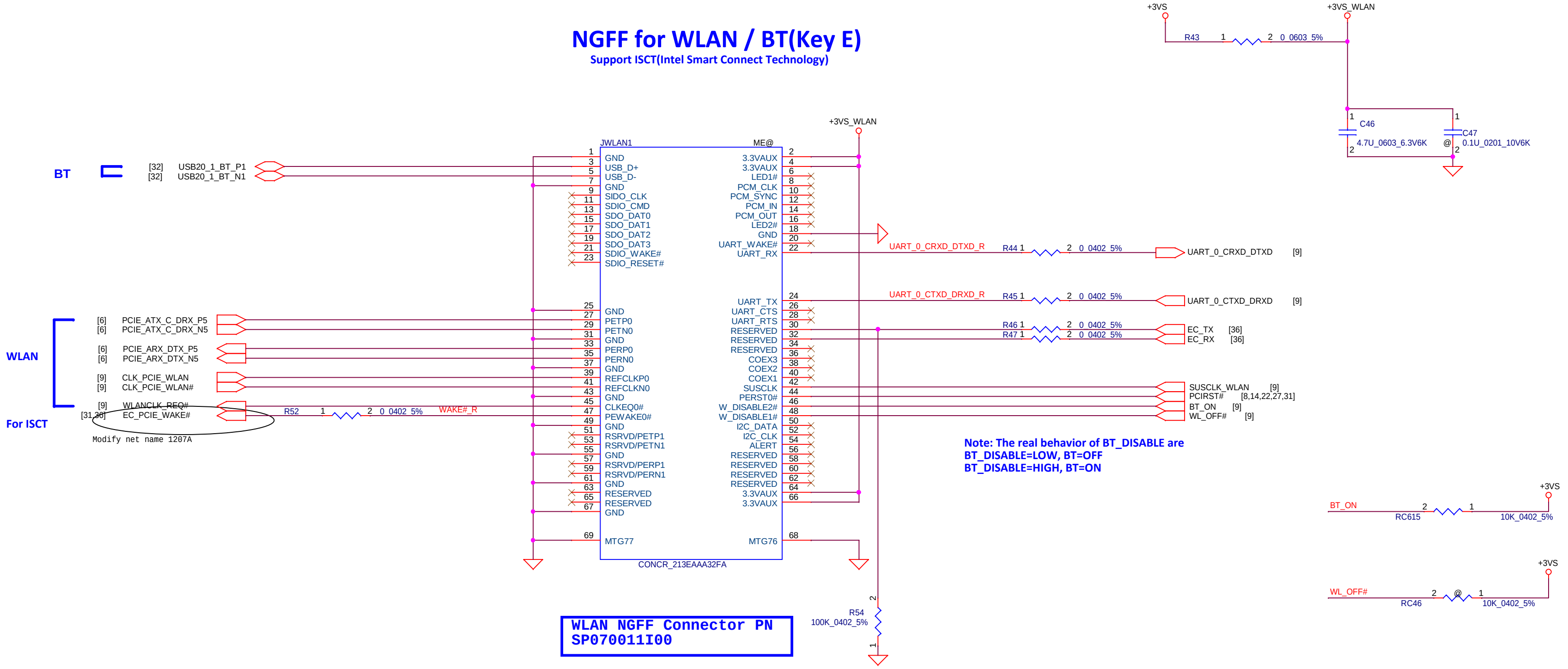
Title: **HDD Connector**

Size	Document Number	Rev
C	LA-F485P	0.2

Date: Monday, December 18, 2017 | Sheet 25 of 54

NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)



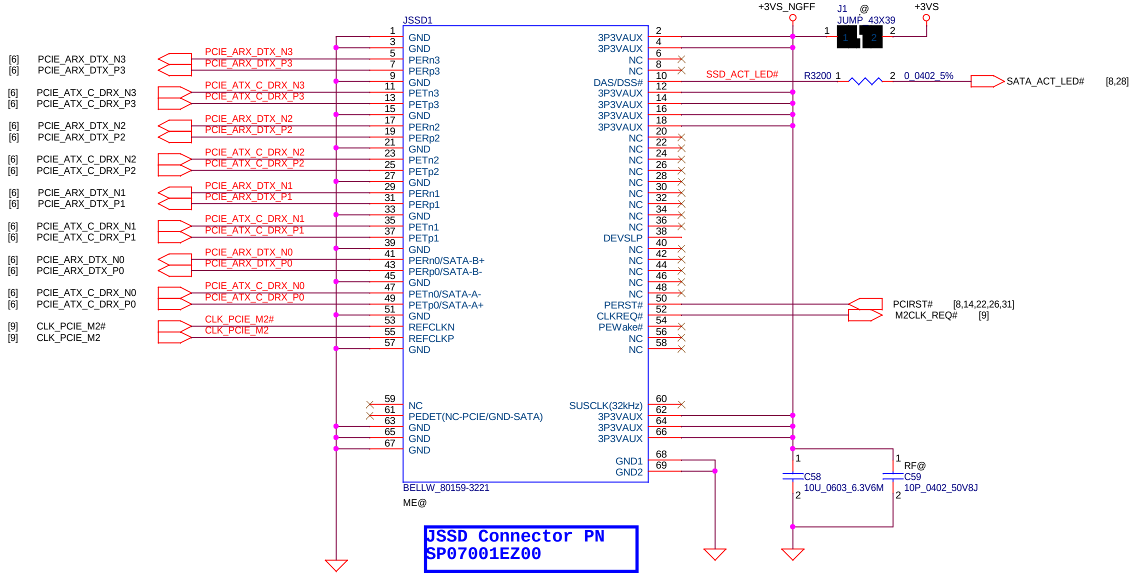
Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

Compal Electronics, Inc.

Title: *Mini-Card/NEW Card/SIM*

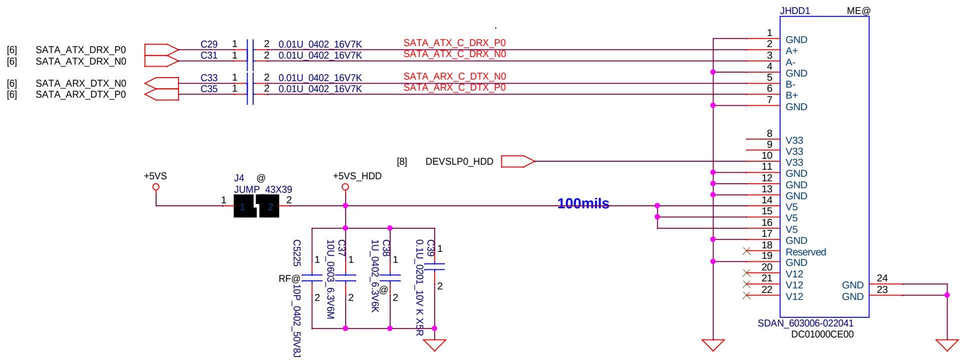
Size | Document Number: LA-F485P | Rev 0.2

M.2 mSATA Conn

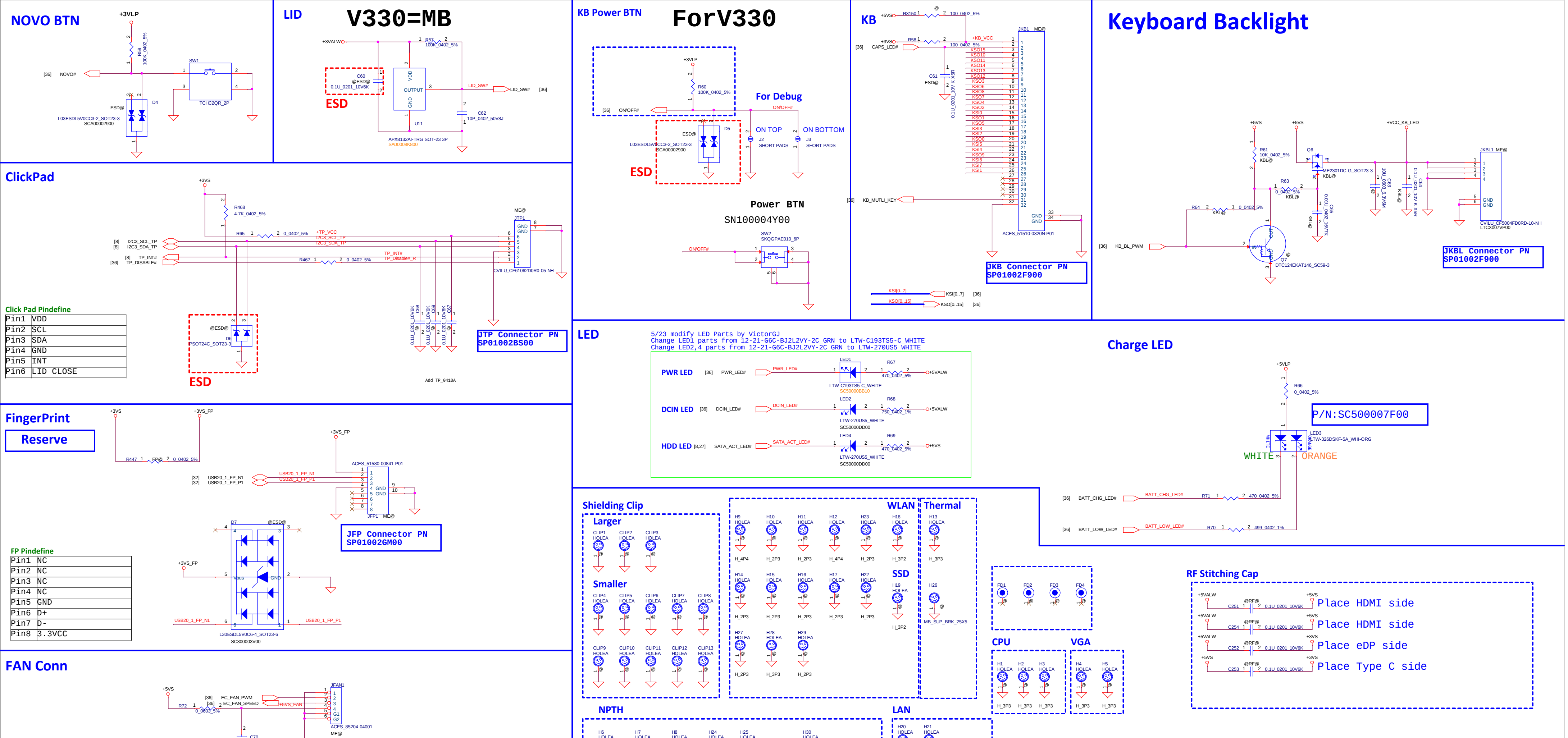


HDD

SATA HDD Conn.



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: M.2 SSD/HDD
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-F485P; Rev 0.2
				Date: Monday, December 18, 2017; Sheet 27 of 54



Click Pad Pindefine

Pin1	VDD
Pin2	SCL
Pin3	SDA
Pin4	GND
Pin5	INT
Pin6	LID CLOSE

FP Pindefine

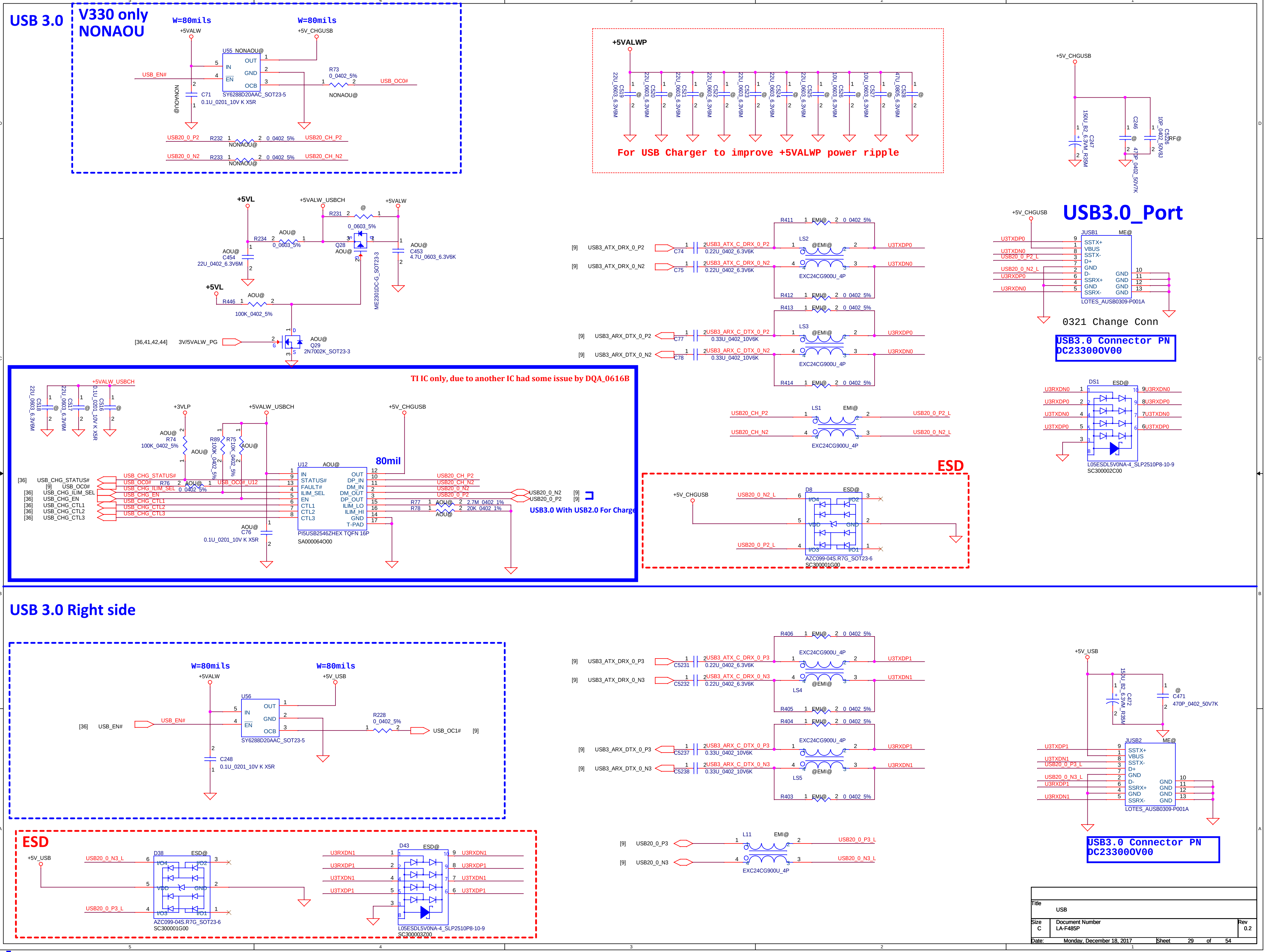
Pin1	NC
Pin2	NC
Pin3	NC
Pin4	NC
Pin5	GND
Pin6	D+
Pin7	D-
Pin8	3.3VCC

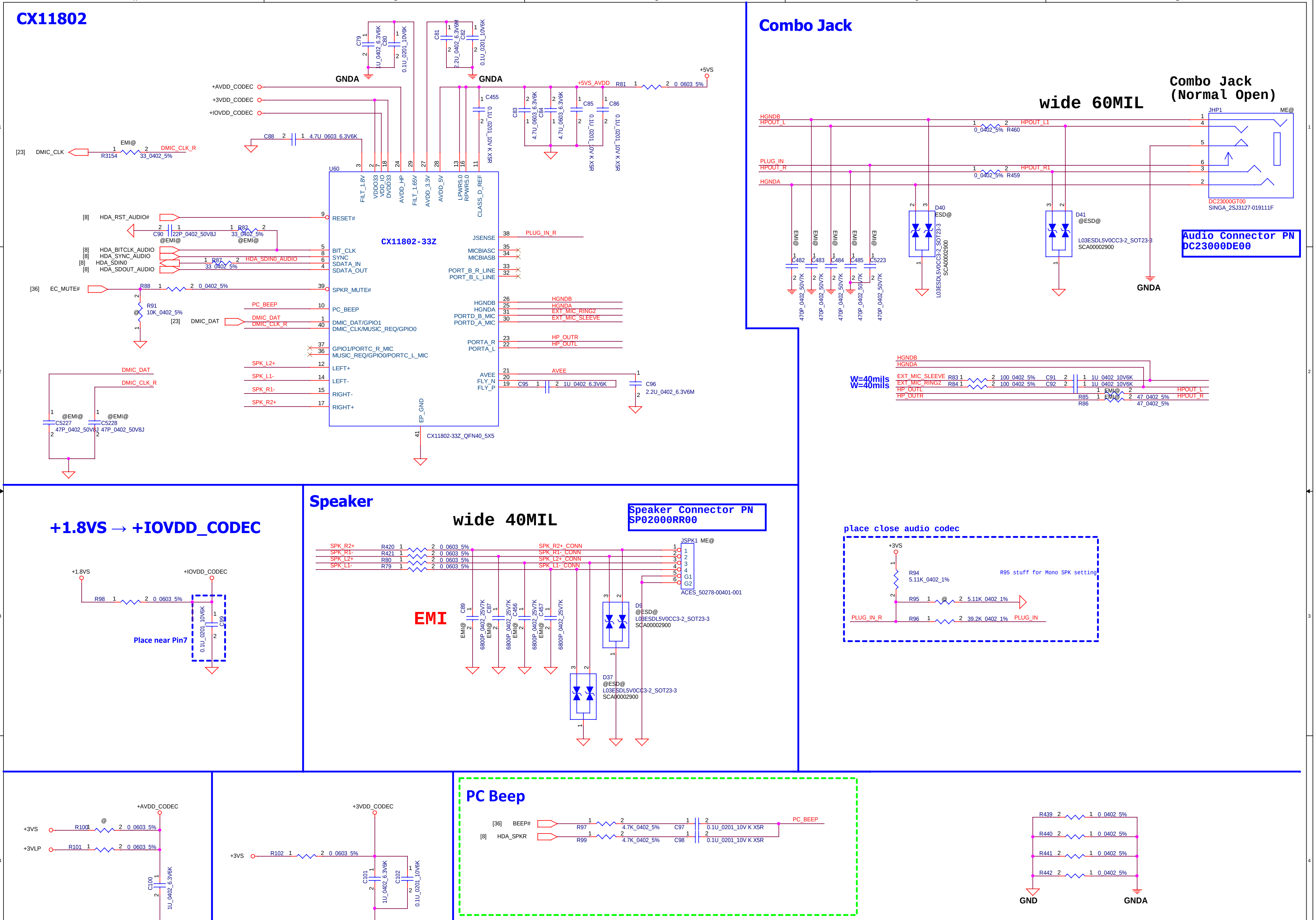
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: KBD/PWR/CR/LED/TP Conn.

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

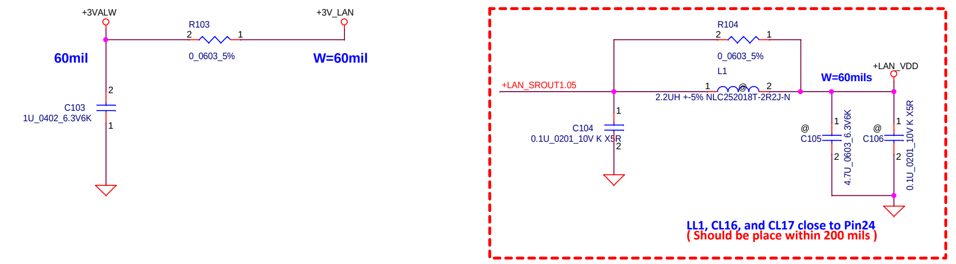
Size: Custom | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017 | Sheet 28 of 54


USB 3.0
V330 only
NONAOU
W=80mils
+5VALW
+5V_CHGUSB
U55_NONAOU@
SY6288D20AAC_SOT23-5
USB_EN#
USB_OC0#
R73
0_0402_5%
NONAOU@
C71
0.1U_0201_10V K X5R
USB20_0_P2
R232
USB20_CH_P2
USB20_0_N2
R233
USB20_CH_N2
+5VALWP
For USB Charger to improve +5VALWP power ripple
+5VL
+5VALW_USBCH
R231
0_0603_5%
R234
Q28
ME2301DC-G_SOT23-3
C454
22U_0402_6.3V6M
C453
4.7U_0603_6.3V6K
R446
100K_0402_5%
3V/5VALW_PG
Q29
2N7002K_SOT23-3
TI IC only, due to another IC had some issue by DQA_0616B
+3VLP
U12
PI5USB2546ZHEX TQFN 16P
SA000064O00
80mil
USB_CHG_STATUS#
USB_CHG_ILIM_SEL
USB_CHG_EN
USB_CHG_CTL1
USB_CHG_CTL2
USB_CHG_CTL3
USB3.0 With USB2.0 For Charger
USB3.0_Port
JUSB1
LOTES_AUSB0309-P001A
0321 Change Conn
USB3.0 Connector PN
DC233000V00
DS1
L05ESDL5V0NA-4_SLP2510P8-10-9
SC300002C00
ESD
D8
AZC099-04S.R7G_SOT23-6
SC300001G00
EXC24CG900U_4P
U3TXDP0
U3TXDN0
U3RXDP0
U3RXDN0
USB 3.0 Right side
W=80mils
+5V_USB
U56
SY6288D20AAC_SOT23-5
R228
0_0402_5%
USB_OC1#
C248
0.1U_0201_10V K X5R
JUSB2
LOTES_AUSB0309-P001A
USB3.0 Connector PN
DC233000V00
ESD
D38
AZC099-04S.R7G_SOT23-6
SC300001G00
D43
L05ESDL5V0NA-4_SLP2510P8-10-9
SC300003Z00
U3TXDP1
U3TXDN1
U3RXDP1
U3RXDN1
L11
USB20_0_P3
USB20_0_N3
Title
USB
Size
C
Document Number
LA-F485P
Rev
0.2
Date: Monday, December 18, 2017
Sheet 29 of 54

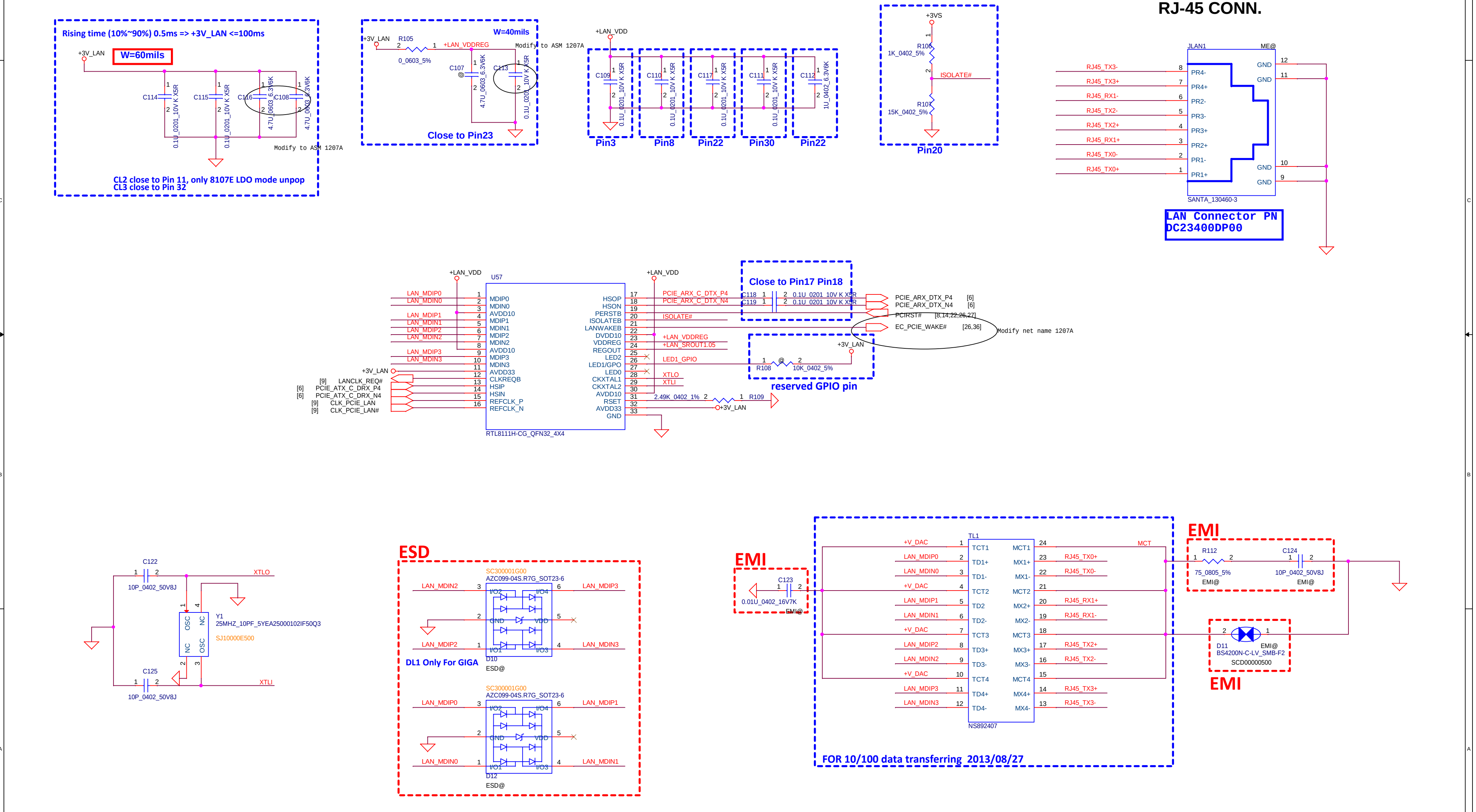


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date 2017/04/03	Title: HD Audio Codec_ALC3240
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size C, Document Number LA-F485P, Rev 0.2
			Date: Monday, December 18, 2017 Sheet 30 of 54



	1.0V Source	LL1	CL16,CL17	CL9,CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O

Please refer to the table above when using different 1.0V supply source.



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

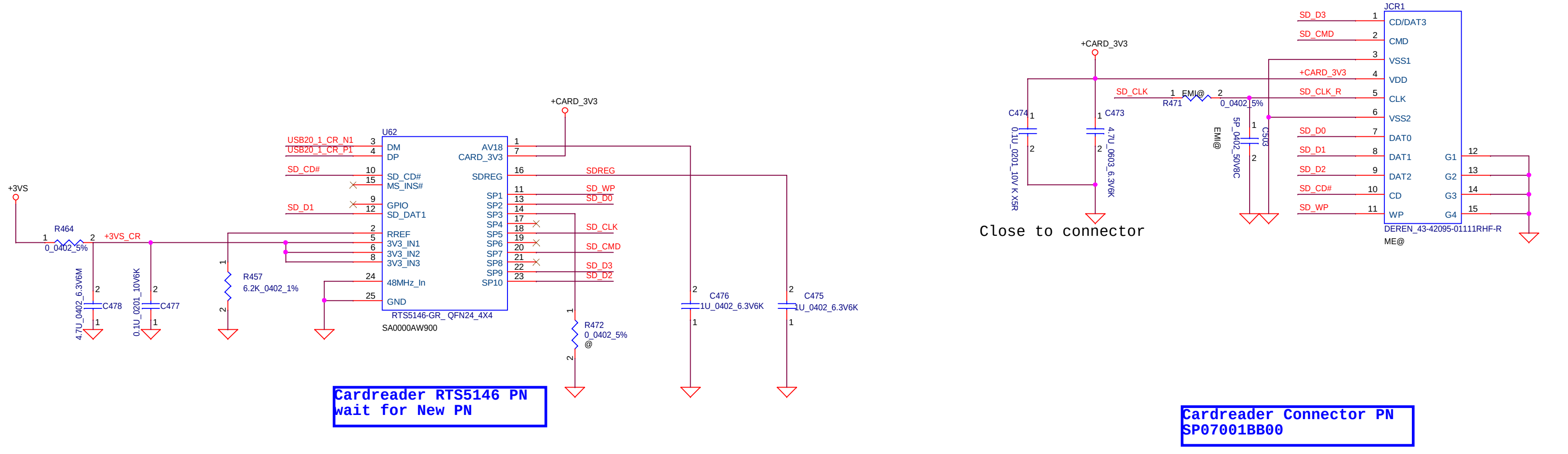
Compal Electronics, Inc.

Title: LAN_RTL8111H / RTL8107E

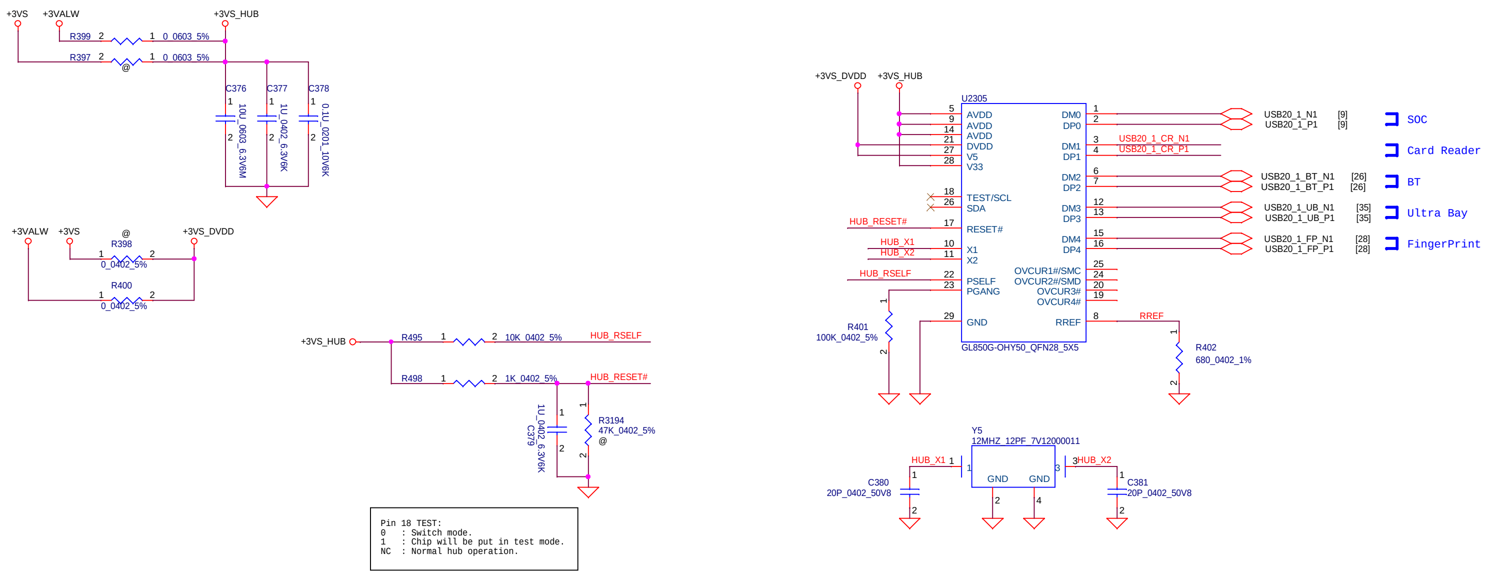
Size: C | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017 | Sheet 31 of 54

CardReader



USB20 HUB

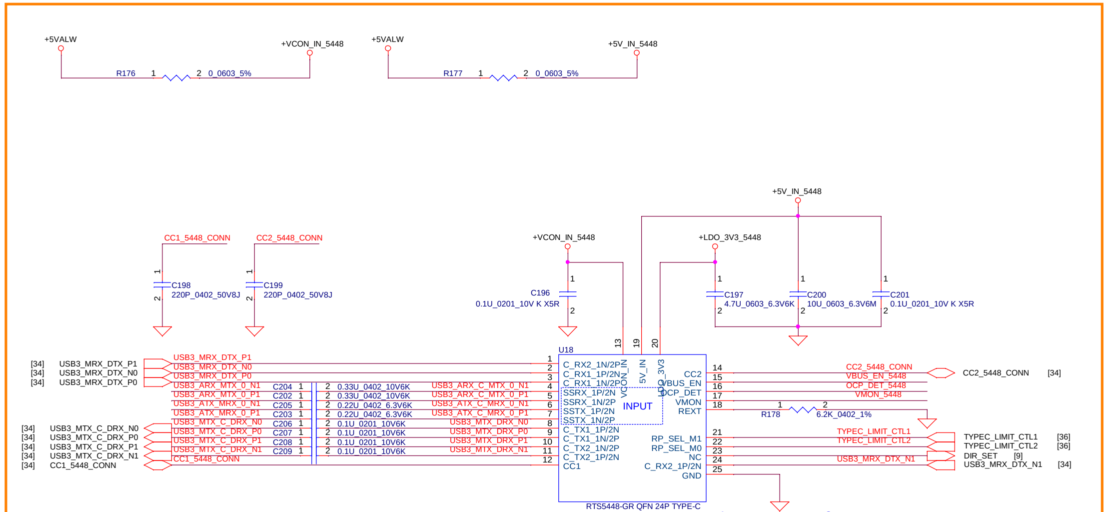


Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

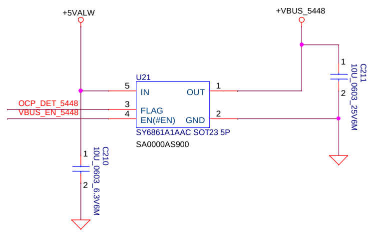
Compal Electronics, Inc.

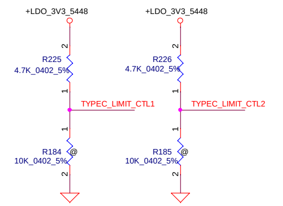
Title: **CARD READER/USB20 HUB**

Size	Document Number	Rev
C	LA-F485P	0.2



Change to RTS5448 for Customer request
Pin to Pin with RTS5441
0419B

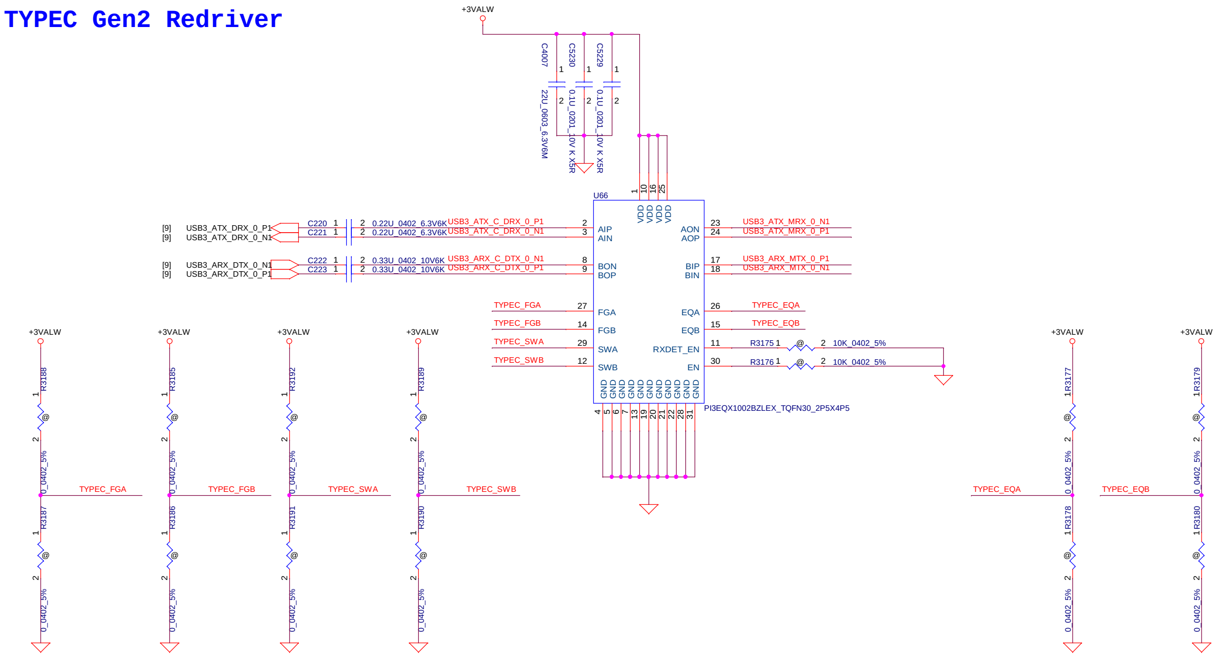


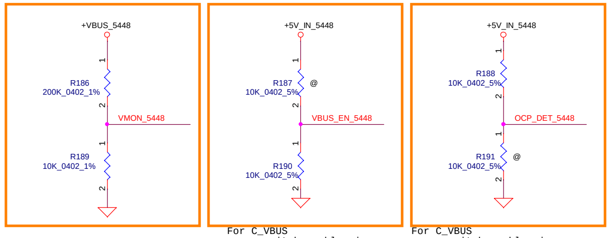


	M1	M0	Note
Rp:900mA	0	1	R184/R226 mount, R225/R185 don't mount
Rp:1.5A	1	0	R225/R185 mount, R184/R226 don't mount
Rp:3.0A	1	1	R225/R226 mount, R184/R185 don't mount

Rp configuration

TYPEC Gen2 Redriver





For C_VBUS power switch enable pin

For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R190/R187 mount
High Active	R190 mount, R187 don't mount

Pull Up & Down
Pull Down

Power switch OCP pin	Note
Low Active	R191/R188 mount
High Active	R191 mount, R188 don't mount

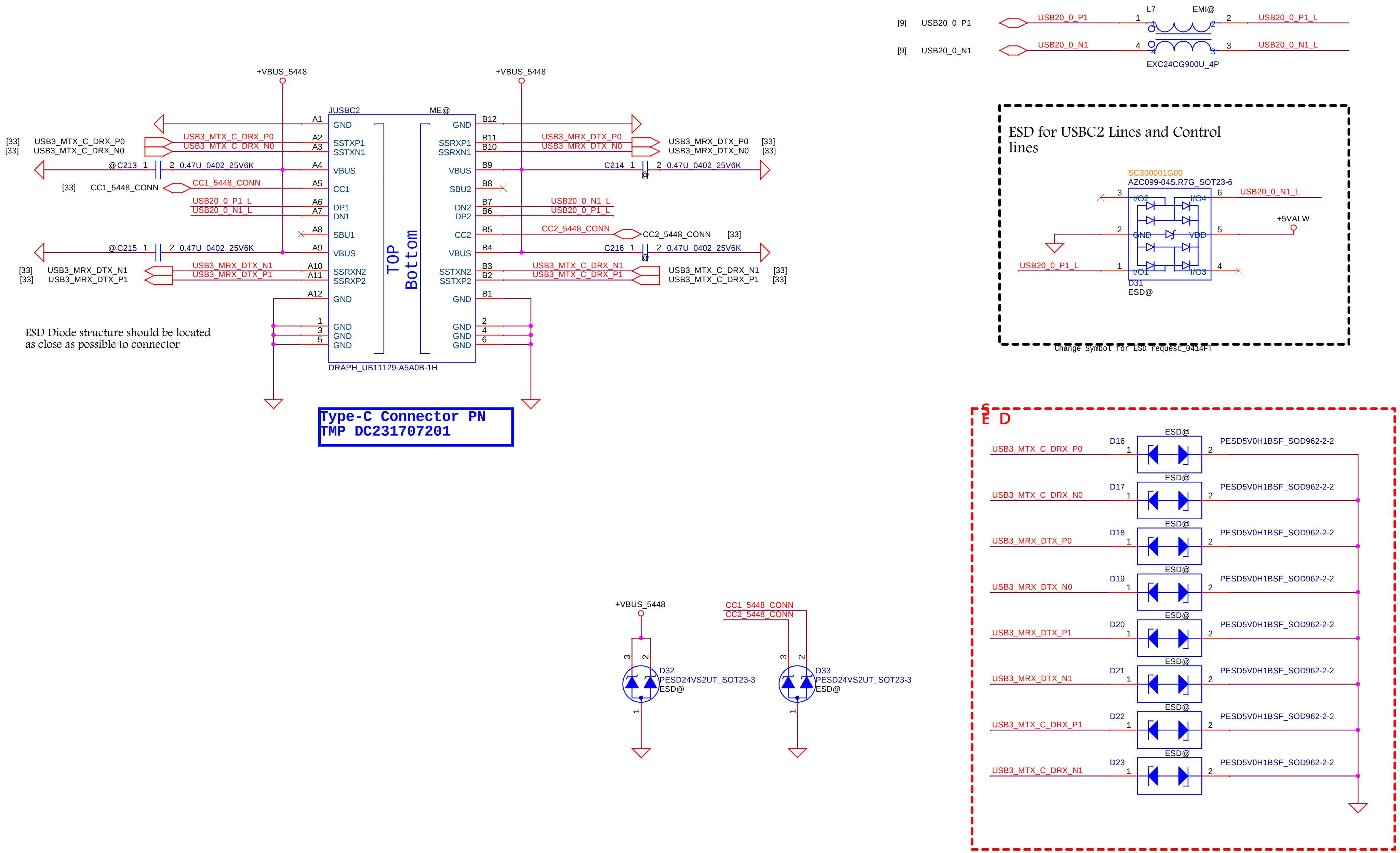
Pull Up & Down
Pull Down

Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

Compal Electronics, Inc.

Title: Type-C_RTS5441

Size: Custom | Document Number: LA-F485P | Rev: 0.2

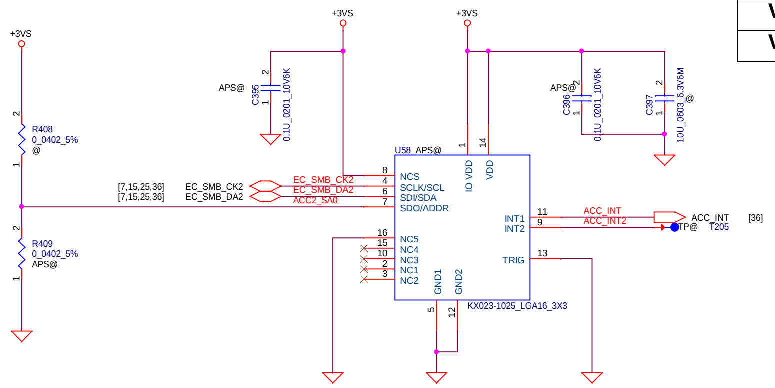


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: Type-C_RTS5441_CONN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 34 of 54

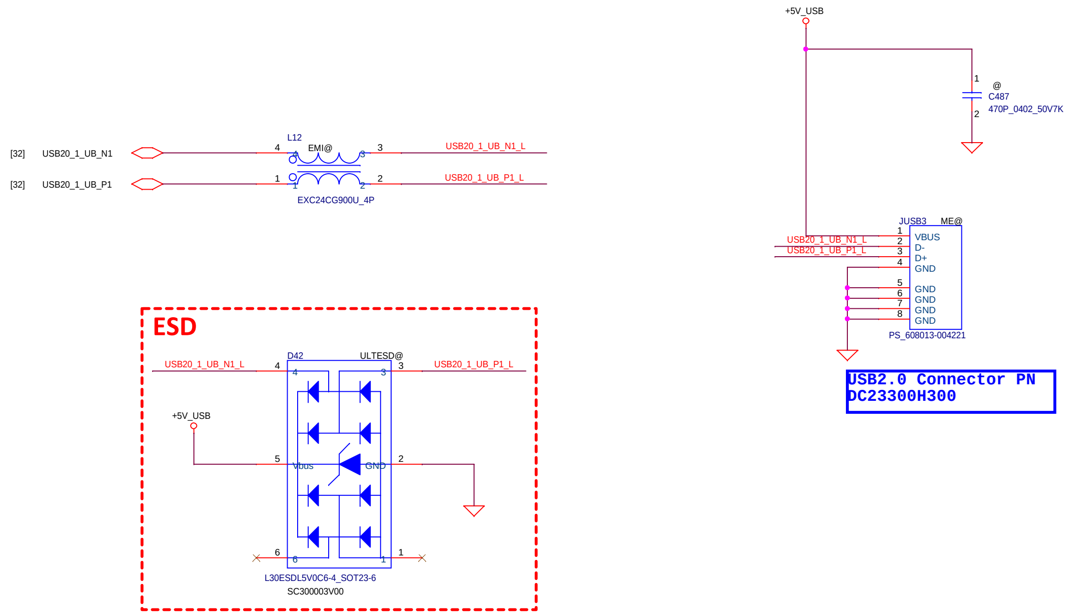
APS G-Sensor

Kionix KX023-1025

SDO/ADDR	Address R/W
VDD	3Fh/3Eh
VSS	3Dh/3Ch

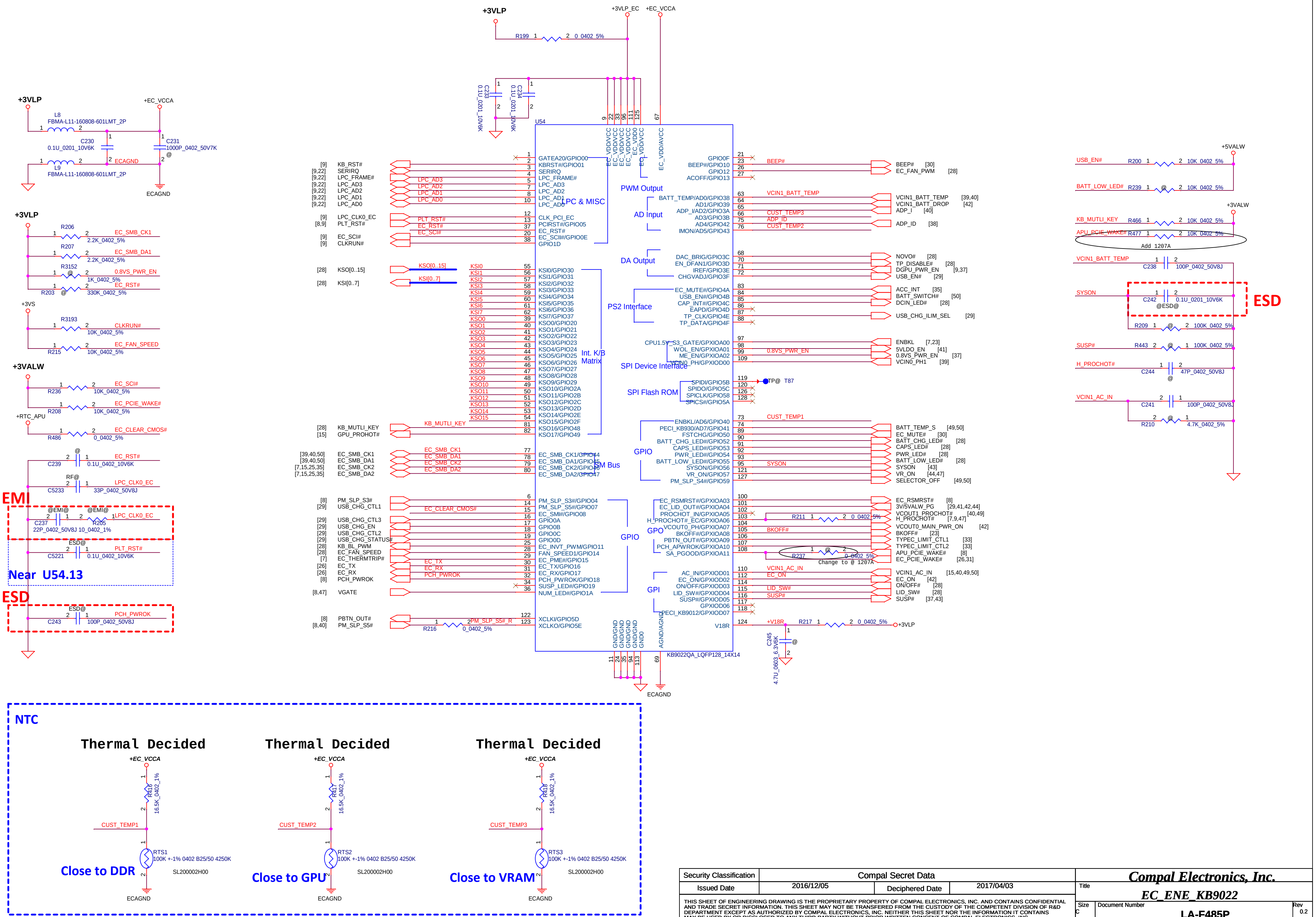


2nd Battery USB2_CONN



USB2.0 Connector PN DC23300H300

Title	APS_2nd Battery	
Size C	Document Number LA-F485P	Rev 0.2
Date: Monday, December 18, 2017	Sheet 35 of 54	



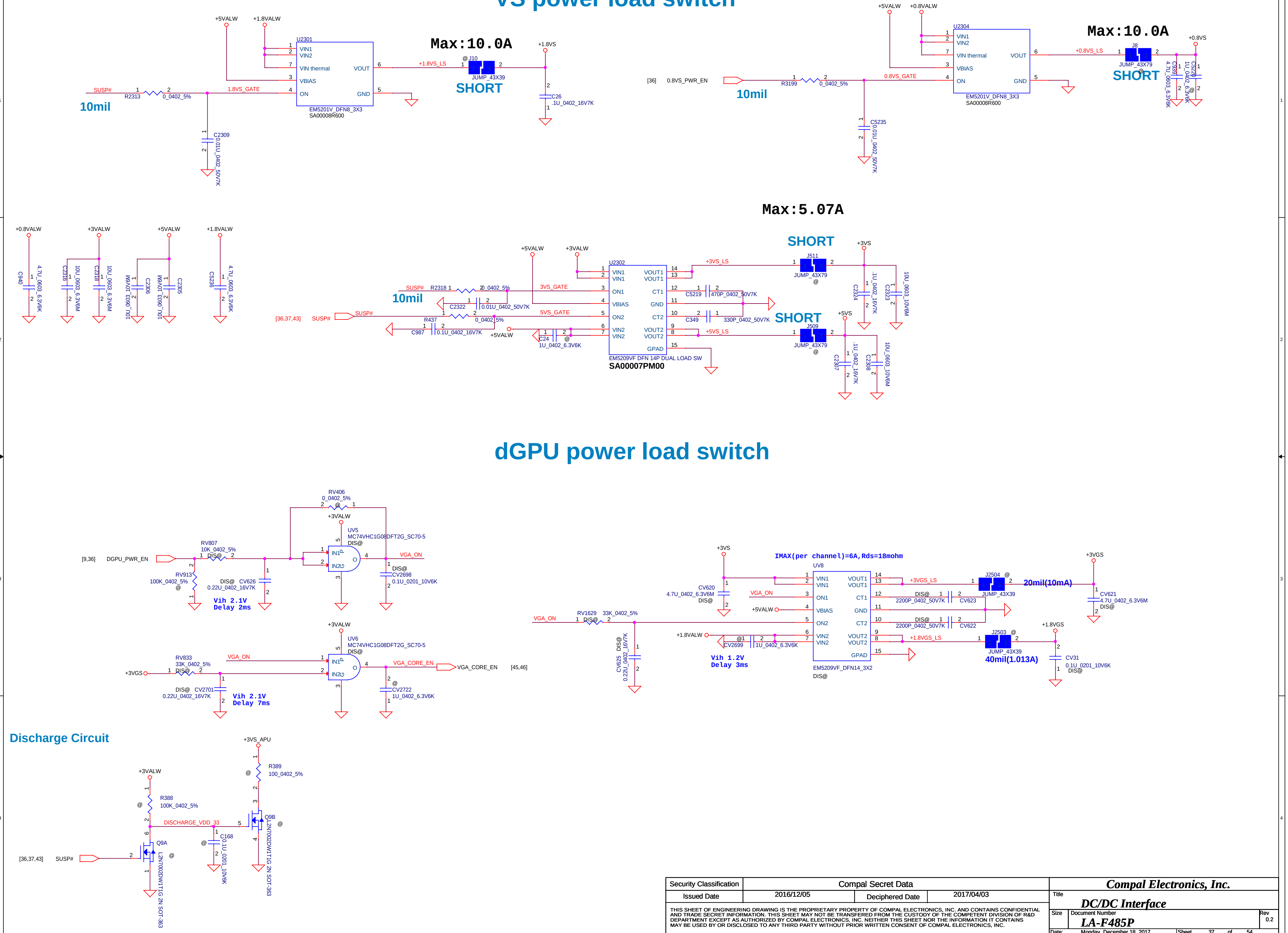
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: EC_ENE_KB9022
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size C / Document Number LA-F485P / Rev 0.2
				Date: Monday, December 18, 2017 / Sheet 36 of 54

Main Func = DC Interface

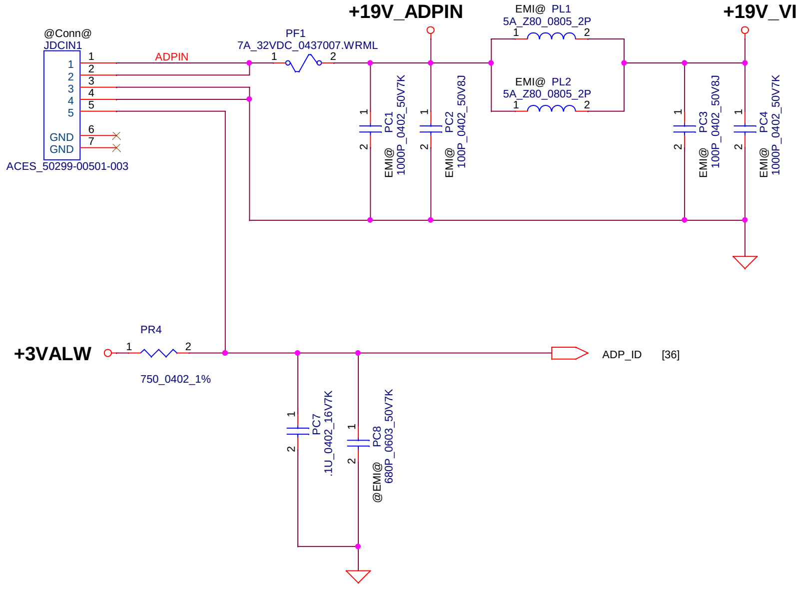
VS power load switch

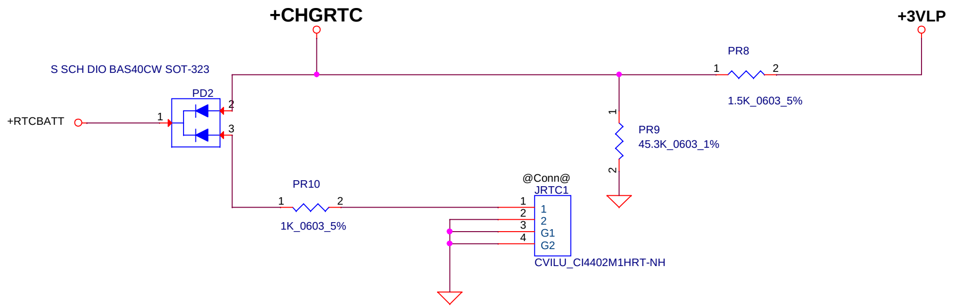
dGPU power load switch

Discharge Circuit



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title: DC/DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-F485P / Rev 0.2
				Date: Monday, December 18, 2017 / Sheet 37 of 54





BOM Structure Table

Item	BOM Structure
Support Type-C PD	PD@
For EMI	EMI@
For RF	RF@
For DIS	VGA@
For DIS of EMI	VGA_EMI@
For DIS of RF	VGA_RF@

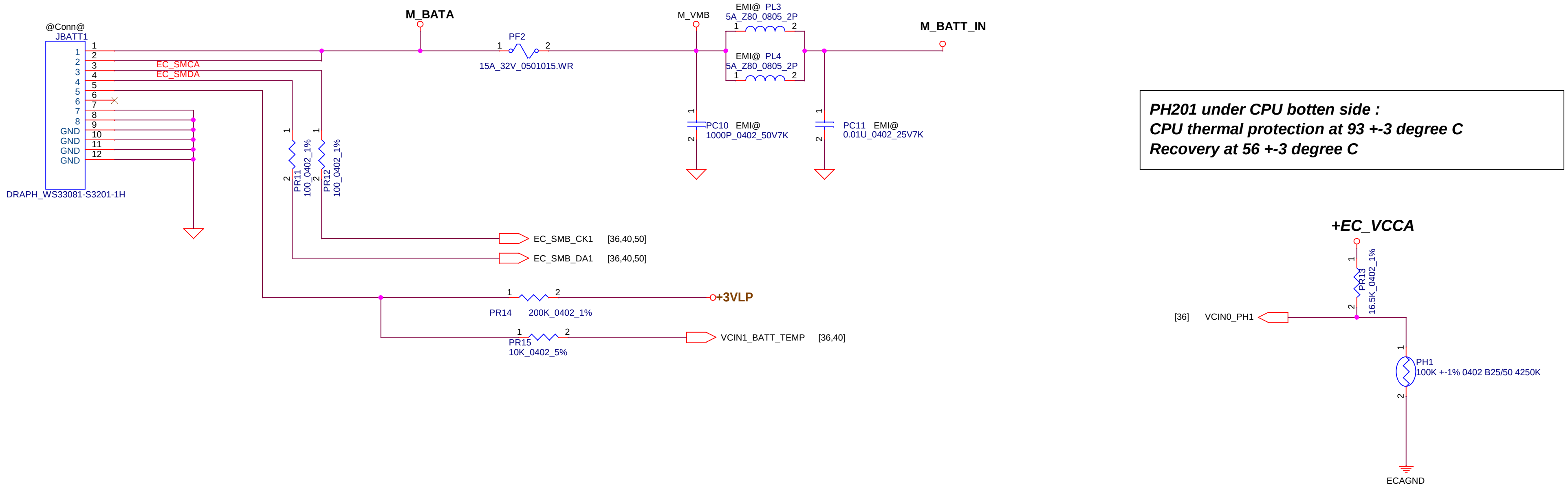
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR-DCIN / Vin Detector**

Size	Document Number	Rev
Custom	LA-F485P	0.2

Date: Monday, December 18, 2017 Sheet 38 of 54



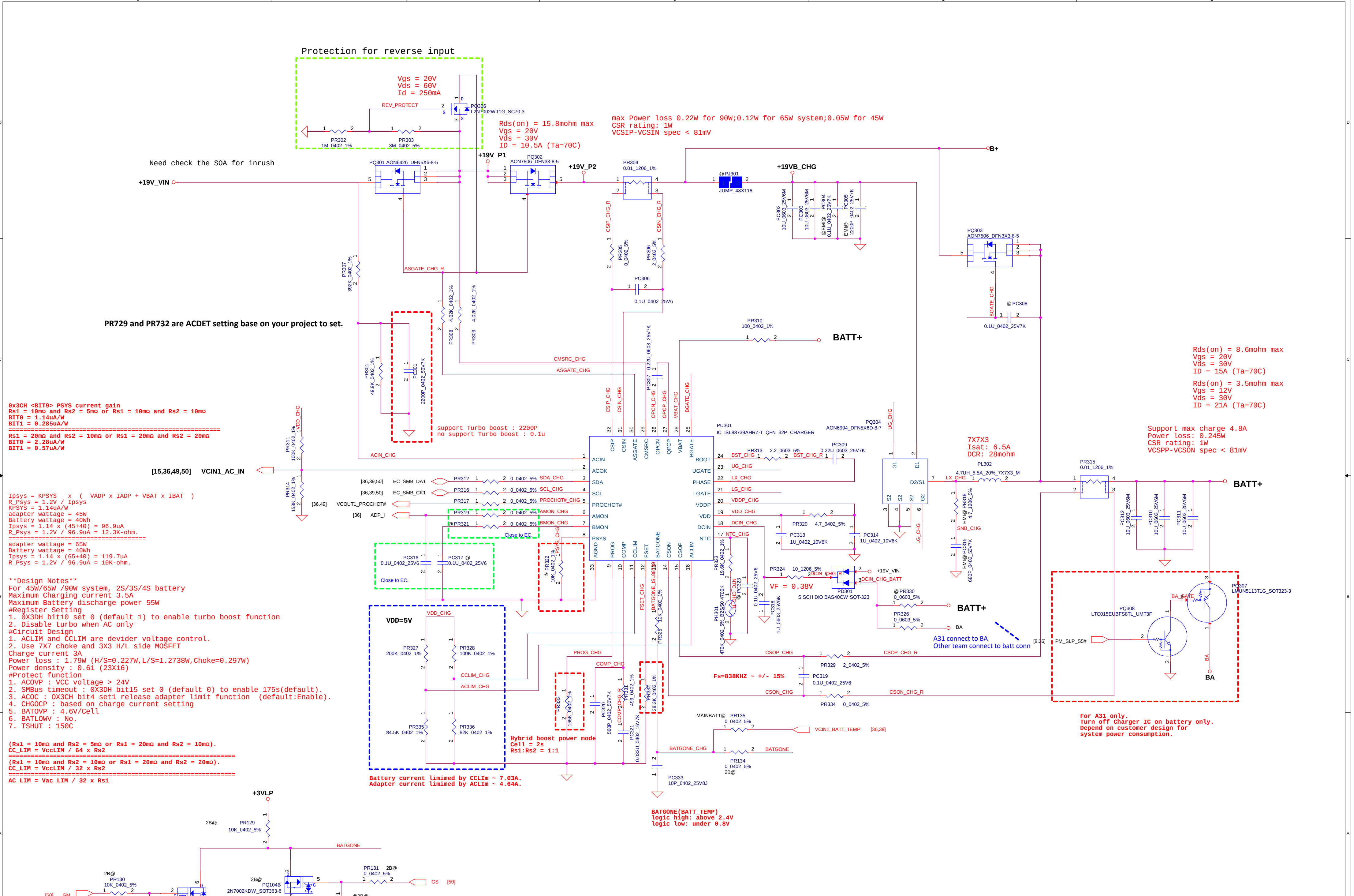
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

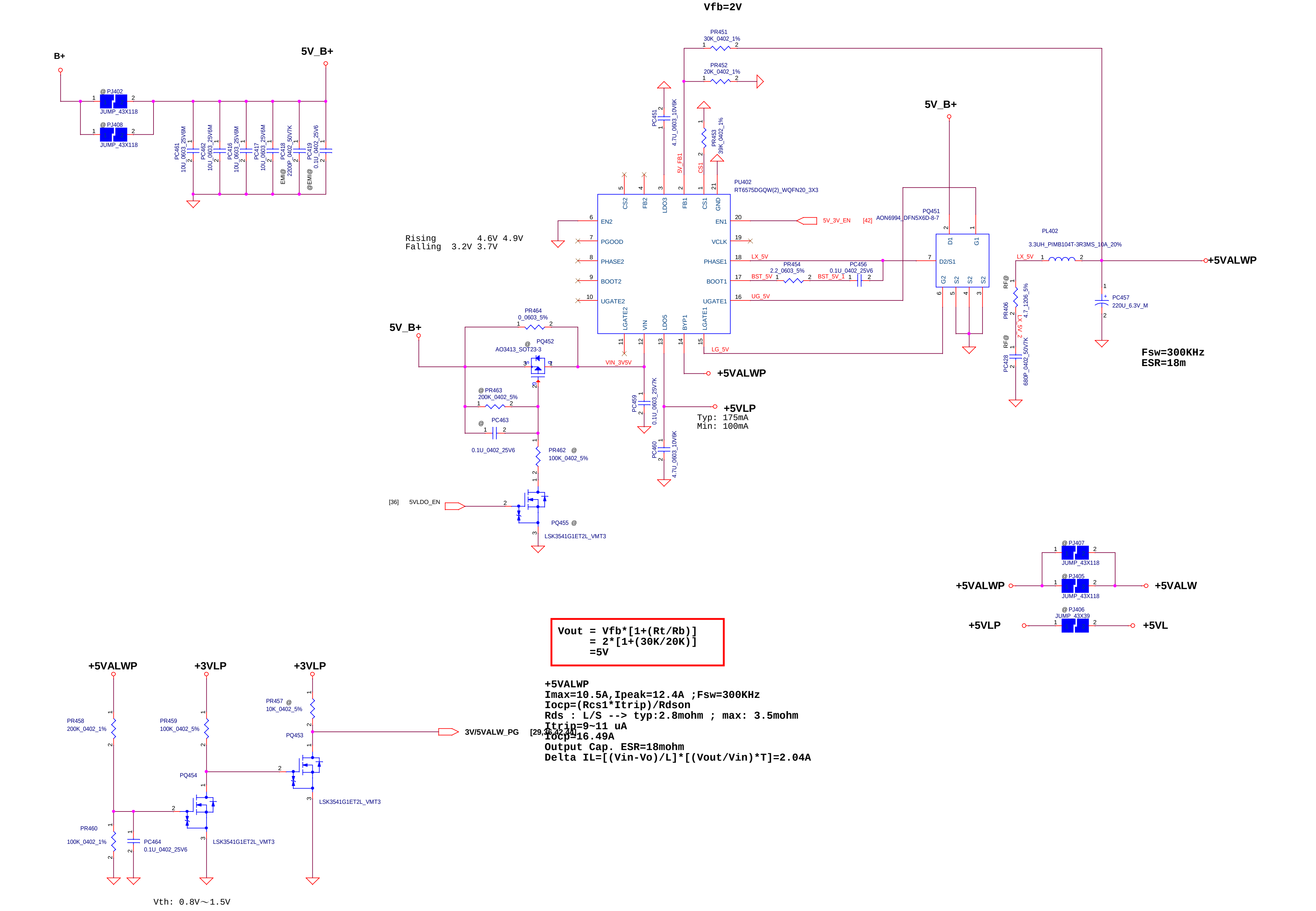
Title: **PWR-BATTERY CONN/OTP**

Size: Custom | Document Number: **LA-F485P** | Rev: 0.2

Date: Monday, December 18, 2017 |



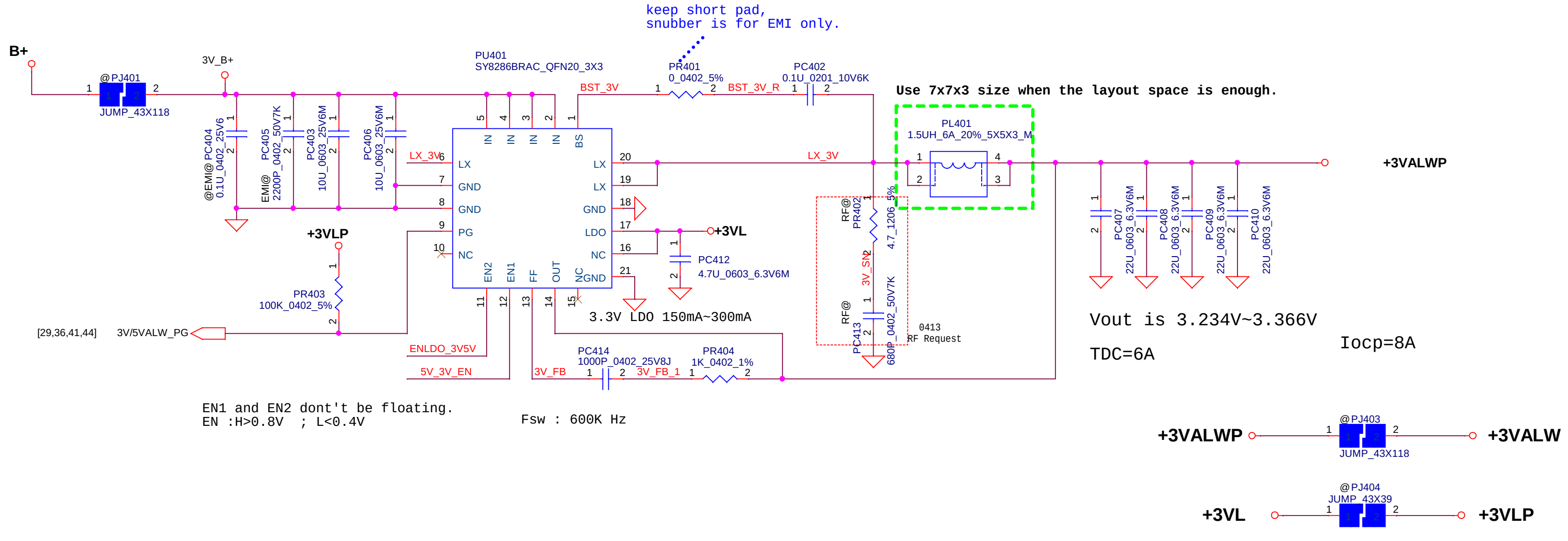
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/12/05	Title: PWR_CHARGER
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-E981P / Rev 0.2
				Date: Monday, December 18, 2017 / Sheet 40 of 54

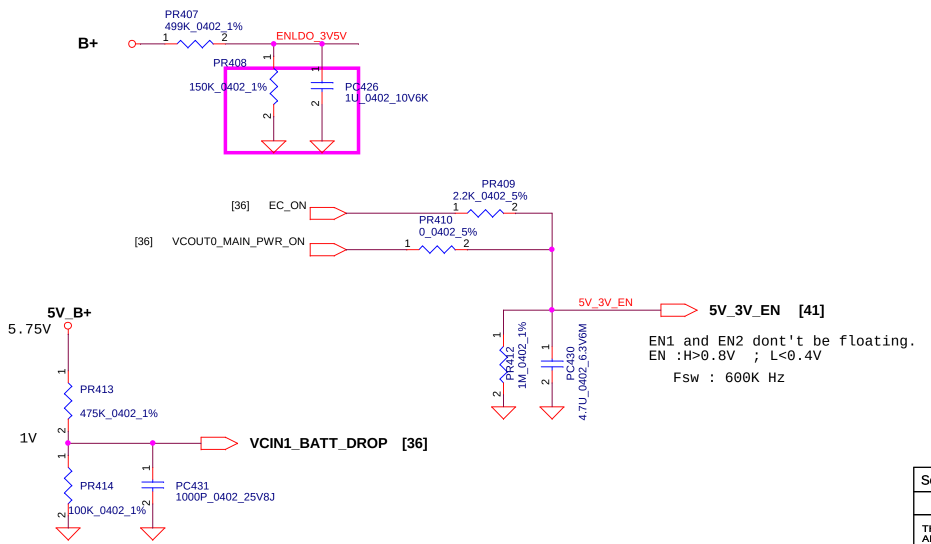


Vout = Vfb*[1+(Rt/Rb)]
     = 2*[1+(30K/20K)]
     =5V

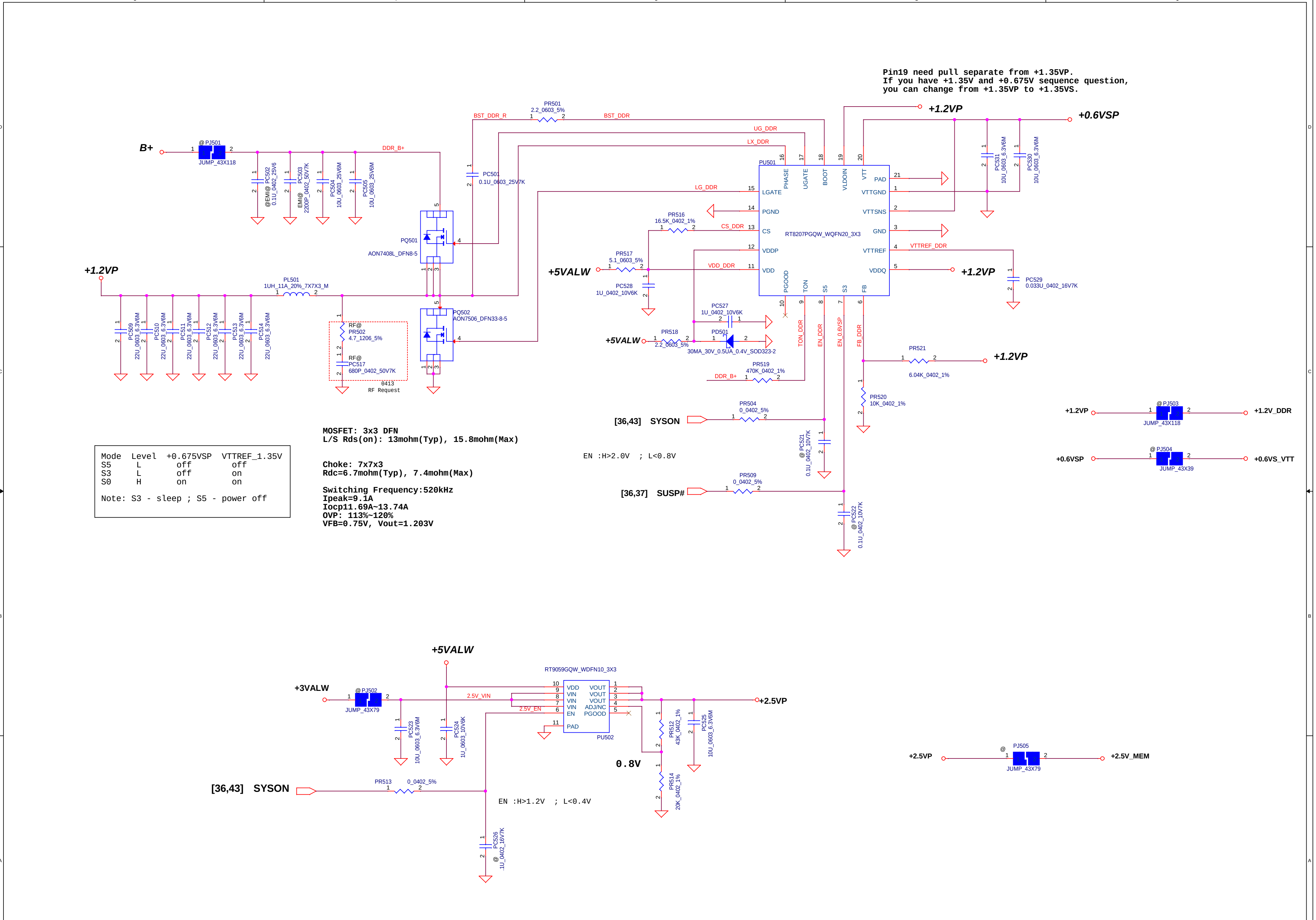
+5VALWP
Imax=10.5A,Ipeak=12.4A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:2.8mohm ; max: 3.5mohm
Itrip=9~11 uA
Iocp=16.49A
Output Cap. ESR=18mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.04A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date	2018/06/30	Title: PWR- 5VALWP
Size: C	Document Number: LA-F485P			Rev: 0.2
Date: Monday, December 18, 2017		Sheet 41 of 54		





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date	2018/06/30	Title: PWR- 3VALWP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-F485P; Rev 0.2
				Date: Monday, December 18, 2017; Sheet 42 of 54

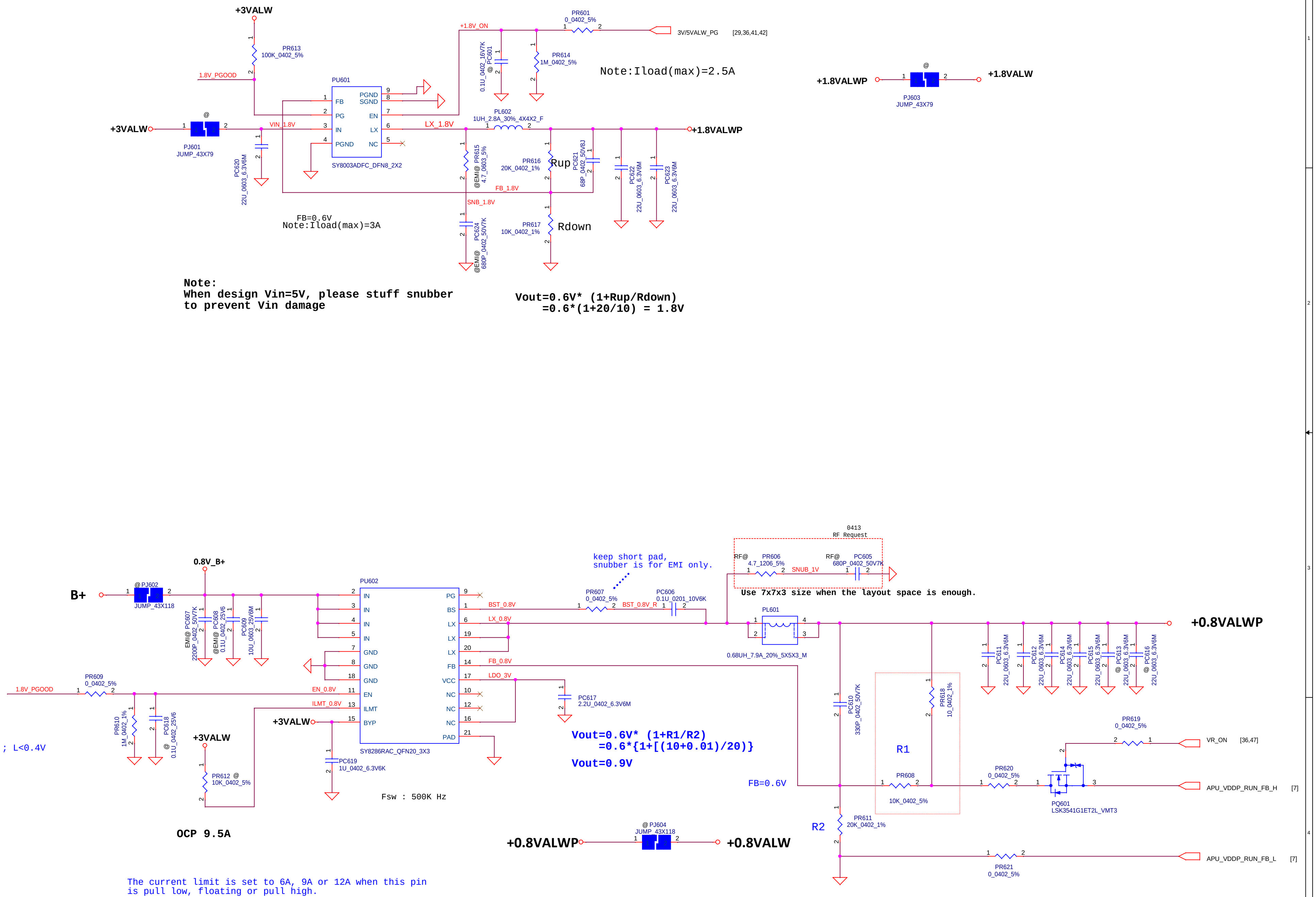


Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: PWR- 1.2VP/0.6VSP/2.5VP

Size: C | Document Number: LA-F485P | Rev: 0.2

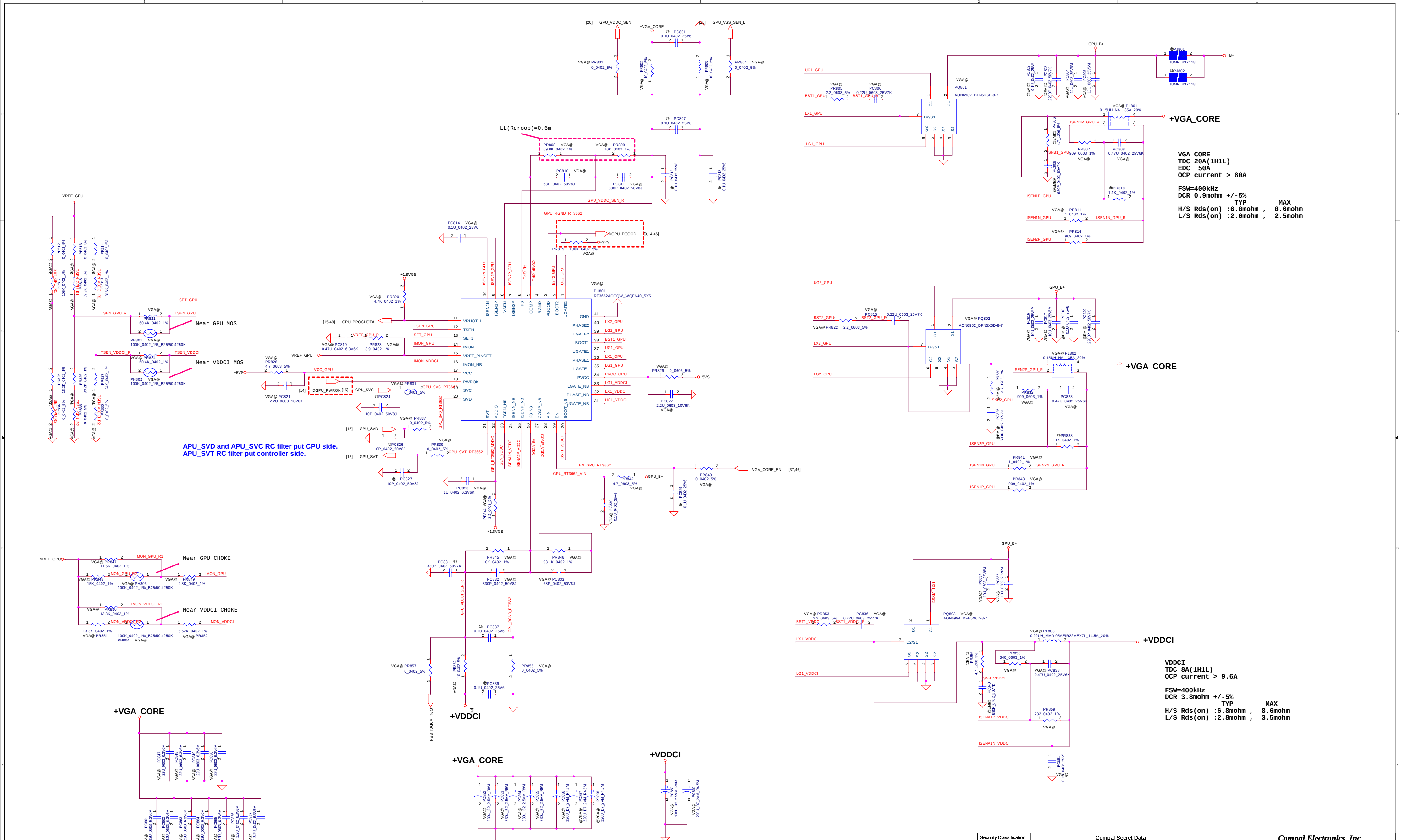


Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

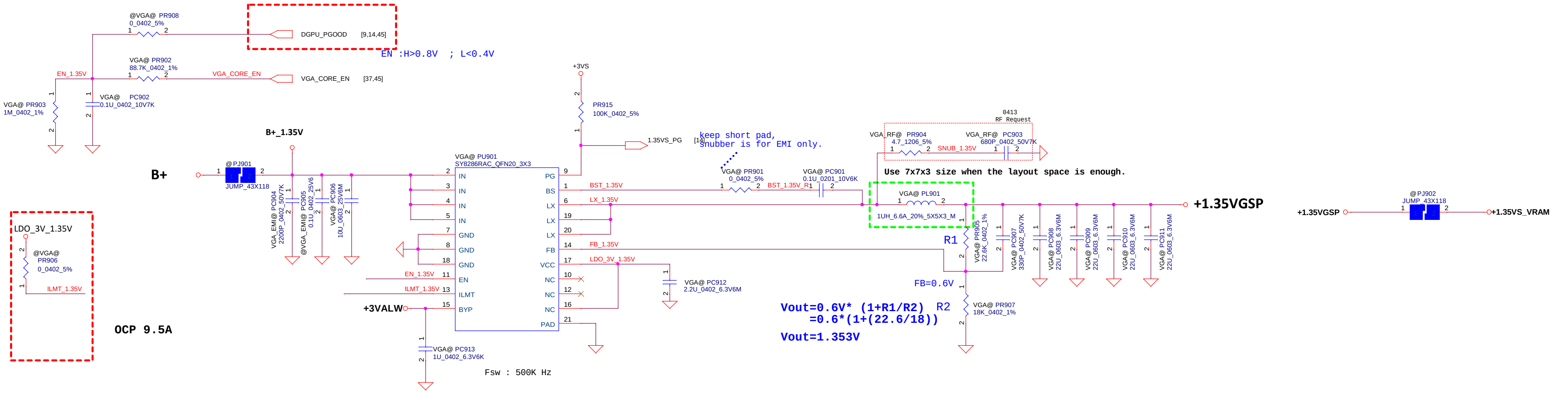
Compal Electronics, Inc.

Title: **PWR- 1.8VALWP/1VALWP**

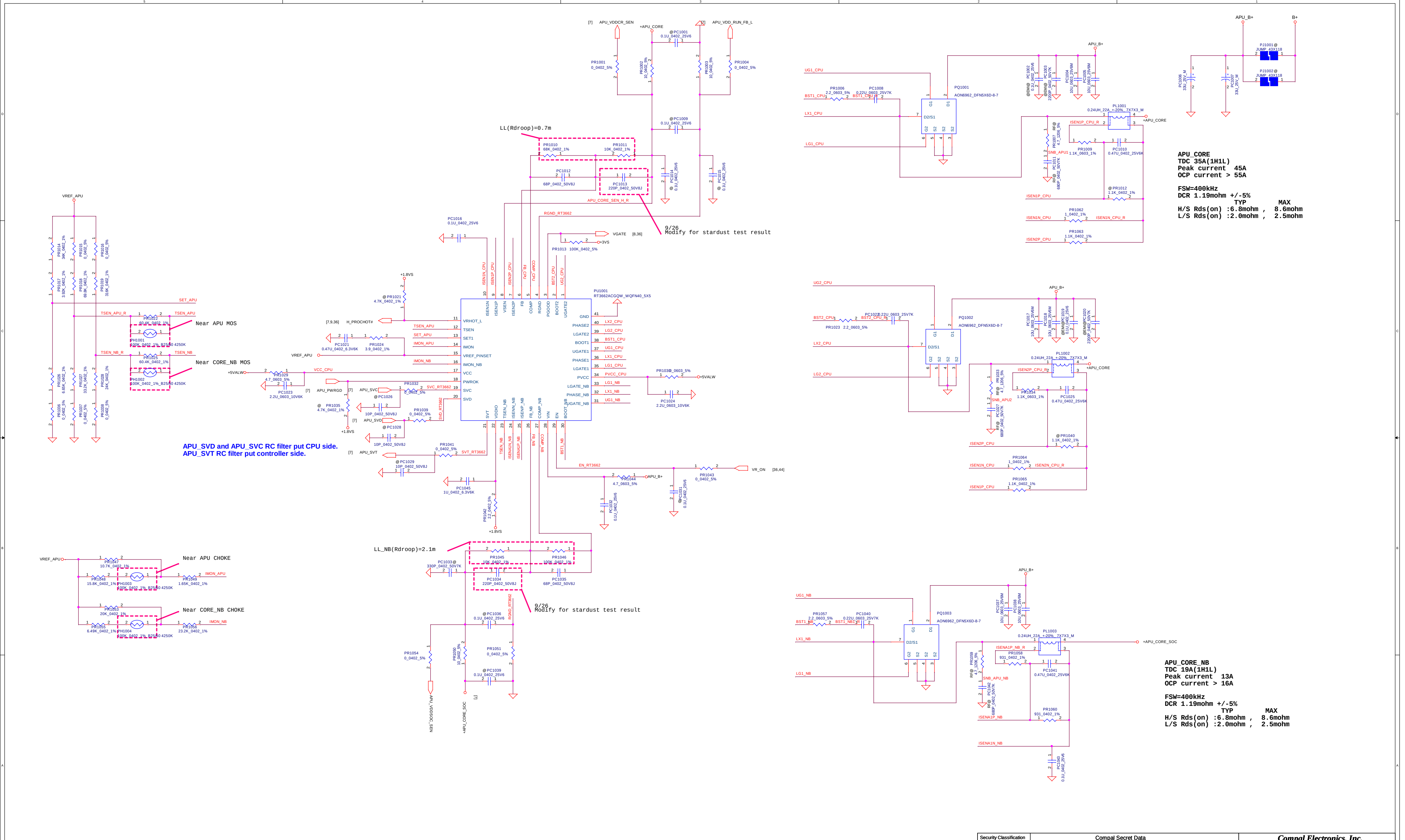
Size: C | Document Number: **LA-F485P** | Rev: 0.2



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/03/11	Deciphered Date 2019/03/11	Title: RT3662ACGQW
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number — Rev 0.2
			Date: Monday, December 18, 2017 — Sheet 45 of 54



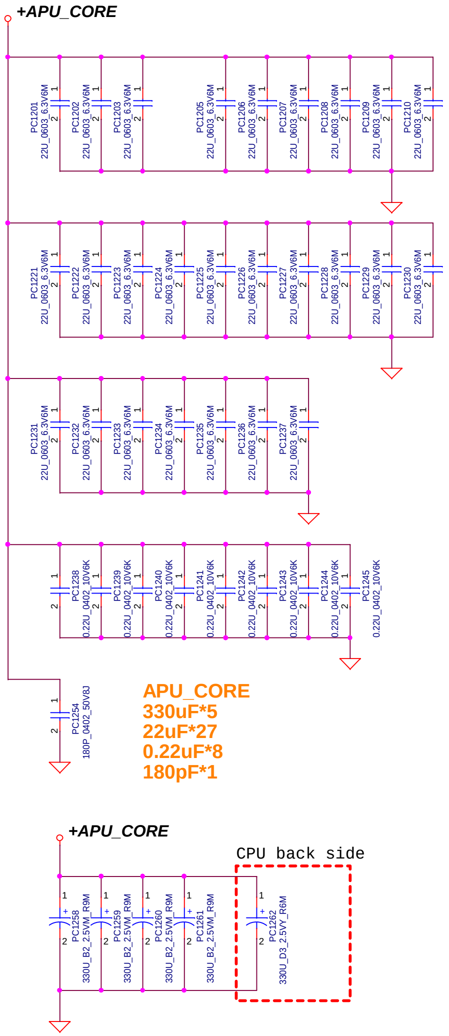
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date	2018/06/30	Title: PWR- 1.35VRAM
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-F485P; Rev 0.2
				Date: Monday, December 18, 2017; Sheet 46 of 54



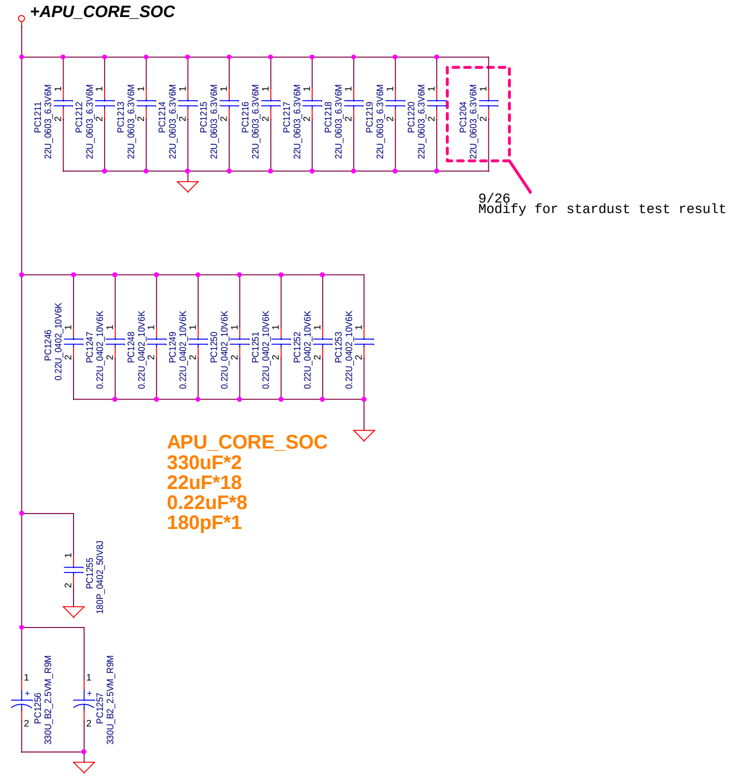
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/03/11	Deciphered Date 2019/03/11	Title: RT3662ACGQW

Size | Document Number | Rev 0.2

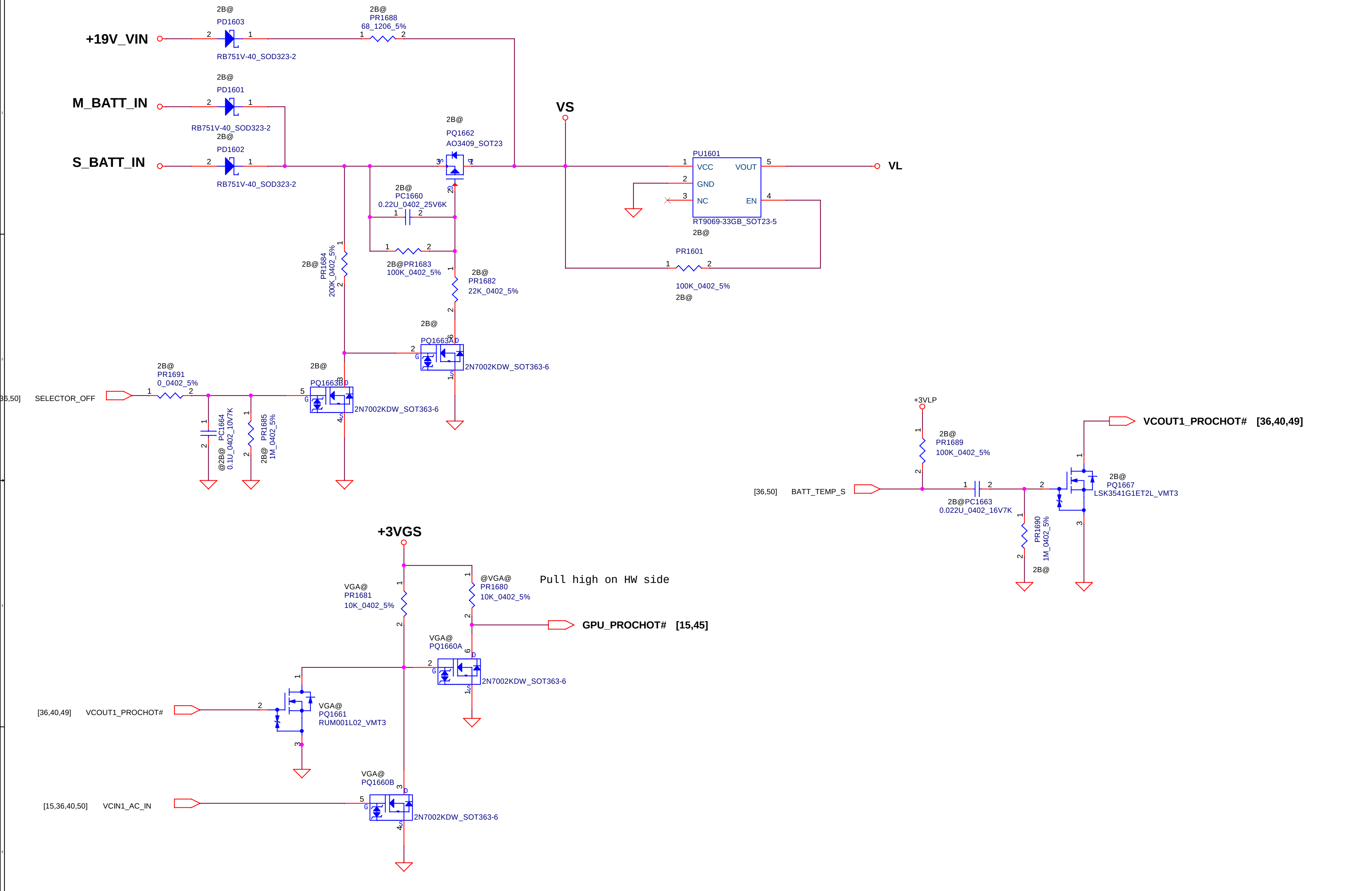
+APU_CORE



+APU_CORE_SOC



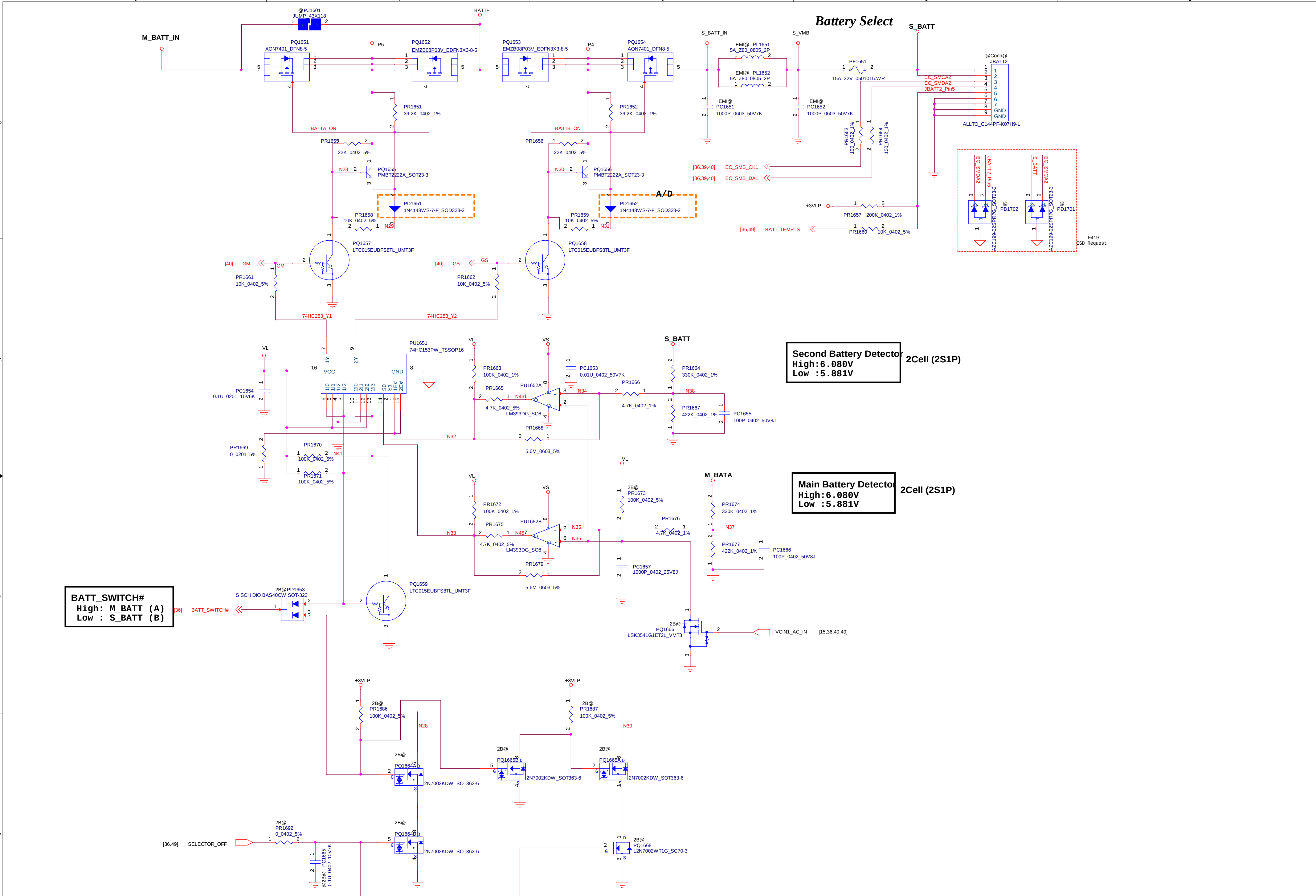
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/12/05	Title: +APU_CORE Cap
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: C; Document Number; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 48 of 54



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date 2018/06/30	Title: PWR- Battery Select (1/2)

Size: Custom | Document Number: LA-F485P | Rev: 0.2

Date: Monday, December 18, 2017 |



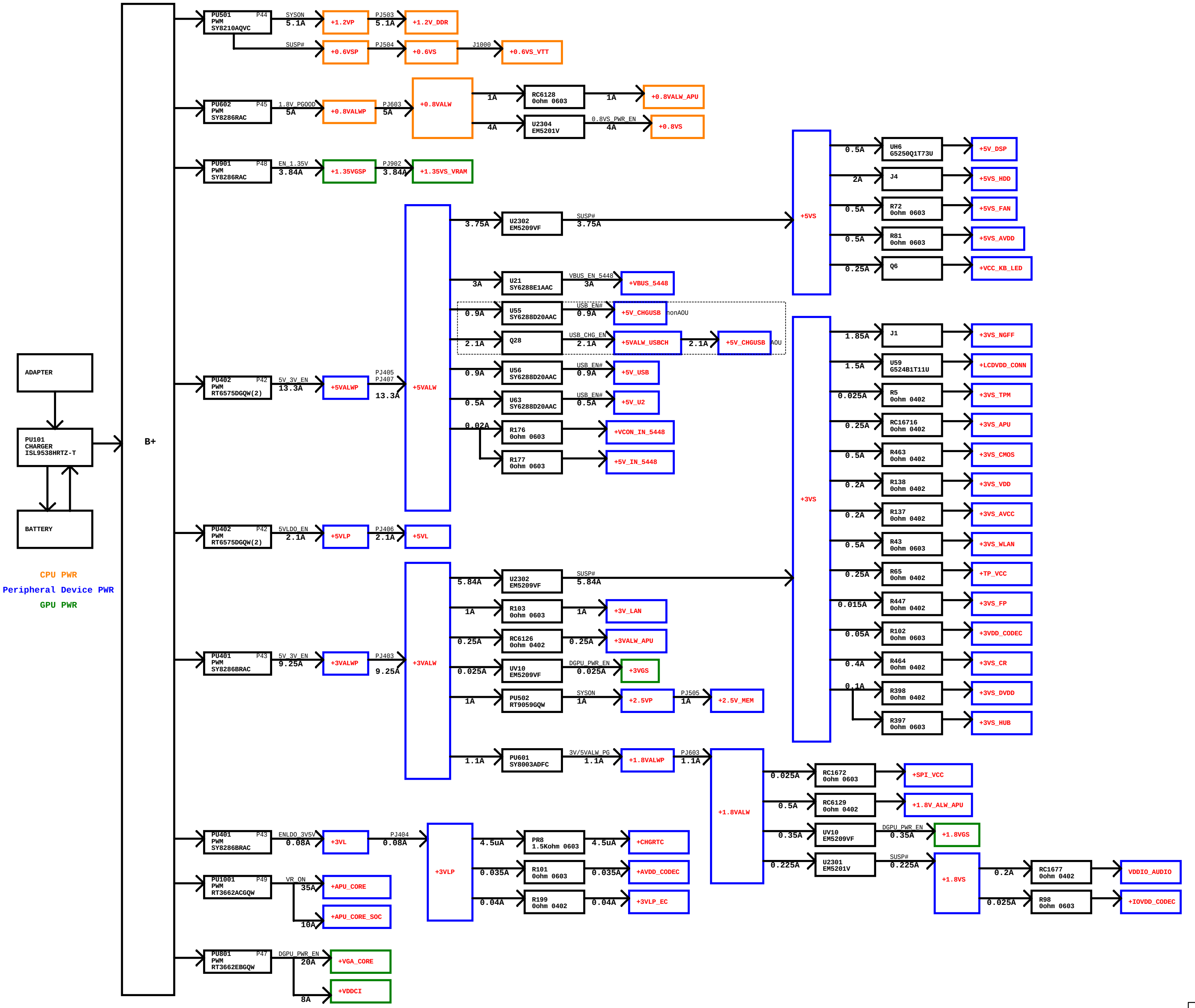
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date	2018/06/30	Title: PWR- Battery Select (2/2)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-F485P; Rev: 0.2
				Date: Monday, December 18, 2017; Sheet 50 of 54

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Consider component de-rating		Change PF3 from SP040003U00(S FUSE 0438005.WR 5A 32V UL/CSA FAST) to SP040003Q00(S FUSE S1206-H-7.0A 7A 32V UL FAST)	6/23	EVT
2	To avoid acustic issue		Change PC906,PC1004,PC1005,PC1017,PC1018,PC1037,PC1038,PC804,PC805 ,PC816,PC817 from SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE00000X200(S CER CAP 10U 25V M X5R 0603)	6/23	EVT
3	Change 5VLDO_EN to reserve		Add PR464(SD013000080,S RES 1/10W 0 +-5% 0603) Delete PQ455(SB00000VY00,S TR LSK3541G1ET2L 1N) Delete PQ452(SB934130000,S TR AO3413 1P SOT-23) Delete PR462,PR463,PC463	6/23	EVT
4	To reduce VS LDO component		Delete PQ1601(SB00000VY00,S TR LSK3541G1ET2L 1N) Delete PD1603(SCS00001200,S SCH DIO BAS40CW SOT-323) Delete PR1601,PR1602	6/23	EVT
5	Add remote sensing to +0.8VALW		Add PQ601(SB00000VY00,S TR LSK3541G1ET2L 1N) Add PR618	6/23	EVT
6	Modify 2nd battery circuit		Change PD1601 from SC1N4148180(S DIO 1N4148WS-7-F SOD-323) to SCS00000Z00(S SCH DIO RB751V-40 SOD-323) Add PD1603(SCS00000Z00,S SCH DIO RB751V-40 SOD-323)	6/23	EVT
7	Modify APU_CORE & APU_CORE_SOC switching frequency from 300K to 400K		Change PR1015 & PR1016 to 0_0402_5% Change PR1018 to 69.8K_0402_1% Change PR1019 to 32.4K_0402_1%	6/23	EVT
8	Modify +0.8VALW OCP setting(min 9.5A)		Change PR612 to reserve	6/23	EVT
9	Modify BATGONE circuit		Change PR130 to 10K_0402_1% Add PC134 to 0.47U_0402_6.3V6K	6/23	EVT
10	Modify BATGONE circuit		Add PR135(0_0402_5%)	6/29	EVT
11	Modify +0.95VGS output voltage		Change PR1502 from 20K_0402_1% to 10K_0402_1%	6/29	EVT
12	Reduce S5 leakage current		Change PR413 from 47.5K to 475K Change PR414 from 10K to 100K	6/29	EVT
13	Remove PD function		Delete PC5,PC6,PC9,PD1,PQ1,PQ2,,PR1,PR2,PR3,PR5,PR6,PR7,PC12,PC13, PC14,PC15,PD3,PF3,PQ3,PQ4,PR16,PR17,PR18,PR19	6/29	EVT
14	Change charger IC solution to ISL88739A			6/29	EVT
15	Modify power sequence for GPU		Change PR902 from 0_0402_5% to 88.7K_0402_1% Change PR1503 from 0_0402_5% to 47K_0402_1% Add PC902 & PC1504(0.1U_0402_10V7K)	7/5	EVT
16	Change GPU CORE solution for R17M-P1-50 GPU		Change PU801 from RT3662EB to RT3662AC	7/25	EVT
17	Delete +0.95VGS power rail for GPU change		Delete PU1501	7/25	EVT
18	Change DDR power solution for cost saving		Change PU501 from SY8210AQVC to RT8207P	7/25	EVT
19	For reduce S5 leakage current , turn off selector in S5		Add PQ1662 ,PQ1663 Add PR1684 , PR1683 , PR1682, PR1691 , PR1685 Add PC1660 , PC1664	7/25	EVT
20	Add prochot function when 2nd battery removed		Add PQ1667 . PR1689 , PR1690 , PC1663	7/25	EVT
21	Modify 2nd battery circuit		Add PQ1666 , PQ1664 , PQ1665 , PD1653 Add PR1666 , PR1687 , PR1692	7/25	EVT
22	Modify for power sequence		Add PR613(100K_0402_5%)	8/8	EVT
23	Modify VGA CORE CHOKE and OCP setting		Change PL801,Pl802 from 0.15UH +-20% 36A 7X7X4(SH00001EE00) to 0.15UH +-20% 35A 7X7X3(SH00001EF00) Change PR807,PR832 from 1.1K_0603_1% to 909_0603_1% Change PR816,PR843 from 1.1K_0402_1% to 909_0402_1% Change PR847 from 13K_0402_1% to 11.5K_0402_1% Change PR848 from 13.7K_0402_1% to 15K_0402_1% Change PR849 from 5K_0402_1% to 2.8K_0402_1%	8/9	EVT

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Item	Reason for change	PG#	Modify List	Date	Phase
1	Modify 2nd battery circuit		Add PQ1668(L2N7002WT1G_SC70-3,SB00000ST00) Change PQ1662 from AO3413_SOT23-3 to AO3409_SOT23-3	9/26	DVT
2	Modify P/N for 2nd source		Change PD301 from SCS00008E00(LRB715FT1G SOT323-3) to SCS00001200(BAS40CW SOT-323)	9/26	DVT
3	Modify for AMD stardust test result		Change PR1046 from 80.6K_0402_1% to 100K_0402_1% Change PC1013 & PC1034 from 330P_0402_50V8J to 220P_0402_50V8J Change PR1027 from 24K to 33.2K	9/26	DVT
4	Correct BOM error		Add PR509(0_0402_5%) Delete PR1021(4.7K_0402_1%)	9/26	DVT
5	Modify for cost down action		Change PC1655 & PC1656 From SE068101K80(S CER CAP 100P 25V K NPO 0402) to SE071101J80(S CER CAP 100P 50V J NPO 0402)	10/6	DVT
6	Modify for cost down action(EMI)		Change PL1,PL2,PL3,PL4,PL1651 & PL1652 from SM01000P200(S SUPPRE_ 5A Z120 25M 0805) to SM01000U600(S SUPPRE_ 5A Z80 20M 0805)	10/6	DVT
7	Modify for cost down action(EMI)		Change PC315,PC413,PC428,PC517,PC605,PC903,PC1011,PC1027,PC1042 from SE025681K80(S CER CAP 680P 50V K X7R 0603) to SE074681K80 (S CER CAP 680P 50V K X7R 0402)	10/6	DVT
8	Follow AMD suggestion, modify 0.8VALWP to 0.9V		Change PR608 from 6.98K to 10K	10/16	DVT
9	Add remote sensing for 0.8VALWP		Add PR619, PR620 ,PR621(0_0402_5%)	10/16	DVT
10	Modify VR_HOT Setting		Change PR1019 from 32.4K_0402_1% to 316K_0402_1%	12/5	PVT
11	Change P/N		Change PC1006 & PC1007 SF000007200(common P/N) to SF000005200	12/5	PVT
12	Change P/N for shortage issue		Change PC313,PC314,PC426 SE00000OU00(1U_0402_16V6K) to SE00000QL10 (1U_0402_10V6K)	12/5	PVT
13	Modify GPU power sequence.		Add PR915(100K_0402_5%)	12/18	PVT



Title	Power MAP		
Size C	Document Number LA-F485P		Rev 0.2
Date: Monday, December 18, 2017	Sheet 53	of 54	

HW SIT PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	17/11/27	15	Add other SCH	Follow HW3 GPU prochot design
2	17/12/07	26, 31	Modify APU_PCIE_WAKE# to EC_PCIE_WAKE#	Follow Intel design
3	17/12/07	36	Add R477 PU to 3VALW	Add EC_PCIE_WAKE# PU prevent floating
4	17/12/07	36	R237 change to @	Seprate WAKE pin, let EC to control
5	17/12/07	31	C116, C108, C113 to ASM	For EMI requirement
6	17/12/18	9	RC88/RC89 change to 33ohm	For EMI requirement
7	17/12/18	16	Change CV450/451 to 15P	Follow XTAL vendor recommand
8	17/12/18	14	Add UV7, RV10~13	AMD GAE recommand
9	17/12/18	9	Change UC1.BA17 net name from DGPU_PWROK to DPGU_PGOOD	AMD GAE recommand