# Model Name: MTQ45NK-LE

*Revision 1.0*

| SHEET | TITLE |
|---|---|
| 01 | COVER SHEET |
| 02 | BOM & PCB MODIFY HISTORY |
| 03 | LGA775_A |
| 04 | LGA775_B |
| 05 | LGA775_C |
| 06 | LGA775_D |
| 07 | GMCH-HOST,PCIE,DMI |
| 08 | GMCH-DDRIII |
| 09 | GMCH-VGA,MISC |
| 10 | GMCH-GND |
| 11 | GMCH-POWER |
| 12 | DDRIII CHANNEL A |
| 13 | DDRIII CHANNEL B |
| 14 | DDRIII TERMINATION |
| 15 | SWITCH&DVI |
| 16 | PCIE SLOT X16,X1 |
| 17 | ICH10-PCI,PCIE,USB,DMI |
| 18 | ICH10-HOST,HDA,LAN,RTC,SPI,LPC,SATA |
| 19 | ICH10-POWER,GND |
| 20 | PCI SLOT |
| 21 | CKG IDT CV184 |
| 22 | SIO SCH5617, TH, FDD |
| 23 | COM, KB/MS, LPT |
| 24 | WPCT200AA, ST19WP18 |
| 25 | FRONT PANEL,BUZZER |
| 26 | FRONT USB & REAL USB |
| 27 | FAN CONTROL |

| SHEET | TITLE |
|---|---|
| 28 | DISCRETE POWER 1 |
| 29 | DISCRETE POWER 2 |
| 30 | VCORE PWM_NCP5392 |
| 31 | AUDIO CODEC |
| 32 | AUDIO JACK |
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| 34 | INTEL 82567LM/LF |
| 35 | NB&SB for GPIO LIST & STRAP |
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| 37 | POWER DELIVERY |
| 38 | POWER SEQUENCE |
| 39 | RESET&PWROK&CLOCK DELIVERY |
| 40 | BOM & PCB MODIFY HISTORY |
| 41 | |
| 42 | |

Example Fab Drawing Note

| Trace Width (mils) | Differential Spacing (mils) | Impedance | Tolerance |
|---|---|---|---|
| 4 | NA | 50 ohm, single-ended | 15% |
| 6.5 | NA | 40 ohm, single-ended | 15% |
| 7.5 | NA | 37 ohm, single-ended | 15% |
| 9.5 | NA | 32 ohm, single-ended | 15% |
| 4 | 8 | 95 ohm, differential | 20%, reference only |
| 4.5 | 7.5 | 90 ohm, differential | 20%, reference only |
| 5 | 5 | 85 ohm, differential | |

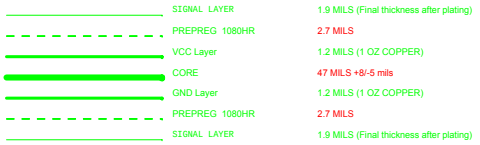
**BEARLAKE Impedance Requirements by Interface**

| Interface | Impedance Required |
|---|---|
| FSB(ALL) | 4x signals 42Ω others 50Ω, single-ended |
| Controller Link | 50 ohm, single-ended |
| PCI Express*2.0 | 85 ohm, single-ended |
| DMI | 95 ohm, differential |
| VGA | 37 ohm, single-ended at (G)MCH breakout, then 50 ohm single-ended to VGA connector. |

**ICH10 Impedance Requirements by Interface**

| Interface | Impedance Required |
|---|---|
| PCI | 50 ohm, single-ended |
| Controller Link | 50 ohm, single-ended |
| Miscellaneous | 50 ohm, single-ended |
| PCIE & DMI | 95 ohm, differential |
| SATA | 95 ohm, differential |
| USB | 90 ohm, differential |

4-layer stack-up total thickness=59mils

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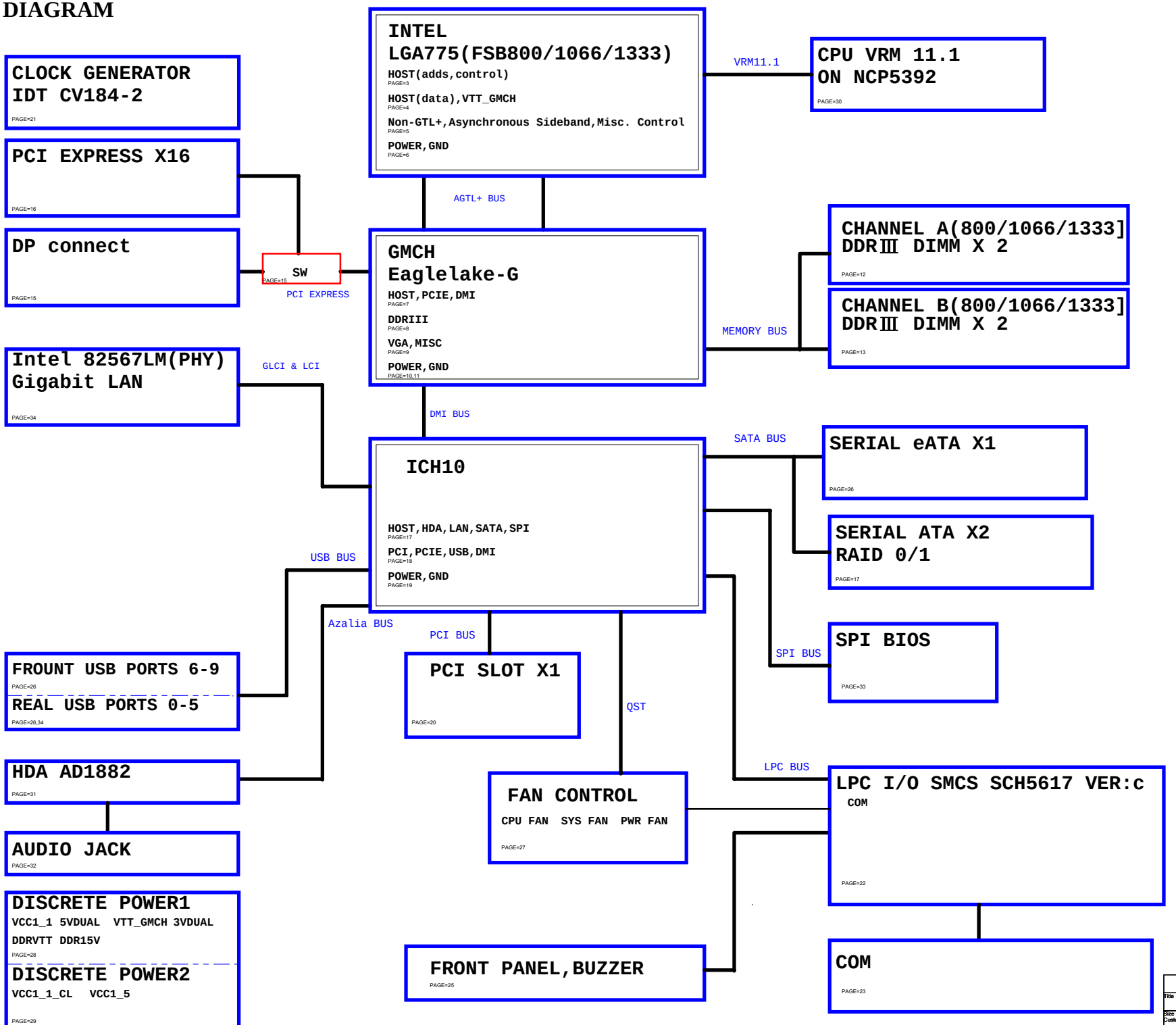
| Title | | |
|---|---|---|
| Cover Sheet | | |
| Size: C | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 1 of 40 | |

# BLOCK DIAGRAM

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| | | |
|---|---|---|
| Title | BLOCK DIAGRAM | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
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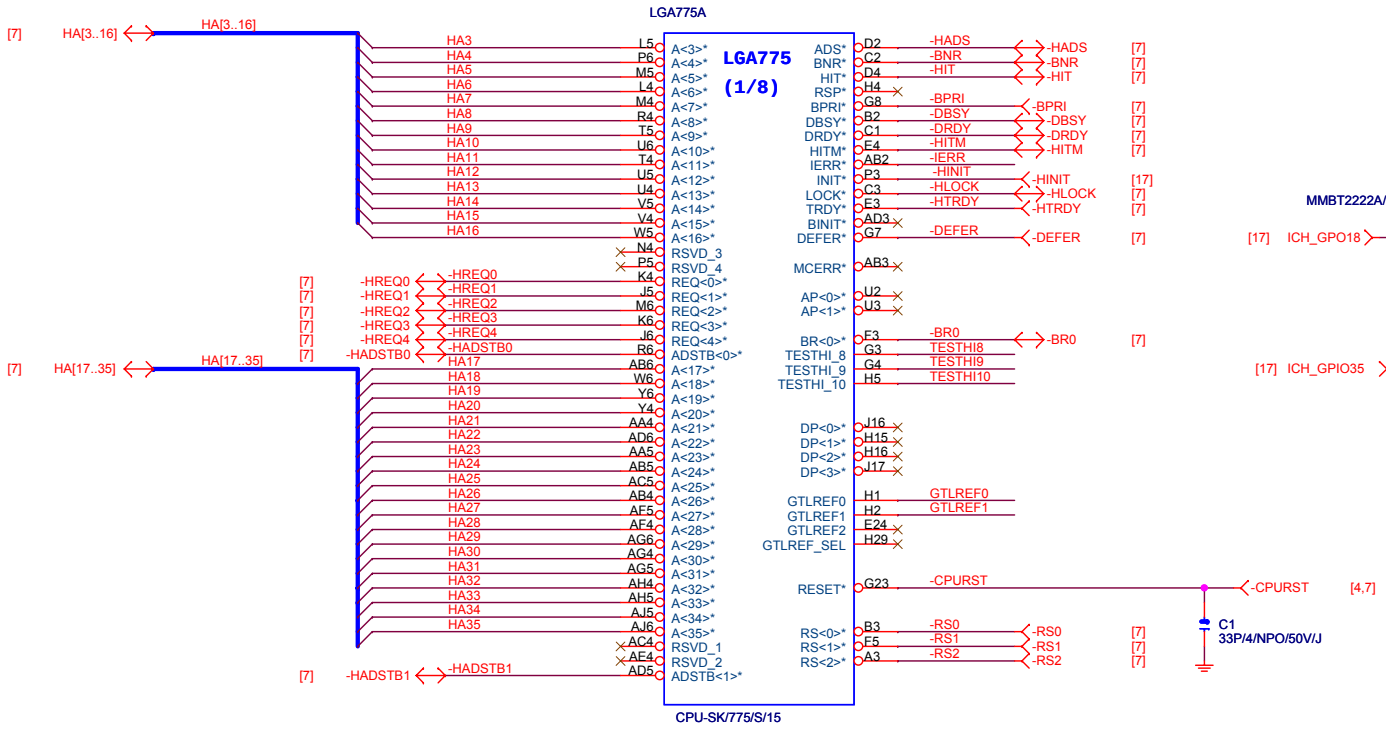
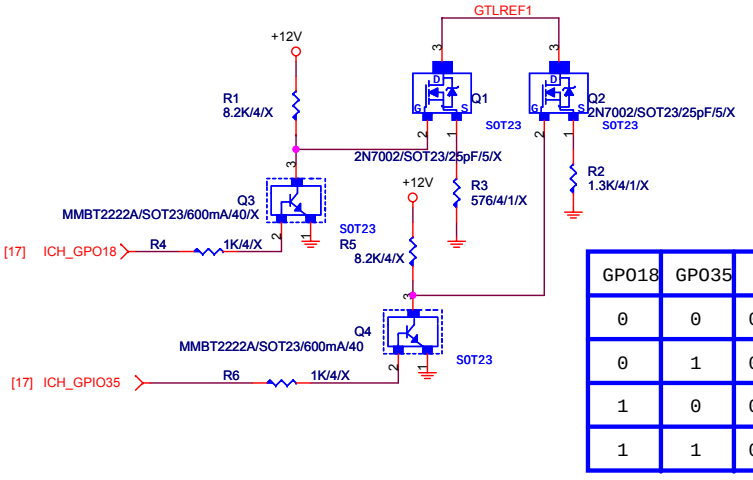
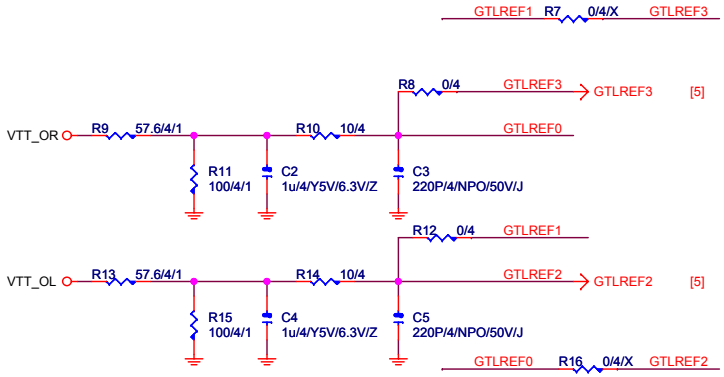
## LGA775-D:FOOTPRINT

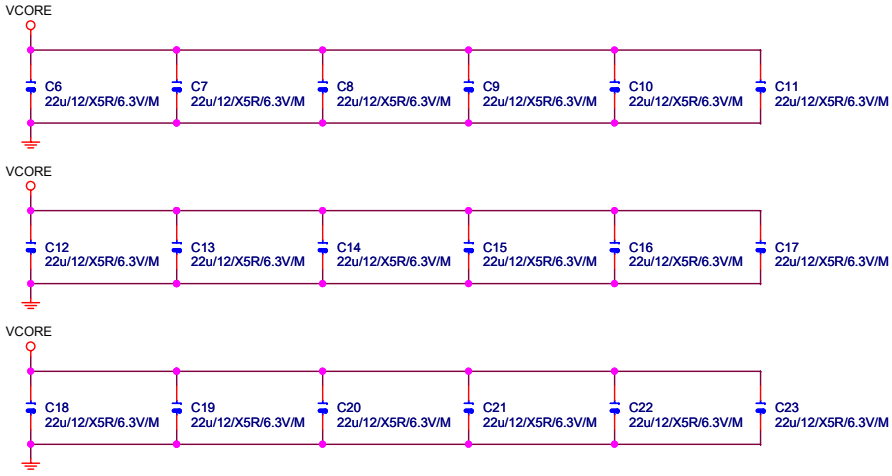


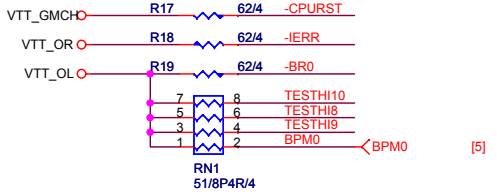




| GPO18 | GPO35 | |
|---|---|---|
| 0 | 0 | 0.615*VTT |
| 0 | 1 | 0.63*VTT |
| 1 | 0 | 0.65*VTT |
| 1 | 1 | 0.667*VTT |

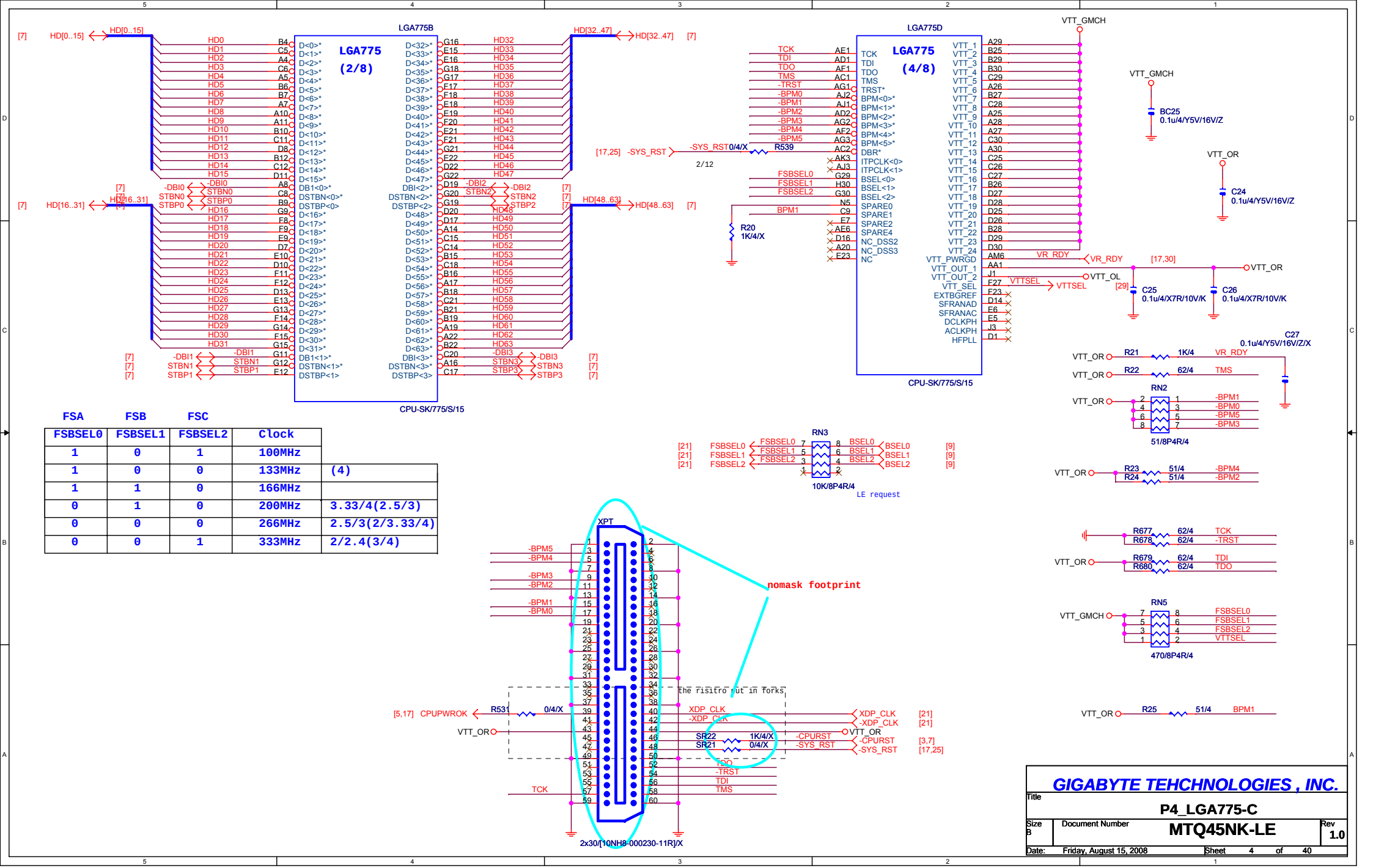
need remove GTLREF3&0 componet
R10 change to 50/4/1




| | | |
|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | |
| Title: P4_LGA775-A | | |
| Size: B | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 3 of 40 | |




| FSA | FSB | FSC | | |
|---|---|---|---|---|
| FSBSEL0 | FSBSEL1 | FSBSEL2 | Clock | |
| 1 | 0 | 1 | 100MHz | |
| 1 | 0 | 0 | 133MHz | (4) |
| 1 | 1 | 0 | 166MHz | |
| 0 | 1 | 0 | 200MHz | 3.33/4(2.5/3) |
| 0 | 0 | 0 | 266MHz | 2.5/3(2/3.33/4) |
| 0 | 0 | 1 | 333MHz | 2/2.4(3/4) |

| | |
|---|---|
| Title | P4_LGA775-C |
| Size B | Document Number MTQ45NK-LE |
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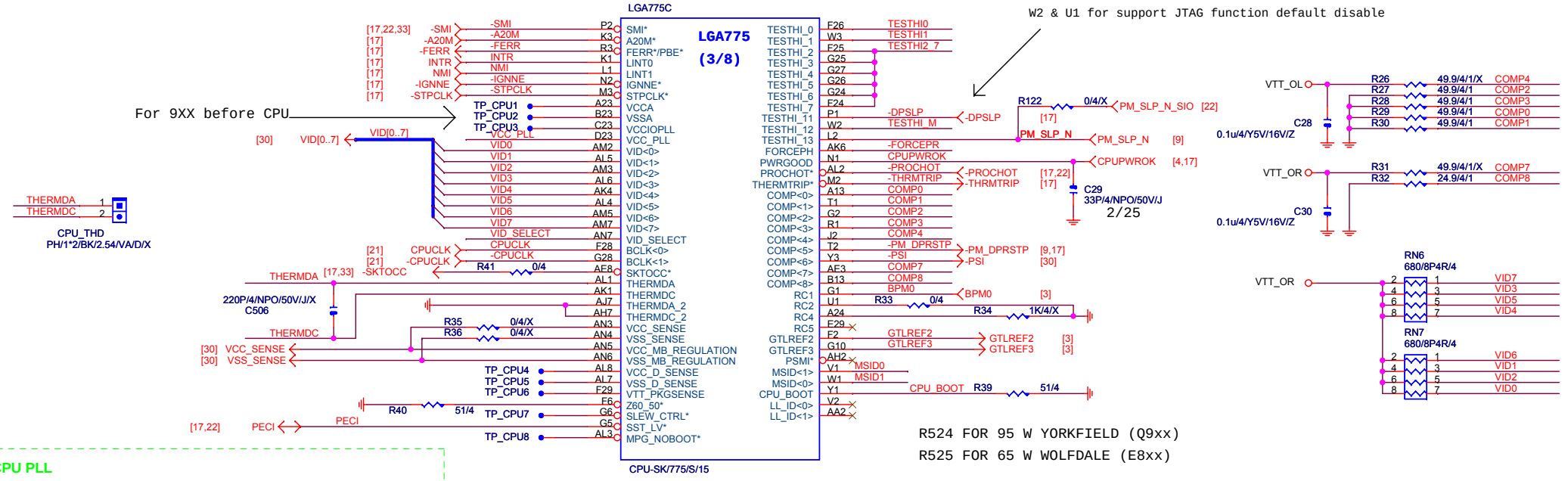


| | | | |
|---|---|---|---|
| VTT_OL | R45 | 49.9/4/1/X | -PM_DPRSTP |
| VTT_OR | R46 | 49.9/4/1 | -PSI |
| VTT_OR | R47 | 130/4/X | -FORCEPR |
| VTT_GMCH | R48 | 51/4 | TESTHI0 |
| VTT_GMCH | R51 | 51/4 | TESTHI2_7 |
| VTT_OL | R53 | 51/4/X | -DPSLP |
| VTT_OR | R55 | 130/4/X | -PROCHOT |
| VTT_OL | R56 | 51/4/X | PM_SLP_N |
| VTT_OL | R655 | 51/4 | TESTHI_M |
| VTT_OL | R656 | 51/4 | TESTHI1 |

| | | | |
|---|---|---|---|
| VTT_OR | R49 | 62/4 | -FERR |
| VTT_OR | R52 | 680/4 | VID_SELECT |
| VTT_OR | R54 | 62/4 | -THRMTRIP |

| | | | |
|---|---|---|---|
| VTT_OL | R26 | 49.9/4/1/X | COMP4 |
| | R27 | 49.9/4/1 | COMP2 |
| | R28 | 49.9/4/1 | COMP3 |
| | R29 | 49.9/4/1 | COMP0 |
| | R30 | 49.9/4/1 | COMP1 |
| VTT_OR | R31 | 49.9/4/1/X | COMP7 |
| | R32 | 24.9/4/1 | COMP8 |

| | | | |
|---|---|---|---|
| VTT_OR | 2 | 1 | VID7 |
| | 4 | 3 | VID3 |
| | 6 | 5 | VID5 |
| | 8 | 7 | VID4 |

| | | | |
|---|---|---|---|
| VTT_OR | 2 | 1 | VID6 |
| | 4 | 3 | VID1 |
| | 6 | 5 | VID2 |
| | 8 | 7 | VID0 |

| | | | |
|---|---|---|---|
| THERMDA | 1 | | |
| THERMDC | 2 | | |

| | | | |
|---|---|---|---|
| [17,22,33] | -SMI | P2 | SMI* |
| [17] | -A20M | K3 | A20M* |
| [17] | -FERR | R3 | FERR*/PBE* |
| [17] | INTR | K1 | LINT0 |
| [17] | NMI | L1 | LINT1 |
| [17] | -IGNNE | N2 | IGNNE* |
| [17] | -STPCLK | M3 | STPCLK* |
| | TP_CPU1 | A23 | VCCA |
| | TP_CPU2 | B23 | VSSA |
| | TP_CPU3 | C23 | VCCIOPLL |
| | VCC_PLL | D23 | VCC_PLL |
| [30] | VID[0..7] | AM2 | VID<0> |
| | VID1 | AL5 | VID<1> |
| | VID2 | AM3 | VID<2> |
| | VID3 | AL6 | VID<3> |
| | VID4 | AK4 | VID<4> |
| | VID5 | AL4 | VID<5> |
| | VID6 | AM5 | VID<6> |
| | VID7 | AM7 | VID<7> |
| | VID_SELECT | AN7 | VID_SELECT |
| [21] | CPUCLK | F28 | BCLK<0> |
| [21] | -CPUCLK | G28 | BCLK<1> |
| [17,33] | -SKTOCC | AE8 | SKTOCC* |
| THERMDA | | AL1 | THERMDA |
| THERMDC | | AK1 | THERMDC |
| | | AJ7 | THERMDA_2 |
| | | AH7 | THERMDC_2 |
| | | AN3 | VCC_SENSE |
| | | AN4 | VSS_SENSE |
| [30] | VCC_SENSE | AN5 | VCC_MB_REGULATION |
| [30] | VSS_SENSE | AN6 | VSS_MB_REGULATION |
| | TP_CPU4 | AL8 | VCC_D_SENSE |
| | TP_CPU5 | AL7 | VSS_D_SENSE |
| | TP_CPU6 | F29 | VTT_PKGSENSE |
| | | F6 | Z60_50* |
| | TP_CPU7 | G6 | SLEW_CTRL* |
| [17,22] | PECI | G5 | SST_LV* |
| | TP_CPU8 | AL3 | MPG_NOBOOT* |
| | | F26 | TESTHI_0 |
| | | W3 | TESTHI_1 |
| | | F25 | TESTHI_2 |
| | | G25 | TESTHI_3 |
| | | G27 | TESTHI_4 |
| | | G26 | TESTHI_5 |
| | | G24 | TESTHI_6 |
| | | F24 | TESTHI_7 |
| | | P1 | TESTHI_T1 |
| | | W2 | TESTHI_12 |
| | | L2 | TESTHI_13 |
| | | AK6 | FORCEPH |
| | | N1 | PWRGOOD |
| | | AL2 | PROCHOT* |
| | | M2 | THERMTRIP* |
| | | A13 | COMP<0> |
| | | T1 | COMP<1> |
| | | G2 | COMP<2> |
| | | R1 | COMP<3> |
| | | J2 | COMP<4> |
| | | T2 | COMP<5> |
| | | Y3 | COMP<6> |
| | | AE3 | COMP<7> |
| | | B13 | COMP<8> |
| | | G1 | RC1 |
| | | U1 | RC2 |
| | | A24 | RC4 |
| | | F29 | RC5 |
| | | F2 | GTLREF2 |
| | | G10 | GTLREF3 |
| | | AH2 | PSMI* |
| | | V1 | MSID<1> |
| | | W1 | MSID<0> |
| | | Y1 | CPU_BOOT |
| | | V2 | LL_ID<0> |
| | | AA2 | LL_ID<1> |

| | | | |
|---|---|---|---|
| | -DPSLP | P1 | -DPSLP |
| | TESTHI_M | W2 | |
| | PM_SLP_N | L2 | |
| | -FORCEPR | AK6 | |
| | CPUPWROK | N1 | |
| | -PROCHOT | AL2 | -PROCHOT [17,22] |
| | -THRMTRIP | M2 | -THRMTRIP [17] |
| | COMP0 | A13 | |
| | COMP1 | T1 | |
| | COMP2 | G2 | |
| | COMP3 | R1 | |
| | COMP4 | J2 | |
| | -PM_DPRSTP | T2 | -PM_DPRSTP [9,17] |
| | -PSI | Y3 | -PSI [30] |
| | COMP7 | AE3 | |
| | COMP8 | B13 | |
| | BPM0 | G1 | BPM0 [3] |
| | MSID0 | U1 | |
| | MSID1 | W1 | |
| | CPU_BOOT | Y1 | |
| | GTLREF2 | F2 | GTLREF2 [3] |
| | GTLREF3 | G10 | GTLREF3 [3] |

| | | | |
|---|---|---|---|
| R122 | 0/4/X | PM_SLP_N_SIO | [22] |
| | [17] | | |
| PM_SLP_N | | PM_SLP_N | [9] |
| R33 | 0/4 | | |
| R34 | 1K/4/X | | |
| R39 | 51/4 | | |
| R35 | 0/4/X | | |
| R36 | 0/4/X | | |
| R40 | 51/4 | | |
| R41 | 0/4 | | |

| | | | |
|---|---|---|---|
| MSID0 | R37 | 0/4/X | |
| MSID1 | R38 | 0/4/X | |

| | | | |
|---|---|---|---|
| [9,15,17,22] | PWROK1 | | |

| | | | |
|---|---|---|---|
| VTT_OR | R42 | 57.6/4/1/X | |
| | R43 | 10/4/X | GTLREF3 |
| | R44 | 100/4/1/X | |
| | C35 | 1u/4/Y5V/6.3V/Z/X | |
| | C36 | 220P/4/NPO/50V/J/X | |

| | | | |
|---|---|---|---|
| | C506 | 220P/4/NPO/50V/J/X | |
| THERMDA | | | |
| THERMDC | | | |

| | | | |
|---|---|---|---|
| | C28 | 0.1u/4/Y5V/16V/Z | |
| | C30 | 0.1u/4/Y5V/16V/Z | |

| | | | |
|---|---|---|---|
| | C29 | 33P/4/NPO/50V/J | |
| | C37 | 220P/4/NPO/50V/J | |

| | | | |
|---|---|---|---|
| | C32 | 4.7U/8/Y5V/10V/Z/X | |
| | C33 | 4.7U/8/Y5V/10V/Z | |
| | C34 | 0.1u/4/Y5V/16V/Z | |

| | | | |
|---|---|---|---|
| | RN6 | 680/8P4R/4 | |
| | RN7 | 680/8P4R/4 | |

| | | | |
|---|---|---|---|
| | R404 | 680/4 | |
| VTT_PWRGD | | | [30] |
| | R406 | 1K/4/X | |
| | Q55 | MMBT2222A/SOT23/600mA/40/X | |
| | | SOT23 | |
| | R50 | 100/4/X | |
| CPUPWROK | | | |
| | Q5 | MMBT2222A/SOT23/600mA/40/X | |
| | | SOT23 | |
| | R57 | 8.2K/4/X | |

| | | | |
|---|---|---|---|
| | R524 | FOR 95 W YORKFIELD (Q9xx) | |
| | R525 | FOR 65 W WOLFDALE (E8xx) | |

| | | | |
|---|---|---|---|
| | TRY ON 0.1 AND CAN BE POWER ON ? | | |

| | | | |
|---|---|---|---|
| | CPU PLL | | |
| | FB19 | 600/6/200mA/S | |
| VCC1_5 | | | |
| | VCC_PLL | | |
| | C32 | 4.7U/8/Y5V/10V/Z/X | |
| | C33 | 4.7U/8/Y5V/10V/Z | |
| | C34 | 0.1u/4/Y5V/16V/Z | |

| | | | |
|---|---|---|---|
| | VTT_PWRGD | | |
| | R404 | 680/4 | |
| | R406 | 1K/4/X | |
| | Q55 | MMBT2222A/SOT23/600mA/40/X | |
| | | SOT23 | |
| | R50 | 100/4/X | |
| CPUPWROK | | | |
| | Q5 | MMBT2222A/SOT23/600mA/40/X | |
| | | SOT23 | |
| | R57 | 8.2K/4/X | |

| | | | |
|---|---|---|---|
| | TRY ON 0.1 AND CAN BE POWER ON ? | | |

| | | | |
|---|---|---|---|
| | GIGABYTE TEHCHNOLOGIES , INC. | | |
| Title | P4_LGA775-B | | |
| Size B | Document Number | MTQ45NK-LE | Rev 1.0 |
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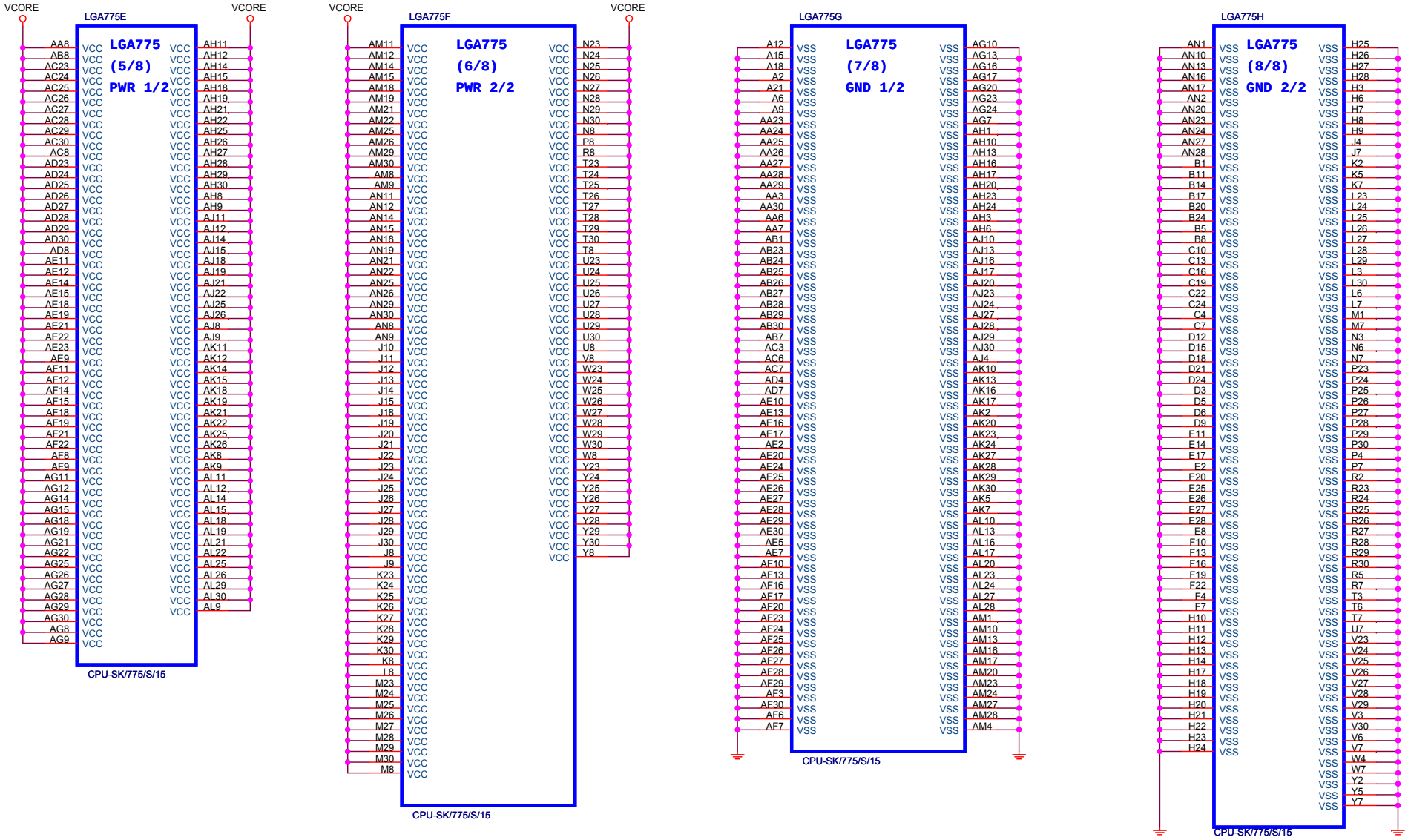
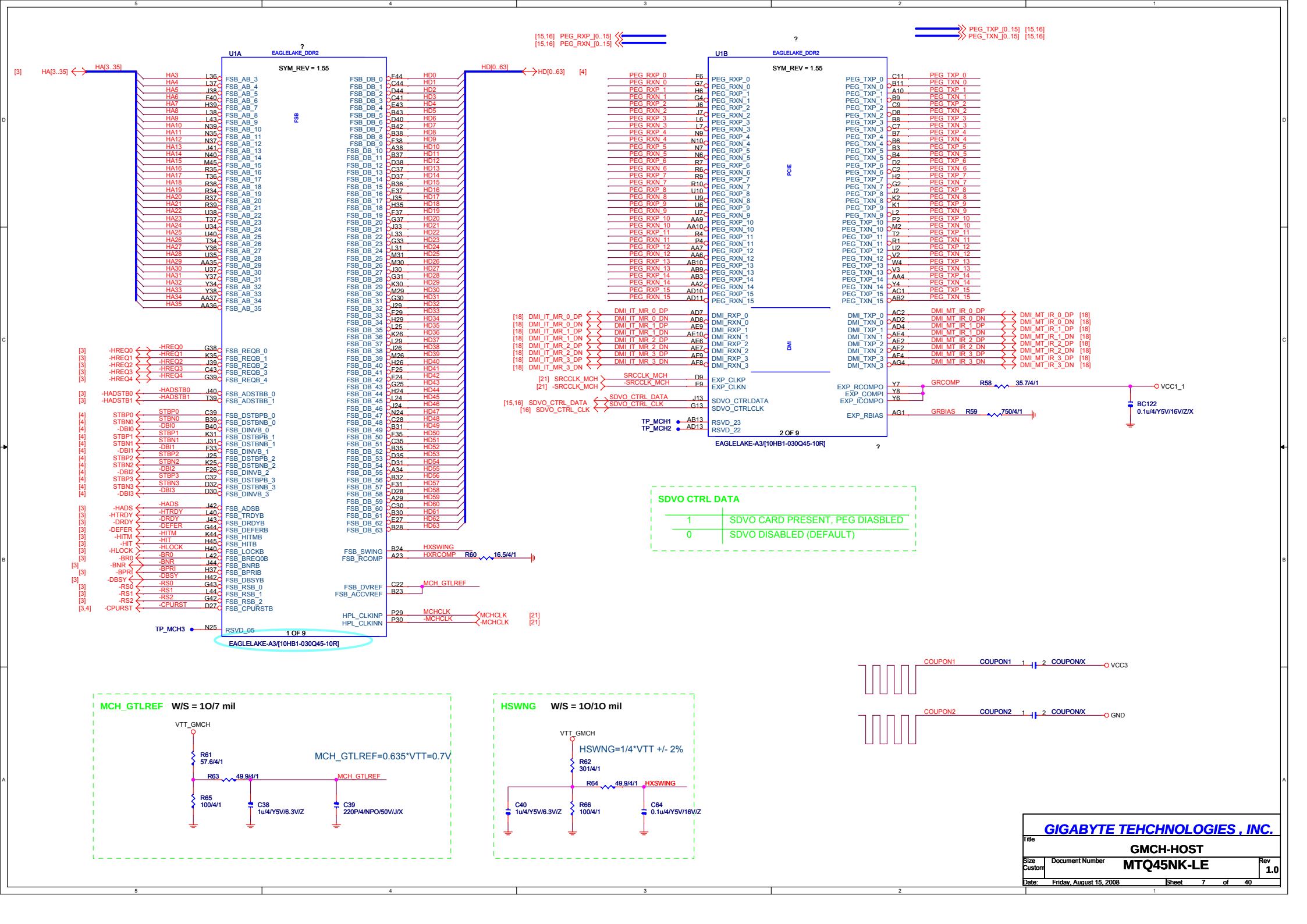



**GIGABYTE TEHCHNOLOGIES , INC.**

| | | |
|---|---|---|
| Title | P4_LGA775-D | |
| Size B | Document Number MTQ45NK-LE | Rev 1.0 |
| Date: Friday, August 15, 2008 | Sheet 6 of 40 | |


U1A
EAGLELAKE_DDR2
SYM_REV = 1.55
FSB
1 OF 9
EAGLELAKE-A3/[10HB1-030Q45-10R]
U1B
EAGLELAKE_DDR2
SYM_REV = 1.55
PCIE
DMI
2 OF 9
EAGLELAKE-A3/[10HB1-030Q45-10R]
SDVO CTRL DATA
1 SDVO CARD PRESENT, PEG DIASBLED
0 SDVO DISABLED (DEFAULT)
MCH_GTLREF W/S = 1O/7 mil
VTT_GMCH
R61 57.6/4/1
R63 49.9/4/1
R65 100/4/1
C38 1u/4/Y5V/6.3V/Z
C39 220P/4/NPO/50V/J/X
MCH_GTLREF=0.635*VTT=0.7V
HSWNG W/S = 1O/1O mil
VTT_GMCH
HSWNG=1/4*VTT +/- 2%
R62 301/4/1
R64 49.9/4/1
R66 100/4/1
C40 1u/4/Y5V/6.3V/Z
C64 0.1u/4/Y5V/16V/Z/X
R60 16.5/4/1
R58 35.7/4/1
R59 750/4/1
BC122 0.1u/4/Y5V/16V/Z/X
COUPON1
COUPON2
VCC3
GND
GIGABYTE TEHCHNOLOGIES , INC.
Title
GMCH-HOST
Size Custom
Document Number MTQ45NK-LE
Rev 1.0
Date: Friday, August 15, 2008
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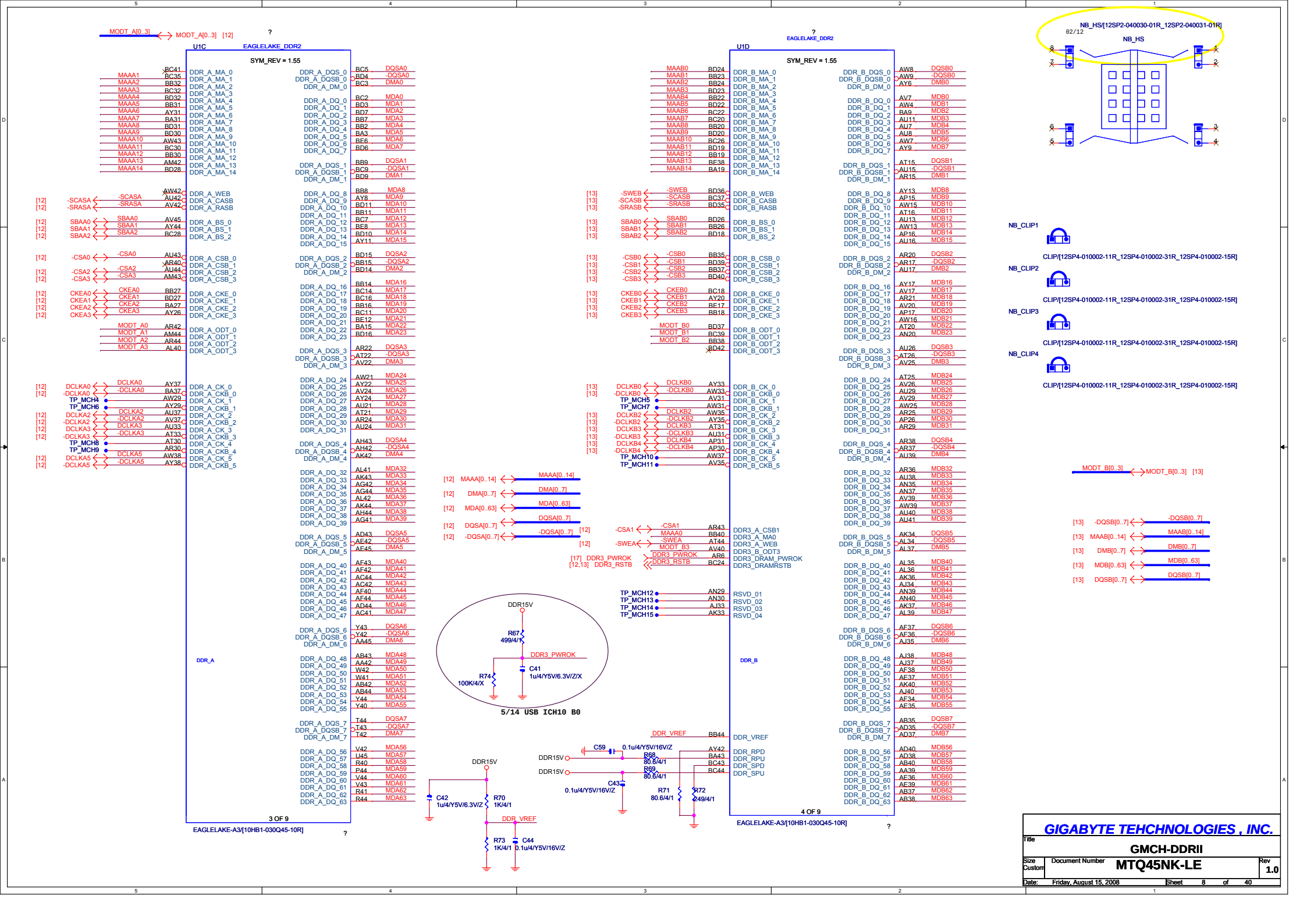
MODT_A[0..3]
MODT_A[0..3] [12]
U1C
EAGLELAKE_DDR2
SYM_REV = 1.55
3 OF 9
EAGLELAKE-A3/[10HB1-030Q45-10R]
U1D
EAGLELAKE_DDR2
SYM_REV = 1.55
4 OF 9
EAGLELAKE-A3/[10HB1-030Q45-10R]
DDR_A
DDR_B
NB_HS/[12SP2-040030-01R_12SP2-040031-01R]
02/12
NB_HS
NB_CLIP1
CLIP/[12SP4-010002-11R_12SP4-010002-31R_12SP4-010002-15R]
NB_CLIP2
CLIP/[12SP4-010002-11R_12SP4-010002-31R_12SP4-010002-15R]
NB_CLIP3
CLIP/[12SP4-010002-11R_12SP4-010002-31R_12SP4-010002-15R]
NB_CLIP4
CLIP/[12SP4-010002-11R_12SP4-010002-31R_12SP4-010002-15R]
MODT_B[0..3]
MODT_B[0..3] [13]
[13] -DQSB[0..7]
-DQSB[0..7]
[13] MAAB[0..14]
MAAB[0..14]
[13] DMB[0..7]
DMB[0..7]
[13] MDB[0..63]
MDB[0..63]
[13] DQSB[0..7]
DQSB[0..7]
[12] MAAA[0..14]
MAAA[0..14]
[12] DMA[0..7]
DMA[0..7]
[12] MDA[0..63]
MDA[0..63]
[12] DQSA[0..7]
DQSA[0..7]
[12] -DQSA[0..7]
-DQSA[0..7] [12]
DDR15V
R67 499/4/1
DDR3_PWROK
C41 1u/4/Y5V/6.3V/Z/X
R74 100K/4/X
5/14 USB ICH10 B0
DDR_VREF
C59 0.1u/4/Y5V/16V/Z
R68 80.6/4/1
R69 80.6/4/1
C43 0.1u/4/Y5V/16V/Z
R71 80.6/4/1
R72 249/4/1
C42 1u/4/Y5V/6.3V/Z
R70 1K/4/1
R73 1K/4/1
C44 0.1u/4/Y5V/16V/Z
GIGABYTE TEHCHNOLOGIES , INC.
Title
GMCH-DDRII
Size Custom
Document Number
MTQ45NK-LE
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Sheet 8 of 40

RSVD_36 L=EXTERNAL GRAPHIC H=INTERNAL GRAPHIC

| INTERNAL TMP | R116 |
|---|---|
| ENABLE | STUFF |
| DISABLE | NO-STUFF |

U1E EAGLELAKE_DDR2 SYM_REV = 1.55

EAGLELAKE-A3/[10HB1-030Q45-10R] 5 OF 9

5 mils trace

8/5 for water-wave

5/5 for measure

## CLINK PWROK GENERATION

check intel R88 1K is OK?

SUPPORT HDMI STUFF R107 & RN10

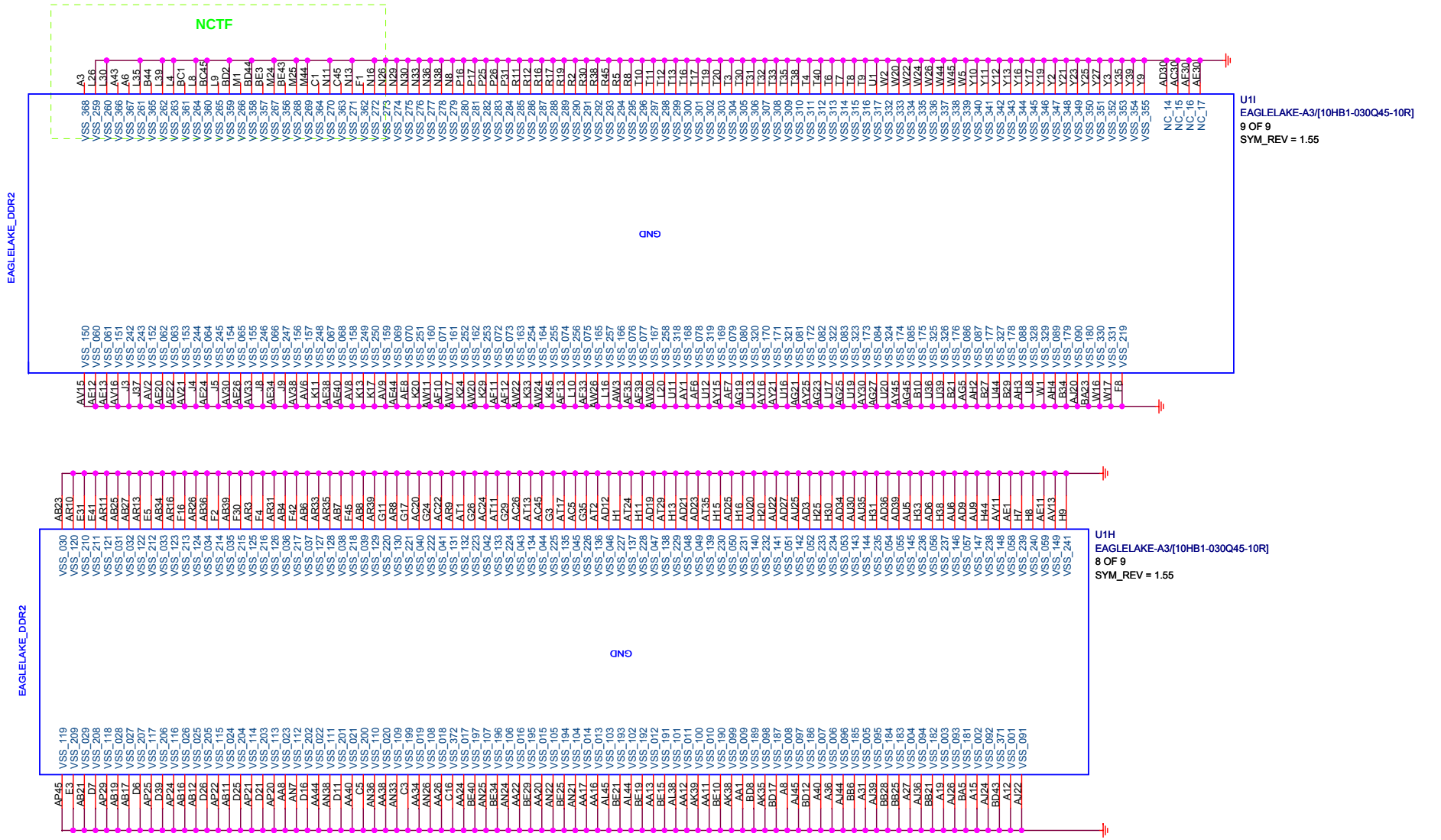
STUFF IT IF NO SUPPORT HDMI & DP

## GMCH STRAP

| PIN | 1 | 0 | DESCRIPTION |
|---|---|---|---|
| TCEN | ENABLE(Default) | DISABLE | TLS CONFIDENTIALITY support AMT need enable |
| EXP_SLR | NORM(Default) | REVERSE | PCIE LANE REVERSAL |
| EXP_SM | CONCURRENT (Default) | NON-CONCURRENT | PCI-E / SDVO CO-EXISTENCE |

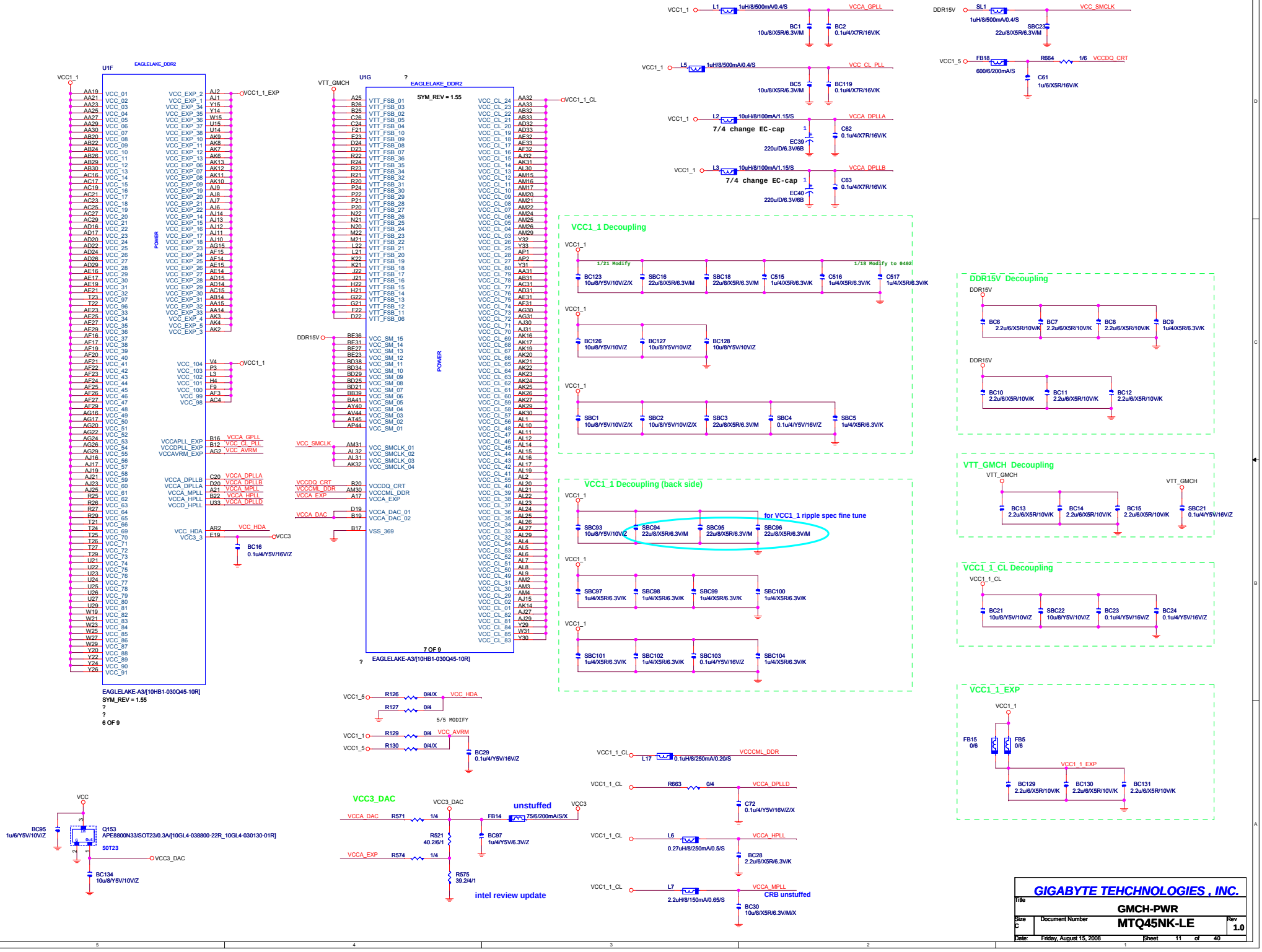
VGA+COM/BLUE/GF/RA/D/[11NR6-904009-41R_11NR6-904009-22R]

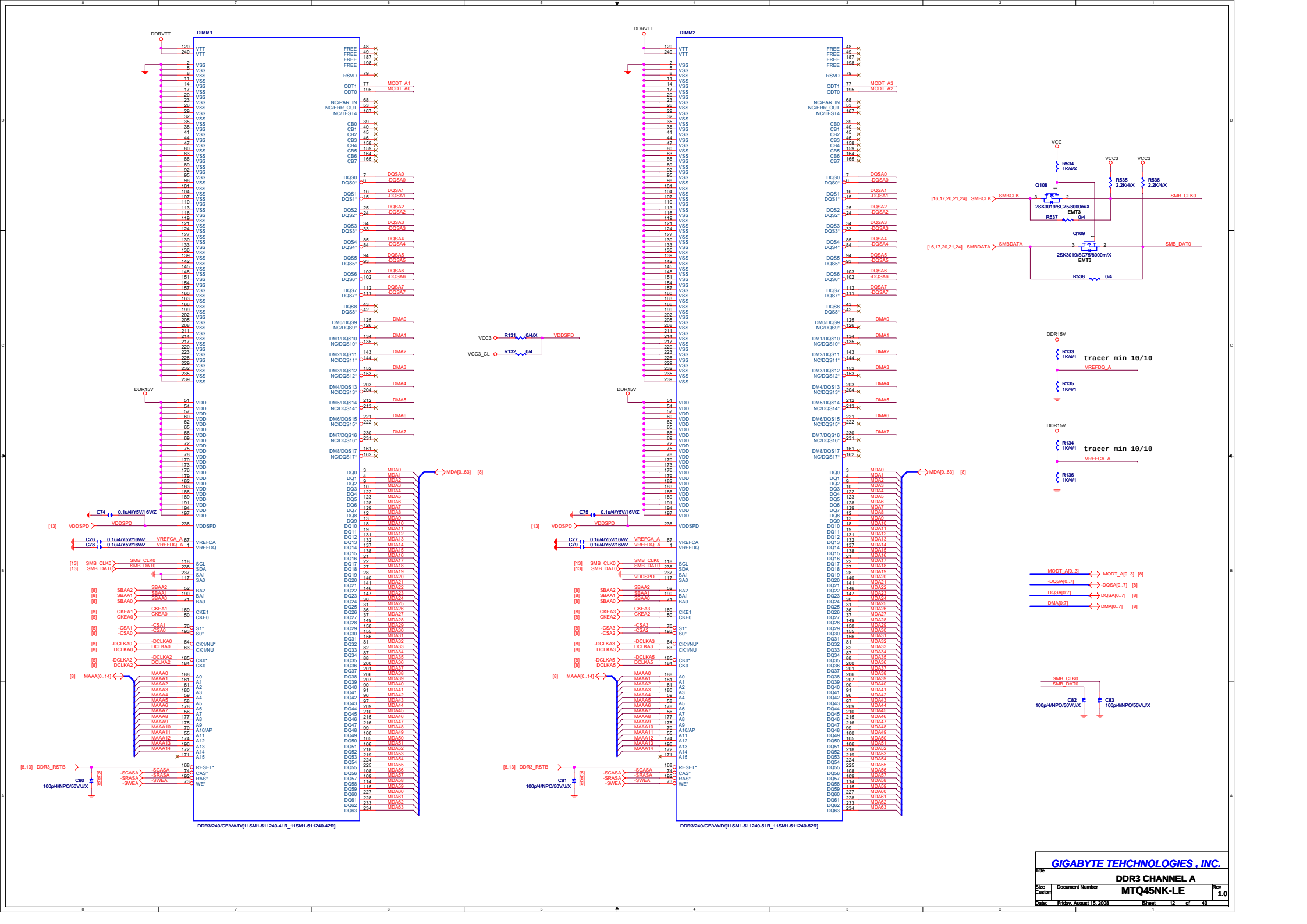
| GIGABYTE TEHCHNOLOGIES , INC. | | |
|---|---|---|
| Title: GMCH-INTERNAL VGA | | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Tuesday, August 19, 2008 | Sheet 9 of 40 | |



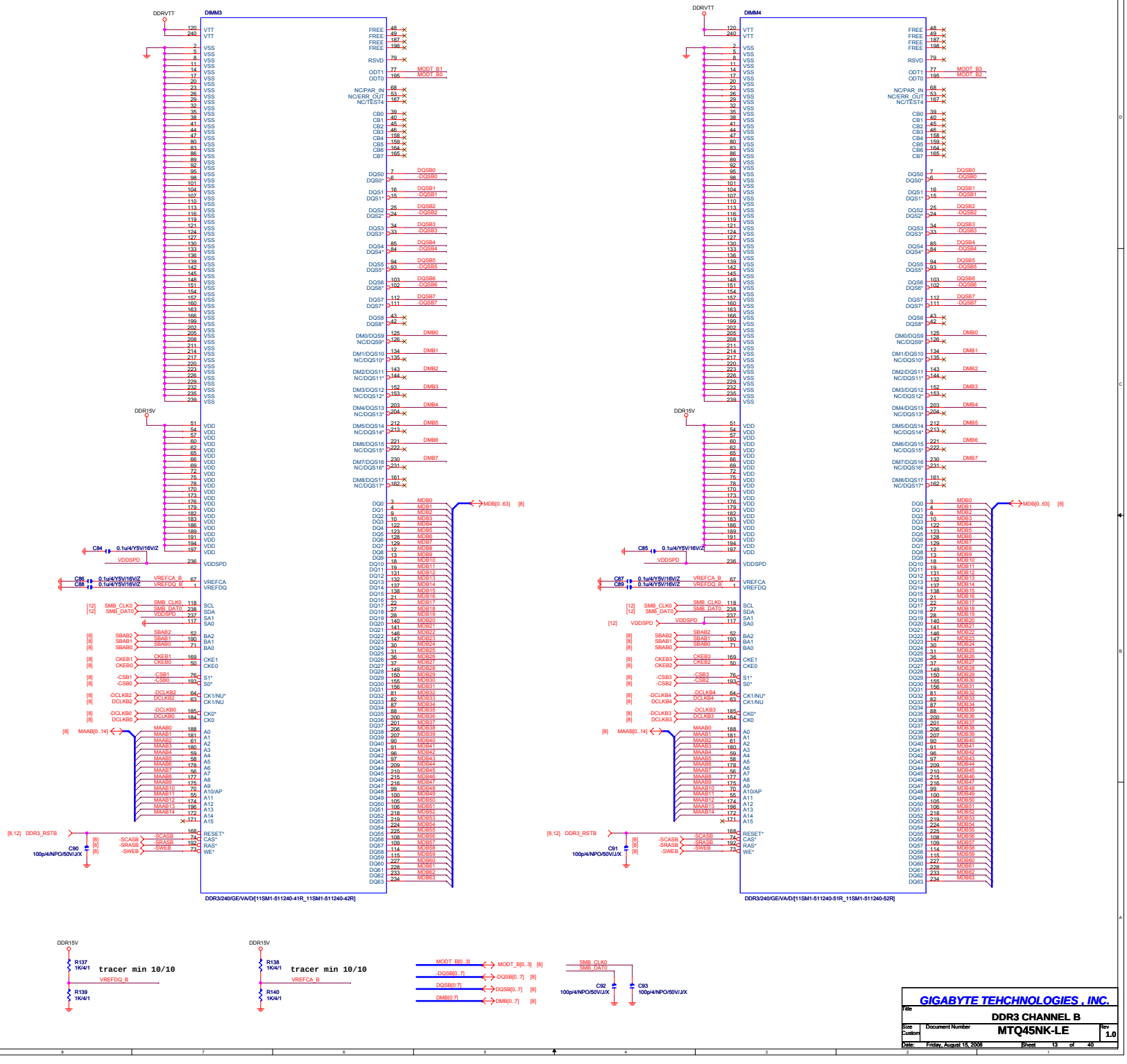

**GIGABYTE TEHCHNOLOGIES , INC.**

| | | |
|---|---|---|
| Title | GMCH-GND | |
| Size B | Document Number MTQ45NK-LE | Rev 1.0 |
| Date: Friday, August 15, 2008 | Sheet 10 of 40 | |


U1F
EAGLELAKE_DDR2
EAGLELAKE-A3/[10HB1-030Q45-10R]
SYM_REV = 1.55
6 OF 9
U1G
SYM_REV = 1.55
7 OF 9
EAGLELAKE-A3/[10HB1-030Q45-10R]
VCC1_1 Decoupling
VCC1_1 Decoupling (back side)
for VCC1_1 ripple spec fine tune
DDR15V Decoupling
VTT_GMCH Decoupling
VCC1_1_CL Decoupling
VCC1_1_EXP
GIGABYTE TEHCHNOLOGIES , INC.
GMCH-PWR
MTQ45NK-LE
1.0
Friday, August 15, 2008




| | |
|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | |
| Title | DDR3 CHANNEL A |
| Size: Custom | Document Number: MTQ45NK-LE |
| Rev: 1.0 | |
| Date: Friday, August 15, 2008 | Sheet 12 of 40 |




| | |
|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | |
| Title | DDR3 CHANNEL B |
| Size: Custom | Document Number: MTQ45NK-LE |
| Rev: 1.0 | |
| Date: Friday, August 15, 2008 | Sheet 13 of 40 |

DDRVTT

EC1 1000U/D/6.3V/8C/36m/X

## CHANNEL A

DDR15V

EC3 1000u/D/6.3V/8C/36m

DDR15V Decoupling

DDR15V

BC31 1u/4/Y5V/6.3V/Z
BC32 1u/4/Y5V/6.3V/Z
BC33 1u/4/Y5V/6.3V/Z
BC34 1u/4/Y5V/6.3V/Z

DDR15V

BC35 1u/4/Y5V/6.3V/Z
BC36 1u/4/Y5V/6.3V/Z
BC37 1u/4/Y5V/6.3V/Z
BC38 1u/4/Y5V/6.3V/Z

DDRVTT Decouple

DDRVTT

BC40 4.7U/8/Y5V/10V/Z
C95 1u/4/Y5V/6.3V/Z
C97 0.1u/4/Y5V/16V/Z/X

## CHANNEL B

DDR15V

EC2 1000u/D/6.3V/8C/36m
EC4 1000u/D/6.3V/8C/36m

DDRVTT Decouple

DDRVTT

BC39 4.7U/8/Y5V/10V/Z
C94 1u/4/Y5V/6.3V/Z
C96 0.1u/4/Y5V/16V/Z/X

GIGABYTE TEHCHNOLOGIES , INC.

| | | |
|---|---|---|
| Title | DDR3 TERMINATOR | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 14 of 40 | |

# Display Port

## Port C

| Strap | DDPC_CTRLDATA |
|---|---|
| PCI Express | Display Port |
| PEG_TXP_8 | DPC_LANE3 |
| PEG_TXN_8 | DPC_LANE3# |
| PEG_TXP_9 | DPC_LANE2 |
| PEG_TXN_9 | DPC_LANE2# |
| PEG_TXP_10 | DPC_LANE1 |
| PEG_TXN_10 | DPC_LANE1# |
| PEG_TXP_11 | DPC_LANE0 |
| PEG_TXN_11 | DPC_LANE0# |
| PEG_RXP_8 | DPC_HPD |
| PEG_RXN_8 | |
| PEG_RXP_9 | DPC_AUX |
| PEG_RXN_9 | DPC_AUX# |

FOR BTX Lanes REVERSAL

U33 PI3PCIE2612-AZFE/QFN56/[10TA1-082612-10R]

SEL Mode

| | |
|---|---|
| SEL=1 | DP |
| SEL=0 | PCIE |

SWAP

SWAP

3/6 fix hot pug issue

2/18

reversed for EMI

only for DP

2/18

Support DP to HDMI Dongle

L=0 channel0
L=1 channel1

L=ENABLE
H=DISABLE

PI5C3257/QSOP16/[10TA1-083257-22R_10TA1-083257-21R_10TA1-081002-A0R]

MINISMDC075F/S

DP_CON DISPLAY/20P/BK/RA/D/G30u

AZ1045

AZ1045

EMI

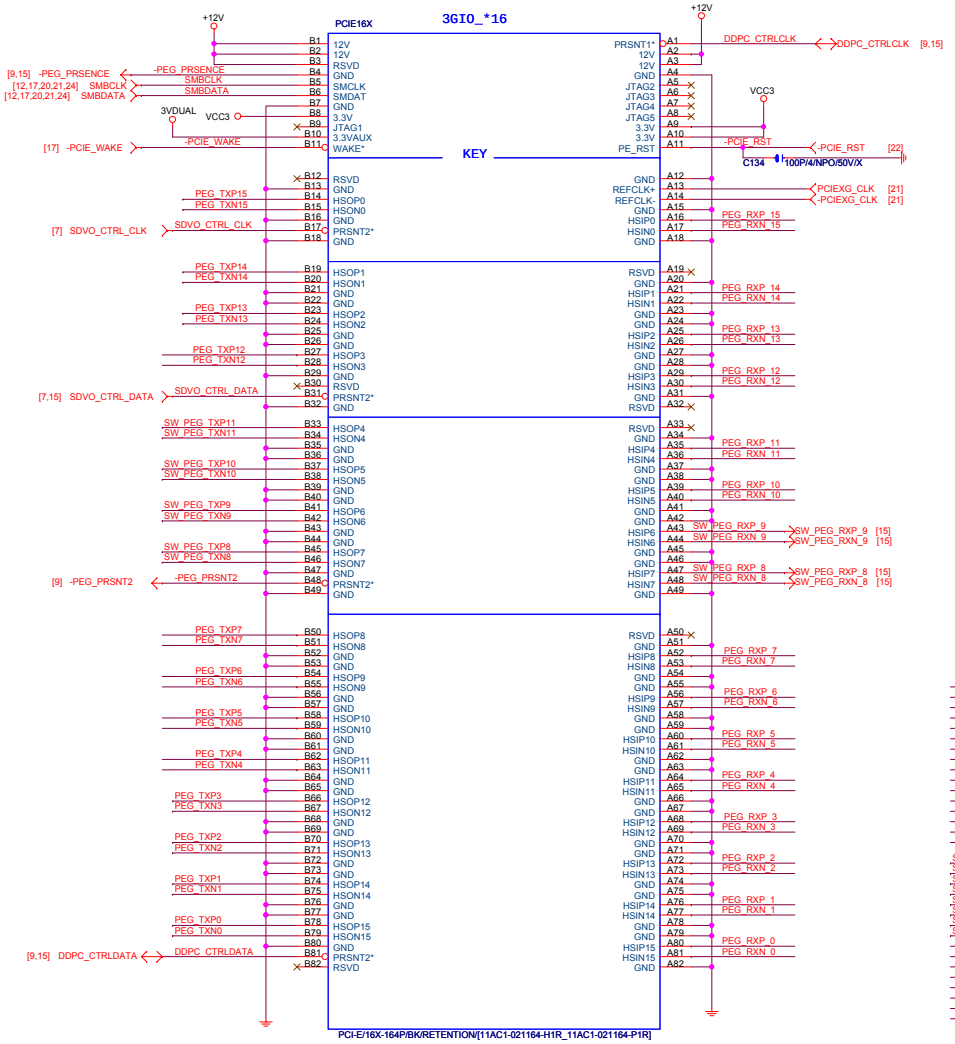
AZ1045

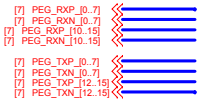
FIX PCIe X 16 issue

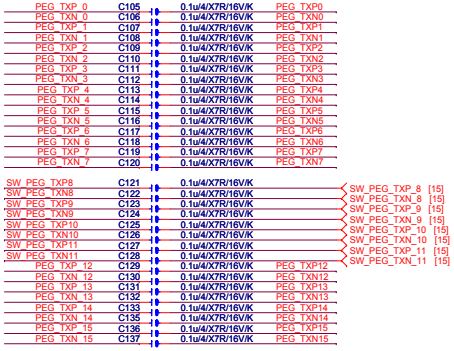
| | |
|---|---|
| Title | SWITCH & DVI/HDMI/DP |
| Size: Custom | Document Number: MTQ45NK-LE |
| Rev | 1.0 |
| Date: | Friday, August 15, 2008 |
| Sheet | 15 of 40 |

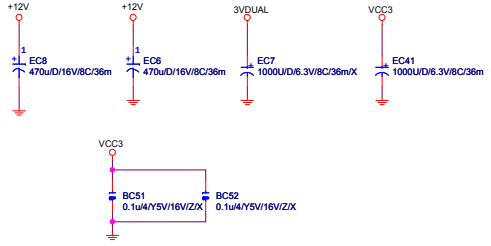
GIGABYTE TEHCHNOLOGIES , INC.

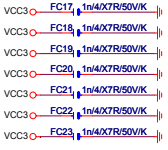
# FOR BTX Lanes REVERSAL

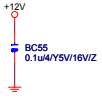


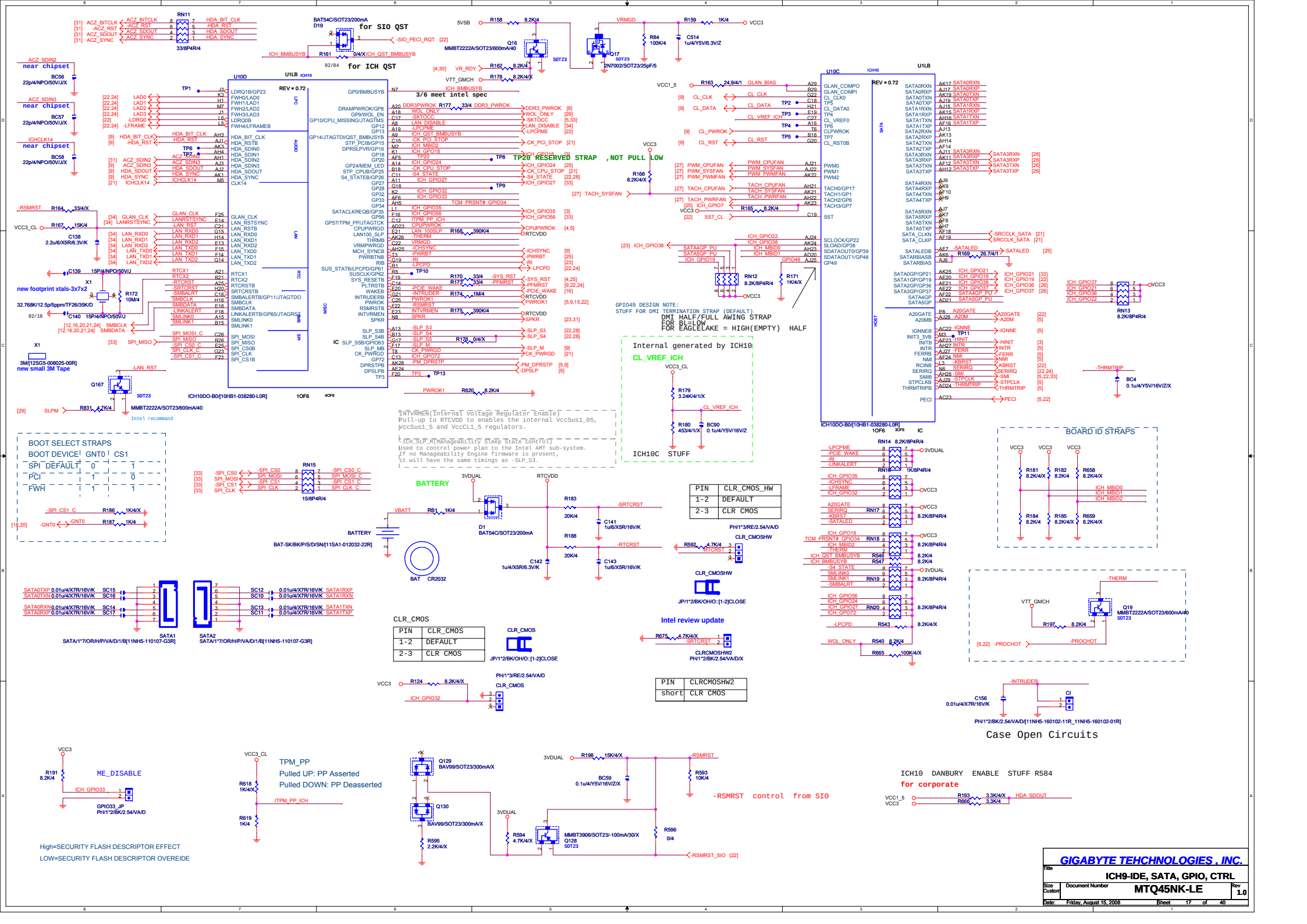


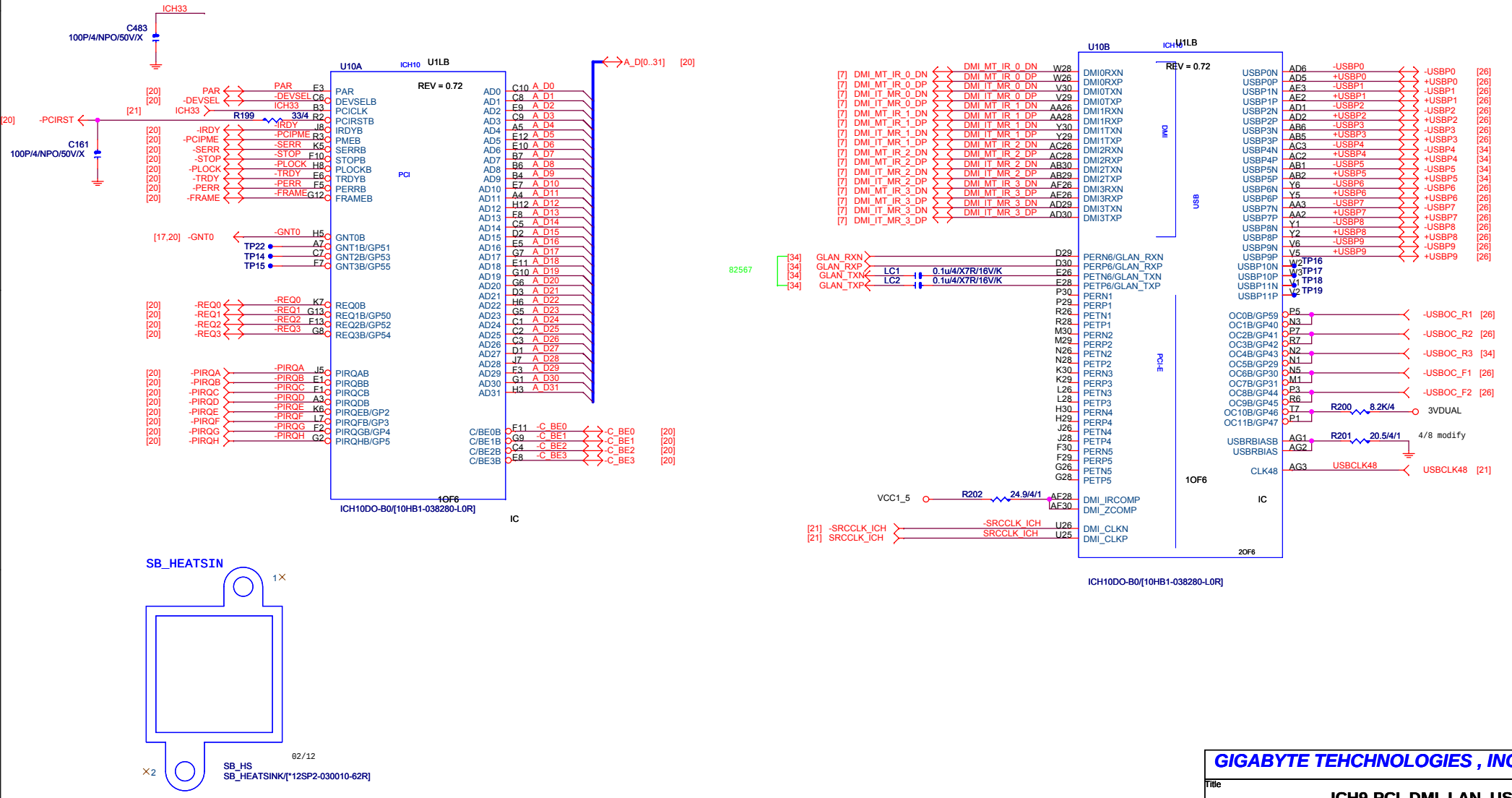




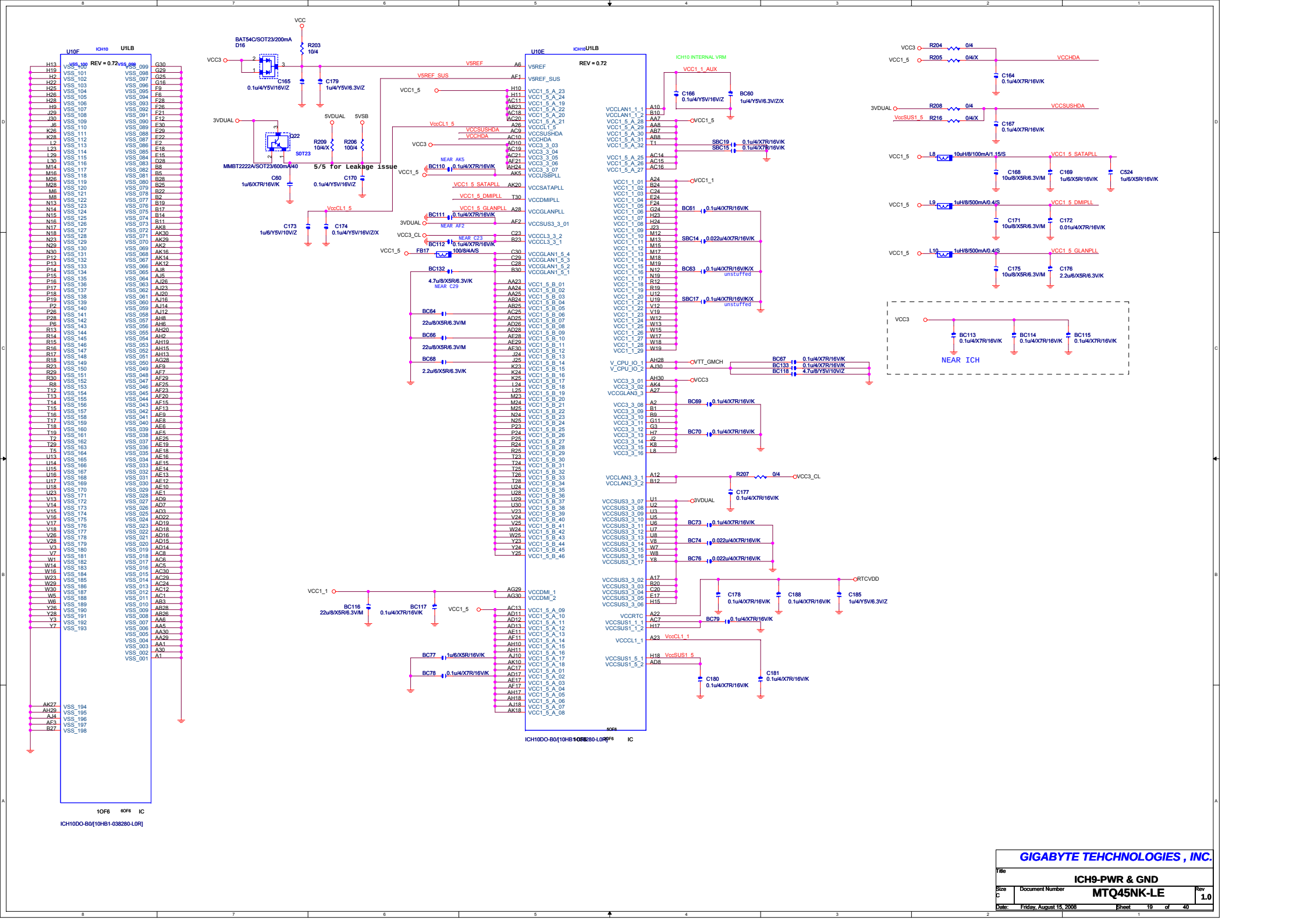


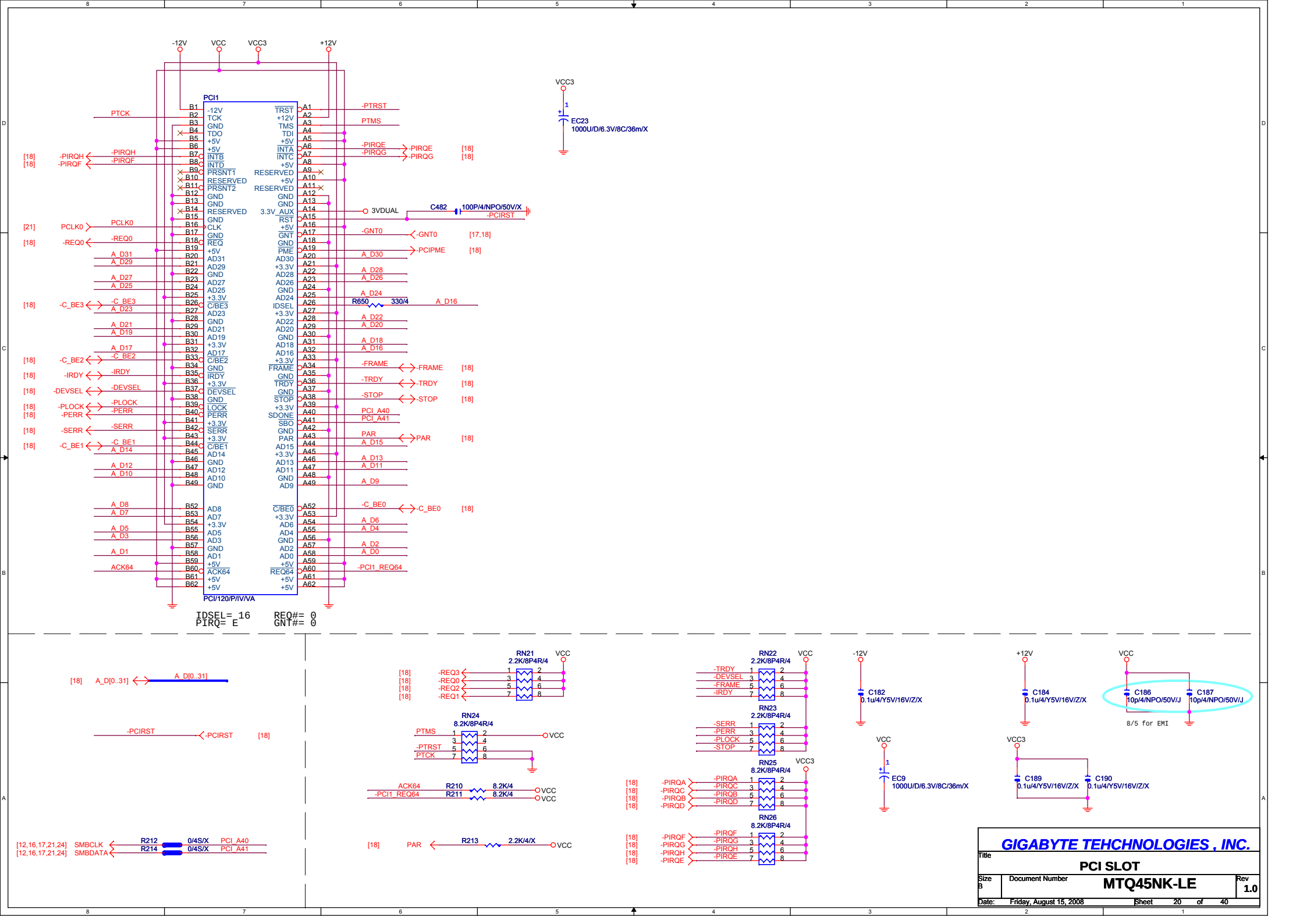
| | |
|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | |
| Title | PCI EXPRESS * 16_A |
| Size C | Document Number MTQ45NK-LE |
| Rev | 1.0 |
| Date: Friday, August 15, 2008 | Sheet 16 of 40 |

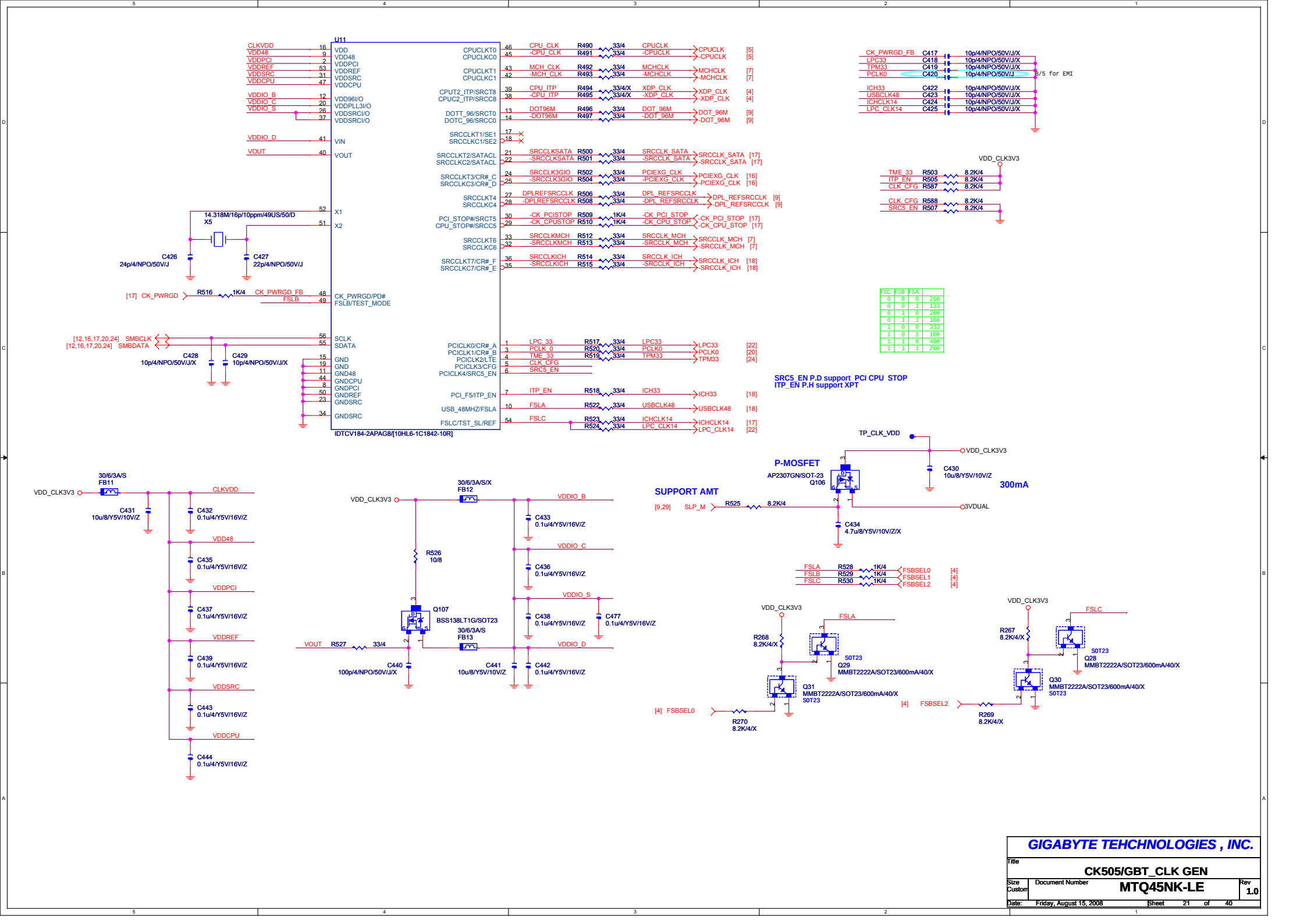

for SIO QST
for ICH QST
3/6 meet intel spec
TP20 RESERVED STRAP ,NOT PULL LOW
Internal generated by ICH10
CL_VREF_ICH
ICH10C STUFF
GPIO49 DESIGN NOTE:
STUFF FOR DMI TERMINATION STRAP (DEFAULT)
DMI HALF/FULL AWING STRAP
FOR BL=LOW
FOR EAGLELAKE = HIGH(EMPTY) HALF
BOOT SELECT STRAPS
BOOT DEVICE GNT0 CS1
SPI DEFAULT 0 1
PCI 1 0
FWH 1 1
BATTERY
BOARD ID STRAPS
Intel review update
CLR_CMOS
PIN CLR_CMOS
1-2 DEFAULT
2-3 CLR CMOS
PIN CLR_CMOS_HW
1-2 DEFAULT
2-3 CLR CMOS
PIN CLRCMOSHW2
short CLR CMOS
ME_DISABLE
TPM_PP
Pulled UP: PP Asserted
Pulled DOWN: PP Deasserted
High=SECURITY FLASH DESCRIPTOR EFFECT
LOW=SECURITY FLASH DESCRIPTOR OVEREIDE
-RSMRST control from SIO
ICH10 DANBURY ENABLE STUFF R584
for corporate
Case Open Circuits
GIGABYTE TEHCHNOLOGIES , INC.
ICH9-IDE, SATA, GPIO, CTRL
MTQ45NK-LE
Rev 1.0
Friday, August 15, 2008
Sheet 17 of 40



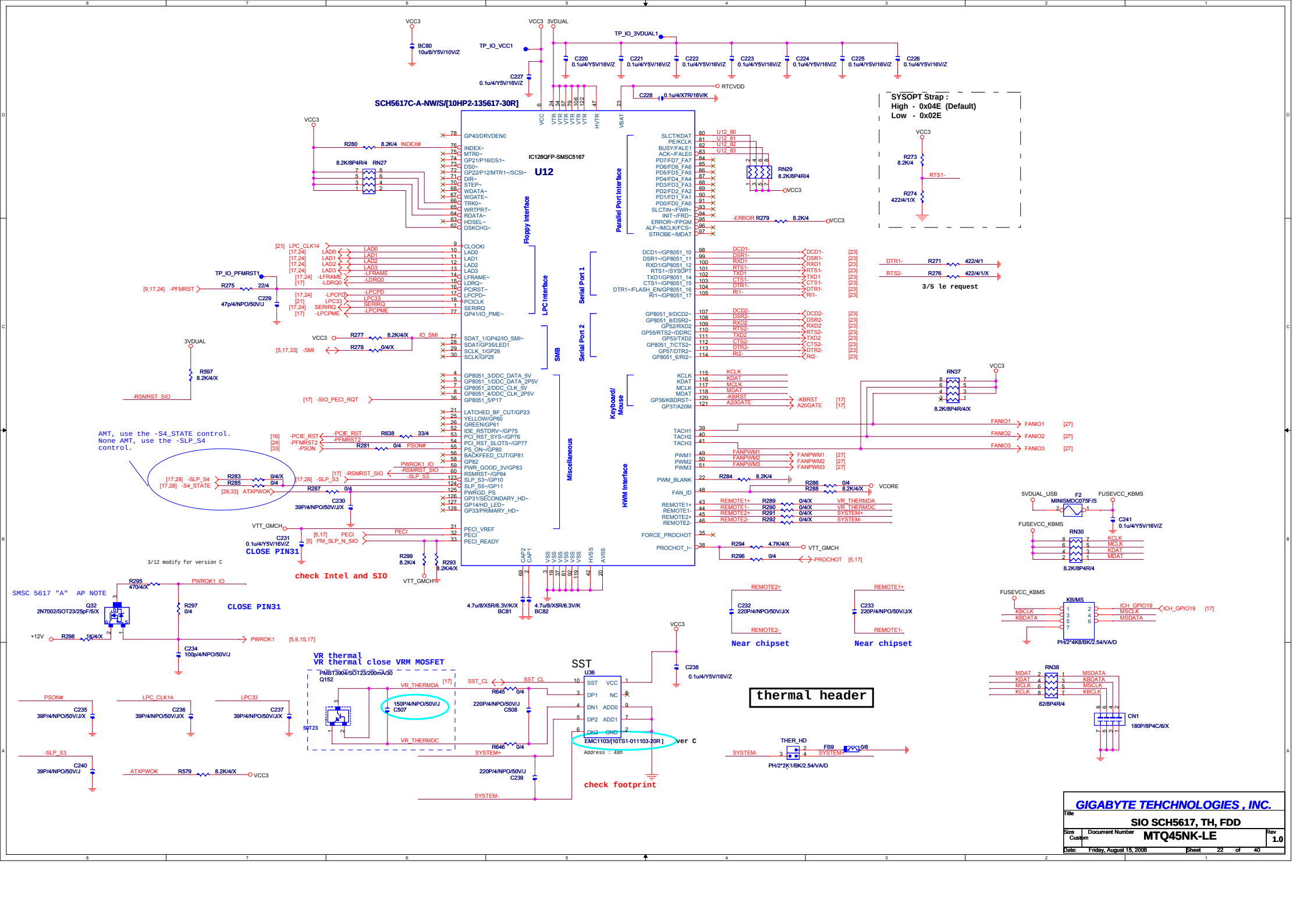

| | | |
|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | |
| Title: ICH9-PCI, DMI, LAN, USB | | |
| Size: B | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 18 of 40 | |


U10F
ICH10
U1LB
REV = 0.72
1OF6
6OF6
IC
ICH10DO-B0/[10HB1-038280-L0R]
U10E
ICH10U1LB
REV = 0.72
ICH10 INTERNAL VRM
ICH10DO-B0/[10HB1-038280-L0R]
1OF6
6OF6
IC
BAT54C/SOT23/200mA
D16
R203
10/4
C165
0.1u/4/Y5V/16V/Z
C179
1u/4/Y5V/6.3V/Z
3VDUAL
5VDUAL
5VSB
Q22
SOT23
MMBT2222A/SOT23/600mA/40
R209
10/4/X
R206
100/4
5/5 for Leakage issue
C60
1u/6/X7R/16V/K
C170
0.1u/4/Y5V/16V/Z
C173
1u/6/Y5V/10V/Z
C174
0.1u/4/Y5V/16V/Z/X
V5REF
V5REF_SUS
VccCL1_5
VCCSUSHDA
VCCHDA
VCC1_5_SATAPLL
VCC1_5_DMIPLL
VCC1_5_GLANPLL
NEAR AK5
NEAR AF2
NEAR C23
NEAR C29
BC110
BC111
BC112
FB17
100/8/4A/S
BC132
4.7u/8/X5R/6.3V/K
BC64
22u/8/X5R/6.3V/M
BC66
22u/8/X5R/6.3V/M
BC68
2.2u/6/X5R/6.3V/K
VCC1_1_AUX
C166
0.1u/4/Y5V/16V/Z
BC60
1u/4/Y5V/6.3V/Z/X
SBC19
SBC15
0.1u/4/X7R/16V/K
BC61
SBC14
0.022u/4/X7R/16V/K
BC63
0.1u/4/X7R/16V/K/X
unstuffed
SBC17
VTT_GMCH
BC67
BC133
BC118
4.7u/8/Y5V/10V/Z
BC69
BC70
R207
0/4
C177
BC73
BC74
0.022u/4/X7R/16V/K
BC76
C178
C188
C185
1u/4/Y5V/6.3V/Z
BC79
C180
C181
BC116
22u/8/X5R/6.3V/M
BC117
BC77
1u/6/X5R/16V/K
BC78
R204
0/4
R205
0/4/X
VCCHDA
C164
0.1u/4/X7R/16V/K
R208
R216
VCCSUSHDA
C167
C168
10u/8/X5R/6.3V/M
C169
1u/6/X5R/16V/K
C524
L8
10uH/8/100mA/1.15/S
VCC1_5_SATAPLL
L9
1uH/8/500mA/0.4/S
VCC1_5_DMIPLL
C171
C172
0.01u/4/X7R/16V/K
L10
VCC1_5_GLANPLL
C175
C176
2.2u/6/X5R/6.3V/K
BC113
BC114
BC115
NEAR ICH
GIGABYTE TEHCHNOLOGIES , INC.
Title
ICH9-PWR & GND
Size
C
Document Number
MTQ45NK-LE
Rev
1.0
Date:
Friday, August 15, 2008
Sheet
19
of
40

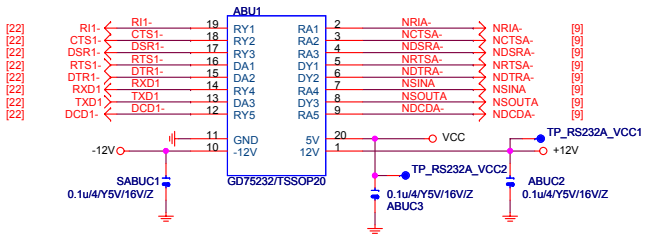

-12V
VCC
VCC3
+12V
PCI1
PCI/120/P/IV/VA
IDSEL= 16
PIRQ= E
REQ#= 0
GNT#= 0
EC23
1000U/D/6.3V/8C/36m/X
C482
100P/4/NPO/50V/X
R650
330/4
RN21
2.2K/8P4R/4
RN22
2.2K/8P4R/4
RN23
2.2K/8P4R/4
RN24
8.2K/8P4R/4
RN25
8.2K/8P4R/4
RN26
8.2K/8P4R/4
C182
0.1u/4/Y5V/16V/Z/X
C184
0.1u/4/Y5V/16V/Z/X
C186
10p/4/NPO/50V/J
C187
10p/4/NPO/50V/J
8/5 for EMI
EC9
1000U/D/6.3V/8C/36m/X
C189
0.1u/4/Y5V/16V/Z/X
C190
0.1u/4/Y5V/16V/Z/X
R210
8.2K/4
R211
8.2K/4
R212
0/4S/X
R214
0/4S/X
R213
2.2K/4/X
GIGABYTE TEHCHNOLOGIES , INC.
Title
PCI SLOT
Size
B
Document Number
MTQ45NK-LE
Rev
1.0
Date:
Friday, August 15, 2008
Sheet
20
of
40

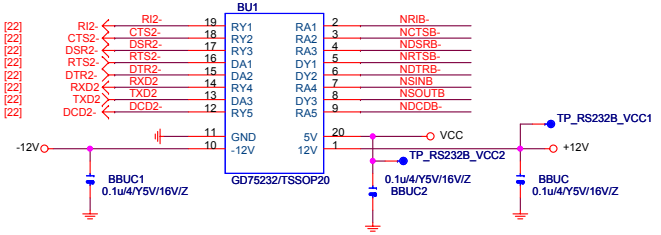


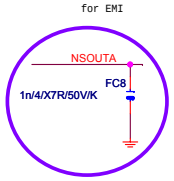

| Title | | |
|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | |
| CK505/GBT_CLK GEN | | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 21 of 40 | |

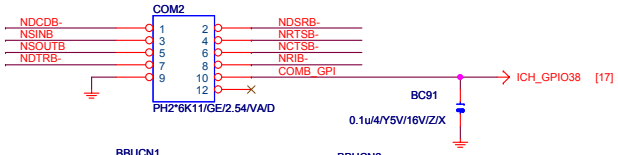

SCH5617C-A-NW/S/[10HP2-135617-30R]
IC128QFP-SMSC5167
U12
SYSOPT Strap :
High - 0x04E (Default)
Low - 0x02E
Floppy Interface
LPC Interface
SMB
Serial Port 1
Serial Port 2
Parallel Port Interface
Keyboard/ Mouse
Miscellaneous
HWM Interface
AMT, use the -S4_STATE control.
None AMT, use the -SLP_S4 control.
CLOSE PIN31
check Intel and SIO
SMSC 5617 "A" AP NOTE
VR thermal
VR thermal close VRM MOSFET
SST
thermal header
check footprint
Near chipset
Near chipset
3/5 le request
GIGABYTE TEHCHNOLOGIES , INC.
SIO SCH5617, TH, FDD
MTQ45NK-LE
Rev 1.0
Friday, August 15, 2008
Sheet 22 of 40

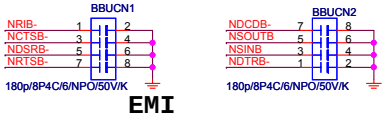
# COM



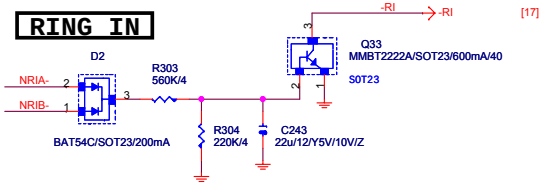



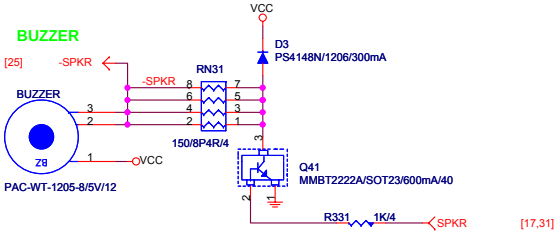




**EMI**

## RING IN

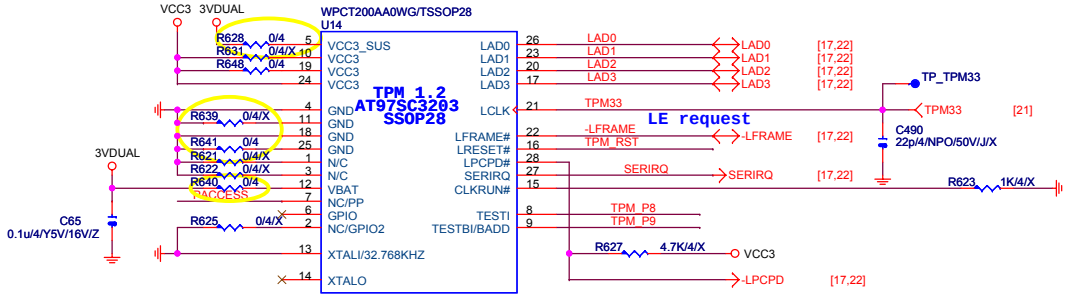


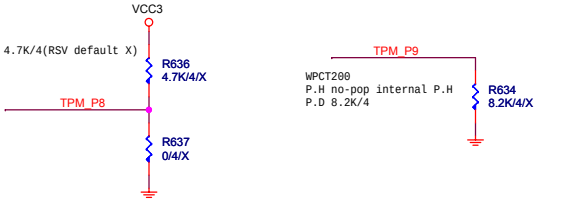




| | | |
|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | |
| Title: COM | | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 23 of 40 | |

Suff R628,R648,R641,R640 FOR WPCT200
Suff R631,R639,R621,R622,R635 FOR ST19WP18

## TPM

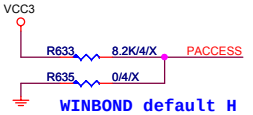


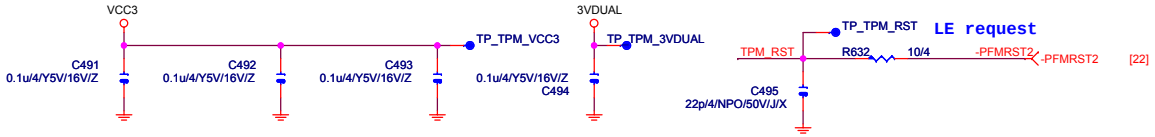




WPCT200 badd table

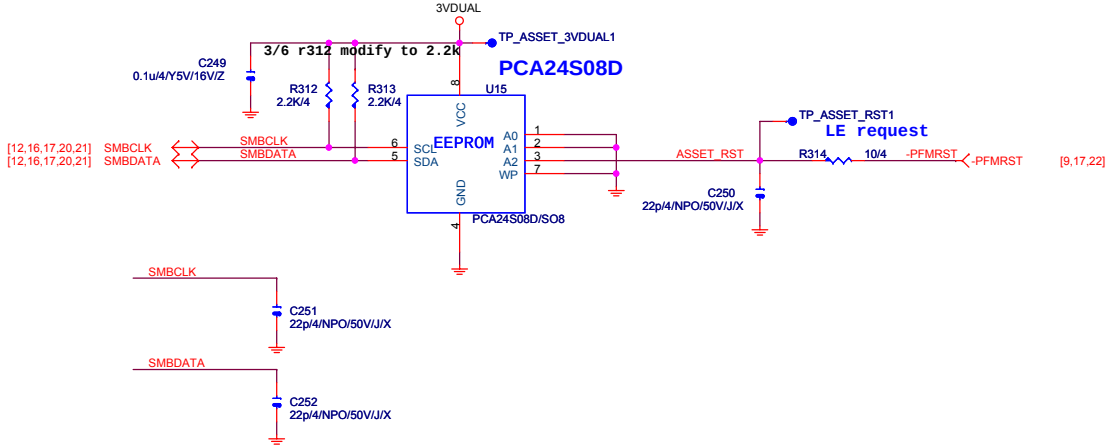
| BADD | SELECTION |
|---|---|
| 0 | EEh - EFh |
| 1 | 7Eh - 7Fh |

'1' - pin is left open.
'0' - pin is pulled down.



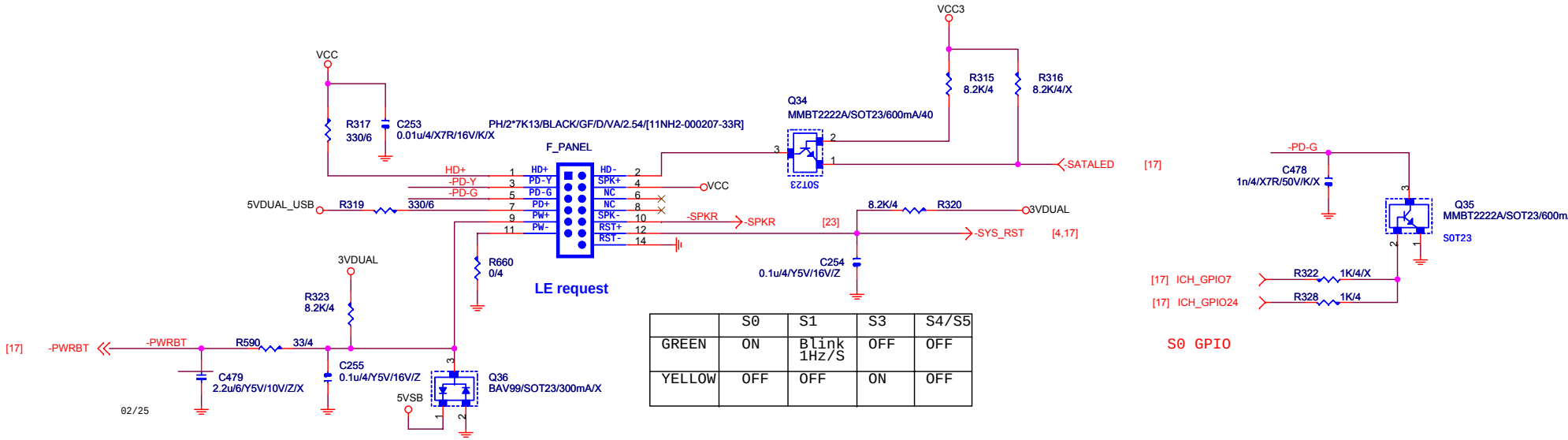

## ASSET ID




GIGABYTE TEHCHNOLOGIES , INC.

| | | |
|---|---|---|
| Title | TPM, ASSET ID | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 24 of 40 | |

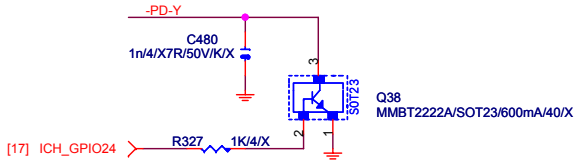
## INTEL FRONT PANEL




| | S0 | S1 | S3 | S4/S5 |
|---|---|---|---|---|
| GREEN | ON | Blink 1Hz/S | OFF | OFF |
| YELLOW | OFF | OFF | ON | OFF |

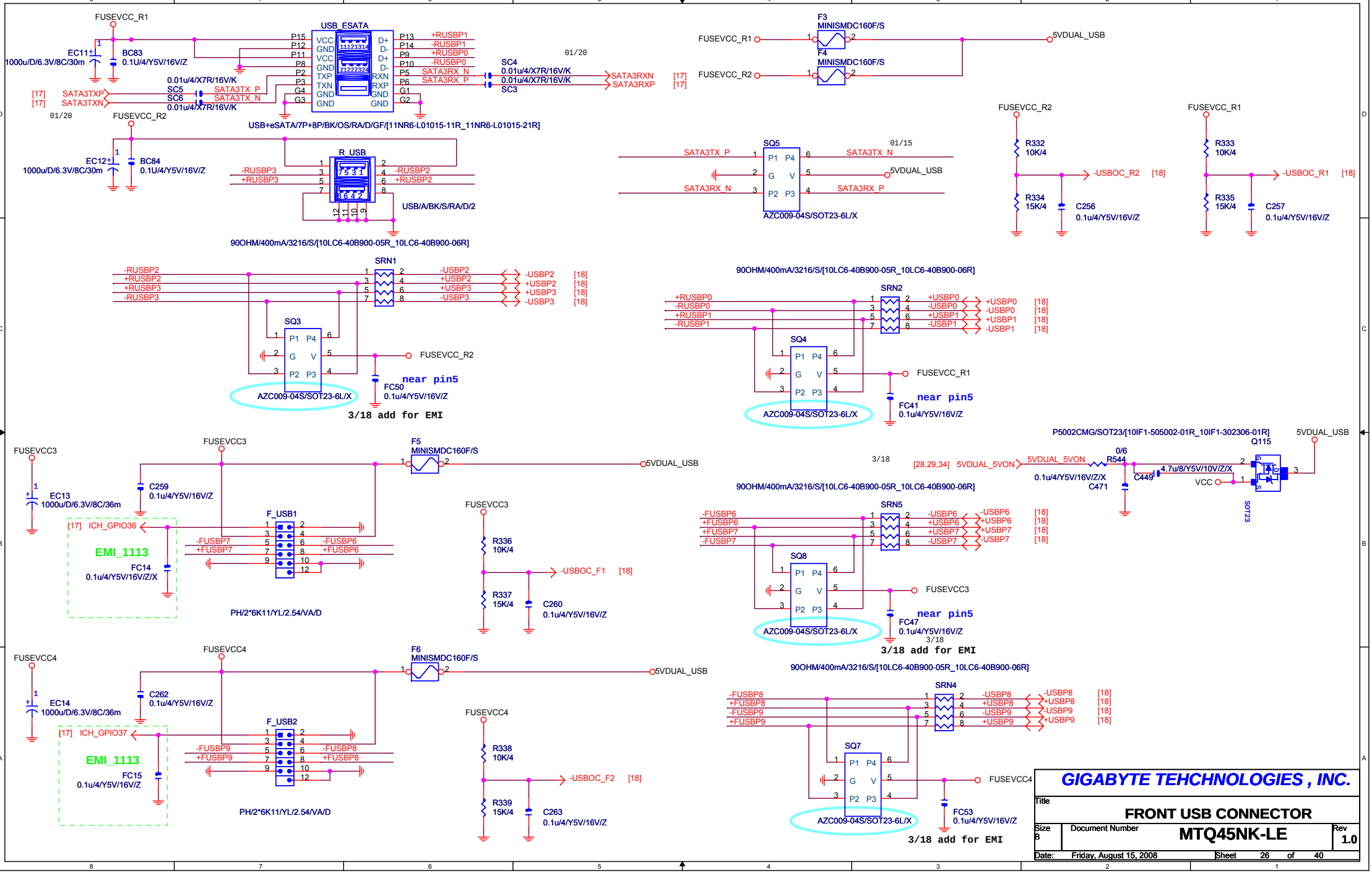


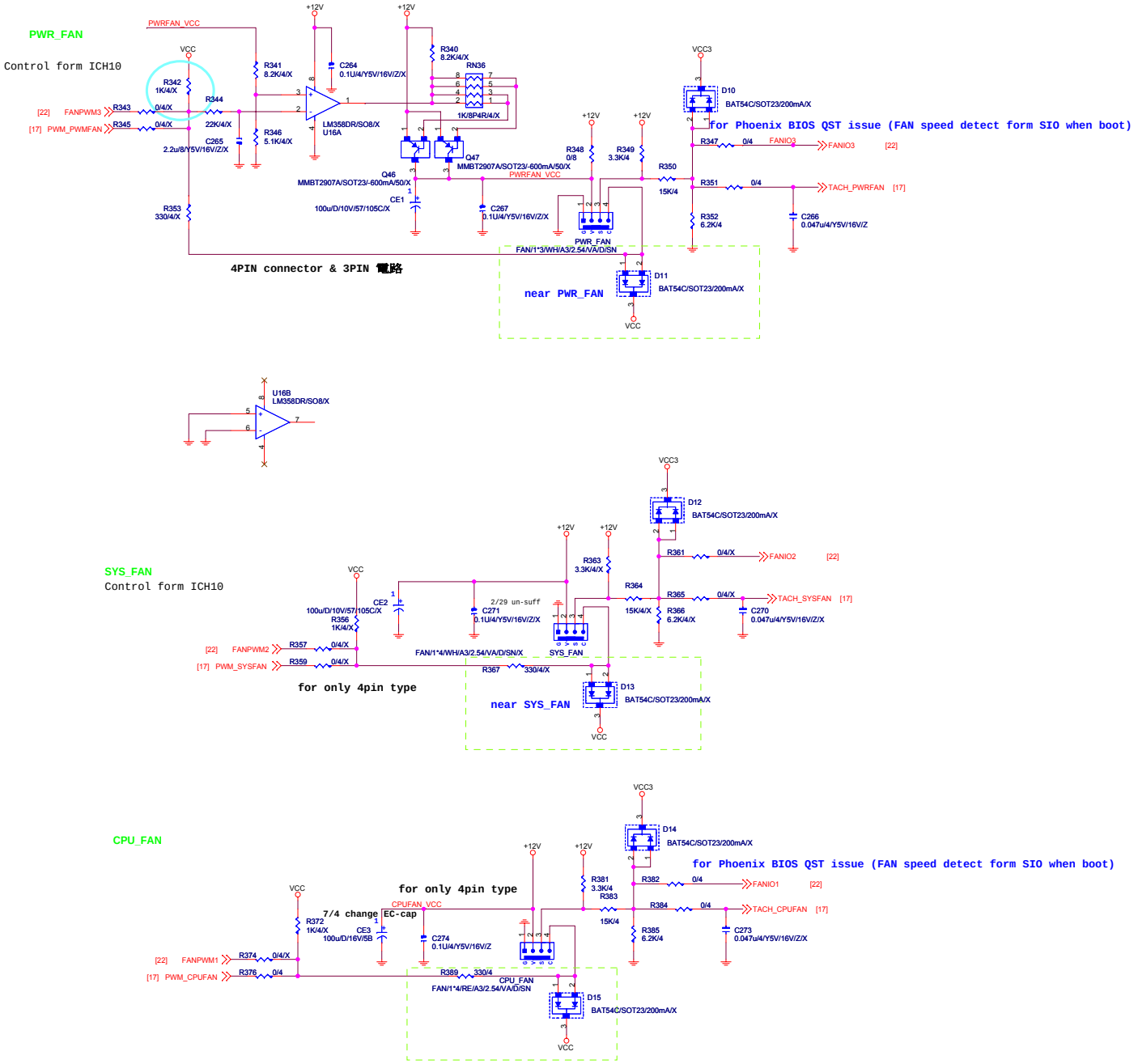

S0 GPIO



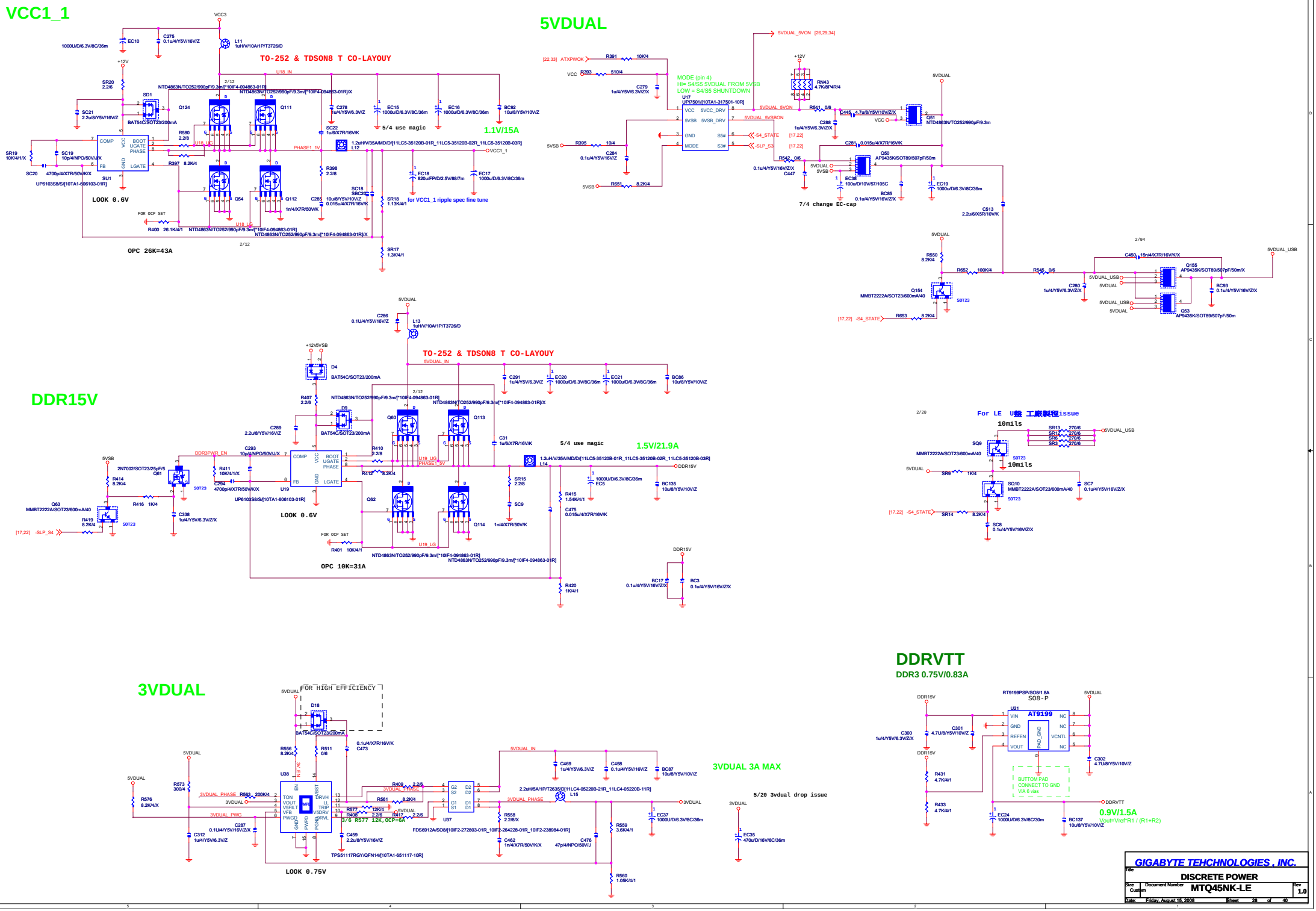

S3 GPIO

| | | | |
|---|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | | |
| Title: FRONT PANEL | | | |
| Size: B | Document Number: MTQ45NK-LE | | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 25 of 40 | | |


FUSEVCC_R1
EC11
1000u/D/6.3V/8C/30m
BC83
0.1U/4/Y5V/16V/Z
USB_ESATA
P15 VCC
P12 GND
P11 VCC
P8 GND
P2 TXP
P3 TXN
G4 GND
G3 GND
D+
D-
D+
D-
RXN
RXP
GND
GND
P13 +RUSBP1
P14 -RUSBP1
P9 +RUSBP0
P10 -RUSBP0
P5 SATA3RX_N
P6 SATA3RX_P
G1
G2
SC4
0.01u/4/X7R/16V/K
SC3
0.01u/4/X7R/16V/K
SATA3RXN [17]
SATA3RXP [17]
01/20
[17] SATA3TXP
[17] SATA3TXN
SC5
SC6
0.01u/4/X7R/16V/K
SATA3TX_P
SATA3TX_N
0.01u/4/X7R/16V/K
01/20
FUSEVCC_R2
USB+eSATA/7P+8P/BK/OS/RA/D/GF/[11NR6-L01015-11R_11NR6-L01015-21R]
EC12
1000u/D/6.3V/8C/30m
BC84
0.1U/4/Y5V/16V/Z
R_USB
-RUSBP3
+RUSBP3
-RUSBP2
+RUSBP2
USB/A/BK/S/RA/D/2
90OHM/400mA/3216/S/[10LC6-40B900-05R_10LC6-40B900-06R]
F3
MINISMDC160F/S
F4
MINISMDC160F/S
FUSEVCC_R1
FUSEVCC_R2
5VDUAL_USB
SQ5
SATA3TX_P
SATA3TX_N
SATA3RX_N
SATA3RX_P
5VDUAL_USB
AZC009-04S/SOT23-6L/X
01/15
FUSEVCC_R2
R332
10K/4
R334
15K/4
C256
0.1u/4/Y5V/16V/Z
-USBOC_R2 [18]
FUSEVCC_R1
R333
10K/4
R335
15K/4
C257
0.1u/4/Y5V/16V/Z
-USBOC_R1 [18]
SRN1
-RUSBP2
+RUSBP2
+RUSBP3
-RUSBP3
-USBP2 [18]
+USBP2 [18]
+USBP3 [18]
-USBP3 [18]
SQ3
FUSEVCC_R2
near pin5
FC50
0.1u/4/Y5V/16V/Z
AZC009-04S/SOT23-6L/X
3/18 add for EMI
90OHM/400mA/3216/S/[10LC6-40B900-05R_10LC6-40B900-06R]
SRN2
+RUSBP0
-RUSBP0
+RUSBP1
-RUSBP1
+USBP0 [18]
-USBP0 [18]
+USBP1 [18]
-USBP1 [18]
SQ4
FUSEVCC_R1
near pin5
FC41
0.1u/4/Y5V/16V/Z
AZC009-04S/SOT23-6L/X
FUSEVCC3
EC13
1000u/D/6.3V/8C/36m
C259
0.1u/4/Y5V/16V/Z
F5
MINISMDC160F/S
5VDUAL_USB
[17] ICH_GPIO36
EMI_1113
FC14
0.1u/4/Y5V/16V/Z/X
F_USB1
-FUSBP7
+FUSBP7
-FUSBP6
+FUSBP6
PH/2*6K11/YL/2.54/VA/D
FUSEVCC3
R336
10K/4
R337
15K/4
C260
0.1u/4/Y5V/16V/Z
-USBOC_F1 [18]
3/18
[28,29,34] 5VDUAL_5VON
5VDUAL_5VON
0/6
R544
0.1u/4/Y5V/16V/Z/X
C471
C449
4.7u/8/Y5V/10V/Z/X
VCC
P5002CMG/SOT23/[10IF1-505002-01R_10IF1-302306-01R]
Q115
SOT23
5VDUAL_USB
90OHM/400mA/3216/S/[10LC6-40B900-05R_10LC6-40B900-06R]
SRN5
-FUSBP6
+FUSBP6
+FUSBP7
-FUSBP7
-USBP6 [18]
+USBP6 [18]
+USBP7 [18]
-USBP7 [18]
SQ8
FUSEVCC3
near pin5
FC47
0.1u/4/Y5V/16V/Z
3/18
AZC009-04S/SOT23-6L/X
3/18 add for EMI
FUSEVCC4
EC14
1000u/D/6.3V/8C/36m
C262
0.1u/4/Y5V/16V/Z
F6
MINISMDC160F/S
5VDUAL_USB
[17] ICH_GPIO37
EMI_1113
FC15
0.1u/4/Y5V/16V/Z
F_USB2
-FUSBP9
+FUSBP9
-FUSBP8
+FUSBP8
PH/2*6K11/YL/2.54/VA/D
FUSEVCC4
R338
10K/4
R339
15K/4
C263
0.1u/4/Y5V/16V/Z
-USBOC_F2 [18]
90OHM/400mA/3216/S/[10LC6-40B900-05R_10LC6-40B900-06R]
SRN4
-FUSBP8
+FUSBP8
-FUSBP9
+FUSBP9
-USBP8 [18]
+USBP8 [18]
-USBP9 [18]
+USBP9 [18]
SQ7
FUSEVCC4
FC53
0.1u/4/Y5V/16V/Z
AZC009-04S/SOT23-6L/X
3/18 add for EMI
GIGABYTE TEHCHNOLOGIES , INC.
Title
FRONT USB CONNECTOR
Size B
Document Number
MTQ45NK-LE
Rev 1.0
Date: Friday, August 15, 2008
Sheet 26 of 40




| | | |
|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | |
| Title: FAN CONTROL | | |
| Size: C | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 27 of 40 | |


VCC1_1
TO-252 & TDSON8 T CO-LAYOUY
1.1V/15A
5/4 use magic
LOOK 0.6V
OPC 26K=43A
for VCC1_1 ripple spec fine tune
5VDUAL
MODE (pin 4)
Hi= S4/S5 5VDUAL FROM 5VSB
LOW = S4/S5 SHUNTDOWN
7/4 change EC-cap
DDR15V
TO-252 & TDSON8 T CO-LAYOUY
1.5V/21.9A
5/4 use magic
LOOK 0.6V
OPC 10K=31A
For LE U盤 工廠製程issue
10mils
3VDUAL
FOR HIGH EFFICIENCY
3VDUAL 3A MAX
5/20 3vdual drop issue
LOOK 0.75V
DDRVTT
DDR3 0.75V/0.83A
0.9V/1.5A
Vout=Vref*R1 / (R1+R2)
BUTTOM PAD
CONNECT TO GND
VIA 6 vias
GIGABYTE TEHCHNOLOGIES , INC.
DISCRETE POWER
MTQ45NK-LE
1.0
Friday, August 15, 2008
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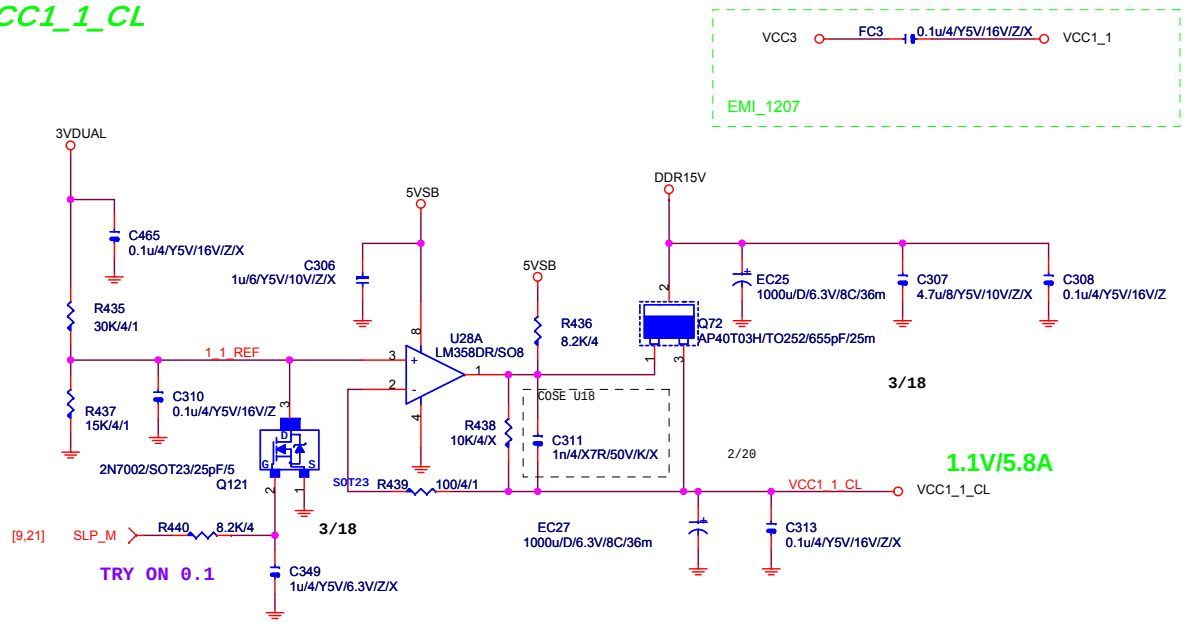
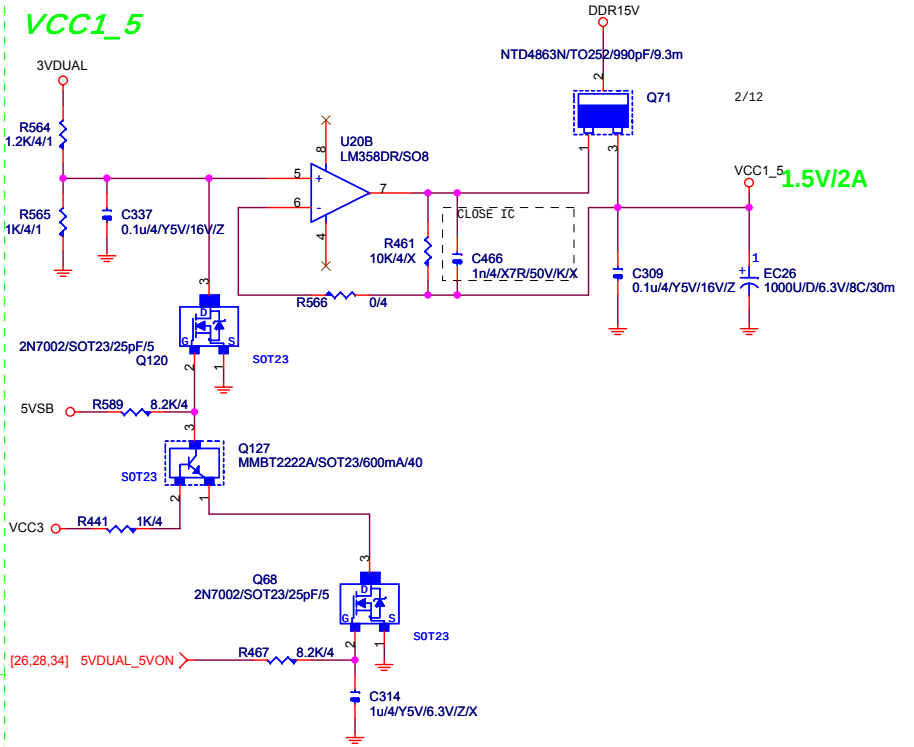
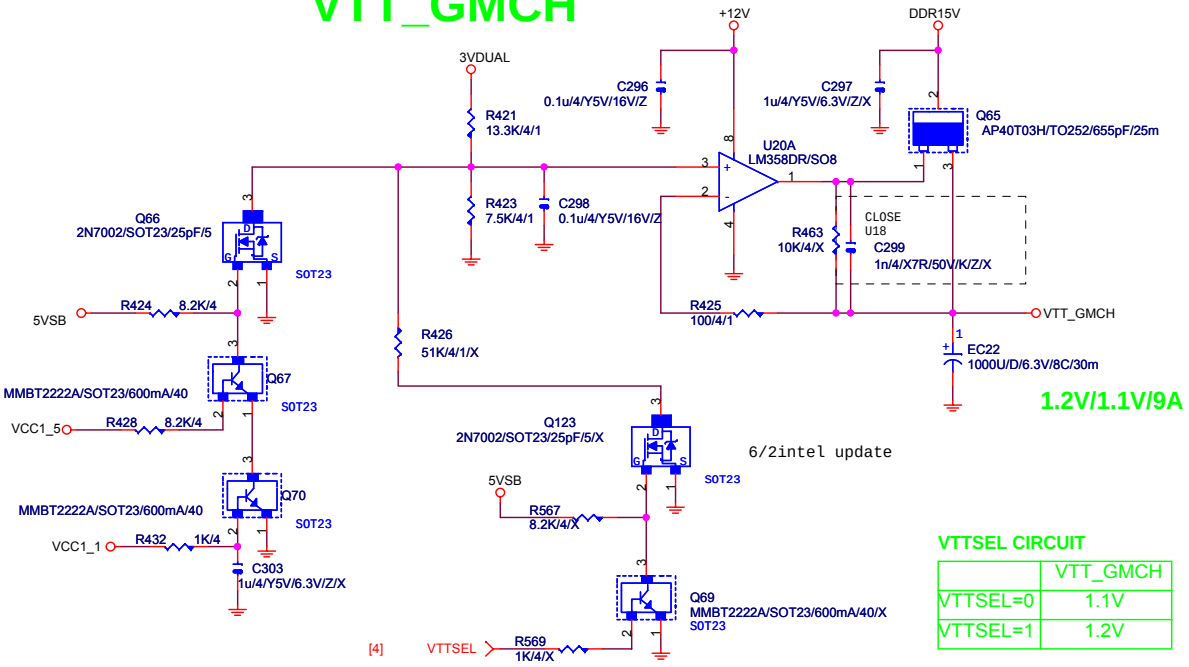
## VCC1_1_CL




## VCC1_5



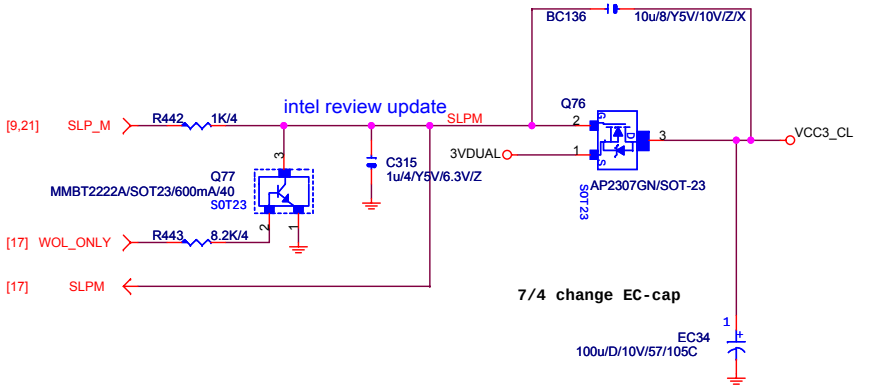

## VTT_GMCH




**VTTSEL CIRCUIT**

| | VTT_GMCH |
|---|---|
| VTTSEL=0 | 1.1V |
| VTTSEL=1 | 1.2V |

## VCC3_CL



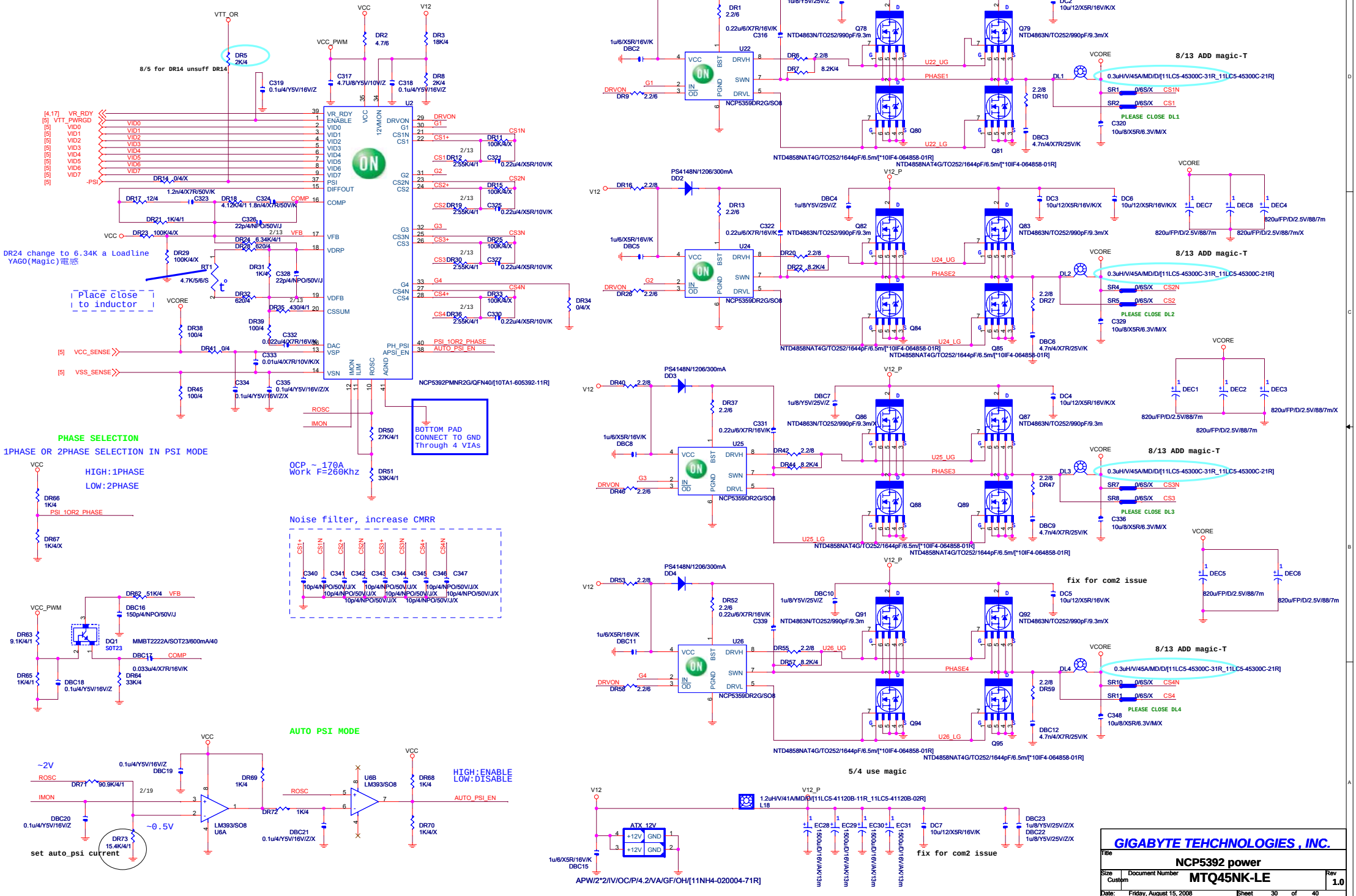

**GIGABYTE TEHCHNOLOGIES , INC.**

| | | |
|---|---|---|
| Title | DISCRETE POWER | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 29 of 40 | |

# NCP5392P Intel VRD11/VRD11.1 (Support auto PSI mode)

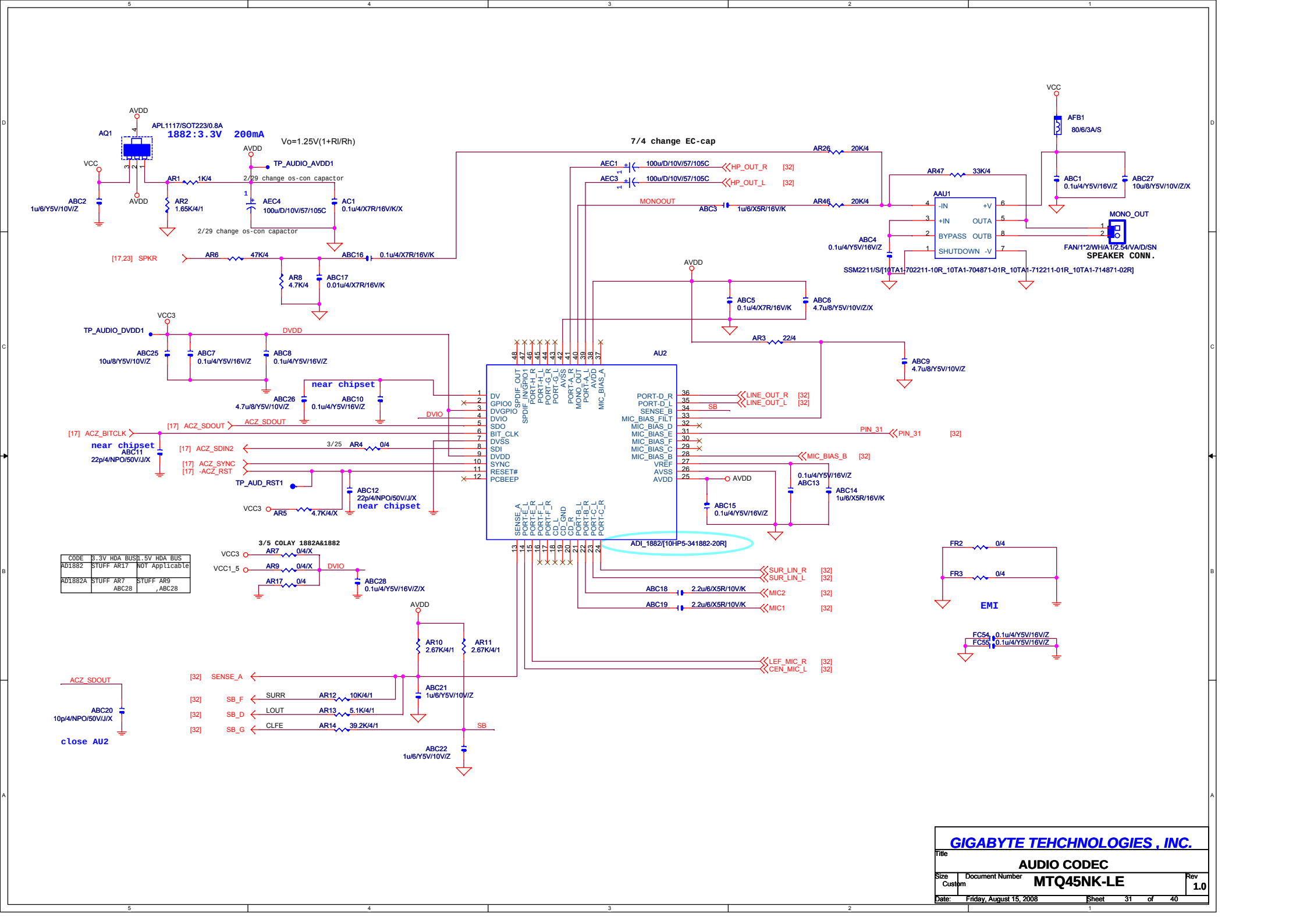
TO-252 & TDSON8 T CO-LAYOUY

0.8V~1.55V/125A




GIGABYTE TEHCHNOLOGIES , INC.

| | | | |
|---|---|---|---|
| Title | NCP5392 power | | |
| Size: Custom | Document Number: MTQ45NK-LE | | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 30 of 40 | | |

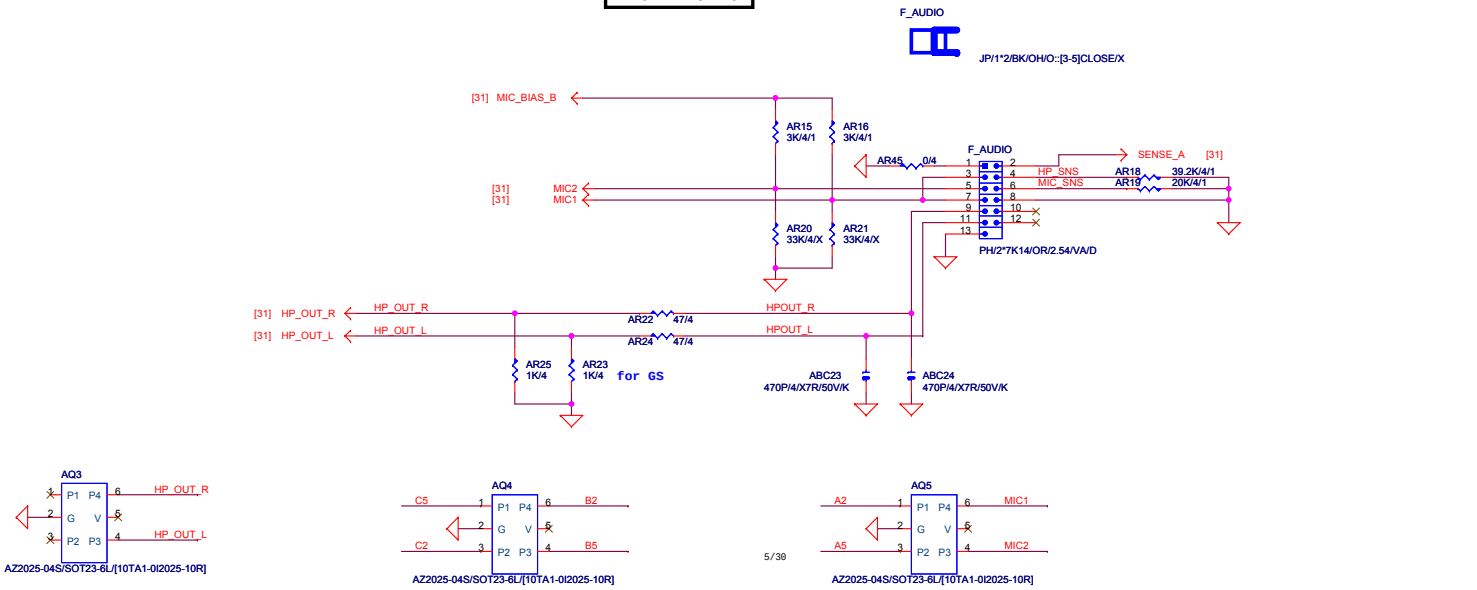



| CODE | 3.3V HDA BUS | 1.5V HDA BUS |
|---|---|---|
| AD1882 | STUFF AR17 | NOT Applicable |
| AD1882A | STUFF AR7 ABC28 | STUFF AR9 ,ABC28 |

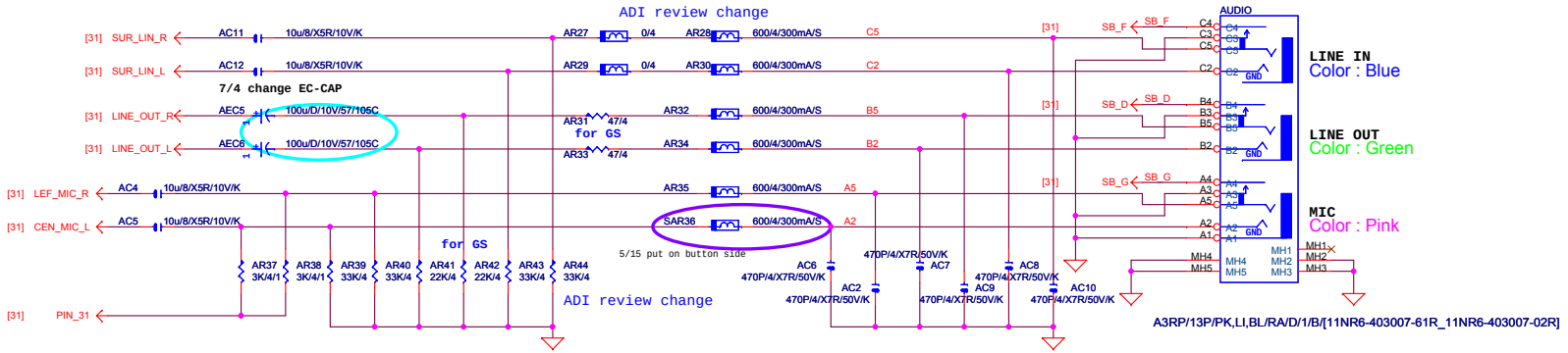
**GIGABYTE TEHCHNOLOGIES , INC.**

| | | |
|---|---|---|
| Title | AUDIO CODEC | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 31 of 40 | |

## FRONT AUDIO

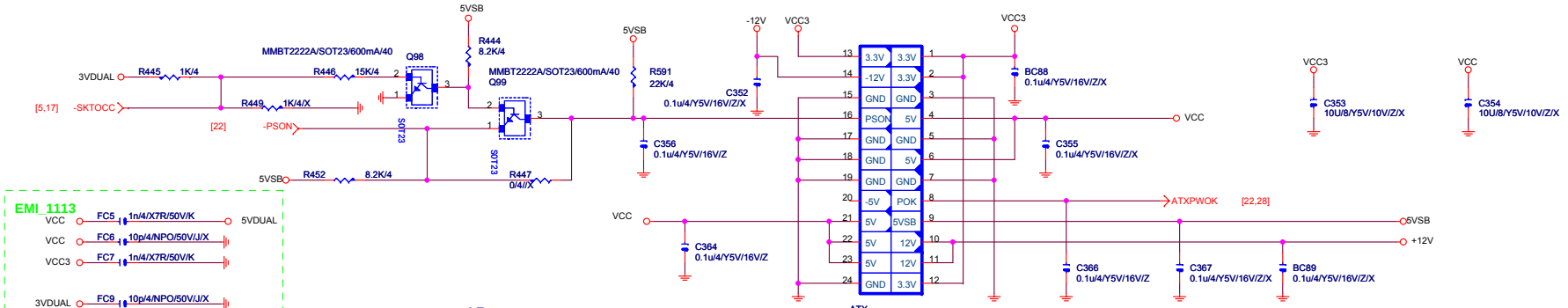



## AUDIO JACK




| | | | |
|---|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | | |
| Title: AUDIO JACK | | | |
| Size: Custom | Document Number: MTQ45NK-LE | | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 32 of 40 | | |

## ATX POWER CONNECTOR



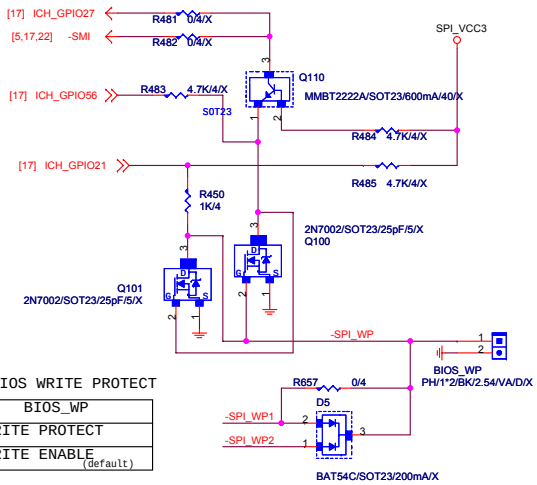

APW/2*12/IV/OC/OP/4.2/VA/GF/LK/2H/[11NH4-020024-54R_11NH4-020024-51R] 3/18 add for EMI

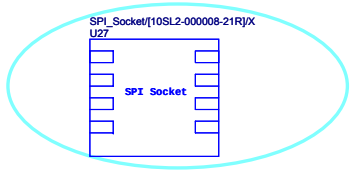
### EMI_1113

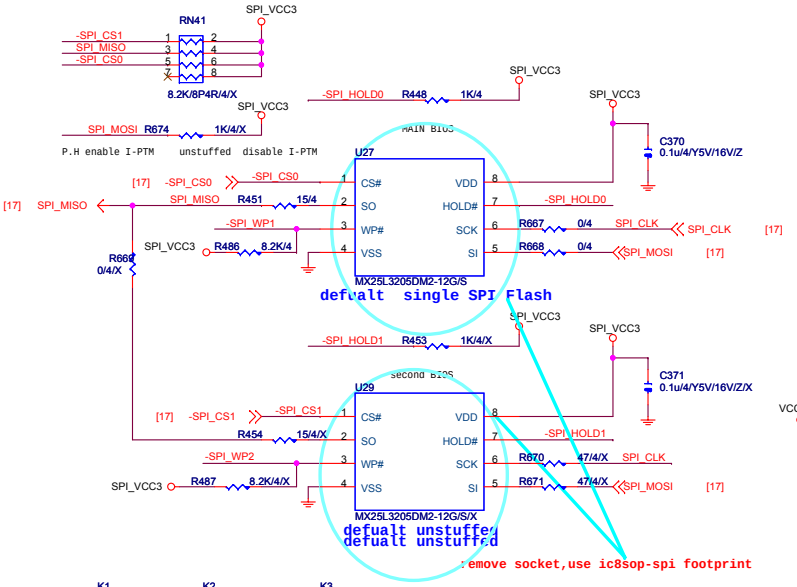


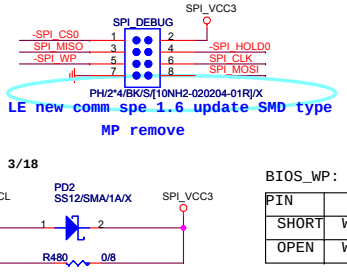

### LE request


### BIOS WP



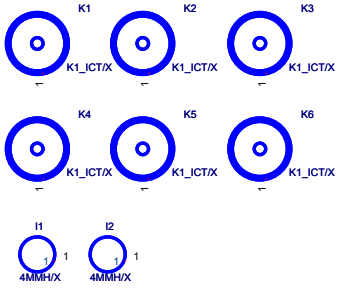



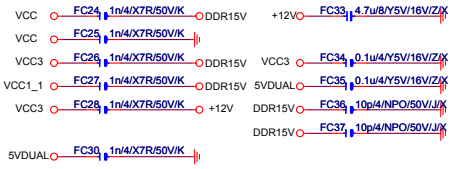

3/18

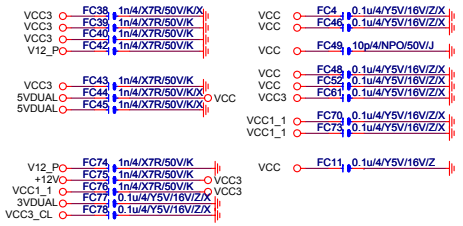



BIOS_WP: BIOS WRITE PROTECT

| PIN | BIOS_WP |
|---|---|
| SHORT | WRITE PROTECT |
| OPEN | WRITE ENABLE (default) |

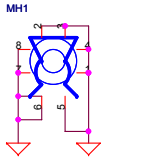


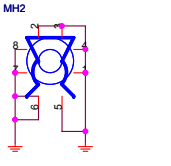



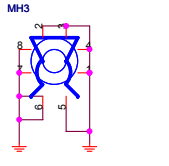



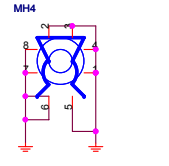







**GIGABYTE TEHCHNOLOGIES , INC.**

| | | |
|---|---|---|
| Title | ATX,SPI(BIOS),MECH HOLD | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 33 of 40 | |

BOAZMAN

LU1
82567LM/[10HP2-402567-32R]

BOAZ

GLAN_RXP [18] C377 0.1u/4/X7R/16V/K GLANRXP
GLAN_RXN [18] C378 0.1u/4/X7R/16V/K GLANRXN
GLAN_TXP [18]
GLAN_TXN [18]
GLAN_CLK [17] 33/4 R455 JKCLK
LANRSTSYNC [17]
LAN_TXD0 [17]
LAN_TXD1 [17]
LAN_TXD2 [17]
LAN_RXD0 [17]
LAN_RXD1 [17]
LAN_RXD2 [17]
LAN_LED1 R465 33/6 LAN_LED0 LAN_LED_1 LAN_LED2
4.87K/4/1 R456 LAN_RSET
7/21 R466 suff
TP20 TP21
VCC3_LAN 1K/4/X R457 1K/4 R458 0/4 R466 8.2K/4 R459 8.2K/4 R460
LAN_DISABLE [17] LAN_DISABLE_R
27P/4/NPO/50V/J C387
X4 25M/20p/30ppm/49US/20/D
27P/4/NPO/50V/J C388
TP_LAN1 TP_LAN2 TP_LAN3 TP_LAN4 TP_LAN5

| | | | | |
|---|---|---|---|---|
| GLAN_TXP | GLAN_TXN | GLAN_RXP | GLAN_RXN | JKCLK |
| JRSTSYNC | JTXD_0 | JTXD_1 | JTXD_2 | JRXD_0 |
| JRXD_1 | JRXD_2 | LED_0 | LED_1 | LED_2 |
| RSET | IEEE_TEST_P | IEEE_TEST_N | DIS_REG10 | LAN_DISABLE_N |
| TEST_EN | XTAL2 | XTAL1 | JTAG_TRST | JTAG_TCK |
| JTAG_TMS | JTAG_TDI | JTAG_TDO | MDI_N_0 | MDI_P_0 |
| MDI_N_1 | MDI_P_1 | MDI_N_2 | MDI_P_2 | MDI_N_3 |
| MDI_P_3 | VDDO_33_3 | VDDO_33_46 | AVDD_33_28 | DVDD_10_5 |
| DVDD_10_8 | DVDD_10_33 | DVDD_10_38 | AVDD_18_11 | AVDD_18_14 |
| AVDD_18_19 | AVDD_18_18 | AVDD_18_24 | AVDD_18_25 | AVDD_18_41 |
| AVDD_18_54 | AVDD_18_32 | AVDD_18_30 | CTRL18 | CTRL10 |
| RESERVED_NC | GND_PAD | TRD0N | TRD0P | TRD1N |
| TRD1P | TRD2N | TRD2P | TRD3N | TRD3P |
| VCC3_LAN | VAUX_10 | VAUX_18 | CTRL_18 | CTRL_10 |

LE LED COMM SPEC 1.6 update

| 10/100M | | LAN LED for LE ONLY | | |
|---|---|---|---|---|
| | | Orange | Green | |
| LINK | 10Mb | | OFF | |
| | 100Mb | | ON | |
| ACTIVE | 10Mb | Blink | | |
| | 100Mb | Blink | | |
| ACTIVE | no Active on | | | |

P35-152-19W9

U4 U3 U2 U1
U8 U7 U6 U5
L1 L3 L5 L7 L9
L2 L4 L6 L8 L10
D1 D2 D3 D4
YELLOW ORANGE GREEN

Dual Color LED
D4 D3 Green
D4 D3 Orange

Single Color LED
D2 D1 Yellow

VAUX_18
Close to 82567
C372 0.1u/4/Y5V/16V/Z
C373 1u/6/Y5V/10V/Z
C374 100P/4/NPO/50V/J
C375 0.1u/4/Y5V/16V/Z
C376 0.1u/4/Y5V/16V/Z/X

VCC3_LAN
R672 5.1K/4
C380 0.1u/4/Y5V/16V/Z
C381 4.7U/8/Y5V/10V/Z
C382 0.1u/4/Y5V/16V/Z
CTRL_10
0507
Q102
BCP69/SOT223/-1A/60/X
0.1u/4/Y5V/16V/Z
C384
C519
C385 10u/8/X5R/6.3V/M
C386 10u/8/X5R/6.3V/M
C383 0.1u/4/Y5V/16V/Z
C518 0.1u/4/Y5V/16V/Z
VAUX_10

VCC3_LAN
R673 5.1K/4
C390 0.1u/4/Y5V/16V/Z
C520 0.1u/4/Y5V/16V/Z
C521 0.1u/4/Y5V/16V/Z
C391 4.7u/8/Y5V/10V/Z
FB10 0/6
C522 10u/8/Y5V/10V/Z
VCC3_CL
CTRL_18
Q103
BCP69/SOT223/-1A/60
C393 10u/8/X5R/6.3V/M
C394 0.1u/4/Y5V/16V/Z
C395 0.1u/4/Y5V/16V/Z
C396 0.1u/4/Y5V/16V/Z
VAUX_18
EC32 100u/D/10V/57/105C/X

VCC3_3:
One – 10uF; Two-4.7uF, Y5V; Five-0.1 uF use near; multiple 3.3V pins
VCC1_8:
Two-10 uF, X5R one on the emitter and one on the collector, One-0.1 uF on the collector and multiple near VCC1_8 power pins.
VCC1_0 : (external)
Two-10 uF,X5R; Two-0.1 uF and multiple; near VCC1_0 power pins
VCC1_0 : (internal)
Two-4.7 uF, X5R and multiple .1uF near the VCC1_0 power pins.

USB_LAN CONNECTOR

VCC3_LAN R462 150/6 LANLED1
90OHM/400mA/3216/S/[10LC6-40B900-05R_10LC6-40B900-06R]
SRN3
-RUSBP4 +RUSBP4 -RUSBP5 +RUSBP5
-USBP4 +USBP4 -USBP5 +USBP5 [18]

C523 10u/8/Y5V/10V/Z
C397 0.1u/4/Y5V/16V/Z CTP
C398 0.1u/4/Y5V/16V/Z/X
VAUX_18
LFB1 0/6

OPC SURGE LAN CONNECTOR
FOR intel 82566 support 8KV

LED1 R552 0/6/X LAN_LED1
LED2 R554 0/6
LED1 R555 0/6
LED2 R553 0/6/X LAN_LED2

04/01

VCC3_LAN 10p/4/NPO/50V/J FC29
VCC3_LAN 10p/4/NPO/50V/J FC32
VAUX_18 10p/4/NPO/50V/J FC56

USB+LAN/1G/GO,Y/OS/RA/D/LE/[11NR6-702009-89R]
USB_LAN
Left Right
UP
DOWN
TRD0P TRD0N TRD1P TRD1N TRD2P TRD2N TRD3P TRD3N
L1 L2 L3 L4 L5 L6 L7 L8 L9 L10
D1 D2 D3 D4
LAN_LED0 10p/4/NPO/50V/J LANLED1 0.1u/4/Y5V/16V/Z
LED1 10p/4/NPO/50V/J LED2 0.1u/4/Y5V/16V/Z
EMI_1113
FC12 FC16 FC31 C400
U5 U6 U7 U8 U1 U2 U3 U4
-RUSBP5 +RUSBP5 -RUSBP4 +RUSBP4
C401 0.1u/4/Y5V/16V/Z
0.1u/4/Y5V/16V/Z/X C402
R464 0/4
VAUX_18 FOR INTEL REQ
P5002CMG/SOT23/[10IF1-505002-01R_10IF1-302306-01R]
SQ6 AZC009-04S/SOT23-6L/X
FUSEVCC_R3
FC51 0.1u/4/Y5V/16V/Z
F7 MINISMDC160F/S
5VDUAL_USB
R473 10K/4
R474 15K/4
C409 0.1u/4/Y5V/16V/Z
-USBOC_R3 [18]
FUSEVCC_R3
EC33 1000u/D/6.3V/8C/36m

MDI termination have been integrated to Boazman silicon

[26,28,29] 5VDUAL_5VON
R551 0/6
0.1u/4/Y5V/16V/Z/X C472
4.7u/8/Y5V/10V/Z/X C454
VCC
Q116
SOT23
5VDUAL_USB

| 10M/100M | Status | Speed | Active |
|---|---|---|---|
| | | Left | Right |
| | | Green | Yellow |
| | 10Mb | OFF | Blink |
| | 100Mb | ON | Blink |

| Gigabit | Status | Speed | | Active |
|---|---|---|---|---|
| | | Left | | Right |
| | | Dual Color LED | | Yellow |
| | | Green | Orange | |
| | 10Mb | OFF | OFF | Blink |
| | 100Mb | ON | OFF | Blink |
| | 1Gb | OFF | ON | Blink |

GIGABYTE TEHCHNOLOGIES , INC.

Title: intel GbE 82567LM BOAZMAN
Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0
Date: Friday, August 15, 2008 | Sheet 34 of 40

## ICH10 GPIO TABLE (EDS Ver:0.7v1)

| GPIO | Use Signal Name | Power | USE In/Out | ACTIVE H/L | Mark | INTERNAL/EXTERIOR PULL HIGH / LOW |
|---|---|---|---|---|---|---|
| GPIO_0 | ICH_BMBUSYB | VCC3 | IN | L | SET Bus master busy from SST | FORM ICH_QST_BMBUSYB |
| GPIO_1 | TACH_SYSFAN | VCC3 | IN | --- | SYSTEM FAN speed detect | EXT / HIGH |
| GPIO_2 | -PIRQE | VCC3 | --- | L | PCI1 solt IRQA | EXT / HIGH |
| GPIO_3 | -PIRQF | VCC3 | --- | L | PCI2 solt IRQA | EXT / HIGH |
| GPIO_4 | -PIRQG | VCC3 | --- | --- | no use | EXT / HIGH |
| GPIO_5 | -PIRQH | VCC3 | --- | --- | no use | EXT / HIGH |
| GPIO_6 | TACH_PWRFAN | VCC3 | IN | --- | PWR FAN speed detect | EXT / HIGH |
| GPIO_7 | -FP_AUD_DET | VCC3 | IN | L | DETECT FRONT AUDIO L=INSERT H=NO-INS DEFAULT=H | EXT / HIGH |
| GPIO_8 | DRAMPWROK | 3VDUAL | Out | H | ICH to MCH | EXT / HIGH |
| GPIO_9 | WOL_ONLY | 3VDUAL | Out | H | enable LAN of power under S3~S5 if AMT or ASF diable | EXT / HIGH |
| GPIO_10 | -SKTOCC | 3VDUAL | IN | L | Detect CPU in socket L=INSERT H=NO-INS DEFAULT=H | EXT / HIGH |
| GPIO_11 | -SMBALRT | 3VDUAL | IN | --- | no use | EXT / HIGH |
| GPIO_12 | LAN_DISABLE | 3VDUAL | Out | H | INTEL 82567LF/LM FUNCTION L=DISABLE H=ENABLE DEFAULT=H | EXT / HIGH |
| GPIO_13 | -LPCPME | 3VDUAL | IN | L | LPC POWER MANAGEMENT EVEN | EXT / HIGH |
| GPIO_14 | ICH_QST_BMBUSYB | 3VDUAL | Out | L | SST Bus master busy arrange | EXT / HIGH |
| GPIO_15 | -CK_PCI_STOP | 3VDUAL | Out | L | set PCI clock to stop from clock gen fot AMT mode L=STOP PCI CLOCK H=ENABLE PCI CLOCK DEFAULT=H | NO NEED |
| GPIO_16 | ICH_GPO16 | VCC3 | Out | L | for LE BIOS WP | INT PULL / DOWN EXT / HIGH |
| GPIO_17 | TACH_CPUFAN | VCC3 | IN | --- | CPU FAN speed detect | EXT / HIGH |
| GPIO_18 | N/C | VCC3 | OUT | --- | no use COME GPO WIILL 1H FREQENCY | EXT / HIGH |
| GPIO_19 | SATA1GP_PU | VCC3 | IN | H | open interlock switch corresponding | EXT / HIGH |
| GPIO_20 | N/C | VCC3 | OUT | L | no use FOR STRAP PIN RESERVED STRAP (DON'T PULL-HIGH) | INT PULL / DOWN TP |
| GPIO_21 | SATA0GP_PU | VCC3 | IN | H | open interlock switch corresponding | EXT / HIGH |
| GPIO_22 | ICH_SGP22_PU | VCC3 | --- | --- | no use | EXT / HIGH |
| GPIO_23 | N/C | VCC3 | --- | --- | no use | INT PULL / HIGH TP |
| GPIO_24 | AMT_LED | 3VDUAL | OUT | H | INDICATE LED FOR ATM MODE L=DRAM NO POWER H=DRAM HAVE POWER | EXT / HIGH |
| GPIO_25 | -CK_CPU_STOP | 3VDUAL | OUT | H | set CPU clock to stop from clock gen fot AMT mode L=STOP CPU CLOCK H=ENABLE CPU CLOCK DEFAULT=H | NO NEED |
| GPIO_26 | N/C | 3VDUAL | OUT | --- | no use | TP |
| GPIO_27 | ICH_GPO27 | 3VDUAL | IN | L | BIOS WRITE PROTECT L=ENABLE H=DISABLE DEFAULT=H | EXT / HIGH |
| GPIO_28 | 5VDUAL_SW | 3VDUAL | Out | L | CONTROL 5VDUAL OUTPUT UNDER S4/S5 MODE L=DIABLE H=ENABLE DEFAULT=L | EXT / HIGH |
| GPIO_29 | -USBOC_R3 | 3VDUAL | IN | L | DETECT USB4,5 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_30 | -USBOC_F1 | 3VDUAL | Out | L | DETECT USB6,7POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_31 | -USBOC_F2 | 3VDUAL | Out | L | DETECT USB6,7POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_32 | ICH_GPO32 | VCC3 | Out | H | CONTROL GTLREF OFFSET | EXT / HIGH |
| GPIO_33 | ICH_GPIO33 | VCC3 | IN | --- | SECURITY FLASH DESCRIPTOR H=EFFECT L=OVERRIDE DEFAULT=H | INT PULL / HIGH EXT / HIGH |
| GPIO_34 | ICH_GPO34 | VCC3 | Out | L | for LE BIOS WP | EXT / HIGH |
| GPIO_35 | ICH_GPO35 | VCC3 | Out | L | CONTROL GTLREF OFFSET | EXT / HIGH |
| GPIO_36 | SATA2GP_PU | VCC3 | IN | H | open interlock switch corresponding | EXT / HIGH |
| GPIO_37 | SATA3GP_PU | VCC3 | IN | H | open interlock switch corresponding | EXT / HIGH |
| GPIO_38 | ICH_SGP38_PU | VCC3 | IN | --- | no use | EXT / HIGH |
| GPIO_39 | ICH_MBID0 | VCC3 | IN | --- | M/B ID 0 | EXT / LOW |
| GPIO_40 | -USBOC_R1 | 3VDUAL | IN | L | DETECT USB0,1 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_41 | -USBOC_R2 | 3VDUAL | IN | L | DETECT USB2,3 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_42 | -USBOC_R2 | 3VDUAL | IN | L | DETECT USB2,3 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_43 | -USBOC_R3 | 3VDUAL | IN | L | DETECT USB4,5 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_44 | -USBOC_F2 | 3VDUAL | IN | L | DETECT USB8,9 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_45 | -USBOC_F2 | 3VDUAL | IN | L | DETECT USB8,9 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_46 | N/C | 3VDUAL | --- | --- | NO USE PUSH HIGH | EXT / HIGH |
| GPIO_47 | N/C | 3VDUAL | --- | --- | NO USE PUSH HIGH | EXT / HIGH |
| GPIO_48 | ICH_MBID1 | VCC3 | IN | --- | M/B ID 1 | EXT / LOW |
| GPIO_49 | GPIO49 | VCC3 | OUT | H | DMI HALF/FULL AWING STRAP FOR EAGLELAKE = HIGH(EMPTY) HALF | INT PULL / HIGH |

| GPIO | Use Signal Name | Power | USE In/Out | ACTIVE H/L | Mark | INTERNAL PULL HIGH / LOW |
|---|---|---|---|---|---|---|
| GPIO_50 | -REQ1 | VCC | --- | L | FOR PCI SOLT1 REQ SIGNAL | EXT / HIGH |
| GPIO_51 | -GNT1 | VCC3 | Out | L | FOR PCI SOLT1 GNT SIGNAL RESERVED STRAP ,NOT PULL LOW | INT PULL / HIGH |
| GPIO_52 | -REQ2 | VCC | --- | --- | NO USE PUSH HIGH | EXT / HIGH |
| GPIO_53 | -GNT2 | VCC3 | --- | --- | NO USE PCIE PORT COFIG 2 STRAP | INT PULL- HIGH |
| GPIO_54 | -REQ3 | VCC | --- | --- | NO USE PUSH HIGH | EXT / HIGH |
| GPIO_55 | -GNT3 | VCC3 | --- | --- | NO USE TOP-BLOCK SWAP OVERRIDE STRAP | INT PULL- HIGH |
| GPIO_56 | ICH_GPIO56 | 3VDUAL | IN | --- | NO USE PUSH HIGH | EXT / HIGH |
| GPIO_57 | ITPM_EN_ICH1 | 3VDUAL | IN | --- | INTERNAL ITPM FUNCTION STRAP H=ENABLE L=DISABLE DEFAULT=H | EXT / HIGH EXT / LOW |
| GPIO_58 | -SPI_CS1_C | 3VDUAL | IN | --- | WITH GNT0 SELETC BIOS TYPE STRAP | INT PULL- HIGH |
| GPIO_59 | -USBOC_R1 | 3VDUAL | IN | L | DETECT USB0,1 POWER OC L=OC OCCUR H=FREE DEFAULT=H | EXT / HIGH |
| GPIO_60 | -LINKALERT | 3VDUAL | --- | --- | NO USE PUSH HIGH | EXT / HIGH |
| GPIO_61 | -LPCPD | 3VDUAL | OUT | L | LPC DEVICE POWER DOWN L=ENABLE H=DISABLE DEFAULT=H | EXT / HIGH |
| GPIO_62 | SUSCLK | 3VDUAL | --- | --- | SAME WITH RTC CLOCK | TP |
| GPIO_63 | -SLP_S5 | 3VDUAL | --- | --- | no use | TP |
| GPIO_72 | TP0 | VCC3 | --- | --- | no use | TP |
| | | | | | | |

## EAGLELAKE PLATFORM STRAP LIST

| Use Signal Name HDA_SDOUT (INT PULL/DOWN) | Use Signal Name TP3 (INT PULL/HIGH) | Usage | When Sample | Comment |
|---|---|---|---|---|
| --- | L | XOR Chain Entrance | Rising Edge of PWROK | Allows entrance to XOR chain testing |
| L | H | PCIE port Config 1 bit1 only for consumer | Rising Edge of PWROK | Chipset Config Registers :offset 224h |
| H | H | Danbury Technology enable only for corporate | Rising Edge of PWROK | H=Danbury enable L= Danbury disable Default |
| -SATALED (INT PULL/HIGH) | | PCIE 1x4 lane reversal only for consumer | Rising Edge of PWROK | If HDA_SDOUT=H HDA_SYNC=H -SATALED =H disable Default -SATALED =L enable set PCIe=1x4 PS:LAYOUT NOT IMPLEMENT |
| HDA_SYNC (INT PULL/DOWN) | | Set PCIE port 1x4 lane only for consumer | Rising Edge of PWROK | collocate with HDA_SDOUT HDA_SDOUT=H HDA_SYNC=H PCIE = 1X4 HDA_SDOUT=L HDA_SYNC=L PCIE = 4X1 Default L,H or H,L reserved PS:LAYOUT NOT IMPLEMENT |
| -GNT2 (INT PULL/HIGH) | | DMI Clock Gate Enable | Rising Edge of PWROK | PRC,PC2 offset :0224 bit 0:1 BIOS must program field 11b H= Enable default L= Disable |
| -GNT1 (INT PULL/HIGH) | | | Rising Edge of PWROK | H= Disable default L= Enable |
| -GNT3 (INT PULL/HIGH) | | Top Block Swap Override | Rising Edge of PWROK | ICH10 inverts A16 for all cycles targeting BIOS sapce H= Enable default L= Disable |
| -GNT0 (INT PULL/HIGH) | -SPI_CS1_C (INT PULL/HIGH) | Boot BIOS Destination selection | Rising Edge of PWROK | If option LPC is selected BIOS may still be placed on LPC ,But all platforms with ICH10(Corportate only) require SPI flash connected directly to the SPI bus with a vaild descriptor in order to boot |
| L | H | SPI ROM default | | |
| H | L | PCI ROM | | |
| H | H | LPC ROM | | |
| TP20 (INT PULL/LOW) | | Reserved | Rising Edge of PWROK | RESERVED STRAP (DON'T PULL-HIGH) |
| SPKR (INT PULL/LOW) | | No Reboot | Rising Edge of PWROK | ICH10 will control the TCO timer system reboot feature. H= Enable L= Disable default |
| ICH_GPIO33 (INT PULL/HIGH) | | Flash Descriptor Security Override | Rising Edge of PWROK | Low , the flash Descriptor secirity overridden HIGH , the flash Descriptor secirity effect H= Enable default L= Disable |
| GPIO49 (INT PULL/HIGH) | | DMI Termination Voltage | Rising Edge of PWROK | FOR BI=LOW FOR EAGLELAKE = HIGH(EMPTY) HALF H= Half Swing default L= Full Swing |
| SPI_MOSI_C (INT PULL/LOW) | | Integrated TPM (for ICH10) | Rising Edge of CLPWROK | H= Enable L= Disable default |
| ITPM_EN (INT PULL/HIGH) | | Integrated TPM (for GMCH) | Rising Edge of PWROK | H= Disable default L= Enable |
| DDPC_CTRLDATA | | Enable Digital port C | Rising Edge of PWROK | H= Enable L= Disable |
| SDVO_CTRL_DATA | | Enable Digital port B | Rising Edge of PWROK | H= Enable L= Disable |
| EXP_SLR | | PCI Express Static Lane Reversal | Rising Edge of PWROK | For BTX platform need reversed L= lane reversed H= Normal Default |
| -PEG_PRSNT2 | | Concurrent SDVO and PCI Express | Rising Edge of PWROK | H= Both SDVO and PCI Express L= Only SDVO or PCI Express |
| CEN | | TLS confidentiality | Rising Edge of PWROK | Support AMT need enable H= Disable TLS L= Enable TLS |
| DUALX8_EN | | 2x8 PEG port Bifurcation | Rising Edge of PWROK | H= 1x16 PCIe Port L= 2x8 PCIe Ports |
| -PEG_PRSENCE | | Enable Eaglelake PEG | Rising Edge of PWROK | H= Eaglelake PEG out L= PCIe x16 insert |

GIGABYTE TEHCHNOLOGIES , INC.

Title: Eaglelake & ICH10 for GPIO & Strap

Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0

Date: Friday, August 15, 2008 | Sheet 35 of 40

## ITE 87210 GPIO TABLE (EDS Ver:0.7v1)

| GPIO | Use Signal Name | Power | USE In/Out | ACTIVE H/L | Mark | INTERNAL/EXTERIOR PULL HIGH / LOW |
|---|---|---|---|---|---|---|
| GPIO_10 | -PFMRST2 | 5VSB | DOD8 | L | Active by LRESET# | EXT/HIGH-3.3 |
| GPIO_11 | -NB_RST | VCC | DOD8 | L | Active by LRESET# | EXT/HIGH-3.3 |
| GPIO_12 | -PCIE_RST | VCC | DOD8 | L | Active by LRESET# | EXT/HIGH-3.3 |
| GPIO_13 | PWROK1 | VCC | DOD8 | H | Active by ATXPWOK | EXT/HIGH-3.3 |
| GPIO_14 | -SIO_PECI_RQT | VCC | --- | --- | Support CPU C4& C3 mode | EXT/HIGH-3.3 |
| GPIO_15 | SVD | VCC | DOD8 | --- | no use | EXT/HIGH-5.0 |
| GPIO_16 | FU_DET2 | VCC | DIOD8 | L | Front USB cable Detect | EXT/HIGH-5.0 |
| GPIO_17 | RI2- | VCC | DI | L | COMB use | BU1/HIGH-5.0 |
| GPIO_20 | CTS2- | VCC | DO8 | L | COMB use | BU1/HIGH-5.0 |
| GPIO_21 | DCD2- | VCC | DI | L | COMB use | BU1/HIGH-5.0 |
| GPIO_22 | -BEEP | VCC | DIOD8 | L | For DRIVER BUZZER | EXT/HIGH-5.0 |
| GPIO_23 | COMB_GPI | VCC | DIOD8 | L | Front COMB cable Detect | EXT/HIGH-5.0 |
| GPIO_24 | RTS2- | VCC | DO8 | L | COMB use | BU1/HIGH-5.0 |
| GPIO_25 | DSR2- | VCC | DI | L | COMB use | BU1/HIGH-5.0 |
| GPIO_26 | TXD2 | VCC | DO8 | H | COMB use | BU1/HIGH-5.0 |
| GPIO_27 | RXD2 | VCC | DI | H | COMB use | BU1/HIGH-5.0 |
| GPIO_30 | VID0 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_31 | VID1 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_32 | VID2 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_33 | VID3 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_34 | VID4 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_35 | VID5 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_36 | FANPWM3 | VCC | DOD8 | --- | For SYSTEM FAN PWM control | EXT/HIGH-5.0 |
| GPIO_37 | FANTACH3 | VCC | DI | --- | Detect SYSTEM FAN speed | EXT/HIGH-5.0 |
| GPIO_40 | 3VSBSW- | 5VSB | DO8 | L | Control POWER LED in S3 status L=Yellow LED on H=Yellow LED off | EXT/HIGH-5.0 |
| GPIO_41 | -THERM | 5VSB | DIOD8 | L | Over Thermal alarm L=Thermal alarm H= normal | EXT/HIGH-5.0 |
| GPIO_42 | -PSON | 5VSB | DOD8 | L | For PUS power ON L=ATX power on H= normal | EXT/HIGH-5.0 |
| GPIO_43 | -PWRBTSW | 5VSB | DI | L | Power button switch iinput single Low active | EXT/HIGH-5.0 |
| GPIO_44 | -PWRBT | 5VSB | DOD8 | L | Power on output to ICH single Low active | EXT/HIGH-3.3 |
| GPIO_46 | -PWRLED_CTRL | 5VSB | DIOD8 | --- | Front LED control L=Yellow Green off H=Green LED on | EXT/HIGH-5.0 |
| GPIO_47 | VR_FAN | VCC | DIOD8 | L | CPU VRM FOR MOSFE THOT enable L=VRM HOT H=normal | EXT/HIGH-5.0 |
| GPIO_50 | FU_DET1 | VCC | DIOD8 | L | Front USB cable Detect | EXT/HIGH-5.0 |
| GPIO_51 | FANPWM2 | VCC | DOD8 | --- | For POWER FAN PWM control | EXT/HIGH-5.0 |
| GPIO_52 | FANTACH2 | VCC | DI | --- | Detect POWER FAN speed | EXT/HIGH-5.0 |
| GPIO_53 | no use | 5VSB | --- | --- | no use | EXT/HIGH-5.0 |
| GPIO_54 | -LPCPME | 5VSB | DOD8 | L | Power Management Event | EXT/HIGH-3.3 |
| GPIO_55 | -RSMRST | 5VSB | DOD8 | L | Resume Reset | EXT/HIGH-3.3 |
| GPIO_56 | MCLK | 5VSB | DIOD24 | --- | PS/2 Mouse Clock | EXT/HIGH-5.0 |
| GPIO_57 | MDAT | 5VSB | DIOD24 | --- | PS/2 Mouse Data | EXT/HIGH-5.0 |
| GPIO_60 | KCLK | 5VSB | DIOD24 | --- | PS/2 Keyboard Clock | EXT/HIGH-5.0 |
| GPIO_61 | KDAT | 5VSB | DIOD24 | --- | PS/2 Keyboard Data | EXT/HIGH-5.0 |
| GPIO_62 | -KBRST | VCC | DO16 | L | Keyboard reset | EXT/HIGH-3.3 |
| GPIO_63 | VID6 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_64 | VID7 | VCC | DIO8 | --- | for CPU VID TABLE input | EXT/HIGH-1.X |
| GPIO_65 | ITE_GPIO17 | VCC | DIOD8 | --- | forLEO connect GPIO | EXT/HIGH-5.0 |
| GPIO_66 | ITE_GPIO20 | VCC | DIOD8 | --- | forLEO connect GPIO | EXT/HIGH-5.0 |
| GPIO_67 | ITE_GPIO21 | VCC | DIOD8 | --- | forLEO connect GPIO | EXT/HIGH-5.0 |
| GPIO_70 | PD0 | VCC | DIOD24 | --- | PARALLEL PORT DATA 0 | EXT/HIGH-5.0 |
| GPIO_71 | PD1 | VCC | DIOD24 | --- | PARALLEL PORT DATA 1 | EXT/HIGH-5.0 |
| GPIO_72 | PD2 | VCC | DIOD24 | --- | PARALLEL PORT DATA 2 | EXT/HIGH-5.0 |

| GPIO | Use Signal Name | Power | USE In/Out | ACTIVE H/L | Mark | INTERNAL PULL HIGH / LOW |
|---|---|---|---|---|---|---|
| GPIO_73 | PD3 | VCC | DIOD24 | --- | PARALLEL PORT DATA 3 | EXT/HIGH-5.0 |
| GPIO_74 | PD4 | VCC | DIOD24 | --- | PARALLEL PORT DATA 3 | EXT/HIGH-5.0 |
| GPIO_75 | PD5 | VCC | DIOD24 | --- | PARALLEL PORT DATA 3 | EXT/HIGH-5.0 |
| GPIO_76 | PD6 | VCC | DIOD24 | --- | PARALLEL PORT DATA 3 | EXT/HIGH-5.0 |
| GPIO_77 | PD7 | VCC | DIOD24 | --- | PARALLEL PORT DATA 3 | EXT/HIGH-5.0 |
| GPIO_80 | SLCT | VCC | DI | H | PRINTER SELECT | EXT/HIGH-5.0 |
| GPIO_81 | PE | VCC | DI | H | PTINTER PAPER END | EXT/HIGH-5.0 |
| GPIO_82 | BUSY | VCC | DI | H | PRINTER BUSY | EXT/HIGH-5.0 |
| GPIO_83 | ACK- | VCC | DI | L | PRINTER ACKNOWLEDGE | EXT/HIGH-5.0 |
| GPIO_84 | SLIN- | VCC | DIO24 | L | PRINTER SELECT INPUT | EXT/HIGH-5.0 |
| GPIO_85 | INIT- | VCC | DIO24 | L | PRINTER INITIALIZE | EXT/HIGH-5.0 |
| GPIO_86 | AFD- | VCC | DIO24 | L | PRINTER AUTO LINE FEED | EXT/HIGH-5.0 |
| GPIO_87 | STB- | VCC | DI | L | PRINTER STROBE | EXT/HIGH-5.0 |
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## 8720PLATFORM STRAP LIST

| | Symbol | value | Description | Default setting | |
|---|---|---|---|---|---|
| JP1 Pin 38 | Flashseg1_EN | 1 | Disabled. | DEFAULT | internal ICH pull-high |
| | | 0 | Flash I/F Address Segment 1 is enabled | | |
| JP2 Pin 122 | VIDO_EN | 1 | Disable VID output pins | DEFAULT | internal AU1 pull-high |
| | | 0 | Enable VID output pins | | |
| JP3 Pin 124 | CHIP_SEL | | Chip selection in Configuration | | internal AU1 pull-high |
| JP4 Pin 126 | K8PWR_EN | 1 | K8 power sequence function is enabled | | |
| | | 0 | K8 power sequence function is disabled | DEFAULT | EXIT resistor pull-down |
| JP3 & JP5 Pin 124 & 46 | FAN_CTL_SEL | 11 | The default value of EC Index 15h/16h/17h is 00h | | |
| | | 10 | The default value of EC Index 15h/16h/17h is 40h | DEFAULT | |
| | | 01 | The default value of EC Index 15h/16h/17h is 20h | | |
| | | 00 | The default value of EC Index 15h/16h/17h is 7Fh | | |
| JP5 Pin46 | WDT_EN | 1 | Disable WDT to rest PWROK | | |
| | | 0 | Enable WDT to rest PWROK | DEFAULT | EXIT resistor pull-down |
| JP6 Pin29 | SVID_EN | 1 | Disable SVID Function | DEFAULT | internal BU1 pull-high |
| | | 0 | Enable SVID Function | | |

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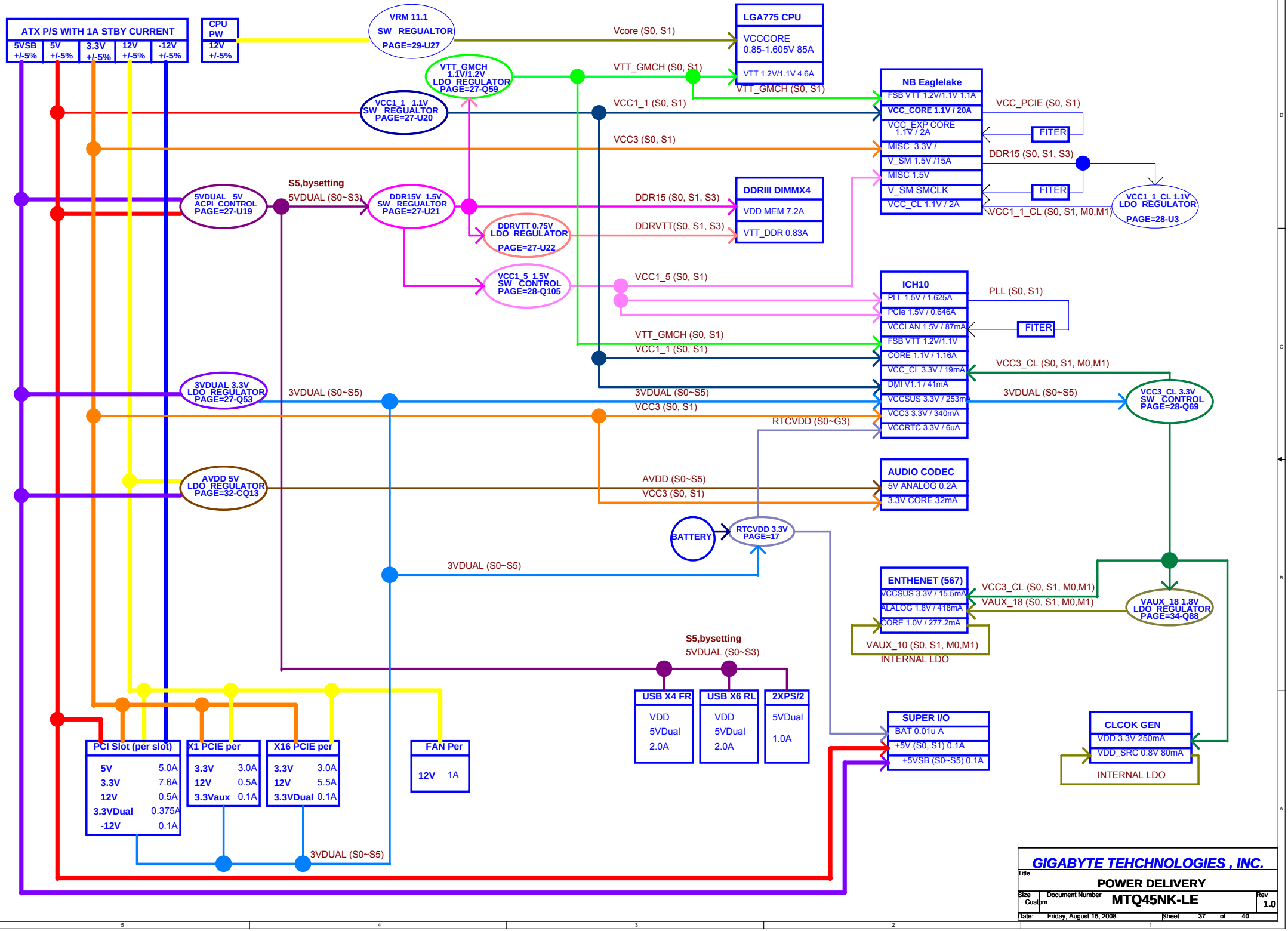
Title: Other GPIO LIST & STRAP

Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0

Date: Friday, August 15, 2008 | Sheet 36 of 40

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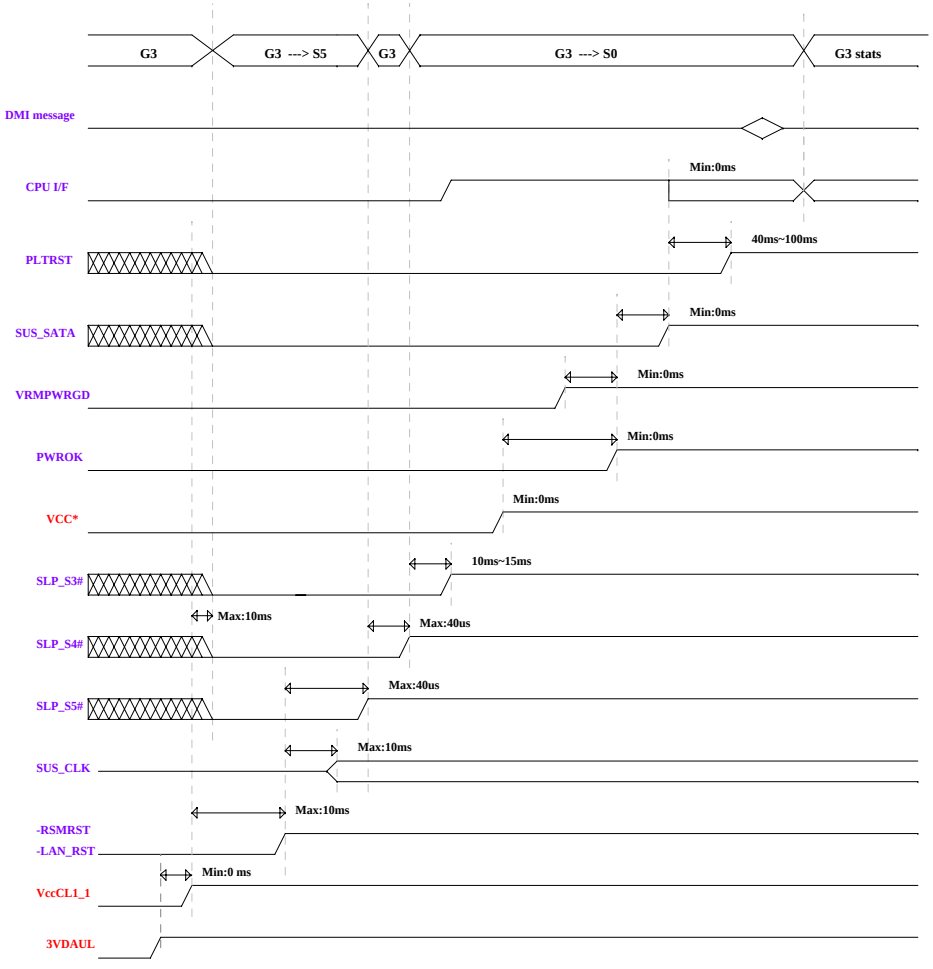
| | | |
|---|---|---|
| Title | POWER DELIVERY | |
| Size: Custom | Document Number: MTQ45NK-LE | Rev: 1.0 |
| Date: Friday, August 15, 2008 | Sheet 37 of 40 | |

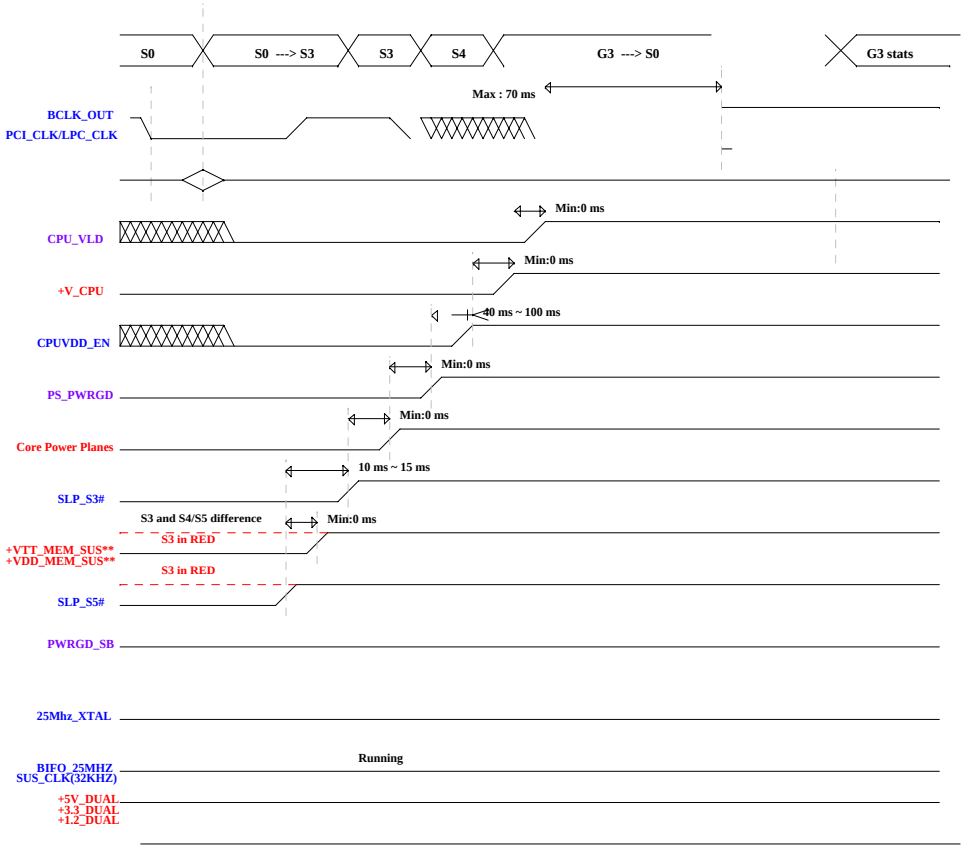
# G3-tO-S0 Power Sequence




**Power Planes in Red** **Motherboard generated signals in Purple**

**VCC* includes** **VCC1_5** **VCC3** **VCC1_1** **VTT_GMCH** **V5REF**

# S3/S4/S5 to S0 Resume Sequence




**Power Planes in Red**

**Motherboard generated signals in Purple**

| | | | |
|---|---|---|---|
| GIGABYTE TEHCHNOLOGIES , INC. | | | |
| Title: POWER SEQUENCE | | | |
| Size: C | Document Number: MTQ45NK-LE | | Rev: 1.0 |
| Date: Friday, August 15, 2008 | | Sheet 38 of 40 | |

GIGABYTE TEHCHNOLOGIES , INC.

Title: RESET&PWROK&CLOCK DELIVERY

Size: C | Document Number: MTQ45NK-LE | Rev: 1.0

Date: Friday, August 15, 2008 | Sheet 39 of 40

# Model Name:MTQ45NK-LE

# Version:1.0

## Component value change history

| Data | Change Item | Reason |
|---|---|---|
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## Circuit or PCB layout change for next version

| DATE | Change Item | Reason |
|---|---|---|
| 01/22 | change SPEK out circuit for LE spec | |
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Title: BOM & PCB MODIFY HISTORY

Size: C | Document Number: MTQ45NK-LE | Rev: 1.0

Date: Friday, August 15, 2008 | Sheet 40 of 40