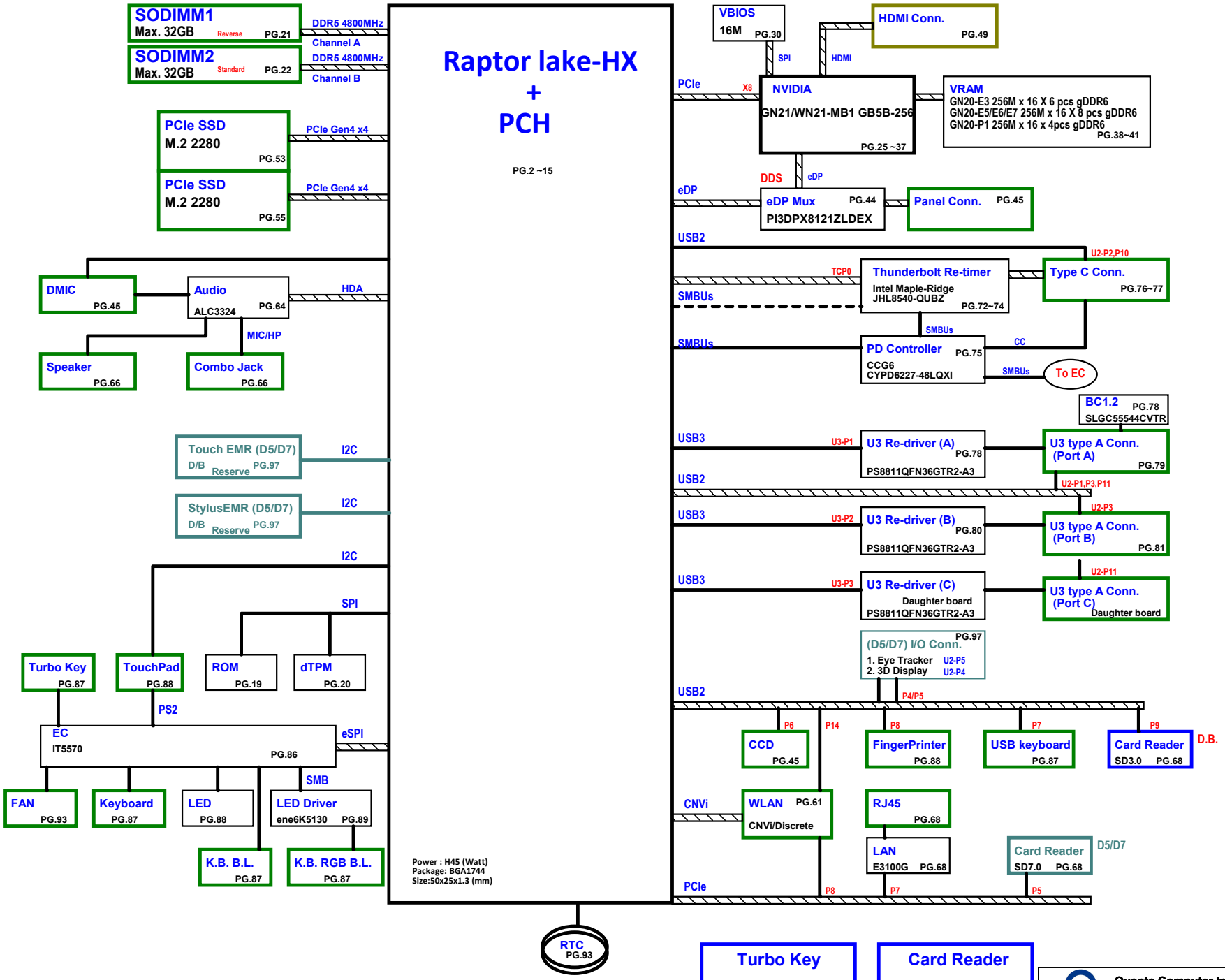
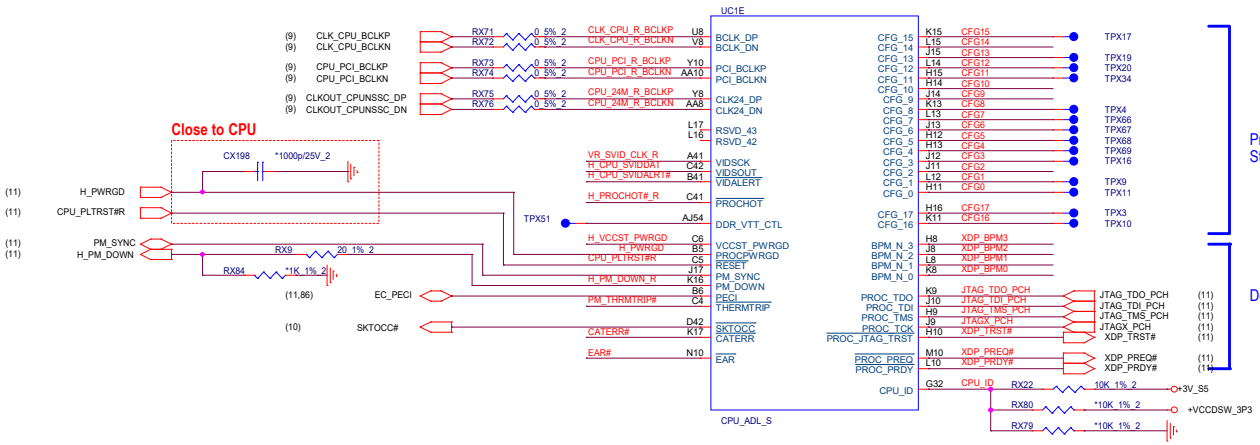
2023 RPL Block Diagram (Roadster - ZGRC/ ZGRE)



Quanta Computer Inc.
PROJECT : Helios(ZGRC)
BLOCK DIAGRAM
Rev 1A
Date: Wednesday, February 15, 2023 Sheet 1 of 149

+VCC_CFG_PU_OUT (3)
+VCCTP05_PROC (5,11,12,141,145)

Host CLK:
Trace length < 8976 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm



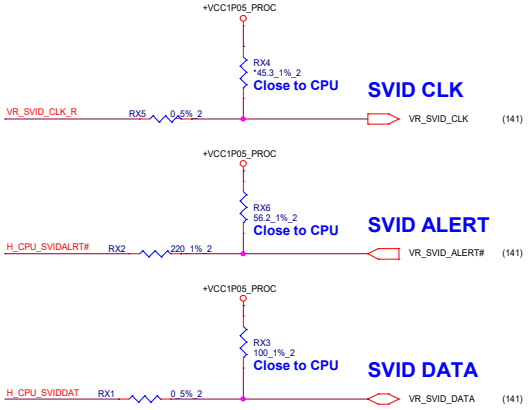
CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

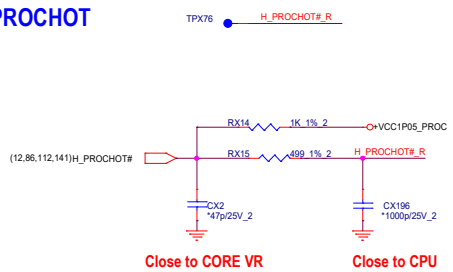
H_PWRGD (50ohm)
Trace Length: <12007 mils

CPU_PLTRST# (50ohm)
Trace Length: <12007 mils

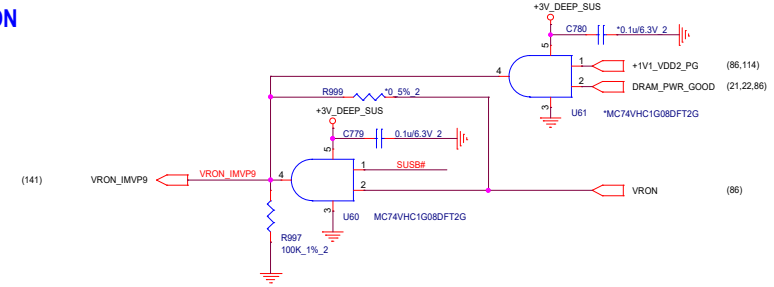
PM_SYNC (50ohm)
Trace Length: 3700~12007 mils



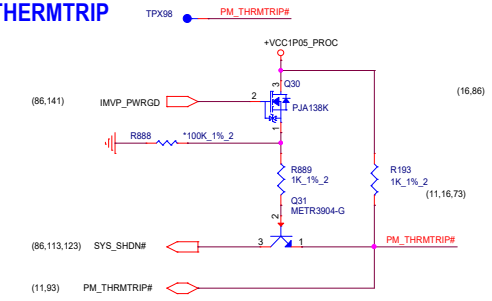
PROCHOT



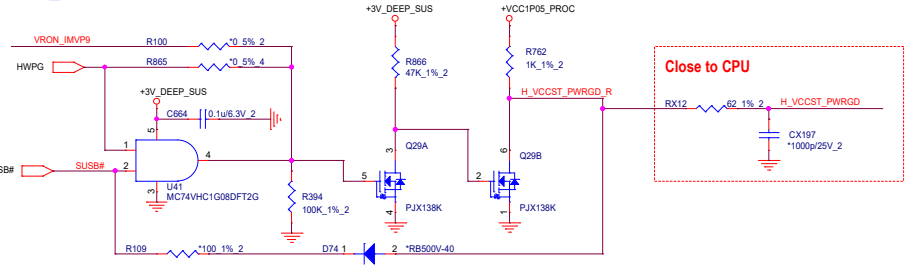
VRON



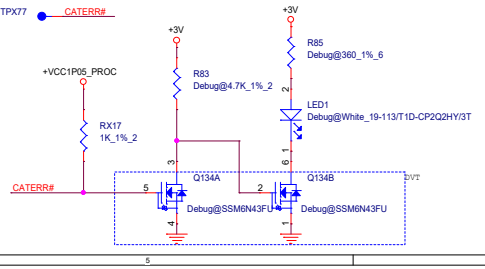
THERMTRIP



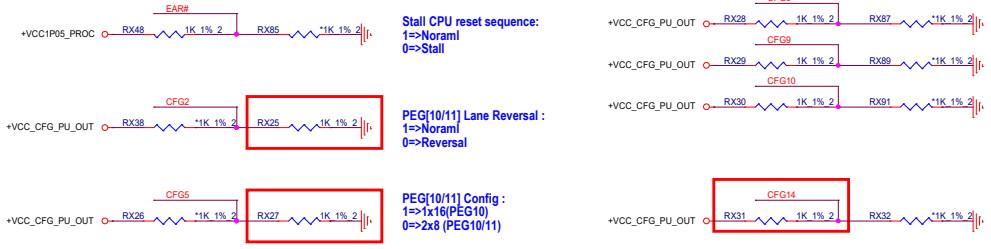
VCCST_PWRGD



CATERR



CFG



Quanta Computer Inc.
PROJECT : Helios(ZGRC)
Size | Document Number: ADL-HX 1/7 (JTAG/MISC) | Rev 1A
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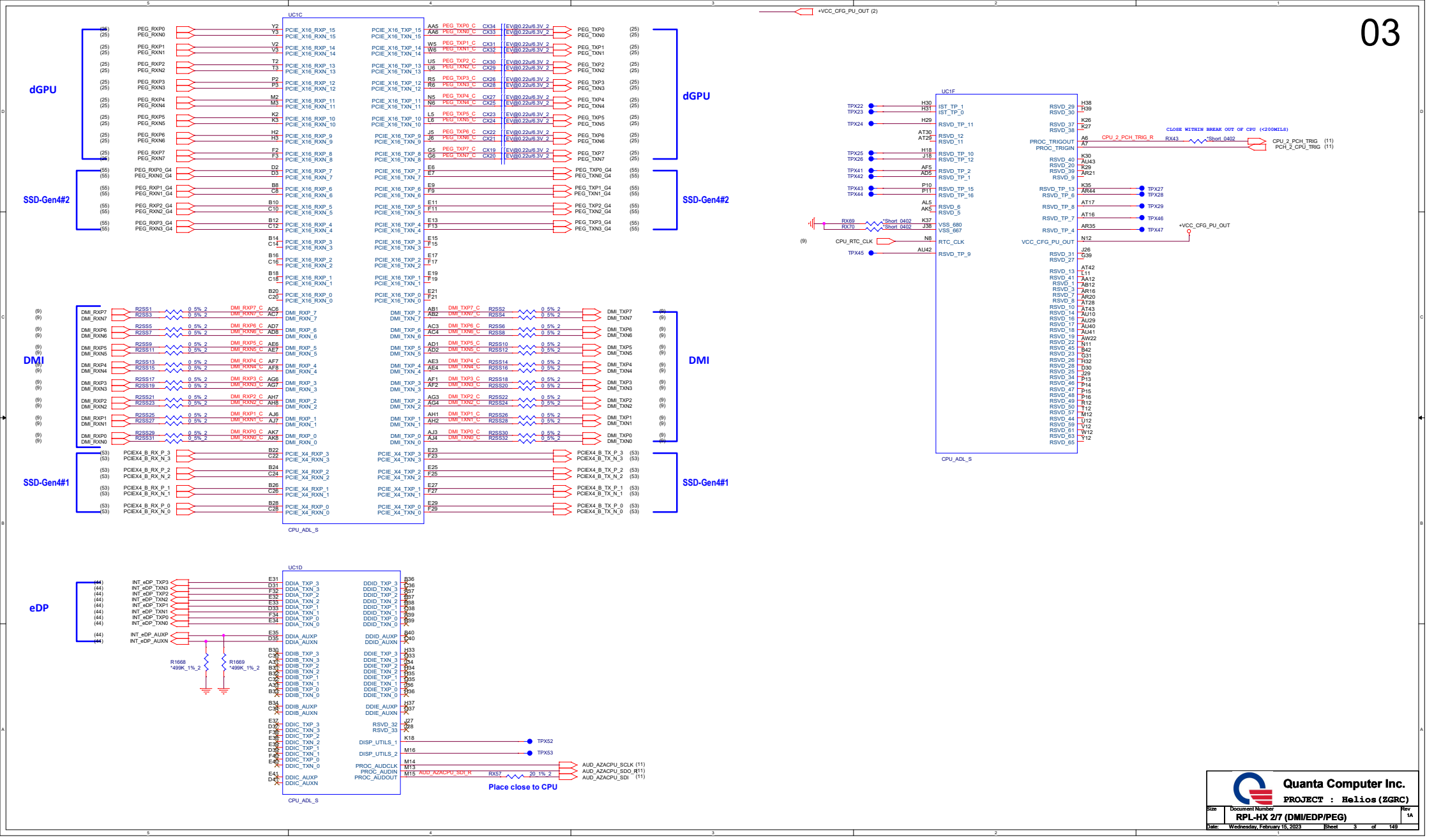

Quanta Computer Inc.	
PROJECT : Helios(ZGRC)	
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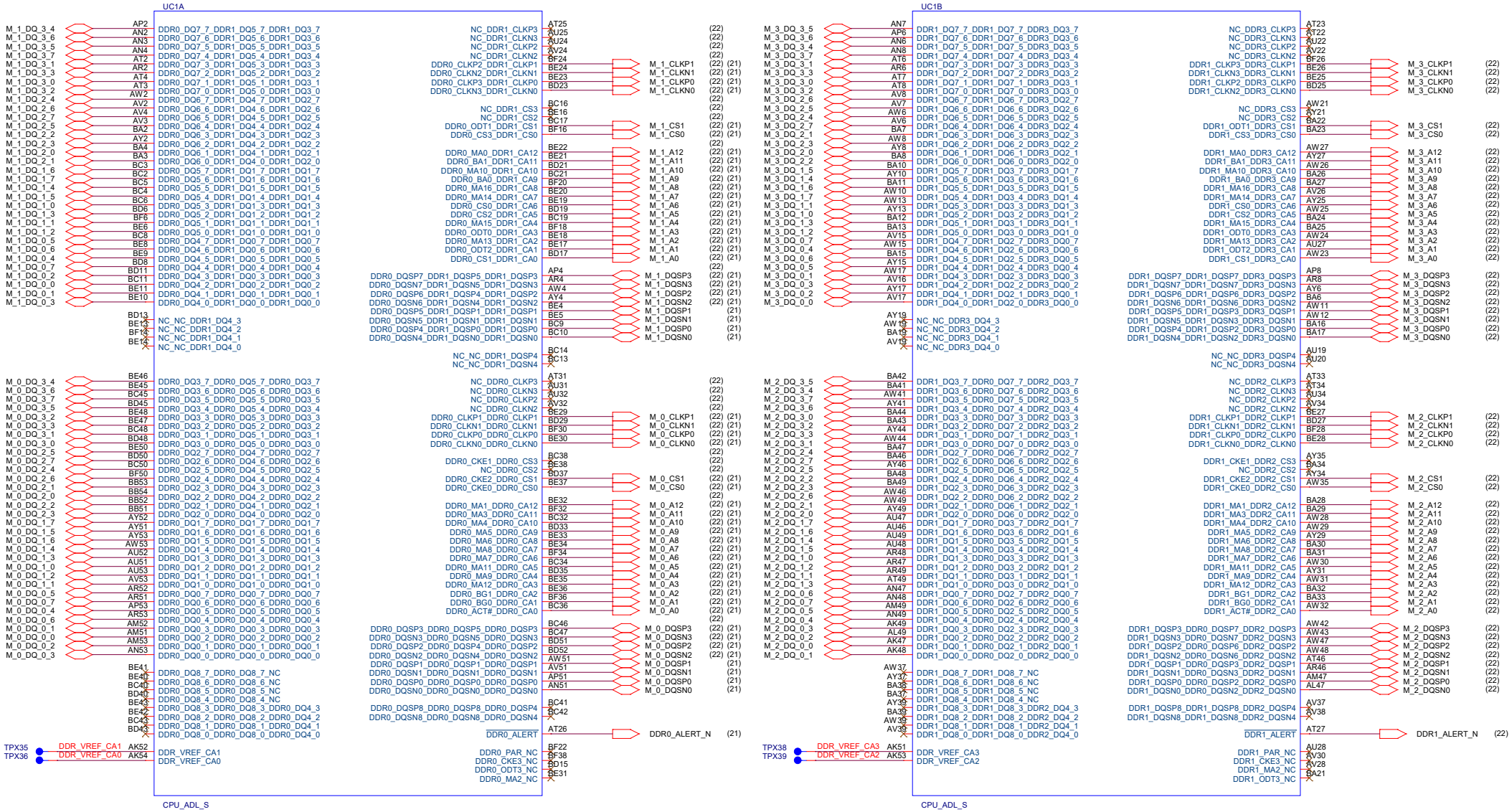
Interleave / butterfly



Quanta Computer Inc.
PROJECT : Helios(ZGRC)

Size	Document Number	Rev
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+VCCIN_AUX (7,143)
+VCC_GT (7,141,142)
+1V1_VDD2 (7,11,114,131)
+VCC1P8_PROC (16,123)
+VCC1P05_PROC (2,11,12,141,145)

ADL-HX Processor (POWER)

05

ESD Close to CPU Side

+VCC_CORE: D20006 *MESD11LH5.0CT5G
+1V1_VDD2: D20007 *MESD11LH5.0CT5G
+VCC_GT: D20008 *MESD11LH5.0CT5G
+VCC1P8_PROC: D20009 *MESD11LH5.0CT5G
+VCCIN_AUX: D20010 *MESD11LH5.0CT5G
+VCC1P05_PROC: D20011 *MESD11LH5.0CT5G

JS-SI-1202 change to MESD11LH5.0CT5G(BCD11LH5Z00)
JS-PV-0104 Change FP to esd-0_61x0_31-2p

EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX

+VCCIN_AUX
CX40 8.2p/50V_2
CX38 8.2p/50V_2
CX39 10p/25V_2
CX37 10p/25V_2

+VCCIN_AUX_FLTR
CX195 47u/6.3V_6

+VCC1P05_PROC
CX237 1u/25V_4
CX238 1u/25V_4
CX239 *1u/25V_4
CX240 *1u/25V_4

+VCC1P8_PROC
CX244 22u/6.3V_6
CX241 22u/6.3V_6
CX242 *1u/25V_4
CX243 *1u/25V_4

+1V1_VDD2

UC1G

AP44	VCCIN_AUX_13	VCC1P05_PROC_1	R8
AP43	VCCIN_AUX_12	VCC1P05_PROC_2	R9
AP42	VCCIN_AUX_11		
AN45	VCCIN_AUX_10	VCCGT_62	AH54
AN44	VCCIN_AUX_9	VCCGT_61	AH53
AN43	VCCIN_AUX_8	VCCGT_60	AH52
AN42	VCCIN_AUX_7	VCCGT_59	AH51
AM45	VCCIN_AUX_6	VCCGT_58	AH50
AM44	VCCIN_AUX_5	VCCGT_57	AH49
AL45	VCCIN_AUX_4	VCCGT_56	AH48
AL44	VCCIN_AUX_3	VCCGT_55	AH47
AK45	VCCIN_AUX_2	VCCGT_54	AH46
AK44	VCCIN_AUX_1	VCCGT_53	AH45
P24	VCCIN_AUX_48	VCCGT_52	AH44
P23	VCCIN_AUX_47	VCCGT_51	AG54
P21	VCCIN_AUX_46	VCCGT_50	AG52
P20	VCCIN_AUX_45	VCCGT_49	AG50
N24	VCCIN_AUX_44	VCCGT_48	AG48
N23	VCCIN_AUX_43	VCCGT_47	AG46
N22	VCCIN_AUX_42	VCCGT_46	AG44
N21	VCCIN_AUX_41	VCCGT_45	AF54
N20	VCCIN_AUX_40	VCCGT_44	AF53
N19	VCCIN_AUX_39	VCCGT_43	AF52
N18	VCCIN_AUX_38	VCCGT_42	AF51
M24	VCCIN_AUX_37	VCCGT_41	AF50
M23	VCCIN_AUX_36	VCCGT_40	AF49
M21	VCCIN_AUX_35	VCCGT_39	AF48
M20	VCCIN_AUX_34	VCCGT_38	AF47
R26	VCCIN_AUX_FLTR_5	VCCGT_37	AF46
P26	VCCIN_AUX_FLTR_4	VCCGT_36	AF45
N26	VCCIN_AUX_FLTR_3	VCCGT_35	AF44
M26	VCCIN_AUX_FLTR_2	VCCGT_34	AE54
L26	VCCIN_AUX_FLTR_1	VCCGT_33	AE52
		VCCGT_32	AE50
		VCCGT_31	AE48
V11		VCCGT_30	AE46
V10	VCC1P05_PROC_7	VCCGT_29	AE44
U11	VCC1P05_PROC_6	VCCGT_28	AD54
U10	VCC1P05_PROC_5	VCCGT_27	AD53
T11	VCC1P05_PROC_4	VCCGT_26	AD52
	VCC1P05_PROC_3	VCCGT_25	AD51
		VCCGT_24	AD50
AL1		VCCGT_23	AD49
AK2	VCC1P8_PROC_3	VCCGT_22	AD48
	VCC1P8_PROC_2	VCCGT_21	AD47
BD38		VCCGT_20	AD46
BD36	VDD2_22	VCCGT_19	AD45
BD34	VDD2_21	VCCGT_18	AD44
BD32	VDD2_20	VCCGT_17	AC54
BD31	VDD2_19	VCCGT_16	AC52
BD22	VDD2_18	VCCGT_15	AC50
BD20	VDD2_17	VCCGT_14	AC48
BD18	VDD2_16	VCCGT_13	AC46
BD16	VDD2_15	VCCGT_12	AC44
BC30	VDD2_14		
BC29	VDD2_13	RSVD_35	J31
BC28	VDD2_12	RSVD_15	AT44
BC27	VDD2_11		
BC26	VDD2_10	B4	VCCST_PWRGD_SX
BC25	VDD2_9		
BC24	VDD2_8	AJ52	VCCGT_SENSE
BC23	VDD2_7	AJ53	VSSGT_SENSE
	VDD2_6		
		H26	VCCIN_AUX_SENSE
		H27	VSSIN_AUX_SENSE
		T10	VCC1P05_PROC_SENSE
		AL2	RSVD_TP_3
		BC31	VDD2_DDR5_SENSE

VCCST_PWRGD_SX → RX77 *Short_0201 → VCCST_OVERRIDE (11,16)
VCCGT_SENSE → VCCGT_SENSE (141)
VSSGT_SENSE → VSSGT_SENSE (141)
VCCIN_AUX_SENSE → VCC_AUX_SENSE (143)
VSSIN_AUX_SENSE → VSS_AUX_SENSE (143)
VCC1P05_PROC_SENSE → VCC1P05_PROC_SENSE (145)
RSVD_TP_3 → RSVD_TP_3 → TPX50
VDD2_DDR5_SENSE → VR_VCCDD2_SENSE (114)

CPU_ADL_S

EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX

+VCCIN_AUX
CX36 8.2p/50V_2
CX35 10p/25V_2

+VCC1P8_PROC
+1V1_VDD2

UC1Q

M19	VCCIN_AUX_33	VCCGT_11	AB54
L24	VCCIN_AUX_32	VCCGT_10	AB53
L23	VCCIN_AUX_31	VCCGT_9	AB52
L22	VCCIN_AUX_30	VCCGT_8	AB51
L21	VCCIN_AUX_29	VCCGT_7	AB50
L20	VCCIN_AUX_28	VCCGT_6	AB49
K24	VCCIN_AUX_27	VCCGT_5	AB48
K23	VCCIN_AUX_26	VCCGT_4	AB47
K21	VCCIN_AUX_25	VCCGT_3	AB46
K20	VCCIN_AUX_24	VCCGT_2	AB45
J24	VCCIN_AUX_23	VCCGT_1	AB44
J23	VCCIN_AUX_22		
J22	VCCIN_AUX_21	RSVD_21	AU44
J21	VCCIN_AUX_20	RSVD_36	J32
J20	VCCIN_AUX_19		
H24	VCCIN_AUX_18		
H23	VCCIN_AUX_17		AA13
H22	VCCIN_AUX_16	RSVD_2	AB13
H21	VCCIN_AUX_15	RSVD_4	R13
H20	VCCIN_AUX_14	RSVD_51	R14
		RSVD_52	R15
AK1	VCC1P8_PROC_1	RSVD_53	R16
		RSVD_54	R17
AR27		RSVD_55	R18
AP27	VDD2_5	RSVD_56	T13
AP26	VDD2_4	RSVD_58	U13
AN27	VDD2_3	RSVD_60	V13
AN26	VDD2_2	RSVD_62	W13
	VDD2_1	RSVD_64	Y13
		RSVD_66	
AR42	RSVD_TP_5		
K38	RSVD_TP_14		
C43	RSVD_24		

TPX48 → RSVD_TP_5
TPX49 → RSVD_TP_14

CPU_ADL_S

Quanta Computer Inc.
PROJECT : Helios(ZGRC)

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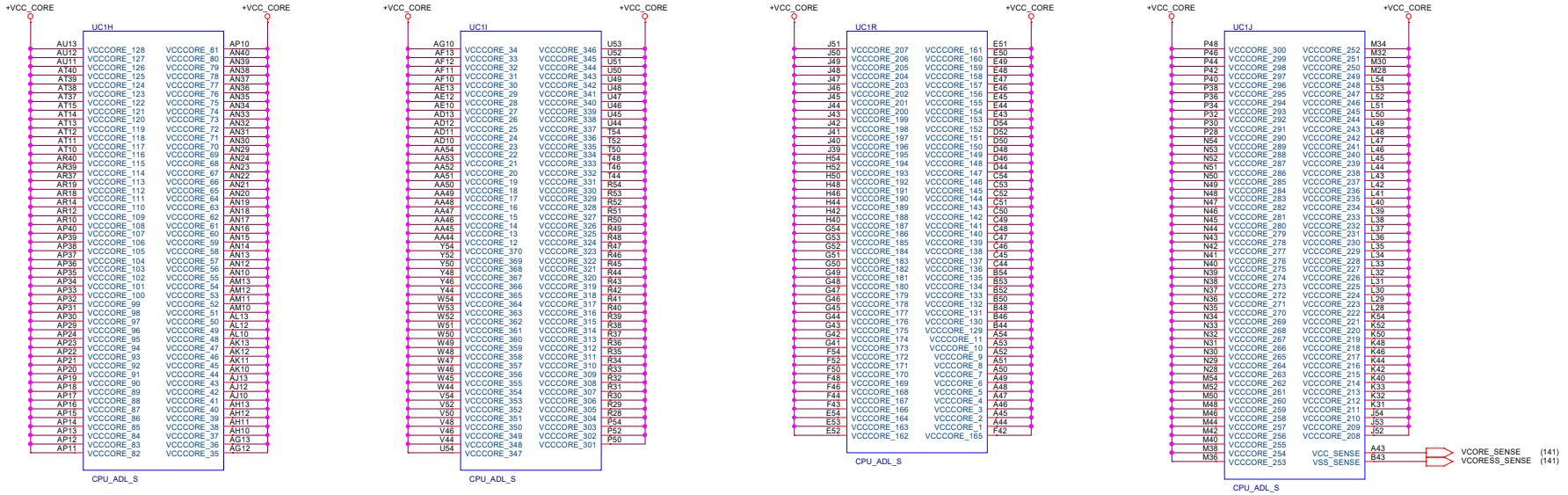
ADL-HX Processor (POWER)

+VCC_CORE (5,7,141,142)



Quanta Computer Inc.

PROJECT : Helios(ZGRC)

Size	Document Number	Rev
	RPL-HX 5/7 (POWER)	1A

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+VCC_CORE (5,6,141,142)
+VCC_GT (5,141,142)
+VCCIN_AUX (5,143)

+VCC_CORE

4x330uF

PC9845 330u/2V_7343H2.22
PC9846 330u/2V_7343H2.22
PC9847 *330u/2V_7343H2.22
PC9848 *330u/2V_7343H2.22

Define to Power , Stuff 2pcs under CPU

7x47uF 0603,

CX169 47u/6.3V_6
CX170 47u/6.3V_6
CX171 47u/6.3V_6
CX172 47u/6.3V_6
CX173 47u/6.3V_6
CX174 47u/6.3V_6
CX175 47u/6.3V_6

3x Placeholder 0603,

CX41 *47u/6.3V_6
CX141 *47u/6.3V_6
CX142 *47u/6.3V_6

15x22uF 0603, (PUG 0402)

CX62 22u/6.3V_6
CX203 22u/6.3V_6
CX204 22u/6.3V_6
CX205 22u/6.3V_6
CX206 22u/6.3V_6
CX207 22u/6.3V_6
CX208 22u/6.3V_6
CX209 22u/6.3V_6
CX210 22u/6.3V_6
CX211 22u/6.3V_6
CX212 22u/6.3V_6
CX213 22u/6.3V_6
CX214 22u/6.3V_6
CX215 22u/6.3V_6

10x placeholder 0402, placement CPU side

CX179 *10u/6.3V_4
CX180 *10u/6.3V_4
CX181 *10u/6.3V_4
CX182 *10u/6.3V_4
CX183 *10u/6.3V_4
CX184 *10u/6.3V_4
CX185 *10u/6.3V_4
CX186 *10u/6.3V_4
CX187 *10u/6.3V_4
CX245 *10u/6.3V_4

+VCCIN_AUX

5x47uF 0603,

CX70 47u/6.3V_6
CX71 47u/6.3V_6
CX72 47u/6.3V_6
CX73 47u/6.3V_6
CX56 47u/6.3V_6

6x10uF 0402,

CX60 10u/6.3V_4
CX61 10u/6.3V_4
CX246 10u/6.3V_4
CX247 10u/6.3V_4
CX248 10u/6.3V_4
CX249 10u/6.3V_4

4x placeholder 0402, placement bottom side

CX63 *10u/6.3V_4
CX64 *10u/6.3V_4
CX65 *10u/6.3V_4
CX66 *10u/6.3V_4

+VCCIN_AUX

For RF

CX257 8.2p/50V_2
CX258 8.2p/50V_2
CX259 8.2p/50V_2
CX260 8.2p/50V_2
CX261 8.2p/50V_2
CX262 8.2p/50V_2

+VCC_CORE

CX263 8.2p/50V_2
CX264 8.2p/50V_2
CX265 8.2p/50V_2
CX266 8.2p/50V_2
CX267 8.2p/50V_2
CX268 8.2p/50V_2

+VCC_GT

2x47uF 0603,placement TOP side

CX177 47u/6.3V_6
CX178 47u/6.3V_6

6x10uF 0402,placement TOP side

CX150 10u/6.3V_4
CX151 10u/6.3V_4
CX152 10u/6.3V_4
CX153 10u/6.3V_4
CX154 10u/6.3V_4
CX155 10u/6.3V_4

3x 0603 placeholder , placement CPU side

CX218 47u/6.3V_6
CX219 47u/6.3V_6
CX220 47u/6.3V_6

DVT

CX276 22u/6.3V_6
CX277 22u/6.3V_6
CX278 22u/6.3V_6
CX279 22u/6.3V_6
CX280 22u/6.3V_6
CX281 22u/6.3V_6

6x22uF 0603,placement BOT side

+1V1_VDD2

CX269 10u/6.3V_4
CX270 10u/6.3V_4
CX271 10u/6.3V_4
CX272 10u/6.3V_4
CX273 10u/6.3V_4
CX274 *22u/6.3V_6
CX275 *22u/6.3V_6

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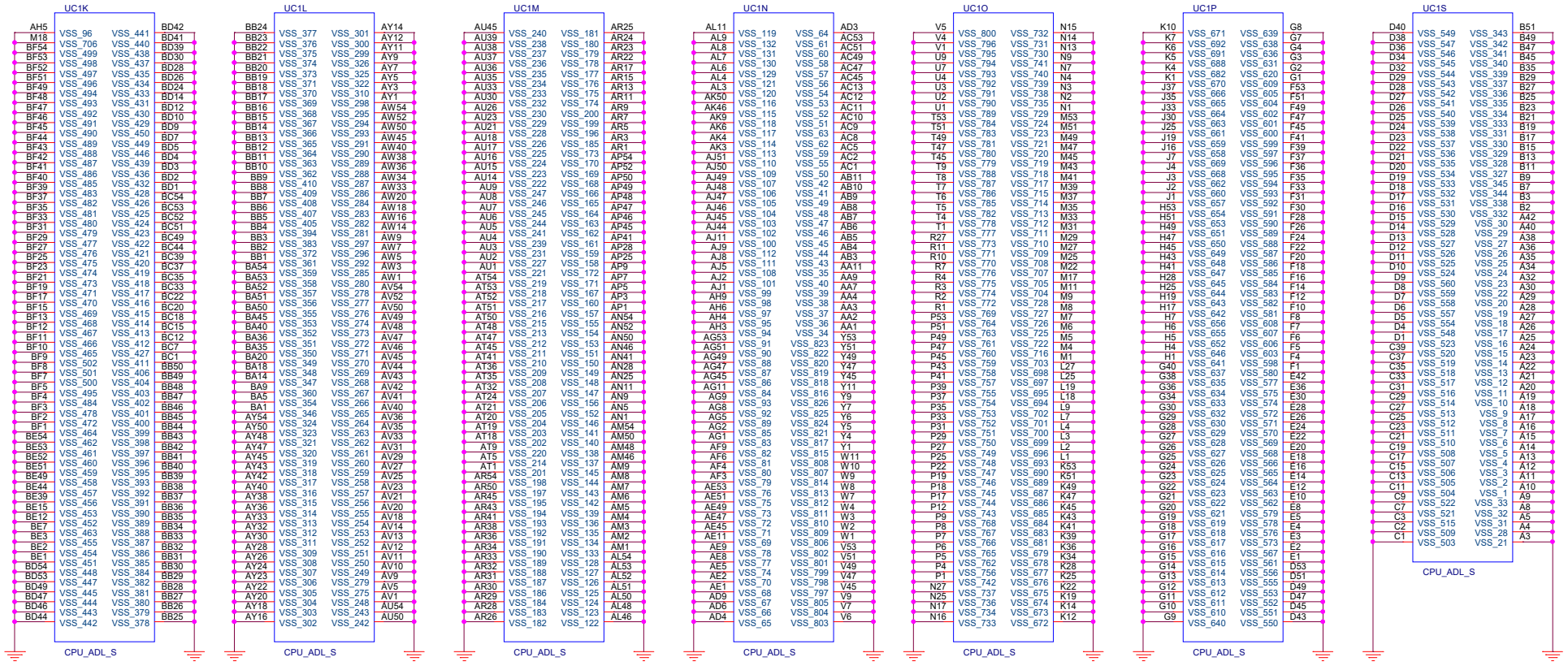
ADL-HX



Quanta Computer Inc.		
PROJECT : Helios(ZGRC)		
Size	Document Number: RPL-HX 7/7 (GND)	Rev: 1A
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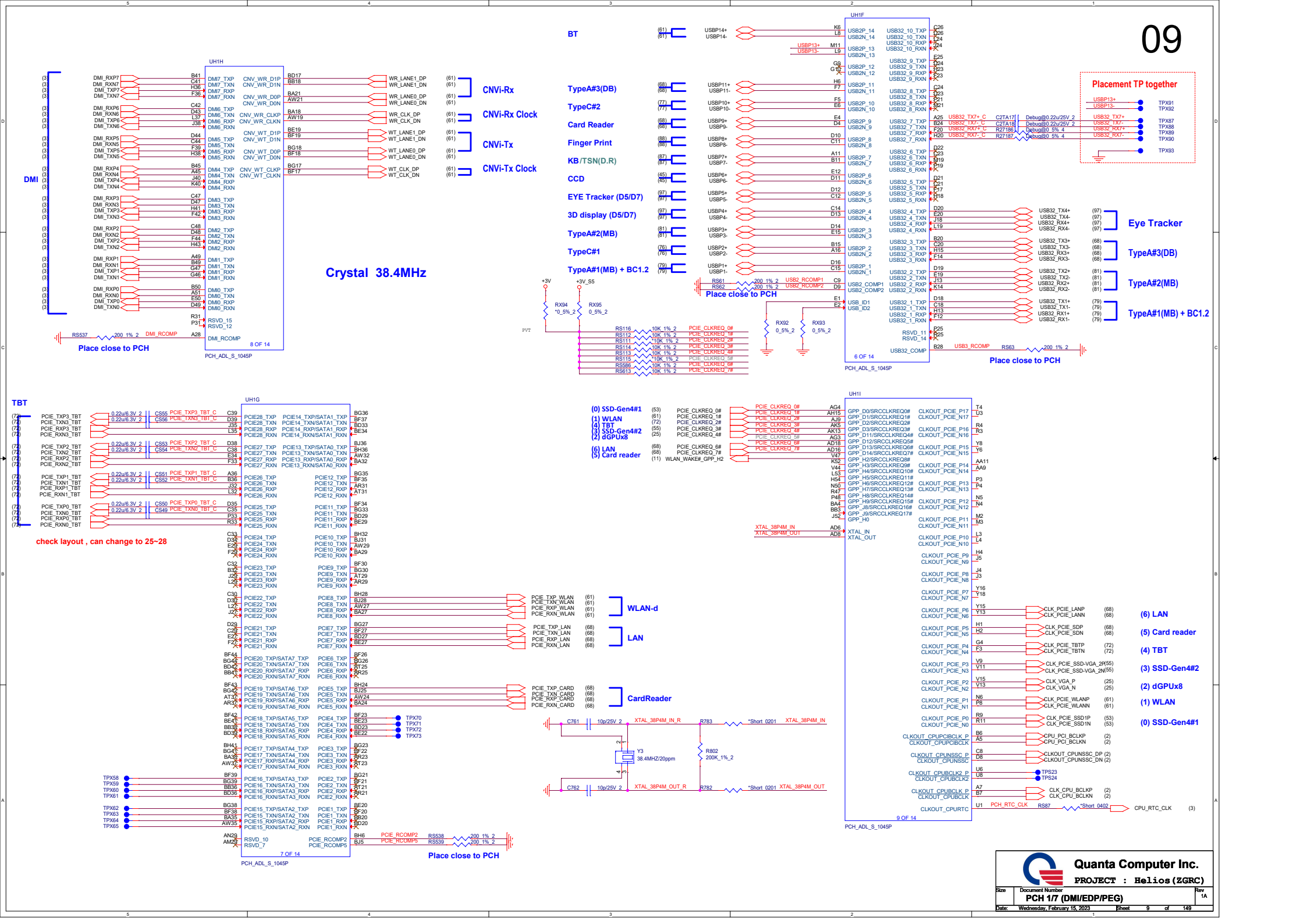
09
DMI
UH1H
DMI7_TXP
DMI7_TXN
DMI7_RXP
DMI7_RXN
DMI6_TXP
DMI6_TXN
DMI6_RXP
DMI6_RXN
DMI5_TXP
DMI5_TXN
DMI5_RXP
DMI5_RXN
DMI4_TXP
DMI4_TXN
DMI4_RXP
DMI4_RXN
DMI3_TXP
DMI3_TXN
DMI3_RXP
DMI3_RXN
DMI2_TXP
DMI2_TXN
DMI2_RXP
DMI2_RXN
DMI1_TXP
DMI1_TXN
DMI1_RXP
DMI1_RXN
DMI0_TXP
DMI0_TXN
DMI0_RXP
DMI0_RXN
RSVD_15
RSVD_12
DMI_RCOMP
8 OF 14
PCH_ADL_S_1045P
CNV_WR_D1P
CNV_WR_D1N
CNV_WR_D0P
CNV_WR_D0N
CNV_WR_CLKP
CNV_WR_CLKN
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_D0P
CNV_WT_D0N
CNV_WT_CLKP
CNV_WT_CLKN
WR_LANE1_DP
WR_LANE1_DN
WR_LANE0_DP
WR_LANE0_DN
WR_CLK_DP
WR_CLK_DN
WT_LANE1_DP
WT_LANE1_DN
WT_LANE0_DP
WT_LANE0_DN
WT_CLK_DP
WT_CLK_DN
CNVi-Rx
CNVi-Rx Clock
CNVi-Tx
CNVi-Tx Clock
RS537
200_1%_2
DMI_RCOMP
Place close to PCH
Crystal 38.4MHz
BT
TypeA#3(DB)
TypeC#2
Card Reader
Finger Print
KB/TSN(D.R)
CCD
EYE Tracker (D5/D7)
3D display (D5/D7)
TypeA#2(MB)
TypeC#1
TypeA#1(MB) + BC1.2
UH1F
USB2P_14
USB2N_14
USB2P_13
USB2N_13
USB2P_12
USB2N_12
USB2P_11
USB2N_11
USB2P_10
USB2N_10
USB2P_9
USB2N_9
USB2P_8
USB2N_8
USB2P_7
USB2N_7
USB2P_6
USB2N_6
USB2P_5
USB2N_5
USB2P_4
USB2N_4
USB2P_3
USB2N_3
USB2P_2
USB2N_2
USB2P_1
USB2N_1
USB_ID1
USB_ID2
USB2_COMP1
USB2_COMP2
USB32_10_TXP
USB32_10_TXN
USB32_10_RXP
USB32_10_RXN
USB32_9_TXP
USB32_9_TXN
USB32_9_RXP
USB32_9_RXN
USB32_8_TXP
USB32_8_TXN
USB32_8_RXP
USB32_8_RXN
USB32_7_TXP
USB32_7_TXN
USB32_7_RXP
USB32_7_RXN
USB32_6_TXP
USB32_6_TXN
USB32_6_RXP
USB32_6_RXN
USB32_5_TXP
USB32_5_TXN
USB32_5_RXP
USB32_5_RXN
USB32_4_TXP
USB32_4_TXN
USB32_4_RXP
USB32_4_RXN
USB32_3_TXP
USB32_3_TXN
USB32_3_RXP
USB32_3_RXN
USB32_2_TXP
USB32_2_TXN
USB32_2_RXP
USB32_2_RXN
USB32_1_TXP
USB32_1_TXN
USB32_1_RXP
USB32_1_RXN
RSVD_11
RSVD_14
USB32_COMP
6 OF 14
PCH_ADL_S_1045P
USB32_TX4+
USB32_TX4-
USB32_RX4+
USB32_RX4-
USB32_TX3+
USB32_TX3-
USB32_RX3+
USB32_RX3-
USB32_TX2+
USB32_TX2-
USB32_RX2+
USB32_RX2-
USB32_TX1+
USB32_TX1-
USB32_RX1+
USB32_RX1-
USB3_RCOMP
RS63
Eye Tracker
TypeA#3(DB)
TypeA#2(MB)
TypeA#1(MB) + BC1.2
Placement TP together
TPX91
TPX92
TPX87
TPX88
TPX89
TPX90
TPX93
Place close to PCH
RS61
RS62
USB2_RCOMP1
USB2_RCOMP2
+3V
+3V_S5
RX94
RX95
RX92
RX93
RS116
RS112
RS111
RS114
RS113
RS115
RS586
RS613
PCIE_CLKREQ_0#
PCIE_CLKREQ_1#
PCIE_CLKREQ_2#
PCIE_CLKREQ_3#
PCIE_CLKREQ_4#
PCIE_CLKREQ_5#
PCIE_CLKREQ_6#
PCIE_CLKREQ_7#
TBT
PCIE_TXP3_TBT
PCIE_TXN3_TBT
PCIE_RXP3_TBT
PCIE_RXN3_TBT
PCIE_TXP2_TBT
PCIE_TXN2_TBT
PCIE_RXP2_TBT
PCIE_RXN2_TBT
PCIE_TXP1_TBT
PCIE_TXN1_TBT
PCIE_RXP1_TBT
PCIE_RXN1_TBT
PCIE_TXP0_TBT
PCIE_TXN0_TBT
PCIE_RXP0_TBT
PCIE_RXN0_TBT
check layout , can change to 25~28
UH1G
PCIE28_TXP
PCIE28_TXN
PCIE28_RXP
PCIE28_RXN
PCIE27_TXP
PCIE27_TXN
PCIE27_RXP
PCIE27_RXN
PCIE26_TXP
PCIE26_TXN
PCIE26_RXP
PCIE26_RXN
PCIE25_TXP
PCIE25_TXN
PCIE25_RXP
PCIE25_RXN
PCIE24_TXP
PCIE24_TXN
PCIE24_RXP
PCIE24_RXN
PCIE23_TXP
PCIE23_TXN
PCIE23_RXP
PCIE23_RXN
PCIE22_TXP
PCIE22_TXN
PCIE22_RXP
PCIE22_RXN
PCIE21_TXP
PCIE21_TXN
PCIE21_RXP
PCIE21_RXN
PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN
PCIE18_TXP/SATA5_TXP
PCIE18_TXN/SATA5_TXN
PCIE18_RXP/SATA5_RXP
PCIE18_RXN/SATA5_RXN
PCIE17_TXP/SATA4_TXP
PCIE17_TXN/SATA4_TXN
PCIE17_RXP/SATA4_RXP
PCIE17_RXN/SATA4_RXN
PCIE16_TXP/SATA3_TXP
PCIE16_TXN/SATA3_TXN
PCIE16_RXP/SATA3_RXP
PCIE16_RXN/SATA3_RXN
PCIE15_TXP/SATA2_TXP
PCIE15_TXN/SATA2_TXN
PCIE15_RXP/SATA2_RXP
PCIE15_RXN/SATA2_RXN
RSVD_10
RSVD_7
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PCH_ADL_S_1045P
PCIE_RCOMP2
PCIE_RCOMP5
RS538
RS539
Place close to PCH
PCIE_TXP_WLAN
PCIE_TXN_WLAN
PCIE_RXP_WLAN
PCIE_RXN_WLAN
WLAN-d
PCIE_TXP_LAN
PCIE_TXN_LAN
PCIE_RXP_LAN
PCIE_RXN_LAN
LAN
PCIE_TXP_CARD
PCIE_TXN_CARD
PCIE_RXP_CARD
PCIE_RXN_CARD
CardReader
TPX70
TPX71
TPX72
TPX73
TPX58
TPX59
TPX60
TPX61
TPX62
TPX63
TPX64
TPX65
(0) SSD-Gen4#1
(1) WLAN
(4) TBT
(3) SSD-Gen4#2
(2) dGPUx8
(6) LAN
(5) Card reader
WLAN_WAKE#_GPP_H2
UH1I
GPP_D0/SRCCLKREQ0#
GPP_D1/SRCCLKREQ1#
GPP_D2/SRCCLKREQ2#
GPP_D3/SRCCLKREQ3#
GPP_D11/SRCCLKREQ4#
GPP_D12/SRCCLKREQ5#
GPP_D13/SRCCLKREQ6#
GPP_D14/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
GPP_J8/SRCCLKREQ16#
GPP_J9/SRCCLKREQ17#
GPP_H0
XTAL_IN
XTAL_OUT
CLKOUT_PCIE_P17
CLKOUT_PCIE_N17
CLKOUT_PCIE_P16
CLKOUT_PCIE_N16
CLKOUT_PCIE_P15
CLKOUT_PCIE_N15
CLKOUT_PCIE_P14
CLKOUT_PCIE_N14
CLKOUT_PCIE_P13
CLKOUT_PCIE_N13
CLKOUT_PCIE_P12
CLKOUT_PCIE_N12
CLKOUT_PCIE_P11
CLKOUT_PCIE_N11
CLKOUT_PCIE_P10
CLKOUT_PCIE_N10
CLKOUT_PCIE_P9
CLKOUT_PCIE_N9
CLKOUT_PCIE_P8
CLKOUT_PCIE_N8
CLKOUT_PCIE_P7
CLKOUT_PCIE_N7
CLKOUT_PCIE_P6
CLKOUT_PCIE_N6
CLKOUT_PCIE_P5
CLKOUT_PCIE_N5
CLKOUT_PCIE_P4
CLKOUT_PCIE_N4
CLKOUT_PCIE_P3
CLKOUT_PCIE_N3
CLKOUT_PCIE_P2
CLKOUT_PCIE_N2
CLKOUT_PCIE_P1
CLKOUT_PCIE_N1
CLKOUT_PCIE_P0
CLKOUT_PCIE_N0
CLKOUT_CPUPCIBCLK_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUBCLK2_P
CLKOUT_CPUBCLK2_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
CLKOUT_CPURTC
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PCH_ADL_S_1045P
XTAL_38P4M_IN
XTAL_38P4M_OUT
C761
C762
Y3
38.4MHZ/20ppm
R783
R782
R802
200K_1%_2
*Short_0201
CLK_PCIE_LANP
CLK_PCIE_LANN
CLK_PCIE_SDP
CLK_PCIE_SDN
CLK_PCIE_TBTP
CLK_PCIE_TBTN
CLK_PCIE_SSD-VGA_2P
CLK_PCIE_SSD-VGA_2N
CLK_VGA_P
CLK_VGA_N
CLK_PCIE_WLANP
CLK_PCIE_WLANN
CLK_PCIE_SSD1P
CLK_PCIE_SSD1N
CPU_PCI_BCLKP
CPU_PCI_BCLKN
CLKCUNSSC_DP
CLKCUNSSC_DN
TPS23
TPS24
CLK_CPU_BCLKP
CLK_CPU_BCLKN
PCH_RTC_CLK
RS87
*Short_0402
CPU_RTC_CLK
(6) LAN
(5) Card reader
(4) TBT
(3) SSD-Gen4#2
(2) dGPUx8
(1) WLAN
(0) SSD-Gen4#1
Quanta Computer Inc.
PROJECT : Helios(ZGRC)
Size
Document Number
PCH 1/7 (DMI/EDP/PEG)
Rev
1A
Date: Wednesday, February 15, 2023
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DP-TBT1

DP-TBT2

HDMI

HDA

DMIC

EDP & DDS Control

MsHybrid

CNVi-RF

CNVi-BT

EDP_CTRL

VGA_DDS

UH1M

PCH_ADL_S_1045P

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UH1N

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UH1L

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Quanta Computer Inc.

PROJECT : Helios(ZGRC)

Size	Document Number	Rev
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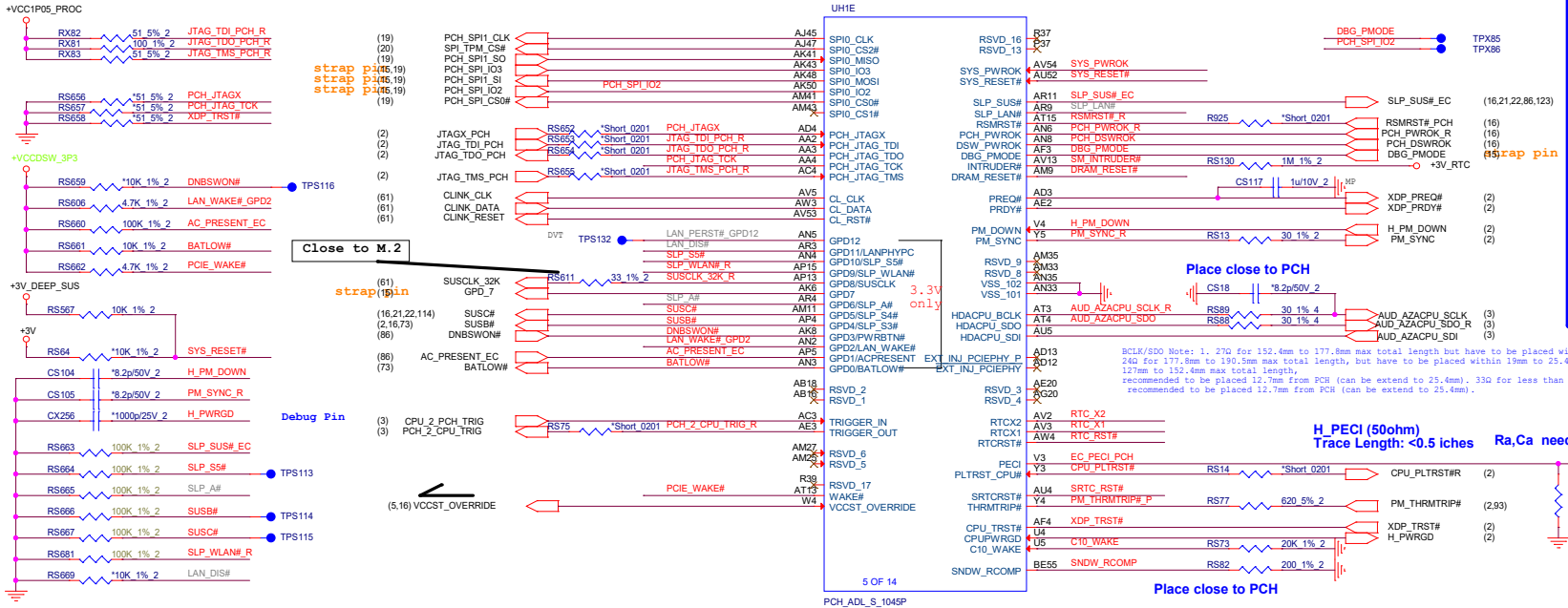
PCH_JTAGX

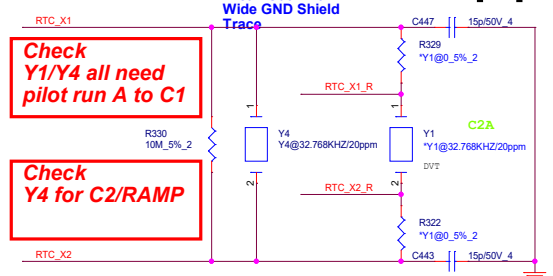


RTC Clock 32.768KHz

Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace

Check Y1/Y4 all need pilot run A to C1

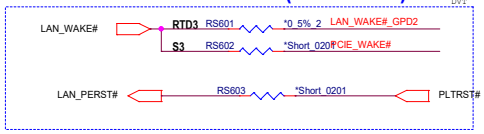
Check Y4 for C2/RAMP



11

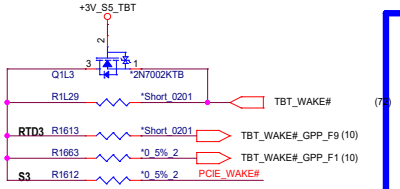
LAN WAKE

LAN WAKE (RTD3 cold)



WLAN WAKE

TBT M.R WAKE

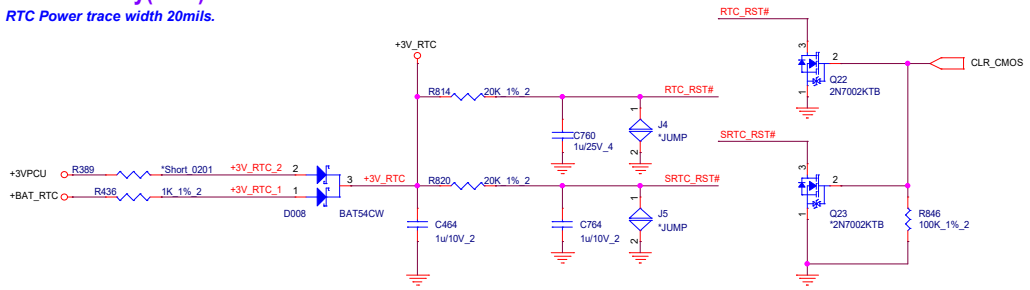


DSW_PWROK

DVT

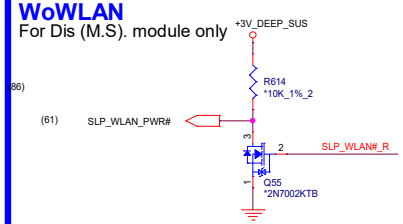
RTC Circuitry(RTC)

RTC Power trace width 20mils.

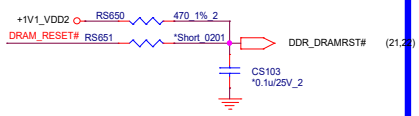


WoWLAN

For Dis (M.S). module only



DRAM reset



PCH_PWROK

PCH_PWROK_R R392 *0_5% 2 PCH_PWROK (16,86)

SYS_PWROK

SYS_PWROK R929 *Short_0201 EC_SYS_PWROK (86)

R927 *10K_1% 2

TPX94 SYS_PWROK
TPX95 PCH_PWROK_R
TPX96 PCH_DSWROK
TPX97 RSMRST#_R

Quanta Computer Inc.
PROJECT : Helios(ZGRC)

Size	Document Number	Rev
	PCH 3/7 (SATA/LPC/CLK)	1A
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+VCC1P05_PROC (2,5,11,141,145)

+1.8V_DEEP_SUS
RS141 *10K_1%_2 GPP_A11
RS142 *10K_1%_2 GPP_A10
RS143 *10K_1%_2 GPP_A7
ECS2 18p/25V_2 ESPI_CLK

ESPI_RESET#_R R27197 75K_1%_2
ESPI_CS#_R R67868 75K_1%_2

(86) ESPI_0 RS133 33_1%_2 ESPI_0_R
(86) ESPI_1 RS135 33_1%_2 ESPI_1_R
(86) ESPI_2 RS136 33_1%_2 ESPI_2_R
(86) ESPI_3 RS137 33_1%_2 ESPI_3_R
(86) ESPI_CS# RS138 0_5%_2 ESPI_CS#_R
(86) ESPI_CLK RS140 33_1%_2 ESPI_CLK_R
(86) ESPI_RESET# RS139 0_5%_2 ESPI_RESET#_R

GPP_A7
GPP_A10
GPP_A11

Panel_OD_PCH RS589 100K_1%_2
(45) Panel_OD_PCH

UH1J
GPP_A14 GPP_B23/SML1ALERT#/PCHHOT# AK52 AA54 SML1ALERT#_R → SML1ALERT#_R (15) strap pin
GPP_A0/ESPI_IO0 GPP_B22 AN54 T51 CCG6DF_OC_FAULT_SoC → CCG6DF_OC_FAULT_SoC (75)
GPP_A1/ESPI_IO1 GPP_B21 AM45 Y53 PD_MR_RST#_PCH → PD_MR_RST#_PCH (75)
GPP_A2/ESPI_IO2/SUSWARN#/SUSPWRDNACK GPP_B20 AN51 T52
GPP_A3/ESPI_IO3/SUSACK# GPP_B20/RSVD AM47 AA53 RF_EN_PCH → RF_EN_PCH (61)
GPP_A4/ESPI_CS0# GPP_B19/RSVD AN52
GPP_A5/ESPI_CLK AN50 V52 PMCALERT#
GPP_A6/ESPI_RESET# GPP_B18/PMCALERT# AK53
GPP_A7/ESPI_CS1# AL52 U52 SENSOR_MODE2_PCH → SENSOR_MODE2_PCH (91)
GPP_A8/ESPI_CS2# GPP_B17/ISH_GP5 AK51 AA45 SENSOR_MODE1_PCH → SENSOR_MODE1_PCH (91)
GPP_A9/ESPI_CS3# GPP_B16/ISH_GP4 AP45 AA52 TPD_INT#_PCH → TPD_INT#_PCH (88)
GPP_A10/ESPI_ALERT0# GPP_B15/ISH_GP3 AM52
GPP_A11/ESPI_ALERT1# AP43 W52
GPP_A12/ESPI_ALERT2# GPP_B14/SPKR AM53 ACZ_SPKR → ACZ_SPKR (15,64,86) strap pin
GPP_A13/ESPI_ALERT3# AN48
GPP_B13/PLTRST# Y52 PLTRST#_PCH
GPP_B12/SLP_S0# V53 AP_SLP_S0_L → AP_SLP_S0_L (20,61)
GPP_B11 AC53 ADDS_EN# → ADDS_EN# (45)
GPP_B10/ISH_GP2 Y50 RS697 *0_5%_2 → LID# (45,86)
GPP_B9/ISH_GP1 V40 G-sensor_INT#_DB → G-sensor_INT#_DB (91)
GPP_B8/ISH_GP0 V41 G-sensor_INT#_MB → G-sensor_INT#_MB (91)
GPP_B7/ISH_GP7 U54 AML_INT# → AML_INT# (91)
GPP_B6/CLKOUT_48 AB51 PTP_PWR_EN# → PTP_PWR_EN# (88)
GPP_B5/SX_EXIT_HOLDOFF#/ISH_GP6 Y51 → TPS130
Y48
GPP_B4/CPU_GP3 U51 BT_OFF_PCH# → TPS118
GPP_B3/CPU_GP2 → BT_OFF_PCH# (61)
GPP_B2/VRALERT# AA47 VRALERT#
GPP_B1/ISH_UART0_RTS#/GSPI2_CS1# U53
GPP_B0/PCIE_LNK_DOWN AC52
10 OF 14
PCH_ADL_S_1045P

+3V_DEEP_SUS
RS119 *49.9K_1%_2 UART2_TXD
RS120 *49.9K_1%_2 UART2_RXD
RS683 *2.2K_1%_2 TSN_I2C_SCL
RS684 *2.2K_1%_2 TSN_I2C_SDA
RS685 *10K_1%_2 TOUCH_INT#
RS131 2.2K_1%_2 TP_I2C_SCL
RS132 2.2K_1%_2 TP_I2C_SDA
RS124 10K_1%_2 TPD_INT#_PCH
RS94 2.2K_1%_2 PCH_SMB_CLK
RS96 2.2K_1%_2 PCH_SMB_DATA
RS692 *2.2K_1%_2 PEN_I2C_SCL
RS693 *2.2K_1%_2 PEN_I2C_SDA

BIOS Debug
TP285 UART2_TXD HX
TP286 UART2_RXD
TP282 UART0_TXD H
TP283 UART0_RXD
TP284
Placement together

UH1K
GPP_C23/UART2_CTS# GPP_D23/UART3_CTS# AJ11 TOUCH_INT# → TOUCH_INT# (45,97)
GPP_C22/UART2_RTS# GPP_D22/UART3_RTS# AM4 TOUCH_RST# → TOUCH_RST# (45,97)
GPP_C21/UART2_TXD GPP_D21/UART3_TXD AH5 PEN_RESET → PEN_RESET (97)
GPP_C20/UART2_RXD GPP_D20/UART3_RXD AM3 PEN_I2C_IRQ → PEN_I2C_IRQ (97)
GPP_C19/I2C1_SCL GPP_D16/GSPI3_CS0# AF11
GPP_C18/I2C1_SDA GPP_D19/GSPI3_MOSI AF9 → PEN_FWE_OUT (97)
GPP_D17/GSPI3_CLK AH13 → PEN_PDCT_IN (97)
GPP_C17/I2C0_SCL GPP_D18/GSPI3_MISO AK15 → PEN_GPIO0 (97)
GPP_C16/I2C0_SDA AK3 PD_I2C_SDA → PEN_GPIO1 (97)
GPP_D15/SML1DATA AL4 PD_I2C_SCL
GPP_C15/UART1_CTS#/ISH_UART1_CTS# GPP_D4/SML1CLK
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AM15 TBT_BB_SMDAT
GPP_C13/UART1_TXD/ISH_UART1_TXD GPP_D10/SML0DATA AM13 TBT_BB_SMCLK
GPP_C12/UART1_RXD/ISH_UART1_RXD GPP_D9/SML0CLK
GPP_C11/UART0_CTS# GPP_D6/MODEM_CLKREQ AJ2
GPP_C10/UART0_RTS# GPP_D7 AJ4 TOUCH_EN → MODEM_CLKREQ (61)
GPP_C9/UART0_TXD GPP_D8 AJ3 → TOUCH_EN (45,97) DVT
GPP_C8/UART0_RXD GPP_D5/CNV_RF_RESET# AK4 CNV_RF_RESET# → CNV_RF_RESET# (61)
GPP_C7/ISH_I2C2_SCL/I2C3_SCL GPP_E21/ISH_UART0_CTS# BC51 → BOARD_ID1 (17)
GPP_C6/ISH_I2C2_SDA/I2C3_SDA BE50 → BOARD_ID2 (17)
GPP_E20 BF52 → BOARD_ID3 (17)
GPP_C5/SML0ALERT# GPP_E19
GPP_C4/ISH_UART0_TXD/I2C2_SCL BE49 → BOARD_ID4 (17)
GPP_C3/ISH_UART0_RXD/I2C2_SDA GPP_E18 BG48 → BOARD_ID5 (17)
GPP_E17 BH49 → BOARD_ID6 (17)
GPP_C2/SMBALERT# GPP_E16/SBK3/BK3 BF49 → BOARD_ID7 (17)
GPP_C1/SMBDATA GPP_E15/SBK2/BK2 BH50 → BOARD_ID8 (17,45)
GPP_C0/SMBCLK GPP_E14/SBK1/BK1 BG49 → BOARD_ID9 (17)
GPP_E13/SBK0/BK0
GPP_E12/USB_OC3# BC47
GPP_E11/USB_OC2# BG51 → USB_OC3# (68)
GPP_E10/USB_OC1# BA43 → USB_OC2# (81)
GPP_E9/USB_OC0# BA40 → USB_OC1# (79)
BOARD_ID10 (17)
GPP_E8/SATALED#/SPI1_CS1# BJ51
GPP_E7/CPU_GP1 BD53 → BOARD_ID0 (17)
GPP_E6/SATA_DEVSLP2 BC52 GPU_WAKE# DVT
GPP_E5/SATA_DEVSLP1 BA47 USBKB_reset → TPS131 → USBKB_reset (87)
GPP_E4/SATA_DEVSLP0 BD52 → TPS26
GPP_E3/CPU_GP0 BB43 → KB_Light_effect# (87)
GPP_E2/SATAXPCIE2/SATAGP2 AY40 → DGPU_HOLD_RST#_GPP_E2
GPP_E1/SATAXPCIE1/SATAGP1 BD44 → TPS133 DVT
GPP_E0/SATAXPCIE0/SATAGP0 BB53
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PCH_ADL_S_1045P

UART2_TXD
UART2_RXD
TSN_I2C_SCL (45,97) TSN_I2C_SCL AD50
TSN_I2C_SDA (45,97) TSN_I2C_SDA AD48
TP_I2C_SCL (88) TP_I2C_SCL AJ53
TP_I2C_SDA (88) TP_I2C_SDA AJ54
(55) Reset_M.2SSD2# → UART0_TXD AF52
UART0_RXD AF48
(97) PEN_I2C_SCL R27232 *0_5%_2 ISH_I2C2_SCL_C AD45
(97) PEN_I2C_SDA R27233 *0_5%_2 ISH_I2C2_SDA_C AD47
strap pin (15) SML0ALERT# SML0ALERT# AB41
AB43
Y43
strap pin (15) SMLALERT# SMLALERT# AD53
Memory SPD (21) PCH_SMB_DATA PCH_SMB_DATA AE54
(21) PCH_SMB_CLK PCH_SMB_CLK AE53

+3V
RS126 *10K_1%_2 GPP_B20
RS117 *100_1%_2
+3V_DEEP_SUS
RS222 100K_1%_2 AP_SLP_S0_L → TPS129
RS558 *100K_1%_2
RS6706 *10K_1%_2 CCG6DF_OC_FAULT_SoC
RS6700 *10K_1%_2 RF_EN_PCH
RS2 *10K_1%_2 BT_OFF_PCH#
RS92 *2.2K_1%_2 PD_I2C_SDA
RS93 *2.2K_1%_2 PD_I2C_SCL
RS291 10K_1%_2 USB_OC1#
RS278 10K_1%_2 USB_OC2#
R27196 10K_1%_2 USB_OC3#
R67867 *10K_1%_2 PTP_PWR_EN#
R67871 10K_1%_2 PMCALERT# DVT
R27247 *10K_1%_2 ADDS_EN#
RS694 *2.2K_1%_2 G-sensor_INT#_DB
RS695 *2.2K_1%_2 G-sensor_INT#_MB
RS696 *2.2K_1%_2 AML_INT#
RS704 *2.2K_1%_2 SENSOR_MODE2_PCH
RS705 *2.2K_1%_2 SENSOR_MODE1_PCH
RS706 *10K_1%_2 PEN_I2C_IRQ

RS6707 100K_1%_2 TOUCH_EN DVT
RS595 *100K_1%_2 PTP_PWR_EN#
RS670 100K_1%_2 CNV_RF_RESET# DVT
RS689 *10K_1%_2 RF_EN_PCH DVT
RS703 *10K_1%_2 PEN_RESET
RS6701 *100K_1%_2 PD_MR_RST#_PCH DVT
RS6702 *100K_1%_2 TOUCH_RST#
RS6703 *100K_1%_2 USBKB_reset

(61) UART_WAKE_N R27181 *0_5%_2

PCH Throttling
+VCC1P05_PROC
(2,86,112,141) H_PROCHOT# Q56 *PJE8406
D76 *RB500V-40
TPS134 CCG6_PCH_PROCHOT# R967 *0_5%_2
+3VPCU
(112) BC_PCH_THROTTING# Q57 *PJE8406
D75 *RB500V-40
+3V_DEEP_SUS R748 10K_1%_2 VRALERT#

PLTRST# (Buffer)
+3V_DEEP_SUS
C1094 0.1u/50V_4
PLTRST#_PCH
R1504 100K_1%_2
U022 MC74VHC1G08DFT2G
R338 *0_5%_2
R1505 100K_1%_2
PLTRST# (11,20,25,53,55,61,72)
TPS109 PLTRST#_PCH
TPS110 PLTRST#

TBT M.R (vPro)
+3V_S5_TBT
+3V_DEEP_SUS RS621 *2.2K_1%_2
TBT_BB_SMDAT
QS13 *2N7002KTB
RS622 *0_5%_2
TBT_SMB_SDA (72)
SML0 FOR TBT Docking vPRO
TBT_BB_SMCLK
QS14 *2N7002KTB
RS624 *0_5%_2
RS623 *2.2K_1%_2
TBT_SMB_SCL (72)

Quanta Computer Inc.
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1. GPP_J and GPP_S groups support 1.8 V only.
2. GPD group supports 3.3 V only.
3. Others groups support per-group configurable voltage, which allows selection of 1.8 V or 3.3 V. The voltage of each GPIO group is selected by both connecting the corresponding GPIO power supply pin and setting the corresponding Group Master Voltage Select soft strap to the desired voltage (i.e 3.3 V or 1.8 V).

Name	Description	ZGP SET
VCCPGPPA	1.8 V or 3.3 V	1.8V
VCCPGPPEFK	1.8 V or 3.3 V	3.3V
VCCPGPPIR	1.8 V or 3.3 V	3.3V
VCCPGPPGH	1.8 V or 3.3 V	3.3V
VCCPGPPBC	1.8 V or 3.3 V	3.3V
VCCPGPPD	1.8 V or 3.3 V	3.3V

+0.82V (113,145)
+VCCPRIM_1P05 (113,145)

ESD Close to PCH Side

D20012 *MESD11LH5.0CT5G
D20013 *MESD11LH5.0CT5G
D20014 *MESD11LH5.0CT5G
D20015 *MESD11LH5.0CT5G

JS-ST-1202 change to MESD11LH5.0CT5G(BCD11LH5Z00)
JS-PV-0104 Change FP to esd-0_61x0_31-2p

caps placement close pin

+1.8V_DEEP_SUS RS671 *Short 0603 VCCPGPP_A CS106 1u/10V 2
+3V_DEEP_SUS RS598 *Short 0603 VCCPGPP_E_F_K CS107 1u/10V 2
+3V_DEEP_SUS RS599 *Short 0603 VCCPGPP_I_R CS108 1u/10V 2
+3V_DEEP_SUS RS672 *Short 0603 VCCPGPP_G_H CS109 1u/10V 2
+3V_DEEP_SUS RS673 *Short 0603 VCCPGPP_B_C CS110 1u/10V 2
+3V_DEEP_SUS RS674 *Short 0603 VCCPGPP_D CS111 1u/10V 2

+3V_S5 R825 *Short 0805 +3V_DEEP_SUS
+1.8V_S5 R850 0_5% 8 +1.8V_DEEP_SUS

+3V_DEEP_SUS RS147 *Short 0805 NON-DSx
+3VPCU RS675 *0_5% 8 DSx
+VCCDSW_3P3

UH1D

+3V_RTC 400uA CS23 1u/10V 2 CS22 0.1U/25V 2 BH51 BH52 BJ52 BJ53 BJ54 VCCRTC_1 VCCRTC_2 VCCRTC_3 VCCRTC_4 VCCRTC_5
400uA CS29 1u/10V 2 BE54 BF54 BF55 BG55 VCCDSW_3P3_1 VCCDSW_3P3_2 VCCDSW_3P3_3 VCCDSW_3P3_4
+0.82V 11.244A CS94 *47u/6.3V 6 AC25 AE25 AC26 AC28 AC30 AC31 AC33 AE26 AE28 AE30 AE31 AE33 VCCPRIM_CORE_0P82_1 VCCPRIM_CORE_0P82_7 VCCPRIM_CORE_0P82_2 VCCPRIM_CORE_0P82_3 VCCPRIM_CORE_0P82_4 VCCPRIM_CORE_0P82_5 VCCPRIM_CORE_0P82_6 VCCPRIM_CORE_0P82_8 VCCPRIM_CORE_0P82_9 VCCPRIM_CORE_0P82_10 VCCPRIM_CORE_0P82_11 VCCPRIM_CORE_0P82_12
+VCCPRIM_1P05 28mA CS24 1u/10V 2 AD15 VCCPRIM_1P05
+0.82V CS20 1u/10V 2 AH25 VCCPRIM_0P82_2
+1.8V_DEEP_SUS 14.44mA 10.2mA AM21 VCCPRIM_1P8_2
VCCPGPP_A VCCPGPP_E_F_K VCCPGPP_I_R VCCPGPP_G_H VCCPGPP_B_C VCCPGPP_D AM38 AR39 AV15 T43 Y41 AF18 VCCPGPPA VCCPGPPEFK VCCPGPPIR VCCPGPPGH VCCPGPPBC VCCPGPPD
RS574 *Short 0603 +VCCA_XTAL_PLL_0P82 300mA CS92 47u/6.3V 6 CS91 1u/10V 2 CS93 1u/10V 2 P13 P15 M15 R17 P17 AG25 U19 VCCA_XTAL_PLL_0P82_2 VCCA_XTAL_PLL_0P82_3 VCCA_XTAL_PLL_0P82_1 VCCA_XTAL_PLL_0P82_5 VCCA_XTAL_PLL_0P82_4 VCCPRIM_0P82_1 VCCA_XTAL_PLL_0P82_6
+0.82V 48.7mA
+VCC_MPHYPLL_LC_1P8 CS85 1u/10V 2 AK22 AK23 AK25 VCCAHSIOPLL_1P8_1 VCCAHSIOPLL_1P8_2 VCCAHSIOPLL_1P8_3
+VCCA_XTAL_PLL_1P8 AM16 AM18 AK16 AK18 VCCA_XTAL_PLL_1P8_3 VCCA_XTAL_PLL_1P8_4 VCCA_XTAL_PLL_1P8_1 VCCA_XTAL_PLL_1P8_2
4 OF 14
PCH_ADL_S_1045P

VCCHSIO_0P82_1 VCCHSIO_0P82_2 VCCHSIO_0P82_3 VCCHSIO_0P82_4 VCCHSIO_0P82_5 VCCHSIO_0P82_6 VCCHSIO_0P82_7 VCCHSIO_0P82_8 VCCHSIO_0P82_9 VCCHSIO_0P82_10 VCCHSIO_0P82_11 VCCHSIO_0P82_12 VCCHSIO_0P82_13 VCCHSIO_0P82_14 VCCHSIO_0P82_15 VCCHSIO_0P82_16 VCCHSIO_0P82_17 VCCHSIO_0P82_18 VCCHSIO_0P82_19 VCCHSIO_0P82_20 VCCHSIO_0P82_21 VCCHSIO_0P82_22 VCCHSIO_0P82_23 VCCHSIO_0P82_24 VCCHSIO_0P82_25 VCCHSIO_0P82_26 VCCHSIO_0P82_27 AB34 AB36 AC36 AE36 AC36 AH28 AH30 AH31 AH33 AH34 AH36 V23 V25 V27 V29 V31 V33 V35 Y23 Y25 Y26 Y28 Y30 Y31 Y33 Y34 Y36
+0.82V 4.39A
CS98 22u/6.3V 6 CS96 2.2U/10V 4 CS97 2.2U/10V 4
CS99 *10u/6.3V 4 CS100 *10u/6.3V 4 CS101 *10u/6.3V 4 CS102 *10u/6.3V 4

DCPCNVILDO2_1 DCPCNVILDO2_3 DCPCNVILDO2_5 DCPCNVILDO2_6 DCPCNVILDO2_7 DCPCNVILDO2_4 DCPCNVILDO2_2 BF1 BG1 BH1 BH2 BJ2 BG3 BF2
CS57 2200p/25V 2 +VCCCNVI_LDO_0P4

DCPRTC AV44 CS28 0.1U/25V 2 +VCCRTCEXT
DCPCNVILDO1 BF4 CS58 2.2U/10V 4 +VCCDPHY_1P24
VCCPRIM_3P3 AV41 +VCCPRIM_3P3 CS87 1u/10V 2 RS582 0_5% 4 +3V_DEEP_SUS 69.33mA
VCCSPI AH41 +VCCSPI CS88 1u/10V 2 RS583 0_5% 4 +3V_DEEP_SUS
VCCDUSB_0P82 AC23 +0.82V 94.8mA
VCCPRIM_0P82_3 AK36 +0.82V 212uA
VCCPRIM_1P8_1 AH20 +1.8V_DEEP_SUS 396mA
VCCPRIM_1P8_3 AM23 CS89 1u/10V 2 +1.8V_DEEP_SUS 78.7uA

+0.82V RS676 *Short 0603 LS2 1 2 *0.68uH 2520 3.3A
Inductor by default is a placeholder.
If stuffed, inductor must meet following requirements:
Rated at least 300mA
Minimum Inductance = 2.2uH

+1.8V_DEEP_SUS RS678 *Short 0805 LS4 1 2 *0.68uH 2520 3.3A
1)L : 0.68uH 3A
Inductor by default is a placeholder.
If stuffed, inductor must meet following requirements:
Rated at least 2000mA
Max DCR = 10mO
Minimum Inductance =250nH
2)CS+1002FB00
This resistor must be placed in Series with Capacitor_1
Default = 0 Ohm;
If Inductor is stuffed = 100 mOhm
RS679 0_5%_4
CS112 10u/6.3V_4

+1.8V_DEEP_SUS RS677 *Short 0603 150mA LS3 1 2 *0.68uH 2520 3.3A 150mA CS82 1u/10V 2 CS95 47u/6.3V 6
Inductor by default is a placeholder.
If stuffed, inductor must meet following requirements:
Rated at least 150mA
Minimum Inductance = 2.2uH

Quanta Computer Inc.
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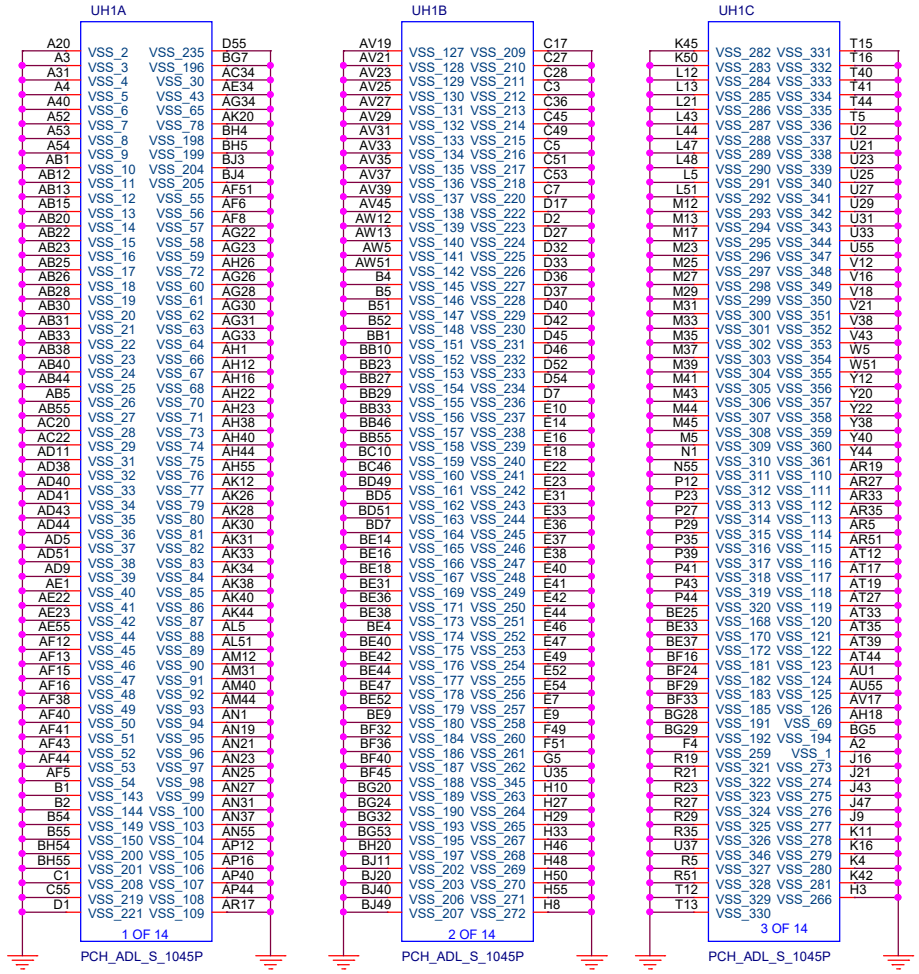

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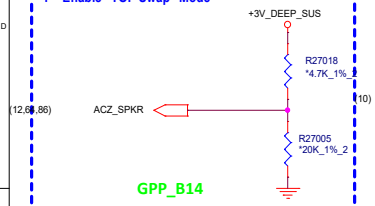
PCH Strap Pin

TOP SWAP OVERRIDE STRAP

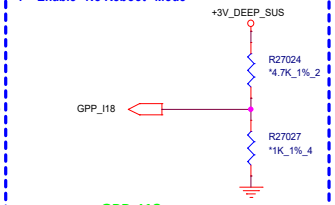
0 = Disable "TOP Swap" Mode (Default)
1 = Enable "TOP Swap" Mode



GPP_B14

NO REBOOT

0 = Disable "No Reboot" Mode (Default)
1 = Enable "No Reboot" Mode

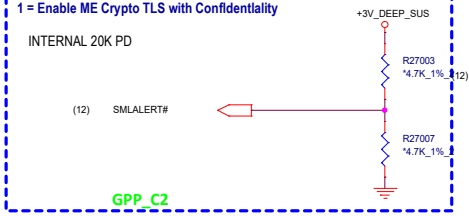


GPP_I18

TLS CONFIDENTIALITY ENABLED

0 = Disable ME Crypto TLS(Default)
1 = Enable ME Crypto TLS with Confidentiality

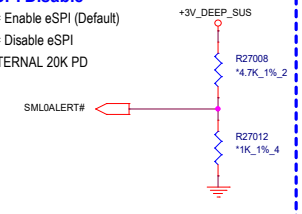
INTERNAL 20K PD



GPP_C2

eSPI Disable

0 = Enable eSPI (Default)
1 = Disable eSPI
INTERNAL 20K PD

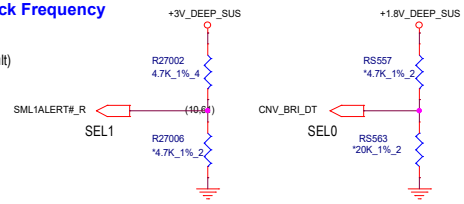


GPP_C5

CPUNSSC Clock Frequency

00 = 24MHz
01 = Reserved
10 = 38.4 MHz (Default)
11 = 25 MHz

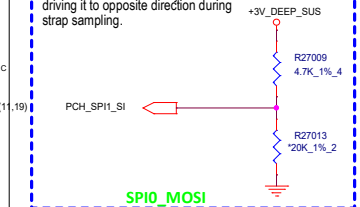
INTERNAL 20K PD



GPP_B23 GPP_J2

RESERVED

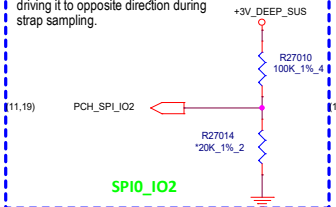
External pull-up is required. Recommend 4.7 kohm pull up
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



SPI0_MOSI

RESERVED

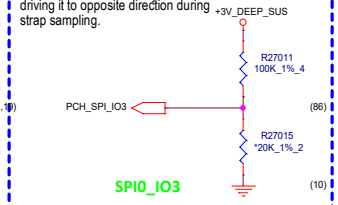
Recommend 20K if pulled up to 3.3V
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



SPI0_IO2

RESERVED

Recommend 100K if pulled up to 3.3V
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

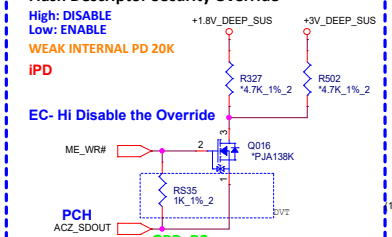


SPI0_IO3

Flash Descriptor Security Override

High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K
iPD

EC- Hi Disable the Override



GPP_R2

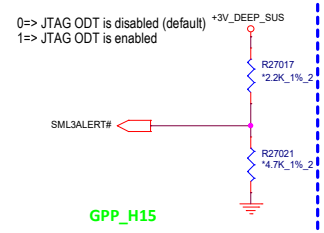
ESPI FLASH SHARING MODE

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
INTERNAL 20K PD

GPP_H12

JTAG ODT Disable

0=> JTAG ODT is disabled (default)
1=> JTAG ODT is enabled

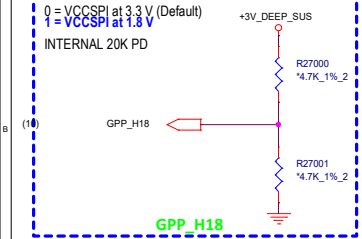


GPP_H15

VCCSPI Voltage Configuration

0 = VCCSPI at 3.3 V (Default)
1 = VCCSPI at 1.8 V

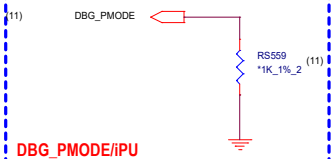
INTERNAL 20K PD



GPP_H18

Reserved

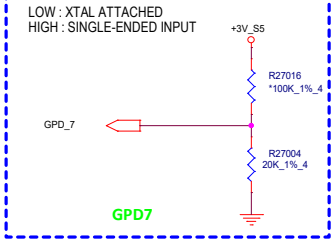
This strap should sample Hi.



DBG_PMODE/iPU

XTAL INPUT MODE

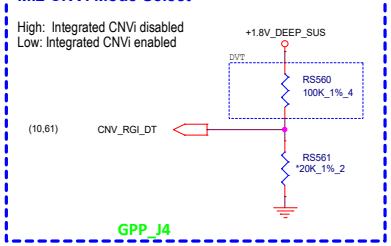
LOW : XTAL ATTACHED
HIGH : SINGLE-ENDED INPUT



GPD7

M.2 CNVi Mode Select

High: Integrated CNVi disabled
Low: Integrated CNVi enabled

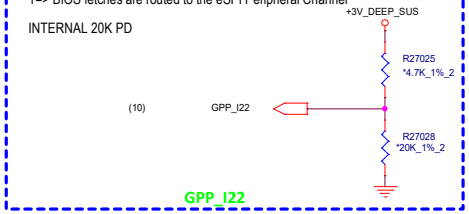


GPP_J4

Boot BIOS Strap (BBS)

0=> BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF)
1=> BIOS fetches are routed to the eSPI Peripheral Channel

INTERNAL 20K PD



GPP_I22

Quanta Computer Inc.
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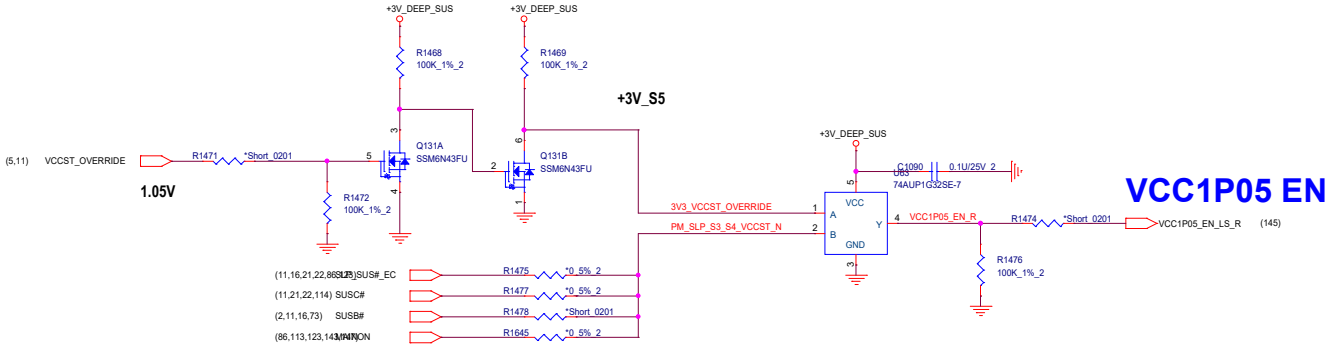
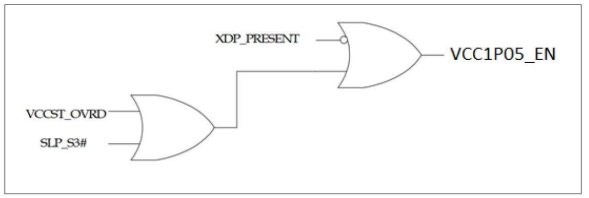
VCC1P05 EN

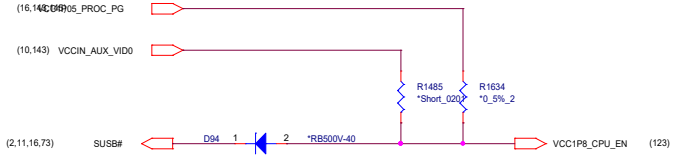


VCC1P05 EN

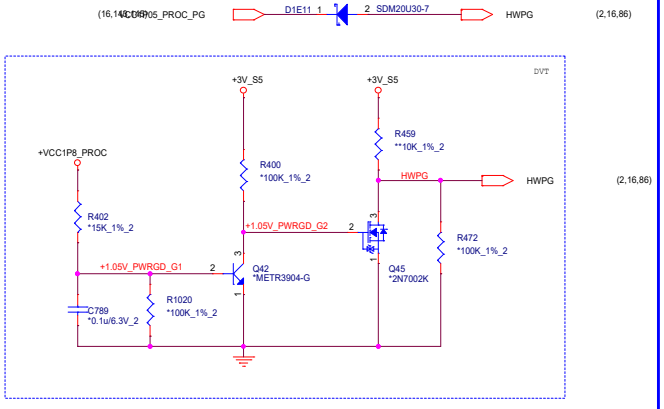
VCC1P05 Enable Logic



+VCC1P8_PROC EN

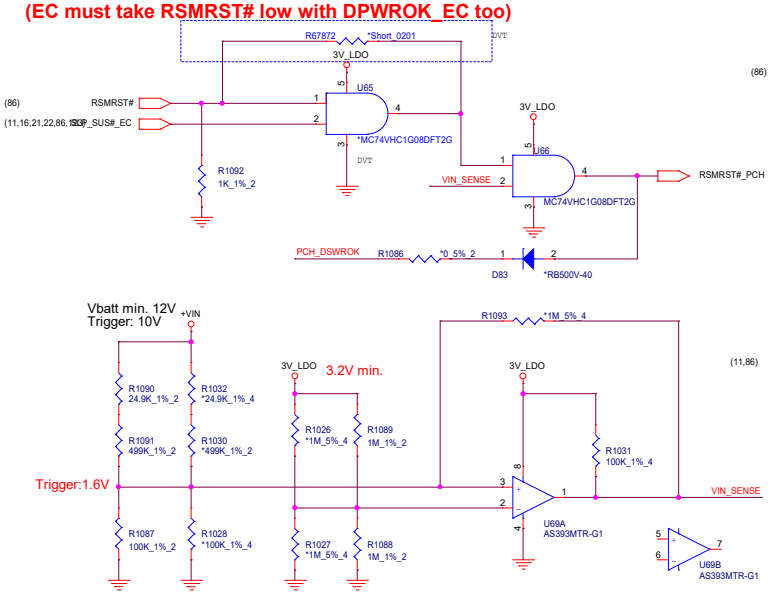


VCCST(+VCC1P05_PROC) - HWPG

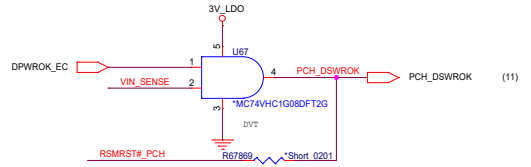


Surprise Power Down

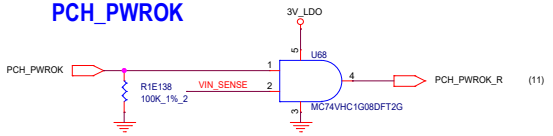
(EC must take RSMRST# low with DPWROK_EC too)



DSWOK



PCH_PWROK



Quanta Computer Inc.
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C	VCCST/VCCSTG POWER SWITHC	A1A
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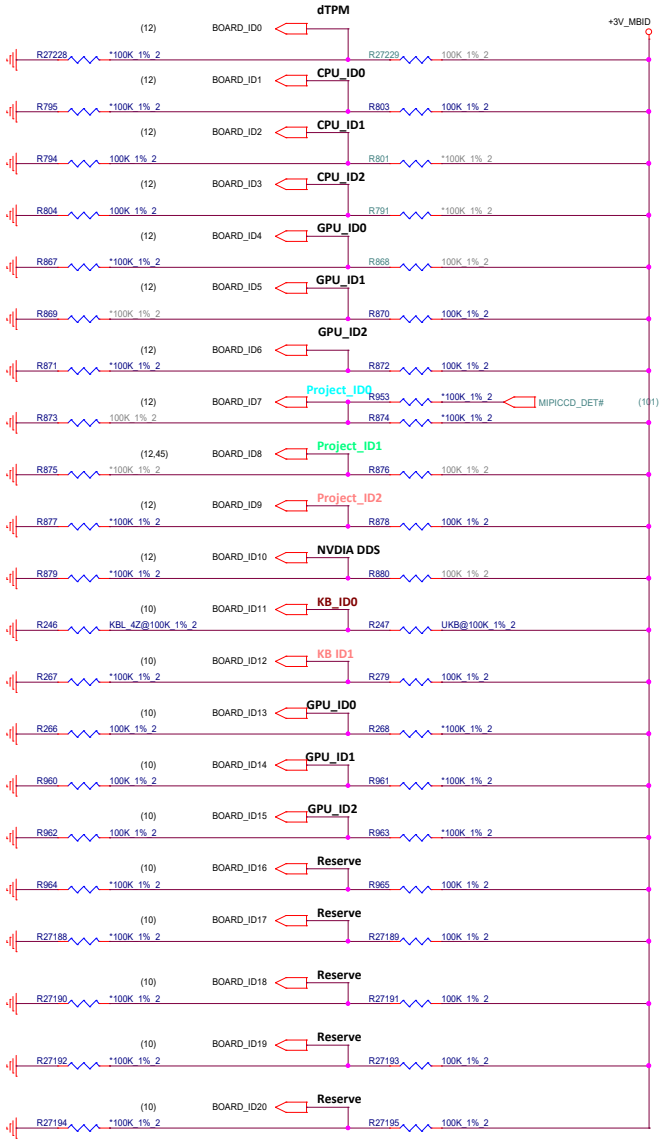
ID.NO	Function	Low	High
BOARD_ID0 GPP_E7	dTPM	0=No dTPM_N@	1=Yes dTPM@
BOARD_ID1 GPP_E21	CPU_ID0	CPU_ID2:CPU_ID1:CPU_ID0 000=I5, 001=I7, 010=I9, 011~111=N/A	
BOARD_ID2 GPP_E20	CPU_ID1		
BOARD_ID3 GPP_E19	CPU_ID2		
BOARD_ID4 GPP_E18	GPU_ID0	GPU_ID2:GPU_ID1:GPU_ID0 010=MB2 111=MB1	
BOARD_ID5 GPP_E17	GPU_ID1		
BOARD_ID6 GPP_E16	GPU_ID2		
BOARD_ID7 GPP_E15	Project ID0	ID0 [0=Helios, 1=Nitro] ID1 [0=16", 1=non 16"]	
BOARD_ID8 GPP_E14	Project ID1		
BOARD_ID9 GPP_E13	Project ID2		
BOARD_ID10 GPP_E9	NVIDIA DDS	0=No DDS_N@	1=Yes DDS@
BOARD_ID11 GPP_R21	KB_ID0	KB_ID1:KB_ID0 00=Single, 01=3zone 10=4zone, 11=PerKey	
BOARD_ID12 GPP_R20	KB_ID1		
BOARD_ID13 GPP_R19	GPU_ID0	GPU_ID2:GPU_ID1:GPU_ID0 000=GN21-X9 001=GN21-X11 111=GN20-E6	
BOARD_ID14 GPP_R18	GPU_ID1		
BOARD_ID15 GPP_R17	GPU_ID2		
BOARD_ID16 GPP_R16	Reserve		
BOARD_ID17 GPP_R15	Reserve		
BOARD_ID18 GPP_R14	Reserve		
BOARD_ID19 GPP_R13	Reserve		
BOARD_ID20 GPP_R12	Reserve		



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
C	ADL-P 14/14 (BLANK)	A1A

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Quanta Computer Inc.

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Size	Document Number	Rev
A	**LTE DB**	A1A

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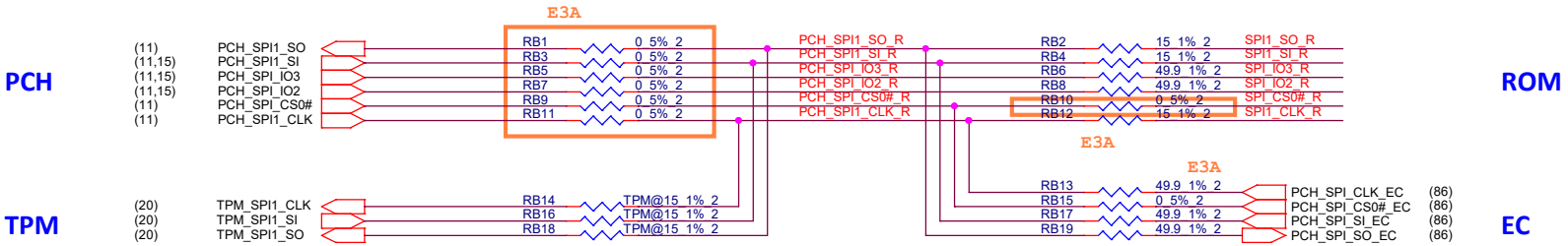
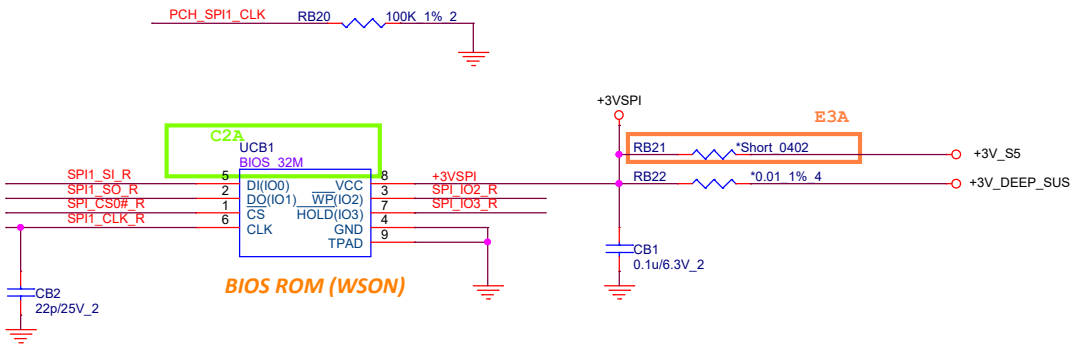


For Glitch Free



PVT

	Vender	Size	P/N	WSON8
	Winbond	32M	AKE3JF-KN01	W25Q256JVEIN
	MAX	32M	AKE3JZ-KZ01	MX25L25673GZ4I-08G
	Winbond	16M	AKE3DF-KN01	W25Q128JVSIQ(SOIC)

Quanta Computer Inc.
PROJECT : ZGN

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B	**BIOSROM**	A1A

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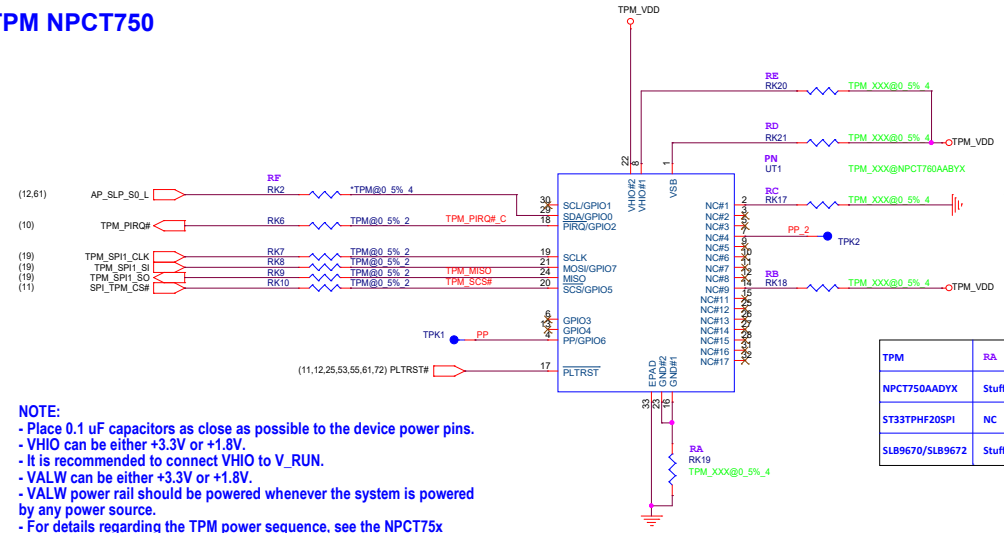
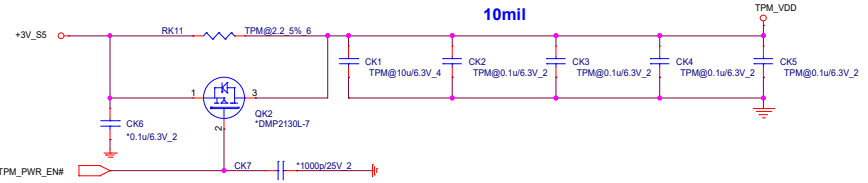
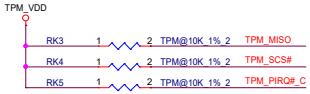
TPM NPCT750





TPM	RA	RB	RC	RD	RE	RF	PN
NPCT750AADYX	Stuff	NC	NC	Stuff	Stuff	Reserve	----------
ST33TPHF20SPI	NC	NC	Stuff	NC	NC	NC	----------
SLB9670/SLB9672	Stuff	Stuff	Stuff	Stuff	Stuff	NC	----------



NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- VHIO can be either +3.3V or +1.8V.
- It is recommended to connect VHIO to V_RUN.
- VALW can be either +3.3V or +1.8V.
- VALW power rail should be powered whenever the system is powered by any power source.
- For details regarding the TPM power sequence, see the NPCT75x Datasheet and Board Design Guidelines.

Quanta Computer Inc.
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Size	Document Number	Rev
C	TPM & HOLE	A1A
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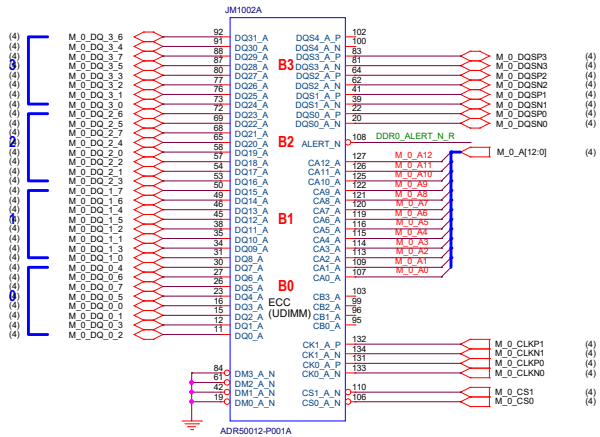
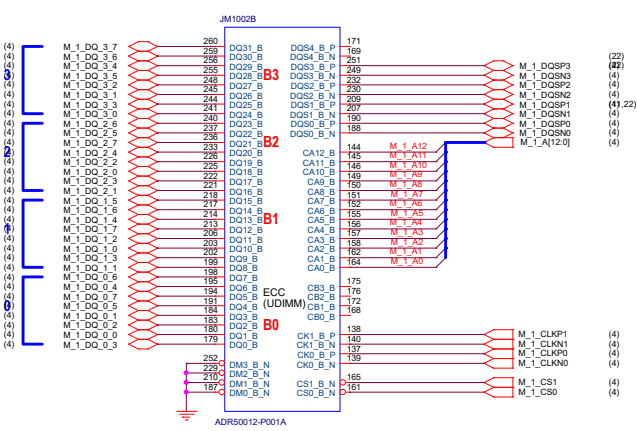
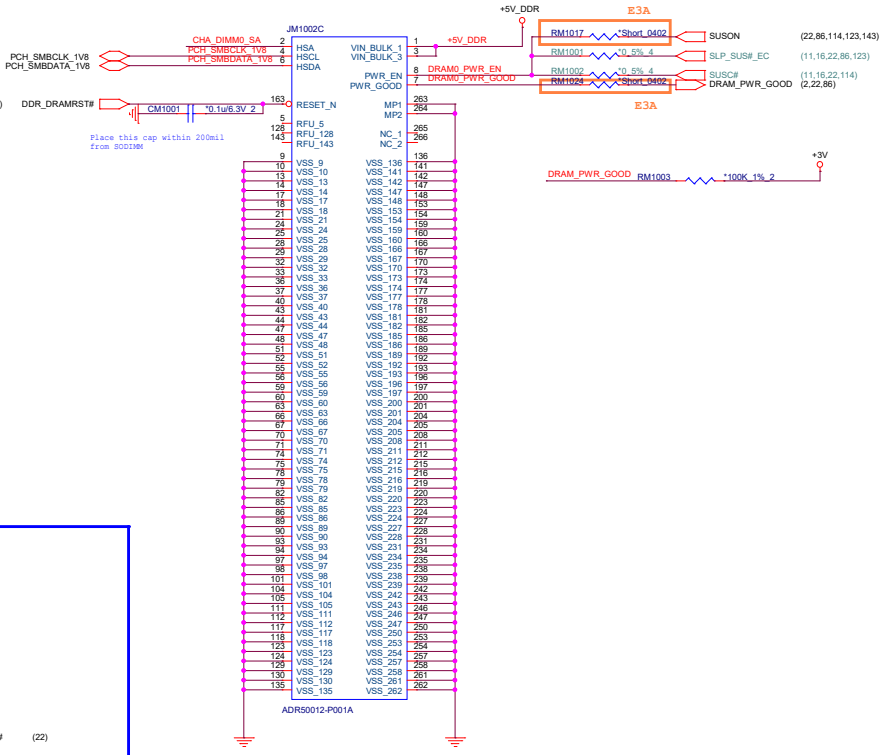
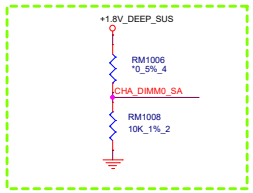
DDR5 SODIMM (Reverse)





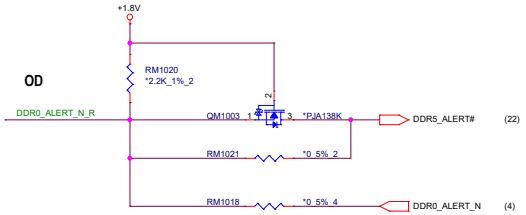




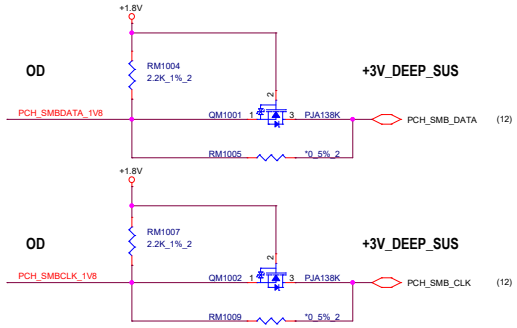
10K ,15.4K,23.2K,35.7K

CPU	CKE0/1 CH.A DIMM1 (JM1001)	CKE0/1 CH.B DIMM2 (JM1002)

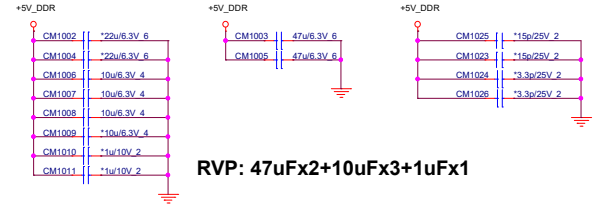
DDR5 CRC / Parity error indicator



Debug purposal



Place these Caps near So-Dimm



RVP: 47uFx2+10uFx3+1uFx1

Memeoy Size Note [619501 - P.112]
Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size should be greater or equal to channel B size.

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Size	Document Number	Rev
Custom	DDR5 CA DIMM0-RVS(4H)B	A1A
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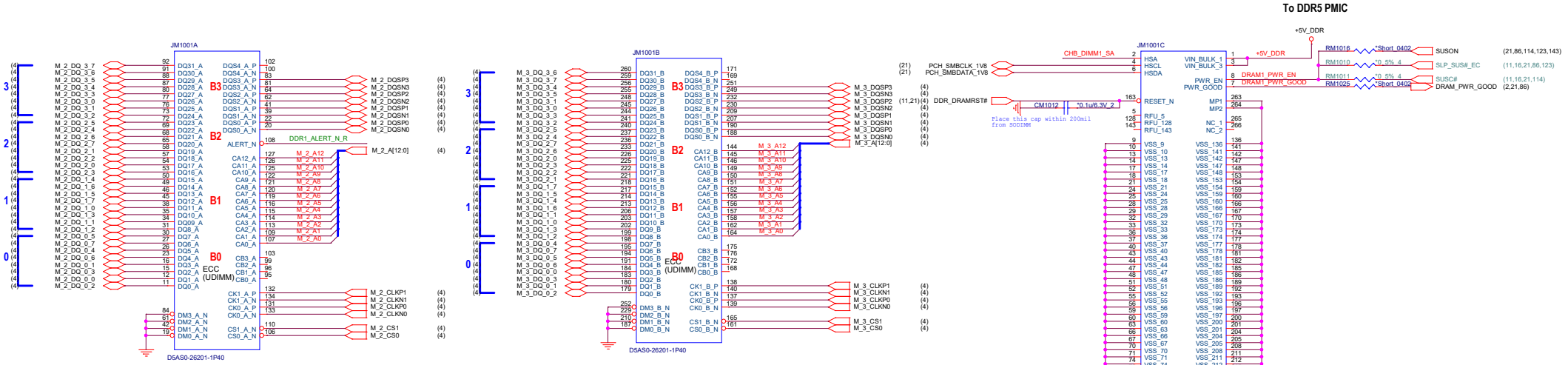
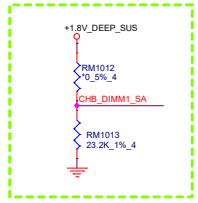
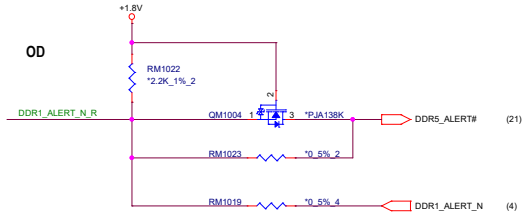
DDR5 SODIMM (Standard)



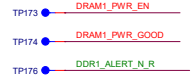


10K,15.4K 23.2K,35.7K

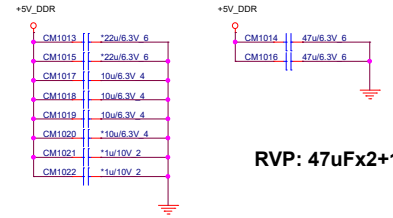
DDR5 CRC / Parity error indicator



Debug purposal



Place these Caps near So-Dimm



RVP: 47uFx2+10uFx3+1uFx1

CPU	CKE0/1 CH.A DIMM1 (JM1001)	CKE0/1 CH.B DIMM2 (JM1002)

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Size: Custom	Document Number: DDR5 CB DIMM0-STD(4H)B	Rev: A1A
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Quanta Computer Inc.

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Size	Document Number	Rev
A	**LTE DB**	A1A

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PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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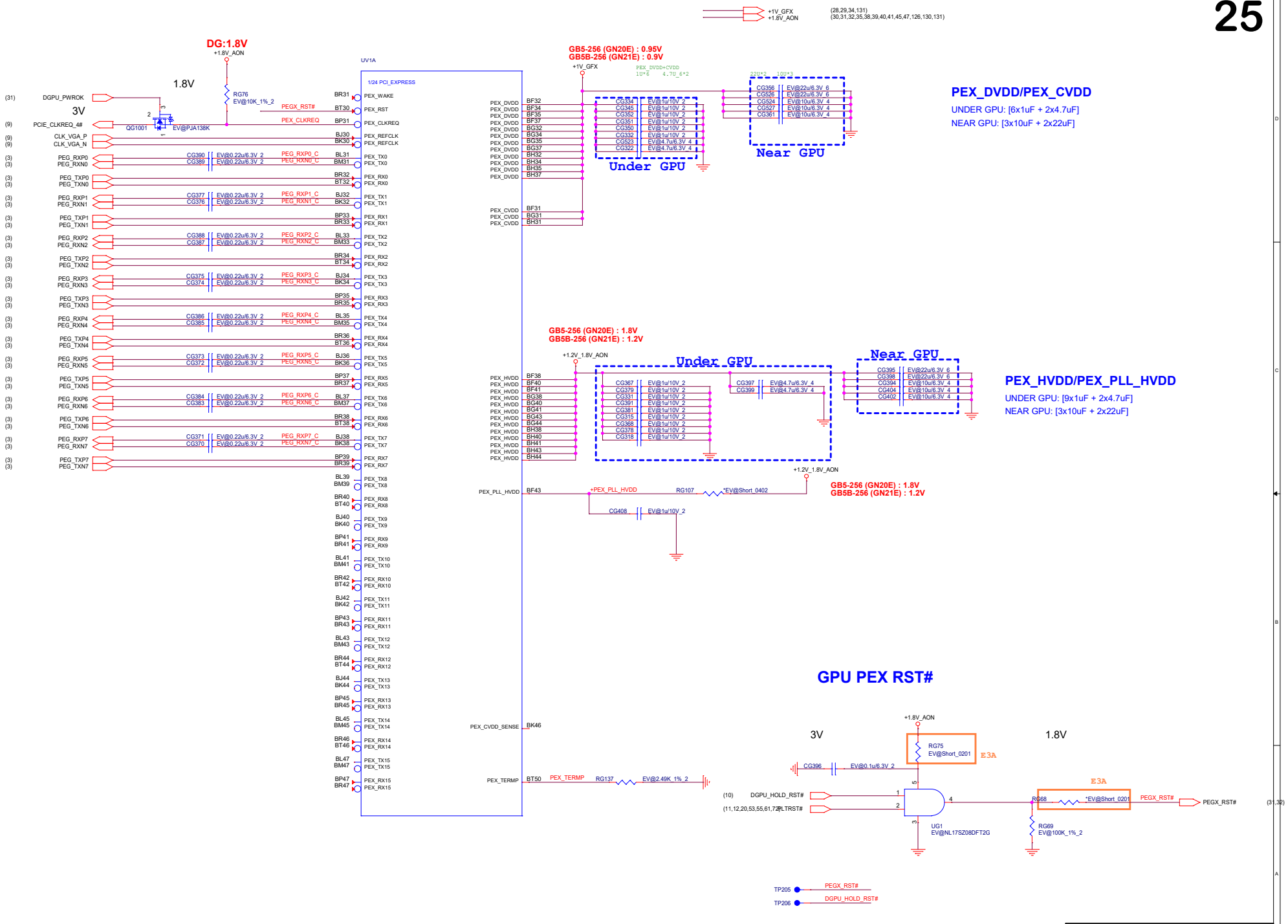

Quanta Computer Inc.
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Size	Document Number	Rev
C	GN20E-1/10 (PCIE)	A1A
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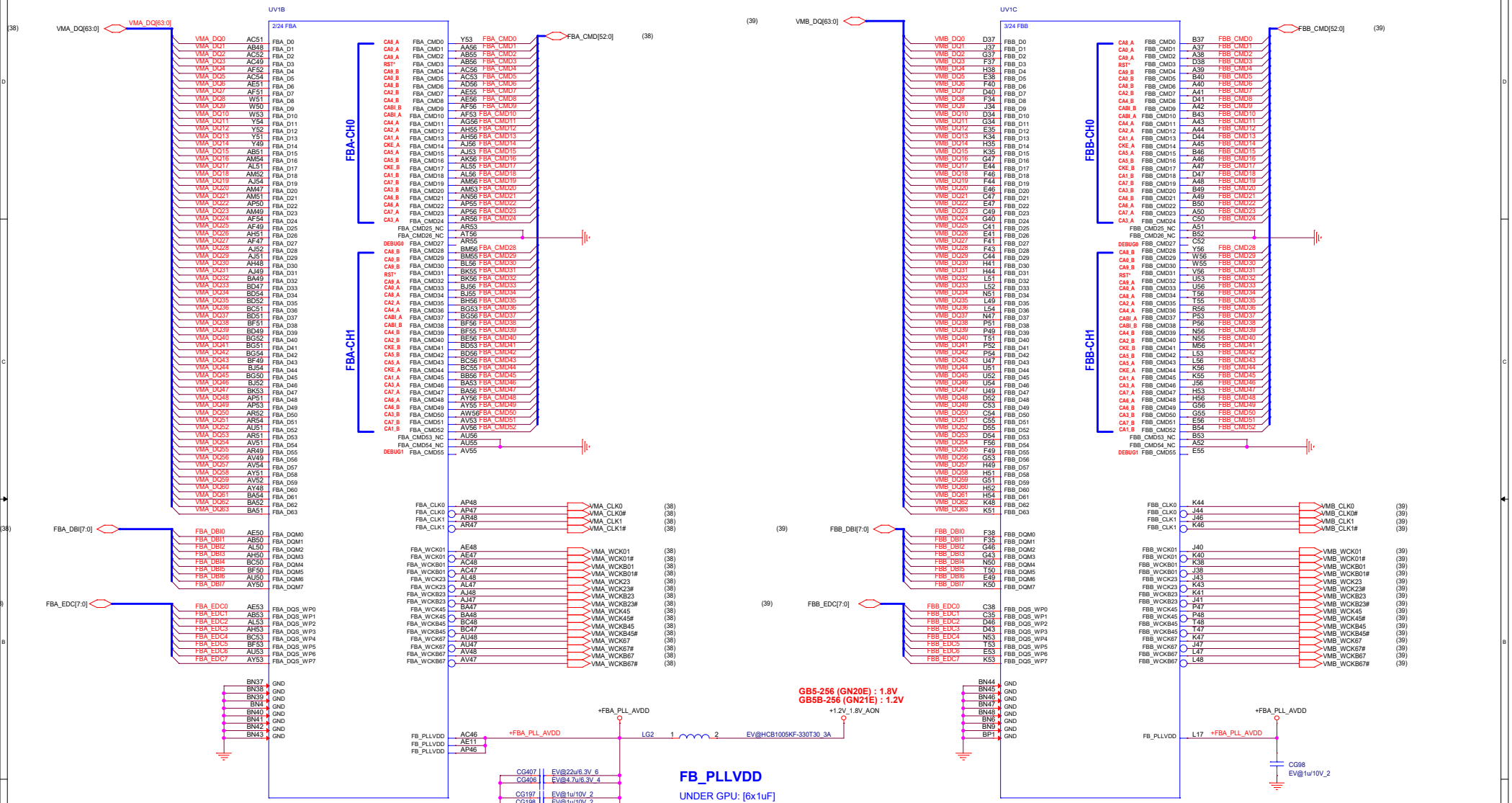
+FBVDDQ_MEM
+FBA_PLL_AVDD
+1.8V_AON
(27,35,38,39,40,41,130)
(27)
(25,30,31,32,35,38,39,40,41,45,47,126,130,131)

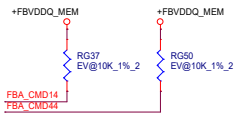


FB_PLLVDD

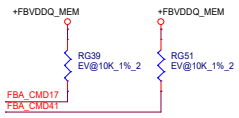
UNDER GPU: [6x1uF]

NEAR GPU: [1x22uF + 1x4.7uF]

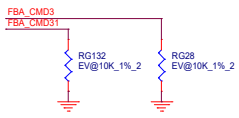
CKE_A



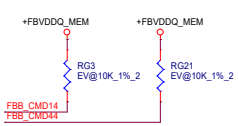
CKE_B



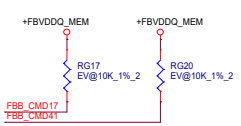
RESET



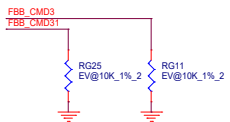
CKE_A



CKE_B



RESET



Quanta Computer Inc.
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Size	Document Number	Rev
C	Memory-FB/AB	A1A
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Channel D is not use for GN20-E3

+FBVDDQ_MEM (26,35,38,39,40,41,130)
+FBA_PLL_AVDD (26)

UV1D 4/24 FBC

(40) VMC_DQ[63:0]

VMC_DQ0	F7	FBC_D0
VMC_DQ1	H5	FBC_D1
VMC_DQ2	F8	FBC_D2
VMC_DQ3	G5	FBC_D3
VMC_DQ4	H8	FBC_D4
VMC_DQ5	E8	FBC_D5
VMC_DQ6	C8	FBC_D6
VMC_DQ7	D10	FBC_D7
VMC_DQ8	D2	FBC_D8
VMC_DQ9	E1	FBC_D9
VMC_DQ10	C2	FBC_D10
VMC_DQ11	D3	FBC_D11
VMC_DQ12	C3	FBC_D12
VMC_DQ13	B4	FBC_D13
VMC_DQ14	E4	FBC_D14
VMC_DQ15	D5	FBC_D15
VMC_DQ16	F17	FBC_D16
VMC_DQ17	E14	FBC_D17
VMC_DQ18	C14	FBC_D18
VMC_DQ19	H14	FBC_D19
VMC_DQ20	E17	FBC_D20
VMC_DQ21	F16	FBC_D21
VMC_DQ22	C17	FBC_D22
VMC_DQ23	H17	FBC_D23
VMC_DQ24	F10	FBC_D24
VMC_DQ25	G10	FBC_D25
VMC_DQ26	C11	FBC_D26
VMC_DQ27	E11	FBC_D27
VMC_DQ28	F11	FBC_D28
VMC_DQ29	F13	FBC_D29
VMC_DQ30	F14	FBC_D30
VMC_DQ31	H11	FBC_D31
VMC_DQ32	F26	FBC_D32
VMC_DQ33	E26	FBC_D33
VMC_DQ34	H26	FBC_D34
VMC_DQ35	D28	FBC_D35
VMC_DQ36	C26	FBC_D36
VMC_DQ37	E29	FBC_D37
VMC_DQ38	F28	FBC_D38
VMC_DQ39	G28	FBC_D39
VMC_DQ40	F31	FBC_D40
VMC_DQ41	K29	FBC_D41
VMC_DQ42	H29	FBC_D42
VMC_DQ43	J28	FBC_D43
VMC_DQ44	D31	FBC_D44
VMC_DQ45	G31	FBC_D45
VMC_DQ46	E32	FBC_D46
VMC_DQ47	H31	FBC_D47
VMC_DQ48	F19	FBC_D48
VMC_DQ49	K17	FBC_D49
VMC_DQ50	C20	FBC_D50
VMC_DQ51	J19	FBC_D51
VMC_DQ52	E20	FBC_D52
VMC_DQ53	F20	FBC_D53
VMC_DQ54	K20	FBC_D54
VMC_DQ55	H20	FBC_D55
VMC_DQ56	G22	FBC_D56
VMC_DQ57	F22	FBC_D57
VMC_DQ58	C23	FBC_D58
VMC_DQ59	D22	FBC_D59
VMC_DQ60	E23	FBC_D60
VMC_DQ61	F23	FBC_D61
VMC_DQ62	F25	FBC_D62
VMC_DQ63	H23	FBC_D63

FBC-CH0

CA8_A	FBC_CMD0	B5	FBC_CMD0
CA0_A	FBC_CMD1	A5	FBC_CMD1
CA9_A	FBC_CMD2	C5	FBC_CMD2
RST*	FBC_CMD3	A6	FBC_CMD3
CA9_B	FBC_CMD4	B7	FBC_CMD4
CA0_B	FBC_CMD5	A7	FBC_CMD5
CA8_B	FBC_CMD6	A8	FBC_CMD6
CA2_B	FBC_CMD7	D8	FBC_CMD7
CA4_B	FBC_CMD8	A9	FBC_CMD8
CABI_B	FBC_CMD9	B10	FBC_CMD9
CABI_A	FBC_CMD10	A10	FBC_CMD10
CA4_A	FBC_CMD11	A11	FBC_CMD11
CA2_A	FBC_CMD12	D11	FBC_CMD12
CA1_A	FBC_CMD13	A12	FBC_CMD13
CKE_A	FBC_CMD14	B13	FBC_CMD14
CA5_A	FBC_CMD15	A13	FBC_CMD15
CA5_B	FBC_CMD16	A14	FBC_CMD16
CKE_B	FBC_CMD17	D14	FBC_CMD17
CA1_B	FBC_CMD18	A15	FBC_CMD18
CA7_B	FBC_CMD19	B16	FBC_CMD19
CA3_B	FBC_CMD20	A16	FBC_CMD20
CA6_B	FBC_CMD21	A17	FBC_CMD21
CA6_A	FBC_CMD22	D17	FBC_CMD22
CA7_A	FBC_CMD23	A18	FBC_CMD23
CA3_A	FBC_CMD24	B19	FBC_CMD24
	FBC_CMD25_NC	A19	
	FBC_CMD26_NC	A20	
DEBUG0	FBC_CMD27	B20	
CA8_B	FBC_CMD28	A36	FBC_CMD28
CA0_B	FBC_CMD29	D35	FBC_CMD29
CA9_B	FBC_CMD30	A35	FBC_CMD30
RST*	FBC_CMD31	A34	FBC_CMD31
CA9_A	FBC_CMD32	B34	FBC_CMD32
CA0_A	FBC_CMD33	A33	FBC_CMD33
CA8_A	FBC_CMD34	D32	FBC_CMD34
CA2_A	FBC_CMD35	A32	FBC_CMD35
CA4_A	FBC_CMD36	A31	FBC_CMD36
CABI_A	FBC_CMD37	B31	FBC_CMD37
CABI_B	FBC_CMD38	A30	FBC_CMD38
CA4_B	FBC_CMD39	D29	FBC_CMD39
CA2_B	FBC_CMD40	A29	FBC_CMD40
CKE_B	FBC_CMD41	A28	FBC_CMD41
CA5_B	FBC_CMD42	B28	FBC_CMD42
CA5_A	FBC_CMD43	A27	FBC_CMD43
CKE_A	FBC_CMD44	D26	FBC_CMD44
CA1_A	FBC_CMD45	A26	FBC_CMD45
CA1_A	FBC_CMD46	A25	FBC_CMD46
CA7_A	FBC_CMD47	B25	FBC_CMD47
CA6_A	FBC_CMD48	A24	FBC_CMD48
CA6_B	FBC_CMD49	D23	FBC_CMD49
CA3_B	FBC_CMD50	A23	FBC_CMD50
CA7_B	FBC_CMD51	A22	FBC_CMD51
CA1_B	FBC_CMD52	B22	FBC_CMD52
	FBC_CMD53_NC	A21	
	FBC_CMD54_NC	D20	
DEBUG1	FBC_CMD55	B23	

FBC-CH1

FBC_CMD[52:0] (40)

(40) FBC_DBI[7:0]

FBC_DBI0	G7	FBC_DQM0
FBC_DBI1	E3	FBC_DQM1
FBC_DBI2	G16	FBC_DQM2
FBC_DBI3	G13	FBC_DQM3
FBC_DBI4	F29	FBC_DQM4
FBC_DBI5	F32	FBC_DQM5
FBC_DBI6	G19	FBC_DQM6
FBC_DBI7	G25	FBC_DQM7

(40) FBC_EDC[7:0]

FBC_EDC0	D7	FBC_DQS_WP0
FBC_EDC1	B3	FBC_DQS_WP1
FBC_EDC2	D16	FBC_DQS_WP2
FBC_EDC3	D13	FBC_DQS_WP3
FBC_EDC4	C29	FBC_DQS_WP4
FBC_EDC5	C32	FBC_DQS_WP5
FBC_EDC6	D19	FBC_DQS_WP6
FBC_EDC7	D25	FBC_DQS_WP7

BP32 BP34 BP36 BP38 BP40 BP42 BP44 BP46 — GND

FBC_CLK0	K22	VMC_CLK0	(40)
FBC_CLK0	J22	VMC_CLK0#	(40)
FBC_CLK1	K23	VMC_CLK1	(40)
FBC_CLK1	J23	VMC_CLK1#	(40)

FBC_WCK01	K13	VMC_WCK01	(40)
FBC_WCK01	J13	VMC_WCK01#	(40)
FBC_WCKB01	K11	VMC_WCKB01	(40)
FBC_WCKB01	J11	VMC_WCKB01#	(40)
FBC_WCK23	J16	VMC_WCK23	(40)
FBC_WCK23	K16	VMC_WCK23#	(40)
FBC_WCKB23	J14	VMC_WCKB23	(40)
FBC_WCKB23	K14	VMC_WCKB23#	(40)
FBC_WCK45	K31	VMC_WCK45	(40)
FBC_WCK45	J31	VMC_WCK45#	(40)
FBC_WCKB45	K32	VMC_WCKB45	(40)
FBC_WCKB45	J32	VMC_WCKB45#	(40)
FBC_WCK67	K25	VMC_WCK67	(40)
FBC_WCK67	J25	VMC_WCK67#	(40)
FBC_WCKB67	J26	VMC_WCKB67	(40)
FBC_WCKB67	K26	VMC_WCKB67#	(40)

+FBA_PLL_AVDD
FB_PLLVDD — L35 — +FBA_PLL_AVDD
CG106 EV@1u/10V_2

UV1E 5/24 FBD

AR4	FBD_D0	AU1
AP6	FBD_D1	AU4
AP6	FBD_D2	AT1
AR6	FBD_D3	AR2 FBD_CMD3
AM6	FBD_D4	AR1
AP3	FBD_D5	AP1
AP5	FBD_D6	AP4
AM9	FBD_D7	AN1
AU5	FBD_D8	AM2
AV6	FBD_D9	AM1
AV9	FBD_D10	AL1
AU3	FBD_D11	AL4
AU6	FBD_D12	AK1
AU8	FBD_D13	AJ2
AU10	FBD_D14	AJ1 FBD_CMD14
AR7	FBD_D15	AH1
AP6	FBD_D16	AH4
AH5	FBD_D17	AG1 FBD_CMD17
AH3	FBD_D18	AF2
AF9	FBD_D19	AF1
AE6	FBD_D20	AE1
AE8	FBD_D21	AE4
AE5	FBD_D22	AD1
AE10	FBD_D23	AC2
AL6	FBD_D24	AC1
AL3	FBD_D25	AB1
AL5	FBD_D26	AB4
AL8	FBD_D27	AB2
AJ6	FBD_D28	G2
AL10	FBD_D29	G1
AH6	FBD_D30	G3
AH8	FBD_D31	H1 FBD_CMD31
T5	FBD_D32	H2
T6	FBD_D33	J1
P6	FBD_D34	K4
T8	FBD_D35	K1
T3	FBD_D36	K2
N5	FBD_D37	L1
N3	FBD_D38	L2
N6	FBD_D39	M1
L6	FBD_D40	N4
N8	FBD_D41	N1 FBD_CMD41
K6	FBD_D42	P1
L9	FBD_D43	P2
K3	FBD_D44	R1 FBD_CMD44
K5	FBD_D45	T4
J2	FBD_D46	T1
K8	FBD_D47	U1
AC7	FBD_D48	U2
AE3	FBD_D49	V1
AC6	FBD_D50	W4
AC4	FBD_D51	W1
AB3	FBD_D52	Y1
AB5	FBD_D53	Y2
AB6	FBD_D54	AA1
AB8	FBD_D55	W2
W6	FBD_D56	
W8	FBD_D57	
W5	FBD_D58	
Y6	FBD_D59	
W3	FBD_D60	
U9	FBD_D61	
U6	FBD_D62	
T10	FBD_D63	

FBD-CH0

CA8_A	FBD_CMD0	AU1	
CA0_A	FBD_CMD1	AU4	
CA9_A	FBD_CMD2	AT1	
RST*	FBD_CMD3	AR2	FBD_CMD3
CA9_B	FBD_CMD4	AR1	
CA0_B	FBD_CMD5	AP1	
CA8_B	FBD_CMD6	AP4	
CA2_B	FBD_CMD7	AN1	
CA4_B	FBD_CMD8	AM2	
CABI_B	FBD_CMD9	AM1	
CABI_A	FBD_CMD10	AL1	
CA4_A	FBD_CMD11	AL4	
CA2_A	FBD_CMD12	AK1	
CA1_A	FBD_CMD13	AJ2	
CKE_A	FBD_CMD14	AJ1	FBD_CMD14
CA5_A	FBD_CMD15	AH1	
CA5_B	FBD_CMD16	AH4	
CKE_B	FBD_CMD17	AG1	FBD_CMD17
CA1_B	FBD_CMD18	AF2	
CA7_B	FBD_CMD19	AF1	
CA3_B	FBD_CMD20	AE1	
CA6_B	FBD_CMD21	AE4	
CA6_A	FBD_CMD22	AD1	
CA7_A	FBD_CMD23	AC2	
CA3_A	FBD_CMD24	AC1	
	FBD_CMD25_NC	AB1	
	FBD_CMD26_NC	AB4	
DEBUG0	FBD_CMD27	AB2	
CA8_B	FBD_CMD28	G2	
CA0_B	FBD_CMD29	G1	
CA9_B	FBD_CMD30	G3	
RST*	FBD_CMD31	H1	FBD_CMD31
CA9_A	FBD_CMD32	H2	
CA0_A	FBD_CMD33	J1	
CA8_A	FBD_CMD34	K4	
CA2_A	FBD_CMD35	K1	
CA4_A	FBD_CMD36	K2	
CABI_A	FBD_CMD37	L1	
CABI_B	FBD_CMD38	L2	
CA4_B	FBD_CMD39	M1	
CA2_B	FBD_CMD40	N4	
CKE_B	FBD_CMD41	N1	FBD_CMD41
CA5_B	FBD_CMD42	P1	
CA5_A	FBD_CMD43	P2	
CKE_A	FBD_CMD44	R1	FBD_CMD44
CA1_A	FBD_CMD45	T4	
CA3_A	FBD_CMD46	T1	
CA7_A	FBD_CMD47	U1	
CA6_A	FBD_CMD48	U2	
CA6_B	FBD_CMD49	V1	
CA3_B	FBD_CMD50	W4	
CA7_B	FBD_CMD51	W1	
CA1_B	FBD_CMD52	Y1	
	FBD_CMD53_NC	Y2	
	FBD_CMD54_NC	AA1	
DEBUG1	FBD_CMD55	W2	

FBD-CH1

FBD_CLK0	AC10	
FBD_CLK0	AC9	
FBD_CLK1	AB10	
FBD_CLK1	AB9	

FBD_WCK01	AP9	
FBD_WCK01	AP10	
FBD_WCKB01	AR9	
FBD_WCKB01	AR10	
FBD_WCK23	AH10	
FBD_WCK23	AH9	
FBD_WCKB23	AJ10	
FBD_WCKB23	AJ9	
FBD_WCK45	P10	
FBD_WCK45	P9	
FBD_WCKB45	N10	
FBD_WCKB45	N9	
FBD_WCK67	Y10	
FBD_WCK67	Y9	
FBD_WCKB67	W9	
FBD_WCKB67	W10	

BP48 BR1 BR12 BR15 BR18 BR2 BR21 BR24 — GND

+FBA_PLL_AVDD
FB_PLLVDD — T46 — +FBA_PLL_AVDD
CG152 EV@1u/10V_2

CKE_A

+FBVDDQ_MEM +FBVDDQ_MEM
RG4 EV@10K_1%_2 RG19 EV@10K_1%_2
FBC_CMD14 FBC_CMD44

CKE_B

+FBVDDQ_MEM +FBVDDQ_MEM
RG18 EV@10K_1%_2 RG5 EV@10K_1%_2
FBC_CMD17 FBC_CMD41

RESET

FBC_CMD3 FBC_CMD31
RG10 EV@10K_1%_2 RG108 EV@10K_1%_2

CKE_A

+FBVDDQ_MEM +FBVDDQ_MEM
RG36 EV@10K_1%_2 RG22 EV@10K_1%_2
FBD_CMD14 FBD_CMD44

CKE_B

+FBVDDQ_MEM +FBVDDQ_MEM
RG38 EV@10K_1%_2 RG23 EV@10K_1%_2
FBD_CMD17 FBD_CMD41

RESET

FBD_CMD3 FBD_CMD31
RG109 EV@10K_1%_2 RG115 EV@10K_1%_2

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GB5-256 (GN20E) : IFPA
GB5B-256 (GN21E) : IFPE

GB5-256 (GN20E) : IFPB
GB5B-256 (GN21E) : Reserve

UV1R

+1V_GFX (25,29,34,131)
+1.8V_AON (25,30,31,32,35,38,39,40,41,45,47,126,130,131)
+CORE_PLLVDD (29,30)

7/24 IFPAB

DL-DVI | DVI/HDMI | DP

RG58 EV@1K_1%_2 IFPAB_RSET BH23 IFPAB_RSET

+CORE_PLLVDD
+CORE_PLLVDD R1037 *EV@Short_0603 BH22 IFPAB_PLLVDD
CG353 EV@1u/10V_2
1.8V
0.4A
R1039 *EV@10K_1%_2

IFPA_AUX	BT10	GFX_TBT1_AUXN	(72)	TCP0/DP0
IFPA_AUX	BT11	GFX_TBT1_AUXP	(72)	
IFPA_L3	BR20	GFX_TBT1_TX3N	(72)	
IFPA_L3	BP20	GFX_TBT1_TX3P	(72)	
IFPA_L2	BP22	GFX_TBT1_TX2N	(72)	
IFPA_L2	BP22	GFX_TBT1_TX2P	(72)	
IFPA_L1	BT22	GFX_TBT1_TX1N	(72)	
IFPA_L1	BT23	GFX_TBT1_TX1P	(72)	
IFPA_L0	BR23	GFX_TBT1_TX0N	(72)	
IFPA_L0	BP23	GFX_TBT1_TX0P	(72)	

GFX_TBT1_AUXN
GFX_TBT1_AUXP
RG189 100K_1%_2
RG1157 100K_1%_2
DVT2

+1V_GFX
R1038 *EV@Short_0603 BF14 IFP_IOVDD
BF13 IFP_IOVDD
BF16 IFP_IOVDD
BF17 IFP_IOVDD
CG335 EV@4.7u/6.3V_4
CG319 EV@1u/10V_2
CG320 EV@1u/10V_2
CG325 EV@1u/10V_2
Near the GPU
Close the GPU

IFPB_AUX	BR11		
IFPB_AUX	BP11		
IFPB_L3	BL22		
IFPB_L3	BM22		
IFPB_L2	BK22		
IFPB_L2	BJ22		
IFPB_L1	BK23		
IFPB_L1	BL23		
IFPB_L0	BK25		
IFPB_L0	BJ25		

GB5B Reseve

IFPAB

[IFP_IOVDD_x]
1uF-0402/0201W-x5
4.7u-0603-x3
1u-0402/0201W-x5

UV1S

GB5-256 (GN20E) : IFPC
GB5B-256 (GN21E) : IFPA

8/24 IFPC

HDMI/Re-Driver

RG56 EV@1K_1%_2 IFPC_RSET BH20 IFPCD_RSET
+CORE_PLLVDD
GB5-256 (GN20E) : 1.8V
GB5B-256 (GN21E) : 1.2V
0.4A
+CORE_PLLVDD BH19 IFPCD_PLLVDD
CG354 EV@1u/10V_2

DVI/HDMI | DP

IFPC_AUX	BM10	GPU_DDCDATA	(47)	
IFPC_AUX	BL10	GPU_DDCCLK	(47)	
IFPC_L3	BK17	GPU_CLK#	(47)	
IFPC_L3	BL17	GPU_CLK	(47)	
IFPC_L2	BL19	GPU_D0#	(47)	
IFPC_L2	BM19	GPU_D0	(47)	
IFPC_L1	BK19	GPU_D1#	(47)	
IFPC_L1	BJ19	GPU_D1	(47)	
IFPC_L0	BK20	GPU_D2#	(47)	
IFPC_L0	BL20	GPU_D2	(47)	

IFPC

+1V_GFX
0.4A
BF19 IFP_IOVDD
BF20 IFP_IOVDD
CG343 EV@4.7u/6.3V_4
CG336 EV@1u/10V_2
CG326 EV@1u/10V_2
CG324 EV@1u/10V_2
Near the GPU
Under the GPU

GPU_DDCDATA
GPU_DDCCLK
RG154 *EV@100K_1%_2
RG155 *EV@100K_1%_2

UV1T

GB5-256 (GN20E) : IFPD
GB5B-256 (GN21E) : IFPB

9/24 IFPD

eDP

DVI/HDMI | DP

IFPD_AUX	BL11	GPU_eDP_AUXN	(44)	
IFPD_AUX	BM11	GPU_eDP_AUXP	(44)	
IFPD_L3	BT16	GPU_eDP_TXN3	(44)	
IFPD_L3	BT17	GPU_eDP_TXP3	(44)	
IFPD_L2	BR17	GPU_eDP_TXN2	(44)	
IFPD_L2	BP17	GPU_eDP_TXP2	(44)	
IFPD_L1	BP19	GPU_eDP_TXN1	(44)	
IFPD_L1	BR19	GPU_eDP_TXP1	(44)	
IFPD_L0	BT19	GPU_eDP_TXN0	(44)	
IFPD_L0	BT20	GPU_eDP_TXP0	(44)	

IFPD

+1V_GFX
BF22 IFP_IOVDD
BF23 IFP_IOVDD
Near the GPU
CG330 EV@1u/10V_2
CG317 EV@1u/10V_2
Under the GPU

GPU_eDP_AUXN
GPU_eDP_AUXP
RG156 EV@100K_1%_2
RG157 EV@100K_1%_2

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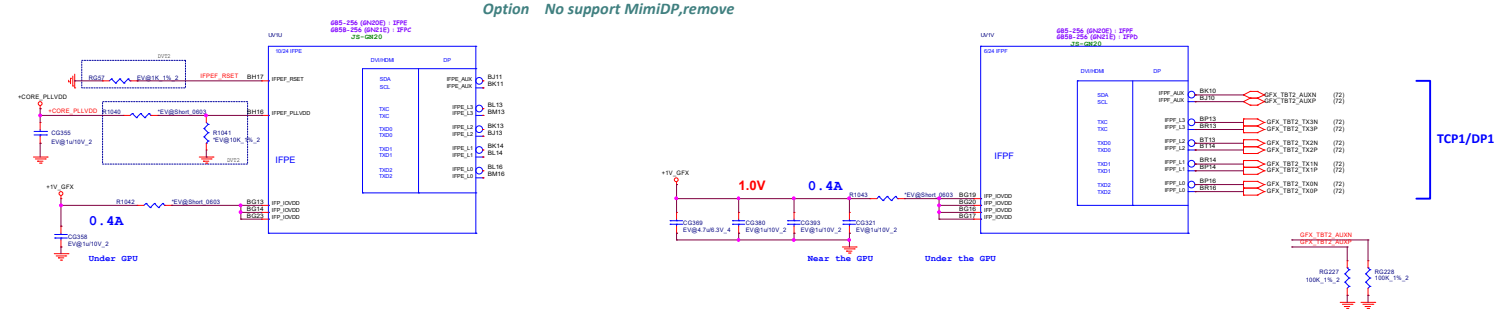
If IFPx are non-used
1. IFPx_PLLVDD should be 10K pull down only.
2. IFPx_RSET no stuff 1K by default

Option No support MimiDP,remove



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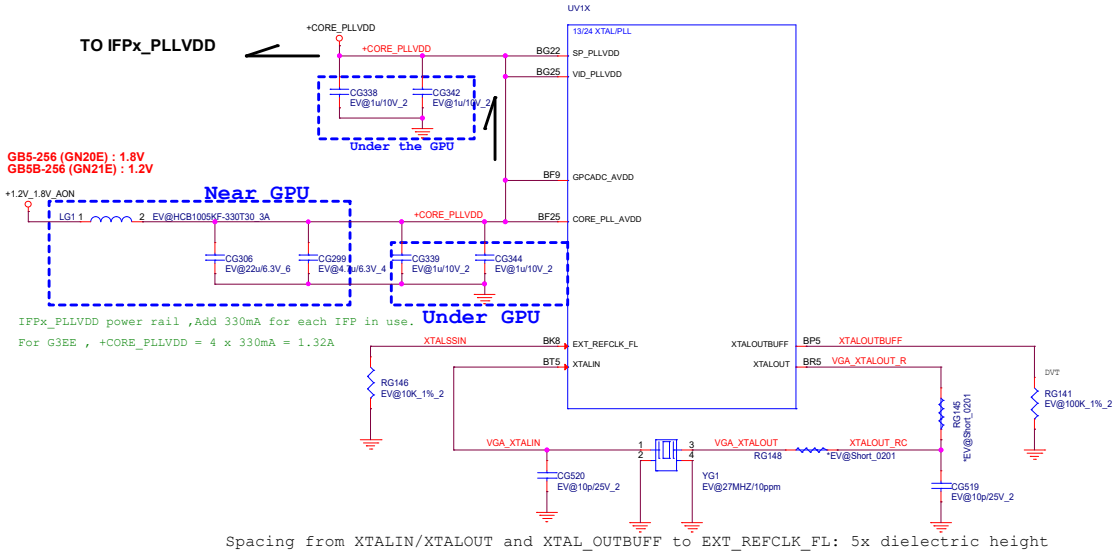
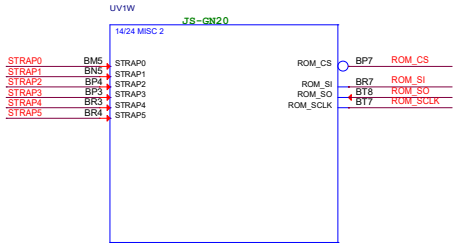
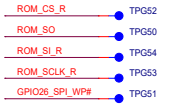


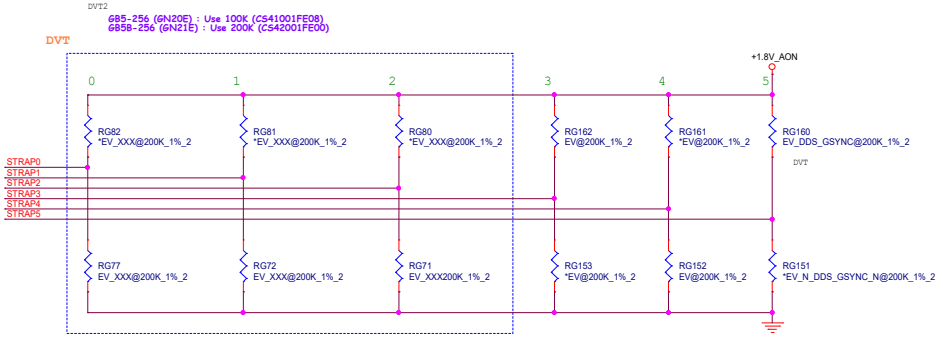
Spacing from XTALIN/XTALOUT and XTAL_OUTBUFF to EXT_REFCLK_FL: 5x dielectric height

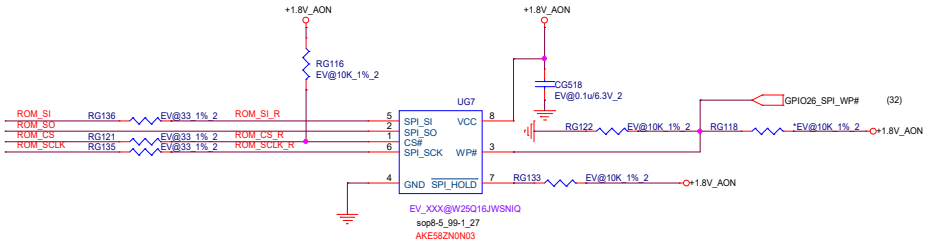
+1.8V_AON (25,31,32,35,38,39,40,41,45,47,126,130,131)



Vendor	Description	Size	P/N	GPU
WND	W25Q16JWSNIQ	16Mb	AKE58ZN0N03	
MAX	MX25U1633FM1I	16Mb	AKE58ZP0Z00	







STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
Non-GSYNC L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
GSYNC H	L	H	0	1	0	1

STRAP2	STRAP1	STRAP0	
L	H	M	ES
L	L	L	QS

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	see Memory RVL for memory configs corresponding to these numbers
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)

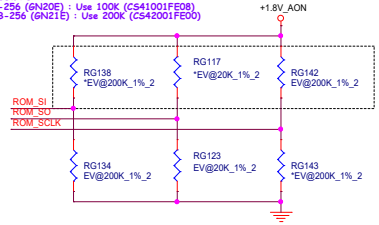
DVT

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT Strap
L	L	L	FS_OVERT# function DISABLED
L	L	H	FS_OVERT# function ENABLED(Default)

DVT2

RG117
GB5-256 (GN20E) : Use 10K (CS31001FE14)
GB5B-256 (GN21E) : Use 20K (CS32001FE00)

RG138& RG142
GB5-256 (GN20E) : Use 100K (CS41001FE08)
GB5B-256 (GN21E) : Use 200K (CS42001FE00)



VRAM Table for GN20-E GDDR6

	RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
QS	0 (0x0)	IC SGRAM(180P)K4ZAF325BC-SC20 STNBS	Samsung 16Gb x16 C-die	K4ZAF325BC-SC20	AKG5RGUT507	

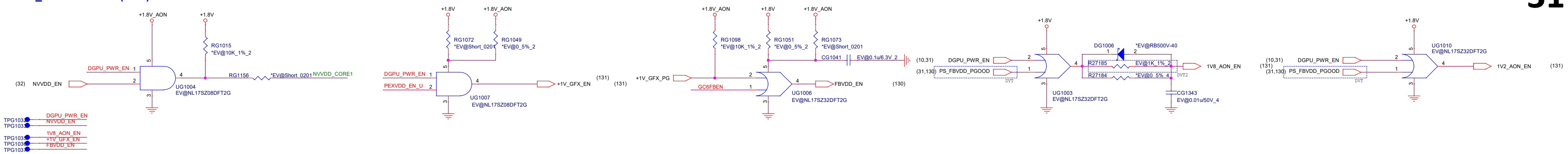
(3) NVVDD ENABLE (GB5B)
1V8_MAIN ENABLE(GB5)

(4) PEX_VDD_ENABLE

(5) FBVDDQ ENABLE for GC6

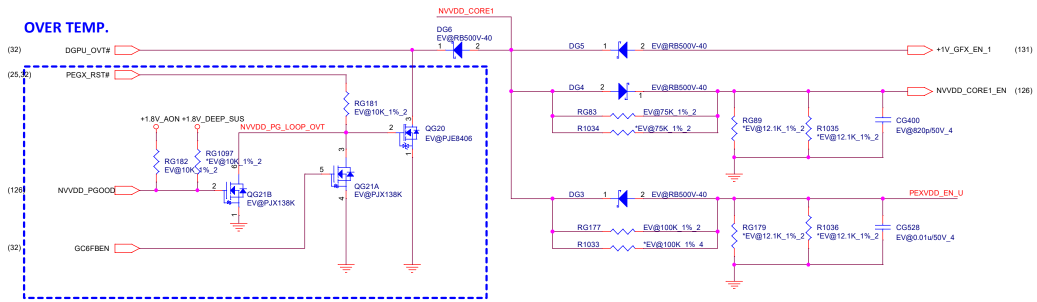
(2) 1V8_AON ENABLE

(1) 1V2_AON ENABLE



(DGPU_PWR_EN) --> 1V8_AON(VPP) -->(NVVDD_EN) --> NVVDD --> (NVVDD_PG) --> PEXVDD (1V_GFX) --> FBVDD --> (FBVDD_PG) --> (DGPU_PWROK_Q) --> (PEX_RST#)

OVER TEMP.



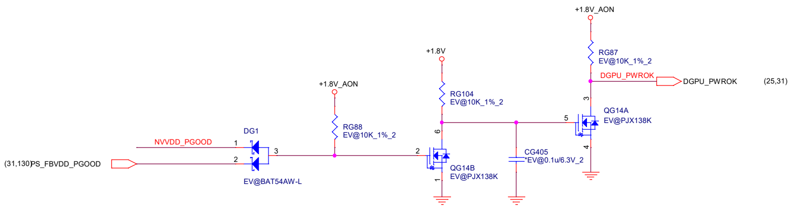
NVVDD POWER GOOD LOOPBACK
![!(NVVDD_PGOOD || GC6FBEN) && (PEGX_RST#)]

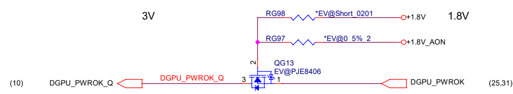
PEX_VDD_ENABLE

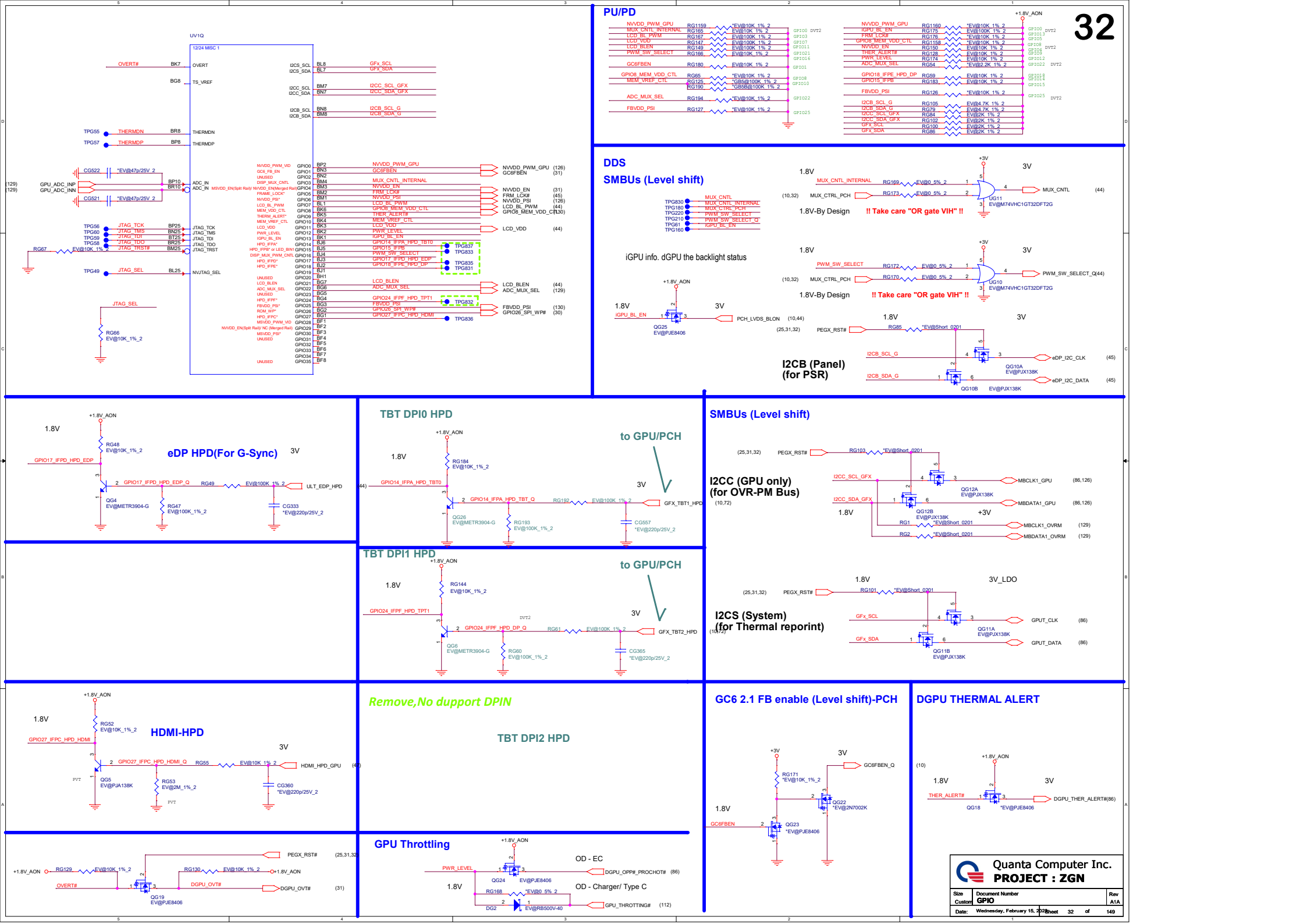
Table 4.6 Low Power State Summary

Low Power Features	1V8	NV3V3	MSVDD	NVVDD	PEXVDD	VPP	FBVDD	3V3	PWR_SRC
Normal Operation	ON	ON	ON	ON	ON	ON	ON	ON	ON
P-State 4.0 Rail Gating (NVVDD & MSVDD split)	ON	ON	ON	OFF	ON	ON	ON	ON	ON
P-State 4.0 Rail Gating (NVVDD & MSVDD merged)	ON	ON	ON	ON	ON	ON	ON	ON	ON
GC6 3.0	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON
GC-OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

POWER GOOD






PU/PD
DDS
SMBUs (Level shift)
1.8V-By Design
!! Take care "OR gate VIH" !!
iGPU info. dGPU the backlight status
I2CB (Panel)
(for PSR)
eDP HPD(For G-Sync)
TBT DPI0 HPD
TBT DPI1 HPD
to GPU/PCH
SMBUs (Level shift)
I2CC (GPU only)
(for OVR-PM Bus)
I2CS (System)
(for Thermal reporint)
HDMI-HPD
Remove,No dupport DPIN
TBT DPI2 HPD
GC6 2.1 FB enable (Level shift)-PCH
DGPU THERMAL ALERT
GPU Throttling
OD - EC
OD - Charger/ Type C
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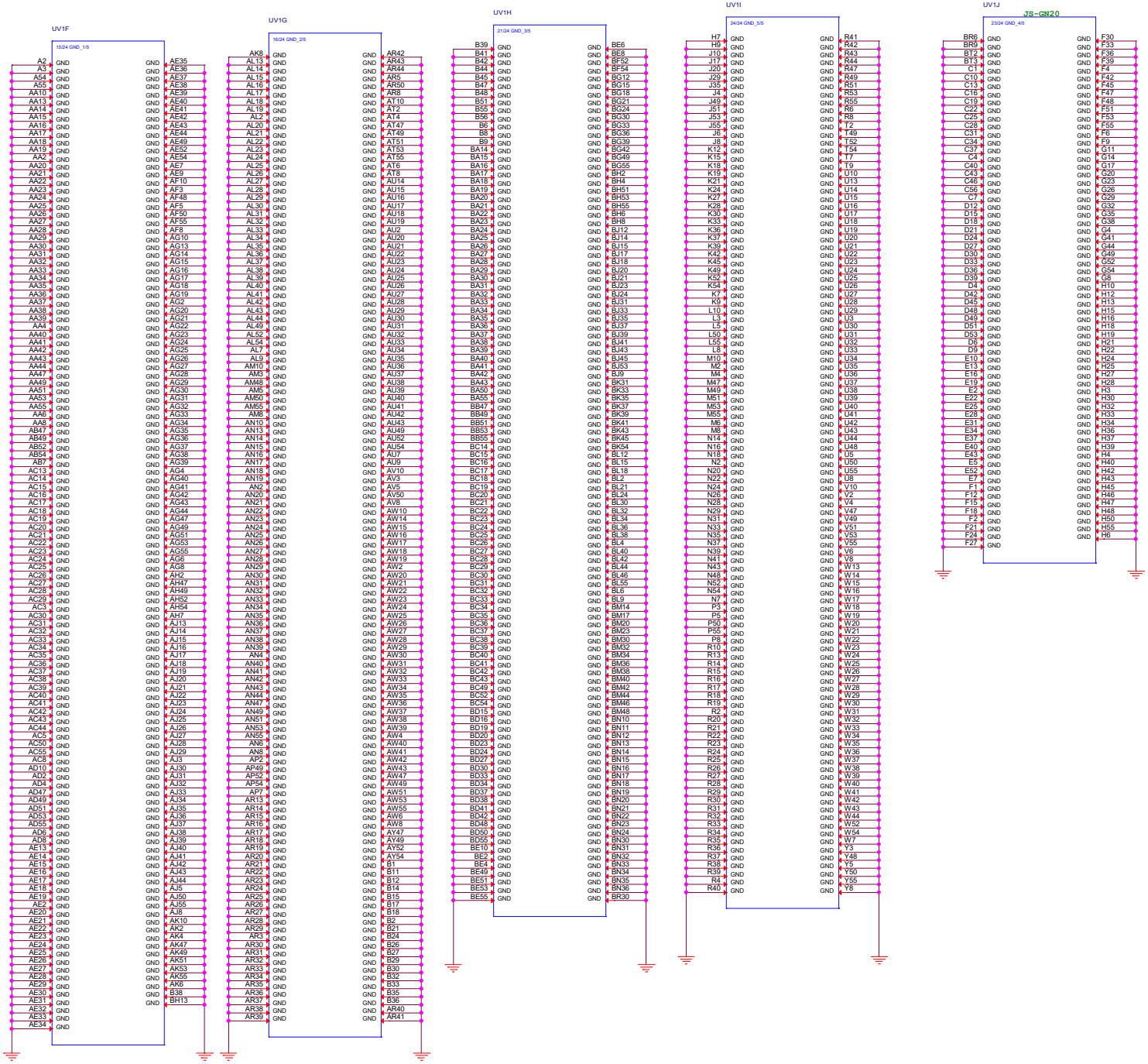

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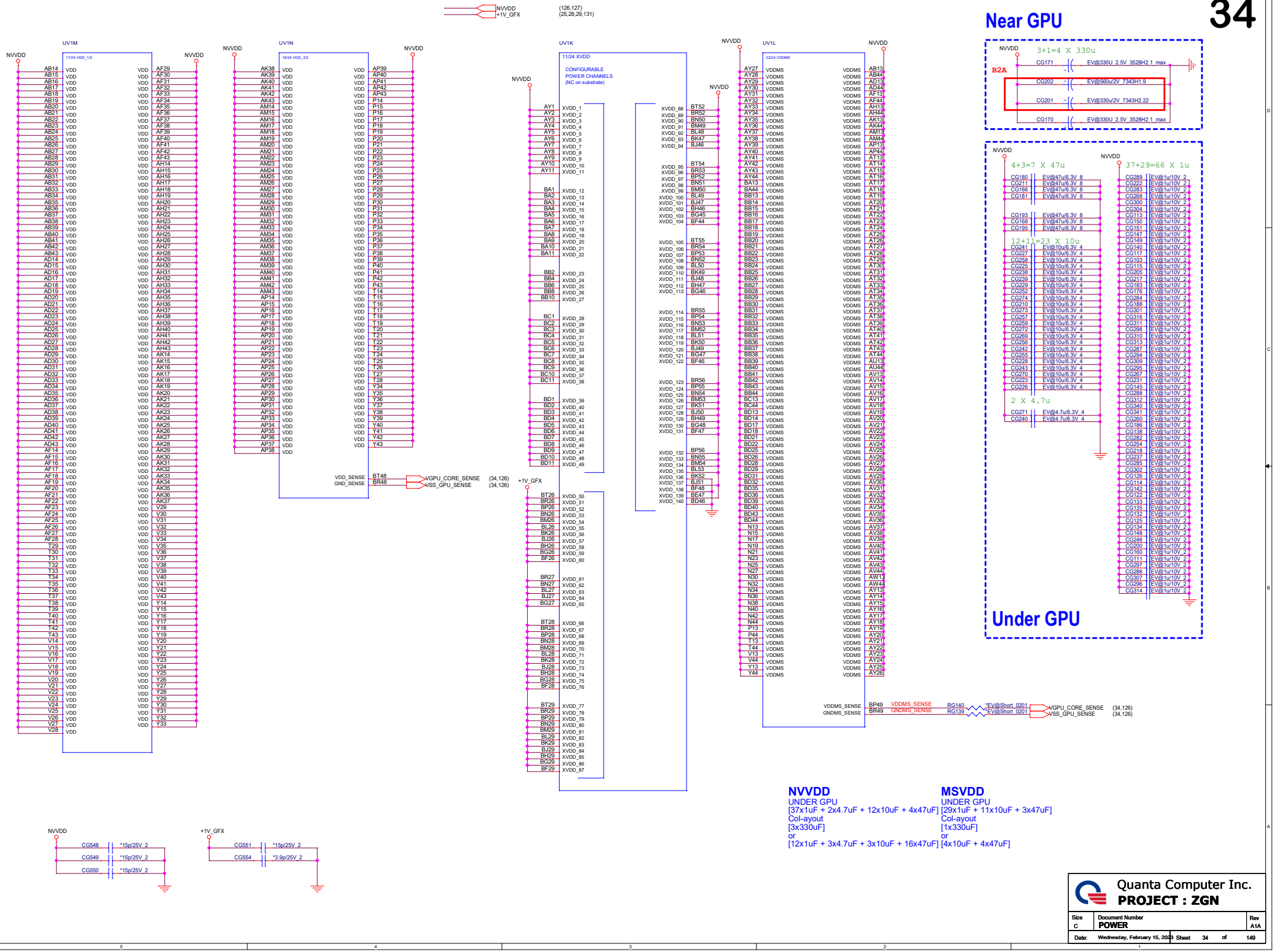

NVVDD

UNDER GPU
[37x1uF + 2x4.7uF + 12x10uF + 4x47uF]
Col-ayout
[3x330uF]
or
[12x1uF + 3x4.7uF + 3x10uF + 16x47uF]

MSVDD

UNDER GPU
[29x1uF + 11x10uF + 3x47uF]
Col-ayout
[1x330uF]
or
[4x10uF + 4x47uF]

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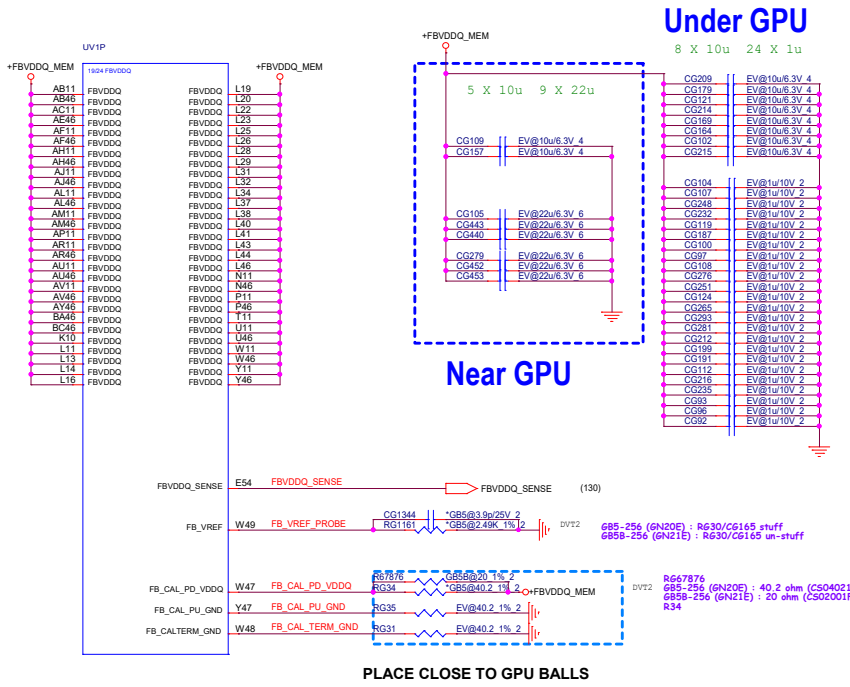
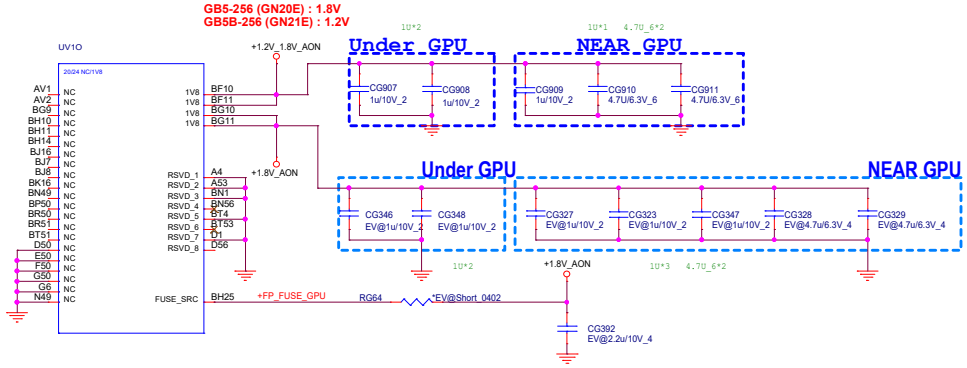
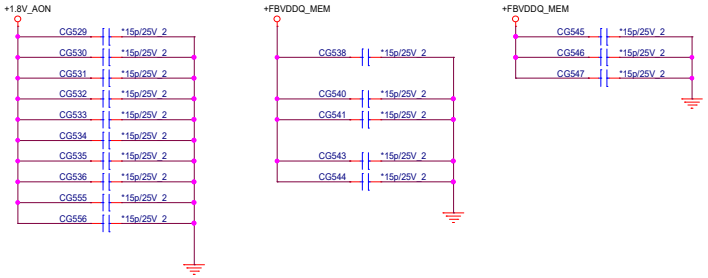
+1.8V_AON (25,30,31,32,38,39,40,41,45,47,126,130,131)
+FBVDDQ_MEM (26,27,38,39,40,41,130)





1V8

UNDER GPU
[2x1uF]
NEAR GPU
[3x1uF + 2x4.7uF]



FBVDDQ-GPU side

UNDER GPU
[24x1uF + 8x10uF]
NEAR GPU
[5x10uF + 9x22uF]

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A	**LTE DB**	A1A

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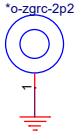
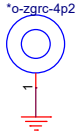
Hole

HOLE1
*o-zgrc-2p2

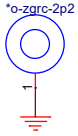


HOLE2
*H-O95X117D95X117N

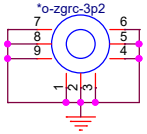
HOLE3
*o-zgrc-4p2



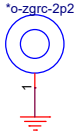
HOLE4
*o-zgrc-2p2



HOLE5
*o-zgrc-3p2



HOLE6
*o-zgrc-2p2

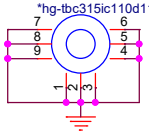


HOLE7
*H-O130X110D130X110N

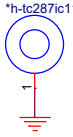
HOLE8
*2D-BARCODE-8X8-S

HOLE9
*2D-BARCODE-8X8-S

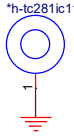
HOLE10
*hg-tbc315ic110d110p2



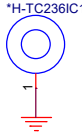
HOLE11
*h-tc287ic110bc315d110p2



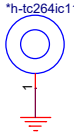
HOLE12
*h-tc281ic110bc315d110p2



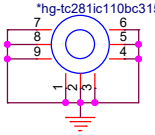
HOLE13
*H-TC236IC110BC197D110P2



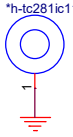
HOLE14
*h-tc264ic110bc236d110p2



HOLE15
*hg-tc281ic110bc315d110p2

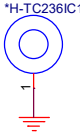


HOLE16
*h-tc281ic110bc276d110p2

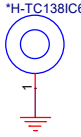


HOLE17
*H-C276D276N

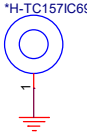
HOLE18
*H-TC236IC138BC148D138P2



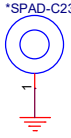
HOLE19
*H-TC138IC69BC79D69P2



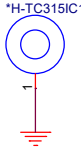
HOLE20
*H-TC157IC69BC79D69P2



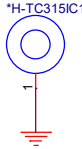
HOLE21
*SPAD-C236NP



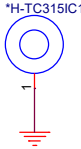
HOLE23
*H-TC315IC157BC177D157P2



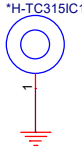
HOLE24
*H-TC315IC157BC177D157P2



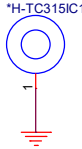
HOLE25
*H-TC315IC157BC177D157P2



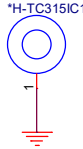
HOLE26
*H-TC315IC157BC177D157P2



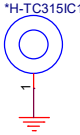
HOLE27
*H-TC315IC157BC177D157P2



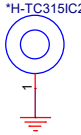
HOLE28
*H-TC315IC157BC177D157P2



HOLE29
*H-TC315IC157BC177D157P2

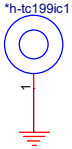


HOLE30
*H-TC315IC236BC236D236PT



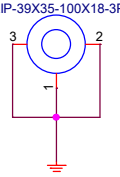
HOLE31
*H-C95D95N

HOLE32
*h-tc199ic110bc315d110p2

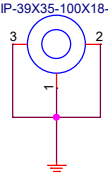


Clips

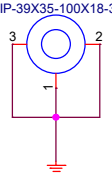
S1
CLIP-39X35-100X18-3P



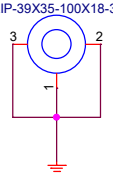
S4
CLIP-39X35-100X18-3P



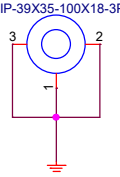
S5
CLIP-39X35-100X18-3P



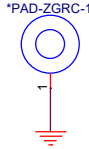
S7
CLIP-39X35-100X18-3P



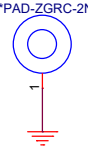
S11
CLIP-39X35-100X18-3P



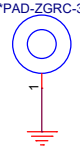
PAD1
*PAD-ZGRC-1NP



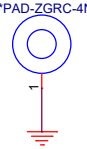
PAD2
*PAD-ZGRC-2NP



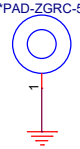
PAD3
*PAD-ZGRC-3NP



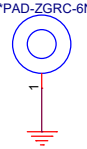
PAD4
*PAD-ZGRC-4NP



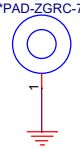
PAD5
*PAD-ZGRC-5NP



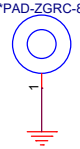
PAD6
*PAD-ZGRC-6NP



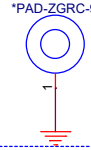
PAD7
*PAD-ZGRC-7NP



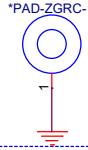
PAD8
*PAD-ZGRC-8NP



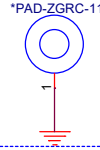
PAD9
*PAD-ZGRC-9NP



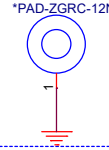
PAD10
*PAD-ZGRC-10NP



PAD11
*PAD-ZGRC-11NP



PAD12
*PAD-ZGRC-12NP

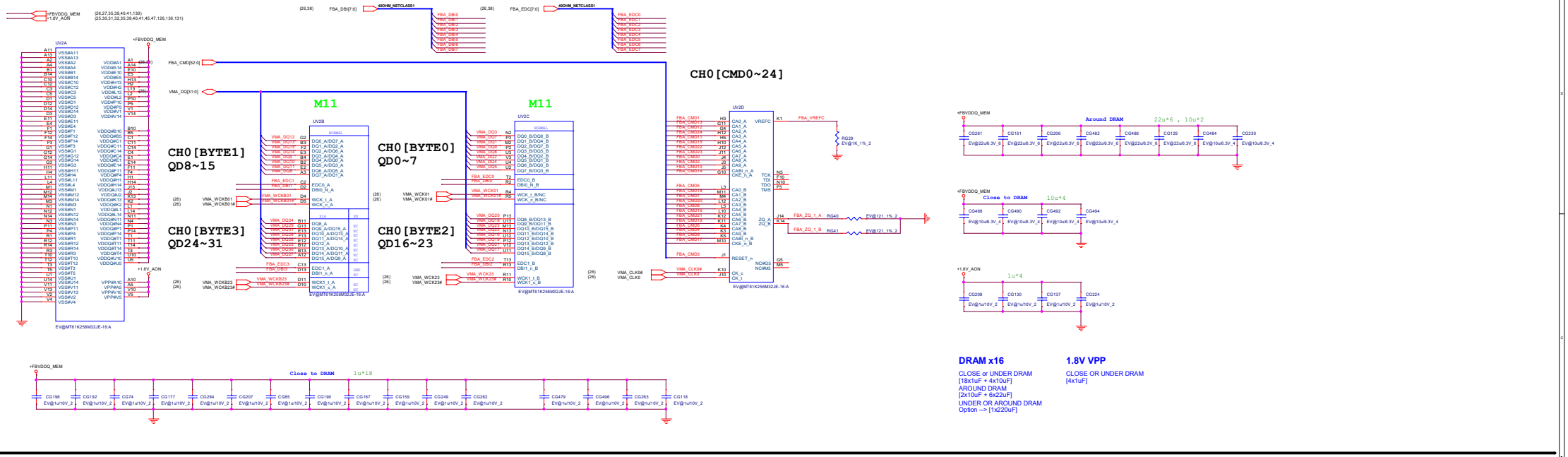


PVT

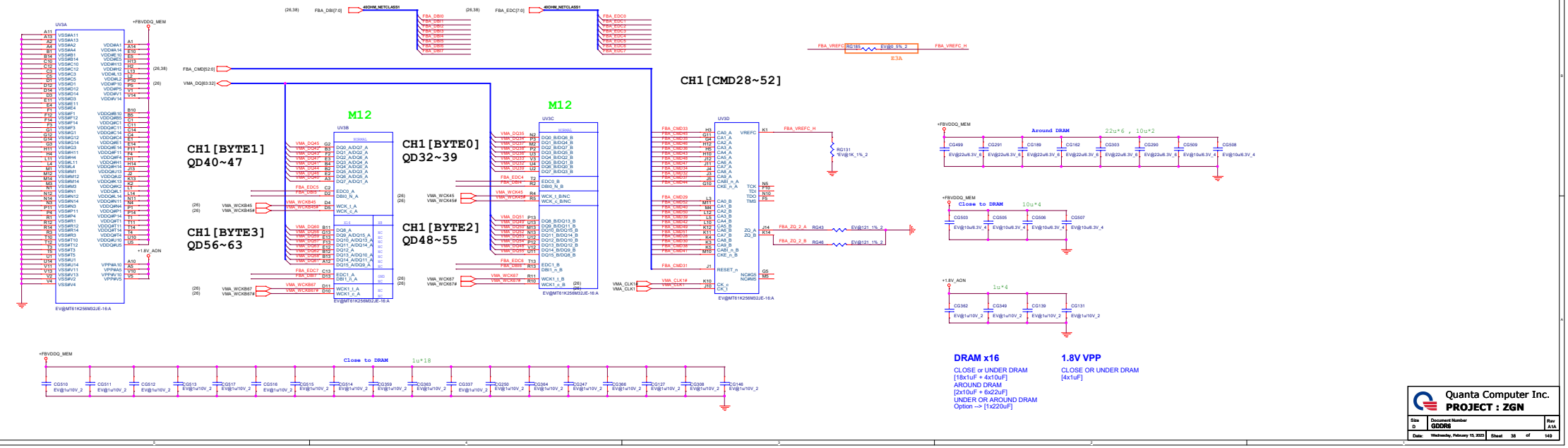
Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	**LTE DB**	A1A
Date: Wednesday, February 15, 2023	Sheet 37 of 149	

MEMORY: FBA Partition 31..0 x16 Dual Channel DRAM



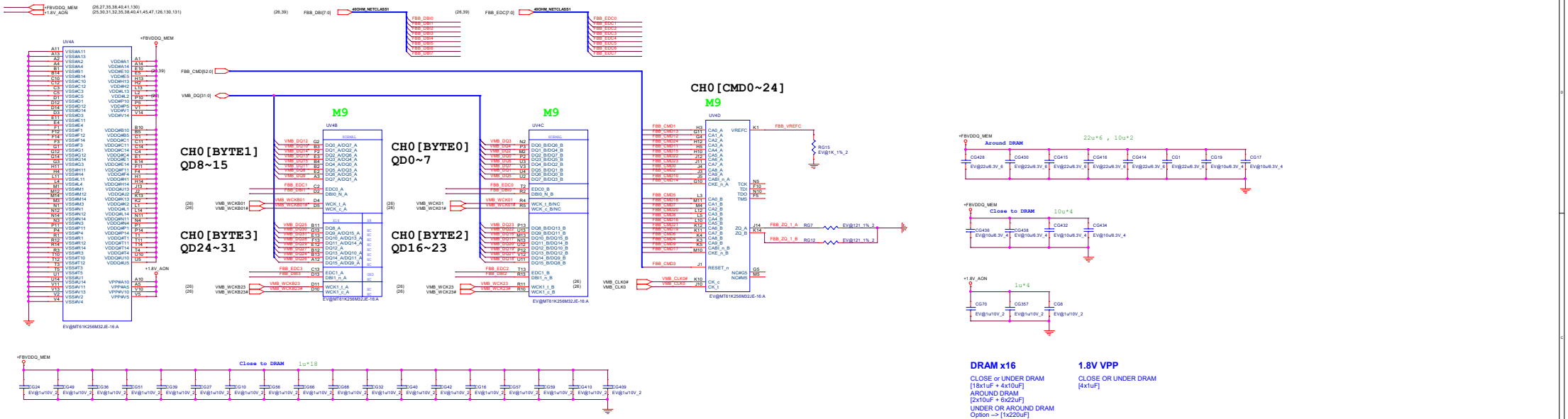
MEMORY: FBA Partition 63..32 x16 Dual Channel DRAM



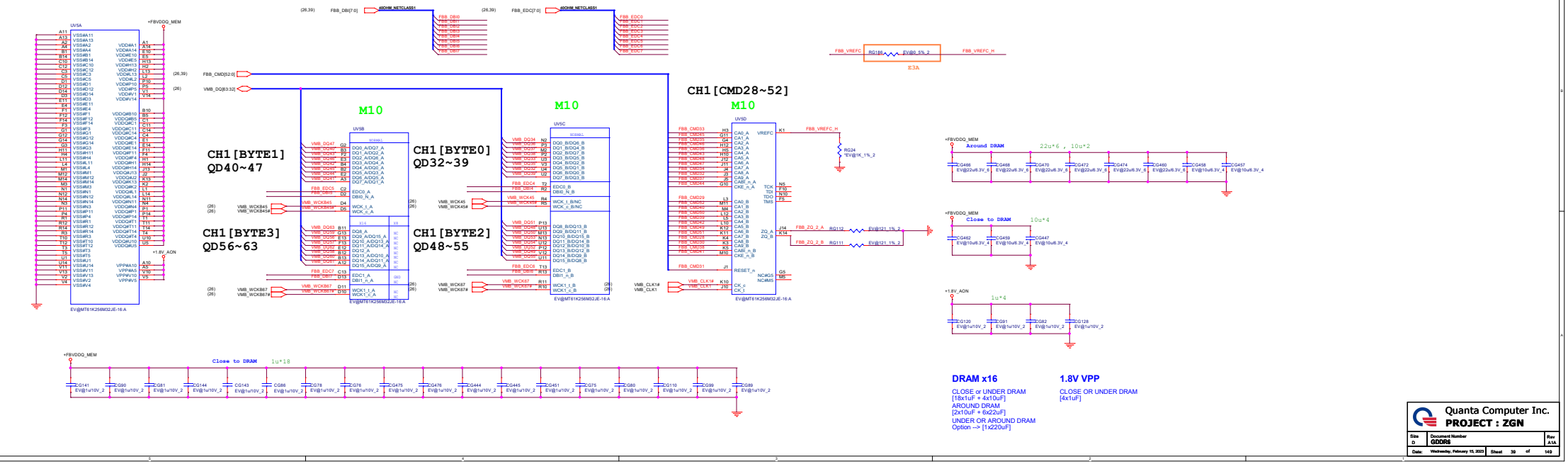
Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
D	GDDR6	A1A
Date: Wednesday, February 15, 2023	Sheet 38 of 142	

MEMORY: FBB Partition 31..0 x16 Dual Channel DRAM



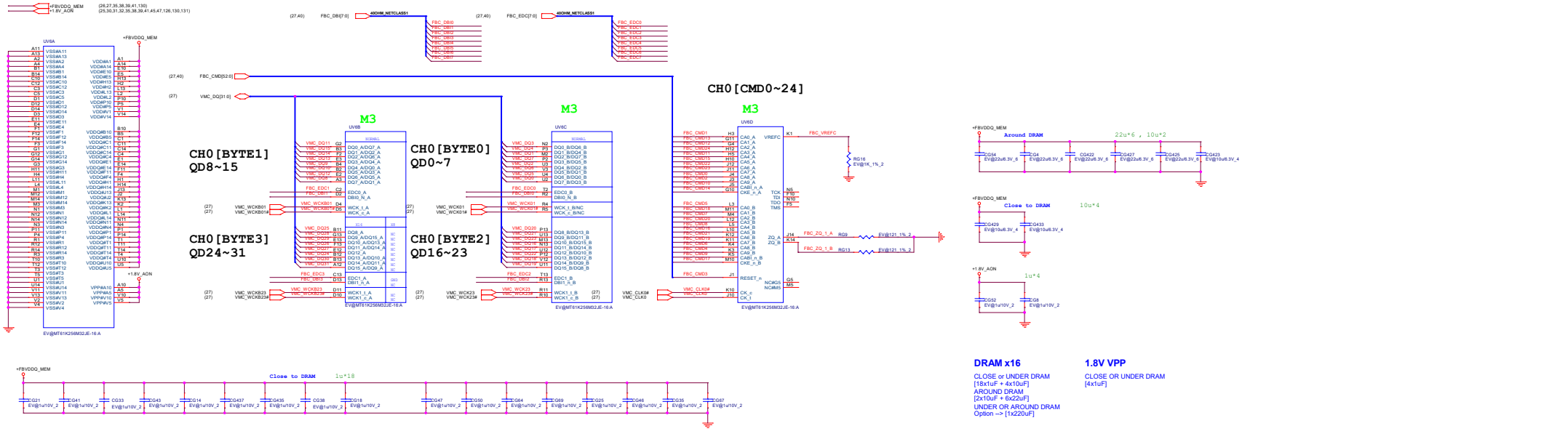
MEMORY: FBB Partition 63..32 x16 Dual Channel DRAM



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
D	GDDR6	A1A
Date: Wednesday, February 15, 2023	Sheet 39 of 142	

MEMORY: FBC Partition 31..0 x16 Dual Channel DRAM



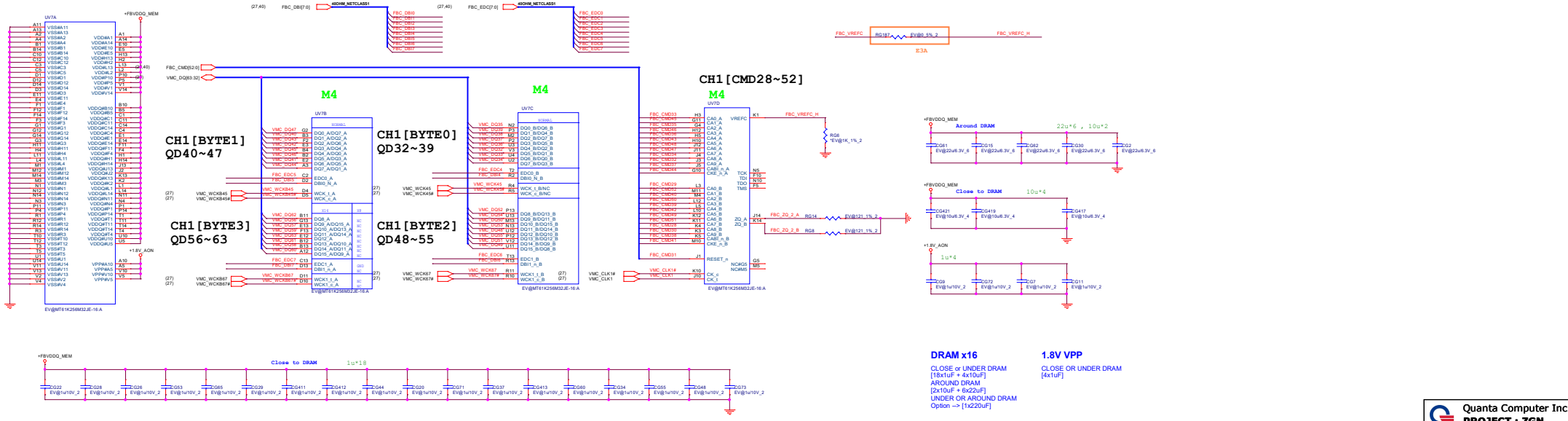
DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

MEMORY: FBC Partition 63..32 x16 Dual Channel DRAM



DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

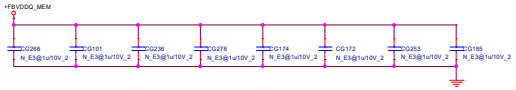
CLOSE OR UNDER DRAM
[4x1uF]

Quanta Computer Inc.
PROJECT : ZGN

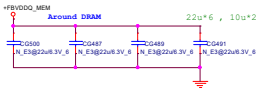
Size	Document Number	Rev
D	GDDR6	A1A
Date: Wednesday, February 15, 2023	Sheet 40 of 142	

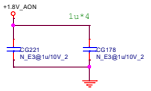
MEMORY: FBD Partition 31..0 x16 Dual Channel DRAM

Channel D is not use for GN20-E3



Close to DRAM 1u*18





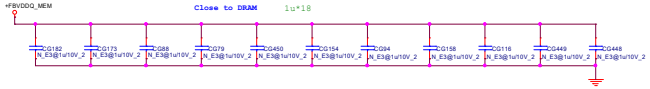
DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

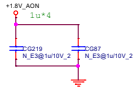
1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

MEMORY: FBD Partition 63..32 x16 Dual Channel DRAM



Close to DRAM 1u*18



DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
D	GDDR6	A1A
Date: Wednesday, February 15, 2023	Sheet 41 of 142	

Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

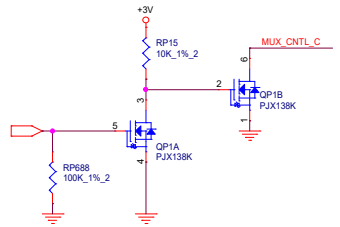
Size	Document Number	Rev
A	**LTE DB**	A1A

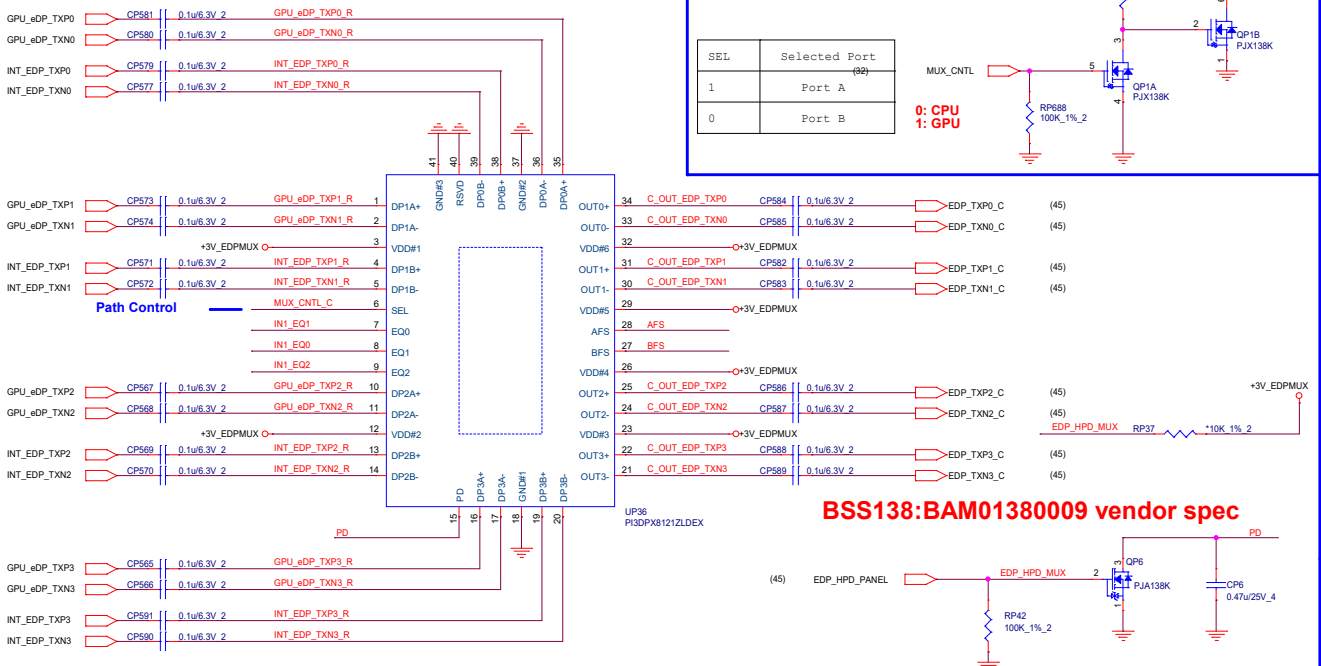
Date:	Wednesday, February 15, 2023	Sheet	43	of	149

MUX Control

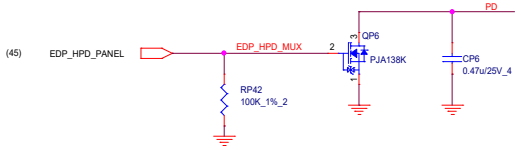
SEL	Selected Port (32)
1	Port A
0	Port B

0: CPU
1: GPU

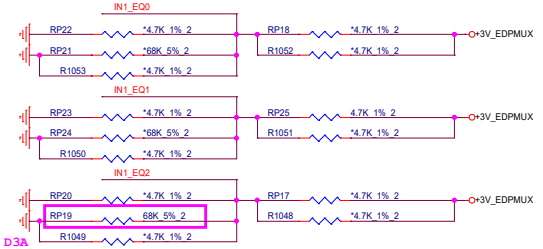




BSS138:BAM01380009 vendor spec



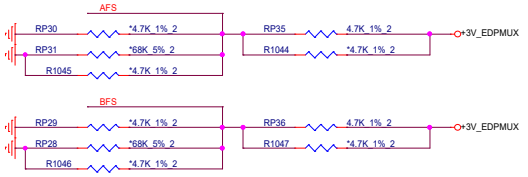
Input EQ



Port A		
Value	EQ0	EQ1
3.2 dB	0	0/R
3.8 dB	0	F/1
4.7 dB	R	0/R
5.9 dB	R	F/1
7.0 dB	F	0/R
7.8 dB	F	F/1
9.0 dB	1	0/R
10.3 dB	1	F/1

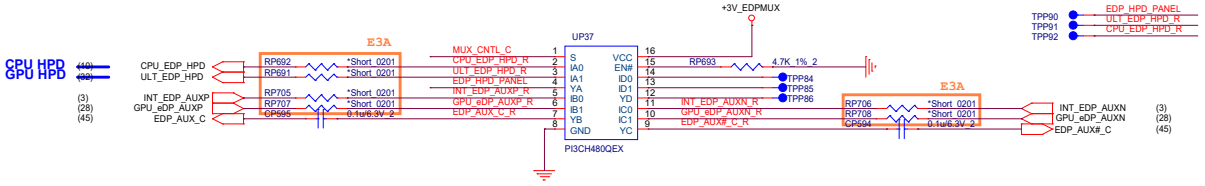
Port B		
Value	EQ2	EQ1
3.2 dB	0	0/F
3.8 dB	0	R/1
4.7 dB	R	0/F
5.9 dB	R	R/1
7.0 dB	F	0/F
7.8 dB	F	R/1
9.0 dB	1	0/F
10.3 dB	1	R/1

Gain and Output Swing

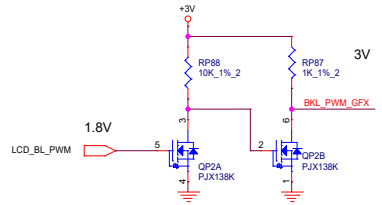


Gain	Swing	AFS or BFS
-3.5 dB	4.7K	0
-0.5 dB	4.7K	R
-3.5 dB	NC	F
-0.5 dB	NC	1

State	Pull-up	Pull-down
0	NC	0
R	NC	68K
F	NC	NC
1	0	NC

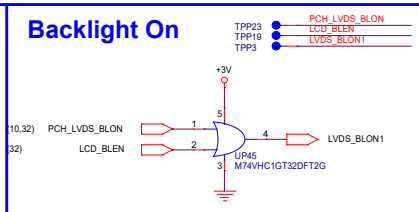


GPU PWM Level shift



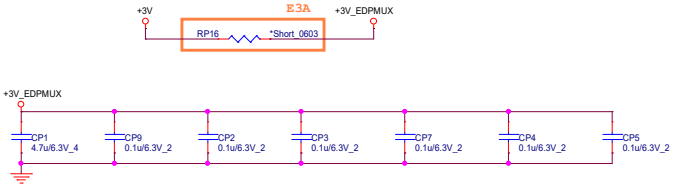
PWM OUT Enable Level shift

Backlight On

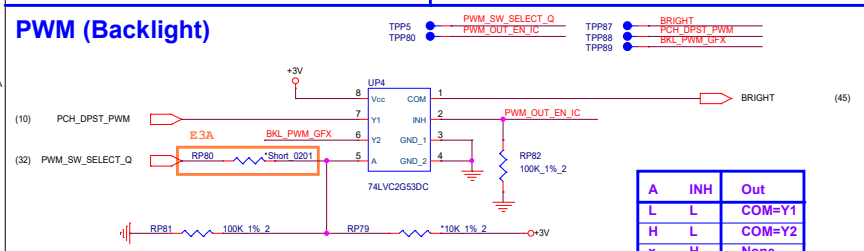


!! Take care "OR gate VIH" !!

Power

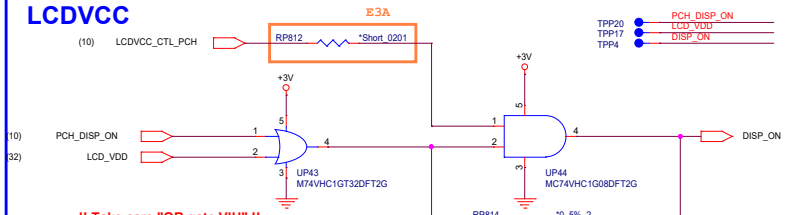


PWM (Backlight)



A	INH	Out
L	L	COM=Y1
H	L	COM=Y2
x	H	None

LCDVCC



!! Take care "OR gate VIH" !!

Quanta Computer Inc.
PROJECT : ZGN

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C	eDP MUX(PS8461E)	A1A
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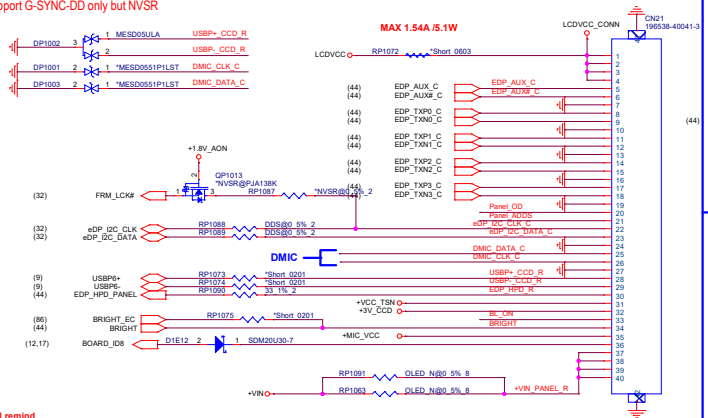
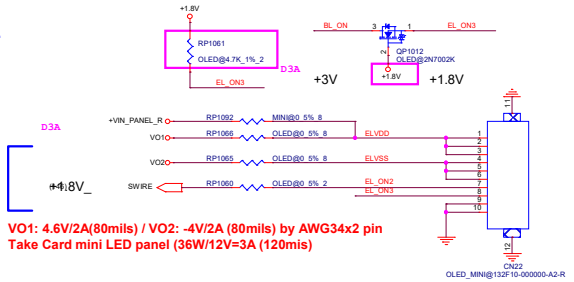
eDP

NV DDS support G-SYNC-DD only but NVSR



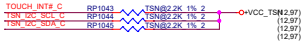
OLED Panel remind
■ VO1=ELVDD, VO2=ELVSS, Swire=EL_ON2 用AWG34
■所有"Power, "GND" 都要有實體cable 接出, 否則會有Abnormal display風險
■ PMIC GND 用AWG34
■ EL_ON3 Connect system GPIO(1.8V), like BL_EN and detail timing will release after kick off
■需用Coaxial線

OLED - Power Conn.

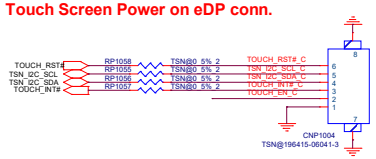


VO1: 4.6V/2A(80mils) / VO2: -4V/2A (80mils) by AWG34x2 pin
Take Card mini LED panel (36W/12V=3A (120mis)

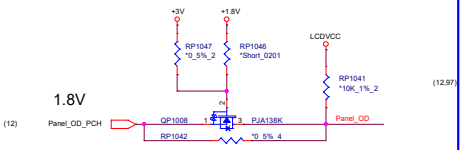
Touch Screen Conn.



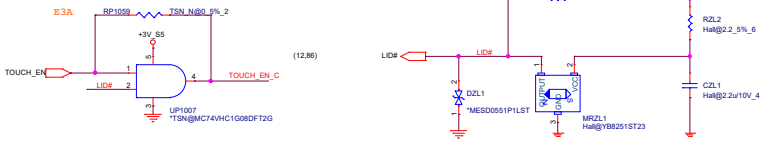
Touch Screen Power on eDP conn.



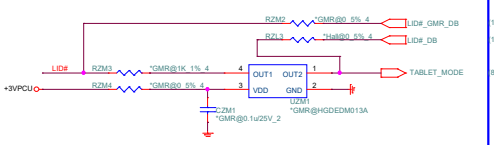
Panel OD control



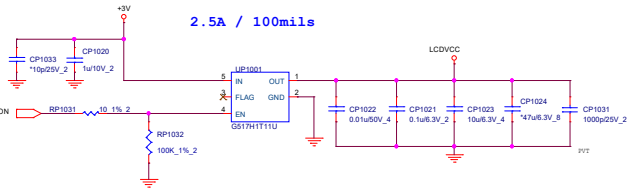
HALL Sensor

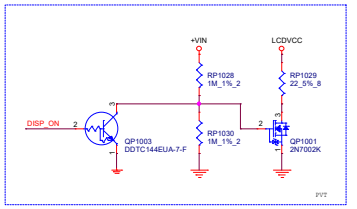


DB GMR/HALL Sensor

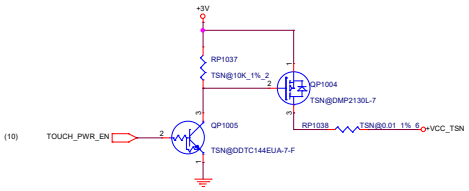


LCDVCC

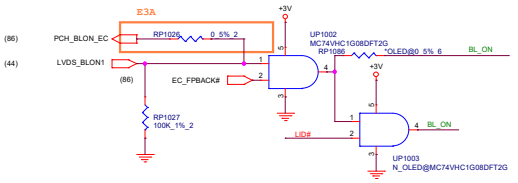




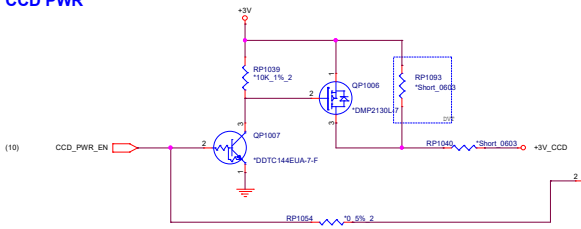
Touch Screen Power



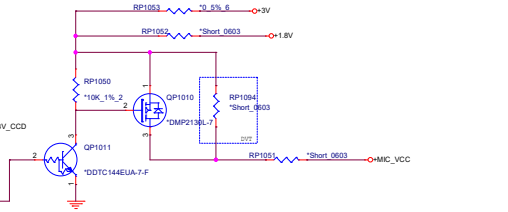
Backlight



CCD PWR

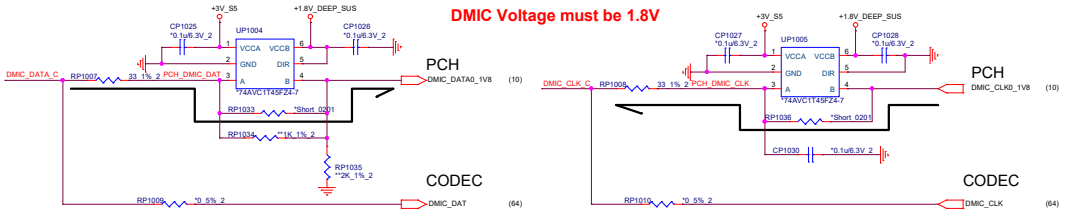


MIC PWR



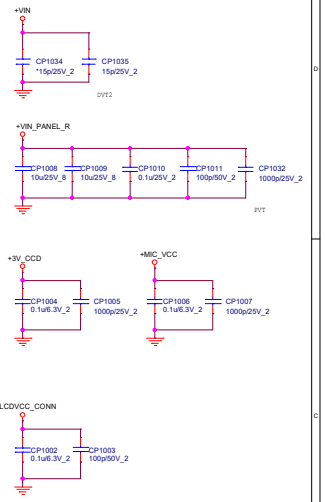
DMIC Level Shift (PCH)

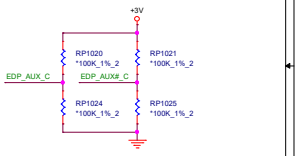
DMIC Voltage must be 1.8V

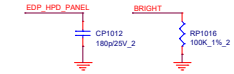


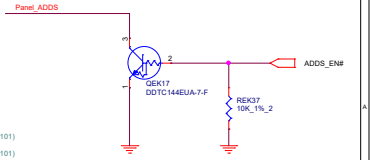
Remove 1pcs before measure

045









Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	eDP CONN.JCCD	A1A
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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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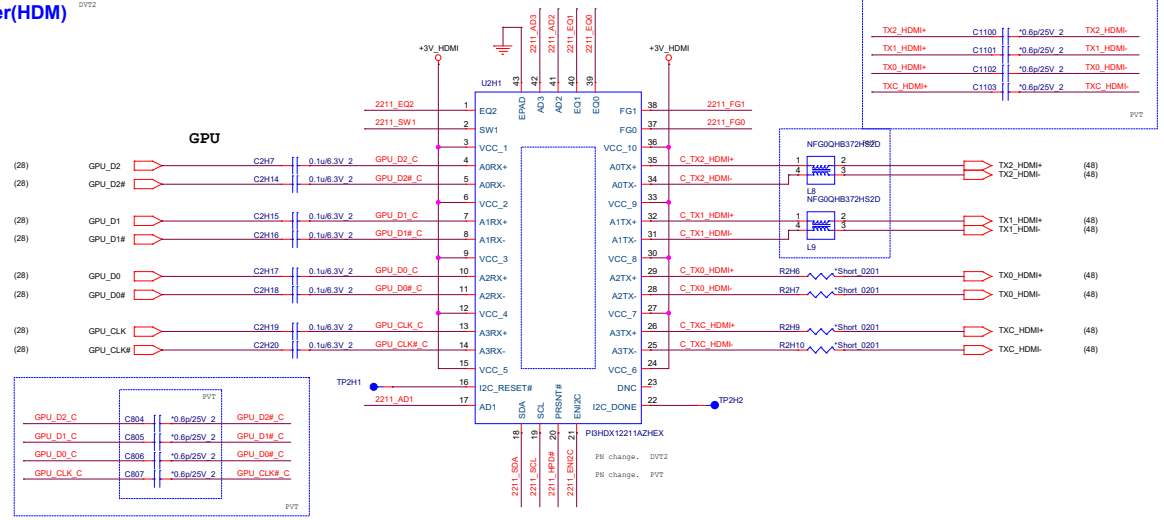
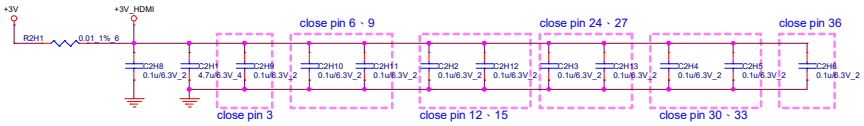
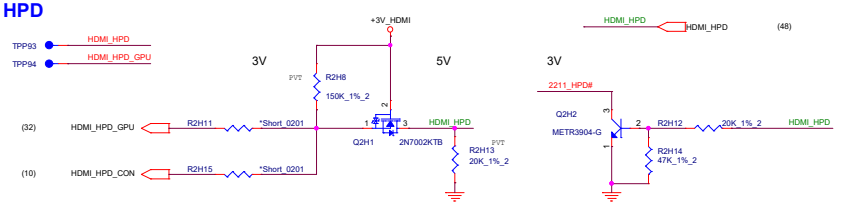
HDMI 2.1 ReDriver(HDM)



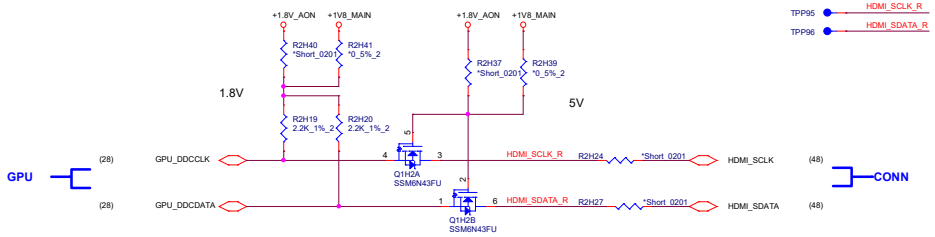
POWER



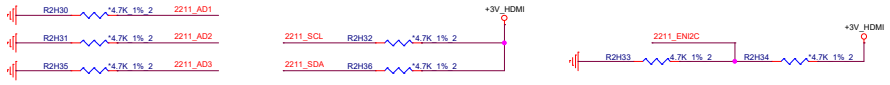
HPD



DDC



Reserve for I2C mode



0: GPIO Mode <--- Default
1: I2C Mode
NC: EEPROM

EQ2	EQ1	EQ0	Input EQ at 12Gbps
0	0	0	6.8dB
0	0	1	7.8dB
0	1	0	9.2dB
0	1	1	10.7dB
1	0	0	12.2dB
1	0	1	13.4dB
1	1	0	14.8dB
1	1	1	16.4dB

FG1	FG0	Output Pre-emphassis
0	0	-3.5dB
0	1	-2dB
1	0	-0.5dB
1	1	1.5dB

SW1	Output Pre-emphassis Swing
0	1000mV
1	1200mV

Quanta Computer Inc.
PROJECT : Helios(ZGRC)

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	HDMI retimer	1A

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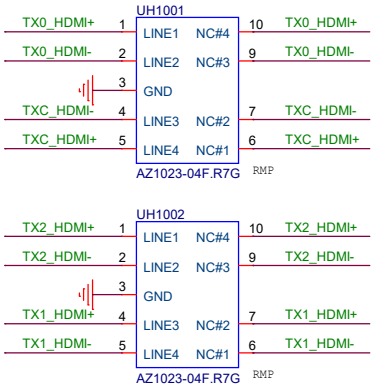
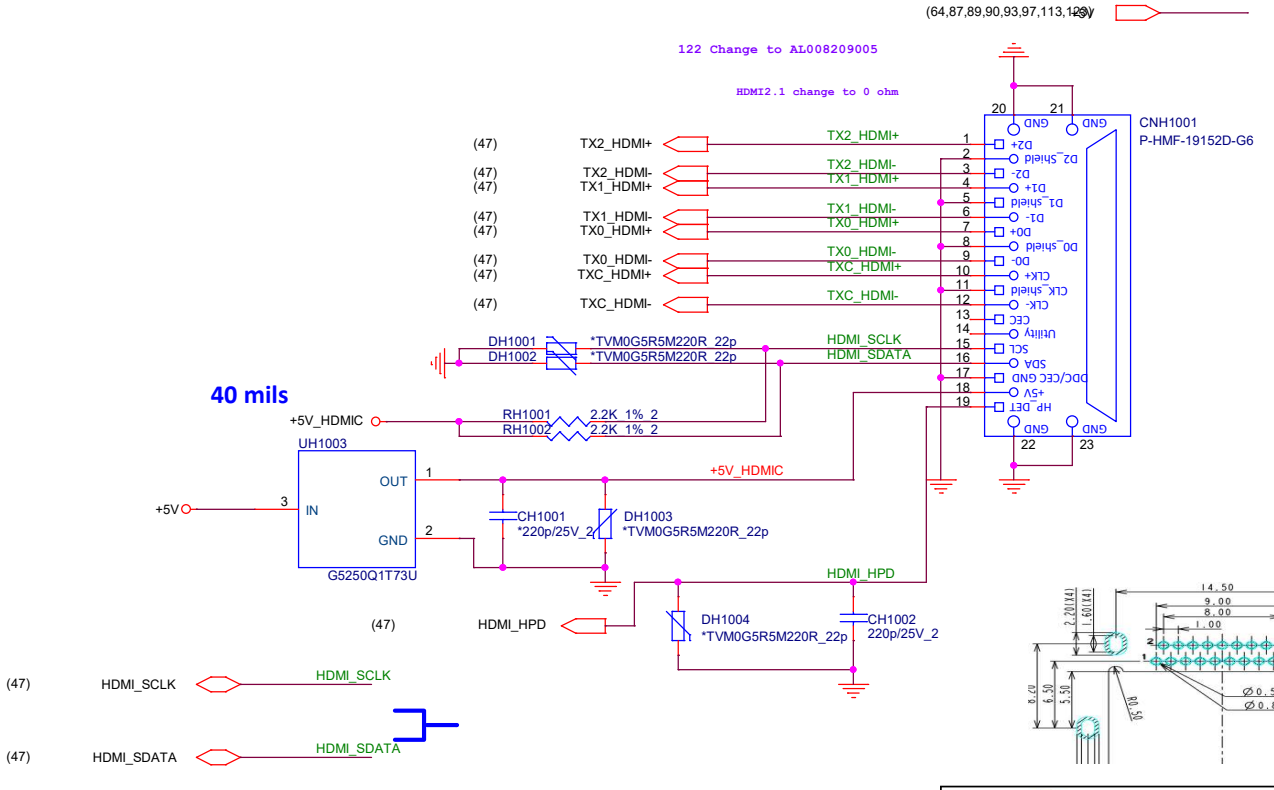
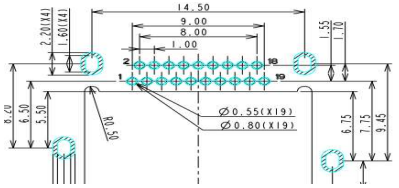
For ESD SOC

Layout note:Place close to HDMI Conn







Quanta Computer Inc.		
PROJECT : Helios(ZGRC)		
Size	Document Number: HDMI CONN	Rev: 1A
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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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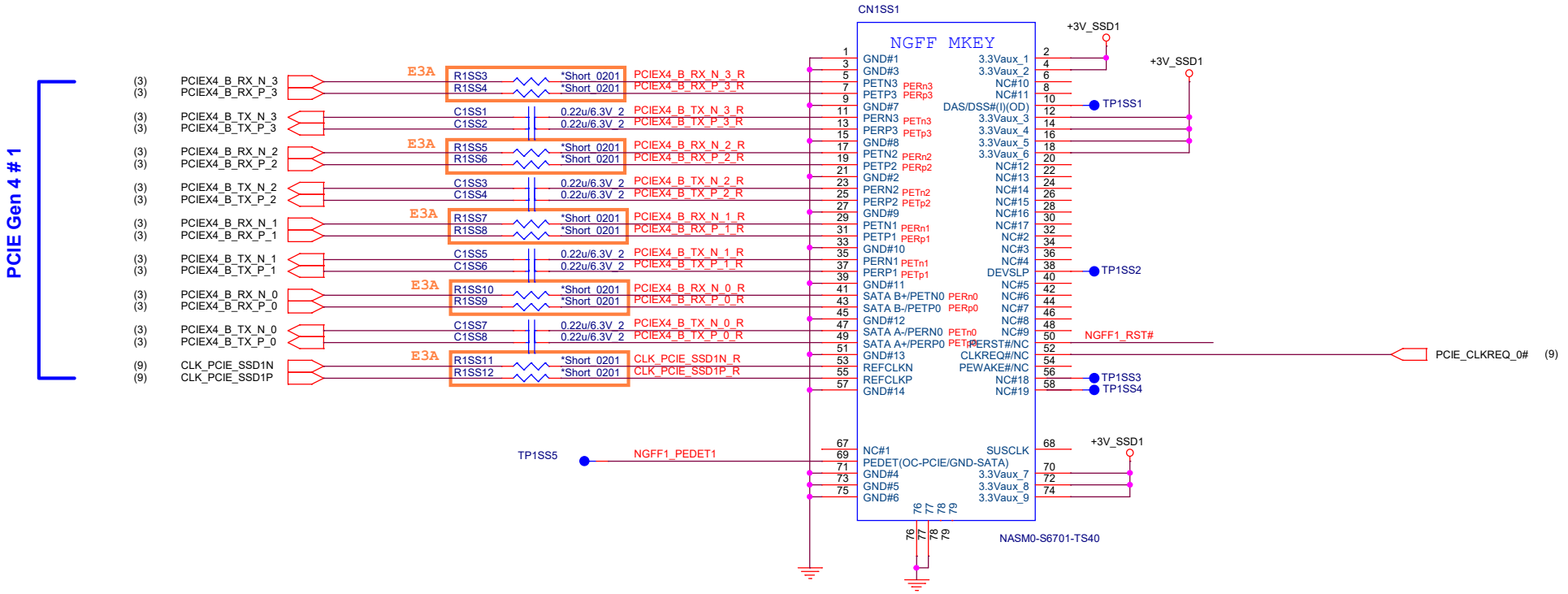
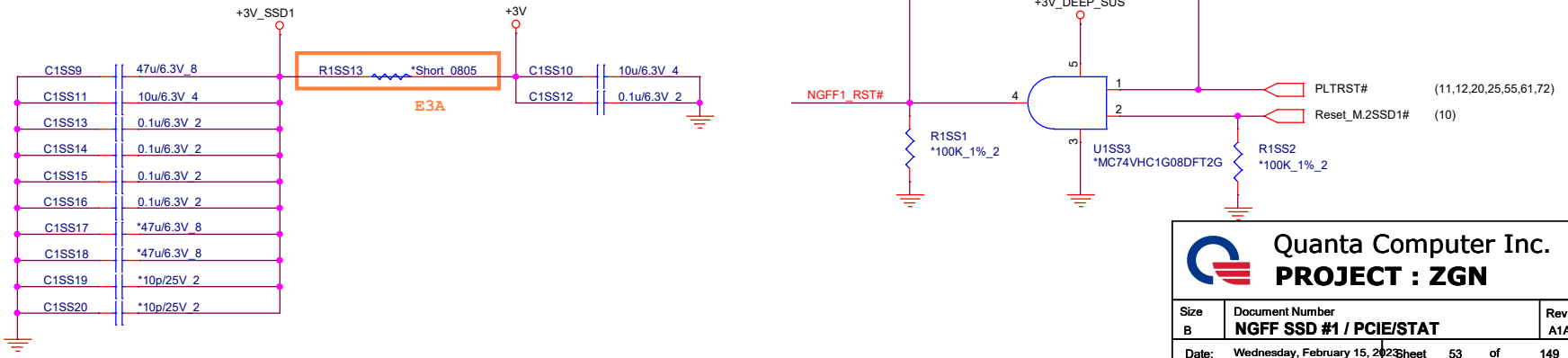
NGFF_M.2 SSD #1 (NGF)

PCIE 1X4 LR /SATA



DECOUPLING



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	NGFF SSD #1 / PCIE/STAT	A1A
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Size	Document Number	Rev
A	**LTE DB**	A1A

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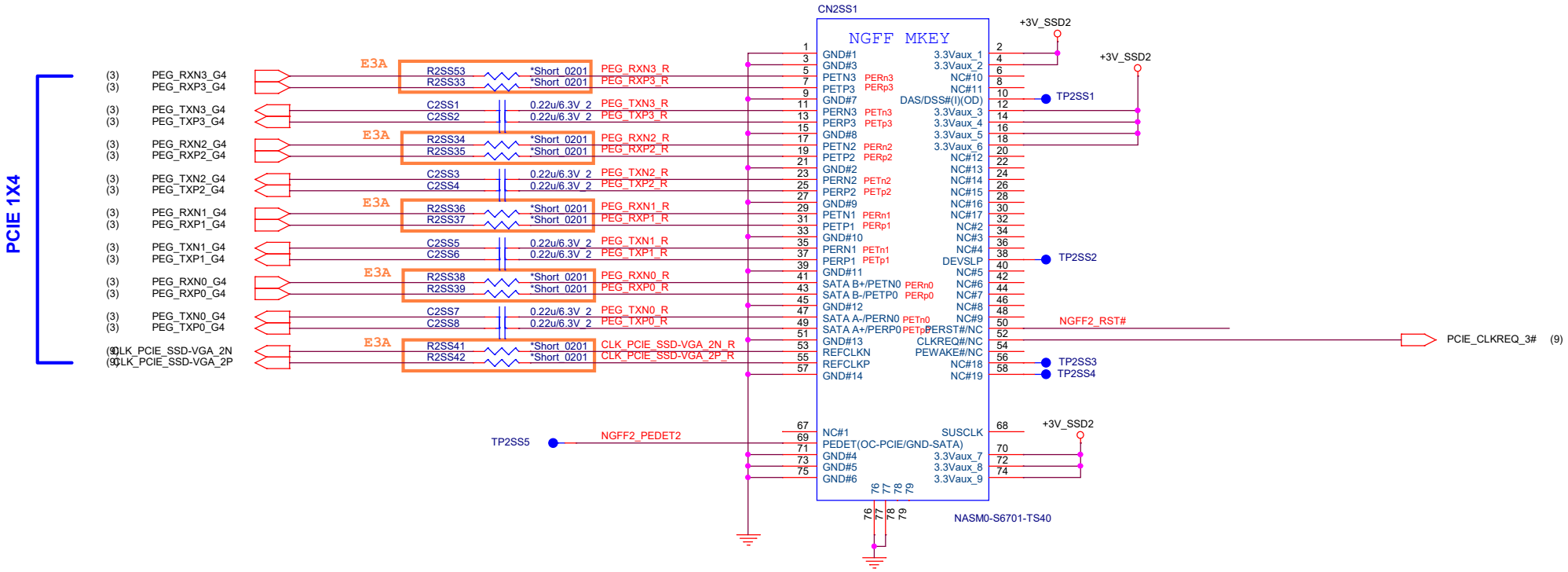
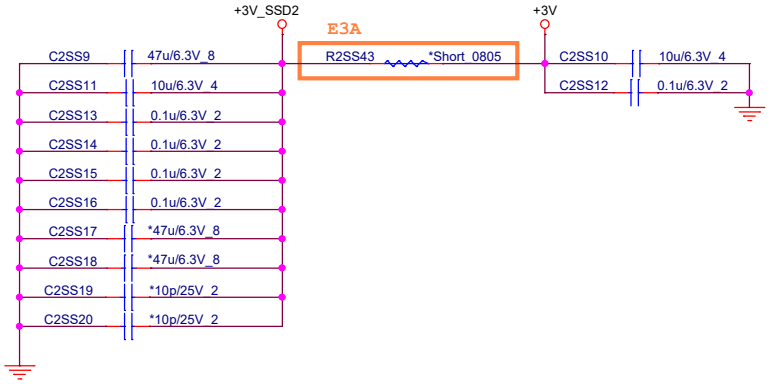
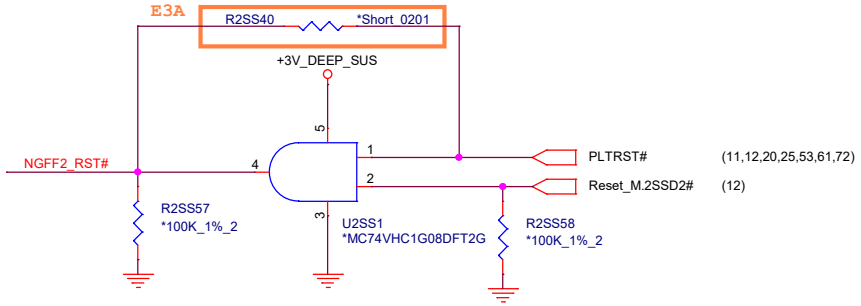
NGFF_M.2 SSD #2 (NGF)



DECOUPLING





Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	NGFF SSD #2 /PCIE	A1A
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Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

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A	**LTE DB**	A1A

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Quanta Computer Inc.

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Size	Document Number	Rev
A	**LTE DB**	A1A

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Size	Document Number	Rev
A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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NGFF_M.2 WiFi & BT (NGF)

E-Key

CN1FW1
NASE0-S6701-TSH4

NGFF EKEY

BT
USBP14+
USBP14-
R1063 *Short_0201
R1064 *Short_0201

CNVi RX
WR_LANE1_DN
WR_LANE1_DP
WR_LANE0_DN
WR_LANE0_DP
WR_CLK_DN
WR_CLK_DP

DISCRETE WIFI
PCIE_TXP_WLAN
PCIE_TXN_WLAN
C1FWR1 0.1u/6.3V_2 PCIE_TXP_WLAN_C
C1FWR2 0.1u/6.3V_2 PCIE_TXN_WLAN_C
PCIE_RXP_WLAN
PCIE_RXN_WLAN
CLK_PCIE_WLANP
CLK_PCIE_WLANN
WLAN_CLKREQ#
WLAN_WAKE_R#

CNVi TX
WT_LANE1_DN
WT_LANE1_DP
WT_LANE0_DN
WT_LANE0_DP
WT_CLK_DN
WT_CLK_DP

+WL_VDD
TP1FWR1
TP1FWR2
TP1FWR3
CNV_RF_RESET_L
MODEM_CLKREQ_L
CNV_BRI_RSP_R R1FWR2 39_1%_2 UART_WAKE_N (12) CNV_BRI_RSP (10)
CNV_RGI_RSP_R R1FWR3 39_1%_2 CNV_RGI_DT (10,15) CNV_RGI_RSP (10) CNV_BRI_DT (10,15)
R1FWR30 *Short_0201 CLINK_RESET (11)
R1FWR31 *Short_0201 CLINK_DATA (11)
R1FWR32 *Short_0201 CLINK_CLK (11)
CNV_PA_BLANKING (10)
CNV_MFUART2_TXD (10)
CNV_MFUART2_RXD (10)
SUSCLK_32K (11)
WLAN_RST#
BT_EN_R
RF_EN_R
R1FWR10 *Debug@0_5%_4 2ND_MBDATA
R1FWR11 *Debug@0_5%_4 2ND_MBCLK
PULSAR_38P4M_REFCLK 38.4M : not supported and not connected by HrP.
TP1FWR4
R1FWR12 Debug@0_5%_4
R1FWR13 Debug@0_5%_4 2ND_MBDATA
R1FWR14 Debug@0_5%_4 2ND_MBCLK
AP_SLP_S0_L (12,20)
2ND_MBDATA (75,86,93)
2ND_MBCLK (75,86,93)

E3A
R1FWR27 *Short_0201
+WL_VDD
U1FWR2 *NL17SZ08DFT2G
PLTRST# (11,12,20,25,53)
PCH_WLAN_RST# (10)
M.S. for Dis. module only
R1FWR7 *0_5%_2
R1FWR4 *0_5%_2 BT_EN (86)
R1FWR1 *Short_0201 BT_OFF_PCH# (12)
R1FWR6 *Short_0201 RF_EN_PCH (12)
R1FWR8 *0_5%_2 RF_EN (86)

PU/PD

+WL_VDD
BT_EN_R R1FWR16 10K_1%_2
RF_EN_R R1FWR17 10K_1%_2
PCH_WLAN_RST# R1FWR20 *100K_1%_2
R1FWR21 *100K_1%_2 WLAN_RST#

By Control
+WL_VDD
+3V
R1FWR26
10K_1%_2
S0
WLAN_CLKREQ#
Q1FWR2 2N7002KTB
PCIE_CLKREQ_1# (9)

Wake

By Control
+WL_VDD
+WL_VDD
R1FWR28
10K_1%_2
S5
WLAN_WAKE_R#
Q1FWR3 2N7002KTB
WLAN_WAKE# (11)

LEVEL SHIFT

1.8V
+1.8V_DEEP_SUS
CNV_RF_RESET# (12)
R1FWR15 *0_5%_2
R1FWR24 *75K_1%_2
U1FWR3 NL17SZ08DFT2G
CNV_RF_RESET_L
R1FWR25 *75K_1%_2
DVT

MODEM_CLKREQ (12)
R1FWR18 *0_5%_2
R1FWR29 75K_1%_2
U1FWR4 NL17SZ08DFT2G
MODEM_CLKREQ_L

POWER SWITCH

+3V_S5
+WL_VDD
R1FWR9 *Short_0805
Q1FWR1 DMP2130L-7
C1FWR3 1u/10V_2
R1FWR19 100K_1%_2
C1FWR4 10u/6.3V_4
C1FWR5 0.1u/6.3V_2
C1FWR6 0.1u/6.3V_2
C1FWR7 0.1u/6.3V_2
R1FWR22 10K_1%_2 WLANPWR# (86)
R1FWR23 *10K_1%_2 SLP_WLAN_PWR# (11)
M.S. for Dis. module only

WLANPWR# --> RSMRST#

+WL_VDD
C1FWR8 10u/6.3V_4
C1FWR9 10u/6.3V_4
C1FWR10 0.1u/6.3V_2
C1FWR11 0.1u/6.3V_2
C1FWR12 *0.1u/6.3V_2
C1FWR13 0.01u/10V_2
C1FWR14 0.01u/10V_2

+WL_VDD
C1FWR15 *10p/25V_2
C1FWR16 *10p/25V_2

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Quanta Computer Inc.

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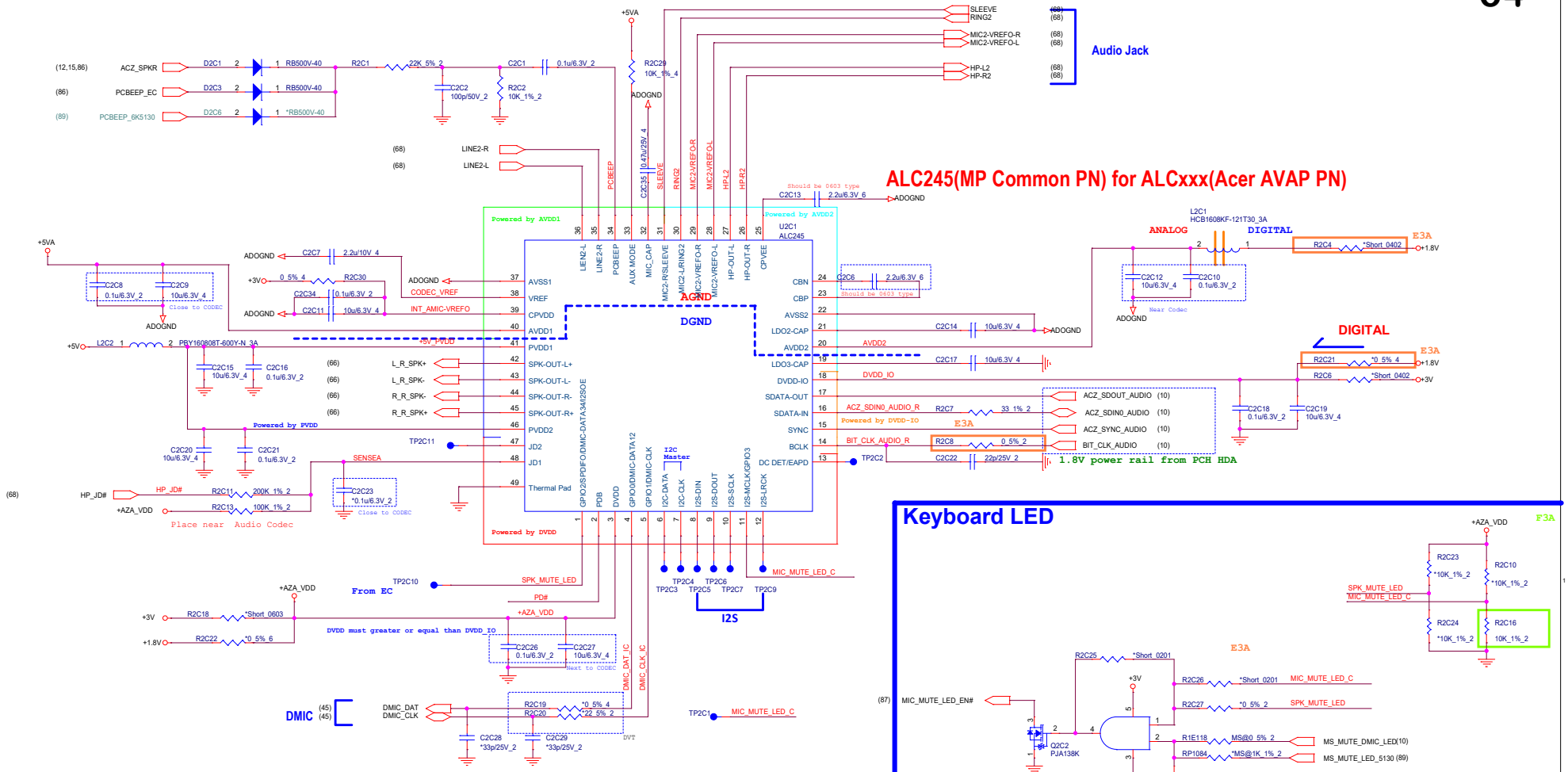
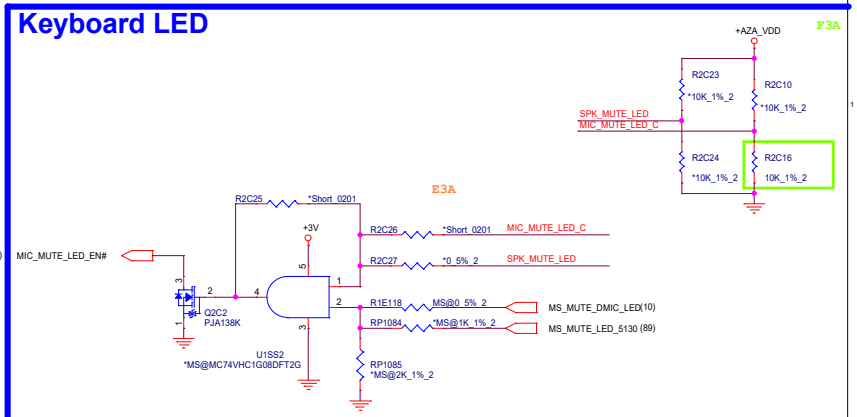
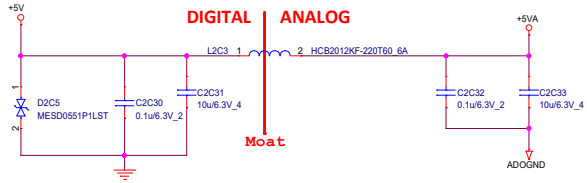
Codec ALC3324 (ADO)



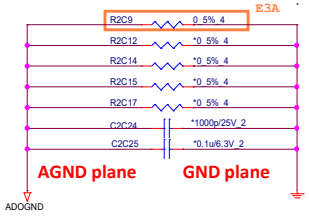
Keyboard LED



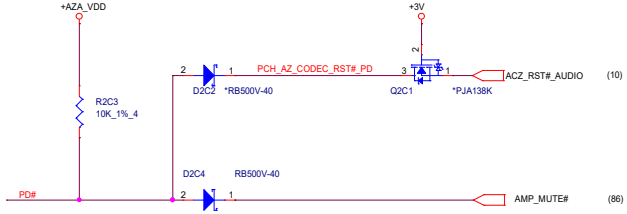
Codec PWR 5V(ADO)



GROUND MOAT



Mute(ADO)



Quanta Computer Inc.
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C	Azalia ALC295M	A1A
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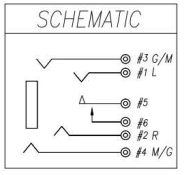
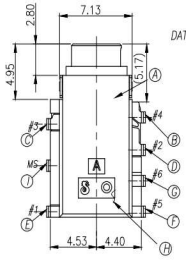
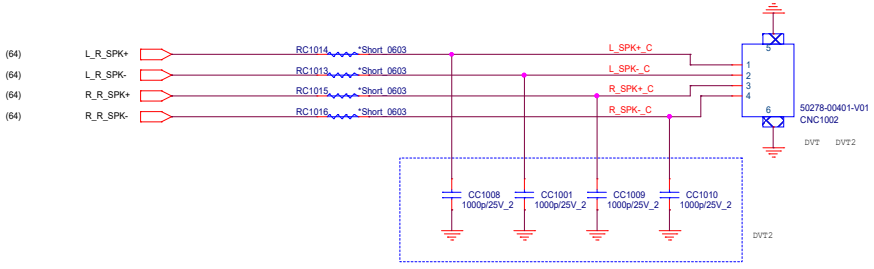
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

Reference select with Line in and without line in

Reference







Quanta Computer Inc.
PROJECT : Nitro(ZGS)

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Quanta Computer Inc.

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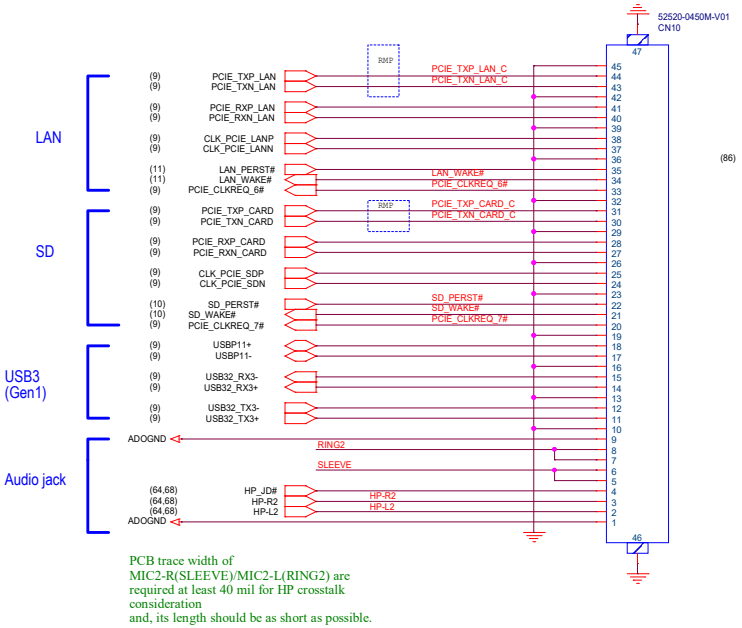
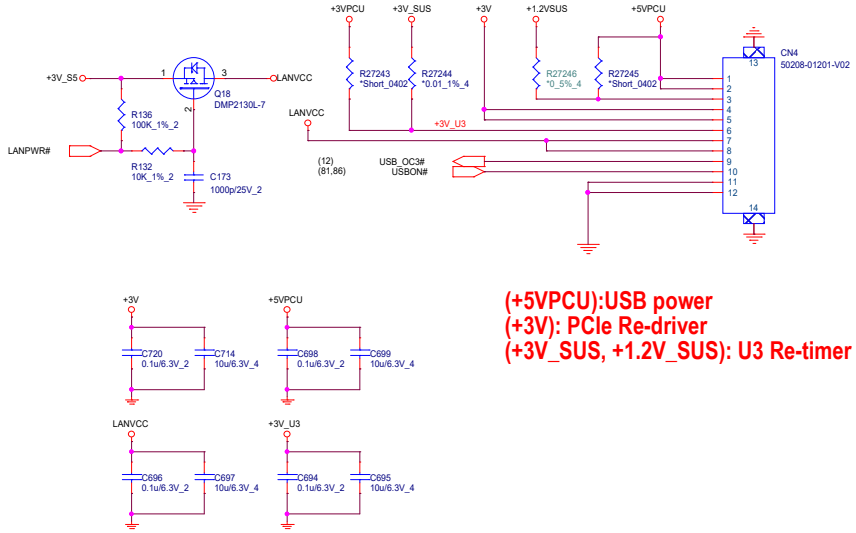


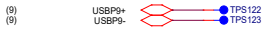
PCB trace width of
MIC2-R(SLEEVE)/MIC2-L(RING2) are
required at least 40 mil for HP crosstalk
consideration
and, its length should be as short as possible.



機構留12Pin

(+5VPCU):USB power
(+3V): PCIe Re-driver
(+3V_SUS, +1.2V_SUS): U3 Re-timer

確認SD最後決定走PCIe還是USB !!

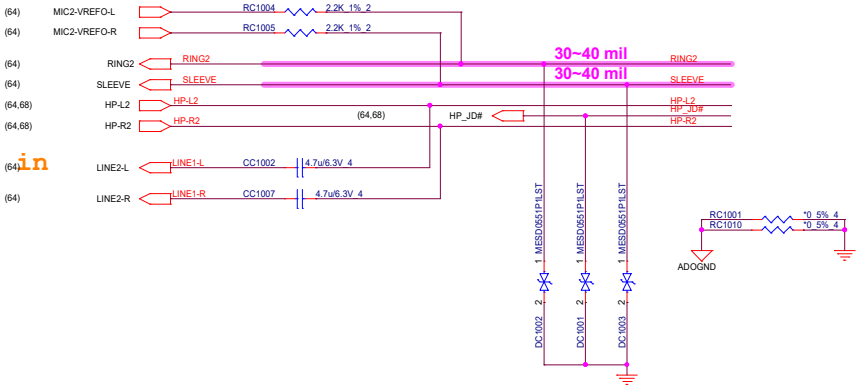


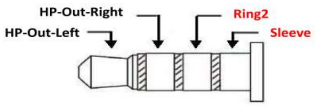
MIC2 DC Bias

U3 Re-timer Level shift

注意Placement與Routing (包在AGND中間)

with Line in circuit





Quanta Computer Inc.
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Quanta Computer Inc.

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PROJECT : ZGN

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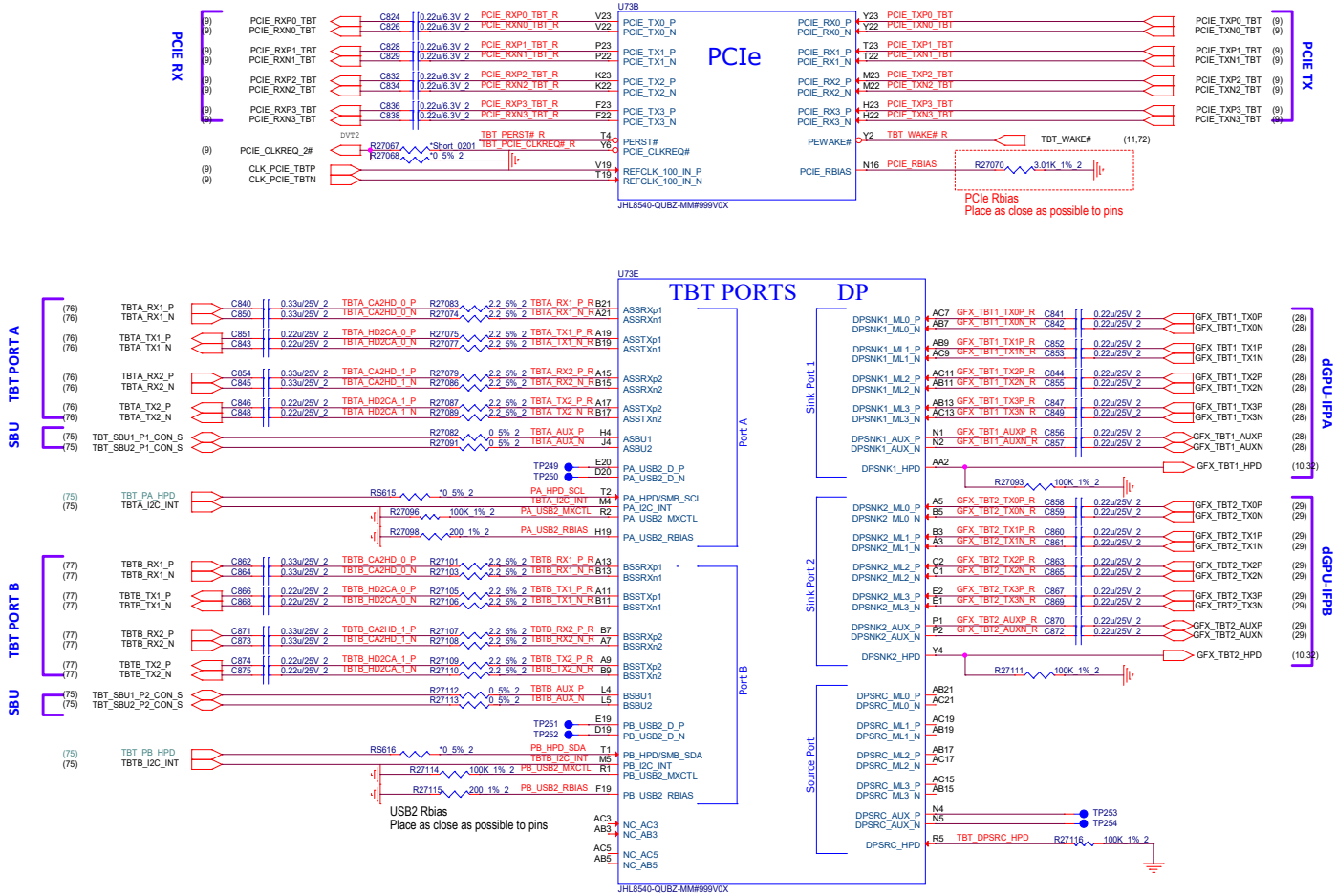
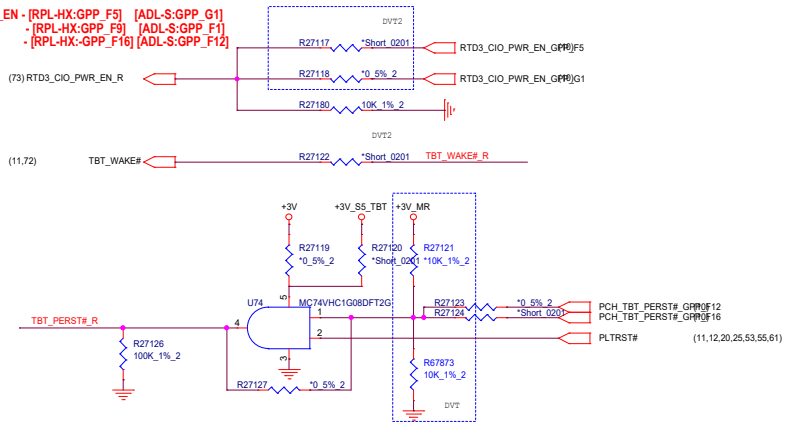
Intel Maple-Ridge (1/3)



RTD3

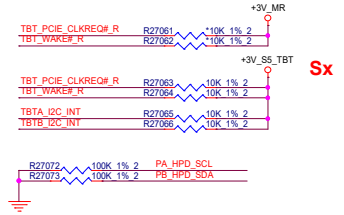
RTD3_PWR_EN - [RPL-HX:GPP_F5] [ADL-S:GPP_G1]
WAKE_N - [RPL-HX:GPP_F9] [ADL-S:GPP_F1]
PERST# - [RPL-HX:GPP_F16] [ADL-S:GPP_F12]



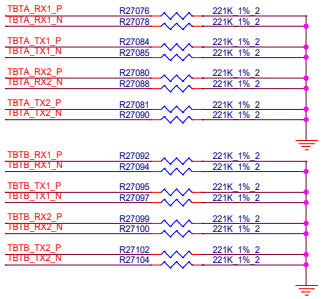
DP AUX Slew Rate Control Caps

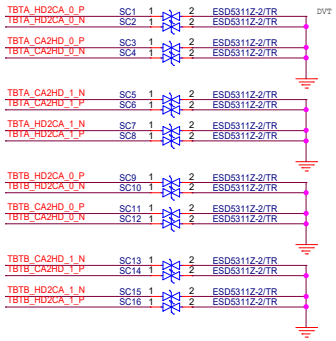
CRB no stuff , Check list stuff

HW Pull-Up/Pull-Down

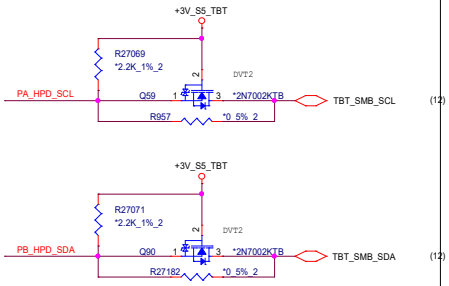


Discharge bleeding resistors





SMBUs(vPRO)



Quanta Computer Inc.
Project: HP-MONTES

Title: Intel Maple-Ridge (1/3)
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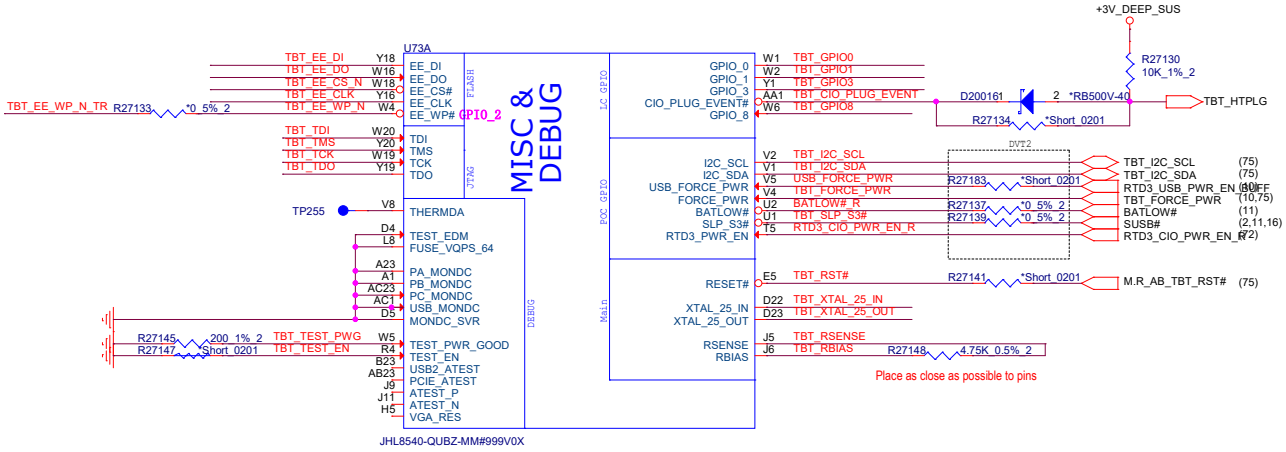
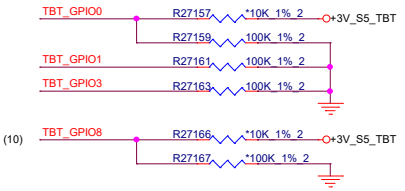
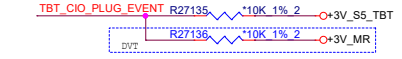
Intel Maple-Ridge (2/3)



GPIO

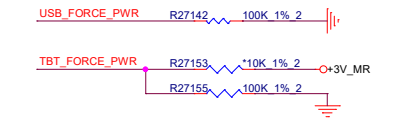


CIO_PLUG_EVENT

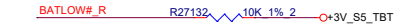


I2C - To PD

Force Power (1:Enable)

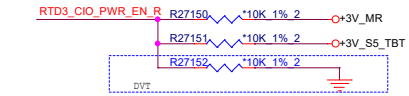


Battery Low (Low-> Prevent wake up)

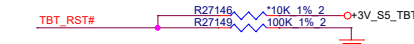


S3 Indicate

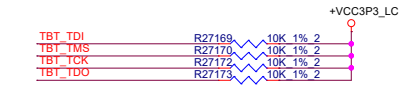
RTD3 (Power off PCIe I/F)



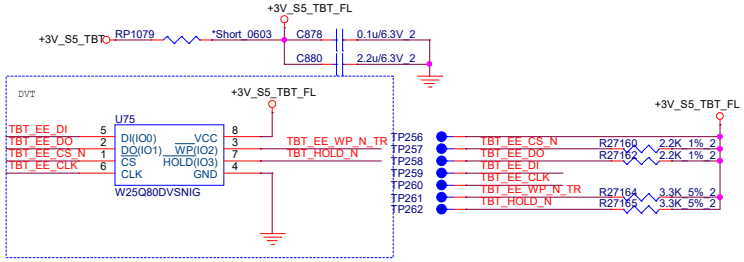
Reset (Main Power)



JTAG

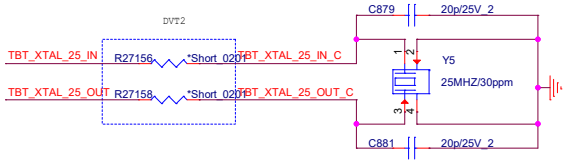


8Mbit Flash



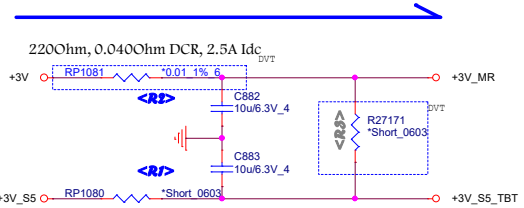
Crystal

25MHz, 30ppm, 20pF TR Crystal



Must use Metal shielded crystal for better noise immunity.

Power



From 3.3v_S0 System Power Rail
Maximum Required Power: 3.3v @ 1A

From 3.3v_SX System Power Rail
Maximum Required Power: 3.3v @ 150mA

Wake Support:

Option 1 for wake support over TBT:
1. Connect <R1> and <R3>. Keep <R2> empty.
2. Make sure PW_VCC3v3_SX_SYS can support TR maximum power consumption.
3. Simple Bios implementation

Option 2 for wake support over TBT:
1. Connect <R1> and <R2>. Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from TR
1. Connect <R2> and <R3>. Keep <R1> empty.

TP264 TBT_CIO_PLUG_EVENT
TP268 USB_FORCE_PWR
TP269 TBT_FORCE_PWR
TP267 RTD3_CIO_PWR_EN_R
TP270 TBT_RST#

Quanta Computer Inc.
Project: HP-MONTES

Title: Intel Maple-Ridge (2/3)		
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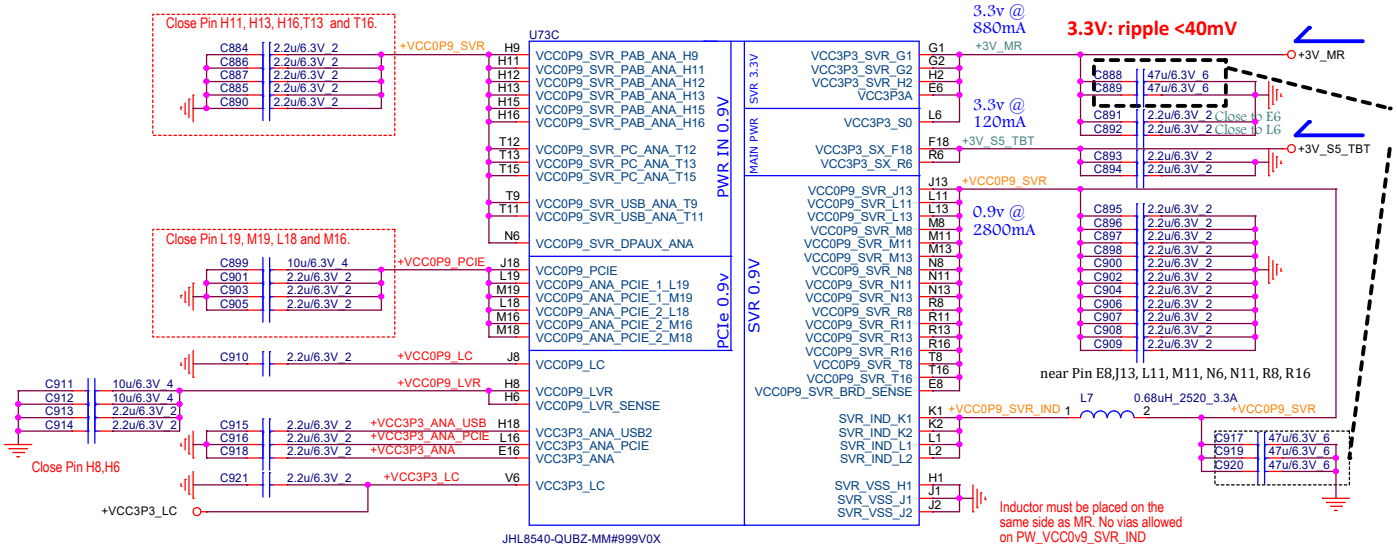
Intel Maple-Ridge (3/3)



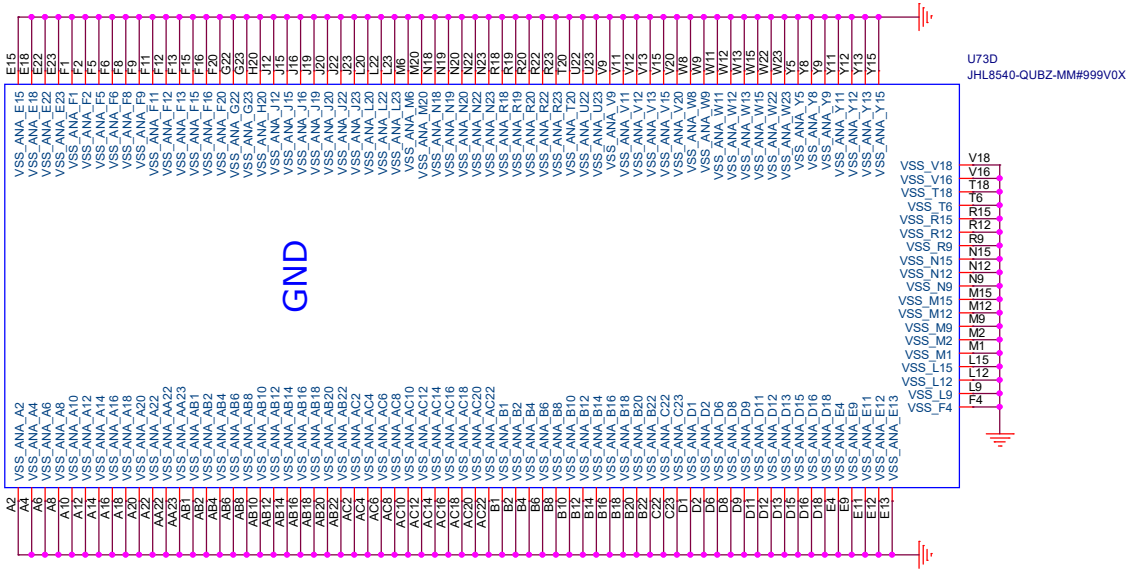


Table 350. External Inductor Parameters

Inductance decreasing at 2.8A	0.6µH			10%
	0.68µH			20%

Titan Ridge DP

Figure 32. Power On Sequence

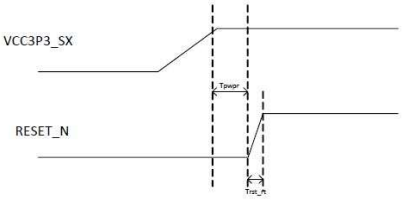


Table 436. Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

Quanta Computer Inc.

Project: HP-MONTES

Title: TBT3-Alpine Ridge (2/2)

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SU1 : QPN:TBD CYPD6227-96BZXI(BGA)

BGA :-6mm x 6mm x 0.5mm

VDDD supply output

CCG6DF

CYPD6227-96BZXI

PART_NUMBER = CCG6DF

Manufacturer = Cypress

To MR

To EC

I2C_SLAVE TO COMMUNICATE WITH EMBEDDED CONTROLLER

Address 0x08 (7bits)

Active High

TO CONN P0

TO CONN P1

TO M.R (P0)

TO M.R (P1)

PD to BBR

I2C master to configure Re-timer

Address Port1:0x40/Port2:0x41

Close to IC ball out

PD Adapter OCP

I2C To EC

S5 /PCU

ALW

To Re-timer

I2C To M.R.

S5 /PCU

S5

Port A

Port B

TO M.R

PROCHOT

Address Setting

For update PD FW

Address 0x08(7bits)

Address 0x10(8bits)

Note:
CCG5/CCG5C I2C address is decided by the SWD clock pin.
Don't mount SR2 and SR5 for the I2C address 0x08. This is the default one. (Floating.)
Mount only SR5 for the I2C address 0x40. (PD)
Mount only SR2 for the I2C address 0x42. (PU)

test points sequence and pitch. (2.54mm with PHY 1.02)

CCG6 SWD PROGRAMMING HEADER

Adapter Control

from Power

to CCG6

from CCG6

to Power

to EC

Quanta Computer Inc.

PROJECT : Helios(ZGRC)

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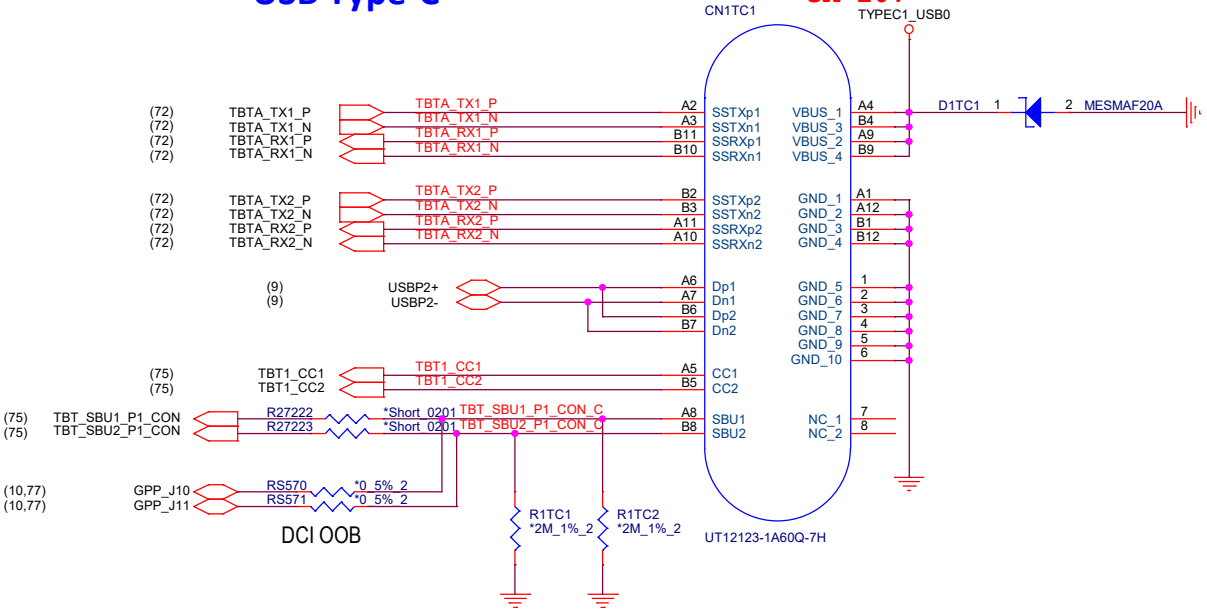
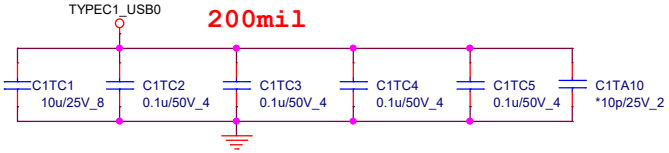
USB Type-C

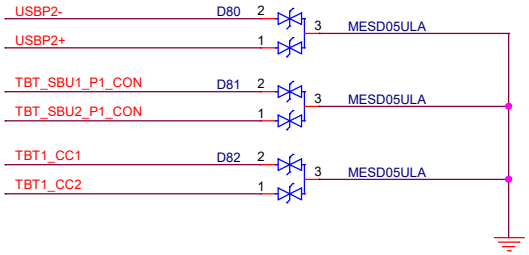
200mil
5A 20V



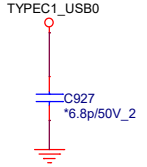
Power Capacitance



ESD



RF CAPS



Quanta Computer Inc.
PROJECT : ZGN

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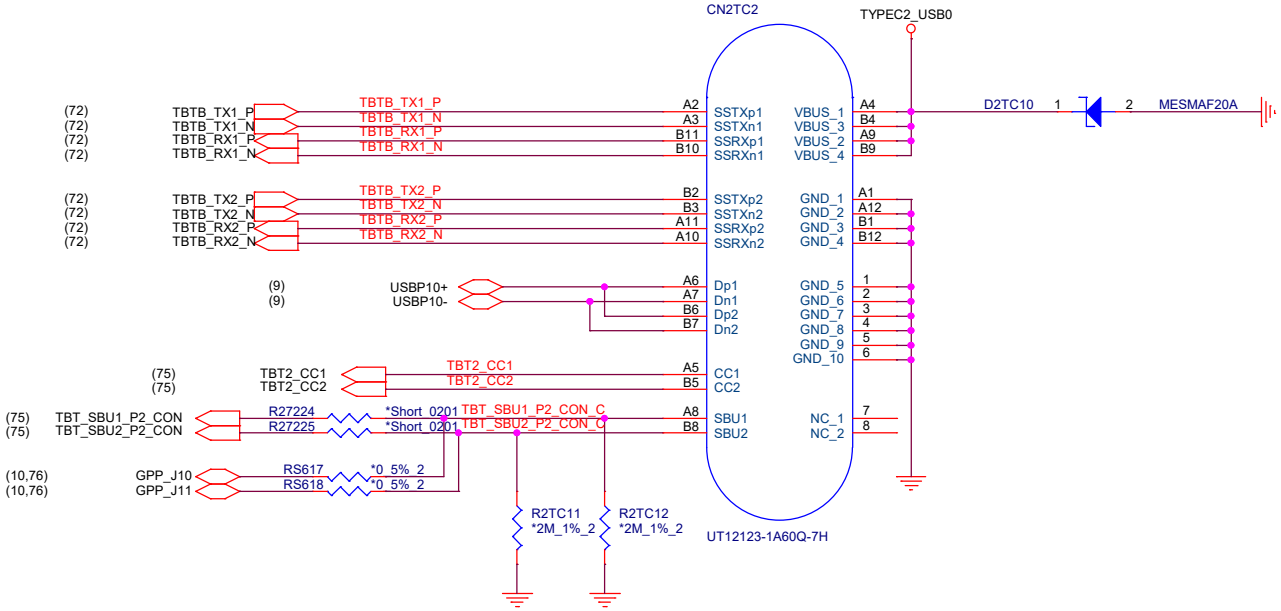
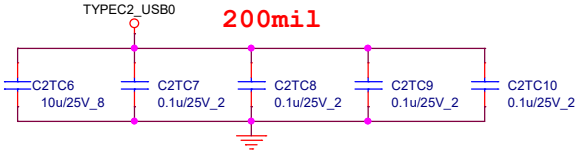
USB Type-C

200mil
5A 20V

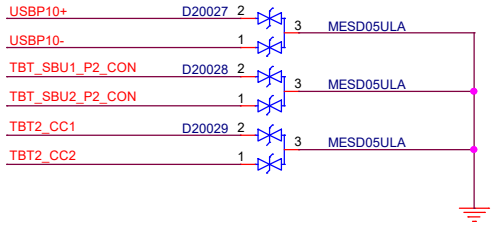


Power Capacitance

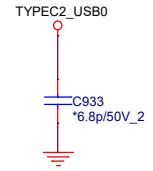
77



ESD



RF CAPS



Quanta Computer Inc.

PROJECT : Helios(ZGRC)

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Quanta Computer Inc.
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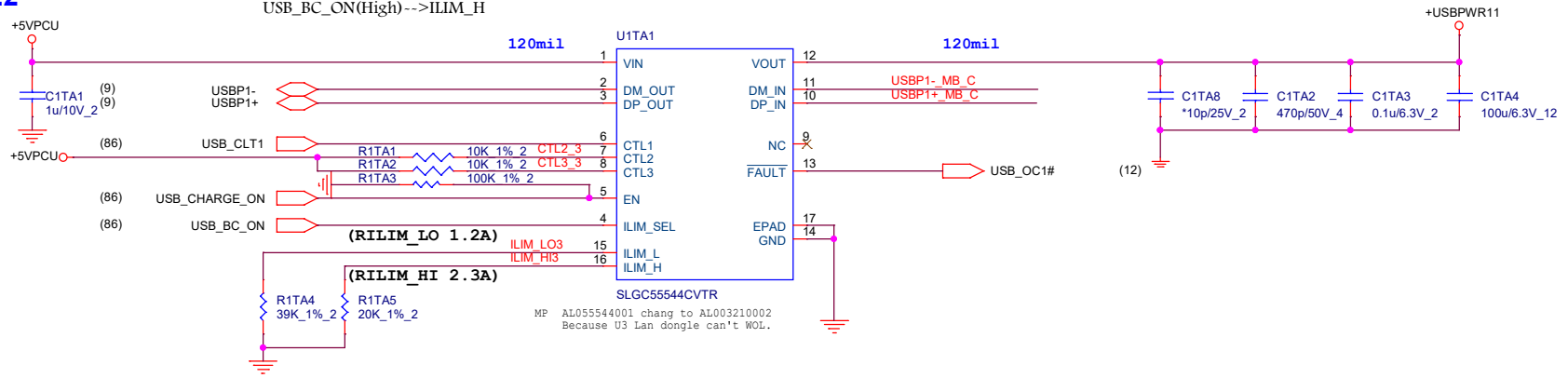
USB Charger (UBC)_BC 1.2

Part Number	Description
AL002544001	TPS2544RTER
AL055544001	SLGC55544CVTR

USB_BC_ON(Low)-->ILIM_L
USB_BC_ON(High)-->ILIM_H

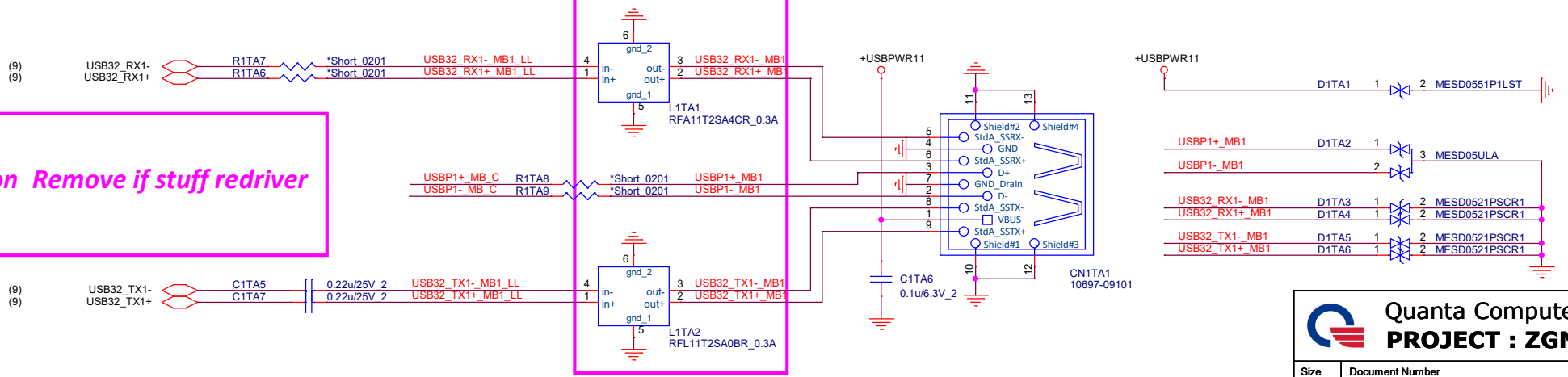


USB Power

TypeA#1

Option Check RF Level2 SPEC and remove, short directly

Option Remove if stuff redriver



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	TypeA1-CONN/BC1.2	A1A
Date: Wednesday, February 15, 2023	Sheet 79 of 149	

BLANK

Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	TypeA2-PS8811QFN36GTR2	A1A

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USB Charger (UBC)_BC 1.2

DVT

R2TA5 0_5%_2 USBON_A2#

R2TA6 *10K_1%_2 +3VPCU

(68,86) USBON# 2 3 1 Q6658 *2N7002K

USB Power

+5VPCU

C2TA1 1u/25V_4

U2TA1 G524B2T11U

5 IN OUT 1

GND 2

USBON_A2# 4 /EN /OC 3

(12) USB_OC2#

+USBPWR21

C2TA2 470p/50V_4

C2TA3 0.1u/50V_4

C2TA4 100u/6.3V_12

C1TA9 *10p/25V_2

Option

Check RF Level2 SPEC and remove, short directly

TypeA#2

RFA11T2SA4CR_0.3A L2TA1

(9) USB32_RX2- R2TA1 *Short_0201 USB32_RX2-_MB2_LL

(9) USB32_RX2+ R2TA2 *Short_0201 USB32_RX2+_MB2_LL

gnd_2 6, in- 4, in+ 1, out- 3, out+ 2, gnd_1 5

USB32_RX2-_MB2

USB32_RX2+_MB2

(9) USBP3+ R2TA3 *Short_0201 USBP3+_MB2

(9) USBP3- R2TA4 *Short_0201 USBP3-_MB2

RFL11T2SA0BR_0.3A L2TA2

(9) USB32_TX2- C2TA5 0.22u/25V_2 USB32_TX2-_MB2_LL

(9) USB32_TX2+ C2TA7 0.22u/25V_2 USB32_TX2+_MB2_LL

USB32_TX2-_MB2

USB32_TX2+_MB2

+USBPWR21

C2TA6 0.1u/6.3V_2

CN2TA1 10697-09101

Shield#2 Shield#4 StdA_SSRX- GND StdA_SSRX+ D+ GND_Drain D- StdA_SSTX- VBUS StdA_SSTX+ Shield#1 Shield#3

+USBPWR21

D2TA1 1 2 MESD0551P1LST

USBP3+_MB2 D2TA2 1 3 MESD05ULA

USBP3-_MB2 2

USB32_RX2-_MB2 D2TA3 1 2 MESD0521PSCR1

USB32_RX2+_MB2 D2TA4 1 2 MESD0521PSCR1

USB32_TX2-_MB2 D2TA5 1 2 MESD0521PSCR1

USB32_TX2+_MB2 D2TA6 1 2 MESD0521PSCR1

Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
B	TypeA2-CONN	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

Date:	Wednesday, February 15, 2023	Sheet	83	of	149

Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

Date:	Wednesday, February 15, 2023	Sheet	84	of	149

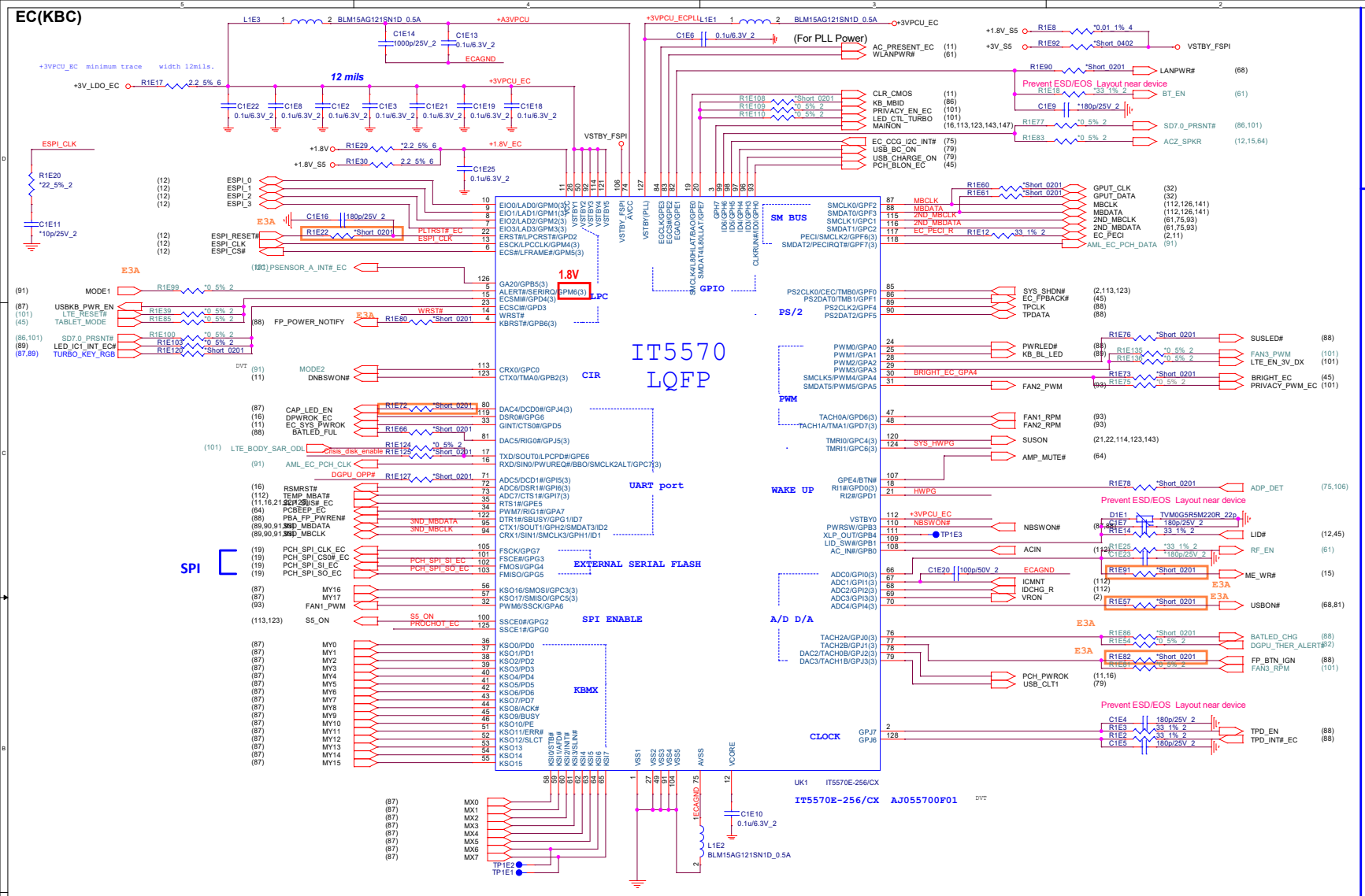
Quanta Computer Inc.

PROJECT : ZGN

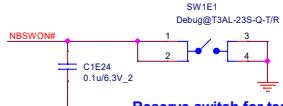
Size	Document Number	Rev
A	**LTE DB**	A1A

Date:	Wednesday, February 15, 2023	Sheet	85	of	149

EC(KBC)



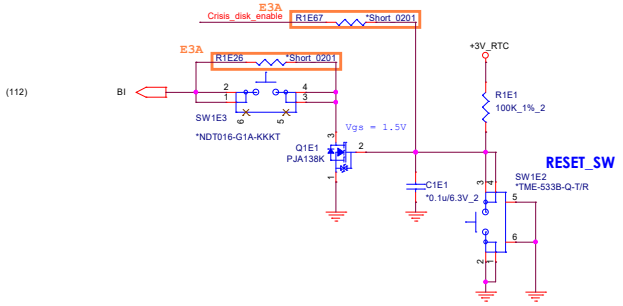
Reserve switch for test (MP remove)



Reserve switch for test (MP remove)

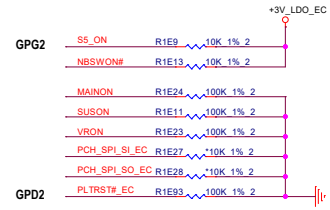
recommad use same as SW2 shortage problem

Reset SW (FSW)

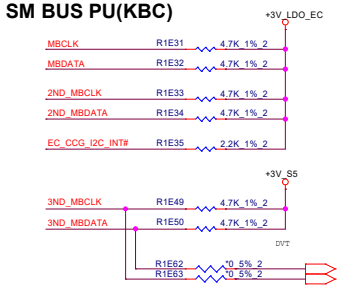


SMBUS	
SM Bus 0	Battery/GPU
SM Bus 1	Debug Card/ PD/ Thermal Sensor (Local:CPU;Remote Panel)
SM Bus 2	N/A
SM Bus 3	U3 Re-driver1/ U3 Re-drivr2/ LED Driver/ Ambient Light Sensor/ Thermal Sensor (Local:GPU;Remote DDR5)

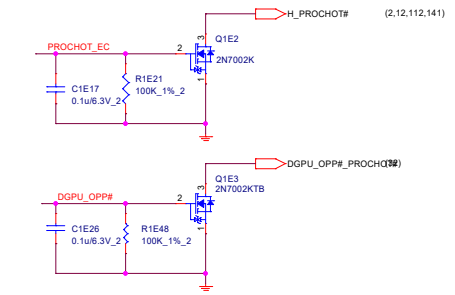
GPG2 / GPD2



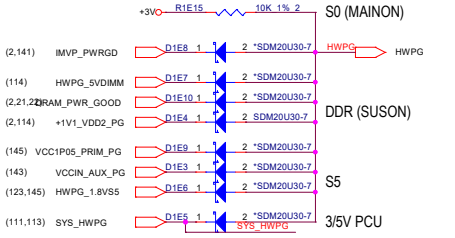
SM BUS PU(KBC)



PROHOT#



HWPG(KBC)



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	KBC IT8987	A1A
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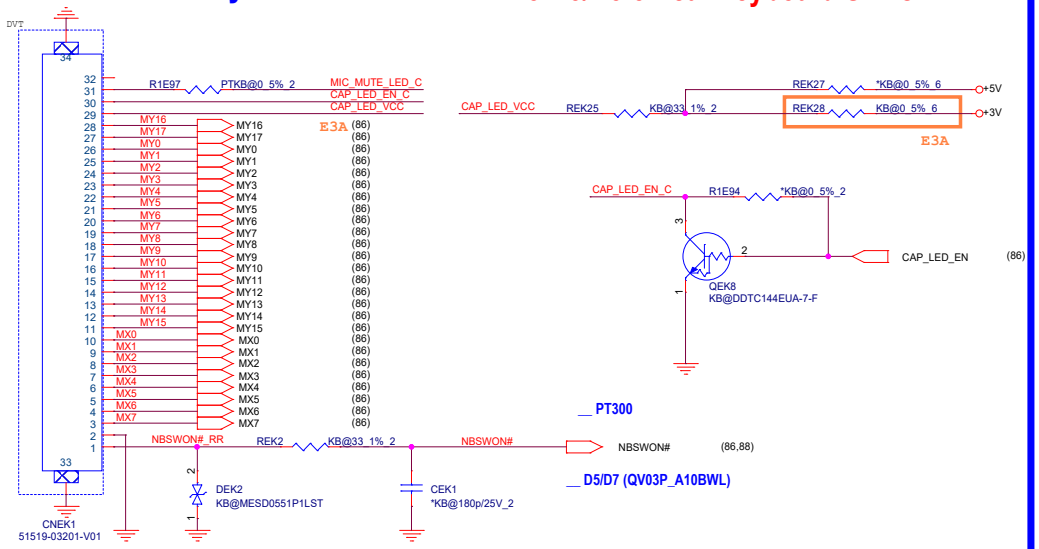
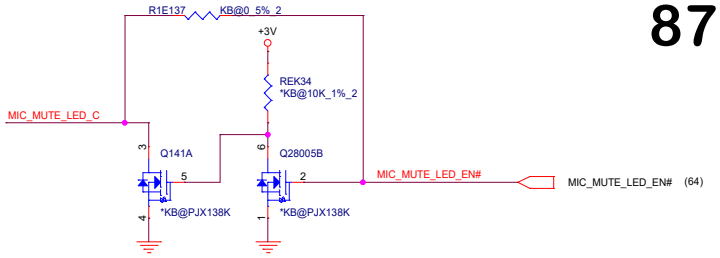
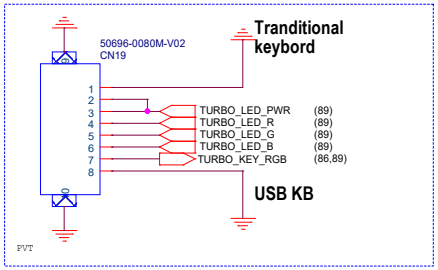
Tranditional keybord

No D5/D5 offical Keyboard SPEC



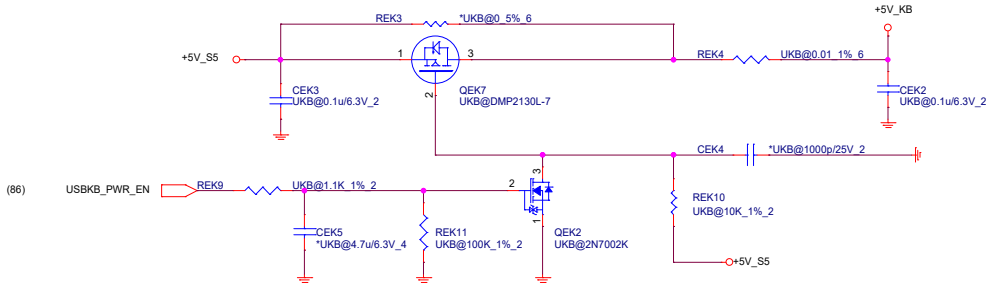


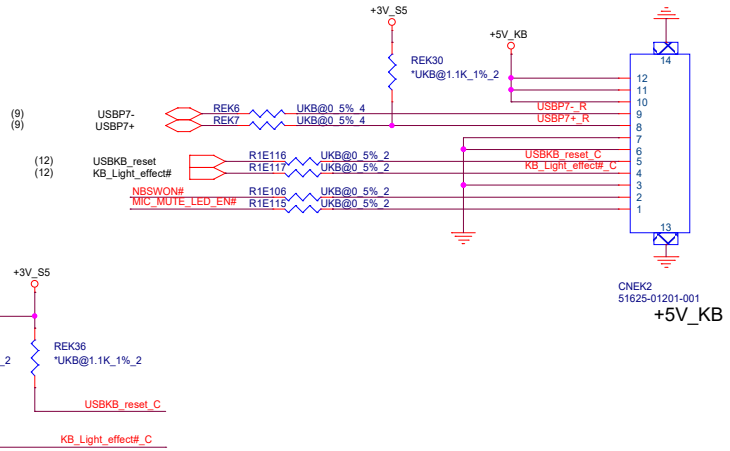
Turbo Key



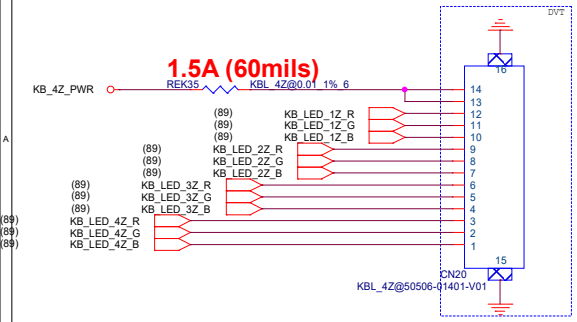
USB Keyboard

No USB Keyboard SPEC Follow XC90

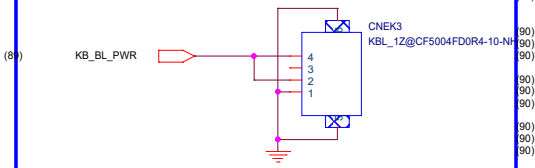




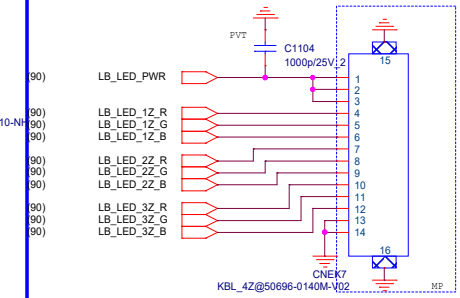
4-Zone RGB (PT300)



Single Color (D5/D7)



Rear Side Light Bar



Logo LED

Quanta Computer Inc.
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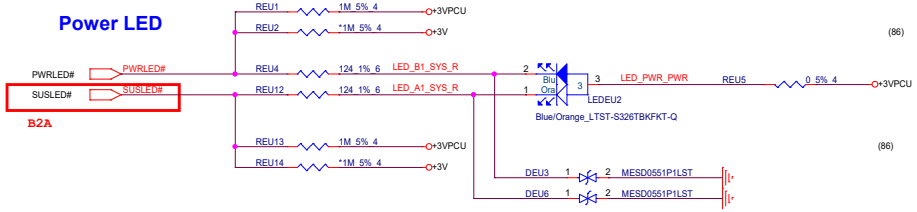
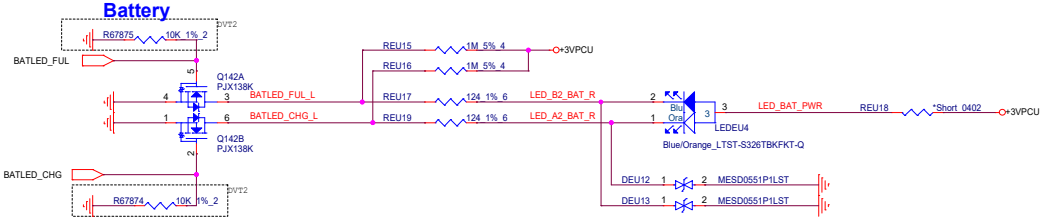
UIF

Power LED

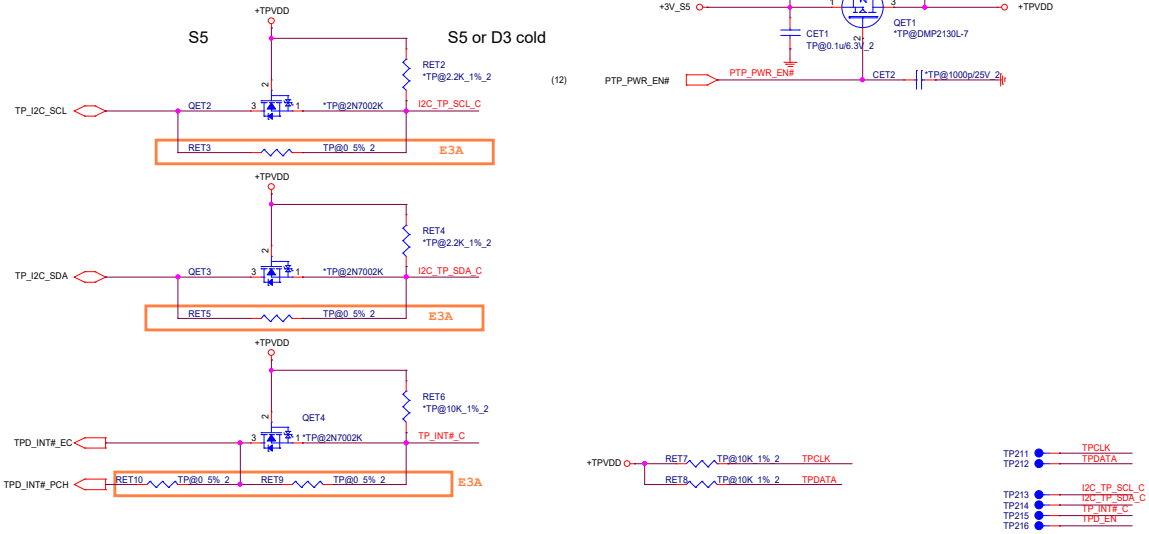


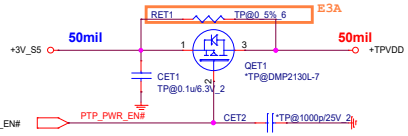
Battery



Touch Pad

Cannot wake once D3 Cold implement

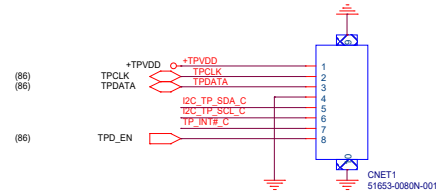




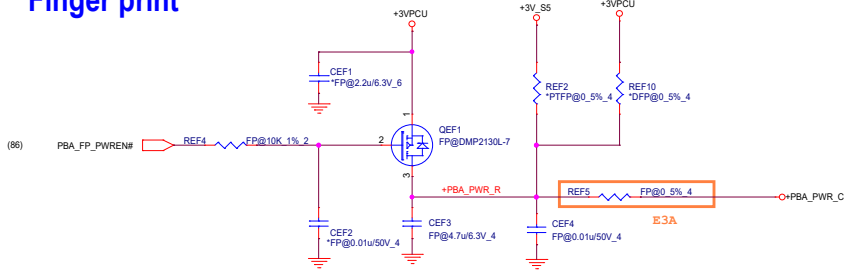
Haptic TouchPAD (D5/D7)

No Haptic Touch SPEC, Follow Beatles

TouchPAD (PT300)

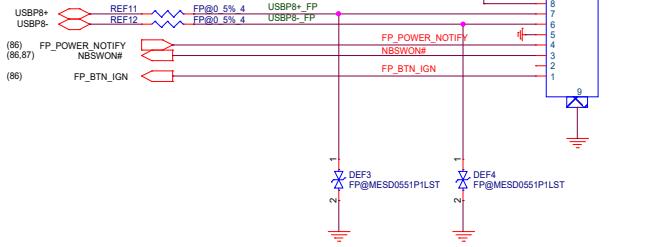


Finger print



Take care placement

FP (PT300) - Secure ID PAD



FP (D5/D7) - POA Like (FP on keyboard)

Should be (QF03P_A11BWL) + (FP)

No FP SPEC

FP_PWR_NTFY:System power status notify, to info FP keep data or not (Hi-power on; low-power off)

FP_BTN_IGN:Notify system to ignore PWR_BTN signal while Enroll/Verify Process
(While Hi notify EC to keep power while FP is working)

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C	UIF LED	A1A
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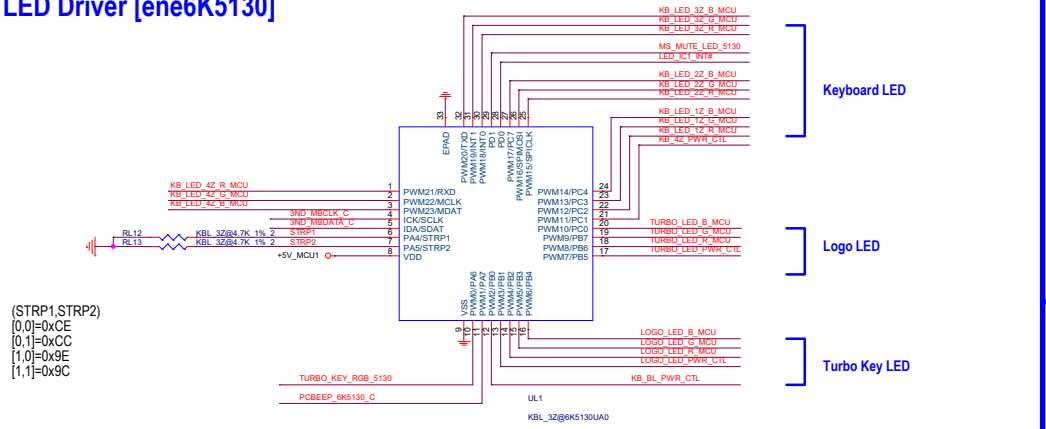
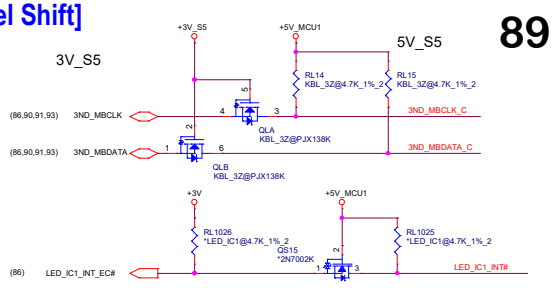
LED Driver [ene6K5130]



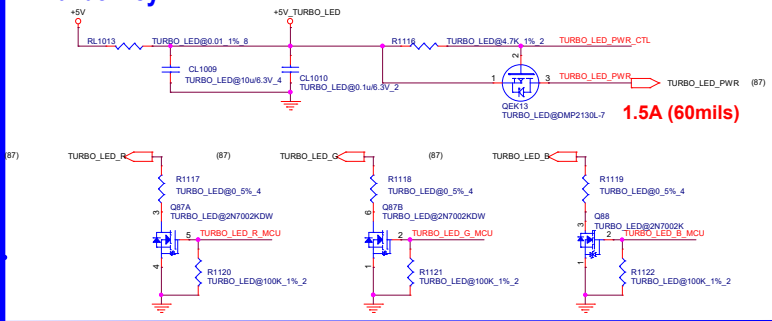
(STRP1,STRP2)
[0,0]=0xCE
[0,1]=0xCC
[1,0]=0x9E
[1,1]=0x9C

PC BEEP

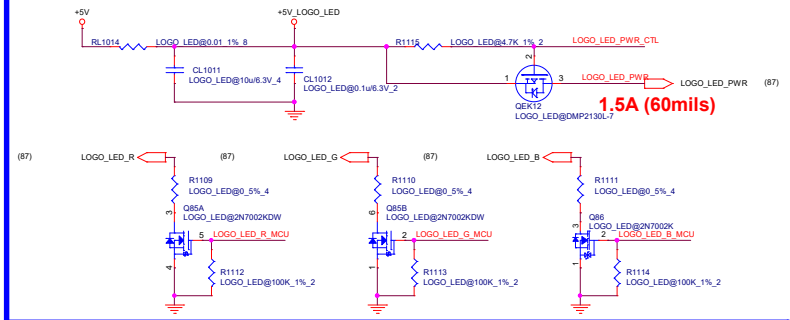
SMBUs [Level Shift]



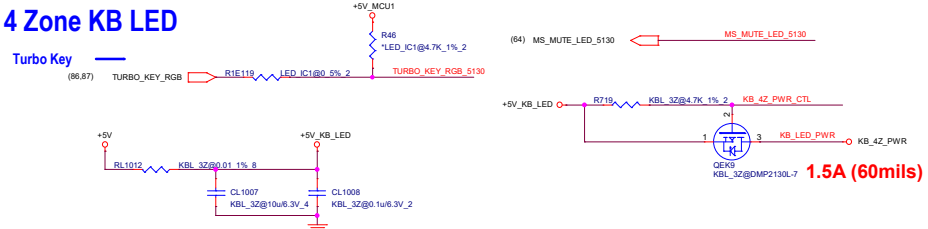
Turbo Key LED

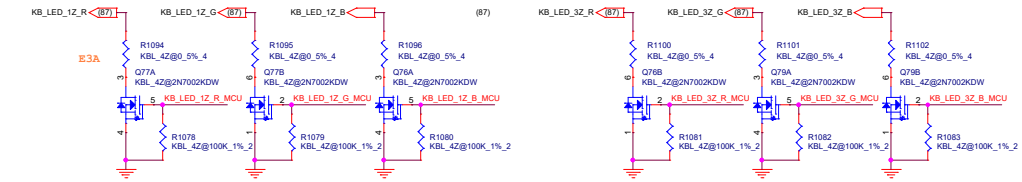


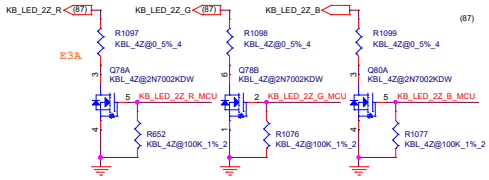
Logo LED

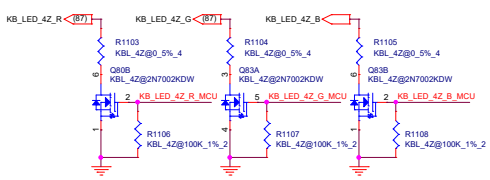


4 Zone KB LED

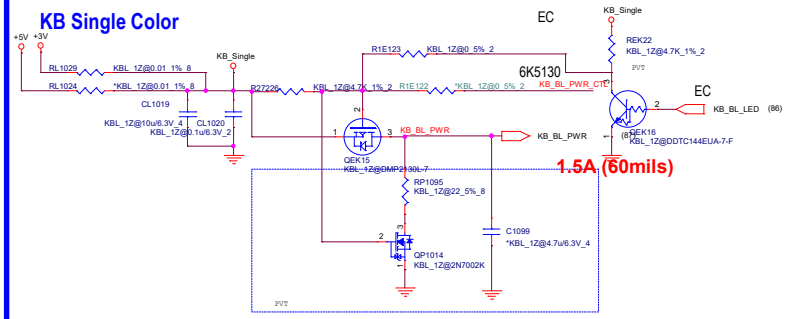








KB Single Color



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Size	Document Number	Rev
Custom	I/O DB (Audio/LAN/U3/LED)	A1A
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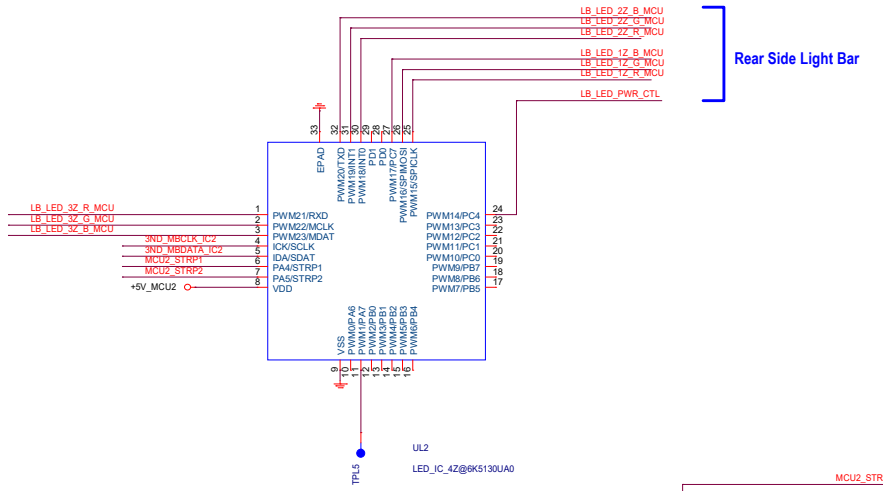
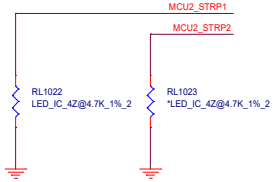
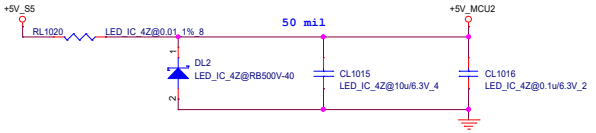
LED Driver [ene6K5130]

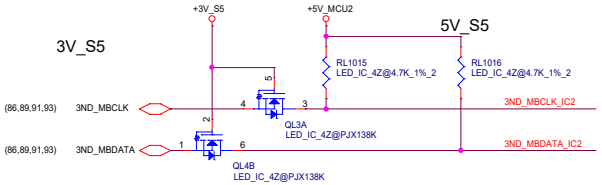


(STRP1,STRP2)
[0,0]=0xCE
[0,1]=0xCC
[1,0]=0x9E
[1,1]=0x9C

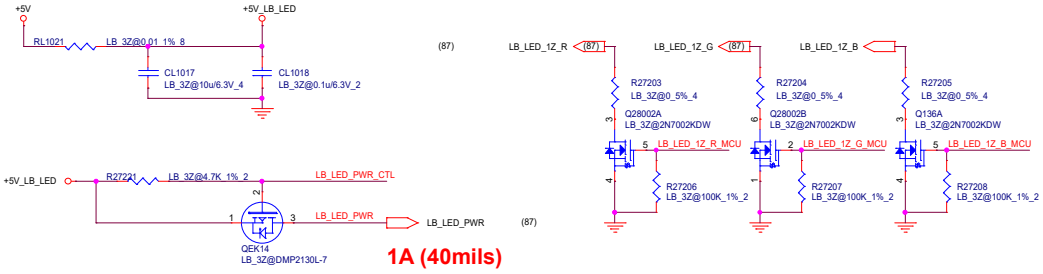


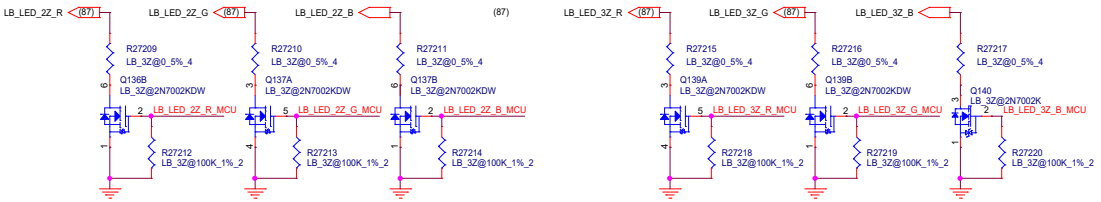


SMBUs [Level Shift]



Rear Side Light Bar





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C	I/O DB (Audio/LAN/U3/LED)	A1A
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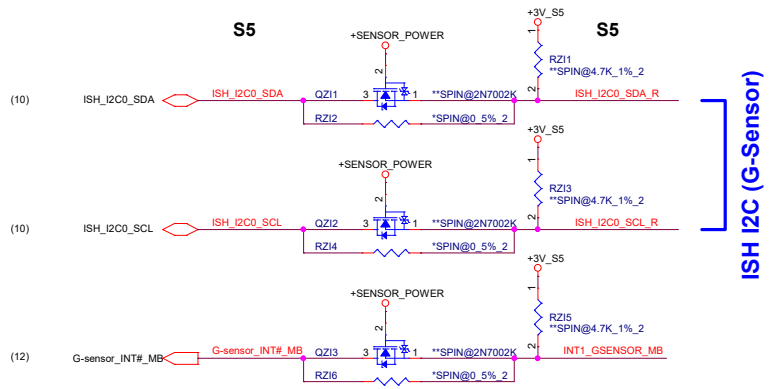
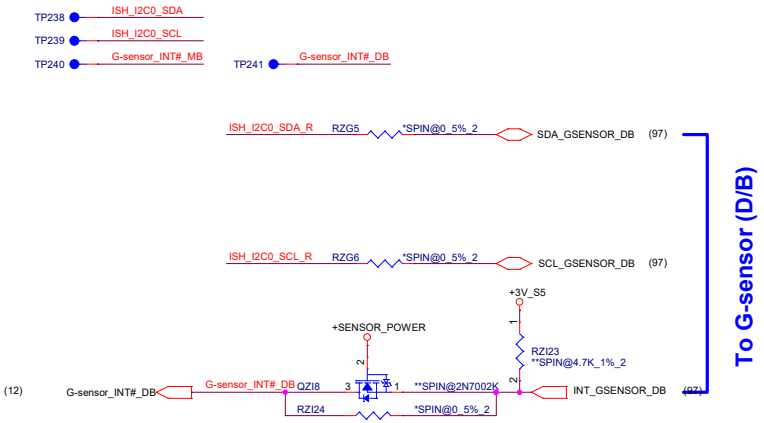
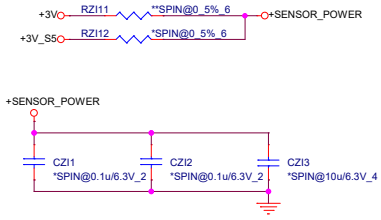
Sensor (D5/D7)

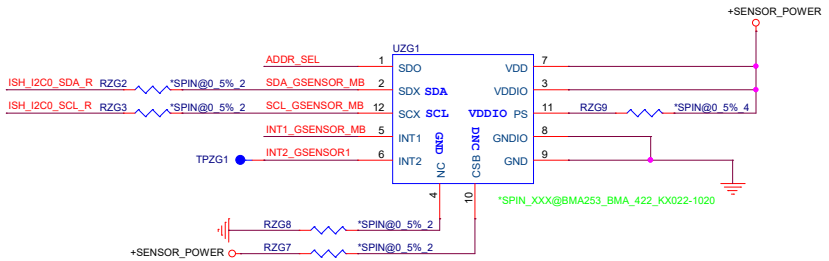


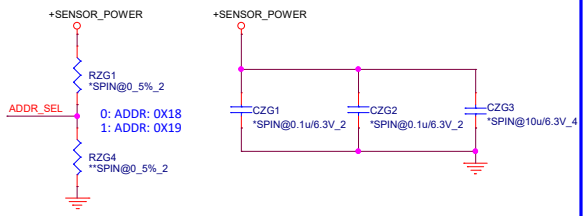


Power



G-sensor (M/B) E-Zel SKU remove on board G-sensor (Need change to BMI260 14 pin)





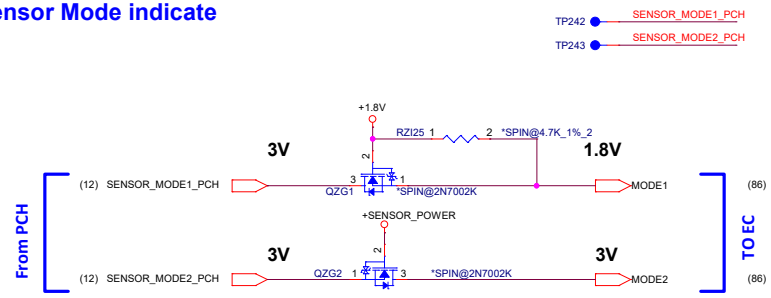
BMA253 AL000253A00
SDO I2C Address:
PU:0X19 (M/B)
PD:0X18 (D/B)

KX022-1020 AL001020A00
SDO I2C Address:
PU:0x1F (M/B)
PD:0x1E (D/B)

BMA422 ----------

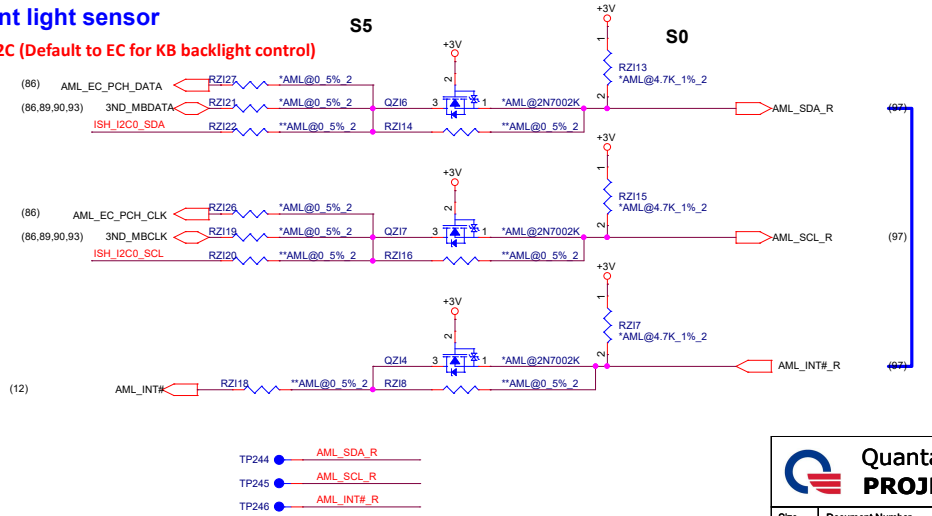
TOF Sensor (For P6 only)

G-sensor Mode indicate



Ambient light sensor

AML I2C (Default to EC for KB backlight control)



TP244 AML_SDA_R
TP245 AML_SCL_R
TP246 AML_INT#_R

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A	**LTE DB**	A1A

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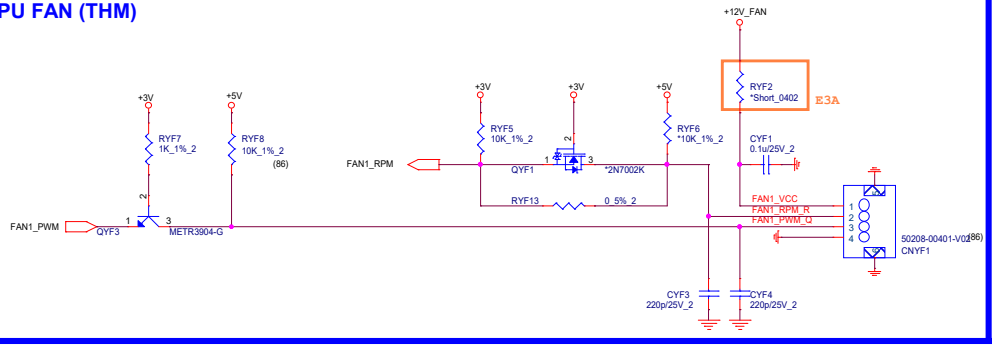
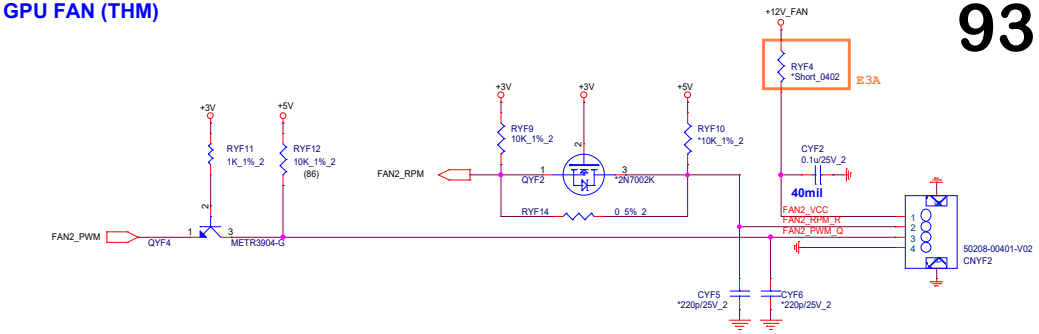
CPU FAN (THM)

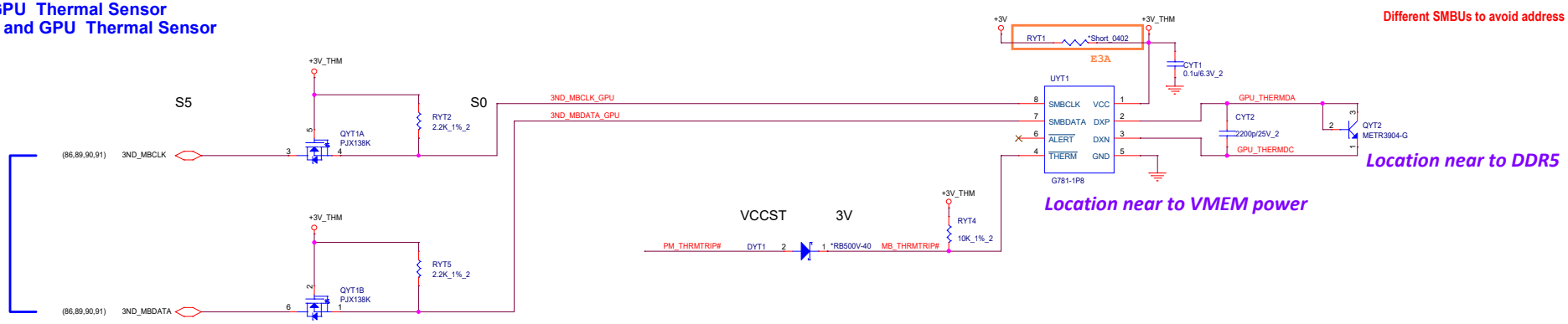


GPU FAN (THM)



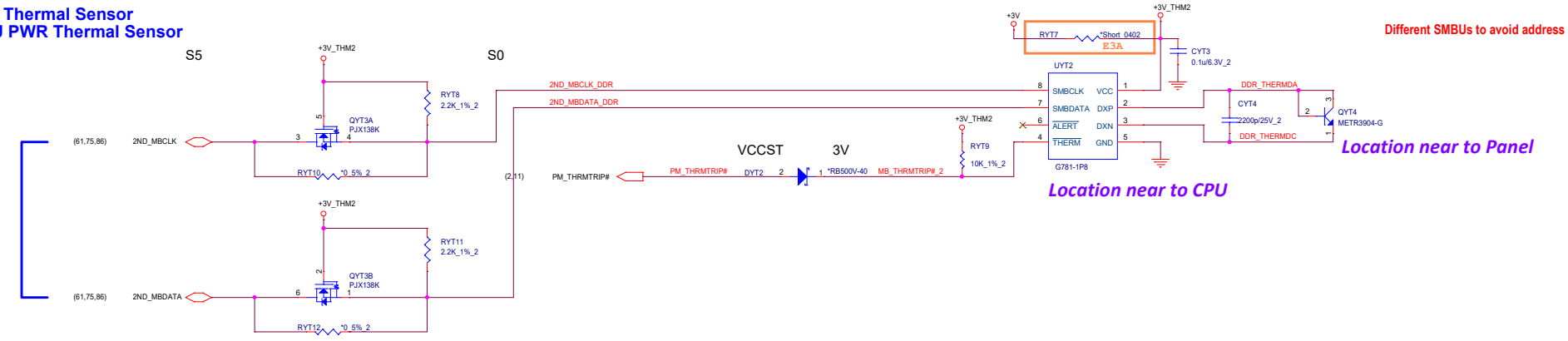
Vram and GPU Thermal Sensor
Local Vram and GPU Thermal Sensor

Different SMBUs to avoid address conflict



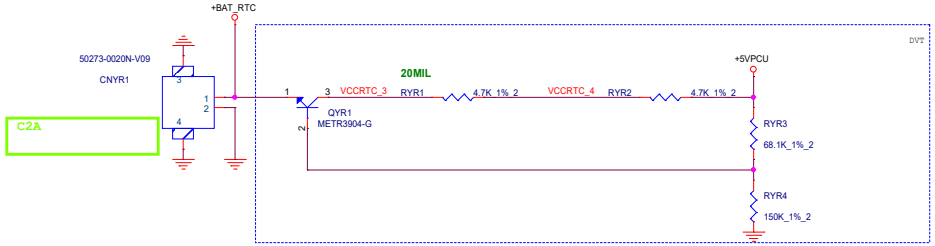
CPU PWR Thermal Sensor
Local CPU PWR Thermal Sensor

Different SMBUs to avoid address conflict



Coin Battery Charging

PT300 non chargeable type



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
C	FAN/Thermal Sensor	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

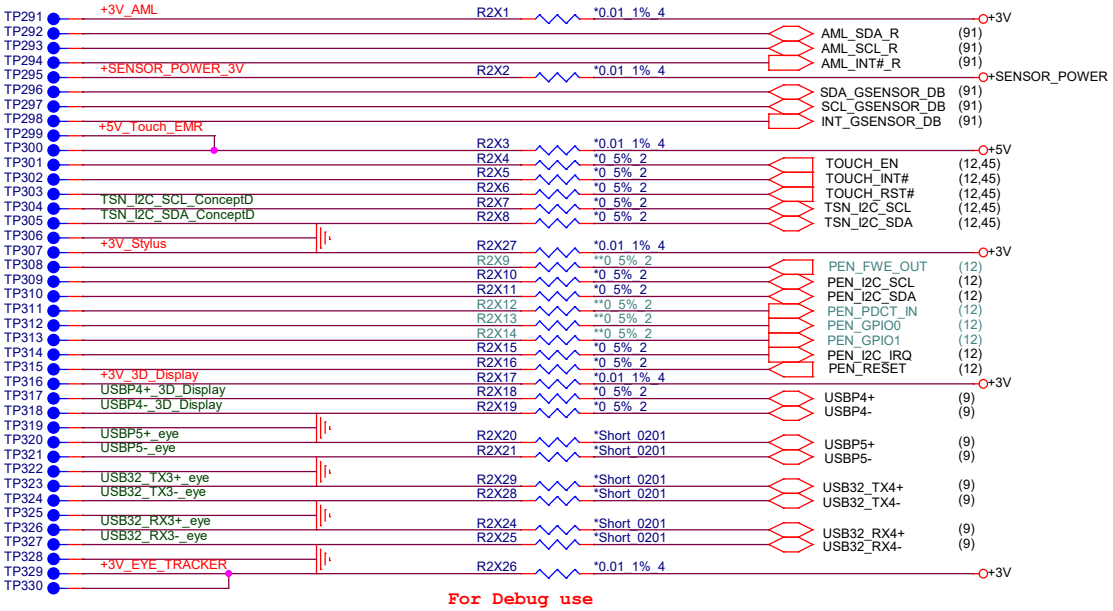
PROJECT : ZGN

Size	Document Number	Rev
A	**DB1 :SD Card+UIF**	A1A

Date:	Sheet	of
Wednesday, February 15, 2023	96	149

Reserve for 3D Display

確認3D Display是不是只有留一組USB就好?



For Debug use

Ambient light sensor

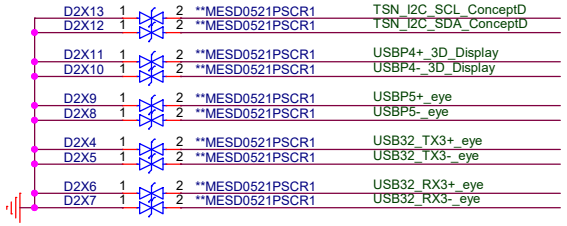
GSENSOR

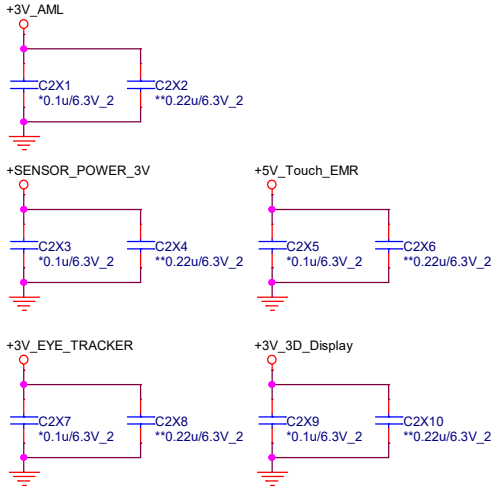
Touch-EMR (I2C)

STYLUS-EMR

3D Display

EYE tracker





Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	LTE DB	A1A
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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

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A	**LTE DB**	A1A

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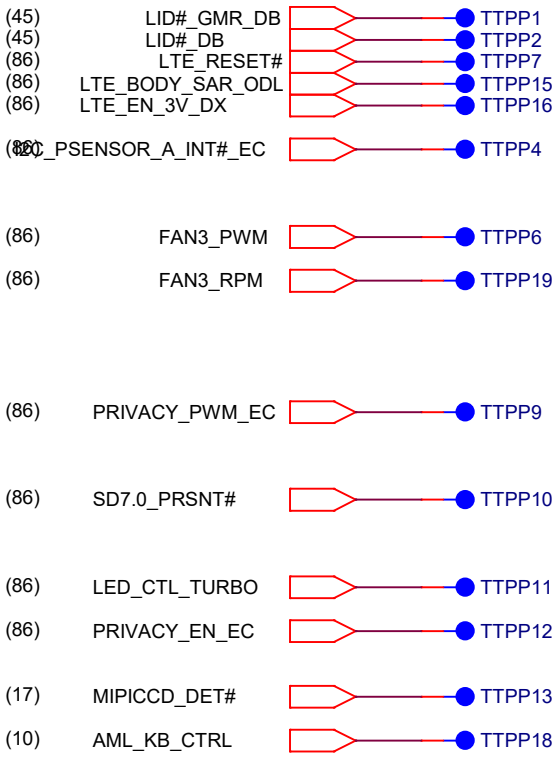
EMC CAPS

PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



Quanta Computer Inc.

PROJECT : ZGN

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A	**LTE DB**	A1A
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Quanta Computer Inc.

PROJECT : ZGN

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A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

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A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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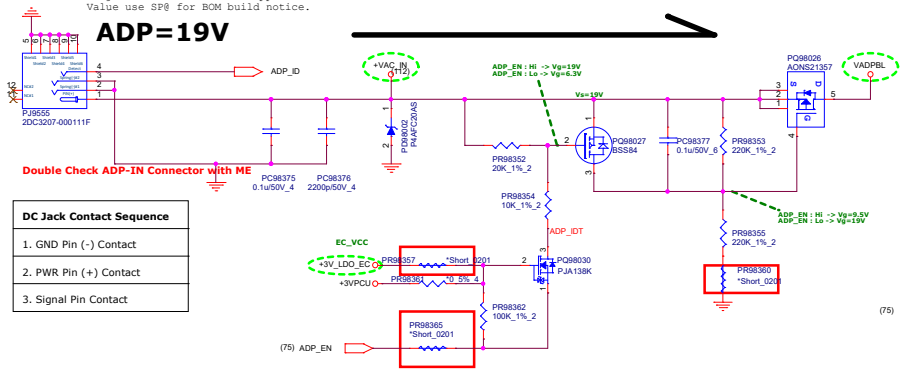
Option for serch.
Project need to check PM support ADP & show into circuit.
Value use SP@ for BOM build notice.

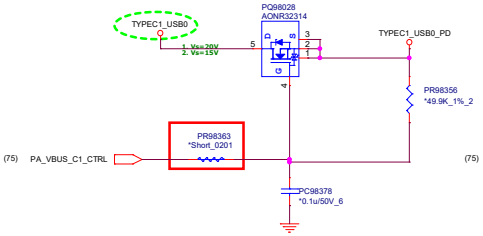
ADP=19V



DC Jack Contact Sequence
1. GND Pin (-) Contact
2. PWR Pin (+) Contact
3. Signal Pin Contact

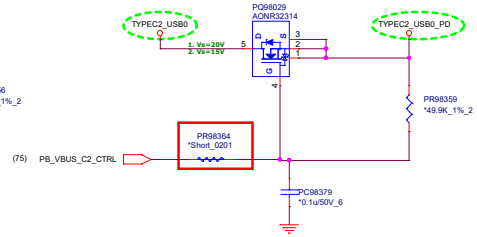
ADP_EN	ADP Switch PQ98026
Hi	ON
Low	OFF

Type C 1 PD=20V



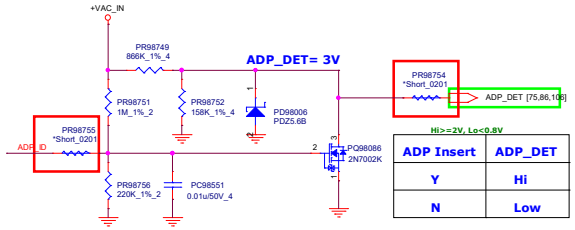
PA_VBUS_C_CTRL	Type C Switch PQ98028
High-Z	ON
Low	OFF

Type C 2 PD=20V



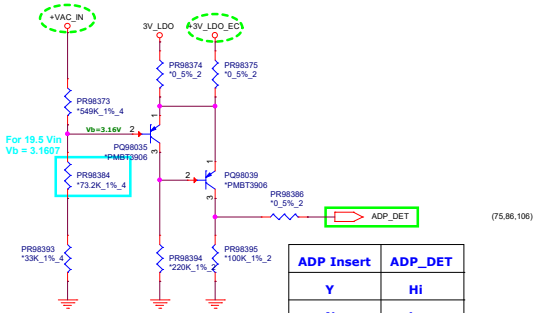
PB_VBUS_C_CTRL	Type C Switch PQ98029
High-Z	ON
Low	OFF

C1



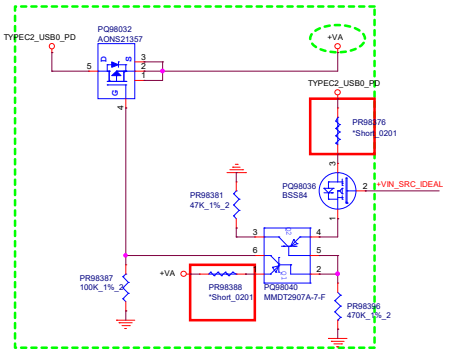
Hi>=2V, Lo<0.8V

ADP Insert	ADP_DET
Y	Hi
N	Low

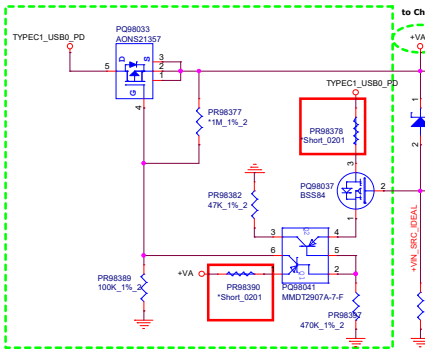


ADP Insert	ADP_DET
Y	Hi
N	Low

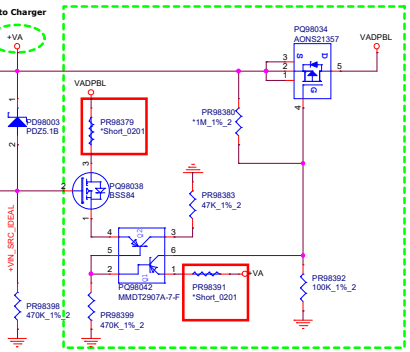
Ideal Diode for Type-C2 Port



Ideal Diode for Type-C1 Port



Ideal Diode for Adapter



Vi compare	Vo (=+VA)
TYPEC_USB0_PD > VADPBL	TYPEC_USB0_PD
TYPEC_USB0_PD < VADPBL	VADPBL

Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	TYPE-C Input	A1A

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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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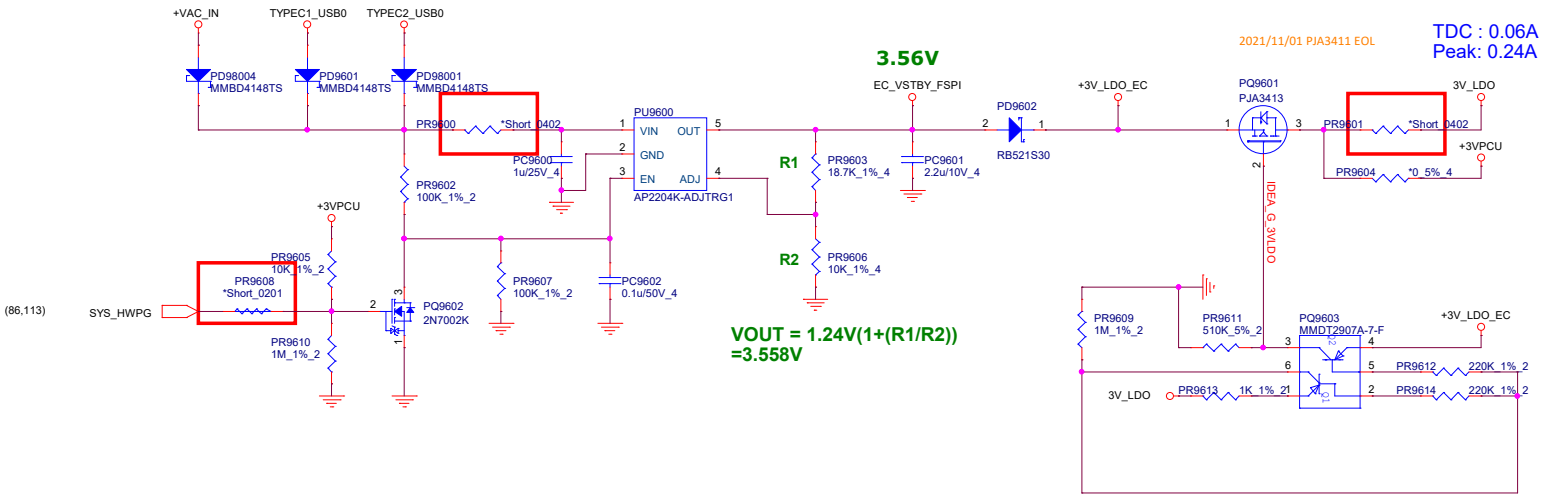
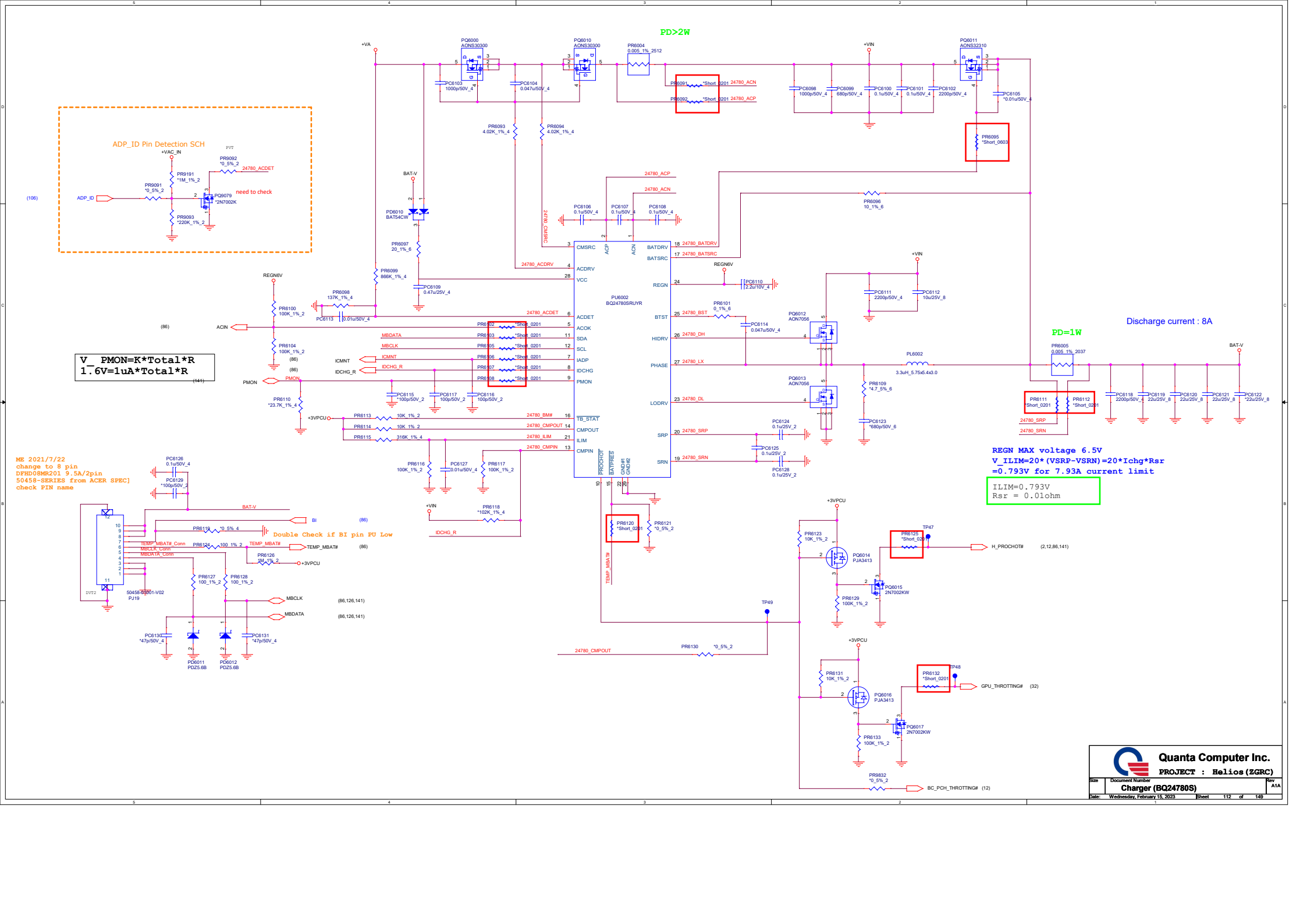
Dead Battery

+VAC_IN (106,112)
TYPEC1_USB0 (75,76,106)
3V_LDO (16,106,113)
+3V_LDO_EC (86,106,113)
+3VPCU (11,13,45,68,75,81,88,106,112,113,123)
+5VPCU (68,75,79,81,93,113,145)

For EC



Quanta Computer Inc.			
PROJECT : Helios(ZGRC)			
Size	Document Number: Dead Battery		Rev: A1A
Date: Wednesday, February 15, 2023		Sheet 111 of 149	


PD>2W
ADP_ID Pin Detection SCH
PVT
+VAC_IN
PR9092 *0_5%_2
24780_ACDET
PR9191 *1M_1%_2
PR9091 *0_5%_2
PQ9079 2N7002K
need to check
ADP_ID
(106)
PR9093 *220K_1%_2
V_ PMON=K*Total*R
1.6V=1uA*Total*R
(141)
+VA
PQ6000 AONS30300
PQ6010 AONS30300
PR6004 0.005_1%_2512
PR6091 *Short_0201 24780_ACN
PR6092 *Short_0201 24780_ACP
PC6103 1000p/50V_4
PC6104 0.047u/50V_4
PR6093 4.02K_1%_4
PR6094 4.02K_1%_4
+VIN
PC6098 1000p/50V_4
PC6099 680p/50V_4
PC6100 0.1u/50V_4
PC6101 0.1u/50V_4
PC6102 2200p/50V_4
PQ6011 AONS32310
PC6105 *0.01u/50V_4
PR6095 *Short_0603
PR6096 10_1%_6
BAT-V
PD6010 BAT54CW
PR6097 20_1%_6
PR6099 866K_1%_4
PC6106 0.1u/50V_4
PC6107 0.1u/50V_4
PC6108 0.1u/50V_4
24780_ACP
24780_ACN
24780_CMSRC
24780_ACDRV
REGN6V
PR6098 137K_1%_4
PC6109 0.47u/25V_4
PC6113 0.01u/50V_4
PR6100 100K_1%_2
(86)
ACIN
PR6104 100K_1%_2
(86)
PMON
PR6110 *23.7K_1%_4
+3VPCU
PR6102 *Short_0201
PR6103 *Short_0201
PR6105 *Short_0201
PR6106 *Short_0201
PR6107 *Short_0201
PR6108 *Short_0201
MBDATA
MBCLK
ICMNT
IDCHG_R
PC6115 100p/50V_2
PC6117 100p/50V_2
PC6116 100p/50V_2
PU6002 BQ24780SRUYR
CMSRC
ACDRV
VCC
ACDET
ACOK
SDA
SCL
IADP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
PROCHOT
BATPRES
GND#1
GND#2
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LODRV
SRP
SRN
24780_BATDRV
24780_BATSRC
24780_BST
24780_DH
24780_LX
24780_DL
24780_SRP
24780_SRN
24780_BM#
24780_CMPOUT
24780_ILIM
24780_CMPIN
PC6110 2.2u/10V_4
PR6101 0.1%_6
PC6114 0.047u/50V_4
PQ6012 AON7056
PQ6013 AON7056
PL6002 3.3uH_5.75x5.4x3.0
PR6109 *4.7_5%_6
PC6123 *680p/50V_6
PC6124 0.1u/25V_2
PC6125 0.1u/25V_2
PC6128 0.1u/25V_2
PC6111 2200p/50V_4
PC6112 10u/25V_8
Discharge current : 8A
PD=1W
PR6005 0.005_1%_2037
BAT-V
PR6111 *Short_0201
PR6112 *Short_0201
PC6118 2200p/50V_4
PC6119 22u/25V_8
PC6120 22u/25V_8
PC6121 22u/25V_8
PC6122 *22u/25V_8
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 7.93A current limit
ILIM=0.793V
Rsr = 0.01ohm
ME 2021/7/22
change to 8 pin
DFHD08MR201 9.5A/2pin
50458-SERIES from ACER SPEC]
check PIN name
PC6126 0.1u/50V_4
PC6129 *100p/50V_2
BAT-V
BI
(86)
PR6119 *0_5%_4
Double Check if BI pin PU Low
PR6124 100_1%_2
TEMP_MBAT#
TEMP_MBAT#_Conn
MBCLK_Conn
MBDATA_Conn
PR6126 1M_1%_2
+3VPCU
PR6127 100_1%_2
PR6128 100_1%_2
50458-0201-V02
PJ19
MBCLK
MBDATA
(86,126,141)
PC6130 *47p/50V_4
PC6131 *47p/50V_4
PD6011 PDZ5.6B
PD6012 PDZ5.6B
PR6116 100K_1%_2
PC6127 0.01u/50V_4
PR6117 100K_1%_2
PR6118 *102K_1%_4
IDCHG_R
PR6120 *Short_0201
PR6121 *0_5%_2
TEMP_MBAT#
24780_CMPOUT
PR6130 *0_5%_2
TP49
PR6123 10K_1%_2
PQ6014 PJA3413
PR6125 *Short_0201
TP47
H_PROCHOT#
(2,12,86,141)
PQ6015 2N7002KW
PR6129 100K_1%_2
PR6131 10K_1%_2
PQ6016 PJA3413
PR6132 *Short_0201
TP48
GPU_THROTTING#
(32)
PQ6017 2N7002KW
PR6133 100K_1%_2
PR9832 *0_5%_2
BC_PCH_THROTTING#
(12)
Quanta Computer Inc.
PROJECT : Helios(ZGRC)
Size
Document Number
Charger (BQ24780S)
Rev
A1A
Date: Wednesday, February 15, 2023
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+VIN (16,45,112,114,123,126,127,131,142,143,145,146,147)
+5VPCU (68,75,79,81,93,145)
+3VPCU (11,13,45,68,75,81,88,106,111,112,123)
SYS_SHDN# (2,86,123)
3V_LDO (16,106,111)

+5VPCU
5 Volt +/- 5%
TDC : 11.8A
OCP : 16A
Width : 480mil

+3VPCU
3.3 Volt +/- 5%
TDC : 9A
PEAK : 12A
OCP : 17.4A
Width : 360mil

PU3005 RT6575AGQW

Rds(on)=4.7m ohm

Rds(on)=4.7m ohm

OCP:18.5A (For BAT 4S1P)
L(ripple current)
=(12-5)*5/(2.2u*0.3M*12)
=4.419A
Iocp=18.5-(4.419/2)=16.29A
Vth=(16.29A*4.7mOhm)+1mV=76.56mV
R(Ilim)=(76.56mV*8)/10uA
~60.45K

OCP:17.4A (For BAT 4S1P)
L(ripple current)
=(12-3.3)*3.3/(1.5u*0.355M*12)
~4.493A
Iocp=17.4-(4.493/2)=15.15352A
Vth=(15.15352A*4.7mOhm)+1mV=71.222mV
R(Ilim)=(71.222mV*8)/10uA
=56.177K

Power Auto Recovery
(Stuff on Dead Battery page)

+5V_S5 (87,89,90,114,126,127,130,131,141,142,143,145)
+5V (48,64,87,89,90,93,97,123)
+3V_S5 (2,10,13,15,16,19,20,45,61,68,73,75,86,87,88,89,90,91,114,123,126,129,131,141,143,145,147)
+3V (2,9,10,11,12,17,21,32,44,45,47,53,55,61,64,68,72,73,86,87,88,89,91,93,97,123,130,131,141,143)

TDC : 5.63A
PEAK : 7.5A
Width : 100mil

TDC : 1.68A
PEAK : 2.24A
Width : 220mil

PU3006 JW7107SDFNC#TRPBF

TDC : 4.68A
PEAK : 6.24A
Width : 140mil

TDC : 4.5A
PEAK : 6A
Width : 240mil

PU3007 JW7107SDFNC#TRPBF

PQ74 AOSS32334C

TDC : 0.05A
PEAK : 0.1A
Width : 20mil

PQ98079 DDTC144EUA-7-F

PQ98080 2N7002K
PQ98081 2N7002K
PQ98074 2N7002K
PQ98082 *2N7002K
PQ98083 2N7002K

Quanta Computer Inc.
PROJECT : Helios(ZGRC)
Size | Document Number: SYSTEM (SY8371BTMC/SY8370C1TMC) | Rev: A1A
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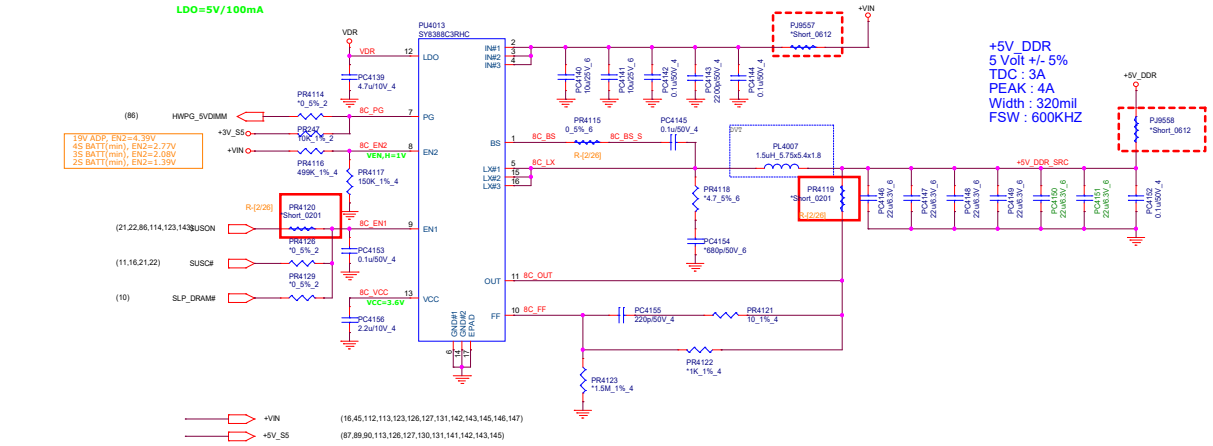

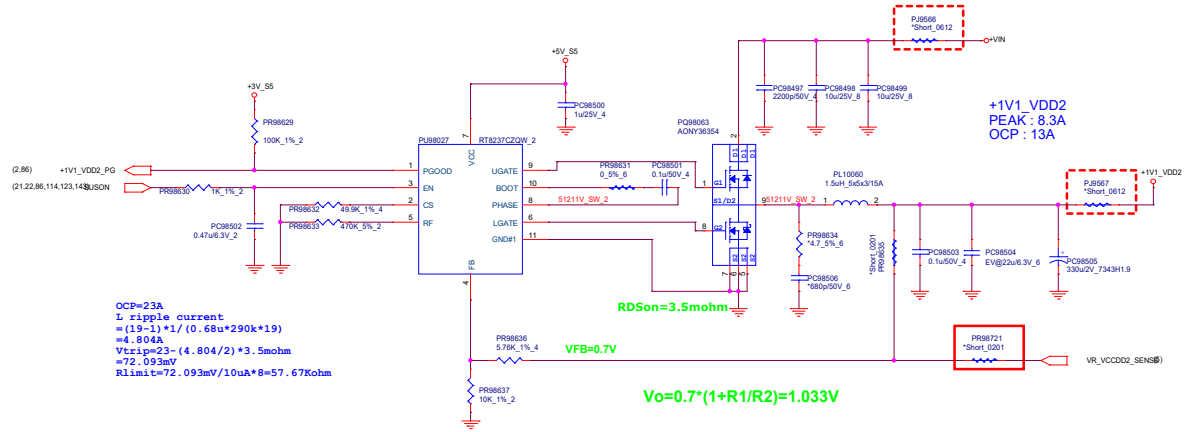

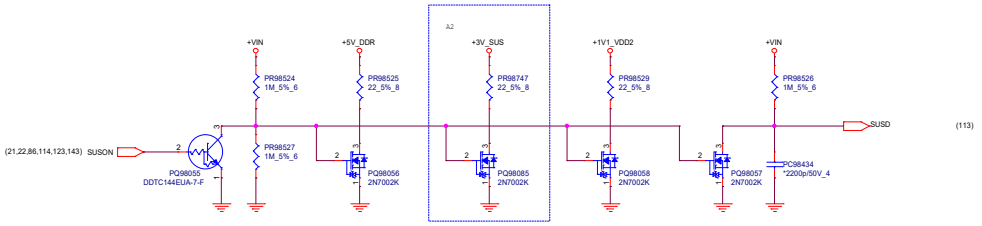

Quanta Computer Inc.			
PROJECT : Helios(ZGRC)			
Size	Document Number		Rev
	+5V_DDR		A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
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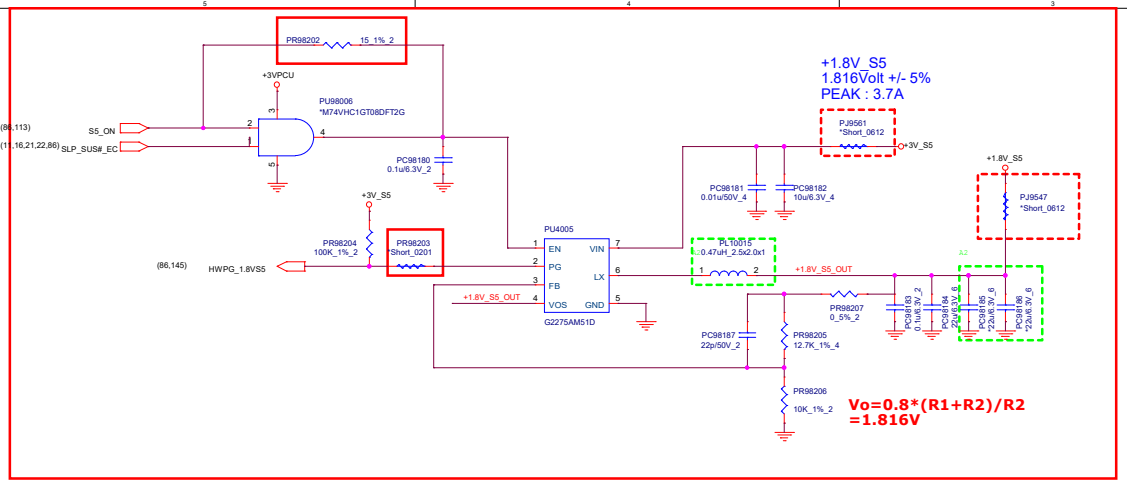
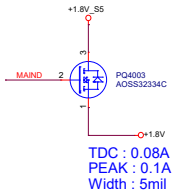
Quanta Computer Inc.
PROJECT : ZGN

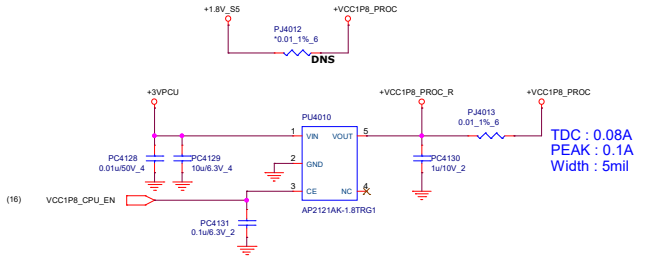
Size	Document Number	Rev
Custom	GPIO	A1A
Date: Wednesday, February 15, 2023	Sheet 120 of 149	

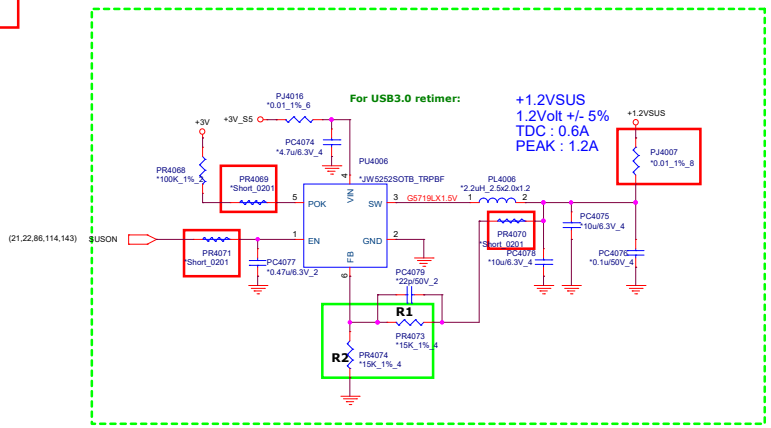
Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	GPIO	A1A
Date: Wednesday, February 15, 2023	Sheet 121 of 149	



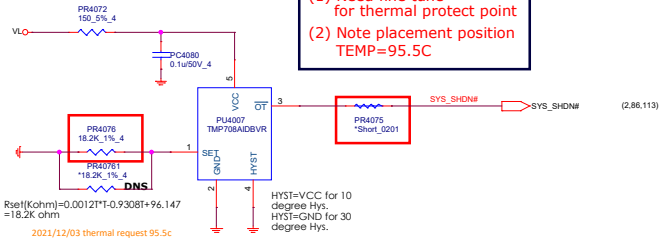


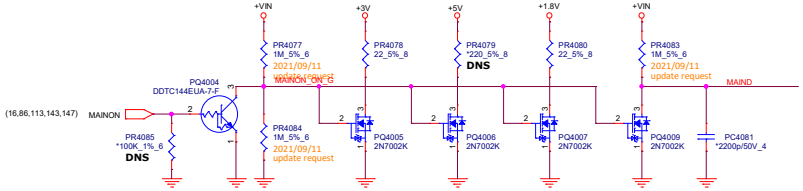




Thermal protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=95.5C





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PROJECT : Helios(ZGRC)

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	+VNN_EXT & +1.05V_EXT (SYV659LQWC)	A1A

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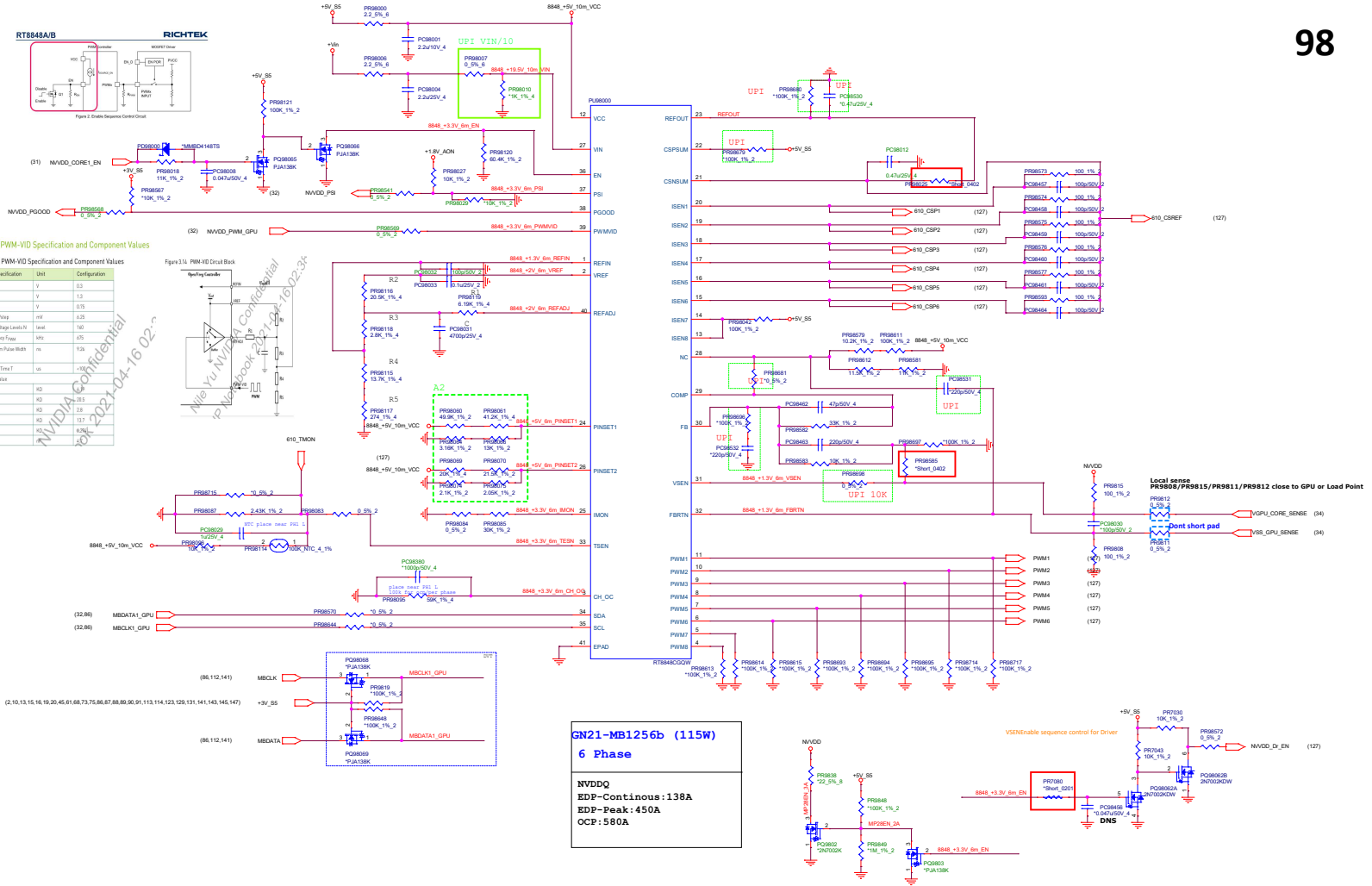
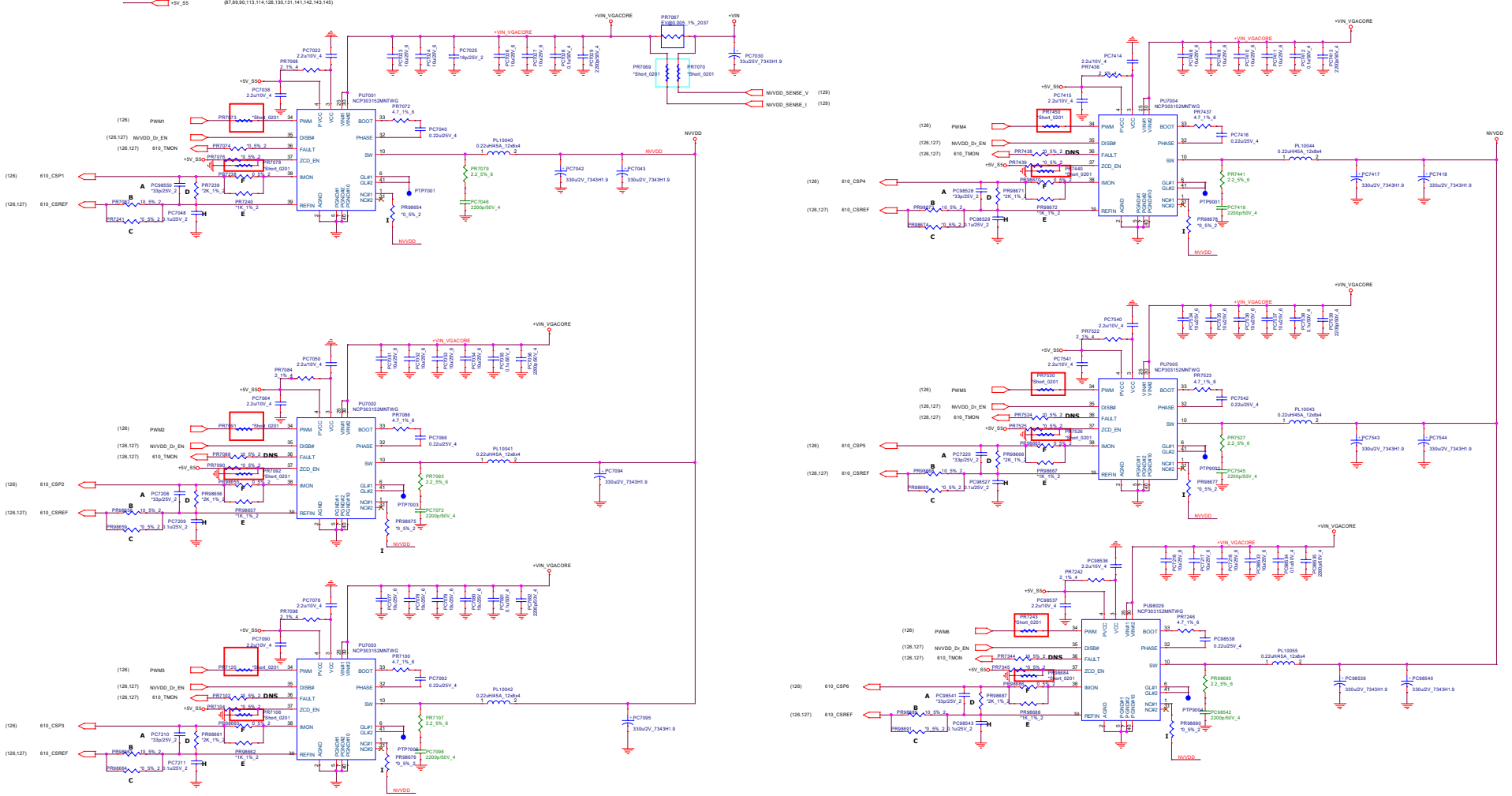


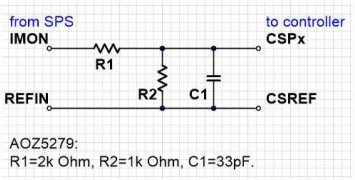
3.4.2.2 PWM-VID Specification and Component Values

Table 3.9 PWM-VID Specification and Component Values

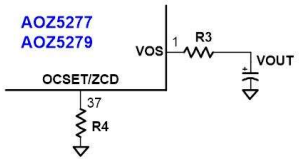
PWM-VID Specification	Unit	Configuration
Kmin	V	0.3
Kmax	V	1.3
Vboot	V	0.75
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OWS}	ns	926
VID Transient Time T	us	~100
Component Value		
R1 (1%)	KΩ	6.8
R2 (1%)	KΩ	28.5
R3 (1%)	KΩ	2.8
R4 (1%)	KΩ	13.7
R5 (1%)	KΩ	6.04
C	nF	4700



	A	B	C	D	E	F		H	I
NCP303152MNTWG	NC	STUFF	NC	NC	NC	STUFF		STUFF	NC
AOZ5279	STUFF	NC	STUFF	STUFF	STUFF	NC		NC	STUFF



AOZ5279:
R1=2k Ohm, R2=1k Ohm, C1=33pF.



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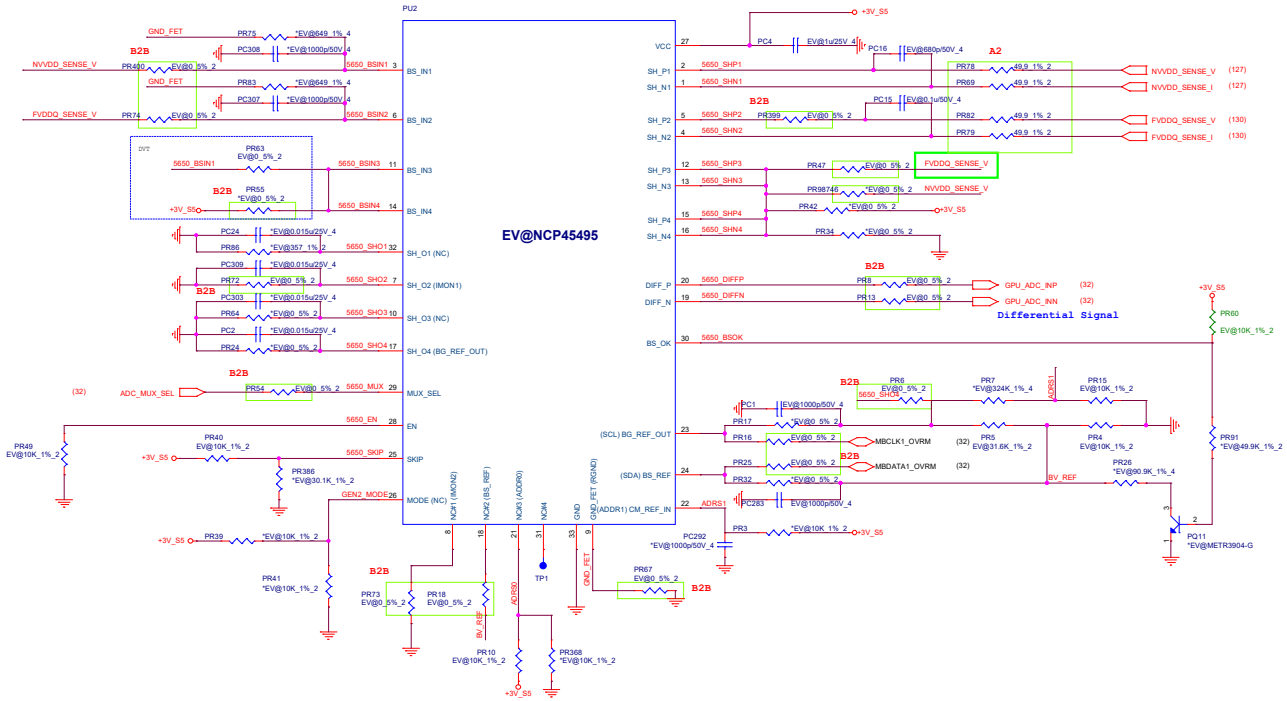
Power Monitoring with OVR-M GEN2



8-BIT I2C ADDR OF OVR-M GEN2

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

		GEN1					GEN2		
		AL045492000			AL005650002		AL045495000		
	Location	status	value	p/n	value	p/n	status	value	p/n
pin3	PR8328	stuff	665 ohm	CS16652FB04	499 ohm	CS14992FB24	un stuff		
	PC8186	stuff	1000pF	CH21006KB16			un stuff		
	PR8332	stuff	75k ohm	CS37501FE00			stuff	0 ohm	CS00001JE18
pin6	PR8330	stuff	665 ohm	CS16652FB04	499 ohm	CS14992FB24	un stuff		
	PC8183	stuff	1000pF	CH21006KB16			un stuff		
	PR8336	stuff	75k ohm	CS37501FE00			stuff	0 ohm	CS00001JE18
pin32	PC8188	stuff	0.015uF	CH3154KB00			un stuff		
	PR8356	stuff	634 ohm	CS16341FE01	475 ohm	CS14751FE00	un stuff		
pin7	PC8189	stuff	0.015uF	CH3154KB00			un stuff		
	PR8357	stuff	634 ohm	CS16341FE01	475 ohm	CS14751FE00	stuff	0 ohm	CS00001JE18
pin8	PR8388	un stuff	0 ohm	CS00001JE18			0 ohm	0 ohm	CS00001JE18
pin18	PR8386	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
pin21	PR8389	un stuff	10k ohm	CS31001FE14			stuff	10k ohm	CS31001FE14
	PR8391	un stuff	10k ohm	CS31001FE14					
pin9	PR8390	stuff	0 ohm	CS00001JE18					
pin22 23 24	PR8385	un stuff	10k ohm	CS31001FE14			un stuff		
	PC8198	stuff	0.015uF	CH3154KB00			un stuff		
	PR10422	stuff	0 ohm	CS00001JE18			un stuff		
	PR10421	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
	PR10424	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
	PR10437	stuff	10k ohm	CS31001FE14					
	PR10423	stuff	0 ohm	CS00001JE18			un stuff		
	PC8197	stuff	1000pF	CH21006KB16					
	PC10413	stuff	1000pF	CH21006KB16			stuff		
	PR10438	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
	PR10425	stuff	365k ohm	CS43651FE01			un stuff		
	PR10436	stuff	681k ohm	CS46811FE01			stuff		
	PR10435	stuff	237k ohm	CS42372FB07	316k	CS43162FB00	stuff	31.6k ohm	CS33161FE00
pin4 5	PC8187	stuff	0.1uF	CH4106K9B01			stuff	0.1uF	CH4106K9B01
	PR10641	stuff	49.9 ohm	CS04991FE00			stuff	0 ohm	CS00001JE18
	PR8340	stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
	PR8338	stuff	49.9 ohm	CS04991FE00			stuff	0 ohm	CS00001JE18
pin1 2	PC8182	stuff	680pF	CH16806KB17			stuff		
	PR8335	stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
	PR8329	stuff	100 ohm	CS11001FE00			stuff	0 ohm	CS00001JE18
pin10	PC8192	un stuff							
	PR10439	un stuff							
pin17	PC8194	un stuff							
	PR10440	un stuff							
pin29	PR8370	stuff	0 ohm	CS00001JE18					
pin28	PR8375	stuff	10k ohm	CS31001FE14					
pin25	PR8376	stuff	10k ohm	CS31001FE14					
	PR8379	un stuff	30.1k ohm	CS33011FE00					
pin26	PR8382	un stuff	10k ohm	CS31001FE14					
	PR8383	un stuff	10k ohm	CS31001FE14					
pin8	PR8388	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
pin30	PR8360	stuff	10k ohm	CS31001FE14			stuff	10k ohm	CS31001FE14
	PR10463	stuff	49.9k ohm	CS34991FE02					
	PR10644	stuff	90.9k ohm	CS39092FB11					
	PQ8040	stuff	0 ohm	CS00001JE18			un stuff	0 ohm	CS00001JE18
pin19	PR8359	stuff	0 ohm	CS00001JE18					
pin20	PR8358	stuff	0 ohm	CS00001JE18					
pin 12 13 15 16	PR8341	stuff	0 ohm	CS00001JE18					
	PR10420	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18
	PR10719	un stuff	0 ohm	CS00001JE18	stuff	CS00001JE18			
pin27	PC8185	stuff	1uF	CH5101K9B01			stuff	1uF	CH5101K9B01
pin 11 14	PR8331	stuff	0 ohm	CS00001JE18			un stuff	0 ohm	CS00001JE18
	PR8344	un stuff	0 ohm	CS00001JE18			stuff	0 ohm	CS00001JE18

PU7012	Status
GB5(GN18-S5-B-KA/KB)	Stuff
GB5B(GN20-P0/P1)	Un-stuff

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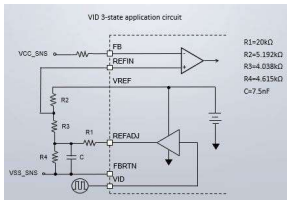
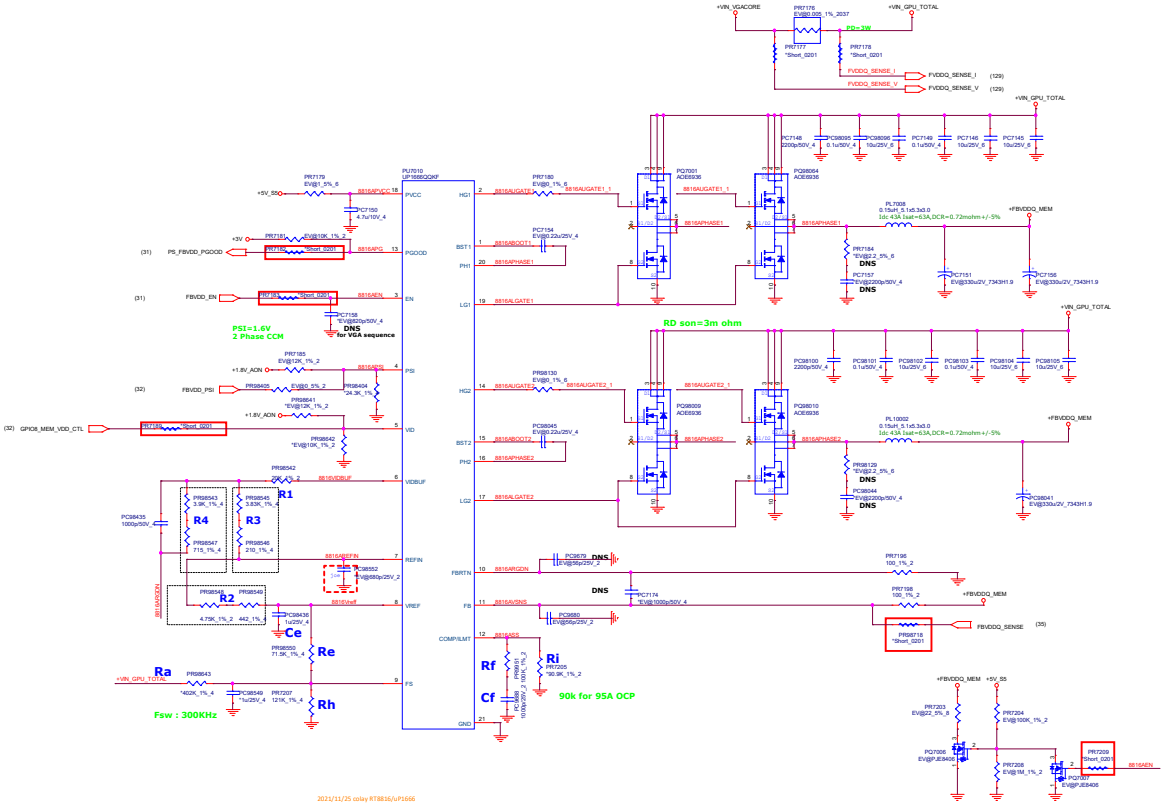
VGA Core - FBVDDQ_MEM

Table 2. Recommended V_{PSI} Setting in Four Operation Modes

Operation Mode	Recommended V_{PSI}
Full-Phase CCM	1.8V
Full-Phase DCM	1.2V
Single-Phase CCM	0.6V
Single-Phase DCM	GND





2021/11/25 colay RT8816/uP1666

	Ra	Ce	Re	Rh	Rf	Cf	Ri
RT8816BGQW AL008816002	stuff	0.1uF	NC	NC	NC	NC	STUFF 73.2K_1%_4 for 50A OCP
UP1666QQKF AL001666000	NC	1uF	STUFF	STUFF	STUFF CS4100 LFE08 100K_1%_2	STUFF CH2104K9E01 1000p/25V_2	NC

GN21-MB1 256b (150W)
2 Phase

FBVDDQ_MEM
EDP-Continous:52A
EDP-Peak:73A
OCP:95A

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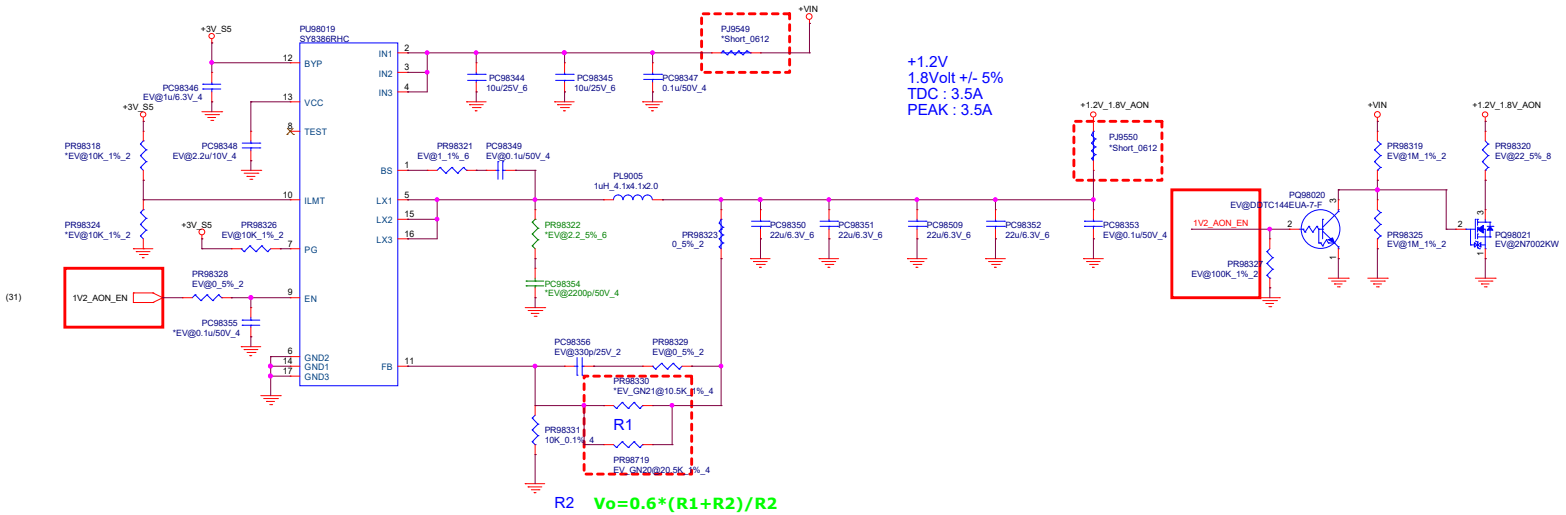
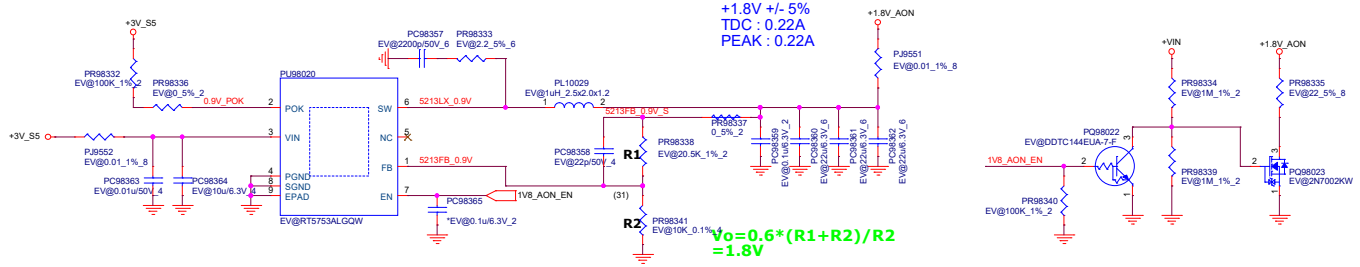
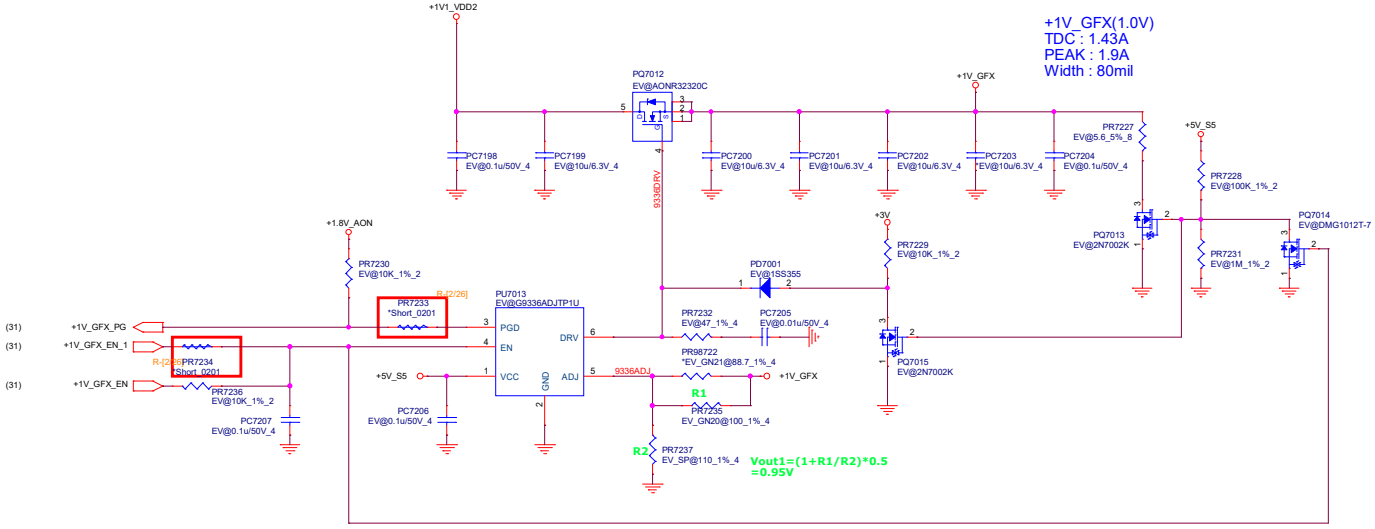
+3VPCU
+1.8V_AON
(11,13,45,68,75,81,88,106,111,112,113,123)
(25,30,31,32,35,38,39,40,41,45,47,126,130)

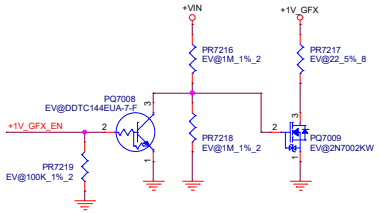
+5VPCU
+VIN
(68,75,79,81,93,113,145)
(16,45,112,113,114,123,126,127,142,143,145,146,147)

+5V_S5
+3V
(87,89,90,113,114,126,127,130,141,142,143,145)
(2,9,10,11,12,17,21,32,44,45,47,53,55,61,64,68,72,73,86,87,88,89,91,93,97,113,123,130,141,143)









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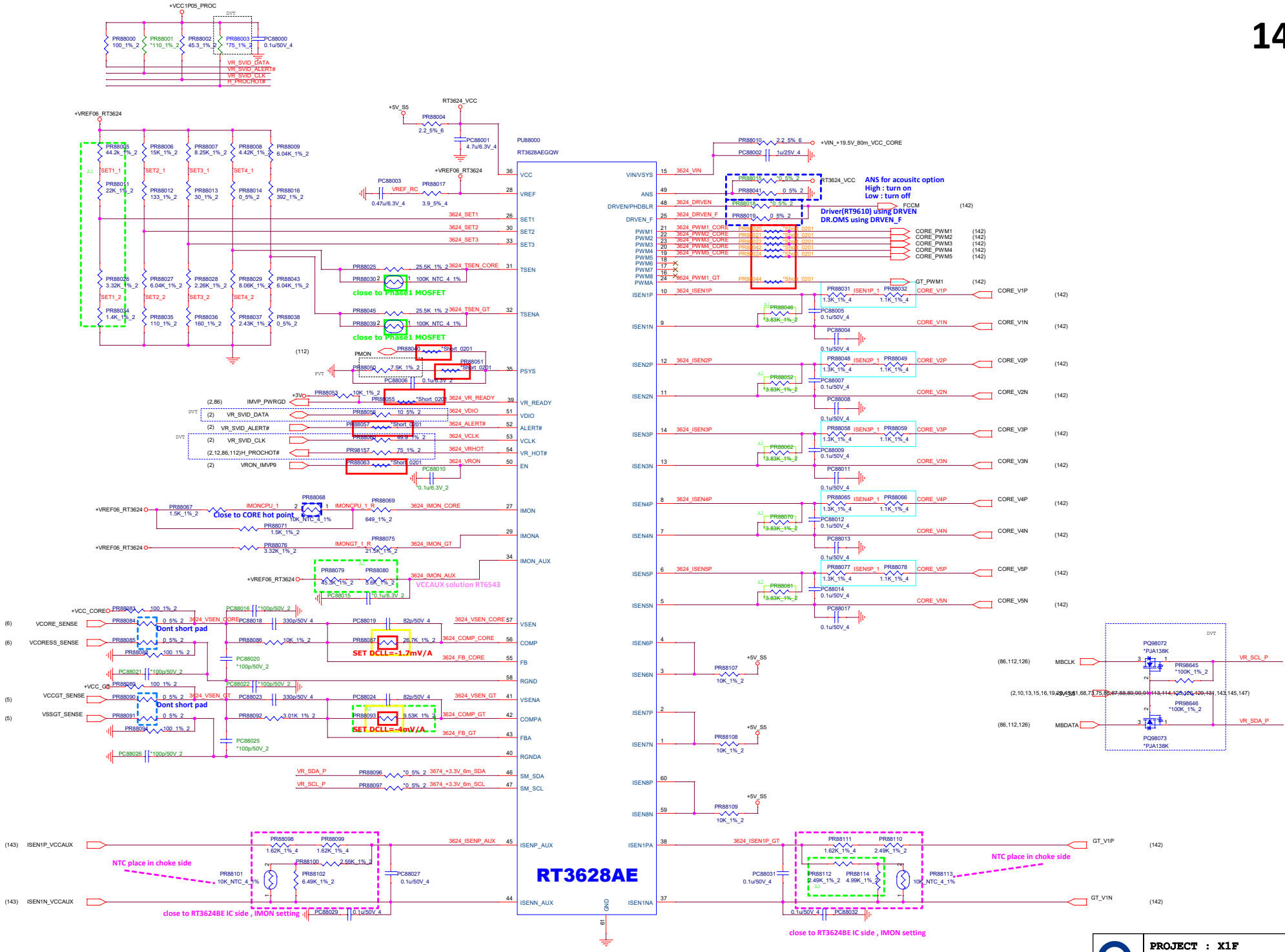
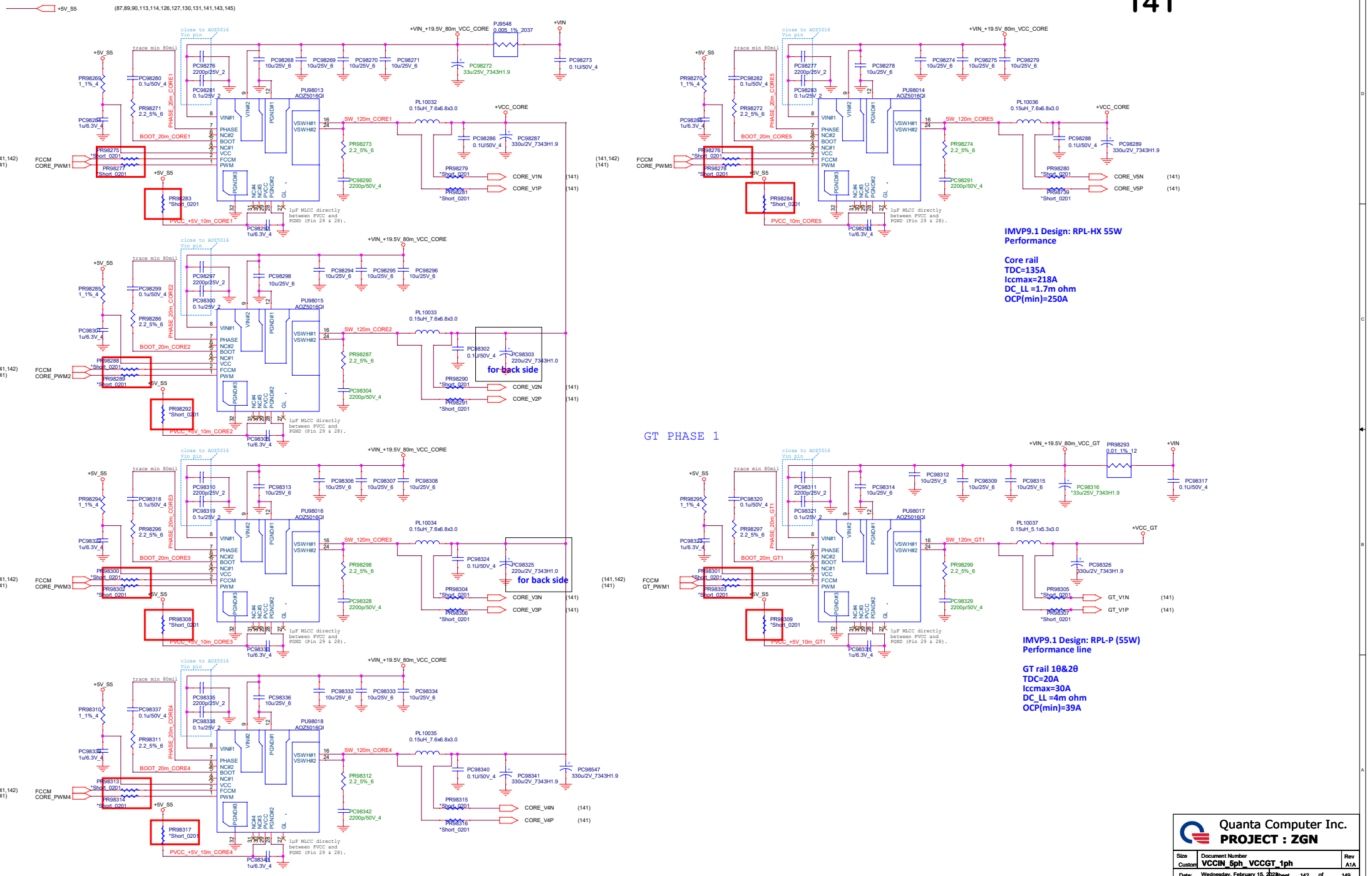

RT3628AE
PU88000
RT3628AEGQW
close to Phase1 MOSFET
Close to CORE hot point
Dont short pad
SET DCLL=-1.7mV/A
SET DCLL=-4mV/A
VCCAUX solution RT6543
NTC place in choke side
close to RT3624BE IC side , IMON setting
ANS for acousitc option
High : turn on
Low : turn off
Driver(RT9610) using DRVEN
DR.OMS using DRVEN_F
PROJECT : X1F
Quanta Computer Inc.
NB5
DDR3 (RT8231B)



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VID1	VID0	O/P
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

Default

+VIN (16,45,112,113,114,123,126,127,131,142,145,146,147)
+VCCIN_AUX (5,7)
+5V_S5 (87,89,90,113,114,126,127,130,131,141,142,145)
+3V_S5 (2,10,13,15,16,19,20,45,61,68,73,75,86,87,88,89,90,91,113,114,123,126,129,131,141,145,147)
+3V (2,9,10,11,12,17,21,32,44,45,47,53,55,61,64,68,72,73,86,87,88,89,91,93,97,113,123,130,131,141)

PR1412 *Short_0201 +3V_S5
PR1413 100K_1%_2 VCCIN_AUX_VID0
PR1414 *100K_1%_2 VCCIN_AUX_VID1
PR1416 *100K_1%_2
PR1417 *100K_1%_2

DNS siince P/H on EE side

2021/10/22
FOR AON36354 274K OCP~45A
OCP~45A@LMOS=3.5m

PU1039 RT6543BGQW

PR1418 357K_1%_2 RT6543_CS_DSI 1 CS_DIS
PR1421 2.2_1%_6 RT6543_VCC 15 PVCC
PC1773 4.7u/6.3V_4 16 VCC
PR1481 10K_1%_2 +3V_S5
PR1420 *10K_1%_2 +3V
(86) VCCIN_AUX_PG PR1423 *Short_0201 RT6543_PG 4 PGOOD
(10) VCCIN_AUX_VID1 PR1424 *Short_0201 RT6543_VID1 17 VID1
(10,16) VCCIN_AUX_VID0 PR1425 *Short_0201 RT6543_VID0 18 VID0
(21,22,86,114,123) SUSON PR1426 *10K_1%_2 RT6543_EN 19 EN
DVT (16,145) VCC1P05_PROC_PG PR1428 *Short_0201
(16,86,113,123,147) MAINON PR1430 *0_5%_2
+5V_S5 PR1434 *10K_1%_2 RT6543_FSWSEL 9 FSWSEL
PC1791 *0.1u/50V_4
PR1435 *10K_1%_2
21 AGND

VSYS 20
PC1774 0.1u/50V_4
RT6543_VSYS
PR1415 2.2_5%_6

UGATE 11 RT6543_UG PR1419 1_5%_6
BOOT 10 RT6543_BOOT PC1779 0.22uF/25V_4
PH 12 RT6543_PH
LGATE 13 RT6543_LG
PGND 14
ISENSEP 2 RT6543_ISP
ISENSEN 3 RT6543_ISN PR1427 *0_5%_2
VOUT 8 RT6543_VOUT
COMP 5 RT6543_COMP
FB 6
RGND 7

PC1792 2200p/50V_4
PR1431 10K_1%_4
PC1793 *470p/50V_4
PR1432 *1.4K_1%_2
PC1794 27p/50V_4
PR1436 6.34K_1%_2
PC1795 *0.1u/50V_4
RT6543_FB
RT6543_RGND

PQ1005 AONY36354
PR1422 2.2_5%_6
PC1786 2200p/25V_2
PVT
LMOS(max)=3.5m

PR1429 *Short_0201
PR1433 100_1%_2
PR1437 *Short_0201 VCC_AUX_SENSE (5)
PR1472 *Short_0201 VSS_AUX_SENSE (5)
PR1473 100_1%_2

+VIN_VCCIN_AUX
PJ9556 *Short_0612 +VIN
PC1775 10u/25V_6
PC1770 10u/25V_6
PC1771 10u/25V_6
PC1776 10u/25V_6
PC1777 0.1u/50V_4
PC1772 2200p/50V_4
PC1778 0.1u/50V_4

VAUX total BOM with EE:
a. 1pcs 330uF/6m
b. 18pcs 22uF/0603 MLCC includ EE side
c. Reserve 4pcs 22uF/6.3V MLCC

PL10038 0.15uH_5.1x5.3x3.0
+VCCIN_AUX
PR1479 *Short_0201
PR1478 *Short_0201
PC1780 0.1u/50V_4
PC98548 220u/2V_7343H1.0
PC1782 330u/2.5V_7343H1.9
ISEN1N_VCCAUX
ISEN1P_VCCAUX

PR1470 *Short_0201 RT6543_ISP
PR1476 5.49K_1%_4
PR1480 1.62K_1%_4
ISEN1P_VCCAUX ISEN1P_VCCAUX (141)
PC1800 *0.01u/50V_4
PC1799 0.22u/10V_4
2021/09/09 PUR request
PR1477 1.87K_1%_4
PR1471 10K_NTC_4_1%
PR1469 *Short_0201 RT6543_ISN
ISEN1N_VCCAUX ISEN1N_VCCAUX (141)

RPL-HX (55W) Performance 1 Φ

+VCCIN_AUX
IPL2:24A
ICCMAX:40A
OCP:55A
L/L=-2.0mV/A

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	VCCIN_AUX IC (RT6543AGQW)	A1A
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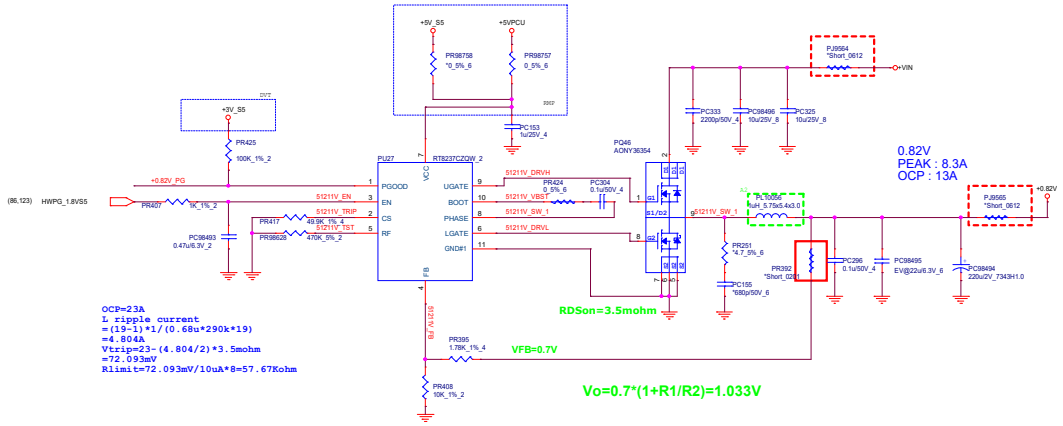

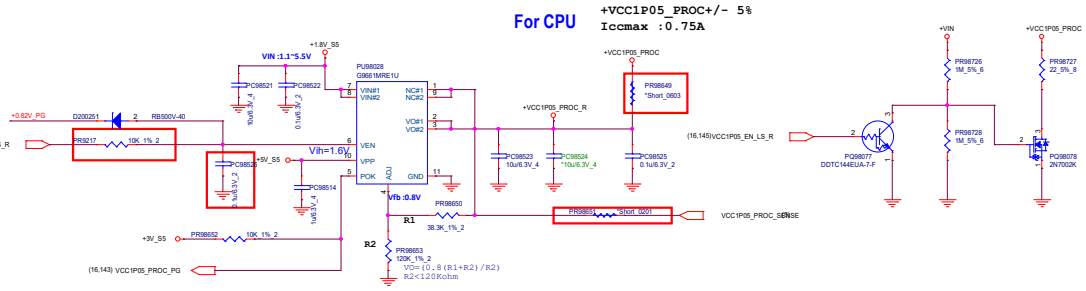

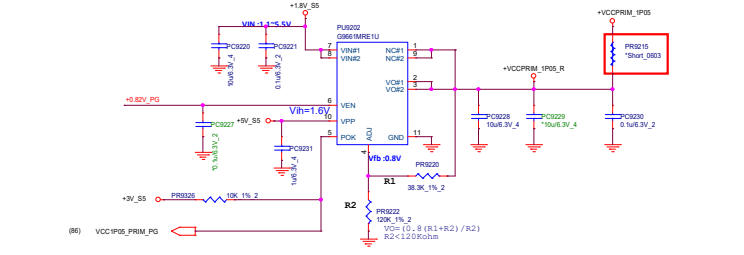

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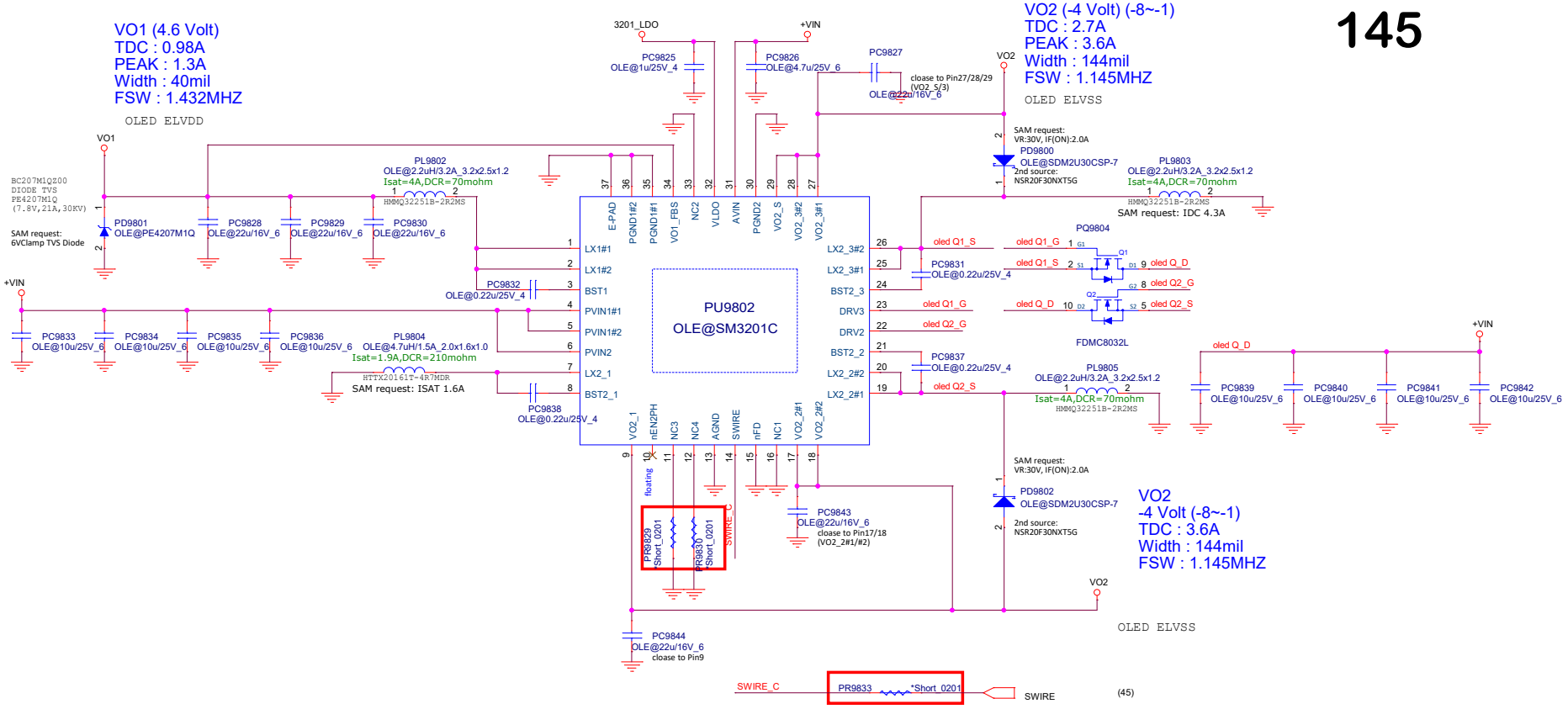

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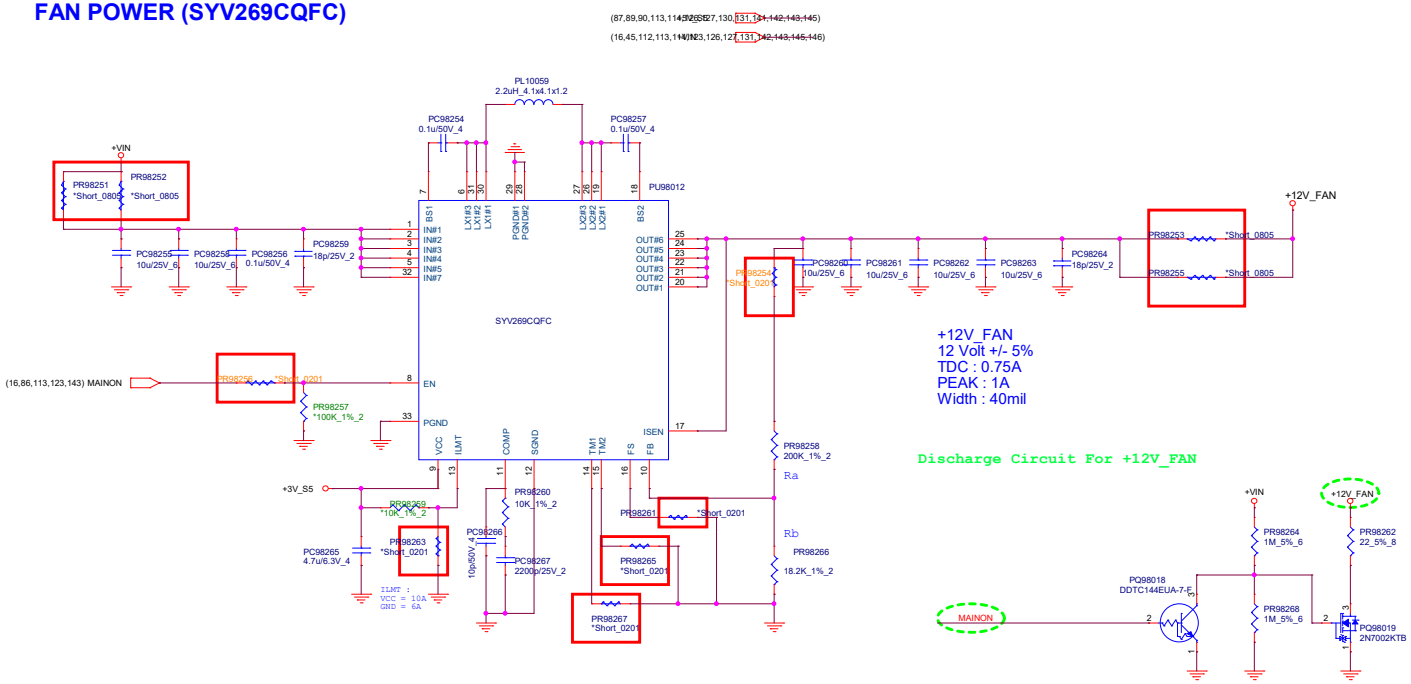
FAN POWER (SYV269CQFC)



+12V_FAN
12 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

Discharge Circuit For +12V_FAN

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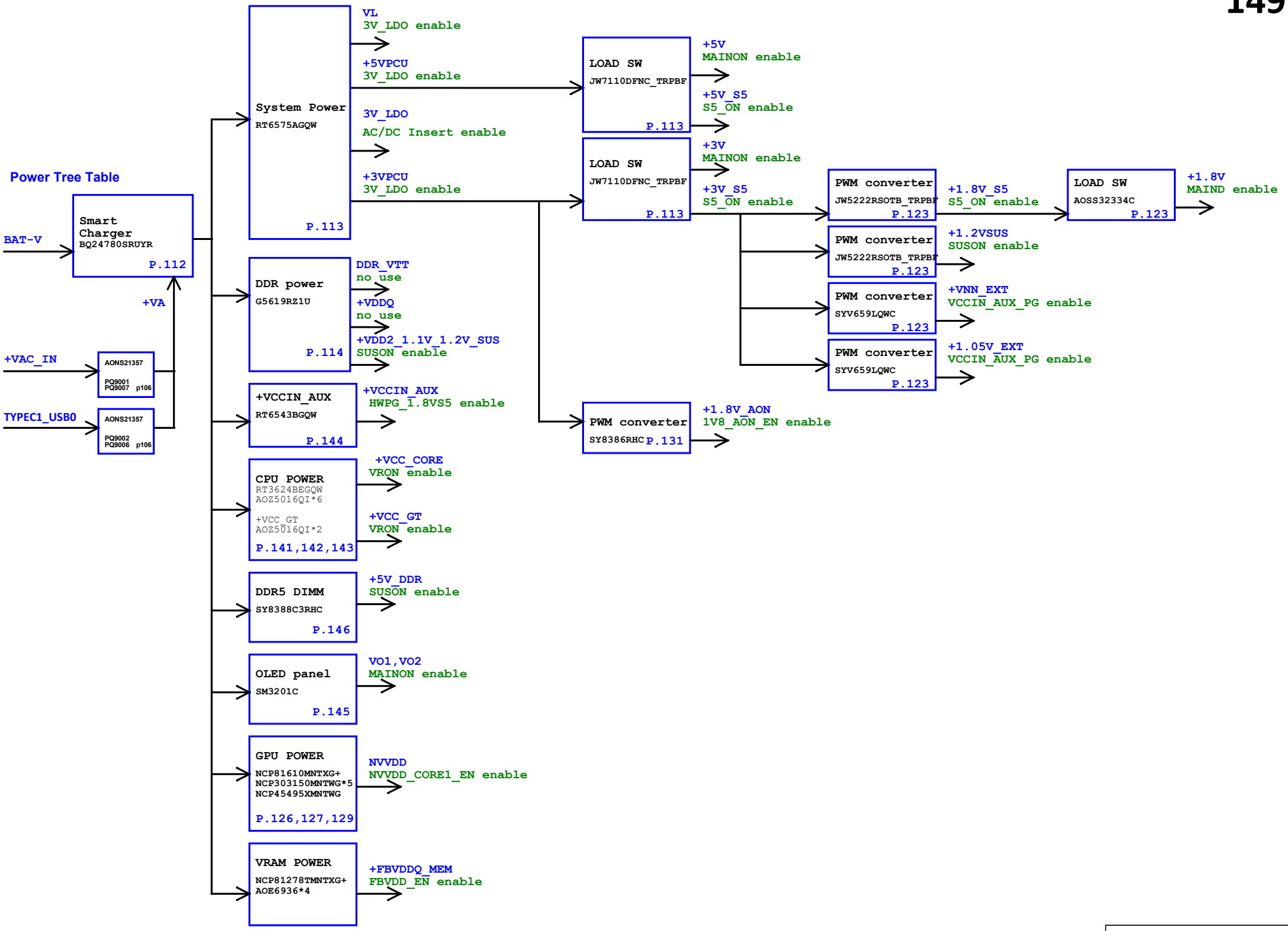

Quanta Computer Inc.
PROJECT : ZGN

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