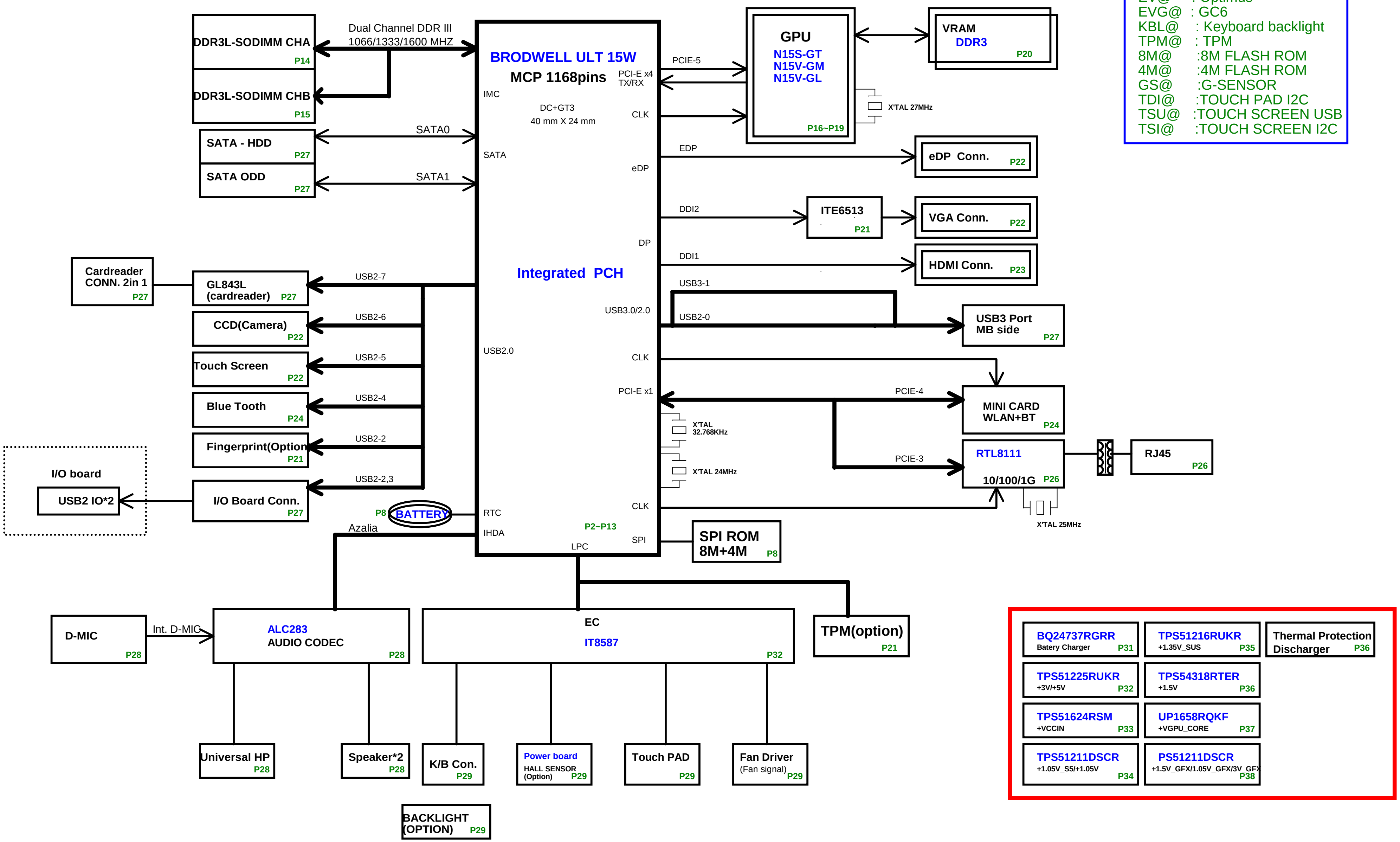
ZQ0_GDDR5 BWD ULT SYSTEM BLOCK DIAGRAM

BOM

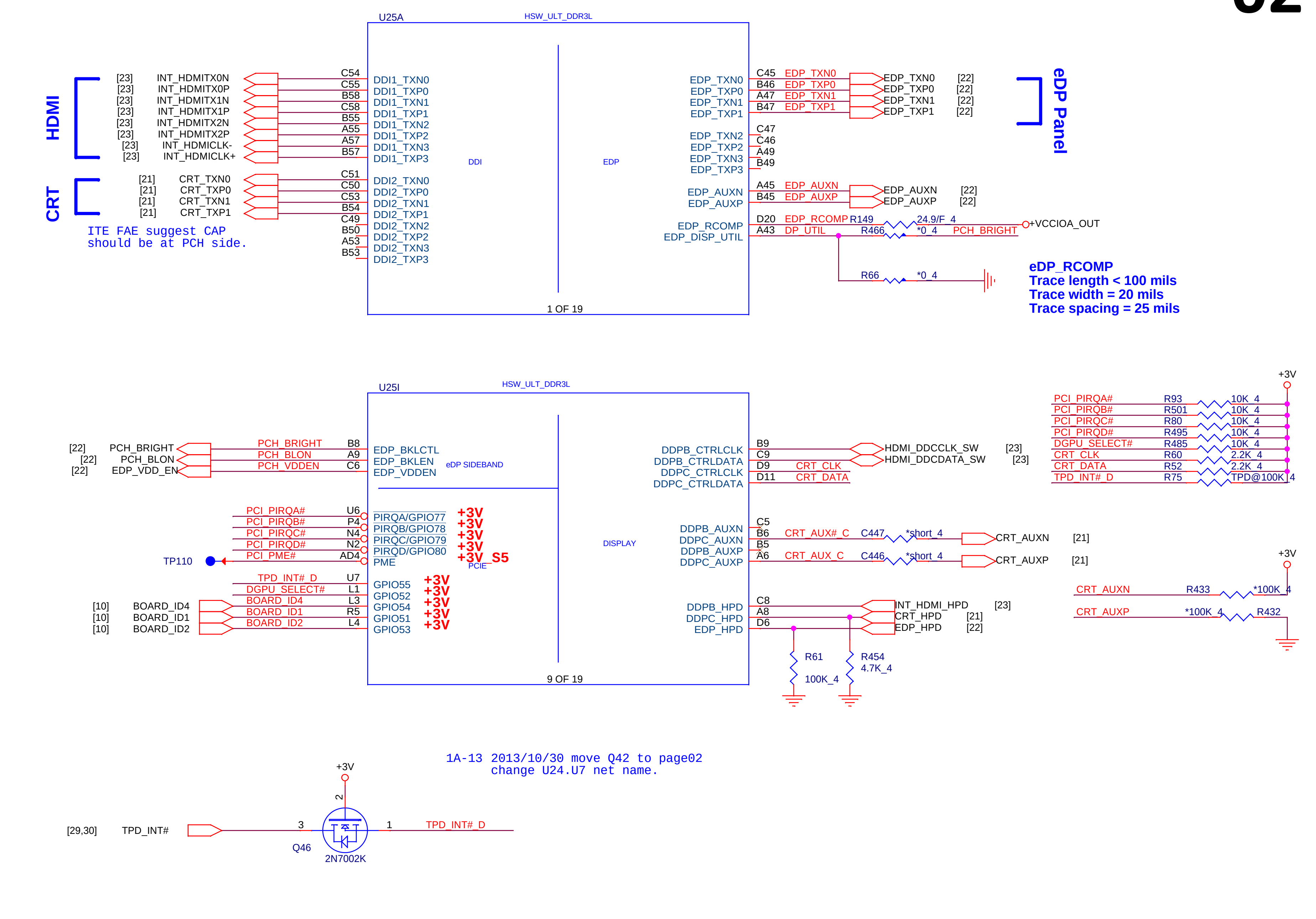
IV@ : iGPU
EV@ : Optimus
EVG@ : GC6
KBL@ : Keyboard backlight
TPM@ : TPM
8M@ :8M FLASH ROM
4M@ :4M FLASH ROM
GS@ :G-SENSOR
TDI@ :TOUCH PAD I2C
TSU@ :TOUCH SCREEN USB
TSI@ :TOUCH SCREEN I2C



Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: Block Diagram	Rev 3A
Date: Monday, April 07, 2014	Sheet 1 of 46	

Haswell ULT (DISPLAY,eDP)

02



Quanta Computer Inc.

PROJECT : ZQ0

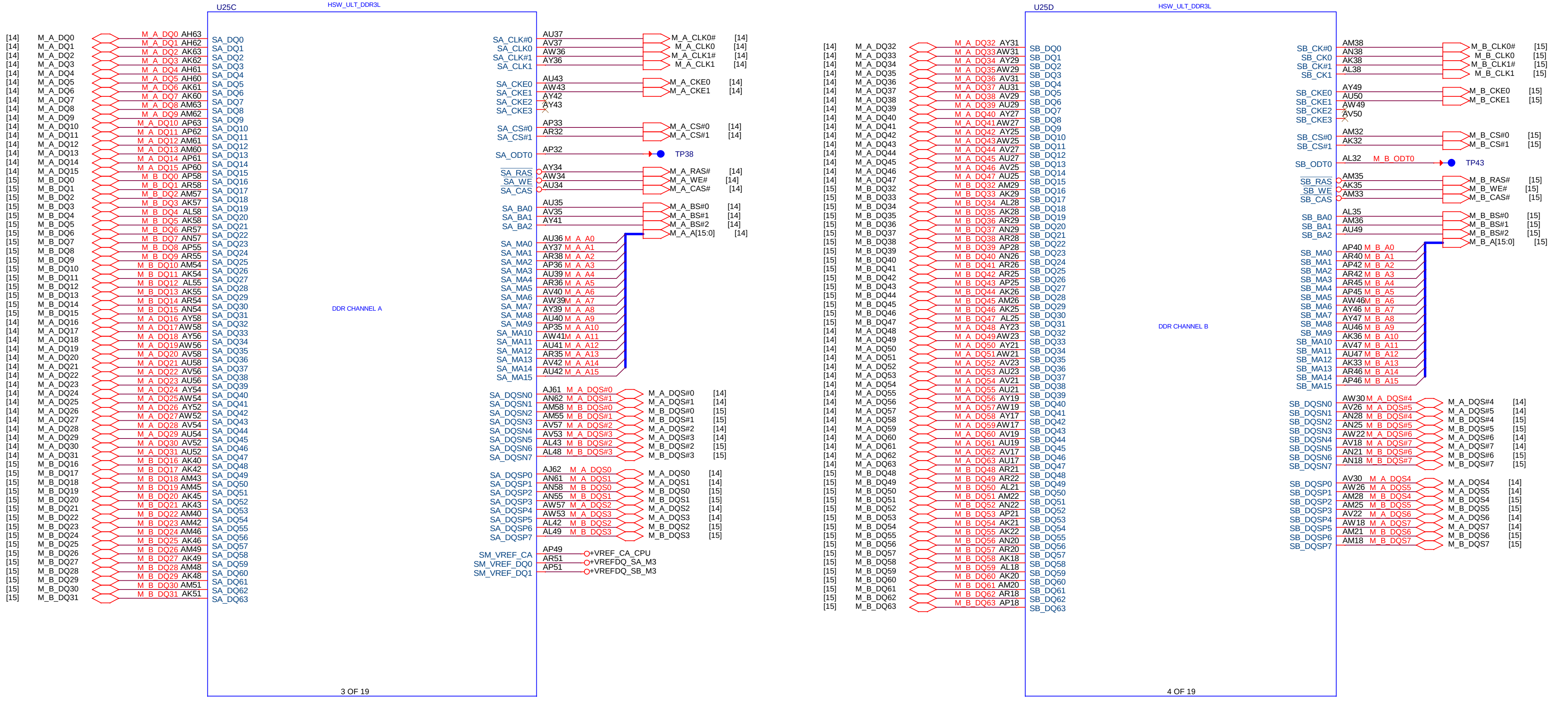
Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	3A

Date: Monday, April 07, 2014 Sheet 2 of 46

Change Data and DQS to interleave.

Haswell ULT (DDR3L)

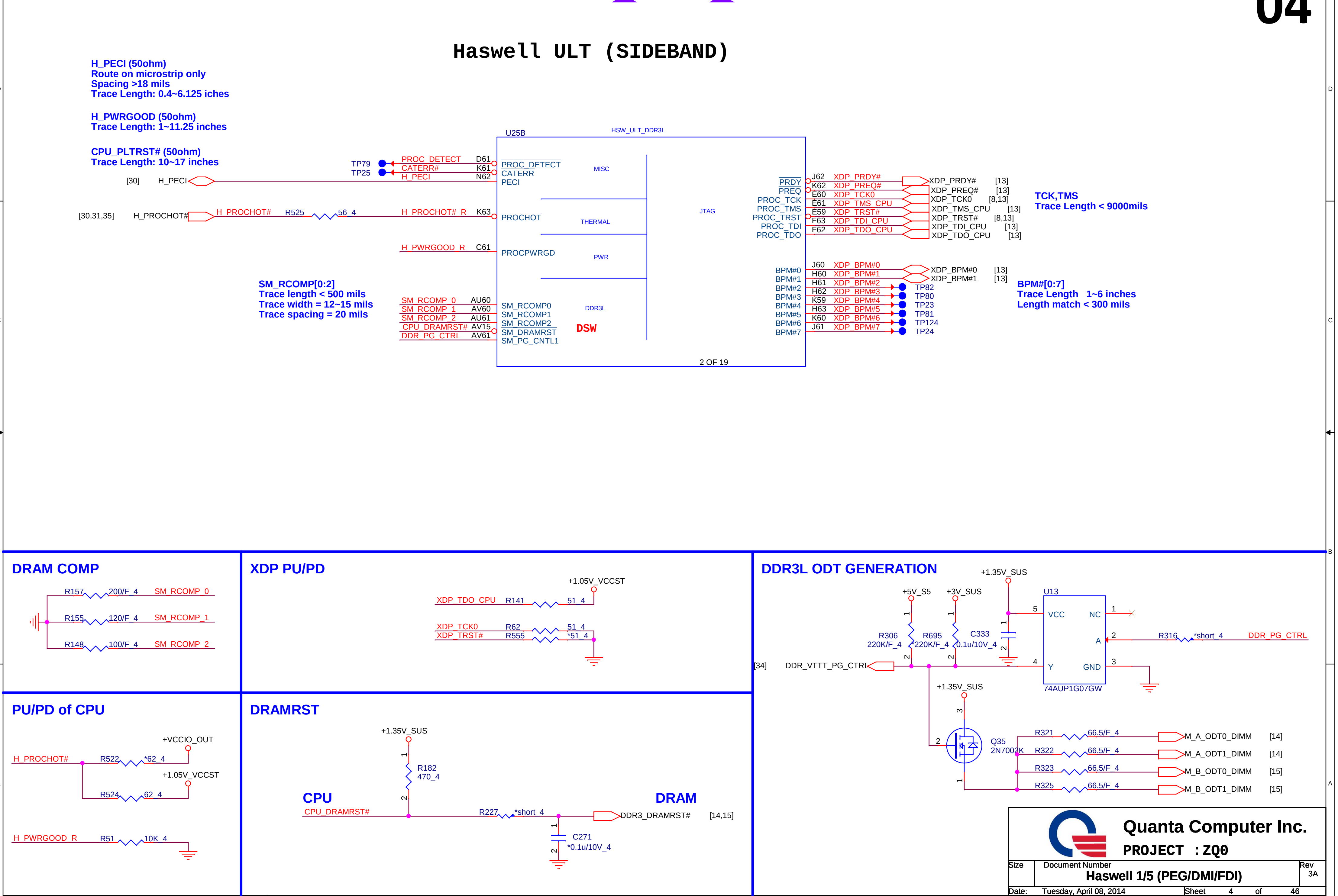
Haswell Processor (DDR3)



Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	3A
Date: Monday, April 07, 2014	Sheet 3 of 46	

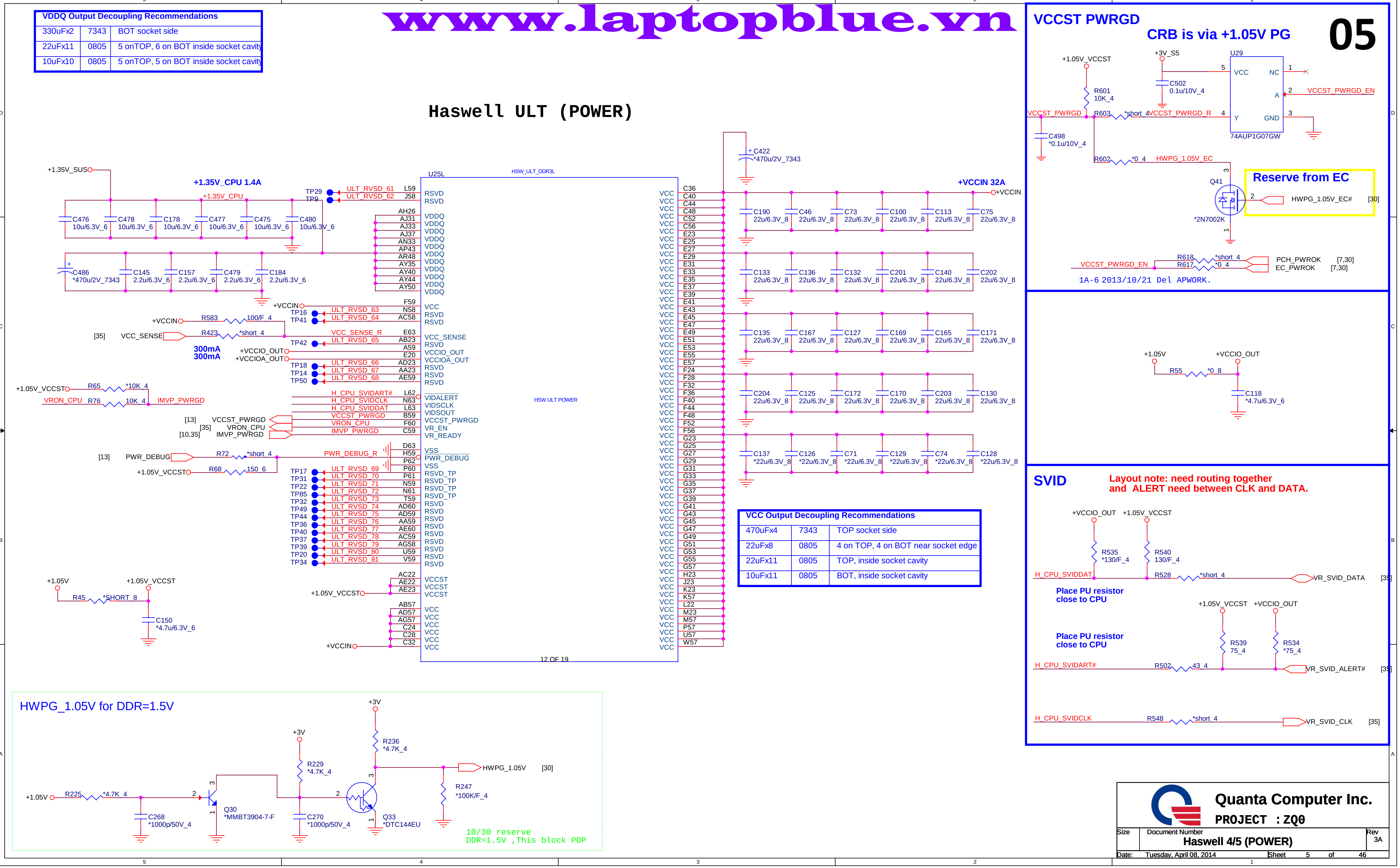


Quanta Computer Inc.	
PROJECT : ZQ0	
Size	Document Number: Haswell 1/5 (PEG/DMI/FDI)	Rev 3A
Date: Tuesday, April 08, 2014	Sheet 4 of 46

Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity



VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

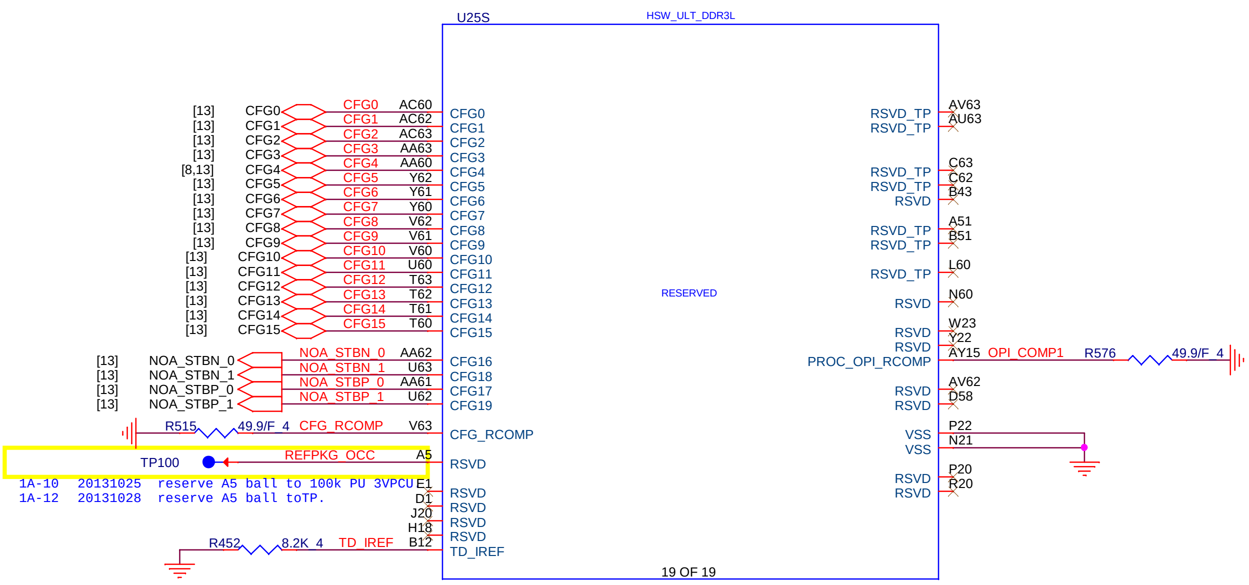
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	Haswell 4/5 (POWER)	3A

Date: Tuesday, April 08, 2014 Sheet 5 of 46

Haswell ULT (CFG,RSVD)



Processor Strapping

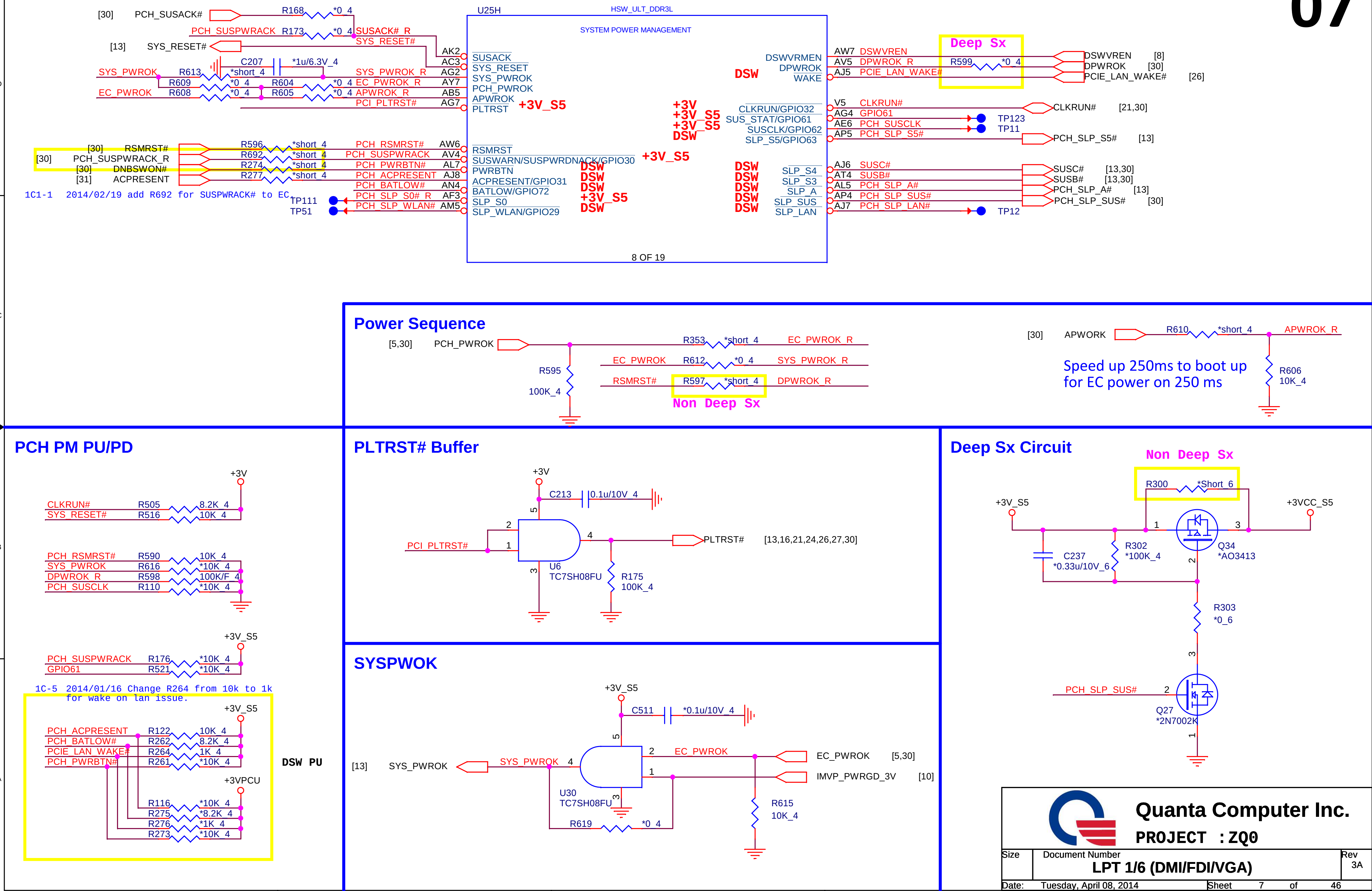
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R134 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R552 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R549 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R537 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R532 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R126 *1K_4

Quanta Computer Inc.
PROJECT : ZQ0

Size | Document Number: Haswell 5/5 (CFG/GND) | Rev 3A
Date: Monday, April 07, 2014 | Sheet 6 of 46

Haswell ULT PCH (PM)

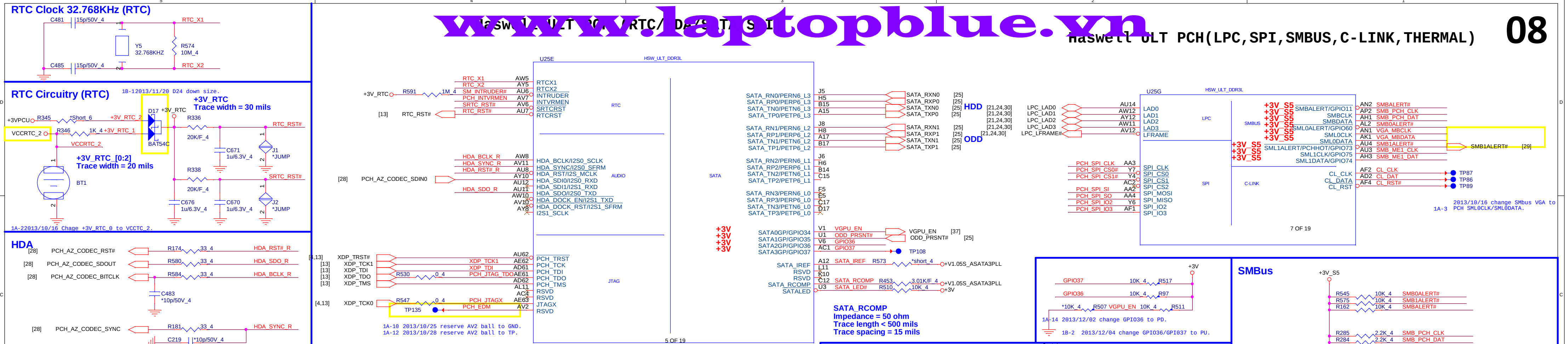
07

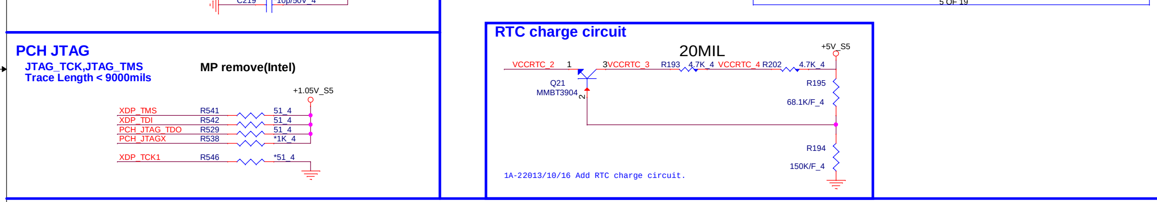


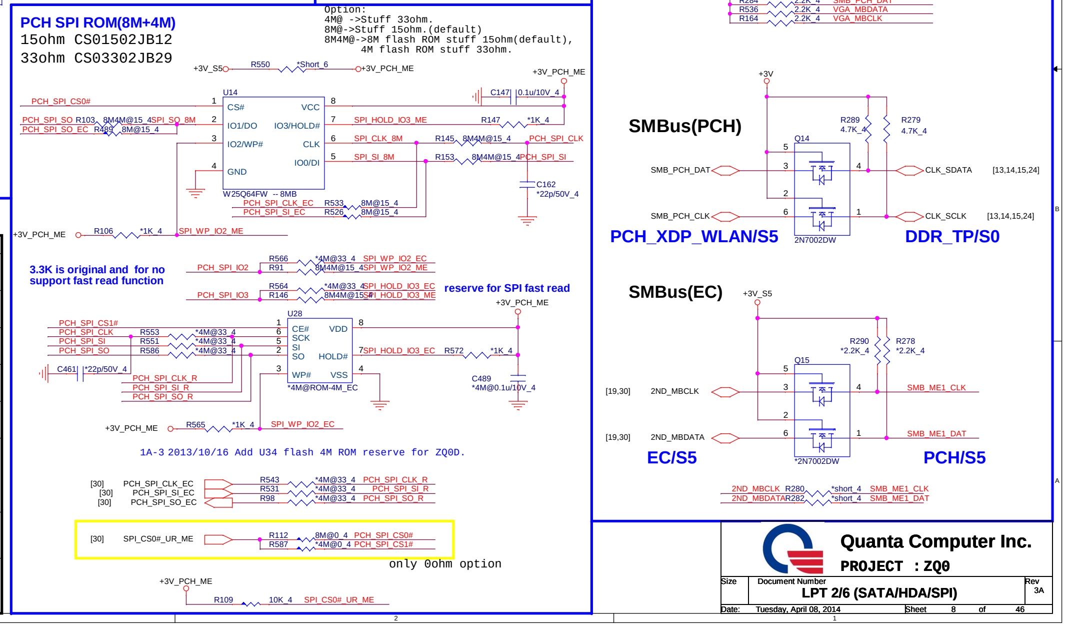
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	3A
Date: Tuesday, April 08, 2014	Sheet 7 of 46	







ULT Strapping Table

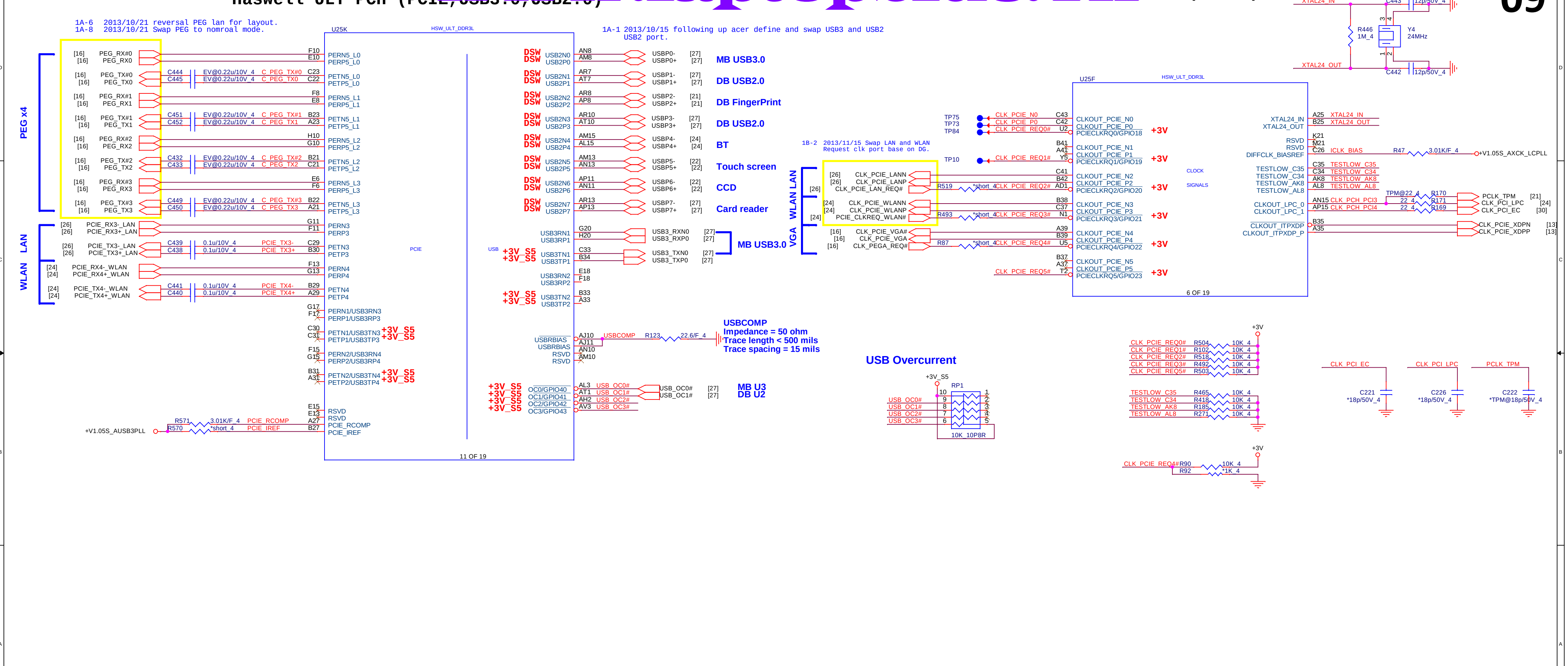
Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	**0 = Default enable (iPD 20K)** 1 =Disable No-Reboot mode	+3V R508 *1K_4 SPKR SPKR [10,28]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	**0 = Default can program ME (iPD 20K)** 1 =can't program ME	HDA_SDO_R R582 *short_4 ME_WR# [30]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**1=Should be always pull-up**	+3V_RTC R592 330K_4 PCH_INTVRMEN R588 *330K_4
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	[10] GPIO66 +3V R578 *1K_4 GPIO66 R577 *1K_4
GPIO86	Boot BIOS Strap Bit		**0 = Default SPI (iPD 20K)** 1 =LPC	[10] GPIO86 +3V R136 *1K_4 GPIO86 R129 *1K_4
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	[10] GPIO15 +3V_S5 R99 8.2K_4 GPIO15 R95 *1K_4
CFG4	DP presence strap		**0 = Enable an external display port is connected to the eDP** 1 =disable	[6,13] CFG4 CFG4 R544 1K_4
DSWVREN	Deep Sx well on die VR enable		**1=Should be always pull-up**	[7] DSWVREN +3V_RTC R589 330K_4 DSWVREN R585 *330K_4

Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	3A

Date: Tuesday, April 08, 2014 Sheet 8 of 46



Quanta Computer Inc.

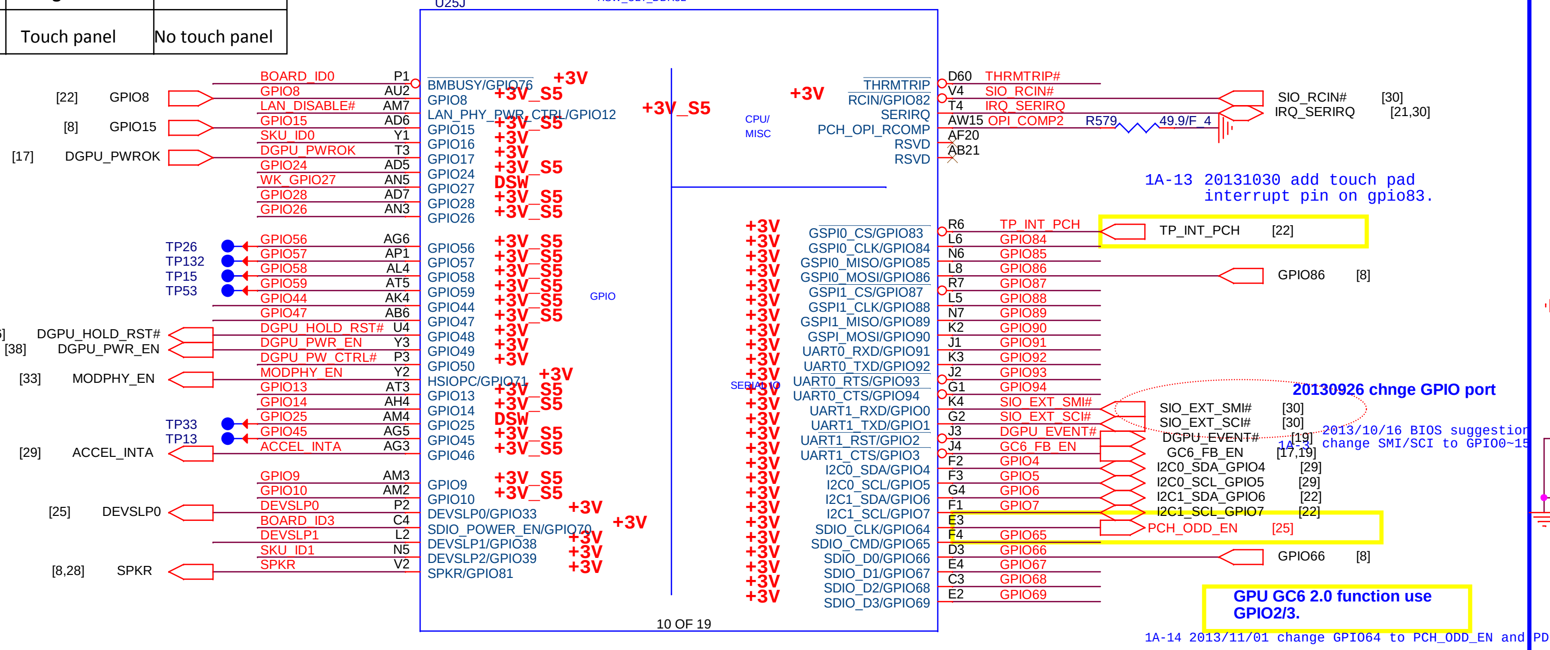
PROJECT : ZQ0

Size	Document Number	Rev
	LPT 3/6 (PCIE/USB/CLK)	3A

Date: Tuesday, April 08, 2014 Sheet 9 of 46

Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

	High	Low
GPIO8	Touch panel	No touch panel



1A-13 20131030 add touch pad interrupt pin on gpio83.

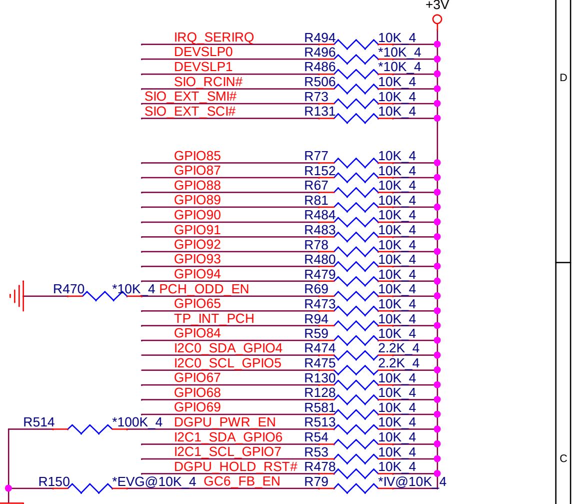
20130926 chnge GPIO port

2013/10/16 BIOS suggestion change SMI/SCI to GPIO0~15

GPU GC6 2.0 function use GPIO2/3.

1A-14 2013/11/01 change GPIO64 to PCH_ODD_EN and PD.

PCH GPIO PU/PD

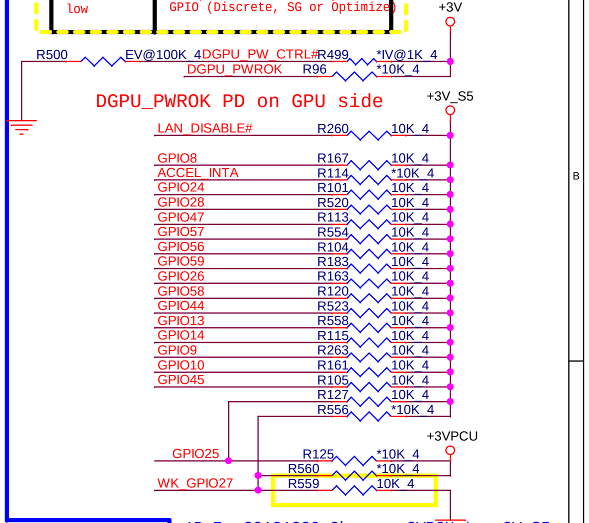


1A-1 20131015 For GC6 NV DG GC6_FB_EN PD.

1A-8 20131022 Change GPIO83/84 GPU GC6 pin to GPIO2/3.

1A-12 20131029 Change GPIO45 to PU S5, duble GPIO58 one is GPIO56.

high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

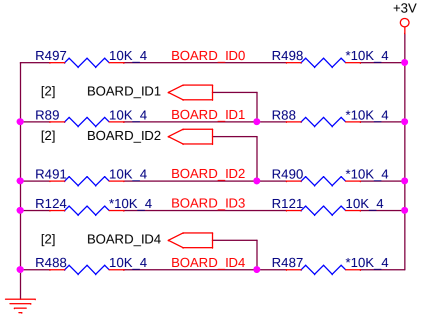


DGPU_PWROK PD on GPU side

1B-7 20131220 Change +3VPCU to +3V_S5 non deep sx

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

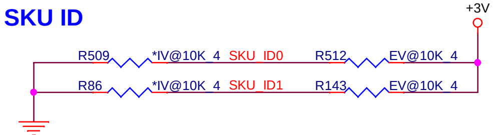
Board ID



	Low	High
BOARD_ID0	N15V-GL-B	N15V-GM-B
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	Reserve for Touch pad, default(low)	
BOARD_ID3	DTPM	No DTPM
BOARD_ID4	Non-Dolly (Default)	Dolly

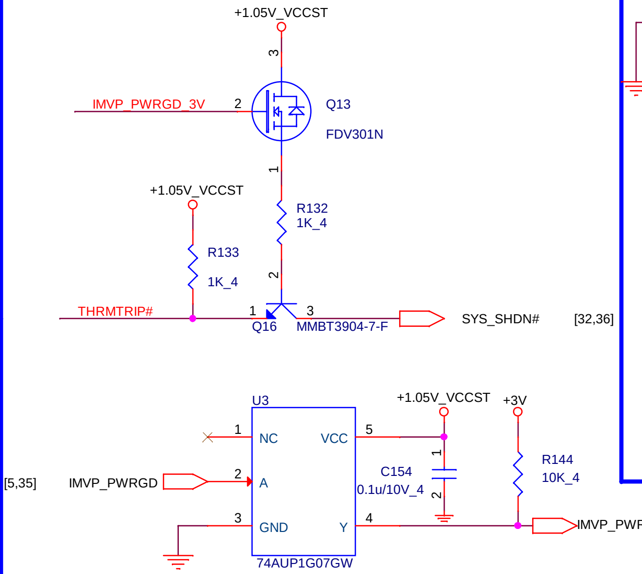
RAM ID

SKU ID



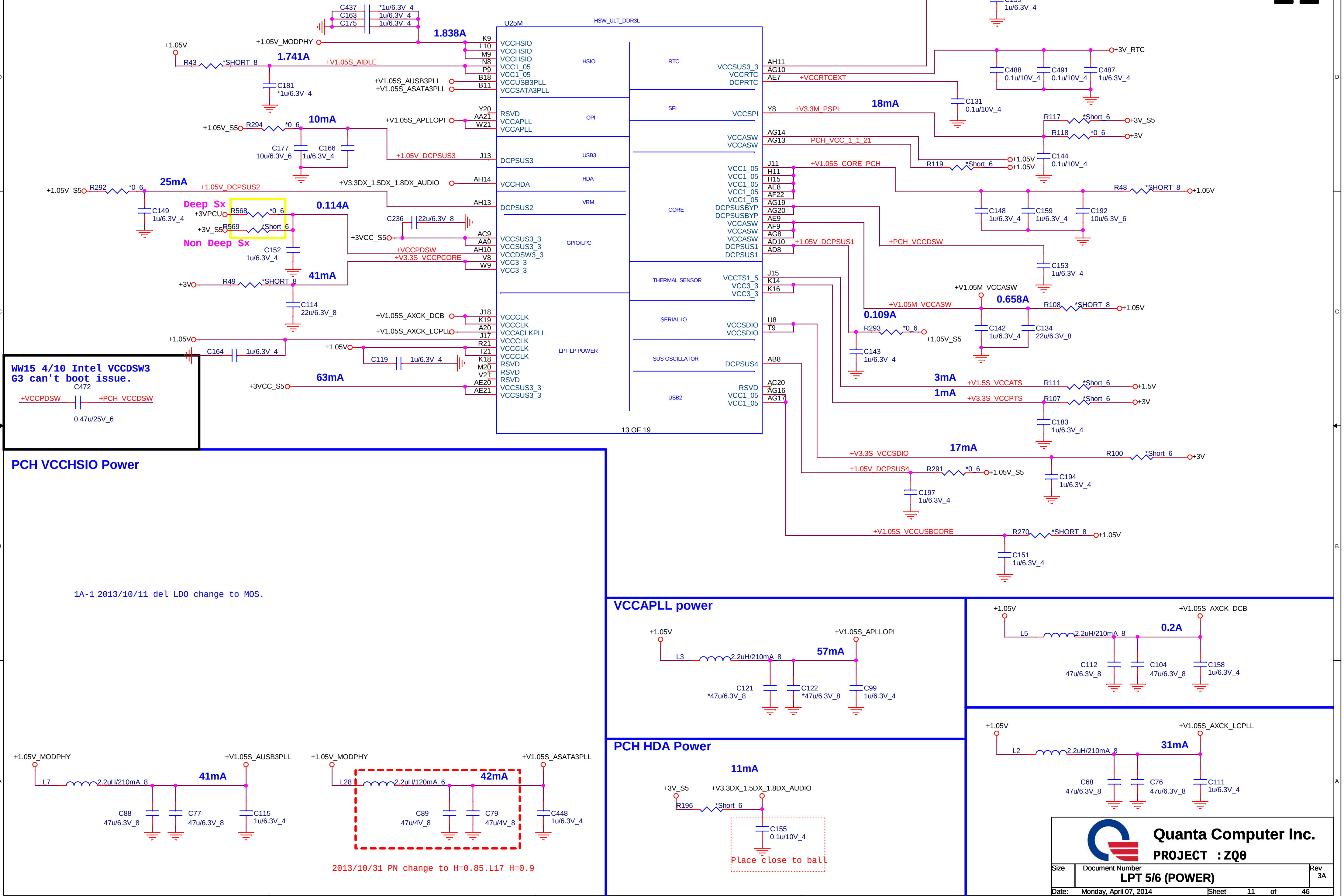
	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



Quanta Computer Inc.
PROJECT : ZQ0
Size | Document Number: LPT 4/6 (GPIO/MISC) | Rev 3A
Date: Tuesday, April 08, 2014 | Sheet 10 of 46

Haswell ULT PCH (Power)



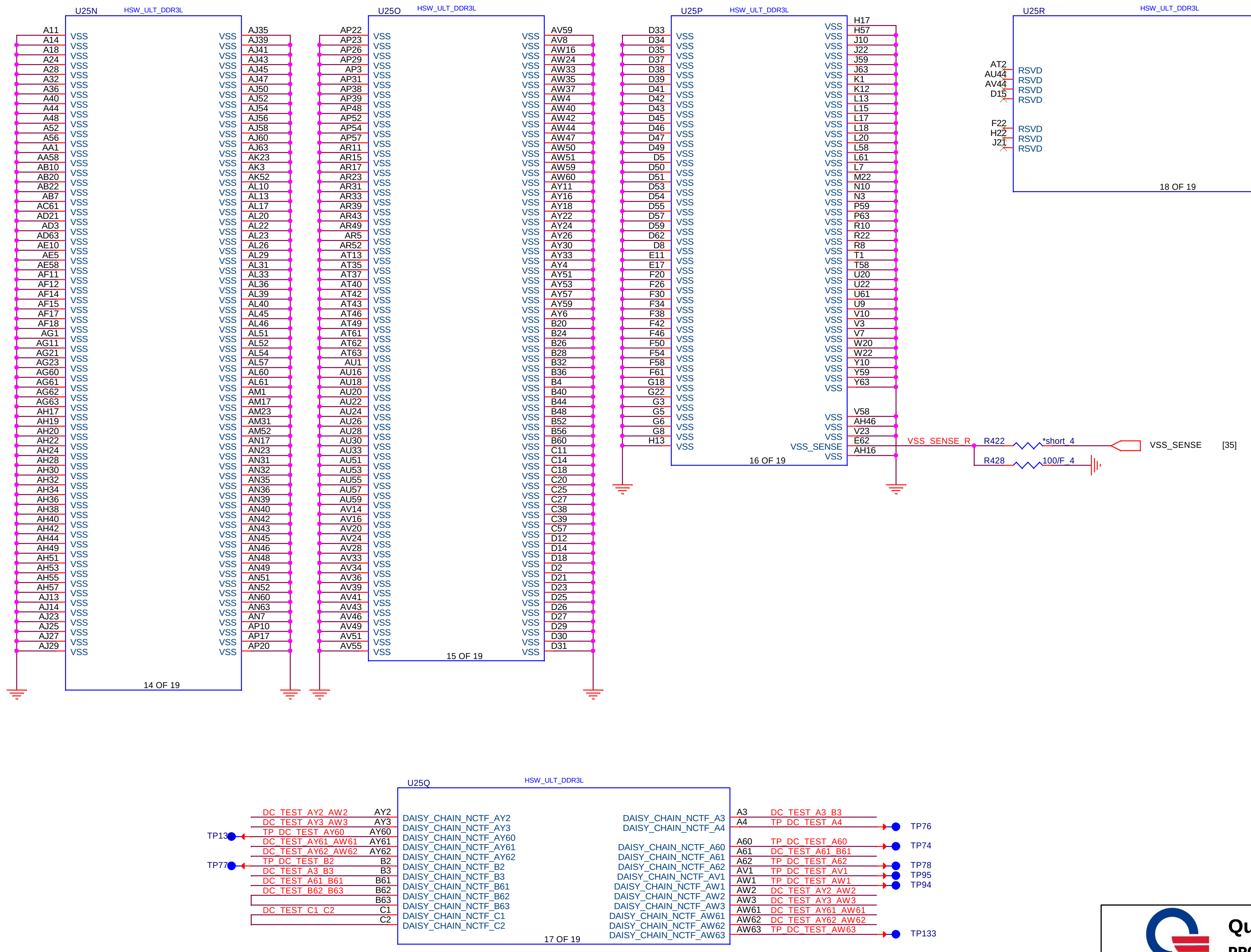
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	LPT 5/6 (POWER)	3A

Date: Monday, April 07, 2014 Sheet 11 of 46

Haswell ULT (GND)

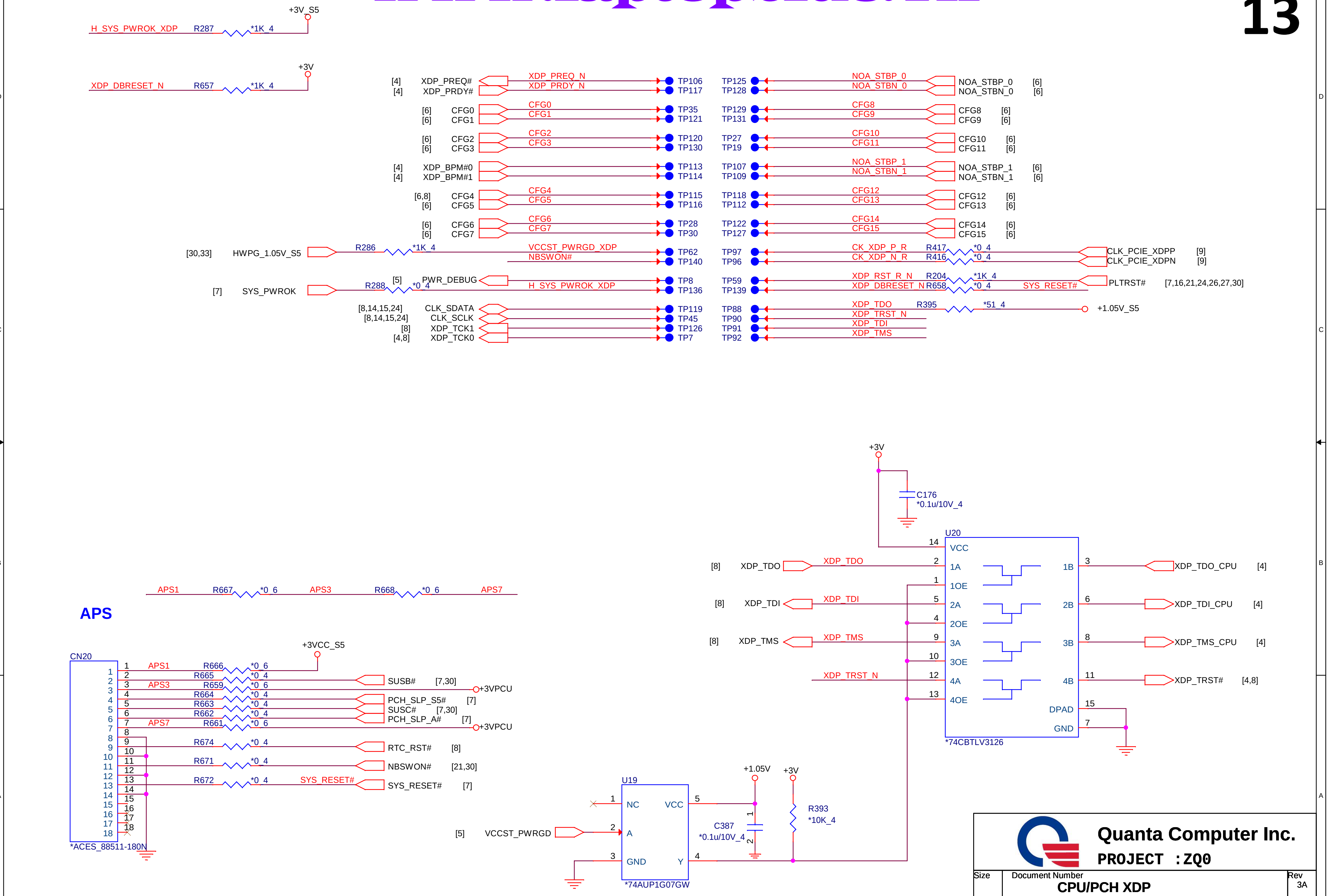


Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	LPT 6/6 (GND)	3A

Date: Monday, April 07, 2014 Sheet 12 of 46

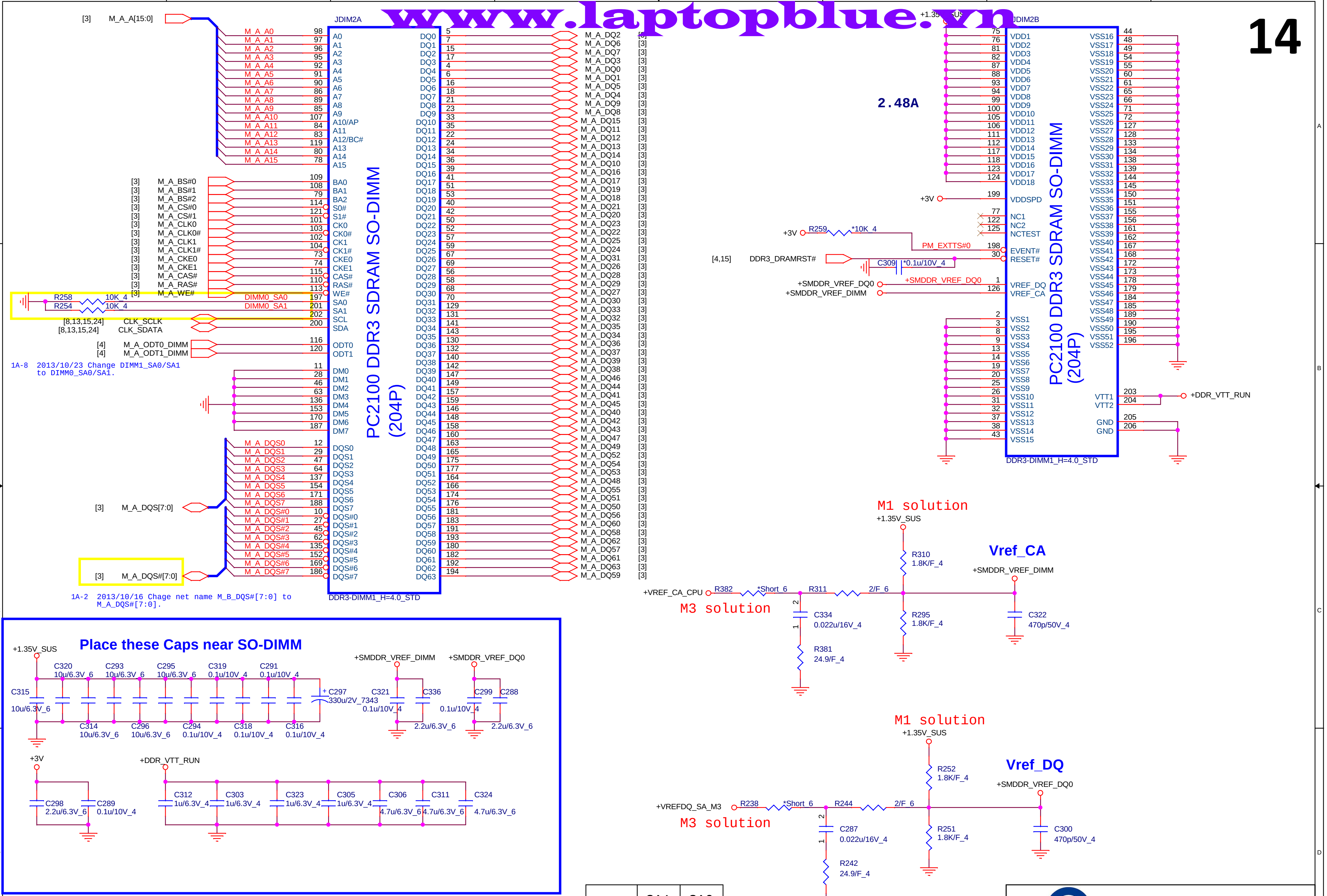


Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	CPU/PCH XDP	3A

Date: Tuesday, April 08, 2014 Sheet 13 of 46



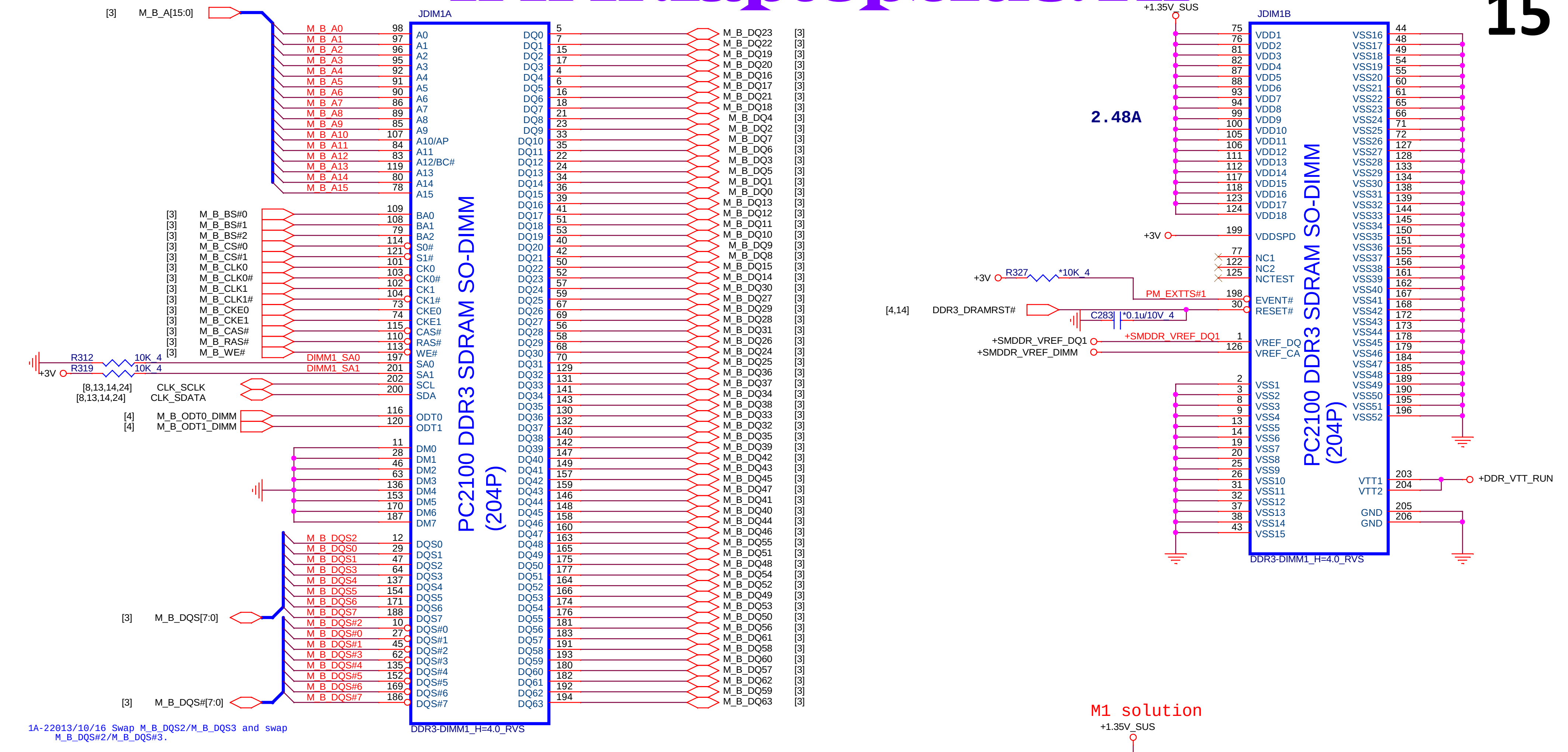
	SA1	SA0
CHA	0	0
CHB	1	0

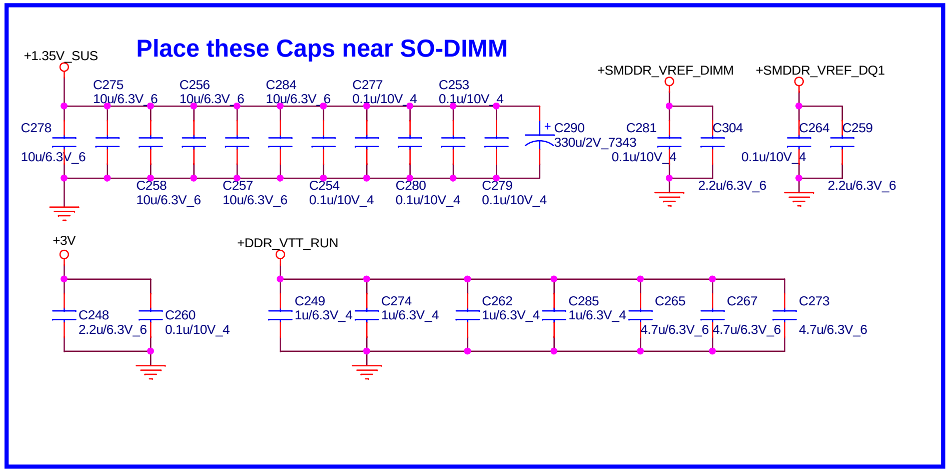
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A

Date: Monday, April 07, 2014 Sheet 14 of 46





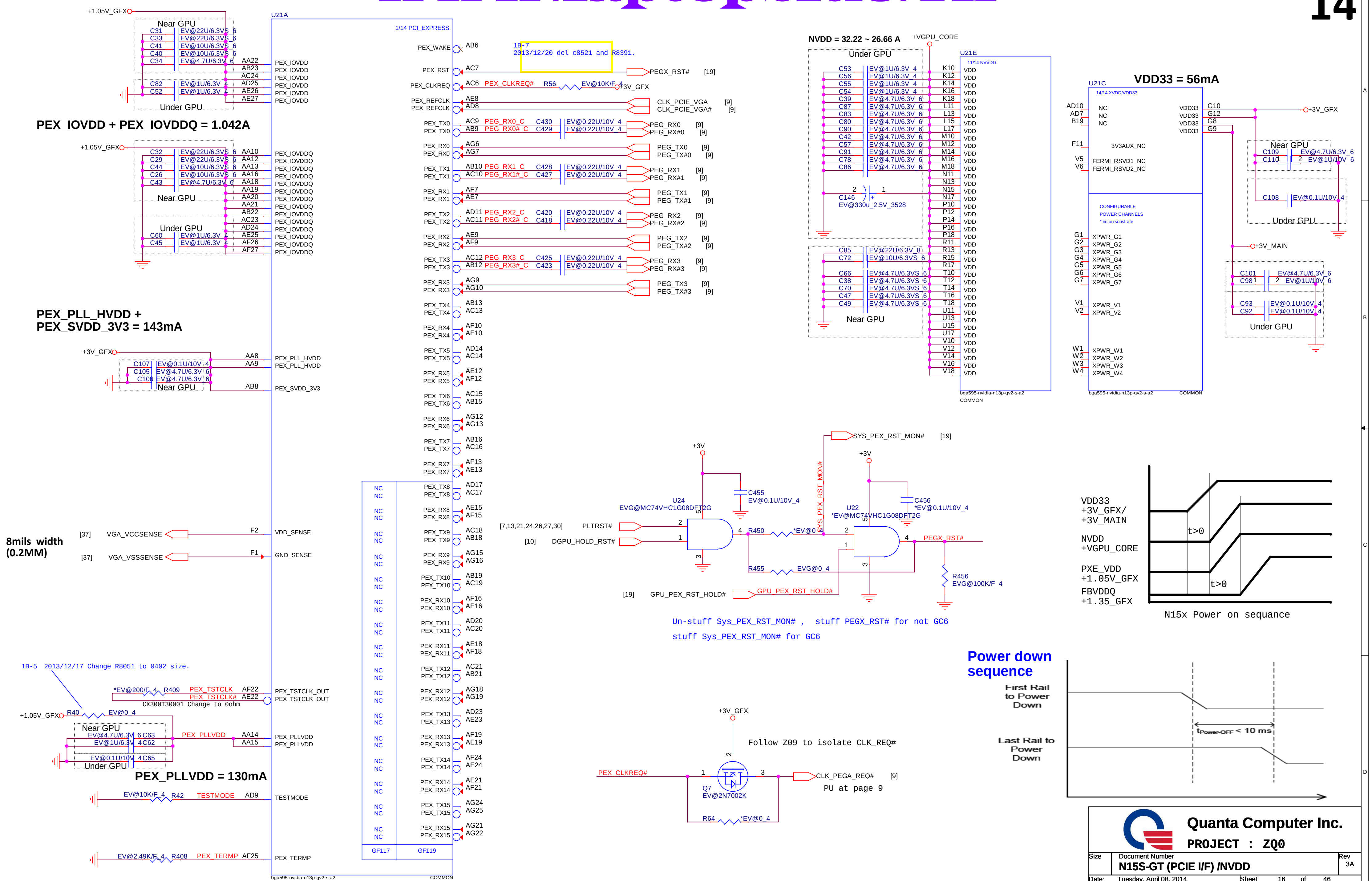
	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.

PROJECT : ZQ0

Size | Document Number: **DDRIII Memory SO-DIMM B** | Rev 3A

Date: Monday, April 07, 2014 | Sheet 15 of 46

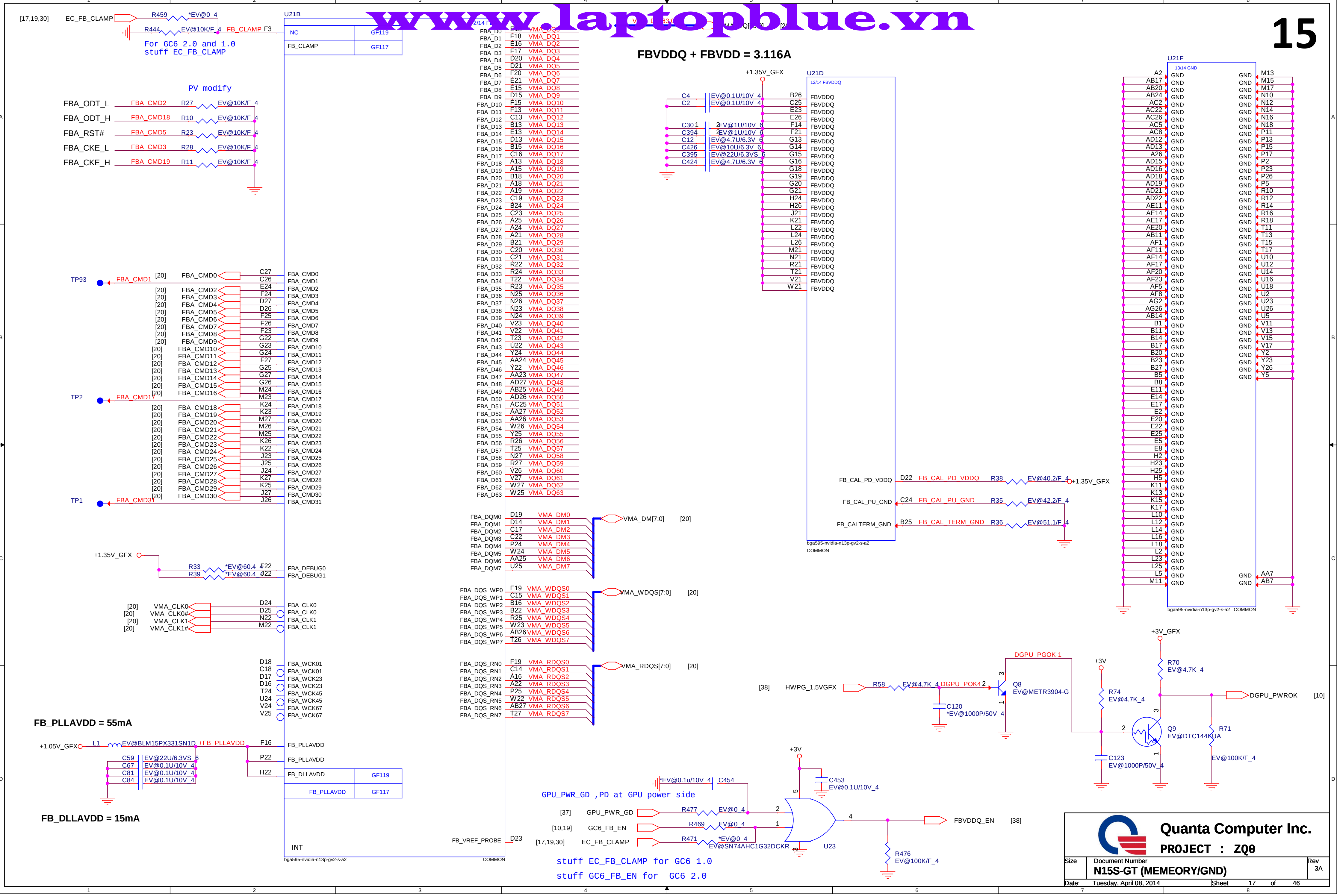


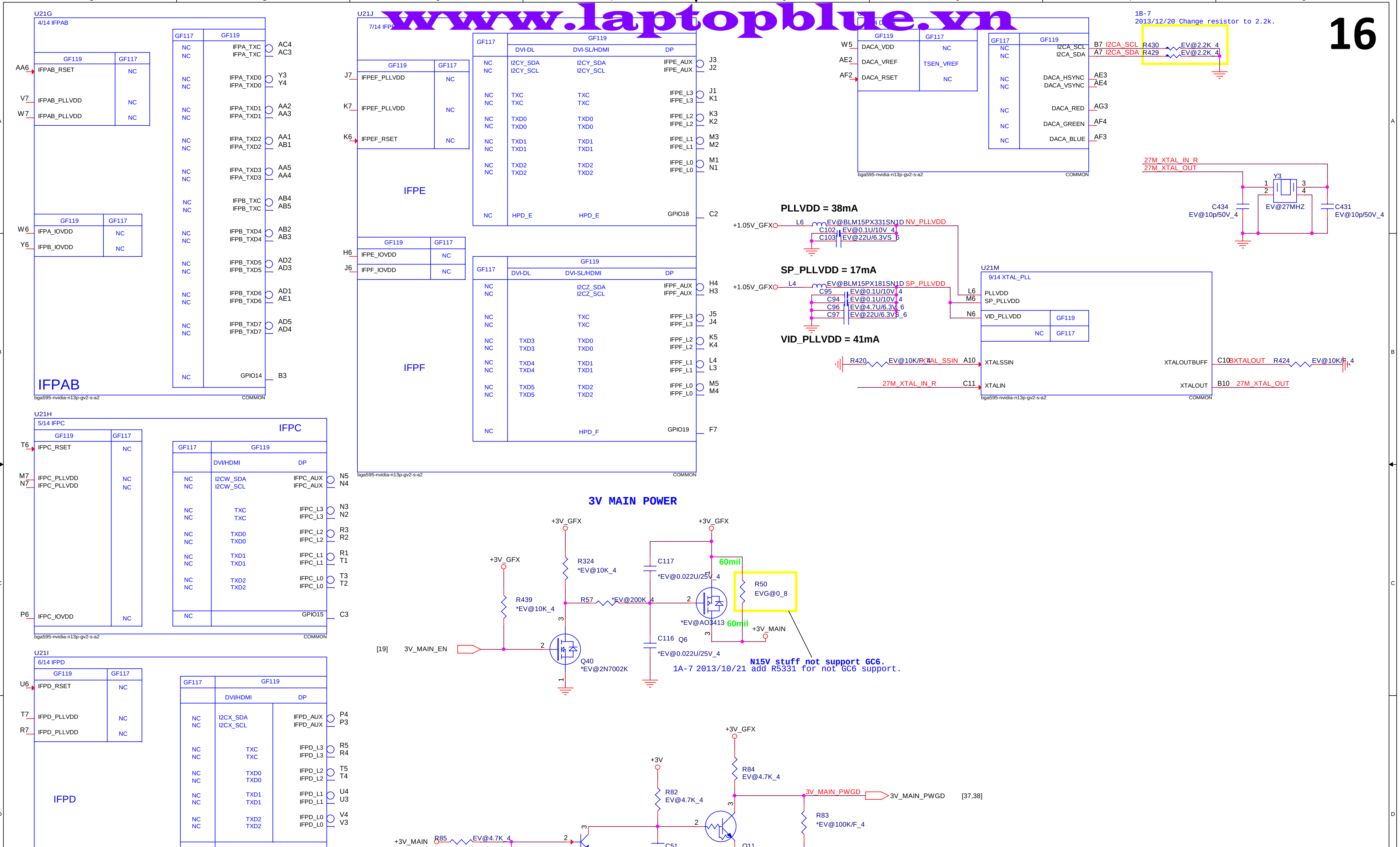
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	N15S-GT (PCIE I/F) /NVDD	3A

Date: Tuesday, April 08, 2014 Sheet 16 of 46


15
FBVDDQ + FBVDD = 3.116A
For GC6 2.0 and 1.0
stuff EC_FB_CLAMP
PV modify
FBA_ODT_L
FBA_ODT_H
FBA_RST#
FBA_CKE_L
FBA_CKE_H
U21B
U21D
U21F
+1.35V_GFX
+1.05V_GFX
+3V_GFX
FB_PLLAVDD = 55mA
FB_DLLAVDD = 15mA
VMA_DM[7:0]
VMA_WDQS[7:0]
VMA_RDQS[7:0]
DGPU_PGOK-1
HWPG_1.5VGFX
DGPU_PWROK
GPU_PWR_GD ,PD at GPU power side
GPU_PWR_GD
GC6_FB_EN
EC_FB_CLAMP
FBVDDQ_EN
stuff EC_FB_CLAMP for GC6 1.0
stuff GC6_FB_EN for GC6 2.0
Quanta Computer Inc.
PROJECT : ZQ0
Size
Document Number
N15S-GT (MEMEORY/GND)
Rev
3A
Date: Tuesday, April 08, 2014
Sheet 17 of 46

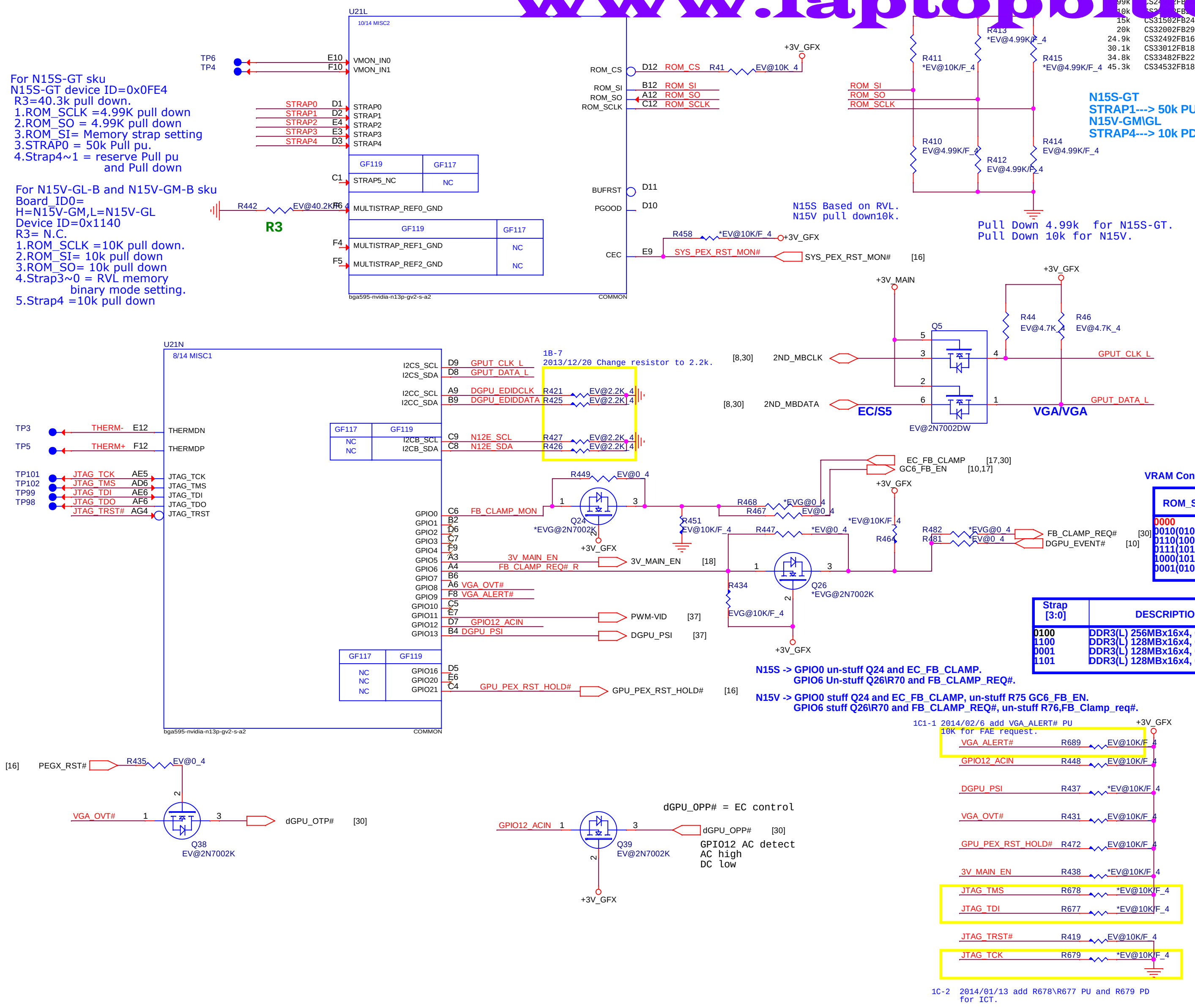


Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	N15S-GT (DISPALY)	3A

Date: Tuesday, April 08, 2014 Sheet 18 of 46



Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	STN P/N
0000	DDR3(L) 256MBx16x4, 64bit,1000MHz(	HYNIX	H5TC4G63AFR-11C	AKD5PGWTW05	AKD5PGWTW13
0010(0101)	DDR3(L) 256MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W4G1646D-BC1A		
0110(1001)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C		
0111(1010)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K		
1000(1011)	DDR3(L) 128MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W2G1646Q-BC1A		
0001(0100)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E		

Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N		Note
0100	DDR3(L) 256MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC4G63AFR-11C			
1100	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C			
0001	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K			
1101	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E			

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

GPIO ASSIGNMENTS

Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	N15S-GT (GPIO/STRAPS)	3A

Date: Monday, April 07, 2014 Sheet 19 of 46

MP-1 20140401 update Footprint like as ZQN.

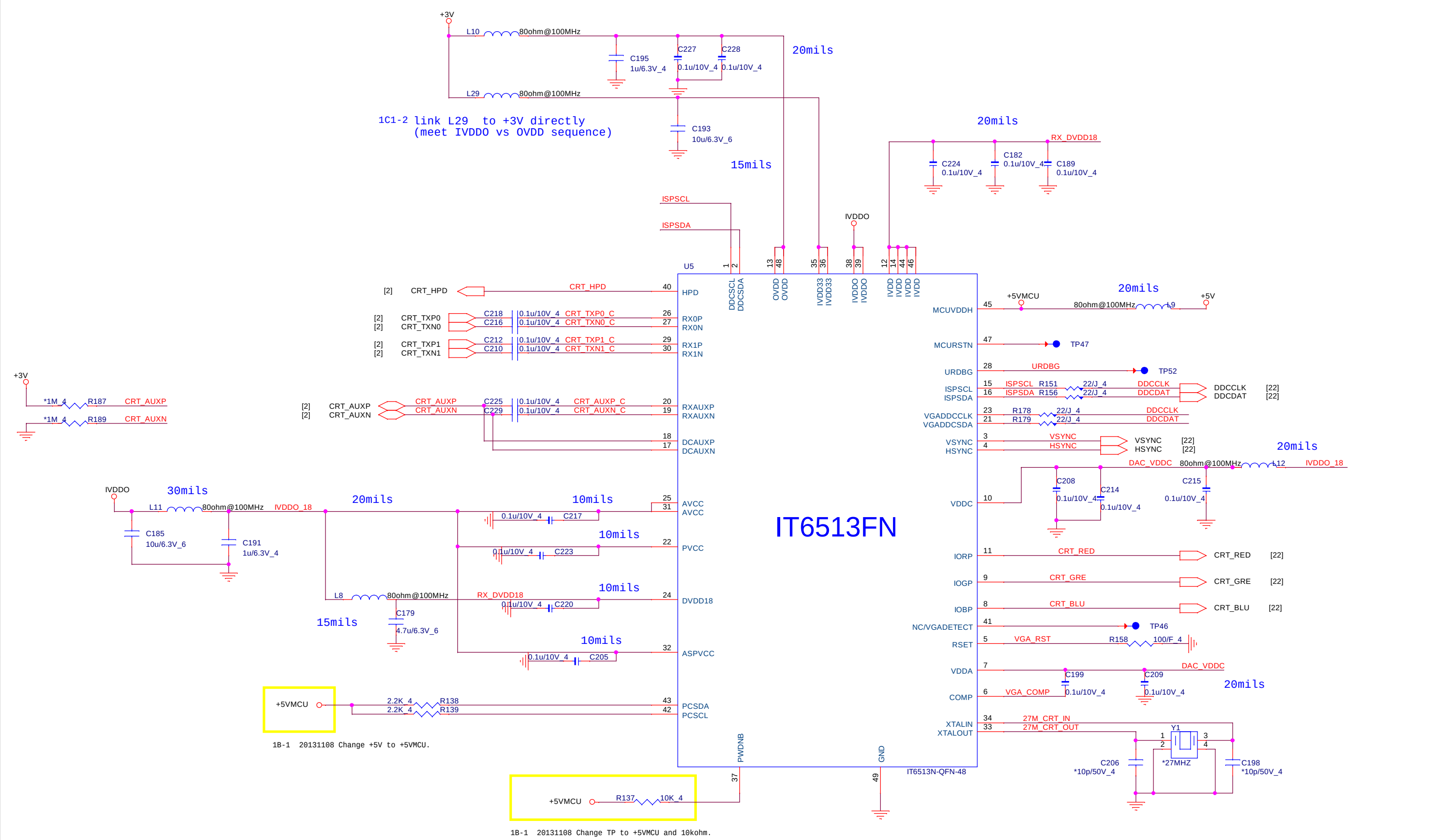
CHANNEL A: 256MB/512MB DDR3

HYN 256Mx16 PN: AKD5PGWTW08---AKD5PGWTW07
HYN 128Mx16 PN: AKD5MZDTW03---AKD5MZDTW02
SAM 256Mx16, PN：AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN：AKD5MGGT535---AKD5MGGT534

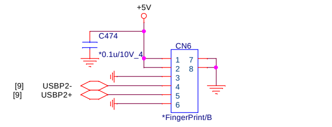
QBC TOP B/S

DP TO VGA

1A-1 2013/10/15 Change VGA ITE soltion to NXP.
1A-5 2013/10/18 Change VGA NXP soltion to ITE.

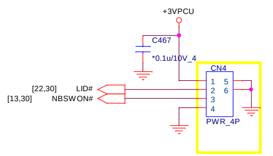


FingerPrint Conn



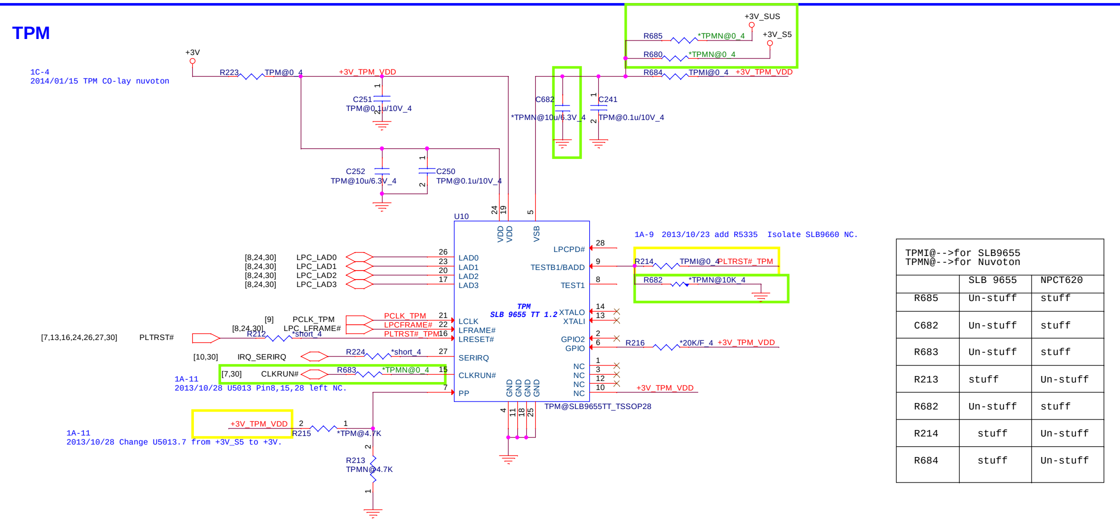
1A-7 2013/10/22 Change CN4 to 6pin.
1B-6 2013/12/18 Change CN5 USB port to port2.

Power Button/Conn



1A-1 2013/10/15 change to 6pin.
1B-2 2013/12/3 change to 4pin.
1B-3 2013/12/10 change CN6 footprint.

TPM



TPMI@-->for SLB9655
TPMN@-->for Nuvoton

	SLB 9655	NPCT620
R685	Un-stuff	stuff
C682	Un-stuff	stuff
R683	Un-stuff	stuff
R213	stuff	Un-stuff
R682	Un-stuff	stuff
R214	stuff	Un-stuff
R684	stuff	Un-stuff

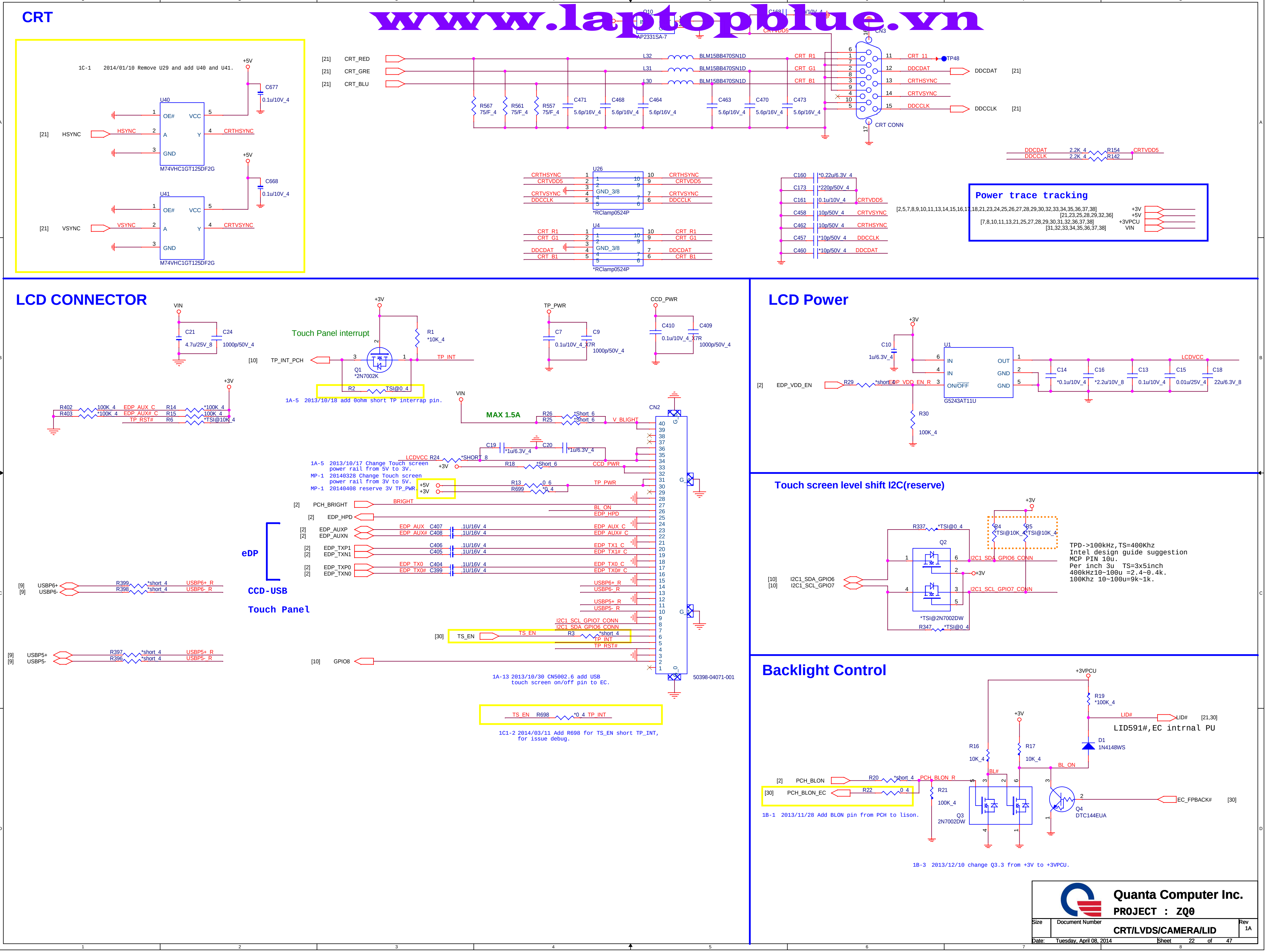
Green CLK Gen

1B-4 2013/12/13 remove Green GLK U9

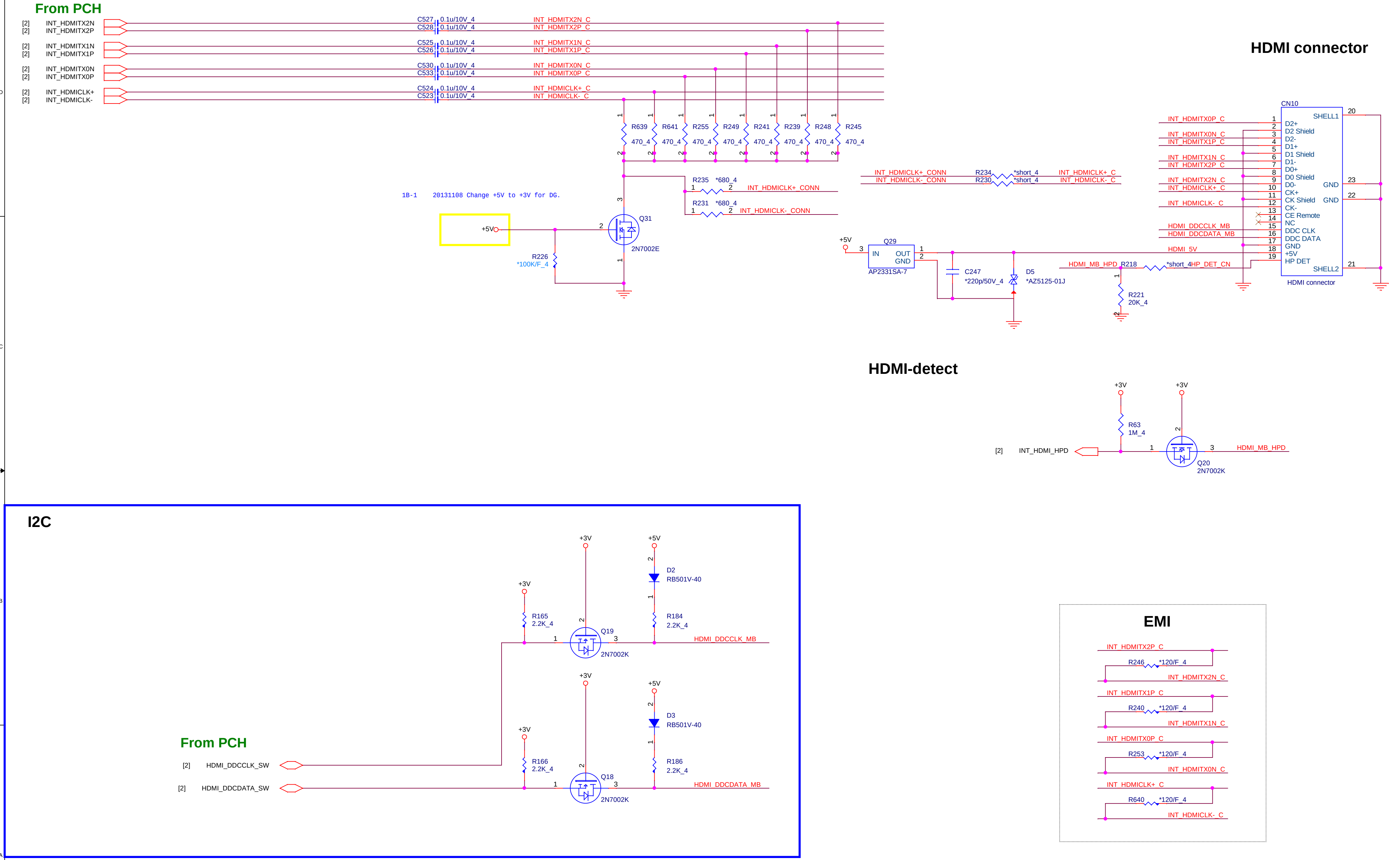
Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	Mini DP/HD3SS2521	3A

Date: Tuesday, April 08, 2014 Sheet 21 of 47


CRT
1C-1 2014/01/10 Remove U29 and add U40 and U41.
LCD CONNECTOR
Touch Panel interrupt
1A-5 2013/10/18 add 0ohm short TP interrap pin.
MAX 1.5A
1A-5 2013/10/17 Change Touch screen power rail from 5V to 3V.
MP-1 20140328 Change Touch screen power rail from 3V to 5V.
MP-1 20140408 reserve 3V TP_PWR.
eDP
CCD-USB
Touch Panel
1A-13 2013/10/30 CN5002.6 add USB touch screen on/off pin to EC.
1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.
LCD Power
Power trace tracking
Touch screen level shift I2C(reserve)
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.
Backlight Control
LID591#,EC intrnal PU
1B-1 2013/11/28 Add BLON pin from PCH to lison.
1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.
Quanta Computer Inc.
PROJECT : ZQ0
CRT/LVDS/CAMERA/LID
Rev 1A
Date: Tuesday, April 08, 2014
Sheet 22 of 47

HDMI



Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,21,22,24,25,26,27,28,29,30,32,33,34,35,36,37,38] +3V
[21,22,25,28,29,32,36] +5V

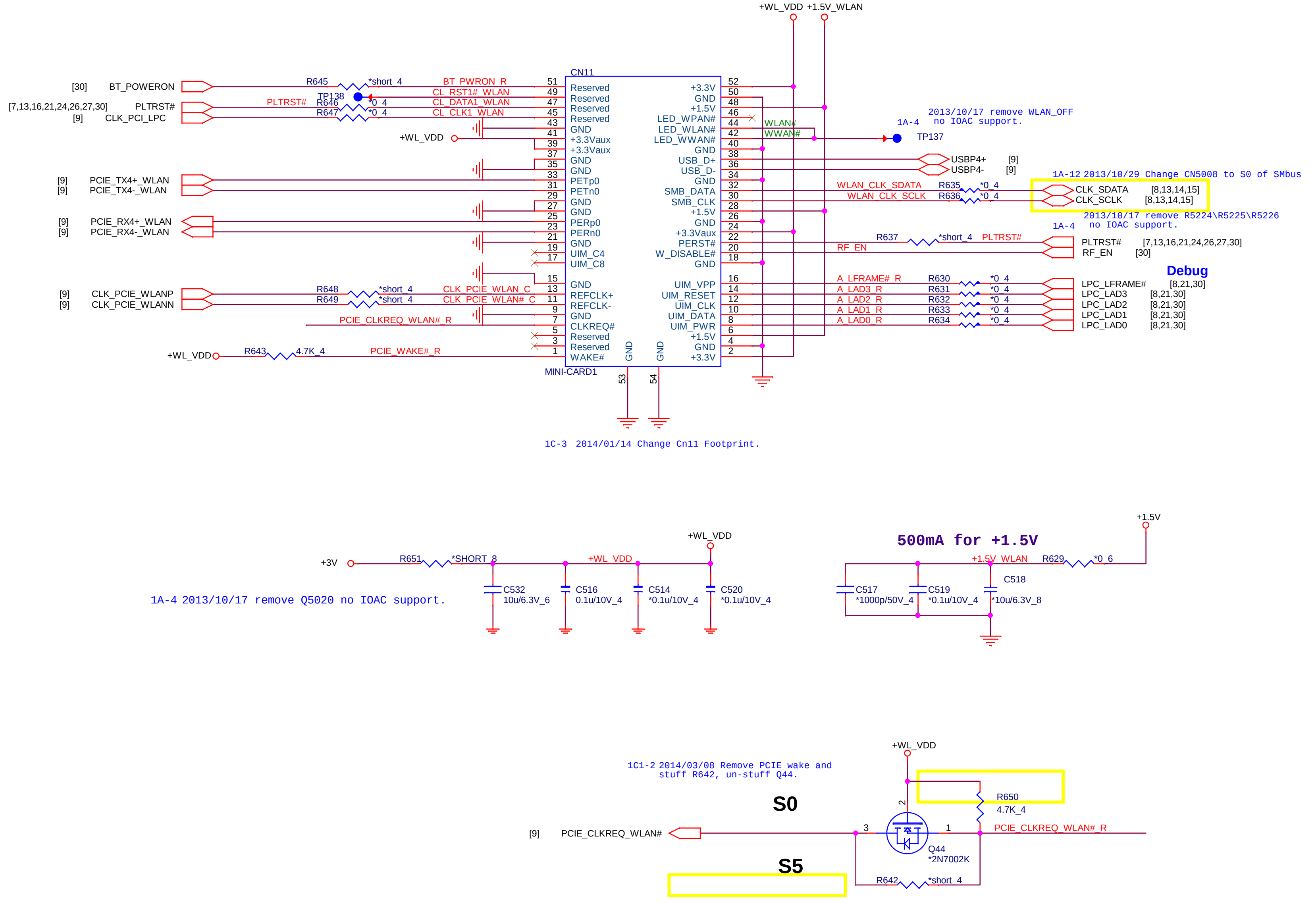
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	HDMI (PS8101)	1A

Date: Tuesday, April 08, 2014 Sheet 23 of 47

Mini Card 1 (MPC)

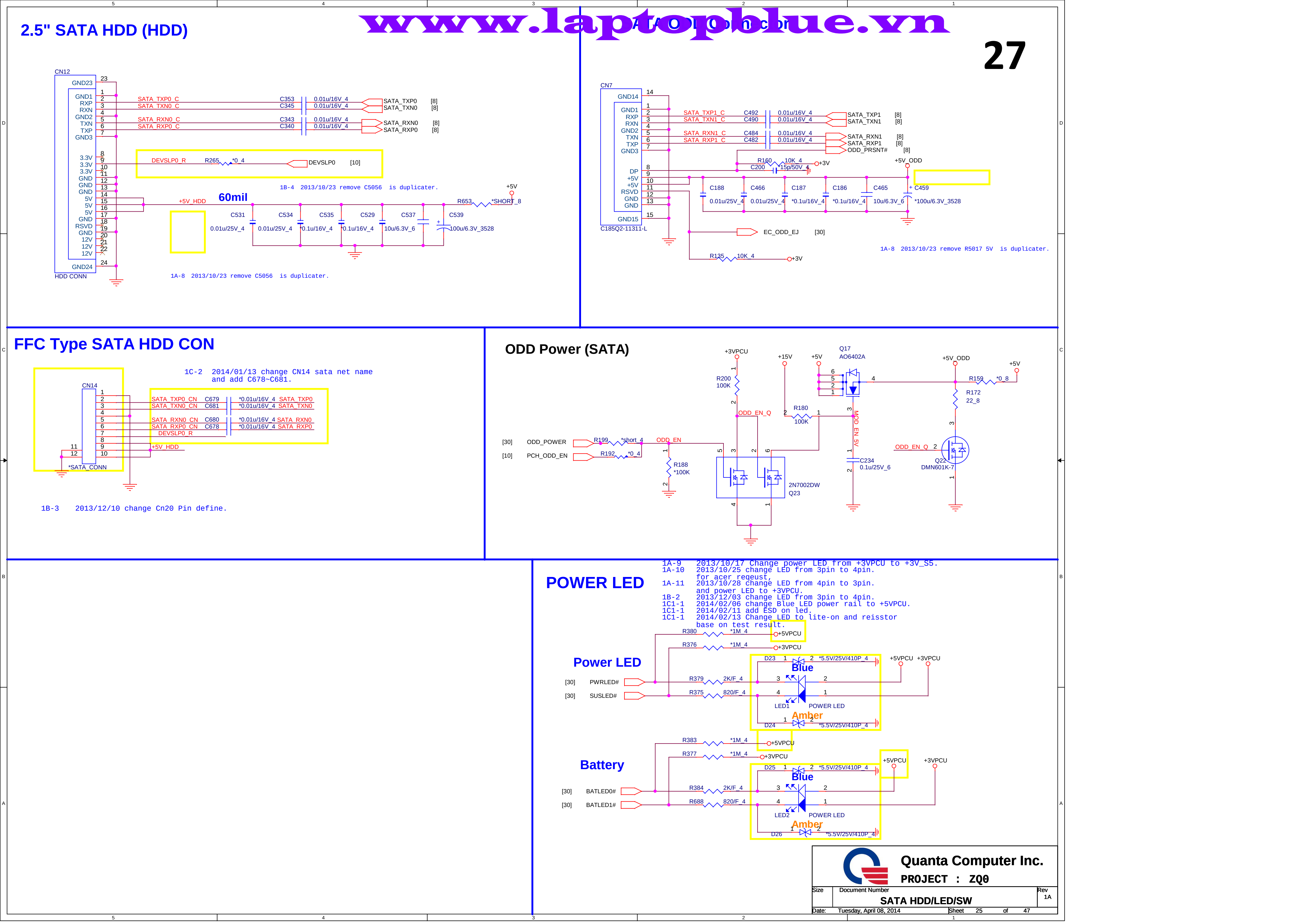


1A-4 2013/10/17 remove Q5019 no IOAC support.

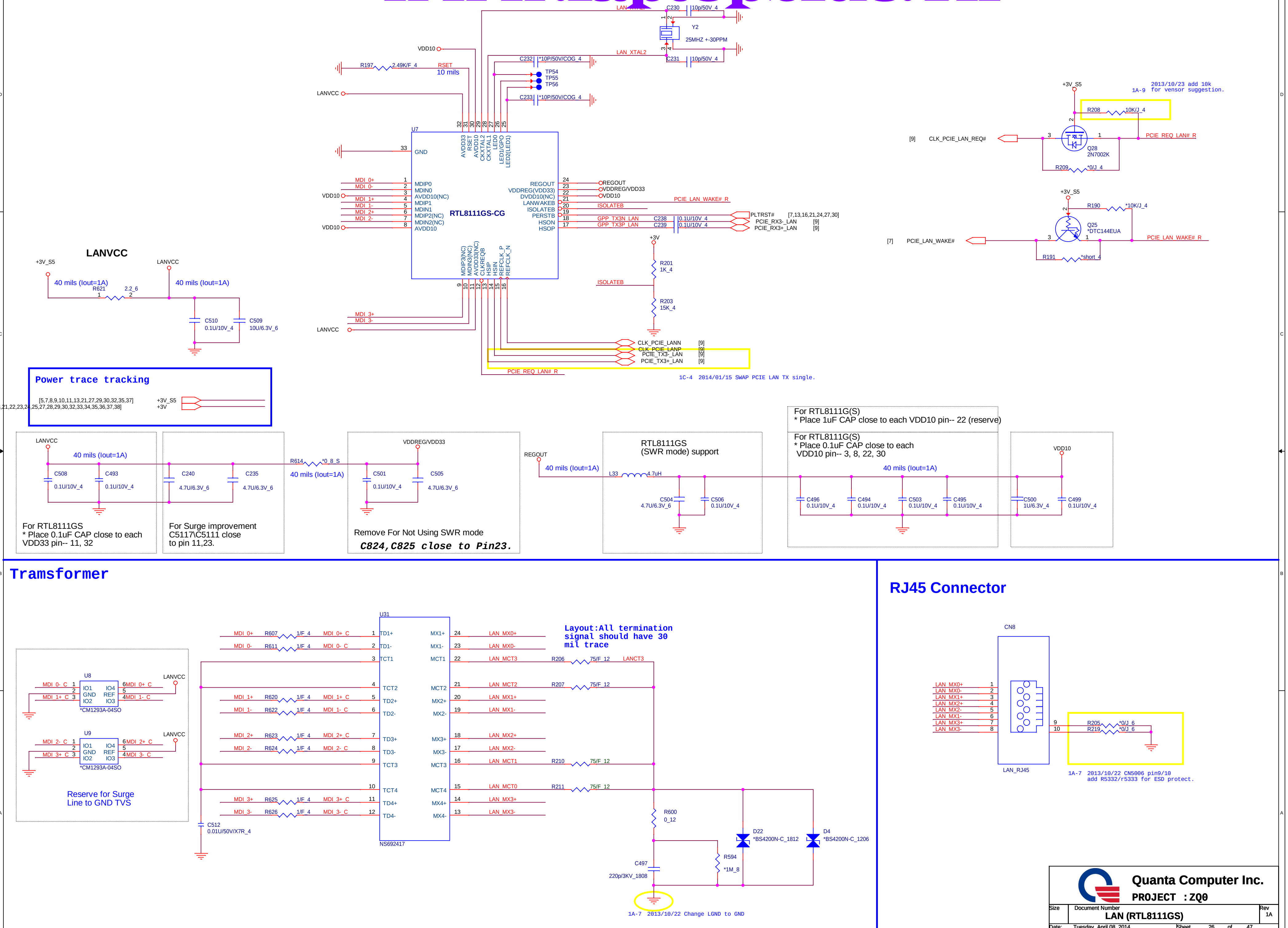
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date: Monday, April 07, 2014	Sheet 24 of 47	


www.laptopblue.vn
27
2.5" SATA HDD (HDD)
CN12
HDD CONN
SATA_TXP0_C
SATA_TXN0_C
SATA_RXN0_C
SATA_RXP0_C
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
DEVSLP0_R
DEVSLP0
+5V_HDD
60mil
1B-4 2013/10/23 remove C5056 is duplicater.
1A-8 2013/10/23 remove C5056 is duplicater.
ODD Connector
CN7
C185Q2-11311-L
SATA_TXP1_C
SATA_TXN1_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXP1
SATA_TXN1
SATA_RXN1
SATA_RXP1
ODD_PRSNT#
+5V_ODD
EC_ODD_EJ
1A-8 2013/10/23 remove R5017 5V is duplicater.
FFC Type SATA HDD CON
CN14
*SATA_CONN
1C-2 2014/01/13 change CN14 sata net name
and add C678~C681.
SATA_TXP0_CN
SATA_TXN0_CN
SATA_RXN0_CN
SATA_RXP0_CN
1B-3 2013/12/10 change Cn20 Pin define.
ODD Power (SATA)
ODD_POWER
PCH_ODD_EN
ODD_EN
ODD_EN_Q
MOD_EN_5V
2N7002DW
Q23
Q17
AO6402A
Q22
DMN601K-7
POWER LED
1A-9 2013/10/17 Change power LED from +3VPCU to +3V_S5.
1A-10 2013/10/25 change LED from 3pin to 4pin.
for acer reqeust,
1A-11 2013/10/28 change LED from 4pin to 3pin.
and power LED to +3VPCU.
1B-2 2013/12/03 change LED from 3pin to 4pin.
1C1-1 2014/02/06 change Blue LED power rail to +5VPCU.
1C1-1 2014/02/11 add ESD on led.
1C1-1 2014/02/13 Change LED to lite-on and reisstor
base on test result.
Power LED
PWRLED#
SUSLED#
Blue
Amber
LED1
POWER LED
Battery
BATLED0#
BATLED1#
LED2
Quanta Computer Inc.
PROJECT : ZQ0
Document Number
SATA HDD/LED/SW
Rev
1A
Date: Tuesday, April 08, 2014
Sheet 25 of 47

LAN



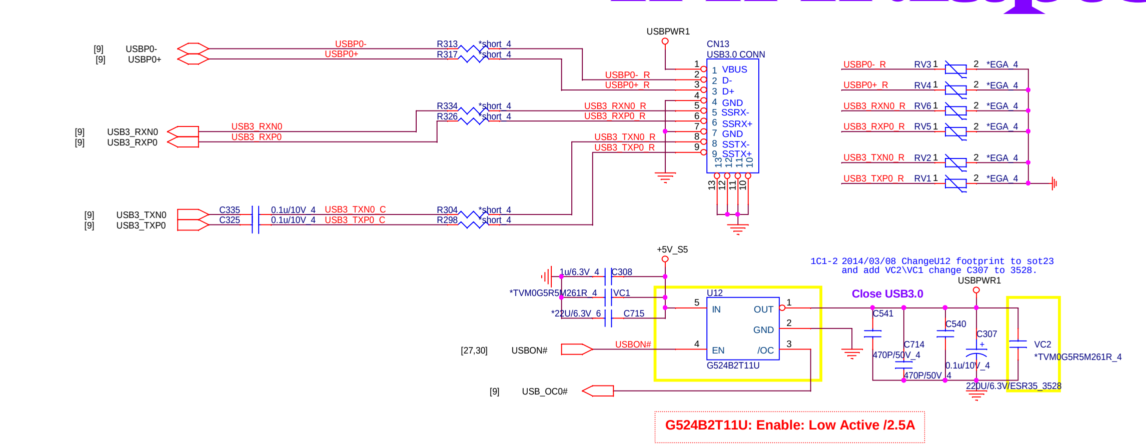
Quanta Computer Inc.

PROJECT : ZQ0

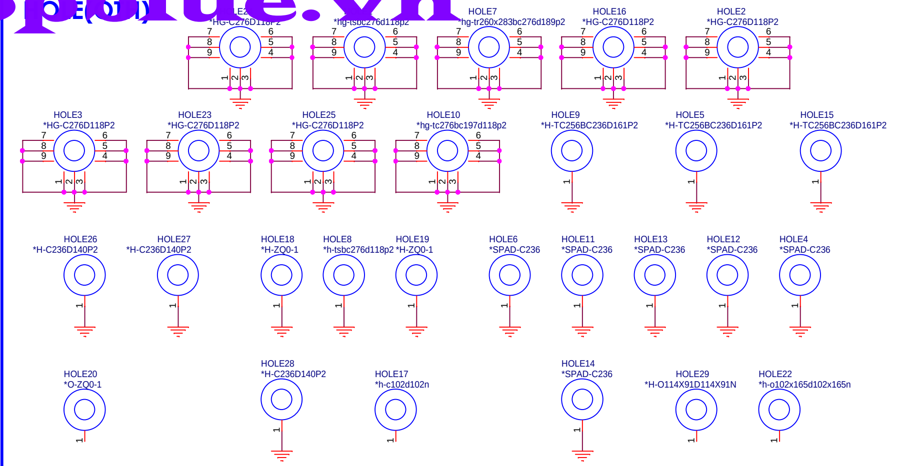
Size	Document Number	Rev
	LAN (RTL8111GS)	1A

Date: Tuesday, April 08, 2014 Sheet 26 of 47

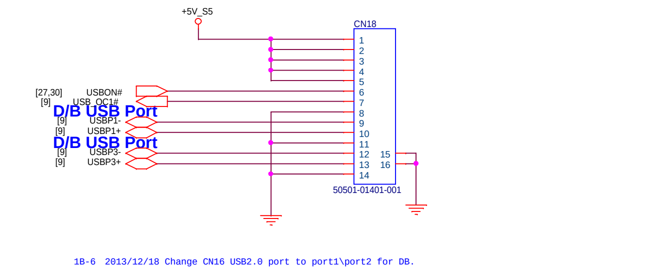
USB 3.0 Connector



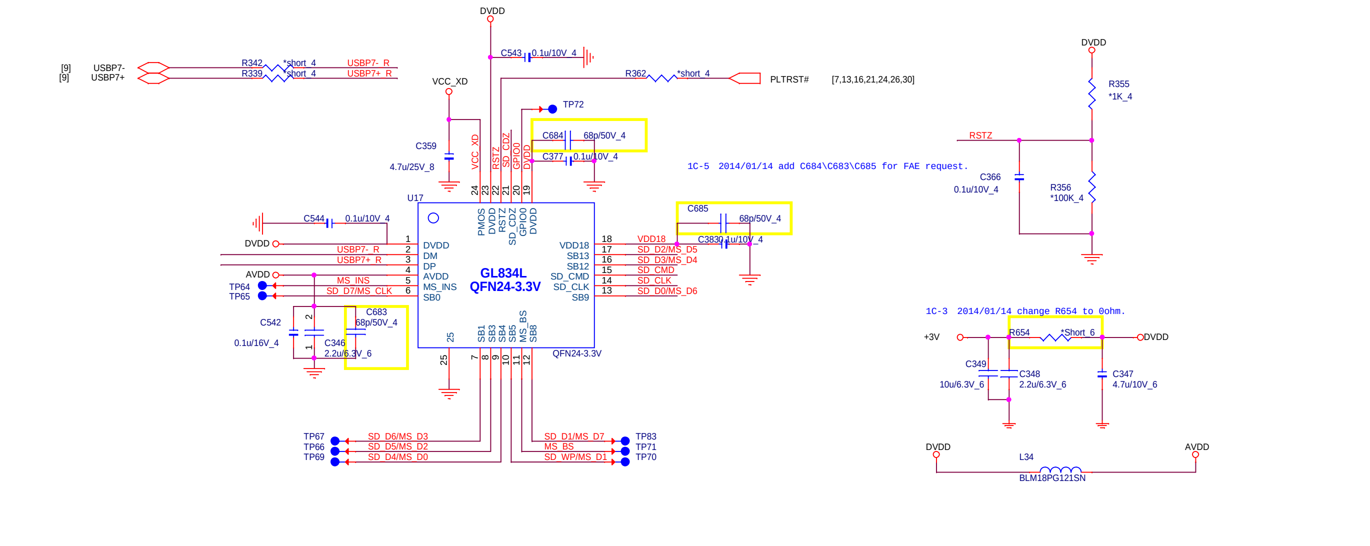
HOLE



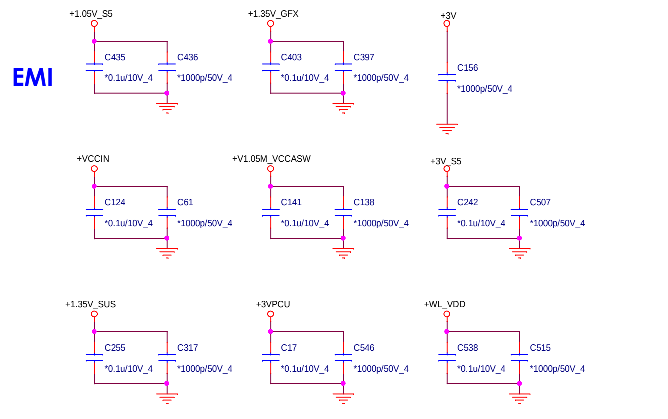
USB IO D/B



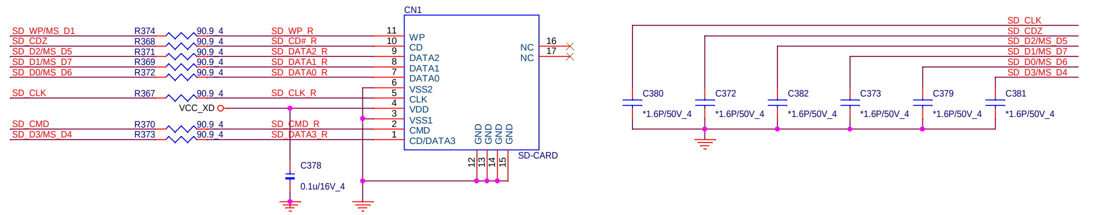
Card Reader and Connector



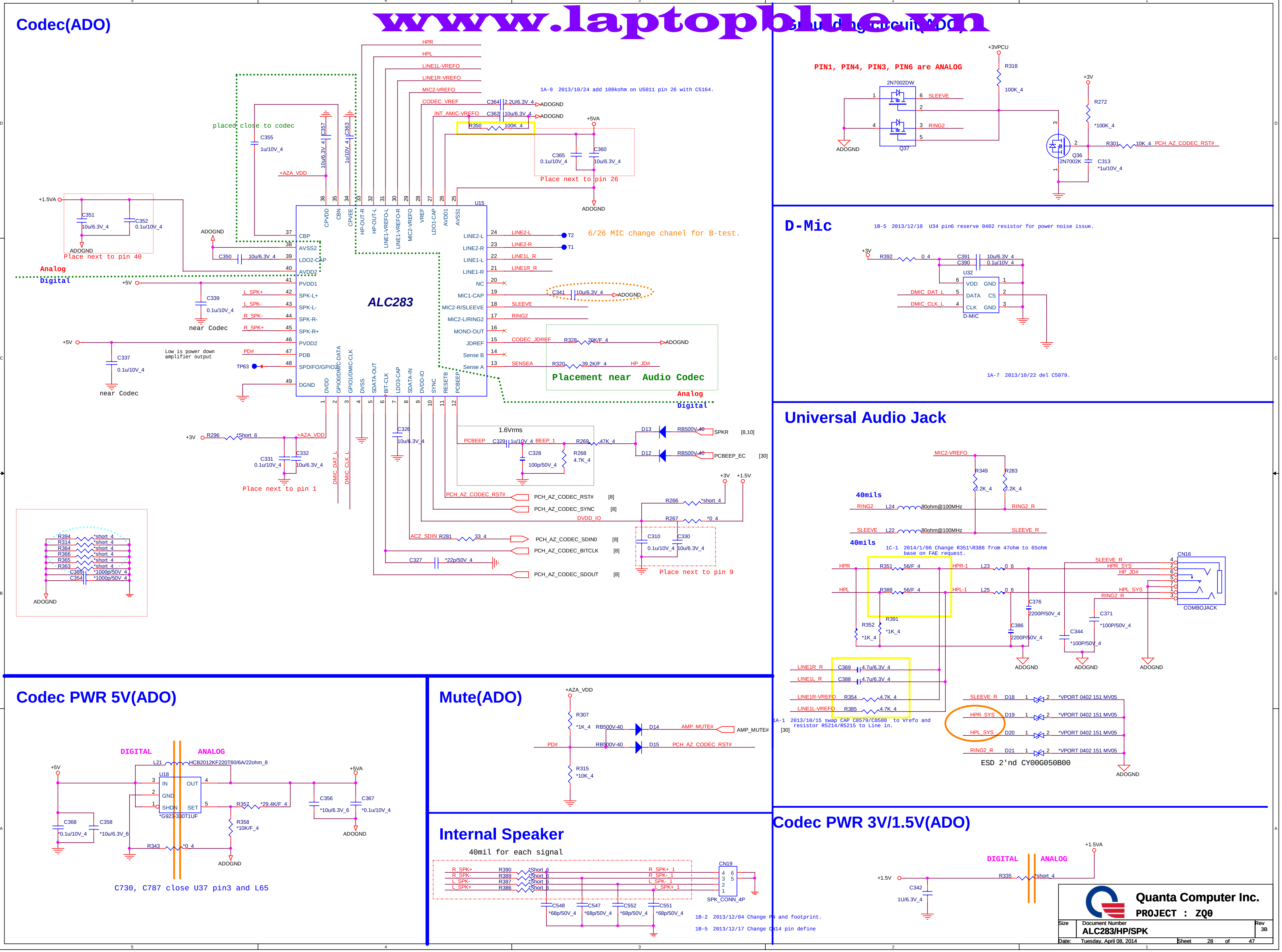
EMI



SD/MMC CARD READER (MMC)

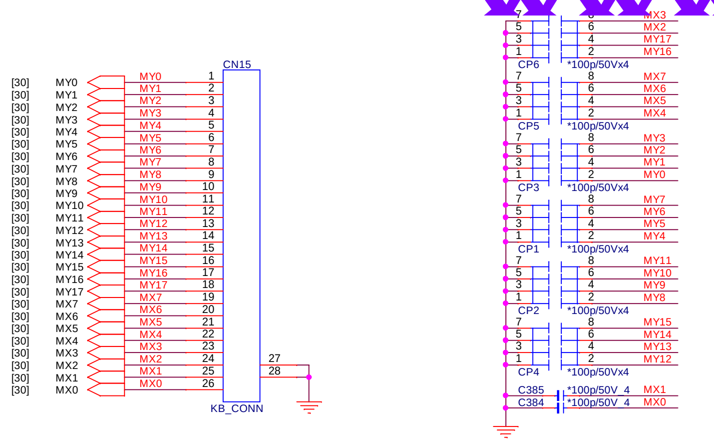


Quanta Computer Inc.	
PROJECT : ZQ0	
Size	Document Number: USB Port/ DB	Rev 1A
Date: Tuesday, April 08, 2014	Sheet 27 of 47



Codec(ADO)
ALC283
placed close to codec
Place next to pin 40
Place next to pin 26
Place next to pin 1
Place next to pin 9
6/26 MIC change chanel for B-test.
1A-9 2013/10/24 add 100kohm on U5011 pin 26 with C5164.
Placement near Audio Codec
Low is power down amplifier output
near Codec
Analog
Digital
1.6Vrms
Grounding circuit(ADO)
PIN1, PIN4, PIN3, PIN6 are ANALOG
D-Mic
1B-5 2013/12/18 U34 pin6 reserve 0402 resistor for power noise issue.
1A-7 2013/10/22 del C5079.
Universal Audio Jack
40mils
1C-1 2014/1/06 Change R351\R388 from 47ohm to 65ohm base on FAE request.
1A-1 2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.
ESD 2'nd CY00G050B00
COMBOJACK
Codec PWR 5V(ADO)
DIGITAL
ANALOG
C730, C787 close U37 pin3 and L65
Mute(ADO)
Internal Speaker
40mil for each signal
1B-2 2013/12/04 Change PN and footprint.
1B-5 2013/12/17 Change CN14 pin define
Codec PWR 3V/1.5V(ADO)
Quanta Computer Inc.
PROJECT : ZQ0
Document Number
ALC283/HP/SPK
Rev 3B
Date: Tuesday, April 08, 2014
Sheet 28 of 47

K/B (KBC)



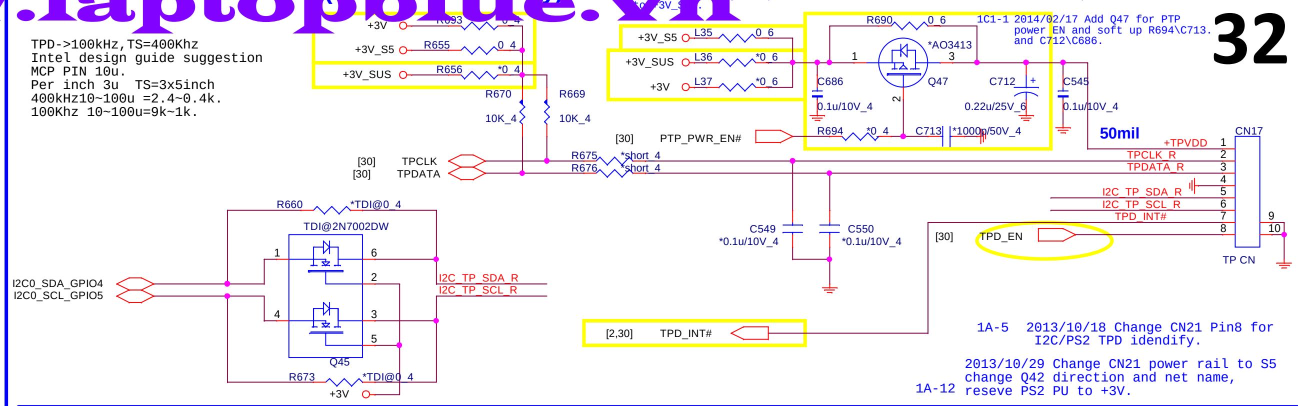
1A-7 2013/10/22 change CN24 pin define based on spec.
1A-8 2013/10/22 change CN24 pin define based on spec based on ZRQ.

TOUCHPAD BOARD CONN (TP I2C/PS2 co-lay)

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

1C-1 2014/01/15 change TP power rail from +3V_S5. 1C-4 2014/01/15 reserve TP power rail +3V_S5.

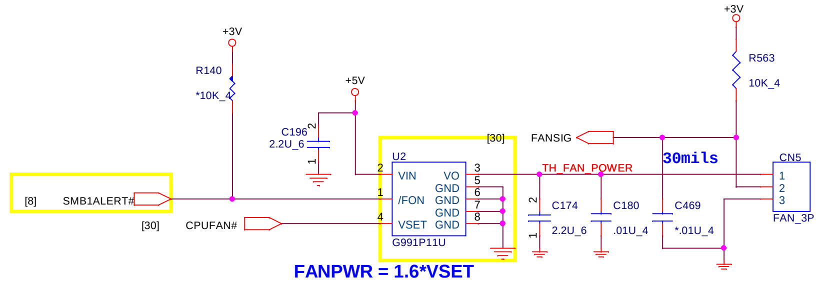
1C1-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.



1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

1A-12 2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name, reseve PS2 PU to +3V.

CPU FAN (THM)



FANPWR = 1.6*VSET

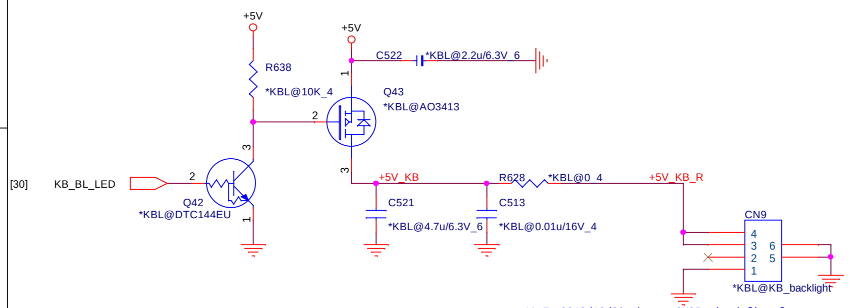
1A-12013/10/15 change pin define and add pwm IC U17.

1A-42013/10/17 Change U17 to G991P11U and PU U17 pin1.

1A-92013/10/24 Add alert on U17.1 for CPU themal tempture.

1A-13 2013/10/31CN15 Pin2/3 swap.

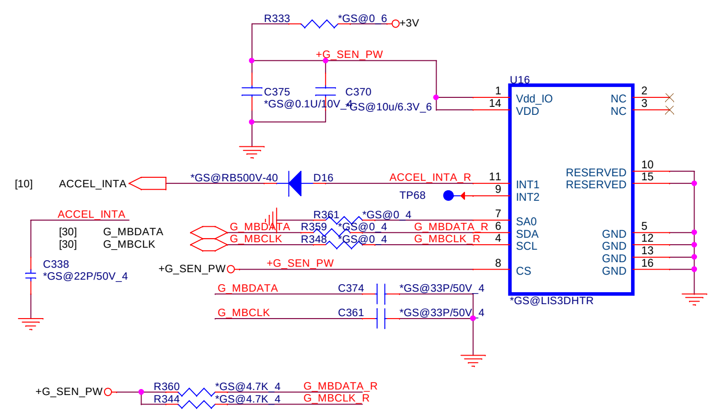
KB_BL LED (KBC)



1A-7 2013/10/22 change CN25 pin define for spec.

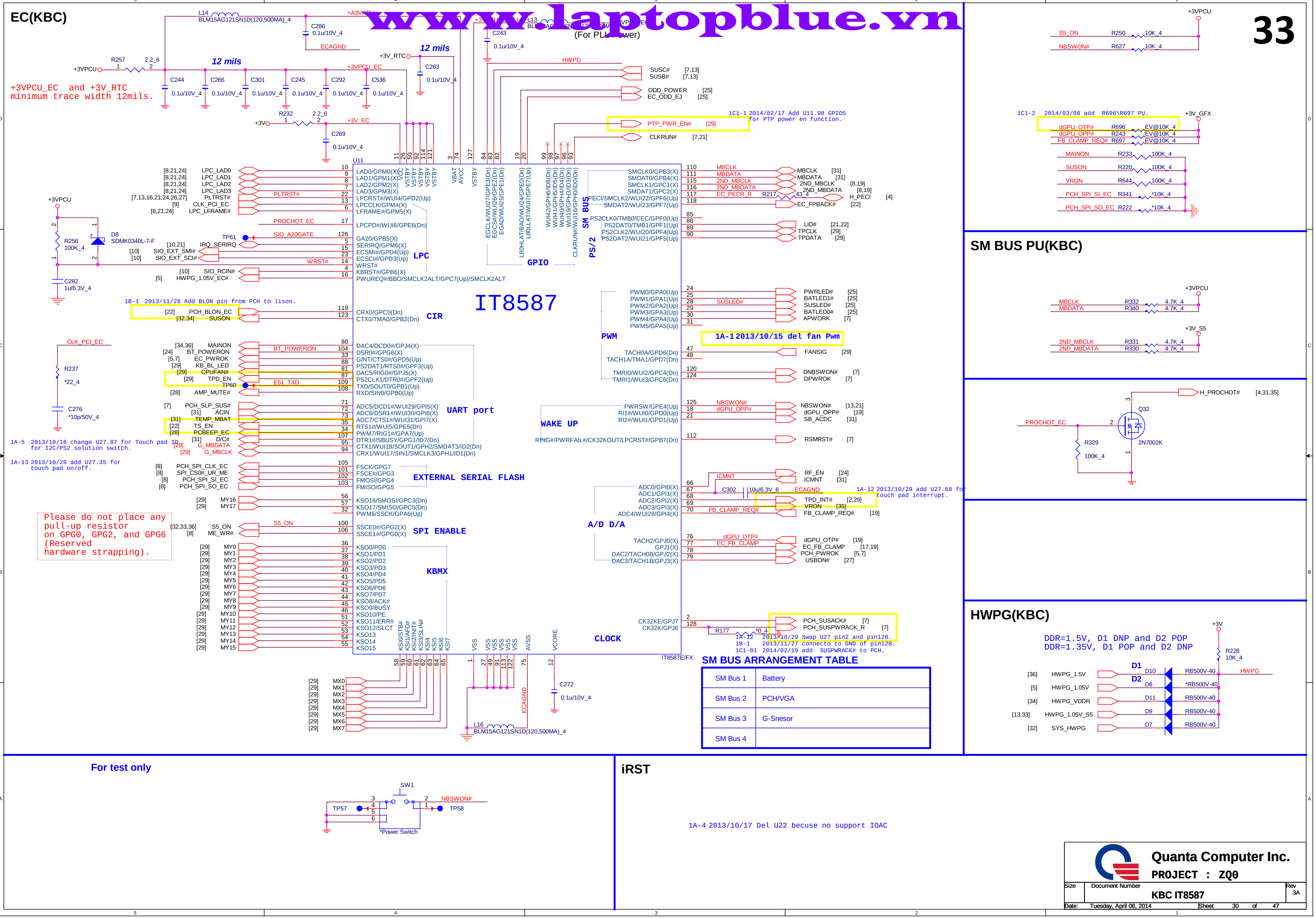
1A-8 2013/10/23 change CN25 footprint.

Accelerometer Sensor(reserve only)



Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: KB/TP/FAN	Rev: 3A
Date: Tuesday, April 08, 2014	Sheet 29 of 47	

EC(KBC)



SM BUS ARRANGEMENT TABLE

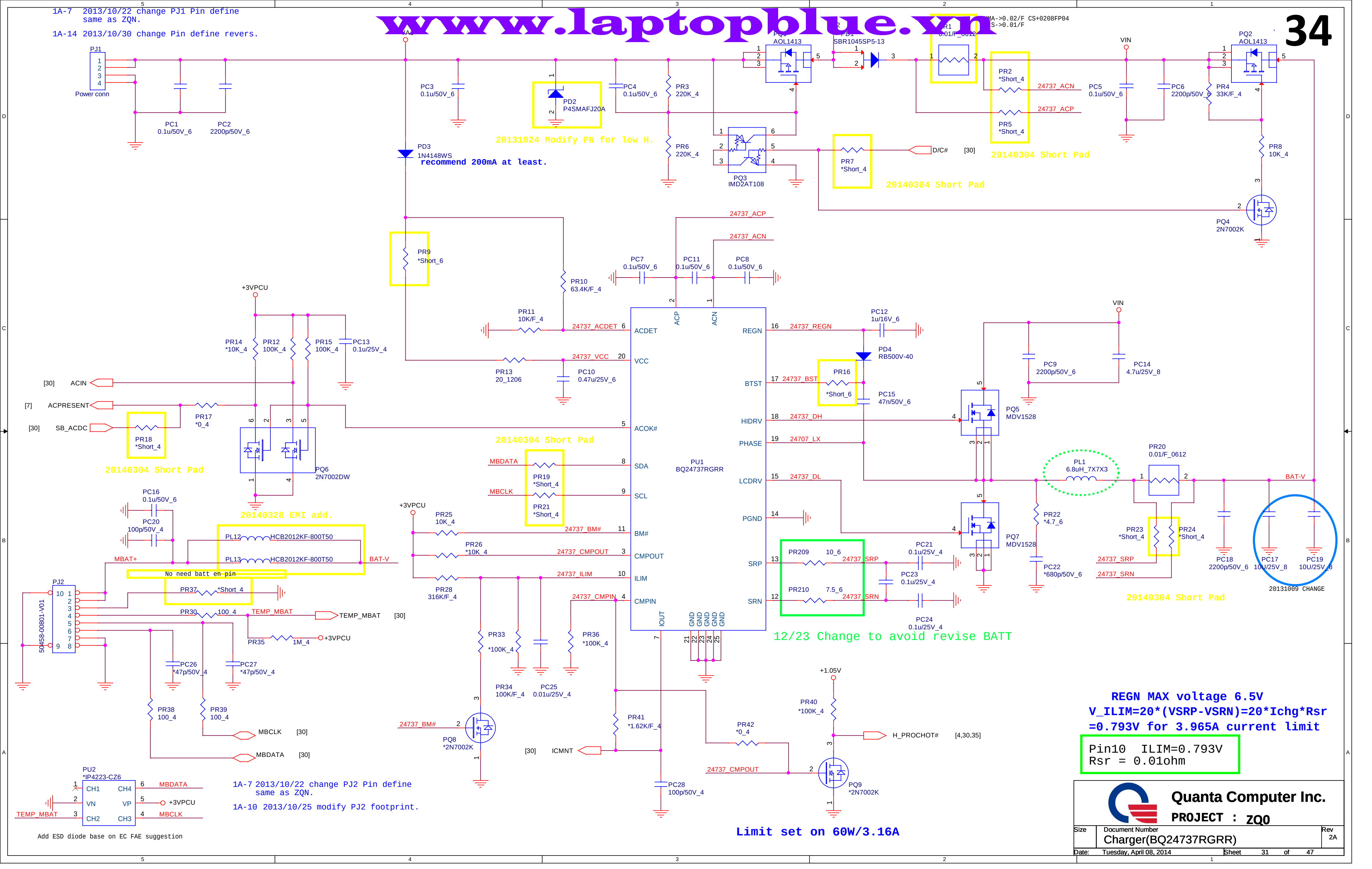
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	G-Snesor
SM Bus 4	

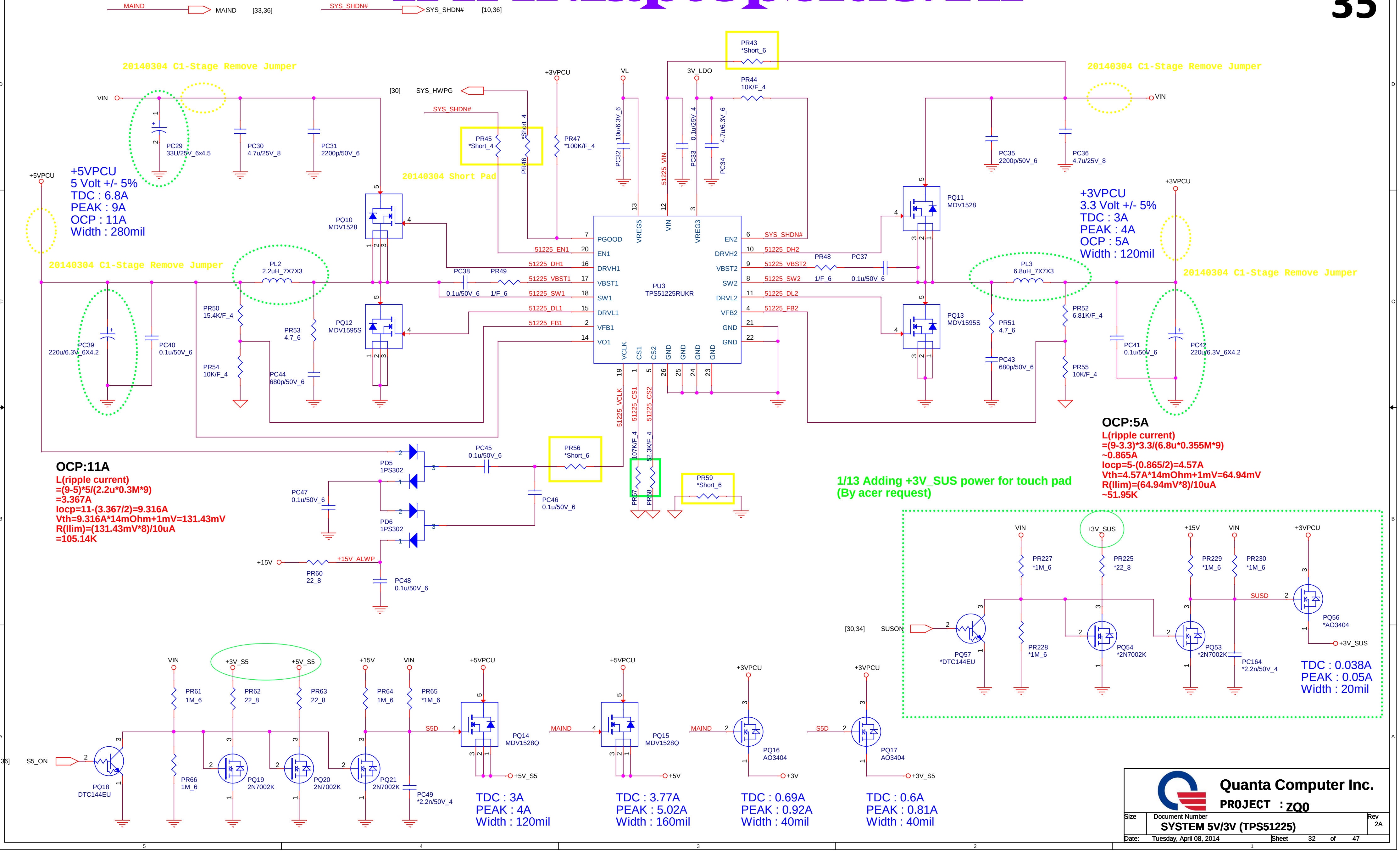
Quanta Computer Inc.

PROJECT : ZQ0

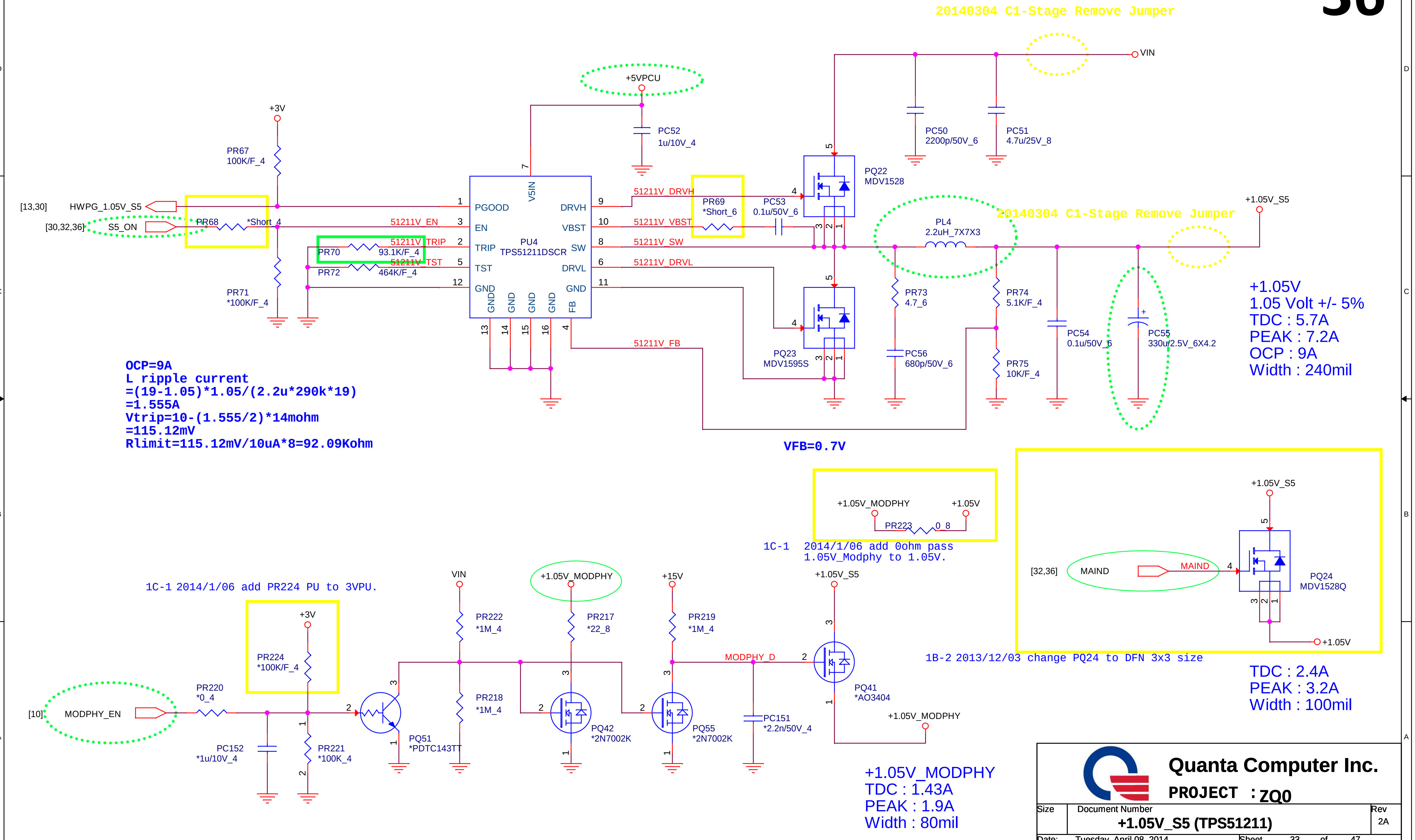
Size	Document Number	Rev
	KBC IT8587	3A

Date: Tuesday, April 08, 2014 Sheet 30 of 47


34
www.laptopblue.vn
1A-7 2013/10/22 change PJ1 Pin define
same as ZQN.
1A-14 2013/10/30 change Pin define revers.
PJ1
Power conn
PC1 0.1u/50V_6
PC2 2200p/50V_6
PC3 0.1u/50V_6
PD2 P4SMAFJ20A
20131024 Modify PN for low H.
PD3 1N4148WS
recommend 200mA at least.
PC4 0.1u/50V_6
PR3 220K_4
PR6 220K_4
PQ3 IMD2AT108
PQ1 AOL1413
PD1 SBR1045SP5-13
PR1 0.01/F_0612
PR2 *Short_4
PR5 *Short_4
24737_ACN
24737_ACP
20140304 Short Pad
PR7 *Short_4
D/C# [30]
PC5 0.1u/50V_6
PC6 2200p/50V_6
VIN
PQ2 AOL1413
PR4 33K/F_4
PR8 10K_4
PQ4 2N7002K
PR9 *Short_6
PR10 63.4K/F_4
PC7 0.1u/50V_6
PC11 0.1u/50V_6
PC8 0.1u/50V_6
+3VPCU
PR14 *10K_4
PR12 100K_4
PR15 100K_4
PC13 0.1u/25V_4
PR11 10K/F_4
24737_ACDET
PR13 20_1206
24737_VCC
PC10 0.47u/25V_6
[30] ACIN
[7] ACPRESENT
[30] SB_ACDC
PR17 *0_4
PR18 *Short_4
PQ6 2N7002DW
PC16 0.1u/50V_6
PC20 100p/50V_4
20140328 EMI add.
PL12 HCB2012KF-800T50
PL13 HCB2012KF-800T50
MBAT+
BAT-V
No need batt en pin
PJ2
50458-00801-V01
PR37 *Short_4
PR30 100_4
TEMP_MBAT
TEMP_MBAT [30]
PR35 1M_4 +3VPCU
PC26 *47p/50V_4
PC27 *47p/50V_4
PR38 100_4
PR39 100_4
MBCLK [30]
MBDATA [30]
PU2 *IP4223-CZ6
CH1 CH4 VN VP CH2 CH3
MBDATA +3VPCU MBCLK
Add ESD diode base on EC FAE suggestion
1A-7 2013/10/22 change PJ2 Pin define
same as ZQN.
1A-10 2013/10/25 modify PJ2 footprint.
PU1 BQ24737RGRR
ACDET VCC ACOK# SDA SCL BM# CMPOUT ILIM CMPIN ACP ACN REGN BTST HIDRV PHASE LCDRV PGND SRP SRN IOUT GND
PR19 *Short_4
PR21 *Short_4
MBDATA MBCLK
PR25 10K_4
PR26 *10K_4
PR28 316K/F_4
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
PR33 *100K_4
PR34 100K/F_4
PC25 0.01u/25V_4
PR36 *100K_4
PQ8 *2N7002K
[30] ICMNT
PR41 *1.62K/F_4
PC28 100p/50V_4
24737_REGN
PC12 1u/16V_6
PD4 RB500V-40
PR16 *Short_6
24737_BST
PC15 47n/50V_6
24737_DH
24707_LX
24737_DL
PQ5 MDV1528
PQ7 MDV1528
PC9 2200p/50V_6
PC14 4.7u/25V_8
PL1 6.8uH_7X7X3
PR20 0.01/F_0612
PR22 *4.7_6
PC22 *680p/50V_6
PR209 10_6
PR210 7.5_6
24737_SRP
24737_SRN
PC21 0.1u/25V_4
PC23 0.1u/25V_4
PC24 0.1u/25V_4
12/23 Change to avoid revise BATT
PR23 *Short_4
PR24 *Short_4
PC18 2200p/50V_6
PC17 10U/25V_8
PC19 10U/25V_8
20131009 CHANGE
+1.05V
PR40 *100K_4
PR42 *0_4
H_PROCHOT# [4,30,35]
PQ9 *2N7002K
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Limit set on 60W/3.16A
Quanta Computer Inc.
PROJECT : ZQ0
Size Document Number Rev
Charger(BQ24737RGRR) 2A
Date: Tuesday, April 08, 2014 Sheet 31 of 47



MAIND
MAIND [33,36]
SYS_SHDN#
SYS_SHDN# [10,36]
20140304 C1-Stage Remove Jumper
20140304 C1-Stage Remove Jumper
20140304 C1-Stage Remove Jumper
20140304 C1-Stage Remove Jumper
20140304 Short Pad
PR43 *Short_6
PR44 10K/F_4
PR45 *Short_4
PR46 *Short_4
PR47 *100K/F_4
VIN
+3VPCU
VL
3V_LDO
[30] SYS_HWPG
PC29 33U/25V_6x4.5
PC30 4.7u/25V_8
PC31 2200p/50V_6
PC32 10u/6.3V_6
PC33 0.1u/25V_4
PC34 4.7u/6.3V_6
PC35 2200p/50V_6
PC36 4.7u/25V_8
+5VPCU
5 Volt +/- 5%
TDC : 6.8A
PEAK : 9A
OCP : 11A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil
PQ10 MDV1528
PQ11 MDV1528
PQ12 MDV1595S
PQ13 MDV1595S
PL2 2.2uH_7X7X3
PL3 6.8uH_7X7X3
PU3 TPS51225RUKR
PGOOD EN1 DRVH1 VBST1 SW1 DRVL1 VFB1 VO1
EN2 DRVH2 VBST2 SW2 DRVL2 VFB2 GND GND
VREG5 VIN VREG3 VCLK CS1 CS2 GND GND GND GND
51225_EN1 51225_DH1 51225_VBST1 51225_SW1 51225_DL1 51225_FB1
51225_DH2 51225_VBST2 51225_SW2 51225_DL2 51225_FB2
51225_VIN 51225_VCLK 51225_CS1 51225_CS2
PC38 0.1u/50V_6
PR49 1/F_6
PR48 1/F_6
PC37 0.1u/50V_6
PC39 220u/6.3V_6X4.2
PC40 0.1u/50V_6
PR50 15.4K/F_4
PR53 4.7_6
PR54 10K/F_4
PC44 680p/50V_6
PR51 4.7_6
PR52 6.81K/F_4
PC43 680p/50V_6
PR55 10K/F_4
PC41 0.1u/50V_6
PC42 220u/6.3V_6X4.2
PD5 1PS302
PD6 1PS302
PC45 0.1u/50V_6
PC46 0.1u/50V_6
PC47 0.1u/50V_6
PR56 *Short_6
PR57 107K/F_4
PR58 52.3K/F_4
PR59 *Short_6
+15V PR60 22_8 +15V_ALWP
PC48 0.1u/50V_6
OCP:11A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=11-(3.367/2)=9.316A
Vth=9.316A*14mOhm+1mV=131.43mV
R(Ilim)=(131.43mV*8)/10uA
=105.14K
OCP:5A
L(ripple current)
=(9-3.3)*3.3/(6.8u*0.355M*9)
~0.865A
Iocp=5-(0.865/2)=4.57A
Vth=4.57A*14mOhm+1mV=64.94mV
R(Ilim)=(64.94mV*8)/10uA
~51.95K
1/13 Adding +3V_SUS power for touch pad
(By acer request)
VIN +3V_SUS +15V VIN +3VPCU
PR227 *1M_6
PR225 *22_8
PR229 *1M_6
PR230 *1M_6
PR228 *1M_6
[30,34] SUSON
PQ57 *DTC144EU
PQ54 *2N7002K
PQ53 *2N7002K
PC164 *2.2n/50V_4
SUSD
PQ56 *AO3404
+3V_SUS
TDC : 0.038A
PEAK : 0.05A
Width : 20mil
VIN +3V_S5 +5V_S5 +15V VIN +5VPCU +5VPCU +3VPCU +3VPCU
PR61 1M_6
PR62 22_8
PR63 22_8
PR64 1M_6
PR65 *1M_6
PR66 1M_6
S5_ON
PQ18 DTC144EU
PQ19 2N7002K
PQ20 2N7002K
PQ21 2N7002K
PC49 *2.2n/50V_4
S5D
PQ14 MDV1528Q
MAIND
PQ15 MDV1528Q
MAIND
PQ16 AO3404
S5D
PQ17 AO3404
+5V_S5
+5V
+3V
+3V_S5
TDC : 3A
PEAK : 4A
Width : 120mil
TDC : 3.77A
PEAK : 5.02A
Width : 160mil
TDC : 0.69A
PEAK : 0.92A
Width : 40mil
TDC : 0.6A
PEAK : 0.81A
Width : 40mil
Quanta Computer Inc.
PROJECT : ZQ0
Size
Document Number
SYSTEM 5V/3V (TPS51225)
Rev 2A
Date: Tuesday, April 08, 2014
Sheet 32 of 47

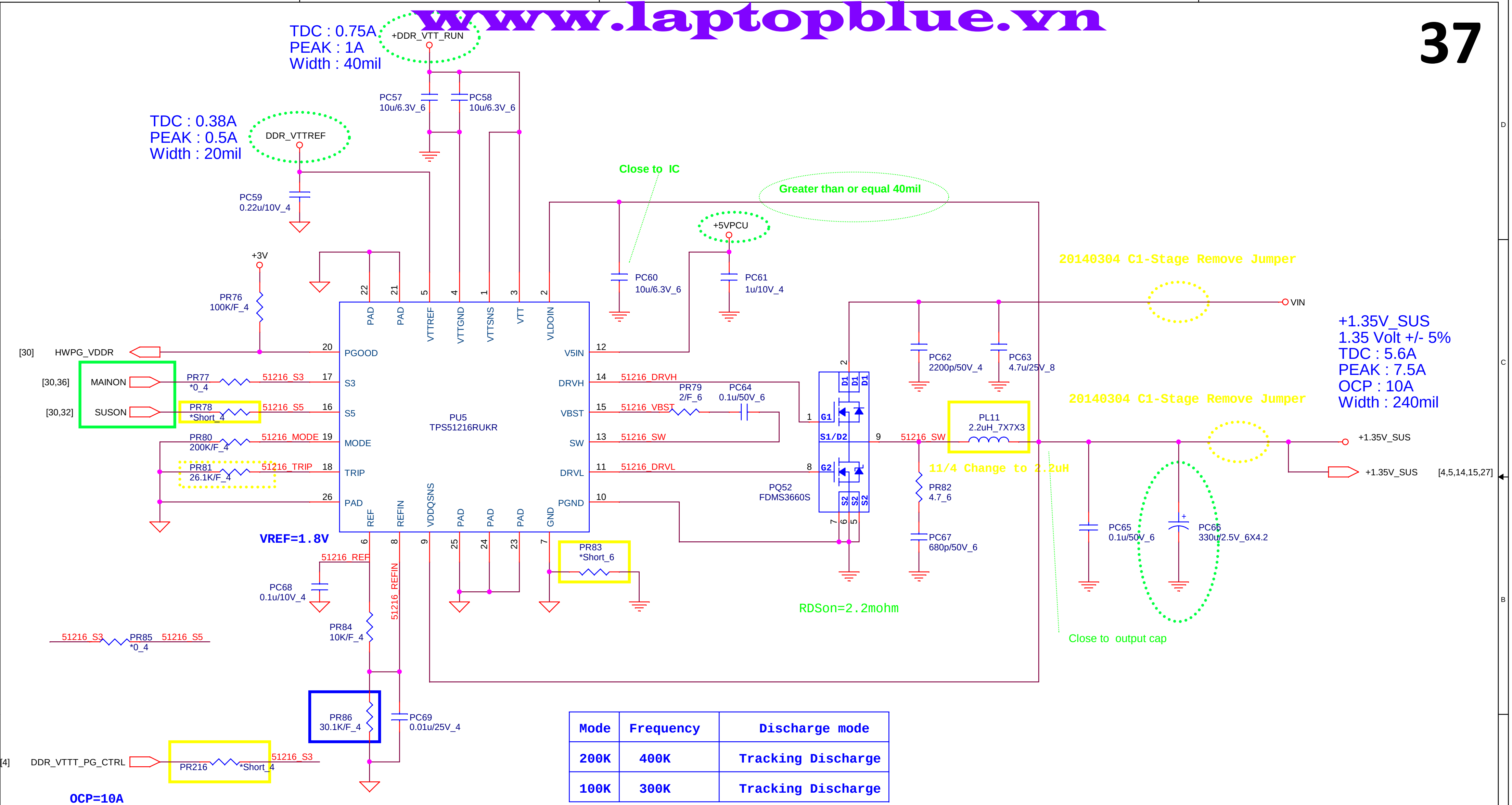


Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	2A

Date: Tuesday, April 08, 2014 Sheet 33 of 47



OCP=10A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=10-(1.425/2)*2.2mohm
=20.432mV
Rlimit=20.432mV/10uA*8=16.35Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

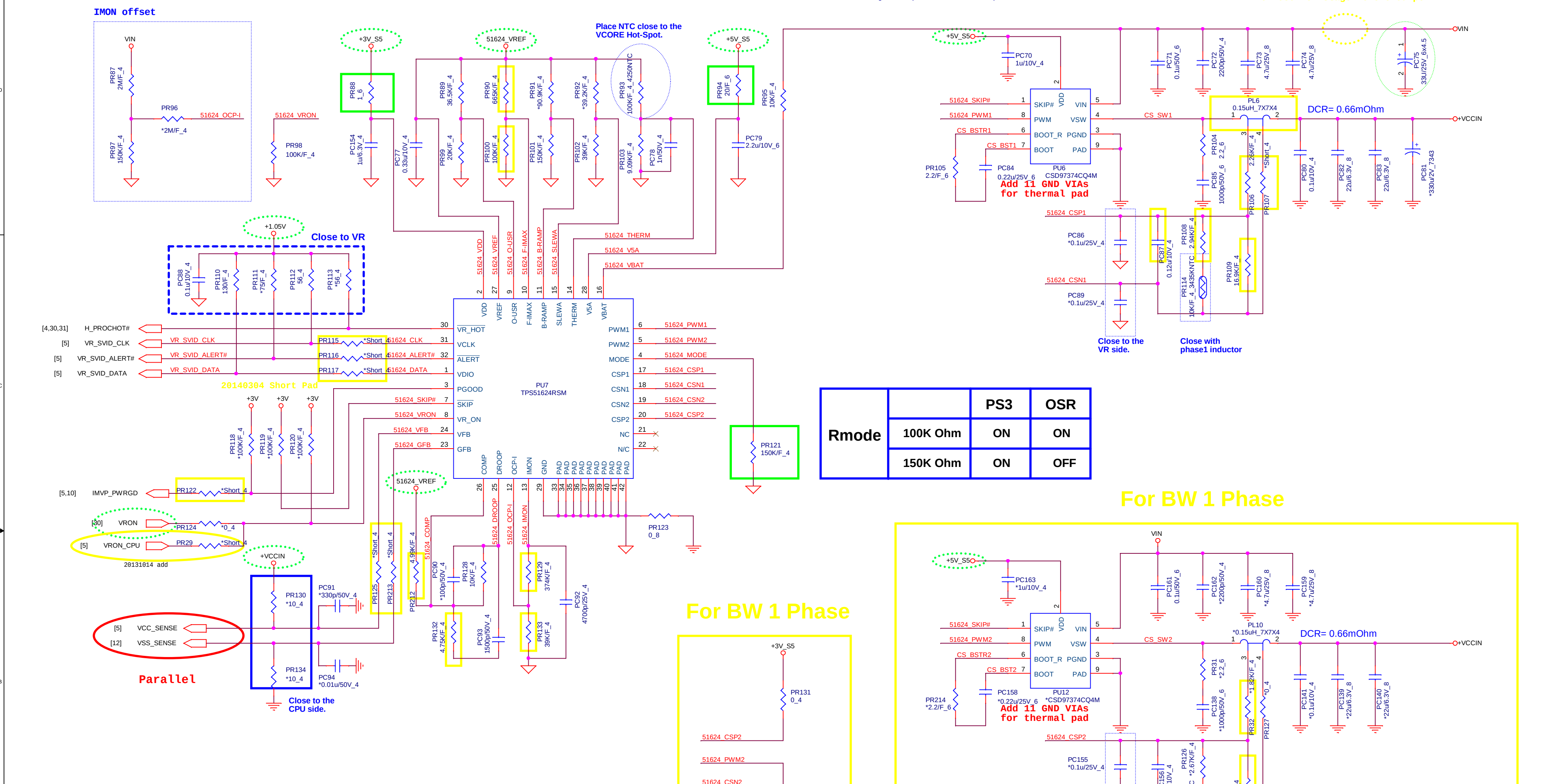
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQ0

Size | Document Number: DDR 1.35V(TPS51216) | Rev 2A

Date: Monday, April 07, 2014 | Sheet 34 of 47



Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

BW-U 15W (1 phase)

Icc TDC PL2：14A

Icc Max：32A

OCP：37A

Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

BW-U 28W (1 phase)

Icc TDC PL2：19A

Icc Max：40A

OCP：47A

Fsw：800KHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

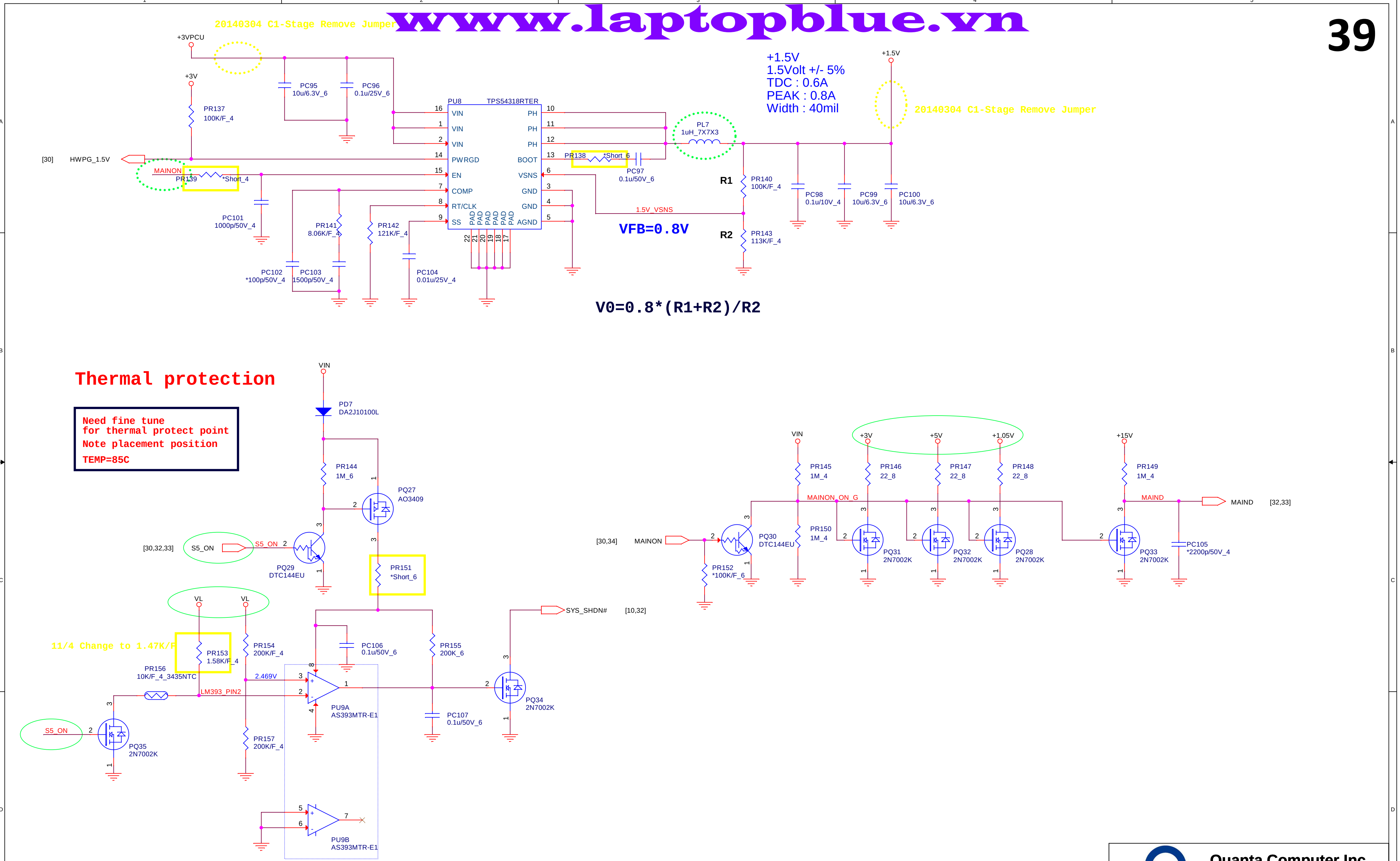
R_AC_LL：- 7.0mV/A

Quanta Computer Inc.

PROJECT：ZQ0

Size	Document Number	Rev
	+VCCIN(TPS51624)	2A

Date: Tuesday, April 08, 2014 Sheet 35 of 47



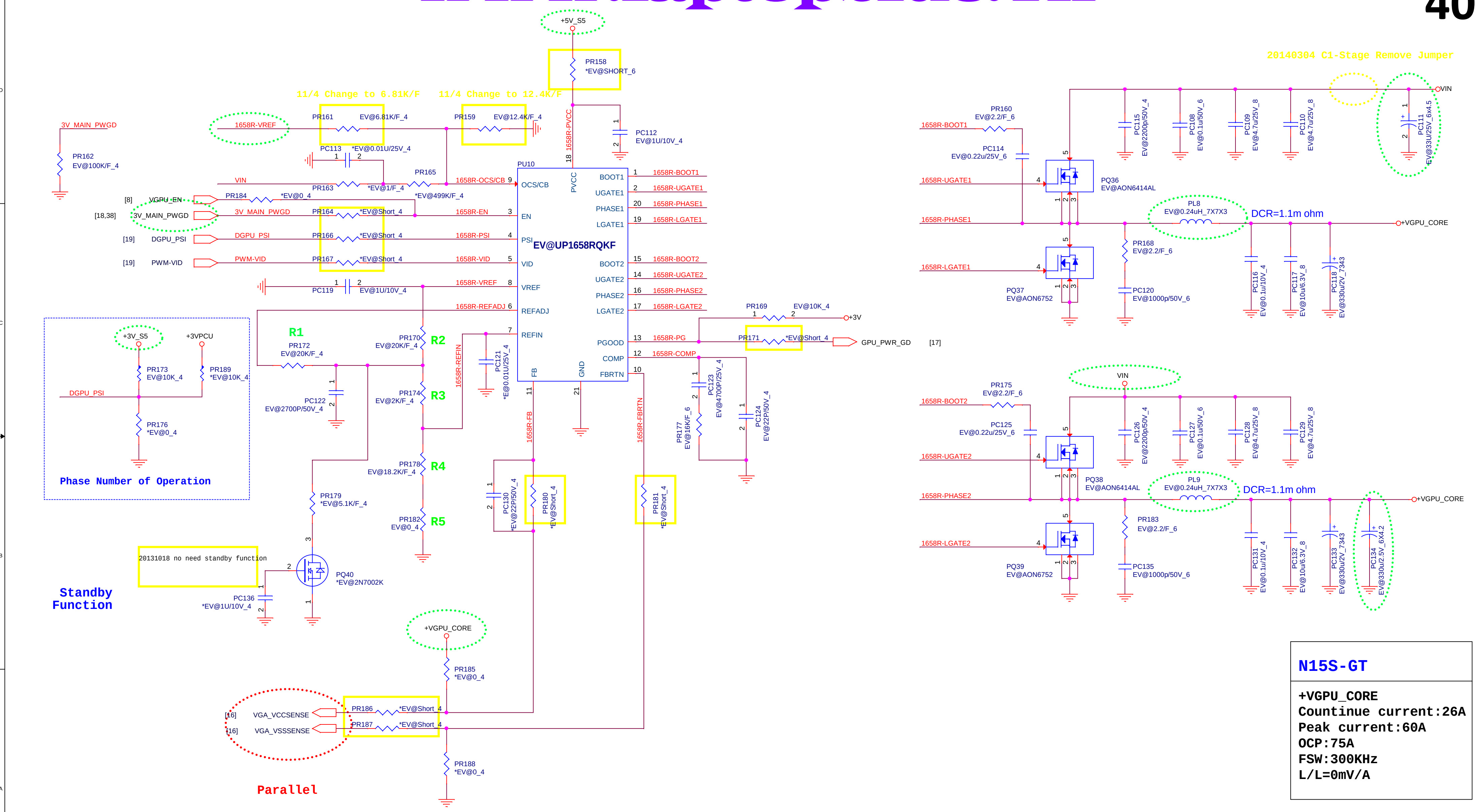
For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	+1.5V/Thermal Protect	2A

Date: Tuesday, April 08, 2014 Sheet 36 of 47

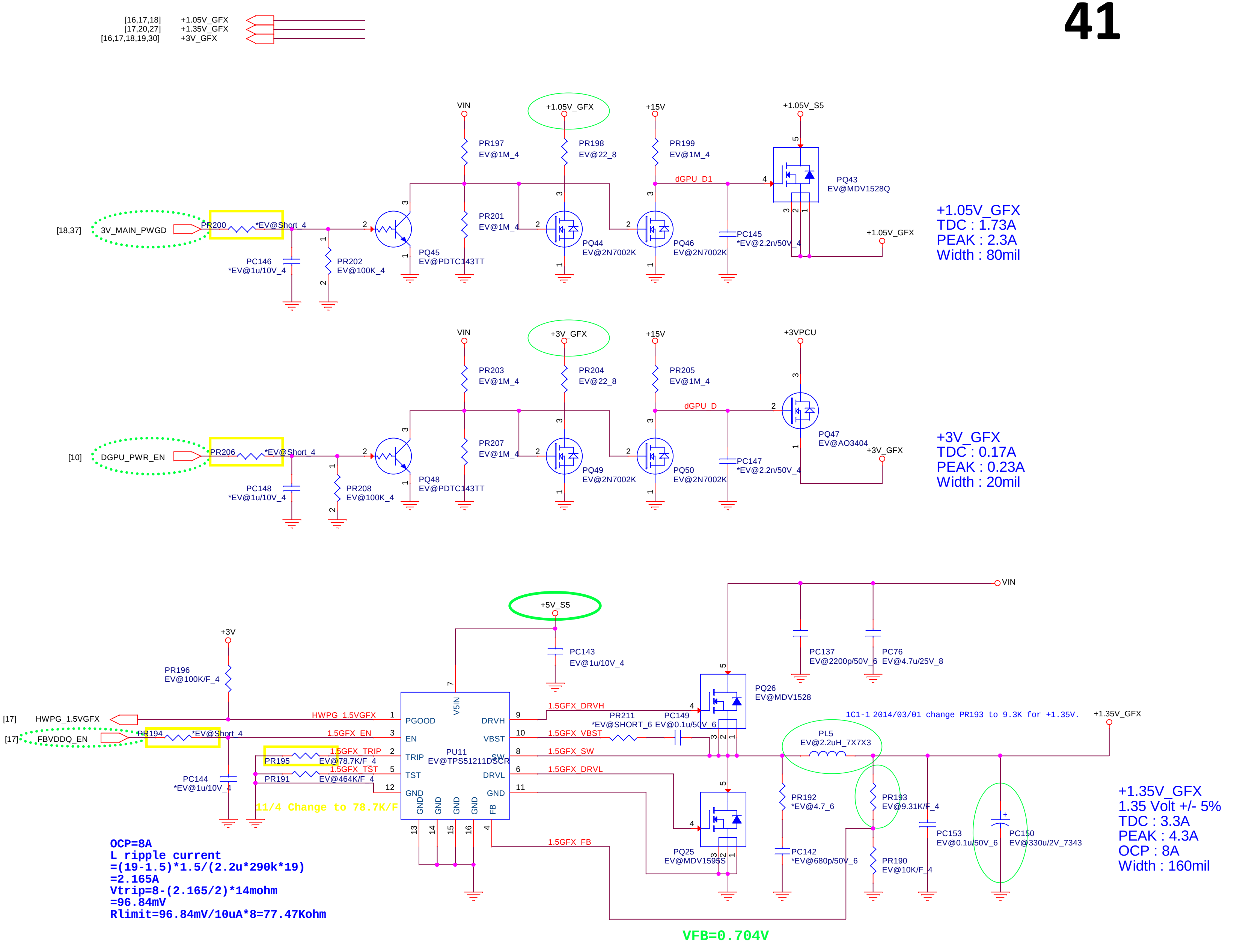


N15S-GT

+VGPU_CORE
Countinue current:26A
Peak current:60A
OCP:75A
FSW:300KHz
L/L=0mV/A

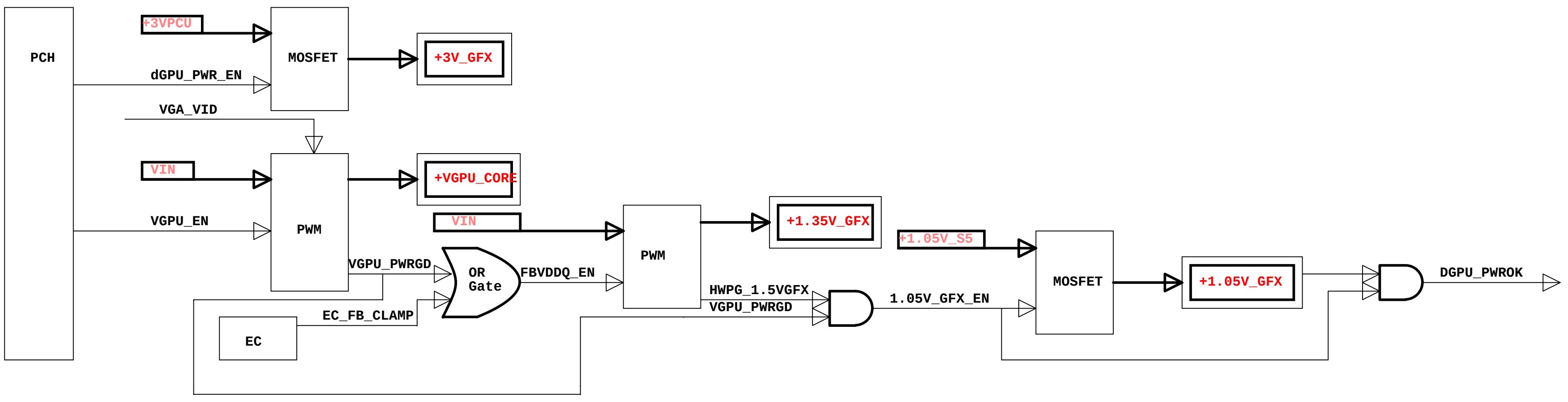
Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	2A
Date: Monday, April 07, 2014	Sheet 37 of 47	

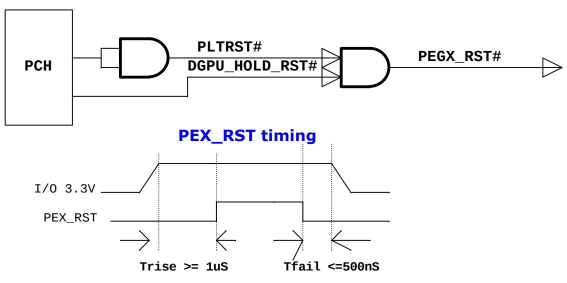


[16,17,18] +1.05V_GFX
[17,20,27] +1.35V_GFX
[16,17,18,19,30] +3V_GFX
VIN
+1.05V_GFX
+15V
+1.05V_S5
PR197 EV@1M_4
PR198 EV@22_8
PR199 EV@1M_4
dGPU_D1
PQ43 EV@MDV1528Q
[18,37] 3V_MAIN_PWGD
PR200 *EV@Short_4
PR201 EV@1M_4
PQ45 EV@PDTC143TT
PQ44 EV@2N7002K
PQ46 EV@2N7002K
PC145 *EV@2.2n/50V_4
+1.05V_GFX
PC146 *EV@1u/10V_4
PR202 EV@100K_4
+1.05V_GFX
TDC : 1.73A
PEAK : 2.3A
Width : 80mil
VIN
+3V_GFX
+15V
+3VPCU
PR203 EV@1M_4
PR204 EV@22_8
PR205 EV@1M_4
dGPU_D
PQ47 EV@AO3404
[10] DGPU_PWR_EN
PR206 *EV@Short_4
PR207 EV@1M_4
PQ48 EV@PDTC143TT
PQ49 EV@2N7002K
PQ50 EV@2N7002K
PC147 *EV@2.2n/50V_4
+3V_GFX
PC148 *EV@1u/10V_4
PR208 EV@100K_4
+3V_GFX
TDC : 0.17A
PEAK : 0.23A
Width : 20mil
VIN
+5V_S5
+3V
PC143 EV@1u/10V_4
PC137 EV@2200p/50V_6
PC76 EV@4.7u/25V_8
PR196 EV@100K/F_4
PQ26 EV@MDV1528
[17] HWPG_1.5VGFX
HWPG_1.5VGFX
1.5GFX_DRVH
PR211 *EV@SHORT_6
PC149 EV@0.1u/50V_6
1C1-1 2014/03/01 change PR193 to 9.3K for +1.35V.
+1.35V_GFX
[17] FBVDDQ_EN
PR194 *EV@Short_4
1.5GFX_EN
1.5GFX_VBST
PL5 EV@2.2uH_7X7X3
PR195 EV@78.7K/F_4
1.5GFX_TRIP
1.5GFX_SW
PR191 EV@464K/F_4
1.5GFX_TST
1.5GFX_DRVL
PGOOD
EN
TRIP
TST
GND
V5IN
DRVH
VBST
SW
DRVL
GND
FB
PU11 EV@TPS51211DSCR
PC144 *EV@1u/10V_4
11/4 Change to 78.7K/F
PR192 *EV@4.7_6
PR193 EV@9.31K/F_4
PQ25 EV@MDV1595S
PC142 *EV@680p/50V_6
PR190 EV@10K/F_4
PC153 EV@0.1u/50V_6
PC150 EV@330u/2V_7343
1.5GFX_FB
+1.35V_GFX
1.35 Volt +/- 5%
TDC : 3.3A
PEAK : 4.3A
OCP : 8A
Width : 160mil
OCP=8A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=8-(2.165/2)*14mohm
=96.84mV
Rlimit=96.84mV/10uA*8=77.47Kohm
VFB=0.704V

VGA power up sequence



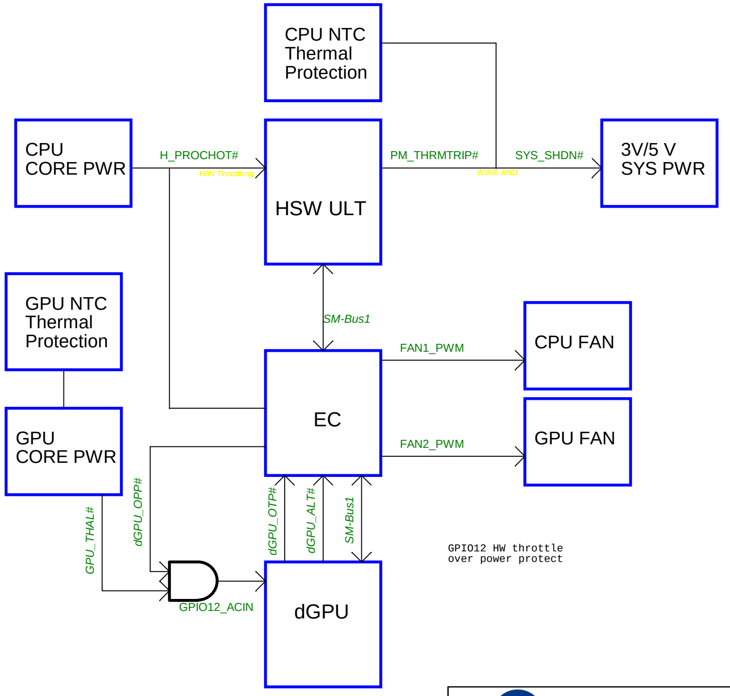
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.35V_GFX	+1.35V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

Thermal Follow Chart

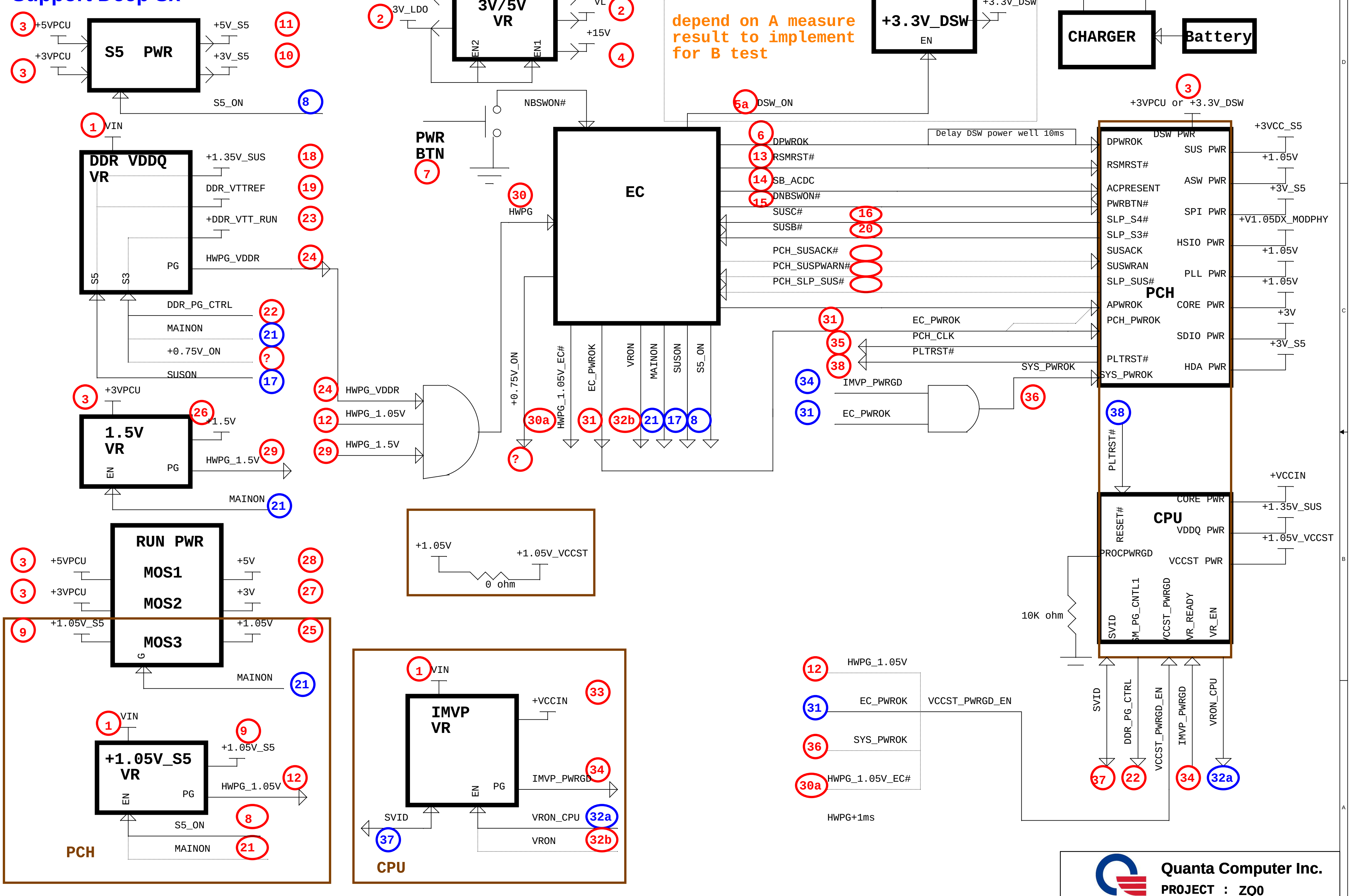


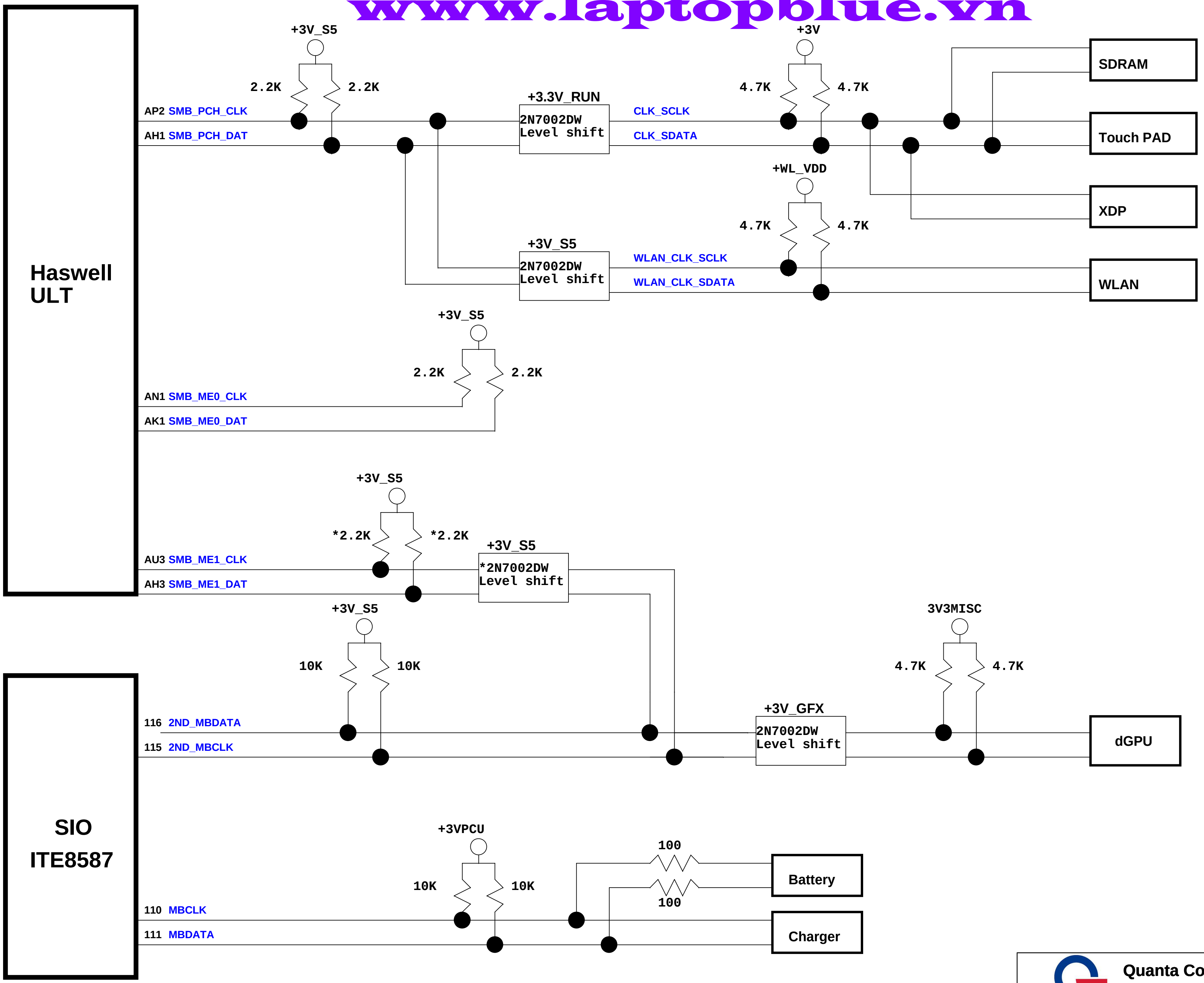
GPIO12 HW throttle over power protect

dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to infrom EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

Battery Mode

Support Deep Sx





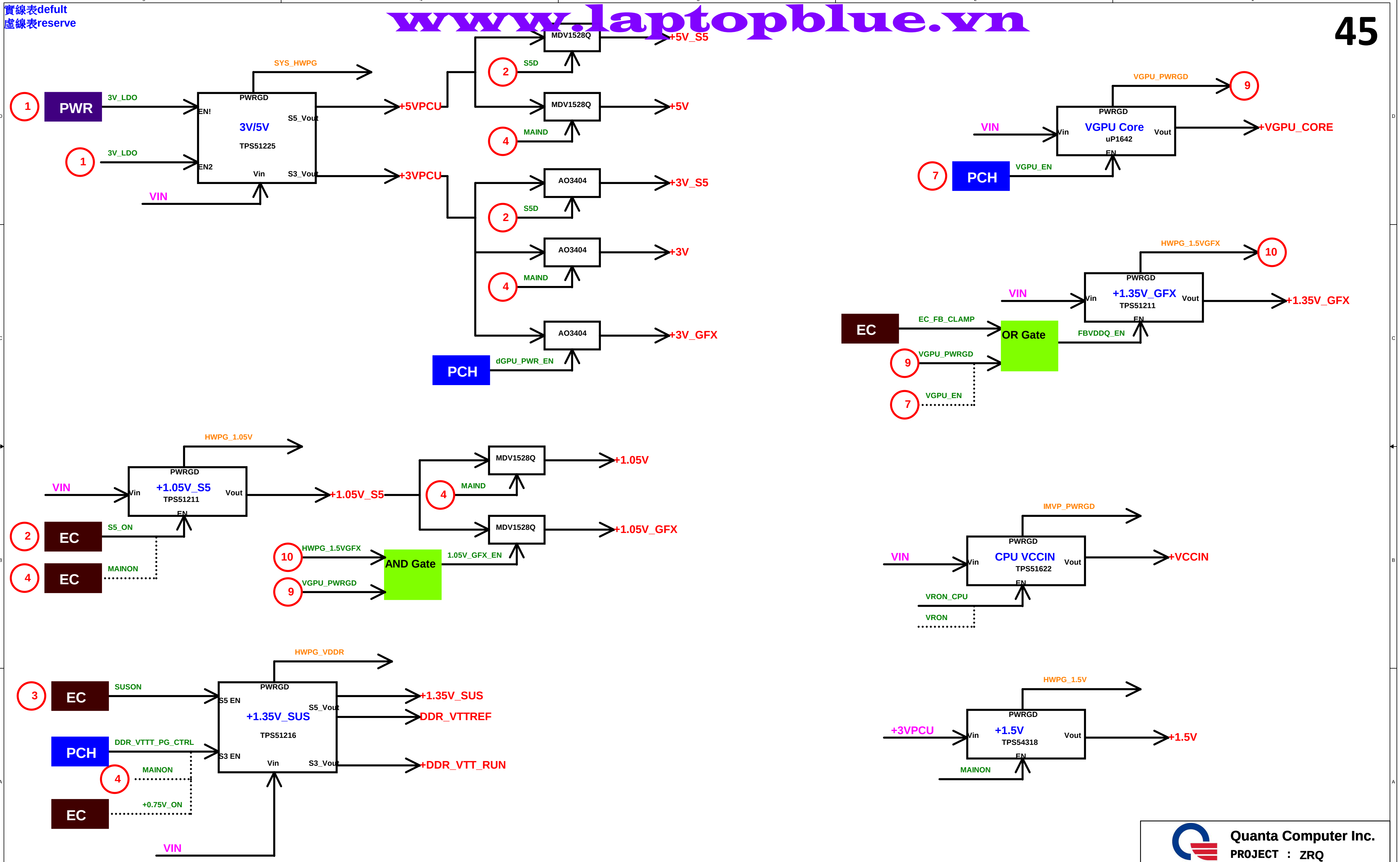
Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	Block Diagram	3A

Date: Monday, April 07, 2014 Sheet 41 of 47

實線表defult
虛線表reserve



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	ULT PWR CONTROL	3A

Date: Monday, April 07, 2014 Sheet 42 of 47

CHANGE LIST

Model	Version		CHANGE LIST
ZQ0	1A-1	1	2013/10/15 change pin define and add pwm IC.(page31)
		2	2013/10/15 Change VGA ITE solution to NXP.(page 23)
		3	2013/10/15 power board CN change to 6pin.(Page 23)
		4	2013/10/15 U5017.12 change 27M crystal to VGA IC.(Page 23)
		5	2013/10/15 U5017.14 add power rail +3V_RTC(page23)
		6	2013/10/15 strap0 R672 DG 50k PU.(Page 19)
		7	2013/10/15 Change AND gat to Q63 D-MOS.(Page 19)
		8	2013/10/15 change pin define and add pwm IC U17.(Page 46)
		9	2013/10/15 for GC6 stuff R228\R1013\R226\R1012.un-stuff Q24\Q26\R227\R1011. (Page19)
		10	20131015 For GC6 NV DG GC6_FB_EN PD.(Page10)
		11	2013/10/15 following up acer define and swap USB3 and USB2 port.(Page9)
		12	2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.(Page30)
		13	2013/10/15 U27.30/U27.31 del fan Pwm signal.(Page32)
		14	20131015 change LVDS\USB3\RJ45\FAN\TPD\USB DB CN\DC-IN CN\Power Button\Cardreader\KB BLK CN\Power board, footprint.
	1A-2	1	2013/10/16 JDIM5 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.(page15)
		2	2013/10/16 JDIM6 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].(page14)
		3	2013/10/16 Add RTC charge circuit.(page8)
		4	2013/10/16 BT1.1 Chage +3V_RTC_0 to VCCTC_2.(page8)
		5	2013/10/15 change power rail from +3V_RTC_0 to VCCRTC_2.(page23)
	1A-3	1	2013/10/16 change R5285 from 330 to 100ohm for charge RTC battery.(page23)
		2	2013/10/16 2013/10/16 U58 add 0ohm R5322/R5323 for SMBus reserve for FW burnning.(page 23)
		3	2013/10/16 U58 pin24/25 add 33ohm for HSYNC/VSYNC.(page23)
		4	2013/10/16 U58.37 add 10 ohm for test pin avide i2c impact.(page 23)
		5	2013/10/16 U24 ball K4/G2 BIOS suggestion change SMI/SCI to GPIO0~15.(page 10)
		6	2013/10/16 Add U34 flash 4M ROM reserve for ZQ0D.(page8)
		7	2013/10/16 change SMbus VGA to PCH SML0CLK/SML0DATA.(page 8)
	1A-4	1	2013/10/17 Change EC pin define for 2014 GPIO table.(page32)
		2	2013/10/17 Change All short pad to resistor.(All)
		3	2013/10/17 Change U17 to G991P11U and PU U17 pin1.(page31)
		4	2013/10/17 Remove Q25\R231\R232 because not support GPIO9 for ADPS circuit to infrom EC NV dGPU VPS Alert.(page19)
		5	2013/10/17 remove Q5020 no IOAC support.(page26)
		6	2013/10/17 remove R5224\R5225\R5226 no IOAC support.(page26)
		7	2013/10/17 remove WLAN_OFF no IOAC support.(page26)
		8	2013/10/17 Del U22 becuse no support IOAC.(page32)
	1A-5	1	2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.(Page31)
		2	2013/10/18 Change VGA NXP soltion to ITE.(page23)
		3	2013/10/18 design change R5293 from 22ohm to 33ohm.(page23)
		4	2013/10/18 Change Touch screen power rail from 5V to 3V.(page24)
		5	2013/10/18 add 0ohm short TP interrap pin.(page24)
		6	2013/10/18 change U27.87 for Touch pad ID for I2C/PS2 solution switch.(page 32)
	1A-6	1	2013/10/18 Change Q63 to MOS.(page19).
		2	2013/10/21 reversal PEG lan for layout.(page9).
		3	2013/10/21 Del APWORK.(page5)
		4	2013/10/19 Swap DDR so-ddim pin for layout request.(page14,15)
	1A-7	1	2013/10/22 change CN24 pin define based on spec.(page31)
		2	2013/10/22 change CN25 pin define for spec.(page31)
		3	2013/10/22 Change CN4 to 6pin.(page23)
		4	2013/10/22 change Y5004 to +/-10PPM(page23)
		5	2013/10/21 add R5331 between 3V_GFX and 3V_MIN for not GC6 support.(page20)
		6	2013/10/22 change PJ1 Pin define same as ZQN.(page33)
		7	2013/10/22 Change LGND to GND.(page28)
		8	2013/10/22 CN5006 pin9/10 add R5332/r5333 for ESD protect.(page28)
		9	2013/10/22 Change CN5009\CN5013\Y7 footprint.
	1A-8	1	2013/10/22 change CN24 pin define based on spec based on ZRQ.(page31)
		2	2013/10/23 change CN25 footprint.(page31)
		3	2013/10/23 Change DIMM1_SA0/SA1 to DIMM0_SA0/SA1.(page14)
		4	20131022 Change GPIO83/84 GPU GC6 pin to GPIO2/3.(page10)
		5	2013/10/21 Swap PEG to nomroal mode.(page9)
		6	2013/10/23 remove R5017 5V is duplicater.(page27).
		7	2013/10/23 remove C5056 is duplicater.(page27)
		8	2013/10/23 change CN5008\CN25 footprint to match DXF.
		9	2013/10/23 add scrow Hole footprint.
	1A-9	1	2013/10/17 Change power LED from +3VPCU to +3V_S5.(page27)
		2	2013/10/24 add 100kohm on U5011 pin 26 with C5164 for discharge(page30)
		3	2013/10/23 add 10k for vendor suggestion.(page28)
		4	2013/10/23 add R5335 Isolate SLB9660 NC.(page23).
		5	2013/10/24 Add alert on U17.1 for CPU themal tempture.(page31).
	1A-10	1	2013/10/25 remove 1.35GFX_PDG NET.(page20)
		2	2013/10/25 remove 1.35GFX_PDG (page20)
		3	2013/10/25 remove 1.35GFX POWER(page20)
		4	2013/10/25 reserve AV2 ball to GND.(page6)
		5	20131025 reserve A5 ball to 100k PU 3VPCU.(page6)
		6	2013/10/25 modify PJ2 footprint.(page33)
		7	2013/10/25 change LED from 3pin to 4pin for acer reqeust,(page27)
	1A-11	1	2013/10/28 Change U5013.7 from +3V_S5 to +3V.(page23)
		2	2013/10/28 change LED from 4pin to 3pin and power LED to +3VPCU.(page27)
		3	2013/10/28 U5013 Pin8,15,28 left NC.(page23)
	1A-12	1	2013/10/29 Change CN21 power rail to S5,change Q42 direction and net name reseve PS2 PU to +3V.(page31)
		2	20131029 Change GPIO45 to PU S5,duble GPIO58 one is GPIO56.(page10).
		3	2013/10/28 reserve AV2 ball to TP.(page8)
		4	20131028 reserve A5 ball toTP.(page6)
		5	2013/10/29 Change CN5008 to S0 of SMbus(page26)
		6	2013/10/29 Swap U27 pin2 and pin128,add U27.68 for touch pad interrupt.(page32)
	1A-13	1	20131030 add touch pad interrupt pin on gpio83.(page10)
		2	2013/10/30 move Q42 to page02 change U24.U7 net name.(page2).
		3	2013/10/30 CN5002.6 add USB touch screen on/off pin to EC.(page24)
		4	2013/10/29 add U27.35 for touch pad on/off.(page32)

DOC NO.	PROJECT MODEL :	ZQ0	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Model	Version		CHANGE LIST
ZQ0	1B-2	1	2013/12/04 change PQ24 to DFN 3x3 size.(page35)
		2	2013/12/04 Change Cn14 PN and footprint.(page30).
		3	2013/12/04 change LED from 3pin to 4pin..(page27)
		4	2013/12/4 change cN6 to 4pin.(page23)
		5	2013/12/04 change GPIO36/GPI037 to PU..(page9)
	1B-3	1	2013/12/10 change Cn20 Pin define.(page25)
		2	2013/12/10 change Q3.3 from +3V to +3VPCU.(page22).
		3	2013/12/10 change CN6 footprint..(page21)
	1B-4	1	2013/12/12 Remove U9 Green CLK circuit.(page21)
	1B-5	1	2013/12/17 Change CN14 pin define.(page28)
		2	2013/12/17 Change R8051 to 0402 size.(page16)
	1B-6	1	2013/12/18 Change USB port USB3.0 to port0,USB2.0 to port1 and port3,Fingerprint to usb port2.
		2	2013/12/17 Change R8051 to 0402 size.(page16)
		3	2013/12/18 U34 pin6 reserve 0402 resistor for power noise issue.(page28)
	1B-7	1	2013/12/20 add U29 VSYNC and HSYNC by pass resistor.(page22)
		2	20131220 Change +3VPCU to +3V_S5 non deep sx(page10).
		3	2013/12/20 del c8521 and R8391..(page16)
	1C-1	1	2014/1/06 add 0ohm pass 1.05V_Modphy to 1.05V.(page33)
		2	2014/1/06 add PR224 PU to 3V.(page33).
		3	2014/1/06 Change R351\R388 from 47ohm to 65ohm base on FAE request..(page28)
		4	2014/01/10 Remove U29 and add U40 and U41..(page22)
	1C-2	1	2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.(page29)
		2	20140113 PU6\PU12 change footprint for SMT request.(page35).
		3	2014/01/13 change CN14 sata net name and add C678~C681.(page25)
		4	2014/01/13 add R678\R677 PU and R679 PD for ICT..(page19)
		5	2014/01/131/13 Adding +3V_SUS power for touch pad (acer request).(page32)
	1C-3	1	2014/01/14 change R654 to 0ohm.(page27)
		2	2014/01/14 Change Cn11 Footprint.(page24).
	1C-4	1	2014/01/15 reserve TP power rail +3V_S5..(page29)
		2	2014/01/15 TPM CO-lay nuvoton(page21).
		3	2014/01/15 SWAP PCIE LAN TX single.(page26).
	1C1-1	1	2014/03/01 change PR193 to 9.3K for +1.35V.(page38)
		2	2014/02/17 Add U11.98 GPIO5 for PTP power en function.(page30).
		3	2014/02/17 Add Q47 for PTP power EN and soft start R694\C713 and C712\C686.(page29)
		4	2014/02/06 change Blue LED power rail to +5VPCU and add ESD and Change LED to lite-on and R379=820,R375=680 base on test result.(page25)
		5	2014/02/6 add VGA_ALERT# PU 10K for FAE request.(page19)
		6	2014/02/19 add R692 for SUSPWRACK# to EC.(page07)
		7	2014/03/01 Change 0ohm to short pad.
		8	2014/03/01 link L29 to +3V directly(meet IVDDO vs OVDD sequence)(page 21)
	1C1-2	1	2014/03/08 add R696\R697 PU..(page30)
		2	2014/03/08 ChangeU12 footprint to sot23 and add VC2\VC1 change C307 to 3528.(page27).
		3	2014/03/08 Remove PCIE wake and stuff R642, un-stuff Q44..(page24)
		4	2014/03/11 Add R698 for TS_EN short TP_INT,for issue debug.(page22)

DOC NO.	PROJECT MODEL :	ZRQ	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	Change list-2	3A

Date: Monday, April 07, 2014 Sheet 44 of 44