H61H2-AM3 Rev : A

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A		

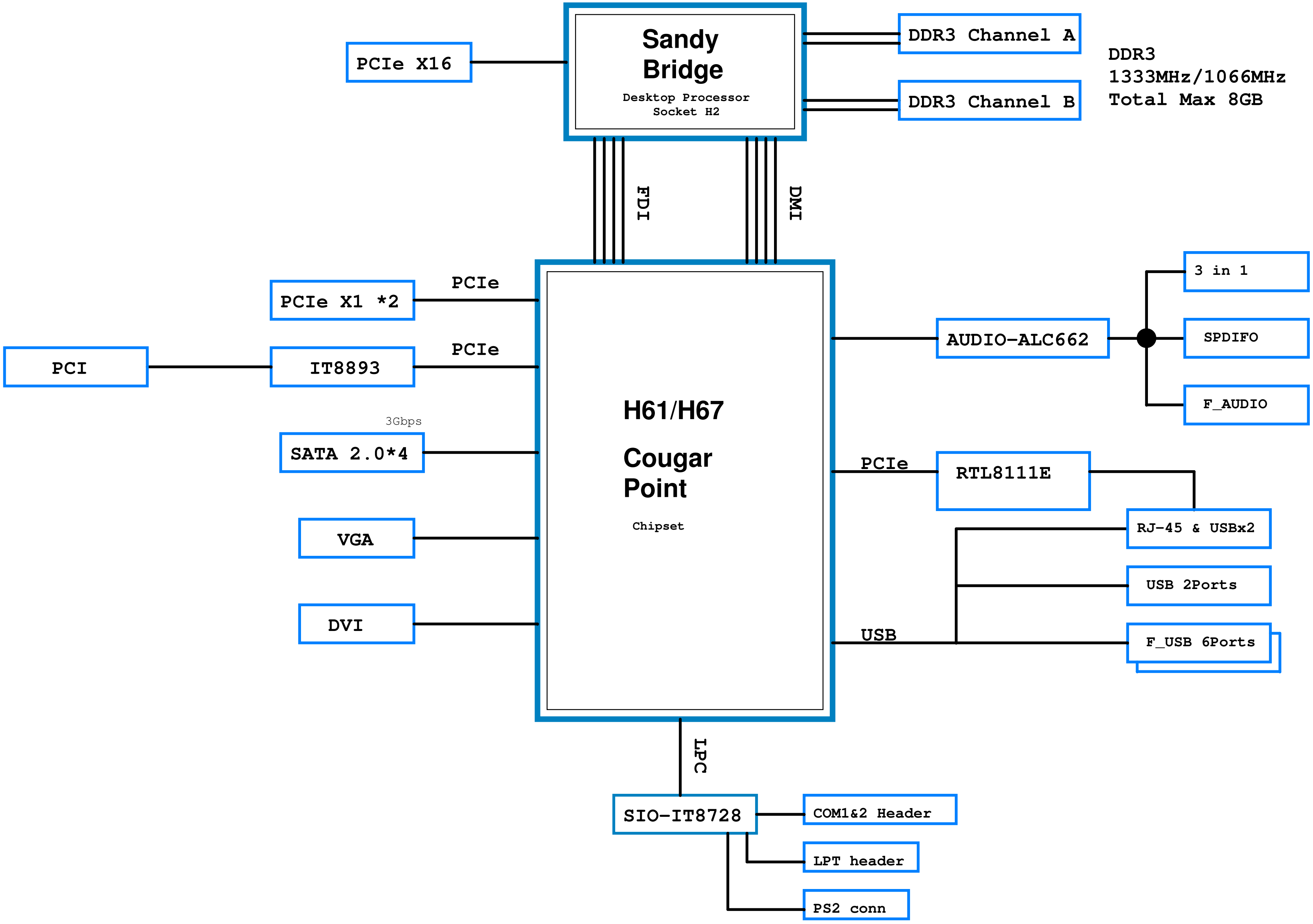
Table 1-2. Desktop Intel® 6 Series Chipset SKUs

Feature Set		Q67	Q65	B65	Z68	H67	P67	H61
PCI Express* 2.0 Ports		8	8	8	8	8	8	6[9]
PCI Interface		Yes	Yes	Yes	No[10]	No[10]	No[10]	No[10]
USB 2.0 Ports		14	14	12[6]	14	14	14	10[7]
Total number of SATA ports		6	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)		2[4]	1[5]	1[5]	2[4]	2[4]	2[4]	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)		4	5	5	4	4	4	4[8]
HDMI/DVI/VGA/DisplayPort*/eDP*		Yes	Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP		Yes	Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	Yes	No[3]
	RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	Yes	No
	Intel RST SSD Caching[11]	No	No	No	Yes	No	No	No
Intel® AT		Yes	Yes	No	No	No	No	No
Intel® AMT 7.0		Yes	No	No	No	No	No	No

NOTES:

1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs
3. The PCH provides hardware support for AHCI functionality when enabled by appropriate system configurations and software drivers.
4. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
5. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
6. USB ports 6 and 7 are disabled.
7. USB ports 6, 7, 12 and 13 are disabled.
8. SATA ports 2 and 3 are disabled.
9. PCIe ports 7 and 8 are disabled.
10. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See Section 5.1.9 for more details.
11. Intel RST SSD Caching naming is not final at this time and is subject to change.

NOTE:
Design by
428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev2_0
443554_443554_Intel6Series_C200Series_Chipset_EDS_Rev2p0
445465_445465_Sandy_Bridge_Family_EDS_Vol2_Rev2p0



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Title	Block Diagram	
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	Case Open GPIO	GPI
GPIO1	VCC3	GPIO1_OBR	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO14	3VSB	USB_OC_L7	Native
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	R_7536_EN	GPO
GPIO34	VCC3	TP_VGA	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO45	3VSB	SPI_WPSW	Native
GPIO57	3VSB	SPI_WP_GPIO	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO72	3VSB	R_7536_EN	Native

SIO-GPIO function

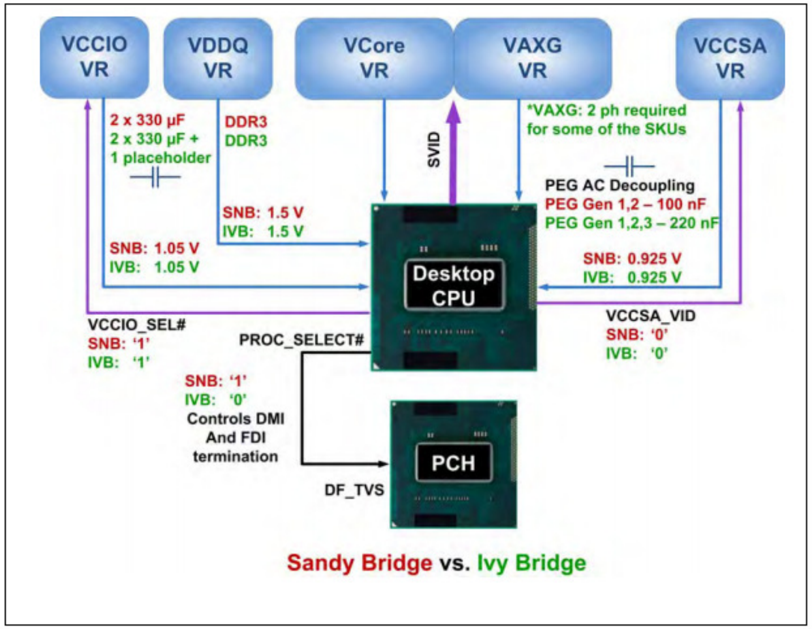
Pin Name	Power Well	Usage	Default Status
GP16	VCC3	SIO_BEEP	
GP23	3VSB	Power LED	
GP22	3VSB	Power LED	
GP40	3VSB	+DIMM_5VDUAL_Control	
* GP35	VCC3	RESERVE	
* GP36	VCC3	RESERVE	
* GP37	VCC3	RESERVE	
GP47	VCC3	RESERVE	
GP14	VCC3	RESERVE	
GP66	3VSB	SMBCLK_STBY	
GP67	3VSB	SMBDATA_STBY	

Sandy Bridge to Ivy Bridge Electrical Compatibility List

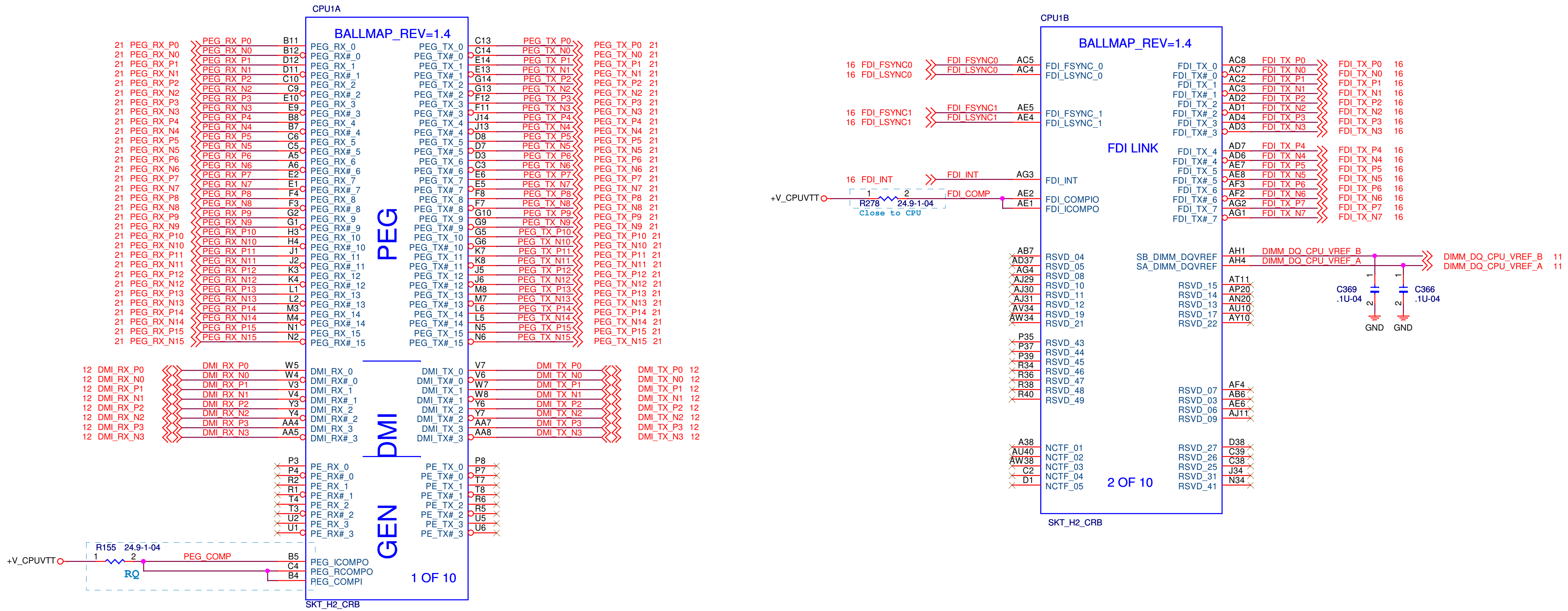
Description: The follow list provides the electrical platform deltas on designing a Desktop/Server/WS board to support both Sandy Bridge and Ivy Bridge Processors.

No	Requirements	Configuration Details	Comments
1	Processor PCI Express Graphics Guidelines	**Ivy Bridge Compatible (PCIe Gen3):** In order to support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 220 nf. Comply with bundle matching and fiber weave as specified in the Rev1.5 PDG. **Sandy Bridge only implementation:** The AC coupling caps are of value 75-200nF to support Gen1 and Gen2 PCIe.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 4.1.7: Table 4.4
2	DDR3 VREF	**Ivy Bridge Compatible:** Route DIMM VREFA and DIMM VREFB from the CPU to the DIMM Write VREF circuit. **Sandy Bridge only implementation:** The DIMM VREFA and DIMM VREFB pins from the CPU do not need to connect to the DIMM write VREF circuit.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 3.4
3	PROC_SELECT# and DF_TVS Signals	**Ivy Bridge Compatible:** Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 4.7K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH V_NAND_IO rail. **Sandy Bridge only implementation:** PROC_SELECT# can be left as No Connect or same as IVB connectivity. DF_TVS needs to be pulled up to V_NAND_IO power rail through 2.2 K Ohm +/-5% resistor.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 5.4.4, Figure 5-4
4	VCCIO VR Implementation	**Ivy Bridge Compatible:** Need to design your VR to be 1.0/1.05V selectable via the VCCIO_SEL pin. No additional VRs needed for compatibility **Sandy Bridge only implementation:** VCCIO VR can be fixed at 1.05V	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 30.9, Table 30-9
5	VCCSA VR implementation	**Ivy Bridge Compatible:** Design your VR to be 0.925/0.85V selectable via VCCSA_VID0 pin. **Sandy Bridge only implementation:** VCCSA VR can be fixed at 0.925 V.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 30.9, Table 30-9

Figure 1-2. Desktop Sandy Bridge vs. Ivy Bridge Compatibility Diagram



Function	INT port	PCI-E X1 port	Chipset
LAN Ethernet Controller	INTC#	PCI Express #3 Pin	Realtek RTL8111E
SATA Controller	INTB#	N/A	H61 intergrated
PCIE to PCI Bridge	INTD#	PCI Express #4 Pin	H61 intergrated
PCIEX1 NO.2	INTA#	PCI Express #5 Pin	H61 intergrated
PCIEX1 NO.1	INTB#	PCI Express #6 Pin	H61 intergrated



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

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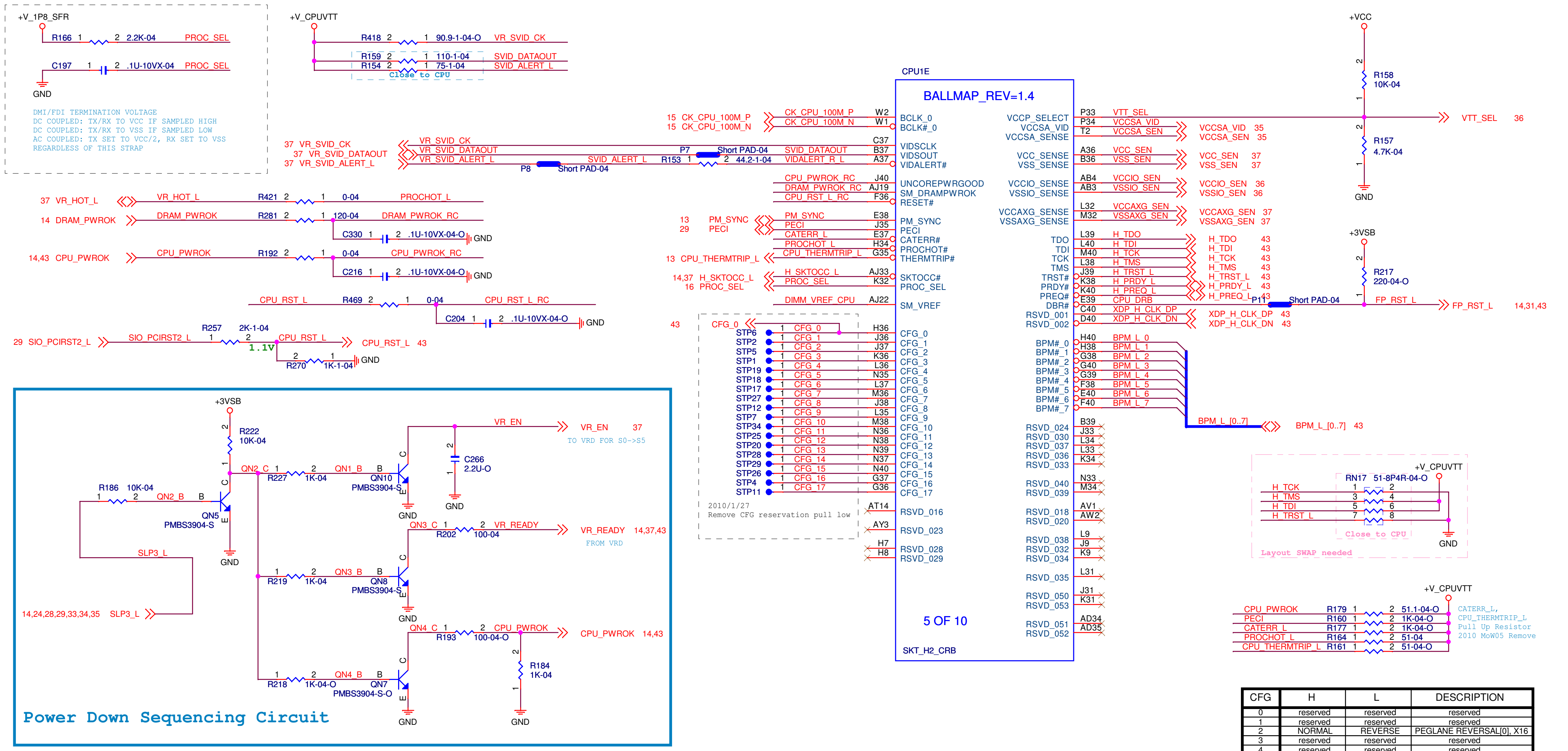

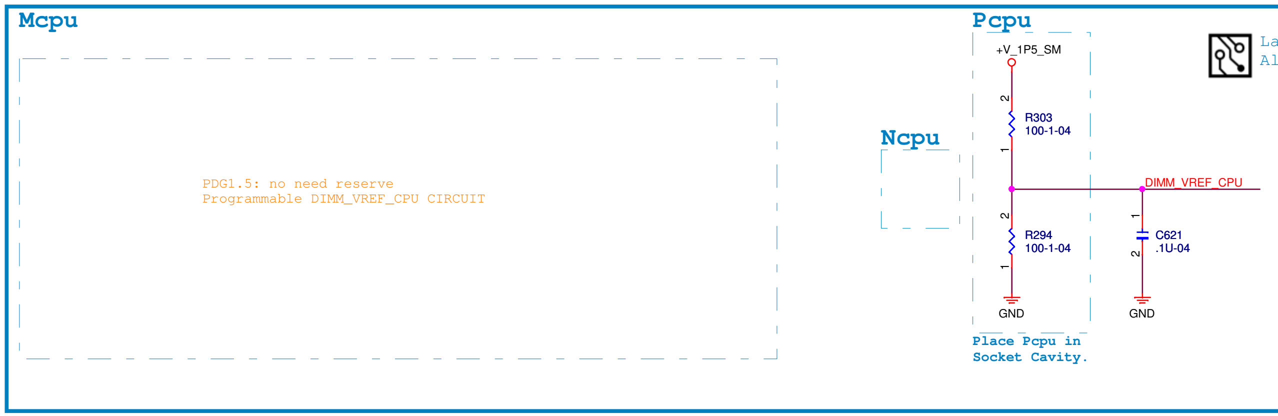

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
* 1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

DIMM_VREF_CPU Control Mode:

Control Mode / Part	Divider	PCH + Controller
Mcpu	X	V
Ncpu	X	V
Pcpu	V	X

Default

DIMM_VREF_CPU Control Circuit

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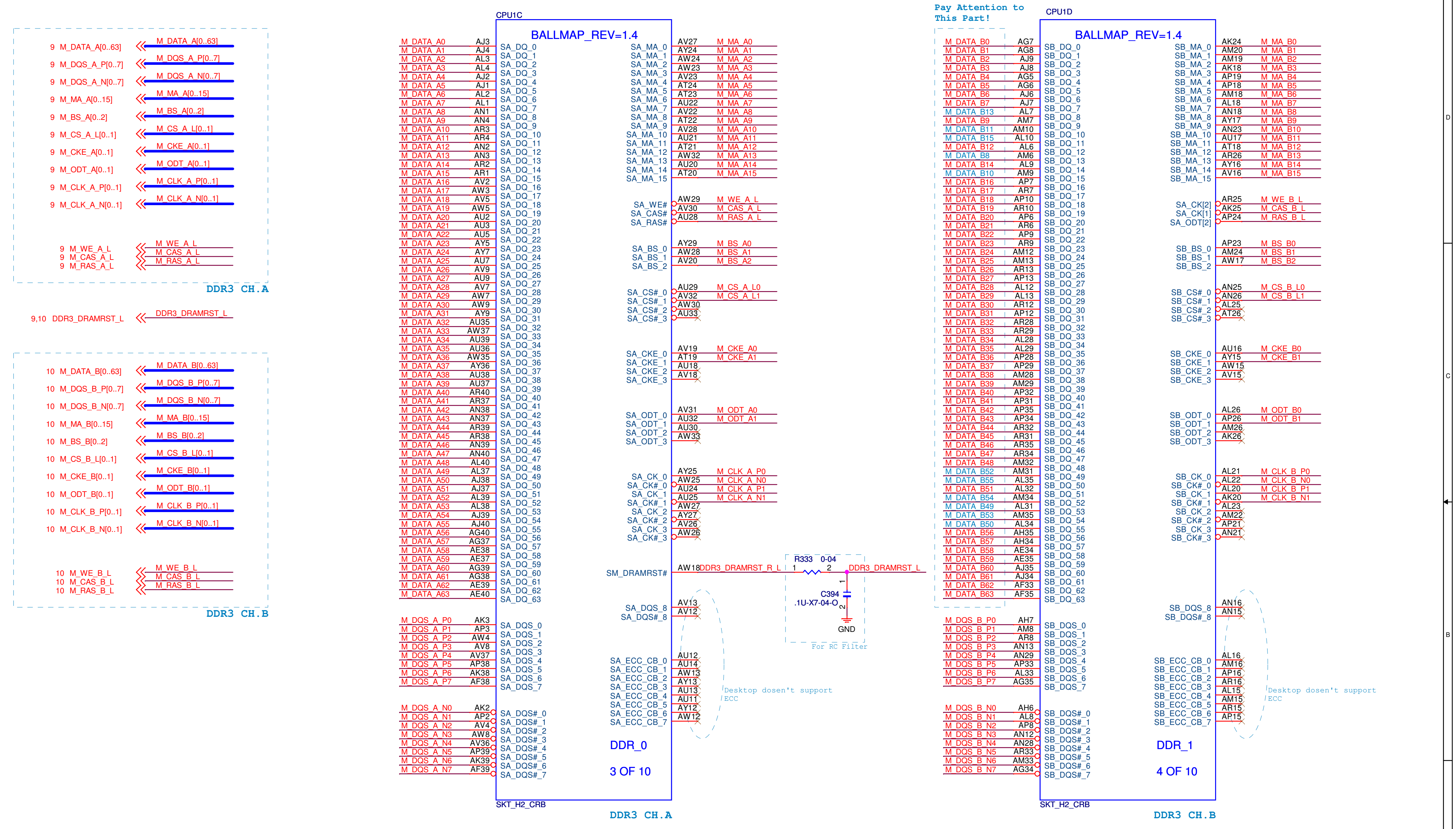

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Title: CPU - DDR3

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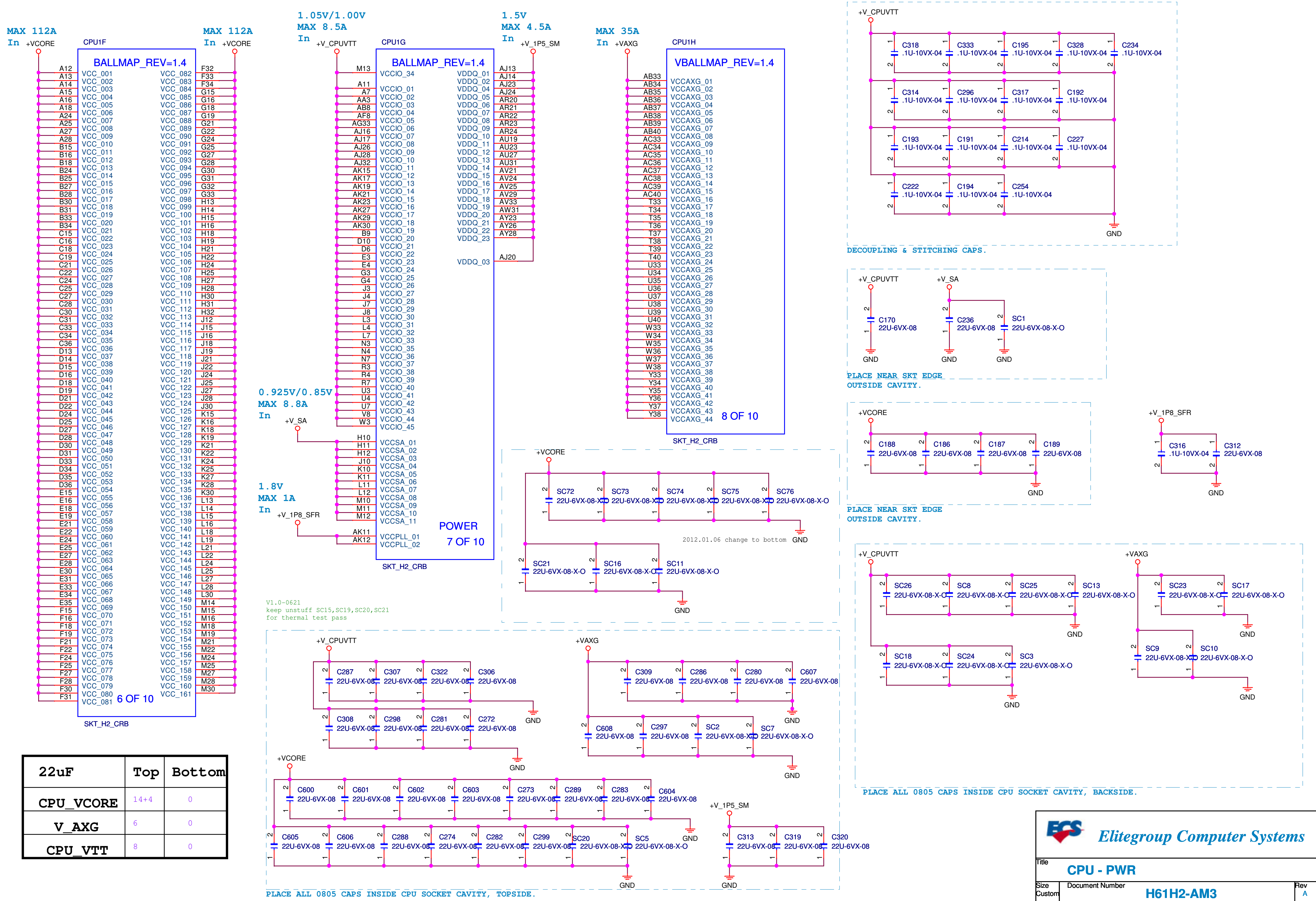

22uF	Top	Bottom
CPU_VCORE	14+4	0
V_AXG	6	0
CPU_VTT	8	0

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Title: CPU - PWR

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CPU1I — BALLMAP_REV=1.4 (SKT_H2_CRB) — 9 OF 10

Pin	Signal	Signal	Pin
A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM39
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM5
AA38	VSS_011	VSS_101	AN10
AA6	VSS_012	VSS_102	AN11
AB5	VSS_013	VSS_103	AN14
AC1	VSS_014	VSS_104	AN17
AC6	VSS_015	VSS_105	AN19
AD33	VSS_016	VSS_106	AN22
AD36	VSS_017	VSS_107	AN24
AD38	VSS_018	VSS_108	AN27
AD39	VSS_019	VSS_109	AN30
AD40	VSS_020	VSS_110	AN31
AD5	VSS_021	VSS_111	AN32
AD8	VSS_022	VSS_112	AN33
AE3	VSS_023	VSS_113	AN34
AE33	VSS_024	VSS_114	AN35
AE36	VSS_025	VSS_115	AN36
AF1	VSS_026	VSS_116	AN5
AF34	VSS_027	VSS_117	AN6
AF36	VSS_028	VSS_118	AN7
AF37	VSS_029	VSS_119	AN8
AF40	VSS_030	VSS_120	AN9
AF5	VSS_031	VSS_121	AP1
AF6	VSS_032	VSS_122	AP11
AF7	VSS_033	VSS_123	AP14
AG36	VSS_034	VSS_124	AP17
AH2	VSS_035	VSS_125	AP22
AH3	VSS_036	VSS_126	AP25
AH33	VSS_037	VSS_127	AP27
AH36	VSS_038	VSS_128	AP30
AH37	VSS_039	VSS_129	AP36
AH38	VSS_040	VSS_130	AP37
AH39	VSS_041	VSS_131	AP4
AH40	VSS_042	VSS_132	AP40
AH5	VSS_043	VSS_133	AP5
AH8	VSS_044	VSS_134	AR11
AJ12	VSS_045	VSS_135	AR14
AJ15	VSS_046	VSS_136	AR17
AJ18	VSS_047	VSS_137	AR18
AJ21	VSS_048	VSS_138	AR19
AJ25	VSS_049	VSS_139	AR27
AJ27	VSS_050	VSS_140	AR30
AJ36	VSS_051	VSS_141	AR36
AJ5	VSS_052	VSS_142	AR5
AK1	VSS_053	VSS_143	AT1
AK10	VSS_054	VSS_144	AT10
AK13	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	AT35
AK8	VSS_072	VSS_162	AT36
AK9	VSS_073	VSS_163	AT37
AL11	VSS_074	VSS_164	AT38
AL14	VSS_075	VSS_165	AT39
AL17	VSS_076	VSS_166	AT4
AL19	VSS_077	VSS_167	AT40
AL24	VSS_078	VSS_168	AT5
AL27	VSS_079	VSS_169	AT6
AL30	VSS_080	VSS_170	AT7
AL36	VSS_081	VSS_171	AT8
AL5	VSS_082	VSS_172	AT9
AM1	VSS_083	VSS_173	AU1
AM11	VSS_084	VSS_174	AU15
AM14	VSS_085	VSS_175	AU26
AM17	VSS_086	VSS_176	AU34
AM2	VSS_087	VSS_177	AU4
AM21	VSS_088	VSS_178	AU6
AM23	VSS_089	VSS_179	AU8
AM25	VSS_090	VSS_180	AV10
A4	VSS_NCTF_01		
AV39	VSS_NCTF_02		

GND GND

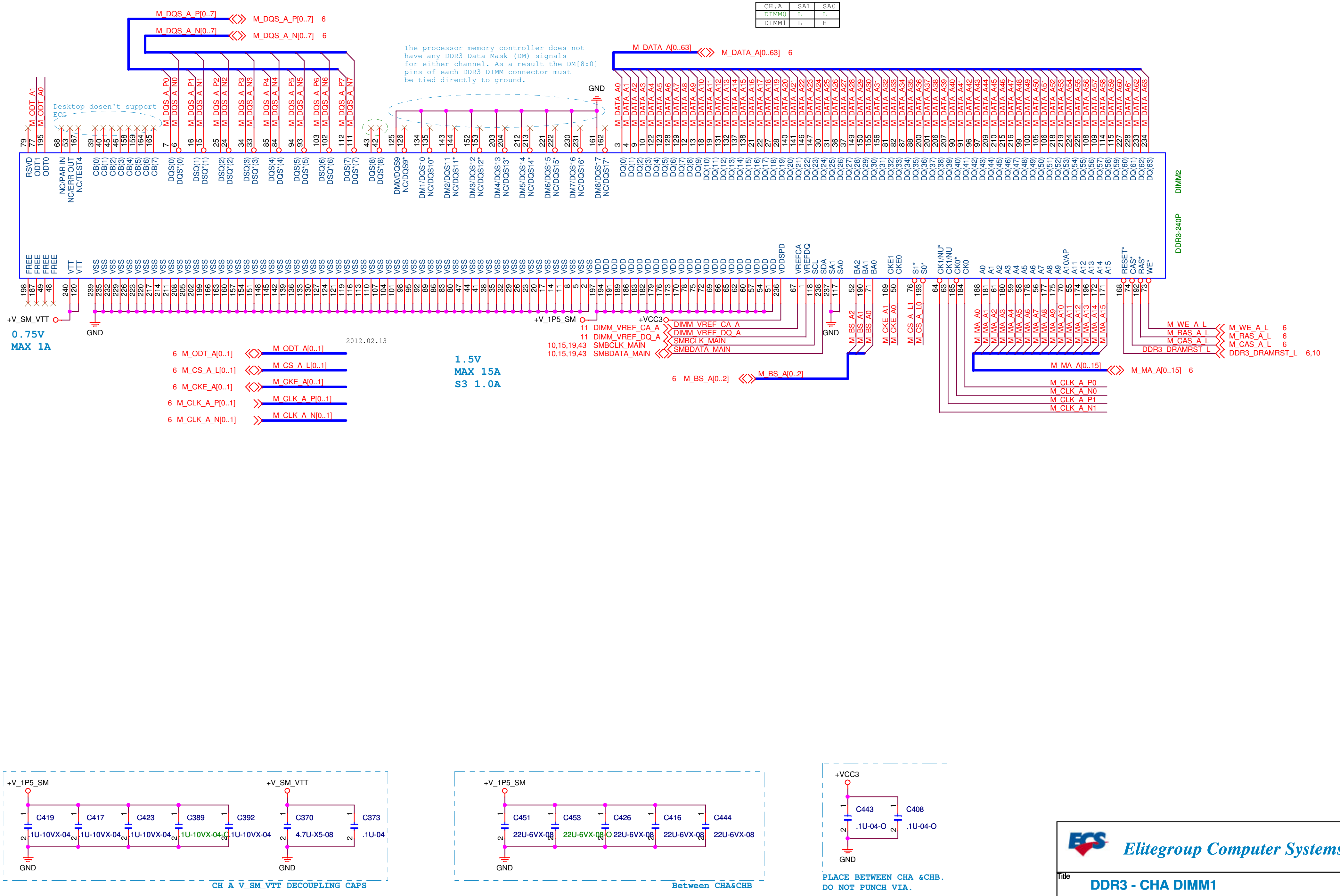
CPU1J — BALLMAP_REV=1.4 (SKT_H2_CRB) — 10 of 10

Pin	Signal	Signal	Pin
AV11	VSS_181	VSS_271	G8
AV14	VSS_182	VSS_272	H1
AV17	VSS_183	VSS_273	H17
AV3	VSS_184	VSS_274	H2
AV35	VSS_185	VSS_275	H20
AV38	VSS_186	VSS_276	H23
AV6	VSS_187	VSS_277	H26
AW10	VSS_188	VSS_278	H29
AW11	VSS_189	VSS_279	H33
AW14	VSS_190	VSS_280	H35
AW16	VSS_191	VSS_281	H37
AW36	VSS_192	VSS_282	H39
AW6	VSS_193	VSS_283	H5
AY11	VSS_194	VSS_284	H6
AY14	VSS_195	VSS_285	H9
AY18	VSS_196	VSS_286	J11
AY35	VSS_197	VSS_287	J17
AY4	VSS_198	VSS_288	J20
AY6	VSS_199	VSS_289	J23
AY8	VSS_200	VSS_290	J26
B10	VSS_201	VSS_291	J29
B13	VSS_202	VSS_292	J32
B14	VSS_203	VSS_293	K1
B17	VSS_204	VSS_294	K12
B23	VSS_205	VSS_295	K13
B26	VSS_206	VSS_296	K14
B29	VSS_207	VSS_297	K17
B32	VSS_208	VSS_298	K2
B35	VSS_209	VSS_299	K20
B38	VSS_210	VSS_300	K23
B6	VSS_211	VSS_301	K26
C11	VSS_212	VSS_302	K29
C12	VSS_213	VSS_303	K33
C17	VSS_214	VSS_304	K35
C20	VSS_215	VSS_305	K37
C23	VSS_216	VSS_306	K39
C26	VSS_217	VSS_307	K5
C29	VSS_218	VSS_308	K6
C32	VSS_219	VSS_309	L10
C35	VSS_220	VSS_310	L17
C7	VSS_221	VSS_311	L20
C8	VSS_222	VSS_312	L23
D17	VSS_223	VSS_313	L26
D2	VSS_224	VSS_314	L29
D20	VSS_225	VSS_315	L8
D23	VSS_226	VSS_316	M1
D26	VSS_227	VSS_317	M17
D29	VSS_228	VSS_318	M2
D32	VSS_229	VSS_319	M20
D37	VSS_230	VSS_320	M23
D39	VSS_231	VSS_321	M26
D4	VSS_232	VSS_322	M29
D5	VSS_233	VSS_323	M33
D9	VSS_234	VSS_324	M35
E11	VSS_235	VSS_325	M37
E12	VSS_236	VSS_326	M39
E17	VSS_237	VSS_327	M5
E20	VSS_238	VSS_328	M6
E23	VSS_239	VSS_329	M9
E26	VSS_240	VSS_330	N8
E29	VSS_241	VSS_331	P1
E32	VSS_242	VSS_332	P2
E36	VSS_243	VSS_333	P36
E7	VSS_244	VSS_334	P38
E8	VSS_245	VSS_335	P40
F1	VSS_246	VSS_336	P5
F10	VSS_247	VSS_337	P6
F13	VSS_248	VSS_338	R33
F14	VSS_249	VSS_339	R35
F17	VSS_250	VSS_340	R37
F2	VSS_251	VSS_341	R39
F20	VSS_252	VSS_342	R8
F23	VSS_253	VSS_343	T1
F26	VSS_254	VSS_344	T5
F29	VSS_255	VSS_345	T6
F35	VSS_256	VSS_346	U8
F37	VSS_257	VSS_347	V1
F39	VSS_258	VSS_348	V2
F5	VSS_259	VSS_349	V33
F6	VSS_260	VSS_350	V34
F9	VSS_261	VSS_351	V35
G11	VSS_262	VSS_352	V36
G12	VSS_263	VSS_353	V37
G17	VSS_264	VSS_354	V38
G20	VSS_265	VSS_355	V39
G23	VSS_266	VSS_356	V40
G26	VSS_267	VSS_357	V5
G29	VSS_268	VSS_358	W6
G34	VSS_269	VSS_359	Y5
G7	VSS_270	VSS_360	Y8
AY37	VSS_NCTF_03		
B3	VSS_NCTF_04		

GND GND

CHANNEL A DIMM

CH.A	SA1	SA0
DIMM0	L	L
DIMM1	L	H



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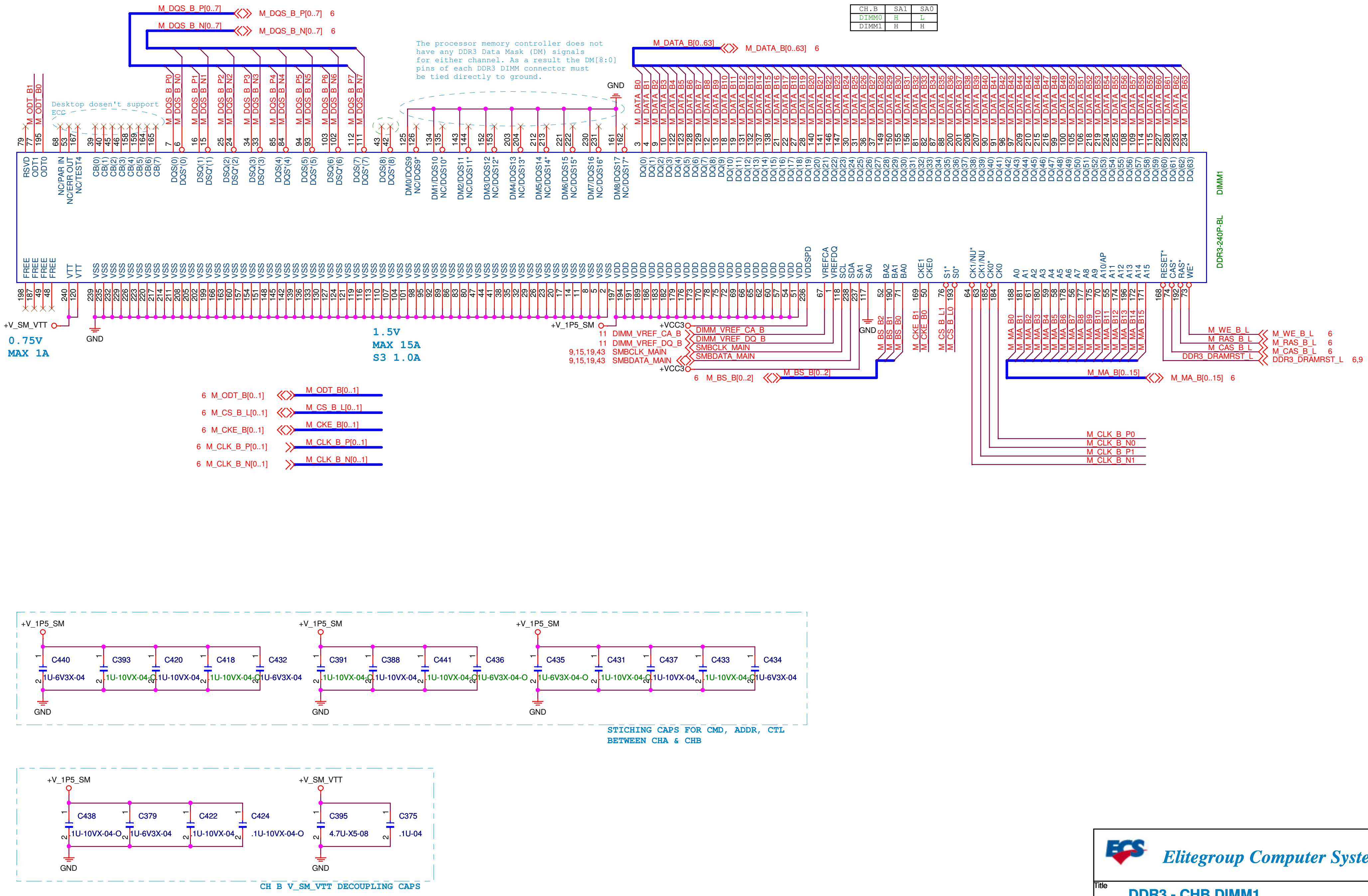
CHANNEL B DIMMs



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Title	DDR3 - CHB DIMM1
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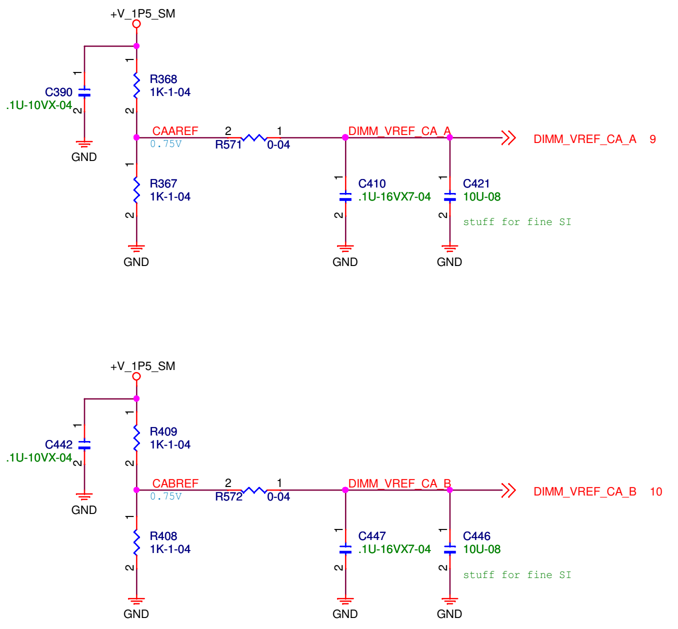
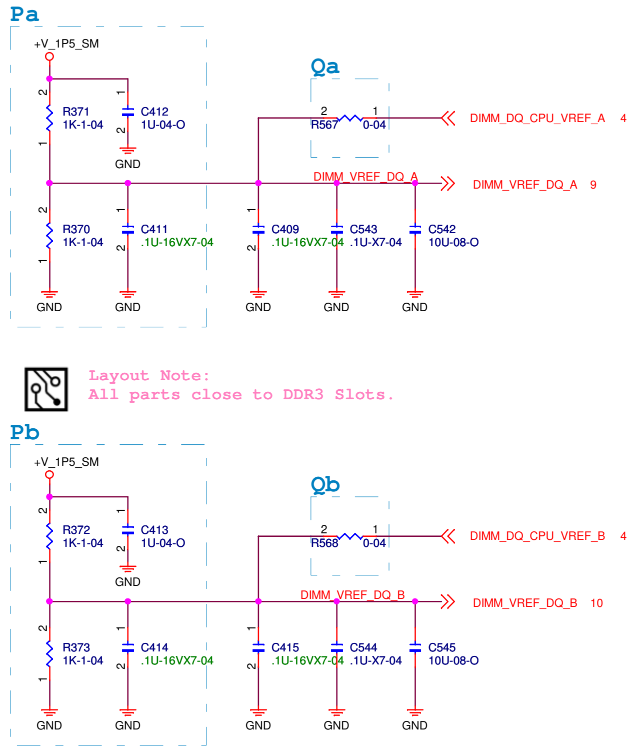


DIMM_VREF_CA Circuit



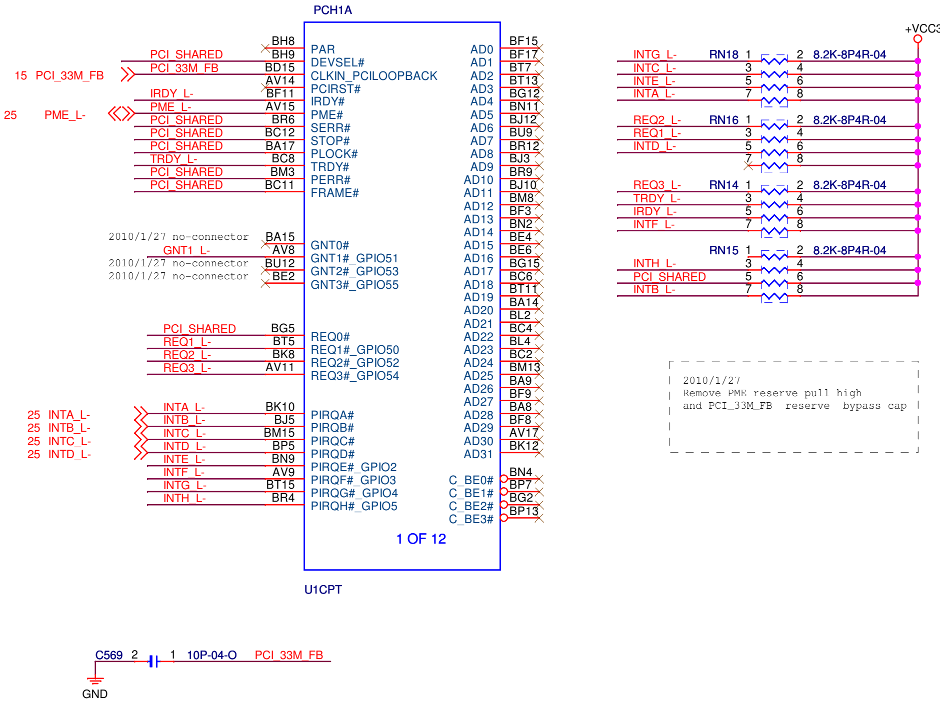
Layout Note:
All parts close to DDR3 Slots.

DIMM_VREF_DQ Control Mode:

Control Mode / Part	CPU	Divider
Pz	X	V
Qz	V	V

Z=a,b Default

DIMM_VREF_DQ Control Circuit



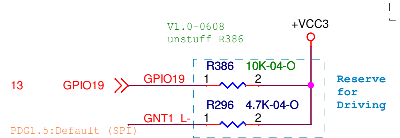
Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
* SPI	1	1

PCI Bridge

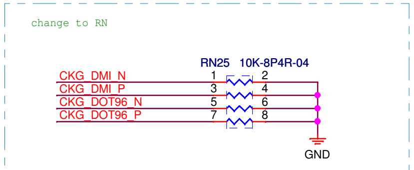
GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

2010/1/27
Remove reserve select strap

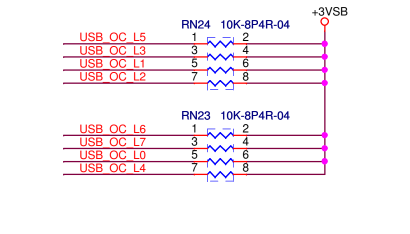


PDG1.5:Default (SPI)
Left both SATA1GP/GPIO19 and GNT1# floating.
No pull up required.

SATA1GP/ GPIO19, GNT1#	I/O	**Default (SPI)** Left both SATA1GP/GPIO19 and GNT1# floating. No pull up required. **Boot from PCI** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GNT1# Floating. **Boot from LPC** Connect both SATA1GP/GPIO19 and GNT1# to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.

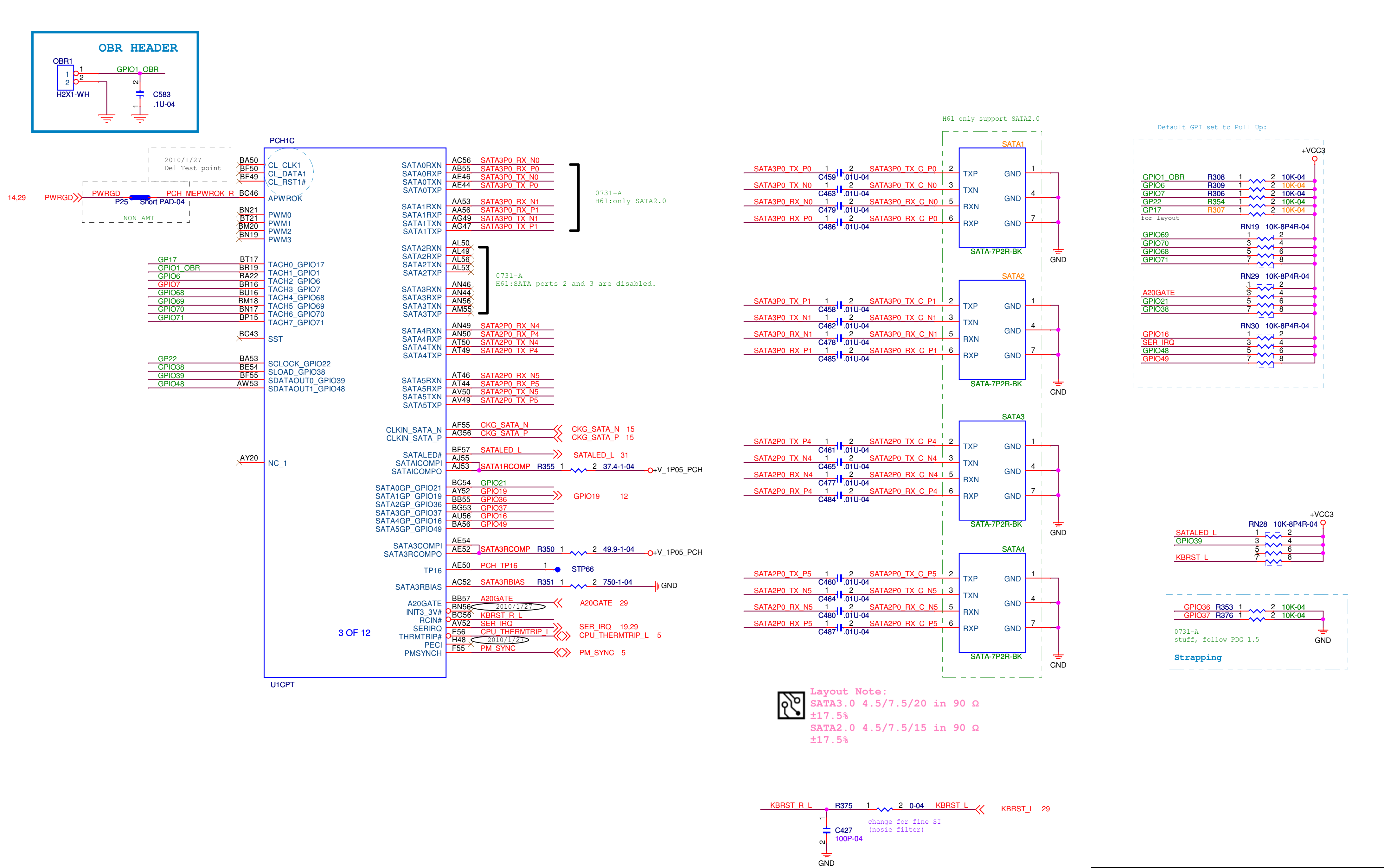


Stuff for Integrated Clock Mode



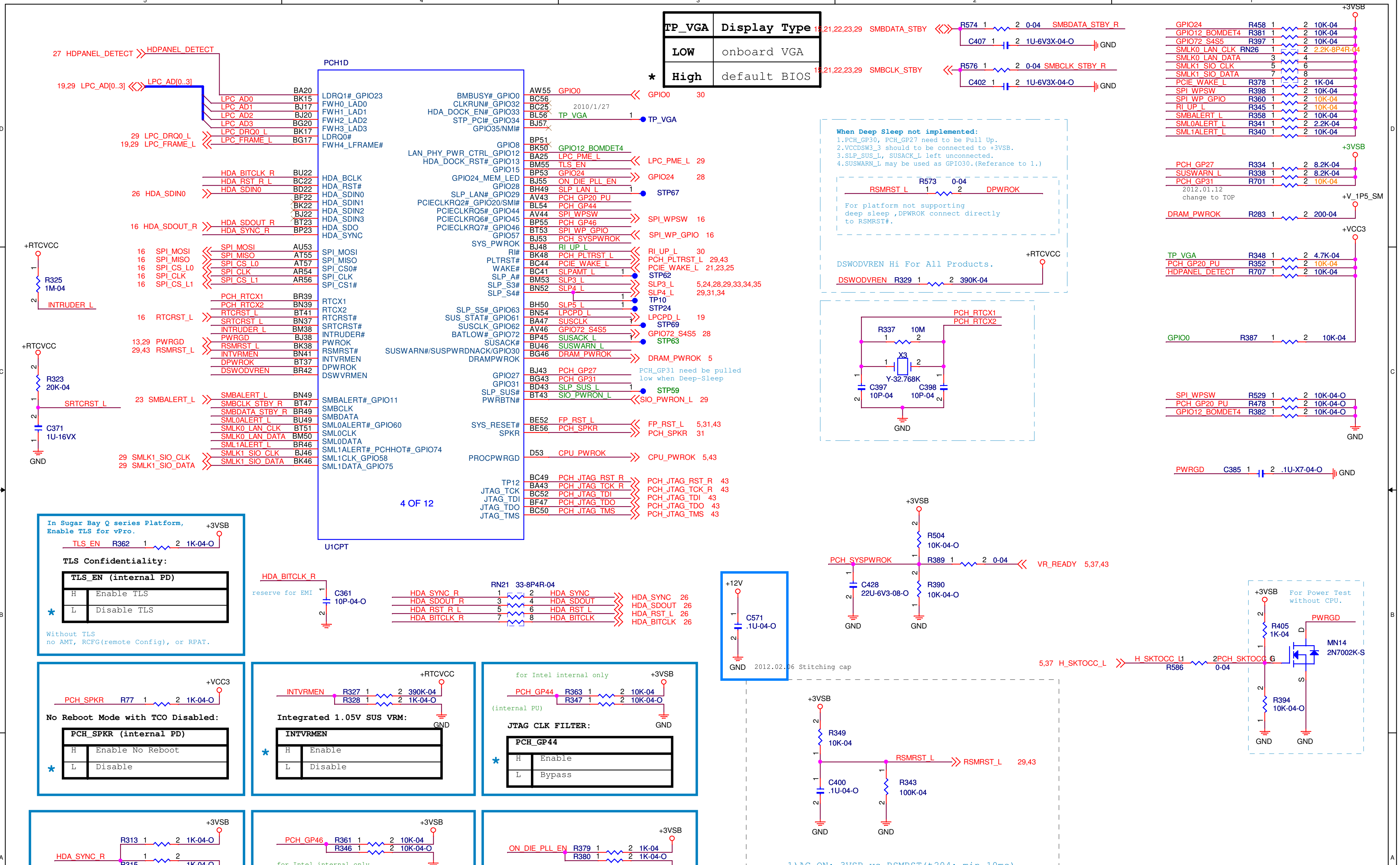
Elitegroup Computer Systems

Title	PCH_DMI/PCH_PE/USB	
Size Custom	Document Number H61H2-AM3	Rev A
Date: Thursday, March 01, 2012	Sheet 12 of 43	



Elitegroup Computer Systems

Title	PCH - SATA, SATA CONN	
Size: Custom	Document Number: H61H2-AM3	Rev: A
Date: Thursday, March 01, 2012	Sheet 13 of 43	

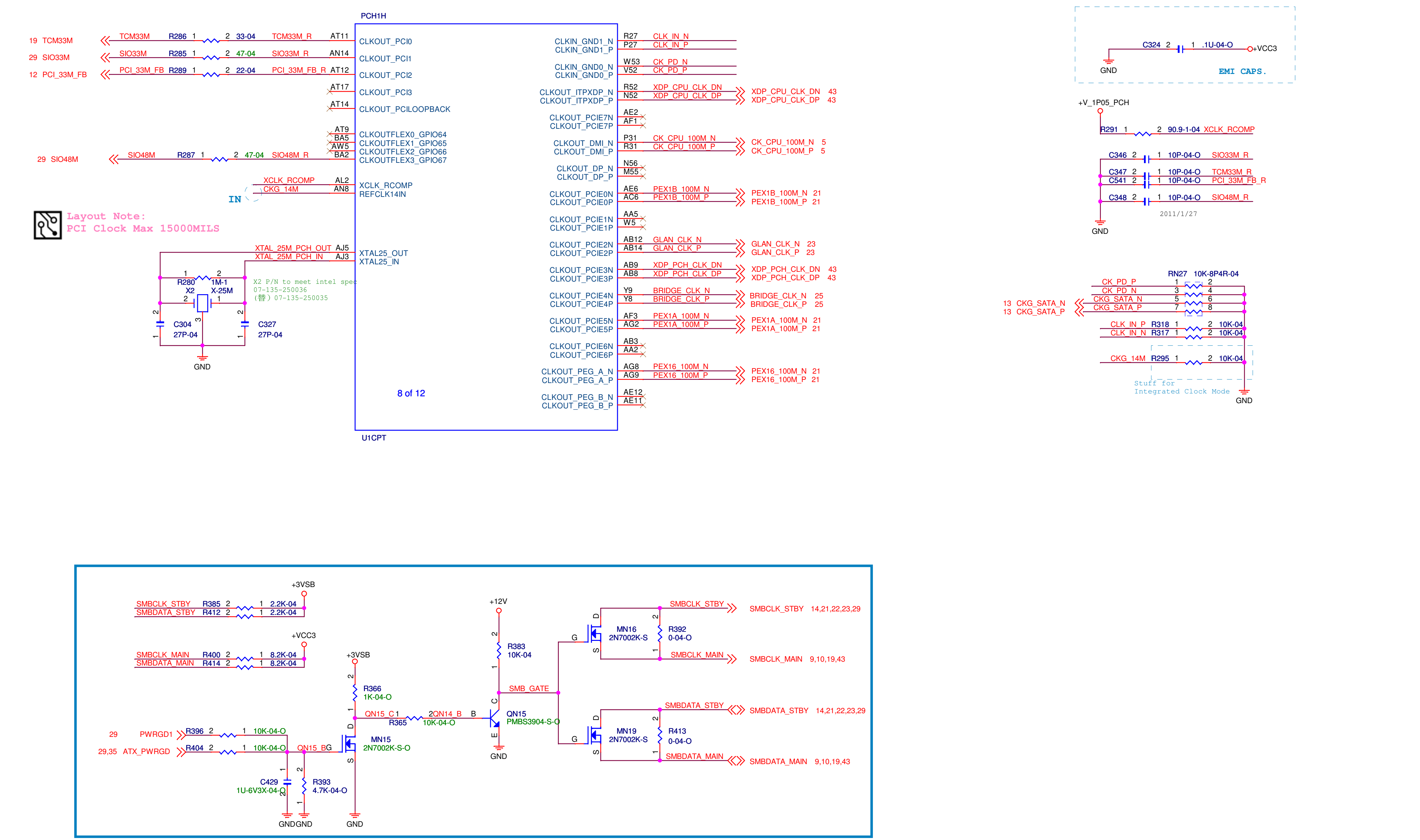


Elitegroup Computer Systems

Title: PCH - MISC, Strap Function

Size	Document Number	Rev
Custom	H61H2-AM3	A

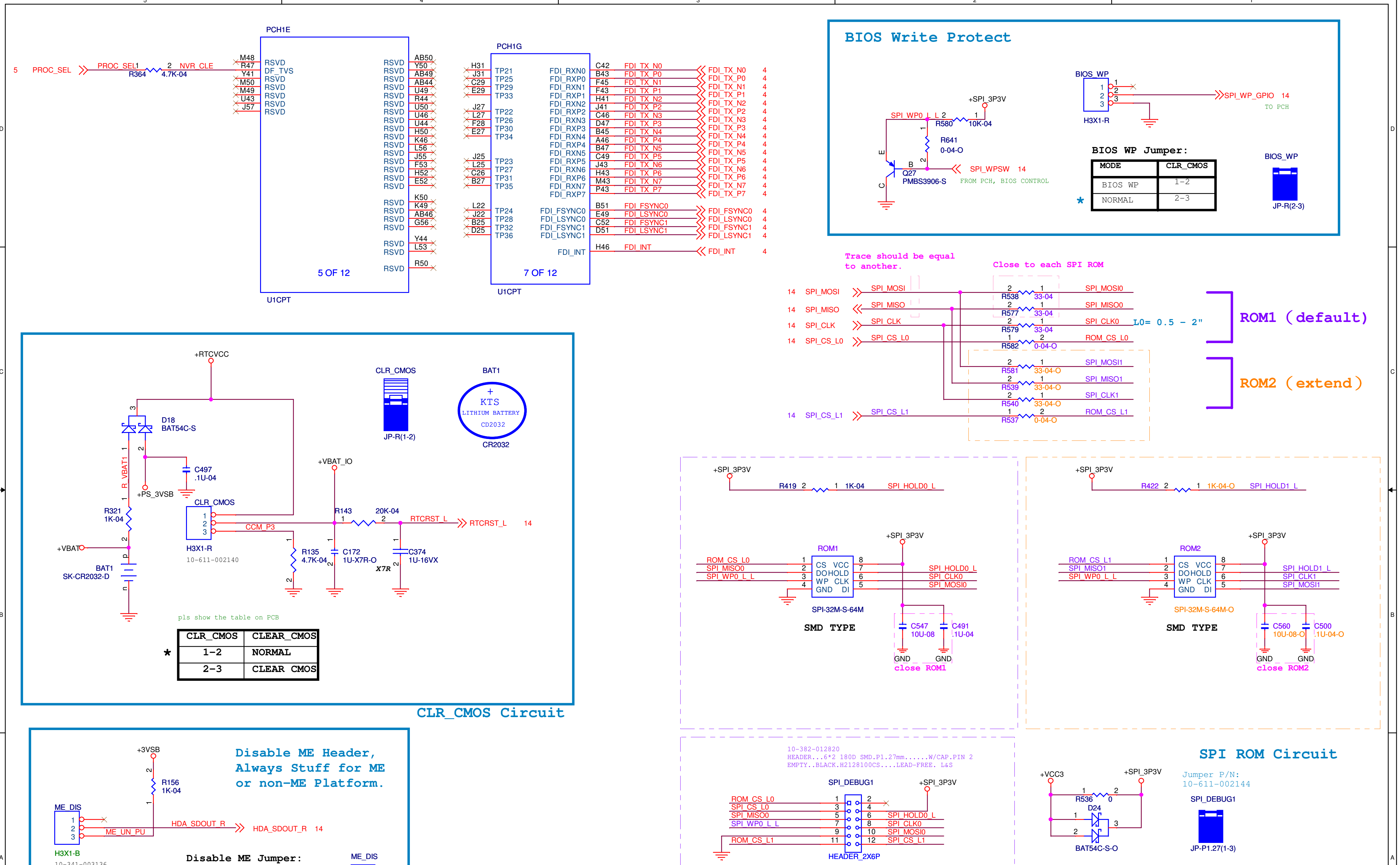
Date: Thursday, March 01, 2012 Sheet 14 of 43



SMBUS Logic Circuit

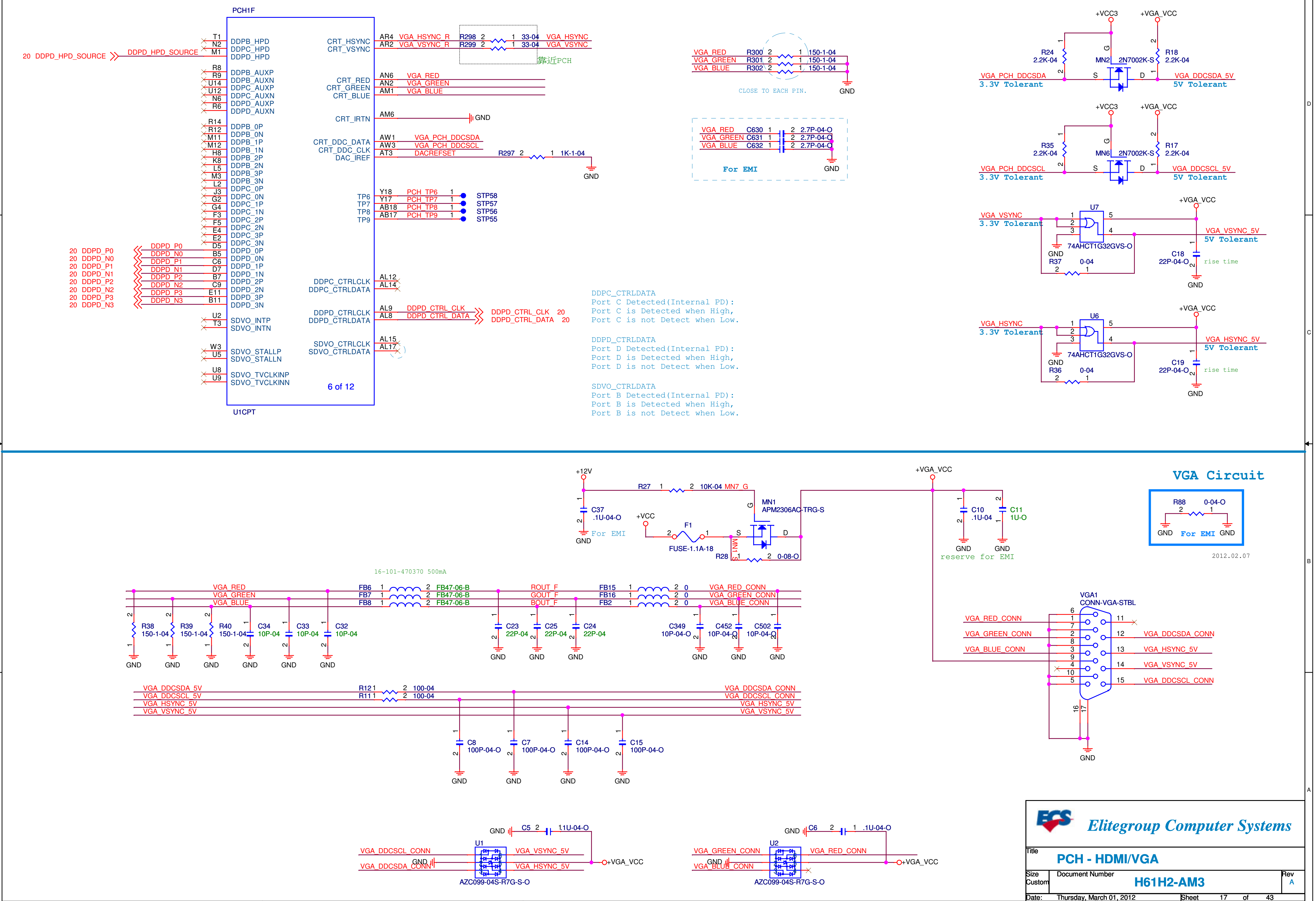
Elitegroup Computer Systems

Title	PCH - CLK IO,SMBu		
Size Custom	Document Number H61H2-AM3		Rev A
Date: Thursday, March 01, 2012	Sheet 15 of 43		



Elitegroup Computer Systems

Title	FDI,CLR_CMOS,ROM
Size: Custom	Document Number: H61H2-AM3
Rev	A
Date:	Thursday, March 01, 2012
Sheet	16 of 43



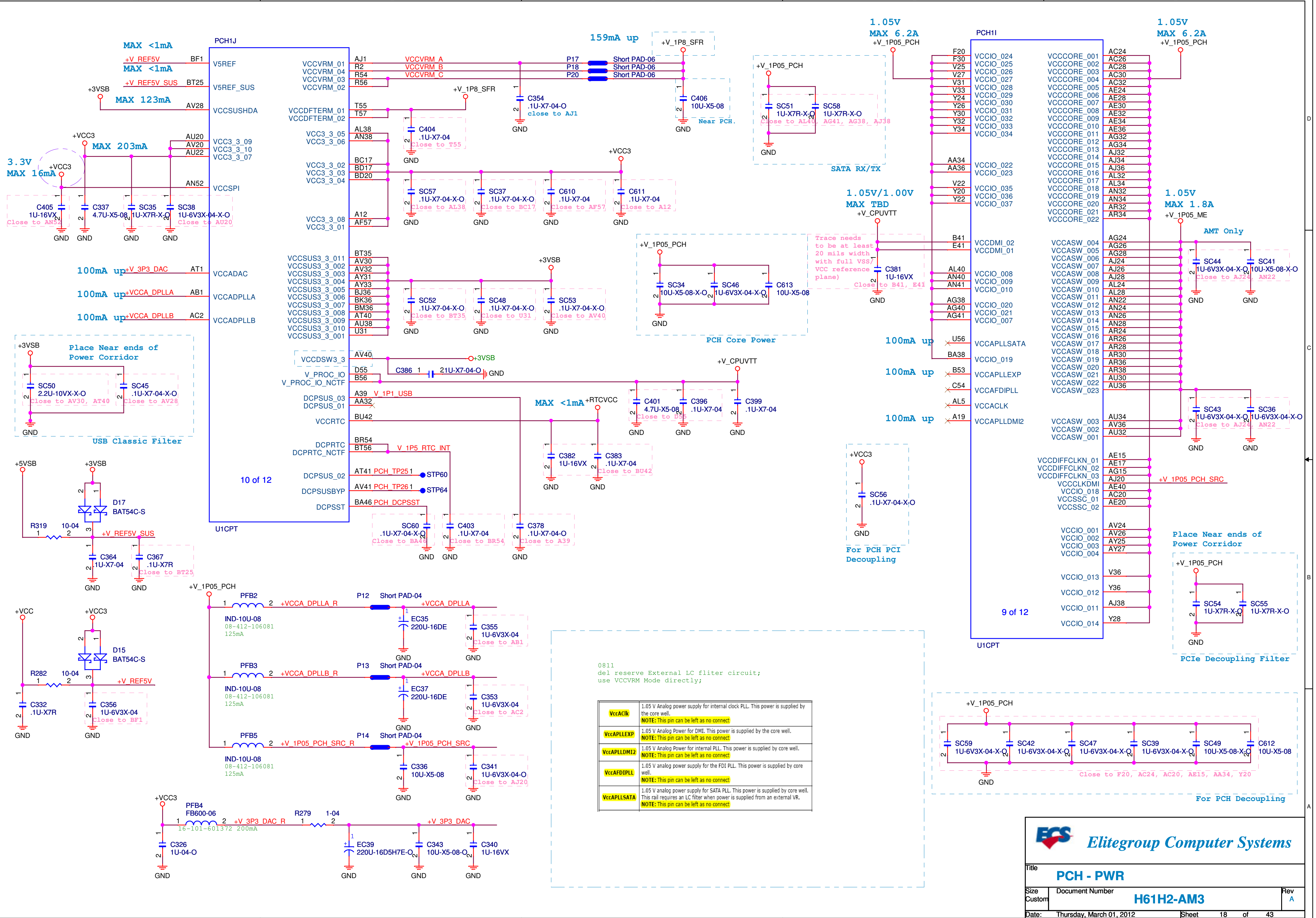
DDPC_CTRLDATA
Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.

DDPD_CTRLDATA
Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.

SDVO_CTRLDATA
Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

Elitegroup Computer Systems

Title	PCH - HDMI/VGA
Size: Custom	Document Number: H61H2-AM3
Rev	A
Date:	Thursday, March 01, 2012
Sheet	17 of 43



0811
del reserve External LC fliter circuit;
use VCCVRM Mode directly;

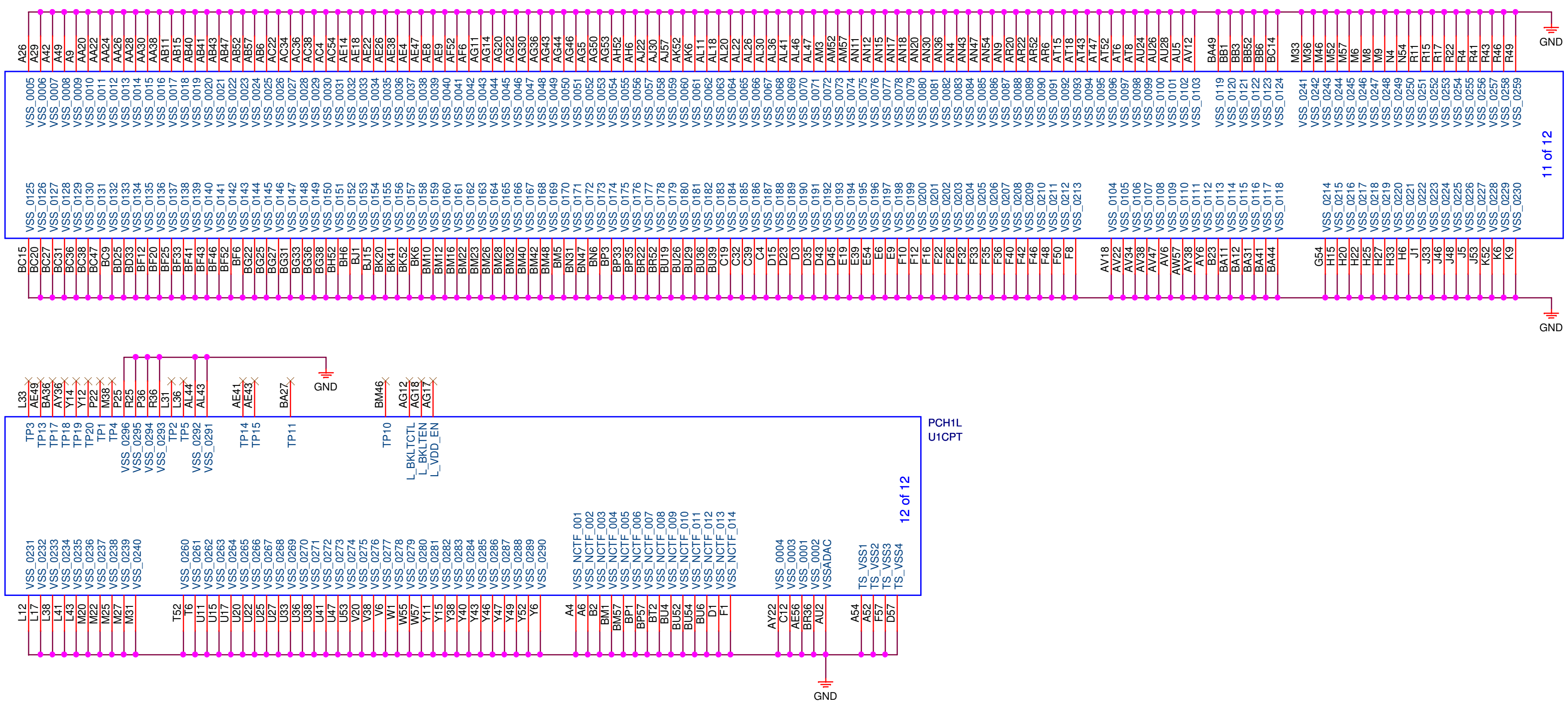
VccAClk	1.05 V Analog power supply for internal clock PLL. This power is supplied by the core well. **NOTE:** This pin can be left as no connect
VccAPLLEXP	1.05 V Analog Power for DMI. This power is supplied by the core well. **NOTE:** This pin can be left as no connect
VccAPLLDMI2	1.05 V Analog Power for internal PLL. This power is supplied by core well. **NOTE:** This pin can be left as no connect
VccAFDIPLL	1.05 V analog power supply for the FDI PLL. This power is supplied by core well. **NOTE:** This pin can be left as no connect
VccAPLLSATA	1.05 V analog power supply for SATA PLL. This power is supplied by core well. This rail requires an LC filter when power is supplied from an external VR. **NOTE:** This pin can be left as no connect

Elitegroup Computer Systems

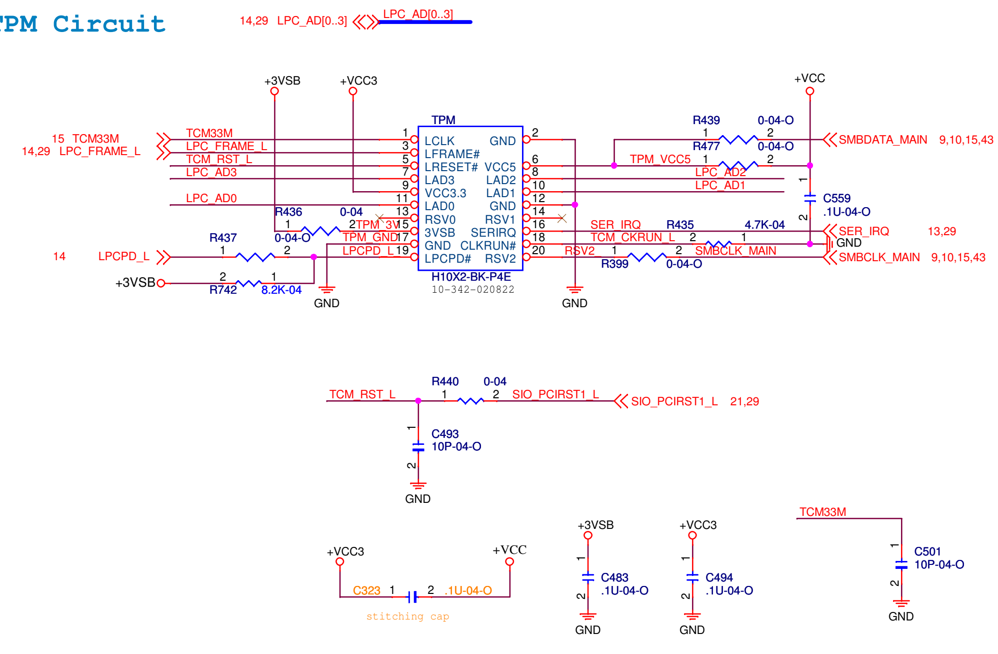
Title: PCH - PWR

Size: Custom | Document Number: H61H2-AM3 | Rev: A

Date: Thursday, March 01, 2012 |

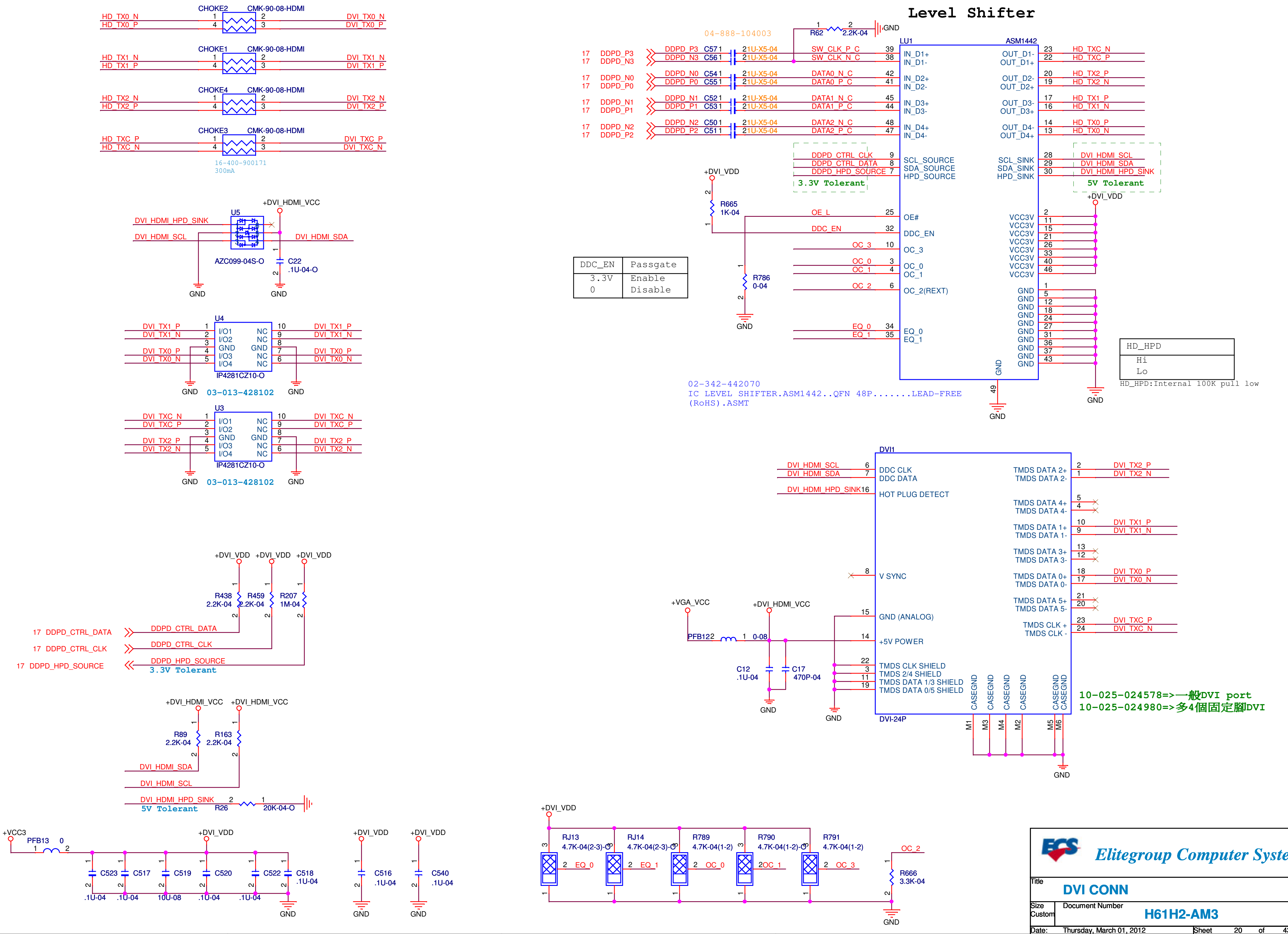


TPM Circuit



Elitegroup Computer Systems

Title	PCH - GND,TCM or TPM	
Size: Custom	Document Number: H61H2-AM3	Rev: A
Date: Thursday, March 01, 2012	Sheet 19 of 43	



DDC_EN	Passgate
3.3V	Enable
0	Disable

HD_HPD
Hi
Lo

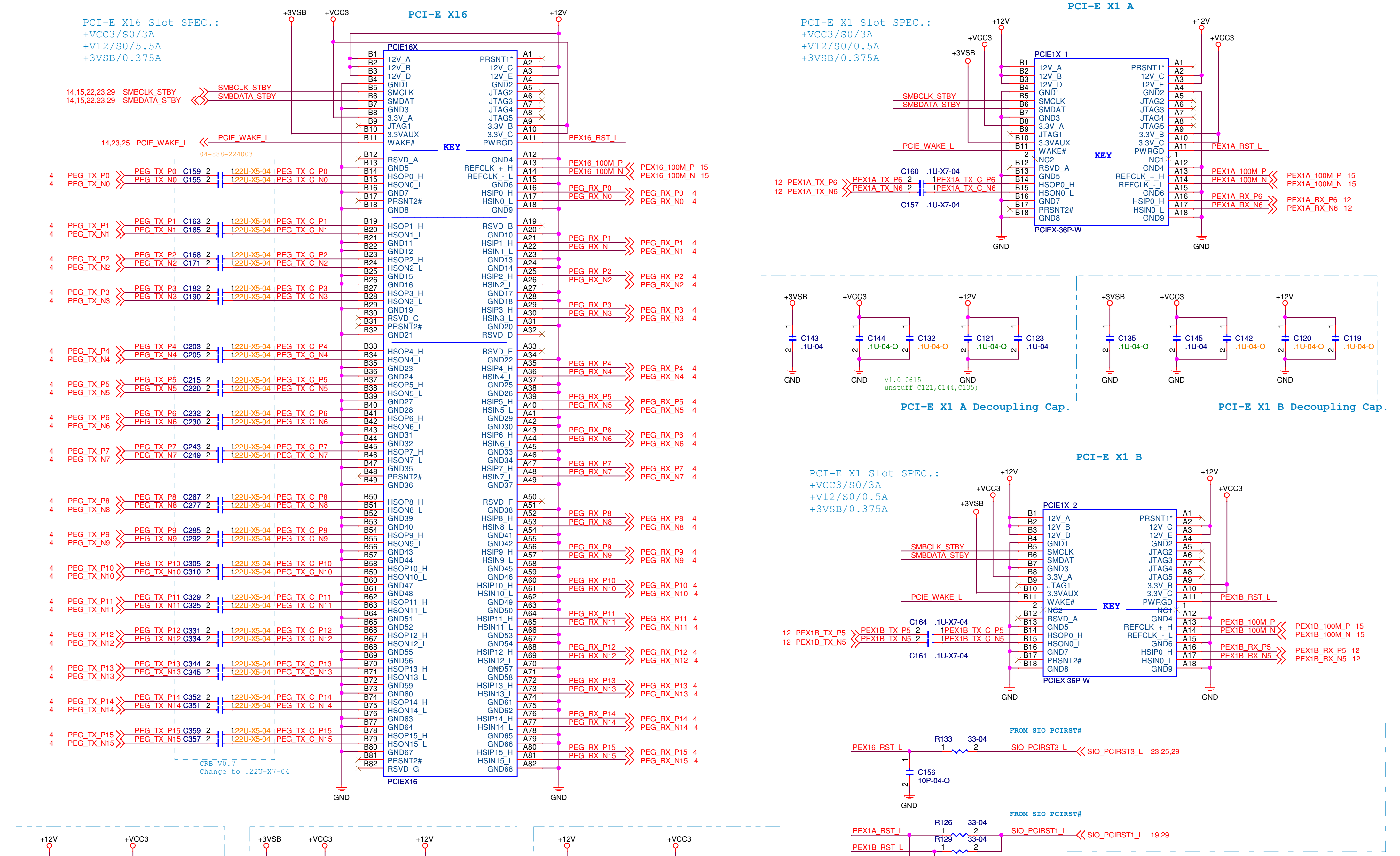
HD_HPD:Internal 100K pull low

Elitegroup Computer Systems

Title: DVI CONN

Size: Custom | Document Number: H61H2-AM3 | Rev: A

Date: Thursday, March 01, 2012 | Sheet 20 of 43



Elitegroup Computer Systems

Title	PCIE*16,PCIE*1 Slot
Size: Custom	Document Number: H61H2-AM3
Rev	A
Date:	Thursday, March 01, 2012
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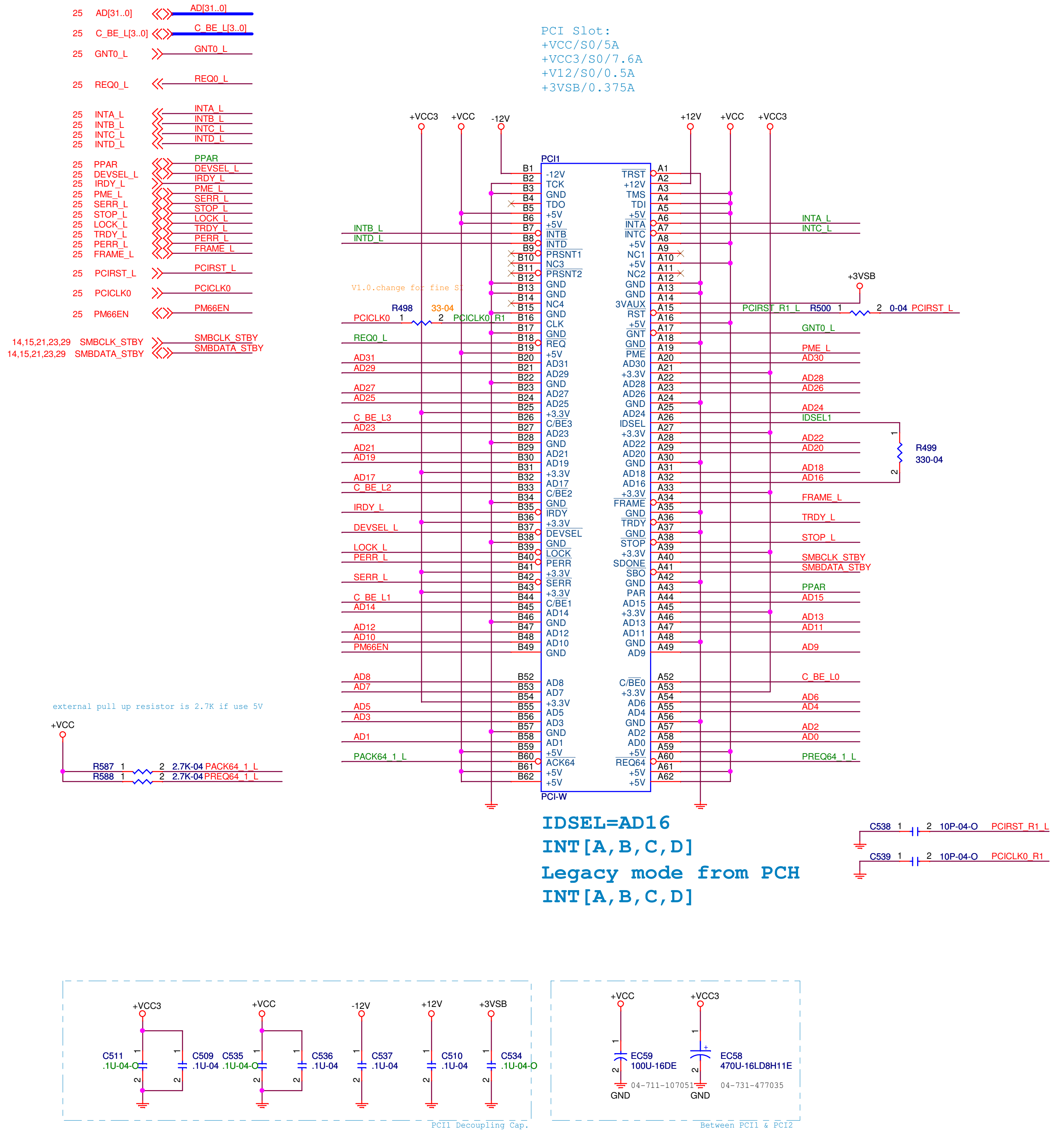
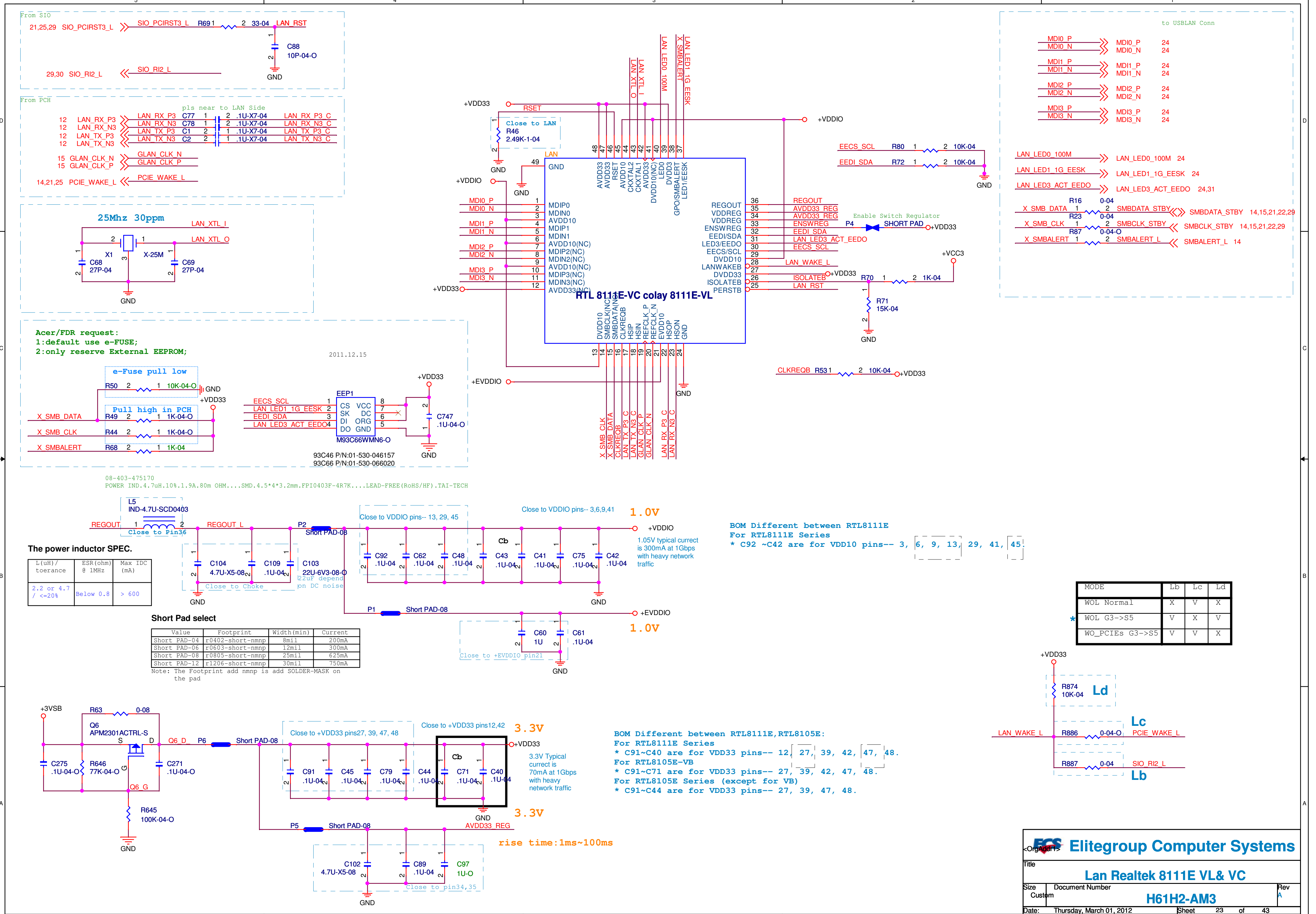


Elitegroup Computer Systems

Title: PCI Slot

Size: Custom | Document Number: H61H2-AM3 | Rev: A

Date: Thursday, March 01, 2012 | Sheet 22 of 43



The power inductor SPEC.

L(uH)/ toerance	ESR(ohm) @ 1MHz	Max IDC (mA)
2.2 or 4.7 / <=20%	Below 0.8	> 600

Short Pad select

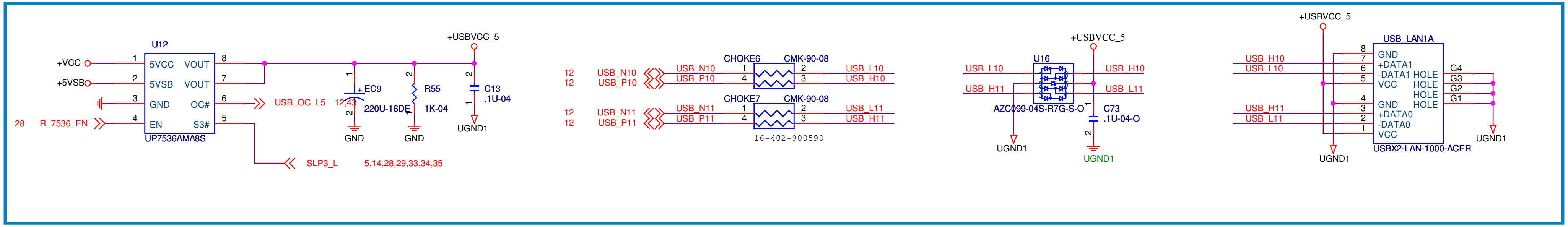
Value	Footprint	Width(min)	Current
Short PAD-04	r0402-short-nmnp	8mil	200mA
Short PAD-06	r0603-short-nmnp	12mil	300mA
Short PAD-08	r0805-short-nmnp	25mil	625mA
Short PAD-12	r1206-short-nmnp	30mil	750mA

Note: The Footprint add nmnp is add SOLDER-MASK on the pad

MODE	Lb	Lc	Ld
WOL Normal	X	V	X
* WOL G3->S5	V	X	V
WO_PCIEs G3->S5	V	V	X

<OrgAddr1> Elitegroup Computer Systems

Title	Lan Realtek 8111E VL& VC		
Size Custom	Document Number H61H2-AM3		Rev A
Date: Thursday, March 01, 2012	Sheet 23	of 43	

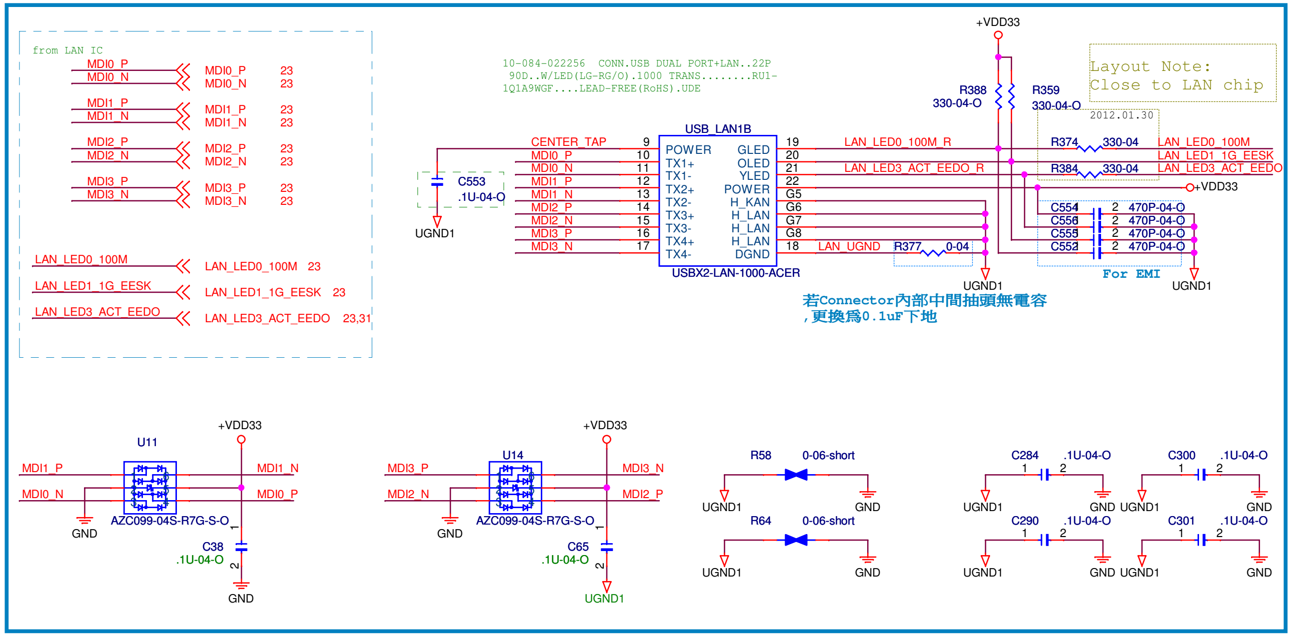


REAR SIDE 2 PORTS ON LANUSB CONN.

Acer Lan LED Status

Wake on LAN (WOL) set to ON ==> In BIOS and OS								
	LED		S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access:Blink	Blink	Blink	Blink	Blink	Blink	OFF
		Others:OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected:OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000:ON with A color:Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100:ON with B color:Green	Green	OFF	OFF	OFF	OFF	OFF
		10:OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blibking Others: OFF	Access: Blibking Others: OFF	OFF	OFF	OFF	OFF

Wake on LAN (WOL) set to OFF ==> In BIOS and OS								
	LED	S0	S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access:Blink	Blink	OFF	OFF	OFF	OFF	OFF
		Others:OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected:OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000:ON with A color:Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100:ON with B color:Green	Green	OFF	OFF	OFF	OFF	OFF
		10:OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	OFF	OFF



REAR SIDE 2 PORTS ON LANUSB CONN.

Table 12. Customized LEDs

	LINK			ACT/Full
Speed	Link 10M	Link 100M	Link 1000M	-
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
Not Defined	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

Note1: ACT means blinking TX and RX. LINK indicates Link 10M/100M/1000M.

Note2: There are four special modes:

Mode A: LED OFF Mode → *Set all bits to 0*

Mode B: Full Duplex LED Mode → *Set LED 0=0, and either LED 1 or LED 3 >0*
LED 0=Full Duplex
LED 1=Follow Customized LED rule
LED 3=Follow Customized LED rule

Mode C: Separated TX/RX Mode → *Set LED 0=0, LED1=0, LED3=1*
LED 0=TX
LED 1=RX
LED 3=LINK

Mode D: Separated Speed ACT Mode → *Set LED 0=0, LED1=1, LED3=1*
LED 0=10ACT
LED 1=100ACT
LED 3=1000ACT

Acer Spec:

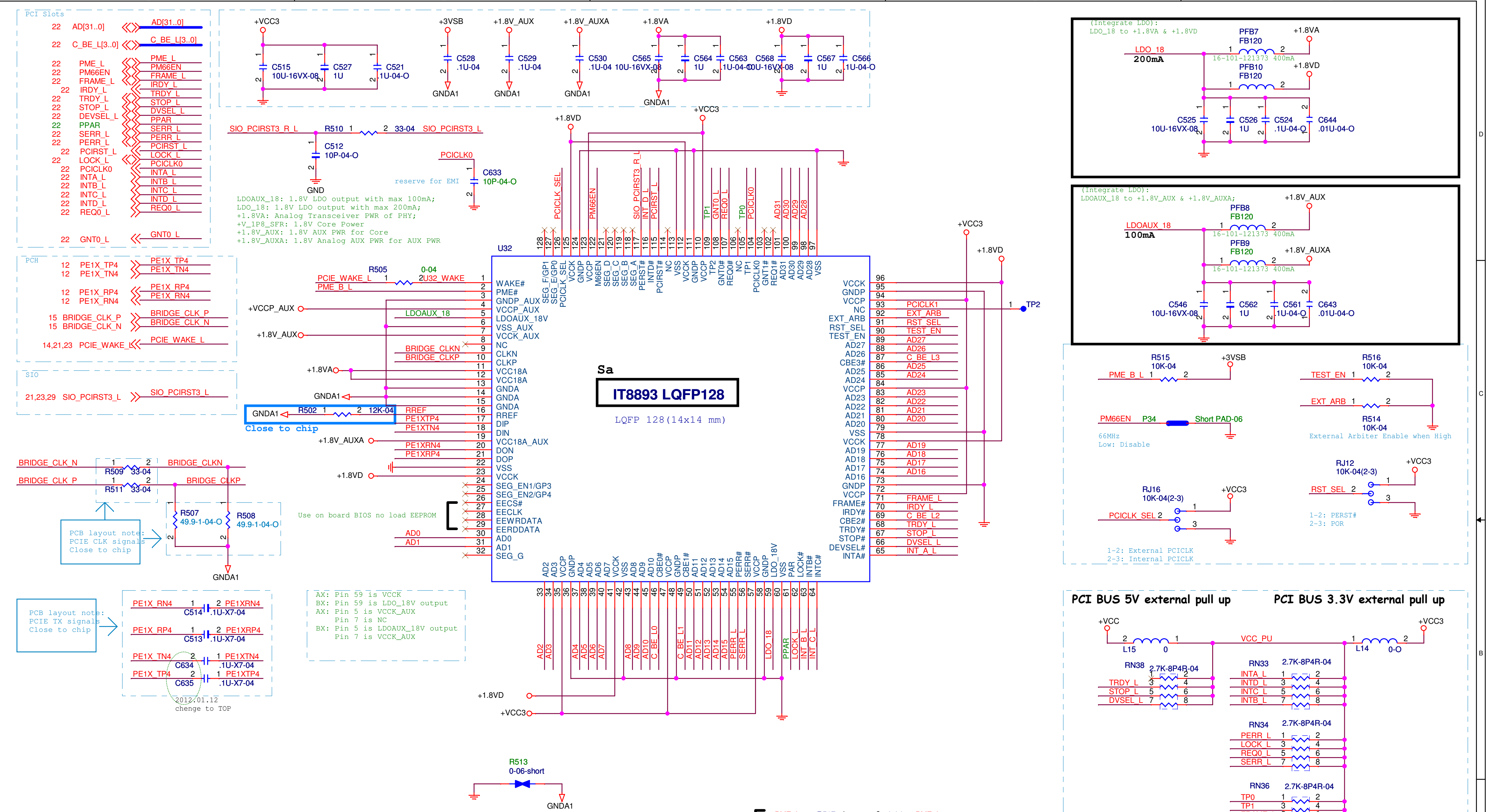
LAN LED	
Active	Green
LINK1000	Orange
LINK100	Green
LINK10	OFF

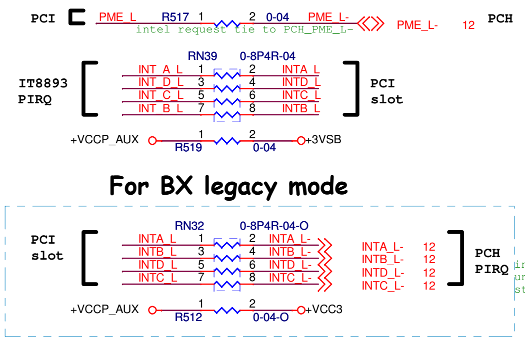
<OrgAddr1> Elitegroup Computer Systems

Title: USBLAN Connector

Size: Custom | Document Number: H61H2-AM3 | Rev: A

Date: Thursday, March 01, 2012 | Sheet 24 of 43



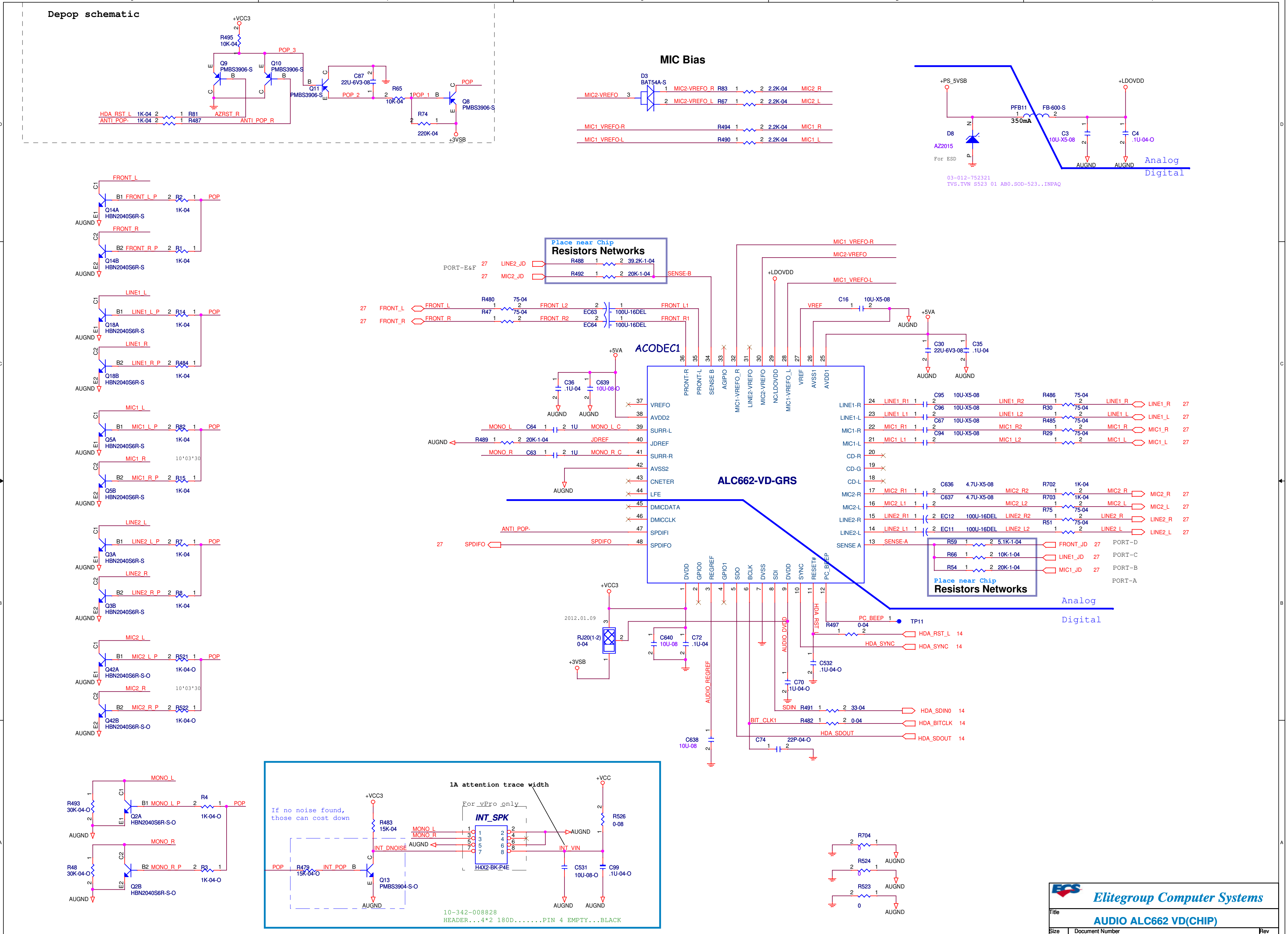


PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"

PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of C24;C25 is "0402"

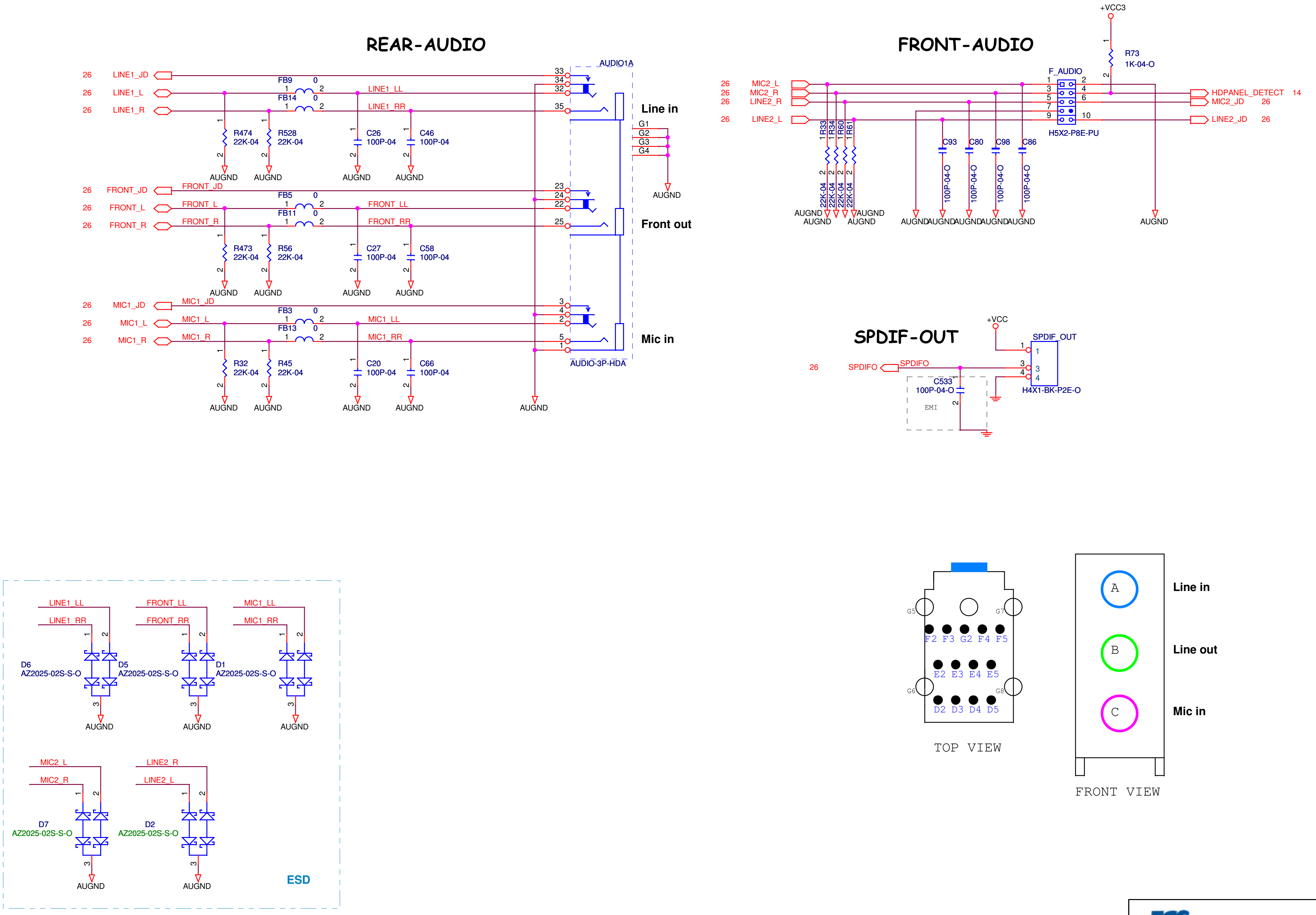
Elitegroup Computer Systems

Title	PCI Bridge	
Size Custom	Document Number H61H2-AM3	Rev A
Date: Thursday, March 01, 2012	Sheet 25 of 43	



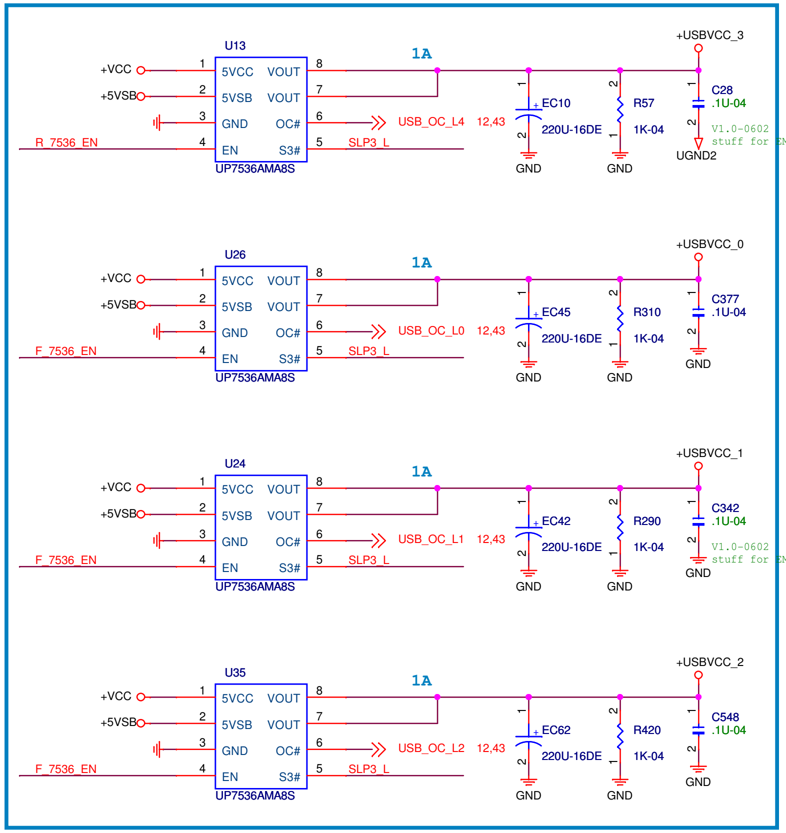
Elitegroup Computer Systems

Title	AUDIO ALC662 VD(CHIP)	
Size: C	Document Number: H61H2-AM3	Rev: A
Date: Thursday, March 01, 2012	Sheet 26 of 43	

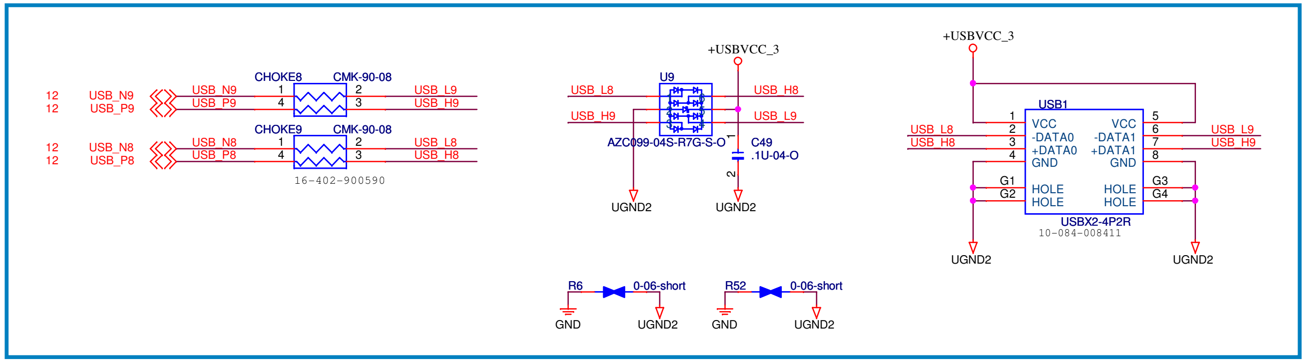


Elitegroup Computer Systems

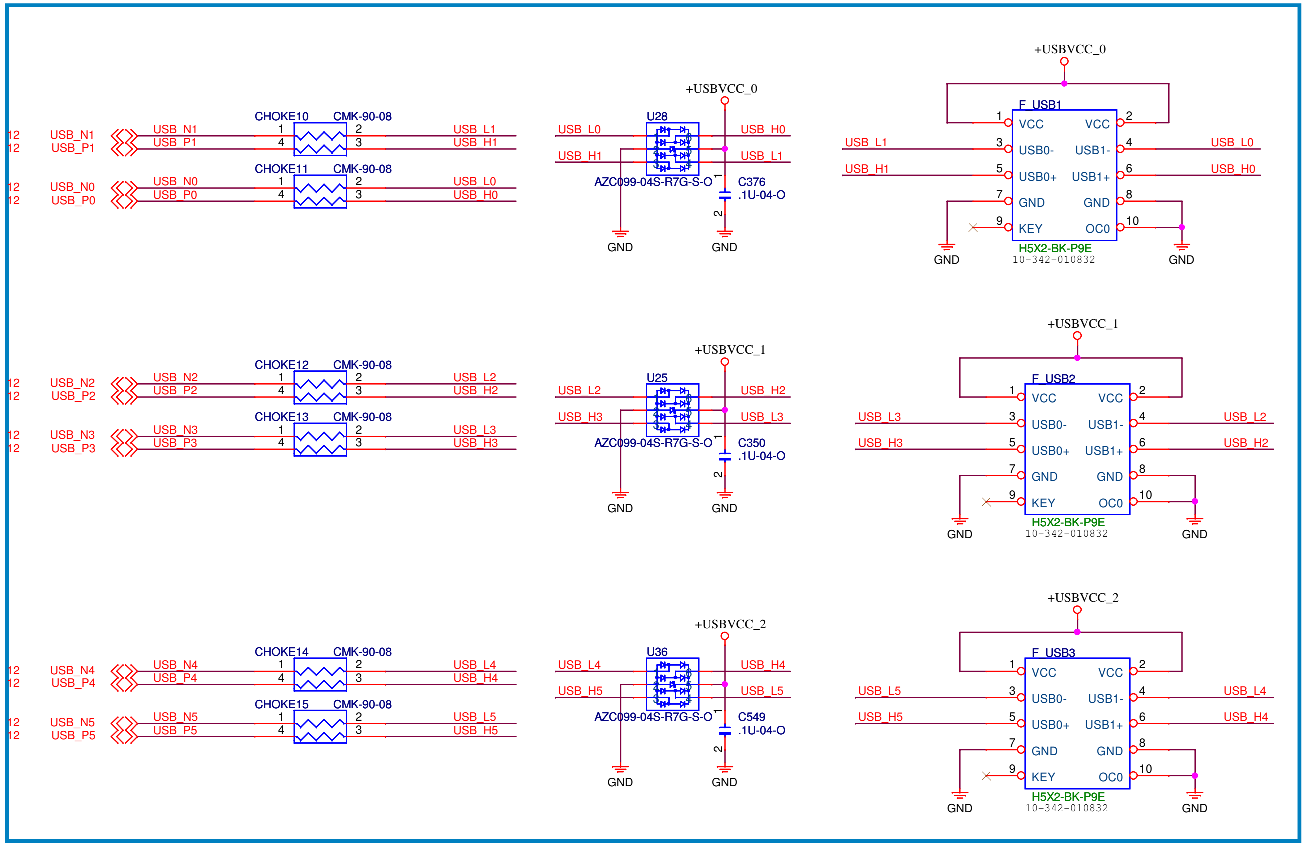
Title	Audio - CONN/HDR	
Size: Custom	Document Number: H61H2-AM3	Rev: A
Date: Thursday, March 01, 2012	Sheet 27 of 43	

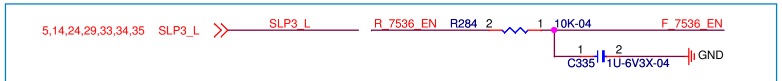


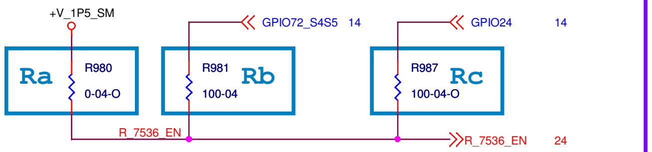
USB POWER CIRCUIT.



REAR SIDE 2 PORTS ON SINGLE USB CONN.

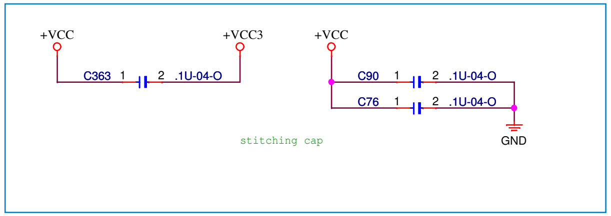


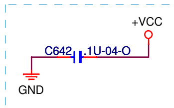




	uP7536 Enable use	Ra	Rb	RC	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm	N A	N A	0 Volt	Acer CONSUMER
*	PCH GPIO72 default High	N A	100ohm	N A	BIOS CONTROL	Acer COMMERCIAL
	PCH GPIO24 default Low	N A	N A	100ohm	BIOS CONTROL	Acer COMMERCIAL

Signal Name	Power Plane	During Reset[1]	Immediately after Reset[1]	S0/S1	S3	S4/S5	
GPIO72[9]	Suspend	High	High	Defined	Defined	Defined	
GPIO24	Suspend	Low	Low	Defined	Defined	Defined	Defined





STITCHING CAPS.

FRONT SIDE 4 PORTS on USB Header

Elitegroup Computer Systems

Title	USB - PWR/CONN/HDR
Size	Custom
Document Number	H61H2-AM3
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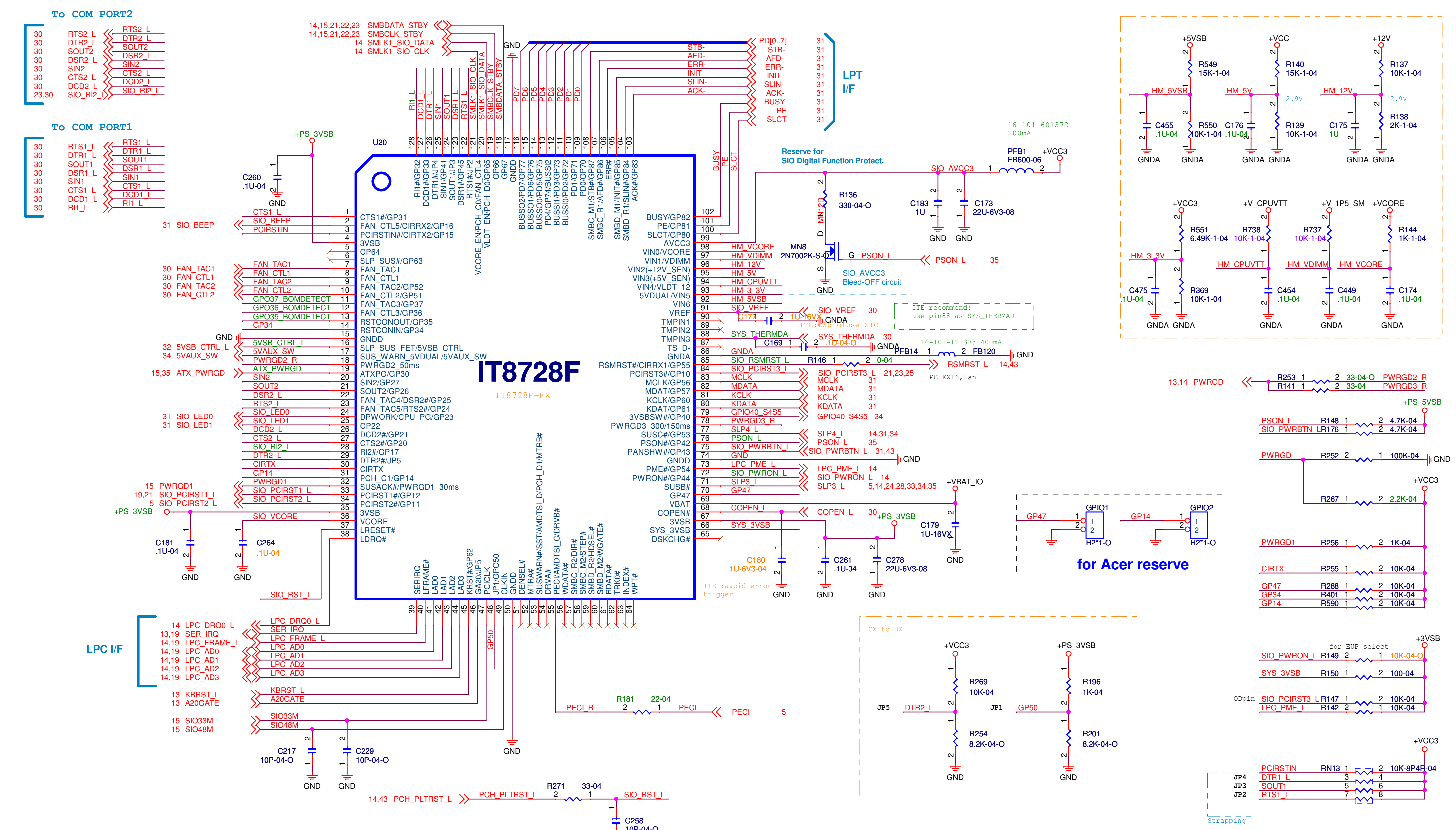

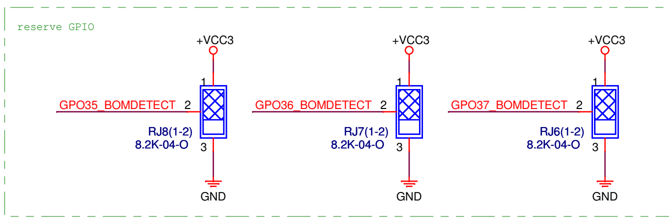

Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
JP1 Pin 48	DSW_EUP_SEL	Internal 3VSB_OK	1	EUP
			0	DSW
JP2 Pin 122	WDT_EN	Internal VCC-OK/ LRESET#	1	Disable WDT to rest PWROK
			0	Enable WDT to rest PWROK
JP3 Pin 124	FAN_CTL_SEL	Internal VCC-OK	1	The default value of EC Index 63h/6Bh/73h is 80h.
			0	The default value of EC Index 63h/6Bh/73h is 00h.
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
JP5 Pin 29	UOVMODE_SEL	Internal VCC-OK	1	Notice Type
			0	Force Type

FAN_CTL_SEL
80h--> default 50%
FFh--> default 0%
00h--> default 100%
40h--> default 75%

Elitegroup Computer Systems

Title: SIO - IT8728 FX

Size	Document Number	Rev
Custom	H61H2-AM3	A

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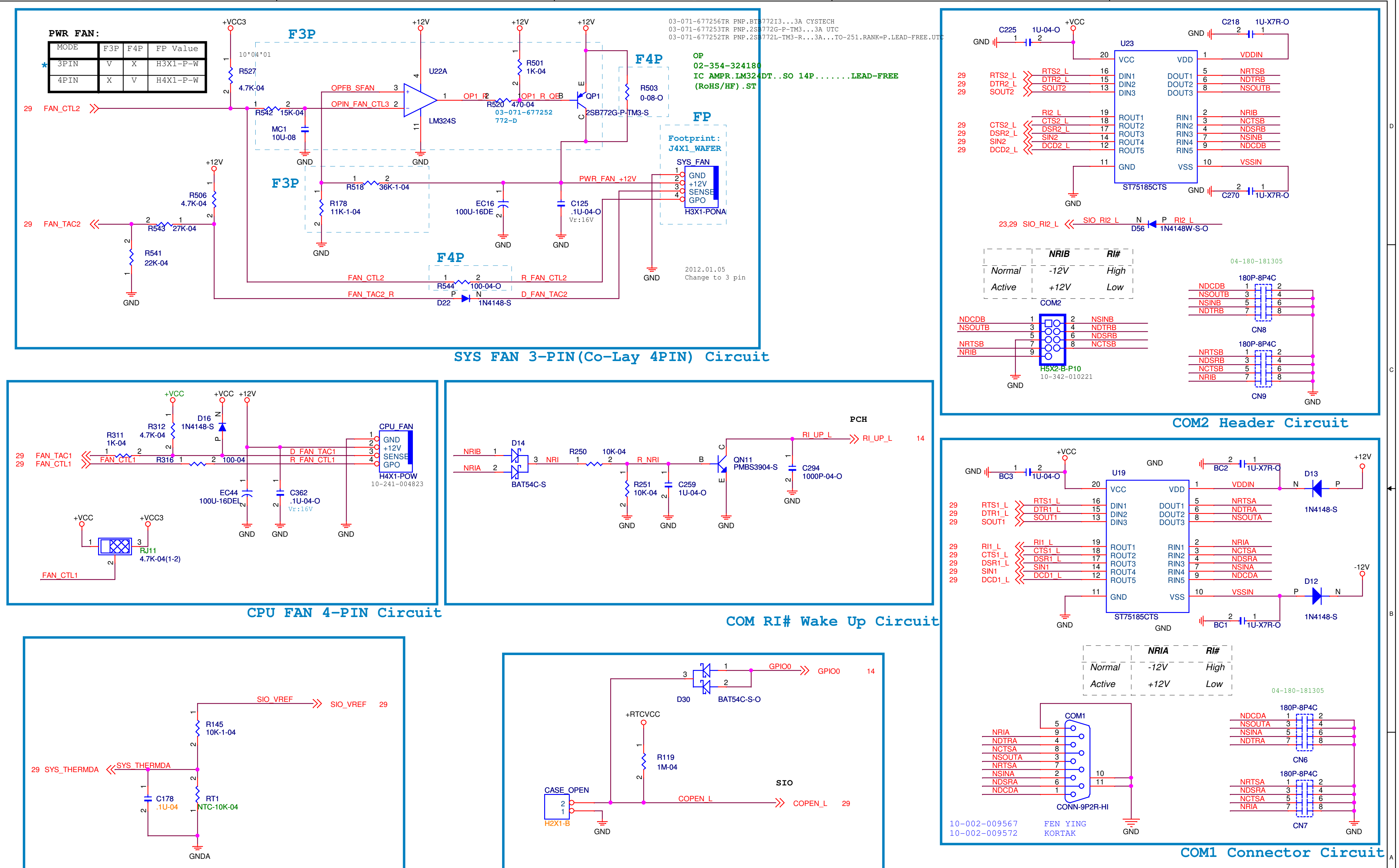

PWR FAN:

MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

	NRIB	RI#
Normal	-12V	High
Active	+12V	Low

	NRIA	RI#
Normal	-12V	High
Active	+12V	Low

Elitegroup Computer Systems

Title: **FAN, COM, CASE_OPEN, THERM**

Size	Document Number	Rev
Custom	H61H2-AM3	A

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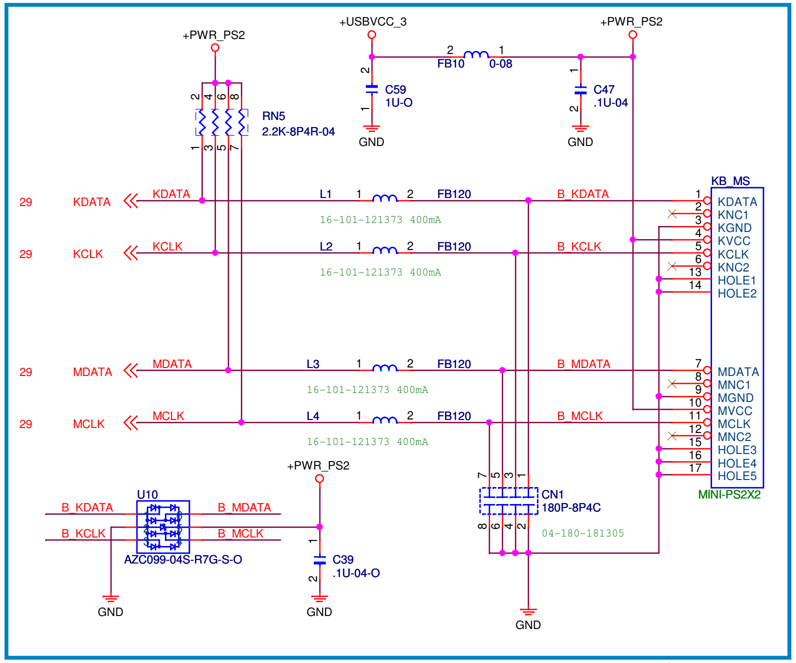
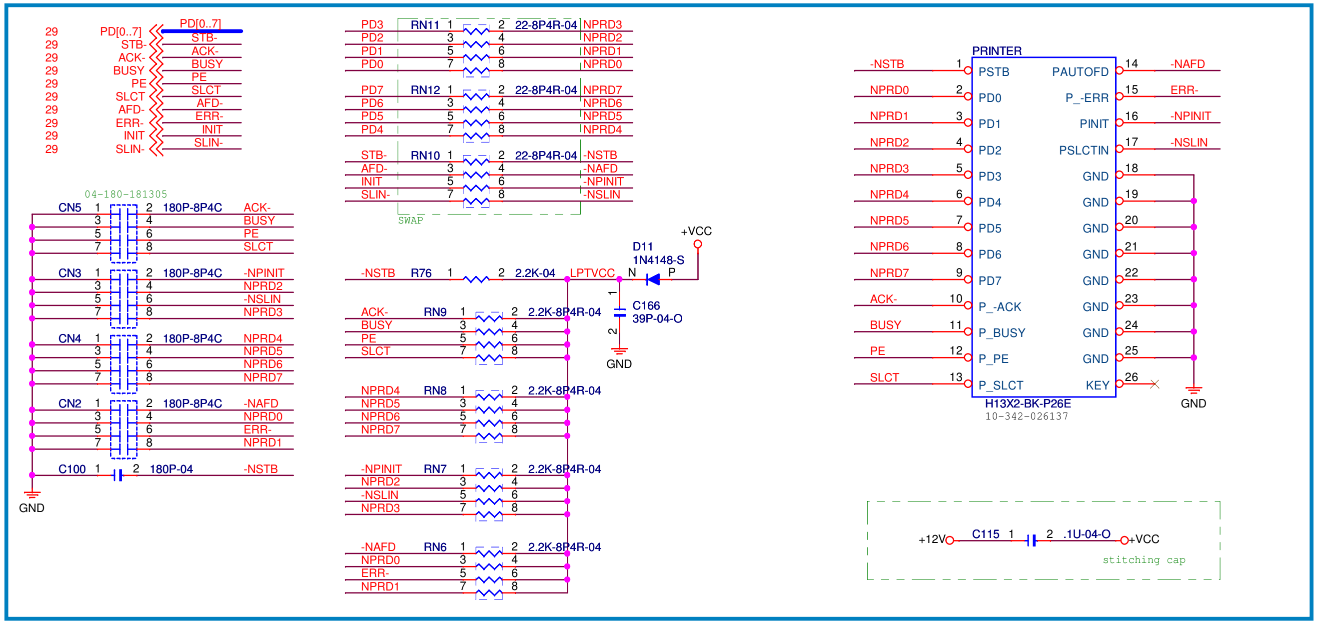
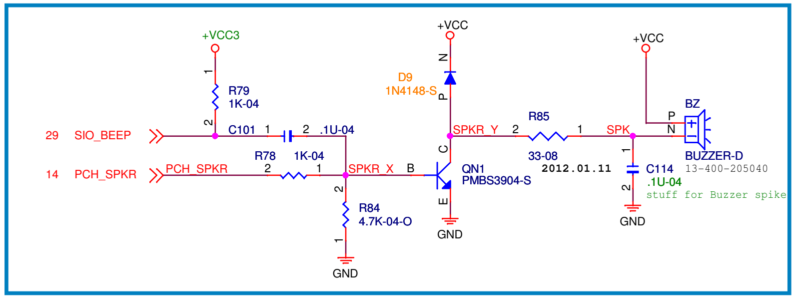


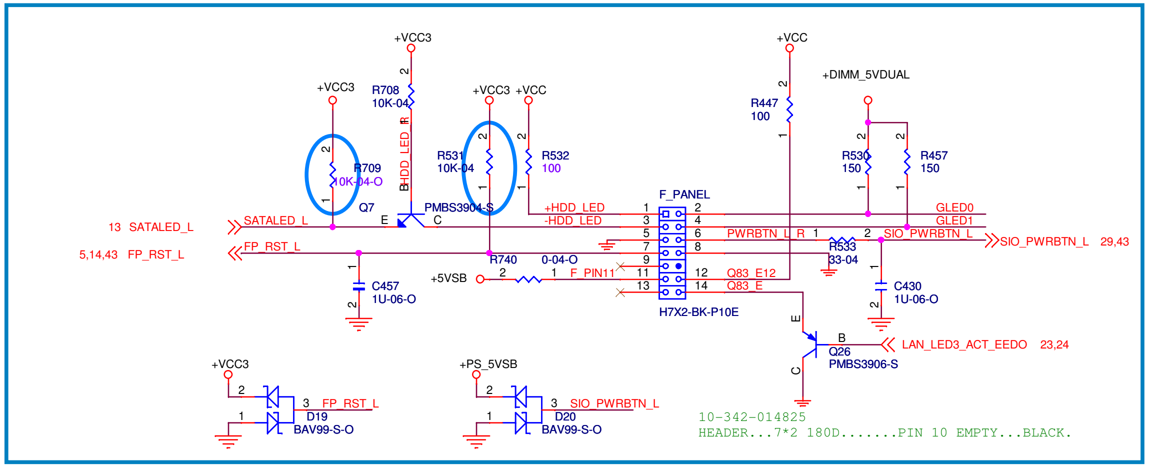
PS2 Circuit



LPT Header Circuit

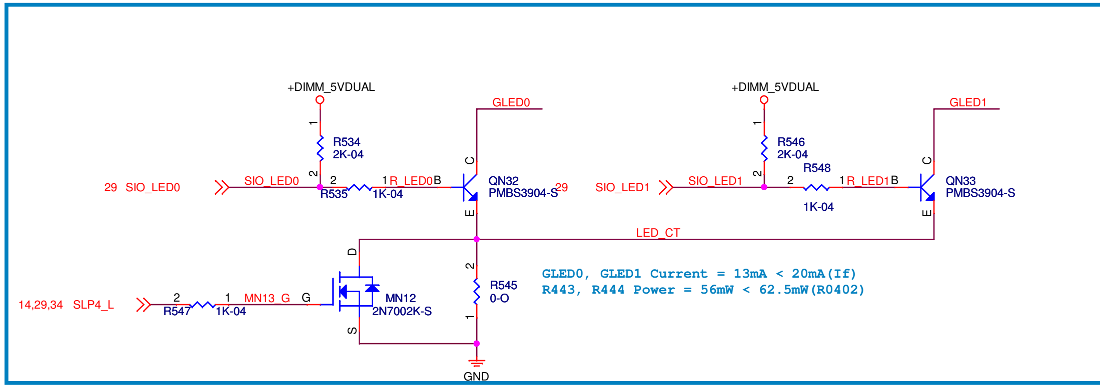


Buzzer Circuit



Front Panel Circuit

PWR_LED Circuit



	LED	S0	S1	S3	S4/S5
Front Side	PWR LED (Single Color)	Always ON	Always ON	Blinking	OFF
	Storage LED (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF
	LAN LED (ACTIVE) (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF

ECS Elitegroup Computer Systems

Title	F_PANEL, BUZ, PS2, LPT
Size / Document Number	H61H2-AM3
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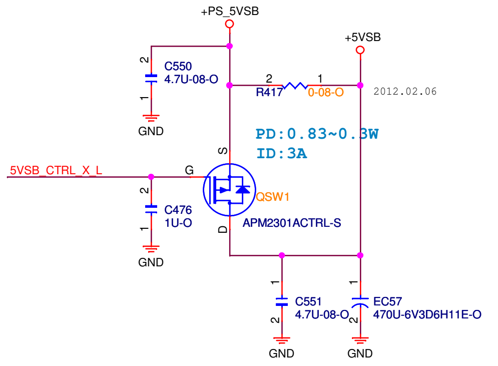
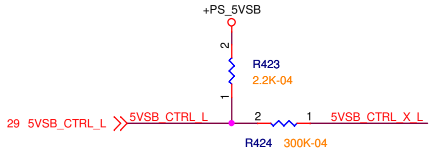
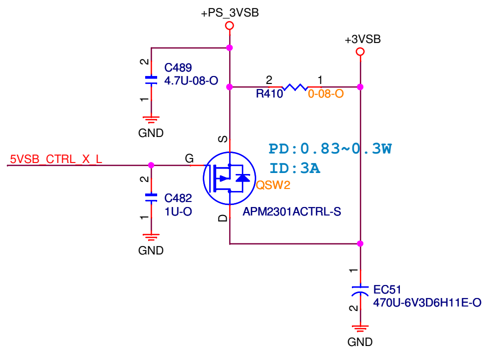
EuP Lot6 Power Saving Circuit





add R51 to Fix EUP enable STBY drop



Layout Note:
Close to ATX 24P2R Connector.

EuP Lot6 2013 0.5W:

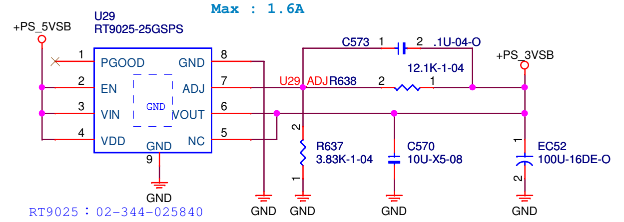
PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF

*** China one Enery Saving Spec**

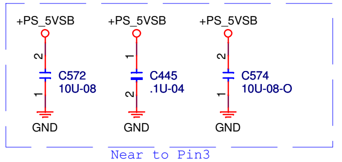
Customer	S3	S5
TF	< 0.4A	< 0.18A
FDR	< 0.3A	< 0.15A

+3VSB Circuit

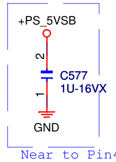
Pd = 2.72 W
Max : 1.6A



RT9025：02-344-025840



Near to Pin3



Near to Pin4

3VSB Non-EuP Lot6 Mode:

Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
TPM(WPCT210)	50mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

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Title	DC/DC 3VDUAL,EUP
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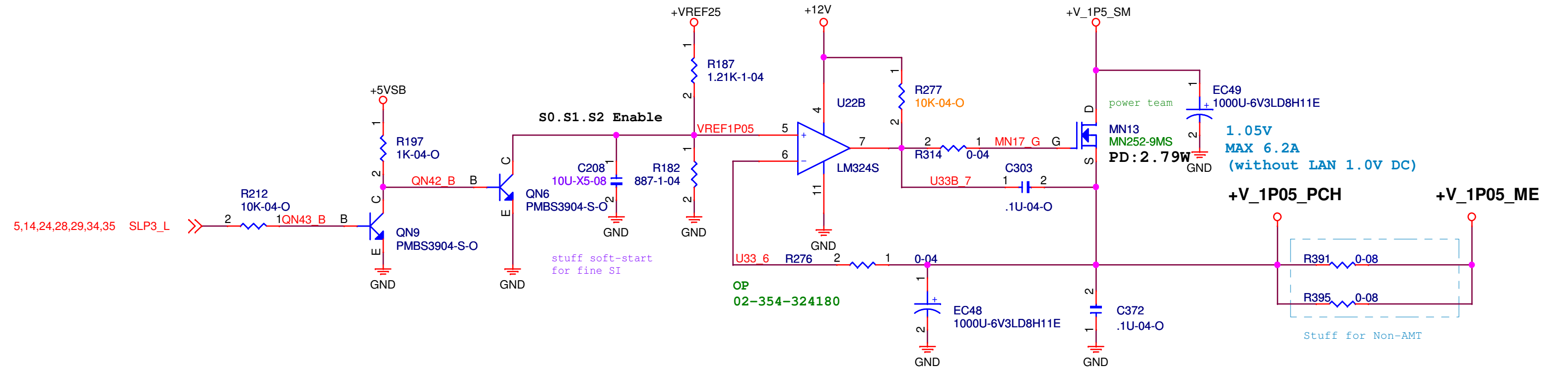
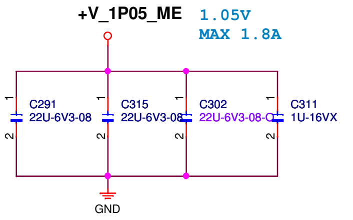
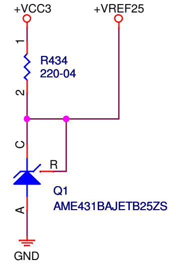
V1P05_PCH

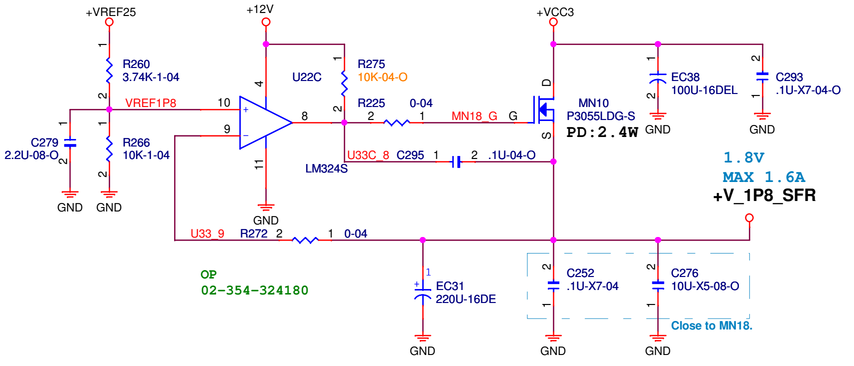




VREF25



V1P8_SFR(1.5A max)



del 1.05V ME power

V1P05_ME

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Title	DC/DC V1P05_PCH,ME/V1P8_SFR	
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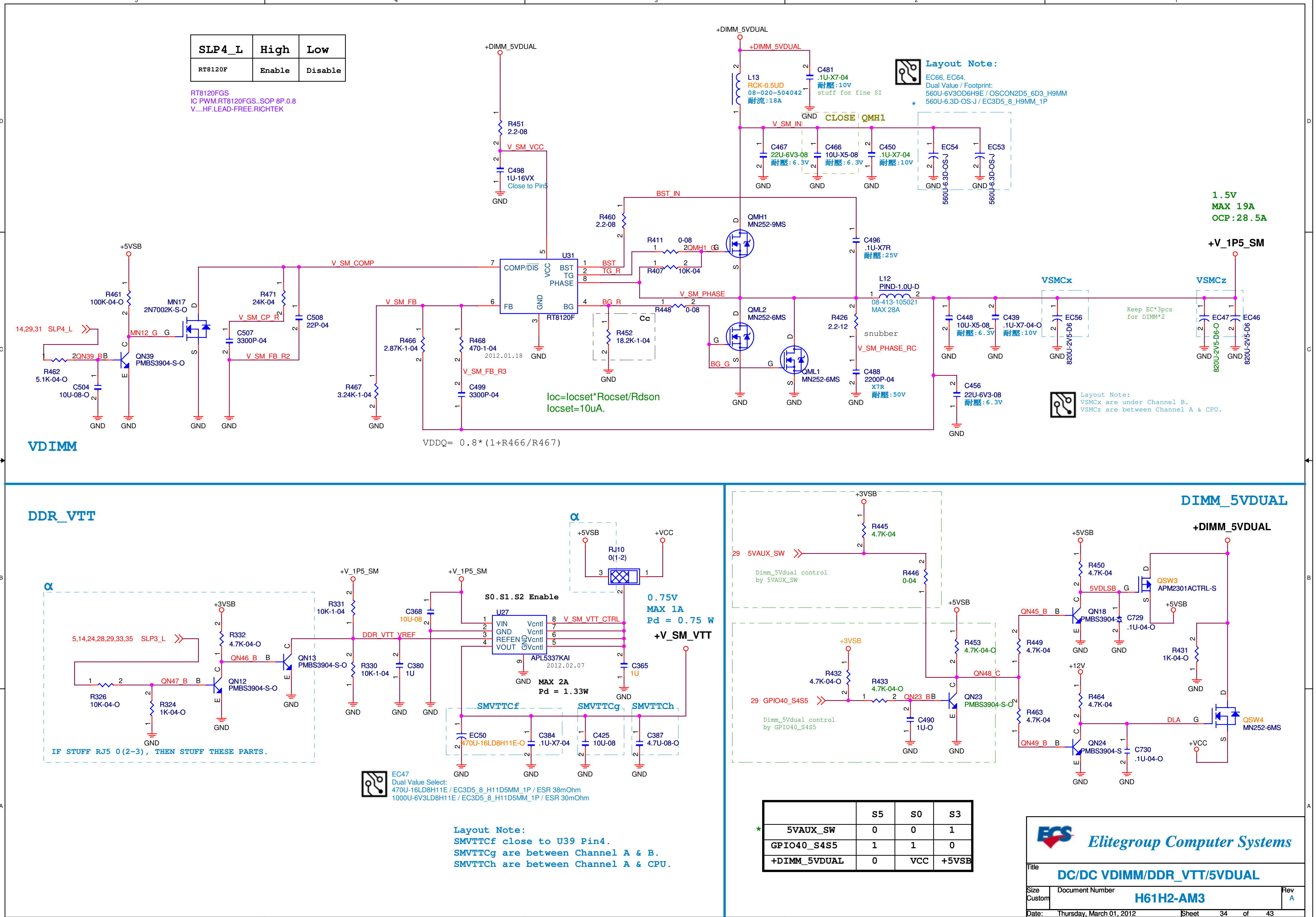

SLP4_L	High	Low
RT8120F	Enable	Disable

Layout Note:
SMVTTCf close to U39 Pin4.
SMVTTCg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

	S5	S0	S3
5VAUX_SW	0	0	1
GPIO40_S4S5	1	1	0
+DIMM_5VDUAL	0	VCC	+5VSB

Elitegroup Computer Systems

Title	DC/DC VDIMM/DDR_VTT/5VDUAL	
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stuff VSAGz

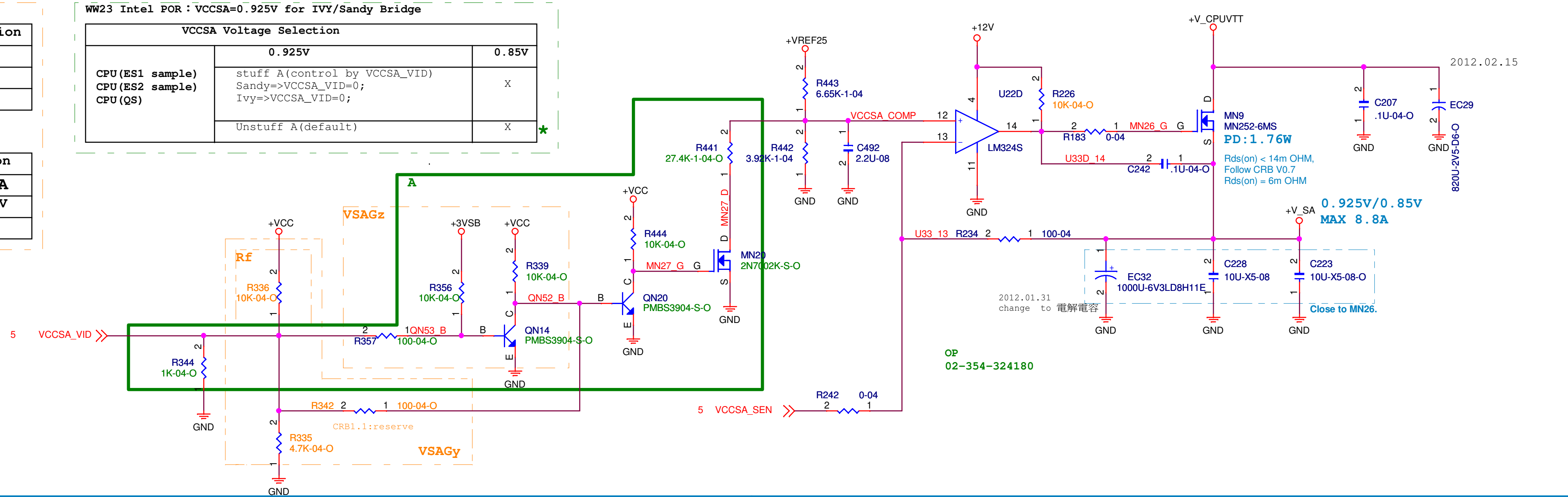
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

stuff VSAGy

VCCSA voltage selection	
Rf	+V_SA
stuff	0.925V
unstuff	0.85V

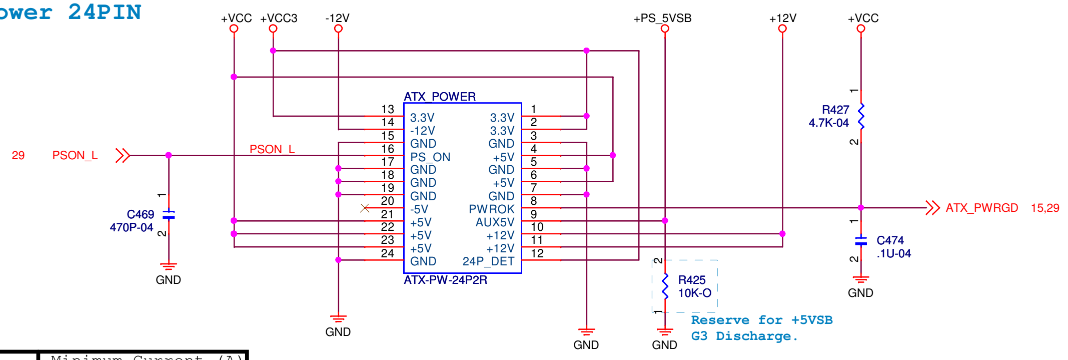
WW23 Intel POR：VCCSA=0.925V for IVY/Sandy Bridge

VCCSA Voltage Selection		
	0.925V	0.85V
CPU(ES1 sample) CPU(ES2 sample) CPU(QS)	stuff A(control by VCCSA_VID) Sandy=>VCCSA_VID=0; Ivy=>VCCSA_VID=0;	X
	Unstuff A(default)	X

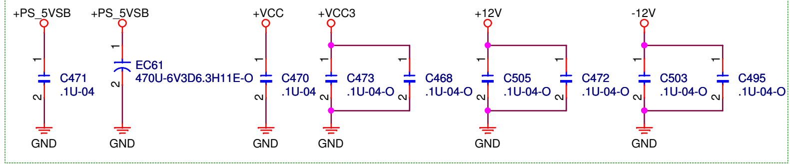


+V_SA

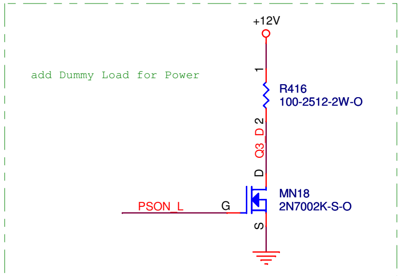
ATX Power 24PIN



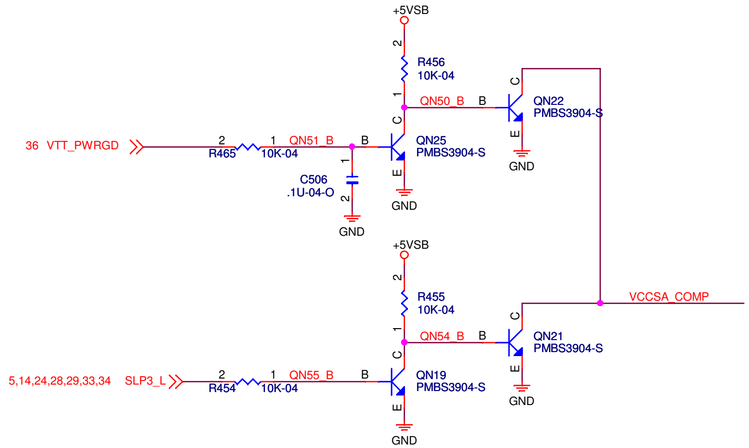
OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



Close to ATX PWR CONN



VCCSA Sequence



Elitegroup Computer Systems

Title	DC/DC VCCSA, ATXPWR	
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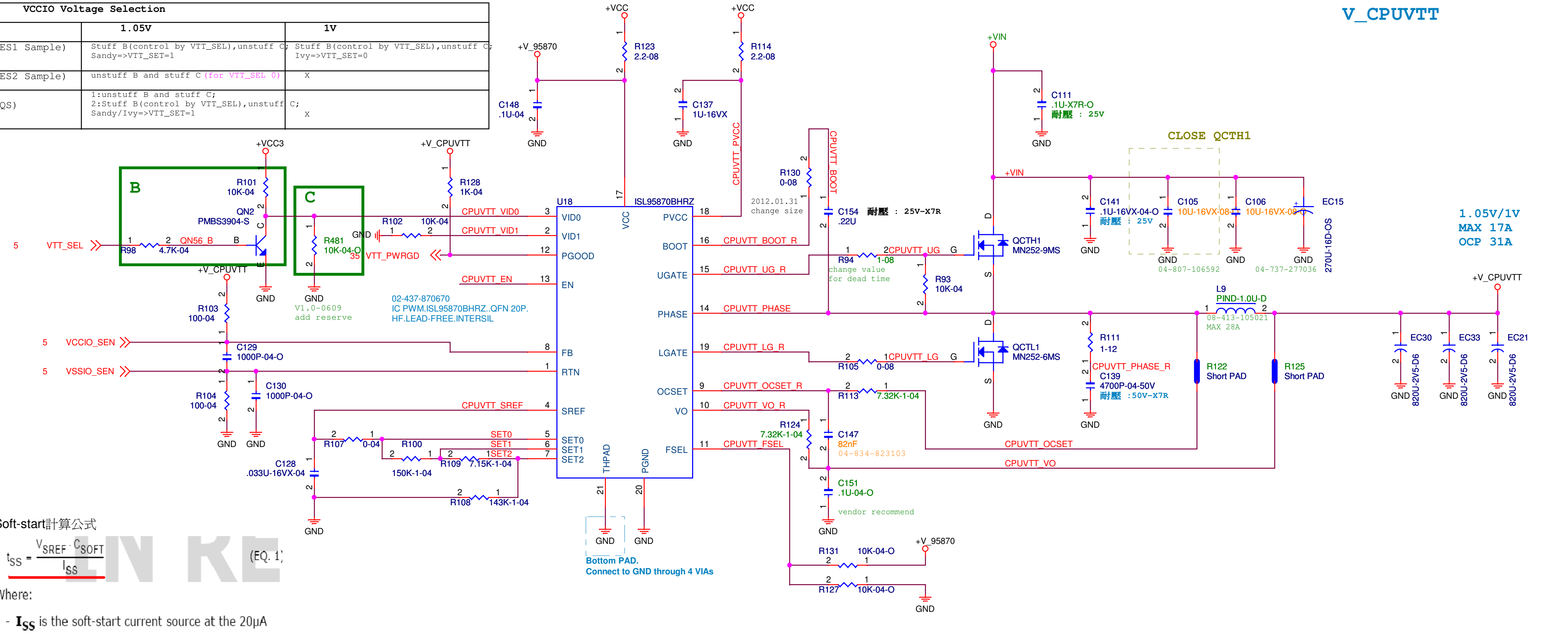
WW23 Intel POR:VCCIO=1.05V for Ivy/Sandy Bridge

VCCIO Voltage Selection		
	1.05V	1V
CPU(ES1 Sample)	Stuff B(control by VTT_SEL),unstuff C; Sandy=>VTT_SET=1	Stuff B(control by VTT_SEL),unstuff C; Ivy=>VTT_SET=0
CPU(ES2 Sample)	unstuff B and stuff C (for VTT_SEL 0)	X
CPU(QS)	1:unstuff B and stuff C; 2:Stuff B(control by VTT_SEL),unstuff C; Sandy/Ivy=>VTT_SET=1	X

V_CPUVTT



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

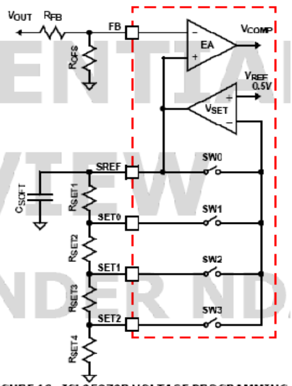
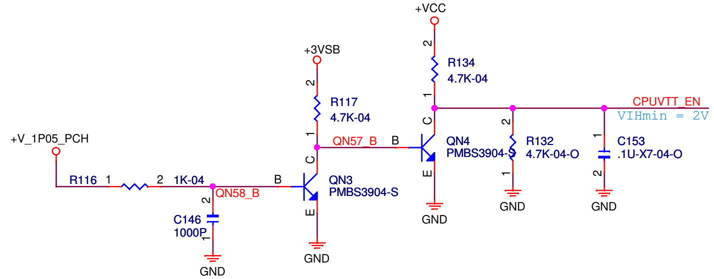
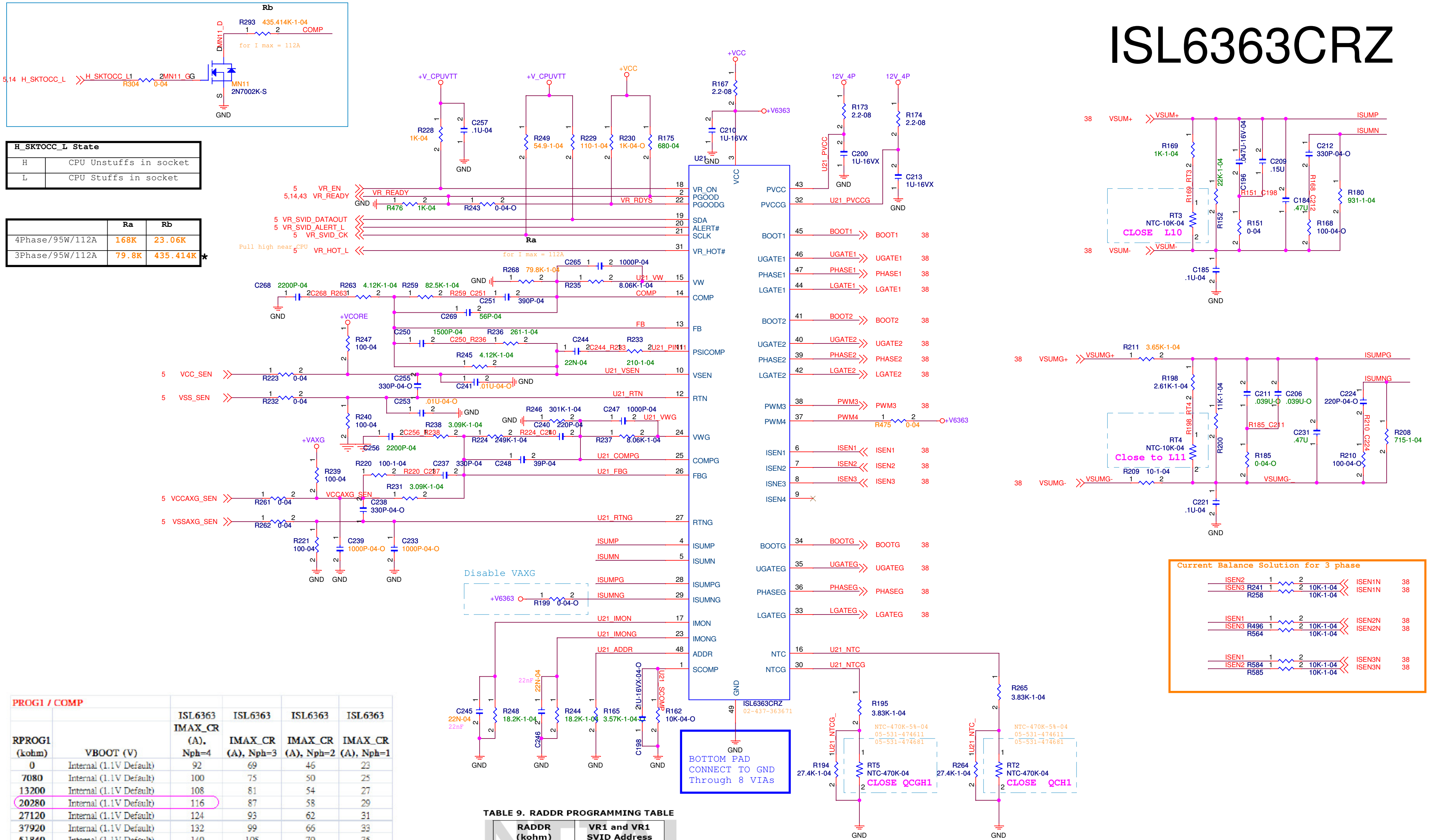


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
* 500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC



ISL6363CRZ



H_SKTOCC_L State	
H	CPU Unstuffs in socket
L	CPU Stuffs in socket

	Ra	Rb
4Phase/95W/112A	168K	23.06K
3Phase/95W/112A	79.8K	435.414K*

PROG1 / COMP

RPROG1 (kohm)	VBOOT (V)	ISL6363 IMAX_CR (A), Nph=4	ISL6363 IMAX_CR (A), Nph=3	ISL6363 IMAX_CR (A), Nph=2	ISL6363 IMAX_CR (A), Nph=1
0	Internal (1.1V Default)	92	69	46	23
7080	Internal (1.1V Default)	100	75	50	25
13200	Internal (1.1V Default)	108	81	54	27
20280	Internal (1.1V Default)	116	87	58	29
27120	Internal (1.1V Default)	124	93	62	31
37920	Internal (1.1V Default)	132	99	66	33
51840	Internal (1.1V Default)	140	105	70	35
67440	Internal (1.1V Default)	148	111	74	37
79800	0	148	111	74	37
94440	0	140	105	70	35
114360	0	132	99	66	33
138000	0	124	93	62	31
168000	0	116	87	58	29
198000	0	108	81	54	27
224400	0	100	75	50	25
298800	0	92	69	46	23

TABLE 9. RADDR PROGRAMMING TABLE

RADDR (kohm)	VR1 and VR1 SVID Address
3.57	0,1
16.5	2,3
32.4	4,5
59	6,7
88.7	8,9
127	A,B
182	C,D
Open Circuit	0,1

Elitegroup Computer Systems

Title	DC/DC VCORE/VAXG1	
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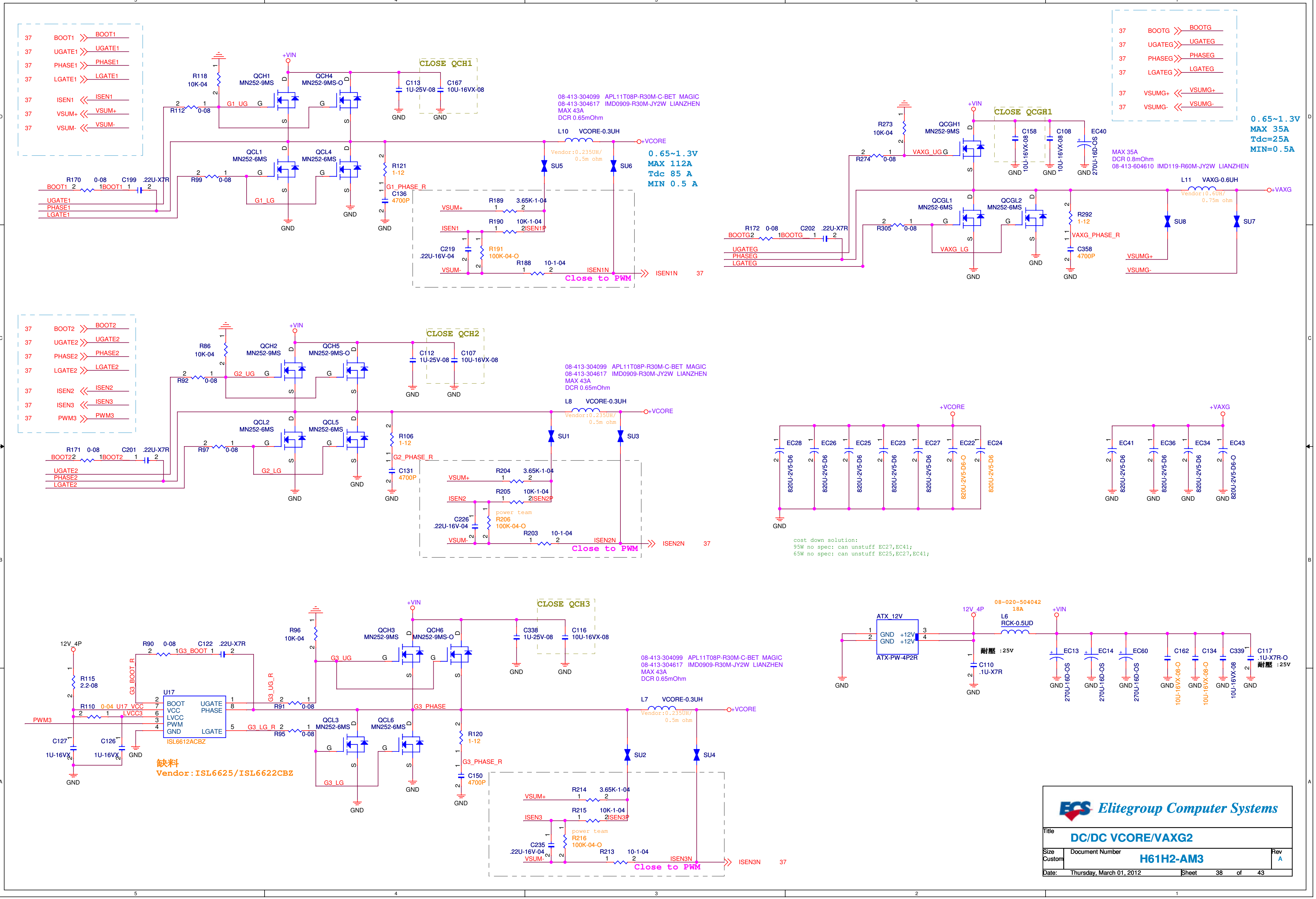

Elitegroup Computer Systems

Title: DC/DC VCORE/VAXG2

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PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down，No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up，intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up，“topblock swap” mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up，Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up，The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up，The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TVS	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

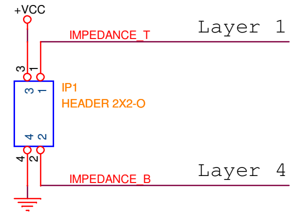
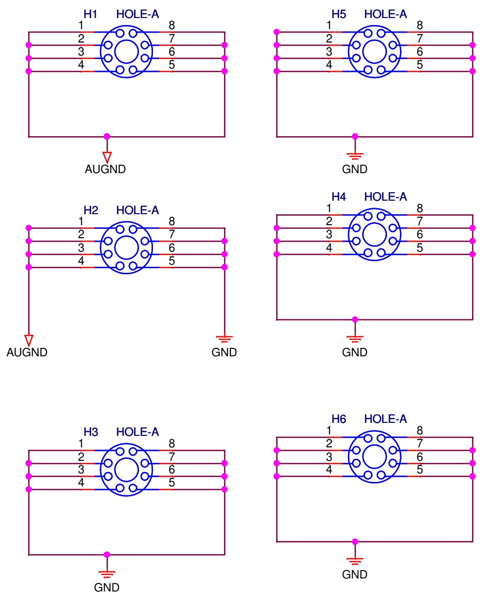


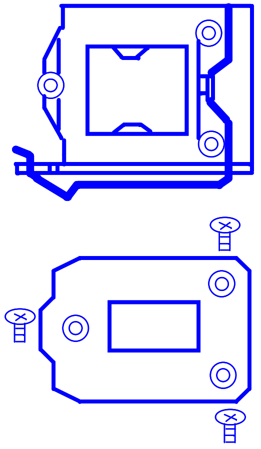
Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
JP2 Pin 122	Flashseg1_EN	Internal VCC-OK/ LRESET#	1	Disable
			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
[JP3,JP5] Pin 124 & Pin 46	FAN_CTL_SEL	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.

update hole,del pin9, and use pin1



CPU1(104)
CPU_SUBASSY_STEEL

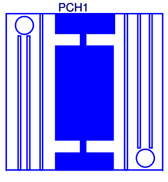


20-800-004611

for 104

special P/N:
20-120-013670
20-120-013671
20-120-013672

PCH1



for 103

X3

JP-WI-P6.25

10-617-002100

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Title: 104 & STRAPPING

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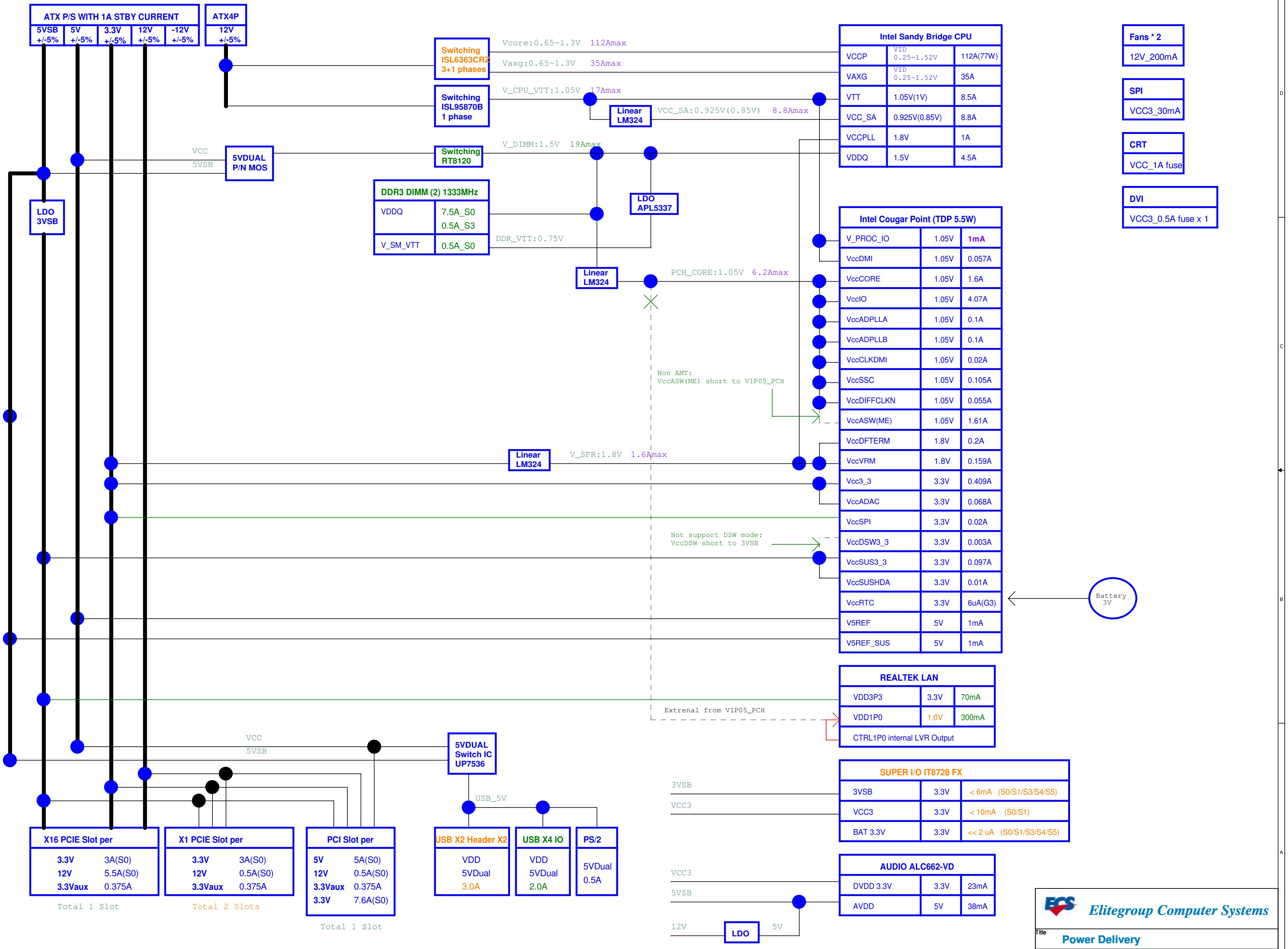

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Title	Power Delivery	
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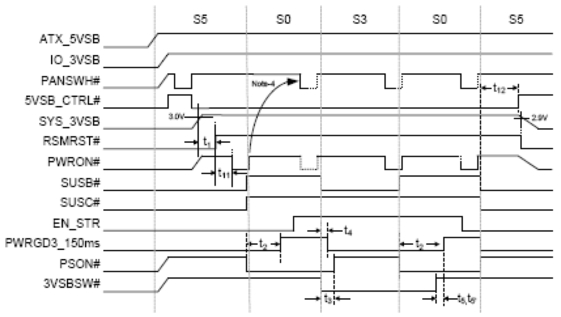
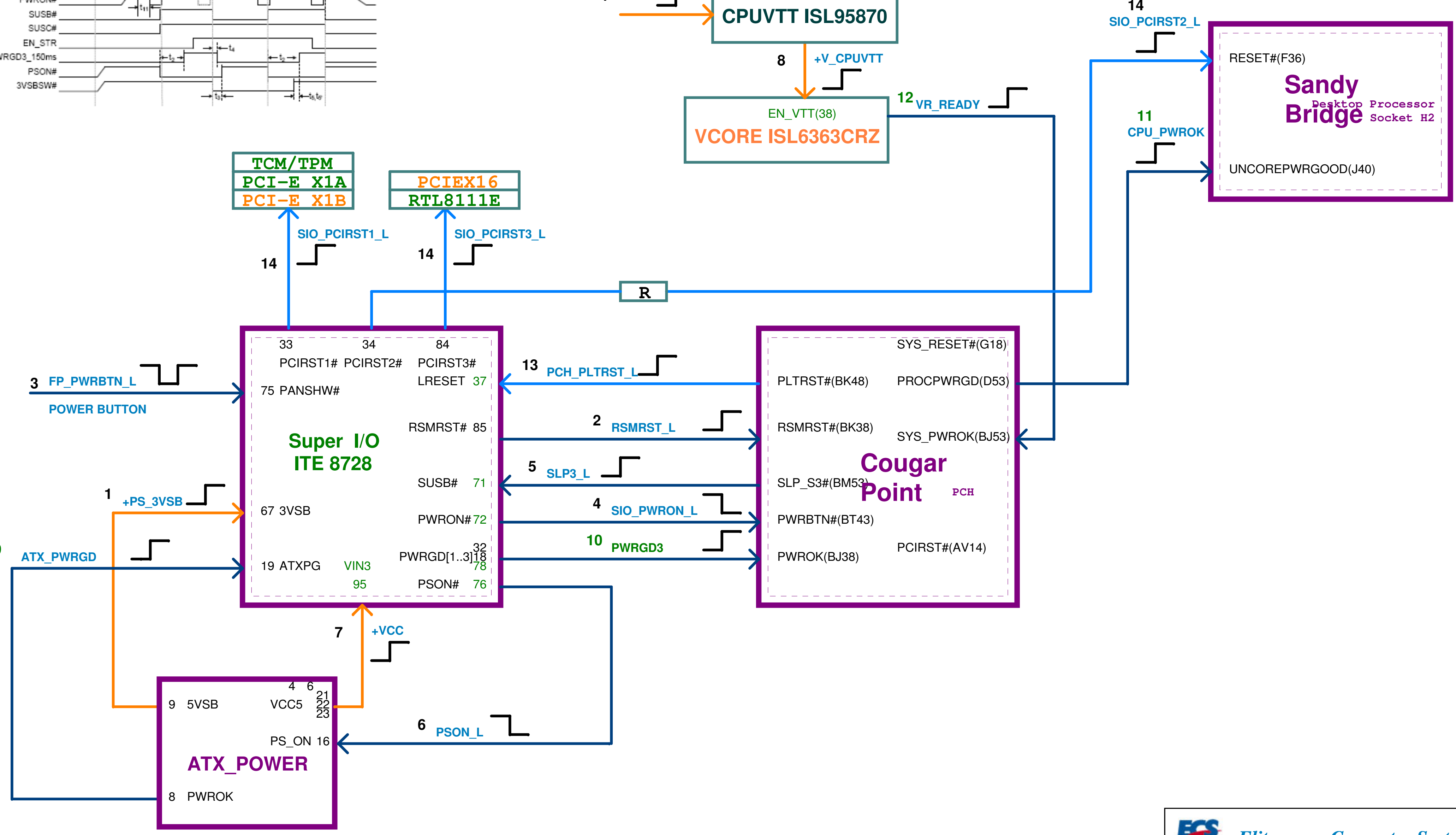
Figure 11-17. EuP Function Signal Timings





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Title: Power Sequence, Reset Diagram

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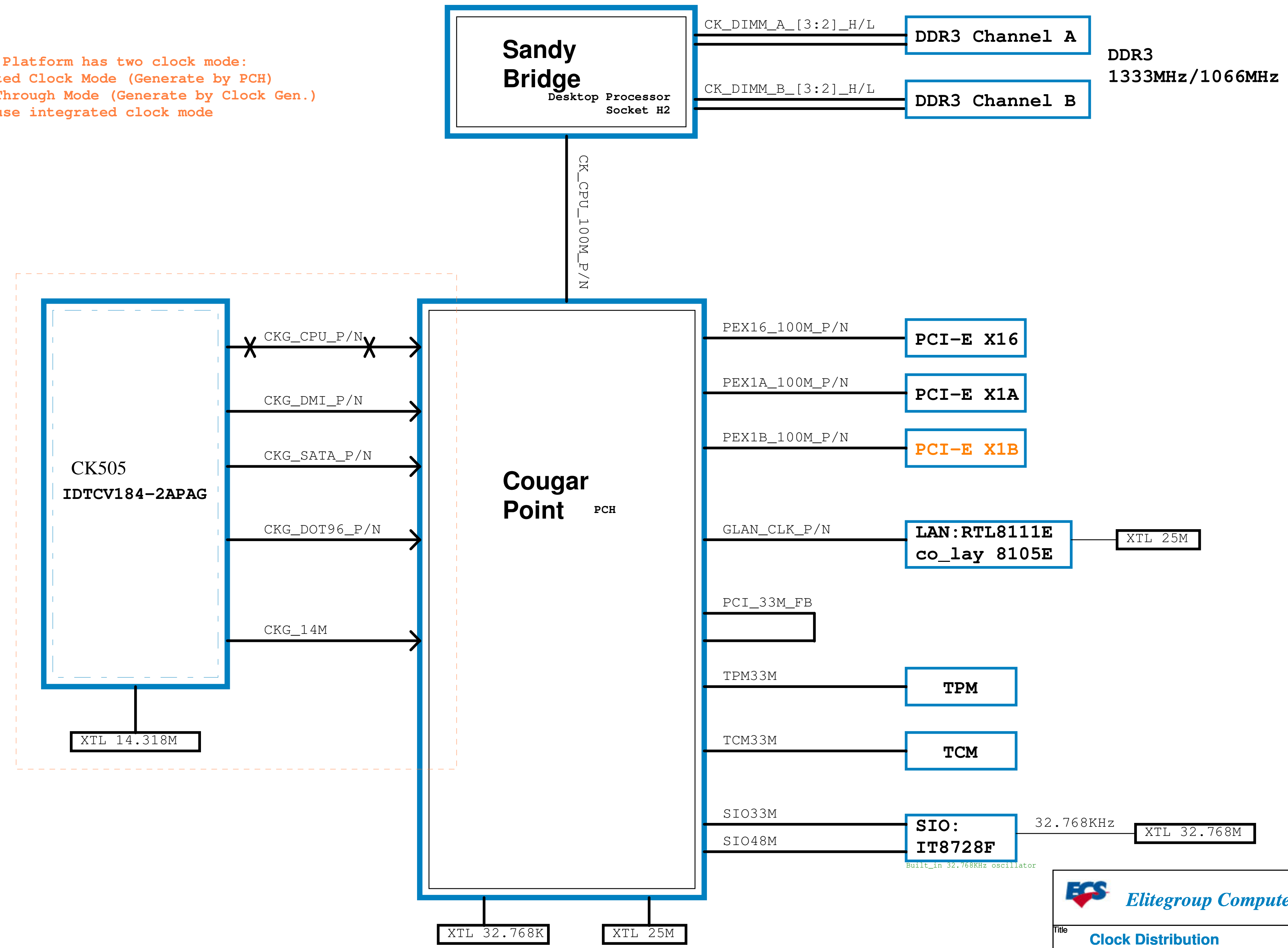
NOTE:
Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
H61H2-CM use integrated clock mode



Elitegroup Computer Systems

Title	Clock Distribution	
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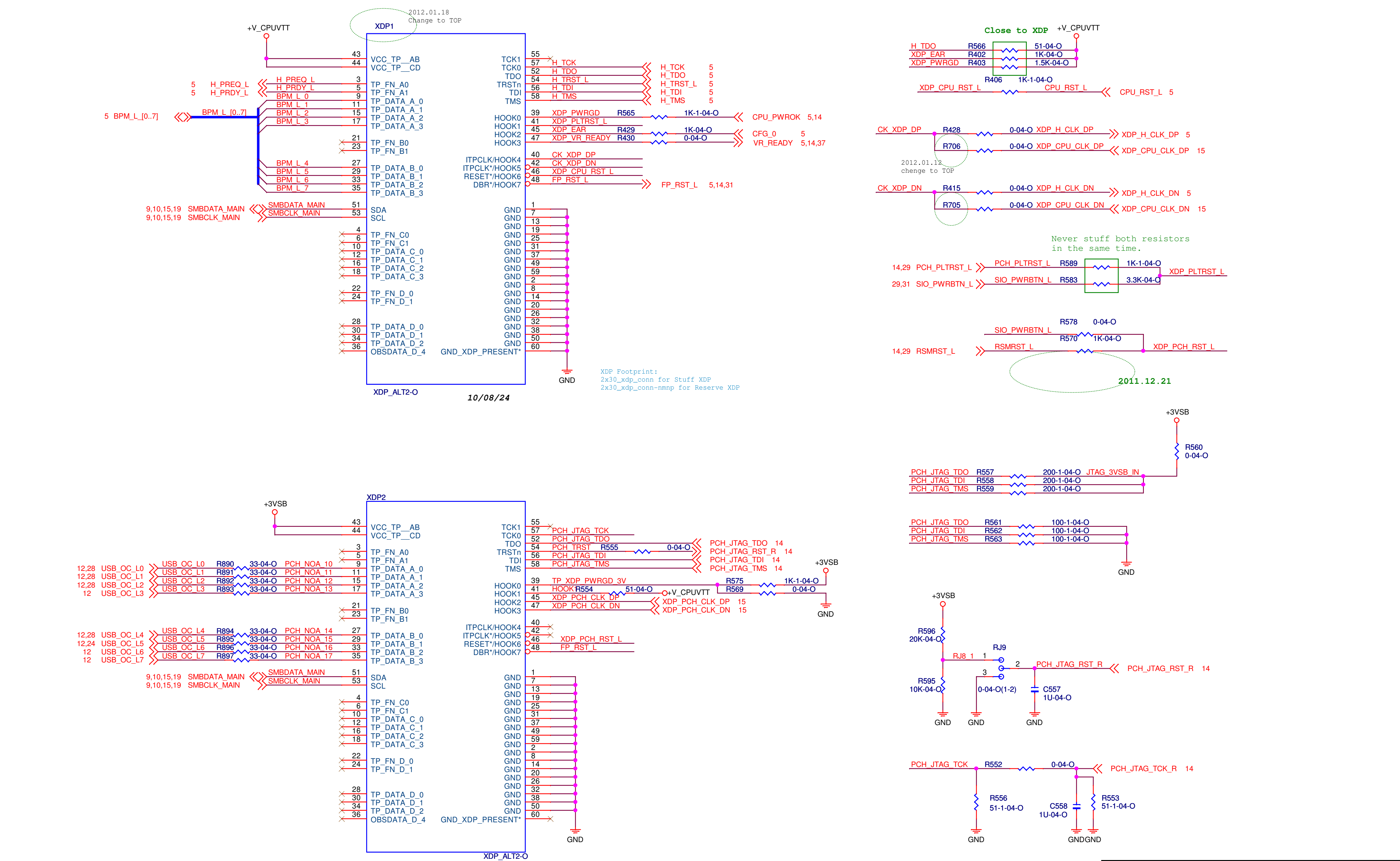

ECS Elitegroup Computer Systems

Title: XDP

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