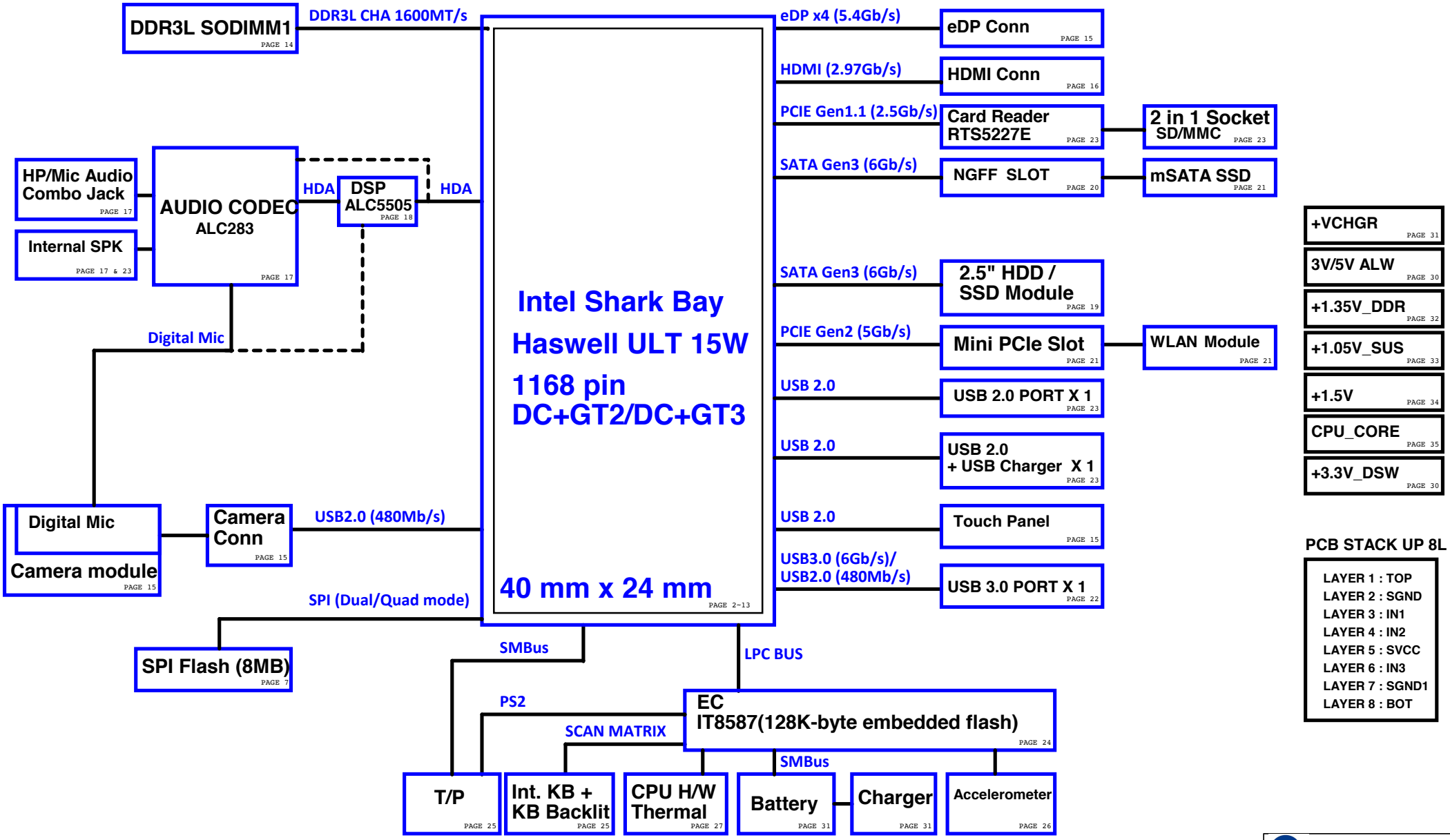
LZ5 13" UMA
INTEL SHARK BAY ULT ONE CHIP PLATFORM



PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

PROJECT : LZ5
Quanta Computer Inc.
System Block Diagram
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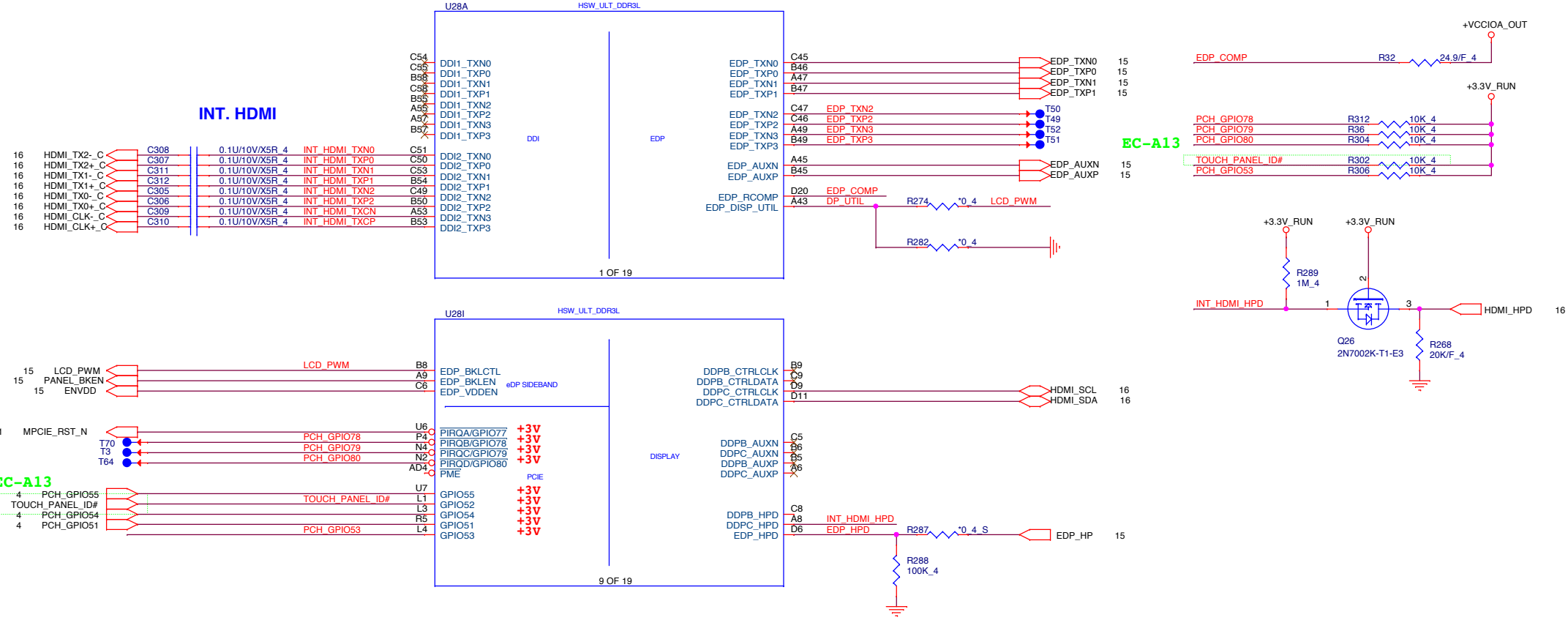
Haswell ULT (DISPLAY)



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Quanta Computer Inc.			
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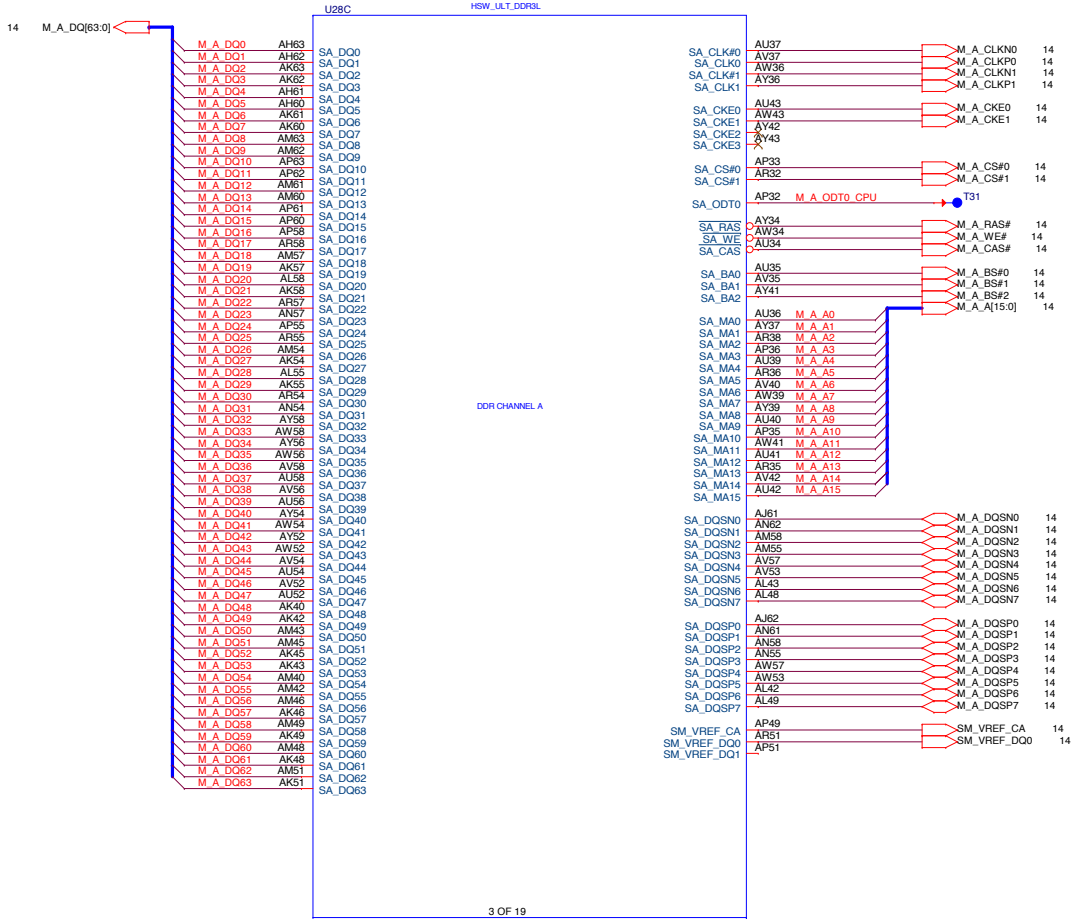
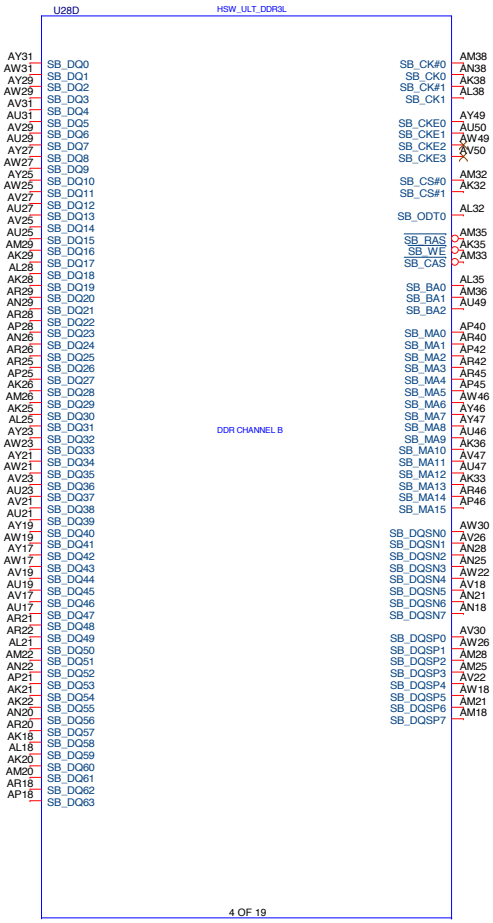
Haswell ULT (DDR3L)





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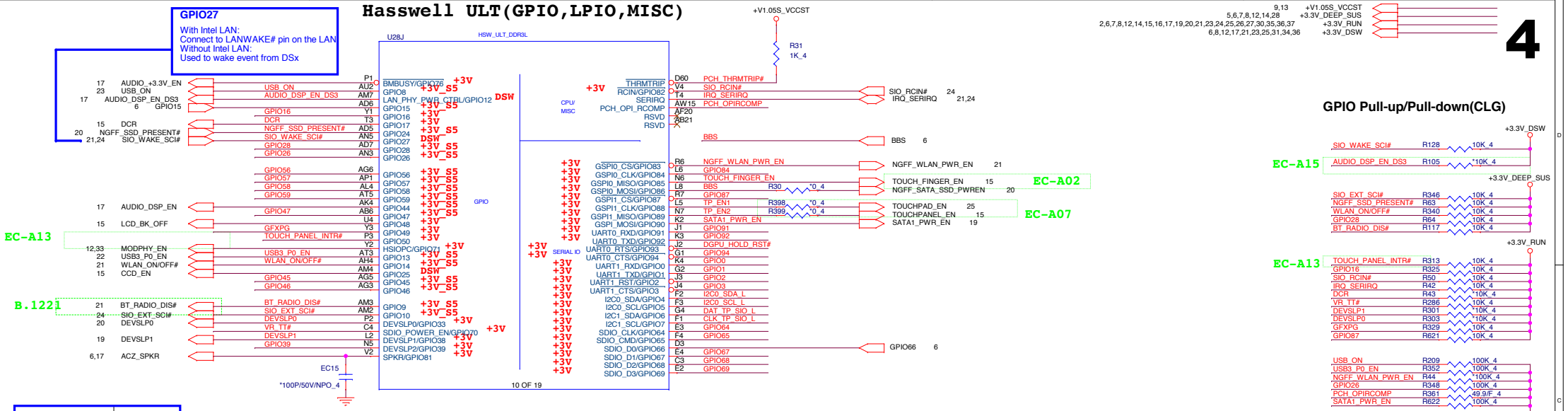
Hasswell ULT(GPIO,LPIO,MISC)

GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



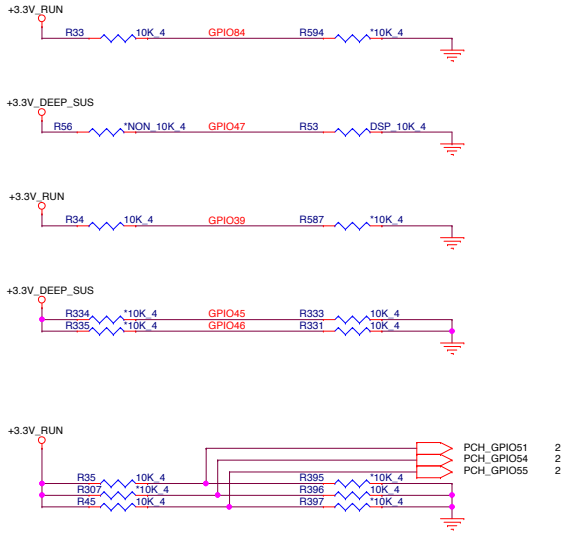
Thunderbolt ID	GPIO84
Supported	0
Not Supported	1

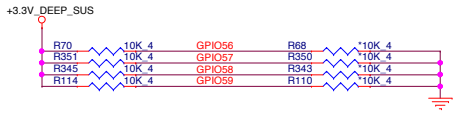
Audio DSP ID	GPIO47
Supported	0
Not Supported	1

DGPU SELECT	GPIO39
Supported	0
Not Supported	1

Model ID	GPIO45	GPIO46
LZ5-UMA	0	0
LZ9-UMA	0	1
LZ9A-DIS	1	0
LZA	1	1

Board ID	GPIO51	GPIO54	GPIO55
SDV	1	1	1
SIV	1	1	0
SIT	1	0	1
SVT			

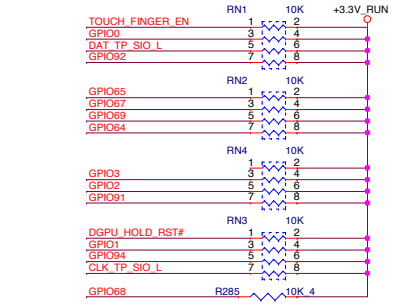


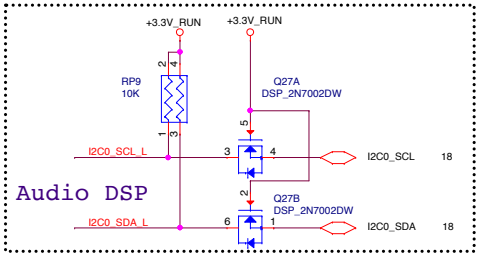


DDR3L Memory Down ID Table , LZ5 don't support DDR3L Memory Down

Vendor	Description	Size	Quanta P/N	GPIO[56,57,58,59]
Default				1111
Samsung	K4B8G1646B-MYK0 (B/4Gb/35nm/DDP)	8Gb x 16	AKD5FGET500	1110
Micron	MT41K512M16TNA-125:E(V80A/4Gb/30nm/DDP)	8Gb x 16	AKD5FGSTL00	1101
ELPIDA	EDJ8416E6MB-GN-F(F/4Gb/30nm/DDP)	8Gb x 16	AKD5FGST402	1100
SK hynix		8Gb x 16		XXXX
Samsung	K4B4G1646B-HYK0(B/4Gb/35nm)	4Gb x 16	AKD5PGET500	1011
Micron	MT41K256M16HA-125:E(V80A/4Gb/30nm)	4Gb x 16	AKD5JGSTL02	1010
ELPIDA	EDJ4216EFBG-GN-F(F/4Gb/30nm)	4Gb x 16	AKD5JGST403	1001
SK hynix	H5TC4G63AFR-PBA(D/4Gb/29nm)	4Gb x 16	AKD5JGETW00	1000

GPIO Pull-up/Pull-down(CLG)





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Haswell ULT (PCIE,USB)

4,6,7,8,12,14,28 +3.3V_DEEP_SUS
12 +V1.05S_AUSB3PLL

U28K HSW_ULT_DDR3L

PCIE

F10 PERN5_L0
E10 PERP5_L0
C23 PETN5_L0
C22 PETP5_L0
F8 PERN5_L1
E8 PERP5_L1
B23 PETN5_L1
A23 PETP5_L1
H10 PERN5_L2
G10 PERP5_L2
B21 PETN5_L2
C21 PETP5_L2
E6 PERN5_L3
F6 PERP5_L3
B22 PETN5_L3
A21 PETP5_L3

21 PCIE_RXN3
21 PCIE_RXP3
WiFi/BT NGFF
21 PCIE_TXN3
21 PCIE_TXP3
C323 0.1U/10V/X5R_4 PCIE_TXN3_C
C324 0.1U/10V/X5R_4 PCIE_TXP3_C

23 PCIE_RXN4
23 PCIE_RXP4
Card Reader
23 PCIE_TXN4
23 PCIE_TXP4
C321 0.1U/10V/X5R_4 PCIE_TXN4_C
C322 0.1U/10V/X5R_4 PCIE_TXP4_C

G11 PERN3
F11 PERP3
C29 PETN3
B30 PETP3
F13 PERN4
G13 PERP4
B29 PETN4
A29 PETP4
G17 PERN1/USB3RN3
F17 PERP1/USB3RP3
C30 PETN1/USB3TN3
C31 PETP1/USB3TP3
F15 PERN2/USB3RN4
G15 PERP2/USB3RP4
B31 PETN2/USB3TN4
A31 PETP2/USB3TP4

+V1.05S_AUSB3PLL
R281 3K/F_4 PCIE_RCOMP
R280 0_4 PCIE_IREF
E15 RSVD
E13 RSVD
A27 PCIE_RCOMP
B27 PCIE_IREF

USB

USB2N0 AN8
USB2P0 AM8
USB2N1 AR7
USB2P1 AT7
USB2N2 AR8
USB2P2 AP8
USB2N3 AR10
USB2P3 AT10
USB2N4 AM15
USB2P4 AL15
USB2N5 AM13
USB2P5 AN13
USB2N6 AP11
USB2P6 AN11
USB2N7 AR13
USB2P7 AP13

USB-_TPanel 15
USB+_TPanel 15
Touch Panel
USBP1- 22
USBP1+ 22
USB3.0 Port 1 (CN7)
USBP2- 23
USBP2+ 23
USB2.0 Port 1
USBP3- 23
USBP3+ 23
USB2.0 Port 2
USBP4- 15
USBP4+ 15
CAMERA
USBP5- 21
USBP5+ 21
WLAN / BT NGFF

USB3RN1 G20
USB3RP1 H20
USB3TN1 C33
USB3TP1 B34
USB3RN2 E18
USB3RP2 F18
USB3TN2 B33
USB3TP2 A33

USB30_RX1- 22
USB30_RX1+ 22
USB30_TX1- 22
USB30_TX1+ 22
USB3.0 Port 1 (CN7)

USBRBIAS AJ10 USB_BIAS R73 22.6/F_4
USBRBIAS AJ11
RSVD AN10 USBPLLMON_N R100 49.9/F_4
RSVD AM10 USBPLLMON_P R99 49.9/F_4

+3V_S5 OC0/GPIO40 AL3 USB_OC0#
+3V_S5 OC1/GPIO41 AT1 USB_OC1#
+3V_S5 OC2/GPIO42 AH2 USB_OC2#
+3V_S5 OC3/GPIO43 AV3 USB_OC3#

USB_OC0# 22
USB_OC1# 23

+3.3V_DEEP_SUS
RP3 10K
USB_OC1# 4 2
USB_OC3# 3 1
RP2 10K
USB_OC2# 4 2
USB_OC0# 3 1

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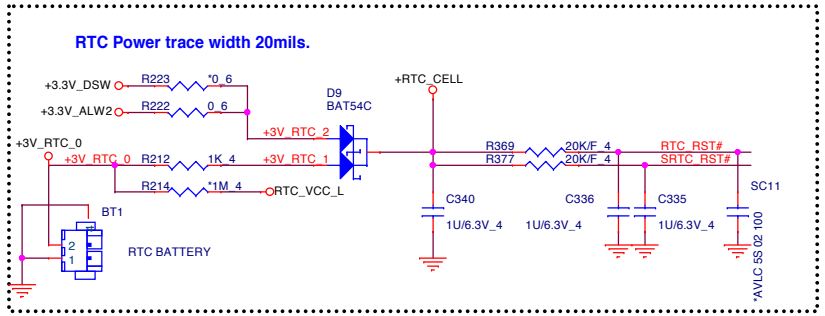
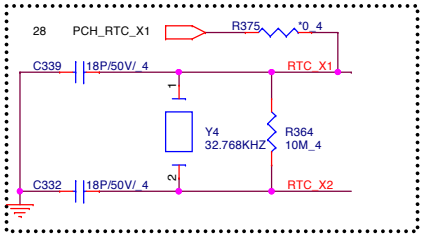
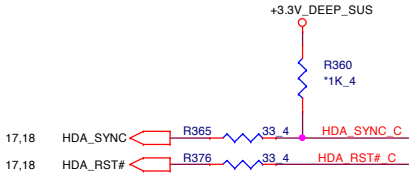
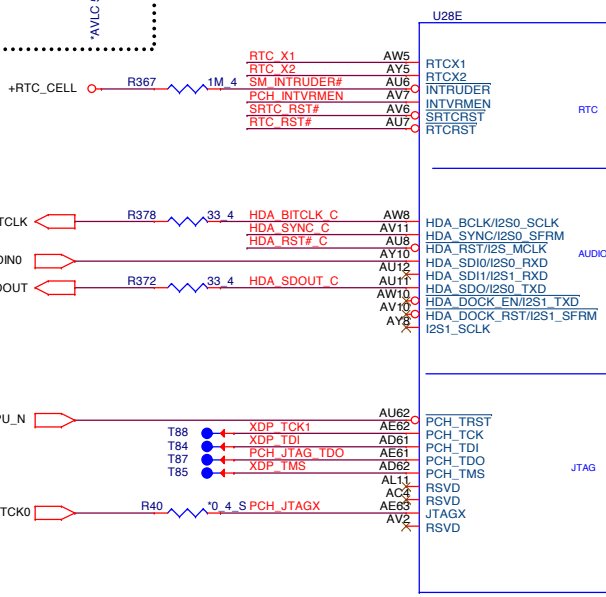
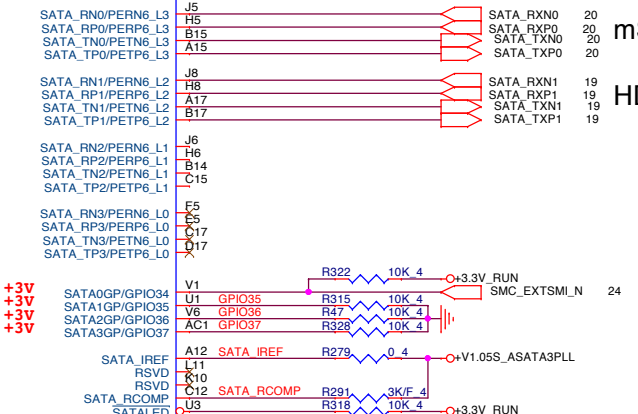
Haswell ULT (RTC, HDA, JTAG, SATA)









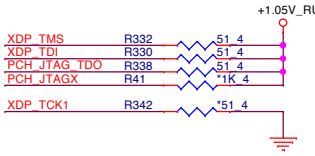


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R321 *1K_4 ACZ_SPKR 4,17
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	24 ME_WR# R371 1K_4 HDA_SDOUT_C EC-A21
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R370 330K_4 PCH_INTVRMEN R359 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO R283 *1K_4 GPIO66 4 R284 *1K_4
GPIO86	BBS(Boot BIOS Strap Bit)		0 = Default SPI (iPD 20K) 1 =LPC	+3.3V_RUN R28 *1K_4 BBS 4 R29 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	+3.3V_DEEP_SUS R59 *10K_4 GPIO15 4
DSWVREN	Deep Sx well on die DSW VR enable		1=Should be always pull-up	+RTC_CELL R368 330K_4 DSWVRMEN 8

PCH JTAG Debug (CLG)

MP remove(Intel)



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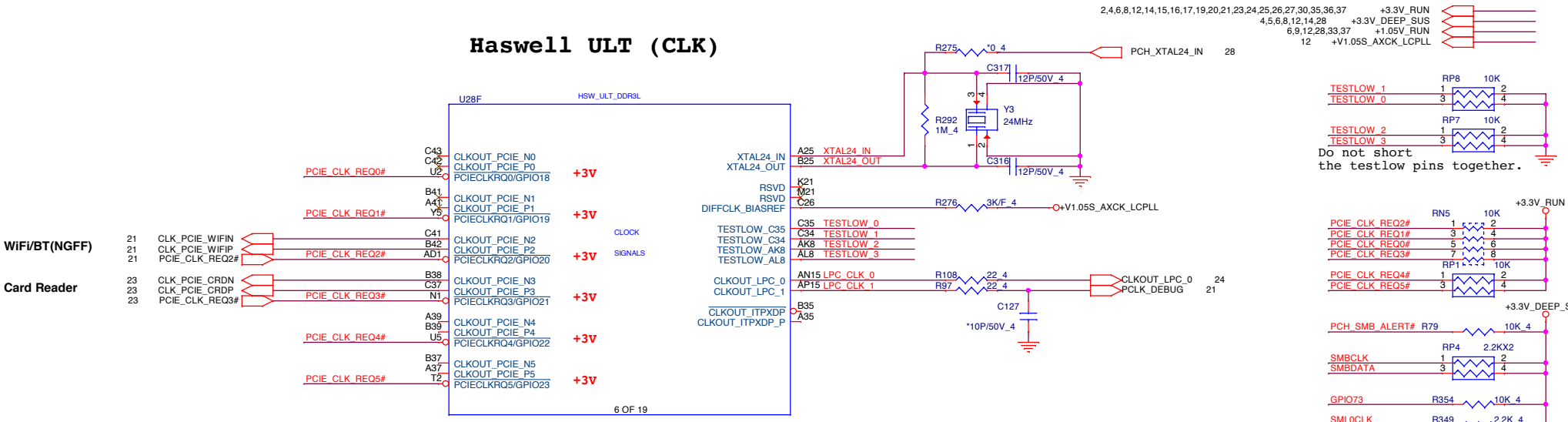
Haswell ULT (CLK)



WiFi/BT(NGFF)

21 CLK_PCIE_WIFIN
21 CLK_PCIE_WIFIP
21 PCIE_CLK_REQ2#

Card Reader

23 CLK_PCIE_CRDN
23 CLK_PCIE_CRDP
23 PCIE_CLK_REQ3#

2,4,6,8,12,14,15,16,17,19,20,21,23,24,25,26,27,30,35,36,37 +3.3V_RUN
4,5,6,8,12,14,28 +3.3V_DEEP_SUS
6,9,12,28,33,37 +1.05V_RUN
12 +V1.05S_AXCK_LCPLL

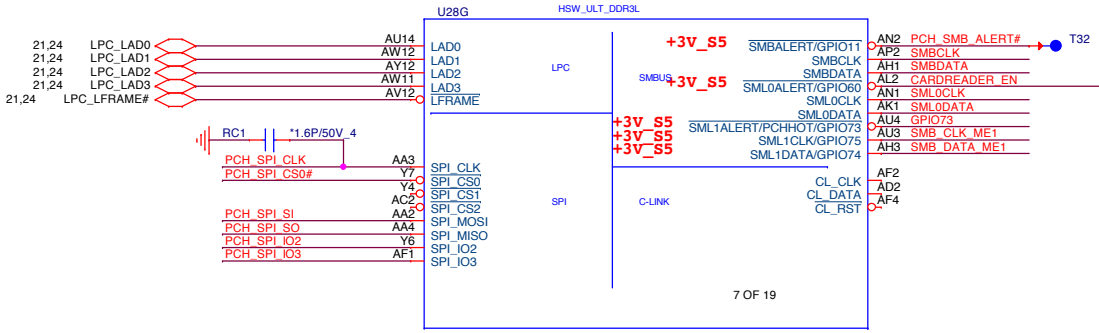
RP8 10K
TESTLOW_1 TESTLOW_0
RP7 10K
TESTLOW_2 TESTLOW_3

Do not short
the testlow pins together.

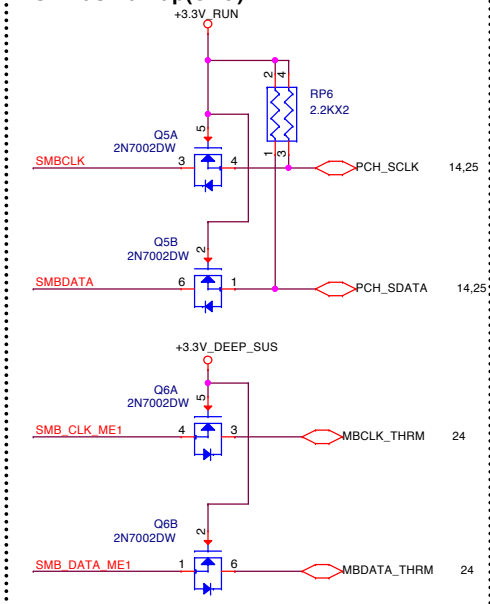
+3.3V_RUN
RN5 10K
PCIE_CLK_REQ2# PCIE_CLK_REQ1# PCIE_CLK_REQ0# PCIE_CLK_REQ3#
RP1 10K
PCIE_CLK_REQ4# PCIE_CLK_REQ5#

+3.3V_DEEP_SUS
PCH_SMB_ALERT# R79 10K_4
RP4 2.2KX2
SMBCLK SMBDATA
GPIO73 R354 10K_4
SML0CLK R349 2.2K_4
SML0DATA R341 2.2K_4
RP5 2.2KX2
SMB_DATA_ME1 SMB_CLK_ME1
CARDREADER_EN R256 100K_4

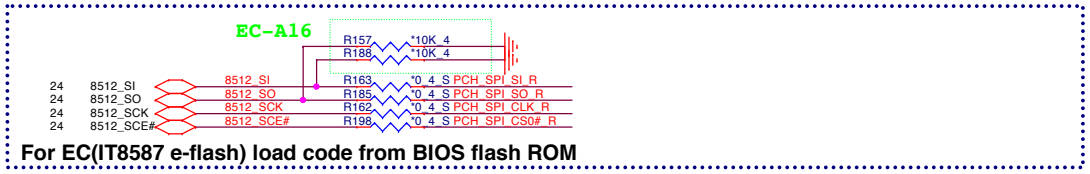
Haswell ULT (LPC/SPI/SMB/CLINK)



SMBus/Pull-up(CLG)

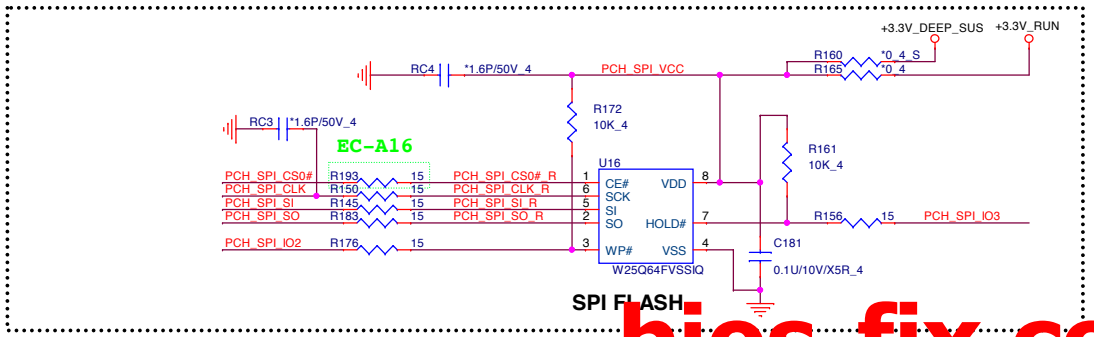


EC-A16



For EC(IT8587 e-flash) load code from BIOS flash ROM

SPI FLASH



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Haswell ULT (SYSTEM POWER MANAGEMENT)

8

4,6,12,17,21,23,25,31,34,36
2,4,6,7,12,14,15,16,17,19,20,21,23,24,25,26,27,30,35,36,37
4,5,6,7,12,14,28
+3.3V_DSW
+3.3V_RUN
+3.3V_DEEP_SUS

PCH Pull-high/low(CLG)

+3.3V_DEEP_SUS
SIO_PWRBTN# R118 *10K_4
SUSWARN# R116 10K_4
SUSCLK R66 10K_4

+3.3V_DSW
AC_PRESENT R101 10K_4
PM_BATLOW# R347 10K_4
PCIE_WAKE#_R R80 1K_4
EC-A29

+3.3V_RUN
CLKRUN# R317 10K_4
SYS_RESET# R327 10K_4
RSMRST# R358 10K_4
SYS_PWROK R337 10K_4
DPWROK_R R357 100K_4

U28H HSW_ULT_DDR3L
SYSTEM POWER MANAGEMENT

24 SUSACK# R339 0_4 SUSACK#_R AK2 SUSACK
SYS_RESET# AC3 SYS_RESET
EC-A17
17,24 EC_PWROK R379 0_4 SYS_PWROK AY7 SYS_PWROK
R380 0_4 PCH_PWROK AB5 PCH_PWROK
PCH_APWROK AG7 APWROK
PLTRST# PLTRST

24 RSMRST# RSMRST# AW6 RSMRST
24 SUSWARN# SUSWARN# AV4 SUSWARN/SUSPWRDNACK/GPIO30
24 SIO_PWRBTN# SIO_PWRBTN# AL7 PWRBTN
24 AC_PRESENT AC_PRESENT AJ8 ACPRESENT/GPIO31
PM_BATLOW# AN4 BATLOW/GPIO72
24 SLP_S0# AF3 SLP_S0
TP6 AM5 SLP_WLAN/GPIO29

+3V
+3V_S5
+3V_S5
DSW
+3V_S5
DSW
DSW
DSW

DSWVRMEN AW7
DPWROK AV5 DPWROK_R
WAKE AJ5 PCIE_WAKE#_R
EC-A04
R366 0_4
R356 *0_4 RSMRST#
R84 *0_4_S
DSWVRMEN 6
DPWROK 24
PCIE_WAKE# 21

CLKRUN/GPIO32 V5 CLKRUN#
SUS_STAT/GPIO61 AG4
SUSCLK/GPIO62 AE6 SUSCLK
SLP_S5/GPIO63 AP5
CLKRUN# 24
T97
T96

SLP_S4 AJ6
SLP_S3 AT4
SLP_A AL5 SIO_SLP_A#
SLP_SUS AP4
SLP_LAN AJ7 SIO_SLP_LAN#
SLP_S4# 24
SIO_SLP_S3# 24
T95
SLP_SUS# 24
TP5

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SYS_PWROK
RSMRST#
PLTRST#
EC_PWROK
*AVLC 5S 02 100
SC13 SC3 SC12 SC10
ESD

+3.3V_DEEP_SUS
R353 *10K_4
Q28 2N7002
PM_BATLOW# 3 2 1
PM_BATLOW_N 24

+3.3V_DEEP_SUS
U8 *TC7SH08FU
C97 *0.1U/10V/X7R_4
20,21 BUF_PLT_RST#
RV3 *EGA-0402
R78 100K_4
R74 *0_4_S
PLTRST#
PLTRST# 23

For DS3

+3.3V_DSW
+3.3V_DEEP_SUS
R107 *0_6
R120 *100K_4
C141 1U/6.3V_4
U12
IN IN ON/OFF OUT GND
IC(5P) G5243AT11U
24 SLP_SUS_ON_GPG2
C140 *10P/50V_4
R119 *100K_4
C135 0.1U/10V_4

System PWR_OK(CLG)

EC-A18
+3.3V_DEEP_SUS
+3.3V_RUN
R608 *10K_4
R609 *10K_4
Q50 *2N7002
24 SYS_PWROK_EC
9,35 IMVP_PWRGD
R611 *4.7K_4
Q43 *MMBT3904-7-F

+3.3V_DEEP_SUS
U32 *TC7SH08FU
C566 *0.1U/10V/X7R_4
IMVP_PWRGD_3V
SYS_PWROK
*AVLC 5S 02
SC33
R610 0_4

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35 +VCCIN
4,13 +V1.05S_VCCST
14,32,37 +V_VDDQ_VR
13 +VCCIO_OUT
6,12,28,33,37 +1.05V_RUN
2 +VCCIOA_OUT

Haswell ULT MCP(POWER)

CPU VDDQ

Haswell ULT 15W : 4.2A

6X10UF MLCC
4X2.2UF MLCC

+V_VDDQ_VR
C79 10U/6.3V/X5R_6
C82 10U/6.3V/X5R_6
C81 10U/6.3V/X5R_6
C80 10U/6.3V/X5R_6
C161 10U/6.3V/X5R_6
C91 10U/6.3V/X5R_6
C160 10U/6.3V/X5R_6
C156 2.2U/6.3V/X5R_4
C188 2.2U/6.3V/X5R_4
C186 2.2U/6.3V/X5R_4
C189 2.2U/6.3V/X5R_4

+V1.05S_VCCST
R277 10K_4
VCCST_PWRGD_L
Q4 2N7002
24 VCCST_PWRGD#
35 H_VR_ENABLE_MCP
8,35 IMVP_PWRGD
R290 10K_4
+V1.05S_VCCST
R39 150_6
T4

EC-A19
C326 *0.1U/10V/X5R_4

+VCCIOA_OUT
+VCCIO_OUT

+1.05V_RUN
R54 *0_12_S
+V1.05S_VCCST

+VCCIN
+VCCIN
R293 100/F_4
35 VCCSENSE
VCCSENSE

+V1.05S_VCCST

U28L
HSW_ULT_DDR3L

T11	MCP_RSVD_61	L59	RSVD
T7	MCP_RSVD_62	J58	RSVD
		AH26	VDDQ
		AJ31	VDDQ
		AJ33	VDDQ
		AJ37	VDDQ
		AN33	VDDQ
		AP43	VDDQ
		AR48	VDDQ
		AY35	VDDQ
		AY40	VDDQ
		AY44	VDDQ
		AY50	VDDQ
		F59	VCC
T13	MCP_RSVD_63	N58	RSVD
T26	MCP_RSVD_64	AC58	RSVD
	VCCSENSE	E63	VCC_SENSE
T19	MCP_RSVD_65	AB23	RSVD
		A59	VCCIO_OUT
		E20	VCCIOA_OUT
T20	MCP_RSVD_66	AD23	RSVD
T18	MCP_RSVD_67	AA23	RSVD
T28	MCP_RSVD_68	AE59	RSVD
	H_CPU_SVIDALRT_N	L62	VIDALERT
	VR_SVID_CLK	N63	VIDSCLK
	VR_SVID_DATA	L63	VIDSOUT
		B59	VCCST_PWRGD
		F60	VR_EN
		C59	VR_READY
		D63	VSS
	FIVR_EN_BUF	H59	PWR_DEBUG
		P62	VSS
T65	MCP_RSVD_69	P60	RSVD_TP
T9	MCP_RSVD_70	P61	RSVD_TP
T14	MCP_RSVD_71	N59	RSVD_TP
T10	MCP_RSVD_72	N61	RSVD_TP
T12	MCP_RSVD_73	T59	RSVD
T27	MCP_RSVD_74	AD60	RSVD
T29	MCP_RSVD_75	AD59	RSVD
T25	MCP_RSVD_76	AA59	RSVD
T86	MCP_RSVD_77	AE60	RSVD
T24	MCP_RSVD_78	AC59	RSVD
T30	MCP_RSVD_79	AG58	RSVD
T15	MCP_RSVD_80	U59	RSVD
T16	MCP_RSVD_81	V59	RSVD
		AC22	VCCST
		AE22	VCCST
		AE23	VCCST
		AB57	VCC
		AD57	VCC
		AG57	VCC
		C24	VCC
		C28	VCC
		C32	VCC

HSW ULT POWER

12 OF 19

CPU VCC

Haswell ULT 15W : 32A

23 X 22UF(MLCC)

+VCCIN

VCC	C36	C71	22U/6.3V/X5R_6
VCC	C40	C76	22U/6.3V/X5R_6
VCC	C44	C37	22U/6.3V/X5R_6
VCC	C48	C50	22U/6.3V/X5R_6
VCC	C52	C59	22U/6.3V/X5R_6
VCC	C56	C51	22U/6.3V/X5R_6
VCC	E23	C46	22U/6.3V/X5R_6
VCC	E25	C34	22U/6.3V/X5R_6
VCC	E27	C52	22U/6.3V/X5R_6
VCC	E29	C38	22U/6.3V/X5R_6
VCC	E31	C60	22U/6.3V/X5R_6
VCC	E33	C53	22U/6.3V/X5R_6
VCC	E35	C32	22U/6.3V/X5R_6
VCC	E37	C47	22U/6.3V/X5R_6
VCC	E39	C67	22U/6.3V/X5R_6
VCC	E41	C66	22U/6.3V/X5R_6
VCC	E43	C43	22U/6.3V/X5R_6
VCC	E45	C39	22U/6.3V/X5R_6
VCC	E47	C35	22U/6.3V/X5R_6
VCC	E49	C64	22U/6.3V/X5R_6
VCC	E51	C36	22U/6.3V/X5R_6
VCC	E53	C55	22U/6.3V/X5R_6
VCC	E55	C61	22U/6.3V/X5R_6
VCC	E57	C48	22U/6.3V/X5R_6
VCC	F24	C33	22U/6.3V/X5R_6
VCC	F28	C62	22U/6.3V/X5R_6
VCC	F32	C63	22U/6.3V/X5R_6
VCC	F36	C65	22U/6.3V/X5R_6
VCC	F40	C49	22U/6.3V/X5R_6
VCC	F44	C54	22U/6.3V/X5R_6
VCC	F48		
VCC	F52		
VCC	F56		
VCC	G23		
VCC	G25		
VCC	G27	C89 1 2	100P/50VX7R_4
VCC	G29	C87 1 2	100P/50VX7R_4
VCC	G31	C45 1 2	100P/50VX7R_4
VCC	G33	C44 1 2	100P/50VX7R_4
VCC	G35		
VCC	G37		
VCC	G39		
VCC	G41		
VCC	G43		
VCC	G45		
VCC	G47		
VCC	G49		
VCC	G51		
VCC	G53		
VCC	G55		
VCC	G57		
VCC	H23		
VCC	J23		
VCC	K23		
VCC	K57		
VCC	L22		
VCC	M23		
VCC	M57		
VCC	P57		
VCC	U57		
VCC	W57		

SVID ALERT

+V1.05S_VCCST +VCCIO_OUT
close to CPU
R310 75_4
R311 *75_4
H_CPU_SVIDALRT_N
R309 43_4
VR_SVID_ALERT# 35

SVID DATA

+V1.05S_VCCST +VCCIO_OUT
close to CPU
R308 130_4
R305 *130_4
VR_SVID_DATA

+V1.05S_VCCST +VCCIO_OUT
close to VR
R49 130_4
R48 *130_4
EC-A03
VR_SVID_DATA 35

SVID CLK

EC-A03 +V1.05S_VCCST +VCCIO_OUT
close to VR
R52 54.9_4
R51 *54.9_4
VR_SVID_CLK
VR_SVID_CLK 35
C567 0.1U/10V_4
+V1.05S_VCCST

PROJECT : LZ5
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 8/12	1A

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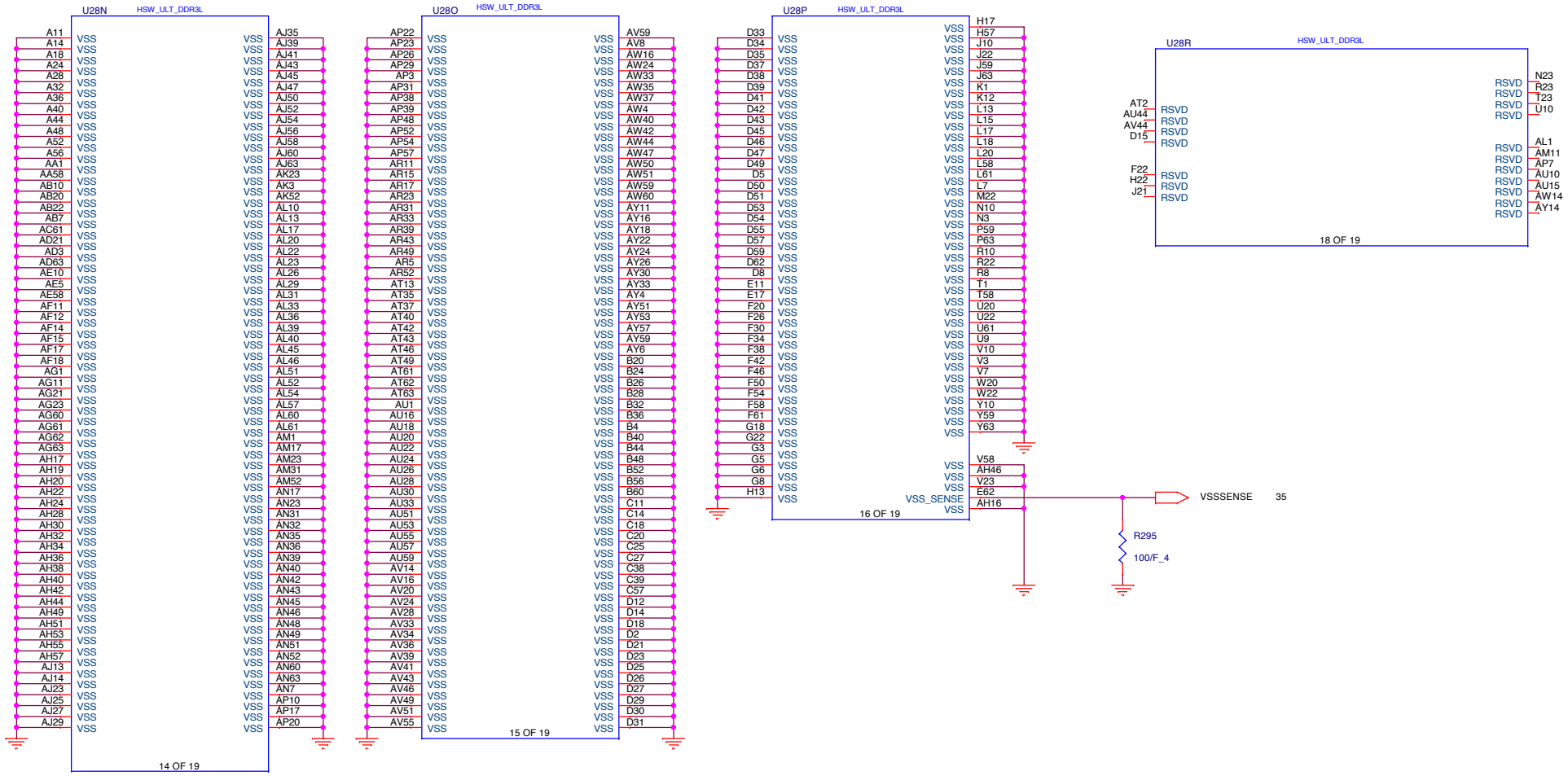
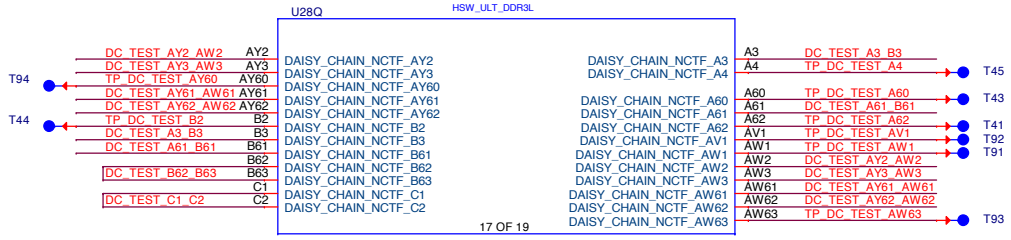
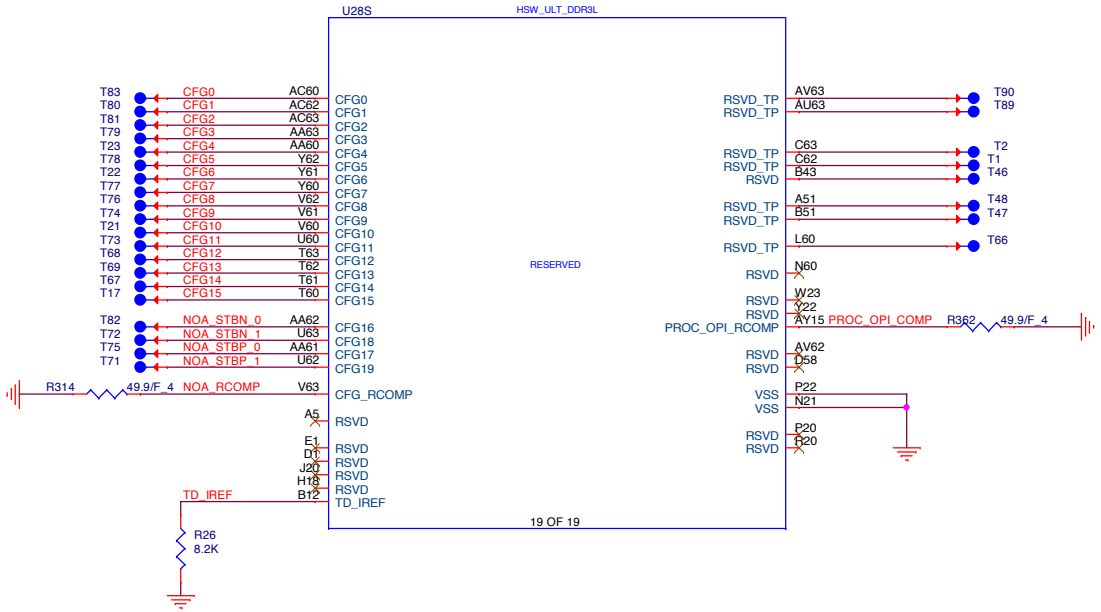
Haswell ULT (GND)





PROJECT : LZ5		
Quanta Computer Inc.		
Size	Document Number: Haswell ULT 9/12	Rev: 1A
Date: Wednesday, February 27, 2013	Sheet 10 of 37	



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R326 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R323 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R320 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R65 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R319 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R316 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R61 *1K_4

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Quanta Computer Inc.
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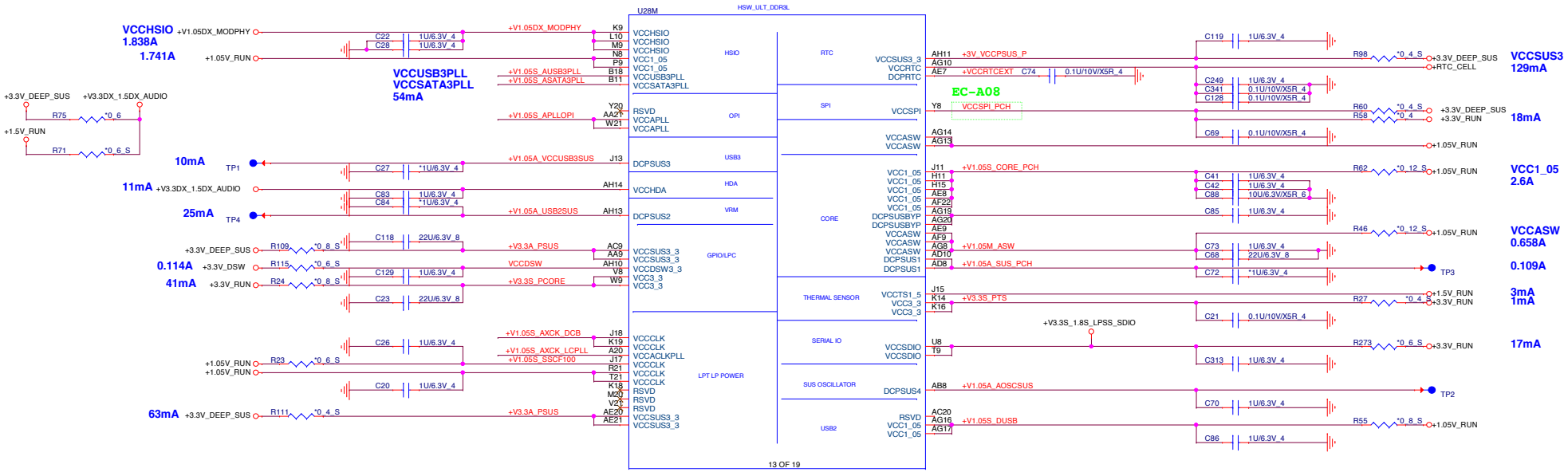
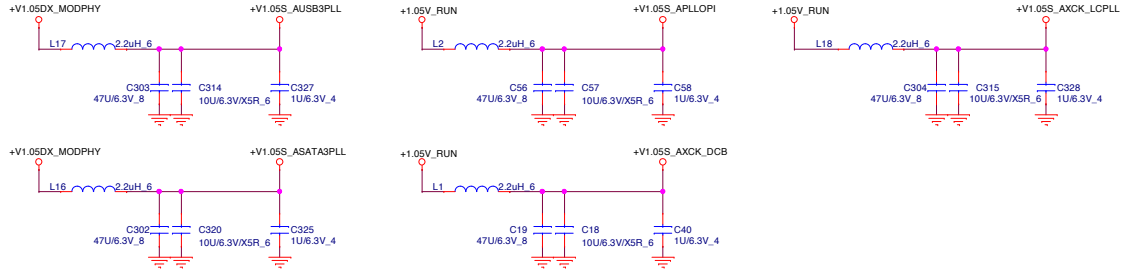
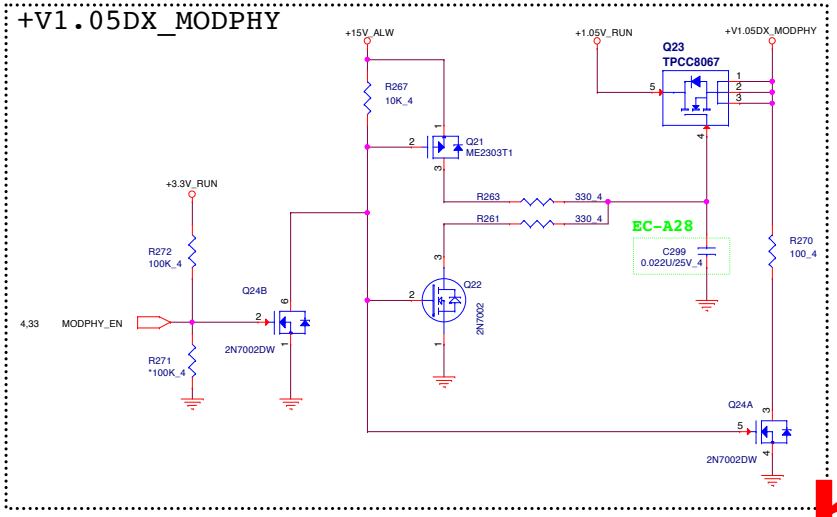
Haswell ULT PCH(POWER)



+V1.05DX_MODPHY





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Quanta Computer Inc.
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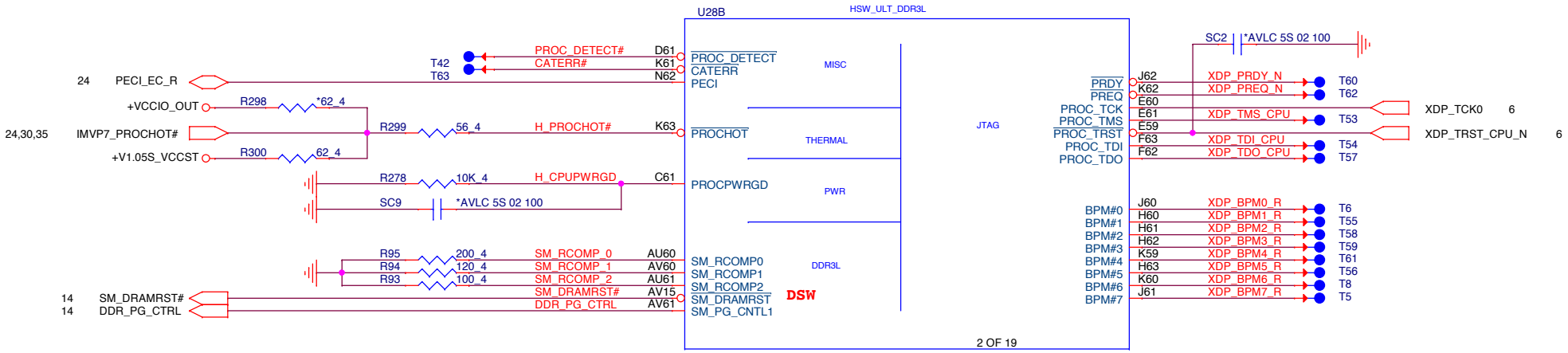
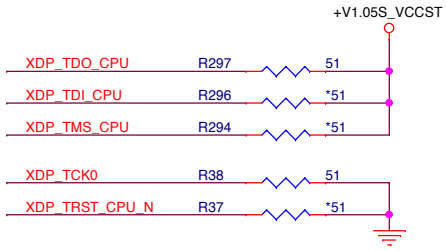
4,9 +V1.05S_VCCST
9 +VCCIO_OUT





PROJECT : LZ5
Quanta Computer Inc.

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	Haswell ULT 12/12	1A
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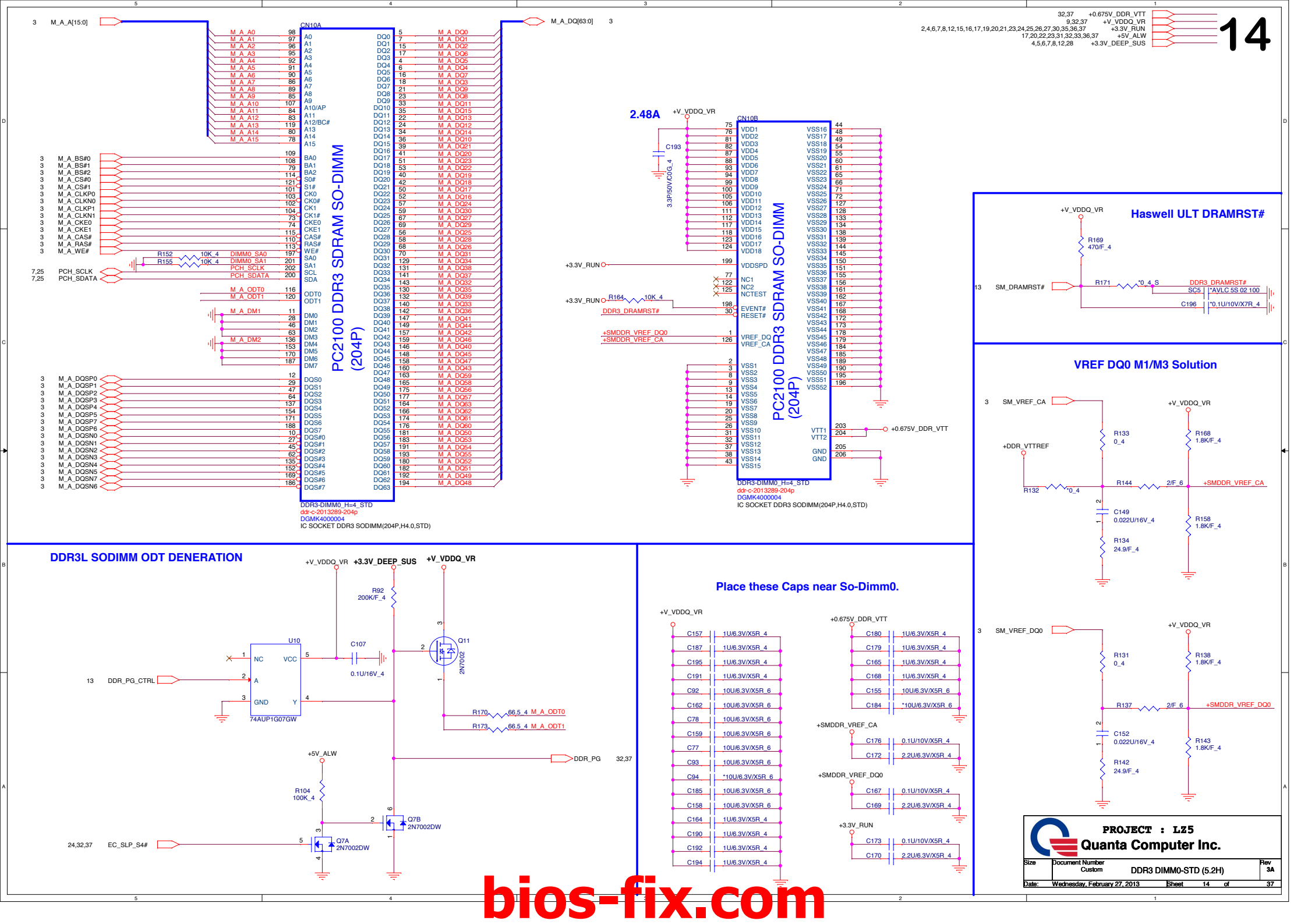
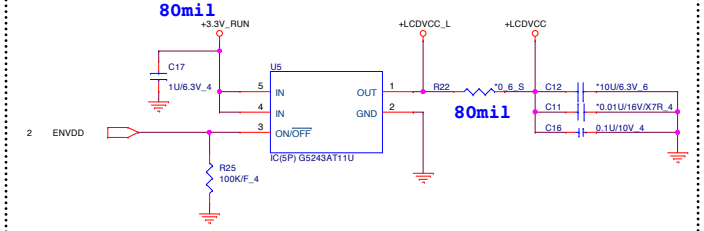
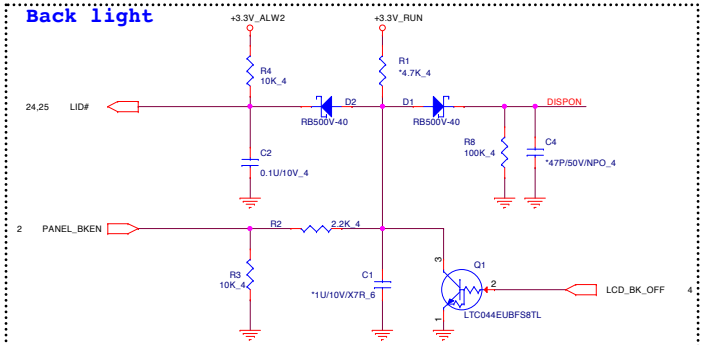

CN10A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4_STD
ddr-c-2013289-204p
DGMK4000004
IC SOCKET DDR3 SODIMM(204P,H4.0,STD)
CN10B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4_STD
ddr-c-2013289-204p
DGMK4000004
IC SOCKET DDR3 SODIMM(204P,H4.0,STD)
2.48A
Haswell ULT DRAMRST#
VREF DQ0 M1/M3 Solution
DDR3L SODIMM ODT DENERATION
Place these Caps near So-Dimm0.
PROJECT : LZ5
Quanta Computer Inc.
DDR3 DIMM0-STD (5.2H)
Wednesday, February 27, 2013

LCDVCC

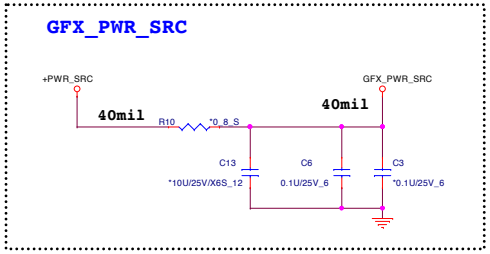
80mil

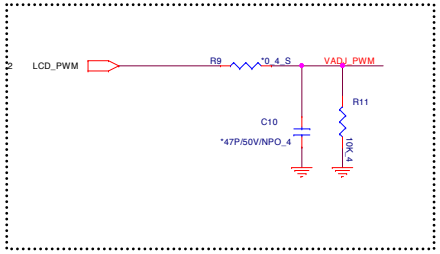


Back light



GFX_PWR_SRC



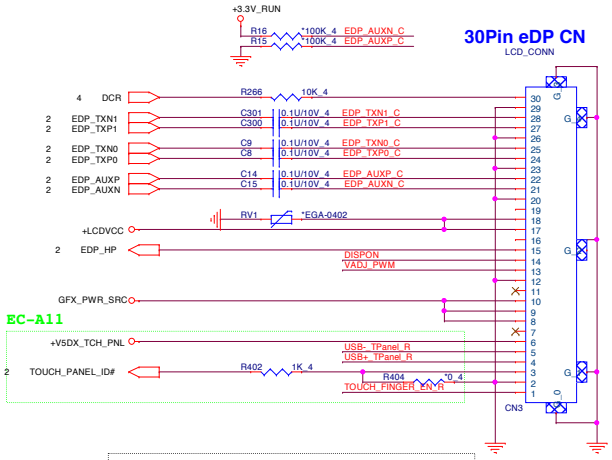


eDP Touch Panel

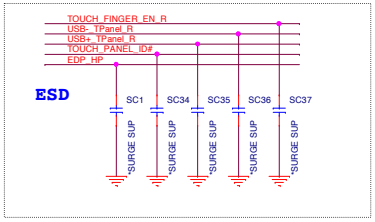
30Pin eDP CN

LCD_CONN

EC-A11



ESD



EC-A13

Touch Panel Interface

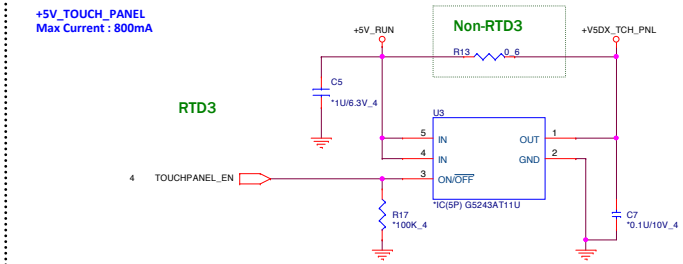
USB interface

Touch Panel VCC Control

+5V_TOUCH_PANEL
Max Current : 800mA

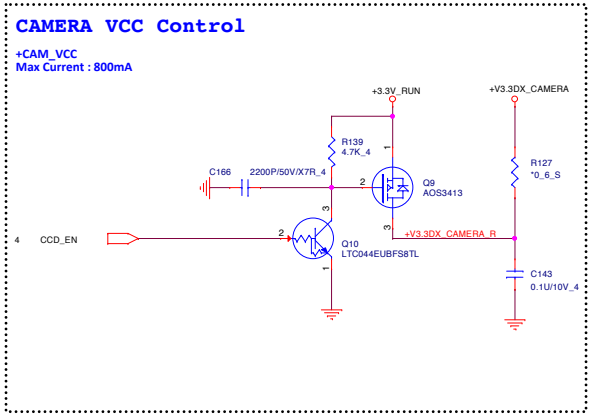
Non-RTD3

RTD3



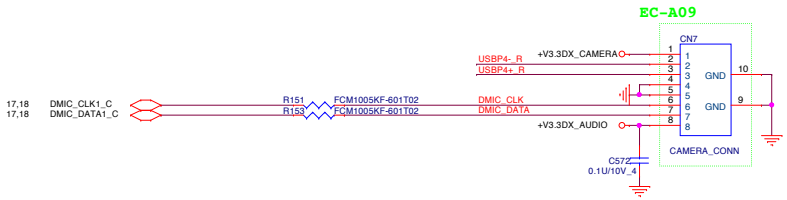
CAMERA VCC Control

+CAM_VCC
Max Current : 800mA

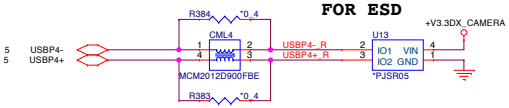


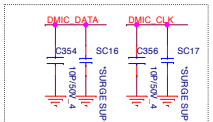
CAMERA/DMIC CONN

EC-A09



FOR ESD





For EMI, Close to CONN

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Quanta Computer Inc.		
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	LCD/CAMERA/Touch Panel	1A
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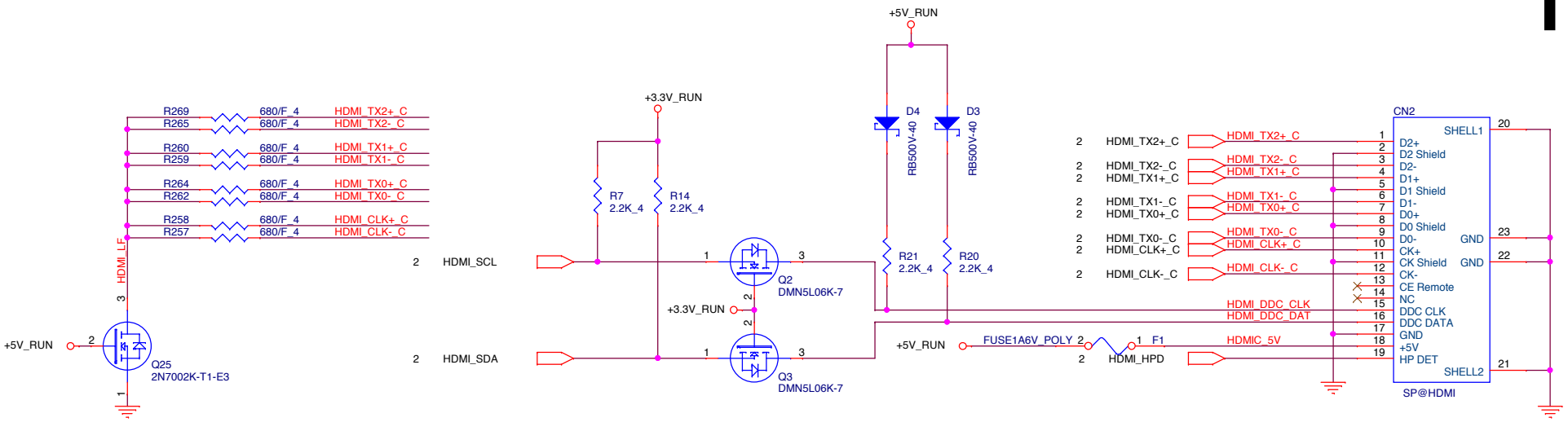
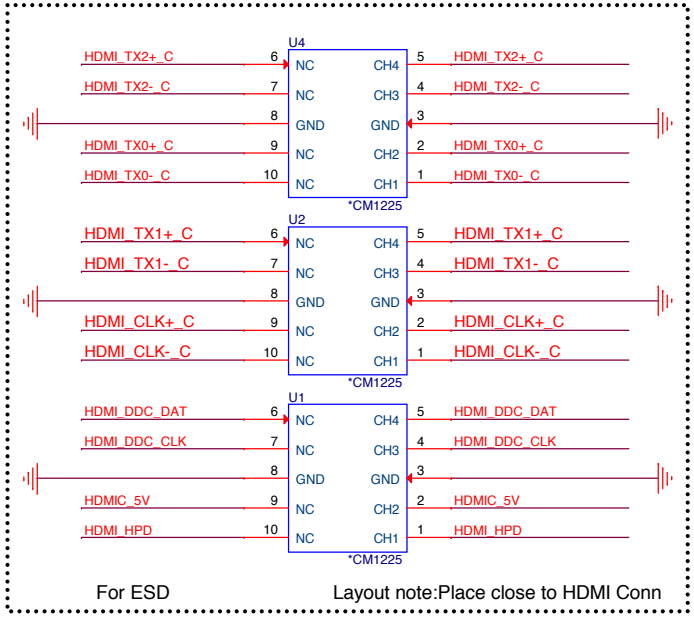
2,4,6,7,8,12,14,15,17,19,20,21,23,24,25,26,27,30,35,36,37
15,17,19,25,27,30,35,36,37

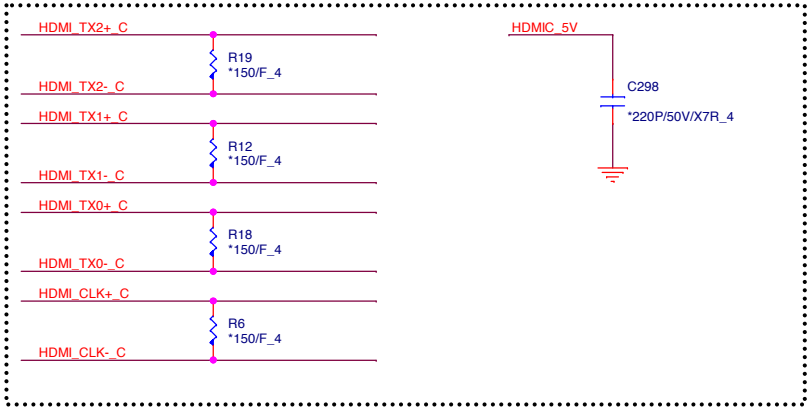
+3.3V_RUN
+5V_RUN



For ESD



EMI reserve for HDMI



PROJECT : LZ5
Quanta Computer Inc.

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	HDMI CONN	1A
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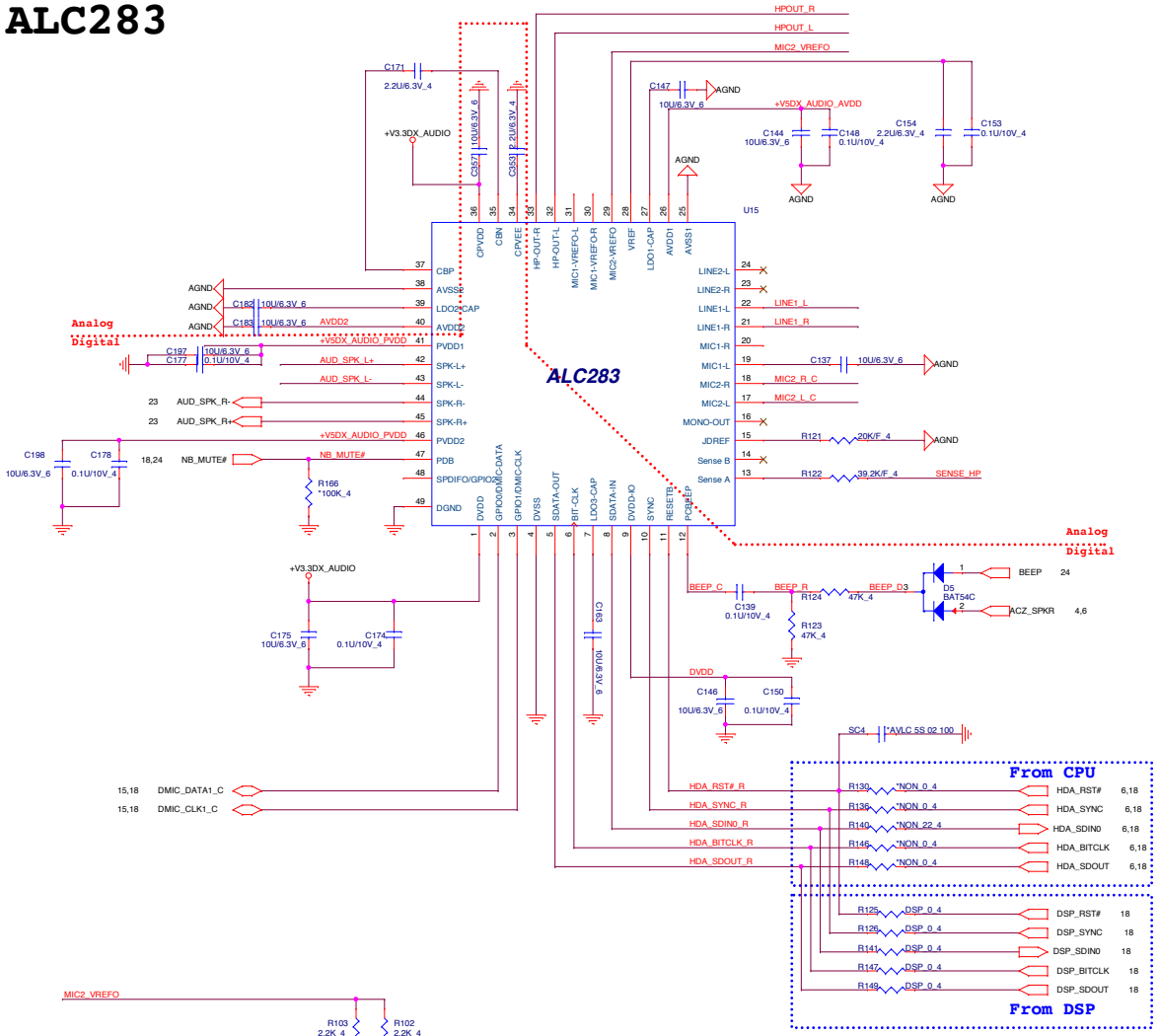
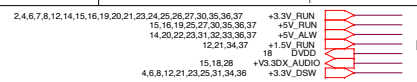
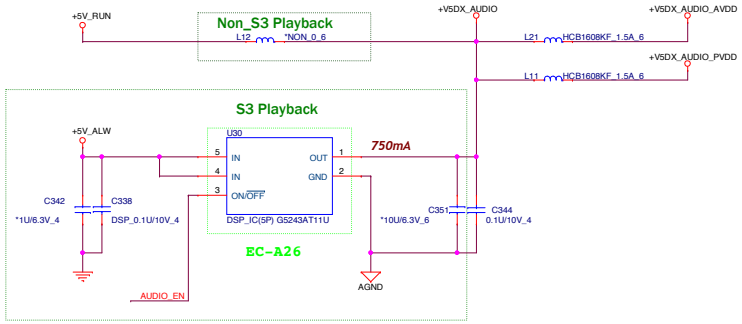
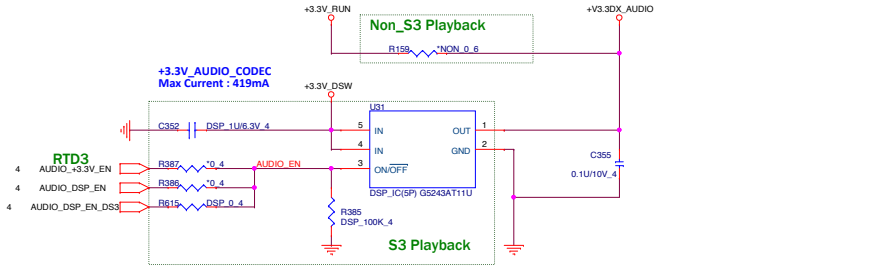
ALC283

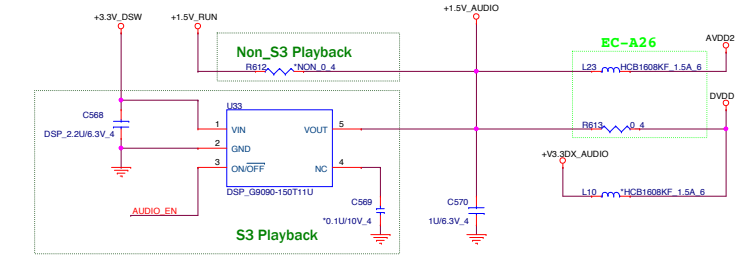




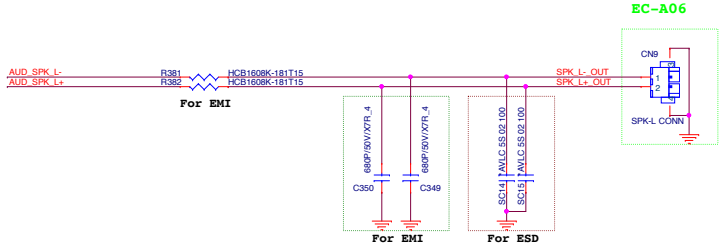
CODEC 5V POWER







INT Speaker



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Quanta Computer Inc.

Size	Document Number	Rev
	Audio(ALC283)	1A

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15,17,28 +V3.3DX_AUDIO
17 DVDD

+1.2V_SWR
C98 DSP_4.7U/6.3V/X5R
C105 DSP_0.1U/10V_4
+DVDD-25-LDO-O
R72 DSP_20K/F_4
C104 DSP_0.1U/10V_4
R67 DSP_20K/F_4
C90 DSP_0.1U/10V_4
+DSP_VREF_IN
+DVDD-25-LDO-O
+V3.3DX_AUDIO
C103 DSP_0.1U/10V_4
C96 DSP_10U/6.3V_6
EC-A10
15,17 DMIC_CLK1_C R408 DSP_0_4 DMIC_CLK1_R
15,17 DMIC_DATA1_C R409 DSP_0_4 DMIC_DATA1_R
+1.2V_SWR
C101 DSP_4.7U/6.3V/X5R
C102 DSP_0.1U/10V_4
28 DSP_XTAL24_IN R69 *0_4
C100 DSP_18P/50V/_4 XTAL24_DSP_IN
Y1 DSP_24MHz R77 DSP_1M_4
C99 DSP_18P/50V/_4 XTAL24_DSP_OUT

U9 ALC5505 DSP_ALC5055

1	DVDD-12-I	37	
2	XTAL-IN	38	I2SCLKI
3	XTAL-OUT	39	I2SLRCKI
4	VGPIO3/VOL-DN/TDI	40	DDR-VREF
5	SDATA-OUT/I2SSDO0-2	41	I2SSDIO
6	BITCLK/I2SCLKI-2	42	DVDD-33
7	VGPIO0-TRST#	43	DVDD-25-LDO-O
8	SDATA-IN/I2SSDI0-2	44	DVSS
9	DVDD-IO	45	VDMIC-CLK2/I2SSDI1
10	SYNC/I2SLRCLK1-2	46	VDMCI-DATA2/I2SSDI2
11	RESETB	47	VDIMC-CLK
12	DVSS-SWR	48	VDMIC-DAT1
		49	DGND

36	SO	24	SDATA-OUT-V/I2SSD01
35	SI	23	BITCLK-V/MCLKI-2
34	SCK	22	VGPIO5/VOL-MUTE/TDO
33	CS-L	21	VGPIO1/SDATA-IN-V/I2SSDI3
32	MCLKO	20	VGPIO4/VOL-UP/TCLK
31	I2SSDO0	19	SYNC-V/I2SSDO2
30	I2SSCLRCKO	18	RESTB-V/I2SSDO3
29	I2SCLKO	17	DSP-DP#
28	VGPIO2/TMS	16	DVDD-33-SWR-C
27	I2C-MASTER-SCL/I2C-SLAVE-SCL	15	FB-SWR
26	I2C-MASTER-SDA/I2C-SLAVE-SDA	14	DVDD-33-SWR
25	DVDD-12-I	13	DVDD-12-SWR

T38
I2C0_SCL 4
I2C0_SDA 4
+1.2V_SWR
C125 DSP_4.7U/6.3V/X5R
C123 DSP_0.1U/10V_4
DSP_SDOUT 17
DSP_BITCLK 17
T39
DSP_SDIN0 17
T40
DSP_SYNC 17
DSP_RST# 17
NB_MUTE# 17,24
+1.2V_SWR
+V3.3DX_AUDIO_R
+1.2V_SWR_L L9 DSP_4.7uH/0.9A_8
C133 DSP_10U/6.3V_6
C132 DSP_0.1U/10V_4
AGND
C134 DSP_10U/6.3V_6
C131 DSP_0.1U/10V_4
AGND
R112 DSP_0_6 +V3.3DX_AUDIO
+1.2V_SWR
C136 *10U/6.3V_6
C130 DSP_4.7U/6.3V/X5R
C124 DSP_0.1U/10V_4
AGND
AGND
T33
T35
HDA_RST# 6,17
HDA_SYNC 6,17
DVDD
HDA_SDIN0_D
R85 DSP_33_4
HDA_SDIN0 6,17
HDA_BITCLK 6,17
HDA_SDOUT 6,17
C106 DSP_10P/50V_4
C108 DSP_10P/50V_4
C112 DSP_10P/50V_4
C114 DSP_10P/50V_4

PROJECT : LZ5
Quanta Computer Inc.

Size	Document Number	Rev
	DSP(ALC5055)	1A

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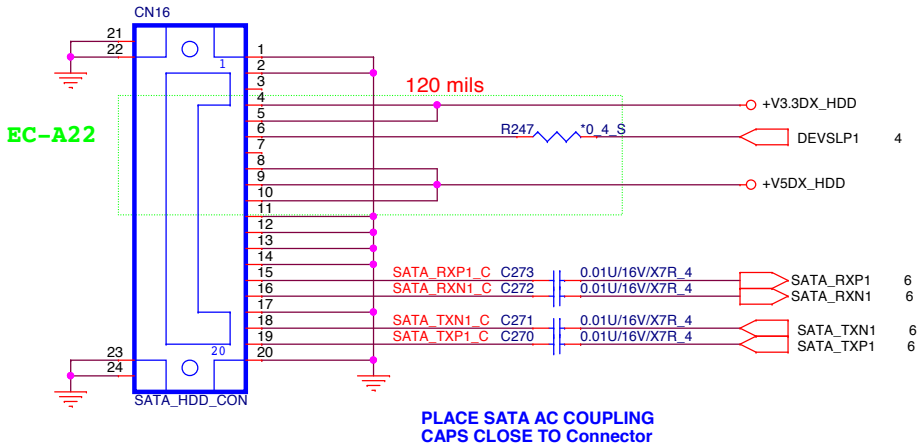
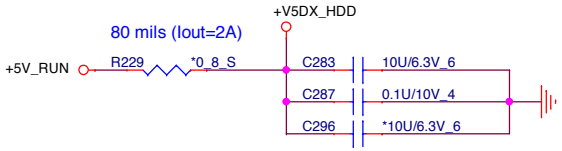
HDD

2,4,6,7,8,12,14,15,16,17,20,21,23,24,25,26,27,30,35,36,37 +3.3V_RUN
15,16,17,25,27,30,35,36,37 +5V_RUN

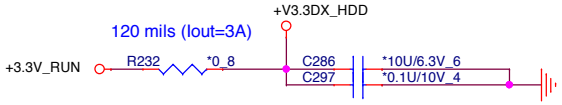


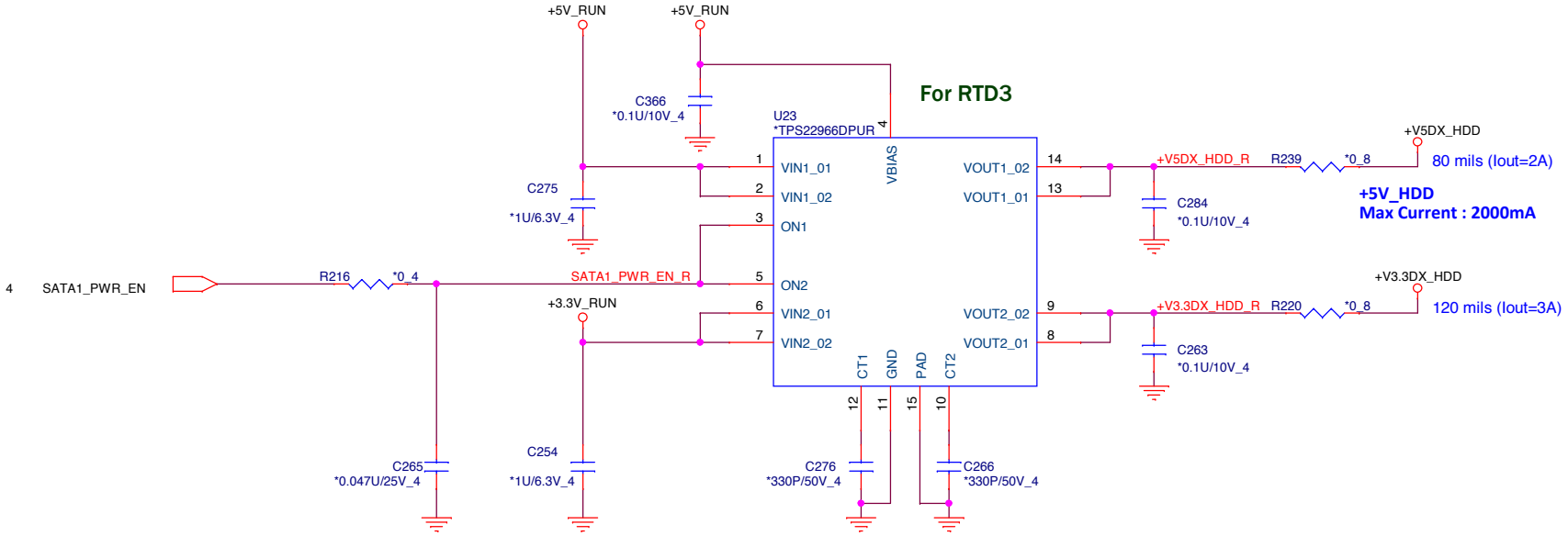
PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)





PROJECT : LZ5
Quanta Computer Inc.

Size	Document Number	Rev
	SATA	1A
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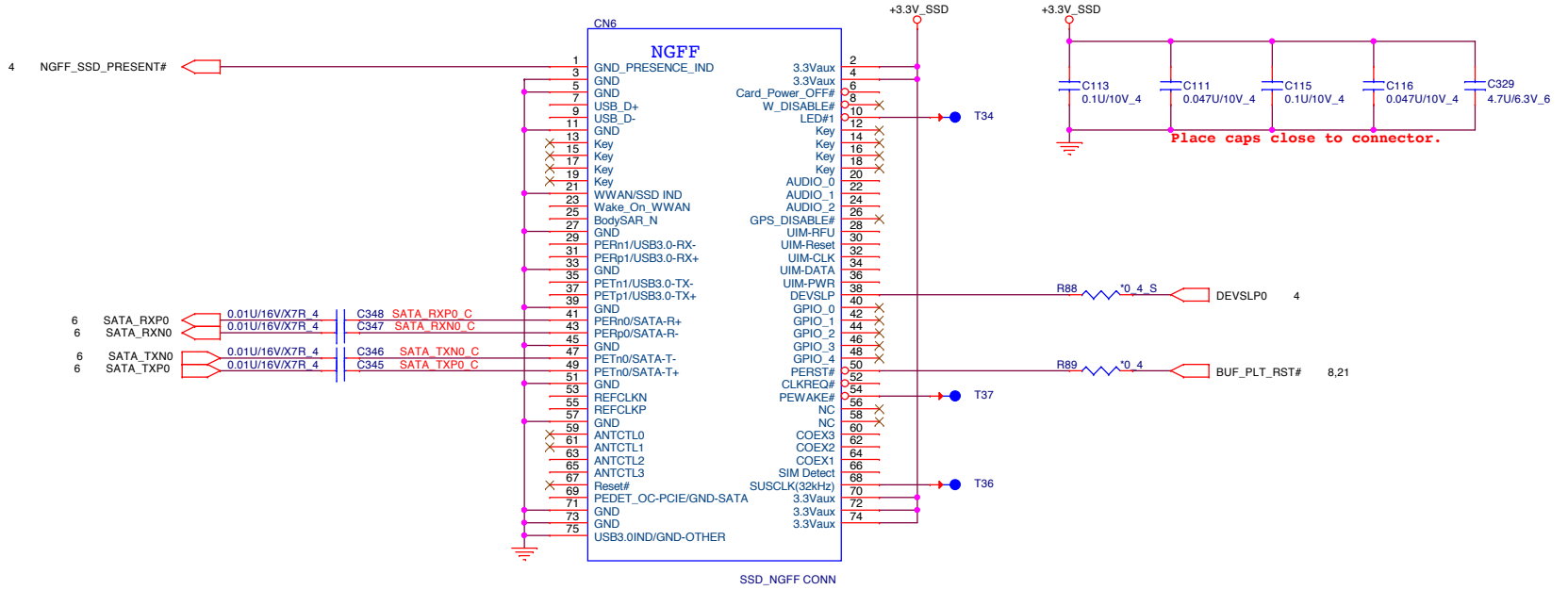
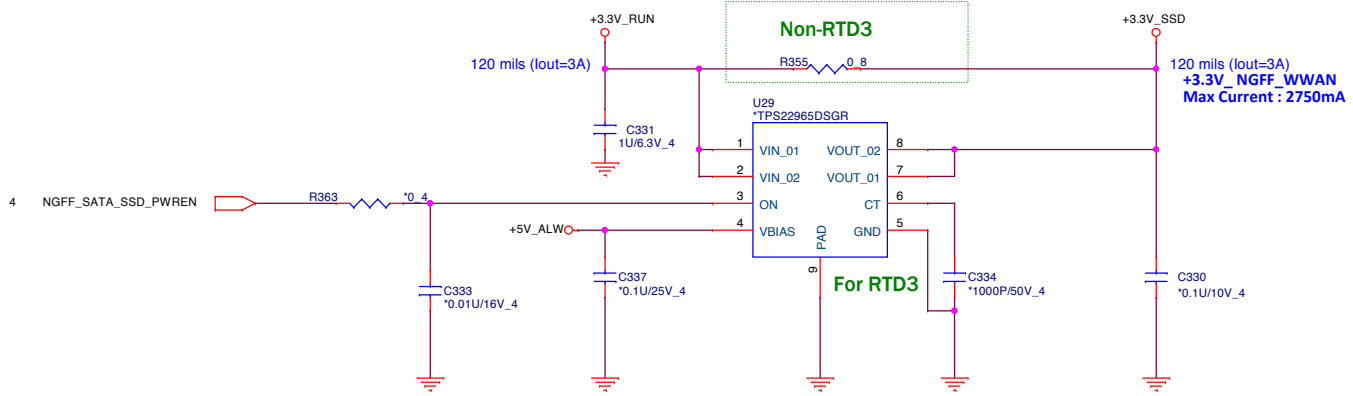
NGFF SSD connector





PROJECT : LZ5

Quanta Computer Inc.

Size	Document Number	Rev
	SSD NGFF	1A

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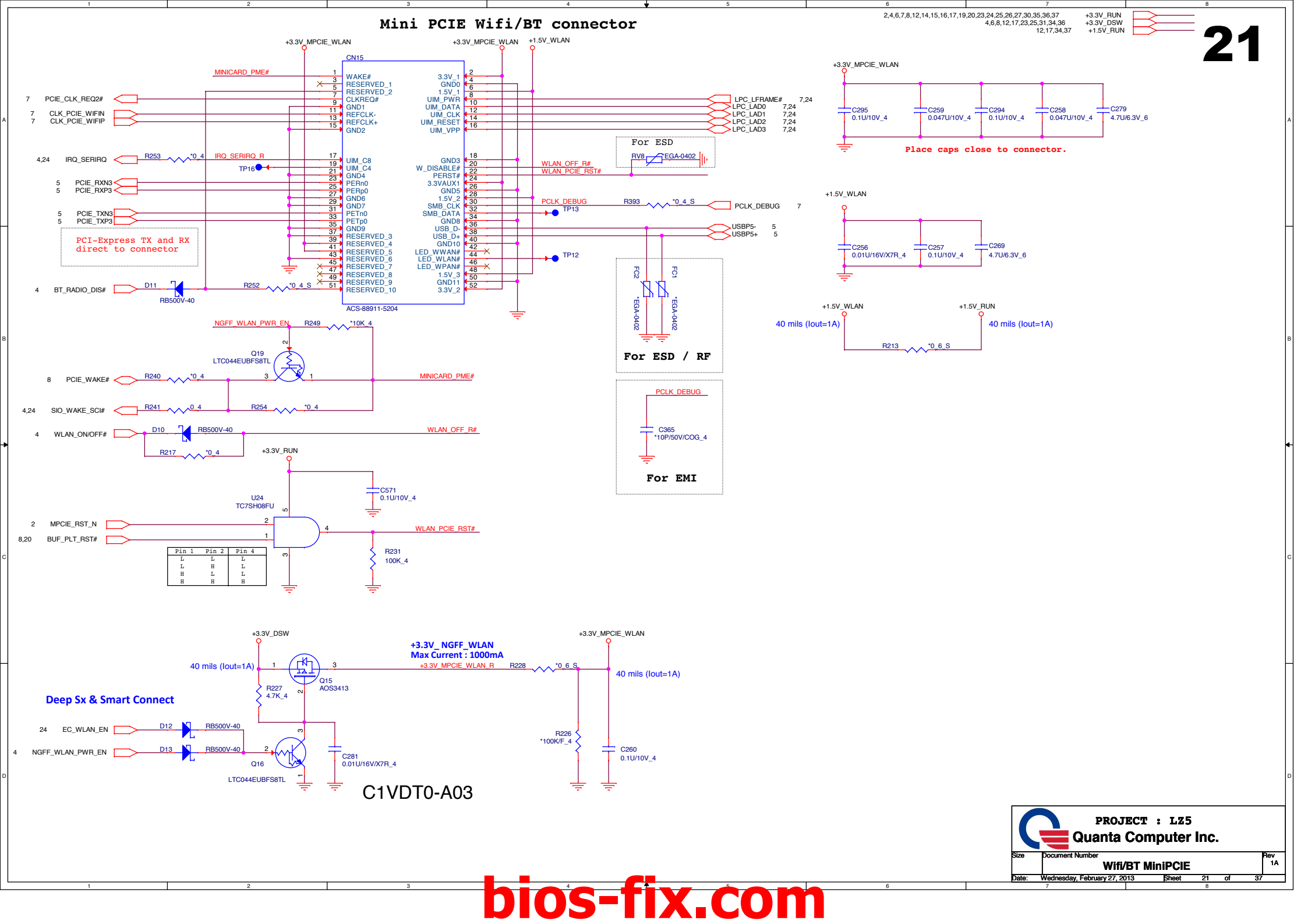
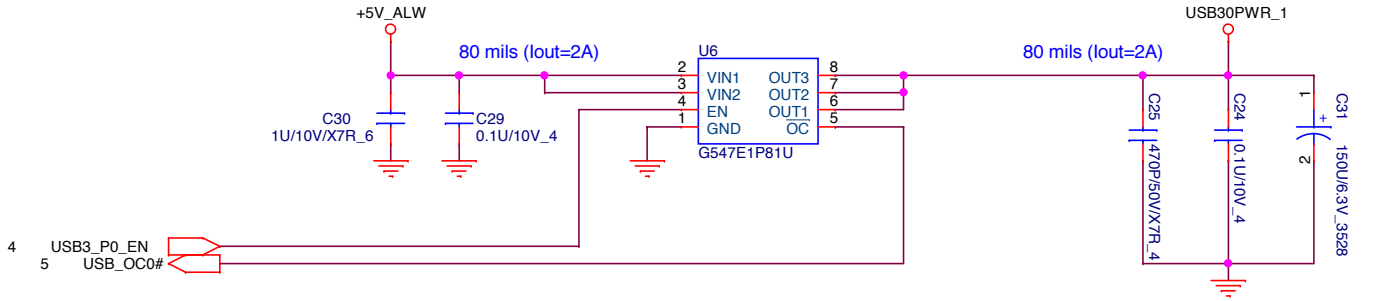
Mini PCIE Wifi/BT connector

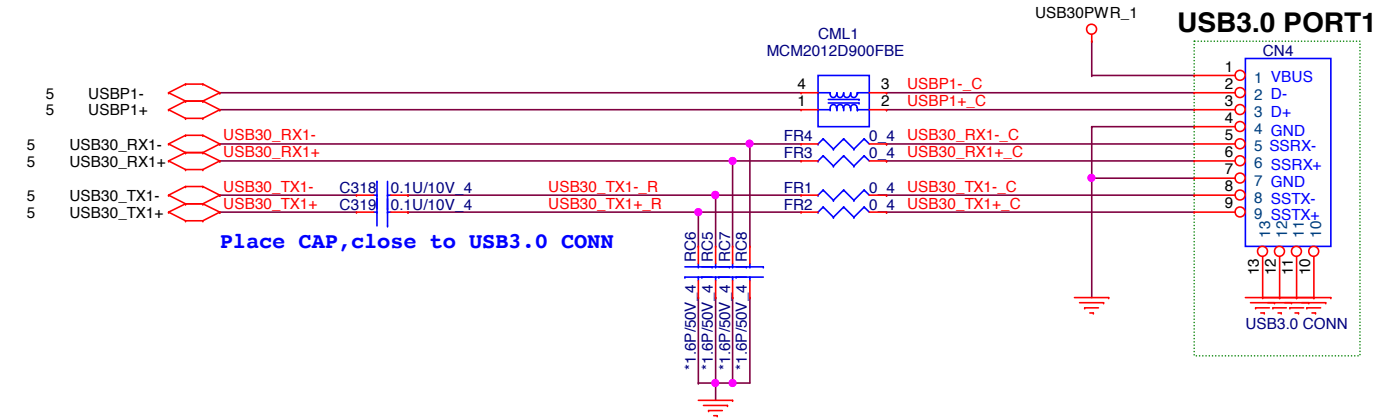


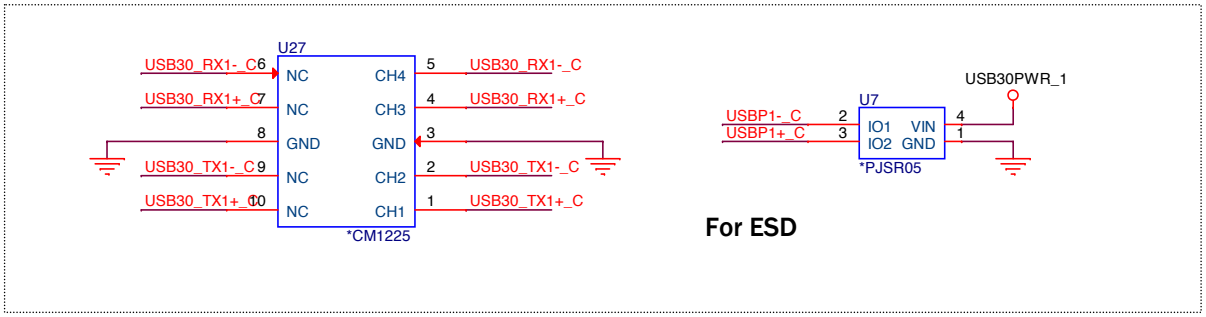
PROJECT : LZ5

Quanta Computer Inc.

Size	Document Number	Rev
	Wifi/BT MiniPCIE	1A
Date: Wednesday, February 27, 2013	Sheet 21 of 37	







PROJECT : LZ5

Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x1	1A
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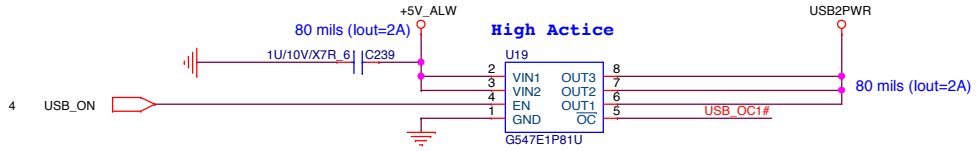
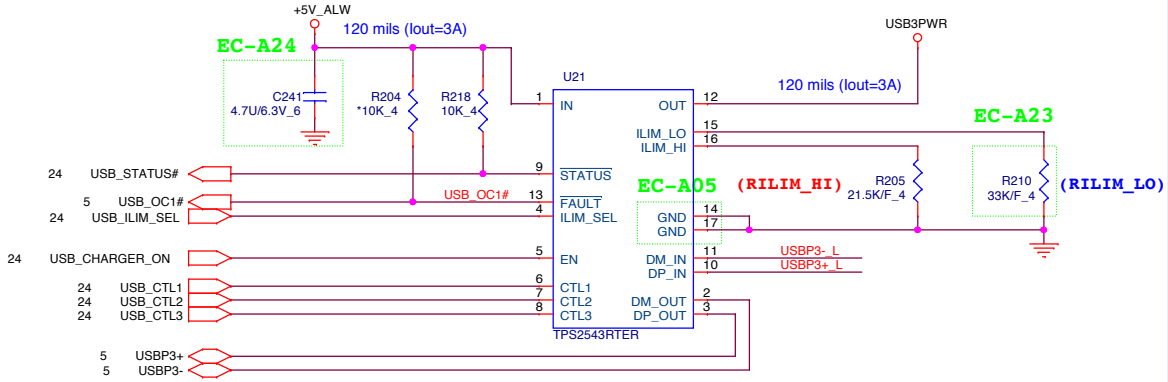
USB 2.0 Port



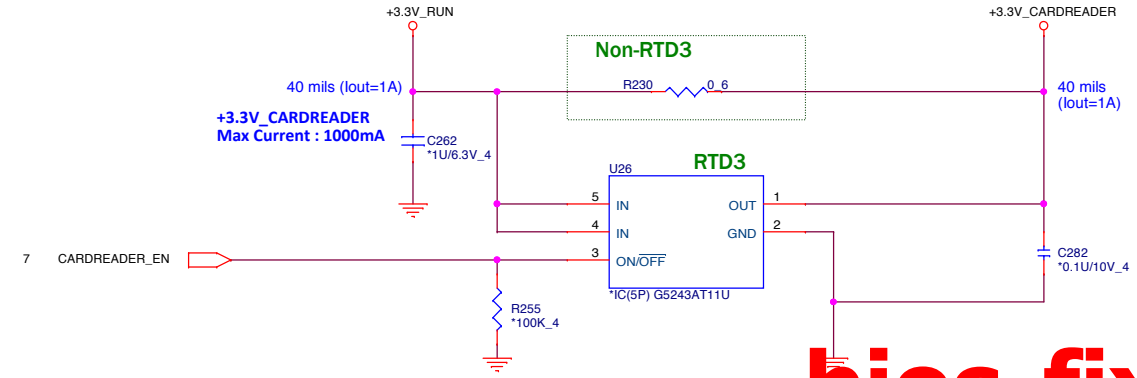
USB Charger 2.0 Port



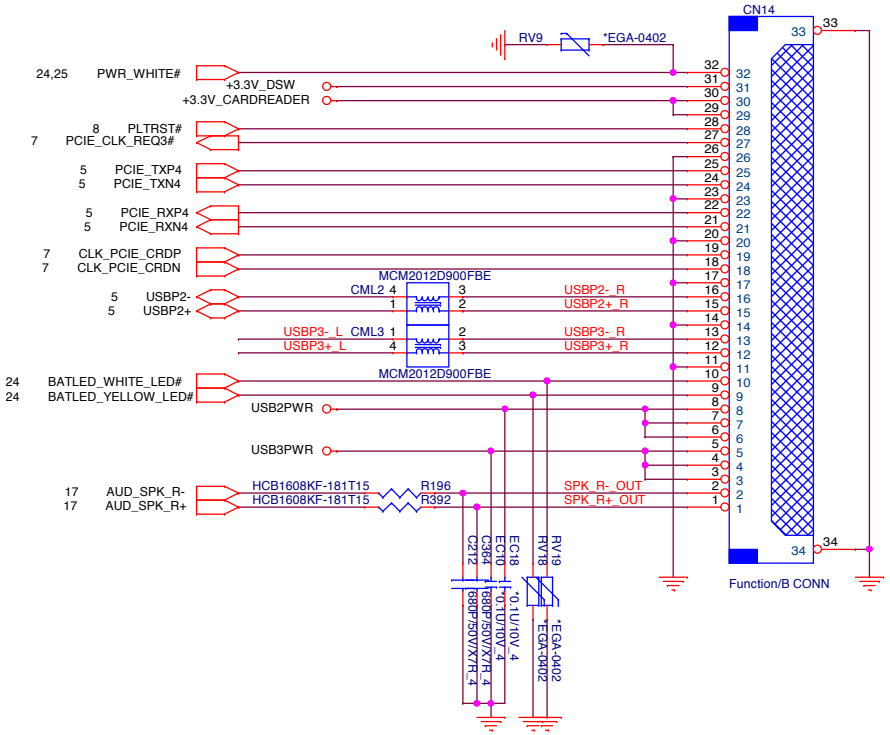
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

Card Reader VCC Control



14,17,20,22,31,32,33,36,37 +5V_ALW
4,6,8,12,17,21,25,31,34,36 +3.3V_DSW
2,4,6,7,8,12,14,15,16,17,19,20,21,24,25,26,27,30,35,36,37 +3.3V_RUN



	PROJECT : LZ5 Quanta Computer Inc.		
Size	Document Number USB2.0--Audio Jack Conn		Rev 1A
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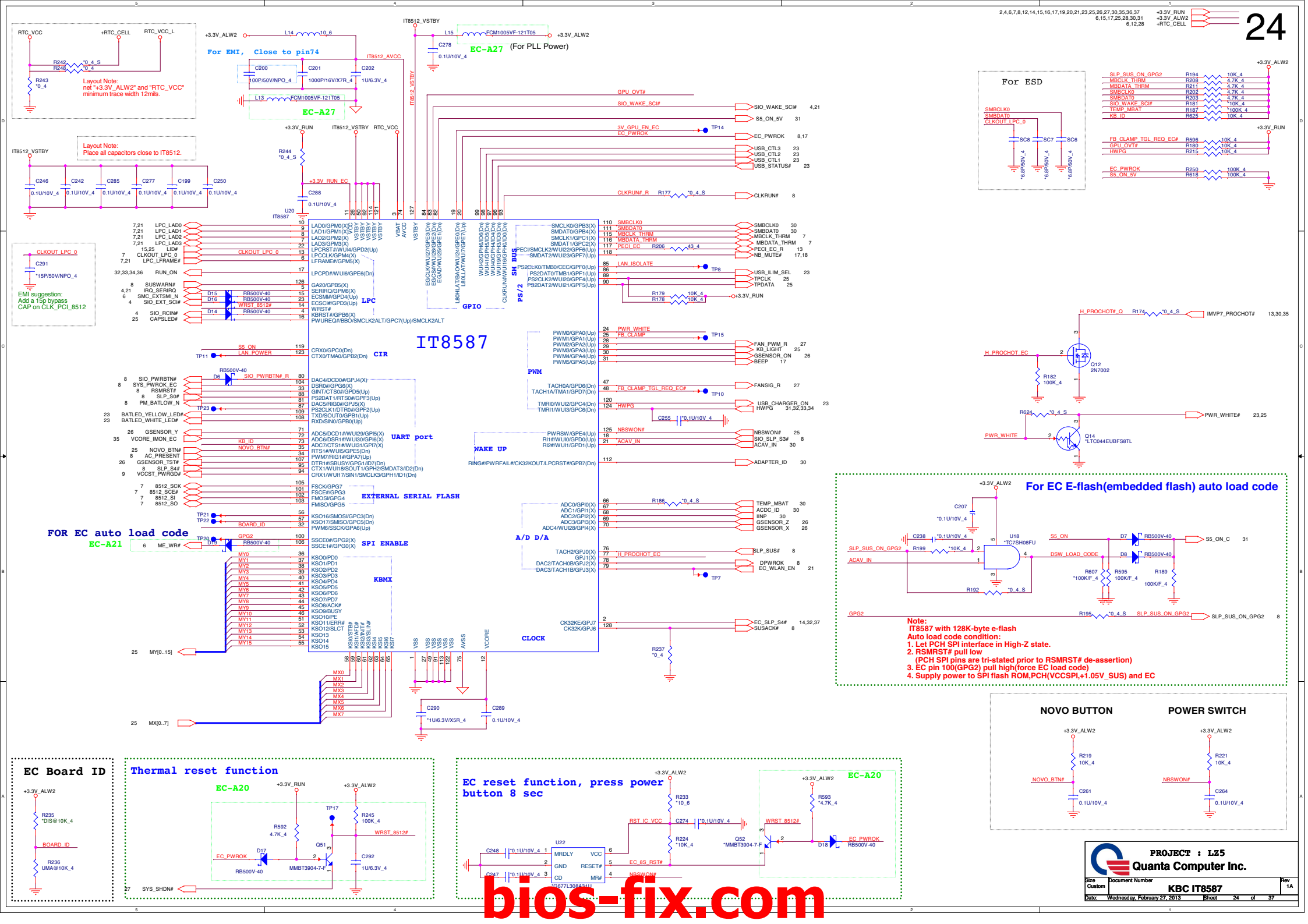

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Quanta Computer Inc.	
Size: Custom	Document Number: KBC IT8587
Rev: 1A	
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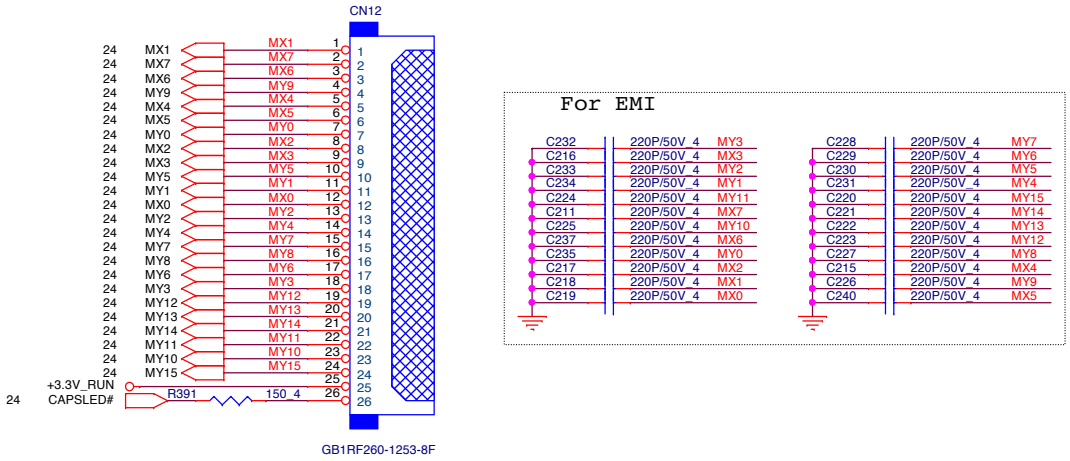
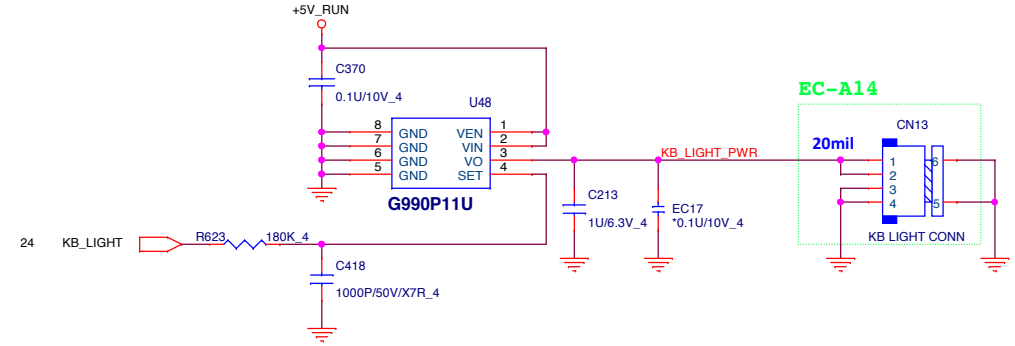
KEYBOARD

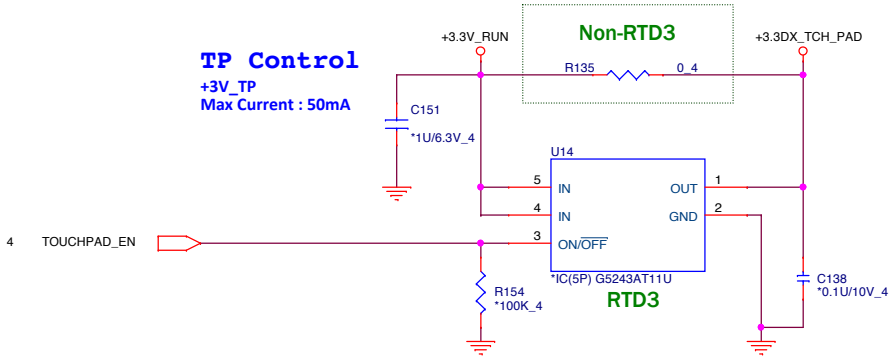


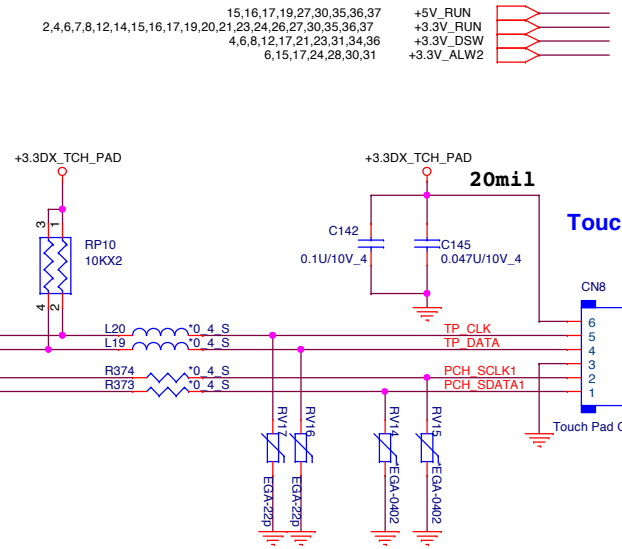
KB Backlit



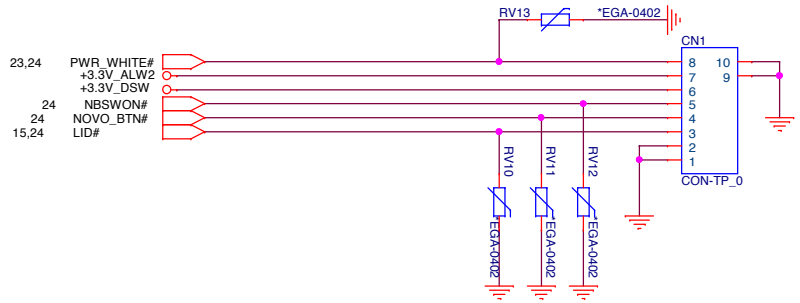
TP Control

+3V_TP
Max Current : 50mA





Power Board CONN



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Quanta Computer Inc.		
Size	Document Number	Rev
	KB/TP/LID	1A
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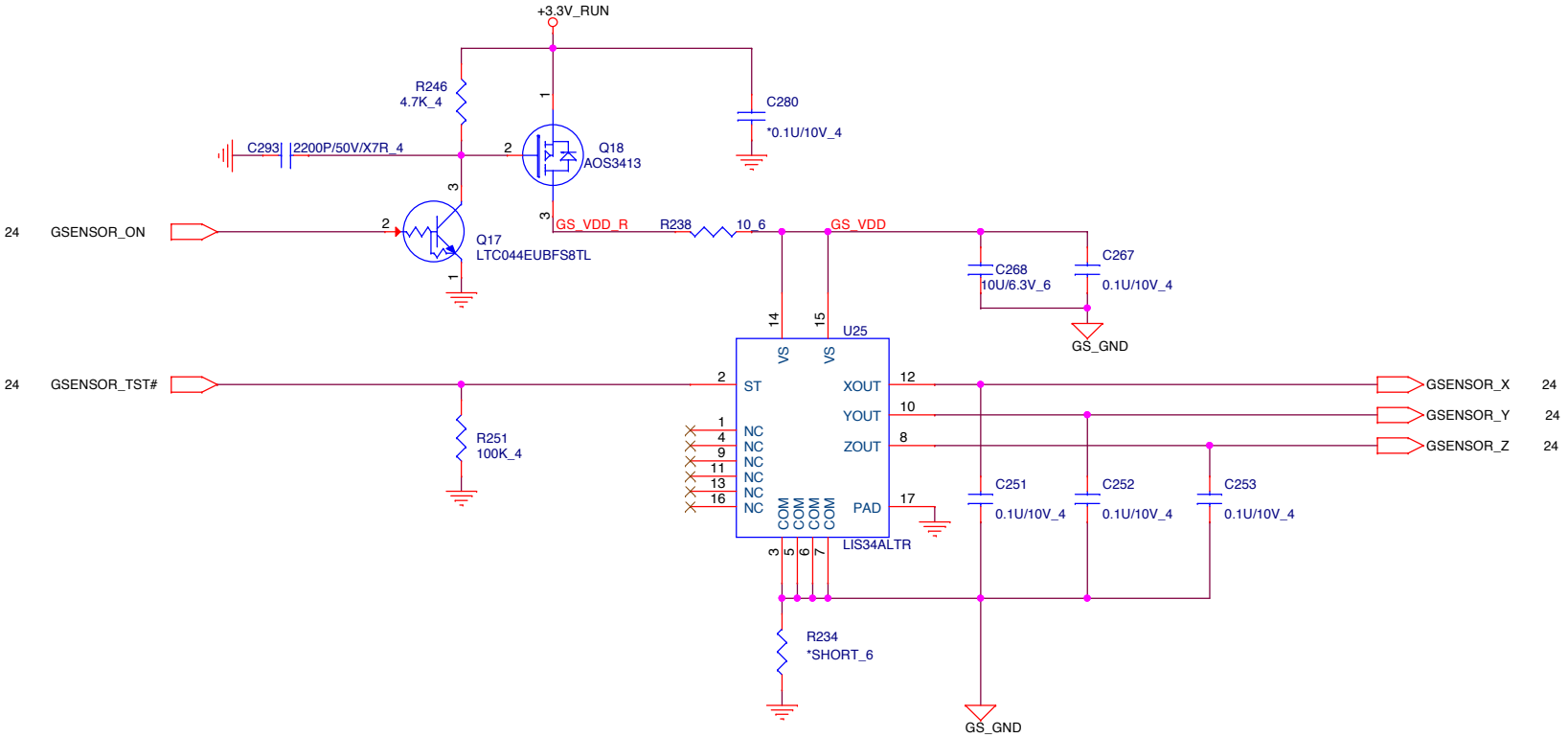
G-SENSOR (3-Axial)

2,4,6,7,8,12,14,15,16,17,19,20,21,23,24,25,27,30,35,36,37 +3.3V_RUN



PROJECT : LZ5

Quanta Computer Inc.

Size	Document Number	Rev
	SW/LED/G-sensor	1A
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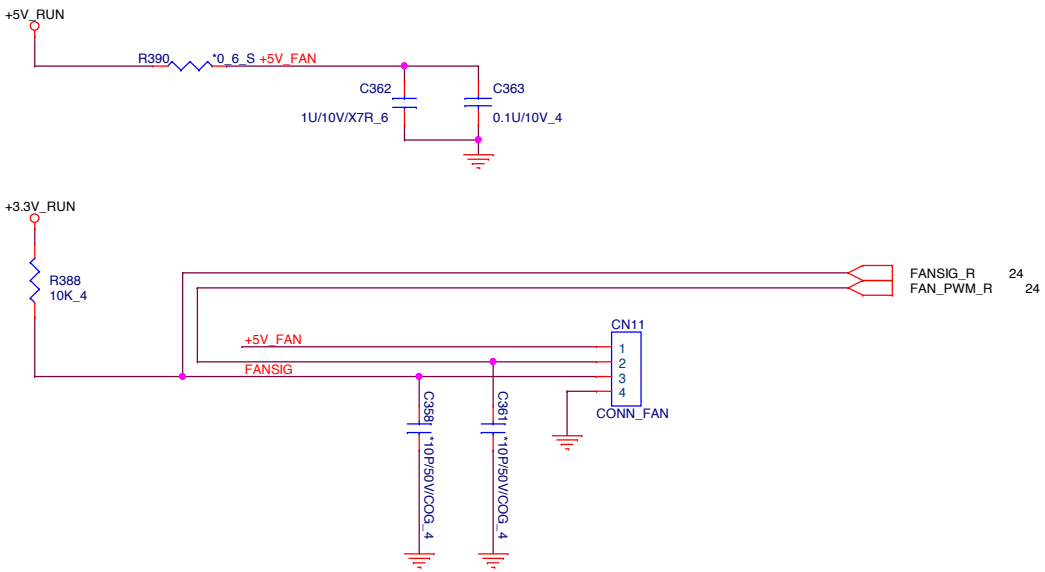
FAN CONTROL

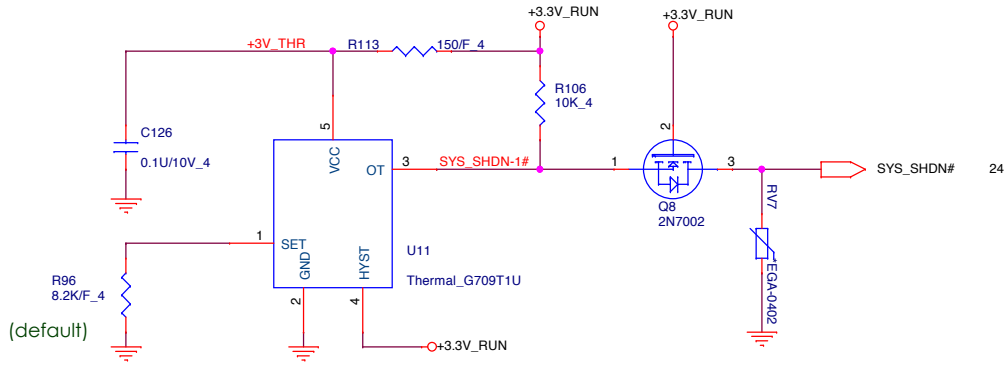
2,4,6,7,8,12,14,15,16,17,19,20,21,23,24,25,26,30,35,36,37
15,16,17,19,25,30,35,36,37

+3.3V_RUN
+5V_RUN

27



Thermal Sensor



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Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal	1A
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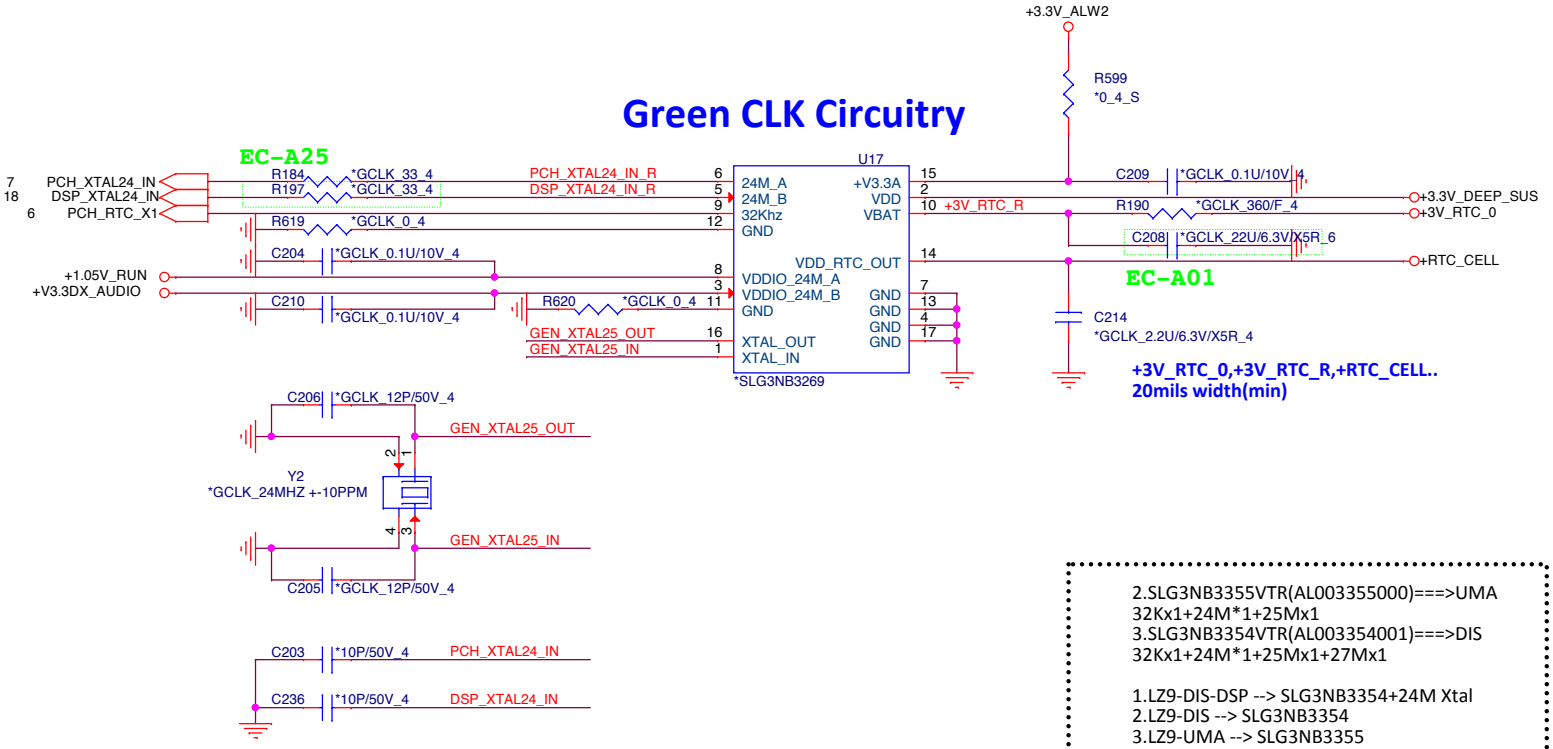
6,15,17,24,25,30,31 +3.3V_ALW2
15,17,18 +V3.3DX_AUDIO
6 +3V_RTC_0
6,12,24 +RTC_CELL
6,9,12,33,37 +1.05V_RUN
4,5,6,7,8,12,14 +3.3V_DEEP_SUS

Green CLK Circuitry



+3V_RTC_0,+3V_RTC_R,+RTC_CELL..
20mils width(min)

2.SLG3NB3355VTR(AL003355000)===>UMA
32Kx1+24M*1+25Mx1
3.SLG3NB3354VTR(AL003354001)===>DIS
32Kx1+24M*1+25Mx1+27Mx1

1.LZ9-DIS-DSP --> SLG3NB3354+24M Xtal
2.LZ9-DIS --> SLG3NB3354
3.LZ9-UMA --> SLG3NB3355
3.LZ9-UMA-DSP --> SLG3NB3389
4.LZ5-UMA-DSP – SLG3NB3269

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Quanta Computer Inc.

Size	Document Number	Rev
	Green Clock	1A
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15,30,31,32,33,35 +PWR_SRC

HOLE4
h-tc146bc217d126p2

HOLE9
h-tc146bc217d102p2

HOLE8
h-tc146bc217d102p2

HOLE5
*h-tc185bc157d146p2

HOLE6
*h-tc165bc157d146p2

+PWR_SRC

EC1	0.1U/25V/X5R_4
EC11	0.1U/25V/X5R_4
EC9	0.1U/25V/X5R_4
EC5	0.1U/25V/X5R_4
EC3	0.1U/25V/X5R_4

HOLE7
*H-C87D87N

HOLE3
*H-C87D87N

HOLE1
*hg-tc256bc217d110p2

HOLE2
*HG-TC256BC217D98P2

HOLE11
*hg-tc256bc217d102p2

HOLE10
*HG-TC256BC217D110P2

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Quanta Computer Inc.

Size	Document Number	Rev
	Screw Hole/EMI	1A
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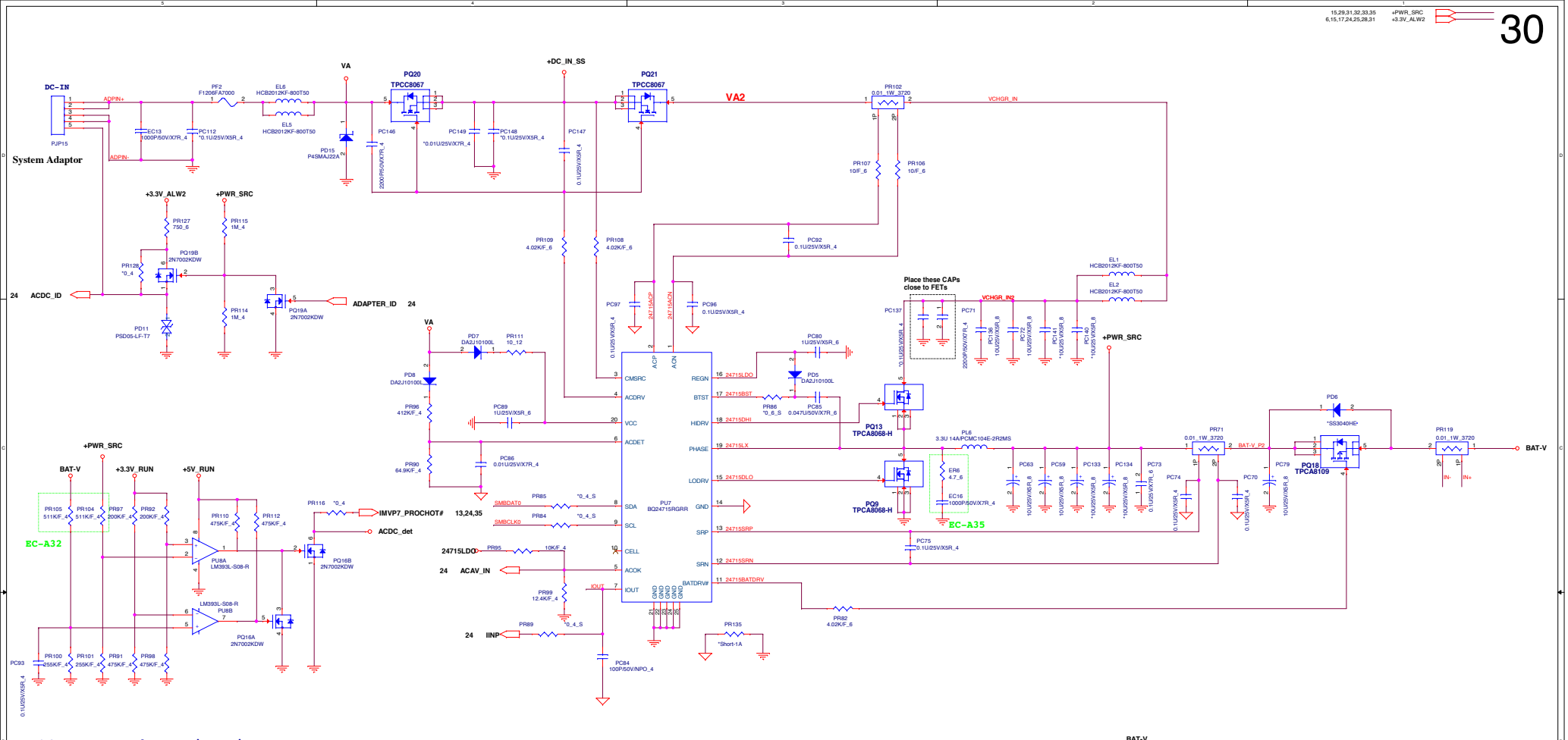
DC-IN
System Adaptor
ADPIN+
ADPIN-
VA
+DC_IN_SS
PQ20 TPCC8067
PQ21 TPCC8067
VA2
VCHGR_IN
+3.3V_ALW2
+PWR_SRC
ACDC_ID
ADAPTER_ID
Place these CAPs close to FETs
PQ13 TPCA8068-H
PQ9 TPCA8068-H
PL6 3.3U 14A/PCMC104E-2R2MS
PQ18 TPCA8109
BAT-V
+5V_RUN
+3.3V_RUN
EC-A32
EC-A35
IMVP7_PROCHOT#
ACDC_det
24715LDO
ACAV_IN
IINP
IOUT
SMBDAT0
SMBCLK0
BQ24715RGRR
CMSRC
ACDRV
VCC
ACDET
REGN
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
BATDRV#
SDA
SCL
CELL
ACOK
IOUT
10ms one-shot circuit
EC-A33
EC-A34
IN+
IN-
VBATT
MBCLK
MBDATA
TEMP_MBAT
PROJECT : LZ5
Quanta Computer Inc.
CHARGER (BQ24715)
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+5V_ALW
5 Volt +/-5%
Fsw : 400KHz
TDC : 7A
OCP : 10A

+3.3V_DSW
3.3 Volt +/-5%
Fsw : 475KHz
TDC : 8A
OCP: 11A

Place these CAPs close to FETs

Place these CAPs close to FETs

+PWR_SRC

+3.3V_ALW2

+5V_ALW

+3.3V_DSW

+15V_ALW

PU6 TPS51285BRUKR

PQ12 TPCC8067

PQ11 TPCC8065

PQ8 TPCC8067

PQ10 TPCC8065

PL7 2.2UH/8A-PCMC063T-2R2MN

PL5 2.2UH/8A-PCMC063T-2R2MN

S5_ON_5V

S5_ON_C

S5_ON_R

HWPG

24,32,33,34

EC-A36

EC-A37

PD4 BAT54S-7-F

PD3 BAT54S-7-F

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Quanta Computer Inc.
DIS

Size	Document Number	Rev
	3V/5V (TPS51285)	1A
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15,29,30,31,33,35 +PWR_SRC
9,14,37 +V_VDDQ_VR
14,17,20,22,23,31,33,36,37 +5V_ALW
14,37 +0.675V_DDR_VTT
14 +DDR_VTTREF

32

+V_VDDQ_VR
1.35 Volt +/-5%
Fsw : 400KHz
TDC : 5A
OCP : 12A

+0.675V_DDR_VTT
TDC : 1A

EC-A38

PU5 AOZ1237
PU4 TPS51206DSQR

PROJECT : LZ5
Quanta Computer Inc.

Size	Document Number	Rev
	1.35V_DDR/0.675 (AOZ1237)	1A
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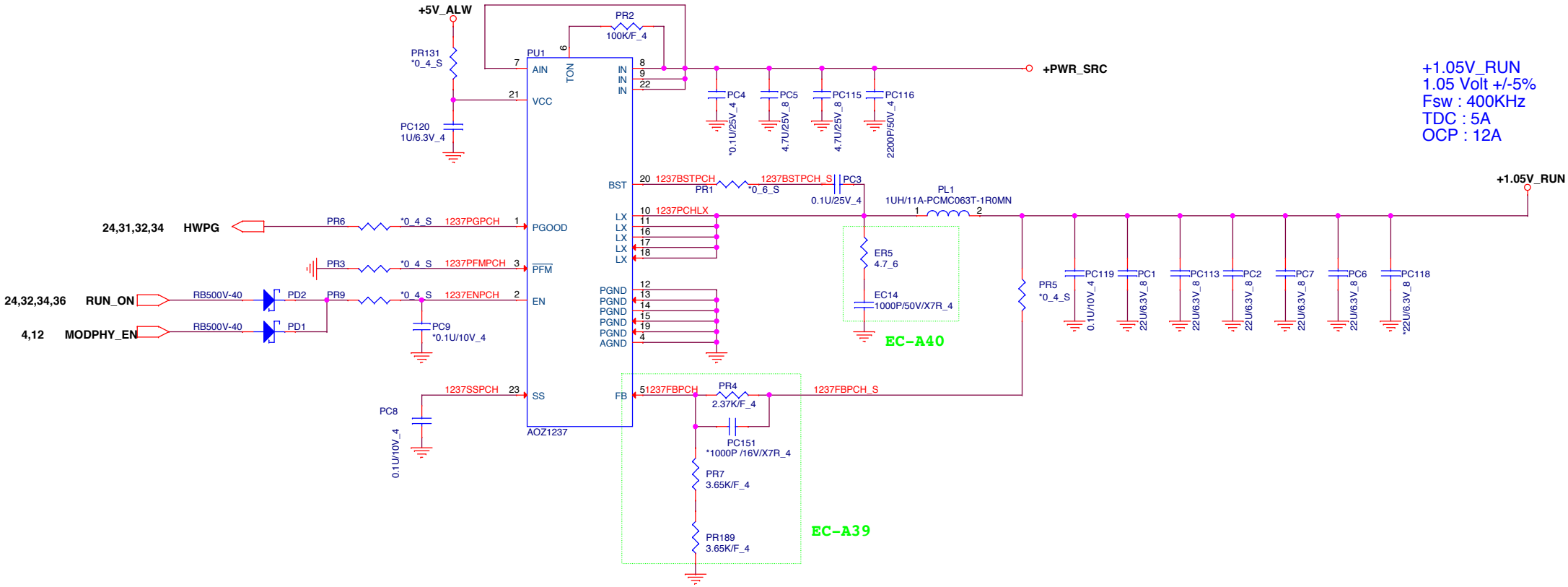
15,29,30,31,32,35 +PWR_SRC
6,9,12,28,37 +1.05V_RUN
14,17,20,22,23,31,32,36,37 +5V_ALW



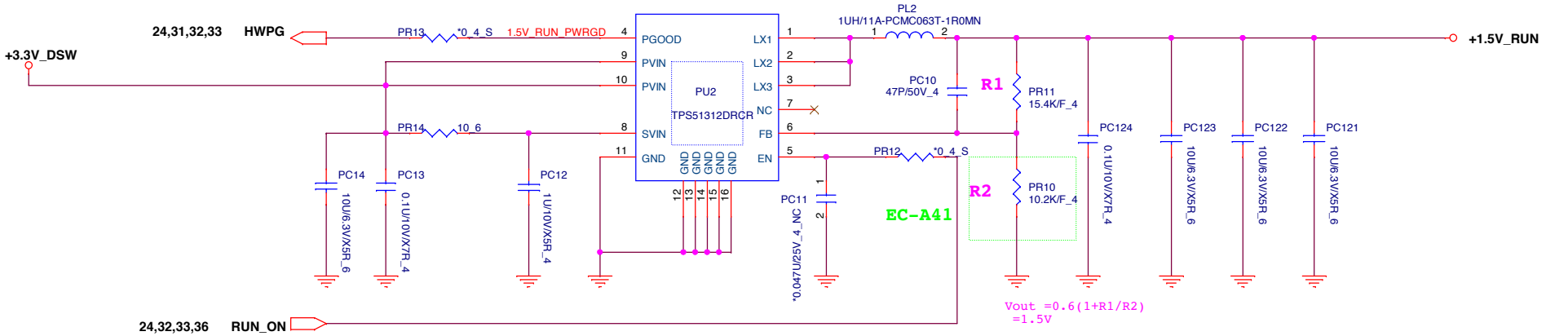
PROJECT : LZ5
Quanta Computer Inc.

Size	Document Number	Rev
	1.05V_RUN (AOZ1237)	1A
Date: Wednesday, February 27, 2013	Sheet 33 of 37	

15,29,30,31,32,33,35 +PWR_SRC
12,17,21,37 +1.5V_RUN
2,4,6,7,8,12,14,15,16,17,19,20,21,23,24,25,26,27,30,35,36,37 +3.3V_RUN

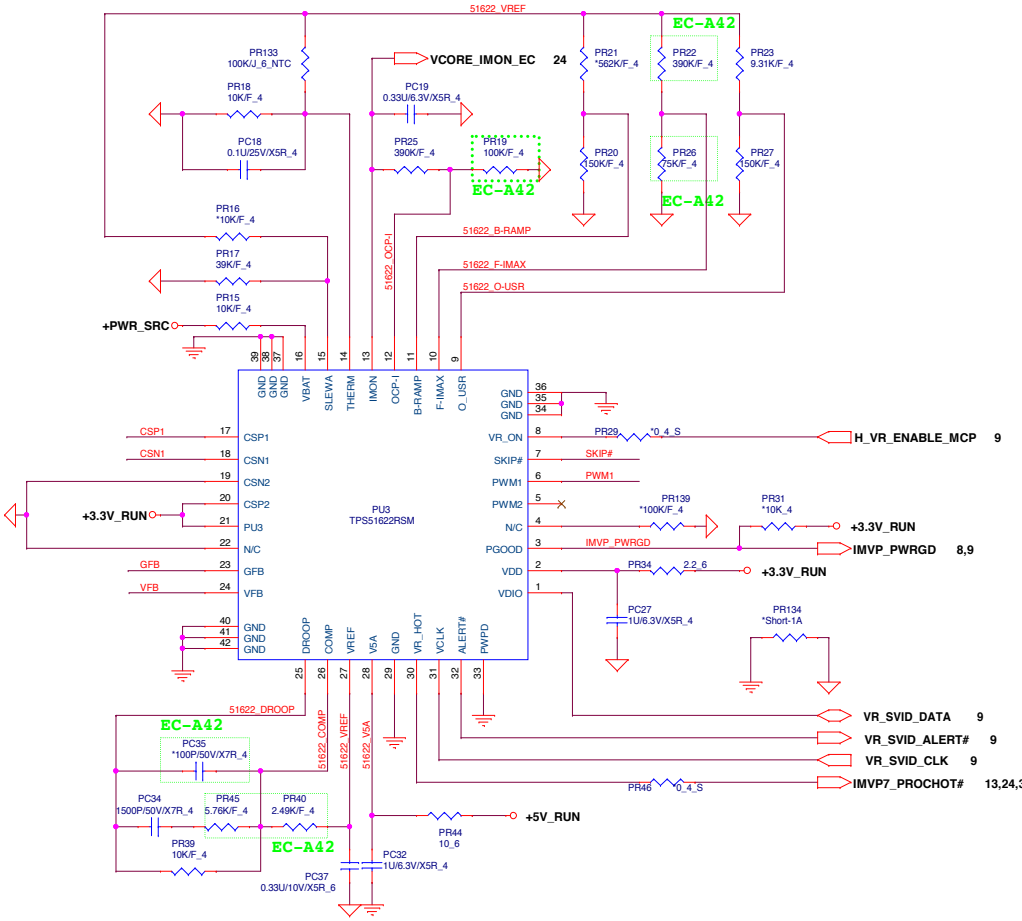
34

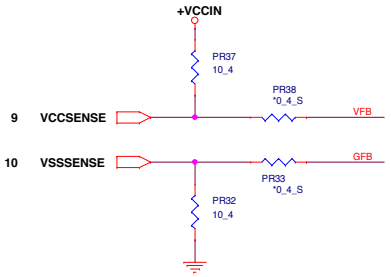
+1.5V_RUN
1.5 Volt +/-5%
Fsw : 900KHz
TDC : 3A
OCP : 4.8A



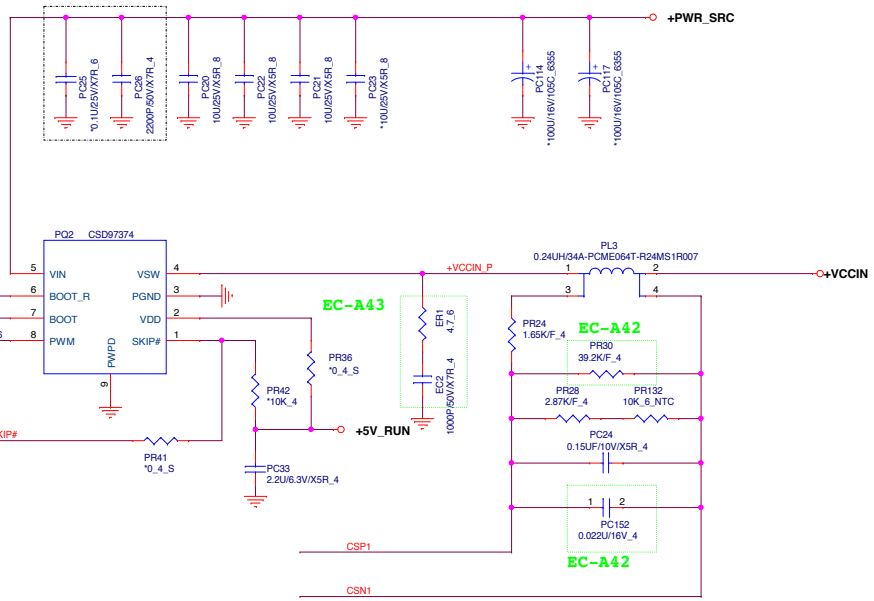
PROJECT : LZ5
Quanta Computer Inc.

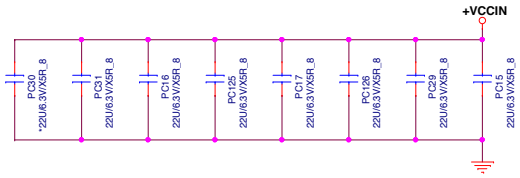
Size	Document Number	Rev
	1.5V_RUN (TPS51312)	1A
Date: Wednesday, February 27, 2013	Sheet 34 of 37	





Place these CAPs close to FETs






```
Icc_Max=32A
I_TDC=14A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=9m
AC_LL_VOS=9.4m
VBOOT=1.7V
```

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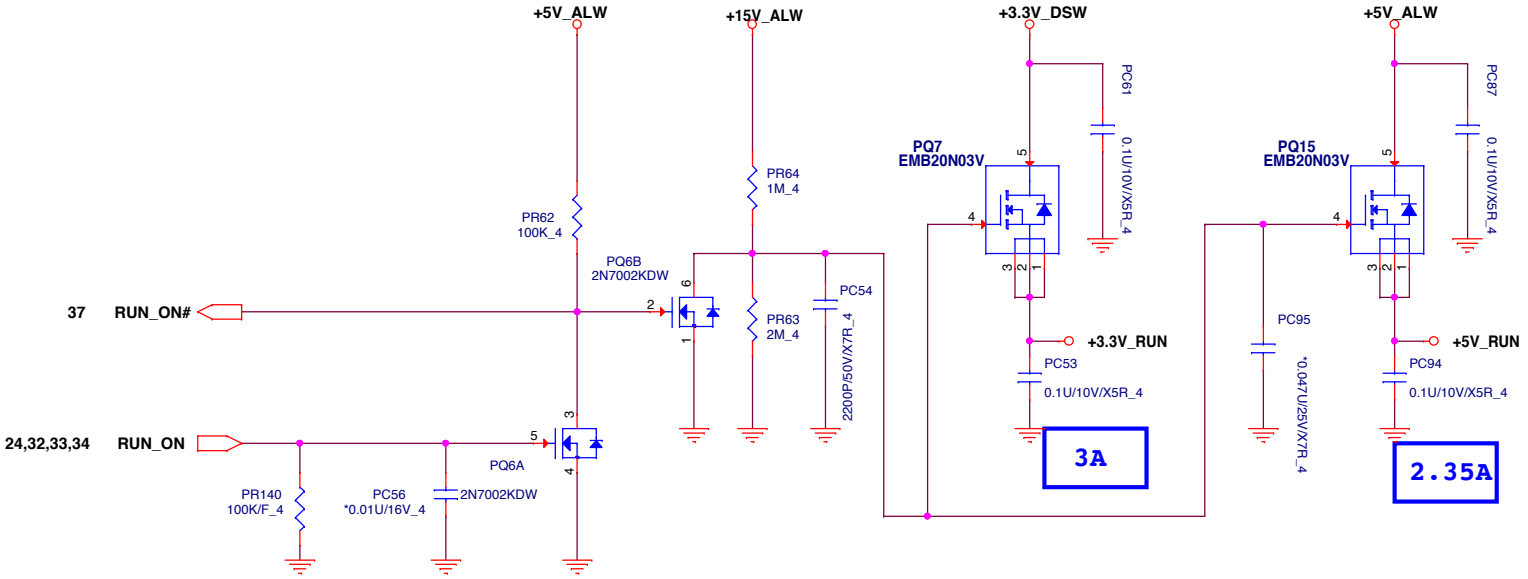
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE (TPS51622RSML)	1A
Date: Wednesday, February 27, 2013	Sheet 35 of 37	

14,17,20,22,23,31,32,33,37	+5V_ALW
12,31	+15V_ALW
4,5,6,7,8,12,14,28	+3.3V_DEEP_SUS
15,16,17,19,25,27,30,35,37	+5V_RUN
2,4,6,7,8,12,14,15,16,17,19,20,21,23,24,25,26,27,30,35,37	+3.3V_RUN
4,6,8,12,17,21,23,25,31,34	+3.3V_DSW
6,9,12,28,33,37	+1.05V_RUN



PROJECT : LZ5

Quanta Computer Inc.

Size	Document Number	Rev
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Date:	Sheet of	

DISCHARGE

14,17,20,22,23,31,32,33,36	+5V_ALW
15,16,17,19,25,27,30,35,36	+5V_RUN
2,4,6,7,8,12,14,15,16,17,19,20,21,23,24,25,26,27,30,35,36	+3.3V_RUN
12,17,21,34	+1.5V_RUN
6,9,12,28,33	+1.05V_RUN
14,32	+0.675V_DDR_VTT
4,5,6,7,8,12,14,28	+3.3V_DEEP_SUS
9,14,32	+V_VDDQ_VR
12,31,36	+15V_ALW

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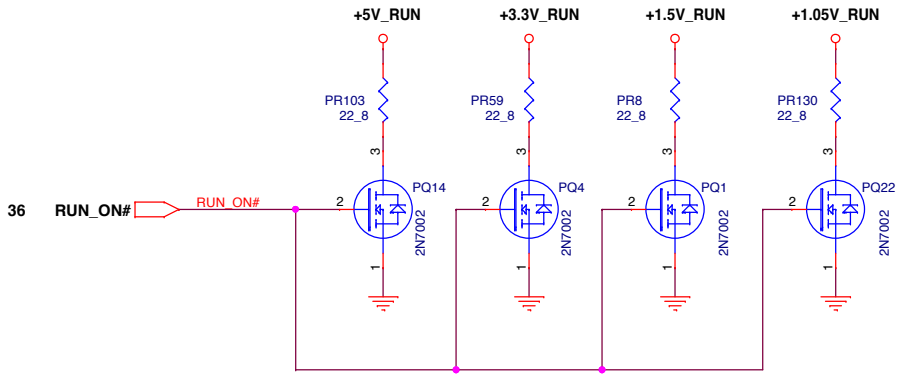

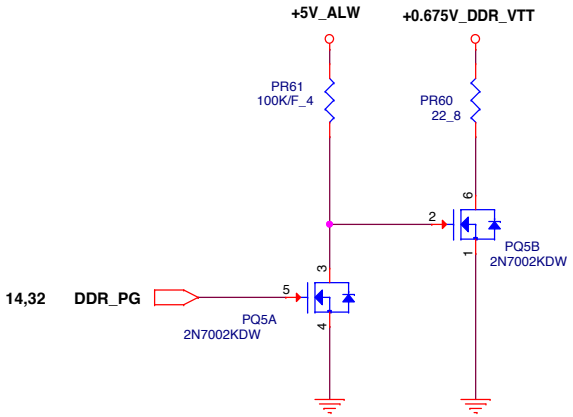

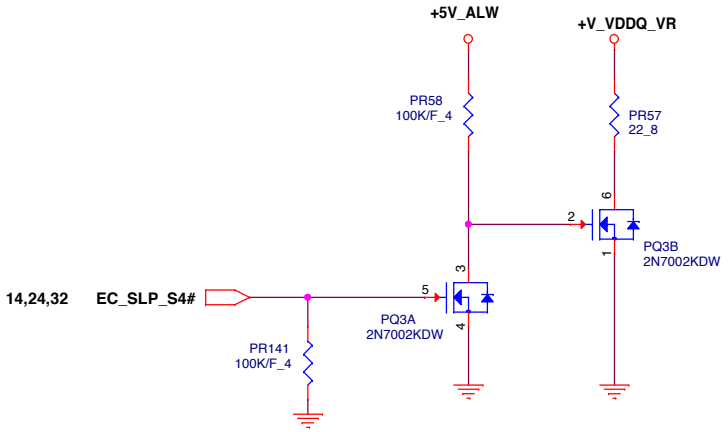

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