Compal Confidential

GOC30

GPU Board Schematic Document

NVIDIA N18S-G5, GDDR6 2G

2021-01-26
LS-K881P
REV：1.0

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Title: Cover Page		
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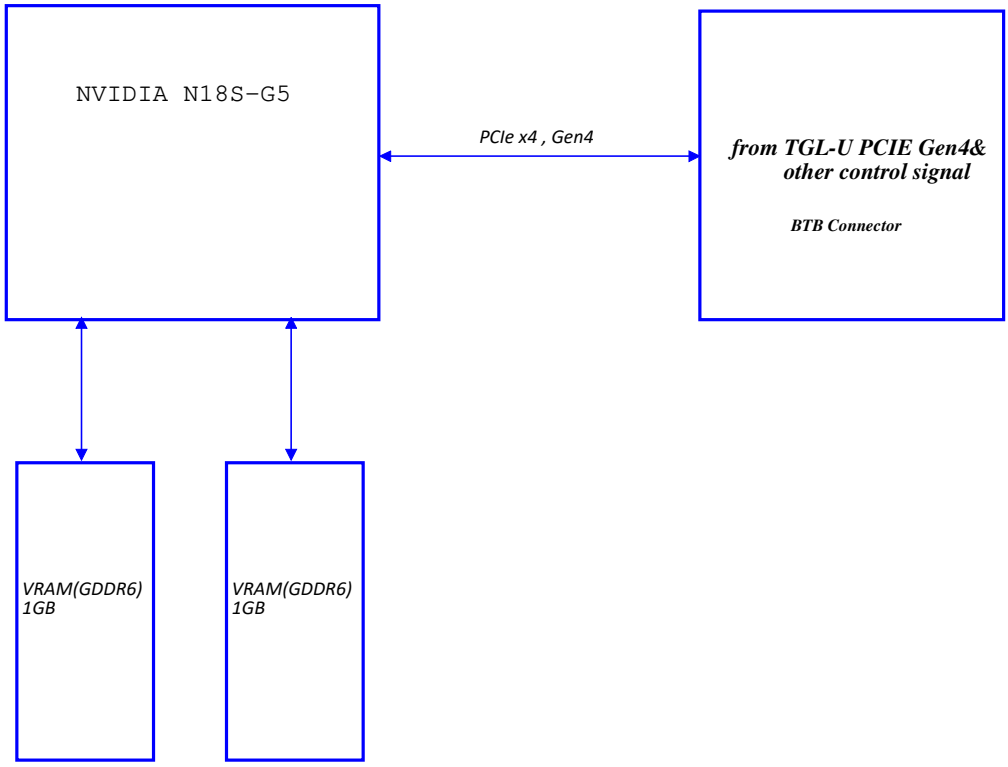

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		Size: LS-K881P
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BOM Structure Table

BOM Structure	BTO Item
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[illegible]	[illegible]
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[illegible]	[illegible]
[illegible]	[illegible]

SKU ID(Project) Table

SKU	A360-GOC30 ITL BOM Configure Table
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X7690438L01	[illegible]
455PC338L02 435PC338L02	[illegible]
X7690438L02	[illegible]
455PC338L03 435PC338L03	[illegible]
X7690438L03	[illegible]

PCB PN

ZZZ
PCB 31E LS-K881P
DA8001PD01S

GPU

UV1
SA0000DGW30
N18S-G5-A1
N18S_G5@

VRAM

Samsung

UG11 SA0000C6260
VRAM_S2G@
K4Z80325BC-HC14 2001

UG12 SA0000C6260
VRAM_S2G@
K4Z80325BC-HC14 2001

Micron

UG11 SA0000BND60
VRAM_M2G@
MT61K256M32JE-14:A 1940

UG12 SA0000BND60
VRAM_M2G@
MT61K256M32JE-14:A 1940

Hynix

UG11 SA0000DUW00
VRAM_H2G@
H56C8H24AIR-S2C

UG12 SA0000DUW00
VRAM_H2G@
H56C8H24AIR-S2C

VRAM X76

ZZZ
X76 VRAM SAM 2G
X7690438L02
X76_S2G@

ZZZ
X76 VRAM MIC 2G
X7690438L01
X76_M2G@

ZZZ
X76 VRAM HYX 2G
X7690438L03
X76_H2G@

X4E

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[Power Map]

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6.4.2 GC6 3.0 Entry/Exit Timing

The following timing diagram describes the GC6 3.0 entry and exit sequence and timing requirements.

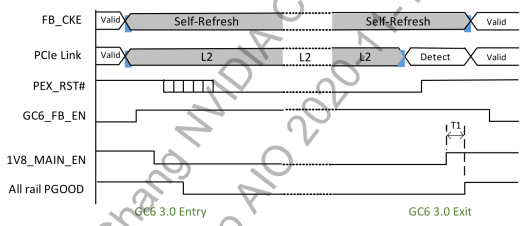


Figure 6.19 GC6 3.0 Entry/Exit Timing Sequence

Table 6.3 GC6 3.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

6.2.3.3 GC OFF 1.0 GPU Power On/Off Timing

GC OFF Entry/Exit and delay timing constraints are given in Figure 6.9 and Table 6.1. All delays should be as short as possible for maximum power saving while meeting the timing constraints.

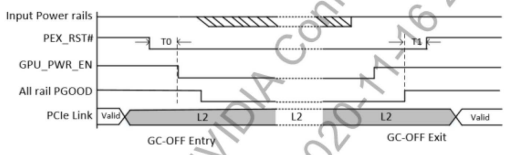


Figure 6.9 GC OFF1.0 Entry/Exit Timing Diagram

Table 6.1 GC OFF1.0 Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

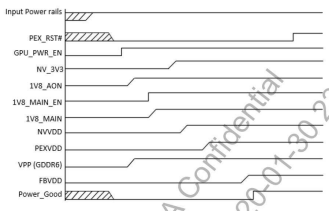


Figure 5.6 Power-Up Sequence

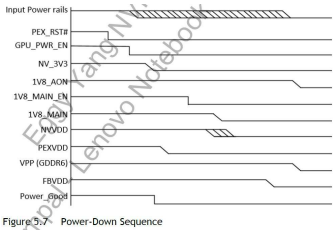
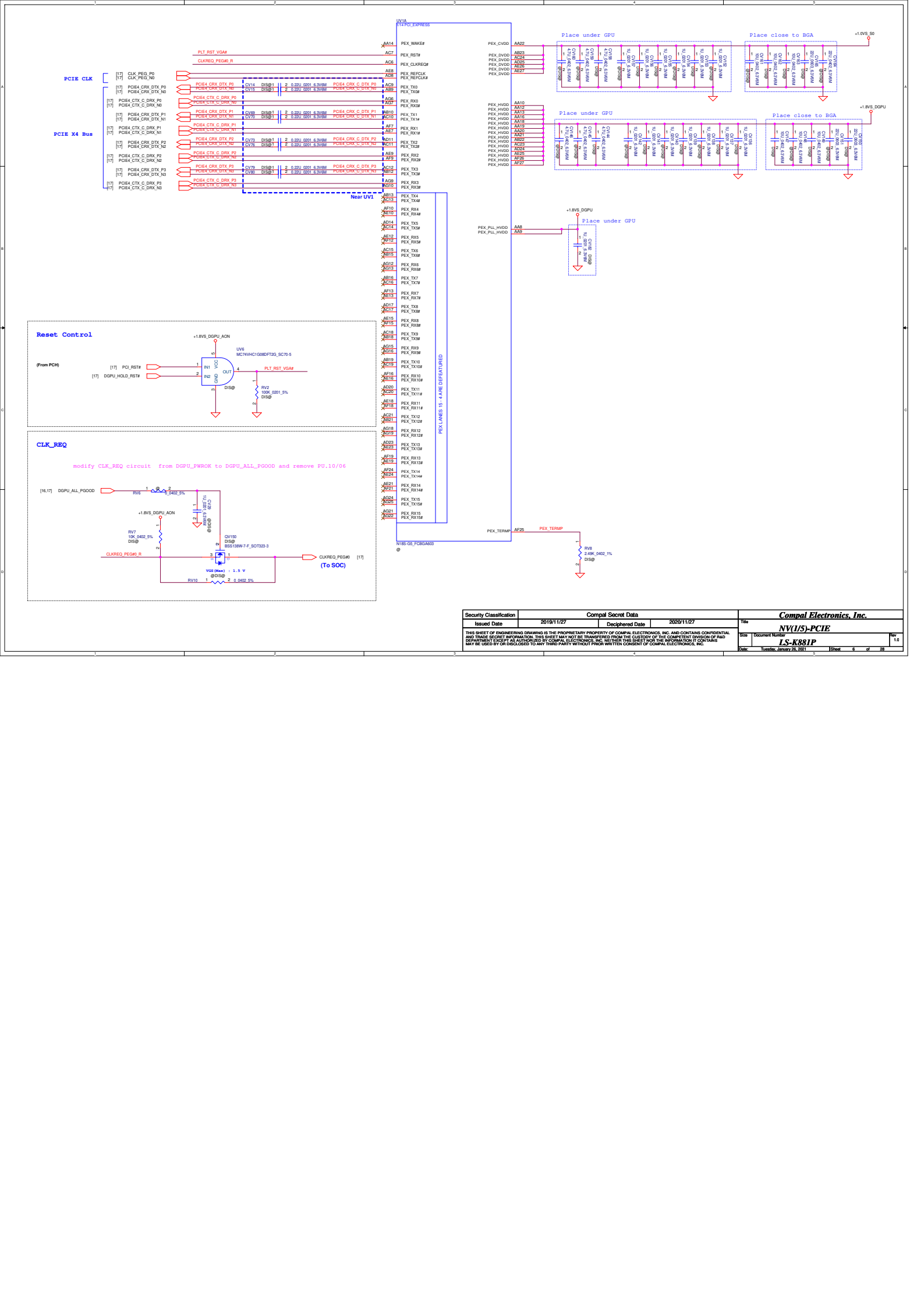


Figure 5.7 Power-Down Sequence



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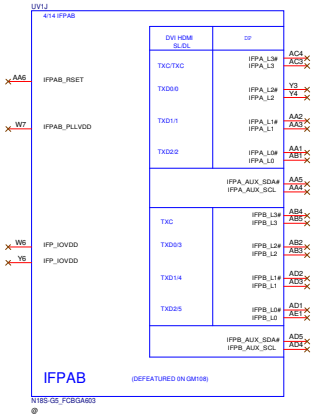

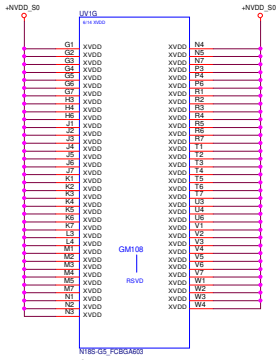

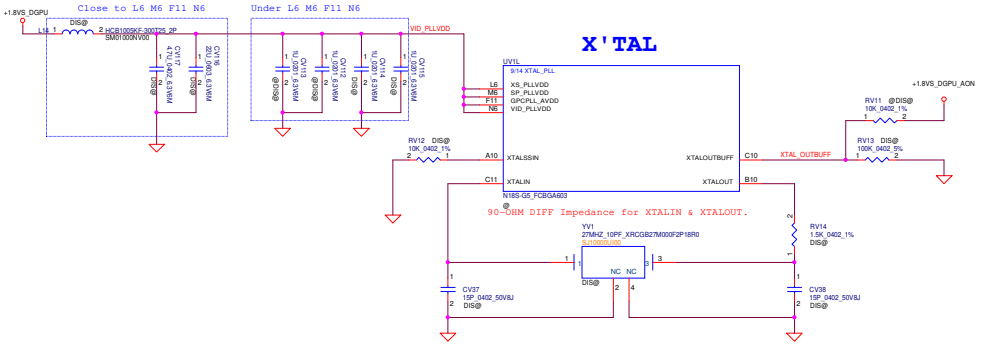

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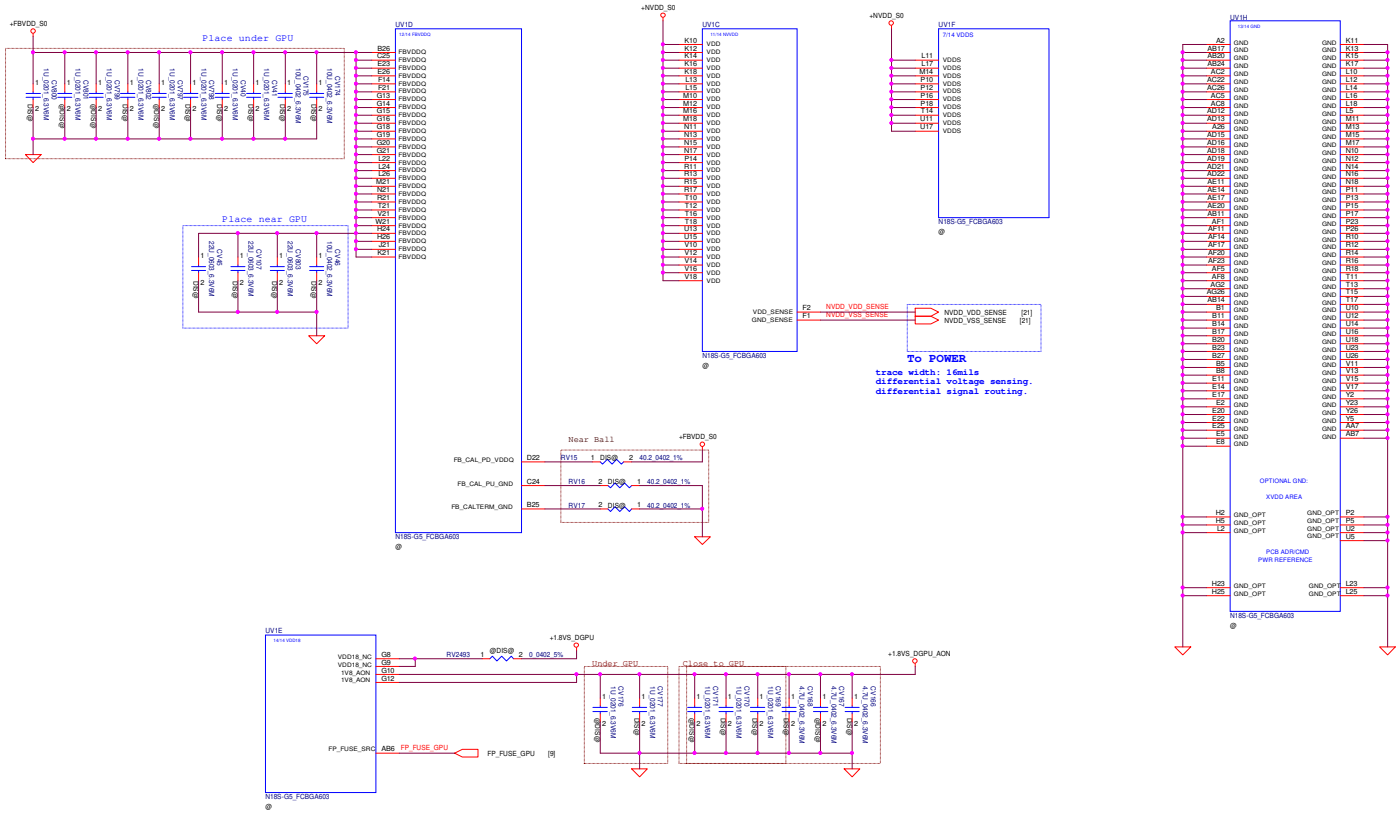

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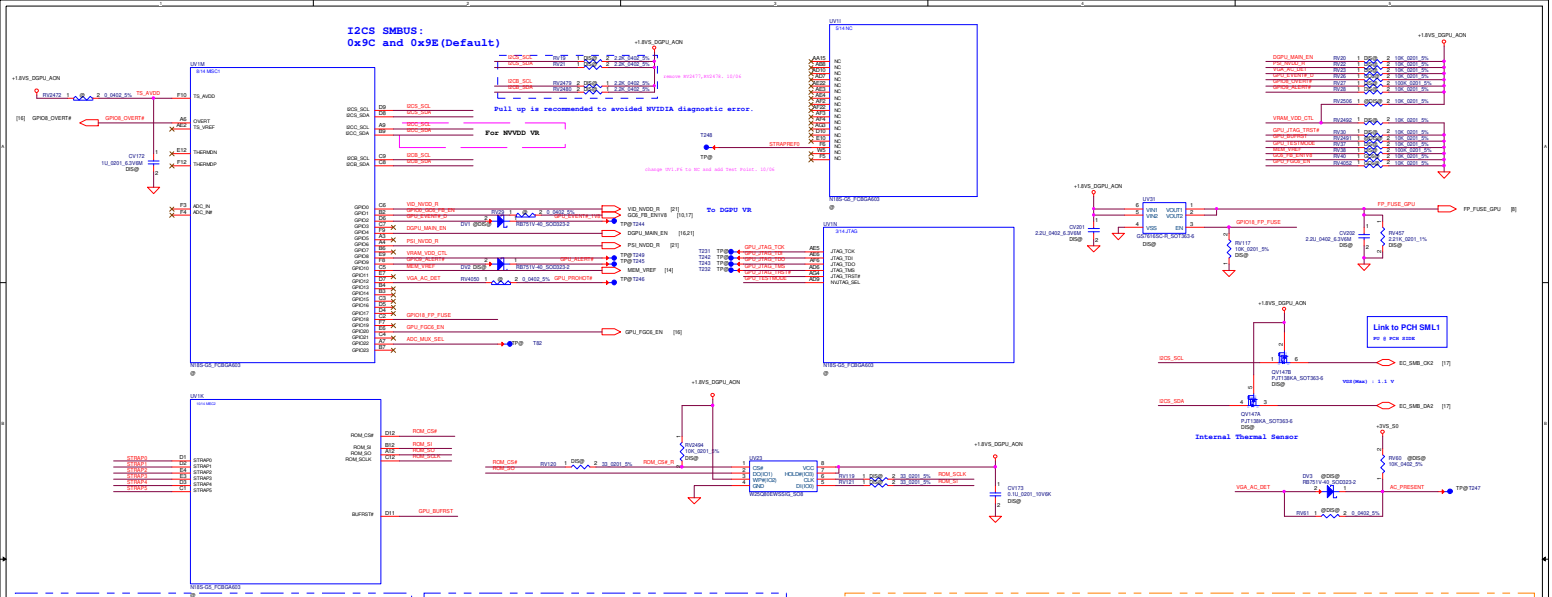


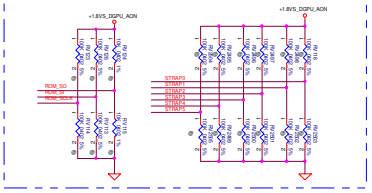
N18S -G5 Strap

ROM_SO	ROM_SI	ROM_SCLK	STRAP3	STRAP4	STRAP5
RV115 DIS@ 10K_0402_5%	RV113 DIS@ 100K_0402_5%	RV114 DIS@ 100K_0402_5%	RV2500 DIS@ 100K_0402_5%	RV2499 DIS@ 100K_0402_5%	RV2505 DIS@ 100K_0402_5%

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

STRAP



N18S -G5 VRAM Strap

RAM_CFG	STRAP2	STRAP1	STRAP0
0x1 (LLH) M2G	RV2501 100K_0402_5% VRAM_M2G@	RV2502 100K_0402_5% VRAM_M2G@	RV116 100K_0402_5% VRAM_M2G@
0x0 (LLL) S2G	RV2501 100K_0402_5% VRAM_S2G@	RV2502 100K_0402_5% VRAM_S2G@	RV2503 100K_0402_5% VRAM_S2G@
0x2 (LHL) H2G	RV2501 100K_0402_5% VRAM_H2G@	RV2498 100K_0402_5% VRAM_H2G@	RV2503 100K_0402_5% VRAM_H2G@

Table 12.3 RAMCFG

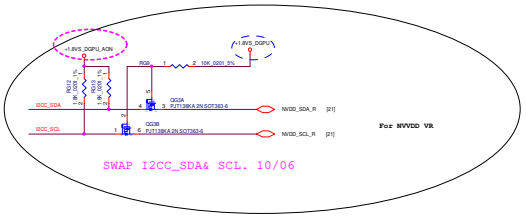
Strap Pins see Note			RAMCFG setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	M	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 12. N18S-G5-B, N18S-G5 and N18S-LP GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production ready
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[3]	Full	Production ready
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production ready

Notes:

1. For N18S-G5-B, N18S-G5 and N18S-LP, the maximum allowable memory case temperature is 95 °C.
2. Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
3. Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.



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Title: NV(4/5)-GPIO/Strap

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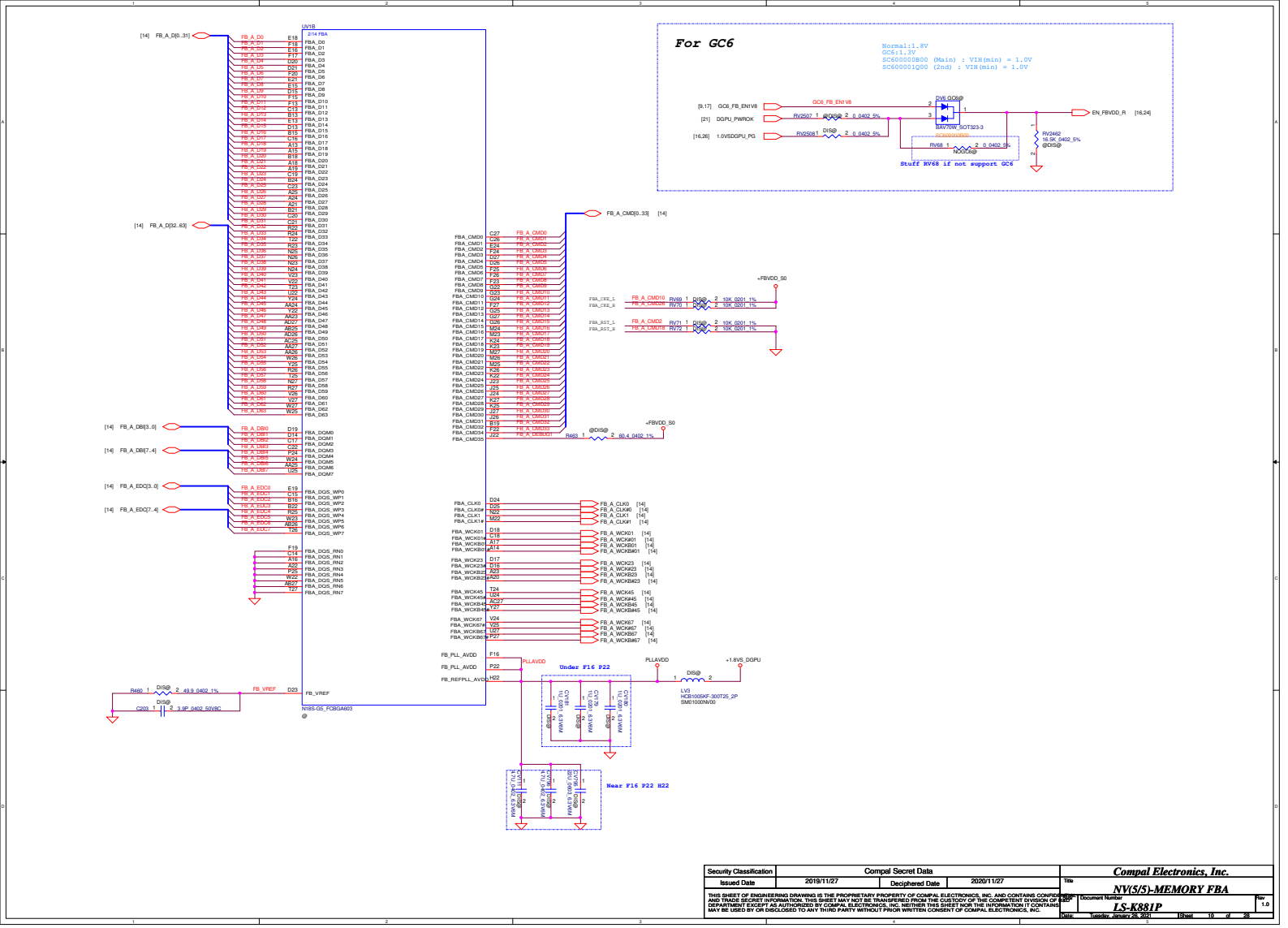

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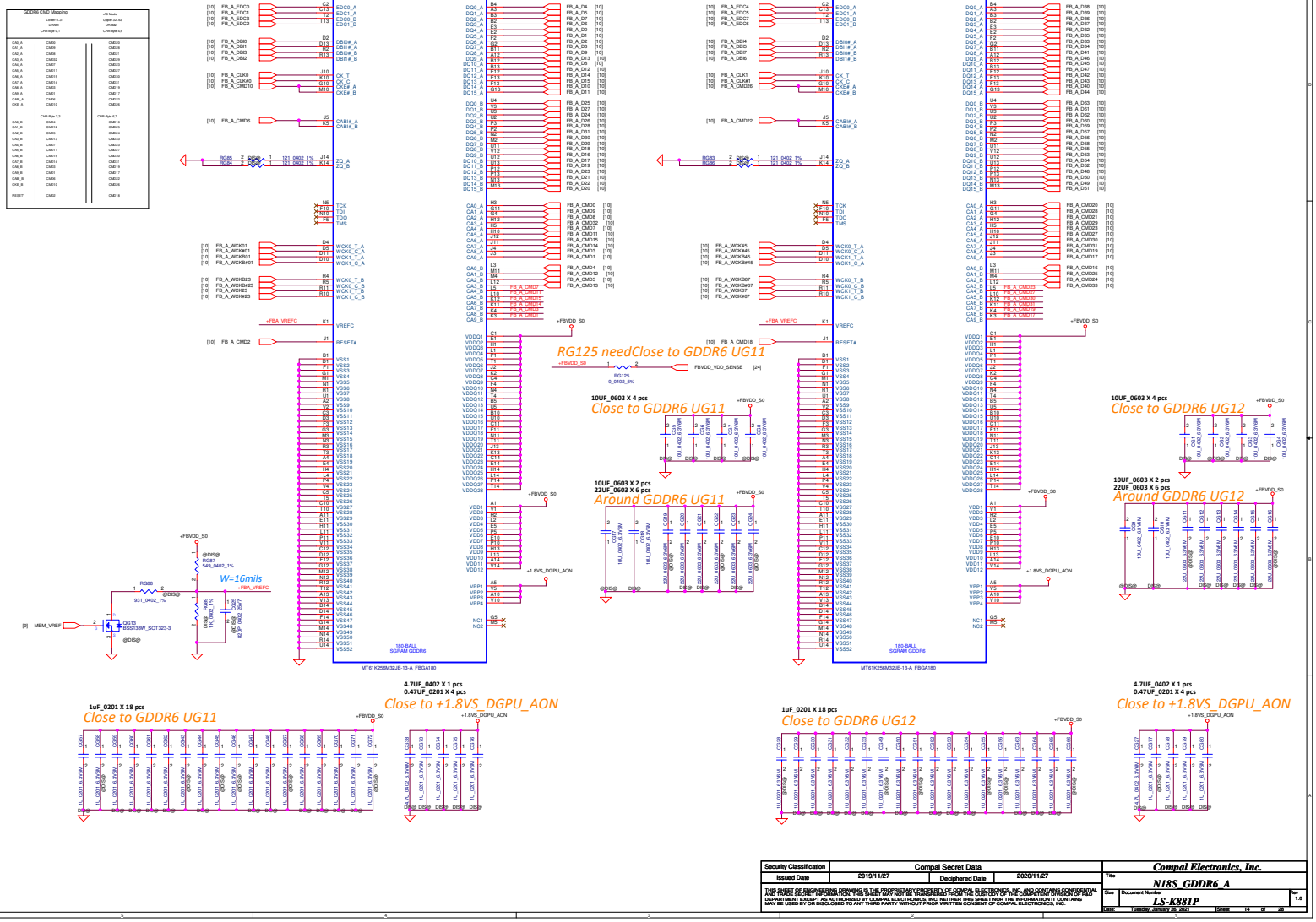
VRAM A



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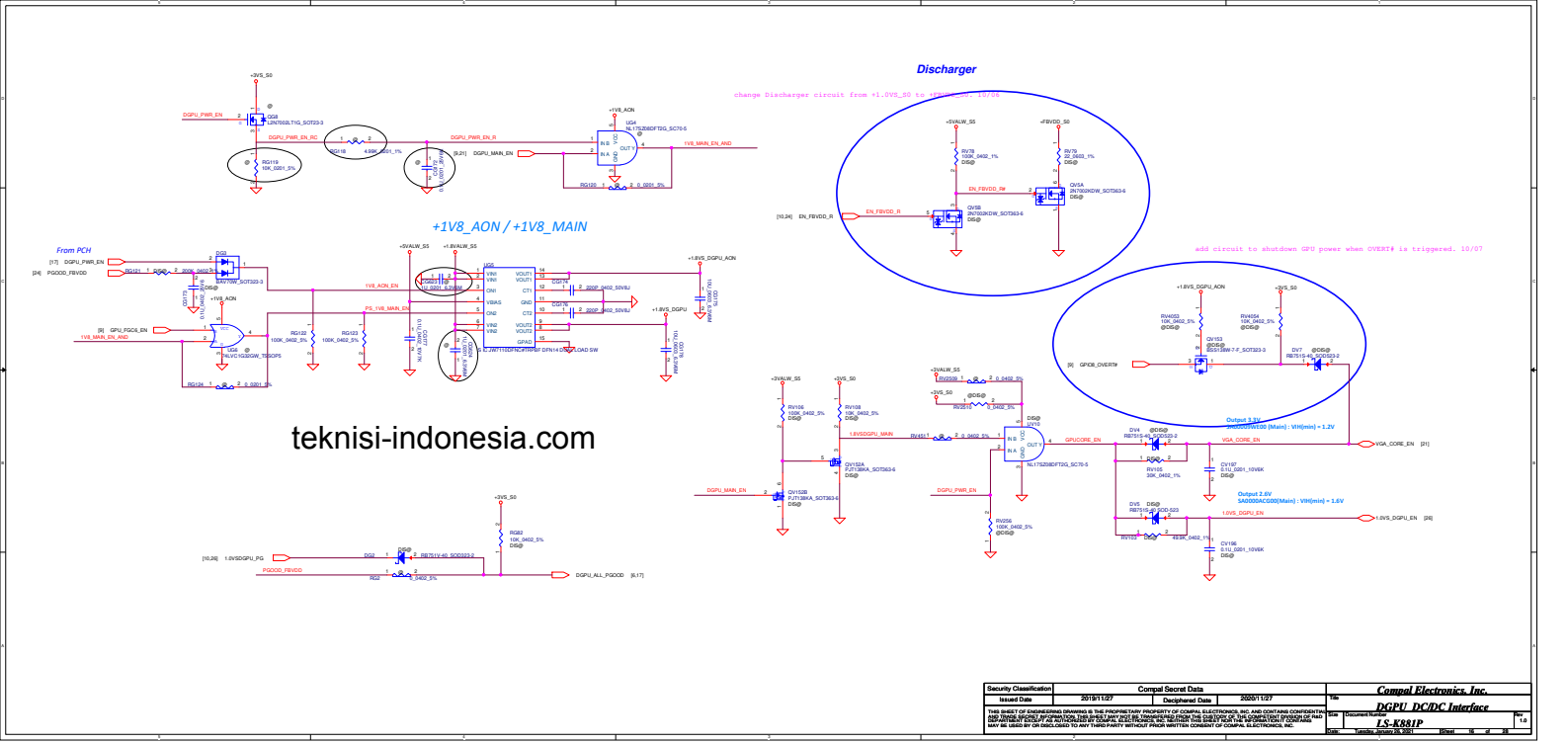

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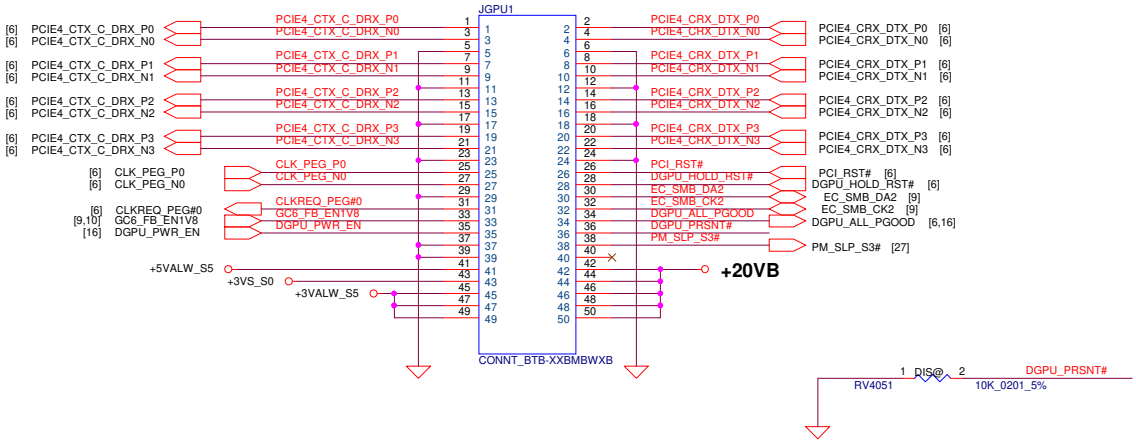

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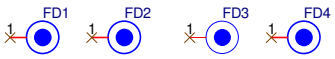
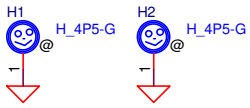
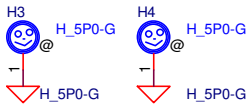
Fiducial Mark



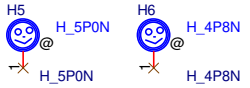
PCB Screw Hole



BTB Screw Hole



GPU Hole



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ET

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5	all			
6	008			
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11	016			
12	009			
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SDV

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16	006			

SIT

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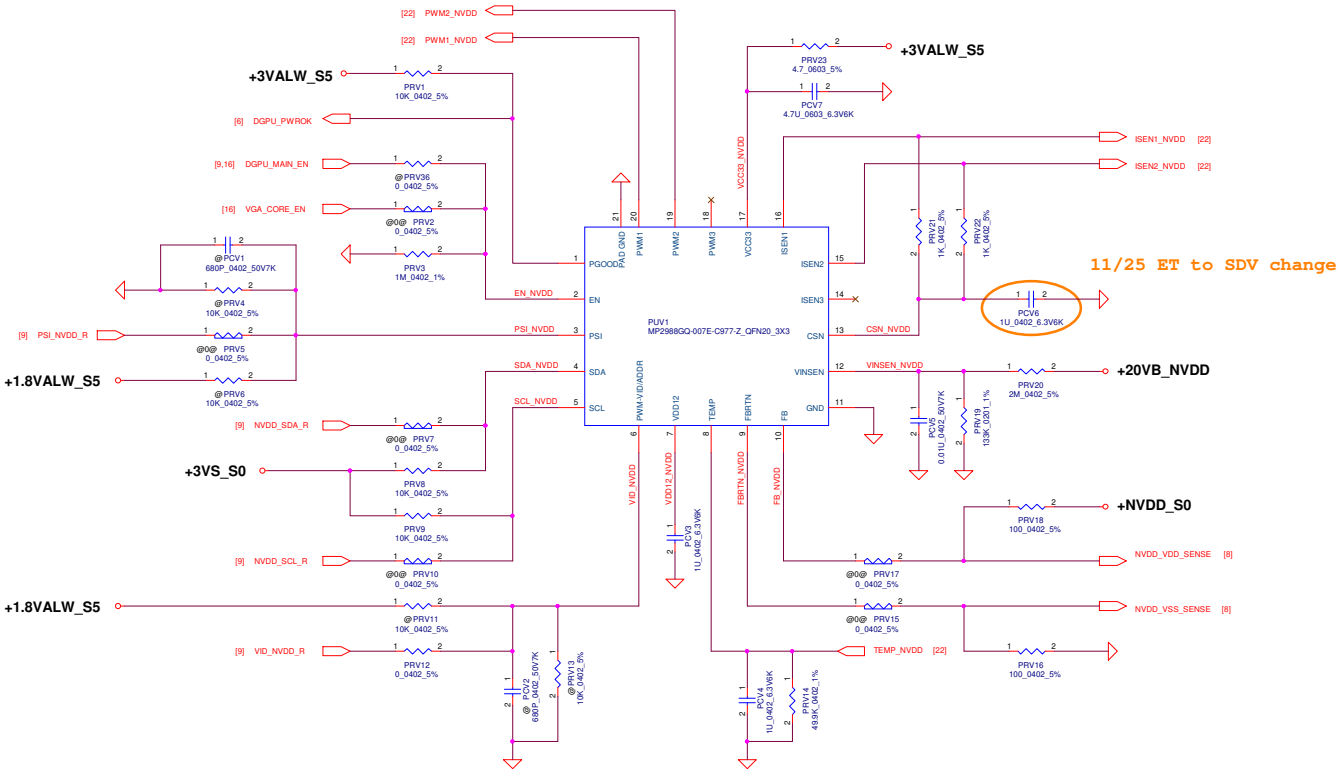
Controller --- MP2988



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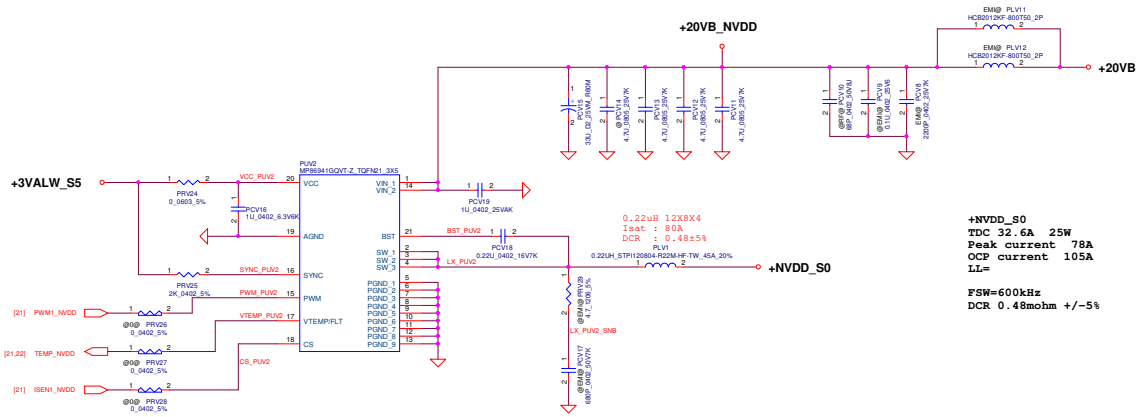

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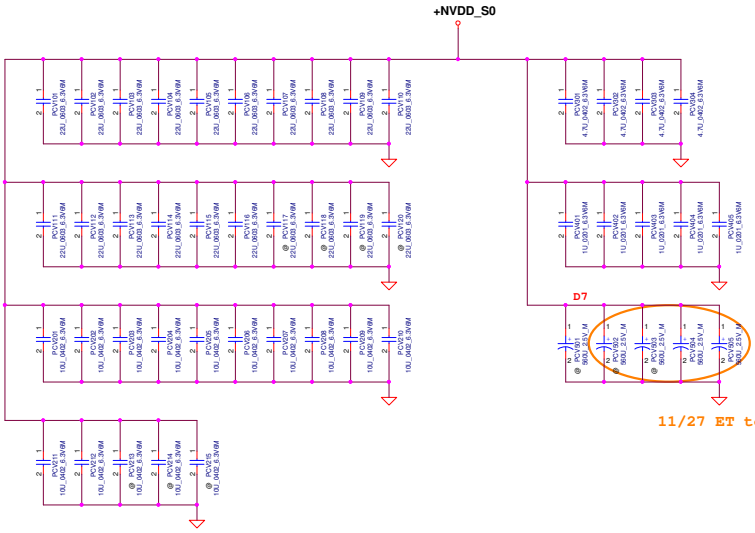

N18S-G5
+NVVDD
560uF X 5 (+1)
22uF_0603 X 16 (+4)
10uF_0402X 12(+3)
4.7uF_0402*4
1uF_0201 X 5

Place near GPU

11/27 ET to SDV change

NVDD (ET)

22uF_0603 16 pcs
10uF_0402 12 pcs
4.7uF_0402 4 pcs
1uF_0201 5 pcs
560uF_10m 2 pcs

Table 4. NVDD Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
NVDD Supply Net						
GB2D-64 /GB2C-64 GB2E-64	1 µF[1]	X6S	0402 or 0201W	5	5	Under GPU
	10 µF	X6S	0603	12	12	Under GPU
	4.7 µF	X6S	0805	0	4	Near GPU
	10 µF	X7R	0805	0	11	Near GPU
	22 µF	X6S	0805	10	4	Near GPU
	330 µF	POS	7343	2	2	Near GPU

Note:
[1]Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

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Title: PWR-VGA DECOUPLING
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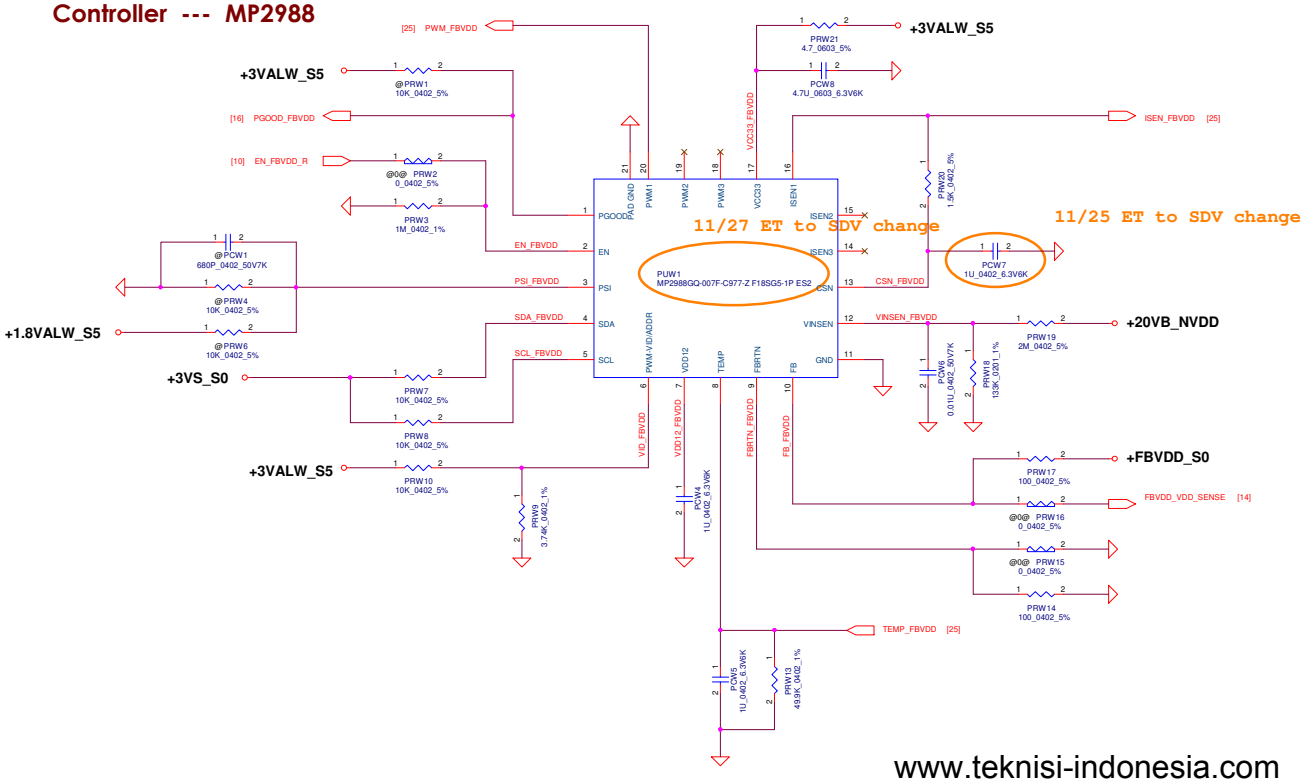
Controller --- MP2988



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Size: Custom	Document Number: <Doc>		Rev: 0.3
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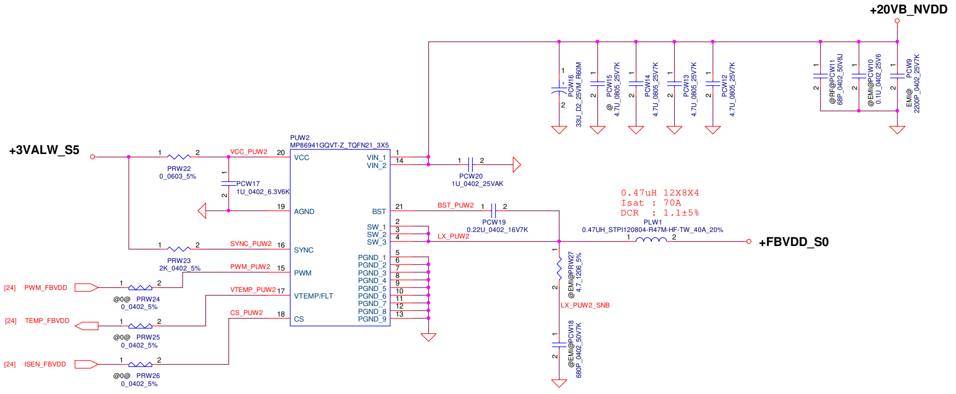
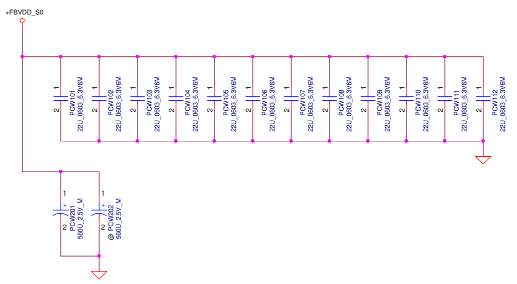


+FBVDD_S0
TDC 11A
Peak current 11A
OCP current 22A
LL=

FSW=600kHz
DCR 1.1mohm +/-5%



Place near GPU

N18S-G5
+FBVDD
560uF X 2
22uF_0603 X 10 (+2)

FBVDD (ET)

22uF_0603 12 pcs
560uF_10m 1 pcs

Table 5. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2D-64 /GB2C-64 GB2E-64	1 µF[1]	X6S	0402 or 0201W	8	8	Under GPU
	10 µF	X6S	0603	2	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603	3	3	Near GPU

Note:
[1]Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2019/11/18	Deciphered Date	2019/11/18	Title: PWR_VCCIN_Driver MOS

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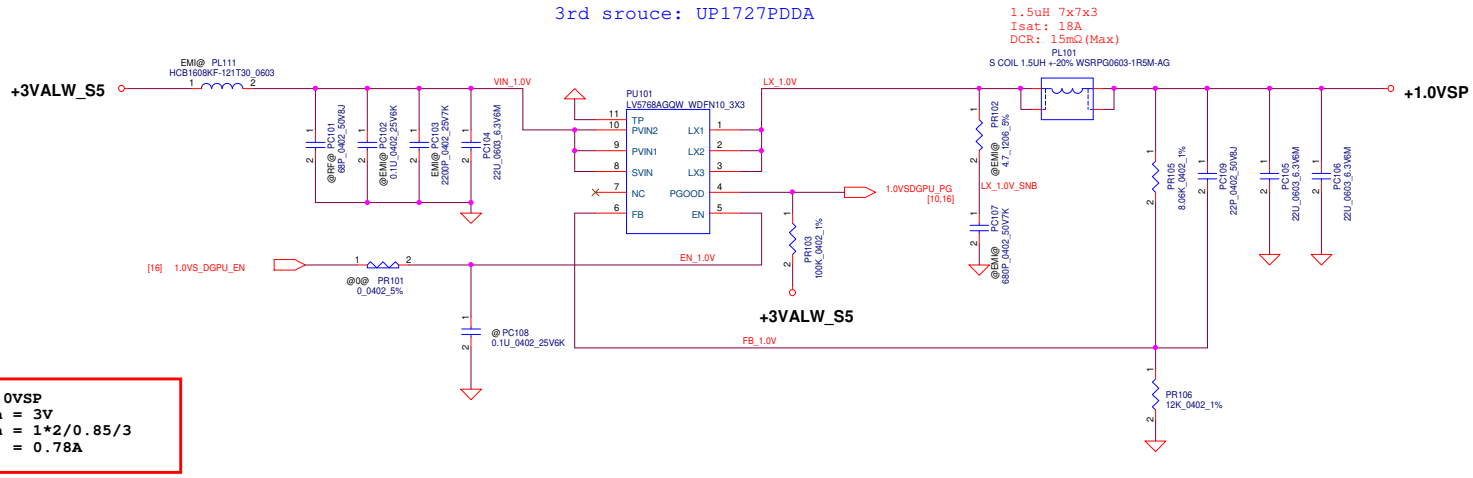
1st source: LV5768A
2nd srouce: GS7302ADTD-R
3rd srouce: UP1727PDDA



+1.0VSP
Vin = 3V
Iin = 1*2/0.85/3
= 0.78A

Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(8K/12K)]
= 1.0V

soldering short

+1.0VS_S0
Imax=1.4A, Ipeak=2A; Fsw=1MHz
Current Limit=4A
Iin_ripple=0.27A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.48A
LIR=Delta IL/Ipeak=0.24
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+DeltaV)^2-Vout^2]
=117uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.03uF

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2017/10/19

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Title: +1.0VSP

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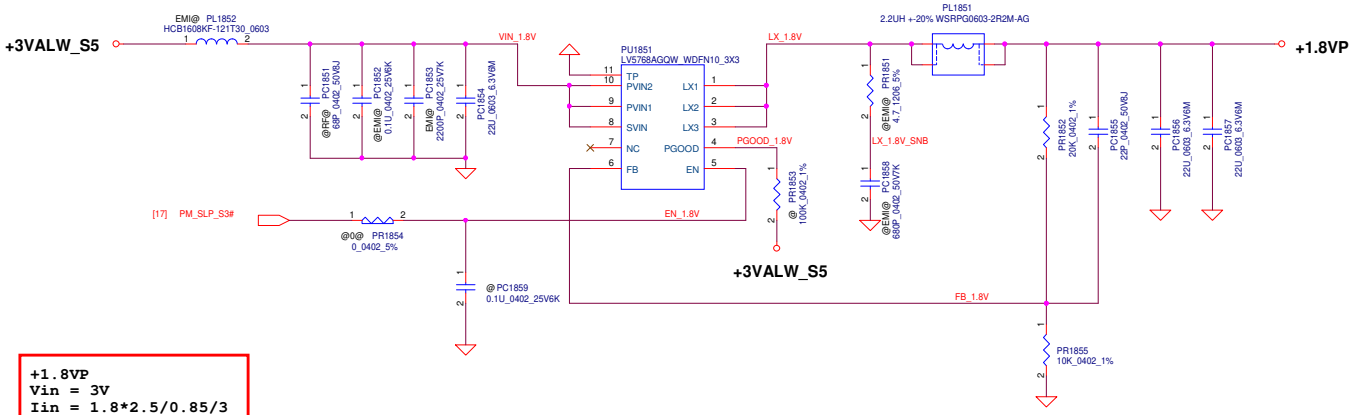
1st source: LV5768A
2nd srouce: GS7302ADTD-R
3rd srouce: UP1727PDDA

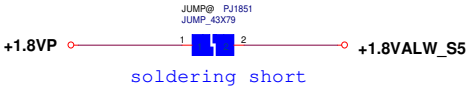
7x7x3
Isat: 18A
DCR: 20mΩ(Max)



+1.8VP
Vin = 3V
Iin = 1.8*2.5/0.85/3
= 1.77A

Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(20K/10K)]
= 1.8V

+1.8VP
Imax=1.75A, Ipeak=2.5A; Fsw=1MHz
Current Limit=4A
Iin_ripple=0.84A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.524A
LIR=Delta IL/Ipeak=0.209
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=68.03uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.81uF



soldering short

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2017/10/19

Compal Electronics, Inc.

Title: +1.8VP

Size | Document Number | Rev 0.1

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NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
Kickoff to ET	2020/08/28	P.027	PU1851 EN Pin Change from 3V5V_PG to PM_SLP_S3#	HW sequence request
		P.024	PUW1 PSI Pin Delete signal PSI_FBVDD_R Delete location PRW5	N18S-G5 GB2E-64 without FBVDD PSI Pin
		P.026, P.027	PR101, PR1854 Change from short-pad to 0ohm	
		P.026	PR104 Delete location PR104	Circuit no need
	2020/09/01	P.022, P.025	PCV19, PCV28, PCW20 Change from 1U 25V K X5R 0805 to 1U 25V K X6S 0402	
		P.024	PQW1, PQW2 Change from SB00000PU00 to SB00000PV00	Reduce layout space
		P.023	PCV506 Delete location	
		P.025	PCW203, PCW204 Delete location	
	2020/09/14	P.021	PUV1 Change from SA0000CGG00 to SA0000E2E10	For N18S-G5 NVDD Digital IC
		P.024	PUW1 Change from SA0000CGG00 to SA0000E2F10	For N18S-G5 FBVDD Digital IC
	2020/09/16	P.023	PCV501, PCV504, PCV505 Change to unpop	FAE suggest NVDD/FBVDD Bulk cap quantity
		P.025	PCW202 Change to unpop	
	2020/09/21	P.021	PUV1 Pin4, 5 Pull high change from +1.8VALW_S5 to +3.3VALW_S5	FAE suggest circuit
		P.022	PCV14, PCV23 Change to unpop	
		P.024	PUW1 Pin4, 5 Pull high change from +1.8VALW_S5 to +3.3VALW_S5	
			PCW2, PCW3 Change to unpop	
		P.025	PCW15 Change to unpop	
	2020/09/22	P.021	PUV1 Pin4, 5 Pull high change from +3VALW_S5 to +3VS_S0	HW sequence request
		P.024	PUW1 Pin4, 5 Pull high change from +3VALW_S5 to +3VS_S0	
	2020/09/29	P.024	PRW1 Change to unpop	Pull high +3VS_S0 on HW side
	2020/10/06	P.024	PRW11, PQW1A/B, PCW2, PCW3, PRW12 Delete location	DDR6 : FBVDD 1.2V only
ET to SDV	2020/11/25	P.021	PCV6 Change to pop	Fix NVDD Vout issue
		P.024	PCW7 Change to pop	Fix NVDD Vout issue
	2020/11/27	P.021	PUW1 Change from SA0000E2F10 to SA0000E2F20	FBVDD IC update FW
			NVDD output Cap_560uF Change location from PCV502, PCV503 to PCV504, PCV505	
SDV to SIT	2021/01/07	P.021, P.022, P.024, P.025, P.026, P.027	PRV2, PRV5, PRV7, PRV10, PRV15, PRV17, PRV26, PRV27, PRV28, PRV32, PRV33, PRV34, PRW2, PRW15, PRW16, PRW24, PRW25, PRW26, PR101, PR1854 Change from 0ohm to short pad	
SIT to SVT	2020/7/28			

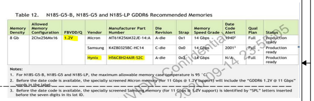

Table 12. N18S-G5-B, N18S-G5 and N18S-LP GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production ready
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[3]	Full	Production ready
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production ready

Notes:
1. For N18S-G5-B, N18S-G5 and N18S-LP, the maximum allowable memory case temperature is 95 °C.
2. Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
3. Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.