MS-AA711 Ver: 2.1

CPU:

INTEL - Ivy bridge LGA1155

System Chipset:

INTEL-Cougar Point (H61)

OnBoard Chipset:

HD Audio Codec:ALC887

LAN:Realtek RTL8111E

SIO:Nuvoton NCT6681D

USB3.0:ASMedia ASM1042

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:NCP6131 3 + 1 Phase (65W)

Other:

SATA(SATA2-300MB/s) *2

USB2.0 *4

USB3.0 *2

HDMI OUT*1

HDMI IN*1

Card reader*1

COM Port*2

MICRO-STAR INT'L CO.,LTD

MS-AA711

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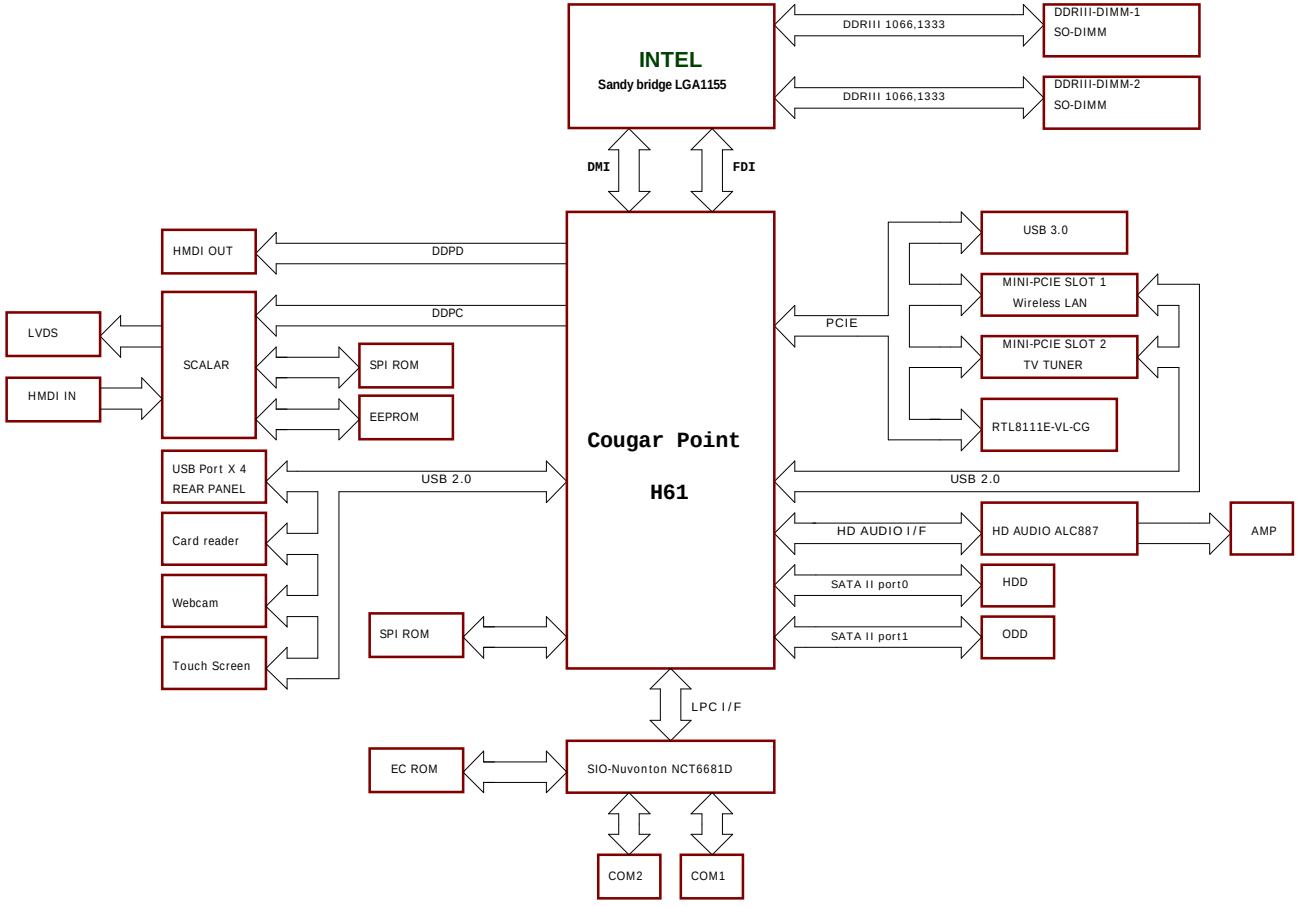
MS-AA711

Ver: 2.1



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	MS-AA711	
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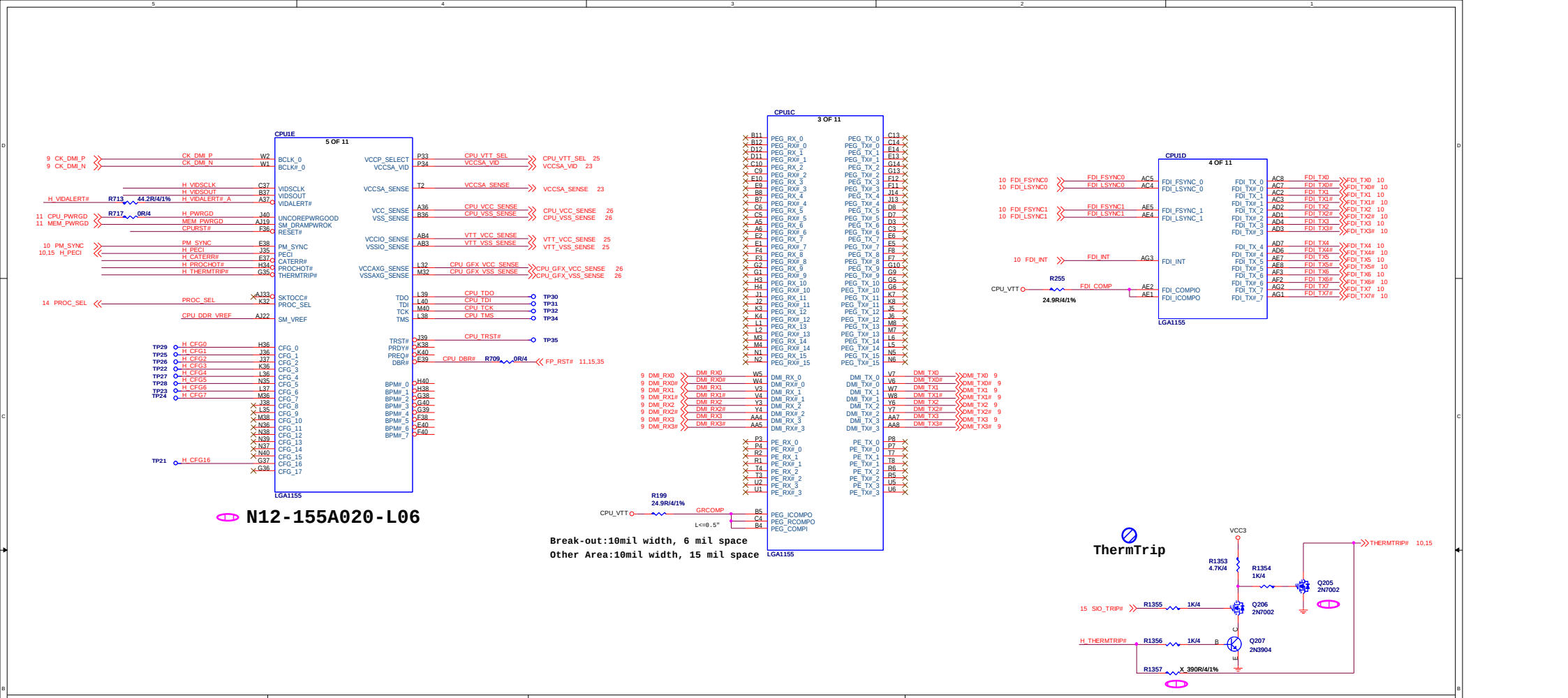

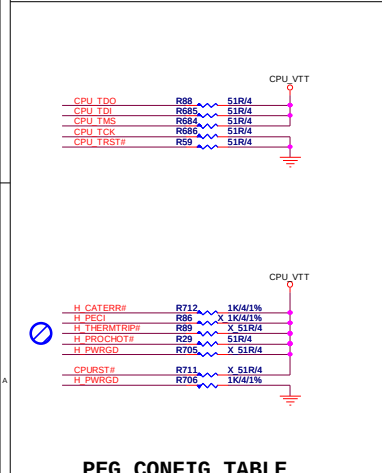

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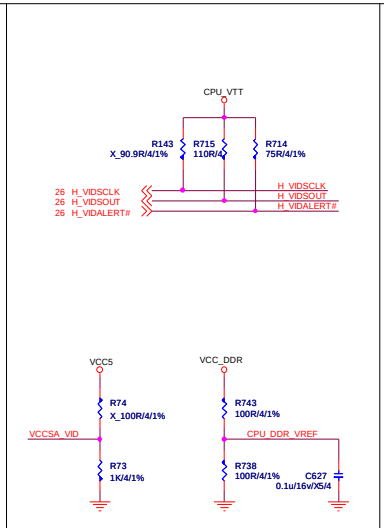
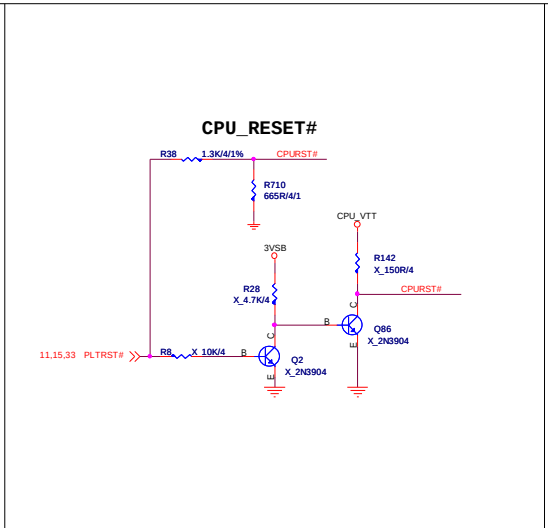
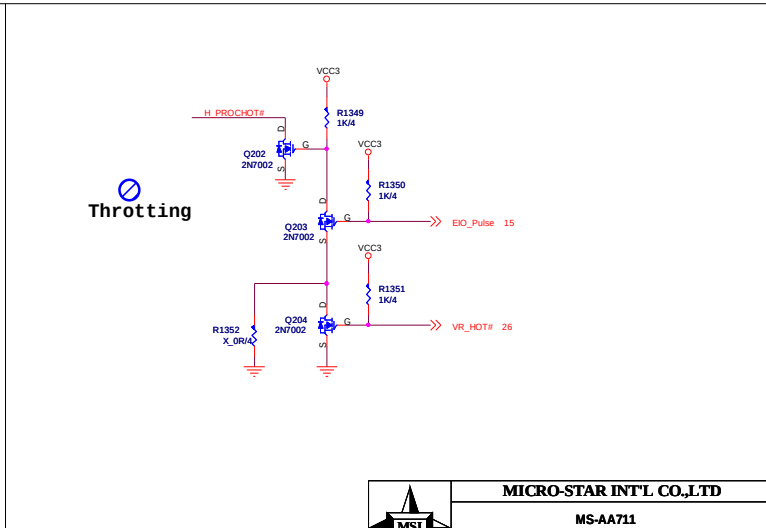
1	1	0	2 X 8







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MS-AA711		
Size: C	Document Description: CPU-CNTL/CLK/MISC	Rev: 2.1
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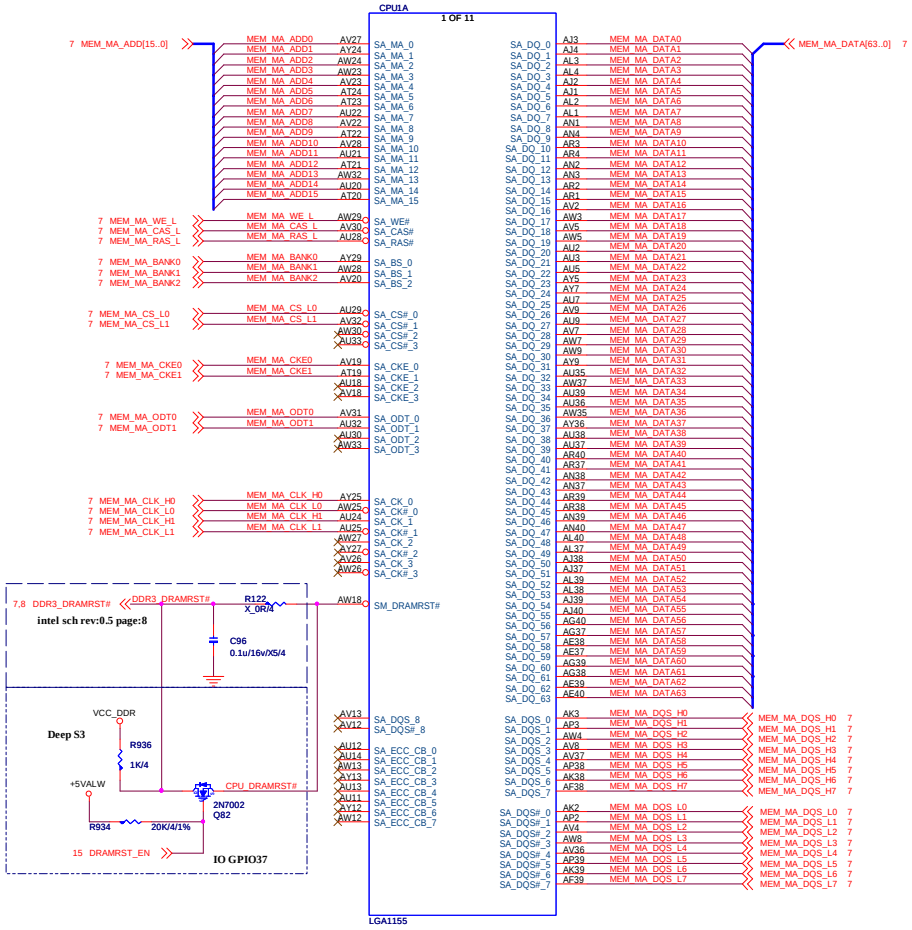

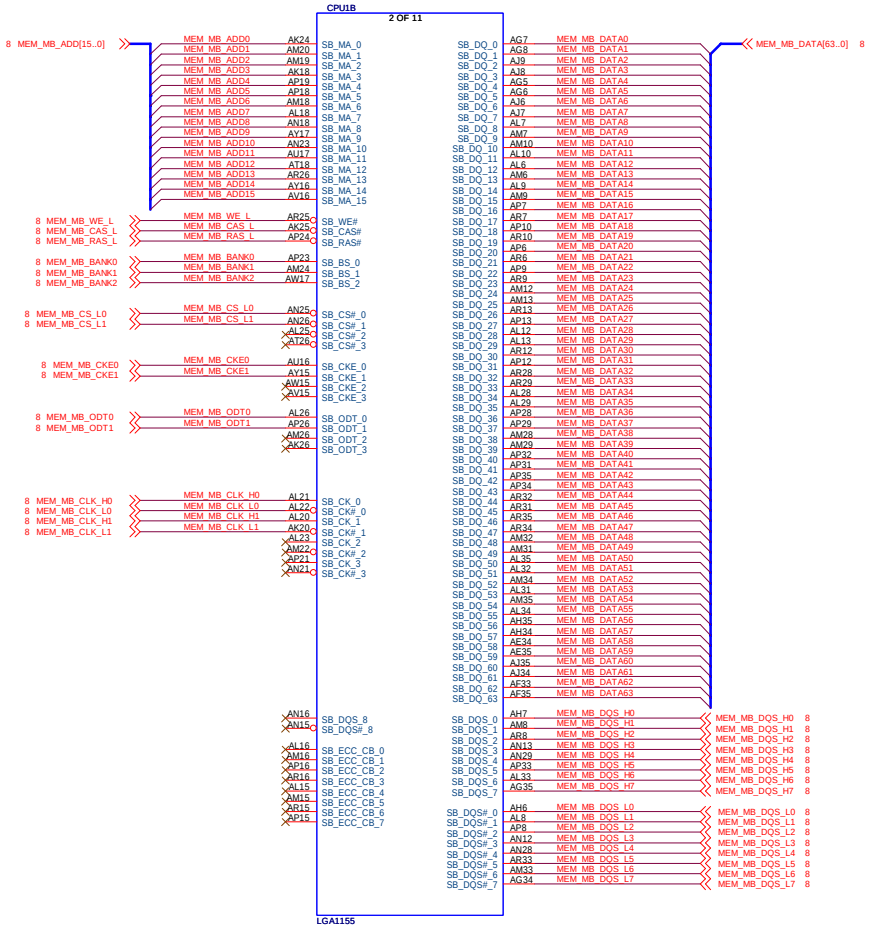

N12-155A020-L06

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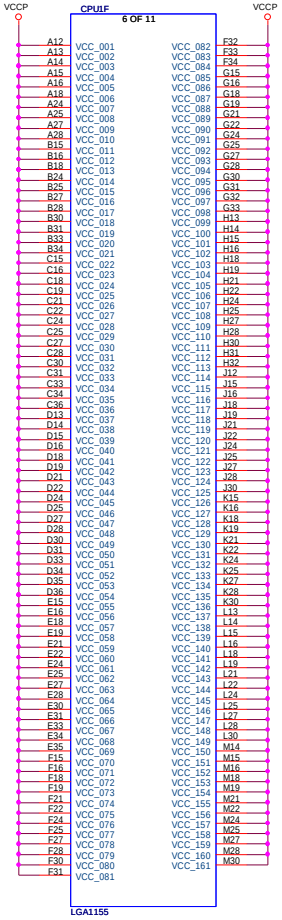

N12-155A020-L06

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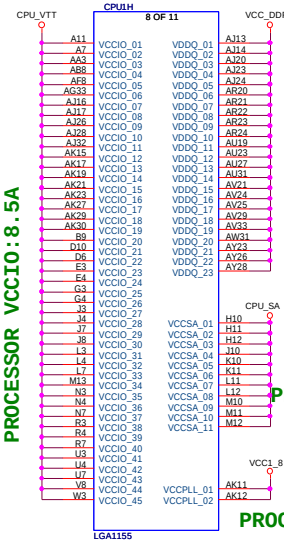
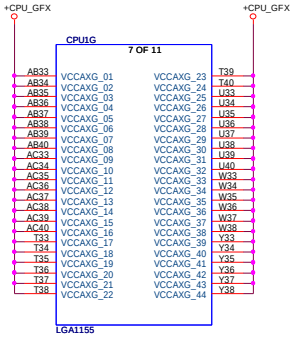
PROCESSOR VCCIO:8.5A

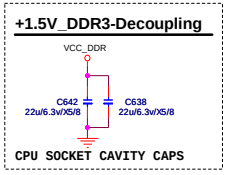


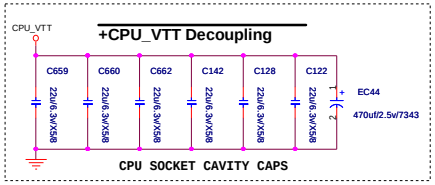
PROCESSOR VCCSA:8.8A

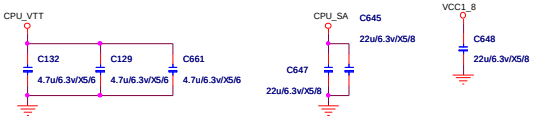
PROCESSOR VCCPLL:1.5A

PROCESSOR VAXG:35A









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	MS-AA711	
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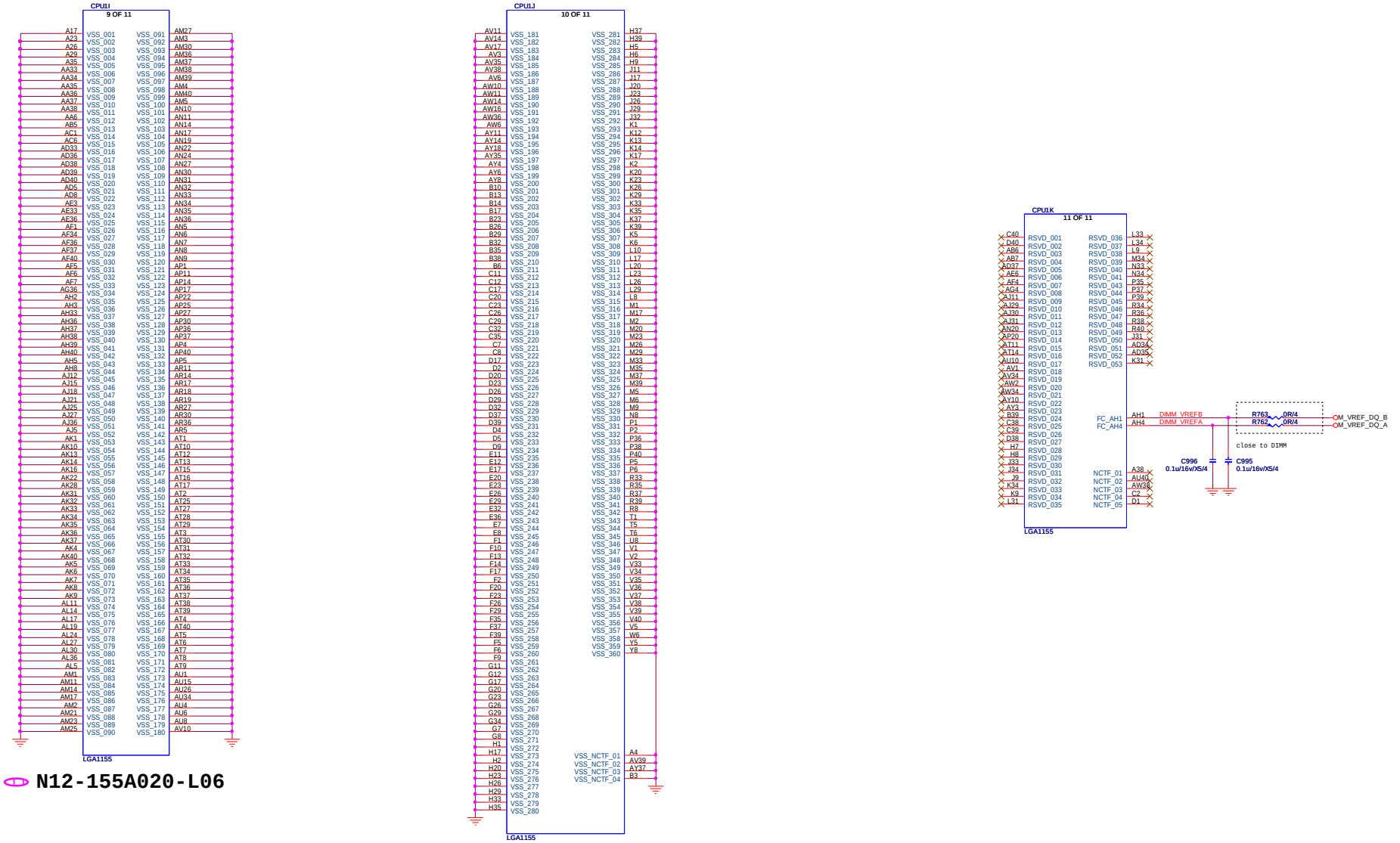

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MS-AA711		
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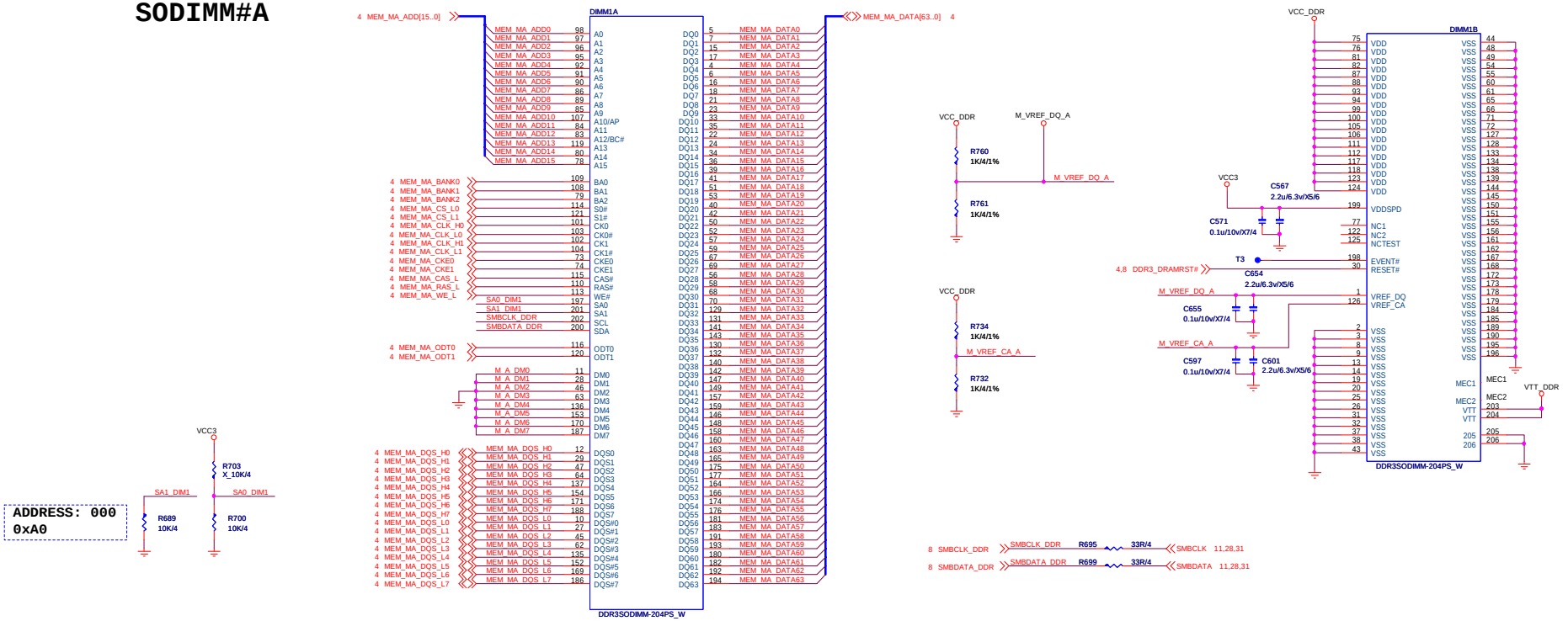
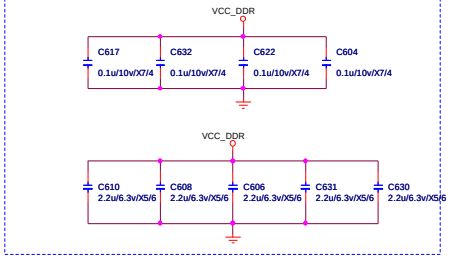
SODIMM#A



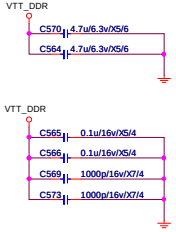
N13-2040790-CK3
H=5.2mm

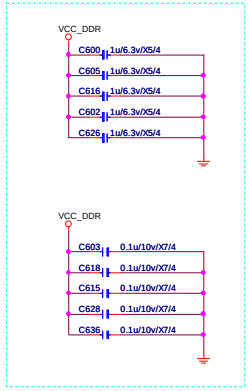
N13-2040800-CK3
H=9.2mm

Layout note: Place capacitors between and near DDR connector if possible.

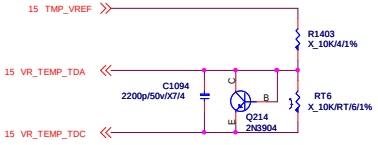


CHANNEL A V_SM_VTT DECOULPING CAPS





Temp. Sensor



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MS-AA711	
Size: C	Document Description: DDR III SODIMM 1
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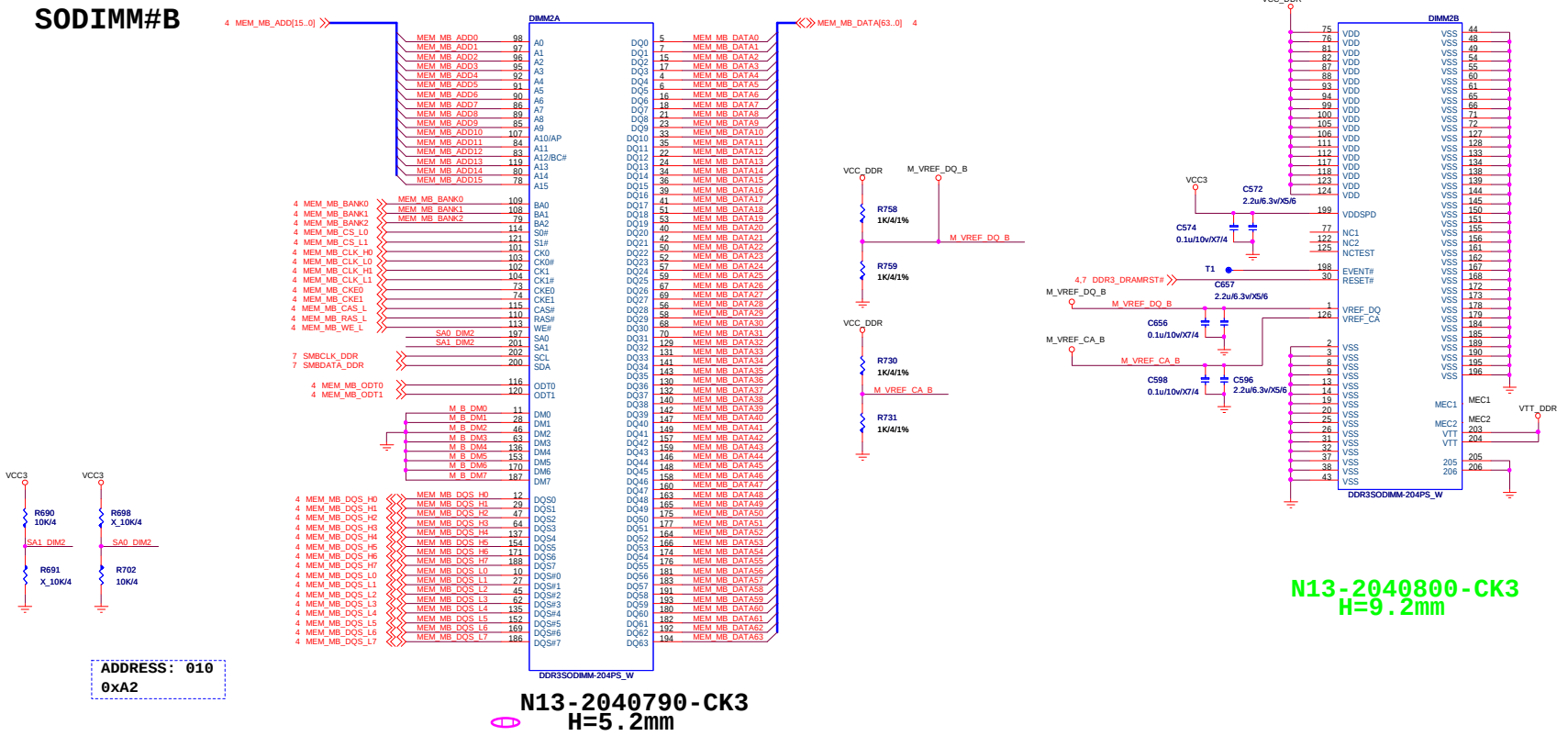
SODIMM#B

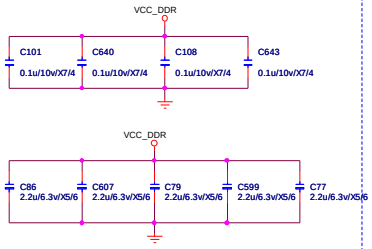


ADDRESS: 010
0xA2

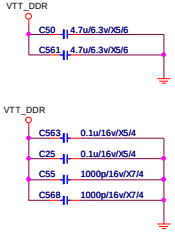
N13-2040790-CK3
H=5.2mm

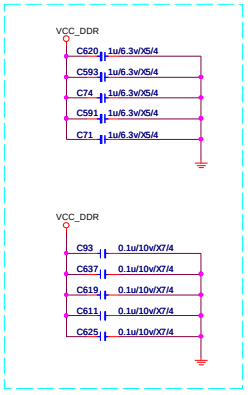
N13-2040800-CK3
H=9.2mm

Layout note: Place capacitors between and near DDR connector if possible.



CHANNEL A V_SM_VTT DECOULPING CAPS





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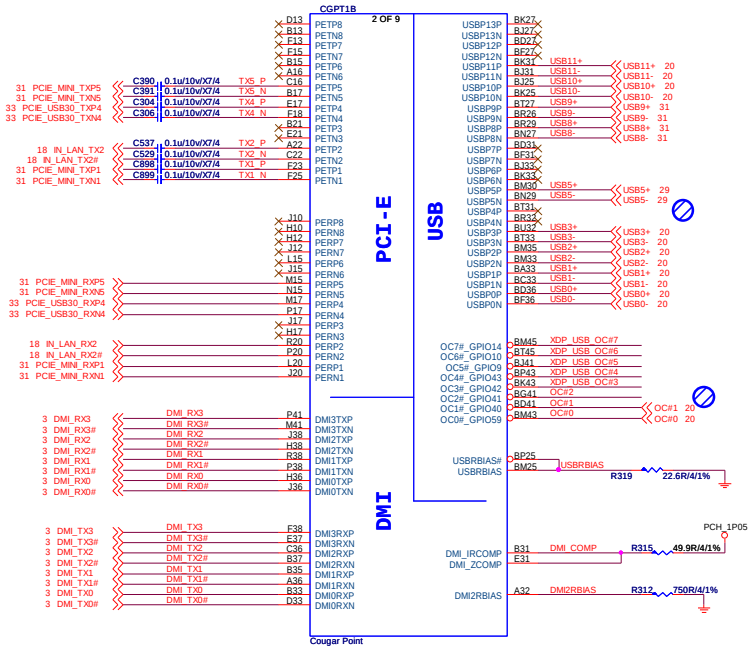
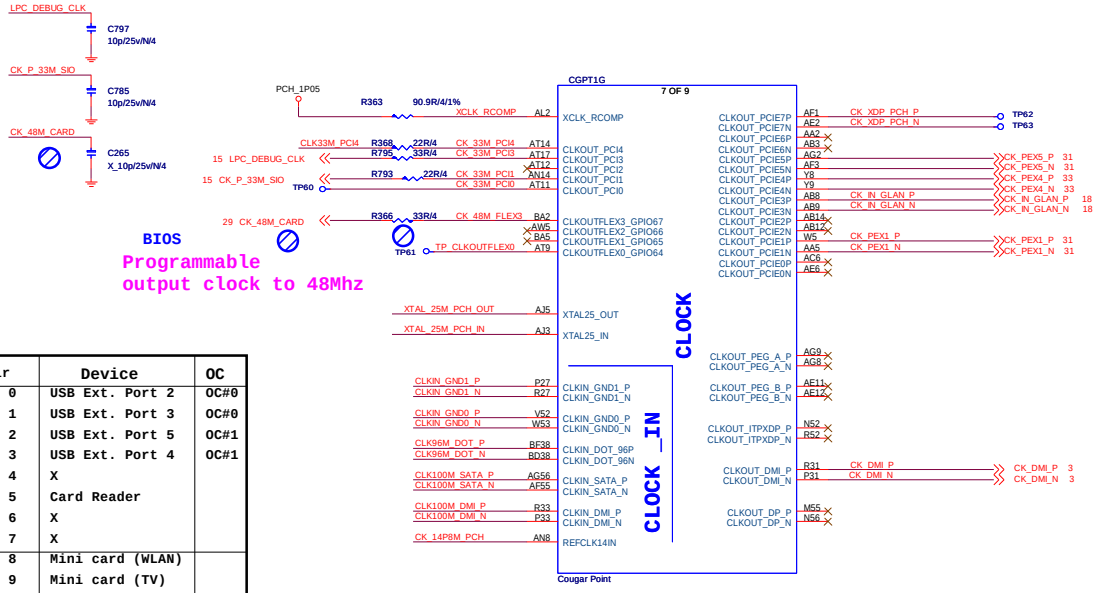
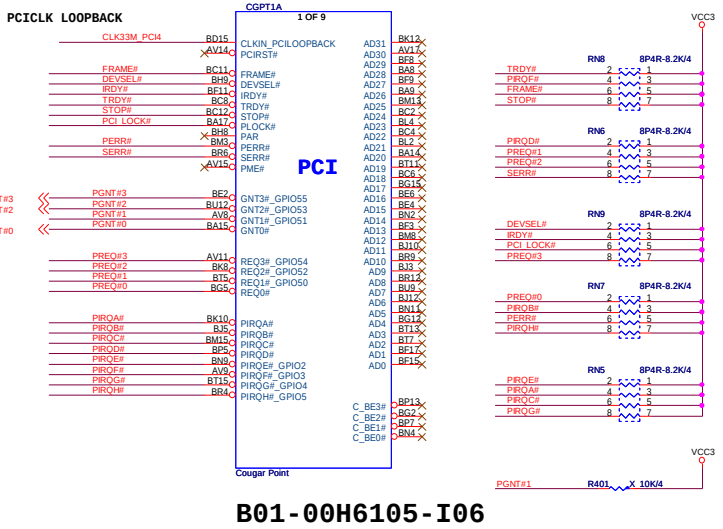
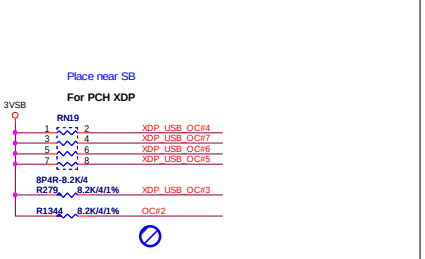
H61 SKU:PCIe ports 7 and 8 are disabled.
H61 SKU:USB ports 6, 7, 12 and 13 are disabled.

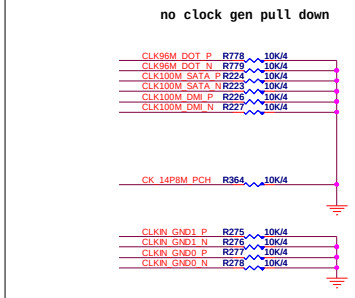


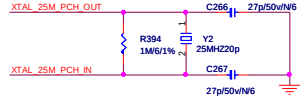


Pair		Device	OC
EHCI#1	0	USB Ext. Port 2	OC#0
	1	USB Ext. Port 3	OC#0
	2	USB Ext. Port 5	OC#1
	3	USB Ext. Port 4	OC#1
	4	X	
	5	Card Reader	
	6	X	
	7	X	
EHCI#2	8	Mini card (WLAN)	
	9	Mini card (TV)	
	10	Webcam	
	11	Touch Screen	
	12	X	
	13	X	









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MS-AA711		
Size: C	Document Description: CP PCI/E/DMI/USB/CLK	Rev: 2.1
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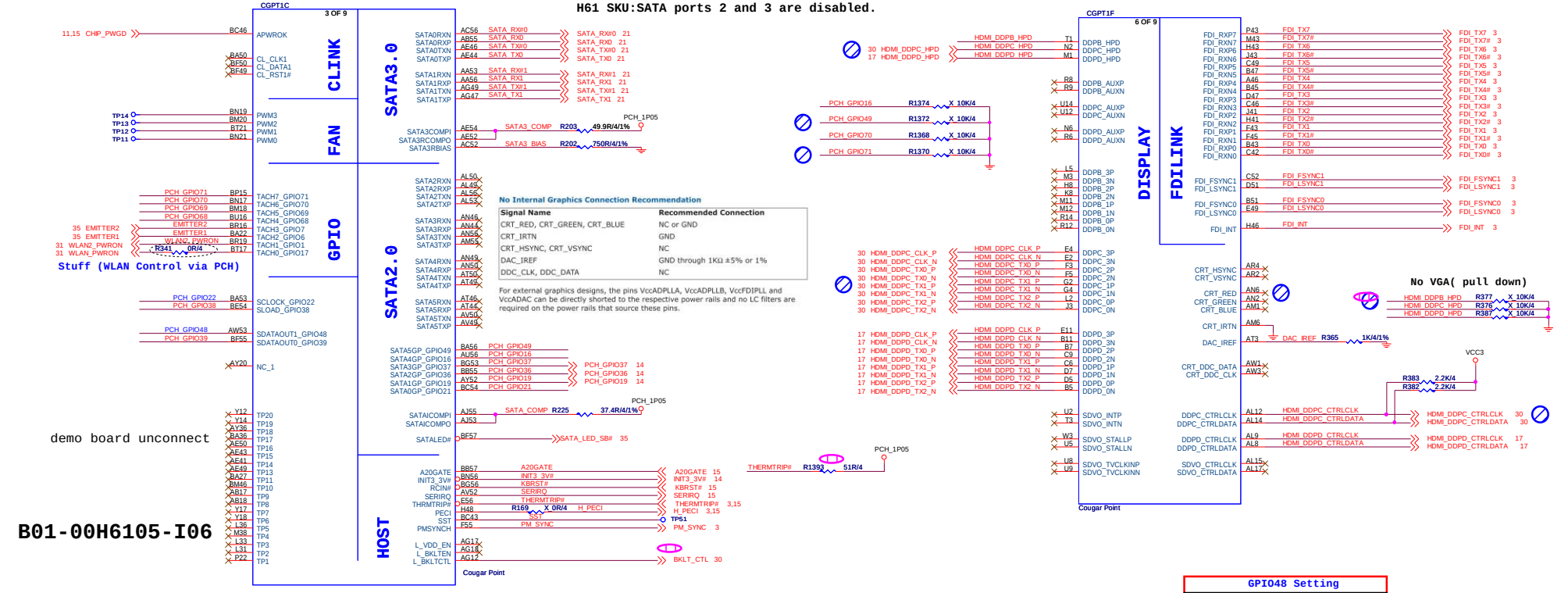
H61 SKU:SATA ports 2 and 3 are disabled.



	BOM Number	OPT	GPIO22	GPIO68	GPIO69	GPIO48	Function	ReMark
AF12			1	0	0	1	Wo/COM Wz/IR Wo/Edi-Tensor	27"
AC92			1	0	0	1	Wo/COM Wz/IR Wo/Edi-Tensor	22"
AC7B			1	0	0	1	Wo/COM Wz/IR Wo/Edi-Tensor	22"
AA5B			1	0	0	1	Wo/COM Wz/IR Wo/Edi-Tensor	20"
AA5B Win8			1	0	0	1	Wo/COM Wz/IR Wo/Edi-Tensor	20"
AA72			1	1	1	0	Wz/COM Wo/IR Wz/Edi-Tensor	20"
AA72 CKD			1	1	1	0	Wz/COM Wo/IR Wz/Edi-Tensor	20"
AA72 THTF			1	1	1	0	Wz/COM Wo/IR Wz/Edi-Tensor	20"

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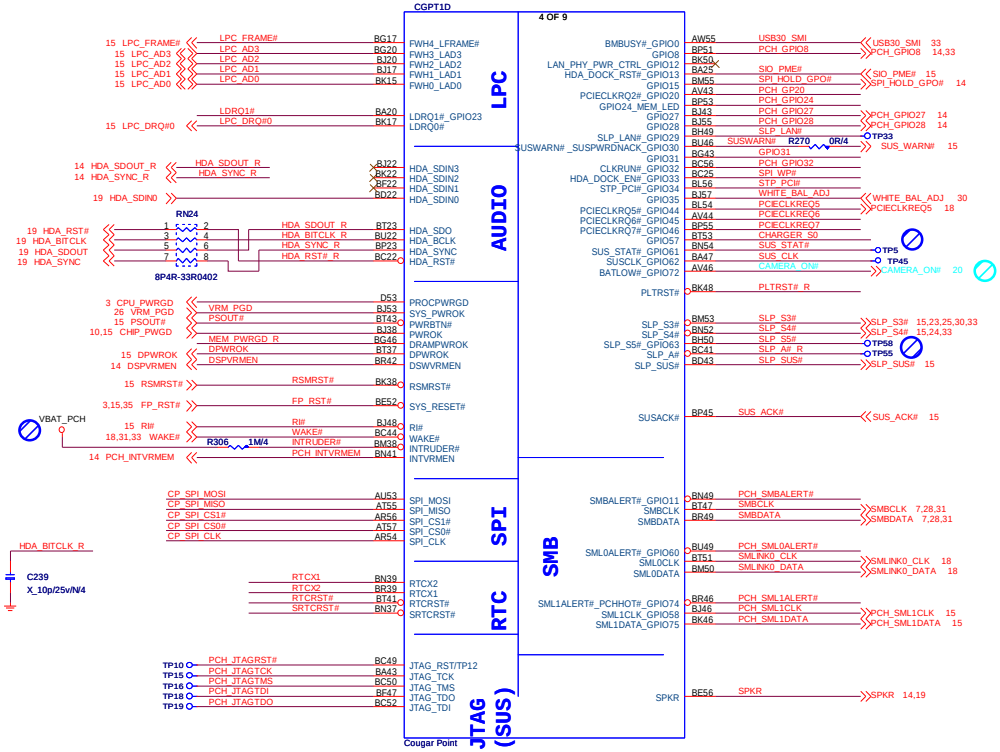

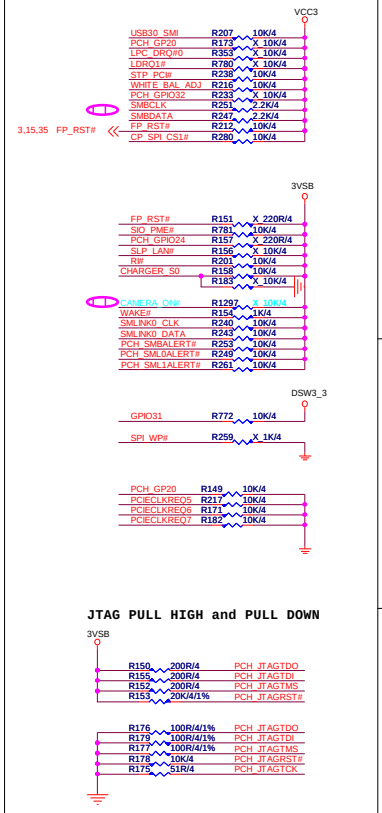

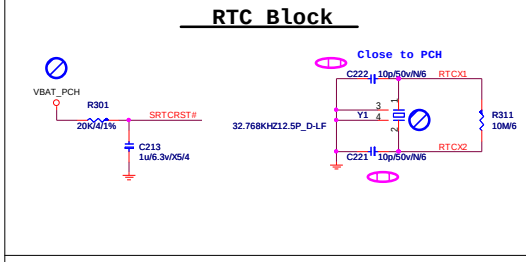

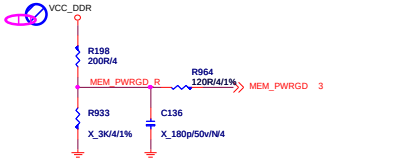

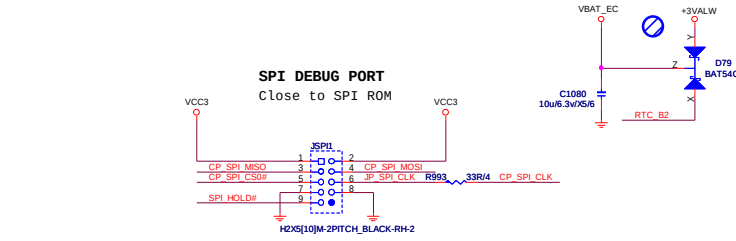

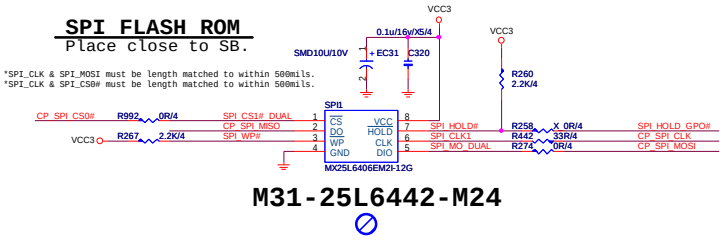

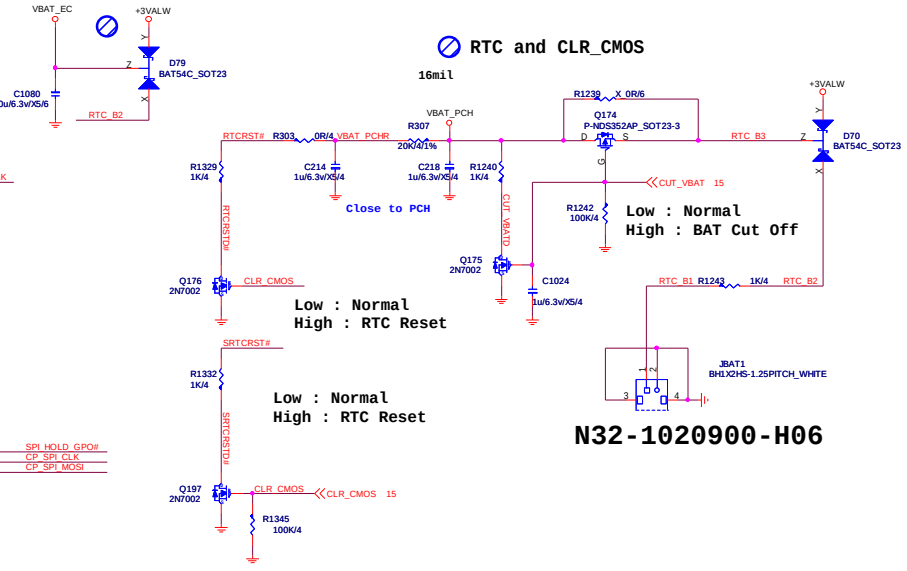

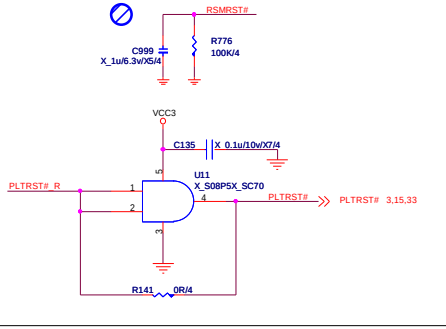

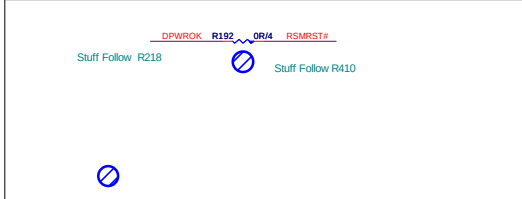

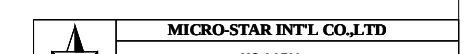

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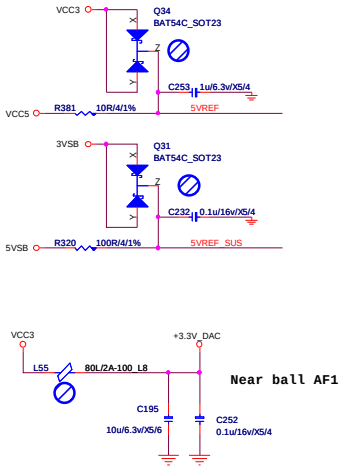
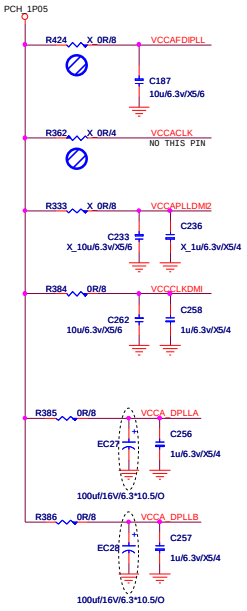
Table 3-7. VCCPLL Decoupling Requirements

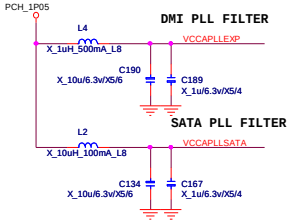
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µF 0805 X5R	1	3mΩ	0.51nH	Output		1, 2, 3

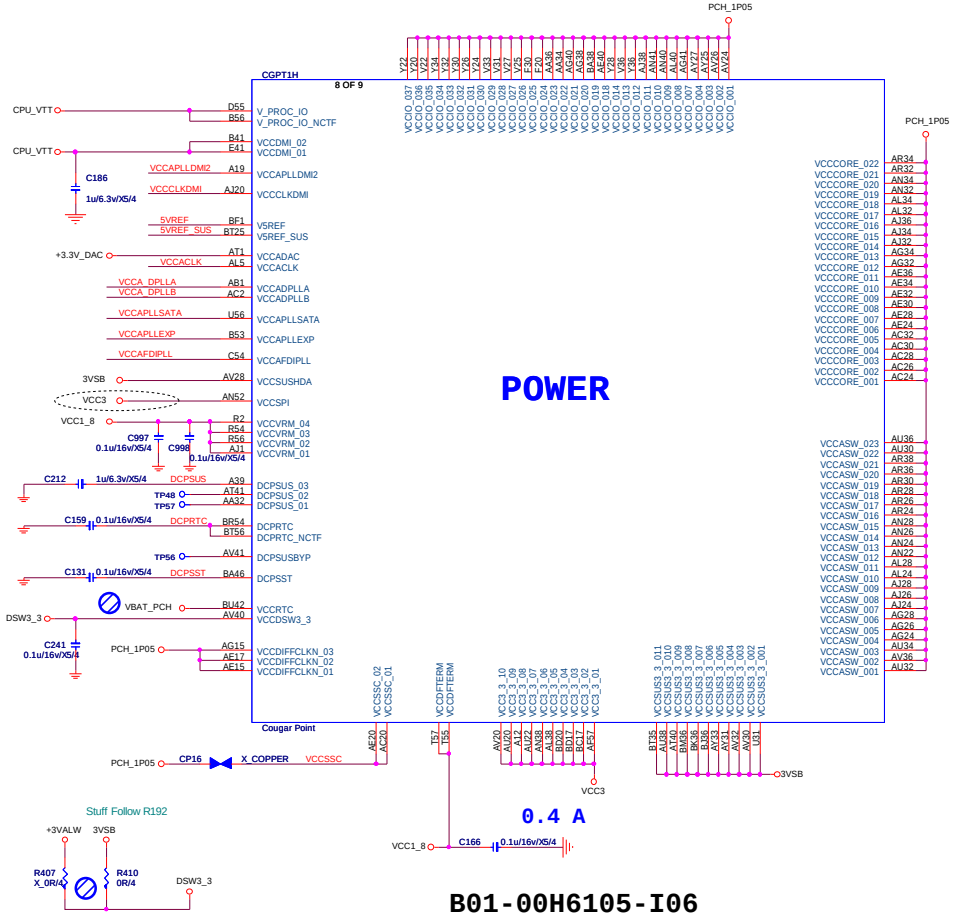
5VREF & 5VREF_SUS Sequencing Circuit



Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.



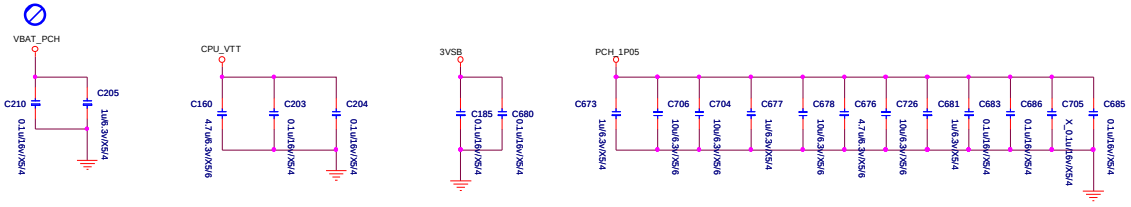


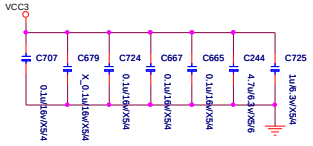


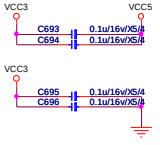
POWER

B01-00H6105-I06

PCH decoupling cap







MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AA711	
Size: C	Document Description: CP POWER	Rev: 2.1
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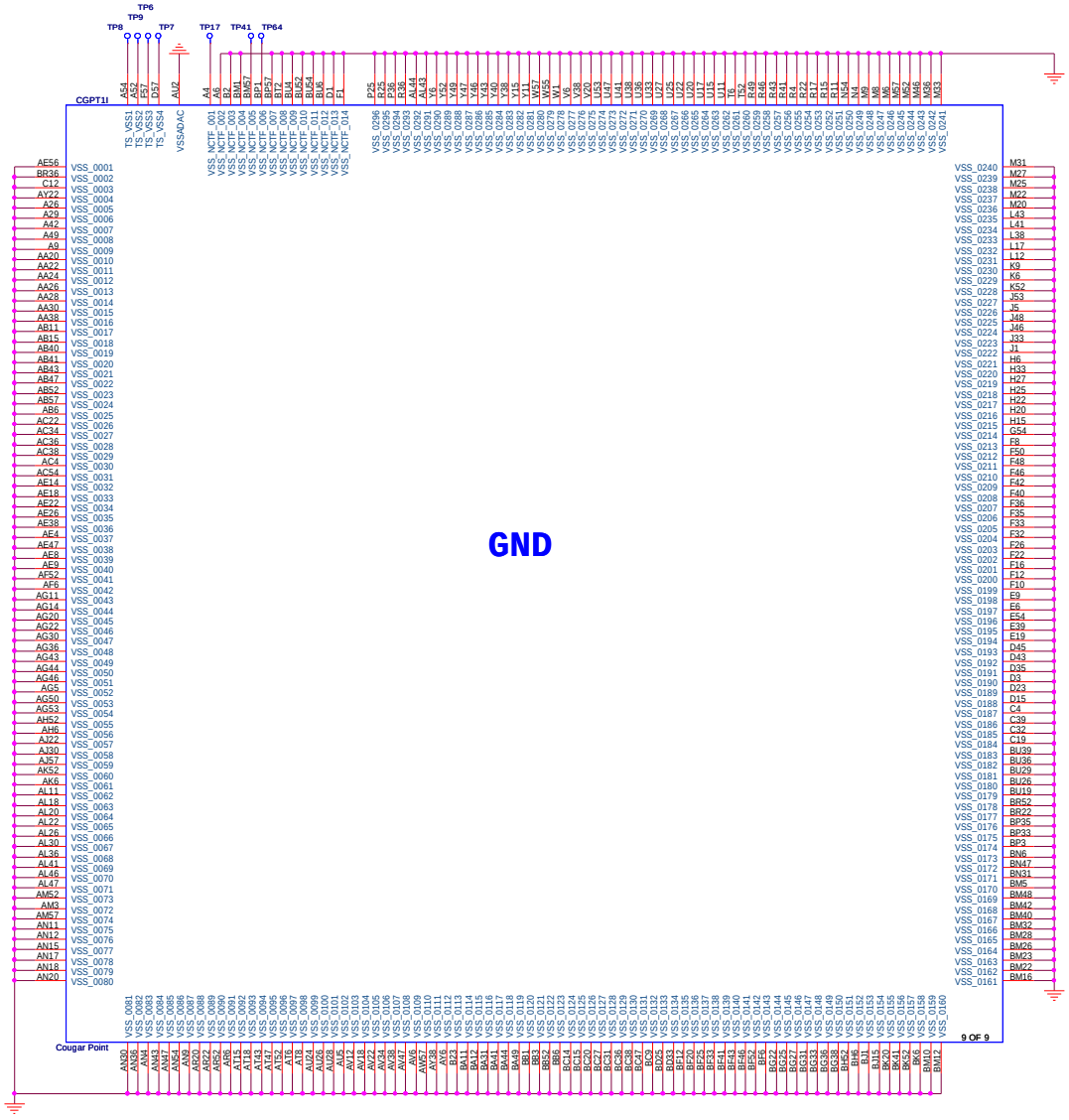
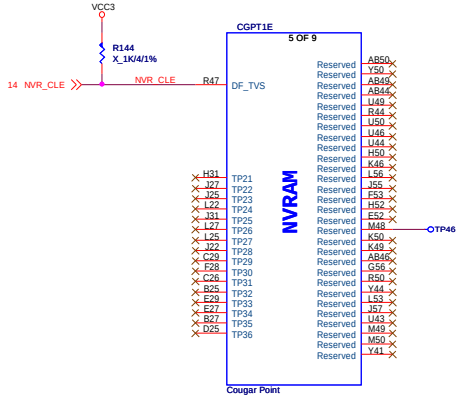


B01-00H6105-I06

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



B01-00H6105-I06

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MS-AA711			
Size: C	Document Description: CP GND/NVRAM		Rev: 2.1
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CP REQUIRED STRAPS

BOOT DEVICE	GNT0	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating

INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

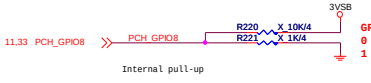
When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

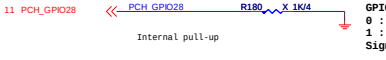
This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

DMI AC/DC MODE
0 : AC
1 : DC *

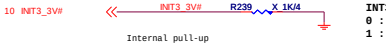
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



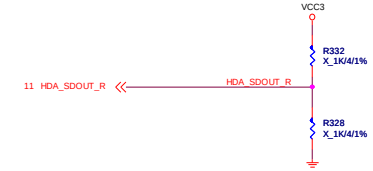
GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ????????????????
1 : ???????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

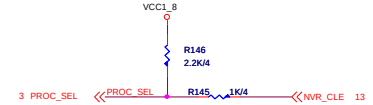
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

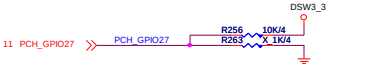
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

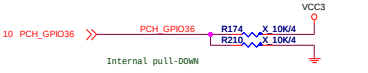


DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

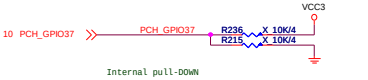
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high

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HDMI IN DETECT PIN

NCT6681D-RH

SC_SMLCLK default is Hi
GPIO pin
When SC w/o display input signal
Then SC change SC_SMLCLK to Lo

Placement On Layer 1

Monitor power button
OSD menu select down button
OSD menu select up button
OSD menu select button

Push-Pull

FOR NCT6681d STUFF

Turn on SC power

OSD state: (Reserved)
1: Scalar OSD state is turn on.
0: Scalar OSD state is turn off.

Voltage Sensing

Temperature Sensing
Place close to
VRM MOSFET

EC ROM
EEPROM Write type : W25X40

M31-25X4033-W03

TPM HEADER

WAKE ON RING

COM PORT 1

COM PORT 2

PIN	Function	DESCRIPTION
33	Strap0	XOR Tree Mode Enable. Pull-up on Pin33 with 4.7KΩ.
34	Strap1	PS2 Port Tri-state Enable and KBC Disable. Pull-up with 4.7KΩ.

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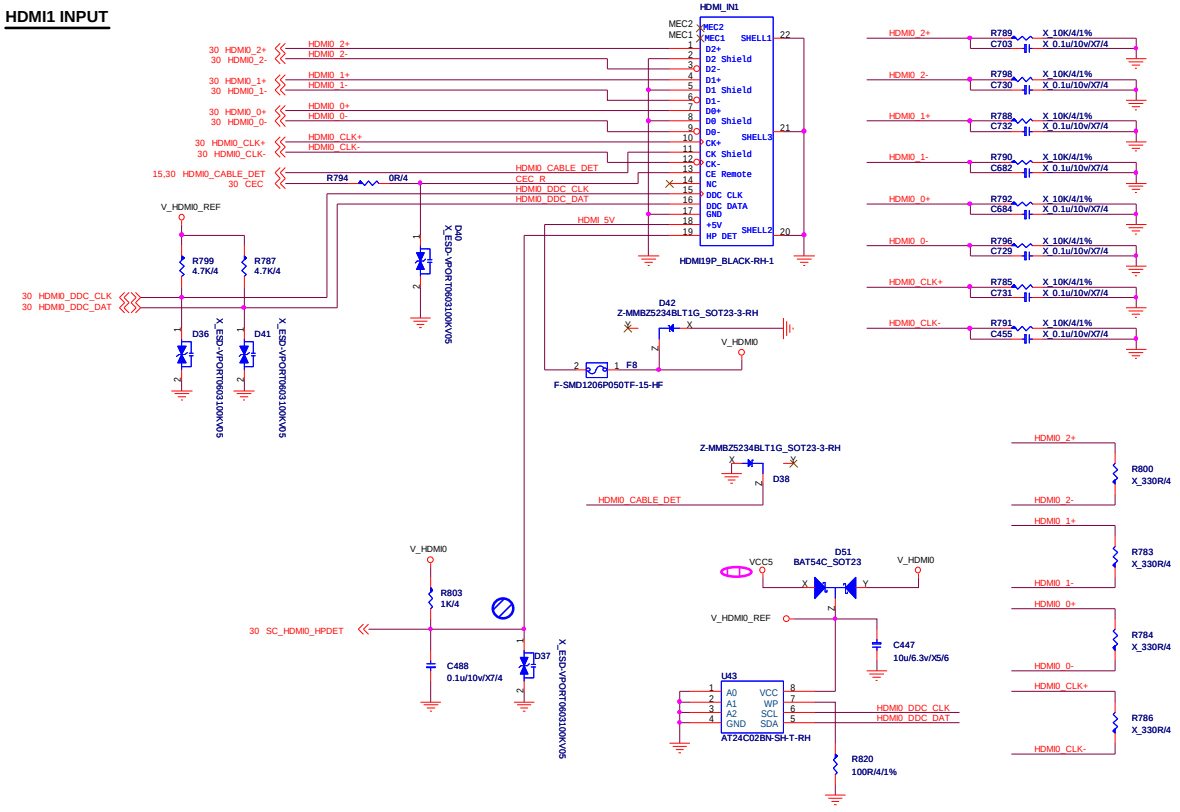
HDMI1 INPUT



M33-24C02X3-A26

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From PCH (PORT D)

10 HDMI_DDPD_TX1_N → HDMI_DDPD_TX1_N → HDMI_DDPDL_TX1_N → C480 0.1u/16v/X5/4 → HDMI_CON_DATA1- → R1327 680R/4/1%
10 HDMI_DDPD_TX1_P → HDMI_DDPD_TX1_P → HDMI_DDPDL_TX1_P → C481 0.1u/16v/X5/4 → HDMI_CON_DATA1+ → R1333 680R/4/1%
RN21 4P2R-0R; R658 X_100R/4/1%

10 HDMI_DDPD_TX2_N → HDMI_DDPD_TX2_N → HDMI_DDPDL_TX2_N → C478 0.1u/16v/X5/4 → HDMI_CON_DATA2- → R1295 680R/4/1%
10 HDMI_DDPD_TX2_P → HDMI_DDPD_TX2_P → HDMI_DDPDL_TX2_P → C479 0.1u/16v/X5/4 → HDMI_CON_DATA2+ → R1289 680R/4/1%
RN22 4P2R-0R; R657 X_100R/4/1%

10 HDMI_DDPD_TX0_N → HDMI_DDPD_TX0_N → HDMI_DDPDL_TX0_N → C432 0.1u/16v/X5/4 → HDMI_CON_DATA0- → R1325 680R/4/1%
10 HDMI_DDPD_TX0_P → HDMI_DDPD_TX0_P → HDMI_DDPDL_TX0_P → C434 0.1u/16v/X5/4 → HDMI_CON_DATA0+ → R1294 680R/4/1%
RN23 4P2R-0R; R587 X_100R/4/1%

10 HDMI_DDPD_CLK_N → HDMI_DDPD_CLK_N → HDMI_DDPDL_CLK_N → C425 0.1u/16v/X5/4 → HDMI_CON_CLK- → R1288 680R/4/1%
10 HDMI_DDPD_CLK_P → HDMI_DDPD_CLK_P → HDMI_DDPDL_CLK_P → C428 0.1u/16v/X5/4 → HDMI_CON_CLK+ → R1328 680R/4/1%
RN20 4P2R-0R; R583 X_100R/4/1%

HDMI_PL → Q109 2N7002; VCC3 → R1334 10K/4

HDMI_OUT1 (HDMI19P_BLACK-RH-1)

HDMI_CON_DATA2+	1	D2+	
	2	D2 Shield	
HDMI_CON_DATA2-	3	D2-	
HDMI_CON_DATA1+	4	D1+	
	5	D1 Shield	
HDMI_CON_DATA1-	6	D1-	
HDMI_CON_DATA0+	7	D0+	
	8	D0 Shield	
HDMI_CON_DATA0-	9	D0-	
HDMI_CON_CLK+	10	CK+	
	11	CK Shield	
HDMI_CON_CLK-	12	CK-	
	13	CE Remote	
	14	NC	
HDMI_CON_SCL	15	DDC CLK	
HDMI_CON_SDA	16	DDC DATA	
	17	GND	
HDMI_VCC5	18	+5V	
HDMI_CON_DET	19	HP DET	

MEC2, MEC1, SHELL1 → 22; SHELL3 → 21; SHELL2 → 20

N5Y-19M0221-H06

+12V → R610 4.7K/4 → Q47 N-NDS351AN_SOT23 (VCC5 → HDMI_VCC5V) → FS1 F-MICROSMD110 → HDMI_VCC5
C444 0.01u/10v/X7/4; C445 0.1u/16v/X5/4; C435 10u/6.3v/X5/6

10 HDMI_DDPD_CTRLCLK → R1336 2.2K/4 (VCC3), R1337 2.2K/4 (HDMI_VCC5) → Q199 2N7002 → HDMI_CON_SCL
10 HDMI_DDPD_CTRLDATA → R1338 2.2K/4 (VCC3), R1339 2.2K/4 (HDMI_VCC5) → Q200 2N7002 → HDMI_CON_SDA

R1389 20K/4/1% → HDMI_CON_DET
L83 180L/230mA-300_L6
VCC3 → R1390 X_0R/4; HDMI_VCC5 → R1391 0R/4
D80 BAV99_SOT23
R1392 1M/4 (VCC3, VCC3) → Q213 APM2300CAC → HDMI_DDPD_HPD 10

Reserved

Symbol	Parameter	Test Conditions	APM2300CA Min.	APM2300CA Typ.	APM2300CA Max.	Unit
Static Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	0.5	0.75	1	V

HDMI_VCC5 → D28 X_ESD-IP4220: HDMI_CON_DATA0- ↔ HDMI_CON_CLK-; HDMI_CON_DATA0+ ↔ HDMI_CON_CLK+
HDMI_VCC5 → D27 X_ESD-IP4220: HDMI_CON_SCL ↔ HDMI_CON_DET; HDMI_CON_SDA
HDMI_VCC5 → D29 X_ESD-IP4220: HDMI_CON_DATA1- ↔ HDMI_CON_DATA2-; HDMI_CON_DATA1+ ↔ HDMI_CON_DATA2+

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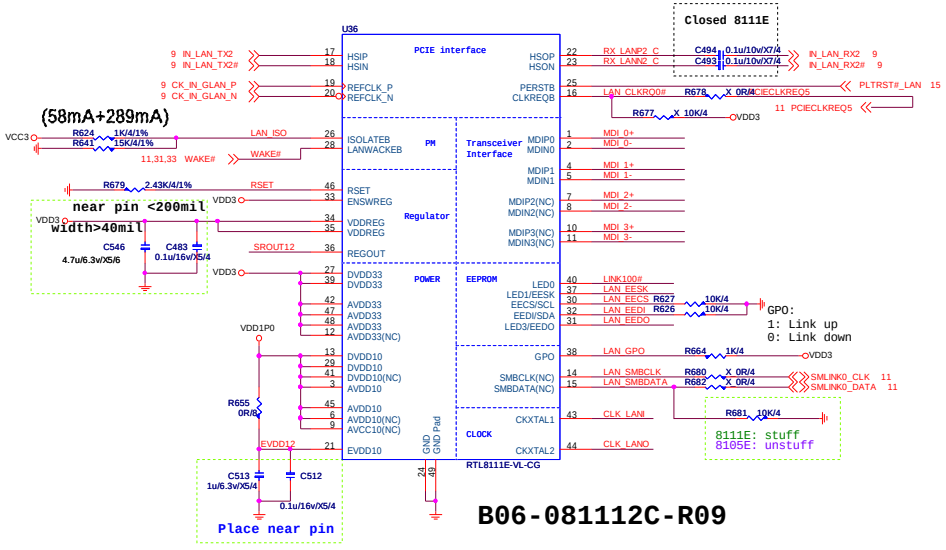
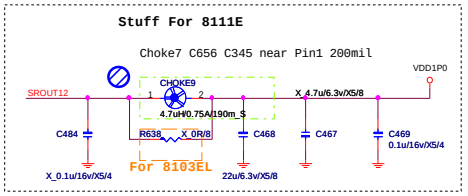
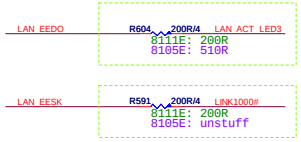
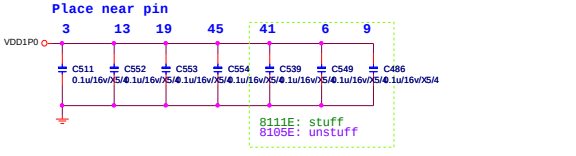
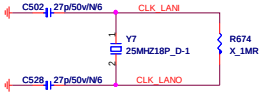


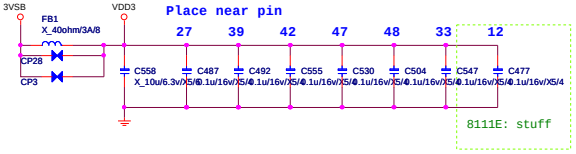
B06-081112C-R09

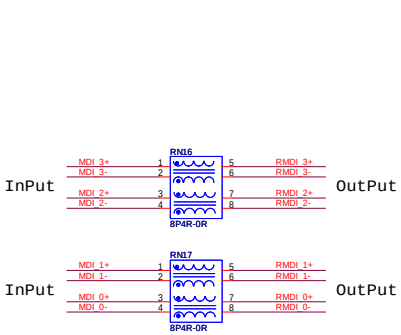


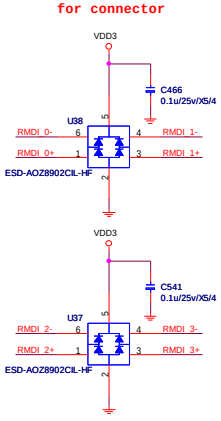


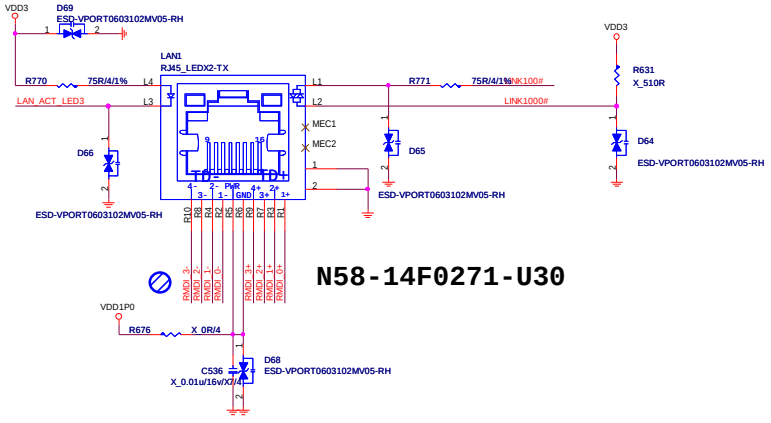












N58-14F0271-U30

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MS-AA711		
Size: C	Document Description: Giga LAN RTL8111E	Rev: 2.1
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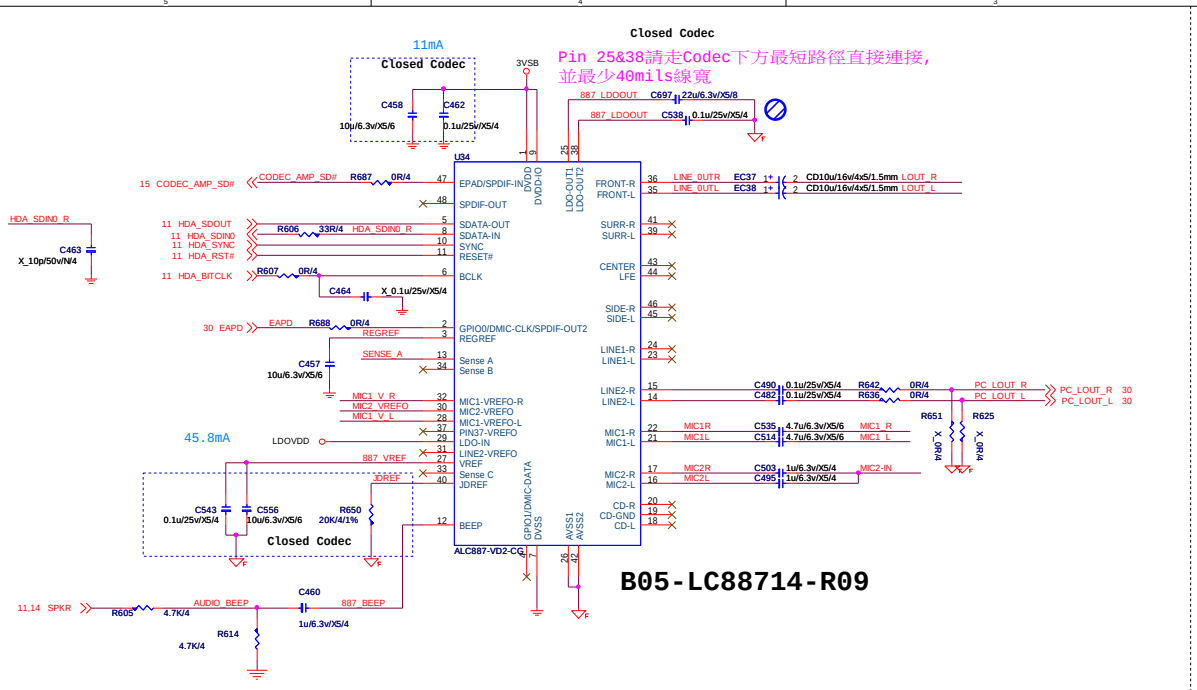

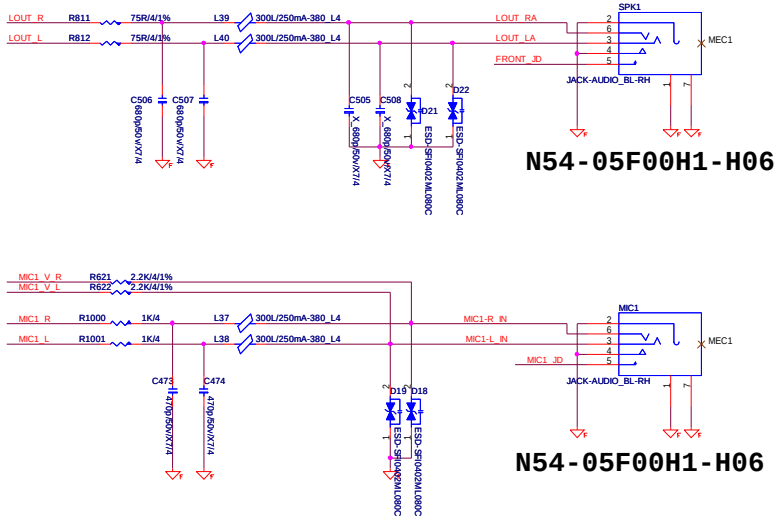

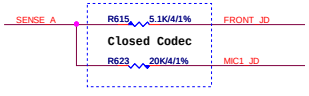

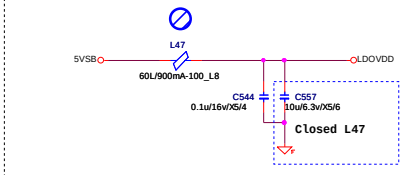

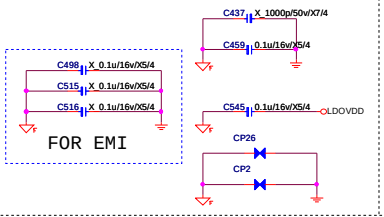

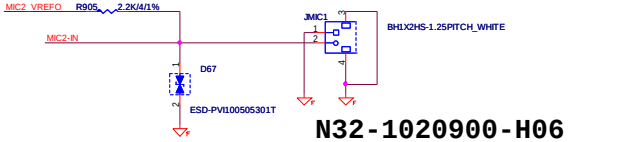

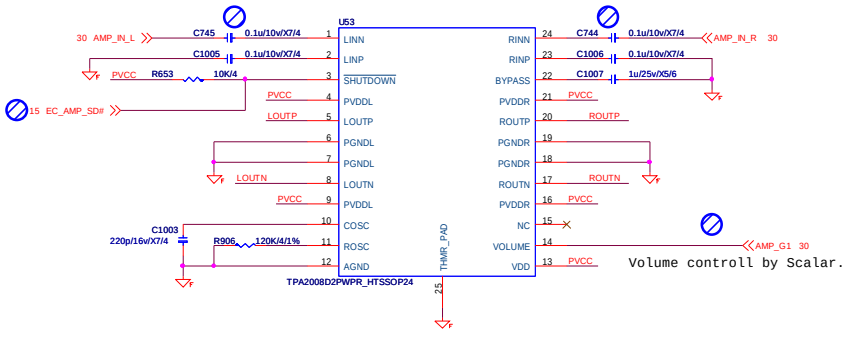

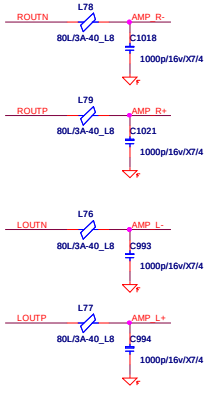

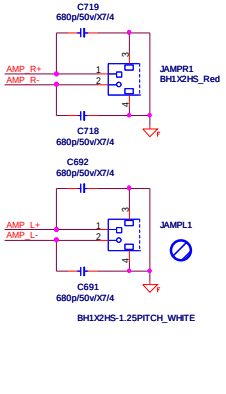

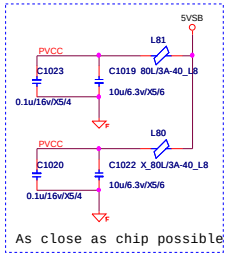

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	MS-AA711	
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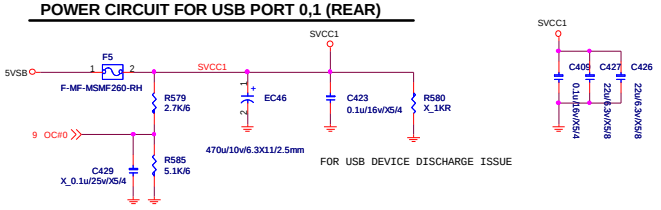
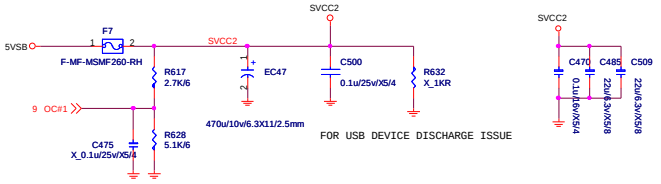
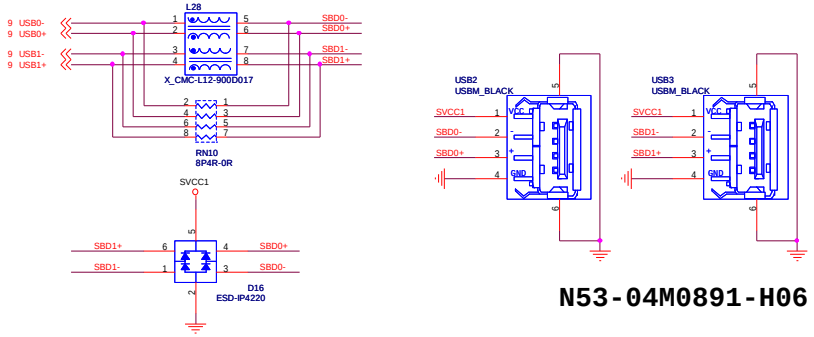
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



POWER CIRCUIT FOR USB PORT 2,3 (REAR)

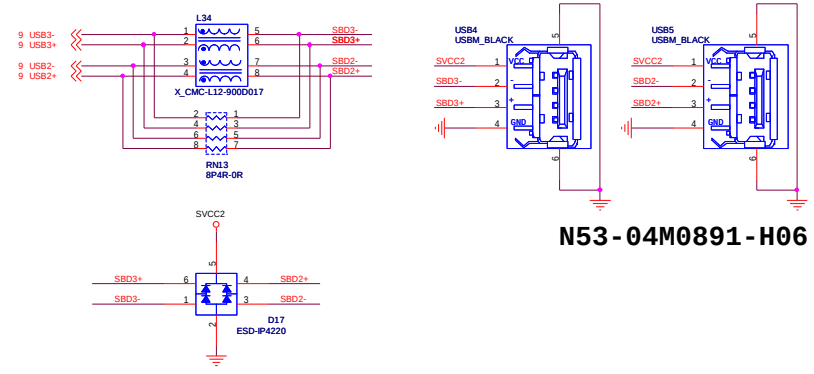


REAR PANEL USB CONNECTOR FOR USB PORT 0,1



N53-04M0891-H06

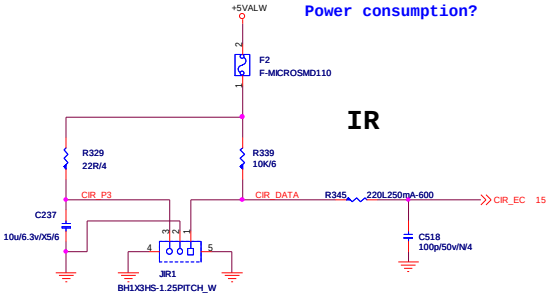
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



N53-04M0891-H06

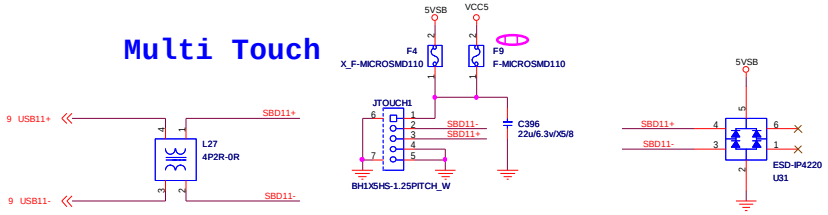
Power consumption?

IR



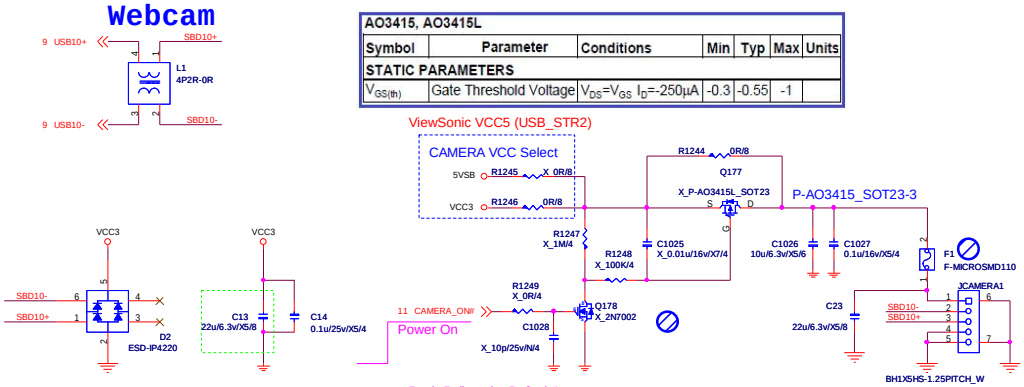
N32-1030130-H06

Multi Touch



N32-1050600-H06

Webcam



AO3415, AO3415L						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.3	-0.55	-1	

N32-1050600-H06

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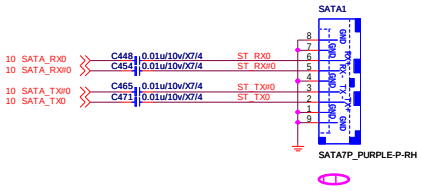
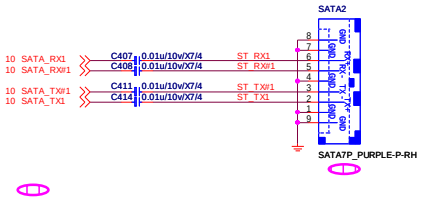
SATA HDD

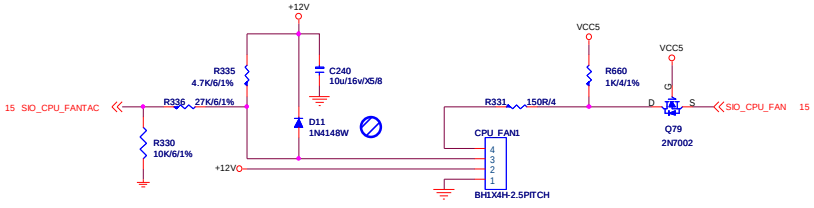


SATA ODD



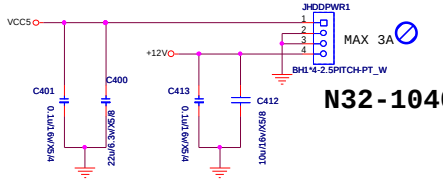
N5N-07M0221-H06

CPU FAN



N32-1040BP1-H06

HDD & ODD Power



N32-1040D31-H06

1.3 Intel® 6 Series Chipset and Intel® C200 Series Chipset SKU Definition

Table 1-2. Desktop Intel® 6 Series Chipset SKUs

Feature Set		SKU Name(s)						
		Q67	Q65	B65	Z68	H67	P67	H61
PCI Express* 2.0 Ports		8	8	8	8	8	8	6[9]
PCI Interface		Yes	Yes	Yes	No[10]	No[10]	No[10]	No[10]
USB 2.0 Ports		14	14	12[6]	14	14	14	10[7]
Total number of SATA ports		6	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)		2[4]	1[5]	1[5]	2[4]	2[4]	2[4]	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)		4	5	5	4	4	4	4[8]
HDMI/DVI/VGA/DisplayPort*/eDP*		Yes	Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP		Yes	Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	Yes	No[3]
	RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	Yes	No
	Intel RST SSD Caching[11]	No	No	No	Yes	No	No	No
Intel® AT		Yes	Yes	No	No	No	No	No
Intel® AMT 7.0		Yes	No	No	No	No	No	No

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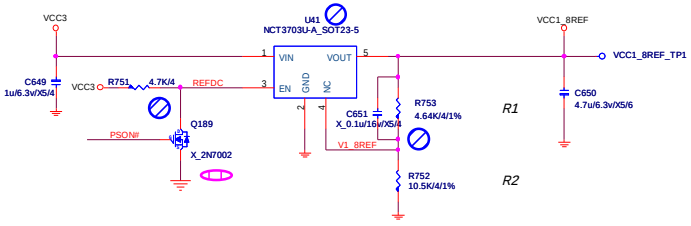
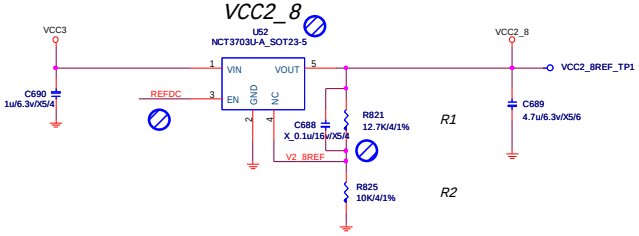
VCC1_8REF

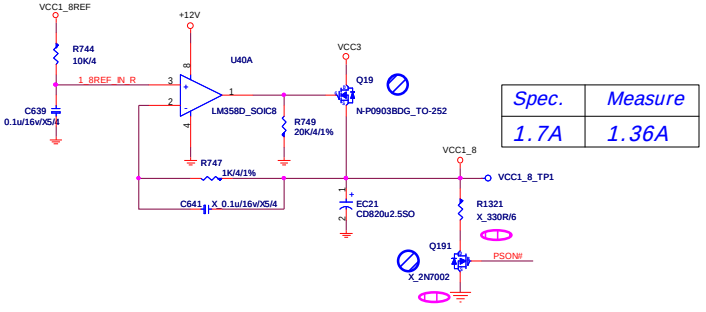


NCT3703U
Vo=Vref(1+R1/R2)*
Vref=1.25

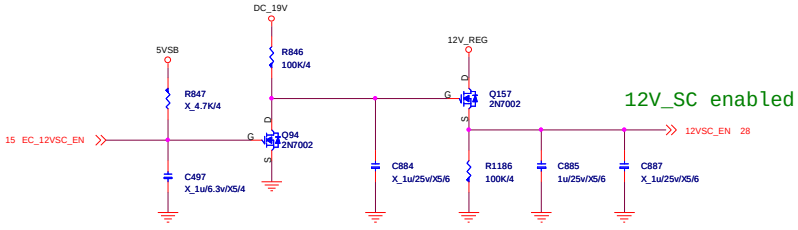
VCC2_8



CPU_PLL_1_8

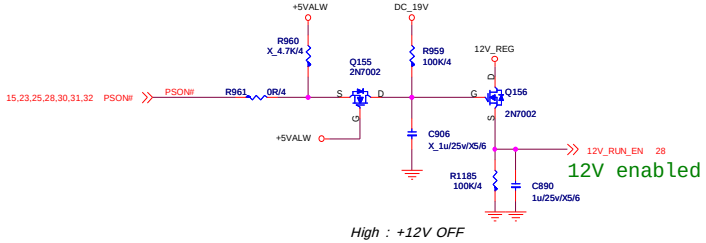


Spec.	Measure
1.7A	1.36A



High : 12V_SC OFF
Low : 12V_SC ON

RUN POWER ACPI



High : +12V OFF
Low : +12V ON

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	MS-AA711	
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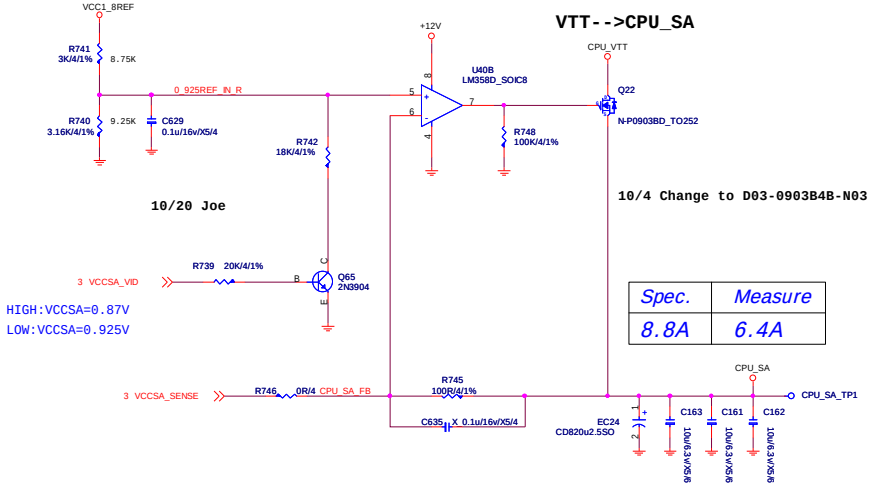
CPU_SA Power

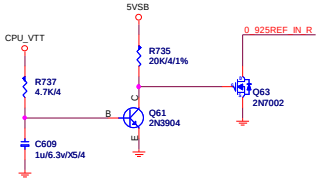


Spec.	Measure
8.8A	6.4A

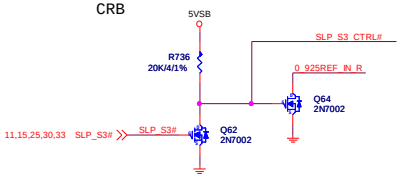
Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 X5R	2	3mΩ	0.5nH	Output	Inside processor socket cavity	1,13

Waitting CPU_VTT Ready

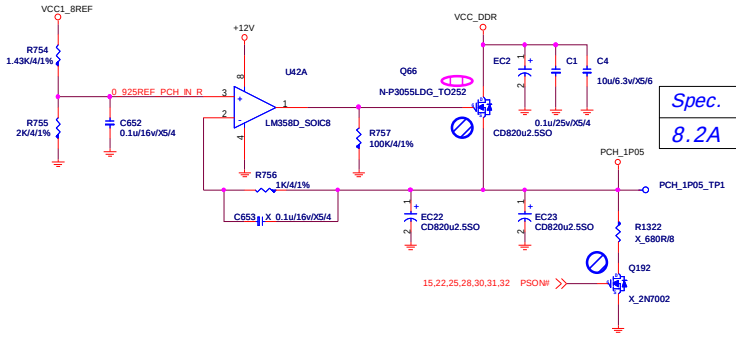


CRB



CP Power

DDR-->PCH



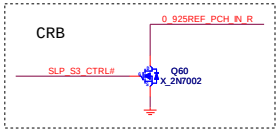
Spec.	Measure
8.2A	6.56A

Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x µF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1X560uF 2x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different that those shown.

CRB



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MS-AA711

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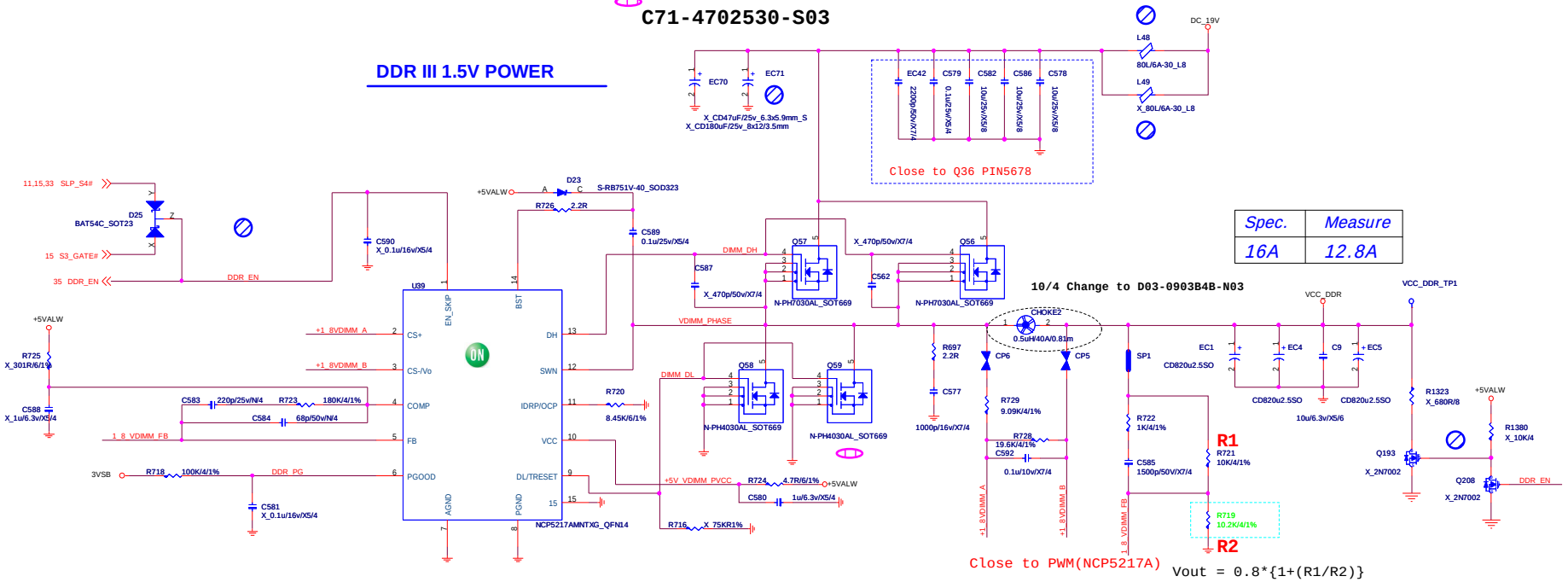
C71-4702540-N07

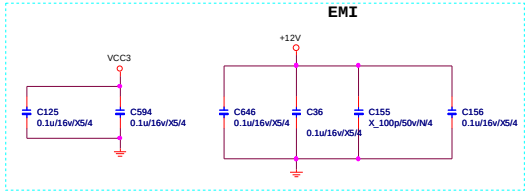
C71-4702530-S03

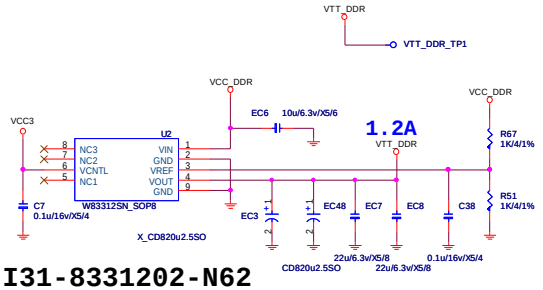
DDR III 1.5V POWER



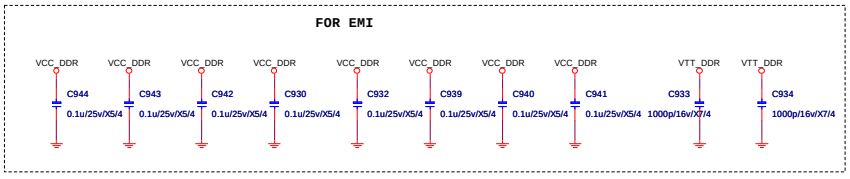
Spec.	Measure
16A	12.8A

I32-5217A0C-O05





I31-8331202-N62



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MS-AA711		
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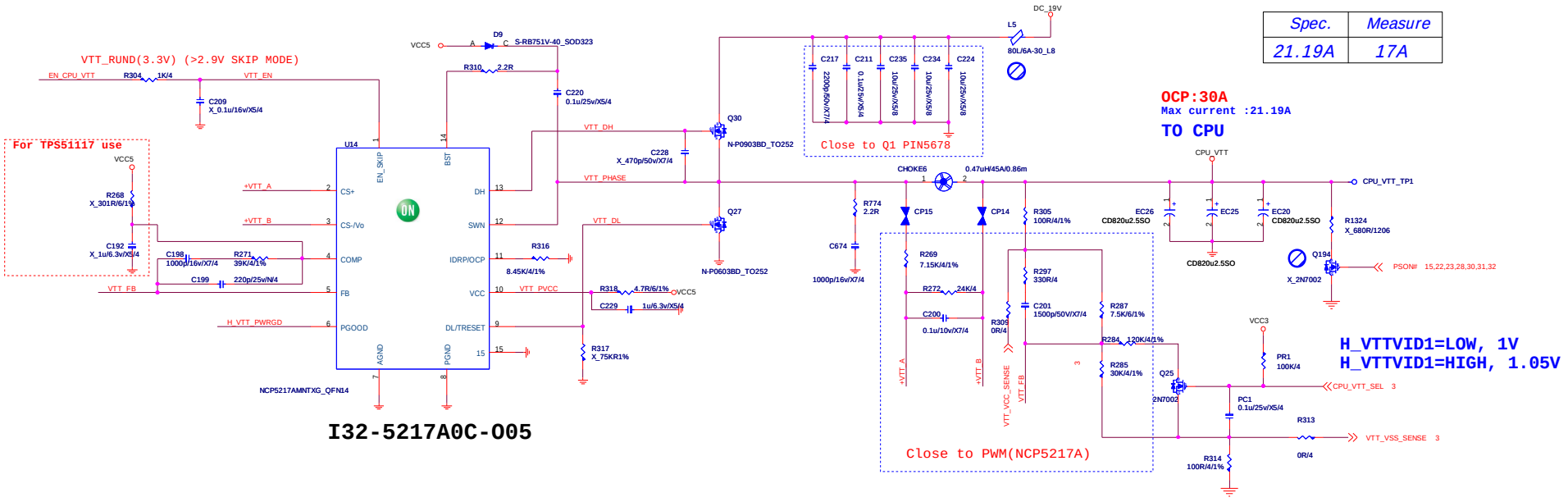
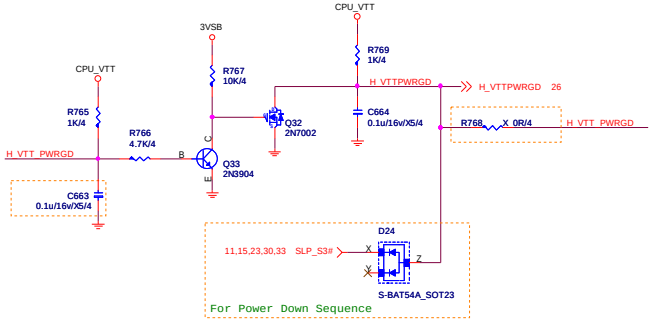
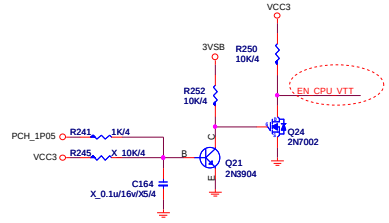


Spec.	Measure
21.19A	17A





1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA

If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K

2. Csen = L/Rocset*DCR

If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

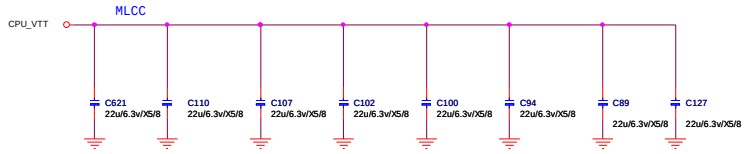


Table 3-6. VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

MICRO-STAR INT'L CO.,LTD	
MS-AA711	
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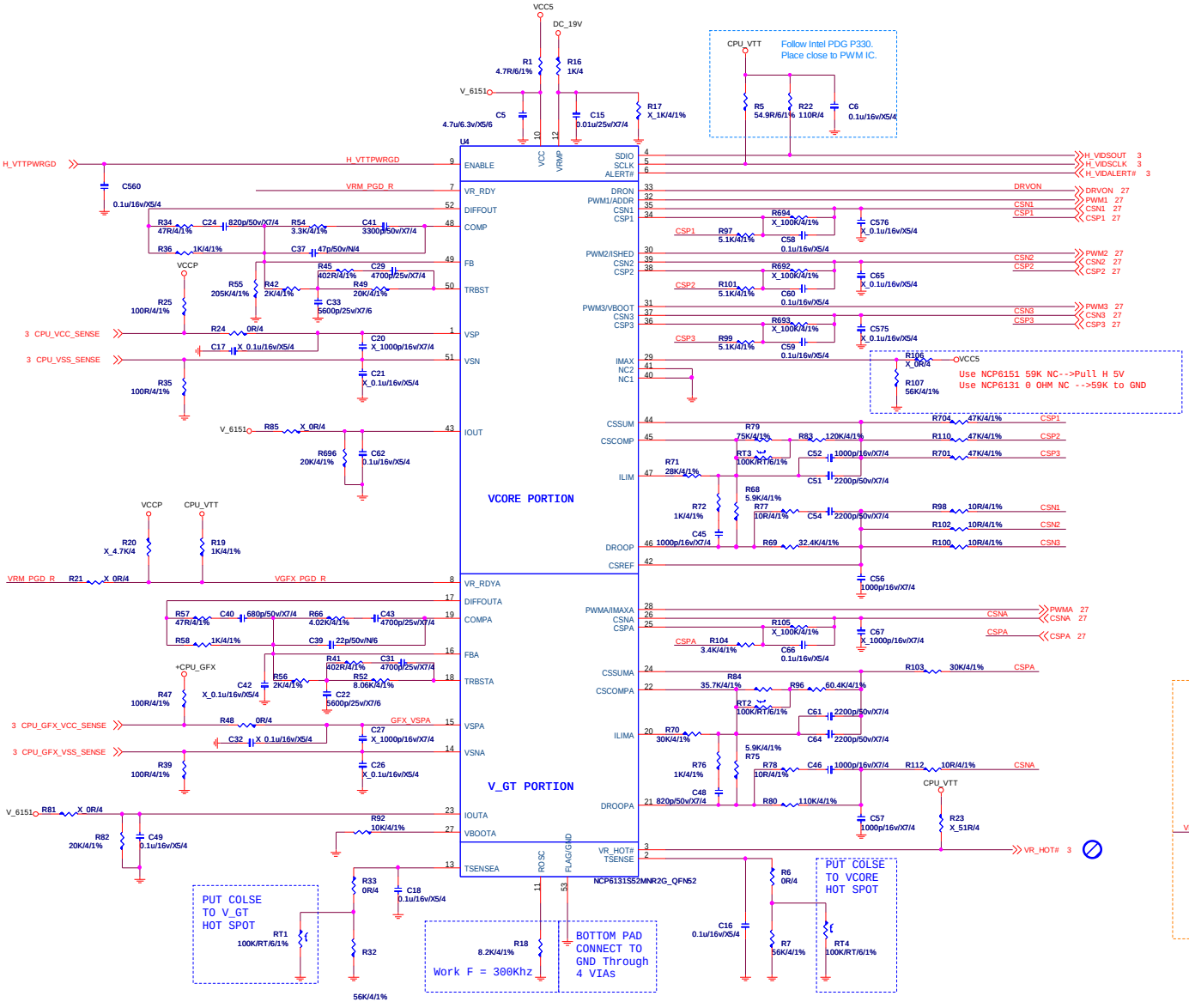
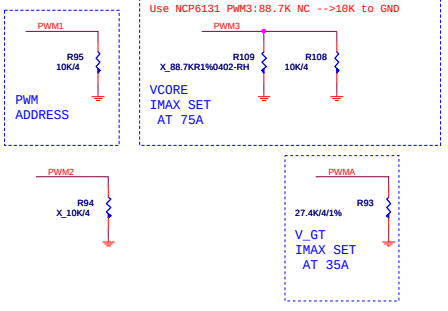
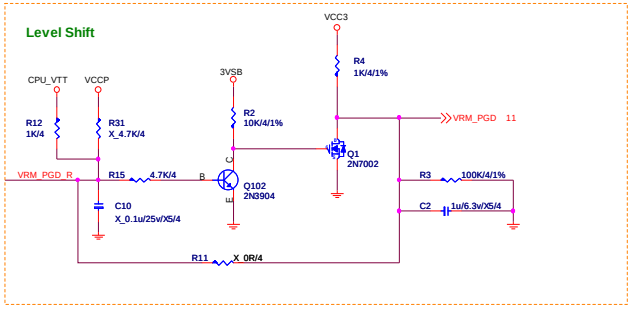
Modulize of NCP6151/NCP6131 COLAY (19V VR12)



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101





I32-6131S0C-005

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MS-AA711		
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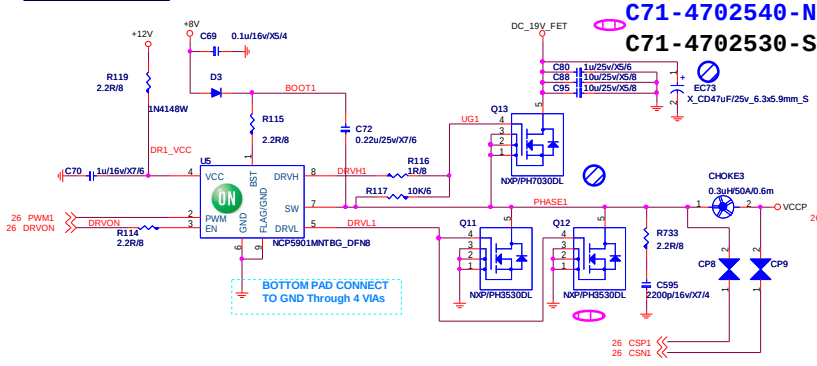
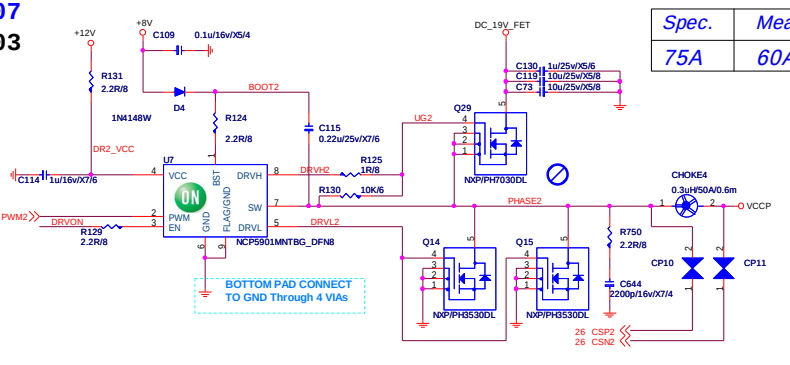
High Side D03-7030D09-N47
Low Side D03-3530D09-N47

+CPU_VCCP

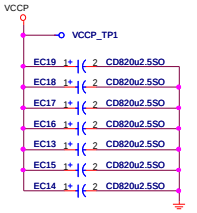
C71-4702540-N07
C71-4702530-S03

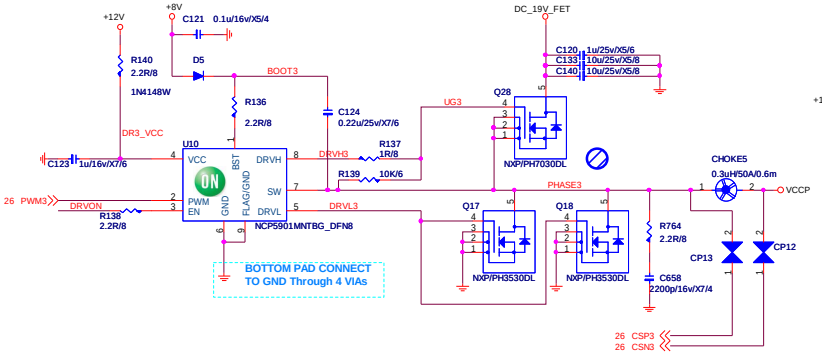




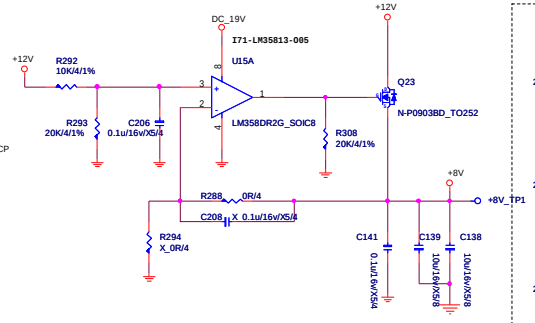
Spec.	Measure
75A	60A

+CPU_VCCP Output Caps

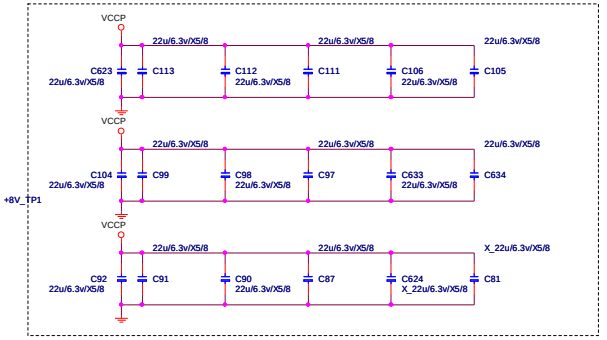




12V to 8V 0.5A

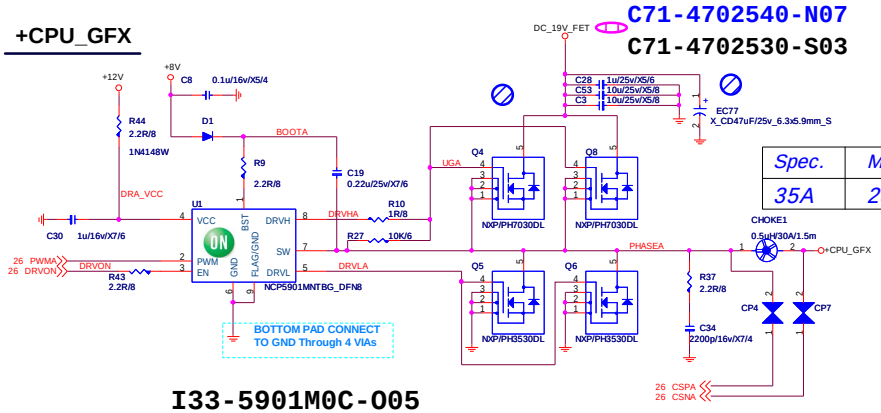


+CPU_VCCP-Decoupling



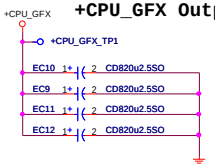
+CPU_GFX

C71-4702540-N07
C71-4702530-S03

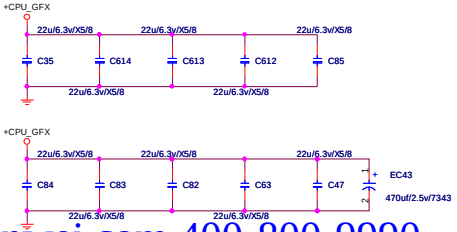


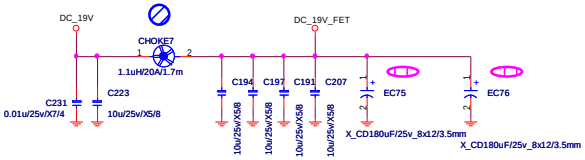
Spec.	Measure
35A	28A

+CPU_GFX Output Caps

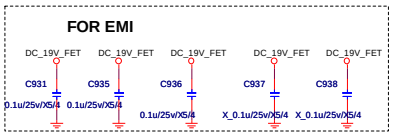


+CPU_GFX Decoupling





FOR EMI



I33-5901M0C-005

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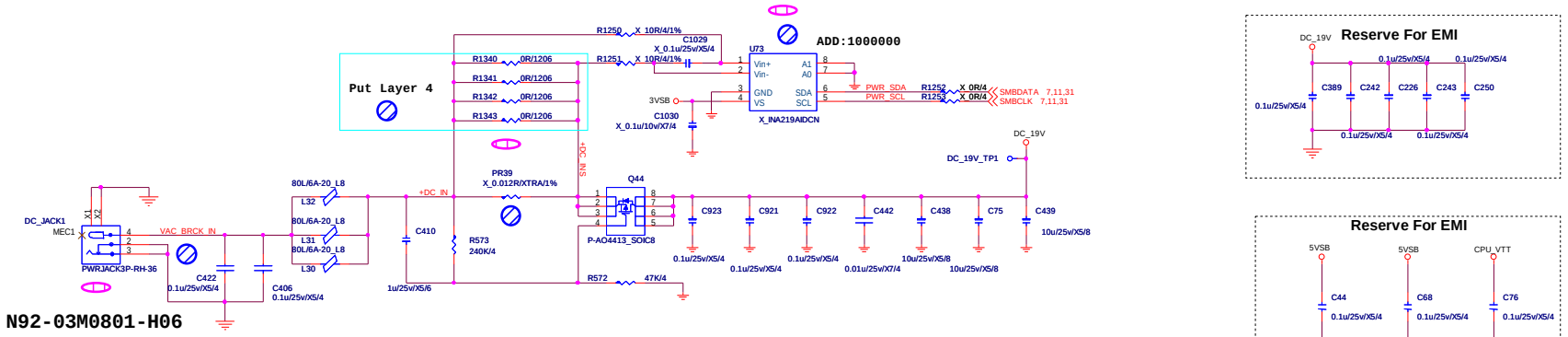
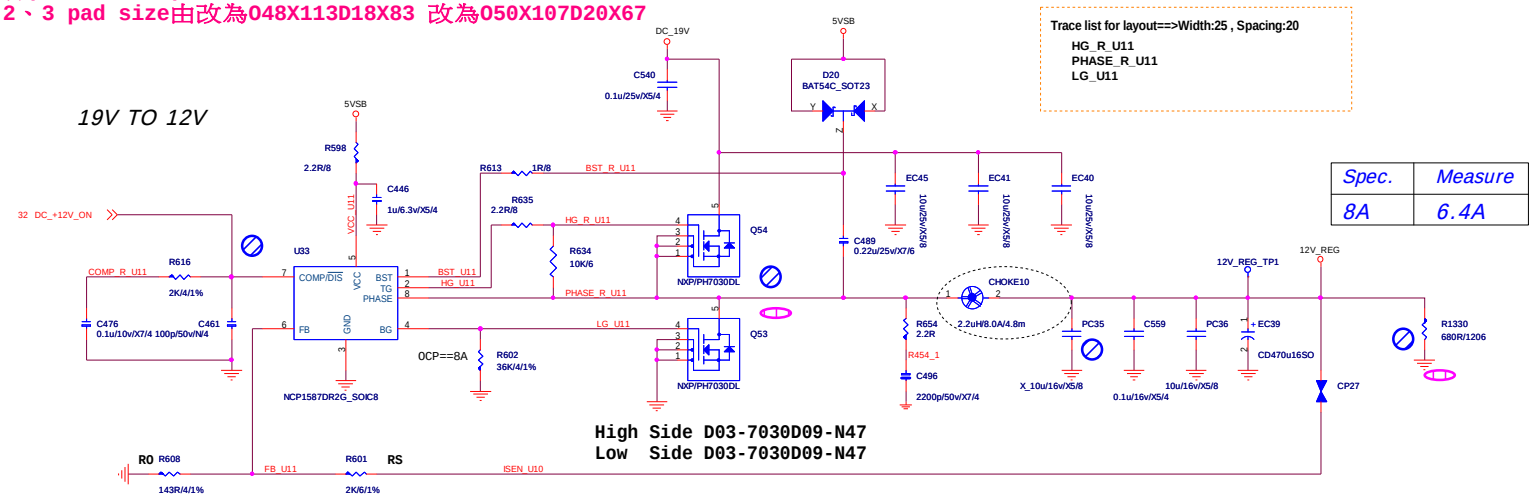


N92-03M0801-H06

請 Layout 重新 更新 Footprint
將零件pin x1、x2 pad size由O50X107D20X67改為O48X113D18X83，
pin 2、3 pad size由改為O48X113D18X83 改為O50X107D20X67



Trace list for layout==>Width:25 , Spacing:20
HG_R_U11
PHASE_R_U11
LG_U11

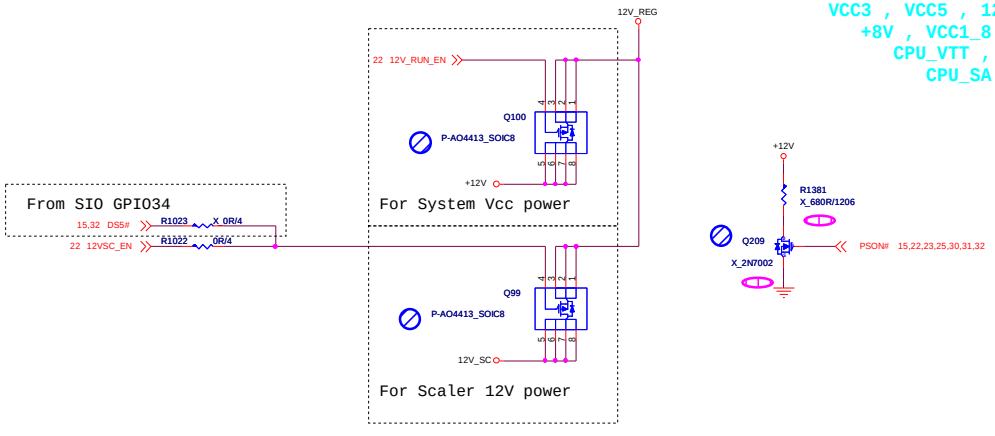
Spec.	Measure
8A	6.4A

High Side D03-7030D09-N47
Low Side D03-7030D09-N47

I32-0158703-O05

Vout = 0.8 (1 + 2K / 143) = 11.989 Volt

DC_19 Volt
+3VALW , +5VALW
VCC3 , VCC5 , 12V_REG , VCC_DDR , VTT_DDR
+8V , VCC1_8 , PCH_1p05
CPU_VTT , +1_5RUN
CPU_SA , VCCP , +CPU_GFX



MICRO-STAR INT'L CO.,LTD
MS-AA711
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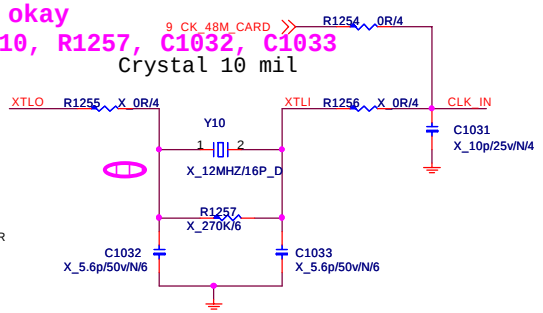
CLK	MODE1 Pin 27 R1262	MODE0 Pin 42 R1258
48MHz	X	X
24MHz	X	1
12MHz (XTAL)	1	1

SBD6 + (USB_CARD_P) / SBD6 – (USB_CARD_N) (Zdiff) is 90Ω±10%
Maintain at least 20 mils air gap to the edge of the reference plane

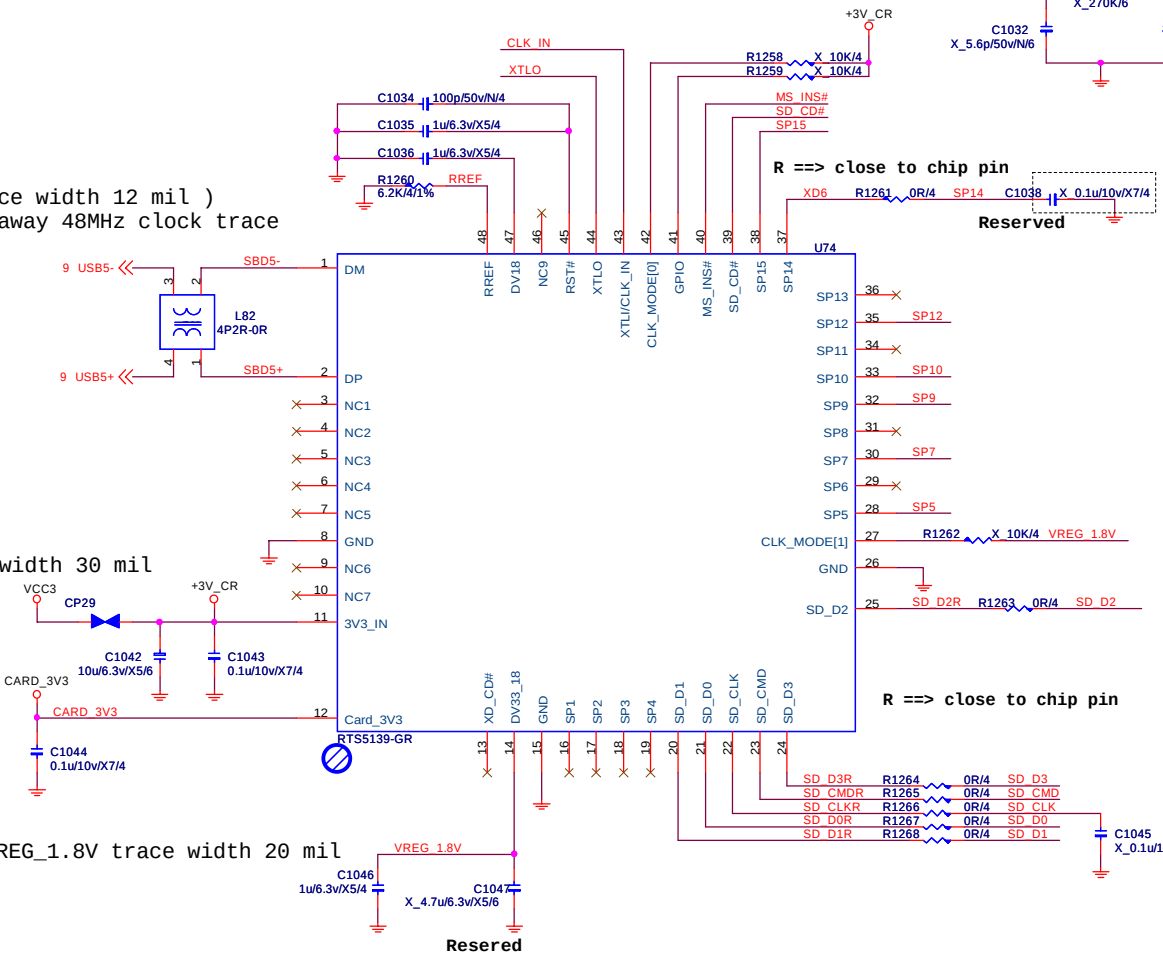
| CLK – DATA | trace length ≦ 100 mils
| DATA – DATA | trace length ≦ 100 mils
no more 2 via ; 2 inch (maximum)

MS_SCLK (Pin 37 SP14) & SD_CLK (Pin 22 SD_CLK)
are impedance are 50Ω±15%

CK_48M_CARD if okay
MP BOM remove Y10, R1257, C1032, C1033
Crystal 10 mil



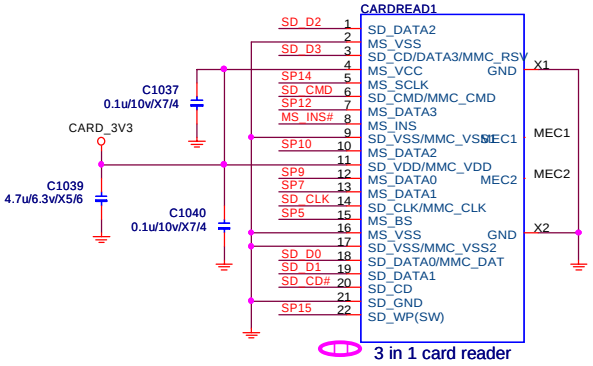
Pin 48(RREF trace width 12 mil)
trace must far away 48MHz clock trace



+3V_CR trace width 30 mil

VREG_1.8V trace width 20 mil

Resered



N58-22F1610-T01

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MS-A612		
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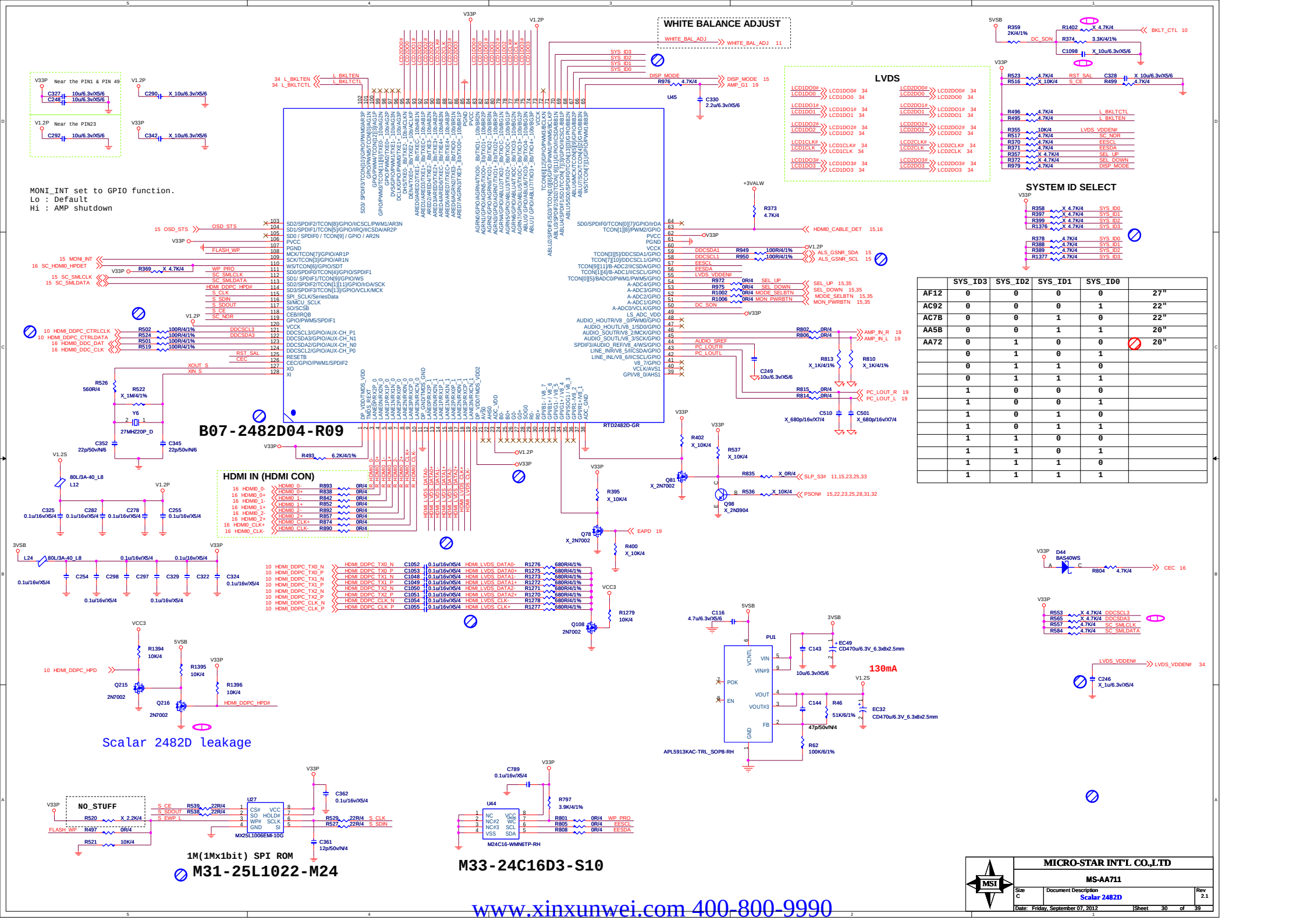
WHITE BALANCE ADJUST
WHITE_BAL_ADJ
WHITE_BAL_ADJ 11
LVDS
SYSTEM ID SELECT
MONI_INT set to GPIO function.
Lo : Default
Hi : AMP shutdown
B07-2482D04-R09
RTD2482D-GR
HDMI IN (HDMI CON)
Scalar 2482D leakage
NO_STUFF
1M(1Mx1bit) SPI ROM
M31-25L1022-M24
M33-24C16D3-S10
MX25L1006EMI-10G
M24C16-WMN6TP-RH
APL5913KAC-TRL_SOP8-RH
130mA
SYS_ID3 SYS_ID2 SYS_ID1 SYS_ID0
AF12 0 0 0 0 27"
AC92 0 0 0 1 22"
AC7B 0 0 1 0 22"
AA5B 0 0 1 1 20"
AA72 0 1 0 0 20"
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1
MICRO-STAR INT'L CO.,LTD
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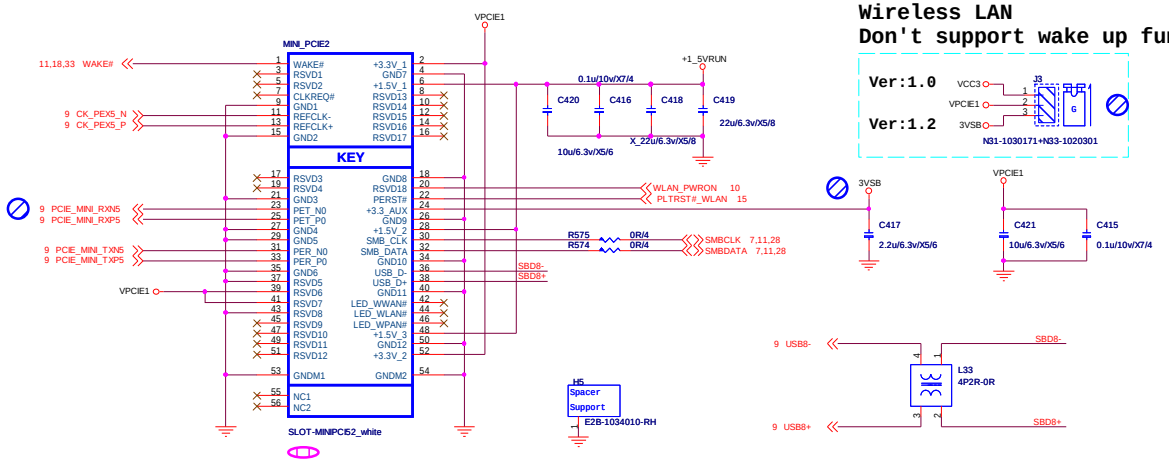
www.xinxunwei.com 400-800-9990

Wireless LAN(Short Card)

VCC3, 1.5A

+1_5VRUN, 0.5A

Wireless LAN
Don't support wake up function.



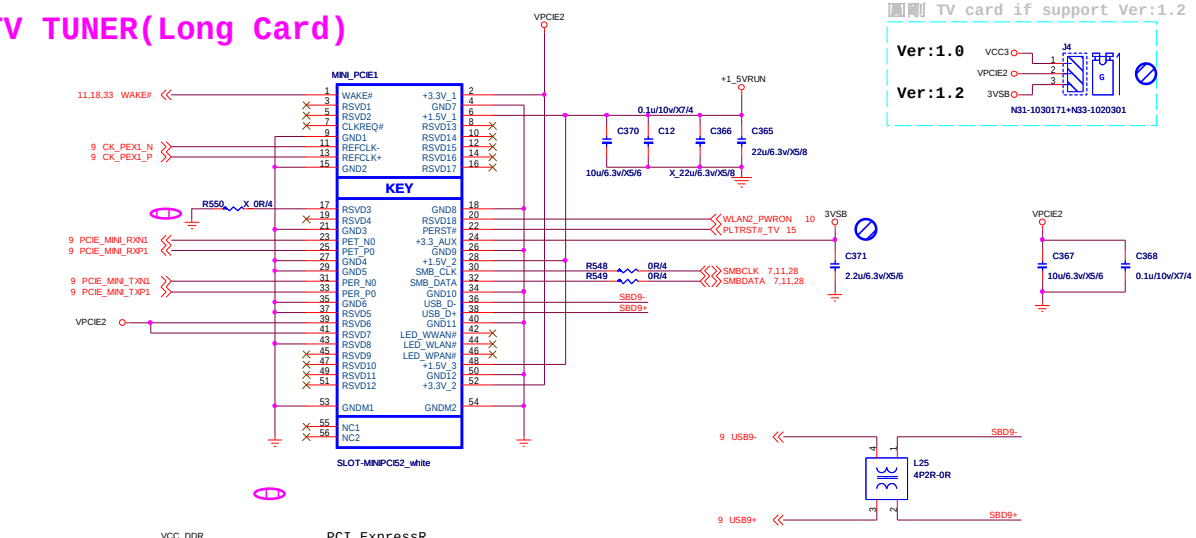
N11-0520240-K06

TV TUNER(Long Card)

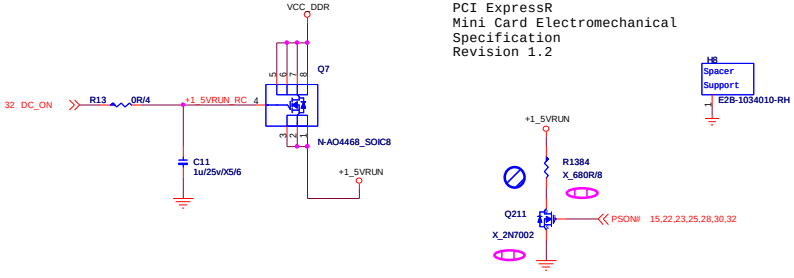
VCC3, 1.5A

+1_5VRUN, 0.5A

TV card if support Ver:1.2



PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2



MICRO-STAR INT'L CO.,LTD		
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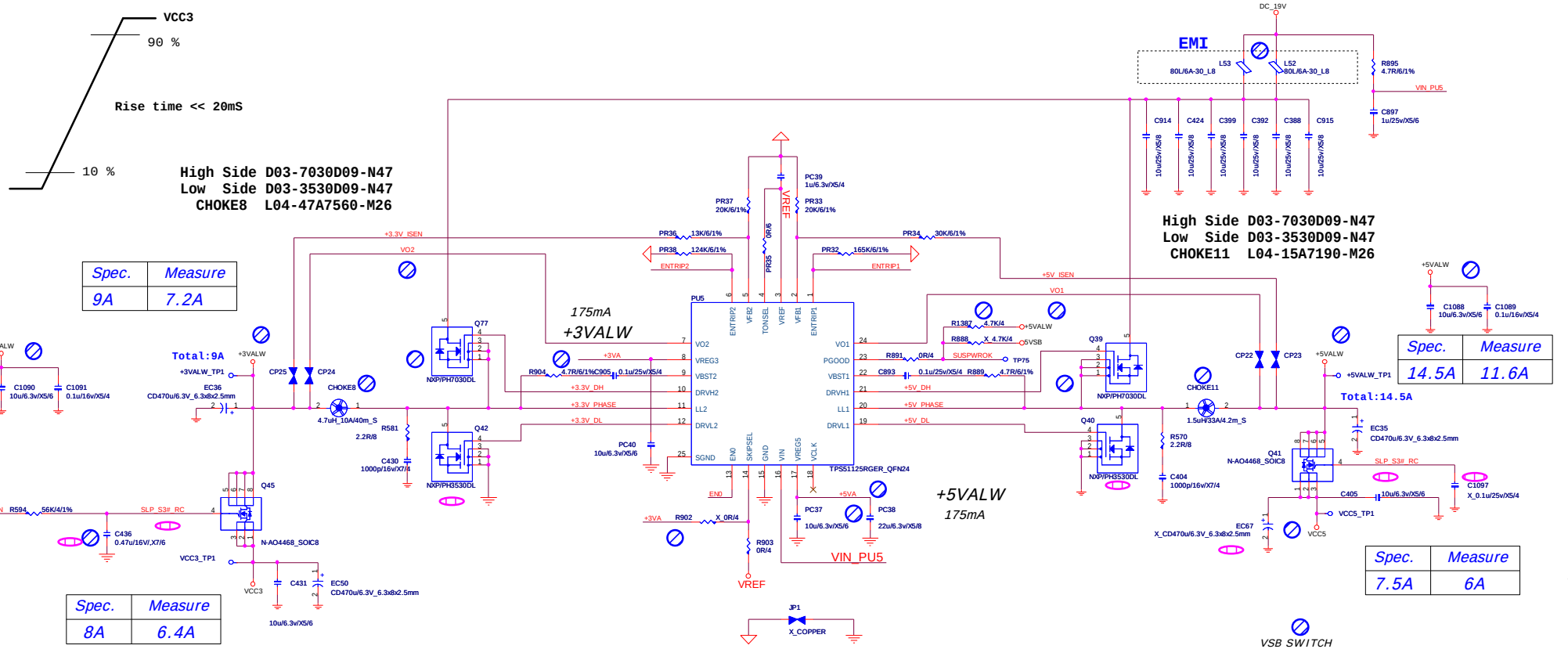

TPS51125

SLUS786A–OCTOBER 2007–REVISED NOVEMBER 2007

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Softstart						
T_{ss}	Internal SS time	Internal soft start	1.1	1.6	2.1	ms

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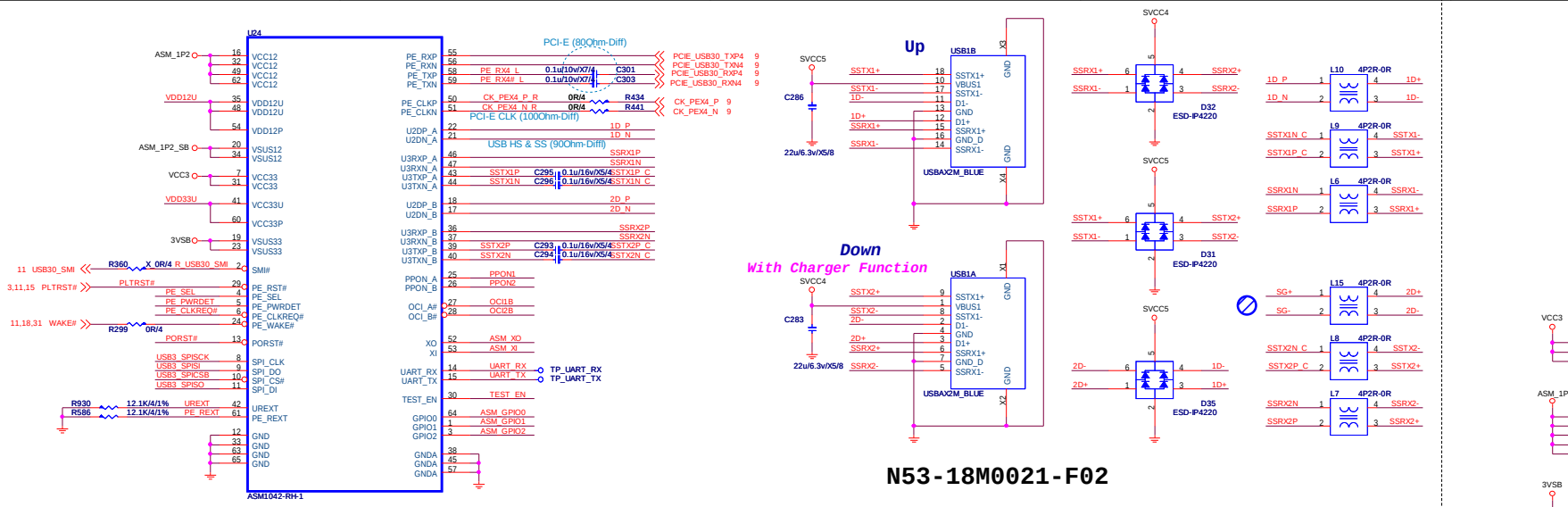
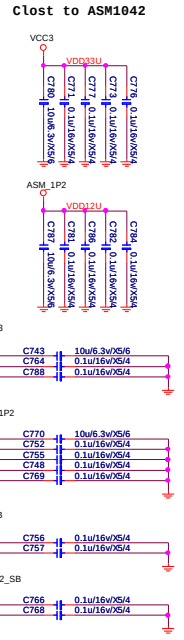
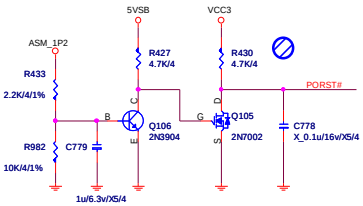
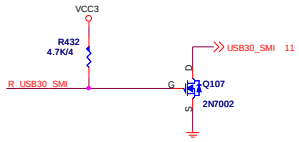


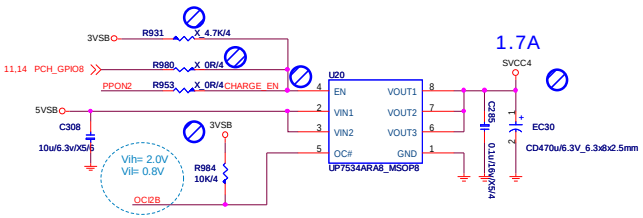
B02-010420C-AD0

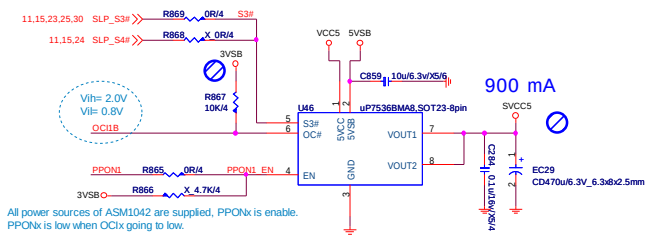
N53-18M0021-F02

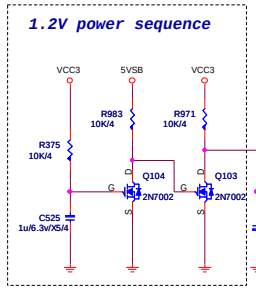


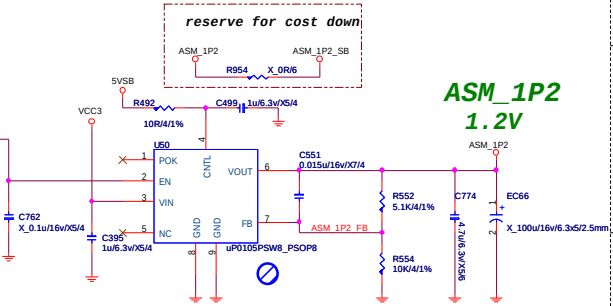




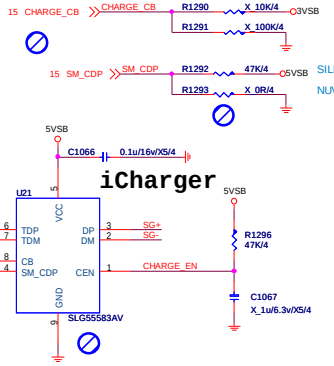


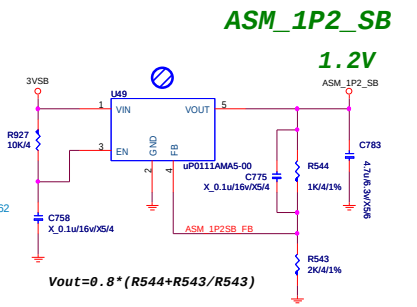






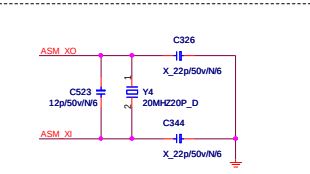
ASM1042 core Power
(ASM_1P2+ASM_1P2_SB < 150mA)

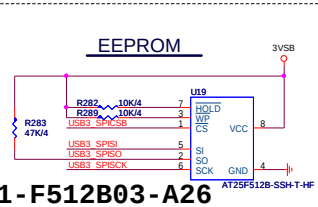




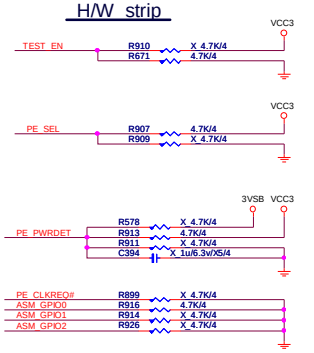
GPIO0	GPIO1	GPIO2	DESCRIPTION
1	1	0	RESERVE MODE
1	1	1	Asynchronous MODE (default)
0	0	X	DEBUG / TEST MODE

GPIO0 / GPIO1 / GPIO2 INTERNAL PULL-HI





M31-F512B03-A26



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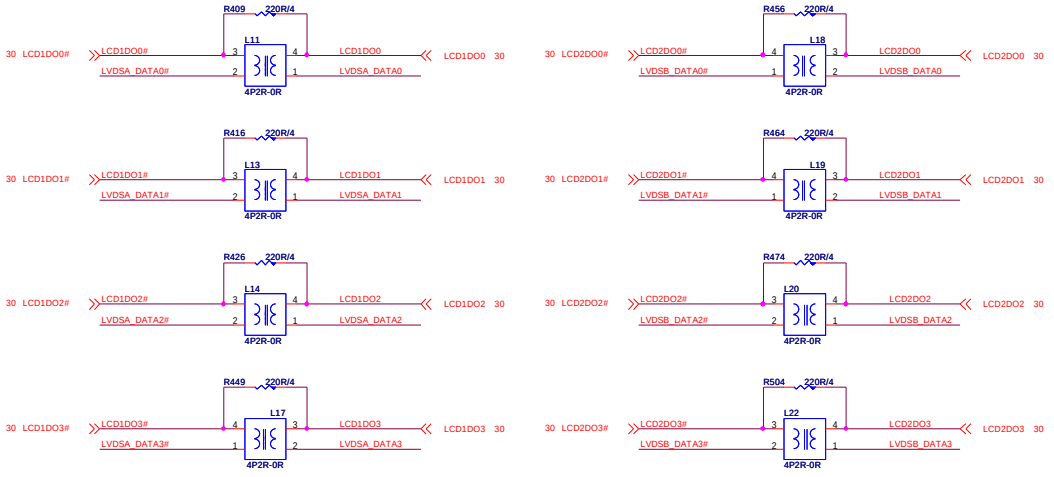
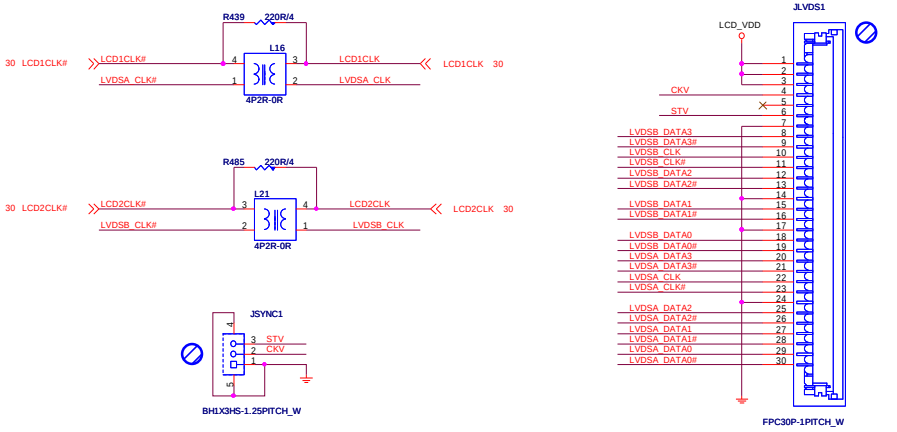
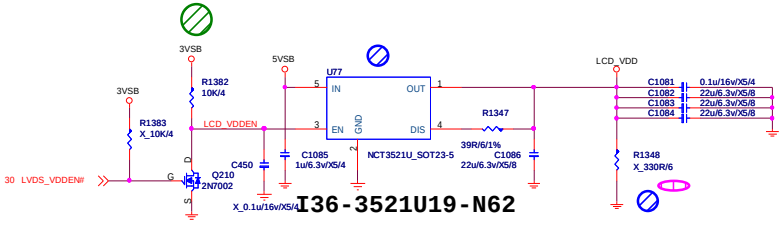




N5A-30F0120-H06



I36-3521U19-N62

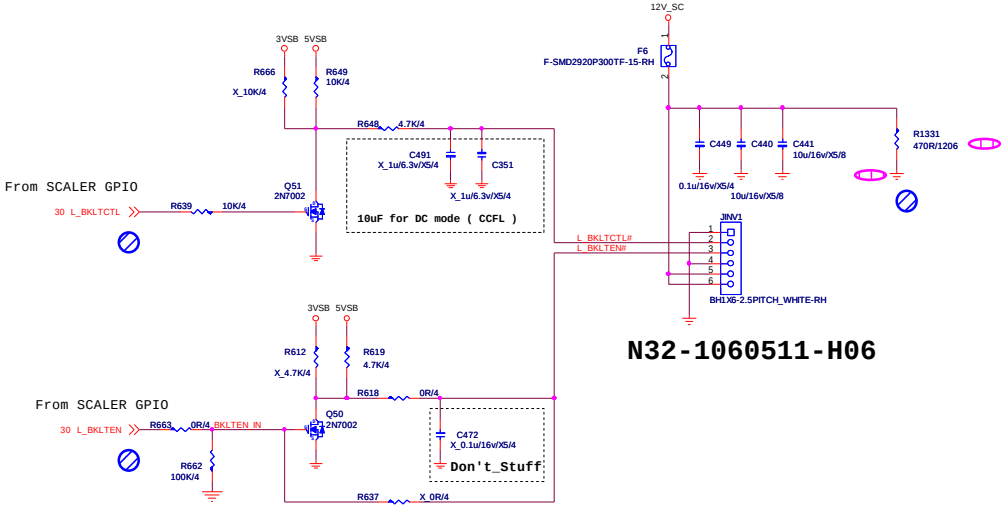
5.26 PCH Display Interfaces

The PCH integrates one Analog, LVDS (mobile only) and three Digital Ports B, C, and D. Each Digital Port can transmit data according to one or more protocols. Digital Port B, C, and D can be configured to drive natively HDMI, DisplayPort, or DVI. Digital Port B also supports Serial Digital Video Out (SDVO) that converts one protocol to another. Digital Port D can be configured to drive natively Embedded DisplayPort (eDP). Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The PCH's Analog Port uses an integrated 340.4 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.

The PCH SDVO port (configured through Digital Port B) is capable of driving a 200 MP/s (Megapixels/second) rate.

Each Digital Port is capable of driving a digital display up to 2560x1600 at 60 Hz using DisplayPort and 1920x1200 at 60 Hz using HDMI, DVI (with reduced blanking).



N32-1060511-H06

MSI	MICRO-STAR INT'L CO.,LTD	
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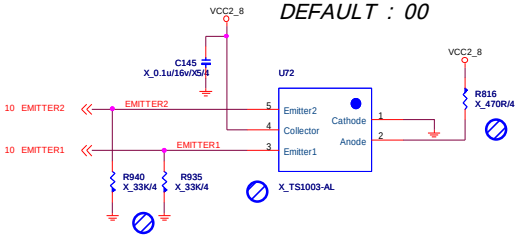
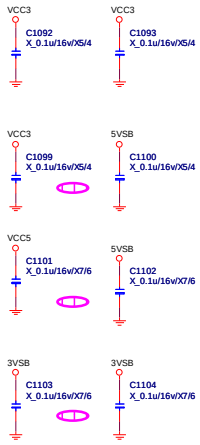
DEFAULT : 00



Detecting Rotation Characteristics

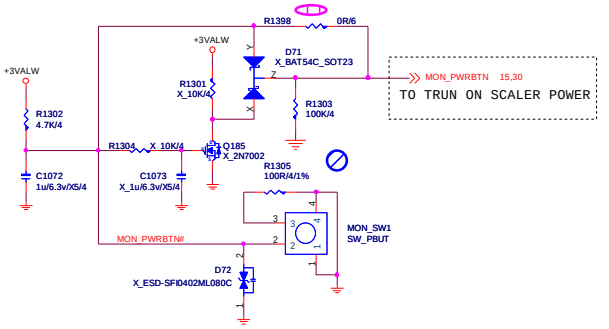
	E1	E2
E2 / LED / E1	0	1
E1 / E2 / LED	0	0
LED / E1 / E2	1	0
LED / E2 / E1	1	1

FOR EMI

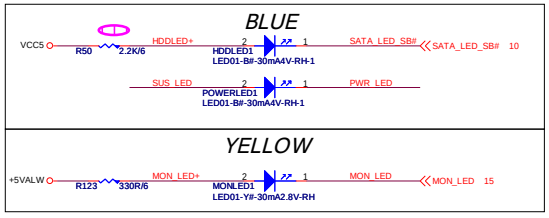


Low pluse wide at least 100 mSec for Scalar.

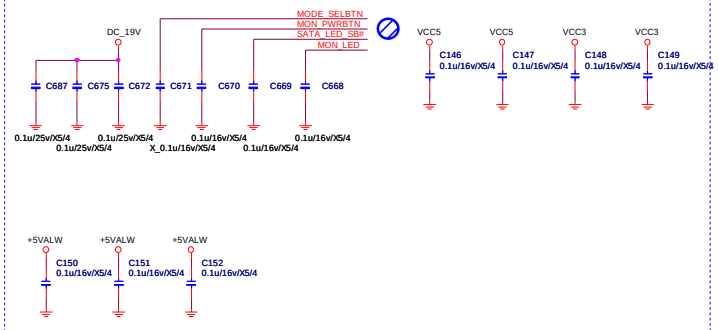
HDMI IN / PC / Monitor OFF BUTTON



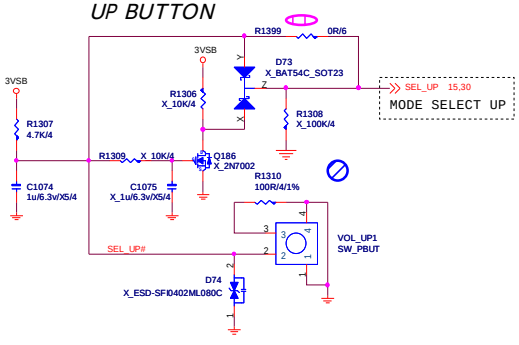
LED



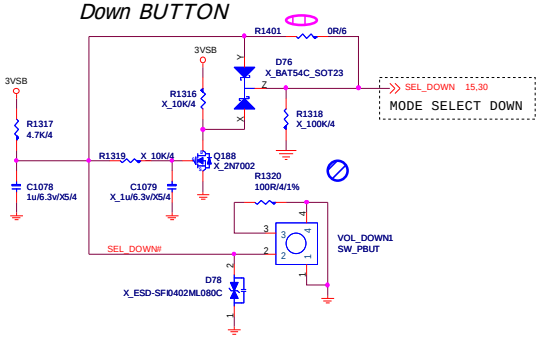
FOR EMI

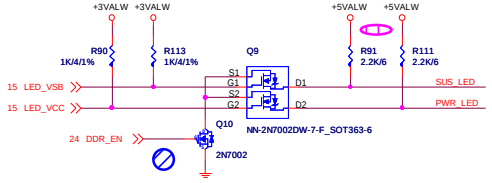


UP BUTTON

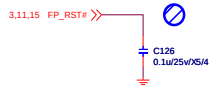


Down BUTTON

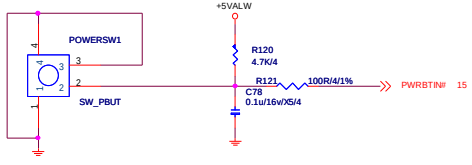




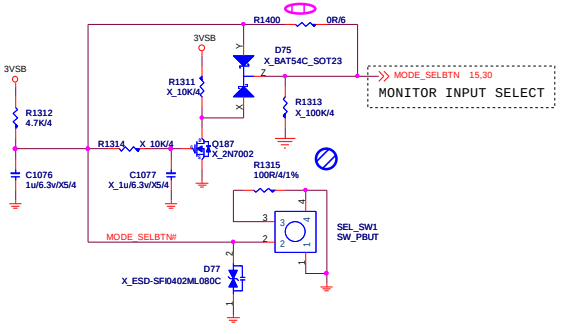
SYSTEM RESET



POWER ON/OFF BUTTON



OSD MODE SELECT BUTTON



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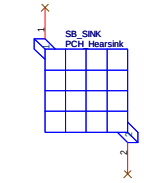
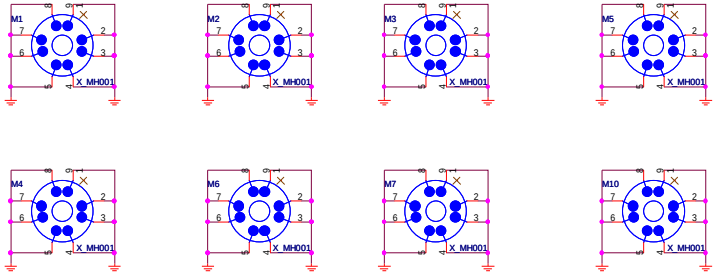
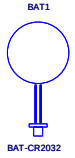
Mounting Holes

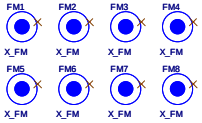


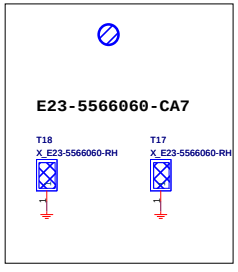
E31-0405500-A87



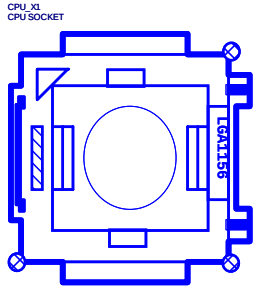


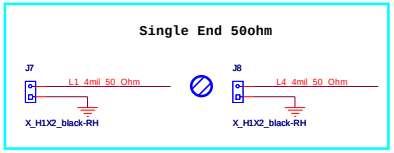
Optical Fiducial Marks-120

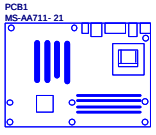




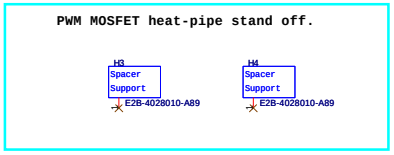
CPU SOCKET

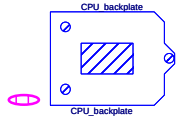






P80-AA71121-E48
P80-AA71121-E55
P80-AA71121-T53





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	MS-AA711	
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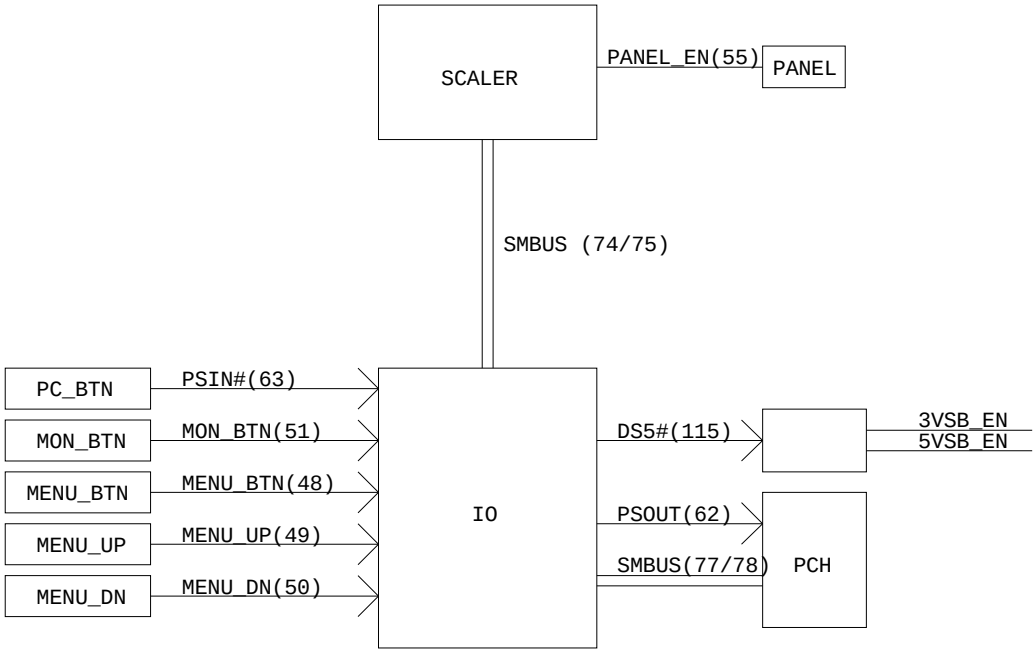

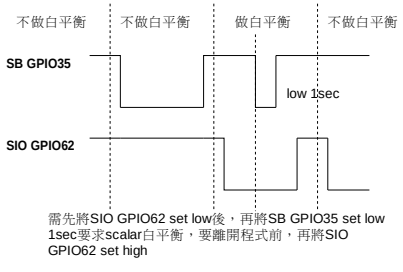

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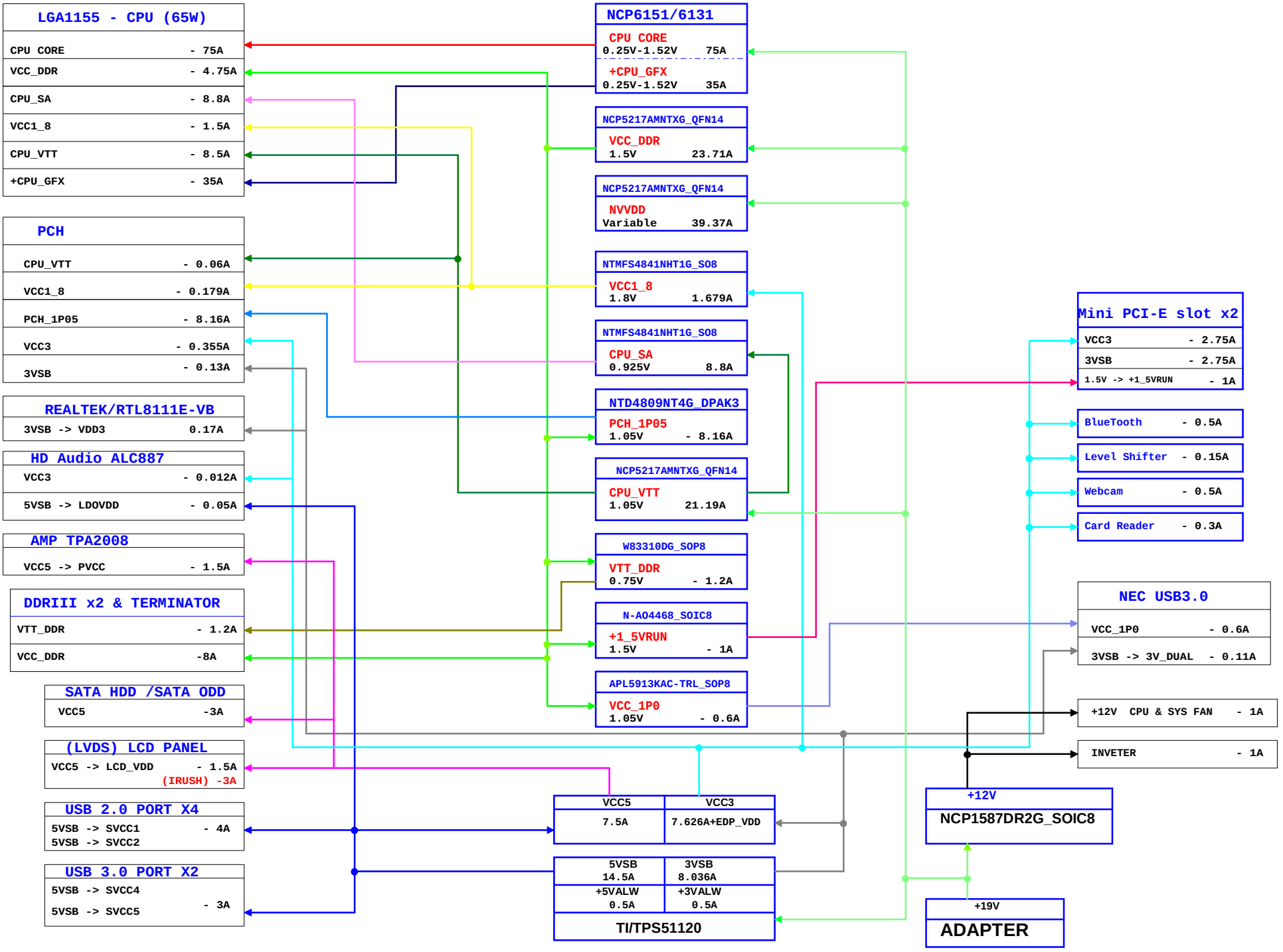

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AIO MS-AA711 Version 2.1 *SCHEMATIC HISTORY*

Modify from MS-AA711 version 1.1

Rev	Date	Page	Description
2.0	20120705		HDMI In and HDMI Out Location swap. HDMI Out level shift from active change to passive. LVDS from VGA change to DDPC, Scalar from 2482 change to 2482D. EC Crystal from DIP change to SMD. ERP Spec. change to 2013. MOSFET from DPAK change to PPAK reduce thermal. EDI-TENSOR change to new version. LVDS connector turn 180 degree. Card Reader from RTS5159 to RTS5139 Card Reader from 6 in 1 change to 3 in 1. Power Connect change new part. Reserved Power meter circuit. Reserved CMOS Power sequence circuit. Add thermal Trip and Throtting circuit. Add automatic clear COMS circuit.
2.1	20120728	03	Change CPU Socket part number for cost down.
	20120728	07	Add temperature sensor circuit; Change SODIMM socket for cost down.
	20120728	08	Change SODIMM socket for cost down.
	20120728	15	U51 from 8M change to 1M for cost down. R1388 add 33 Ohm for EMI request.
	20120728	20	Reserved F9 for Touch.
	20120728	23	Change PCH_1P05 MOSFET (Q66) for cost down.
	20120728	28	Don't stuff power meter component for cost down. Modify DC_Jack footprint.
	20120728	29	Modify Card Reader Socket footprint.
	20120728	30	Add DDPC HPD circuit. Reserved BKLTCTL circuit.
	20120728	31	Change Mini PCIE Slot part number for cost down.
	20120728	32	3VSB_EN and 5VSB_EN reserved C1095, C1096 . Delete R589, R571; Remove EC67. C436 stuff 0.47uf for WebCom issue.
	20120829		1uf / 6.3v from 0603 change to 0402 for cost down. 10uf / 6.3v from 0805 change to 0603 for cost down. 10uf / 16v from 1206 change to 0805 for cost down. 10uf / 25v from 1206 change to 0805 for cost down.
	201200904	08	Power and HDD LED from 330 Ohm change to 2.2K Ohm.
	201200905		Footprint SOT669 change to SOT669_COLAY, for Power team request.

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