Model Name : H510M H

Rev 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B-DDR4
06	CPU_LGA1151-C
07	CPU_LGA1150-D
08	DDR4 CHANNEL A
09	DDR4 CHANNEL B
10	PCH_CLK BUFFER
11	PCH_DMI,USB,PCIE
12	PCH_MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH PWR
15	PCH GND
16	ITE 8686 LPC IO
17	HWM
18	FAN CTRL--SIO
19	BIOS
20	CEC
21	PCI EXPRESS*16 SLOT
22	PCI EXPRESS*1 SLOT
23	SATA Connector
24	M.2 X4 (A)
25	IT8892E (NA)
26	PCI SLOT (NA)
27	ASM1085 POWER (NA)
28	LDO POWER (NA)

SHEET	TITLE
29	ISL95866 PWM-IRON
30	ISL95866 VCORE-IRON
31	ISL95866 VCCGT-IRON
32	VCCSA_VCCIO_VCCPLL
33	RT8237_DDR_BEAD
34	RT8068A_VPP
35	RT8237_PCH-BEAD
36	DISCRETE POWER
37	POWER MAP
38	ATX POWER , A_-PROCHOT
39	KB_MS
40	DVI CONN
41	RTD2168 - DP to VGA - IC
42	RTD2168 - DP to VGA - Conn
43	REALTEK 8111G
44	USB_LAN CONNECTOR-81118
45	Realtek ALC887
46	REAR AUDIO JACK
47	ADUIO LED
48	R_USB30_1
49	R_USB30_2
50	HDMI (MASK)
51	Redriver-R_USB31 (NA)
52	F_USB30
53	F_USB
54	F_PANEL
55	COM, TPM
56	EMI-ESD
	NTC MAP

Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: H510M H | Rev: 1.0

Date: Wednesday, January 06, 2021 | Sheet 1 of 62

Model Name : H410M H

Component value change history

Data	Change Item	Reason
2019/12/12	1. H410M H 改 S2	R01
2019/12/12	1. EVT	9MH410MS2-00-01
2020/02/24	1. 修改模組線路 & note	R10
2020/03/12	1. DVT	9MH410MS2-00-10A
2020/03/17	1. 修改模組線路 & note	R101
2020/03/29	1. PVT	9MH410MS2-00-10E
2020/04/07	1. 修改模組線路 & note	9MH410MS2-00-10F
2020/04/17	1. 採購修改電容用料	9MH410MS2-00-10G
2020/08/27	1. H410M S2 改 H510M S2	R01

Circuit or PCB layout change

DATE	Change Item	Reason

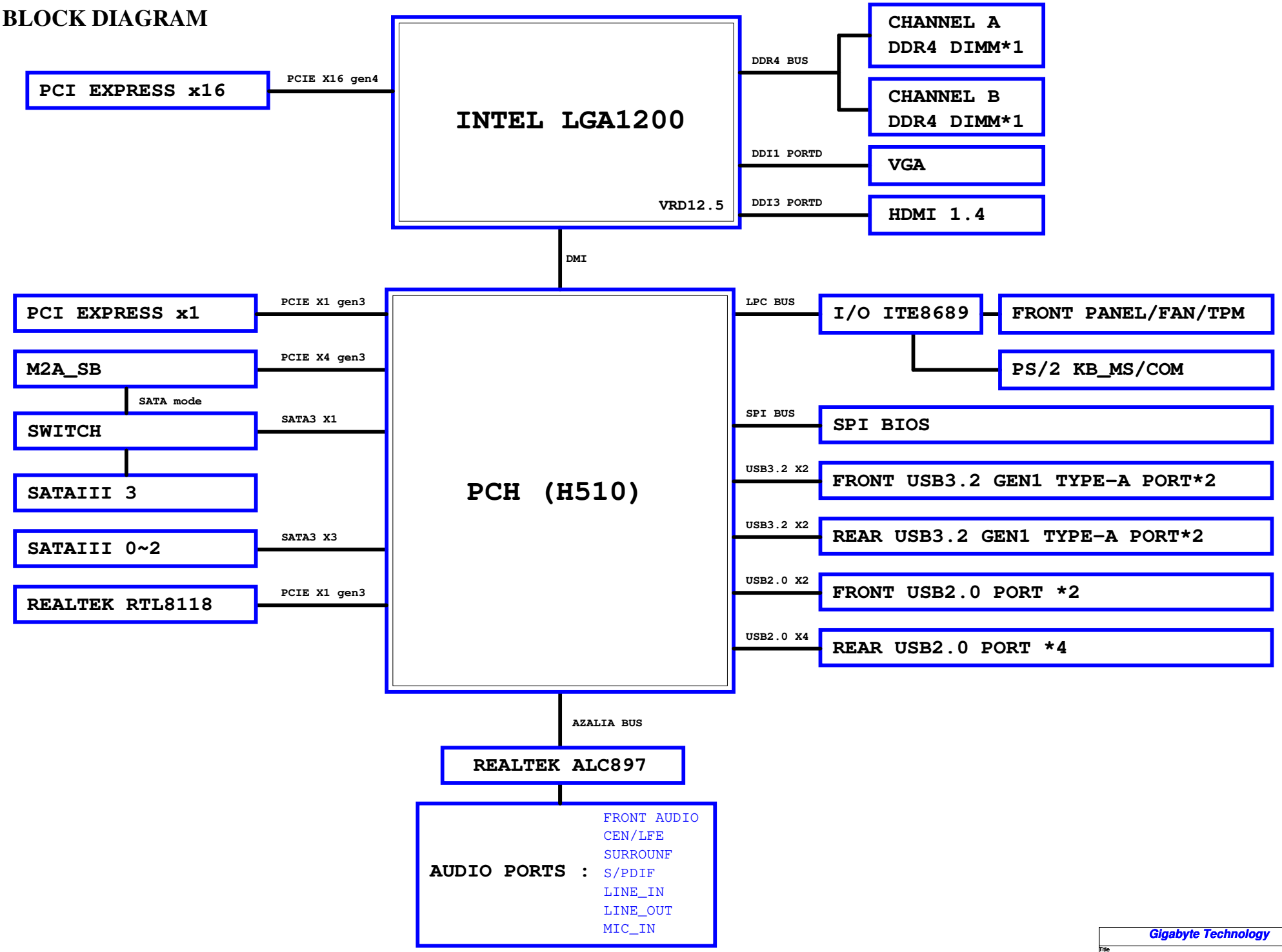
GIGABYTE™

Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: H510M H | Rev: 1.0

Date: Wednesday, January 06, 2021 | Sheet 2 of 62

BLOCK DIAGRAM



Gigabyte Technology		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 3 of 62	

檢查組態調整線路
The CFG signals default value of '1'

CFG[4]: 0=eDP enable / 1=eDP disable
CFG[7]: 1=PEG Train immediately following RESET
0=PEG Wait for BIOS

CFG[13]: 1=VCCSA Fixed Mode / 0=SVID Mode

LGA1200E
CML_S_IP
T=190922B
5 OF 13
CPU-SK/1200/S/GF

LGA1200C
CML_S_IP
T=190922B
3 OF 13
CPU-SK/1200/S/GF

LGA1200D
CML_S_IP
T=190922B
4 OF 13
CPU-SK/1200/S/GF

DP-VGA
DVI
HDMI

* CPU_ID
1: RKL -->VCCIO=1.0V
0: CML -->VCCIO=0V

若有不上CODEC出貨的可能，請預留CLK and SDO對地電阻。

B560/H510
REMOVE DMI4~7

Gigabyte Technology	
Title	CPU LGA1200-A
Size: Custom	Document Number: H510M H
Rev	1.0
Date: Wednesday, January 06, 2021	Sheet 4 of 62

LGA1200A

CML_S_IP

T=190922B

MDA0	AE39	DDR0_DQ[0]		AU24	M_DCLKA0	M_DCLKA0	8
MDA1	AE38	DDR0_DQ[1]		AV24	M_-DCLKA0	M_-DCLKA0	8
MDA2	AH39	DDR0_DQ[2]		AY23	M_DCLKA1	M_DCLKA1	8
MDA3	AH38	DDR0_DQ[3]		AW23	M_-DCLKA1	M_-DCLKA1	8
MDA4	AF40	DDR0_DQ[4]		AT19			
MDA5	AE40	DDR0_DQ[5]		AU19			
MDA6	AH40	DDR0_DQ[6]		AY18			
MDA7	AG40	DDR0_DQ[7]		AW18			
MDA8	AK39	DDR0_DQ[8]					
MDA9	AK40	DDR0_DQ[9]	DDR0_CKP[0]	AY31	CKEA0	CKEA0	8
MDA10	AN39	DDR0_DQ[10]	DDR0_CKN[0]	AW31	CKEA1	CKEA1	8
MDA11	AM40	DDR0_DQ[11]	DDR0_CKP[1]	AV30			
MDA12	AL40	DDR0_DQ[12]	DDR0_CKN[1]	AV31			
MDA13	AK38	DDR0_DQ[13]	DDR0_CKP[2]				
MDA14	AN40	DDR0_DQ[14]	DDR0_CKN[2]	AY15	M_-CSA0	M_-CSA0	8
MDA15	AN38	DDR0_DQ[15]	DDR0_CKP[3]	AY13	M_-CSA1	M_-CSA1	8
MDA16	AR39	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_CKN[3]	AV15			
MDA17	AR40	DDR0_DQ[17]/DDR0_DQ[33]		AV13			
MDA18	AV39	DDR0_DQ[18]/DDR0_DQ[34]					
MDA19	AU40	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_CS#[0]	AY14	MODT_A0	MODT_A0	8
MDA20	AR38	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_CS#[1]	AV14	MODT_A1	MODT_A1	8
MDA21	AT40	DDR0_DQ[21]/DDR0_DQ[37]	DDR0_CS#[2]	AU14			
MDA22	AW38	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_CS#[3]	AT14			
MDA23	AV38	DDR0_DQ[23]/DDR0_DQ[39]					
MDA24	AV36	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_ODT[0]	AY16	SBAA0	SBAA0	8
MDA25	AY36	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_ODT[1]	AW17	SBAA1	SBAA1	8
MDA26	AV33	DDR0_DQ[26]/DDR0_DQ[42]	DDR0_ODT[2]				
MDA27	AY34	DDR0_DQ[27]/DDR0_DQ[43]	DDR0_ODT[3]	AY29	BG_A0	BG_A0	8
MDA28	AY35	DDR0_DQ[28]/DDR0_DQ[44]		AW29	BG_A1	BG_A1	8
MDA29	AW36	DDR0_DQ[29]/DDR0_DQ[45]					
MDA30	AY33	DDR0_DQ[30]/DDR0_DQ[46]					
MDA31	AW33	DDR0_DQ[31]/DDR0_DQ[47]		AV16	MAAA16		
MDA32	AW11	DDR0_DQ[32]/DDR1_DQ[0]		AW16	MAAA14		
MDA33	AV11	DDR0_DQ[33]/DDR1_DQ[1]		AU16	MAAA15		
MDA34	AY7	DDR0_DQ[34]/DDR1_DQ[2]					
MDA35	AY8	DDR0_DQ[35]/DDR1_DQ[3]		AU18	MAAA0		
MDA36	AW9	DDR0_DQ[36]/DDR1_DQ[4]		AY25	MAAA1		
MDA37	AW10	DDR0_DQ[37]/DDR1_DQ[5]		AY24	MAAA2		
MDA38	AV7	DDR0_DQ[38]/DDR1_DQ[6]		AW25	MAAA3		
MDA39	AW7	DDR0_DQ[39]/DDR1_DQ[7]		AV25	MAAA4		
MDA40	AW5	DDR0_DQ[40]/DDR1_DQ[8]		AY26	MAAA5		
MDA41	AY5	DDR0_DQ[41]/DDR1_DQ[9]		AV26	MAAA6		
MDA42	AW2	DDR0_DQ[42]/DDR1_DQ[10]		AY27	MAAA7		
MDA43	AW3	DDR0_DQ[43]/DDR1_DQ[11]		AW27	MAAA8		
MDA44	AY4	DDR0_DQ[44]/DDR1_DQ[12]		AY28	MAAA9		
MDA45	AV5	DDR0_DQ[45]/DDR1_DQ[13]		AU17	MAAA10		
MDA46	AV1	DDR0_DQ[46]/DDR1_DQ[14]		AV27	MAAA11		
MDA47	AV2	DDR0_DQ[47]/DDR1_DQ[15]		AV28	MAAA12		
MDA48	AT1	DDR0_DQ[48]/DDR1_DQ[32]		AW14	MAAA13		
MDA49	AN1	DDR0_DQ[49]/DDR1_DQ[33]					
MDA50	AT3	DDR0_DQ[50]/DDR1_DQ[34]					
MDA51	AP1	DDR0_DQ[51]/DDR1_DQ[35]		AY30	M_-ACT_A	M_-ACT_A	8
MDA52	AT2	DDR0_DQ[52]/DDR1_DQ[36]		AV18	DDR0_PAR	M_DDR_PARA	8
MDA53	AN3	DDR0_DQ[53]/DDR1_DQ[37]		AY29	DDR0_ALERT#	M_-ALERT_A	8
MDA54	AR1	DDR0_DQ[54]/DDR1_DQ[38]					
MDA55	AN2	DDR0_DQ[55]/DDR1_DQ[39]					
MDA56	AL2	DDR0_DQ[56]/DDR1_DQ[40]					
MDA57	AH1	DDR0_DQ[57]/DDR1_DQ[41]	DDR0_DQSP[7]/DDR1_DQSP[5]	AJ3	M_DQSA7		
MDA58	AL3	DDR0_DQ[58]/DDR1_DQ[42]	DDR0_DQSN[7]/DDR1_DQSN[5]	AK3	M_-DQSA7		
MDA59	AJ1	DDR0_DQ[59]/DDR1_DQ[43]	DDR0_DQSP[6]/DDR1_DQSP[4]	AP3	M_DQSA6		
MDA60	AH3	DDR0_DQ[60]/DDR1_DQ[44]	DDR0_DQSN[6]/DDR1_DQSN[4]	AR3	M_-DQSA6		
MDA61	AL1	DDR0_DQ[61]/DDR1_DQ[45]	DDR0_DQSP[5]/DDR1_DQSP[1]	AV3	M_DQSA5		
MDA62	AH2	DDR0_DQ[62]/DDR1_DQ[46]	DDR0_DQSN[5]/DDR1_DQSN[1]	AV4	M_-DQSA5		
MDA63	AK1	DDR0_DQ[63]/DDR1_DQ[47]	DDR0_DQSP[4]/DDR1_DQSP[0]	AV8	M_DQSA4		
			DDR0_DQSN[4]/DDR1_DQSN[0]	AV9	M_-DQSA4		
			DDR0_DQSP[3]/DDR0_DQSP[5]	AV34	M_DQSA3		
			DDR0_DQSN[3]/DDR0_DQSN[5]	AV35	M_-DQSA3		
			DDR0_DQSP[2]/DDR0_DQSP[4]	AU38	M_DQSA2		
			DDR0_DQSN[2]/DDR0_DQSN[4]	AT38	M_-DQSA2		
			DDR0_DQSP[1]	AM38	M_DQSA1		
			DDR0_DQSN[1]	AL38	M_-DQSA1		
			DDR0_DQSP[0]	AG38	M_DQSA0		
			DDR0_DQSN[0]	AF38	M_-DQSA0		
AK30		DDR0_ECC[7]					
AM32		DDR0_ECC[6]					
AJ32		DDR0_ECC[5]					
AK32		DDR0_ECC[4]					
AL32		DDR0_ECC[3]					
AM31		DDR0_ECC[2]					
AM30		DDR0_ECC[1]					
AL30		DDR0_ECC[0]					
AC38		DDR_VREF_CA_1	DDR0_DQSP[8]	AJ30			
AG40		DDR_VREF_CA_0	DDR0_DQSN[8]	AJ31			

8 VREF_CA0 ← VREF_CA0

DDR CHANNEL A

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CPU-SK/1200/S/GF

LGA1200B

CML_S_IP

T=190922B

MDB0	AD34	DDR1_DQ[0]/DDR0_DQ[16]		AT23	M_DCLKB0	M_DCLKB0	9
MDB1	AD35	DDR1_DQ[1]/DDR0_DQ[17]		AU23	M_-DCLKB0	M_-DCLKB0	9
MDB2	AE36	DDR1_DQ[2]/DDR0_DQ[18]		AV22	M_DCLKB1	M_DCLKB1	9
MDB3	AF36	DDR1_DQ[3]/DDR0_DQ[19]		AU22	M_-DCLKB1	M_-DCLKB1	9
MDB4	AG35	DDR1_DQ[4]/DDR0_DQ[20]		AT21			
MDB5	AG34	DDR1_DQ[5]/DDR0_DQ[21]		AU21			
MDB6	AD36	DDR1_DQ[6]/DDR0_DQ[22]		AU20			
MDB7	AG36	DDR1_DQ[7]/DDR0_DQ[23]		AV20			
MDB8	AJ36	DDR1_DQ[8]/DDR0_DQ[24]					
MDB9	AJ35	DDR1_DQ[9]/DDR0_DQ[25]	DDR1_CKP[0]	AT25	CKEB0	CKEB0	9
MDB10	AL36	DDR1_DQ[10]/DDR0_DQ[26]	DDR1_CKN[0]	AR26	CKEB1	CKEB1	9
MDB11	AM35	DDR1_DQ[11]/DDR0_DQ[27]	DDR1_CKP[1]	AT26			
MDB12	AK36	DDR1_DQ[12]/DDR0_DQ[28]	DDR1_CKN[1]	AP26			
MDB13	AJ34	DDR1_DQ[13]/DDR0_DQ[29]	DDR1_CKP[2]				
MDB14	AM36	DDR1_DQ[14]/DDR0_DQ[30]	DDR1_CKN[2]	AN17	M_-CSB0	M_-CSB0	9
MDB15	AM34	DDR1_DQ[15]/DDR0_DQ[31]	DDR1_CKP[3]	AN15	M_-CSB1	M_-CSB1	9
MDB16	AT36	DDR1_DQ[16]/DDR0_DQ[48]	DDR1_CKN[3]	AR16			
MDB17	AP36	DDR1_DQ[17]/DDR0_DQ[49]		AM15			
MDB18	AT34	DDR1_DQ[18]/DDR0_DQ[50]					
MDB19	AP33	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_CS#[0]	AM17	MODT_B0	MODT_B0	9
MDB20	AR36	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_CS#[1]	AP14	MODT_B1	MODT_B1	9
MDB21	AT35	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_CS#[2]	AM16			
MDB22	AR33	DDR1_DQ[22]/DDR0_DQ[54]	DDR1_CS#[3]	AM14			
MDB23	AT33	DDR1_DQ[23]/DDR0_DQ[55]					
MDB24	AP31	DDR1_DQ[24]/DDR0_DQ[56]	DDR1_ODT[0]	AP18	SBAB0	SBAB0	9
MDB25	AT31	DDR1_DQ[25]/DDR0_DQ[57]	DDR1_ODT[1]	AN19	SBAB1	SBAB1	9
MDB26	AT29	DDR1_DQ[26]/DDR0_DQ[58]	DDR1_ODT[2]				
MDB27	AP28	DDR1_DQ[27]/DDR0_DQ[59]	DDR1_ODT[3]	AM23	BG_B0	BG_B0	9
MDB28	AR31	DDR1_DQ[28]/DDR0_DQ[60]		AM22	BG_B1	BG_B1	9
MDB29	AT30	DDR1_DQ[29]/DDR0_DQ[61]					
MDB30	AR28	DDR1_DQ[30]/DDR0_DQ[62]		AN18	MAAB16		
MDB31	AT28	DDR1_DQ[31]/DDR0_DQ[63]		AP17	MAAB14		
MDB32	AT12	DDR1_DQ[32]/DDR0_DQ[16]		AP16	MAAB15		
MDB33	AR12	DDR1_DQ[33]/DDR0_DQ[17]					
MDB34	AT10	DDR1_DQ[34]/DDR0_DQ[18]		AP19	MAAB0		
MDB35	AR10	DDR1_DQ[35]/DDR0_DQ[19]		AP20	MAAB1		
MDB36	AP12	DDR1_DQ[36]/DDR0_DQ[20]		AR20	MAAB2		
MDB37	AT11	DDR1_DQ[37]/DDR0_DQ[21]		AM20	MAAB3		
MDB38	AP10	DDR1_DQ[38]/DDR0_DQ[22]		AP21	MAAB4		
MDB39	AN10	DDR1_DQ[39]/DDR0_DQ[23]		AN21	MAAB5		
MDB40	AR8	DDR1_DQ[40]/DDR0_DQ[24]		AR22	MAAB6		
MDB41	AT8	DDR1_DQ[41]/DDR0_DQ[25]		AM21	MAAB7		
MDB42	AT5	DDR1_DQ[42]/DDR0_DQ[26]		AP22	MAAB8		
MDB43	AT6	DDR1_DQ[43]/DDR0_DQ[27]		AN23	MAAB9		
MDB44	AP8	DDR1_DQ[44]/DDR0_DQ[28]		AR18	MAAB10		
MDB45	AT7	DDR1_DQ[45]/DDR0_DQ[29]		AP23	MAAB11		
MDB46	AP5	DDR1_DQ[46]/DDR0_DQ[30]		AR24	MAAB12		
MDB47	AR5	DDR1_DQ[47]/DDR0_DQ[31]		AP15	MAAB13		
MDB48	AM8	DDR1_DQ[48]					
MDB49	AM7	DDR1_DQ[49]					
MDB50	AK6	DDR1_DQ[50]		AP25	M_-ACT_B	M_-ACT_B	9
MDB51	AM5	DDR1_DQ[51]	DDR1_PAR	AM19	M_DDR_PARB	M_DDR_PARB	9
MDB52	AM6	DDR1_DQ[52]	DDR1_ALERT#	AP24	M_-ALERT_B	M_-ALERT_B	9
MDB53	AK7	DDR1_DQ[53]					
MDB54	AK5	DDR1_DQ[54]					
MDB55	AL5	DDR1_DQ[55]					
MDB56	AF7	DDR1_DQ[56]	DDR1_DQSP[7]	AF8	M_DQSB7		
MDB57	AH8	DDR1_DQ[57]	DDR1_DQSN[7]	AG8	M_-DQSB7		
MDB58	AG5	DDR1_DQ[58]	DDR1_DQSP[6]	AK8	M_DQSB6		
MDB59	AF6	DDR1_DQ[59]	DDR1_DQSN[6]	AL8	M_-DQSB6		
MDB60	AH6	DDR1_DQ[60]	DDR1_DQSP[5]/DDR1_DQSP[3]	AP6	M_DQSB5		
MDB61	AH7	DDR1_DQ[61]	DDR1_DQSN[5]/DDR1_DQSN[3]	AP7	M_-DQSB5		
MDB62	AF5	DDR1_DQ[62]	DDR1_DQSP[4]/DDR1_DQSP[2]	AN11	M_DQSB4		
MDB63	AH5	DDR1_DQ[63]	DDR1_DQSN[4]/DDR1_DQSN[2]	AN12	M_-DQSB4		
			DDR1_DQSP[3]/DDR0_DQSP[7]	AP29	M_DQSB3		
			DDR1_DQSN[3]/DDR0_DQSN[7]	AP30	M_-DQSB3		
			DDR1_DQSP[2]/DDR0_DQSP[6]	AP34	M_DQSB2		
			DDR1_DQSN[2]/DDR0_DQSN[6]	AP35	M_-DQSB2		
			DDR1_DQSP[1]/DDR0_DQSP[3]	AL34	M_DQSB1		
			DDR1_DQSN[1]/DDR0_DQSN[3]	AK34	M_-DQSB1		
			DDR1_DQSP[0]/DDR0_DQSP[2]	AF34	M_DQSB0		
			DDR1_DQSN[0]/DDR0_DQSN[2]	AE34	M_-DQSB0		
AM26		DDR1_ECC[7]					
AM27		DDR1_ECC[6]					
AL28		DDR1_ECC[5]					
AK28		DDR1_ECC[4]					
AM28		DDR1_ECC[3]					
AL26		DDR1_ECC[2]					
AK26		DDR1_ECC[1]					
AJ28		DDR1_ECC[0]					
AB40		DDR_VREF_CA_3	DDR1_DQSP[8]	AJ27			
AC39		DDR_VREF_CA_2	DDR1_DQSN[8]	AJ26			

9 VREF_CA2 ← VREF_CA2

DDR CHANNEL B

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CPU-SK/1200/S/GF

8 MDA[0..63] ↔ MDA[0..63]

9 MDB[0..63] ↔ MDB[0..63]

8 M_DQSA[0..7] ↔ M_DQSA[0..7]

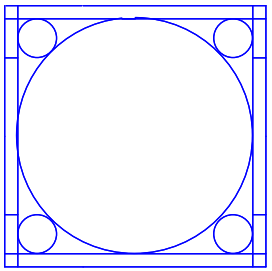
8 M_-DQSA[0..7] ↔ M_-DQSA[0..7]

8 MAAA[0..16] ↔ MAAA[0..16]

9 MAAB[0..16] ↔ MAAB[0..16]

9 M_DQSB[0..7] ↔ M_DQSB[0..7]

9 M_-DQSB[0..7] ↔ M_-DQSB[0..7]



黑色cover

LGA1200

ILM_BP_CR/115X/BKNI/[12KRC-SF0001-83R_12KRC-SF0001-84R]

Gigabyte Technology

Title: CPU LGA1200-B

Size: Custom | Document Number: H510M H | Rev: 1.0

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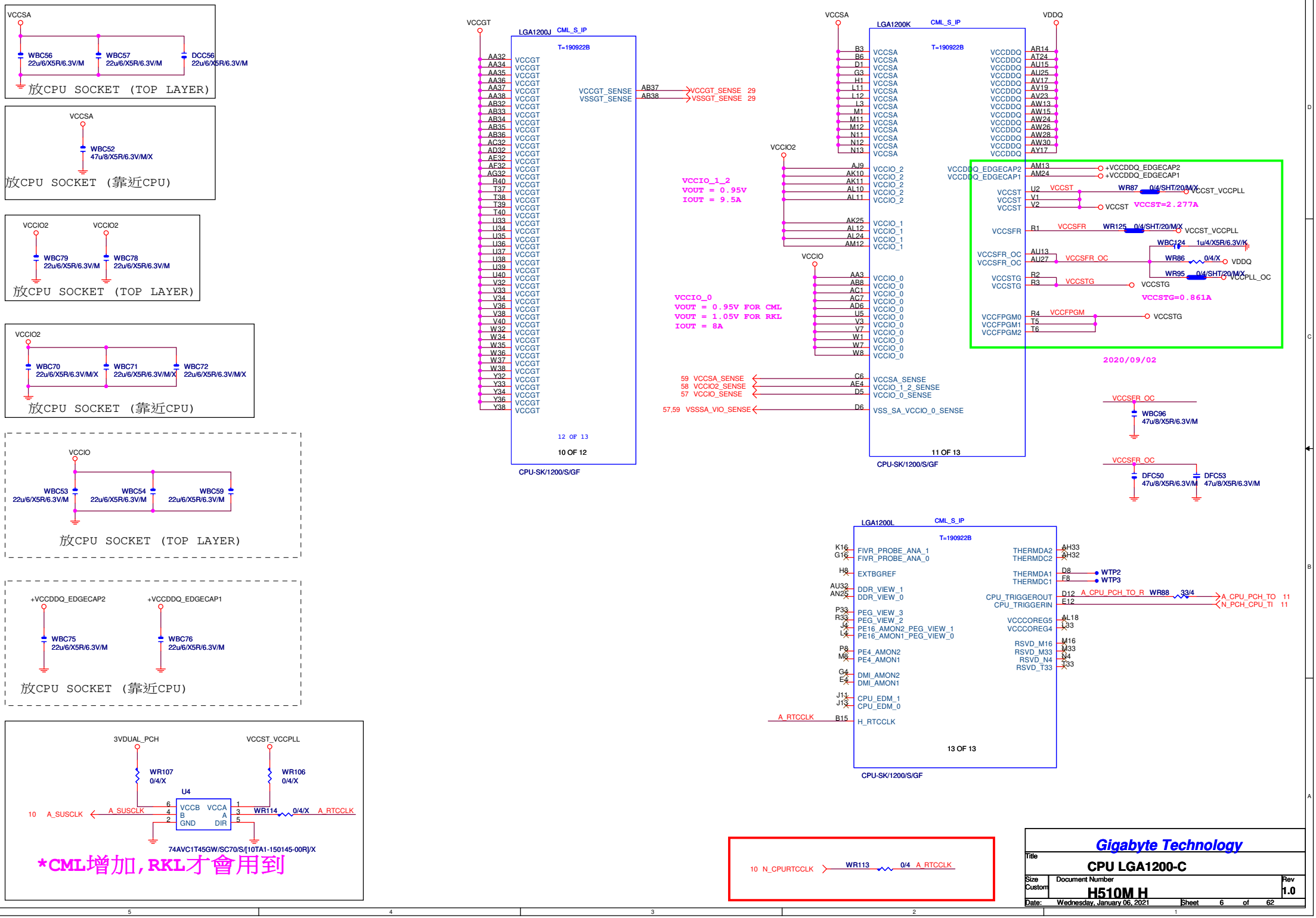
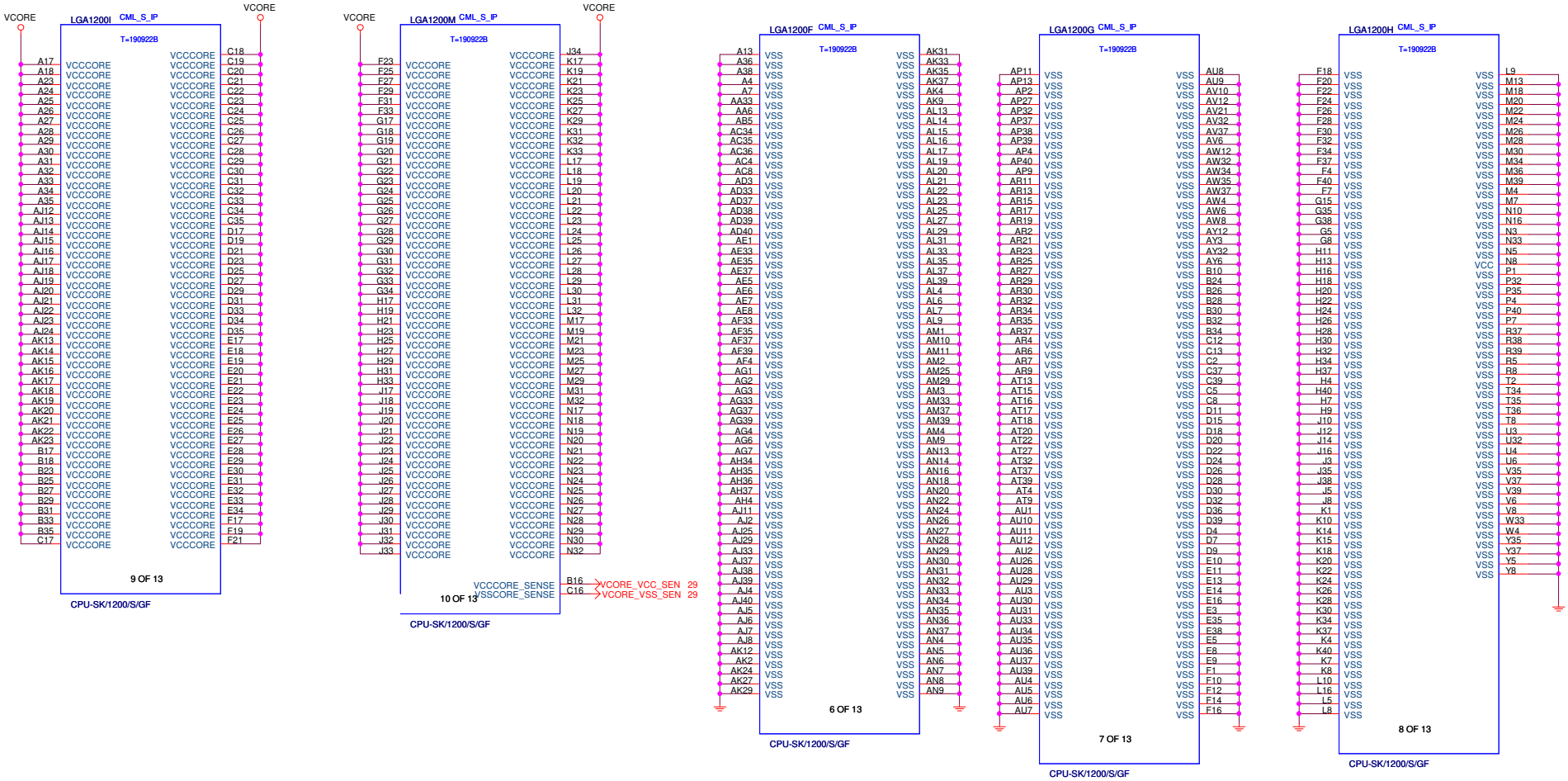
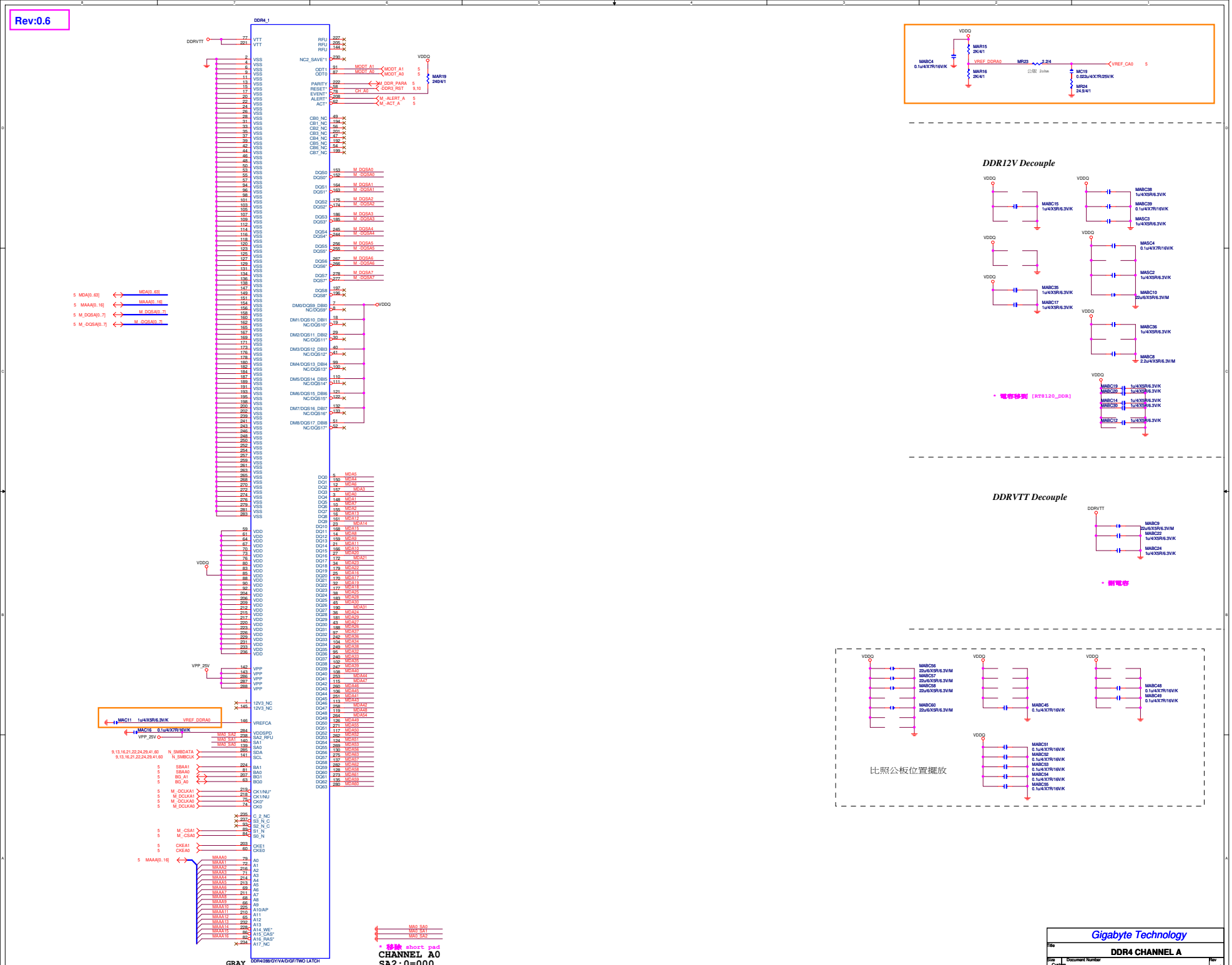

VCCSA
WBC56 22u/6/X5R/6.3V/M
WBC57 22u/6/X5R/6.3V/M
DCC56 22u/6/X5R/6.3V/M
放CPU SOCKET (TOP LAYER)
VCCSA
WBC52 47u/8/X5R/6.3V/M/X
放CPU SOCKET (靠近CPU)
VCCIO2
VCCIO2
WBC79 22u/6/X5R/6.3V/M
WBC78 22u/6/X5R/6.3V/M
放CPU SOCKET (TOP LAYER)
VCCIO2
WBC70 22u/6/X5R/6.3V/M/X
WBC71 22u/6/X5R/6.3V/M/X
WBC72 22u/6/X5R/6.3V/M/X
放CPU SOCKET (靠近CPU)
VCCIO
WBC53 22u/6/X5R/6.3V/M
WBC54 22u/6/X5R/6.3V/M
WBC59 22u/6/X5R/6.3V/M
放CPU SOCKET (TOP LAYER)
+VCCDDQ_EDGECAP2
+VCCDDQ_EDGECAP1
WBC75 22u/6/X5R/6.3V/M
WBC76 22u/6/X5R/6.3V/M
放CPU SOCKET (靠近CPU)
3VDUAL_PCH
VCCST_VCCPLL
WR107 0/4/X
WR106 0/4/X
U4
10 A_SUSCLK
A_SUSCLK
VCCB
B
GND
VCCA
A
DIR
WR114 0/4/X A_RTCCLK
74AVC1T45GW/SC70/S/[10TA1-150145-00R]/X
*CML增加,RKL才會用到
VCCGT
LGA1200J CML_S_IP
T=190922B
AA32 AA34 AA35 AA36 AA37 AA38 AB32 AB33 AB34 AB35 AB36 AC32 AD32 AE32 AF32 AG32 R40 T37 T38 T39 T40 U33 U34 U35 U36 U37 U38 U39 U40 V32 V33 V34 V36 V38 V40 W32 W34 W35 W36 W37 W38 Y32 Y33 Y34 Y36 Y38
VCCGT
VCCGT_SENSE AB37
VSSGT_SENSE AB38
VCCGT_SENSE 29
VSSGT_SENSE 29
12 OF 13
10 OF 12
CPU-SK/1200/S/GF
VCCSA
LGA1200K CML_S_IP
T=190922B
B3 B6 D1 G3 H1 L11 L12 L3 M1 M11 M12 N11 N12 N13
VCCSA
VCCDDQ
AR14 AT24 AU15 AU25 AV17 AV19 AV23 AW13 AW15 AW24 AW26 AW28 AW30 AY17
VDDQ
VCCIO2
VCCIO_1_2
VOUT = 0.95V
IOUT = 9.5A
AJ9 AK10 AK11 AL10 AL11
VCCIO_2
AK25 AL12 AL24 AM12
VCCIO_1
VCCIO
VCCIO_0
VOUT = 0.95V FOR CML
VOUT = 1.05V FOR RKL
IOUT = 8A
AA3 AB8 AC1 AC7 AD6 U5 V3 V7 W1 W7 W8
VCCIO_0
59 VCCSA_SENSE C6
58 VCCIO2_SENSE AE4
57 VCCIO_SENSE D5
57,59 VSSSA_VIO_SENSE D6
VCCSA_SENSE
VCCIO_1_2_SENSE
VCCIO_0_SENSE
VSS_SA_VCCIO_0_SENSE
VCCDDQ_EDGECAP2 AM13
VCCDDQ_EDGECAP1 AM24
+VCCDDQ_EDGECAP2
+VCCDDQ_EDGECAP1
VCCST U2 V1 V2
VCCST
WR87 0/4/SHT/20/M/X
VCCST_VCCPLL
VCCST=2.277A
VCCSFR R1
VCCSFR
WR125 0/4/SHT/20/M/X
VCCST_VCCPLL
WBC124 1u/4/X5R/6.3V/K
VCCSFR_OC AU13 AU27
VCCSFR_OC
WR86 0/4/X
VDDQ
WR95 0/4/SHT/20/M/X
VCCPLL_OC
VCCSTG R2 R3
VCCSTG
VCCSTG
VCCSTG=0.861A
VCCFPGM0 R4
VCCFPGM1 T5
VCCFPGM2 T6
VCCFPGM
VCCSTG
11 OF 13
CPU-SK/1200/S/GF
2020/09/02
VCCSFR_OC
WBC96 47u/8/X5R/6.3V/M
VCCSFR_OC
DFC50 47u/8/X5R/6.3V/M
DFC53 47u/8/X5R/6.3V/M
LGA1200L CML_S_IP
T=190922B
K16 G16 H8 AU32 AN25 P33 R33 J4 L4 P8 M8 G4 E4 J11 J13 B15
FIVR_PROBE_ANA_1
FIVR_PROBE_ANA_0
EXTBGREF
DDR_VIEW_1
DDR_VIEW_0
PEG_VIEW_3
PEG_VIEW_2
PE16_AMON2_PEG_VIEW_1
PE16_AMON1_PEG_VIEW_0
PE4_AMON2
PE4_AMON1
DMI_AMON2
DMI_AMON1
CPU_EDM_1
CPU_EDM_0
H_RTCCLK
A_RTCCLK
THERMDA2 AH33
THERMDC2 AH32
THERMDA1
THERMDC1
D8 WTP2
F8 WTP3
CPU_TRIGGEROUT D12
CPU_TRIGGERIN E12
A_CPU_PCH_TO_R WR88 33/4
A_CPU_PCH_TO 11
N_PCH_CPU_TI 11
VCCCOREG5 AL18
VCCCOREG4 L33
RSVD_M16 M16
RSVD_M33 M33
RSVD_N4 N4
RSVD_T33 T33
13 OF 13
CPU-SK/1200/S/GF
10 N_CPURTCCLK
WR113 0/4 A_RTCCLK
Gigabyte Technology
Title
CPU LGA1200-C
Size Custom
Document Number
H510M H
Rev 1.0
Date: Wednesday, January 06, 2021
Sheet 6 of 62



Gigabyte Technology		
Title: CPU LGA1200-D		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 7 of 62	

Rev:0.6

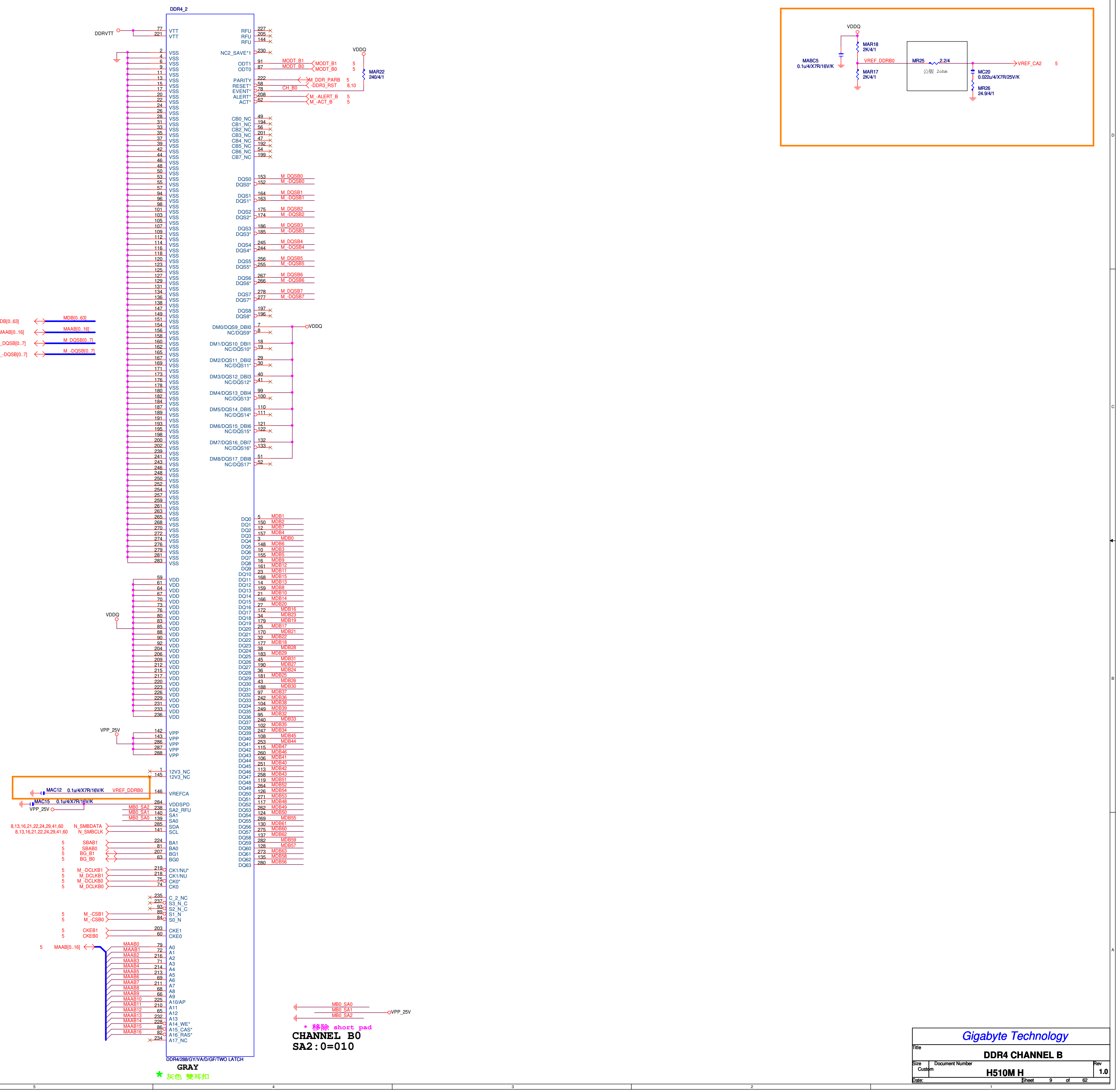


DDR12V Decouple

DDRVTT Decouple

Gigabyte Technology			
Title: DDR4 CHANNEL A			
Size: Custom	Document Number: H510M H		Rev: 1.0
Date:	Sheet 8 of 62		

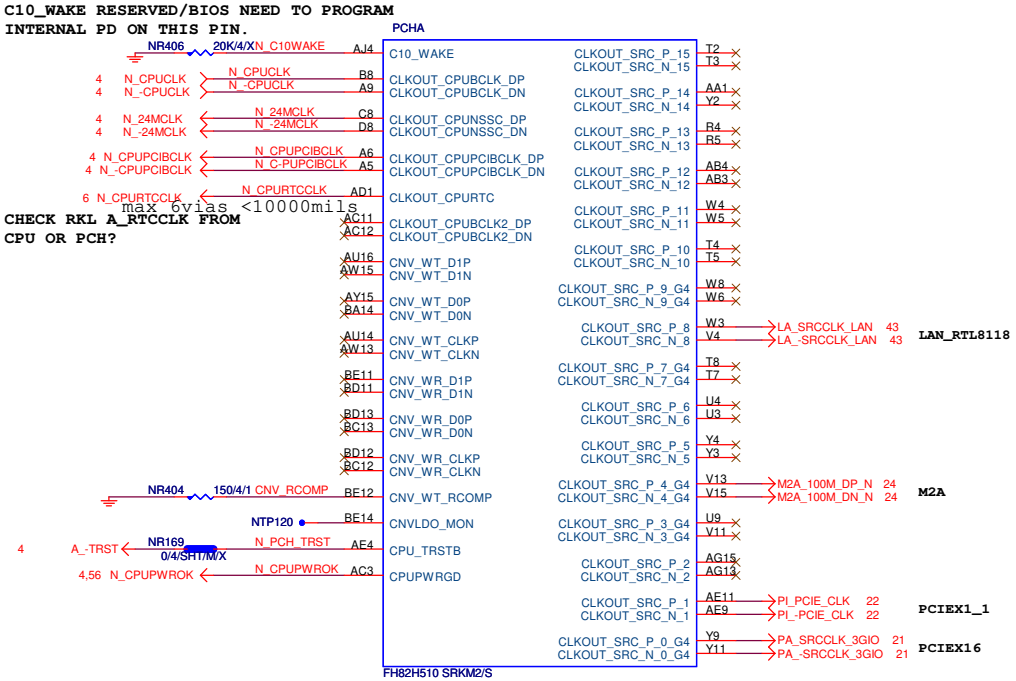
Rev:0.6

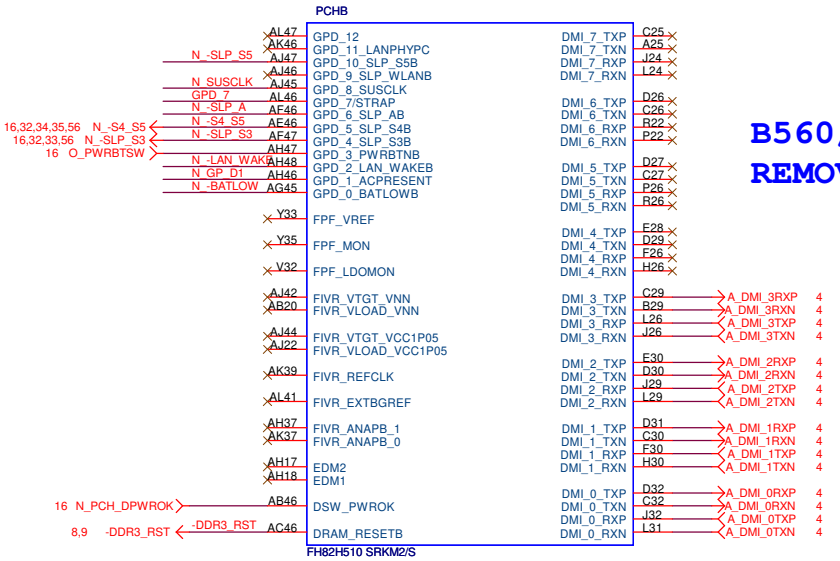


Gigabyte Technology		
Title: DDR4 CHANNEL B		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date:	Sheet 9 of 62	

RKL_TGP_PCH-H R0.11

C10_WAKE RESERVED/BIOS NEED TO PROGRAM
INTERNAL PD ON THIS PIN.



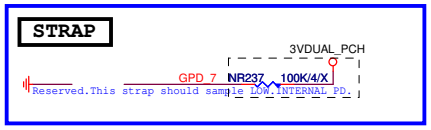


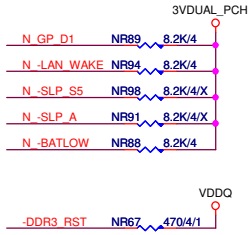
B560/H510
REMOVE DMI4~7

GPD: 3.3 V only, powered by the PCH DSW_3P3 power rail.

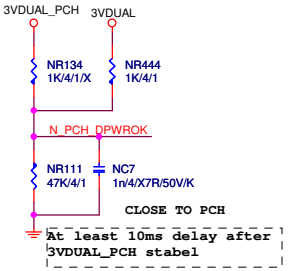
CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

STRAP

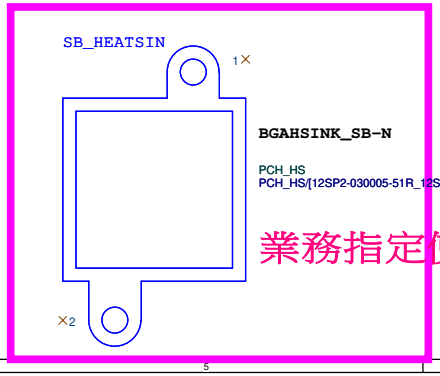




N_SUSCLK MAX 2 LOADS SUPPORTED



PCH Signal Glitch Free



業務指定使用B150M-EVO Heatsink

ANS 8477624 Gigabyte Technology

Title	PCH CLOCK BUFFER	
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 10 of 62	

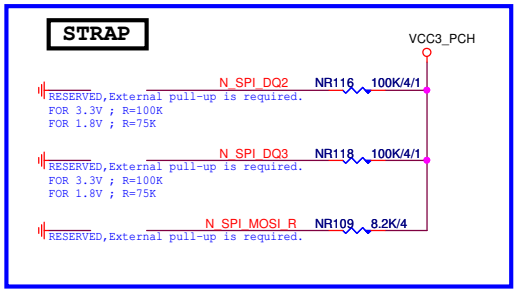
RKL_TGP_PCH-H R0.11

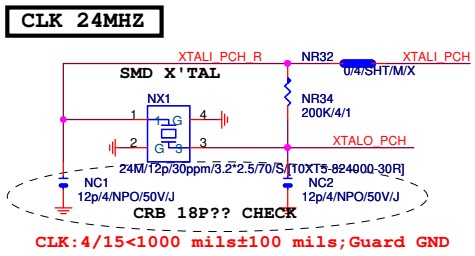
Intel 500 series PCH USB configration P1~P6

ITEM	USB P1	USB P2	USB P3	USB P4	USB P5	USB P6
H510	U3.2 Gen1x1	U3.2 Gen1x1	U3.2 Gen1x1	U3.2 Gen1x1	NA	NA
B560	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
H570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	Gen2x2		Gen2x2		Gen2x2	

Intel 500 series PCH USB20 configration

ITEM	USB P1~9	USB P10	USB P11	USB P12	USB P13	USB P14
H510	USB2	NA	NA	NA	NA	For Intel® Wireless-AC
B560	USB2	USB2	USB2	NA	NA	
H570	USB2	USB2	USB2	USB2	USB2	
Z590	USB2	USB2	USB2	USB2	USB2	
Q570	USB2	USB2	USB2	USB2	USB2	
W580	USB2	USB2	USB2	USB2	USB2	





PCH Signal Glitch Free

ANS 8477624

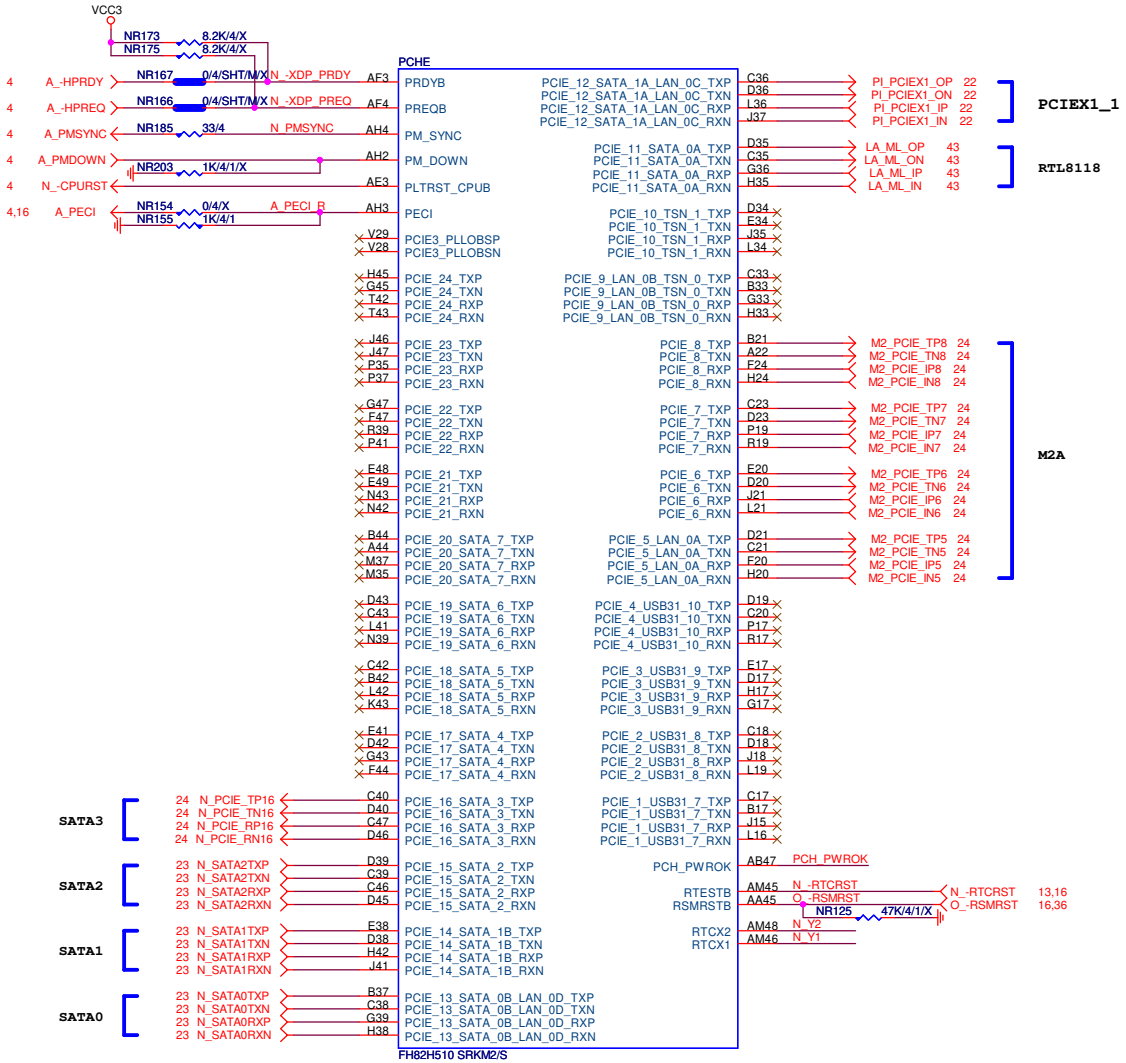
Gigabyte Technology

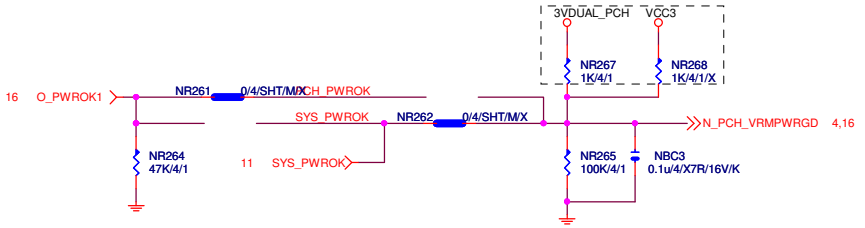
Title: PCH DMI,USB,PCIE

Size: Custom | Document Number: H510M H | Rev: 1.0

Date: Wednesday, January 06, 2021 | Sheet 11 of 62

RKL_TGP_PCH-H R0.11



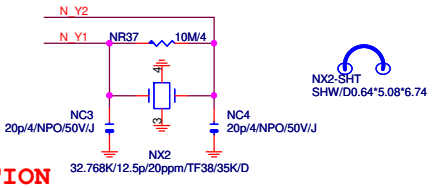


Intel 500 series PCH PCIE P5~P12								
ITEM	PCIE P5	PCIE P6	PCIE P7	PCIE P8	PCIE P9	PCIE P10	PCIE P11	PCIE P12
H510	PCIE /GbE	PCIE	PCIE	PCIE	GbE ONLY	N/A	PCIE	PCIE /GbE
B560	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
H570	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Z590	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Q570	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
W580	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
					Intel® RST for x2/x4 M.2			

Intel 500 series PCH PCIE P13~P24												
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23	PCIE P24
H510	SATA_0 /GbE	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 /GbE	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE	PCIE
H570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE	PCIE
					Intel® RST for x2/x4 M.2				Intel® RST for x2/x4 M.2			

RTC 32.768KHZ

DIP X'TAL



OPTION

SMD X'TAL

Intel 500 series PCH USB P7~P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
	PCIE	PCIE	PCIE	PCIE
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE

ANS 8477624 **Gigabyte Technology**

Title: **PCH MISC**

Size: Custom | Document Number: **H510M H** | Rev: **1.0**

Date: Wednesday, January 06, 2021 | Sheet 12 of 62

RKL TGP PCH-H R0.13

GPP_D PU/PD

GPP_B PU/PD

3VDUAL
NR296 8.2K/4 N_-VRALERT
N_-SLP_S0 NR438 100K/4/1

3VDUAL
CLKREQ PU/PD
NR2 8.2K/4 N_GPP_B5 PCIEX16
NR3 8.2K/4 N_GPP_B6 PCIEX1_1
PCIEX1_2
PCIEX4
NR6 8.2K/4 N_GPP_B9 M2A
M2P

ON-BOARD DEVICE PULL DOWN
N_GPP_B9 NR13 8.2K/4/X

綠框處為高階板預留使用，
無FUNCTION可刪除.

SYS_FAN5_PUMP_MODE

GEN4 不可變.
其餘依組態可更換

SYS_FAN1 MODE
CPU_FAN MODE

BATTERY

3VDUAL_PCH ND1 BAS40-05/0.2A/SOT23
NRB1 必須放在BAT外
BAT
BAT-SK/BK/P/S/D/SN
DIP款式矮的電池座
BATTERY-DN-1
N_VBATT NRB1 1K/4/1
NR136 1M/4 N_-INTRUDER
N_RTCVDD N_RTCVDD 11,15,54
NR142 20K/4/1 N_-RTCRST N_-RTCRST 12,16
NC10 1u/4/X5R/6.3V/K
NC9 1u/4/X5R/6.3V/K
RB_TP1 N_VBAT N_VBAT 16

BATTERY
CR2032

CLR_CMOS

CLR_CMOS
N_-RTCRST
PH/1*2/BK/2.54/VA/D

PCH Signal Glitch Free

N_-PFMRST NR129 100K/4/1/X

W_BUTTON LED
AUDIO
AUDIO beat mode
U32GEN2*2
MINI LOAD
U32GEN2*2
FOR EC MODEL/AUDIO
THB_C
PCIEX16 BIFURCATION
THB_C
PCIEX16 BIFURCATION
PCIEX16 BIFURCATION
CPU_OPT_MODE
HPWR_FAN_PUMP
SYS_FAN4 MODE
SYS_FAN3 MODE
SYS_FAN2 MODE
REMOVE N_-DDR_V_SEL

PCHD

AU29	GPP_D_23_UART3_CTSB_THC1_SPI2_INTB	
AY30	GPP_D_22_UART3_RTSB_THC1_SPI2_RSTB	
AW29	GPP_D_21_UART3_TXD_THC1_SPI2_IO_3	
BD30	GPP_D_20_UART3_RXD_THC1_SPI2_IO_2	
BD35	GPP_D_19_GSPI3_MOSI_THC1_SPI2_IO_1	
BD34	GPP_D_18_GSPI3_MISO_THC1_SPI2_IO_0	
BC34	GPP_D_17_GSPI3_CLK_THC1_SPI2_CLK	
BE35	GPP_D_16_GSPI3_CS0B_THC1_SPI2_CSB	
BB30	GPP_D_15_SML1DATA	
BC30	GPP_D_14_SPI1_IO_3_THC0_SPI1_IO_3	
BE30	GPP_D_13_SPI1_IO_2_THC0_SPI1_IO_2	
BD31	GPP_D_12_ISH_UART0_CTSB_SML0BALERTB	
BD32	GPP_D_11	
BC33	GPP_D_10_SML0DATA	
BE32	GPP_D_9_SML0CLK	
BD36	GPP_D_8_I2S2_SCLK_THC0_SPI1_INTB	
BE36	GPP_D_7_I2S2_RXD_THC0_SPI1_RSTB	
AY33	GPP_D_6_I2S2_TXD_MODEM_CLKREQ_CRF_XTAL_CLKREQ	
BA33	GPP_D_5_I2S2_SFRM_CNV_RF_RESET_B	
BF33	GPP_D_4_SML1CLK	
BD33	GPP_D_3_SPI1_MOSI_IO_0_THC0_SPI1_IO_0_SBK_3_BK_3	
BE33	GPP_D_2_SPI1_MISO_IO_1_THC0_SPI1_IO_1_SBK_2_BK_2	
AW32	GPP_D_1_SPI1_CLK_THC0_SPI1_CLK_SBK_1_BK_1	
AU31	GPP_D_0_SPI1_CSB_THC0_SPI1_CSB_SBK_0_BK_0	
BB26	GPP_C_23_UART2_CTSB_CNV_MFUART0_CTS_B	
AU26	GPP_C_22_UART2_RTSB_CNV_MFUART0_RTS_B	
AW26	GPP_C_21_UART2_TXD_CNV_MFUART0_TXD	
AY26	GPP_C_20_UART2_RXD_CNV_MFUART0_RXD	
BD20	GPP_C_19_I2C1_SCL	
BE21	GPP_C_18_I2C1_SDA	
BD21	GPP_C_17_I2C0_SCL	
BC22	GPP_C_16_I2C0_SDA	
BF23	GPP_C_15_UART1_CTSB_ISH_UART1_CTSB	
BD24	GPP_C_14_UART1_RTSB_ISH_UART1_RTSB	
BD23	GPP_C_13_UART1_TXD_ISH_UART1_TXD	
BC28	GPP_C_12_UART1_RXD_ISH_UART1_RXD	
BD29	GPP_C_11_UART0_CTSB	
BF29	GPP_C_10_UART0_RTSB	
BE29	GPP_C_9_UART0_TXD	
BE27	GPP_C_8_UART0_RXD	
BB24	GPP_C_7_ISH_I2C2_SCL_I2C3_SCL	
AY24	GPP_C_6_ISH_I2C2_SDA_I2C3_SDA_SBK_4_BK_4	
BD27	GPP_C_5_SML0ALERTB/STRAP	
BE25	GPP_C_4_ISH_UART0_TXD_SML0BCLK_I2C2_SCL	
BE24	GPP_C_3_ISH_UART0_RXD_SML0BDATA_I2C2_SDA	
BD26	GPP_C_2_SMBALERTB/STRAP	
BD25	GPP_C_1_SMBDATA	
BE26	GPP_C_0_SMBCLK	
BD42	GPP_B_23_SML1ALERTB_PCHHOTB/STRAP	
AW41	GPP_B_22_GSPI1_MOSI/STRAP	
BE46	GPP_B_21_GSPI1_MISO_NFC_CLKREQ	
BB42	GPP_B_20_GSPI1_CLK_NFC_CLK	
BD45	GPP_B_19_GSPI1_CS0B	
AU36	GPP_B_18_GSPI0_MOSI/STRAP	
BA36	GPP_B_17_GSPI0_MISO	
AY38	GPP_B_16_GSPI0_CLK	
BA39	GPP_B_15_GSPI0_CS0B	
BD40	GPP_B_14_SPKR/STRAP	
BD39	GPP_B_13_PLTRSTB	
BE40	GPP_B_12_SLP_S0B	
BE39	GPP_B_11_I2S_MCLK	
BD38	GPP_B_10_SRCCLKREQB_5	
BE38	GPP_B_9_SRCCLKREQB_4	
BF37	GPP_B_8_SRCCLKREQB_3	
BD37	GPP_B_7_SRCCLKREQB_2	
BC38	GPP_B_6_SRCCLKREQB_1	
BC37	GPP_B_5_SRCCLKREQB_0	
AU34	GPP_B_4_CPU_GP_3	
AW35	GPP_B_3_CPU_GP_2	
AY35	GPP_B_2_VRALERTB	
AY42	GPP_B_1_GSPI1_CS1B_TIME_SYNC_1	
AW37	GPP_B_0_GSPI0_CS1B	

FH82H510 SRKM2/S

AW46	GPPC_A_14	
AV46	GPPC_A_13_ESPI_ALERT3B	
AV47	GPPC_A_12_ESPI_ALERT2B	
AU45	GPPC_A_11_ESPI_ALERT1B	
AU46	GPPC_A_10_ESPI_ALERT0B	ESPI_ALERT
AU47	GPPC_A_9_ESPI_CS3B	
AT48	GPPC_A_8_ESPI_CS2B	
AT46	GPPC_A_7_ESPI_CS1B	
AT45	GPPC_A_6_ESPI_RESETB	ESPI_RESET-
AR47	GPPC_A_5_ESPI_CLK	N_GPP_A5 NR46 10/4
AR46	GPPC_A_4_ESPI_CS0B	ESPI_CS-
AP46	GPPC_A_3_ESPI_IO_3_SUSACKB	N_ESPI_IO3
AP47	GPPC_A_2_ESPI_IO_2_SUSWARNB_SUSPWRDNACK	N_ESPI_IO2
AN45	GPPC_A_1_ESPI_IO_1	N_ESPI_IO1
AN46	GPPC_A_0_ESPI_IO_0	N_ESPI_IO0
AL21	STRAP/GPPC_G_15_DDP2_CTRLDATA_TBT_LSX1_B	N_GPP_G15
AN21	GPPC_G_14_DDP2_CTRLCLK_TBT_LSX1_A	N_GPP_G14
AU19	STRAP/GPPC_G_13_DDP1_CTRLDATA_TBT_LSX0_B	N_GPP_G13
AW18	GPPC_G_12_DDP1_CTRLCLK_TBT_LSX0_A	N_GPP_G12
AY17	STRAP/GPPC_G_11_ISH_SPI_MOSI_DDP4_CTRLDATA_GSPI2_MOSI_TBT_LSX3_B	N_GPP_G11
BA17	GPPC_G_10_ISH_SPI_MISO_DDP4_CTRLCLK_GSPI2_MISO_TBT_LSX3_A	
BC17	STRAP/GPPC_G_9_ISH_SPI_CLK_DDP3_CTRLDATA_GSPI2_CLK_TBT_LSX2_B	N_GPP_G9
BE18	GPPC_G_8_ISH_SPI_CSB_DDP3_CTRLCLK_GSPI2_CS0B_TBT_LSX2_A	
BF17	GPPC_G_7	N_GPP_G7
BD17	GPPC_G_6	N_GPP_G6
BE17	GPPC_G_5_SLP_DRAMB	
BD16	GPPC_G_4_GMII_MDIO_0	
BC16	GPPC_G_3_GMII_MDC_0	
BE15	GPPC_G_2_DNX_FORCE_RELOAD	
BD15	GPPC_G_1_DDPA_CTRLDATA	
BD14	GPPC_G_0_DDPA_CTRLCLK	
BG13	GPPC_RCOMP	GPPC_COMP NR45 200/4/1
B13	MPHY_RCOMPP	PCIECOMP_P_R NR38 100/4/1 PCIECOMP_P
A13	MPHY_RCOMPN	PCIECOMP_N
AR3	MLK_RSTB	
AR4	MLK_DATA	
AP4	MLK_CLK	
AM2	JTAGX	N_PCH_JTAGX NR66 0/4/SHT/M/X A_TCK 4
AM4	JTAG_TMS	N_PCH_TMS NR92 0/4/SHT/M/X A_TMS 4
AM3	JTAG_TDO	N_PCH_TDO NR93 0/4/SHT/M/X A_TDO 4
AN4	JTAG_TDI	N_PCH_TDI NR95 0/4/SHT/M/X A_TDI 4
AM5	JTAG_TCK	N_PCH_TCK NR110 51/4/1/X
AG5	STRAP/DBG_PMODE	N_ITP_PMODE
AE47	INTRUDERB	N_-INTRUDER
AJ5	HDACPU_SDO	DISPA_SDO NR298 33/4 N_AZCPU_SDOUT 4
AK4	HDACPU_SDI	A_AZ_CPU_SDI 4
AJ3	HDACPU_BCLK	DISPA_BCLK NR68 33/4 N_AZCPU_SCLK 4

PLACE 510HM PD WITHIN 1.1INCH OF PCH

DDPB/C -->CHIPSET U3C

USB_OC
SPI_TPM

NR46/NR47/NR48/NR50/NR57
CLOSE TO PCH<500mil

TCP* pins can be routed to USB-C* connector or DP/HDMI native connector

GPPC_A/GPPC_G (VCCPRIM_3P3 or VCCPRIM_1P8):
each pin voltage is selected by setting the corresponding voltage select soft strap of the pin.

VCCSTG
N_PCH_TMS NR79 51/4/1
N_PCH_TDO NR82 100/4/1
N_PCH_TDI NR84 51/4/1
N_PCH_JTAGX

VCC3 3VDUAL
N_GPP_G12 NR275 3.3K/4/1/X
N_GPP_G14 NR276 3.3K/4/1/X
N_SMBCLK NR53 1K/4/1
N_SMBDATA NR55 1K/4/1
N_SML0CLK NR58 499/4/1
N_SML0DAT NR59 499/4/1
N_SML1DAT NR61 8.2K/4
N_SML1CLK NR292 8.2K/4

For eSPI
VCCBT
N_GPPC_G7 NR71 8.2K/4
ESPI_ALERT NR49 8.2K/4/X
ESPI_RESET- NR51 8.2K/4/X
ESPI_CS- NR52 8.2K/4/X
ESPI_RESET- NR137 75K/4/1
ESPI_CS- NR138 75K/4/1

STRAP

N_SPKR NR131 8.2K/4/X VCC3
TOP SWAP OVERRIDE STRAP, PCH HAS INTERNAL WEAK PD
HIGH:TOP SWAP ENABLED
LOW:TOP SWAP DISABLED

N_GPP_B18 NR133 8.2K/4/X 3VDUAL
NO REBOOT IF SAMPLED HIGH, PCH HAS INTERNAL WEAK PD

N_GPP_B22 NR124 8.2K/4/X
Boot BIOS Strap (BBS),PCH HAS INTERNAL WEAK PD.
1 : ESPI PERIPHERAL CHANNEL
0 : SPI(MAF) OR ESPI FLASH CHANNEL(SAF)

NR102 1K/4/1/X N_GPP_C2 NR103 8.2K/4 VCC3_PCH
TLS Confidentiality IF SAMPLED HIGH,
CH HAS INTERNAL WEAK PD

NR105 1K/4/1/X N_GPP_C5
ESPI DISABLE STRAP PCH HAS INTERNAL WEAK PD
HIGH:DISABLE
LOW:ENABLE(DEFAULT)
For eSPI

N_-PCH_HOT NR114 8.2K/4/X VCC3_PCH
CPUNSSC Clock Frequency, PCH HAS INTERNAL 20K PD
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)

NR249 1K/4/1/X N_ITP_PMODE V1P05A
Reserved.INTERNAL WEAK PH.

* RKL
N_GPP_G15 NR247 2.2K/4/X 3VDUAL_PCH
N_GPP_G13 NR248 2.2K/4/X
N_GPP_G11 NR241 2.2K/4/X
N_GPP_G9 NR242 2.2K/4/X
TBT VCCIO CONFIGURATION,PCH HAS INTERNAL WEAK PD
HIGH:3.3V
LOW:1.8V

ANS 8477624

Gigabyte Technology

Title	PCH SATA,PCIE,SATA_EXPRESS	
Size: Custom	Document Number: H510M H	Rev: 1.0
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RKL_TGP_PCH-H R0.11

PCHC

FH82H510 SRKM2/S

DEBUG LED
PCIEX8 A19
PCIEX8 A33
PCIEX8 A32
PCIEX8 PRESENT

CNVI WIFI/BT DISABLE

TBT RTD3
M2B CPU DETECT
M2A CPU IFDET
M2A CPU DETECT

J GROUP ONLY 1.8V LEVEL

**DDPC CHANGE TO GPP_G12/G13

U32GEN2*2 C.C DETECT

VCCIO VID
M2C CPU DETECT
M2P IFDET
M2P DETECT
M2M IFDET
M2M DETECT

M2A CPU DEVSLP
M2B CPU DEVSLP
M2C CPU DEVSLP

EC MODEL

EC MODEL
for ASM3142 use
E1/E0-->Multi Key

Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP_J and GPP_S (1.8 V/VCCPRIM_1P8)

CLKREQ PH/PD
M2M
WIFI
RT8118
ON-BOARD DEVICE

注意:PWM SIDE PD 100K.

Internal pull up

RESERVED STRAP

STRAP

HDA_SDO:Flash Descriptor Security (override);
1=DIS,0=ENABLE
PCH INTERNAL PD

ESPI FLASH SHARING MODE,INTERNAL 20K PD
0: MASTER ATTACHED FLASH SHARIN
1: SLAVE ATTACEHD FLASH SHARING

XTAL Frequency Selection,INTERNAL 20K PD
0 = 38.4 MHz (default)
1 = 24 MHz

Reserved.INTERNAL 20K PD.
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

M.2 CNVi Mode Select,external PU is required.
0=>Integrated CNVi enabled.
1=>Integrated CNVi disabled.
Note: When connected to the PCH CNVi interface, the device internal PD resistor will pull the strap low to enable CNVi interface

SPI FLASH INTERFACE VOLTAGE,INTERNAL 20K PD
0=> VCCSPI at 3.3 V (Default)
1=> VCCSPI at 1.8 V

Display Port DDC/HOT PLUG SIGNAL

CPU PORT	PCH DDC	PCH HPD
DDI_A/EDP	GPP_G0/G1	GPP_K6
DDI_1/B	GPP_I5/I6	GPP_K7
DDI_2/C	GPP_G12/G13	GPP_I1
DDI_3/D	GPP_G14/G15	GPP_I2

*** HPD: DDI*. PULL DOWN IF NO USE.

A B C D — DP to VGA

PCH Signal Glitch Free

RTD3 GPIO	CML-S	RKL-S
TBT_PERST_N	GPP_F2	GPP_F16
TBT_Wake_N	GPP_H15	GPP_H9
RTD3_PWN_EN	GPP_K23	GPP_K3

ANS 8477624

Gigabyte Technology

Title: PCH PWR

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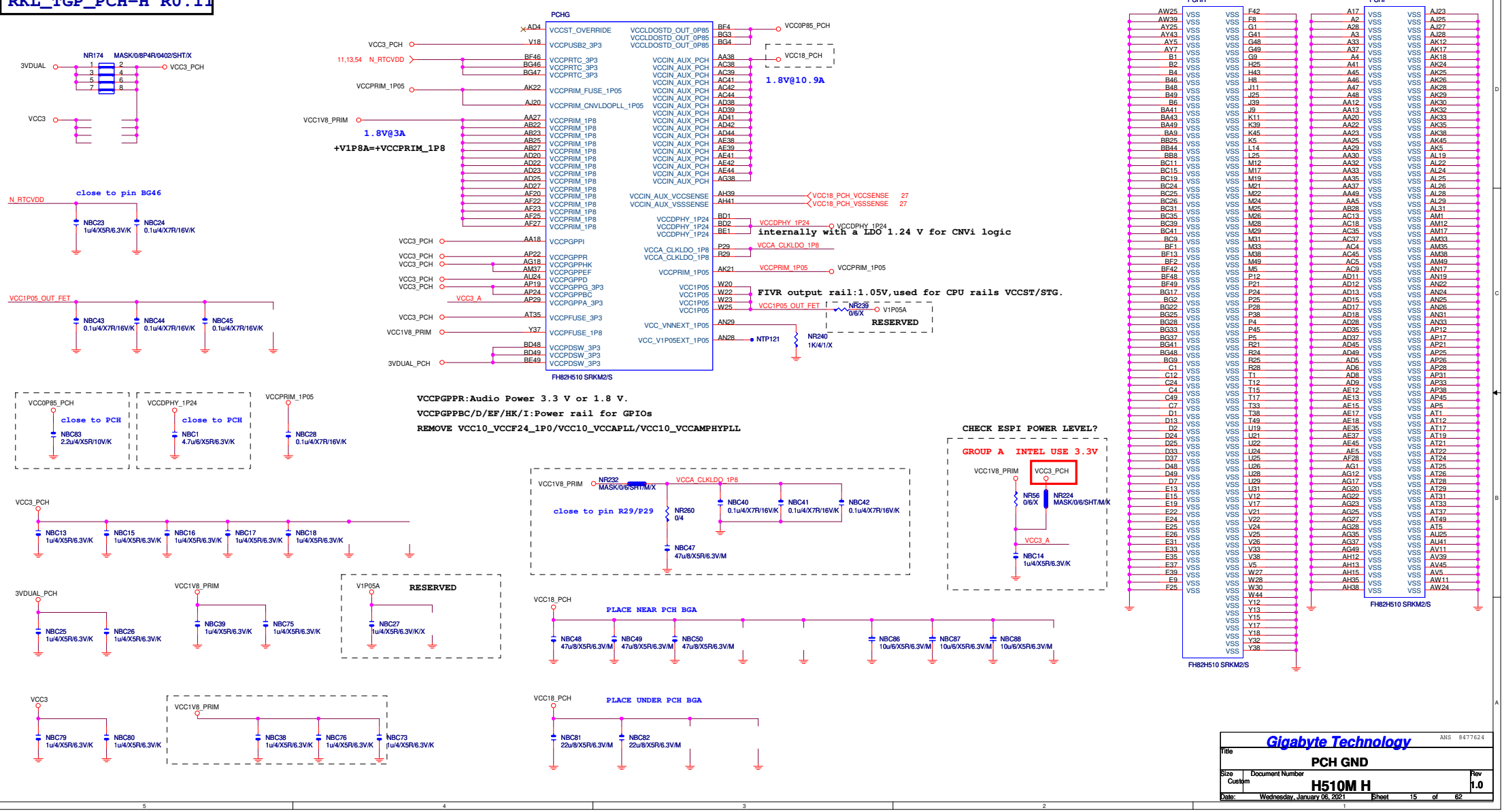
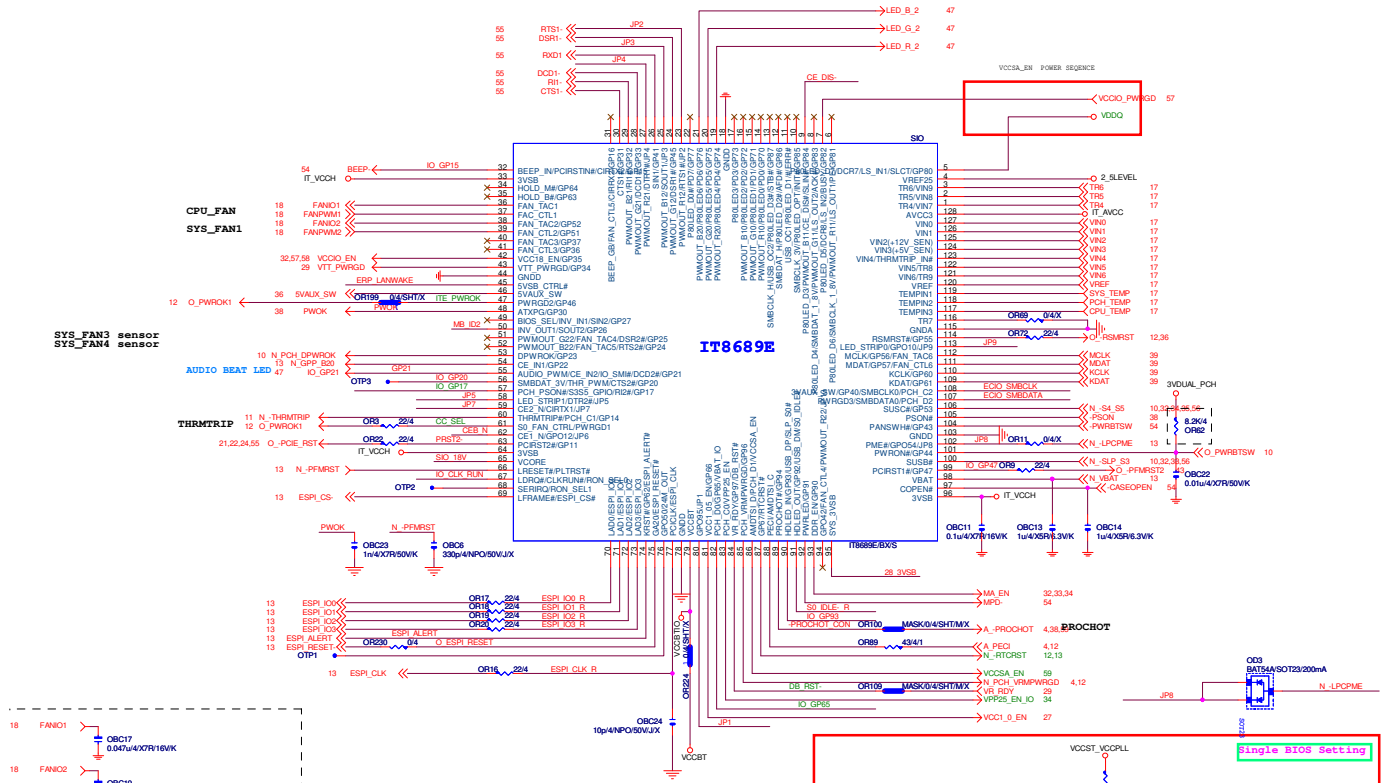
RKL_TGP_PCH-H R0.11

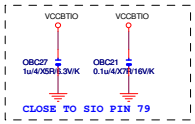


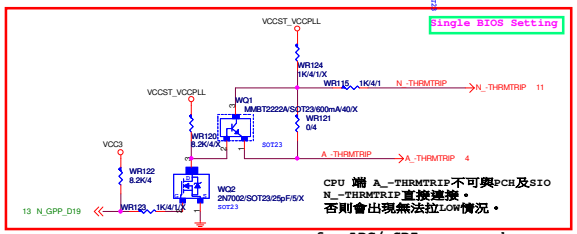
Gigabyte Technology	ANS 8477624
Title	PCH GND
Size: Custom	Document Number: H510M H
Rev	1.0
Date: Wednesday, January 06, 2021	Sheet 15 of 62

CFL SIO IT8686 REV:0.5

IT8686 LPT+COMA

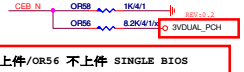






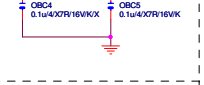
FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

DUAL BIOS OPT STRAP

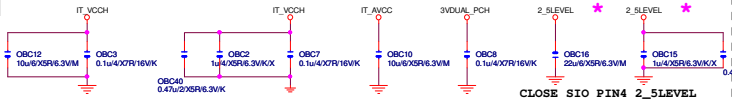


MB ID

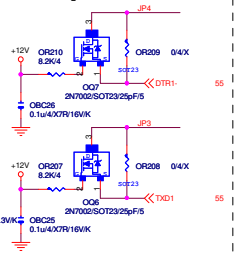
SIO_18V



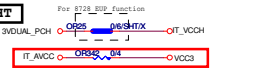
SIO CAP



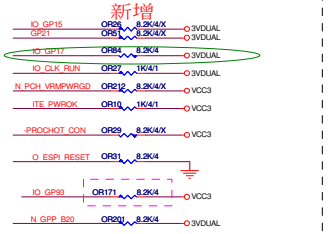
for LPC/eSPI power mode



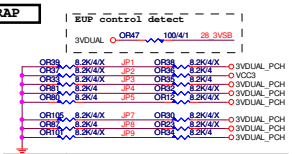
PWR SHT



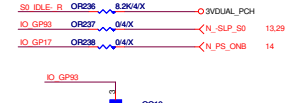
SIO PU

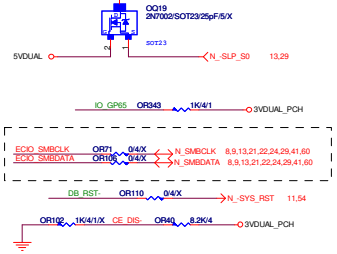


SIO STRAP



JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7 JP3	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

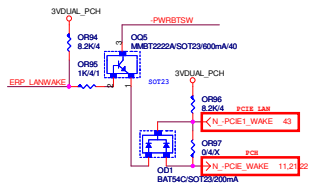




ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	
	Intel 219	組態二
Dual LAN (只管一個LAN支援ERP下WAKE UP)	Atheros+Atheros	組態一
	Intel 219+Atheros	組態三
	Intel 219+Intel 210	
No Support ERP	Single LAN BOM只上OR97。 Dual LAN BOM只上OR97、OR99。	

請依開案規格，選擇Support Erp下 LAN Wake up組態。

(組態一) PCIE LAN(Single & Dual LAN)



Gigabyte Technology

Title	IT8686	
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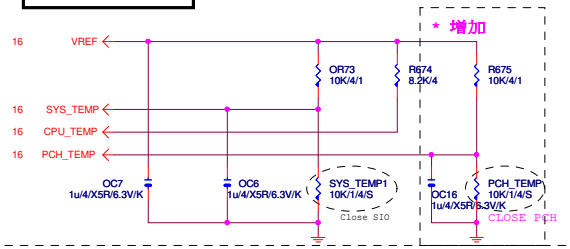
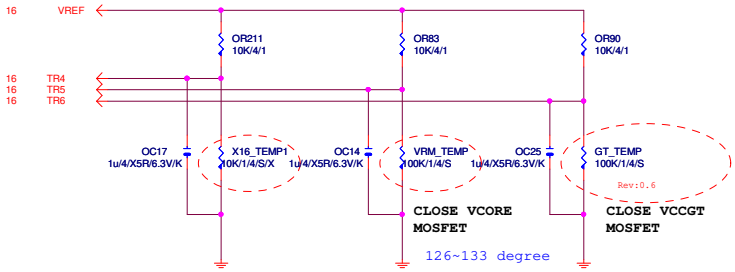
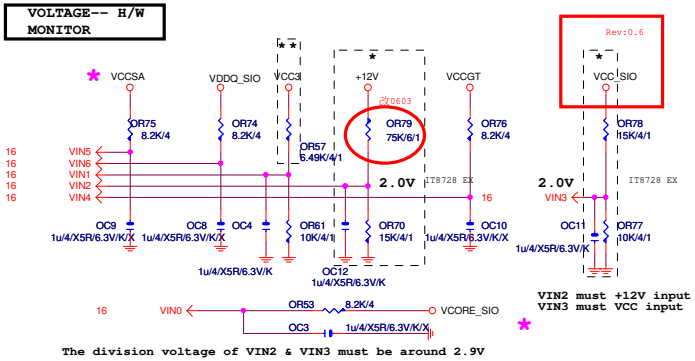
TEMP H/W MONITOR



低階機種:3個FAN時使用



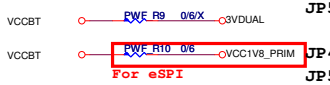
VOLTAGE-- H/W MONITOR

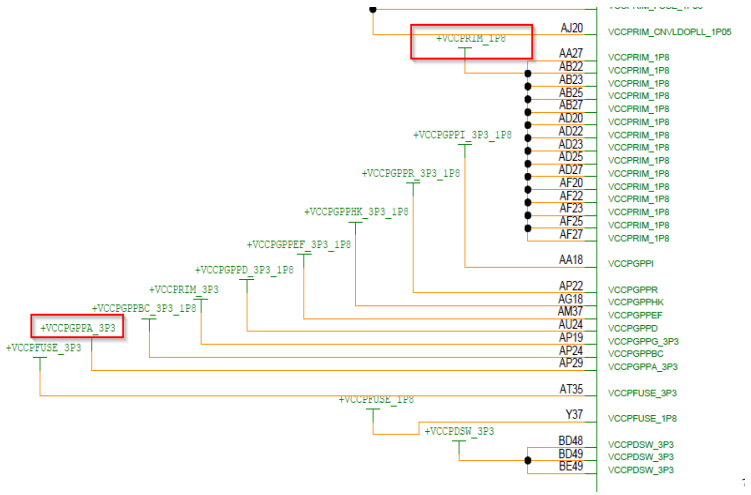


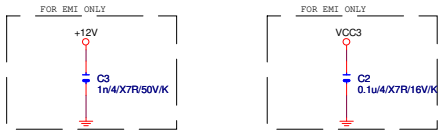
The division voltage of VIN2 & VIN3 must be around 2.9V

JP4 HI ESPI MODE VCCBT 3.3V
JP5 HI ESPI MODE LPC I/F

JP4 LO ESPI MODE VCCBT 1.8V
JP5 LO ESPI MODE ESPI I/F







★Update 2015-04.24

Gigabyte Technology			
Title: HWM,KB/MS, FAN CTRL			
Size: Custom	Document Number: H510M H		Rev: 1.0
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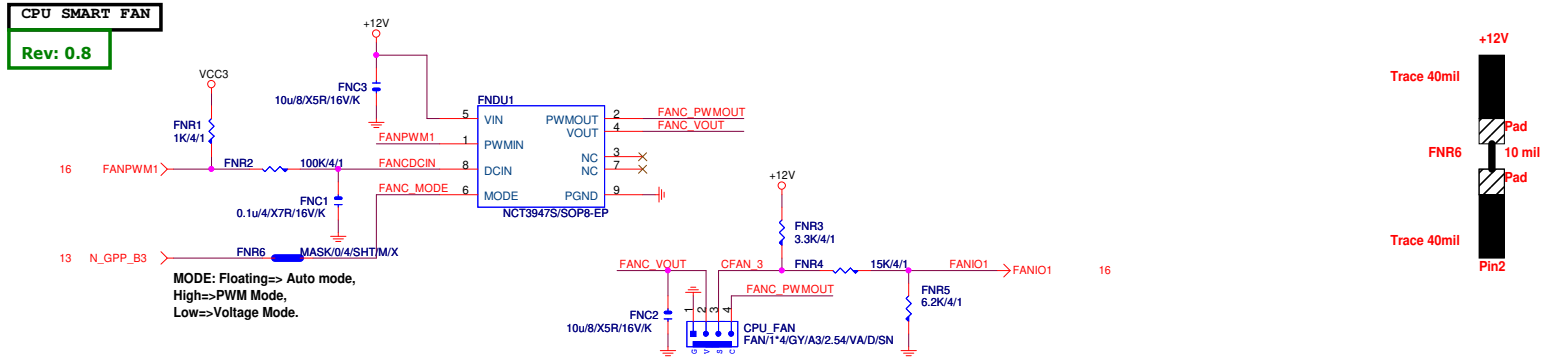
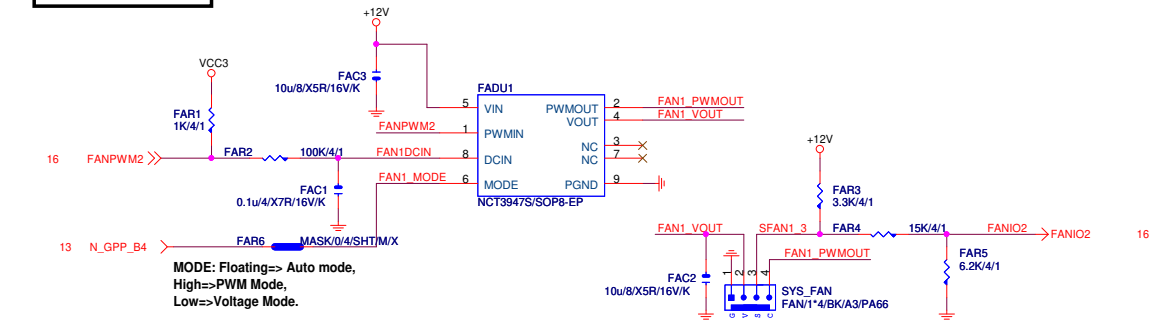
CPU SMART FAN

Rev: 0.8



A. SYSTEM FAN1



Gigabyte Technology		
Title: FAN CTRL		
Size: Custom	Document Number: H510M H	Rev: 1.0
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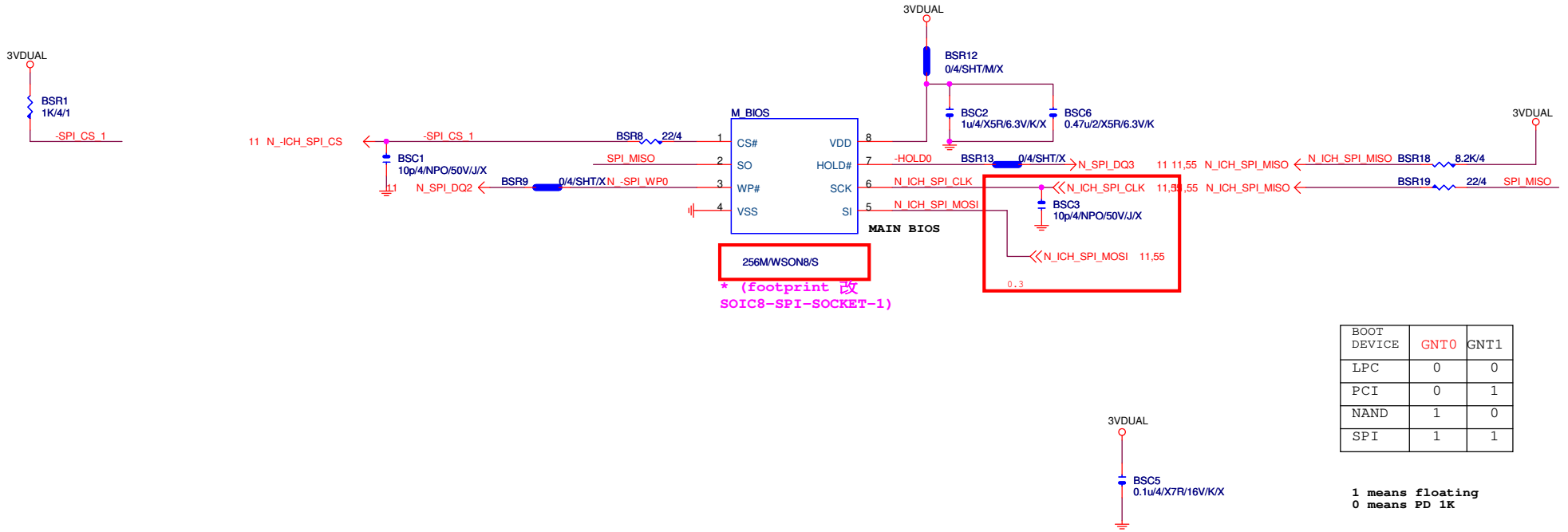
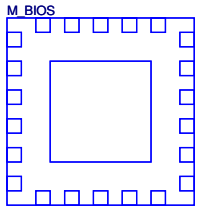
DUAL BIOS

MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K



SMD WSON8 SK 8P 200MIL LOTES/[10SL2-000008-71R]/X

* 試產先上 , PVT 移除

Gigabyte Technology

Title: BIOS

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CEC_R0.3

GIGABYTE™

Title: CEC relate circuit

Size	Document Number	Rev
Custom	H510M H	1.0

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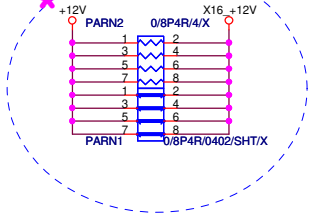
Rev 0.2

+12 protect
short-wire test



PCIESLOT-164P

PCIEX16

3GIO_*16

KEY

PCI-E/16X-164P/GY/LONG DOUBLE/HK*2/GEN4.0/[11AC1-023164-X1R_11AC1-023164-X2R]

PCIEX16:16/5/5/5/16

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology		
Title: PCI EXPRESS * 16		
Size: Custom	Document Number: H510M H	Rev: 1.0
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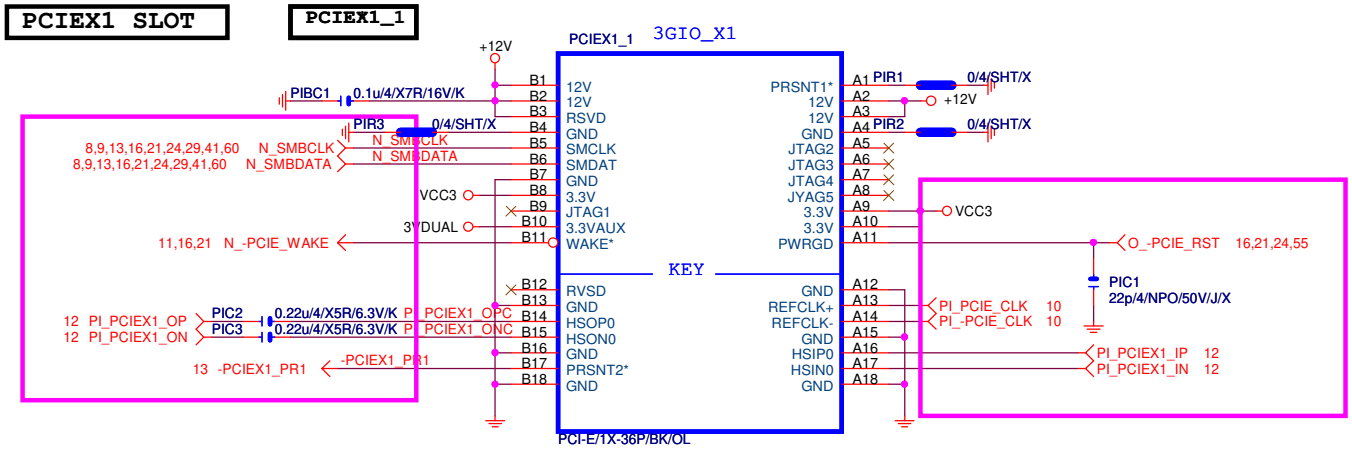
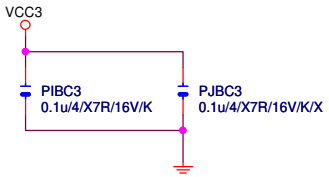
Rev 0.51





Gigabyte Technology

Title: PCIE_X4

Size	Document Number	Rev
Custom	H510M H	1.0

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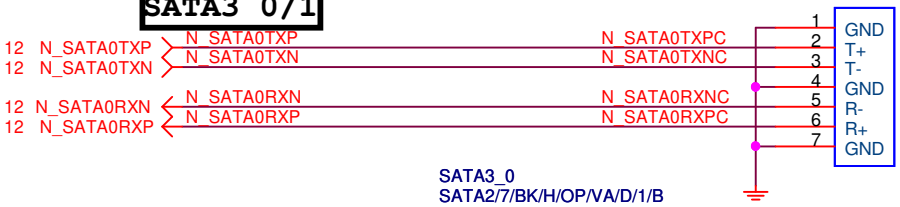
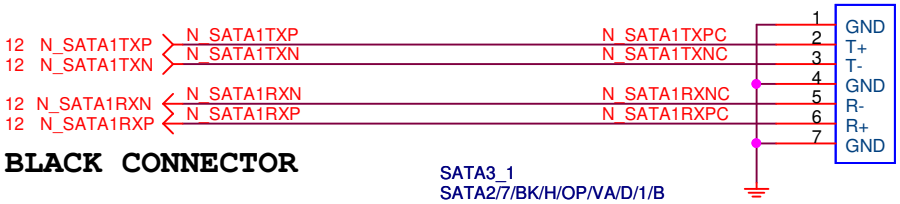
SATA3 0/1



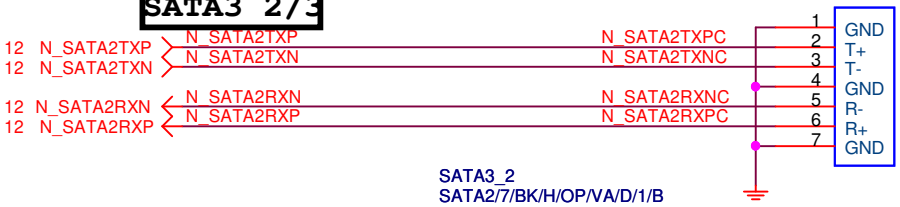
SATA3_0
SATA2/7/BK/H/OP/VA/D/1/B

BLACK CONNECTOR



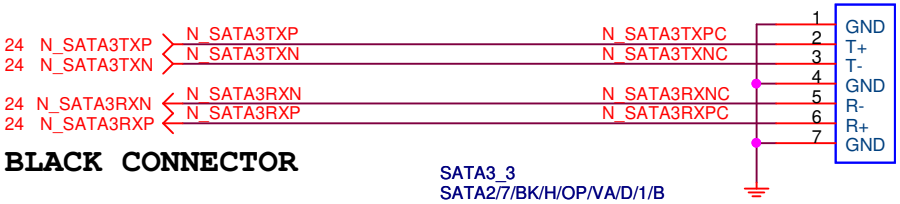
SATA3_1
SATA2/7/BK/H/OP/VA/D/1/B

SATA3 2/3



SATA3_2
SATA2/7/BK/H/OP/VA/D/1/B

BLACK CONNECTOR

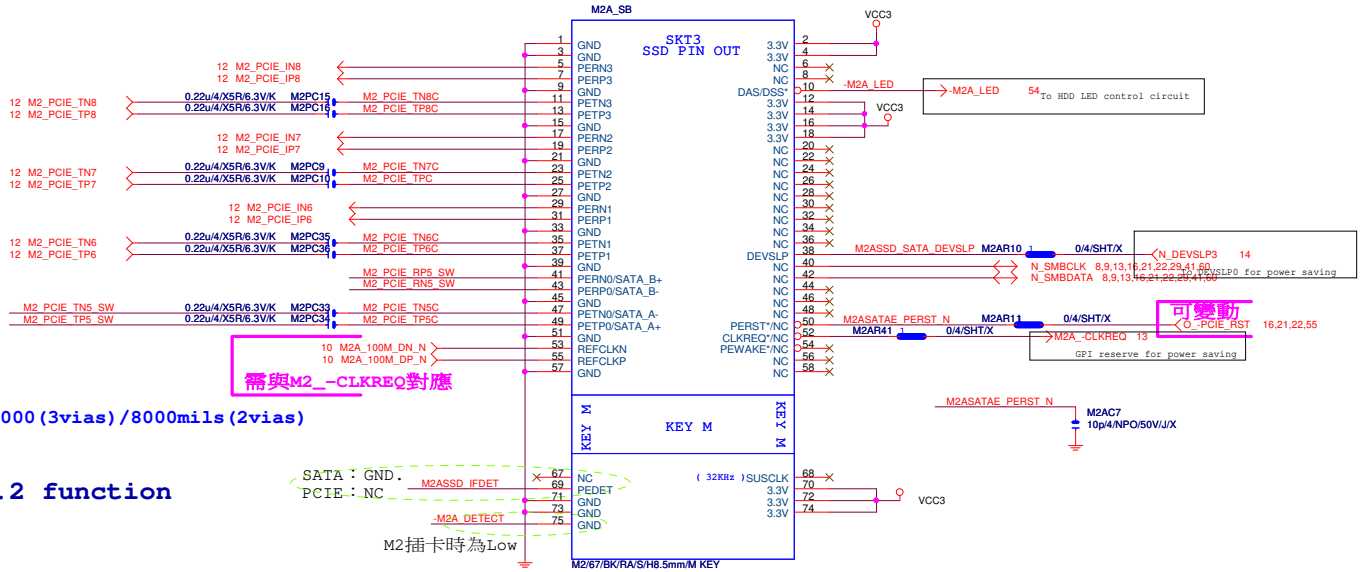


SATA3_3
SATA2/7/BK/H/OP/VA/D/1/B

SATA3 4/5

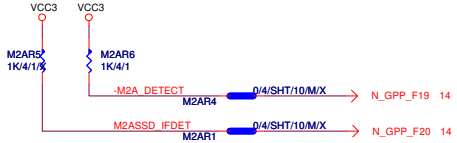
Gigabyte Technology		
Title: SATA		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 23 of 62	

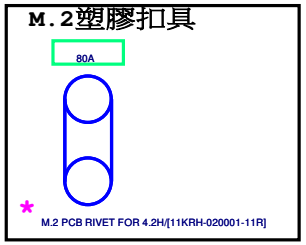
Rev 0.1



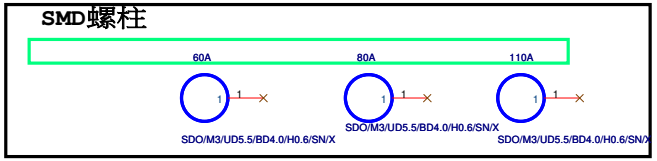
Length Total:2000mis~7000(3vias)/8000mils(2vias)

支援SATA and M.2 function



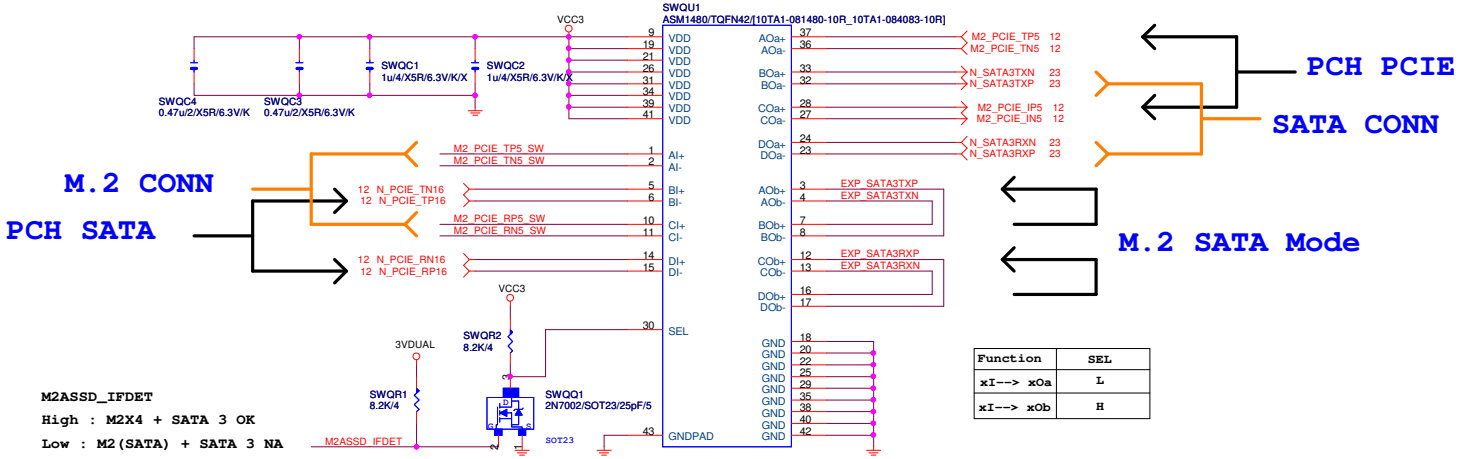


Footprint : NGFF-M-75P-11CM-3-SMD



★ Footprint : HOLE_165NP

舊的Switch,價格低



Function	SEL
xI--> xOa	L
xI--> xOb	H

Gigabyte Technology			
Title: M.2 X4			
Size: Custom	Document Number: H510M H		Rev: 1.0
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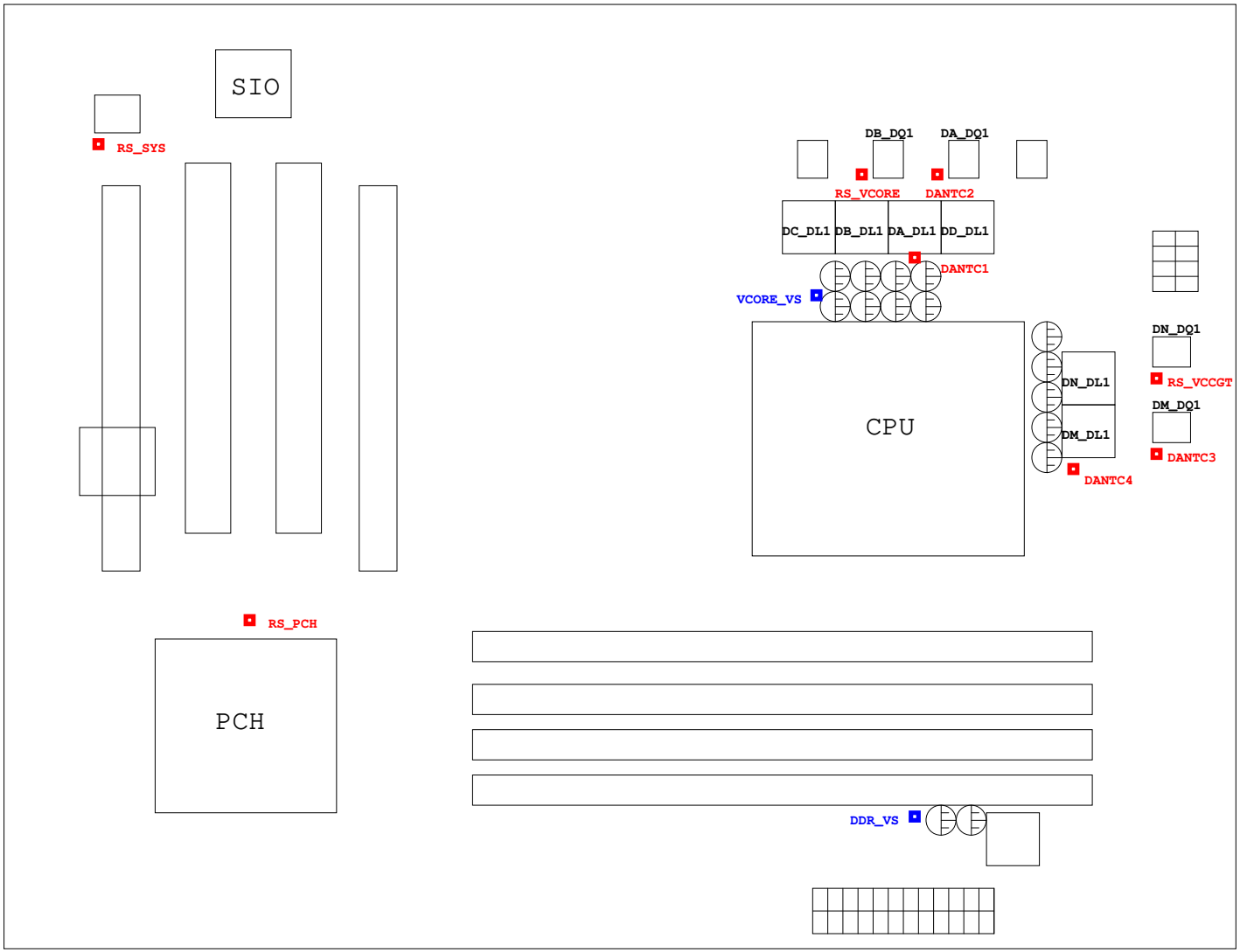

熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL1	N/A
DANTC2	DA_DQ1	Differential
DANTC3	DM_DQ1	N/A
DANTC4	DM_DL1	Differential
RS_VCORE	DB_DQ1	N/A
RS_VCCGT	DN_DQ1	N/A
RS_PCH	PCH	N/A
RS_SYS	CU1	N/A

Gigabyte Technology

Title: NTC MAP

Size: Custom | Document Number: H510M H | Rev: 1.0

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Gigabyte Technology

Title

IT8892E

Size	Document Number	Rev
Custom	H510M H	1.0

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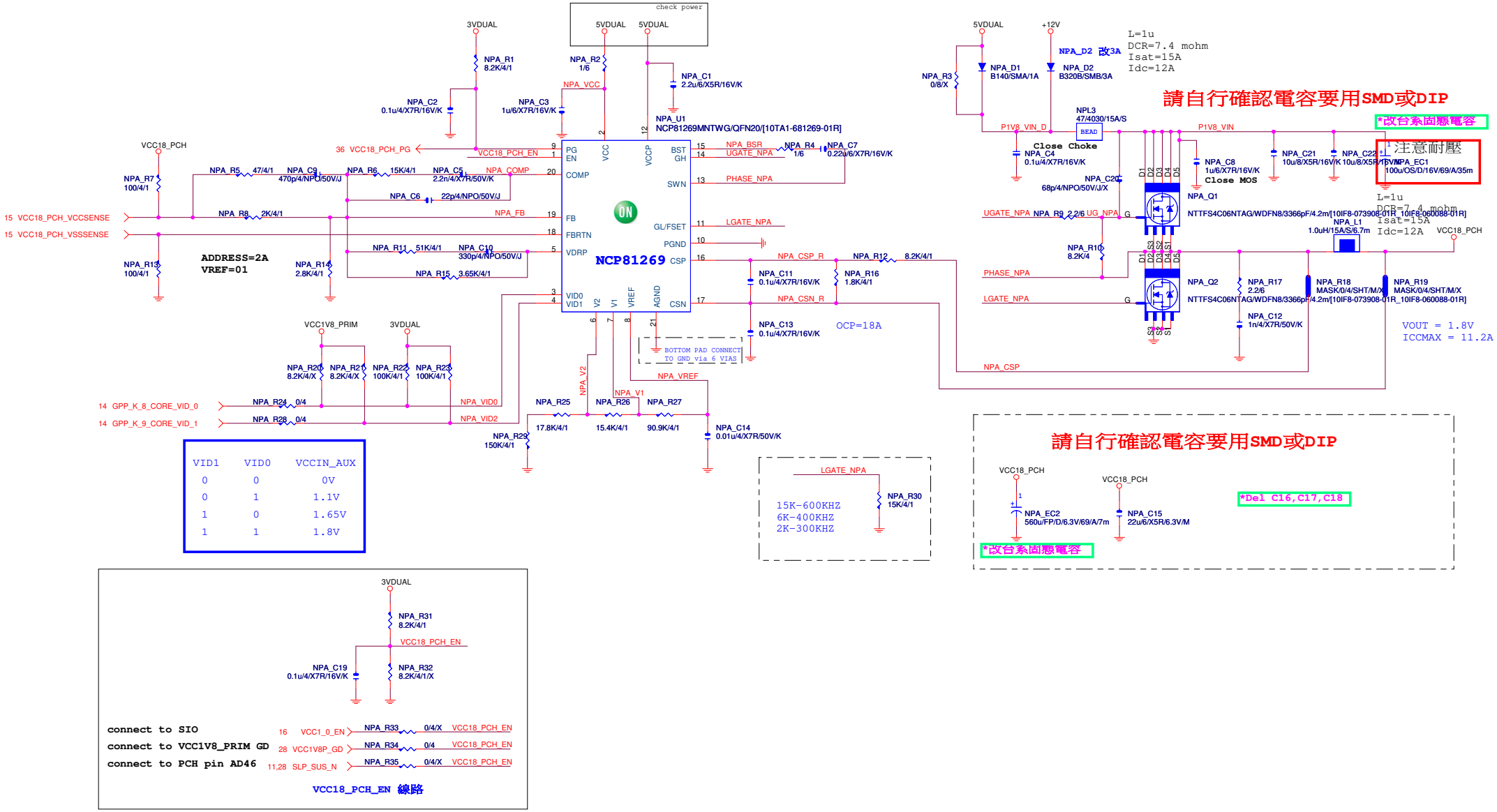


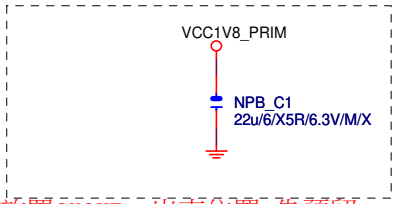
GIGABYTE

Title	NCP81269_PCH POWER	
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 27 of 62	

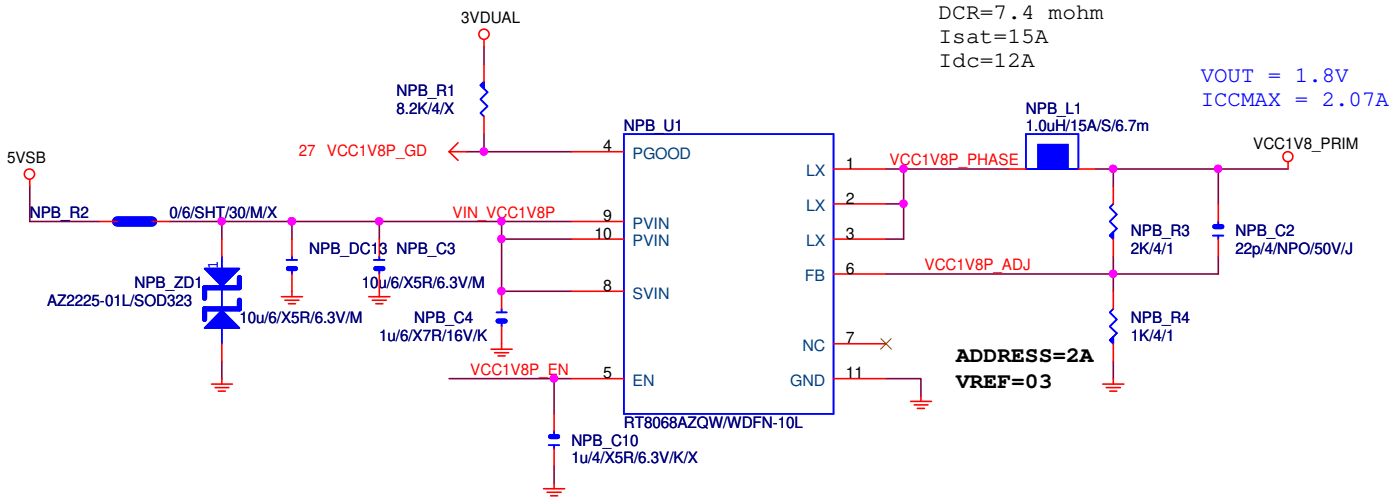
REV:0.1

VCC1V8_PRIM

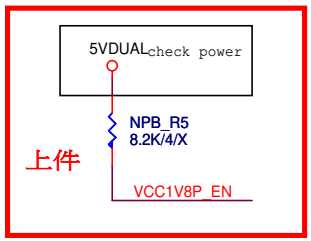
CHOKE與CAP料號可變



請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

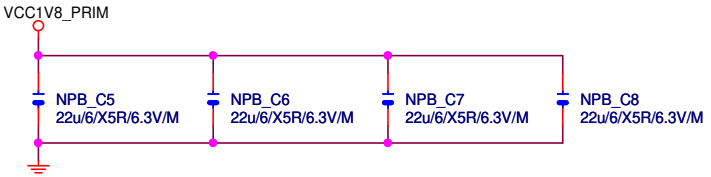


PWR SEQ



connect to PCH pin AD46

VCC1V8_PRIM CAP 22u*4PCS



Gigabyte Technology			
Title: RT8068_VCC1V8_PRIM			
Size: Custom	Document Number: H510M H		Rev: 1.0
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Intel IMVP8 POWER CKT - RKL S-LINE 125W - 6+2 phase

S-Line 125W CPU power spec
Vcore ICCMAX=245A, PL2=185A
Loadline=1.1m ohm
VccGT ICCMAX=55A, PL2=46A
Loadline=4m ohm

Choke : 0.3uH/0.72m ohm

SR: Slew Rate set at 10mV/uS — DAR137 10K/4/1

ADDR: VCORE SVID ADDRESS=00h; VCCGT SVID ADDRESS=01h — DAR138 10K/4/1

ICCMAX: VCORE IMAX SET AT 245A — DAR139 243K/4/1

VBOOT: VCORE VBOOT=0V — DAR148 59K/4/1

ICCMAXA: VCCGT IMAX SET AT 55A; 54.9K/4/1/A — DAR149

VBOOTA: VCCGT VBOOT=0V — DAR161 59K/4/1

ROSC: VCORE WORKING FREQ ~ 270KHZ — DAR216 21K/4/1

ROSCA: VccGT WORKING FREQ ~ 270KHZ — DAR217 21K/4/1

DAU1 NCP81229MNTXG/QFN52 6X6 52PIN QFN

VCORE PORTION

VCCGT PORTION

OCP~350A

OCP~85A

PUT CLOSE TO PWM

PUT COLSE TO VCORE HOT SPOT

BOTTOM PAD CONNECT TO GND Through 6 VIAs

PUT COLSE TO VCCGT HOT SPOT

VCORE_SIO — VCORE_VS MASK/0/4/SHT/M/X — VCORE

請注意擺放位置

ENABLE

NOT INSTALL CPU --> VBOOT=1.05V
INSTALL CPU --> VBOOT=0V

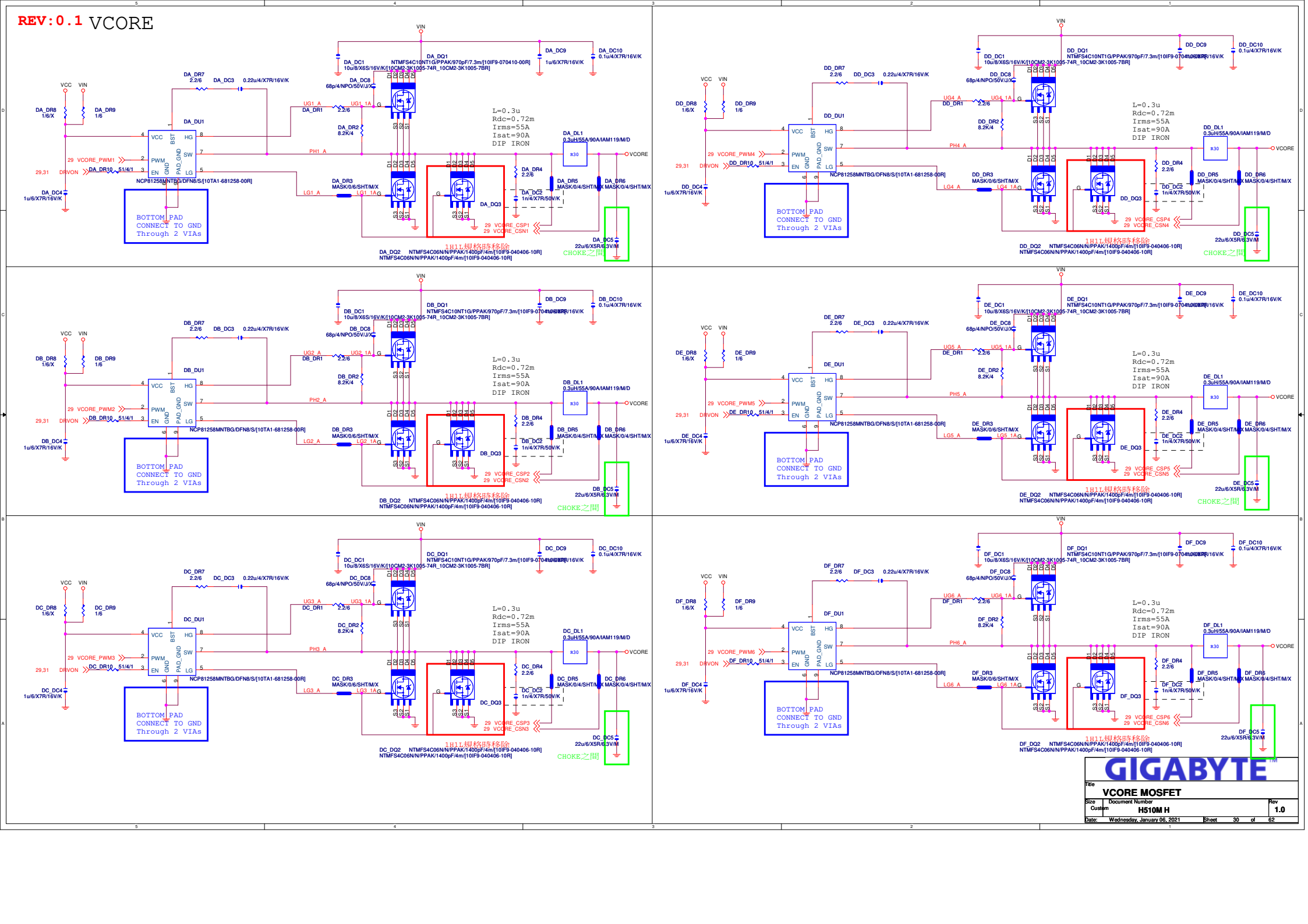
Gigabyte Technology

Title

Size | Document Number | Rev

Date: Wednesday, January 06, 2021 | Sheet 29 of 62

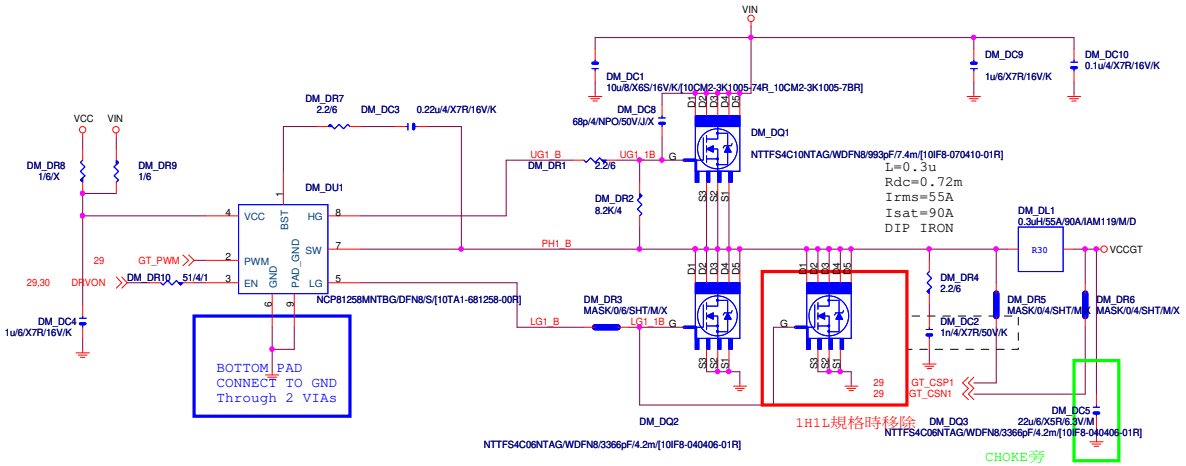
REV:0.1 VCORE

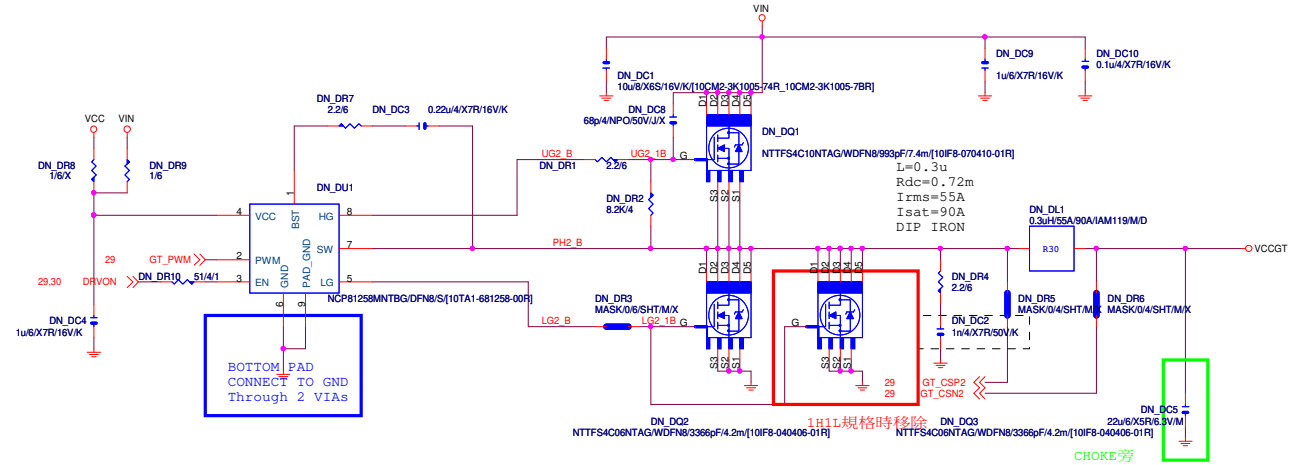


GIGABYTE

Title	VCORE MOSFET	
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 30 of 62	

REV::0.1 VCCGT 3X3 MOSFET





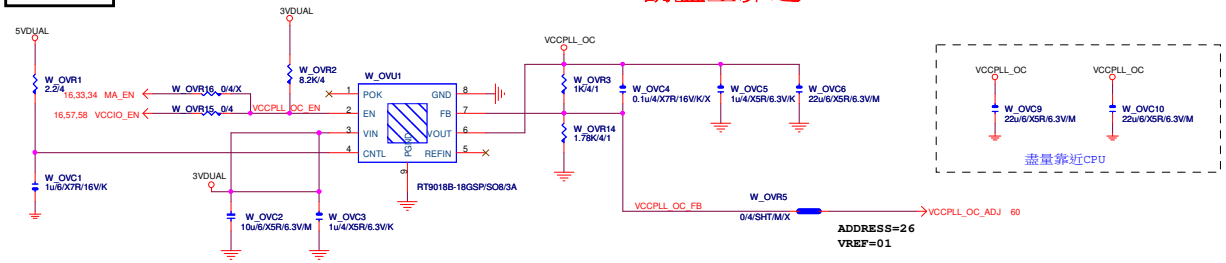
GIGABYTE™

Title: VCCGT MOSFET		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 31 of 62	

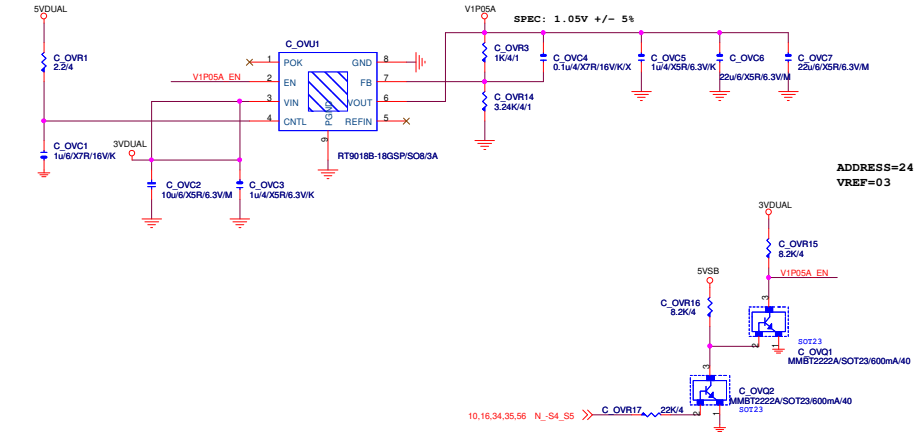
REV:0.12

VCCPLL_OC

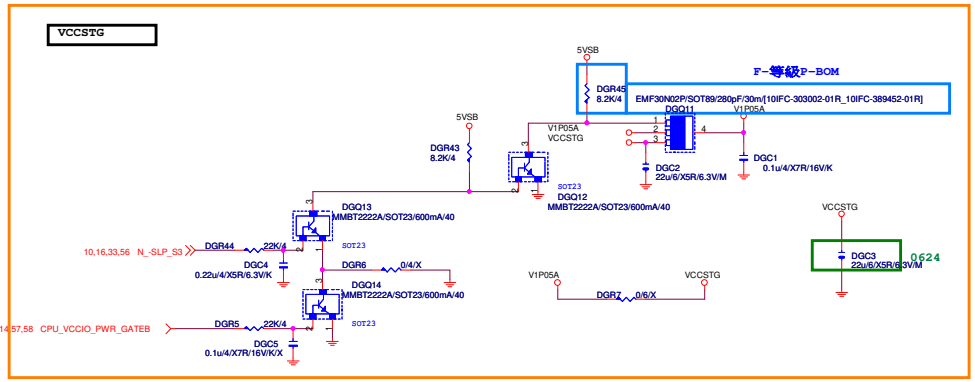
請盡量靠近CPU



V1P05A



VCCSTG



GIGABYTE™

Title: CPU POWER-1		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 32 of 62	

REV:0.11

DDR4

5VDUAL
MAR2
8.2K/4
MA_EN
上件

MA_DR38.MA_DC15

VPP_25V使用8120.8068A.RT8237時上件

VDDQ_SIO
VDDQ
DDR_VS
MASK/0/4/SHT/M/X

CLOSE TO DDR POWER PLANE

FS=290K
OCP=40A

MAU2
RT8237/[10TA1-608237-01R]

MA_DR8 2.2/6
MA_DC10 1u/6/X7R/16V/K
MA_DR37 100K/4/1
VDDQ_GD
MA_DC9 0.1u/6/X7R/25V/K
VPP_25V
MA_DR40 8.2K/4/X
MA_DR41 8.2K/4
34 VPP25V_GD
16,32,34 MA_EN
MA_DR38
MASK/0/4/SHT/M/10/X
DDR_EN
MA_DR39 0/4/X
MA_DC15 0.1u/4/X7R/16V/K
EN PGOOD VCC BOOT UGATE PHASE FB CS RF GND LGATE
MA_UGATE
MA_PHASE
MA_LGATE
MA_RF
MA_DR45
VDDQ_GD 470K/4/1
MA_DR15 182K/4/1
MA_DR19 470K/4/1/X

PIN7-->20mil
PIN1-->6mil
PIN2-->6mil
PIN5-->6mil
PIN3-->6mil

MOSFET請依MOSFET使用規則,自行選擇
ON-->10IF9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]
VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKSO8/2070pF/4.3m]

5VDUAL
MA_L2 47/4030/15A/S
BEAD
MA_DC6 0.1u/4/X7R/16V/K Close Choke
MA_DC25 68p/4/NPO/50V/J/X
MA_VIN
MA_DC7 1u/6/X7R/16V/K Close MOS
MAEC1 560u/FP/D/6.3V/69/A/7m

DDR VIN CAP
560u*2PCS

CHOKE與CAP料號可變

1uH/35A/IMD109/M/D

MA_DQ1 NTMFS4C06N/N/PPAK/1400pF/4m/[10IF9-040406-10R]
MA_UGATE MA_DR1 2.2/6 MA_UG
MA_DR2 8.2K/4
MA_PHASE
MA_DQ2
MA_LGATE MA_DR9 2.2/6 MA_LG
NTMFS4C06N/N/PPAK/1400pF/4m/[10IF9-040406-10R]
MA_L1 1uH/35A/IMD109/M/D/[11LC5-M3100B-41R_11LC5-M3100B-42R]
R50
10*10
VDDQ
MA_DR5 2.2/6
MA_DC5 1n/4/X7R/50V/K
MA_DC14 22p/4/NPO/50V/J/X
RS
MA_DR13 1K/4/1
L=1u
DCR=2.5 mohm
Isat=35A
Idc=28A
MAC60 22u/6/X5R/6.3V/M
請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件
Remote sense請從最重的負載端點拉回
1H1L規格移除
DDR_ADJ
60 DDR_ADJ
1.35V
1.25V
1.4V
RO
MA_DR12 1.4K/4/1

SUPPORT DDR4 1.2V
25A MAX

PWR SEQ

For power sequence require

VPP_25V使用8120時上件

MAU1上RT9045時上件(不可MASK)

DDRVTT

VDDQ
NCT3103S/SOP8/2A/[10GL2-203103-01R]
MAC2 1u/4/X5R/6.3V/K
MAR5 1K/4/1
MAU1
VIN GND VREF1 VOUT VREF2 ENABLE VCNTL BOOT_SEL GND
MA_VTT_REF
MAC1 0.01u/4/X7R/50V/K
MAR4 1K/4/1
1.1A MAX
DDRVTT
DDRVTT_EN
DDRVTT_BOOT
5VDUAL
MAC7 10u/6/X5R/6.3V/M

DDR CAP

560u*4PCS 22u*2PCS

VDDQ
Footprint
EC6D8MM-RH-2
MAEC3 560u/FP/D/6.3V/69/A/7m
MAEC4 560u/FP/D/6.3V/69/A/7m
* 大電容 x4

DDRVTT CAP

DDRVTT
MAC4 22u/6/X5R/6.3V/M
* 大電容 x0

4 DDR_VTT_CTL
10,16,32,56 N_SLP_S3
DDR_VTT_CTL MAR110 MASK/0/4/SHT/M/10/X DDRVTT_EN
N_SLP_S3 MAR111 MASK/0/4/SHT/M/10/X DDRVTT_BOOT

GIGABYTE

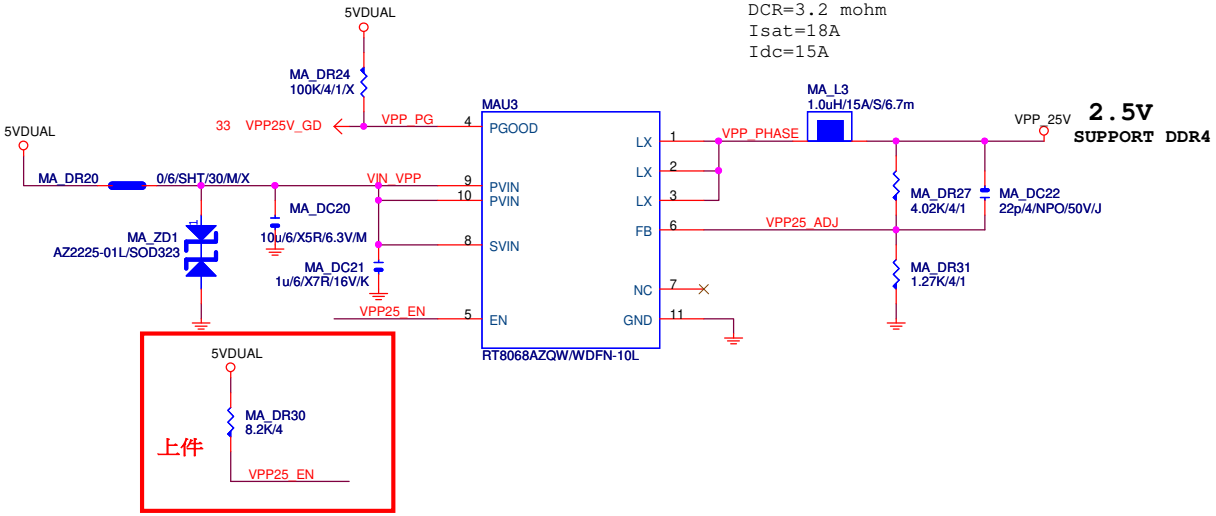
Title	RT8237_DDR4 POWER	
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 33 of 62	

REV:0.1

VPP_25V

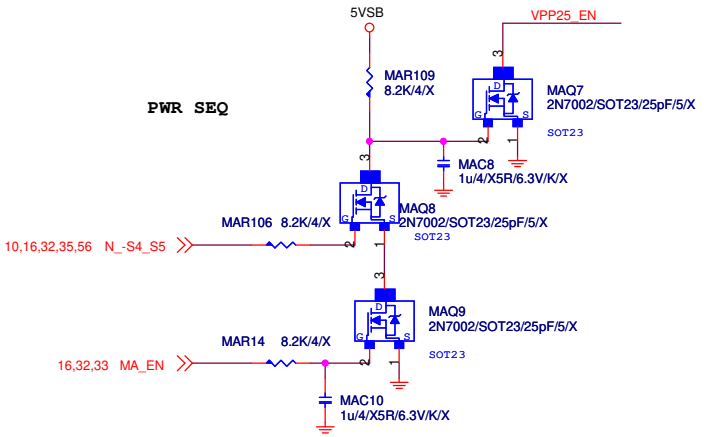
CHOKE與CAP料號可變

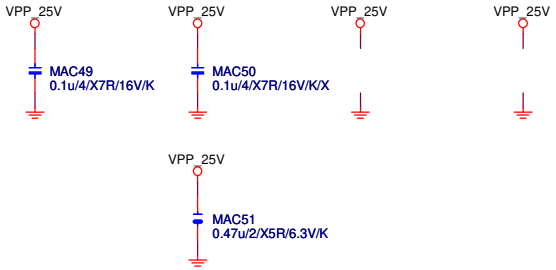
L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A

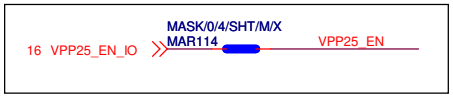


PWR SEQ

* 刪 MA_DR32

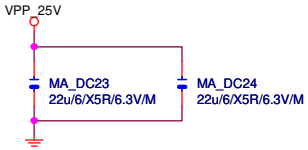






VPP CAP 22u*1PCS

* 大電容 x0

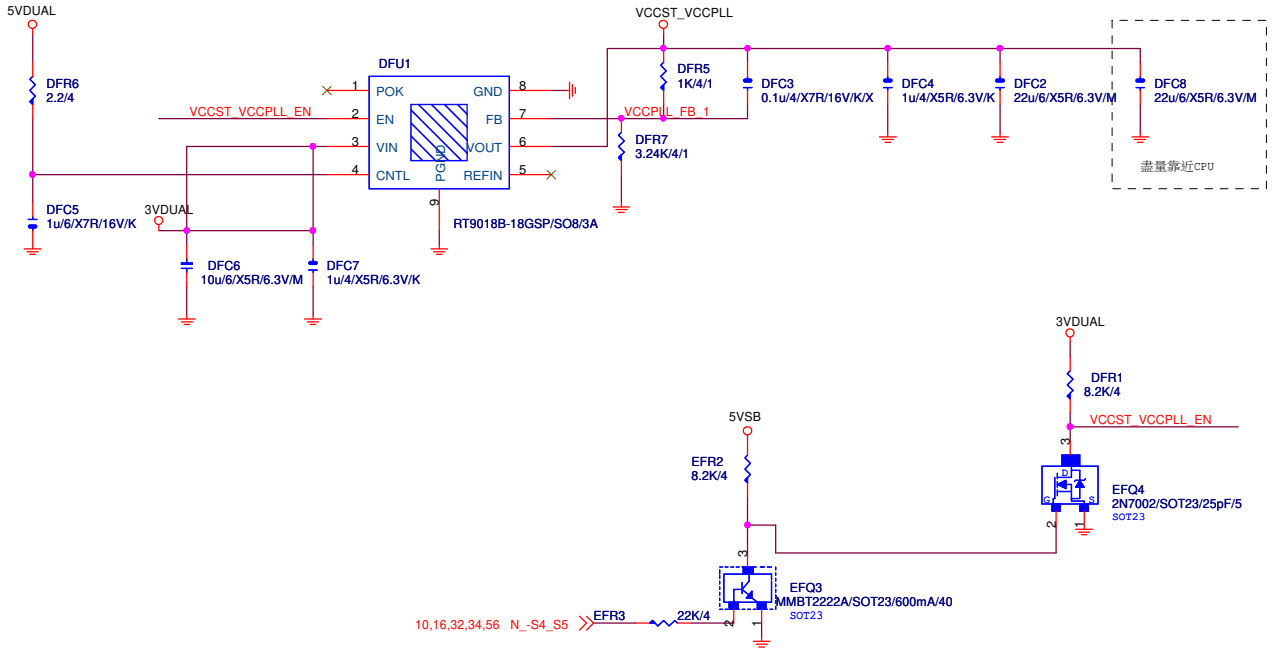


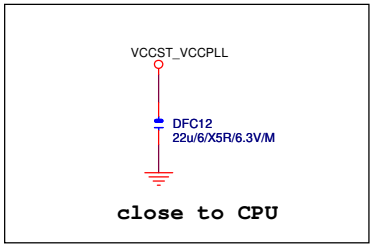
GIGABYTE™

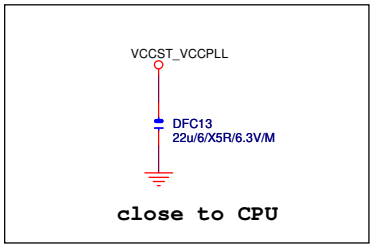
Title: RT8068A_VPP25 POWER		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 34 of 62	

REV:0.12

VCCST_VCCPLL 替換原先MOS開關線路







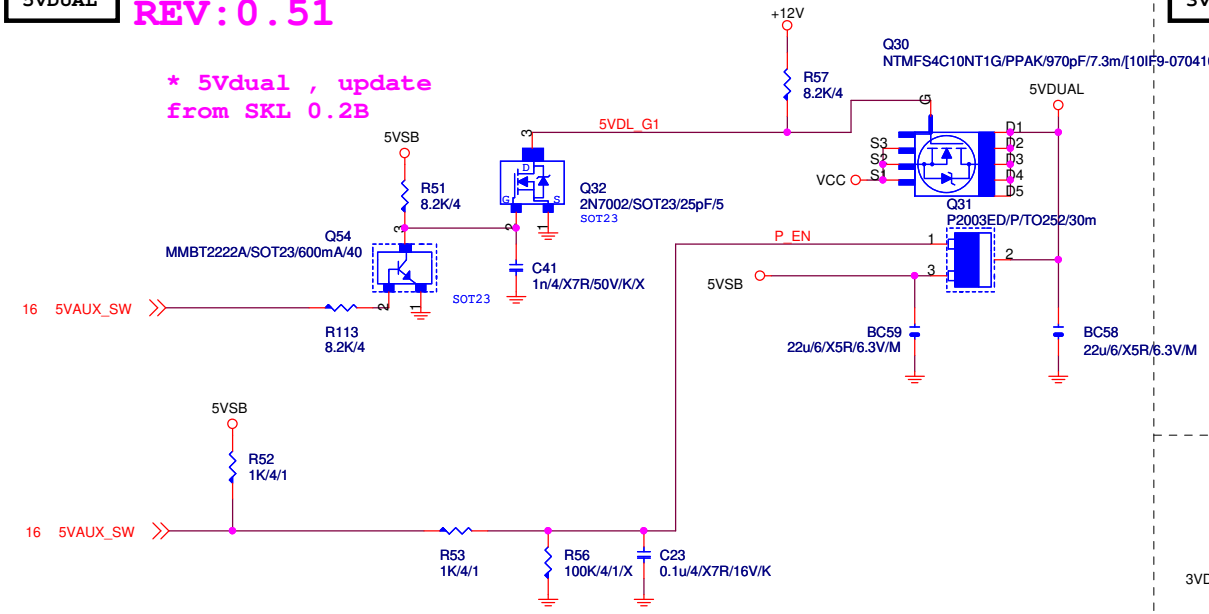
GIGABYTE™

Title: CPU POWER-2		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 35 of 62	

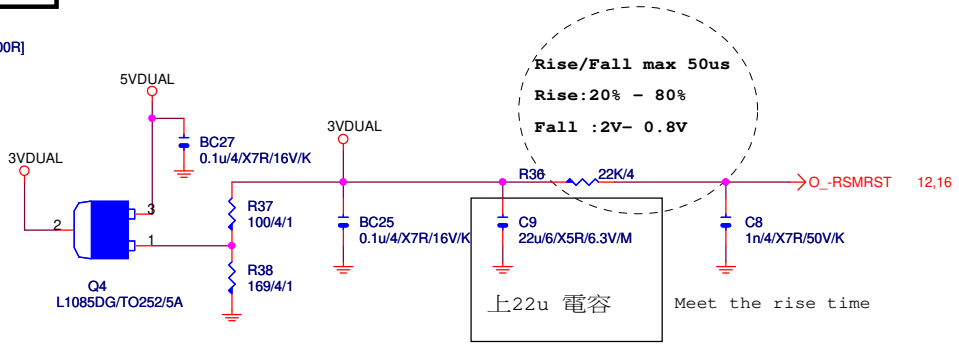
5VDUAL

REV:0.51

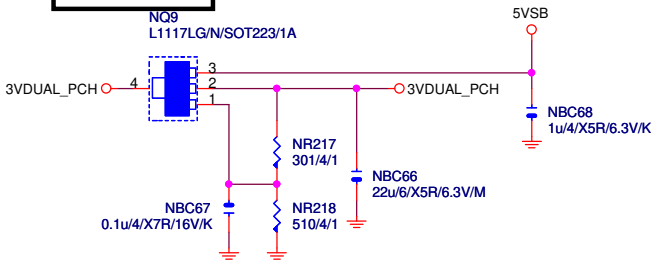
* 5Vdual , update from SKL 0.2B



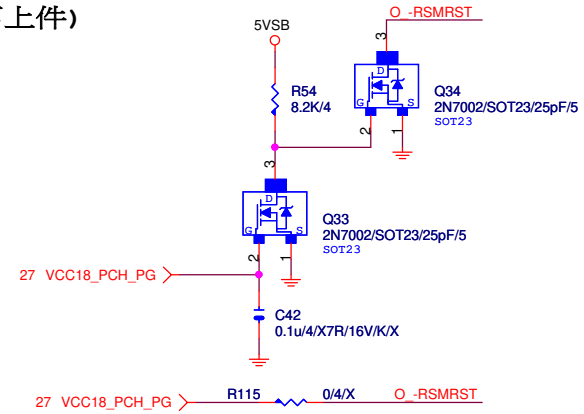
3VDUAL



3VDUAL_PCH



O_-RSMRST （不上件）

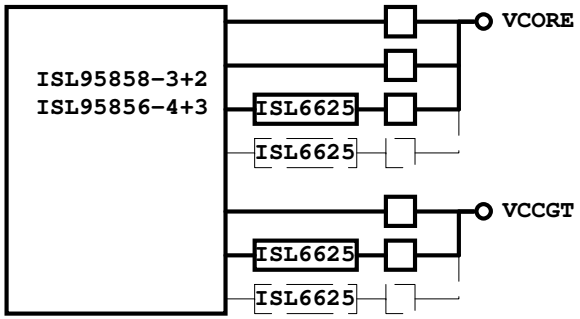


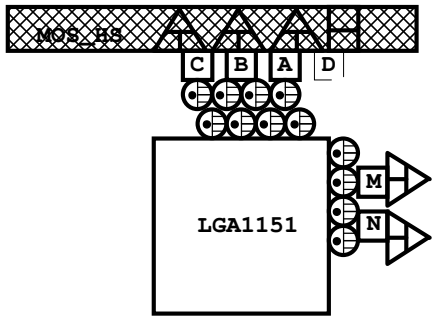
Gigabyte Technology		
Title: DISCRETE POWER		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 36 of 62	

POWER BLOCK MAP

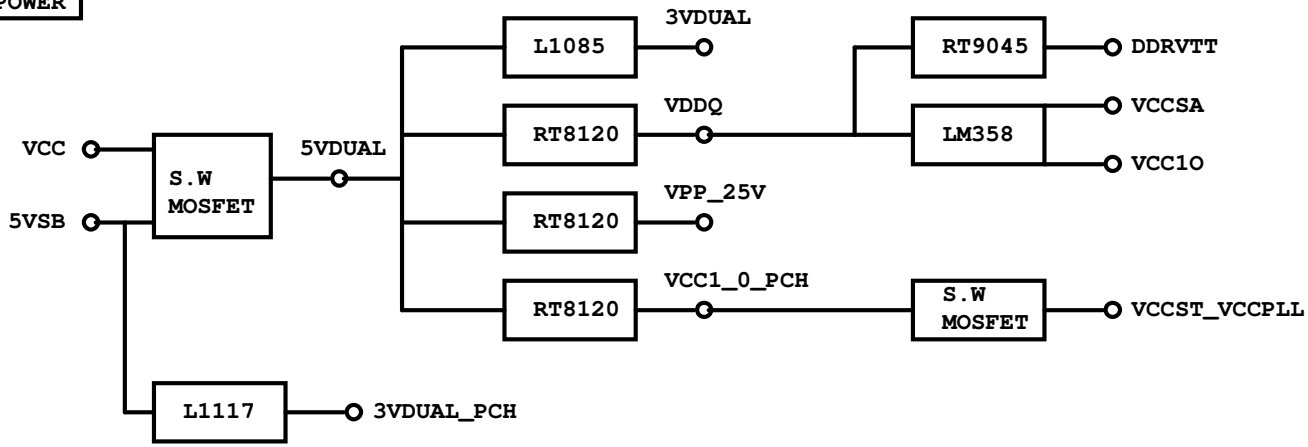
- **CPU**
  - VCORE
  - VCCGT
  - VCCSA
  - VCCIO
  - VDDQ
  - VCCST_VCCPLL
  - VCCSFUSEPRG
- **DDR4**
  - VDDQ
  - DDRVTT
  - VPP_25V
  - VDDSPD(VCC3)
- **PCH**
  - VCC1_0_PCH
  - VCC1_0_PCH_DSW
  - VCC10_VCCF24_1P0
  - VCC10_VCCAMPHYPLL
  - VCC10_VCCAPLL
  - VCC3_PCH
  - 3VDUAL_PCH
  - VCC3
  - N_RTCVDD
- **IT8628**
  - IT_VCCH
  - IT_AVCC
  - 2_5LEVEL
- **HM**
  - +12V
  - VCC
  - VCC3
  - VCORE
  - VCCGT(IMON_VCCGT)
  - VDDQ
  - VCCSA(IMON_VCORE)

VCORE/VCCGT

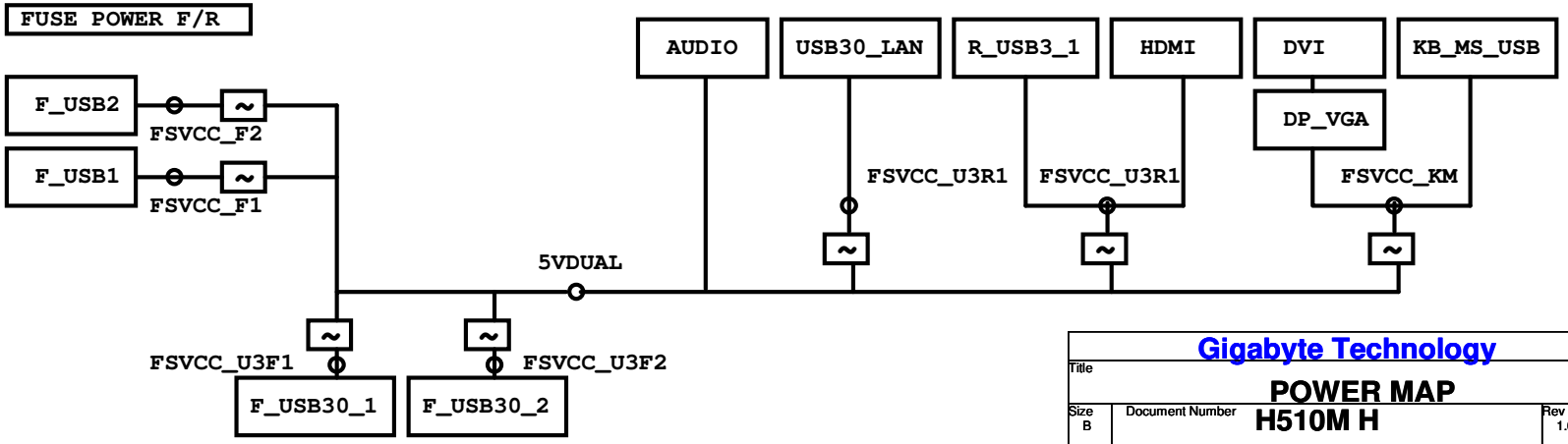




POWER



FUSE POWER F/R



Gigabyte Technology

Title	POWER MAP	
Size B	Document Number H510M H	Rev 1.0
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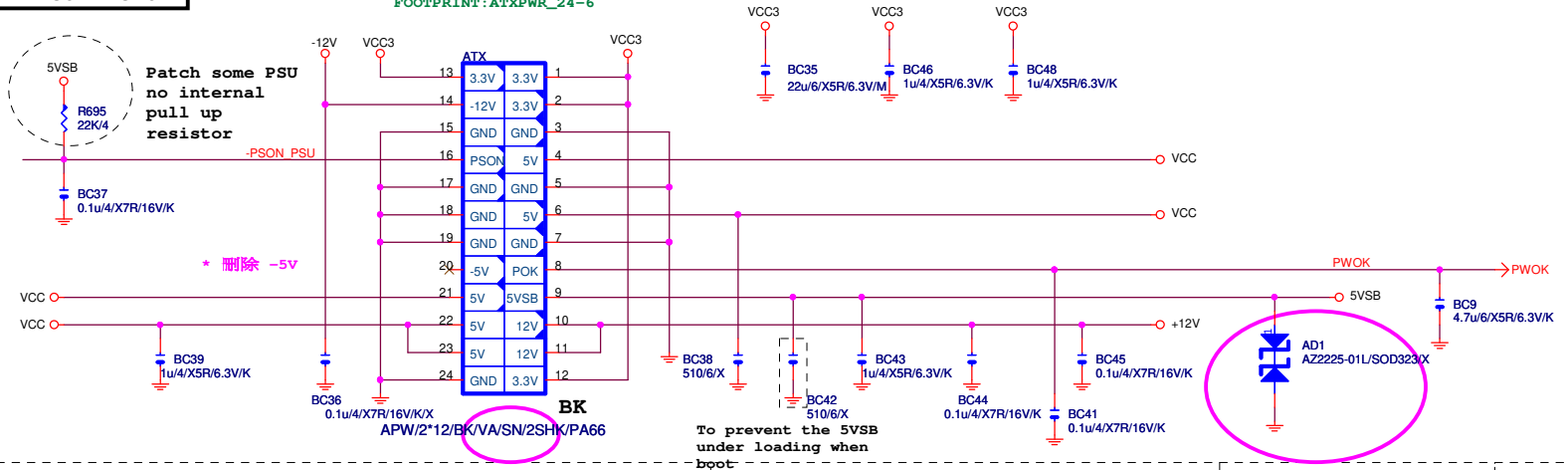
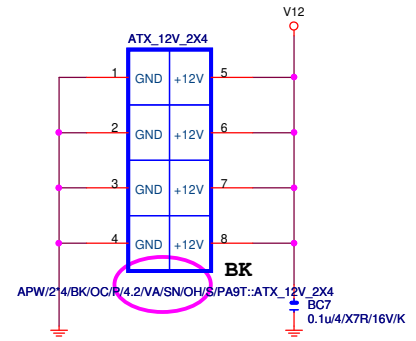
ATXX24 POWER CONNECTOR

2x12 (空心Pin)
FOOTPRINT:ATXPWR_24-6

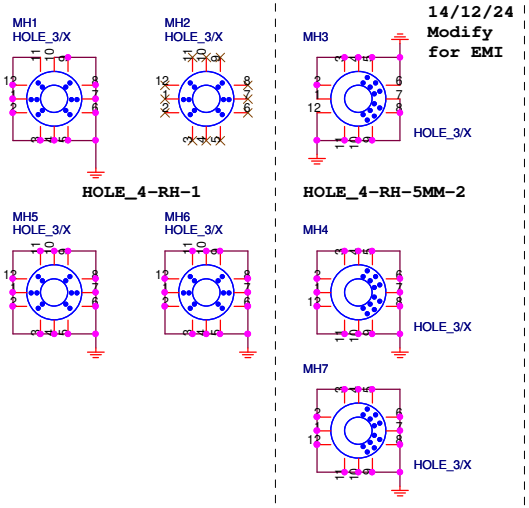


ATXX4 POWER CONNECTOR

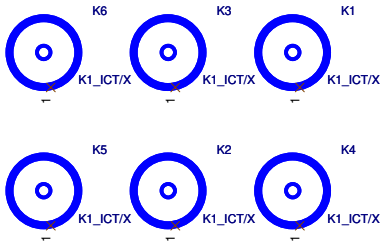
2x4 (空心Pin)
FOOTPRINT:ATXPW2X4-SOLID

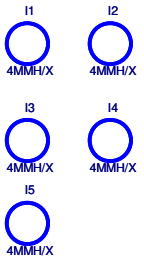


螺絲孔



固定孔/光學點

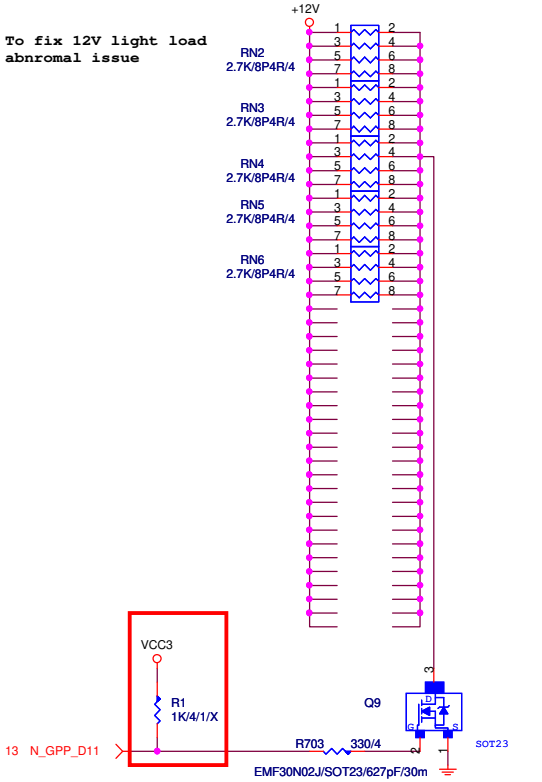




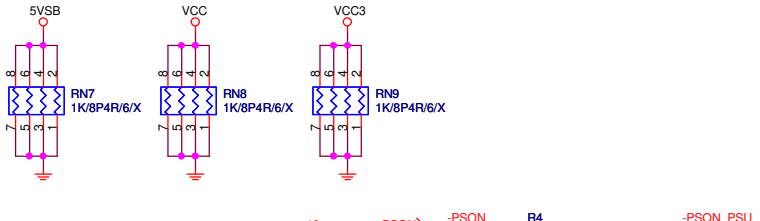
+12V DUMMY LOAD

【技術通報R&D技術通報153】

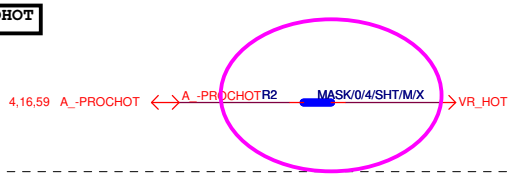
To fix 12V light load abnromal issue



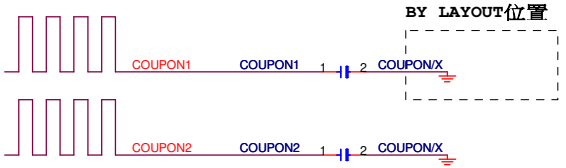
DUMMY LOAD



-PROHOT



COUPON



Gigabyte Technology			
Title: ATX POWER CONNECTOR			
Size: Custom	Document Number: H510M H		Rev: 1.0
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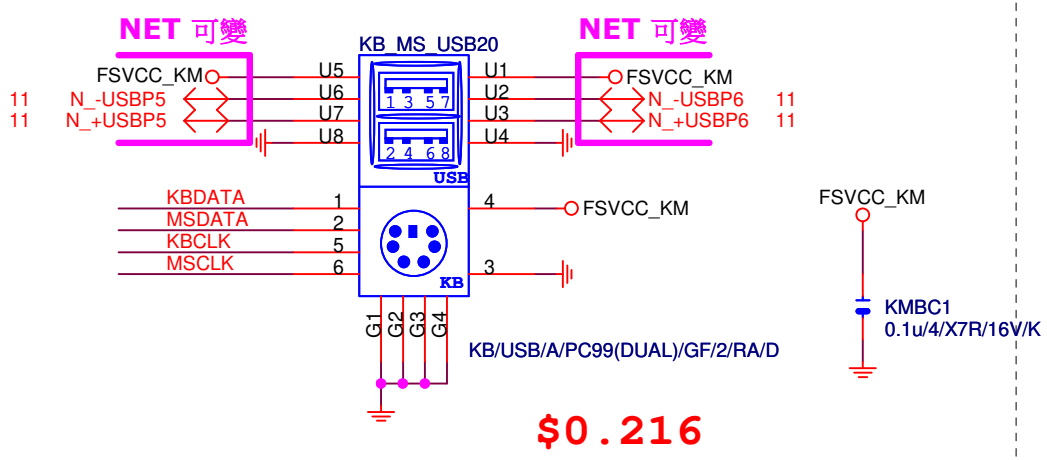
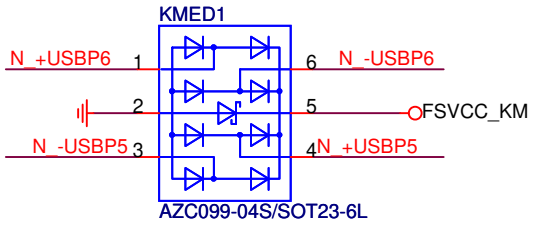
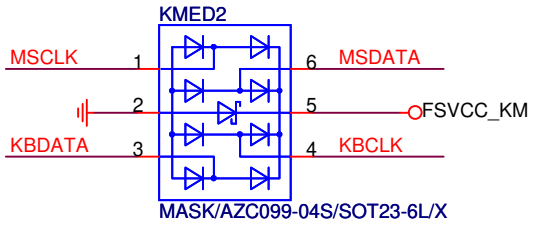
KB_MS_USB



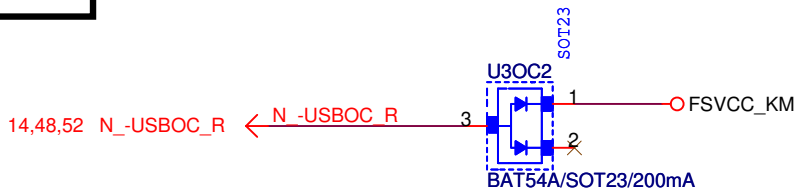
$0.216

ESD



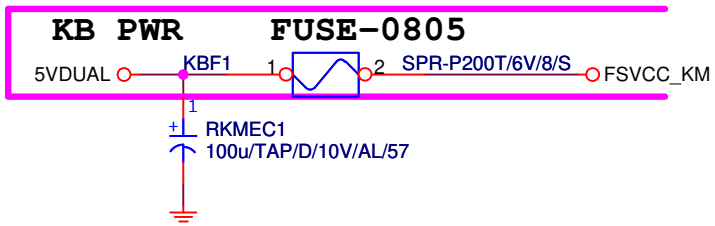


USB OC PROTECT

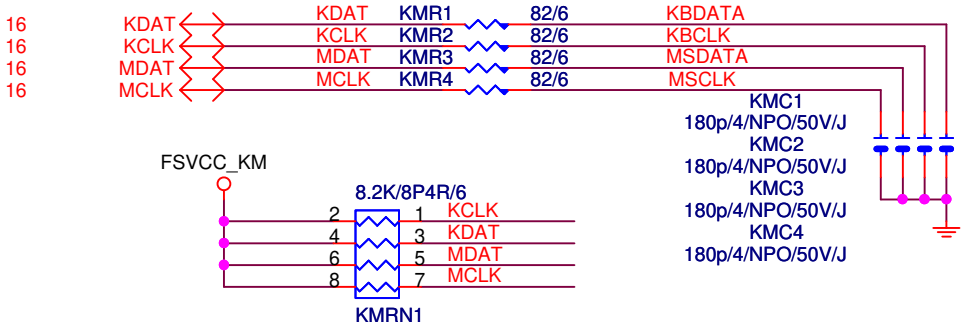


KB_MS_USB PWR

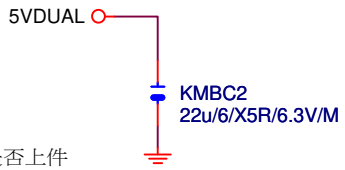
NET 可變, 與其他USB SHARE



KB_MS_USB DAMPING/PU



USB OC PROTECT



確認電壓ripple後決定是否上件

Gigabyte Technology			
Title: KB_MS			
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Gigabyte Technology

Title: DVI

Size: Custom | Document Number: H510M H | Rev: 1.0

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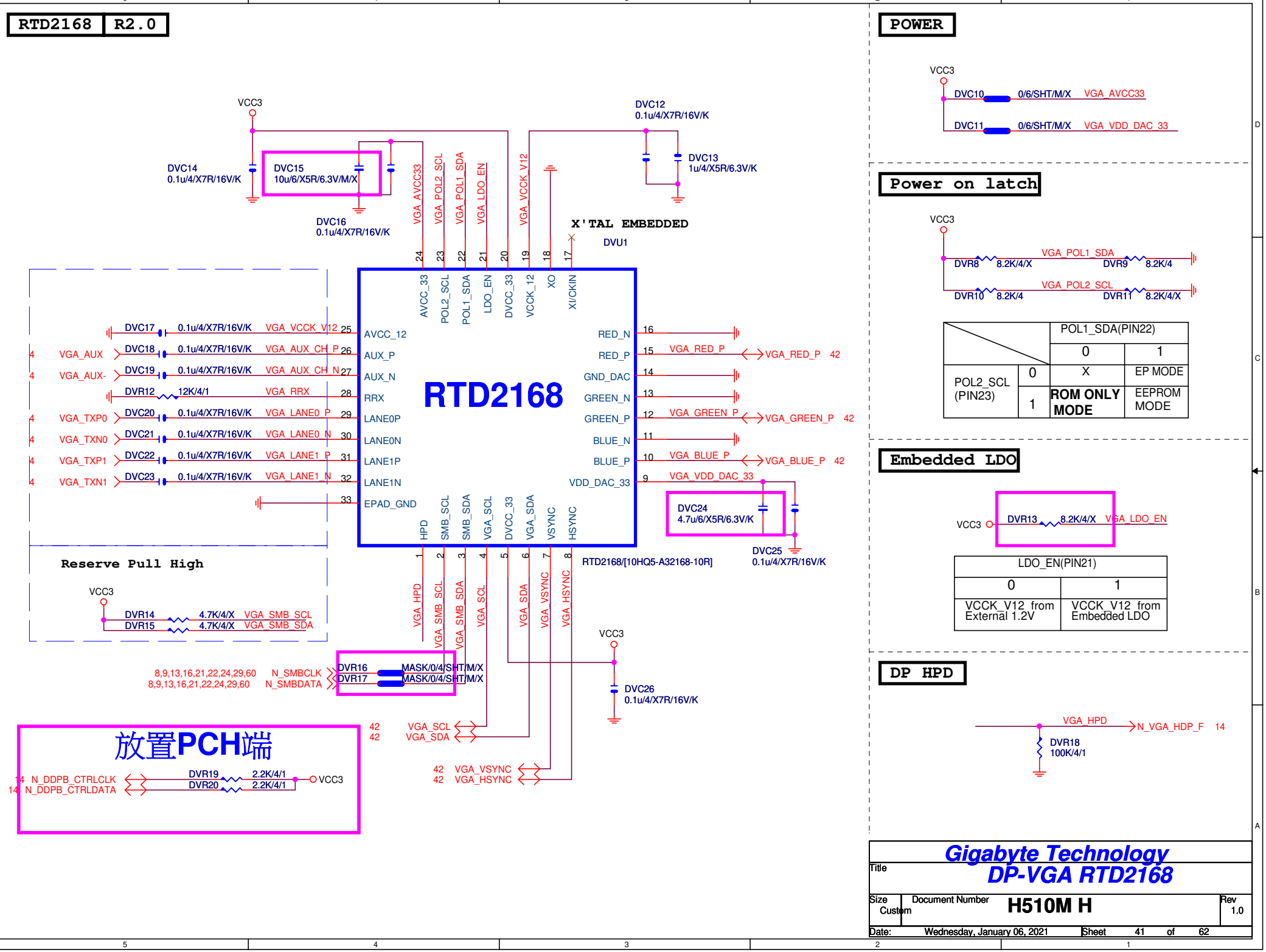
RTD2168 | R2.0



POWER

Power on latch

		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	**ROM ONLY MODE**	EEPROM MODE

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD

Title	Gigabyte Technology DP-VGA RTD2168		
Size Custom	Document Number H510M H		Rev 1.0
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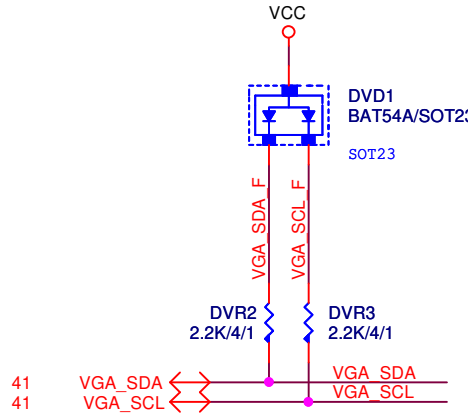
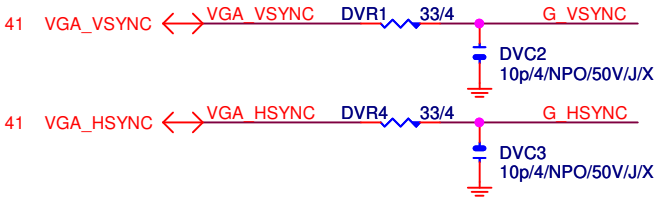
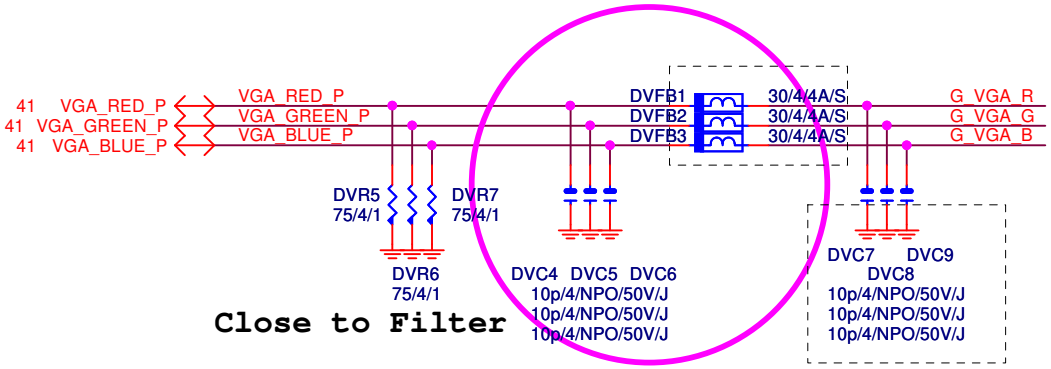
VGA SIGNAL R2.0

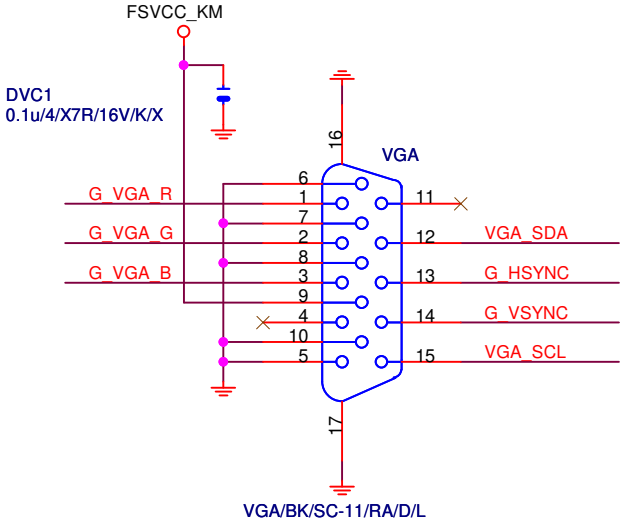




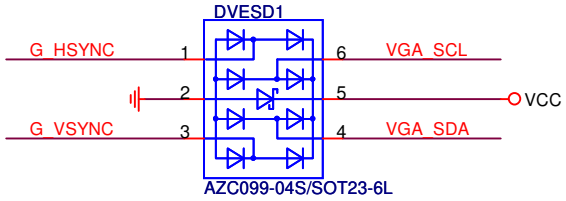


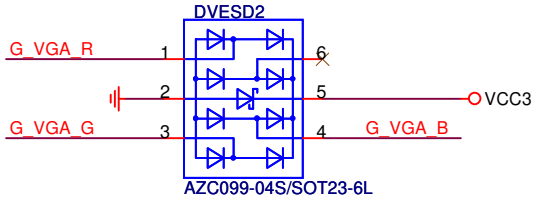
FOR EMI

VGA CONN.



VGA ESD





Gigabyte Technology

Title: DP-VGA RTD2168

Size: Custom | Document Number: H510M H | Rev: 1.0

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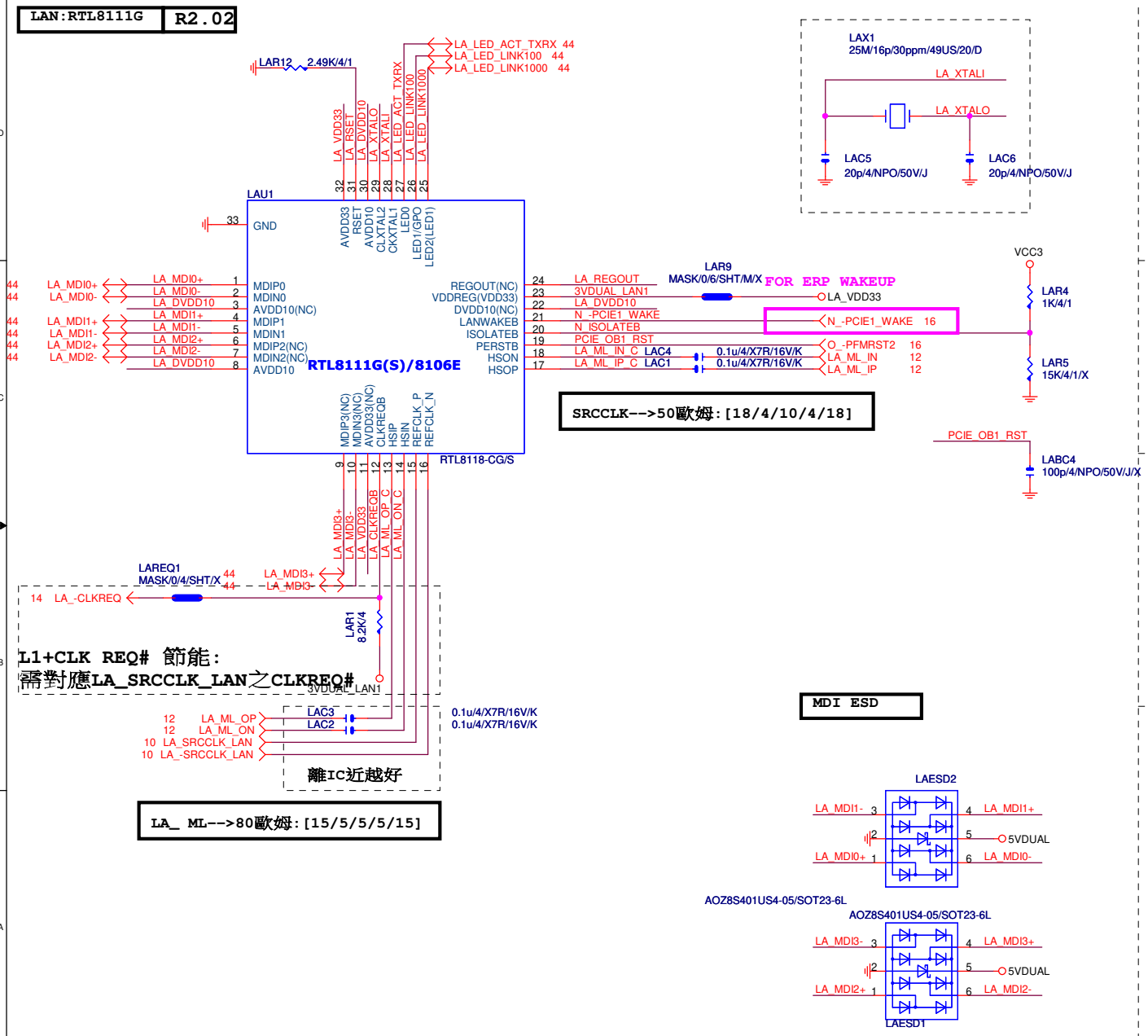
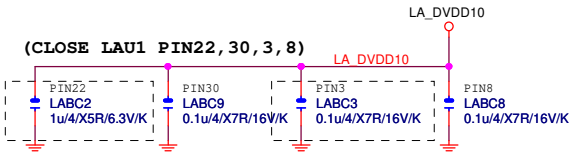
LAN:RTL8111G R2.02



MDI ESD

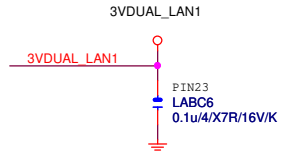
LAN POWER



LABC2:1U CLOSE PIN22[REALTEK REQ]

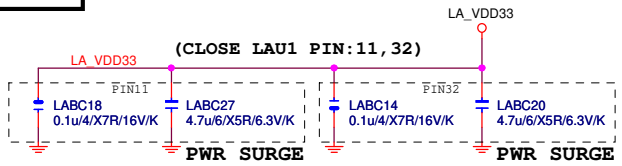
LAN POWER

note: lan power連接及電流



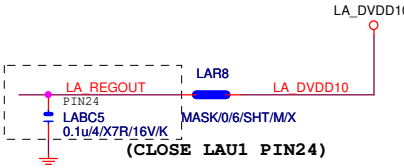
(CLOSE LAU1 PIN23)

LAN POWER



LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]

LAN POWER



Gigabyte Technology

Title: Realtek RTL8111G

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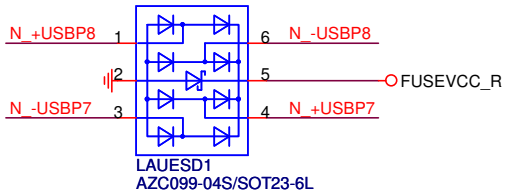
USB_LAN CONNECTOR R2.02

RMA ESD PROTECT

note:可變更USB NAME

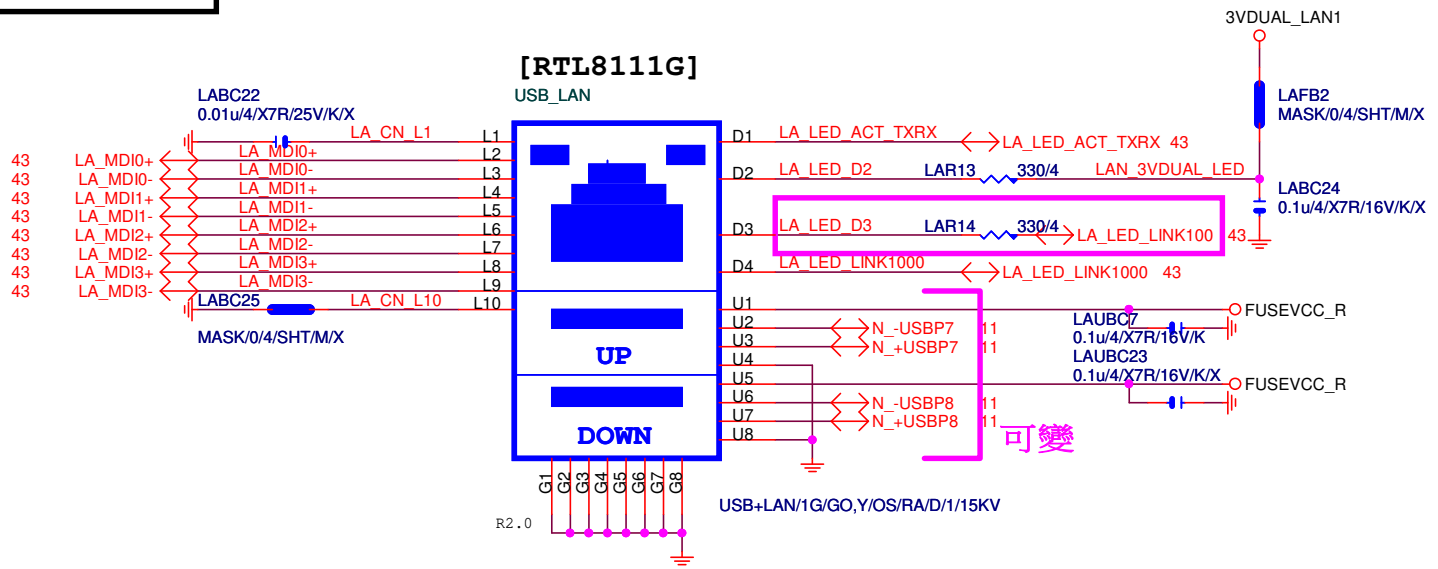
可變



LAUESD1
AZC099-04S/SOT23-6L

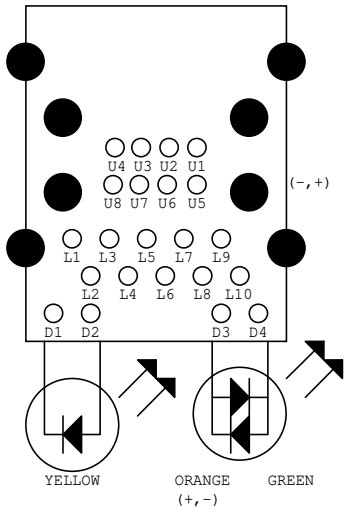
USB_LAN CONNECTOR

note:可變更USB NAME

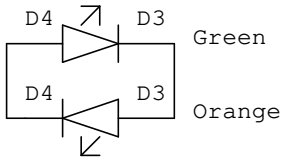


LA_MDI-->100歐姆:[20/4/8/4/20]

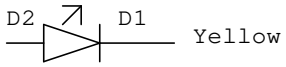
USB_LAN LAYOUT示意圖



Dual Color LED



Single Color LED



USB POWER

note:可變更FUSE

可變

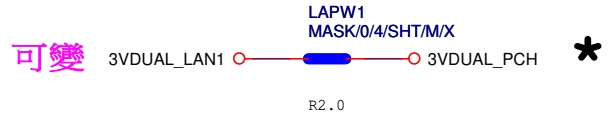
Close to connector

USB_LAN 2-Port 2.0A

FUSE-0805

LAN POWER

note: lan power連接及電流



Gigabyte Technology			
Title: LAN CONNECTOR-RTL8111G			
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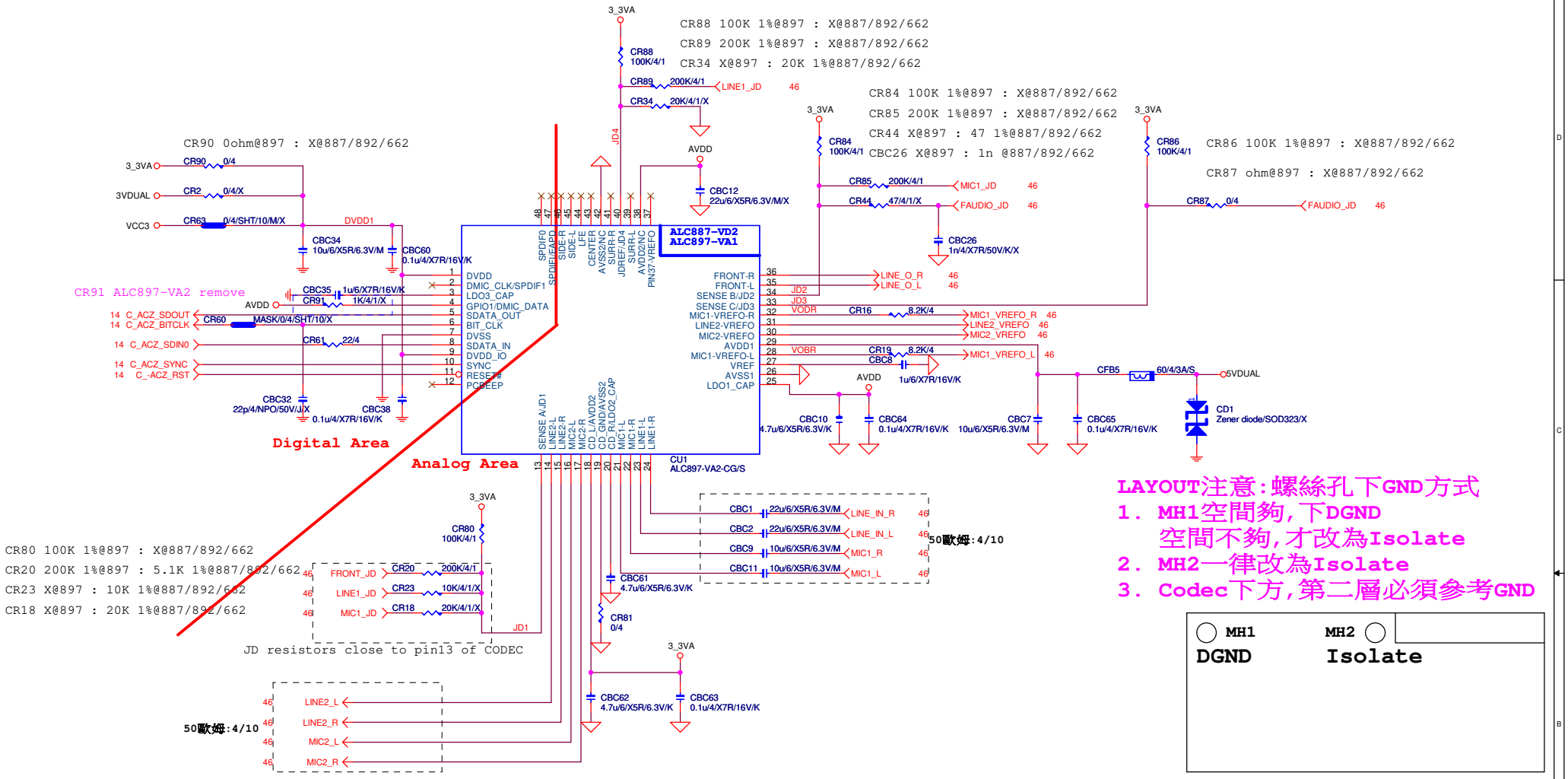

LAYOUT注意:螺絲孔下GND方式

1. MH1空間夠,下DGND
   空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND

MH1	MH2
DGND	Isolate

LAYOUT注意:要加

GND切割線

音效區域印刷

		897	887/892/662
Pin03	LDO3	1uF	10uF
Pin09	DVDD-IO	0.1uF	1uF
Pin18	AVDD2	4.7uF/0.1uF	NC
CR81	AVDD2	0ohm	NC
Pin20	LDO2	4.7uF	NC
Pin25	LDO1	4.7uF	22uF
Pin27	VREF	1uF	10uF
Pin38	AVDD2	NC	22uF

BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

GIGABYTE™

Title	HD AUDIO ALC887	
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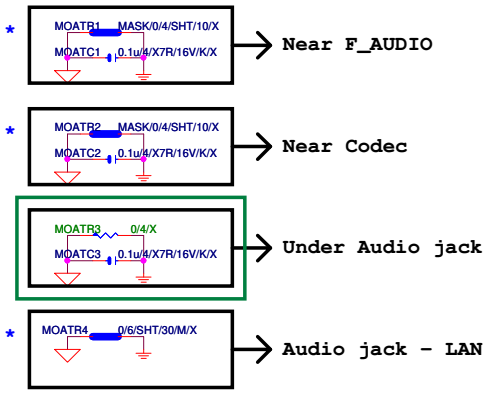
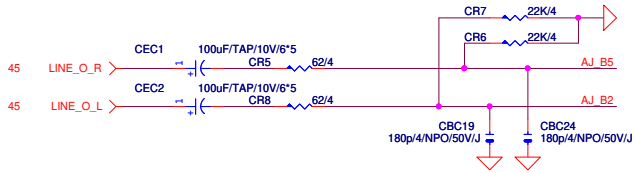
Rev 6.0

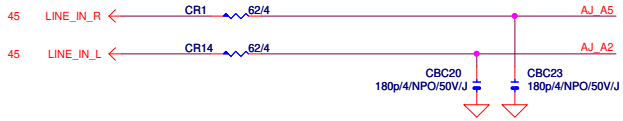


*量產前,MOATR1/MOATR2/MOATR4 ....0ohm改short pad

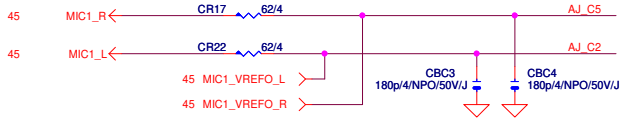
LINE-OUT



LINE-IN



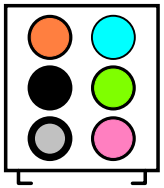
MIC-IN

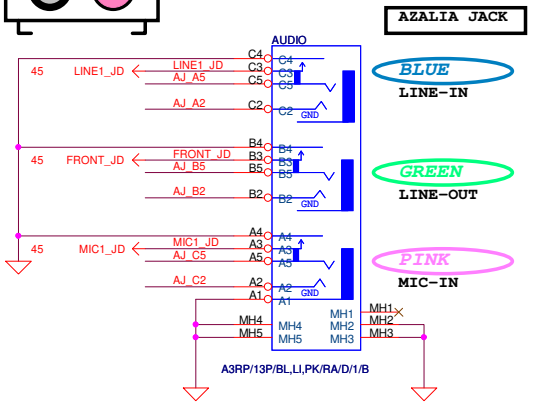


SURROUND

CEN/LFE

AZALIA JACK





AZALIA JACK

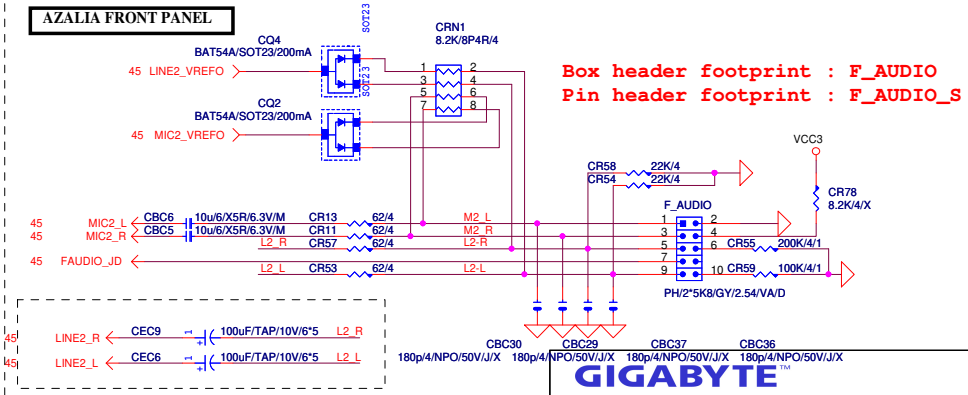
BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN

SURR BACK

AZALIA FRONT PANEL



GIGABYTE™

Title	AUDIO JACK	
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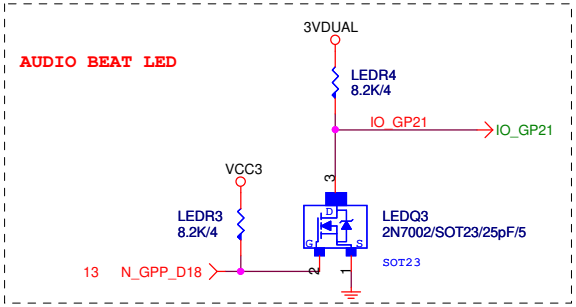
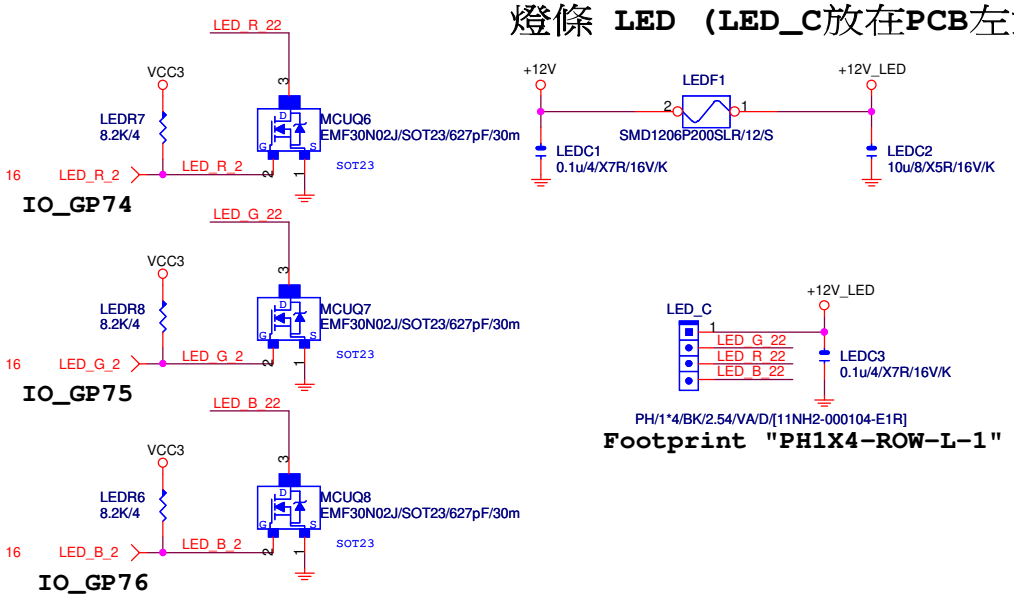
Rev 1.0



第二區 LED CONTROL

燈條 LED (LED_C放在PCB左邊板邊位置)



GIGABYTE™

Title	Amient Single LED		
Size: Custom	Document Number: H510M H		Rev: 1.0
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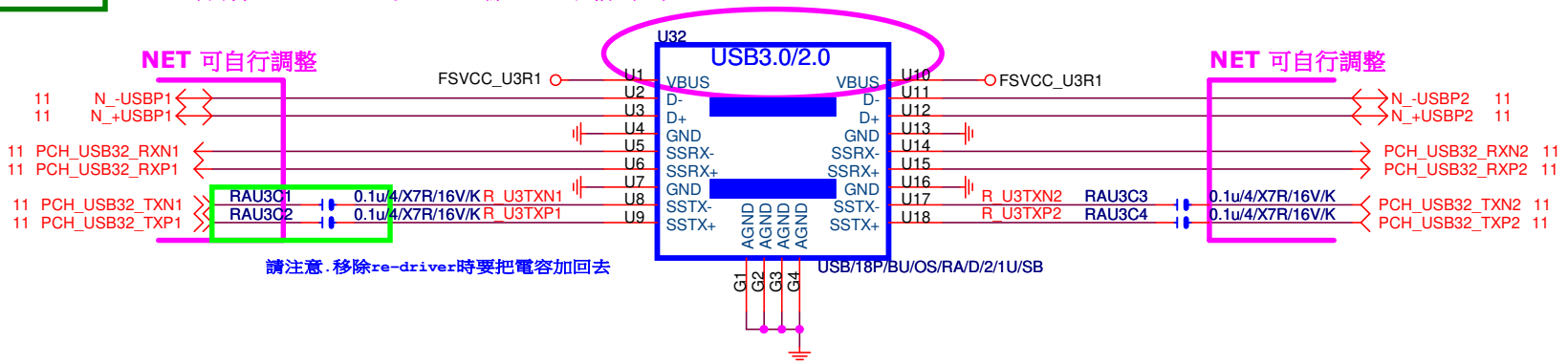
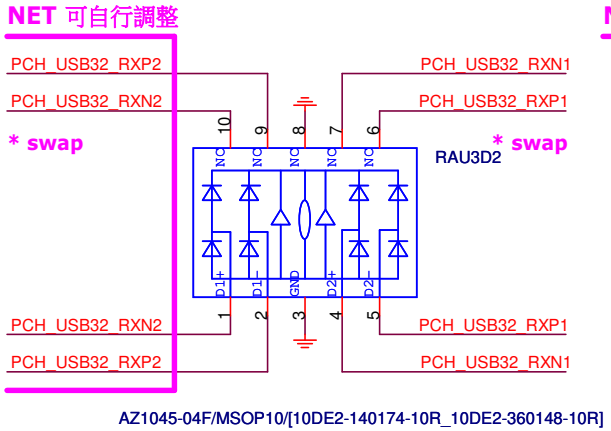
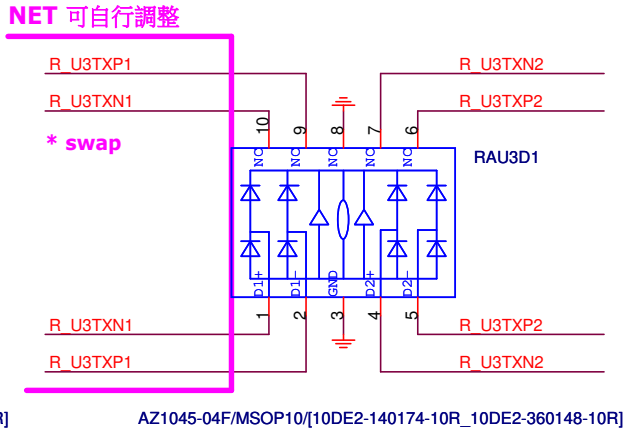
Rev: 0.7

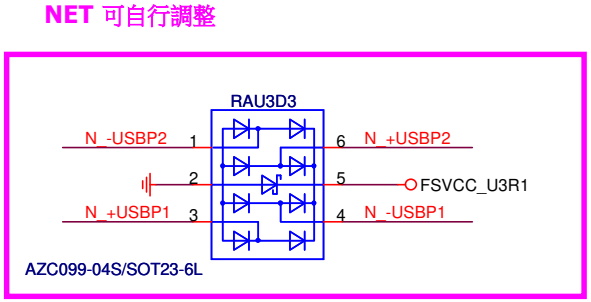
ESD 可自行SWAP PIN ,CONN端 NET 名稱 不可



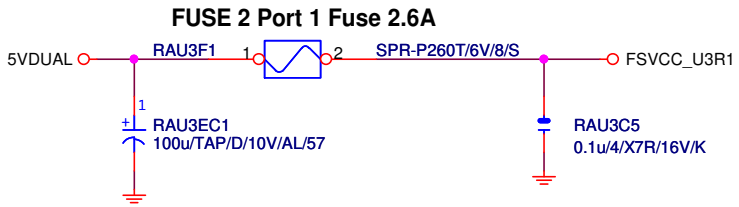
ESD

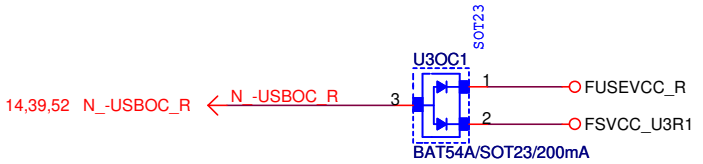






FUSE





Gigabyte Technology		
Title: R_USB30,USB_OC		
Size: Custom	Document Number: H510M H	Rev: 1.0
Date: Wednesday, January 06, 2021	Sheet 48 of 62	

Gigabyte Technology

Title

R_USB30,USB_OC

Size	Document Number	Rev
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Gigabyte Technology

Title: FP,F_USB,USB PWR,BZ

Size: Custom | Document Number: H510M H | Rev: 1.0

Date: Wednesday, January 06, 2021 | Sheet 50 of 62

GIGABYTE™

Title
PI3EQX1002B Redriver/DC-J

Size	Document Number	Rev
Custom	H510M H	1.0

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Rev: 0.7

Front USB3.0

NET 自行調整

F_U32 REV=1

BH/2*10K20/BK/ON/2.0/V/AUSB3.0/PRT

NET 可自行調整

NET 可自行調整

F_USB30 PWR

5VDUAL — FAU3F1 — SPR-P260T/6V/8/S — FSVCC_U3F1

FAU3EC1 100u/TAP/D/10V/AL/57

FAU3C5 0.1u/4/X7R/16V/K

U3OC3 SOT23 BAT54A/SOT23/200mA

NET 可自行調整

NET 可自行調整

FAU3D1 AZ1045-04F/MSOP10/[10DE2-140174-10R_10DE2-360148-10R]

FAU3D3 AZC099-04S/SOT23-6L

CLOSE F_USB30

FAU3D2 AZ1045-04F/MSOP10/[10DE2-140174-10R_10DE2-360148-10R]

CLOSE F_USB30

-USBOC_F

POWER 可自行調整

FSVCC_U3F1 — UAR1 8.2K/4 — N_-USBOC_F — N_-USBOC_F 14

UAR2 15K/4/1

-USBOC_R

POWER 可自行調整

FSVCC_U3F1 — UBR1 8.2K/4 — N_-USBOC_R — N_-USBOC_R 14,39,48

UBR2 15K/4/1

* 接 PCH N_GPP_G7(SMI) & PCH PU 3Vdual

13 N_GPPC_G7

UAD5 SOT23 BAT54A/SOT23/200mA

Gigabyte Technology		
Title: R_USB30,F_USB30, USB_OC		
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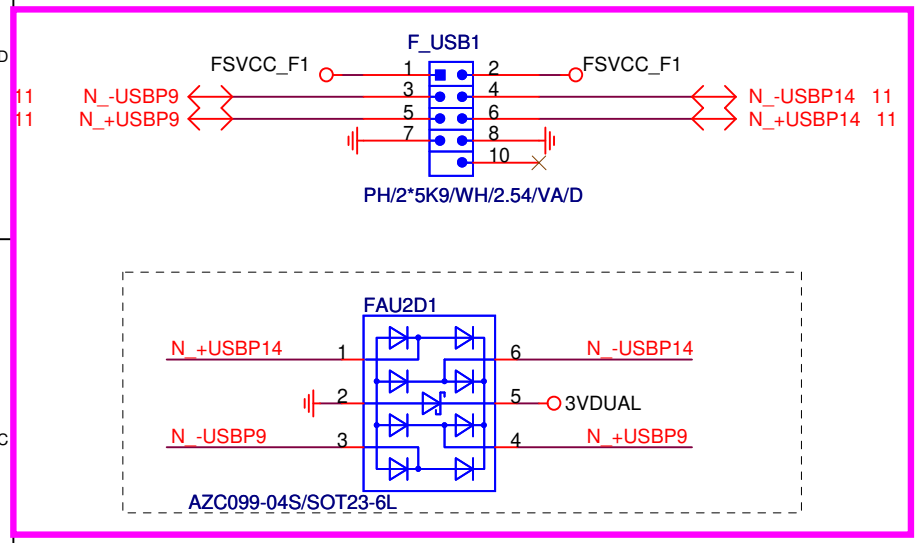
Rev: 0.7

FRONT USB1

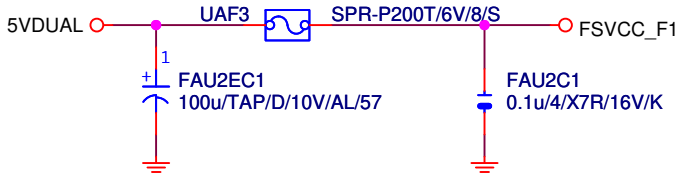
NET 可變

FUSB2X5-HS



Close to connector

FUSE 2 Port 1 Fuse 2A



F_USB 2.0 OC SIGNAL

Gigabyte Technology			
Title: USB2.0			
Size: A	Document Number: H510M H		Rev: 1.0
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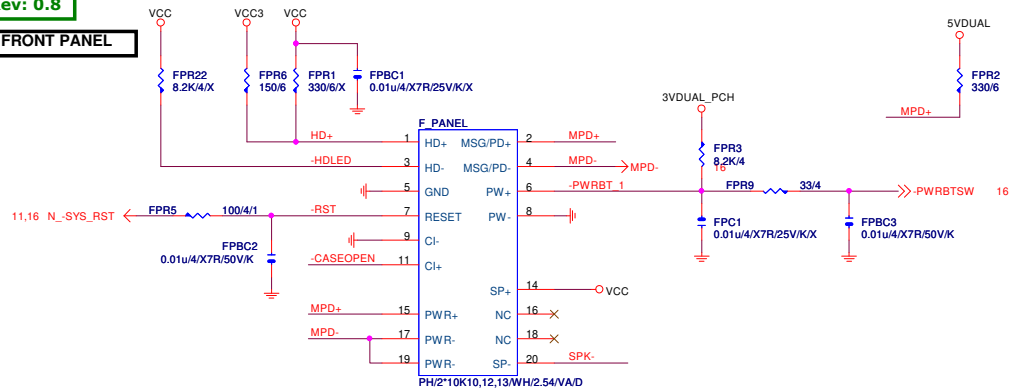
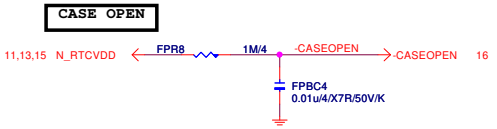
Rev: 0.8

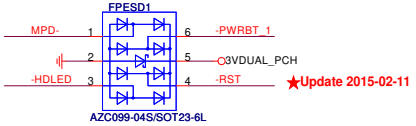
FRONT PANEL

★Update 2016.06.15



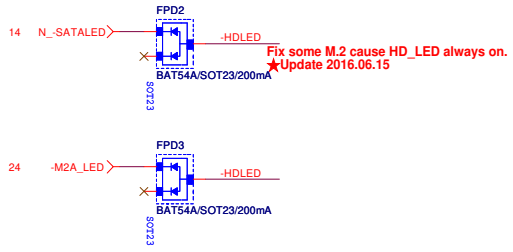
CASE OPEN





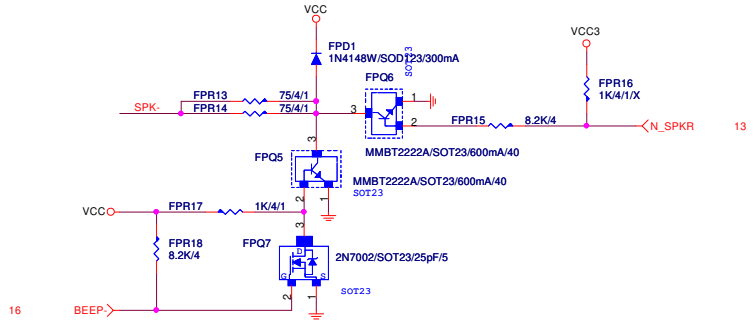
★Update 2015-02-11

SATA/M.2 LED



Fix some M.2 cause HD_LED always on.
★Update 2016.06.15

SPKR



For SPKR voltage issue. FPQ6=>2222, FPQ7=>7002

FRONT PANEL SHORT

Gigabyte Technology		
Title: FRONT PANEL		
Size: Custom	Document Number: H510M H	Rev: 1.0
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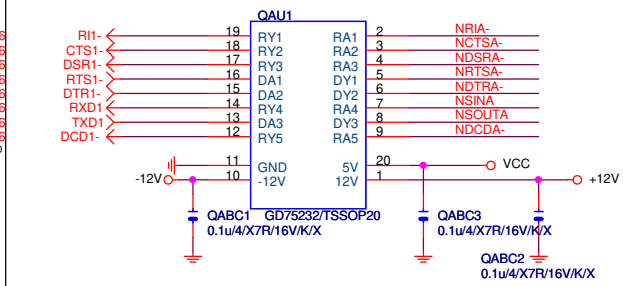
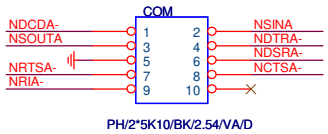
COM PORT

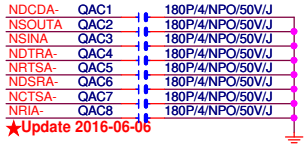
Rev: 0.7





PH/2*5K10/BK/2.54/VA/D

F_COM-HS



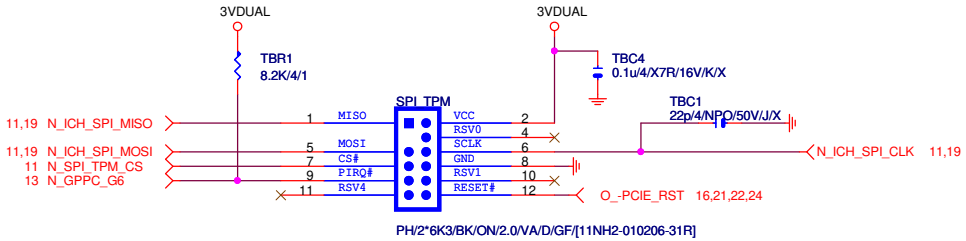
★Update 2016-06-06

LPT PORT

COM RI

N/A

TPM CONNECT



PH/2*6K3/BK/ON/2.0/VA/D/GF/[11NH2-010206-31R]

Footprint: TPM2X6-CUT3(2mm)

Gigabyte Technology		
Title: FP,F_USB,USB PWR,BZ		
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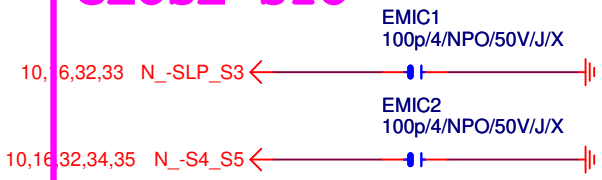
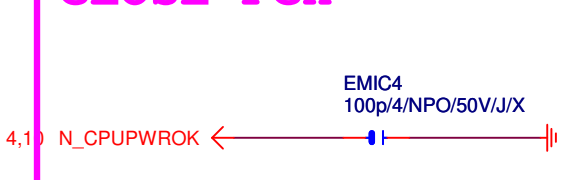
EMI/ESD R0.1

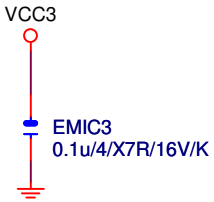
CLOSE SIO



CLOSE PCH



CLOSE NR47



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Title	EMI/ESD	
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VCCIO

RKL MODIFY

REV:0.12

5VDUAL

DFR11 2.2/6

DRV_VIO

DFC11 1u/6/X7R/16V/K

VCC

DFR10 100K/4/1

VCCIO_PG

VCC3

DFR25 8.2K/4

VCCIO_EN_1

DFR18 169K/4/1 VCCIO_CS

VCCIO0_MODE

DFU2

RT6541AGQW/WDFN-14L

VCC UGATE BOOT PHASE LGATE LPM RGND FB G0 G1 MODE CS GND PGOOD EN

UGATE_VIO

VCCIO_BOOT DFR19 0/6 DFC10 0.1u/6/X7R/25V/K

PHASE_VIO

LGATE_VIO

VIO_LPM DFR20 0/4 CPU_VCCIO_PWR_GATEB 14,32,58

VIO_RGND

VCCIO0_G0

VCCIO0_G1

VIO_VSA_RGND DFR35 0/4/X VSSSA_VIO_SENSE 6,59

請盡量靠近分支點

RKL MODIFY

VCC1V8_PRIM

DFR24 8.2K/4/X

VIO_LPM

DFR26 0/4

DFR34 0/4/X VIO_VSA_RGND

放置靠近output cap端

使用GPIO超壓

1. DFR26須改為100/4/1
2. DFR34需上件

+12V

L=1u
DCR=6.7 mohm
Isat=15A
Idc=12A

CHOKE與CAP料號可變

注意耐壓

DCL1 6*6 47/4030/15A/S

BEAD

Close Choke

DFC36 0.1u/4/X7R/16V/K

DFC37 0.1u/4/X7R/16V/K

DFC39 0.1u/4/X7R/16V/K

DFC27 68p/4/NPO/50V/J/X 0.1u/4/X7R/16V/K

VCCIO_VIN

DFC9 1u/6/X7R/16V/K Close MOS

DFC24 10u/8/X5R/16V/K

DFC25 10u/8/X5R/16V/K

DFC26 10u/8/X5R/16V/K

DFQ5

NTTFS4C10NTAG/WDFN8/993pF/7.4m/[10IF8-060088-01R_10IF8-073908-01R]

UGATE_VIO DFR12 2.2/6 UG_VIO

DFR13 8.2K/4

PHASE_VIO

LGATE_VIO

DFQ6

NTTFS4C10NTAG/WDFN8/993pF/7.4m/[10IF8-060088-01R_10IF8-073908-01R]

DFL2 1.0uH/12A/15A/S/7.4 6*6

L=1u
DCR=6.7 mohm
Isat=15A
Idc=12A

DFR15 2.2/6

DFC14 1n/4/X7R/50V/K

VCCIO

使用GPIO超壓須移除

DFR16 487/4/1/X

DFR17 1K/4/1

DFEC2 560u/FP/D/6.3V/69/A/7m

DFC38 22u/6/X5R/6.3V/M

DFC15 3.3n/4/X7R/50V/K/X

RS

VCCIO_OV

DFR28 100/4/1/X

DFR27 10K/4/1/X

DFR9 0/4/X VCCIO_SENSE 6

使用GPIO超壓須上件

DFC51 47u/8/X5R/6.3V/M/X

DFC52 47u/8/X5R/6.3V/M/X

DFC54 47u/8/X5R/6.3V/M/X

DFC55 47u/8/X5R/6.3V/M/X

放CPU SOCKET (Bottom LAYER)

ADDRESS=2A
VREF=02

VCCIO_EN DFR36 0/4/X VCCIO_EN_1

Connect to IT8795

Connect to IT8686

16,32,58 VCCIO_EN

DCR35 MASK/0/4/SHT/X

DCR22 8.2K/4/X

DCR23 100K/4/1

DCC16 1u/6/X7R/16V/K

DCR21 8.2K/4

DCQ7 2N7002/SOT23/25pF/5

DCQ8 2N7002/SOT23/25pF/5

SOT23

* A_CPU_ID
1: RKL -->VCCIO=1.05V
0: CML -->VCCIO=0.95V

DFR37 8.2K/4/1

A_CPU_ID_N

DFQ1 2N7002/SOT23/25pF/5

DFQ11 2N7002/SOT23/25pF/5

4,58,59 A_CPU_ID

VCCIO0_G1

VCCIO0_G0

VCCIO0_MODE

DFR38 100K/4/1

DFR39 0/4/X

DFR40 100K/4/1

DFR41 0/4/X

DFR14 100K/4/1

DFR42 0/4/X

VCCIO_OV

DFR33 422K/4/1/X VIO_RGND

DFR43 42.2K/4/1

DFR44 21K/4/1

DFR29 100K/4/1/X

DFR31 100K/4/1/X

DFQ2 2N7002/SOT23/25pF/5

DFQ3 2N7002/SOT23/25pF/5

14 VCCIO_VID1

14 VCCIO_VID2

VIO_RGND

DFR30 100K/4/1

DFR32 100K/4/1

DFC28 0.1u/4/X7R/16V/K

DFC29 0.1u/4/X7R/16V/K

VCCIO_VID1-->GPP_F_22

VCCIO_VID2-->GPP_F_23

使用GPIO超壓須上件

VCC3

VCCIO_PG DGR36 MASK/0/4/SHT/X PWRGD

Connector to SIO PIN7

VCCIO_PWRGD 16

DGR3 100K/4/1/X

DGR2 100K/4/1/X

DGR4 100K/4/1

DGQ1 2N7002/SOT23/25pF/5/X

DGQ2 2N7002/SOT23/25pF/5/X

DGQ3 2N7002/SOT23/25pF/5

DGQ4 2N7002/SOT23/25pF/5

DGQ10 2N7002/SOT23/25pF/5

* A_CPU_ID_N
0: RKL
1: CML

A_CPU_ID_N

58 VCCIO2_PG

VCCIO2_PG

VCCIO_VID1	VCCIO_VID2	VCCIO_0_G1	VOUT
LOW	LOW	LOW	0.950V
LOW	LOW	HIGH	1.050V
HIGH	LOW	HIGH	1.075V
LOW	HIGH	HIGH	1.100V
HIGH	HIGH	HIGH	1.125V

Mode	VR	Mode logic	LPM	VID Setting G1 logic	VID Setting G0 logic	VOUT (V)
Mode1	VCCIO	0	0	x	x	0(LPM)
			1	0	0	0.85
			1	0	1	0.875
			1	1	0	0.95
			1	1	1	0.975
Mode2	VPRIMCORE	Floating	0	x	x	0.7V(LPM)
			1	0	0	0.85
			1	0	1	0.9
			1	1	0	0.95
			1	1	1	1
Mode3	VccEDRAM/ VccEOPIO	1	0	x	x	0(LPM)
			1	0	0	0.8
			1	0	1	0.95
			1	1	0	1
			1	1	1	1.05

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Title: VCCIO

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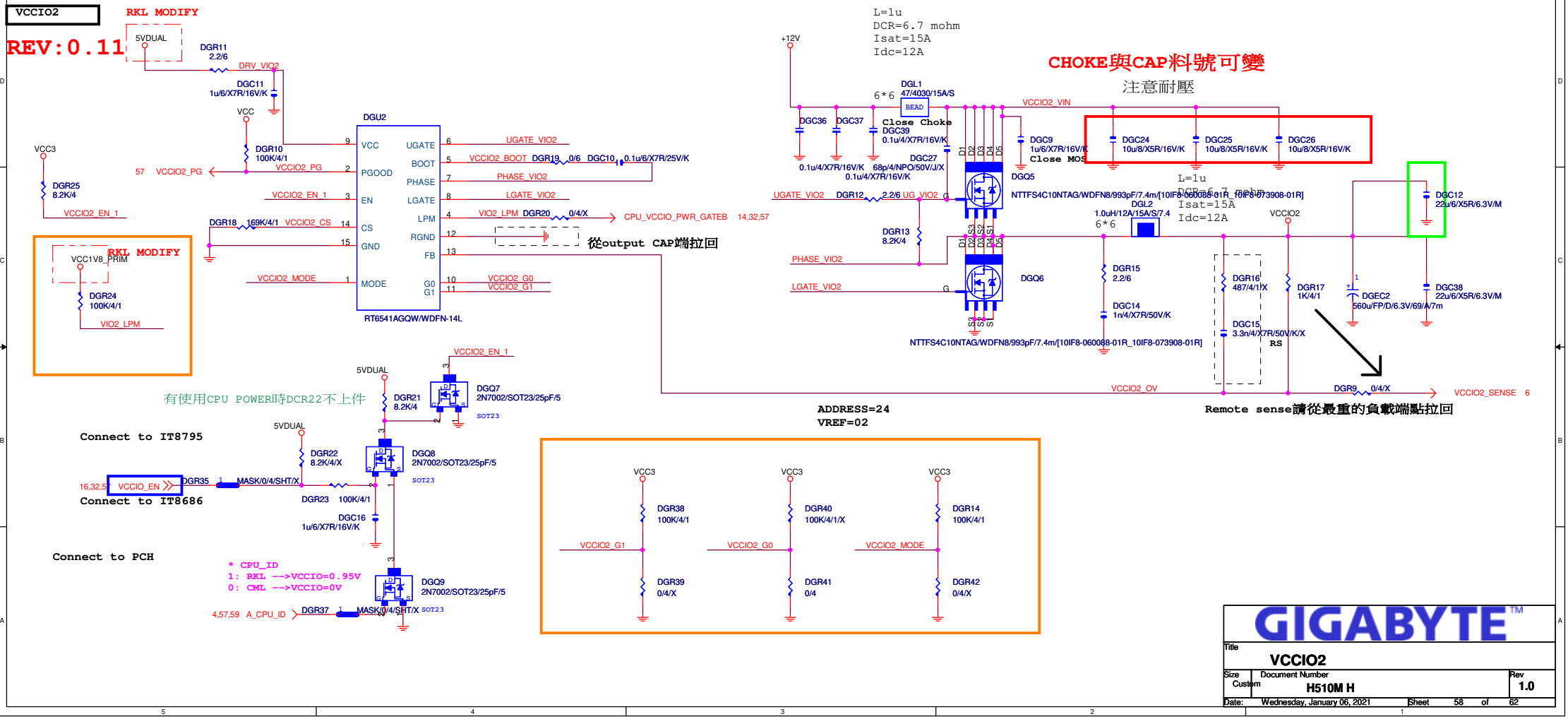
VCCIO2

RKL MODIFY

REV:0.11



Title	VCCIO2		
Size: Custom	Document Number: H510M H		Rev: 1.0
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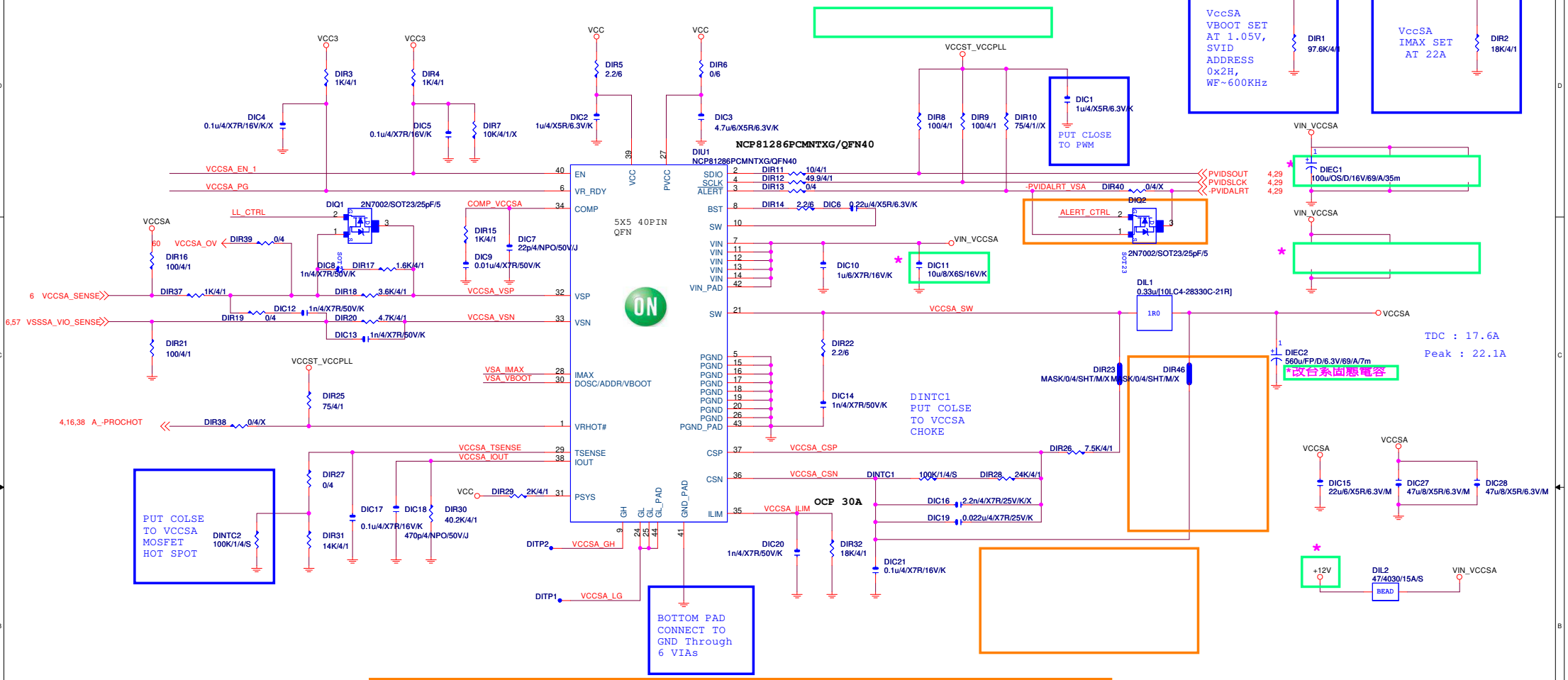
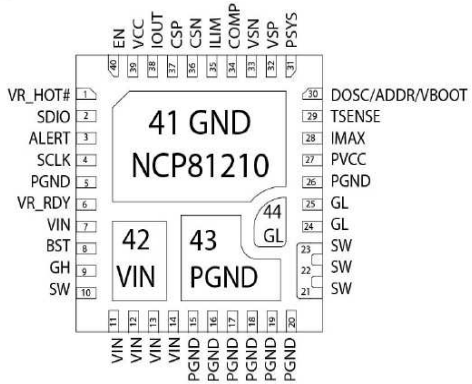
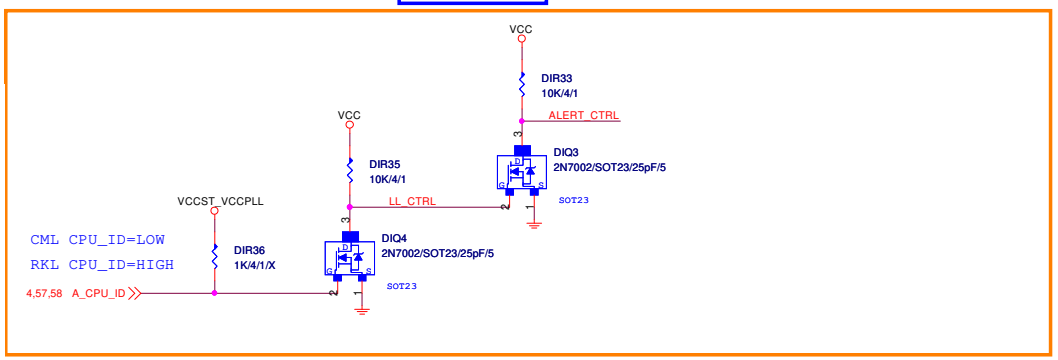
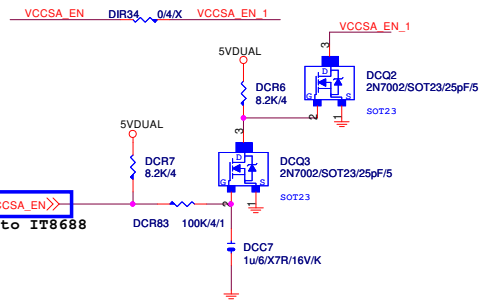
REV:0.12

IMVP8 RKL VCCSA POWER CKT









VCCSA VR

- VCCSA VR need to be IMVP8 SVID controller. Recommend VCCSA VR design to 22.1A.
  - When CPU_ID = 0 (CML-S CPU), set DC load line to 0 Ohm and disconnect VCCSA SVID Alert# from common (VCCCORE/VCCGT) SVID Alert# bus. A bypass feature (0 ohm) resistor should be provided around the disconnect circuit.
  - When CPU_ID = 1 (RKL-S CPU), set DC load line to 10.3mOhm and connect VCCSA SVID Alert# to common SVID Alert# bus

GIGABYTE™

Title	NCP81210 VCCSA	
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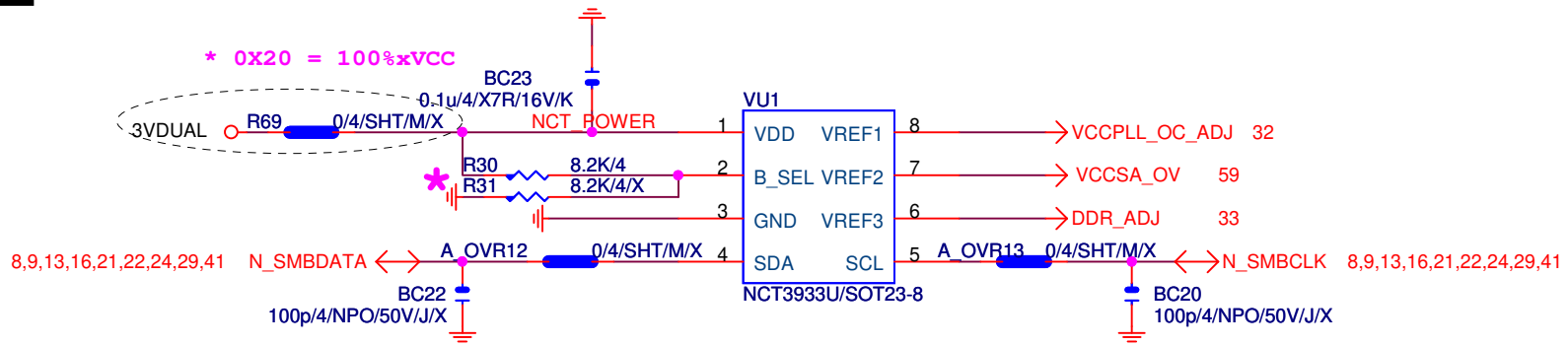
OVER VOLTAGE



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

NCT3933	
VREF1	VCCPLL_OC
VREF2	VCCSA
VREF3	VDDQ

Title: NCP3933		
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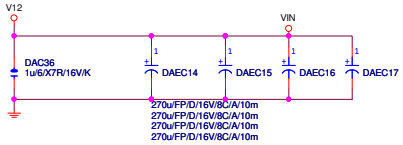
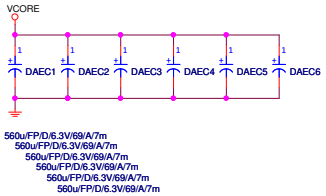
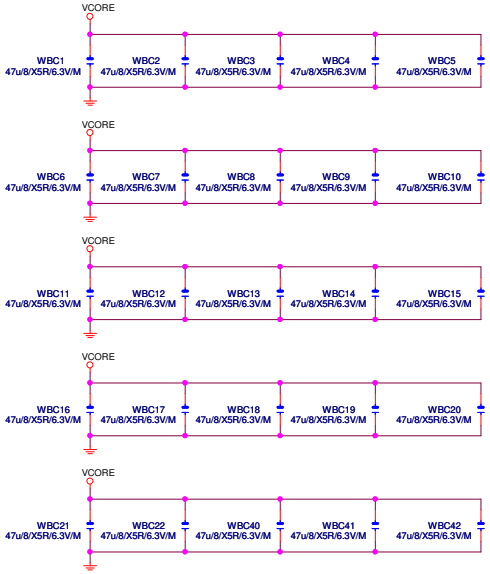
VIN CAP 270u*4PCS

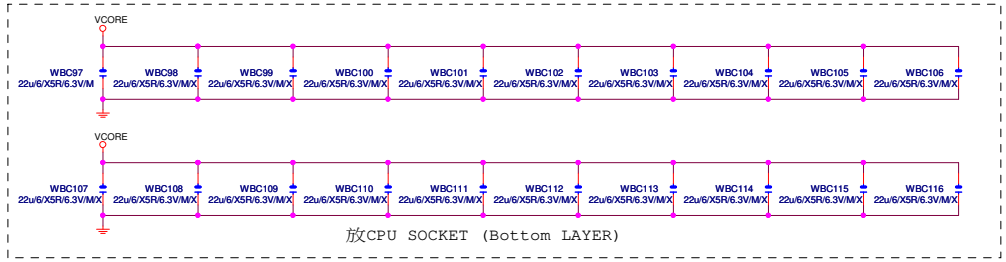


VCORE CAP 560u*6PCS 22u*20PCS

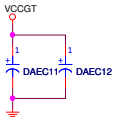


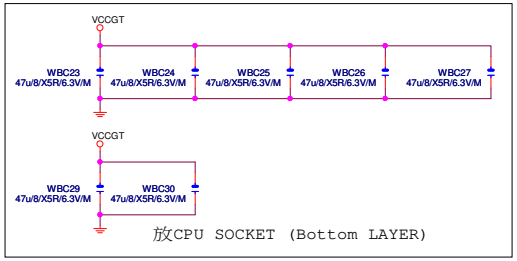


放CPU SOCKET (TOP LAYER)



VCCGT CAP 560u*2PCS 22u*4PCS





Title	CPU CAP.	
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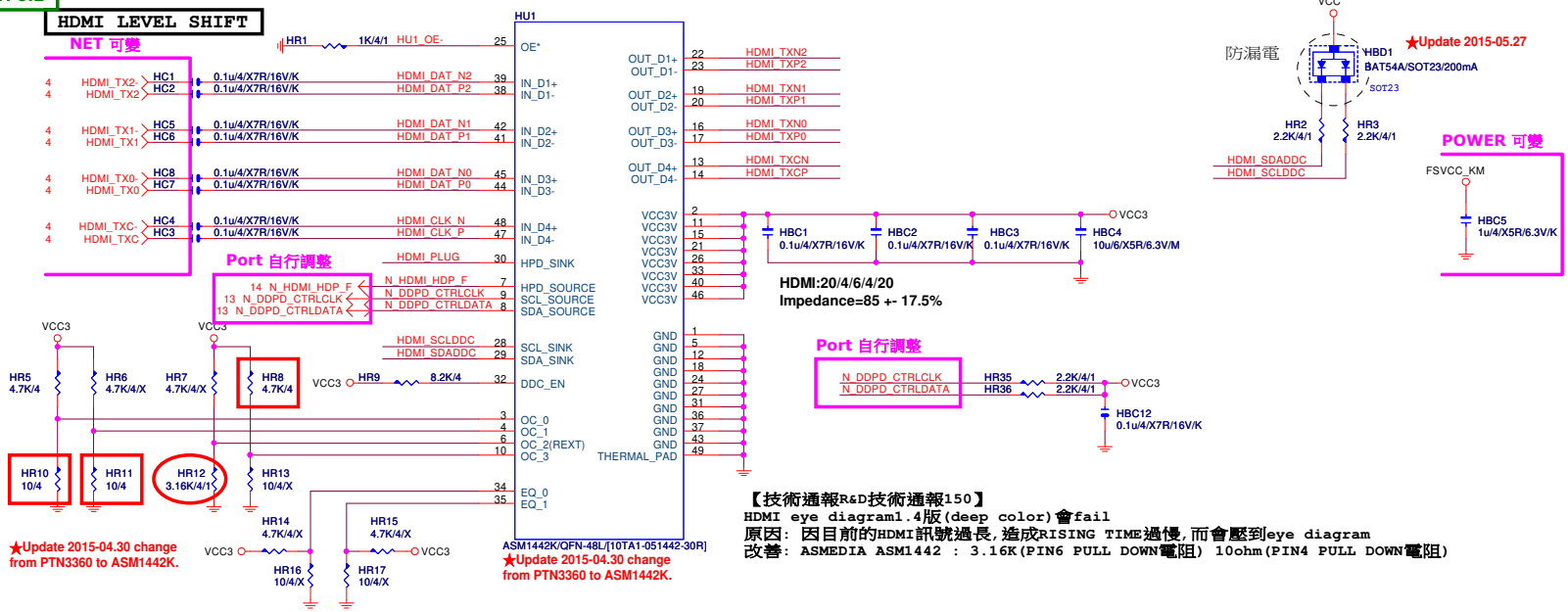
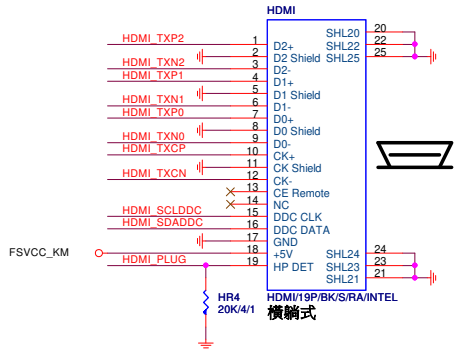


【技術通報R&D技術通報150】
HDMI eye diagram1.4版(deep color)會fail
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)



PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K

Gigabyte Technology			
Title: FP,F_USB,USB PWR,BZ			
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