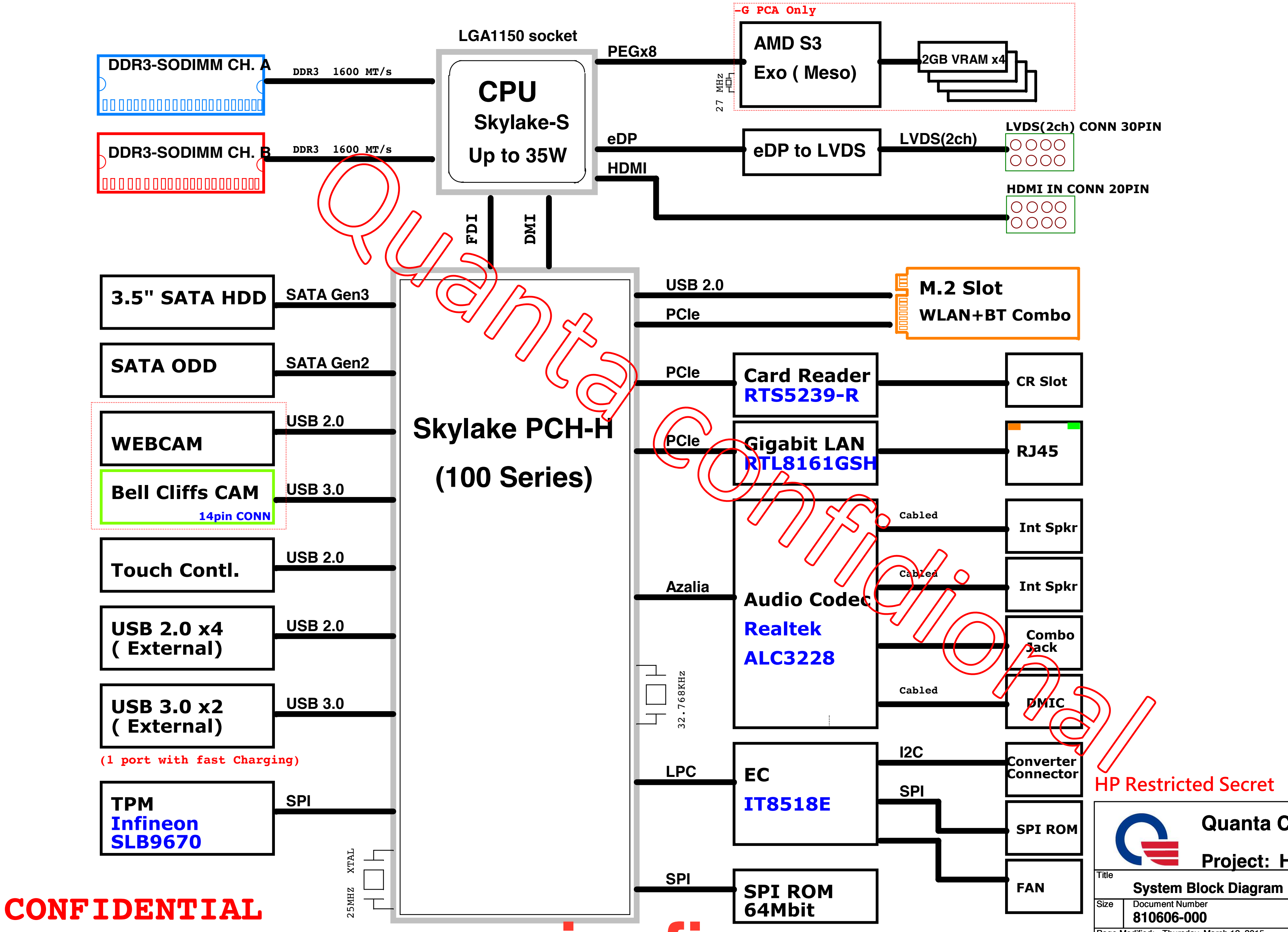
HP Crane System Block Diagram

01



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Project: HP-CRANE

Title	System Block Diagram	
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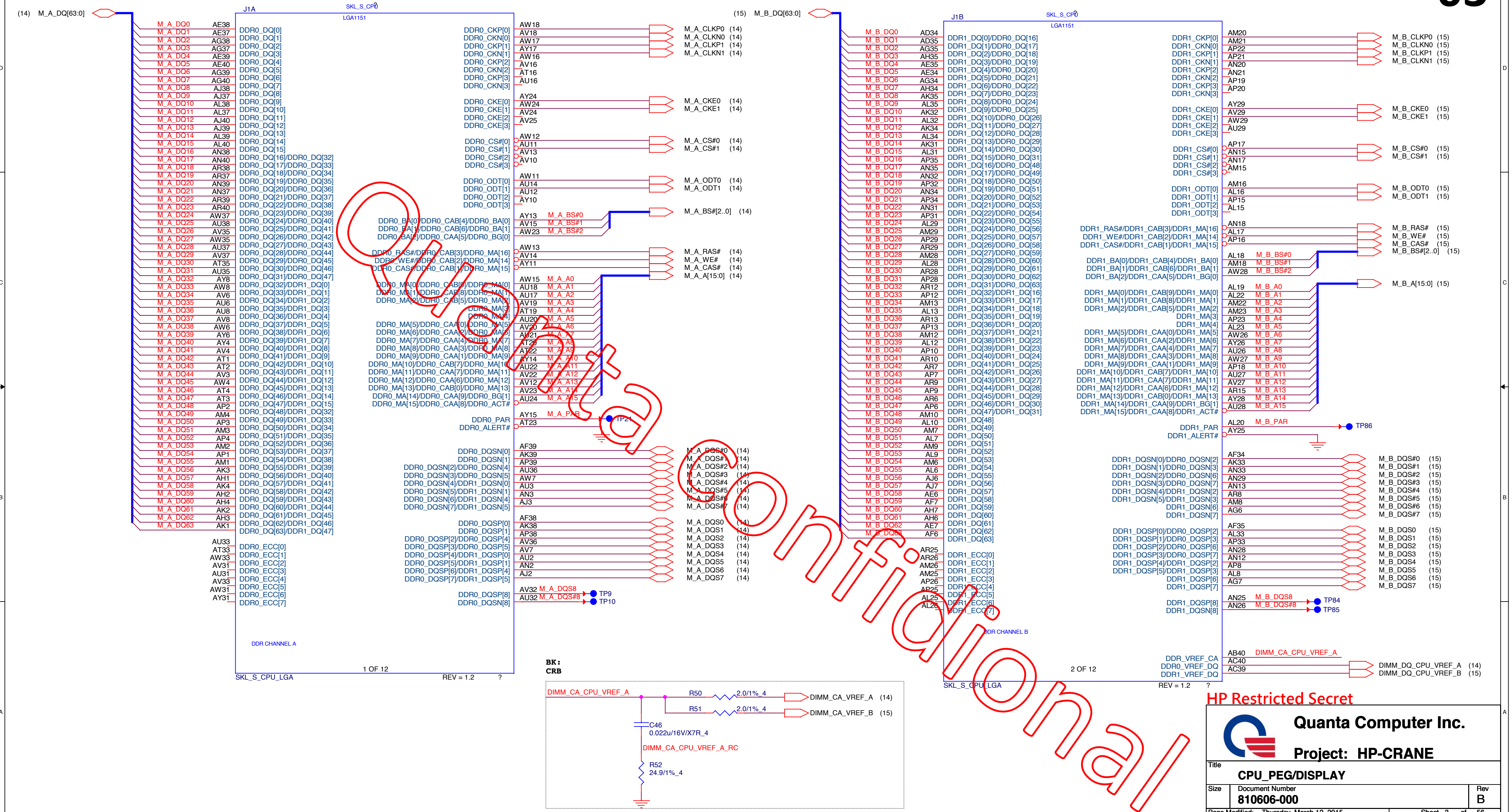
Voltage Rails

Power Rail	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal	
+RTC_VCC	3V	ON	ON	ON	ON	ON	ON		RTC Batt, PCH , EC
+VIN	19V	ON	ON	ON	ON	ON	OFF	Adaptor in	
+5V_AUX	5V	ON	ON	ON	ON	ON	OFF	AUX_ON	USB Charger
+3.3V_AUX	3.3V	ON	ON	ON	ON	ON	OFF	3V/5V PWM IC_LDO	EC, Flash
+5V_SUS	5V	ON	ON	ON	ON	OFF	OFF	EC_SUS_ON	PCH, USB, 3D WebCAM, Touch Panel
+3.3V_SUS	3.3V	ON	ON	ON	ON	OFF	OFF	EC_SUS_ON	PCH, XDP, SPI flash ROM,NGFF LAN
+1.8V_SUS	1.8V	ON	ON	ON	ON	OFF	OFF	EC_SUS_ON	PCH, XDP, NGFF LAN
+1.0V_SUS	1.0V	ON	ON	ON	ON	OFF	OFF	PG_+1.8V_SUS	PCH
+VCCST_VCCPLL	1.0V	ON	ON	OFF	OFF	OFF	OFF	S3_ON	CPU, PCH, XDP
+VDDQ	1.35V	ON	ON	OFF	OFF	OFF	OFF	S3_ON	DDR3, CPU DDR3 I/O
SMDDR_VTERM	0.75V	ON	ON	OFF	OFF	OFF	OFF	DDR_VTT_CNTL	DDR3
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	HDD, ODD,Audio AMP,Panel VCC,FAN
+3.3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	PCH, Audio, Card Reader, TPM, FHD CAM
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	3.5" HDD
+VCCIO	0.95V	ON	OFF	OFF	OFF	OFF	OFF	PG_MAIN	CPU
+VCCSA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+VCCIO	PCH, CPU
+VCCGT	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON	PCH
+3.3V_VGA	3.3V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dGPU
+1.8V_VGA	1.8V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dGPU
+0.95V_VGA	0.95V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dGPU
+VGA_CORE	0.8~1.15V	ON	OFF	OFF	OFF	OFF	OFF	PG_+1.8V_VGA	dGPU
+1.5V_VGA	1.5V	ON	OFF	OFF	OFF	OFF	OFF	GFX_PWR_GOOD	dGPU, VRAM
+VCCCORE	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON	CPU

Schematic "Value" Definition

Intel Platform Crusher-G and Crusher-U			DB/SI/PV Stage			MP		
By Value format	Description	Auto BOM Control	UMA	Discrete Meso GPU	Discrete Exo GPU	UMA	Discrete Meso GPU	Discrete Exo GPU
XX	Install	V	V	V	V	V	V	V
*XX	Non-Install	V						
PROTO@XX	Install in Pre-production only	V	V	V	V			
MP@XX	Install in MP only	V				V	V	V
DIS@xx	Install Discrete (DGPU) only	V		V	V		V	V
UMA@xx	Install UMA	V	V			V		
M_DIS@xx	Install Discrete Meso GPU only	V		V			V	
E_DIS@xx	Install Discrete Exo GPU only	V			V			V

***Board ID and VRAM ID by manual control



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Project: HP-CRANE

Title	CPU_PEG/DISPLAY	
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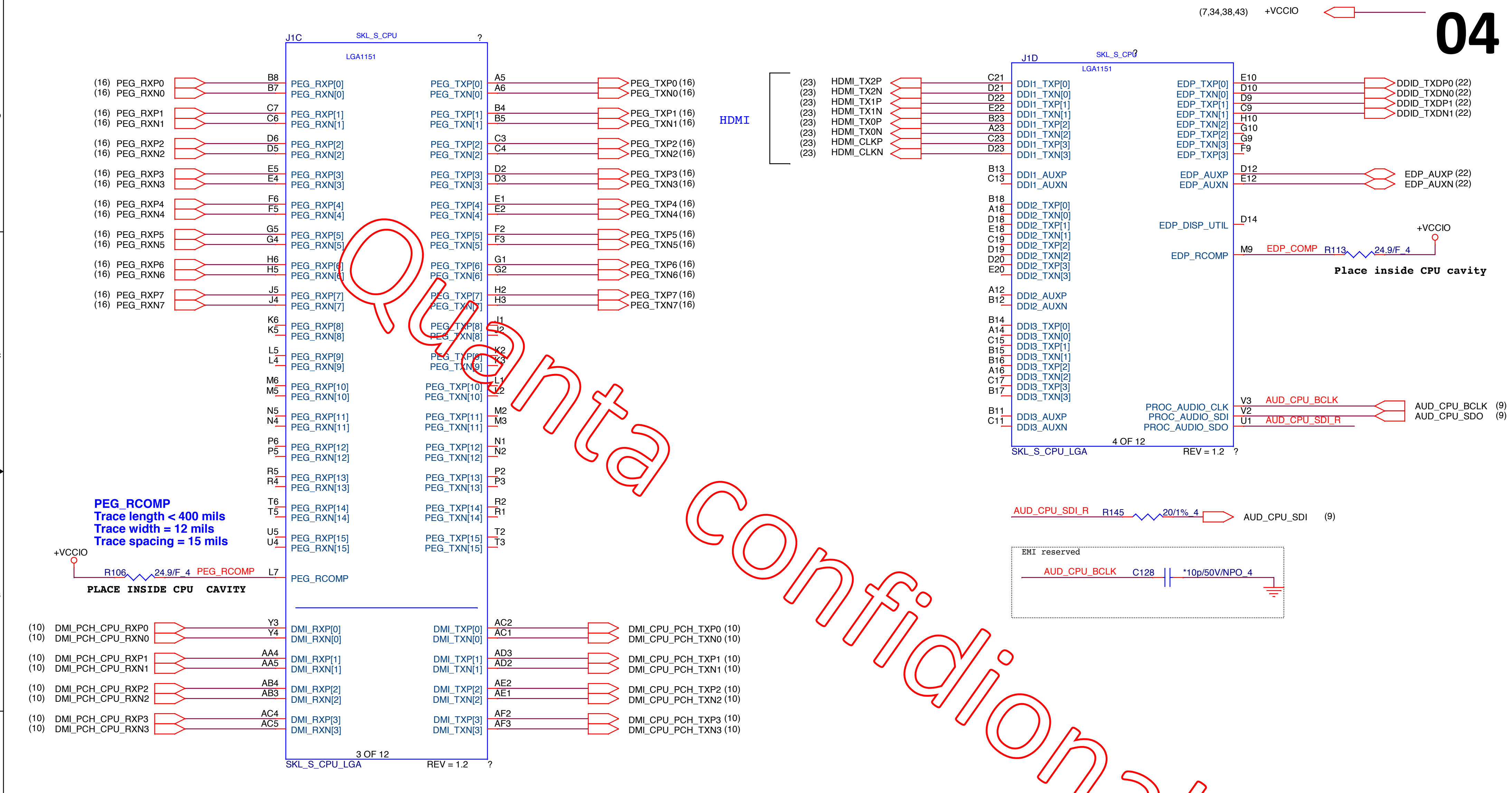

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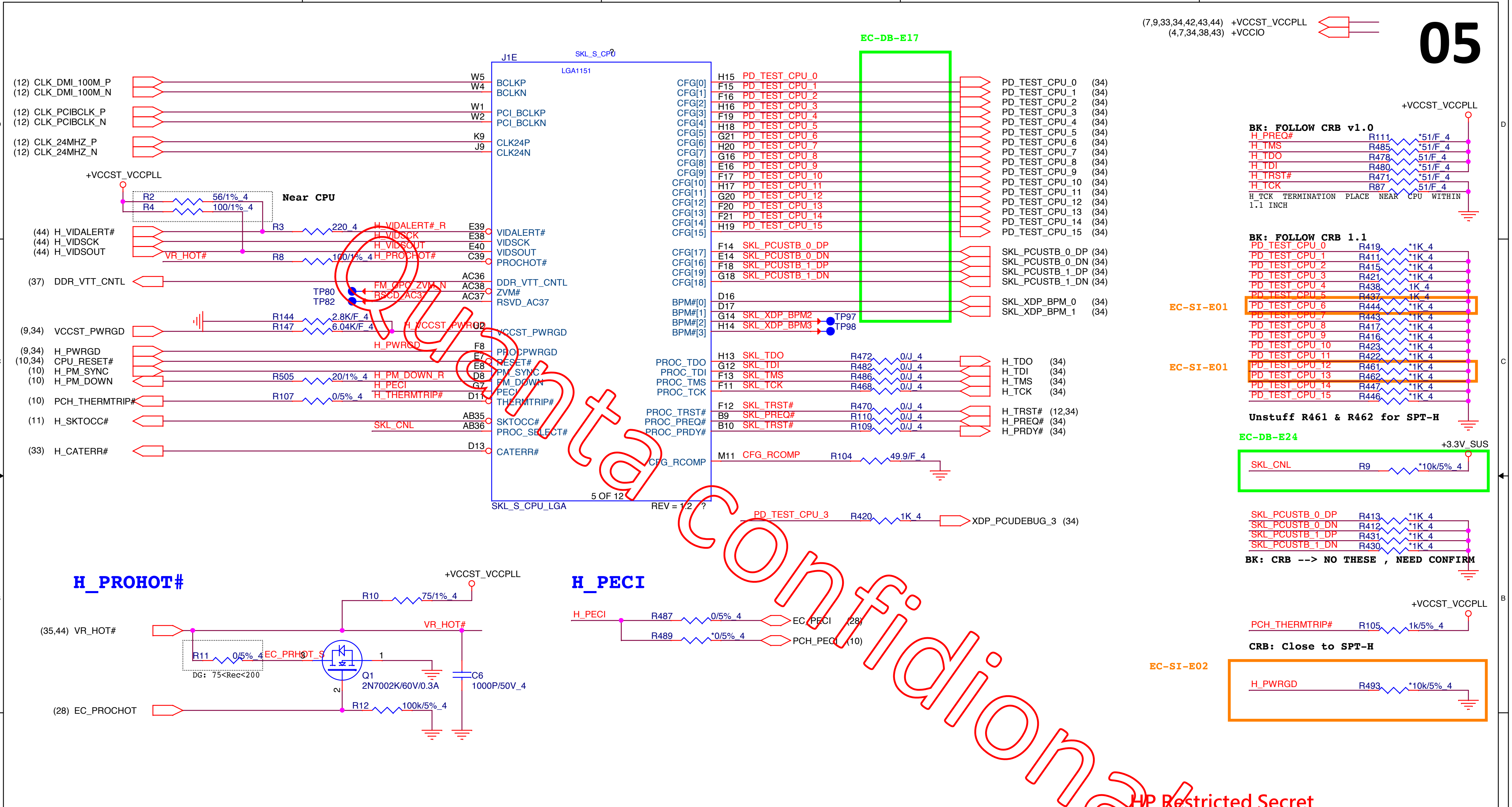
Project: HP-CRANE

Title: CPU_PEG/DISPLAY

Size	Document Number	Rev
	810606-000	B



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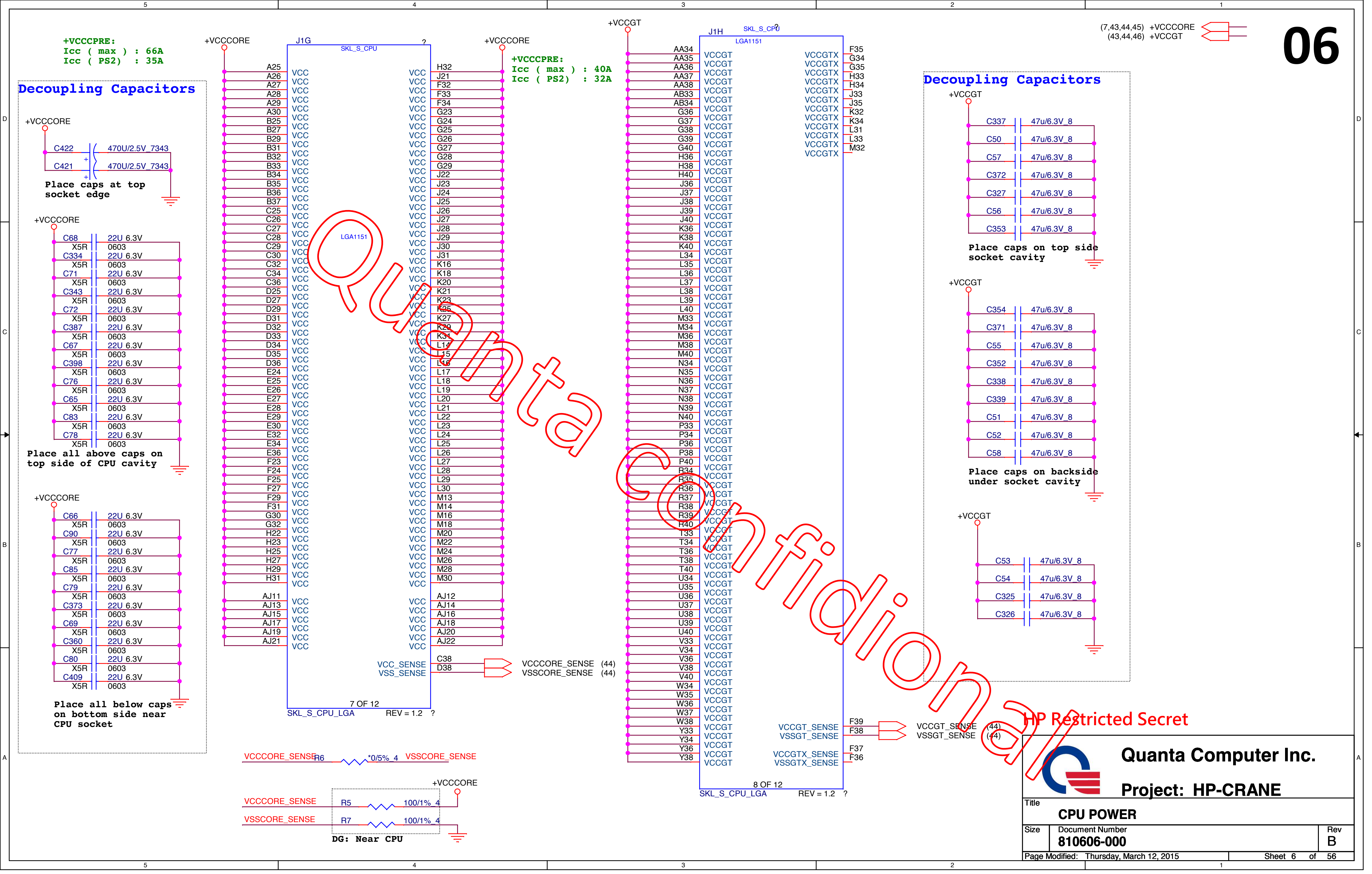
Project: HP-CRANE

Title: CPU MISC

Size | Document Number: 810606-000 | Rev: B


06
+VCCCPRE:
Icc (max) : 66A
Icc (PS2) : 35A
+VCCCPRE:
Icc (max) : 40A
Icc (PS2) : 32A
Decoupling Capacitors
+VCCCORE
C422 470U/2.5V_7343
C421 470U/2.5V_7343
Place caps at top socket edge
C68 C334 C71 C343 C72 C387 C67 C398 C76 C65 C83 C78 22U 6.3V X5R 0603
Place all above caps on top side of CPU cavity
C66 C90 C77 C85 C79 C373 C69 C360 C80 C409 22U 6.3V X5R 0603
Place all below caps on bottom side near CPU socket
J1G SKL_S_CPU LGA1151
VCC
VCC_SENSE
VSS_SENSE
VCCCORE_SENSE (44)
VSSCORE_SENSE (44)
7 OF 12
SKL_S_CPU_LGA REV = 1.2
+VCCGT
J1H SKL_S_CPU LGA1151
VCCGT
VCCGTX
VCCGT_SENSE
VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE
VCCGT_SENSE (44)
VSSGT_SENSE (44)
8 OF 12
SKL_S_CPU_LGA REV = 1.2
(7,43,44,45) +VCCCORE
(43,44,46) +VCCGT
Decoupling Capacitors
+VCCGT
C337 C50 C57 C372 C327 C56 C353 47u/6.3V_8
Place caps on top side socket cavity
C354 C371 C55 C352 C338 C339 C51 C52 C58 47u/6.3V_8
Place caps on backside under socket cavity
C53 C54 C325 C326 47u/6.3V_8
VCCCORE_SENSE R6 *0/5%_4 VSSCORE_SENSE
VCCCORE_SENSE R5 100/1%_4
VSSCORE_SENSE R7 100/1%_4
DG: Near CPU
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Project: HP-CRANE
Title
CPU POWER
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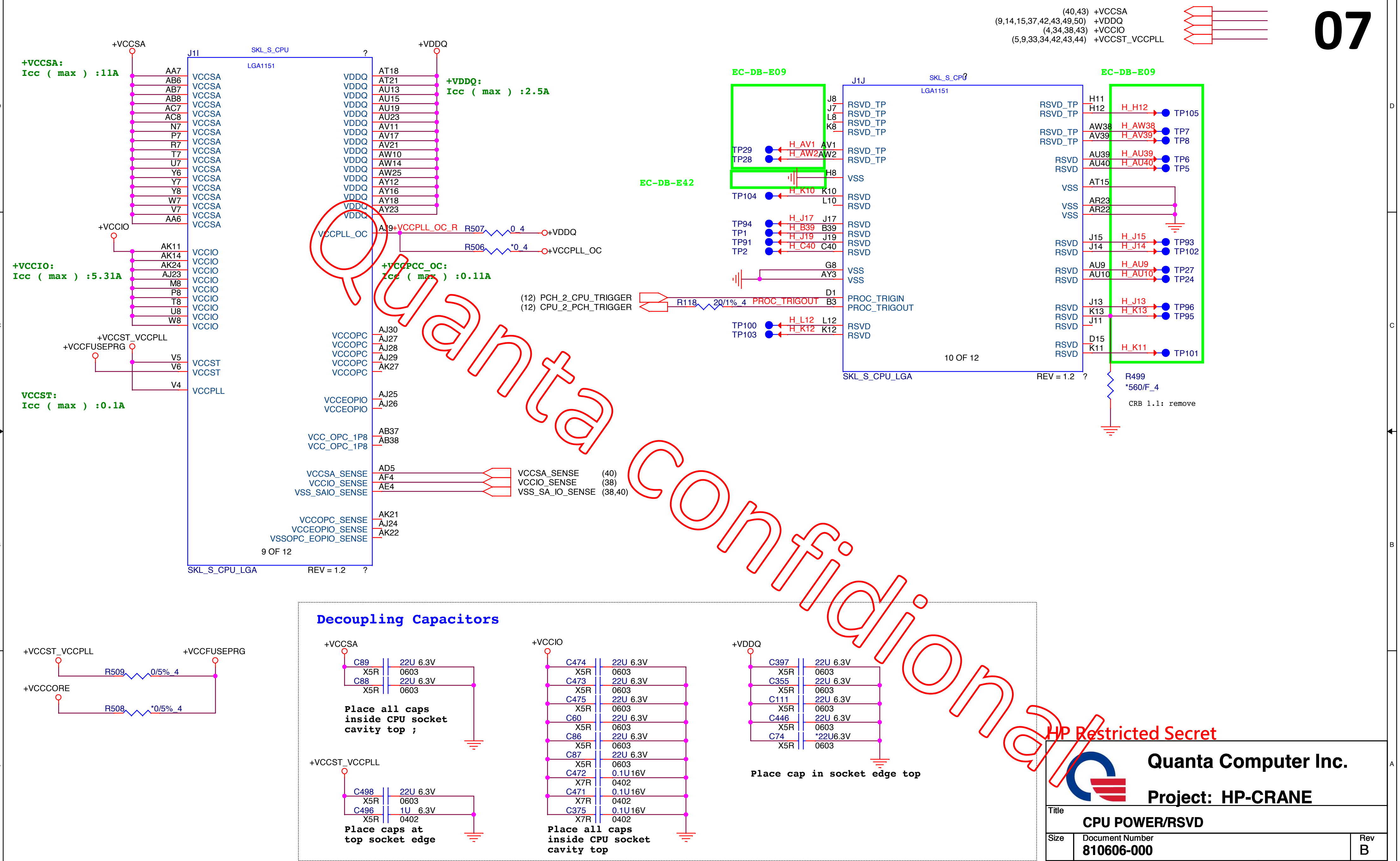

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Project: HP-CRANE

Title: CPU POWER/RSVD

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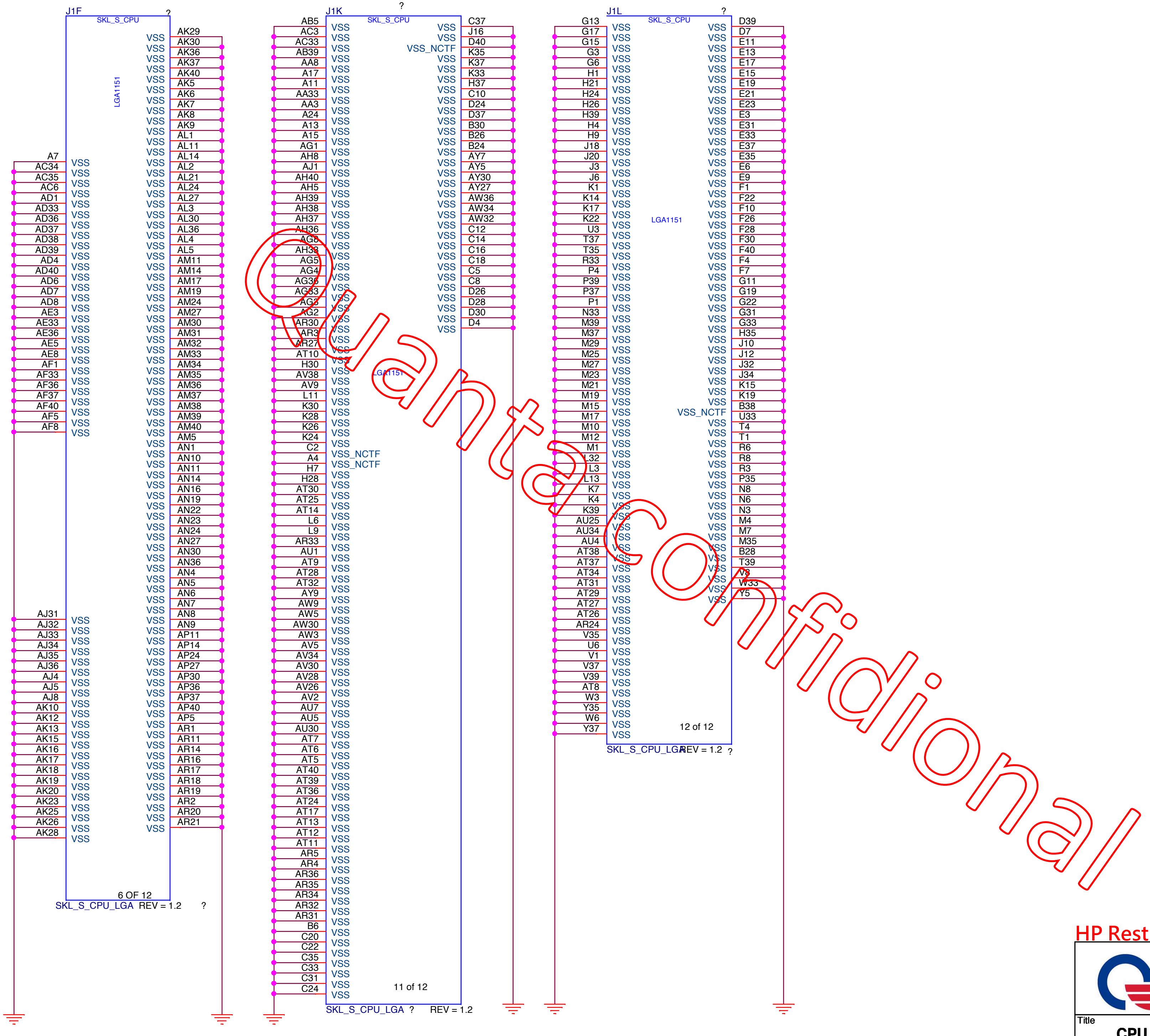

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Project: HP-CRANE

Title: CPU GND

Size	Document Number	Rev
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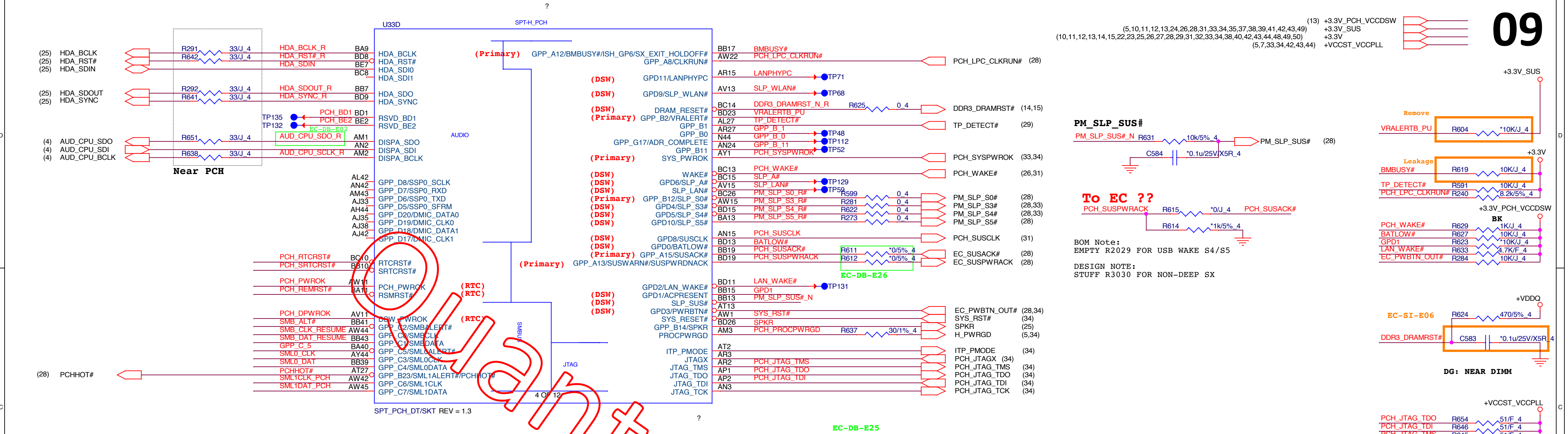
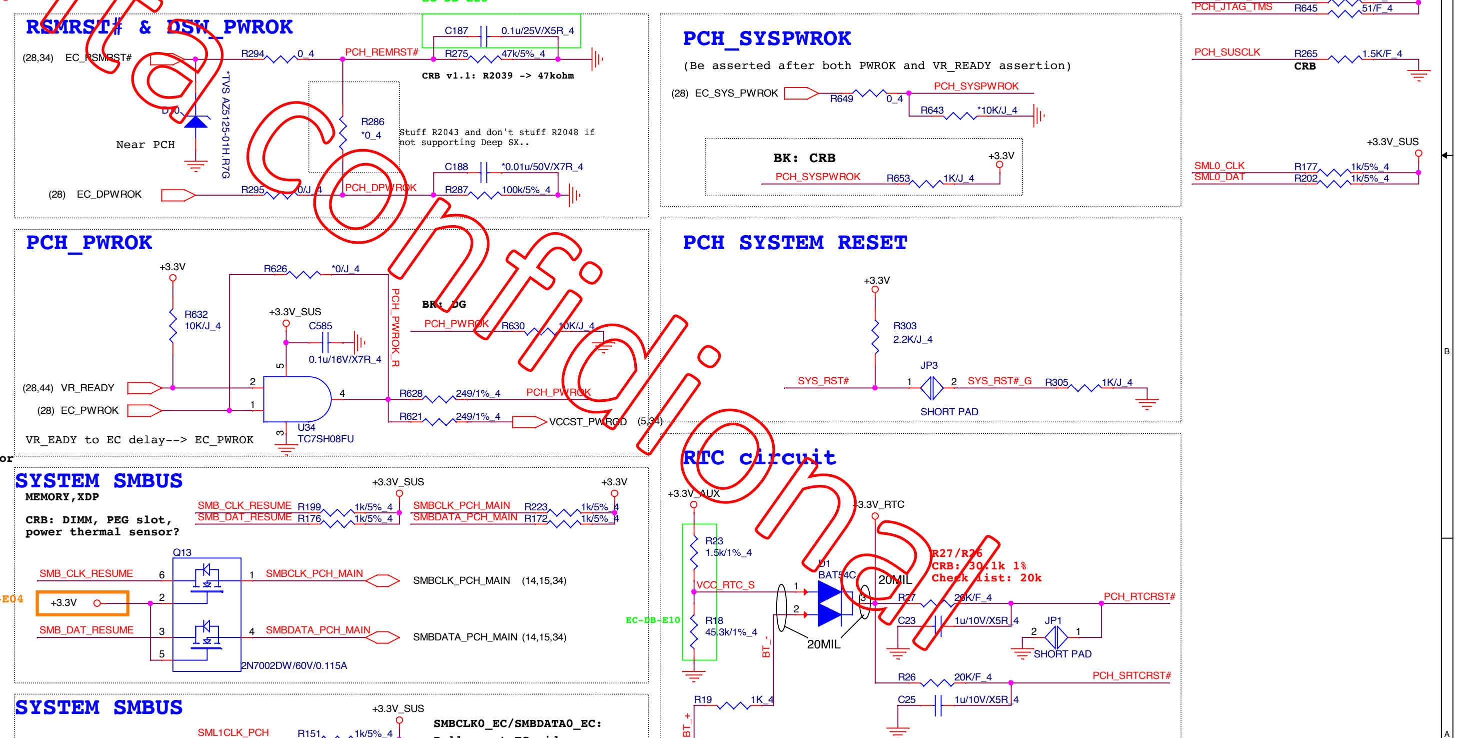
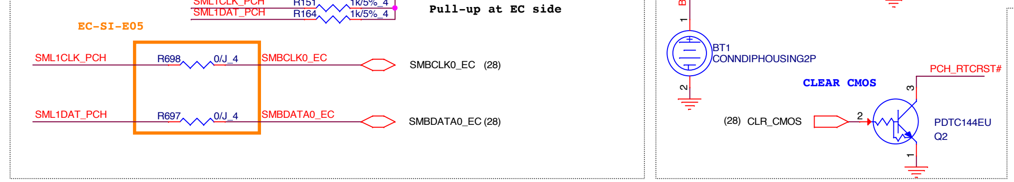


Strap Pin Table

Configuration	Note
"Top swap" mode 0 = Disable, Default (Internal pull-down) 1 = Enable	SPKR R593 *4.7K/F_4 R600 *20k/5%_4 +3.3V
"No-Reboot" mode 0 = Disable, Default (Internal pull-down) 1 = Enable	(12) LPSS_GSPI0_MOSI R588 *4.7K/F_4 R590 *1k/5%_4 +3.3V CRB 1.0
Intel ME Crypto TLS cipher suite. 0 = Disable, Default (Internal pull-down) 1 = Enable	SMB_ALT# R198 4.7K/F_4 R200 *20k/5%_4 +3.3V_SUS
BOOT SELECT STRAP 0 = SPI, Default (Internal pull-down) 1 = LPC	(12) LPSS_GSPI1_MOSI R230 *4.7K/F_4 R232 *20k/5%_4 +3.3V_SUS
ESPI/LPC SELECT STRAP (for EC) 0 = LPC (Default, int. pull-down) 1 = ESPI	GPP_C_5 R550 *4.7K/F_4 R549 20K/5%_4 +3.3V_SUS EC-DB-E43
BOOT HALT 0 = Enable 1 = PCH has Internal weak pull-up	(10,33,34) SPI_MOSI R585 1k/5%_4 R586 *4.7K/F_4 +3.3V_SUS_SPI
JTAG ODT 0 = Enable 1 = PCH has Internal weak pull-up	(10,33) SPI_MISO R582 *20k/5%_4 R579 *4.7K/F_4 +3.3V_SUS_SPI
CONSENT STRAP 0 = Consent strap is enabled 1 = PCH has Internal weak pull-up	(10,34) SPI_IO2 R592 *20k/5%_4 R589 *1.2k/5%_4 +3.3V_SUS_SPI EC-SI-E03
PERSONALITY STRAP 0 = Enable 1 = PCH has Internal weak pull-up	(10) SPI_IO3 R570 *20k/5%_4 R563 *4.7K/F_4 +3.3V_SUS_SPI pull down is needed for pre-ES1/ES1 samples.
0 = PCH has Internal weak pull-down 1 = EXI boot stall bypass is enabled	150K PU NEEDED TO DISABLE EXI BOOT STALL BYPASS PCHHOT# R235 150k/1%_4 R236 *20k/5%_4 +3.3V_SUS EC-DB-E44
SECRUITY MEASURES. 0 = Enable, Default (Internal weak pull-down) 1 = Disable. Flash Descriptor Security overrided, pull up for debug only.	CN20 HDA_SDOUT_R 1 2 HDA_SDO R283 1K/J_4 +DVDDIO_AUDIO FDO_SLHY-02B1-B-045-F-R
ESPI FLASH SHARING MODE 0 = Master (Internal weak pull-down) 1 = Slave	(10) GPP_H_12 R556 *4.7K/F_4 R555 *20k/5%_4 +3.3V_SUS
DFX TEST MODE XTAL input is single ended if sampled low else differential	(10,34) VISACH2_D3 R544 *4.7K/F_4 R543 *20k/5%_4 +3.3V_SUS
TEST SETUP MENU 0 = Test setup menu enabled 1 = Disabled (Default)	(11) TEST_SETUP_MENU R524 10K/J_4 R525 *0/5%_4 +3.3V EC-DB-E45
SV ADVANCE MENU TABLE 0 = SV ADVANCE MENU 1 = Normal Menu (Default)	(10) SV_ADVANCE_GP48 R523 20K/5%_4 R526 *0/5%_4 +3.3V EC-DB-E46





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Project: HP-CRANE

Title: PCH_HDA/SMBUS/MISC

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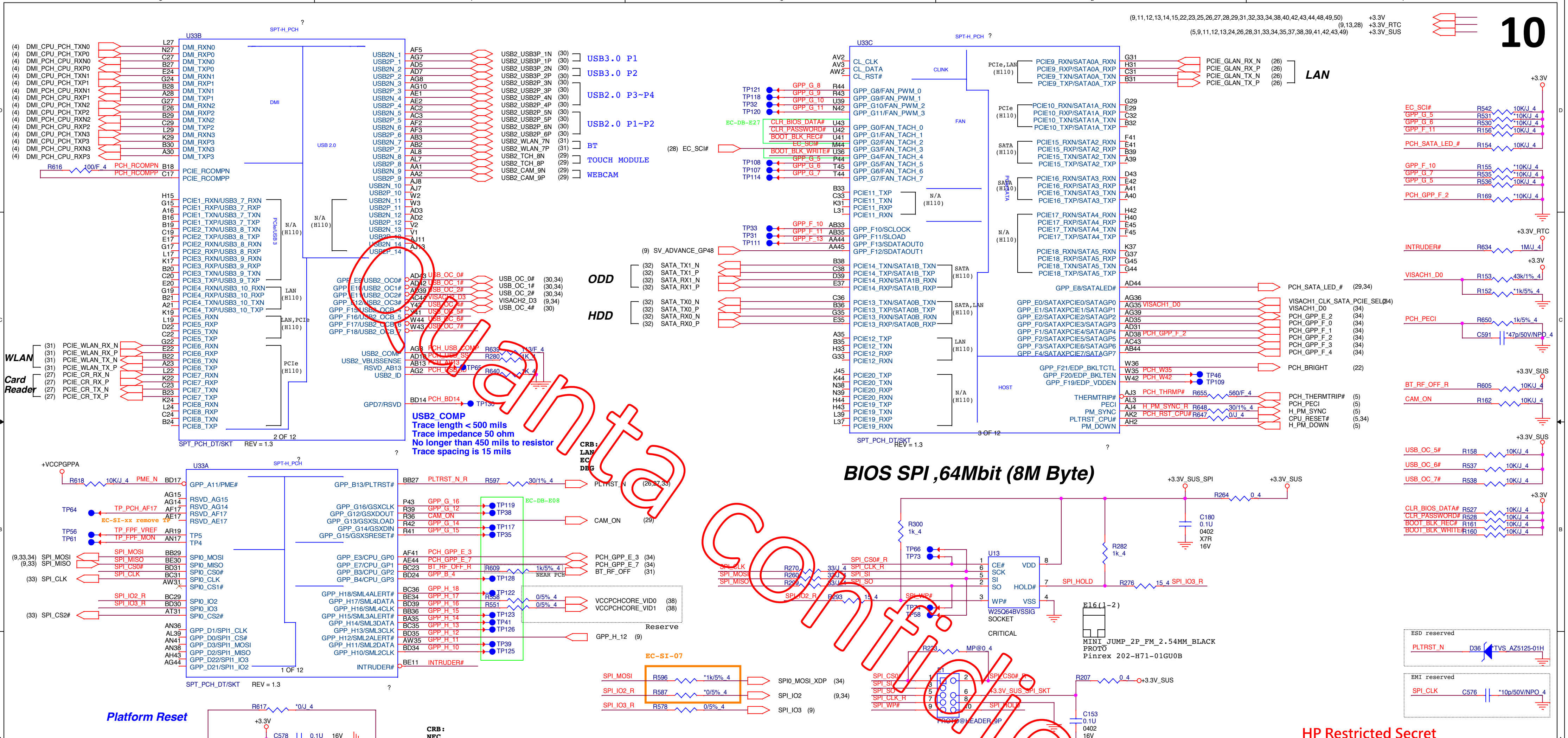

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Title	PCH_DMI/PCIE/USB/SATA/GPIO
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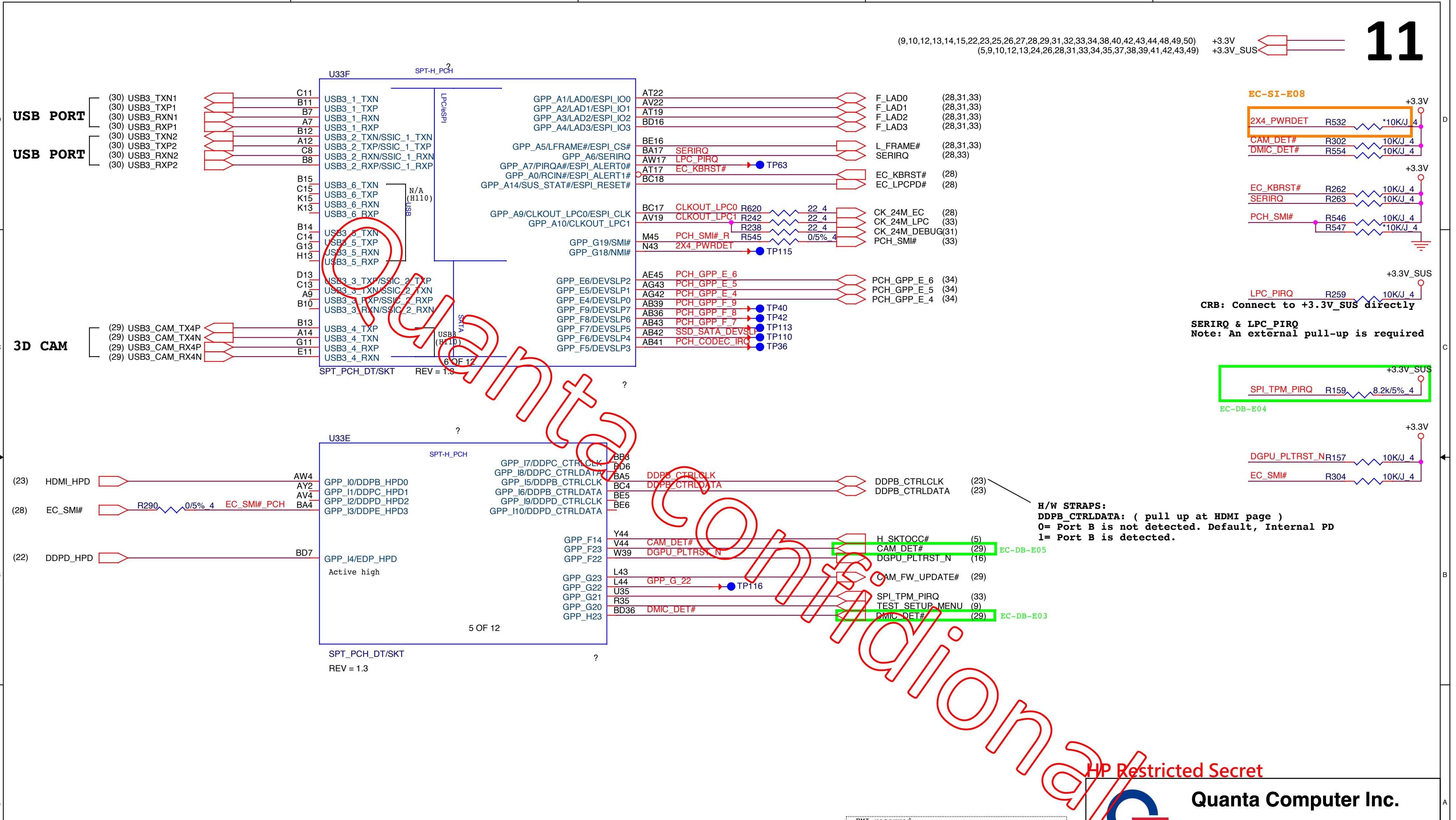

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Project: HP-CRANE

Title	PCH_USB3/LPC	
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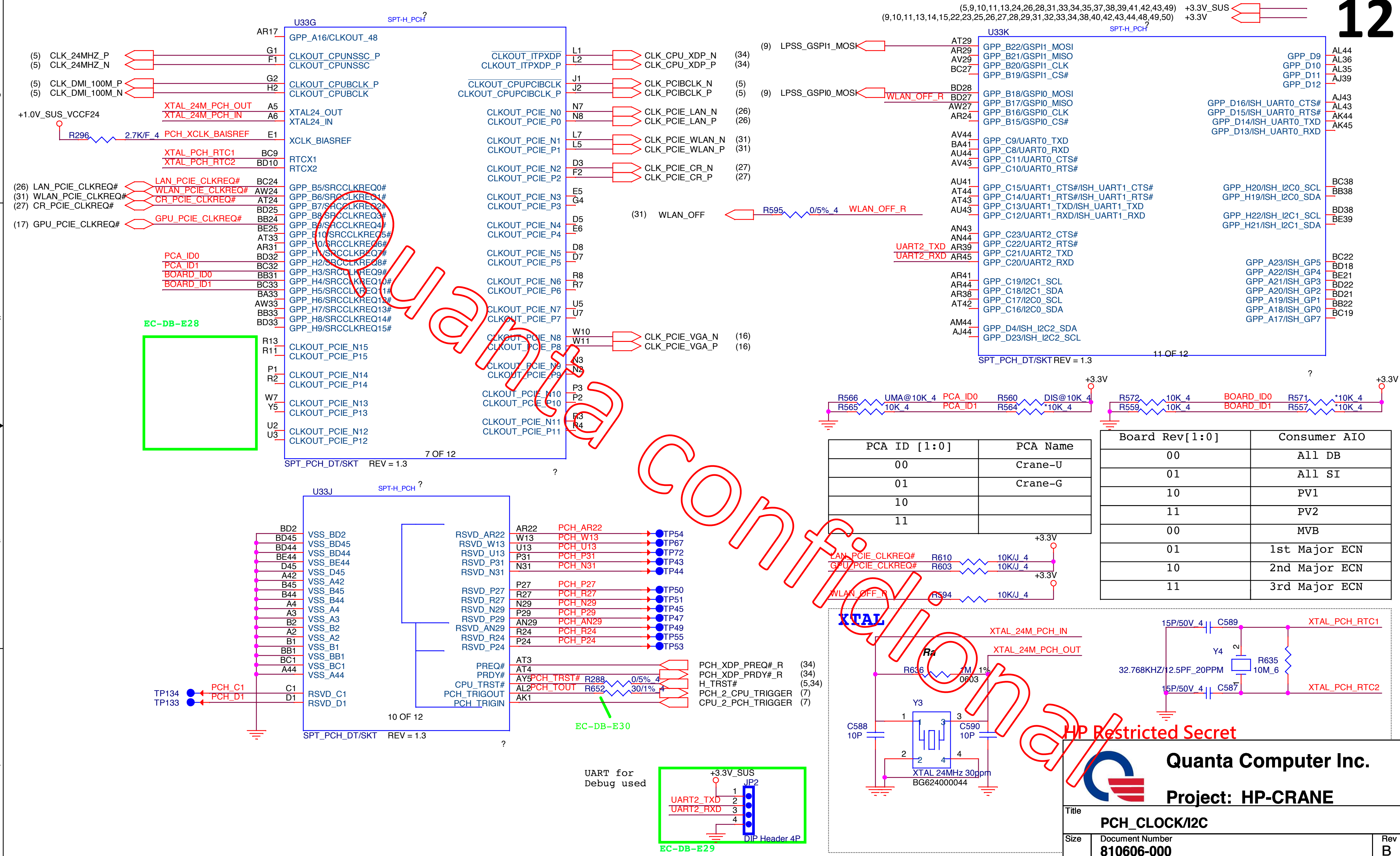

PCA ID [1:0]	PCA Name
00	Crane-U
01	Crane-G
10	
11	

Board Rev[1:0]	Consumer AIO
00	All DB
01	All SI
10	PV1
11	PV2
00	MVB
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN

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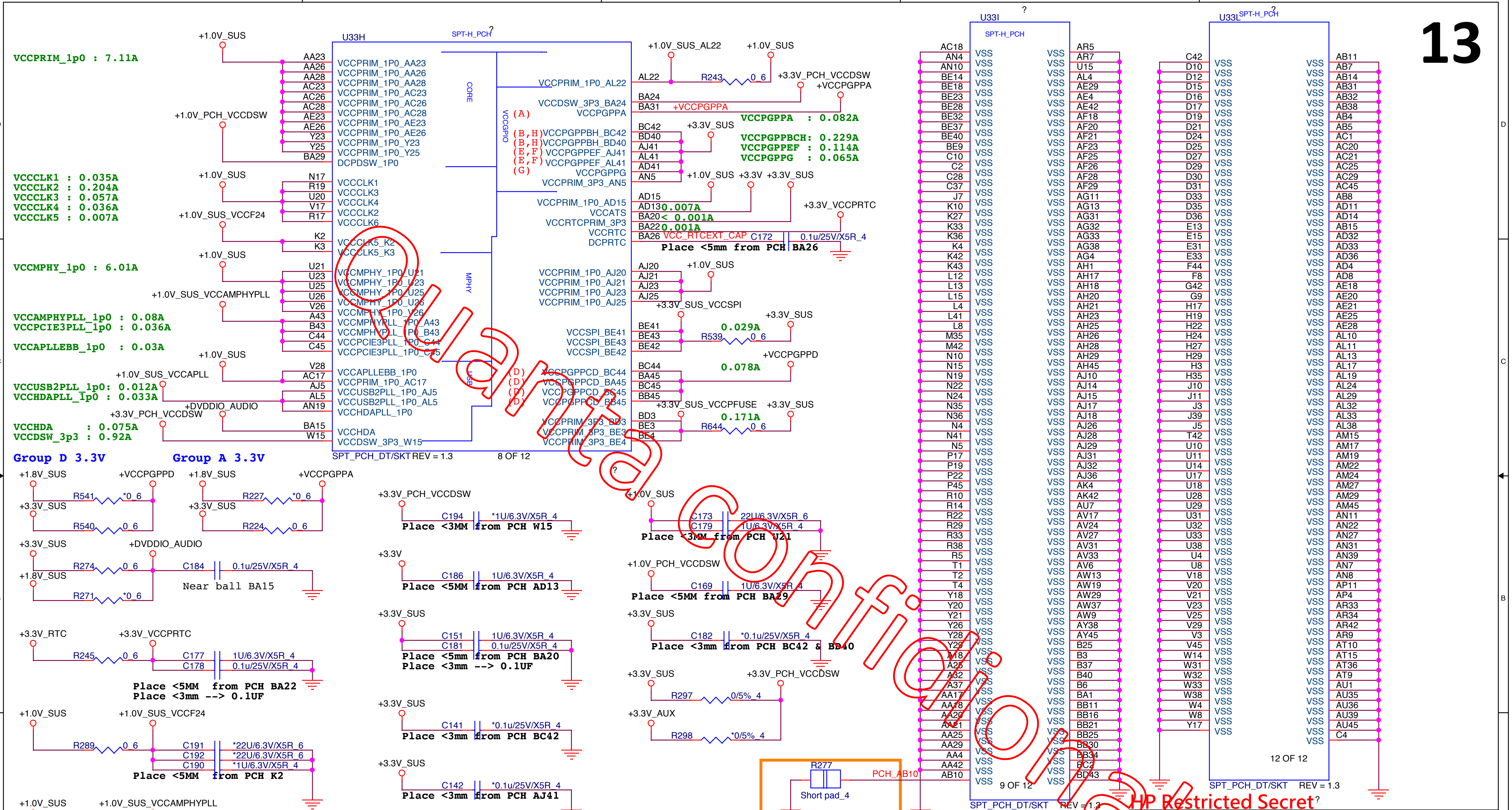
Project: HP-CRANE

Title: PCH_CLOCK/I2C

Size | Document Number: 810606-000 | Rev: B



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Project: HP-CRANE

Title: PCH_POWER/GND

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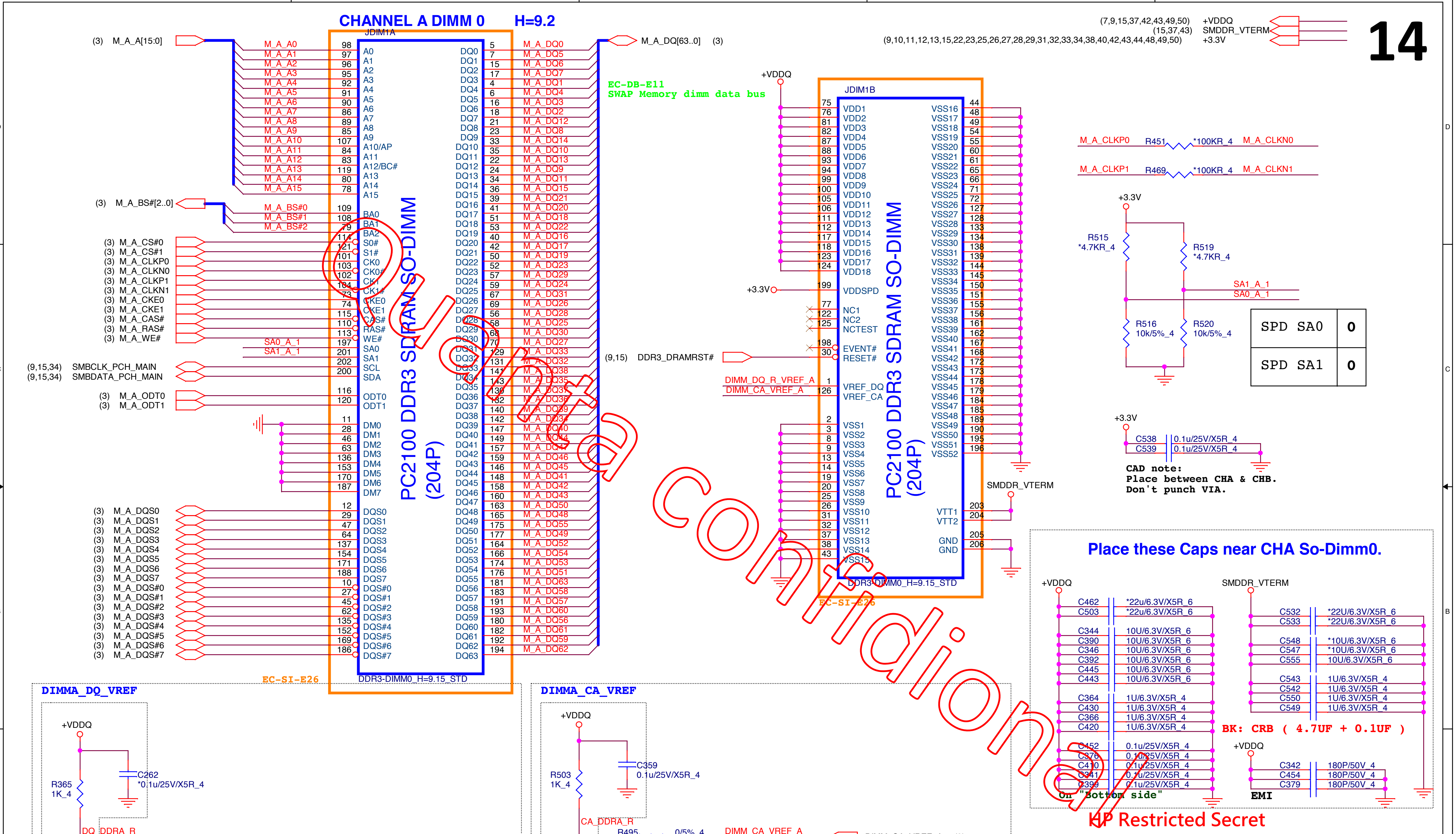

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Project: HP-CRANE

Title	DDR3 CHA DIMM 0	
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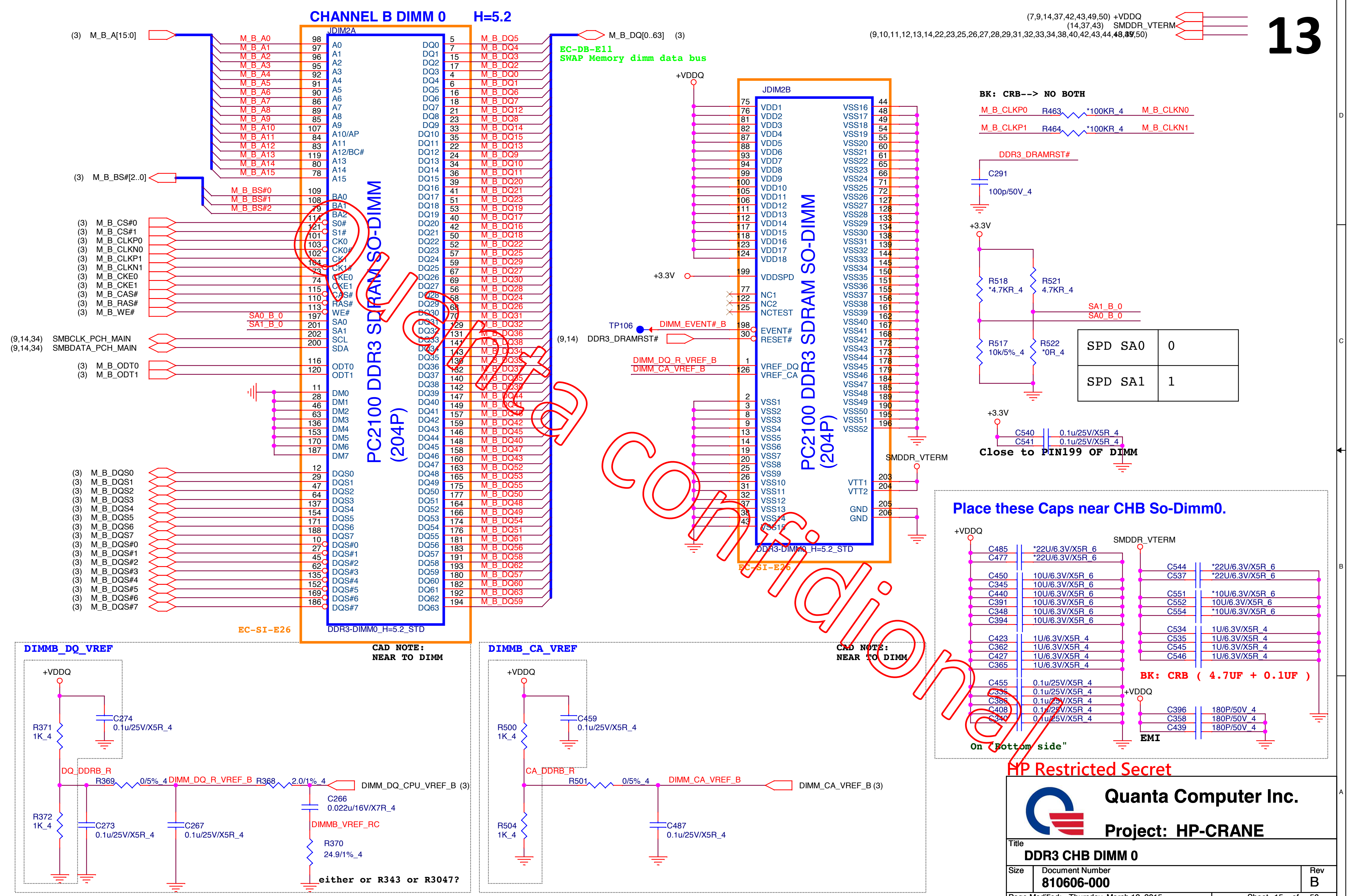

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Project: HP-CRANE

Title: DDR3 CHB DIMM 0

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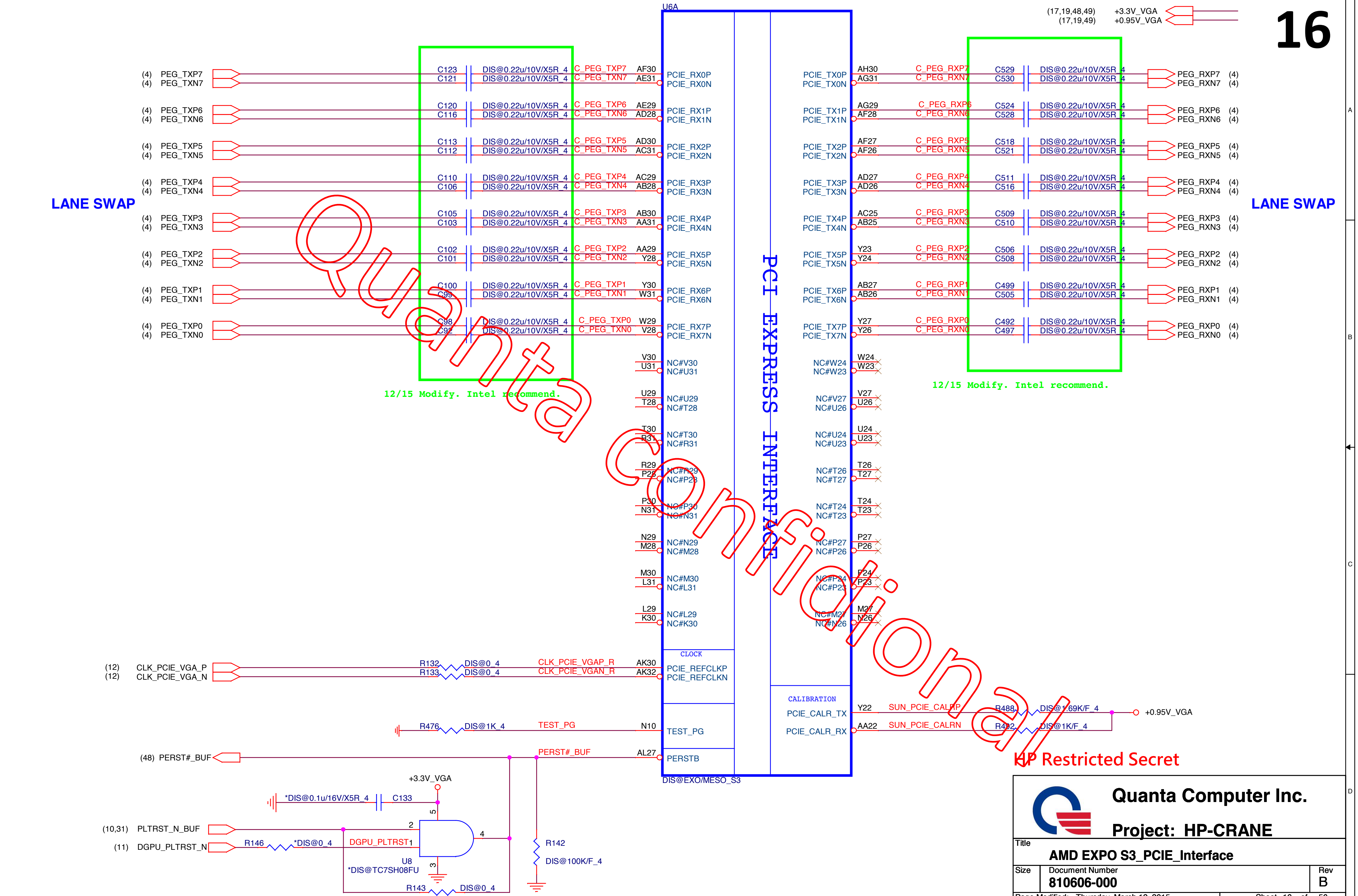

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Project: HP-CRANE

Title	AMD EXPO S3_PCIE_Interface	
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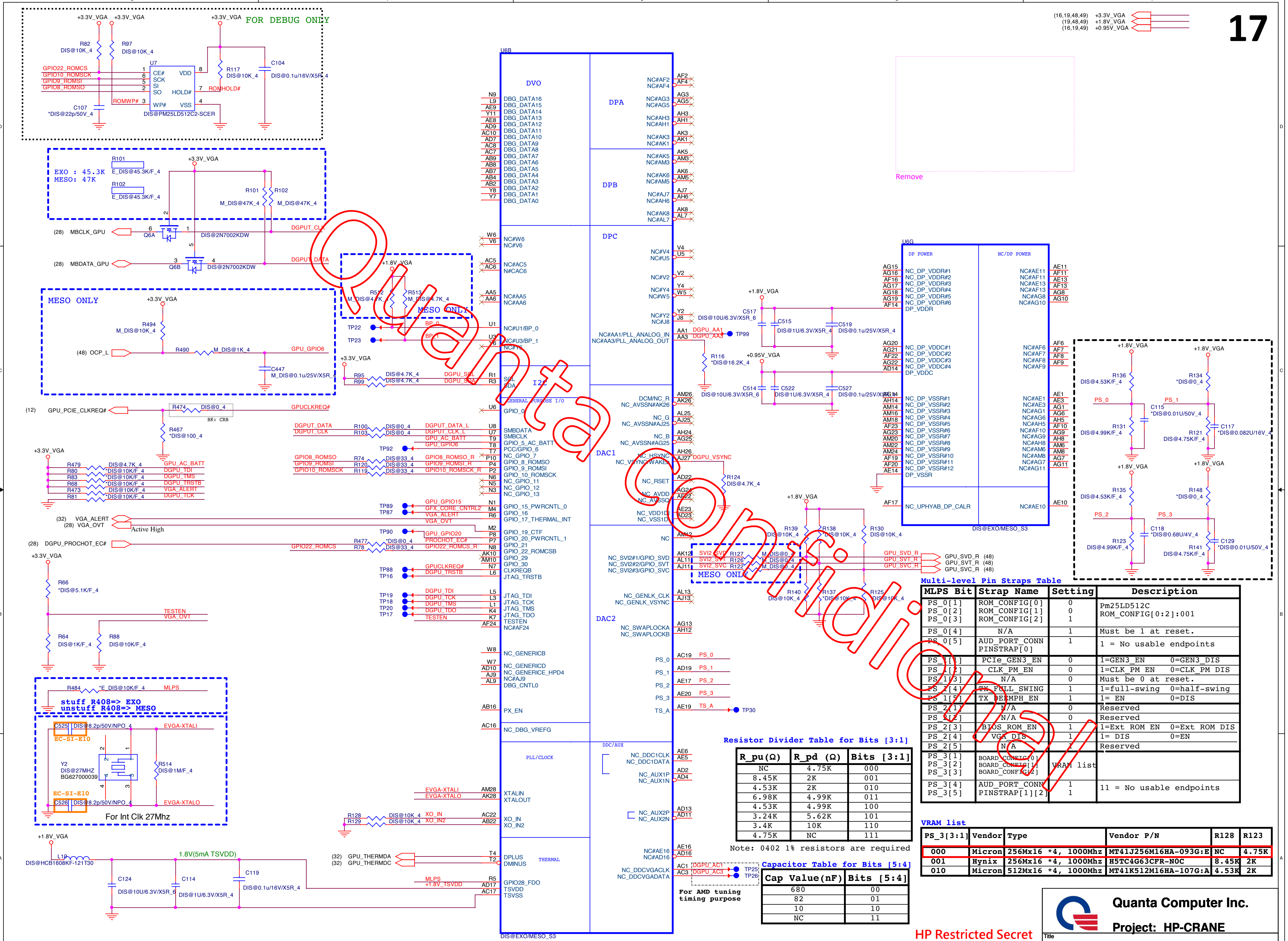


Multi-level Pin Straps Table

MLPS Bit	Strap Name	Setting	Description
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	0 0 1	Pm25LD512C ROM_CONFIG[0:2]:001
PS_0[4]	N/A	1	Must be 1 at reset.
PS_0[5]	AUD_PORT_CONN PINSTRAP[0]	1	1 = No usable endpoints
PS_1[1]	PCIe_GEN3_EN	0	1=GEN3_EN 0=GEN3_DIS
PS_1[2]	CLK_PM_EN	0	1=CLK_PM EN 0=CLK_PM DIS
PS_1[3]	N/A	0	Must be 0 at reset.
PS_1[4]	TX_FULL_SWING	1	1=full-swing 0=half-swing
PS_1[5]	TX_DEEMPH_EN	1	1= EN 0=DIS
PS_2[1]	N/A	0	Reserved
PS_2[2]	N/A	0	Reserved
PS_2[3]	BIOS_ROM_EN	1	1=Ext ROM EN 0=Ext ROM DIS
PS_2[4]	VGA_DIS	1	1= DIS 0=EN
PS_2[5]	N/A	1	Reserved
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	VRAM list	
PS_3[4] PS_3[5]	AUD_PORT_CONN PINSTRAP[1][2]	1 1	11 = No usable endpoints

Resistor Divider Table for Bits [3:1]

R_pu(Ω)	R_pd (Ω)	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Note: 0402 1% resistors are required

Capacitor Table for Bits [5:4]

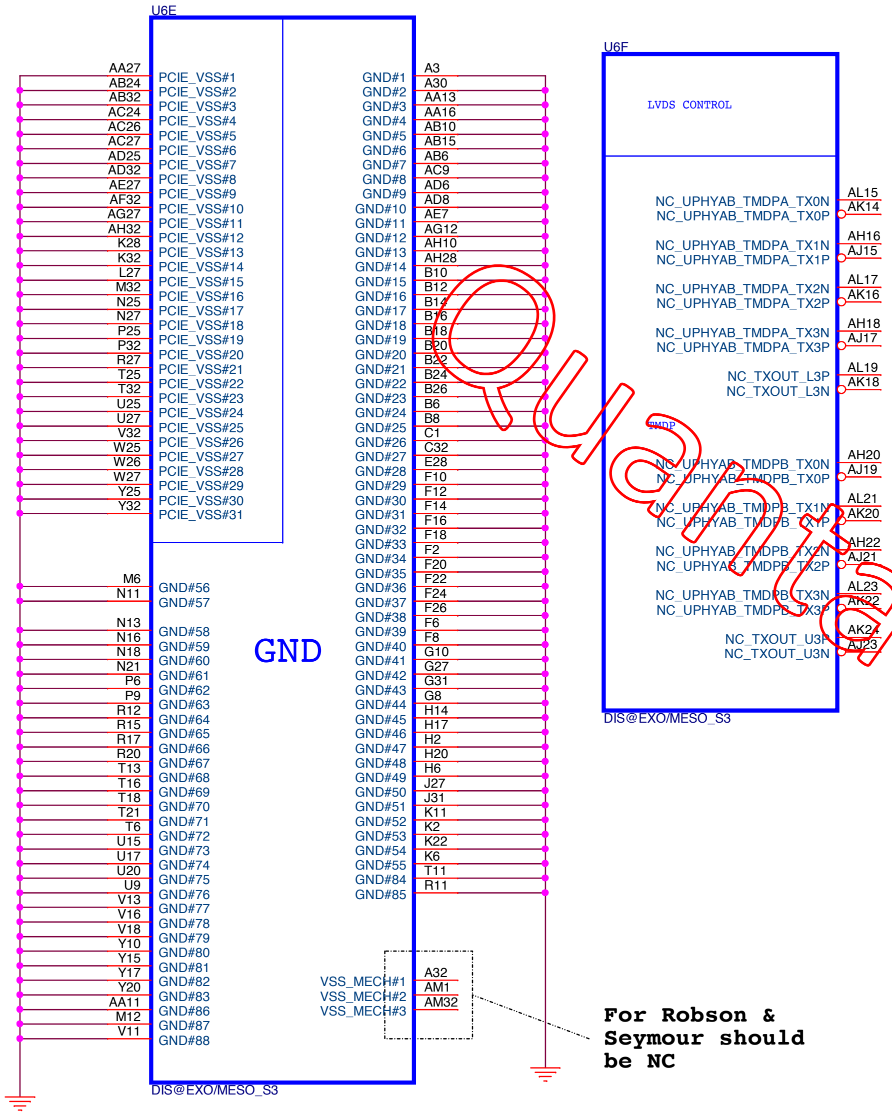
Cap Value(nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

For AMD tuning timing purpose

VRAM list

PS_3[3:1]	Vendor	Type	Vendor P/N	R128	R123
000	Micron	256Mx16 *4, 1000Mhz	MT41J256M16HA-093G:E	NC	4.75K
001	Hynix	256Mx16 *4, 1000Mhz	H5TC4G63CFR-N0C	8.45K	2K
010	Micron	512Mx16 *4, 1000Mhz	MT41K512M16HA-107G:A	4.53K	2K

(16,17,19,48,49) +3.3V_VGA



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

VGA HOLE

Quanta Computer Inc.

Project: HP-CRANE

Title: **AMD EXO PRO S3_GND/LVDS/Strap**

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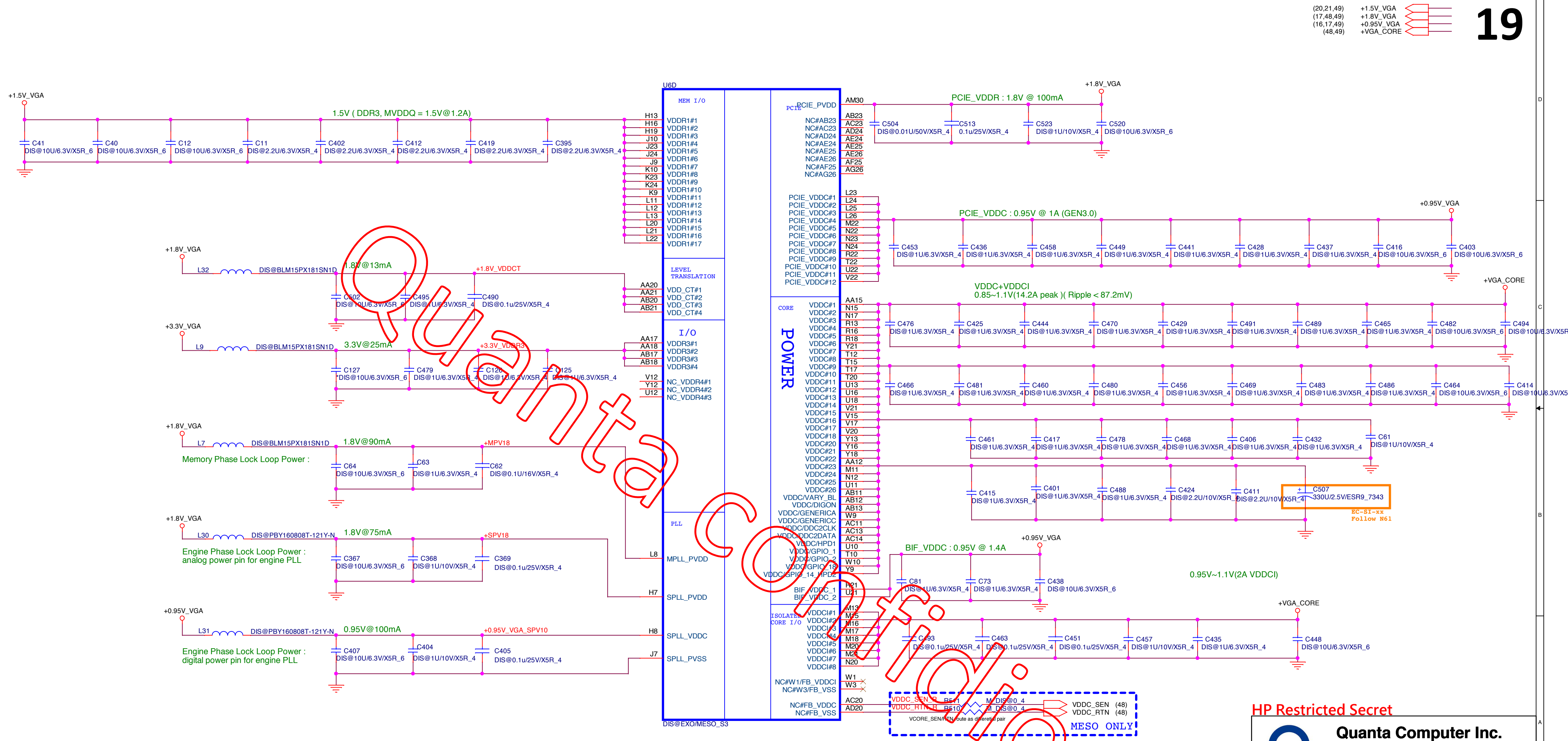

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Project: HP-CRANE

Title	AMD EXO PRO_Power	
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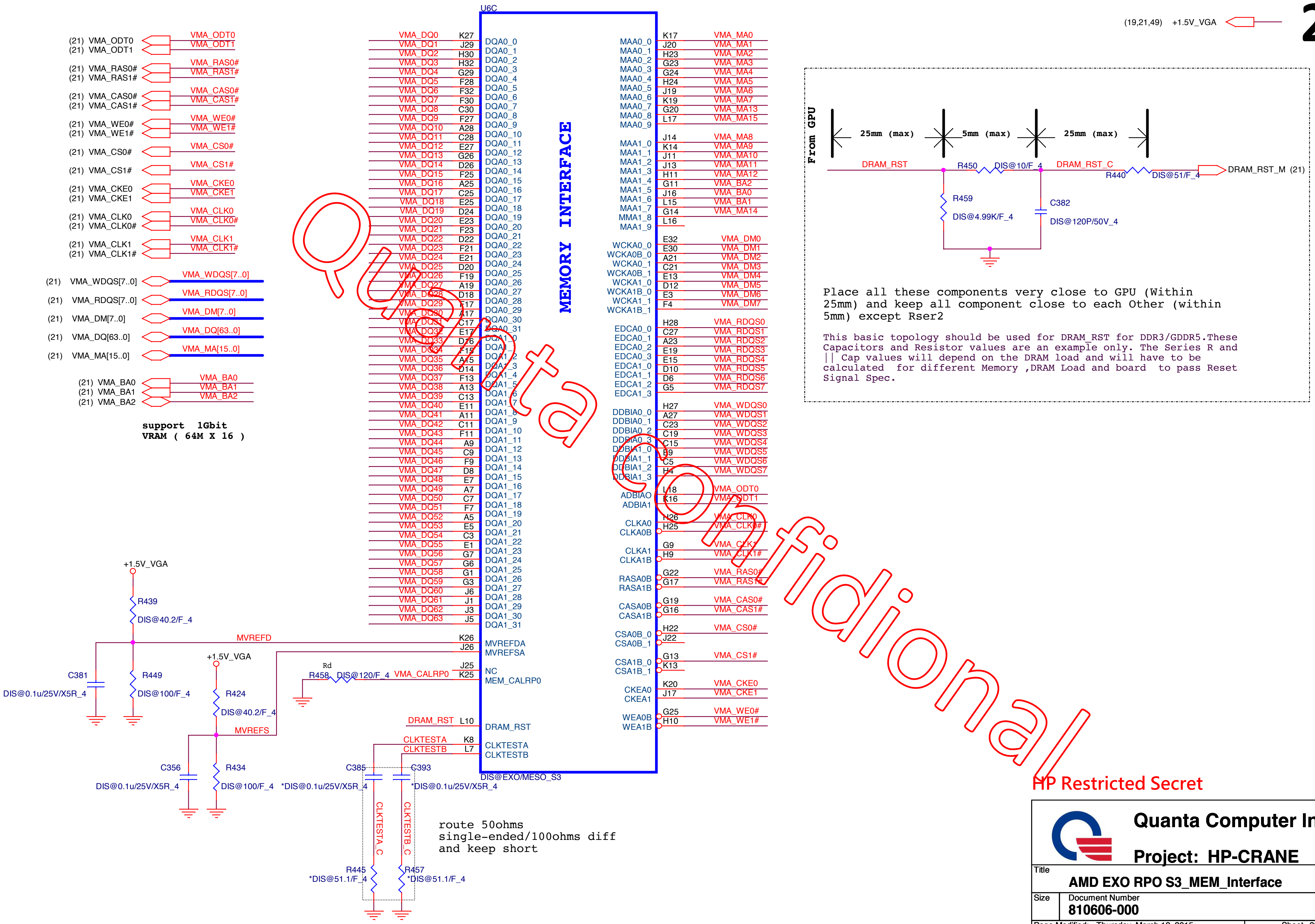

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

route 50ohms single-ended/100ohms diff and keep short

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Title	AMD EXO RPO S3_MEM_Interface
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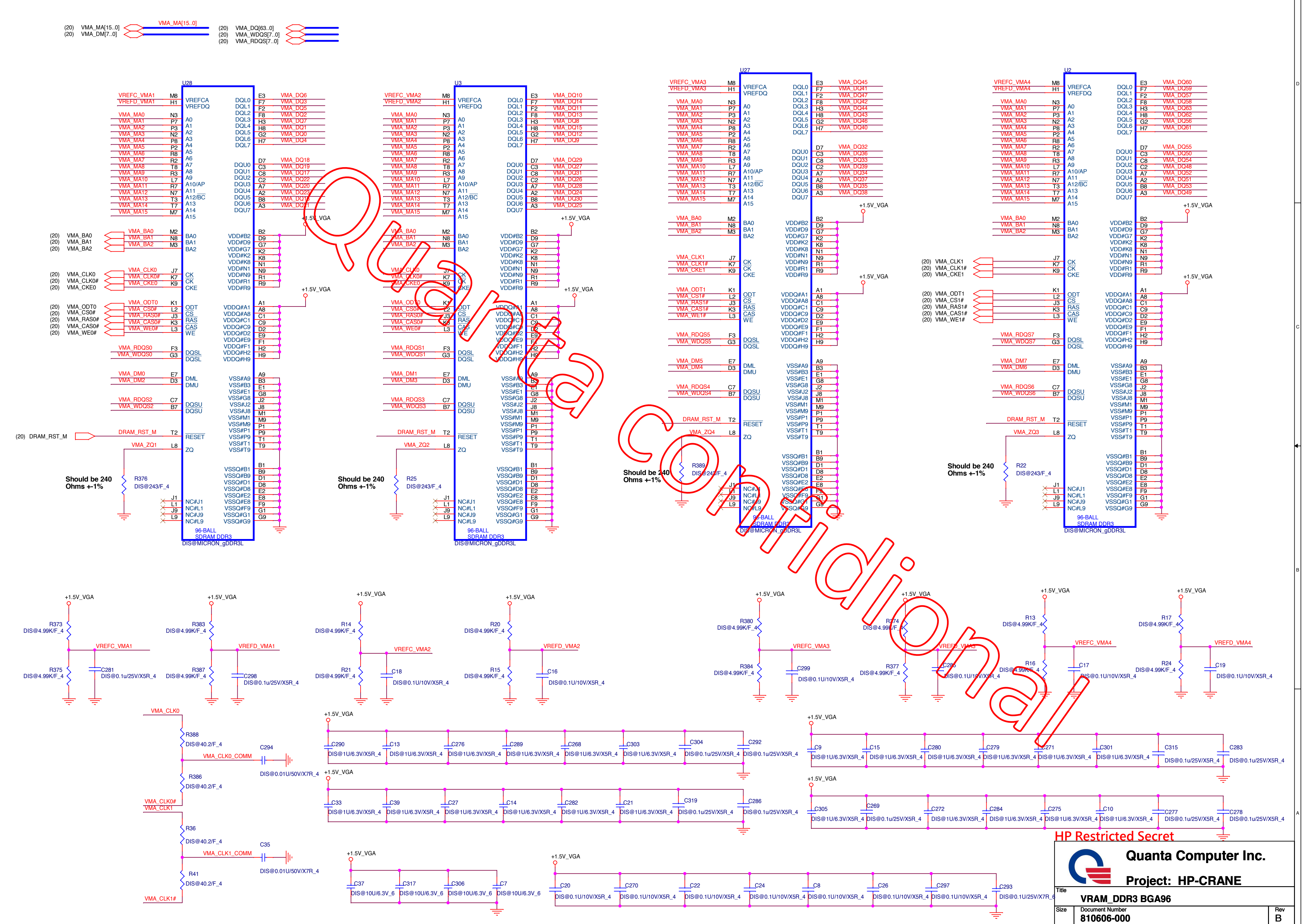
2GB gDDR3L



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Project: HP-CRANE	
Title	VRAM_DDR3 BGA96
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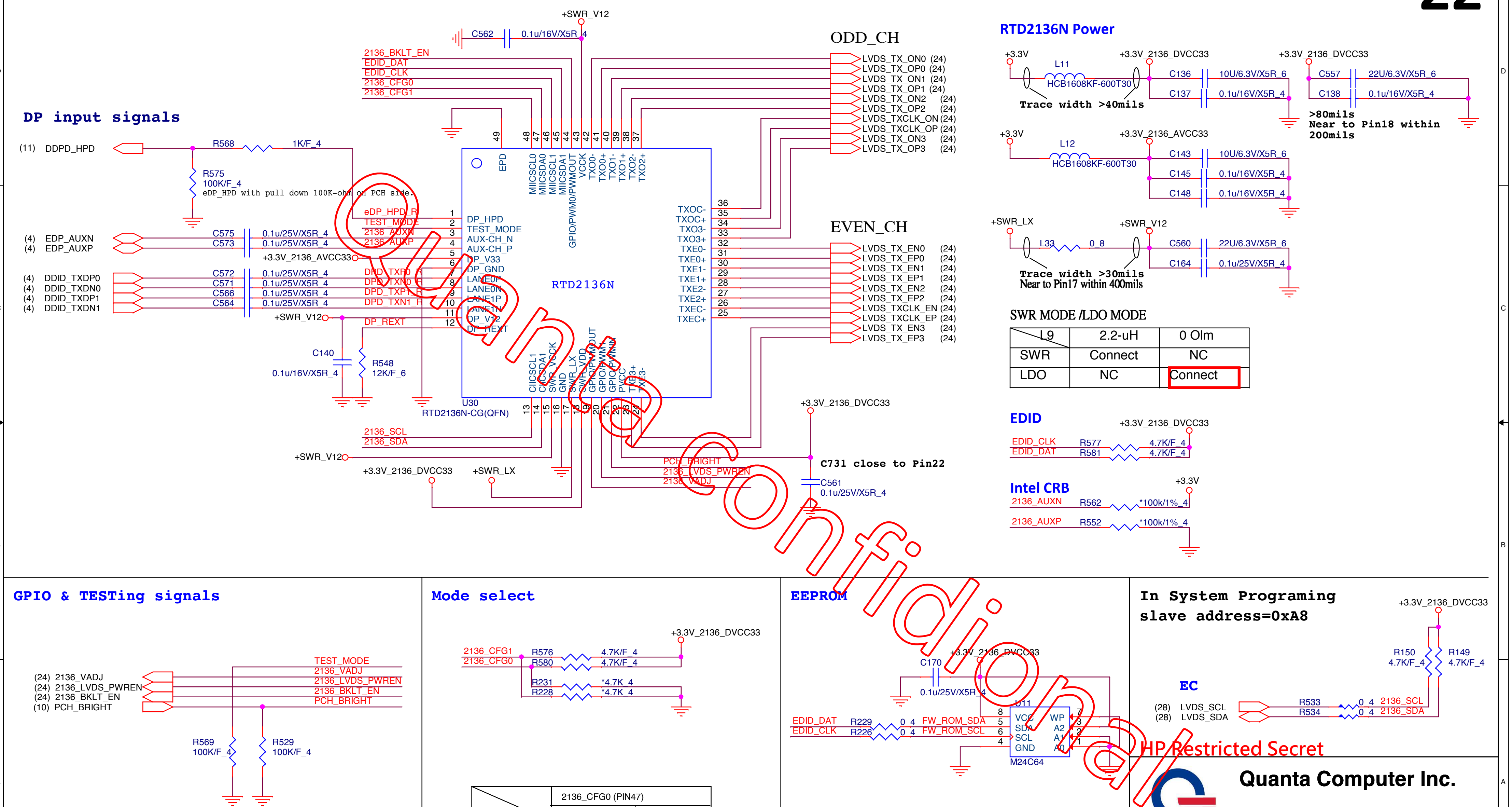
eDP to LVDS (RTD2136N-CG)



SWR MODE /LDO MODE

L9	2.2-uH	0 Olm
SWR	Connect	NC
LDO	NC	Connect

		2136_CFG0 (PIN47)	
		0	1
2136_CFG1 (PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

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Project: HP-CRANE

Title	eDP-LVDS_RTD2136N	
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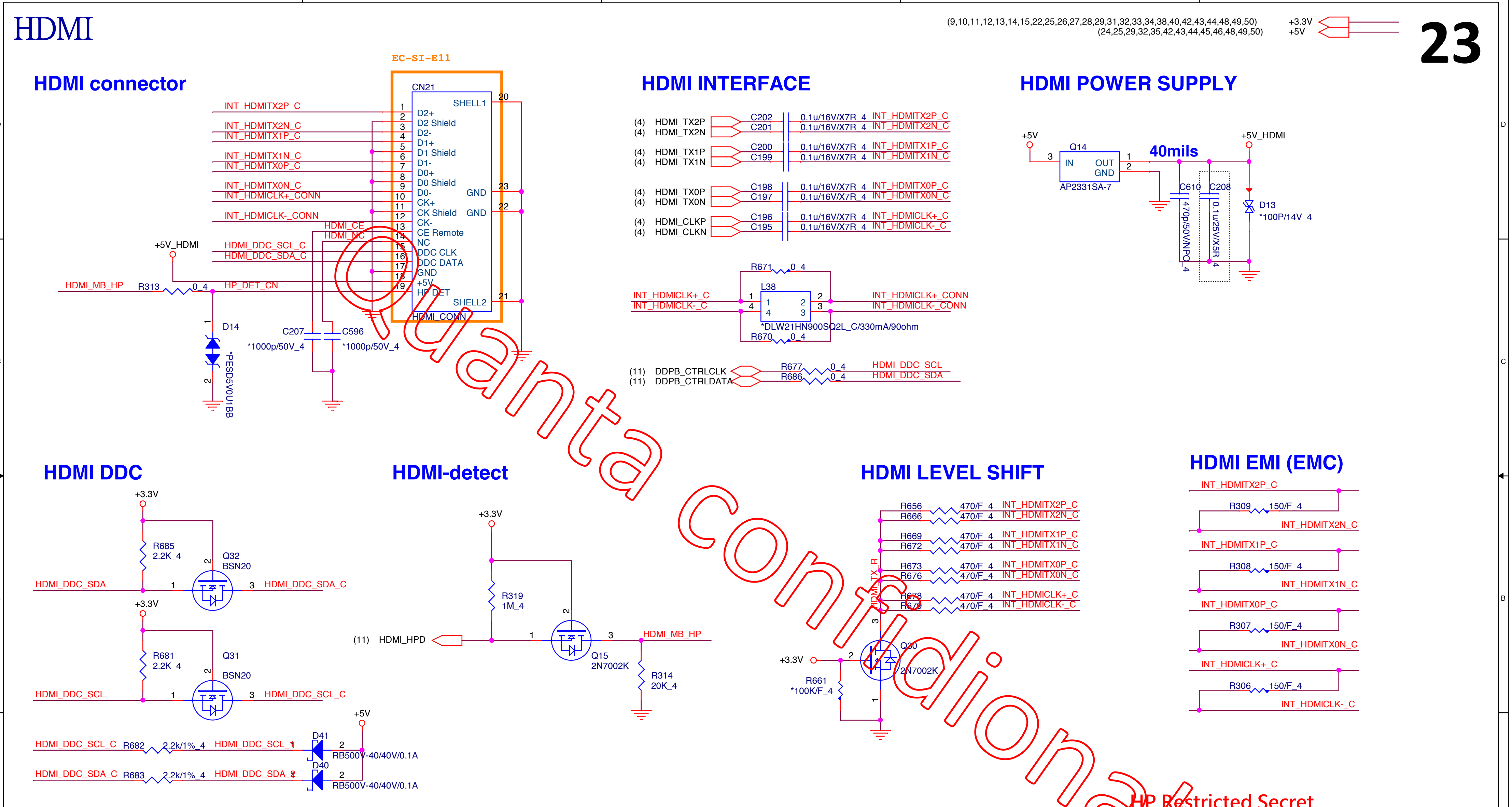

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Project: HP-CRANE

Title	HDMI	
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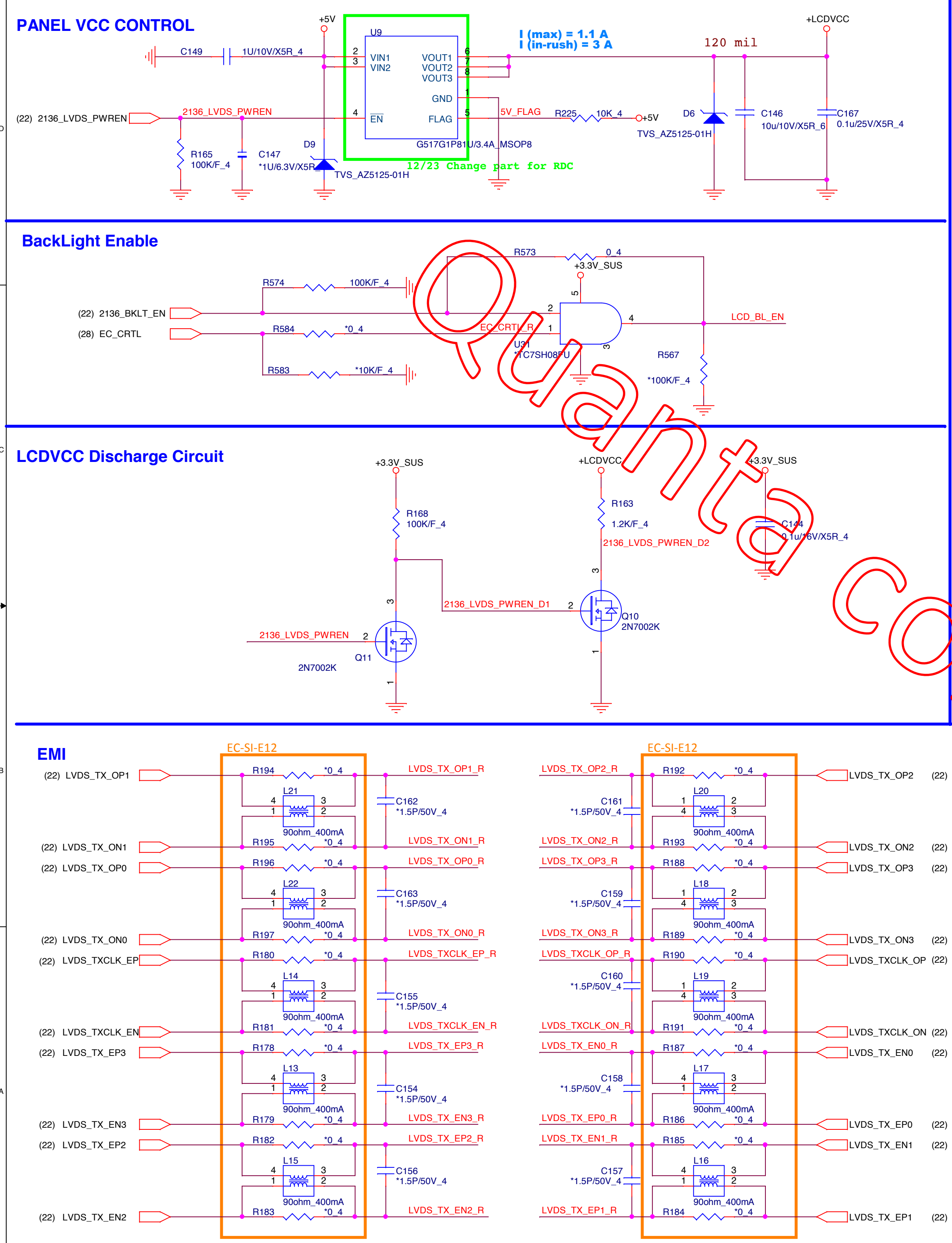
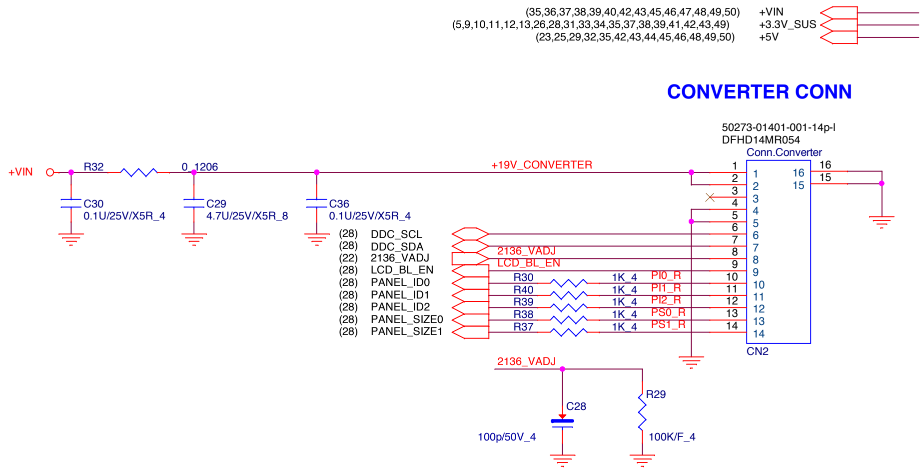
LED PANEL



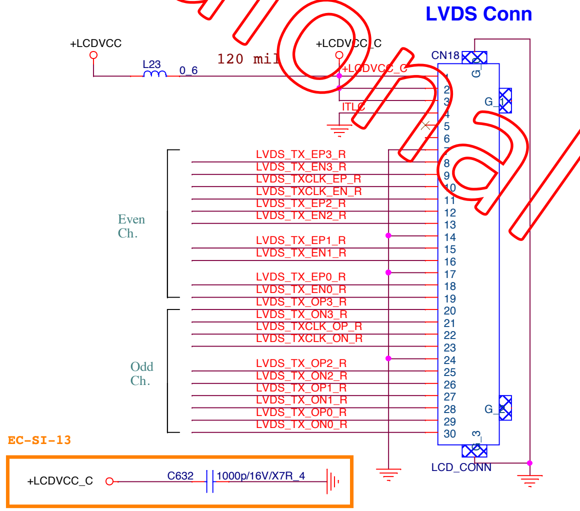


PANEL_Size Table

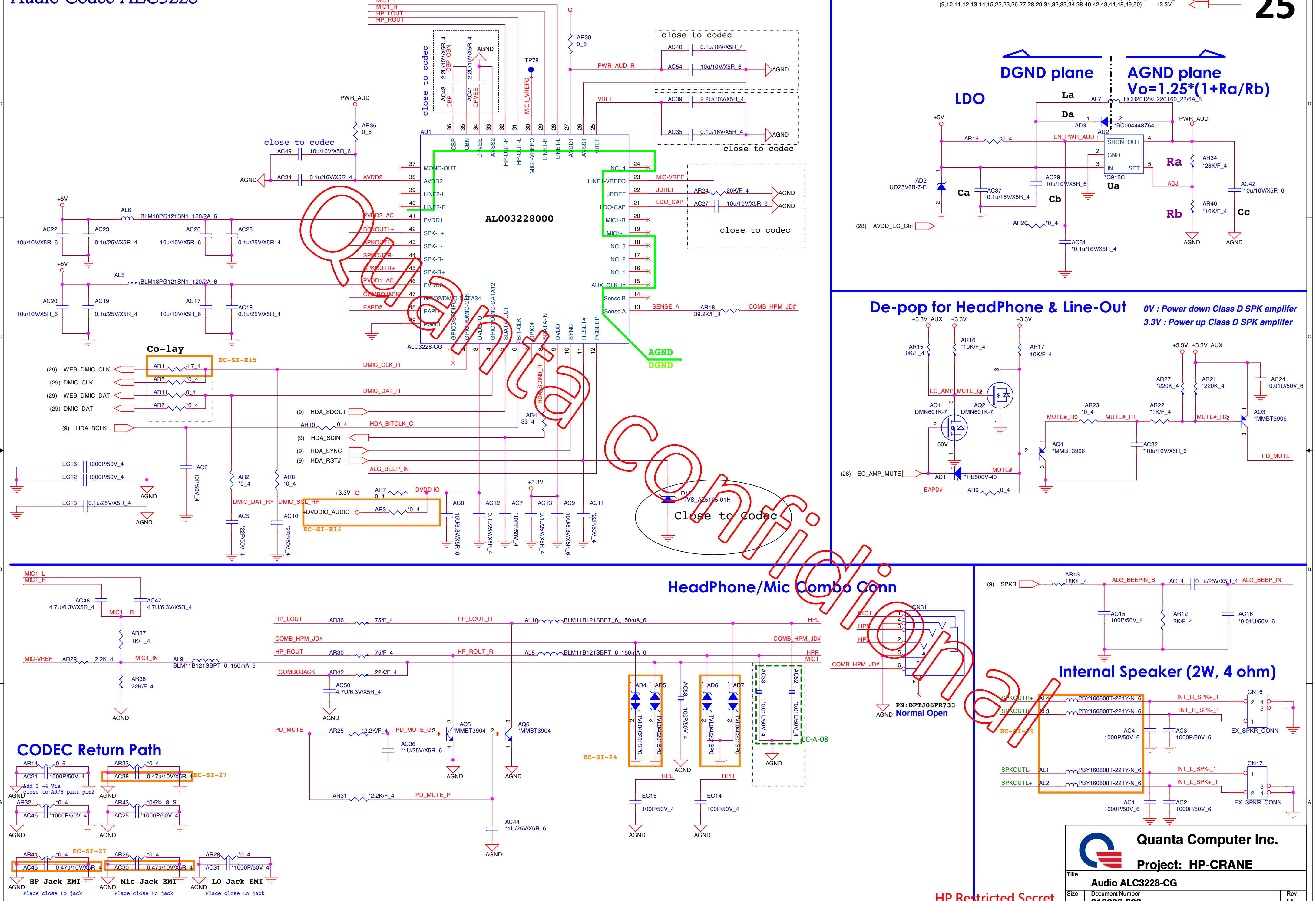
PANEL_Size[1:0]	Size
10	21.5
11	23"

PANEL_ID Table

PANEL_ID[2:0]	Panel model
000	Reserve
001	SDC LTM215HL01_H02
010	SDC LTM230HL08 LTM215HL01_H01
011	Reserve
100	LGD LM230WF3 LM215WF3
101	Reserve
110	Reserve
111	No Connect



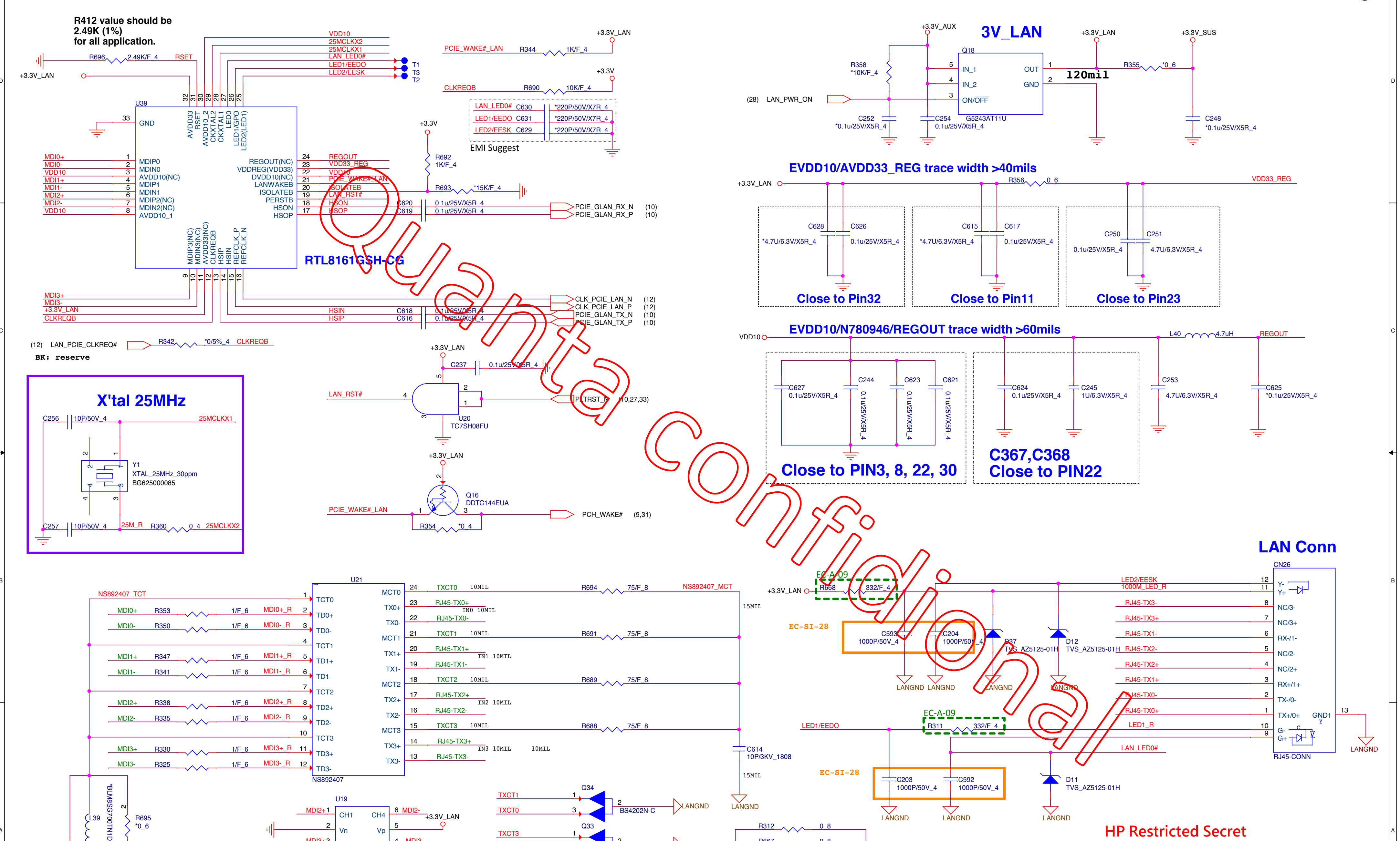
Audio Codec ALC3228



HP Restricted Secret

Quanta Computer Inc.	
Project: HP-CRANE	
Title	Audio ALC3228-CG
Size / Document Number	810606-000
Rev	B
Page Modified: Thursday, March 12, 2015	Sheet 25 of 56

LAN (RTL8161GSH) 10/100/1000



HP Restricted Secret

Quanta Computer Inc.

Project: HP-CRANE

Title	RTL8161/RJ45
Size	Document Number: 810606-000
Rev	B
Page Modified:	Thursday, March 12, 2015
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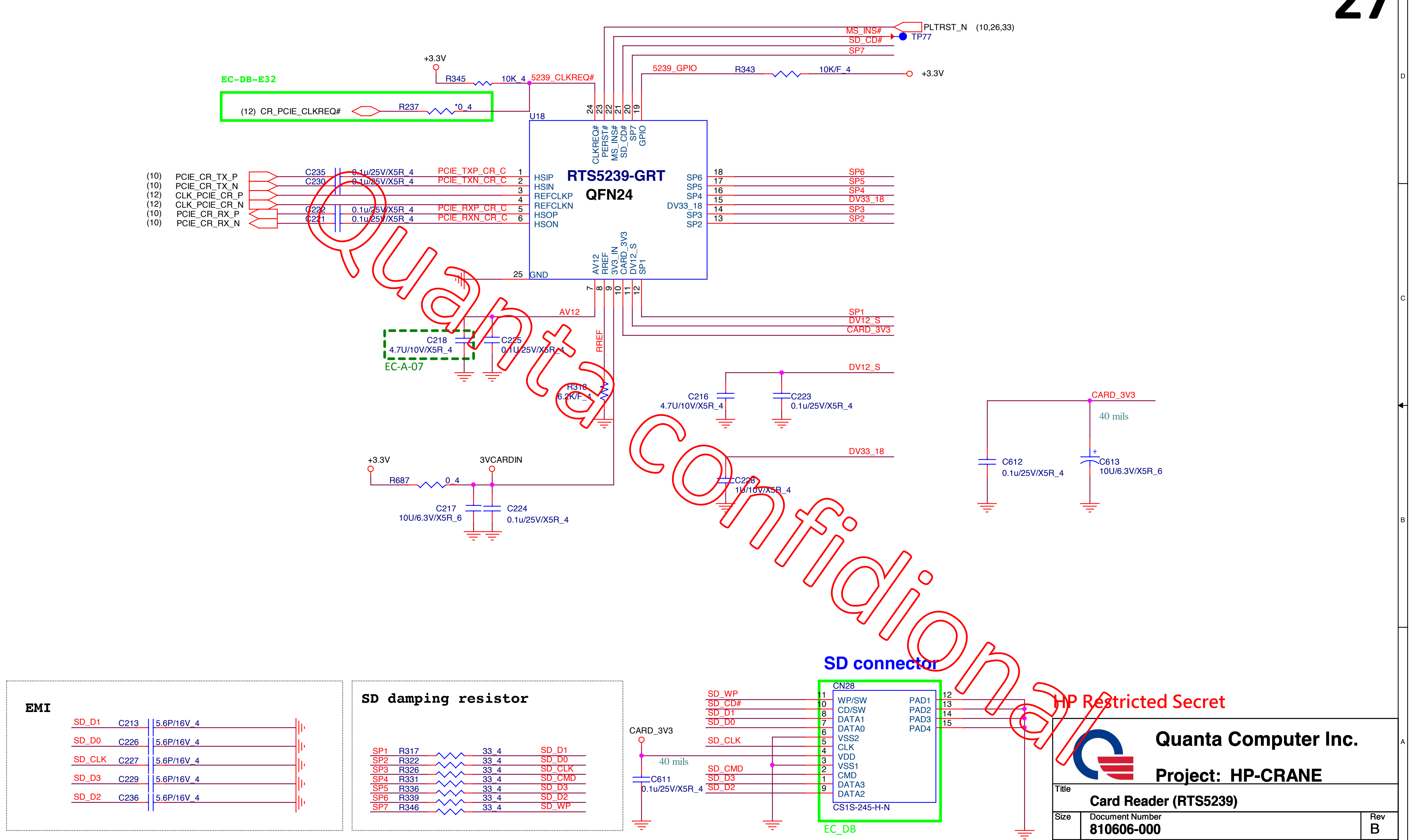
CARD READER RTD5239-GRT

27

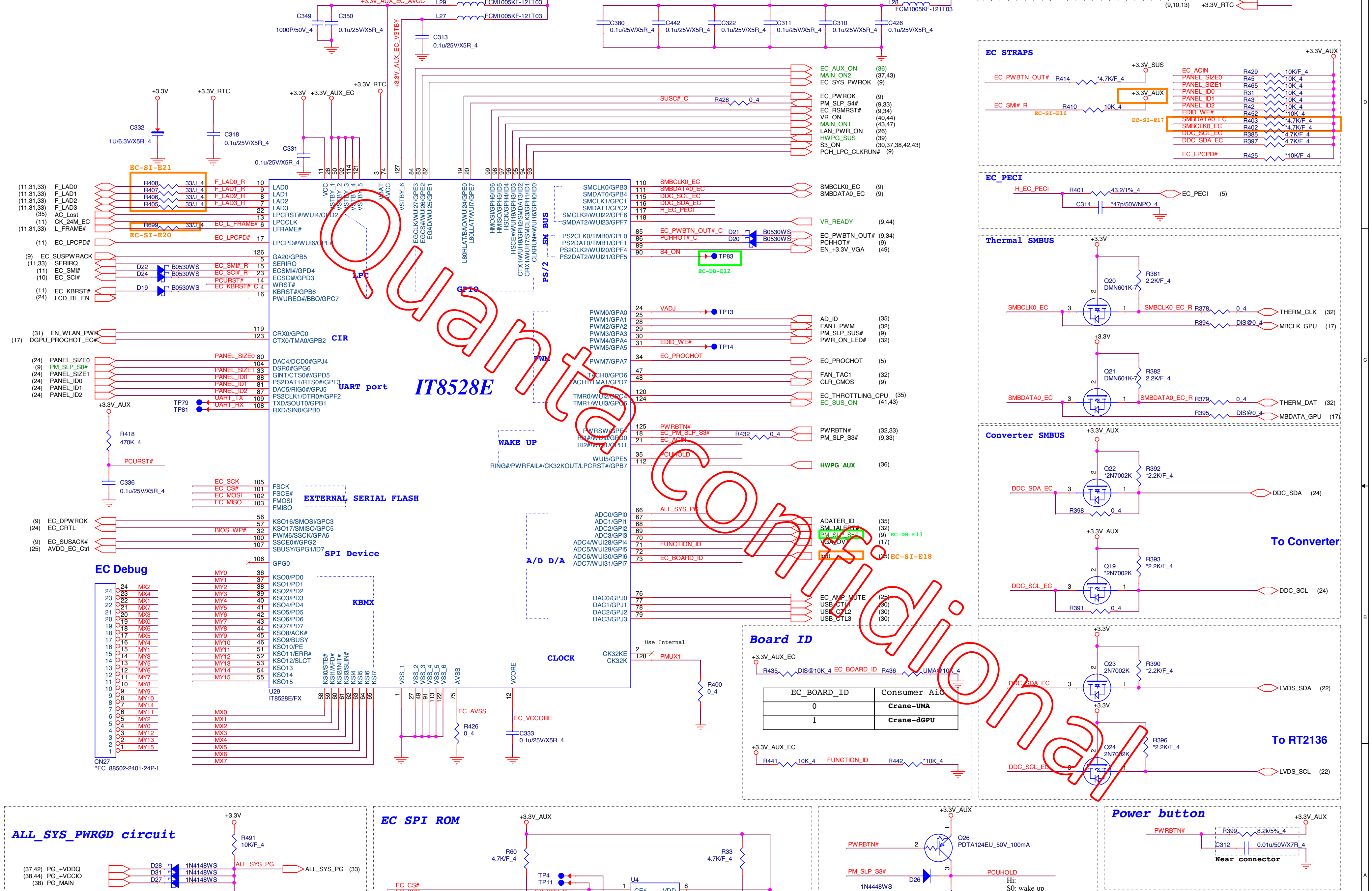


Quanta Computer Inc.

Project: HP-CRANE

Title	Card Reader (RTS5239)	
Size	Document Number 810606-000	Rev B
Page Modified: Thursday, March 12, 2015		Sheet 27 of 56

EC ITE 8528

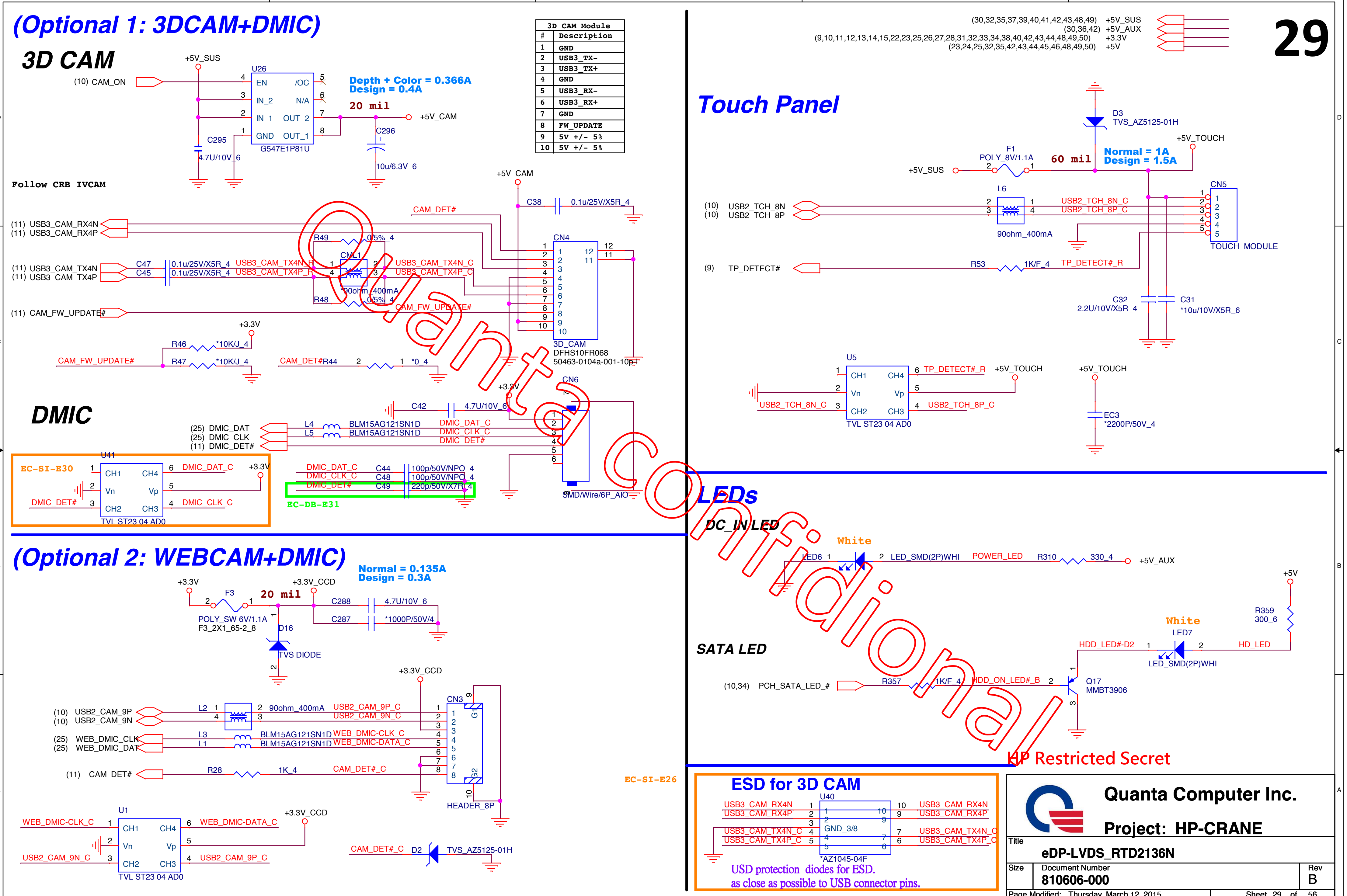


Quanta Computer Inc.

Project: HP-CRANE

Title: EC ITE 8528/ FlashROM

Size | Document Number: 810606-000 | Rev: B



3D CAM Module

#	Description
1	GND
2	USB3_TX-
3	USB3_TX+
4	GND
5	USB3_RX-
6	USB3_RX+
7	GND
8	FW_UPDATE
9	5V +/- 5%
10	5V +/- 5%

Quanta Computer Inc.

Project: HP-CRANE

Title: eDP-LVDS_RTD2136N

Size | Document Number: 810606-000 | Rev: B

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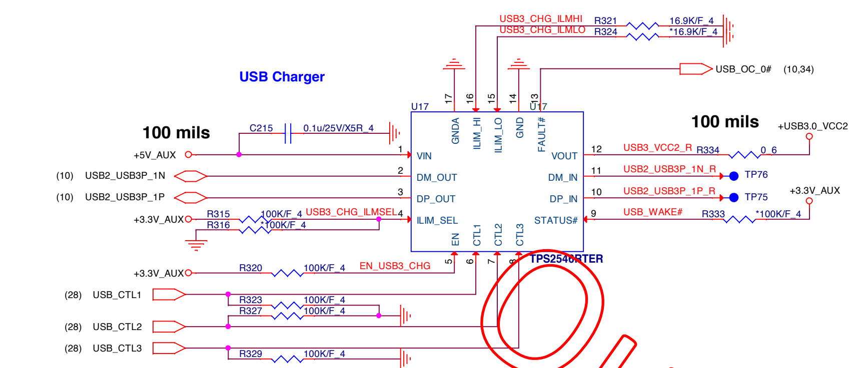
USB PORT

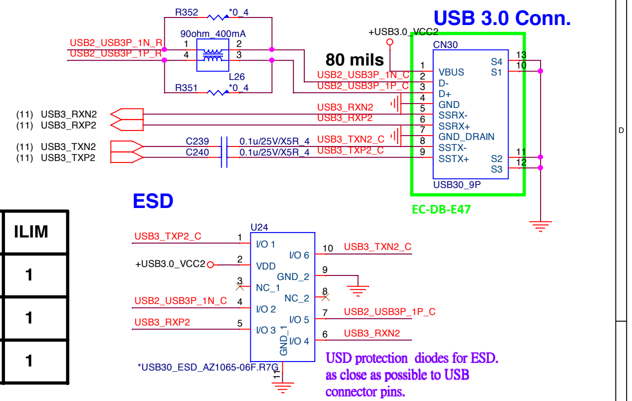
USB3.0 Charging Port

(9,13,25,26,28,34,35,36,42,50) +3.3V_AUX
(29,32,35,37,39,40,41,42,43,48,49) +5V_SUS
(29,36,42) +5V_AUX

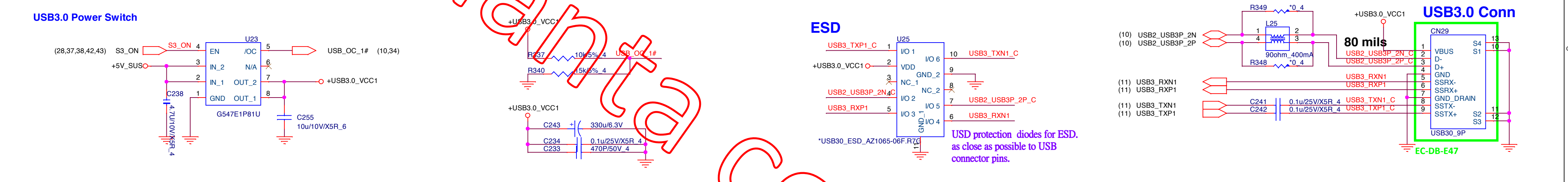


SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by
BIOS

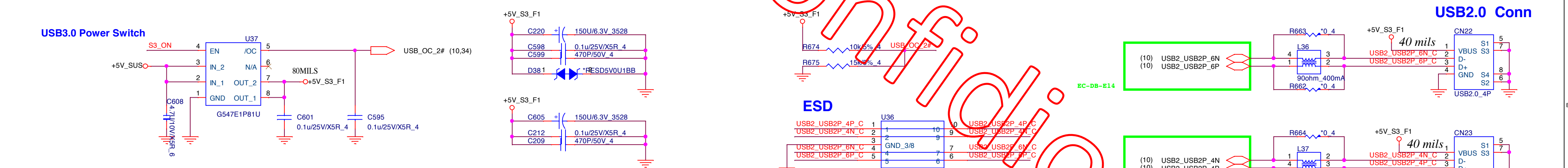
POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLDS	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS	0	0	1	1



USB3.0 PORT

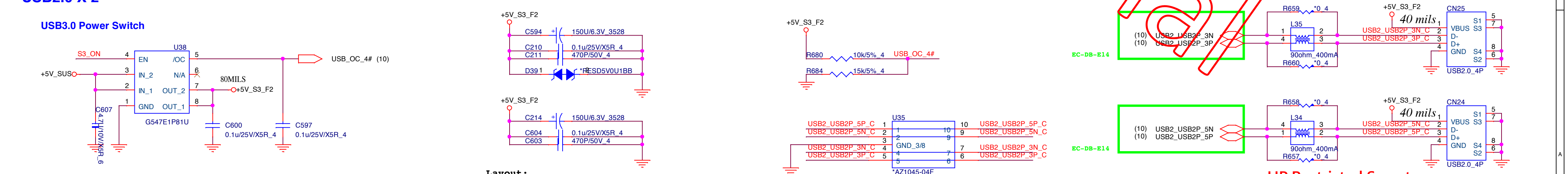


USB2.0 X 2



Layout:
1. All caps Near to Connector
2. Place D40 near CN21 and CN22

USB2.0 X 2



Layout:
1. All caps Near to Connector
2. Place D41 near CN23 and CN24

USD protection diodes for ESD.
as close as possible to USB connector pins.

Quanta Computer Inc.

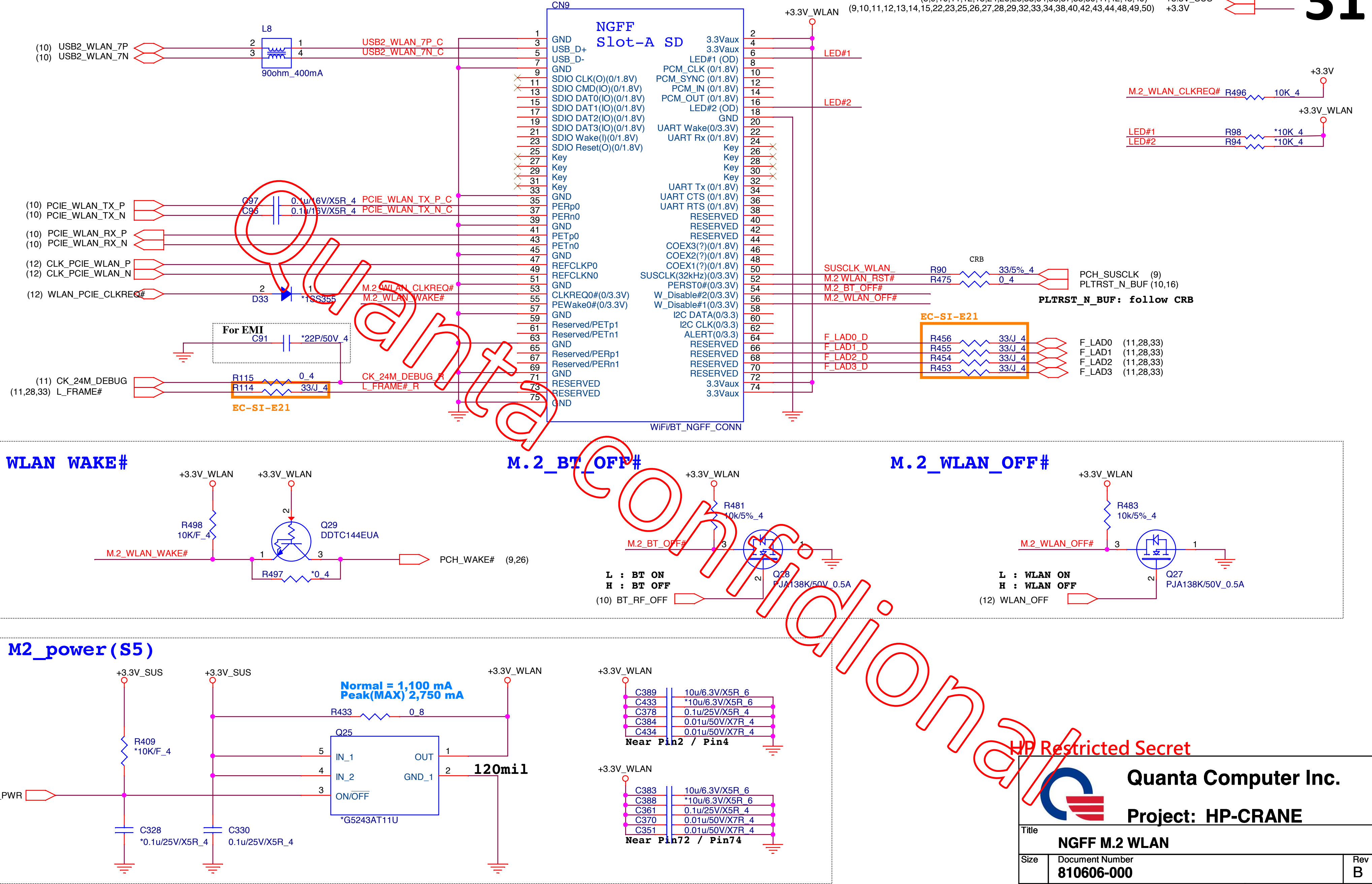
Project: HP-CRANE

Title: USB2.0/USB3.0 Conn

Size | Document Number: 810606-000 | Rev: B

NGFF M2 Socket

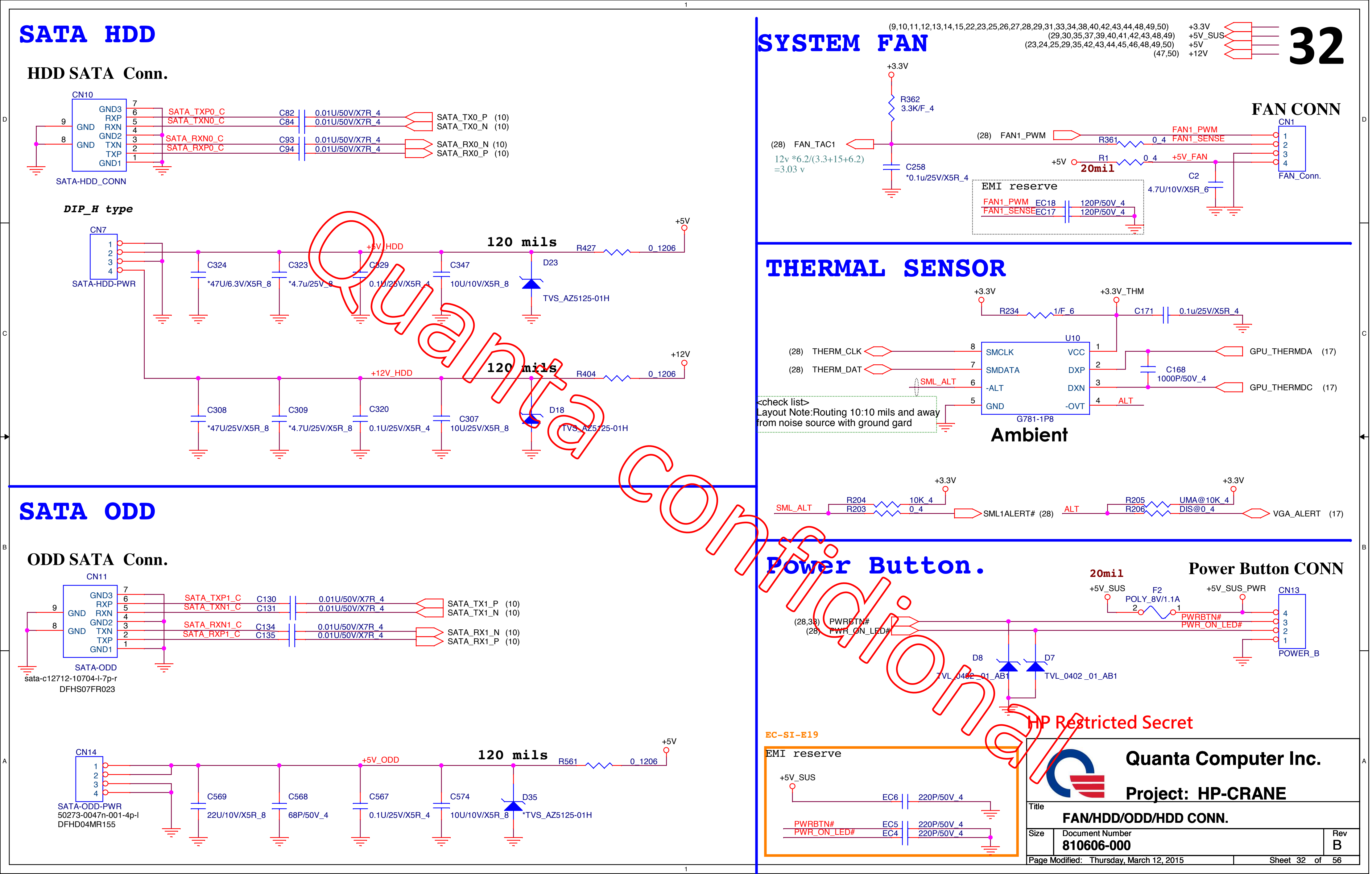
H=9.0



Quanta Computer Inc.

Project: HP-CRANE

Title	NGFF M.2 WLAN	
Size	Document Number 810606-000	Rev B
Page Modified: Thursday, March 12, 2015		Sheet 31 of 56



32
SATA HDD
HDD SATA Conn.
CN10
SATA-HDD_CONN
SATA_TXP0_C
SATA_TXN0_C
SATA_RXN0_C
SATA_RXP0_C
C82 0.01U/50V/X7R_4
C84 0.01U/50V/X7R_4
C93 0.01U/50V/X7R_4
C94 0.01U/50V/X7R_4
SATA_TX0_P (10)
SATA_TX0_N (10)
SATA_RX0_N (10)
SATA_RX0_P (10)
DIP_H type
CN7
SATA-HDD-PWR
+5V_HDD
120 mils
R427 0_1206
+5V
C324 *47U/6.3V/X5R_8
C323 *4.7u/25V_8
C329 0.1U/25V/X5R_4
C347 10U/10V/X5R_8
D23 TVS_AZ5125-01H
+12V_HDD
120 mils
R404 0_1206
+12V
C308 *47U/25V/X5R_8
C309 *4.7U/25V/X5R_8
C320 0.1U/25V/X5R_4
C307 10U/25V/X5R_8
D18 TVS_AZ5125-01H
SATA ODD
ODD SATA Conn.
CN11
SATA-ODD
sata-c12712-10704-l-7p-r
DFHS07FR023
SATA_TXP1_C
SATA_TXN1_C
SATA_RXN1_C
SATA_RXP1_C
C130 0.01U/50V/X7R_4
C131 0.01U/50V/X7R_4
C134 0.01U/50V/X7R_4
C135 0.01U/50V/X7R_4
SATA_TX1_P (10)
SATA_TX1_N (10)
SATA_RX1_N (10)
SATA_RX1_P (10)
CN14
SATA-ODD-PWR
50273-0047n-001-4p-l
DFHD04MR155
+5V_ODD
120 mils
R561 0_1206
+5V
C569 22U/10V/X5R_8
C568 68P/50V_4
C567 0.1U/25V/X5R_4
C574 10U/10V/X5R_8
D35 *TVS_AZ5125-01H
SYSTEM FAN
(9,10,11,12,13,14,15,22,23,25,26,27,28,29,31,33,34,38,40,42,43,44,48,49,50) +3.3V
(29,30,35,37,39,40,41,42,43,48,49) +5V_SUS
(23,24,25,29,35,42,43,44,45,46,48,49,50) +5V
(47,50) +12V
+3.3V
R362 3.3K/F_4
(28) FAN_TAC1
12v *6.2/(3.3+15+6.2)
=3.03 v
C258 *0.1u/25V/X5R_4
(28) FAN1_PWM
R361 0_4
FAN1_PWM
FAN1_SENSE
+5V R1 0_4 +5V_FAN
20mil
C2 4.7U/10V/X5R_6
FAN CONN
CN1
FAN_Conn.
EMI reserve
FAN1_PWM EC18 120P/50V_4
FAN1_SENSE EC17 120P/50V_4
THERMAL SENSOR
+3.3V
R234 1/F_6
+3.3V_THM
C171 0.1u/25V/X5R_4
U10
G781-1P8
(28) THERM_CLK
(28) THERM_DAT
SMCLK VCC
SMDATA DXP
-ALT DXN
GND -OVT
SML_ALT
ALT
GPU_THERMDA (17)
GPU_THERMDC (17)
C168 1000P/50V_4
<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard
Ambient
+3.3V
SML_ALT
R204 10K_4
R203 0_4
SML1ALERT# (28)
+3.3V
ALT
R205 UMA@10K_4
R206 DIS@0_4
VGA_ALERT (17)
Power Button.
20mil
Power Button CONN
+5V_SUS
F2 POLY_8V/1.1A
+5V_SUS_PWR
CN13
POWER_B
(28,33) PWRBTN#
(28) PWR_ON_LED#
PWRBTN#
PWR_ON_LED#
D8 TVL_0402_01_AB1
D7 TVL_0402_01_AB1
EC-SI-E19
EMI reserve
+5V_SUS
EC6 220P/50V_4
PWRBTN# EC5 220P/50V_4
PWR_ON_LED# EC4 220P/50V_4
HP Restricted Secret
Quanta Computer Inc.
Project: HP-CRANE
Title
FAN/HDD/ODD/HDD CONN.
Size
Document Number
810606-000
Rev
B
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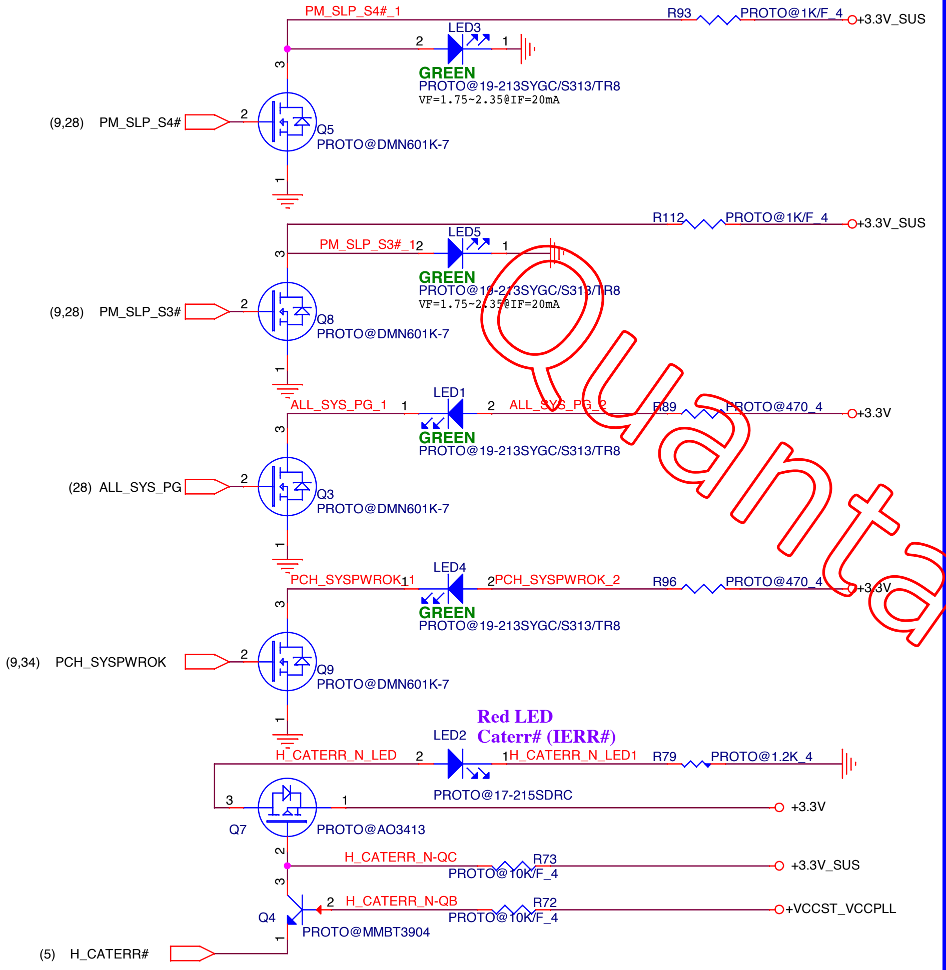
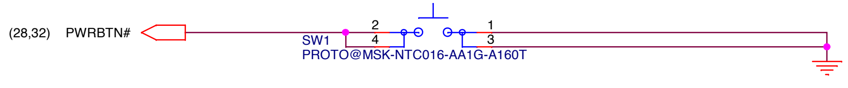
PCA debug LED requirement:



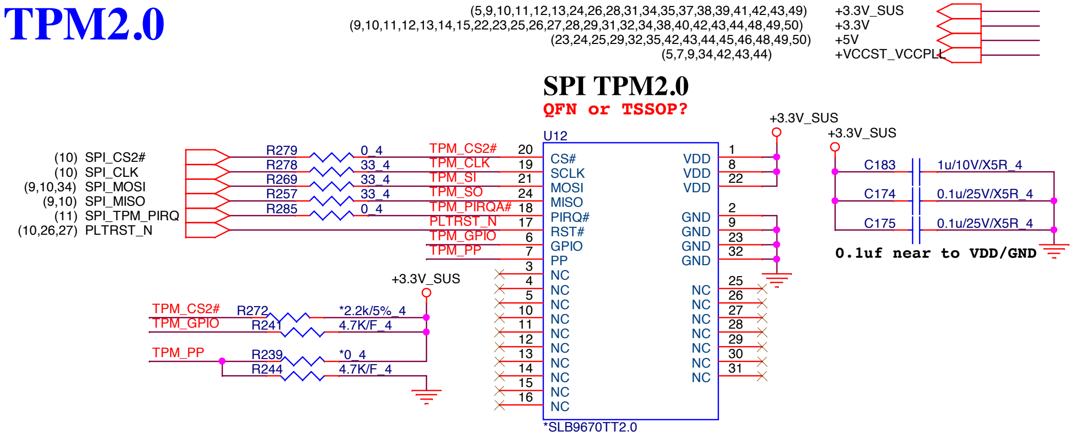
SW1 For Debug.MP will remove it.



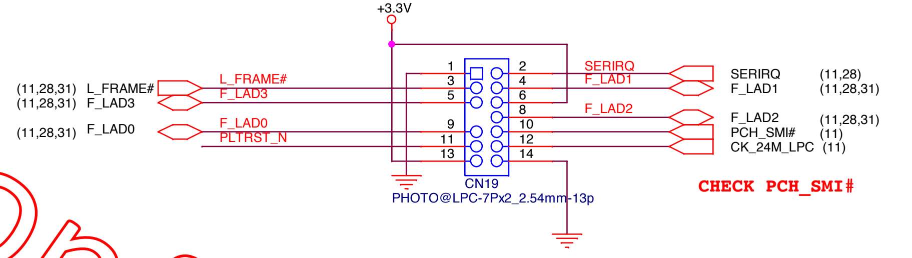
TPM2.0

SPI TPM2.0

QFN or TSSOP?



LPC HEADER



CHECK PCH_SMI#

Quanta Computer Inc.		
Project: HP-CRANE		
Title: Debug /LPC Header/TPM		
Size	Document Number: 810606-000	Rev: B
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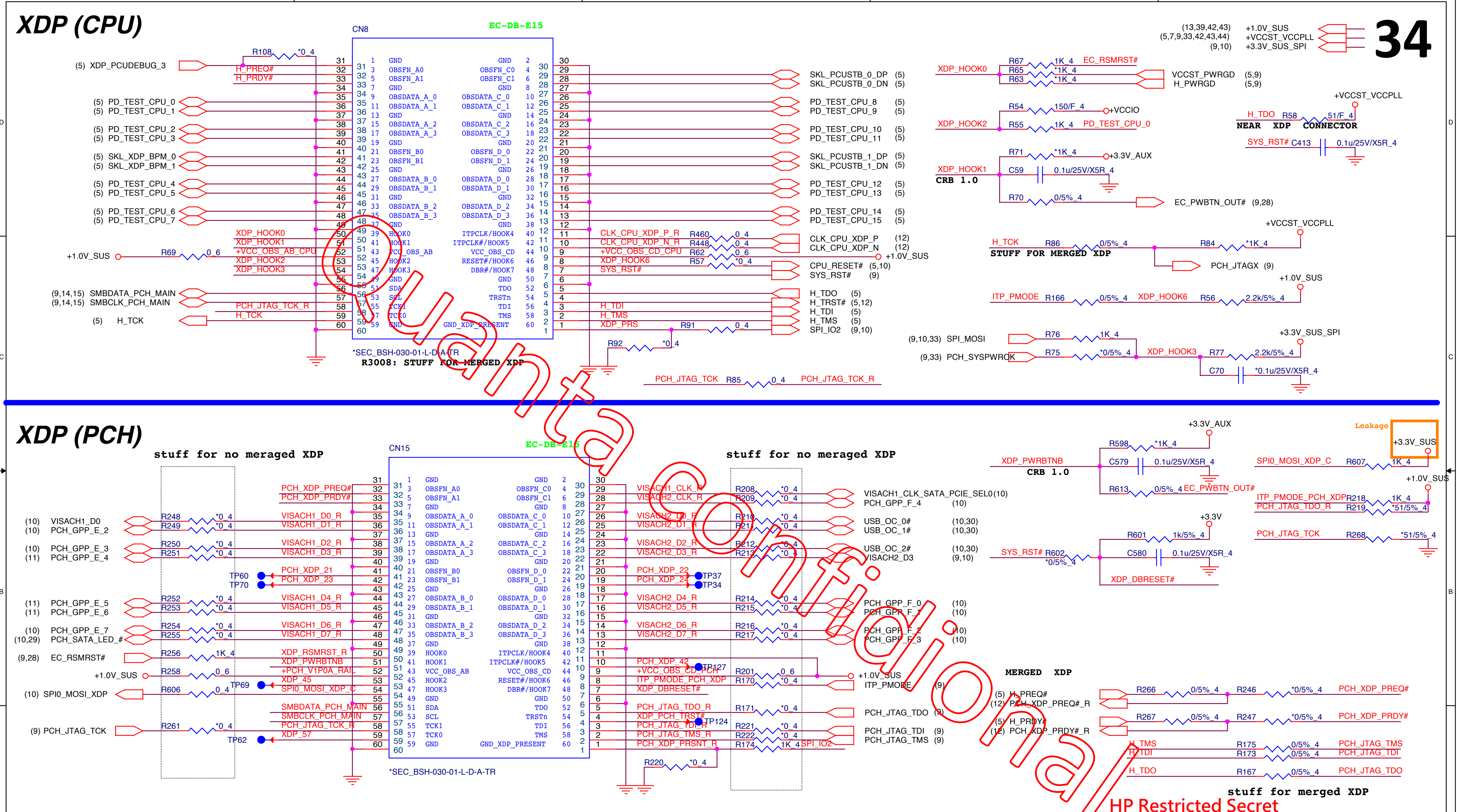

Quanta Computer Inc.

Project: HP-CRANE

Title: XDP DEBUG

Size | Document Number: 810606-000 | Rev: B

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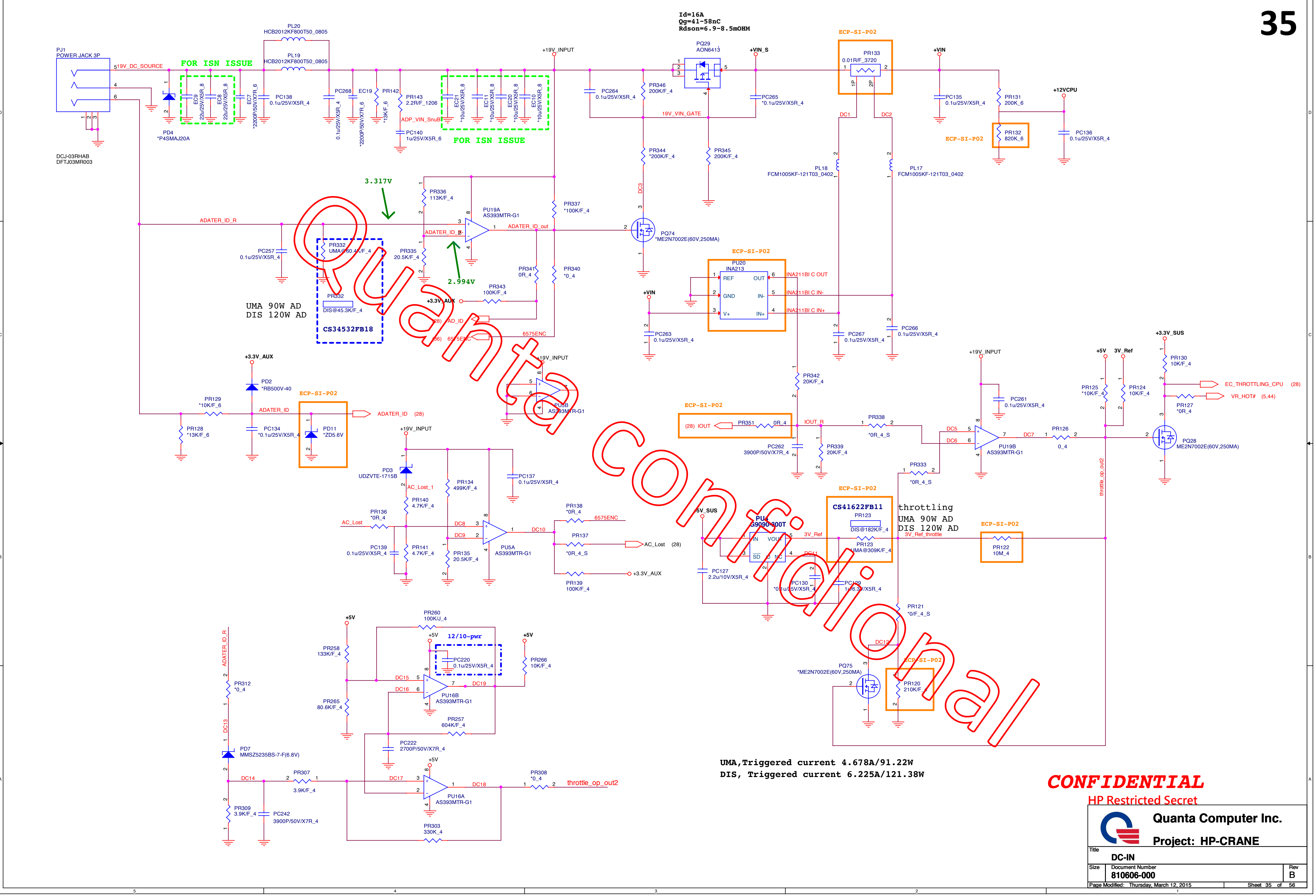
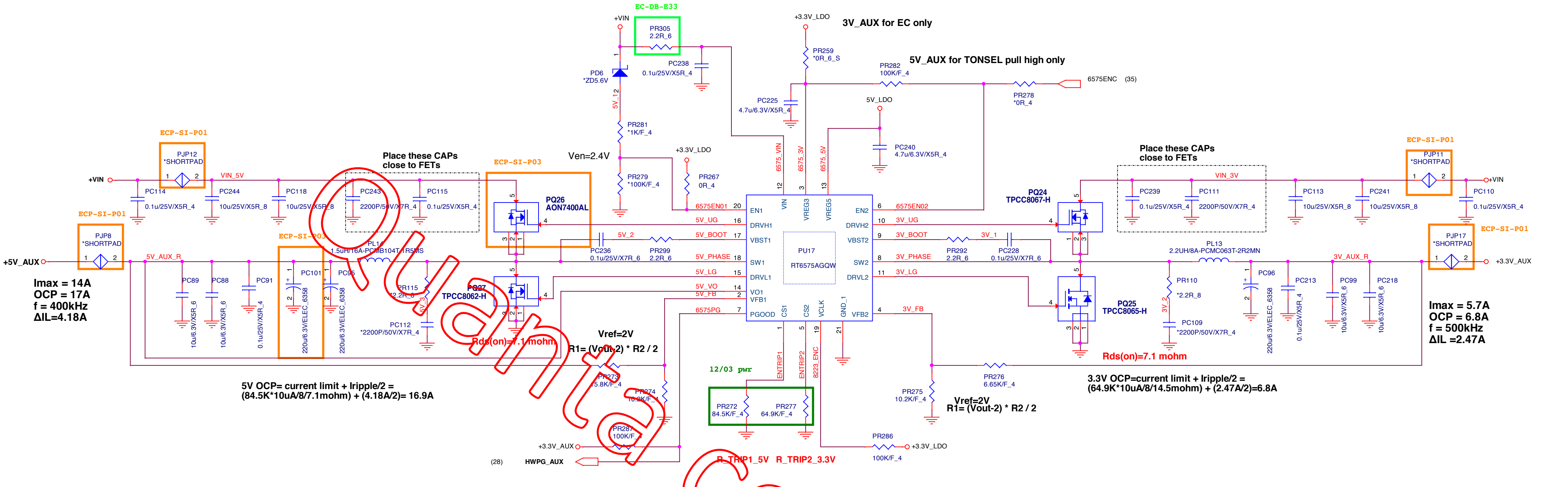
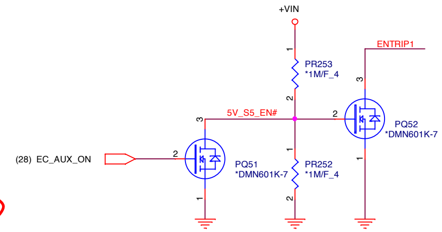


Quanta Computer Inc.
Project: HP-CRANE

Title	DC-IN	
Size	Document Number 810606-000	Rev B
Page Modified: Thursday, March 12, 2015		Sheet 35 of 56



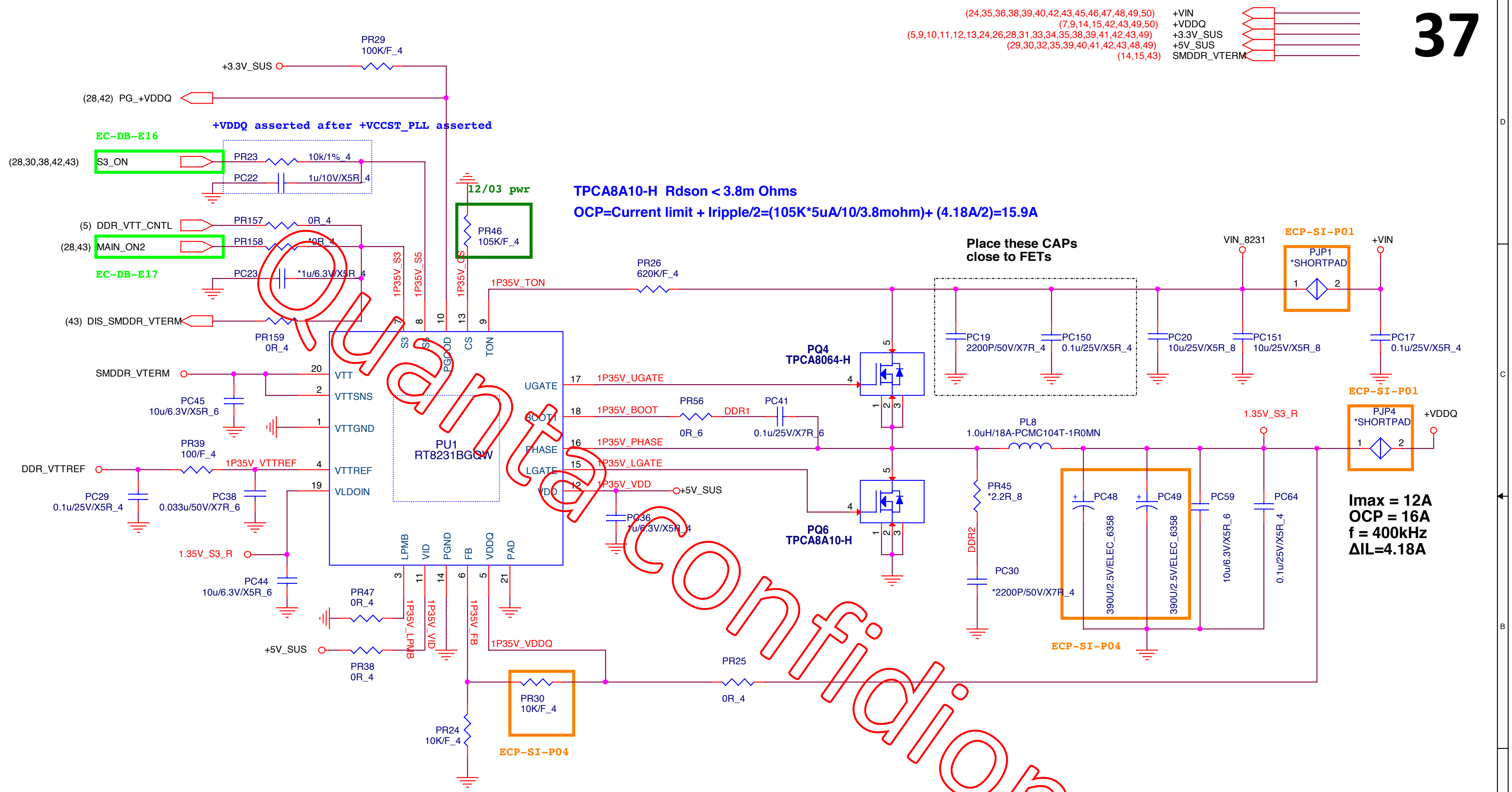


L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

Power On sequencing

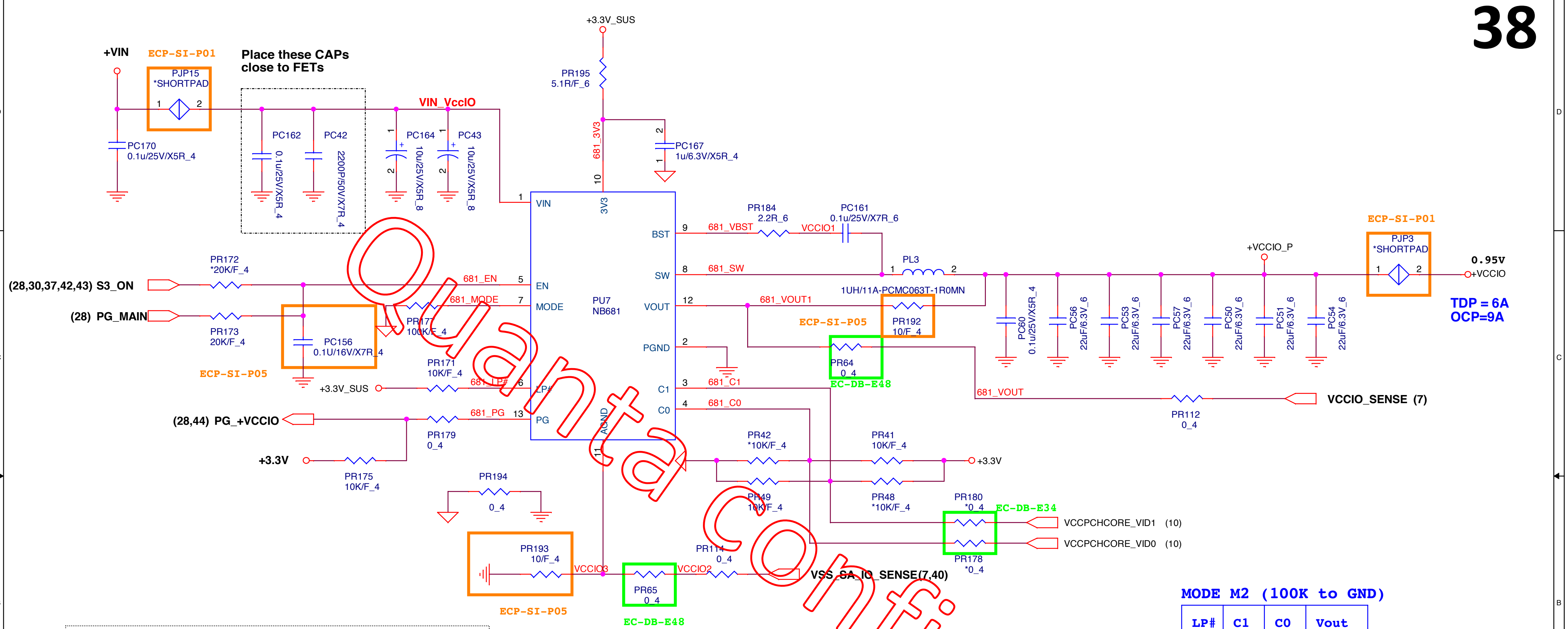
EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON



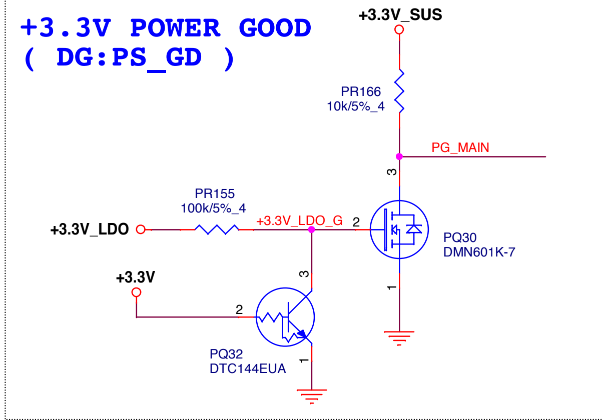
Quanta Computer Inc.

Project: HP-CRANE

Title	+VDDQ /SMDDR_VTERM (RT8231BGQW)	
Size	Document Number 810606-000	Rev B
Page Modified: Thursday, March 12, 2015		Sheet 37 of 56



+3.3V POWER GOOD
(DG:PS_GD)



MODE M2 (Float)-Pre-ES

LP#	C1	C0	Vout
0	x	x	0.7V
1	0	0	0.8V
1	0	1	0.85V
1	1	0	0.9V
1	1	1	0.95V

MODE M2 (Float)-ES

LP#	C1	C0	Vout
0	x	x	0.7V
1	0	0	0.85V
1	0	1	0.9V
1	1	0	0.95V
1	1	1	1V

MODE M2 (100K to GND)

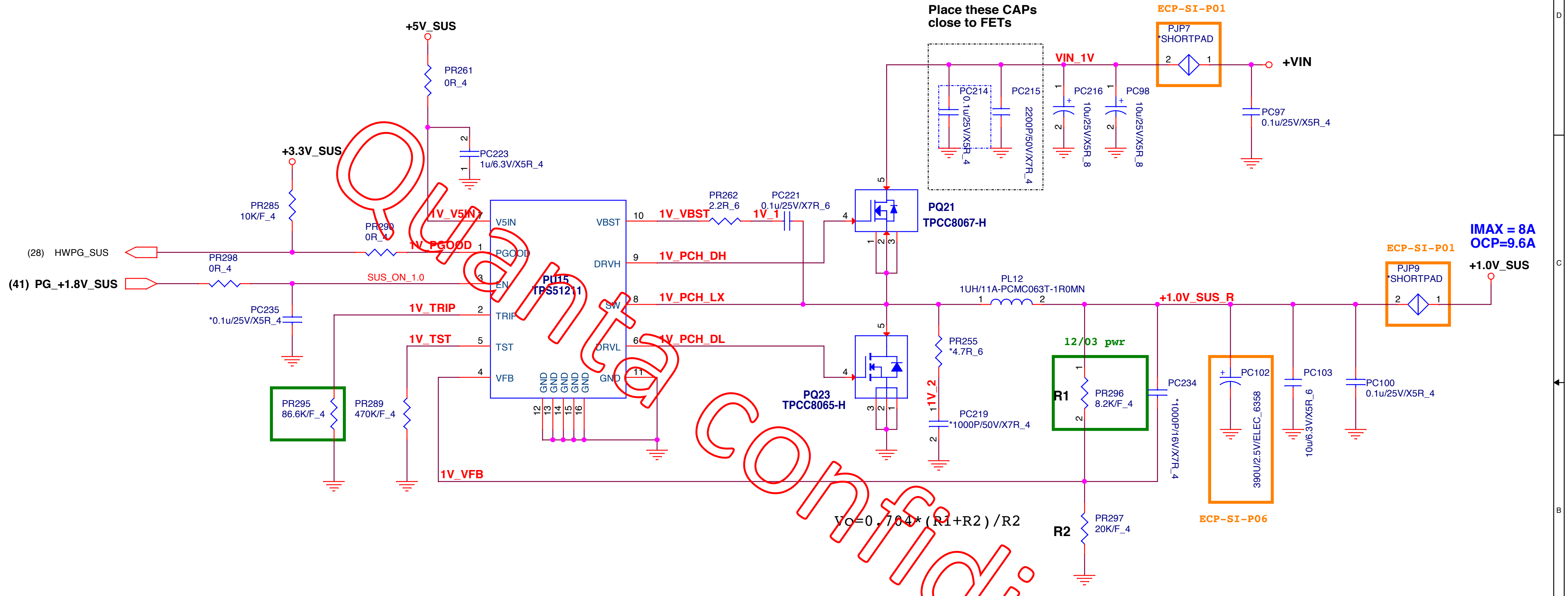
LP#	C1	C0	Vout
0	x	x	0V
1	0	0	0.8V
1	0	1	0.95V
1	1	0	1V
1	1	1	1.05V

Quanta Computer Inc.

Project: HP-CRANE

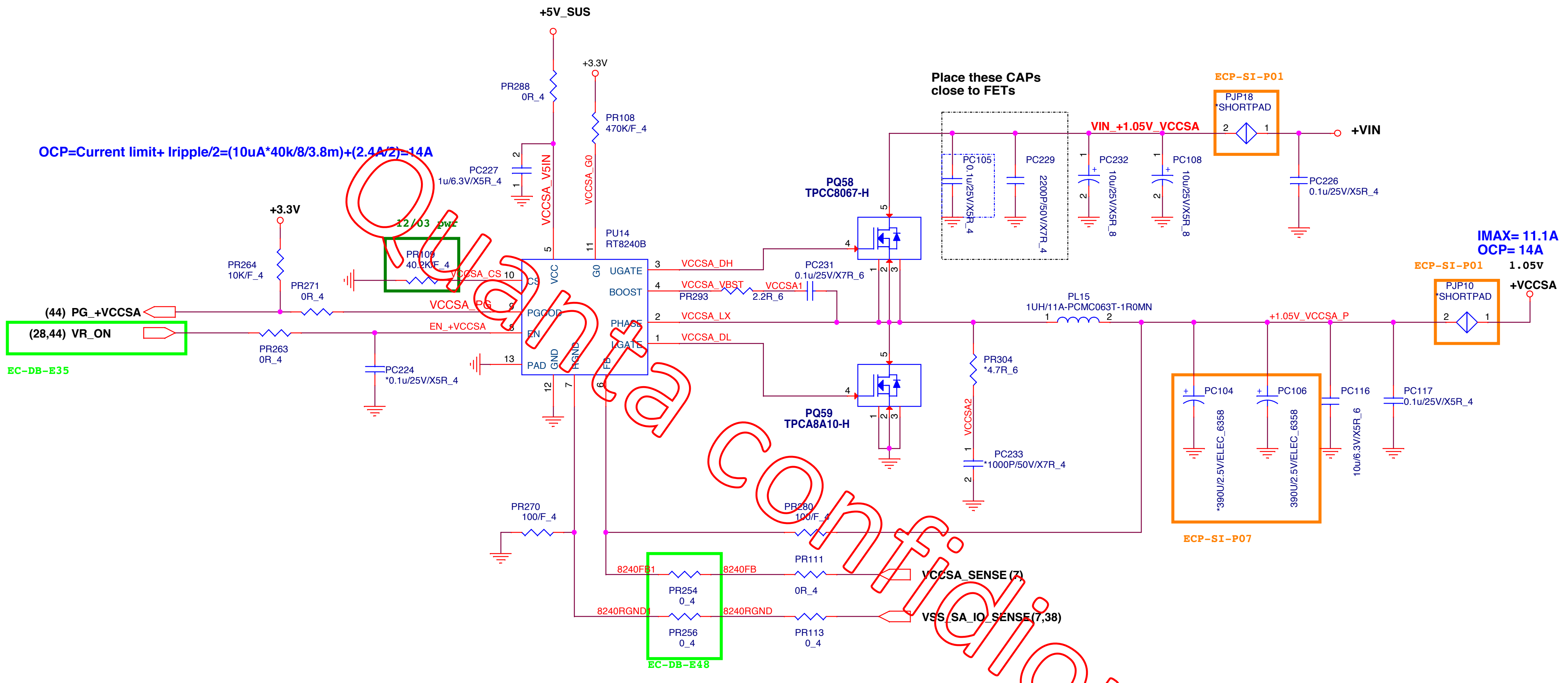
Title: +VCCIO(NB681)

Size | Document Number: 810606-000 | Rev: B



Quanta Computer Inc.
Project: HP-CRANE

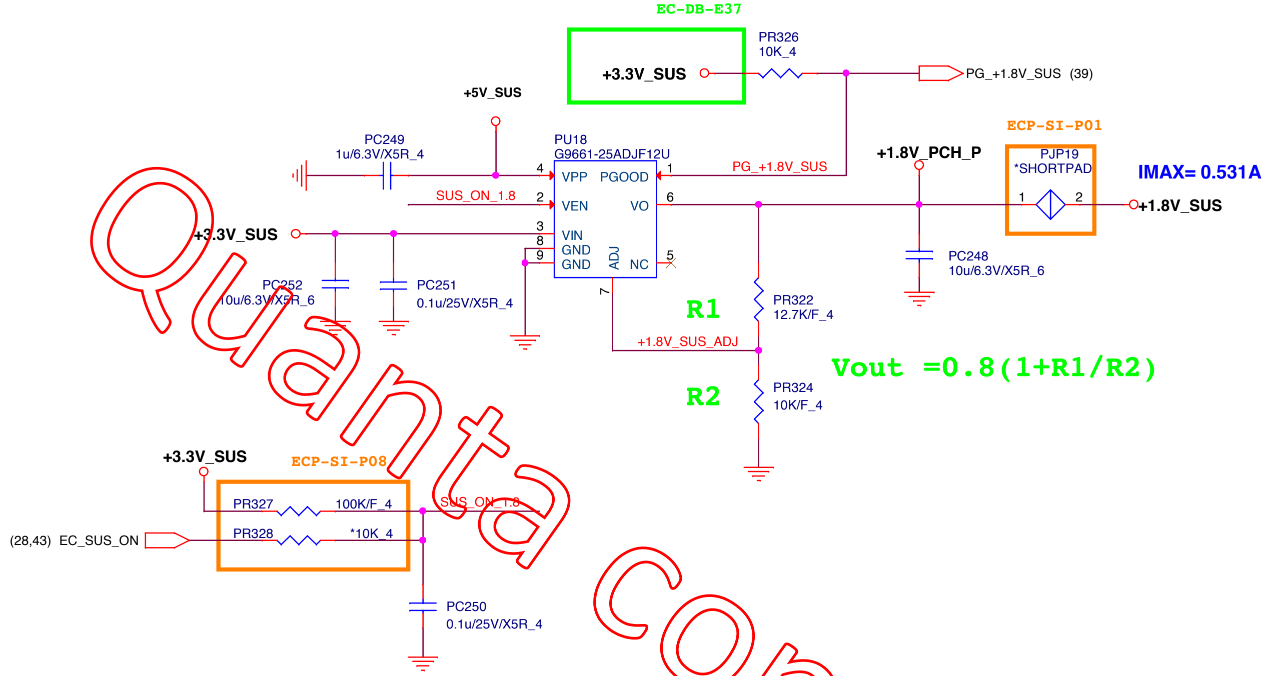
Title	+1.0V_SUS(TPS51211)	
Size	Document Number 810606-000	Rev B
Page Modified: Thursday, March 12, 2015		Sheet 39 of 56



Quanta Computer Inc.

Project: HP-CRANE

Title	+VCCSA(RT8240B)	
Size	Document Number: 810606-000	Rev: B
Page Modified: Thursday, March 12, 2015		Sheet 40 of 56



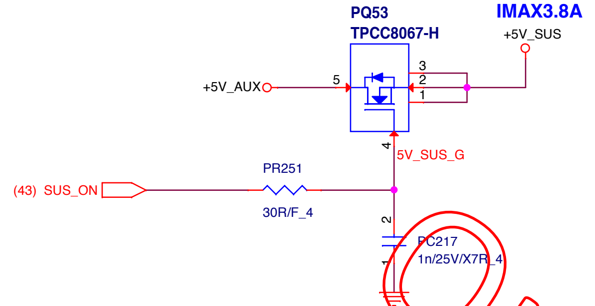
Quanta Computer Inc.

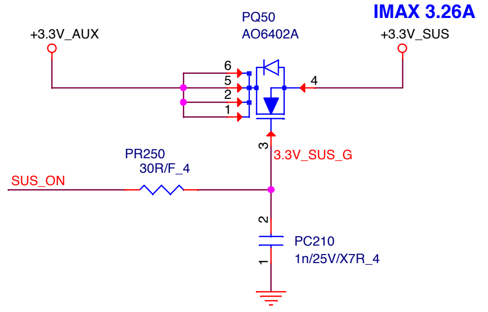
Project: HP-CRANE

Title: +1.8V_SUS (G9661)

Size | Document Number: 810606-000 | Rev: B

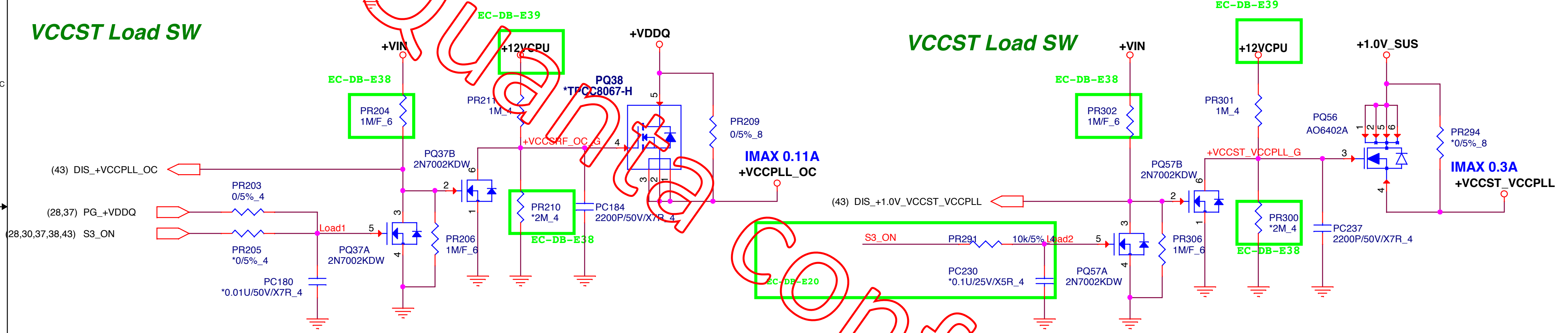
SUS ON Load SW



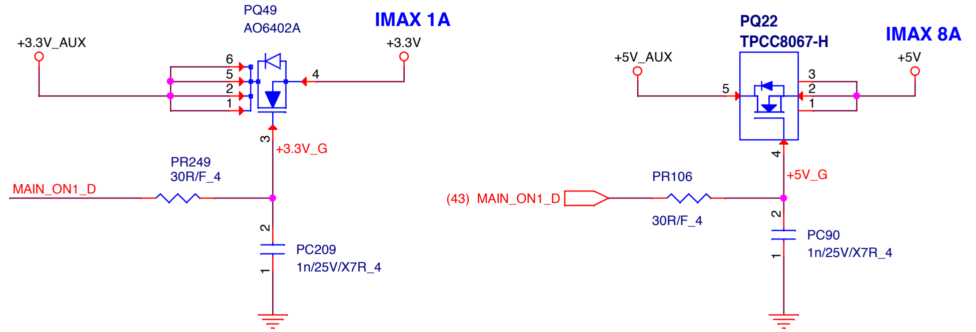


VCCST Load SW

VCCST Load SW



MAIN ON_1 Load SW



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
ME3424D-G	TSOP-6	5.0A/6.7A	42m	+/- 20V
TPCC8067-H	3x3	9A	26m	+/- 20V
TPCA8064-H	SO-8	20A	7.9m	+/- 20V

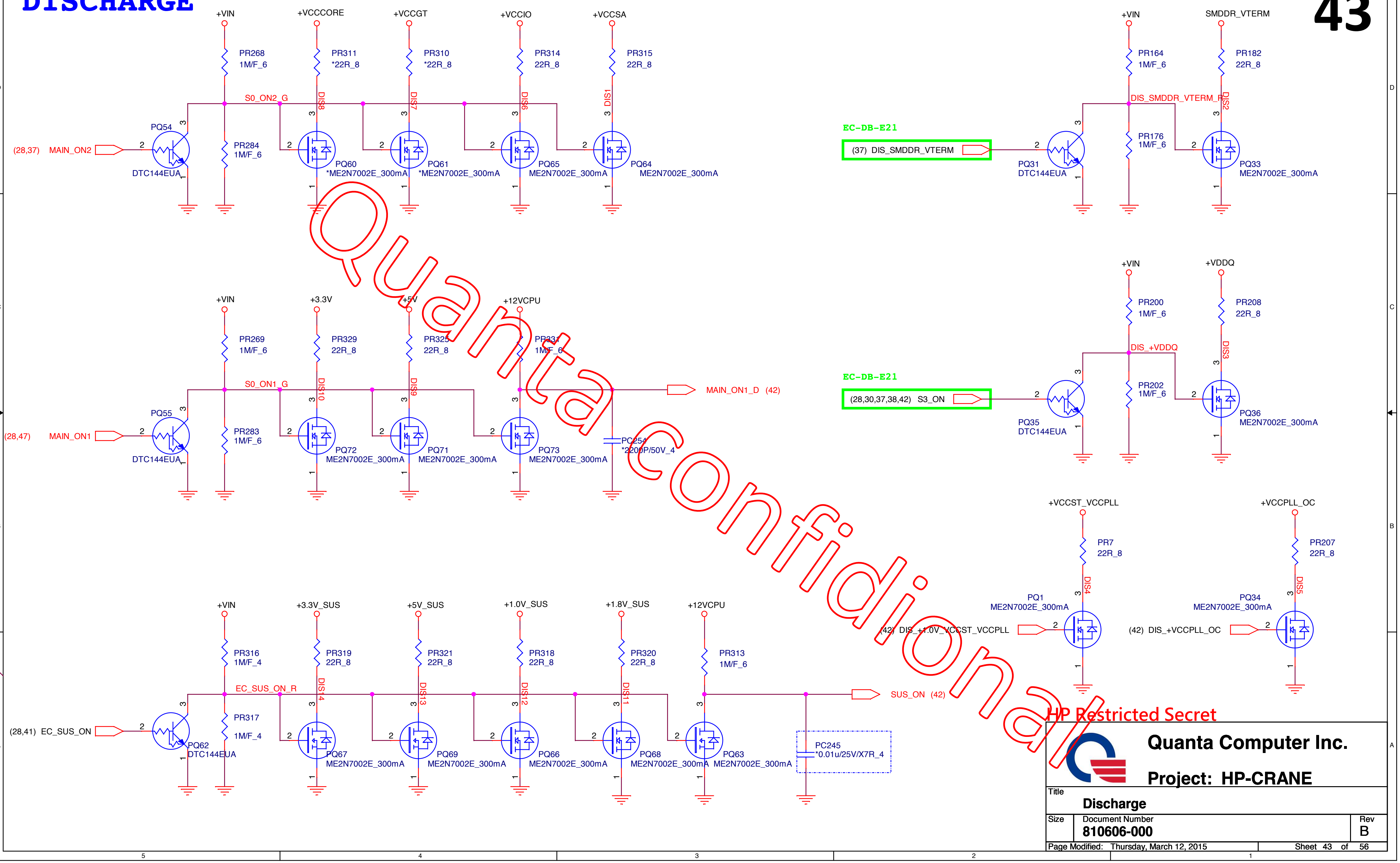
Quanta Computer Inc.

Project: HP-CRANE

Title: Load Switch

Size | Document Number: 810606-000 | Rev: B

DISCHARGE



+VIN
+VCCCORE
+VCCGT
+VCCIO
+VCCSA
PR268 1M/F_6
PR311 *22R_8
PR310 *22R_8
PR314 22R_8
PR315 22R_8
S0_ON2_G
DIS8
DIS7
DIS6
DIS1
PQ54
(28,37) MAIN_ON2
DTC144EUA
PR284 1M/F_6
PQ60 *ME2N7002E_300mA
PQ61 *ME2N7002E_300mA
PQ65 ME2N7002E_300mA
PQ64 ME2N7002E_300mA
+VIN
SMDDR_VTERM
PR164 1M/F_6
PR182 22R_8
DIS_SMDDR_VTERM_R
DIS2
EC-DB-E21
(37) DIS_SMDDR_VTERM
PQ31 DTC144EUA
PR176 1M/F_6
PQ33 ME2N7002E_300mA
+VIN
+3.3V
+5V
+12VCPU
PR269 1M/F_6
PR329 22R_8
PR325 22R_8
PR331 1M/F_6
S0_ON1_G
DIS10
DIS9
MAIN_ON1_D (42)
PQ55
(28,47) MAIN_ON1
DTC144EUA
PR283 1M/F_6
PQ72 ME2N7002E_300mA
PQ71 ME2N7002E_300mA
PQ73 ME2N7002E_300mA
PC254 *2200P/50V_4
+VIN
+VDDQ
PR200 1M/F_6
PR208 22R_8
DIS_+VDDQ
DIS3
EC-DB-E21
(28,30,37,38,42) S3_ON
PQ35 DTC144EUA
PR202 1M/F_6
PQ36 ME2N7002E_300mA
+VCCST_VCCPLL
+VCCPLL_OC
PR7 22R_8
PR207 22R_8
DIS4
DIS5
PQ1 ME2N7002E_300mA
PQ34 ME2N7002E_300mA
(42) DIS_+1.0V_VCCST_VCCPLL
(42) DIS_+VCCPLL_OC
+VIN
+3.3V_SUS
+5V_SUS
+1.0V_SUS
+1.8V_SUS
+12VCPU
PR316 1M/F_4
PR319 22R_8
PR321 22R_8
PR318 22R_8
PR320 22R_8
PR313 1M/F_6
EC_SUS_ON_R
DIS14
DIS13
DIS12
DIS11
SUS_ON (42)
(28,41) EC_SUS_ON
PR317 1M/F_4
PQ62 DTC144EUA
PQ67 ME2N7002E_300mA
PQ69 ME2N7002E_300mA
PQ66 ME2N7002E_300mA
PQ68 ME2N7002E_300mA
PQ63 ME2N7002E_300mA
PC245 *0.01u/25V/X7R_4
Quanta confidional
HP Restricted Secret
Quanta Computer Inc.
Project: HP-CRANE
Title
Discharge
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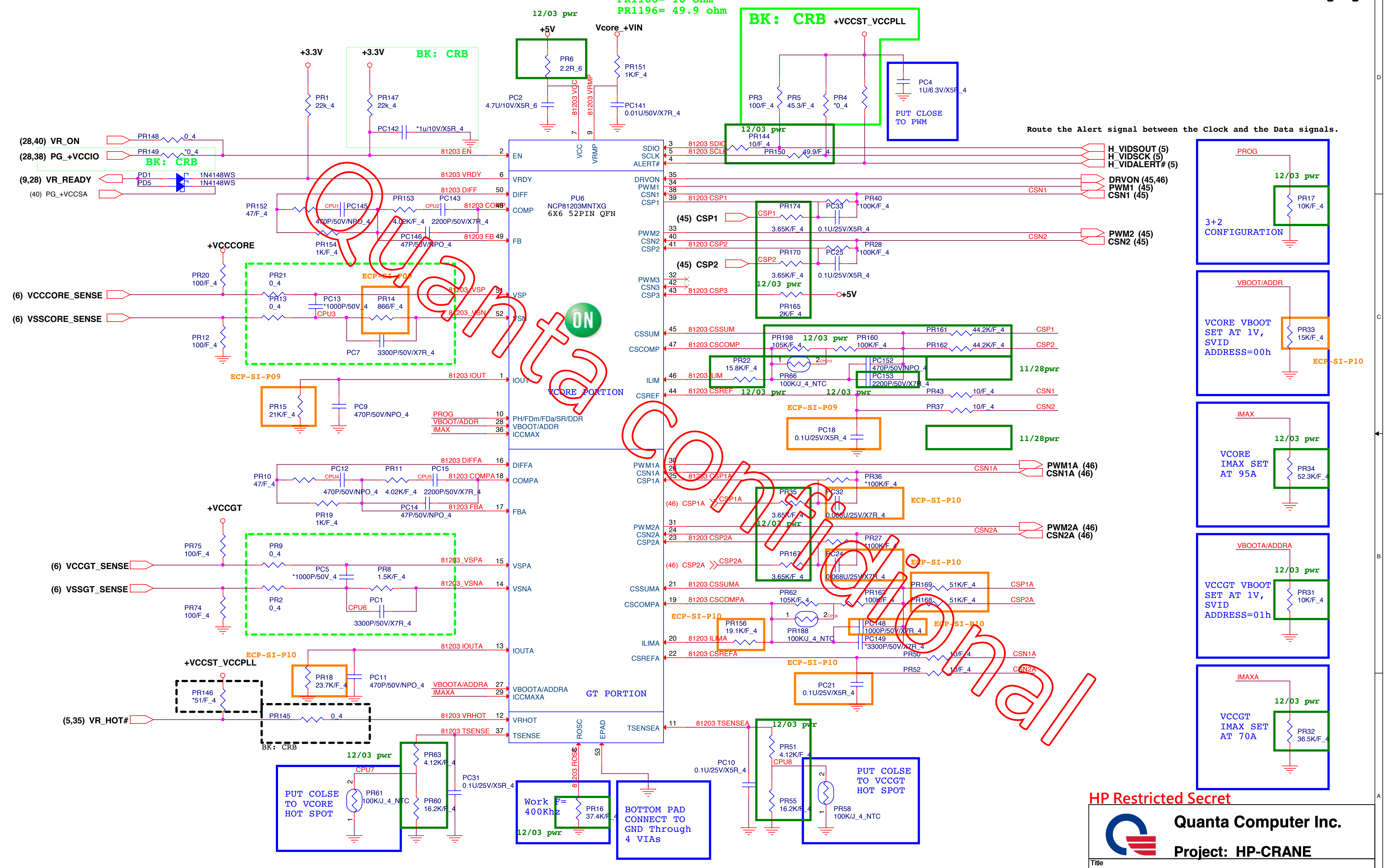
Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



HP Restricted Secret

Quanta Computer Inc.

Project: HP-CRANE

Title	VCC_CORE & VCC_GT	
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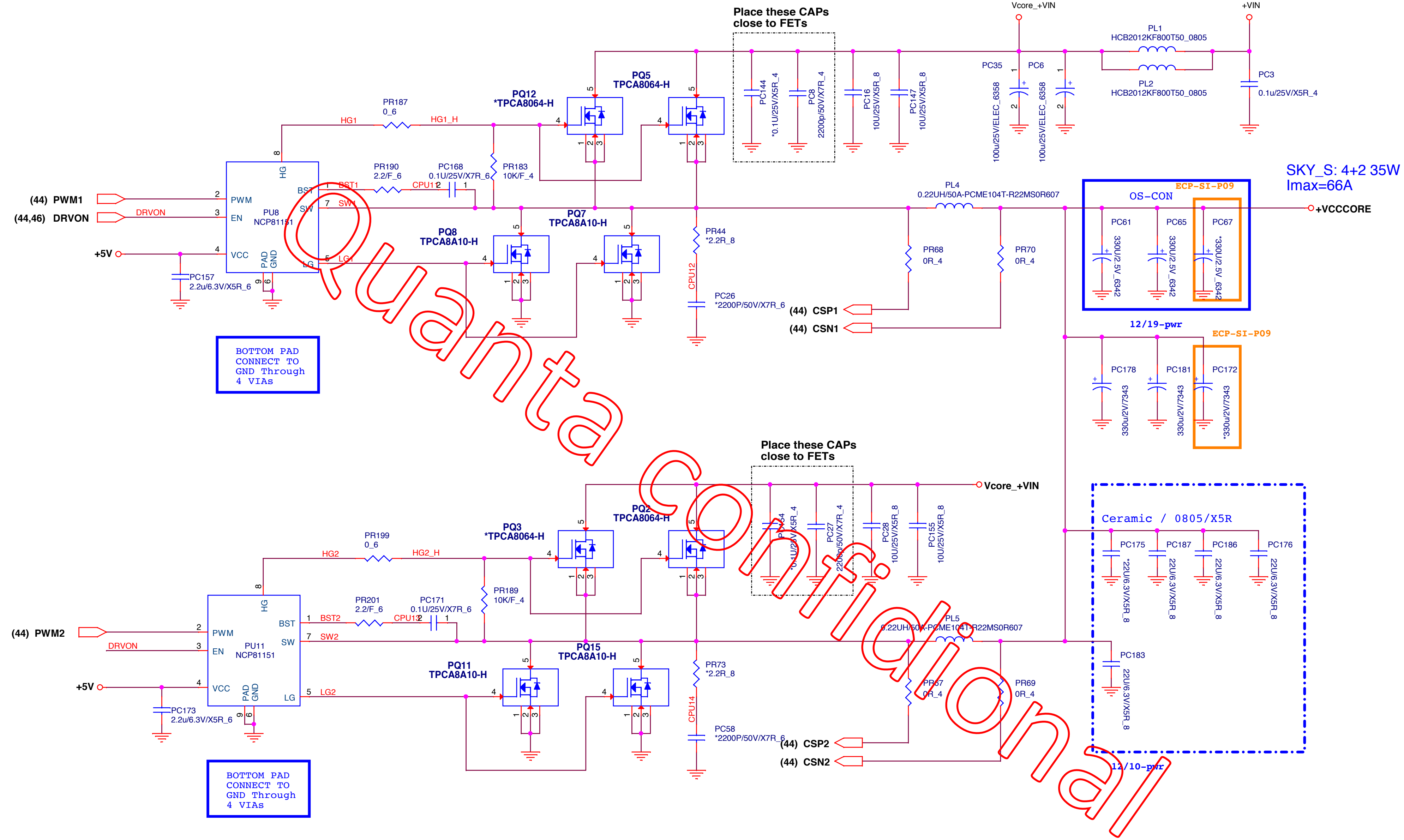
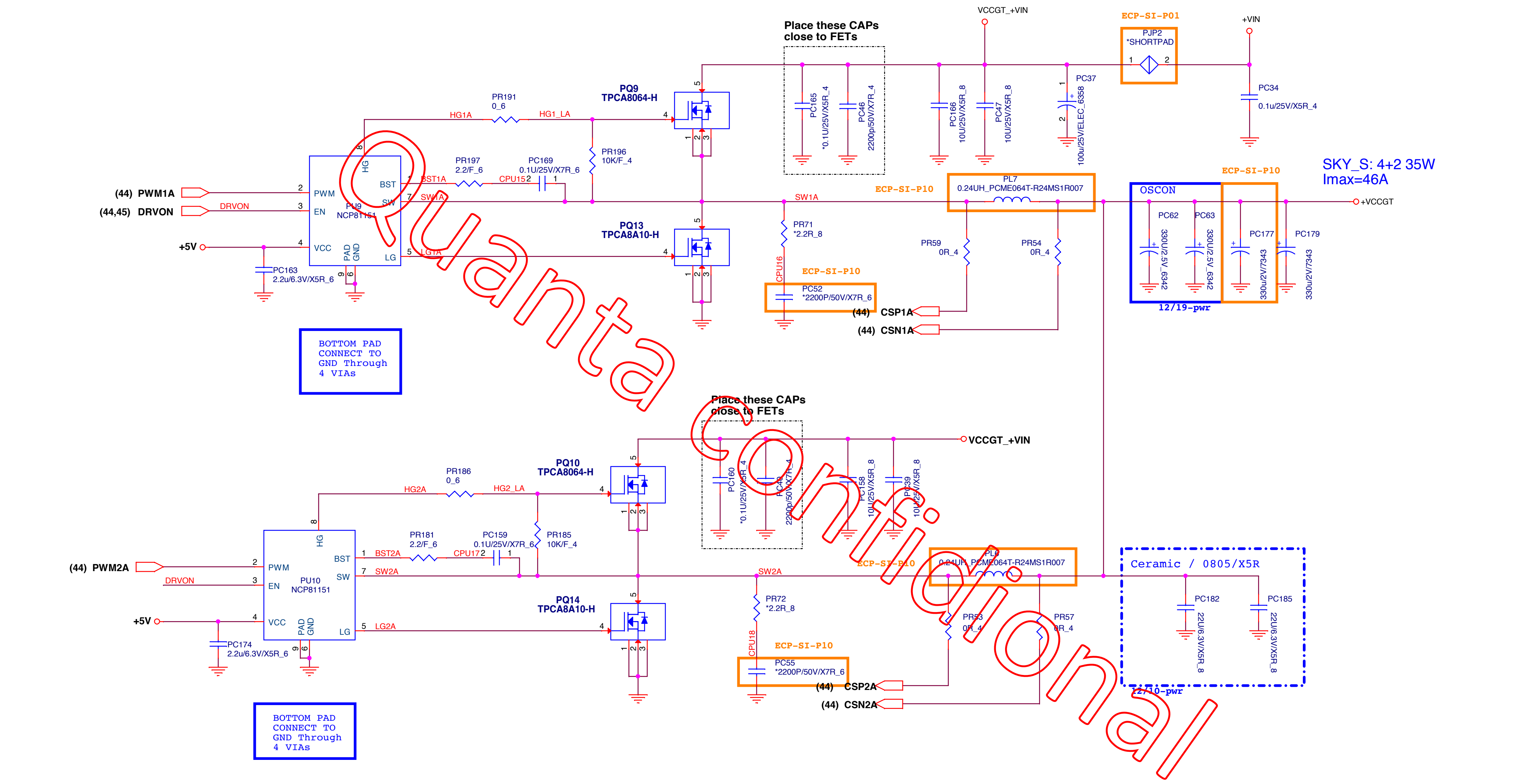

Place these CAPs close to FETs
Vcore_+VIN
+VIN
PL1 HCB2012KF800T50_0805
PL2 HCB2012KF800T50_0805
PC3 0.1u/25V/X5R_4
PC35 100u/25V/ELEC_6358
PC6 100u/25V/ELEC_6358
PC144 *0.1U/25V/X5R_4
PC8 2200p/50V/X7R_4
PC16 10U/25V/X5R_8
PC147 10U/25V/X5R_8
PQ5 TPCA8064-H
PQ12 *TPCA8064-H
PR187 0_6
HG1
HG1_H
PR190 2.2/F_6
PC168 0.1U/25V/X7R_6
PR183 10K/F_4
BST1
CPU12
SW1
LG1
PU8 NCP81151
(44) PWM1
(44,46) DRVON
+5V
PC157 2.2u/6.3V/X5R_6
PQ8 TPCA8A10-H
PQ7 TPCA8A10-H
PL4 0.22UH/50A-PCME104T-R22MS0R607
PR44 *2.2R_8
PC26 *2200P/50V/X7R_6
PR68 0R_4
PR70 0R_4
(44) CSP1
(44) CSN1
+VCCCORE
SKY_S: 4+2 35W
Imax=66A
OS-CON
ECP-SI-P09
PC61 330U/2.5V_6342
PC65 330U/2.5V_6342
PC67 *330U/2.5V_6342
12/19-pwr
PC178 330u/2V/7343
PC181 330u/2V/7343
PC172 *330u/2V/7343
BOTTOM PAD CONNECT TO GND Through 4 VIAs
Vcore_+VIN
PQ2 TPCA8064-H
PQ3 *TPCA8064-H
PC54 *0.1U/25V/X5R_4
PC27 2200p/50V/X7R_4
PC28 10U/25V/X5R_8
PC155 10U/25V/X5R_8
PR199 0_6
HG2
HG2_H
PR189 10K/F_4
PR201 2.2/F_6
PC171 0.1U/25V/X7R_6
BST2
CPU13
SW2
LG2
PU11 NCP81151
(44) PWM2
DRVON
+5V
PC173 2.2u/6.3V/X5R_6
PQ11 TPCA8A10-H
PQ15 TPCA8A10-H
PL5 0.22UH/50A-PCME104T-R22MS0R607
PR73 *2.2R_8
CPU14
PC58 *2200P/50V/X7R_6
PR67 0R_4
PR69 0R_4
(44) CSP2
(44) CSN2
Ceramic / 0805/X5R
PC175 *22U/6.3V/X5R_8
PC187 22U/6.3V/X5R_8
PC186 22U/6.3V/X5R_8
PC176 22U/6.3V/X5R_8
PC183 22U/6.3V/X5R_8
12/10-pwr
BOTTOM PAD CONNECT TO GND Through 4 VIAs



Quanta Computer Inc.

Project: HP-CRANE

Title: VCCGT OUTPUT STAGE

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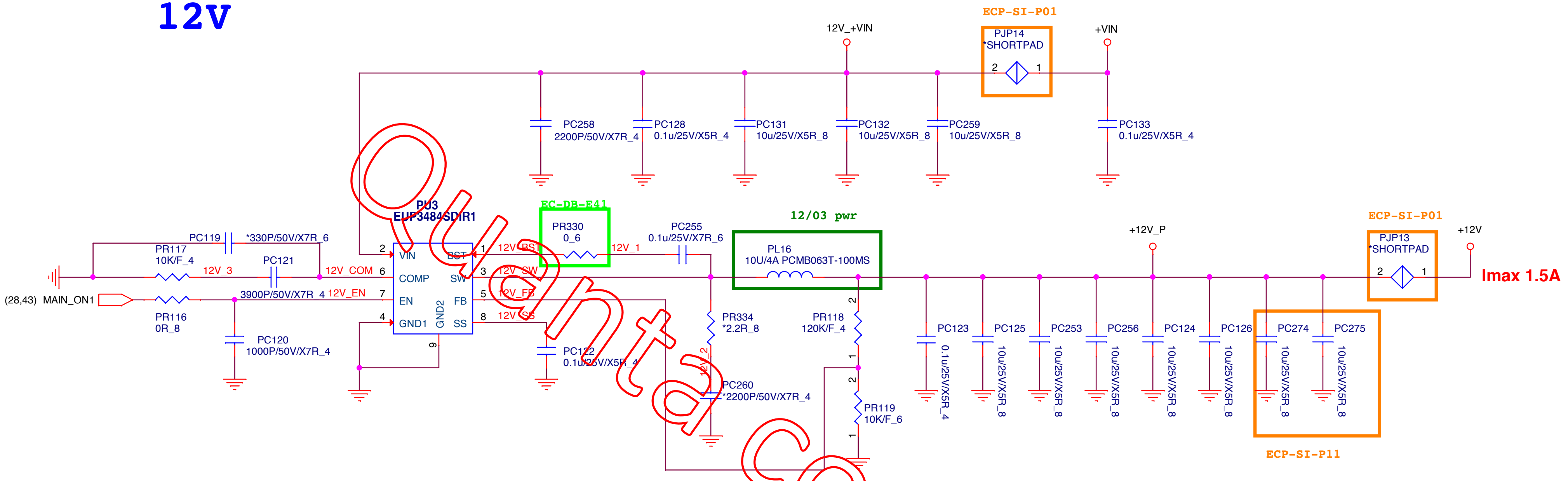
12V



Vout=0.923*((R1+R2)/R2)

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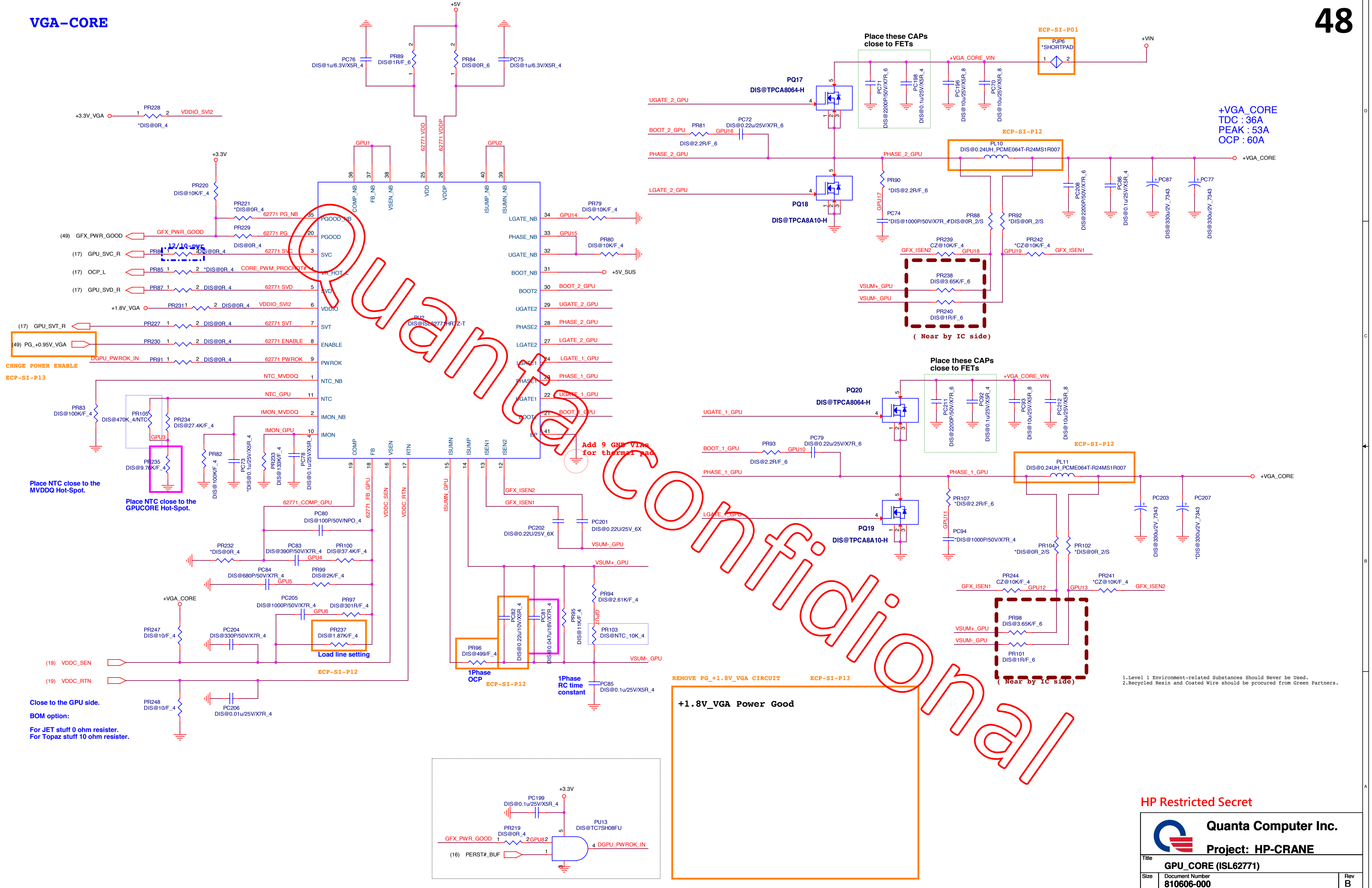
VGA-CORE



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

Project: HP-CRANE

Title	GPU_CORE (ISL62771)
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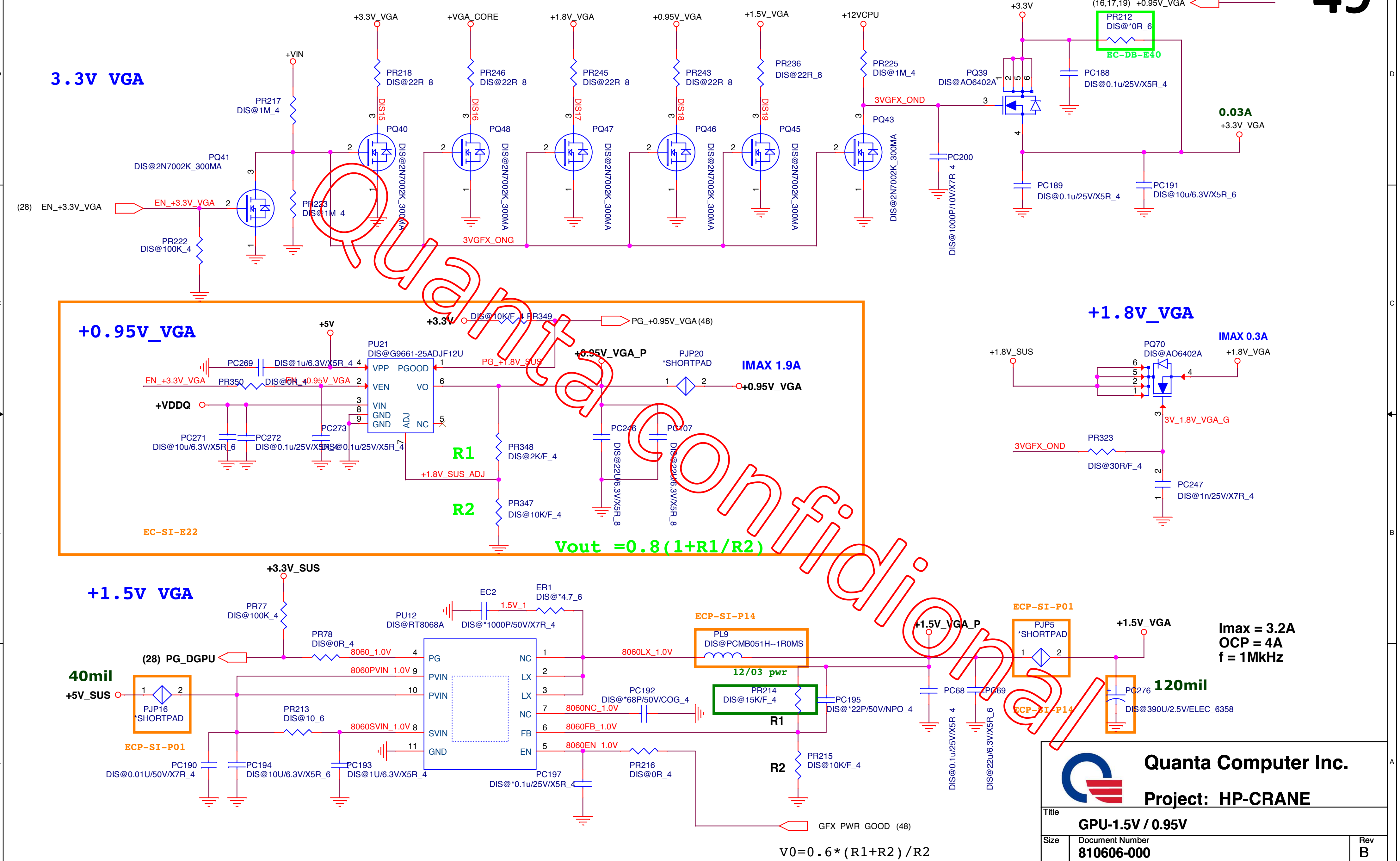
VGA POWER



Quanta Computer Inc.

Project: HP-CRANE

Title	GPU-1.5V / 0.95V	
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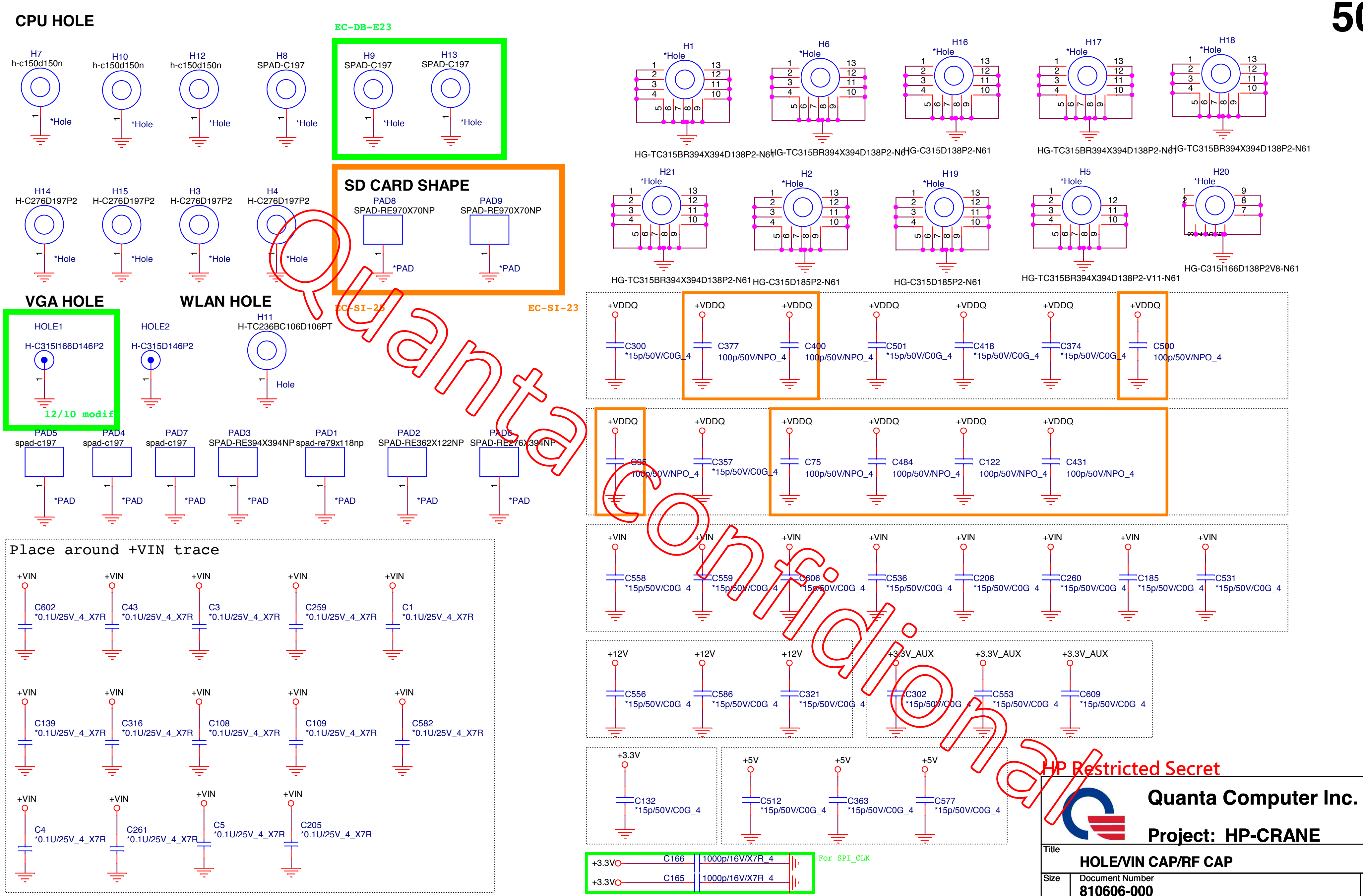

Quanta Computer Inc.

Project: HP-CRANE

Title: HOLE/VIN CAP/RF CAP

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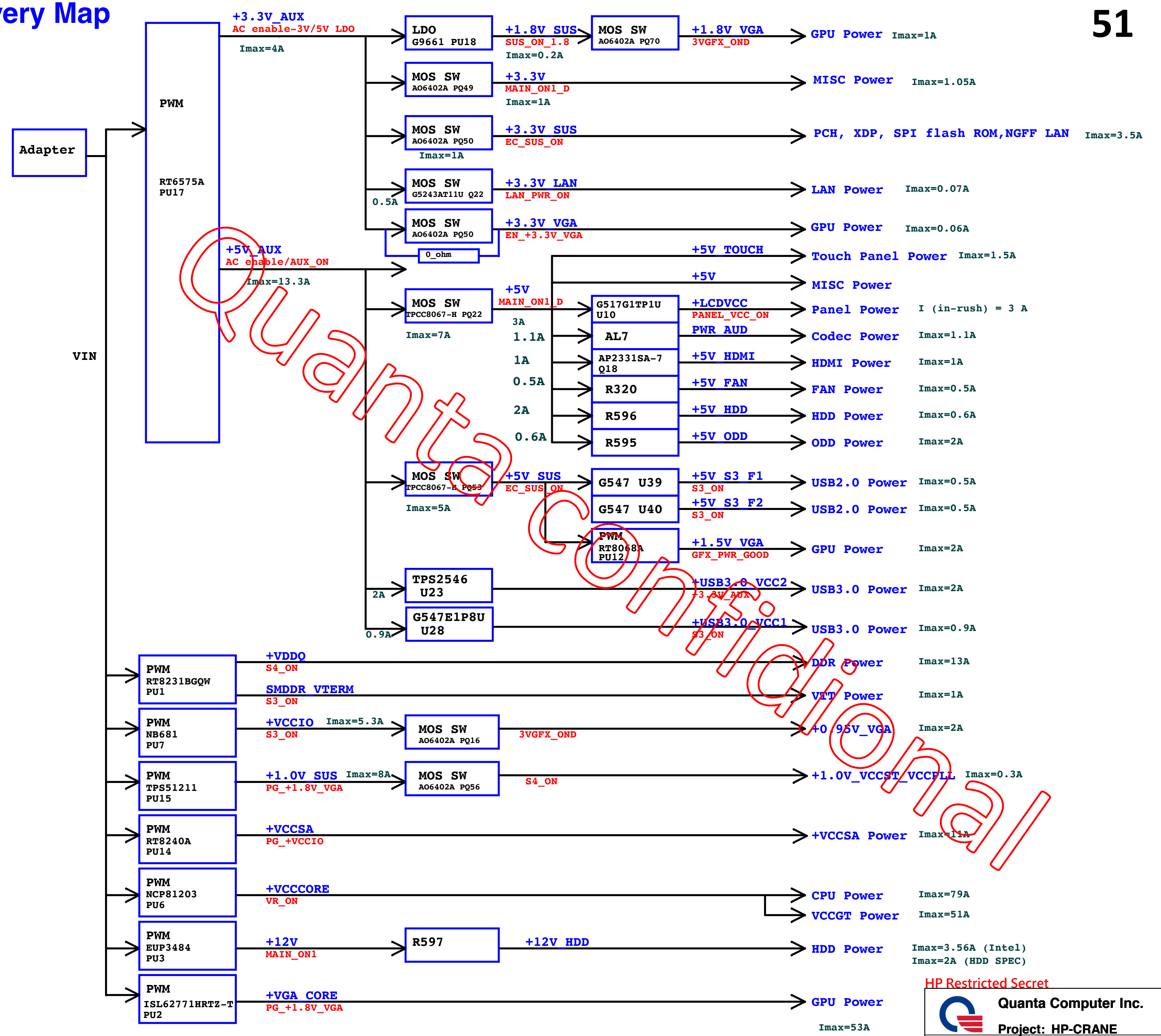
Power Delivery Map



Quanta Computer Inc.		
Project: HP-CRANE		
Title: Power Delivery Map		
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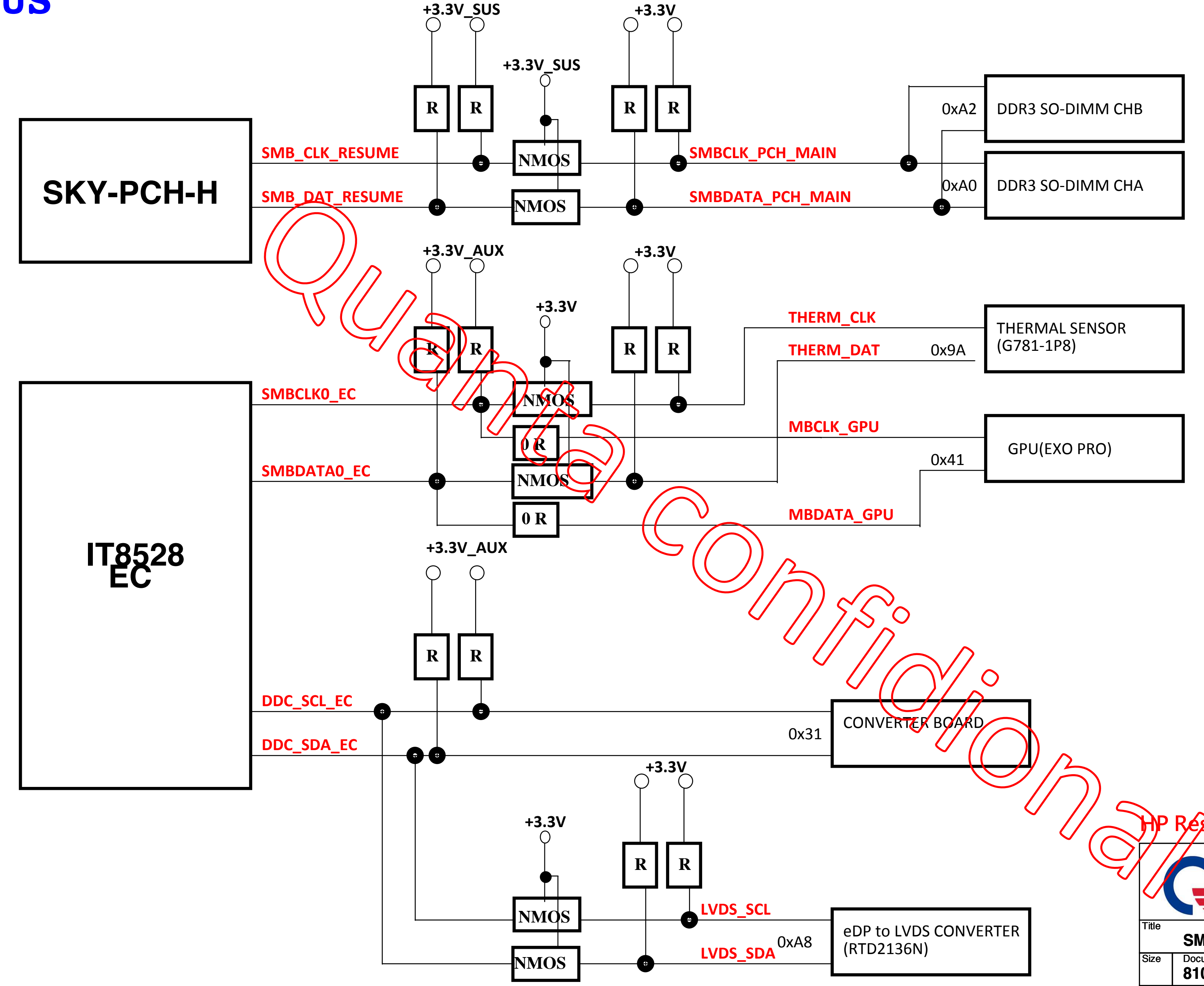
SMBUS



Quanta Computer Inc.

Project: HP-CRANE

Title	SMBus	
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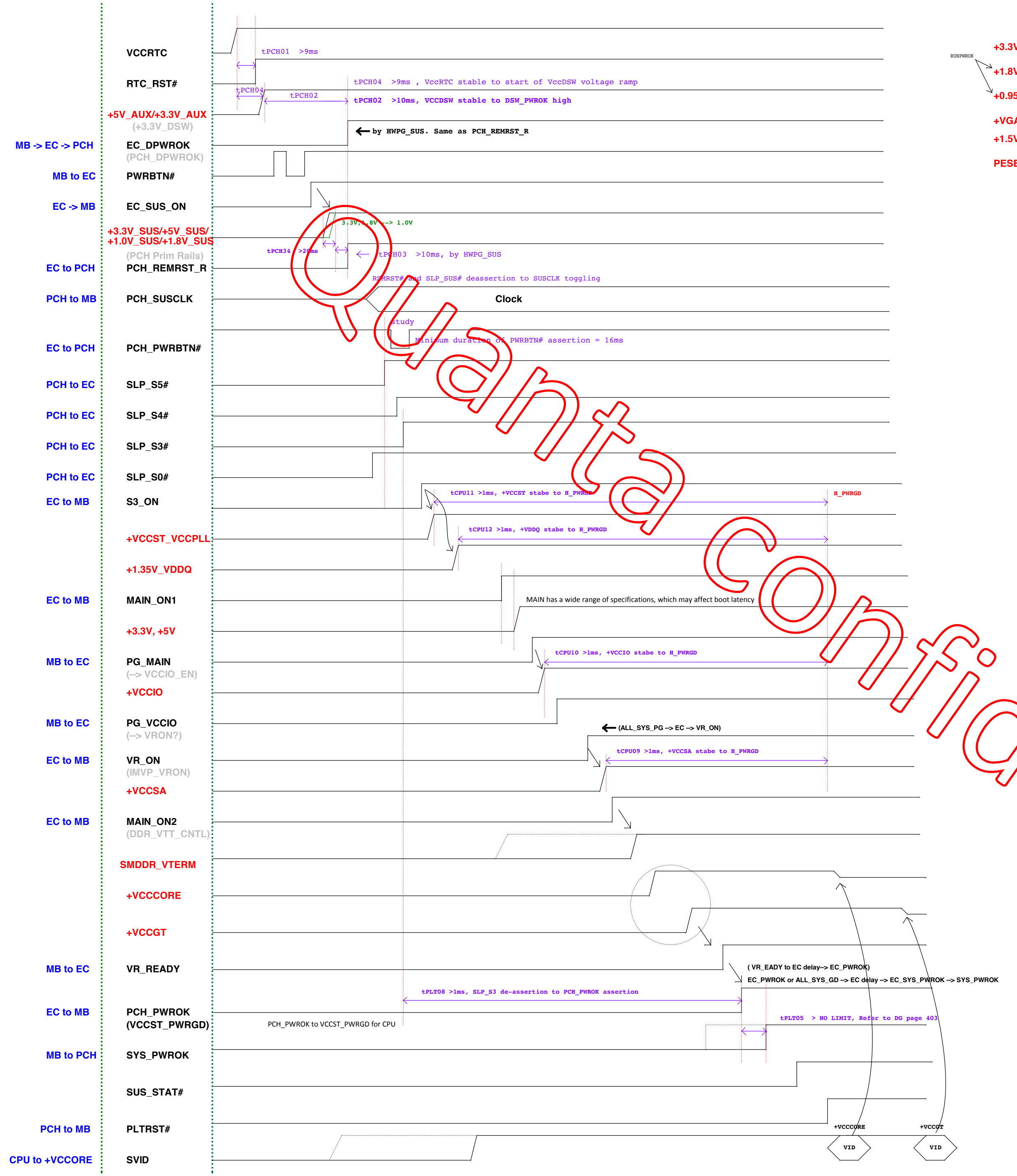
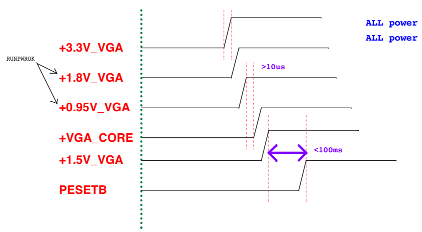
SKY-S POWER SEQUENCE



AMD dGPU POWER SEQUENCE



ALL power rail Tramp-up : > 20ms
ALL power rail Tramp-down : > 20ms

Quanta Computer Inc.		
Project: HP-CRANE		
Title: Power Sequence		
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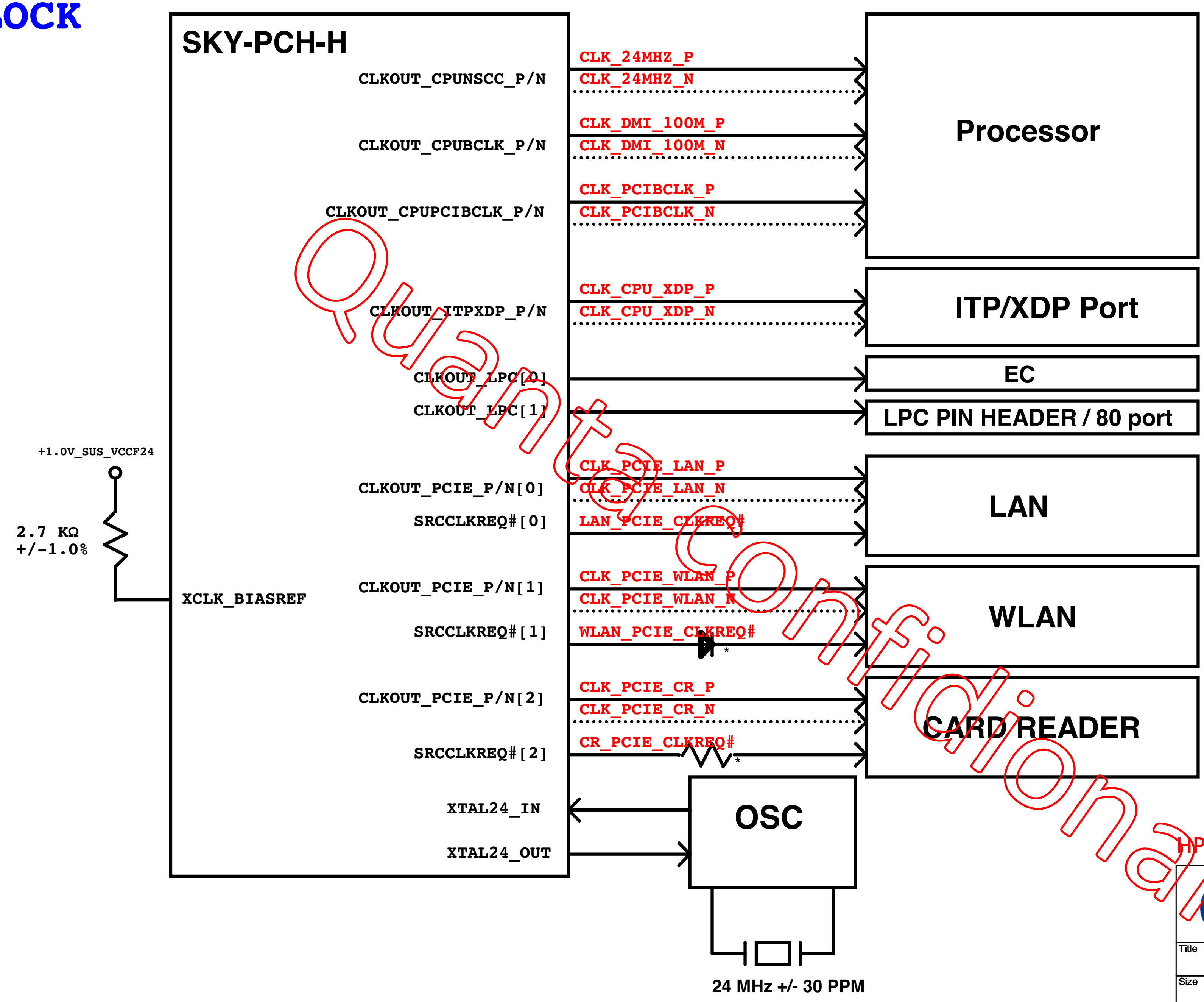
CLOCK



Quanta Computer Inc.

Project: HP-CRANE

Title: CLOCK MAP

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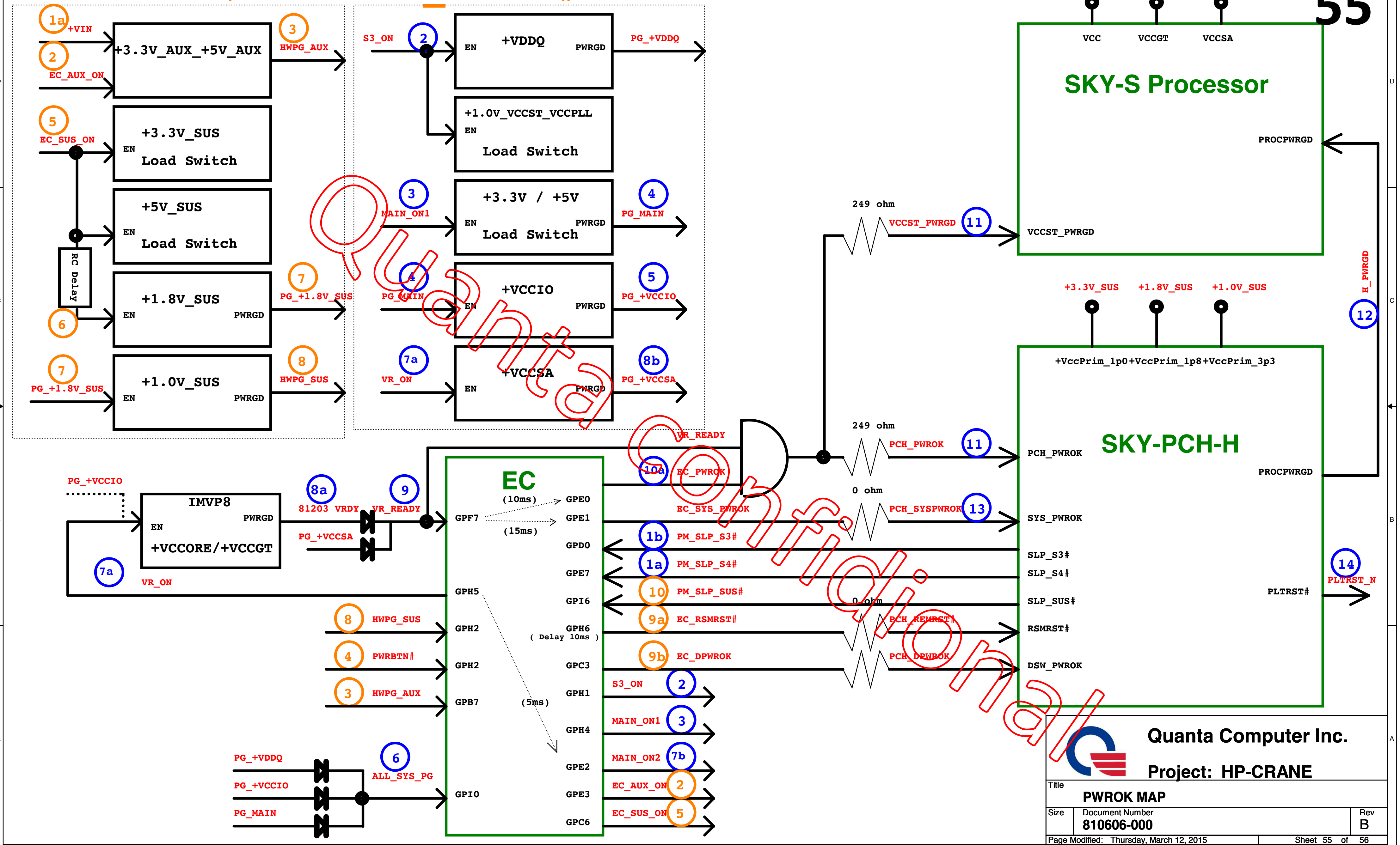
PWROK MAP / RSMRST_PWRGD#



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Project: HP-CRANE

Title: PWROK MAP

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DB to SI Change List


```
EC-SI-E01 Un-stuff  CPU HW straps, R444,R61,R462 -- Page 5
EC-SI-E02 Un-stuff H_PWRGD  pull down, R493 -- Page 5
EC-SI-E03 Un-stuff SPI_IO2 pull downy, R589 -- Page 9
EC-SI-E04 Change Q13 gate power rail,   -- Page 9
EC-SI-E05 Remove Q12 and add R698/R697 -- Page 9
EC-SI-E06 Remove C583 to fix DRAMRST rise time -- Page 9
EC-SI-E07 For XDP only, R596,R587 -- Page 10
EC-SI-E08 Don't populate R532 for +3.3V Leakage --  Page 11
EC-SI-E09 CRB: U33.AB10 connect to GND-- Page 13
EC-SI-E10 Vendor suggest to change for 27MHz frequency accuracy, C525/C526  -- Page 17
EC-SI-E11 Change HDMI connector follow Crusher  -- Page 23
EC-SI-E12 Change LVDS interface EMI solution L13~L22  -- Page 24
EC-SI-E13 Add C632 1000pf on +LCDVCC_C for EMI  -- Page 24
EC-SI-E14 Don't populate AR3 for +3.3V Leakage  -- Page 25
EC-SI-E15 Change AR1 to 4.7 ohm for EA-- Page 25
EC-SI-E16 Change from +3.3V to +3.3V_AUX for EC_SMI#_R for +3.3V_SUS Leakage -- Page 25
EC-SI-E17 Don't stuff R402/R403 for +3.3V_SUS leakage     -- Page 28
EC-SI-E18 Change U29.72 to IOUT     -- Page 28
EC-SI-E19 Add EC6 220pf on +5V_SUS, EC5 220pf on PWRBTN#, EC4 220pf on PWR_ON_LED# -- Page 32
EC-SI-E20 Add serial resistor R699 on L_FRAME#  -- Page 28
EC-SI-E21 rChange serial resistor from 33ohm to 100ohm on F_LAD0_R,F_LAD1_R,F_LAD2_R,F_LAD3_RmL_FRAME#_R,L_FRAME#_R,F_LAD0_D,F_LAD1_D,F_LAD2_D,F_LAD3_D,R405,R406,R408,R456,R455,R454,R453 -- Page 28
EC-SI-E22 Add+0.95V_VGA power LDO circuit   -- Page 49
EC-SI-E23 Stuff some capacitors EMI reserved before.   -- Page 50
EC-SI-E24 Change AD4,AD5,AD6,AD7 part and their pin2 connect to GND   -- Page 25
EC-SI-E25 Change DDR3L socket, JDIM1,JDIM2-- Page 14,15
EC-SI-E26 Add ESD protector for 3D CAMERA, U41-- Page 29
EC-SI-E27 Add ESD capactior for Audio codec return path   AC38,AC30,AC45 -- Page 25
EC-SI-E28  C203, C204, C592 and C593 change with 1000pf cap for ESD -- Page 26
EC-SI-E29 AL1-AL4 change to 220 ohm bead same as previous mode for EMI, AL1~AL4   -- Page 25
EC-SI-E30 Add ESD protector for DMIC (close to CN6)  -- Page 25

ECP-SI-P01 change footprint to short pad, PJP1~PJP19 -- Page35~49
ECP-SI-P02 change current sense IC multiple and EC detect system power consumption,PU20,PR133,PR351,PR132 -- Page 35
ECP-SI-P03 add power rating,PQ26,PC101 -- Page 36
ECP-SI-P04 adjust output voltage and common design. PR30/PC48/PC49 -- Page 36
ECP-SI-P05 adjust sequence and remote sense resistor.PC156/PR192/PR193  -- Page 38
ECP-SI-P06 common design. PC102 -- Page 39
ECP-SI-P07 common design. PC104/PC106-- Page 40
ECP-SI-P08 adjust sequence. PR327/PR328-- Page
ECP-SI-P09 Iout and load line setting. PR14/PR15/PC18/PC67/PC172-- Page 44
ECP-SI-P10 OCP, Iout, load line setting and common design. PR33/PR18/PR156/PR168/PR169/PC24/PC32/PC148/PC21/PL6/PL7/PC52/PC55-- Page 44
ECP-SI-P11 improve ripple. PC274/PC275-- Page 47
ECP-SI-P12 OCP, load line setting and common design. PR96/PR237/PC82/PL10/PL11-- Page 48
ECP-SI-P13 Remove PG_+1.8V_VGA circuit. PQ42/PQ44/PR224/PR226 -- Page48
ECP-SI-P14 add power rating. PL9/PC276 -- Page 49
ECP-SI-P15 change power solution from load switch to LDO. PQ16/PR76/PC66/PC107/PC246/PU21/PR347/PR349/PR348/PR350/PR269/PC271/PC272/PC273 -- Page49
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