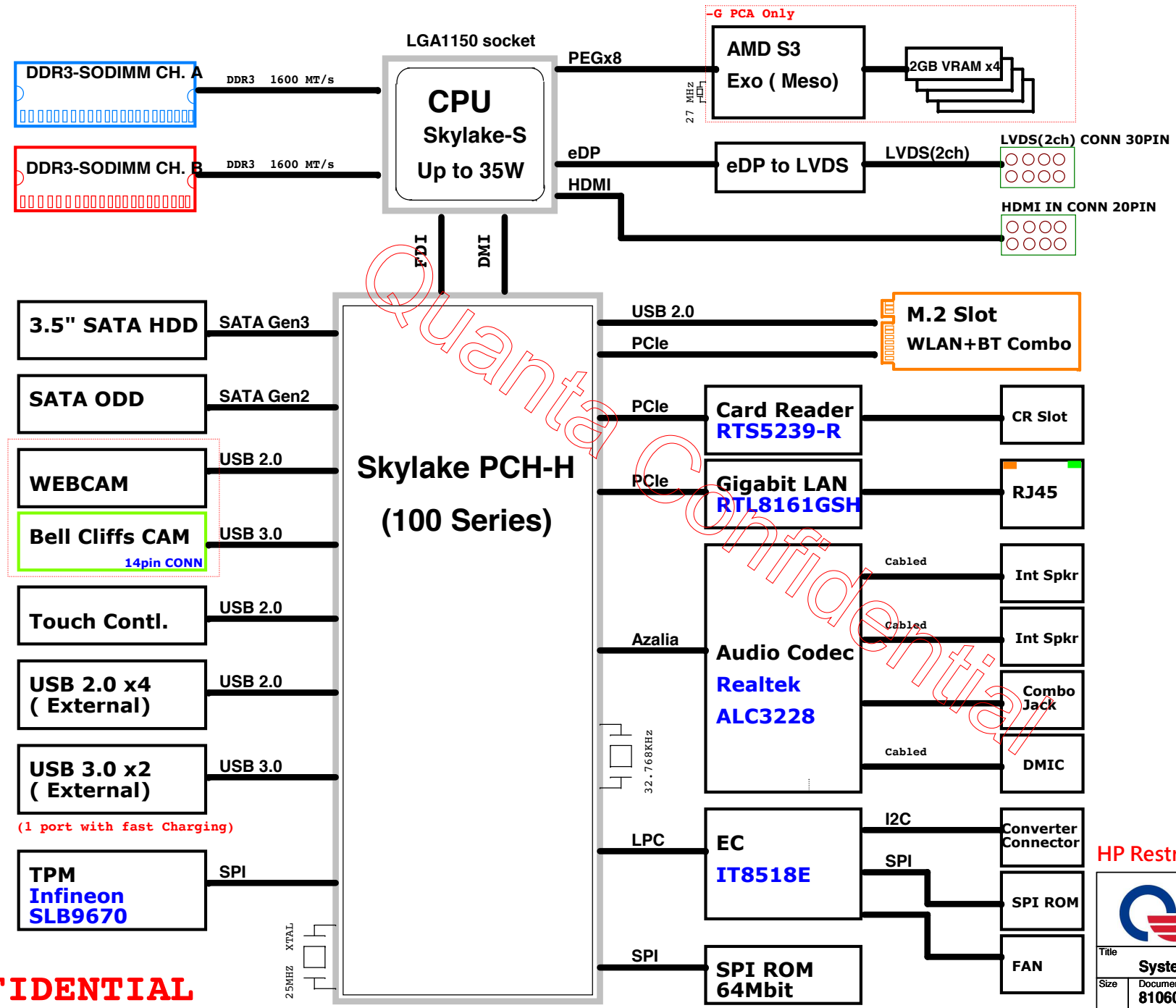
HP Crane System Block Diagram

01



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Project: HP-CRANE

Title		
System Block Diagram		
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CONFIDENTIAL

Voltage Rails

Power Rail	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal	
+RTC_VCC	3V	ON	ON	ON	ON	ON	ON		RTC Batt, PCH , EC
+VIN	19V	ON	ON	ON	ON	ON	OFF	Adaptor in	
+5V_AUX	5V	ON	ON	ON	ON	ON	OFF	AUX_ON	USB Charger
+3.3V_AUX	3.3V	ON	ON	ON	ON	ON	OFF	3V/5V PWM IC_LDO	EC, Flash
+5V_SUS	5V	ON	ON	ON	ON	OFF	OFF	EC_SUS_ON	PCH, USB, 3D WebCAM, Touch Panel
+3.3V_SUS	3.3V	ON	ON	ON	ON	OFF	OFF	EC_SUS_ON	PCH, XDP, SPI flash ROM,NGFF LAN
+1.8V_SUS	1.8V	ON	ON	ON	ON	OFF	OFF	EC_SUS_ON	PCH, XDP, NGFF LAN
+1.0V_SUS	1.0V	ON	ON	ON	ON	OFF	OFF	PG_+1.8V_SUS	PCH
+VCCST_VCCPLL	1.0V	ON	ON	OFF	OFF	OFF	OFF	S3_ON	CPU, PCH, XDP
+VDDQ	1.35V	ON	ON	OFF	OFF	OFF	OFF	S3_ON	DDR3, CPU DDR3 I/O
SMDDR_VTERM	0.75V	ON	ON	OFF	OFF	OFF	OFF	DDR_VTT_CNTL	DDR3
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	HDD, ODD,Audio AMP,Panel VCC,FAN
+3.3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	PCH, Audio, Card Reader, TPM, FHD CAM
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	3.5" HDD
+VCCIO	0.95V	ON	OFF	OFF	OFF	OFF	OFF	PG_MAIN	CPU
+VCCSA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+VCCIO	PCH, CPU
+VCCGT	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON	PCH
+3.3V_VGA	3.3V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dGPU
+1.8V_VGA	1.8V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dGPU
+0.95V_VGA	0.95V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dCPU
+VGA_CORE	0.8~1.15V	ON	OFF	OFF	OFF	OFF	OFF	PG_+1.8V_VGA	dGPU
+1.5V_VGA	1.5V	ON	OFF	OFF	OFF	OFF	OFF	GFX_PWR_GOOD	dGPU, VRAM
+VCCCORE	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON	CPU

Schematic "Value" Definition

Intel Platform Crusher-G and Crusher-U			DB/SI/PV Stage			MP		
By Value format	Description	Auto BOM Control	UMA	Discrete Meso GPU	Discrete Exo GPU	UMA	Discrete Meso GPU	Discrete Exo GPU
XX	Install	V	V	V	V	V	V	V
*XX	Non-Install	V						
PROTO@XX	Install in Pre-production only	V	V	V	V			
MP@XX	Install in MP only	V				V	V	V
DIS@xx	Install Discrete (DGPU) only	V		V	V		V	V
UMA@xx	Install UMA	V	V			V		
M_DIS@xx	Install Discrete Meso GPU only	V		V			V	
E_DIS@xx	Install Discrete Exo GPU only	V			V			V

***Board ID and VRAM ID by manual control

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Title: Power States & Value Definition

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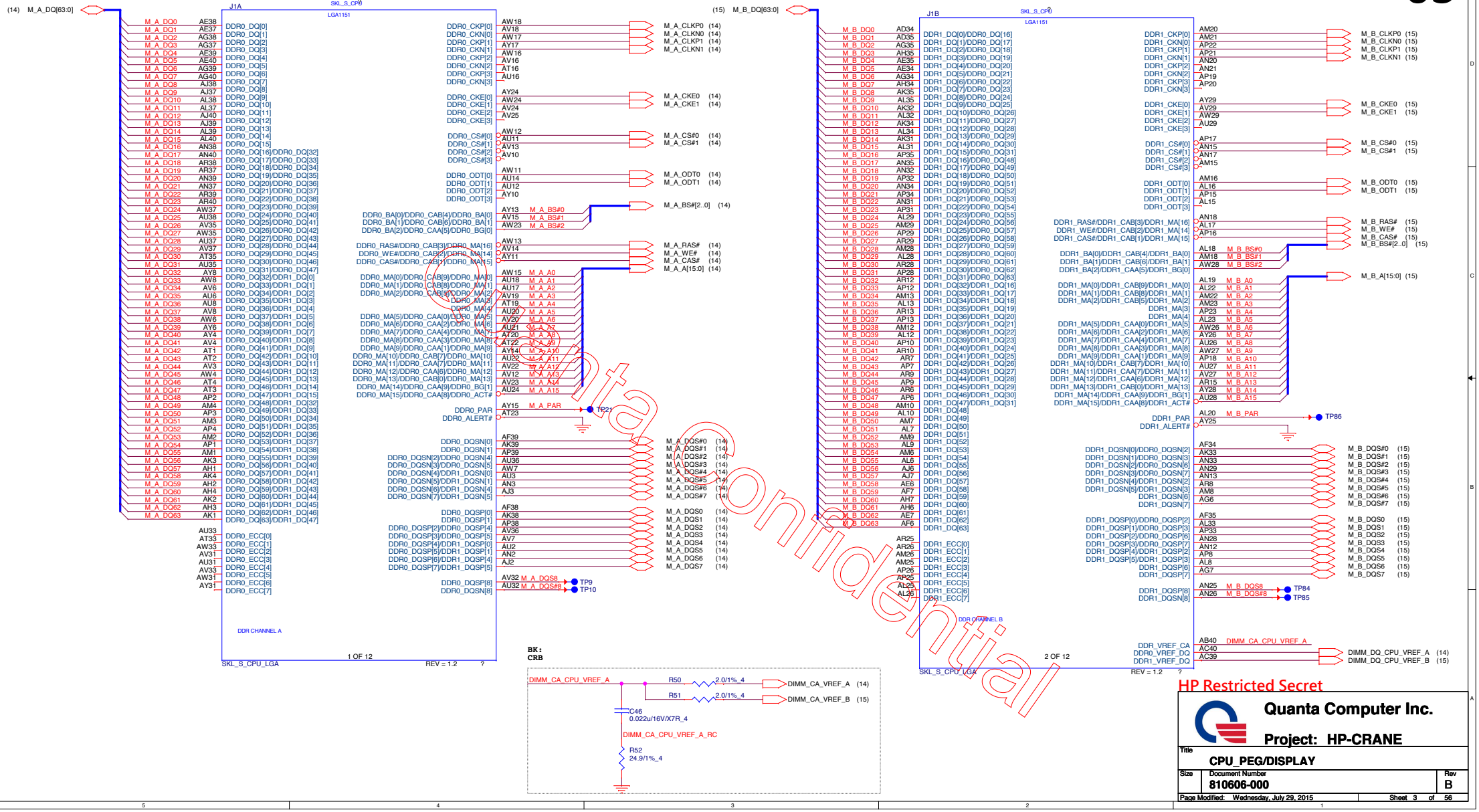

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Project: HP-CRANE

Title: CPU_PEG/DISPLAY

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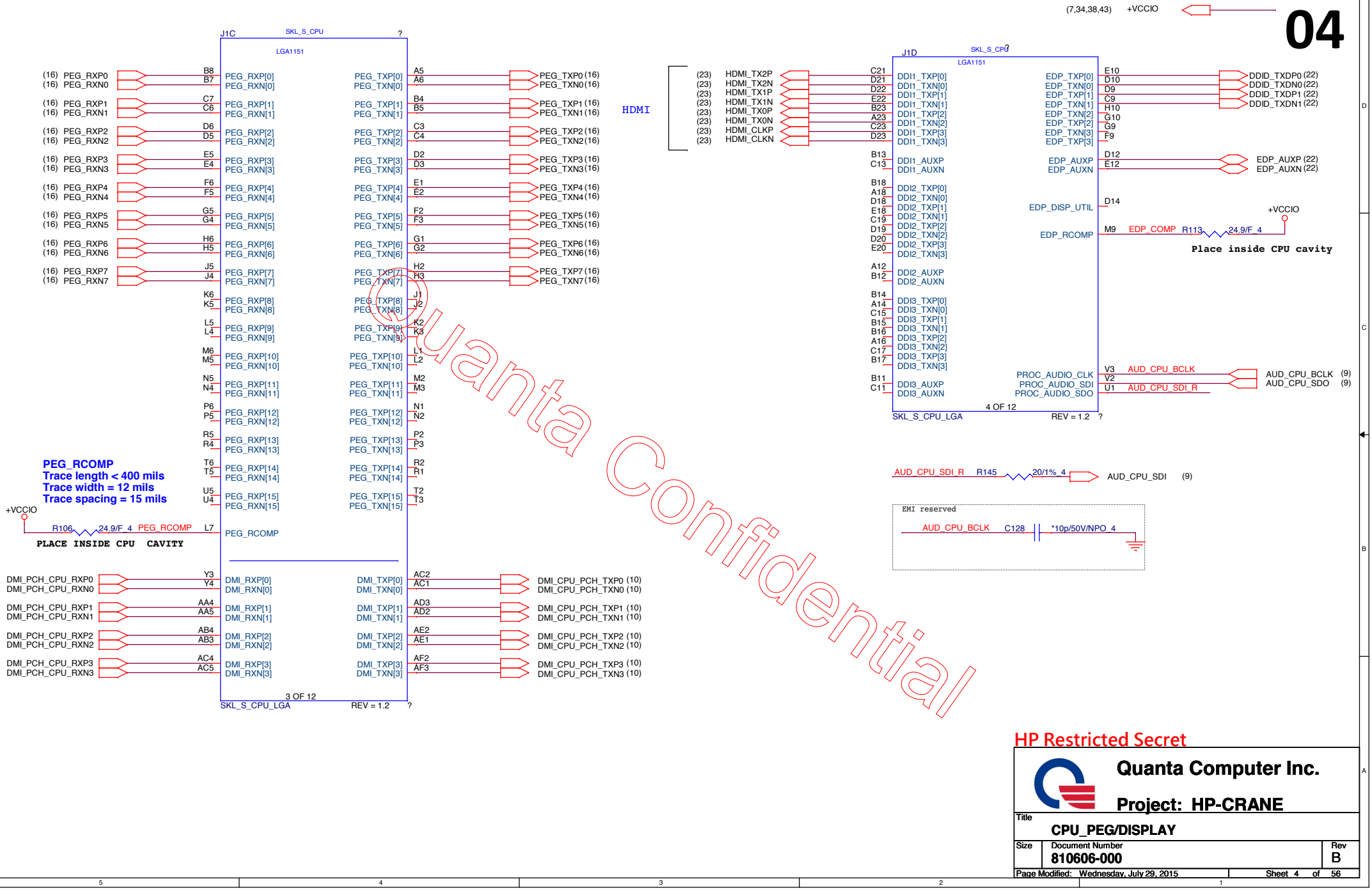

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Project: HP-CRANE

Title		
CPU_PEG/DISPLAY		
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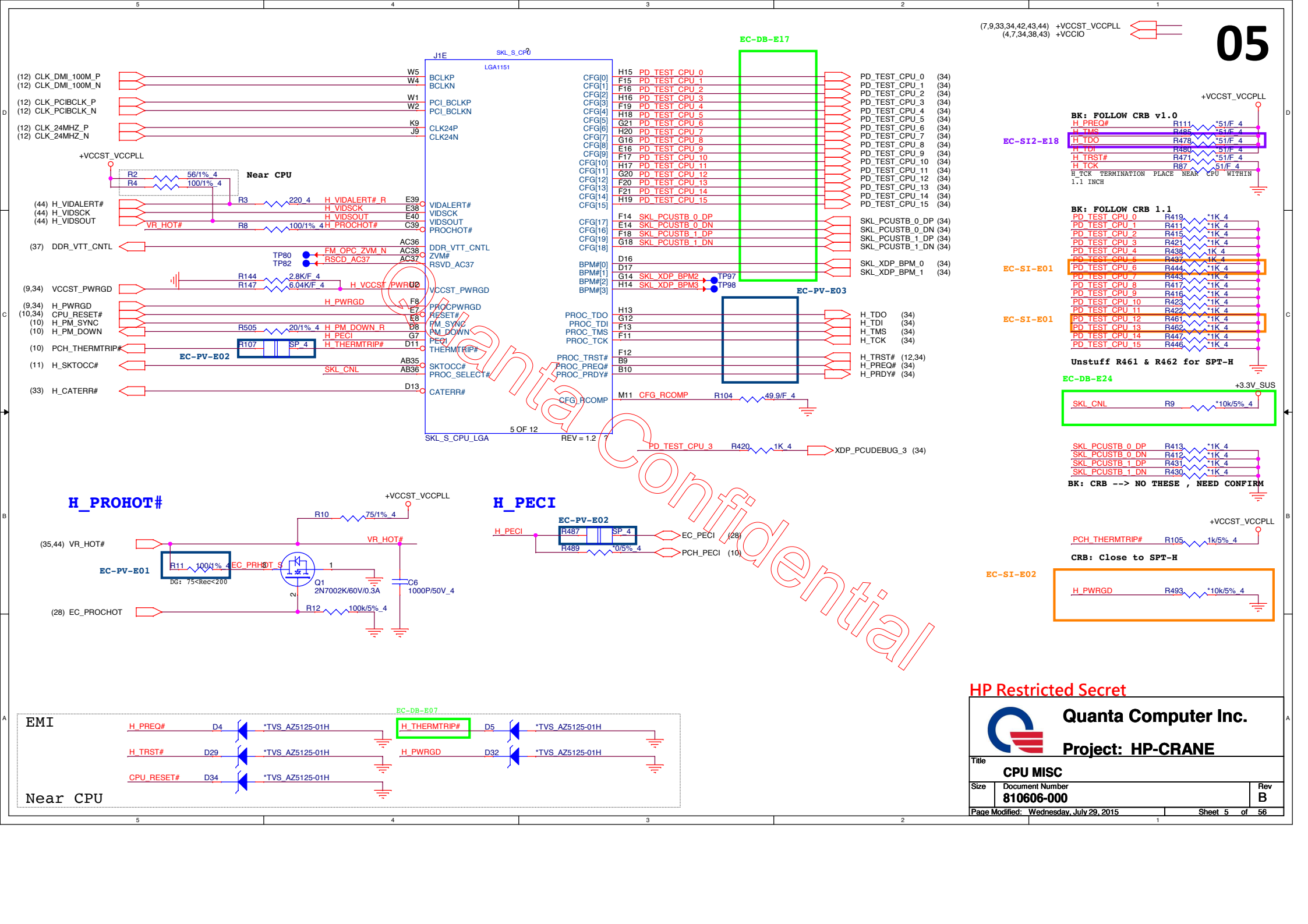
05
J1E
SKL_S_CPU
LGA1151
5 OF 12
SKL_S_CPU_LGA
REV = 1.2
Near CPU
EC-DB-E17
EC-PV-E03
EC-PV-E02
EC-SI2-E18
EC-SI-E01
EC-SI-E01
EC-DB-E24
EC-SI-E02
BK: FOLLOW CRB v1.0
BK: FOLLOW CRB 1.1
Unstuff R461 & R462 for SPT-H
BK: CRB --> NO THESE , NEED CONFIRM
CRB: Close to SPT-H
H_PROHOT#
H_PECI
EMI
Near CPU
EC-DB-E07
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+VCCCPRE:
Icc (max) : 66A
Icc (PS2) : 35A

Decoupling Capacitors

+VCCCORE

C422 470U/2.5V_7343
C421 470U/2.5V_7343

Place caps at top socket edge

+VCCCORE

C68	22U 6.3V X5R	0603
C334	22U 6.3V X5R	0603
C71	22U 6.3V X5R	0603
C343	22U 6.3V X5R	0603
C72	22U 6.3V X5R	0603
C387	22U 6.3V X5R	0603
C67	22U 6.3V X5R	0603
C398	22U 6.3V X5R	0603
C76	22U 6.3V X5R	0603
C65	22U 6.3V X5R	0603
C83	22U 6.3V X5R	0603
C78	22U 6.3V X5R	0603

Place all above caps on top side of CPU cavity

+VCCCORE

C66	22U 6.3V X5R	0603
C90	22U 6.3V X5R	0603
C77	22U 6.3V X5R	0603
C85	22U 6.3V X5R	0603
C79	22U 6.3V X5R	0603
C373	22U 6.3V X5R	0603
C69	22U 6.3V X5R	0603
C360	22U 6.3V X5R	0603
C80	22U 6.3V X5R	0603
C409	22U 6.3V X5R	0603

Place all below caps on bottom side near CPU socket

+VCCCORE

J1G SKL_S_CPU LGA1151

A25	VCC	VCC	H32
A26	VCC	VCC	J21
A27	VCC	VCC	F32
A28	VCC	VCC	F33
A29	VCC	VCC	F34
A30	VCC	VCC	G23
B25	VCC	VCC	G24
B27	VCC	VCC	G25
B29	VCC	VCC	G26
B31	VCC	VCC	G27
B32	VCC	VCC	G28
B33	VCC	VCC	G29
B34	VCC	VCC	J22
B35	VCC	VCC	J23
B36	VCC	VCC	J24
B37	VCC	VCC	J25
C25	VCC	VCC	J26
C26	VCC	VCC	J27
C27	VCC	VCC	J28
C28	VCC	VCC	J29
C29	VCC	VCC	J30
C30	VCC	VCC	J31
C32	VCC	VCC	K16
C34	VCC	VCC	K18
C36	VCC	VCC	K20
D25	VCC	VCC	K21
D27	VCC	VCC	K23
D29	VCC	VCC	K25
D31	VCC	VCC	K27
D32	VCC	VCC	K29
D33	VCC	VCC	K31
D34	VCC	VCC	L14
D35	VCC	VCC	L15
D36	VCC	VCC	L16
E24	VCC	VCC	L17
E25	VCC	VCC	L18
E26	VCC	VCC	L19
E27	VCC	VCC	L20
E28	VCC	VCC	L21
E29	VCC	VCC	L22
E30	VCC	VCC	L23
E32	VCC	VCC	L24
E34	VCC	VCC	L25
E36	VCC	VCC	L26
F23	VCC	VCC	L27
F24	VCC	VCC	L28
F25	VCC	VCC	L29
F27	VCC	VCC	L30
F29	VCC	VCC	M13
F31	VCC	VCC	M14
G30	VCC	VCC	M16
G32	VCC	VCC	M18
H22	VCC	VCC	M20
H23	VCC	VCC	M22
H25	VCC	VCC	M24
H27	VCC	VCC	M26
H29	VCC	VCC	M28
H31	VCC	VCC	M30
AJ11	VCC	VCC	AJ12
AJ13	VCC	VCC	AJ14
AJ15	VCC	VCC	AJ16
AJ17	VCC	VCC	AJ18
AJ19	VCC	VCC	AJ20
AJ21	VCC	VCC	AJ22

7 OF 12
SKL_S_CPU_LGA REV = 1.2 ?

VCC_SENSE C38 → VCCCORE_SENSE (44)
VSS_SENSE D38 → VSSCORE_SENSE (44)

VCCCORE_SENSE R6 *0/5%_4 VSSCORE_SENSE

+VCCCORE

VCCCORE_SENSE R5 100/1%_4
VSSCORE_SENSE R7 100/1%_4

DG: Near CPU

+VCCCPRE:
Icc (max) : 40A
Icc (PS2) : 32A

+VCCGT

J1H SKL_S_CPU LGA1151

AA34	VCCGT	VCCGTX	F35
AA35	VCCGT	VCCGTX	G34
AA36	VCCGT	VCCGTX	G35
AA37	VCCGT	VCCGTX	H33
AA38	VCCGT	VCCGTX	H34
AB33	VCCGT	VCCGTX	J33
AB34	VCCGT	VCCGTX	J35
G36	VCCGT	VCCGTX	K32
G37	VCCGT	VCCGTX	K34
G38	VCCGT	VCCGTX	L31
G39	VCCGT	VCCGTX	L33
G40	VCCGT	VCCGTX	M32
H36	VCCGT		
H38	VCCGT		
H40	VCCGT		
J36	VCCGT		
J37	VCCGT		
J38	VCCGT		
J39	VCCGT		
J40	VCCGT		
K36	VCCGT		
K38	VCCGT		
K40	VCCGT		
L34	VCCGT		
L35	VCCGT		
L36	VCCGT		
L37	VCCGT		
L38	VCCGT		
L39	VCCGT		
L40	VCCGT		
M33	VCCGT		
M34	VCCGT		
M36	VCCGT		
M38	VCCGT		
M40	VCCGT		
N34	VCCGT		
N35	VCCGT		
N36	VCCGT		
N37	VCCGT		
N38	VCCGT		
N39	VCCGT		
N40	VCCGT		
P33	VCCGT		
P34	VCCGT		
P36	VCCGT		
P38	VCCGT		
P40	VCCGT		
R34	VCCGT		
R35	VCCGT		
R36	VCCGT		
R37	VCCGT		
R38	VCCGT		
R39	VCCGT		
R40	VCCGT		
T33	VCCGT		
T34	VCCGT		
T36	VCCGT		
T38	VCCGT		
T40	VCCGT		
U34	VCCGT		
U35	VCCGT		
U36	VCCGT		
U37	VCCGT		
U38	VCCGT		
U39	VCCGT		
U40	VCCGT		
V33	VCCGT		
V34	VCCGT		
V36	VCCGT		
V38	VCCGT		
V40	VCCGT		
W34	VCCGT		
W35	VCCGT		
W36	VCCGT		
W37	VCCGT		
W38	VCCGT		
Y33	VCCGT		
Y34	VCCGT		
Y36	VCCGT		
Y38	VCCGT		

8 OF 12
SKL_S_CPU_LGA REV = 1.2 ?

VCCGT_SENSE F39 → VCCGT_SENSE (44)
VSSGT_SENSE F38 → VSSGT_SENSE (44)
VCCGTX_SENSE F37
VSSGTX_SENSE F36

(7,43,44,45) +VCCCORE
(43,44,46) +VCCGT

Decoupling Capacitors

+VCCGT

C337	47u/6.3V_8
C50	47u/6.3V_8
C57	47u/6.3V_8
C372	47u/6.3V_8
C327	47u/6.3V_8
C56	47u/6.3V_8
C353	47u/6.3V_8

Place caps on top side socket cavity

+VCCGT

C354	47u/6.3V_8
C371	47u/6.3V_8
C55	47u/6.3V_8
C352	47u/6.3V_8
C338	47u/6.3V_8
C339	47u/6.3V_8
C51	47u/6.3V_8
C52	47u/6.3V_8
C58	47u/6.3V_8

Place caps on backside under socket cavity

+VCCGT

C53	47u/6.3V_8
C54	47u/6.3V_8
C325	47u/6.3V_8
C326	47u/6.3V_8

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(40,43) +VCCSA
(9,14,15,37,42,43,49,50) +VDDQ
(4,34,38,43) +VCCIO
(5,9,33,34,42,43,44) +VCCST_VCCPLL

+VCCSA:
Icc (max) :11A

+VCCIO:
Icc (max) :5.31A

VCCST:
Icc (max) :0.1A

+VDDQ:
Icc (max) :2.5A

+VCCPCC_OC:
Icc (max) :0.11A

J1I SKL_S_CPU LGA1151 ?

SKL_S_CPU_LGA REV = 1.2 ?

9 OF 12

EC-PV-E05: R507 SP_4 (+VCCPLL_OC_R → +VDDQ); R506 *0_4 (→ +VCCPLL_OC)

(12) PCH_2_CPU_TRIGGER
(12) CPU_2_PCH_TRIGGER
R118 20/1% 4 PROC_TRIGOUT B3

EC-DB-E09 / EC-DB-E42

J1J SKL_S_CPU LGA1151

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SKL_S_CPU_LGA REV = 1.2 ?

R499 *560/F_4
CRB 1.1: remove

Decoupling Capacitors

+VCCSA
C89 22U 6.3V X5R 0603
C88 22U 6.3V X5R 0603
Place all caps inside CPU socket cavity top ;

+VCCST_VCCPLL
C498 22U 6.3V X5R 0603
C496 1U 6.3V X5R 0402
Place caps at top socket edge

+VCCIO
C474 22U 6.3V X5R 0603
C473 22U 6.3V X5R 0603
C475 22U 6.3V X5R 0603
C60 22U 6.3V X5R 0603
C86 22U 6.3V X5R 0603
C87 22U 6.3V X5R 0603
C472 0.1U16V X7R 0402
C471 0.1U16V X7R 0402
C375 0.1U16V X7R 0402
Place all caps inside CPU socket cavity top

+VDDQ
C397 22U 6.3V X5R 0603
C355 22U 6.3V X5R 0603
C111 22U 6.3V X5R 0603
C446 22U 6.3V X5R 0603
C74 *22U6.3V X5R 0603
Place cap in socket edge top

+VCCST_VCCPLL
EC-PV-E05: R509 SP_4 (→ +VCCFUSEPRG)
+VCCCORE
R508 *0/5% 4

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CPU POWER/RSVD		
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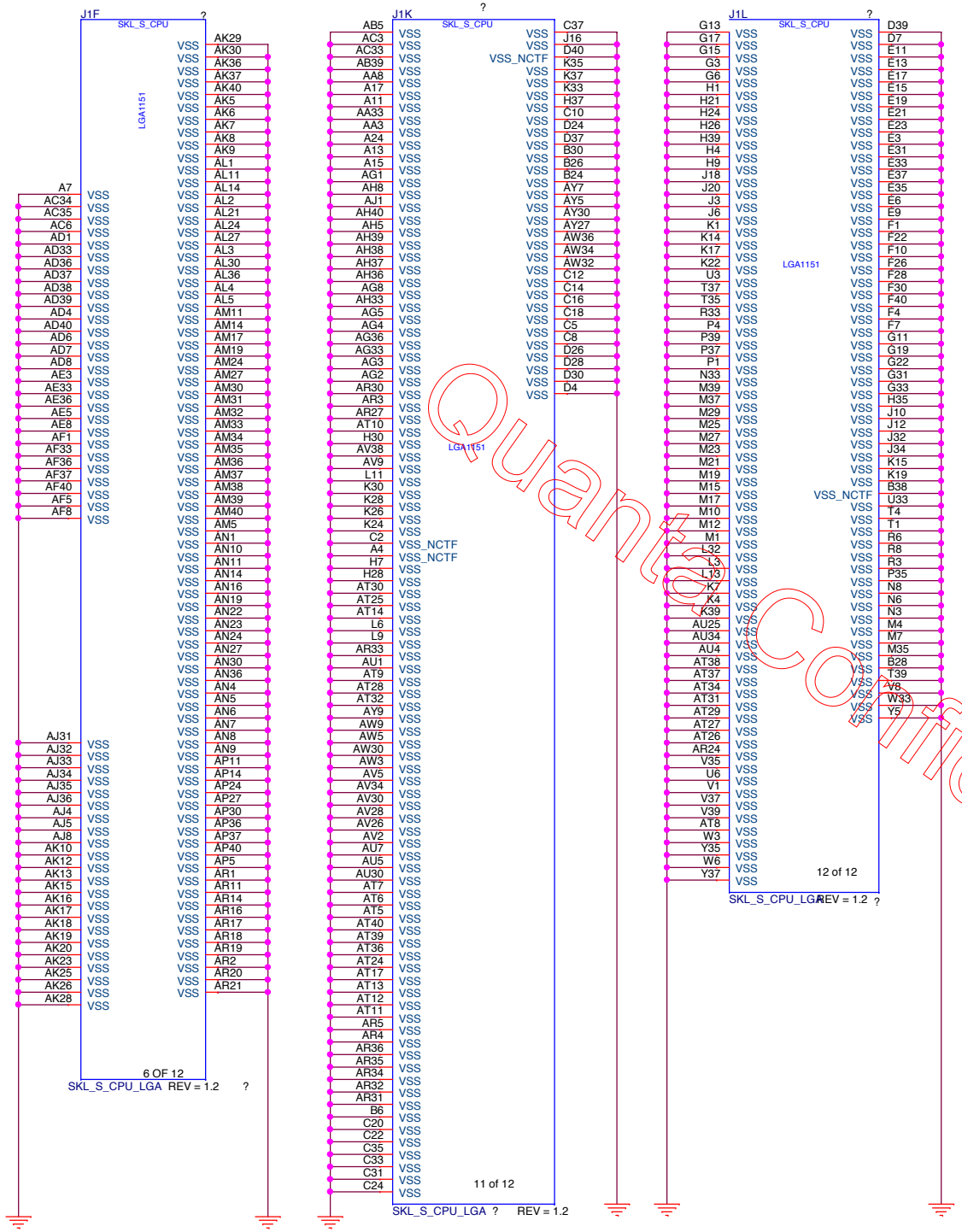

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Project: HP-CRANE

Title: CPU GND

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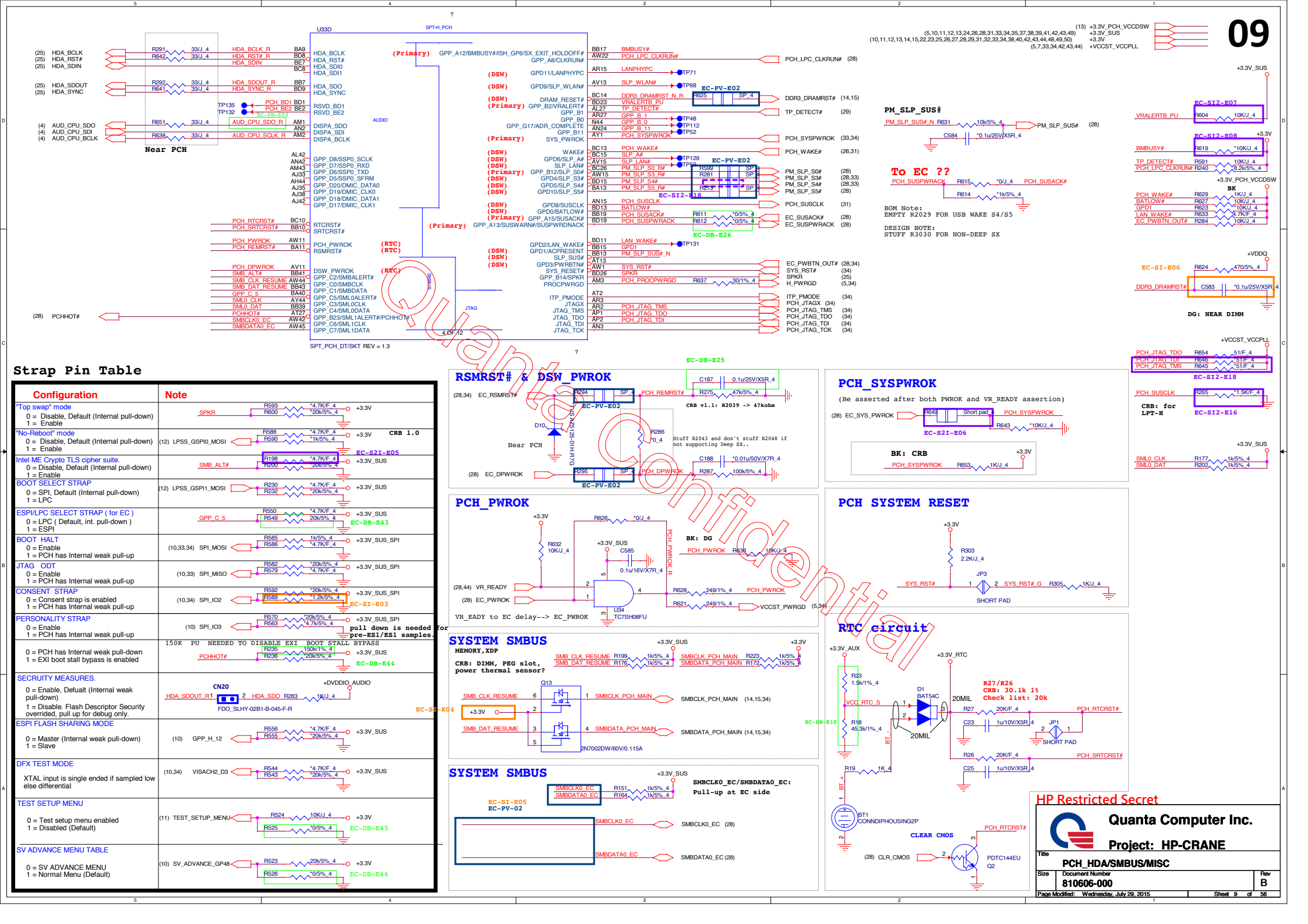
09
U33D
SPT-H_PCH
AUDIO
Near PCH
HDA_BCLK
HDA_RST#
HDA_SDIN
HDA_SDOUT
HDA_SYNC
AUD_CPU_SDO
AUD_CPU_SDI
AUD_CPU_BCLK
PCHHOT#
PCH_RTCRST#
PCH_SRTCRST#
PCH_PWROK
PCH_REMRST#
PCH_DPWROK
SMB_ALT#
SMB_CLK_RESUME
SMB_DAT_RESUME
GPP_C_5
SMLO_CLK
SMLO_DAT
PCHHOT#
SMBCLK0_EC
SMBDATA0_EC
JTAG
4 OF 12
SPT_PCH_DT/SKT REV = 1.3
PM_SLP_SUS#
To EC ??
BOM Note:
EMPTY R2029 FOR USB WAKE S4/S5
DESIGN NOTE:
STUFF R3030 FOR NON-DEEP SX
DG: NEAR DIMM
BK
RSMRST# & DSW_PWROK
PCH_SYSPWROK
(Be asserted after both PWROK and VR_READY assertion)
BK: CRB
PCH_PWROK
BK: DG
VR_EADY to EC delay--> EC_PWROK
PCH SYSTEM RESET
SHORT PAD
SYSTEM SMBUS
MEMORY,XDP
CRB: DIMM, PEG slot, power thermal sensor?
2N7002DW/60V/0.115A
SYSTEM SMBUS
SMBCLK0_EC/SMBDATA0_EC:
Pull-up at EC side
RTC circuit
R27/R26
CRB: 30.1k 1%
Check list: 20k
CLEAR CMOS
Strap Pin Table
Configuration
Note
"Top swap" mode
0 = Disable, Default (Internal pull-down)
1 = Enable
"No-Reboot" mode
0 = Disable, Default (Internal pull-down)
1 = Enable
CRB 1.0
Intel ME Crypto TLS cipher suite.
0 = Disable, Default (Internal pull-down)
1 = Enable
BOOT SELECT STRAP
0 = SPI, Default (Internal pull-down)
1 = LPC
ESPI/LPC SELECT STRAP (for EC)
0 = LPC (Default, int. pull-down)
1 = ESPI
BOOT HALT
0 = Enable
1 = PCH has Internal weak pull-up
JTAG ODT
0 = Enable
1 = PCH has Internal weak pull-up
CONSENT STRAP
0 = Consent strap is enabled
1 = PCH has Internal weak pull-up
PERSONALITY STRAP
0 = Enable
1 = PCH has Internal weak pull-up
pull down is needed for pre-ES1/ES1 samples
0 = PCH has Internal weak pull-down
1 = EXI boot stall bypass is enabled
150K PU NEEDED TO DISABLE EXI BOOT STALL BYPASS
SECRUITY MEASURES.
0 = Enable, Defualt (Internal weak pull-down)
1 = Disable. Flash Descriptor Security overrided, pull up for debug only.
CN20
FDO_SLHY-02B1-B-045-F-R
ESPI FLASH SHARING MODE
0 = Master (Internal weak pull-down)
1 = Slave
DFX TEST MODE
XTAL input is single ended if sampled low else differential
TEST SETUP MENU
0 = Test setup menu enabled
1 = Disabled (Default)
SV ADVANCE MENU TABLE
0 = SV ADVANCE MENU
1 = Normal Menu (Default)
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Quanta Computer Inc.
Project: HP-CRANE
PCH_HDA/SMBUS/MISC
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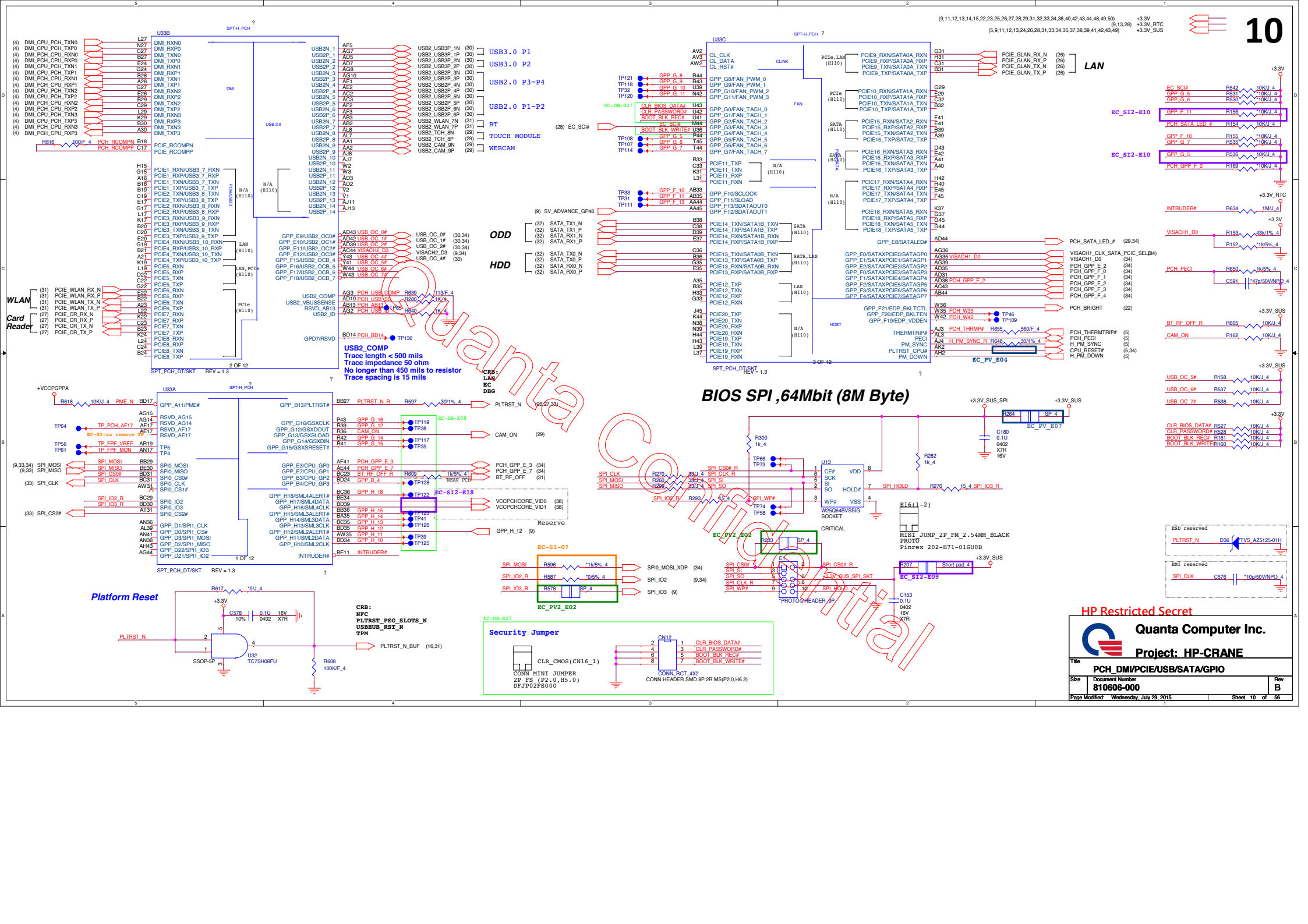
USB3.0 P1
USB3.0 P2
USB2.0 P3~P4
USB2.0 P1~P2
BT
TOUCH MODULE
WEBCAM
LAN
ODD
HDD
WLAN
Card Reader
USB2_COMP
Trace length < 500 mils
Trace impedance 50 ohm
No longer than 450 mils to resistor
Trace spacing is 15 mils
BIOS SPI ,64Mbit (8M Byte)
Platform Reset
Security Jumper
CLR_CMOS(CN16_1)
CONN MINI JUMPER 2P FS (P2.0,H5.0) DFJP02FS000
CONN_RCT_4X2
CONN HEADER SMD 8P 2R MS(P2.0,H6.2)
MINI_JUMP_2P_FM_2.54MM_BLACK PROTO Pinrex 202-H71-01GU0B
W25Q64BVSSIG SOCKET
CRITICAL
*PROTO@HEADER_8P
TC7SH08FU
SSOP-5P
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Quanta Computer Inc.
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PCH_DMI/PCIE/USB/SATA/GPIO
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(9,10,12,13,14,15,22,23,25,26,27,28,29,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V
(5,9,10,12,13,24,26,28,31,33,34,35,37,38,39,41,42,43,49) +3.3V_SUS

USB PORT
(30) USB3_TXN1
(30) USB3_TXP1
(30) USB3_RXN1
(30) USB3_RXP1

USB PORT
(30) USB3_TXN2
(30) USB3_TXP2
(30) USB3_RXN2
(30) USB3_RXP2

3D CAM
(29) USB3_CAM_TX4P
(29) USB3_CAM_TX4N
(29) USB3_CAM_RX4P
(29) USB3_CAM_RX4N

U33F
SPT-H_PCH
C11 USB3_1_TXN
B11 USB3_1_TXP
B7 USB3_1_RXN
A7 USB3_1_RXP
B12 USB3_2_TXN/SSIC_1_TXN
A12 USB3_2_TXP/SSIC_1_TXP
C8 USB3_2_RXN/SSIC_1_RXN
B8 USB3_2_RXP/SSIC_1_RXP
B15 USB3_6_TXN
C15 USB3_6_TXP
K15 USB3_6_RXN
K13 USB3_6_RXP
B14 USB3_5_TXN
C14 USB3_5_TXP
G13 USB3_5_RXN
H13 USB3_5_RXP
D13 USB3_3_TXP/SSIC_2_TXP
C13 USB3_3_TXN/SSIC_2_TXN
A9 USB3_3_RXP/SSIC_2_RXP
B10 USB3_3_RXN/SSIC_2_RXN
B13 USB3_4_TXP
A14 USB3_4_TXN
G11 USB3_4_RXP
E11 USB3_4_RXN
N/A (H110)
USB3 (H110)
SATA
LPC/eSPI
6 OF 12
SPT_PCH_DT/SKT
REV = 1.3

GPP_A1/LAD0/ESPI_IO0 AT22 F_LAD0 (28,31,33)
GPP_A2/LAD1/ESPI_IO1 AV22 F_LAD1 (28,31,33)
GPP_A3/LAD2/ESPI_IO2 AT19 F_LAD2 (28,31,33)
GPP_A4/LAD3/ESPI_IO3 BD16 F_LAD3 (28,31,33)
GPP_A5/LFRAME#/ESPI_CS# BE16 L_FRAME# (28,31,33)
GPP_A6/SERIRQ BA17 SERIRQ SERIRQ (28,33)
GPP_A7/PIRQA#/ESPI_ALERT0# AW17 LPC_PIRQ TP63
GPP_A0/RCIN#/ESPI_ALERT1# AT17 EC_KBRST# EC_KBRST# (28)
GPP_A14/SUS_STAT#/ESPI_RESET# BC18 EC_LPCPD# (28)
GPP_A9/CLKOUT_LPC0/ESPI_CLK BC17 CLKOUT_LPC0 R620 22_4 CK_24M_EC (28)
GPP_A10/CLKOUT_LPC1 AV19 CLKOUT_LPC1 R242 22_4 CK_24M_LPC (33)
R238 22_4 CK_24M_DEBUG (31)
GPP_G19/SMI# M45 PCH_SMI#_R R545 SP_4 PCH_SMI# (33)
GPP_G18/NMI# N43 2X4_PWRDET TP115
EC_PV_E02
GPP_E6/DEVSLP2 AE45 PCH_GPP_E_6 PCH_GPP_E_6 (34)
GPP_E5/DEVSLP1 AG43 PCH_GPP_E_5 PCH_GPP_E_5 (34)
GPP_E4/DEVSLP0 AG42 PCH_GPP_E_4 PCH_GPP_E_4 (34)
GPP_F9/DEVSLP7 AB39 PCH_GPP_F_9 TP40
GPP_F8/DEVSLP6 AB36 PCH_GPP_F_8 TP42
GPP_F7/DEVSLP5 AB43 PCH_GPP_F_7 TP113
GPP_F6/DEVSLP4 AB42 SSD_SATA_DEVSLP TP110
GPP_F5/DEVSLP3 AB41 PCH_CODEC_IRQ TP36

EC-SI-E08
+3.3V
2X4_PWRDET R532 *10K/J_4
CAM_DET# R302 10K/J_4
DMIC_DET# R554 10K/J_4
+3.3V
EC_KBRST# R262 10K/J_4
SERIRQ R263 10K/J_4
PCH_SMI# R546 10K/J_4
R547 *10K/J_4
+3.3V_SUS
LPC_PIRQ R259 10K/J_4
CRB: Connect to +3.3V_SUS directly
SERIRQ & LPC_PIRQ
Note: An external pull-up is required
+3.3V_SUS
SPI_TPM_PIRQ R159 8.2k/5%_4
EC-DB-E04
+3.3V
DGPU_PLTRST_N R157 10K/J_4
EC_SMI# R304 10K/J_4

U33E
SPT-H_PCH
(23) HDMI_HPD AW4 GPP_I0/DDPB_HPD0
AY2 GPP_I1/DDPC_HPD1
AV4 GPP_I2/DDPD_HPD2
(28) EC_SMI# R290 SP_4 EC_SMI#_PCH BA4 GPP_I3/DDPE_HPD3
EC_PV_E02
(22) DDPD_HPD BD7 GPP_I4/EDP_HPD
Active high
GPP_I7/DDPC_CTRLCLK BB3
GPP_I8/DDPC_CTRLDATA BD6
GPP_I5/DDPB_CTRLCLK BA5 DDPB_CTRLCLK DDPB_CTRLCLK (23)
GPP_I6/DDPB_CTRLDATA BC4 DDPB_CTRLDATA DDPB_CTRLDATA (23)
GPP_I9/DDPD_CTRLCLK BE5
GPP_I10/DDPD_CTRLDATA BE6
GPP_F14 Y44 H_SKTOCC# (5)
GPP_F23 V44 CAM_DET# CAM_DET# (29) EC-DB-E05
GPP_F22 W39 DGPU_PLTRST_N DGPU_PLTRST_N (16)
EC_PV_E05
GPP_G23 L43 CAM_FW_UPDATE# (29)
GPP_G22 L44 GPP_G_22 R702 DIS@0_4 EN_+3.3V_VGA (28,49)
GPP_G21 U35 SPI_TPM_PIRQ (33)
GPP_G20 R35 TEST_SETUP_MENU (9)
GPP_H23 BD36 DMIC_DET# DMIC_DET# (29) EC-DB-E03
5 OF 12
SPT_PCH_DT/SKT
REV = 1.3

H/W STRAPS:
DDPB_CTRLDATA: (pull up at HDMI page)
0= Port B is not detected. Default, Internal PD
1= Port B is detected.

EMI reserved
CK_24M_EC C581 *10p/50V/NPO_4
CK_24M_LPC C176 *10p/50V/NPO_4

Quanta Computer Inc.
Project: HP-CRANE
Title: PCH_USB3/LPC
Size: Document Number: 810606-000 Rev: B
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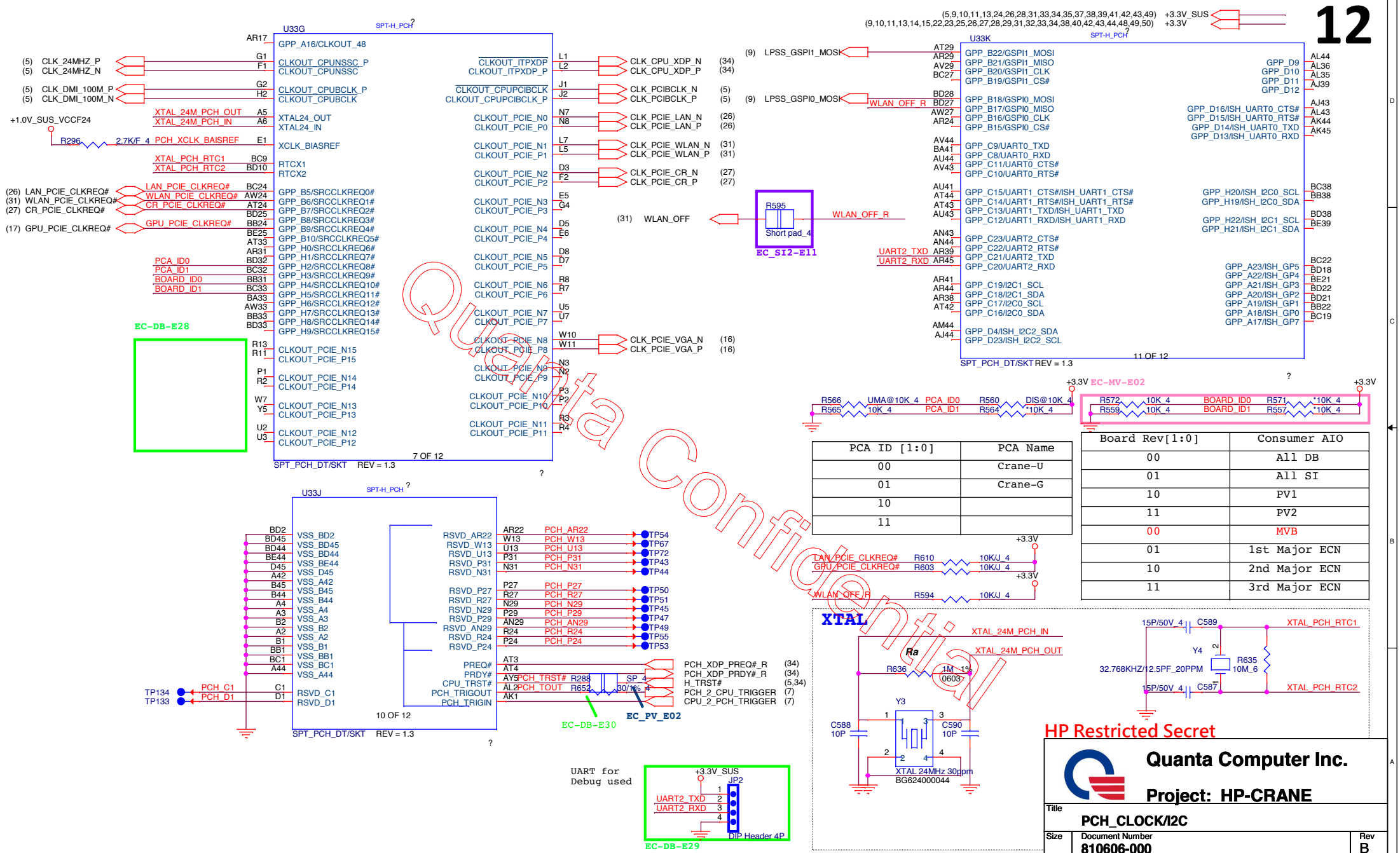

PCA ID [1:0]	PCA Name
00	Crane-U
01	Crane-G
10	
11	

Board Rev[1:0]	Consumer AIO
00	All DB
01	All SI
10	PV1
11	PV2
00	MVB
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN

Quanta Computer Inc.
Project: HP-CRANE

Title		
PCH_CLOCK/I2C		
Size	Document Number	Rev
	810606-000	B
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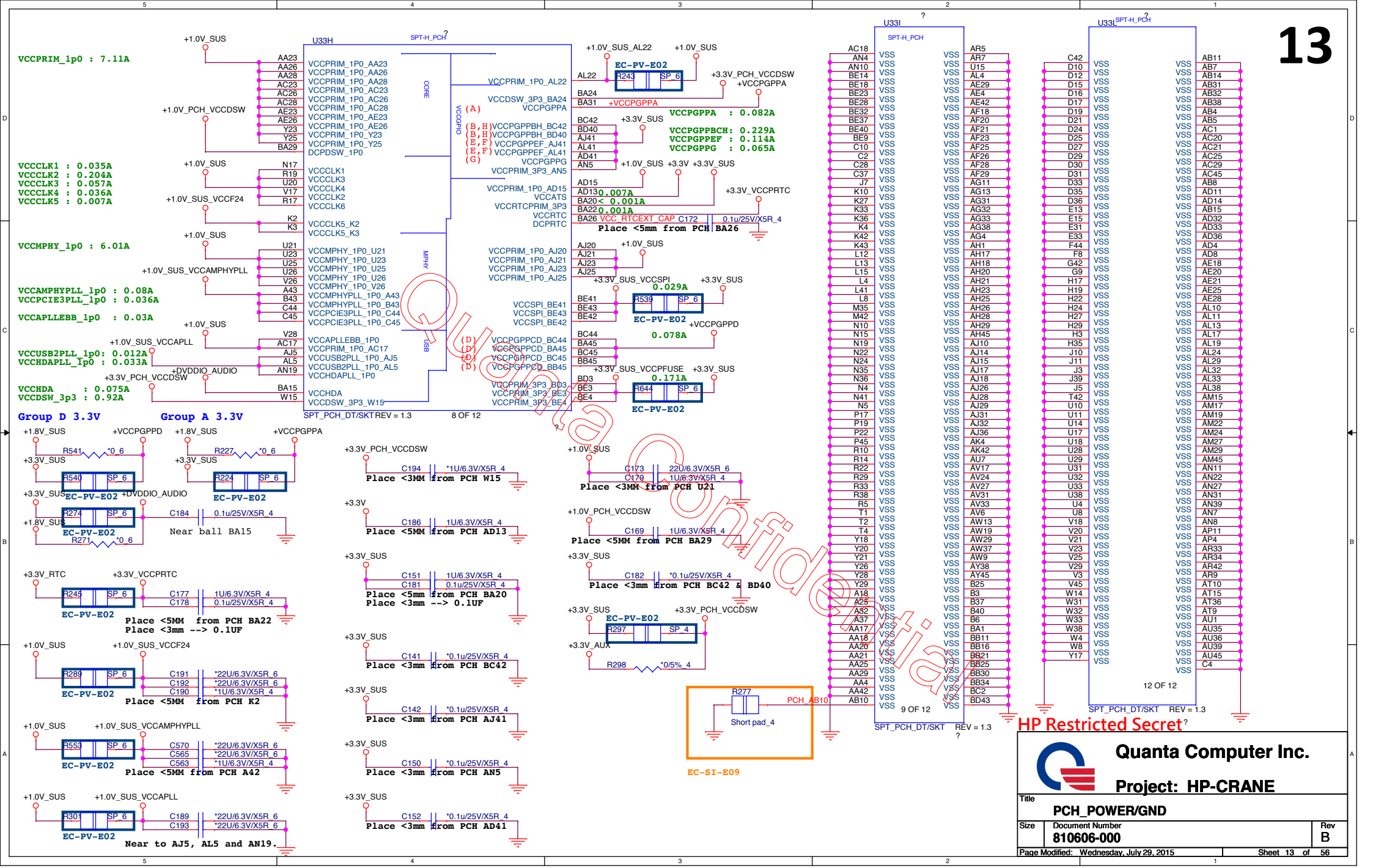
13
VCCPRIM_1p0 : 7.11A
VCCCLK1 : 0.035A
VCCCLK2 : 0.204A
VCCCLK3 : 0.057A
VCCCLK4 : 0.036A
VCCCLK5 : 0.007A
VCCMPHY_1p0 : 6.01A
VCCAMPHYPLL_1p0 : 0.08A
VCCPCIE3PLL_1p0 : 0.036A
VCCAPLLEBB_1p0 : 0.03A
VCCUSB2PLL_1p0: 0.012A
VCCHDAPLL_1p0 : 0.033A
VCCHDA : 0.075A
VCCDSW_3p3 : 0.92A
Group D 3.3V
Group A 3.3V
U33H
SPT-H_PCH
SPT_PCH_DT/SKT REV = 1.3
8 OF 12
U33I
9 OF 12
U33L
12 OF 12
VCCPGPPA : 0.082A
VCCPGPPBCH: 0.229A
VCCPGPPEF : 0.114A
VCCPGPPG : 0.065A
EC-PV-E02
EC-SI-E09
Short pad_4
Place <5mm from PCH BA26
Place <3MM from PCH W15
Place <3MM from PCH U21
Place <3MM from PCH BA29
Place <3mm from PCH BC42 & BD40
Place <5mm from PCH BA20
Place <3mm --> 0.1UF
Place <3mm from PCH BC42
Place <3mm from PCH AJ41
Place <3mm from PCH AN5
Place <3mm from PCH AD41
Place <3MM from PCH AD13
Place <5MM from PCH BA22
Place <3mm --> 0.1UF
Place <5MM from PCH K2
Place <5MM from PCH A42
Near to AJ5, AL5 and AN19.
Near ball BA15
Quanta Confidential
HP Restricted Secret
Quanta Computer Inc.
Project: HP-CRANE
PCH_POWER/GND
Size
Document Number
810606-000
Rev
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CHANNEL A DIMM 0 H=9.2

JDIM1A

(3) M_A_A[15:0]

M_A_A0	98	A0	DQ0	5	M_A_DQ0
M_A_A1	97	A1	DQ1	7	M_A_DQ5
M_A_A2	96	A2	DQ2	15	M_A_DQ6
M_A_A3	95	A3	DQ3	17	M_A_DQ7
M_A_A4	92	A4	DQ4	4	M_A_DQ1
M_A_A5	91	A5	DQ5	6	M_A_DQ4
M_A_A6	90	A6	DQ6	16	M_A_DQ3
M_A_A7	86	A7	DQ7	18	M_A_DQ2
M_A_A8	89	A8	DQ8	21	M_A_DQ12
M_A_A9	85	A9	DQ9	23	M_A_DQ8
M_A_A10	107	A10/AP	DQ10	33	M_A_DQ14
M_A_A11	84	A11	DQ11	35	M_A_DQ10
M_A_A12	83	A12/BC#	DQ12	22	M_A_DQ13
M_A_A13	119	A13	DQ13	24	M_A_DQ9
M_A_A14	80	A14	DQ14	34	M_A_DQ11
M_A_A15	78	A15	DQ15	36	M_A_DQ15
			DQ16	39	M_A_DQ21
(3) M_A_BS#[2..0]			DQ17	41	M_A_DQ20
M_A_BS#0	109	BA0	DQ18	51	M_A_DQ18
M_A_BS#1	108	BA1	DQ19	53	M_A_DQ22
M_A_BS#2	79	BA2	DQ20	40	M_A_DQ16
(3) M_A_CS#0	114	S0#	DQ21	42	M_A_DQ17
(3) M_A_CS#1	121	S1#	DQ22	50	M_A_DQ19
(3) M_A_CLKP0	101	CK0	DQ23	52	M_A_DQ23
(3) M_A_CLKN0	103	CK0#	DQ24	57	M_A_DQ29
(3) M_A_CLKP1	102	CK1	DQ25	59	M_A_DQ24
(3) M_A_CLKN1	104	CK1#	DQ26	67	M_A_DQ31
(3) M_A_CKE0	73	CKE0	DQ27	69	M_A_DQ26
(3) M_A_CKE1	74	CKE1	DQ28	56	M_A_DQ28
(3) M_A_CAS#	115	CAS#	DQ29	58	M_A_DQ25
(3) M_A_RAS#	110	RAS#	DQ30	68	M_A_DQ30
(3) M_A_WE#	113	WE#	DQ31	70	M_A_DQ27
SA0_A_1	197	SA0	DQ32	129	M_A_DQ33
SA1_A_1	201	SA1	DQ33	131	M_A_DQ32
(9,15,34) SMBCLK_PCH_MAIN	202	SCL	DQ34	141	M_A_DQ38
(9,15,34) SMBDATA_PCH_MAIN	200	SDA	DQ35	143	M_A_DQ35
			DQ36	130	M_A_DQ37
(3) M_A_ODT0	116	ODT0	DQ37	132	M_A_DQ36
(3) M_A_ODT1	120	ODT1	DQ38	140	M_A_DQ29
			DQ39	142	M_A_DQ34
	11	DM0	DQ40	147	M_A_DQ40
	28	DM1	DQ41	149	M_A_DQ44
	46	DM2	DQ42	157	M_A_DQ47
	63	DM3	DQ43	159	M_A_DQ46
	136	DM4	DQ44	146	M_A_DQ45
	153	DM5	DQ45	148	M_A_DQ41
	170	DM6	DQ46	158	M_A_DQ42
	187	DM7	DQ47	160	M_A_DQ43
(3) M_A_DQS0	12	DQS0	DQ48	163	M_A_DQ50
(3) M_A_DQS1	29	DQS1	DQ49	165	M_A_DQ48
(3) M_A_DQS2	47	DQS2	DQ50	175	M_A_DQ55
(3) M_A_DQS3	64	DQS3	DQ51	177	M_A_DQ49
(3) M_A_DQS4	137	DQS4	DQ52	164	M_A_DQ52
(3) M_A_DQS5	154	DQS5	DQ53	166	M_A_DQ54
(3) M_A_DQS6	171	DQS6	DQ54	174	M_A_DQ53
(3) M_A_DQS7	188	DQS7	DQ55	176	M_A_DQ51
(3) M_A_DQS#0	10	DQS#0	DQ56	181	M_A_DQ63
(3) M_A_DQS#1	27	DQS#1	DQ57	183	M_A_DQ58
(3) M_A_DQS#2	45	DQS#2	DQ58	191	M_A_DQ57
(3) M_A_DQS#3	62	DQS#3	DQ59	193	M_A_DQ60
(3) M_A_DQS#4	135	DQS#4	DQ60	180	M_A_DQ56
(3) M_A_DQS#5	152	DQS#5	DQ61	182	M_A_DQ61
(3) M_A_DQS#6	169	DQS#6	DQ62	192	M_A_DQ59
(3) M_A_DQS#7	186	DQS#7	DQ63	194	M_A_DQ62

PC2100 DDR3 SDRAM SO-DIMM (204P)

EC-SI-E26

DDR3-DIMM0_H=9.15_STD

M_A_DQ[63..0] (3)

EC-DB-E11
SWAP Memory dimm data bus

JDIM1B

+VDDQ	75	VDD1	VSS16 44
	76	VDD2	VSS17 48
	81	VDD3	VSS18 49
	82	VDD4	VSS19 54
	87	VDD5	VSS20 55
	88	VDD6	VSS21 60
	93	VDD7	VSS22 61
	94	VDD8	VSS23 65
	99	VDD9	VSS24 66
	100	VDD10	VSS25 71
	105	VDD11	VSS26 72
	106	VDD12	VSS27 127
	111	VDD13	VSS28 128
	112	VDD14	VSS29 133
	117	VDD15	VSS30 134
	118	VDD16	VSS31 138
	123	VDD17	VSS32 139
	124	VDD18	VSS33 144
			VSS34 145
+3.3V	199	VDDSPD	VSS35 150
			VSS36 151
	77	NC1	VSS37 155
	122	NC2	VSS38 156
	125	NCTEST	VSS39 161
			VSS40 162
	198	EVENT#	VSS41 167
(9,15) DDR3_DRAMRST#	30	RESET#	VSS42 168
			VSS43 172
			VSS44 173
DIMM_DQ_R_VREF_A	1	VREF_DQ	VSS45 178
DIMM_CA_VREF_A	126	VREF_CA	VSS46 179
			VSS47 184
			VSS48 185
	2	VSS1	VSS49 189
	3	VSS2	VSS50 190
	8	VSS3	VSS51 195
	9	VSS4	VSS52 196
	13	VSS5	
	14	VSS6	
	19	VSS7	
	20	VSS8	
	25	VSS9	
	26	VSS10	VTT1 203
	31	VSS11	VTT2 204
	32	VSS12	
	37	VSS13	GND 205
	38	VSS14	GND 206
	43	VSS15	

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=9.15_STD

EC-SI-E26

SMDDR_VTERM

(7,9,15,37,42,43,49,50) +VDDQ
(15,37,43) SMDDR_VTERM
(9,10,11,12,13,15,22,23,25,26,27,28,29,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V

M_A_CLKP0 R451 *100KR_4 M_A_CLKN0

M_A_CLKP1 R469 *100KR_4 M_A_CLKN1

+3.3V

R515 *4.7KR_4

R519 *4.7KR_4

SA1_A_1
SA0_A_1

R516 10k/5%_4

R520 10k/5%_4

SPD SA0	0
SPD SA1	0

+3.3V

C538 0.1u/25V/X5R_4
C539 0.1u/25V/X5R_4

CAD note:
Place between CHA & CHB.
Don't punch VIA.

Place these Caps near CHA So-Dimm0.

+VDDQ

C462	*22u/6.3V/X5R_6
C503	*22u/6.3V/X5R_6
C344	10U/6.3V/X5R_6
C390	10U/6.3V/X5R_6
C346	10U/6.3V/X5R_6
C392	10U/6.3V/X5R_6
C445	10U/6.3V/X5R_6
C443	10U/6.3V/X5R_6
C364	1U/6.3V/X5R_4
C430	1U/6.3V/X5R_4
C366	1U/6.3V/X5R_4
C420	1U/6.3V/X5R_4
C452	0.1u/25V/X5R_4
C376	0.1u/25V/X5R_4
C410	0.1u/25V/X5R_4
C341	0.1u/25V/X5R_4
C399	0.1u/25V/X5R_4

On "Bottom side"

SMDDR_VTERM

C532	*22U/6.3V/X5R_6
C533	*22U/6.3V/X5R_6
C548	*10U/6.3V/X5R_6
C547	*10U/6.3V/X5R_6
C555	10U/6.3V/X5R_6
C543	1U/6.3V/X5R_4
C542	1U/6.3V/X5R_4
C550	1U/6.3V/X5R_4
C549	1U/6.3V/X5R_4

BK: CRB (4.7UF + 0.1UF)

+VDDQ

C342	180P/50V_4
C454	180P/50V_4
C379	180P/50V_4

EMI

DIMMA_DQ_VREF

+VDDQ

R365 1K_4

C262 *0.1u/25V/X5R_4

DQ_DDRA_R

EC-PV-E02

R366 SP_4

DIMM_DQ_R_VREF_A

R367 2.0/1%_4

DIMM_DQ_CPU_VREF_A (3)

C265 0.022u/16V/X7R_4

DIMMA_VREF_RC

R364 24.9/1%_4

R363 1K_4

C263 0.1u/25V/X5R_4

C264 0.1u/25V/X5R_4

CAD NOTE:
NEAR TO DIMM

DIMMA_CA_VREF

+VDDQ

R503 1K_4

C359 0.1u/25V/X5R_4

CA_DDRA_R

EC-PV-E02

R495 SP_4

DIMM_CA_VREF_A

DIMM_CA_VREF_A (3)

R502 1K_4

C467 0.1u/25V/X5R_4

CAD NOTE:
NEAR TO DIMM

Quanta Computer Inc.

Project: HP-CRANE

Title: **DDR3 CHA DIMM 0**

Size	Document Number	Rev
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CHANNEL B DIMM 0 H=5.2

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_STD

EC-SI-E26

(3) M_B_A[15:0]

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15

(3) M_B_BS#[2..0]

M_B_BS#0 M_B_BS#1 M_B_BS#2

(3) M_B_CS#0 (3) M_B_CS#1 (3) M_B_CLKP0 (3) M_B_CLKN0 (3) M_B_CLKP1 (3) M_B_CLKN1 (3) M_B_CKE0 (3) M_B_CKE1 (3) M_B_CAS# (3) M_B_RAS# (3) M_B_WE#

SA0_B_0 SA1_B_0

(9,14,34) SMBCLK_PCH_MAIN (9,14,34) SMBDATA_PCH_MAIN

(3) M_B_ODT0 (3) M_B_ODT1

(3) M_B_DQS0 (3) M_B_DQS1 (3) M_B_DQS2 (3) M_B_DQS3 (3) M_B_DQS4 (3) M_B_DQS5 (3) M_B_DQS6 (3) M_B_DQS7 (3) M_B_DQS#0 (3) M_B_DQS#1 (3) M_B_DQS#2 (3) M_B_DQS#3 (3) M_B_DQS#4 (3) M_B_DQS#5 (3) M_B_DQS#6 (3) M_B_DQS#7

M_B_DQ[0..63] (3)

EC-DB-E11
SWAP Memory dimm data bus

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_STD

EC-SI-E26

+VDDQ

+3.3V

TP106 DIMM_EVENT#_B

(9,14) DDR3_DRAMRST#

DIMM_DQ_R_VREF_B

DIMM_CA_VREF_B

SMDDR_VTERM

(7,9,14,37,42,43,49,50) +VDDQ
(14,37,43) SMDDR_VTERM
(9,10,11,12,13,14,22,23,25,26,27,28,29,31,32,33,34,38,40,42,43,44,48,49,50)

BK: CRB--> NO BOTH

M_B_CLKP0 R463 *100KR_4 M_B_CLKN0

M_B_CLKP1 R464 *100KR_4 M_B_CLKN1

DDR3_DRAMRST#

C291 100p/50V_4

+3.3V

R518 *4.7KR_4 R521 4.7KR_4

SA1_B_0 SA0_B_0

R517 10k/5%_4 R522 *0R_4

SPD SA0	0
SPD SA1	1

+3.3V

C540 0.1u/25V/X5R_4
C541 0.1u/25V/X5R_4

Close to PIN199 OF DIMM

Place these Caps near CHB So-Dimm0.

+VDDQ

C485 *22U/6.3V/X5R_6
C477 *22U/6.3V/X5R_6

C450 10U/6.3V/X5R_6
C345 10U/6.3V/X5R_6
C440 10U/6.3V/X5R_6
C391 10U/6.3V/X5R_6
C348 10U/6.3V/X5R_6
C394 10U/6.3V/X5R_6

C423 1U/6.3V/X5R_4
C362 1U/6.3V/X5R_4
C427 1U/6.3V/X5R_4
C365 1U/6.3V/X5R_4

C455 0.1u/25V/X5R_4
C335 0.1u/25V/X5R_4
C386 0.1u/25V/X5R_4
C408 0.1u/25V/X5R_4
C340 0.1u/25V/X5R_4

SMDDR_VTERM

C544 *22U/6.3V/X5R_6
C537 *22U/6.3V/X5R_6

C551 *10U/6.3V/X5R_6
C552 10U/6.3V/X5R_6
C554 *10U/6.3V/X5R_6

C534 1U/6.3V/X5R_4
C535 1U/6.3V/X5R_4
C545 1U/6.3V/X5R_4
C546 1U/6.3V/X5R_4

BK: CRB (4.7UF + 0.1UF)

+VDDQ

C396 180P/50V_4
C358 180P/50V_4
C439 180P/50V_4

EMI

On "Bottom side"

DIMMB_DQ_VREF

+VDDQ

R371 1K_4 C274 0.1u/25V/X5R_4

DQ_DDRB_R EC-PV-E02 R369 SP_4 DIMM_DQ_R_VREF_B R368 2.0/1%_4 DIMM_DQ_CPU_VREF_B (3)

R372 1K_4 C273 0.1u/25V/X5R_4 C267 0.1u/25V/X5R_4

C266 0.022u/16V/X7R_4

DIMMB_VREF_RC

R370 24.9/1%_4

either or R343 or R3047?

CAD NOTE: NEAR TO DIMM

DIMMB_CA_VREF

+VDDQ

R500 1K_4 C459 0.1u/25V/X5R_4

CA_DDRB_R EC-PV-E02 R501 SP_4 DIMM_CA_VREF_B DIMM_CA_VREF_B (3)

R504 1K_4 C487 0.1u/25V/X5R_4

CAD NOTE: NEAR TO DIMM

Quanta Computer Inc.

Project: HP-CRANE

Title: DDR3 CHB DIMM 0

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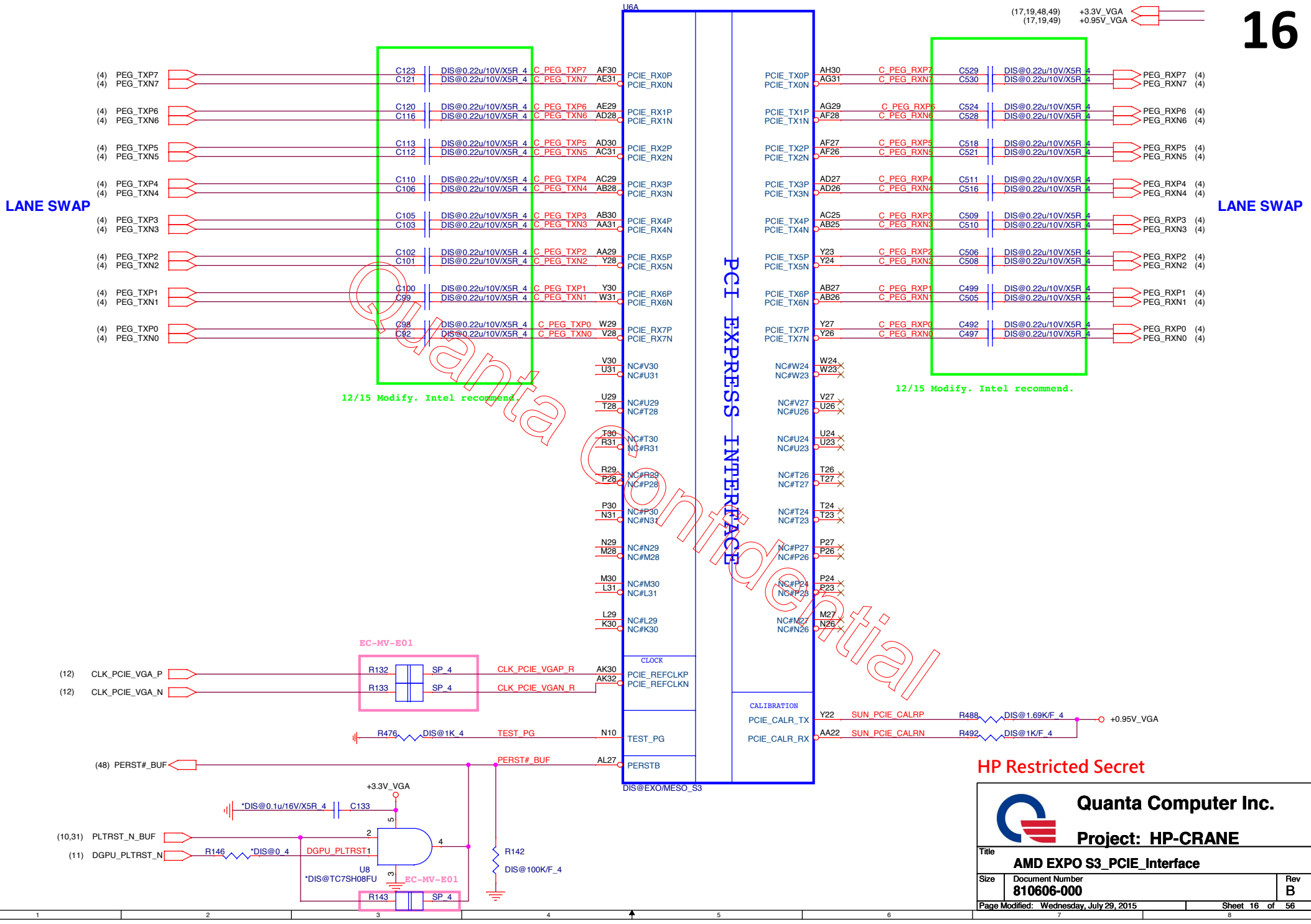

HP Restricted Secret

Quanta Computer Inc.

Project: HP-CRANE

Title: AMD EXPO S3_PCIE_Interface

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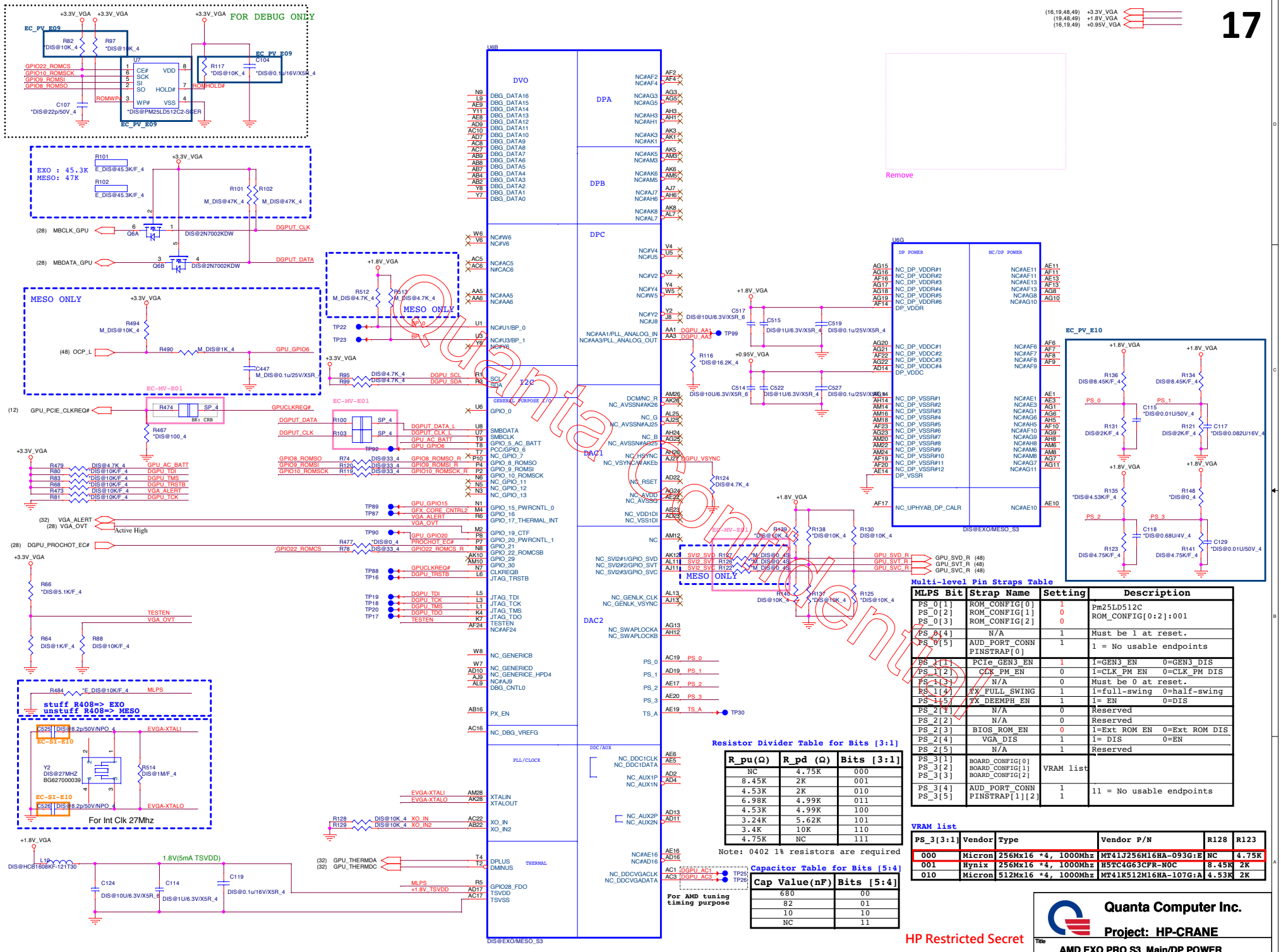

Multi-level Pin Straps Table

MLPS Bit	Strap Name	Setting	Description
PS_0[1]	ROM_CONFIG[0]	1	Pm25LD512C
PS_0[2]	ROM_CONFIG[1]	0	ROM_CONFIG[0:2]:001
PS_0[3]	ROM_CONFIG[2]	0	
PS_0[4]	N/A	1	Must be 1 at reset.
PS_0[5]	AUD_PORT_CONN PINSTRAP[0]	1	1 = No usable endpoints
PS_1[1]	PCIe_GEN3_EN	1	1=GEN3_EN 0=GEN3_DIS
PS_1[2]	CLK_PM_EN	0	1=CLK_PM_EN 0=CLK_PM_DIS
PS_1[3]	N/A	0	Must be 0 at reset.
PS_1[4]	TX_FULL_SWING	1	1=full-swing 0=half-swing
PS_1[5]	TX_DEEMPH_EN	1	1= EN 0=DIS
PS_2[1]	N/A	0	Reserved
PS_2[2]	N/A	0	Reserved
PS_2[3]	BIOS_ROM_EN	0	1=Ext ROM EN 0=Ext ROM DIS
PS_2[4]	VGA_DIS	1	1= DIS 0=EN
PS_2[5]	N/A	1	Reserved
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	VRAM list	
PS_3[4] PS_3[5]	AUD_PORT_CONN PINSTRAP[1][2]	1 1	11 = No usable endpoints

Resistor Divider Table for Bits [3:1]

R_pu(Ω)	R_pd (Ω)	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Note: 0402 1% resistors are required

Capacitor Table for Bits [5:4]

Cap Value(nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

VRAM list

PS_3[3:1]	Vendor	Type	Vendor P/N	R128	R123
000	Micron	256Mx16 *4, 1000Mhz	MT41J256M16HA-093G:E	NC	4.75K
001	Hynix	256Mx16 *4, 1000Mhz	H5TC4G63CFR-N0C	8.45K	2K
010	Micron	512Mx16 *4, 1000Mhz	MT41K512M16HA-107G:A	4.53K	2K

Quanta Computer Inc.
Project: HP-CRANE

Title: AMD EXO PRO S3_Main/DP POWER
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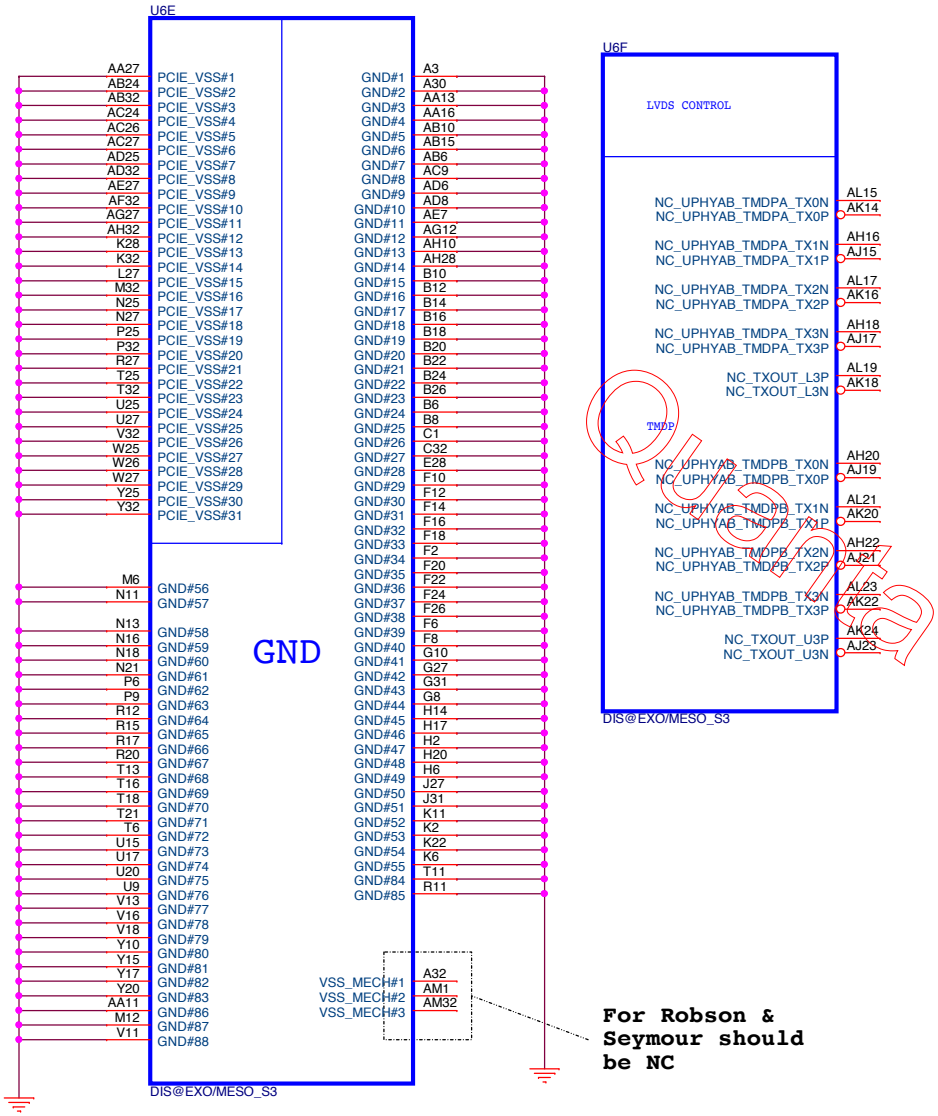
(16,17,19,48,49) +3.3V_VGA



For Robson & Seymour should be NC

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

VGA HOLE

Quanta Computer Inc.

Project: HP-CRANE

Title: AMD EXO PRO S3_GND/LVDS/Strap

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(20,21,49) +1.5V_VGA
(17,48,49) +1.8V_VGA
(16,17,49) +0.95V_VGA
(48,49) +VGA_CORE

+1.5V_VGA
1.5V (DDR3, MVDDQ = 1.5V@1.2A)
C41 DIS@10U/6.3V/X5R_6
C40 DIS@10U/6.3V/X5R_6
C12 DIS@10U/6.3V/X5R_6
C11 DIS@2.2U/6.3V/X5R_4
C402 DIS@2.2U/6.3V/X5R_4
C412 DIS@2.2U/6.3V/X5R_4
C419 DIS@2.2U/6.3V/X5R_4
C395 DIS@2.2U/6.3V/X5R_4

U6D
MEM I/O
H13 VDDR1#1
H16 VDDR1#2
H19 VDDR1#3
J10 VDDR1#4
J23 VDDR1#5
J24 VDDR1#6
J9 VDDR1#7
K10 VDDR1#8
K23 VDDR1#9
K24 VDDR1#10
K9 VDDR1#11
L11 VDDR1#12
L12 VDDR1#13
L13 VDDR1#14
L20 VDDR1#15
L21 VDDR1#16
L22 VDDR1#17

LEVEL TRANSLATION
AA20 VDD_CT#1
AA21 VDD_CT#2
AB20 VDD_CT#3
AB21 VDD_CT#4

I/O
AA17 VDDR3#1
AA18 VDDR3#2
AB17 VDDR3#3
AB18 VDDR3#4
V12 NC_VDDR4#1
Y12 NC_VDDR4#2
U12 NC_VDDR4#3

PLL
L8 MPLL_PVDD
H7 SPLL_PVDD
H8 SPLL_VDDC
J7 SPLL_PVSS

DIS@EXO/MESO_S3

+1.8V_VGA
L32 DIS@BLM15PX181SN1D
1.8V@13mA
+1.8V_VDDCT
C502 DIS@10U/6.3V/X5R_6
C495 DIS@1U/6.3V/X5R_4
C490 DIS@0.1u/25V/X5R_4

+3.3V_VGA
L9 DIS@BLM15PX181SN1D
3.3V@25mA
+3.3V_VDDR3
C127 DIS@10U/6.3V/X5R_6
C479 DIS@1U/6.3V/X5R_4
C126 DIS@1U/6.3V/X5R_4
C125 DIS@1U/6.3V/X5R_4

+1.8V_VGA
L7 DIS@BLM15PX181SN1D
1.8V@90mA
+MPV18
Memory Phase Lock Loop Power :
C64 DIS@10U/6.3V/X5R_6
C63 DIS@1U/6.3V/X5R_4
C62 DIS@0.1U/16V/X5R_4

+1.8V_VGA
L30 DIS@PBY160808T-121Y-N
1.8V@75mA
+SPV18
Engine Phase Lock Loop Power :
analog power pin for engine PLL
C367 DIS@10U/6.3V/X5R_6
C368 DIS@1U/10V/X5R_4
C369 DIS@0.1u/25V/X5R_4

+0.95V_VGA
L31 DIS@PBY160808T-121Y-N
0.95V@100mA
+0.95V_VGA_SPV10
Engine Phase Lock Loop Power :
digital power pin for engine PLL
C407 DIS@10U/6.3V/X5R_6
C404 DIS@1U/10V/X5R_4
C405 DIS@0.1u/25V/X5R_4

PCIE
AM30 PCIE_PVDD
NC#AB23
NC#AC23
NC#AD24
NC#AE24
NC#AE25
NC#AE26
NC#AF25
NC#AG26
PCIE_PVDD : 1.8V @ 100mA
C504 DIS@0.01U/50V/X5R_4
C513 0.1u/25V/X5R_4
C523 DIS@1U/10V/X5R_4
C520 DIS@10U/6.3V/X5R_6

L23 PCIE_VDDC#1
L24 PCIE_VDDC#2
L25 PCIE_VDDC#3
L26 PCIE_VDDC#4
M22 PCIE_VDDC#5
N22 PCIE_VDDC#6
N23 PCIE_VDDC#7
N24 PCIE_VDDC#8
R22 PCIE_VDDC#9
T22 PCIE_VDDC#10
U22 PCIE_VDDC#11
V22 PCIE_VDDC#12
PCIE_VDDC : 0.95V @ 1A (GEN3.0)
C453 DIS@1U/6.3V/X5R_4
C436 DIS@1U/6.3V/X5R_4
C458 DIS@1U/6.3V/X5R_4
C449 DIS@1U/6.3V/X5R_4
C441 DIS@1U/6.3V/X5R_4
C428 DIS@1U/6.3V/X5R_4
C437 DIS@1U/6.3V/X5R_4
C416 DIS@10U/6.3V/X5R_6
C403 DIS@10U/6.3V/X5R_6

CORE POWER
AA15 VDDC#1
N15 VDDC#2
N17 VDDC#3
R13 VDDC#4
R16 VDDC#5
R18 VDDC#6
Y21 VDDC#7
T12 VDDC#8
T15 VDDC#9
T17 VDDC#10
T20 VDDC#11
U13 VDDC#12
U16 VDDC#13
U18 VDDC#14
V21 VDDC#15
V15 VDDC#16
V17 VDDC#17
V20 VDDC#18
Y13 VDDC#20
Y16 VDDC#21
Y18 VDDC#22
AA12 VDDC#23
M11 VDDC#24
N12 VDDC#25
U11 VDDC#26
AB11 VDDC/VARY_BL
AB12 VDDC/DIGON
AB13 VDDC/GENERICA
W9 VDDC/GENERICC
AC11 VDDC/DDC2CLK
AC13 VDDC/DDC2DATA
AC14 VDDC/HPD1
U10 VDDC/GPIO_1
T10 VDDC/GPIO_2
W10 VDDC/GPIO_18
Y9 VDDC/GPIO_14_HPD2
P21 BIF_VDDC_1
U21 BIF_VDDC_2
VDDC+VDDCI
0.85~1.1V(14.2A peak)(Ripple < 87.2mV)
C476 DIS@1U/6.3V/X5R_4
C425 DIS@1U/6.3V/X5R_4
C444 DIS@1U/6.3V/X5R_4
C470 DIS@1U/6.3V/X5R_4
C429 DIS@1U/6.3V/X5R_4
C491 DIS@1U/6.3V/X5R_4
C489 DIS@1U/6.3V/X5R_4
C465 DIS@1U/6.3V/X5R_4
C482 DIS@10U/6.3V/X5R_6
C494 DIS@10U/6.3V/X5R_6
C466 DIS@1U/6.3V/X5R_4
C481 DIS@1U/6.3V/X5R_4
C460 DIS@1U/6.3V/X5R_4
C480 DIS@1U/6.3V/X5R_4
C456 DIS@1U/6.3V/X5R_4
C469 DIS@1U/6.3V/X5R_4
C483 DIS@1U/6.3V/X5R_4
C486 DIS@1U/6.3V/X5R_4
C464 DIS@10U/6.3V/X5R_6
C414 DIS@10U/6.3V/X5R_6
C461 DIS@1U/6.3V/X5R_4
C417 DIS@1U/6.3V/X5R_4
C478 DIS@1U/6.3V/X5R_4
C468 DIS@1U/6.3V/X5R_4
C406 DIS@1U/6.3V/X5R_4
C432 DIS@1U/6.3V/X5R_4
C61 DIS@1U/10V/X5R_4
C415 DIS@1U/6.3V/X5R_4
C401 DIS@1U/6.3V/X5R_4
C488 DIS@1U/6.3V/X5R_4
C424 DIS@2.2U/10V/X5R_4
C411 DIS@2.2U/10V/X5R_4
C507 330U/2.5V/ESR9_7343
EC-SI-xx Follow N61

ISOLATED CORE I/O
M13 VDDCI#1
M15 VDDCI#2
M16 VDDCI#3
M17 VDDCI#4
M18 VDDCI#5
M20 VDDCI#6
M21 VDDCI#7
N20 VDDCI#8
BIF_VDDC : 0.95V @ 1.4A
C81 DIS@1U/6.3V/X5R_4
C73 DIS@1U/6.3V/X5R_4
C438 DIS@10U/6.3V/X5R_6
0.95V~1.1V(2A VDDCI)
C493 DIS@0.1u/25V/X5R_4
C463 DIS@0.1u/25V/X5R_4
C451 DIS@0.1u/25V/X5R_4
C457 DIS@1U/10V/X5R_4
C435 DIS@1U/6.3V/X5R_4
C448 DIS@10U/6.3V/X5R_6

W1 NC#W1/FB_VDDCI
W3 NC#W3/FB_VSS
AC20 NC#FB_VDDC
AD20 NC#FB_VSS
VDDC_SEN_R R511 *M_DIS@0_4S
VDDC_RTN_R R519 *M_DIS@0_4S
VCORE_SEN/RTN route as differential pair
VDDC_SEN (48)
VDDC_RTN (48)
MESO ONLY

+1.8V_VGA
+0.95V_VGA
+VGA_CORE

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(19,21,49) +1.5V_VGA

U6C

MEMORY INTERFACE

(21) VMA_ODT0 — VMA_ODT0
(21) VMA_ODT1 — VMA_ODT1
(21) VMA_RAS0# — VMA_RAS0#
(21) VMA_RAS1# — VMA_RAS1#
(21) VMA_CAS0# — VMA_CAS0#
(21) VMA_CAS1# — VMA_CAS1#
(21) VMA_WE0# — VMA_WE0#
(21) VMA_WE1# — VMA_WE1#
(21) VMA_CS0# — VMA_CS0#
(21) VMA_CS1# — VMA_CS1#
(21) VMA_CKE0 — VMA_CKE0
(21) VMA_CKE1 — VMA_CKE1
(21) VMA_CLK0 — VMA_CLK0
(21) VMA_CLK0# — VMA_CLK0#
(21) VMA_CLK1 — VMA_CLK1
(21) VMA_CLK1# — VMA_CLK1#
(21) VMA_WDQS[7..0] — VMA_WDQS[7..0]
(21) VMA_RDQS[7..0] — VMA_RDQS[7..0]
(21) VMA_DM[7..0] — VMA_DM[7..0]
(21) VMA_DQ[63..0] — VMA_DQ[63..0]
(21) VMA_MA[15..0] — VMA_MA[15..0]
(21) VMA_BA0 — VMA_BA0
(21) VMA_BA1 — VMA_BA1
(21) VMA_BA2 — VMA_BA2

support 1Gbit VRAM (64M X 16)

VMA_DQ0	K27	DQA0_0	
VMA_DQ1	J29	DQA0_1	
VMA_DQ2	H30	DQA0_2	
VMA_DQ3	H32	DQA0_3	
VMA_DQ4	G29	DQA0_4	
VMA_DQ5	F28	DQA0_5	
VMA_DQ6	F32	DQA0_6	
VMA_DQ7	F30	DQA0_7	
VMA_DQ8	C30	DQA0_8	
VMA_DQ9	F27	DQA0_9	
VMA_DQ10	A28	DQA0_10	
VMA_DQ11	C28	DQA0_11	
VMA_DQ12	E27	DQA0_12	
VMA_DQ13	G26	DQA0_13	
VMA_DQ14	D26	DQA0_14	
VMA_DQ15	F25	DQA0_15	
VMA_DQ16	A25	DQA0_16	
VMA_DQ17	C25	DQA0_17	
VMA_DQ18	E25	DQA0_18	
VMA_DQ19	D24	DQA0_19	
VMA_DQ20	E23	DQA0_20	
VMA_DQ21	F23	DQA0_21	
VMA_DQ22	D22	DQA0_22	
VMA_DQ23	F21	DQA0_23	
VMA_DQ24	E21	DQA0_24	
VMA_DQ25	D20	DQA0_25	
VMA_DQ26	F19	DQA0_26	
VMA_DQ27	A19	DQA0_27	
VMA_DQ28	D18	DQA0_28	
VMA_DQ29	F17	DQA0_29	
VMA_DQ30	A17	DQA0_30	
VMA_DQ31	C17	DQA0_31	
VMA_DQ32	E17	DQA1_0	
VMA_DQ33	D16	DQA1_1	
VMA_DQ34	F15	DQA1_2	
VMA_DQ35	A15	DQA1_3	
VMA_DQ36	D14	DQA1_4	
VMA_DQ37	F13	DQA1_5	
VMA_DQ38	A13	DQA1_6	
VMA_DQ39	C13	DQA1_7	
VMA_DQ40	E11	DQA1_8	
VMA_DQ41	A11	DQA1_9	
VMA_DQ42	C11	DQA1_10	
VMA_DQ43	F11	DQA1_11	
VMA_DQ44	A9	DQA1_12	
VMA_DQ45	C9	DQA1_13	
VMA_DQ46	F9	DQA1_14	
VMA_DQ47	D8	DQA1_15	
VMA_DQ48	E7	DQA1_16	
VMA_DQ49	A7	DQA1_17	
VMA_DQ50	C7	DQA1_18	
VMA_DQ51	F7	DQA1_19	
VMA_DQ52	A5	DQA1_20	
VMA_DQ53	E5	DQA1_21	
VMA_DQ54	C3	DQA1_22	
VMA_DQ55	E1	DQA1_23	
VMA_DQ56	G7	DQA1_24	
VMA_DQ57	G6	DQA1_25	
VMA_DQ58	G1	DQA1_26	
VMA_DQ59	G3	DQA1_27	
VMA_DQ60	J6	DQA1_28	
VMA_DQ61	J1	DQA1_29	
VMA_DQ62	J3	DQA1_30	
VMA_DQ63	J5	DQA1_31	
	K26	MVREFDA	
	J26	MVREFSA	
	J25	NC	
VMA_CALRP0	K25	MEM_CALRP0	
DRAM_RST	L10	DRAM_RST	
CLKTESTA	K8	CLKTESTA	
CLKTESTB	L7	CLKTESTB	

MAA0_0	K17	VMA_MA0	
MAA0_1	J20	VMA_MA1	
MAA0_2	H23	VMA_MA2	
MAA0_3	G23	VMA_MA3	
MAA0_4	G24	VMA_MA4	
MAA0_5	H24	VMA_MA5	
MAA0_6	J19	VMA_MA6	
MAA0_7	K19	VMA_MA7	
MAA0_8	G20	VMA_MA13	
MAA0_9	L17	VMA_MA15	
MAA1_0	J14	VMA_MA8	
MAA1_1	K14	VMA_MA9	
MAA1_2	J11	VMA_MA10	
MAA1_3	J13	VMA_MA11	
MAA1_4	H11	VMA_MA12	
MAA1_5	G11	VMA_BA2	
MAA1_6	J16	VMA_BA0	
MAA1_7	L15	VMA_BA1	
MMA1_8	G14	VMA_MA14	
MAA1_9	L16		
WCKA0_0	E32	VMA_DM0	
WCKA0B_0	E30	VMA_DM1	
WCKA0_1	A21	VMA_DM2	
WCKA0B_1	C21	VMA_DM3	
WCKA1_0	E13	VMA_DM4	
WCKA1B_0	D12	VMA_DM5	
WCKA1_1	E3	VMA_DM6	
WCKA1B_1	F4	VMA_DM7	
EDCA0_0	H28	VMA_RDQS0	
EDCA0_1	C27	VMA_RDQS1	
EDCA0_2	A23	VMA_RDQS2	
EDCA0_3	E19	VMA_RDQS3	
EDCA1_0	E15	VMA_RDQS4	
EDCA1_1	D10	VMA_RDQS5	
EDCA1_2	D6	VMA_RDQS6	
EDCA1_3	G5	VMA_RDQS7	
DDBIA0_0	H27	VMA_WDQS0	
DDBIA0_1	A27	VMA_WDQS1	
DDBIA0_2	C23	VMA_WDQS2	
DDBIA0_3	C19	VMA_WDQS3	
DDBIA1_0	C15	VMA_WDQS4	
DDBIA1_1	E9	VMA_WDQS5	
DDBIA1_2	C5	VMA_WDQS6	
DDBIA1_3	H4	VMA_WDQS7	
ADBIAO	L18	VMA_ODT0	
ADBIA1	K16	VMA_ODT1	
CLKA0	H26	VMA_CLK0	
CLKA0B	H25	VMA_CLK0#	
CLKA1	G9	VMA_CLK1	
CLKA1B	H9	VMA_CLK1#	
RASA0B	G22	VMA_RAS0#	
RASA1B	G17	VMA_RAS1#	
CASA0B	G19	VMA_CAS0#	
CASA1B	G16	VMA_CAS1#	
CSA0B_0	H22	VMA_CS0#	
CSA0B_1	J22		
CSA1B_0	G13	VMA_CS1#	
CSA1B_1	K13		
CKEA0	K20	VMA_CKE0	
CKEA1	J17	VMA_CKE1	
WEA0B	G25	VMA_WE0#	
WEA1B	H10	VMA_WE1#	

DIS@EXO/MESO_S3

+1.5V_VGA
R439 DIS@40.2/F_4
MVREFD
C381 DIS@0.1u/25V/X5R_4
R449 DIS@100/F_4
+1.5V_VGA
R424 DIS@40.2/F_4
MVREFS
Rd R458 DIS@120/F_4 VMA_CALRP0
C356 DIS@0.1u/25V/X5R_4
R434 DIS@100/F_4
C385 *DIS@0.1u/25V/X5R_4
C393 *DIS@0.1u/25V/X5R_4
CLKTESTA_C
CLKTESTB_C
R445 *DIS@51.1/F_4
R457 *DIS@51.1/F_4

route 50ohms
single-ended/100ohms diff
and keep short

From GPU
25mm (max) 5mm (max) 25mm (max)
DRAM_RST — R450 DIS@10/F_4 — DRAM_RST_C — R440 DIS@51/F_4 — DRAM_RST_M (21)
R459 DIS@4.99K/F_4
C382 DIS@120P/50V_4

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Quanta Computer Inc.
Project: HP-CRANE

Title: AMD EXO RPO S3_MEM_Interface
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2GB gDDR3L

(19,20,49) +1.5V_VGA

(20) VMA_MA[15..0]
(20) VMA_DM[7..0]
VMA_MA[15..0]
(20) VMA_DQ[63..0]
(20) VMA_WDQS[7..0]
(20) VMA_RDQS[7..0]

U28 / U3 / U27 / U2 — 96-BALL SDRAM DDR3 DIS@MICRON_gDDR3L

(20) VMA_BA0
(20) VMA_BA1
(20) VMA_BA2
(20) VMA_CLK0
(20) VMA_CLK0#
(20) VMA_CKE0
(20) VMA_ODT0
(20) VMA_CS0#
(20) VMA_RAS0#
(20) VMA_CAS0#
(20) VMA_WE0#
(20) DRAM_RST_M

Should be 240 Ohms +-1%
R376 DIS@243/F_4
R25 DIS@243/F_4
R389 DIS@243/F_4
R22 DIS@243/F_4

(20) VMA_CLK1
(20) VMA_CLK1#
(20) VMA_CKE1
(20) VMA_ODT1
(20) VMA_CS1#
(20) VMA_RAS1#
(20) VMA_CAS1#
(20) VMA_WE1#

+1.5V_VGA

R373 DIS@4.99K/F_4
R375 DIS@4.99K/F_4
VREFC_VMA1
C281 DIS@0.1u/25V/X5R_4
R383 DIS@4.99K/F_4
R387 DIS@4.99K/F_4
VREFD_VMA1
C298 DIS@0.1u/25V/X5R_4
R14 DIS@4.99K/F_4
R21 DIS@4.99K/F_4
VREFC_VMA2
C18 DIS@0.1U/10V/X5R_4
R20 DIS@4.99K/F_4
R15 DIS@4.99K/F_4
VREFD_VMA2
C16 DIS@0.1U/10V/X5R_4
R380 DIS@4.99K/F_4
R384 DIS@4.99K/F_4
VREFC_VMA3
C299 DIS@0.1U/10V/X5R_4
R374 DIS@4.99K/F_4
R377 DIS@4.99K/F_4
VREFD_VMA3
C285 DIS@0.1U/10V/X5R_4
R13 DIS@4.99K/F_4
R16 DIS@4.99K/F_4
VREFC_VMA4
C17 DIS@0.1U/10V/X5R_4
R17 DIS@4.99K/F_4
R24 DIS@4.99K/F_4
VREFD_VMA4
C19 DIS@0.1U/10V/X5R_4

VMA_CLK0
R388 DIS@40.2/F_4
VMA_CLK0_COMM
C294 DIS@0.01U/50V/X7R_4
R386 DIS@40.2/F_4
VMA_CLK0#
VMA_CLK1
R36 DIS@40.2/F_4
VMA_CLK1_COMM
C35 DIS@0.01U/50V/X7R_4
R41 DIS@40.2/F_4
VMA_CLK1#

C290 C13 C276 C289 C268 C303 C304 DIS@1U/6.3V/X5R_4 DIS@0.1u/25V/X5R_4 C292 DIS@0.1u/25V/X5R_4
C33 C39 C27 C14 C282 C21 C319 DIS@1U/6.3V/X5R_4 DIS@0.1u/25V/X5R_4 C286 DIS@0.1u/25V/X5R_4
C9 C15 C280 C279 C271 C301 C315 DIS@1U/6.3V/X5R_4 DIS@0.1u/25V/X5R_4 C283 DIS@0.1u/25V/X5R_4
C305 C269 C272 C284 C275 C10 C277 DIS@1U/6.3V/X5R_4 DIS@0.1u/25V/X5R_4 C278 DIS@0.1u/25V/X5R_4
C37 C317 C306 C7 DIS@10U/6.3V_6 DIS@10U/6.3V_6 DIS@10U/6.3V_6 DIS@10U/6.3V_6
C20 C270 C22 C24 C8 C26 C297 C293 DIS@0.1U/10V/X5R_4 DIS@0.1U/25V/X7R_4

Quanta Computer Inc.
Project: HP-CRANE
Title: VRAM_DDR3 BGA96
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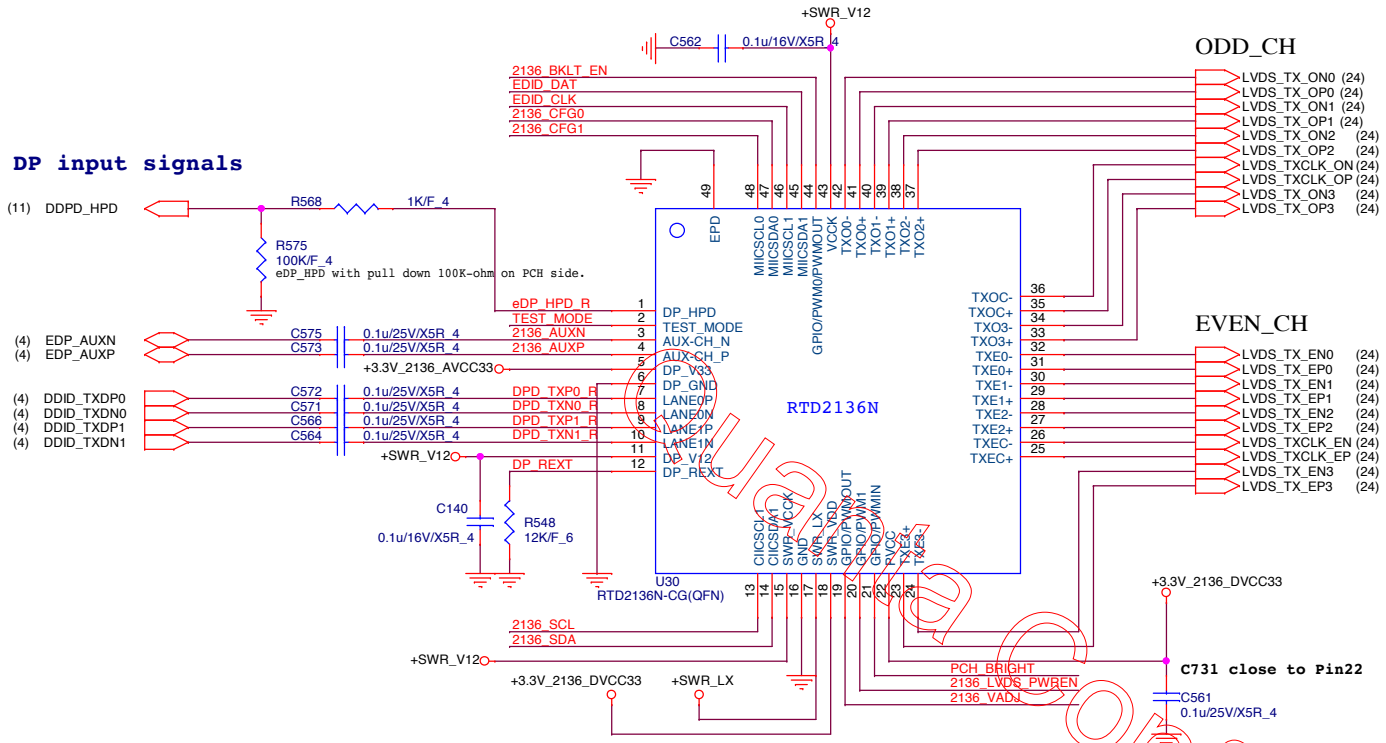
eDP to LVDS (RTD2136N-CG)

(9,10,11,12,13,14,15,23,25,26,27,28,29,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V

DP input signals



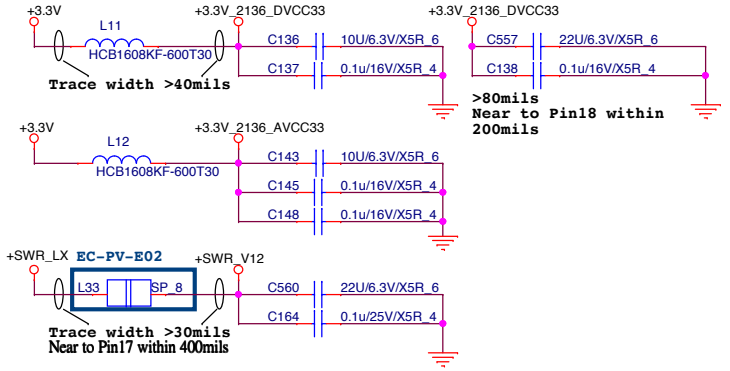
ODD_CH

LVDS_TX_ON0 (24)
LVDS_TX_OP0 (24)
LVDS_TX_ON1 (24)
LVDS_TX_OP1 (24)
LVDS_TX_ON2 (24)
LVDS_TX_OP2 (24)
LVDS_TXCLK_ON (24)
LVDS_TXCLK_OP (24)
LVDS_TX_ON3 (24)
LVDS_TX_OP3 (24)

EVEN_CH

LVDS_TX_EN0 (24)
LVDS_TX_EP0 (24)
LVDS_TX_EN1 (24)
LVDS_TX_EP1 (24)
LVDS_TX_EN2 (24)
LVDS_TX_EP2 (24)
LVDS_TXCLK_EN (24)
LVDS_TXCLK_EP (24)
LVDS_TX_EN3 (24)
LVDS_TX_EP3 (24)

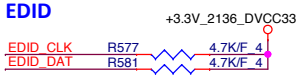
RTD2136N Power



SWR MODE /LDO MODE

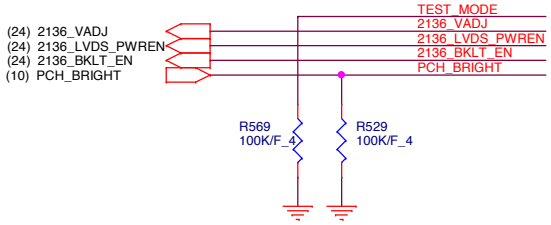
L9	2.2-uH	0 Olm
SWR	Connect	NC
LDO	NC	Connect

EDID



Intel CRB

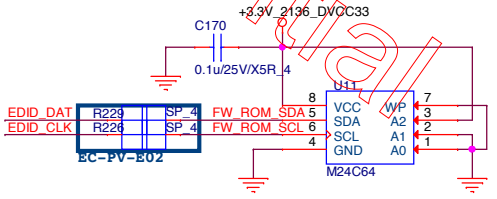
GPIO & TESTing signals



Mode select

2136_CFG1 (PIN48)	2136_CFG0 (PIN47) = 0	2136_CFG0 (PIN47) = 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

EEPROM

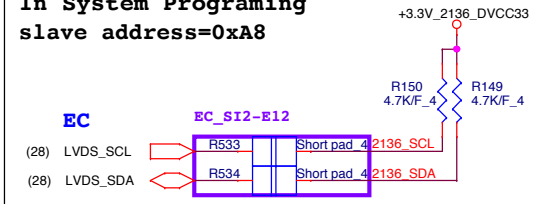


1- EEPROM with a size 8K-Byte

2- EEPROM device should be 2-byte addressing device

3- Slave address should configure as 0xA8

In System Programing slave address=0xA8



HP Restricted Secret

Quanta Computer Inc.

Project: HP-CRANE

Title		
eDP-LVDS_RTD2136N		
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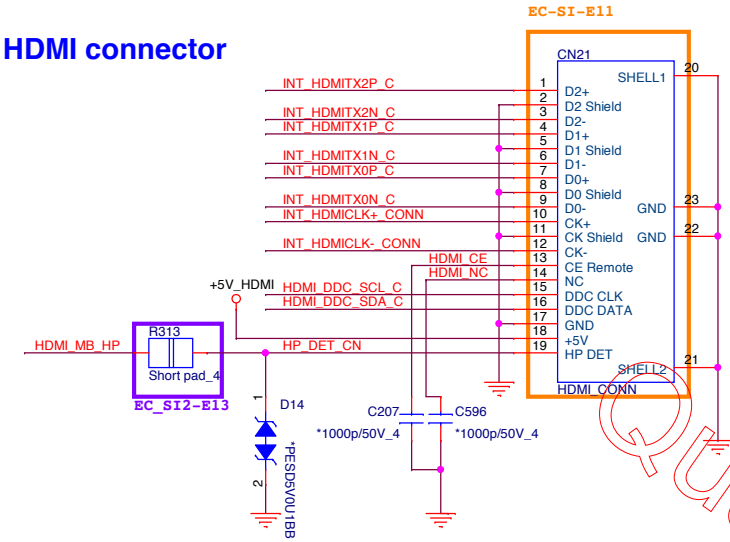
HDMI

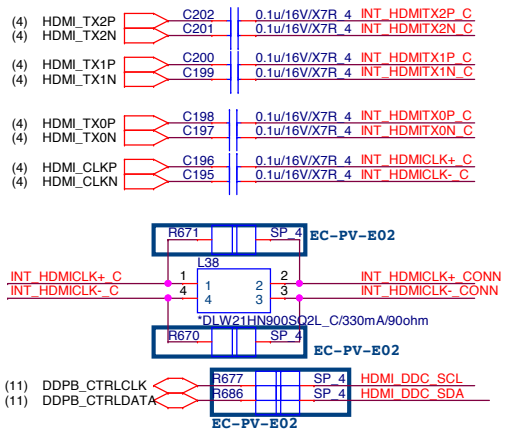
(9,10,11,12,13,14,15,22,25,26,27,28,29,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V
(24,25,29,32,35,42,43,44,45,46,48,49,50) +5V

23

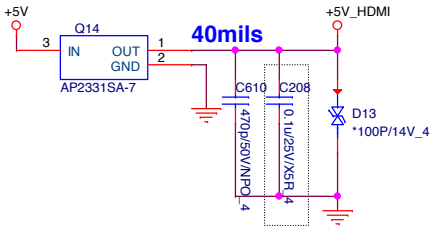
HDMI connector



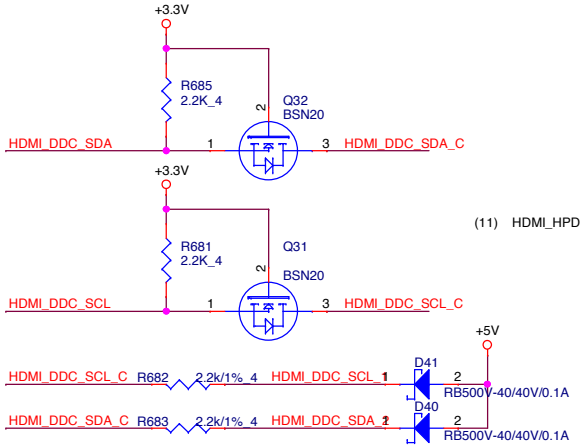
HDMI INTERFACE



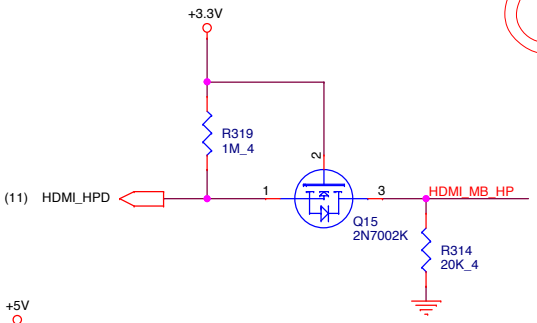
HDMI POWER SUPPLY



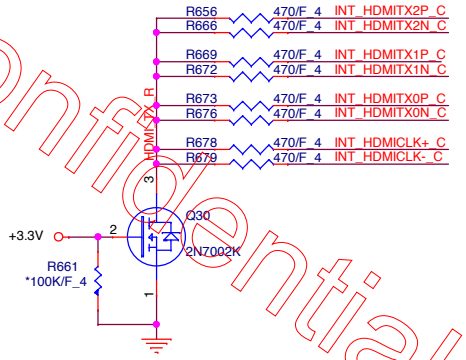
HDMI DDC



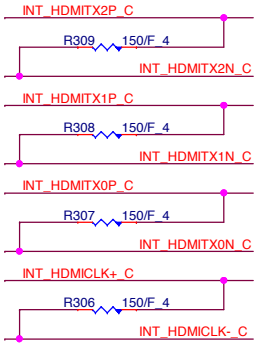
HDMI-detect



HDMI LEVEL SHIFT

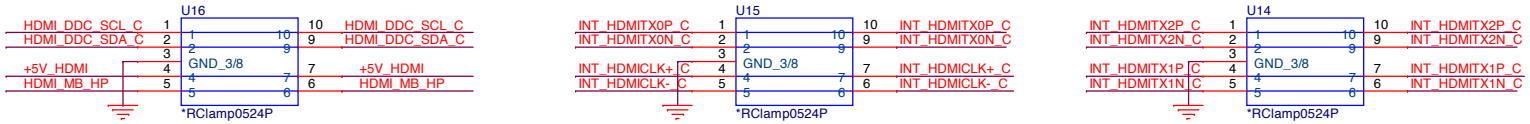


HDMI EMI (EMC)



ESD reserve for HDMI

Layout Notes:
Place decoupling CAPs close to Connector



HP Restricted Secret

Quanta Computer Inc.

Project: HP-CRANE

Title: HDMI		
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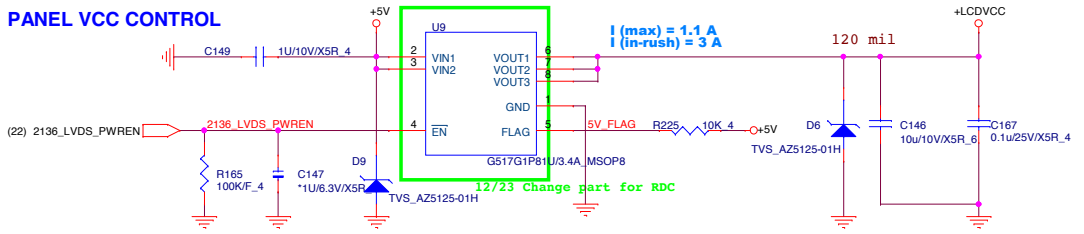
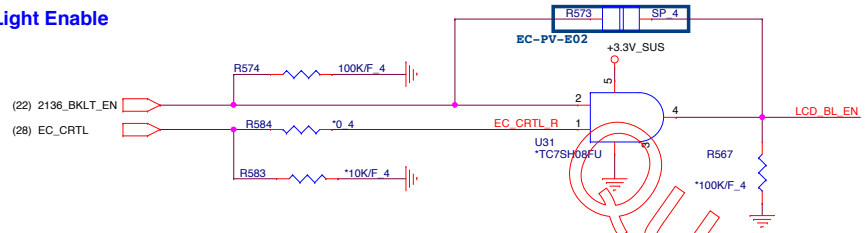
LED PANEL

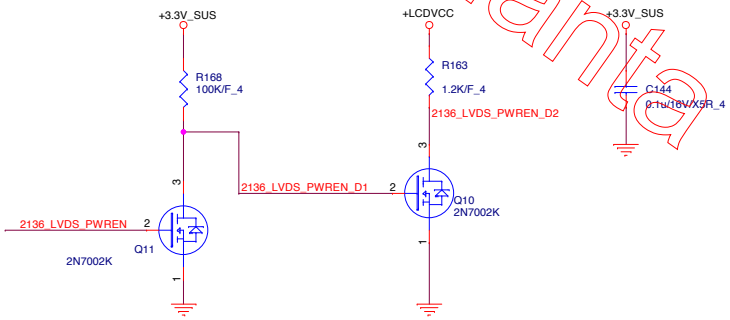
PANEL VCC CONTROL



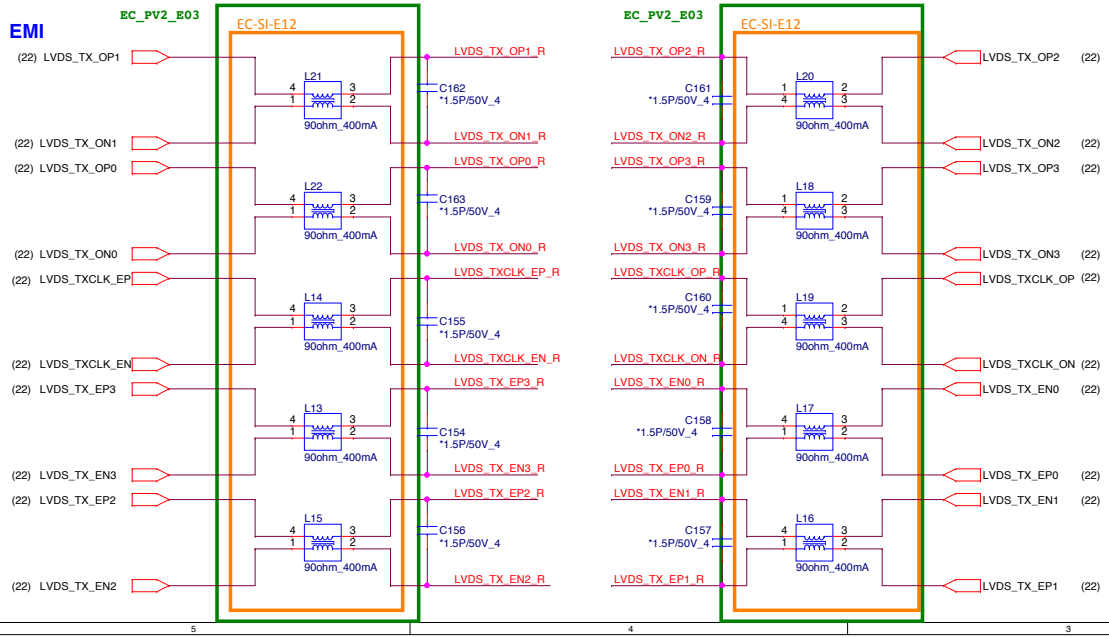
BackLight Enable



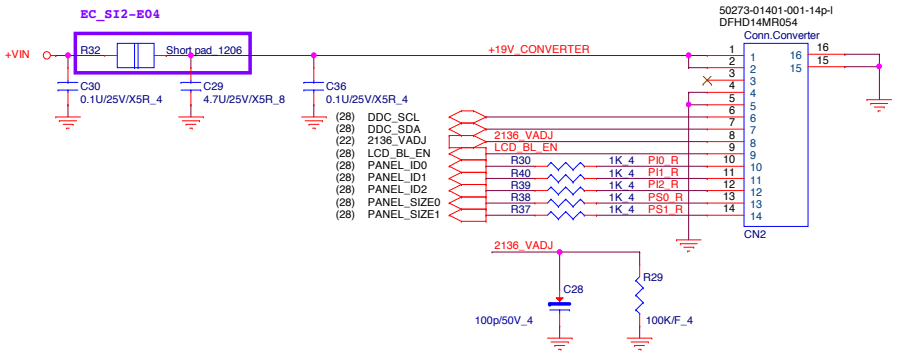
LCDVCC Discharge Circuit



EMI



CONVERTER CONN



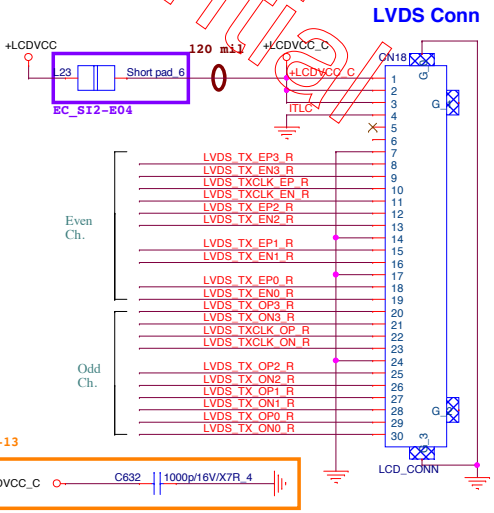
PANEL_Size Table

PANEL_Size[1:0]	Size
10	23"
11	21.5
01	27

PANEL_ID Table

PANEL_ID[2:0]	Panel model
000	Reserve
001	SDC LTM215HL01_H02
010	SDC LTM230HL08 LTM215HL01_H01
011	Reserve
100	LGD LM230WF3 LM215WF3
101	Reserve
110	Reserve
111	No Connect

LVDS Conn



Quanta Computer Inc.

Project: HP-CRANE

Title: Panel (Control).LVDS-Conn.

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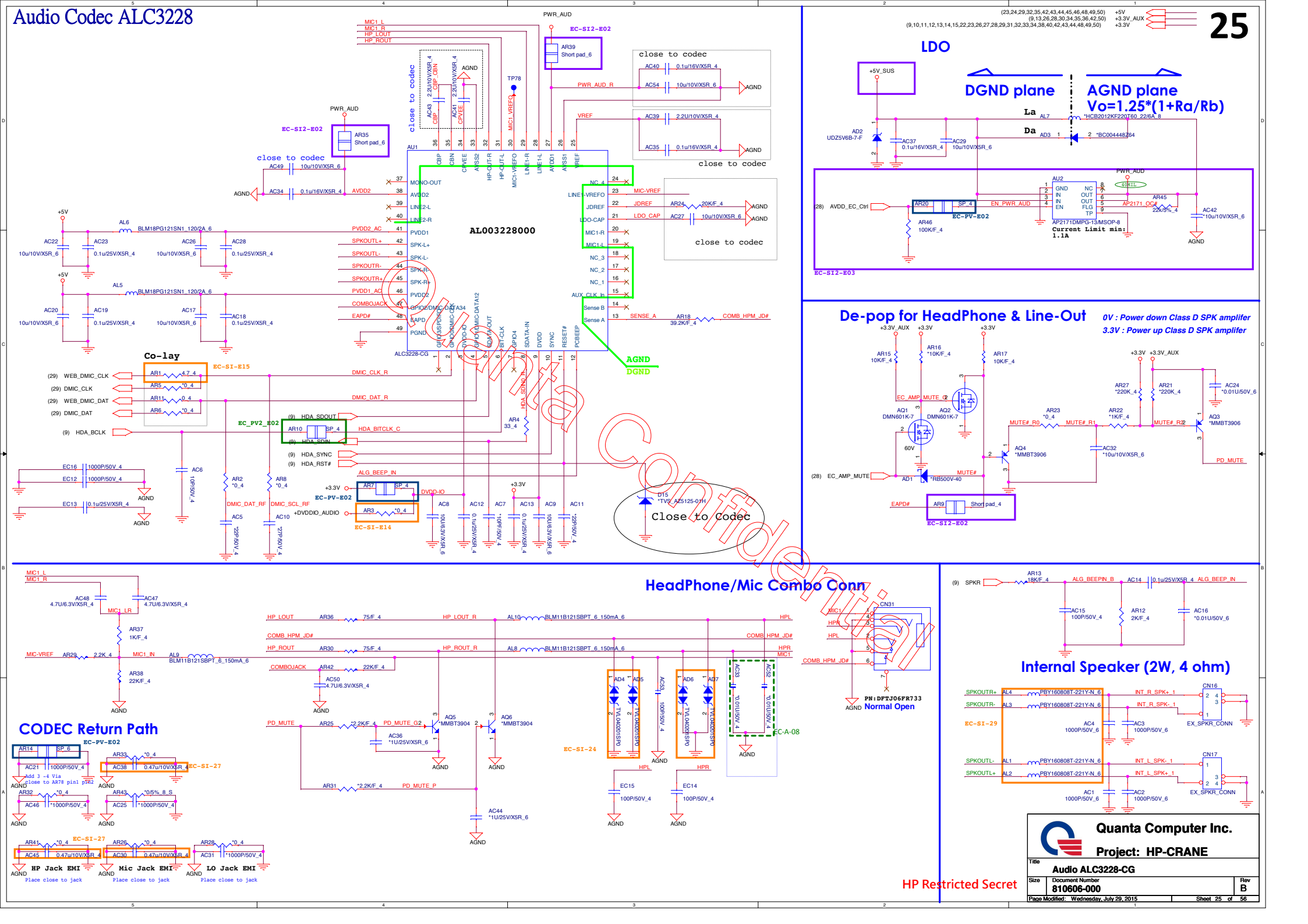
Audio Codec ALC3228



LAN (RTL8161GSH) 10/100/1000

(9,10,11,12,13,14,15,22,23,25,27,28,29,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V
(9,13,25,28,30,34,35,36,42,50) +3.3V_AUX

R412 value should be 2.49K (1%) for all application.

R696 2.49K/F_4 RSET +3.3V_LAN

U39 RTL8161GSH-CG

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-

PCIE_WAKE# R344 1K/F_4 +3.3V_LAN
CLKREQB R690 10K/F_4 +3.3V

EMI Suggest
LAN_LED0# C630 *220P/50V/X7R_4
LED1/EEDO C631 *220P/50V/X7R_4
LED2/EESK C629 *220P/50V/X7R_4

R692 1K/F_4
R693 *15K/F_4

C620 0.1u/25V/X5R_4 PCIE_GLAN_RX_N (10)
C619 0.1u/25V/X5R_4 PCIE_GLAN_RX_P (10)

C618 0.1u/25V/X5R_4 CLK_PCIE_LAN_N (12)
C616 0.1u/25V/X5R_4 CLK_PCIE_LAN_P (12)
PCIE_GLAN_TX_N (10)
PCIE_GLAN_TX_P (10)

(12) LAN_PCIE_CLKREQ# R342 *0/5%_4 CLKREQB

BK: reserve

X'tal 25MHz

C256 10P/50V_4 25MCLKX1
Y1 XTAL_25MHz_30ppm BG625000085
C257 10P/50V_4 25M_R R360 SP_4 25MCLKX2
EC-PV-E02

LAN_RST# U20 TC7SH08FU PLTRST_N (10,27,33)

PCIE_WAKE# R354 *0_4 Q16 DDTC144EUA PCH_WAKE# (9,31)

3V_LAN

+3.3V_AUX Q18 G5243AT11U
R358 *10K/F_4
(28) LAN_PWR_ON
C252 *0.1u/25V/X5R_4
C254 0.1u/25V/X5R_4
120mil
R355 *0_6
+3.3V_SUS
C248 *0.1u/25V/X5R_4

EVDD10/AVDD33_REG trace width >40mils

EC-PV-E02
+3.3V_LAN R356 SP_6 VDD33_REG

C628 *4.7U/6.3V/X5R_4 C626 0.1u/25V/X5R_4 — Close to Pin32
C615 *4.7U/6.3V/X5R_4 C617 0.1u/25V/X5R_4 — Close to Pin11
C250 0.1u/25V/X5R_4 C251 4.7U/6.3V/X5R_4 — Close to Pin23

EVDD10/N780946/REGOUT trace width >60mils

VDD10
C627 0.1u/25V/X5R_4
C244 0.1u/25V/X5R_4
C623 0.1u/25V/X5R_4
C621 0.1u/25V/X5R_4
Close to PIN3, 8, 22, 30

C624 0.1u/25V/X5R_4
C245 1U/6.3V/X5R_4
L40 4.7uH REGOUT
C253 4.7U/6.3V/X5R_4
C625 *0.1u/25V/X5R_4
C367,C368 Close to PIN22

LAN Conn

U21 NS892407
NS892407_TCT
MDI0+ R353 1/F_6 MDI0+_R
MDI0- R350 1/F_6 MDI0-_R
MDI1+ R347 1/F_6 MDI1+_R
MDI1- R341 1/F_6 MDI1-_R
MDI2+ R338 1/F_6 MDI2+_R
MDI2- R335 1/F_6 MDI2-_R
MDI3+ R330 1/F_6 MDI3+_R
MDI3- R325 1/F_6 MDI3-_R

TXCT0 10MIL R694 75/F_8 NS892407_MCT
RJ45-TX0+ IN0 10MIL
RJ45-TX0-
TXCT1 10MIL R691 75/F_8
RJ45-TX1+ IN1 10MIL
RJ45-TX1-
TXCT2 10MIL R689 75/F_8
RJ45-TX2+ IN2 10MIL
RJ45-TX2-
TXCT3 10MIL R688 75/F_8
RJ45-TX3+ IN3 10MIL 10MIL
RJ45-TX3-

15MIL
C614 10P/3KV_1808
15MIL
LANGND

L39 *BLM8SG370TN1D(70_4A)_6
R695 *0_6
C622 0.1U/50V/X7R_6

U19 TVL ST23 04 AD0
MDI2+ MDI2- MDI3+ MDI3- +3.3V_LAN

U22 TVL ST23 04 AD0
MDI0+ MDI0- MDI1+ MDI1- +3.3V_LAN

Q34 BS4202N-C
Q33 BS4202N-C
TXCT1 TXCT0 TXCT3 TXCT2 LANGND

EC-PV-E02
R312 SP_8
R667 SP_8
L24 HCB1608KF-221T20
C231 0.1U/50V/X7R_6
C219 *0.1U/25V/X5R_4
C249 *0.1U/25V/X5R_4
LANGND

EC-A-09
+3.3V_LAN R668 332/F_4
EC-SI-28
C593 1000P/50V_4
C204 1000P/50V_4
D37 TVS_AZ5125-01H
D12 TVS_AZ5125-01H
LANGND

CN26 RJ45-CONN
LED2/EESK 1000M_LED_R
RJ45-TX3- RJ45-TX3+ RJ45-TX1- RJ45-TX2- RJ45-TX2+ RJ45-TX1+ RJ45-TX0- RJ45-TX0+
NC/3- NC/3+ RX-/1- NC/2- NC/2+ RX+/1+ TX-/0- TX+/0+ G- G+
GND1 13 LANGND

EC-A-09
LED1/EEDO R311 332/F_4 LED1_R
LAN_LED0#
EC-SI-28
C203 1000P/50V_4
C592 1000P/50V_4
D11 TVS_AZ5125-01H
LANGND

Quanta Computer Inc.
Project: HP-CRANE

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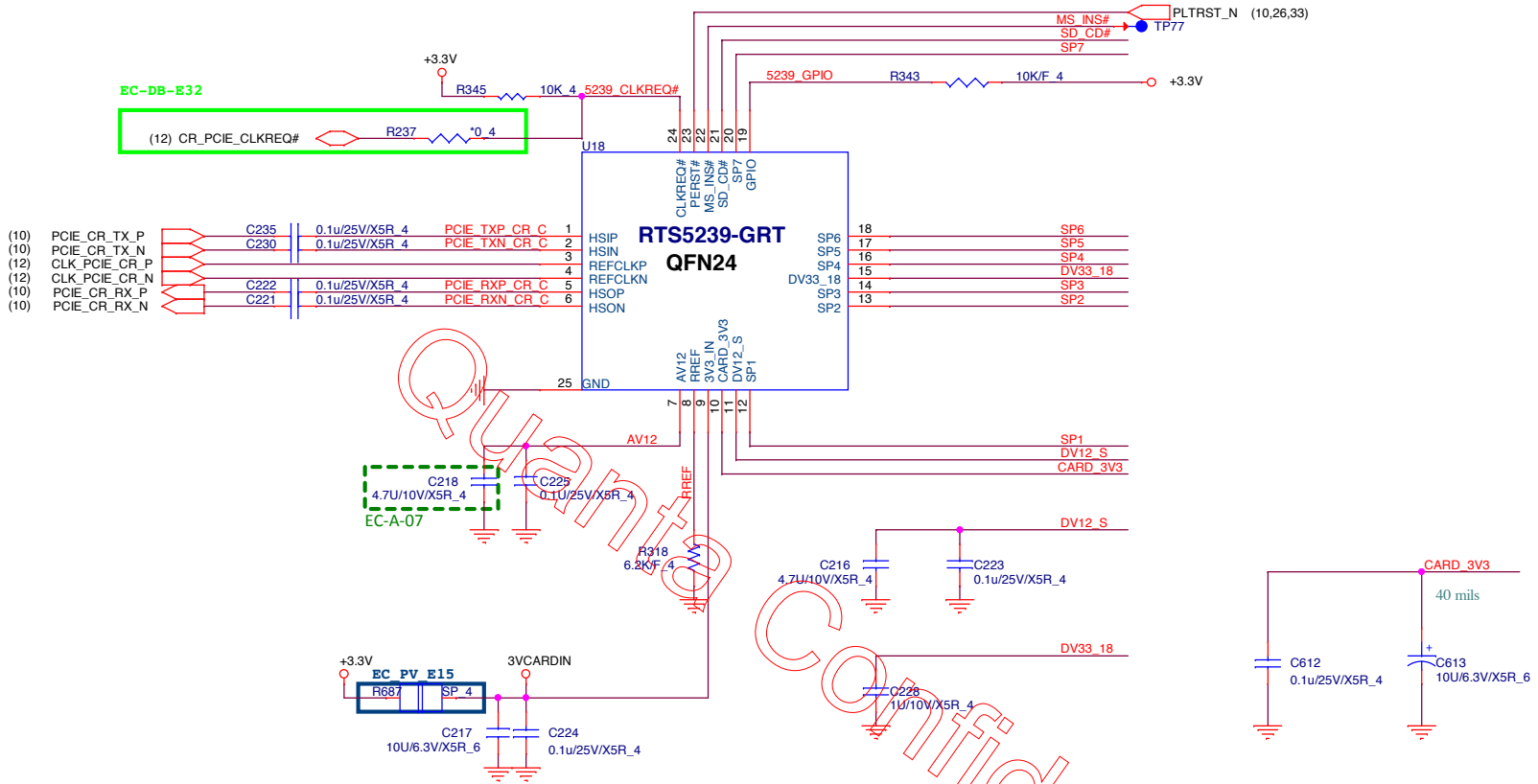
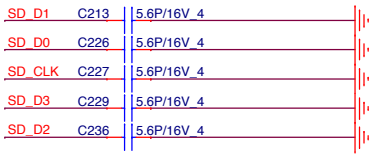
CARD READER RTD5239-GRT

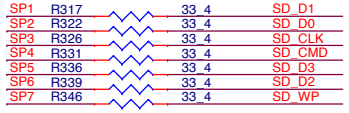
(9,10,11,12,13,14,15,22,23,25,26,28,29,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V



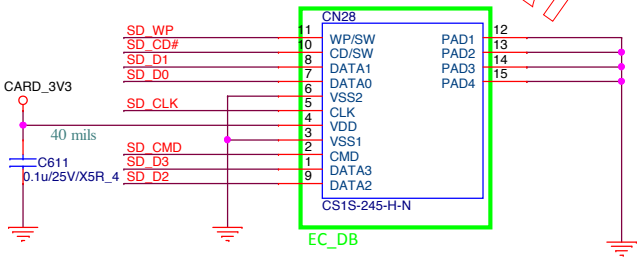
EMI



SD damping resistor



SD connector



HP Restricted Secret

Quanta Computer Inc.

Project: HP-CRANE

Title: Card Reader (RTS5239)		
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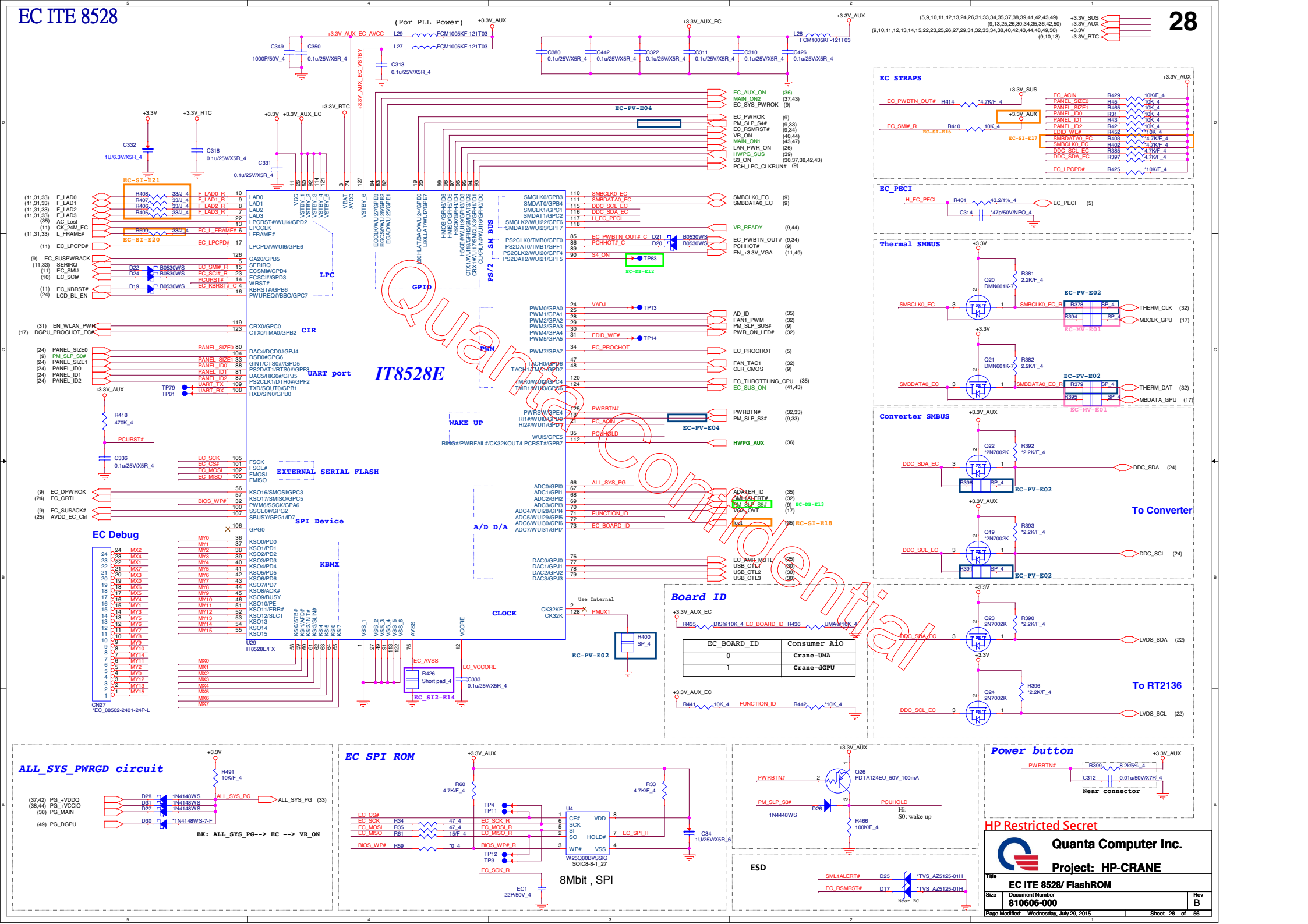
EC ITE 8528



Quanta Computer Inc.	
Project: HP-CRANE	
Title	EC ITE 8528/ FlashROM
Size	Document Number: 810606-000
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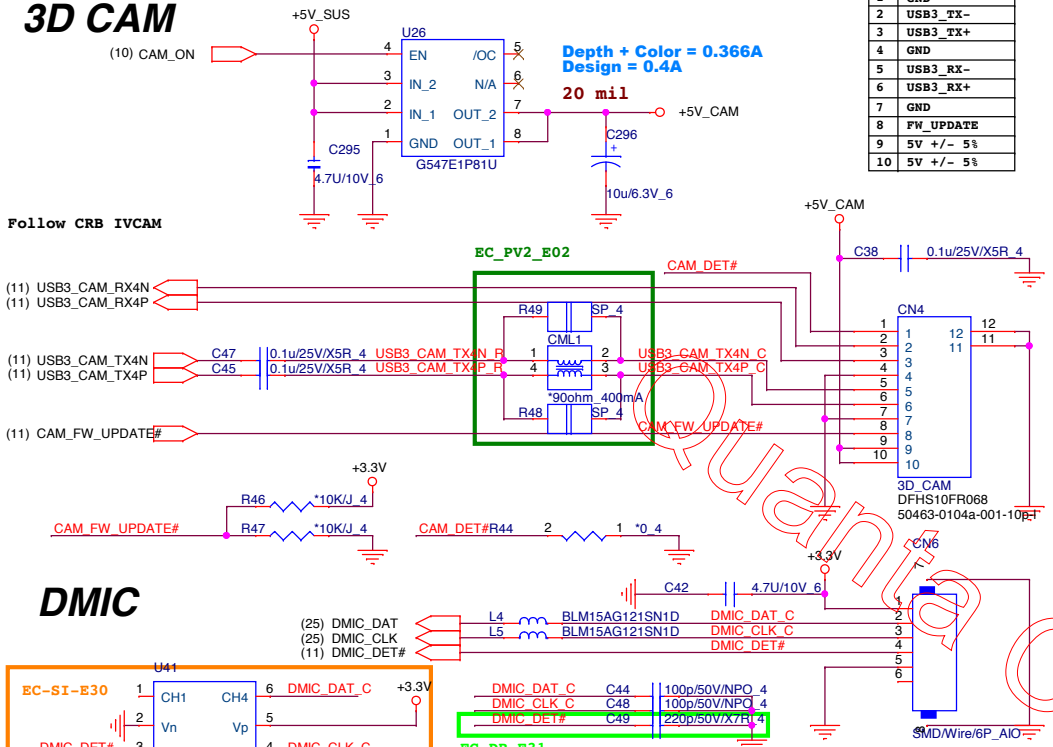
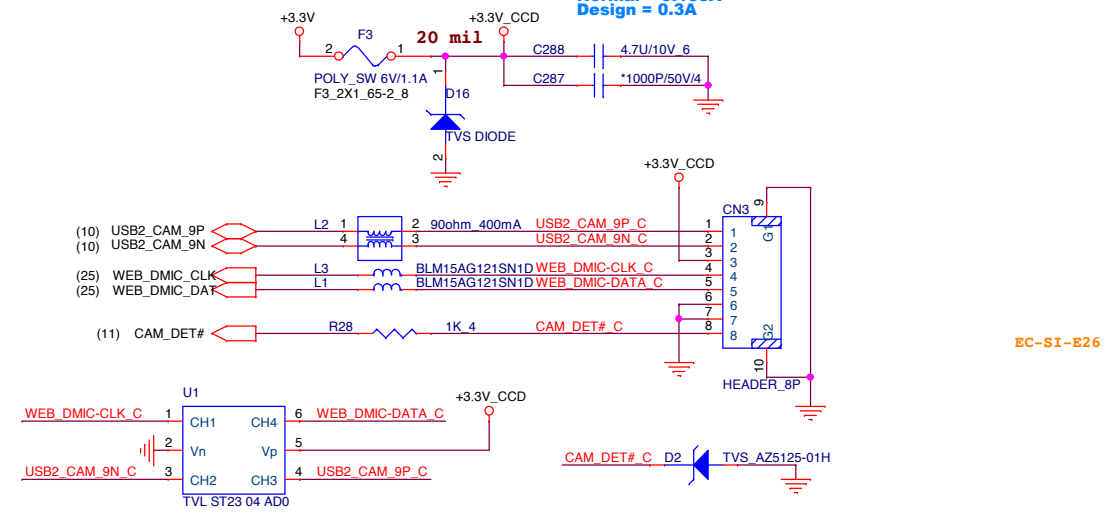
(Optional 1: 3DCAM+DMIC)

3D CAM



DMIC

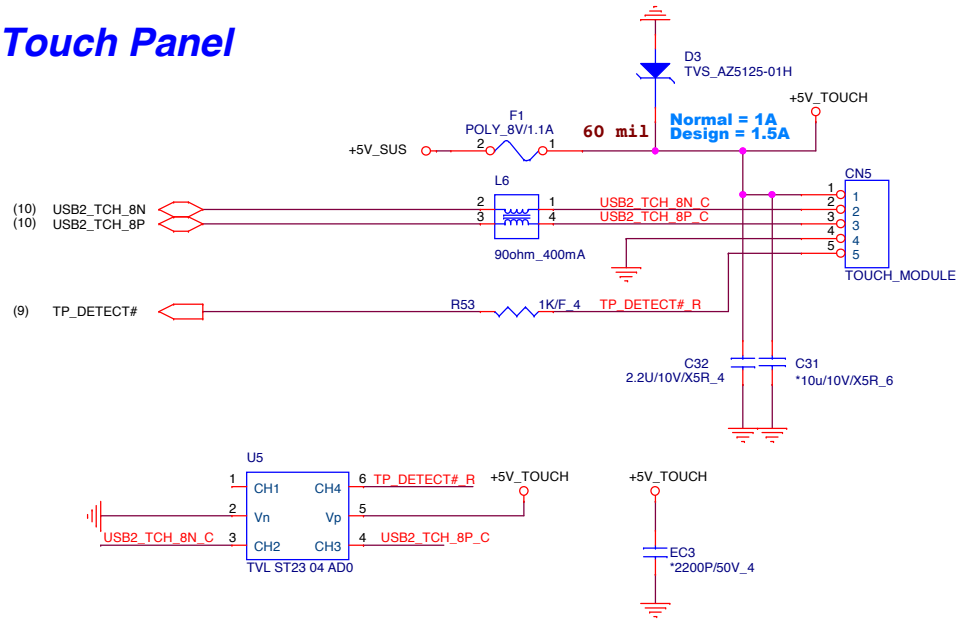
(Optional 2: WEBCAM+DMIC)



3D CAM Module	
#	Description
1	GND
2	USB3_TX-
3	USB3_TX+
4	GND
5	USB3_RX-
6	USB3_RX+
7	GND
8	FW_UPDATE
9	5V +/- 5%
10	5V +/- 5%

(25,30,32,35,37,39,40,41,42,43,48,49) +5V_SUS
(30,36,42) +5V_AUX
(9,10,11,12,13,14,15,22,23,25,26,27,28,31,32,33,34,38,40,42,43,44,48,49,50) +3.3V
(23,24,25,32,35,42,43,44,45,46,48,49,50) +5V

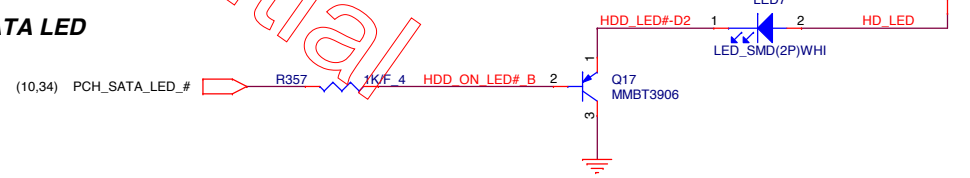
Touch Panel



LEDs

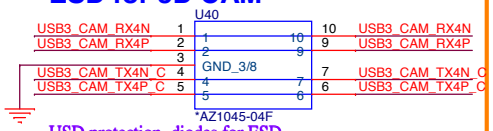
DC_IN LED

SATA LED



HP Restricted Secret

ESD for 3D CAM



USD protection diodes for ESD.
as close as possible to USB connector pins.

Quanta Computer Inc.

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Title: eDP-LVDS_RTD2136N

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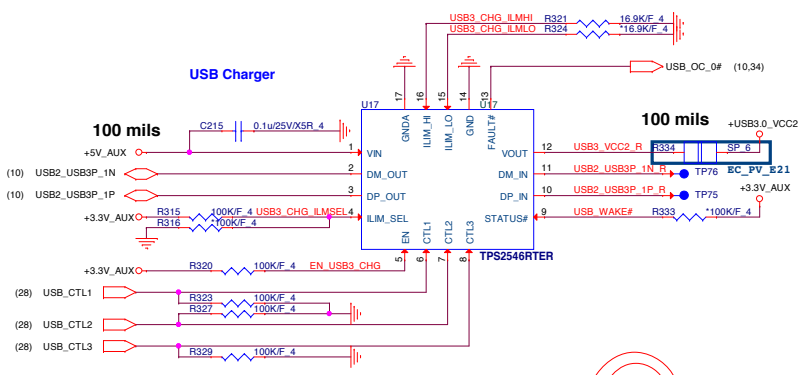
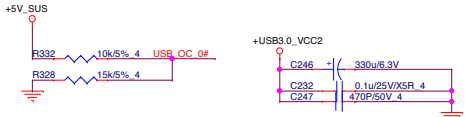
USB PORT

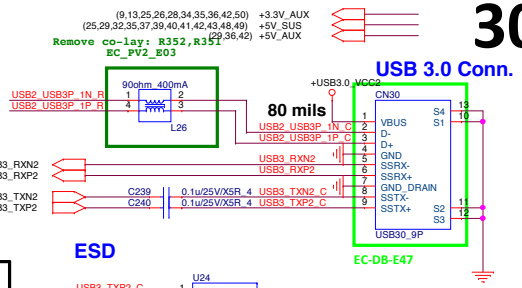
USB3.0 Charging Port



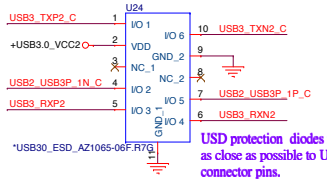
SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLDS	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS	0	0	1	1



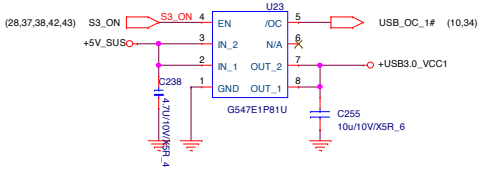


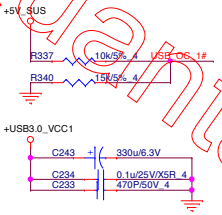
ESD



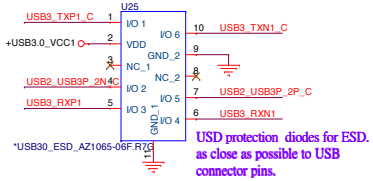
USB3.0 PORT

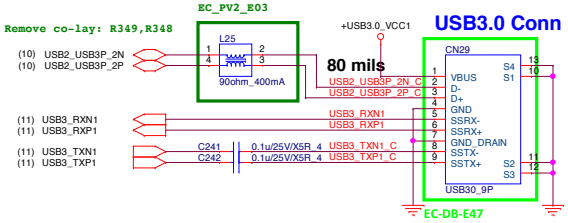
USB3.0 Power Switch





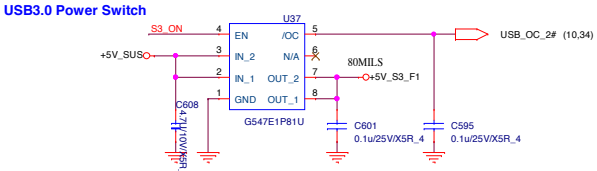
ESD

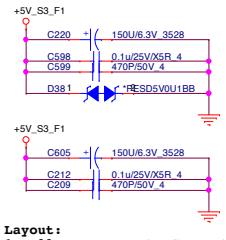




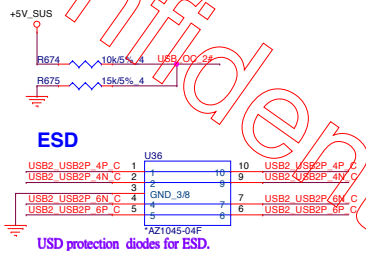
USB2.0 X 2

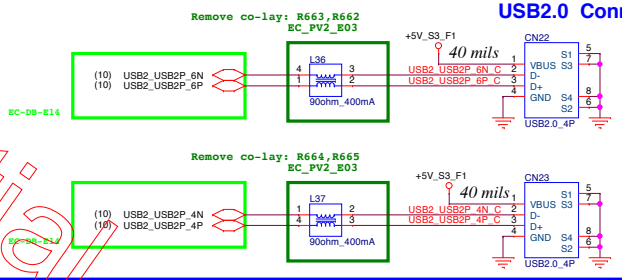
USB3.0 Power Switch





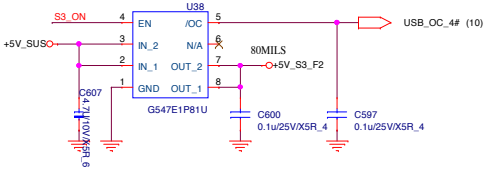
Layout:
1. All caps Near to Connector
2. Place D40 near CN21 and CN22

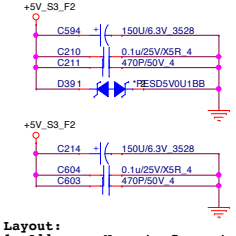




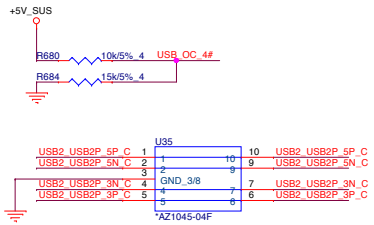
USB2.0 X 2

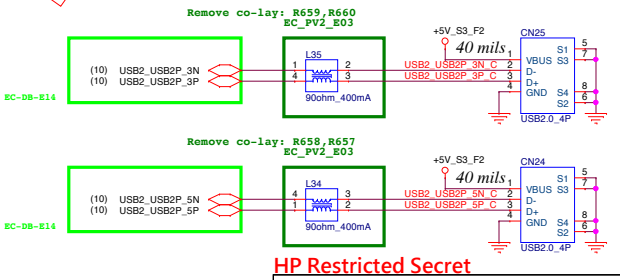
USB3.0 Power Switch





Layout:
1. All caps Near to Connector
2. Place D41 near CN23 and CN24





Quanta Computer Inc.
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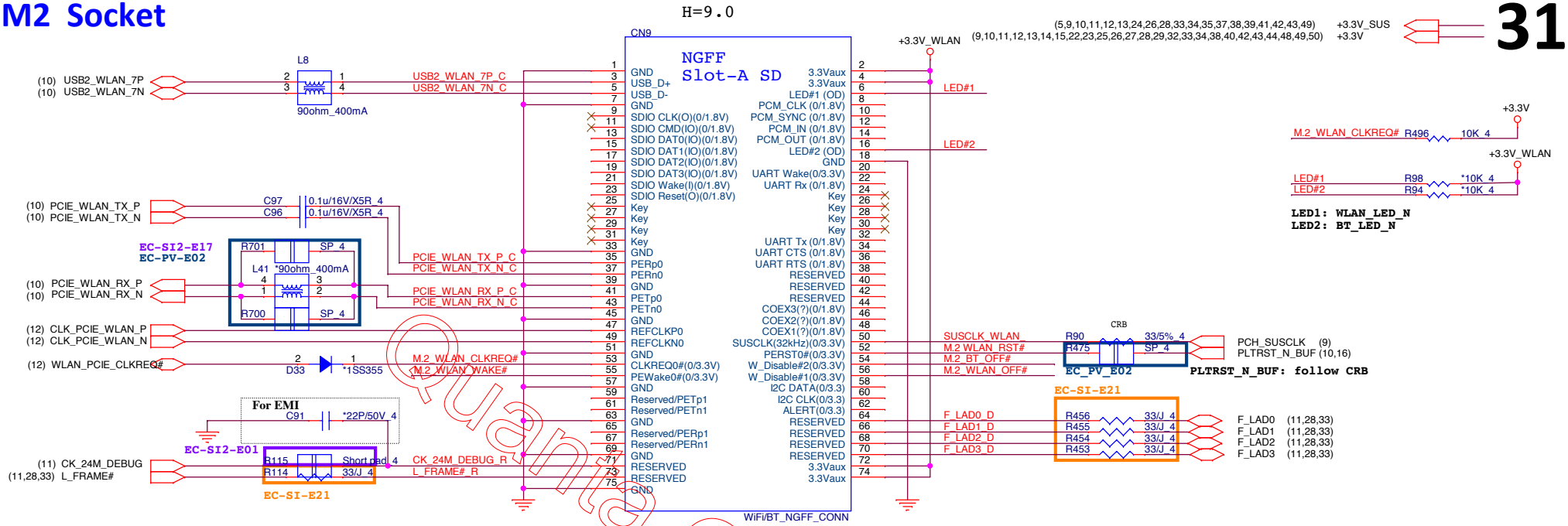
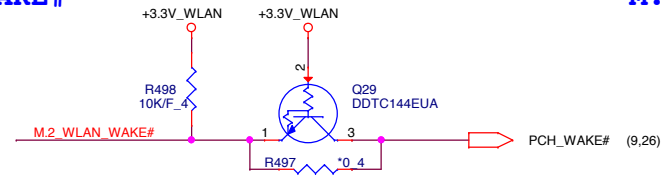
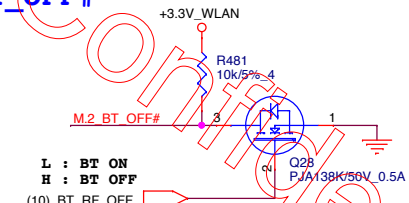
NGFF M2 Socket



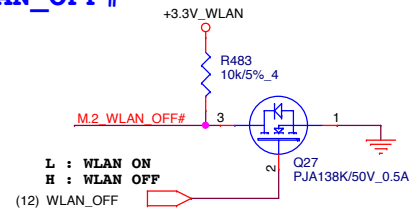
M.2 WLAN WAKE#



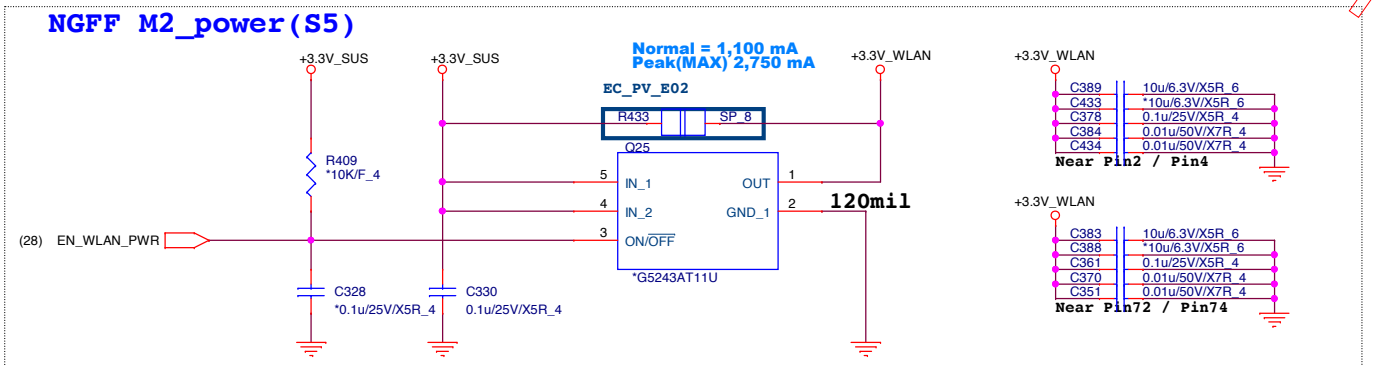
M.2_BT_OFF#



M.2_WLAN_OFF#



NGFF M2_power(S5)



Quanta Computer Inc.

Project: HP-CRANE

Title	NGFF M.2 WLAN	
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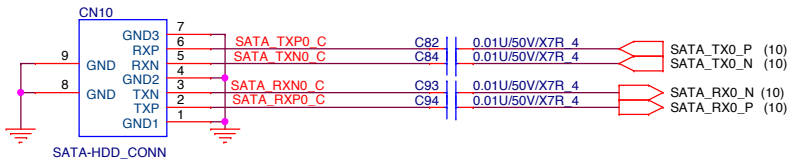
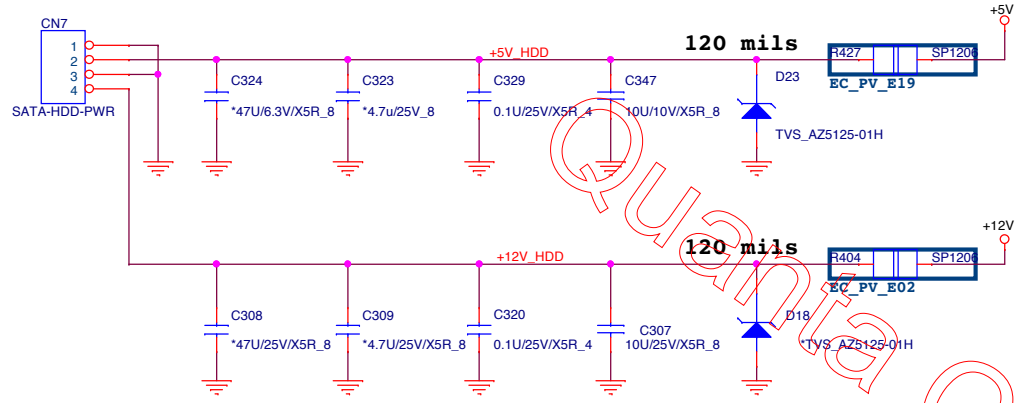
SATA HDD

HDD SATA Conn.

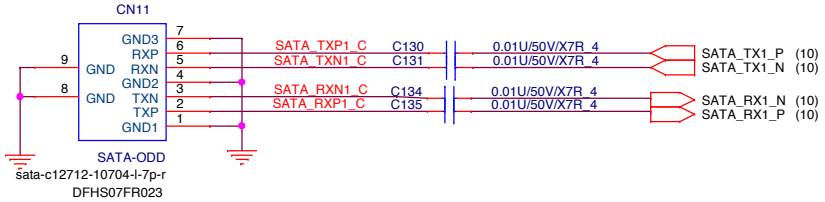


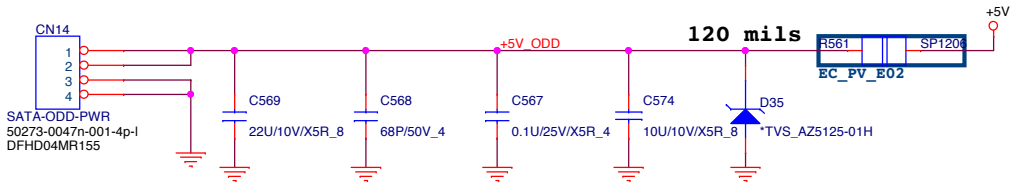
DIP_H type



SATA ODD

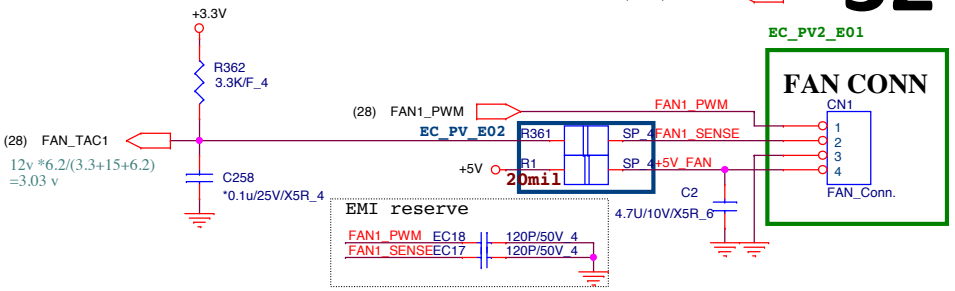
ODD SATA Conn.



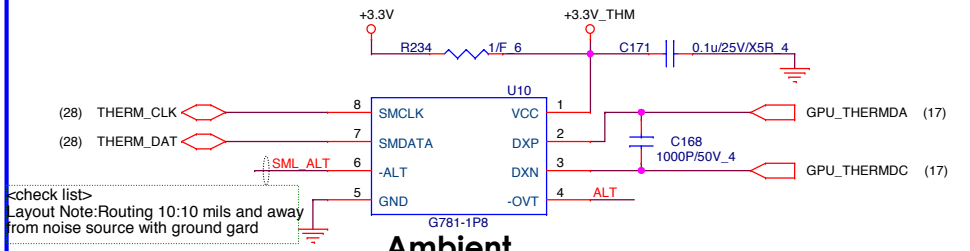


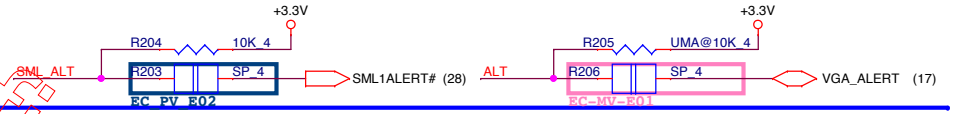
SYSTEM FAN

(9,10,11,12,13,14,15,22,23,25,26,27,28,29,31,33,34,38,40,42,43,44,48,49,50) +3.3V
(25,29,30,35,37,39,40,41,42,43,48,49) +5V_SUS
(23,24,25,29,35,42,43,44,45,46,48,49,50) +5V
(47,50) +12V

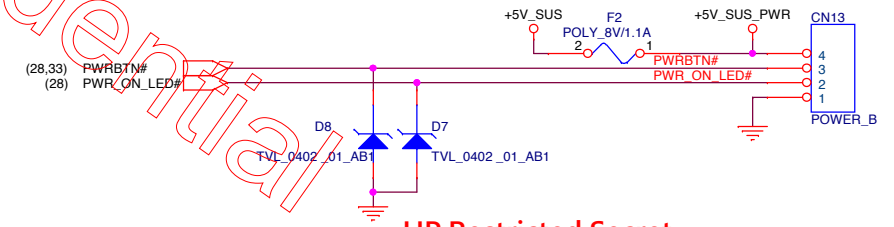


THERMAL SENSOR



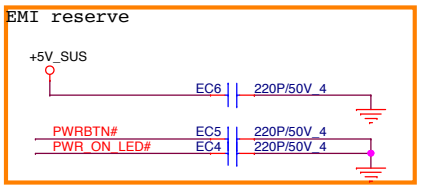


Power Button.



HP Restricted Secret

EC-SI-E19



Quanta Computer Inc.

Project: HP-CRANE

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FAN/HDD/ODD/HDD CONN.		
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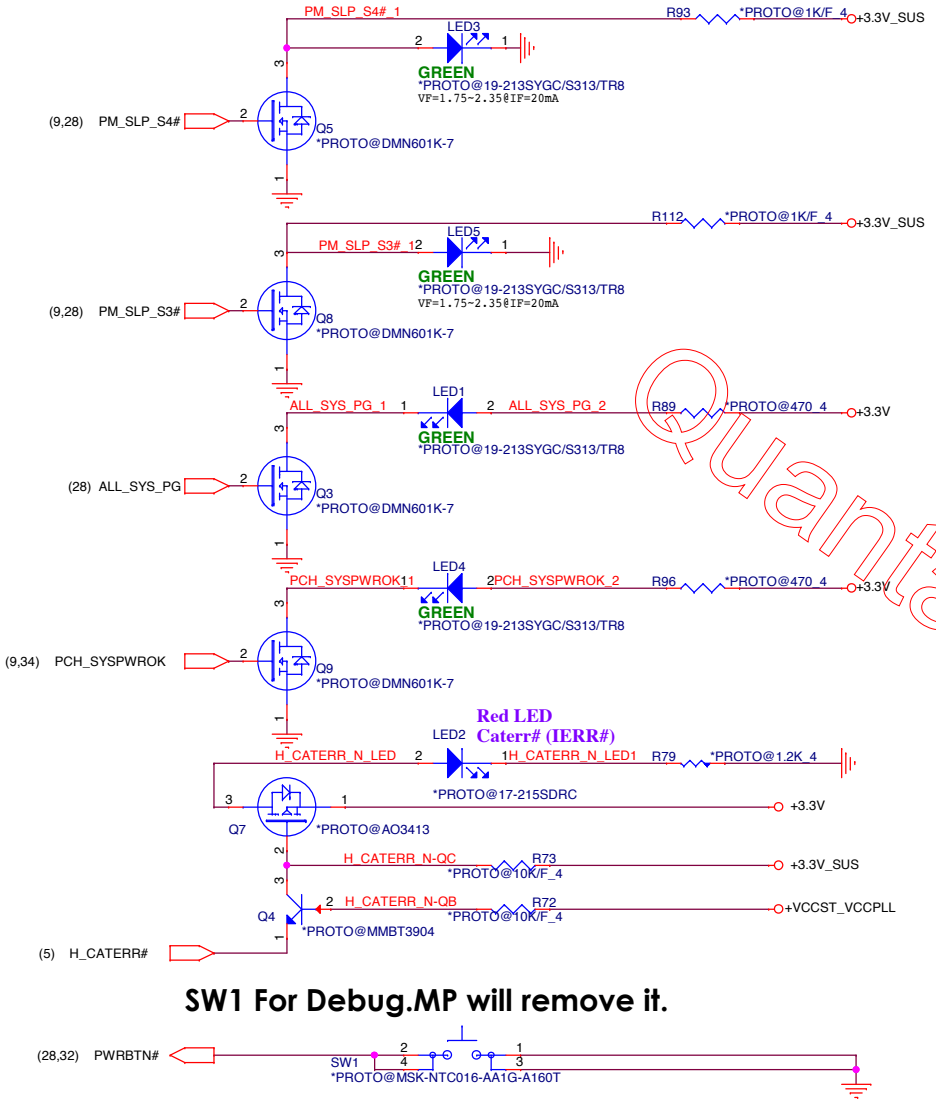
PCA debug LED requirement:



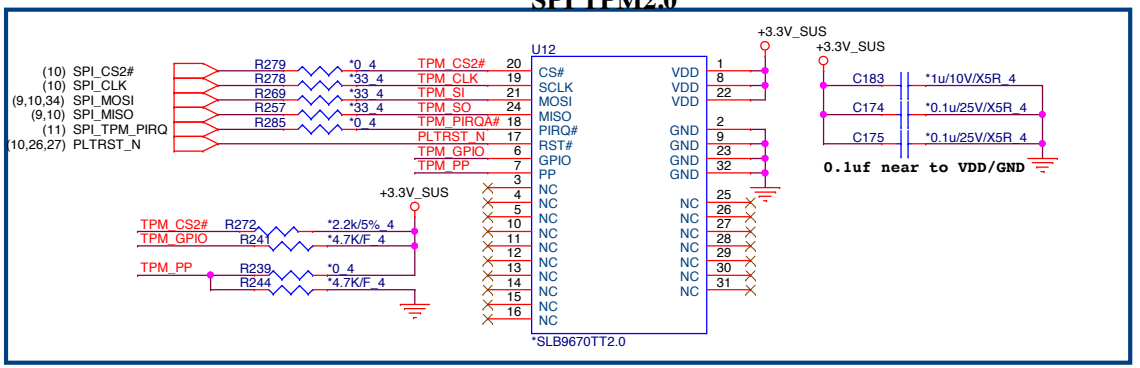
SW1 For Debug.MP will remove it.

TPM2.0

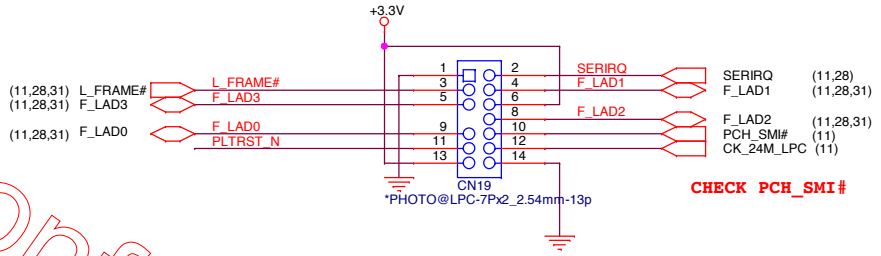
(5,9,10,11,12,13,24,26,28,31,34,35,37,38,39,41,42,43,49) +3.3V_SUS
(9,10,11,12,13,14,15,22,23,25,26,27,28,29,31,32,34,38,40,42,43,44,48,49,50) +3.3V
(23,24,25,29,32,35,42,43,44,45,46,48,49,50) +5V
(5,7,9,34,42,43,44) +VCCST_VCCPLL

EC_PV_E07

SPI TPM2.0



LPC HEADER



CHECK PCH_SMI#

HP Restricted Secret

Quanta Computer Inc.

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Title: Debug /LPC Header/TPM

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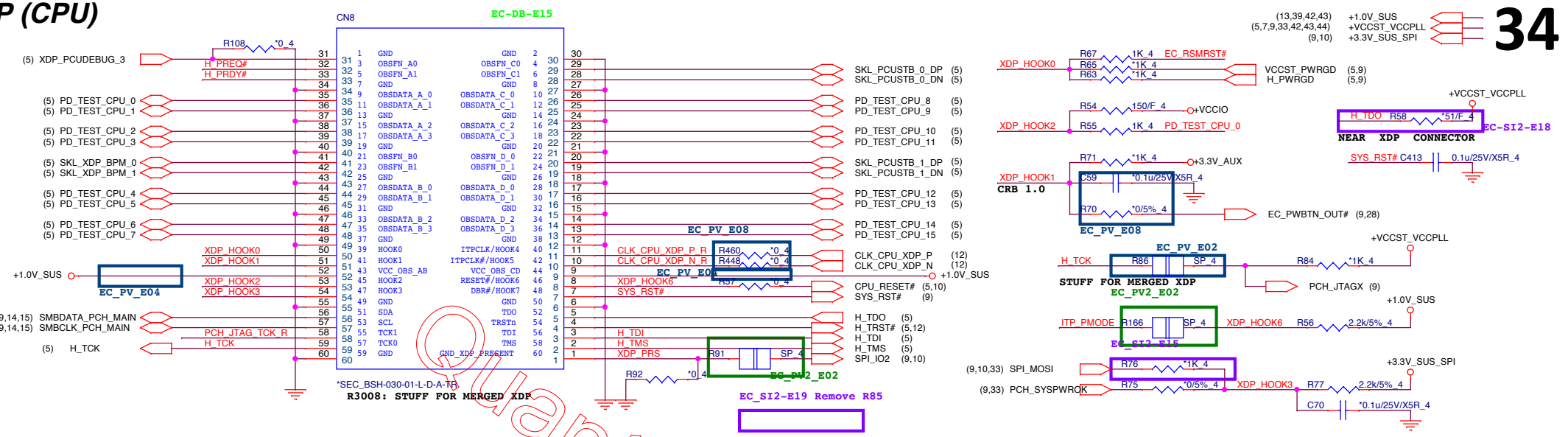
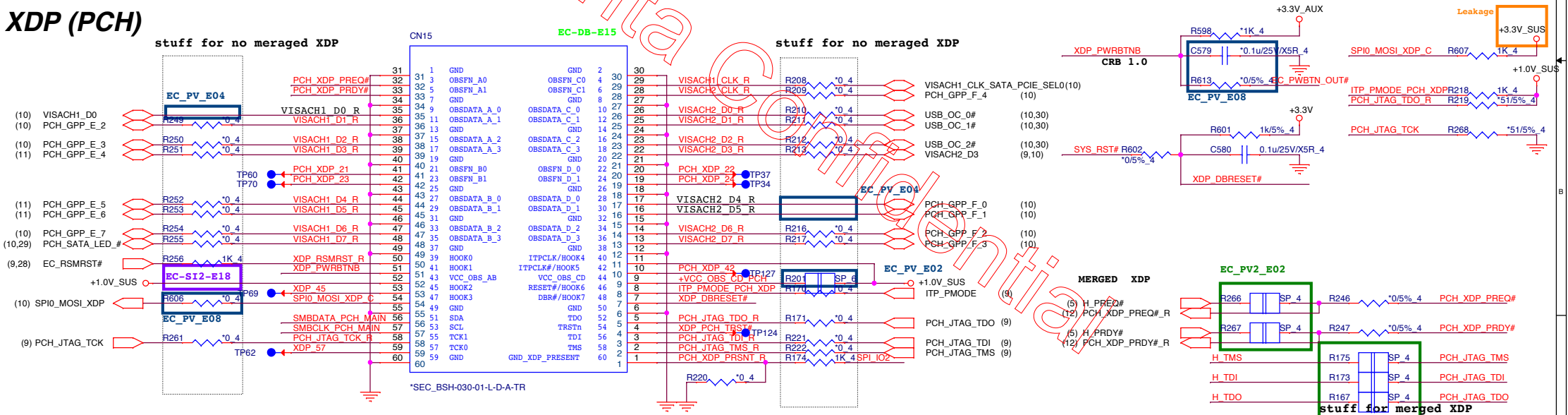
XDP (CPU)



XDP (PCH)



Quanta Computer Inc.

Project: HP-CRANE

Title		
XDP DEBUG		
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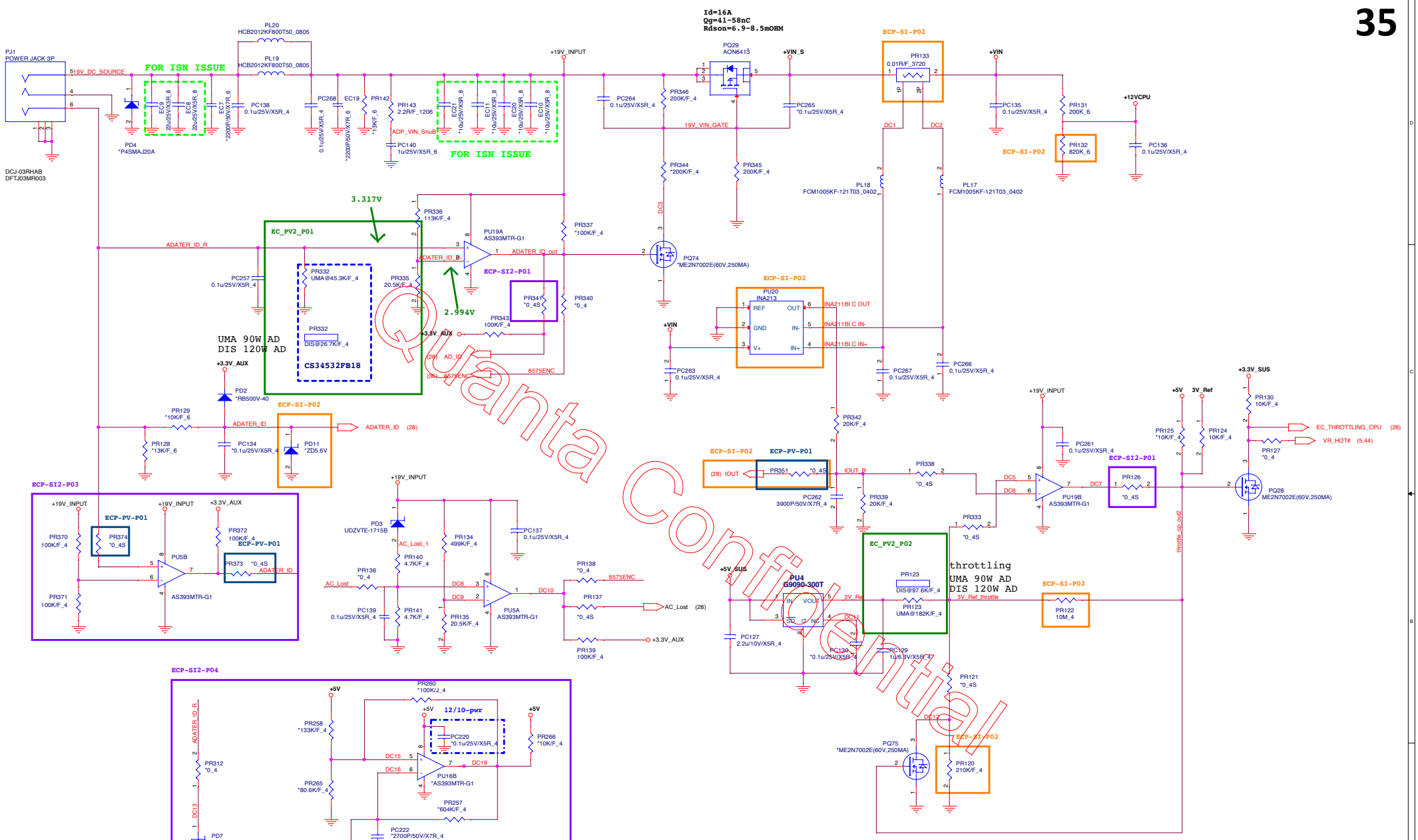

UMA,Triggered current 4.678A/91.22W
DIS, Triggered current 6.225A/121.38W

Quanta Computer Inc.
Project: HP-CRANE

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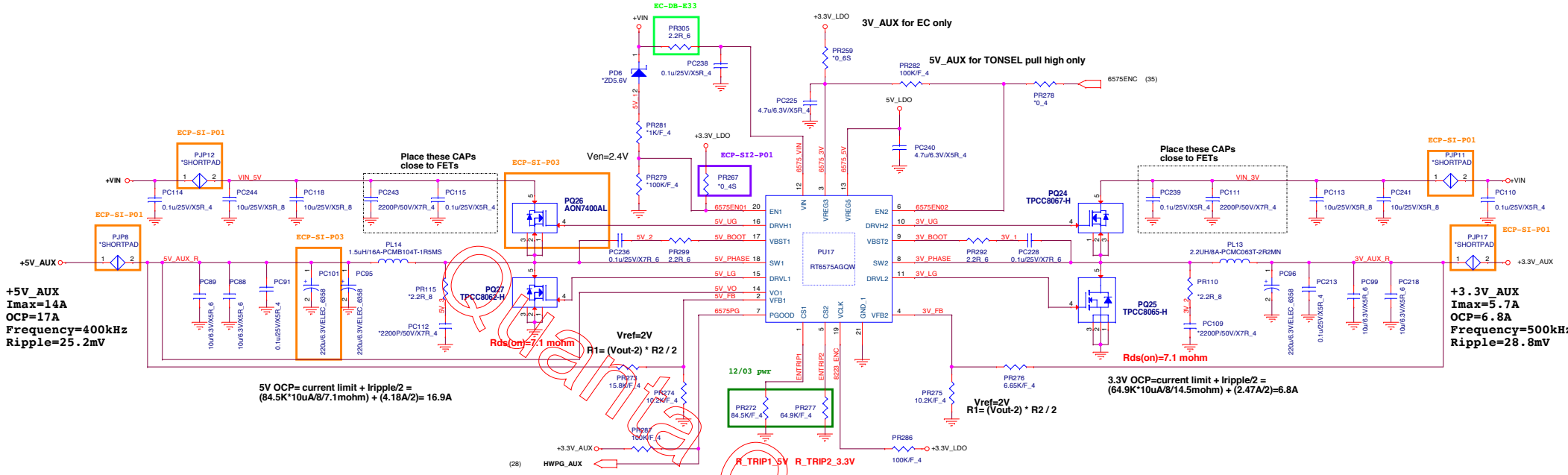

L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

Quanta Computer Inc.

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Title: 3V_AUX/5V_AUX(RT6575AGQW)

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(24,35,36,38,39,40,42,43,45,46,47,48,49,50) +VIN
(7,9,14,15,42,43,49,50) +VDDQ
(5,9,10,11,12,13,24,26,28,31,33,34,35,38,39,41,42,43,49) +3.3V_SUS
(25,29,30,32,35,39,40,41,42,43,48,49) +5V_SUS
(14,15,43) SMDDR_VTERM

+VDDQ asserted after +VCCST_PLL asserted

TPCA8A10-H Rdson < 3.8m Ohms
OCP=Current limit + Iripple/2=(105K*5uA/10/3.8mohm)+ (4.18A/2)=15.9A

Place these CAPs close to FETs

PU1 RT8231BGQW

PQ4 TPCA8064-H
PQ6 TPCA8A10-H

+VDDQ
Imax=12A
OCP=16A
Frequency=400kHz
Ripple=21mV

Quanta Computer Inc.
Project: HP-CRANE

Title: +VDDQ /SMDDR_VTERM (RT8231BGQW)
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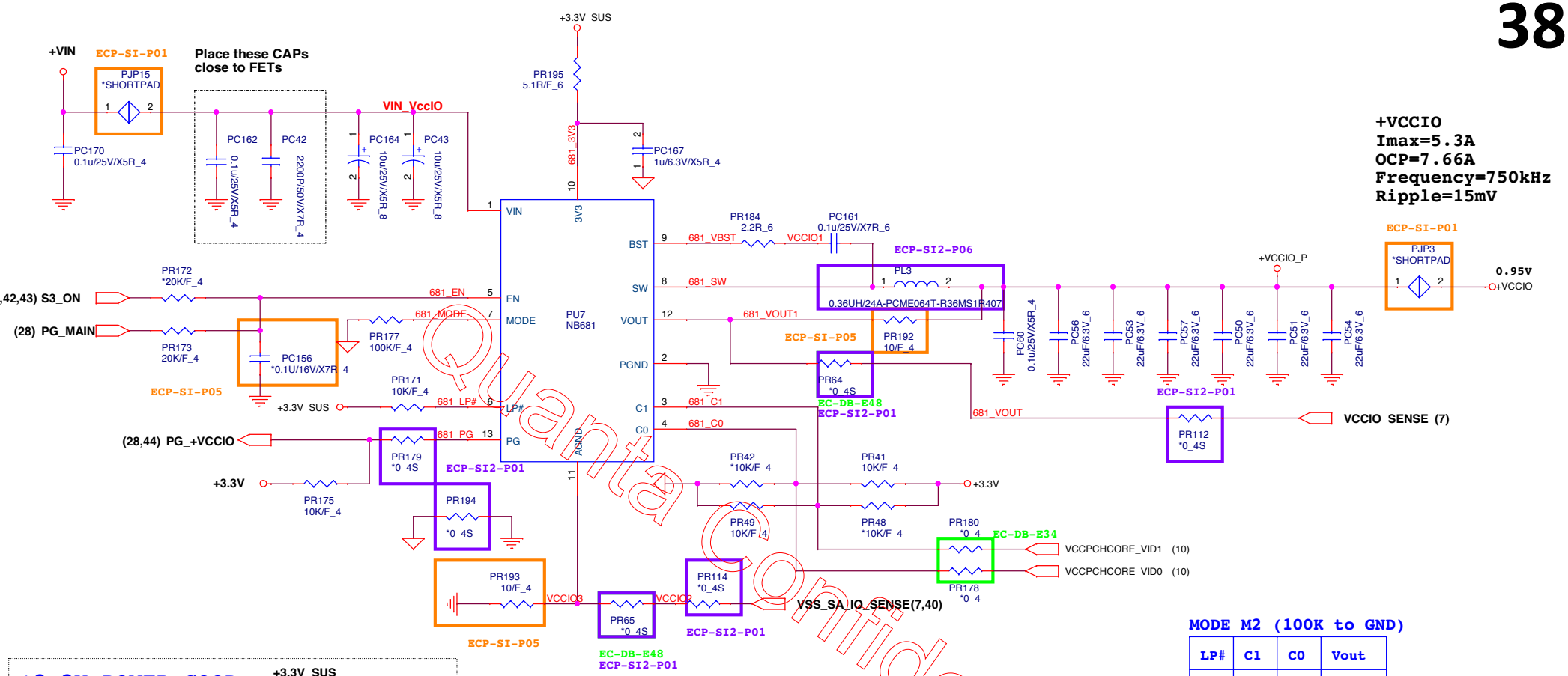
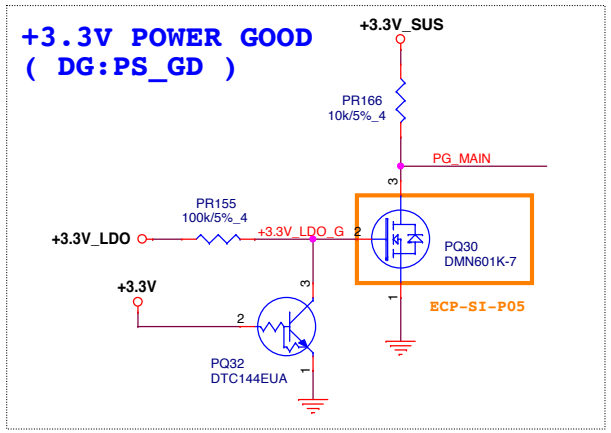


+VCCIO
Imax=5.3A
OCP=7.66A
Frequency=750kHz
Ripple=15mV



MODE M2 (Float)-Pre-ES

LP#	C1	C0	Vout
0	X	X	0.7V
1	0	0	0.8V
1	0	1	0.85V
1	1	0	0.9V
1	1	1	0.95V

MODE M2 (Float)-ES

LP#	C1	C0	Vout
0	X	X	0.7V
1	0	0	0.85V
1	0	1	0.9V
1	1	0	0.95V
1	1	1	1V

MODE M2 (100K to GND)

LP#	C1	C0	Vout
0	X	X	0V
1	0	0	0.8V
1	0	1	0.95V
1	1	0	1V
1	1	1	1.05V

Quanta Computer Inc.

Project: HP-CRANE

Title: +VCCIO(NB681)

Size | Document Number: 810606-000 | Rev: A

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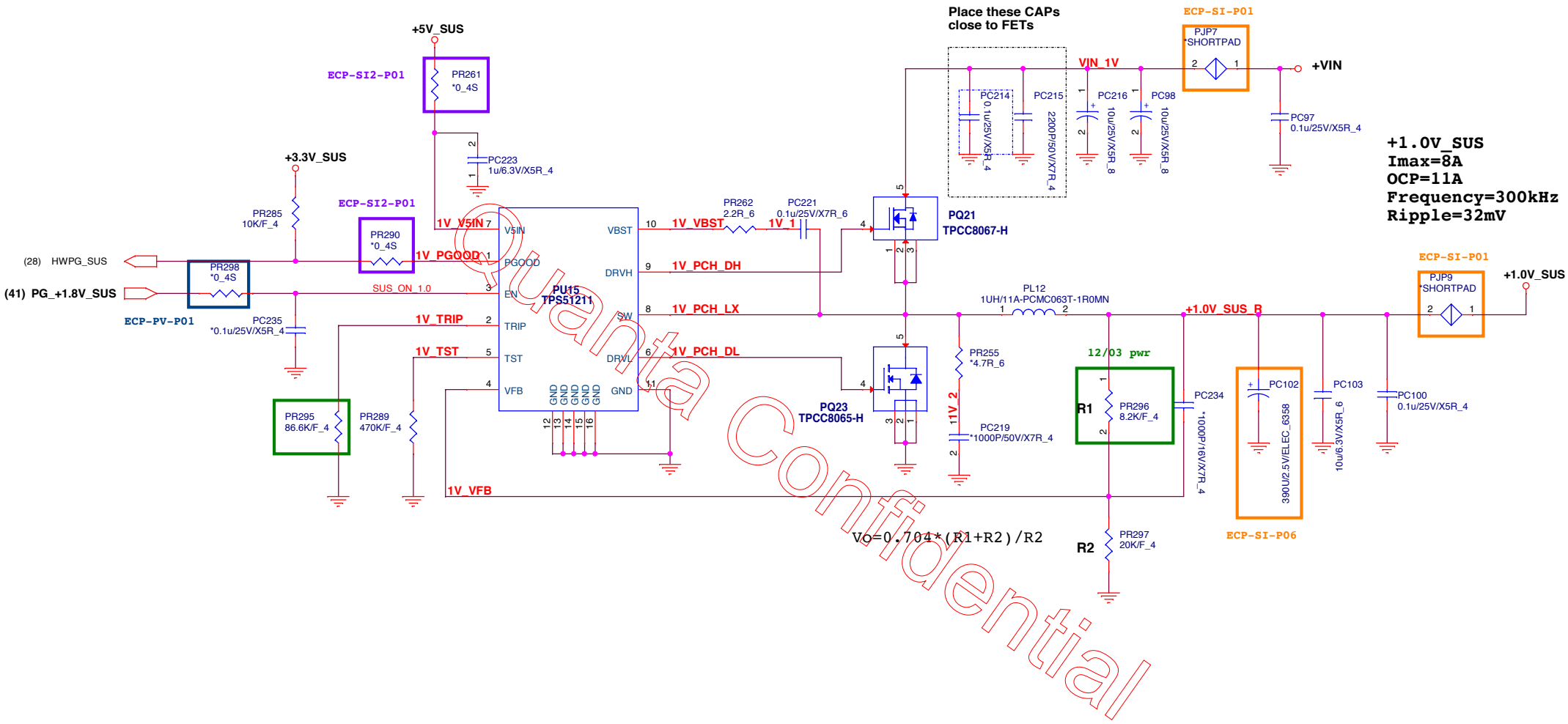

Quanta Computer Inc.	
Project: HP-CRANE	
Title: +1.0V_SUS(TPS51211)	
Size	Document Number: 810606-000 — Rev: A
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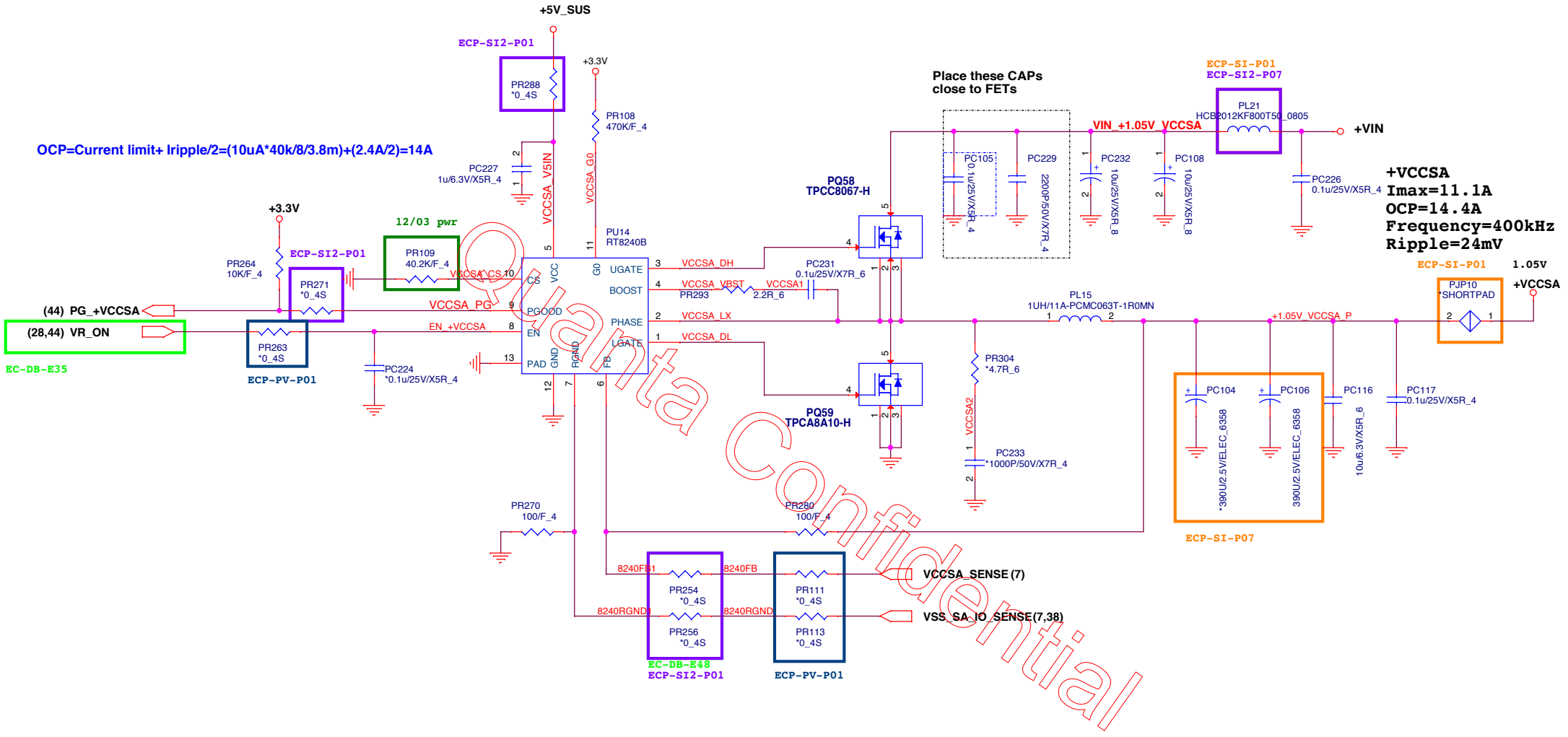

Quanta Computer Inc.	
Project: HP-CRANE	
Title: +VCCSA(RT8240B)	
Size	Document Number: 810606-000 — Rev: A
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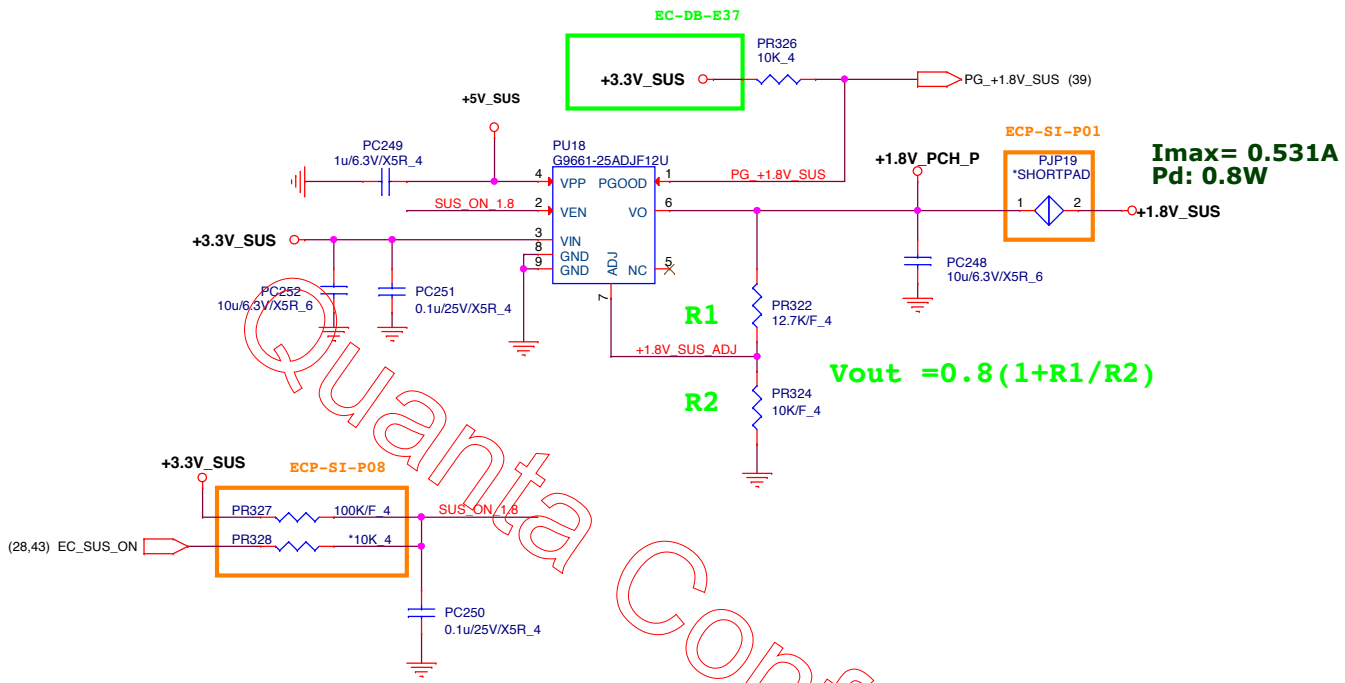

Quanta Computer Inc.

Project: HP-CRANE

Title: +1.8V_SUS (G9661)

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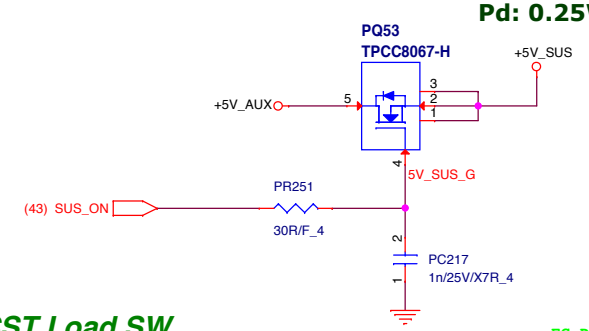
SUS ON Load SW

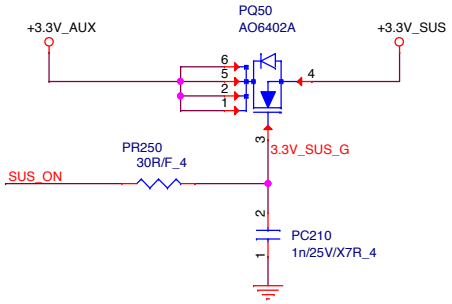
TPCC8067-H
Rdson=20m@10V Vgs

Imax=3.8A
Pd: 0.25W

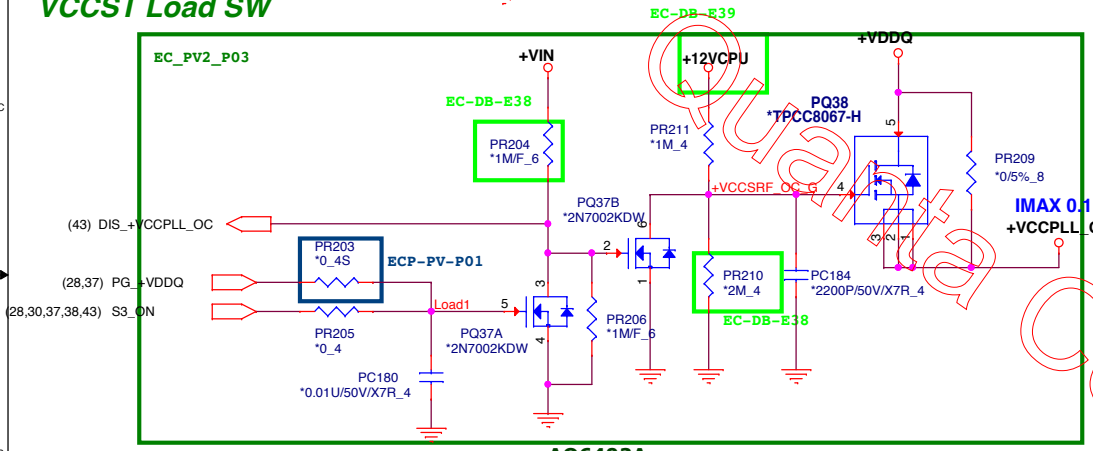


AO6402A
Rdson=24m@10V Vgs

Imax=3.26A
Pd: 0.255W

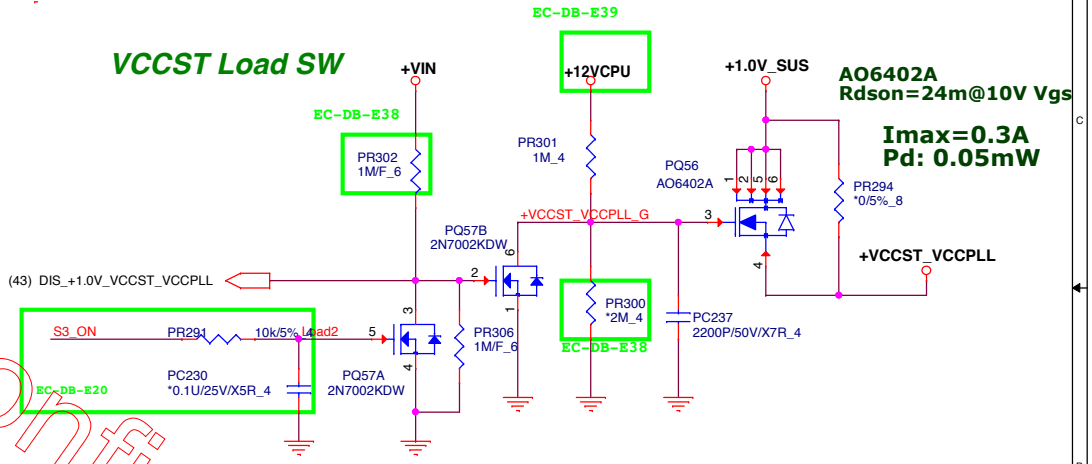


VCCST Load SW



AO6402A
Rdson=24m@10V Vgs

VCCST Load SW



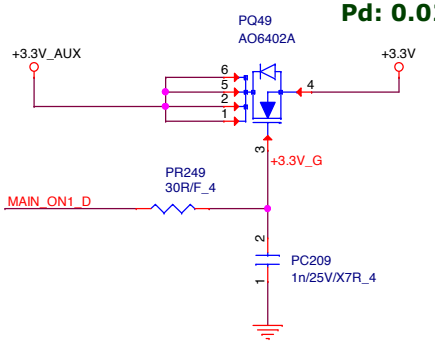
AO6402A
Rdson=24m@10V Vgs

Imax=0.3A
Pd: 0.05mW

MAIN ON_1 Load SW

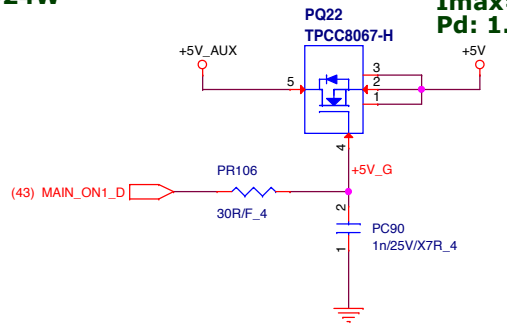
AO6402A
Rdson=24m@10V Vgs

Imax=1A
Pd: 0.024W



TPCC8067-H
Rdson=20m@10V Vgs

Imax=8A
Pd: 1.28W



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
ME3424D-G	TSOP-6	5.0A/6.7A	42m	+/- 20V
TPCC8067-H	3x3	9A	26m	+/- 20V
TPCA8064-H	SO-8	20A	7.9m	+/- 20V

Quanta Computer Inc.
Project: HP-CRANE

Title: Load Switch
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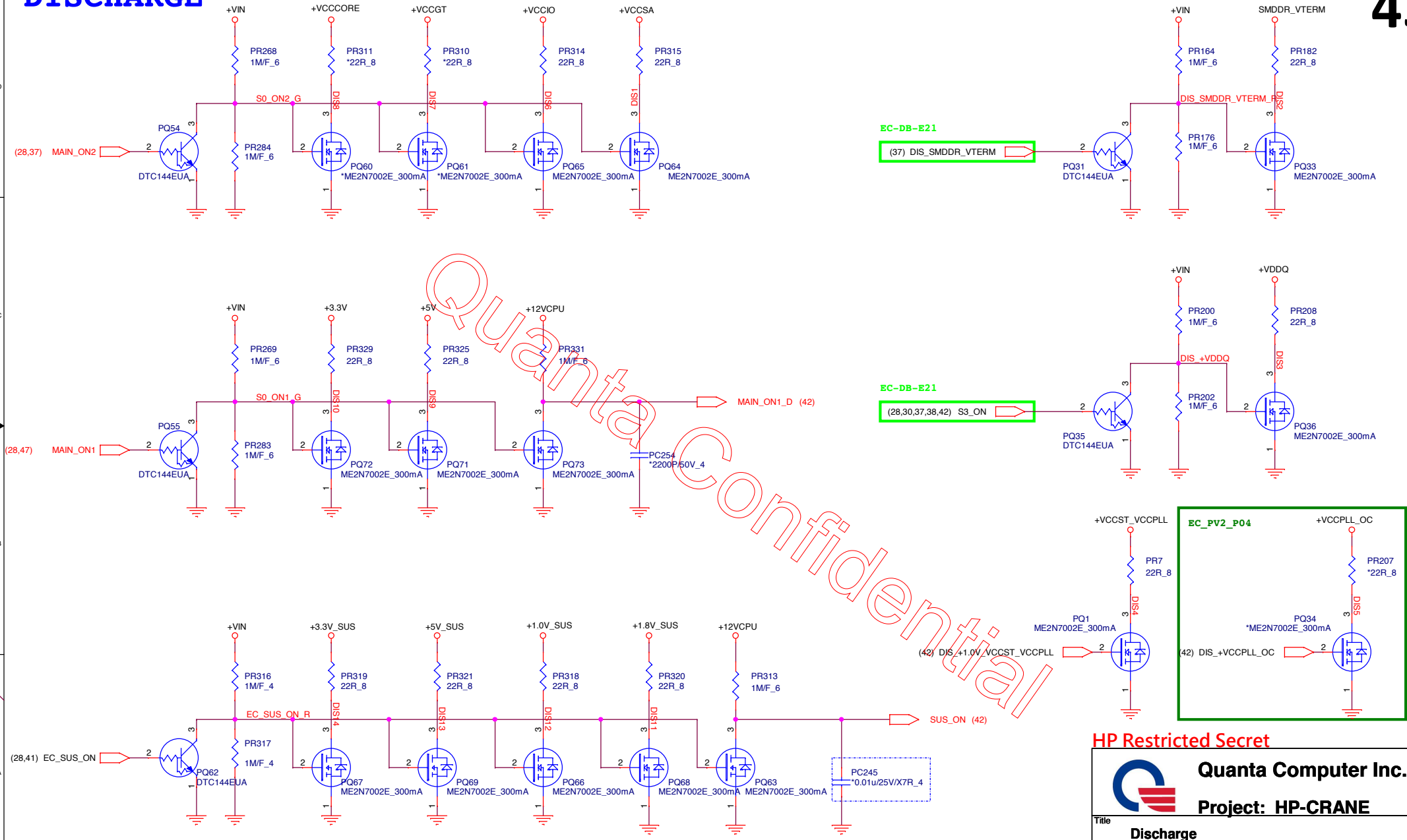
DISCHARGE



Quanta Computer Inc.

Project: HP-CRANE

Title: Discharge		
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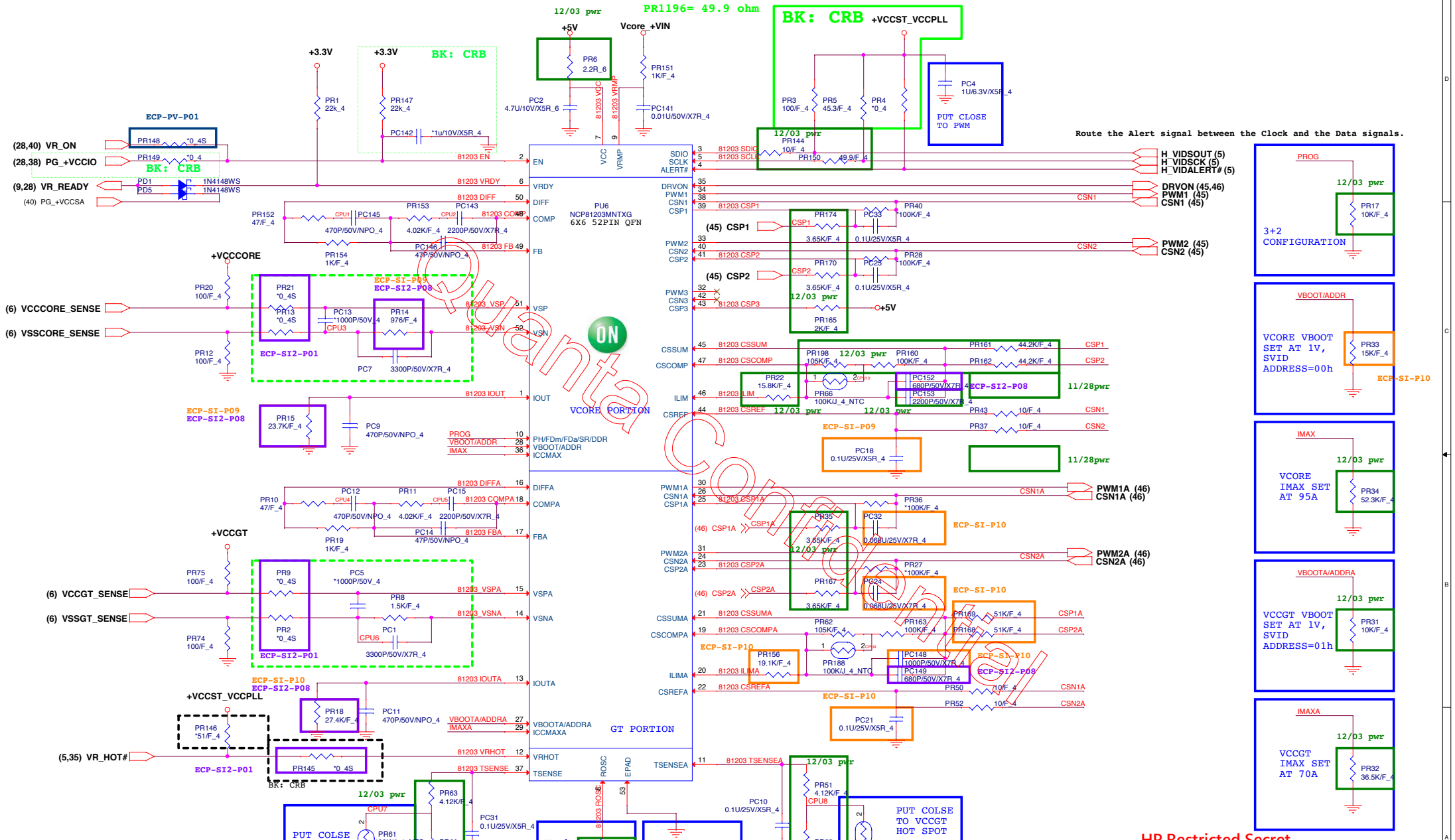
Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



HP Restricted Secret

Quanta Computer Inc.	
Project: HP-CRANE	
Title: VCC_CORE & VCC_GT	
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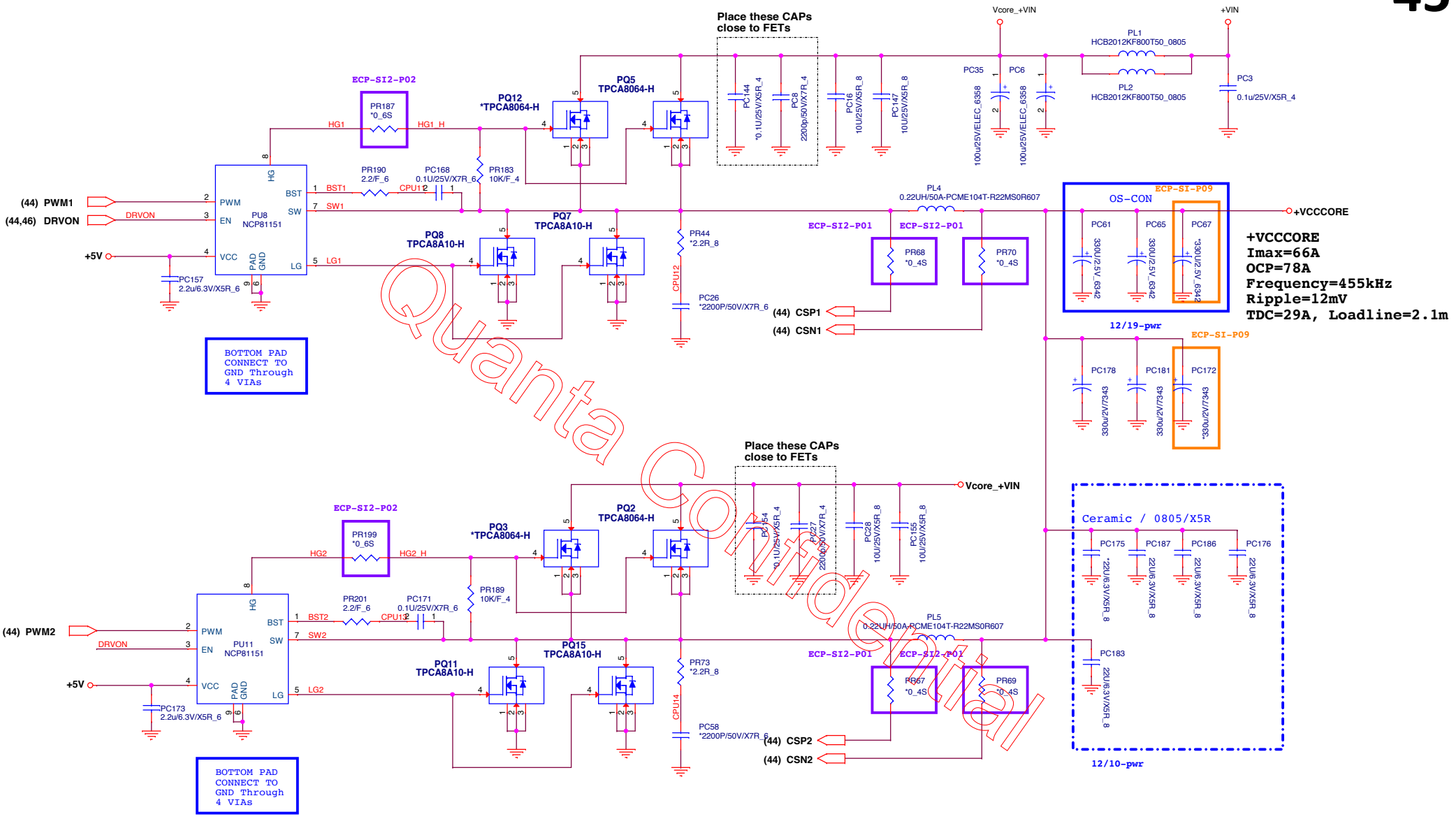

Quanta Computer Inc.

Project: HP-CRANE

Title		
VCORE OUT STAGE		
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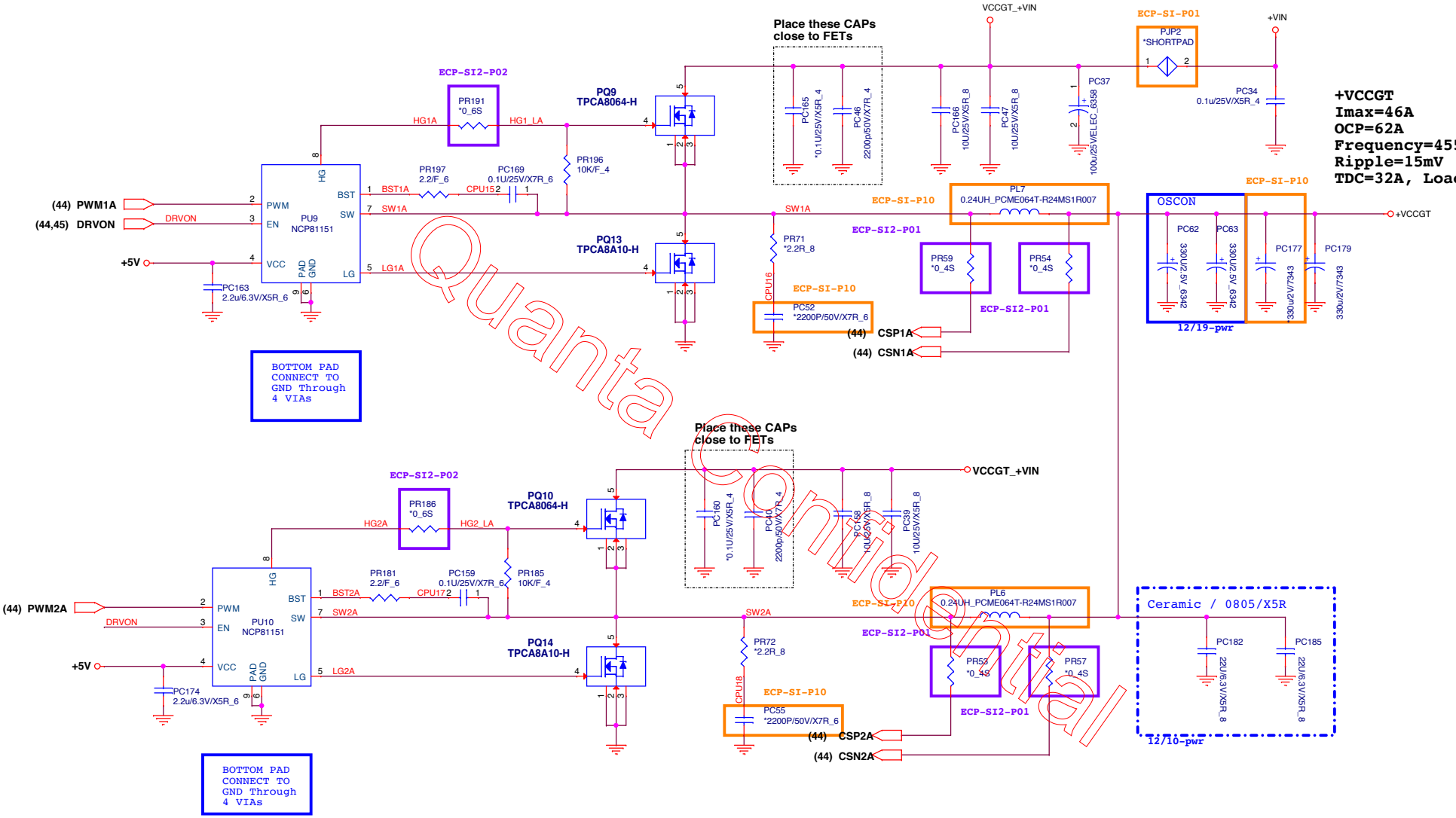

Quanta Computer Inc.

Project: HP-CRANE

Title	VCCGT OUTPUT STAGE	
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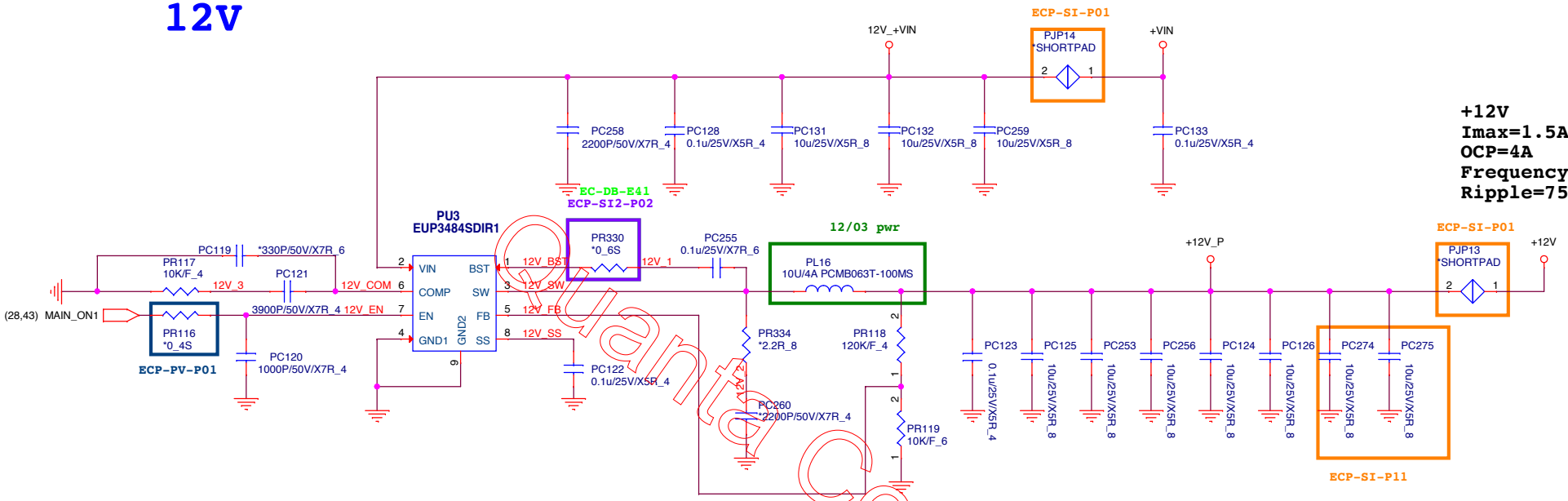
12v



+12V
Imax=1.5A
OCP=4A
Frequency=357kHz
Ripple=75mV

Vout=0.923*((R1+R2)/R2)

Quanta Computer Inc.

Project: HP-CRANE

Title		
+12V		
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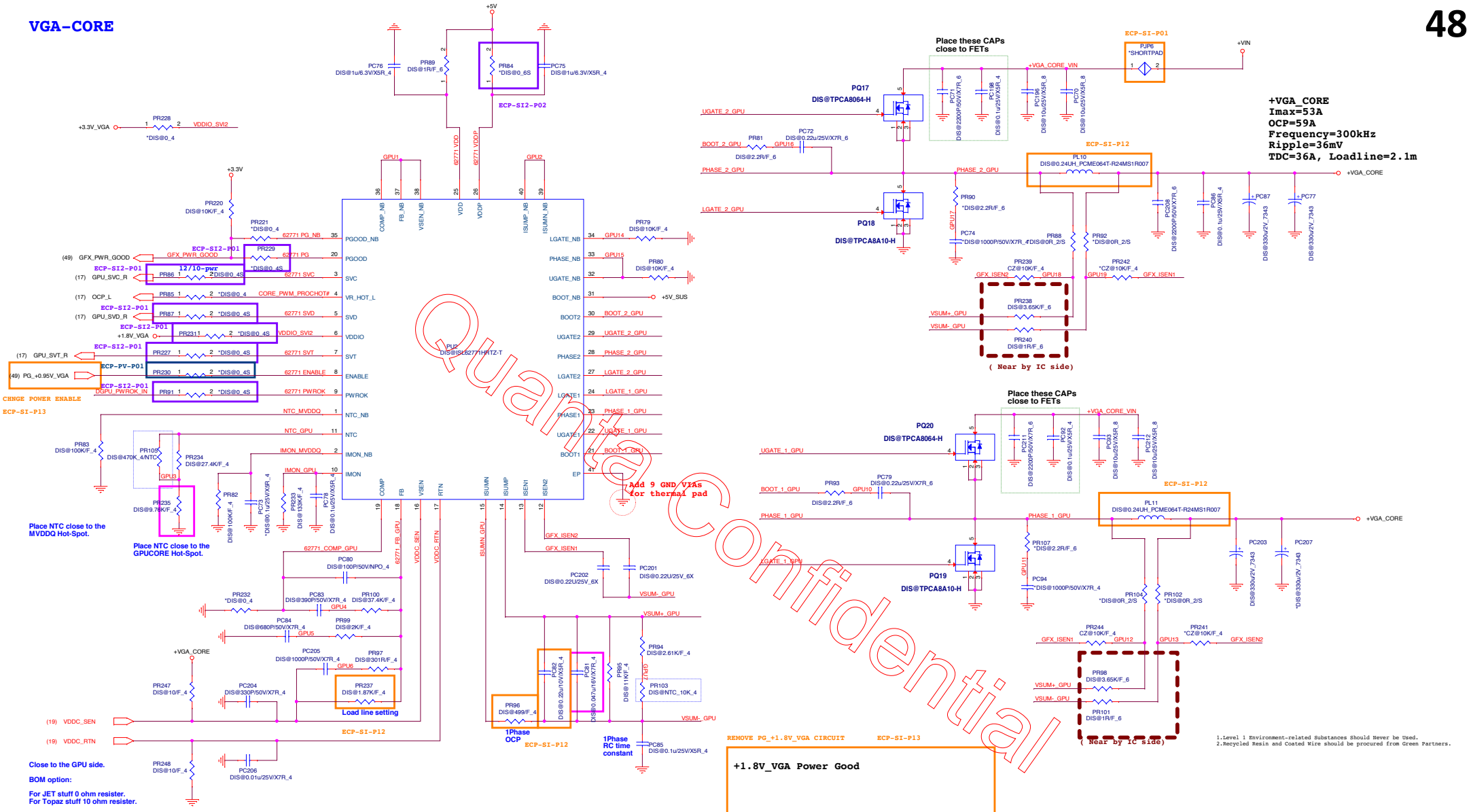
VGA-CORE



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
Project: HP-CRANE

Title: GPU_CORE (ISL62771)
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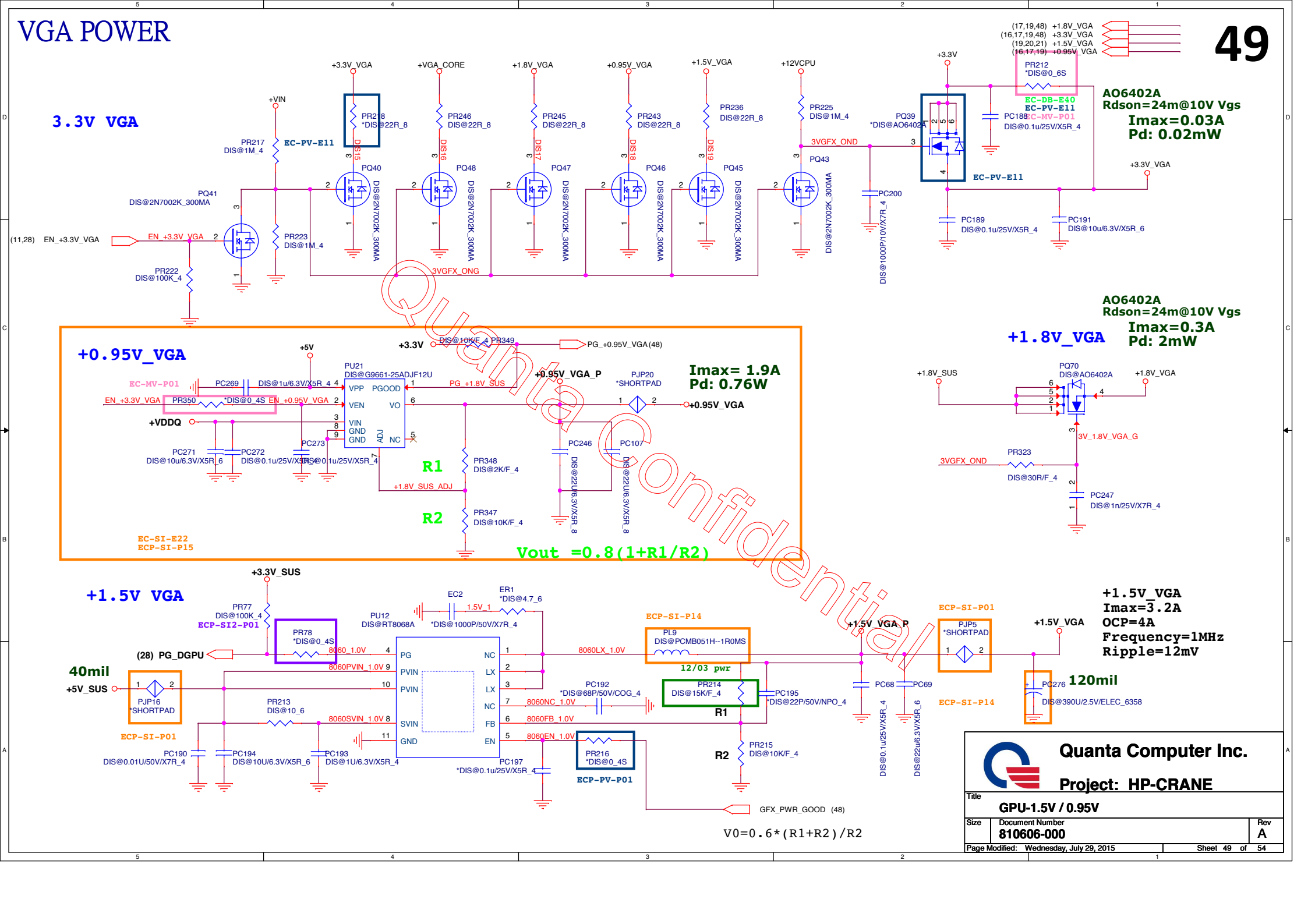
VGA POWER



CPU HOLE

H7 h-c150d150n *Hole
H10 h-c150d150n *Hole
H12 h-c150d150n *Hole
H8 SPAD-C197 *Hole

EC-DB-E23

H9 SPAD-C197 *Hole
H13 SPAD-C197 *Hole

H14 H-C276D197P2 *Hole
H15 H-C276D197P2 *Hole
H3 H-C276D197P2 *Hole
H4 H-C276D197P2 *Hole

SD CARD SHAPE

PAD8 SPAD-RE970X70NP *PAD
PAD9 SPAD-RE970X70NP *PAD

EC-SI-25 EC-SI-23

VGA HOLE

HOLE1 H-C315I166D146P2
12/10 modify

HOLE2 H-C315D146P2

WLAN HOLE

H11 H-TC236BC106D106PT Hole

PAD5 spad-c197 *PAD
PAD4 spad-c197 *PAD
PAD7 spad-c197 *PAD
PAD3 SPAD-RE394X394NP *PAD
PAD1 spad-re79x118np *PAD
PAD2 SPAD-RE362X122NP *PAD
PAD6 SPAD-RE276X394NP *PAD

Place around +VIN trace

+VIN C602 *0.1U/25V_4_X7R
+VIN C43 *0.1U/25V_4_X7R
+VIN C3 *0.1U/25V_4_X7R
+VIN C259 *0.1U/25V_4_X7R
+VIN C1 *0.1U/25V_4_X7R

+VIN C139 *0.1U/25V_4_X7R
+VIN C316 *0.1U/25V_4_X7R
+VIN C108 *0.1U/25V_4_X7R
+VIN C109 *0.1U/25V_4_X7R
+VIN C582 *0.1U/25V_4_X7R

+VIN C4 *0.1U/25V_4_X7R
+VIN C261 *0.1U/25V_4_X7R
+VIN C5 *0.1U/25V_4_X7R
+VIN C205 *0.1U/25V_4_X7R

H1 *Hole HG-TC315BR394X394D138P2-N61
H6 *Hole HG-TC315BR394X394D138P2-N61
H16 *Hole HG-C315D138P2-N61
H17 *Hole HG-TC315BR394X394D138P2-N61
H18 *Hole HG-TC315BR394X394D138P2-N61

H21 *Hole HG-TC315BR394X394D138P2-N61
H2 *Hole HG-C315D185P2-N61
H19 *Hole HG-C315D185P2-N61
H5 *Hole HG-TC315BR394X394D138P2-V11-N61
H20 *Hole HG-C315I166D138P2V8-N61

+VDDQ C300 *15p/50V/C0G_4
+VDDQ C377 100p/50V/NPO_4
+VDDQ C400 100p/50V/NPO_4
+VDDQ C501 *15p/50V/C0G_4
+VDDQ C418 *15p/50V/C0G_4
+VDDQ C374 *15p/50V/C0G_4
+VDDQ C500 100p/50V/NPO_4

+VDDQ C95 100p/50V/NPO_4
+VDDQ C357 *15p/50V/C0G_4
+VDDQ C75 100p/50V/NPO_4
+VDDQ C484 100p/50V/NPO_4
+VDDQ C122 100p/50V/NPO_4
+VDDQ C431 100p/50V/NPO_4

+VIN C558 *15p/50V/C0G_4
+VIN C559 *15p/50V/C0G_4
+VIN C606 *15p/50V/C0G_4
+VIN C536 *15p/50V/C0G_4
+VIN C206 *15p/50V/C0G_4
+VIN C260 *15p/50V/C0G_4
+VIN C185 *15p/50V/C0G_4
+VIN C531 *15p/50V/C0G_4

+12V C556 *15p/50V/C0G_4
+12V C586 *15p/50V/C0G_4
+12V C321 *15p/50V/C0G_4
+3.3V_AUX C302 *15p/50V/C0G_4
+3.3V_AUX C553 *15p/50V/C0G_4
+3.3V_AUX C609 *15p/50V/C0G_4

+3.3V C132 *15p/50V/C0G_4

+5V C512 *15p/50V/C0G_4
+5V C363 *15p/50V/C0G_4
+5V C577 *15p/50V/C0G_4

+3.3V C166 1000p/16V/X7R_4
+3.3V C165 1000p/16V/X7R_4
For SPI_CLK

Quanta Computer Inc.
Project: HP-CRANE

Title	HOLE/VIN CAP/RF CAP	
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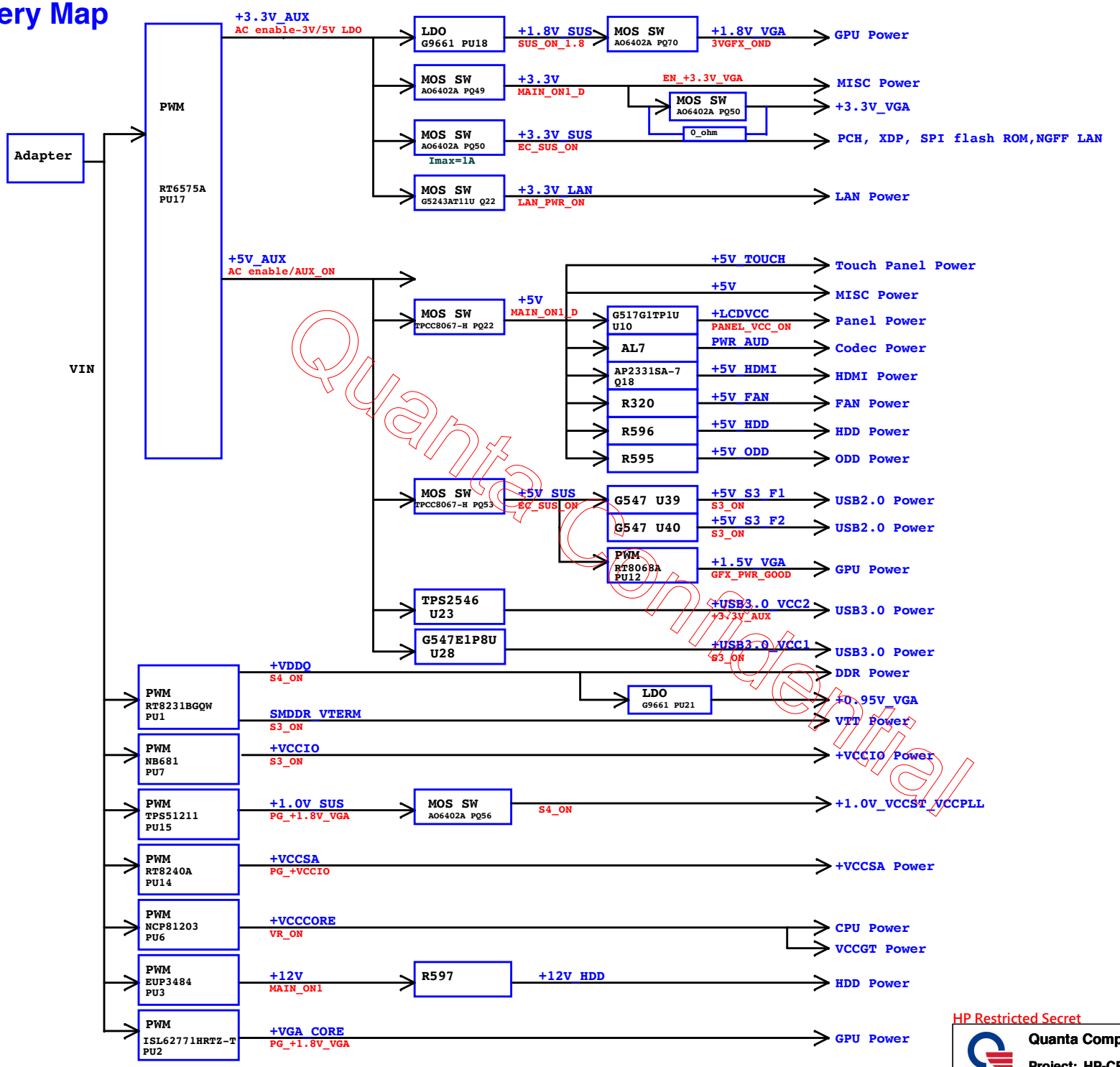
Power Delivery Map



Quanta Computer Inc.

Project: HP-CRANE

Title: Power Delivery Map

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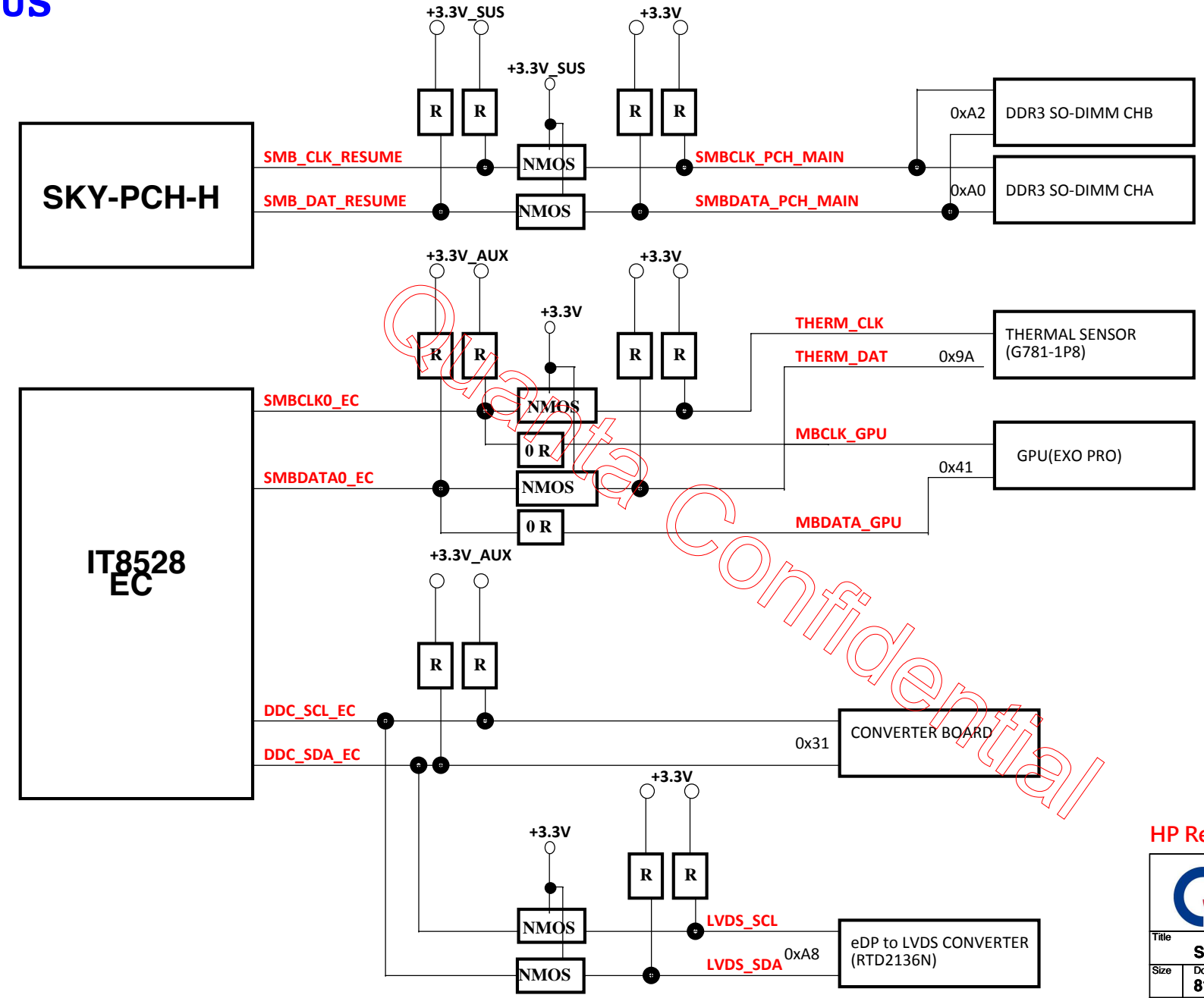
SMBUS



Quanta Computer Inc.

Project: HP-CRANE

Title: SMBus		
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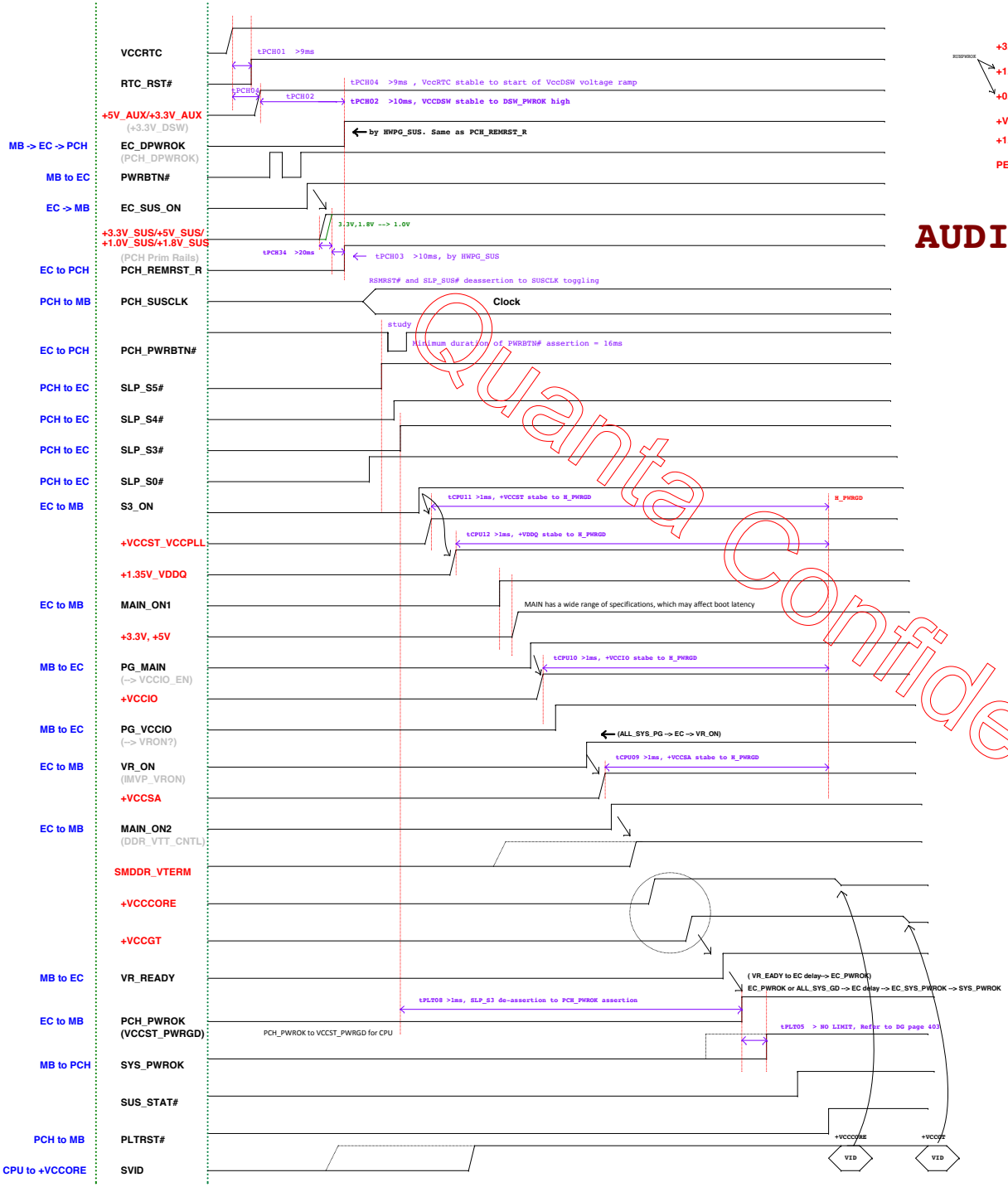
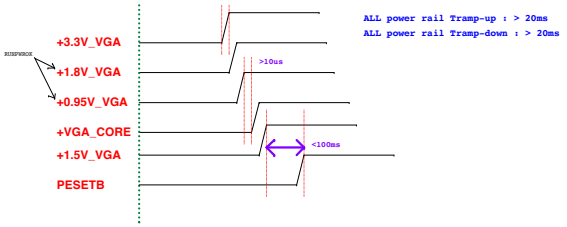
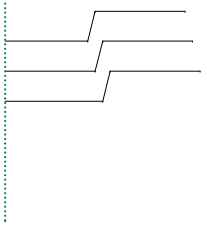
SKY-S POWER SEQUENCE



AMD dGPU POWER SEQUENCE



AUDIO POWER SEQUENCE



Quanta Computer Inc.
Project: HP-CRANE

Title		
Power Sequence		
Size	Document Number	Rev
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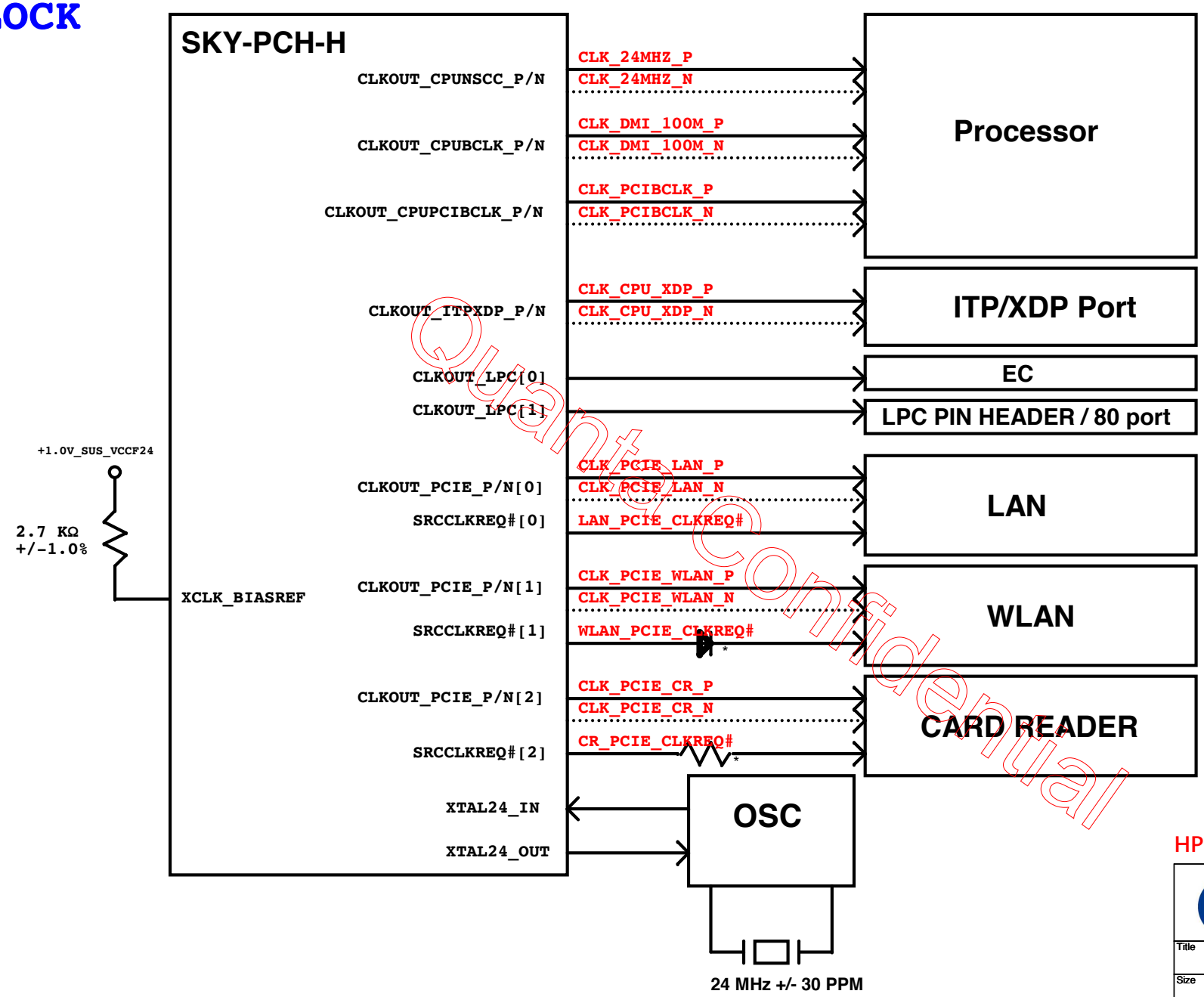
CLOCK



Quanta Computer Inc.

Project: HP-CRANE

Title	CLOCK MAP	
Size	Document Number 810606-000	Rev B
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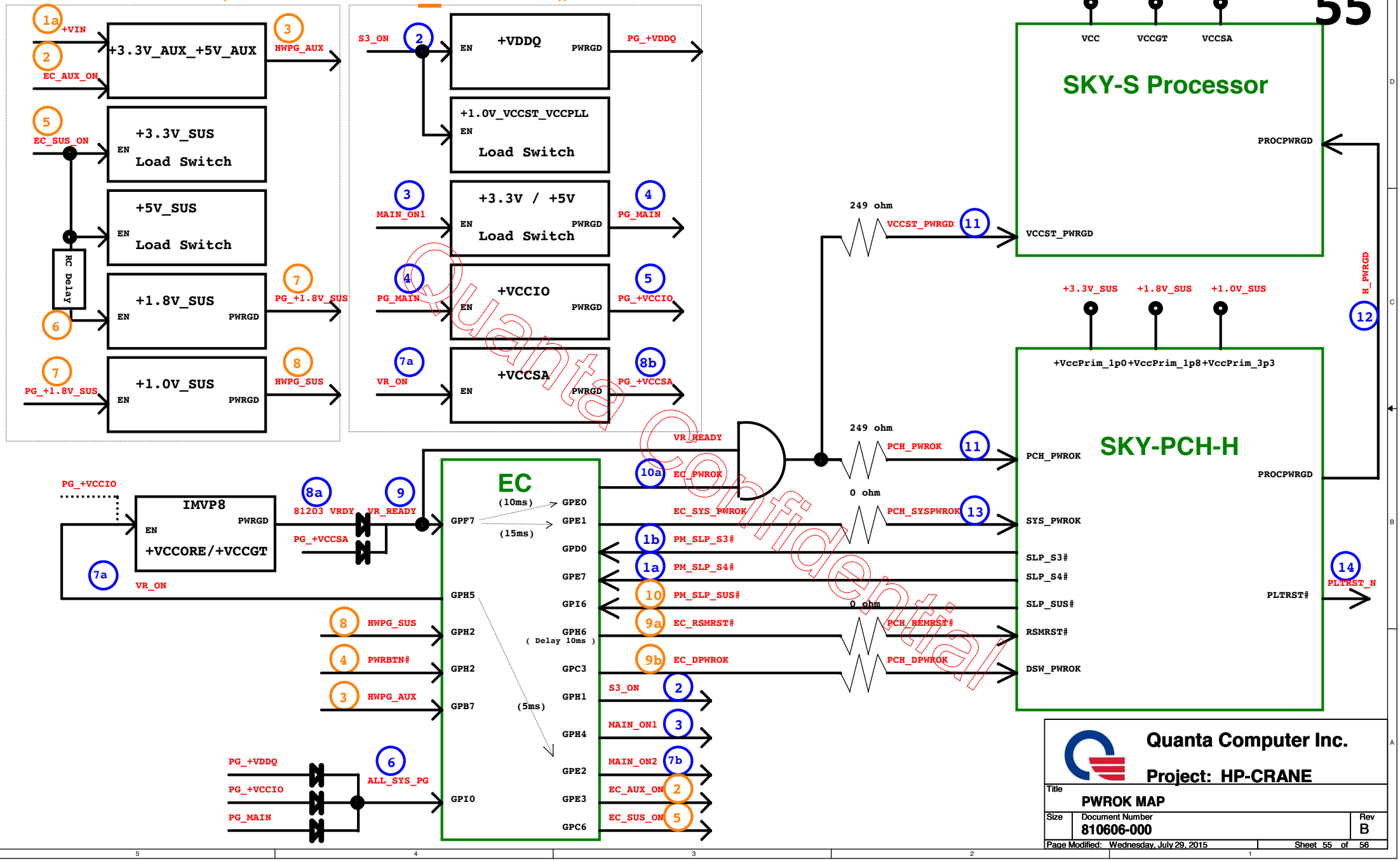
PWROK MAP / RSMRST_PWRGD#



Quanta Computer Inc.

Project: HP-CRANE

Title: PWROK MAP		
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DB to SI Change List

EC-SI-E01 Un-stuff CPU HW straps, R444,R61,R462 -- Page 5
EC-SI-E02 Un-stuff H_PWRGD pull down, R493 -- Page 5
EC-SI-E03 Un-stuff SPI_IO2 pull downy, R589 -- Page 9
EC-SI-E04 Change Q13 gate power rail,   -- Page 9
EC-SI-E05 Remove Q12 and add R698/R697 -- Page 9
EC-SI-E06 Remove C583 to fix DRAMRST rise time -- Page 9
EC-SI-E07 For XDP only, R596,R587 -- Page 10
EC-SI-E08 Don't populate R532 for +3.3V Leakage -- Page 11
EC-SI-E14 Don't populate AR3 for +3.3V Leakage -- Page 25
EC-SI-E15 Change AR1 to 4.7 ohm for EA-- Page 25
EC-SI-E16 Change from +3.3V to +3.3V_AUX for EC_SMI#_R for +3.3V_SUS Leakage -- Page 25
EC-SI-E17 Don't stuff R402/R403 for +3.3V_SUS leakage   -- Page 28
EC-SI-E18 Change U29.72 to IOUT   -- Page 28
EC-SI-E19 Add EC6 220pf on +5V_SUS, EC5 220pf on PWRBTN#, EC4 220pf on PWR_ON_LED# -- Page 32
EC-SI-E20 Add serial resistor R699 on L_FRAME# -- Page 28
EC-SI-E21 rChange serial resistor from 33ohm to 100ohm on F_LAD0_R,F_LAD1_R,F_LAD2_R,F_LAD3_RmL_FRAME#_R,L_FRAME#_R,F_LAD0_D,F_LAD1_D,F_LAD2_D,F_LAD3_D,R405,R406,R408,R456,R455,R454,R453 -- Page 28
EC-SI-E22 Add+0.95V_VGA power LDO circuit   -- Page 49
EC-SI-E23 Stuff some capactiors EMI reserved before.   -- Page 50
EC-SI-E24 Change AD4,AD5,AD6,AD7 part and their pin2 connect to GND   -- Page 25
EC-SI-E25 Change DDR3L socket, JDIM1,JDIM2-- Page 14,15
EC-SI-E26 Add ESD protector for 3D CAMERA, U41-- Page 29
EC-SI-E27 Add ESD capactior for Audio codec return path   AC38,AC30,AC45 -- Page 25
EC-SI-E28 C203, C204, C592 and C593 change with 1000pf cap for ESD -- Page 26
EC-SI-E29 AL1-AL4 change to 220 ohm bead same as previous mode for EMI, AL1~AL4   -- Page 25
EC-SI-E30 Add ESD protector for DMIC (close to CN6) -- Page 25

ECP-SI-P01 change footprint to short pad, PJP1~PJP19 -- Page35~49
ECP-SI-P02 change current sense IC multiple and EC detect system power consumption,PU20,PR133,PR351,PR132 -- Page 35
ECP-SI-P03 add power rating,PQ26,PC101 -- Page 36
ECP-SI-P04 adjust output voltage and common design. PR30/PC48/PC49 -- Page 36
ECP-SI-P05 adjust sequence and remote sense resistor.PC156/PR192/PR193 -- Page 38
ECP-SI-P06 common design. PC102 -- Page 39
ECP-SI-P07 common design. PC104/PC106-- Page 40
ECP-SI-P08 adjust sequence. PR327/PR328-- Page
ECP-SI-P09 Iout and load line setting. PR14/PR15/PC18/PC67/PC172-- Page 44
ECP-SI-P10 OCP, Iout, load line setting and common design. PR33/PR18/PR156/PR168/PR169/PC24/PC32/PC148/PC21/PL6/PL7/PC52/PC55-- Page 44
ECP-SI-P11 improve ripple. PC274/PC275-- Page 47
ECP-SI-P12 OCP, load line setting and common design. PR96/PR237/PC82/PL10/PL11-- Page 48
ECP-SI-P13 Remove PG_+1.8V_VGA circuit. PQ42/PQ44/PR224/PR226 -- Page48
ECP-SI-P14 add power rating. PL9/PC276 -- Page 49
ECP-SI-P15 change power solution from load switch to LDO. PQ16/PR76/PC66/PC107/PC246/PU21/PR347/PR349/PR348/PR350/PR269/PC271/PC272/PC273 -- Page49

SI-1 to SI-2 Change List

EC-SI2-E01 Chagne 0 ohm to shortpad., R115 -- Page 31
EC-SI2-E02 Chagne 0 ohm to shortpad., AR35,AR39,AR9 -- Page 25
EC-SI2-E03 Change and stuff Audio power., AU2,AR20,AR46,AR45 -- Page 25
EC-SI2-E04 Chagne 0 ohm to shortpad. L23,R32,   -- Page 24
EC-SI2-E05 Un-stuff Intel ME Crypto TLS pull up resistor, R198 -- Page 9
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EC-SI2-E10 Un-stuff GPP_F_11, GPP_G_5 pull up ,R156/R536 -- Page 10
EC-SI2-E11 Chagne 0 ohm to shortpad. R595 -- Page 12
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EC-SI2-E15 Un-stuff SPI_MOSI to XDP_HOOK3, R76-- Page 34
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EC-SI2-E18 Delete 0 ohm., R558,R551,R258,R622   -- Page 9,10,34

ECP-S2I-P01 change 0R_0402 to shortpad, -- Page35-40, 44-46,48-49
ECP-SI2-P02 chagne 0R_0603 to shortpad. PR56,PR187,PR199,PR186,PR191,PR330,PR84 -- Page 37, 45-48
ECP-SI2-P03 add adapter protect detect schematic ,PR370,PR371,PR372,PR373,PR374 -- Page 35
ECP-SI2-P04 delete adapter protect detect schematic . PU16,PD7,PC220,PC222,PC242,PR257,PR258,PR260,PR265,PR266,PR303,PR307,PR309 -- Page 35
ECP-SI2-P05 adjust VDDQ power rail output voltage.PR30 -- Page 37
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ECP-SI2-P08 change PR14,PR15,PR18,PC149,PC152 value- Page44

SI-2 to PV Change List

EC-PV-E01 Change serial resistor value from 0 ohm to 100ohm on EC_PRHOT_S - page5
EC-PV-E02 Chagne 0 ohm to shortpad., R107,R487,R294,R295,R265,R599,R281,R273,R264,R545,R290,R288,R243,R539,R644,R540,R224,R274,R245,
R289,R553,R301,R297,R366,R495,R369,R501,L33,R299,R226,R671,R670,R677,R686,R573,AR20,AR14,AR7,R356,R312,R667,R360,R687,R400,R391,R398,R379,R378,
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EC-PV-E03 Remove 0 ohm and short net on CPU XDP traces., R472,R482,R486,R468,R470,R110,R109 -- Page 5
EC-PV-E04 Remove 0 ohm., R647,R432,R428,R69,R62 -- Page 10,28,34
EC-PV-E05 Reserve 0 ohm for AMD dgfx power off mode. R702,   -- Page 9
EC-PV-E06 Don't stuff R559/R571 and stuff R572/R557, -- Page 12
EC-PV-E07 Don't stuff some components for TPM., R279,R278,R269,R257,R285,R241,R244,C183,C174,C175 -- Page 33
EC-PV-E08 Don't stuff conponents, R606,C59,R70,R460,R448,C579,R613 -Page 34

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EC-PV2-E02 Change 0 ohm to shortpad. R233,R578,AR10,R91,R166,R266,R267,R175,R173,R167,R48,R49
EC-PV2-E03 Remove co-lay 0ohm:R194,R195,R196,R197,R180,R181,R178,R179,R182,R183,R192,R193,R188,R189,R190,R191,R187,R186,R185,R184 -- Page 24
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EC-PV2-E04 Board ID to PV2 -- Page 12
EC_PV2_P01 Throttling point setting change: UMA(182K), DIS(97.6K) -- Page 35
EC_PV2_P02 Adapter ID setting change: UMA(45.3K), DIS(26.7K). -- Page 35
EC_PV2_P03 Remove power control of +VCCPLL_OC related circuit. -- Page 42
EC_PV2_P04 Remove Discharge related circuit of +VCCPLL_OC. -- Page 43

PV2 to MV Change List

EC-MV-E01 Change 0 ohm to shortpad. R132,R133,R143,R100,R103,R474,R122,R126,R127,R510,R511,R394,R395,R206
EC-MV-E02 Board ID to MV -- Page 12
EC_MV_P01 Change 0 ohm to shortpad. PR212,PR350