



MS-7459 VER:1.0

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780G

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111DL

HD Codec -- ALC888S-VC2

BIOS -- SPI ROM 8M

Main Memory:

DDR SO-DIMM X 2 (Max 4GB)

Expansion Slots:

MINI-PCI-E X 1 *2

IDE X 1

Clock Generator:

Controller--RTM880N-793-VB-GR

PWM:

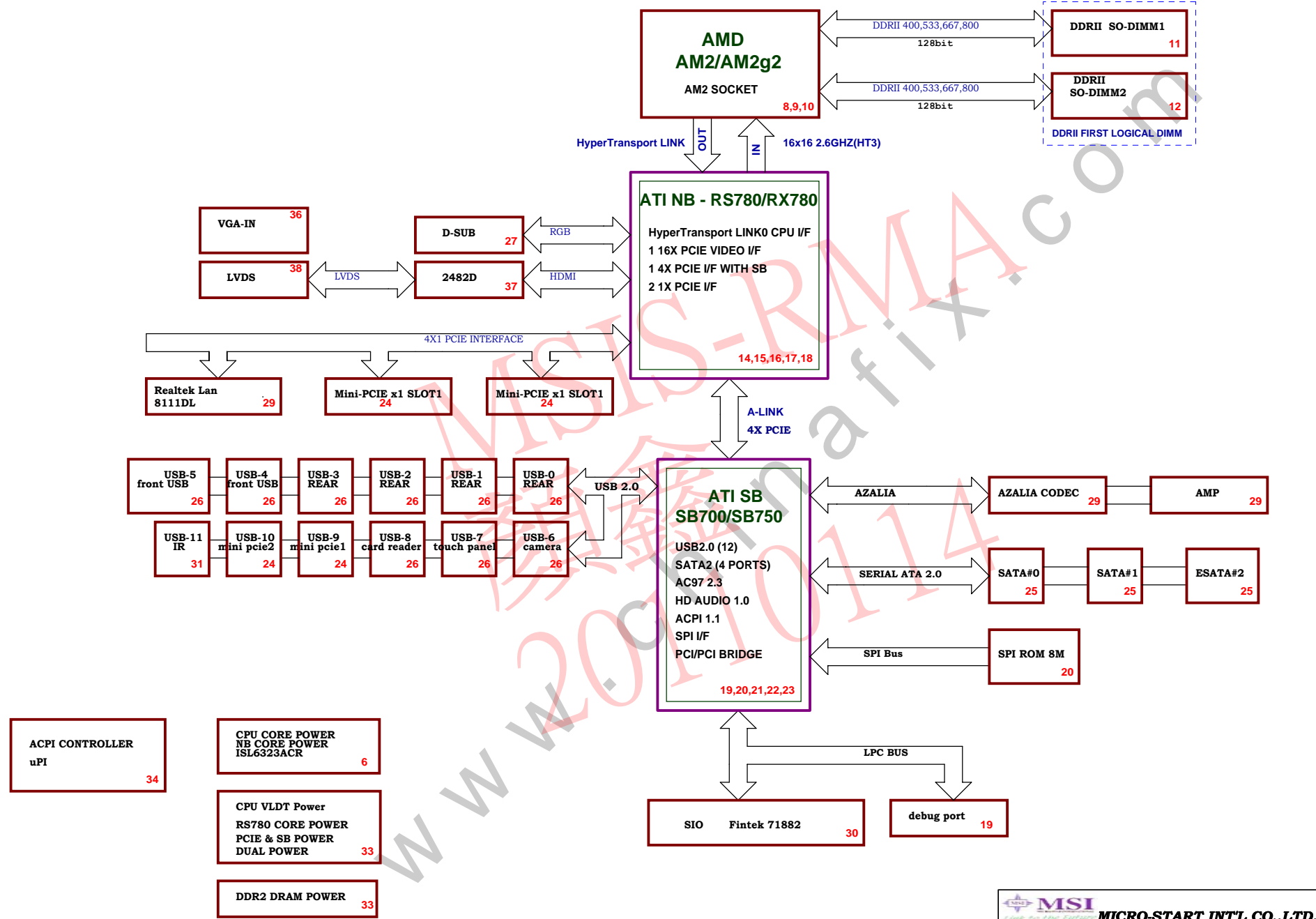
ISL6323CR

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Micro Star Restricted Secret		
Title	Cover Sheet	Rev
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Project RS780/RX780BLOCK DIAGRAM





SB700/750 GPIO Config

GPIO Name	Type	Function description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	19
REQ3#/GPIO70		PREQ#3	A6	19
REQ4#/GPIO71		PREQ#4	A6	19
GNT3#/GPIO72		Unused	AC6	19
GNT4#/GPIO73		Unused	AE5	19
INTE#/GPIO33		PCI_INTA#	AD3	19
INTF#/GPIO33		PCI_INTB#	AC4	19
INTG#/GPIO33		PCI_INTC#	AE2	19
INTH#/GPIO33		PCI_INTD#	AE3	19
LDRLQ1#/GNT5#/GPIO68		Unused	A8	19
BMREQ#/REQ5#/GPIO68		PREQ#5	AD7	19
RI#/EXTENVNT0#		RI#	E2	19
SLP_S2/GPM9#		Unused	H7	19
GA20IN/GEVENT0#		A20GATE	V15	19
KBRST#/GEVENT1#		KBRST#	W15	19
LPC_PME#/GEVENT3#		LPC_PME#	K4	19
LPC_SMI#/EXTENVNT1#		LPC_SMI3	K24	19
S3_STATE/GEVENT5#		Unused	F1	19
SYS_RESET#/GPM7#		FP_RST#	J2	19
WAKE#/GEVENT8#		WAKE#	H6	19
BLINK/GPM6#		Unused	F2	19
MBALERT1#TMRMTRIP#/GEVENT2#		SMBALERT#	J6	19
SATA_ISO#/GPIO10		SB_GPIO10	AE18	19
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6	AD18	19
SMARTVOLT/SATA_IS2/GPIO4		SB_GPIO4	AA19	19
CLK_REQ0#SATA_IS3#/GPIO0		SB_GPIO0	W18	19
CLK_REQ1#/SATA_IS4#/GPIO3		SB_GPIO3	V17	19
CLK_REQ2#/SATA_IS5#/GPIO40		SB_GPIO40	W20	19
SPKR#/GPIO2		SPKR	K21	19
SCLO/GPOC0#		SCLK	AA18	19
SDA0/GPOC1#		SDATA	W18	19
SC1I/GPOC2#		SCLK1	K1	19
SDA1/GPOC3#		SDATA1	K2	19
DDC1_SCL/GPIO9		Unused	AA20	19
DDC1_SDA/GPIO8		SPI_WP#	V18	19
LLB3/GPIO66		LC_SENSE	C1	19
SHUTDOWN#/GPIO5		SB_GPIO5	V19	21
DDR3_RST#/GEVENT7#		Unused	G5	21
SB_OC6#/IR_TX1/GEVENT6#		OC6#	B9	21
USB_OC5#IR_TX0/GPM5#		OC5#	B8	21
USB_OC4#IO_RX0/GPM4#		OC4#	A8	21
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	21
USB_OC2#/GPM2#		OC2#	E5	21
USB_OC1#/GPM1#		OC1#	F8	21
USB_OC0#/GPM0#		OC0#	E4	21
A2_SDINO/GPIO42		SDATA_IN_R	J7	21
A2_SDINI/GPIO43		Unused	J8	21
A2_SDIN2/GPIO44		Unused	L8	21
A2_SDIN3/GPIO46		Unused	M3	21

SB700/750 GPIO Config

GPIO Name	Type	Function description	Pin	Page
AZ_DOCK_RST#/GPM8#	3.3V	Unused	L5	21
PS2_DAT#/EC_GPIO0		Unused	H19	21
PS2_CLK#/EC_GPIO1		Unused	H20	21
SP1_CS2#/EC_GPIO2		Unused	H21	21
1DE_RST#/F_RST#/EC_GPO3		Unused	F25	21
PS2KB_DAT#/EC_GPIO4		Unused	D22	21
PS2KB_CLK#/EC_GPIO5		Unused	E24	21
PS2M_DAT#/EC_GPIO6		Unused	E25	21
PS2M_CLK#/EC_GPIO7		Unused	D23	21
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	21
KSO_16/EC_GPIO8		Unused	A18	21
KSO_17/EC_GPIO9		Unused	B18	21
EC_PWM0/EC_GPIO10		Unused	F21	21
SC12/EC_GPIO11		Unused	D21	21
SDA2/EC_GPIO12		Unused	F19	21
SC13_LV/EC_GPIO13		Unused	E20	21
SDA3_LV/EC_GPIO14		Unused	E21	21
EC_PWM1/EC_GPIO15		Unused	E19	21
EC_PWM2/EC_GPIO16		SB_GP16	D19	21
EC_PWM3/EC_GPIO17		Unused	E18	21
KSI_0/EC_GPIO18		Unused	G20	21
KSI_1/EC_GPIO19		Unused	G21	21
KSI_2/EC_GPIO20		Unused	D25	21
KSI_3/EC_GPIO21		Unused	D24	21
KSI_4/EC_GPIO22		Unused	C25	21
KSI_5/EC_GPIO23		Unused	C24	21
KSI_6/EC_GPIO24		Unused	B25	21
KSI_7/EC_GPIO25		Unused	C23	21
KSO_0/EC_GPIO26		Unused	B24	21
KSO_1/EC_GPIO27		Unused	B23	21
KSO_2/EC_GPIO28		Unused	A23	21
KSO_3/EC_GPIO29		Unused	C22	21
KSO_4/EC_GPIO30		Unused	A22	21
KSO_5/EC_GPIO31		Unused	B22	21
KSO_6/EC_GPIO32		Unused	B21	21
KSO_7/EC_GPIO33		Unused	A21	21
KSO_8/EC_GPIO34		Unused	D20	21
KSO_9/EC_GPIO35		Unused	C20	21
KSO_10/EC_GPIO36		Unused	A20	21
KSO_11/EC_GPIO37		Unused	B20	21
KSO_12/EC_GPIO38		Unused	B19	21
KSO_13/EC_GPIO39		Unused	A19	21
KSO_14/EC_GPIO40		Unused	D18	21
KSO_15/EC_GPIO41		Unused	C18	21
SATA_ACT#/GPIO67		SATA_LED#	W11	21
1DE_D0/GPIO15		Unused	AD24	21
1DE_D1/GPIO16		Unused	AD23	21
1DE_D2/GPIO17		Unused	AE22	24
1DE_D3/GPIO18		Unused	AC22	21

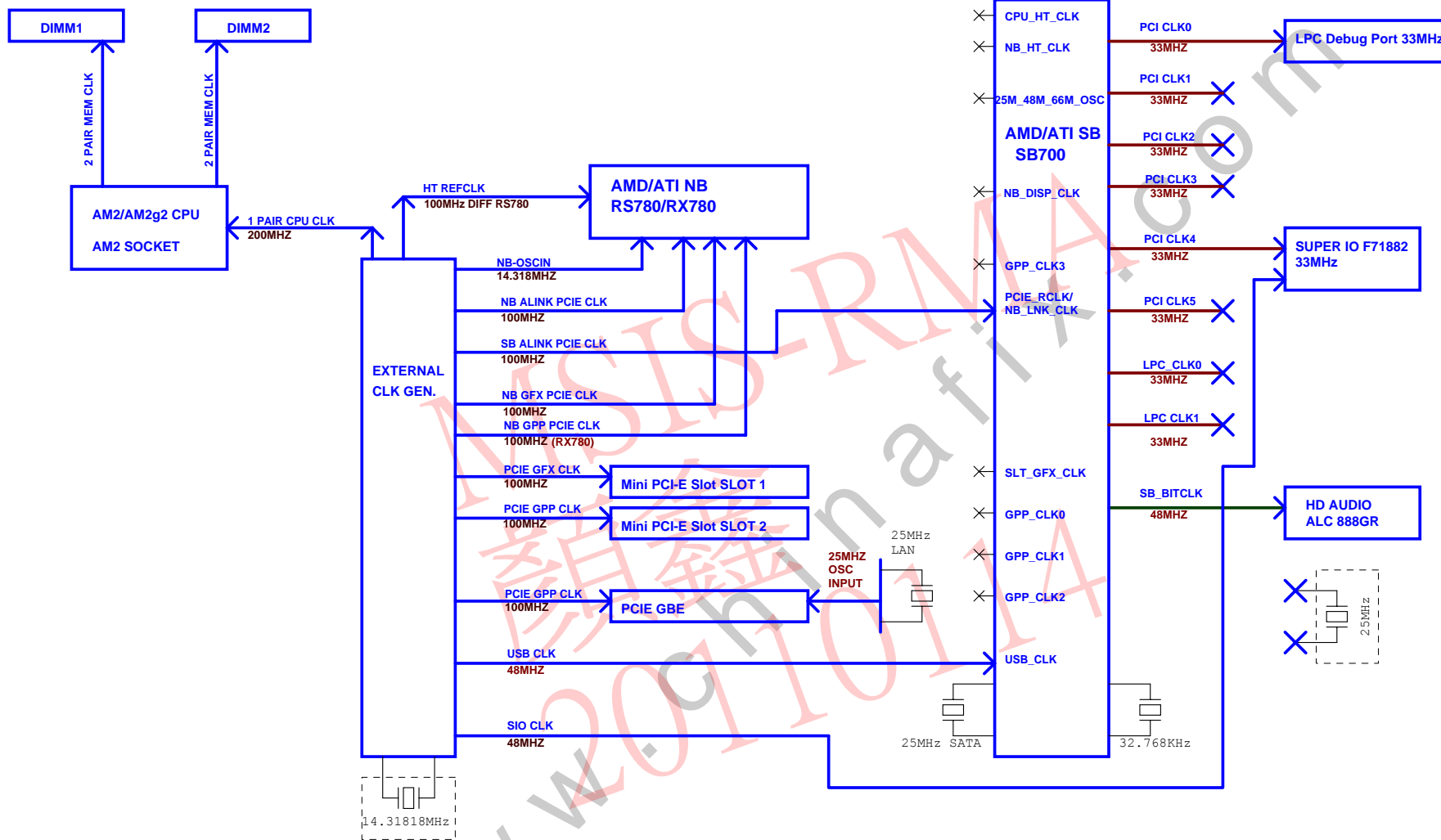
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F71882 GPIO Config

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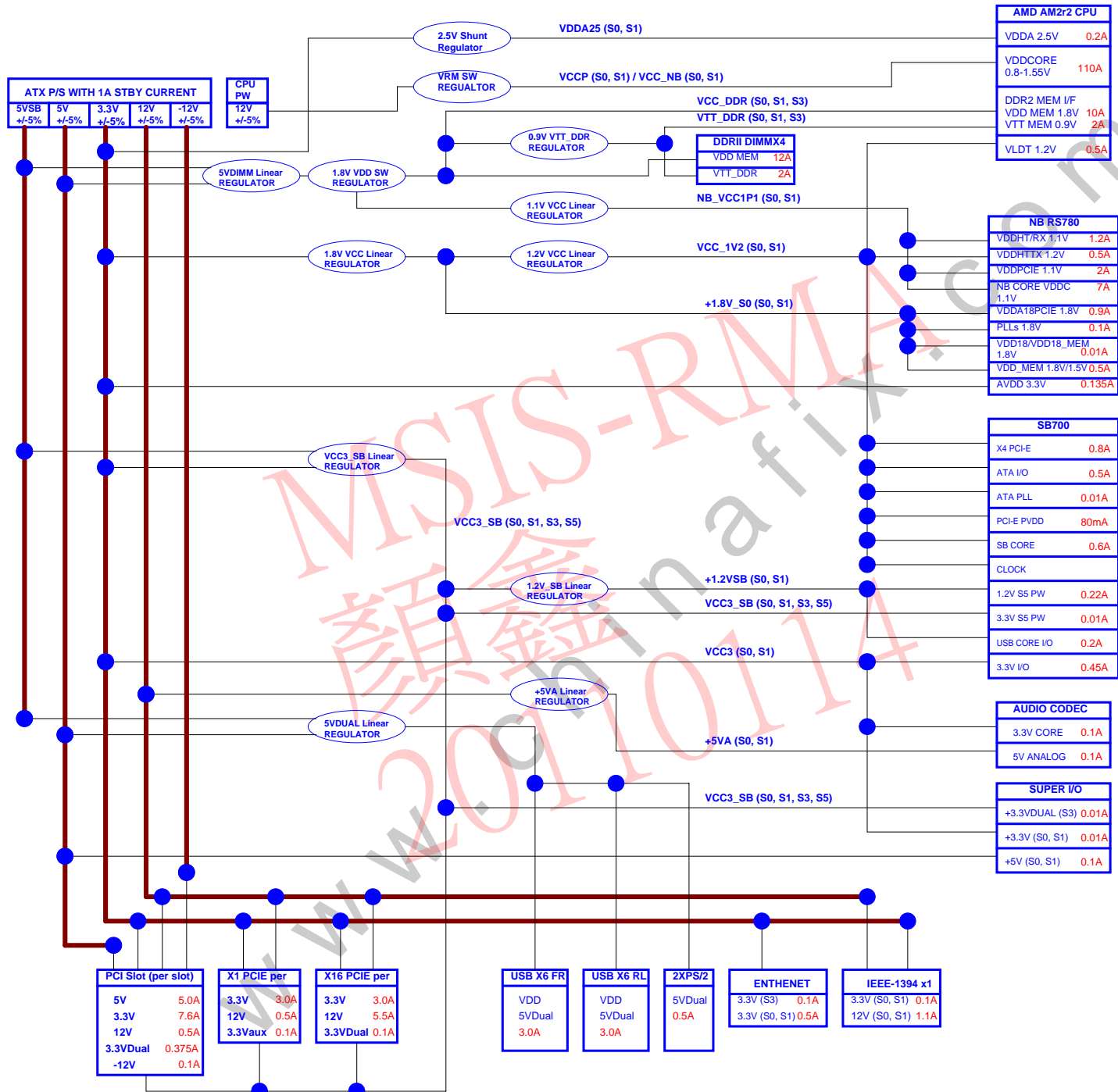
PCI Config.

DEVICE	MCP1_INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT# PCI_INTF# PCI_INTG# PCI_INTH#	REQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTG# PCI_INTH# PCI_INTE#	REQ#1 PGNT#1	AD22	PCICLK1
PCI Slot 3	PCI_INTG# PCI_INTH# PCI_INTE# PCI_INTF#	REQ#2 PGNT#2	AD23	PCICLK3

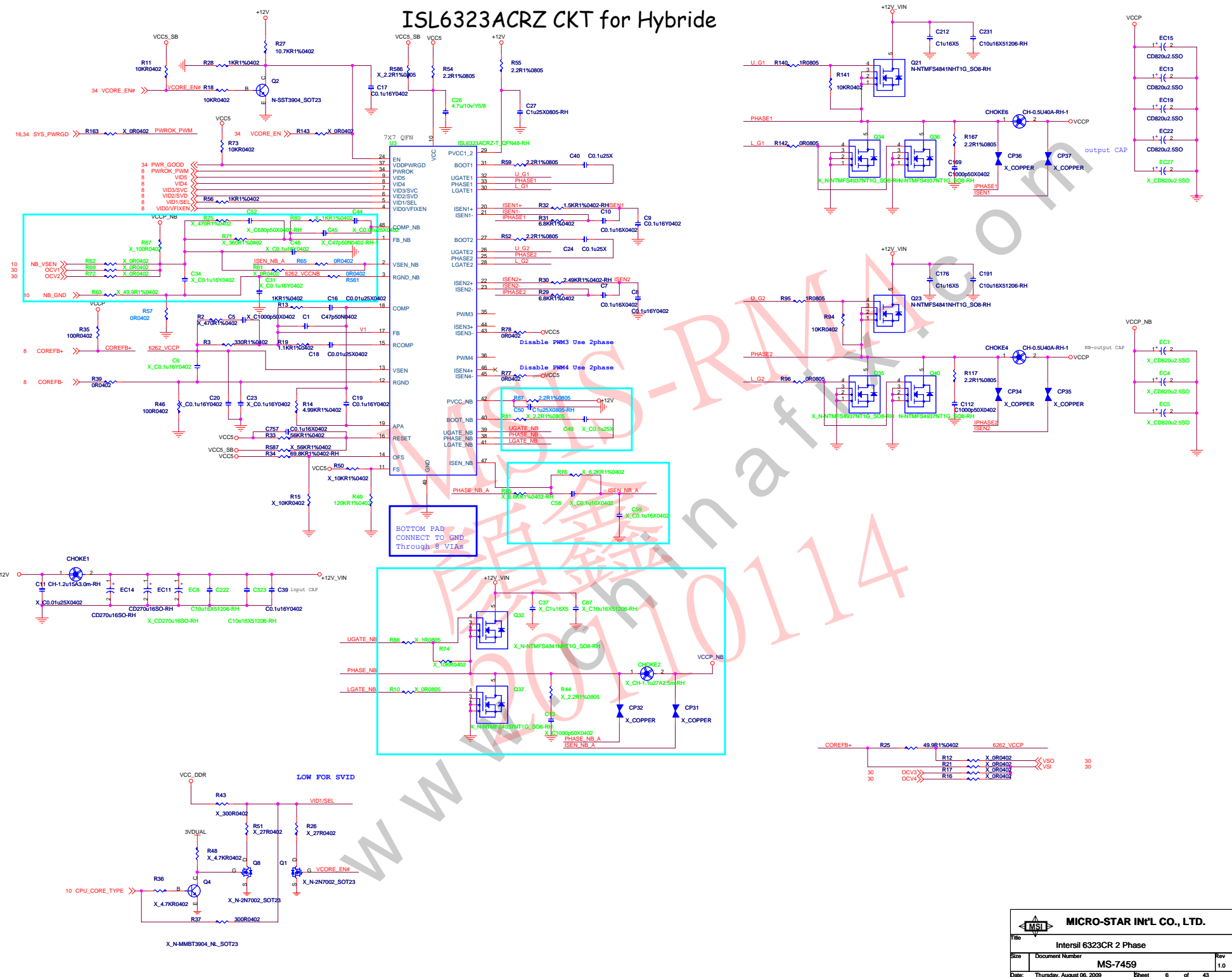


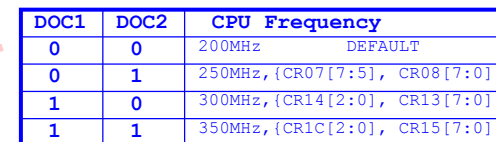
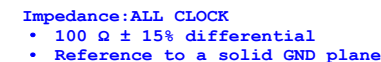
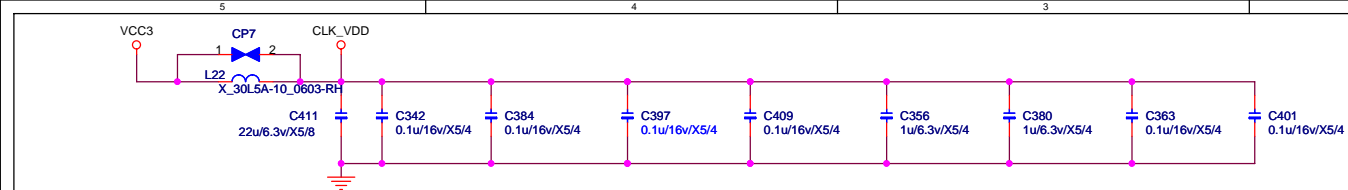
External clock mode
Internal clock mode

Power Deliver Chart



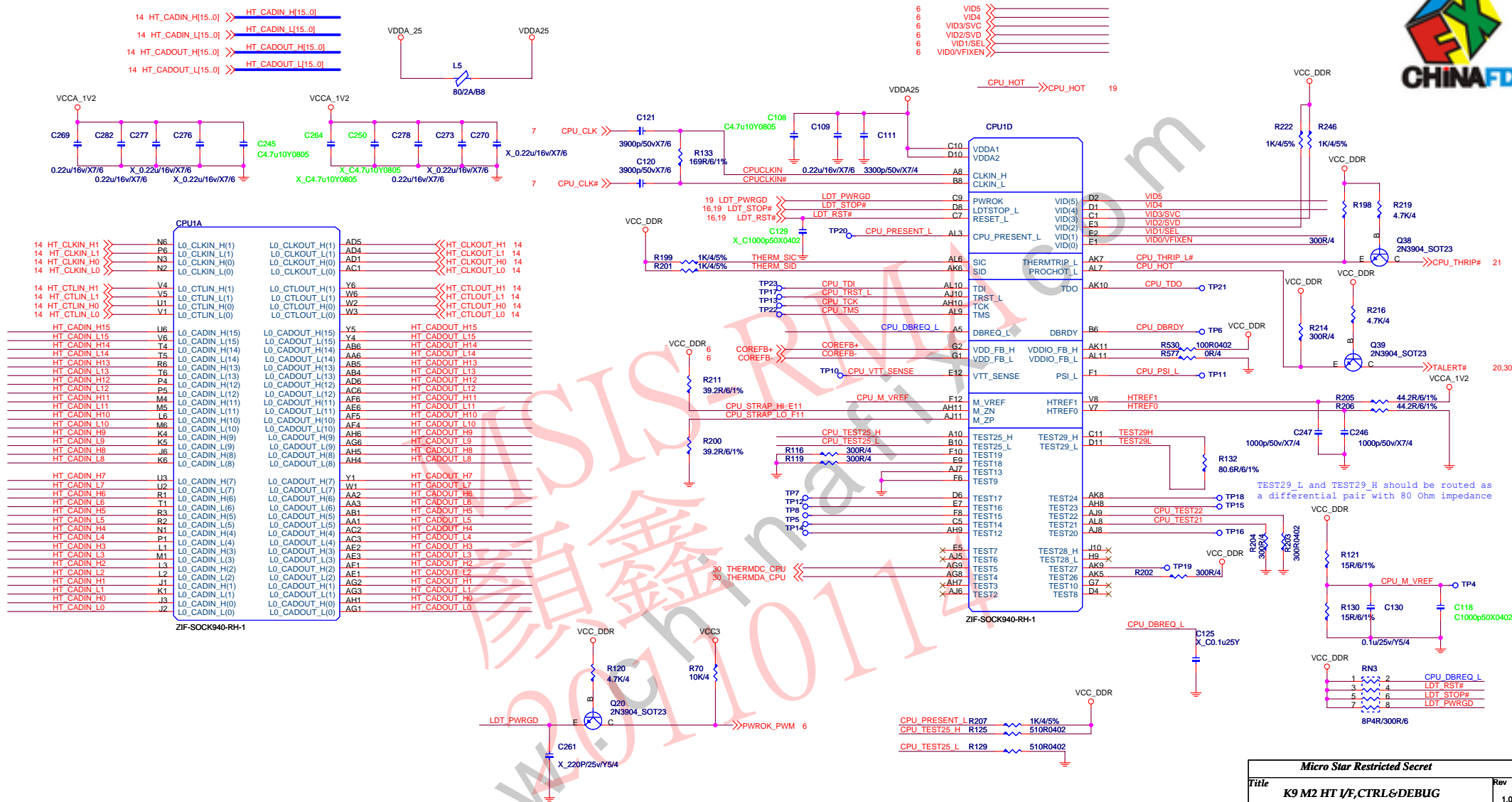
ISL6323ACRZ CKT for Hybride





FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

<i>Micro Star Restricted Secret</i>			
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11 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
11 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
11 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
11,13 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
11 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

12 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
12 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
12 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
12,13 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
12 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



CPU1B

11,13 MEM_MA0_CLK_H2 >> MEM_MA0_CLK_H2 AG21
11,13 MEM_MA0_CLK_L2 >> MEM_MA0_CLK_L2 AG20
11,13 MEM_MA0_CLK_H1 >> MEM_MA0_CLK_H1 H19
11,13 MEM_MA0_CLK_L1 >> MEM_MA0_CLK_L1 U27
11,13 MEM_MA0_CS_L1 >> MEM_MA0_CS_L1 AC25
11,13 MEM_MA0_CS_L0 >> MEM_MA0_CS_L0 AA24
11,13 MEM_MA0_ODT0 >> MEM_MA0_ODT0 AC28
11,13 MEM_MA1_ODT0 >> MEM_MA1_ODT0 AC27
11,13 MEM_MA_CAS_L >> MEM_MA_CAS_L AB25
11,13 MEM_MA_WE_L >> MEM_MA_WE_L AB27
11,13 MEM_MA_RAS_L >> MEM_MA_RAS_L AA26
11,13 MEM_MA_BANK2 >> MEM_MA_BANK2 N25
11,13 MEM_MA_BANK1 >> MEM_MA_BANK1 Y27
11,13 MEM_MA_BANK0 >> MEM_MA_BANK0 AA27
11,13 MEM_MA_CKE1 >> MEM_MA_CKE1 L27
11,13 MEM_MA_CKE0 >> MEM_MA_CKE0 M25
MEM_MA_ADD15 M27
MEM_MA_ADD14 N24
MEM_MA_ADD13 AC26
MEM_MA_ADD12 N26
MEM_MA_ADD11 P25
MEM_MA_ADD10 Y25
MEM_MA_ADD9 N27
MEM_MA_ADD8 R24
MEM_MA_ADD7 P27
MEM_MA_ADD6 R25
MEM_MA_ADD5 R26
MEM_MA_ADD4 R27
MEM_MA_ADD3 T25
MEM_MA_ADD2 U25
MEM_MA_ADD1 T27
MEM_MA_ADD0 W24
MEM_MA_DQS_H7 AD15
MEM_MA_DQS_L7 AE15
MEM_MA_DQS_H6 AG18
MEM_MA_DQS_L6 AG19
MEM_MA_DQS_H5 AG24
MEM_MA_DQS_L5 AG25
MEM_MA_DQS_H4 AG27
MEM_MA_DQS_L4 AG28
MEM_MA_DQS_H3 C29
MEM_MA_DQS_L3 C25
MEM_MA_DQS_H2 C29
MEM_MA_DQS_L2 D25
MEM_MA_DQS_H1 E19
MEM_MA_DQS_L1 F19
MEM_MA_DQS_H0 F15
MEM_MA_DQS_L0 G15
MEM_MA_DM7 AE15
MEM_MA_DM6 AE19
MEM_MA_DM5 AH29
MEM_MA_DM3 B29
MEM_MA_DM2 E24
MEM_MA_DM1 E18
MEM_MA_DM0 H15
MA0_CLK_H(2) AG21
MA0_CLK_L(2) AG20
MA0_CLK_H(1) H19
MA0_CLK_L(1) U27
MA0_CLK_H(0) U26
MA0_CLK_L(0) U26
MA0_CS_L(1) AC25
MA0_CS_L(0) AA24
MA0_ODT(0) AC28
MA1_CLK_H(2) AE20
MA1_CLK_L(2) G20
MA1_CLK_H(1) G21
MA1_CLK_L(1) U27
MA1_CLK_H(0) V27
MA1_CLK_L(0) W27
MA1_CS_L(1) AD27
MA1_CS_L(0) AA25
MA1_ODT(0) AC27
MA_CAS_L AB25
MA_WE_L AB27
MA_RAS_L AA26
MA_BANK(2) N25
MA_BANK(1) Y27
MA_BANK(0) AA27
MA_CKE(1) L27
MA_CKE(0) M25
MA_ADD(15) M27
MA_ADD(14) N24
MA_ADD(13) AC26
MA_ADD(12) N26
MA_ADD(11) P25
MA_ADD(10) Y25
MA_ADD(9) N27
MA_ADD(8) R24
MA_ADD(7) P27
MA_ADD(6) R25
MA_ADD(5) R26
MA_ADD(4) R27
MA_ADD(3) T25
MA_ADD(2) U25
MA_ADD(1) T27
MA_ADD(0) W24
MA_DQS_H(7) AD15
MA_DQS_L(7) AE15
MA_DQS_H(6) AG18
MA_DQS_L(6) AG19
MA_DQS_H(5) AG24
MA_DQS_L(5) AG25
MA_DQS_H(4) AG27
MA_DQS_L(4) AG28
MA_DQS_H(3) C29
MA_DQS_L(3) C25
MA_DQS_H(2) C29
MA_DQS_L(2) D25
MA_DQS_H(1) E19
MA_DQS_L(1) F19
MA_DQS_H(0) F15
MA_DQS_L(0) G15
MA_DM(7) AE15
MA_DM(6) AE19
MA_DM(5) AH29
MA_DM(3) B29
MA_DM(2) E24
MA_DM(1) E18
MA_DM(0) H15
MA_DATA(63) AE14
MA_DATA(62) AG14
MA_DATA(61) AG16
MA_DATA(60) AD17
MA_DATA(59) AD13
MA_DATA(58) AE13
MA_DATA(57) AG15
MA_DATA(56) AE16
MA_DATA(55) AG17
MA_DATA(54) AE18
MA_DATA(53) AD21
MA_DATA(52) AG22
MA_DATA(51) AE17
MA_DATA(50) AG20
MA_DATA(49) AE21
MA_DATA(48) AE21
MA_DATA(47) AE23
MA_DATA(46) AE23
MA_DATA(45) AG26
MA_DATA(44) AE22
MA_DATA(43) AG23
MA_DATA(42) AG23
MA_DATA(41) AH25
MA_DATA(40) AE25
MA_DATA(39) AJ28
MA_DATA(38) AJ29
MA_DATA(37) AE29
MA_DATA(36) AE26
MA_DATA(35) AJ27
MA_DATA(34) AH27
MA_DATA(33) AG29
MA_DATA(32) AE27
MA_DATA(31) E29
MA_DATA(30) E28
MA_DATA(29) D27
MA_DATA(28) C27
MA_DATA(27) G26
MA_DATA(26) F27
MA_DATA(25) C28
MA_DATA(24) E27
MA_DATA(23) F25
MA_DATA(22) E25
MA_DATA(21) E23
MA_DATA(20) D23
MA_DATA(19) E26
MA_DATA(18) C26
MA_DATA(17) G23
MA_DATA(16) F23
MA_DATA(15) E22
MA_DATA(14) E21
MA_DATA(13) F17
MA_DATA(12) G17
MA_DATA(11) G22
MA_DATA(10) F21
MA_DATA(9) G18
MA_DATA(8) E17
MA_DATA(7) G16
MA_DATA(6) E15
MA_DATA(5) G13
MA_DATA(4) H13
MA_DATA(3) H12
MA_DATA(2) E14
MA_DATA(1) G14
MA_DATA(0) G14
MA_DQS_H(8) J28
MA_DQS_L(8) J27
MA_DM(8) J25
MA_CHECK(7) K25
MA_CHECK(6) J26
MA_CHECK(5) G27
MA_CHECK(4) G27
MA_CHECK(3) I24
MA_CHECK(2) K27
MA_CHECK(1) H29
MA_CHECK(0) H27

CPU1C

12,13 MEM_MB0_CLK_H2 >> MEM_MB0_CLK_H2 AJ19
12,13 MEM_MB0_CLK_L2 >> MEM_MB0_CLK_L2 AK19
12,13 MEM_MB0_CLK_H1 >> MEM_MB0_CLK_H1 AJ18
12,13 MEM_MB0_CLK_L1 >> MEM_MB0_CLK_L1 AJ19
12,13 MEM_MB0_CS_L1 >> MEM_MB0_CS_L1 AE30
12,13 MEM_MB0_CS_L0 >> MEM_MB0_CS_L0 AC31
12,13 MEM_MB0_ODT0 >> MEM_MB0_ODT0 AD29
12,13 MEM_MB1_ODT0 >> MEM_MB1_ODT0 AD31
12,13 MEM_MB_CAS_L >> MEM_MB_CAS_L AC29
12,13 MEM_MB_WE_L >> MEM_MB_WE_L AC30
12,13 MEM_MB_RAS_L >> MEM_MB_RAS_L AB29
12,13 MEM_MB_BANK2 >> MEM_MB_BANK2 N31
12,13 MEM_MB_BANK1 >> MEM_MB_BANK1 AA31
12,13 MEM_MB_BANK0 >> MEM_MB_BANK0 AA28
12,13 MEM_MB_CKE1 >> MEM_MB_CKE1 M31
12,13 MEM_MB_CKE0 >> MEM_MB_CKE0 M29
MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R28
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30
MEM_MB_DQS_H7 AK13
MEM_MB_DQS_L7 AJ13
MEM_MB_DQS_H6 AK17
MEM_MB_DQS_L6 AJ17
MEM_MB_DQS_H5 AK23
MEM_MB_DQS_L5 AL23
MEM_MB_DQS_H4 AL28
MEM_MB_DQS_L4 D31
MEM_MB_DQS_H3 C31
MEM_MB_DQS_L2 C24
MEM_MB_DQS_H1 C23
MEM_MB_DQS_L1 D17
MEM_MB_DQS_H0 C14
MEM_MB_DQS_L0 C13
MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13
MB0_CLK_H(2) AJ19
MB0_CLK_L(2) AK19
MB0_CLK_H(1) AJ18
MB0_CLK_L(1) AJ19
MB0_CLK_H(0) U31
MB0_CLK_L(0) U30
MB0_CS_L(1) AE30
MB0_CS_L(0) AC31
MB0_ODT(0) AD29
MB1_CLK_H(2) AL19
MB1_CLK_L(2) C19
MB1_CLK_H(1) D19
MB1_CLK_L(1) W29
MB1_CLK_H(0) W28
MB1_CLK_L(0) W28
MB1_CS_L(1) AE29
MB1_CS_L(0) AB31
MB1_ODT(0) AD31
MB_CAS_L AC29
MB_WE_L AC30
MB_RAS_L AB29
MB_BANK(2) N31
MB_BANK(1) AA31
MB_BANK(0) AA28
MB_CKE(1) M31
MB_CKE(0) M29
MB_ADD(15) N28
MB_ADD(14) N29
MB_ADD(13) AE31
MB_ADD(12) N30
MB_ADD(11) P29
MB_ADD(10) AA29
MB_ADD(9) P31
MB_ADD(8) R28
MB_ADD(7) R28
MB_ADD(6) R31
MB_ADD(5) R30
MB_ADD(4) T31
MB_ADD(3) T29
MB_ADD(2) U29
MB_ADD(1) U28
MB_ADD(0) AA30
MB_DQS_H(7) AK13
MB_DQS_L(7) AJ13
MB_DQS_H(6) AK17
MB_DQS_L(6) AJ17
MB_DQS_H(5) AK23
MB_DQS_L(5) AL23
MB_DQS_H(4) AL28
MB_DQS_L(4) D31
MB_DQS_H(3) C31
MB_DQS_L(2) C24
MB_DQS_H(1) C23
MB_DQS_L(1) D17
MB_DQS_H(0) C14
MB_DQS_L(0) C13
MB_DM(7) AJ14
MB_DM(6) AH17
MB_DM(5) AJ23
MB_DM(4) AK29
MB_DM(3) C30
MB_DM(2) A23
MB_DM(1) B17
MB_DM(0) B13
MB_DATA(63) AH13
MB_DATA(62) AL13
MB_DATA(61) AL15
MB_DATA(60) AJ15
MB_DATA(59) AE13
MB_DATA(58) AG13
MB_DATA(57) AL14
MB_DATA(56) AK15
MB_DATA(55) AL16
MB_DATA(54) AK21
MB_DATA(53) AK21
MB_DATA(52) AL21
MB_DATA(51) AL16
MB_DATA(50) AH19
MB_DATA(49) AL20
MB_DATA(48) AJ22
MB_DATA(47) AL22
MB_DATA(46) AL24
MB_DATA(45) AK25
MB_DATA(44) AJ21
MB_DATA(43) AH21
MB_DATA(42) AH23
MB_DATA(41) AL24
MB_DATA(40) AL27
MB_DATA(39) AK27
MB_DATA(38) AH31
MB_DATA(37) AG30
MB_DATA(36) AJ25
MB_DATA(35) N31
MB_DATA(34) AJ30
MB_DATA(33) AJ31
MB_DATA(32) E31
MB_DATA(31) E30
MB_DATA(30) B27
MB_DATA(29) A27
MB_DATA(28) F29
MB_DATA(27) F29
MB_DATA(26) F31
MB_DATA(25) A28
MB_DATA(24) A25
MB_DATA(23) A24
MB_DATA(22) D22
MB_DATA(21) C21
MB_DATA(20) D21
MB_DATA(19) B25
MB_DATA(18) B23
MB_DATA(17) A22
MB_DATA(16) B21
MB_DATA(15) A20
MB_DATA(14) C16
MB_DATA(13) D15
MB_DATA(12) C21
MB_DATA(11) A21
MB_DATA(10) A17
MB_DATA(9) A16
MB_DATA(8) B15
MB_DATA(7) A14
MB_DATA(6) A14
MB_DATA(5) F13
MB_DATA(4) C15
MB_DATA(3) A15
MB_DATA(2) A13
MB_DATA(1) D13
MB_DATA(0) J31
MB_DQS_H(8) J30
MB_DQS_L(8) J29
MB_DM(8) J29
MB_CHECK(7) K29
MB_CHECK(6) K31
MB_CHECK(5) G30
MB_CHECK(4) G29
MB_CHECK(3) L29
MB_CHECK(2) L28
MB_CHECK(1) H31
MB_CHECK(0) G31

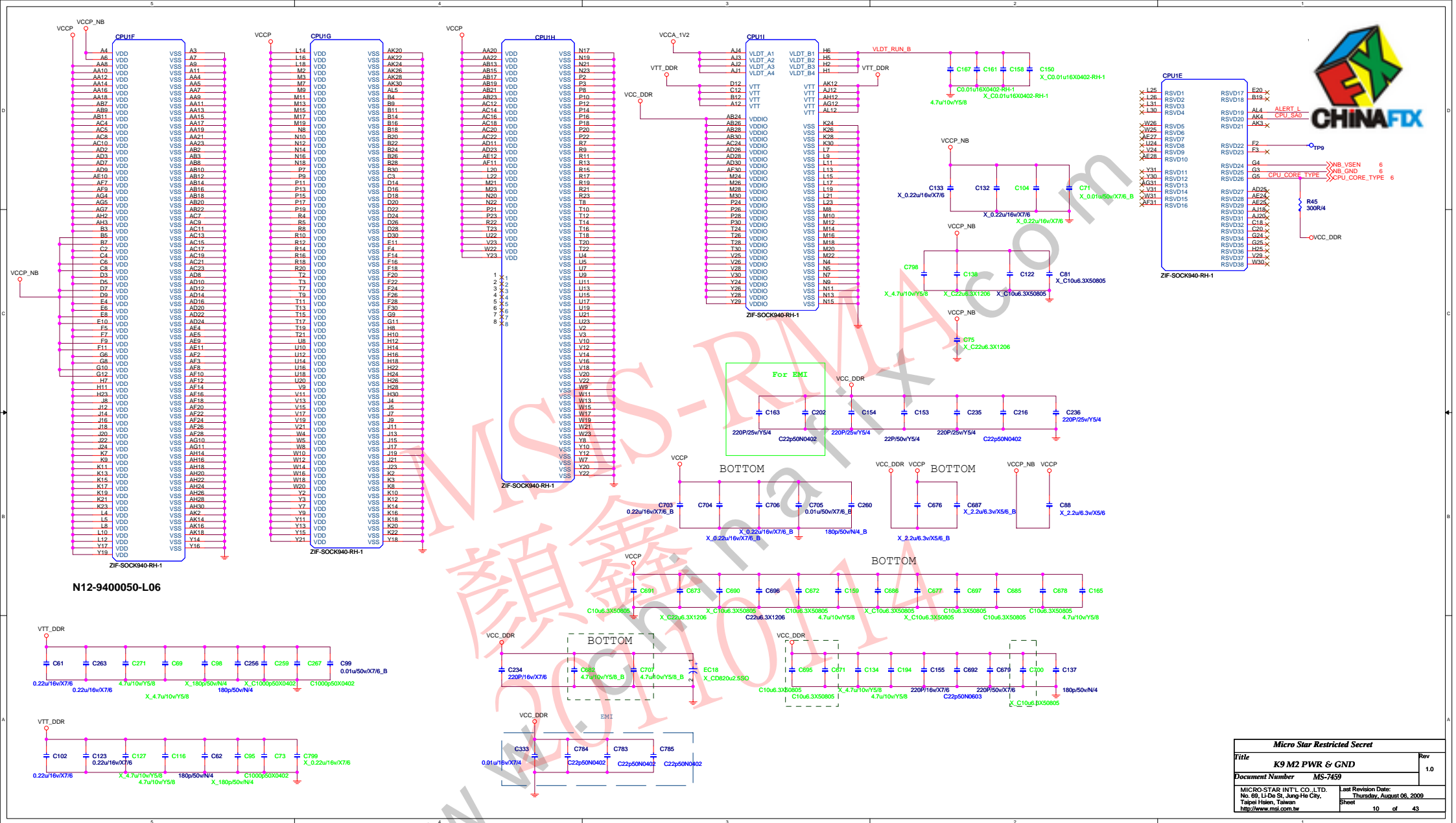
Impedance:MEM CLK
• Impedance = 100 Ω \pm 15% differential.
• Reference to a solid GND plane.

Impedance:Data or Data Mask or Strobes
• Data, Data Mask: 50 Ω \pm 15% single ended impedance
• Data Strobes: 100 Ω \pm 15% differential impedance
• Reference to a solid GND plane

Impedance:Address, Command or Control
• Impedance = 50 Ω \pm 15%
• Reference to a solid GND plane

ZIF-SOCK940-RH-1

Micro Star Restricted Secret	
Title	Rev
K9 M2 DDR MEMORY I/F	1.0
Document Number	MS-7459
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	
Last Revision Date: Thursday, August 06, 2009	
Sheet	9 of 43



Micro Star Restricted Secret		
Title	K9 M2 PWR & GND	Rev 1.0
Document Number	MS-7459	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-He City, Taippei Hsien, Taiwan		Last Revision Date: Thursday, August 06, 2009
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DDR2 SODIMM A0

ADDR=1010000B

9 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
9 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
9 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
9,13 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
9 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

MEM_MA_DATA0	5	DQ0	102	MEM_MA_ADD0
MEM_MA_DATA1	7	DQ1	101	MEM_MA_ADD1
MEM_MA_DATA2	17	DQ2	100	MEM_MA_ADD2
MEM_MA_DATA3	19	DQ3	99	MEM_MA_ADD3
MEM_MA_DATA4	4	DQ4	98	MEM_MA_ADD4
MEM_MA_DATA5	6	DQ5	97	MEM_MA_ADD5
MEM_MA_DATA6	14	DQ6	94	MEM_MA_ADD6
MEM_MA_DATA7	16	DQ7	92	MEM_MA_ADD7
MEM_MA_DATA8	23	DQ8	93	MEM_MA_ADD8
MEM_MA_DATA9	25	DQ9	91	MEM_MA_ADD9
MEM_MA_DATA10	35	DQ10	105	MEM_MA_ADD10
MEM_MA_DATA11	37	DQ11	90	MEM_MA_ADD11
MEM_MA_DATA12	20	DQ12	89	MEM_MA_ADD12
MEM_MA_DATA13	22	DQ13	116	MEM_MA_ADD13
MEM_MA_DATA14	36	DQ14	86	MEM_MA_ADD14
MEM_MA_DATA15	38	DQ15	84	MEM_MA_ADD15
MEM_MA_DATA16	43	DQ16	85	MEM_MA_BANK2
MEM_MA_DATA17	45	DQ17	107	MEM_MA_BANK0
MEM_MA_DATA18	55	DQ18	106	MEM_MA_BANK1
MEM_MA_DATA19	57	DQ19	110	MEM_MA0_CS_L0
MEM_MA_DATA20	44	DQ20	115	MEM_MA0_CS_L1
MEM_MA_DATA21	46	DQ21	30	MEM_MA0_CLK_H1
MEM_MA_DATA22	56	DQ22	32	MEM_MA0_CLK_L1
MEM_MA_DATA23	58	DQ23	164	MEM_MA0_CLK_H2
MEM_MA_DATA24	61	DQ24	166	MEM_MA0_CLK_L2
MEM_MA_DATA25	63	DQ25	79	MEM_MA_CKE0
MEM_MA_DATA26	73	DQ26	80	MEM_MA_CKE1
MEM_MA_DATA27	75	DQ27	113	MEM_MA_CAS_L
MEM_MA_DATA28	62	DQ28	108	MEM_MA_RAS_L
MEM_MA_DATA29	64	DQ29	109	MEM_MA_WE_L
MEM_MA_DATA30	74	DQ30	198	SA_SAO
MEM_MA_DATA31	76	DQ31	200	SA_SAT
MEM_MA_DATA32	123	DQ32	197	SCL0
MEM_MA_DATA33	125	DQ33	195	SDA0
MEM_MA_DATA34	135	DQ34	114	MEM_MA0_ODT0
MEM_MA_DATA35	137	DQ35	119	MEM_MA1_ODT0
MEM_MA_DATA36	124	DQ36	10	MEM_MA_DM0
MEM_MA_DATA37	126	DQ37	26	MEM_MA_DM1
MEM_MA_DATA38	134	DQ38	52	MEM_MA_DM2
MEM_MA_DATA39	136	DQ39	67	MEM_MA_DM3
MEM_MA_DATA40	141	DQ40	130	MEM_MA_DM4
MEM_MA_DATA41	143	DQ41	147	MEM_MA_DM5
MEM_MA_DATA42	151	DQ42	170	MEM_MA_DM6
MEM_MA_DATA43	153	DQ43	185	MEM_MA_DM7
MEM_MA_DATA44	140	DQ44		
MEM_MA_DATA45	142	DQ45		
MEM_MA_DATA46	152	DQ46		
MEM_MA_DATA47	154	DQ47		
MEM_MA_DATA48	157	DQ48		
MEM_MA_DATA49	159	DQ49		
MEM_MA_DATA50	173	DQ50		
MEM_MA_DATA51	175	DQ51		
MEM_MA_DATA52	158	DQ52		
MEM_MA_DATA53	160	DQ53		
MEM_MA_DATA54	174	DQ54		
MEM_MA_DATA55	176	DQ55		
MEM_MA_DATA56	181	DQ56		
MEM_MA_DATA57	179	DQ57		
MEM_MA_DATA58	180	DQ58		
MEM_MA_DATA59	191	DQ59		
MEM_MA_DATA60	180	DQ60		
MEM_MA_DATA61	182	DQ61		
MEM_MA_DATA62	192	DQ62		
MEM_MA_DATA63	194	DQ63		

DIMM1A

DDR2_SO-DIMM_STD

VCC3

R238 X 2.7K R0402 PM_EXTTS#0

VCC3

C627

X 2.2U6.3Y

C624

0.1U10X0402

VCC3

C631

2.2U6.3Y

C632

0.1U10X0402

VCC3

D18

X 1PS226_SOT23

VCC3

D20

X 1PS226_SOT23

VCC_DDR

R58

15R/4/1%

R68

15R/4/1%

C488

0.1U10X0402

as close as SO-DIMM

SMDR_VREF

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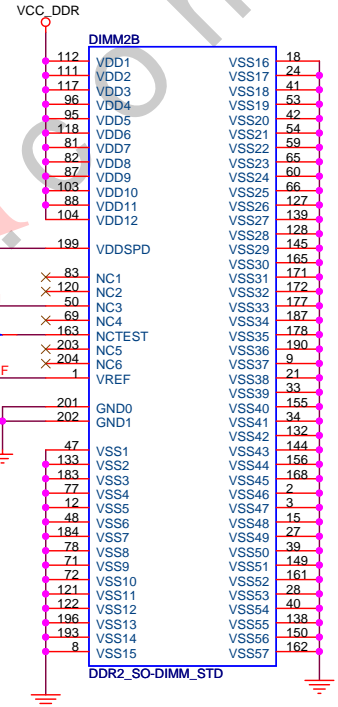
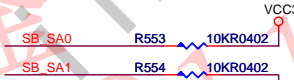
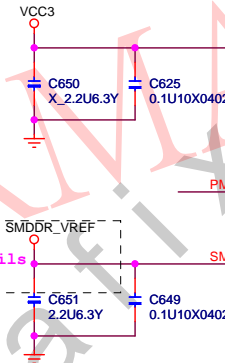
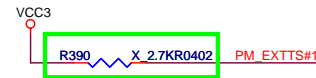
DDRII SODIMM B0

ADDR=1010010B

9 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
 9 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
 9 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
 9,13 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
 9 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

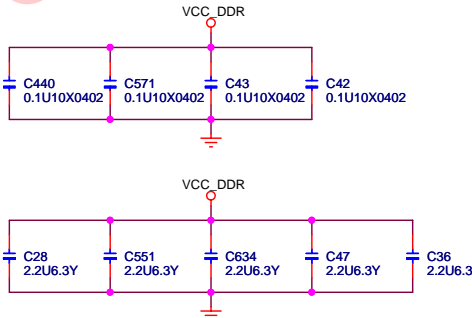
DIMM2A			
MEM_MB_DATA0	5	DO0	A0
MEM_MB_DATA1	7	DO1	A1
MEM_MB_DATA2	17	DO2	A2
MEM_MB_DATA3	19	DO3	A3
MEM_MB_DATA4	4	DO4	A4
MEM_MB_DATA5	6	DO5	A5
MEM_MB_DATA6	14	DO6	A6
MEM_MB_DATA7	16	DO7	A7
MEM_MB_DATA8	23	DO8	A8
MEM_MB_DATA9	25	DO9	A9
MEM_MB_DATA10	35	DO10	A10/AP
MEM_MB_DATA11	37	DO11	A11
MEM_MB_DATA12	20	DO12	A12
MEM_MB_DATA13	22	DO13	A13
MEM_MB_DATA14	36	DO14	A14
MEM_MB_DATA15	38	DO15	A15
MEM_MB_DATA16	43	DO16	A16_BA2
MEM_MB_DATA17	45	DO17	
MEM_MB_DATA18	55	DO18	BA0
MEM_MB_DATA19	57	DO19	BA1
MEM_MB_DATA20	44	DO20	SO#
MEM_MB_DATA21	46	DO21	S1#
MEM_MB_DATA22	56	DO22	CK0#
MEM_MB_DATA23	58	DO23	CK1#
MEM_MB_DATA24	61	DO24	CK2#
MEM_MB_DATA25	63	DO25	CKE0
MEM_MB_DATA26	73	DO26	CKE1
MEM_MB_DATA27	75	DO27	CKE2
MEM_MB_DATA28	62	DO28	CAS#
MEM_MB_DATA29	64	DO29	RAS#
MEM_MB_DATA30	74	DO30	WE#
MEM_MB_DATA31	76	DO31	SA0
MEM_MB_DATA32	123	DO32	SA1
MEM_MB_DATA33	125	DO33	SCL
MEM_MB_DATA34	135	DO34	SDA
MEM_MB_DATA35	137	DO35	
MEM_MB_DATA36	124	DO36	ODT0
MEM_MB_DATA37	126	DO37	ODT1
MEM_MB_DATA38	134	DO38	
MEM_MB_DATA39	136	DO39	DM0
MEM_MB_DATA40	141	DO40	DM1
MEM_MB_DATA41	143	DO41	DM2
MEM_MB_DATA42	151	DO42	DM3
MEM_MB_DATA43	153	DO43	DM4
MEM_MB_DATA44	140	DO44	DM5
MEM_MB_DATA45	142	DO45	DM6
MEM_MB_DATA46	152	DO46	DM7
MEM_MB_DATA47	154	DO47	
MEM_MB_DATA48	157	DO48	DQS0
MEM_MB_DATA49	159	DO49	DQS1
MEM_MB_DATA50	173	DO50	DQS2
MEM_MB_DATA51	175	DO51	DQS3
MEM_MB_DATA52	158	DO52	DQS4
MEM_MB_DATA53	160	DO53	DQS5
MEM_MB_DATA54	174	DO54	DQS6
MEM_MB_DATA55	176	DO55	DQS7
MEM_MB_DATA56	179	DO56	DQS8
MEM_MB_DATA57	181	DO57	DQS9
MEM_MB_DATA58	189	DO58	DQS10
MEM_MB_DATA59	191	DO59	DQS11
MEM_MB_DATA60	180	DO60	DQS12
MEM_MB_DATA61	182	DO61	DQS13
MEM_MB_DATA62	192	DO62	DQS14
MEM_MB_DATA63	194	DO63	DQS15

DDR2_SO-DIMM_STD

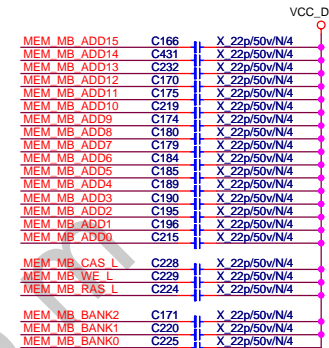
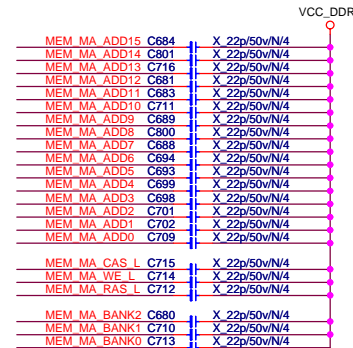
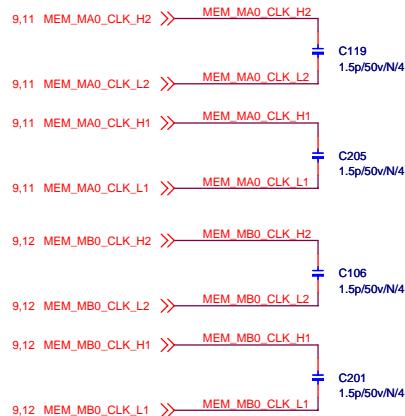


ADDRESS: 001
0xA2

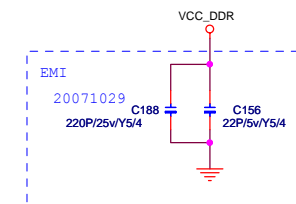
Layout note: Place capacitors between and near DDR connector if possible.



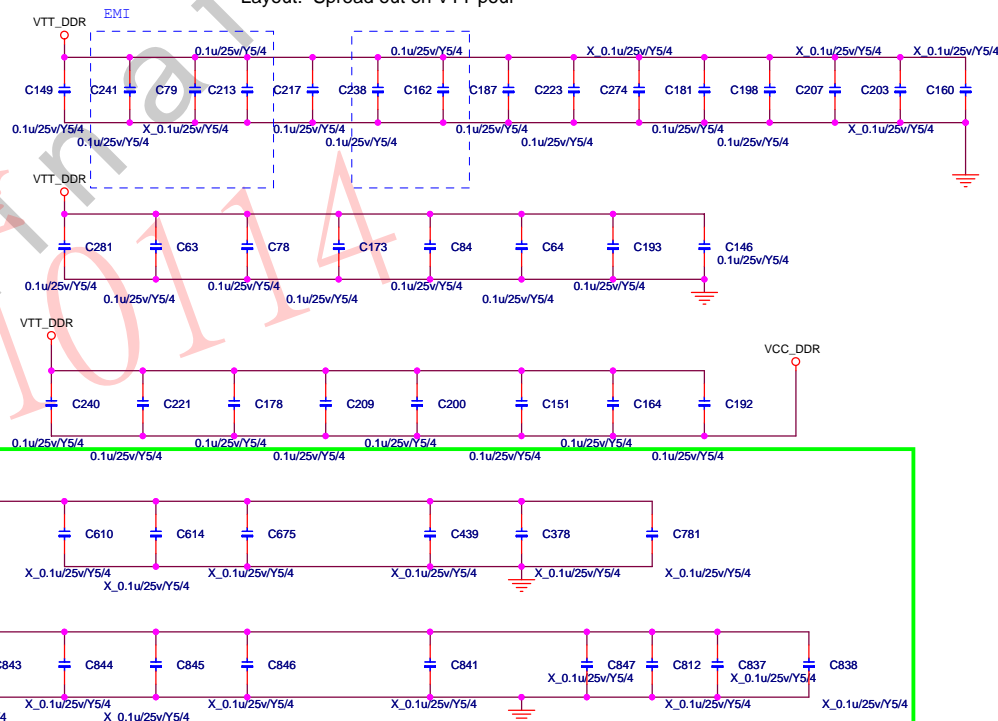
Micro Star Restricted Secret		
Title	DDR SO-DIMM2	Rev 1.0
Document Number	MS-7459	
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, August 06, 2009 Sheet 12 of 43



Decoupling Between Processor and DIMMs

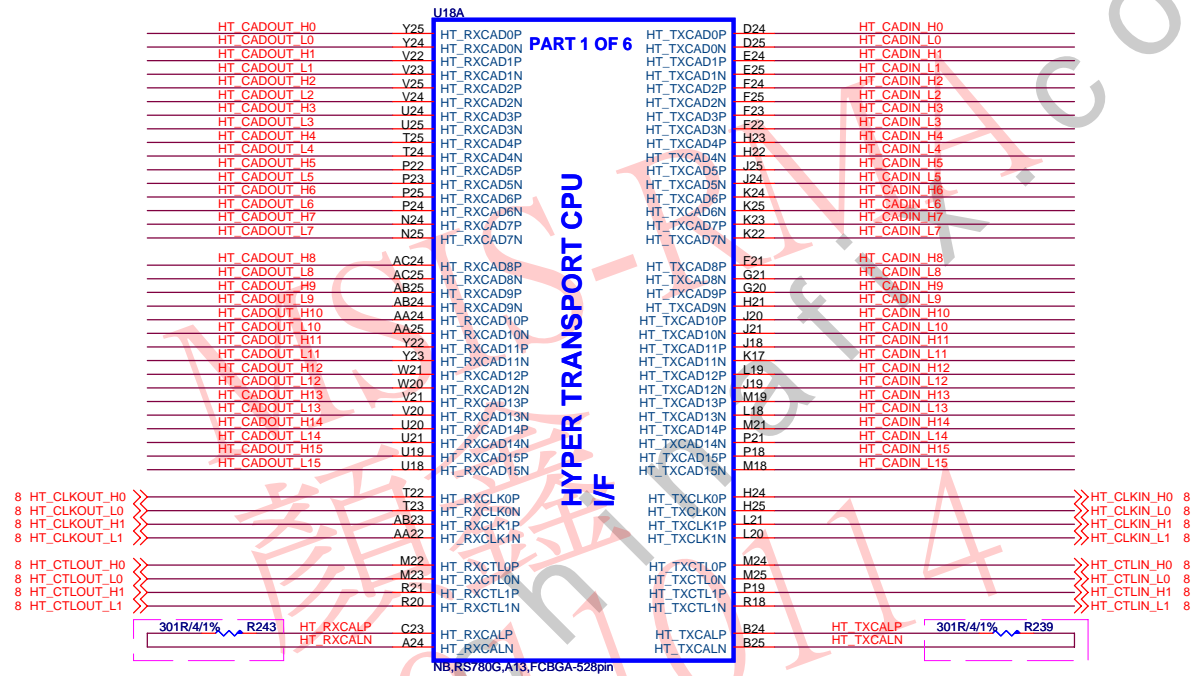


Layout: Spread out on VTT pour



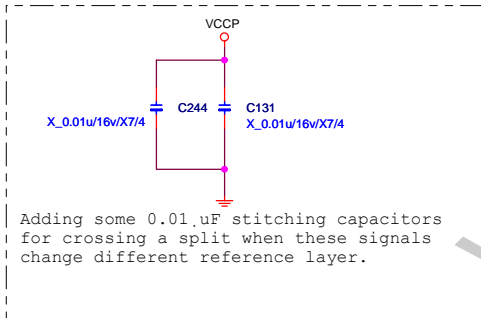
8 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
8 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

8 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
8 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]



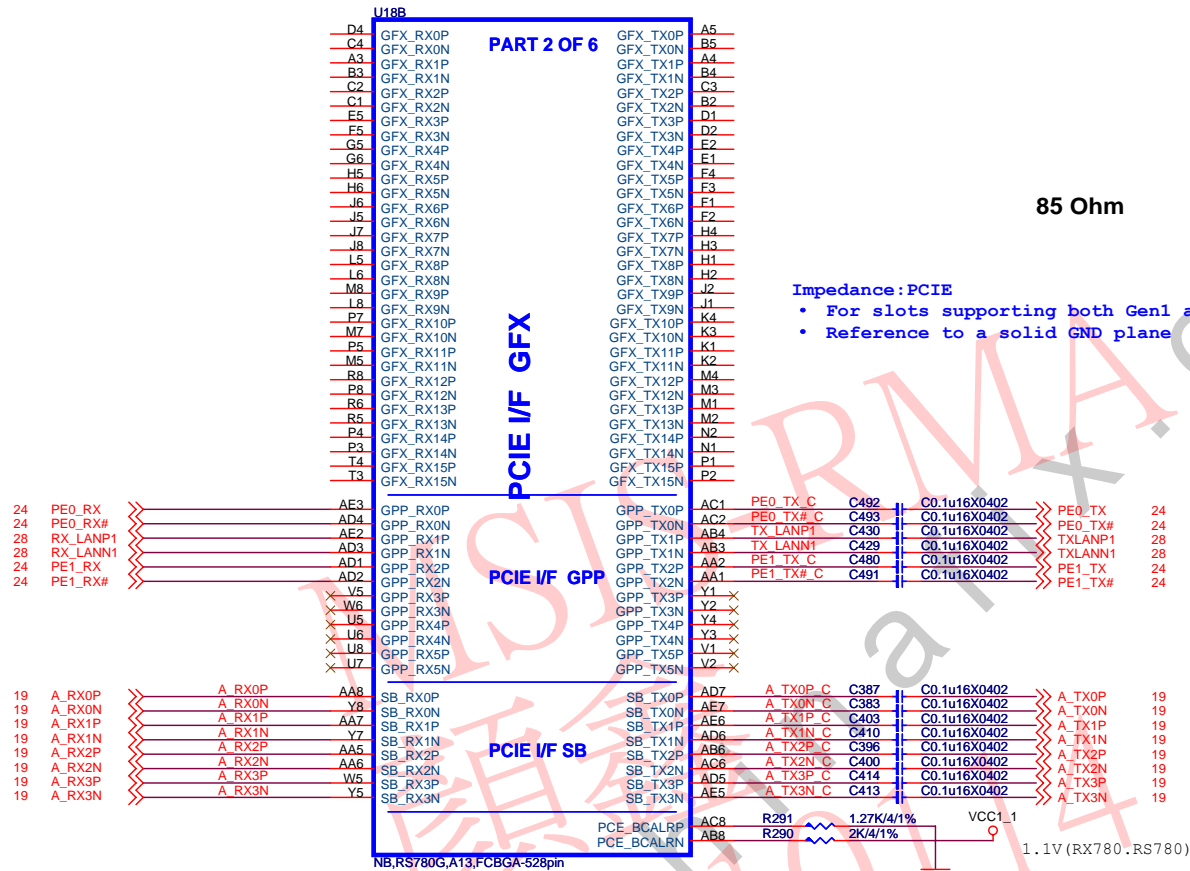
RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)	1.21K	301R
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



MICRO-STAR IN'L CO., LTD.

Title			RS780-HT L
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RX780/RS740/RS780 GPP difference table

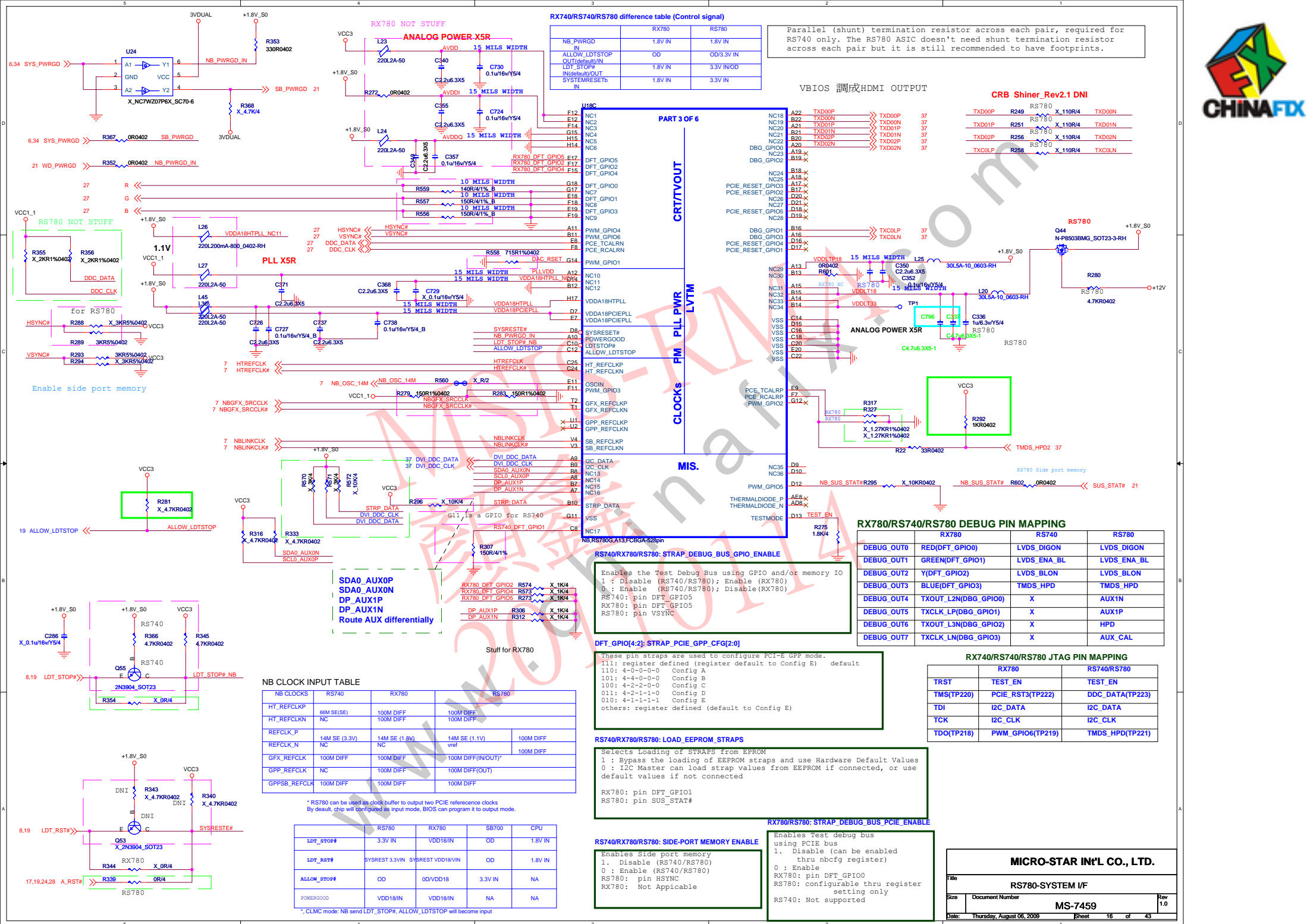
	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

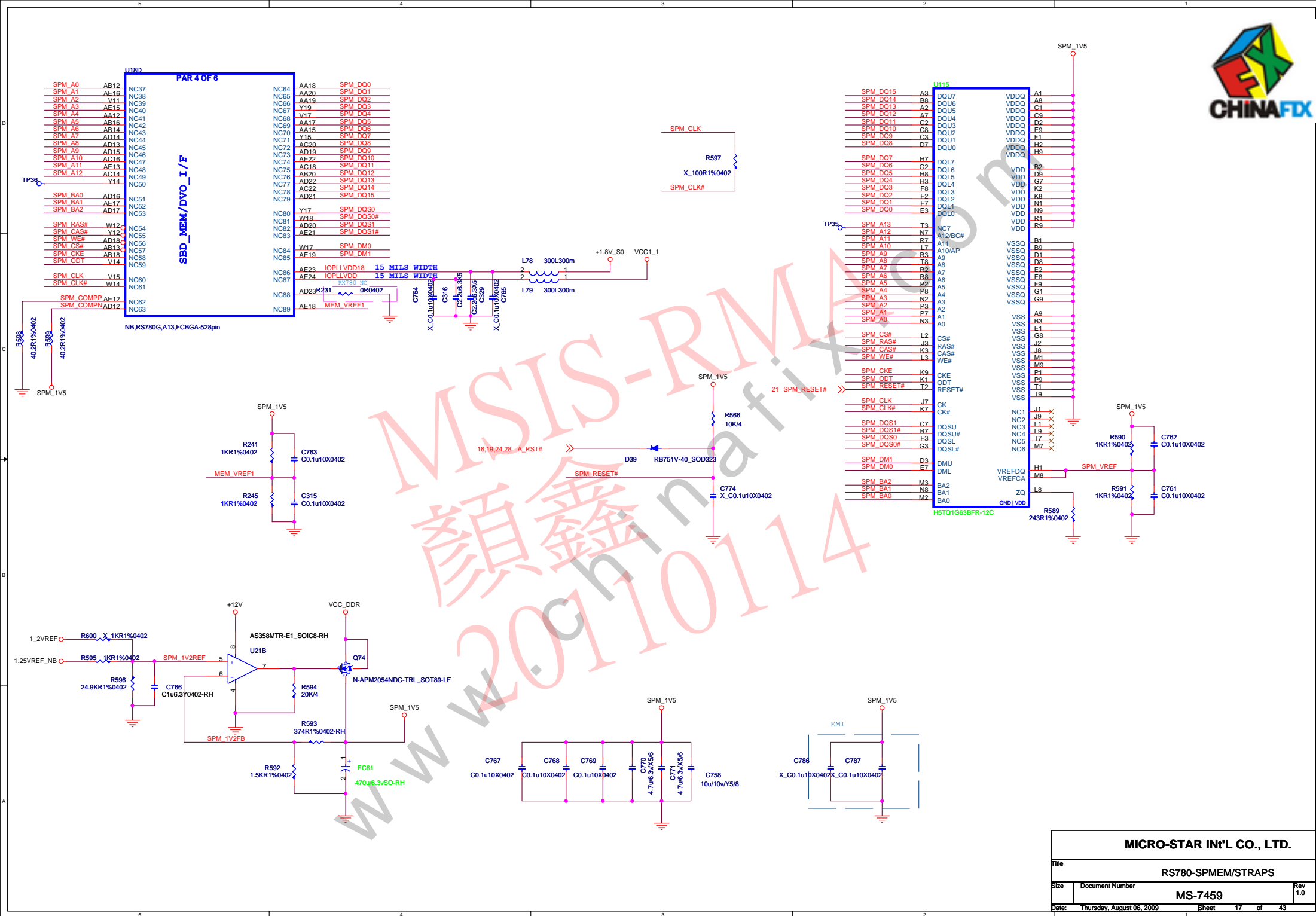
RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

MICRO-STAR INT'L CO., LTD.

Title RS780-PCIE I/F		
Size	Document Number MS-7459	Rev 1.0
Date:	Thursday, August 06, 2009	Sheet 15 of 43

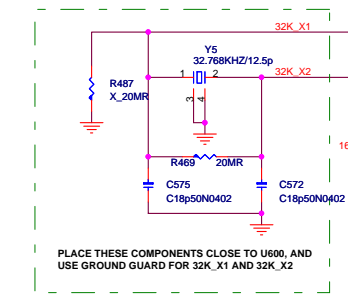




100 Ohm

Impedance: A-LINK
 • 100 $\Omega \pm 15\%$ differential
 • Reference to a solid GND plane

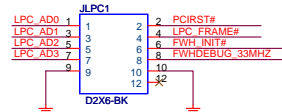
100 Ohm



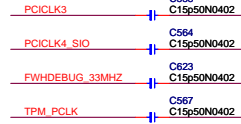
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

SB700-A12FCBGA-528pin
B01-SB70035-A08

LPC Debug Port



For EMI



Impedance: LPC & PCI CLOCK
 • 60 $\Omega \pm 15\%$
 • Reference to a solid GND or PWR plane.

Adding some 0.1 μ F stitching capacitors for crossing a split when these signals change different reference layer.

PCI PULL-UP / DOWN RESISTORS

Impedance: PCI
 • 60 $\Omega \pm 15\%$
 • Reference to a solid GND or PWR plane.

Shiner_Rev2.3c

Impedance: LPC
 • 60 $\Omega \pm 15\%$
 • Reference to a solid GND or PWR plane.



MICRO-STAR INT'L CO., LTD.

SB700-PCIE/PCI/CPU/LPC

MS-7459

Title		
SB700-PCIE/PCI/CPU/LPC		
Size	Document Number	Rev
		1.0
Date:	Thursday, August 06, 2009	Sheet 19 of 43

SATA HDD

SATA CDROM/DVD

E-SATA

the signal pairs are not longer than 4-inches.

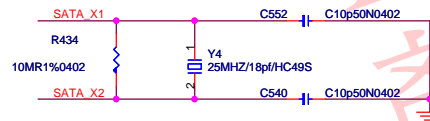
SATA 90 Ohm

Impedance:

- 90-Ω ± 10% differential
- Reference to a solid GND (not PWR) plane.

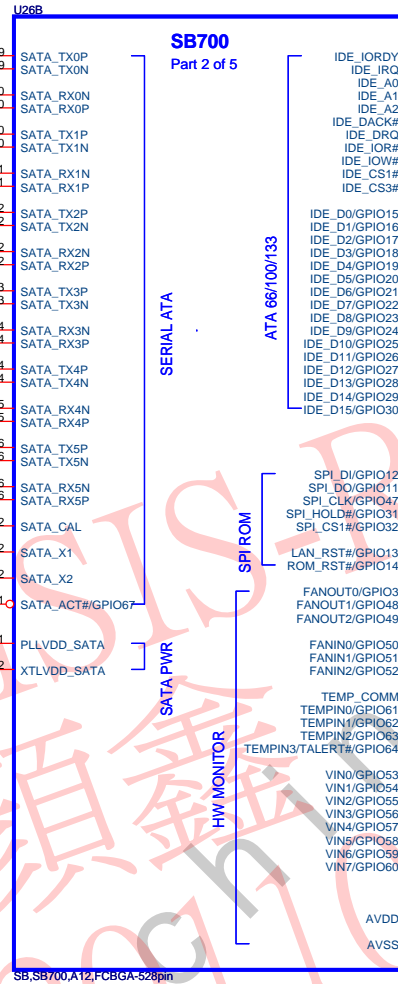
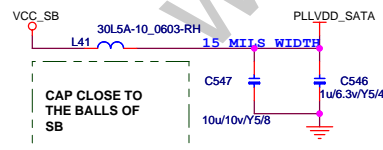
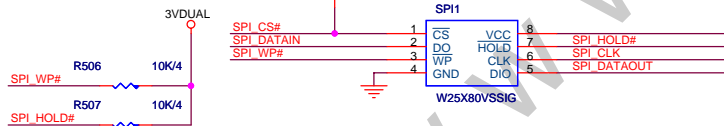
R272 IS 1K 1% FOR XTAL,
4.99K 1% FOR INTERNAL CLK

N5N-07M0231-H06



Impedance:SPI

- 60 Ω ± 15%.
- Reference to a solid GND or PWR plane.

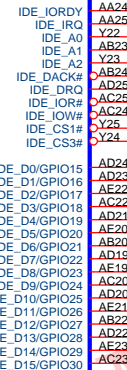


SERIAL ATA

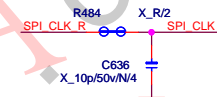
SATA PWR

HW MONITOR

SB,SB700,A12,PC8GA-528pin



Reserved for EMI 0906



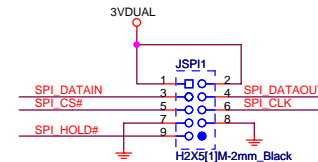
TEMP_COMM
connect to GND
for AMD recommend

TALERT# 8.30

SPI FLASH MEMORY

SPI DEBUG PORT

Place close to SPI ROM



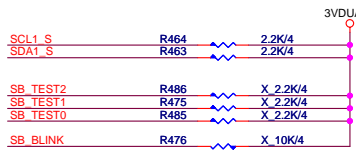
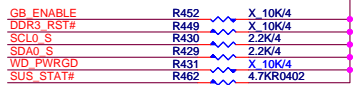
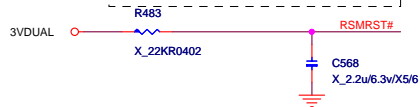
Part Number : N31-2051451-H06

MICRO-STAR INT'L CO., LTD.

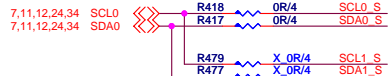
Title			SB700-SATA/IDE/HWM/SPI
Size	Document Number	MS-7459	Rev 1.0
Date:	Thursday, August 06, 2009	Sheet	20 of 43



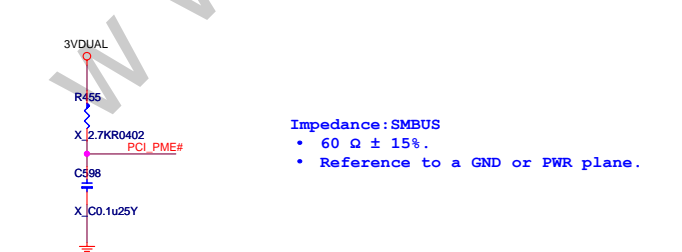
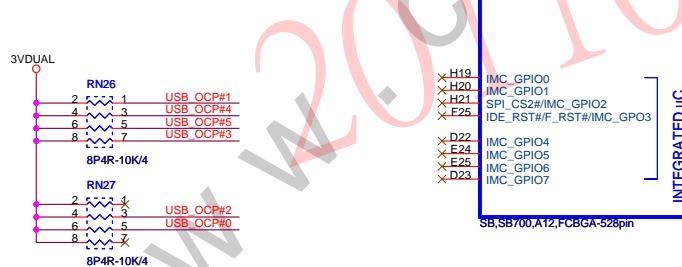
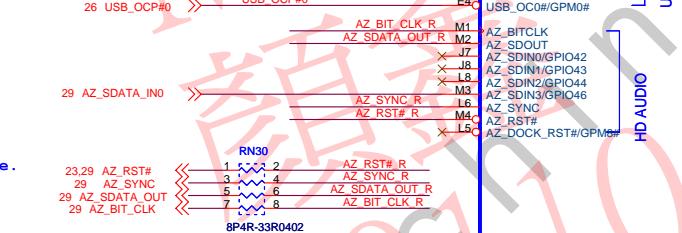
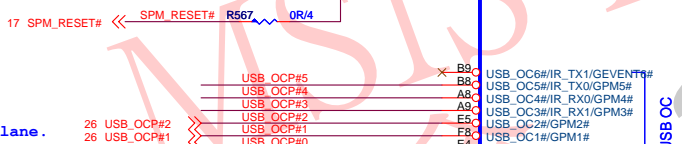
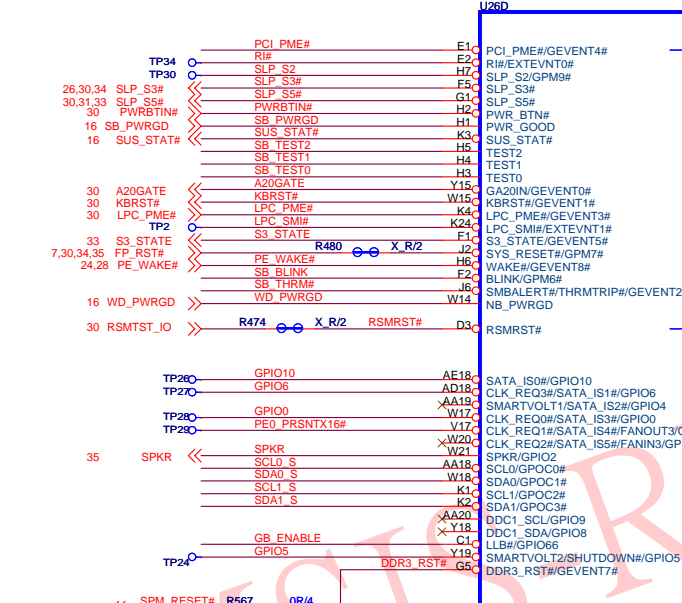
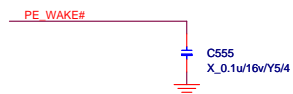
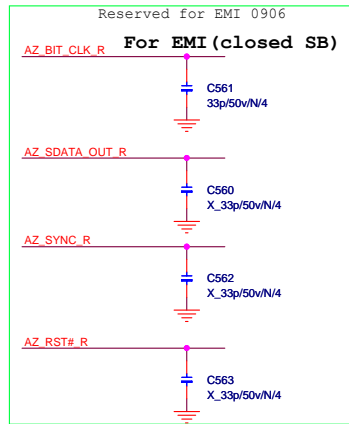
Cap have been unpopulate for meet power sequence



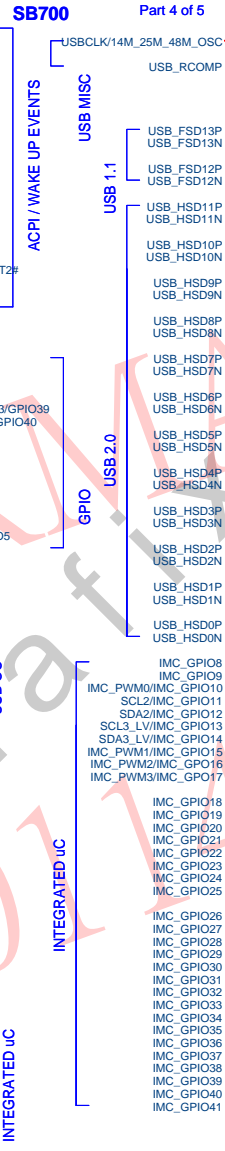
Impedance:USB OC
• 60 Ω \pm 15%
• Reference to a GND or PWR plane.



Impedance:HD AUDIO
• 60 Ω \pm 15%
• Reference to a solid GND or PWR plane.



Impedance:SMBUS
• 60 Ω \pm 15%
• Reference to a GND or PWR plane.

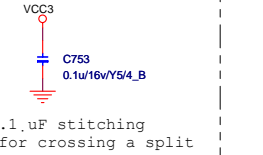


SB700 Pin C8 USBCLK/14M_25M_48M_OSC
Function set output pin by BIOS.

Impedance:USB RCOMP
• 35 Ω \pm 15%
• Reference to the (GND) or USB PWR plane

90 Ohm

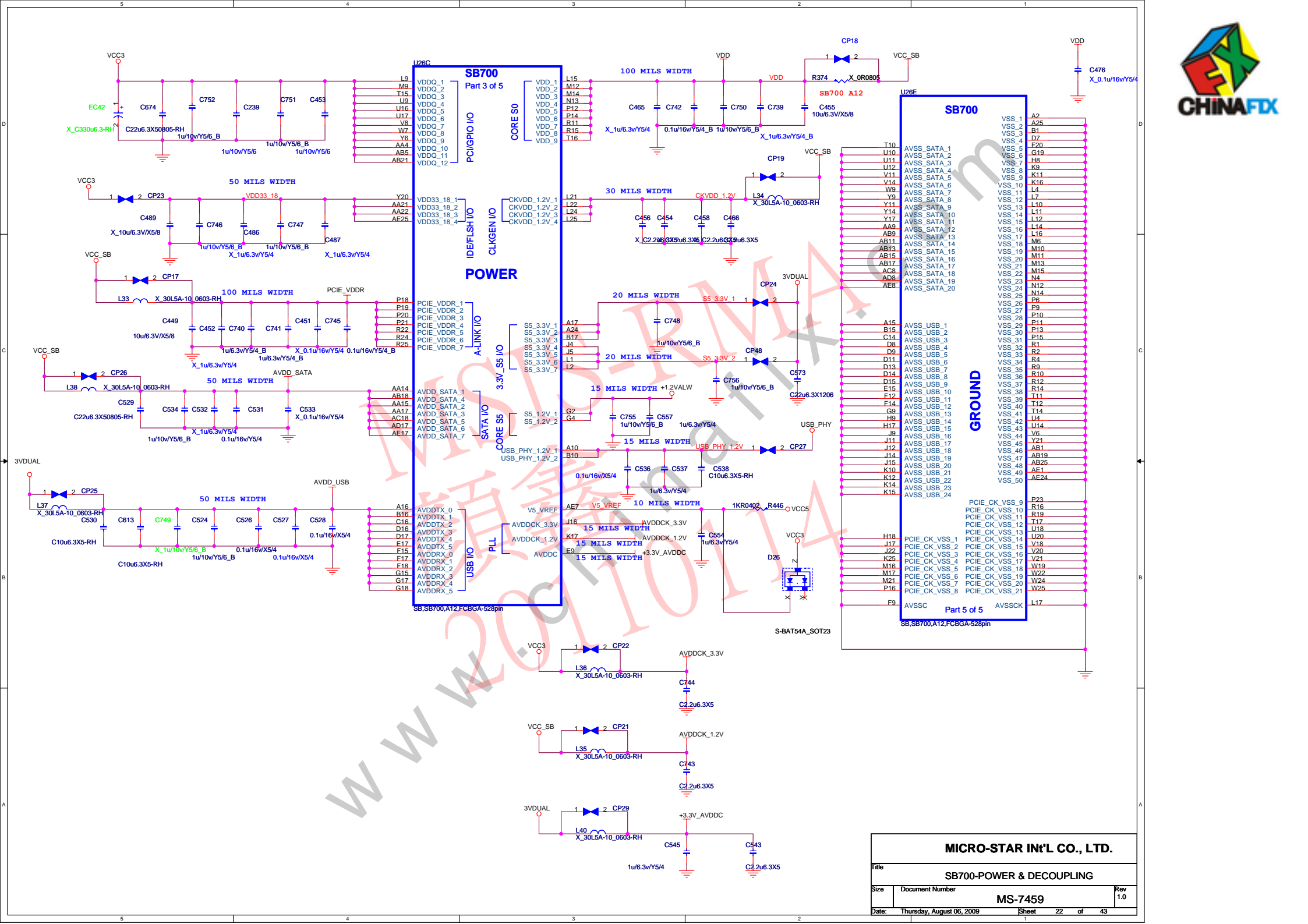
Impedance:USB
• 90- Ω \pm 15% differential
• Reference to a solid GND (not PWR) plane.



Added Cap 0.1uF stitching capacitors for crossing a split

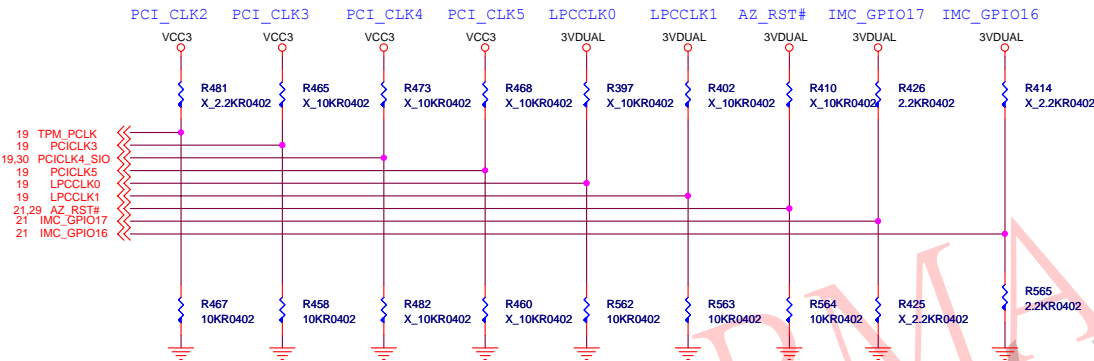
MICRO-STAR INT'L CO., LTD.

Title			
SB700-ACPI/GPIO/USB/AUDIO			
Size	Document Number		Rev
	MS-7459		1.0
Date:	Thursday, August 06, 2009	Sheet	21 of 43



REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS

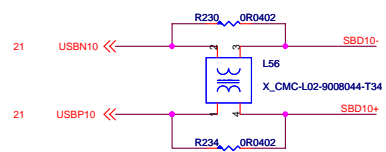
SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	





PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2

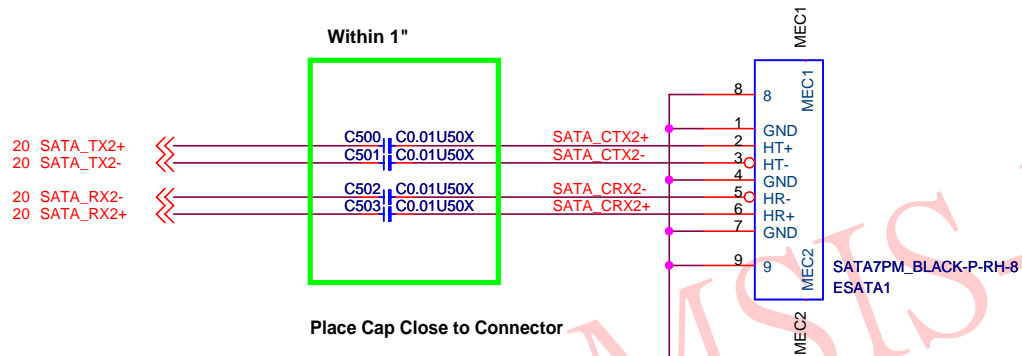


ok

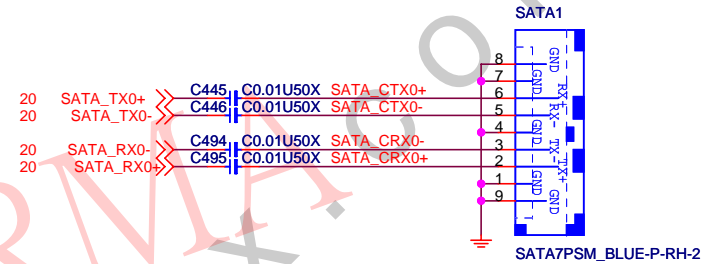
SERIAL ATA CONNECTOR BLOCK



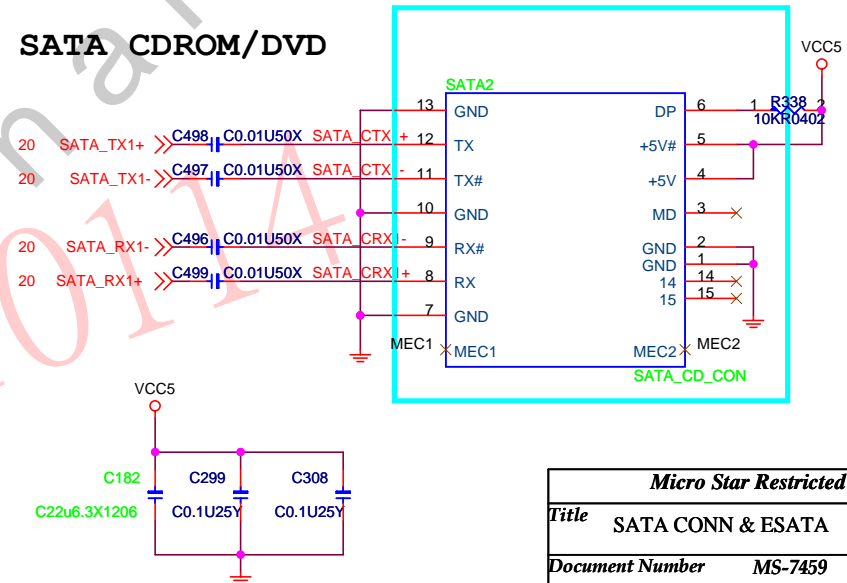
E-SATA



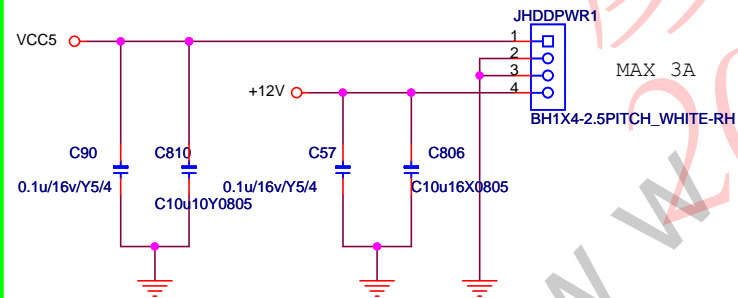
SATA HDD



SATA CDROM/DVD



HDD Power For 3.5"



Micro Star Restricted Secret

Title SATA CONN & ESATA

Rev
1.0

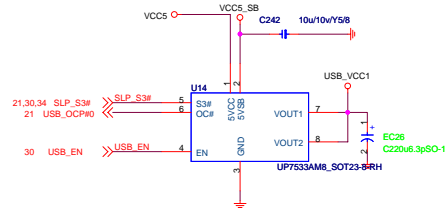
Document Number MS-7459

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No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw

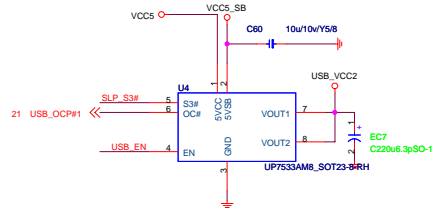
Last Revision Date:
Thursday, August 06, 2009

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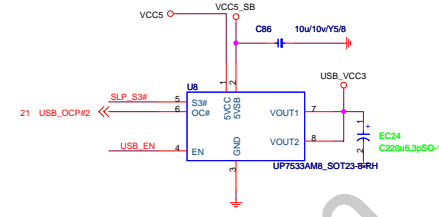
POWER CIRCUIT FOR USB PORT 0,1



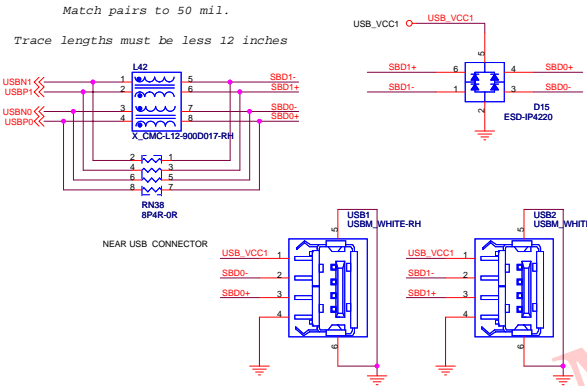
POWER CIRCUIT FOR USB PORT 2,3



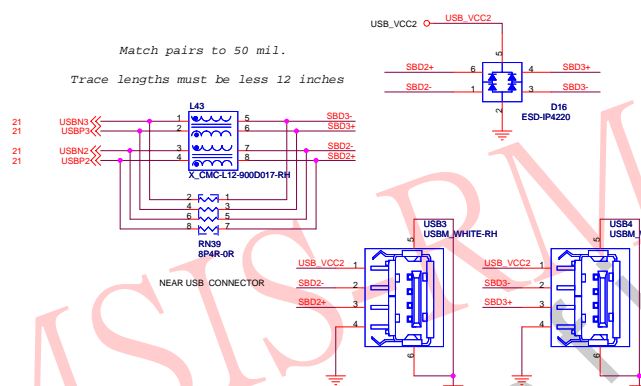
POWER CIRCUIT FOR USB PORT 4,5



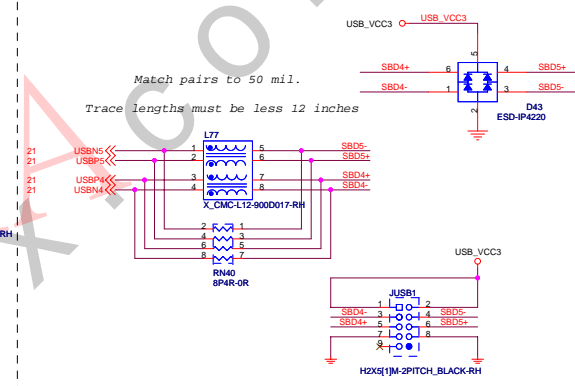
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



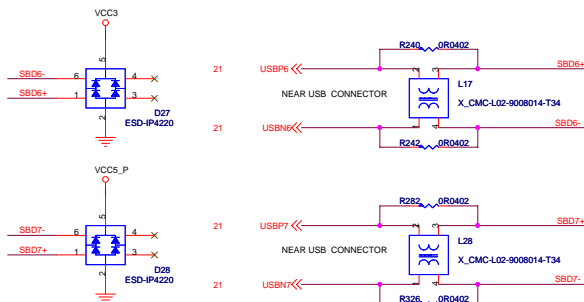
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



REAR PANEL USB CONNECTOR FOR USB PORT 4,5

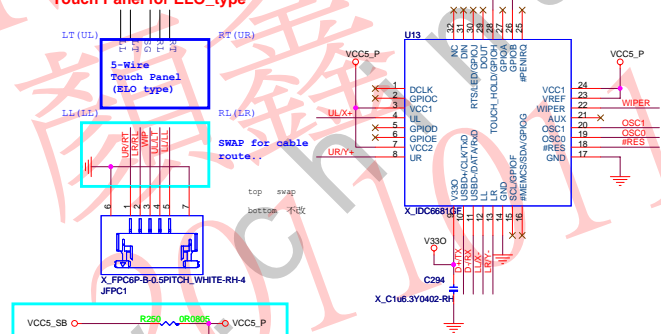


REAR PANEL USB CONNECTOR FOR USB PORT 6,7

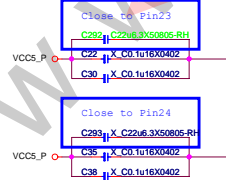


(Option 1) 5-Wire Resistive Touch Panel for ELO_type

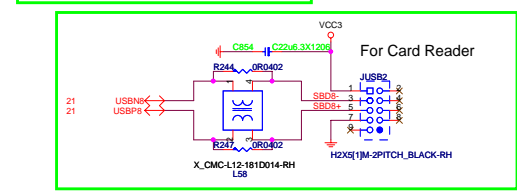
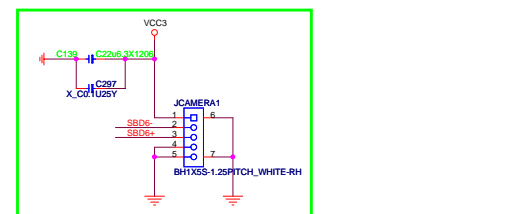
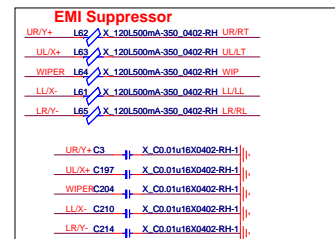
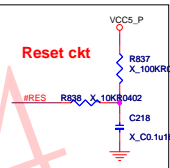
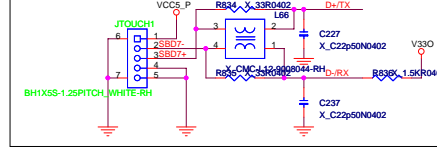
(Note1): Pull-low to disable the Touch_Hold feature.



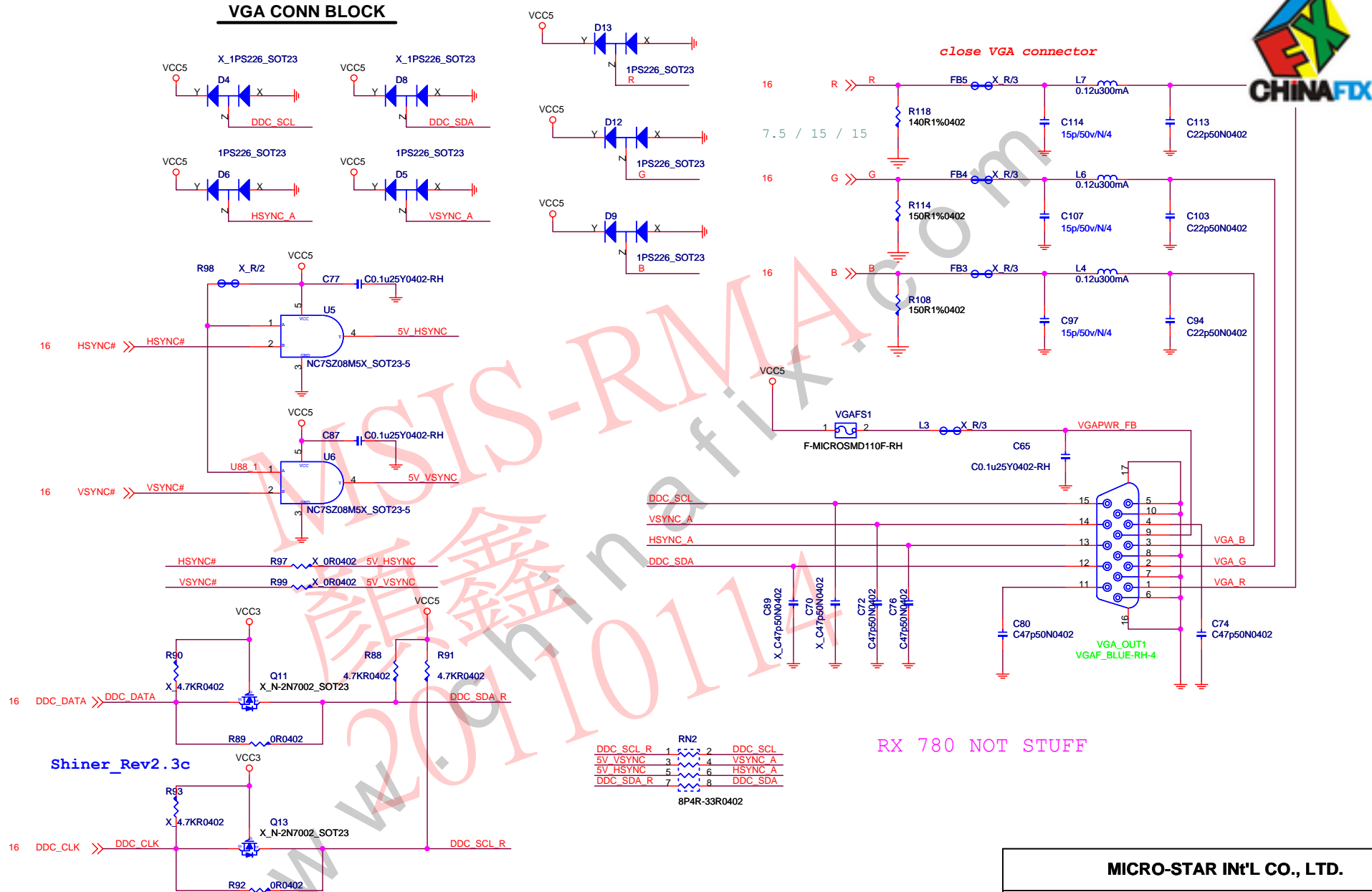
Decoupling Cap.



Low Speed USB D+/-



VGA CONN BLOCK



RX 780 NOT STUFF

MICRO-STAR INT'L CO., LTD.

Title

VGA-OUT CONN

Size

Document Number

MS-7459

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Date: Thursday, August 06, 2009

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ALC888

CO-LAY

option ==>ALC888S

ALC888

option ==>ALC889

ALC889 : Stuff

ALC888S : No Stuff

靠近codec

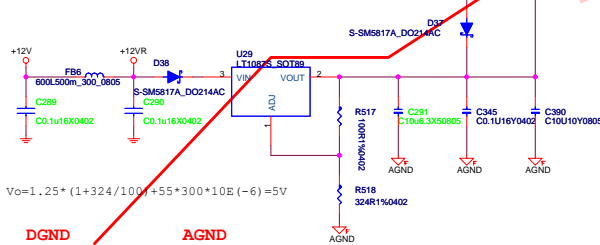
靠近codec

ok

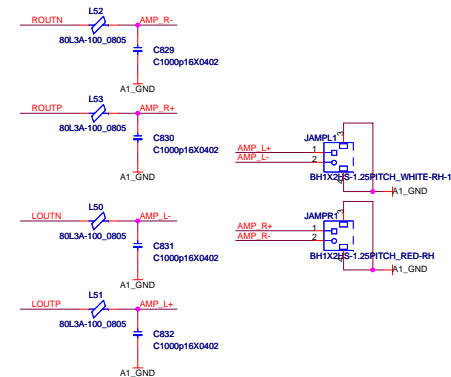
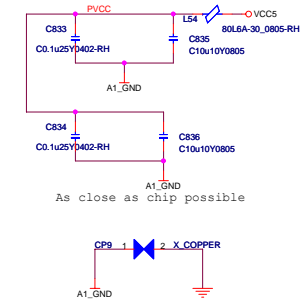
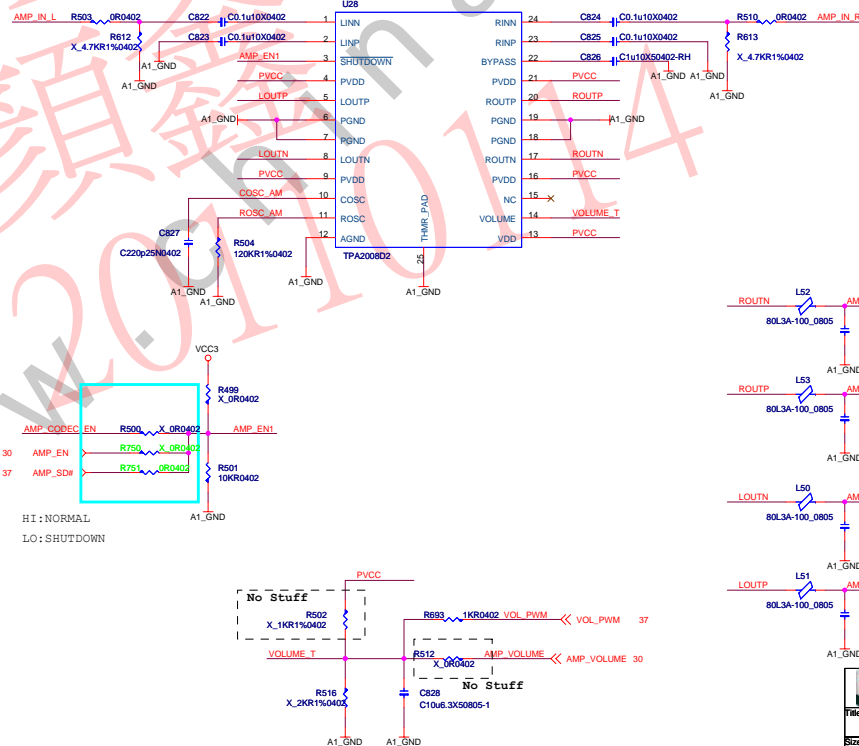
ALC889 : C11-1067424-Y01

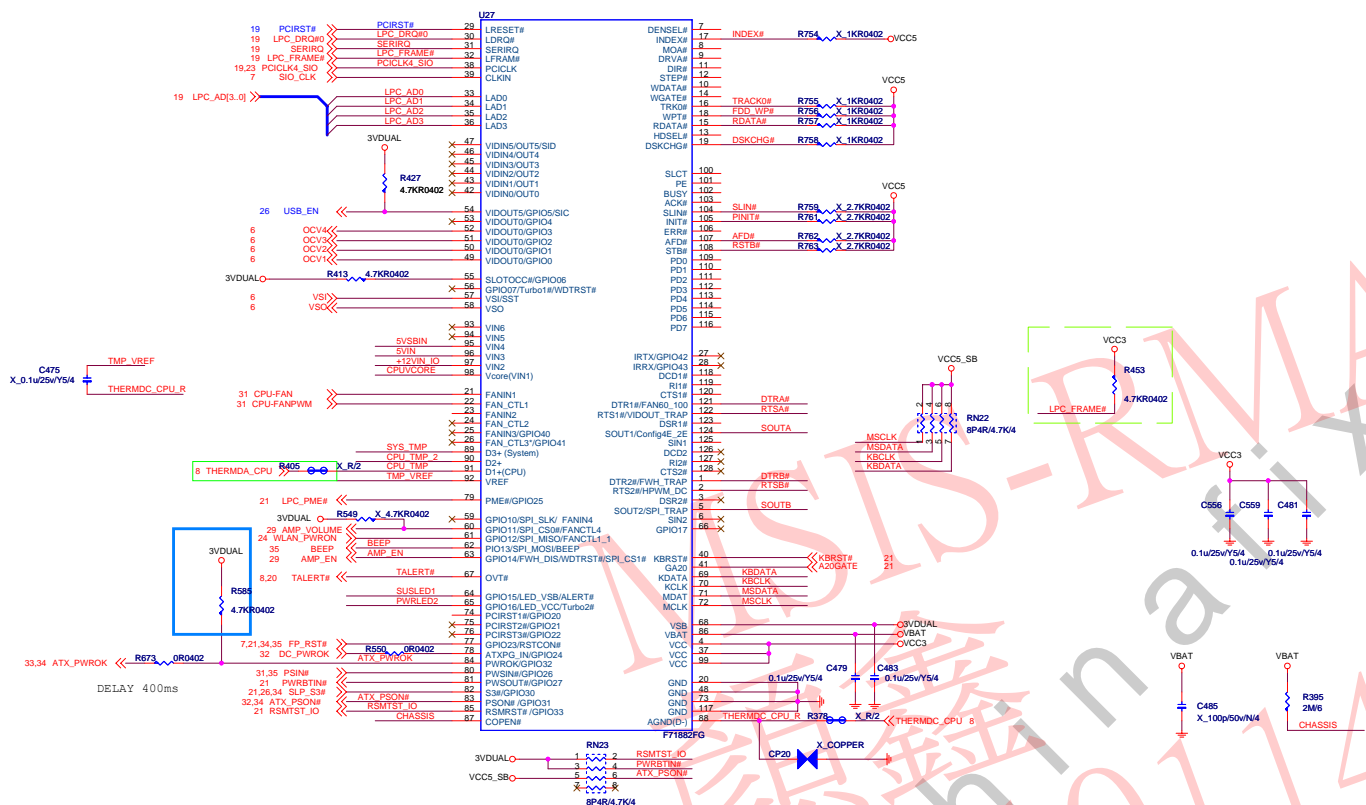
ALC888S : C11-4757013-W08

REAR IO

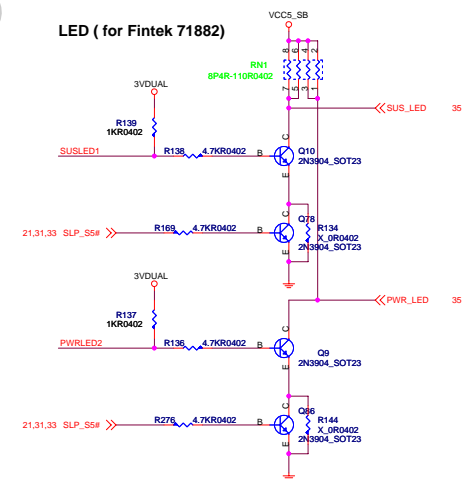
AUDIO CODE
REGULATORS

避開power走線以及noise干擾

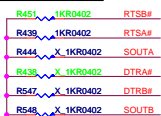
For
EMI



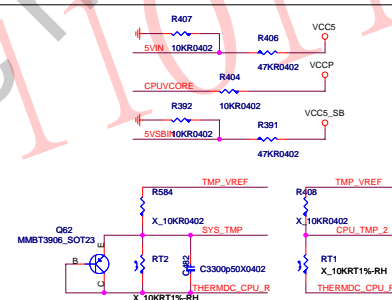
LED (for Fintek 71882)



LPC I/O STRAPPING RESISTOR

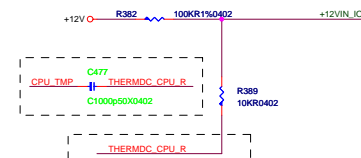


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49=54=VID_OUT PIN42=47=VIDIN	PIN49=54=GPIO PIN42=47=VIDIN/OUT
SCOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTRB#	SPI as a backup BIOS	SPI as a primary BIOS
SOUTB	SPI function disabled	SPI function enable



**NOTE: LOCATE CLOSE
STATUS PANEL**

Thermal Resistor



MICRO-STAR INT'L CO., LTD.

<OrgAddr1>

LPC-F71882

Size	Document Number
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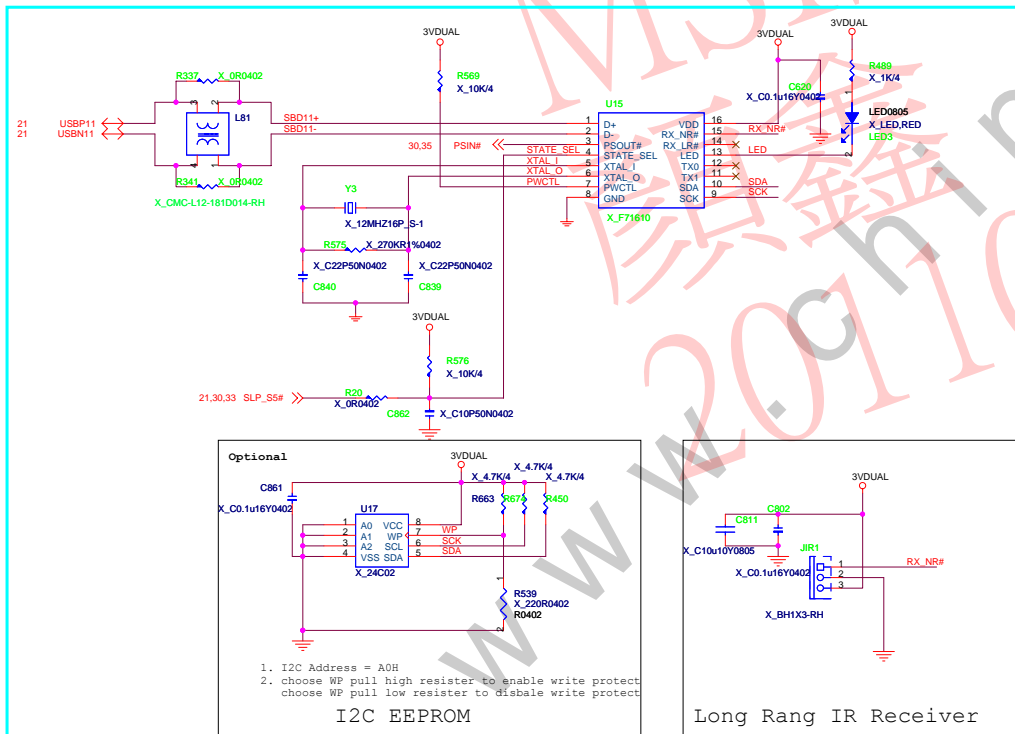
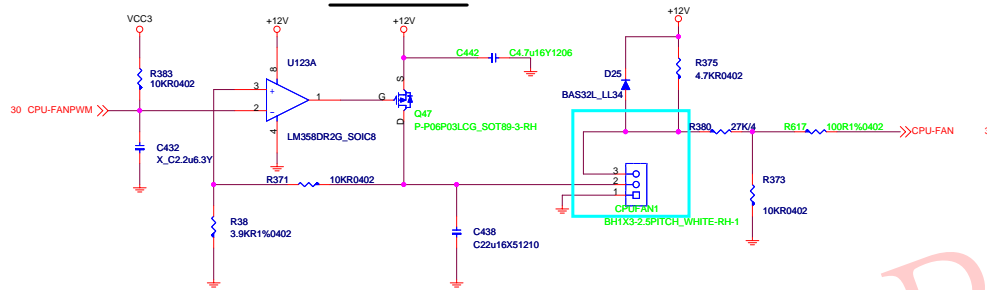
Date: Thursday, August 06, 2009 Sheet 30 of 43

FAN CONTROL

DC MODE

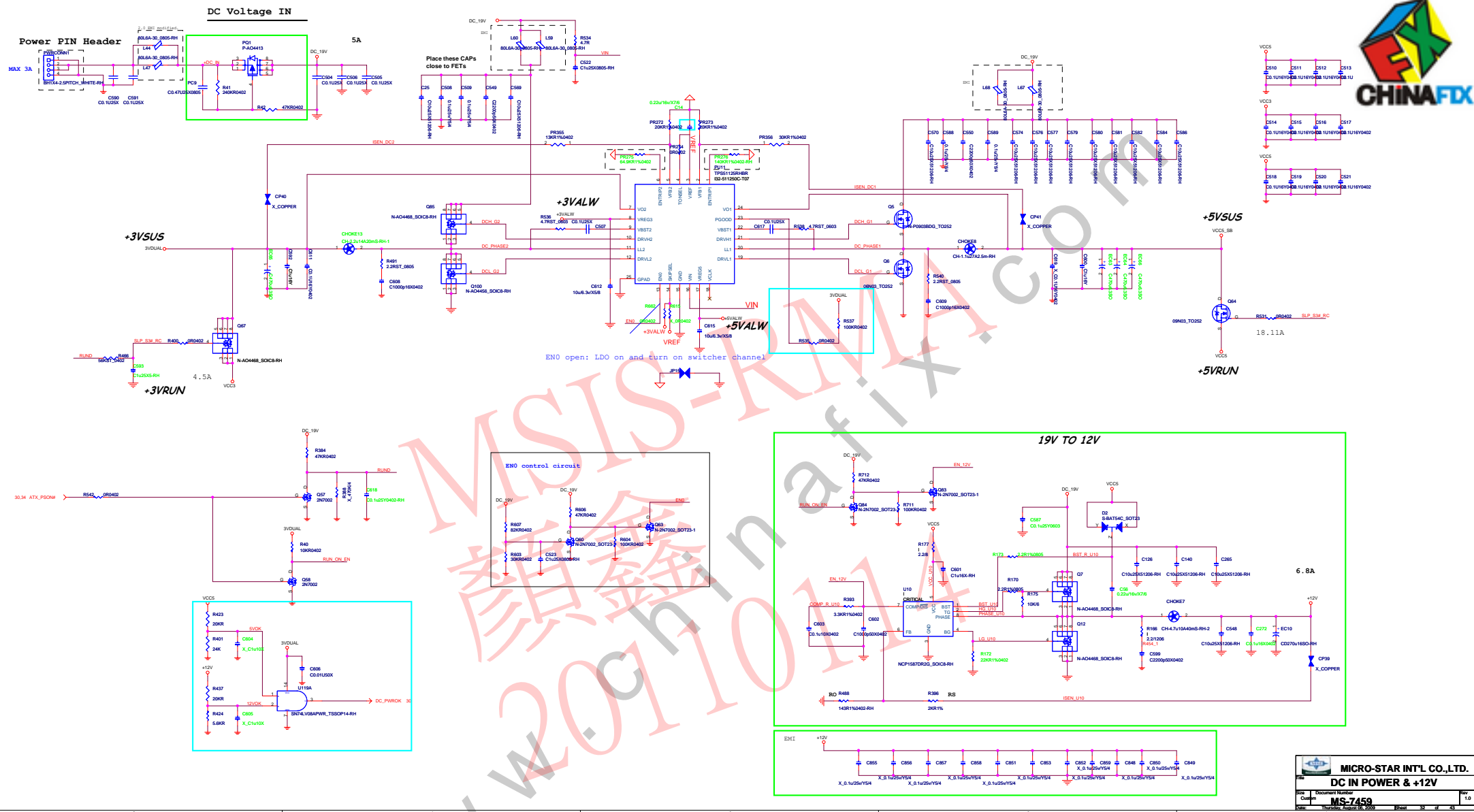
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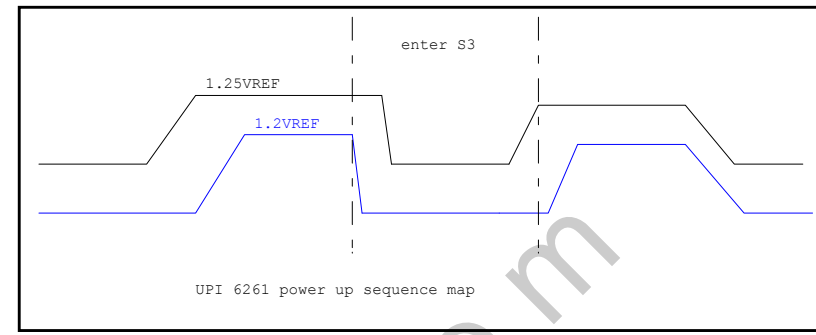
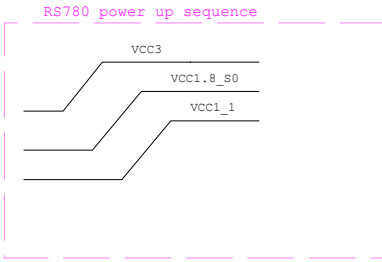
CPU FAN



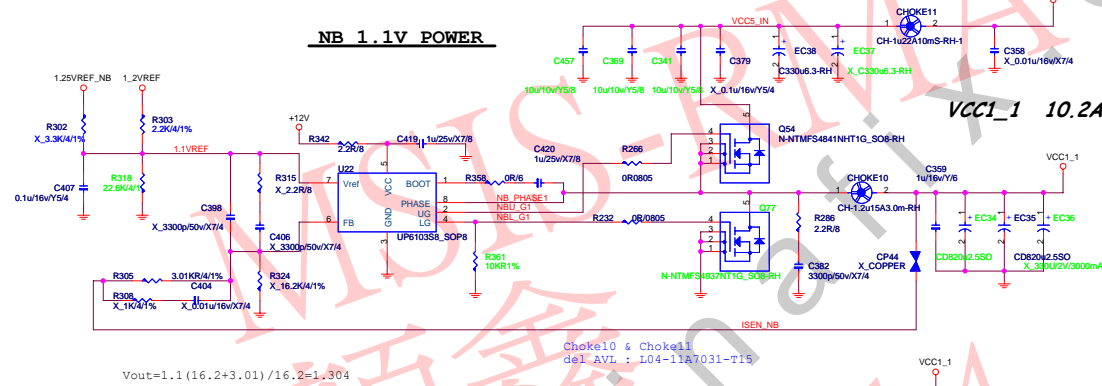
Micro Star Restricted Secret

Title	FAN & IR	Rev	1.0
Document Number	MS-7459		
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, August 06, 2009	
Sheet	31	of	43

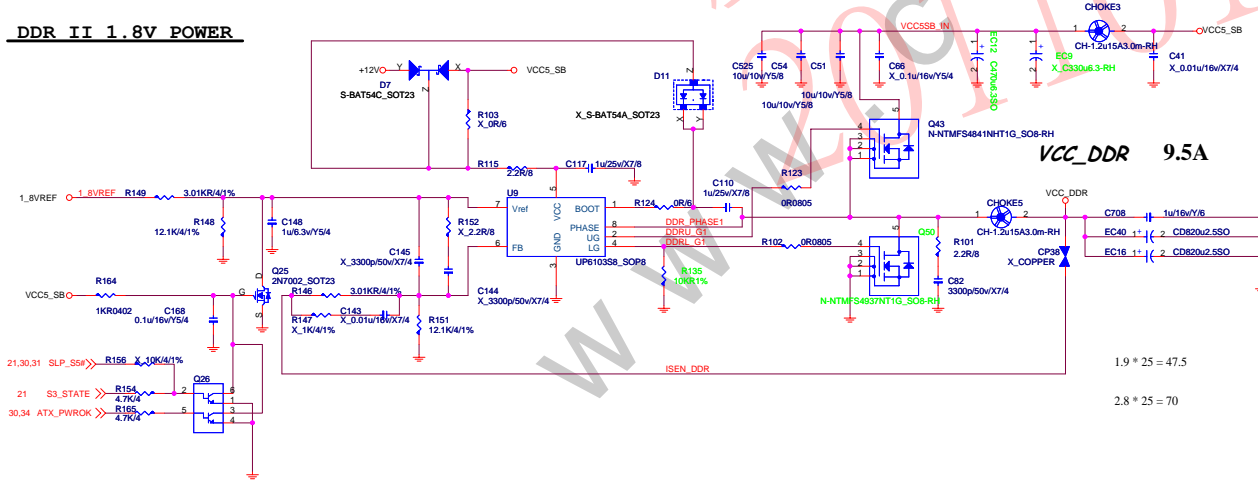




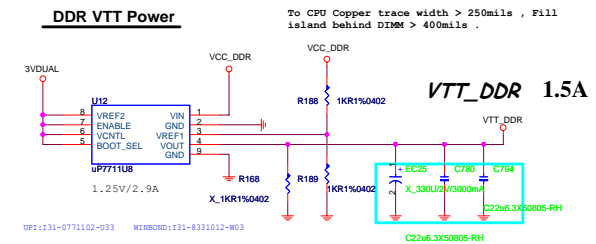
NB 1.1V POWER

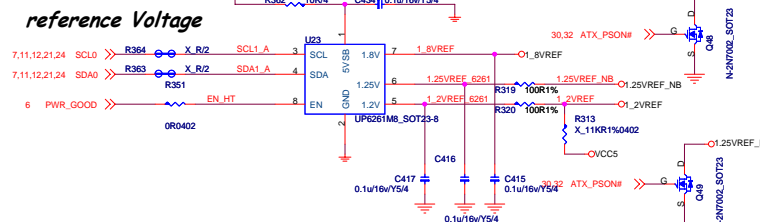
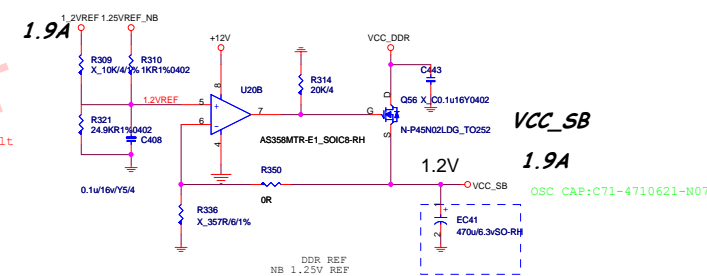
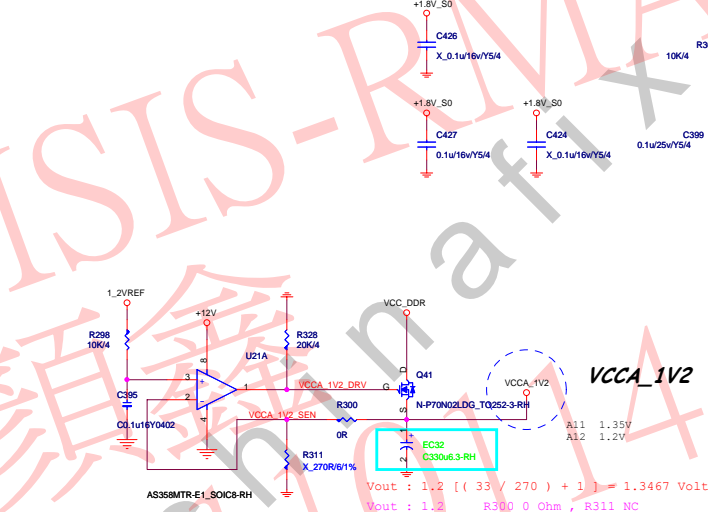
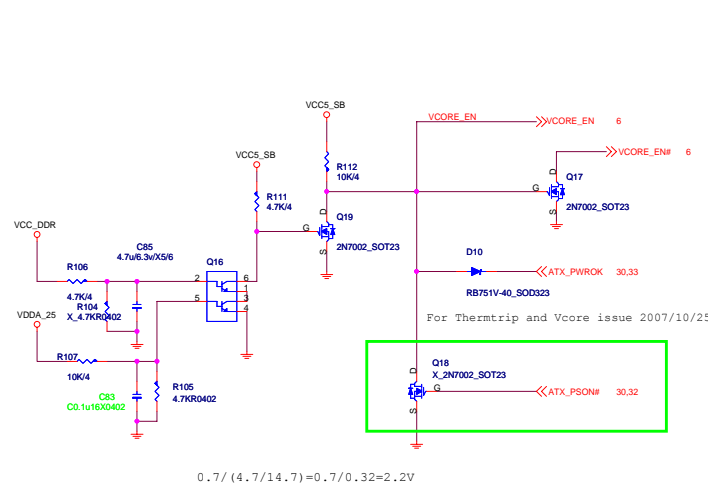


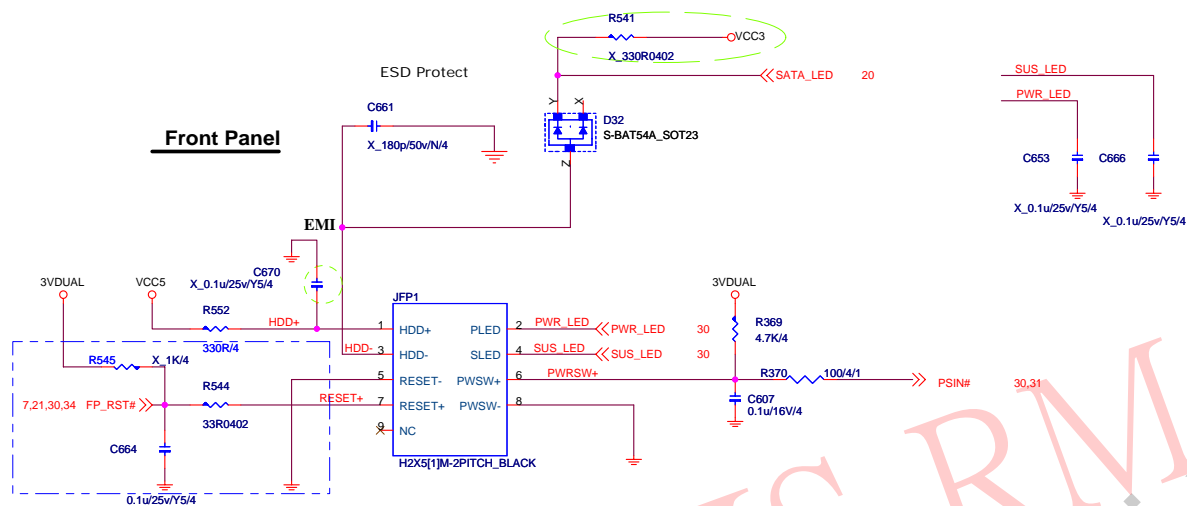
DDR II 1.8V POWER



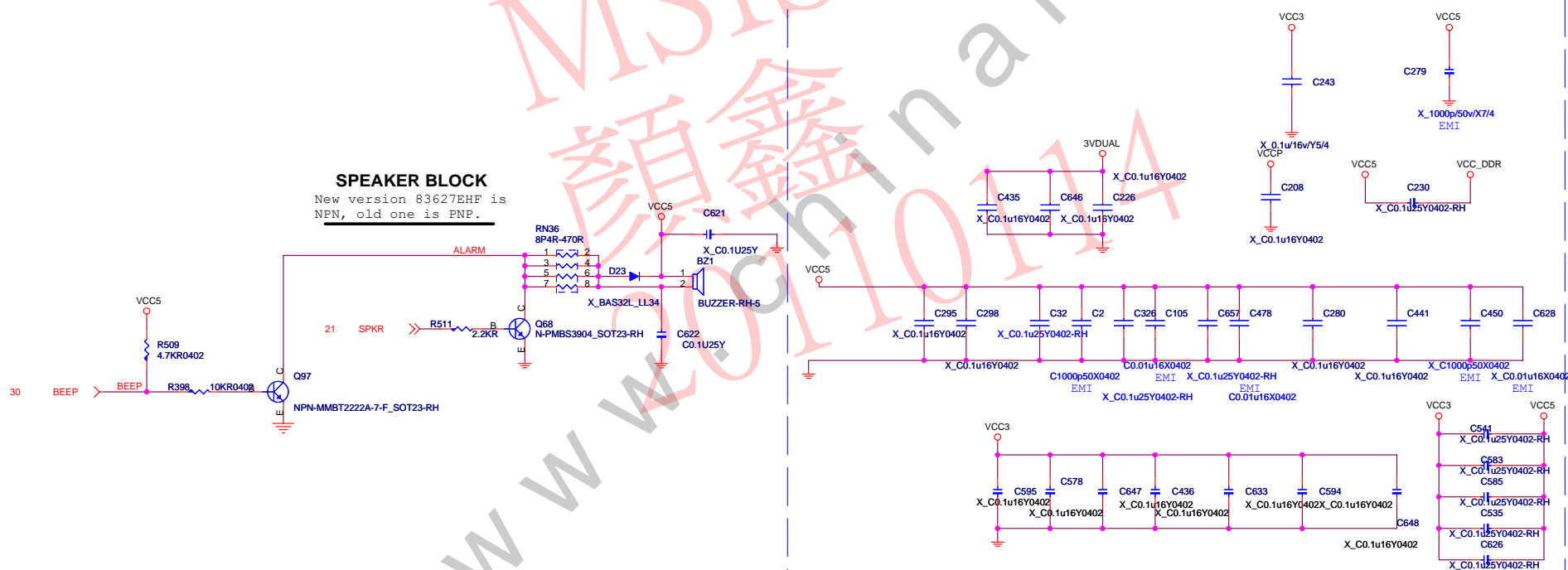
DDR VTT Power





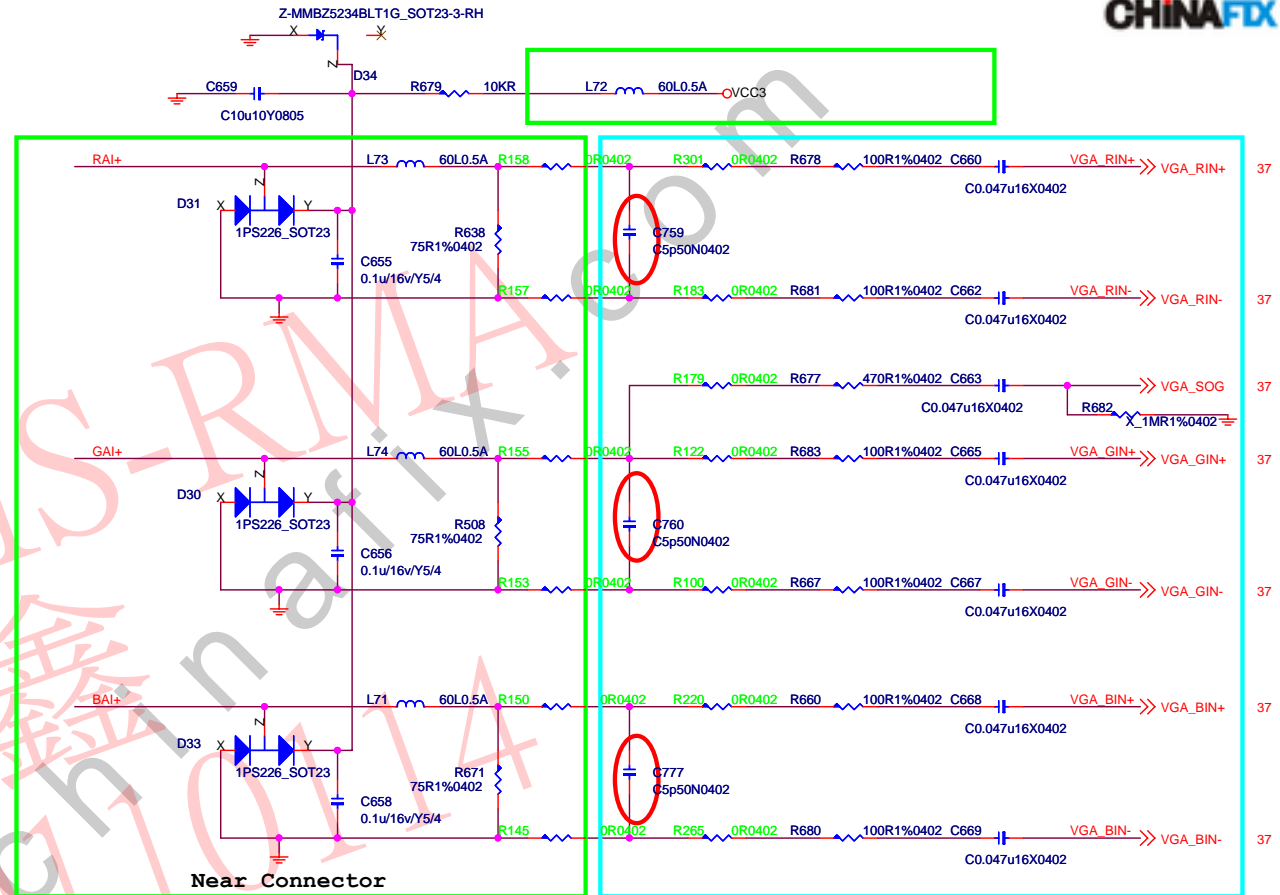
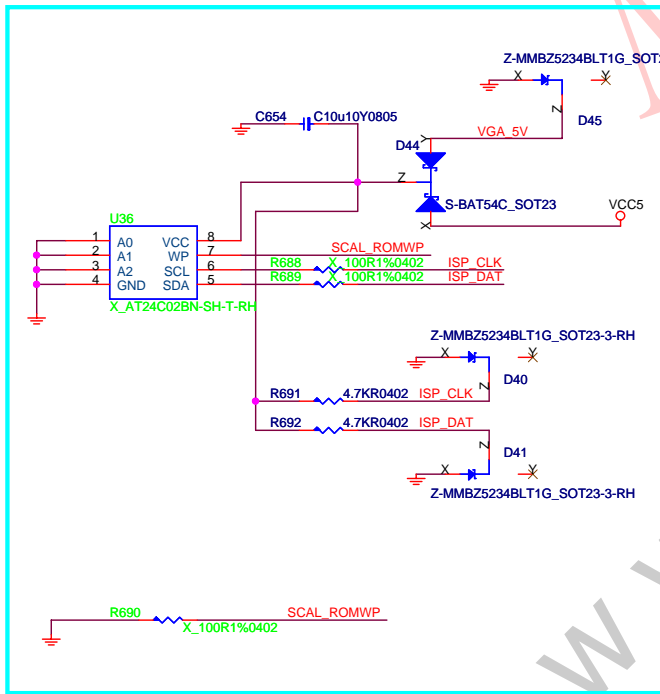
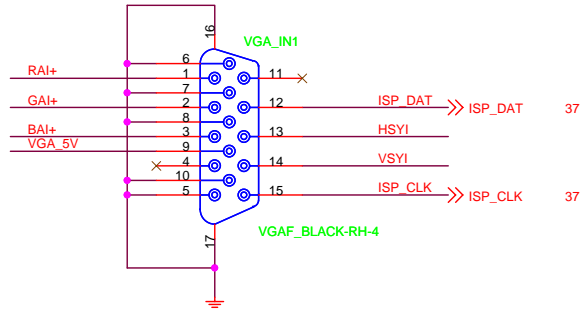


EMI solution

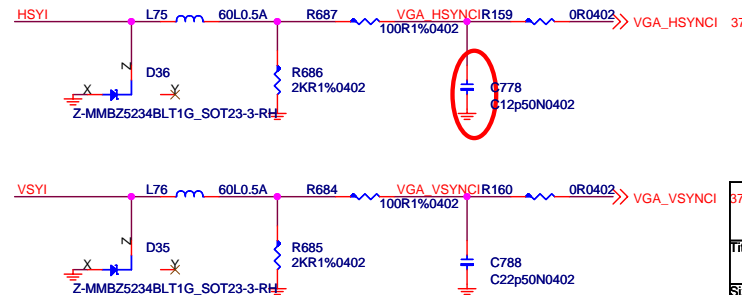


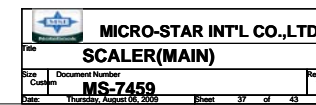
Micro Star Restricted Secret		
Title	Rev	
Front Panel/EMI		1.0
Document Number	MS-7459	
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, August 06, 2009 Sheet 35 of 43

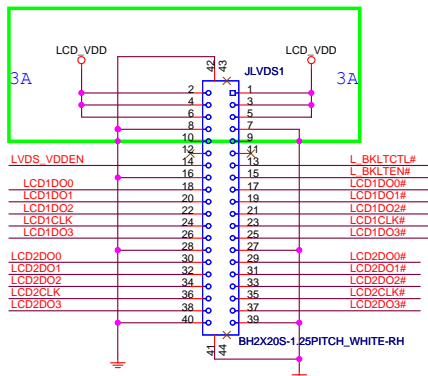
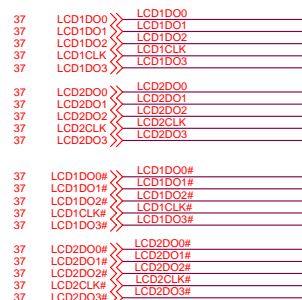
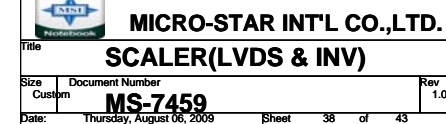
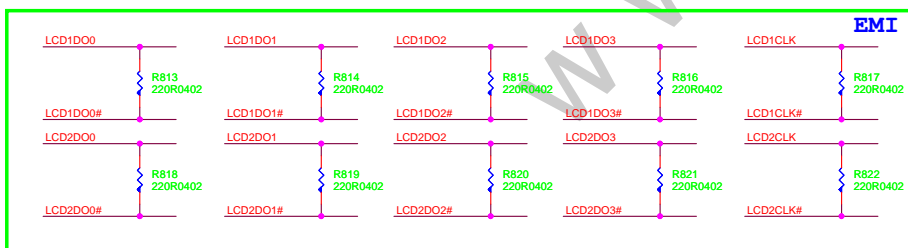
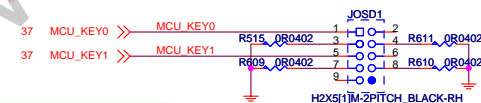
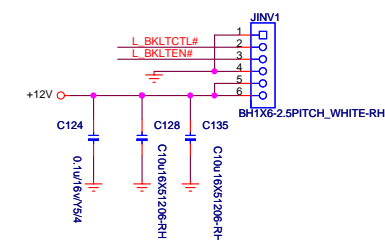
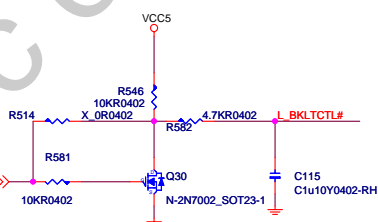
D-SUB INPUT

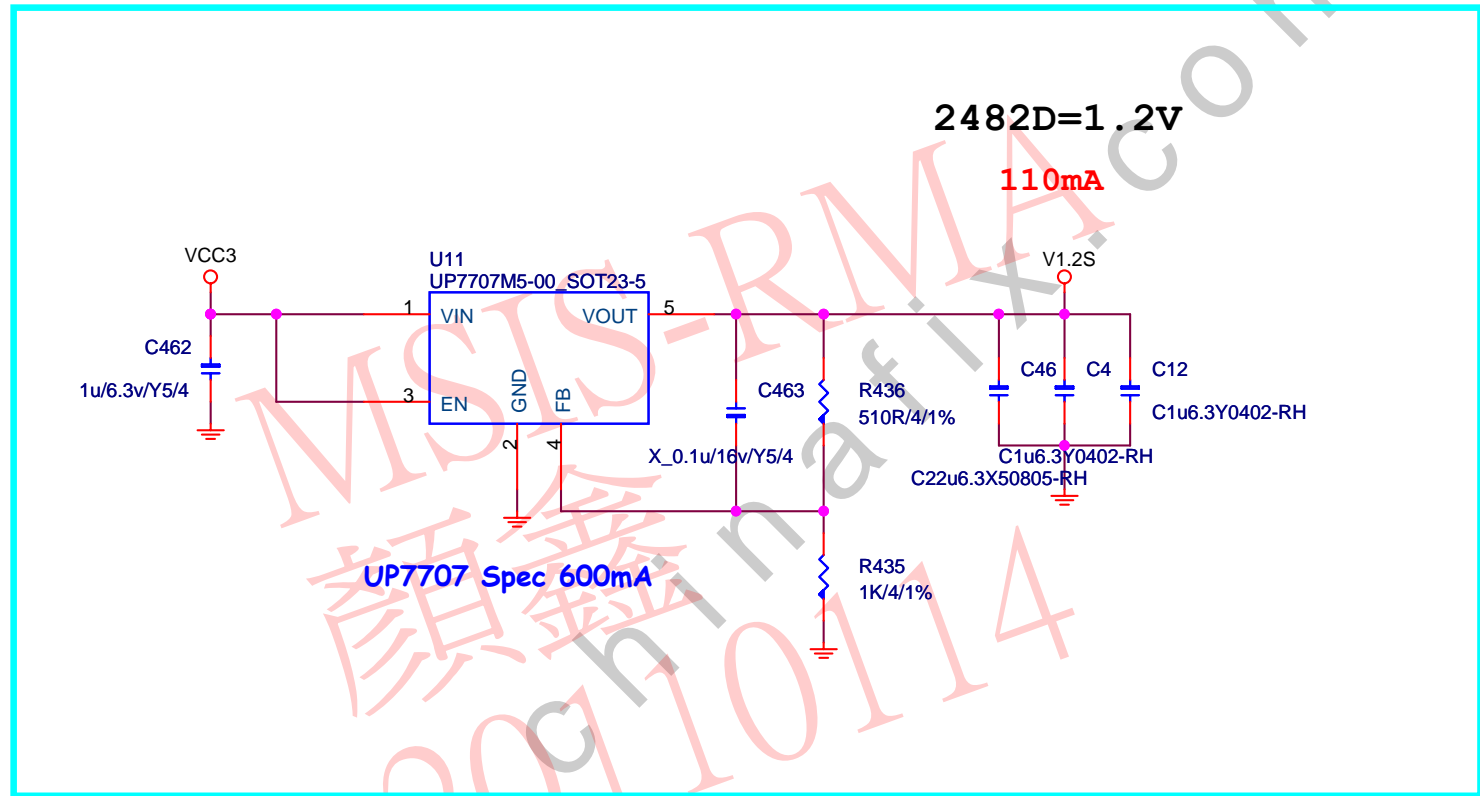


Near 2382 SCALAR

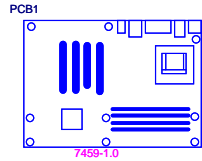




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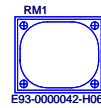


PCB

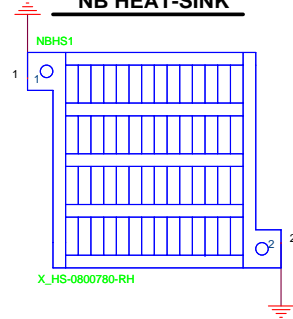


PCB : 1080

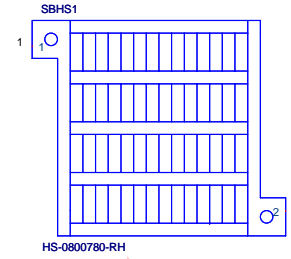
CPU RM



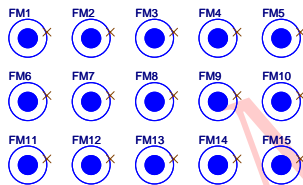
NB HEAT-SINK



SB HEAT-SINK

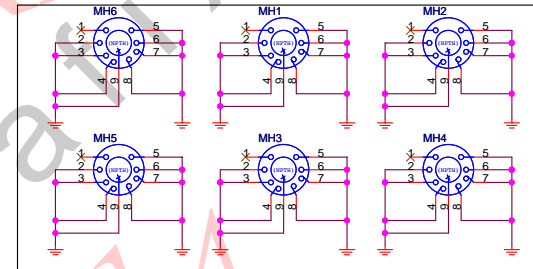


Optics Orientation Holes

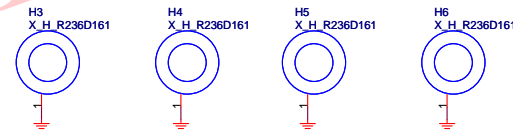
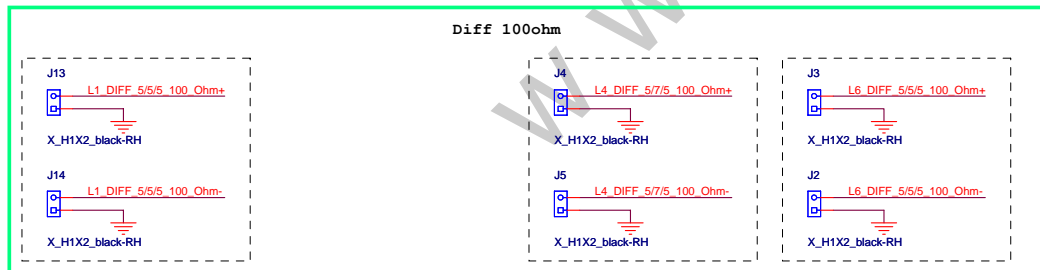
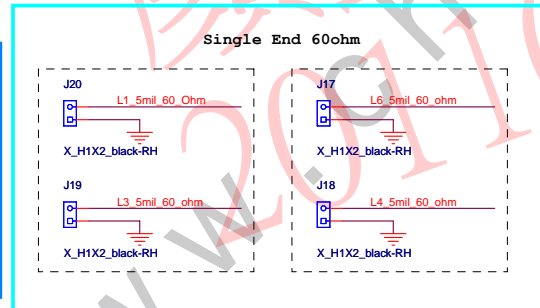
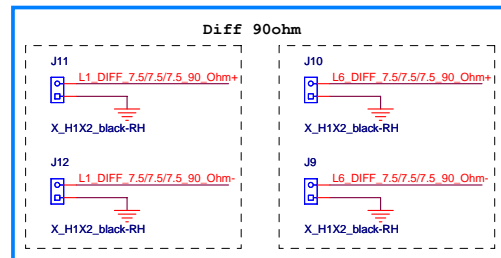


LABEL1
RESISTER
LABEL1

Main Board Holes



Simulation

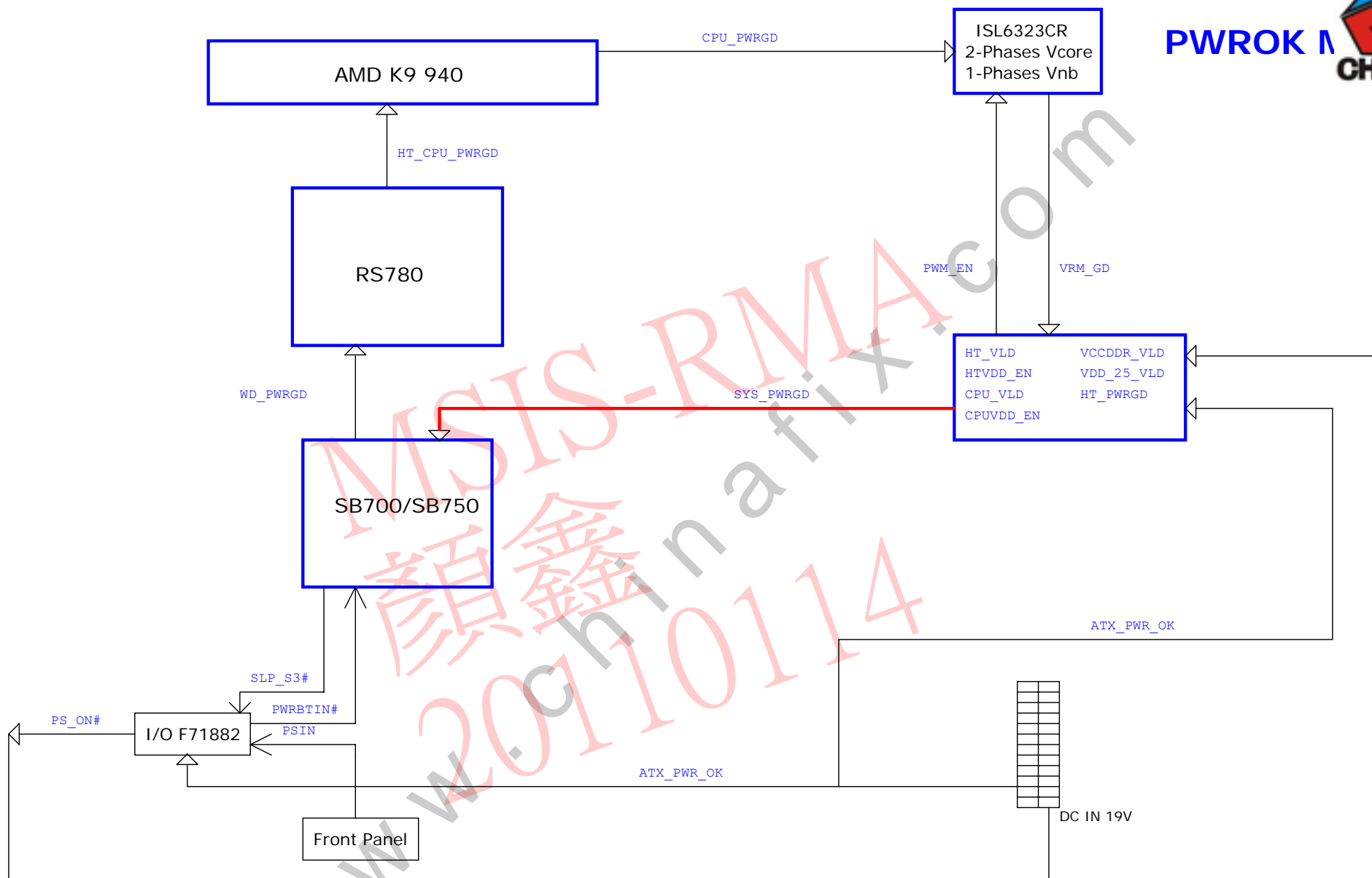


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PWROK M



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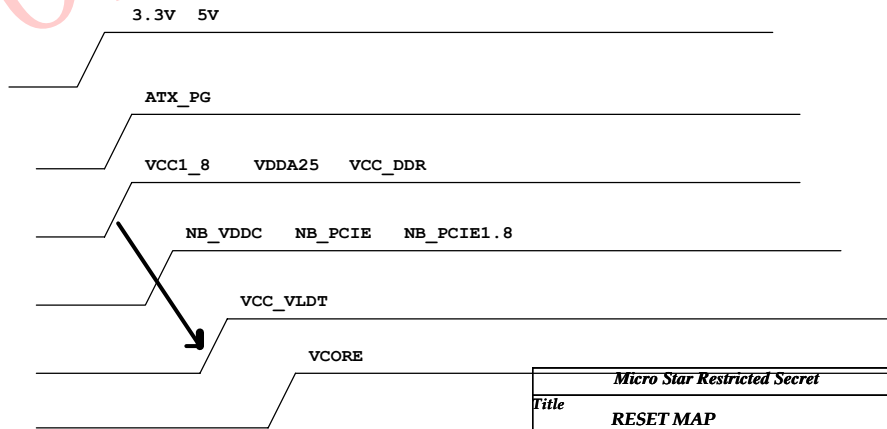
- 1.Lan LED reverse.
- 2.change U32 to M31-25L1002-M24
- 3.fan connector 1 and 3 pin reverse and add R617 預防逆電流.
- 4.Remove C6 解不上CPU電壓會不正常切換.
- 5.sata2 connector 換料.
- 6.remove R250 staff R264解touch ic s3 resume no power issue.
- 7.將U14&U4&U8 pin5改接SLP_S3#.
- 8.remove DC-POWER OK CIRCUIT.
- 9.change EC46,EC32,EC47,EC52,EC25,C142,C182,Q47,Q47,Y6 COST DOWN.
- 10.modify ISP_CLK & ISP_DATA.
- 11.change CN1 & HDMI -IN signal & SCALAR IC 2382



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