

First International Computer, Inc

Portable Computer Group HW Department

Board name : Mother Board Schematic

Project : LM10W

Version : 0.7

Initial Date : Feb 21 , 2006

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3. Block Diagram :
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9. switch setting

Manager Sign by:

Drawing by :

Total confirm by: Jack Chen

LAN Circuit check by:

Audio Circuit check by:

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Title LM10W < VIA VN896 + VT8237A >			
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1. Schematic Page Description :

LM10W Schematic Ver : 0.7

- | | | |
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| 20. VT1634AL LVDS Transmitter | 42. G1432+1410 Audio Amplifier | |
| 21. LCD Connector | 43. H.P. Out / Audio CNN | |
| 22. CRT Connector | 44. DDR PWR | |

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)

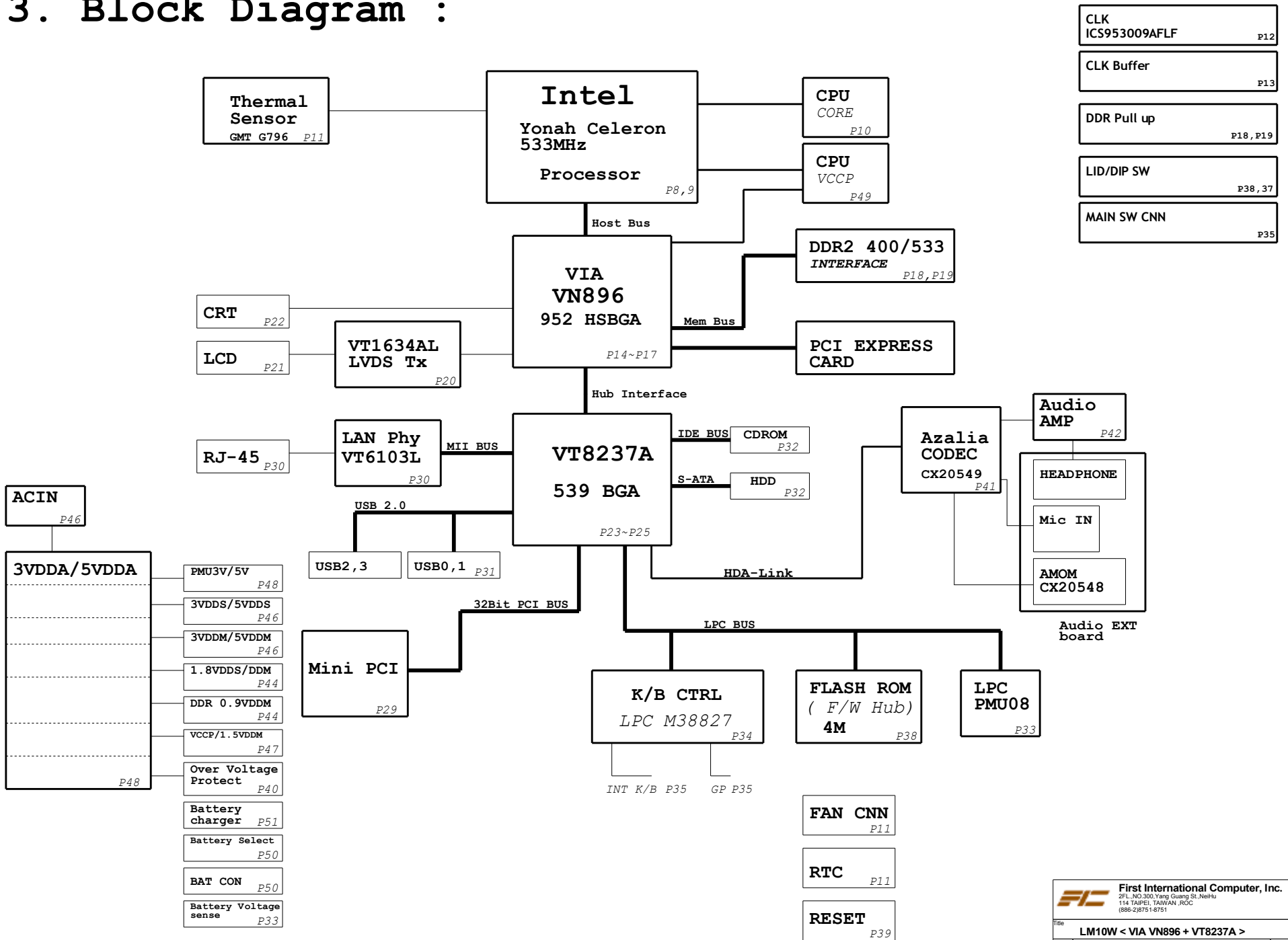
PCIINT	CHIP
IRQA	NB
IRQB	MiniPCI
IRQC	MiniPCI
IRQD	IRQH PCI-E

BUSMASTER	CHIP
REQ	
REQ0 / GNT0	
REQ1 / GNT1	
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Description
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Cascade)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	FLOPPY DISK
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

3. Block Diagram :



4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU

VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR 0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	= Capacitor
CN	= Connector
D	= Diode
F	= Fuse
L	= Inductor
Q	= Transistor
R	= Resistor
RP	= Resistor Pack
U	= Arbitrary Logic Device
Y	= Crystal and Osc

Net Name Suffix

0	= Active Low signal
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Signal Conditioning

D	= Damped (by a resistor)
Q	= Isolated (by a Q-switch)
L	= Filtered (by an inductor or bead)

5.Board Stack up Description

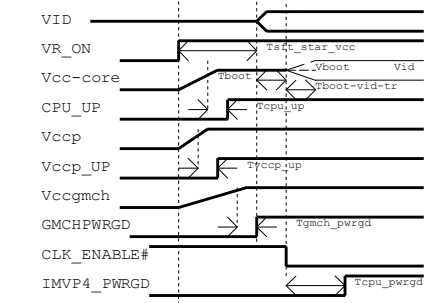
PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer (AGTL, CLOCK, DDR)
Layer 4		Stripline Layer (Analog, LVDS, other)
Layer 5		Power Plane
Layer 6		Solder Side, Microstrip signal Layer

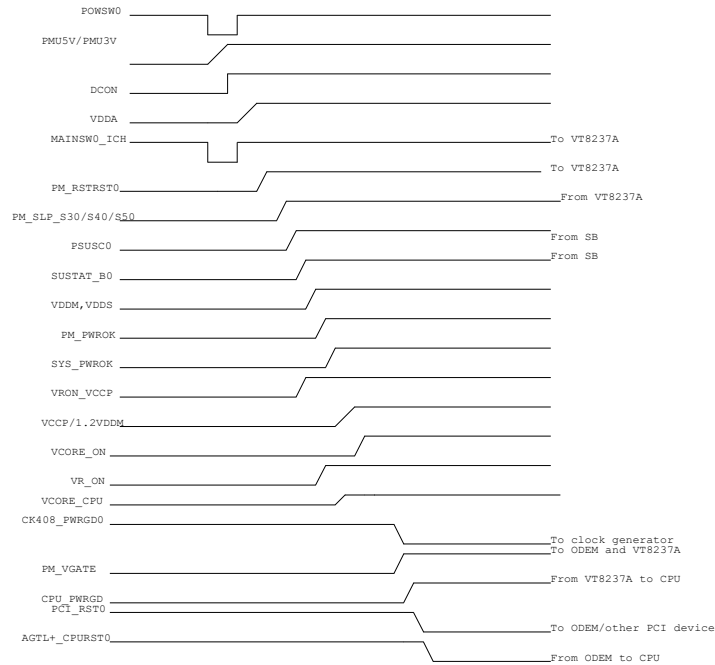
6.Schematic modify Item and History :

7. power on & off & S3 Sequence :

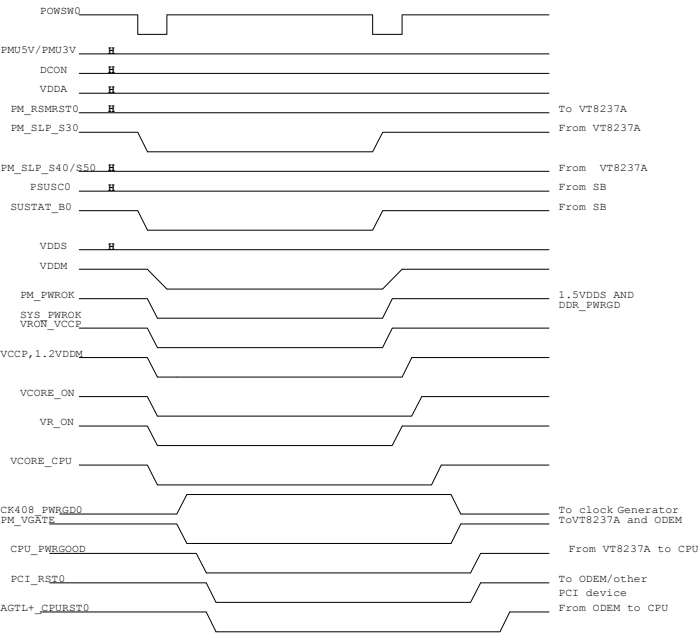
Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

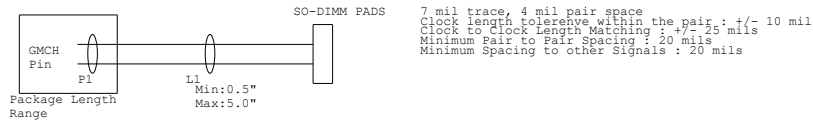
DDR Signal Groups

Group	Signal Name
Clocks	SCK[5:0] SCK# [5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS# [3:0]
Command	SMA[12:6,3:0] SBA[1:0] SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

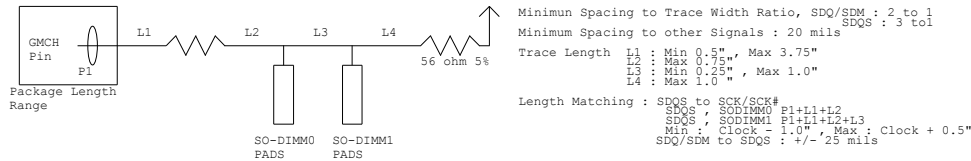
Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

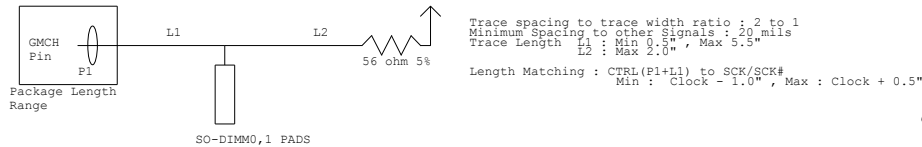
Clock Signals Topologies and Routing Guidelines



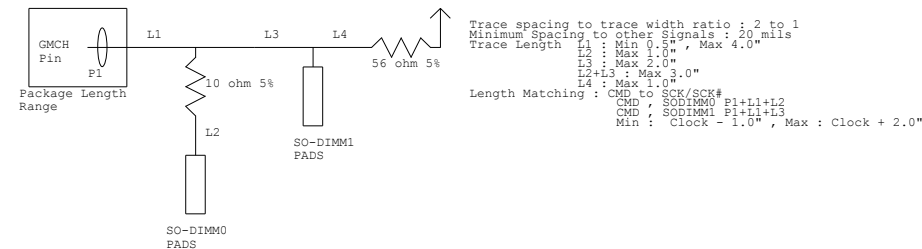
Data Signals Topologies and Routing Guidelines



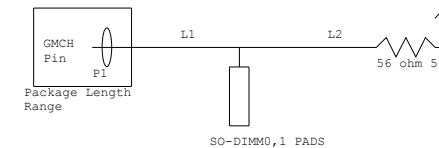
Control Signals Topologies and Routing Guidelines



Command Signals Topologies and Routing Guidelines



CPC Signals Topologies and Routing Guidelines

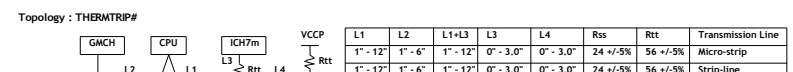
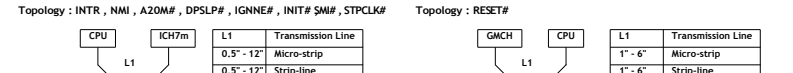
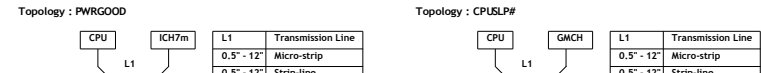
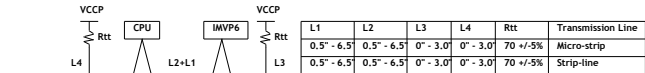
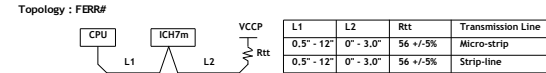
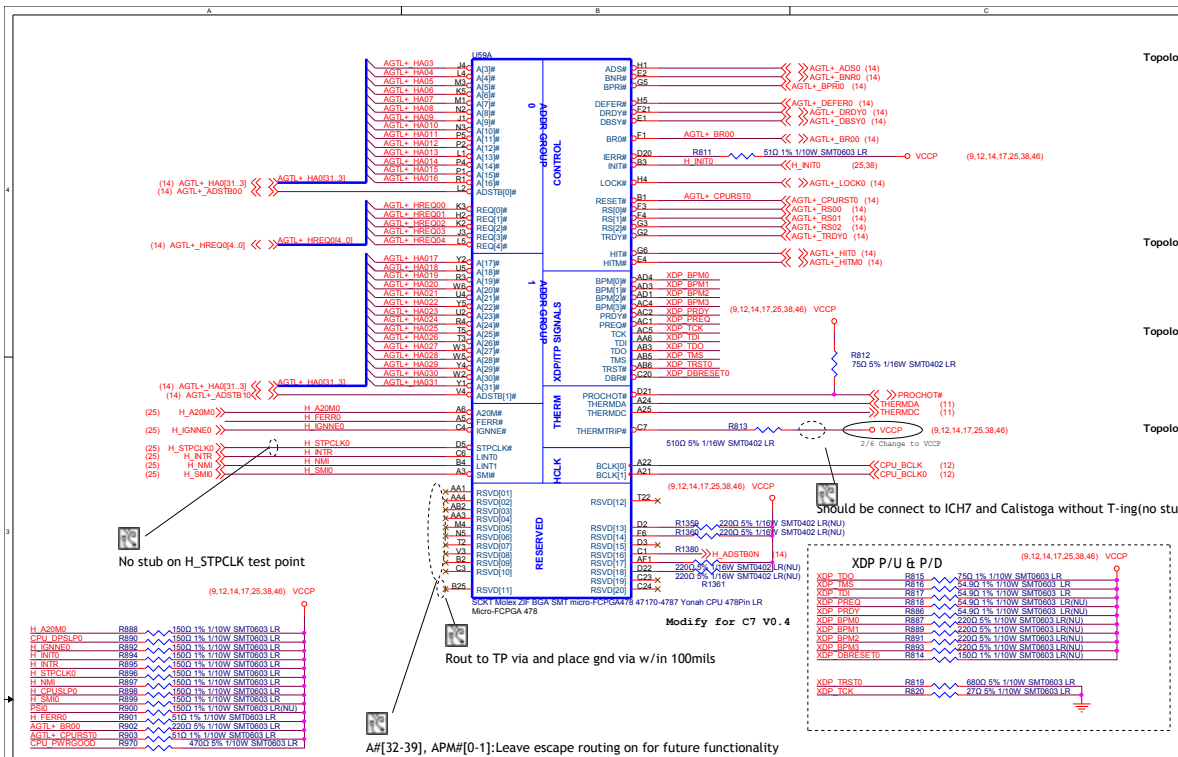


CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" ~ 8"	5 / 20 mils (5 mil space between + & -)	1. Differentials pairs with the same length (within 10 mil) 2. CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH AGPCLK_ATI	4.5" ~ 9.0" MAX : 8.5"	5 / 20 mils	* 66MCLK ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5" ~ 9.0"	5 / 20 mils	1. Making PCI length with minimum various 2. Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5" ~ 9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" ~ 12.5"	5 / 20 mils	

SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5", Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0", Max : Clock + 0.5"



FSB Common Clock Signal Layout Guide :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 - 6.5 inch	55+/-15%	4 & 8 mils	
Micro-strip(Ext. Layer)	1.0 - 6.5 inch	55+/-15%	4 & 8 mils	

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0], DINV0#	+/- 100 mls	DSTBP0#,DSTBN0#	+/- 25 mls
DATA#[31..16], DINV1#	+/- 100 mls	DSTBP1#,DSTBN1#	+/- 25 mls
DATA#[47..32], DINV2#	+/- 100 mls	DSTBP2#,DSTBN2#	+/- 25 mls
DATA#[63..48], DINV3#	+/- 100 mls	DSTBP3#,DSTBN3#	+/- 25 mls

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
DINV#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 8 mils
DATA#[63..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 8 mils
DSTBN#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 - 5.5 inch	55+/-15%	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
ADDR#[16..3], REQ#[4..0]	+/- 200 mls	ADSTB0#	+/- 200 mls
ADDR#[31..17]	+/- 200 mls	ADSTB1#	+/- 200 mls

*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 - 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 - 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 - 6.5 inch	55+/-15%	4 & 8 mils

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

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Place these inside socket cavity on L8
(North side secondary)

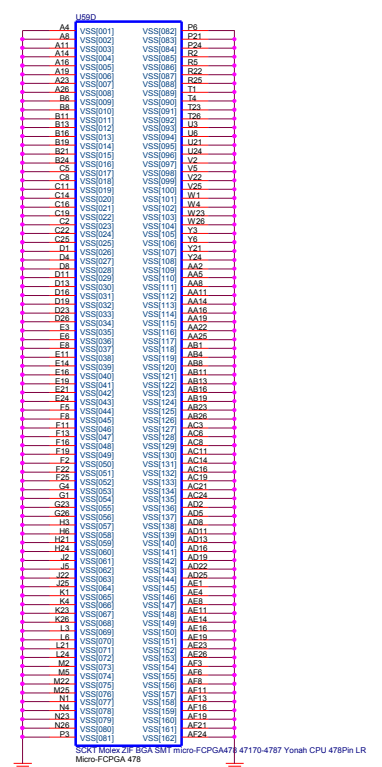
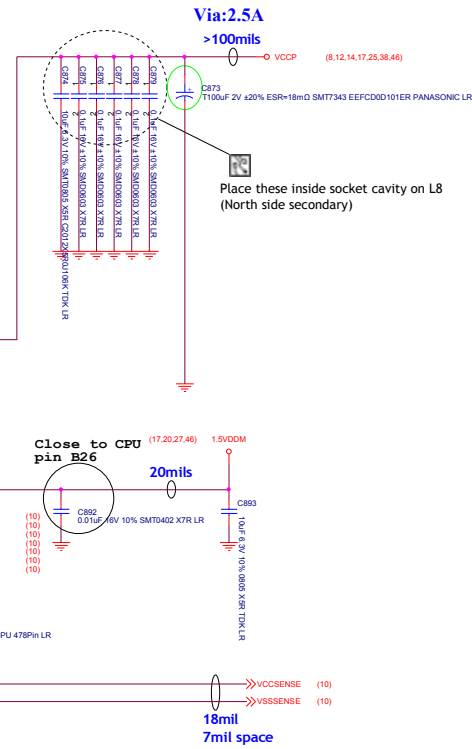
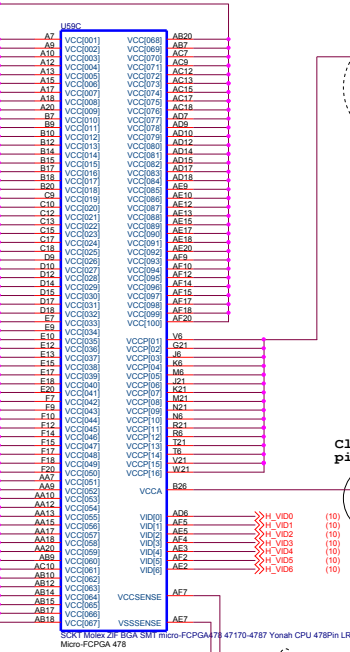
Place these inside socket cavity on
L8 (South side secondary)

Place these inside socket cavity on L1
(North side Primary)

Place these inside socket cavity on L1
(South side Primary)

North side secondary

South side secondary



Clock Latout Guideline

CLOCKS	LENGTH	TRACE / SPACE	NOTES
HOST Clock			
CPU_BCLK[1..0] MCH_BCLK[1..0] ITP_BCLK[1..0]	2" - 8"	5 / 20 mils (5 mil space between 1 & 0)	1. Differentials pairs with the same length (within 10 mil) 2. CPU & NB trace mismatch within 20 mil
CLK66 Clock			
CLK_ICH66 CLK_MCH66 CLK_AGP	4.5" - 9.0"	5 / 20 mils MAX : 8.5"	Length mismatch within 100 mils
CLK33 Clock			
CLK_ICHPCI CLK_SIOPCI CLK_FWHPCI	4.5" - 9.0"	5 / 20 mils	Length same as CLK66 Clock Length mismatch within 100mils
PCI Clock			
CLK_MINIPCI CLK_1394PCI CLK_PMU08PCI CLK_CBPCI	4.5"-9.0"	5 / 20 mils	1. Making PCI length with minimum various 2. Length Require CLK33-2.5" 3. Length mismatch +/- 2.0"
CLK14 Clock			
CLK_SIO14 CLK_ICH14 CLK_TV14	2.0"-9.0"	5 / 20 mils	1. Length mismatch +/- 500 mils
CLK_ICH48 CLK_MCH48	3.5" - 12.5"	5 / 20 mils	

Clock Package Length
Banais Processor Package Length 495 mils
Monitor-GM CLKCH Package Length 1142 mils
CPU Socket Equivalent Length 157 mils

For X*TAL fin tunV0.4

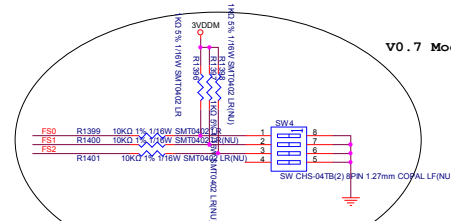
Clock Layout :

1. Close to Clock generator
2. Trace as short as possible and use 12 mil
3. Place crystal within 500 mils of CLK Generator

FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	PCI-EX
0	0	1	0	1	100.00M	66.67M	33.33M	100.00M
0	0	0	0	1	133.33M	66.67M	33.33M	100.00M
0	0	0	1	1	166.66M	66.67M	33.33M	100.00M
0	0	0	1	0	200.00M	66.67M	33.33M	100.00M

GND Shielding 10 mil space 5 mil space
DISPCLKI, DISPCLK0 10 mil space 5 mil space
GND Shielding 10 mil space 5 mil space

V0.7 Modify

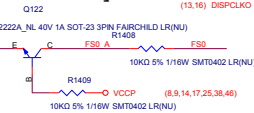


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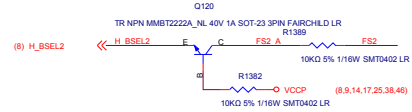
For CLK set up install V0.6

(10,11,13,16,17,18,19,20,21,22,23,24,25,26,27,29,34,36,37,38,42,45,46,48,52)

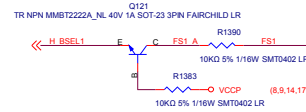
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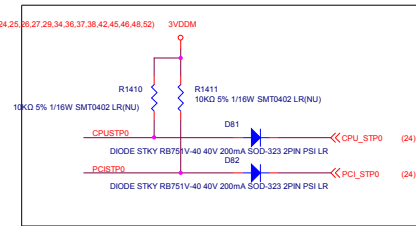
V0.7 Modify



V0.7 Modify



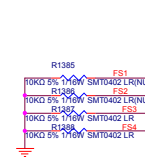
V0.7 modify



Mount these capacitor 2006.0602 Modify

- CLK14M_SB C732 10K 5% 1/16W SMT0402 NPO LR
- CLK14M_GU C729 10K 5% 1/16W SMT0402 NPO LR
- CLK48M_SB C230 10K 5% 1/16W SMT0402 NPO LR
- CLK48M_NB C697 10K 5% 1/16W SMT0402 NPO LR
- CLK48M_SB C688 10K 5% 1/16W SMT0402 NPO LR
- CLK33M_SB C241 10K 5% 1/16W SMT0402 NPO LR
- CLK33M_EC C238 10K 5% 1/16W SMT0402 NPO LR
- CLK33M_APIC C237 10K 5% 1/16W SMT0402 NPO LR
- CLK33M_KBC C235 10K 5% 1/16W SMT0402 NPO LR
- CLK33M_FWH C234 10K 5% 1/16W SMT0402 NPO LR
- CLK33M_MINI C231 10K 5% 1/16W SMT0402 NPO LR
- CPU_BCLK C709 10K 5% 1/16W SMT0402 NPO LR
- CPU_BCLK C704 10K 5% 1/16W SMT0402 NPO LR
- HCLKNB C707 10K 5% 1/16W SMT0402 NPO LR
- HCLKNB C708 10K 5% 1/16W SMT0402 NPO LR

V0.6 MODIFY 9/28



V0.6Modify



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File: **LM10W < VIA NR896 + VT8237A >**
Doc: **<Clock-Gen>**
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DDR CLOCK BUFFER

EMI solution 2006.0627

EMI solution 2006.0627

Mount these capacitor 2006.0602 Modify



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Title

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Size

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Document Number

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Rev

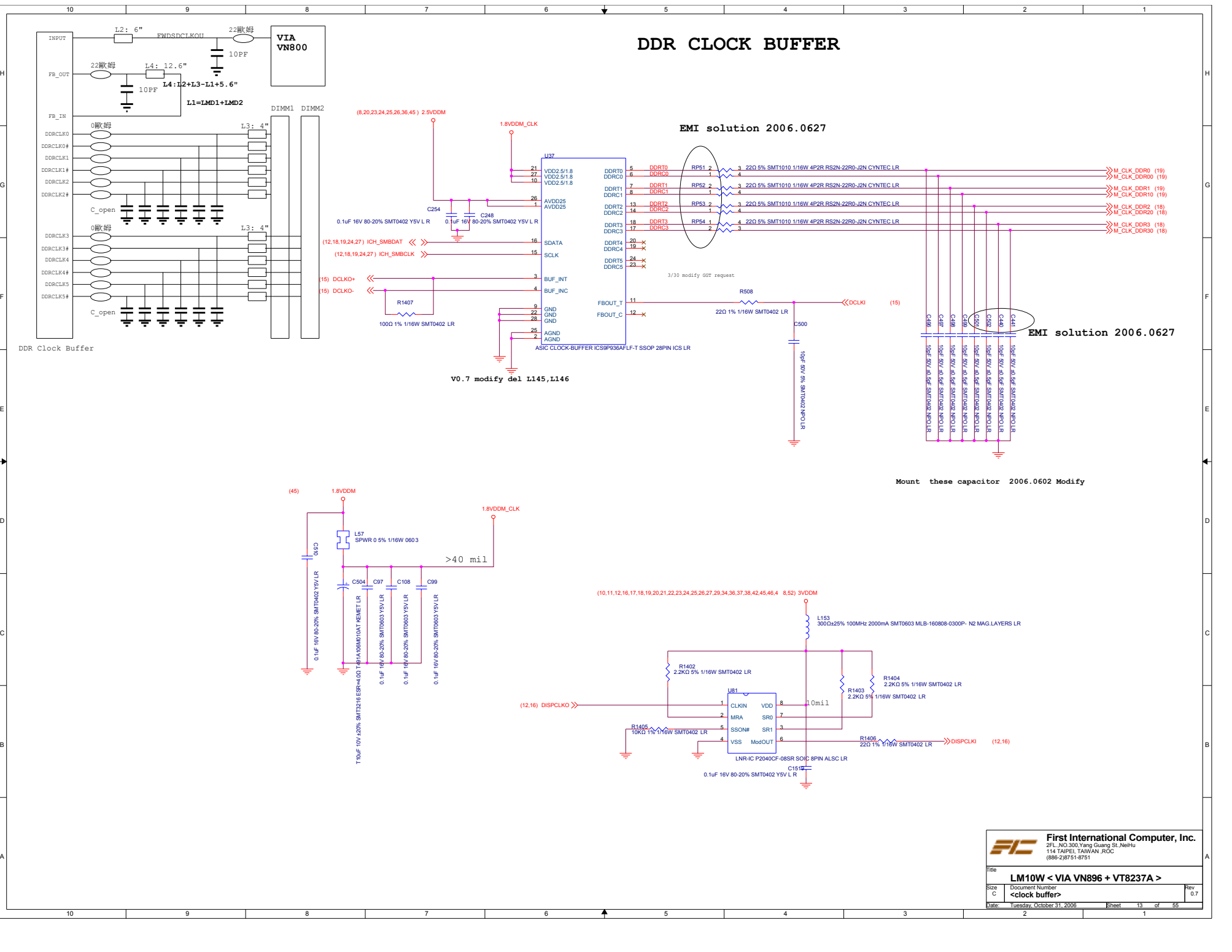
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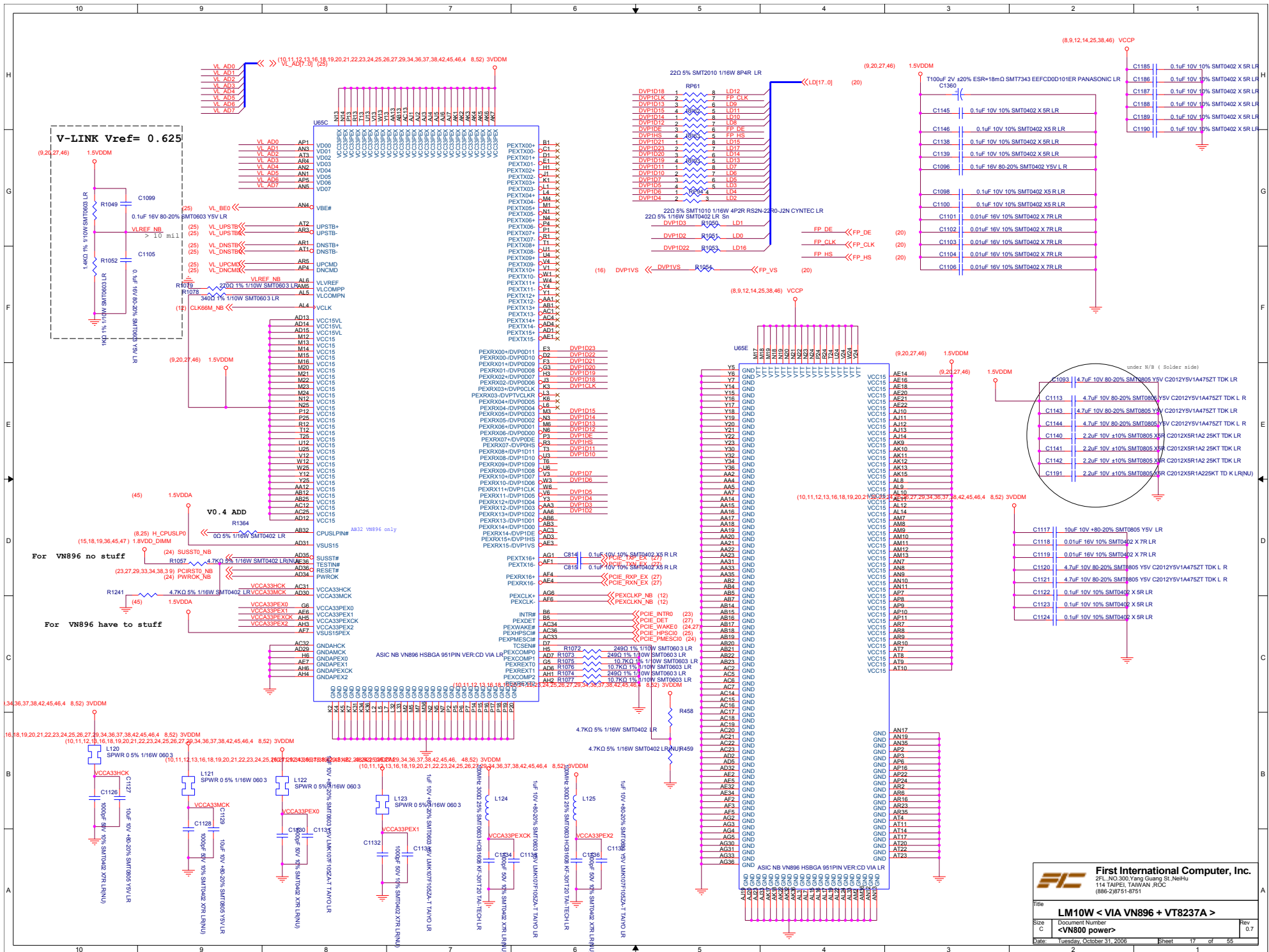
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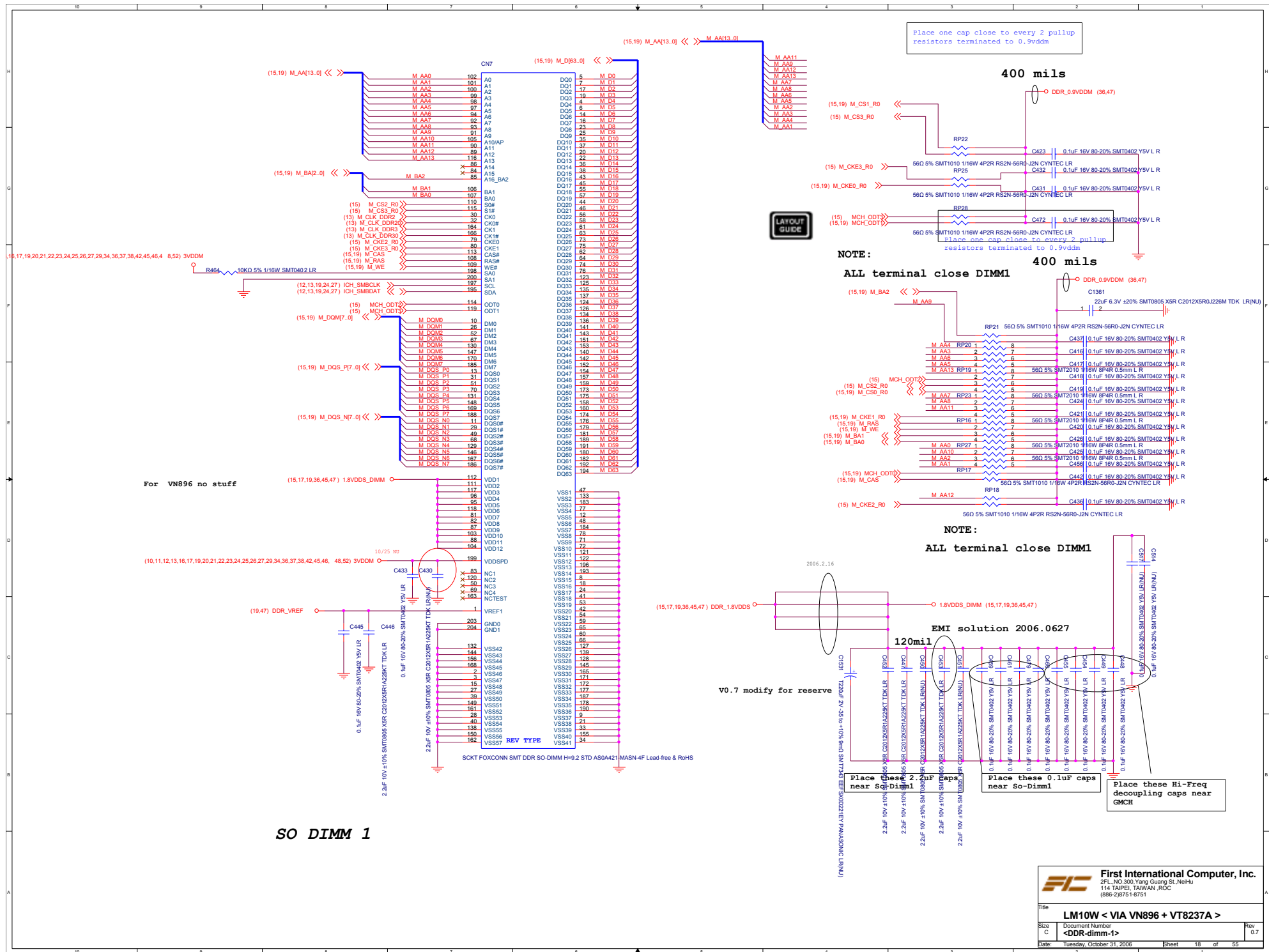
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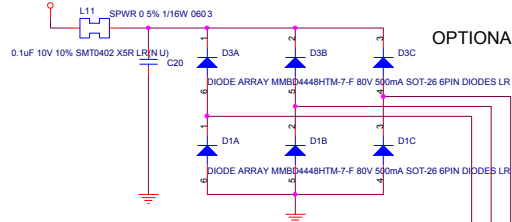
13 of 56





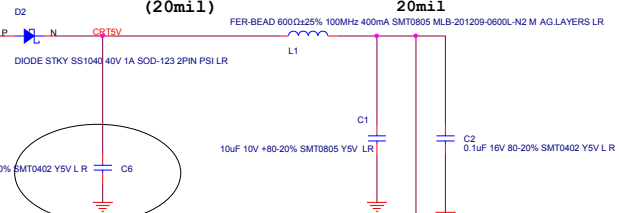


(11,24,26,29,32,34,35,36,37,41,42,46,48, 52) 5VDDM



OPTIONAL ESD PROTECTION DIODES

(11,24,26,29,32,34,35,36,37,41,42,46,48, 52) 5VDDM



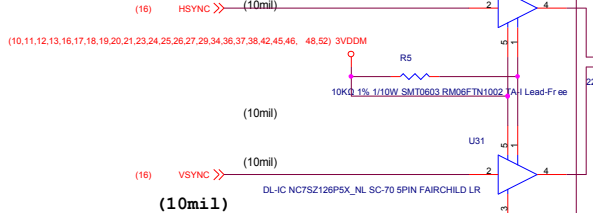
(20mil)

20mil

(16) RED << (10mil)
(16) GREEN << (10mil)
(16) BLUE << (10mil)

R1266 100 5% 1/10W SMT0603 LRL4 68nH ±5% SMT0805 CLH2012T-68NJ-S CHILISIN LR
R1267 100 5% 1/10W SMT0603 LRL3 68nH ±5% SMT0805 CLH2012T-68NJ-S CHILISIN LR
R1268 100 5% 1/10W SMT0603 LRL2 68nH ±5% SMT0805 CLH2012T-68NJ-S CHILISIN LR

(10mil) QVEDAT R400 SHW 0.5% 1/16W 0402
(10mil) QVECLK R402 SHW 0.5% 1/16W 0402



(16) HSYNC << (10mil)

(10,11,12,13,16,17,18,19,20,21,23,24,25,26,27,29,34,36,37,38,42,45,46, 48,52) 3VDDM

(10mil)

(16) VSYNC << (10mil)

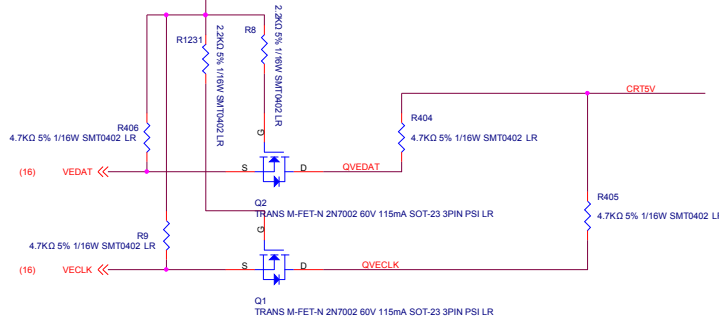
(10mil)

R0.4 Modify

2006.0706 change to 15pF for VESA SPEC 0703 change to 10pF for VESA SPEC

(10,11,12,13,16,17,18,19,20,21,23,24,25,26,27,29,34,36,37,38,42,45,46, 48,52) 3VDDM

V0.4 Modify



(16) VEDAT <<

(16) VECLK <<

First International Computer, Inc.	
2FL, NO.300 Yang Guang St, NeiHu 114 TAIPEI, TAIWAN, ROC (886-2)8751-8751	
Title	
LM10W < VIA VN896 + VT8237A >	
Size	Document Number
C	<CRT connector>
Date	Tuesday, October 31, 2006
Sheet	22 of 56
Rev	0.7

SB_VREF=0.45

V0.4 Modify

V0.7 Modify

(RP49 close to S/B)

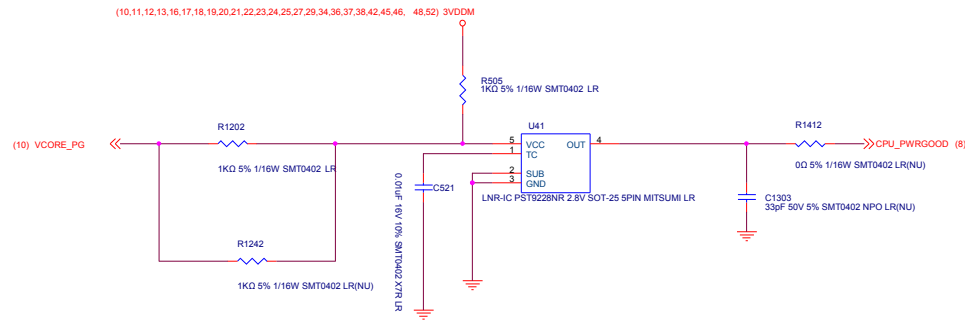
V0.4 EMI Modify

ADD PCIE_DET 2006.0705 Modify

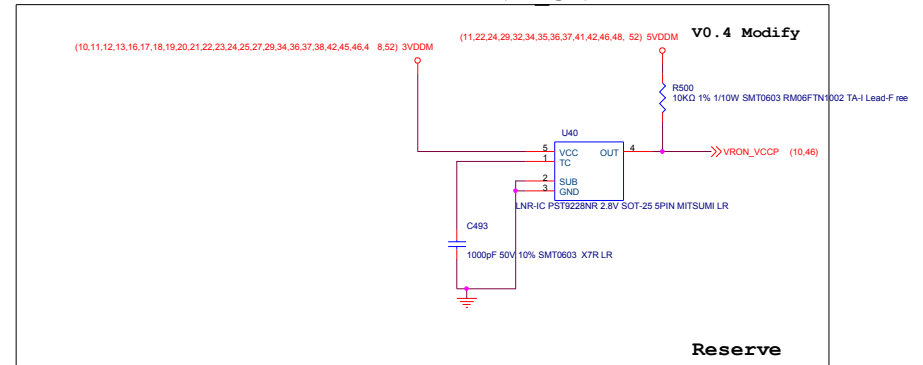
V0.4 EMI Modify

Follow VIA demo board to 2.5V V0.3

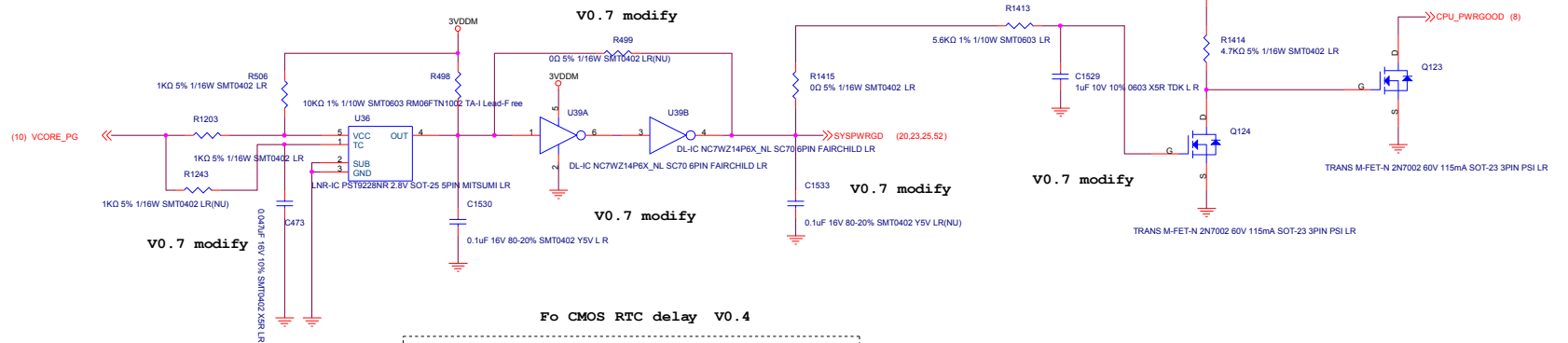
CPU POWER OK CIRCUIT



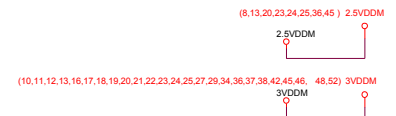
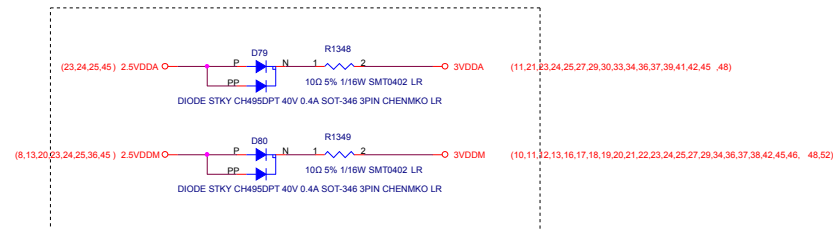
VR ON

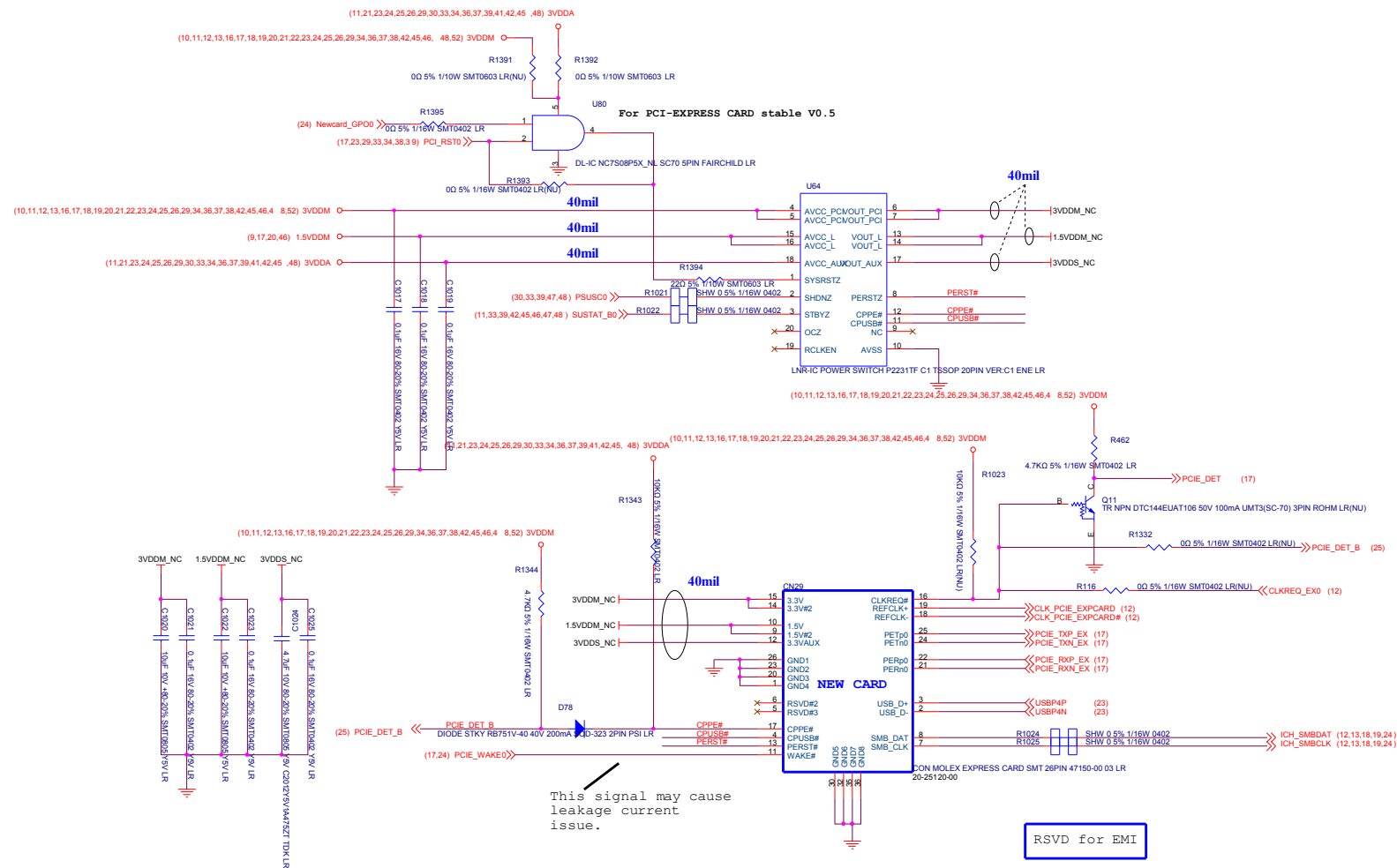


SYSTEM POWER OK CIRCUIT

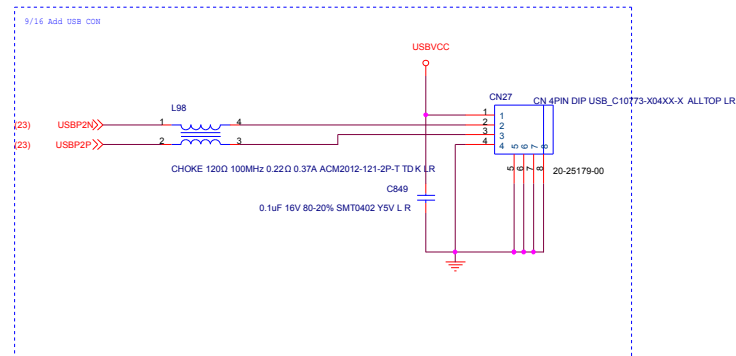
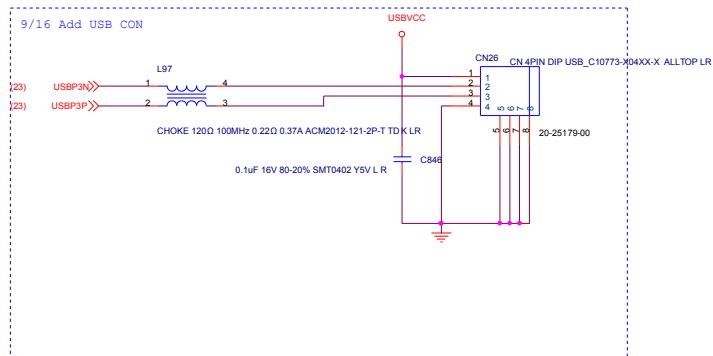
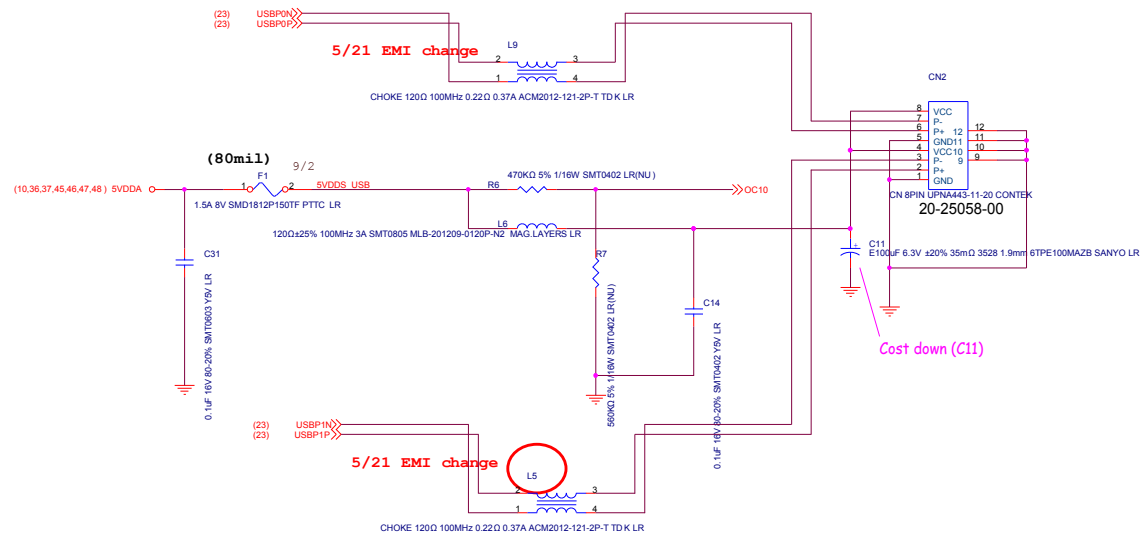
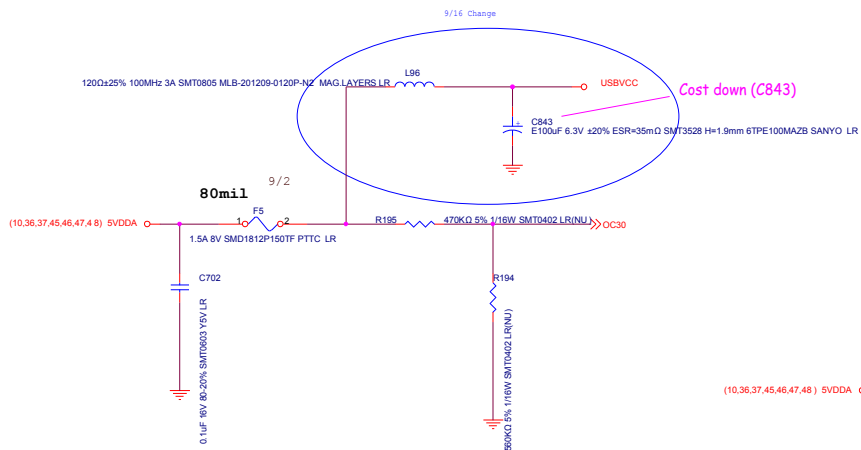


Fo CMOS RTC delay V0.4





[illegible]



NOTE

SATA differential stripline 20:5:6:5:20
SATA differential microstripline 20:6:6:6:20
請包GROUND



SATA Layout Note:

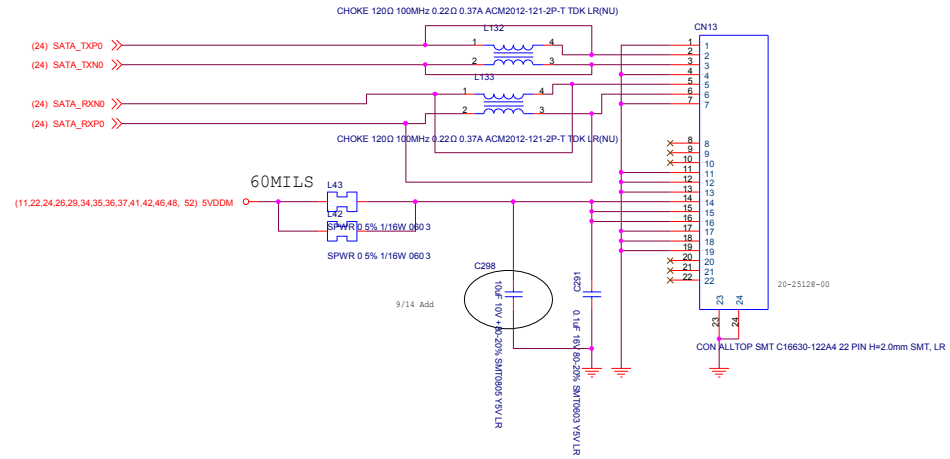
MS or SL:

6mils 6mils 20mils 6mils 6mils 20mils

TX

RX

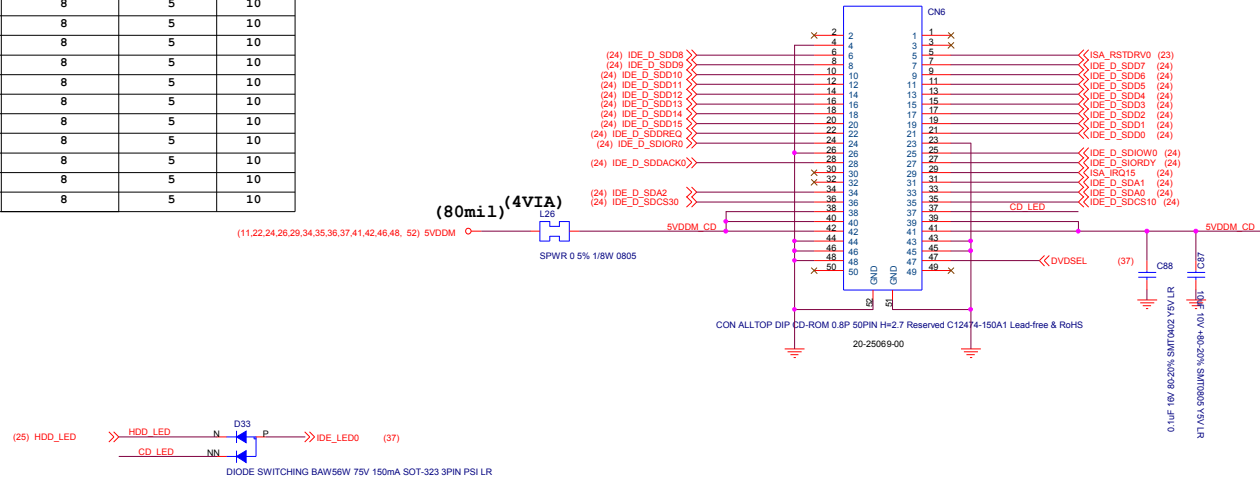
- * Zdiff = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
- * TX/RX trace length < 2 inches.
- * TX+/- need matching trace ±10 mils length.
- * RX+/- need matching trace ±10 mils length.
- * SATA Pair to Pair Trace matching trace ±10 mils length.



IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN

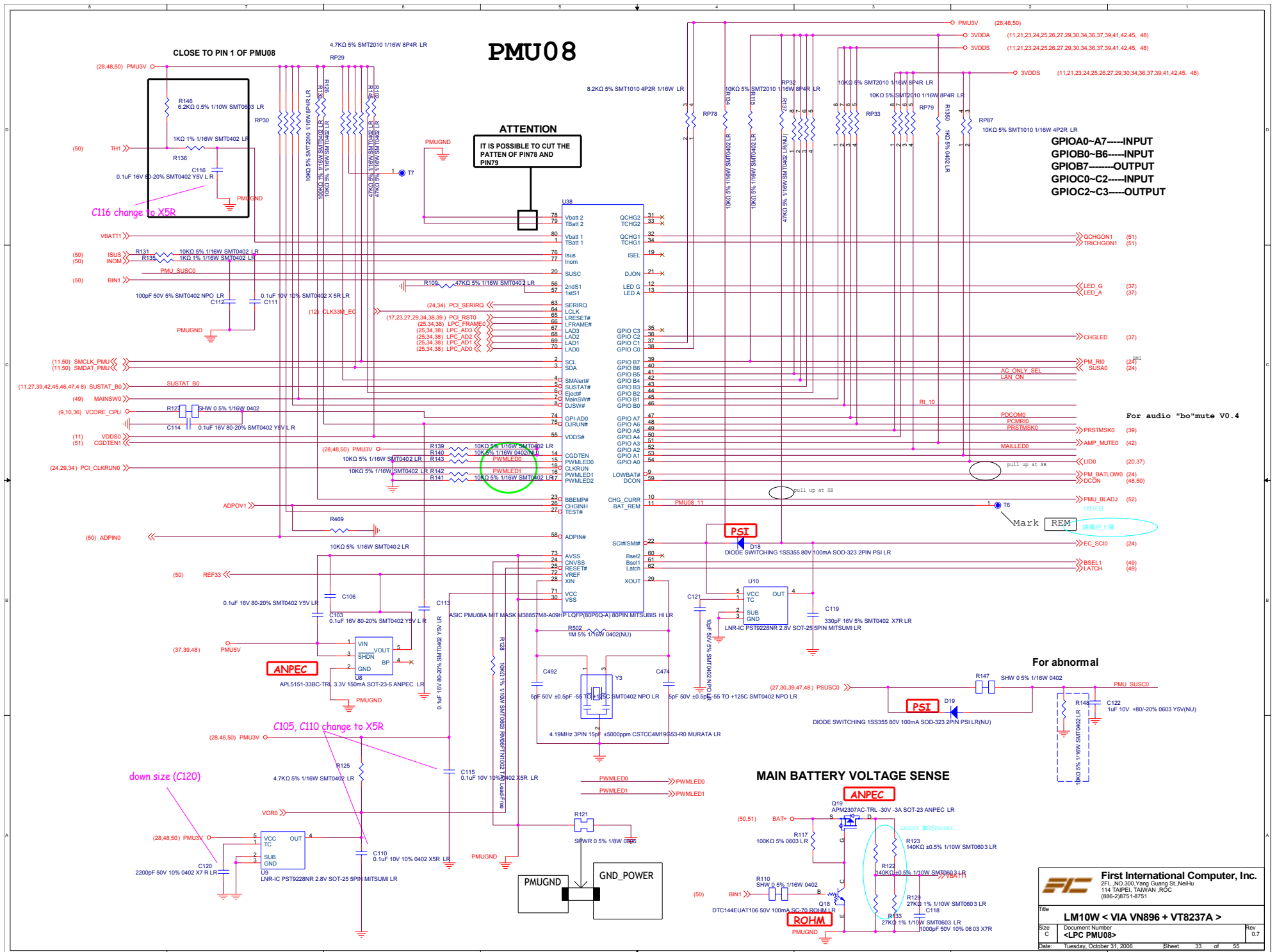


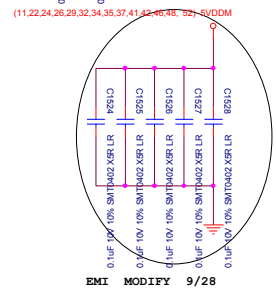
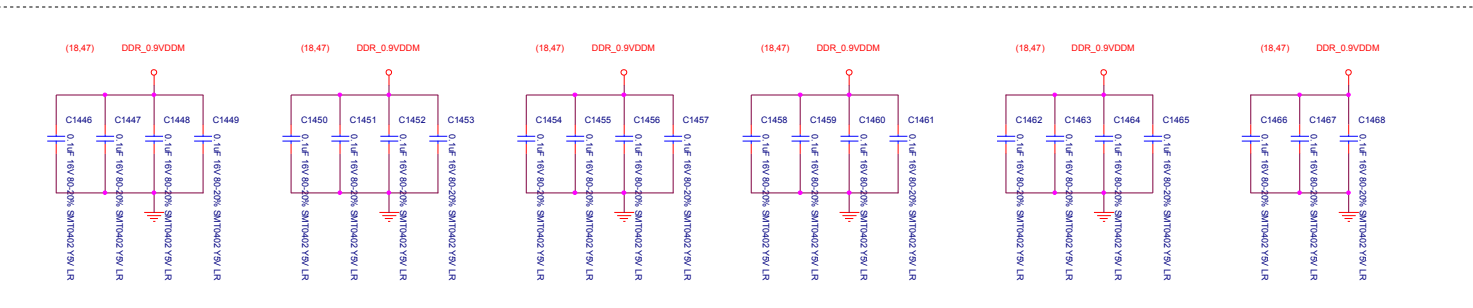
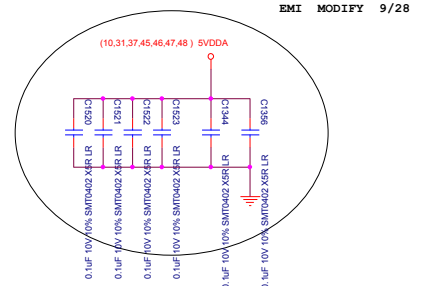
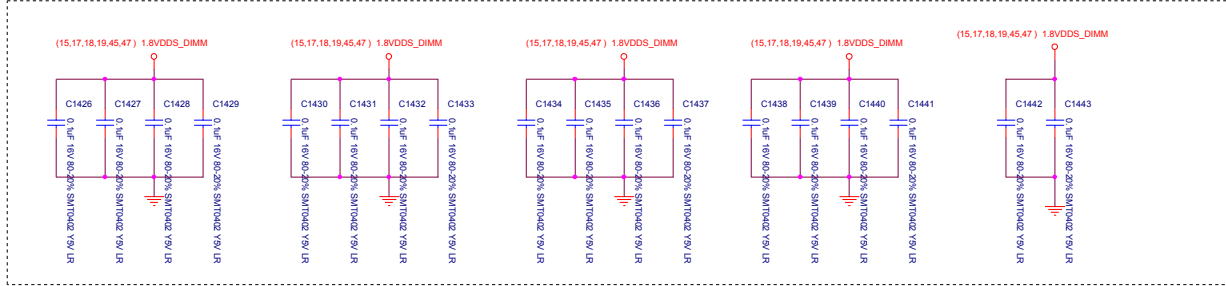
PMU08

ATTENTION

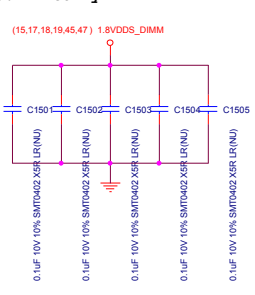
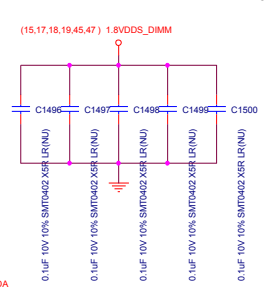
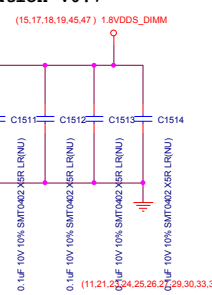
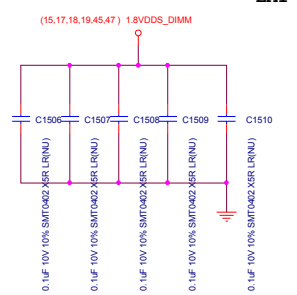
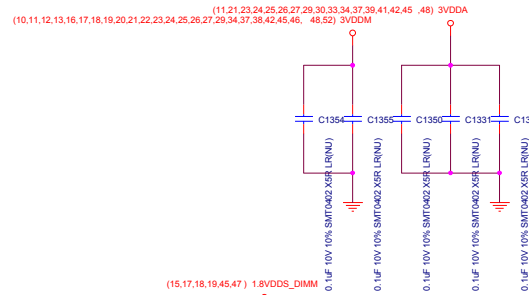
IT IS POSSIBLE TO CUT THE PATTERN OF PIN78 AND PIN79

GPIOA0-A7-----INPUT
GPIOB0-B6-----INPUT
GPIOB7-----OUTPUT
GPIOC0-C2-----INPUT
GPIOC2-C3-----OUTPUT

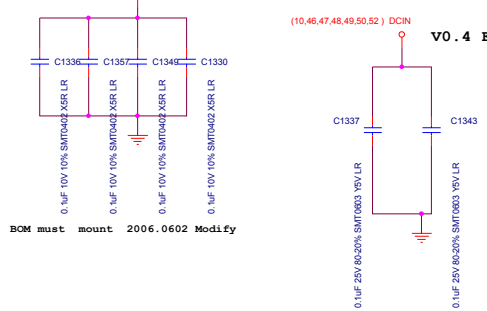




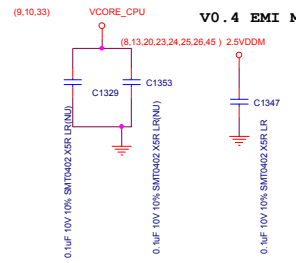
EMI solution V0.7



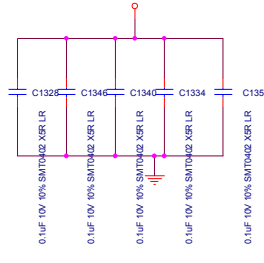
EMI V0.4 Modify



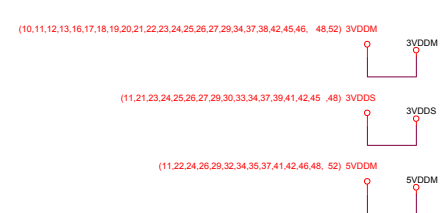
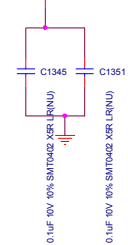
V0.4 EMI Modify



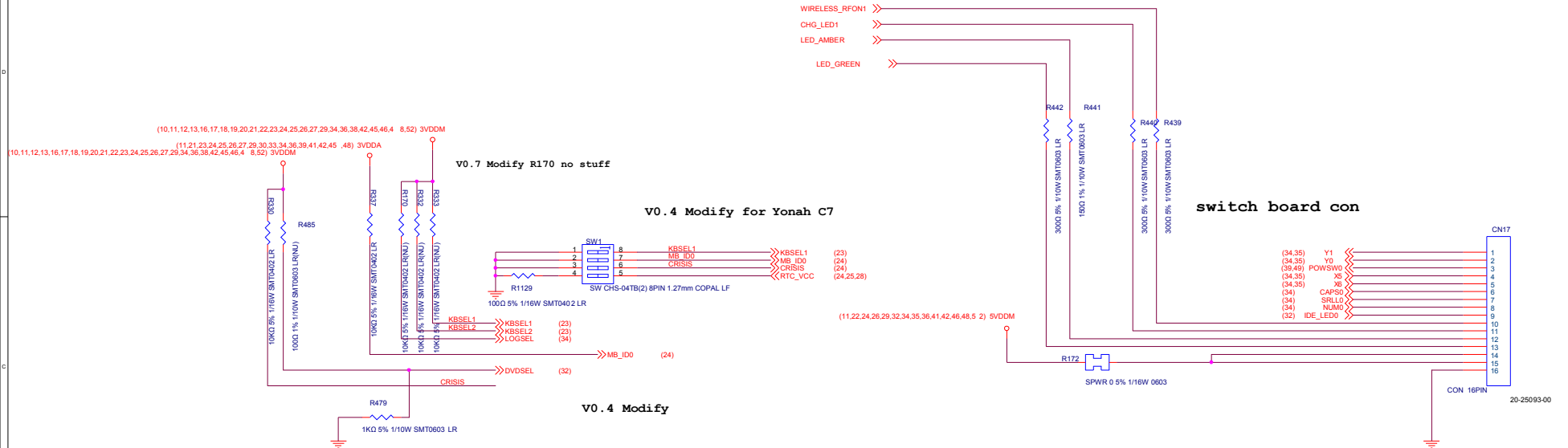
V0.4 EMI Modify



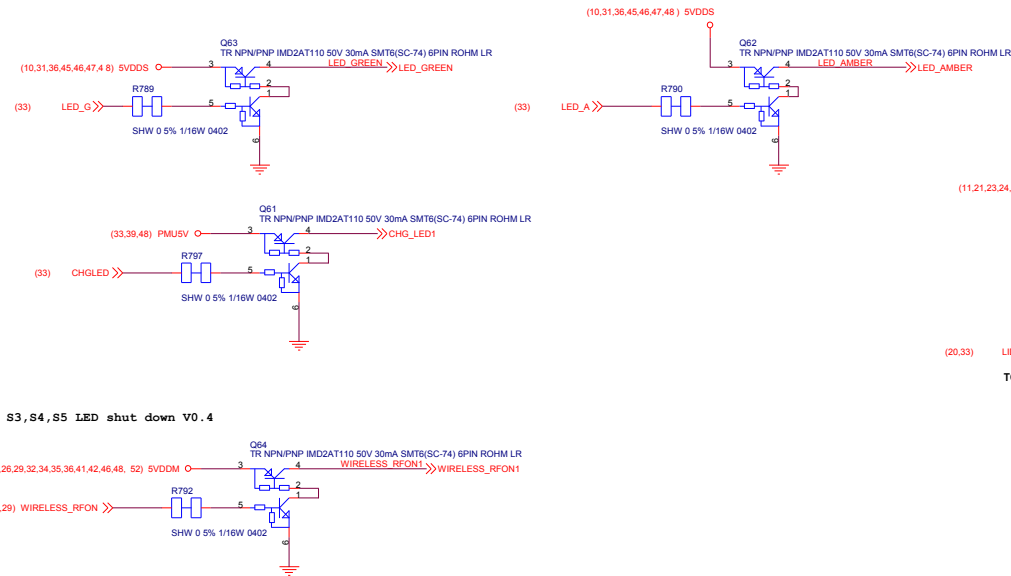
BOM must mount 2006.0602 Modify



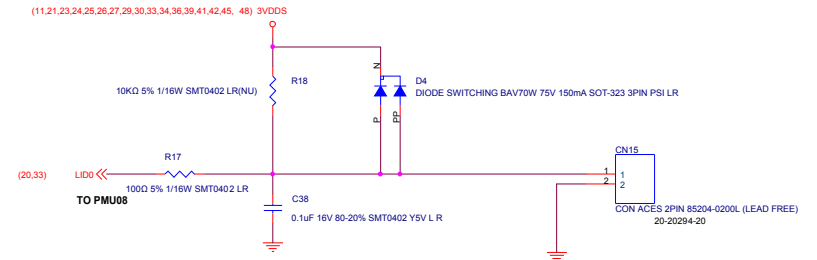
DIP SWITCH



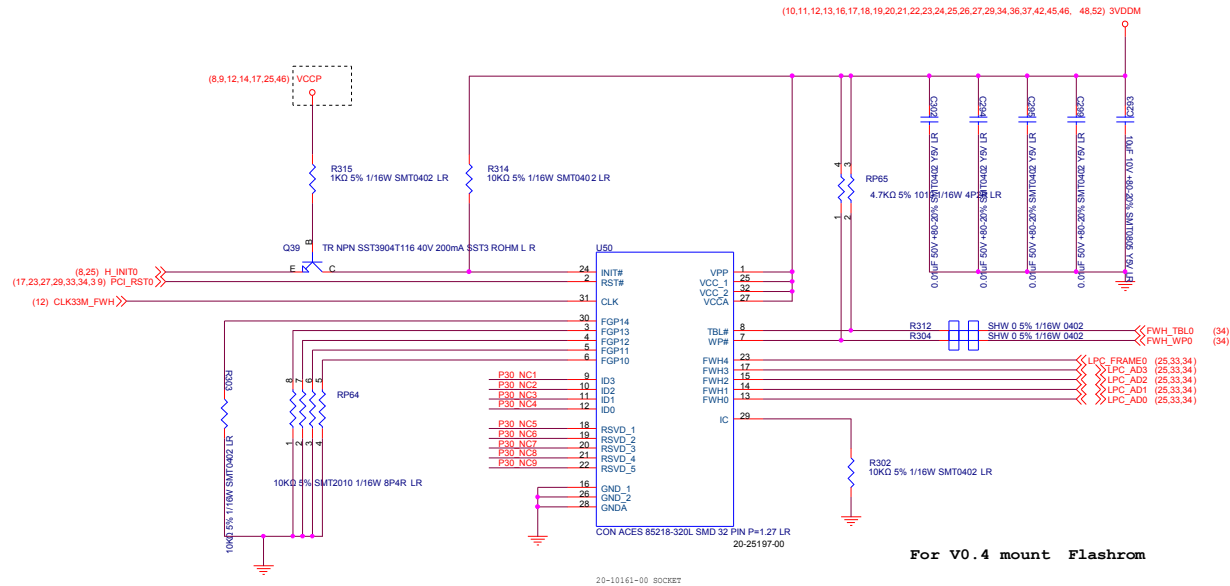
LED indicator control logic



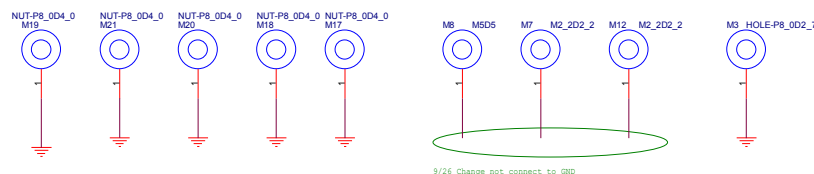
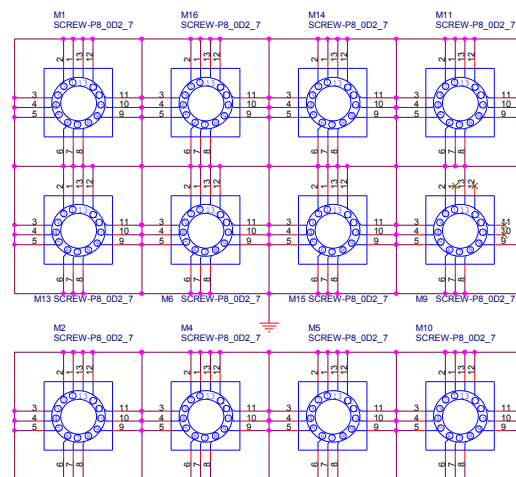
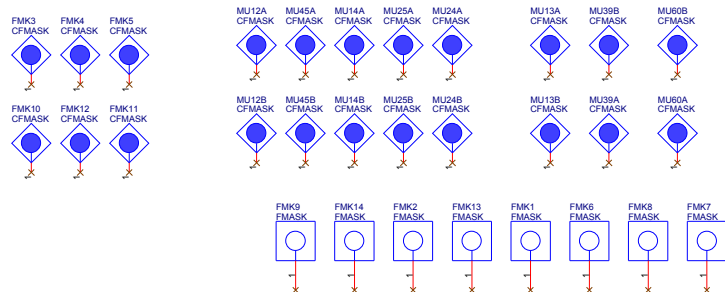
LID Switch



4M FLASH ROM

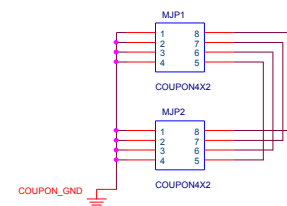


For V0.4 mount Flashrom

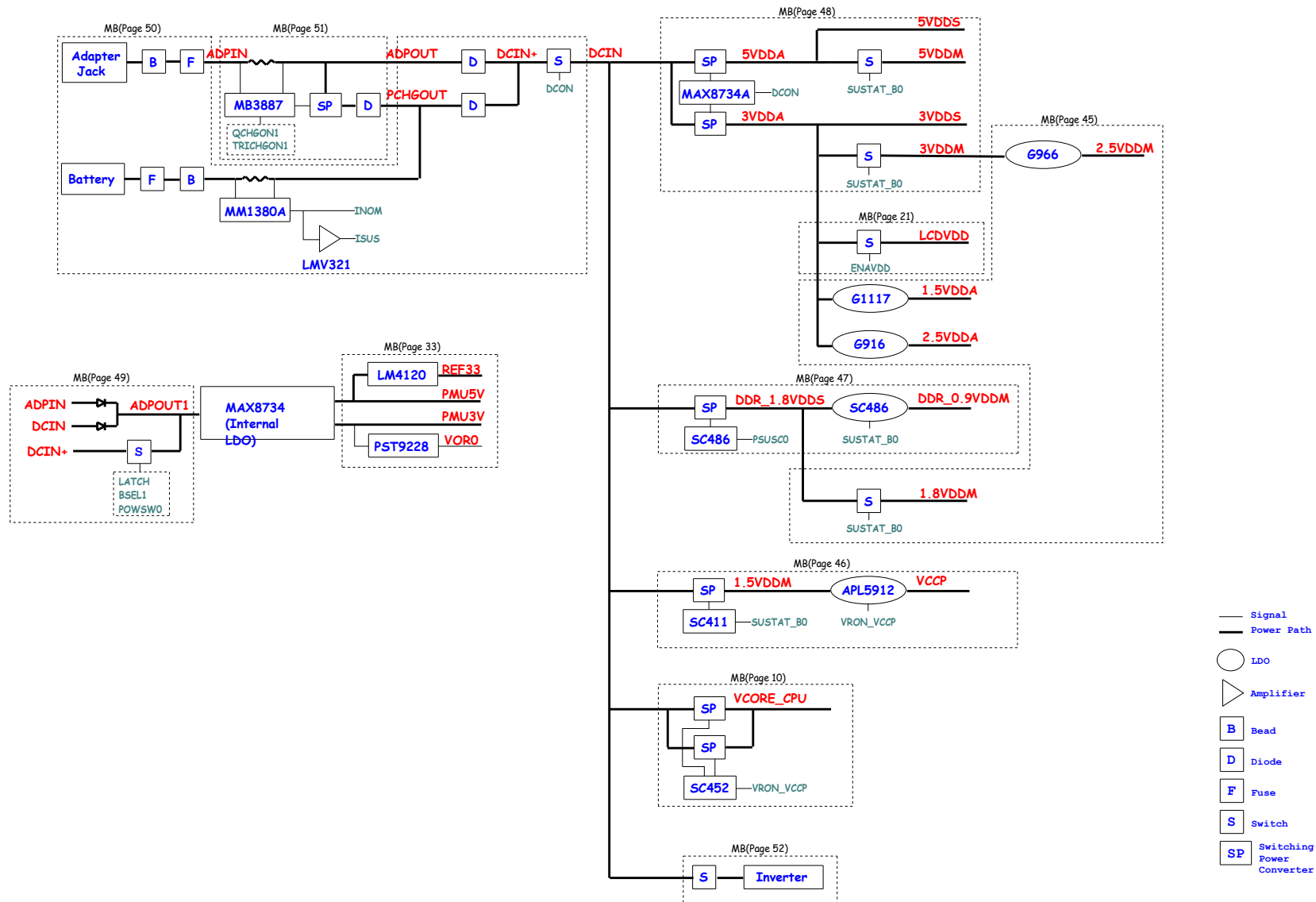


9/26 Change not connect to GND

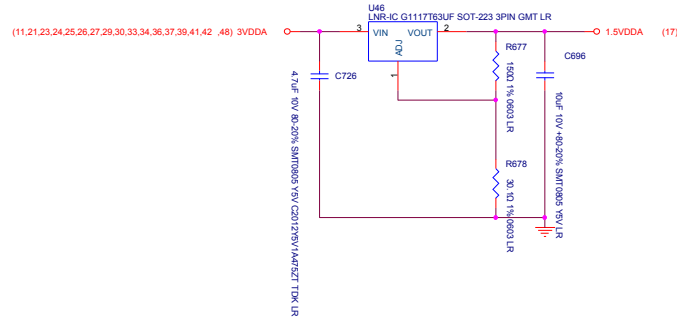
COUPON4X2



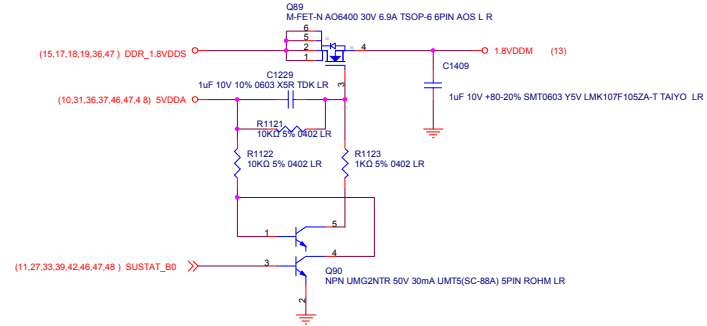
LM10W Power Block



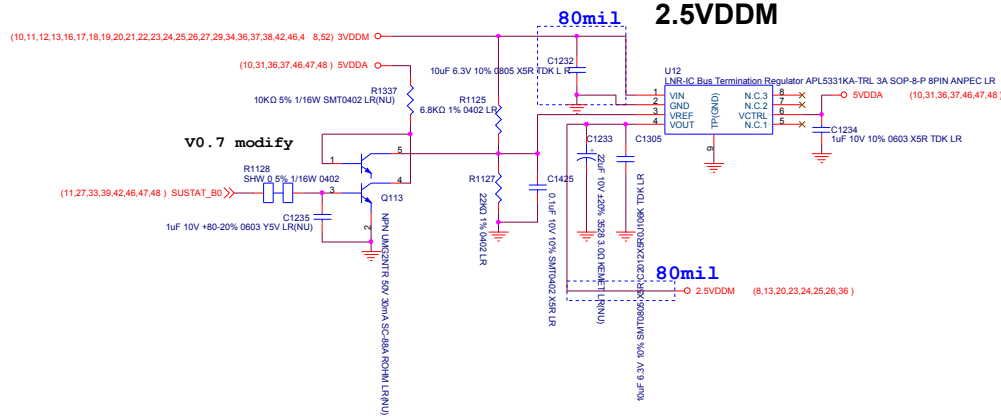
1.5VDDA 0.5A



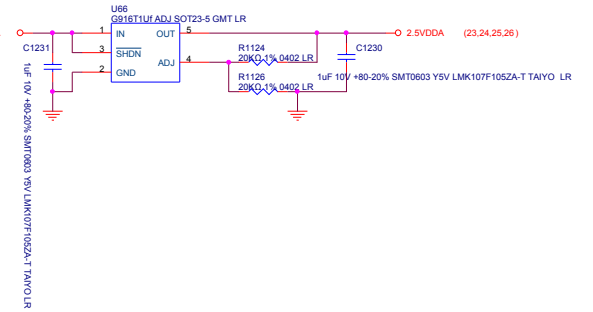
1.8VDDM 1.5A



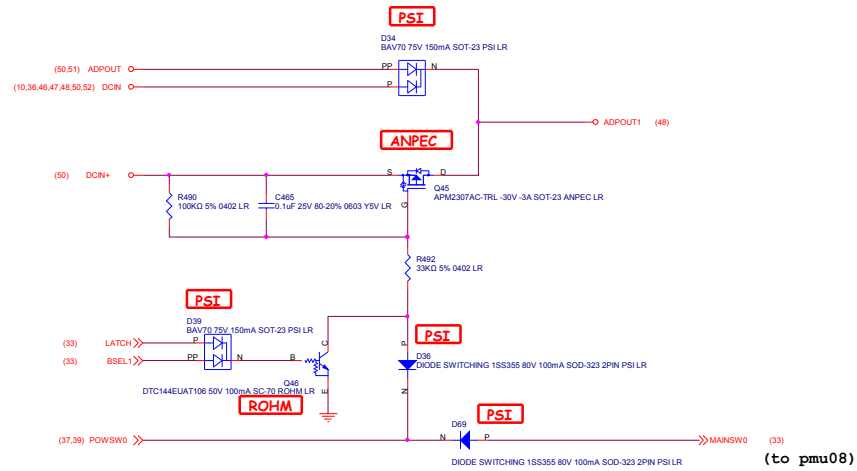
2.5VDDM



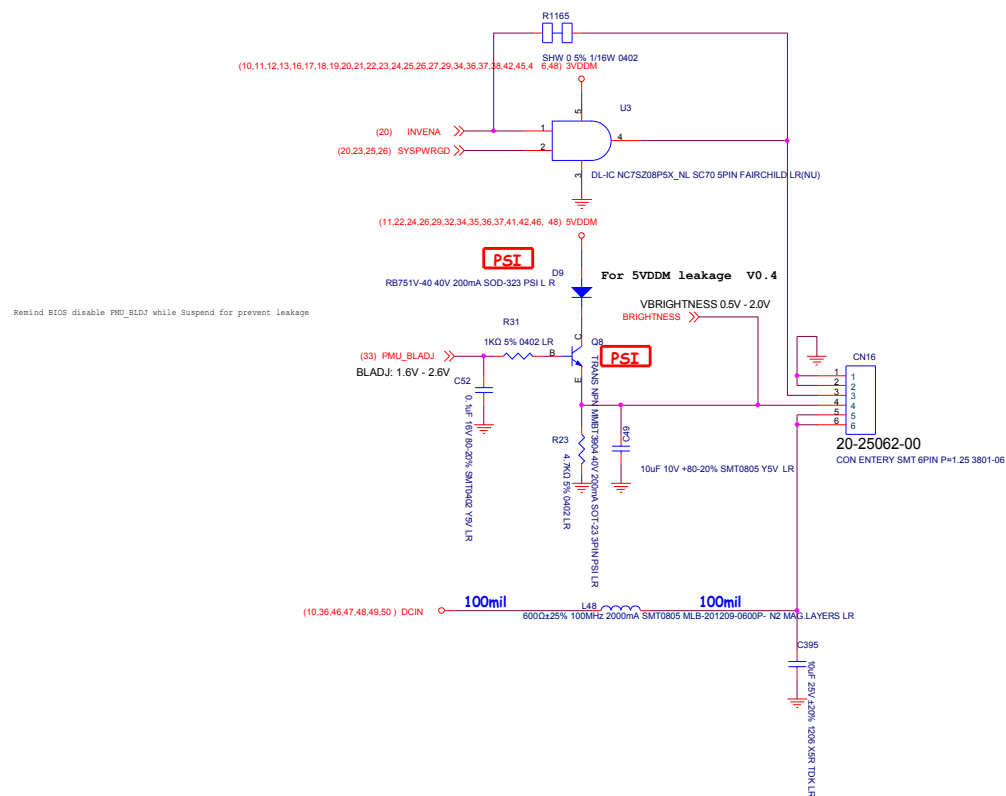
2.5VDDA 0.5A

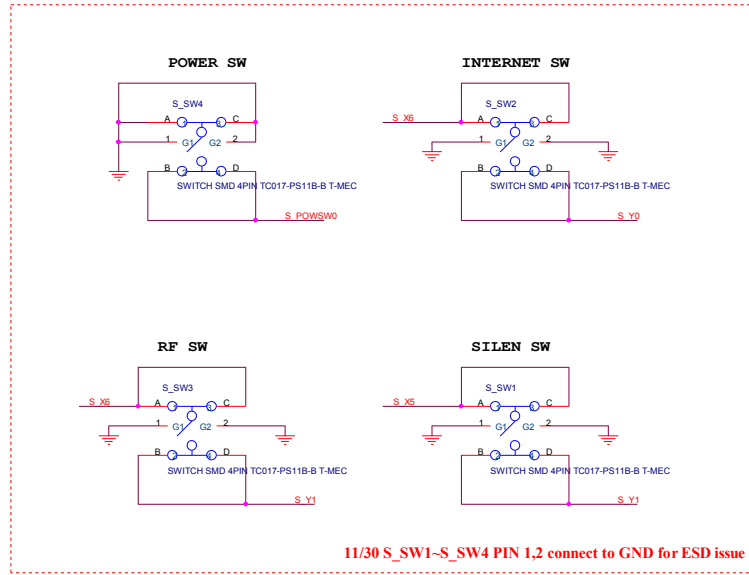
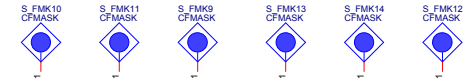
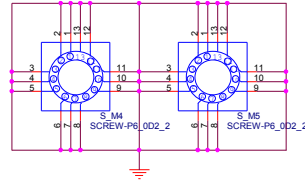






Inverter Connector





switch board con

