C560 TGL Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DY	***DUMMY, NOT ASM***
DDP/ SDP	***Memory down BOM Control***
DDR4_CTRL	***Memory down BOM Control***
MEM_IDx_x	***Memory ID for SW Team (BOM Control)***
PCB_ID	***PCB ID for SW Team (PCB version)***
SKU_ID	***SKU ID for SW Team (Model ID)***
DIS	***GPU***
PSL/ Non PSL	***Support / Non Support KBC Power Switched Logic***
AOU/Non AOU	***USB port AOU function***
EMC/DY-EMC	***EMI team suggest***
Wlan Non-PS	***Support WLAN type***
LC56_14T/ LC56_15T	***Difference between 14T and 15T***

C560

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***COVER PAGE***

Size	Document Number	Rev
A3	C560-TGL	-1

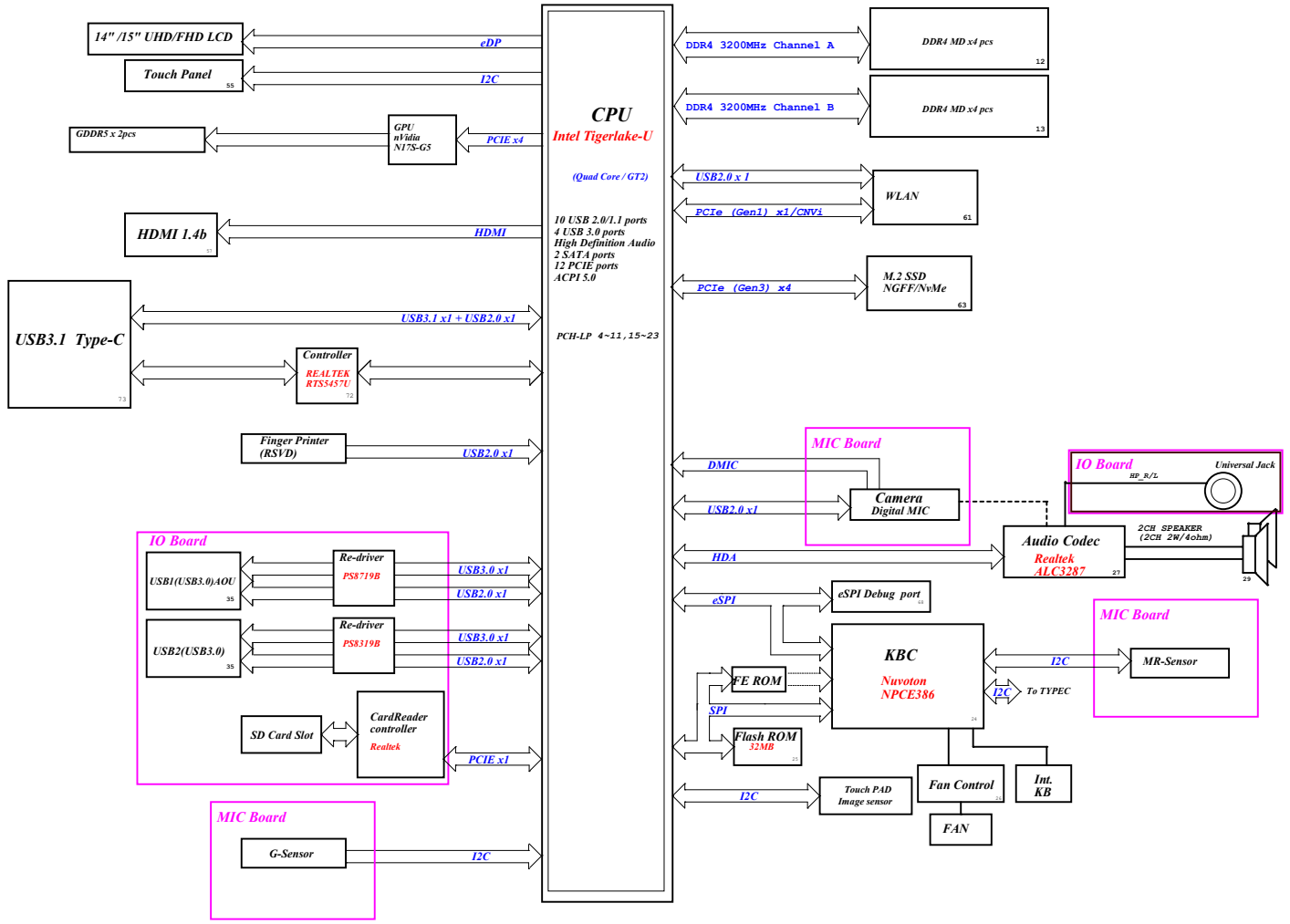
Date: Saturday, August 15, 2020 Sheet 1 of 106

C560 TGL Block Diagram

Project code: LC56-14T
4PD0K101C001
LC56-15T
4PD0K101E001

PCB P/N: 203013
Revision: -1

IO/Sensor BD



PCB Layer Stackup

L1: Signal
L2: GND/POWER
L3: Signal
L4: Signal
L5: GND/POWER
L6: Signal
L7: GND/POWER
L8: Signal

Battery Charger/Selector	
BQ25710RSNR-GP	44
20V_IN	19V_DCBATOUT BT~
System DC/DC	
TPS51393PRJER-GP	
TPS51395PRJER-GP	45
19V_DCBATOUT	PWR_5V PWR_3D3V
CPU_VCORE	
RT3612EBGQW-1-GP	46
1V_CPU_CORE	
AOE6936	47
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCAUX	
MP2941BGL-C669-Z-GP	50
19V_DCBATOUT	1D8V_VCCIN_AUX
DC/DC 1D2V_S3	
TPS51486RJER-GP	51
19V_DCBATOUT	1D2V_S3
DC/DC 0D6V_VREF_S0	
TPS51486RJER-GP	51
5V_S5	0D6V_VREF_S0
DC/DC 1D8V_S5	
RT5797ALGQW-GP	53
19V_DCBATOUT	1D8V_S5

C560

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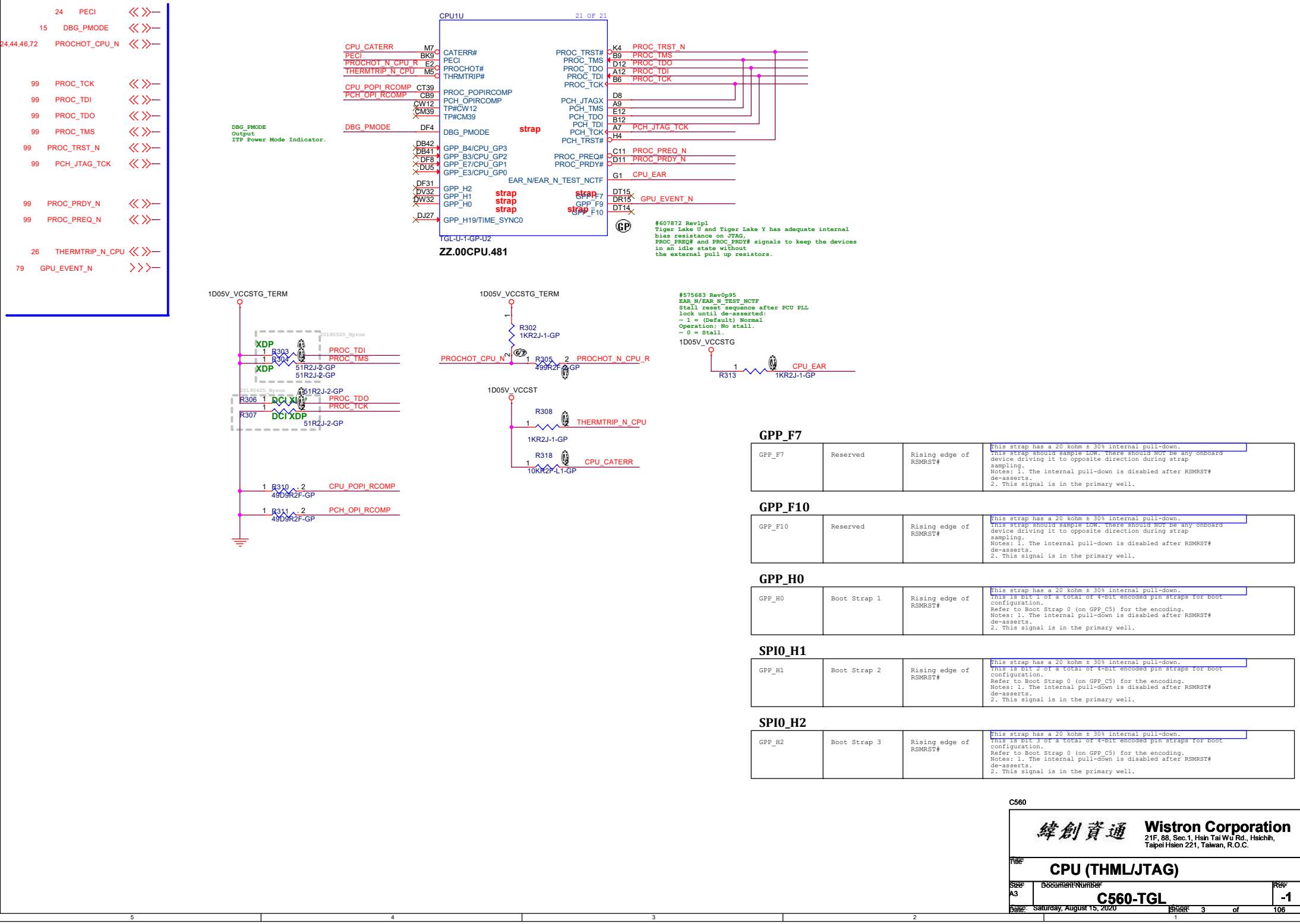
Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 2 of 55



GPP_F7

GPP_F7	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_F10

GPP_F10	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H0

GPP_H0	Boot Strap 1	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 1 of a total of 4-bit encoded pin straps for boot configuration. Refer to Boot Strap 0 (on GPP_C5) for the encoding. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SPI0_H1

GPP_H1	Boot Strap 2	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 2 of a total of 4-bit encoded pin straps for boot configuration. Refer to Boot Strap 0 (on GPP_C5) for the encoding. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SPI0_H2

GPP_H2	Boot Strap 3	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 3 of a total of 4-bit encoded pin straps for boot configuration. Refer to Boot Strap 0 (on GPP_C5) for the encoding. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

C560

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Title: CPU (THML/JTAG)

Size: A3 | Document Number: C560-TGL | Rev: -1

Date: Saturday, August 15, 2020 | Sheet 3 of 106

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 L_BKLT_EN
40,55 eDP_VDDEN_CPU
55 L_BKLT_CTRL
55 eDP_HPD_CPU

USB-C Port2

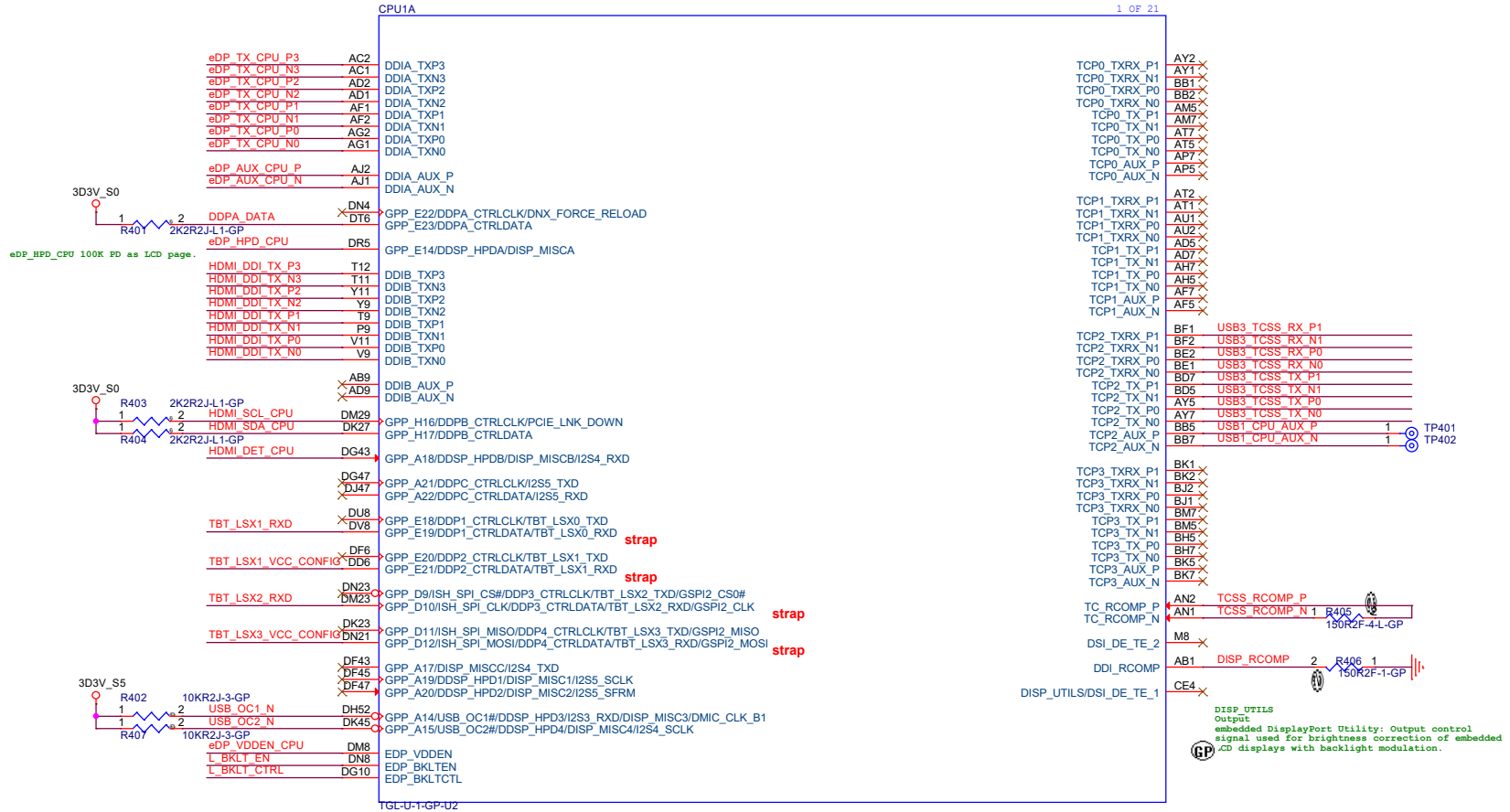
73 USB3_TCSS_TX_P0
73 USB3_TCSS_TX_N0
73 USB3_TCSS_TX_P1
73 USB3_TCSS_TX_N1
73 USB3_TCSS_RX_P0
73 USB3_TCSS_RX_N0
73 USB3_TCSS_RX_P1
73 USB3_TCSS_RX_N1

HDMI

57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DET_CPU
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU

Others

15 TBT_LSX1_VCC_CONFIG
15 TBT_LSX3_VCC_CONFIG
15 TBT_LSX2_RXD
15 TBT_LSX1_RXD



NOTE:
"eDP_HPD_CPU"
"eDP_VDDEN_CPU"
"L_BKLT_EN"
"L_BKLT_CTRL"
PD 100K to LCD side

ZZ.00CPU.481

C560

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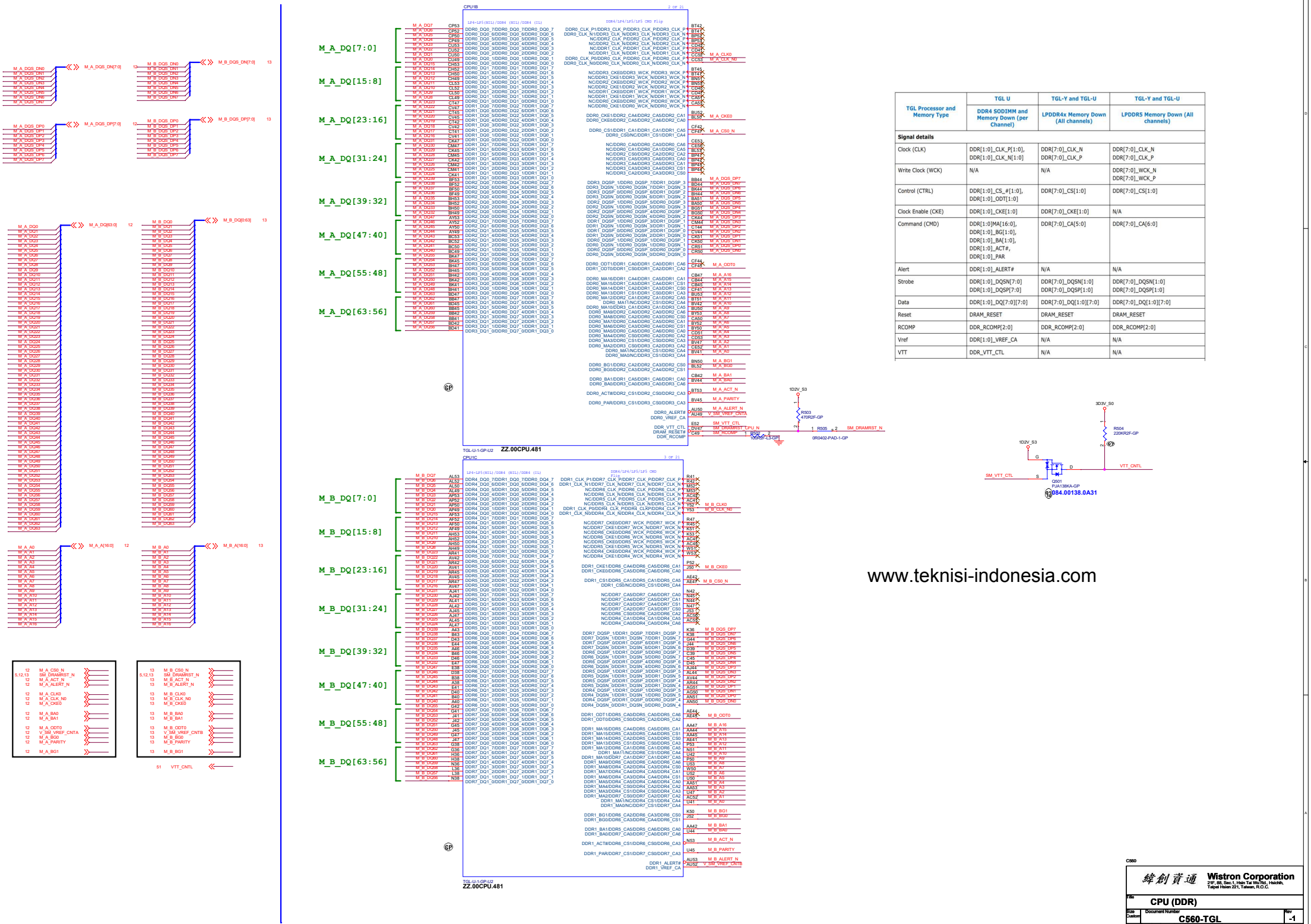
Title: CPU (DDI/EDP/TBT/TPC/)

Size	Document Number	Rev
A3	C560-TGL	-1

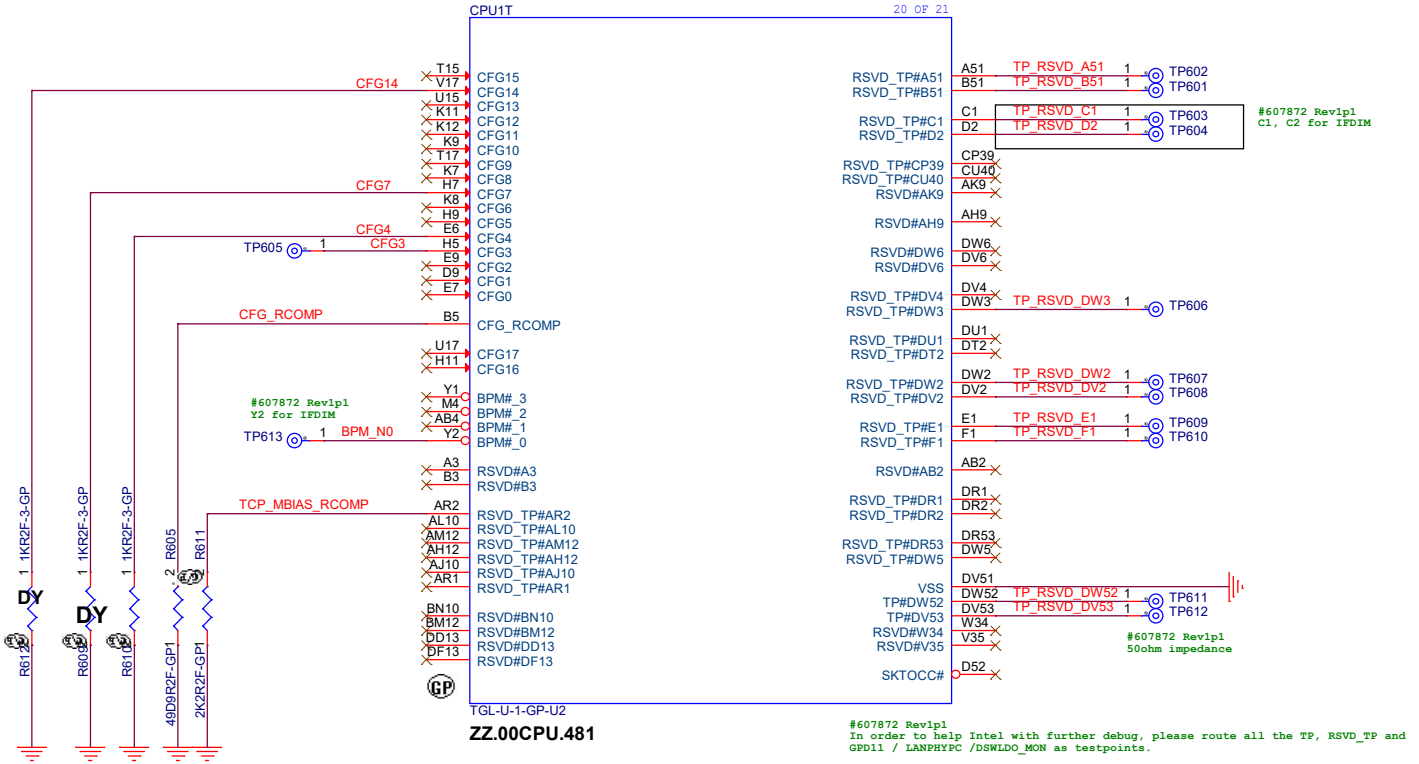
Date: Saturday, August 15, 2020 Sheet 4 of 106



TGL Processor and Memory Type	TGL U	TGL-Y and TGL-U	TGL-Y and TGL-U
	DDR4 SODIMM and Memory Down (per Channel)	LPDDR4x Memory Down (All channels)	LPDDR5 Memory Down (All channels)
Signal details			
Clock (CLK)	DDR[1:0]_CLK_P[1:0], DDR[1:0]_CLK_N[1:0]	DDR[7:0]_CLK_N DDR[7:0]_CLK_P	DDR[7:0]_CLK_N DDR[7:0]_CLK_P
Write Clock (WCK)	N/A	N/A	DDR[7:0]_WCK_N DDR[7:0]_WCK_P
Control (CTRL)	DDR[1:0]_CS_#[1:0], DDR[1:0]_ODT[1:0]	DDR[7:0]_CS[1:0]	DDR[7:0]_CS[1:0]
Clock Enable (CKE)	DDR[1:0]_CKE[1:0]	DDR[7:0]_CKE[1:0]	N/A
Command (CMD)	DDR[1:0]MA[16:0], DDR[1:0]_BG[1:0], DDR[1:0]_BA[1:0], DDR[1:0]_ACT#, DDR[1:0]_PAR	DDR[7:0]_CA[5:0]	DDR[7:0]_CA[6:0]
Alert	DDR[1:0]_ALERT#	N/A	N/A
Strobe	DDR[1:0]_DQSN[7:0] DDR[1:0]_DQSP[7:0]	DDR[7:0]_DQSN[1:0] DDR[7:0]_DQSP[1:0]	DDR[7:0]_DQSN[1:0] DDR[7:0]_DQSP[1:0]
Data	DDR[1:0]_DQ[7:0][7:0]	DDR[7:0]_DQ[1:0][7:0]	DDR[7:0]_DQ[1:0][7:0]
Reset	DRAM_RESET	DRAM_RESET	DRAM_RESET
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]
Vref	DDR[1:0]_VREF_CA	N/A	N/A
VTT	DDR_VTT_CTL	N/A	N/A

絳創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**CPU (DDR)**		
Size: Custom	Document Number: **C560-TGL**		Rev: -1
Date: Saturday, August 15, 2020	Sheet 5 of 106		

#575683 Rev0p95
CFG[17:0]
Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.
• CFG[3], CFG[0]: Reserved configuration lane.
• CFG[2]: TGL UP4/UP3 Reserved
• CFG[2]: TGL H PCI Express* Static x16 Lanes Numbering Reversal.Reserved
• CFG[4]: eDP enable:
– 1 = Disabled.
– 0 = Enabled.
• CFG[6:5]: TGL UP4/UP3 Reserved
• CFG[6:5]: TGL H PCI Express* Bifurcation
– 00 = 1 x8, 2 x4 PCI Express*
– 01 = reserved
– 10 = 2 x8 PCI Express*
– 11 = 1 x16 PCI Express*
• CFG[7]: PEG Training:
– 1 = (default) PEG Train immediately following RESET# de assertion.
– 0 = PEG Wait for BIOS for training.
• CFG[13:8]: Reserved configuration lanes.
• CFG[14]: PEG60 (PCIE4) Lane Reversal.
– 1 - (Default) Normal
– 0 - Reversed
• CFG[17:15]: Reserved configuration lanes.



C560

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Title: CPU (CFG/IST)		
Size: B	Document Number: C560-TGL	Rev: -1
Date: Saturday, August 15, 2020	Sheet 6 of 106	

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_ALERT_N_CPU
46 SVID_CLK_CPU
46 SVID_DATA_CPU

VCCIN
Input
Input FIVR, Processor IA Cores and Graphics Power Rail.

1V_CPU_CORE
(55A)

CPU1M
13 OF 21

A24	VCCIN	VCCIN	G32
A26	VCCIN	VCCIN	H24
A29	VCCIN	VCCIN	H26
A30	VCCIN	VCCIN	H30
A33	VCCIN	VCCIN	H32
A35	VCCIN	VCCIN	J1
AY39	VCCIN	VCCIN	J2
B24	VCCIN	VCCIN	K1
B26	VCCIN	VCCIN	K2
B29	VCCIN	VCCIN	K24
B30	VCCIN	VCCIN	K26
B33	VCCIN	VCCIN	K30
B35	VCCIN	VCCIN	K32
BA10	VCCIN	VCCIN	L24
BA40	VCCIN	VCCIN	L26
BB39	VCCIN	VCCIN	L30
BB9	VCCIN	VCCIN	L32
BC10	VCCIN	VCCIN	N24
BC40	VCCIN	VCCIN	N26
BD39	VCCIN	VCCIN	N30
BD9	VCCIN	VCCIN	N32
BE10	VCCIN	VCCIN	P24
BE40	VCCIN	VCCIN	P26
BF9	VCCIN	VCCIN	P28
BG10	VCCIN	VCCIN	P30
BG40	VCCIN	VCCIN	P32
BH12	VCCIN	VCCIN	T21
BH39	VCCIN	VCCIN	T23
BH9	VCCIN	VCCIN	T25
BJ10	VCCIN	VCCIN	T27
BJ40	VCCIN	VCCIN	T31
BK39	VCCIN	VCCIN	U23
BL10	VCCIN	VCCIN	U27
BL40	VCCIN	VCCIN	U29
BM39	VCCIN	VCCIN	U31
BN40	VCCIN	VCCIN	U33
BP12	VCCIN	VCCIN	V23
BP39	VCCIN	VCCIN	V25
BR10	VCCIN	VCCIN	V27
BR40	VCCIN	VCCIN	V29
BT12	VCCIN	VCCIN	V31
BT39	VCCIN	VCCIN	V33
BU10	VCCIN	VCCIN	W22
BU40	VCCIN	VCCIN	W24
BV12	VCCIN	VCCIN	W28
BY12	VCCIN	VCCIN	W32
CA10	VCCIN	VCCIN	
CB12	VCCIN		
D24	VCCIN	VCCIN_SENSE	R38 VCCCORE_SENSE
D26	VCCIN	VSSIN_SENSE	R37 VSSCORE_SENSE
D29	VCCIN		
D30	VCCIN	VIDSOUT	M12 SVID_DATA_CPU
D33	VCCIN	VIDSCK	M11 SVID_CLK_CPU
D35	VCCIN	VIDALERT#	P12 SVID_ALERT_N_CPU_R
E24	VCCIN		
E26	VCCIN		
E27	VCCIN		
E29	VCCIN		
E30	VCCIN		
E32	VCCIN		
E33	VCCIN		
G2	VCCIN		
G24	VCCIN		
G26	VCCIN		
G30	VCCIN		

TGL-U-1-GP-U2

ZZ.00CPU.481

1V_CPU_CORE

SVID DATA

1D05V_VCCST
R701 100R2F-L1-GP-U
SVID_DATA_CPU

SVID ALERT

1D05V_VCCST
R702 56R2J-4-GP
SVID_ALERT_N_CPU
R703 0R0402-PAD-1-GP
SVID_ALERT_N_CPU_R

Layout note:
3.Length matchin 25mil, and close SOC in 2inch "

1V_CPU_CORE
R704 100R2F-L1-GP-U VCCCORE_SENSE
R705 100R2F-L1-GP-U VSSCORE_SENSE

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

C560

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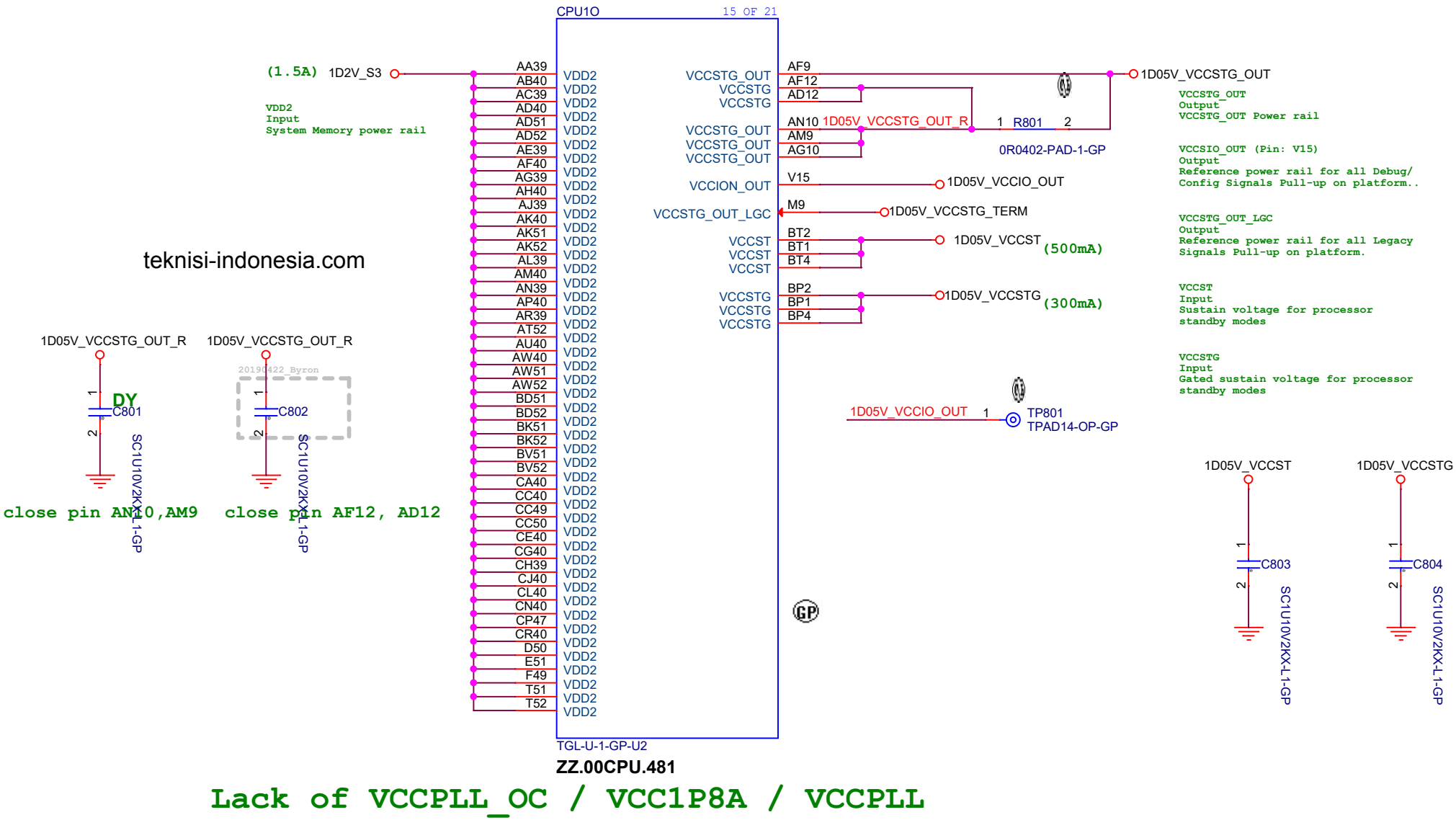
Title: **CPU (VCCIN/VID)**

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 7 of 106



C560

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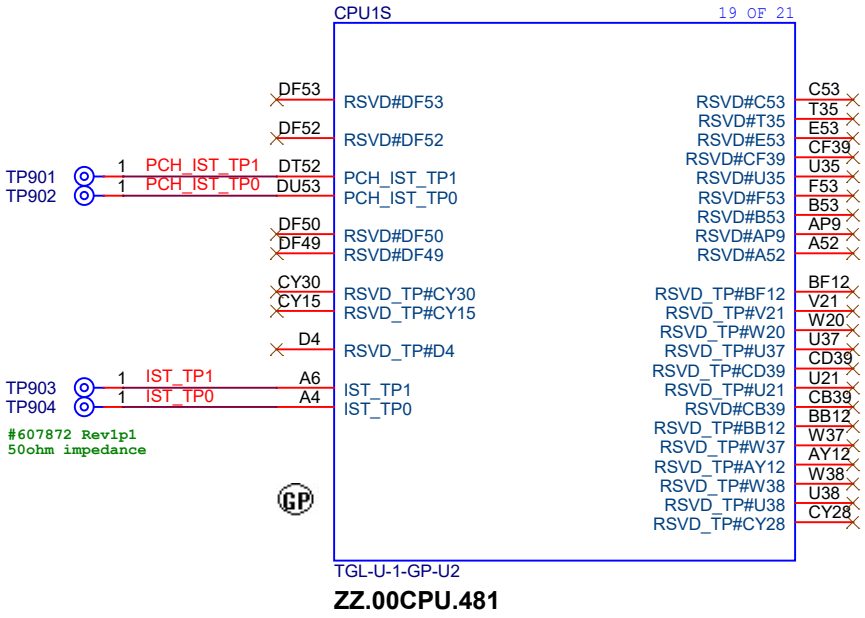
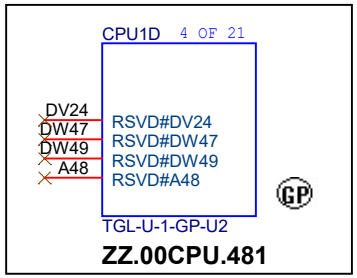
Title	**CPU (VDDQ/VCC/VCCST)**	
Size A4	Document Number **C560-TGL**	Rev -1
Date: Saturday, August 15, 2020	Sheet 8 of 106	



#607872 Rev1p1
Impedance Spectrum Tool (IST/IFDIM) Testing
Requirements and Recommendations

NOTE
IST/IFDIM is not directly available to customers, Intel will need these trigger points to support debug of customer issues at Intel validation labs. Intel recommends customers implement the IST tool requirements from this section.



C560

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Title: CPU (RSVD)		
Size: A4	Document Number: C560-TGL	Rev: -1
Date: Saturday, August 15, 2020	Sheet 9 of 106	

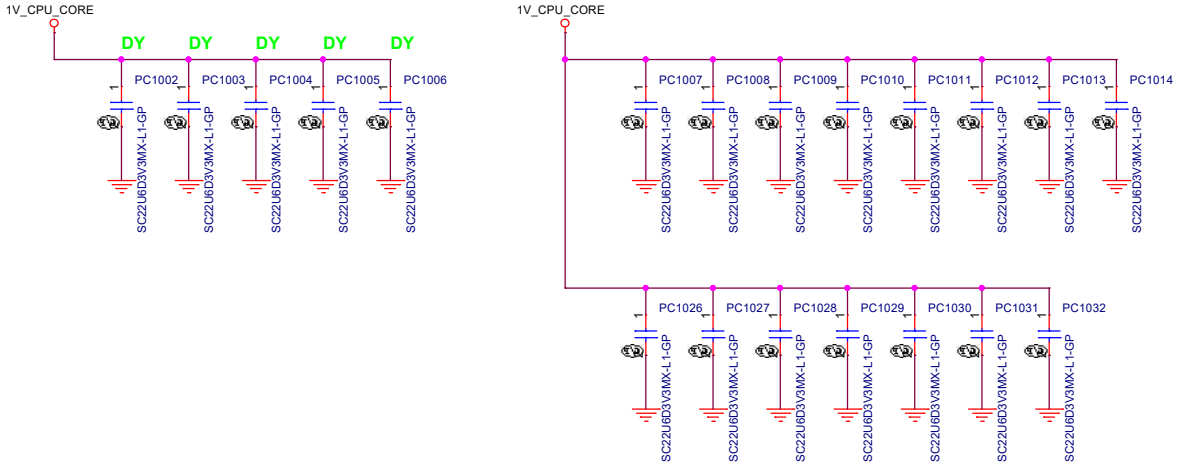
Main Func = CPU

ICL_U42

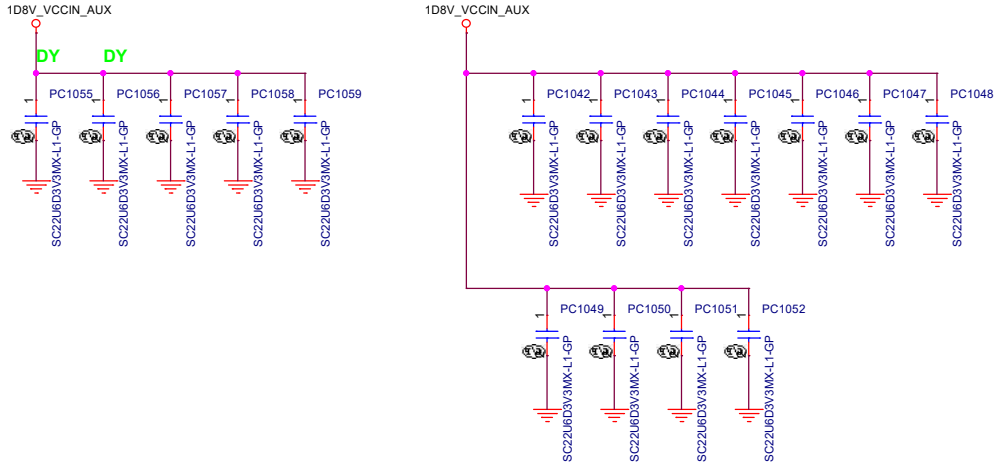
U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	15	220uF*2

VCORE



1D8V_VCCIN_AUX



C560

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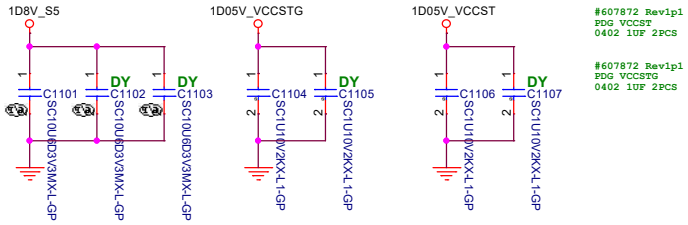
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER CAP1)

Size: A3 | Document Number: C560-TGL | Rev: -1

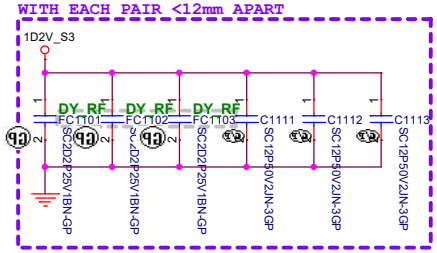
Date: Saturday, August 15, 2020 | Sheet 10 of 106



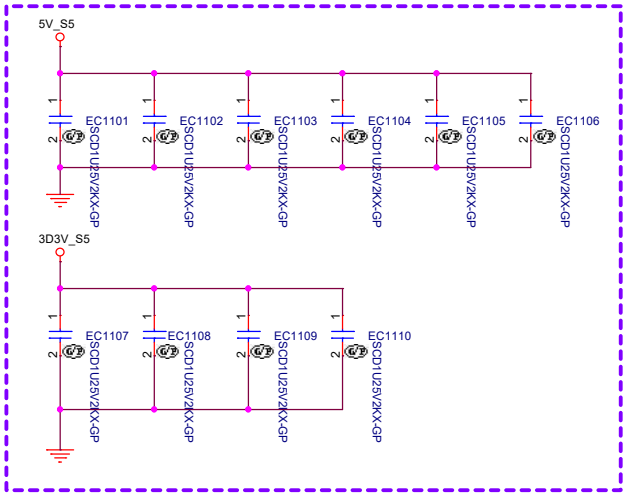
#607872 Rev1p1
PDG VCCST
0402 1UF 2PCS

#607872 Rev1p1
PDG VCCSTG
0402 1UF 2PCS

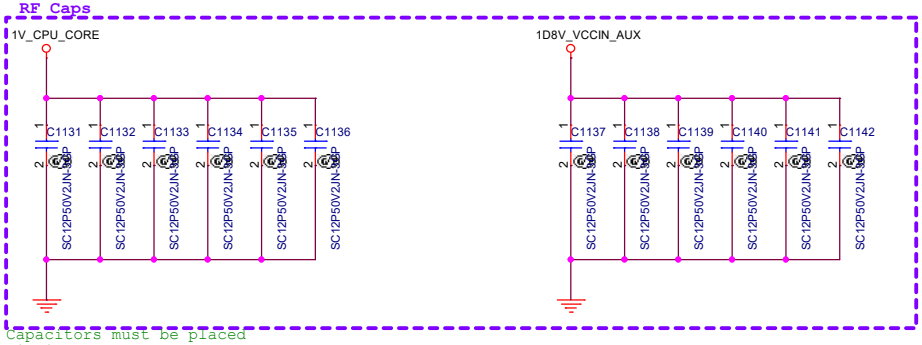
EMC CAPS - PLACE <4mm FROM SOC VDDQ,
WITH EACH PAIR <12mm APART



C560 EVT EMC add Caps



RF Caps



Capacitors must be placed
within 5 mm from SOC
and distributed in the power planes

C560

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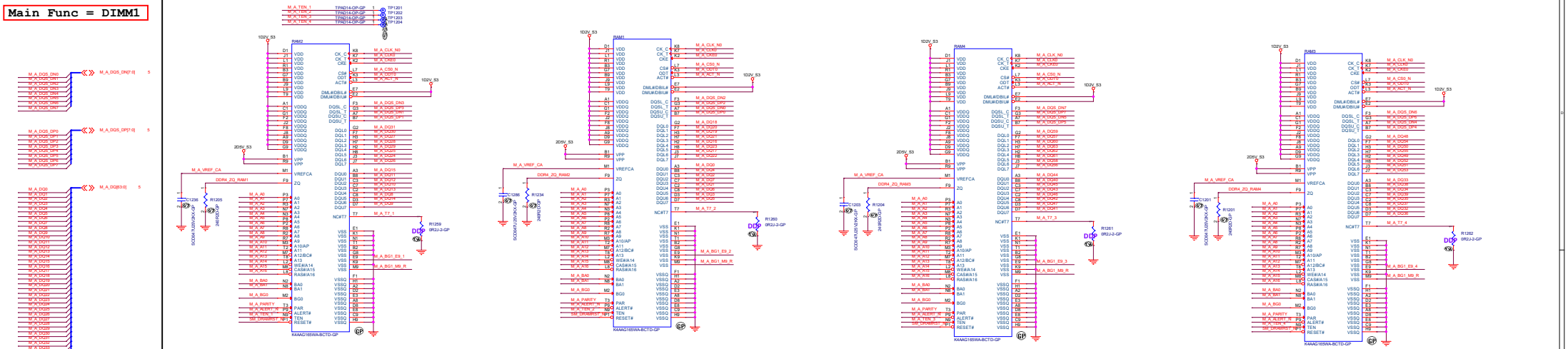
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (Power Cap2)	
Size A3	Document Number C560-TGL	Rev -1
Date: Saturday, August 15, 2020	Sheet 11 of 106	

(Off-Page)

Main Func = DIMM1

Layout Note:Place as pic..



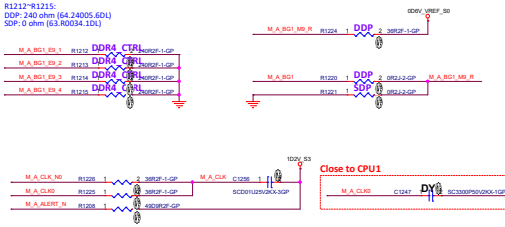
SDP and DDP BOM Control Table

		SDPx16 8Gb	SDPx16 16Gb	SDPx16 8Gb	SDPx16 8Gb	SDPx16 16Gb	DDPx16 16Gb
		SM30N76632	SM30N76633	SM30N76639	SM30N76570	SM30N76641	SM30N76640
		Samsung K4ABG165WC-BCWE	Samsung K4AAG165WA-BCWE	SK Hynix H5AN8G6NCJR-VKC	Micron MT40A512M16TB-062E	Micron MT40A1G16KD-062E:E	SK Hynix H5ANAG6NCJR-XNC
DDR4_CTRL	R1212	0R	0R	0R	0R	0R	240R 1%
	R1213	0R	0R	0R	0R	0R	240R 1%
	R1214	0R	0R	0R	0R	0R	240R 1%
	R1215	0R	0R	0R	0R	0R	240R 1%
SDP	R1221	ASM	ASM	ASM	ASM	ASM	DY
DDP	R1220	DY	DY	DY	DY	DY	ASM
	R1224	DY	DY	DY	DY	DY	ASM

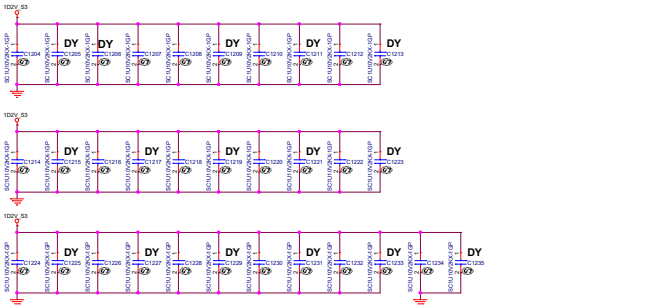
BOM control

SDP & DDP SETTING

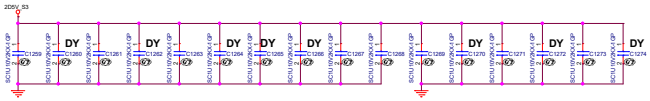
R1212~R1215:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.80034.1DL)



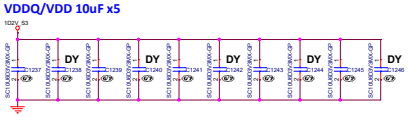
VDDQ/VDD 1uF x16



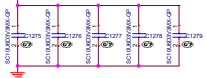
VPP 1uF x8



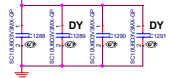
VDDQ/VDD 10uF x5



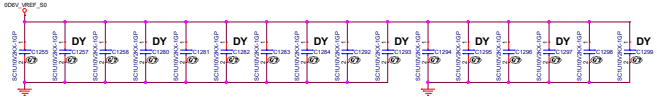
VPP 10uF x2

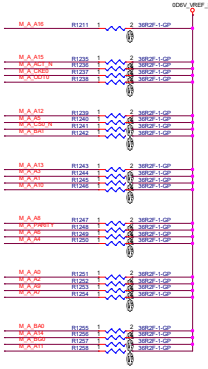


VTT 10uF x2



VTT 1uF x8





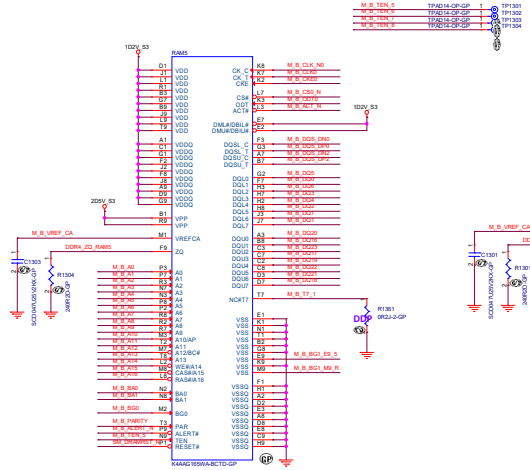
C560

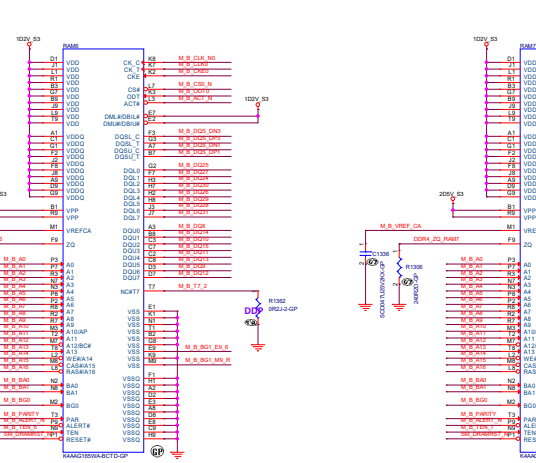
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

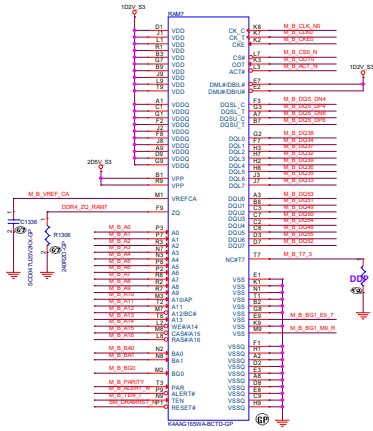
Title:	DDR (DDR4-CHA)	
Size: A1	Document Number: C560-TGL	Rev: -1
Date: Saturday, August 15, 2020	Sheet 12 of 106	

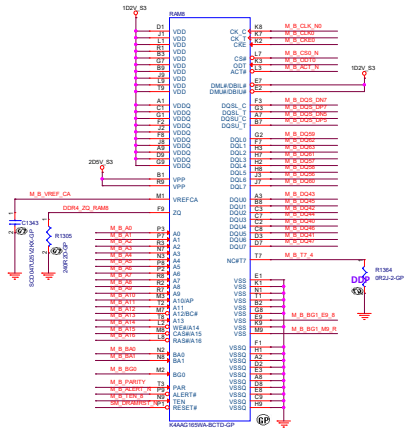
(Off-Page)

Main Func = DIMM2



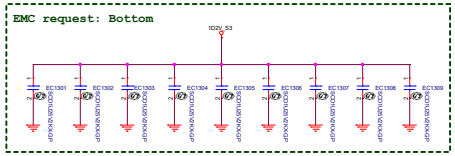


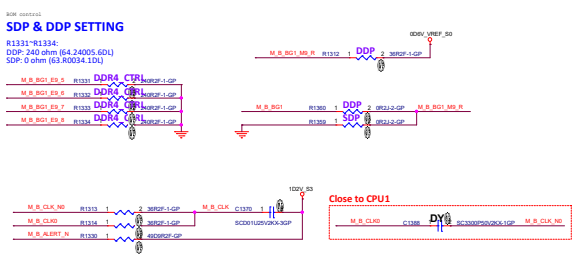


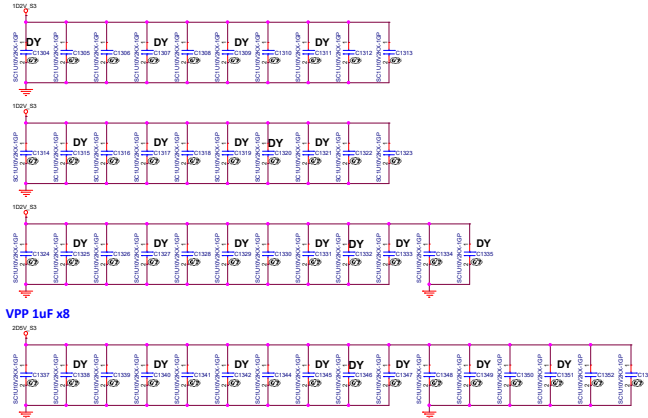


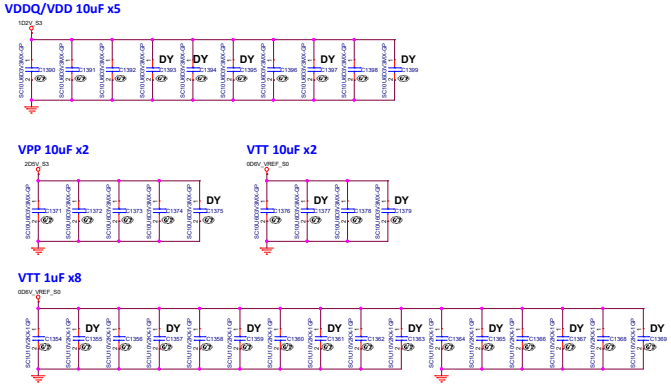
SDP and DDP BOM Control Table

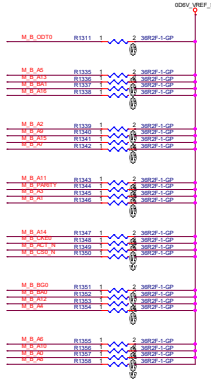
		SDPx16 8Gb	SDPx16 16Gb	SDPx16 8Gb	SDPx16 8Gb	SDPx16 16Gb	DDPx16 16Gb
		SM30N76632	SM30N76633	SM30N76639	SM30N76570	SM30N76641	SM30N76640
		Samsung K4A8G165WC-BCWE	Samsung K4AAG165WA-BCWE	SK Hynix H5ANBG6NCJR-VKC	Micron MT40A512M16TB-062E	Micron MT40A1G16KD-062E:E	SK Hynix H5ANAG6NCJR-XNC
DDR4_CTRL	R1331 R1332 R1333 R1334	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%
SDP	R1359	ASM	ASM	ASM	ASM	ASM	DY
DDP	R1312 R1360	DY DY	DY DY	DY DY	DY DY	DY DY	ASM ASM











BLANK

C560

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***DDR (RSVD)***		
Size: A4	Document Number: **C560-TGL**	Rev: **-1**
Date: Saturday, August 15, 2020	Sheet 14 of 106	

24	ME_FWP
21,61	CNV_RGI_DT
18	GPP_C5_SML0ALERT_N
18	GPP_E6_JTAG_ODT
19	HDA_SDOUT_CPU
4	TBT_LSX1_RXD
4	TBT_LSX2_RXD
3	DBG_PMODE
4	TBT_LSX3_VCC_CONFIG
4	TBT_LSX1_VCC_CONFIG
18	GPP_E10
18	GPP_E11

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
		Move to Page 25			Move to Page 25		
GPIO	**TBT LSX VCCIO conf.#0**	**TBT LSX VCCIO conf.#1**	**TBT LSX VCCIO conf.#2**	**TBT LSX VCCIO conf.#3**	**A0**		**GPP_E10** / **GPP_E11**
Schematic	E19	E21		D12	Move to Page 25		1D8V_S5 — R1518 20KR2J-L3-GP — GPP_E10; 1D8V_S5 — R1519 20KR2J-L3-GP — GPP_E11

Why GPP_E10, GPP_E11 need PU?

GPP_C5

GPP_C5 / SML0ALERT#	Boot Strap 0	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration. This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively). 4-bit boot strap configuration encodings: 0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled. 0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled 0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI 1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device). 1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI. Others: Reserved Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1501 4K7R2J-L-GP — GPP_C5_SML0ALERT_N — DY R1502 20KR2J-L3-GP

GPP_E6

GPP_E6	JTAG ODT Disable	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. External pull-up is recommended 0=> JTAG ODT is disabled 1=> JTAG ODT is enabled

1D8V_S5 — R1503 100KR2J-1-GP — GPP_E6_JTAG_ODT — DY R1509 4K7R2J-L-GP

GPP_D10

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / GSPI2_CLK	DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8V 1 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1520 4K7R2J-L-GP — TBT_LSX2_RXD — R1512 20KR2J-L3-GP

GPP_E19

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD	DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V 1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1513 4K7R2J-L-GP — TBT_LSX1_RXD

GPP_D12

GPP_D12 / ISH_SPI_MOSI / DDP4_CTRLDATA / CAS_SPIM_MOSI / TBT_LSX3_RXD	DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 1.8V 1 = DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1515 4K7R2J-L-GP — TBT_LSX3_VCC_CONFIG — R1516 20KR2J-L3-GP

GPP_E21

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD	DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8V 1 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1514 4K7R2J-L-GP — TBT_LSX1_VCC_CONFIG — R1522 20KR2J-L3-GP

GPP_R2

GPP_R2 / HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This strap has a 20 kohm ± 30% internal pull-down. 0=> Enable security measures defined in the Flash Descriptor. (Default) 1=> Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

ME_FWP — R1511 1KR2J-1-GP — HDA_SDOUT_CPU
EC control.

DBG_PMODE

DBG_PMODE	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-up. This strap should sample high. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

1D05V_S5_OUT — XDP R1517 1KR2J-1-GP — DBG_PMODE

GPP_F2

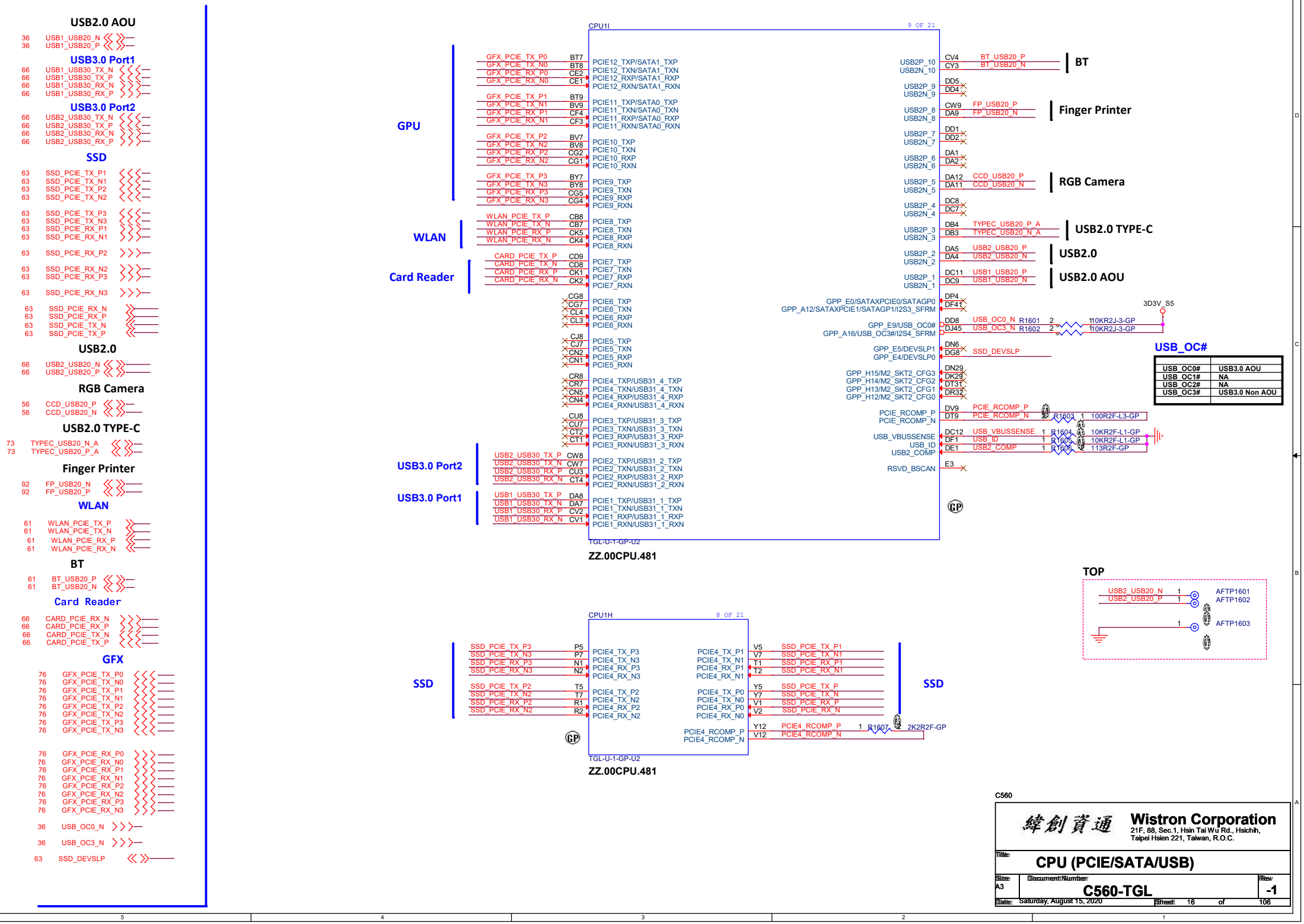
GPP_F2 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled. Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

1D8V_S5 — R1505 100KR2J-1-GP — CNV_RGI_DT — DY R1521 4K7R2J-L-GP

C560

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)
Size: A2 | Document Number: C560-TGL | Rev: -1
Date: Saturday, August 15, 2020 | Sheet 15 of 106


USB2.0 AOU
USB1_USB20_N
USB1_USB20_P
USB3.0 Port1
USB1_USB30_TX_N
USB1_USB30_TX_P
USB1_USB30_RX_N
USB1_USB30_RX_P
USB3.0 Port2
USB2_USB30_TX_N
USB2_USB30_TX_P
USB2_USB30_RX_N
USB2_USB30_RX_P
SSD
SSD_PCIE_TX_P1
SSD_PCIE_TX_N1
SSD_PCIE_TX_P2
SSD_PCIE_TX_N2
SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_RX_N
SSD_PCIE_RX_P
SSD_PCIE_TX_N
SSD_PCIE_TX_P
USB2.0
USB2_USB20_N
USB2_USB20_P
RGB Camera
CCD_USB20_P
CCD_USB20_N
USB2.0 TYPE-C
TYPEC_USB20_N_A
TYPEC_USB20_P_A
Finger Printer
FP_USB20_N
FP_USB20_P
WLAN
WLAN_PCIE_TX_P
WLAN_PCIE_TX_N
WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
BT
BT_USB20_P
BT_USB20_N
Card Reader
CARD_PCIE_RX_N
CARD_PCIE_RX_P
CARD_PCIE_TX_N
CARD_PCIE_TX_P
GFX
GFX_PCIE_TX_P0
GFX_PCIE_TX_N0
GFX_PCIE_TX_P1
GFX_PCIE_TX_N1
GFX_PCIE_TX_P2
GFX_PCIE_TX_N2
GFX_PCIE_TX_P3
GFX_PCIE_TX_N3
GFX_PCIE_RX_P0
GFX_PCIE_RX_N0
GFX_PCIE_RX_P1
GFX_PCIE_RX_N1
GFX_PCIE_RX_P2
GFX_PCIE_RX_N2
GFX_PCIE_RX_P3
GFX_PCIE_RX_N3
USB_OC0_N
USB_OC3_N
SSD_DEVSLP
CPU1I
9 OF 21
GPU
WLAN
Card Reader
USB3.0 Port2
USB3.0 Port1
PCIE12_TXP/SATA1_TXP
PCIE12_TXN/SATA1_TXN
PCIE12_RXP/SATA1_RXP
PCIE12_RXN/SATA1_RXN
PCIE11_TXP/SATA0_TXP
PCIE11_TXN/SATA0_TXN
PCIE11_RXP/SATA0_RXP
PCIE11_RXN/SATA0_RXN
PCIE10_TXP
PCIE10_TXN
PCIE10_RXP
PCIE10_RXN
PCIE9_TXP
PCIE9_TXN
PCIE9_RXP
PCIE9_RXN
PCIE8_TXP
PCIE8_TXN
PCIE8_RXP
PCIE8_RXN
PCIE7_TXP
PCIE7_TXN
PCIE7_RXP
PCIE7_RXN
PCIE6_TXP
PCIE6_TXN
PCIE6_RXP
PCIE6_RXN
PCIE5_TXP
PCIE5_TXN
PCIE5_RXP
PCIE5_RXN
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PCIE1_RXN/USB31_1_RXN
TGL-U-1-GP-U2
ZZ.00CPU.481
USB2P_10
USB2N_10
USB2P_9
USB2N_9
USB2P_8
USB2N_8
USB2P_7
USB2N_7
USB2P_6
USB2N_6
USB2P_5
USB2N_5
USB2P_4
USB2N_4
USB2P_3
USB2N_3
USB2P_2
USB2N_2
USB2P_1
USB2N_1
BT
Finger Printer
RGB Camera
USB2.0 TYPE-C
USB2.0
USB2.0 AOU
GPP_E0/SATAXPCIE0/SATAGP0
GPP_A12/SATAXPCIE1/SATAGP1/I2S3_SFRM
GPP_E9/USB_OC0#
GPP_A16/USB_OC3#/I2S4_SFRM
GPP_E5/DEVSLP1
GPP_E4/DEVSLP0
GPP_H15/M2_SKT2_CFG3
GPP_H14/M2_SKT2_CFG2
GPP_H13/M2_SKT2_CFG1
GPP_H12/M2_SKT2_CFG0
PCIE_RCOMP_P
PCIE_RCOMP_N
USB_VBUSSENSE
USB_ID
USB2_COMP
RSVD_BSCAN
3D3V_S5
R1601 110KR2J-3-GP
R1602 110KR2J-3-GP
SSD_DEVSLP
USB_OC#
USB_OC0# USB3.0 AOU
USB_OC1# NA
USB_OC2# NA
USB_OC3# USB3.0 Non AOU
R1603 100R2F-L3-GP
R1604 10KR2F-L1-GP
R1605 10KR2F-L1-GP
R1606 113R2F-GP
CPU1H
8 OF 21
SSD
SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_TX_P2
SSD_PCIE_TX_N2
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_TX_P1
SSD_PCIE_TX_N1
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1
SSD_PCIE_TX_P
SSD_PCIE_TX_N
SSD_PCIE_RX_P
SSD_PCIE_RX_N
PCIE4_RCOMP_P
PCIE4_RCOMP_N
R1607 2K2R2F-GP
TOP
AFTP1601
AFTP1602
AFTP1603
C560
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCIE/SATA/USB)
Size A3
Document Number
C560-TGL
Rev -1
Date: Saturday, August 15, 2020
Sheet 16 of 106

26,61,63,66,76 PLT_RST_N
24,40 PM_SLP_SUS_N
24,40 PM_SLP_S3_N
24,51 PM_SLP_S4_N
24 PM_PWRBTN_N
24,40 ALL_SYS_PWRGD
99 SYS_RESET_N
50 VCCAUX_PWRGD
24 RSMRST_N_KBC
24 DSW_PWROK
40 PCH_PWROK
24 SYS_PWROK
55 PM_SLP_S0_N
24 AC_PRESENT
40 VCCST_OVERRIDE
40 CPU_C10_GATE_N
72 CPU_SMB_ALERT_PCH_N
61 PCIE_WAKE_N

CPU1L 12 OF 21

PM_SLP_SUS_N DV49 SLP_SUS#
PM_SLP_S4_N DM43 GPD10/SLP_S5#
PM_SLP_S3_N DJ41 GPD5/SLP_S4#
DJ43 GPD4/SLP_S3#
DR41 GPD6/SLP_A#
DT44 GPD9/SPL_WLAN#
PM_SLP_S0_N DD42 GPP_B12/SLP_S0#
DN39 SLP_LAN#
PM_RSMRST_N DM35 RSMRST#
SYS_RESET_N DD10 SYS_RESET#
PLT_RST_N DD41 GPP_B13/PLTRST#
DSW_PWROK_R DK35 DSW_PWROK
SYS_PWROK 1 R1701 2 SYS_PWROK_R DF10 SYS_PWROK
PCH_PWROK 1 R1704 2 PCH_PWROK_R DN35 PCH_PWROK
0R0402-PAD-1-GP
RTC_INTRUDER_N DM37 INTRUDER#
SPI_VCC_SEL DT49 SPIVCCIOSEL
strap
TGL-U-1-GP-U2

PROCPWRGD BM9 TP_VCORE_PWRGD 1 TP1701
GPD3/PWRBTN# DK41 PM_PWRBTN_N
GPD0/BATLOW# DN41 PM_BATLOW_N
GPD1/ACPRESENT DK43 AC_PRESENT
GPP_B11/PMCALERT# CW40 CPU_SMB_ALERT_PCH_N 1 R1732 DY 2 75KR2J-GP
GPP_H18/CPU_C10_GATE# DN27 CPU_C10_GATE_N
GPP_H3/SX_EXIT_HOLDOFF# DG31
WAKE# DK39 PCIE_WAKE_N
GPD2/LAN_WAKE# DM41
GPD11/LANPHYPC/DSWLDO_MON DT41 TP_GPG11 1 TP1702
strap GPD7 DN43
VCCSTPWRGOOD_TCSS CE5 VCCSTPWRGOOD_TCSS 1 R1703 VCCST_OVERRIDE
VCCST_PWRGD BP8 VCCST_PWRGD_R 0R0402-PAD-1-GP
VCCST_OVERRIDE BP9 VCCST_OVERRIDE_R 1 R1705 2 VCCST_OVERRIDE
0R0402-PAD-1-GP
GPP_F20/EXT_PWR_GATE# DR12
GPP_F21/EXT_PWR_GATE2# DW12

VCCST_OVERRIDE
VccST Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability.

ZZ.00CPU.481

3D3V_S0
1 R1706 2 SYS_RESET_N 10KR2J-3-GP

3D3V_S5
1 R1708 2 AC_PRESENT 100KR2J-1-GP
1 R1709 2 PCIE_WAKE_N 1KR2J-1-GP
1 R1710 2 PM_BATLOW_N 10KR2J-3-GP
2 R1715 1 VCCST_OVERRIDE 100KR2J-1-GP
2 R1717 1 PCH_PWROK_R 100KR2J-1-GP
2 R1720 1 SYS_PWROK_R 100KR2J-1-GP
R1713
2 DY 1 PM_SLP_S0_N 100KR2J-4-GP

Volatge Level 1V

3D3V_S5
1D05V_VCCST
U1701
1 NC#1 VCC 5
ALL_SYS_PWRGD 2 A
3 GND Y 4 VCCST_PWRGD
74LVC1G07GW-GP
C1702 SCD1U16V2KX-L-GP
R1726 1KR2F-3-GP
R1727 60D4R2F-GP VCCST_PWRGD_R
73.01G07.0HG

SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V

SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V

3D3V_RTC_AUX
DY
R1707 1MR2F-GP
RTC_INTRUDER_N
C1701 SCD1U16V2KX-L-GP
R1711 1MR2F-GP
SPI_VCC_SEL
R1712 4K7R2J-L-GP

From EC Control
DSW_PWROK_R 1 R1723 2 DSW_PWROK
0R0402-PAD-1-GP
R1724 100KR2J-1-GP
Delay 3D3V_S5 over 10ms.

Q1701
LSK3541G1ET2L-1-GP
084.03541.M001
S D PM_RSMRST_N 1 R1721 1KR2J-1-GP RSMRST_N_KBC
G
R1725 100KR2J-1-GP
3D3V_S5
R1718 100KR2J-1-GP
3D3V_S5
3V_5V_POK_C
1 R1722 2 VCCAUX_PWRGD
0R0402-PAD-1-GP
G
2 R1719 10KR2J-3-GP 1 3V_5V_POK_N D S
Q1702
LSK3541G1ET2L-1-GP
084.03541.M001

GPD7

GPD7	Reserved	Rising edge of DSW_PWROK	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after DSW_PWROK is high. 2. This signal is in the DSW well.

C560

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: B
Document Number: C560-TGL
Rev: -1
Date: Saturday, August 15, 2020
Sheet 17 of 106

SPI ROM

25 SPI_WP_CPU
25 SPI_HOLD_CPU
25 SPI_CLK_CPU
25 SPI_CS_CPU_N0
25 SPI_CS_CPU_N1
25 SPI_SI_CPU
25 SPI_SO_CPU

WLAN

61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N

CARD

66 CARD_CLK_CPU_P
66 CARD_CLK_CPU_N
66 CARD_CLKREQ_CPU_N

SSD

63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 SSD_CLKREQ_CPU_N

ESPI

24,68 ESPI_CPU_IO0
24,68 ESPI_CPU_IO1
24,68 ESPI_CPU_IO2
24,68 ESPI_CPU_IO3
24,68 ESPI_CPU_CS_N
24,68 ESPI_CPU_RST_N
24,68 ESPI_CPU_CLK

OTHER

15 GPP_C5_SML0ALERT_N
61 SUS_CLK
79,88 GC6_FB_EN_PCH
24,25 RTCRST_ON
15 GPP_E6_JTAG_OD
76 DGPU_HOLD_RST_N
72 CPU_SMB_SCL_P
72 CPU_SMB_SDA_P
15 GPP_E10
15 GPP_E11

GFX

76 PEG_CLK_CPU_P
76 PEG_CLK_CPU_N
76 PEG_CLKREQ_CPU_N

CPU1E — 5 OF 21

SPI_CLK_CPU DJ37 — SPI0_CLK — strap
SPI_HOLD_CPU DG35 — SPI0_IO3 — strap
SPI_WP_CPU DJ39 — SPI0_IO2 — strap
SPI_SO_CPU DJ33 — SPI0_MISO
SPI_SI_CPU DJ35 — SPI0_MOSI
SPI_CS_CPU_N1 DF35 — SPI0_CS1#
SPI_CS_CPU_N0 DG37 — SPI0_CS0#
DF39 — SPI0_CS2#

GPP_E11 DJ6 — GPP_E11/SPI1_CLK/THC0_SPI1_CLK
DN5 — GPP_E2/SPI1_IO3/THC0_SPI1_IO3
DN9 — GPP_E1/SPI1_IO2/THC0_SPI1_IO2
DM6 — GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
DK6 — GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
DK8 — GPP_E10/SPI1_CS#/THC0_SPI1_CS#
DV11 — GPP_E8/SPI1_CS1#/SATA_LED#
DW9 — GPP_E17/THC0_SPI1_INT#
DT8 — GPP_E6/THC0_SPI1_RST#

Why GPP_E10, GPP_E11 need PU?

1 R1835 2 10KR2J-GP — DGPU_HOLD_RST_N — GPP_E6_JTAG_OD1

GC6_FB_EN_PCH — DN15 — GPP_F11/THC1_SPI2_CLK
SDRAM_ID3 DK13 — GPP_F15/GSXSRESET#/THC1_SPI2_IO3
SDRAM_ID2 DM13 — GPP_F14/GSXDIN/THC1_SPI2_IO2
SDRAM_ID1 DN13 — GPP_F13/GSXSLOAD/THC1_SPI2_IO1
SDRAM_ID0 DJ15 — GPP_F12/GSXDOUT/THC1_SPI2_IO0
SDRAM_ID4 DK15 — GPP_F16/GSXCLK/THC1_SPI2_CS#
DN10 — GPP_F18/THC1_SPI2_INT#
DV11 — GPP_F17/THC1_SPI2_RST#
DH3 — CL_CLK
DH4 — CL_DATA
DF2 — CL_RST#

GPP_C0/SMBCLK — DK21 — CPU_SMB_SCL
GPP_C1/SMBDATA — DM19 — CPU_SMB_SDA
GPP_C2/SMBALERT# — DN19 — CPU_SMB_ALERT_N
GPP_C3/SML0CLK — DK19
GPP_C4/SML0DATA — DM17
GPP_C5/SML0ALERT# — DN17 — GPP_C5_SML0ALERT_N
GPP_C6/SML1CLK — DK17 — CPU_SMB_SCL_P1
GPP_C7/SML1DATA — DJ17 — CPU_SMB_SDA_P1
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# — CY50 — GPP_B23_CLK_FREQ — 1 TP1801 — To PD

GPP_A5/ESPI_CLK — DN53 — ESPI_CPU_CLK_R
GPP_A3/ESPI_IO3/SUSACK# — DJ53 — ESPI_CPU_IO3_R
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK — DH50 — ESPI_CPU_IO2_R
GPP_A1/ESPI_IO1 — DP50 — ESPI_CPU_IO1_R
GPP_A0/ESPI_IO0 — DP52 — ESPI_CPU_IO0_R
GPP_A4/ESPI_CS# — DK52 — ESPI_CPU_CS_N_R
GPP_A6/ESPI_RESET# — DL50 — ESPI_CPU_RST_N_R — 2 R1805 1 75KR2J-GP

TGL-U-1-GP-U2
ZZ.00CPU.481

CPU1K — 11 OF 21

BW1 — CLKOUT_PCIE_P6
BW2 — CLKOUT_PCIE_N6
CB2 — CLKOUT_PCIE_P5
CB1 — CLKOUT_PCIE_N5
BW4 — CLKOUT_PCIE_P4
BW5 — CLKOUT_PCIE_N4
CL7 — CLKOUT_PCIE_P3
CL8 — CLKOUT_PCIE_N3
CB4 — CLKOUT_PCIE_P2
CB5 — CLKOUT_PCIE_N2
BY4 — CLKOUT_PCIE_P1
BY5 — CLKOUT_PCIE_N1
CN7 — CLKOUT_PCIE_P0
CN8 — CLKOUT_PCIE_N0

PEG_CLK_CPU_P
PEG_CLK_CPU_N
CARD_CLK_CPU_P
CARD_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
SSD_CLK_CPU_P
SSD_CLK_CPU_N

DJ5 — XCLK_BIASREF — 2 R1812 1 60D4R2F-GP

GPP_F19/SRCCLKREQ6# — DU14
GPP_H11/SRCCLKREQ5# — DF21 — PEG_CLKREQ_CPU_N
GPP_H10/SRCCLKREQ4# — DD25 — CARD_CLKREQ_CPU_N
GPP_D8/SRCCLKREQ3# — DT24 — WLAN_CLKREQ_CPU_N
GPP_D7/SRCCLKREQ2# — DT30
GPP_D6/SRCCLKREQ1# — DV30 — SSD_CLKREQ_CPU_N
GPP_D5/SRCCLKREQ0# — DW30

DM1 — XTL_38D4M_X2_CPU — R18181 — 33R1J-GP — XTL_38D4M_X2_CPU_R
DL1 — XTL_38D4M_X1_CPU — R18191 — 33R1J-GP — XTL_38D4M_X1_CPU_R
XTAL_OUT
XTAL_IN
DW41 — SUS_CLK
GPD8/SUSCLK

DT47 — XTL_32K_X2_CPU — R18201 — 0R0201-PAD-GP — XTL_32K_X2_CPU_R
DR47 — XTL_32K_X1_CPU — R18211 — 0R0201-PAD-GP — XTL_32K_X1_CPU_R
RTCX2
RTCX1

DN7 — RTC_RST_N
DK57 — SRTC_RST_N
RTCRST#
SRTCRST#

TGL-U-1-GP-U2
ZZ.00CPU.481

1D8V_S5

MEM_ID0_1 R1823 10KR2J-3-GP — SDRAM_ID0
MEM_ID1_1 R1825 10KR2J-3-GP — SDRAM_ID1
MEM_ID2_1 R1827 10KR2J-3-GP — SDRAM_ID2
MEM_ID3_1 R1829 10KR2J-3-GP — SDRAM_ID3
MEM_ID4_1 R1831 10KR2J-3-GP — SDRAM_ID4

MEM_ID0_0 R1824 10KR2J-3-GP
MEM_ID1_0 R1826 10KR2J-3-GP
MEM_ID2_0 R1828 10KR2J-3-GP
MEM_ID3_0 R1830 10KR2J-3-GP
MEM_ID4_0 R1832 10KR2J-3-GP

SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Wisrton PN	Vendor	Density	Chanel		
0	0	0	0	0	SM30N76633	Samsung	8GB+8GB	A+B	SDP	
0	0	0	0	1	SM30N76641	Micron	8GB+8GB	A+B	SDP	
0	0	0	1	0	SM30N76640	SK hynix	8GB+8GB	A+B	DDP	SKU2
0	0	0	1	1						
0	0	1	0	0	SM30N76632	Samsung	4GB+4GB	A+B	SDP	SKU4
0	0	1	0	1	SM30N76570	Micron	4GB+4GB	A+B	SDP	SKU3
0	0	1	1	0	SM30N76639	SK hynix	4GB+4GB	A+B	SDP	SKU5
0	0	1	1	1						
0	1	0	0	0						
0	1	0	0	1						
0	1	0	1	0						
0	1	0	1	1	SM30N76632	Samsung	4GB	A	SDP	
0	1	1	0	0	SM30U97726	HT Micron	4GB	A	SDP	
0	1	1	0	1	SM30N76570	Micron	4GB	A	SDP	
0	1	1	1	0	SM30N76639	SK hynix	4GB	A	SDP	SKU7
0	1	1	1	1	SM30N76640	SK hynix	8GB	A	DDP	

0=L ,1=H

1	0	0	0	0	SM30N76633	Samsung	8GB	A	SDP	SKU1 SKU6
1	0	0	0	1	SM30N76632	Samsung	4GB	B	SDP	
1	0	1	0	1	SM30N76641	Micron	8GB	A	SDP	
1	0	1	1	0	SM30N76570	Micron	4GB	B	SDP	

SVT Stage

ESPI_CPU_CLK_R 1 R1801 49D9R2F-GP ESPI_CPU_CLK
ESPI_CPU_IO0_R 1 R1802 15R2J-GP ESPI_CPU_IO0
ESPI_CPU_IO1_R 1 R1803 15R2J-GP ESPI_CPU_IO1
ESPI_CPU_IO2_R 1 R1804 15R2J-GP ESPI_CPU_IO2
ESPI_CPU_IO3_R 1 R1805 15R2J-GP ESPI_CPU_IO3
ESPI_CPU_CS_N_R 1 R1806 0R0402-PAD-1-GP ESPI_CPU_CS_N
ESPI_CPU_RST_N_R 1 R1807 2 0R0402-PAD-1-GP ESPI_CPU_RST_N

3D3V_S5
RN1801 — CPU_SMB_SCL_P1 — CPU_SMB_SDA_P1 — SRN1KJ-7-GP
DX
R1809 4K7R2J-L-GP — CPU_SMB_ALERT_N

3D3V_S0
RN1802 — CPU_SMB_SCL — CPU_SMB_SDA — SRN1KJ-7-GP

3D3V_S0
R1817 SSD_CLKREQ_CPU_N
R1833 WLAN_CLKREQ_CPU_N
R1822 PEG_CLKREQ_CPU_N
R1834 CARD_CLKREQ_CPU_N
10KR2J-L-GP

Q1801 LSK3541G1ET2L-1-GP 084.03541.M001
SRTC_RST_N — D S G
RTCRST_ON
R1811 100KR2J-1-GP
Q1802 LSK3541G1ET2L-1-GP 084.03541.M001
S D G — RTC_RST_N

3D3V_RTC_AUX
R1815 20KR2J-L3-GP — SRTC_RST_N — C1805 SC1U10V2KX-L1-GP
3D3V_RTC_AUX
R1816 20KR2J-L3-GP — RTC_RST_N — C1806 SC1U10V2KX-L1-GP

X1802	C1802	C1803
EPSON 082.30003.0191	15pF	12pF
SEIKO 082.30003.0301	15pF	12pF
NDK 082.30003.0221	15pF	12pF

XTL_32K — R1813 10MR2J-L-GP — XTL_32K
X1802 XTAL-32.768KHZ-88-GP 082.30003.0191
C1802 SC15P50V2JN-2-LL-GP — C1803 SC12P50V2JN-3GP

X1801 (38.4MHz)	C1801	C1804
HOSONIC 082.30040.0241	10pF	10pF
HARMONY 082.30040.0231	10pF	10pF
TXC 082.30040.0221	10pF	10pF

XTL_38D4M_X1_CPU_R — C1801 SC10P50V2JN-4GP — X1801 XTAL-38D4MHZ-38-GP 082.30040.0241 — R1814 200KR2F-L-3-GP — C1804 SC10P50V2JN-4GP — XTL_38D4M_X2_CPU_R

GPP_B23

GPP_B23 / SMLIALERT# / PCHHOT# / GSPI1_CS1#	CPUNSSC Clock Frequency	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = 38.4 MHz clock (direct from crystal) (default) 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. 1. This signal is in the primary well.

SPI0_MOSI

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling. Follow #607872 SchChk Rev1p1 PU 100K

SPI0_IO2

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.

SPI0_IO3

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.

GPP_C2

GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0=Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1=Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

C560

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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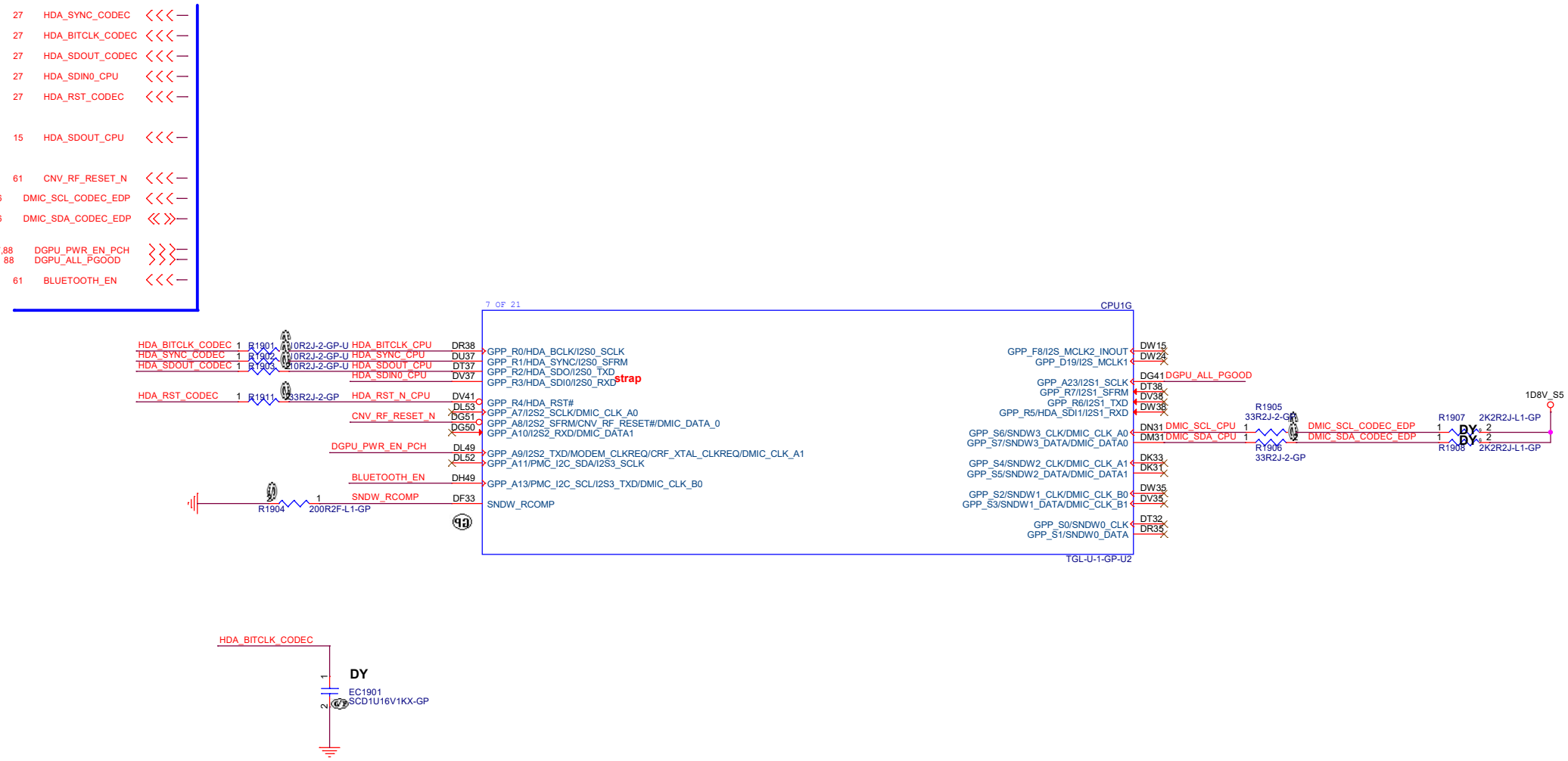
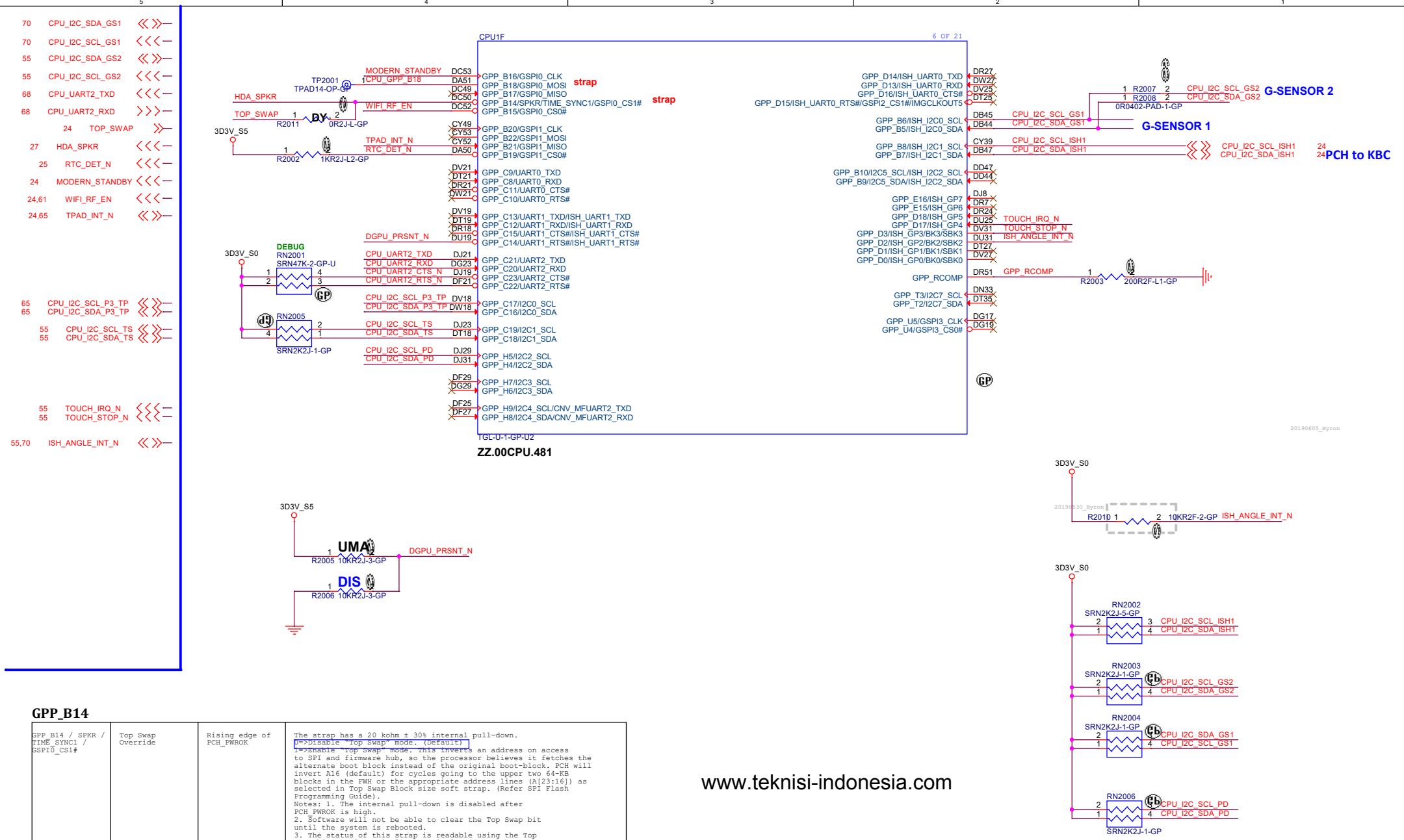
Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: A2 — Document Number: C560-TGL — Rev: -1
Date: Tuesday, August 25, 2020 — Sheet 18 of 106



C560

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CPU (HAD/I2S/SD/DMIC)**		
Size: A3	Document Number: **C560-TGL**	Rev: **-1**
Date: Saturday, August 15, 2020	Sheet 19 of 106	



GPP_B14

GPP_B14 / SPKR / TIME_SYNC1 / GSPI0_CS1#	Top Swap Override	Rising edge of PCH_PWROK	The strap has a 20 kohm ± 30% internal pull-down. 0=>Disable "Top Swap" mode. (Default) 1=>Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap. (Refer SPI Flash Programming Guide). Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B18

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The strap has a 20 kohm ± 30% internal pull-down. 0=>Disable "No Reboot" mode. (Default) 1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

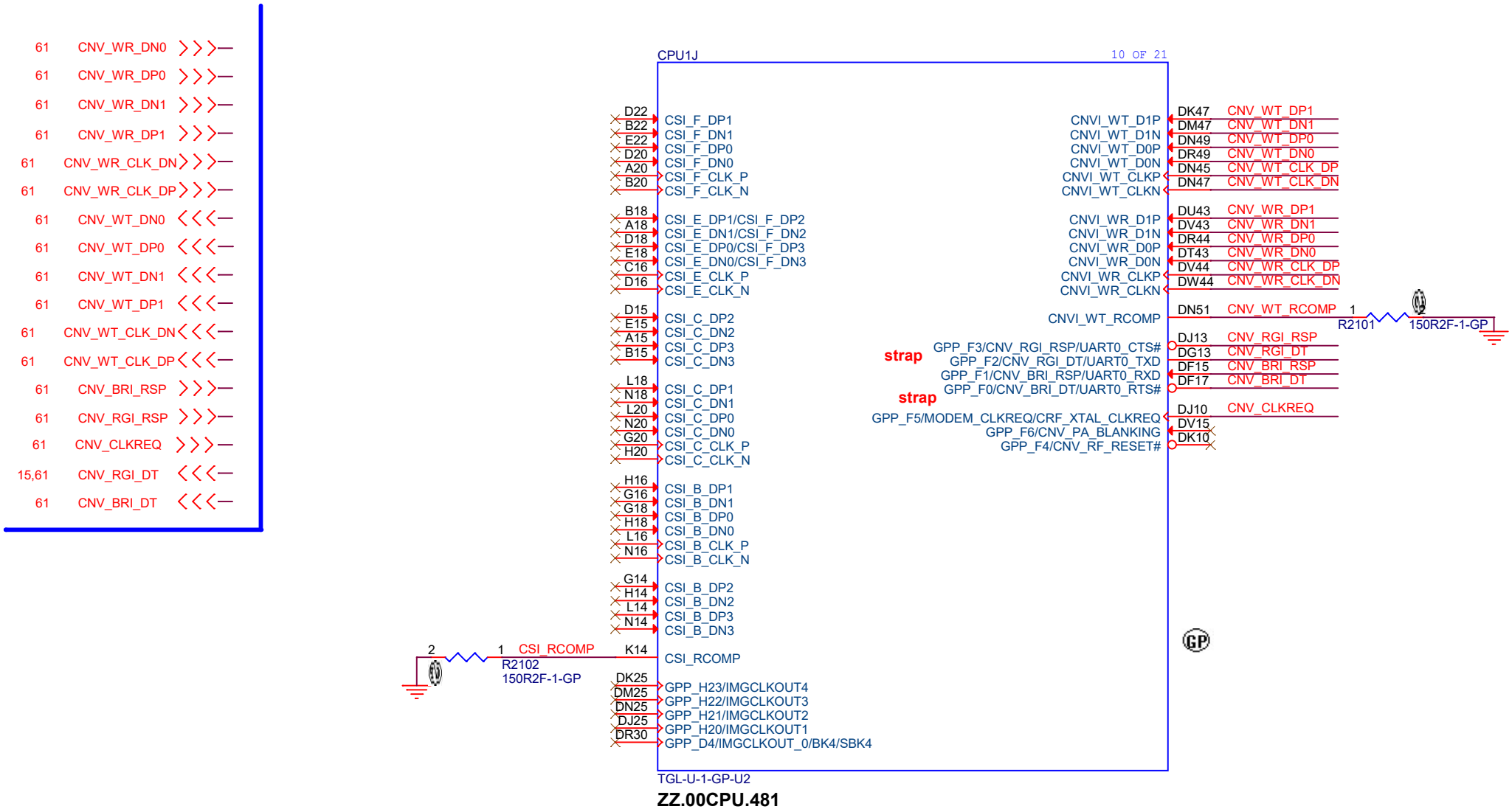
C560

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: A3 | Document Number: C560-TGL | Rev: -1

Date: Saturday, August 15, 2020 | Sheet 20 of 106



GPP_F0

GPP_F0 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Selection	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should not be pulled high since 24 MHz crystal is not supported on the PCH. 0 = 38.4 MHz (default) 1 = 24 MHz Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

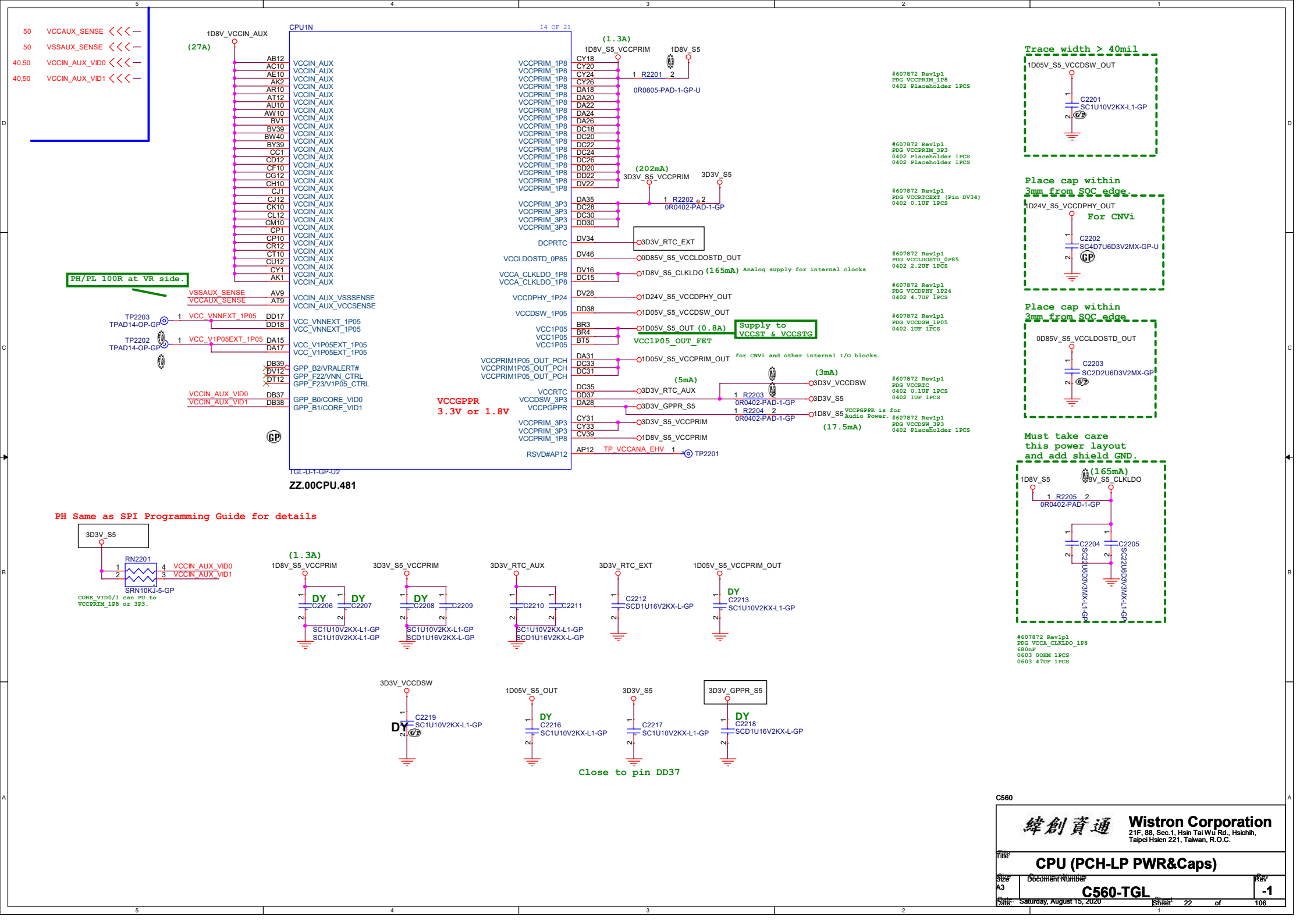
C560

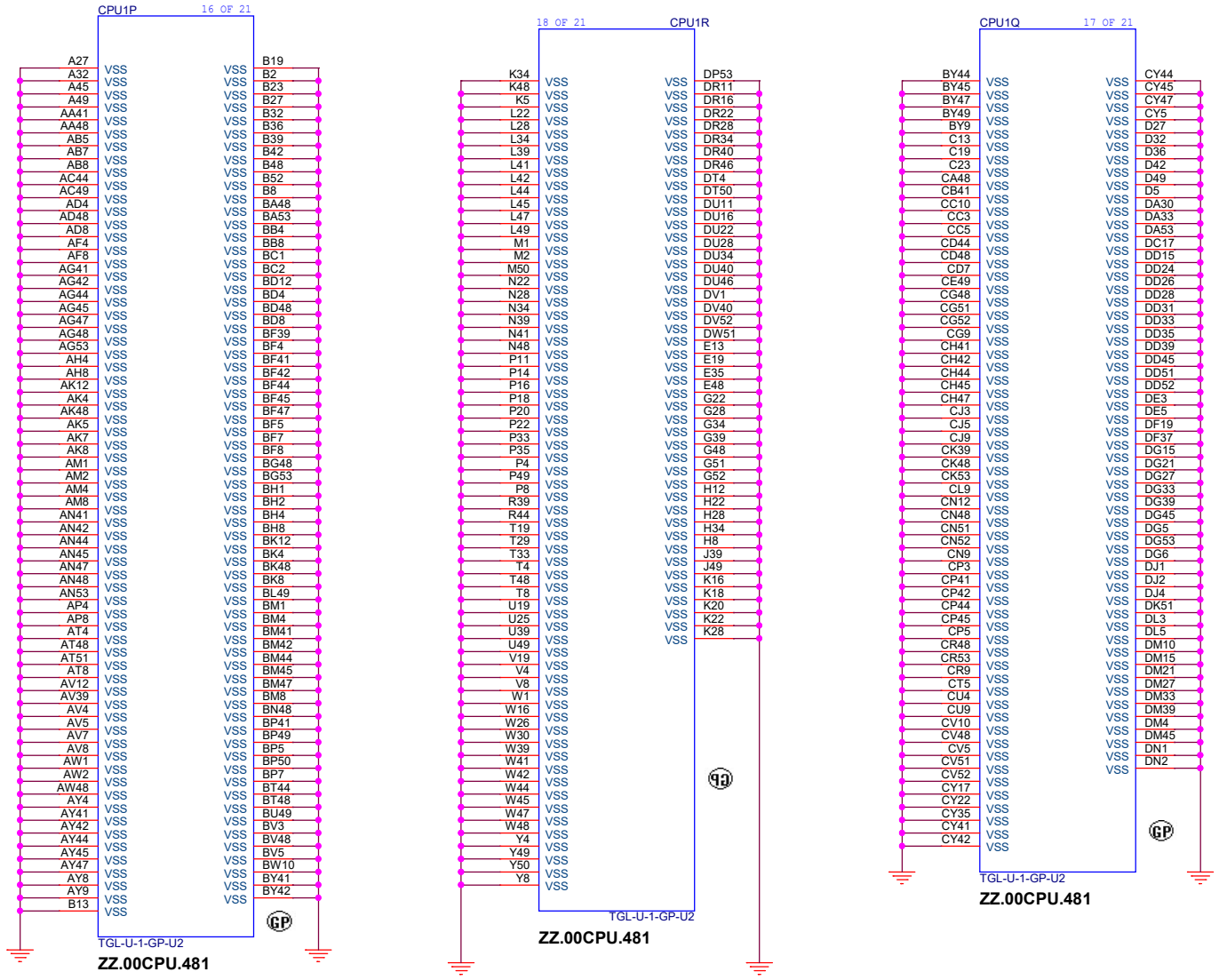
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 21 of 106


50 VCCAUX_SENSE
50 VSSAUX_SENSE
40,50 VCCIN_AUX_VID0
40,50 VCCIN_AUX_VID1
1D8V_VCCIN_AUX
(27A)
CPU1N
14 OF 21
TGL-U-1-GP-U2
ZZ.00CPU.481
PH/PL 100R at VR side.
VSSAUX_SENSE
VCCAUX_SENSE
VCCIN_AUX_VSSSENSE
VCCIN_AUX_VCCSENSE
TP2203
TPAD14-OP-GP
TP2202
TPAD14-OP-GP
VCC_VNNEXT_1P05
VCC_V1P05EXT_1P05
GPP_B2/VRALERT#
GPP_F22/VNN_CTRL
GPP_F23/V1P05_CTRL
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
VCCIN_AUX_VID0
VCCIN_AUX_VID1
VCCGPPR
3.3V or 1.8V
(1.3A)
1D8V_S5_VCCPRIM
1D8V_S5
R2201
0R0805-PAD-1-GP-U
(202mA)
3D3V_S5_VCCPRIM
3D3V_S5
R2202
0R0402-PAD-1-GP
DCPRTC
3D3V_RTC_EXT
0D85V_S5_VCCLDOSTD_OUT
1D8V_S5_CLKLDO (165mA) Analog supply for internal clocks
1D24V_S5_VCCDPHY_OUT
1D05V_S5_VCCDSW_OUT
1D8V_S5_OUT (0.8A)
Supply to VCCST & VCCSTG
VCC1P05_OUT_FET
1D05V_S5_VCCPRIM_OUT
for CNVi and other internal I/O blocks.
(5mA)
3D3V_RTC_AUX
(3mA)
3D3V_VCCDSW
3D3V_S5
R2203
0R0402-PAD-1-GP
3D3V_GPPR_S5
R2204
0R0402-PAD-1-GP
1D8V_S5
VCCPGPPR is for Audio Power.
(17.5mA)
3D3V_S5_VCCPRIM
1D8V_S5_VCCPRIM
TP_VCCANA_EHV
TP2201
RSVD#AP12
#607872 Rev1p1
PDG VCCPRIM_1P8
0402 Placeholder 1PCS
#607872 Rev1p1
PDG VCCPRIM_3P3
0402 Placeholder 1PCS
0402 Placeholder 1PCS
#607872 Rev1p1
PDG VCCRTCEXT (Pin DV34)
0402 0.1UF 1PCS
#607872 Rev1p1
PDG VCCLDOSTD_0P85
0402 2.2UF 1PCS
#607872 Rev1p1
PDG VCCDPHY_1P24
0402 4.7UF 1PCS
#607872 Rev1p1
PDG VCCDSW_1P05
0402 1UF 1PCS
#607872 Rev1p1
PDG VCCRTC
0402 0.1UF 1PCS
0402 1UF 1PCS
#607872 Rev1p1
PDG VCCDSW_3P3
0402 Placeholder 1PCS
Trace width > 40mil
1D05V_S5_VCCDSW_OUT
C2201
SC1U10V2KX-L1-GP
Place cap within 3mm from SOC edge.
1D24V_S5_VCCDPHY_OUT
For CNVi
C2202
SC4D7U6D3V2MX-GP-U
Place cap within 3mm from SOC edge
0D85V_S5_VCCLDOSTD_OUT
C2203
SC2D2U6D3V2MX-GP
Must take care this power layout and add shield GND.
1D8V_S5
(165mA)
3V_S5_CLKLDO
R2205
0R0402-PAD-1-GP
C2204
SC22U6D3V3MX-L1-GP
C2205
SC22U6D3V3MX-L1-GP
#607872 Rev1p1
PDG VCCA_CLKLDO_1P8
680nF
0603 0OHM 1PCS
0603 47UF 1PCS
PH Same as SPI Programming Guide for details
3D3V_S5
RN2201
SRN10KJ-5-GP
CORE_VID0/1 can PU to VCCPRIM_1P8 or 3P3.
(1.3A)
1D8V_S5_VCCPRIM
C2206
C2207
SC1U10V2KX-L1-GP
3D3V_S5_VCCPRIM
C2208
C2209
SC1U10V2KX-L-GP
3D3V_RTC_AUX
C2210
C2211
3D3V_RTC_EXT
C2212
SCD1U16V2KX-L-GP
1D05V_S5_VCCPRIM_OUT
C2213
SC1U10V2KX-L1-GP
3D3V_VCCDSW
C2219
SC1U10V2KX-L1-GP
1D05V_S5_OUT
C2216
SC1U10V2KX-L1-GP
3D3V_S5
C2217
SC1U10V2KX-L1-GP
3D3V_GPPR_S5
C2218
SCD1U16V2KX-L-GP
Close to pin DD37
C560
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCH-LP PWR&Caps)
Size A3
Document Number
C560-TGL
Rev -1
Date: Saturday, August 15, 2020
Sheet 22 of 106



C560

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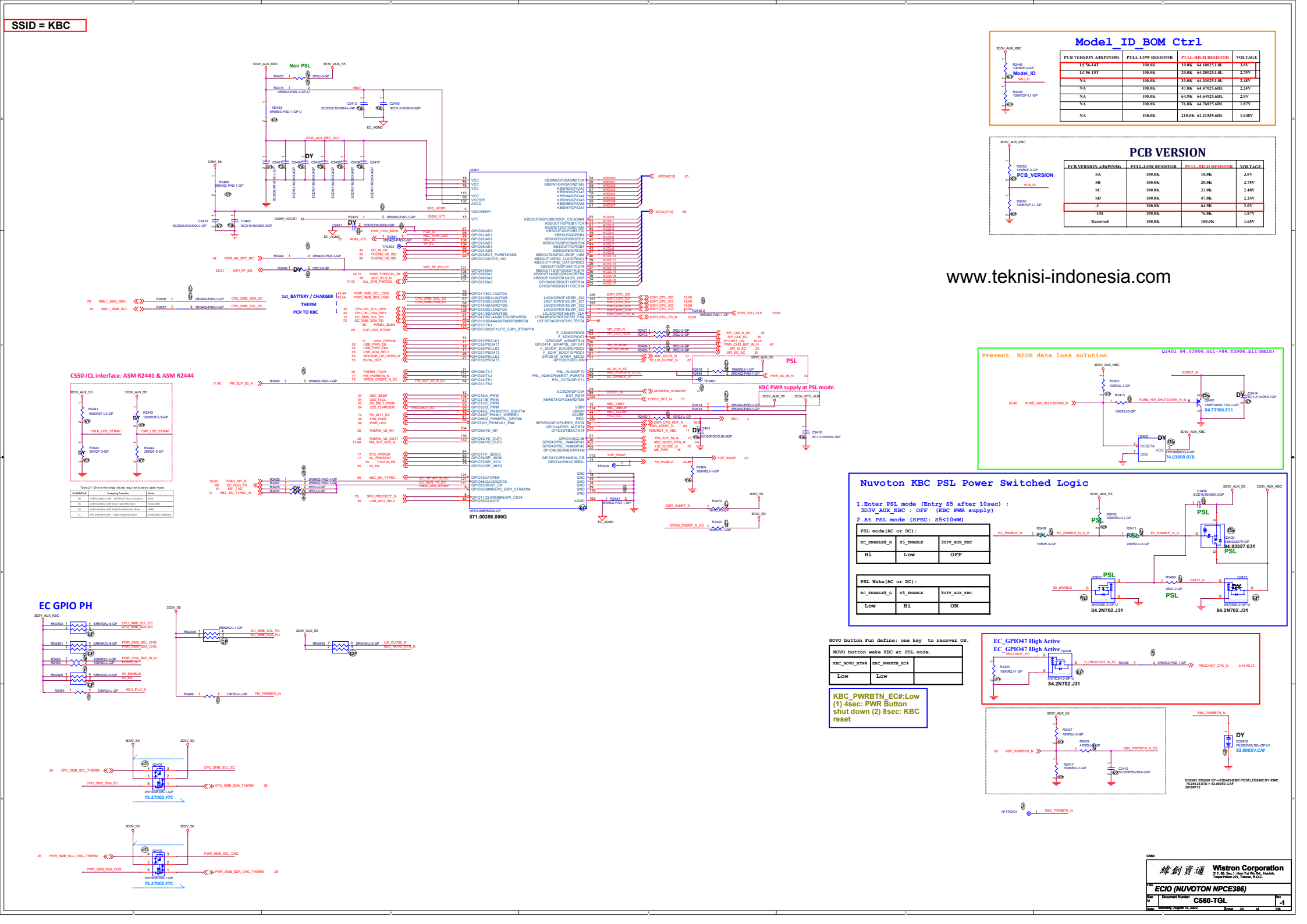
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
B	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 23 of 106

SSID = KBC



Model_ID_BOM Ctrl

PCB VERSION A/D(PIN100)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LC56-14T	100.0K	10.0K 64.39025I.0L	3.0V
LC56-15T	100.0K	20.0K 64.39025I.0L	2.75V
NA	100.0K	33.0K 64.33025I.0L	2.48V
NA	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

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Prevent BIOS data loss solution

Q2401 84.03906.G11->84.T3906.E11(main)

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):

EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):

EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down (2) 8sec: KBC reset

EC_GPIO47 High Active

EC_GPIO47 High Active

84.2N702.J31

ED2401,ED2402 DY:=ED2401(EMC-TEST),ED2402 DY-EMC: 75.00125.07D-> 83.0005V.CAF
20150712

C560

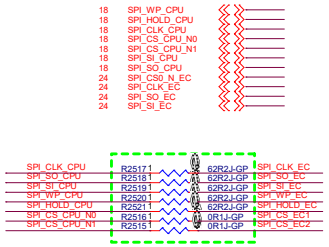
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

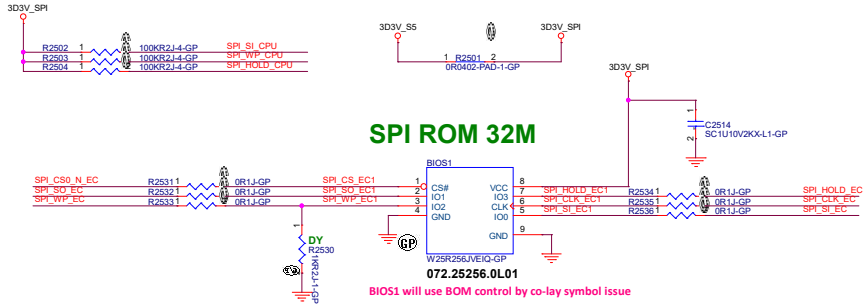
Title: ECIO (NUVOTON NPCE386)

Size: M | Document Number: C560-TGL | Rev: -1

Date: Saturday, August 15, 2009 | Sheet 24 of 100

SSID = Flash.ROM





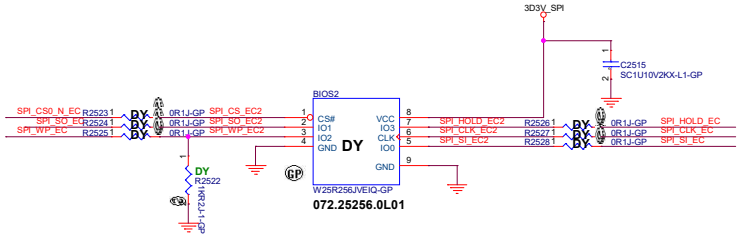


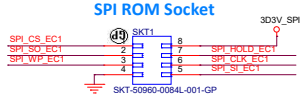
TABLE BIOS1
32MB(256Mb) WSON8 (Optional)

Vender	Vender P/N	Wistron P/N
WINBOND	W25R256JVEIQ	072.25256.0L01
GIGADEVICE	GD25R256DYIGR	072.25256.0H03

EVT ASM

Co-Layout Design on BIOS1

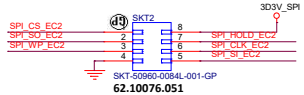
SPI ROM Socket



62.10076.051

DY

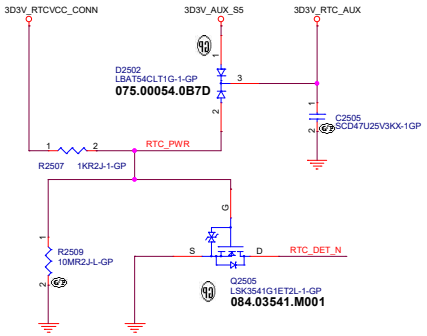
Co-Layout Design on BIOS2

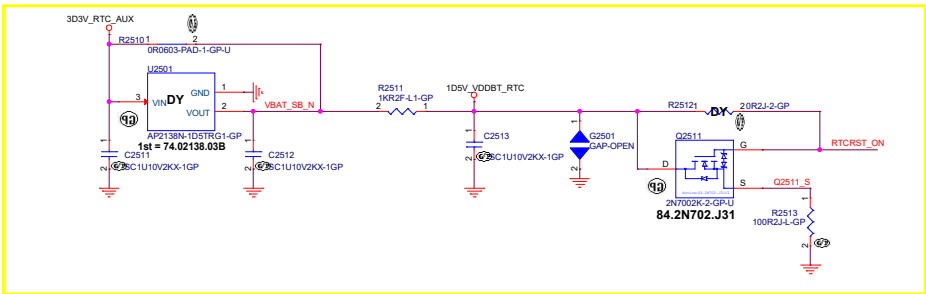


62.10076.051

DY

SSID = RBAT





C560

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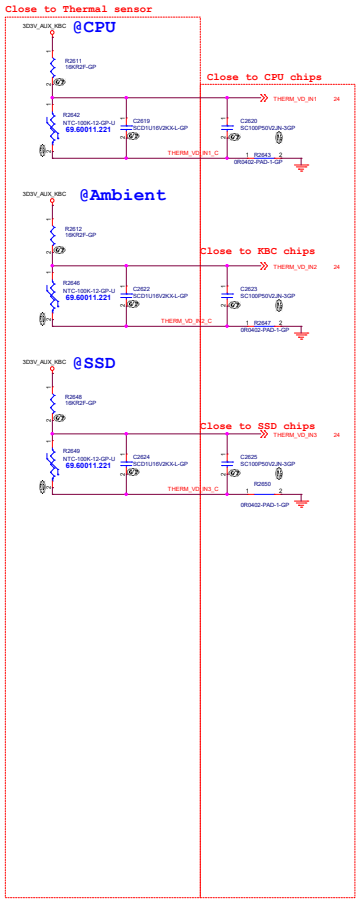
Taipei Hsien 221, Taiwan, R.O.C.

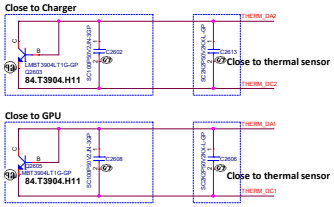
Title: **FLASH/RTC**

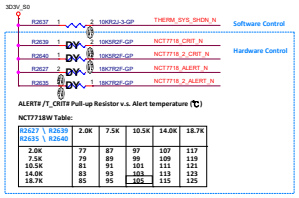
Size: A2 | Document Number: **C560-TGL** | Rev: -1

Date: Tuesday, August 25, 2020 | Sheet 25 of 106

Main Func = Thermal Sensor



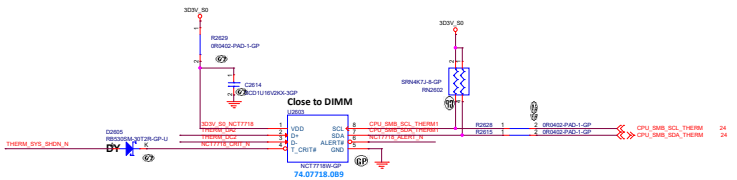


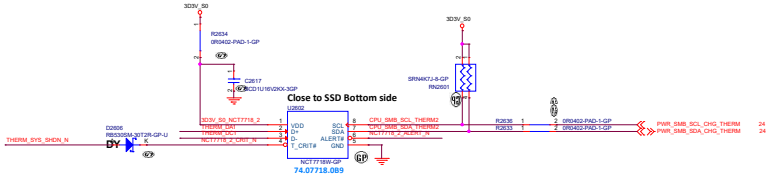


ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

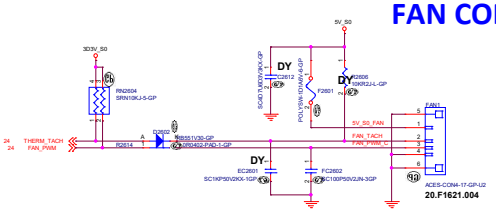
NCT7718W Table:

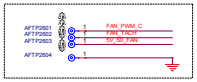
R2627 \ R2639 R2635 \ R2640	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

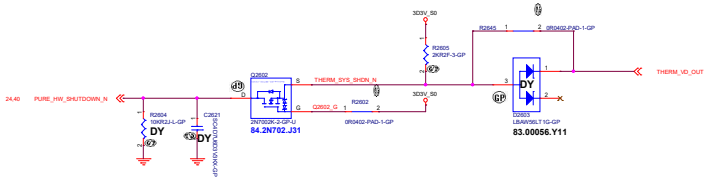


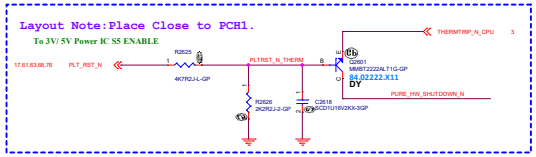


FAN CONN







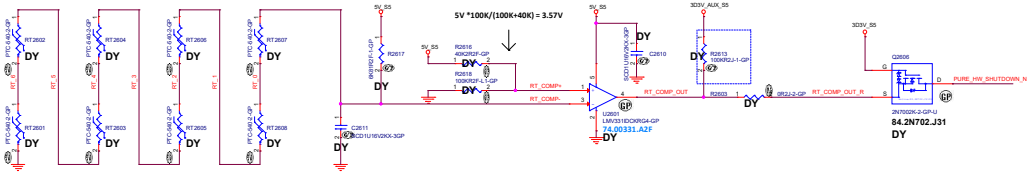


PURE_HW_SHUTDOWN# logic table

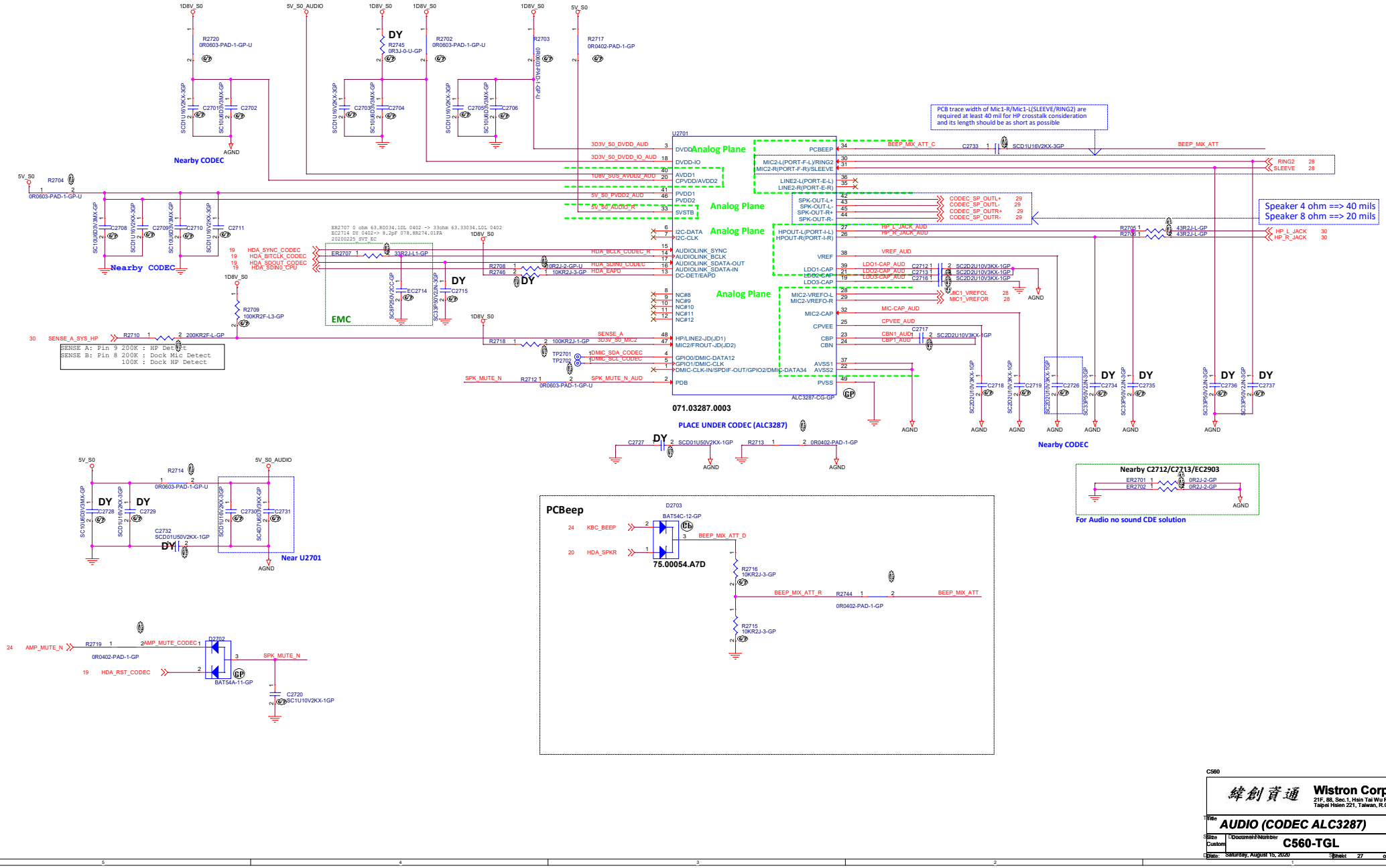
signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

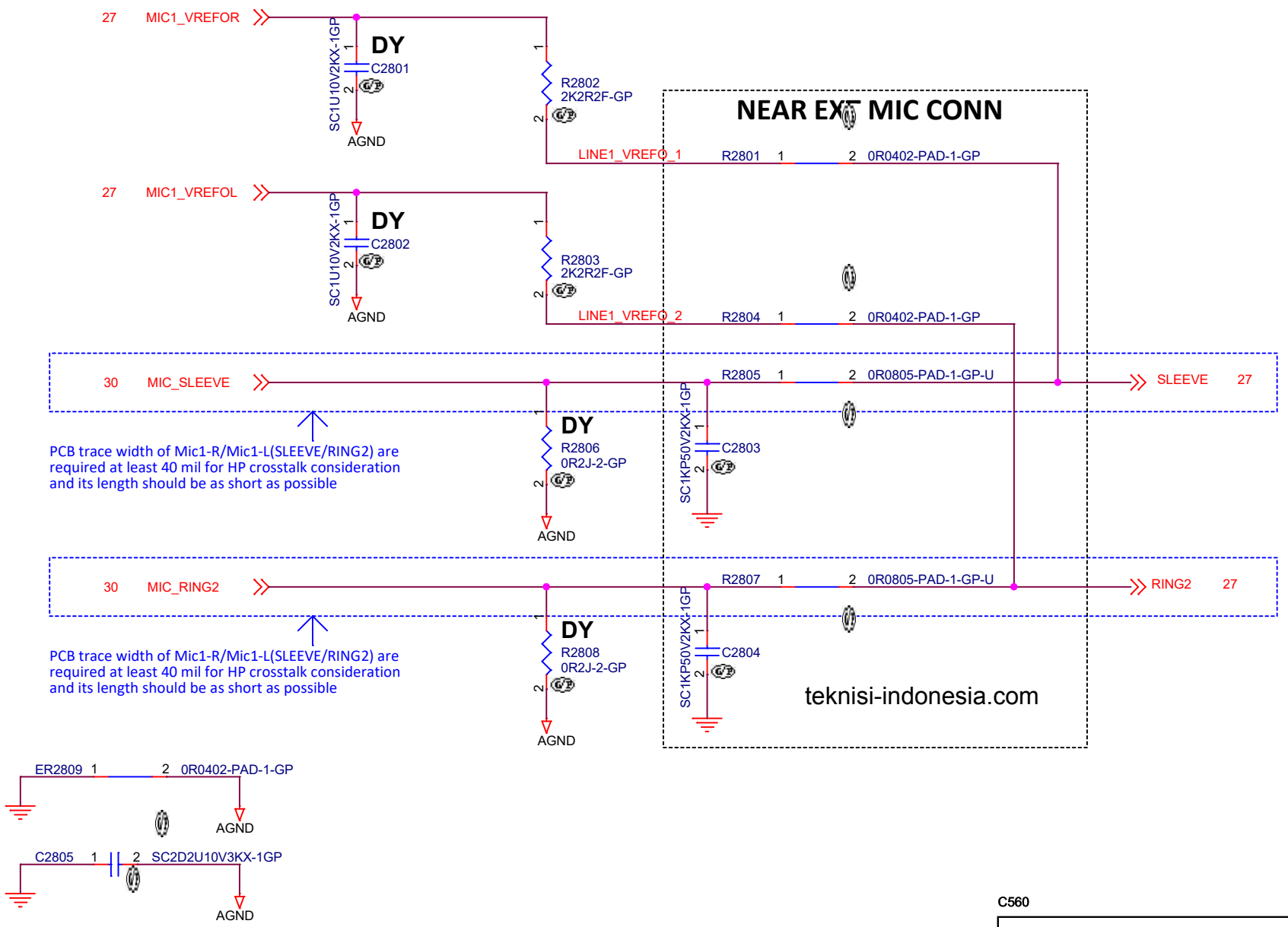
TABLE:

ID	Target	Function
RT2601	PU5101	1D2V_S3
RT2602	PU4801	1V_VCCGT
RT2603	PQ5201	1D05V_SUS
RT2604	PU4701	1V_CPU_CORE
RT2605	PQ4505	5V_S5
RT2606	PQ4506	3D3V_S5
RT2607	PU4404	Charger-Buck
RT2608	PU4406	Charger-Boost



C560	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title:	INT IO (THERMAL/FAN)
Size: D	Document Number: C560-TGL
Rev: -1	
Date: Saturday, August 15, 2020	Sheet 26 of 106


Nearby CODEC
Nearby CODEC
EMC
Analog Plane
Analog Plane
Analog Plane
Analog Plane
U2701
ALC3287-CG-GP
071.03287.0003
PLACE UNDER CODEC (ALC3287)
Nearby CODEC
Near U2701
PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
SENSE A: Pin 9 200K : HP Detect
SENSE B: Pin 8 200K : Dock Mic Detect
100K : Dock HP Detect
PCBeep
75.00054.A7D
Nearby C2712/C2713/EC2903
For Audio no sound CDE solution
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (CODEC ALC3287)
C560-TGL
Saturday, August 15, 2020
Sheet 27 of 106



C560

緯創資通

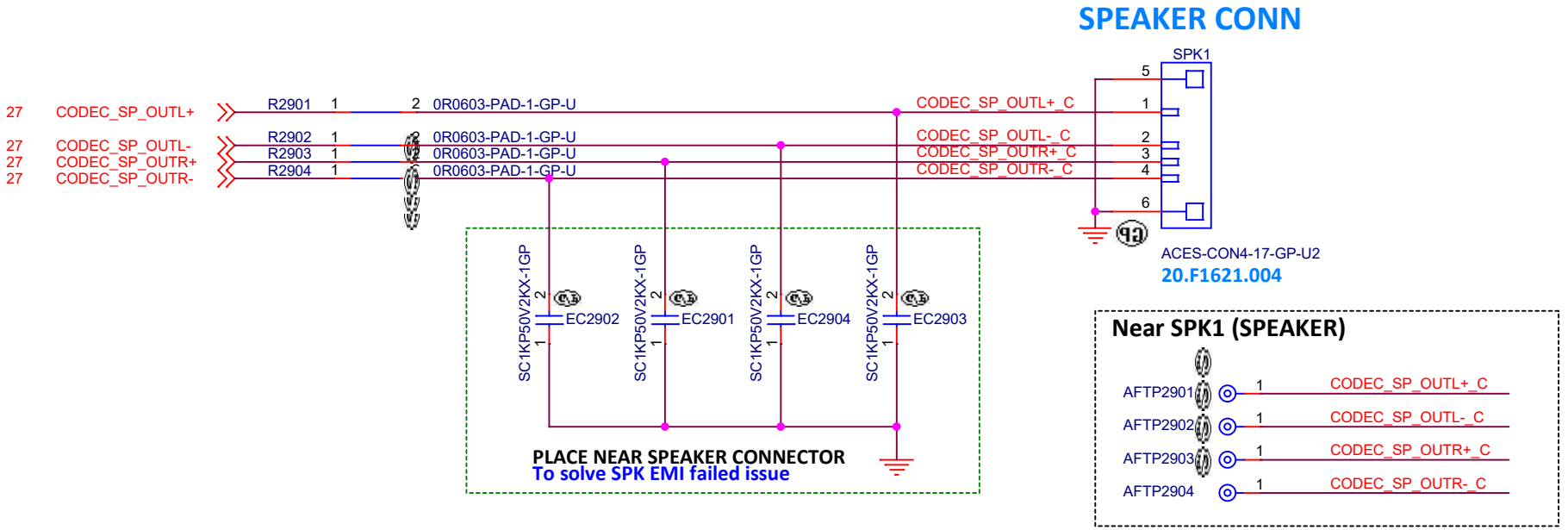
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (MIC I/F)***

Size	Document Number	Rev
A4	C560-TGL	-1

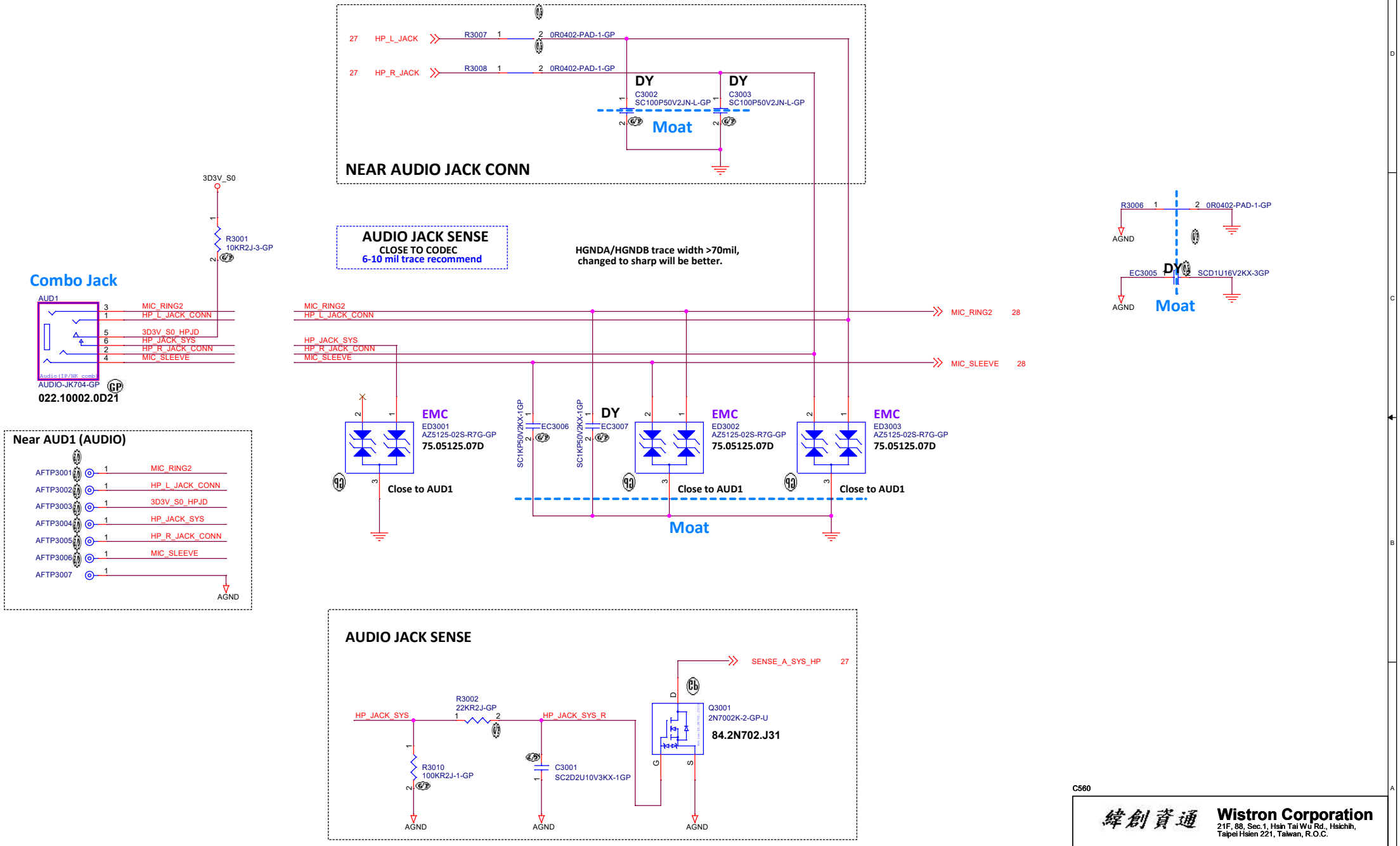
Date: Saturday, August 15, 2020 Sheet 28 of 106

Main Func = AUDIO



C560

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (SPEAKER)		
Size: A4	Document Number: C560-TGL	Rev: -1
Date: Saturday, August 15, 2020	Sheet 29 of 106	



C560

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (AUDIO JACK)

Size	Document Number	Rev
A3	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 30 of 106

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C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN (RSVD)*

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 31 of 106

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C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **LAN (RSVD)**

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 32 of 106

(Blanking)

C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARDREADER (SDIO/SD CONN)***

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 33 of 106

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB (RSVD)*

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 34 of 106

(Blanking)

C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

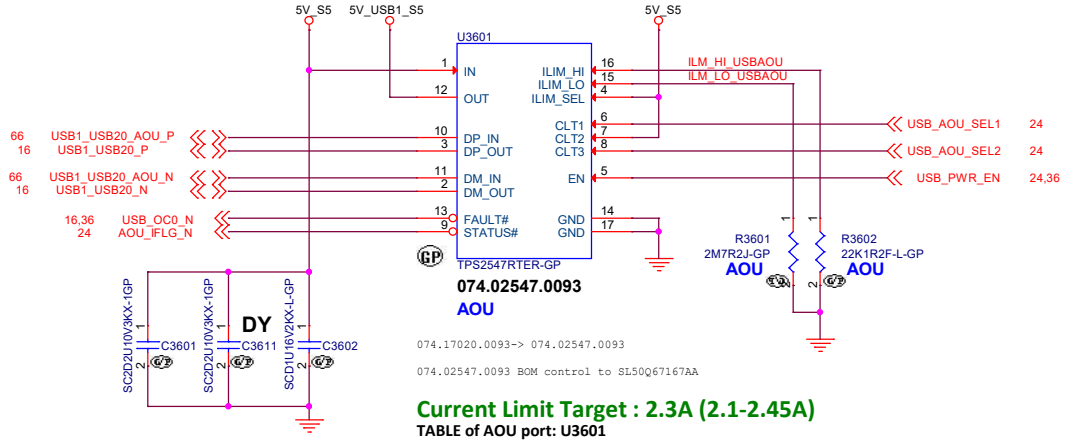
Title: ***USB (CHARGER/SWITCH)***

Size	Document Number	Rev
A4	C560-TGL	-1

Date: Saturday, August 15, 2020 Sheet 35 of 106

Main Func = USB Charger

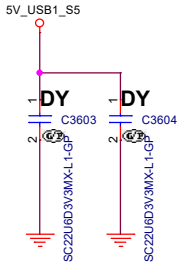
For USB3.0 System Port1 (For AOU)



074.17020.0093-> 074.02547.0093

074.02547.0093 BOM control to SL50Q67167AA

Layout Note: Close 5V_USB1_S5



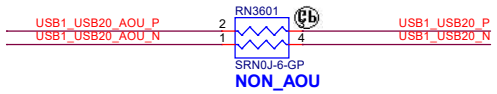
Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3601

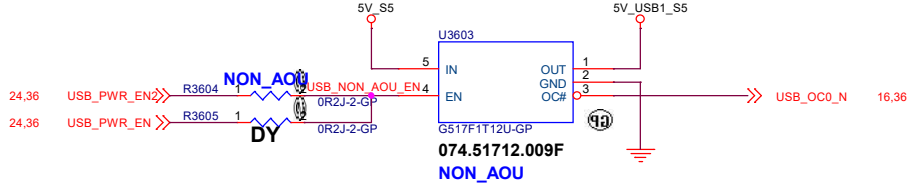
	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER	SL50Q67167AA
2nd	DIODES	PI5USB2546HZHEX	SL50Q67168AA

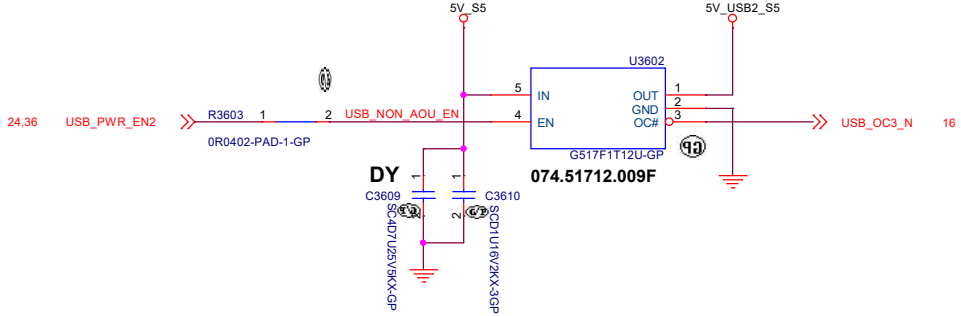
LC560 SIT Verify

SN1702001RTER is not equivalent device of TPS2546RTER

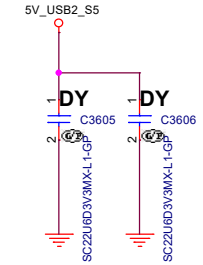


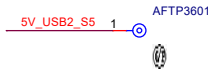
For USB3.0 System Port2





Layout Note: Close 5V_USB2_S5





C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB(USB Charger)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB (RSVD)*

Size	Document Number	Rev
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)(USB Redriver/Hub)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SEQUENCE (RSVD)***

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RUN Power

17,24 PM_SLP_S3_N
17,24 PM_SLP_SUS_N
46 PWR_VCORE_VR_EN
17 PCH_PWROK
51 PWR_VDDQ_PG
22,50 VCCIN_AUX_VID0
22,50 VCCIN_AUX_VID1
17 VCCST_OVERRIDE
17,24 ALL_SYS_PWRGD
46 VCORE_READY
17 CPU_C10_GATE_N
24,26 PURE_HW_SHUTDOWN_N
53 1D8V_S5_EN
50,53 1D8V_S5_PWRGD
4,55 eDP_VDDEN_CPU

RUN Power

5V_S0/3D3V_S0

U4001 G2898KD1U-GP
074.02898.0093
074.22976.0091
SW_5V_S0_CT
SW_3D3V_S0_CT
5V_S0_FIP
3D3V_S0_FIP
5V_S0 (2.5A)
3D3V_S0 (2A)
3V_5V_S0_EN

For CODEC

U4003 G2898KD1U-GP
074.02898.0093
074.22976.0091
SW_3D3V_LCD_S0_CT
SW_1D8V_S0_CT
3D3V_LCD_S0_FIP
1D8V_S0_FIP
1D8V_S0 (150mA)
eDP_VDDEN_CPU
U4003_EN1
U4003_EN2

R4031 100KR1J-GP U4003_EN1

6A/Rds(on):4.5mOhm/Tr:7~20us

U4004 APE8939GN3-GP
074.08939.0093
1D05V_S5_OUT
1D05V_VCCSTG_FIP
1D05V_VCCSTG (300mA)
VCCSTG_EN

D4001 BAT54C-12-GP
VCCIN_AUX_VID0
VCCIN_AUX_VID1
VCCST_READY
VCCST_OVERRIDE_3D3V
D4002 LRB520S-30T1G-GP
PM_SLP_S3_N
D4003 LRB520S-30T1G-GP
VCCST_READY
VCCST_EN
D4007 LRB520S-30T1G-GP
CPU_C10_GATE_N
D4004 LRB520S-30T1G-GP
VCCST_READY
VCCSTG_EN
D4008 LRB520S-30T1G-GP

U4002 G2898KD1U-GP
074.02898.0093
074.22976.0091
SW_3D3V_S5_CT
3D3V_SUS_FIP
3D3V_S5 (2A)
3D3V_EN_R
S5_ENABLE
D4006 LRB520S-30T1G-GP
PURE_HW_SHUTDOWN_N

6A/Rds(on):4.5mOhm/Tr:7~20us

U4005 APE8939GN3-GP
074.08939.0093
1D05V_S5_OUT
1D05V_VCCST_FIP
1D05V_VCCST (500mA)
VCCST_EN

TOP

AFTP4001
AFTP4002
AFTP4003
AFTP4004
AFTP4005

Power Sequence / Pull High PWRGD

R4014 10KR2J-3-GP
VCORE_READY
PCH_PWROK
R4018 0R0402-PAD-1-GP
C4028 SCD1U16V2KX-L-GP

PM_SLP_SUS_N
R4013 0R0402-PAD-1-GP
1D8V_S5_EN
C4027 SCD1U16V2KX-L-GP

R4021 1KR2J-1-GP
D4005 LRB520S-30T1G-GP
PM_SLP_S3_N
PWR_VDDQ_PG
R4024 0R0402-PAD-1-GP
ALL_SYS_PWRGD
R4025 0R0402-PAD-1-GP
PWR_VCORE_VR_EN

R4022 20KR2J-L3-GP
1D8V_S5_PWRGD

R4016 100KR2J-1-GP
VCCST_OVERRIDE_Q1
Q4002 LSI1012LT1G-GP
084.01012.0031
(1.05V)
VCCST_OVERRIDE

R4017 100KR2J-1-GP
VCCST_OVERRIDE_3D3V
Q4003 LSK3541G1ET2L-1-GP
084.03541.M001

C560

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SEQUENCE (POWER PLANE EN)
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C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SEQUENCE (RSVD)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*

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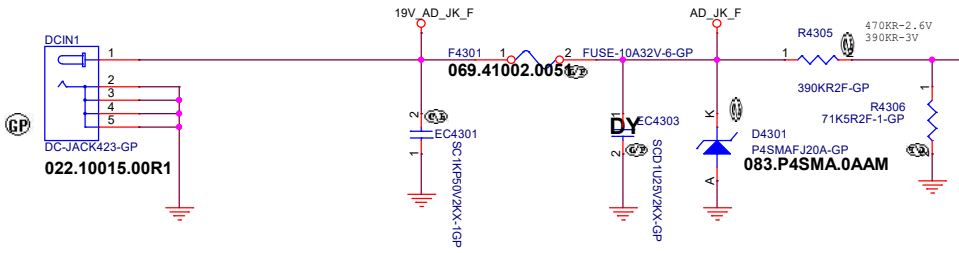
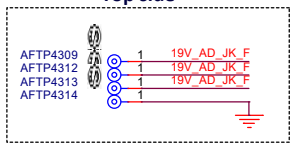
Total MLCC capacitance at DCIN connector
is smaller than 1000pf to avoid LC resonance

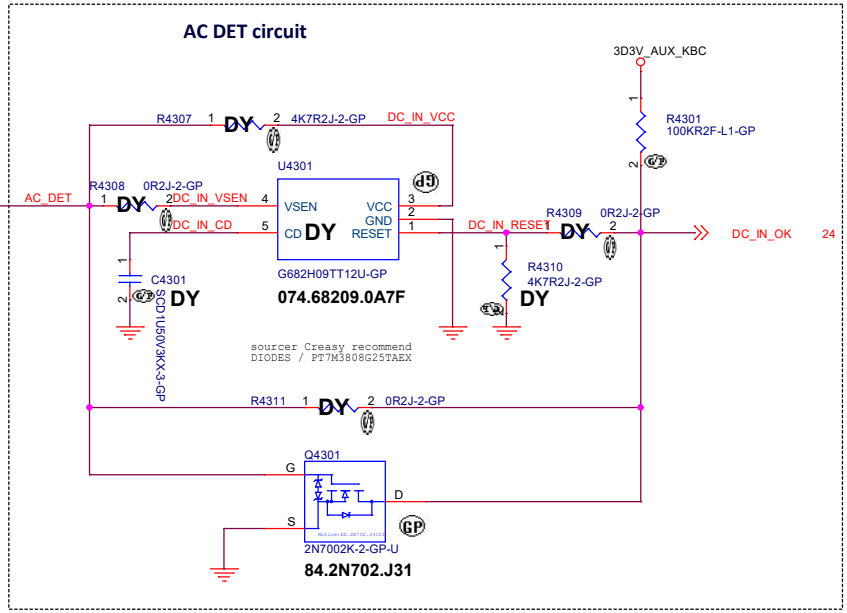
DCIN CONN



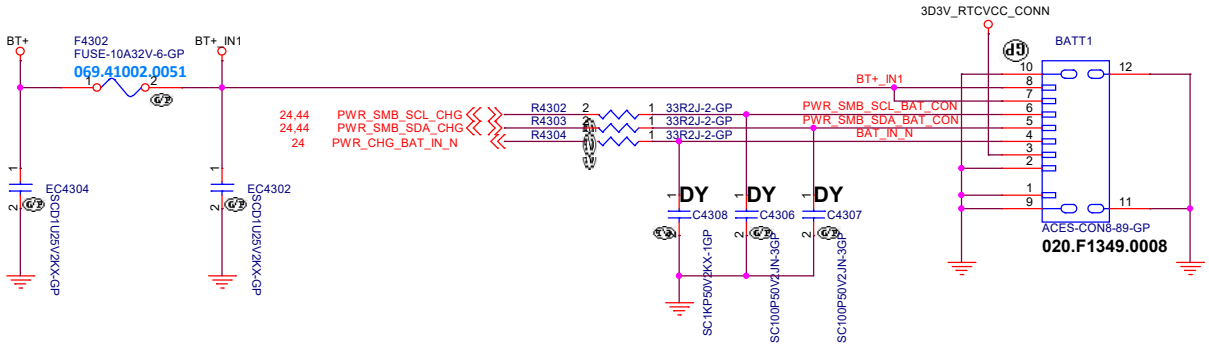
Top side



AC DET circuit



Main Battery Connector



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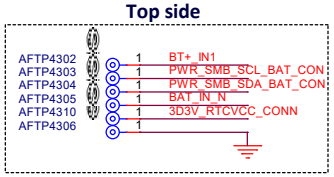

C560

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *INT IO (DCIN/BATT CONN)*		
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OFFPAGE - PIC - EE

PH on EE Side

PWR_SMB_SCL_CHG
PWR_SMB_SDA_CHG

PH on EE Side

PROCHOT_CPU_N
PWR_AD_OFF_RC
PWR_TYPECIN_OK
for typeC
CHGR_PSYS_IMVP
PWR_AC_IN_N
PWR_CHG_IMON

Device will be transition from normal Buck-Boost operation to PFM operation by:
- Set REGN[7] = 0, to disable the EN_EXTILIM.
- Set REGN[8] = 1.
- Set REGN[9] = 1.
- Ground ILIM_HIZ pin.

Device will transition out of PFM mode with host control by:
- Set REGN[9] = 0 to
- Pull ILIM_HIZ pin to high

- Device exits PFM to buck-boost operation if tripping VINDPM or IINDPM
- Device exits PFM to buck-boost operation under fault conditions (ACOC, TSHUT, BATOC)

For Adapter IN
Confirm with EE

AD_JK_F

PWR_ADP_19V

PWR_ADP_TOSYS

Id= -10A
Qg= -22nC
Rdson=14-22mohm

AD+_2 trace width > 8mil
Length < 500mil

For Adapter IN
Confirm with EE

PWR_ADP_TOSYS

0505
buyer: 7"

	V (1120)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

Reserve for Power test

# of CELL	VCELL_PROG	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

Company	Wistron Corporation	
Title	POWER (CHARGER_BQ25710R)	
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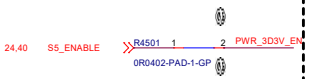
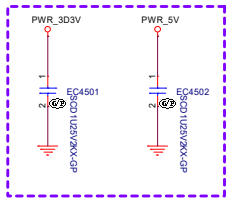


C560 EVT EMC



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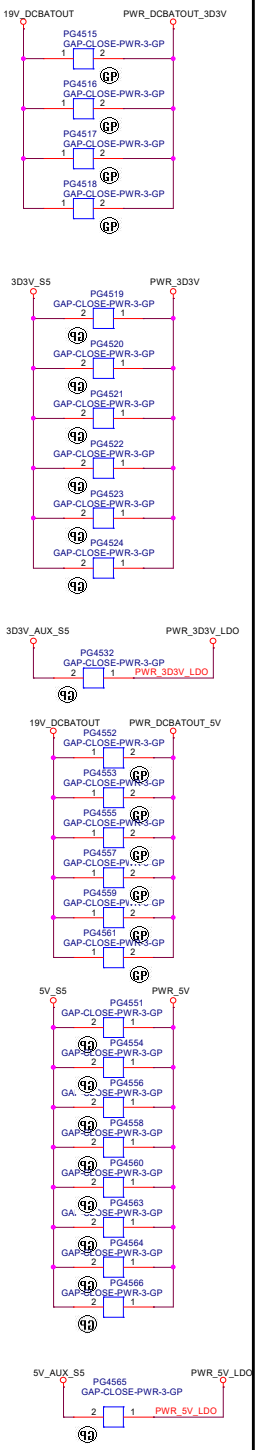

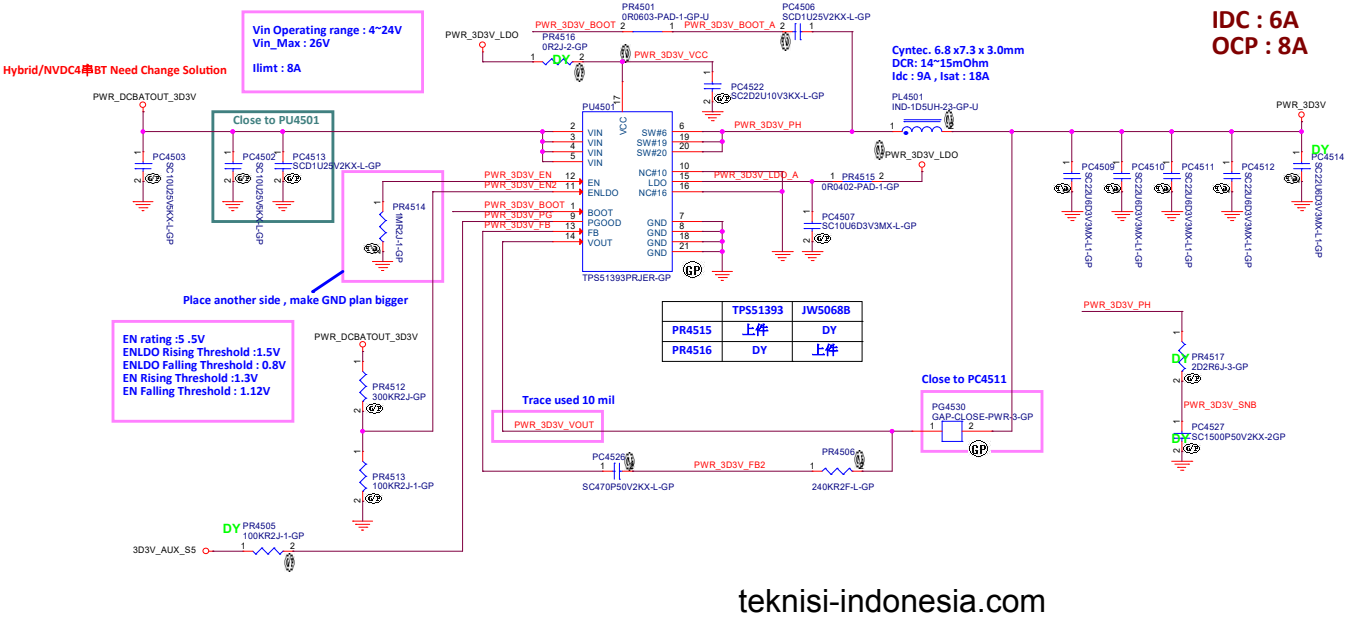

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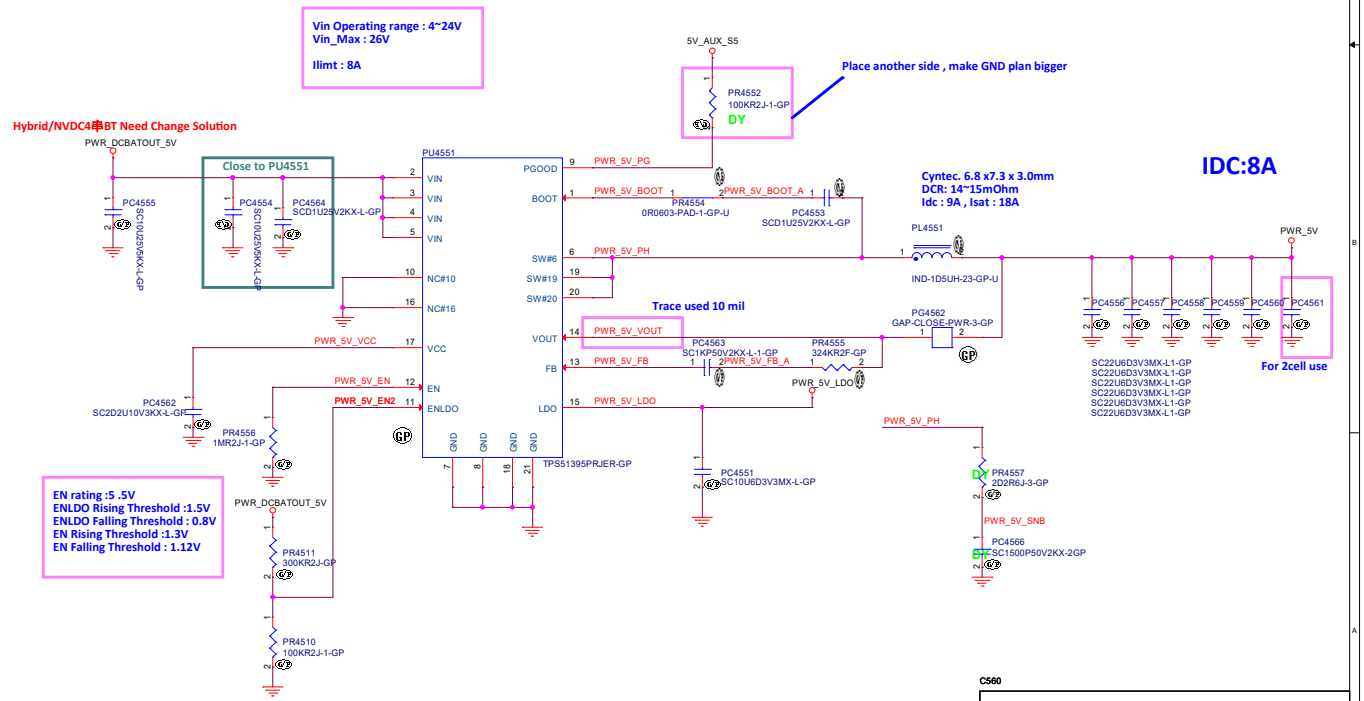

C560

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	POWER (TPS51393_5V/3D3V)
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PH on CPU side
PROCHOT_CPU_N
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT_N_CPU
PWR_VCORE_VR_EN
VCORE_PG
PH on CPU side
VCORE_READY
PWR_VCORE_VR_READY
VSSCORE_SENSE
VSSCORE_SENSE
VCCCORE_SENSE
VCCCORE_SENSE
CHGR_PSYS_IMVP
CHGR_PSYS_IMVP
2E side Link
SVID Pull High V
1D05V_VCCST
PWR_VCORE_VCCST

Reserve for Power test

PWR_VCORE_VCCST
PWR_VCORE_VR_READY
PROCHOT_CPU_N
CHGR_PSYS_IMVP
PWR_VCORE_PSYS

	ICL IccMax=72A	TGL IccMax=66A
PR4619	3.57K	1.4K
PR4666	357	0
PR4624	3.48K	1.02K
PR4669	100	100

TGL_28W測試單板 VBOOT = 1.8V
PR4666 = 2.74kohm
PR4624 = 3.24kohm

TGL_15W單板測試VBOOT = 1.8V
PR4619 = 1.4 kohm
PR4666 = 3.92 kohm
PR4624 = 2.87 kohm
PR4669 = 10 ohm

VR_HOT Thermal_Alert#	100C/97C	Lily 120C/100C
PR4627	24.9K	36.5K
PR4622	12.4K	17.8K
PR4701	110K	3.48K

電感3/高 0.9mohm	ICL IccMax=72A	TGL IccMax=66A
PR4601	26.7K	30.1K
PR4665	2.87K	2.05K
PR4643	17.8K	18.7K

PWR_VCORE_VREF
PWR_VCORE_SET1_A
PWR_VCORE_SET2_A
PWR_VCORE_SET3_A
PWR_VCORE_TSEN
PWR_VCORE_TSEN_A
PWR_VCORE_SET1_B
PWR_VCORE_SET2_B
PWR_VCORE_TSEN_A_A
PWR_VCORE_SET3_B
PWR_VCORE_VCCST
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT_N_CPU
LL/IMON Compesation
NCP15XH103F03RC
Need confirm with RT If you change Chock
Close to PL47[0]
B = 4250
PWR_VCORE_NTC1N
PWR_VCORE_NTC1N_A
PWR_VCORE_NTC1P
PWR_VCORE_VREF
PWR_VCORE_VR_READY
PWR_VCORE_PSYS
PWR_VCORE_CLK
PWR_VCORE_DATA
PWR_VCORE_ALERT_N
PWR_VCORE_IMON

PU4601
RT3612EB
RT3612EBGQW-1-GP

電感3/高 0.9mohm	電感4/高 0.66mohm
PR4628 PR4633	2K	2K
PR4655 PR4646	2K	2K
PR4662 PR4665	2.61K	4.64K

0603_Size
0603_Size

電感3/高 0.9mohm	ICL IccMax=72A	TGL IccMax=66A
PR4640	31.6K	34K

1V_CPU_CORE
PWR_VCORE_VSEN
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RGND
VCCCORE_SENSE
VSSCORE_SENSE

C560

緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title:	POWER (RT3612EB_VCORE(1/2))	
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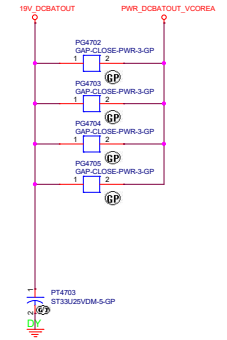

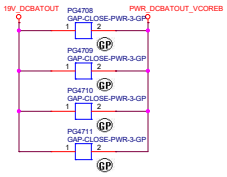

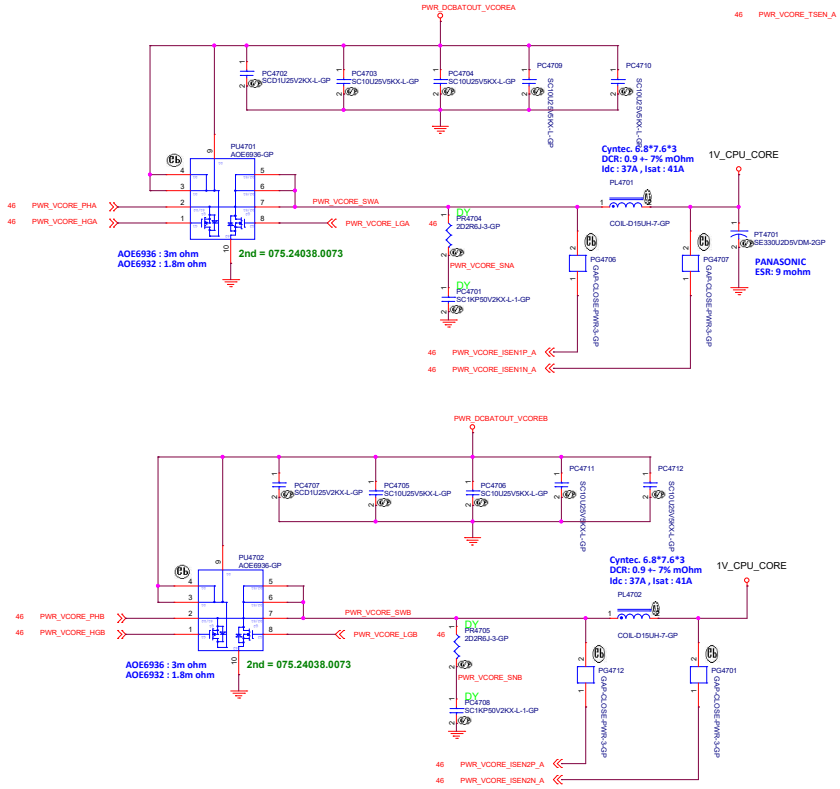

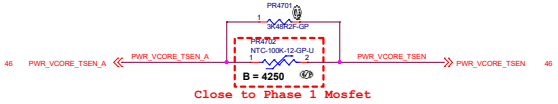

C560

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER (AOE6936_VCORE(2/2))		
Size: Custom	Document Number: C560-TGL	Rev: -1
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C560

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RSVD)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RSVD)***

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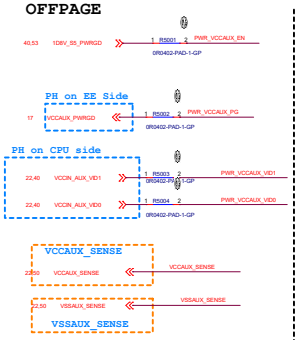

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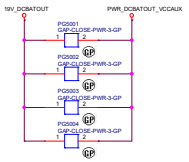

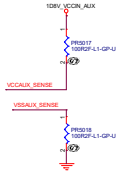

TABLE: MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

LOGIC

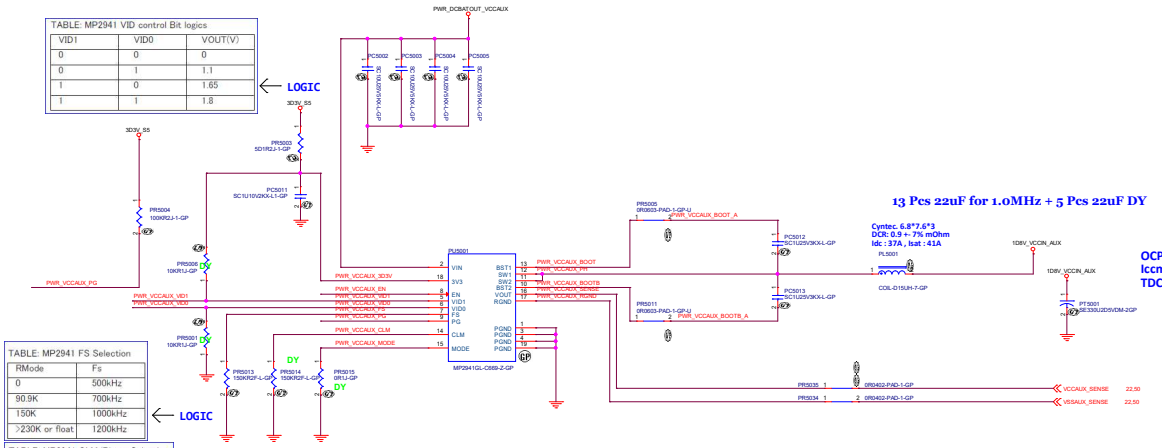

TABLE: MP2941 FS Selection

RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

LOGIC

TABLE: MP2941 CLM/Phase Selection

RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

LOGIC

TABLE: MP2941 Mode Selection

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

LOGIC

TABLE : MP2941

Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary

C560

緯創資通	Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	POWER (RT6543_VCCAUX)
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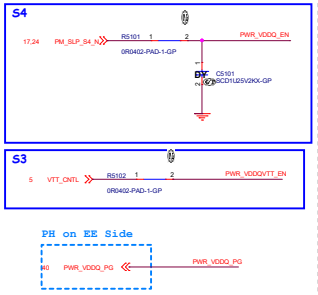

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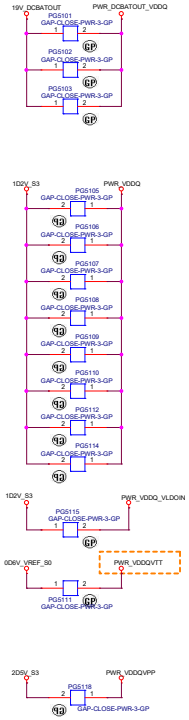

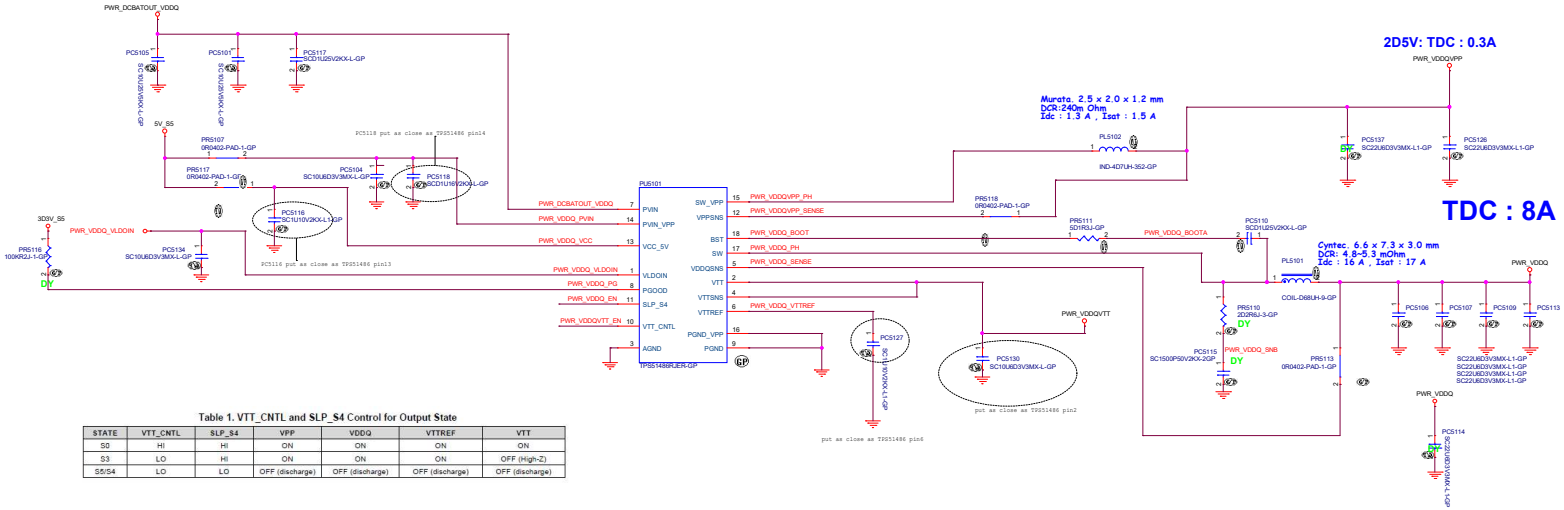

Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

C560

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS51486R_VDDQ/VTT)

Size: Custom | Document Number: C560-TGL | Rev: -1

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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OFFPAGE

PH on EE Side

40,50 1D8V_S5_PWRGD — R5301 1 2 PWR_1D8V_PG — 0R0402-PAD-1-GP

40 1D8V_S5_EN — R5302 1 2 PWR_1D8V_EN — 0R0402-PAD-1-GP

OFFPAGE_GAP

3D3V_S5 — PG5301 GAP-CLOSE-PWR-3-GP — PWR_1D8V_VIN

PG5302 GAP-CLOSE-PWR-3-GP

1D8V_S5 — PG5303 GAP-CLOSE-PWR-3-GP — PWR_1D8V

PG5304 GAP-CLOSE-PWR-3-GP

PG5305 GAP-CLOSE-PWR-3-GP

TDC=2A
Imax= 3A

TOKO. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A

PWR_1D8V_VIN

PC5301 SC22U6D3V3MX-L1-GP

3D3V_S5

DY PR5305 100KR2F-L1-GP

PWR_1D8V_EN

DY PC5307 SC1U10V2KX-L1-GP

PU5301 RT5797ALGQW-GP

PGND 9
PGND 4
VIN 3
PG 2
FB 1
NC#5 5
LX 6
EN 7
SGND 8

PWR_1D8V_VIN
PWR_1D8V_PG
PWR_1D8V_FB
PWR_1D8V_PH
PWR_1D8V_EN

PL5301 IND-1UH-382-GP

PR5303 100KR2F-L1-GP

PR5304 49K9R2F-L-GP

DY PC5305 SC22P50V2JN-L-GP

PWR_1D8V

PC5302 SC22U6D3V3MX-L1-GP

PC5303 SC22U6D3V3MX-L1-GP

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Title: POWER (RT5797_1D8V)

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Title: *POWER(APW8743_VNN1D05V)*		
Size: Custom	Document Number: C560-TGL	Rev: -1
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Main Func = LCD

LCD Connector

INVERTER POWER

F5501 69.50007.A31->69.42402.001 (main)_20180718

EMC request:Top

Test point

1) DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

Touch Connector

Touch

PLACE NEAR MIC1

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Title: DISPLAY (LCD/TOUCH)

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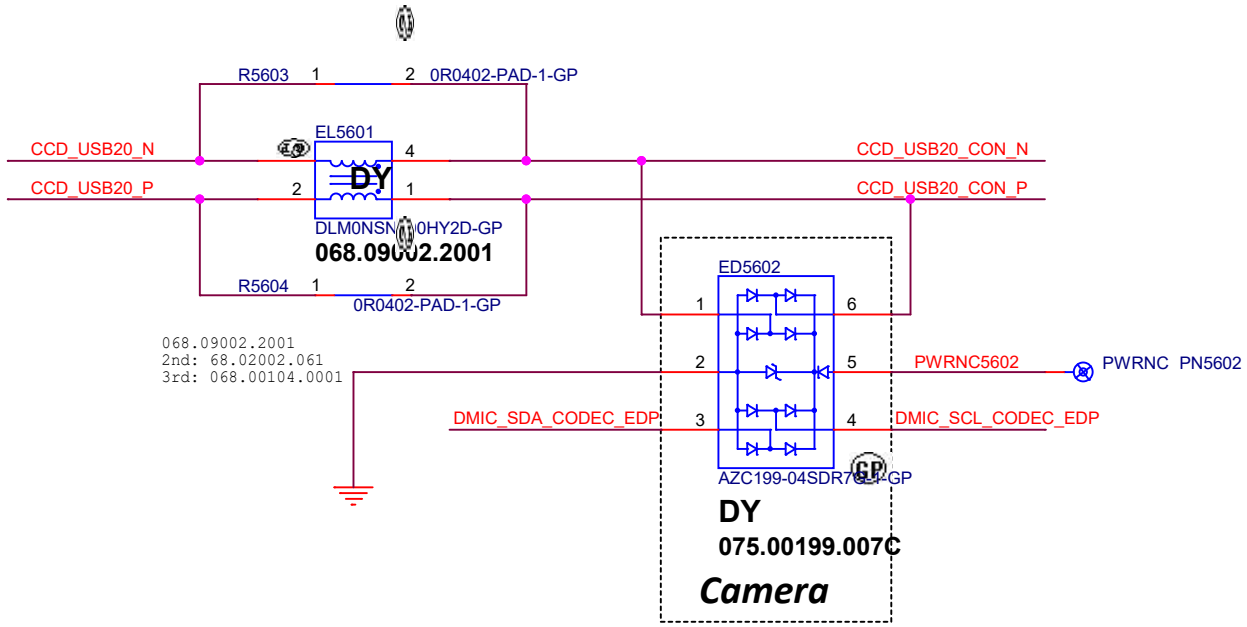
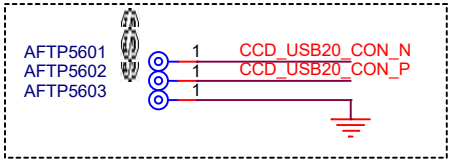
(Off-Page)

16 CCD_USB20_N
16 CCD_USB20_P
55 CCD_USB20_CON_N
55 CCD_USB20_CON_P
19,55 DMIC_SCL_CODEC_EDP
19,55 DMIC_SDA_CODEC_EDP

CCD CONN



BOT side



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Title: ***DISPLAY (CAMERA)***

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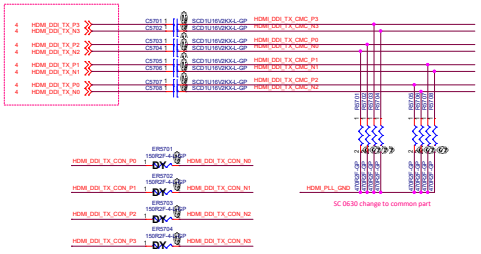
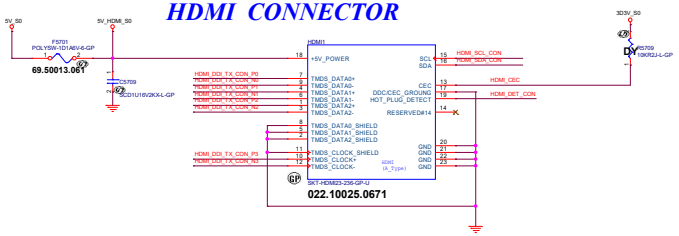
HDMI

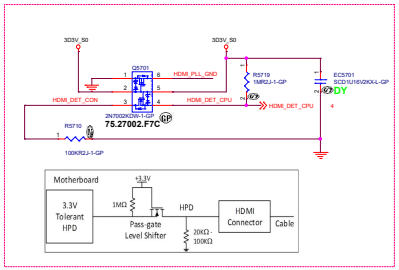
HDMI Passive Level Shifter

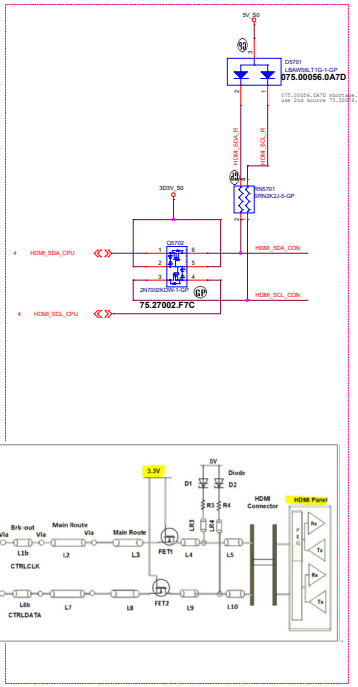
Close to HDMI Connector

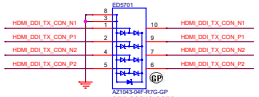


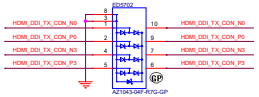
HDMI CONNECTOR

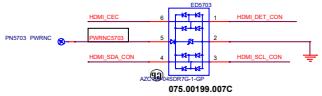


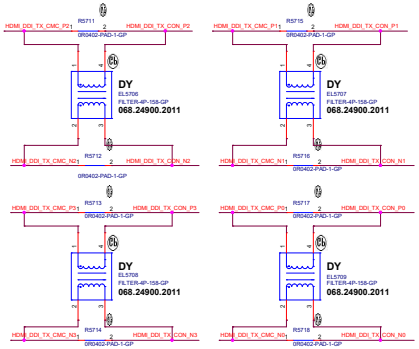












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Title: DISPLAY (HDMI CONN/RETIMER)

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Title: ***DISPLAY (RSVD)***		
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *DISPLAY (RSVD)*

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Title: *INT IO (RSVD)*

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Main Func = WLAN

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20,24 WIFI_RF_EN
19 BLUETOOTH_EN

17,26,63,66,76 PLT_RST_N
18 SUS_CLK
21 CNV_CLKREQ
19 CNV_RF_RESET_N

21 CNV_BRI_RSP
21 CNV_BRI_DT
21 CNV_RGI_RSP
15,21 CNV_RGI_DT

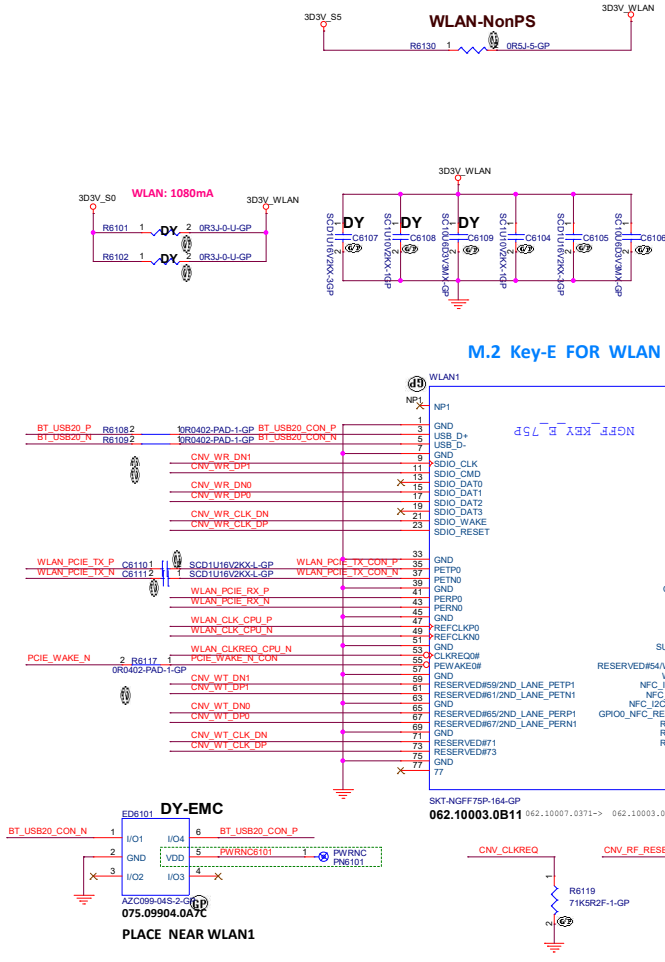
21 CNV_WT_CLK_DP
21 CNV_WT_CLK_DN
21 CNV_WT_DP0
21 CNV_WT_DN0
21 CNV_WT_DP1
21 CNV_WT_DN1

21 CNV_WR_CLK_DP
21 CNV_WR_CLK_DN
21 CNV_WR_DP0
21 CNV_WR_DN0
21 CNV_WR_DP1
21 CNV_WR_DN1

16 BT_USB20_P
16 BT_USB20_N

16 WLAN_PCIE_TX_P
16 WLAN_PCIE_TX_N
16 WLAN_PCIE_RX_P
16 WLAN_PCIE_RX_N
18 WLAN_CLK_CPU_P
18 WLAN_CLK_CPU_N

18 WLAN_CLKREQ_CPU_N
17 PCIE_WAKE_N



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Title: INT IO (WLAN/CNVi)

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SSD CONN

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16 SSD_PCIE_RX_N3
16 SSD_PCIE_RX_P3
16 SSD_PCIE_TX_N3
16 SSD_PCIE_TX_P3

16 SSD_PCIE_RX_N2
16 SSD_PCIE_RX_P2
16 SSD_PCIE_TX_N2
16 SSD_PCIE_TX_P2

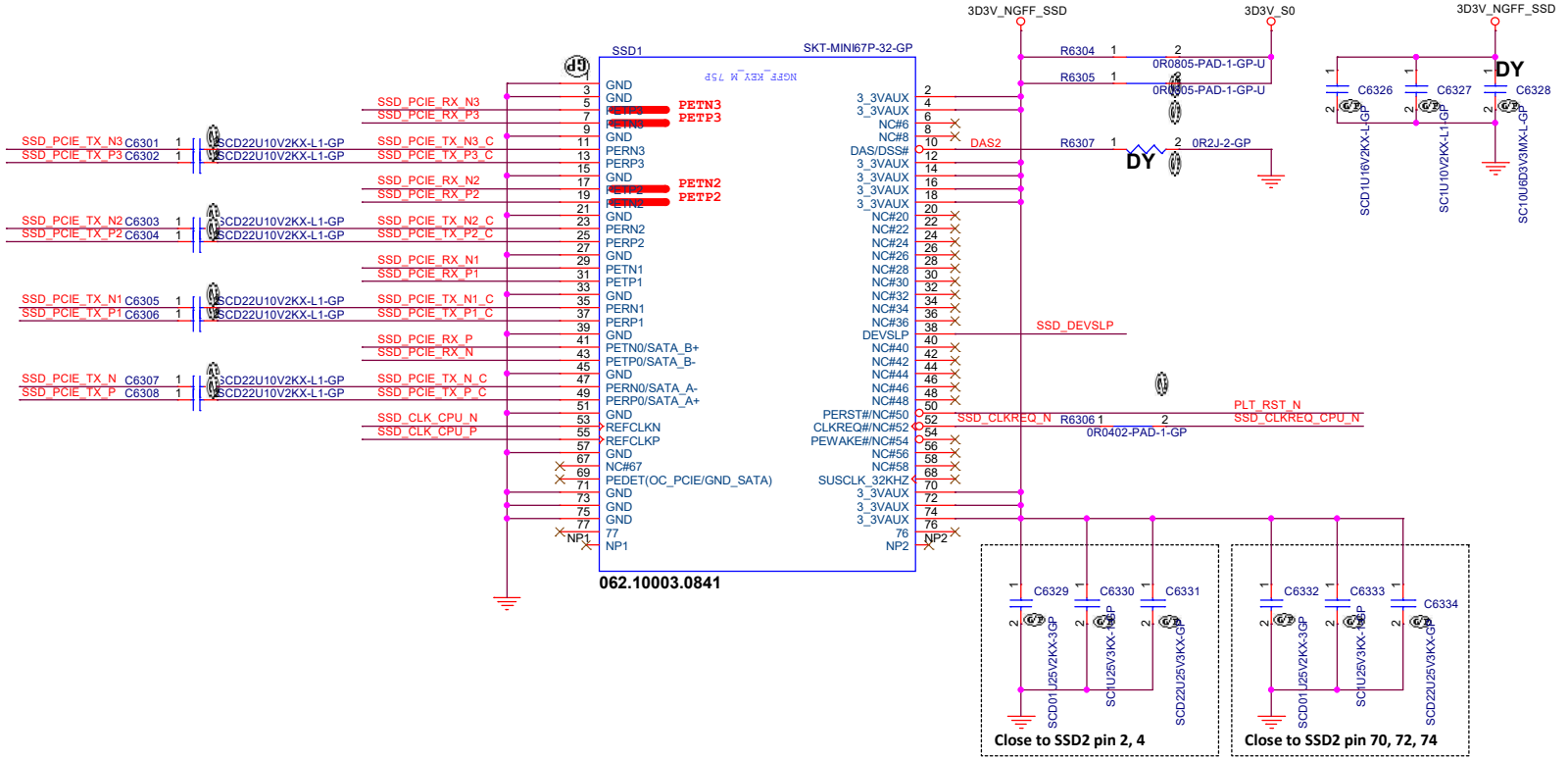
16 SSD_PCIE_RX_N1
16 SSD_PCIE_RX_P1
16 SSD_PCIE_TX_N1
16 SSD_PCIE_TX_P1

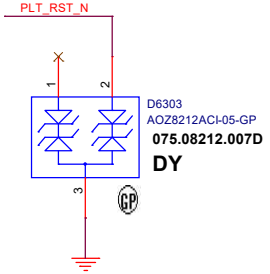
16 SSD_PCIE_RX_N
16 SSD_PCIE_RX_P
16 SSD_PCIE_TX_N
16 SSD_PCIE_TX_P

18 SSD_CLK_CPU_N
18 SSD_CLK_CPU_P
18 SSD_CLKREQ_CPU_N

17,26,61,66,76 PLT_RST_N

16 SSD_DEVSLP





close to SSD1
main: 075.08212.007D AOS
2nd: 075.52215.007D NXP
3rd: 75.05125.07D Amazing

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Title: INT IO (SSD M.2/eMMC)

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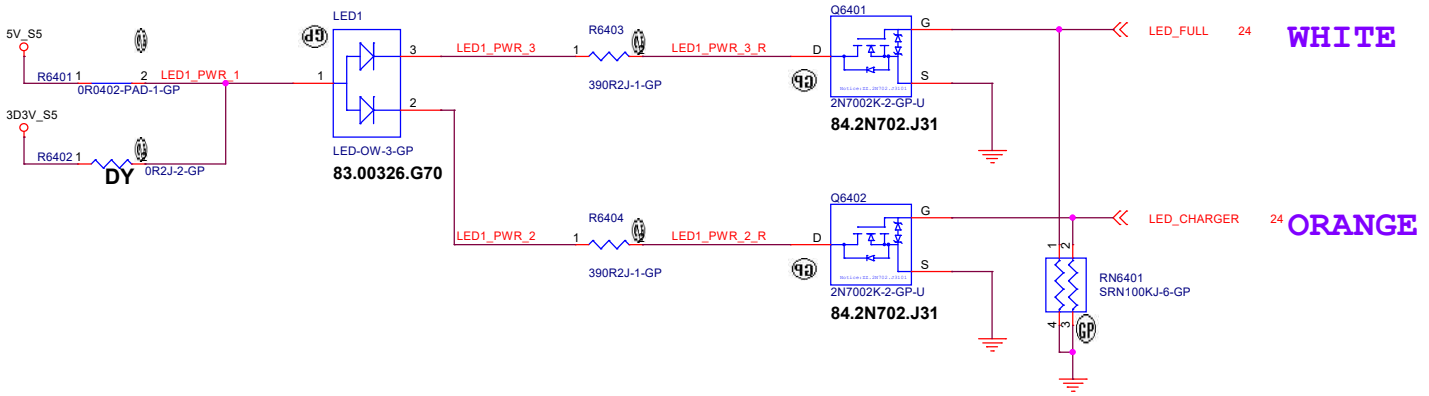
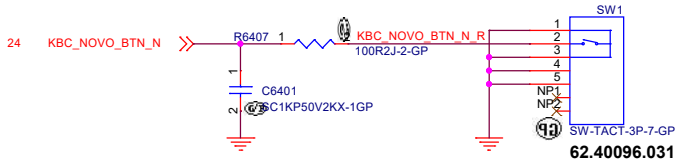
LED

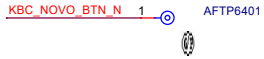
DC-IN

Charger LED



NOVO BUTTON





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Title: LED/NOVO BUTTON		
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24 KCOL[17:0]

24 KROW[7:0]

CLOSE keyboard connector

KB CONN for 14T

KB1

ACES-CON34-5-GP

020.K0013.0034

LC56_14T

KB CONN for 15T

KB2

ACES-CON34-5-GP

020.K0013.0034

LC56_15T

Q6502 2N7002K-2-GP-U 84.2N702.J31

Q6501 2N7002K-2-GP-U 84.2N702.J31

Q6504 FUA138KA-GP 084.00138.0A31

Follow LS1511A

I2C Port3

Follow Raichu

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

TPAD CONN

TPAD1

HRS-CON8-1G-GP

020.K0376.0008

TOP side

KBD BL CONN FOR 14T

KBBL1

ACES-CON4-83-GP

020.K0206.0004

LC56_14T

KBD BL CONN FOR 15T

KBBL2

ACES-CON4-83-GP

020.K0206.0004

LC56_15T

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Title: INT IO (KB/TP)

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USB3.0 Port1

16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P

36 USB1_USB20_AOU_N
36 USB1_USB20_AOU_P

USB3.0 Port2

16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P

16 USB2_USB20_N
16 USB2_USB20_P

CARD

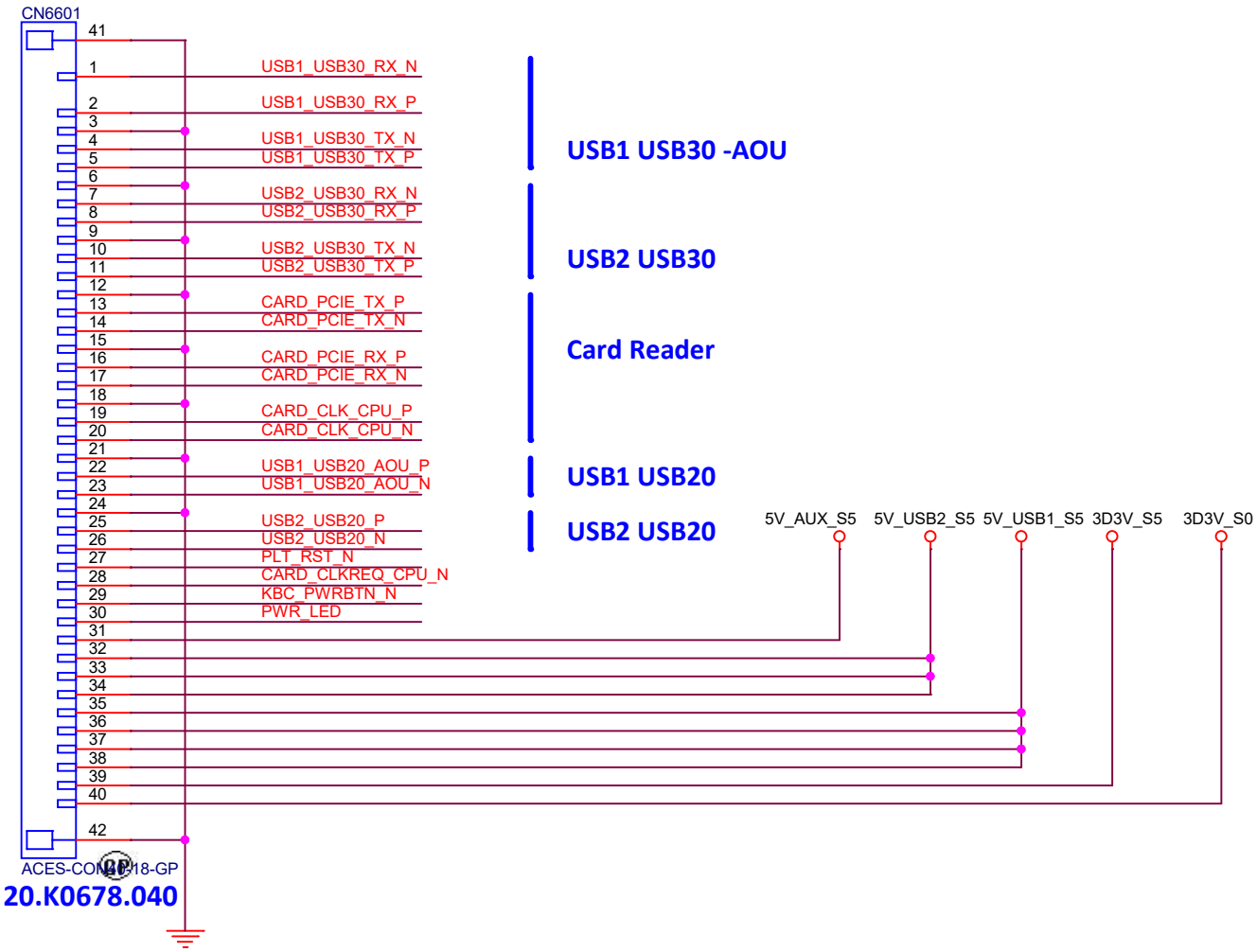
16 CARD_PCIE_RX_N
16 CARD_PCIE_RX_P
16 CARD_PCIE_TX_N
16 CARD_PCIE_TX_P

18 CARD_CLK_CPU_P
18 CARD_CLK_CPU_N
18 CARD_CLKREQ_CPU_N

Others

17,26,61,63,76 PLT_RST_N
24 KBC_PWRBTN_N
24 PWR_LED

MB to IO Board



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Title: ***IO BOARD CONN***

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C560

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Title ***SENSOR (RSVD)(HALL-SENSOR)***

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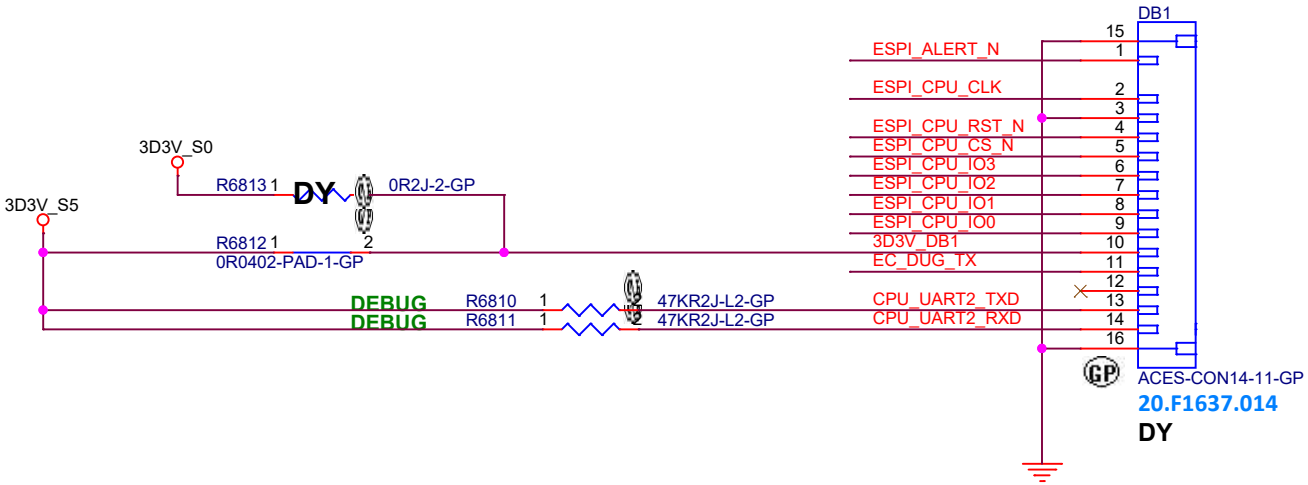
20 CPU_UART2_TXD
20 CPU_UART2_RXD
24 ESPI_ALERT_N
18,24 ESPI_CPU_CLK

18,24 ESPI_CPU_RST_N

24 EC_DUG_TX

18,24 ESPI_CPU_CS_N
18,24 ESPI_CPU_IO3
18,24 ESPI_CPU_IO2
18,24 ESPI_CPU_IO1
18,24 ESPI_CPU_IO0



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Title: ***DEBUG (ESPI DEBUG)***

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Title: ***SENSOR (RSVD)***

Size	Document Number	Rev
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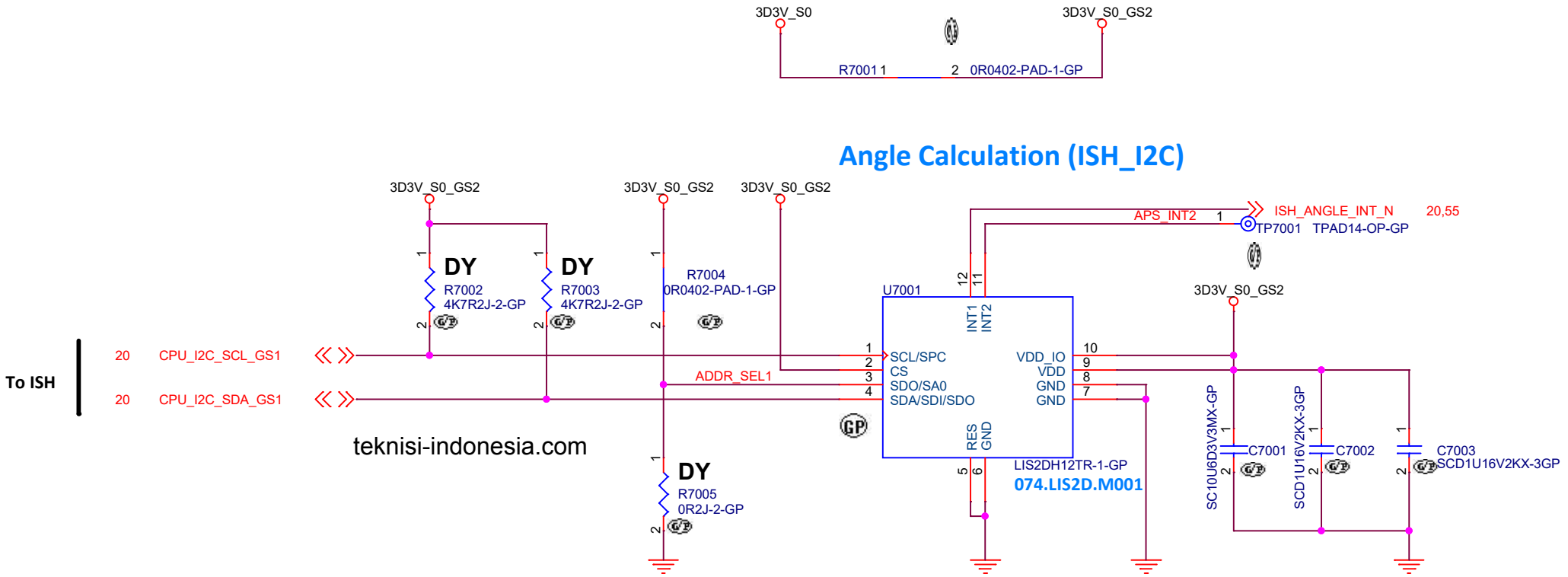

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address
LIS2DH12TR	H L	32h(W) & 33h(R) 30h(W) & 31h(R)

← Logic

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001

C560

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Title: **SENSOR (G-SENSOR)**

Size	Document Number	Rev
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *EXT IO (RSVD)*

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USB Port3, Type C_USB3.0, PD

KBC and PD communication

24 EC_SMB_SCL_PD
24 EC_SMB_SDA_PD
24 PD_INT1_EC

3,24,44,46 PROCHOT_CPU_N
16 CPU_SMB_SDA_P1
16 CPU_SMB_SCL_P1
17 CPU_SMB_ALERT_PCH_N

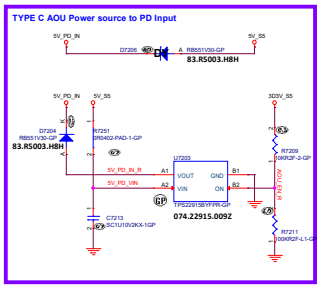
KBC Control VBUS Power to System

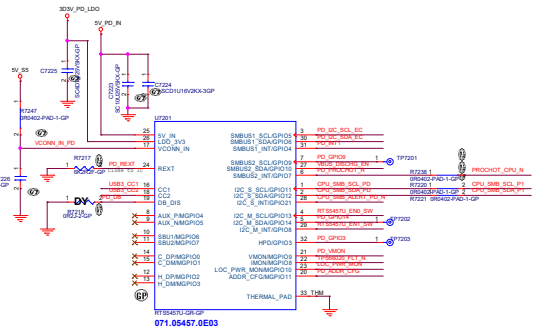
24,44 PWR_TYPECIN_OK

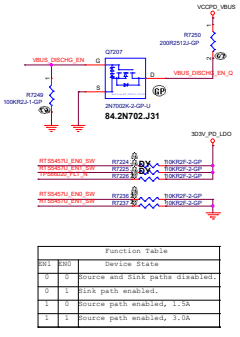
To TYPEC Connector

73 USB3_CC1
73 USB3_CC2

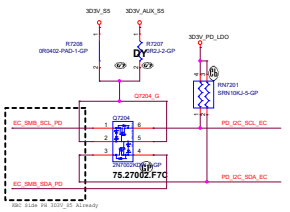
TYPE C AOU Power source to PD Input

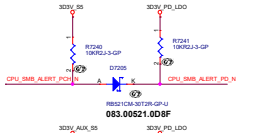


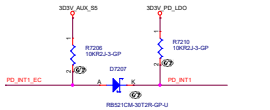


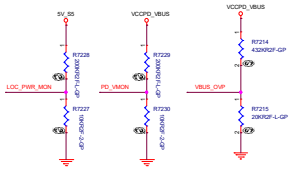


Function Table		
EN1	EN0	Device State
0	0	Source and Sink paths disabled.
0	1	Sink path enabled.
1	0	Source path enabled, 1.5A
1	1	Source path enabled, 3.0A









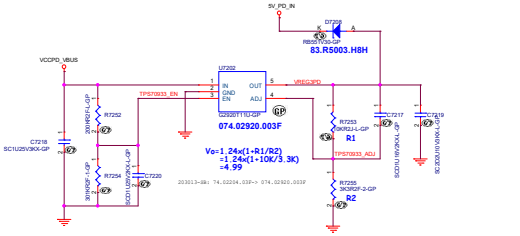
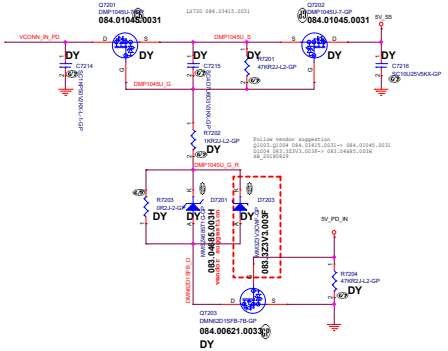
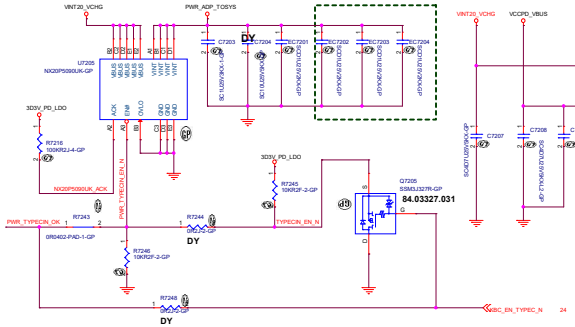
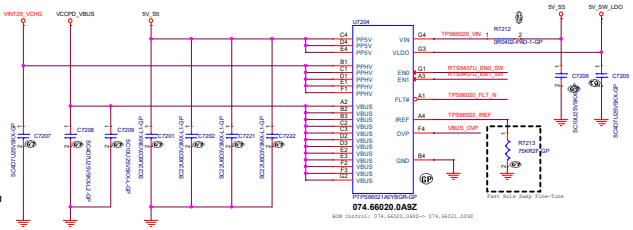


TABLE U7202

Vender	Vender P/N	Wistron P/N
GMT	G2920T11U	074.02920.003F
DIODES	AP2205-WS-7	074.02205.000F







Slave Addr	PULL-HIGH RESISTOR (R7231)	PULL-LOW RESISTOR (R7232)	VOLTAGE
addr0: 0xC4	NC	10.0K	>= 1.8V
addr1: 0xC6	75K	10.0K	>= 0.2V && < 0.6V
addr2: 0xC8	33.0K	10.0K	>= 0.6V && < 1.0V
addr3: 0xCa	10.0K	10.0K	>= 1.0V

It's is used for SMBUS slave addr0/1/2/3 setting during power on initialization.

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Size: B	Document Number: C560-TGL		Rev: -1
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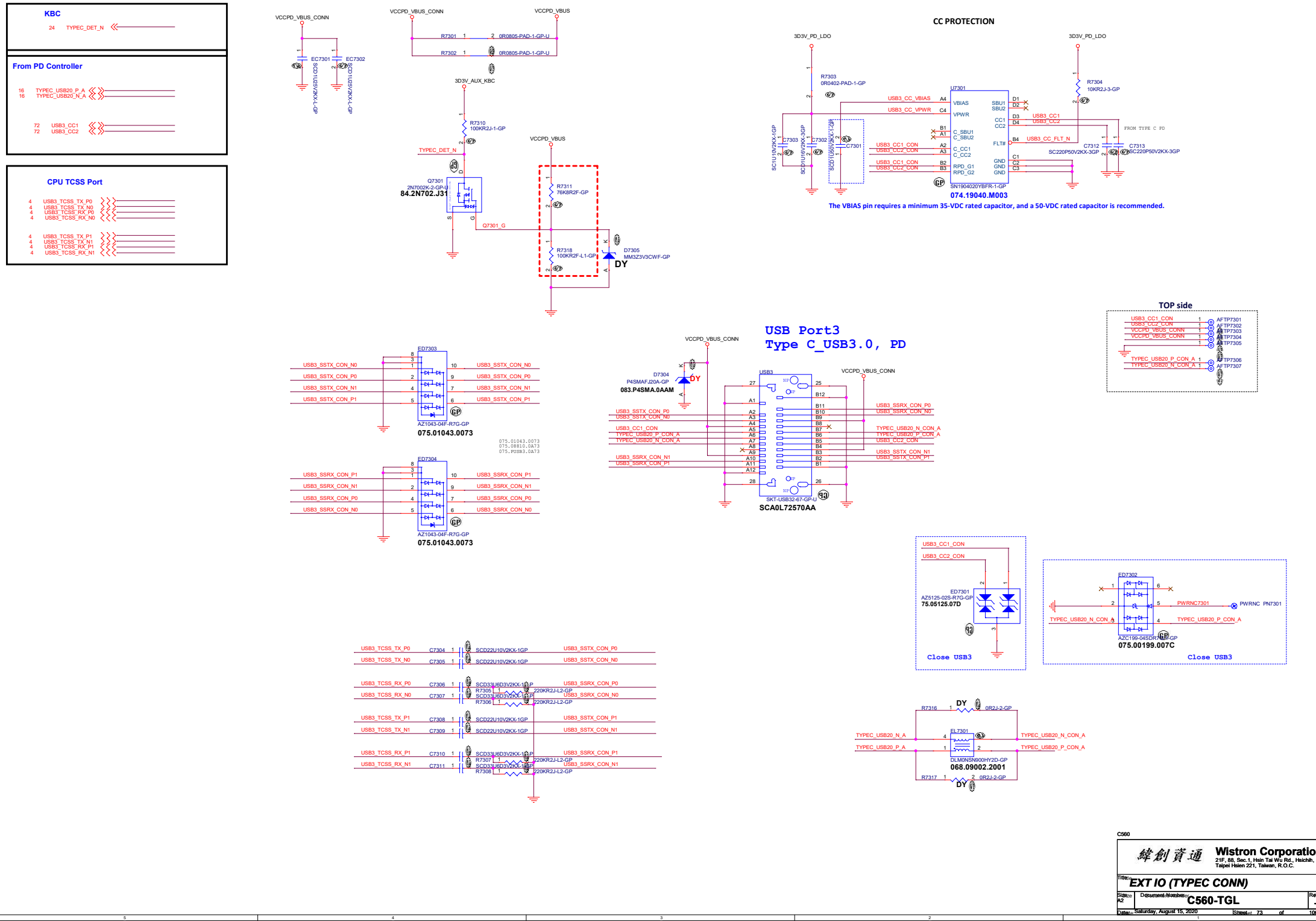

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▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.

18 PEG_CLKREQ_CPU_N
18 DGPU_HOLD_RST_N
17,26,61,63,66 PLT_RST_N
79 SYS_PEX_RST_MON_N

EMI Reserved
GPU_PEX_RST_N
EC7601 SC33P50V2JN-3GP DY

dGPU Reset
U7601 DIS 74LVC1G08GW-1-GP
DGPU_HOLD_RST_N
PLT_RST_N
SYS_PEX_RST_MON_N
R7607 10KR1J-GP DIS
R7606 100KR1J-GP DIS
1D8V_AON_S0
73.01G08.L04
2nd = 73.7SZ08.DAH

1D8V_VGA_S0
1D8V_AON_S0
R7603 10KR2J-3-GP DIS
Q7601 PJA138KA-GP DIS
084.00138.0A31
2nd = 084.00138.0C31
PEG_CLKREQ_CPU_N
SYS_PEX_RST_MON_N
GFX_CLKREQ_dGPU_N
R7613 0R0402-PAD-1-GP
GPU_PEX_RST_N

GPU1A 1 OF 14
1/14 PCI_EXPRESS
PEX_WAKE# AA14
PEX_RST# AC7
PEX_CLKREQ# AC6
PEX_REFCLK AE8
PEX_REFCLK* AD8
PEG_CLK_CPU_P
PEG_CLK_CPU_N
PCIE/PLL DIGITAL PWR
PEX_CVDD AA22
PEX_DVDD_2 AB23
PEX_DVDD_3 AC24
PEX_DVDD_4 AD25
PEX_DVDD_5 AE26
PEX_DVDD_6 AE27
1V Interface
PCIE/PLL ANALOG PWR
PEX_HVDD_2 AA10
PEX_HVDD_3 AA12
PEX_HVDD_4 AA13
PEX_HVDD_5 AA16
PEX_HVDD_6 AA18
PEX_HVDD_7 AA19
PEX_HVDD_8 AA20
PEX_HVDD_9 AA21
PEX_HVDD_10 AB22
PEX_HVDD_11 AC23
PEX_HVDD_12 AD24
PEX_HVDD_13 AE25
PEX_HVDD_14 AF26
AF27
1.8V Interface
PEX_PLL_HVDD_1 AA8
PEX_PLL_HVDD_2 AA9
PEX_TERMP AF25 PEX_TERMP 1 R7601 2K49R2F-GP DIS
N18S-G5-A1-GP

PEX_TX0 PEX_TX0* PEX_RX0 PEX_RX0* PEX_TX1 PEX_TX1* PEX_RX1 PEX_RX1* PEX_TX2 PEX_TX2* PEX_RX2 PEX_RX2* PEX_TX3 PEX_TX3* PEX_RX3 PEX_RX3*
PEX_TX4 PEX_TX4* PEX_RX4 PEX_RX4* PEX_TX5 PEX_TX5* PEX_RX5 PEX_RX5* PEX_TX6 PEX_TX6* PEX_RX6 PEX_RX6* PEX_TX7 PEX_TX7* PEX_RX7 PEX_RX7* PEX_TX8 PEX_TX8* PEX_RX8 PEX_RX8* PEX_TX9 PEX_TX9* PEX_RX9 PEX_RX9* PEX_TX10 PEX_TX10* PEX_RX10 PEX_RX10* PEX_TX11 PEX_TX11* PEX_RX11 PEX_RX11* PEX_TX12 PEX_TX12* PEX_RX12 PEX_RX12* PEX_TX13 PEX_TX13* PEX_RX13 PEX_RX13* PEX_TX14 PEX_TX14* PEX_RX14 PEX_RX14* PEX_TX15 PEX_TX15* PEX_RX15 PEX_RX15*
DIS
PEX LANES 15 - 4 ARE DEFEATURED

GFX_PCIE_RX_P0 GFX_PCIE_RX_N0 GFX_PCIE_TX_P0 GFX_PCIE_TX_N0 GFX_PCIE_RX_P1 GFX_PCIE_RX_N1 GFX_PCIE_TX_P1 GFX_PCIE_TX_N1 GFX_PCIE_RX_P2 GFX_PCIE_RX_N2 GFX_PCIE_TX_P2 GFX_PCIE_TX_N2 GFX_PCIE_RX_P3 GFX_PCIE_RX_N3 GFX_PCIE_TX_P3 GFX_PCIE_TX_N3
C7601 C7602 C7603 C7604 C7605 C7606 C7607 C7608 C7609 C7610 C7611 C7612 C7613 C7614 C7615 C7616
SCD22U10V2KX-L1-GP
GFX_PCIE_RX_P0_C GFX_PCIE_RX_N0_C GFX_PCIE_TX_P0_C GFX_PCIE_TX_N0_C GFX_PCIE_RX_P1_C GFX_PCIE_RX_N1_C GFX_PCIE_TX_P1_C GFX_PCIE_TX_N1_C GFX_PCIE_RX_P2_C GFX_PCIE_RX_N2_C GFX_PCIE_TX_P2_C GFX_PCIE_TX_N2_C GFX_PCIE_RX_P3_C GFX_PCIE_RX_N3_C GFX_PCIE_TX_P3_C GFX_PCIE_TX_N3_C

1U 0201*6 X6S
Place under GPU
C7627 C7628 C7629 C7630 C7631 C7632 DIS SC1UF6V3MX-GP

4.7U 0603*3 X6S
Place under GPU
C7633 C7634 C7635 DY SC4D7UF6D3V6KX-L-GP

10U 0805*3 X6S
Place near GPU
C7650 C7624 C7623 DIS SC10UF6V5KX-GP

22U 0603*2 X6S
Place near GPU
C7636 C7637 DIS SC22UF6D3V3MX-1-GP

1U 0201*7 X6S
Place under GPU
C7638 C7639 C7640 C7641 C7642 C7643 C7652 DIS SC1UF6V3MX-GP

4.7U 0603*3 X6S
Place under GPU
C7645 C7646 C7647 DY SC4D7UF6D3V3KX-L-GP

10U 0603*3 X6S
Place near GPU
C7648 C7649 C7651 DIS SC10UF6D3V5MX-GP

22U 0603*2 X6S
Place near GPU
C7660 C7661 DIS SC22UF6D3V3MX-1-GP

1U 0201*1 X6S
Place under GPU
C7644 DIS SC1UF6V3MX-GP

1D0V_VGA_S0
1D8V_VGA_S0

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Title: GPU (PEG 1/5)
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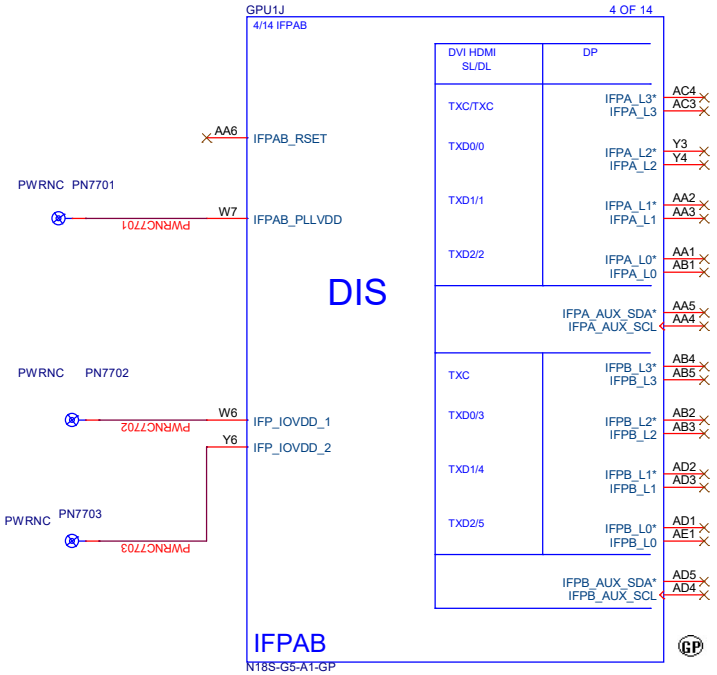
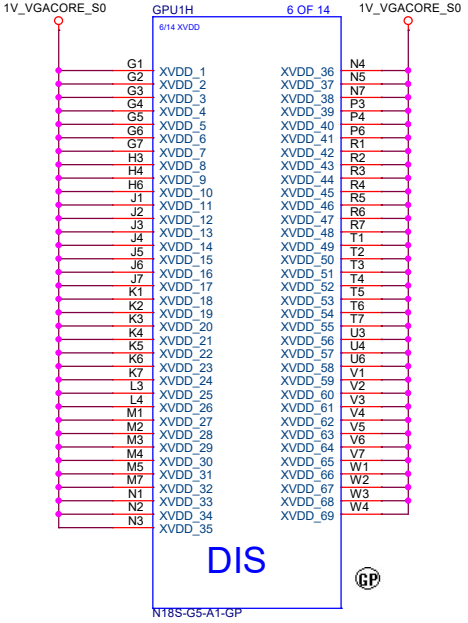
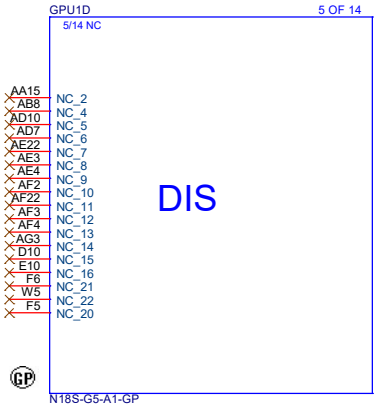
Main Func = dGPU







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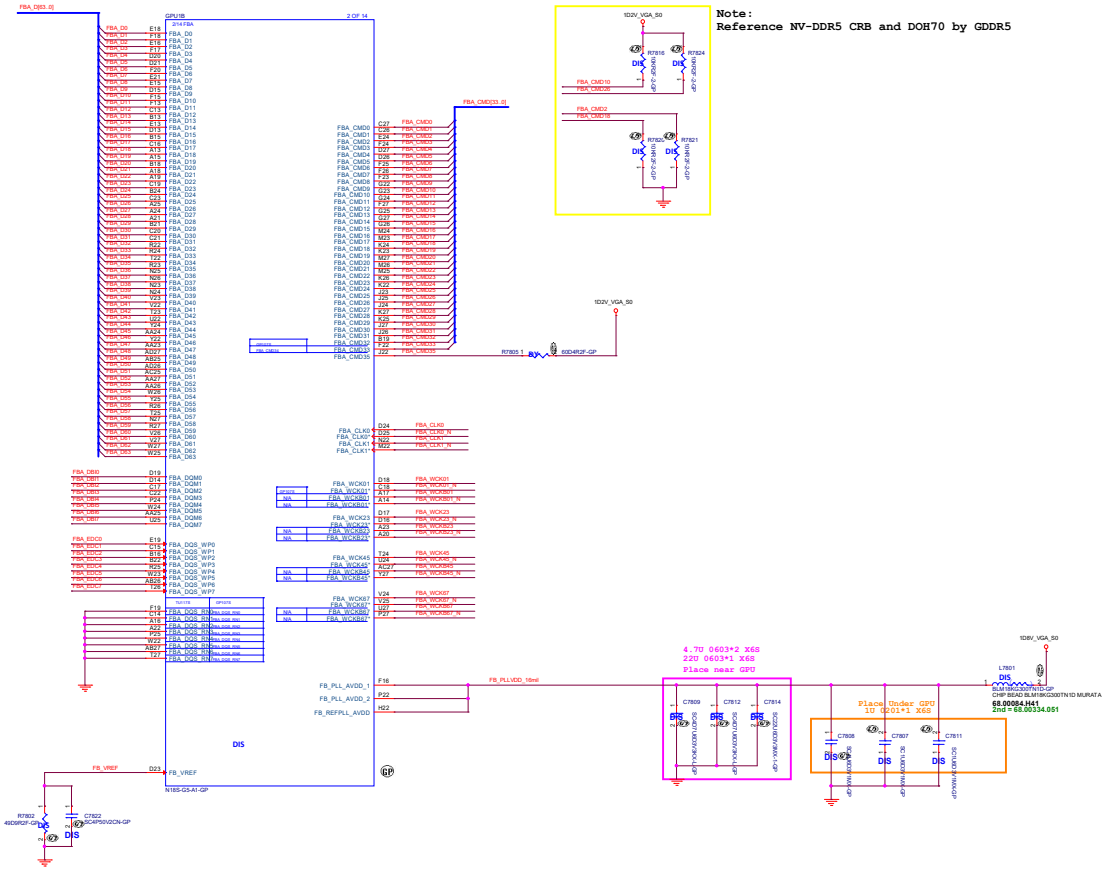
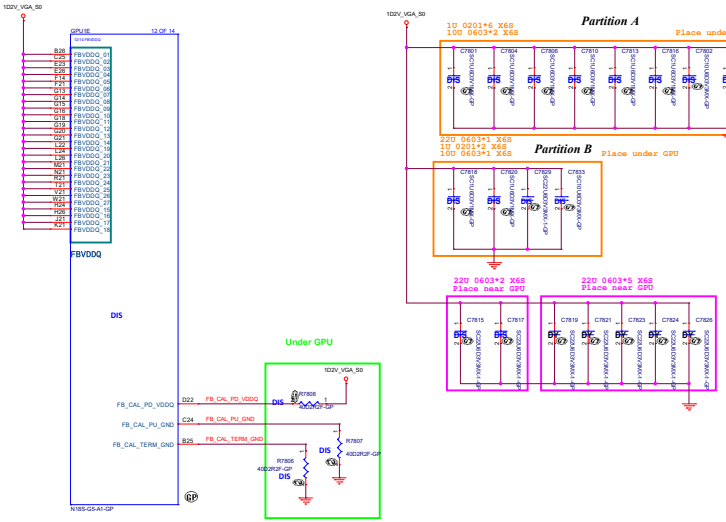
Group A

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5





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Title: GPU (VRAM 3/5)

Size	Document Number	Rev
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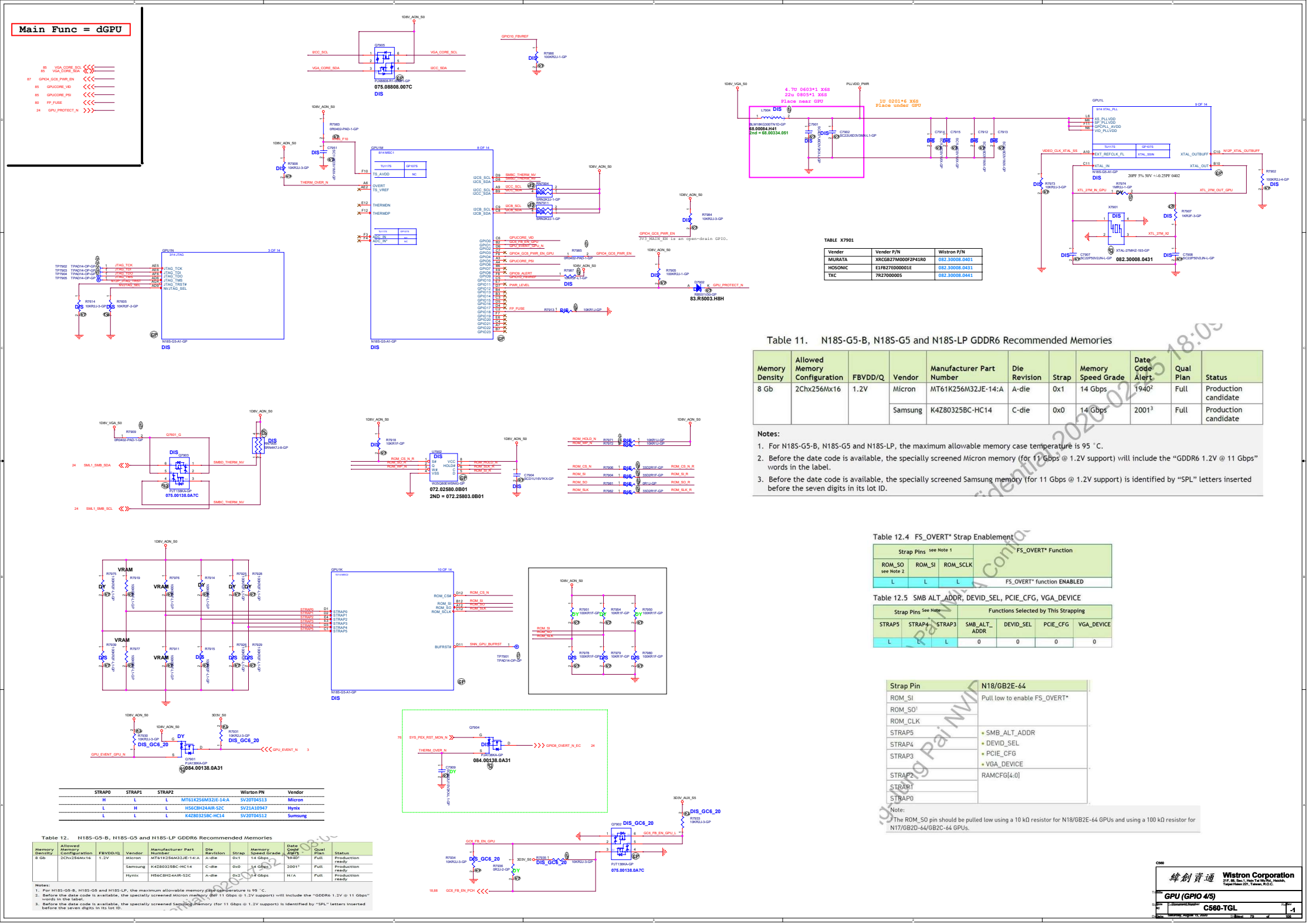
Main Func = dGPU
VGA_CORE_SCL
VGA_CORE_SDA
GPIO4_GC6_PWR_EN
GPUCORE_VID
GPUCORE_PSI
FP_FUSE
GPU_PROTECT_N
075.08808.007C
DIS
4.7U 0603*1 X6S
22u 0805*1 X6S
Place near GPU
1U 0201*6 X6S
Place under GPU
68.00084.H41
2nd = 68.00334.051
TABLE X7901
Vender
Vender P/N
Wistron P/N
MURATA
XRCGB27M000F2P41R0
082.30008.0401
HOSONIC
E1FB27E000001E
082.30008.0431
TXC
7R27000005
082.30008.0441
082.30008.0431
83.R5003.H8H
072.02580.0B01
2ND = 072.25803.0B01
075.00138.0A7C
084.00138.0A31
VRAM
Table 11. N18S-G5-B, N18S-G5 and N18S-LP GDDR6 Recommended Memories
Memory Density
Allowed Memory Configuration
FBVDD/Q
Vendor
Manufacturer Part Number
Die Revision
Strap
Memory Speed Grade
Date Code Alert
Qual Plan
Status
8 Gb
2Chx256Mx16
1.2V
Micron
MT61K256M32JE-14:A
A-die
0x1
14 Gbps
1940[2]
Full
Production candidate
Samsung
K4Z80325BC-HC14
C-die
0x0
14 Gbps
2001[3]
Full
Production candidate
Notes:
1. For N18S-G5-B, N18S-G5 and N18S-LP, the maximum allowable memory case temperature is 95 °C.
2. Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
3. Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.
Table 12.4 FS_OVERT* Strap Enablement
Strap Pins see Note 1
ROM_SO see Note 2
ROM_SI
ROM_SCLK
FS_OVERT* Function
L
L
L
FS_OVERT* function ENABLED
Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE
Strap Pins See Note
STRAP5
STRAP4
STRAP3
Functions Selected by This Strapping
SMB_ALT_ADDR
DEVID_SEL
PCIE_CFG
VGA_DEVICE
0
Strap Pin
N18/GB2E-64
ROM_SI
ROM_SO[1]
ROM_CLK
STRAP5
STRAP4
STRAP3
STRAP2
STRAP1
STRAP0
Pull low to enable FS_OVERT*
• SMB_ALT_ADDR
• DEVID_SEL
• PCIE_CFG
• VGA_DEVICE
RAMCFG[4:0]
Note:
1. The ROM_SO pin should be pulled low using a 10 kΩ resistor for N18/GB2E-64 GPUs and using a 100 kΩ resistor for N17/GB2D-64/GB2C-64 GPUs.
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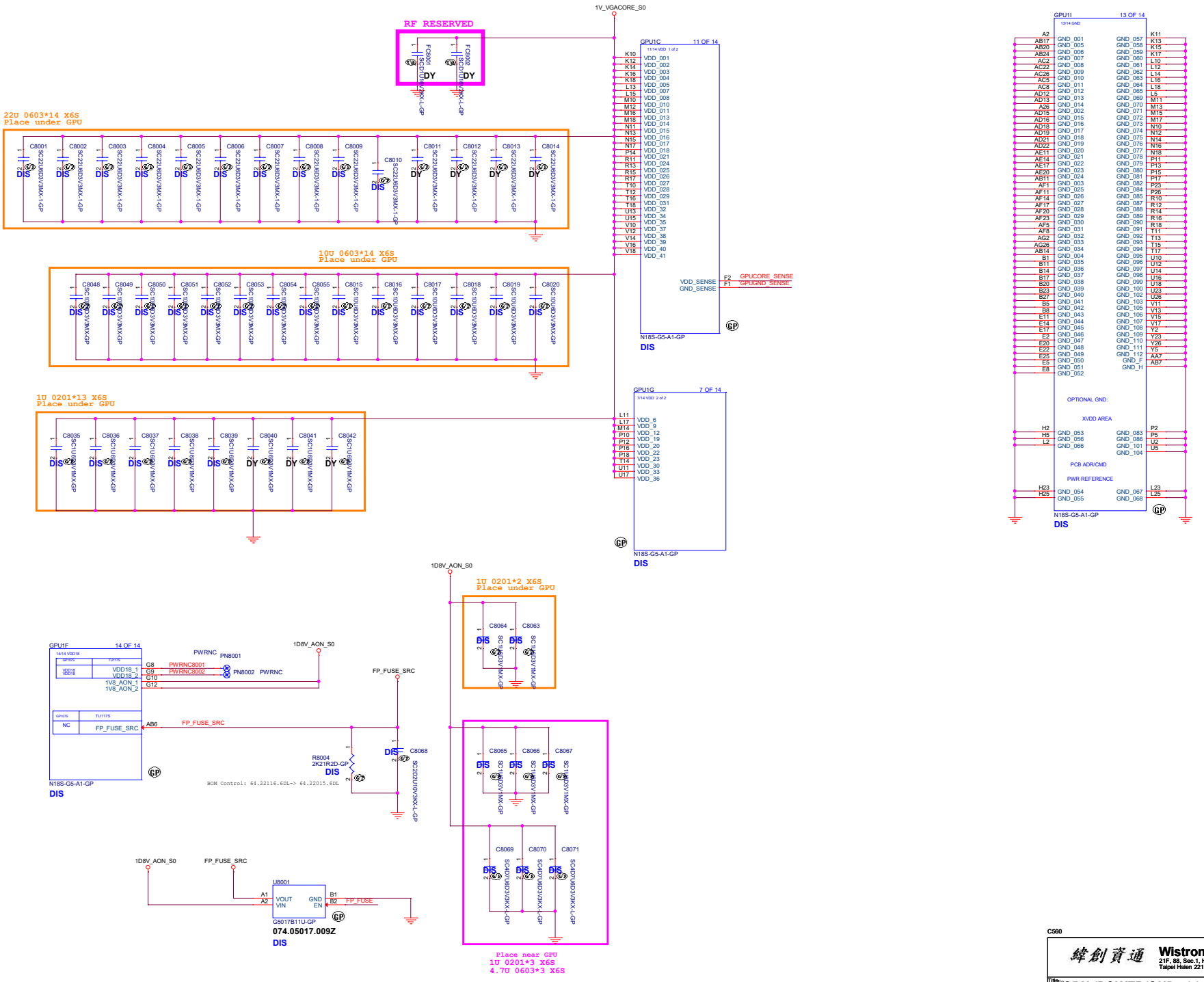
GPU (GPIO 4/5)
C560-TGL
-1

Main Func = GPU

79 FP_FUSE

85 GPUCORE_SENSE

85 GPUGND_SENSE



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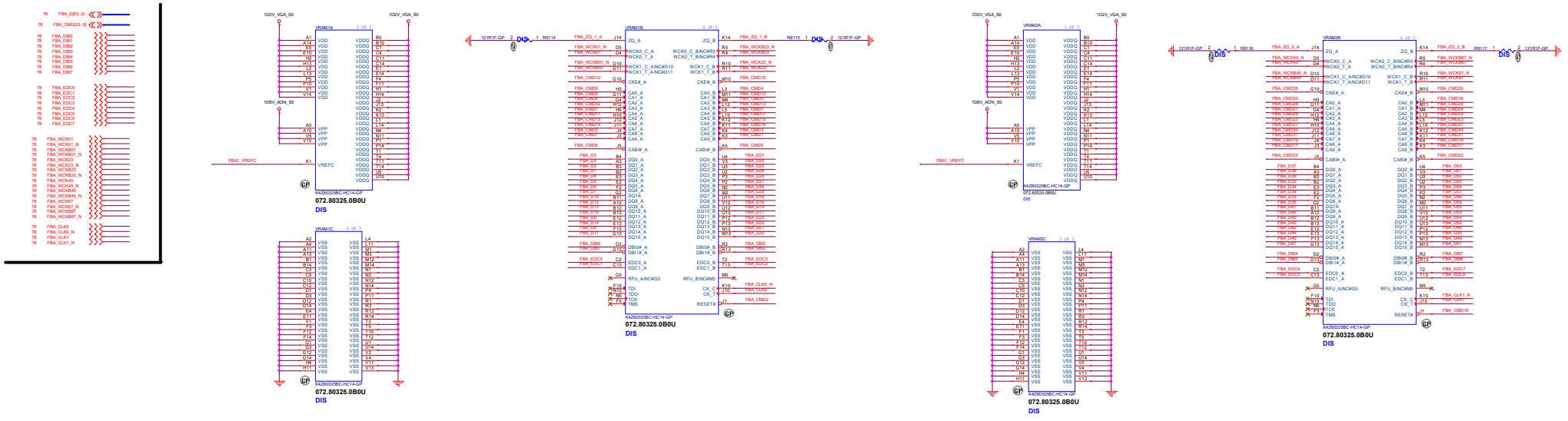


8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

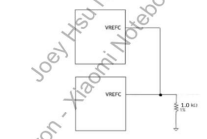
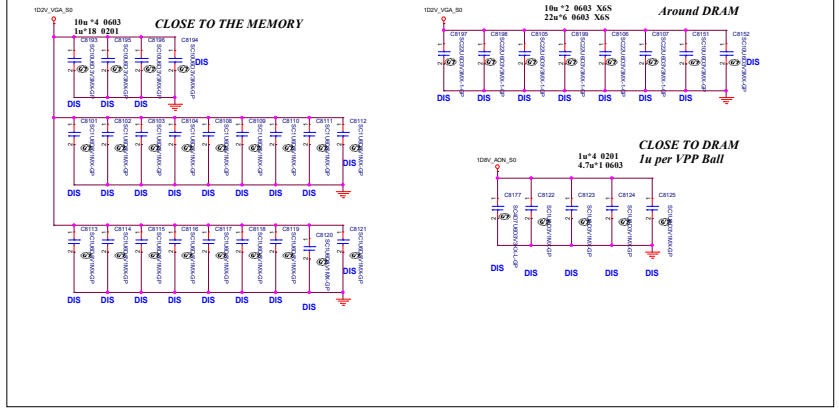
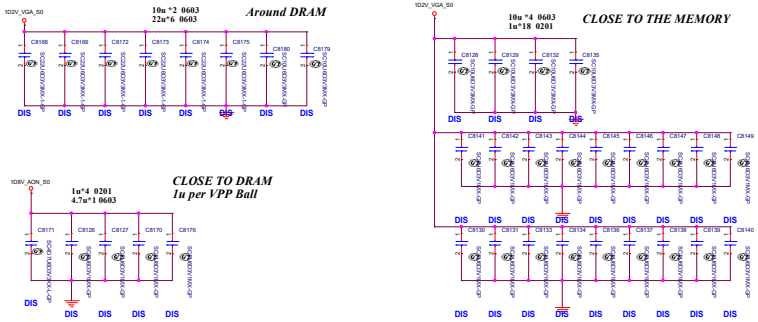


Figure 8.8 Use of Integrated VREFC for ×16 Mode





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Title: *GPU (RSVD)*

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Title: *GPU (RSVD)*

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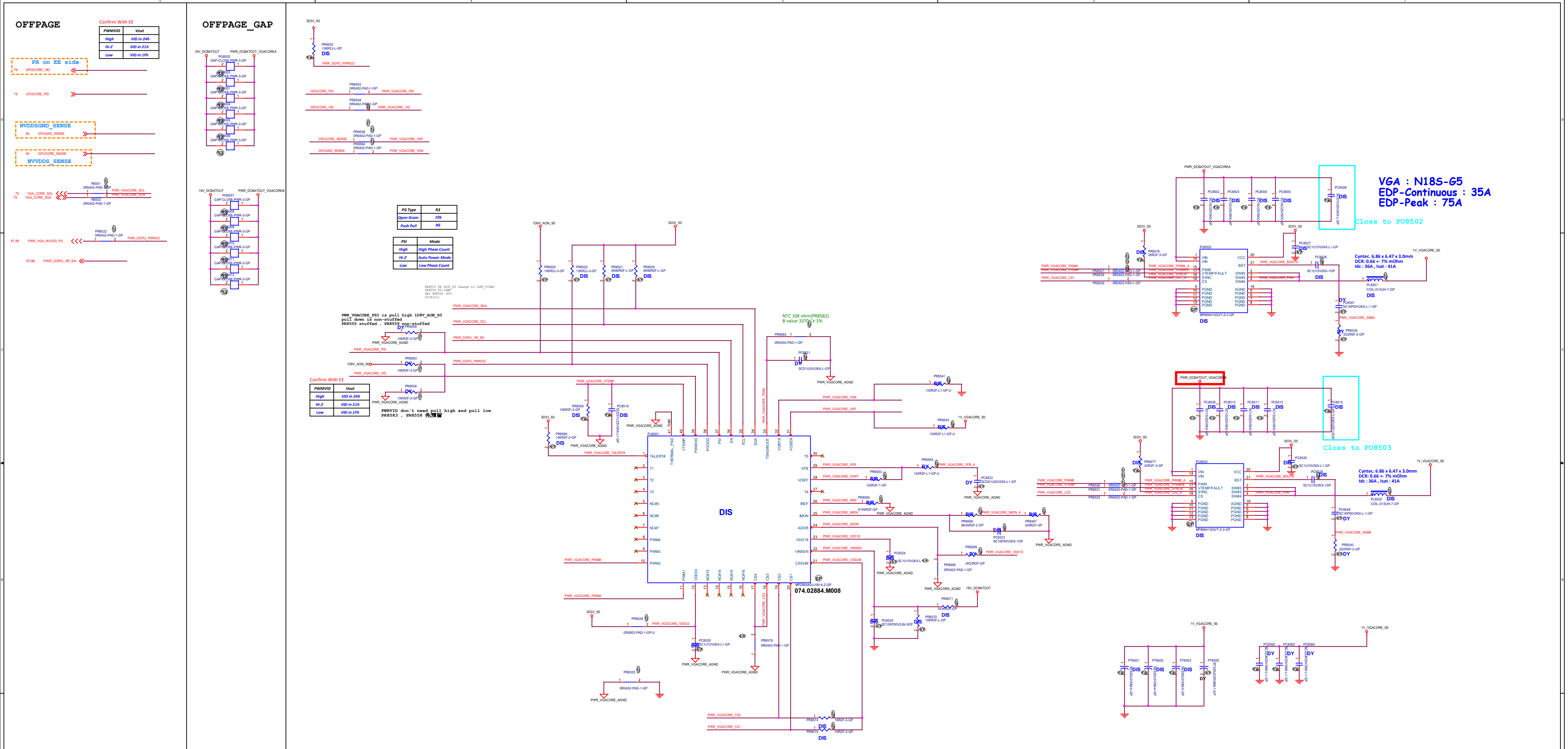

Confirm With EE

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh

PG Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

	N17 P-G0	N17 P-G1	N17 E-G1	Power Phase	Mosfet (per phase)	CAP
NVVDD	40	47	62	P-G0/G1 : 3 E-G1 : 3	P-G0/G1 : 2 (Low cost) E-G1 : 2	P-G0/G1 : 470uF x 4 E-G1 : 470uF x 4 + 330uF(H1.4) x 2 - Pluto 470uF x 4 + 470uF x 2 - Neptune
NVVDD – Peak	85	90	164			
NVVDDS	16	19	21	P-G0/G1 : 2 E-G1 : 2	P-G0/G1 : 1 E-G1 : 2	P-G0/G1 : 470uF x 2 E-G1 : 470uF x 2
NVVDDS – Peak	35	42	49			
FB Total	11+6.2	11+6.2	25+6.2	P-G0/G1 : 1 E-G1 : 1	P-G0/G1 : 1 E-G1 : 2	P-G0/G1 : 330uF x 2 E-G1 : 470uF x 2

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Title	GPU (MP2884_VGA)		
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OFFPAGE

PH on EE Side

88 1D2V_PGOOD — PR8674 — 1PWR_VRAM_PG — 0R0402-PAD-1-GP

88 DGPU_PWR_EN — PR8677 — 1PWR_DGPU1D8V_EN — 0R0402-PAD-1-GP

88 PWR_VRAM_EN

PH on EE Side

87,88 1V_VGA_S0_PG — PR8675 — 1PWR_DGPU1D0V_PG — 0R0402-PAD-1-GP

87,88 1V_VGA_EN_R — PR8676 — 1PWR_DGPU1D0V_EN — 0R0402-PAD-1-GP

OFFPAGE_GAP

1D2V_VGA_S0 — PWR_VRAM

PG8603 GAP-CLOSE-PWR-3-GP
PG8605 GAP-CLOSE-PWR-3-GP
PG8606 GAP-CLOSE-PWR-3-GP
PG8607 GAP-CLOSE-PWR-3-GP
PG8608 GAP-CLOSE-PWR-3-GP
PG8609 GAP-CLOSE-PWR-3-GP
PG8610 GAP-CLOSE-PWR-3-GP

1D2V_VGA_S0 — PWR_VRAM

PG8613 GAP-CLOSE-PWR-3-GP
PG8614 GAP-CLOSE-PWR-3-GP
PG8615 GAP-CLOSE-PWR-3-GP
PG8616 GAP-CLOSE-PWR-3-GP
PG8617 GAP-CLOSE-PWR-3-GP
PG8618 GAP-CLOSE-PWR-3-GP
PG8619 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_DGPU1D8V_VIN

PG8652 GAP-CLOSE-PWR-3-GP
PG8653 GAP-CLOSE-PWR-3-GP

1D8V_AON_S0 — PWR_DGPU1D8V

PG8654 GAP-CLOSE-PWR-3-GP
PG8655 GAP-CLOSE-PWR-3-GP
PG8651 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_DGPU1D0V_VIN

PG8671 GAP-CLOSE-PWR-3-GP
PG8672 GAP-CLOSE-PWR-3-GP

1D0V_VGA_S0 — PWR_DGPU1D0V

PG8673 GAP-CLOSE-PWR-3-GP
PG8674 GAP-CLOSE-PWR-3-GP
PG8675 GAP-CLOSE-PWR-3-GP

MLCCs must placed symmetrically on TOP and BOTTOM side

3D3V_S5 — PR8610 100KR2F-L3-GP — PWR_VRAM_PG

PWR_VRAM_AGND — PC8602 SC1U25V2KX-2-GP (DY)

PR8606 100KR2F-L3-GP (DIS)

PR8609 0R0603-PAD-1-GP-U — PWR_VRAM_BOOT_A — PC8608 SCD1U25V2KX-L-GP (DIS)

PWR_VRAM_PG

PU8601 (PWR_VRAM_MODE, PWR_VRAM_PG, PWR_VRAM_BOOT)

PWR_VRAM_VREF — PR8611 24KR2F-GP (DIS) — PC8609 SC1U10V2KX-L1-GP (DIS)

PWR_VRAM_REFIN — PR8615 40KR2F-GP (DIS) — PC8612 SC1U10V2KX-L1-GP (DIS)

PC8615 SCD01U25V2KX-L1-GP (DY) — PR8617 39KR2F-GP (DIS) — PC8616 SC1U10V2KX-L1-GP (DIS)

PWR_VRAM_AGND

PWR_VRAM_VSNS

PWR_VRAM_GSNS — PR8624 0R2J-2-GP (DIS)

PG8601 GAP-CLOSE-PWR-3-GP

PWR_VRAM_AGND

PU8602 FDMS3600-02-RJK0215-COLAY-GP (1st = 075.36354.0073) (DIS)

PWR_VRAM_PH
PWR_VRAM_HG
PWR_VRAM_LG
PWR_VRAM_VS

TPS51219RTER-1-GP

PR8613 0R0402-PAD-1-GP — 05V_S5

PC8611 SC2D2U10V3KX-L-GP (DIS)

PC8617 SCD01U25V2KX-L1-GP (DIS)

PR8620 10R2F-L1-GP (DIS)

PWR_VRAM_COMP_A — PC8618 SC1KP50V2KX-L1-GP (DIS)

1D2V_VGA_S0 — PR8621 10R2J-2-GP-U (DIS)

19V_DCBATOUT

PC8605 SC10U25V6KX-L-GP (DY)
PC8619 SC10U25V6KX-L-GP (DY)
PC8601 SC10U25V6KX-L-GP (DIS)
PC8607 SC10U25V6KX-L-GP (DIS)

Cyntec, 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

PL8601 COIL-1UH-34-GP-U1

VCC1D2V
Max 12A
Peak 13A
PWR_VRAM

PC8610 SC100P50V2JN-L-GP (DY)
PWR_VRAM_3N4LB
PR8619 2D2R5J-L-GP (DY)

PT8601 SP-TS3DU0D0V6MA-1-GP (DIS)
PT8602 SP-TS3DU0D0V6MA-1-GP (DIS)

PR8606	PC8615	PC8617	mode	sw freq
1Kohm	ASM	NO ASM	D_CAP2	500KHz
200Kohm	NO ASM	ASM	D_CAP	400KHz
100Kohm	NO ASM	ASM	D_CAP	300KHz

Select

PWR_DGPU1D8V_VIN — PU8651 RT5797ALGQW-GP — 074.05797.0073

PC8652 SC22U6D3V3MX-L1-GP (DIS)

3D3V_S5 — PR8657 100KR2F-L1-GP (DY)

PWR_DGPU1D8V_PG — PWR_DGPU1D8V_PH — PWR_DGPU1D8V_EN — PWR_DGPU1D8V_FB

TOKO, 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A

PL8651 IND-1UH-382-GP

PR8658 100KR2F-L1-GP (DIS)

PR8656 49K9R2F-L-GP (DIS)

PC8653 SC2D2U6D3V2MX-L1-GP (DY)

PC8654 SC22U6D3V3MX-L1-GP (DIS)

PC8651 SC22U6D3V3MX-L1-GP (DIS)

PWR_DGPU1D8V

TDC=1.6A
Imax= 3A

PWR_DGPU1D8V_EN — PC8655 SC1U10V2KX-L1-GP (DY)

PWR_DGPU1D0V_VIN — PU8671 RT5797ALGQW-GP — 074.05797.0073

PC8671 SC22U6D3V3MX-L1-GP (DIS)

3D3V_S5 — PR8671 100KR2F-L1-GP (DIS)

PWR_DGPU1D0V_PG — PWR_DGPU1D0V_PH — PWR_DGPU1D0V_EN — PWR_DGPU1D0V_FB

TOKO, 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A

PL8671 IND-1UH-382-GP

PR8672 100KR2F-L1-GP (DIS)

PR8673 150KR2F-L-GP (DIS)

PC8673 SC2D2U6D3V2MX-L1-GP (DY)

PC8674 SC22U6D3V3MX-L1-GP (DIS)

PC8675 SC22U6D3V3MX-L1-GP (DIS)

PWR_DGPU1D0V

TDC=1.1A
Imax= 3A

PWR_DGPU1D0V_EN — PC8672 SC1U10V2KX-L1-GP (DY)

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Title: TPS51219/5797_1D2V/1D8V/1D0V

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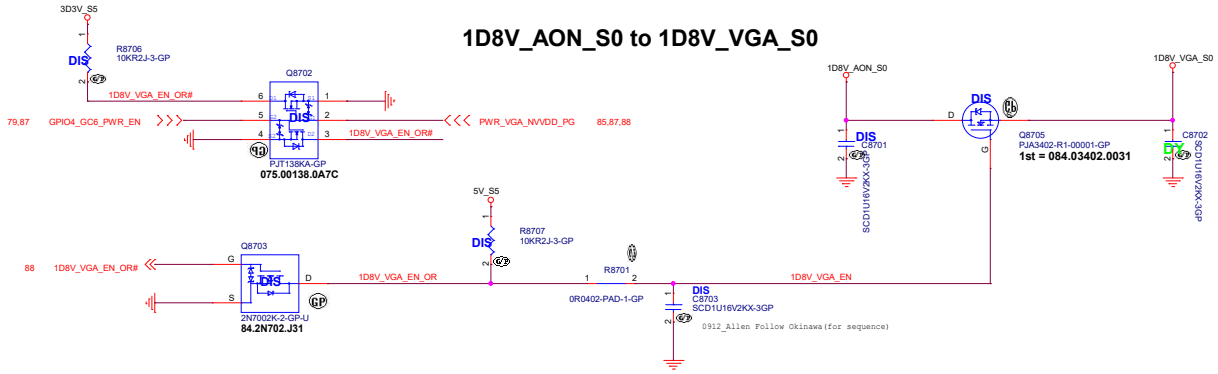

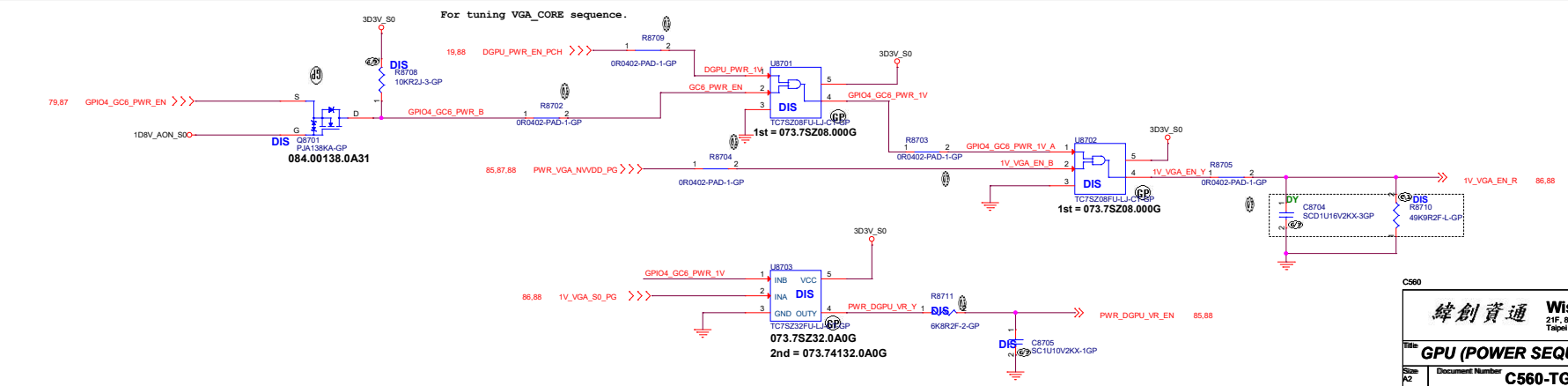

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Title	GPU (POWER SEQUENCE)
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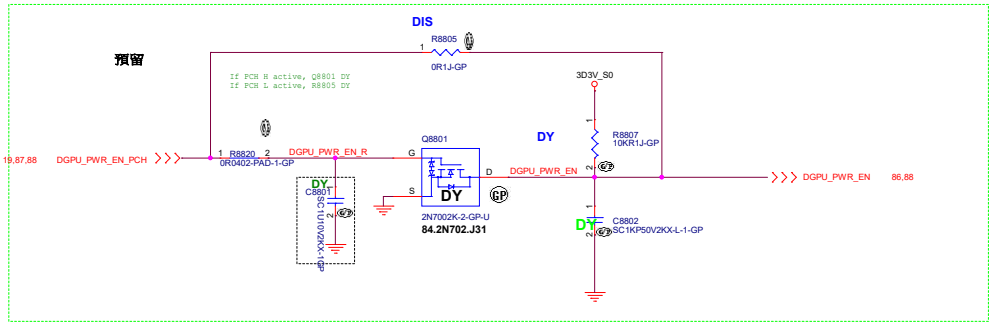

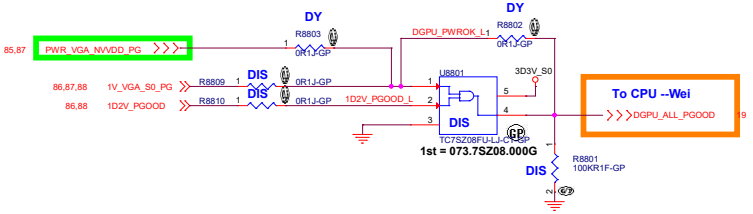

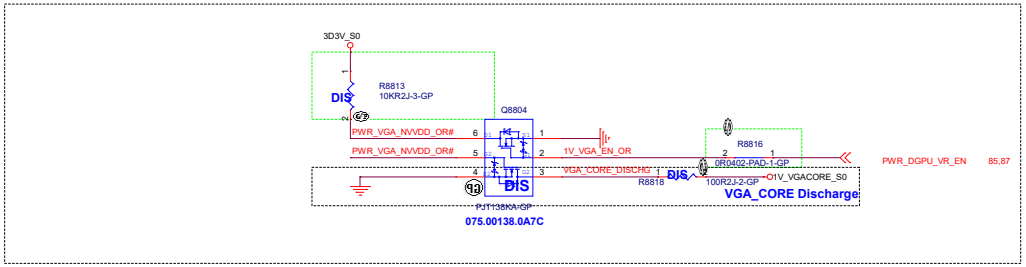

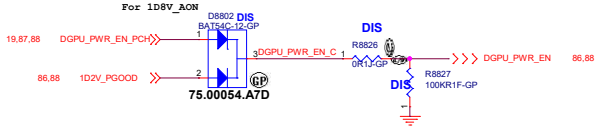

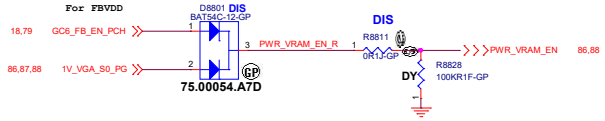

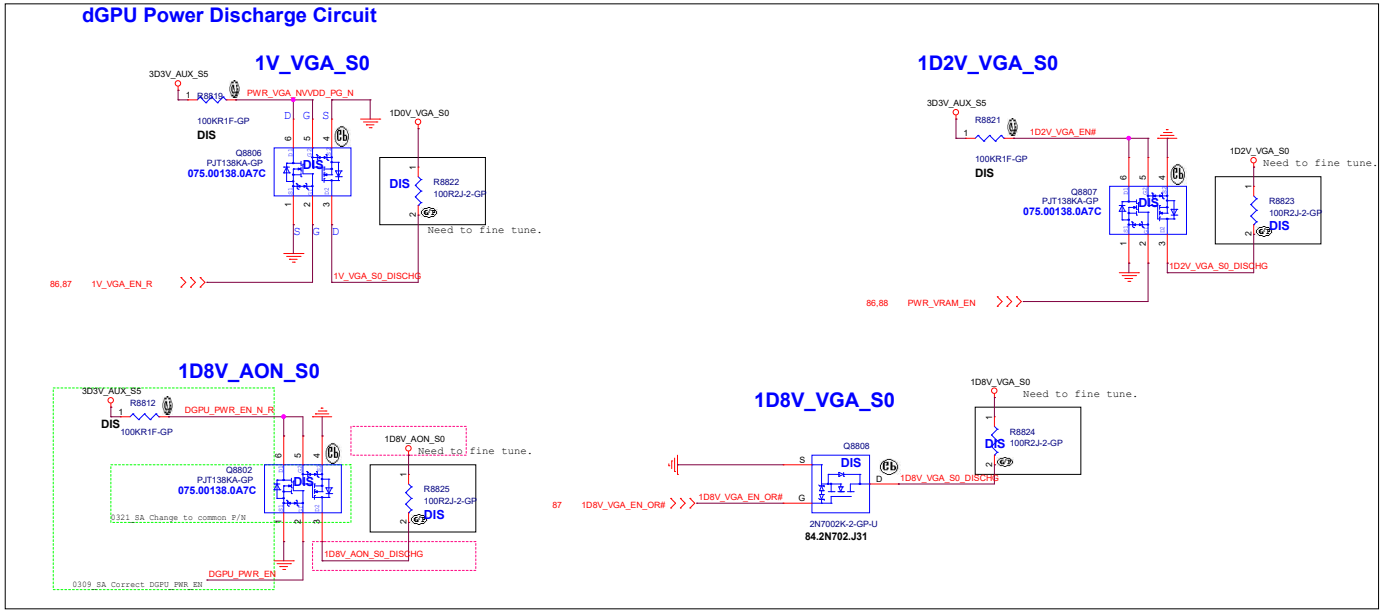

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Title: GPU (DISCHARGE/SEQUENCE)

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ZZ.00PAD.EJ1 H1 HOLE237R103-GP
ZZ.00PAD.QN1 H2 HOLE158R103-GP
ZZ.00PAD.EJ1 H3 HOLE237R103-GP
ZZ.00PAD.EJ1 H4 HOLE237R103-GP
ZZ.00PAD.EJ1 H5 HOLE237R103-GP
ZZ.00PAD.QN1 H6 HOLE158R103-GP
ZZ.SCREW.1A1 H8 HOLE197R111-GP
ZZ.SCREW.1A1 H9 HOLE197R111-GP
ZZ.00PAD.QN1 H12 HOLE158R103-GP
ZZ.00PAD.6N1 H13 HOLE197R67-GP
ZZ.00PAD.6N1 H14 HOLE197R67-GP

434.0HH0K.0001 HS1 STF237R113H91-GP
34.4EO02.001 HS2 STFT236B142R128H43-1-GP
34.4SE26.001 HS3 STF237R113H62-4-GP
34.4SE26.001 HS4 STF237R113H62-4-GP
34.4SE26.001 HS5 STF237R113H62-4-GP
34.4SE26.001 HS6 STF237R113H62-4-GP
34.4SE26.001 HS7 STF237R113H62-4-GP
34.4EO02.001 HS8 STFT236B142R128H43-1-GP

C550 FVT EMC request: change to 0.1U

PWR_DCBATOUT_VCCAUX: EC8901 SCD1U25V2KX-GP, EC8902 SCD1U25V2KX-GP
PWR_DCBATOUT_5V: EC8903 SCD1U25V2KX-GP
PWR_DCBATOUT_3D3V: EC8904 SCD1U25V2KX-GP
PWR_DCBATOUT_VGACOREB: EC8905 SCD1U25V2KX-GP, EC8907 SCD1U25V2KX-GP
PWR_DCBATOUT_VGACOREA: EC8906 SCD1U25V2KX-GP, EC8908 SCD1U25V2KX-GP
19V_DCBATOUT: EC8911 SCD1U25V2KX-GP

19V_DCBATOUT: EC8909 SCD1U25V2KX-GP, EC8910 SCD1U25V2KX-GP, EC8912 SCD1U25V2KX-GP, EC8913 SCD1U25V2KX-GP, EC8914 SCD1U25V2KX-GP, EC8915 SCD1U25V2KX-GP, EC8916 SCD1U25V2KX-GP, EC8917 SCD1U25V2KX-GP, EC8918 SCD1U25V2KX-GP, EC8919 SCD1U25V2KX-GP, EC8920 SCD1U25V2KX-GP, EC8921 SCD1U25V2KX-GP, EC8922 SCD1U25V2KX-GP, EC8923 SCD1U25V2KX-GP

C550 SIT EMC request: TOP

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Title: *INT IO (RSVD)*

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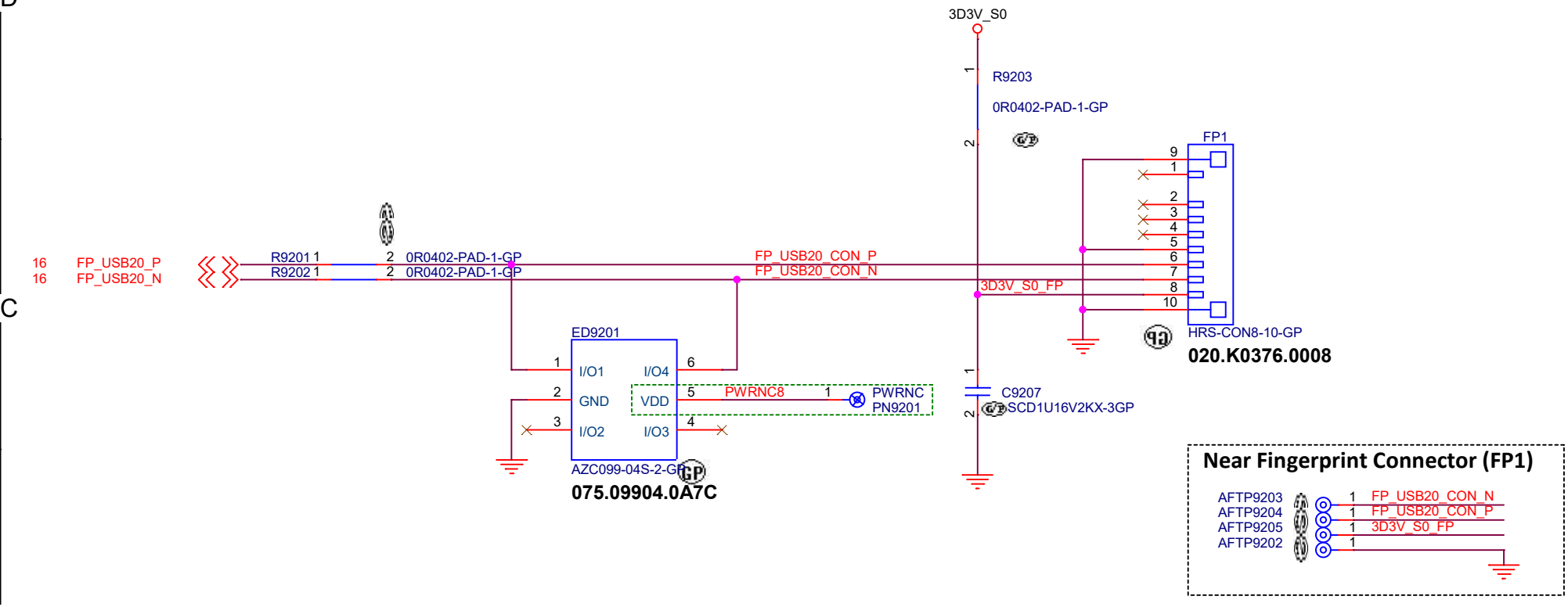
Fingerprint Connector



Near Fingerprint Connector (FP1)

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Taipei Hsien 221, Taiwan, R.O.C.

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Title: *COMMERCIAL (RSVD)*

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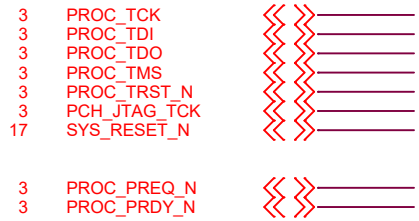

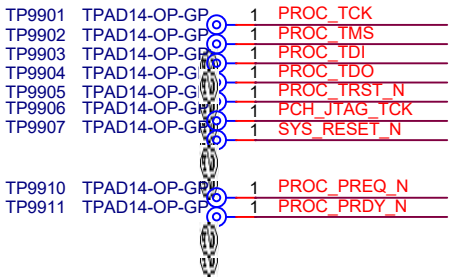

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DEBUG (XDP/DCI)***

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Title **CHANGE HISTORY**

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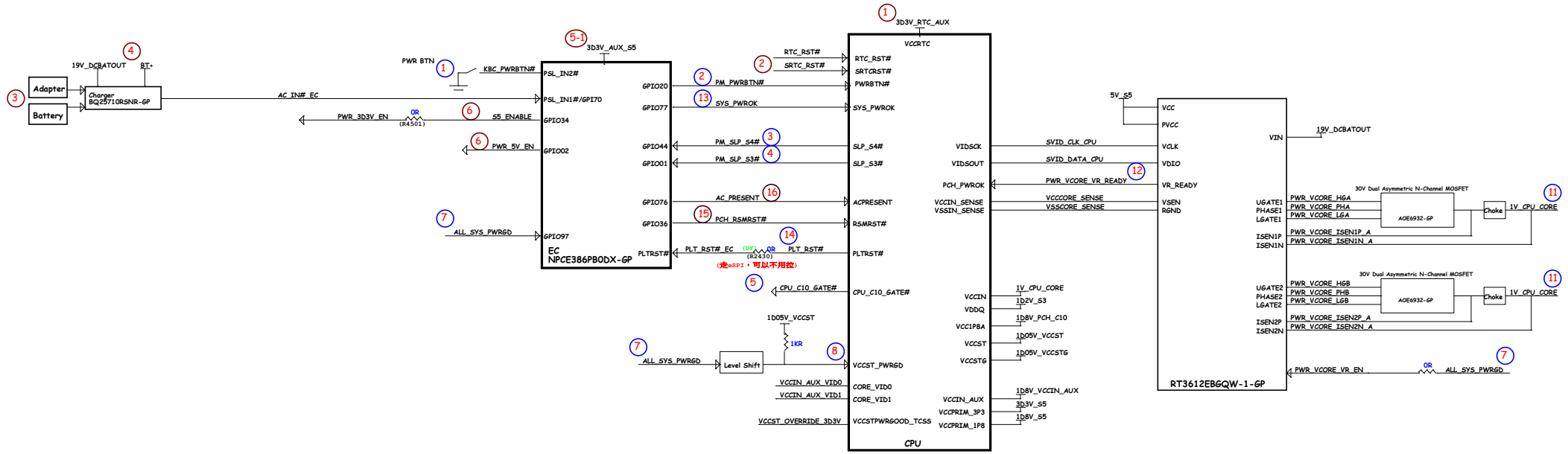
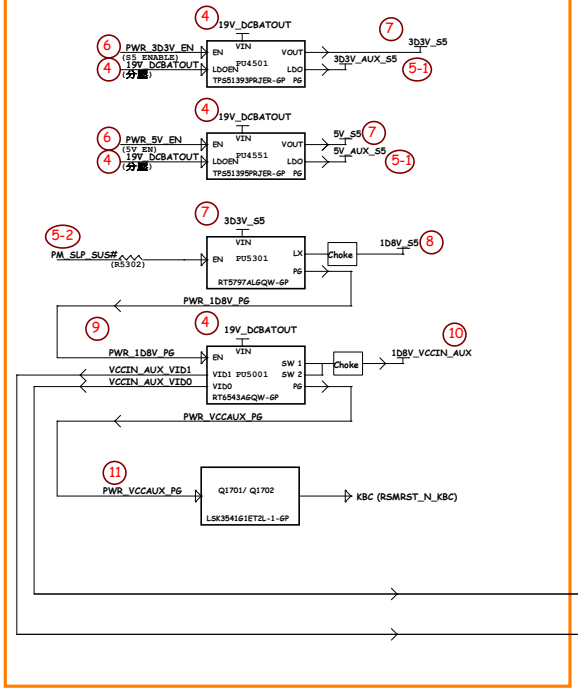
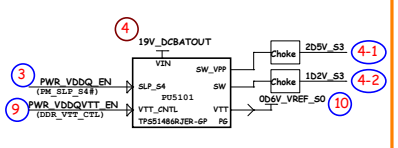
LC56 TGL SEQUENCE & BLOCK DIAGRAM



S5 PWR



S3 PWR



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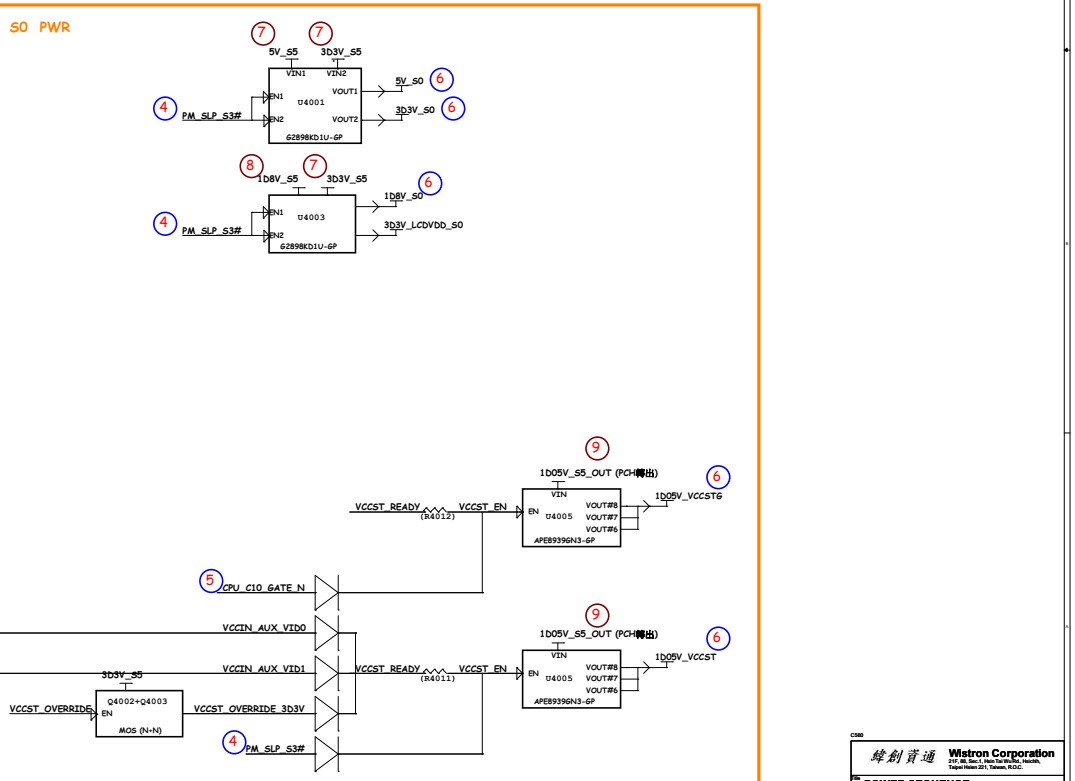

Wistron Corporation
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POWER SEQUENCE
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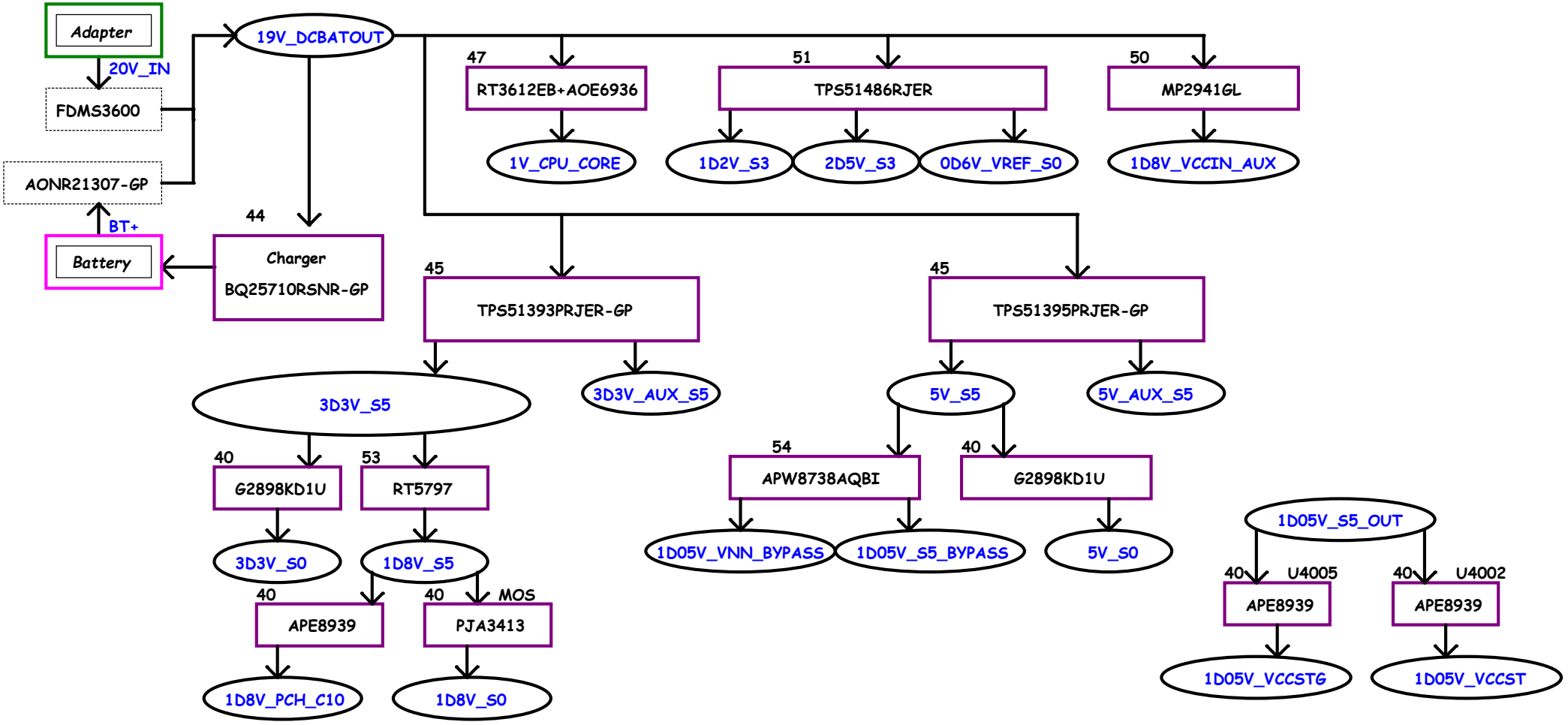
LC56 TGL Power Block Diagram



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Title: POWER BLOCK DIAGRAM

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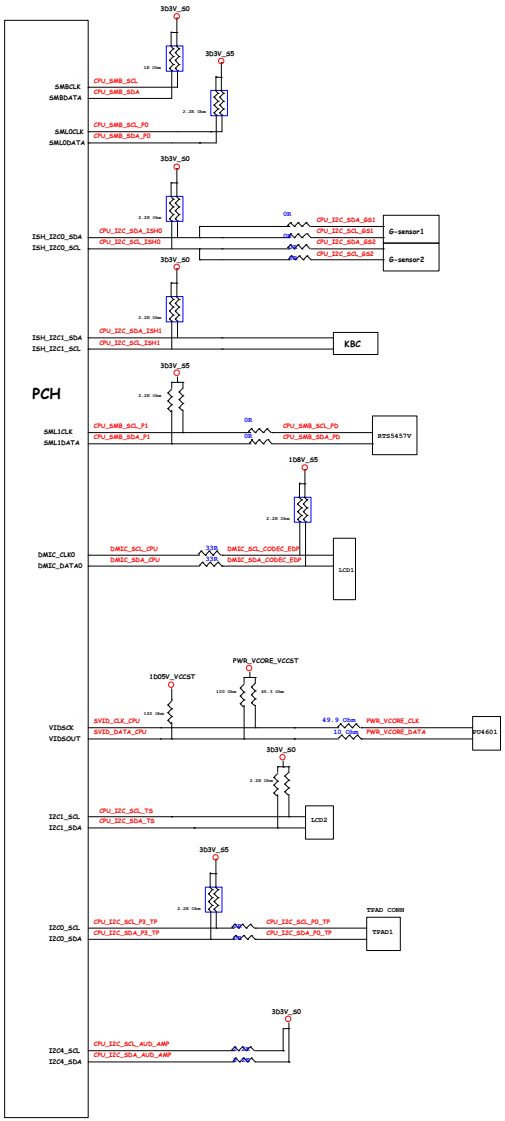
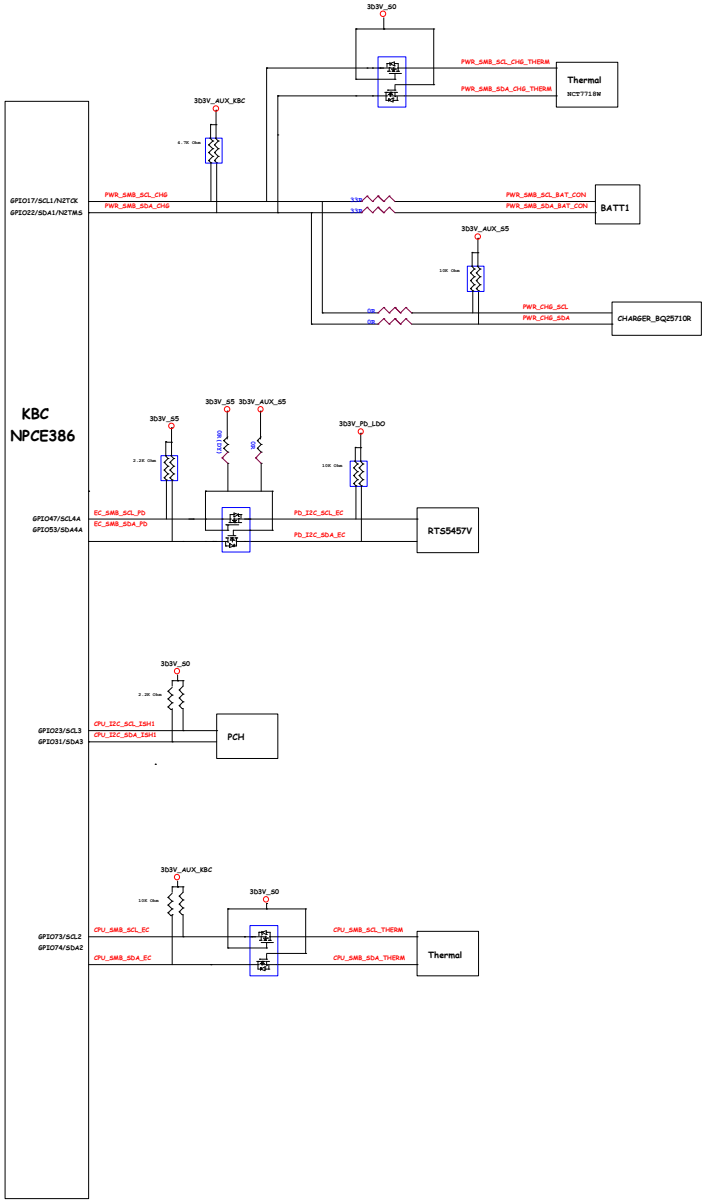
LC56 TGL SMBUS/I2C BLOCK DIAGRAM

PCH SMBus Block Diagram



KBC SMBus Block Diagram



CS60			
蜂創資通 Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: SMBUS/I2C BLOCK DIAGRAM			
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Title: ***THERMAL/AUDIO BLOCK DIAGRAM***

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Title: ***CLK BLOCK***

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