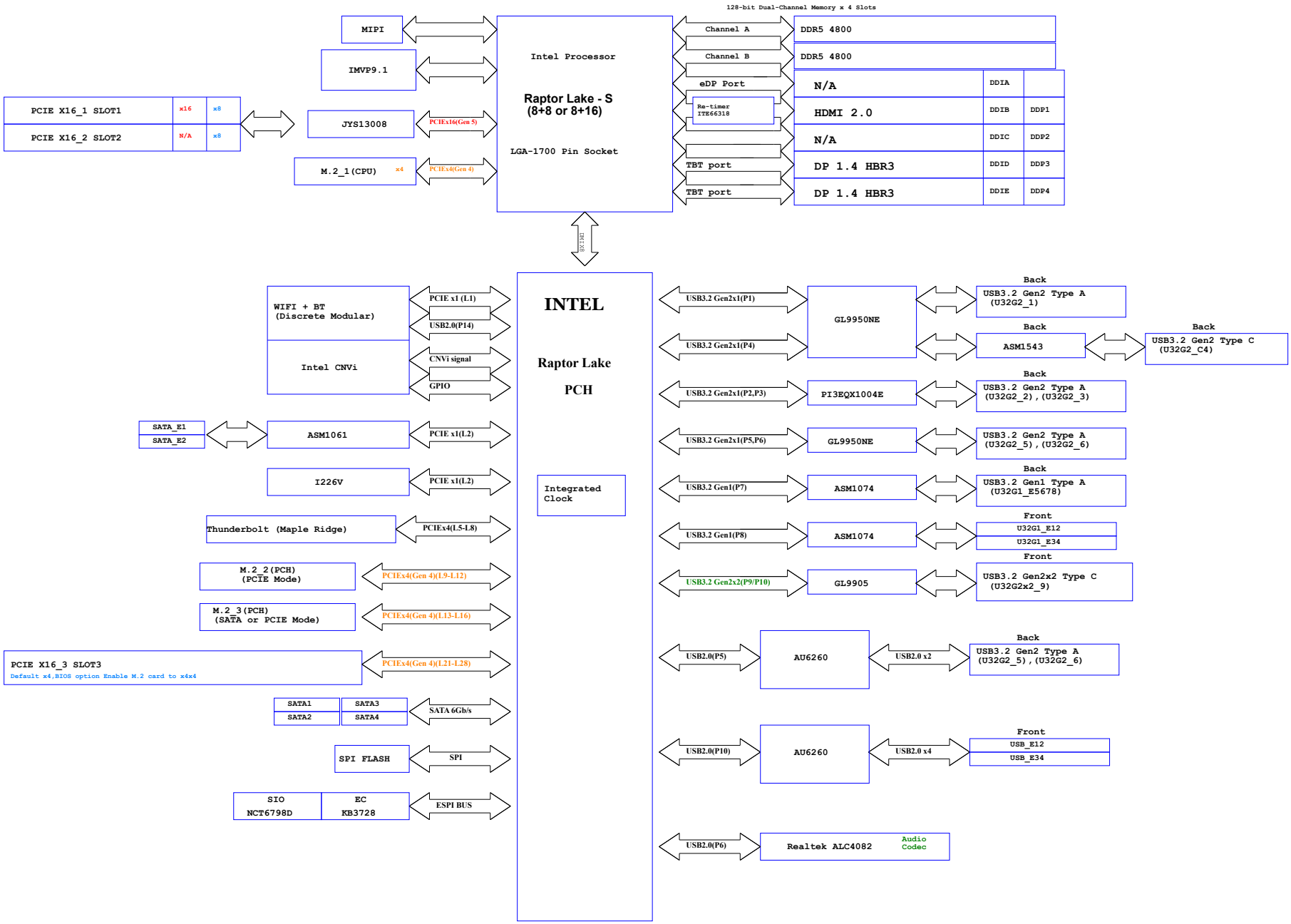
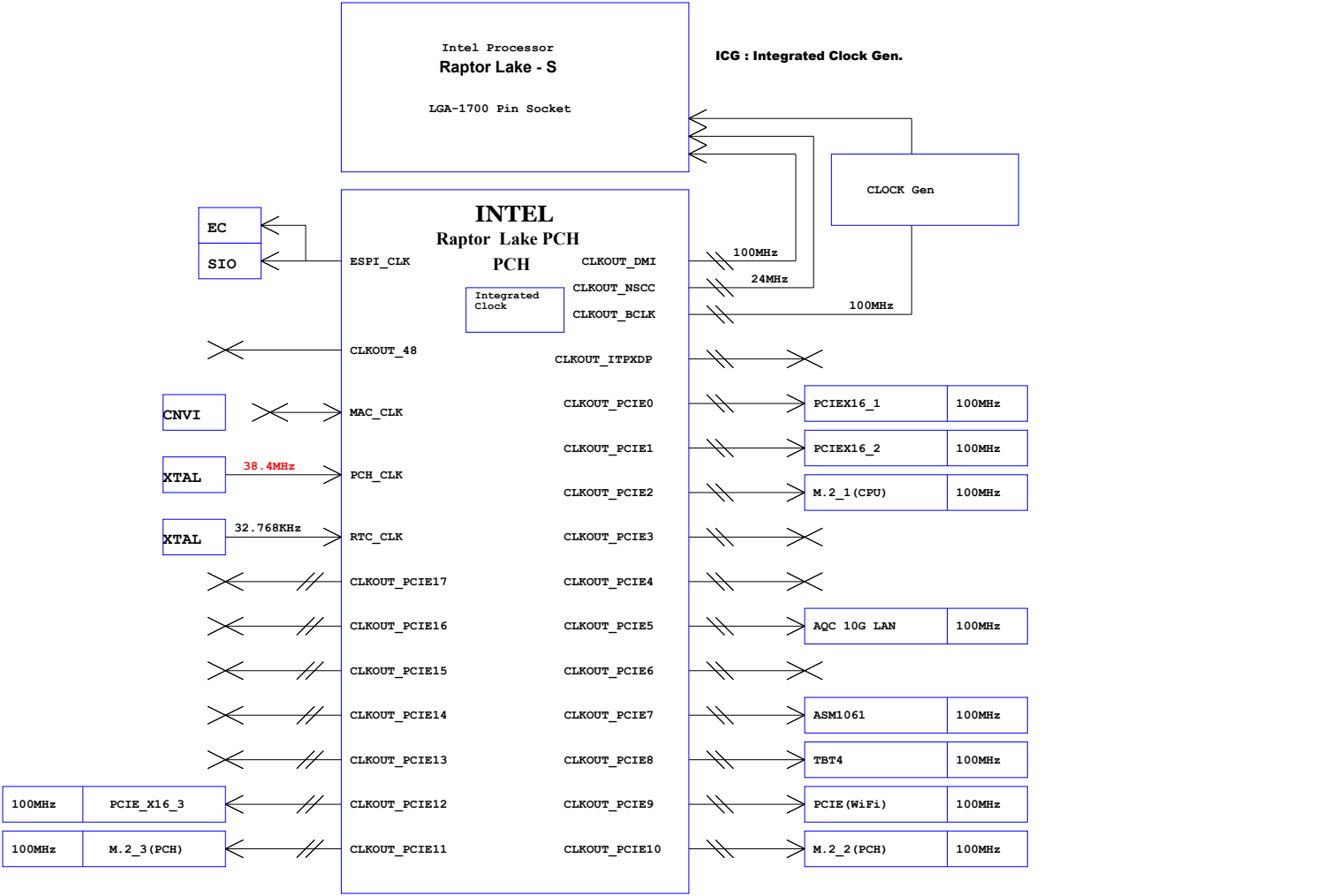
ROG MAXIMUS Z790 HERO

Rev 1.00X
2021/04





<Variant Name>

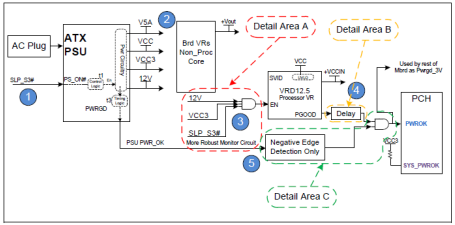
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: Leo_Chen

Size	Project Name	Rev
A3	ROG MAXIMUS Z790 HERO	R1.00

Date: Wednesday, July 06, 2022 Sheet 2 of 170



PCI_Express x 16_1 — PWRGD — <19>O_PCIRST#_PCIEX16_1

PCI_Express x 16_2 — PWRGD — <19>O_PCIRST#_PCIEX16_2

PCI_Express x 1_1,2 & x16_3 — PWRGD — <19>O_PCIRST#_PCIEX16_3

POWER_SWITCH — PWRBTN — <5>O_PWRBTN#IN

SIO NCT6779D

PS_IN# — PCIRST1# — PCIRST2# — PCIRST3# — LRESET# — KBRST# — RSMRST# — PS_OUT# — PSON# *1 — ATXPGD *2 — PWROK — SUSC# — SUSB#

<18>S_PLTRST# *8 — O_KB_RST# — <4>O_RSMRST# — <6>O_PWRBTN# — <4.1> / <8>S_SLPS4# — <4.2> / <9>S_SLPS3#

POWER SUPPLY

Main PWR — VSB — PSON# — PWROK

<2>AC Power Switch On

<10>12V,5V,3V — <3>+5VSB, +3VSB — <9>O_PSON# — <11>B_ATX_PWROK

PCH LYNX POINT

HDA_RST# — AZ_RST# — RESET# — AUDIO ALC898

SYS_RESET# — PLTRST# — PLTRST_PROC# — RCIN# — DRAMPWROK — RSMRST# — RTCRST# — PWRBTN# — SRTCRST# — SLP_S5# — SLP_S4# *4 — SLP_S3# *5 — PROCPUPWRGD — SLP_A# *3 — SLP_LAN# — DPWROK — SYS_PWROK — PCH_PWROK — MEPWROK

<1>RTCRST# — <1>SRTCRST# — BATTERY

<7>S_SLP_A# — <7.1>S_SLP_LAN# — <3.1>S_DPWROK

Non-AMT — AMT

<12>O_PWROK

RESET_SWITCH — SYS_RESET#

XDP — DBR# — RESET# — OBSDATA — SYS_RESET# — H_CPURST#

PROCESSOR HASWELL

SYS_RESET# *9 — <18>H_CPURST# — <13>S_DRAMPWRGD — <1>RTCRST# — <1>SRTCRST# — *7 — <14>H_CPUPWRGD

DBR# — RESET# — SM_DRAMPWROK — CFG — PWRGOOD — SVID — VCORE

<15>VRM_SVID — <16>VCORE

ME_POWER — +1.05ME — +3V_DUAL_LAN/EPW — <7.2>S_MEPWROK

Vcore Controller — SVID — VCORE — VR_ON — PGOOD — ISL95818

*6 — S_SLPS3# — +12V — +3V — <17>VRMPWRGD

*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

*5 Come with 1.5VDUAL

*6 Come with +3V,+12V and gated by SLP_S3#

*7 CPUPWRGD= After PWROK

*8 PLTRST# = PCH PWROK AND PCH SYS_PWROK

*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

CHIP — SOCKET or SLOT

<Variant Name>

ASUSTek COMPUTER INC.

Title : Signal & Reset map

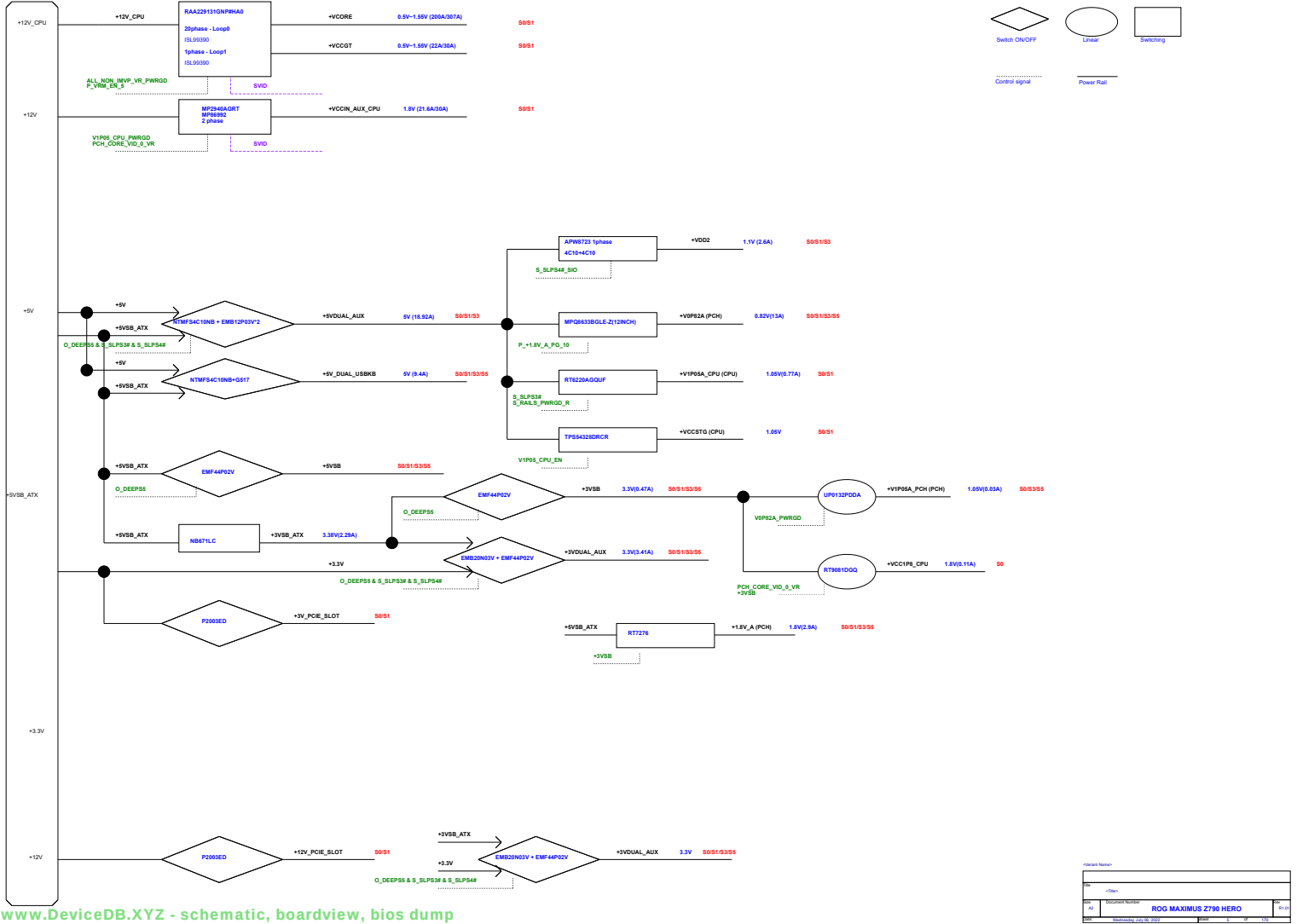
Engineer: Eason

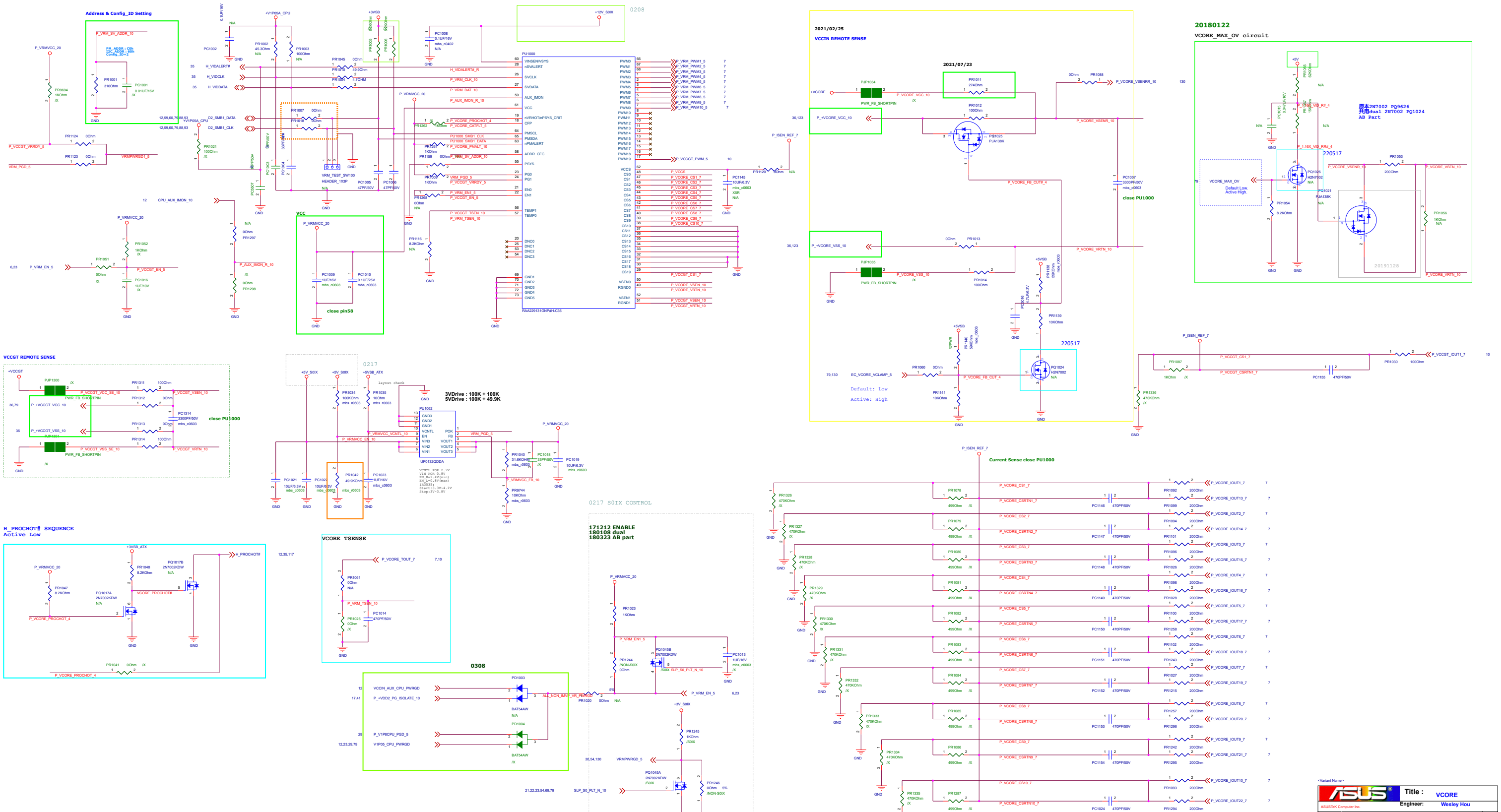
Size: A3 — Project Name: ROG MAXIMUS Z790 HERO — Rev: R1.00

Date: Wednesday, July 06, 2022 — Sheet 3 of 170

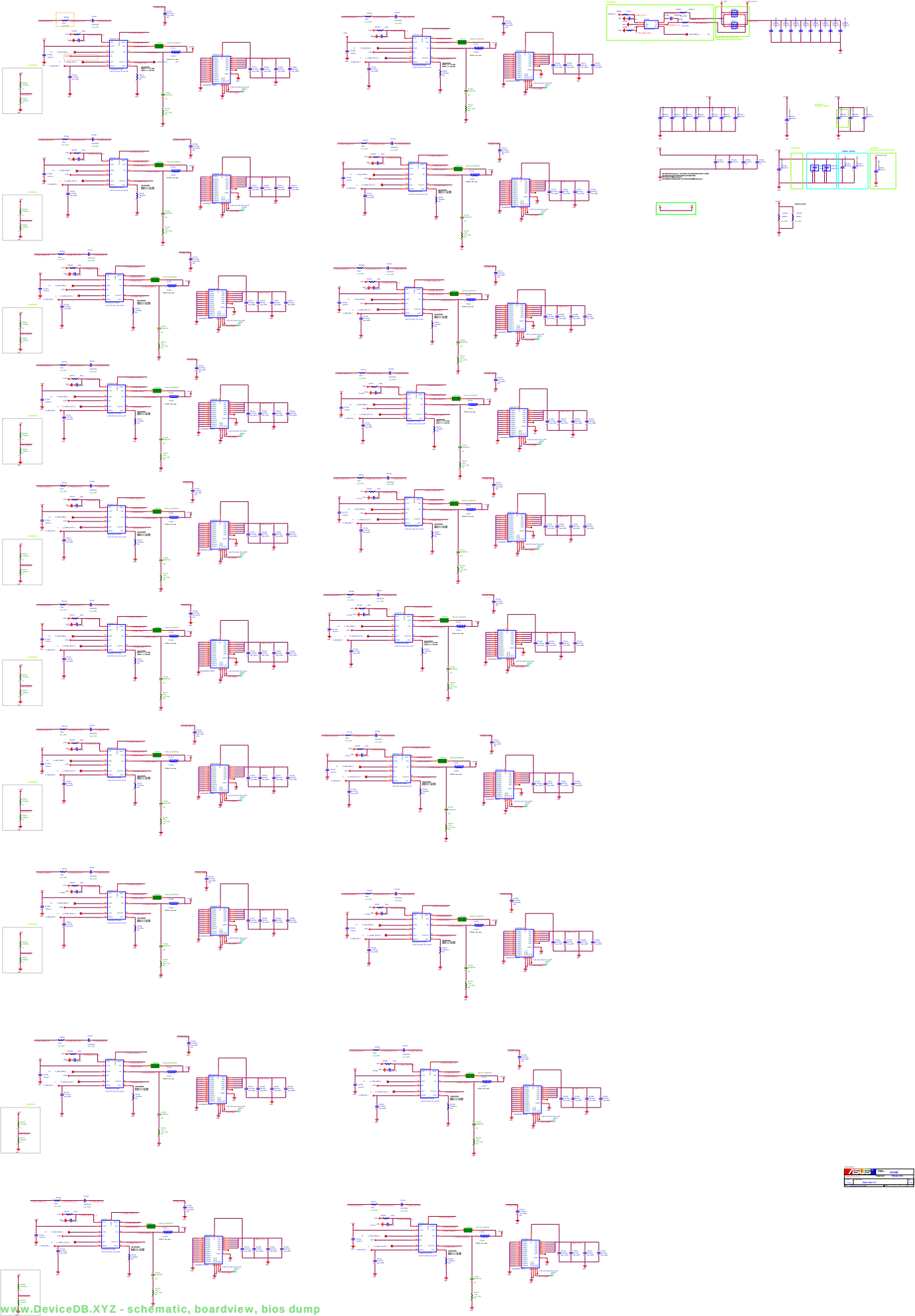
<Variant Name>

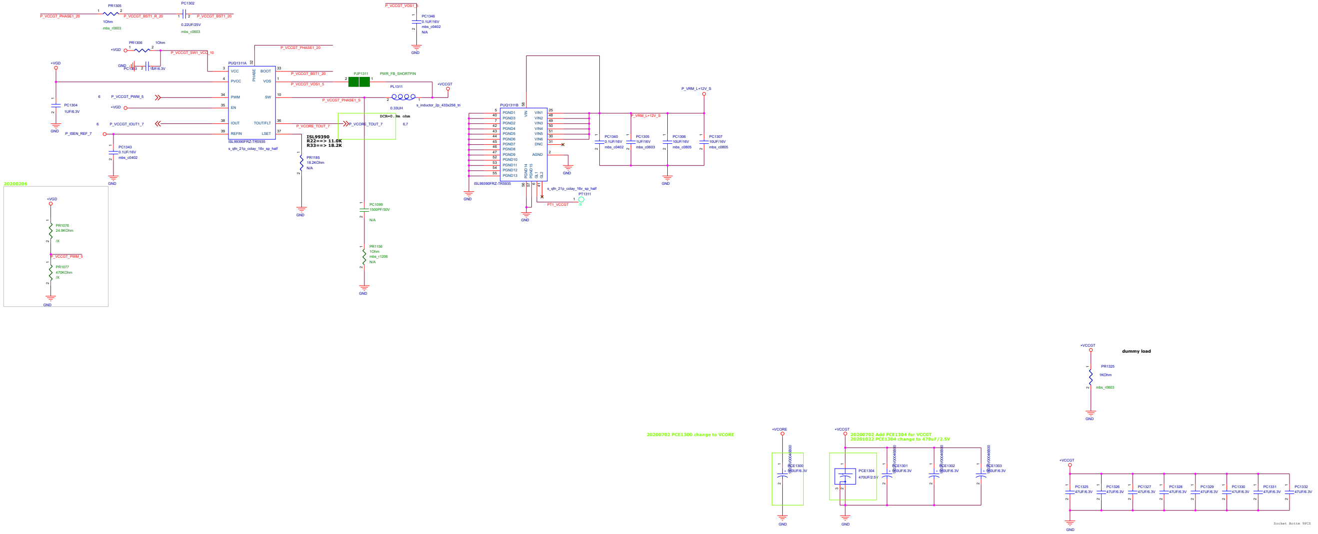
ASUSTek COMPUTER INC.	Title : POWER FLOW CHART	
	Engineer: Cisco	
Size: Custom	Project Name: ROG MAXIMUS Z790 HERO	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 4 of 170	




Address & Config_ID Setting
PM_ADDR : C0h
I2C_ADDR : 80h
Config_ID=2
0208
VCC
close pin58
2021/02/25
VCCIN REMOTE SENSE
2021/07/23
close PU1000
20180122
VCORE_MAX_OV circuit
原本2N7002 PQ9626
共用dual 2N7002 PQ1024
AB Part
220517
VCORE_MAX_OV
Default Low.
Active High.
20191128
VCCGT REMOTE SENSE
close PU1000
0217
layout check
3VDrive : 100K + 100K
5VDrive : 100K + 49.9K
PU1062
UP0132QDDA
Default: Low
Active: High
Current Sense close PU1000
H_PROCHOT# SEQUENCE
Active Low
VCORE TSENSE
0308
0217 S0IX CONTROL
171212 ENABLE
180108 dual
180323 AB part
PU1000
RAA229131GNP#H-C35
PD1003
BAT54AW
PD1004
BAT54AW

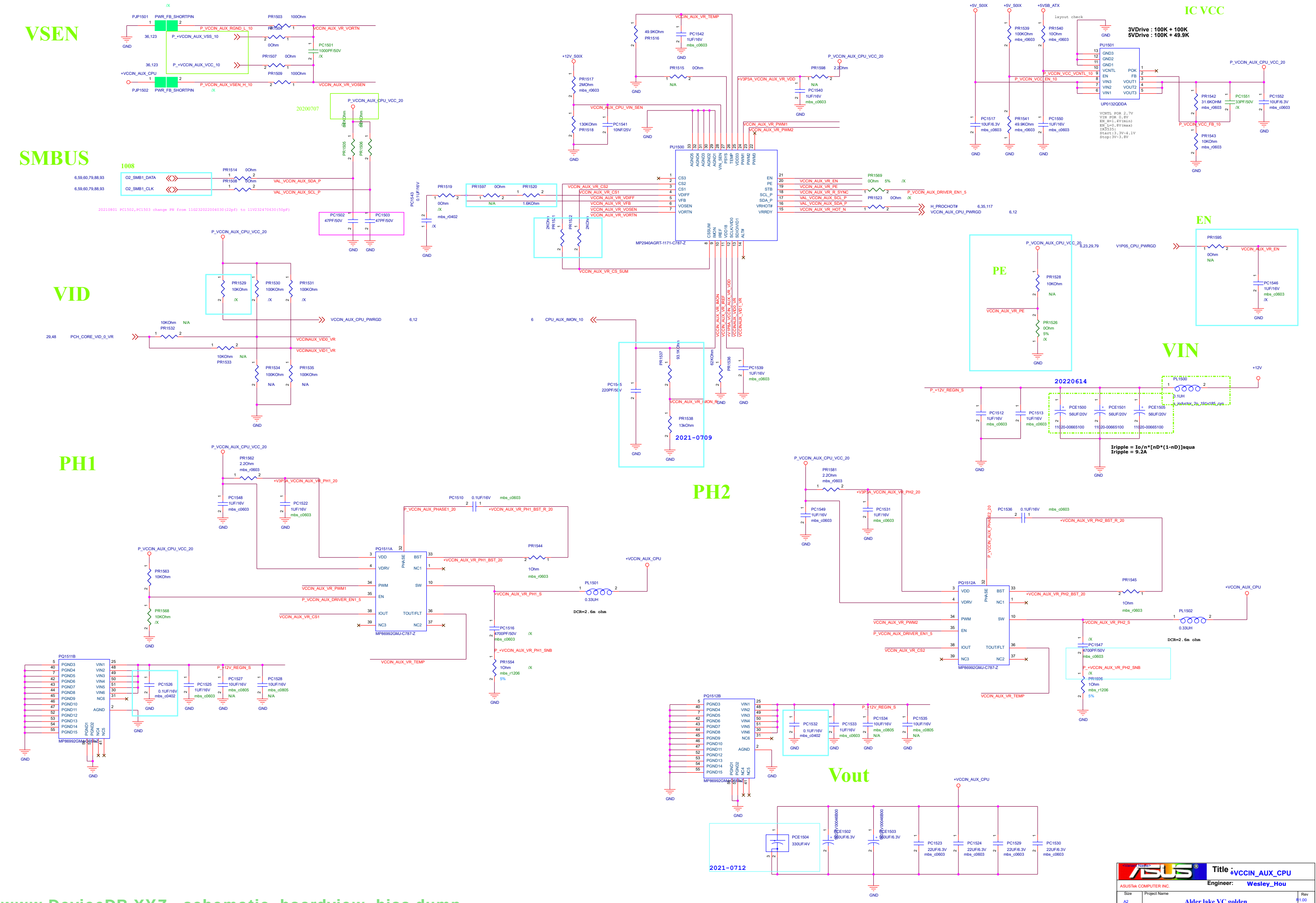
Title : VCORE
Engineer: Wesley Hou
ASUSTeK Computer Inc.
Project Name: Alder lake VC golden
Rev R1.00
Date: Wednesday, July 06, 2022 Sheet 6 of 170





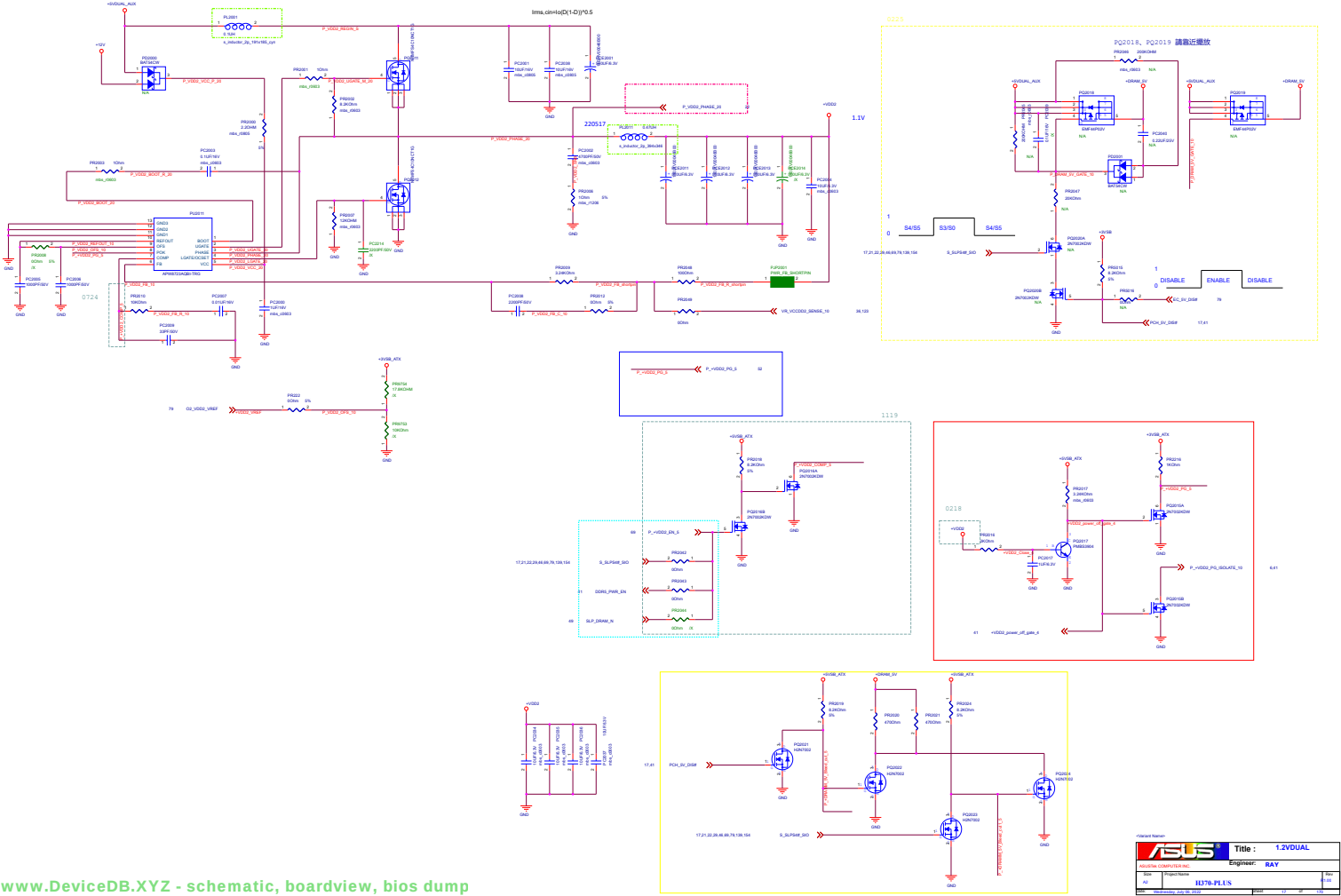
<Variant Name>

ASUSTeK Computer Inc.	Title : VCCGT	
	Engineer:	
Size: Custom	Project Name: Alder lake VC	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 10 of 170	



<Variant Name>

ASUSTeK Computer Inc.	Title : VCORE MLCC&CAP	
	Engineer: Wesley Hou	
Size: Custom	Project Name: Alder lake VC golden	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 16 of 170	

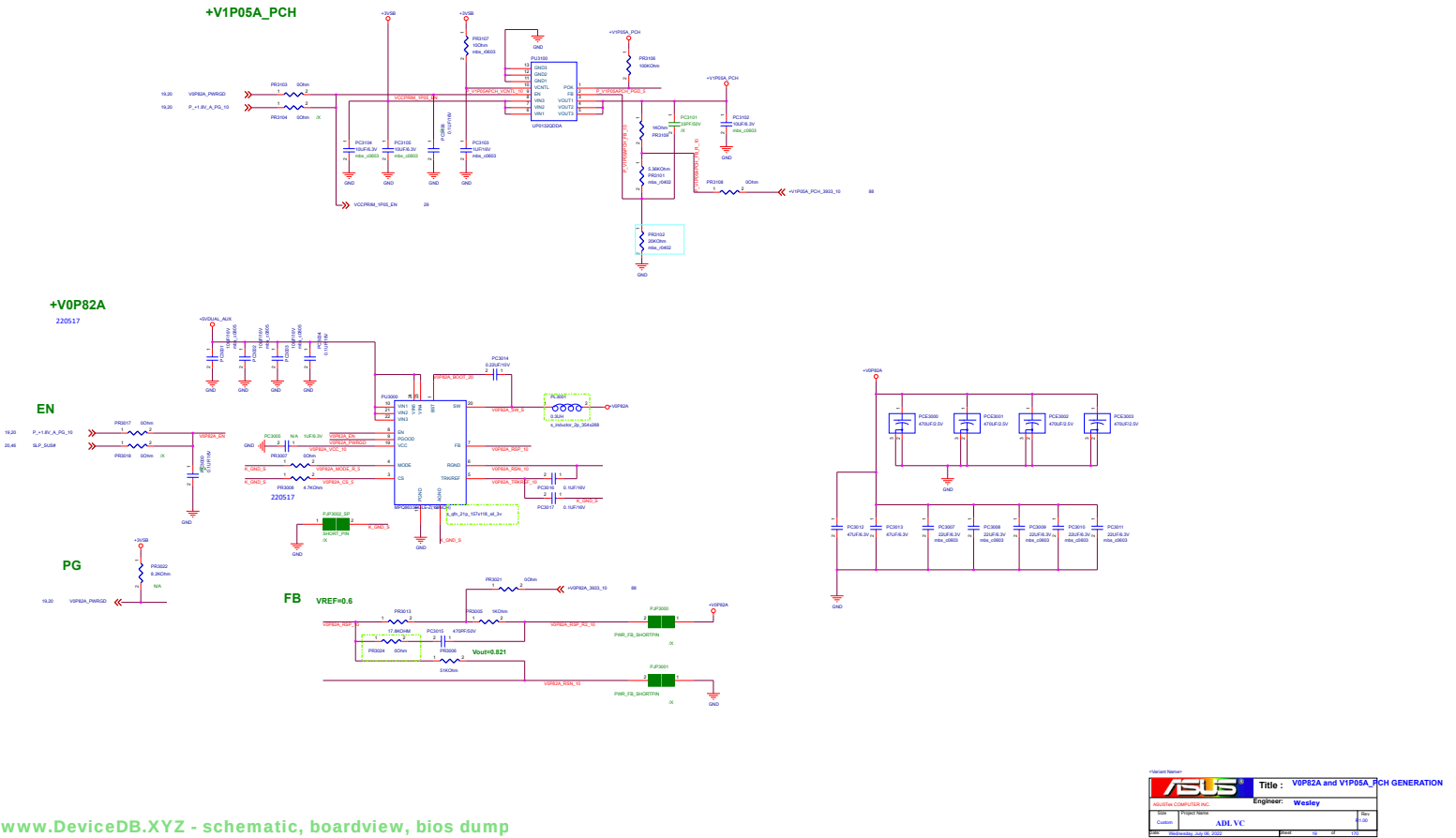


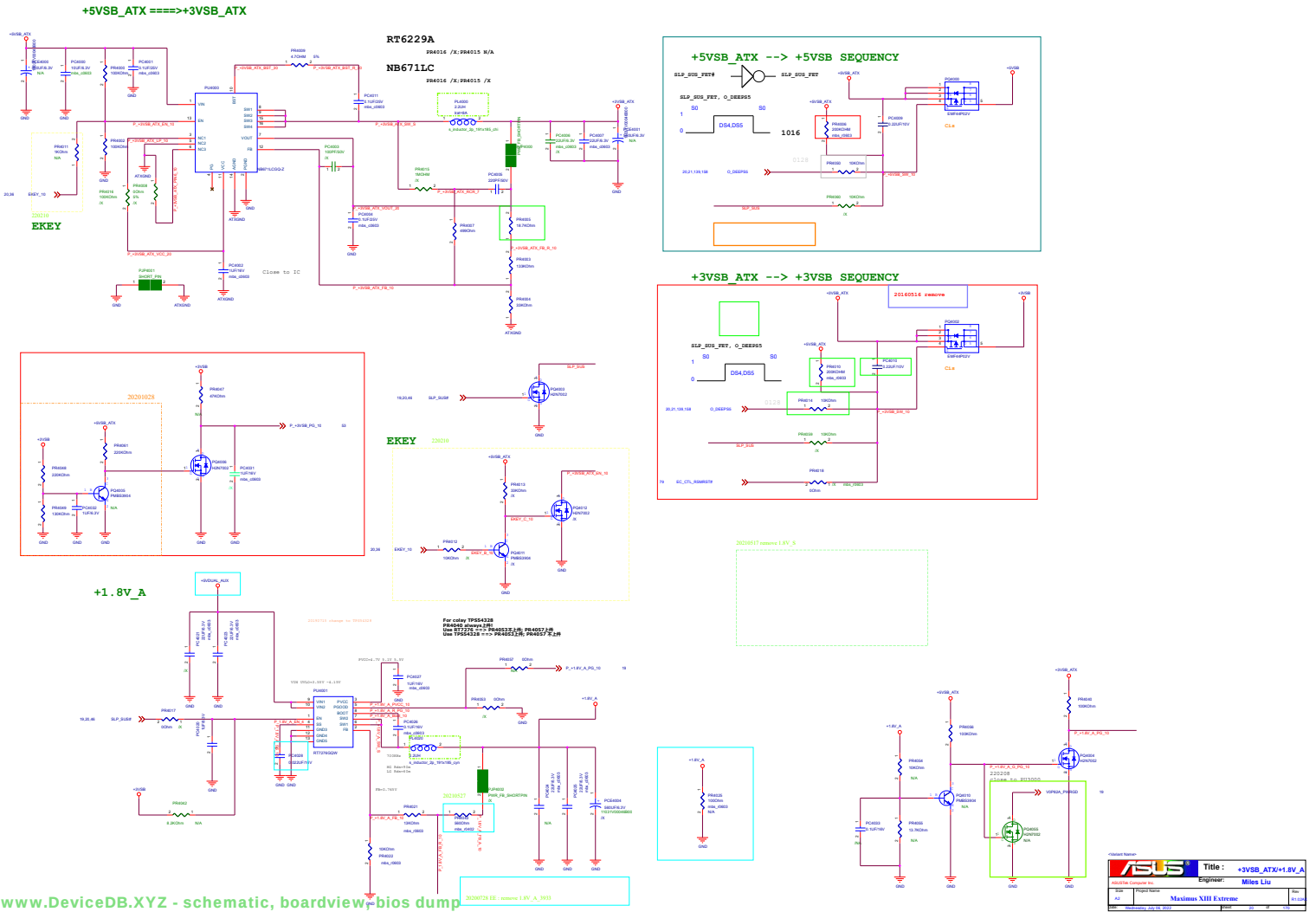
Variant Name:

Title :	1.2VDUAL
Engineer:	RAY
ASUSTeK COMPUTER INC.	
Size: A2	Project Name: H370-PLUS
Rev: 0.01	
Date: Wednesday, July 06, 2016	Sheet 17 of 105

<Variant Name>

ASUSTek Computer Inc.	Title : +VPPDDR(NB671)	
	Engineer: Wesley Hou	
Size: Custom	Project Name: ROG MAXIMUS Z790 HERO	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 18 of 170	





USBKB

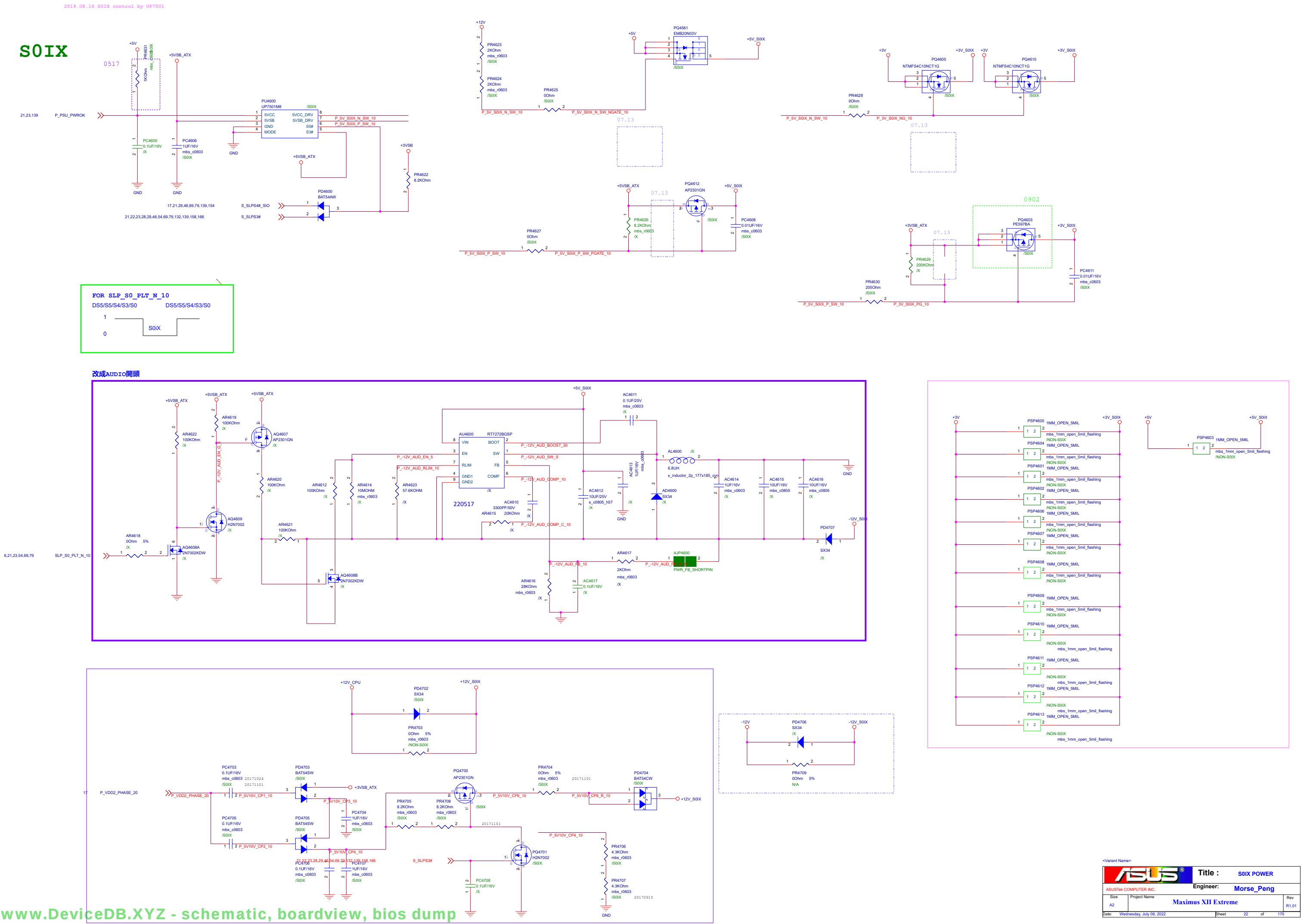
5VDUAL_AUX

set MODE pin (AUX & USB)

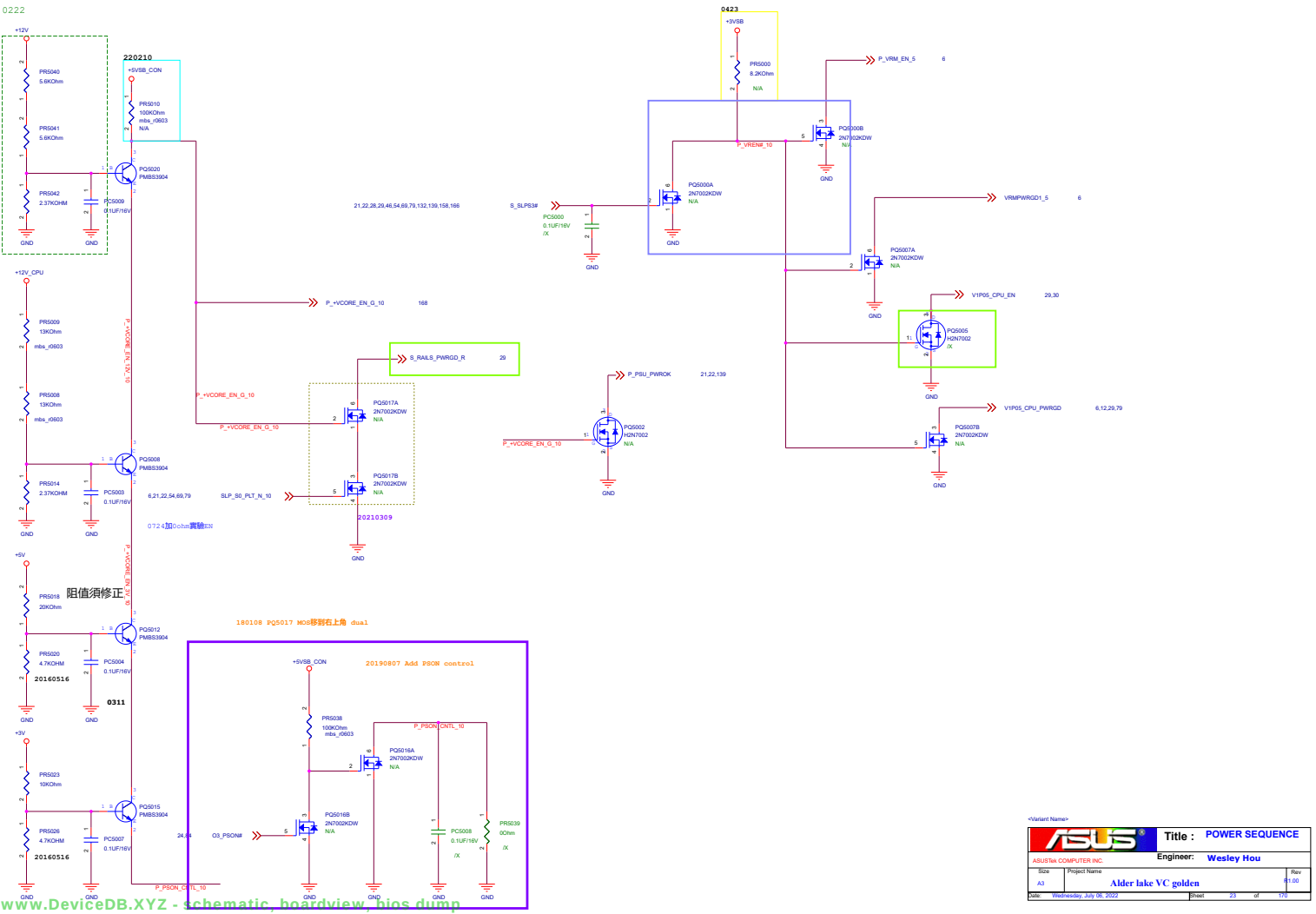
20180201 移除5VDUAL 3VDUAL

控制S0IX UP7501

Title : +5V_UDAL_USBKB
Engineer: Miles Liu
Maximus XII Extreme



2019.08.16 S0IX control by UP7501
S0IX
0517
+5V
+5VSB_ATX
PR4631
1KOhm
21,23,139
P_PSU_PWROK
PU4600
UP7501M8
/S0IX
5VCC
5VSB
GND
MODE
5VCC_DRV
5VSB_DRV
S5#
S3#
P_5V_S0IX_N_SW_10
P_5V_S0IX_P_SW_10
PC4605
0.1UF/16V
/X
PC4606
1UF/16V
mbs_c0603
/S0IX
GND
+3VSB
PR4622
8.2KOhm
PD4600
BAT54AW
17,21,29,46,69,79,139,154
S_SLPS4#_SIO
21,22,23,28,29,46,54,69,79,132,139,158,166
S_SLPS3#
+12V
PR4623
2KOhm
mbs_r0603
/S0IX
PR4624
2KOhm
mbs_r0603
/S0IX
PR4625
0Ohm
/S0IX
P_5V_S0IX_N_SW_NGATE_10
PQ4561
EMB20N03V
+5V_S0IX
07.13
PQ4612
AP2301GN
+5V_S0IX
PR4626
8.2KOhm
mbs_r0603
/X
PC4608
0.01UF/16V
mbs_c0603
/S0IX
PR4627
0Ohm
/S0IX
P_5V_S0IX_P_SW_10
P_5V_S0IX_P_SW_PGATE_10
+3V
+3V_S0IX
PQ4605
NTMFS4C10NCT1G
PQ4610
NTMFS4C10NCT1G
PR4628
0Ohm
/S0IX
P_3V_S0IX_NG_10
0902
+3VSB_ATX
PQ4603
PE597BA
PR4629
200KOhm
/X
PR4630
205Ohm
/S0IX
P_3V_S0IX_PG_10
PC4611
0.01UF/16V
mbs_c0603
/S0IX
FOR SLP_S0_PLT_N_10
DS5/S5/S4/S3/S0
DS5/S5/S4/S3/S0
1
0
S0IX
改成AUDIO開頭
AU4600
RT7272BGSP
VIN
EN
RLIM
GND1
GND2
BOOT
SW
FB
COMP
P_-12V_AUD_BOOST_20
P_-12V_AUD_EN_5
P_-12V_AUD_RLIM_10
P_-12V_AUD_SW_S
P_-12V_AUD_COMP_10
P_-12V_AUD_COMP_C_10
P_-12V_AUD_FB_10
220517
AC4611
0.1UF/25V
mbs_c0603
AL4600
6.8UH
s_inductor_2p_177x185_cyn
AD4600
SX34
AC4614
1UF/16V
AC4615
10UF/16V
AC4616
10UF/16V
-12V_S0IX
PD4707
SX34
AR4617
2KOhm
AJP4600
PWR_FB_SHORTPIN
AR4616
28KOhm
AC4617
0.1UF/16V
AR4622
100KOhm
AR4619
100KOhm
AQ4607
AP2301GN
AR4620
100KOhm
AR4612
100KOhm
AR4614
10MOHM
AR4623
57.6KOHM
AC4610
3300PF/50V
AR4615
20KOhm
AR4621
100KOhm
AQ4609
H2N7002
AR4618
0Ohm 5%
AQ4608A
2N7002KDW
AQ4608B
2N7002KDW
6,21,23,54,69,79
SLP_S0_PLT_N_10
+12V_CPU
+12V_S0IX
PD4702
SX34
/S0IX
PR4703
0Ohm 5%
mbs_r0603
/NON-S0IX
P_VDD2_PHASE_20
PC4703
0.1UF/16V
PC4705
0.1UF/16V
PD4703
BAT54SW
PD4705
BAT54SW
P_5V10V_CP1_10
P_5V10V_CP2_10
P_5V10V_CP3_10
P_5V10V_CP4_10
PC4704
1UF/16V
PC4706
0.1UF/16V
PC4707
1UF/16V
PQ4700
AP2301GN
PR4705
8.2KOhm
PR4708
8.2KOhm
PR4704
0Ohm 5%
P_5V10V_CP6_10
P_5V10V_CP6_R_10
PD4704
BAT54CW
+12V_S0IX
S_SLPS3#
PC4708
0.1UF/16V
PQ4701
H2N7002
PR4706
4.3KOhm
PR4707
4.3KOhm
20170915
-12V
-12V_S0IX
PD4706
SX34
PR4709
0Ohm 5%
N/A
PSP4605
PSP4604
PSP4601
PSP4602
PSP4606
PSP4607
PSP4608
PSP4609
PSP4610
PSP4611
PSP4612
PSP4613
PSP4603
1MM_OPEN_5MIL
mbs_1mm_open_5mil_flashing
/NON-S0IX
<Variant Name>
Title : S0IX POWER
ASUSTek COMPUTER INC.
Engineer: Morse_Peng
Size A2
Project Name
Maximus XII Extreme
Rev R1.01
Date: Wednesday, July 06, 2022
Sheet 22 of 170



All Gaming only

20150602

20150602

20150602

20150602

20150602

20150602

20150602

20150602

20150602

20150602

0225
update 1.7V & 2.3V 2level protection
1225:
改1+3VSB_ATX_2顆電阻+5VSB_ATX
適用Gaming 相位數下降給2.3V

0225
update 1.7V & 2.3V 2level protection
1225:
改1+3VSB_ATX_2顆電阻+5VSB_ATX
適用Gaming 相位數下降給2.3V

20170919

Protection threshold is 2.64V

Protection threshold is 3.515V

0515 add

0515 add

0205 add PC9637 & PC9504 close PQ9507

20180323 single

20110424C06

20110424C06

141106 避開RC,C座1000P

141106 避開RC,C座1000P

141106 避開RC,C座1000P

20180109 刪除phase FLT

POWER TEST

POWER TEST

20160516 remove
141225 ray加的濾磁版OVP

20160516 remove
141225 ray加的濾磁版OVP

<Variant Name>

ASUSTeK Computer Inc.

Title : PWM7-8

Engineer: Miles Liu

Size: Custom

Project Name: Maximus XIII Extreme

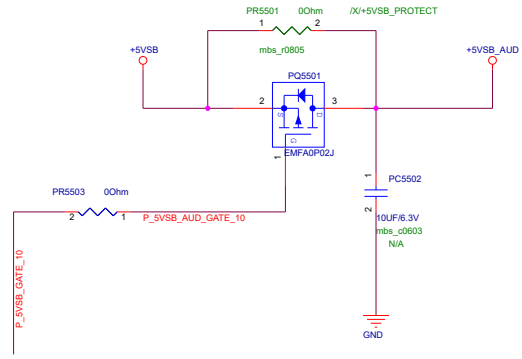
Rev: 1.01

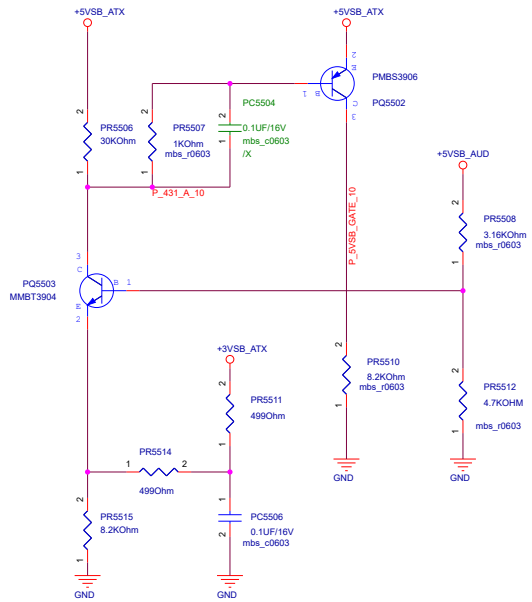
Date: Wednesday, July 08, 2020

Sheet 24 of 110

20160520 follow Strix Z270

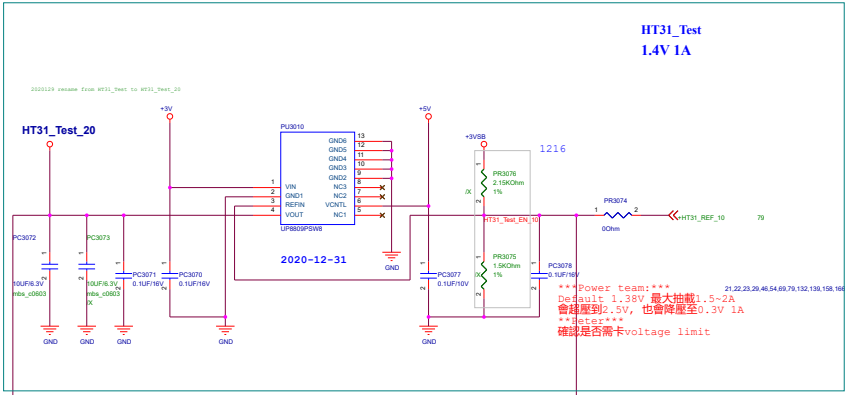
2018.01.17

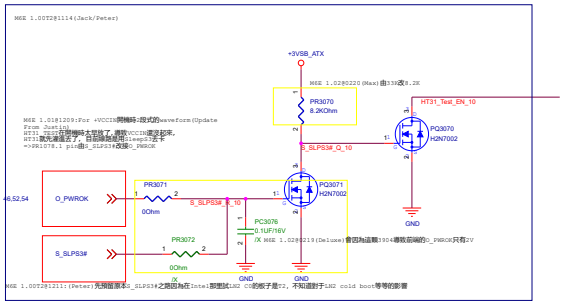


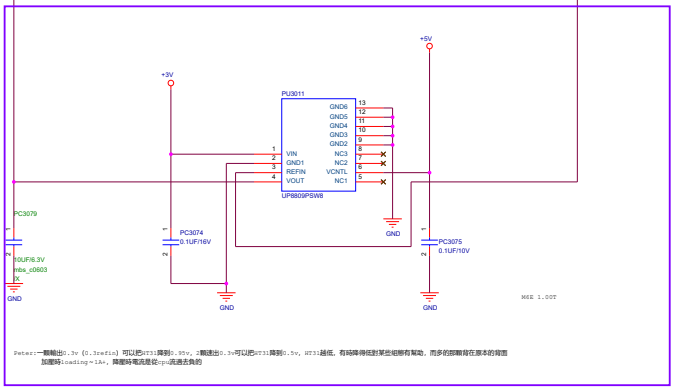


<Variant Name>

ASUSTek COMPUTER INC.	Title : +5VSB_AUD	
	Engineer: RAY	
Size: Custom	Project Name: Maximus XIII Extreme	Rev: P1.02AX
Date: Wednesday, July 06, 2022	Sheet 25 of 170	



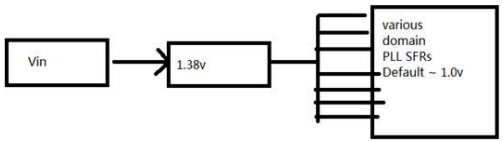


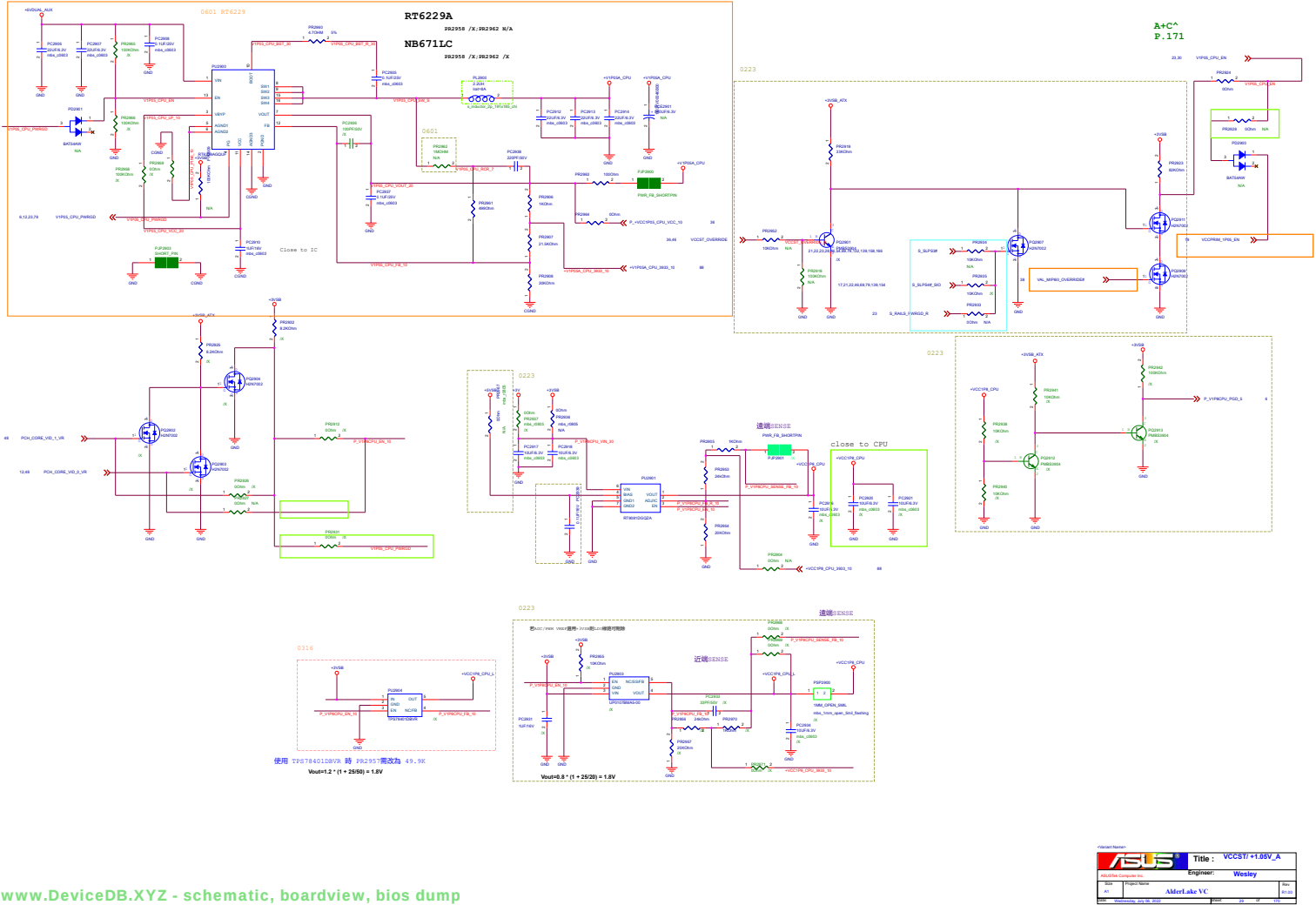


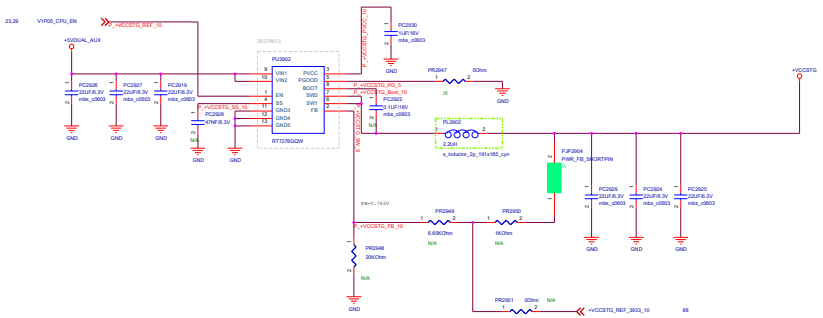
OV EC1_PWM3

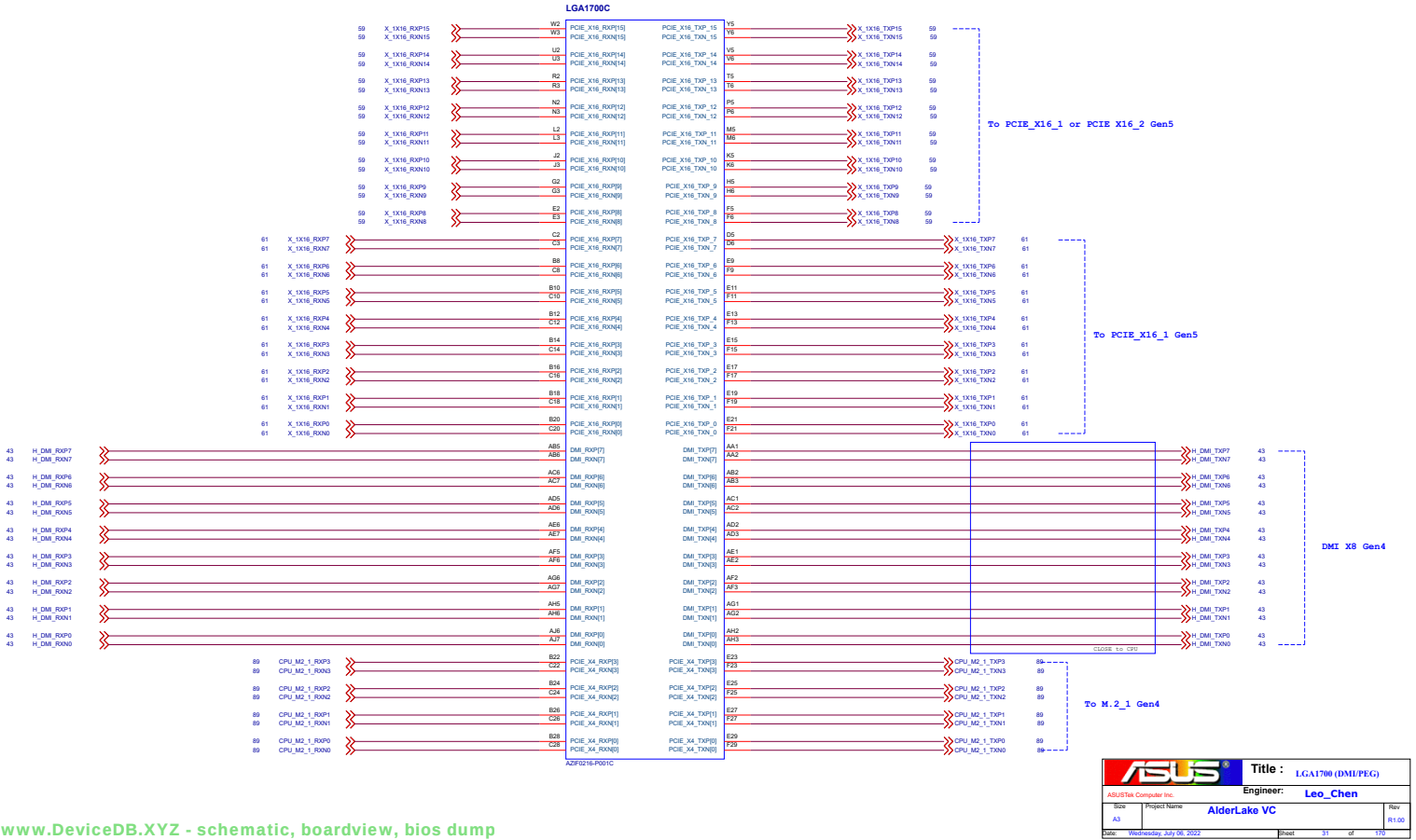
placement close to O2U1

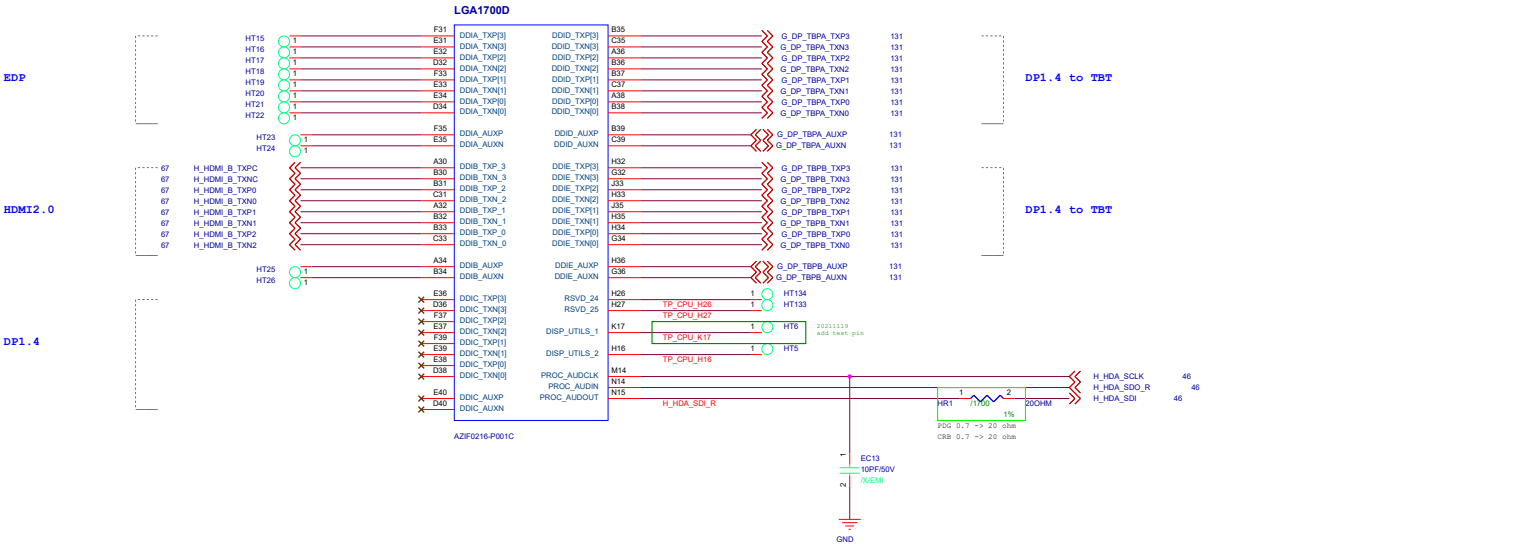
在 intel 问到 PLL Engineer PLL SFRs 的前一届的 level 是 1.38v，应该就是 HT31. 前一届上，后面会上，比例不一样罢了. 所以 HT31 先来才会罐回到 VIN



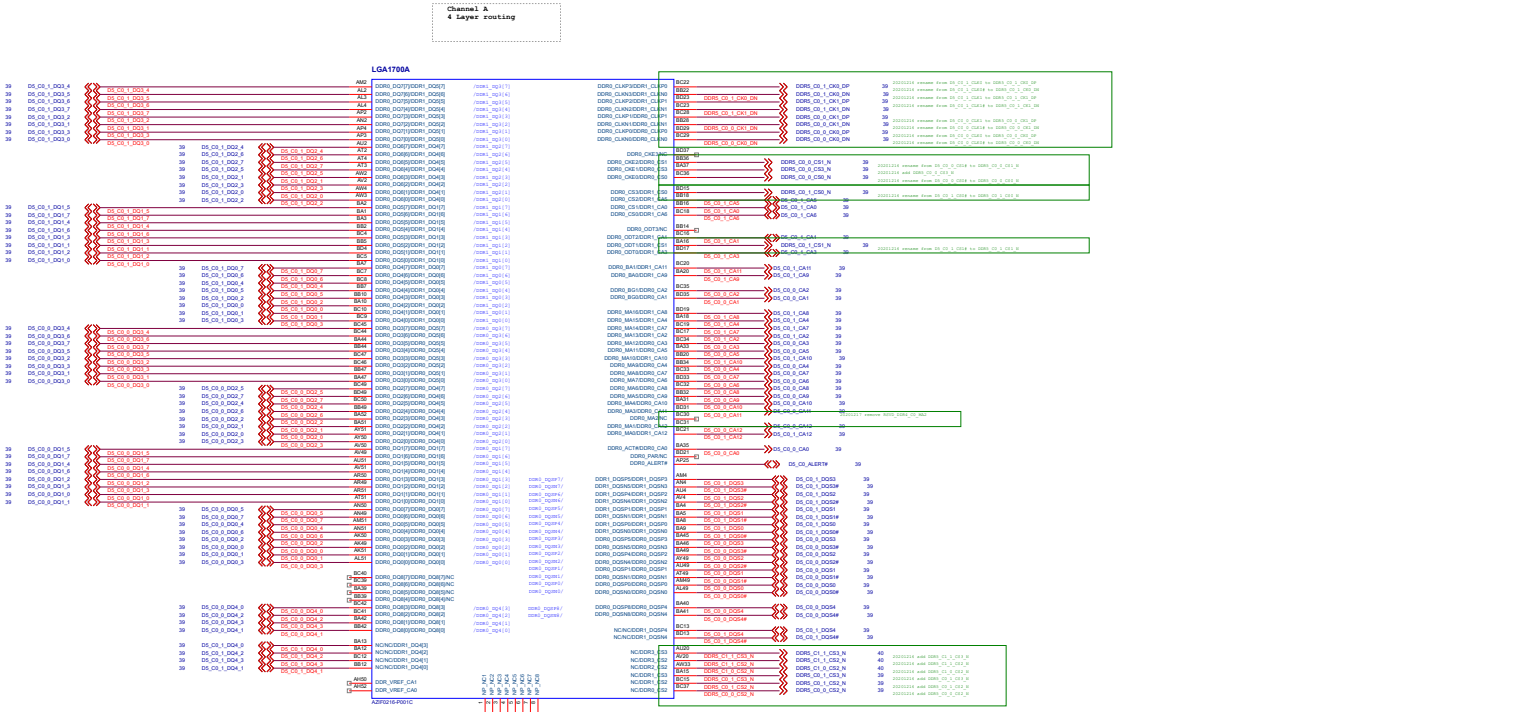




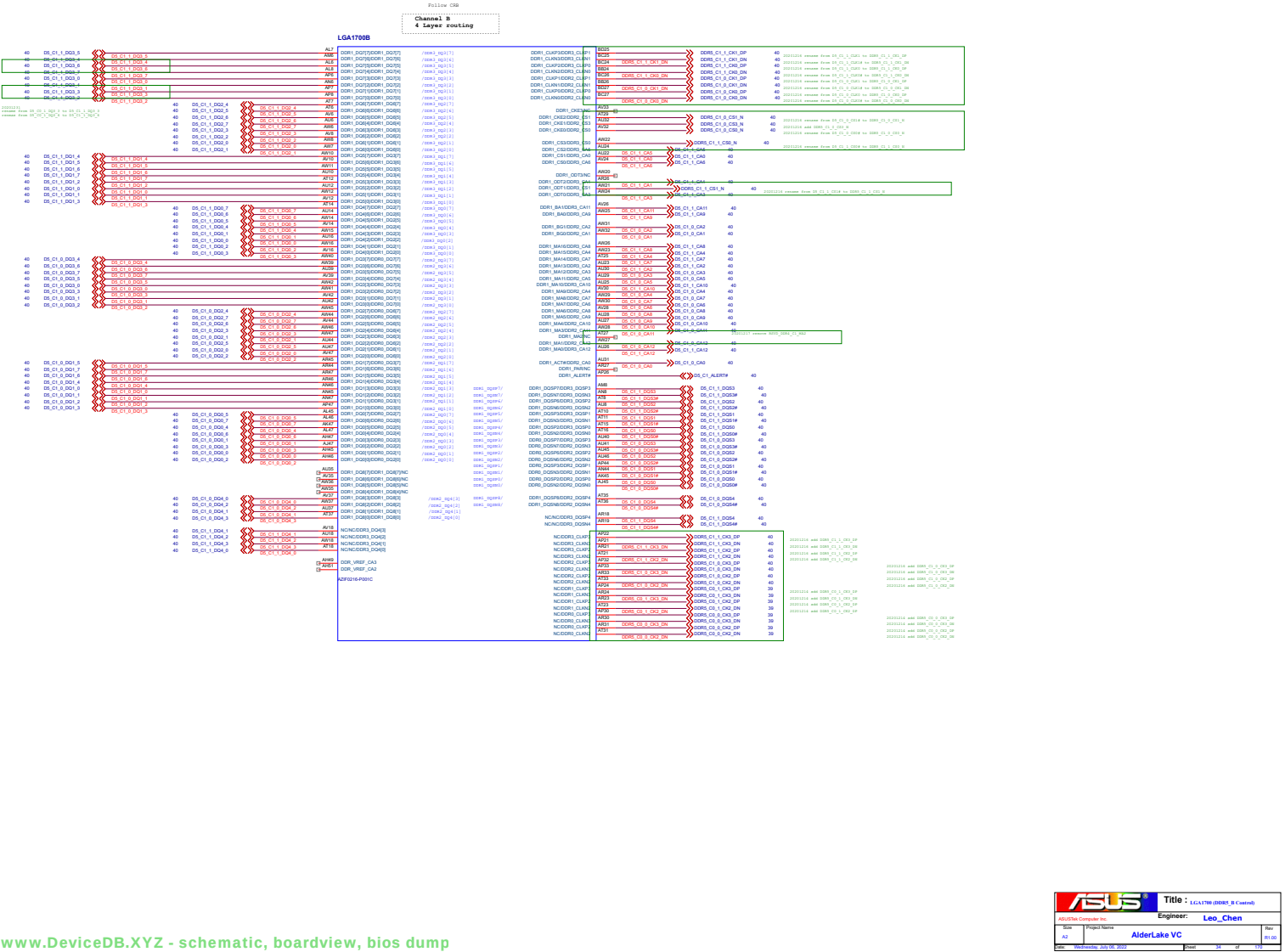




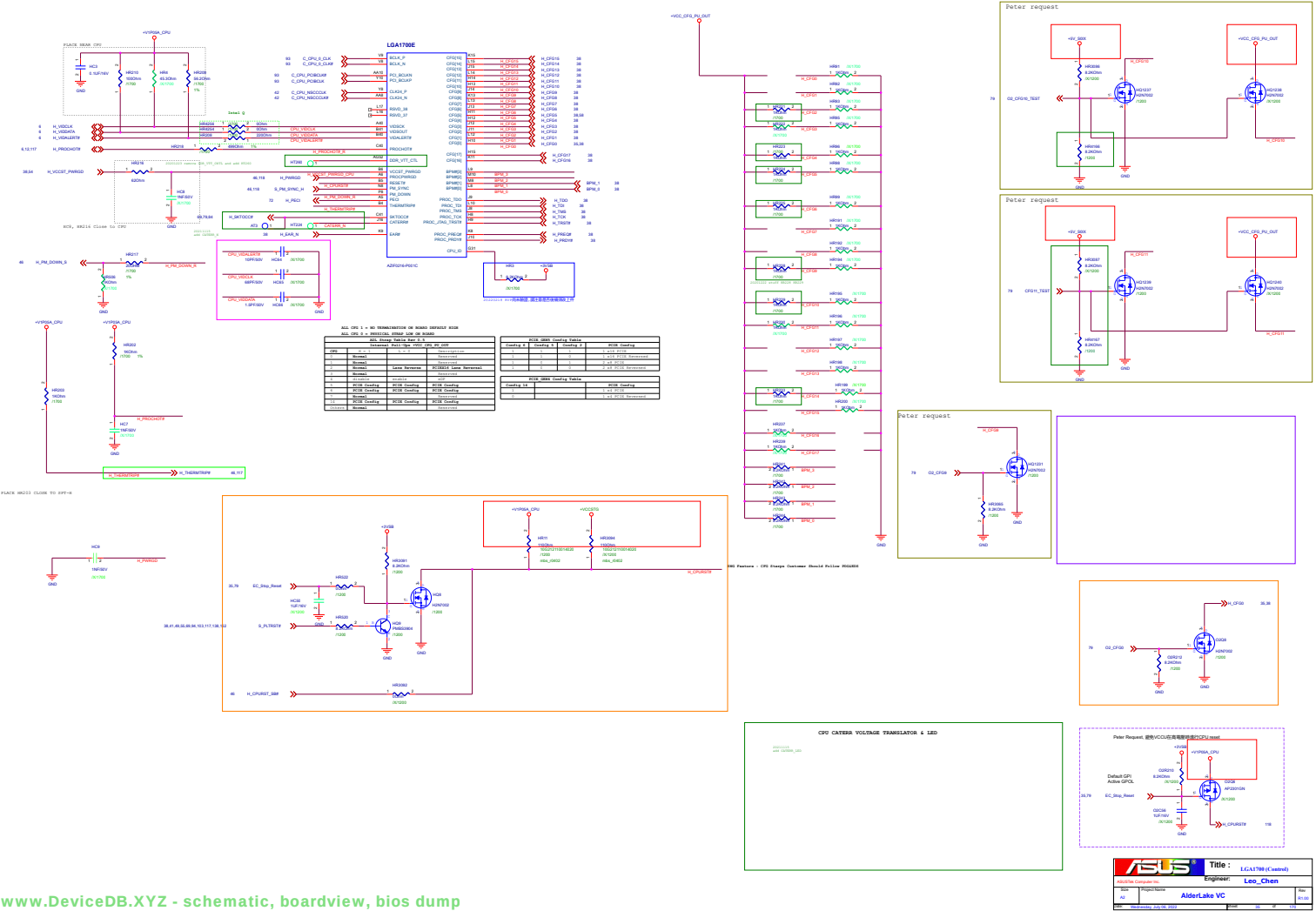
ASUSTek Computer Inc.	Title : LGA1700 (FDI/DISPLAY)		
	Engineer: Leo_Chen		
Size: A3	Project Name: AlderLake VC		Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 32 of 170		

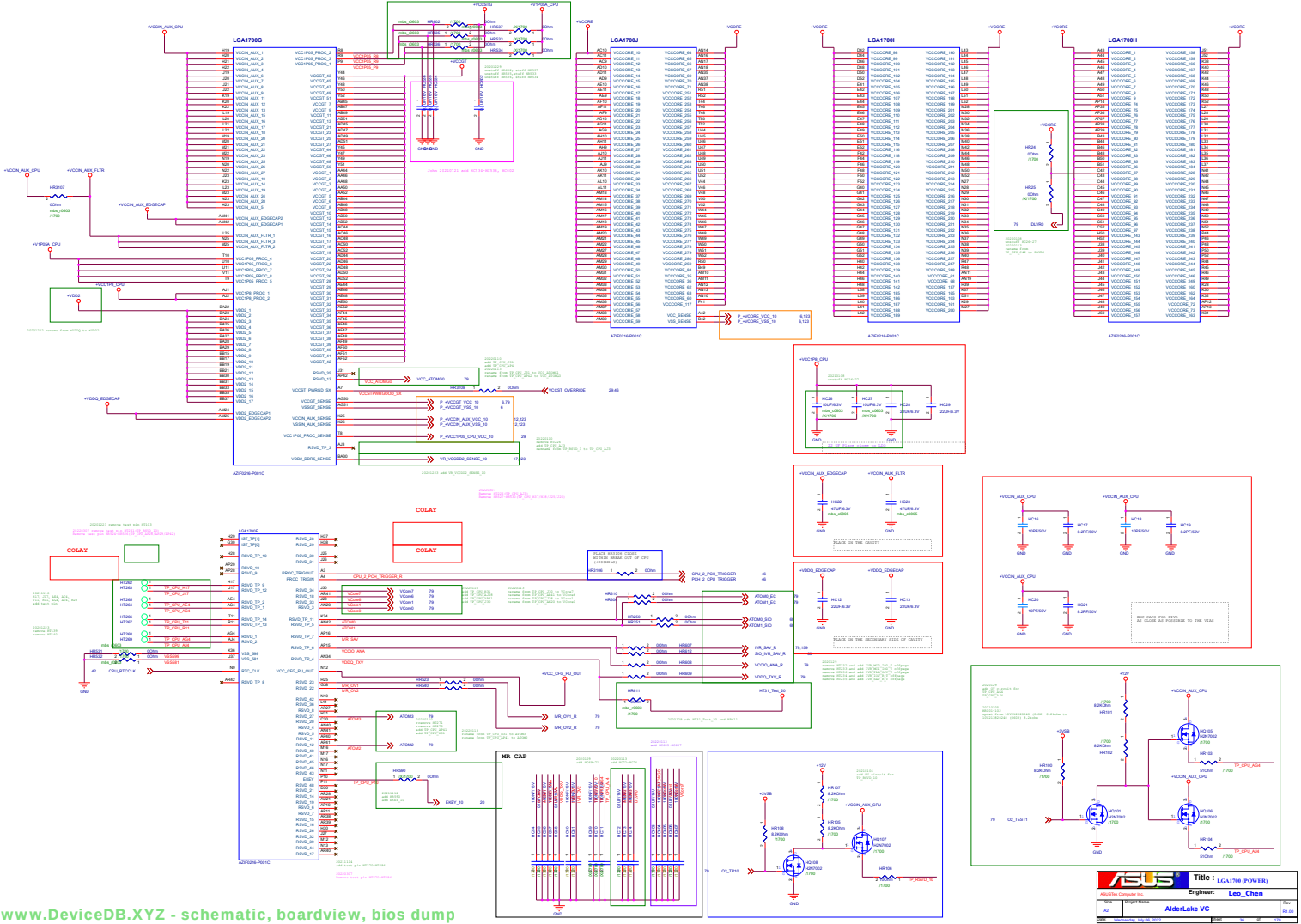


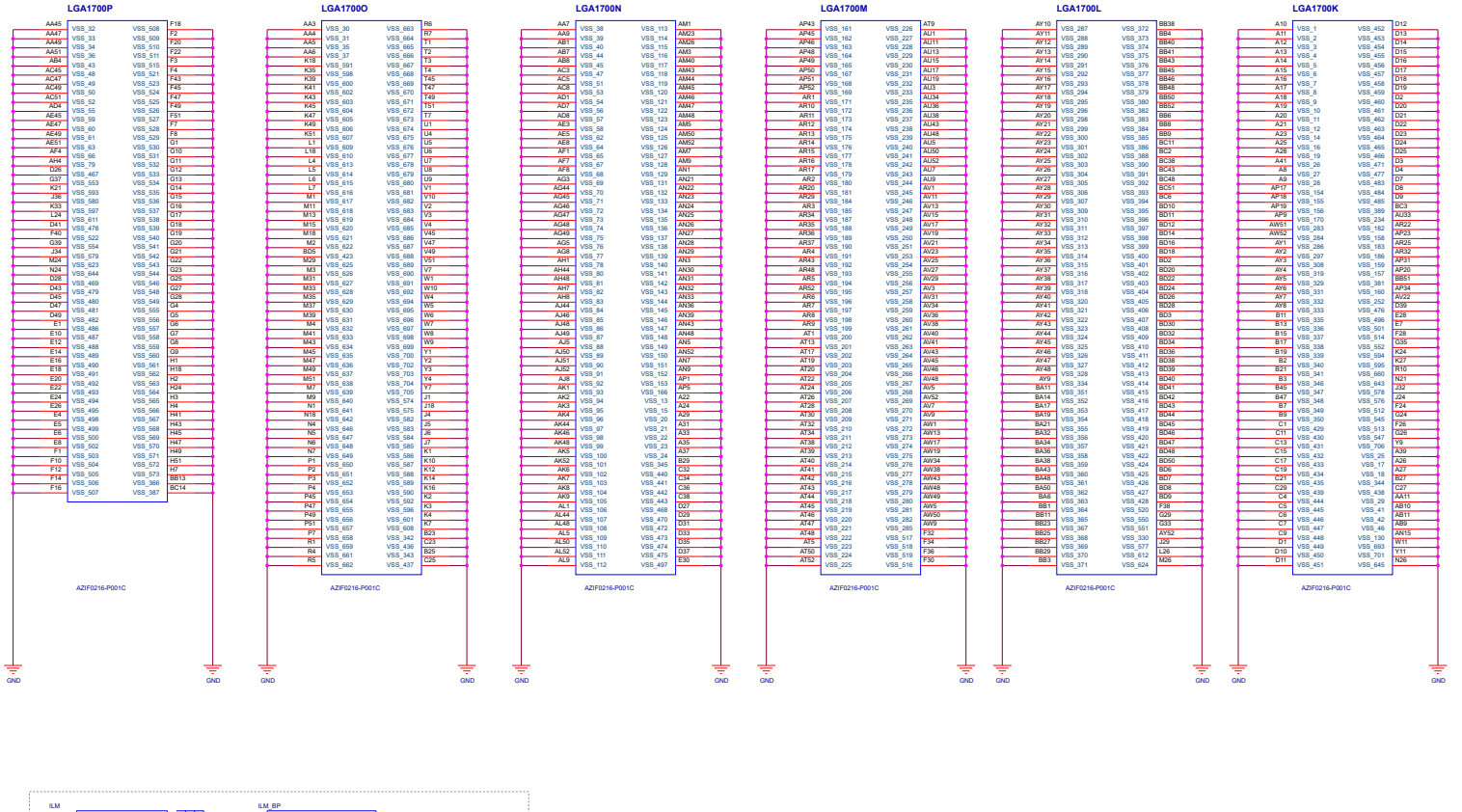
Title :	LGA1700 (DDR5_A Control)
Engineer:	Leo_Chen
Size	A2
Project Name	AlderLake VC
Rev	R1.03
Date:	Wednesday, July 06, 2022
Sheet	33 of 170

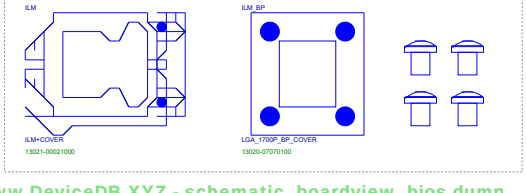


Title : LGA1700 (DDR5_B Control)			
ASUSTek Computer Inc.	Engineer: Leo_Chen		
Size: A2	Project Name: AlderLake VC		Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 34 of 170		

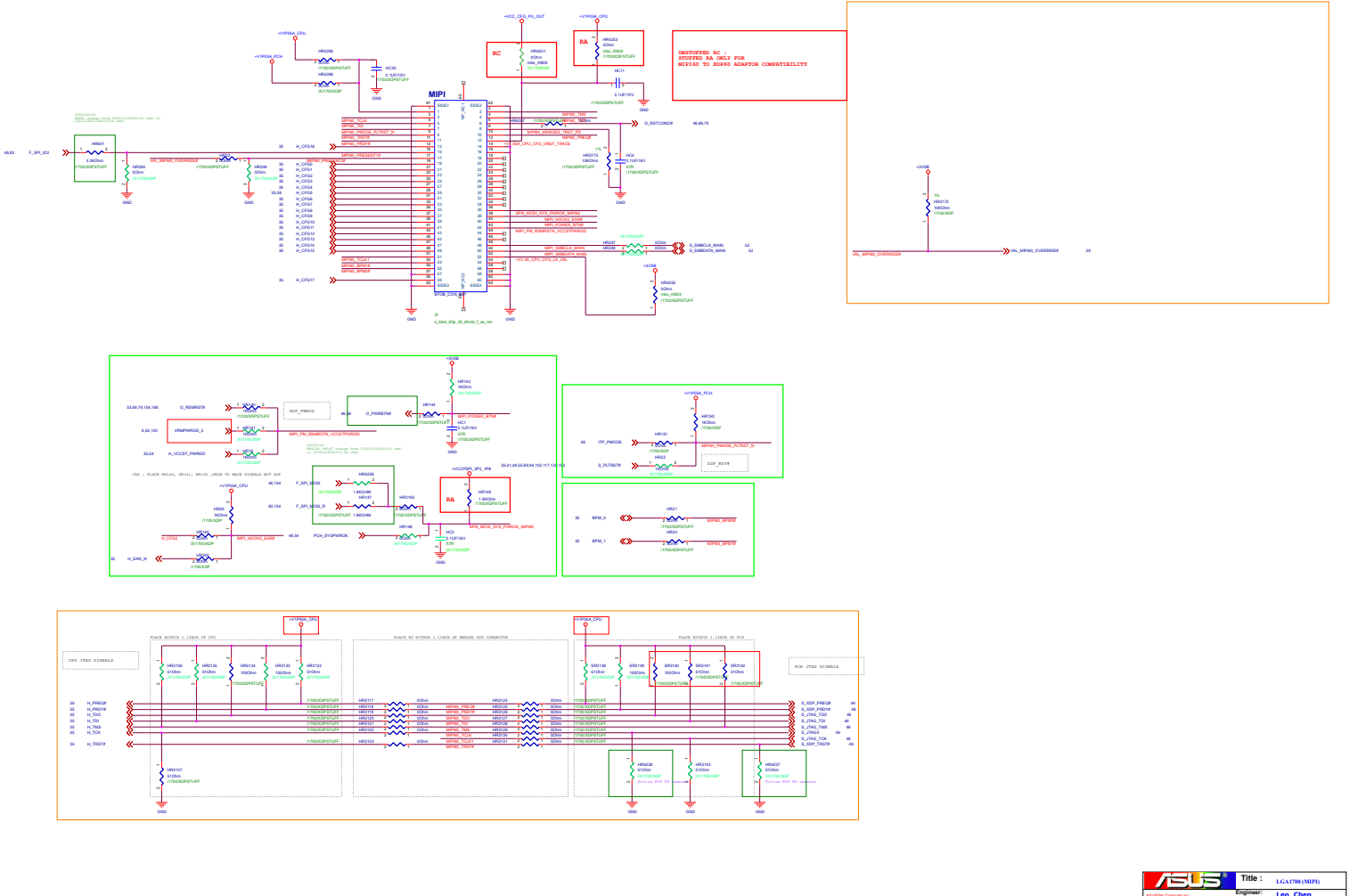


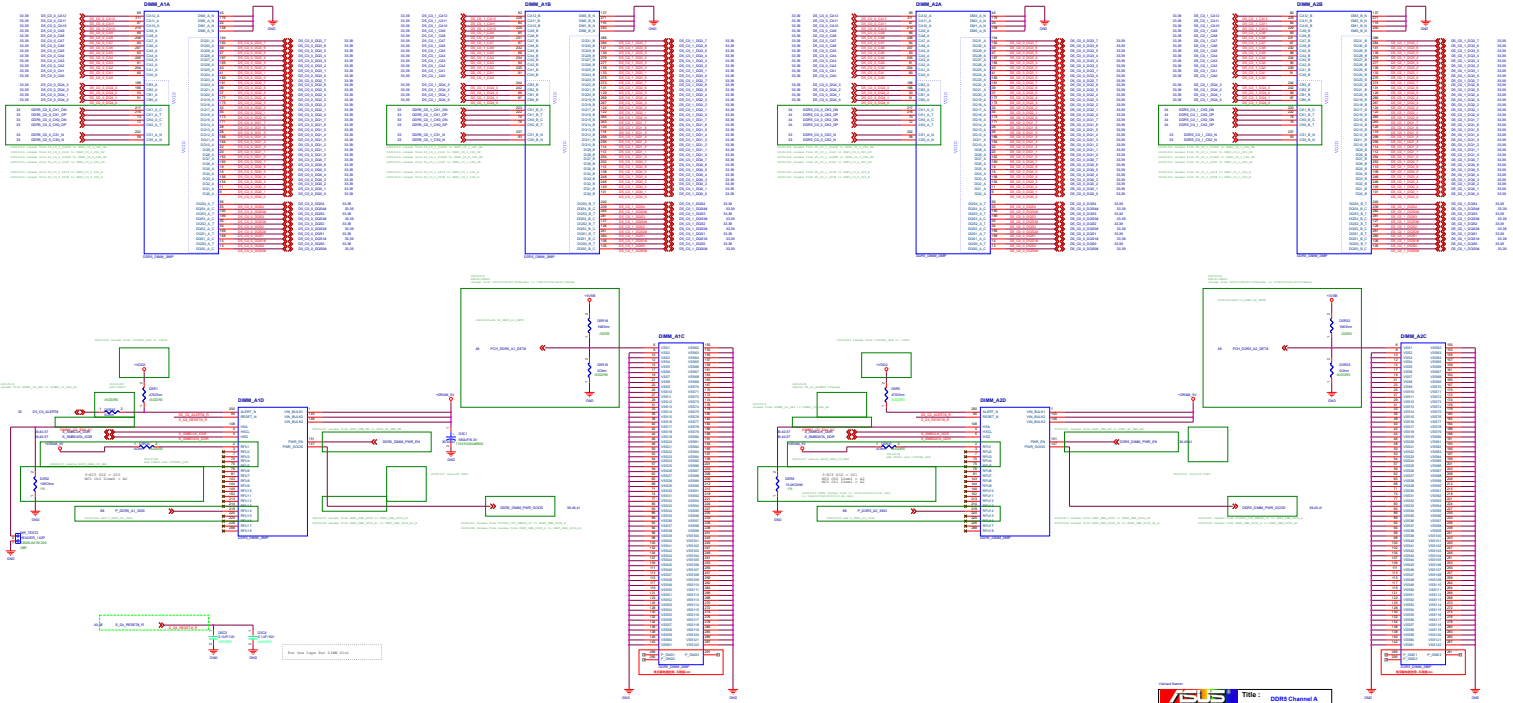


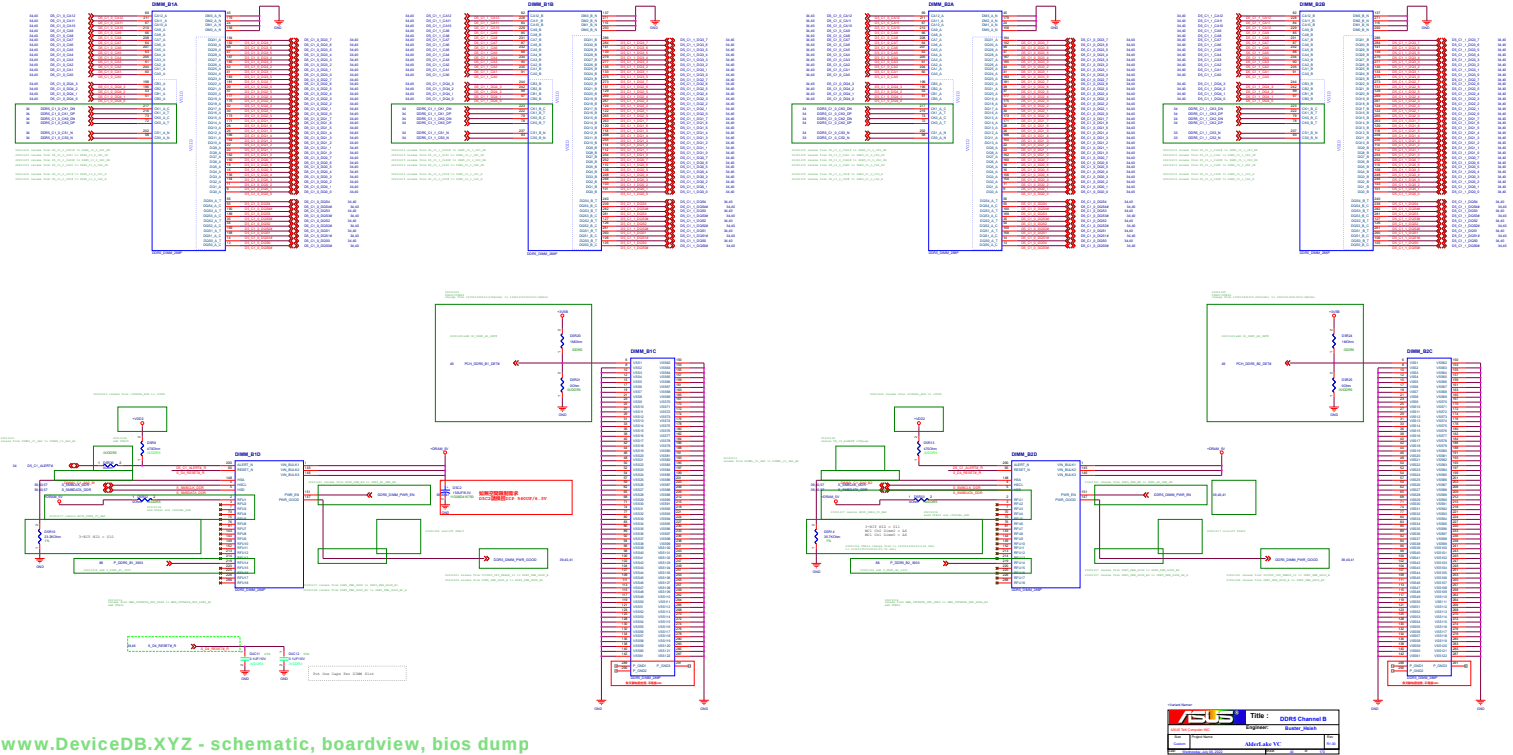


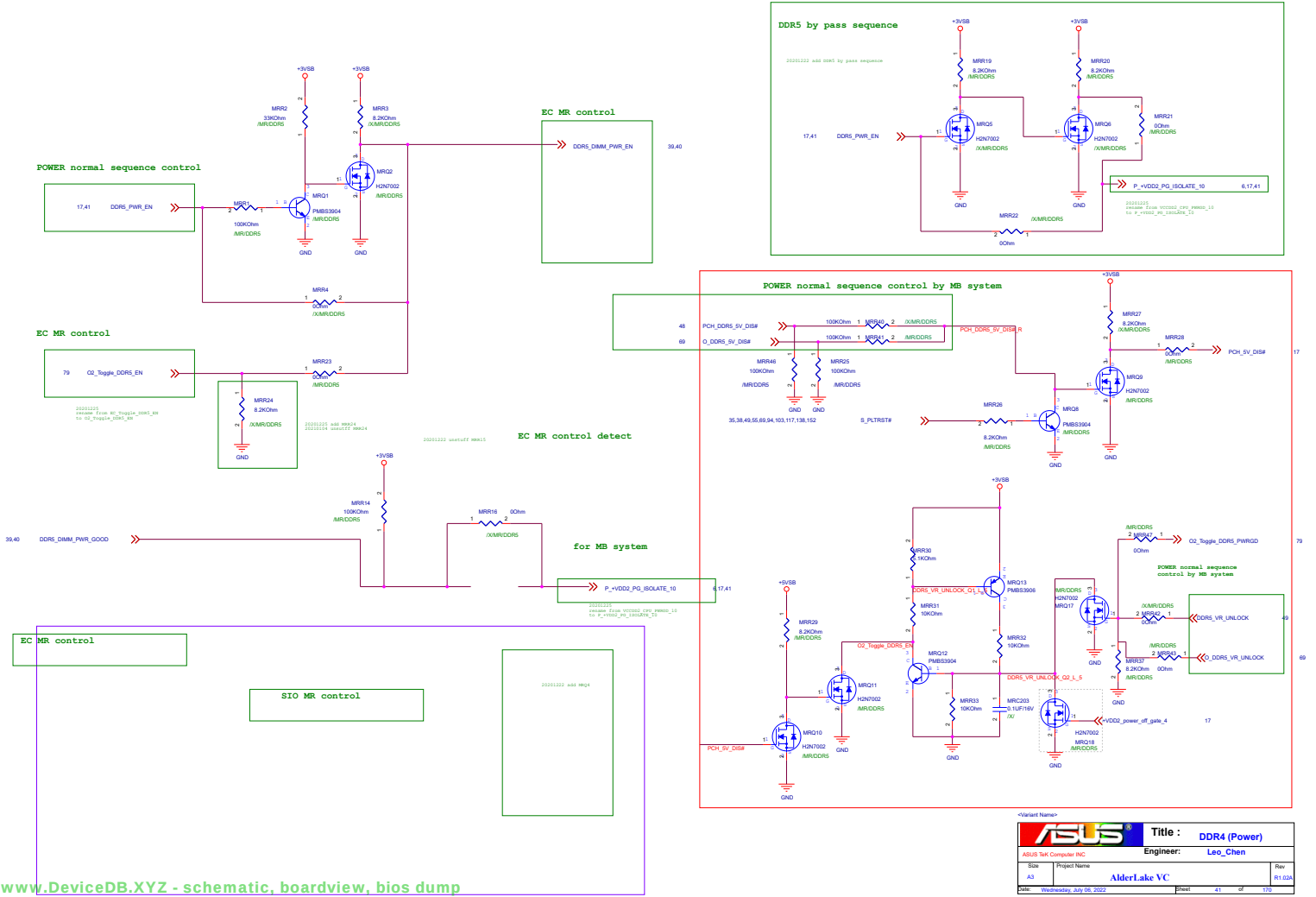


ASUSTeK Computer Inc.	Title :	LGA1700 (GND)	
	Engineer:	Leo_Chen	
Size: A3	Project Name: AlderLake VC		Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 37 of 170		

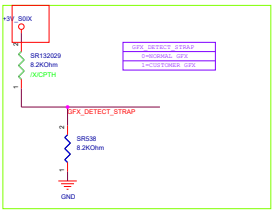




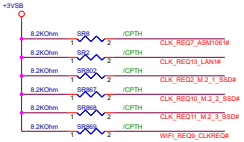


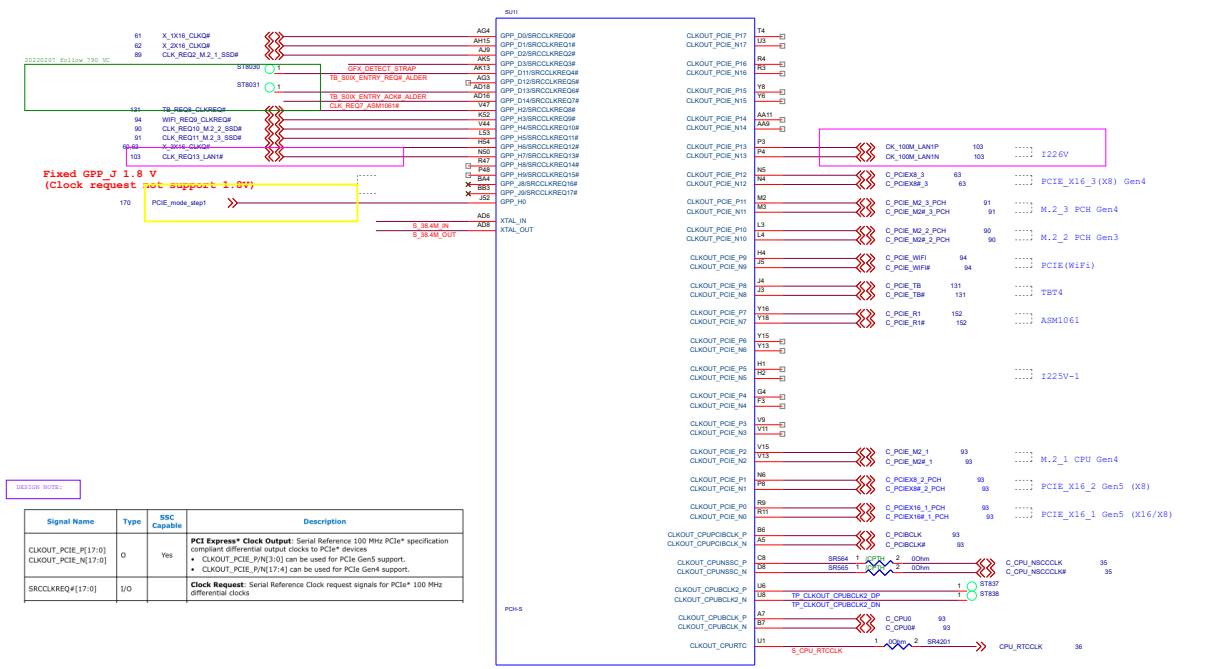


PCH PIN STRAP



PCH PU

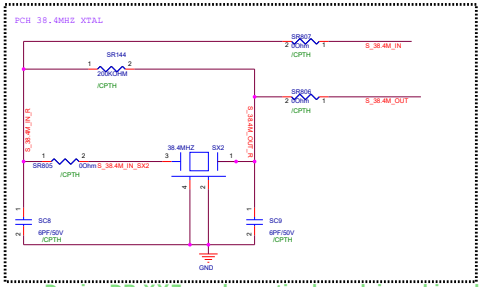




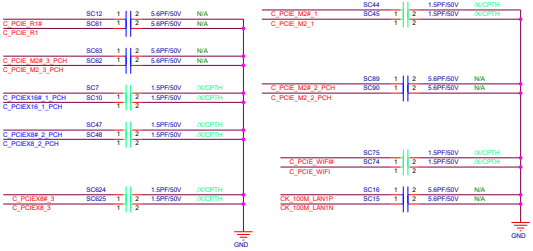
DESIGN NOTE:

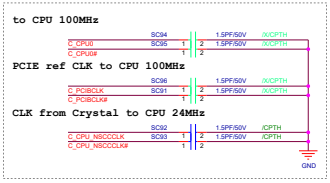
Signal Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[17:0] CLKOUT_PCIE_N[17:0]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N[3:0] can be used for PCIe Gen5 support. • CLKOUT_PCIE_P/N[17:4] can be used for PCIe Gen4 support.
SRCCLKREQ#[17:0]	I/O		**Clock Request**: Serial Reference Clock request signals for PCIe* 100 MHz differential clocks

PCH 38.4MHZ XTAL

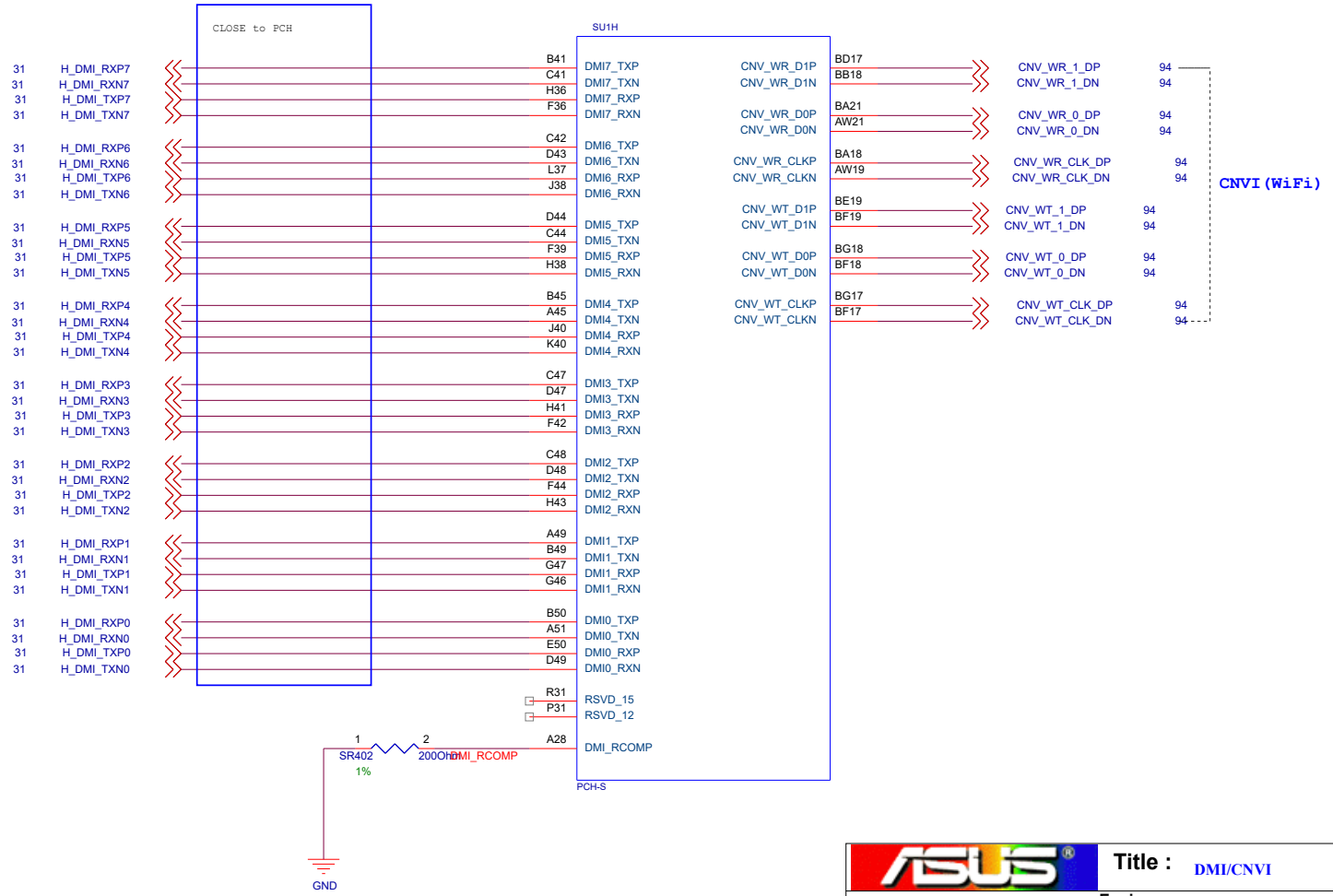


PEG 100MHz

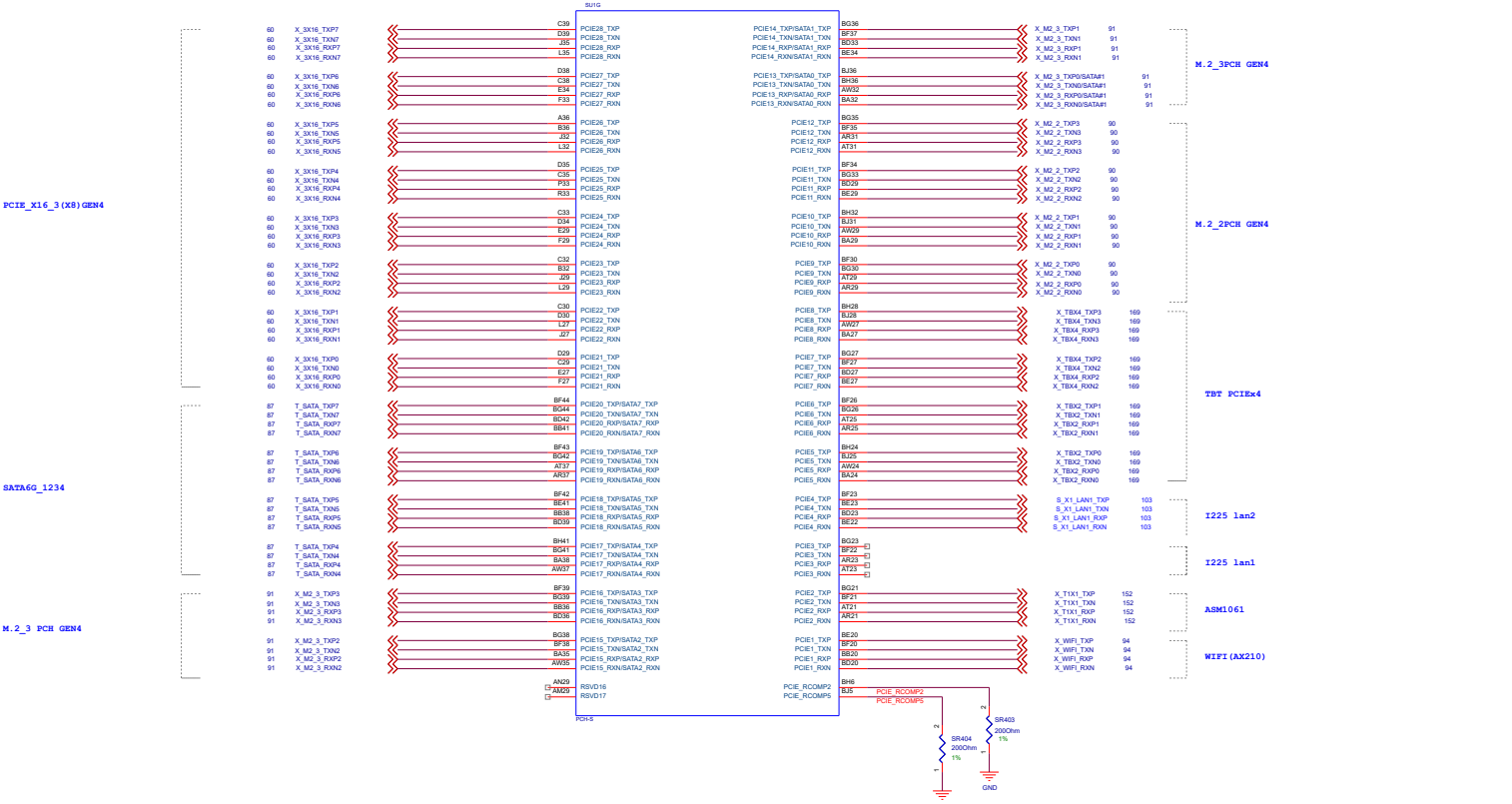




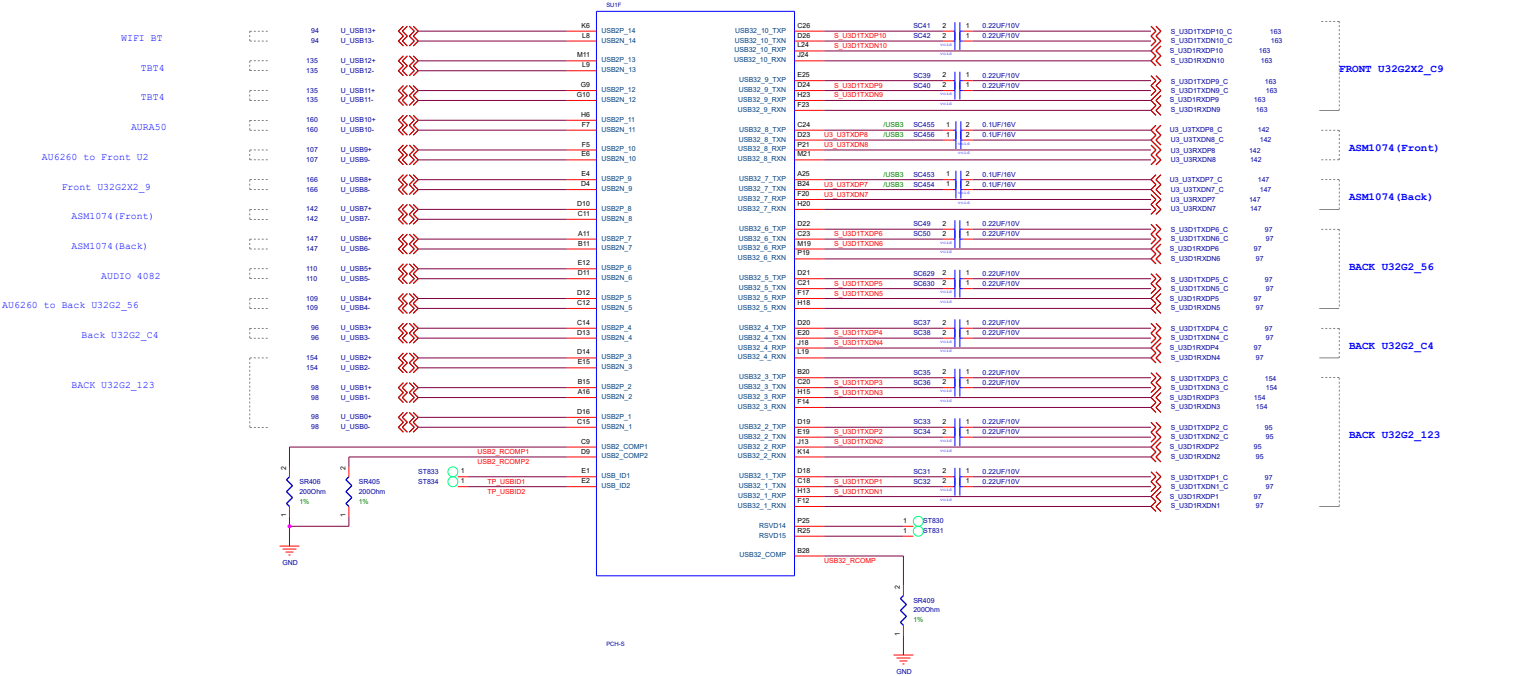
ASUSTek Computer Inc.	Title : CLOCK		
	Engineer: Leo_Chen		
Size: A3	Project Name: AlderLake VC		Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 42 of 170		



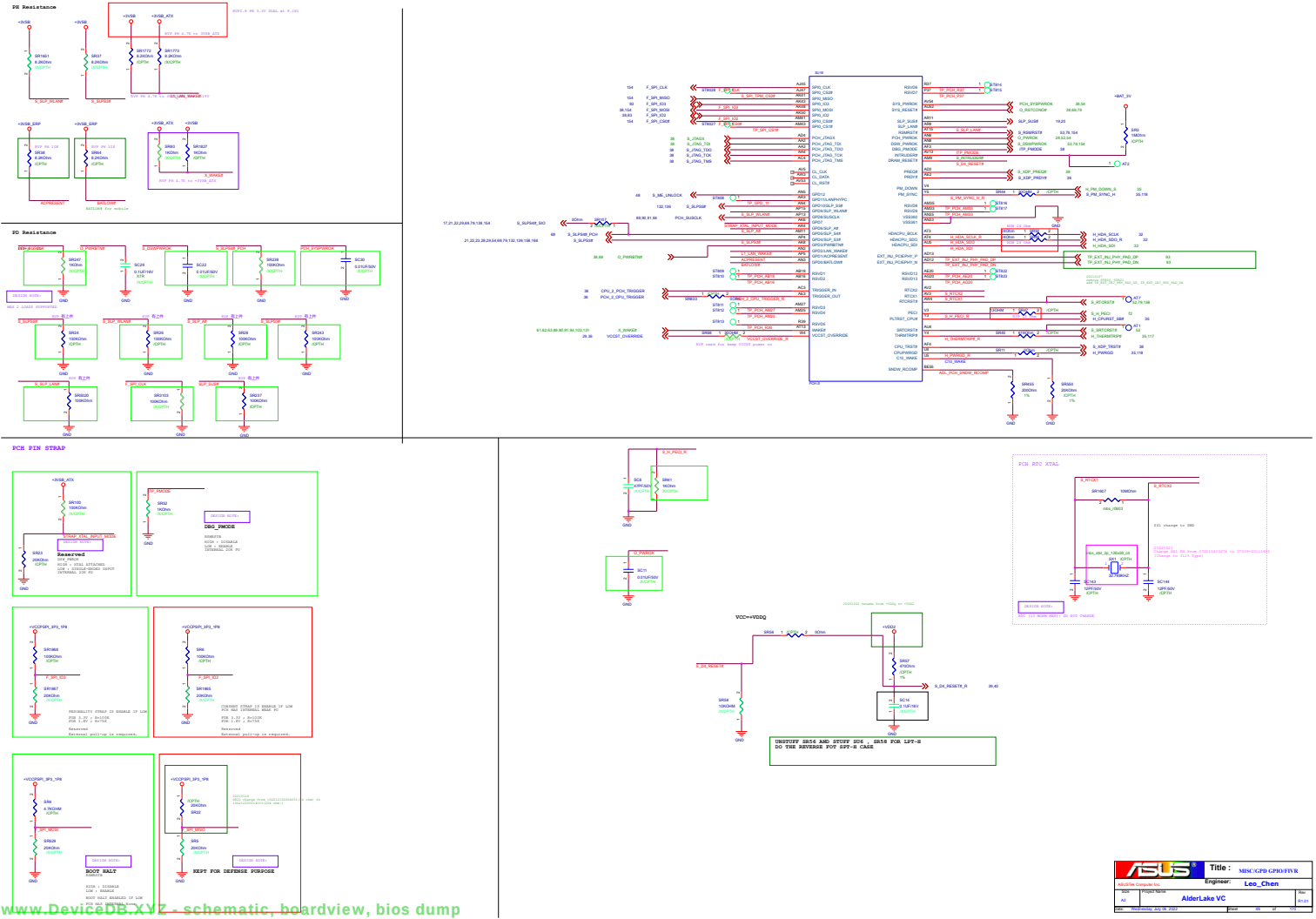
ASUSTek Computer Inc.	Title : DMI/CNVI		
	Engineer: Leo_Chen		
Size: A	Project Name: AlderLake VC		Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 43 of 170		

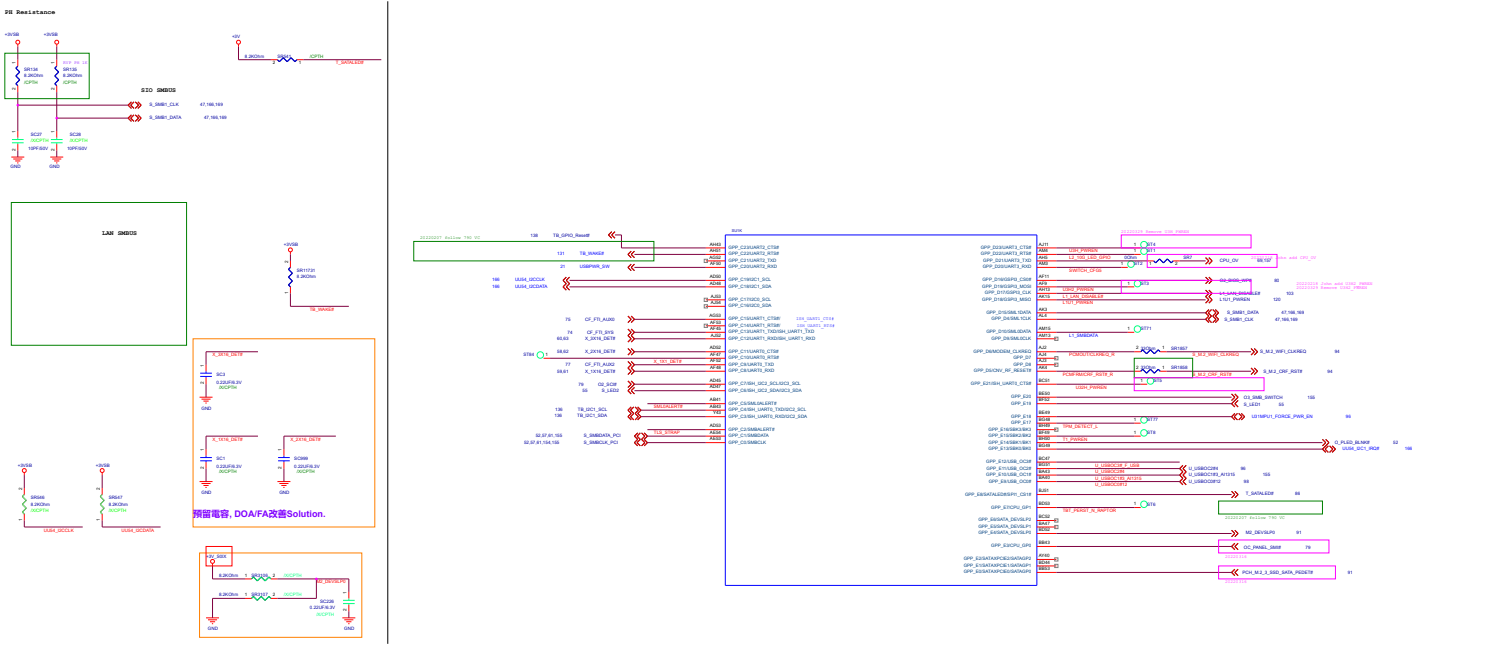


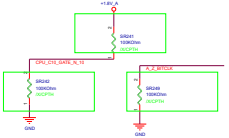
Title :	PCIE/SATA
Engineer:	Leo_Chen
ASUSTeK Computer Inc.	
Size	A3
Project Name	AlderLake VC
Rev	R1.01
Date:	Wednesday, July 06, 2022
Sheet	44 of 170

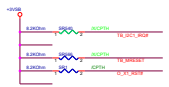


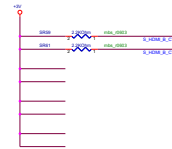
ASUSTek Computer Inc.	Title : USB	
	Engineer: Leo_Chen	
Size: A3	Project Name: AlderLake VC	Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 45 of 170	





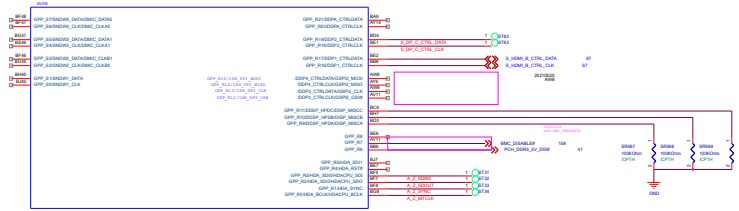






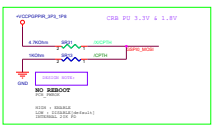
PORT	HPD	DDC
EDP(DDIA)	DDSP_HPDA	N/A
DDIB	DDSP_HPD1	DDP1 (CLK, DATA)
DDIC	DDSP_HPD2	DDP2 (CLK, DATA)
DDID	DDSP_HPD3	DDP3 (CLK, DATA)
DDIE	DDSP_HPD4	DDP4 (CLK, DATA)

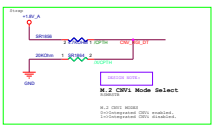
GPP_S Only 1.8 V

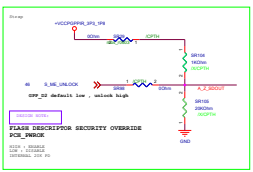


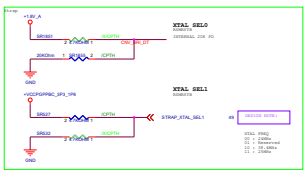
Fixed GPP_J 1.8 V

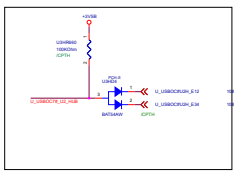
PCH PIN STRAP

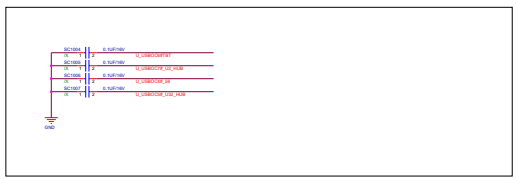




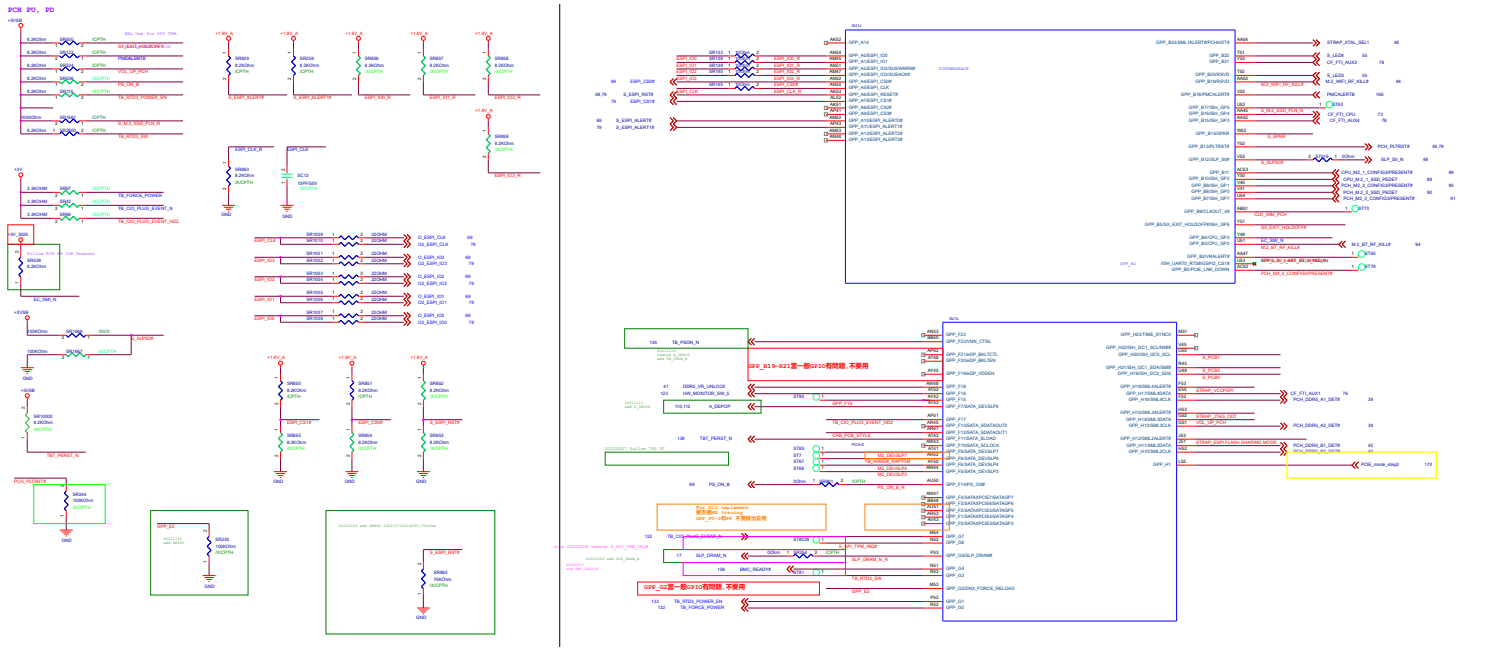


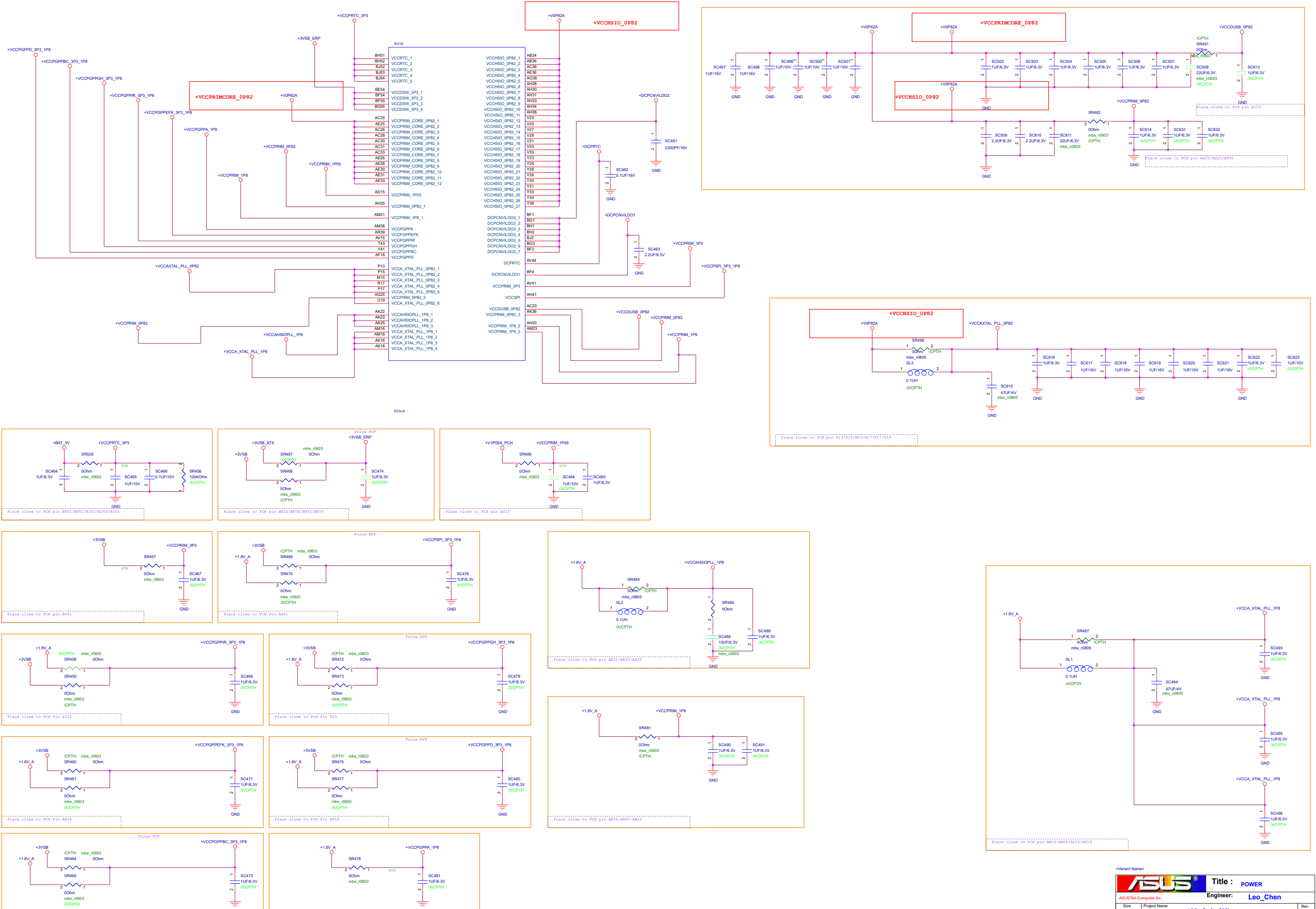






ASUSTeK Computer Inc.	Title :	GPIO_J_J_K_R_SCNVI	
	Engineer:	Leo_Chen	
Size: A2	Project Name:	AlderLake VC	Rev: 01.01
Date: Wednesday, July 06, 2022	Sheet: 49	of: 170	





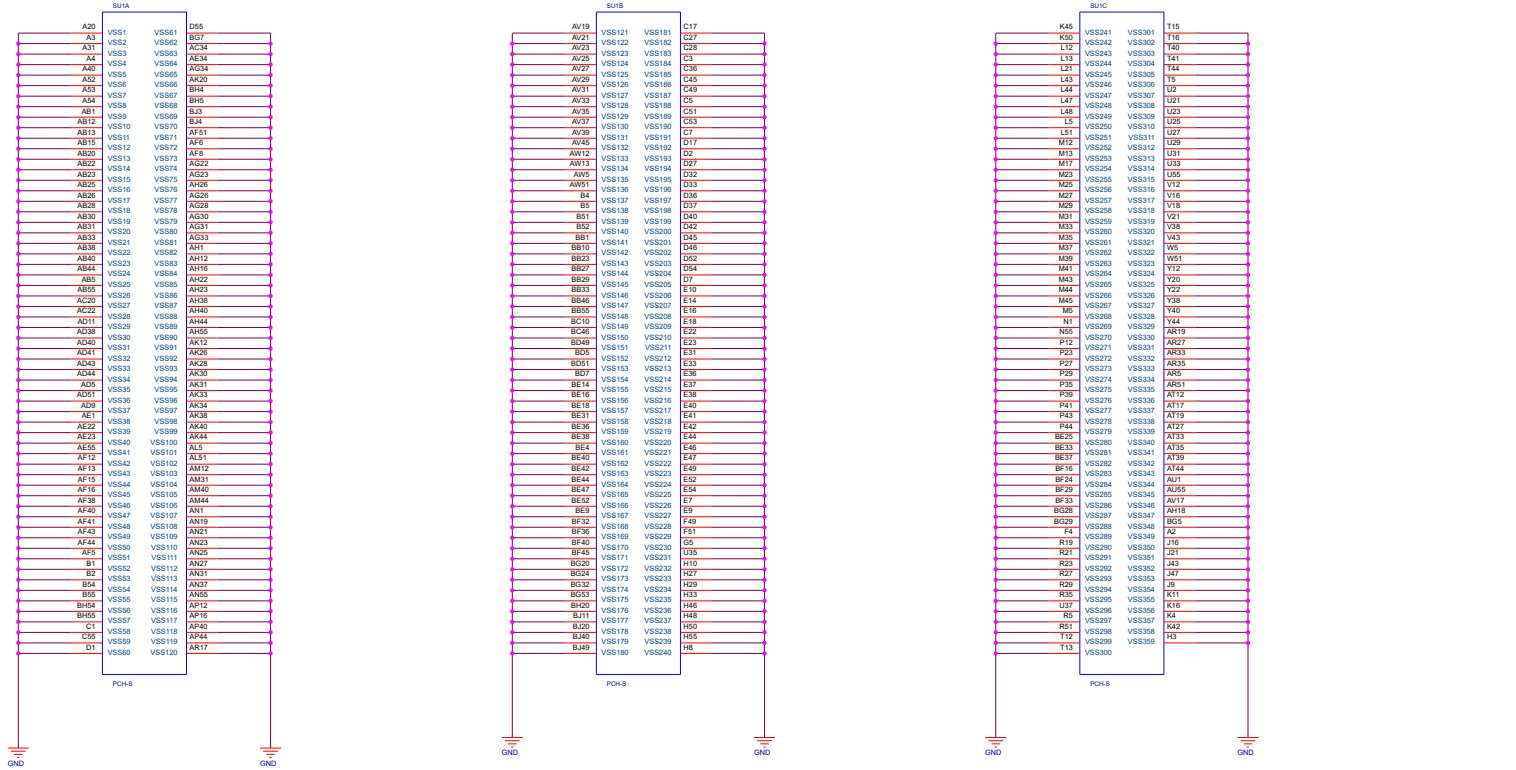
Title : POWER

Engineer: Leo_Chen

ASUSTek Computer Inc.

Size	Project Name	Rev
A2	AlderLake VC	1P6

Date: Wednesday, July 06, 2022 Sheet 50 of 170



<Variant Name>

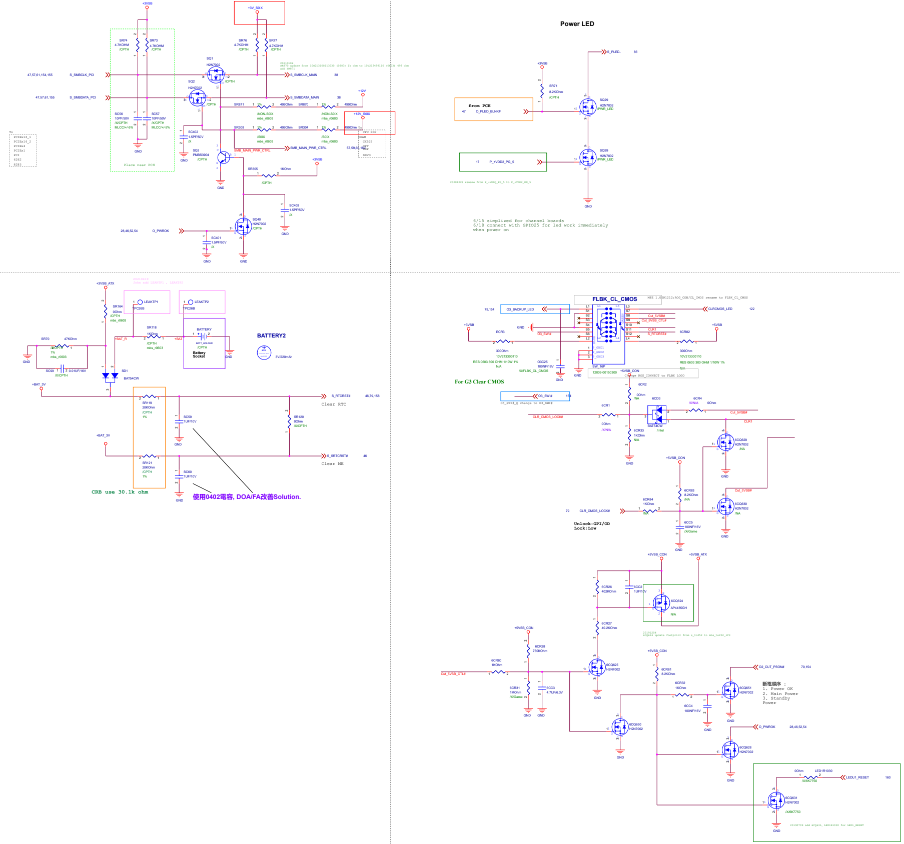
ASUSTek Computer Inc.

Title : GND

Engineer: Leo_Chen

Size	Project Name	Rev
A3	AlderLake VC	1P6

Date: Wednesday, July 06, 2022 Sheet 51 of 170



Title : CPTH (SMBUS/CLRTC)

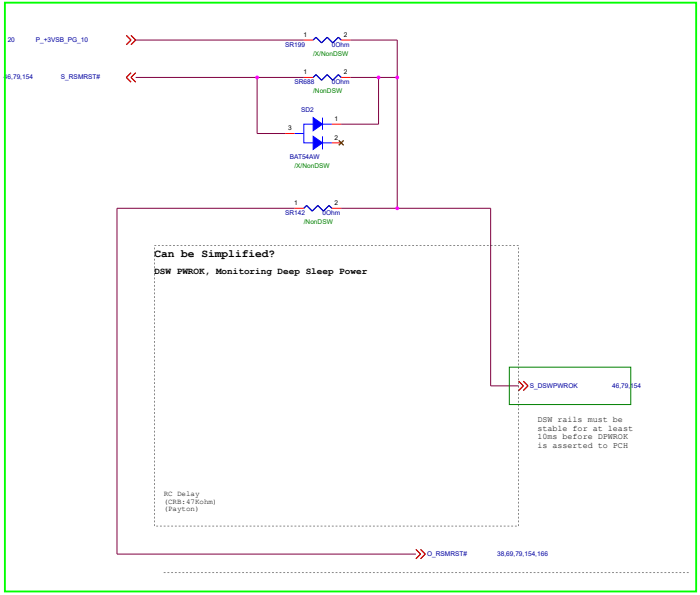
Engineer: Leo_Chen

ASUSTek Computer Inc.

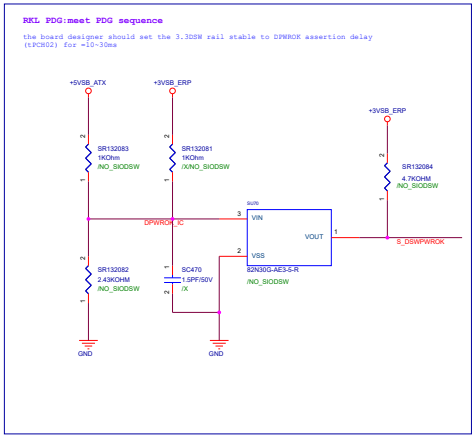
Project Name: AlderLake VC

Size A1 | Rev R1.01

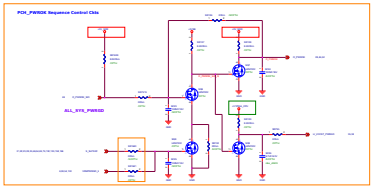
Date: Wednesday, July 06, 2022 | Sheet 52 of 170

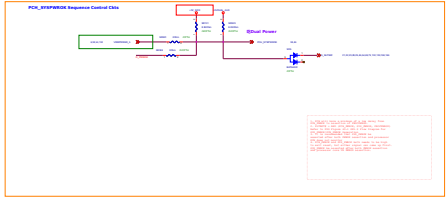


BackFeed Cut DSW &
Backfeed Cut Logic



ASUSTek Computer Inc.	Title : SPTH (DSW SEQUENCE)		
	Engineer: Leo_Chen		
Size: A3	Project Name: AlderLake VC		Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 53 of 170		

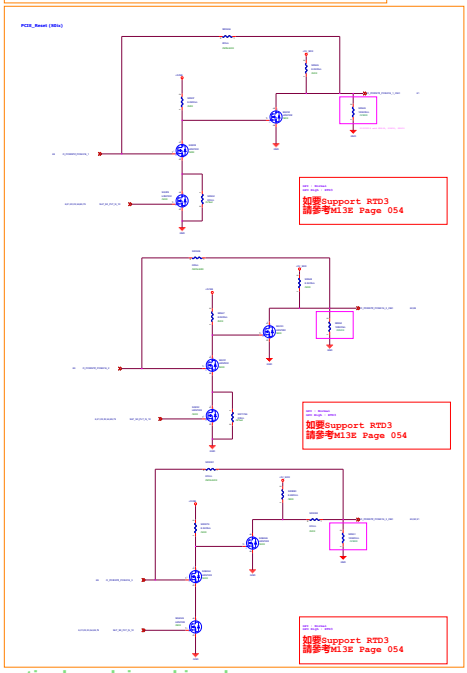


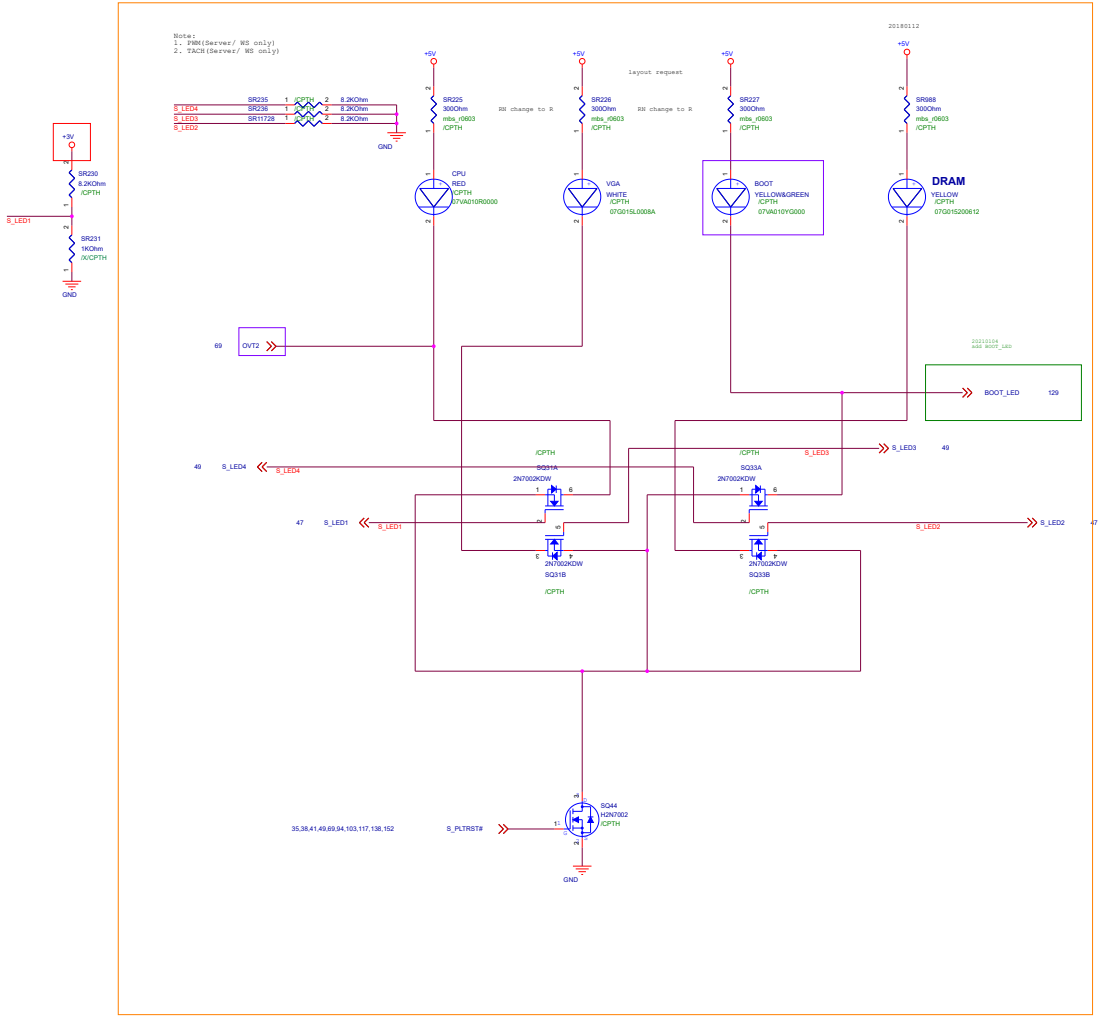


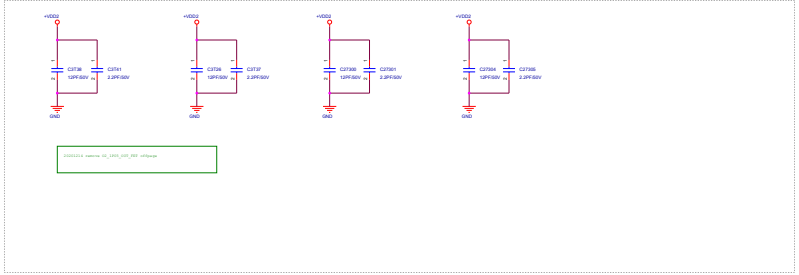
VCCST_PWRGD Sequence Control Chits

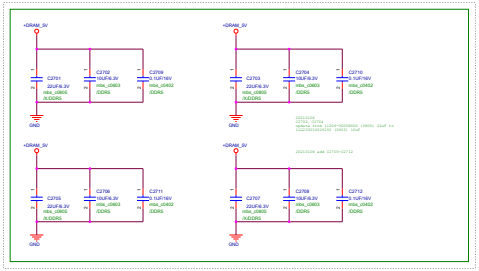
SUSx Sequence Control Chits

PS_ONJ Logic

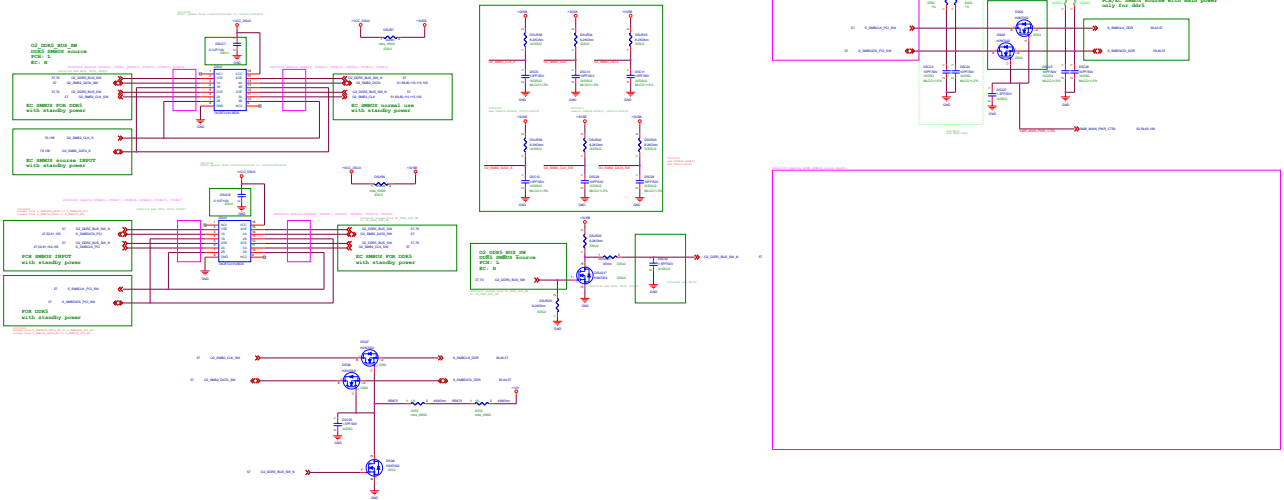


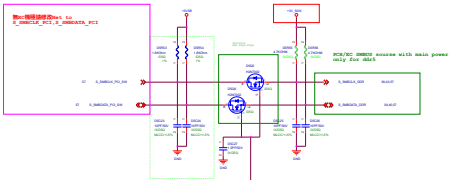


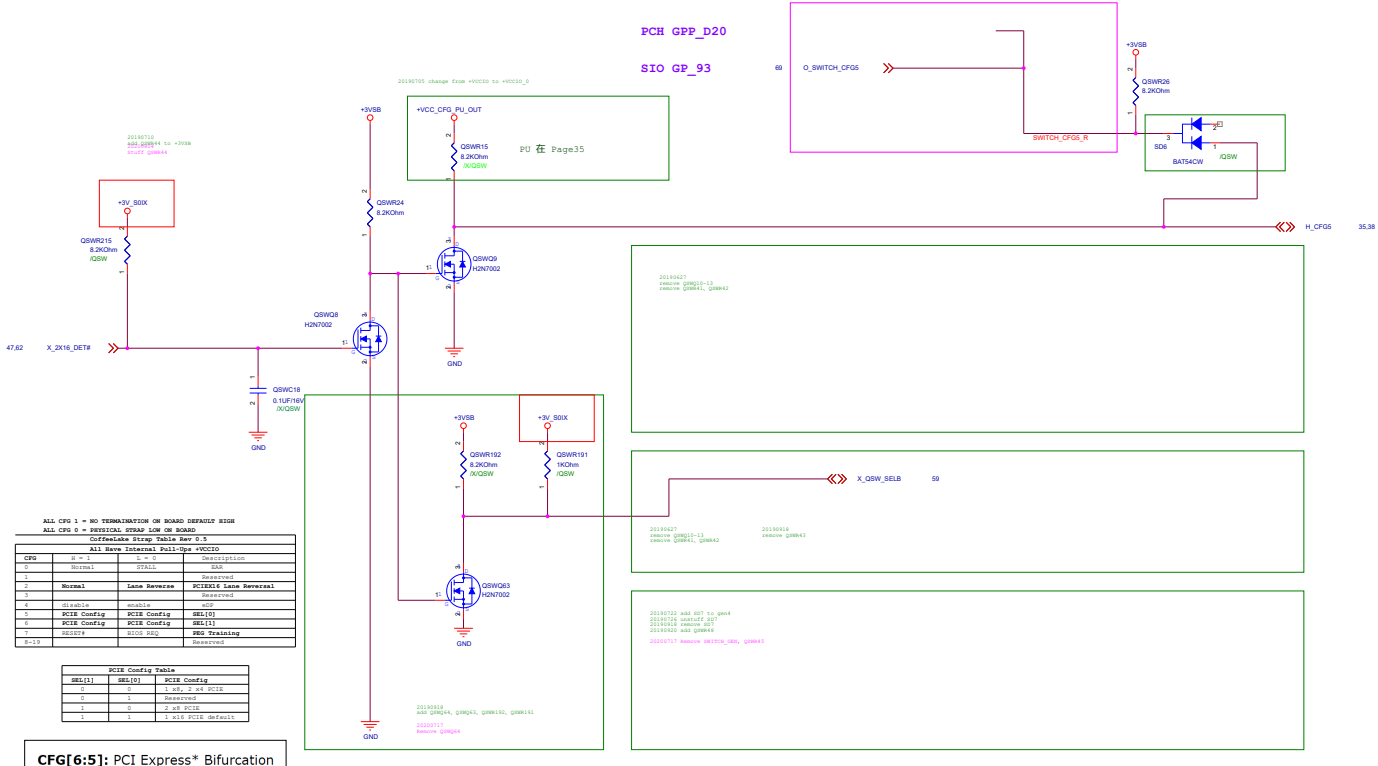




無EC機種請刪除此橘框，並將077頁的O2_SMB2_CLK_S, O2_SMB2_DATA_S
修改成O2_SMB2_CLK, O2_SMB2_DATA_S







ALL CFG 1 = NO TERMINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD

CoffeeLake Strap Table Rev 0.5
All Have Internal Pull-Ups +VCCIO

CFG	1 = 1	1 = 0	Description
0	Normal	STALL	EAB
1			Reserved
2	**Normal**	**Lane Reverse**	**PCIEX16 Lane Reversal**
3			Reserved
4	disable	enable	eDP
5	**PCIE Config**	**PCIE Config**	**SEL[0]**
6	**PCIE Config**	**PCIE Config**	**SEL[1]**
7	RESET#	BIOS REQ	**PEG Training**
8-19			reserved

PCIE Config Table

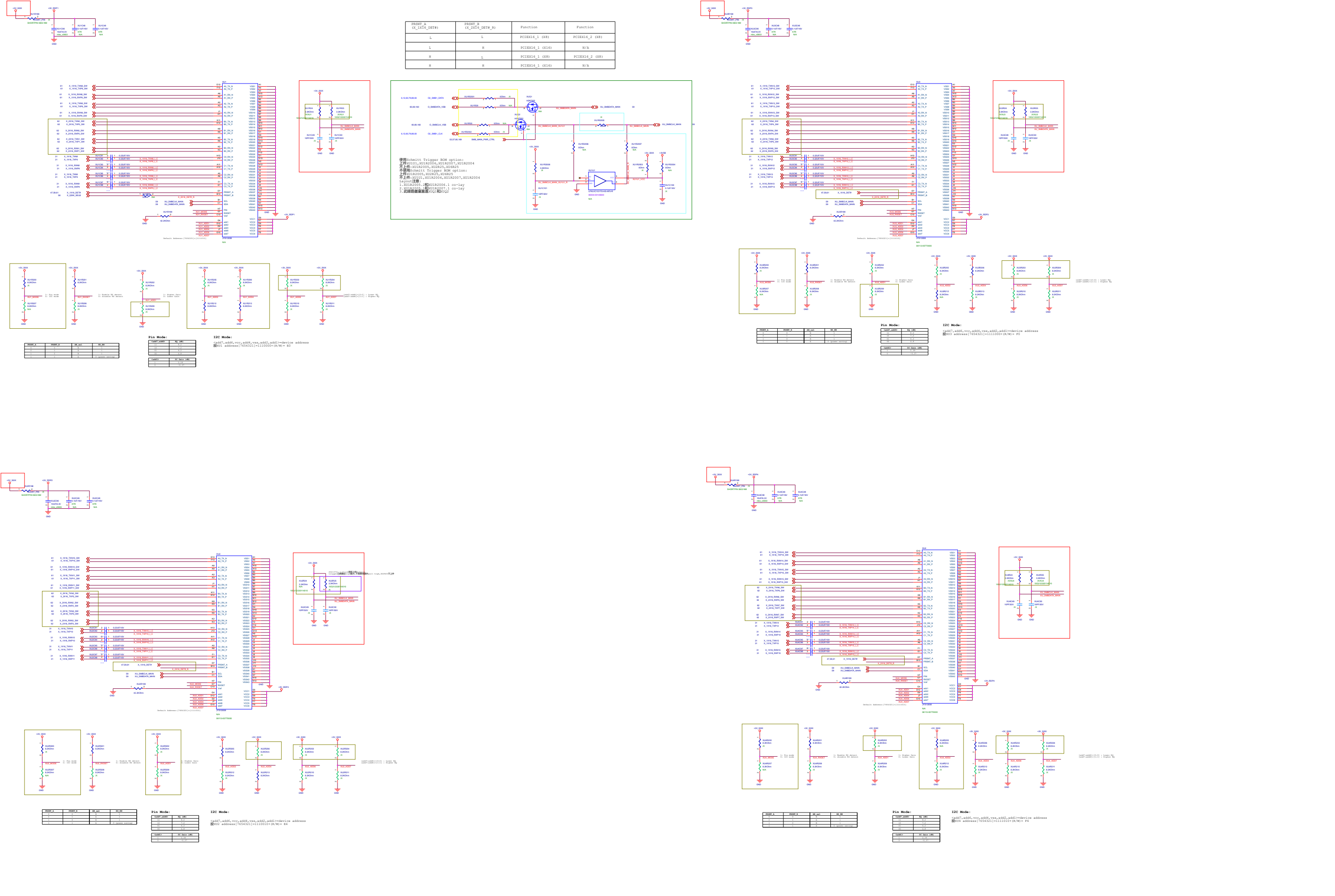
SEL[1]	SEL[0]	PCIE Config
0	0	1 x8, 2 x4 PCIE
0	1	Reserved
1	0	2 x8 PCIE
1	1	1 x16 PCIE default

CFG[6:5]: PCI Express* Bifurcation
- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = 1 x16 PCI Express*

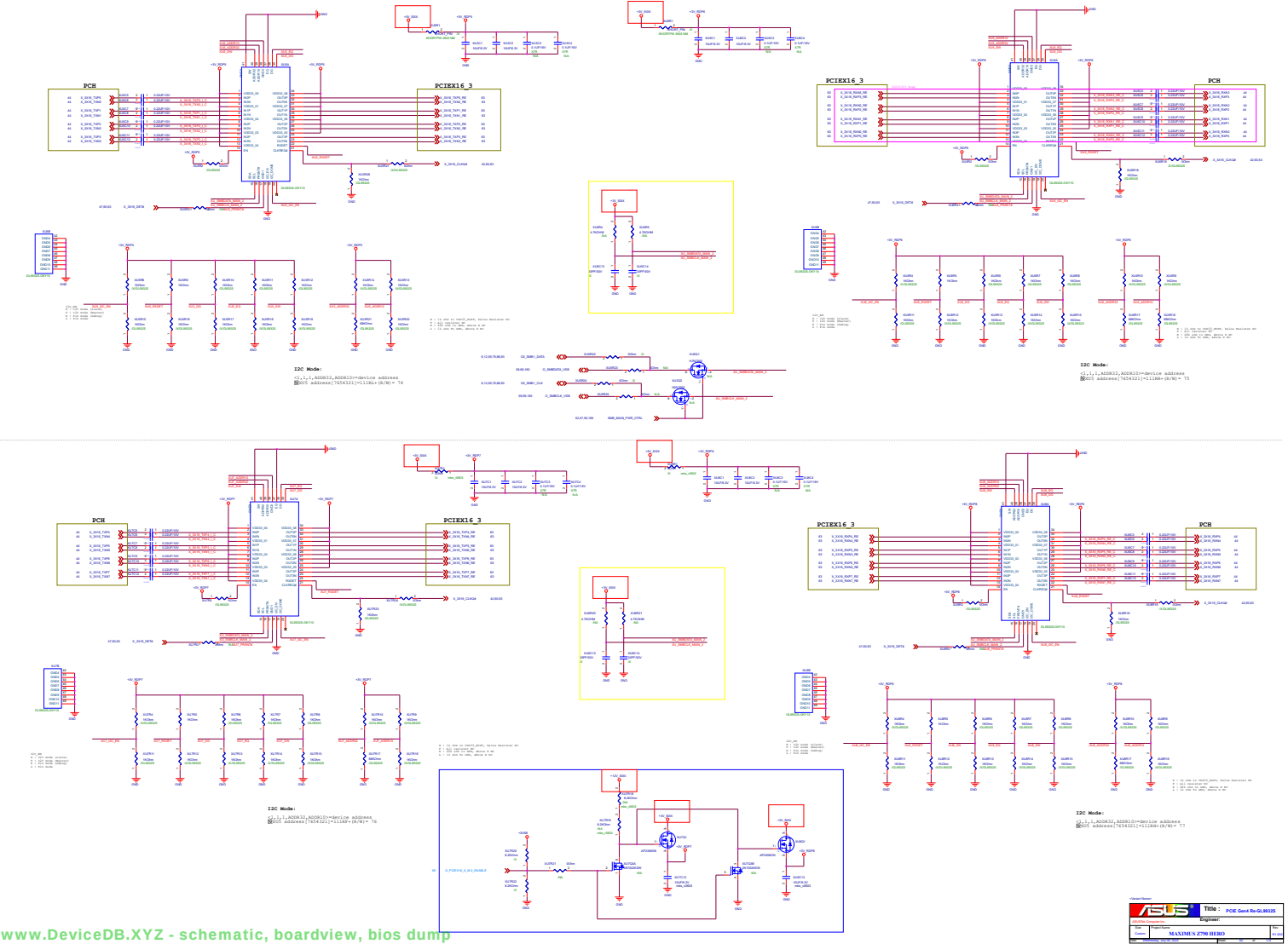
X_2X16_DET#

<Variant Name>

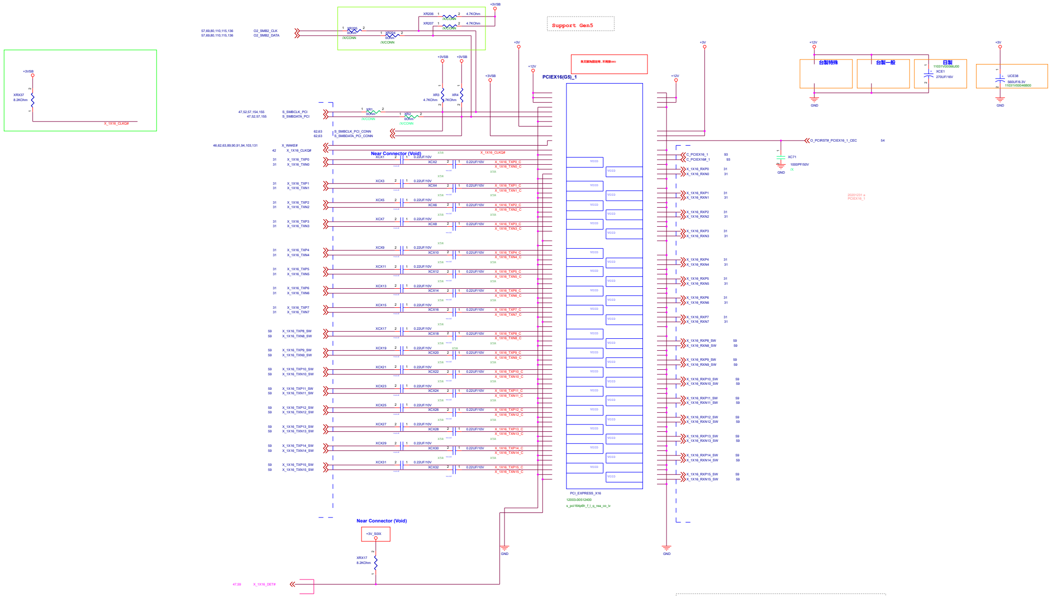
ASUSTeK COMPUTER INC.	Title :	QUICK SWITCH(PCIEX16_1)
	Engineer:	Aaron_Su
Size: A3	Project Name: Maximus XI Extreme	Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 55 of 170	



PRSNT_A (X_1X16_DET#)	PRSNT_B (X_2X16_DET#_R)	Function	Function
L	L	PCIEX16_1 (X8)	PCIEX16_2 (X8)
L	H	PCIEX16_1 (X16)	N/A
H	L	PCIEX16_1 (X8)	PCIEX16_2 (X8)
H	H	PCIEX16_1 (X16)	N/A



如要Support RTD3
請參考M13E Page049,065



	SLOT 顏色
PCIEX16_1	LIGHT GRAY

X_WAKE#

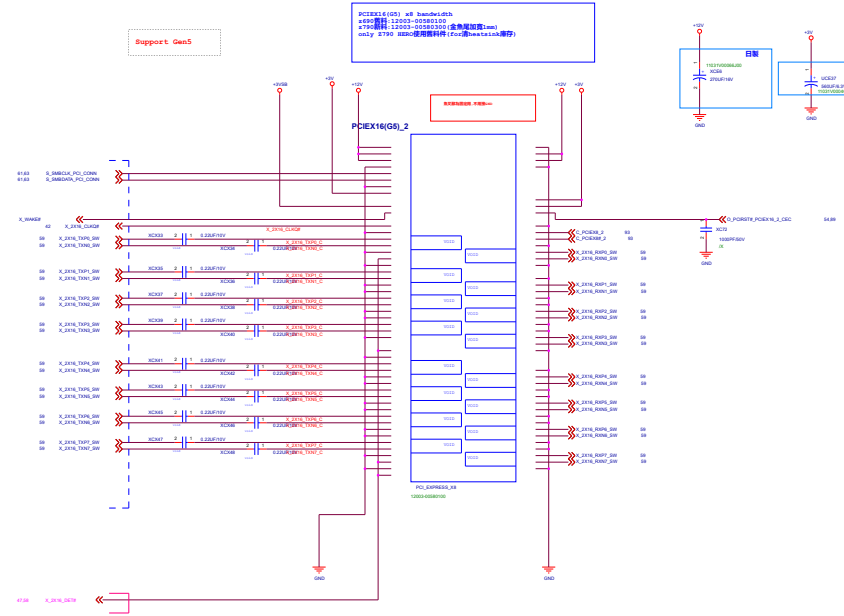
需在SB端Pull-high

PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請將PIN B17,B31,B48,B81 netname 改為X_1X16PRSNT#.
不使用此功能,且不support SLOT_WARN & SDVO線路（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17,B31,B48,B81 netname 改為GND.
Only support SDVO線路	PIN B17 --> X_SDVO_CLK PIN B31 --> X_SDVO_DATA PIN B48 --> X_EXP_SM

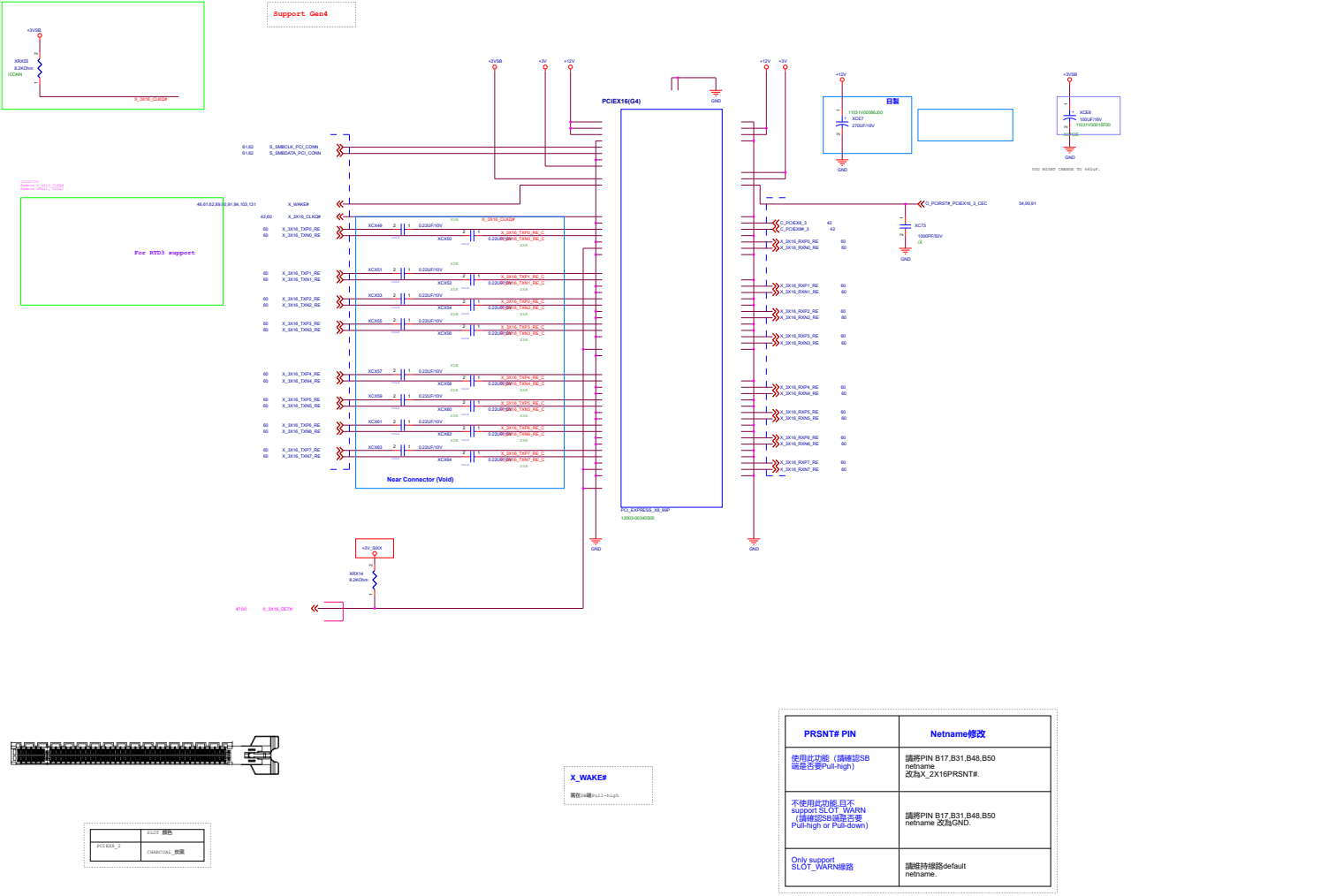
<Variant Name>

ASUSTek Computer Inc.	Title : PCIEX16_1(LIGHT GRAY)		
	Engineer: Martino_Yang		
Size A1	Project Name CometLake VC		Rev 3.1
Date: Wednesday, July 06, 2022	Sheet 61	of 170	

如要Support RTD3
請參考M13E Page049,066



PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請將PIN B17,B31,B48,B50 netname 改為X_2X16PRSNT#.
不使用此功能,且不support SLOT_WARN（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17,B31,B48,B50 netname 改為GND.
Only support SLOT_WARN線路	請維持線路default netname.



PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請將PIN B17,B31,B48,B50 netname 改為X_2X16PRSNT#.
不使用此功能,且不support SLOT_WARN（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17,B31,B48,B50 netname 改為GND.
Only support SLOT_WARN線路	請維持線路default netname.

X_WAKE#

需在SB端Pull-high

	SLOT 顏色
PCIEX8_2	CHARCOAL_炭黑

<Variant Name>

ASUSTeK Computer Inc.

Title : PCIEX4_3(BLACK_黑)

Engineer: Aaron_Su

Size: A2 | Project Name: Maximus XI Extreme | Rev: 0.01

Date: Wednesday, July 08, 2020 | Sheet 68 of 134

3.2

PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請維持線路default netname.
不使用此功能（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17 netname改為GND.

PCIEX1	SLOT 顏色 BLACK

<Variant Name>

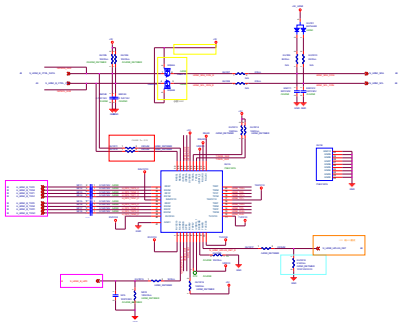
ASUSTeK Computer Inc.

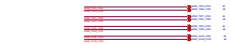
Title : PCIEX1 (BLACK)

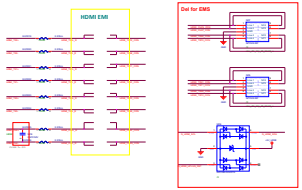
Engineer: Aaron_Su

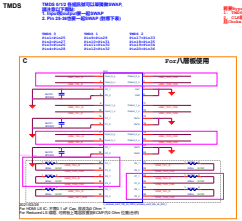
Size	Project Name	Rev
A2	Maximus XI Extreme	0.01

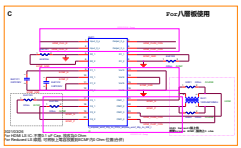
Date: Wednesday, July 08, 2020 Sheet 64 of 150

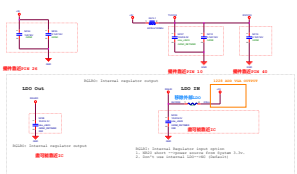


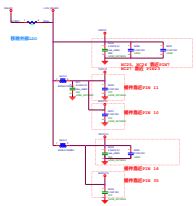






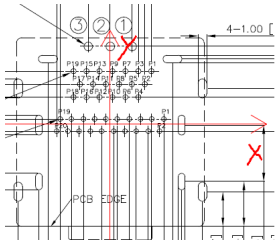




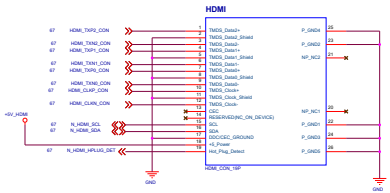


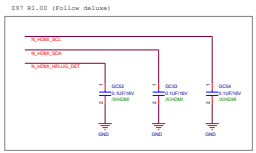
FOLLOW X570 ProArt

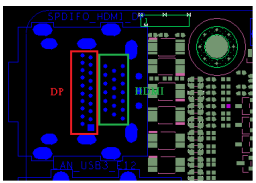
2016.03.30 Remove VGA Connector

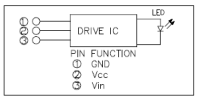


HDMI2.0





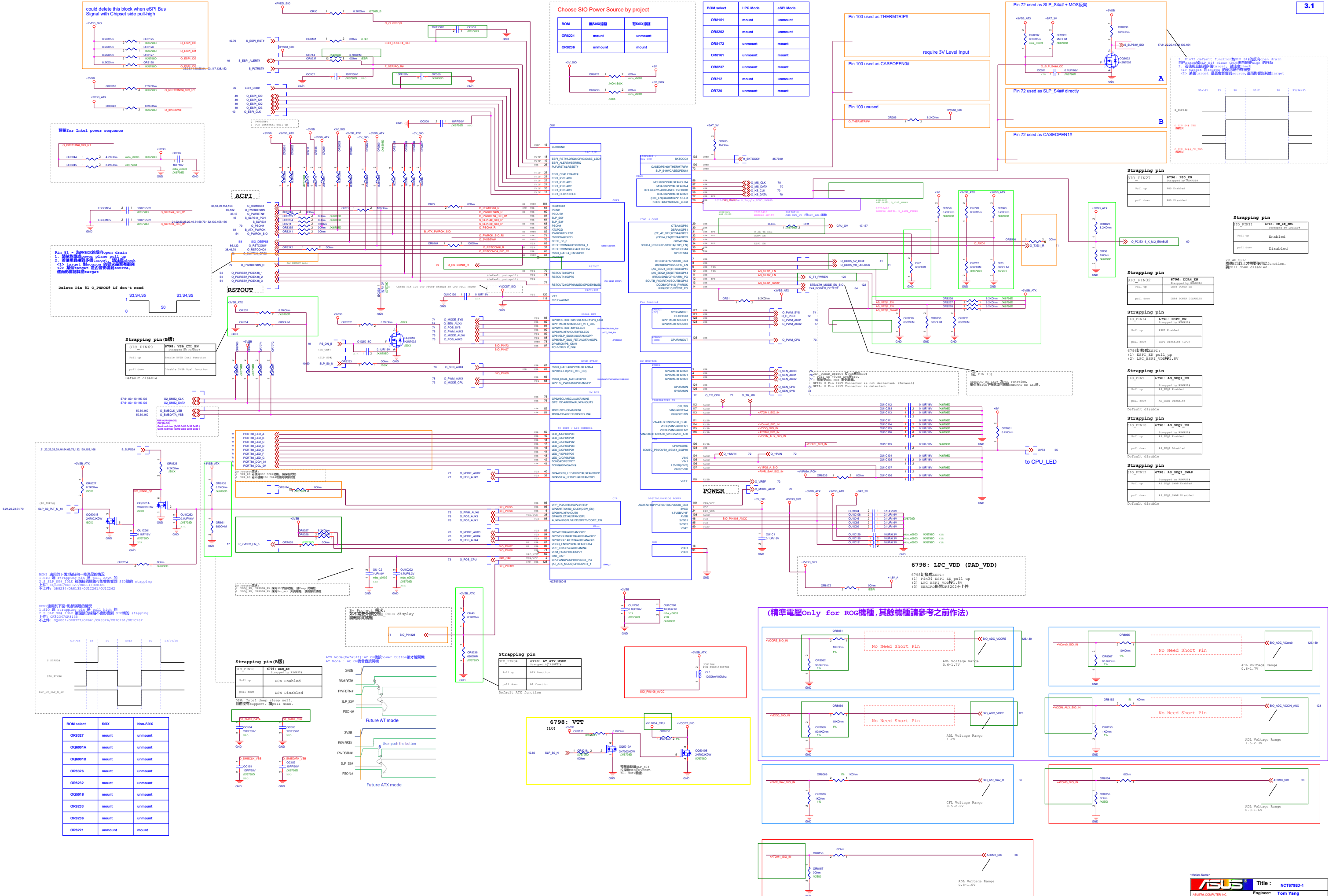




7. HDMI AND DP PIN ASSIGNMENTS:

HDMI			
PIN NO.	SIGNAL ASSIGNMENT	PIN NO.	SIGNAL ASSIGNMENT
P1	TMDS DATA2+	P2	TMDS DATA2 SHIELD
P3	TMDS DATA2-	P4	TMDS DATA1+
P5	TMDS DATA1 SHIELD	P6	TMDS DATA1-
P7	TMDS DATA0+	P8	TMDS DATA0 SHIELD
P9	TMDS DATA0-	P10	TMDS CLOCK+
P11	TMDS CLOCK SHIELD	P12	TMDS CLOCK-
P13	CEC	P14	RESERVED (NC ON DEVICE)
P15	SCL	P16	SDA
P17	DDC/CEC GROUND	P18	+5V POWER
P19	HOT PLUG DETECT		

DISPLAYPORT		
PIN NUMBER	SOURCE-SIDE PIN ASSIGNMENT	SINK-SIDE PIN ASSIGNMENT
P1	ML_Lane 0(p)	ML_Lane 3(n)
P2	GND	GND
P3	ML_Lane 0(n)	ML_Lane 3(p)
P4	ML_Lane 1(p)	ML_Lane 2(n)
P5	GND	GND
P6	ML_Lane 1(n)	ML_Lane 2(p)
P7	ML_Lane 2(p)	ML_Lane 1(n)
P8	GND	GND
P9	ML_Lane 2(n)	ML_Lane 1(p)
P10	ML_Lane 3(p)	ML_Lane 0(n)
P11	GND	GND
P12	ML_Lane 3(n)	ML_Lane 0(p)
P13	CONFIG1	CONFIG1
P14	CONFIG2	CONFIG2
P15	AUX CH (p)	AUX CH (p)
P16	GND	GND
P17	AUX CH (n)	AUX CH (n)
P18	HOT PLUG DETECT	HOT PLUG DETECT
P19	RETURN	RETURN
P20	DP PWR	DP PWR



Choose SIO Power Source by project

BOM	無S0iX線路	有S0iX線路
OR8221	mount	unmount
OR8236	unmount	mount

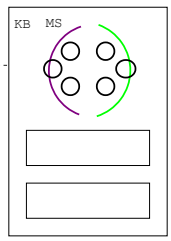
BOM select	LPC Mode	eSPI Mode
OR8151	mount	unmount
OR8202	mount	unmount
OR8172	unmount	mount
OR8161	unmount	mount
OR8237	unmount	mount
OR212	mount	unmount
OR720	unmount	mount

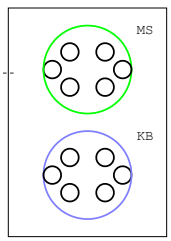
BOM select	S0IX	Non-S0IX
OR8327	mount	unmount
OQ6001A	mount	unmount
OQ6001B	mount	unmount
OR8326	mount	unmount
OR8232	mount	unmount
OQ5018	mount	unmount
OR8233	mount	unmount
OR8236	mount	unmount
OR8221	unmount	mount

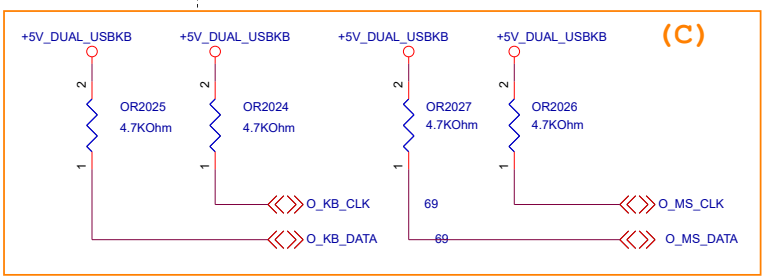
<Variant Name>

ASUS	Title :	NCT6798D-1
ASUSTek COMPUTER INC.	Engineer:	Tom Yang
Size: A1	Project Name: Standard Circiut	Rev: 3.1
Date: Wednesday, July 06, 2022	Sheet 69 of 170	

3擇1, By Project 需求:
1. 如無Onboard KBMS connector , 請保留(C)框, 刪除(A)(B)框.
2. 如connector只有一個KBMS孔 請留(A)框, 刪除(B)(C)框.
3. 如connector分別各有一個KB, 一個MOS孔, 請留(A)(B)框, 刪除(C)框.





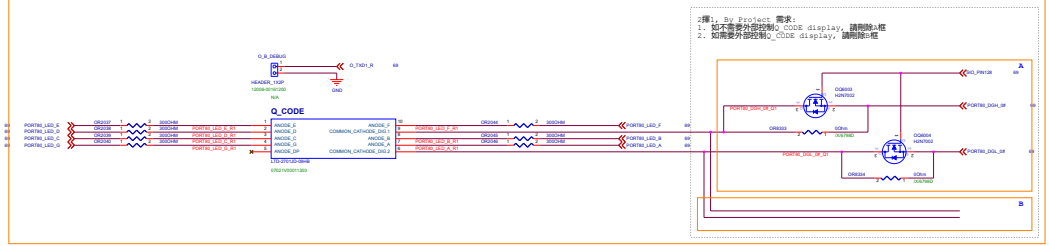


<Variant Name>

ASUSTek COMPUTER INC.	Title : NCT6798D-2	
	Engineer: Tom Yang	
Size: A3	Project Name: Standard Circiut	Rev: 3.1
Date: Wednesday, July 06, 2022	Sheet 70 of 170	

1.板子80Port Debug使用On board debug LED且無COM Port spec
留Debug LED+1x2 BIOS DEBUG Header (O_TXD1_R/GND用訊號不需留COM Port level shift IC)

2.擇1, By Project 需求:
1. 如不需要外部控制Q_CODE display, 請刪除A框
2. 如需要外部控制Q_CODE display, 請刪除B框



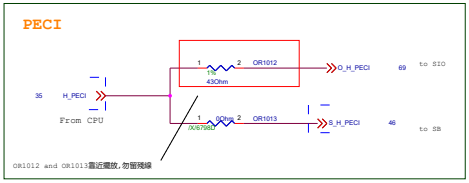
<Variant Name>

ASUSTeK COMPUTER INC	Title :	NCT6796D-3	
	Engineer:	Tom Yang	
Size: A2	Project Name:	Standard Circuit	Rev: 2.1
Date: Wednesday, July 06, 2022	Sheet: 71	of: 130	

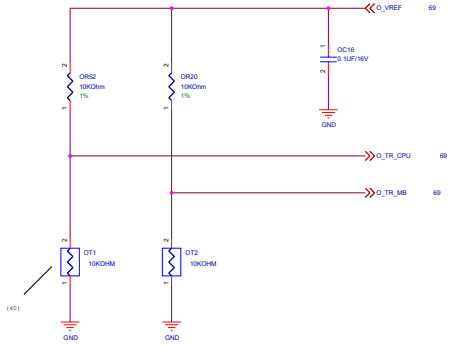
6/12 revised the circuits to two 0 ohm style

SKL PDG CRB CPU PECI to EC PECI have 43 ohm

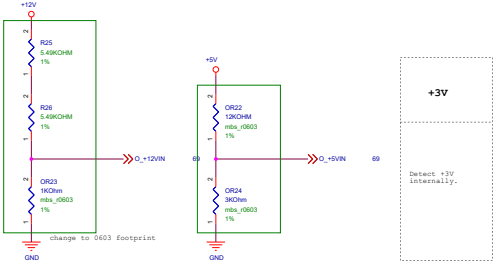
Z97 OR1012 0 ohm



Hardware Monitor for Temperature



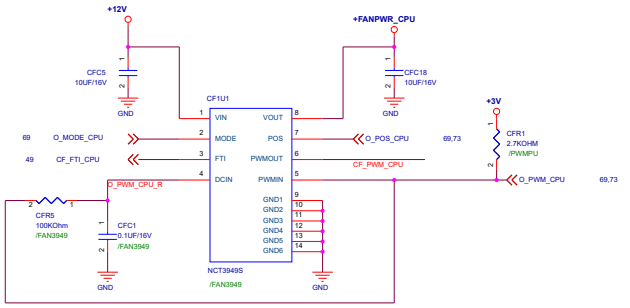
Hardware Monitor for VIN

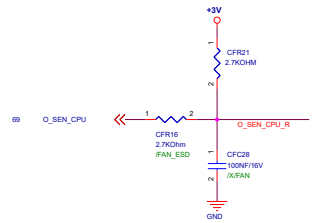


<Variant Name>

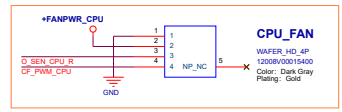
ASUSTeK COMPUTER INC	Title : NCT6798D-4	
	Engineer: Tom Yang	
Size: A3	Project Name: Standard Circuit	Rev: 3.1
Date: Wednesday, July 06, 2022	Sheet 72 of 170	

CPU_FAN (3949)

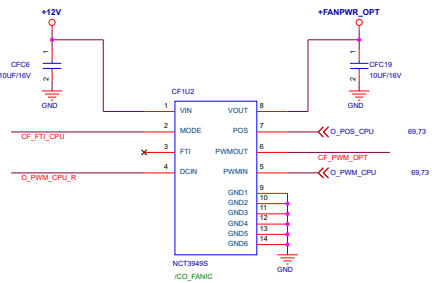


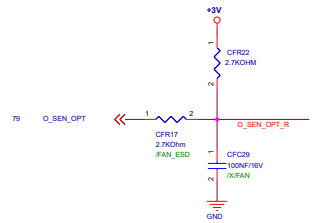


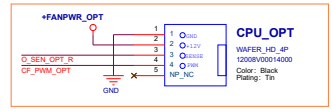
CPU_FAN header	part number	Category
Color:Dark Gray Plating:Gold	12008V00015400	ROG
Color:Dark Gray Plating:Tin	12008V00015500	STRIX TUF GAMING PRIME PRO



CPU_OPT (3949)







Title : FAN
ASUSTek COMPUTER INC.
Engineer: Yodream_Chen
Size: Custom
Project Name: Innovation Circuit
Rev: -
Date:
Sheet 73 of
<Variant Name>

CHA_FAN (3949)

CHA_FANP (3961)

+FANPWR_SYS & +FANPWR_SYS_L 請支援到3A

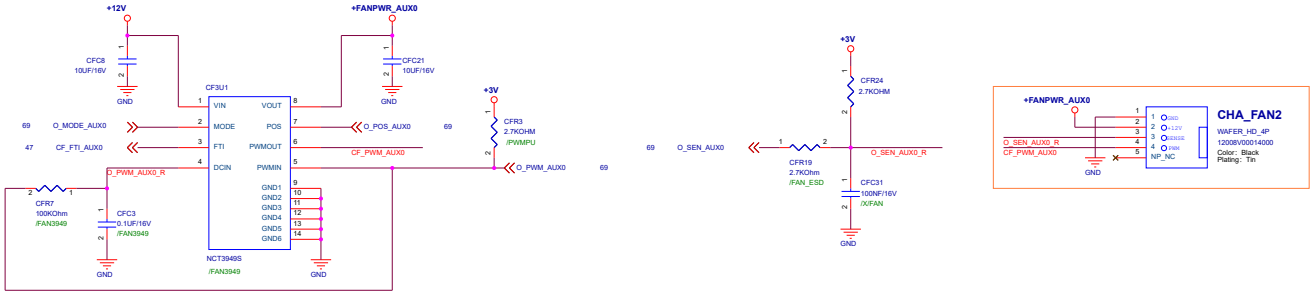
CHA_FAN1 (3949)

CHA_FAN1P (3961)

+FANPWR_SYS & +FANPWR_SYS_L 請支援到3A

ASUSTek COMPUTER INC.	Title : FAN	
	Engineer: Yodream_Chen	
Size: Custom	Project Name: Innovation Circuit	Rev: -
Date:	Sheet 74 of	
<Variant Name>		

CHA_FAN2 (3949)



CHA_FAN2P

+FANPWR_AUX0 & +FANPWR_AUX0_L 請支援到3A

ASUSTek COMPUTER INC.	Title : FAN	
	Engineer: Yodream_Chen	
Size: Custom	Project Name: Innovation Circuit	Rev: -
Date:	Sheet 75 of	
<Variant Name>		

CHA_FAN3 (3949)

CHA_FAN3P (3961)

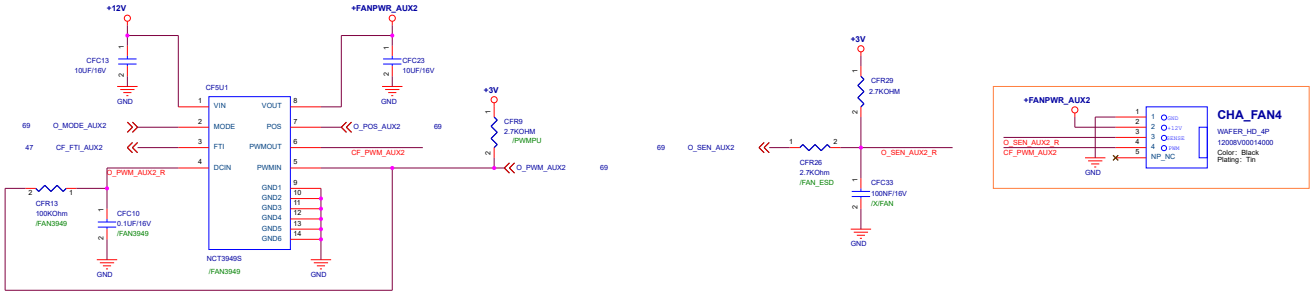
+FANPWR_AUX1 & +FANPWR_AUX1_L 請支援到3A

RAD_FAN1 (3961)

+FANPWR_AUX1 請支援到4A

ASUSTek COMPUTER INC.	Title : FAN		
	Engineer: Yodream_Chen		
Size: Custom	Project Name: Innovation Circuit		Rev: -
Date:	Sheet 76 of		
<Variant Name>			

CHA_FAN4 (3949)



RAD_FAN2 (3961)

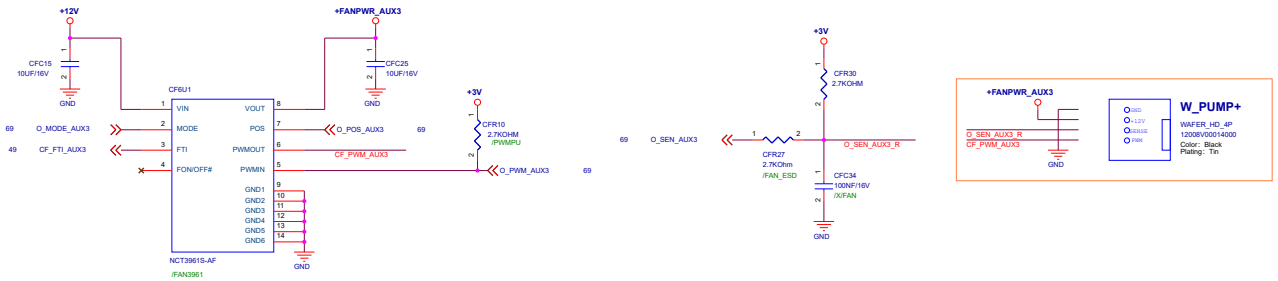
+FANPWR_AUX2 請支援到4A

ASUSTek COMPUTER INC.	Title : FAN	
	Engineer: Yodream_Chen	
Size: Custom	Project Name: Innovation Circuit	Rev: -
Date:	Sheet 77 of	
<Variant Name>		

AIO_PUMP (3949)

W_PUMP+ (3961)

+FANPWR_AUX3 請支援到3A



W_PUMP+2 (3961)

+FANPWR_AUX4 請支援到3A

ASUSTek COMPUTER INC.	Title : FAN		
	Engineer: Yodream_Chen		
Size: Custom	Project Name: Innovation Circuit		Rev: -
Date:	Sheet 78 of		
<Variant Name>			

[EC]

Shared function with KB3724

Blue text means New Function

Ver 2.0

EC TX log

EC FAN

BIOS Flash Back

Water cooling

PLC interrupt

CLR_CMOS

Thermal Detect

EC HWM

Power Ref.

Dual BIOS

For ESPI Issue

ADC CAP/Resistor

SMBUS

MR

OC Panel

V-Latch

V-Clamp

CLK Gen.

3.2V PWM

RESET/ SAFE Button

RSVD Switch

RSVD2 Switch

Puse mode Switch

System Int.

ESPI

EC Flash(EC F/W)

FLEXKEY

Power Cut

PMIC (DDR5)

DDR4

TBT PD

Vboot Porting

IC Power

PWR Sequence

EC HW reset

INTRUDER test

SDix

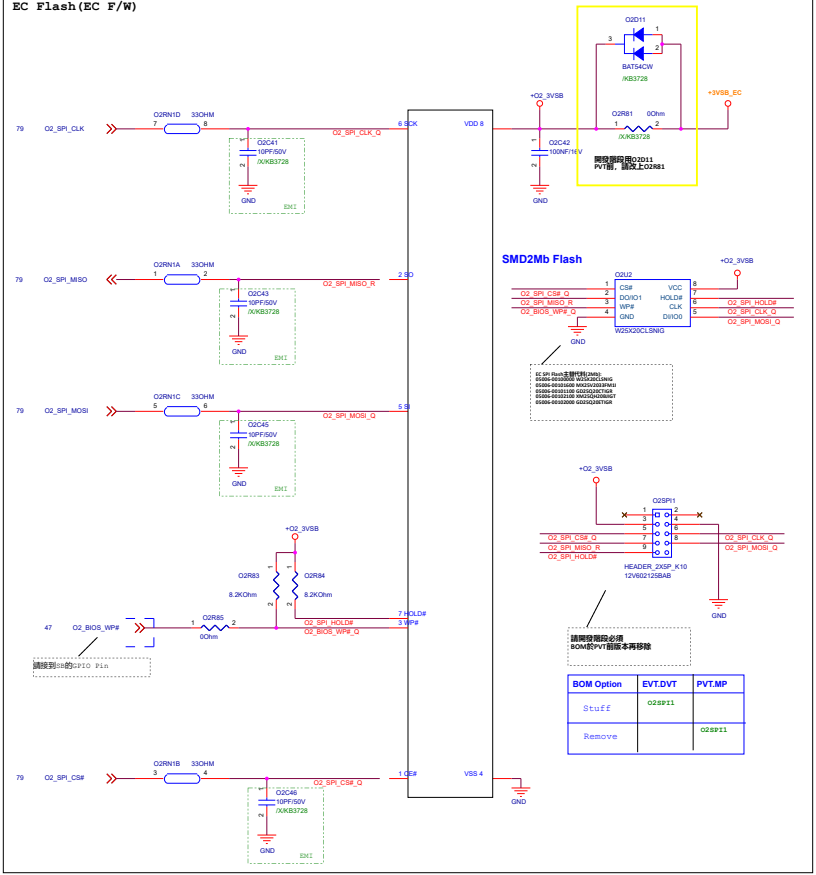
EC PCB ID

ADC CAP/Resistor (MR)

[EC Flash / MR Flash / Power]

Ver 2.0

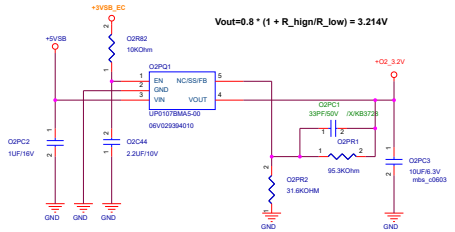
EC Flash(EC F/W)



BOM Option	EVT.DVT	PVT.MP
Stuff	O2SPI1	
Remove		O2SPI1

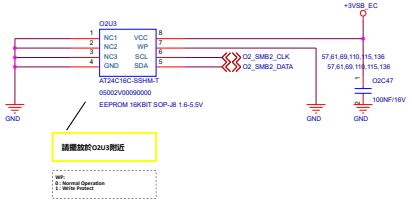
LDO for EC Power

若ADC/PWM VREF選用+3VSB則LDO線路可刪除



EEPROM Circuit (Peter MR use)

用於紀錄CPU,Cooler特性及記錄CPU電壓for BIOS 進入對應的MR profile

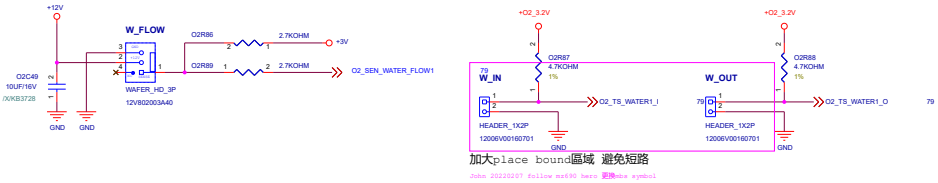


<Variant Name>

ASUSTek Computer Inc.	Title : Flash/Power	
	Engineer: Kaizer Luo	
Size: A3	Project Name: EC Standard Circiut	Rev: 2.0
Date: Wednesday, July 06, 2022	Sheet 80 of 170	

Ver 2.0

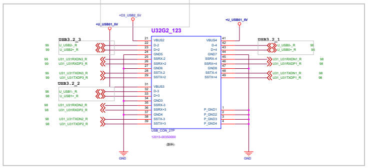
Water Flow

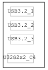


Water Block(WB)

Node / OC Panel Circuit (Peter MR use)

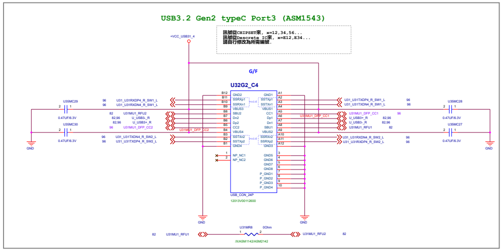
3 port 架高U32G2(紅)



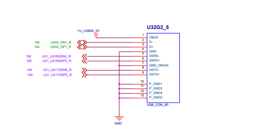


1 port U32G2(Type-C)

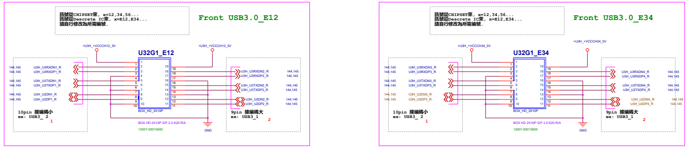
USB3.2 Gen2 typeC Port3 (ASM1543)



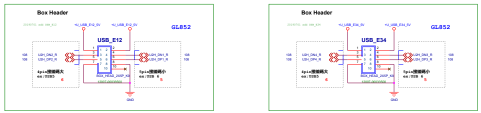
port(紅) U32G2架高



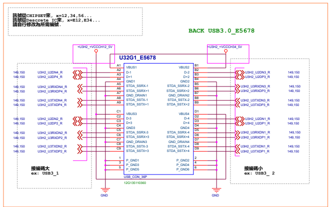
Front U32G1



Front USB2.0



Back U32G1

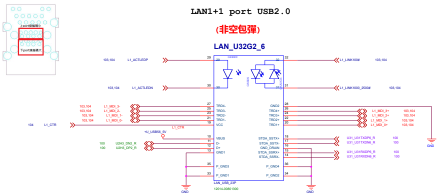


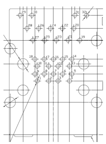
CHANGE to A+C type LAN

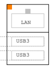
LAN1+1 port USB2.0

(非空包彈)

LAN_U32G2_6







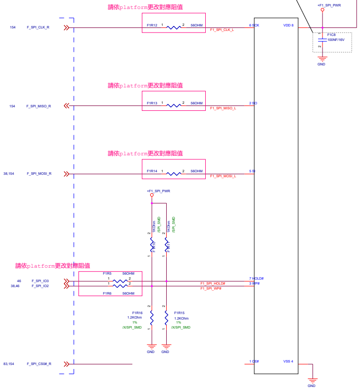
SPEED LED:
1. GREEN : 1000Mbps
2. ORANGE : 100Mbps
3. No Light : 10Mbps

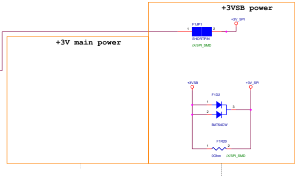
只使用一顆LAN,
LAN1_USB3_x改為LAN_USB3_x,
USB3_x;
挑號從CHIPSET來, x=12,34,56...
挑號從Descrete IC來, x=E12,E34...
請自行修改為所需編號.

USB 3.0 STANDARD-A CONNECTOR PIN ASSIGNMENTS

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1 10	VBUS	POWER
2 11	D-	USB 2.0 DIFFERENTIAL PAIR
3 12	D+	
4 13	GND	GROUND FOR POWER RETURN
5 14	StdA_SSRX-	SUPERSPEED RECEIVER DIFFERENTIAL PAIR
6 15	StdA_SSRX+	
7 16	GND_DRAIN	GROUND FOR SIGNAL RETURN
8 17	StdA_SSTX-	SUPERSPEED TRANSMITTER DIFFERENTIAL PAIR
9 18	StdA_SSTX+	

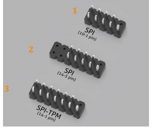
<Variant Name>
ASUSTek COMPUTER INC.
Title : Front&Back IO_USB3.0
Engineer: Aaron_Su
Size: A1 | Project Name: Maximus XI Extreme | Rev: R1.01
Date: Wednesday, July 06, 2022 | Sheet 82 of 170





	使用的料件	一般適用機種	說明	備註	料号
1	10-1 pin SPI header	ROG/STRIX 系列	開案前請與 SPM leader 確認	SPI 不會有文字面	12G06110010M
2	14-5 pin SPI header	Channel 機種	開案前請與 SPM leader 確認	SPI 不會有文字面，但是需預留 TPM 的線路不上件不蓋綠漆	12006-00322500
3	14-1 pin SPI-TPM header	客戶或 SPM leader 指定機種	開案前請與 SPM leader 確認	SPI-TPM 會帶有 “TPM” 文字面，TPM 線路上件	12006-00321700

二擇一：
1. 12V06110010M for 水平插入SPI CARD
優點是不會與PCIE顯卡或device卡件，但限制區域面積較大.
2. 12006V00023300 for 垂直插入SPI CARD
優點是限制區域面積較小，但使用上可能與PCIE顯卡或Device卡件.
兩者link的G料相同.

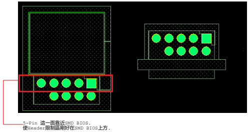


0.5I

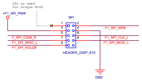
12006V00023301(FOR 10-1 IPMI CARD)

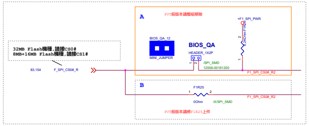
12V06110010M for 水平插入SPI CARD
mbs_hd_2x5p_79_k10_pin_lf3

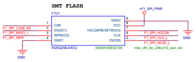
12006V00023300 for 垂直插入SPI CARD
mbs_hd_2x5p_79_k10_ls_lf3



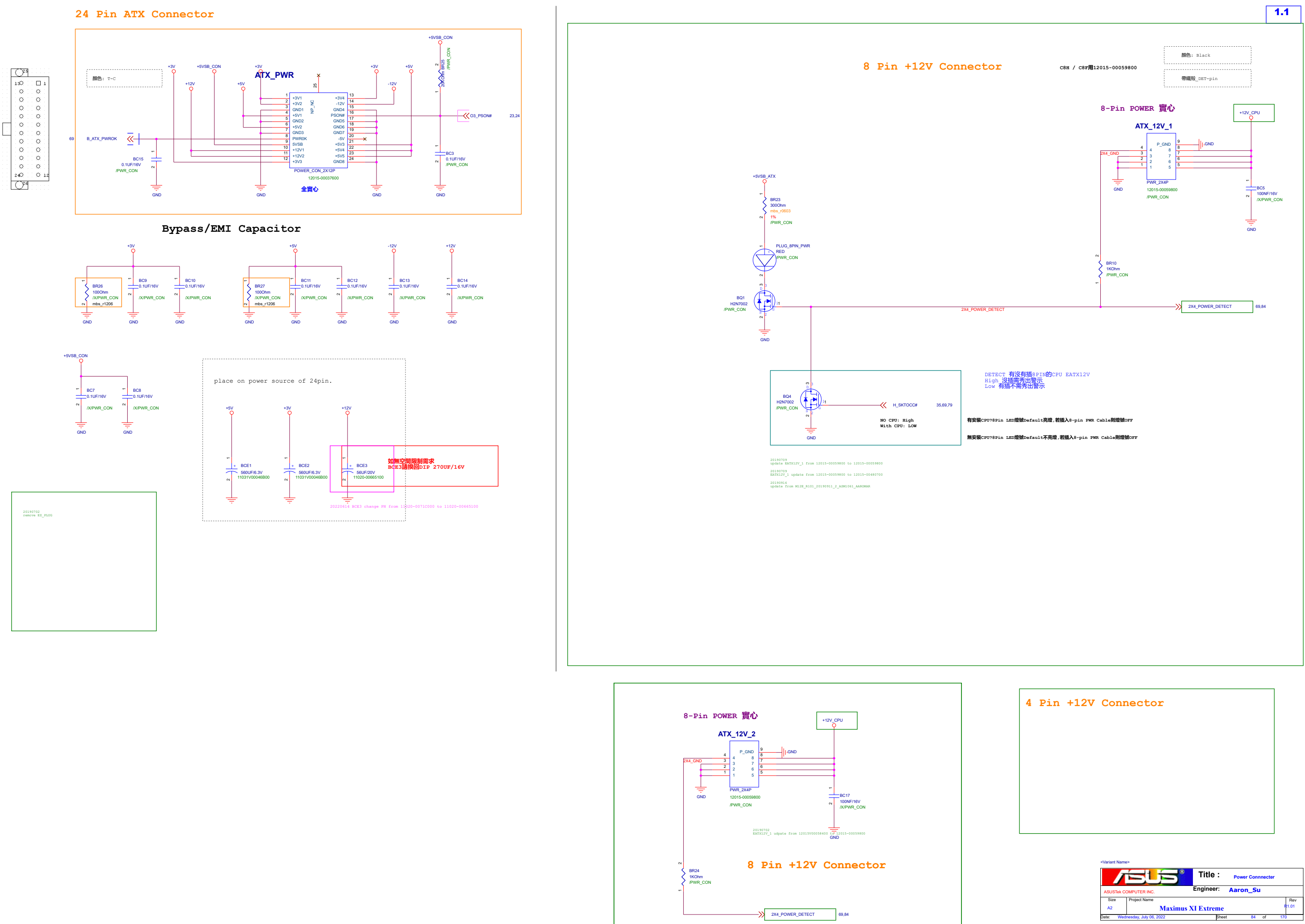
5-Pin 這一面靠近SMD BIOS.
使Header限制區剛好在SMD BIOS上方.



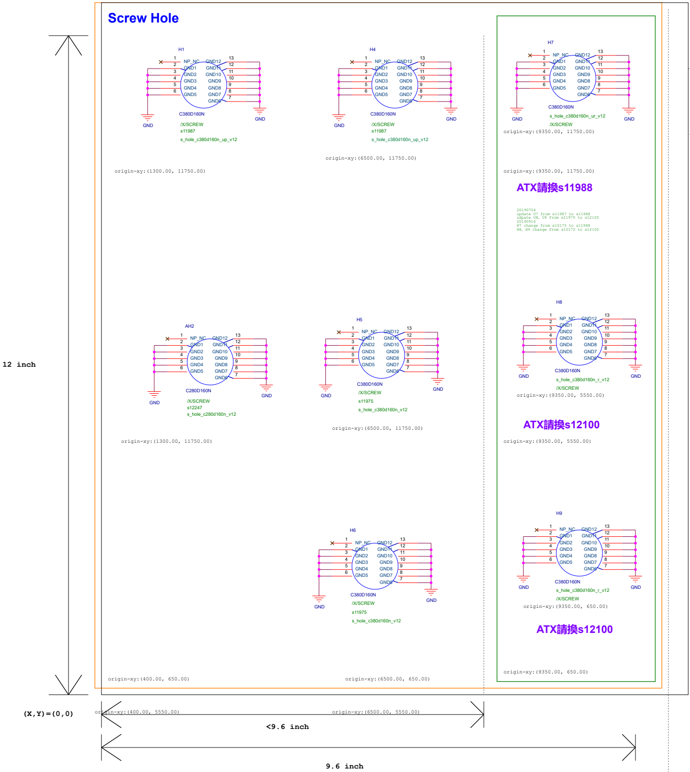




ASUSTeK COMPUTER INC.
Title : SINGLE BIOS_SPI SMD-1
Engineer: Bobson Hsu
Project Name: Standard Circuit
Rev 0.5I
Date: Wednesday, July 06, 2022


1.1
24 Pin ATX Connector
ATX_PWR
POWER_CON_2X12P
12015-00037600
全實心
+5VSB_CON
O3_PSON#
B_ATX_PWROK
BC15
0.1UF/16V
/PWR_CON
BC3
0.1UF/16V
/PWR_CON
GND
Bypass/EMI Capacitor
BR26
BC9
BC10
BR27
BC11
BC12
BC13
BC14
BC7
BC8
place on power source of 24pin.
BCE1
560UF/6.3V
11031V00046B00
BCE2
560UF/6.3V
11031V00046B00
BCE3
56UF/20V
11020-00665100
如無空間限制需求
BCE3請換回DIP 270UF/16V
8 Pin +12V Connector
8-Pin POWER 實心
ATX_12V_1
PWR_2X4P
12015-00059800
/PWR_CON
+12V_CPU
BC5
100NF/16V
/X/PWR_CON
+5VSB_ATX
BR23
300Ohm
PLUG_8PIN_PWR
RED
BQ1
H2N7002
BR10
1KOhm
2X4_POWER_DETECT
BQ4
H2N7002
H_SKTOCC#
NO CPU: High
With CPU: LOW
8-Pin POWER 實心
ATX_12V_2
PWR_2X4P
12015-00059800
BC17
100NF/16V
BR24
1KOhm
8 Pin +12V Connector
2X4_POWER_DETECT
4 Pin +12V Connector
Title : Power Connnecter
Engineer: Aaron_Su
ASUSTek COMPUTER INC.
Maximus XI Extreme
Date: Wednesday, July 06, 2022
Sheet 84 of 170
Rev R1.01

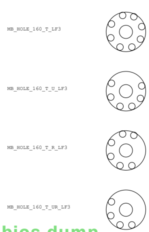
Screw Hole



Screw Select

	Standard (12 x 9.6)	scale down (12 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H9	V	X

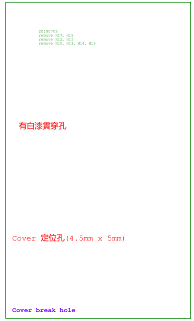
MB SCREW FOOTPRINT

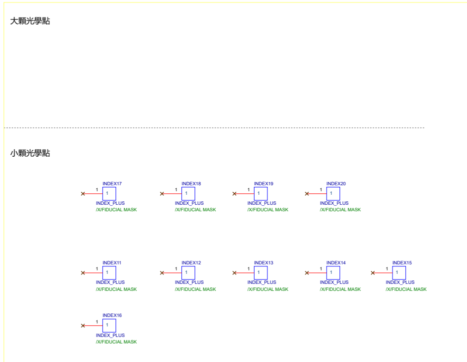


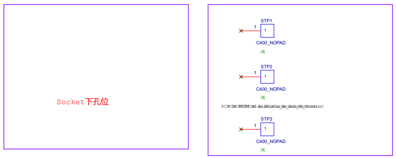
Fiducial Mask (光學點)

光學點需要10顆，
LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除。

20180105 Add







<Variant Name>

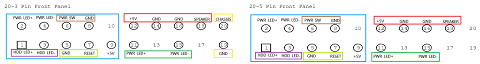
Title :	ATX Screw Hole/Fiducial Mask
ASUSTek COMPUTER INC. Engineer:	Aaron_Su
Size A2	Project Name: Maximus XI Extreme — Rev R1.01
Date: Wednesday, July 06, 2022	Sheet 85 of 170

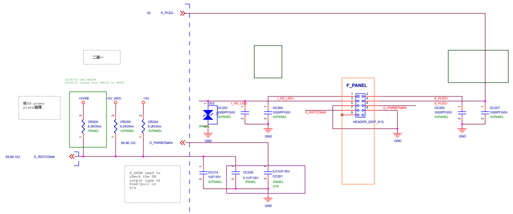
Front Panel 20-3pin Colay 20-5 pin

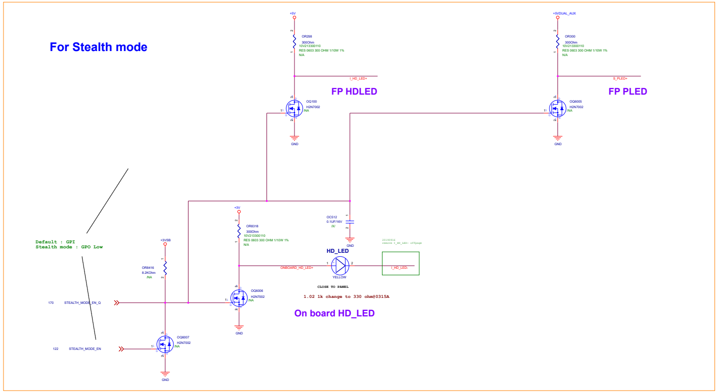
PART Reference 與SIO共用D 並從2005編起

20-3 Pin Front Panel

20-5 Pin Front Panel







chassis intruder support	Footprint P/N	實際上料 Front Panel P/N	BOM option
支援	20-3 Pin 12006-00201700	20-3 Pin 12006-00201700	紅框內線路全上件
不支援(預留不上)	20-3 Pin 12006-00201700	20-5 Pin 12006-00202000	紅框內線路為/X 預留不上
不支援	20-5 Pin 12006-00202000	20-5 Pin 12006-00202000	移除紅框內線路

pull high 2M Ohm to +3V_BAT & 100PF Cap to GND on SIO side or Chipset side

若使用Standby LED,把PWR Button+RST Button移除;
若使用PWR Button+RST Button,把Standby LED移除.

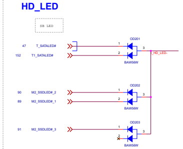
Standby LED

PWR Button

For EuP, RD可自行fine-tune.

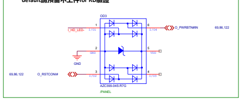
RST Button

HD_LED



ESD protection diode

default請預留不上件for RD驗證



Change the net name to combine the HD LED active

請按照下列 Net name 修改:

T1_SATALED#
T2_SATALED#

M2_SSDLED#
M2_2_SSDLED#

用不到的 net 請Delete,並打x

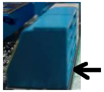
Title : Panel&HotStart&Stealth

Engineer: Aaron_Su

Project Name: Maximus XI Extreme

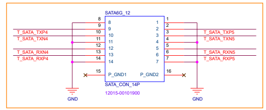
Rev R1.01

	Connector 顏色
SATA6G_123456	LIGHT GRAY
	BROWN

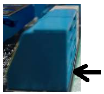


R/A Connector擺放與板端切齊,
如上圖黑色箭頭處.

顏色: D-G

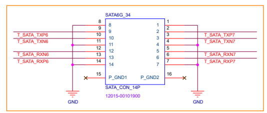


	Connector 顏色
SATA6G_123456	LIGHT GRAY
	BROWN

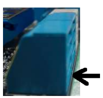


R/A Connector擺放與板端切齊,
如上圖黑色箭頭處.

顏色: D-G



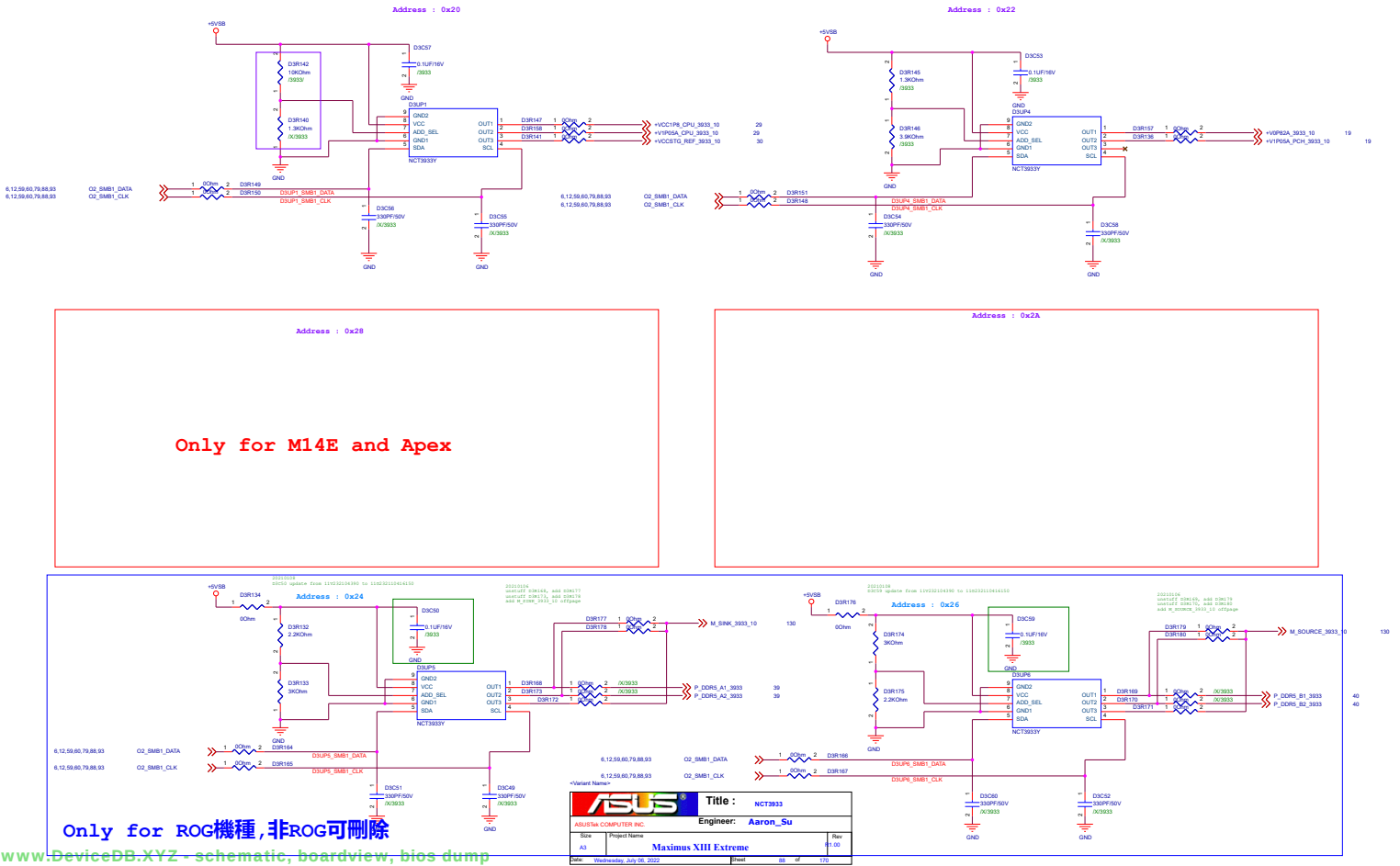
	Connector 顏色
SATA6G_123456	LIGHT GRAY
	BROWN

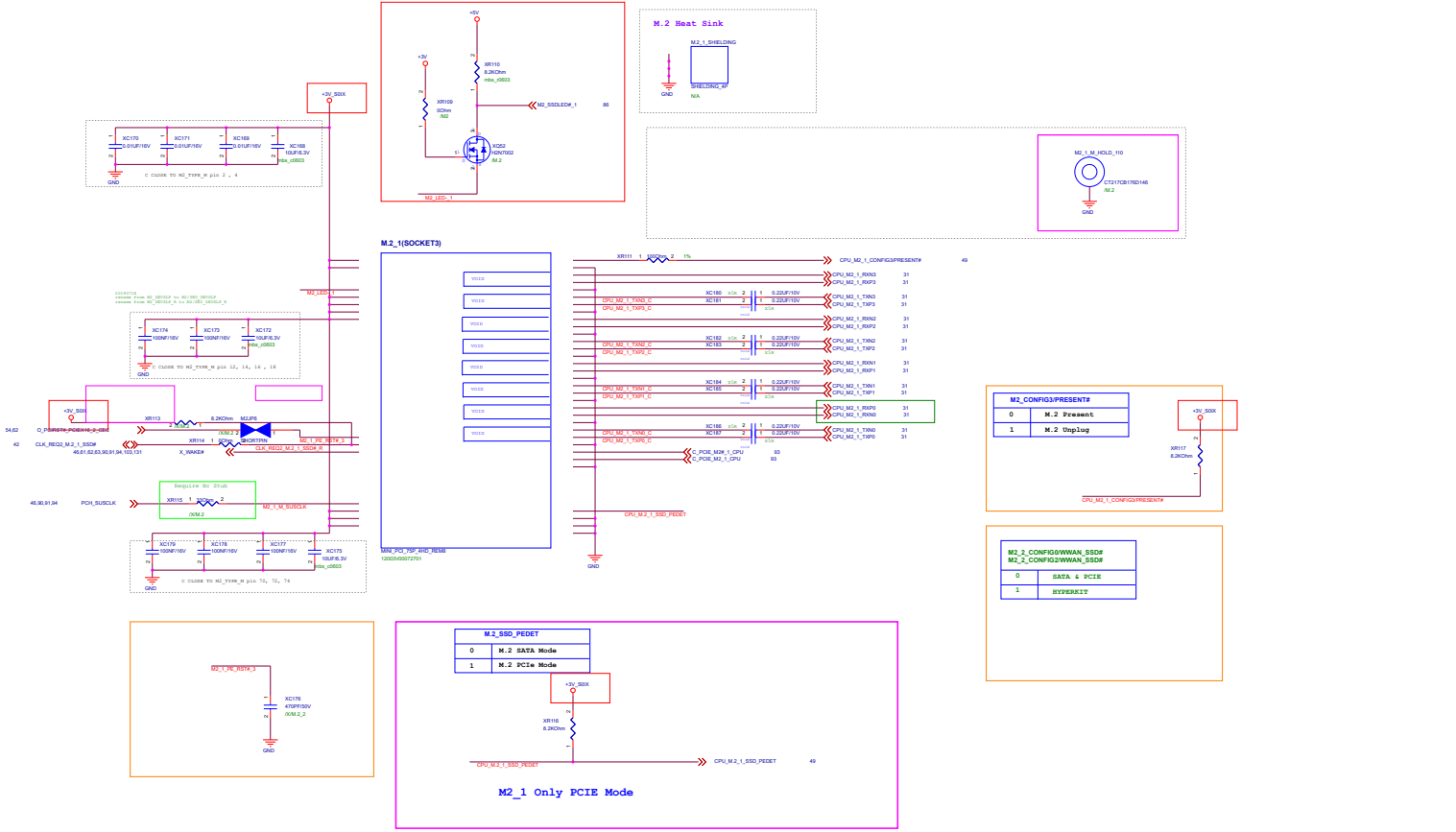


R/A Connector擺放與板端切齊,
如上圖黑色箭頭處.

<Variant Name>

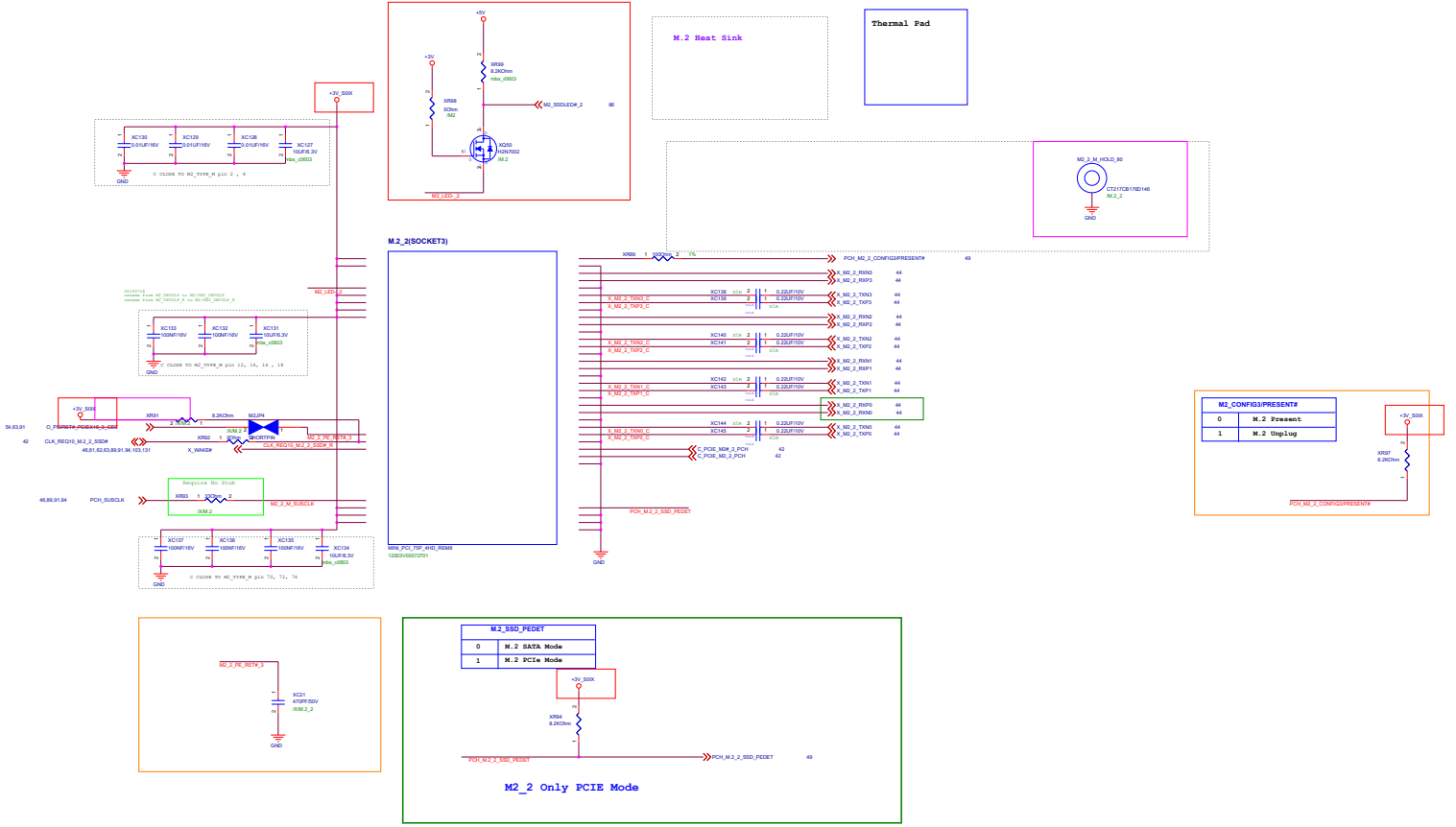
ASUSTek COMPUTER INC.	Title : SATA6G_123456(CHIPSET)
	Engineer: Aaron_Su
Size: A2	Project Name: Maximus XI Extreme — Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 87 of 170


Address : 0x20
Address : 0x22
Address : 0x28
Only for M14E and Apex
Address : 0x2A
Address : 0x24
Address : 0x26
Only for ROG機種,非ROG可刪除
Title : NCT3933
Engineer: Aaron_Su
ASUSTeK COMPUTER INC.
Maximus XIII Extreme
Wednesday, July 06, 2022
www.DeviceDB.XYZ - schematic, boardview, bios dump



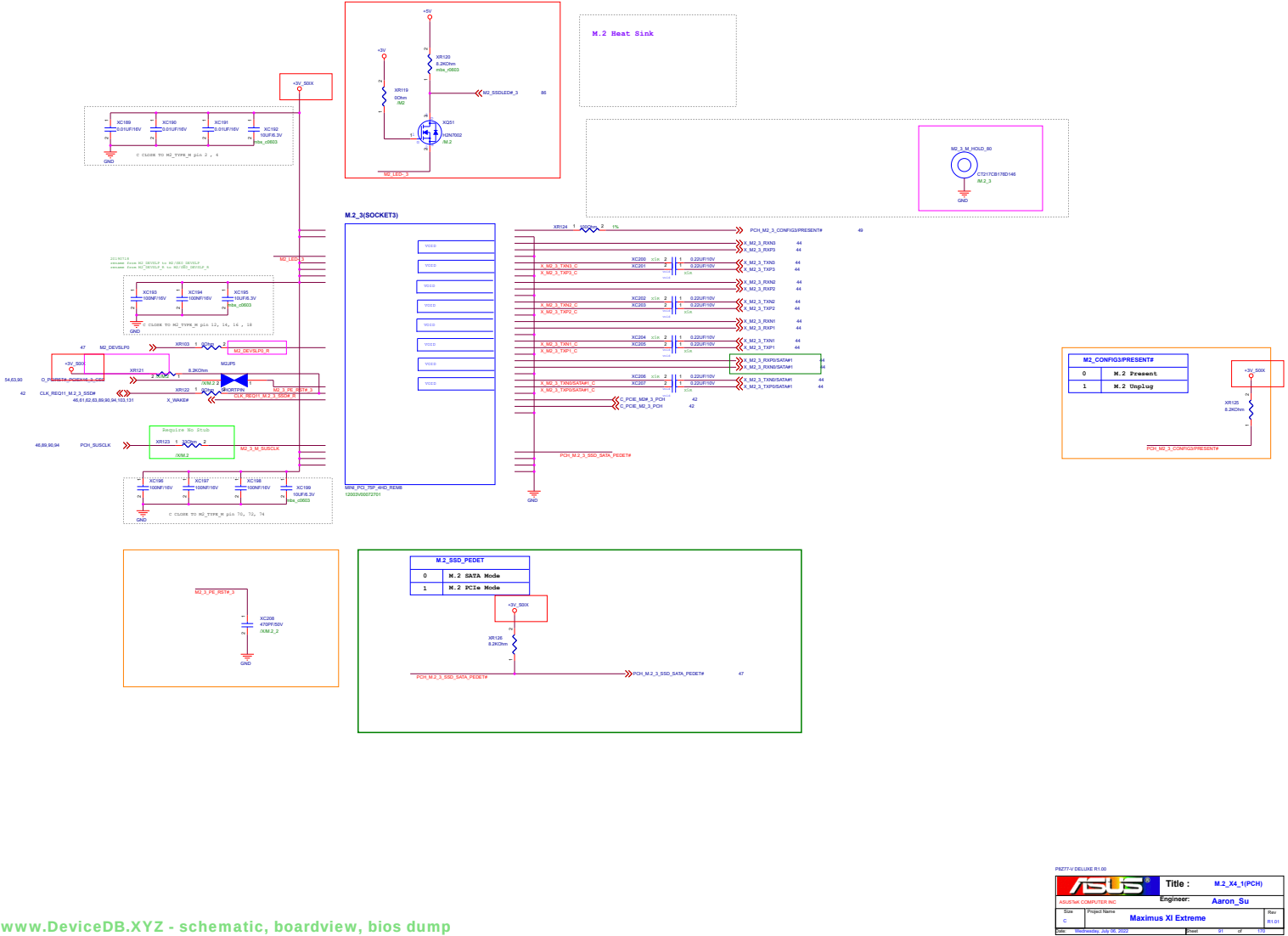
P8Z77-V DELUXE R1.00

ASUSTeK COMPUTER INC	Title :	M.2_X4_2
	Engineer:	Aaron_Su
Size: C	Project Name: Maximus XI Extreme	Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 89 of 170	



RMZ77-V DELUXE R1.00

ASUSTeK COMPUTER INC	Title :	M.2_X4_2
	Engineer:	Aaron_Su
Size: C	Project Name:	Maximus XI Extreme
Rev: R1.01		
Date: Wednesday, July 06, 2022	Sheet 90 of 140	



20190726
add H50, H51
20190802
change from 13020-01372000 to 13020-01378500

H50 change PN from 13020-01378500 to 13020-04422200
H51 change PN from 13020-01378500 to 13020-01372000
20200825
H51 change PN from 13020-01372000 to 13020-01377600

20190705
update from M11A_WIFI_M102A_SM4_STUFF_20181008_1030.dsn
20190726
update H10, H11, H14, H19, H17
20190802
H18, H15, H11, H14 change from a12080 to a12668
H17 change from a12080 to a13044

H14, H11 change PN from a12668 to a13583
20200818 H14, H11 change PN from a13583 to a12851

20210705 Remove H10,H12

Back I/O Cover螺孔

Cover break hole

M.2 Heat Sink_BP

HEATSINK_M2_BP1
HEATSINK
13020-06470200
/X

HEATSINK_M2_BP2
HEATSINK
13020-06470300
/X

HEATSINK_M2_BP3
HEATSINK
13020-06470300
/X

ME hole

H67 /X C185D185N
H62 /X C165D165N
H68 /X C185D185N
H64 /X C165D165N

背板 hole

H10 /X C165D165N
H11 /X C165D165N
H12 /X C165D165N
H13 /X C165D165N

Thermal hole

CPU hole

H54 /X C126D126N_A165

PCH hole

H57 /X C126D126N_A165
H58 /X C126D126N_A165
H59 /X C126D126N_A165
H60 /X C126D126N_A165

1200 定位孔

LGA_1200_HOLE
NP_NC1
NP_NC2
NP_NC3
NP_NC4
CT59D159N
/X

20220331 H56 change PN from a13471 to 13020-01575800

底板NUT

H66 CT217BC176D146 /X
H2 CT217BC176D146 /X

AUDIO_COVER
GND1 GND2
SHIELDING_2P
13020-01430400

HEATSINK_MOS
HEATSINK
temp_T_005630
Scotchspice_mos_hs
/X

HEATSINK_PCH
HEATSINK
temp_T_005058
GODMOTHER
/X

HEATSINK_M.2_1
HEATSINK
temp_T_005784
Scotchspice_M2-C
/X

HEATSINK_M.2_23
HEATSINK
temp_T_005057
GODMOTHER-M.2_P.HS
/X

EMI

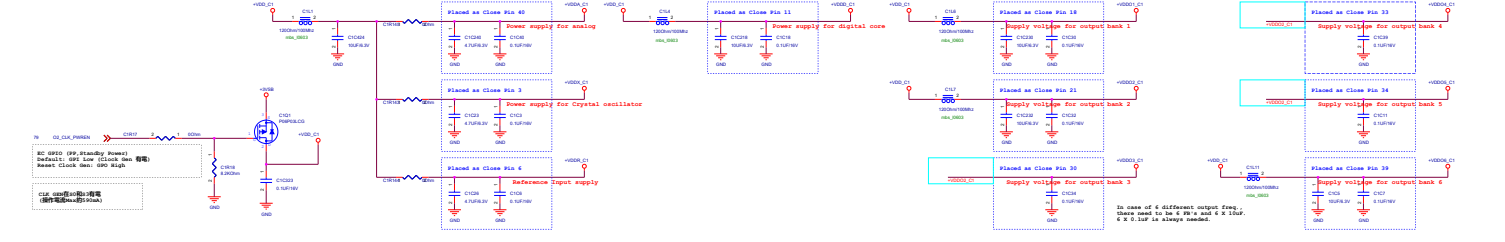
H19 /X
H55 /X
H17 /X
H18 /X
NP_NC
GND1
GND2
CT232D126N
GND

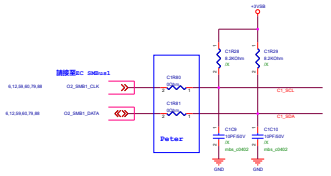
EMI下地孔位

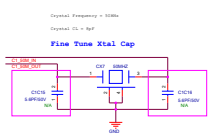
<Variant Name>

ASUSTeK COMPUTER INC

Title : HEAT SINK
Engineer: Aaron_Su
Size: A3
Project Name: Maximus XI Extreme
Rev: R1.01
Date: Wednesday, July 06, 2022
Sheet 92 of 170

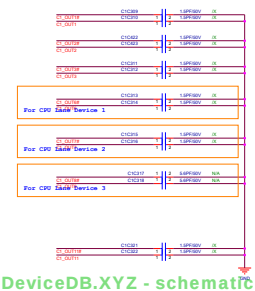


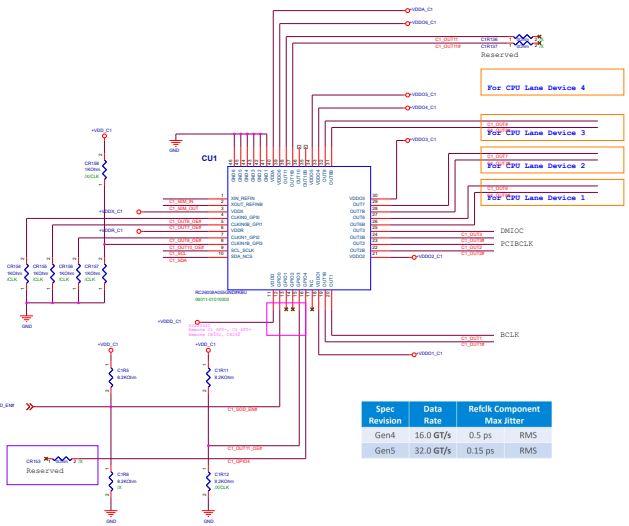




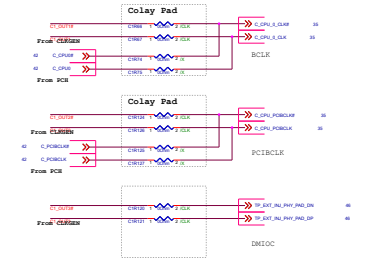
General Configuration

Parameter	Value
Device I²C Address	Primary 0x12

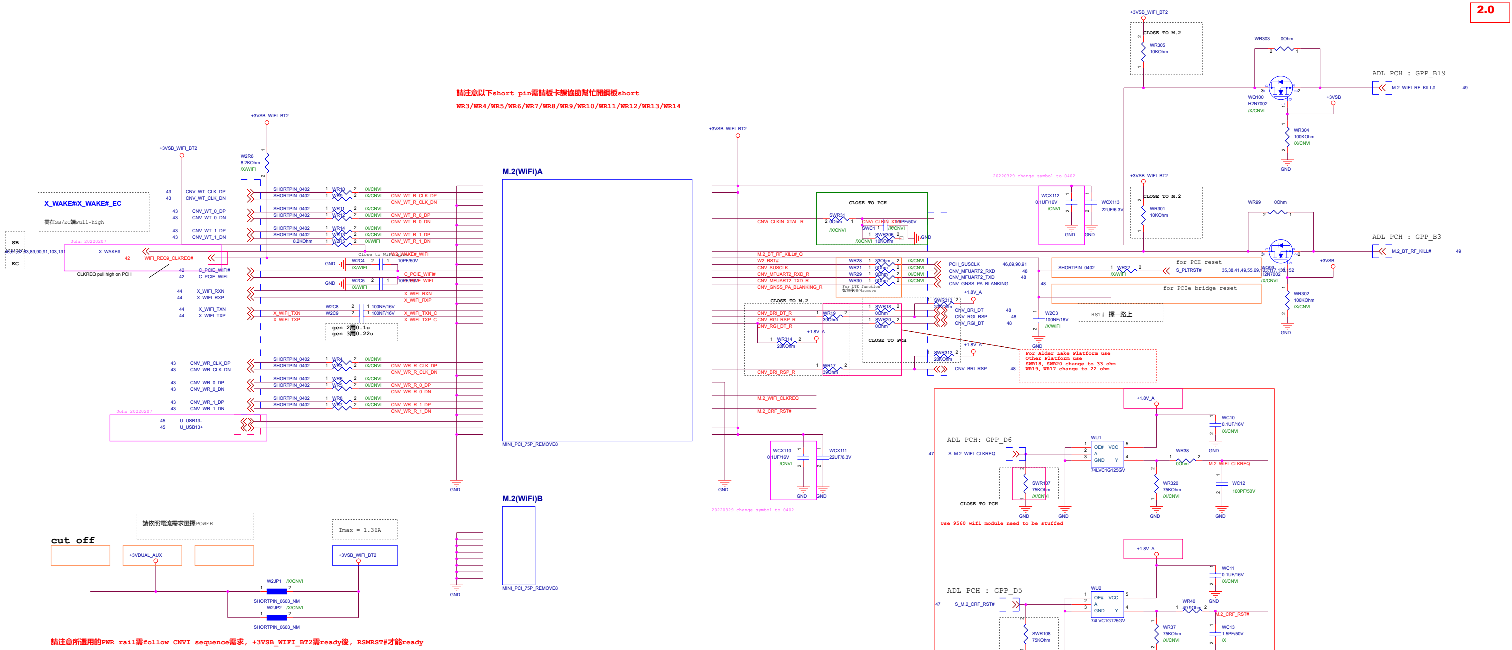


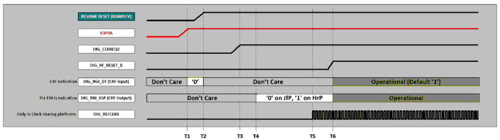


Spec Revision	Data Rate	Refclk Component Max Jitter
Gen4	16.0 GT/s	0.5 ps RMS
Gen5	32.0 GT/s	0.15 ps RMS



Title :	CLKGEN RC26008
Engineer:	Scott2_Lin
Size	A2
Project Name	CLKGEN RC26008
Rev	A0.00
Date	Wednesday, July 09, 2025
Sheet	83 of 126





Legend -	Timing Constrains -	Notes -
T1 – V3P3A turned on (3.3V)	T2 – T1 > 0 ms	(1) POWER_GOOD should be kept NC on all functional boards
T2 – Platform releases the reset and locks the Strap pin value	T3 – T2 ≥ 0 ms	(2) DIG_RGI_DT should be '0' between T1 and T2 for CRF indication to the platform
T3 – Platform asserts DIG_CLKREQ0, which triggers the JfP CRF Power Up	T4 – T3 ≥ 0 ms	(3) DIG_BRI_RSP indicates the CRF in use between T4 and T6: '0' indicates Jefferson Peak; '1' indicates Harrison Peak
T4 – Initial CRF state	T6 – T3 ≥ 2 ms	(5) DIG_REFCLK0 should be available on Jefferson Peak only, no T5 on Harrison Peak
T5 – REFCLK0 is generated by CRF per CLKREQ0	T6 – T5 > 0 ms	
T6 – CNVI release the DIG_RF_RESET_B (CRF interfaces are functional)	20ms ≥ (T5 – T3) ≥ 5ms (Due to crystal stabilization)	

<Variant Name>

ASUSTeK COMPUTER INC	Title : CNVi_PCIe_Colay	
	Engineer: Tom Yang	
Size A2	Project Name Standard Circiut	Rev 2.0
Date: Wednesday, July 06, 2022	Sheet 94 of 170	

USB 3.1 Re-Driver PI3EQX1004 Circuit

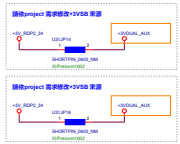
1. Modify USB 3.1 Port TX/RX Signal(input & output) Net Name by Project

2. When UU41 TXA output signals send to ASM1543, UU41C34 & UU41C35 change from 11V232224416150 to 11G232247415150

3. When UU41 TXB output signals send to ASM1543, UU41C26 & UU41C27 change from 11V232224416150 to 11G232247415150

L.2

3.3V for PI3EQX1004 *2-3pcs, 340mA/pcs@S0



Power Component place near each other!

請依project 需求修改+3VSB 來源

Re-Driver output signal pull down resistor for VCM

Re-Driver output signal pull down resistor for VCM

Place near power pin Pin3, Pin7, Pin14, Pin21,Pin25,Pin32,Pin36,Pin40

From AI1315

Connect to Choke

GL9950NE : 06113-00460300
PI3EQX1004E : 06113-00270300
PI3EQX1004Z for VCM: 06113-00270400

Pin42 (F) Pin1 (R) Pin29 (R) Pin28 (F) Pin11 (F) Pin10 (R) Pin18 (R) Pin19 (F)

4-Level Logic Selection

0	Pull down 1k to Gnd
R	Pull down 68k to Gnd
F	Floating
1	Pull high 1k to Vcc

Strapping pin

EN_AB(Pin 2)	
pull up	Enable(IPU 300k)
pull down	Disable

Strapping pin

EN_CD(Pin 20)	
pull up	Enable(IPU 300k)
pull down	Disable

EQA~D, FGA~D

EQA(Pin1), FGA(Pin42) for Port1 TX(Pin4,5)
EQB(Pin29), FGB(Pin28) for Port1 RX(Pin8,9)
EQC(Pin11), FGC(Pin10) for Port2 TX(Pin12,13)
EQB(Pin18), FGB(Pin19) for Port2 RX(Pin16,17)

	1st Port	2nd Port
TX EQ	EQA	EQC
TX FG	FGA	FGC
RX EQ	EQB	EQD
RX FG	FGB	FGD

EQ, FG Pin	
0	1K Ohm pull down
R	68K Ohm pull down
F	Floating
1	1K Ohm pull high

<Variant Name>

Title : Pericom 1004

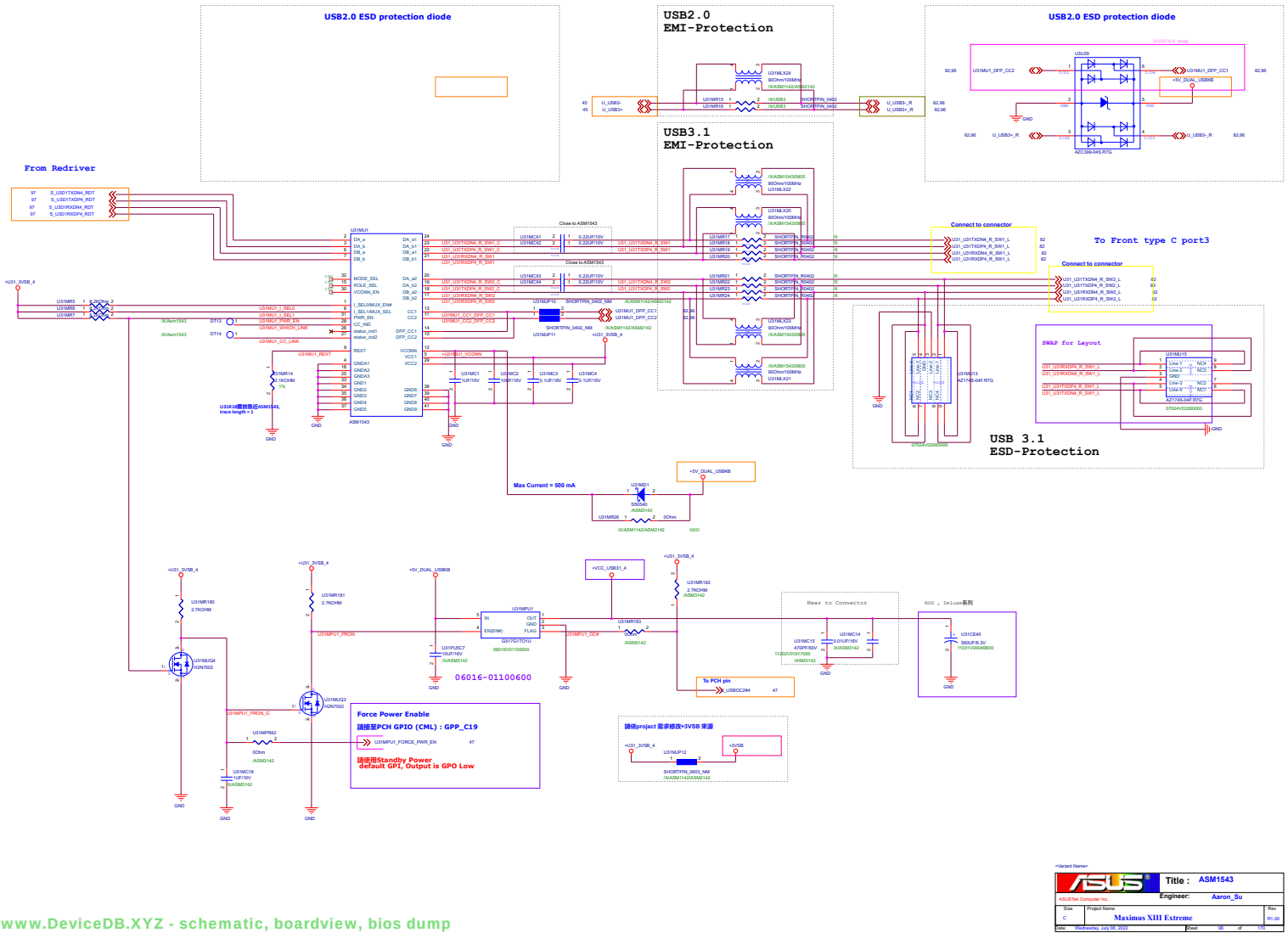
ASUSTeK Computer Inc.

Engineer: Aaron_Su

Size	Project Name	Rev
A2	Maximus XIII Extreme	R1.02

Date: Wednesday, July 06, 2022 Sheet 85 of 100

Back Type C Connector_3



USB 3.1 Re-Driver PI3EQX1004 Circuit

A. Delete the Re-Driver IC which is not needed by Project

B. Modify Input USB 3.1 TX/RX Signal Net Name by Project

C. Modify Output USB 3.1 TX/RX Signal Net Name by Project

D. for AMD Platform, RX signal's AC CAP between CPU/Chipset & Re-Driver change Part Number from 11V2322224161 50 to 11V232334350

E. If UU41 TXA output signals send to ASM1543, UU41C34 & UU41C35 change from 11V232222416150 to 11V232334150 & mount UU41R34, UU41R35, otherwise could delete UU41R34, UU41R35

F. If UU41 TXB output signals send to ASM1543, UU41C26 & UU41C27 change from 11V232222416150 to 11V232334150 & mount UU41R26, UU41R27, otherwise could delete UU41R26, UU41R27

G. If UU42 TXA output signals send to ASM1543, UU42C34 & UU42C35 change from 11V232222416150 to 11V232334150 & mount UU42R34, UU42R35, otherwise could delete UU42R34, UU42R35

H. If UU42 TXB output signals send to ASM1543, UU42C26 & UU42C27 change from 11V232222416150 to 11V232334150 & mount UU42R26, UU42R27, otherwise could delete UU42R26, UU42R27

I. If UU43 TXA output signals send to ASM1543, UU43C34 & UU43C35 change from 11V232222416150 to 11V232334150 & mount UU43R34, UU43R35, otherwise could delete UU43R34, UU43R35

J. If UU43 TXB output signals send to ASM1543, UU43C26 & UU43C27 change from 11V232222416150 to 11V232334150 & mount UU43R26, UU43R27, otherwise could delete UU43R26, UU43R27

K. Modify EQ/FG Pins' pull high/pull down BOM by layout

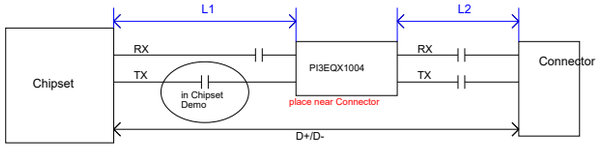
L. Choose PI3EQX1004 Power Solution by PI3EQX1004 count

BOM	PI3EQX1004 Power generated by LDO	PI3EQX1004 Power from LAN1	PI3EQX1004 Power from LAN2	PI3EQX1004 Power from Wifi
/PI3EQX1004_PWR_from_LDO	mount	unmount	unmount	unmount
/PI3EQX1004_PWR_from_LAN1	unmount	mount	unmount	unmount
/PI3EQX1004_PWR_from_LAN2	unmount	unmount	mount	unmount
/PI3EQX1004_PWR_from_WIFI	unmount	unmount	unmount	mount

M. UU41, UU42 & UU43 default use PI3EQX1004B1

EQ/FG Setting Table for Intel Platform	L2 < 2.5"			
	TX EQ	TX FG	RX EQ	RX FG
L1 < 7"	R	R	R	0
7" <= L1 <= 9" (demo default)	F	R	R	F
9" < L1 < 10"	1	R	R	1

EQ/FG Setting Table for AMD Platform	L2 < 2"			
	TX EQ	TX FG	RX EQ	RX FG
L1 < 7"	R	R	R	0
7" <= L1 <= 9"	F	R	R	F
9" < L1 < 10"	1	R	R	1



Net	Impedance/Width	Space	Length
TX/RX L1	follow USB 3.1 Controller Rule	30 mils	< 10", prefer 5" - 9"
TX/RX L2		30 mils	< 2.5", prefer 0.5" - 1.5"
+3V_RDP2	>= PI3EQX1004 IC Count *20 mils		
Other Power Net	>= 20 mils		

L.1

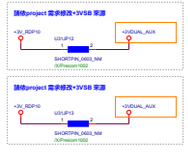
3.3V for PI3EQX1004 *1pcs, 340mA/pcs@S0

Power Component place near each other!

L.2

3.3V for PI3EQX1004 *2-3pcs, 340mA/pcs@S0

Vout=1.25*(2.15k+1.27k)/1.27k=3.366V



Power Component place near each other!

L.3

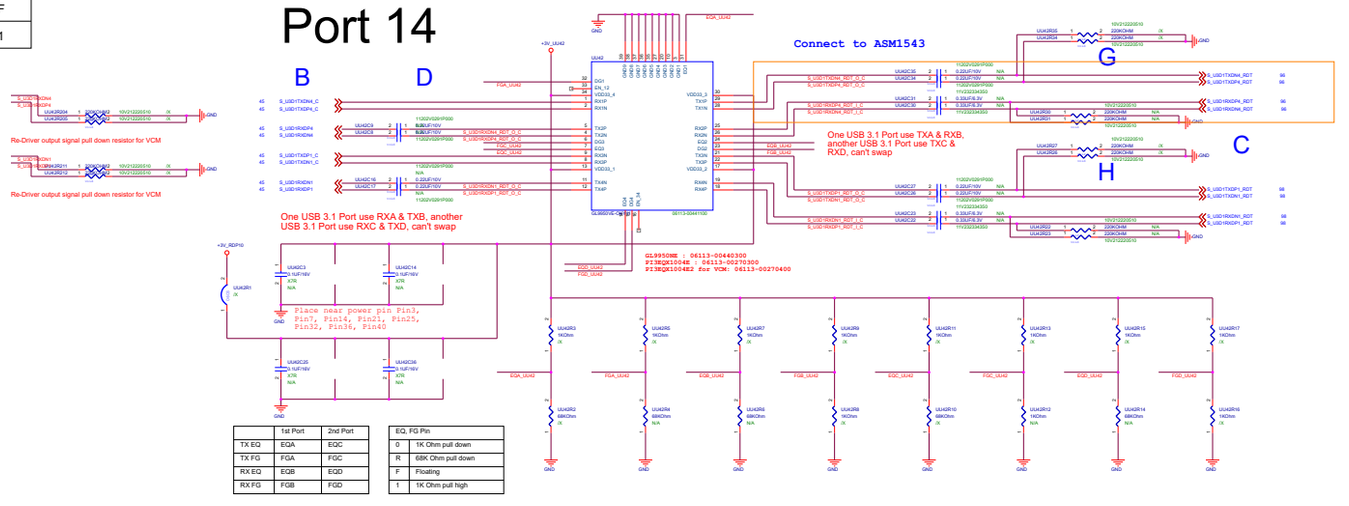
3.3V Stand By Power (not ATX Power) from LAN1 Dual MOS Power which could provide large current 3V power

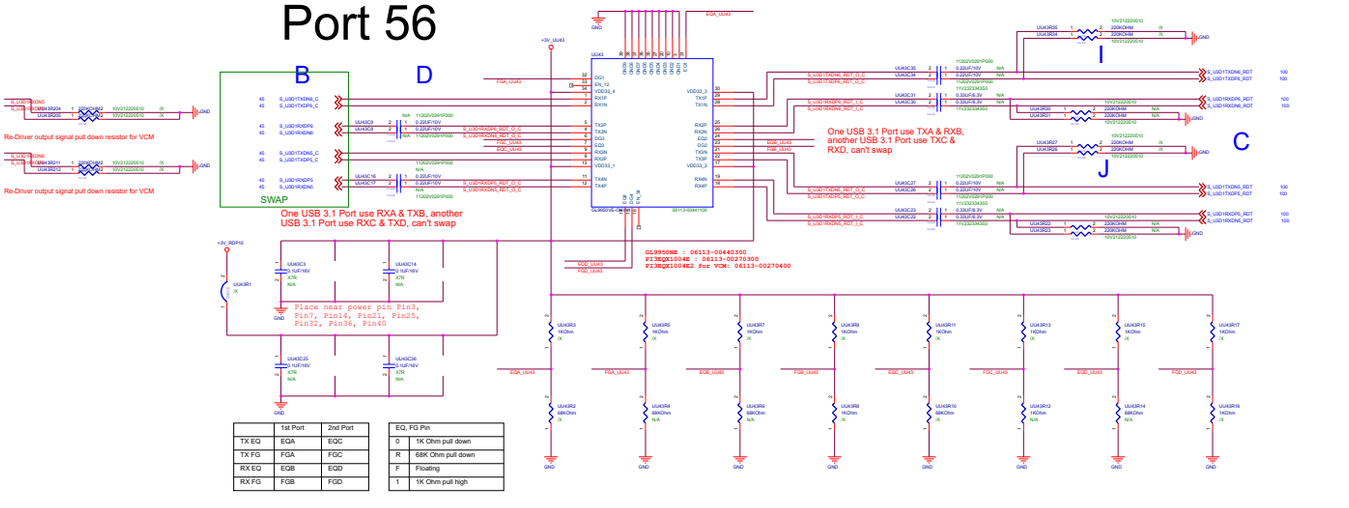
L.4

3.3V Stand By Power (not ATX Power) from LAN2 Dual MOS Power which could provide large current 3V power

L.5

3.3V Stand By Power (not ATX Power) from Wifi Dual MOS Power which could provide large current 3V power





Title : PI3EQX1004
Engineer: SZ Design IP
ASUSTeK COMPUTER INC.
Chipset USB Re-Driver

請確認是否為 USB3.1GEN1 或GEN2
1.GEN1請選擇2.6A/GEN2請選擇3.5A
2. 兩個port共用一組OCP & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

Connect to Chipset

Connect to Redriver or Retimer

Connect to Redriver or Retimer

請確認USB訊號是否為 USB3.1GEN1 或GEN2
1.預設 For GEN2，使用VR1.
2. For GEN1，電阻請改 temp_M05_0040,
Choke請改 09V949003000.

請確認USB訊號是否為 USB3.1GEN1 或GEN2
1.預設 For GEN2，使用VR1.
2. For GEN1，電阻請改 temp_M05_0040,
Choke請改 09V949003000.

Reserve for EMI

ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

ESD檔框選擇方式:

Connect to Connector

USB31_1

USB31_2

USB1

USB2

USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

U31 GEN2 & GEN1 PIN ESD 檔框選擇方式:

檔框 / 組合	A	B
U31 GEN 2 PIN ESD	Keep	Delete
U31 GEN 1 PIN ESD	Delete	Keep

A

U31GEN2 PIN ESD

Port 1

A

U31GEN2 PIN ESD

Port 2

Port 1,2

C

Title :	CHIPSET U31_Port1,2
Engineer:	Eddie Chiu
Size	A2
Project Name	Standard Circiut
Rev	2.7
Date:	Wednesday, July 06, 2022
Sheet	88 of 101

請確認是否為 USB3.1GEN1 或GEN2
1.GEN1請選擇2.6A/GEN2請選擇3.5A
2. 兩個port共用一組OC# & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

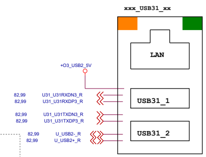
Connect to Chipset

以下 16 顆零件需請板卡課協助幫忙開銅板
UR84~UR87 U31R123~U31R130

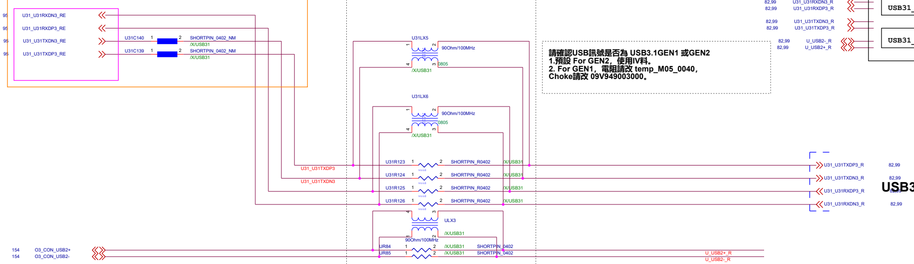
USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

Connect to Connector



Connect to Redriver or Retimer



請確認USB訊號是否為 USB3.1GEN1 或GEN2
1.預設 For GEN2，使用IV料。
2. For GEN1，電阻請改 temp_M05_0040，
Choke請改 09V949003000。

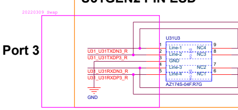
U31 GEN2 & GEN1 PIN ESD 橋框選擇方式:

橋框 / 組合	A	B
U31 GEN 2 PIN ESD	Keep	Delete
U31 GEN 1 PIN ESD	Delete	Keep

Port 3

A

U31GEN2 PIN ESD



B

U31GEN1 PIN ESD

Port 5

A

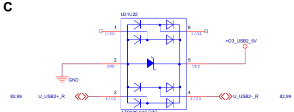
U31GEN2 PIN ESD

B

U31GEN1 PIN ESD

C

Port 3,4



<Variant Name>

ASUSTeK COMPUTER INC	Title : CHIPSET U31_Port3,4
	Engineer: Eddie Chiu
Size: A2	Project Name: Standard Circiut	Rev: 2.7
Date: Wednesday, July 06, 2022	Sheet 99 of 170

請確認是否為 USB3.1GEN1 或GEN2
1.GEN1請選擇2.6A/GEN2請選擇3.5A
2. 兩個port共用一顆OCP & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

Connect to Chipset

Connect to Redriver or Retimer

Connect to Connector

USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

請確認USB訊號是否為 USB3.1GEN1 或GEN2
1.預設 For GEN2，使用IV料。
2. For GEN1，電阻調改 temp_M05_0040，
Choke調改 09V949003000。

USB5

USB6

ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

ESD機構選擇方式:

Reserve for EMI

U31 GEN2 & GEN1 PIN ESD 機構選擇方式:

機構 / 組合	A	B
U31 GEN 2 PIN ESD	Keep	Delete
U31 GEN 1 PIN ESD	Delete	Keep

A

U31GEN2 PIN ESD

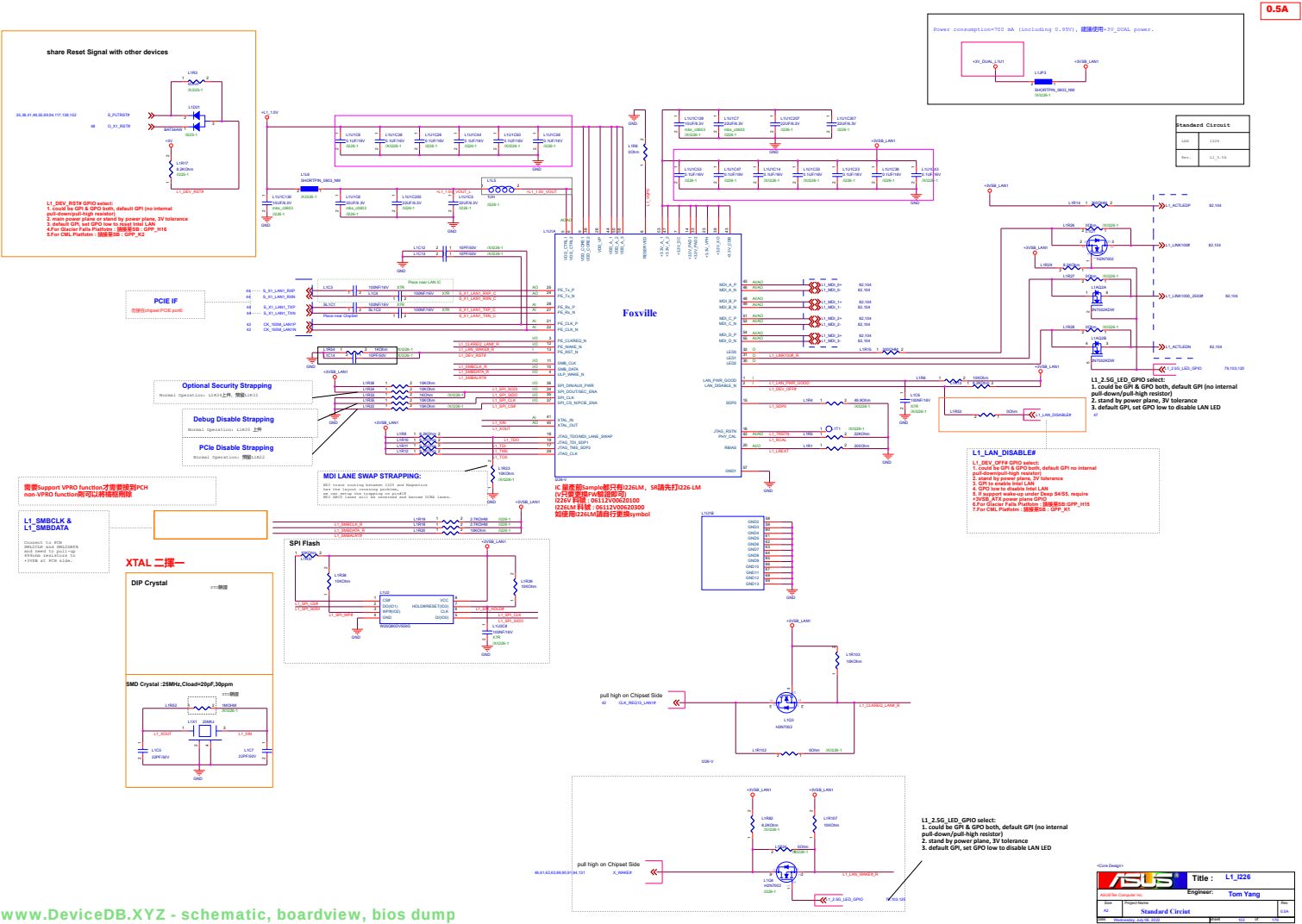
Port 5

Port 6

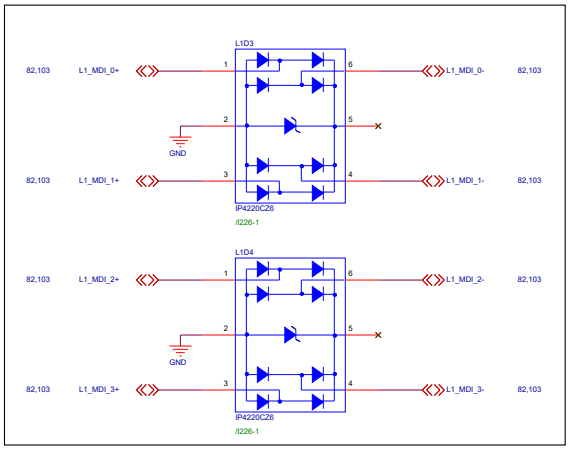
C

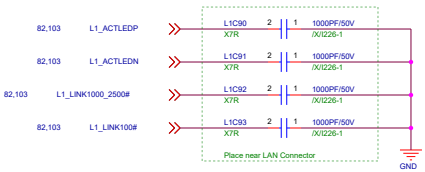
Port 5,6

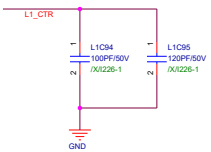
Title : CHIPSET U31_Port5,6
Engineer: Eddie Chiu
Standard Circuit



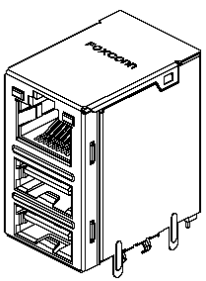
Delete it for EMS STD驗證







Choose a proper LAN Connector in page Back I/O Connector



L1_ACTLEDP
L1_ACTLEDN

GND

L1_MDI_3-
L1_MDI_3+
L1_MDI_2-
L1_MDI_2+
L1_MDI_1-
L1_MDI_1+
L1_MDI_0-
L1_MDI_0+

82 L1_CTR

L1_LINK1000#
L1_LINK100#

L1C46 1UF/10V /X/I226-1
GND

Place capacitors near the Lan Connector.
Maybe need to be modified according to the different EMI consideration.

<Core Design>

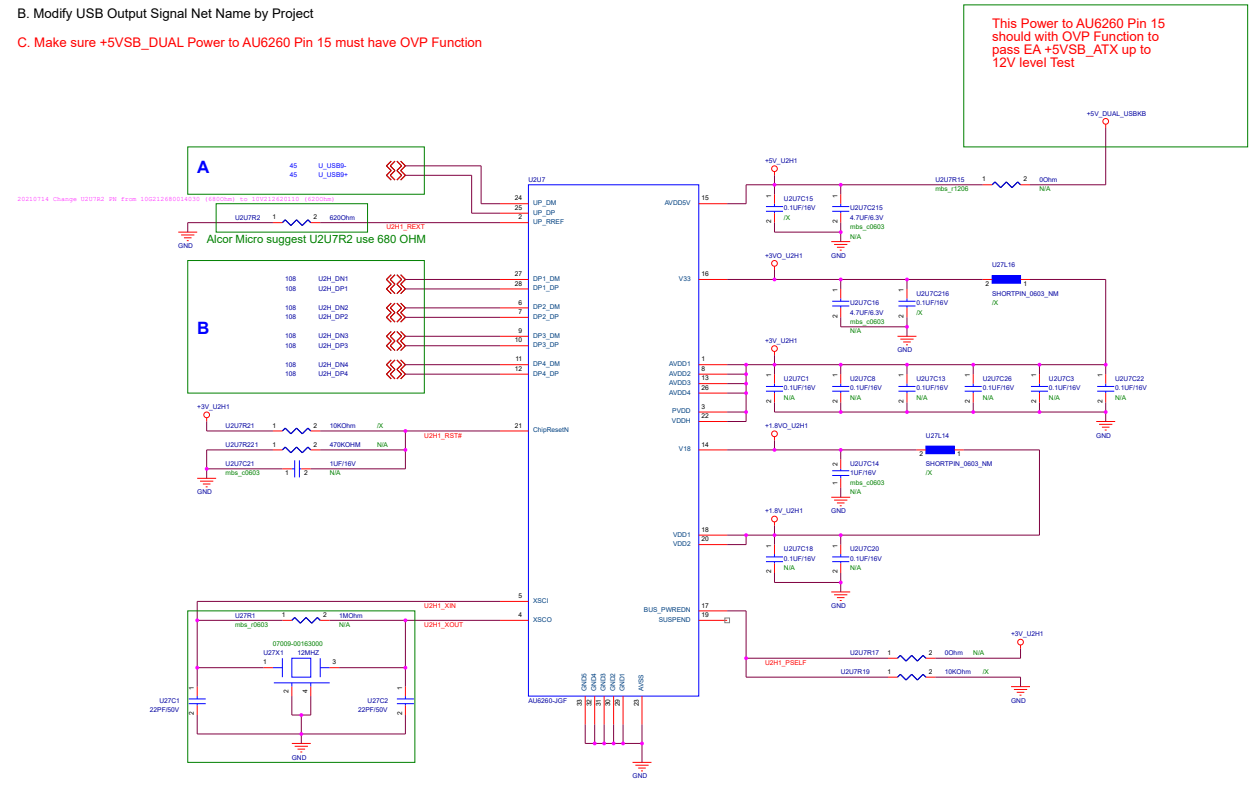
ASUSTek Computer Inc.	Title : L1_I226_Connector	
	Engineer: Tom Yang	
Size: A3	Project Name: Standard Circiut	Rev: 0.5A
Date: Wednesday, July 06, 2022	Sheet 104 of 170	

AU6260 Circuit

A. Modify USB Input Signal Net Name by Project

B. Modify USB Output Signal Net Name by Project

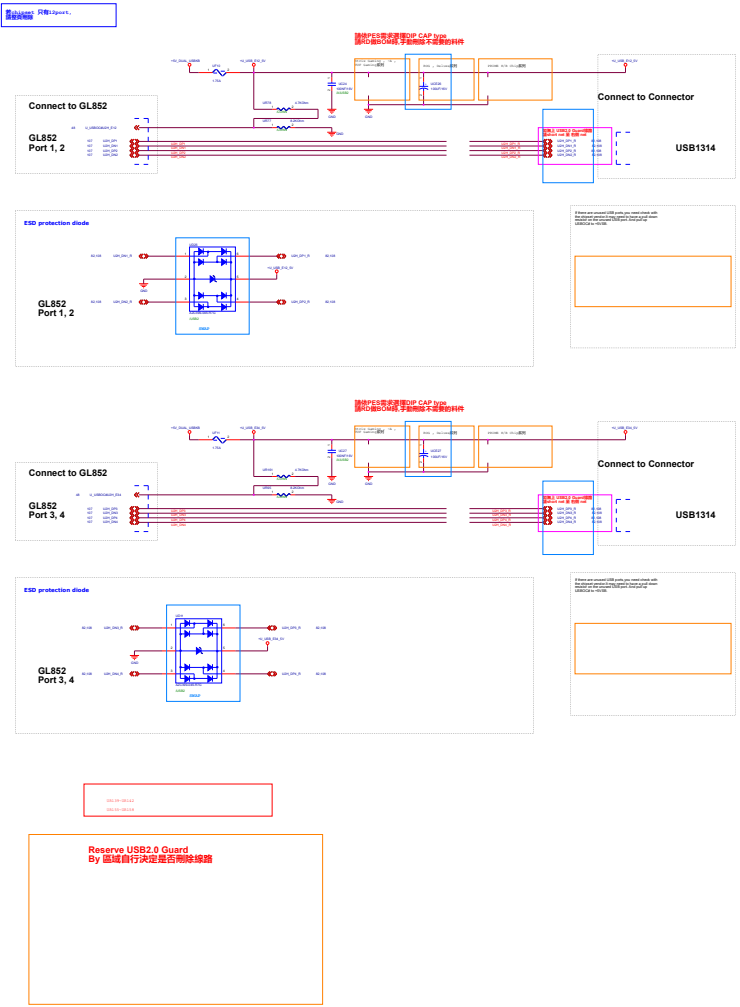
C. Make sure +5VSB_DUAL Power to AU6260 Pin 15 must have OVP Function

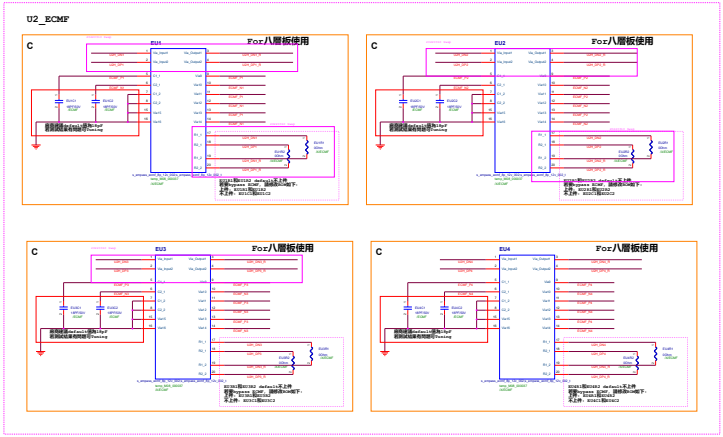


BOM	
N/A	mount
/X	unmount

<Variant Name>

ASUSTEK COMPUTER INC	Title : AU6260	
	Engineer: SZ Design IP	
Size: A3	Project Name: USB2 Hub Demo Circuit	Rev: 0.0
Date: Wednesday, July 06, 2022	Sheet 107 of 170	



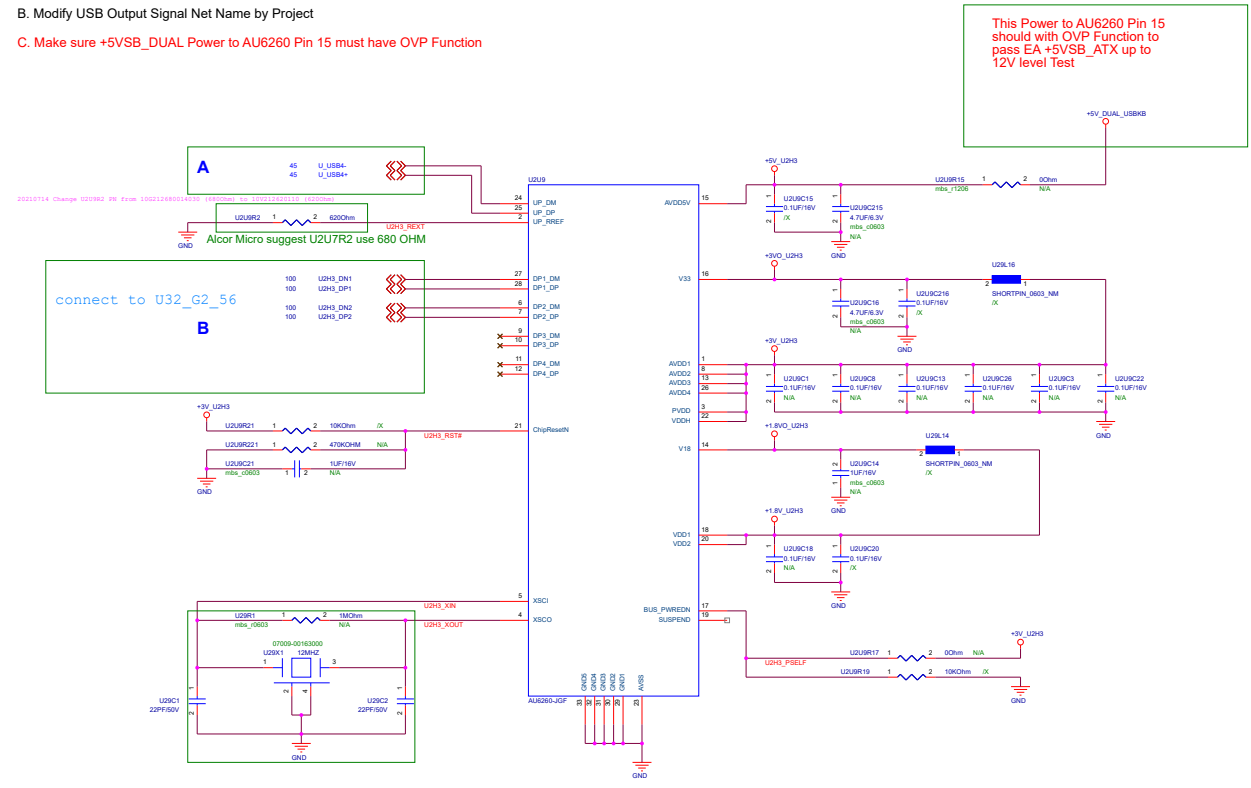


AU6260
Circuit

A. Modify USB Input Signal Net Name by Project

B. Modify USB Output Signal Net Name by Project

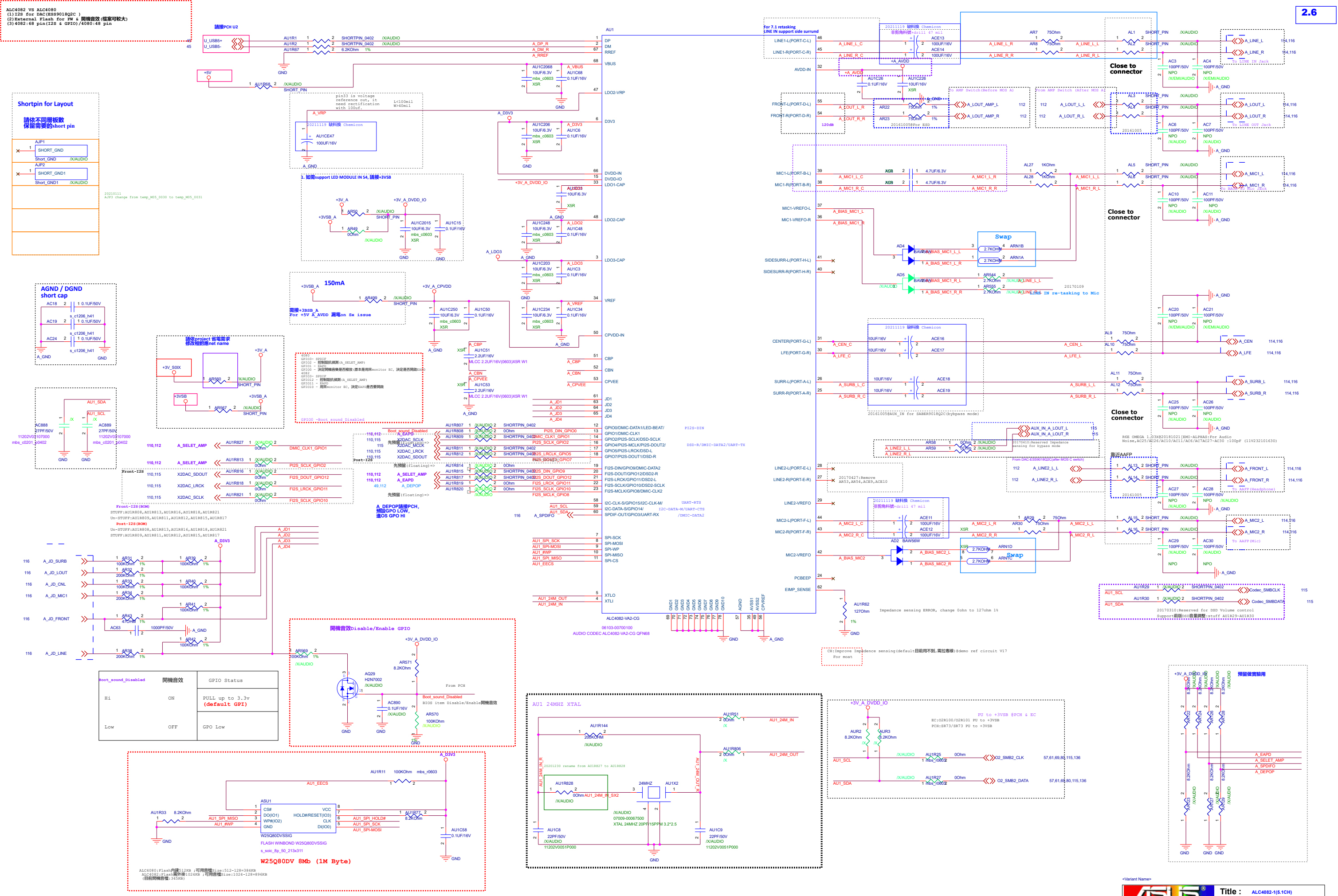
C. Make sure +5VSB_DUAL Power to AU6260 Pin 15 must have OVP Function



BOM	
N/A	mount
/X	unmount

<Variant Name>

ASUSTEK COMPUTER INC	Title : AU6260	
	Engineer: SZ Design IP	
Size: A3	Project Name: USB2 Hub Demo Circuit	Rev: 0.0
Date: Wednesday, July 06, 2022	Sheet 109 of 170	



Size	Project Name	Rev
A2	Standard Circiut	2.3

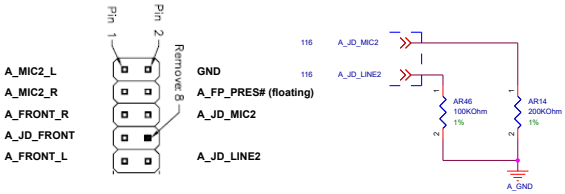
Title : ALC4082-1(5.1CH)

ASUSTek Computer Inc.

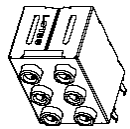
Engineer:

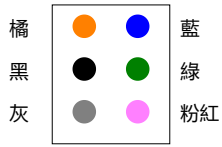
Date: Wednesday, July 06, 2022 Sheet 110 of 170

Front Panel

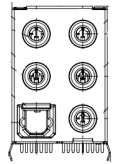


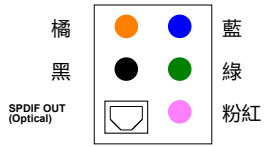
Back Panel
7.1 Channel Connector(示意圖)



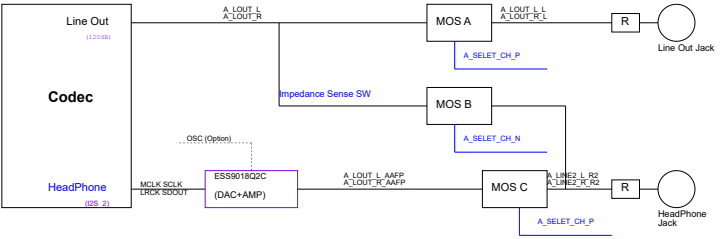


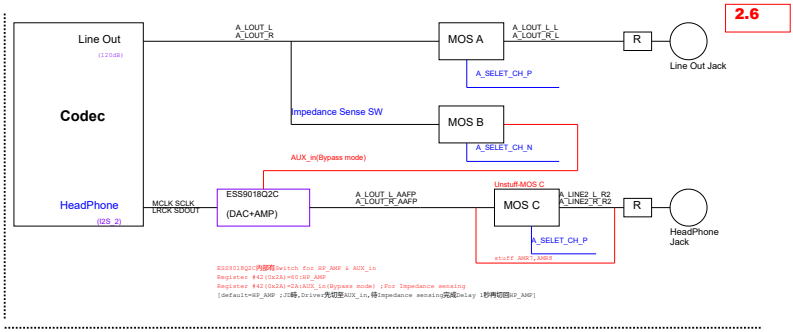
Back Panel
5.1Channel Connector
+SPDIF OUT(Optical)(示意圖)



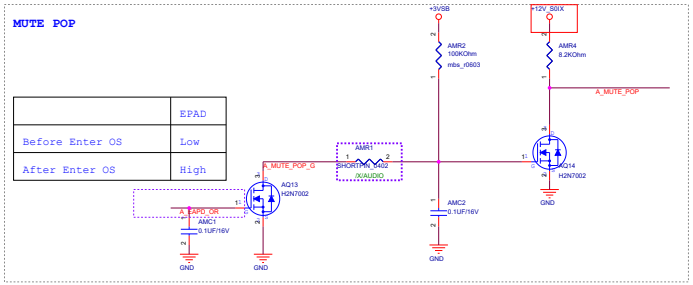


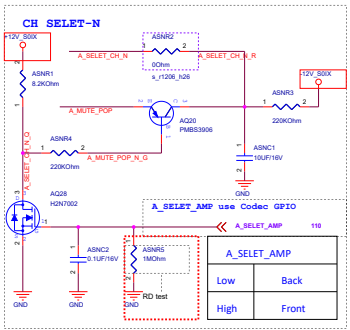
SPDIF OUT (Optical)(示意圖)

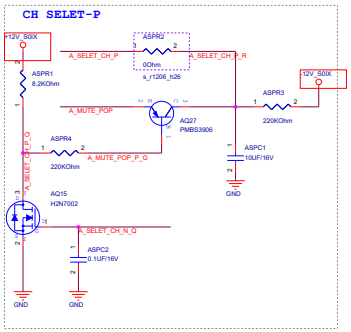


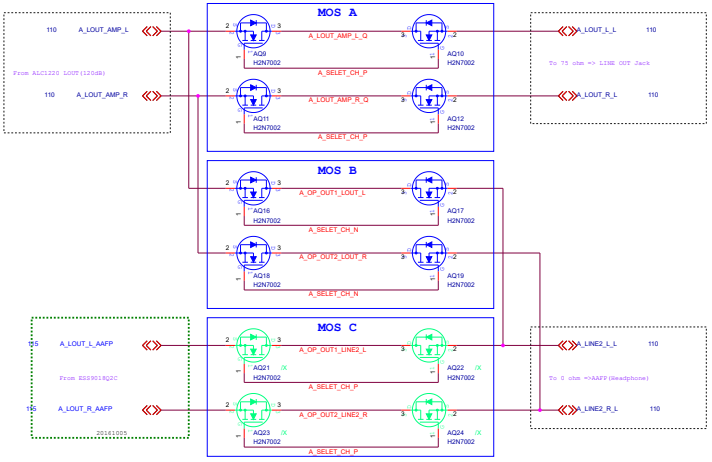


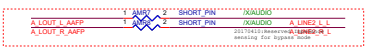
SELET_CH_P	SELET_CH_N	MOS A&C	MOS B	
-12V	-12V	Off	Off	De-POP for Power On & Power Off
+12V	-12V	On	Off	Impedance sensing for Lout Jack
-12V	+12V	Off	On	Impedance sensing for HP Jack
+12V	+12V	On	On	Not Allowed

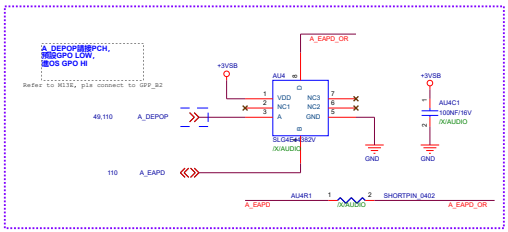


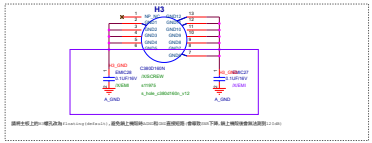






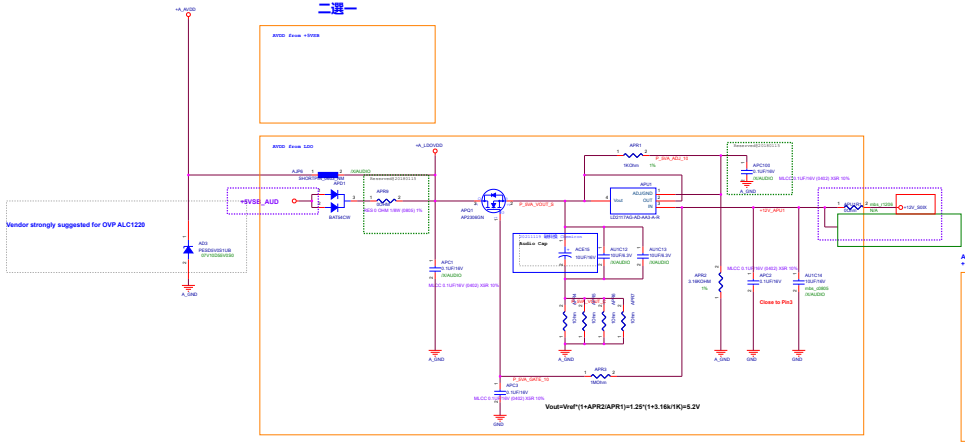




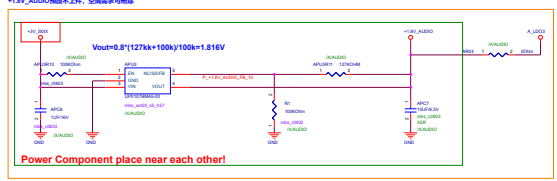


請依PES是否有上LDO 選擇相對應線路

二選一



Audio滿載情況下，LDO3會有少許電壓浮動。
+1.8V_AUDIO開啟不上件，空間需求可開放



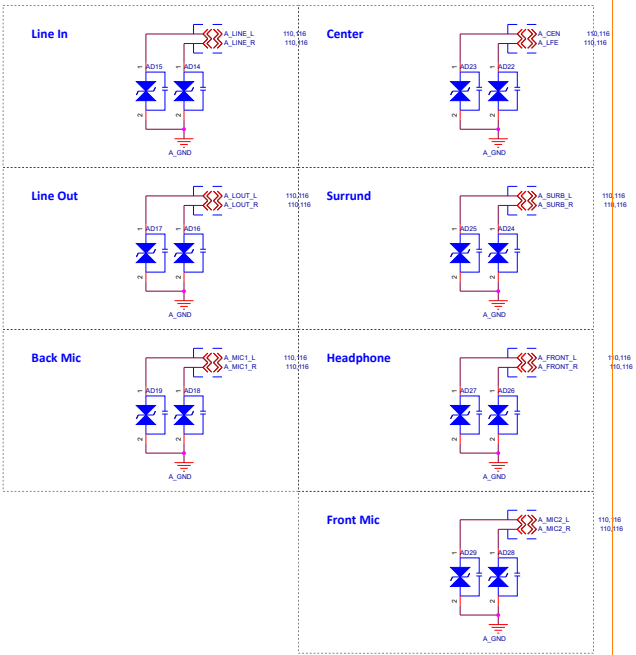
VARISTOR

Pin ESD spec (自Z370起spec)

Line Out	Headphone	Center	Surrund	Front Mic	Line In	Back Mic
5KV	5KV	4.5KV	4.5KV	5KV	4.5KV	5KV

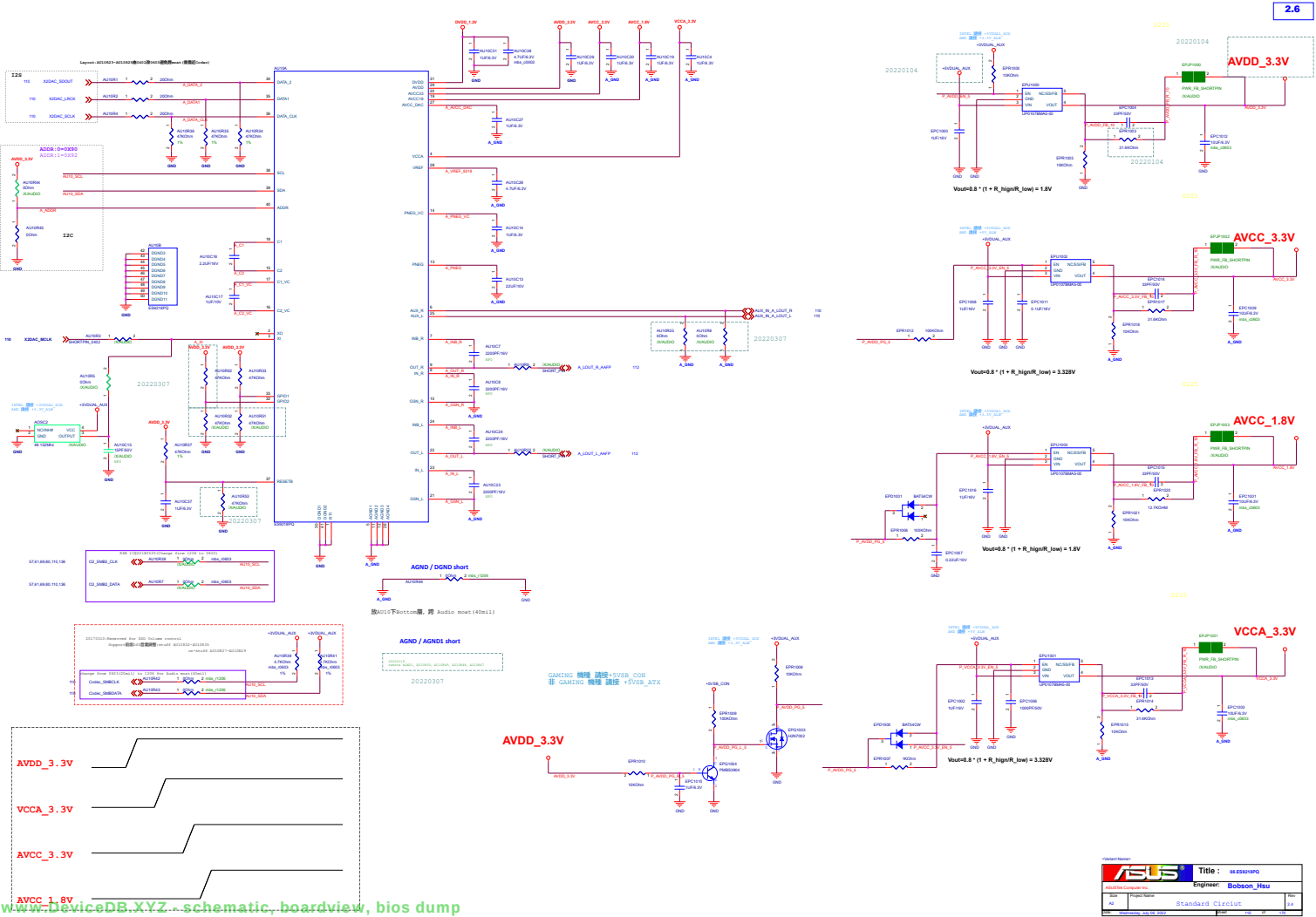
For Strix model (ESD Spec: 5KV)
For TUF model (ESD Spec: 8KV)

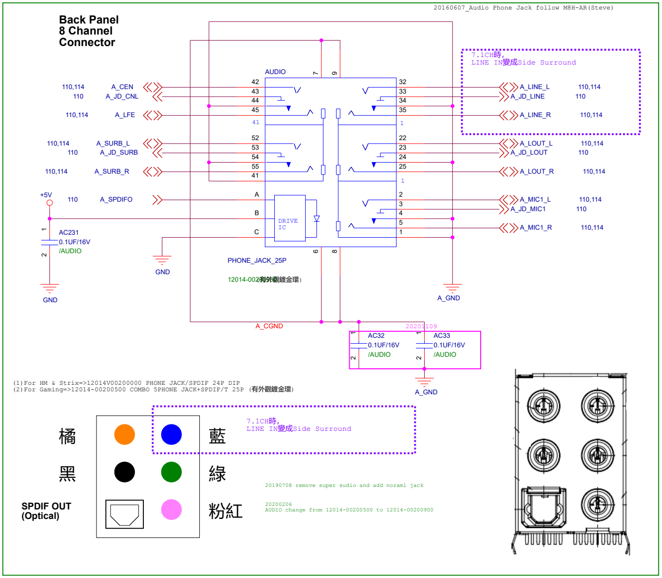
Default 全部Varistor皆需上件



<Variant Name>

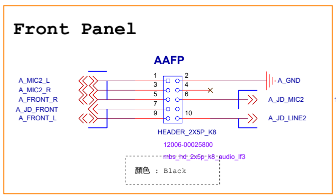
ASUSTek Computer Inc.	Title : ALC1220-S (VARISTOR)	
	Engineer: Bobson Hsu	
Size: A3	Project Name: Standard Circiut	Rev: 2.3
Date: Wednesday, July 06, 2022	Sheet 114 of 170	





20160607_Audio Phone Jack follow M8H-AR(Steve)
Back Panel
8 Channel
Connector
AUDIO
110,114 A_CEN
110 A_JD_CNL
110,114 A_LFE
110,114 A_SURB_L
110 A_JD_SURB
110,114 A_SURB_R
+5V
110 A_SPDIFO
AC231
0.1UF/16V
/AUDIO
GND
DRIVE IC
PHONE_JACK_25P
12014-002(有外觀鍍金環)
7.1CH時,
LINE IN變成Side Surround
A_LINE_L 110,114
A_JD_LINE 110
A_LINE_R 110,114
A_LOUT_L 110,114
A_JD_LOUT 110
A_LOUT_R 110,114
A_MIC1_L 110,114
A_JD_MIC1 110
A_MIC1_R 110,114
A_GND
A_CGND
20201109
AC32
0.1UF/16V
/AUDIO
AC33
0.1UF/16V
/AUDIO
A_GND
(1)For HM & Strix=>12014V00200000 PHONE JACK/SPDIF 24P DIP
(2)For Gaming=>12014-00200500 COMBO 5PHONE JACK+SPDIF/T 25P (有外觀鍍金環)
橘
黑
SPDIF OUT
(Optical)
藍
綠
粉紅
7.1CH時,
LINE IN變成Side Surround
20190708 remove super audio and add noraml jack
20200206
AUDIO change from 12014-00200500 to 12014-00200900

20190708 remove led control



20170308:Remove AUDIO_COVER

<Variant Name>

ASUSTek Computer Inc.	Title :	BACK IO_AUDIO	
	Engineer:	Tom Yang	
Size: A3	Project Name	Standard Circuit	Rev: 4.8
Date: Wednesday, July 06, 2022		Sheet 116 of 170	

LN2 Mode

20190704 remove LN2_MODE:12
20190918 Add LN2_MODE:12
20200714 Remove LN2_MODE:12

Switch	COLD_BOOT1
1-2	CPU_PLL 1.8V OFF
2-3	CPU_PLL 1.5V ON

20200130 rename from +VCCST to +V1P05A_CPU

+V1P05A_CPU

HR3029
1KOhm
/XLGA2011

6CR29 0Ohm /Game

EC1/SB

79 H_THERMTRIP#_SB

CPU

H_THERMTRIP# 35,46

20200117
unstuff LN2_MODE:12
20200807
Remove LN2_MODE:12

20190704
unstuff HR3029
stuff 6CR29
remove 6CQ99

20190918
stuff HR3029
unstuff 6CR29
add 6CQ99

20200714
unstuff HR3029
stuff 6CR29
remove 6CQ99

EC1 pin

Pin name	Net name	Function name
P4[4]	O2_GPI1	VRMPWRGD
P8[3]	O2_GPO1	O2_VRMPWRGD
P2[6]	O2_GPO2	O2_LGSPARE_0_OC
P2[7]	O2_GPO3	O2_LGSPARE_1_OC

20190704
remove R3VO_SWITCH, SLIDE_SWITCH_3P

20140410:Modify circuit for PLTRST時EC不控制

H_PROCHOT# 6,12,35

+3VSB

79 PROCHOT_EC

6CR3
8.2KOhm

HQ103
H2N7002

HQ102
H2N7002

6CR6
8.2KOhm

HQ104
H2N7002

GND

35,38,41,49,55,69,94,103,138,152 S_PLTRST#

20190704
remove SLOW_MODE

SLOW_MODE_CTL
Default=Low (off)
Active=High(on)
LN2 Mode
Default=High(off)
Active=Low(on)

High:Disable LN2 mode & slow mode

Modify80825

+5VSB ====>+3VSB_EC

<Variant Name>

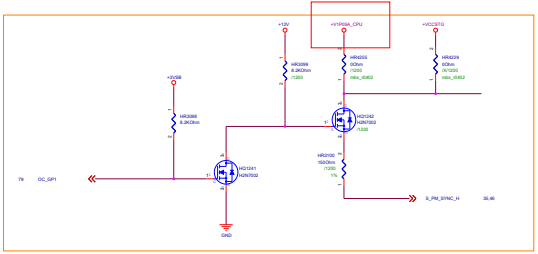
ASUSTek Computer Inc.

Title : LN2 Mode & Slow mode

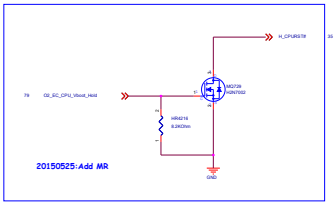
Engineer: Aaron_Su

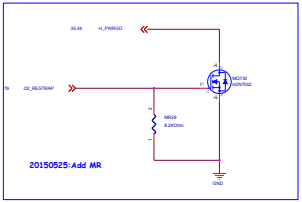
Size	Project Name	Rev
A3	Maximus XI Extreme	R1.01

Date: Wednesday, July 06, 2022 Sheet 117 of 170



Only for M14E and Apex





<Variant Name>

ASUSTeK COMPUTER INC	Title :	OC	
	Engineer:	Peter tan	
Size: A2	Project Name:	Maximus XI Extreme	Rev: 00.01
Date: Wednesday, July 06, 2022	Sheet	118 of 130	

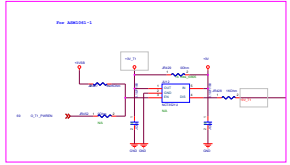
<Variant Name>

ASUSTEK COMPUTER INC	Title : +VCCCMP/+VCCIO_G	
	Engineer: Aaron_Su	
Size: A2	Project Name: ROG MAXIMUS Z790 HERO	Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 119 of 170	

ADM1074-2 (Back)

ADM1074

WIFI



GL3590

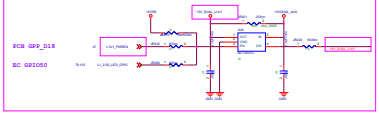
1225V

PCH GPP_D18

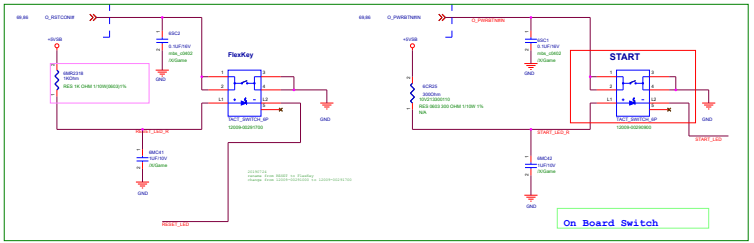
SIO GP_91

Q_LIU1_PWREN 0ohm, high 靠位在SIO端

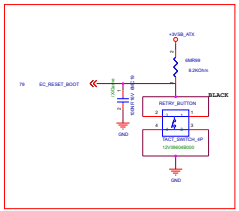
1224V

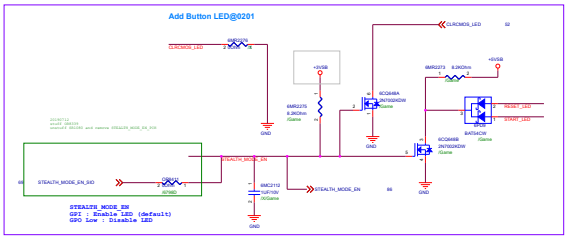


Title : Power Cut off - detect
Engineer: Aaron_Su
Maximus XI Extreme



OC Button Circuit
20170508 Allen Remove





PCH Voltage LED

DDR_CD Voltage LED

CPU Voltage LED

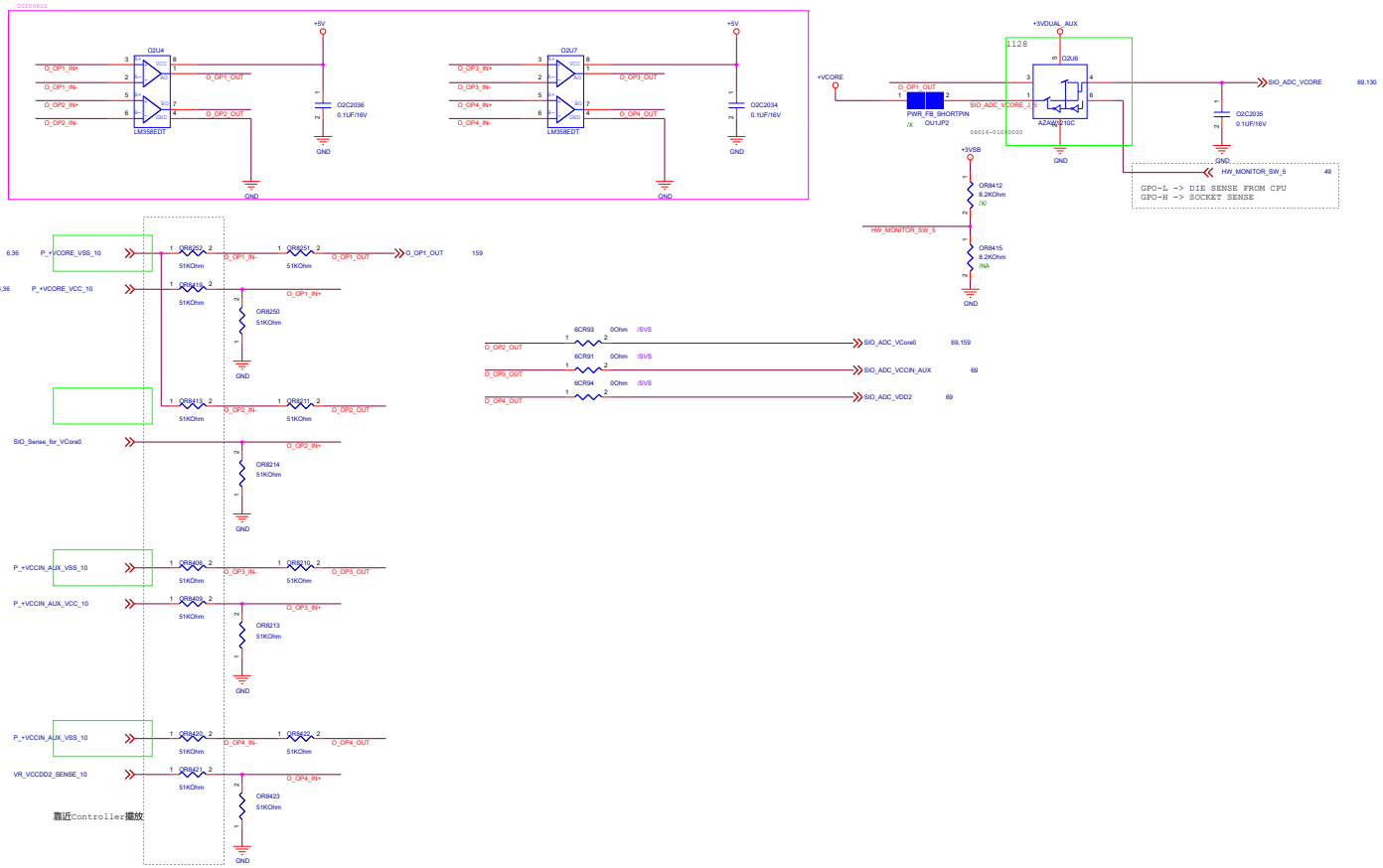
DDR_AB Voltage LED

**重要

1.6G_ROG_SW請選擇Stand by仍有電的GPIO。

當LED點亮時,LED=端2.84V
I=(5.2-3.61)/0.33=6.54mA
電流流過排阻的P=(6.54)^2*0.33=0.014W
Spec(0603)=1/10W>0.014W

<Variant Name>
Title : ROG button
Engineer: Aaron_Su
ASUSTeK Computer Inc.
Size: A2 | Project Name: Maximus XI Extreme | Rev: 0.01
Date: Wednesday, July 06, 2022 | Sheet 122 of 170



<Variant Name>

ASUSTek Computer Inc.	Title : SIO Sense	
	Engineer: Jon	
Size: A3	Project Name: Maximus XIII Extreme	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 123 of 170	

Part For ROG Only

Page	Part Name	Note
108	UF2	
109	UF8	
110	UF4	
111	UF9	
112	UF6	
115	U3EF1	
118	UF7	
131	LED1_F1	
131	LED1_F2	
133	LED1_F3	
133	LED1_F4	
135	OSDF3	
39 40	DIMM_A1 DIMM_A2 DIMM_B1 DIMM_B2	
73	OR8081 OR8082	
73	OR8065 OR8066 OR8067 OR8068	
73	OR8244	

<Variant Name>

ASUSTek Computer Inc.	Title : TMP007	
	Engineer: Aaron_Su	
Size: C	Project Name: ROG MAXIMUS Z790 HERO	Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 124 of 170	

For DOA/FA improvement

NET	TestPoint name	Note
H_SKTOCC#	AT3	
S_RTCRST#	AT4	
S_SRTCRST#	AT5	
S_INTRUDER#	AT6	
O_CASEOPEN#	AT88	

<Variant Name>

ASUSTEK COMPUTER INC	Title : DOA/FA improvement	
	Engineer: Aaron Su	
Size: A	Project Name: Maximus XI Extreme	Rev: R1.01
Date: Wednesday, July 06, 2022	Sheet 125 of 170	

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	V	V	temp_M01_000320

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	V	V	temp_T_001453

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	X	V	temp_T_001454

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	X	V	temp_T_001455

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	X	X	temp_T_001456

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	X	X	temp_T_001457

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X	V	X	temp_T_001458

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	V	X	temp_T_001486

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	V	X	temp_T_001487

請依PES選擇相對應文字框及修改流水號

M.2_1

PCIE	SATA	IRST
4_0 X4	X	V

TEXT_ M.2_25 /X

M.2_2

PCIE	SATA	IRST
4_0 X4	X	V

TEXT_ M.2_25 /X

M.2_3

PCIE	SATA	IRST
4_0 X4	V	V

TEXT_ M.2_24 /X

John 20200706

<Variant Name>

ASUSTEK COMPUTER INC

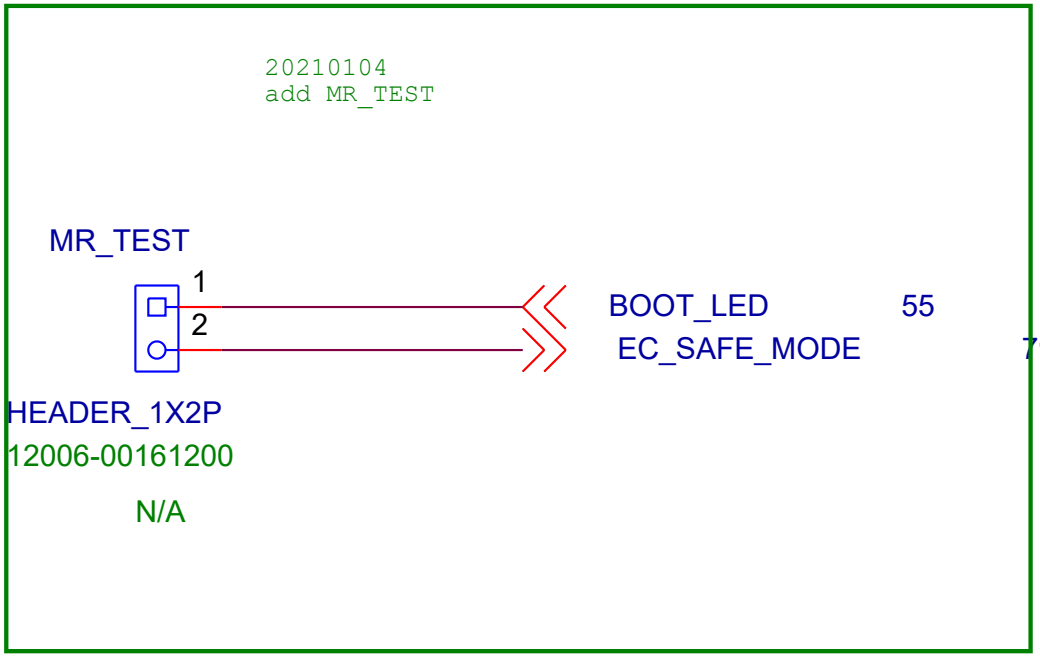
Title : M2_TEXT

Engineer: Grace Wu

Size	Project Name	Rev
A3	Silkscreen	0.2N

Date: Wednesday, July 06, 2022 Sheet 128 of 170

20210104
add MR_TEST



<Variant Name>

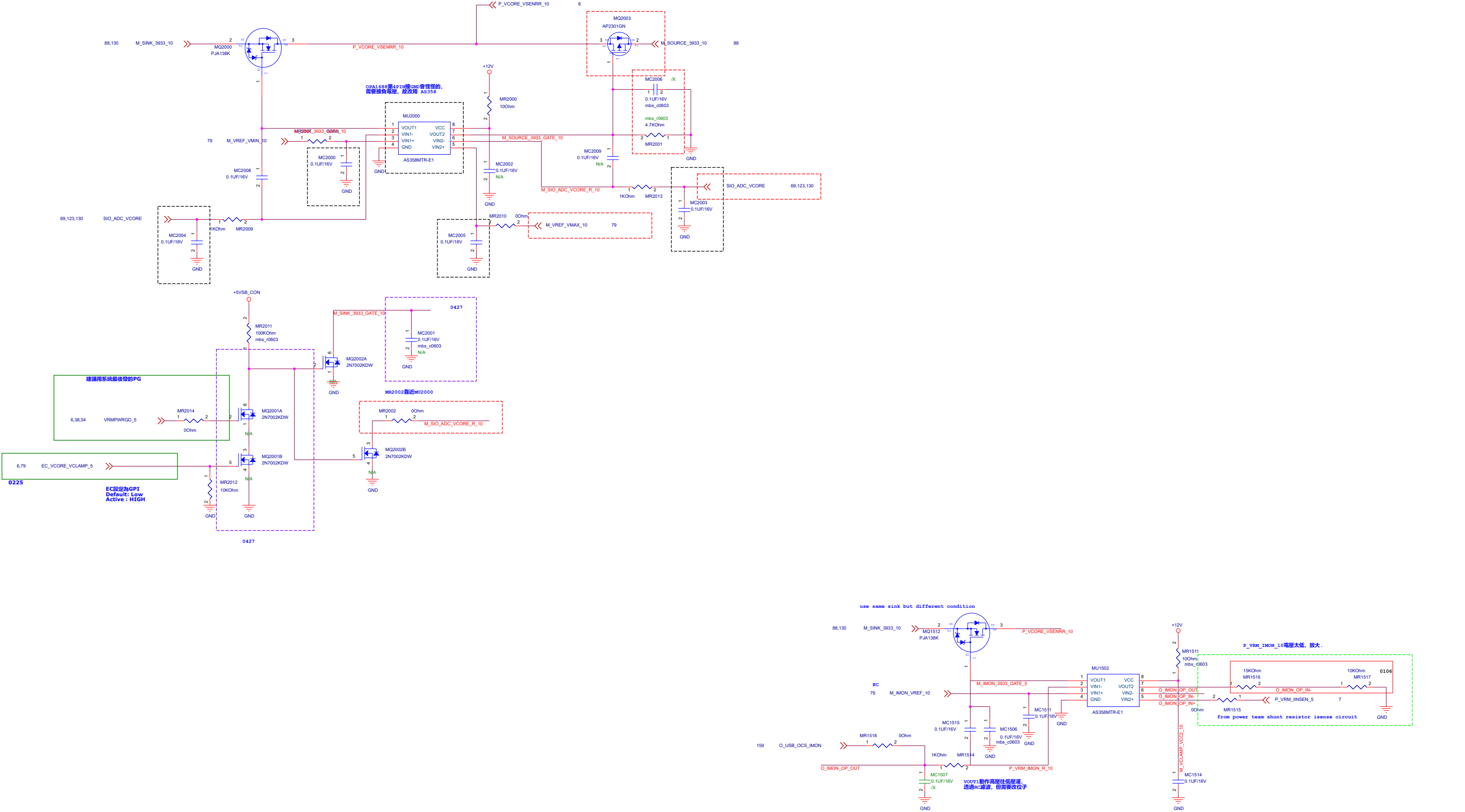
ASUSTeK COMPUTER INC

Title : OC

Engineer: Peter

Size	Project Name	Rev
A	ROG MAXIMUS Z790 HERO	2.1

Date: Wednesday, July 06, 2022 Sheet 129 of 170



<Variant Name>

ASUSTeK Computer Inc.

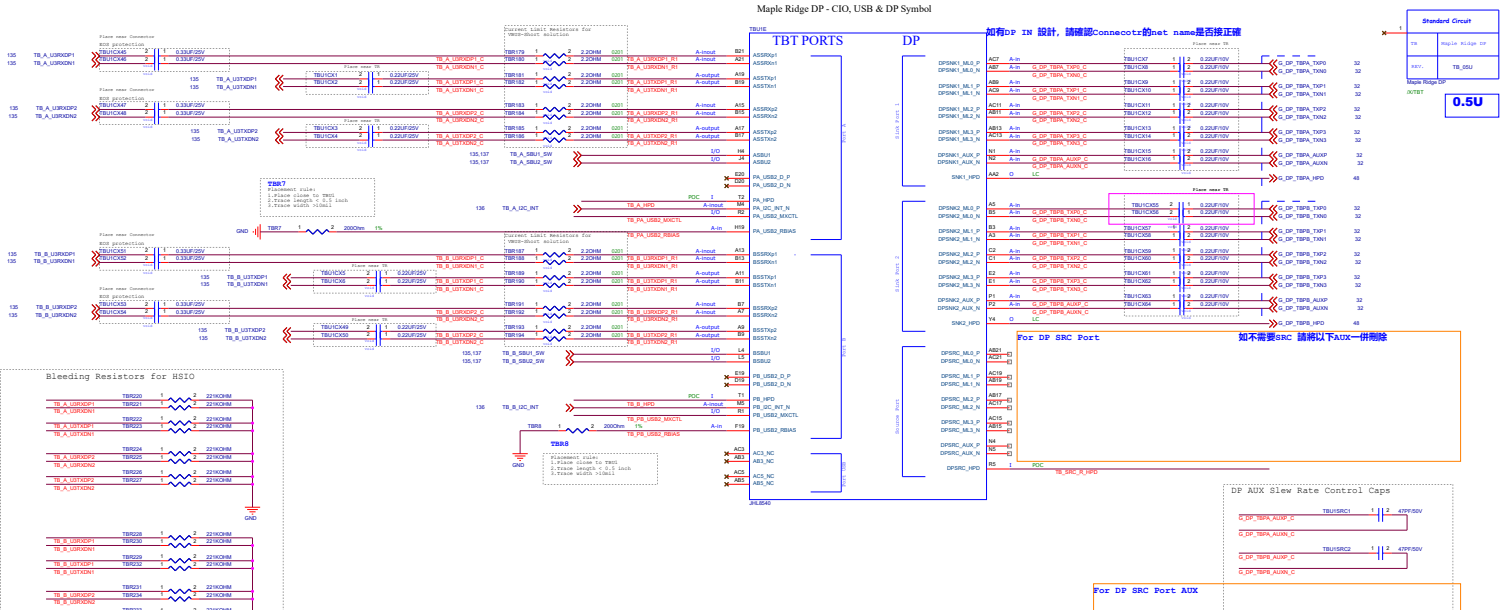
Title : CUT Circuit

Engineer: TOM

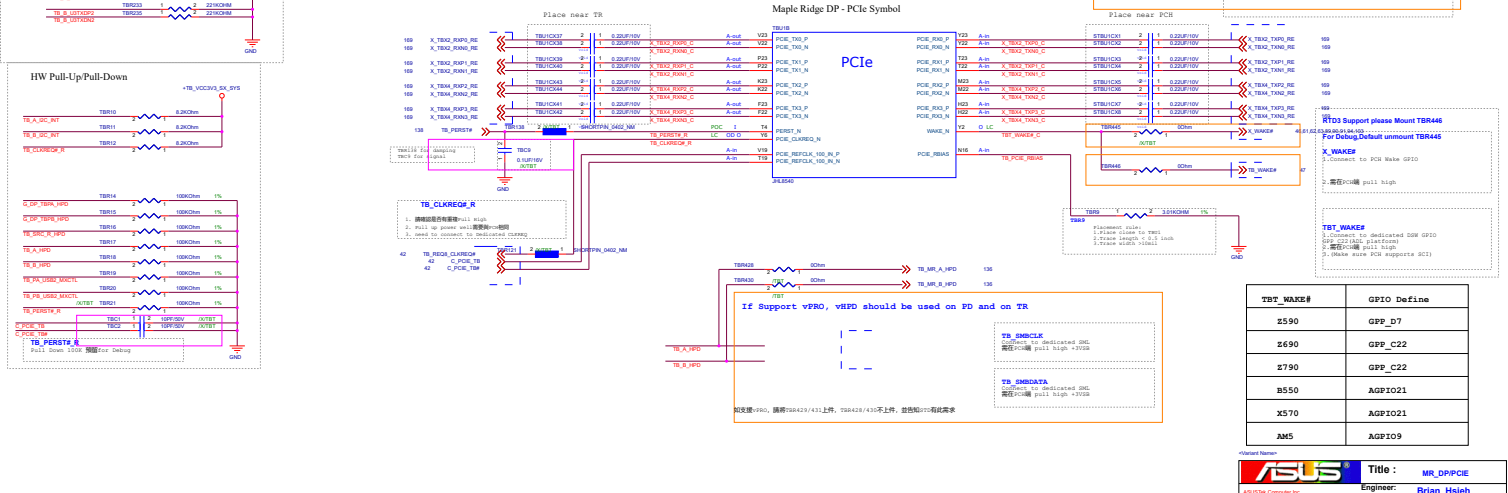
Size	Project Name	Rev
A2	BASIN FALLS_VC_	1.00

Date: Wednesday, July 06, 2022 Sheet 130 of 170

Maple Ridge DP - CIO, USB & DP Symbol

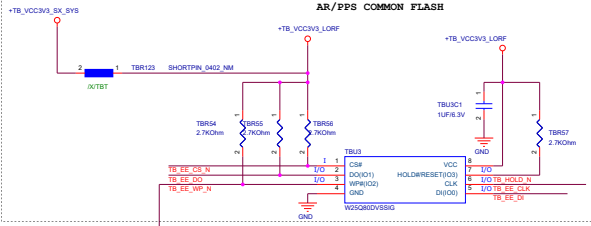


Maple Ridge DP - PCIe Symbol



0.5U

AR/PPS COMMON FLASH



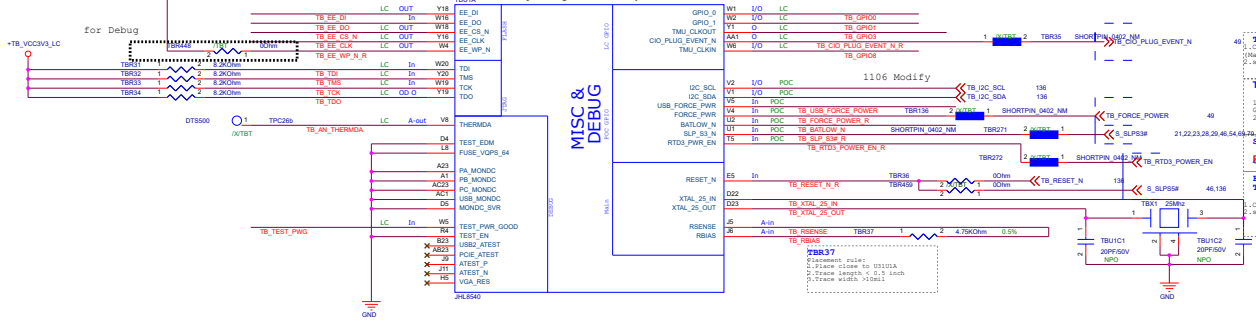
Flash Types Supported

Manufacturer	Type
AMIC	A25L080
Spansion	S25FL208K
Winbond	W25Q80DVSNIG
Macronix	MX25L8006EM1I
Micron	M25PE80-VMN6TP
Micron	M25PX80-VMN6TP

GPIO table

	TB_CIO_PLUG_EVENT_N	TB_FORCE_POWER	TB_RTD3_POWER_EN
Z590	GPP_K0	GPP_K4	GPP_F9
Z690	GPP_G7	GPP_G0	GPP_G1
Z790	GPP_G7	GPP_G0	GPP_G1
B550	AGPIO4	SIO_GP73	SIO_GP24
X570	AGPIO18	EGPIO42	EGPIO140
AM5	AGPIO7	AGPIO8	AGPIO12

Maple Ridge DP - Misc Symbol



TB_CIO_PLUG_EVENT_N:
0.Connect To GPIO GPP_G7 (ADL platfrom)
1Make sure PCH supports SCI)
2.select GPIO of +3V Main power domain

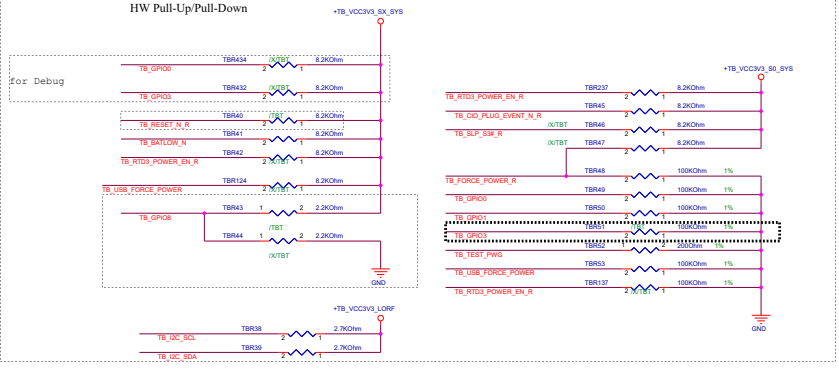
TB_FORCE_PWR
1.Connect to GPIO GPP_G0 default GPIO(LOW) (ADL platfrom)
2.select GPIO of +3V Main power domain

S_SLPS3#

PU should be on PCH side

For Support RTD3
TB_RTD3_POWER_EN
1.Connect to PCH GPP_G1(ADL platfrom)
2.select GPIO of +3V Main power domain

HW Pull-Up/Pull-Down

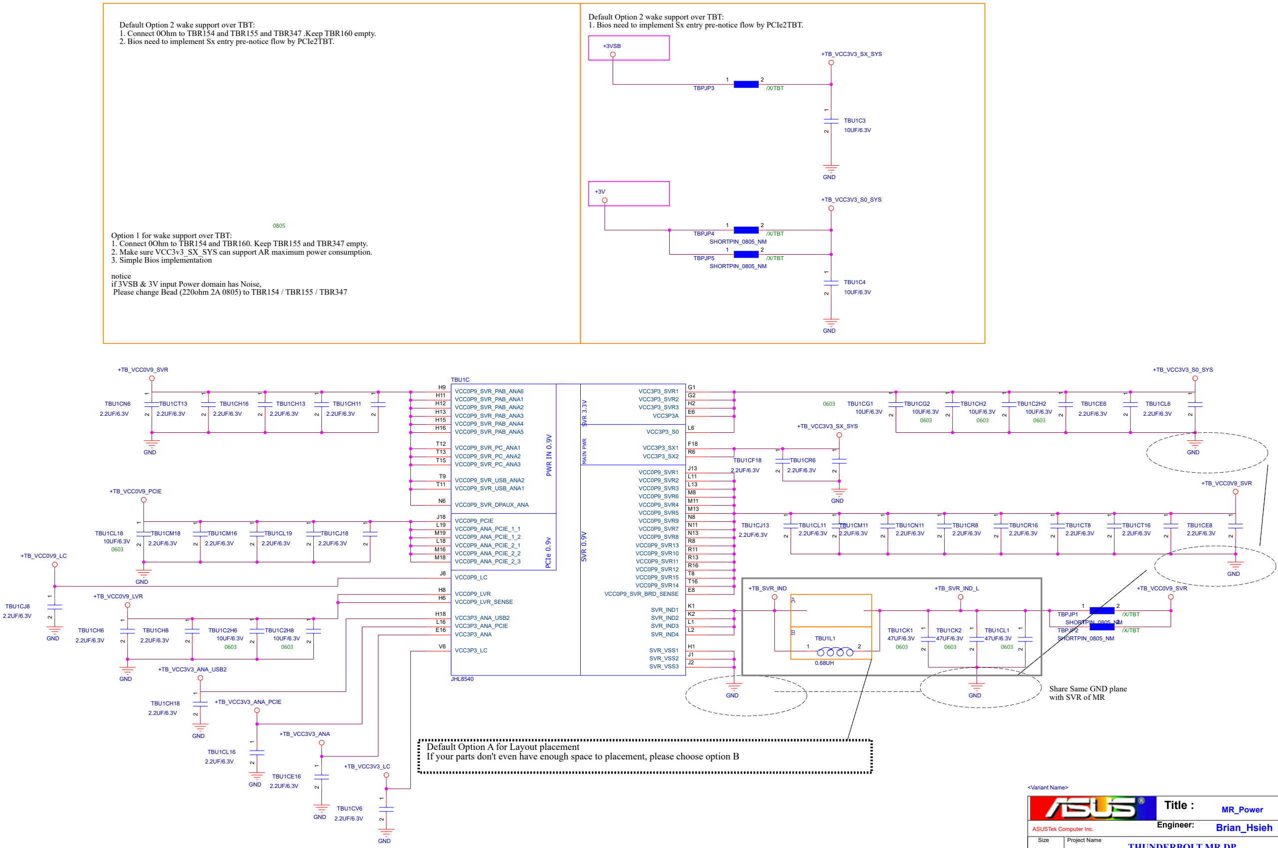


<Variant Name>

ASUSTek Computer Inc.	Title :	MR_MISC	
	Engineer:	Brian_Hsieh	
Size: A3	Project Name: THUNDERBOLT MR DP		Rev: 0.5T
Date: Wednesday, July 06, 2022	Sheet: 132	of: 170	

0.5U

left circuit and right circuit default值一樣(option2 support wake),the same BIOS porting
left circuit for STD reserve debug experiment,請RD依需求手動刪掉不要橘框



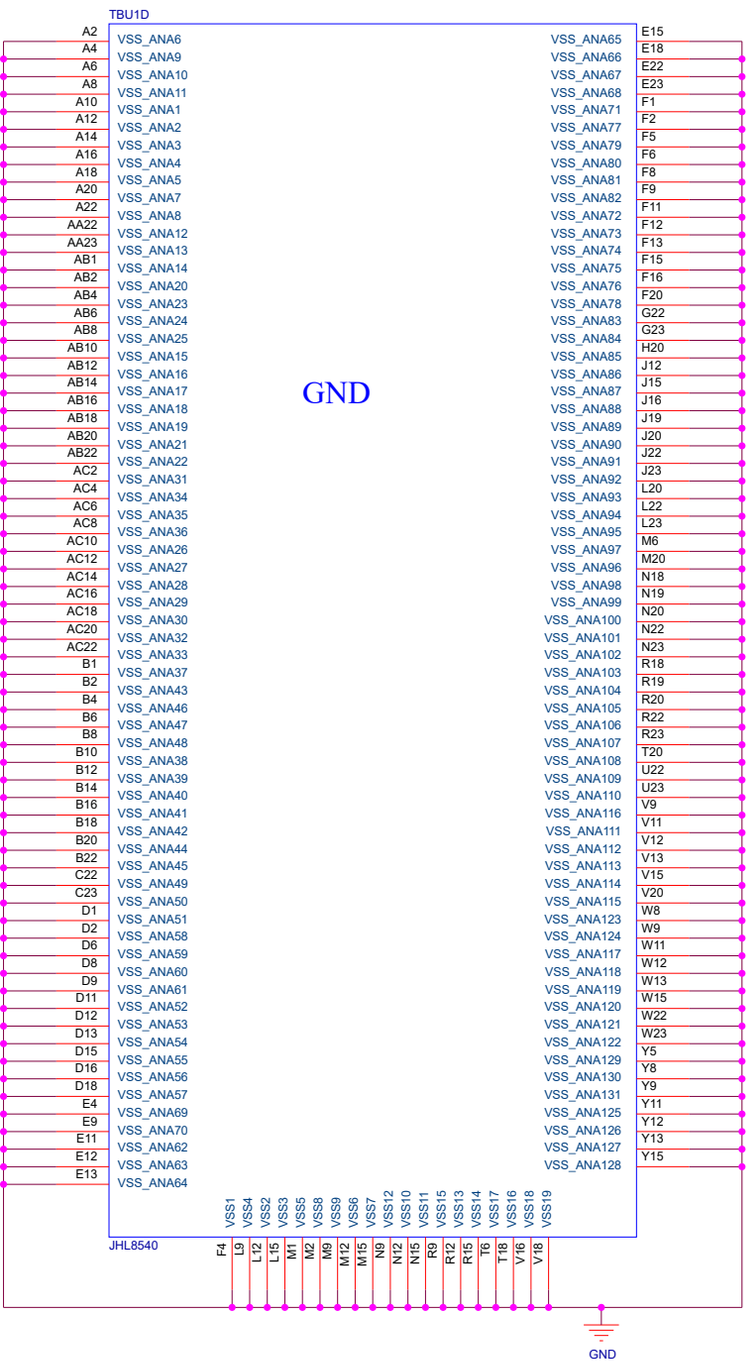
<Variant Name>

ASUSTek Computer Inc.	Title : MR_Power		
	Engineer: Brian_Hsieh		
Size: A3	Project Name: THUNDERBOLT MR DP		Rev: 0.5T
Date: Wednesday, July 06, 2022	Sheet 133	of 170	

B

0.5A

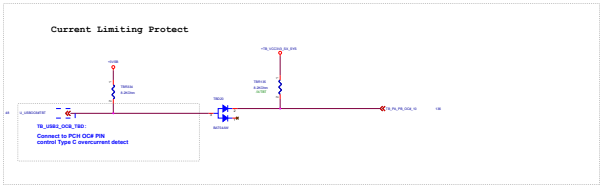
Maple Ridge DP - GND Symbol



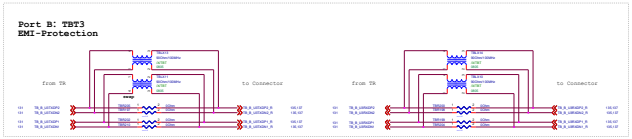
<Variant Name>

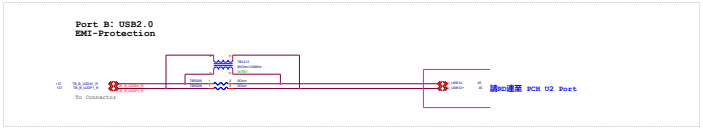
ASUSTek Computer Inc.	Title : TR_Ground	
	Engineer: Brian_Hsieh	
Size: A3	Project Name: THUNDERBOLT MR DP	Rev: 05A
Date: Wednesday, July 06, 2022	Sheet 134 of 170	

0.5A

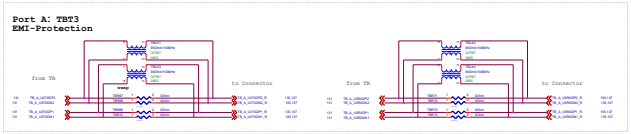


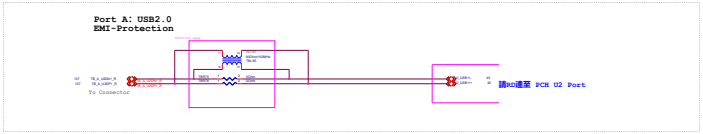
Port B : Type C Connector

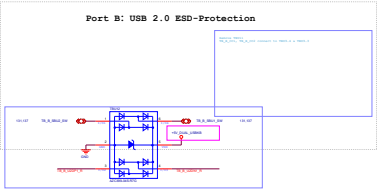


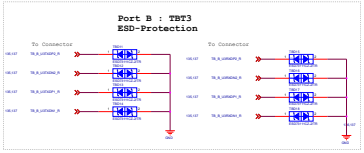


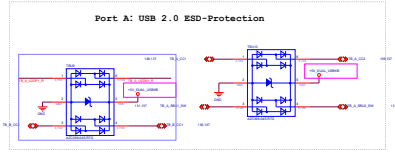
Port A : Type C Connector

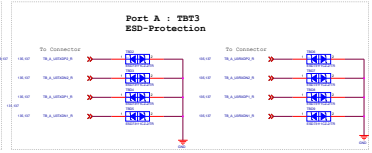




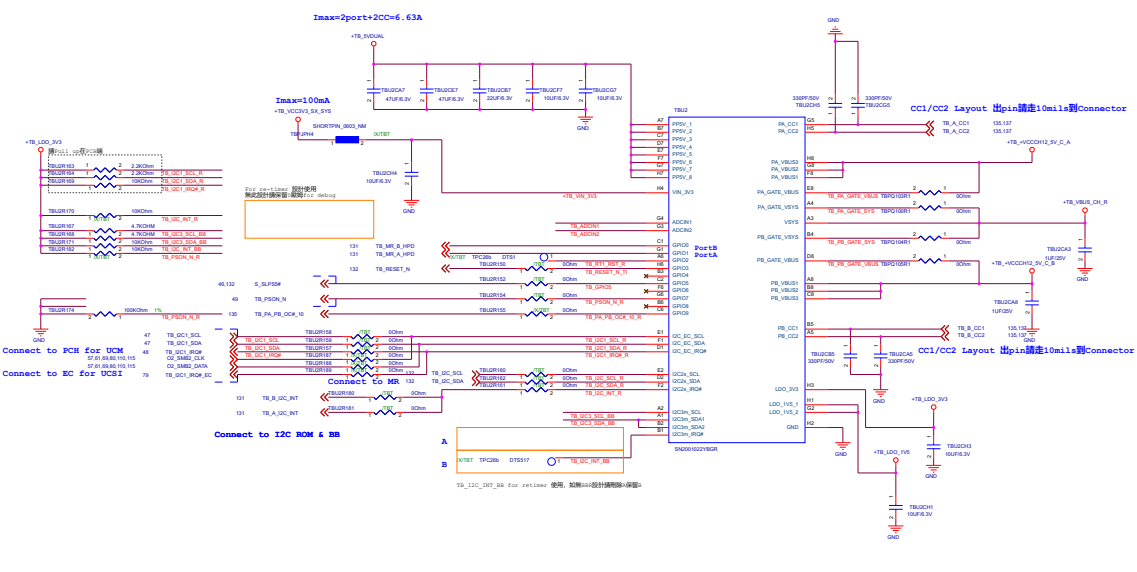








Title : EM6450
Engineer: Brian_Hsieh
THUNDERBOLT MB DP

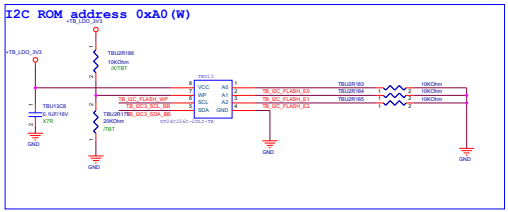


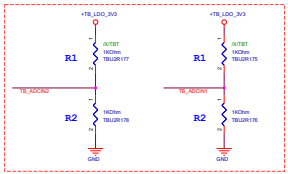
GPIO table

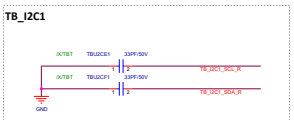
	TB_PSON_N
Z690	GPP_D14
Z790	GPP_F22
AM5	AGPIO32

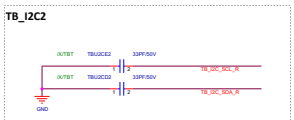
GPIO table

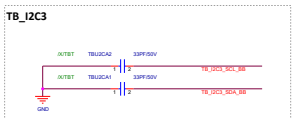
	TB_I2C1_SCL	TB_I2C1_SDA	TB_I2C1_IRQ#
Z690	GPP_C4	GPP_C3	GPP_K0
Z790	GPP_C4	GPP_C3	GPP_K0
AM5	EGPIO145	EGPIO146	AGPIO90



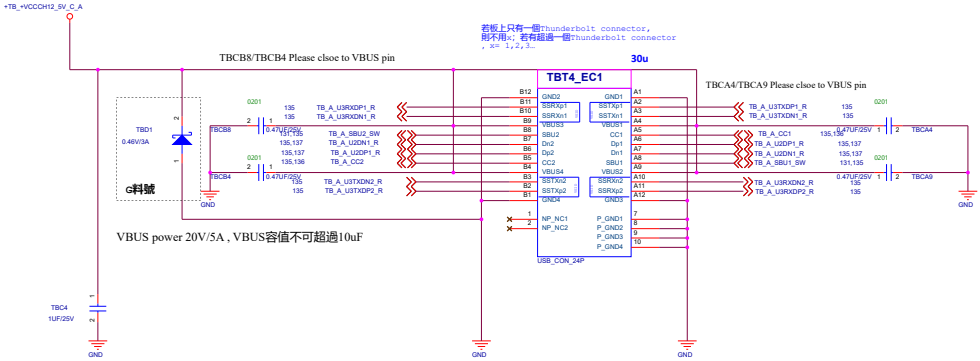




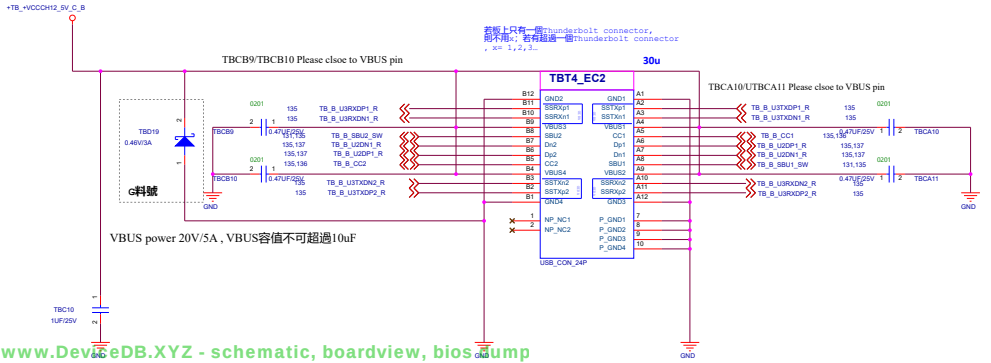




1 port Type C USB3.1 (CE team update)

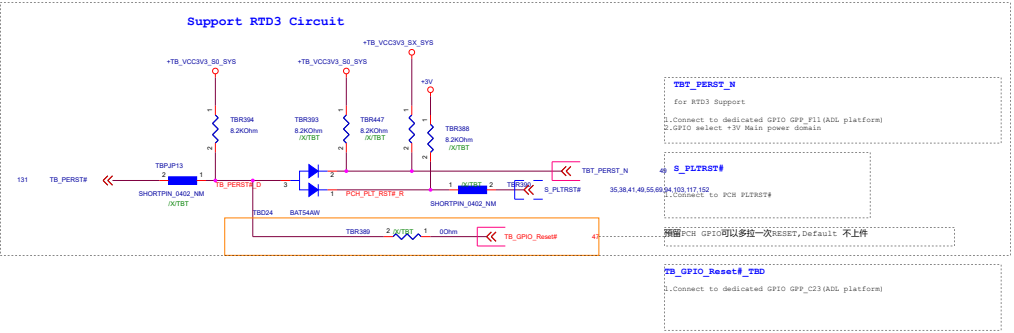


1 port Type C USB3.1 (CE team update)



<Variant Name>

ASUSTek Computer Inc.	Title :	TB_Connector	
	Engineer:	Brian_Hsieh	
Size: A3	Project Name: THUNDERBOLT MR DP		Rev: 0.5T
Date: Wednesday, July 06, 2022	Sheet 137 of 170		



GPIO table

	TB_GPIO_Reset#_TBD	TBT_PERST_N
Z590	GPP_F16	GPP_D8
Z690	GPP_C23	GPP_F11
Z790	GPP_C23	GPP_F11
B550	GPIO0	SIO_GP76
X570	AGPIO92	AGPIO11
AM5	GPIO4	AGPIO2

0.5U

<Variant Name>

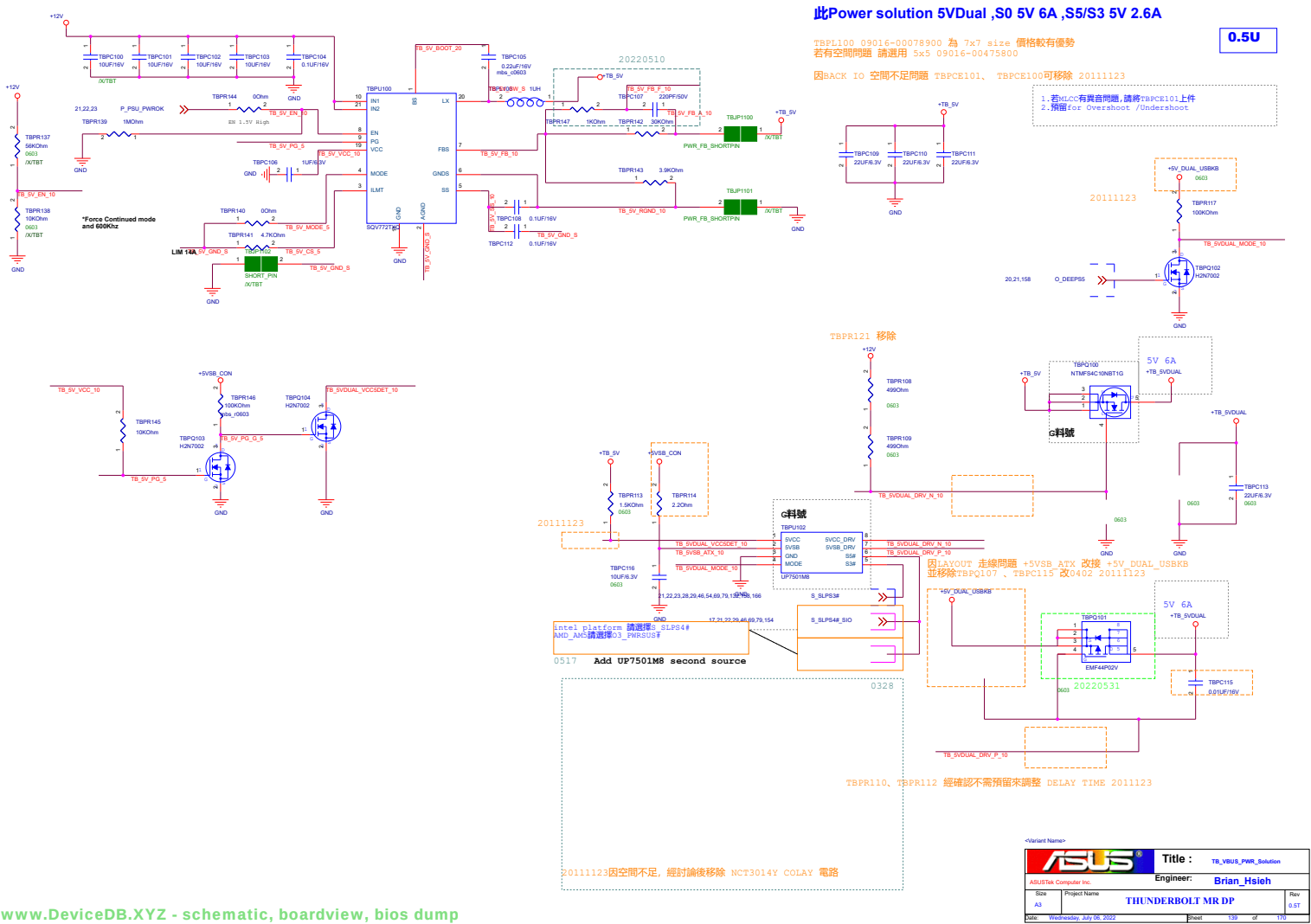
ASUSTeK Computer Inc.

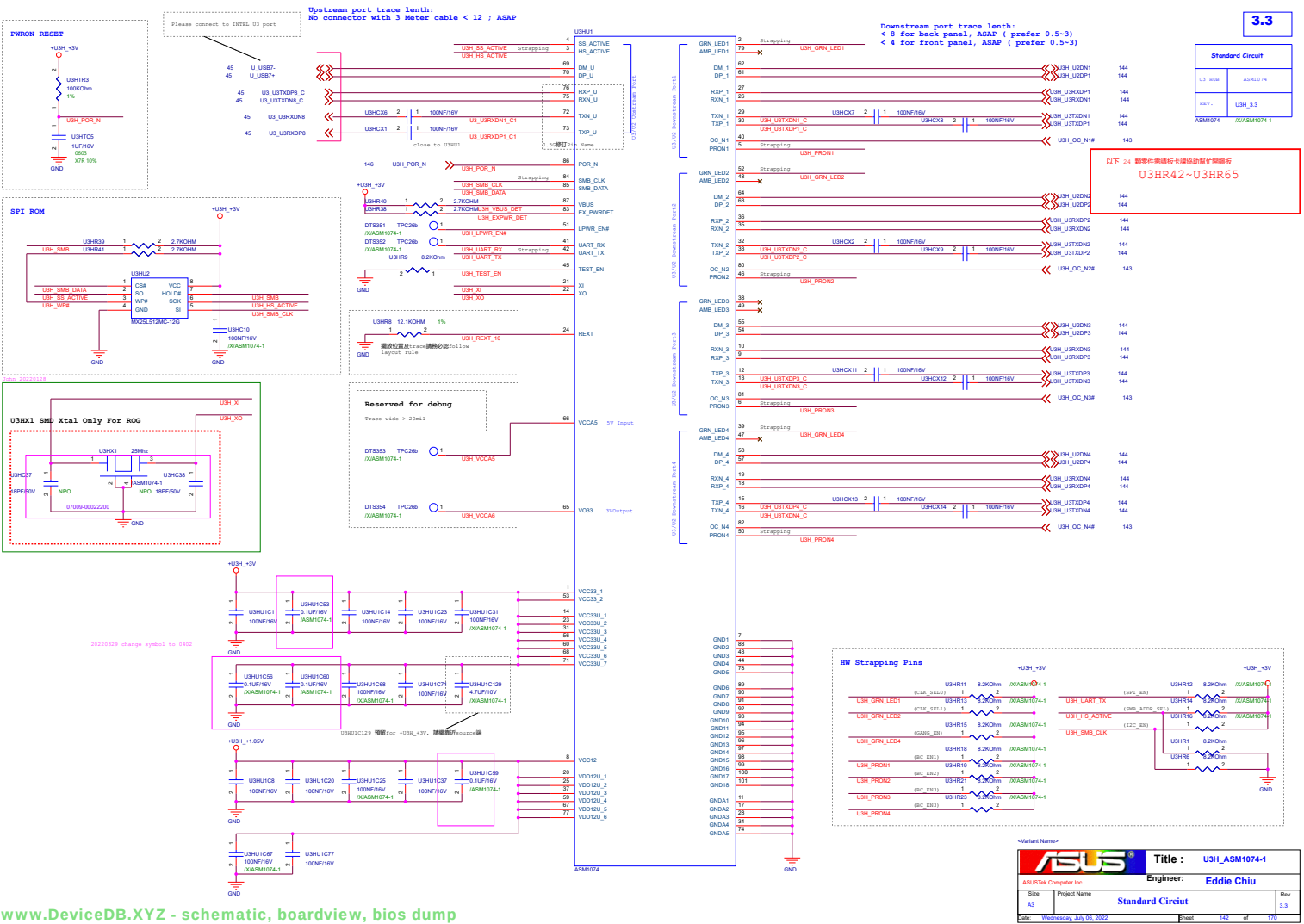
Title : RTD3 & EEPROM

Engineer: Brian_Hsieh

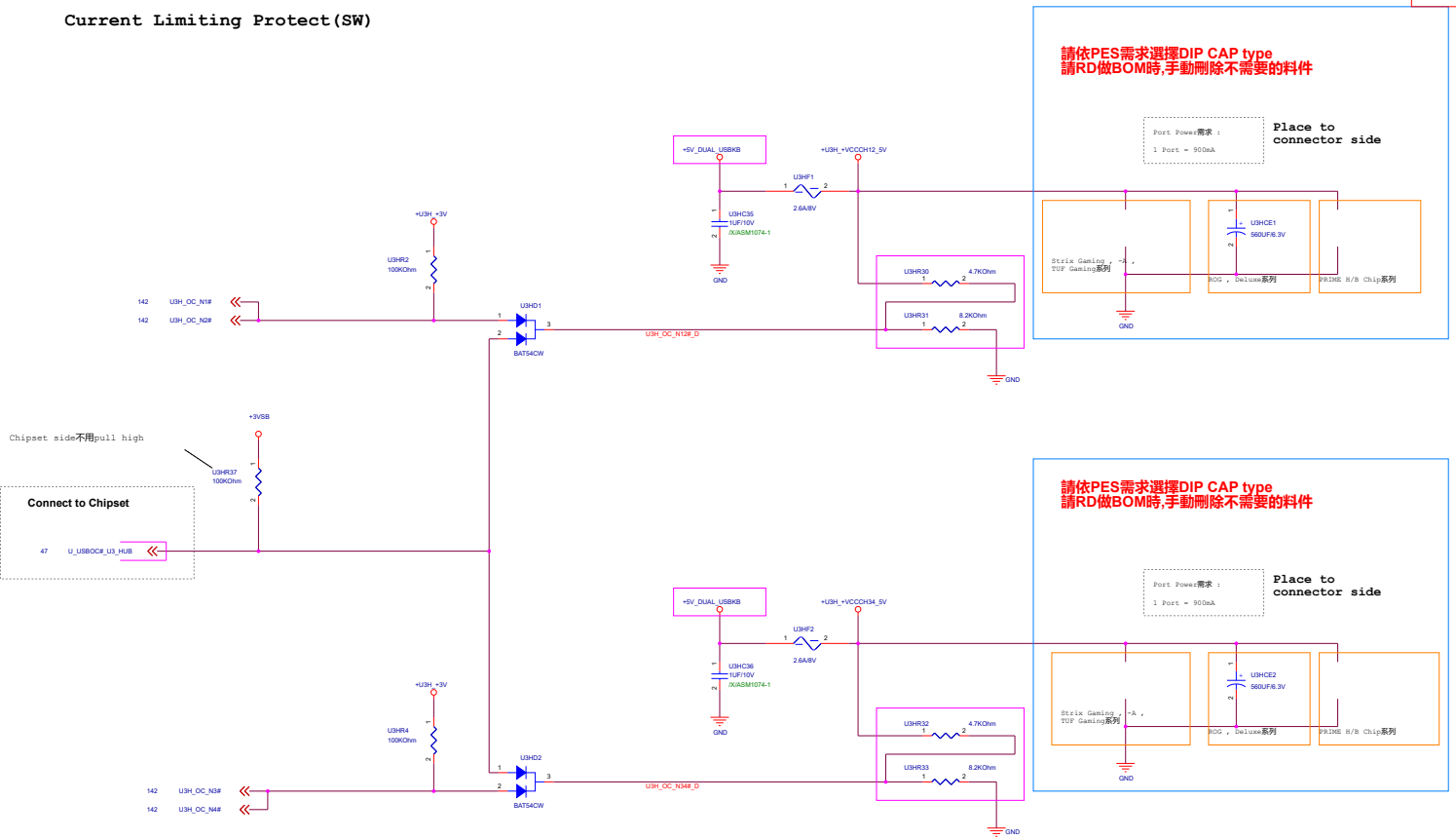
Size	Project Name	Rev
A3	THUNDERBOLT MR DP	0.5T

Date: Wednesday, July 06, 2022 Sheet 138 of 170




3.3
PWRON RESET
SPI ROM
U3HX1 SMD Xtal Only For ROG
Reserved for debug
HW Strapping Pins
Standard Circuit
Upstream port trace lenth:
No connector with 3 Meter cable < 12 ; ASAP
Downstream port trace lenth:
< 8 for back panel, ASAP (prefer 0.5~3)
< 4 for front panel, ASAP (prefer 0.5~3)
以下 24 顆零件需調板卡調協助幫忙開關板
U3HR42~U3HR65
U3H_ASM1074-1
Eddie Chiu
Standard Circuit
Wednesday, July 06, 2022
www.DeviceDB.XYZ - schematic, boardview, bios dump

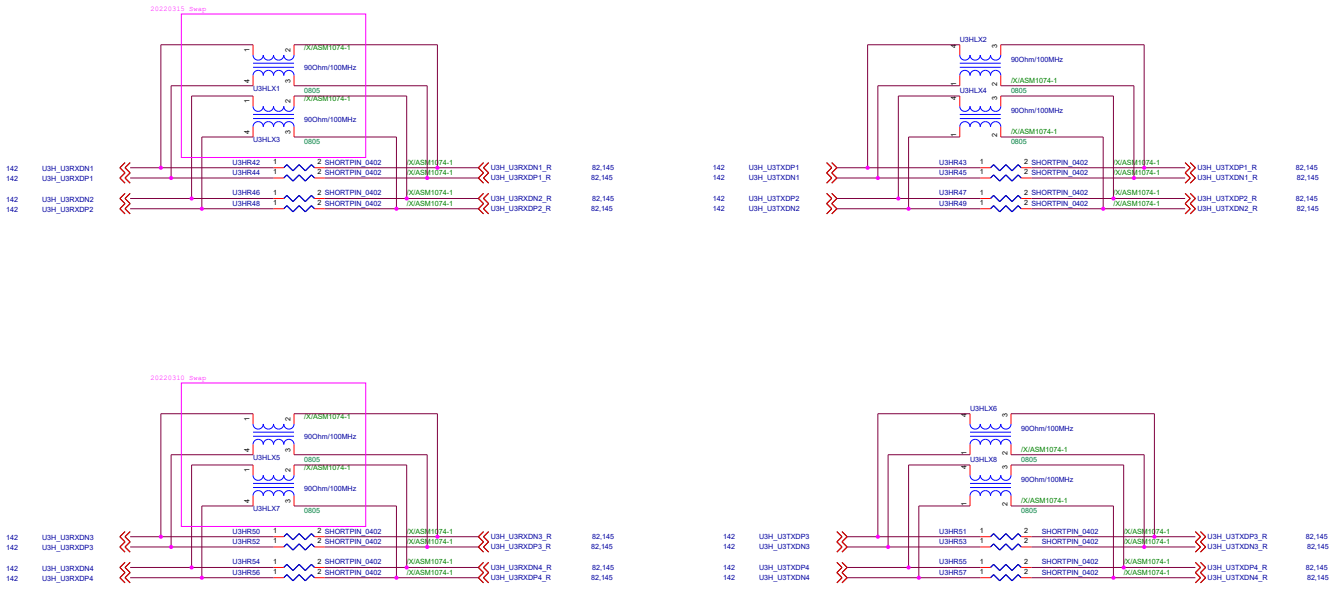
Current Limiting Protect(SW)



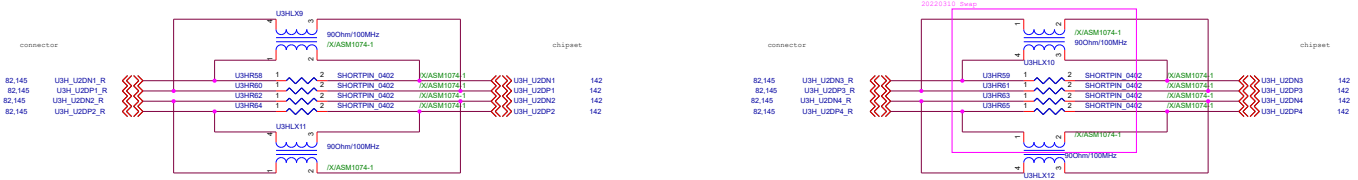
<Variant Name>

ASUSTek Computer Inc.	Title :	U3H_ASM1074-2	
	Engineer:	Eddie Chiu	
Size: A3	Project Name: Standard Circuit		Rev: 3.3
Date: Wednesday, July 06, 2022	Sheet 143 of 170		

USB3.0
EMI-Protection



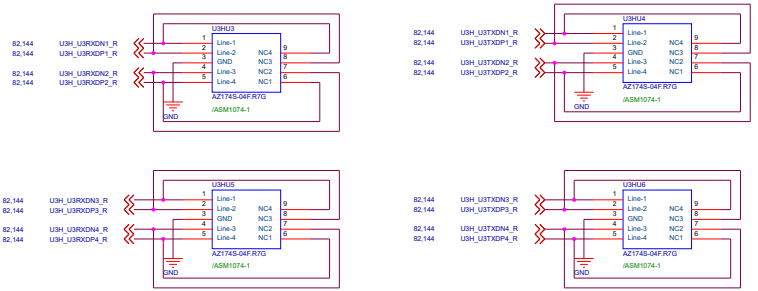
USB2.0
EMI-Protection



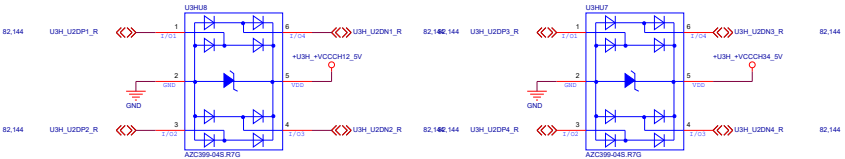
<Variant Name>

ASUSTek Computer Inc.	Title : U3H_ASM1074-4	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circiut	Rev: 3.3
Date: Wednesday, July 06, 2022	Sheet 144 of 170	

USB3.0 ESD-Protection



USB 2.0 ESD-Protection



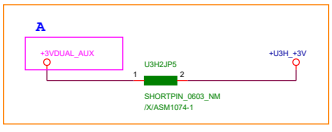
1.05V for ASM1074, 390mA@S0, little @S5

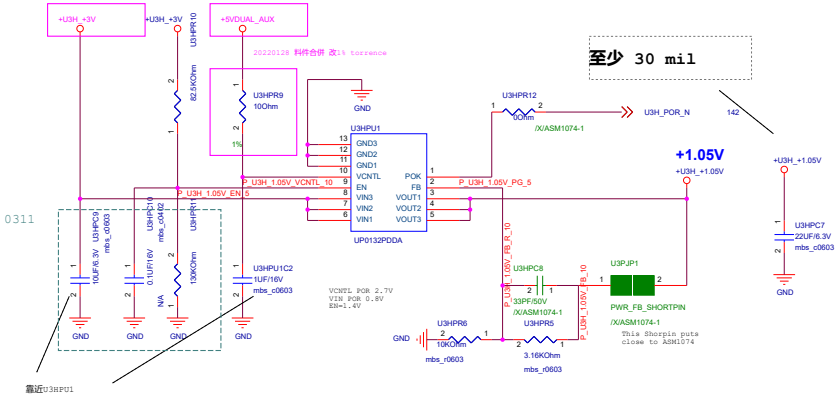
Date : 11/01/2018

請依Platform需求選擇橋框

A: 沒有cut-off power 線路

B: 有cut-off power 線路





7. Timing Diagram

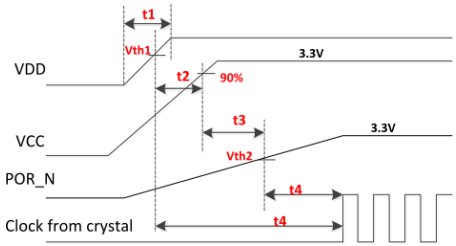


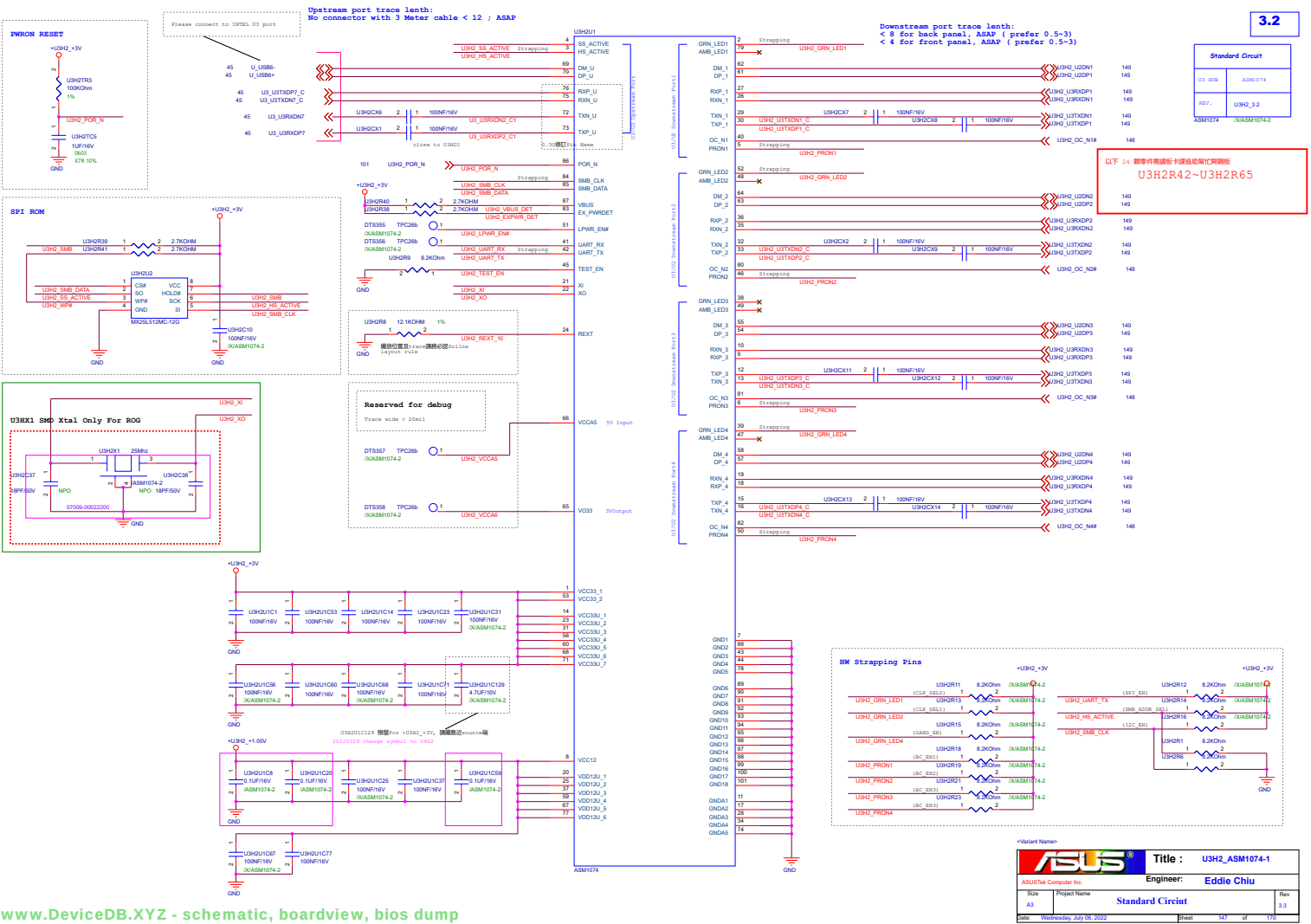
Figure 5: Power on Sequence for crystal mode

Power on Sequence Timing Specification for crystal mode

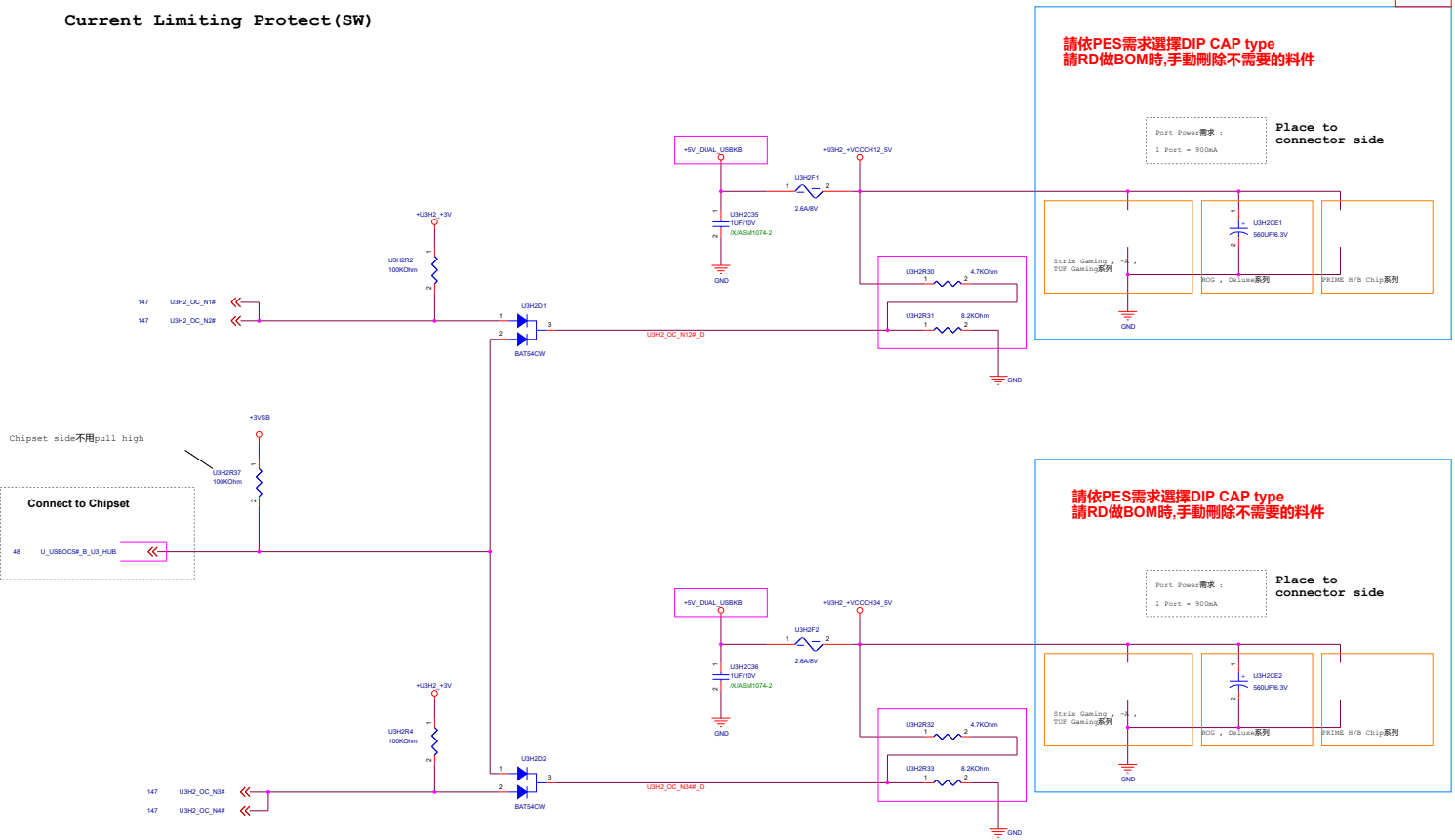
Symbols	Parameter	Min	Typ	Max	Unit	Remark
Vth1	The threshold of VDD internal power detect	0.49	0.7	0.92	V	
Vth2	The threshold of POR_N signal detect		0.5*VCC		V	
t1	Settling time of VDD stable power			6	ms	Measure from 10% to 90%
t2	The maximum delay timing of VCC power ready after the threshold of VDD	N/A		6	ms	Measure the timing between the point of Vth1 to 90% of VCC
t3	POR_N goes high after VCC power ready	0		N/A	ms	Measure the timing between the 90% of VCC to Vth2 of POR# (If without external POR_N circuit, this rule could be skipped)
t4	Maximum delay of stable clock available after the latest available point of Vth1 or Vth2			26	ms	Measure the timing between the point of Vth to stable clock available (self-powered mode)
				151	ms	Measure the timing between the point of Vth to stable clock available (bus-powered mode)

<Variant Name>

ASUSTek Computer Inc.	Title : U3H_ASM1074-6	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circiut	Rev: 3.3
Date: Wednesday, July 06, 2022	Sheet: 146 of 170	


3.2
PWRON RESET
SPI ROM
U3H1 SMD Xtal Only For ROG
Upstream port trace lenth:
No connector with 3 Meter cable < 12 ; ASAP
Downstream port trace lenth:
< 8 for back panel, ASAP (prefer 0.5~3)
< 4 for front panel, ASAP (prefer 0.5~3)
Please connect to INTEL U3 port
Reserved for debug
HW Strapping Pins
Standard Circuit
U3H2_ASM1074-1
Eddie Chiu
Standard Circuit
www.DeviceDB.XYZ - schematic, boardview, bios dump

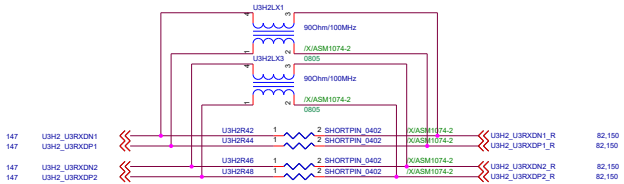
Current Limiting Protect(SW)

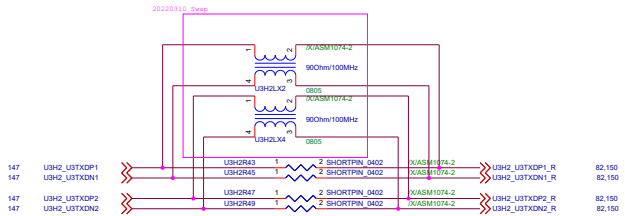


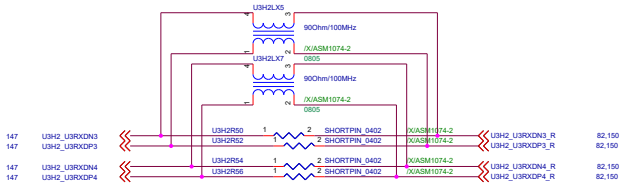
<Variant Name>

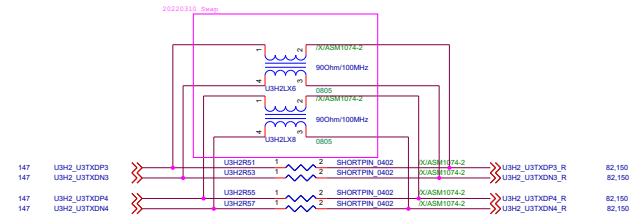
ASUSTek Computer Inc.	Title : U3H2_ASM1074-2	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circuit	Rev: 3.3
Date: Wednesday, July 06, 2022	Sheet 148 of 170	

USB3.0
EMI-Protection

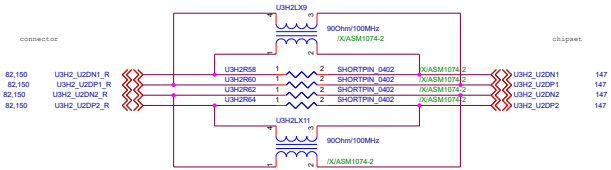


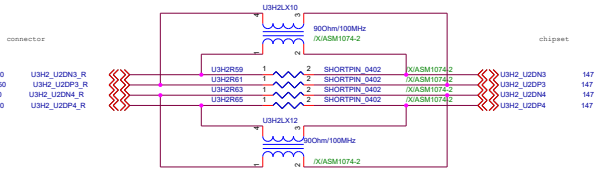




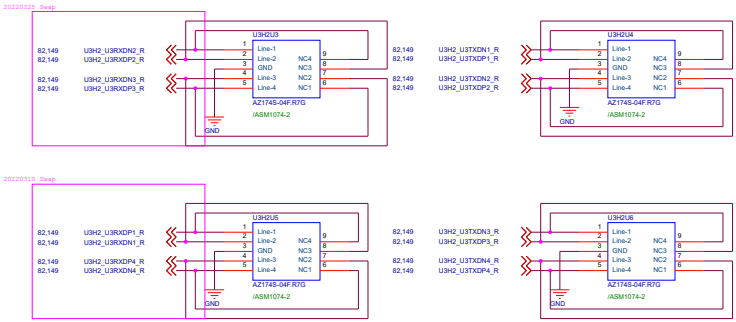


USB2.0
EMI-Protection

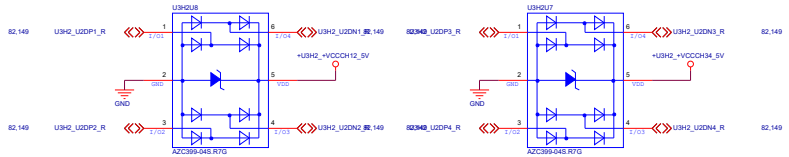




USB3.0
ESD-Protection



USB 2.0
ESD-Protection



<Variant Name>

ASUSTek Computer Inc.	Title : U3H2_ASM1074-4	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circiut	Rev: 3.3
Date: Wednesday, July 06, 2022	Sheet 150 of 170	

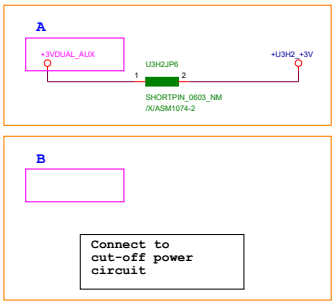
1.05V for ASM1074, 390mA@S0, little @S5

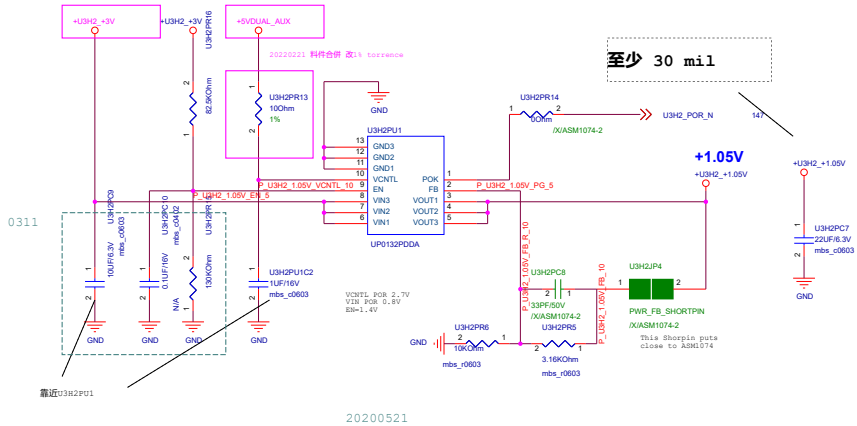
Date : 11/01/2018

請依Platform需求選擇橋框

A: 沒有cut-off power 線路

B: 有cut-off power 線路

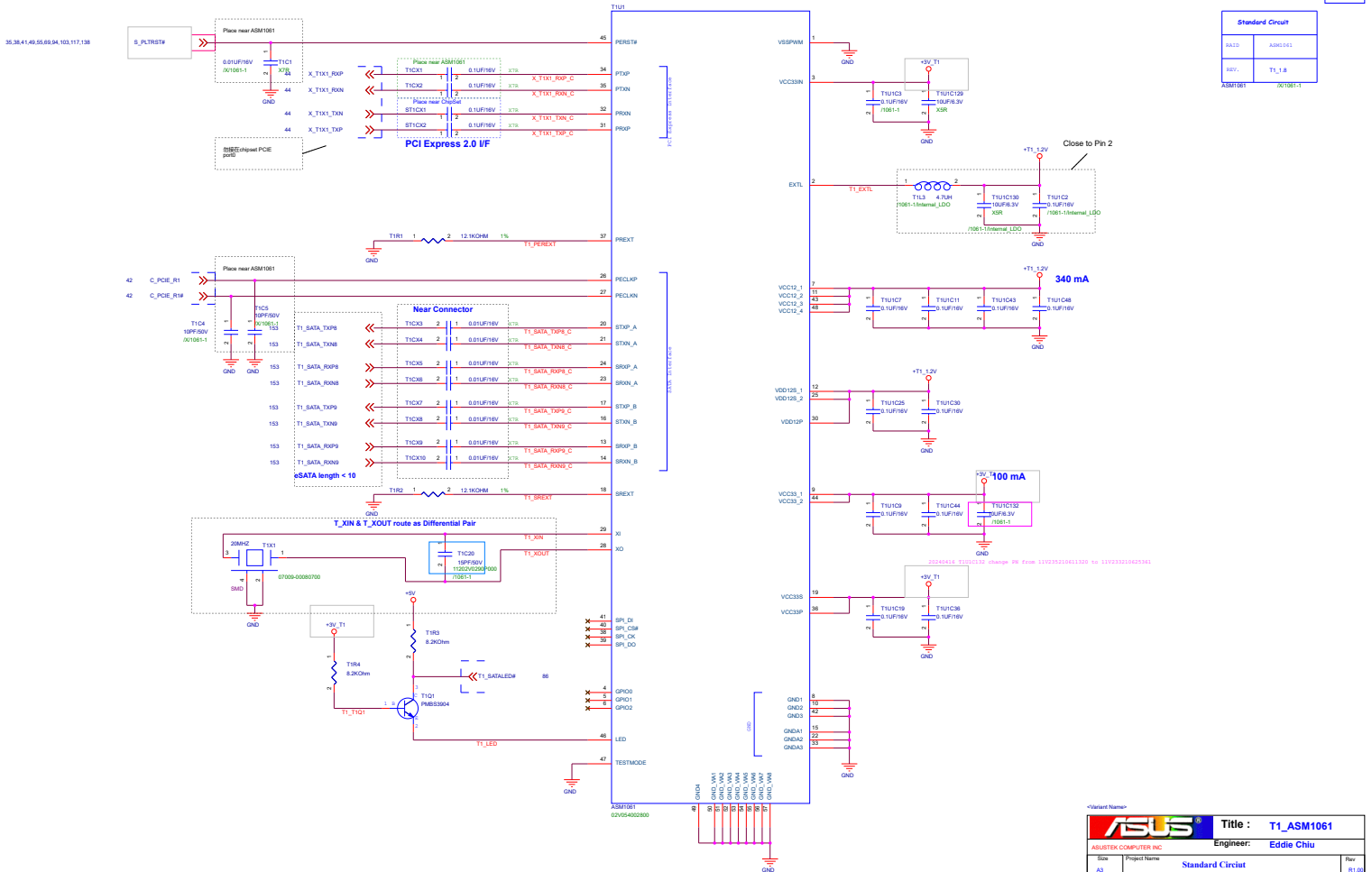




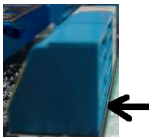
<Variant Name>

ASUSTek Computer Inc.	Title :	U3H2_ASM1074-5	
	Engineer:	Eddie Chiu	
Size: A3	Project Name: Standard Circiut		Rev: 3.3
Date: Wednesday, July 06, 2022	Sheet 151 of 170		

Standard Circuit	
BAID	ASM1061
REV.	T1_1.8
ASM1061	/X01061-1



	Connector 顏色
SATA6G_123456	LIGHT GRAY
	BROWN

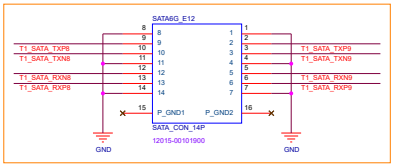


R/A Connector退放與板端切齊，
如上圖黑色箭頭處。

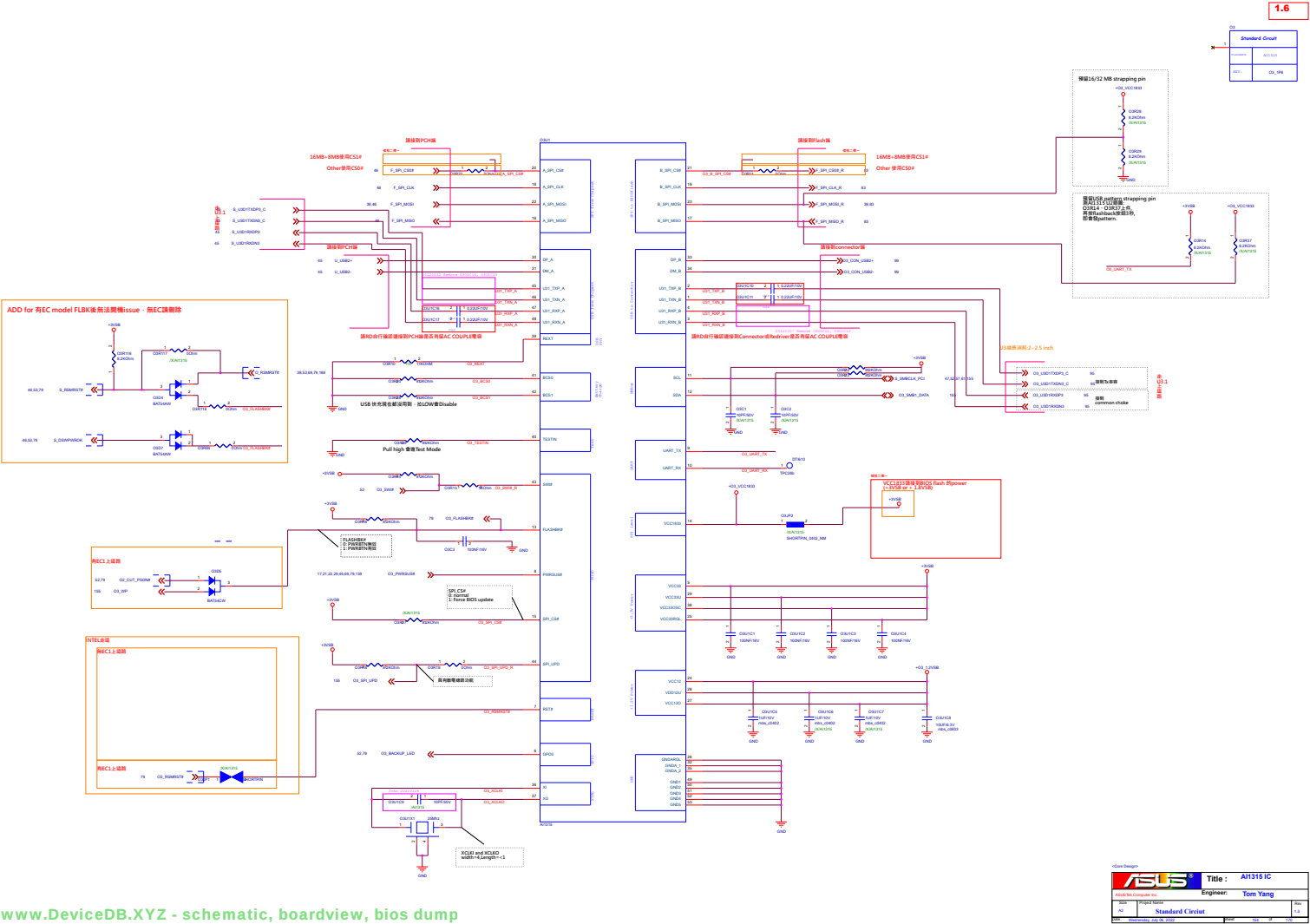
Near Connector (Void)

152	T1_SATA_TXP8	T1_SATA_TXP8
152	T1_SATA_TXN8	T1_SATA_TXN8
152	T1_SATA_RXN8	T1_SATA_RXN8
152	T1_SATA_RXP8	T1_SATA_RXP8
152	T1_SATA_TXP9	T1_SATA_TXP9
152	T1_SATA_TXN9	T1_SATA_TXN9
152	T1_SATA_RXN9	T1_SATA_RXN9
152	T1_SATA_RXP9	T1_SATA_RXP9

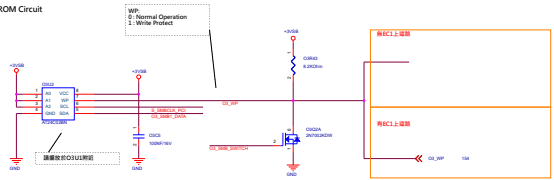
顏色: D-G



ASUSTek Computer Inc.	Title :	T1_ASM1061_SATA_Connector
	Engineer:	Aaron_Su
Size: A3	Project Name: Maximus XIII Extreme	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 153 of 170	

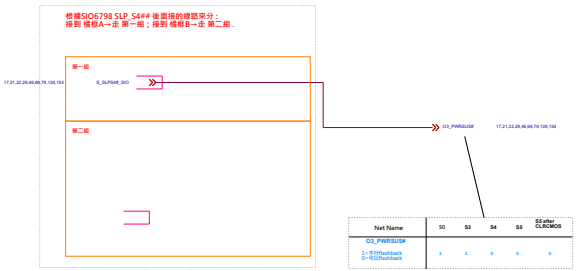

1.6
Standard Circuit
AI1315
03_YP4
預留16/32 MB strapping pin
+3V_VCC1833
預留USB pattern strapping pin
如AI1315 U2要做
Q3R14、Q3R37上拉
再做Pullback或接地
想看做pattern.
+3VSB
+3V_VCC1833
Q3_UART_TX
16MB+8MB使用CS1#
Other使用CS0#
請接到PCH端
請接到Flash端
請接到connector端
ADD for 宥EC model FLBK後無法開機issue，無EC請刪除
USB 供充電在睡眠期間，拉LOW會Disable
Pull high 會進Test Mode
SPI_CS#
2: Normal
3: Force BIOS update
其他除電總線功能
XCLKI and XCLKO
width=4,length=<1
INTEL走線
EC1上這顆
EC1上這顆
EC1上這顆
VCC1833連接到BIOS flash 的power
(+3VSB or + 1.8VSB)
3.5線長須在2~2.5 inch
接到Tx連接
接到Rx連接
接到common choke
U3.1
Q3
Standard Circuit
AI1315
03_YP4
Title :
AI1315 IC
Engineer:
Tom Yang
Standard Circuit
Wednesday, July 06, 2022
www.DeviceDB.XYZ - schematic, boardview, bios dump

EEPROM Circuit

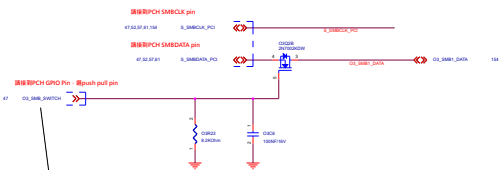


	GPO 控main Power，default GPI					
	G3	S5	S0	S0實現	S3	S4
WP Pin (Default: PH)	N/A	normal: H (WP) factory: L (normal) update BIOS: L (normal)	normal: H (WP) update EEPROM: GPOL (normal)	normal: H (WP) update EEPROM: GPOL (normal)	normal: H (WP)	normal: H (WP)
O3_FLASHBK#	N/A	normal: OD H factory: OD L update BIOS: OD L	normal: OD H Can't update BIOS	normal: OD H Can't update BIOS	normal: OD H Can't update BIOS	normal: OD H
O3_WP(default GPI)	N/A	default GPI	normal: GPI update EEPROM: GPOL(Push-Pull)	normal: GPI update EEPROM: GPOL通程中若遇到當機/鎖機，Main Power 掉了則GPIO 切回default GPI	default GPI	default GPI

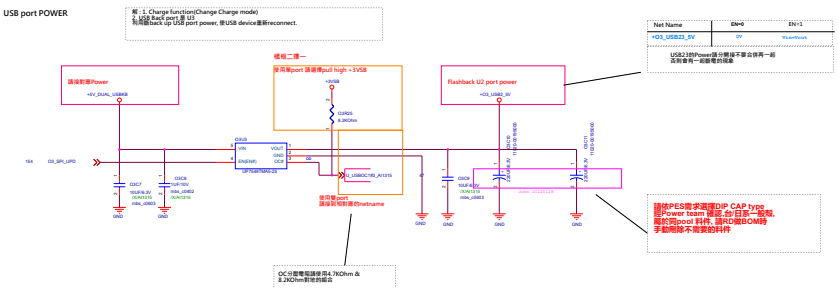
FlashBack Enable/disable Circiut

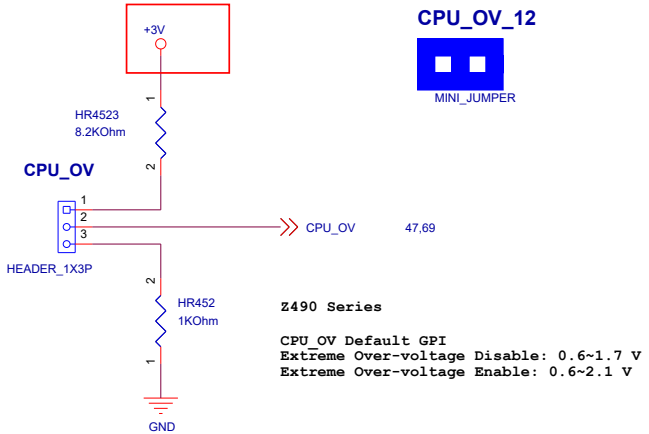


SMBUS Switch Circuit (for CheckSUM & update EEPROM)



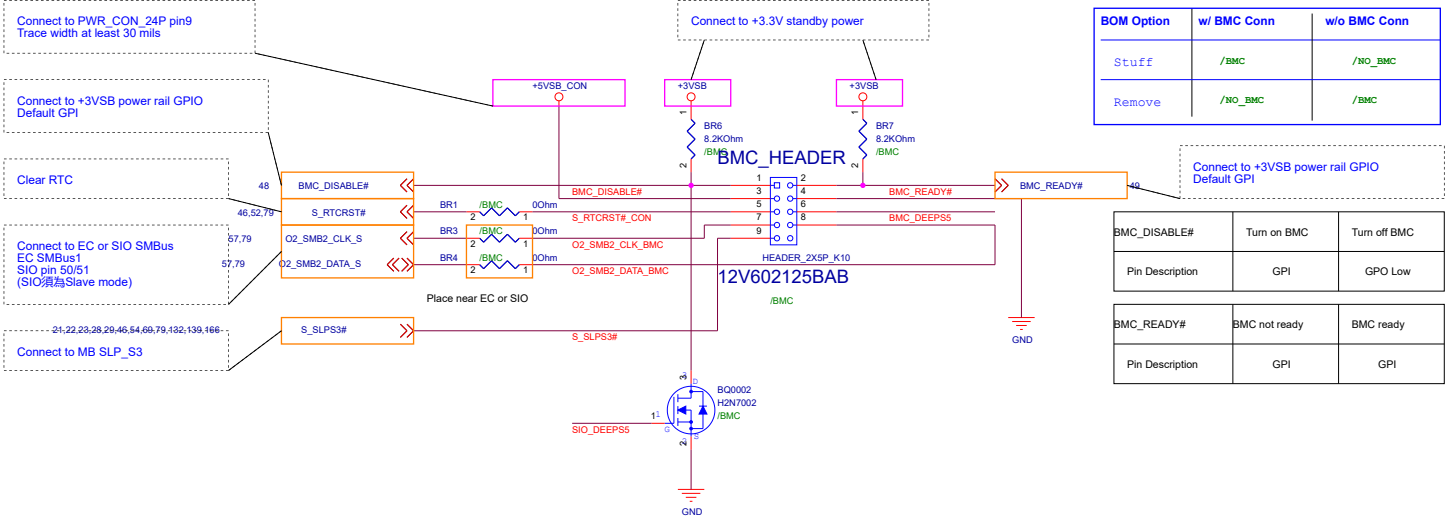
USB port POWER

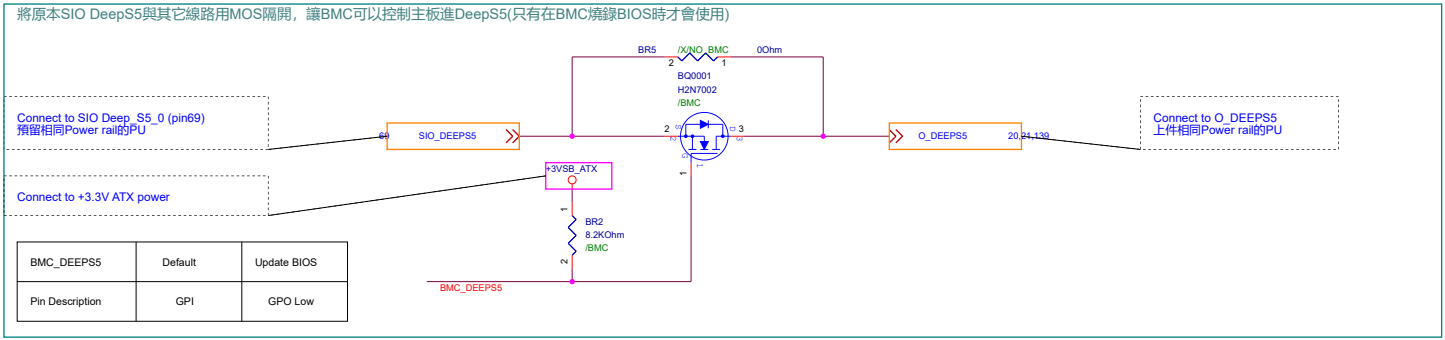




<Variant Name>

ASUSTek Computer Inc.	Title : AT32F403A	
	Engineer: Kelvin_Huang	
Size: A	Project Name: Innovation Circuit	Rev: 1.0
Date: Wednesday, July 06, 2022	Sheet 157 of 170	





<Core Design>

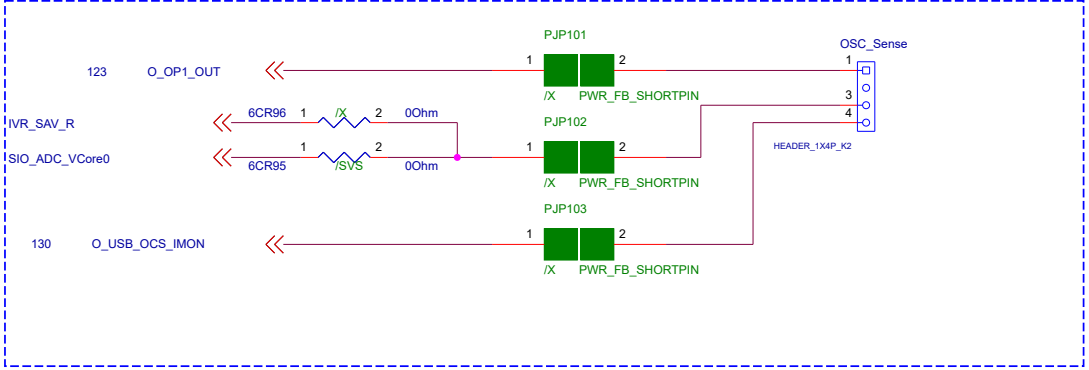
ASUSTeK COMPUTER INC

Title : BMC Header

Engineer: Mark Yu

Size	Project Name	Rev
A4	BMC_HEADER	1.0

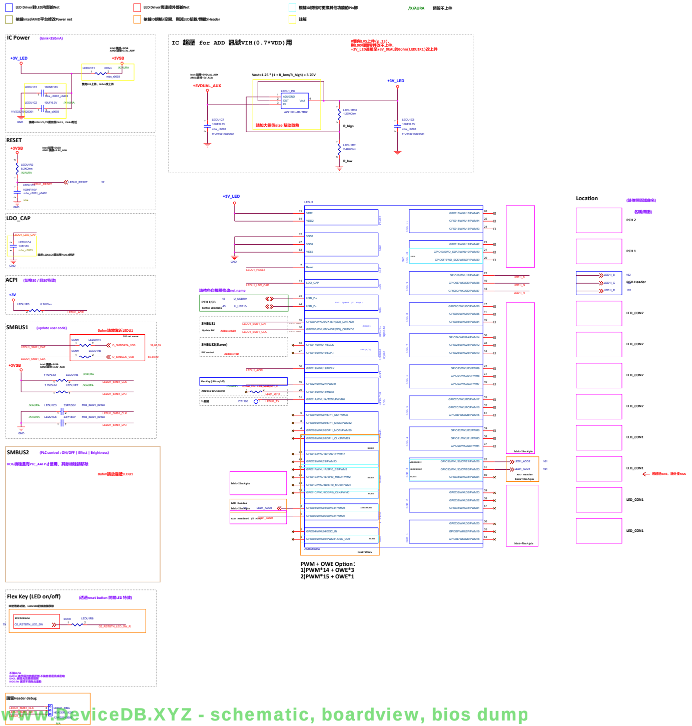
Date: Wednesday, July 06, 2022 Sheet 158 of 170



<Variant Name>

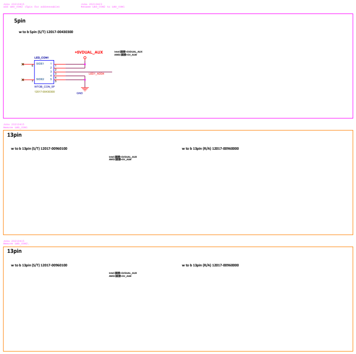
ASUSTek Computer Inc.	Title : AT32F403A	
	Engineer: Kelvin_Huang	
Size: A	Project Name: Innovation Circuit	Rev: 1.0
Date: Wednesday, July 06, 2022	Sheet 159 of 170	

Ver 1.8



(區域名稱選項)

ID 91 : Unit00 Location
0x00: CPU
0x01: VRM
0x02: center
0x03: PCH
0x04: Audio
0x05: Back IO
0x06: RGB strip-1
0x07: RGB strip-2
0x08: Back Plate
0x09: Edge-Left
0x0A: Memory
0x0B: PCIE
0x0C: Area
0x0D: PCB Surround
0x0E: DIMM.2
0x0F: Light Bar
0x10: ODD
0x11: RGB_HEADER
0x12: M.2
0x13: RGB_HEADER 1 2
0x14: RGB_HEADER 3 4
0x15: Start/retry Button
0x16: Edge-Right & RGB Strip
0x17: PCH LED & Edge-right & RGB Strip
0x18: Back IO low + START & RESET button
0x19: PCIEX1 + SATA12
0x1A: PCIEX16_1 + SATA34
0x1B: PCIEX16_2 + SATA56
0x1C: PCIEX1 + Center
0x1D: Audio Box
0x1E: IO+BACK LED ZONE
0x1F: NB+BACK LED ZONE
0x20: Back IO top
0x21: ROG logo
0x22: PCIEX16_1
0x23: PCIEX16_2
0x24: EXT_RGB_Header
0x25: ADD_Header
0x26: PCH+BACK LED ZONE
0x27: PCH TOP
0x28: Nameplate
0x29: PCH LOGO
0x2A: SATA
0x2B: WB_ADD



Cable list(請與機構確認cable長度需求):

若需求不符，請找CE Team協助

5Pin

14011-00770100 96mm 黑色塑膠HD
14011-00770200 200mm 黑色塑膠HD
14011-00770300 160mm 醋酸膠布
14011-00770500 50mm 醋酸膠布
14011-00770400 130mm 醋酸膠布
14011-00770600 130mm 熱縮套管
14011-00770700 70mm 熱縮套管

8Pin

14011-00700100 115mm 醋酸膠布 [背板connector]
14011-00700200 70mm 醋酸膠布
14011-00700300 110mm 醋酸膠布
14011-00701300 125mm 自帶latch
14011-00701200 115mm 自帶latch

13Pin

14011-02620200 50mm 醋酸膠布
14011-02620100 370mm 醋酸膠布
14011-02620300 60mm 醋酸膠布
14011-02620000 130mm 醋酸膠布

<Variant Name>

ASUSTek Computer Inc.	Title : AURA50(64Pin)		
	Engineer: Kaizer_Luo		
Size: Custom	Project Name: LED Standard Circiut		Rev: 1.8
Date: Wednesday, July 06, 2022	Sheet 160 of 170		

Addressable Header

Ver 1.8

LED Driver對LED內部的Net

LED Driver需連接外部的Net

根據ID規格可更換其他功能的Pin腳

/X/AURA 預設不上件

依據Intel/AMD平台修改Power net

依據ID規格/空間，刪減LED組數/顆數/Header

註解

Addressable Header（支援2組以上），不要的線路請刪除

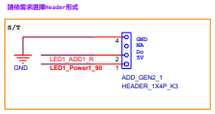
第1組

ADD LED Power 1

ADD LED Data 1

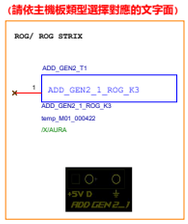
Addreesable LED Header 1

請依需求選擇Header形式



ADD_HEADER1 反白文字面

（請依主機板類型選擇對應的文字面）



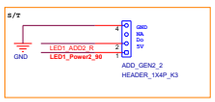
第2組

ADD LED Power 2

ADD LED Data 2

Addreesable LED Header 2

請依需求選擇Header形式



ADD_HEADER2 反白文字面

（請依主機板類型選擇對應的文字面）

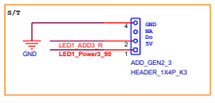
第3組

ADD LED Power 3

ADD LED Data 3

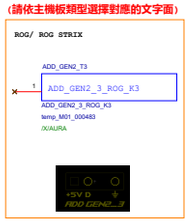
Addreesable LED Header 3

請依需求選擇Header形式



ADD_HEADER3 反白文字面

（請依主機板類型選擇對應的文字面）



<Variant Name>

ASUSTek Computer Inc.

Title : ADD_Header

Engineer: Kaizer_Luo

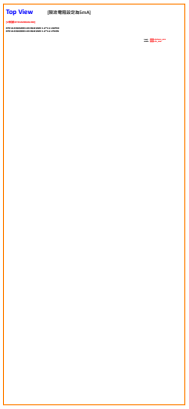
Size: Custom | Project Name: LED Standard Circiut | Rev: 1.8

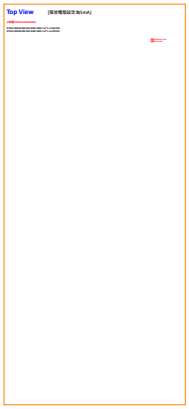
Date: Wednesday, July 06, 2022 | Sheet 161 of 170

PWM_Port_D

Ver 1.0

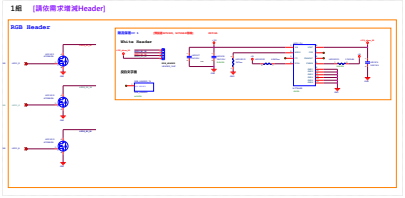
1.On board RGB





2.RGB Header

1板 [請依需求增減Header]



White Header [5V4]

3.LED Card

Port A

背板, 前板各使用一組Gen2x2
or 兩組Gen2x2共用PD controller

USB 3.2 Re-Driver PI3EQX2024 Circuit

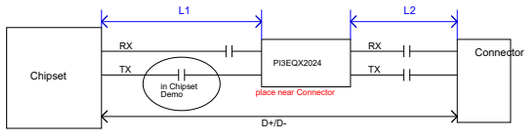
A. Choose type of AC CAP between CPU/Chipset & Re-Driver

B. Modify Input USB 3.2 TX/RX Signal Net Name by Project

C. Modify Output USB 3.2 TX/RX Signal Net Name by Project

D. Modify EQ/FG Pins' pull high/pull down BOM by layout

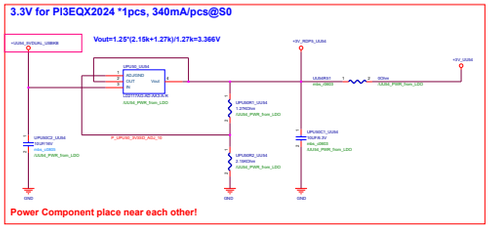
EQ/FG Setting Table for USB 3.2 Port	L2 < 2.5"			
	TX EQ	TX FG	RX EQ	RX FG
L1 < 7"	R	R	R	0
7" <= L1 <= 9"	F	R	R	F
9" < L1 < 10"	1	R	R	1

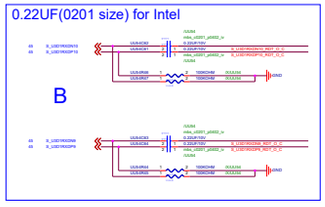


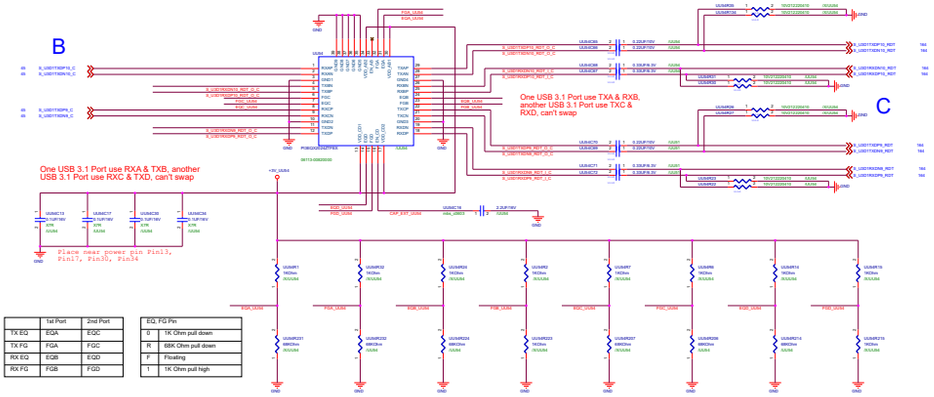
Net	Impedance/Width	Space	Length
TX/RX L1	follow USB 3.2 Controller Rule	30 mils	< 10", prefer 5" - 9"
TX/RX L2		30 mils	< 2.5", prefer 0.5" - 1.5"
+3V_RDP5	>= PI3EQX2024 IC Count *20 mils		
Other Power Net	>= 20 mils		

E. Choose PI3EQX2024 Power Solution by Project

BOM	PI3EQX2024 Power generated by LDO	PI3EQX2024 Power From WIFI	PI3EQX2024 Power From LAN1	PI3EQX2024 Power From LAN2
/UU51_PWR_from_LDO	mount	unmount	unmount	unmount
/UU51_PWR_from_WIFI	unmount	mount	unmount	unmount
/UU51_PWR_from_LAN1	unmount	unmount	mount	unmount
/UU51_PWR_from_LAN2	unmount	unmount	unmount	mount







	1st Port	2nd Port
TX EQ	EQA	EQC
TX FG	FGA	FGC
RX EQ	EQB	EQD
RX FG	FGB	FGD

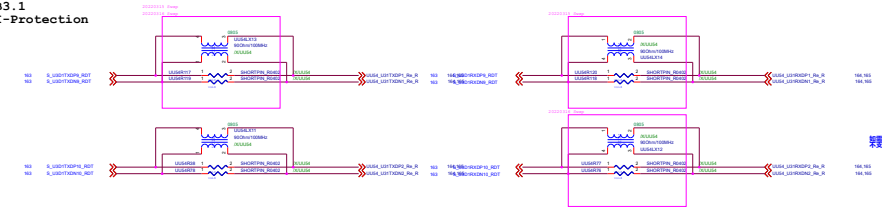
EQ, FG Pin	
0	1K Ohm pull down
R	68K Ohm pull down
F	Floating
1	1K Ohm pull high

Port B

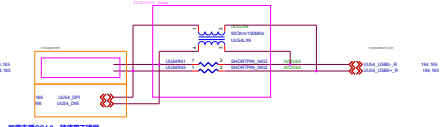
Title :	U32 REDRIVER-1
Engineer:	Murphy_Lee
Custom	Standard Circiut
Date: Wednesday, July 06, 2022	Sheet 102 of 116

Port A

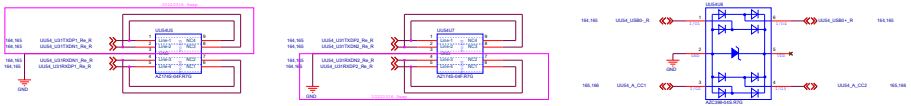
USB3.1 EMI-Protection



USB2.0 EMI-Protection



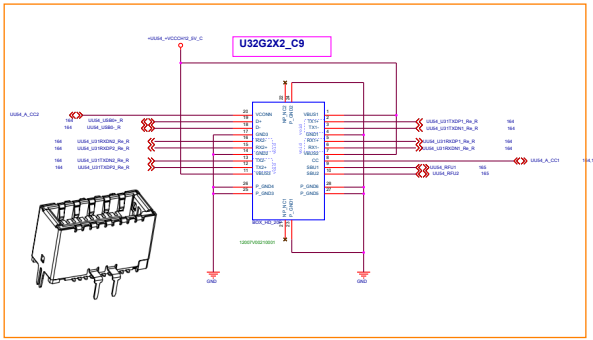
USB3.1/USB 2.0 ESD-Protection

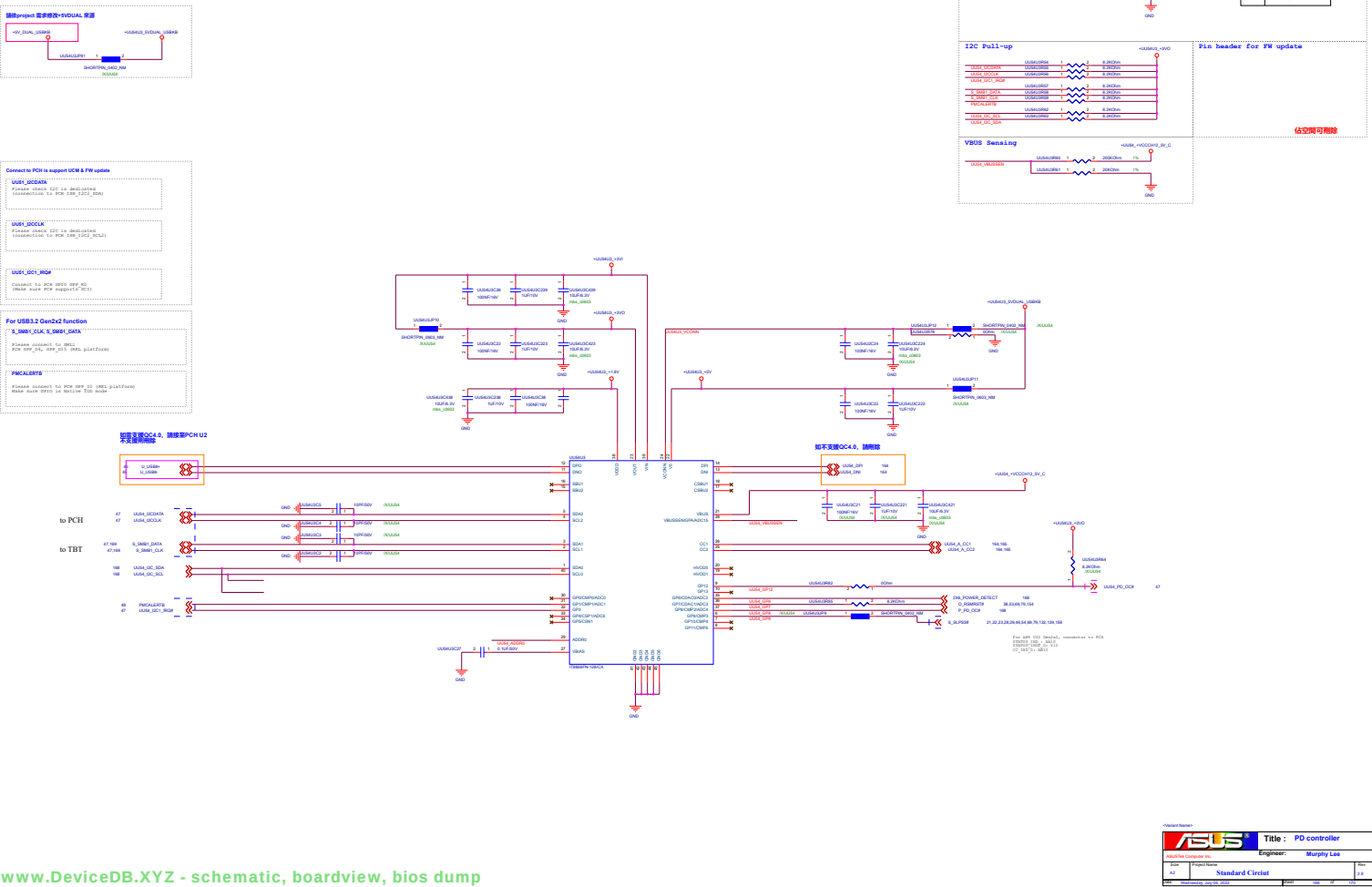


Title :	ESD_EMI	
Engineer:	Murphy Lee	
Size: A2	Project Name: Standard Circiut	Rev: 2.8
Date: Wednesday, July 06, 2022	Sheet 164 of 190	

Port A

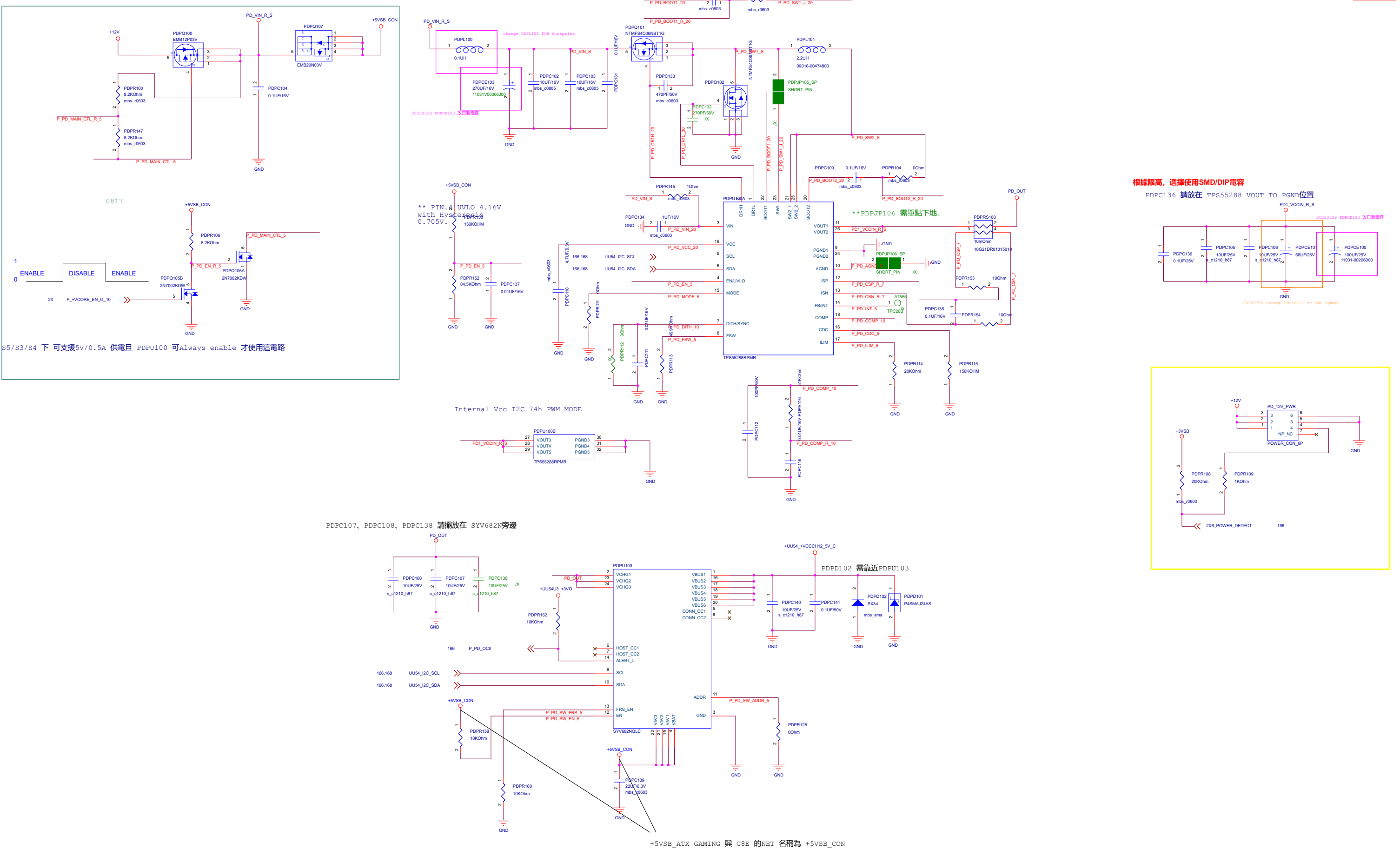
164,166 UL64_A_CC2



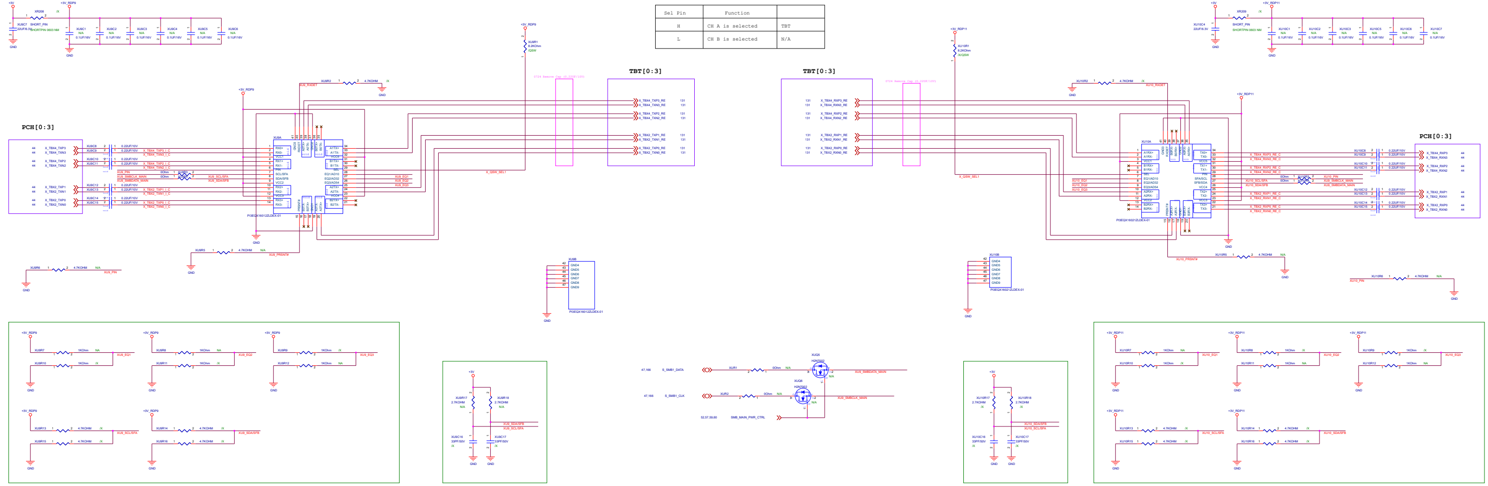


ASUSTeK Computer Inc.	Title : PD controller		
	Engineer: Murphy Lee		
Size A2	Project Name Standard Circuit		Rev 2.8
Date Wednesday, July 06, 2022	Sheet 168 of 194		

如不使用PD 60W，請刪除此頁



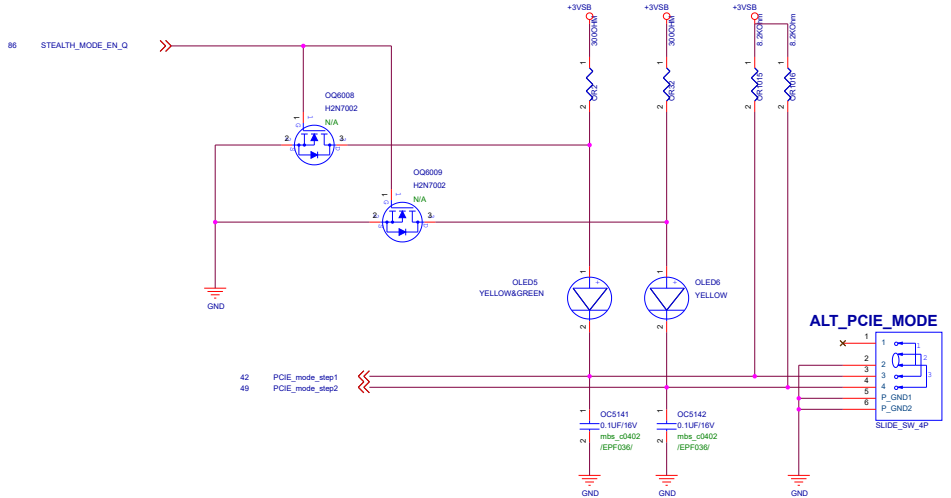
Title :	+12V/+12VSB
ASUSTeK COMPUTER INC. NB4	Engineer: Murphy Lee
Size A2	Project Name: Standard Circiut	Rev 2.8
Date: Wednesday, July 06, 2022	Sheet 168 of 170



Sel Pin	Function	
H	CH A is selected	TBT
L	CH B is selected	N/A

<Variant Name>

ASUSTek Computer Inc.	Title : PCIE GEN4 Re-Driver	
	Engineer:	
Size: Custom	Project Name: Maximus Z790 Hero	Rev: R1.00
Date: Wednesday, July 06, 2022	Sheet 169 of 170	



Switch	PCIE_mode	status
1-2	Disable	STEP1: H STEP2: H
2-3	1st step	STEP1: L STEP2: H
2-4	2nd step	STEP1: H STEP2: L

<Variant Name>

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
A3		R1.02A

Date: Wednesday, July 06, 2022 Sheet 170 of 170