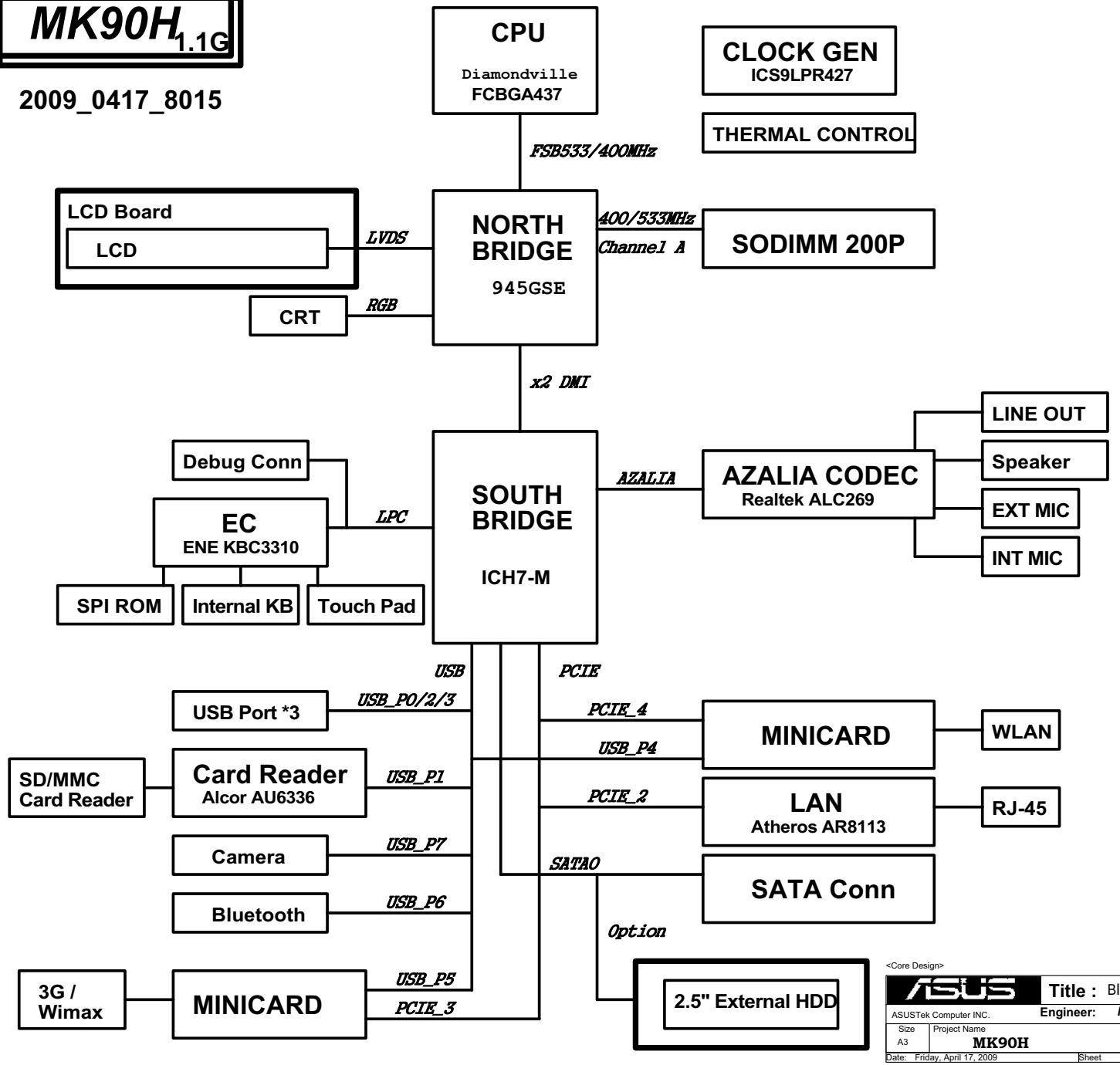
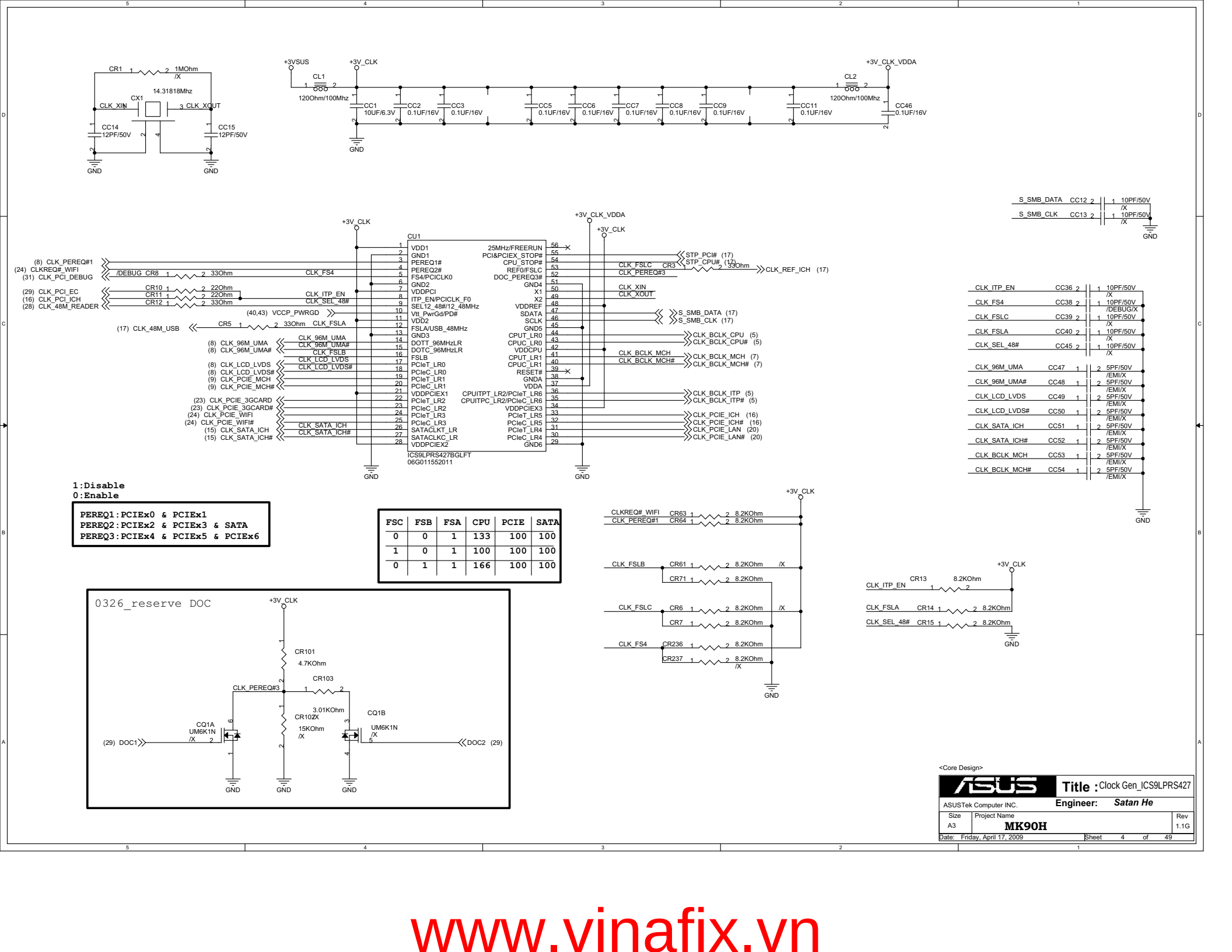
MK90H 1.1G

2009_0417_8015



<Core Design>

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Regin Chiang	
Size A3	Project Name MK90H	Rev 1.1G
Date: Friday, April 17, 2009	Sheet 1 of 49	



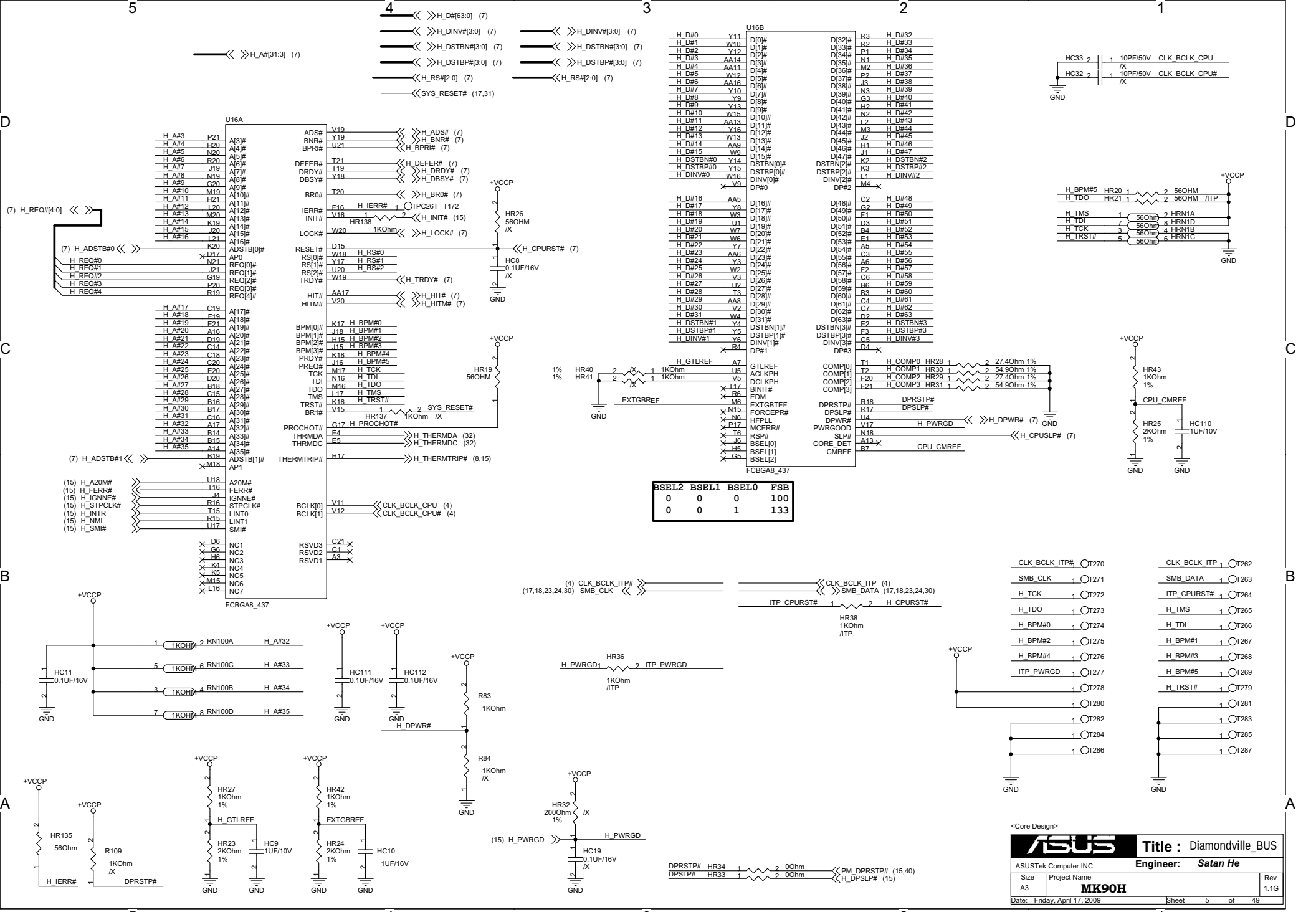
1:Disable
0:Enable

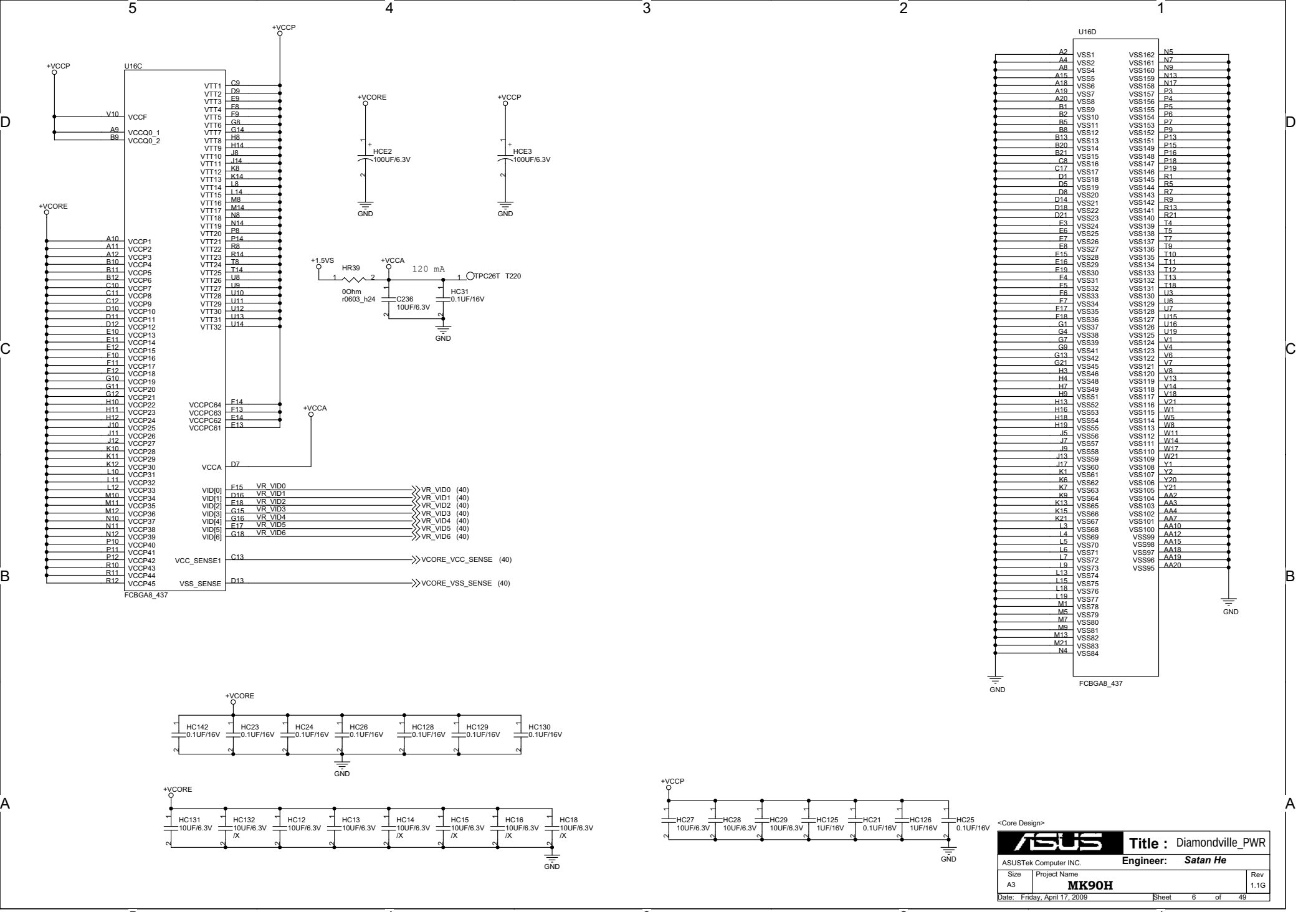
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100
0	1	1	166	100	100

<Core Design>

ASUSTek Computer INC.	Title : Clock Gen_ICS9LPRS427	
	Engineer: Satan He	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 4 of 49	

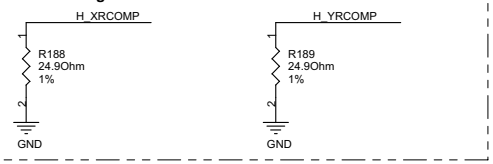




Power:
+VCCP

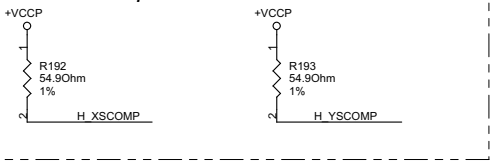
RCOMP

For Calibrating the FSB I/O Buffer



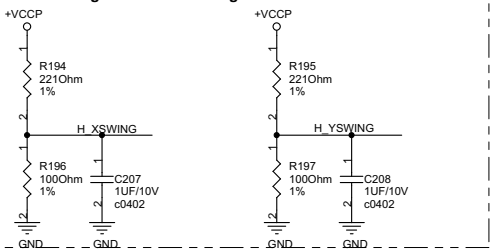
SCOMP

For Slew Rate Compenssation on the FSB

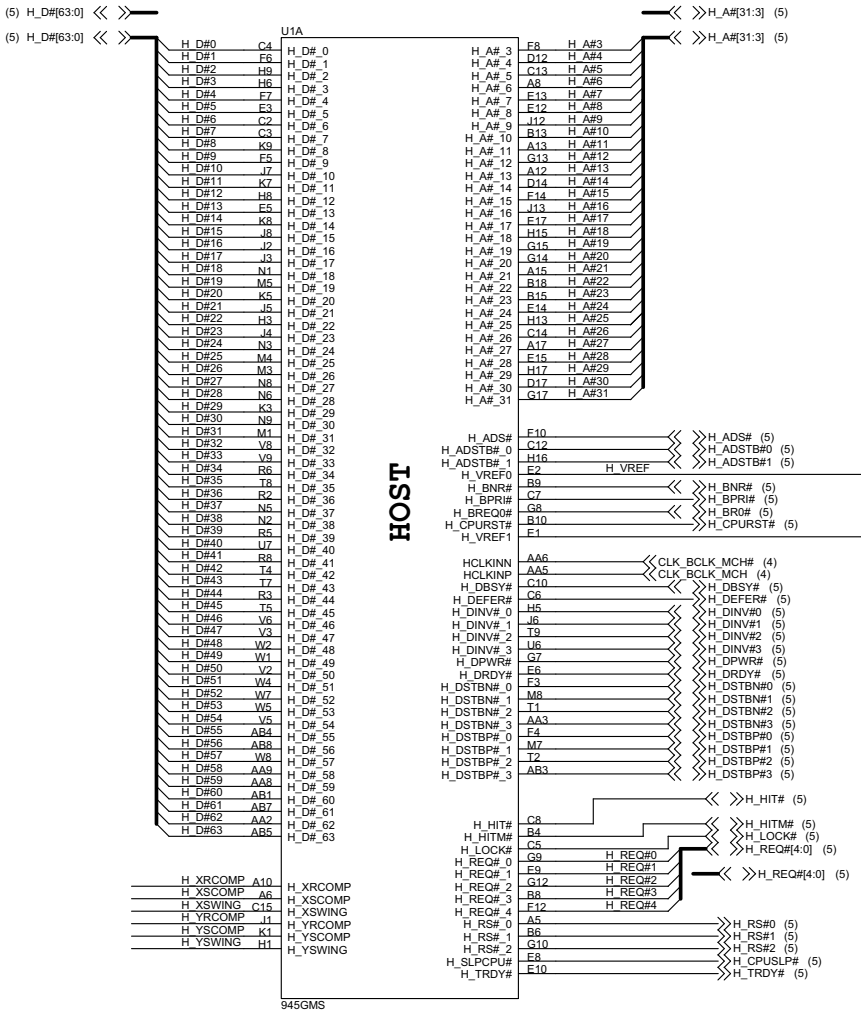


Voltage Swing

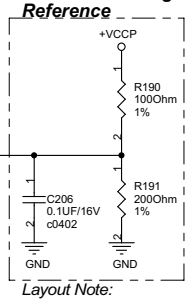
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



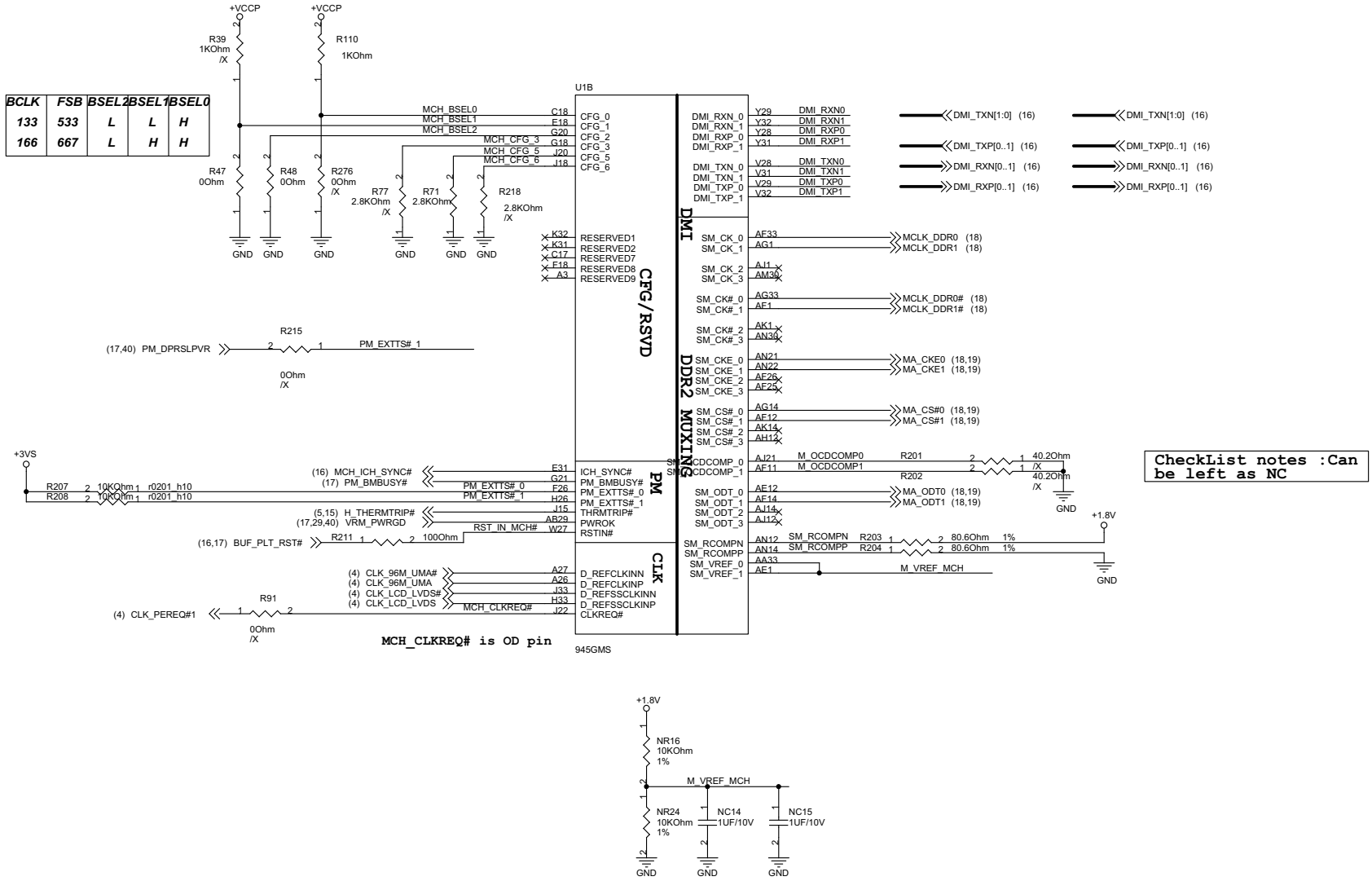
AGTL+ I/O Voltage Reference



Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

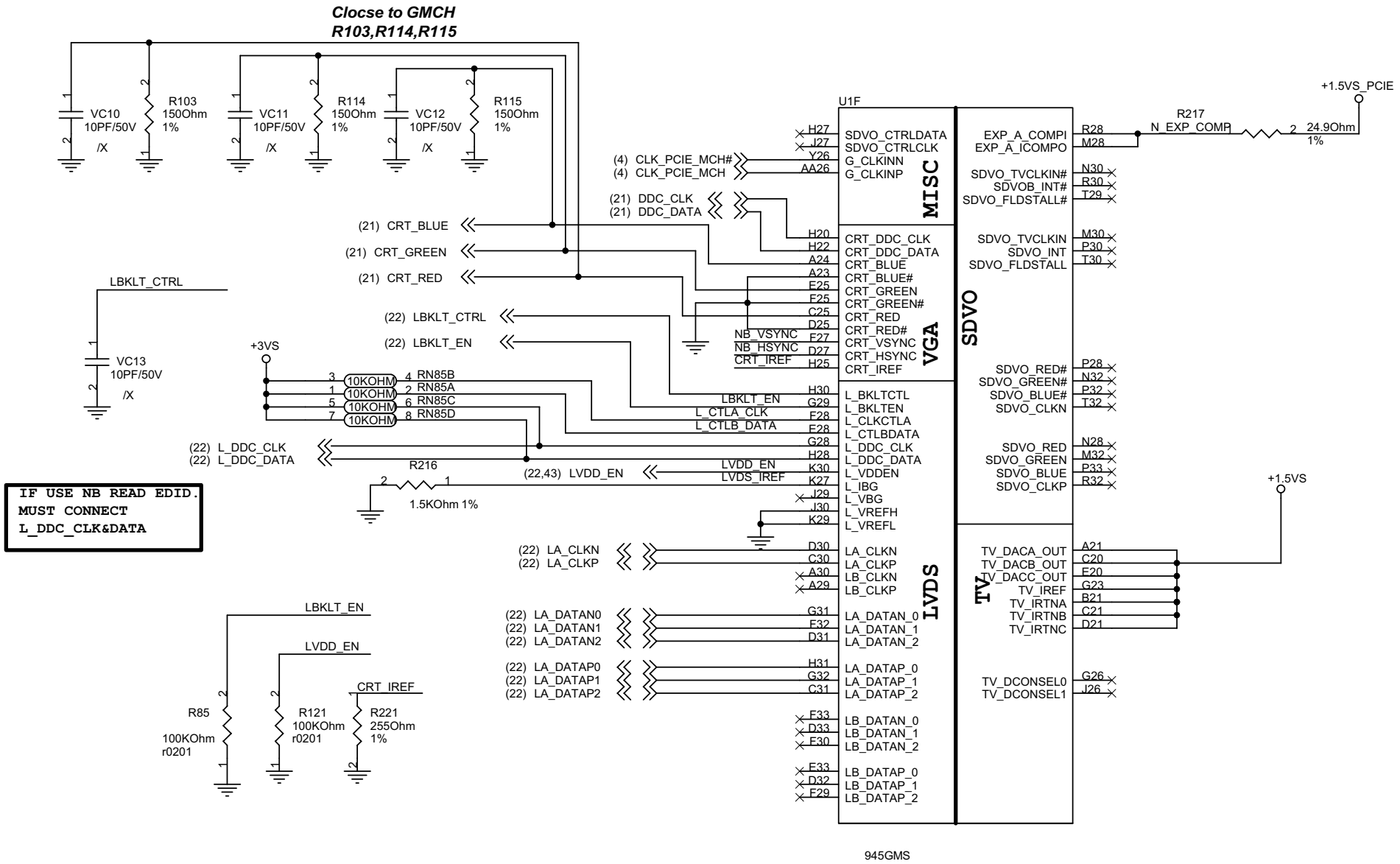
<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(HOST)	
	Engineer: *Satan He*	
Size: A3	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 7 of 49	



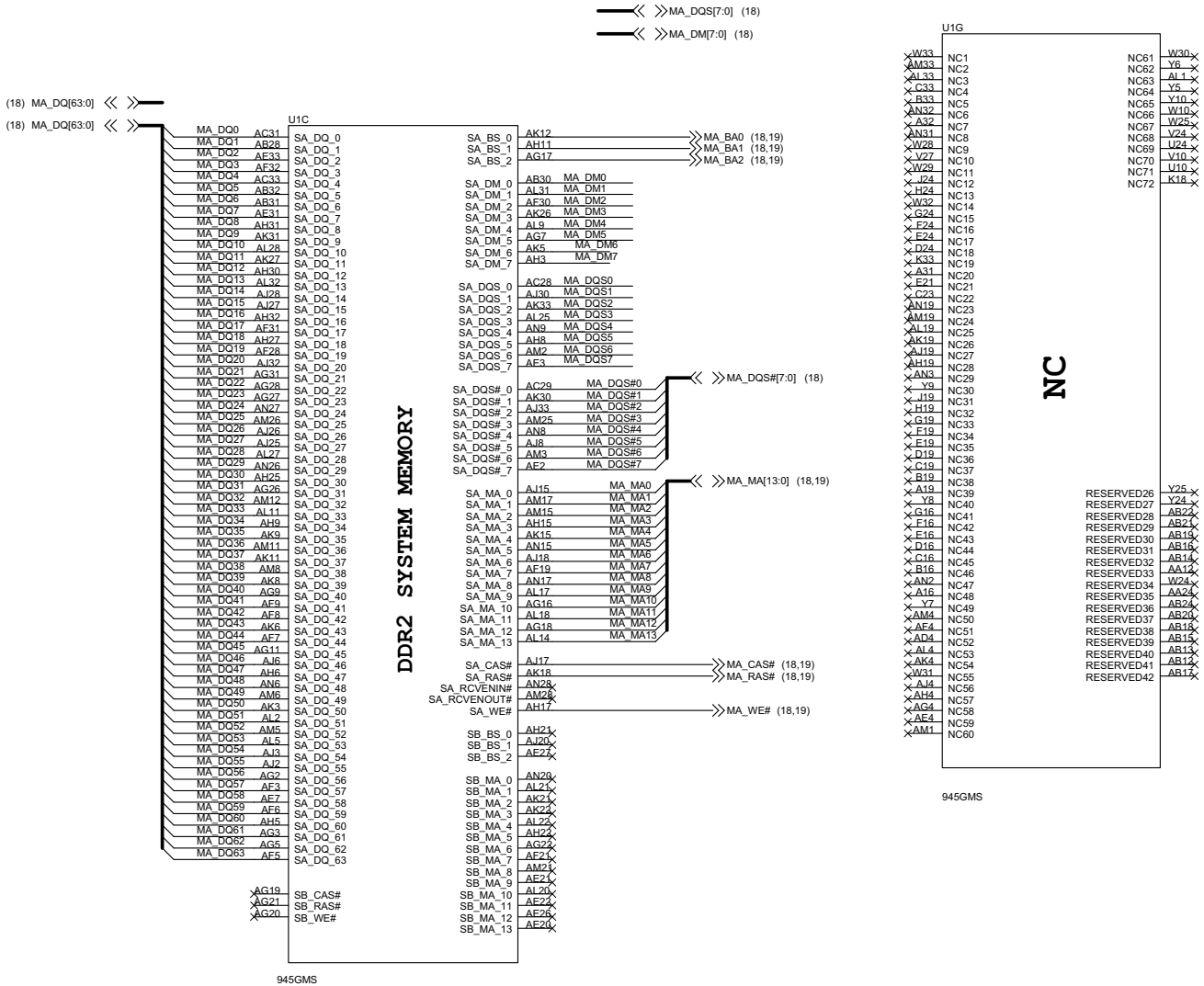
<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(DMI & CFG)	
	Engineer: *Satan He*	
Size: A3	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 8 of 49	



<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(GRAPHIC)	
	Engineer: *Satan_He*	
Size: A4	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 9 of 49	



<Core Design>

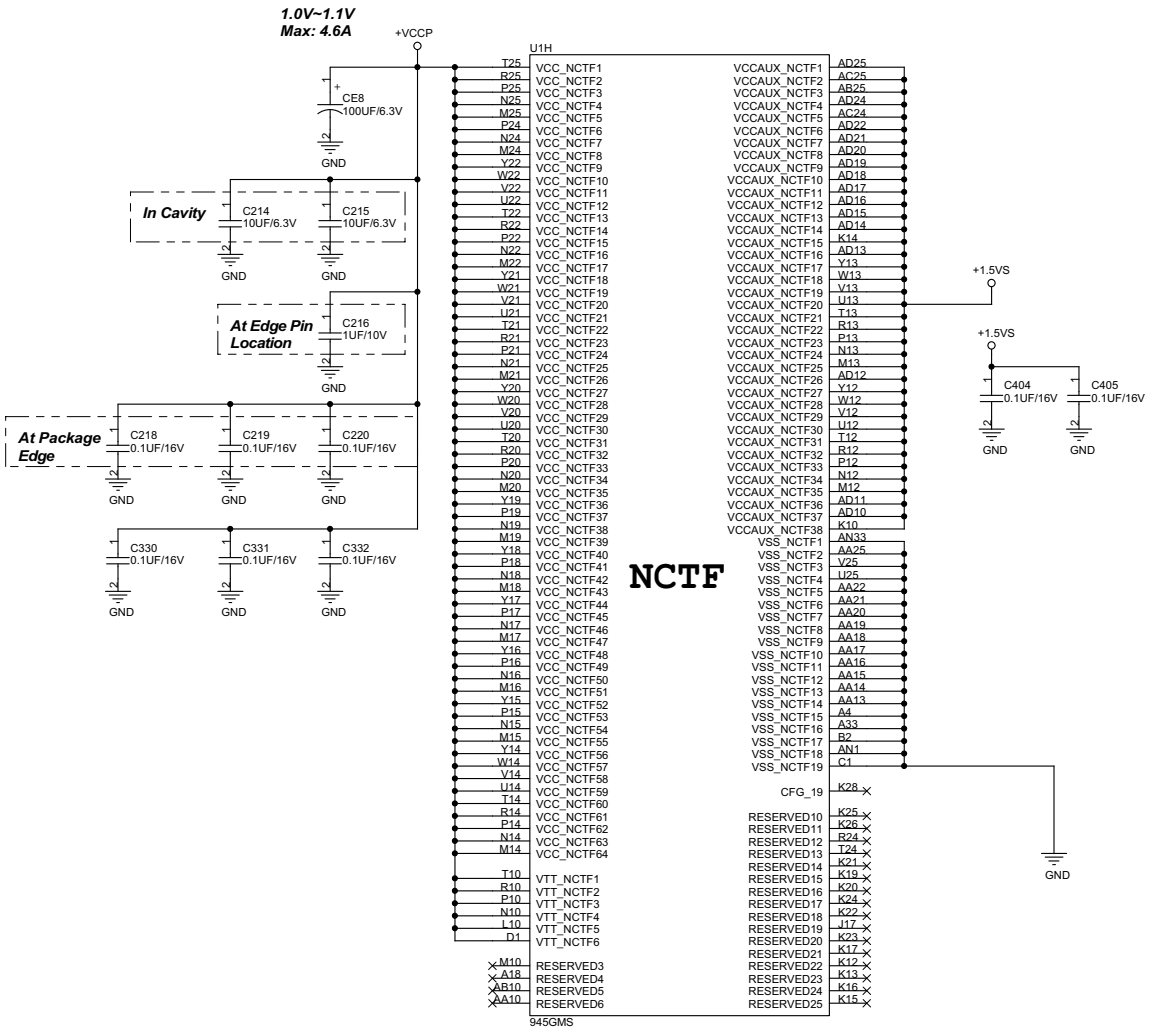
ASUSTeK COMPUTER INC.

Title : NB-945GMS(DDR2)

Engineer: *Satan He*

Size	Project Name	Rev
A3	**MK90H**	1.1G

Date: Friday, April 17, 2009 Sheet 10 of 49




```
CFG_19(K28) Strapping :
DMI LANE Reversal:
0:Normal Operation (Default)
1.:Reversal Lanes, 3->0,2->1..etc
Note:945GMS doesn't support DMI Lane
Reversal
```

<Core Design>

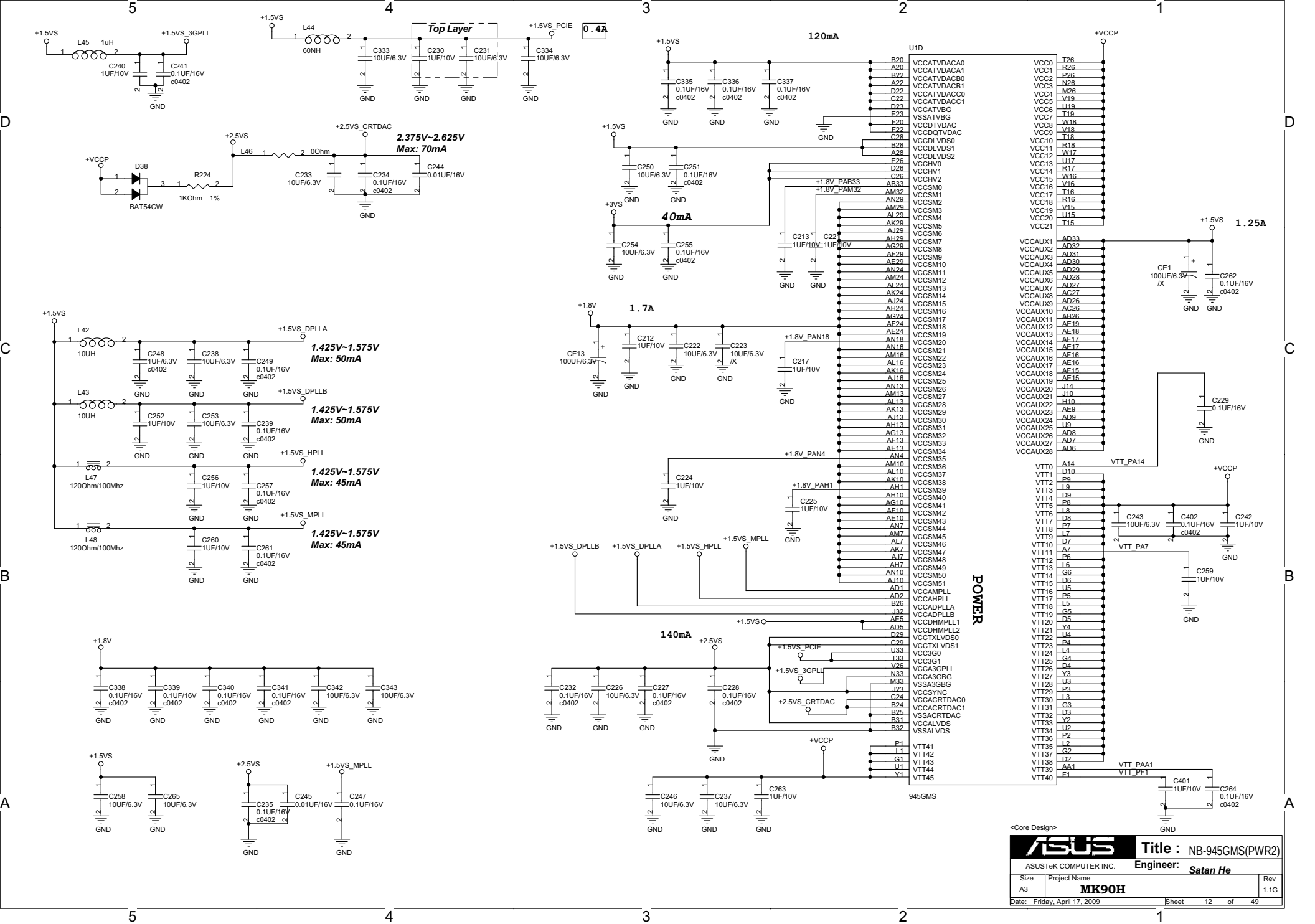
ASUSTeK COMPUTER INC.

Title : NB-945GMs(PWR)

Engineer: Satan_He

Size	Project Name	Rev
A3	MK90H	1.1G

Date: Friday, April 17, 2009 Sheet 11 of 49



<Core Design>

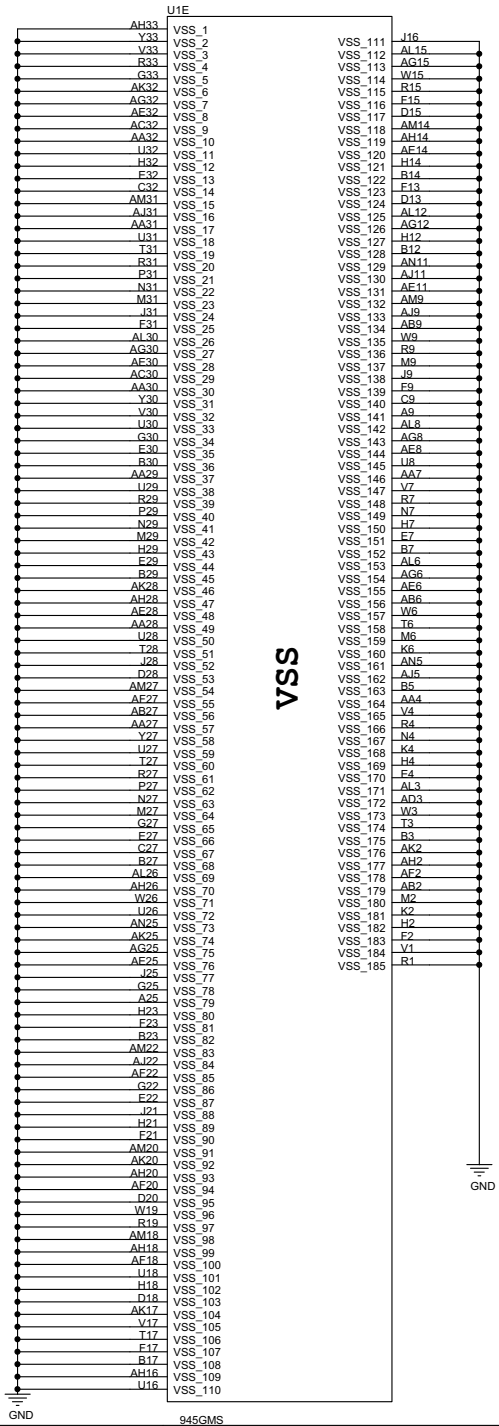
ASUSTeK COMPUTER INC.

Title : NB-945GMS(PWR2)

Engineer: Satan He

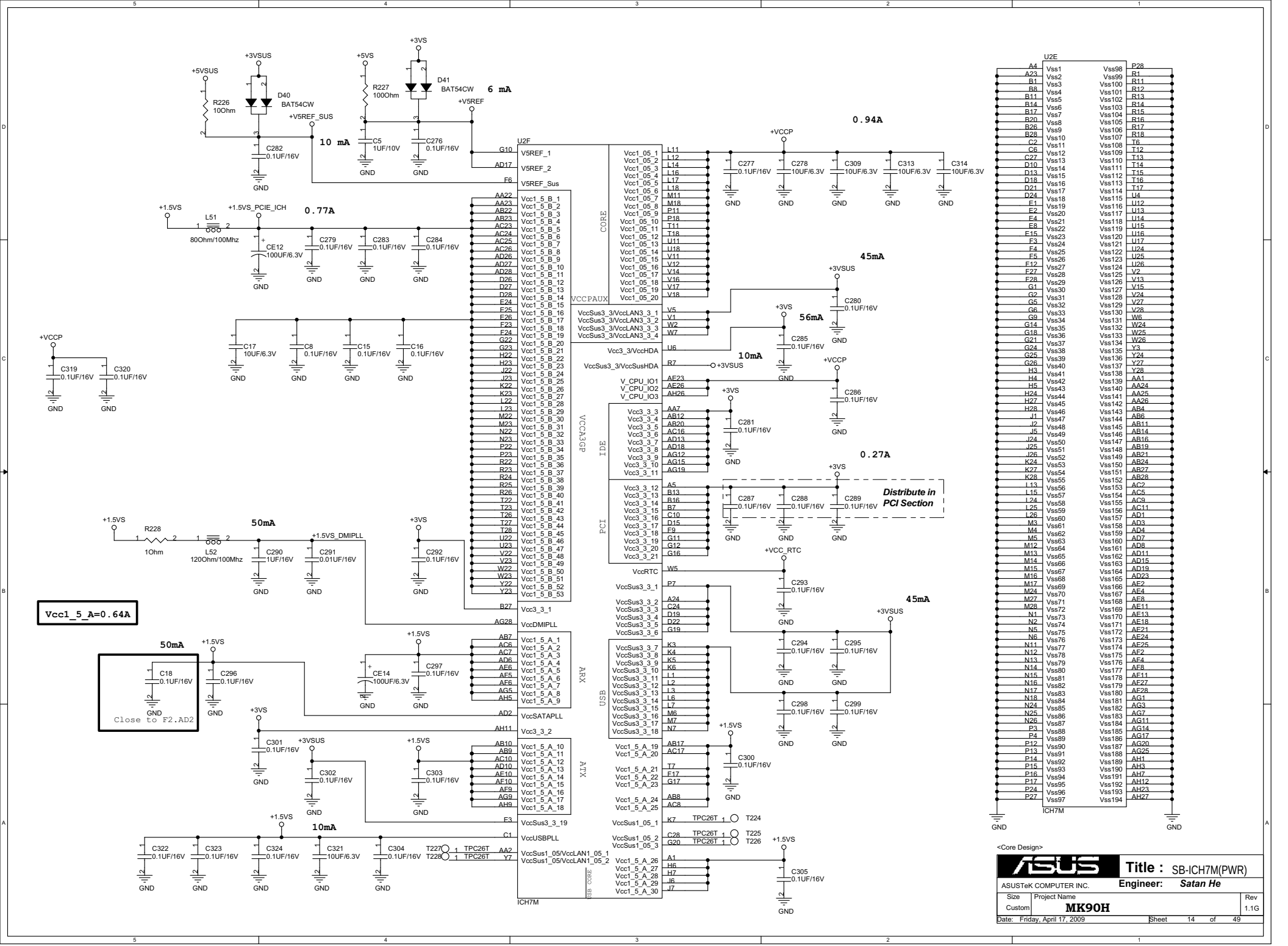
Size	Project Name	Rev
A3	MK90H	1.1G

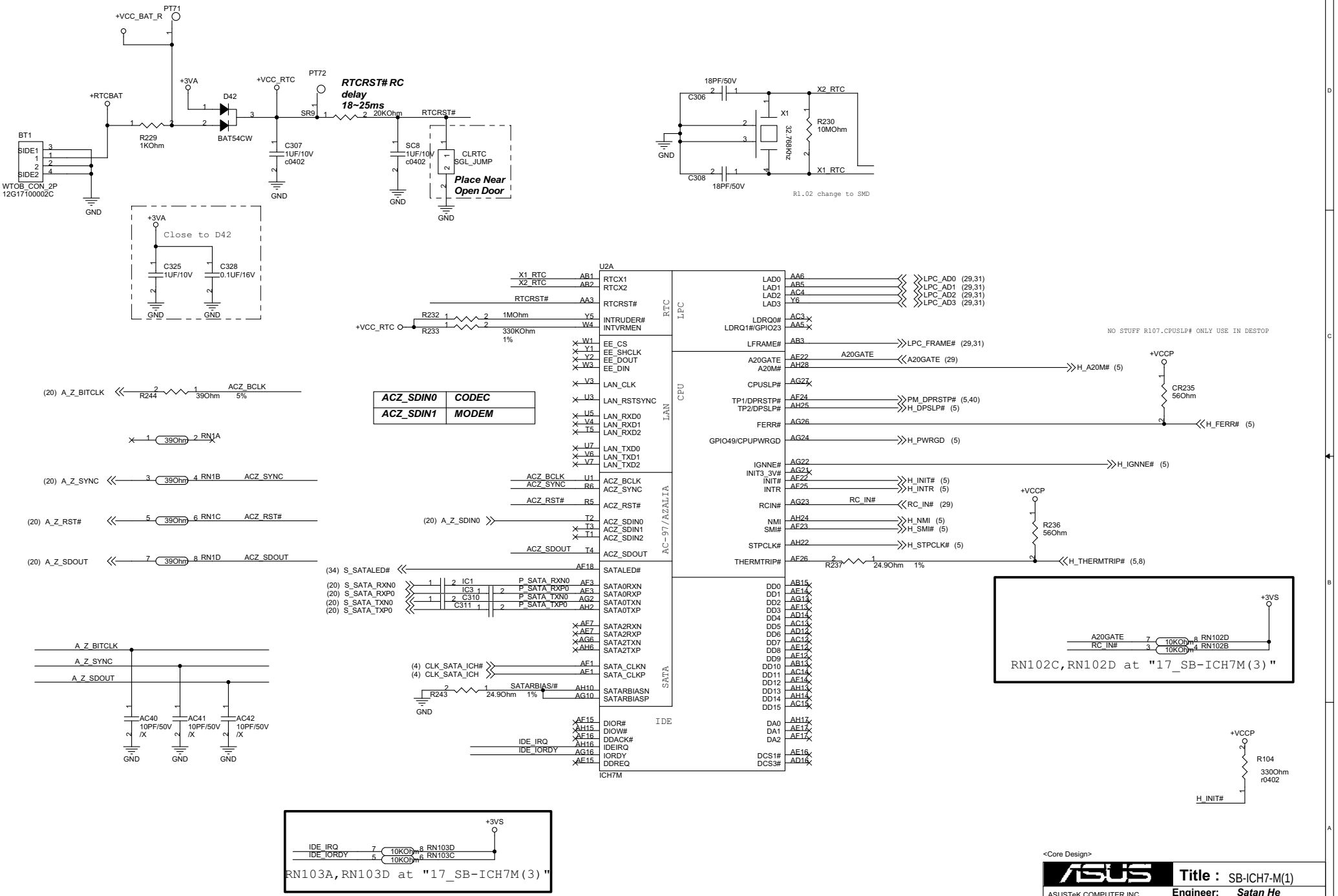
Date: Friday, April 17, 2009 Sheet 12 of 49



<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945PMS(GND)	
	Engineer: *Satan_He*	
Size: A3	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 13 of 49	





<Core Design>

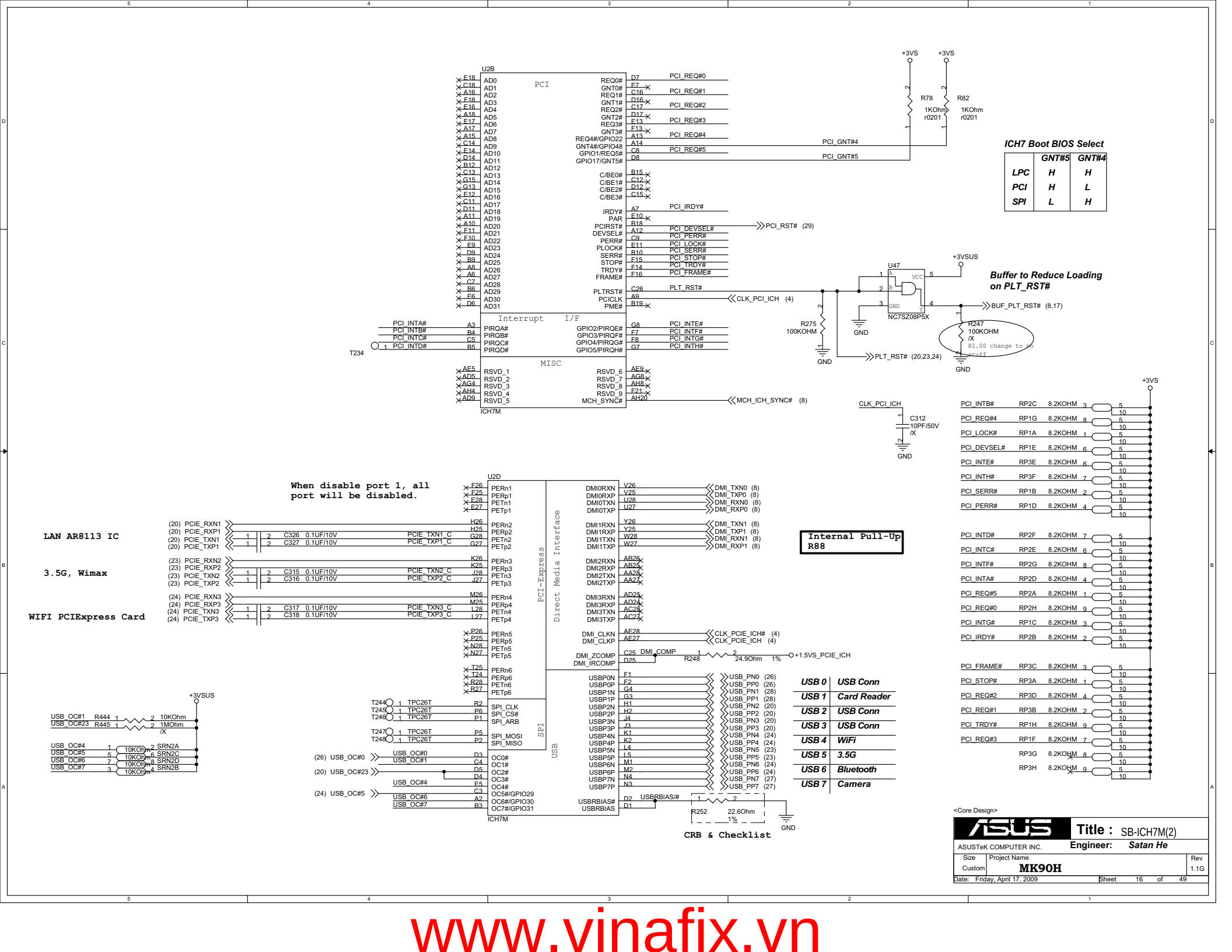
ASUSTeK COMPUTER INC.

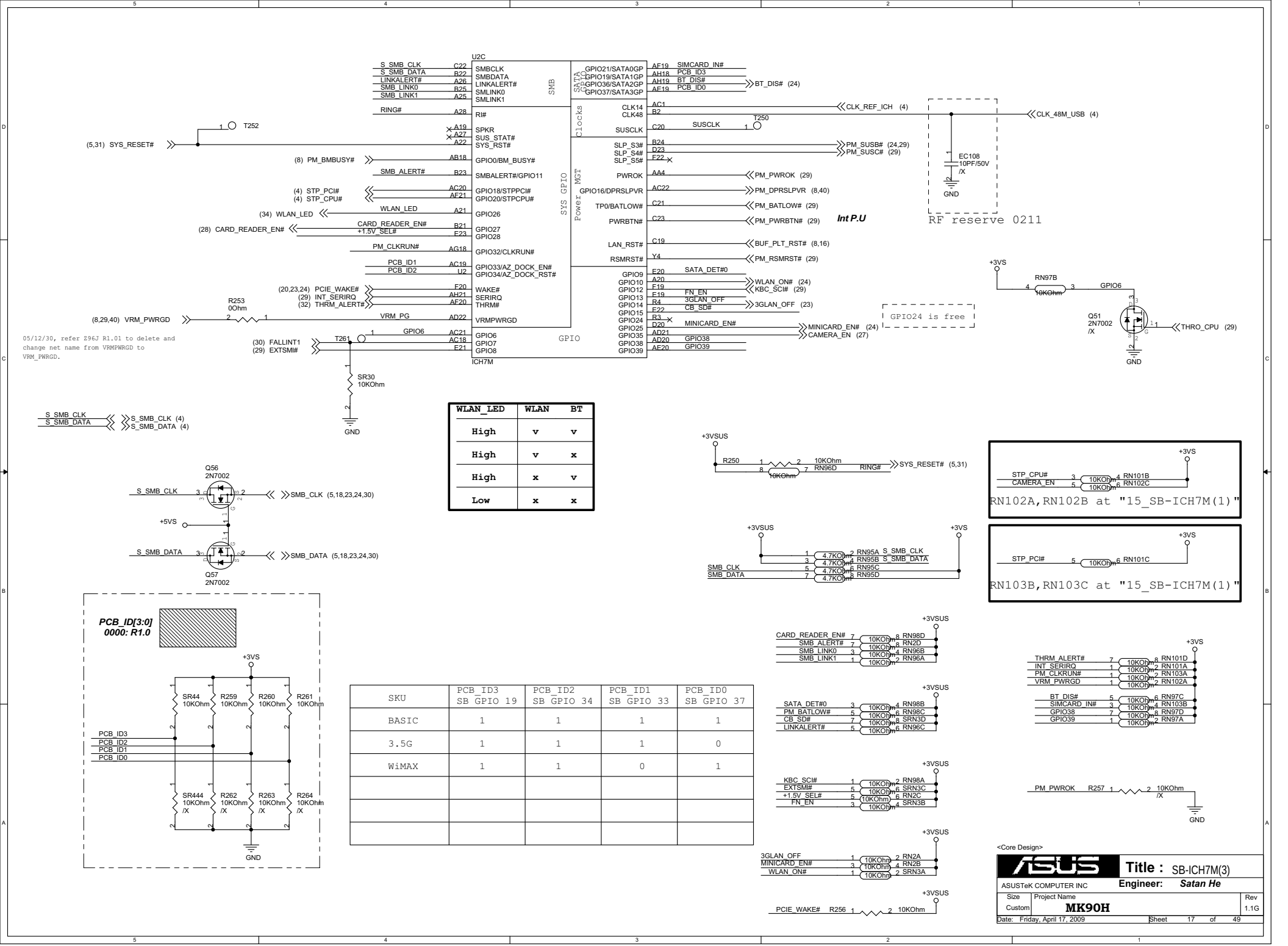
Title : SB-ICH7-M(1)

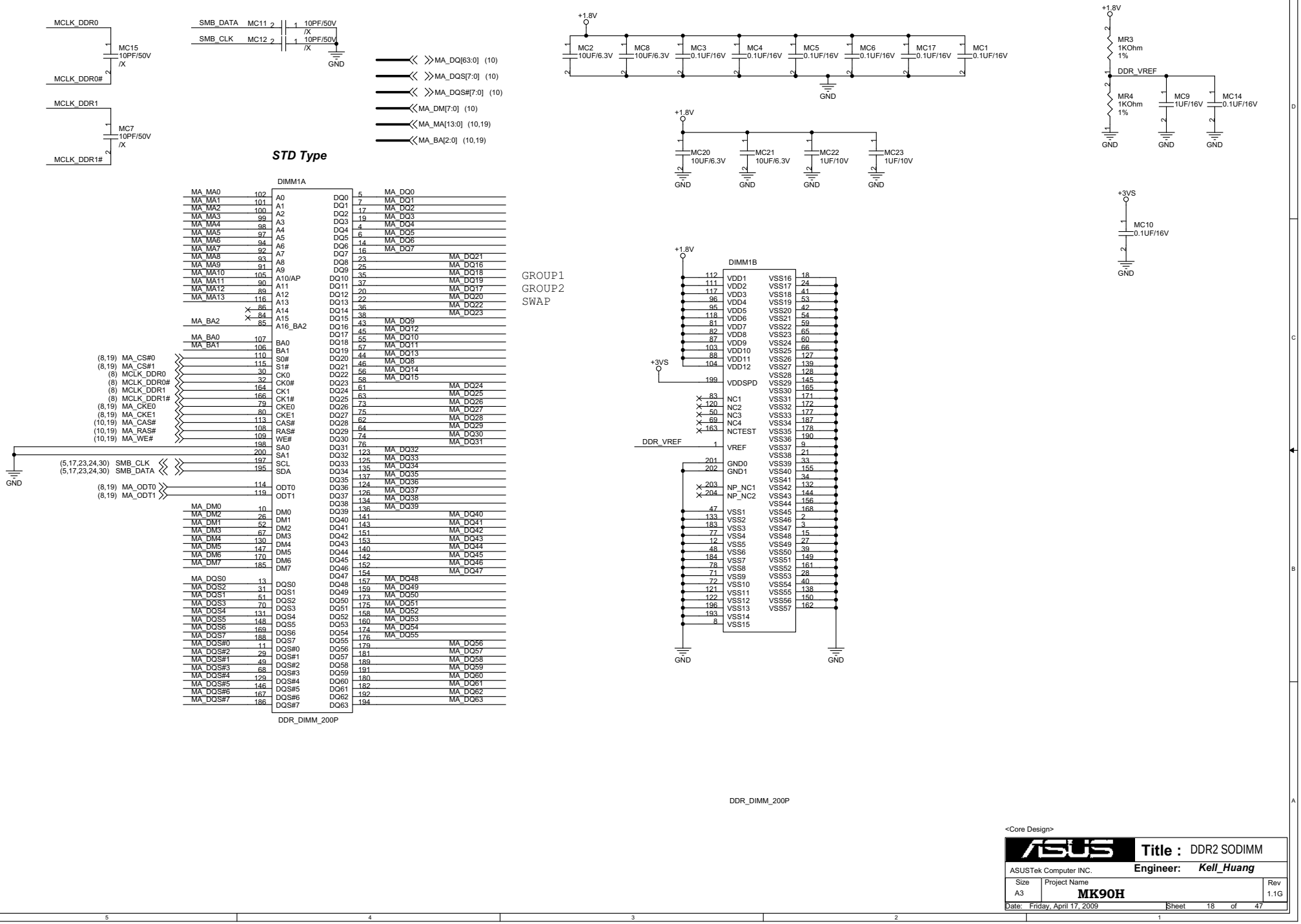
Engineer: Satan He

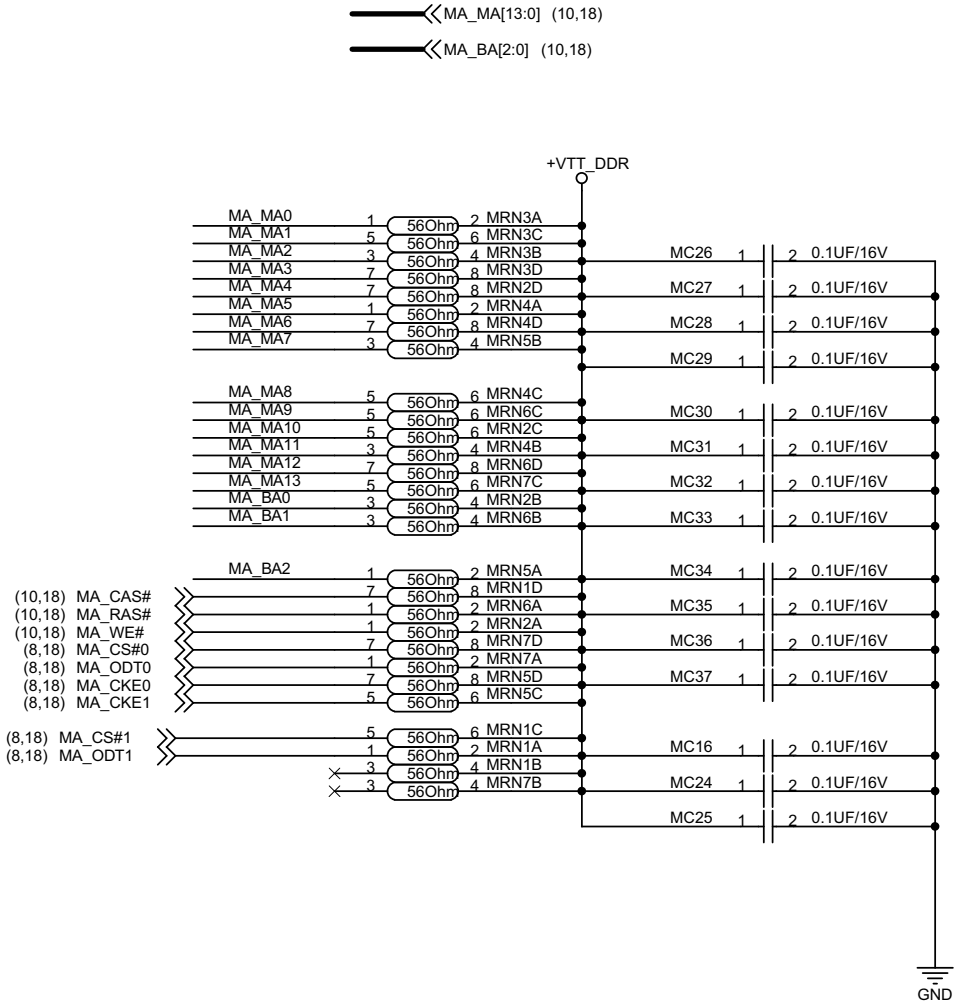
Size	Project Name	Rev
Custom	MK90H	1.1G

Date: Friday, April 17, 2009 Sheet 15 of 49



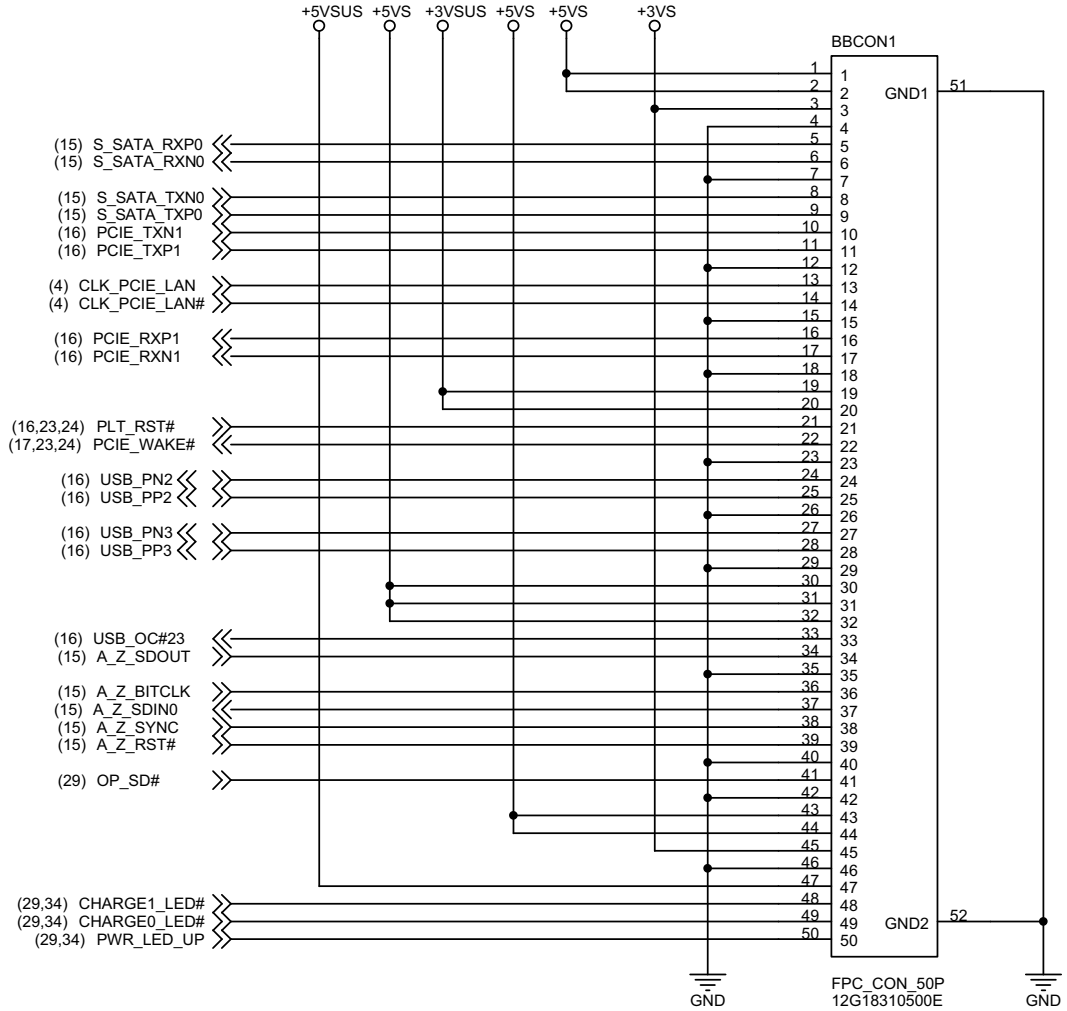






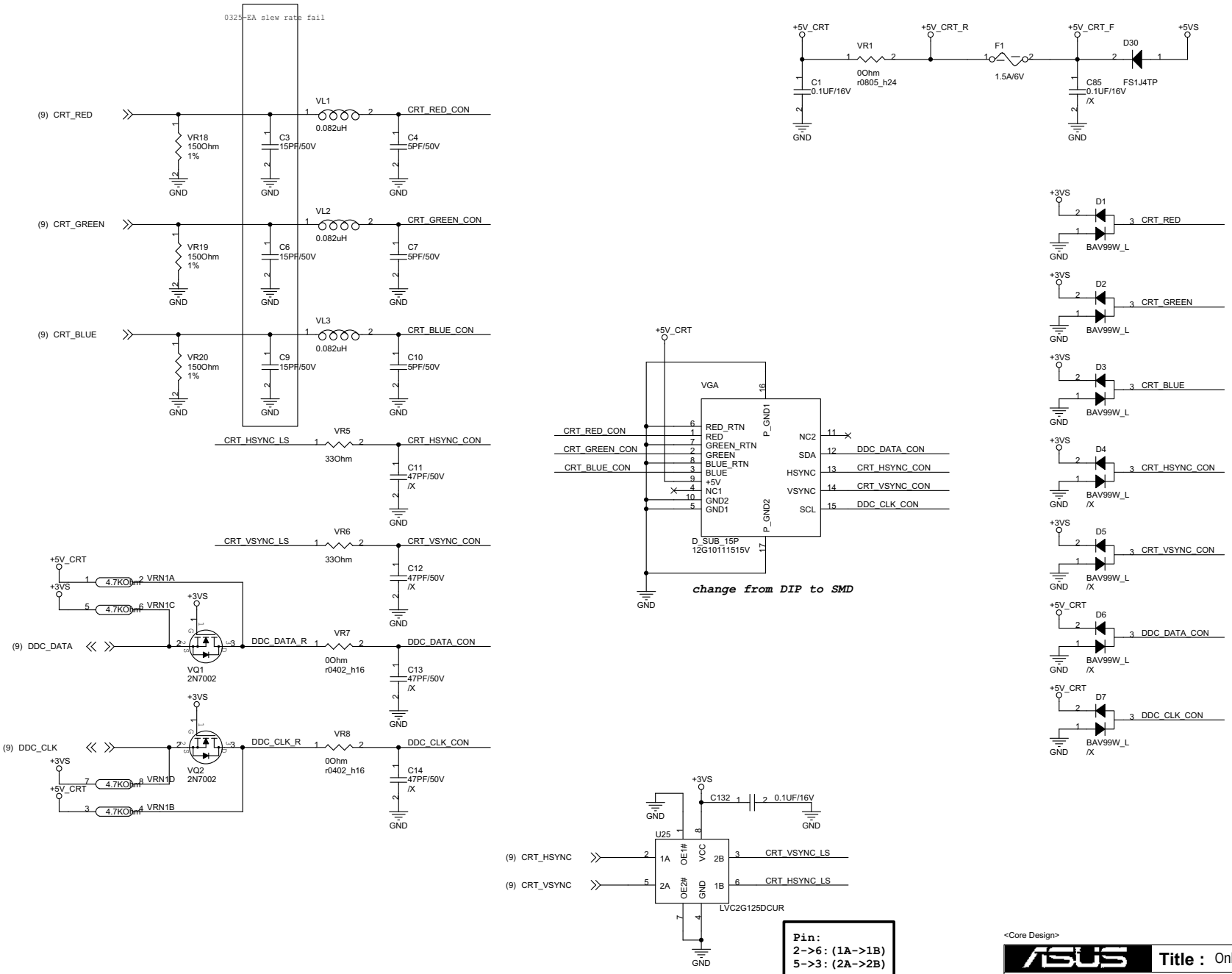
<Core Design>

ASUSTek Computer Inc.	Title : DDR2_Termination	
	Engineer: Kell_Huang	
Size: A4	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 19 of 49	



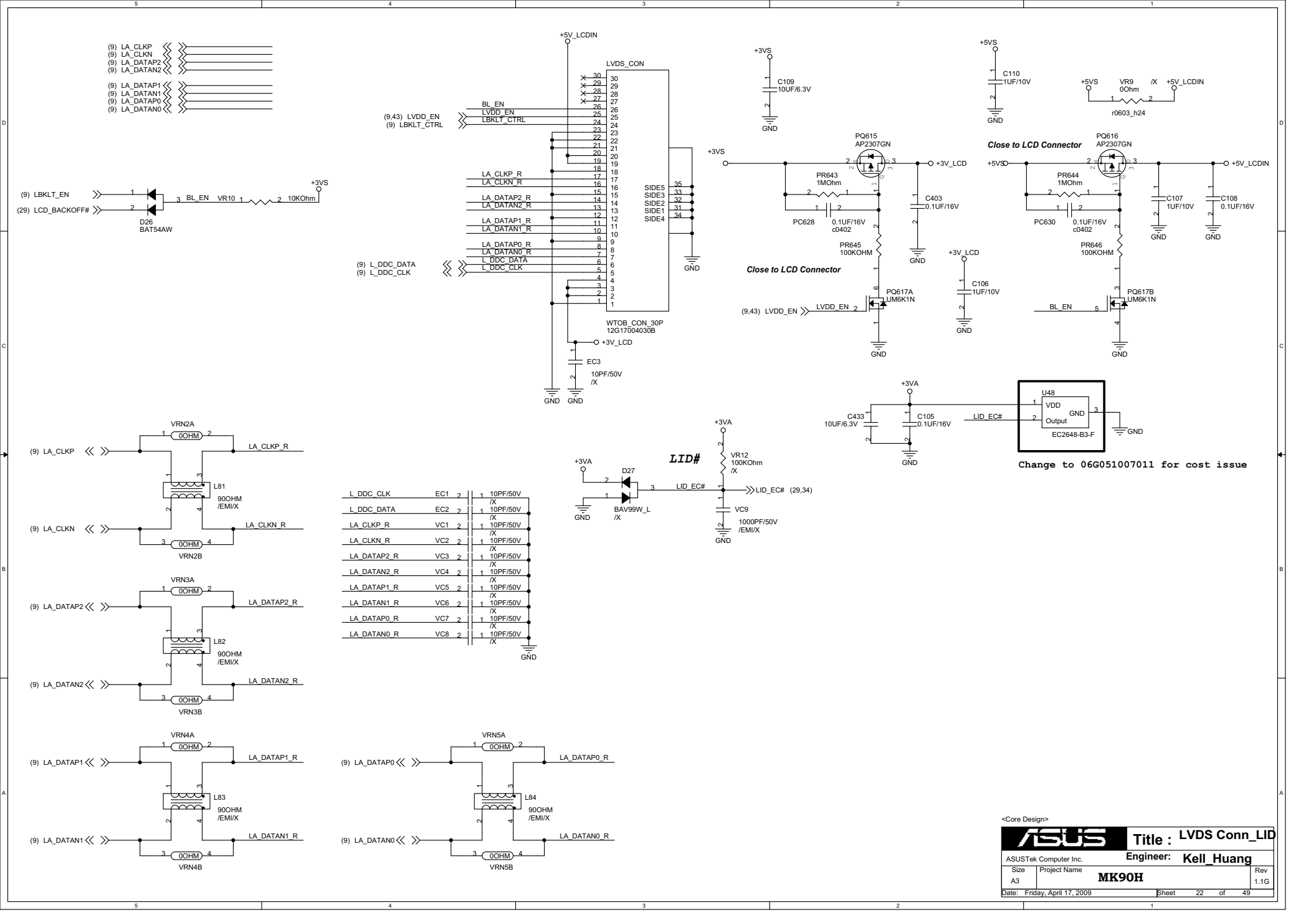
<Core Design>

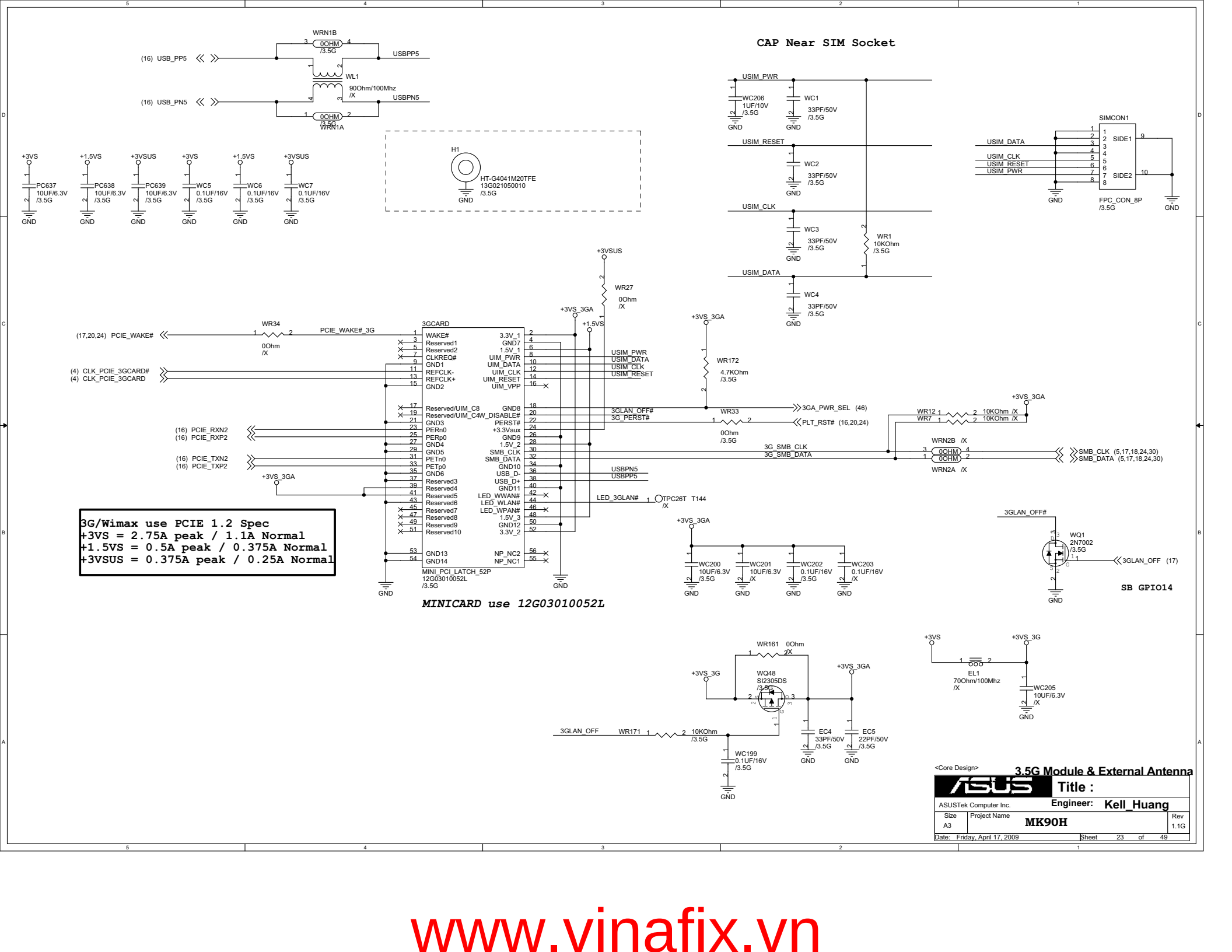
ASUSTek Computer INC.	Title : B to B connector	
	Engineer: *Boison_Hung*	
Size: A4	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 20 of 49	

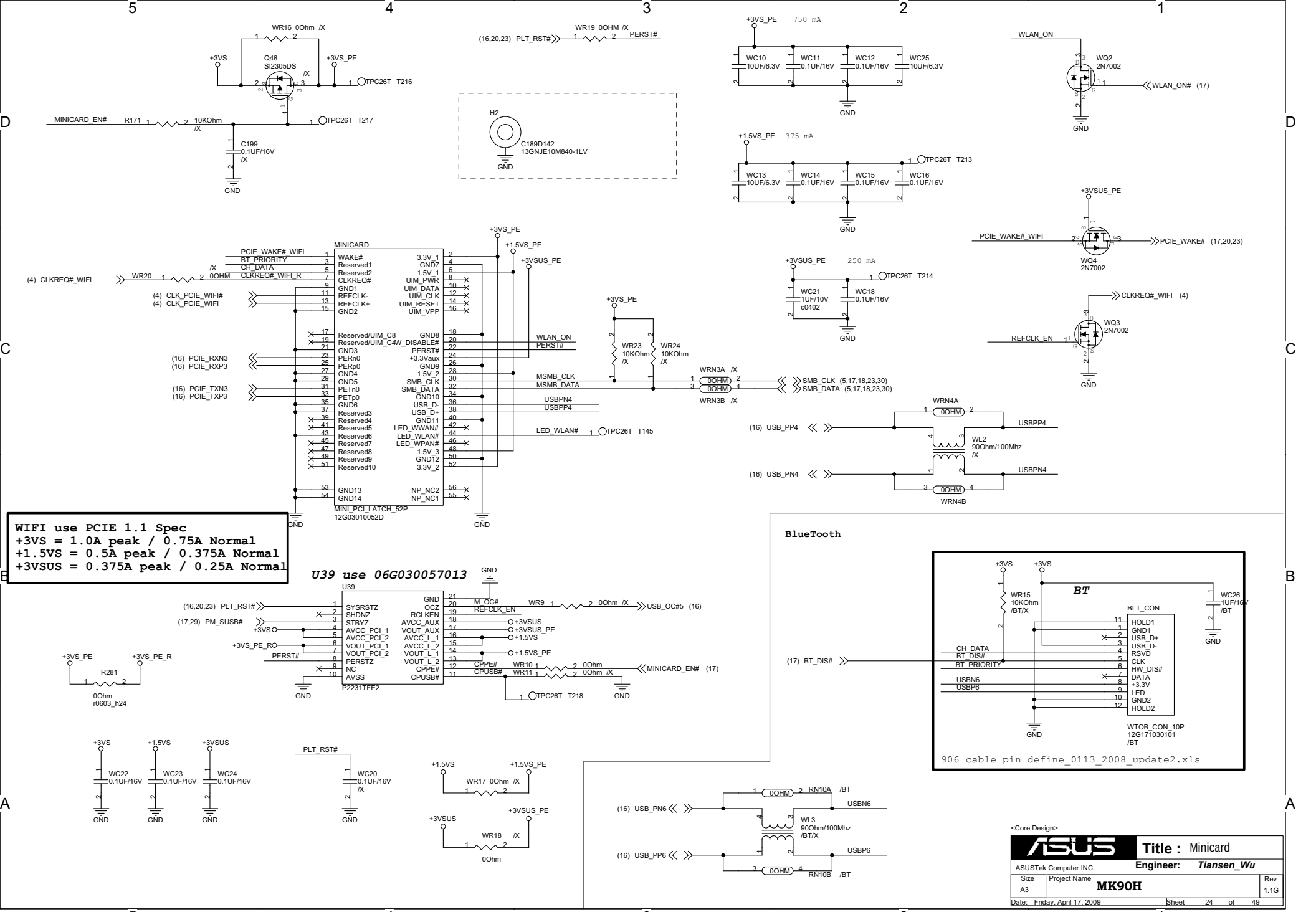


<Core Design>

ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: *Kell_Huang*	
Size: A3	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 21 of 49	







Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?

<Core Design>

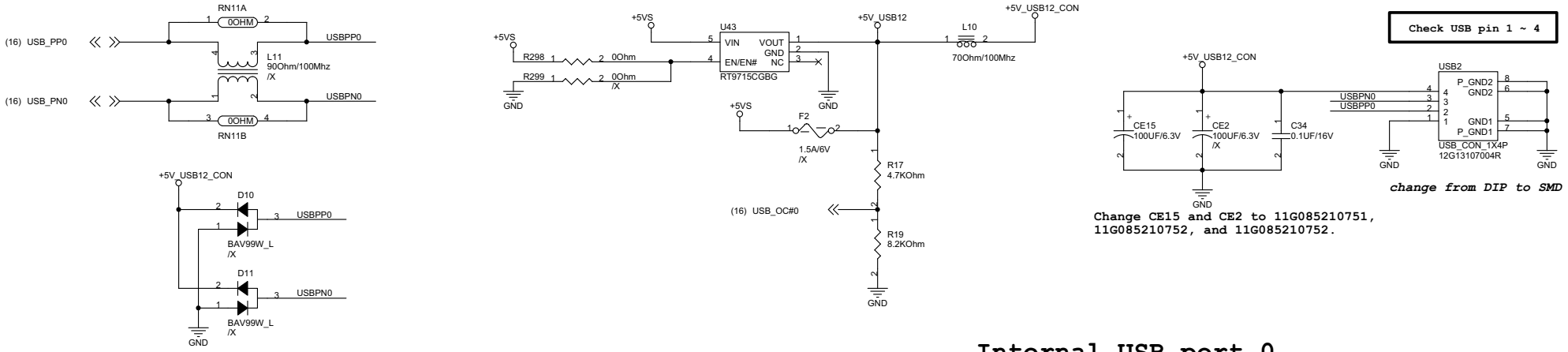
ASUSTek Computer INC.

Title : HD + Flash Conn

Engineer: *Kell_Huang*

Size	Project Name	Rev
A4	**MK90H**	1.1G

Date: Friday, April 17, 2009 Sheet 25 of 49



Change CE15 and CE2 to 11G085210751, 11G085210752, and 11G085210752.

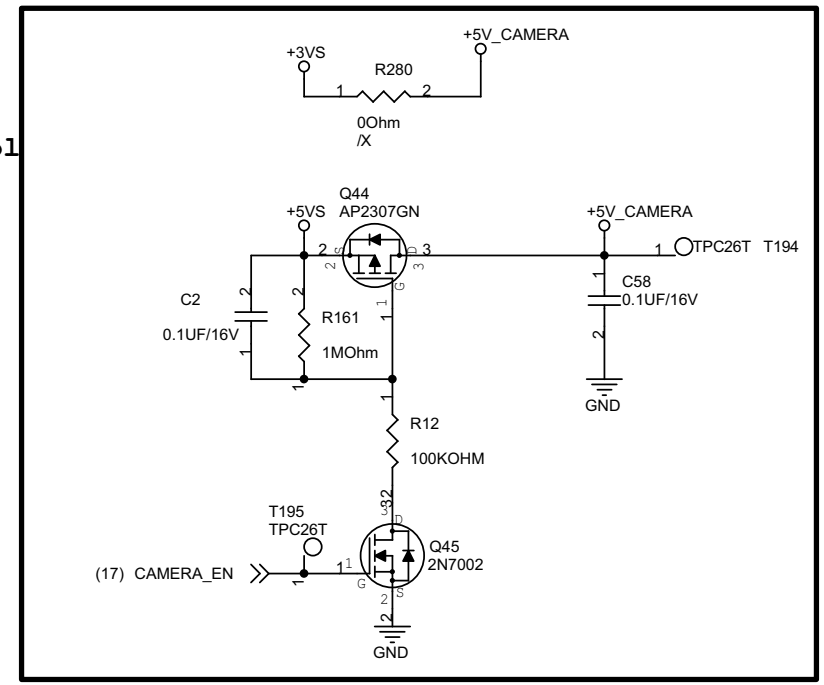
Internal USB port 0

External USB port 2,3

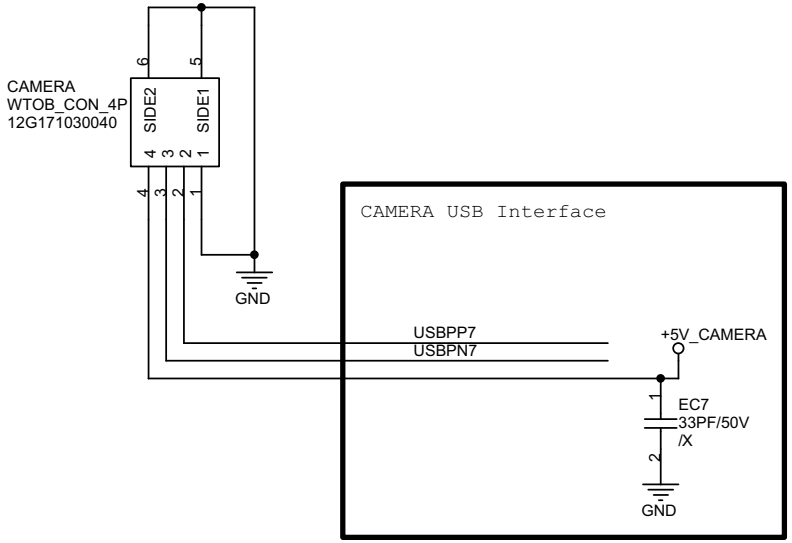
<Core Design>

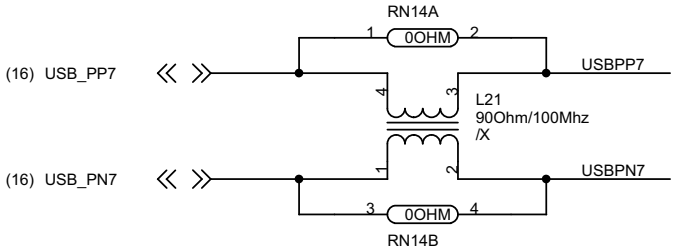
ASUSTek Computer Inc.	Title : USB Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 26 of 49	

Power Control



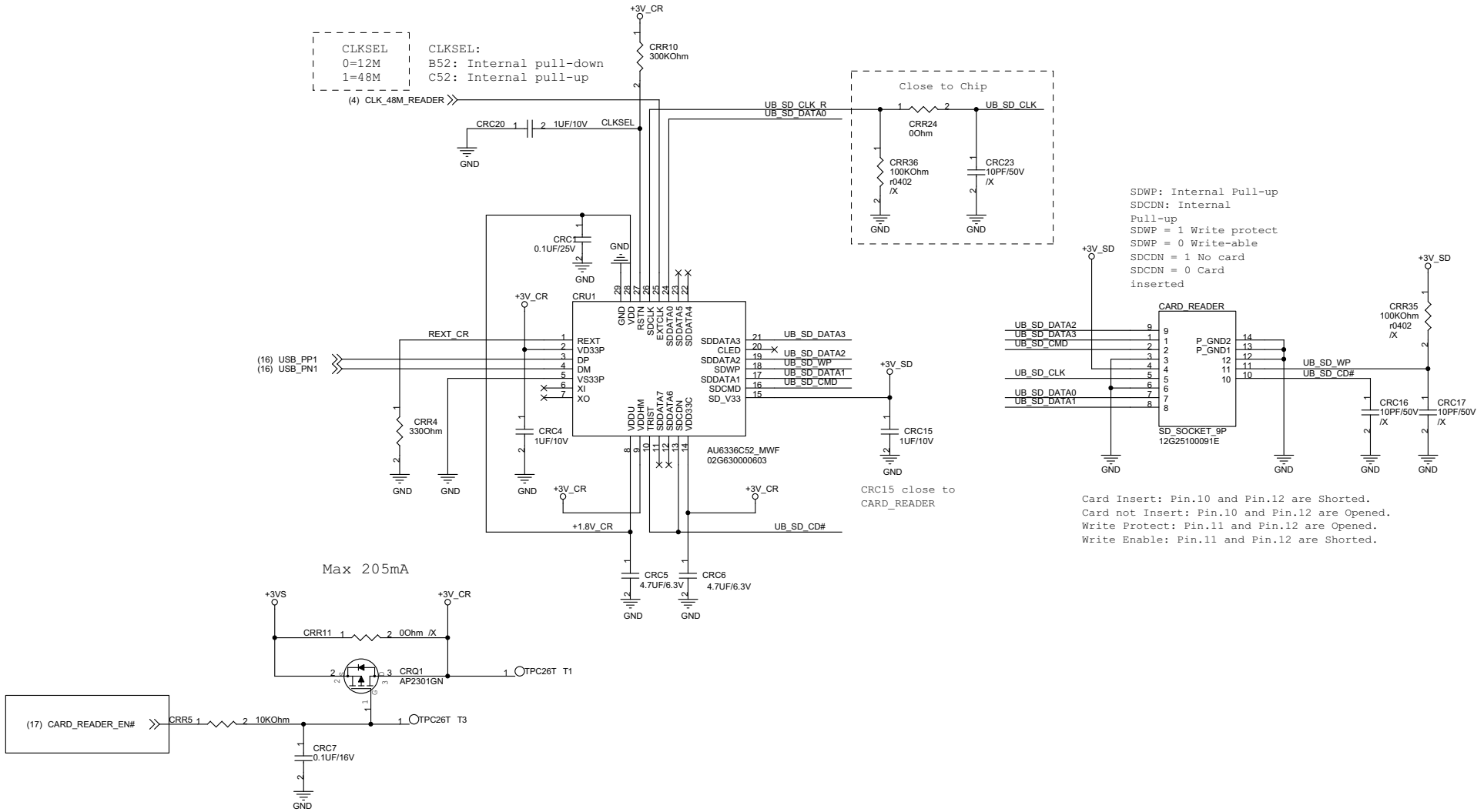
Check





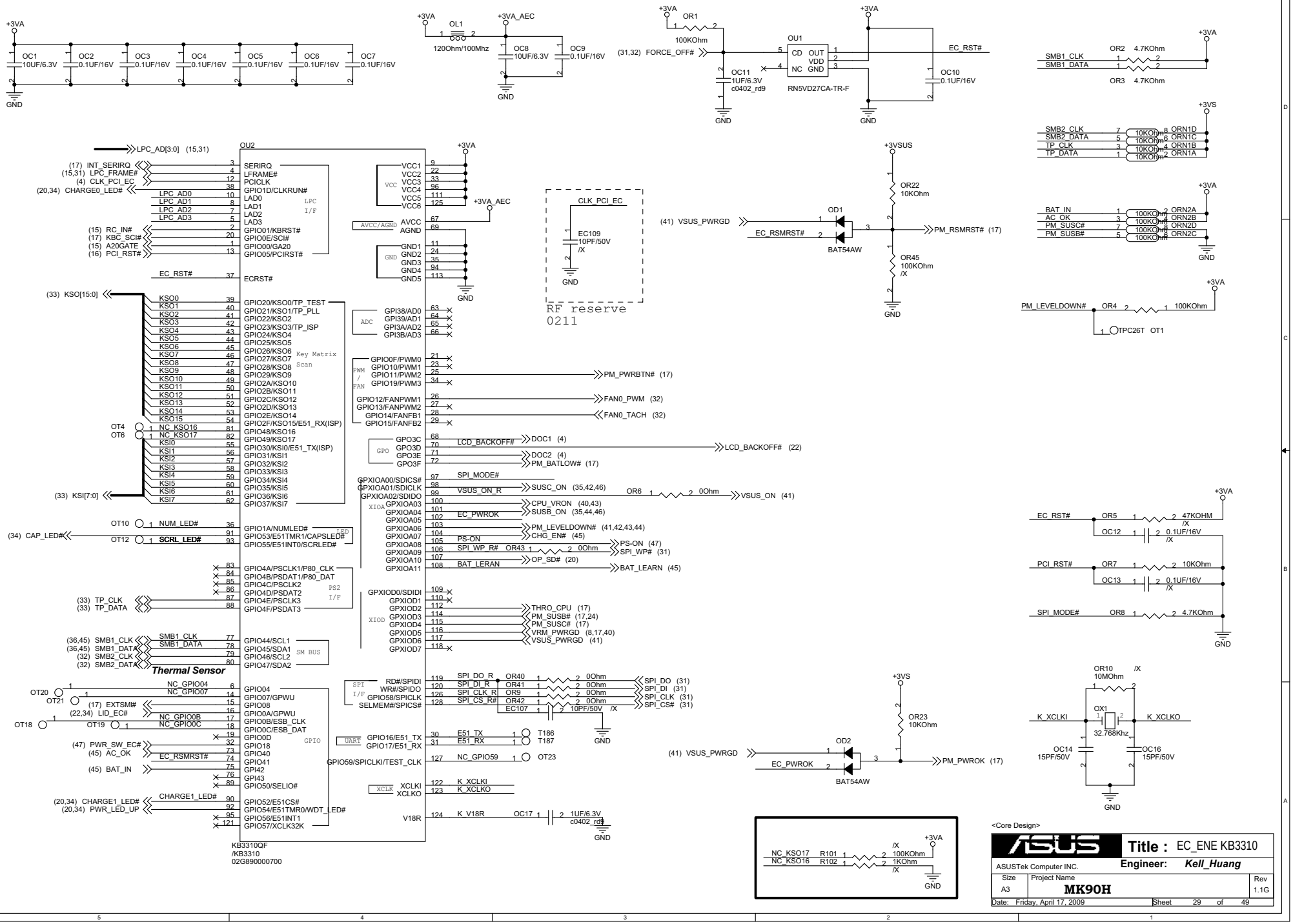
<Core Design>

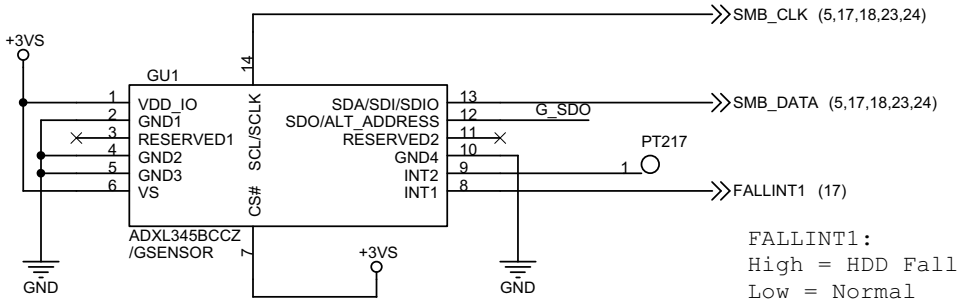
ASUSTek Computer Inc.	Title : Camera Power	
	Engineer: Kell_Huang	
Size: A4	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 27 of 49	



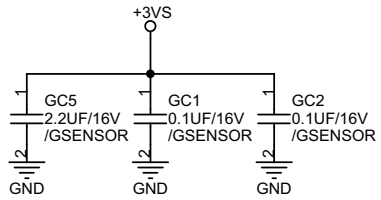
<Core Design>

ASUSTek Computer Inc.	Title : AU6336-C52	
	Engineer: Boison Hung	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 28 of 49	

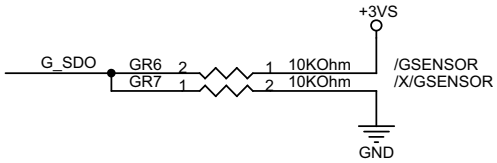


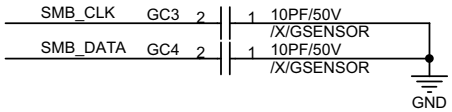


FALLINT1:
High = HDD Fall
Low = Normal



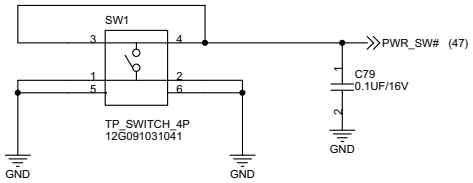
Install GR6 being slaveaddr "3A"
for ADI/Freescale/ST G-sensors

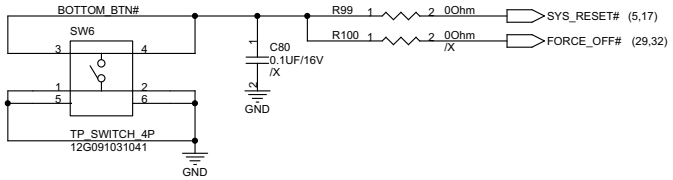




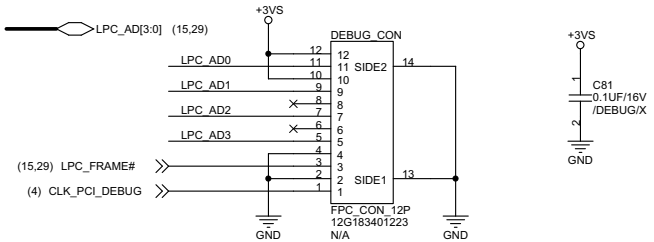
<Core Design>

ASUSTek Computer INC.	Title : G-Sensor	
	Engineer: *Kell_Huang*	
Size: A4	Project Name: **MK90H**	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 30 of 49	

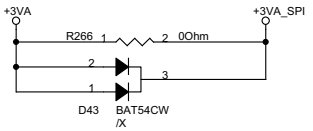


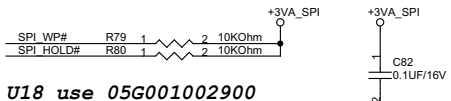


For Debug

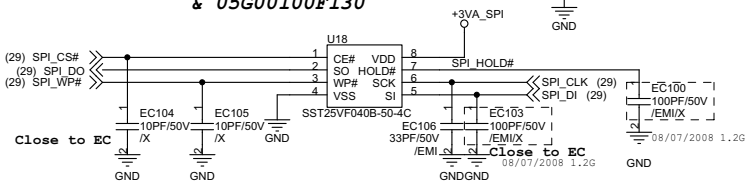


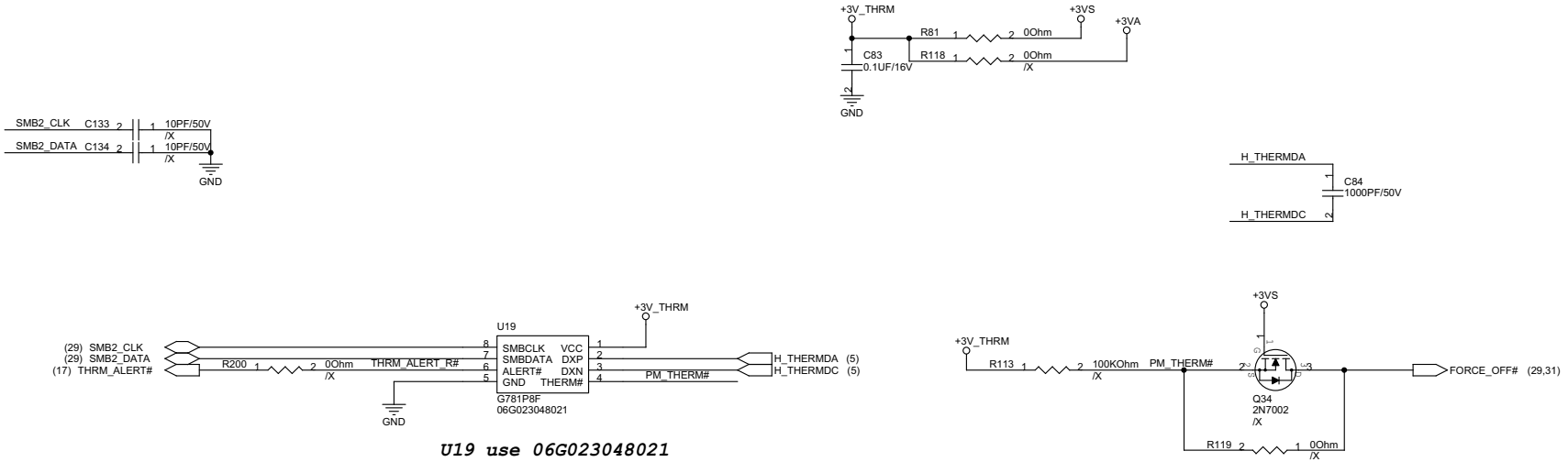
Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125



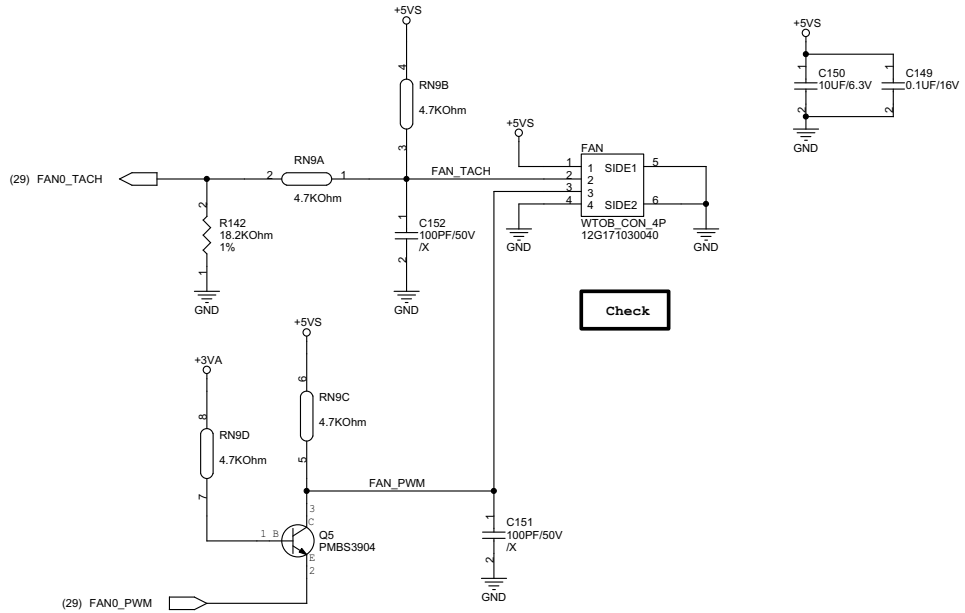


U18 use 05G001002900 & 05G00100F130

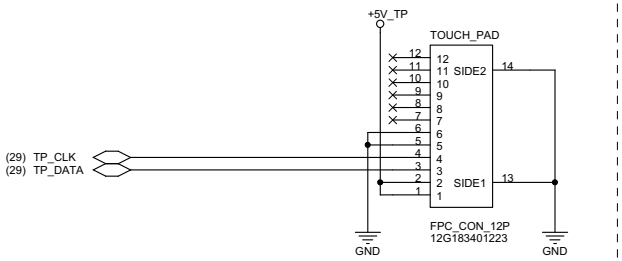


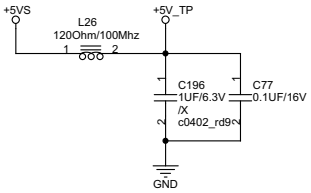


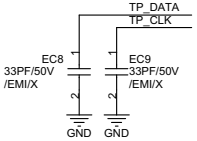
U19 use 06G023048021



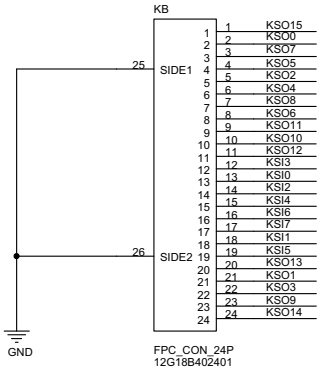
For Touch-Pad

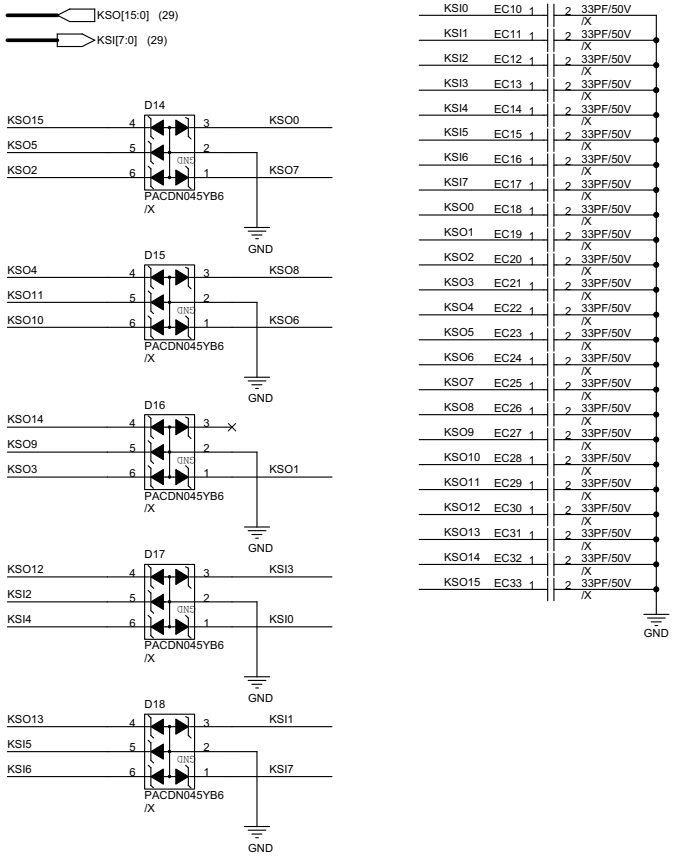






For Keyboard Connector

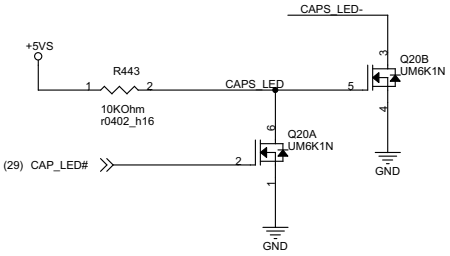




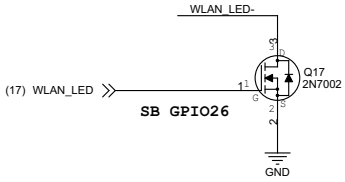
<Core Design>

ASUSTek Computer Inc.	Title : KB_Touch Pad	
	Engineer: Kell_Huang	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 33 of 49	

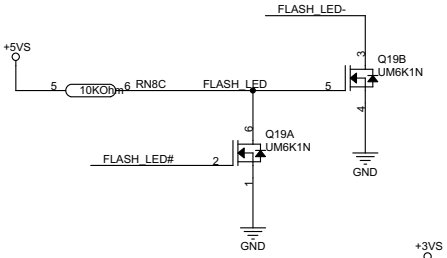
for CAPLOCK LED

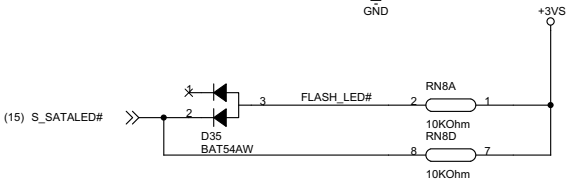


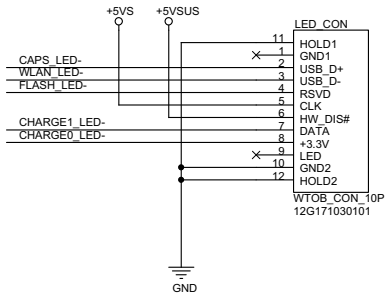
for WLAN/BlueTooth LED



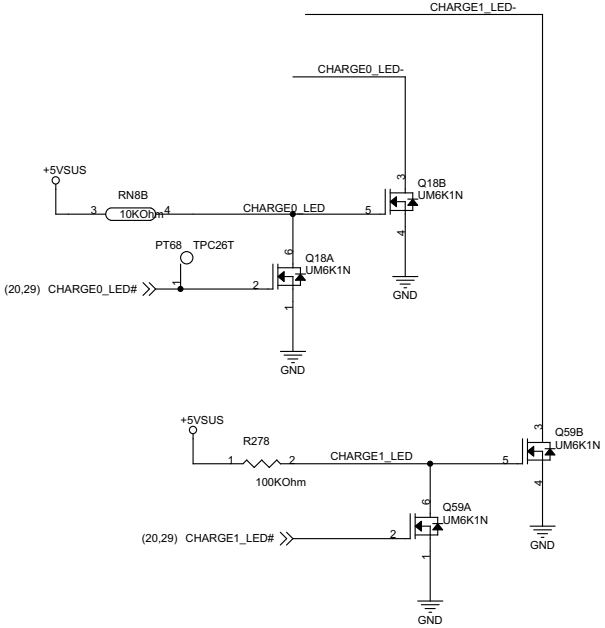
for FLASH LED



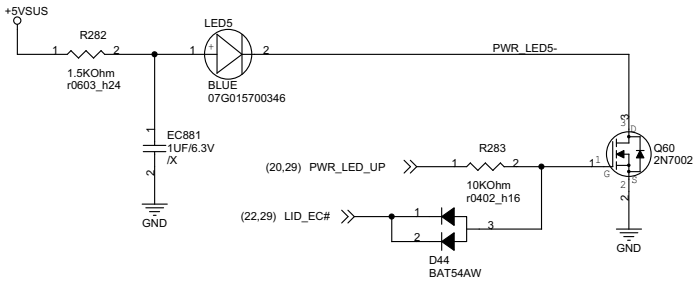




for CHARGE LED

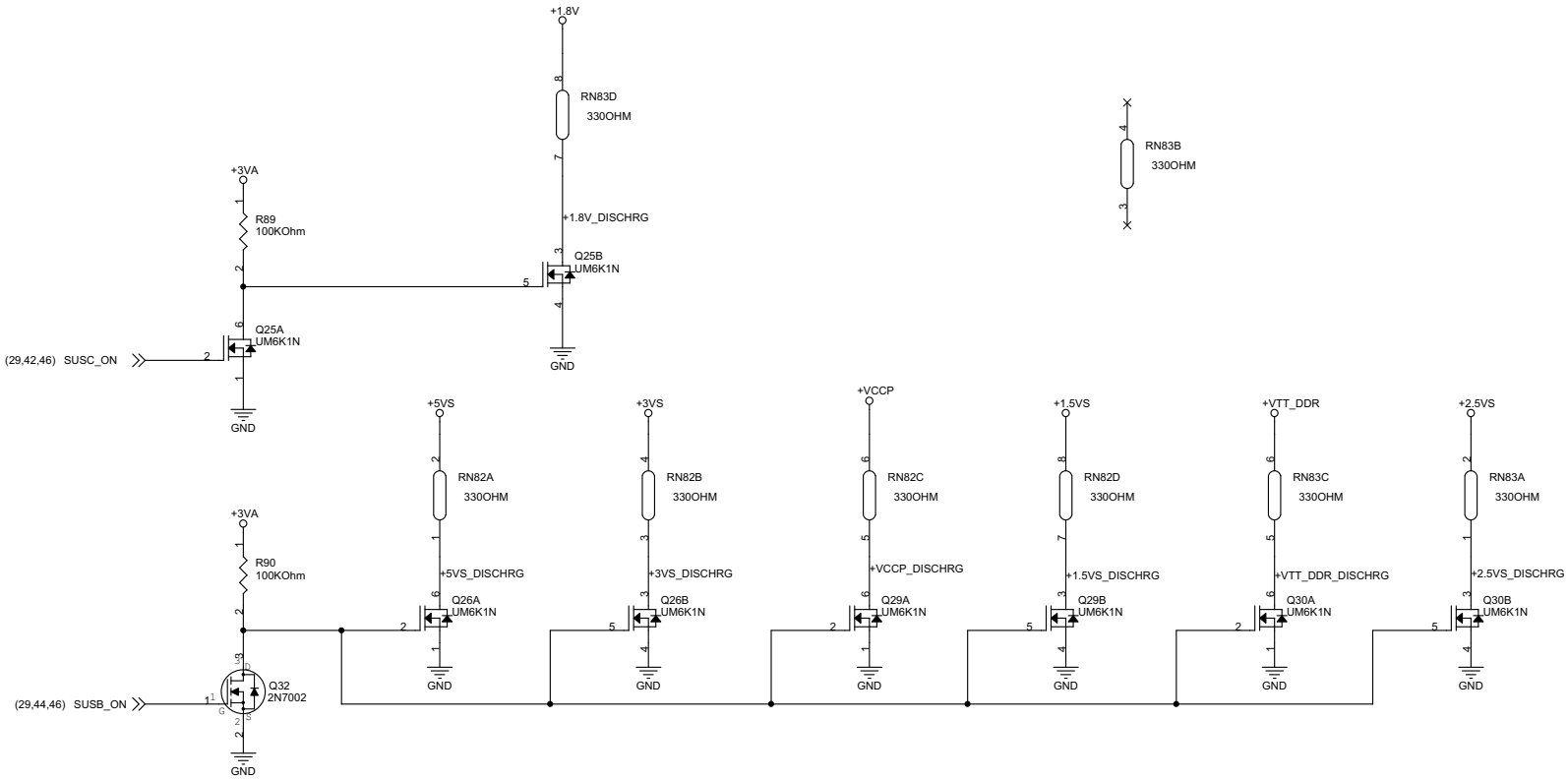


for POWER BOTTOM LED



<Core Design>

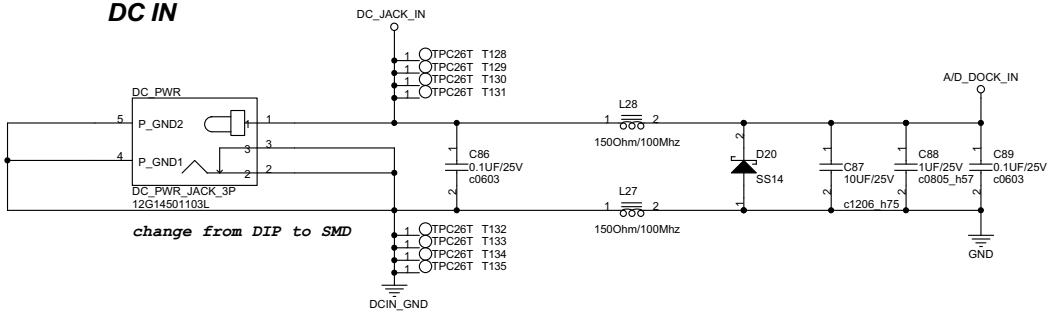
ASUSTek Computer Inc.	Title : LED	
	Engineer: Kell_Huang	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 34 of 49	



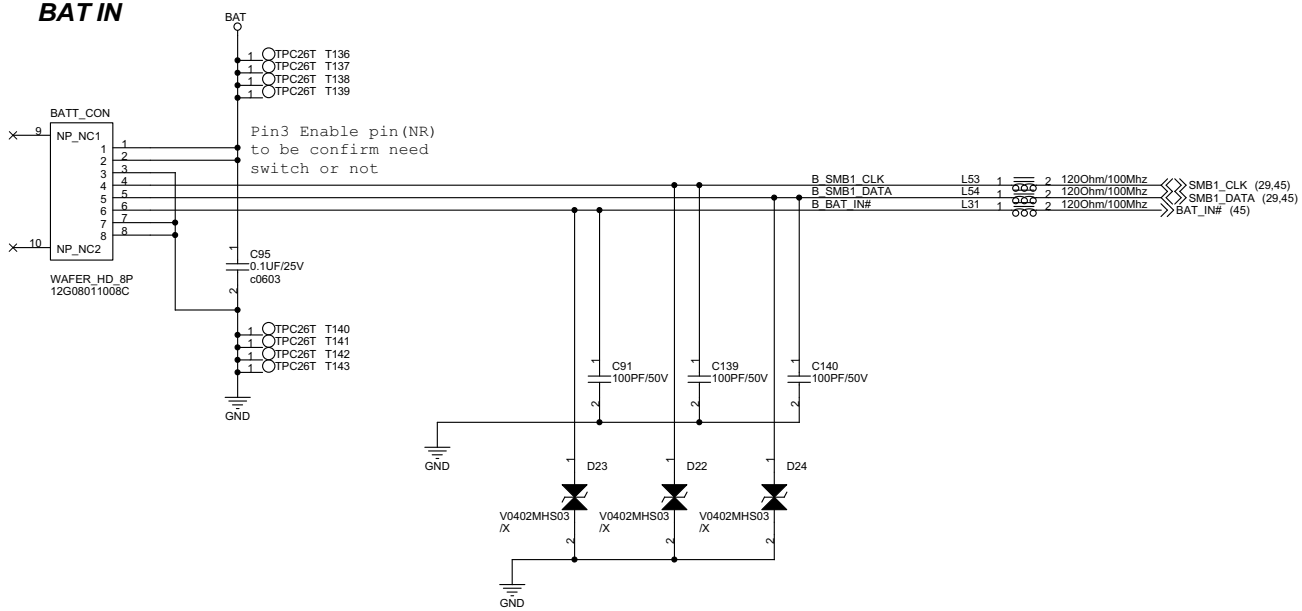
<Core Design>

ASUSTek Computer Inc.	Title : Discharge	
	Engineer: Kell_Huang	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 35 of 49	

DC IN

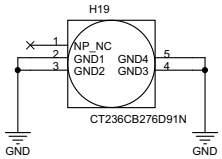


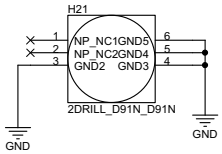
BAT IN

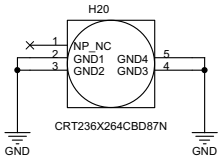


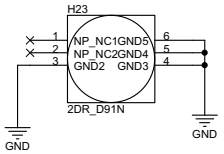
<Core Design>

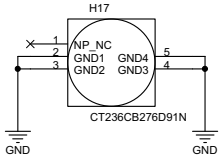
ASUSTek Computer Inc.	Title : PWR Jack	
	Engineer: Kell_Huang	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 36 of 49	



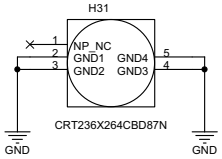








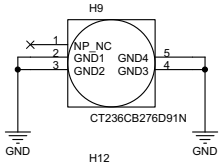
Top side :C size
Bottom side : E size

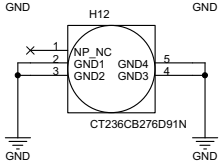


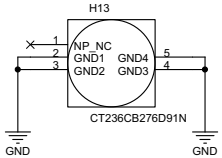
Top side : B size
Bottom side : E size

直徑2.3mm
Tooling hole

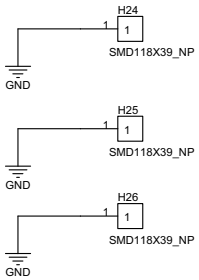
Top side : H size
Bottom side : E size



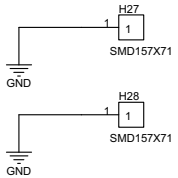




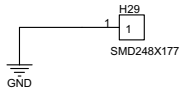
Top side : A size
Bottom side : E size



Size: I copper Pad



Size: F copper Pad



Size: J copper Pad

<Core Design>

ASUSTek Computer Inc.

Title : Srew Hole

Engineer: Kell_Huang

Size	Project Name	Rev
A3	MK90H	1.1G

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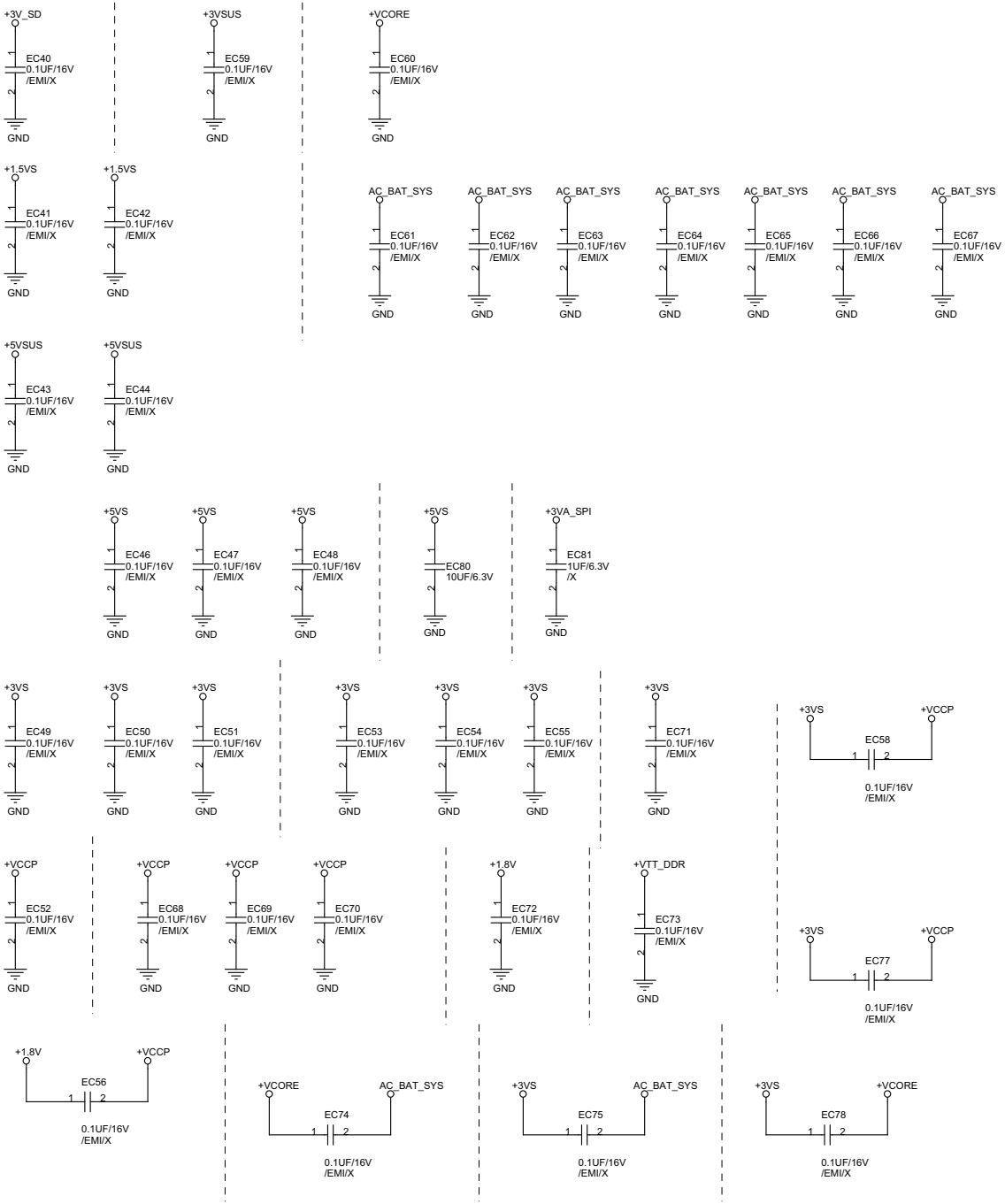
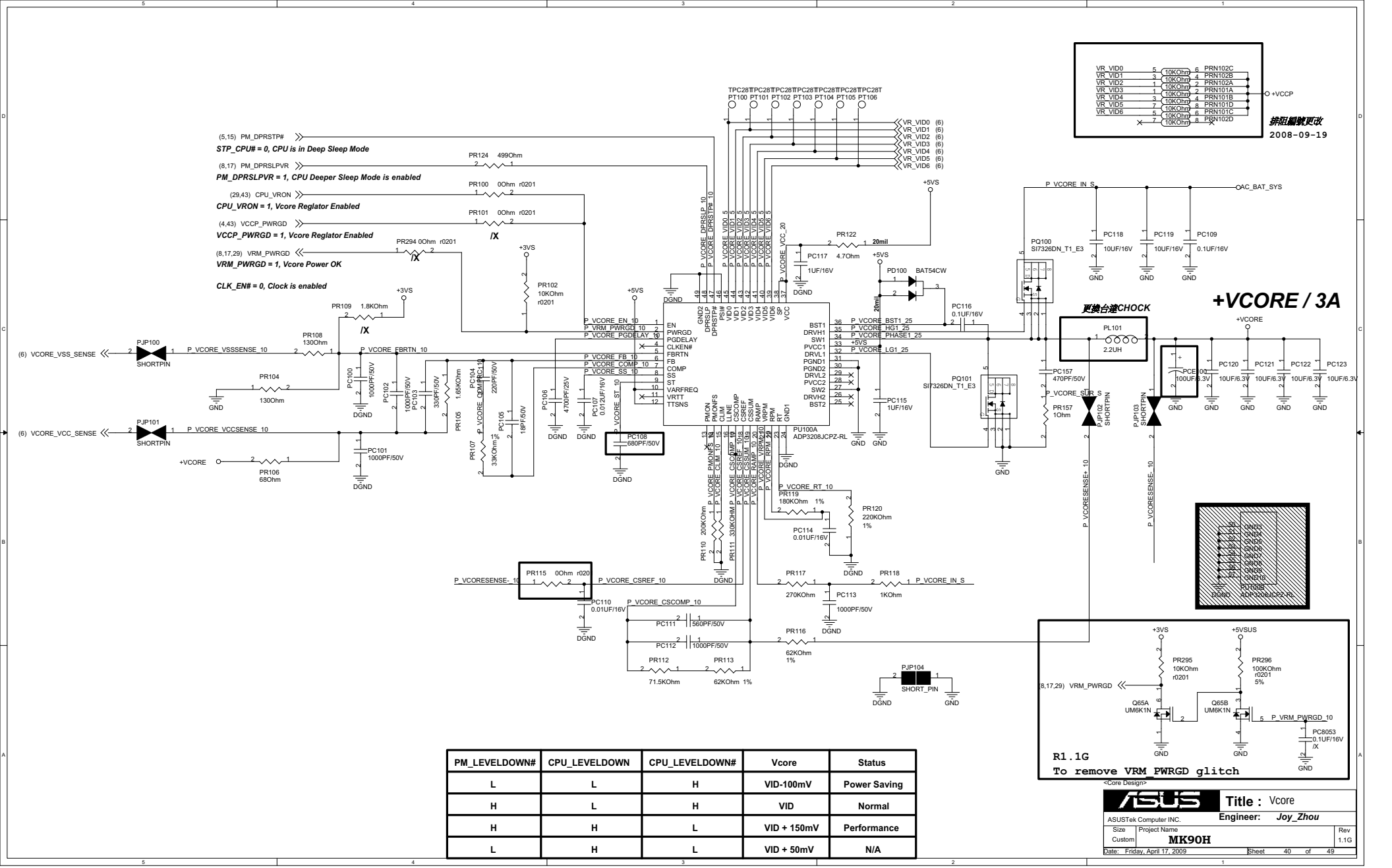
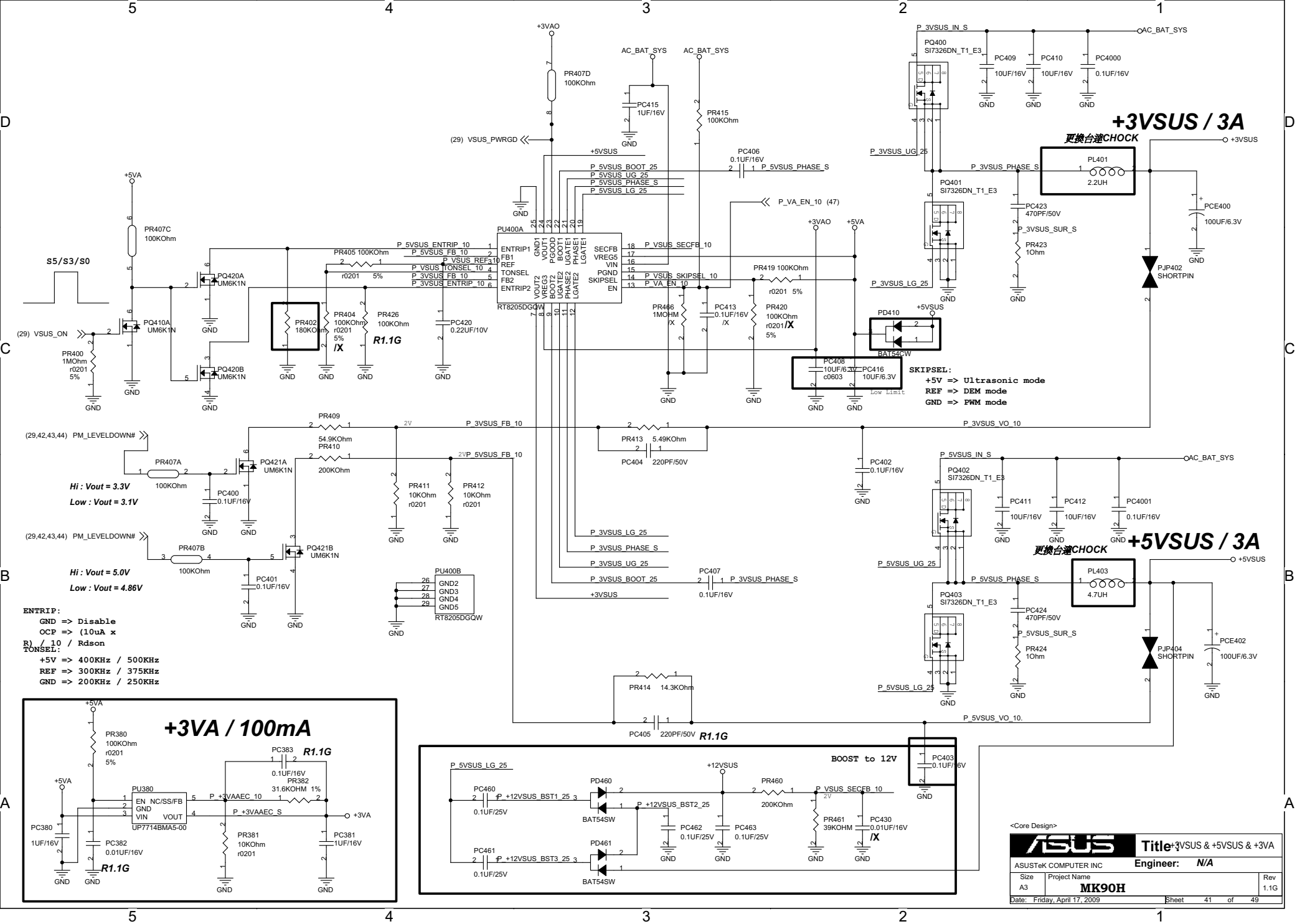


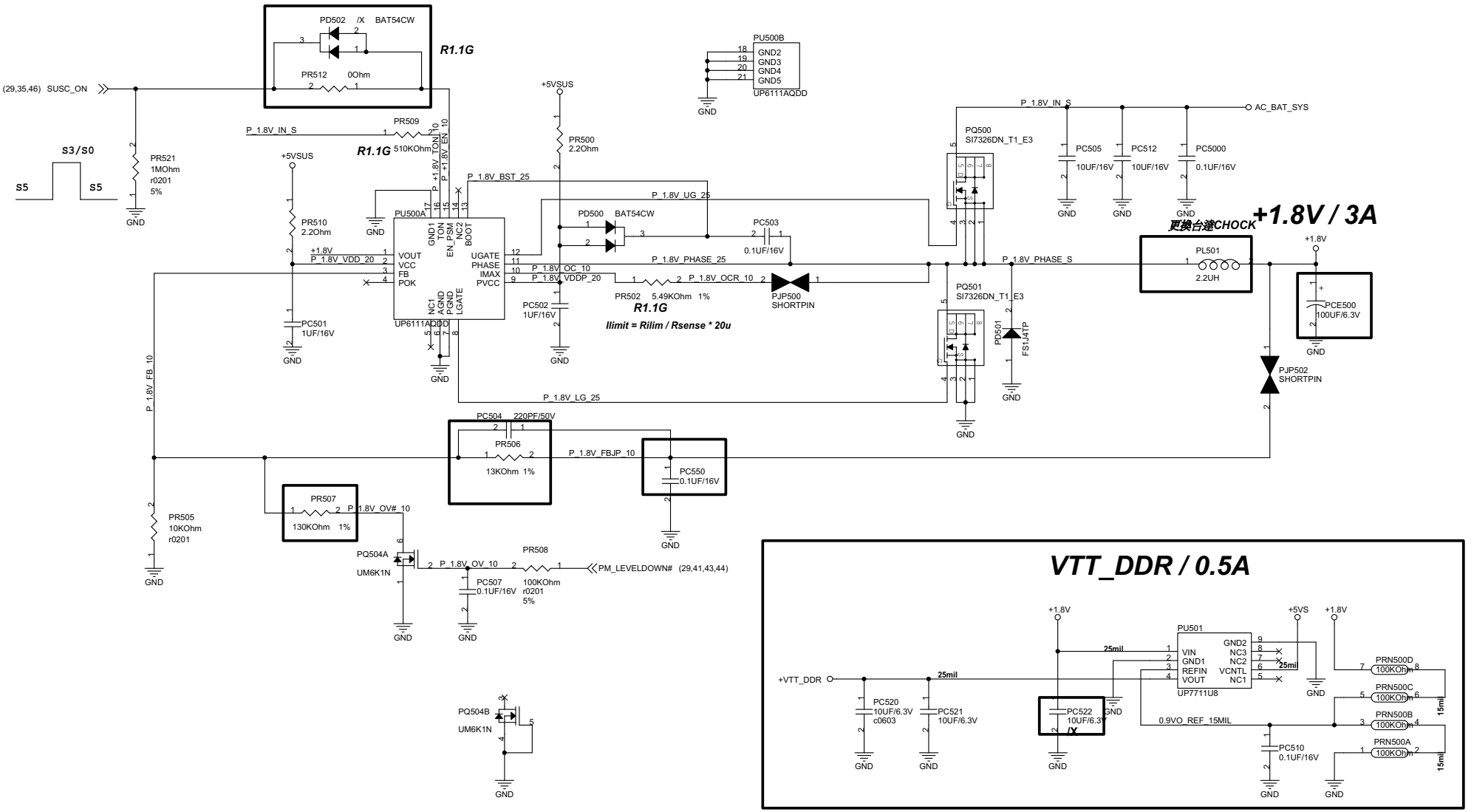
<Core Design>

ASUSTek Computer Inc.	Title : EMI	
	Engineer: Kell_Huang	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 38 of 49	



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 150mV	Performance
L	H	L	VID + 50mV	N/A





PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage
L	L	1.725V
H	L	1.8V
H	H	1.902V
L	H	1.827V

Only for 1.8V

PR506改13K(0402 1%)

PR507改130K(0402 1%)

PR514改95.3K(0402 1%)

<Core Design>

ASUSTek Computer INC.	Title : +1.8V & VTTDDR	
	Engineer: Joy_Zhou	
Size A3	Project Name MK90H	Rev 1.1G
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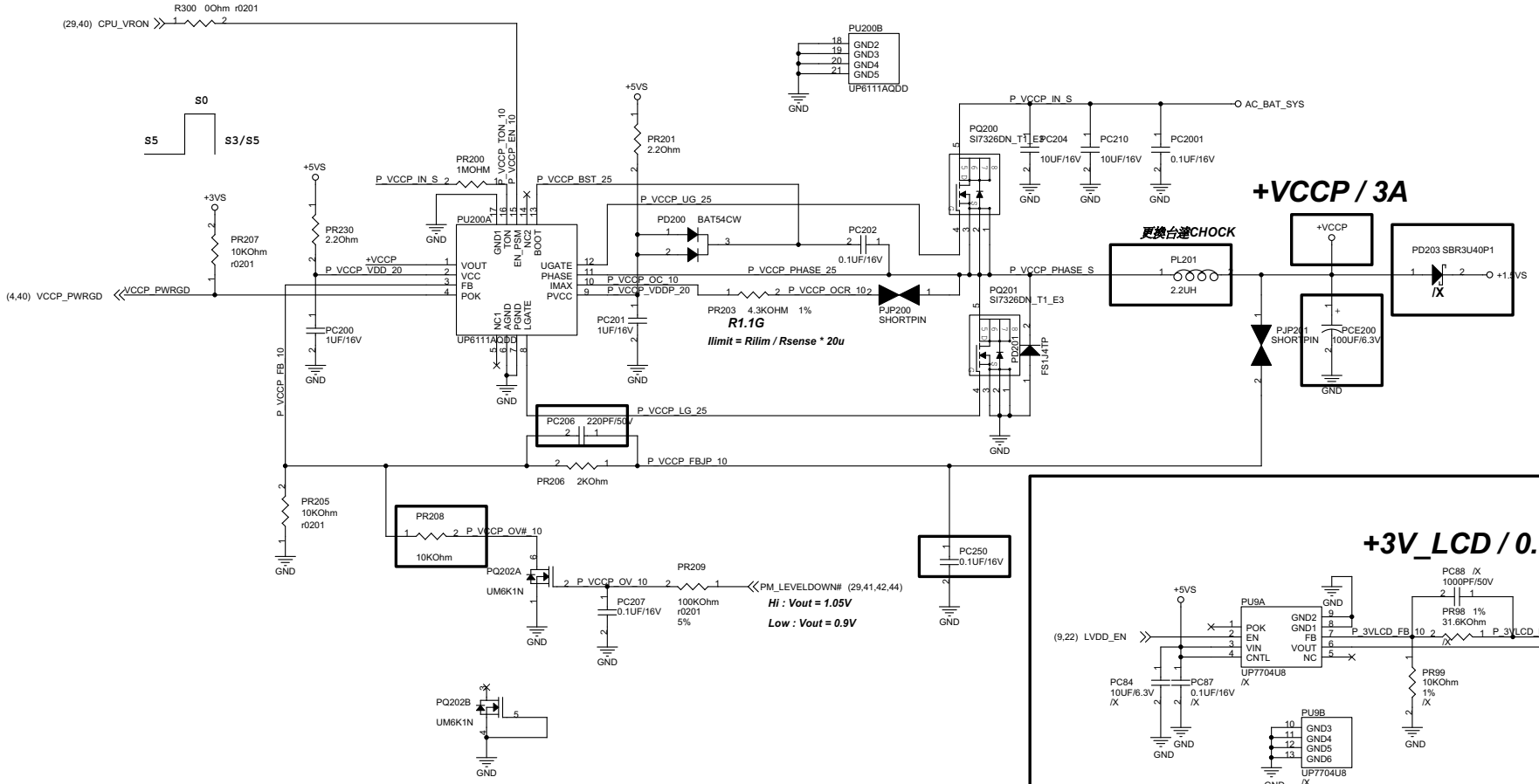
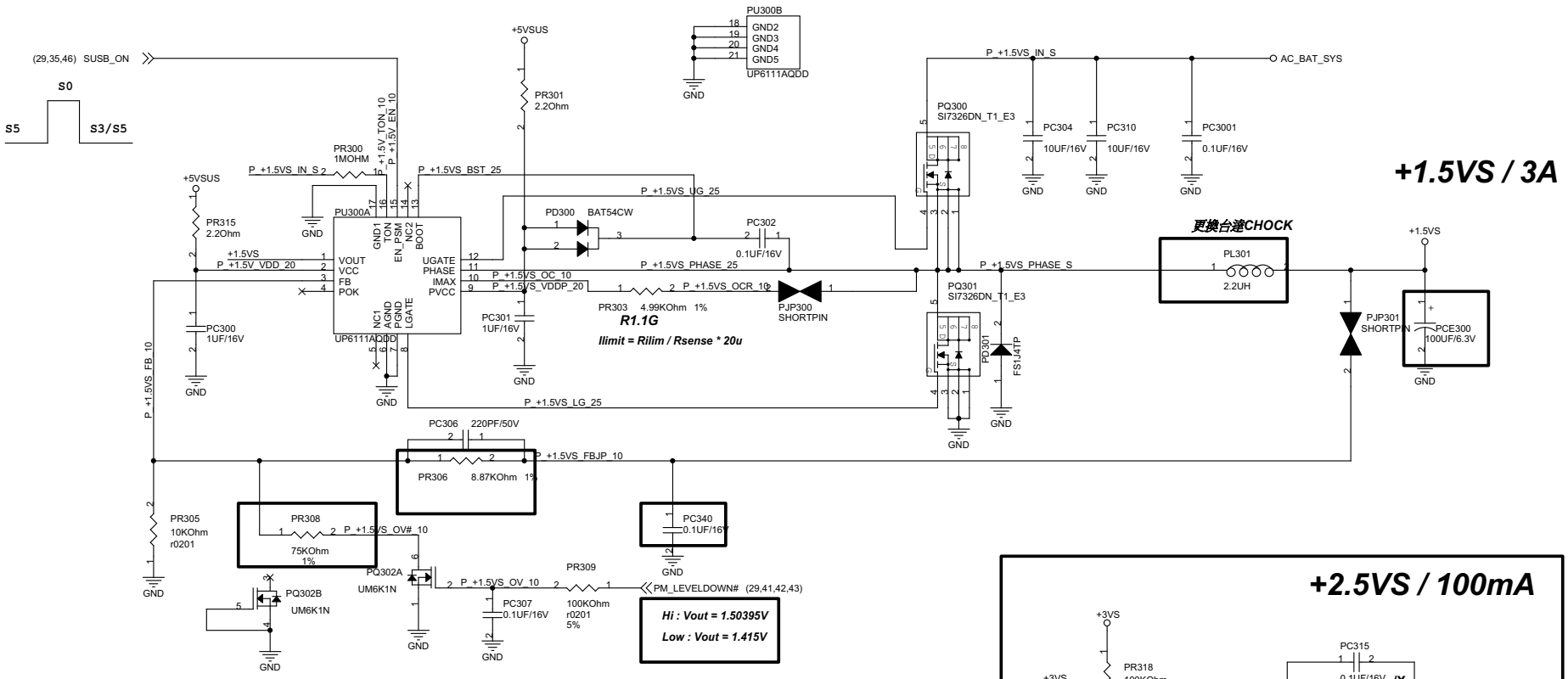
1.1G change Enable signal from CPU_VRON



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.9V	Power Saving
H	L	H	1.05V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

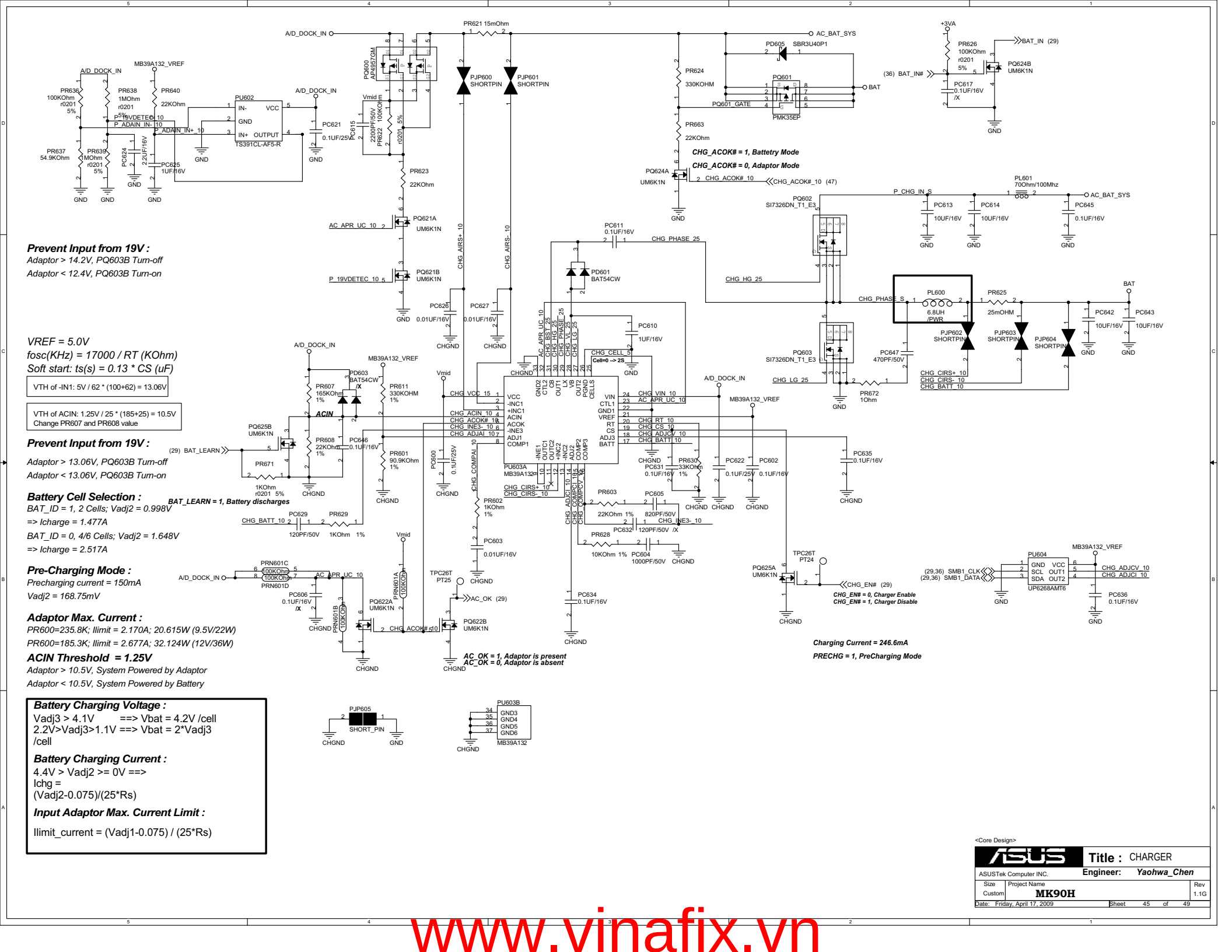
<Core Design>

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: Custom	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 43 of 49	



<Core Design>

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: MK90H	Rev: 1.1G
Date: Friday, April 17, 2009	Sheet 44 of 49	



<Core Design>
ASUSTek Computer INC.
Title : CHARGER
Engineer: Yaohwa_Chen
Size: Custom
Project Name: MK90H
Rev: 1.1G
Date: Friday, April 17, 2009
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