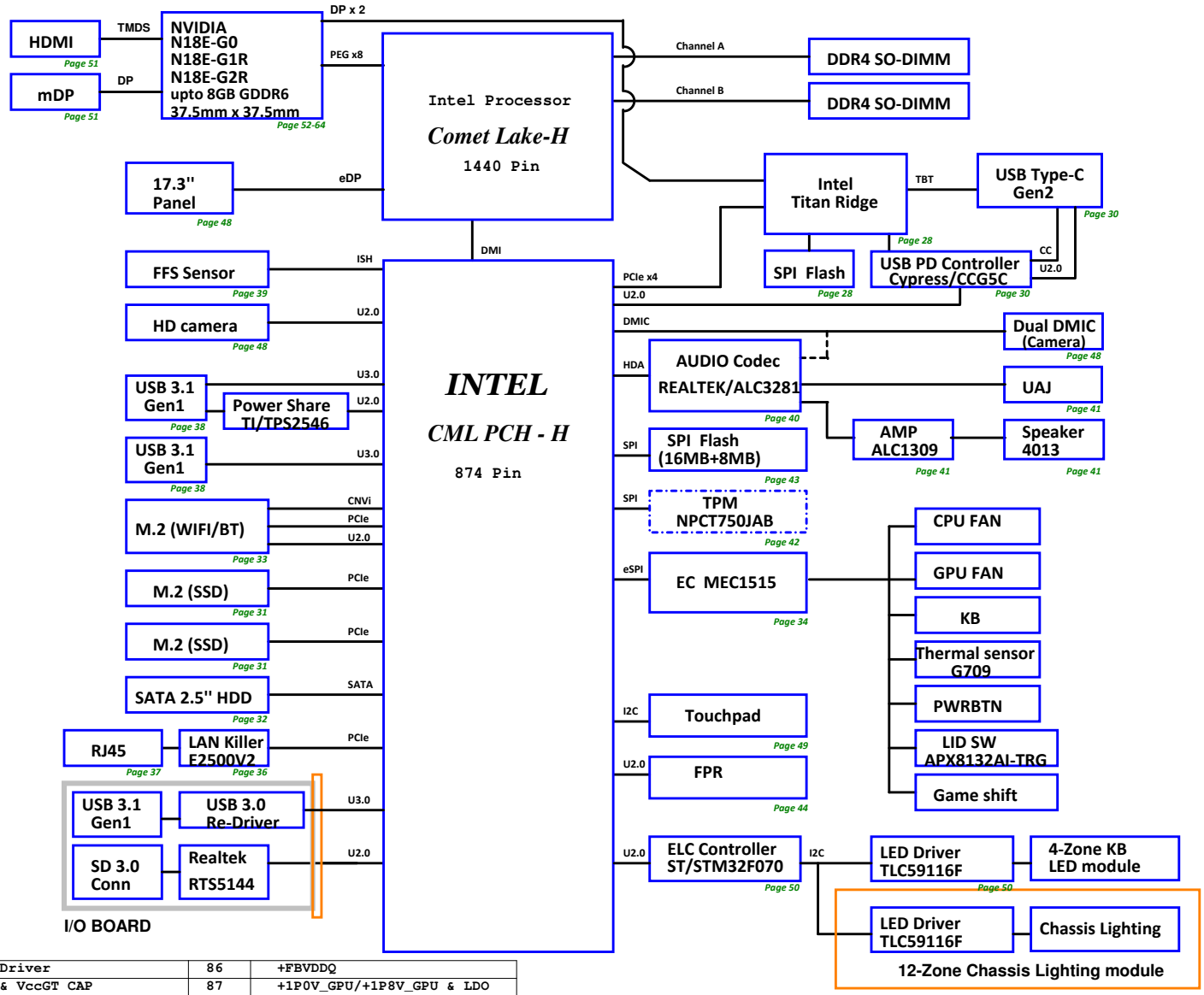
Hela (Comet Lake-H / N18E-RTX/GTX)



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02	SIGNAL & RESET MAP
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06	Power flow & sequence
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12	CPU MISC
13	CPU VSS
14	CPU POWER
15	CPU DECOUPLING
16	LCD_BIST/MB_BIST
17	DDR4_SO-DIMM0
18	DDR4_SO-DIMM1
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21	PCH SATA/PCIE
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26	PCH VCC
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29	
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38	USB CONN and power
39	SENSOR
40	AUDIO CODEC ALC3281
41	AMP ALC1309_AUDIO JACK
42	TPM
43	SM BUS & SPI ROM
44	Other Conn
45-46	ACAV_IN & XDP CONN
47	ME Screw
48	eDP Conn
49	Touch & Keyboard BL
50	ELC MCU
51	HDMI/mDP
52	GPU_PCIE
53	GPU-Xtal & Straps
54	GPU-BUFFER PARTITION A/B
55	GDDR6 256Mx2chx16bit _Ch_A
56	GDDR6 256Mx2chx16bit _Ch_B
57	GPU-BUFFER PARTITION C/D
58	GDDR6 256Mx2chx16bit _Ch_C
59	GDDR6 256Mx2chx16bit _Ch_D
60	GPU-MIO&IFPAB_DDI
61	GPU mini DP/HDMI/MUX
62	GPU-GPIO
63	GPU-POWER&GND
64	GPU-Decoupling
65	
66	GPU POWER DISCHARGE
67	GPU-POWER Sequence
68	DC_IN
69	Charger_ISL95522
70	VR CONTROLLER
71-72	Vcore Driver
73	VccGT Driver

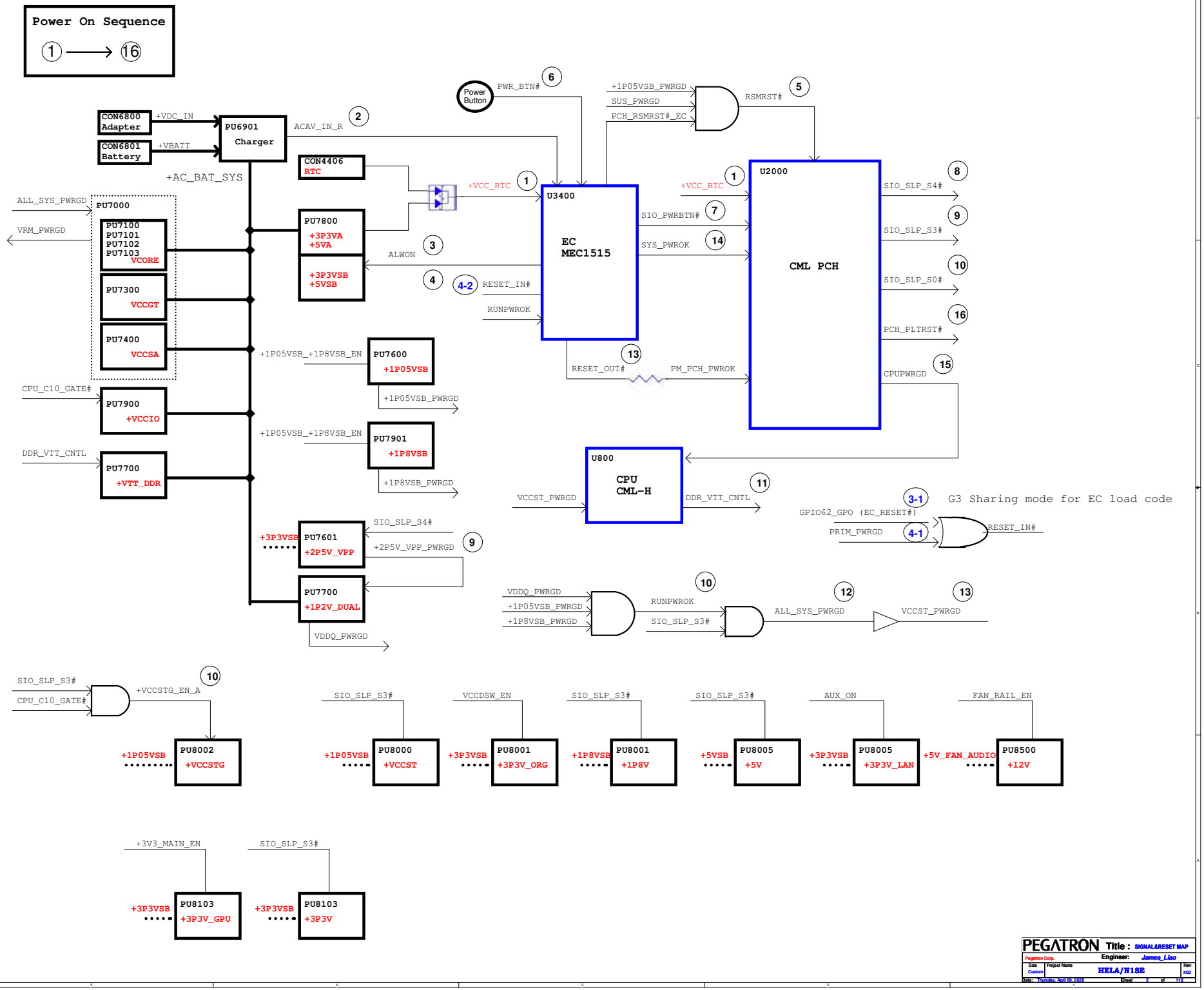
74	VccSA Driver	86	+FBVDDQ
75	Vcore & VccGT CAP	87	+1P0V_GPU/+1P8V_GPU & LDO
76	+1P05VSB/+2P5VPP	88	GPU_POWER_CAP
77	+1P2V_DUAL & +VTTDDR	89	
78	+3P3VSB / +5VSB	90	Power Sense
79	+VCCIO / +1P8V	91	
80-81	Load switch	92	POWER SENSE MAX34417
82	NVVDD CONTROLLER		
83-84	NVVDD Driver		
85	+12V		

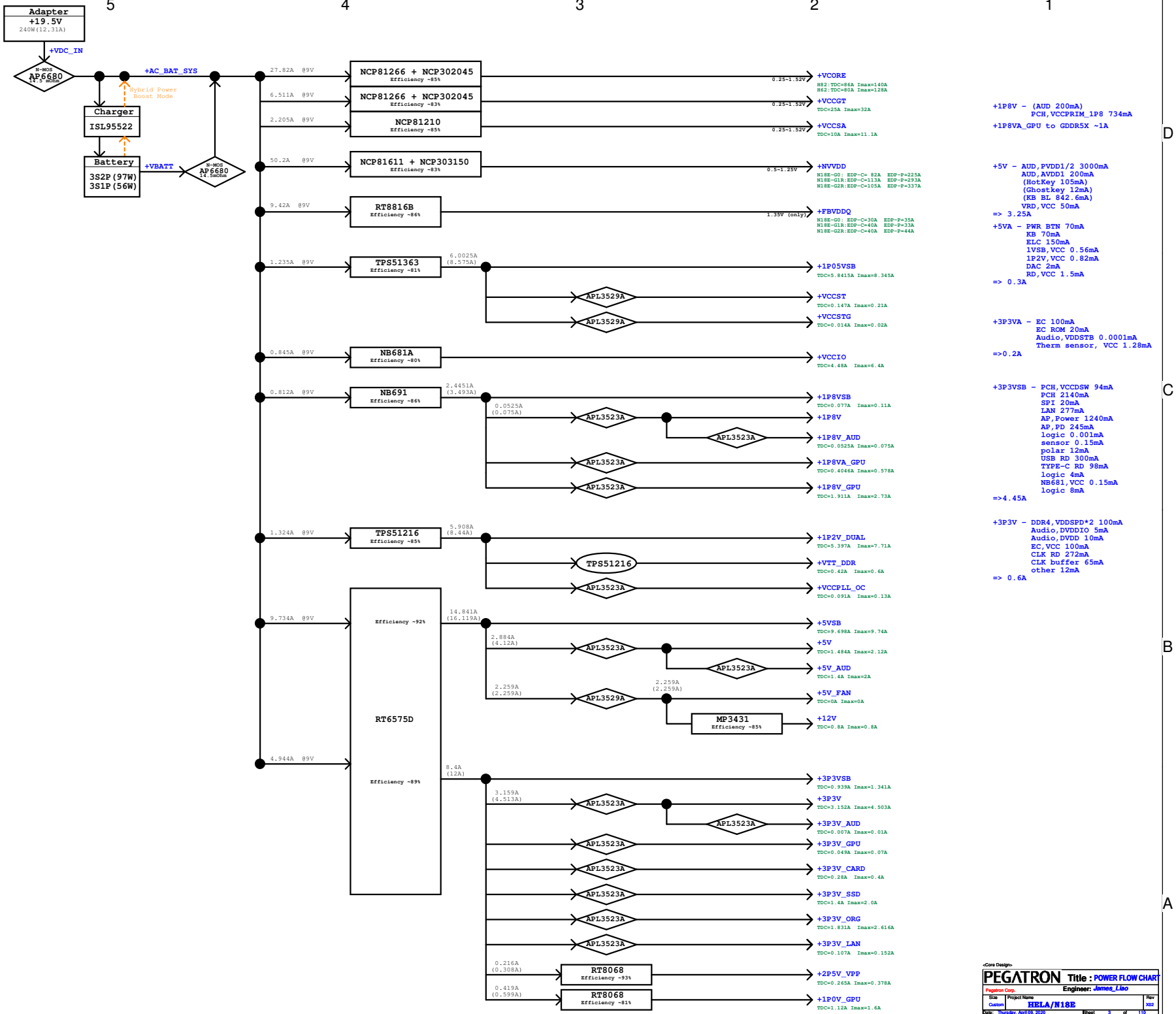
PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
C	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 1 of 110

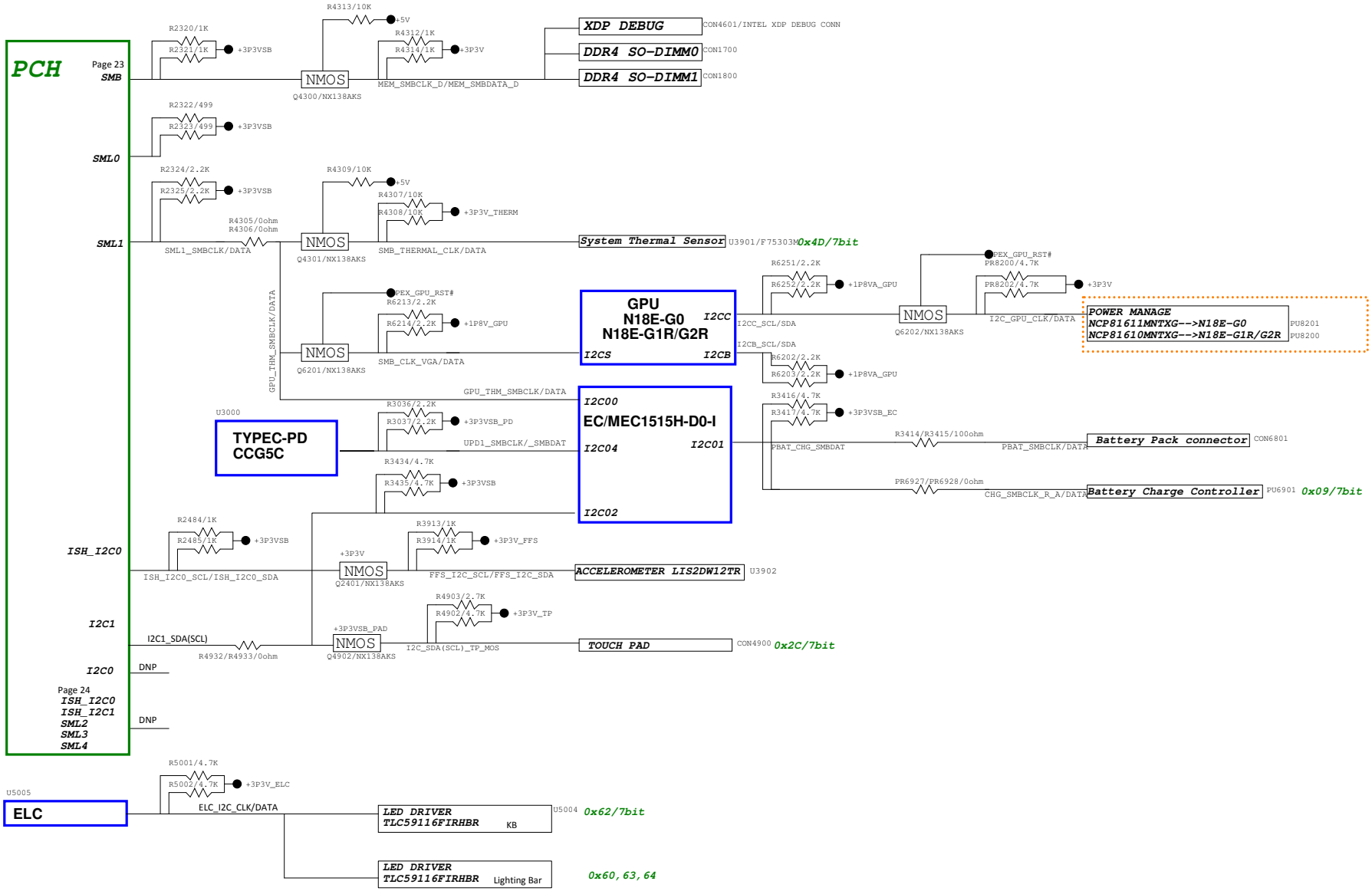

Power On Sequence
1 → 16
Power Button
PWR_BTN#
CON6800 Adapter
CON6801 Battery
+VDC_IN
+VBATT
PU6901 Charger
ACAV_IN_R
+AC_BAT_SYS
CON4406 RTC
+VCC_RTC
U3400
EC MEC1515
+1P05VSB_PWRGD
SUS_PWRGD
PCH_RSMRST#_EC
RSMRST#
U2000
CML PCH
SIO_SLP_S4#
SIO_SLP_S3#
SIO_SLP_S0#
PCH_PLTRST#
CPUPWRGD
SIO_PWRBTN#
SYS_PWROK
ALWON
RESET_IN#
RUNPWROK
RESET_OUT#
PM_PCH_PWROK
ALL_SYS_PWRGD
VRM_PWRGD
PU7000
PU7100
PU7101
PU7102
PU7103
VCORE
PU7300
VCCGT
PU7400
VCCSA
PU7800
+3P3VA
+5VA
+3P3VSB
+5VSB
+1P05VSB_+1P8VSB_EN
PU7600
+1P05VSB
+1P05VSB_PWRGD
PU7901
+1P8VSB
+1P8VSB_PWRGD
CPU_C10_GATE#
PU7900
+VCCIO
DDR_VTT_CNTL
PU7700
+VTT_DDR
U800
CPU CML-H
VCCST_PWRGD
DDR_VTT_CNTL
GPIO62_GPO (EC_RESET#)
PRIM_PWRGD
RESET_IN#
G3 Sharing mode for EC load code
PU7601
+2P5V_VPP
+2P5V_VPP_PWRGD
PU7700
+1P2V_DUAL
VDDQ_PWRGD
VDDQ_PWRGD
+1P05VSB_PWRGD
+1P8VSB_PWRGD
RUNPWROK
SIO_SLP_S3#
ALL_SYS_PWRGD
VCCST_PWRGD
SIO_SLP_S3#
CPU_C10_GATE#
+VCCSTG_EN_A
PU8002
+1P05VSB
+VCCSTG
SIO_SLP_S3#
PU8000
+1P05VSB
+VCCST
VCCDSW_EN
SIO_SLP_S3#
PU8001
+3P3VSB
+3P3V_ORG
SIO_SLP_S3#
PU8001
+1P8VSB
+1P8V
SIO_SLP_S3#
PU8005
+5VSB
+5V
AUX_ON
PU8005
+3P3VSB
+3P3V_LAN
FAN_RAIL_EN
PU8500
+5V_FAN_AUDIO
+12V
+3V3_MAIN_EN
PU8103
+3P3VSB
+3P3V_GPU
SIO_SLP_S3#
PU8103
+3P3VSB
+3P3V
PEGATRON
Title : SIGNAL&RESET MAP
Engineer: James_Liao
HELA/N18E


Adapter
+19.5V
240W(12.31A)
+VDC_IN
N-MOS
AP6680
13.5 mOhm
+AC_BAT_SYS
Hybrid Power
Boost Mode
Charger
ISL95522
Battery
3S2P(97W)
3S1P(56W)
+VBATT
N-MOS
AP6680
13.5mOhm
27.82A @9V
NCP81266 + NCP302045
Efficiency ~85%
+VCORE
0.25~1.52V
H82:TDC=86A Imax=140A
H62:TDC=80A Imax=128A
6.511A @9V
NCP81266 + NCP302045
Efficiency ~83%
+VCCGT
0.25~1.52V
TDC=25A Imax=32A
2.205A @9V
NCP81210
Efficiency ~85%
+VCCSA
0.25~1.52V
TDC=10A Imax=11.1A
50.2A @9V
NCP81611 + NCP303150
Efficiency ~83%
+NVVDD
0.5~1.25V
N18E-G0: EDP-C= 82A EDP-P=225A
N18E-G1R:EDP-C=113A EDP-P=293A
N18E-G2R:EDP-C=105A EDP-P=337A
9.42A @9V
RT8816B
Efficiency ~86%
+FBVDDQ
1.35V (only)
N18E-G0: EDP-C=30A EDP-P=35A
N18E-G1R:EDP-C=40A EDP-P=33A
N18E-G2R:EDP-C=40A EDP-P=44A
1.235A @9V
TPS51363
Efficiency ~81%
6.0025A
(8.575A)
+1P05VSB
TDC=5.8415A Imax=8.345A
APL3529A
+VCCST
TDC=0.147A Imax=0.21A
APL3529A
+VCCSTG
TDC=0.014A Imax=0.02A
0.845A @9V
NB681A
Efficiency ~80%
+VCCIO
TDC=4.48A Imax=6.4A
0.812A @9V
NB691
Efficiency ~86%
2.4451A
(3.493A)
+1P8VSB
TDC=0.077A Imax=0.11A
0.0525A
(0.075A)
APL3523A
+1P8V
APL3523A
+1P8V_AUD
TDC=0.0525A Imax=0.075A
APL3523A
+1P8VA_GPU
TDC=0.4046A Imax=0.578A
APL3523A
+1P8V_GPU
TDC=1.911A Imax=2.73A
1.324A @9V
TPS51216
Efficiency ~85%
5.908A
(8.44A)
+1P2V_DUAL
TDC=5.397A Imax=7.71A
TPS51216
+VTT_DDR
TDC=0.42A Imax=0.6A
APL3523A
+VCCPLL_OC
TDC=0.091A Imax=0.13A
9.734A @9V
Efficiency ~92%
14.841A
(16.119A)
+5VSB
TDC=9.698A Imax=9.74A
2.884A
(4.12A)
APL3523A
+5V
TDC=1.484A Imax=2.12A
APL3523A
+5V_AUD
TDC=1.4A Imax=2A
2.259A
(2.259A)
2.259A
(2.259A)
APL3529A
+5V_FAN
TDC=0A Imax=0A
MP3431
Efficiency ~85%
+12V
TDC=0.8A Imax=0.8A
RT6575D
4.944A @9V
Efficiency ~89%
8.4A
(12A)
+3P3VSB
TDC=0.939A Imax=1.341A
3.159A
(4.513A)
APL3523A
+3P3V
TDC=3.152A Imax=4.503A
APL3523A
+3P3V_AUD
TDC=0.007A Imax=0.01A
APL3523A
+3P3V_GPU
TDC=0.049A Imax=0.07A
APL3523A
+3P3V_CARD
TDC=0.28A Imax=0.4A
APL3523A
+3P3V_SSD
TDC=1.4A Imax=2.0A
APL3523A
+3P3V_ORG
TDC=1.831A Imax=2.616A
APL3523A
+3P3V_LAN
TDC=0.107A Imax=0.152A
0.216A
(0.308A)
RT8068
Efficiency ~93%
+2P5V_VPP
TDC=0.265A Imax=0.378A
0.419A
(0.599A)
RT8068
Efficiency ~81%
+1P0V_GPU
TDC=1.12A Imax=1.6A
+1P8V - (AUD 200mA)
PCH,VCCPRIM_1P8 734mA
+1P8VA_GPU to GDDR5X ~1A
+5V - AUD,PVDD1/2 3000mA
AUD,AVDD1 200mA
(HotKey 105mA)
(Ghostkey 12mA)
(KB BL 842.6mA)
VRD,VCC 50mA
=> 3.25A
+5VA - PWR BTN 70mA
KB 70mA
ELC 150mA
1VSB,VCC 0.56mA
1P2V,VCC 0.82mA
DAC 2mA
RD,VCC 1.5mA
=> 0.3A
+3P3VA - EC 100mA
EC ROM 20mA
Audio,VDDSTB 0.0001mA
Therm sensor, VCC 1.28mA
=>0.2A
+3P3VSB - PCH,VCCDSW 94mA
PCH 2140mA
SPI 20mA
LAN 277mA
AP,Power 1240mA
AP,PD 245mA
logic 0.001mA
sensor 0.15mA
polar 12mA
USB RD 300mA
TYPE-C RD 98mA
logic 4mA
NB681,VCC 0.15mA
logic 8mA
=>4.45A
+3P3V - DDR4,VDDSPD*2 100mA
Audio,DVDDIO 5mA
Audio,DVDD 10mA
EC,VCC 100mA
CLK RD 272mA
CLK buffer 65mA
other 12mA
=> 0.6A
<Core Design>
PEGATRON
Title : POWER FLOW CHART
Pegatron Corp.
Engineer: James_Liao
Size
Custom
Project Name
HELA/N18E
Rev
X02
Date: Thursday, April 09, 2020
Sheet 3 of 110

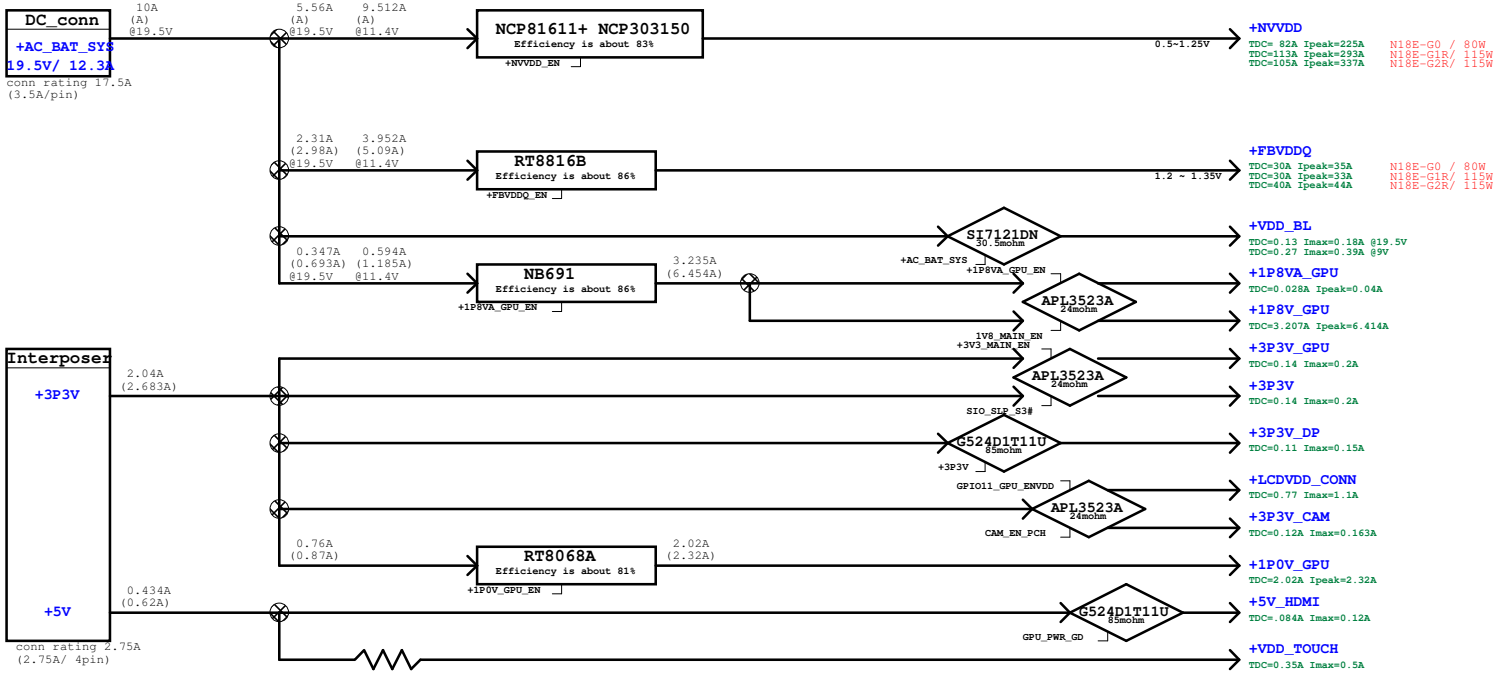
Schematics Change History

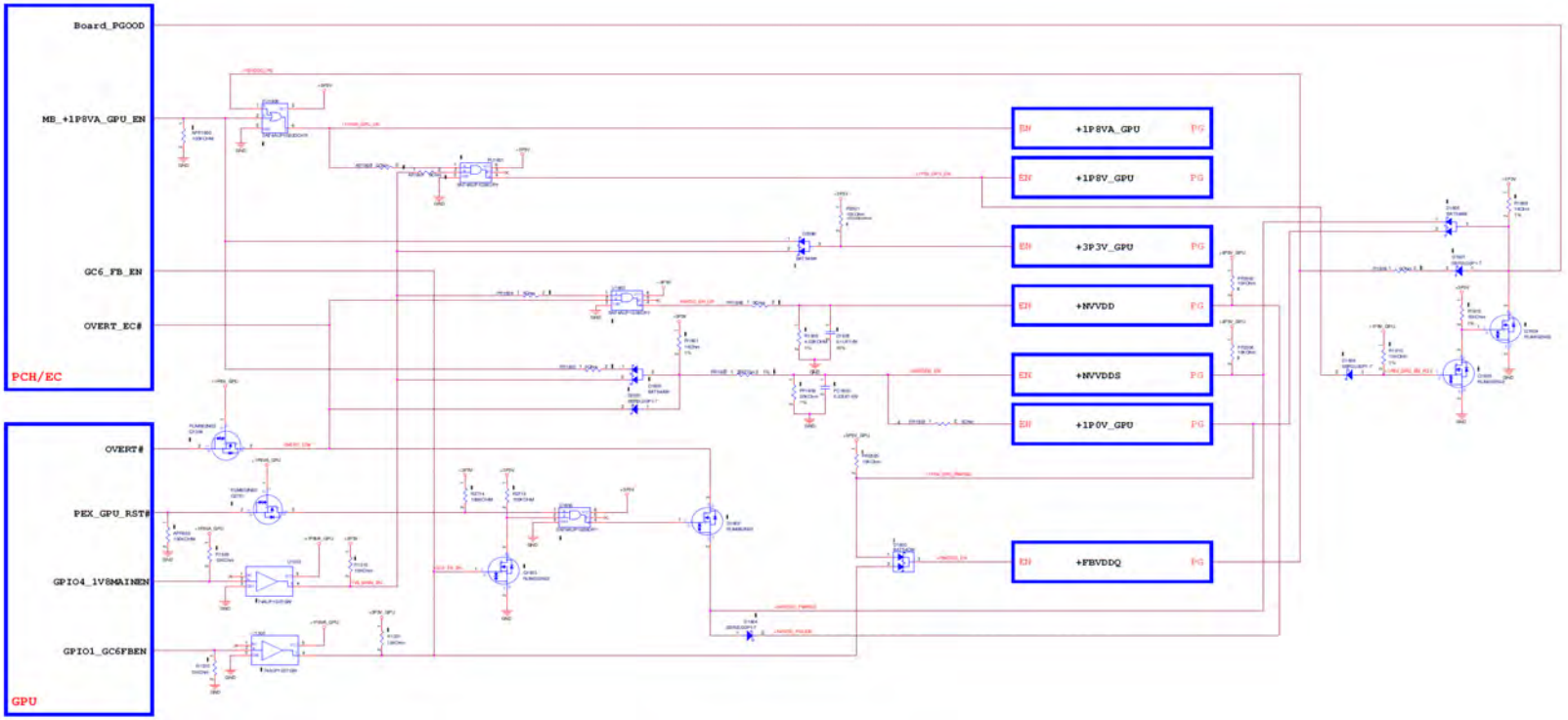
Version	Date	Description	Comments
1.00			

SMBUS & I2C Block Diagram



PEGATRON Title : SMBus & I2C Flow
Engineer: Jiamin_Liao
HKLA/H18R





<Core Design>

PEGATRON Title : GPU Power flow & sequence

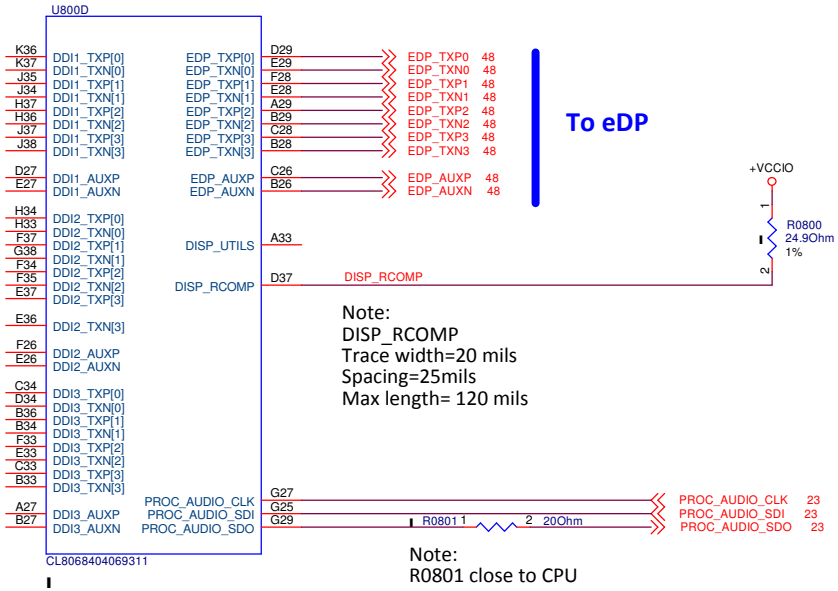
Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A2	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 6 of 119

Reserved Page

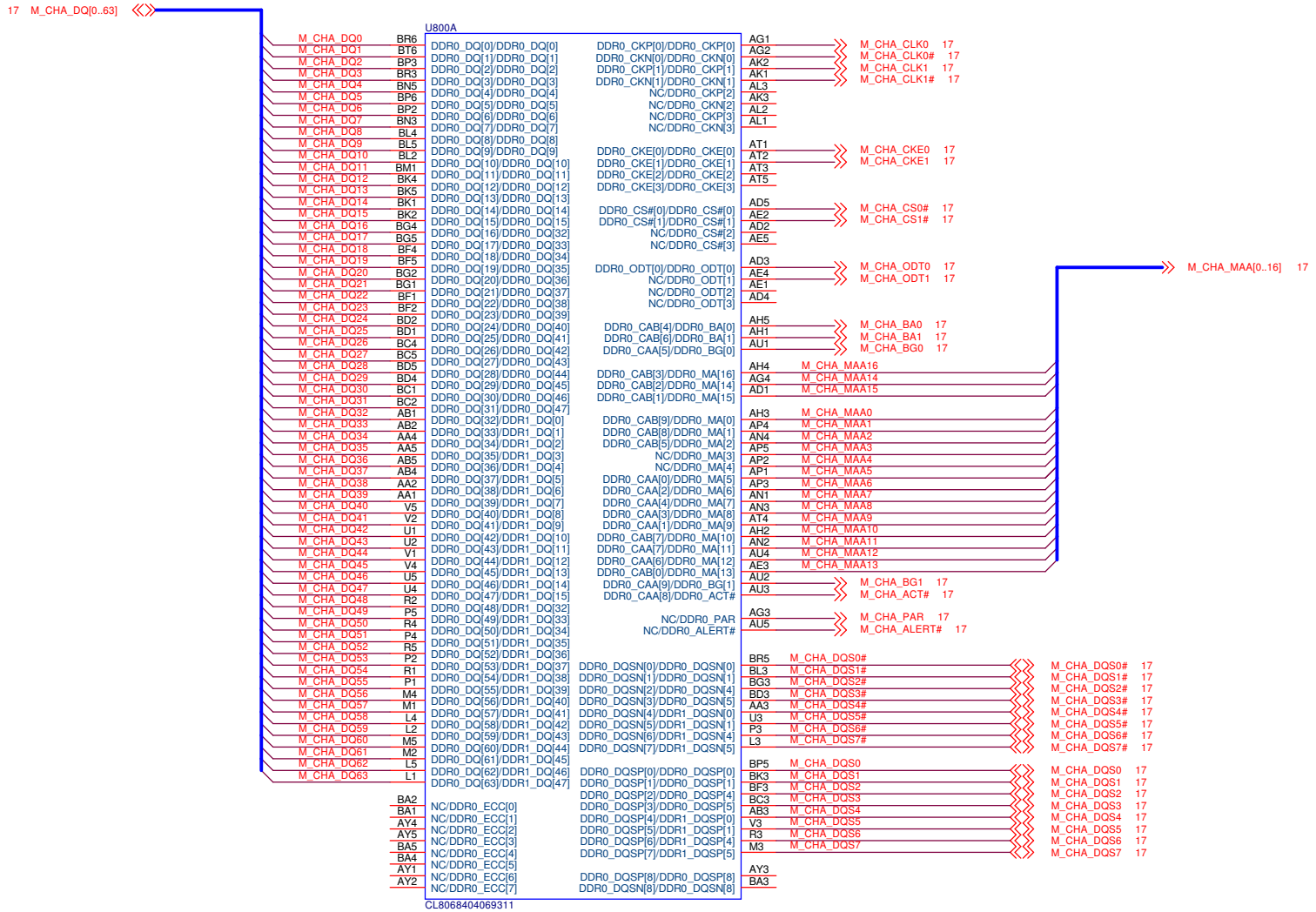
08.CPU DDI/EDP



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU DDI/EDP	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 8 of 110	

09.CPU DDR4 CHA



PEGATRON DT-MB RESTRICTED SECRET

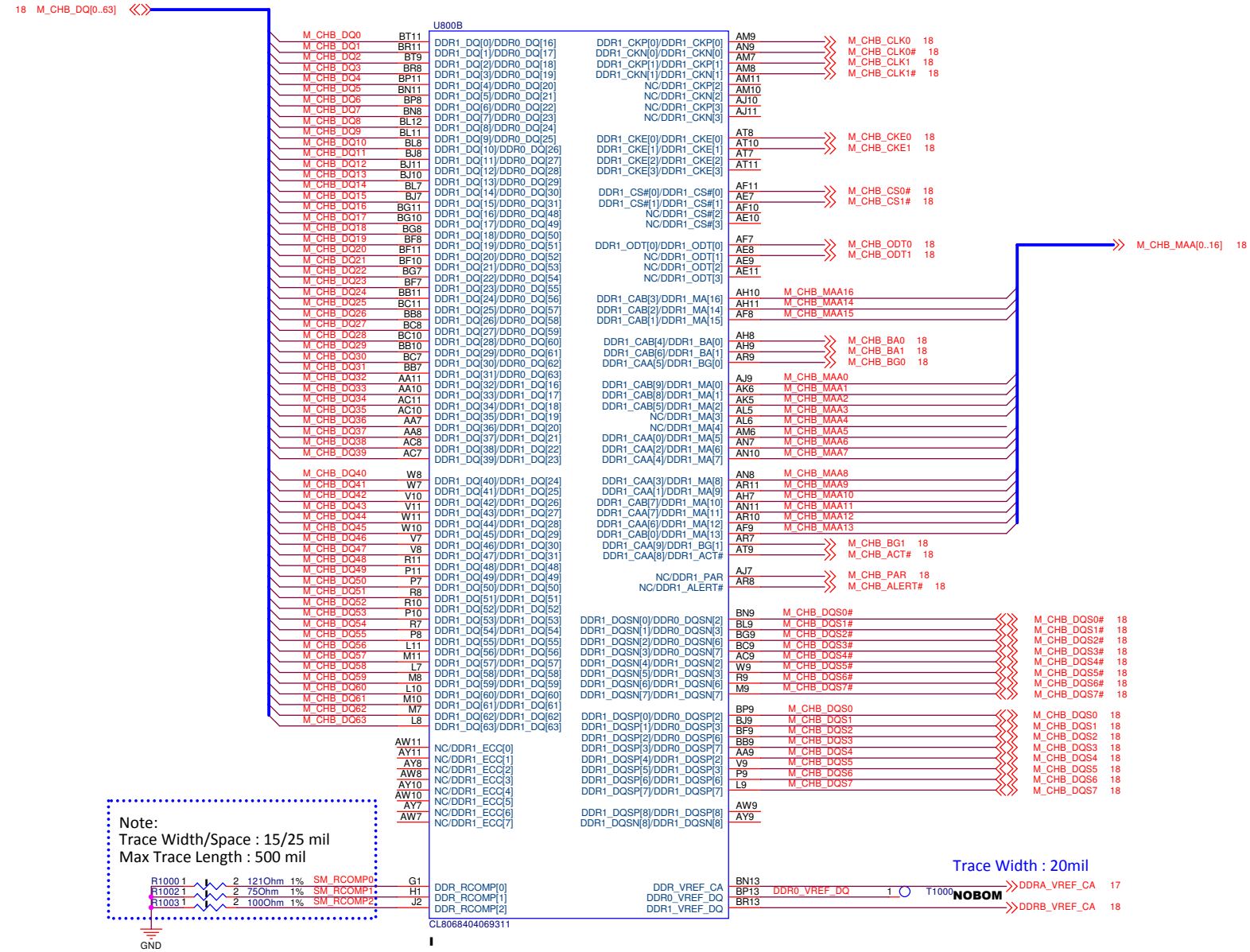
PEGATRON Title : CPU DDR4 CHA

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A3	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 9 of 110

10.CPU DDR4 CHB



Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max Length (mils)			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group [1]/[2]	Byte [1]/[2]	Region	Breakout [1,2]	Total		
RCOMP [0]	M	MS	VSS	2	12-15					20	25/25				500	121	
RCOMP [1]	M	MS	VSS	2	12-15					20	25/25				500	75	
RCOMP [2]	M	MS	VSS	2	12-15					20	25/25				500	100	

PEGATRON DT-MB RESTRICTED SECRET

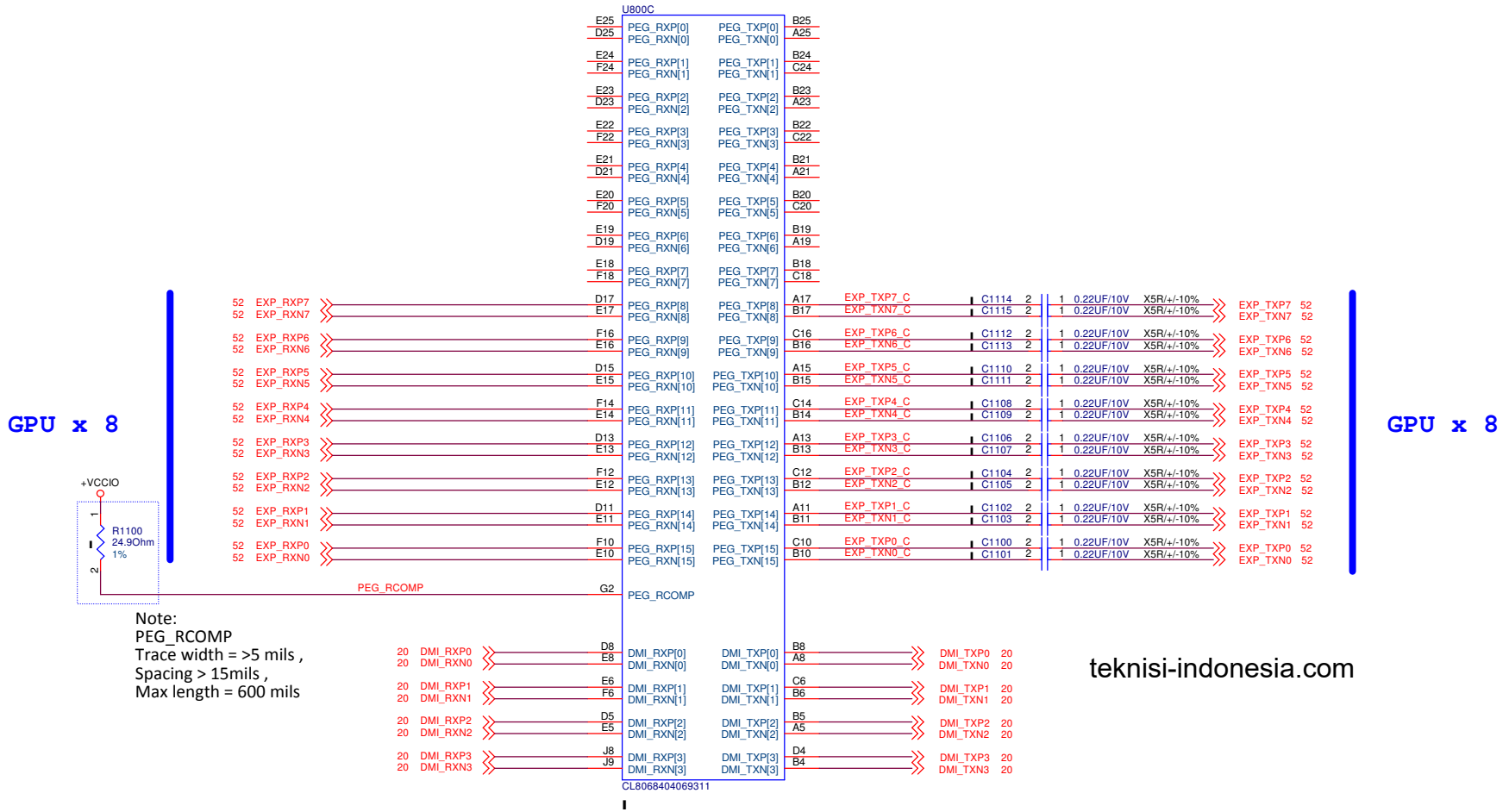
PEGATRON Title : CPU DDR4 CHB

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A3	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 10 of 110

11.CPU PEG/DMI



Note:
PEG_RCOMP
Trace width = >5 mils ,
Spacing > 15mils ,
Max length = 600 mils

PEGATRON	Title : CPU PEG/DMI	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 11 of 110	

12.CPU MISC

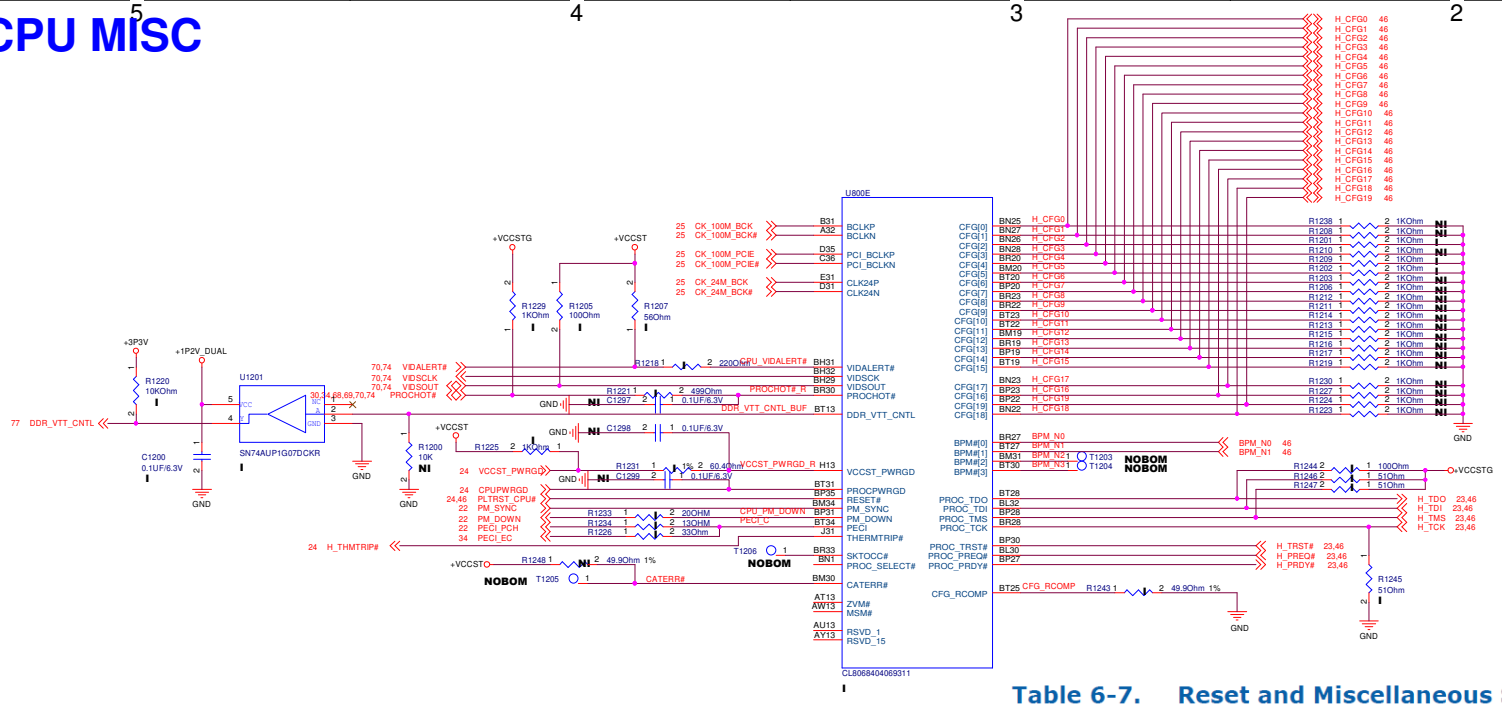


Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.

Table 6-10. Processor Clocking Signals

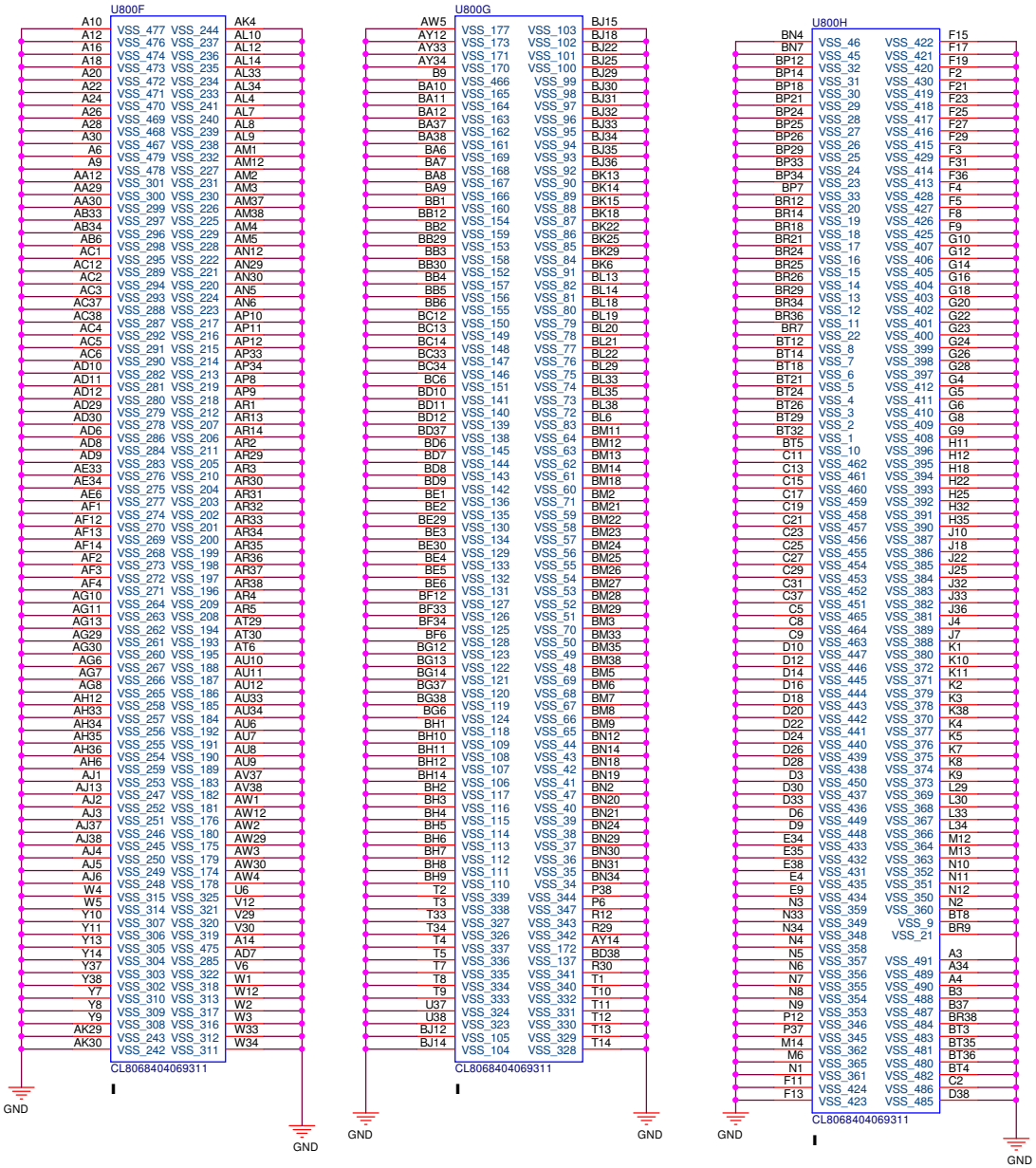
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

Table 51-39. Processor/PCH Strapping Checklist (Sheet 2 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			

PEGATRON Title : CPU MISC
Pegatron Corp. Engineer: James_Liao
Size A2 | Project Name HELA/N18E | Rev X02
Date: Thursday, April 09, 2020 Sheet 12 of 110

13.CPU VSS



PEGATRON DT-MB RESTRICTED SECRET

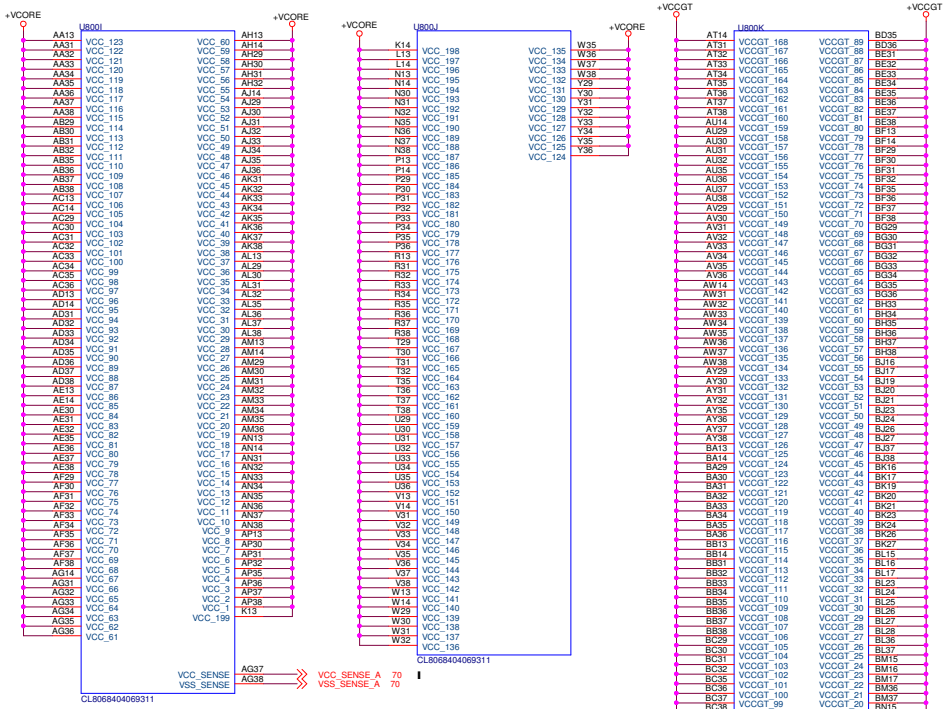
PEGATRON Title : CPU VSS

Pegatron Corp. Engineer: James_Liao

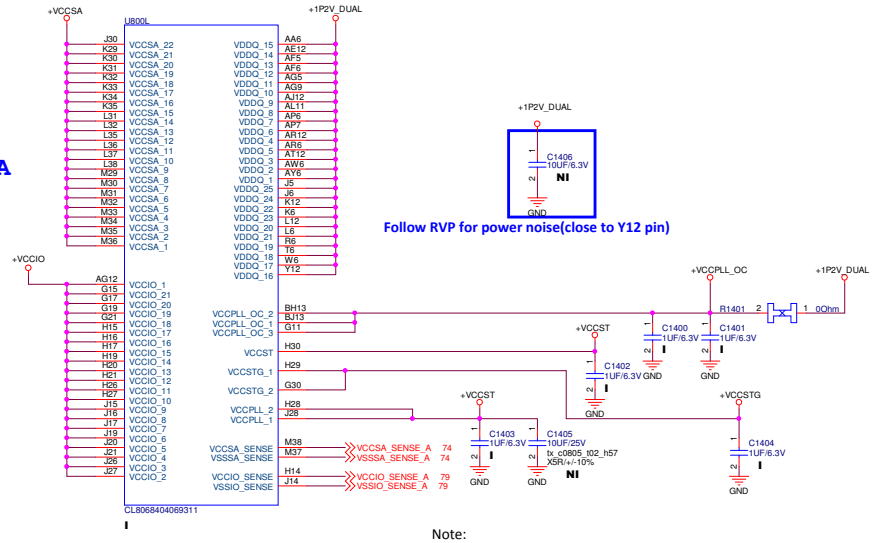
Size	Project Name	Rev
Custom	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 13 of 110

14.CPU POWER



+Vcore Max 140A
+Vccgt Max 32A
+Vccsa Max 11.1A



Note:

1. VCCSA_SENSE / VSSSA_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7423 / PR7424 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCSA_SENSE / VSSSA_SENSE line resistance.

Note:

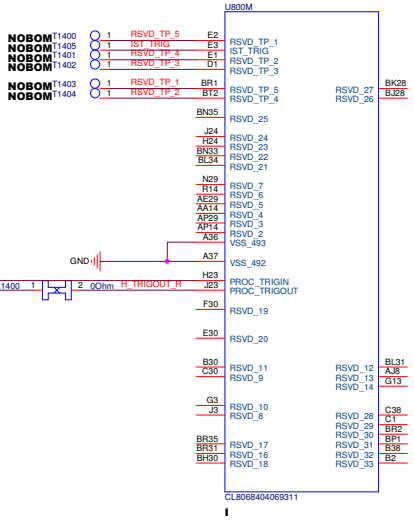
1. VCCIO_SENSE / VSSIO_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7906 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCIO_SENSE / VSSIO_SENSE line resistance.

Note:

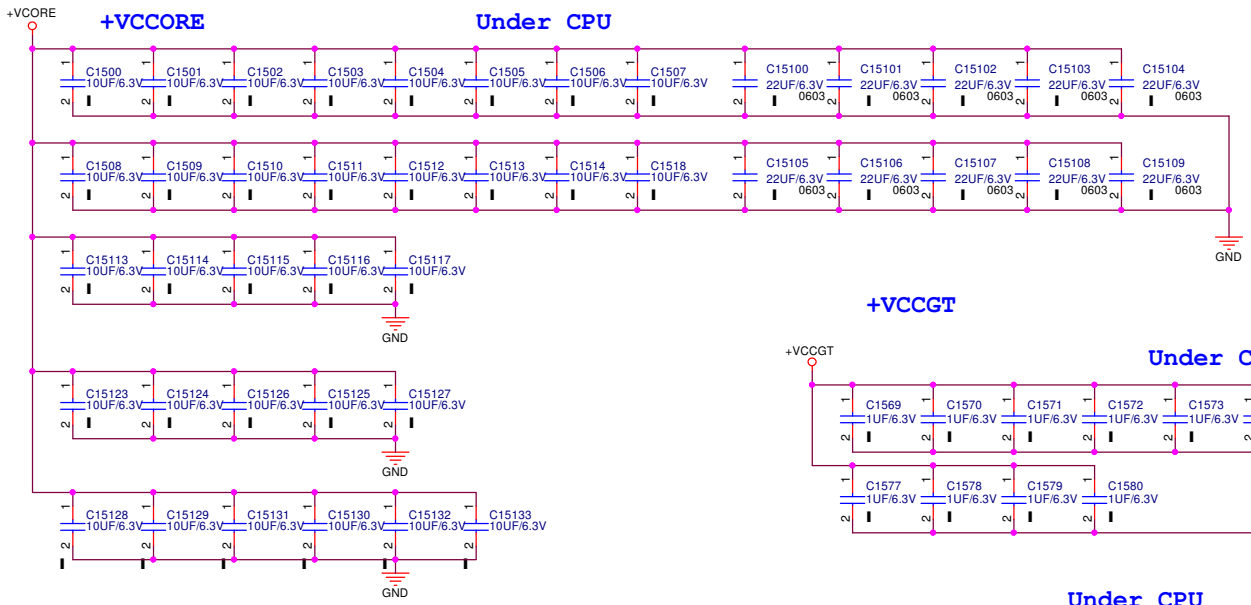
1. VCC_SENSE / VSS_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7038 / PR7043 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCC_SENSE / VSS_SENSE line resistance.

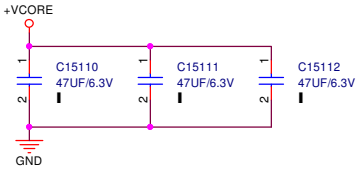
Note:

1. VSSGT_SENSE / VCCGT_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7059 / PR7067 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VSSGT_SENSE / VCCGT_SENSE line resistance.



15.CPU DECOUPLING





+VCCGT

+VCCGT
1UF*12

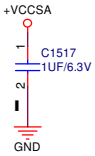
Table 326. CML H 8+2 Processor Decoupling Requirements

Domain	Board Edge cap	Backside cap	Notes
Vcc	20x 47uF 0805		
		13x 47uF 0603	
		32x 10uF 0402	
		45x 1uF 0201/0402	
		24x 0201/0402 (placeholder)	
VccGT	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201/0402	
VccSA	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201/0402	
VDDQ		4x 22uF 0603	
		11x 10uF 0402	
VccIO		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.

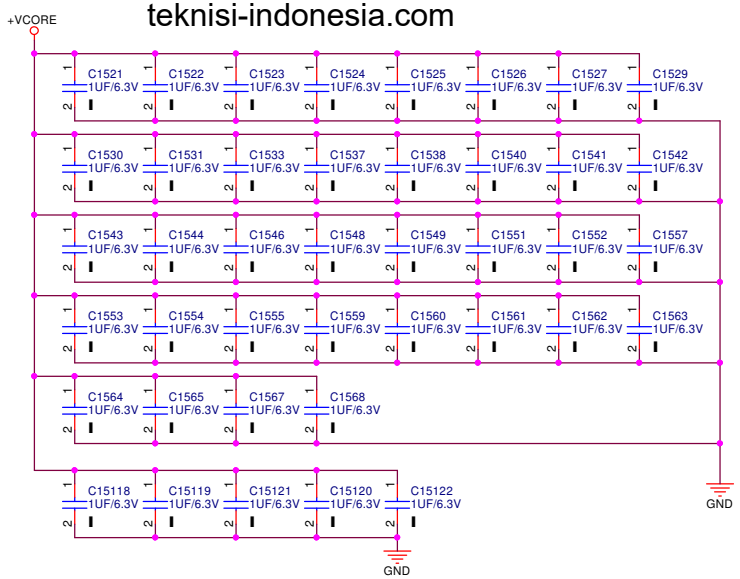
continued...

+VCCSA

Under CPU



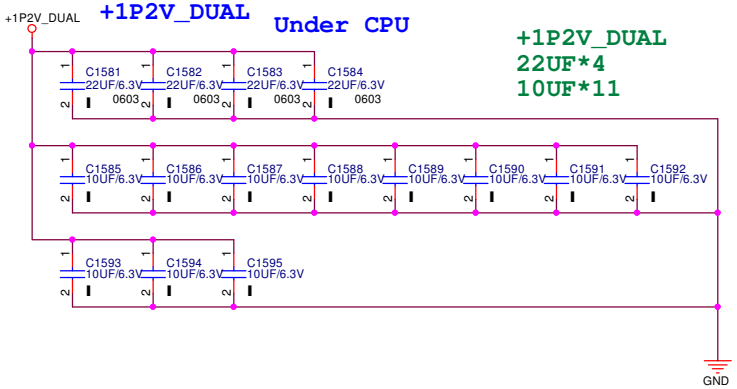
+VCCSA
1UF*1



+VCCORE
47UF*3
22UF*10
10UF*32
1UF*41

+1P2V_DUAL

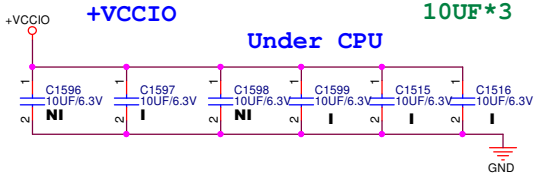
Under CPU



+1P2V_DUAL
22UF*4
10UF*11

+VCCIO

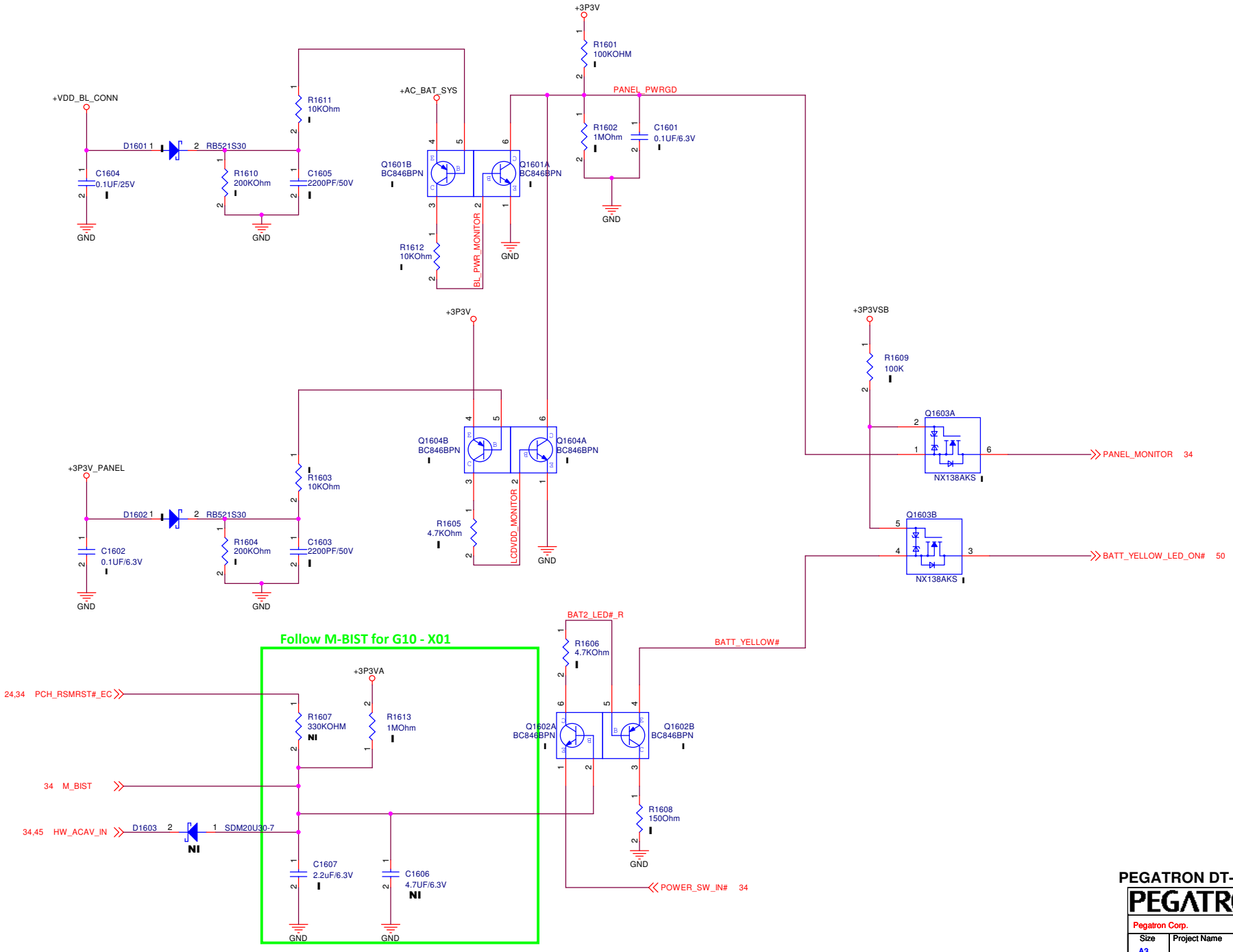
Under CPU



+VCCIO
10UF*3

PEGATRON	Title : CPU DECOUPLING	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 15 of 110	

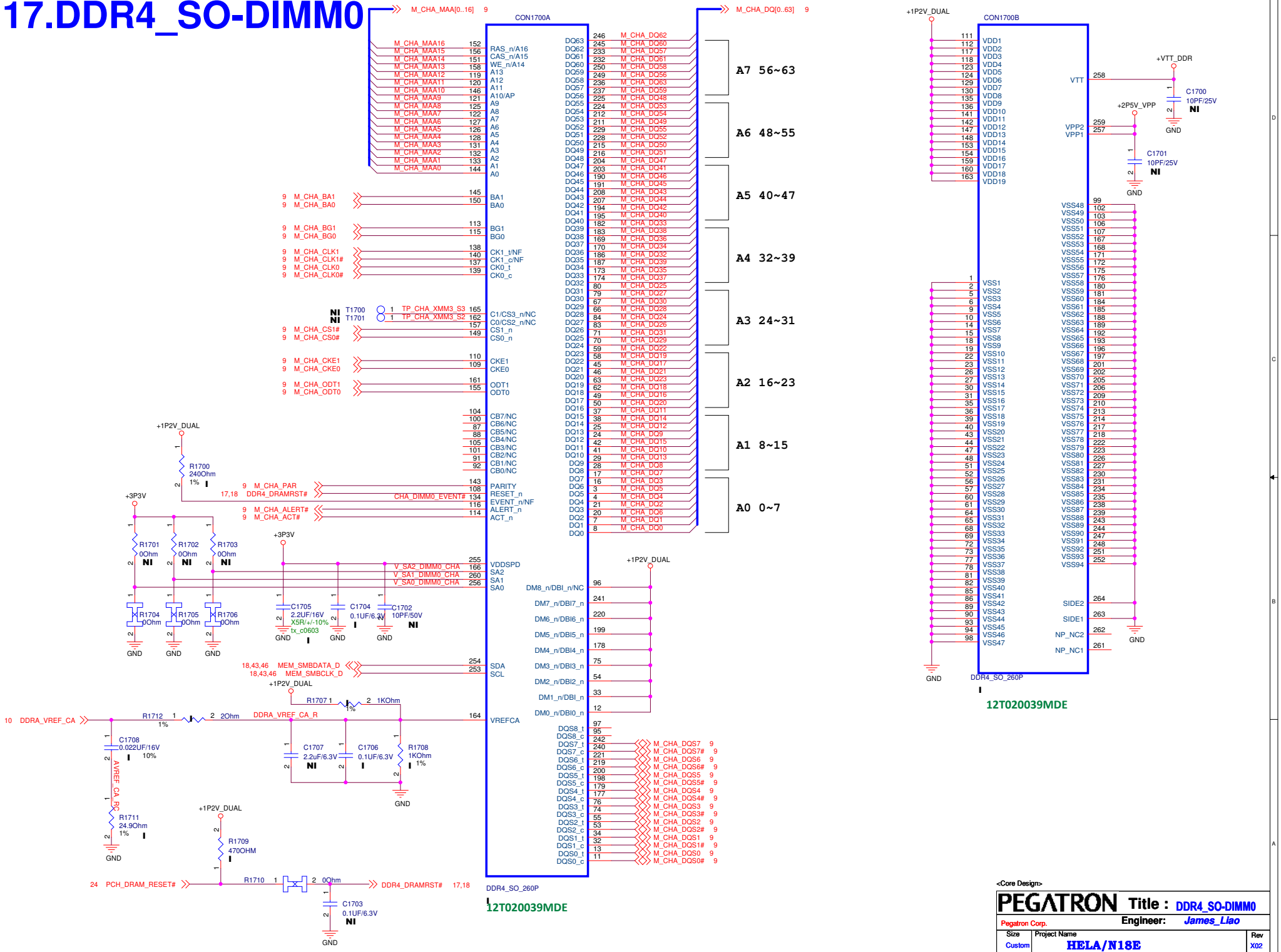
16.LCD_BIST/MB_BIST



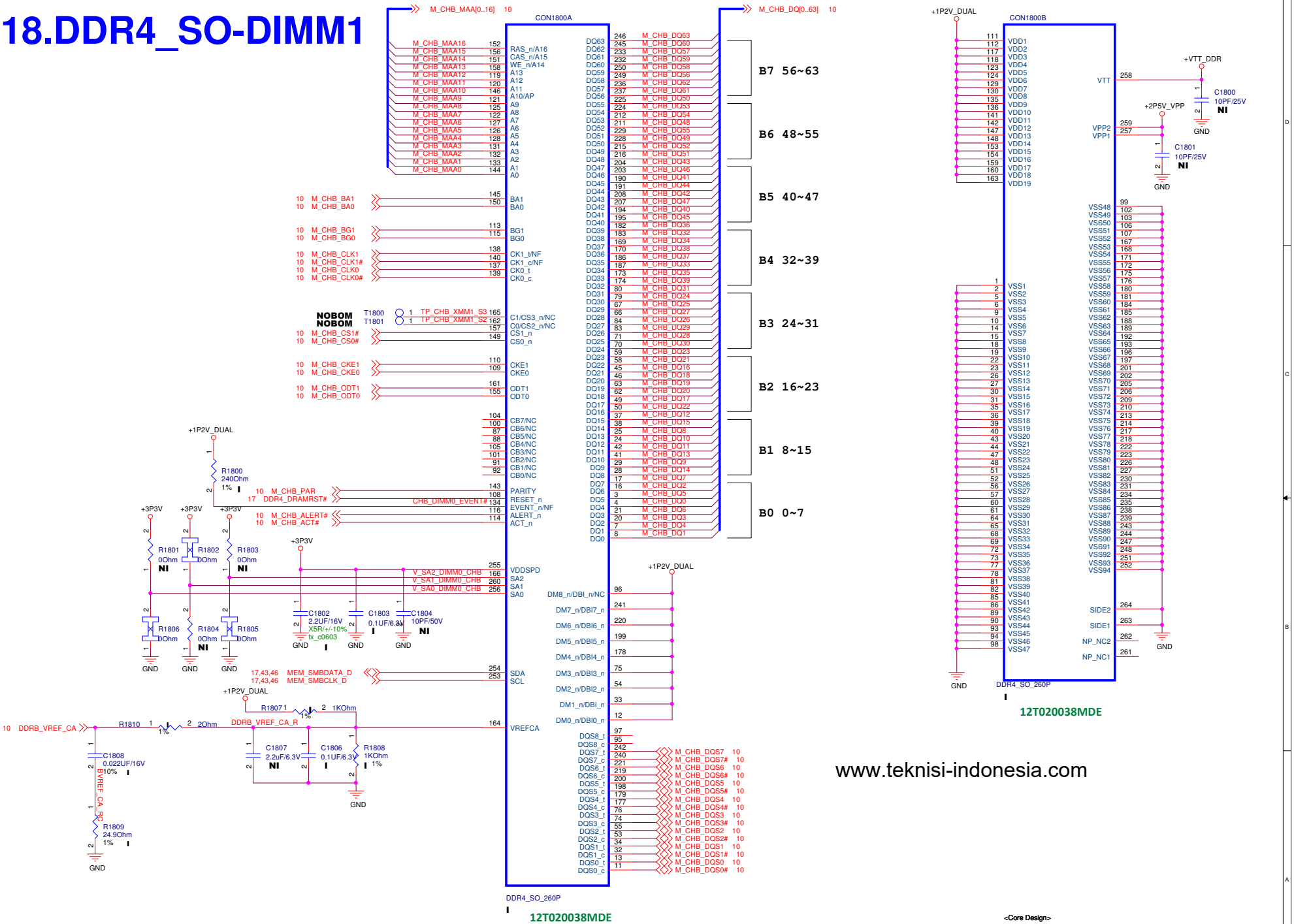
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : LCD_BIST/MB_BIST	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 16 of 110	

17.DDR4_SO-DIMM0



18.DDR4_SO-DIMM1



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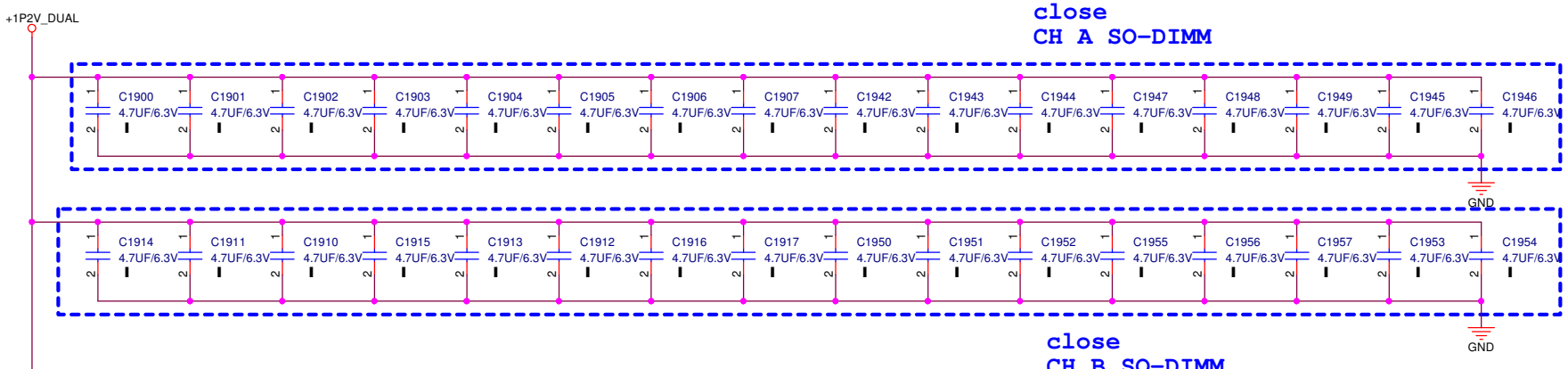
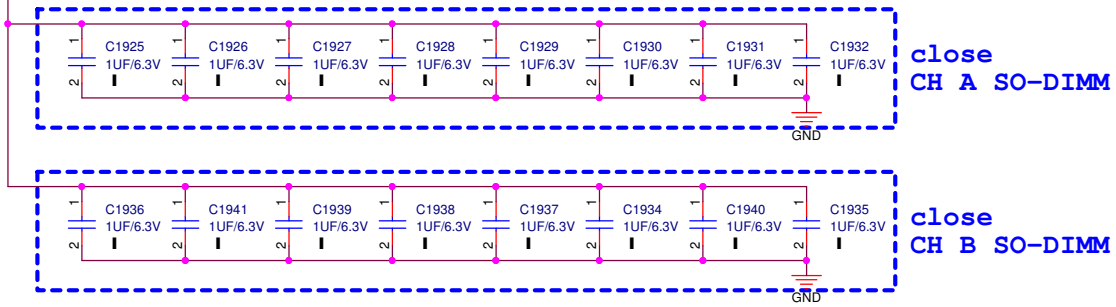
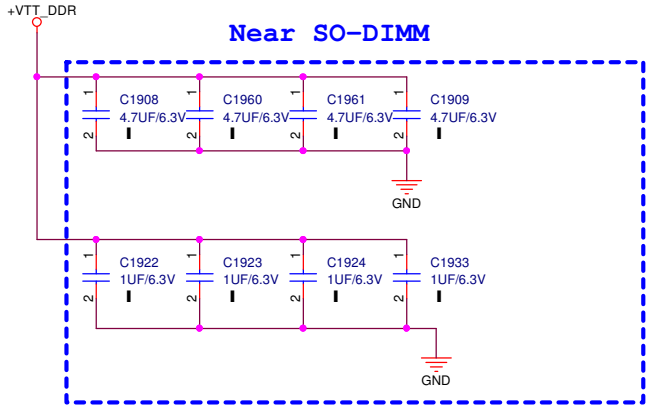
<Core Design>

PEGATRON	Title : DDR4_SO-DIMM1	
Pegatron Corp.	Engineer: James_Liao	
Size: Custom	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 18 of 110	

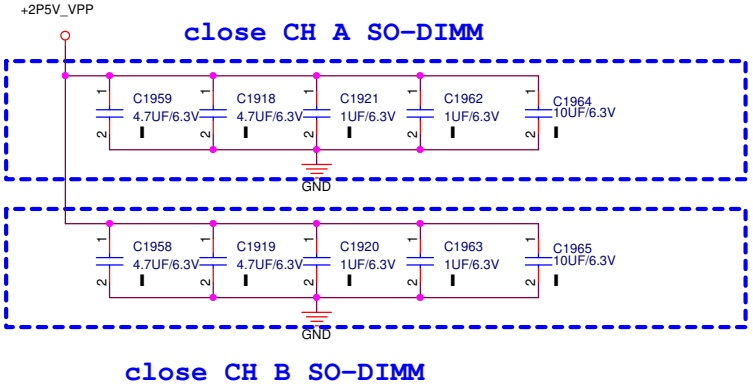






DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	



PEGATRON Title : DDR DECOUPLING

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 19 of 110

20.PCH DMI_PCIE_USB_SATA

U2000A

DMI

DMI_TXN0 DMI_TXP0 DMI_RXN0 DMI_RXP0 → K34 J35 C33 B33 → DMI0_RXN DMI0_RXP DMI0_TXN DMI0_TXP

DMI_TXN1 DMI_TXP1 DMI_RXN1 DMI_RXP1 → G33 F34 C32 B32 → DMI1_RXN DMI1_RXP DMI1_TXN DMI1_TXP

DMI_TXN2 DMI_TXP2 DMI_RXN2 DMI_RXP2 → K32 J32 C31 B31 → DMI2_RXN DMI2_RXP DMI2_TXN DMI2_TXP

DMI_TXN3 DMI_TXP3 DMI_RXN3 DMI_RXP3 → G30 F30 C29 B29 → DMI3_RXN DMI3_RXP DMI3_TXN DMI3_TXP

M29 K29 E28 D29 → RSVD_1 RSVD_2 RSVD_3 RSVD_4

M26 L26 C27 B27 → RSVD_5 RSVD_6 RSVD_7 RSVD_8

G26 F26 B26 C26 → RSVD_9 RSVD_10 RSVD_11 RSVD_12

R24 P24 B25 A25 → RSVD_13 RSVD_14 RSVD_15 RSVD_16

High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE		SATA 0b	SATA 1a	SATA 0a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	SATA 6	SATA 7				
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

PCIE/USB/SATA

PCIE1_TXP/USB31_7_TXP PCIE1_TXN/USB31_7_TXN PCIE1_RXP/USB31_7_RXP PCIE1_RXN/USB31_7_RXN

PCIE2_TXP/USB31_8_TXP PCIE2_TXN/USB31_8_TXN PCIE2_RXP/USB31_8_RXP PCIE2_RXN/USB31_8_RXN

PCIE3_TXP/USB31_9_TXP PCIE3_TXN/USB31_9_TXN PCIE3_RXP/USB31_9_RXP PCIE3_RXN/USB31_9_RXN

PCIE4_TXP/USB31_10_TXP PCIE4_TXN/USB31_10_TXN PCIE4_RXP/USB31_10_RXP PCIE4_RXN/USB31_10_RXN

PCIE5_TXP PCIE5_TXN PCIE5_RXP PCIE5_RXN

PCIE6_TXP PCIE6_TXN PCIE6_RXP PCIE6_RXN

PCIE7_TXP PCIE7_TXN PCIE7_RXP PCIE7_RXN

PCIE8_TXP PCIE8_TXN PCIE8_RXP PCIE8_RXN

PCIE9_TXP PCIE9_TXN PCIE9_RXP PCIE9_RXN

PCIE10_TXP PCIE10_TXN PCIE10_RXP PCIE10_RXN

PCIE11_TXP/SATA0A_TXP PCIE11_TXN/SATA0A_TXN PCIE11_RXP/SATA0A_RXP PCIE11_RXN/SATA0A_RXN

PCIE12_TXP/SATA1A_TXP PCIE12_TXN/SATA1A_TXN PCIE12_RXP/SATA_1A_RXP PCIE12_RXN/SATA1A_RXN

FH82HM370

USB2.0

USB2P_1 / USB2N_1	J2 / J3	IPD 14~24KOHM	USBP1 44 / USBN1 44 — IO USB3.1(Type-A_1)
USB2P_2 / USB2N_2	N15 / N13	IPD 14~24KOHM	USBP2 38 / USBN2 38 — RIGHT USB3.1(Type-A) -Power share
USB2P_3 / USB2N_3	K3 / K4	IPD 14~24KOHM	USBP3 38 / USBN3 38 — MB USB3.1(Type-A)
USB2P_4 / USB2N_4	L9 / M10	IPD 14~24KOHM	USBP4 30 / USBN4 30 — TBT USB3.1(Type-C)
USB2P_5 / USB2N_5	L2 / M1	IPD 14~24KOHM	USBP5 48 / USBN5 48 — WEBCAM
USB2P_6 / USB2N_6	K6 / K7	IPD 14~24KOHM	USBP6 44 / USBN6 44 — Card Reader
USB2P_7 / USB2N_7	L3 / L4	IPD 14~24KOHM	
USB2P_8 / USB2N_8	G5 / G4	IPD 14~24KOHM	
USB2P_9 / USB2N_9	N8 / M6	IPD 14~24KOHM	USBP9 44 / USBN9 44 — Finger Print Reader
USB2P_10 / USB2N_10	H2 / H3	IPD 14~24KOHM	
USB2P_11 / USB2N_11	P9 / R10	IPD 14~24KOHM	USBP11 50 / USBN11 50 — ELC
USB2P_12 / USB2N_12	G2 / G1	IPD 14~24KOHM	
USB2P_13 / USB2N_13	N2 / N3	IPD 14~24KOHM	
USB2P_14 / USB2N_14	F6 / E5	IPD 14~24KOHM	USBP14 33 / USBN14 33 — M.2 2230 WLAN KEY-E

USB3.1

USB31_1_TXP / TXN / RXP / RXN	F7 / F9 / C11 / D11		USB3_TX_P1 44 / USB3_TX_N1 44 / USB3_RX_P1 44 / USB3_RX_N1 44 — USB3.1 Gen1 Type-A IODB
USB31_2_TXP / TXN / RXP / RXN	D4 / C3 / C9 / B9	USB3_TX_P2_C — C2006 0.1UF/6.3V; USB3_TX_N2_C — C2007 0.1UF/6.3V	USB3_TX_P2 38 / USB3_TX_N2 38 / USB3_RX_P2 38 / USB3_RX_N2 38 — USB3.1 Gen1 Type-A Power share Right Side
USB31_3_TXP / TXN / RXP / RXN	G12 / F11 / C10 / B10	USB3_TX_P3_C — C2008 0.1UF/6.3V; USB3_TX_N3_C — C2009 0.1UF/6.3V	USB3_TX_P3 38 / USB3_TX_N3 38 / USB3_RX_P3 38 / USB3_RX_N3 38 — USB3.1 Gen1 Type-A Rear Side
USB31_4_TXP / TXN / RXP / RXN	C14 / B14 / J15 / K16		
USB31_5_TXP / TXN / RXP / RXN	B15 / C15 / K13 / J13		
USB31_6_TXP / TXN / RXP / RXN	C16 / C17 / F14 / G14		

USB2_ID G3 — USB2_VBUSSENSE F3 — USB2_VBUSSENSE

R2000 1K NI (1 — 2) — GND GND

M.2 PCIE X4 #1

31 PCIE9_SSD1_TXP / TXN / RXP / RXN

31 PCIE10_SSD1_TXP / TXN / RXP / RXN

31 PCIE11_SSD1_TXP / TXN / RXP / RXN

31 PCIE12_SATA1A_SSD1_TXP / TXN / RXP / RXN

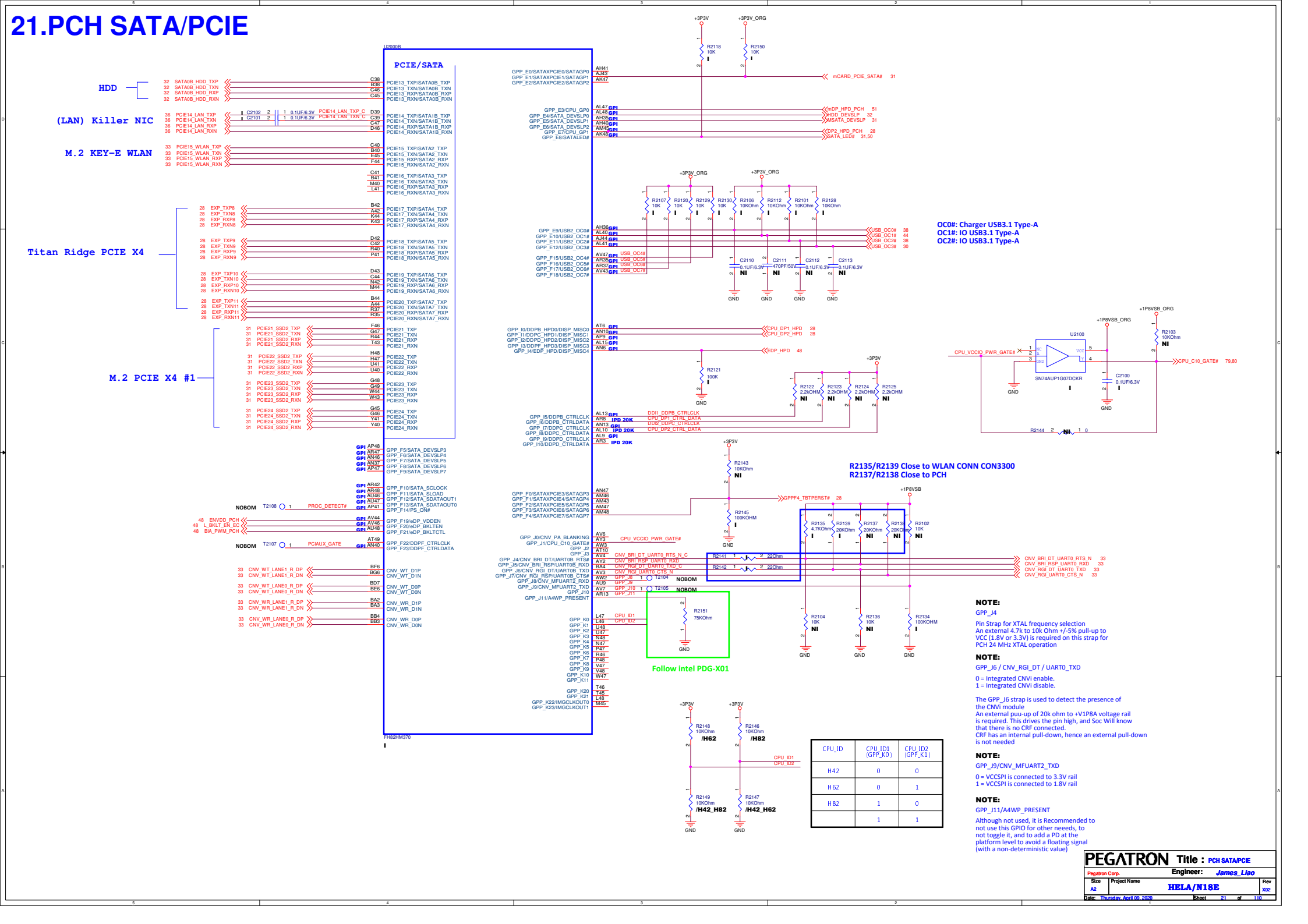
PEGATRON Title : PCH DMI_PCIE_USB_SATA

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 20 of 110

21.PCH SATA/PCIE



CPU_ID	CPU_ID1 (GPP_K0)	CPU_ID2 (GPP_K1)
H42	0	0
H62	0	1
H82	1	0
	1	1

NOTE:

GPP_J4

Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

NOTE:

GPP_J6 / CNV_RGI_DT / UART0_TXD

0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

The GPP_J6 strap is used to detect the presence of the CNVi module
An external puu-up of 20k ohm to +V1P8A voltage rail is required. This drives the pin high, and Soc Will know that there is no CRF connected.
CRF has an internal pull-down, hence an external pull-down is not needed

NOTE:

GPP_J9/CNV_MFUART2_TXD

0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

NOTE:

GPP_J11/A4WP_PRESENT

Although not used, it is Recommended to not use this GPIO for other neeeds, to not toggle it, and to add a PD at the platform level to avoid a floating signal (with a non-deterministic value)

PEGATRON Title : PCH SATA/PCIE

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A2	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 21 of 110

22.PCH ESPI/SPI/FAN/HOST

NOTE:
eSPI operates at 1.8V

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE: GPP_G
Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G supports dynamic voltage configuration ONLY when the family is used for SOXC functionality. If the family is used for GPIOs, per pin voltage configuration is NOT supported. GPP_G group voltage is selected by setting the corresponding soft strap only.

U2000F

LPC/ESPI
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K18/NMI#
GPP_K19/SMI#

SD
GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP

SPI0
SPI0_CS2#
SPI0_CS1#
SPI0_CS0#
SPI0_MOSI
SPI0_MISO
SPI0_CLK
SPI0_IO3
SPI0_IO2

HOST
PM_DOWN
PM_SYNC
PECI

ISH_GP
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
GPP_K16/GSXCLK
GPP_K17/ADR_COMPLETE
GPP_A8/CLKRUN#
GPP_A11/PME#/SD_VDD2_PWR_EN#
GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
GPP_A16/CLKOUT_48

FH82HM370

Close to PCH

Follow PDG 15 ohm->0ohm -X01

Change FFS_INT1 connection to GPP_A23- X01

follow GPIO table

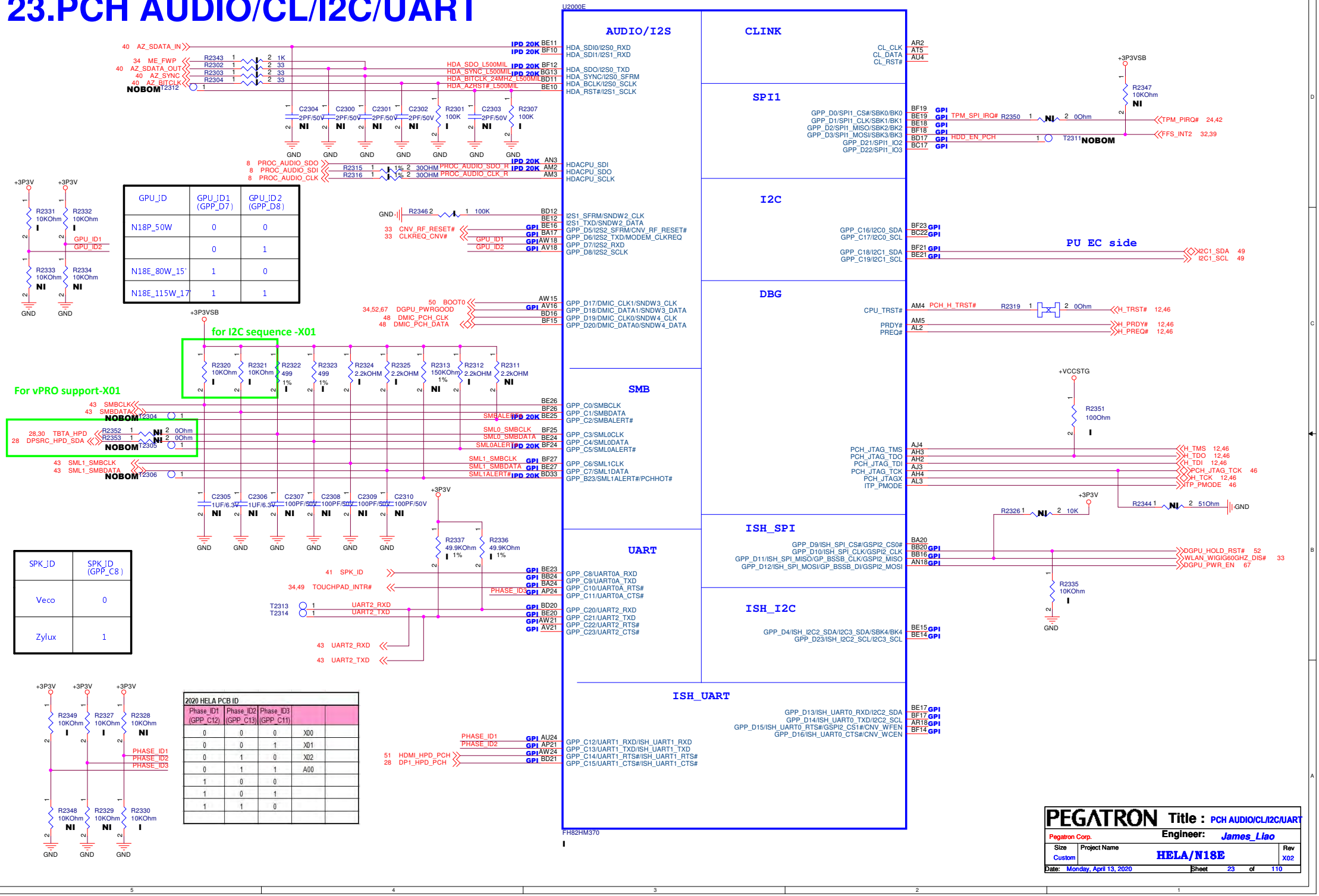
GPP_G3 / GPP_G4	0	1
0		
1		

	TPM ID (GPP_G7)
iTPM	0
dTPM	1

NOTE:
SUSACK#: If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.

PEGATRON Title : PCH ESPI/SPI/FAN/HOST
Pegatron Corp. Engineer: James_Liao
Size: Custom | Project Name: HELA/N18E | Rev: X02
Date: Thursday, April 09, 2020 | Sheet 22 of 110

23.PCH AUDIO/CL/I2C/UART



GPU_ID	GPU_ID1 (GPP_D7)	GPU_ID2 (GPP_D8)
N18P_50W	0	0
	0	1
N18E_80W_15'	1	0
N18E_115W_17	1	1

SPK_ID	SPK_ID (GPP_C8)
Veco	0
Zylux	1

2020 HELA PCB ID			
Phase_ID1 (GPP_C12)	Phase_ID2 (GPP_C13)	Phase_ID3 (GPP_C11)	
0	0	0	X00
0	0	1	X01
0	1	0	X02
0	1	1	A00
1	0	0	
1	0	1	
1	1	0	

PEGATRON Title : PCH AUDIO/CL/I2C/UART

Pegatron Corp. Engineer: James_Liao

Size: Custom | Project Name: HELA/N18E | Rev: X02

Date: Monday, April 13, 2020 | Sheet 23 of 110

24.PCH SML/I2C/MISC

NOTE:
GPP_B22/GSPI1_MOSI

This Signal has a weak internal pull-down.
Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI0_MOSI/GPP_B18

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

Change FFS_INT1 connection to GPP_A23- X01

NOTE:
GPP_B14 / SPKR

0 = Disable “Top Swap” mode. (Default)
1 = Enable “Top Swap” mode.

NOTE:
GPP_H15/SML3ALERT#
External pull-up is required. Recommend 100K if pulled

NOTE:
GPP_H12/SML2ALERT#

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

Warning: This strap must be configured to ‘0’ (SAFS is disabled) if the eSPI or LPC strap is configured to ‘0’ (eSPI is disabled

for sequence

PEGATRON	Title : PCH SML/I2C/MISC		
Pegatron Corp.	Engineer: James_Liao		
Size: A2	Project Name: HELA/N18E	Rev: X02	
Date: Thursday, April 09, 2020	Sheet 24 of 110		

25.PCH CLOCK

NOTE:
CRB: 2.71Kohm
Refer to GND; NOT near switching noise; spacing 3x
Add a GND shield(Width>4 mils)
between XCLK_BIASREF and adjacent IO signals

U2000C

CLOCK

CK_100M_BCK
CK_100M_BCK#
CK_24M_BCK
CK_24M_BCK#
CK_100M_PCIE
CK_100M_PCIE#
CK_100M_XDP
CK_100M_XDP#

CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUPCIBCLK_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_ITPXDP_P
CLKOUT_ITPXDP_N

CLKOUT_PCIE_P0 … CLKOUT_PCIE_P3
CLKOUT_PCIE_N0 … CLKOUT_PCIE_N3
CLKOUT_PCIE_P4 … CLKOUT_PCIE_P9
CLKOUT_PCIE_N4 … CLKOUT_PCIE_N9
CLKOUT_PCIE_P10 … CLKOUT_PCIE_P15
CLKOUT_PCIE_N10 … CLKOUT_PCIE_N15

CLK_100M_P2_LAN_R → R2512 → CLK_100M_P2_LAN 36
CLK_100M_N2_LAN_R → R2513 → CLK_100M_N2_LAN 36
CLK_100M_P3_WLAN_R → R2514 → CLK_100M_P3_WLAN 33
CLK_100M_N3_WLAN_R → R2515 → CLK_100M_N3_WLAN 33
CLK_100M_P5_TBT_R → R2508 → CLK_100M_P5_TBT 28
CLK_100M_N5_TBT_R → R2509 → CLK_100M_N5_TBT 28
CLK_100M_P6_SSD1_R → R2517 → CLK_100M_P6_SSD1 31
CLK_100M_N6_SSD1_R → R2518 → CLK_100M_N6_SSD1 31
CLK_100M_P7_GPU_R → R2510 → CLK_100M_P7_GPU 52
CLK_100M_N7_GPU_R → R2511 → CLK_100M_N7_GPU 52
CLK_100M_P8_SSD2_R → R2526 → CLK_100M_P8_SSD2 31
CLK_100M_N8_SSD2_R → R2527 → CLK_100M_N8_SSD2 31

All: 2 0Ohm NOBOM

LAN
M2 WLAN
Titan-Ridge
M2 SSD1
GPU
M2 SSD2

R2500 2 1 60.4Ohm XCLK_BIASREF T3 → XCLK_BIASREF
R2516 2 1% 1 100 PCIE_RCOMPP A13 / PCIE_RCOMPN B12 → PCIE_RCOMPP / PCIE_RCOMPN
GND

NOBOM T2500 1 TP_PCH_RSVD_BD1 AL35 → TP_1
NOBOM T2501 1 TP_PCH_RSVD_BE2 AN35 → TP_2

RSVD_19 AH15
RSVD_20 R32
RSVD_21 N32
RSVD_22 U35
RSVD_23 U37
RSVD_24 R15
RSVD_25 R13
RSVD_26 U13
RSVD_27 Y35
RSVD_28 Y36
RSVD_29 Y15
RSVD_30 Y14

Q2500 SSM3K36FV
34,44 RTCRST_ON
R2524 100KOHM
/RTC_GEN9
/RTC_GEN9
GND GND

44 RTCRST# → BE47 RTCRST#
RTCX2_NO_IO BA48 RTCX2
RTCX1_NO_IO BA49 RTCX1

R2519 1 2 10MOhm
R2520 1 2 0Ohm NOBOM
Y5_R
X2500 32.768KHZ
C2500 18PF/50V
C2501 18PF/50V
GND GND

33 CLKIN_XTAL
R2523 1 2 0Ohm CLKIN_XTAL_C R6 → CLKIN_XTAL
NOBOM
R2507 10K
GND

AK2 TRIGGER_IN
AK3 TRIGGER_OUT
H_TRIGIN_R
14 H_TRIGOUT
14 H_TRIGIN
R2522 2 1 0Ohm
NOBOM

FH82HM370

CNV_WR_CLKP BE3 / CNV_WR_CLKN BD4 → CNV_WR_CLK_R_DP 33 / CNV_WR_CLK_R_DN 33
CNV_WT_CLKP BB6 / CNV_WT_CLKN BC5 → CNV_WT_CLK_R_DP 33 / CNV_WT_CLK_R_DN 33

XTAL_IN
XTAL_OUT
USB2_COMP F4
RSVD_17 BC1
RSVD_18 AH14
CNV_WT_RCOMP BA1
SD_1P8_RCOMP BE5
SD_3P3_RCOMP BE4
GPPJ_RCOMP_1P8_1 BD1
GPPJ_RCOMP_1P8_2 BE1
GPPJ_RCOMP_1P8_3 BE2

U10 XTAL24_IN R2525 1 2 0Ohm NOBOM XTAL24_IN_R
U9 XTAL24_OUT R2521 1 2 0Ohm NOBOM XTAL24_OUT_R
R2505 2 1% 1 113ohm NOBOM
T2502 NOBOM
CNV_WT_RCOMP_C R2501 1 1% 2 150Ohm
SD_RCOMP_1P8_C R2503 1 1% 2 200Ohm
SD_RCOMP_3P3_C R2504 1 1% 2 200Ohm
GPPJ_RCOMP_1P8_C R2506 1 1% 2 200Ohm

R2502 2 1% 1 200KOhm
X2501 24MHZ
C2502 10PF/50V
C2503 10PF/50V
GND GND GND GND

Table 28-7. 24 MHz Crystal Specifications

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

NOTE:
24MHz crystal : ESR 30 OHM

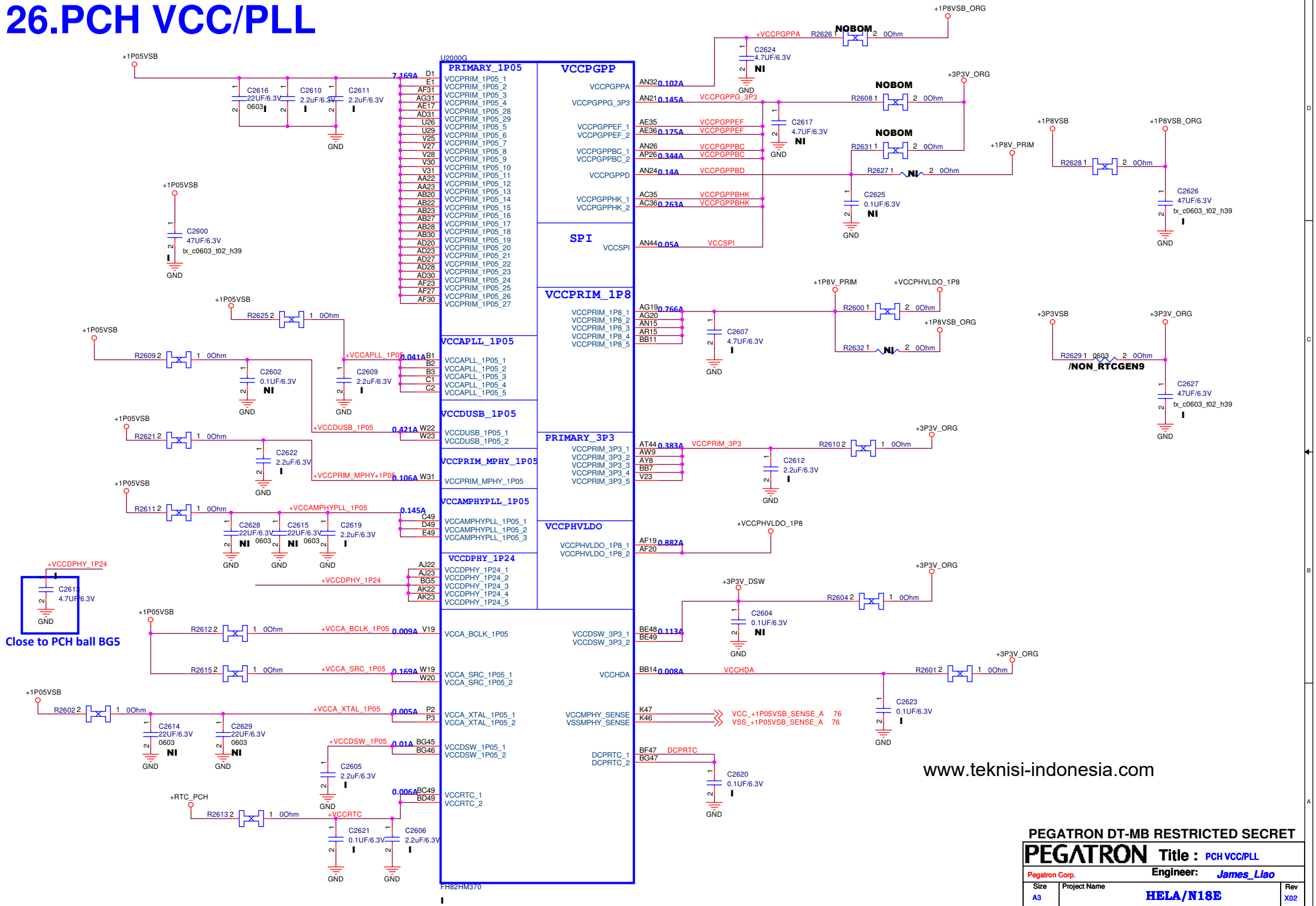
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH CLOCK
Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A3	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 25 of 110

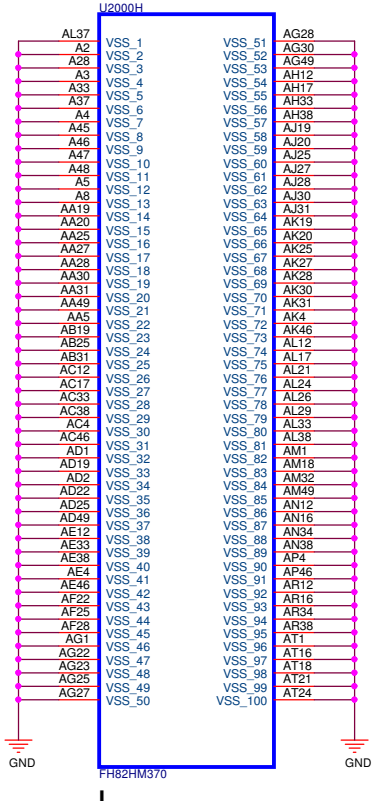
26.PCH VCC/PLL

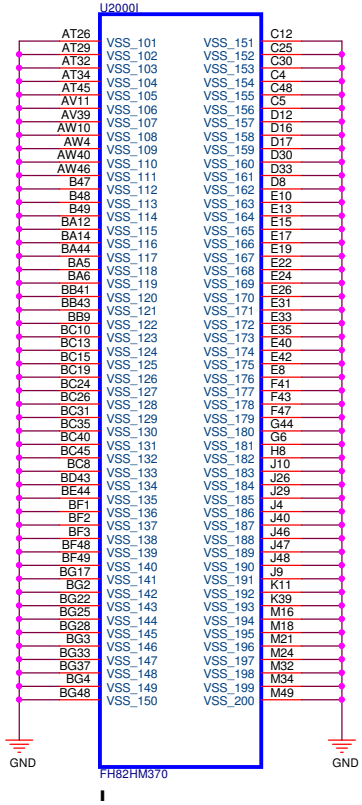


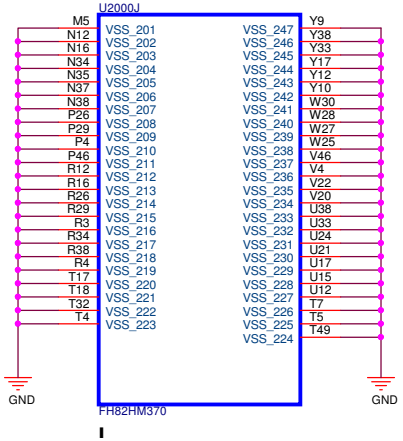
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCH VCC/PLL	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 26 of 110	

27.PCH VSS



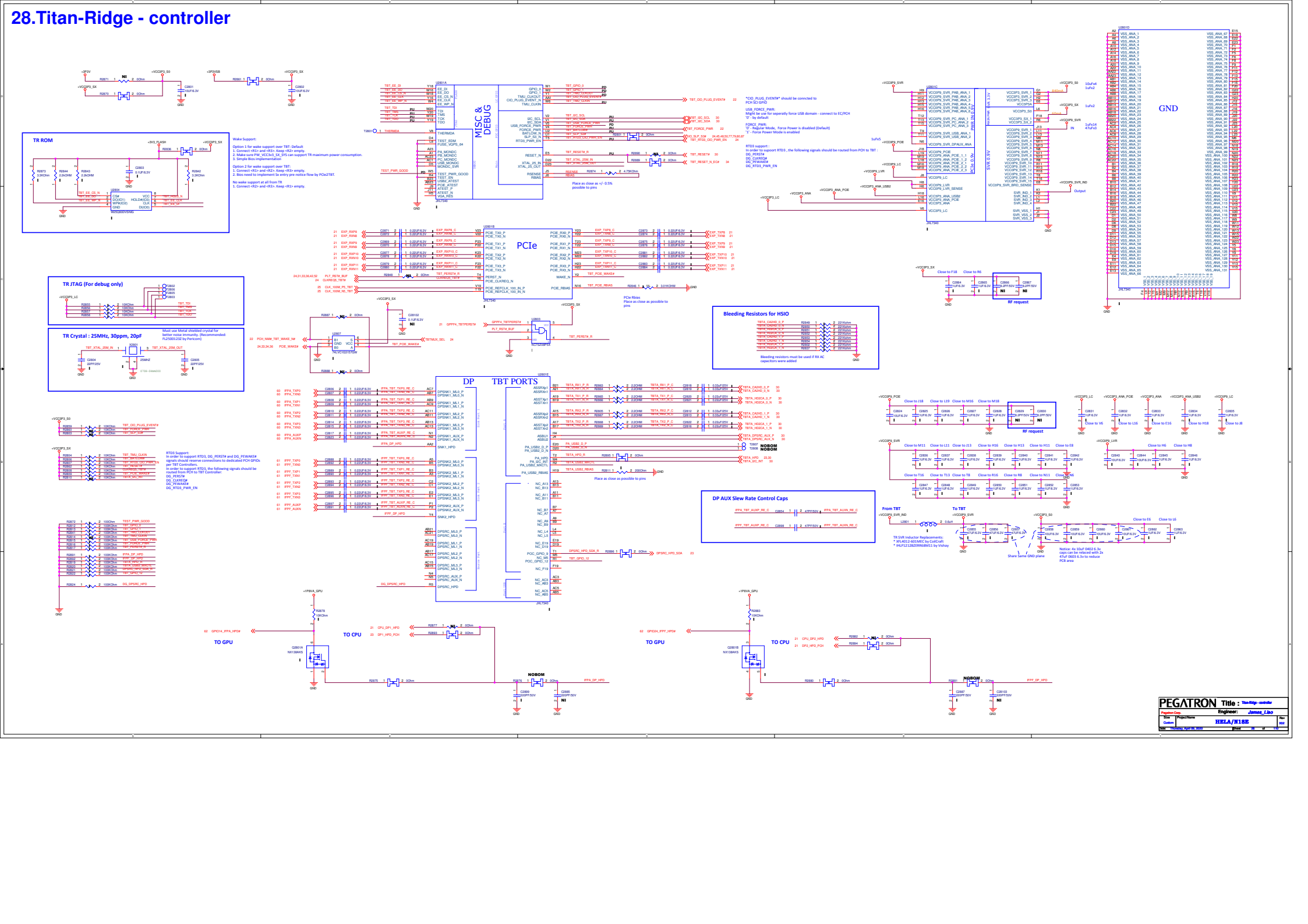




PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCH VSS	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 27 of 110	

28.Titan-Ridge - controller



PEGATRON DT-MB RESTRICTED SECRET

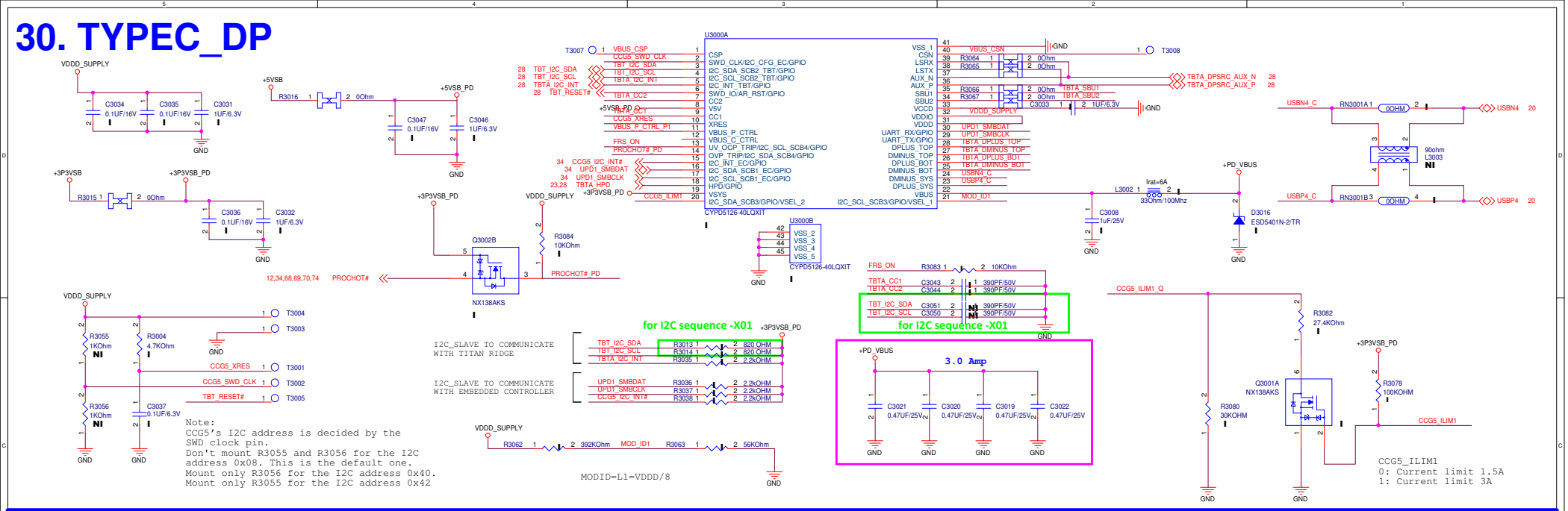
PEGATRON Title : <Title>

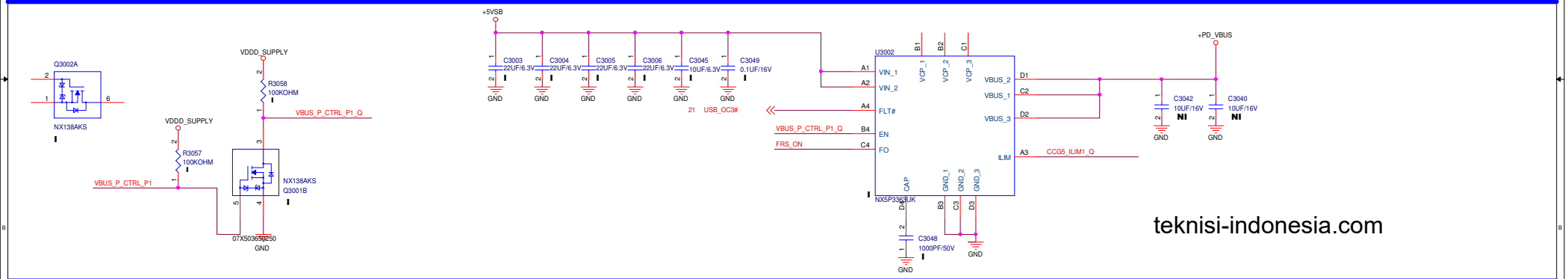
Pegatron Corp. Engineer: James_Liao

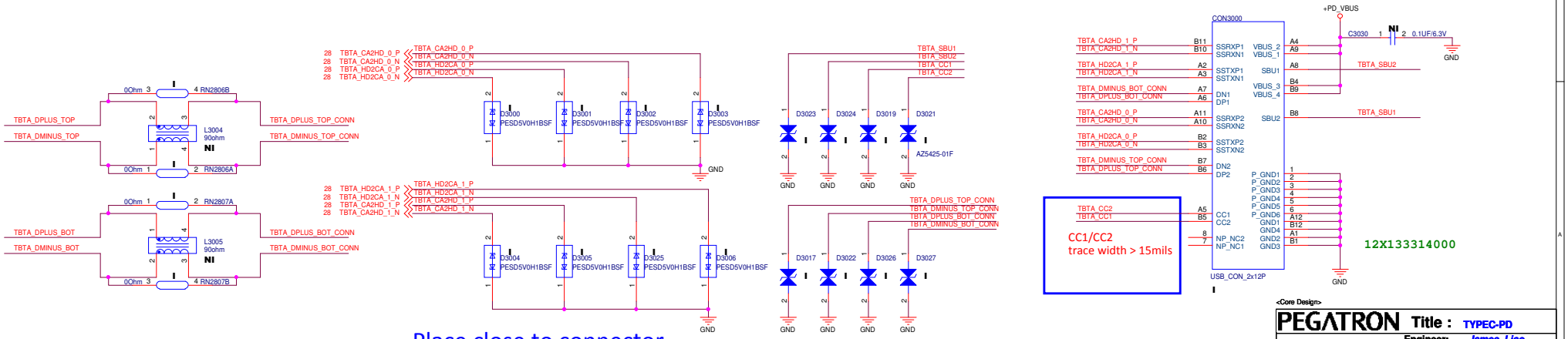
Size	Project Name	Rev
D	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 29 of 119

30. TYPEC_DP



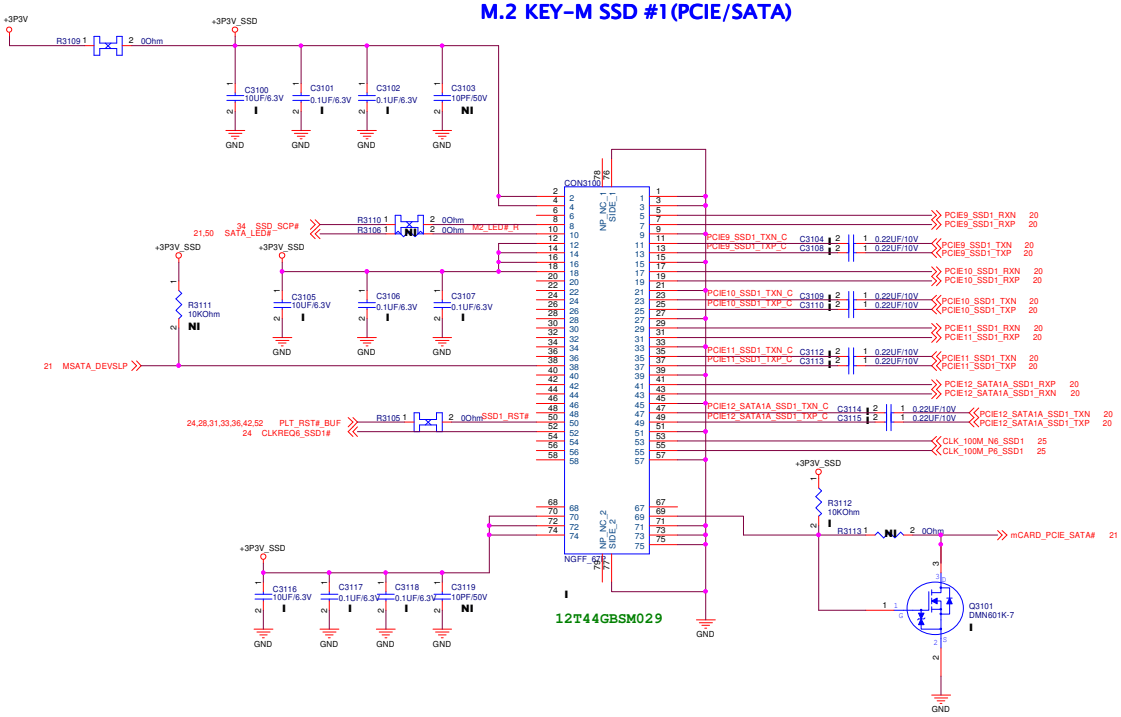




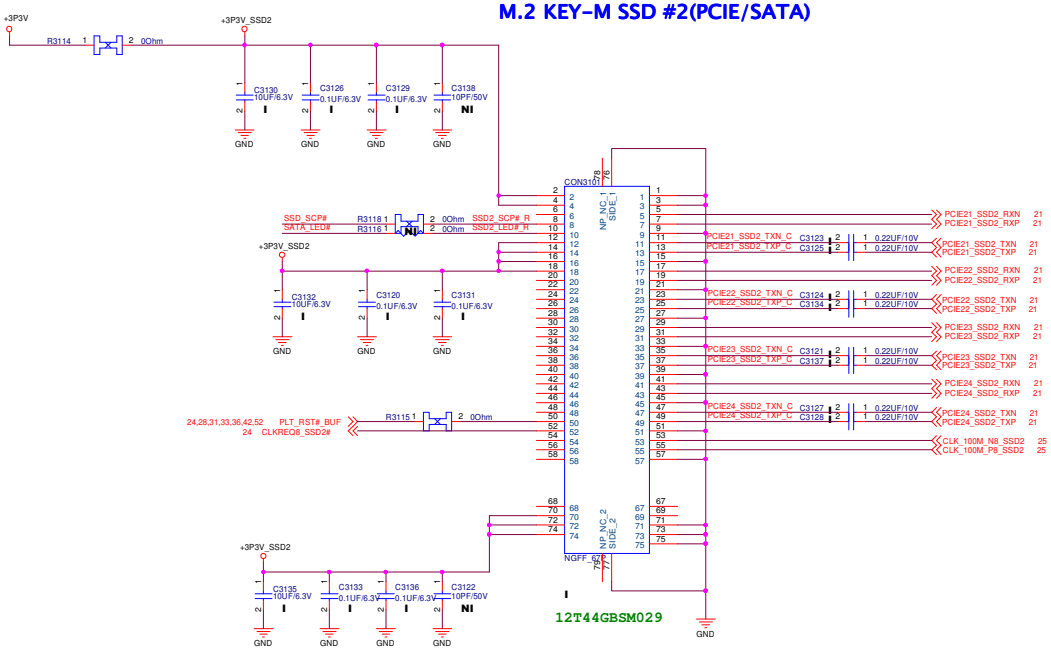
<Core Design>
PEGATRON Title : TYPEC-PD
Pegatron Corp. Engineer: James_Liao
Size C | Project Name HELA/N18E | Rev X02
Date: Thursday, April 09, 2020 | Sheet 30 of 110

31. M.2 2280 SSD #1 & #2

M.2 KEY-M SSD #1(PCIE/SATA)

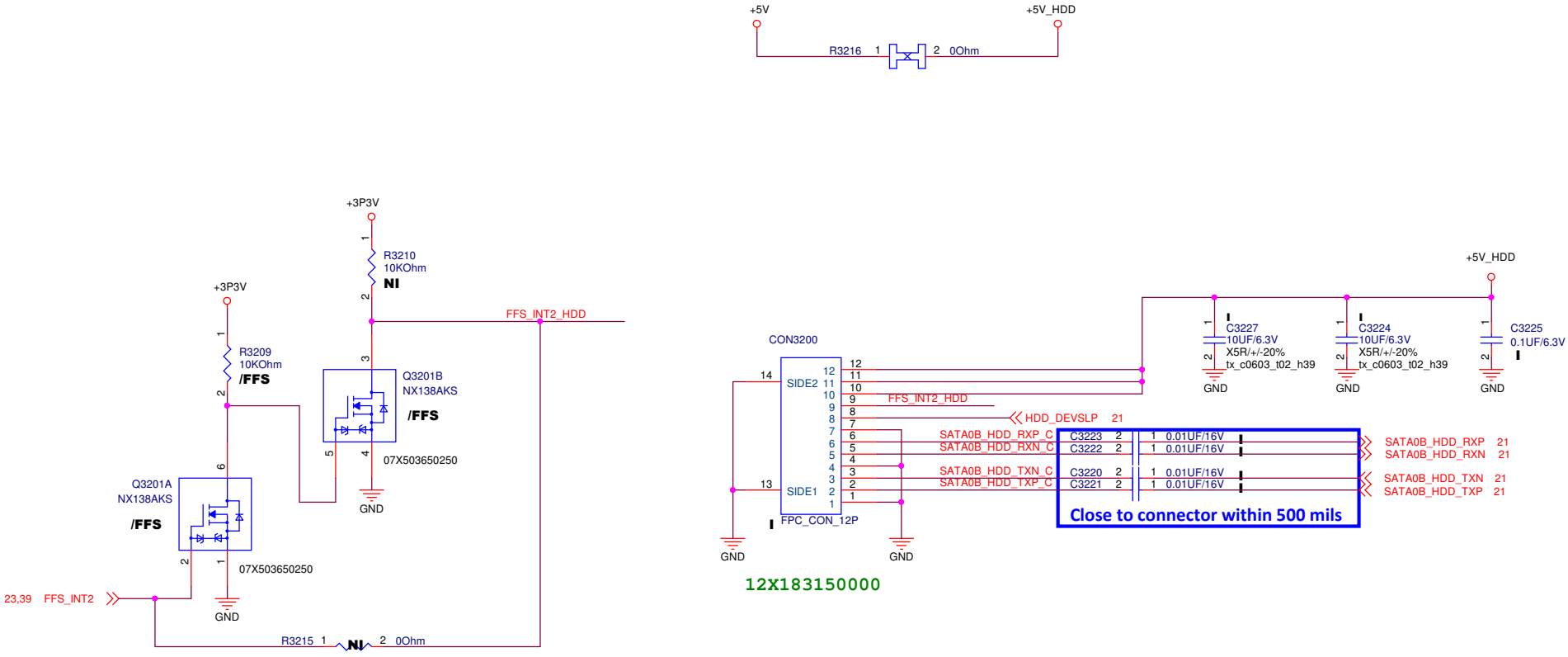


M.2 KEY-M SSD #2(PCIE/SATA)



PEGATRON	Title : M.2 2280 SSD #1 & #2		
Pegatron Corp.	Engineer: James_Liao		
Size: Custom	Project Name: HELA/N18E		Rev: X02
Date: Thursday, April 09, 2020	Sheet 31 of 110		

32. SATA HDD



<Core Design>

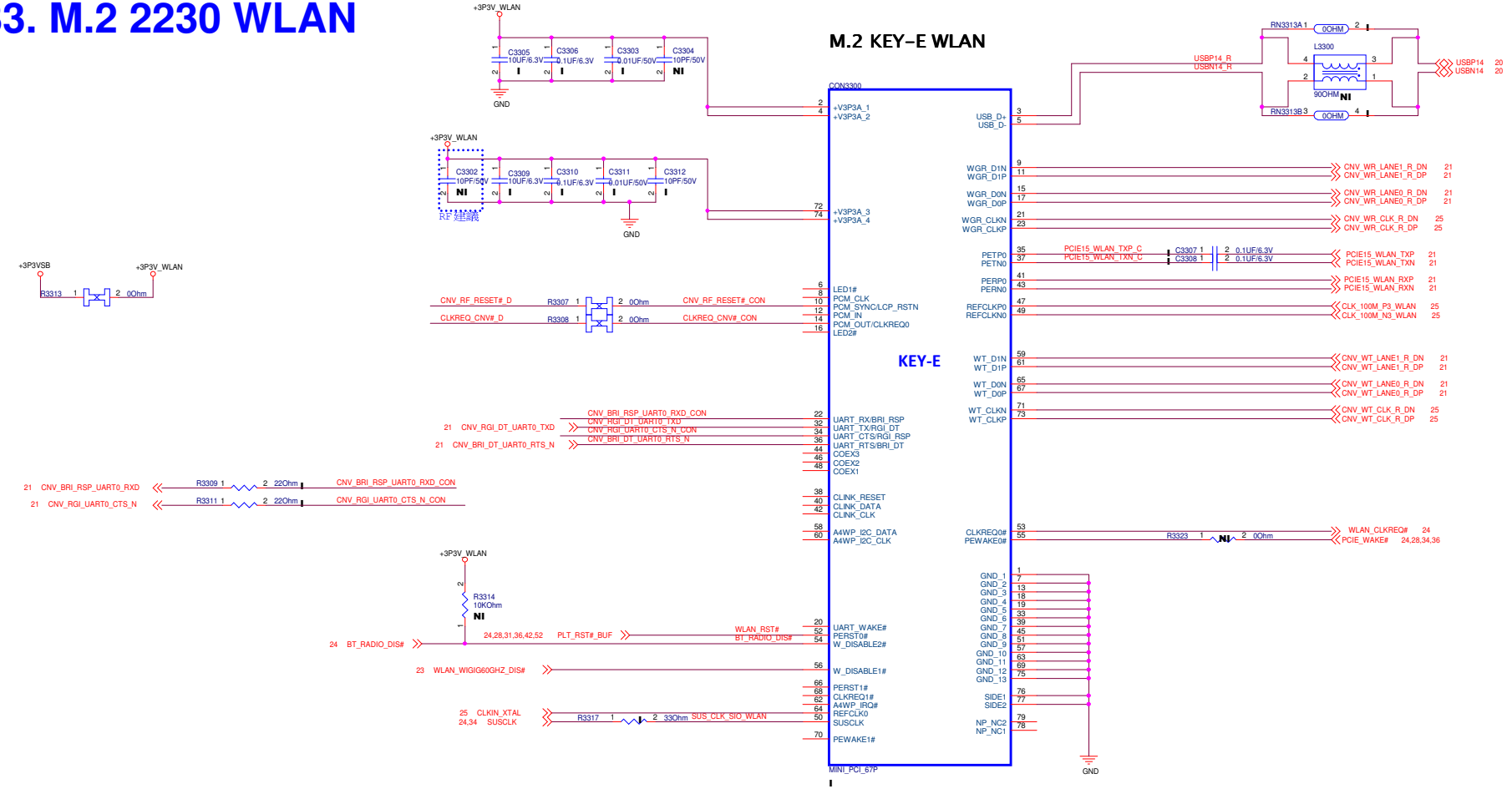
PEGATRON Title : SATA HDD

Pegatron Corp. Engineer: James_Liao

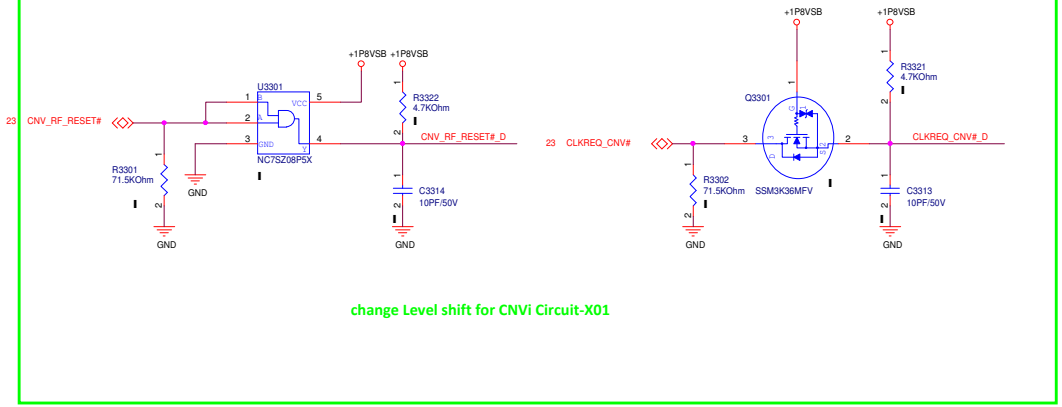
Size	Project Name	Rev
B	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 32 of 110

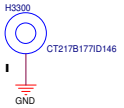
33. M.2 2230 WLAN



12T440036M00



Remark: 1.NC is not connected; YES is connected.
2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
4. Pin44, 46, 48, QCA suggest platform to NC.
5. Pin17 and 19 suggest reserve test point at platform side.



13XN00227000

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Corp.	Title : M.2 KEY-A 2230 WLAN	
	Engineer: James_Liao	
Size: C	Project Name: HELA/N18E	Rev: X02
Date: Monday, April 13, 2020	Sheet 33 of 110	

34.ME MEC1515

EC Power

eSPI Strap

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
1	1	Use 3.3V Shared SPI

Note:
If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel
If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

GPIO123/SHD_CS# (BSS_STRAP)

C3400 close to U3400.A8
C3401 close to U3400.B11
C3402 close to U3400.A15
C3403 close to U3400.B5

Imax:12.5mA

C3404 close to U3400.B48
C3405 close to U3400.B39
C3406 close to U3400.A52
C3407 close to U3400.B26
C3432 close to U3400.B9

Mount R3429 RTC current issue - X01

Mount R34167 for G-shift LED issue - X02

Mount R34171 for Audio MS power consumption issue - X02

Adapter power monitor to EC ADC pin
Need very close to EC

Close to U3400.B4

Close to U3400

Follow PDG 49.9 ohm->33ohm -X01

Follow PDG 49.9 ohm->33ohm -X01

mount R34152 for G3 Sharing -X01

Unmount R3404 RTC current issue - X01

BOARD_ID

BOARD_ID(GPIO155)	PULL-LOW RES	PULL-HIGH RES	VOLTAGE
X00	100.0K	10.0K	3.000
X01	100.0K	17.8K	2.801
X02	100.0K	27.0K	2.598
X03(reserve)	100.0K	37.4K	2.402
A00	100.0K	49.9K	2.201
A01	100.0K	64.9K	2.001
A02	100.0K	82.5K	1.809
A03	100.0K	107K	1.594
Reserve	100.0K	154K	1.299
Reserve	100.0K	200K	1.100
Reserve	100.0K	TBD	0.900
Reserve	100.0K	TBD	0.700
Reserve	100.0K	TBD	0.500
Reserve	100.0K	TBD	0.300

MODEL_ID

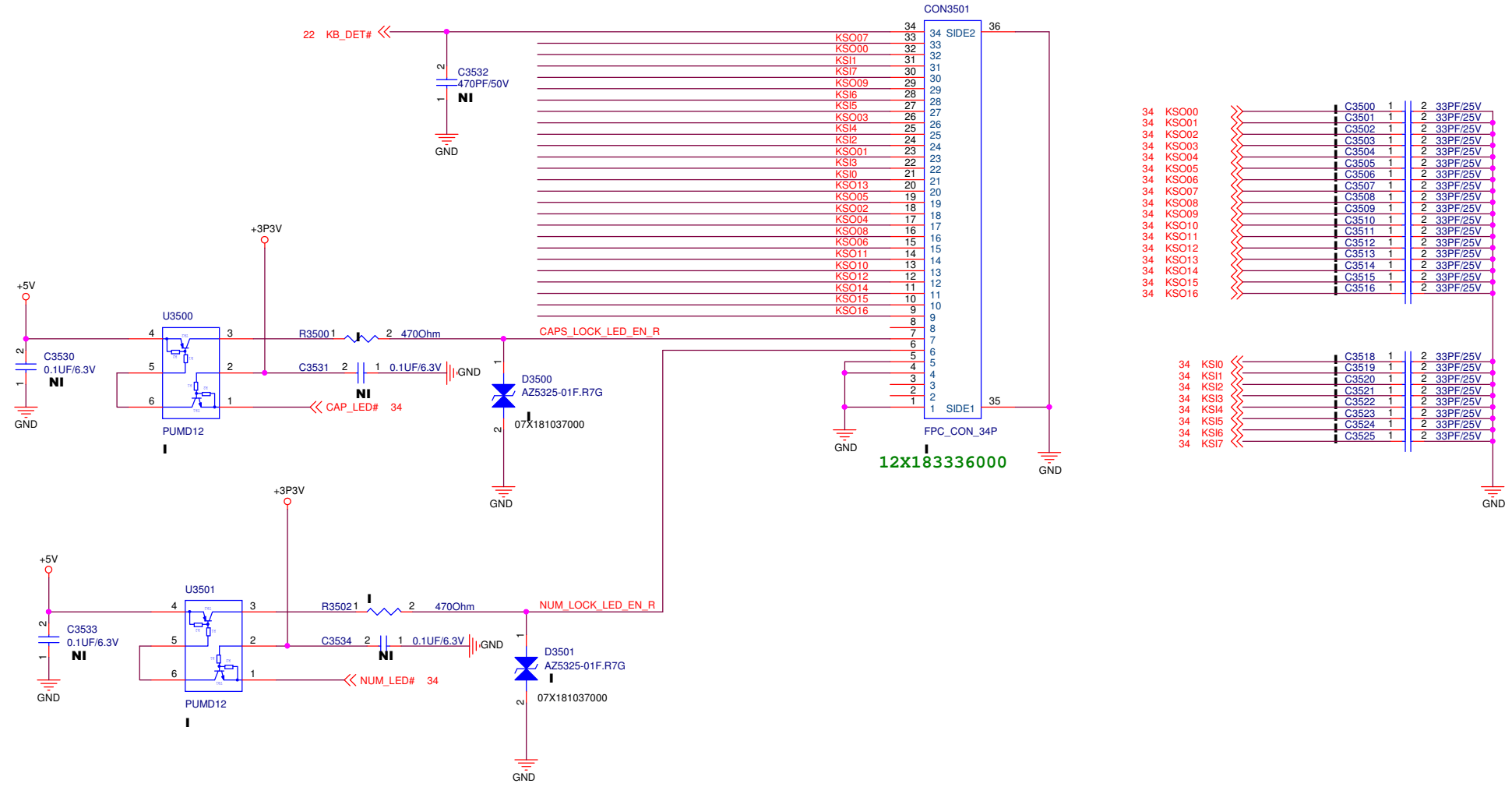
MODEL_ID(GPIO153)	PULL-LOW RES	PULL-HIGH RES	VOLTAGE
N18P-G62 15"	100.0K	10.0K	3.000
	100.0K	17.8K	2.801
N18E-G0 15"	100.0K	27.0K	2.598
N18E-G1R-MQ 15"	100.0K	37.4K	2.402
N18E-G0 17"	100.0K	49.9K	2.201
N18E-G1R 17"	100.0K	64.9K	2.001
N18E-G2R 17"	100.0K	82.5K	1.809
Reserve	100.0K	107K	1.594
Reserve	100.0K	154K	1.299
Reserve	100.0K	200K	1.100
Reserve	100.0K	TBD	0.900
Reserve	100.0K	TBD	0.700
Reserve	100.0K	TBD	0.500
Reserve	100.0K	TBD	0.300

HELA15(50W)
HELA15(80W)
HELA15(80W)
HELA15(115W)
HELA15(115W)

JTAG Strap

PEGATRON	Title : EC_MEC1515
Pegatron Corp.	Engineer: James_Liao
Size: Custom	Project Name: HELA/N18E
Date: Monday, April 15, 2020	Sheet 36 of 150

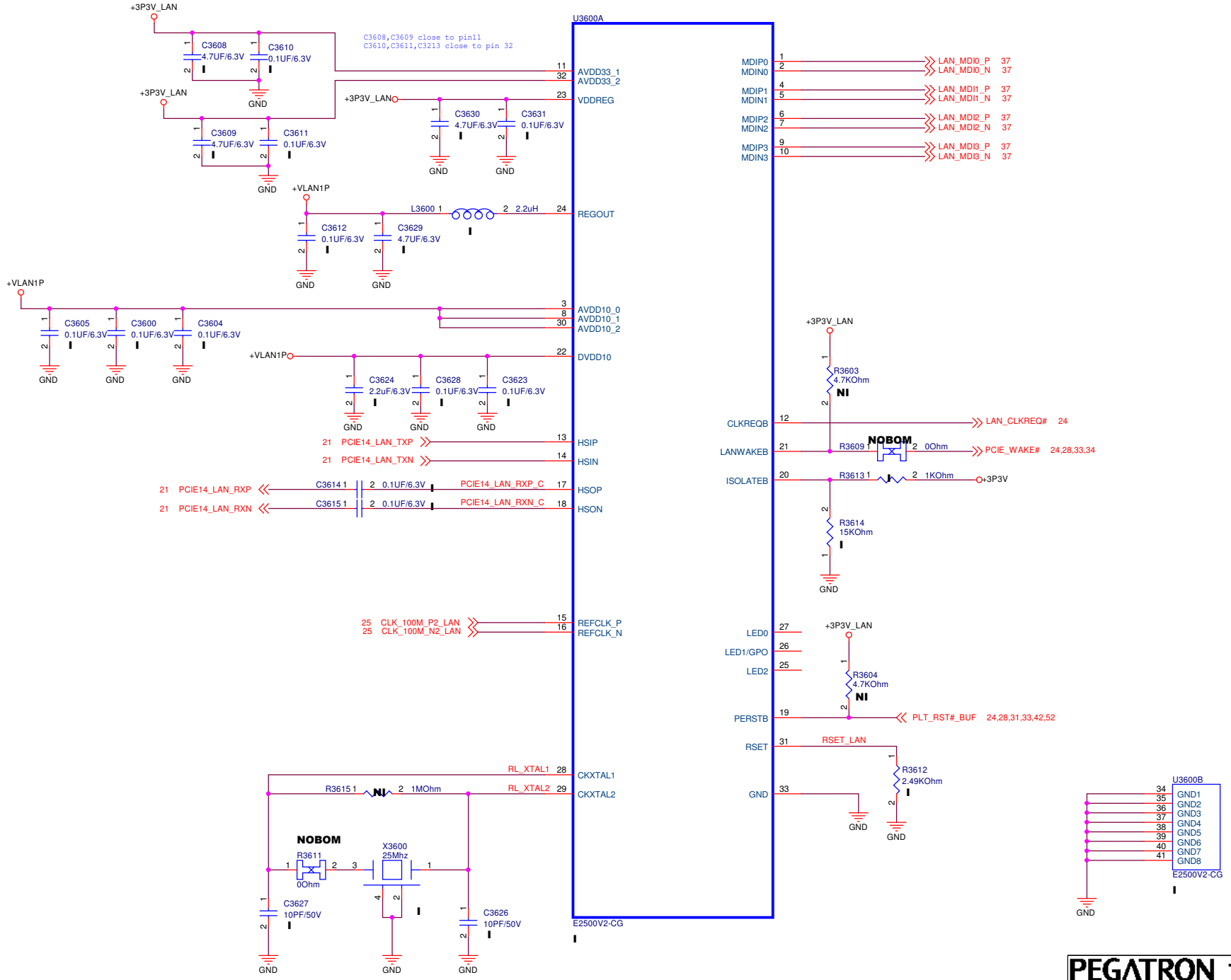
35.KEYBOARD



PEGATRON DT-MB RESTRICTED SECRET

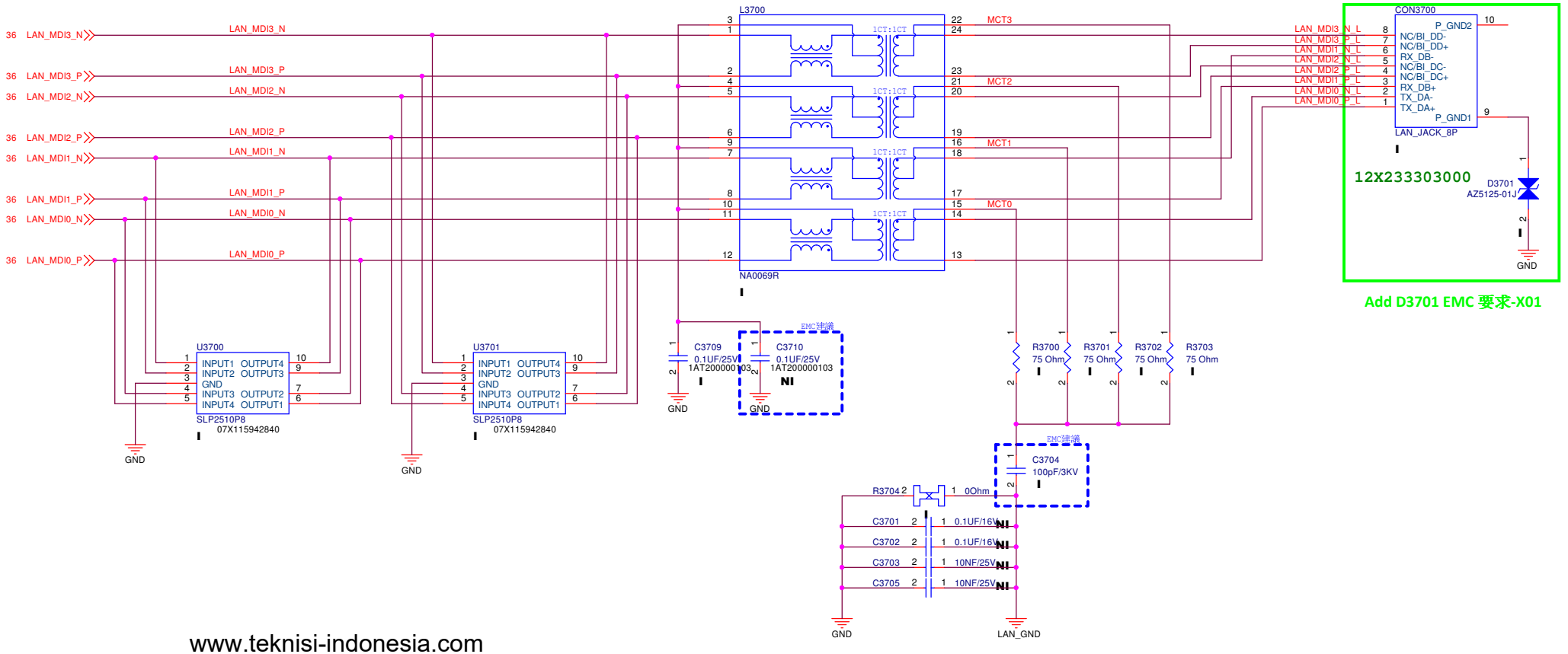
PEGATRON	Title : KEYBOARD	
Pegatron Corp.	Engineer: James_Liao	
Size: B	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 35 of 110	

36.KILLER LAN E2500V2



PEGATRON	Title : KILLER LAN E2500V2		
Pegatron Corp.	Engineer: James_Liao		
Size: A3	Project Name: HELA/N18E		Rev: X02
Date: Thursday, April 09, 2020	Sheet 36 of 110		

37.LAN JACK



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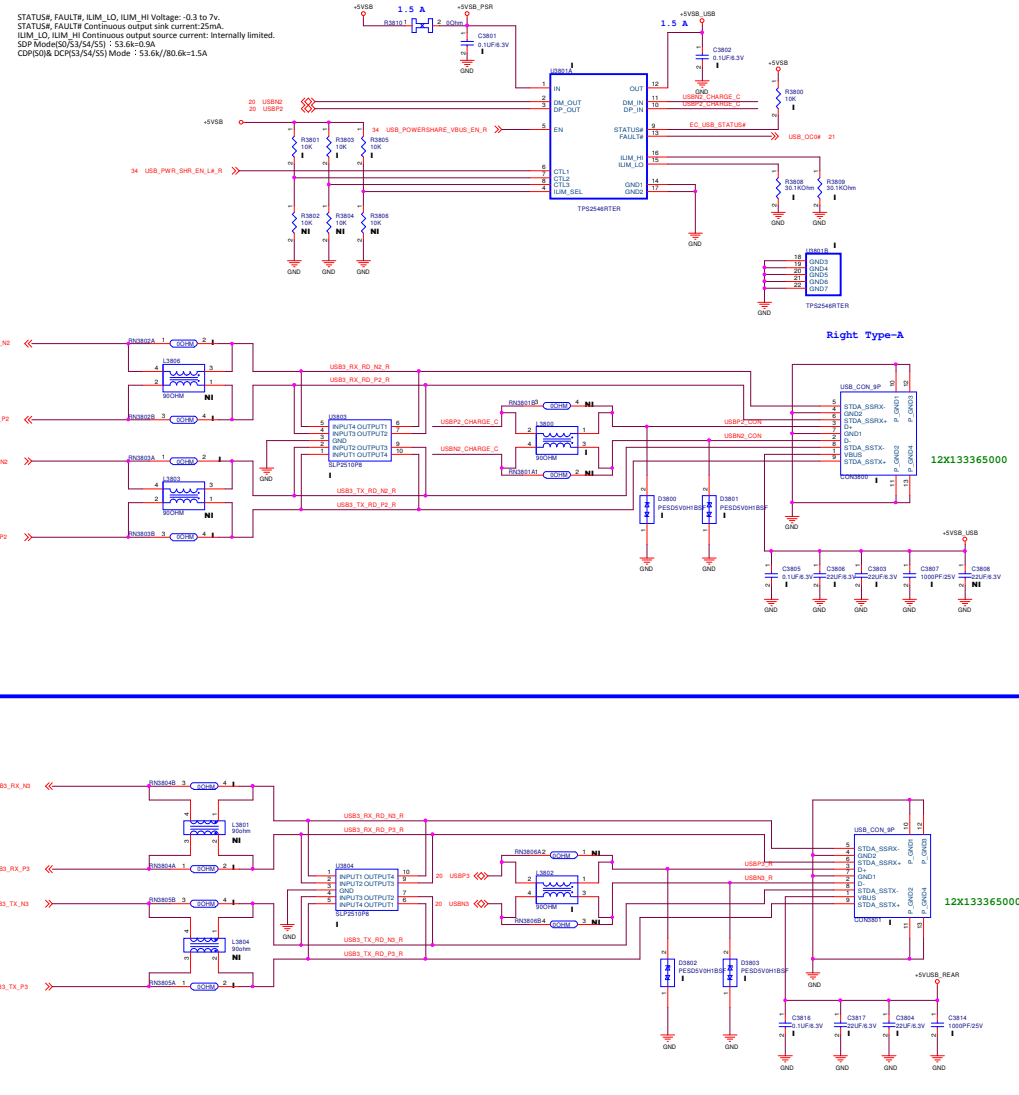
<Core Design>

PEGATRON	Title : LAN JACK	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 37 of 110	

38.USB CONN & POWER

Power Share



<Core Design>

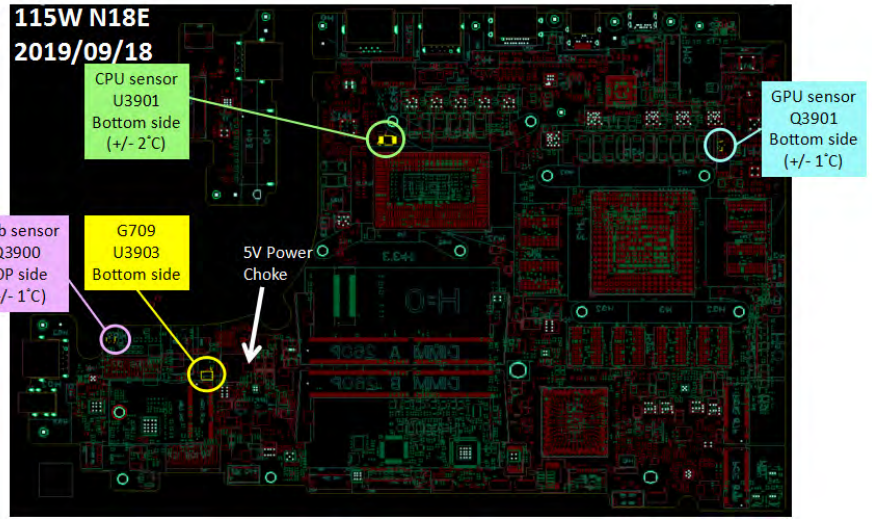
PEGATRON Title : USB CONN & POWER

Pegatron Corp. Engineer: James_Liao

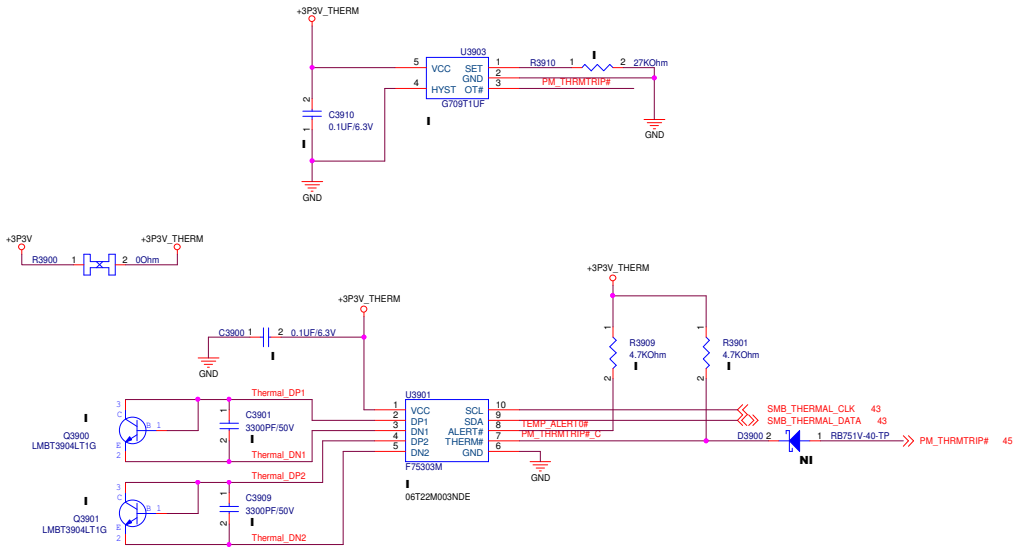
Size	Project Name	Rev
Custom	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 38 of 110

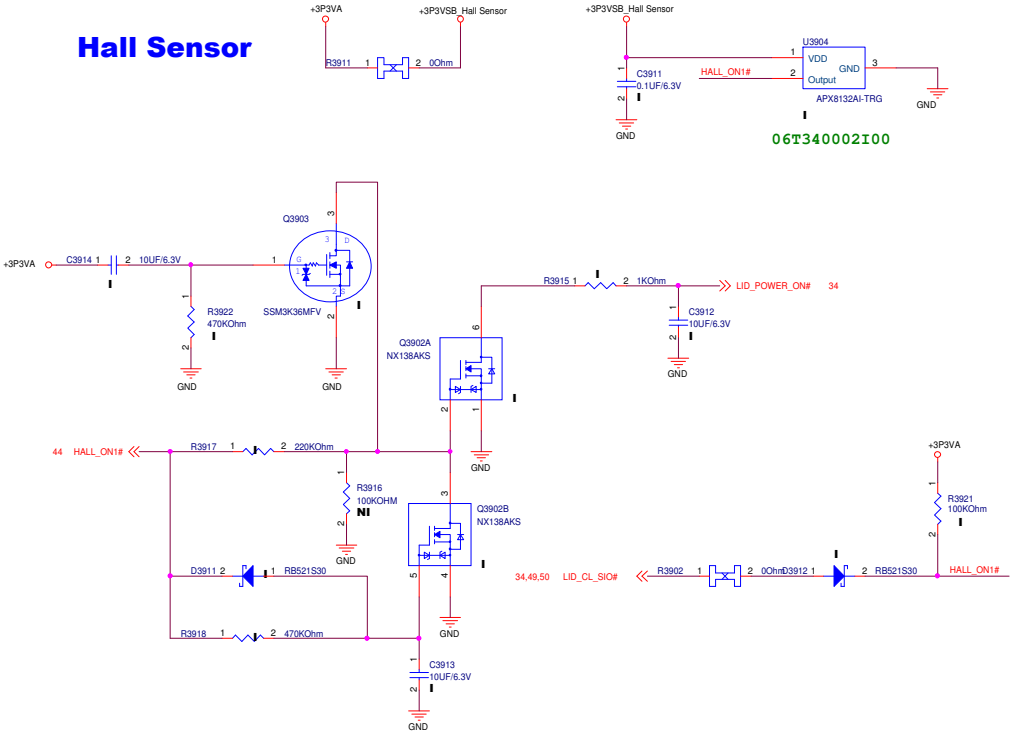
39. SENSOR



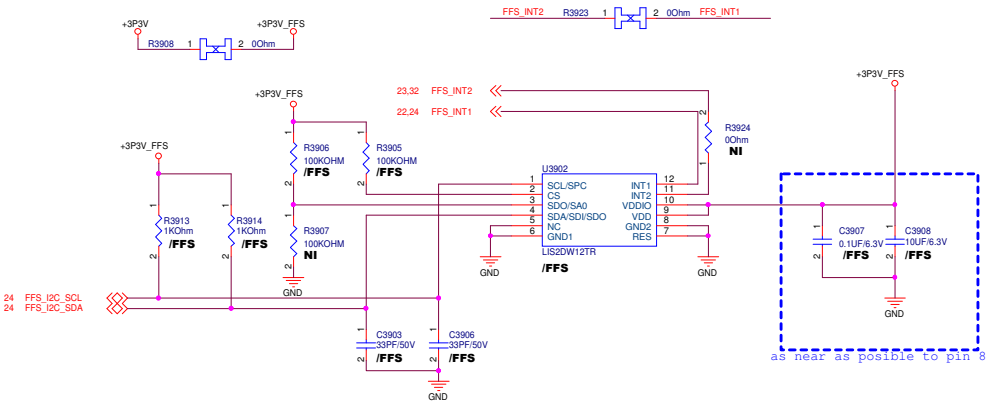
G709



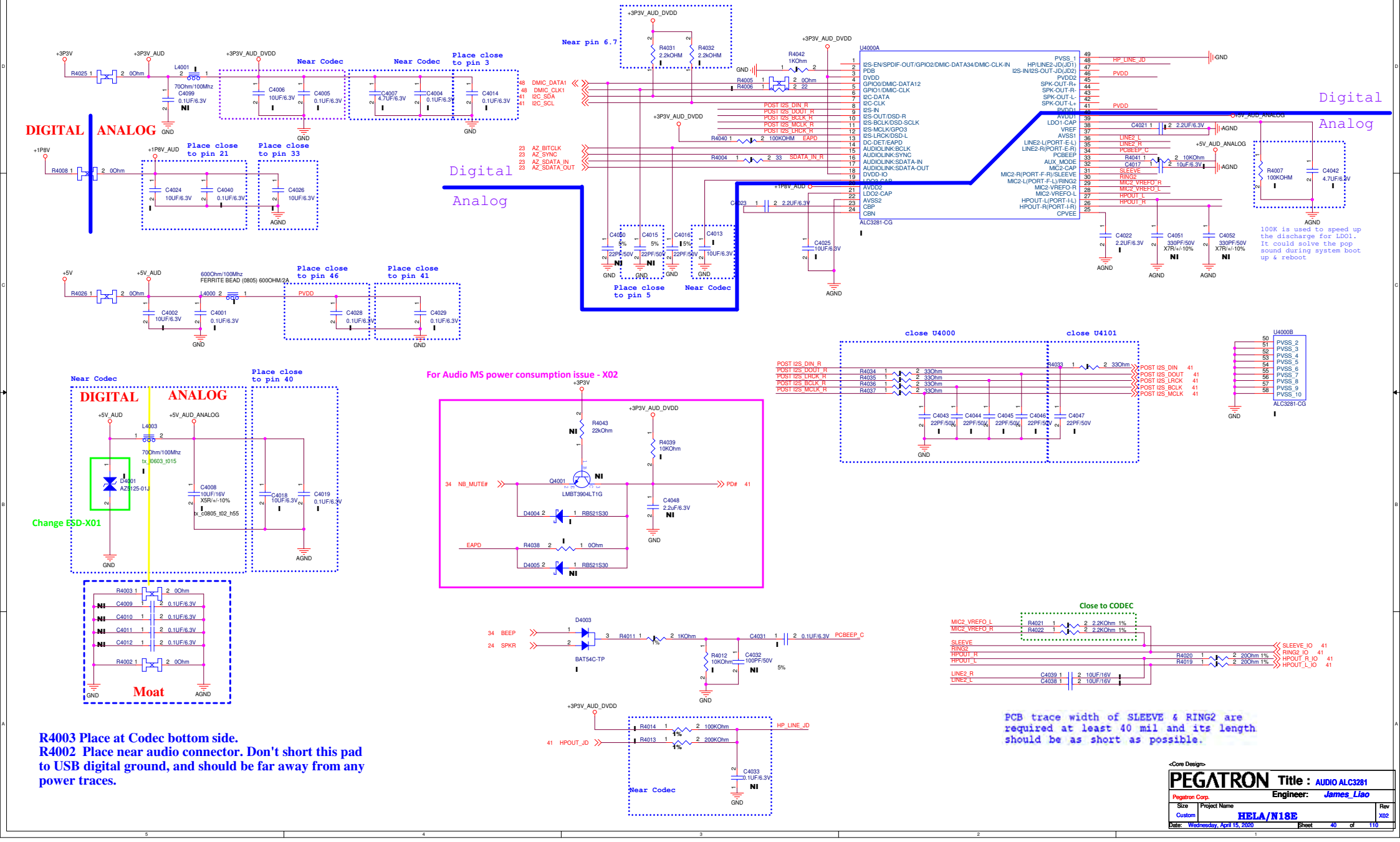
Hall Sensor



Free Fall Sensor



40.AUDIO CODEC- ALC3281



R4003 Place at Codec bottom side.
R4002 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

<Core Design>
PEGATRON Title : AUDIO ALC3281
Pegatron Corp. Engineer: James_Liao
Size: Custom | Project Name: HELA/N18E | Rev: X02
Date: Wednesday, April 15, 2020 | Sheet 40 of 110

41. AMP ALC1309_AUDIO JACK

GLOBAL HEADSET CONNECTOR

OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

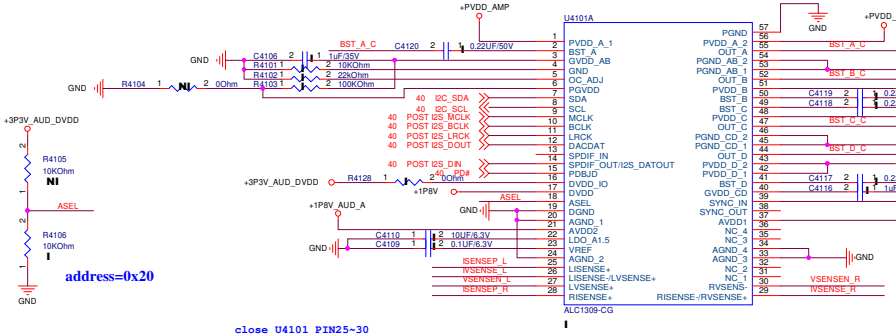
This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin. This kind of design will significantly improve the false detect caused by JD triggered timing

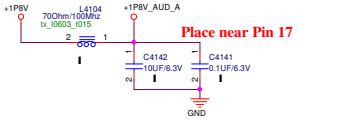
PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.

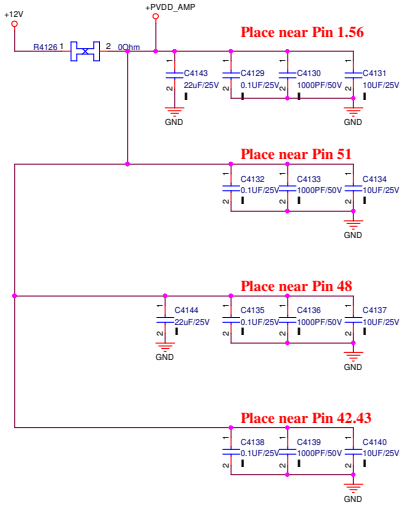
L4100/L4103 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

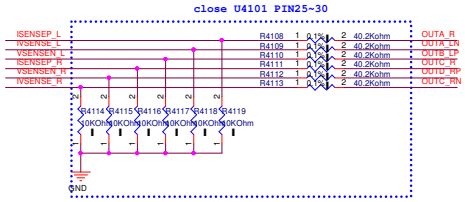
Stereo Output
(BTL Mode)

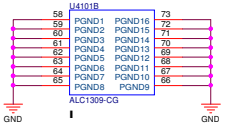
Power domain:
PVDD:6~26V
DVDD & AVDD2:1.8V
DVDD_IO:1.8V~3.3V

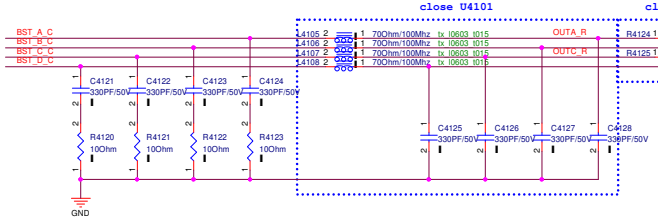


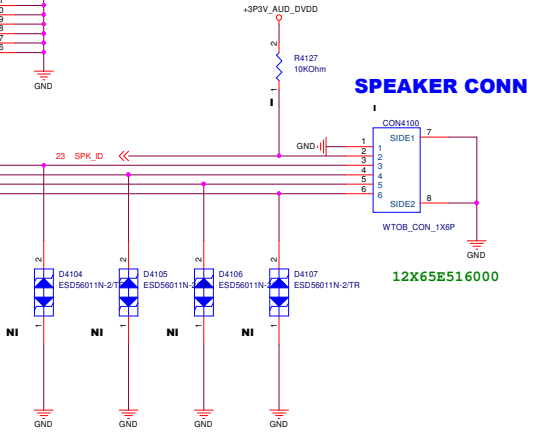


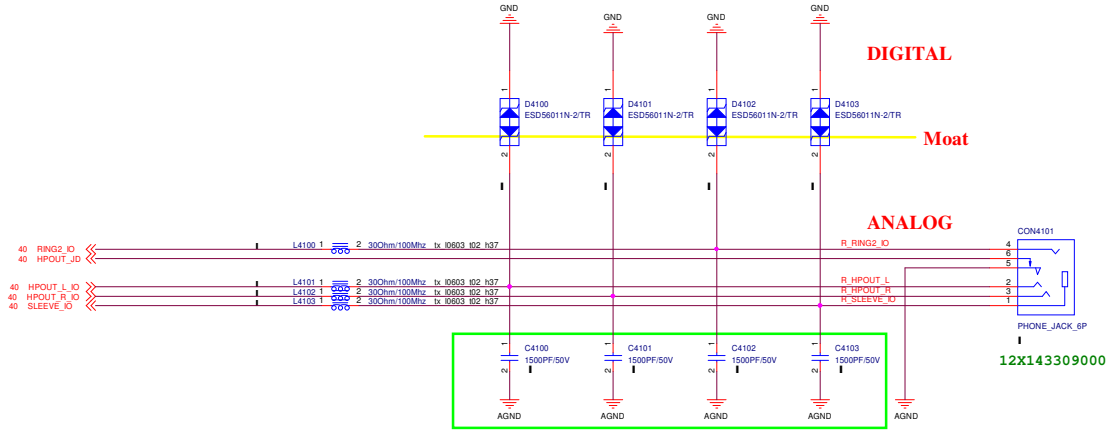












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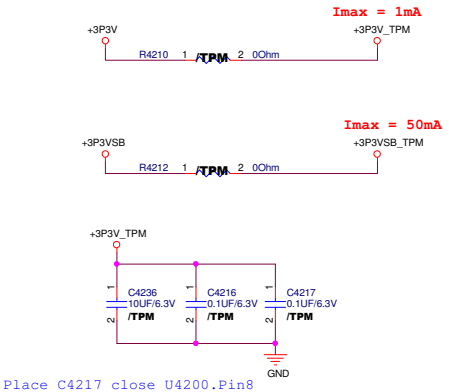
<Core Design>
PEGATRON Title : AUDIO JACK
Pegatron Corp. Engineer: James_Liao
Size A2 | Project Name HELA/N18E | Rev X02
Date: Thursday, April 09, 2020 Sheet 41 of 110

42. TPM



Place C4217 close U4200.Pin8

Place C4216 close U4200.Pin22
Place C4236 close U4202.Pin22

Place C4210 close U4200.Pin1
Place C4213 close U4200.Pin1

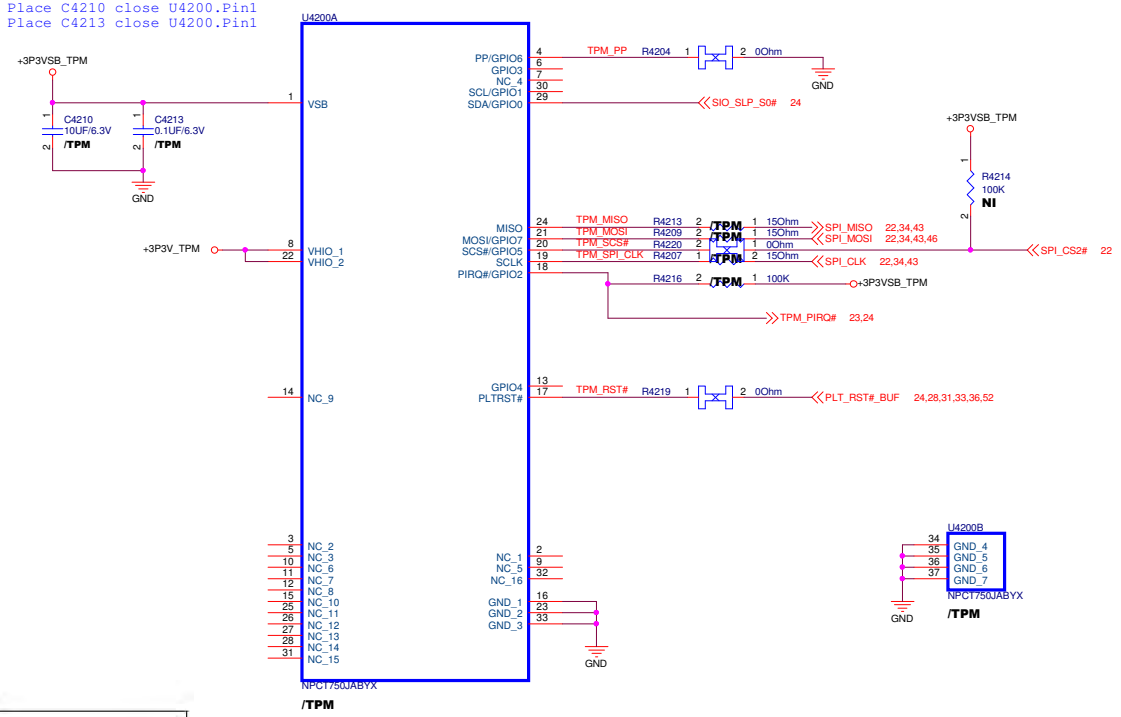
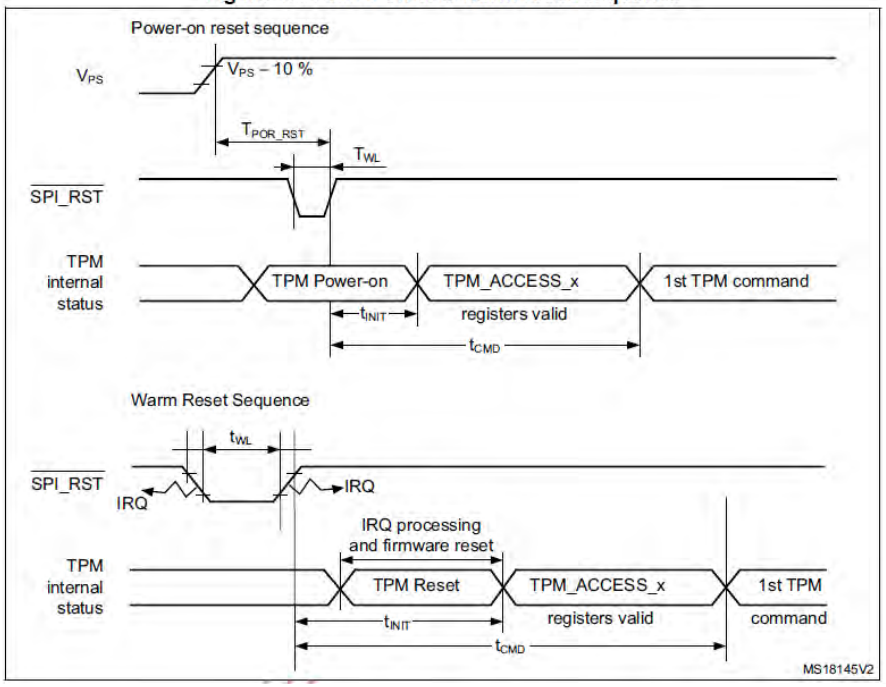


Figure 12. Power on and warm reset sequence



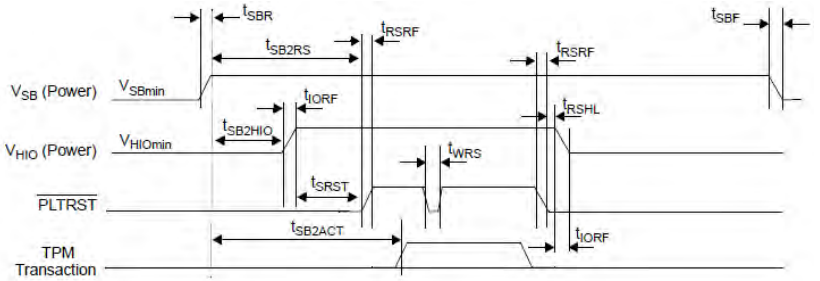
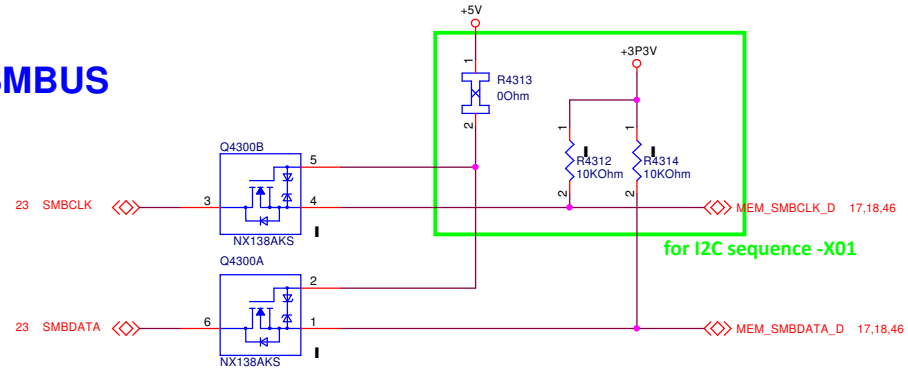


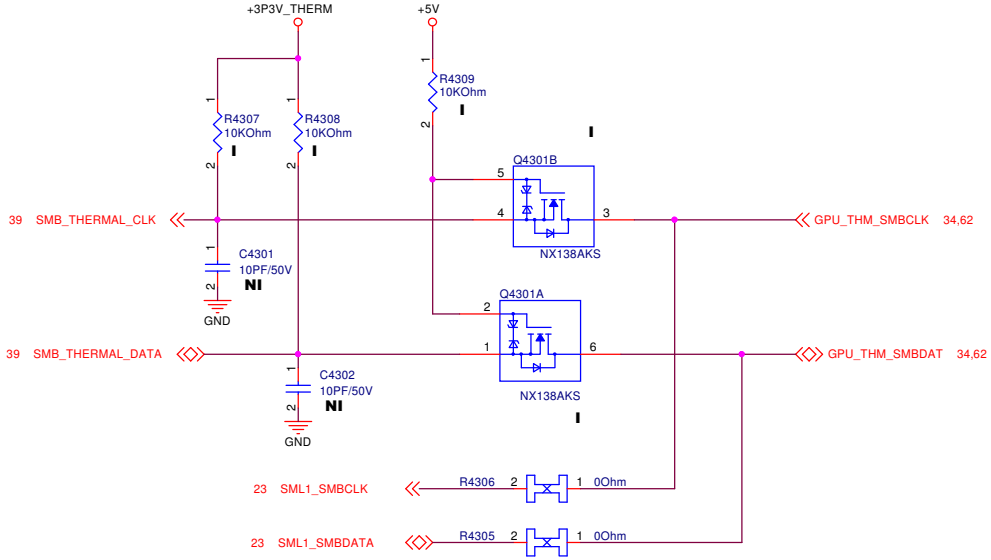
Figure 6. Power and Reset Timing Diagram

PEGATRON	Title : TPM	
Pegatron Corp.	Engineer: James_Liao	
Size: Custom	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 42 of 110	

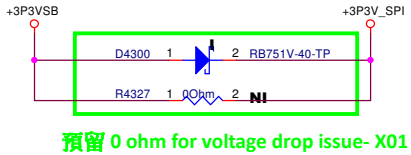
43.SM BUS & SPI ROM

SMBUS

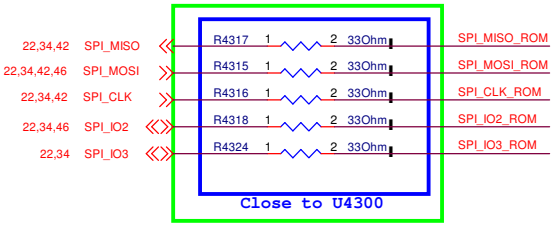




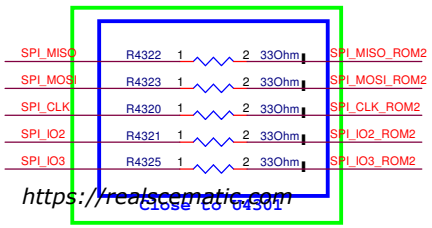
SPI ROM (Quad I/O Supported)



預留 0 ohm for voltage drop issue- X01



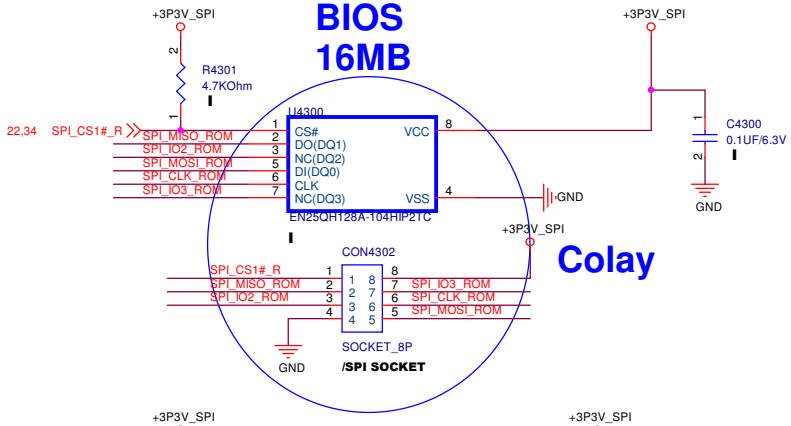
Follow PDG 15 ohm->33 ohm -X01



Follow PDG 15 ohm->33 ohm -X01

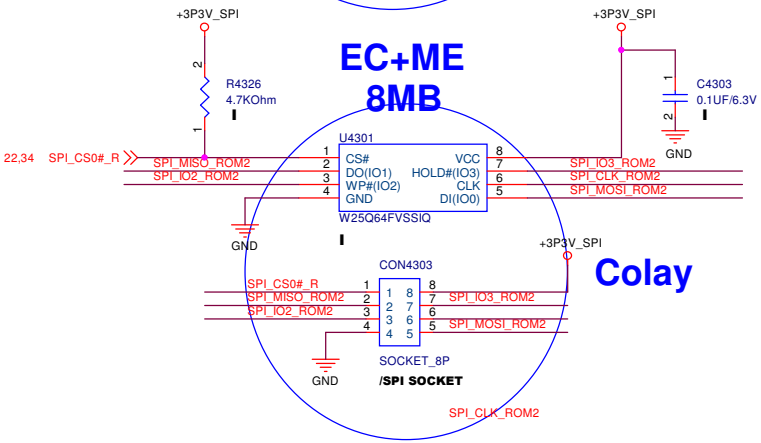
https://realschematic.com

BIOS 16MB

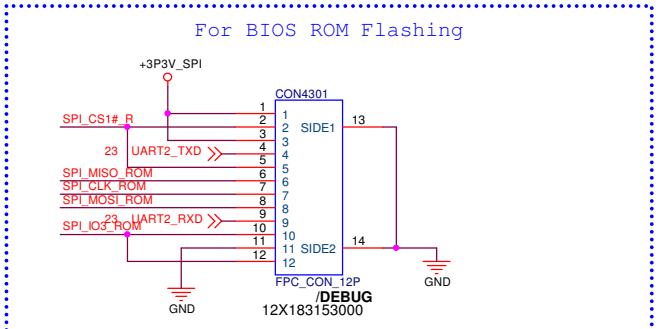


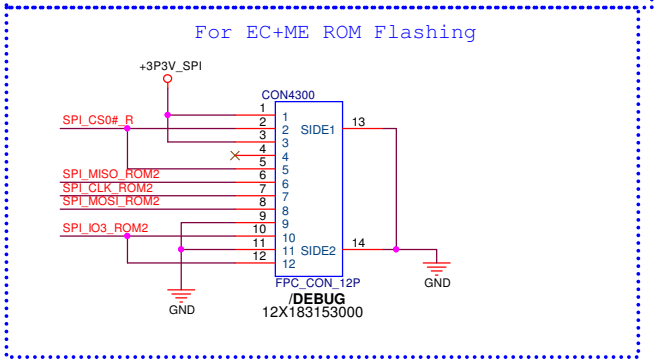
Colay

EC+ME 8MB



Colay

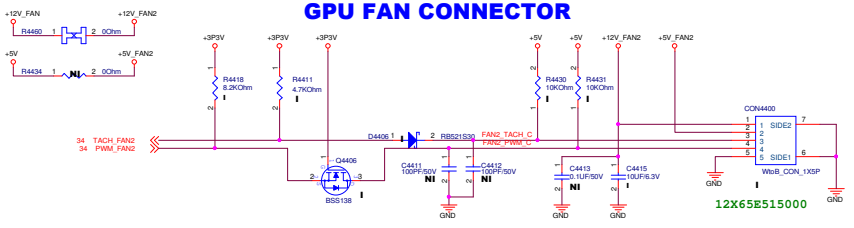




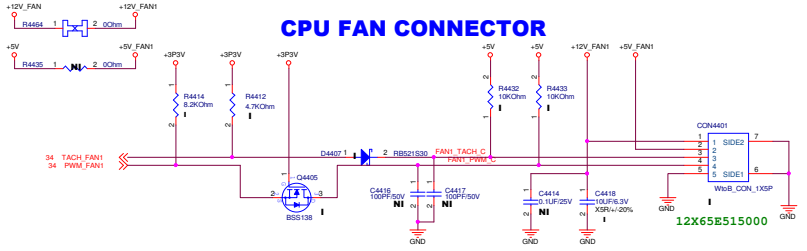
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	SM BUS & SPI ROM
Pegatron Corp.	Engineer:	James_Liao
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 43 of 110	

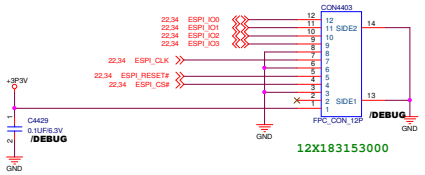
GPU FAN CONNECTOR



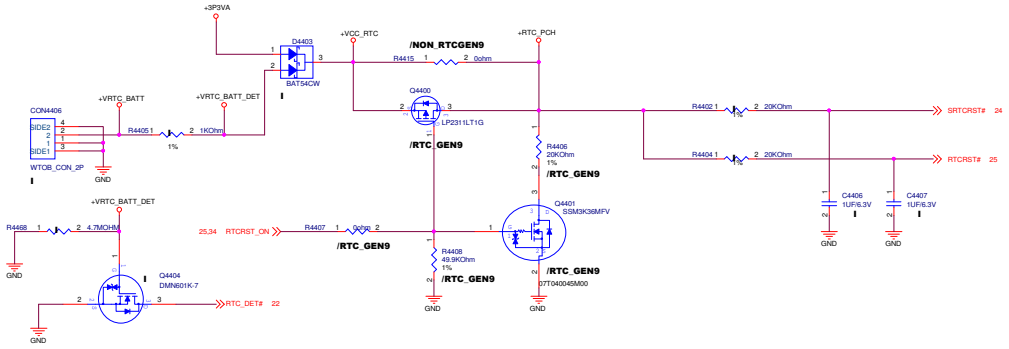
CPU FAN CONNECTOR



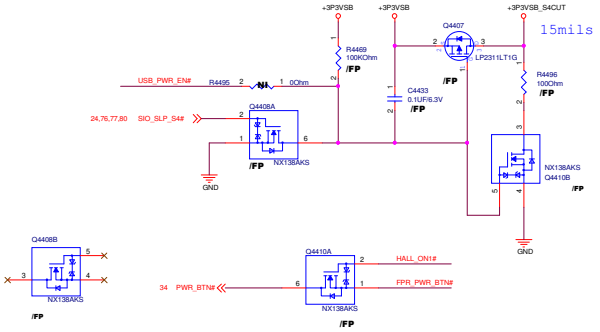
eSPI DEBUG PORT



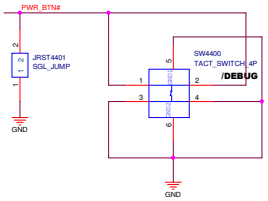
RTC CONN



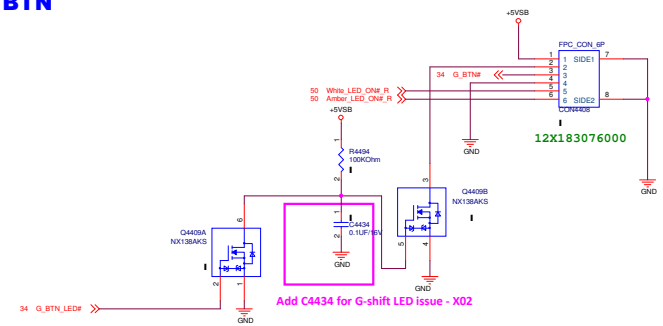
FPR CONNECTOR



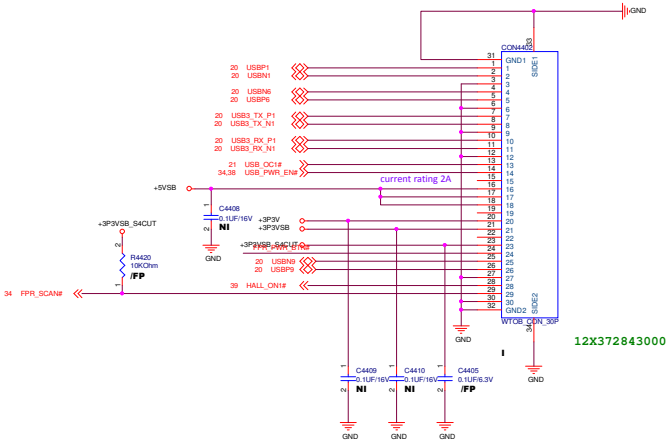
Power BTN



Game Shift



IO Board CON



PEGATRON Title : Other CONN

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

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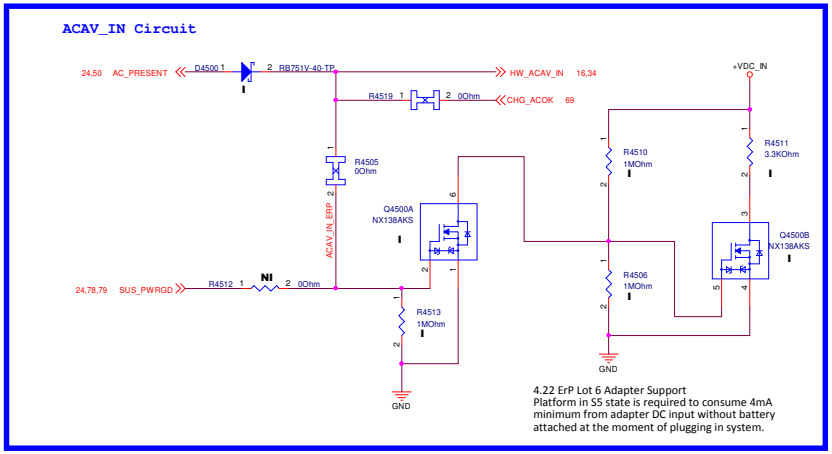
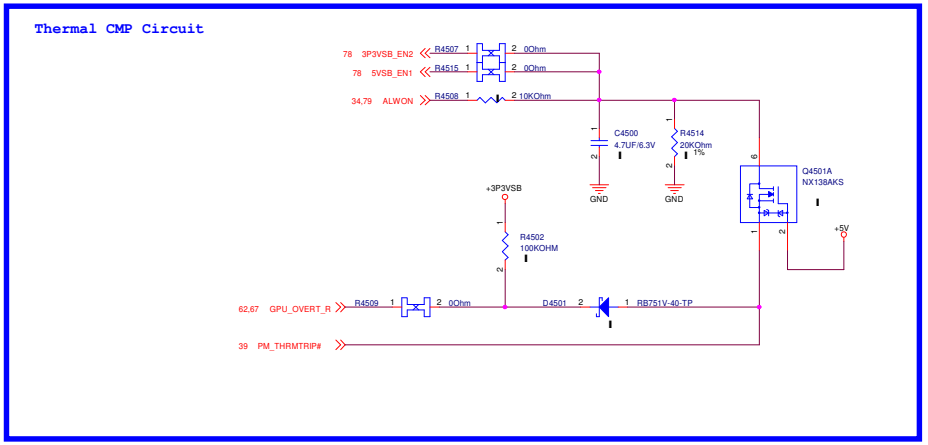
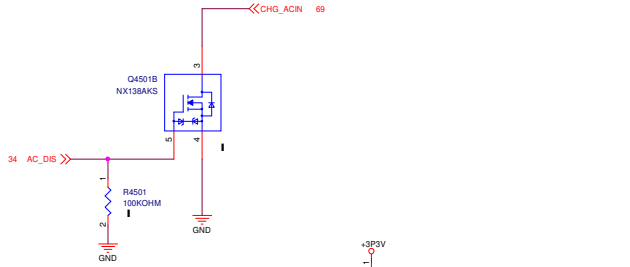
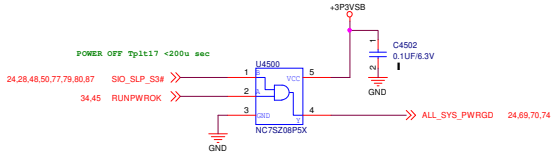
45. ACAV_IN

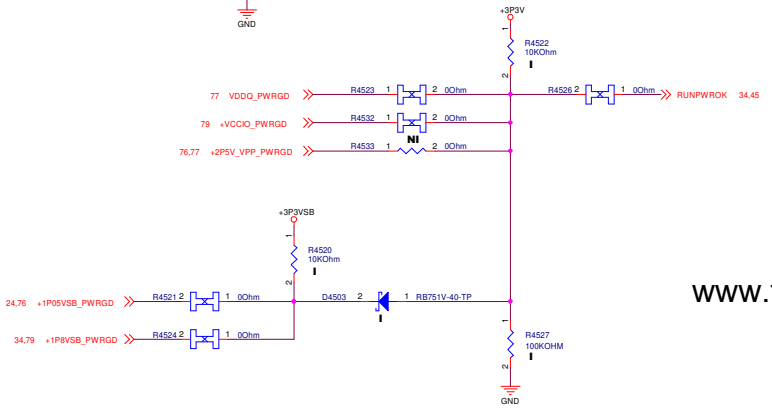




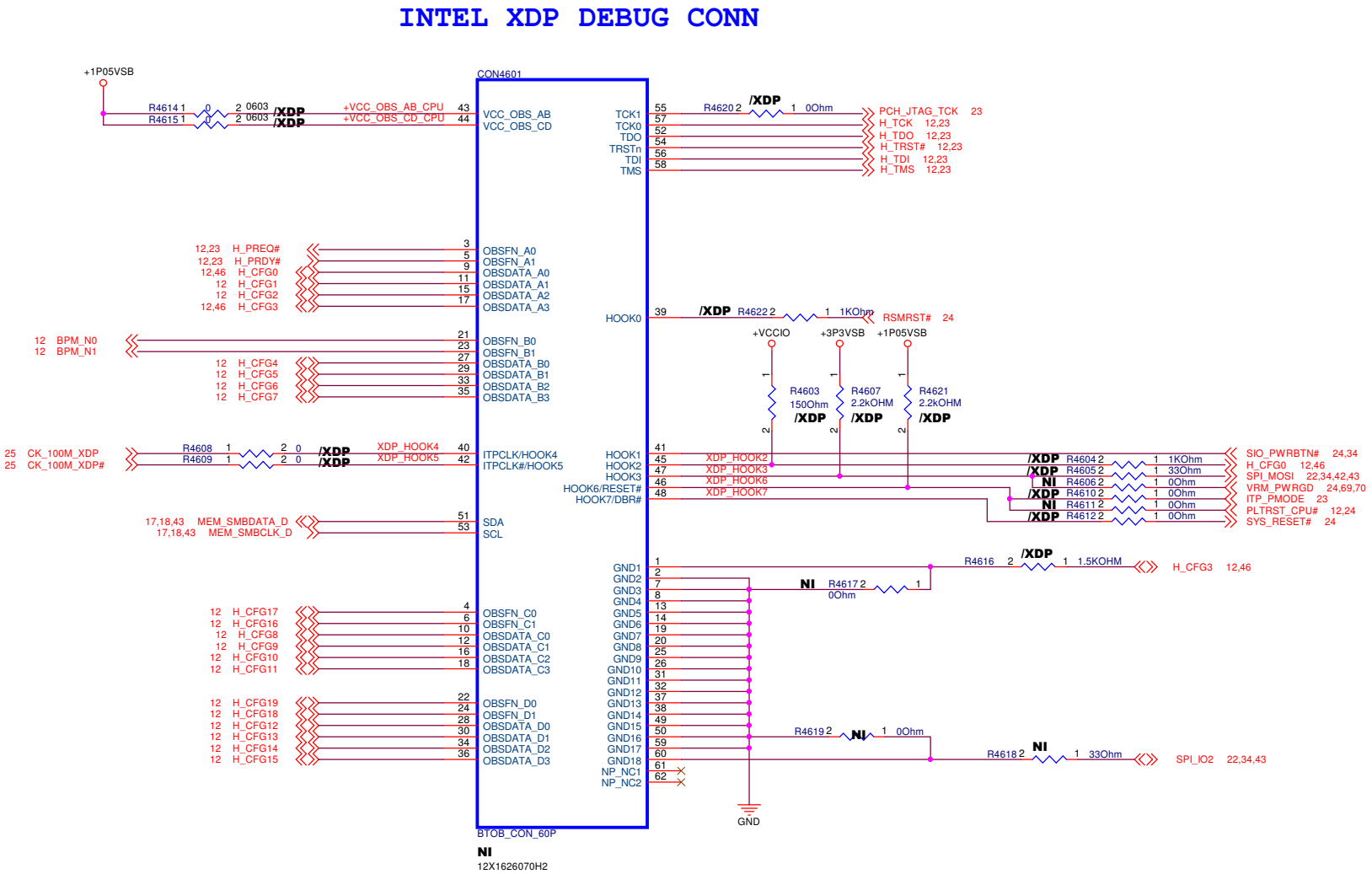


POWER GOOD DETECTER





46. INTEL XDP DEBUG CONN



PEGATRON	Title : XDP	
Pegatron Corp.	Engineer: James_Liao	
Size: A3	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 46 of 110	

A

H4701 1 CT276CB315D165 GND

H4736 1 CT276CB315D165 GND

H4702 1 CT276RB378X311D165 GND

B

H4712 1 C276D146 GND

H4713 1 C276D146 GND

H4714 1 C276D146 GND

H4715 1 C276D146 GND

H4716 1 C276D146 GND

H4717 1 C276D146 GND

H4718 1 C276D146 GND

H4719 1 C276D146 GND

C

H4706 1 RTB356x315D165 GND

F

H4733 1 CT276SB315D118 GND

I

H4731 1 CT276RB315x307D165 GND

D

H4721 1 O315x276DO236x197 GND

G

H4703 1 CT276RB295x394D98 GND

J

H4730 1 CT276RB329x315D98 GND

E

H4709 1 CT276CB315DO205x165 GND

H

H4704 1 CT276CB315D98 GND

K

H4729 1 CT276B315X311D98 GND

M

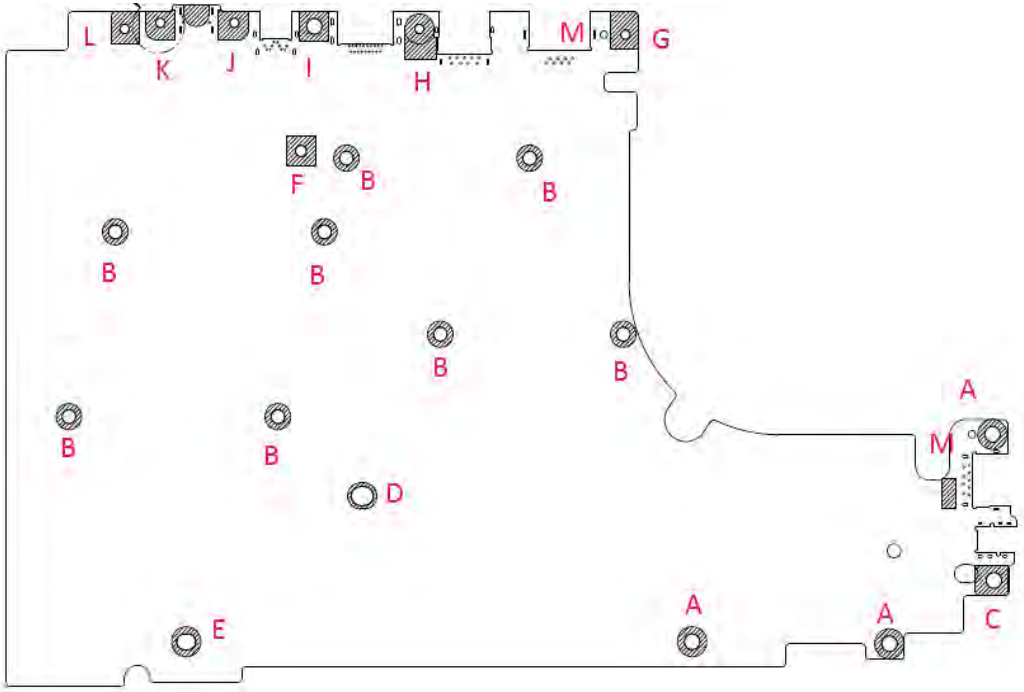
H4727 1 O79X91DO79X91N

H4737 1 C79D79N

H4732 1 DO252x193N

L

H4705 1 CT276RB303X335D98 GND



<Core Design>

PEGATRON Title : ME Screw

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
B	HELA/N18E	X02

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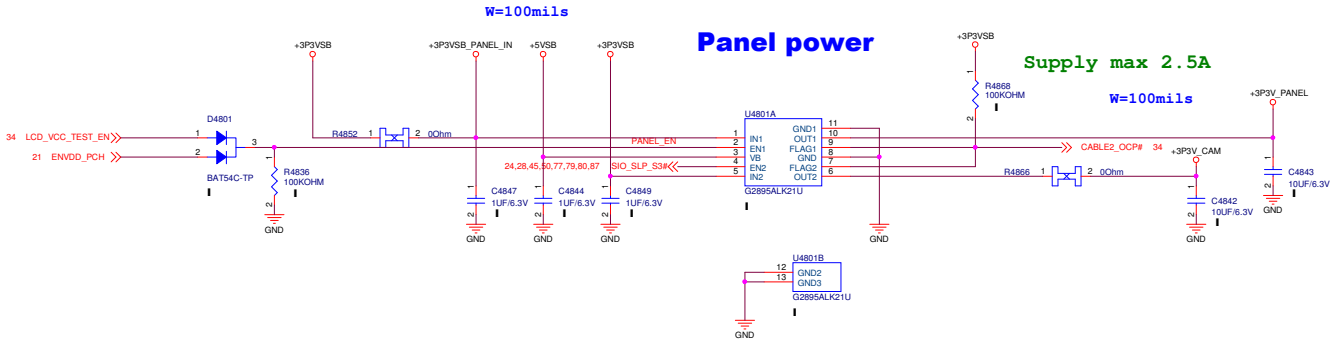
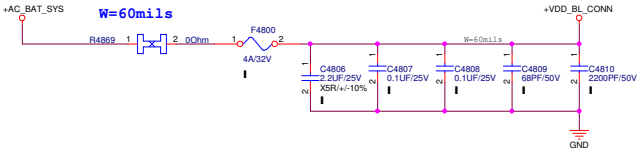
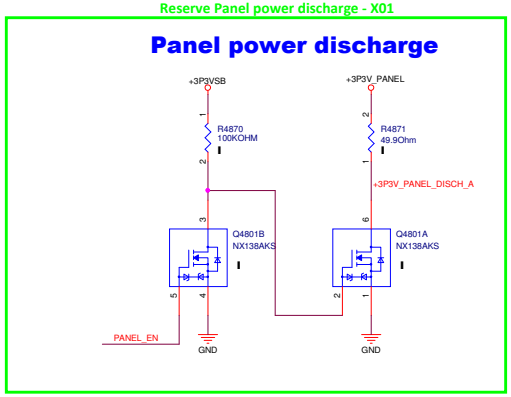
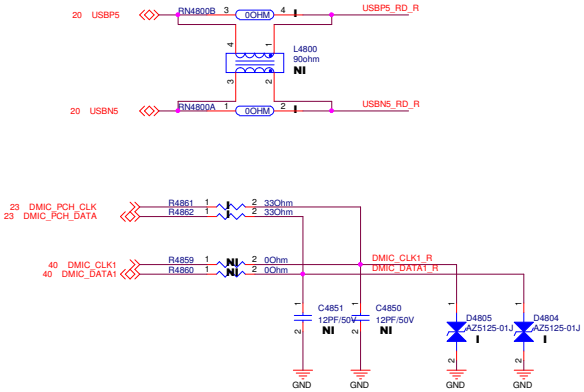
48.EDP CONN

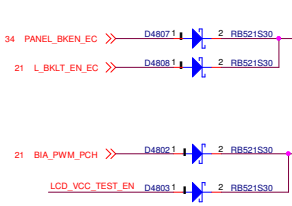


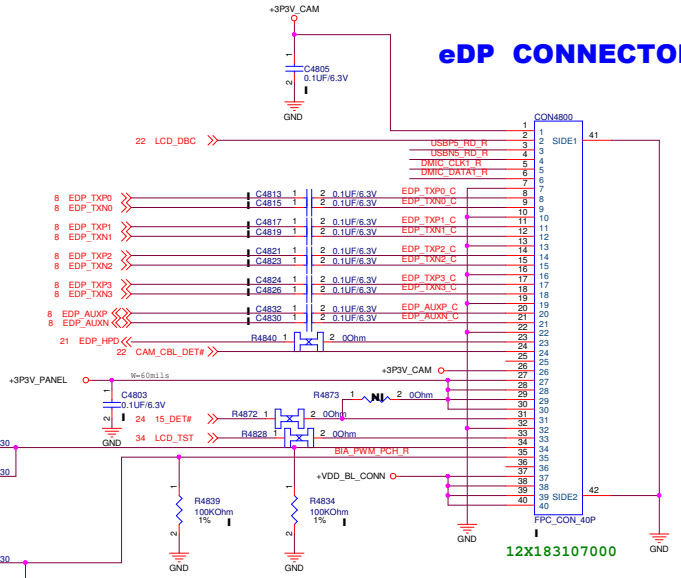


Reserve Panel power discharge - X01



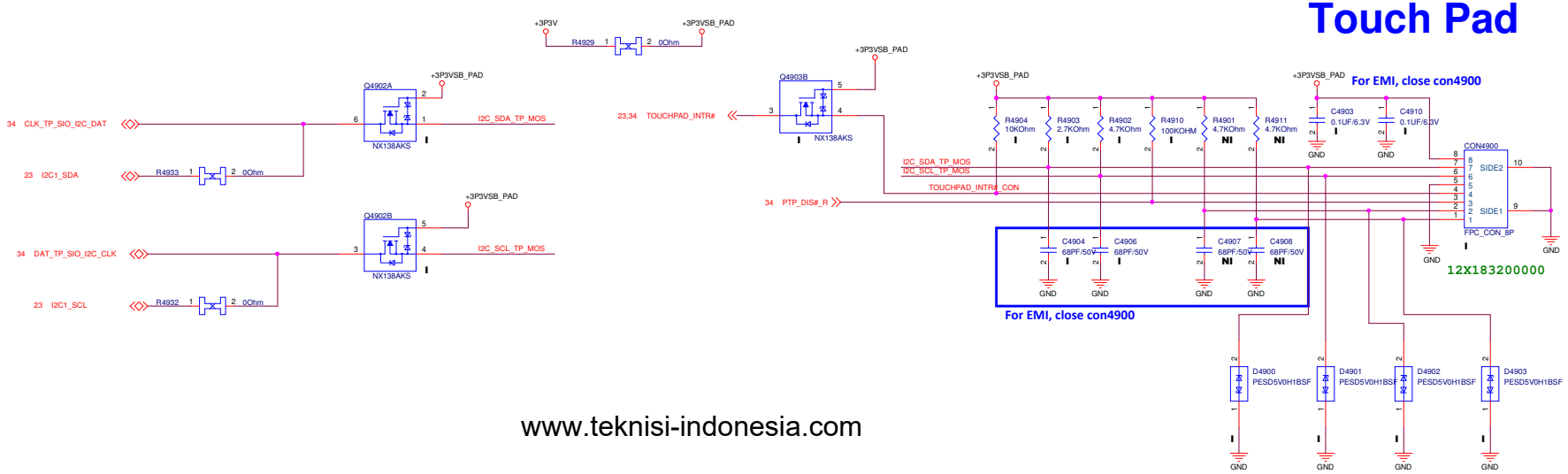






49. Touch & Keyboard BL

Touch Pad



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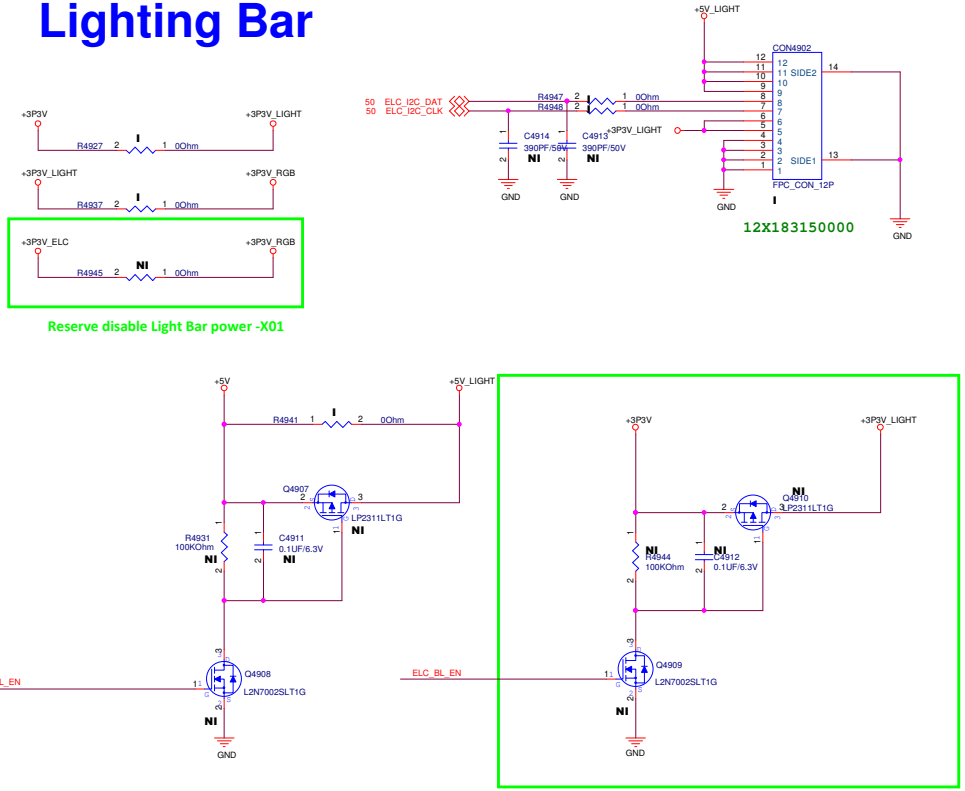
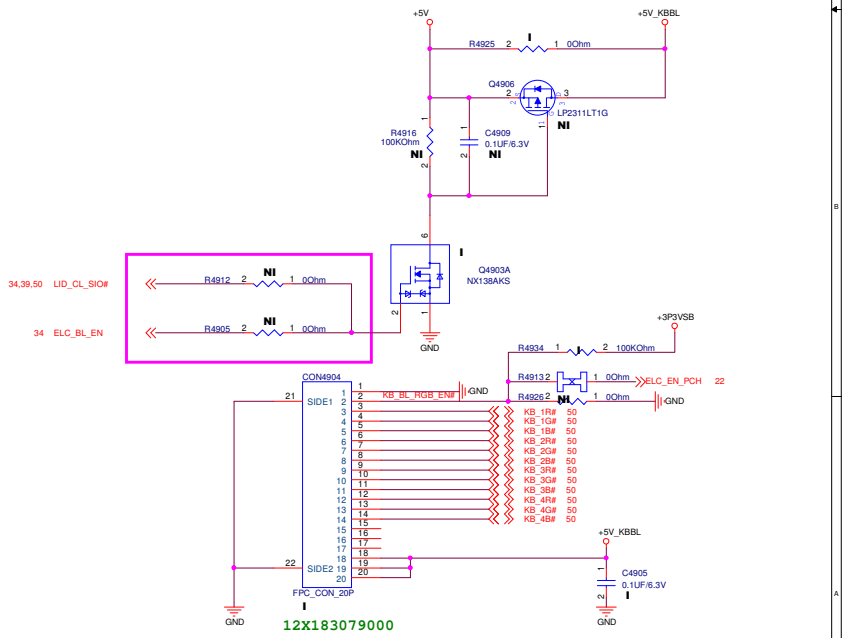
Lighting Bar



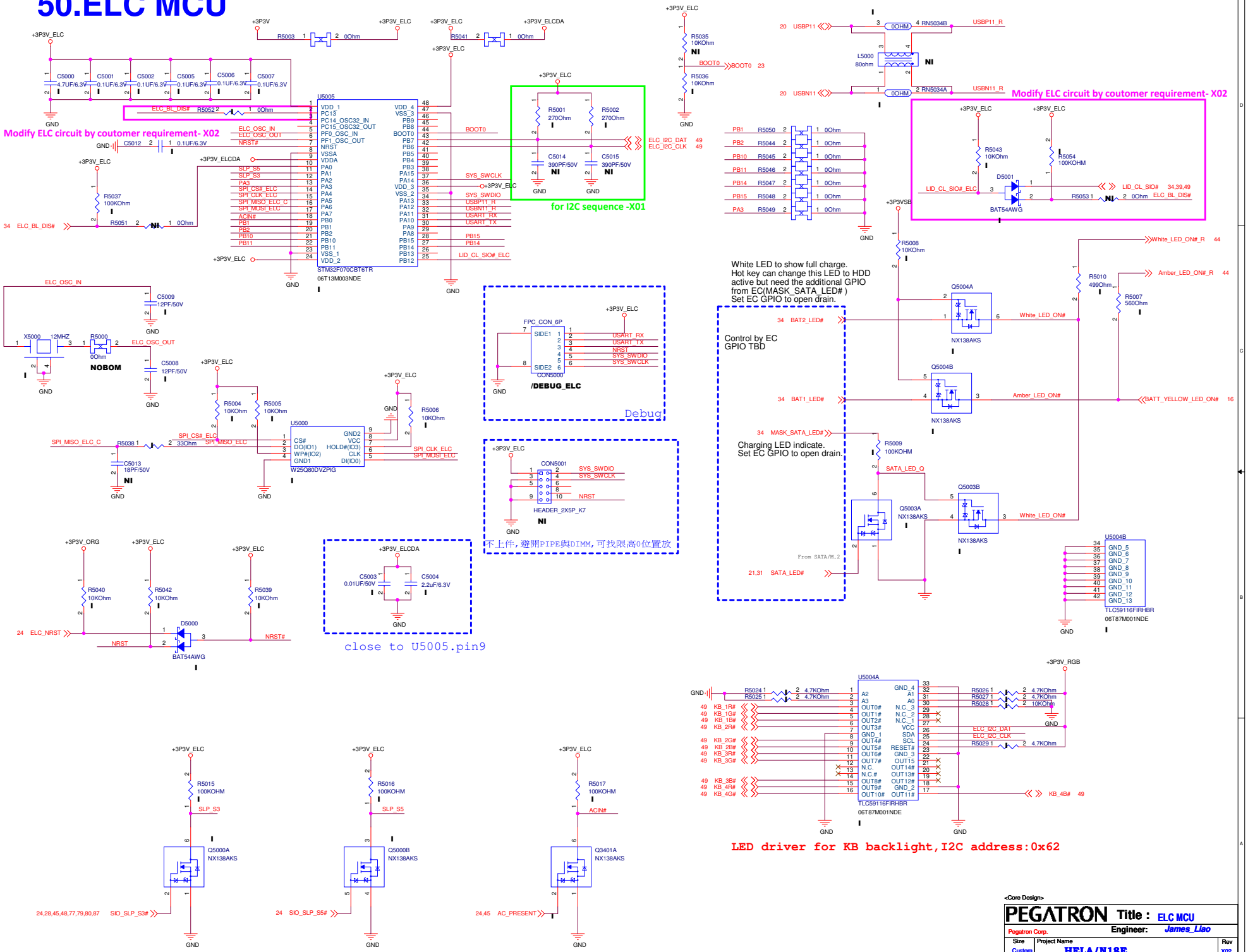
Keyboard backlight RGB



<Core Design>

PEGATRON	Title : Touch & Keyboard BL	
Pegatron Corp.	Engineer: James_Liao	
Size: Custom	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 49 of 110	

50.ELC MCU



<Core Design>

PEGATRON Title : ELC MCU

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

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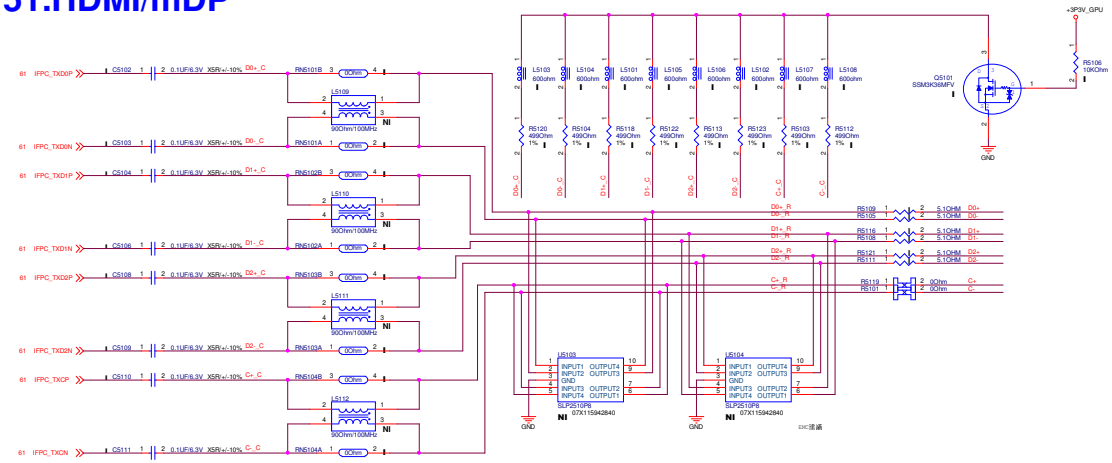
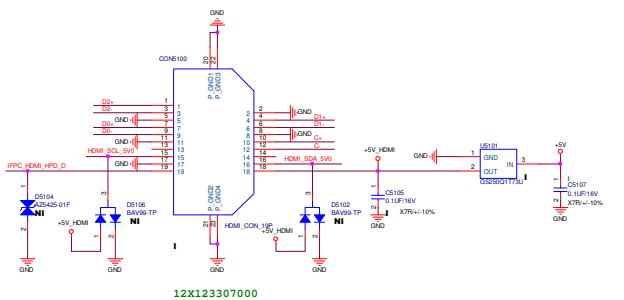
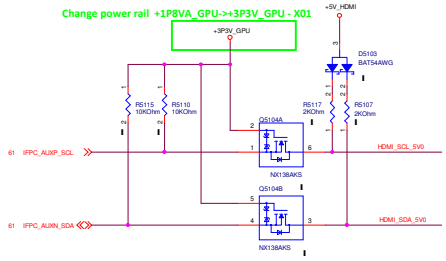
51.HDMI/mDP

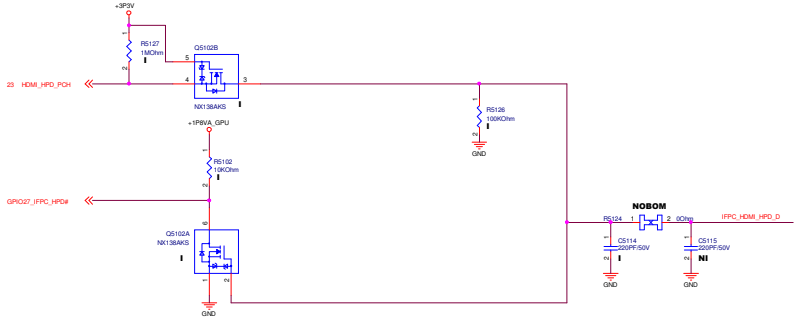


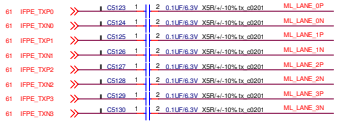
HDMI out connector

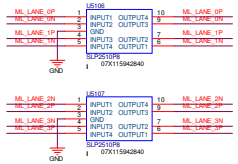


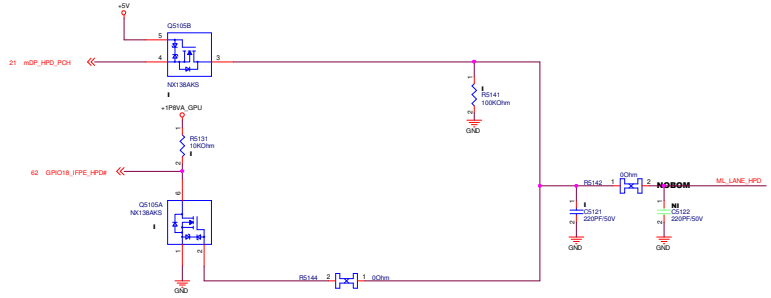
Change power rail +1P8VA_GPU->+3P3V_GPU - X01

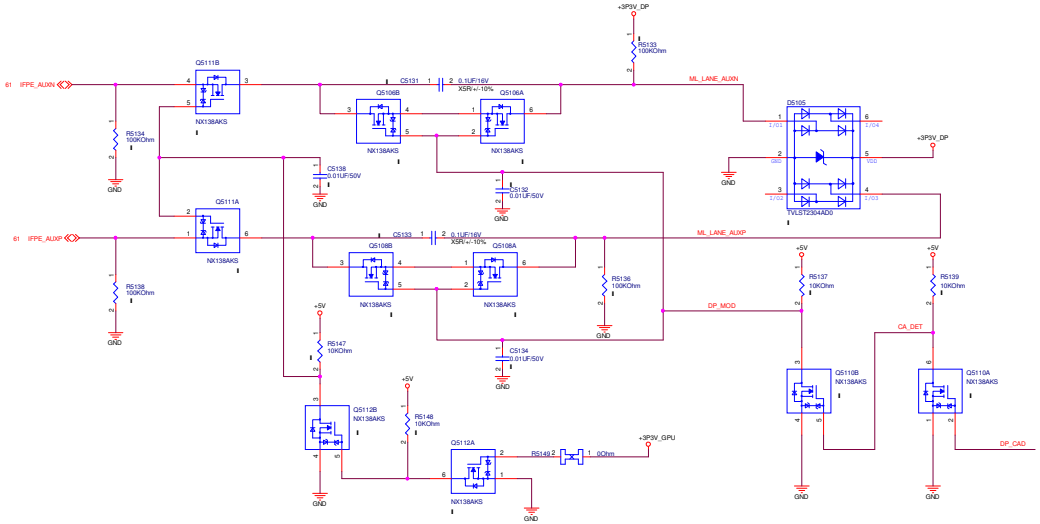




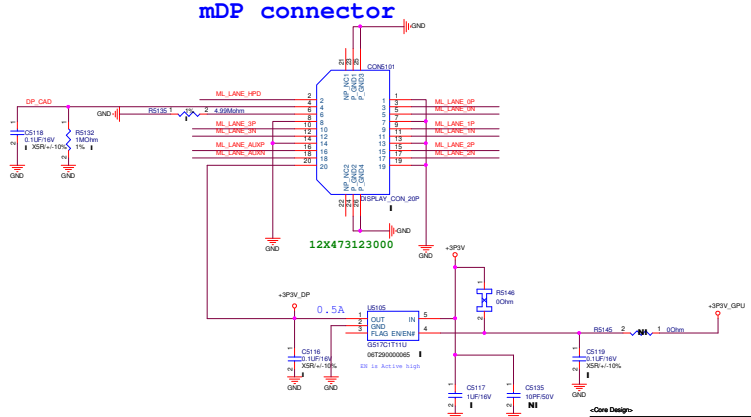








mDP connector



<Core Design>

PEGATRON Title : HDMI/mDP

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

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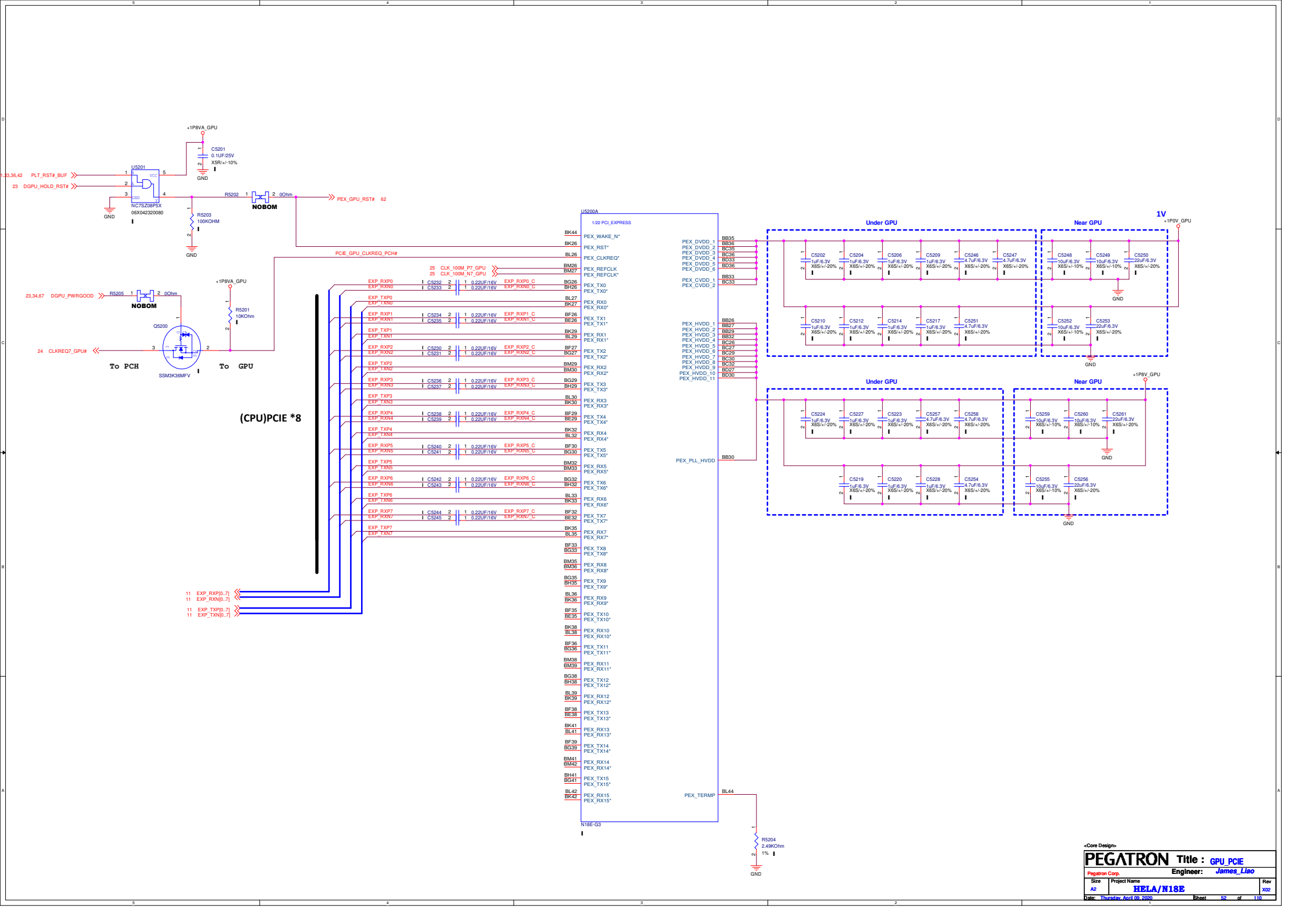
+1P8VA_GPU
C5201
0.1UF/25V
X5R/+/-10%
GND
U5201
NC7SZ08P5X
06X042320080
1,33,36,42 PLT_RST#_BUF
23 DGPU_HOLD_RST#
R5202 0Ohm
NOBOM
PEX_GPU_RST# 62
R5203
100KOHM
PCIE_GPU_CLKREQ_PCH#
23,34,67 DGPU_PWRGOOD
R5205 0Ohm
NOBOM
R5201
10KOhm
Q5200
SSM3K36MFV
24 CLKREQ7_GPU#
To PCH
To GPU
(CPU)PCIE *8
11 EXP_RXP[0..7]
11 EXP_RXN[0..7]
11 EXP_TXP[0..7]
11 EXP_TXN[0..7]
25 CLK_100M_P7_GPU
25 CLK_100M_N7_GPU
U5200A
1/22 PCI_EXPRESS
N18E-G3
PEX_WAKE_N*
PEX_RST*
PEX_CLKREQ*
PEX_REFCLK
PEX_REFCLK*
PEX_TX0
PEX_TX0*
PEX_RX0
PEX_RX0*
PEX_TX1
PEX_TX1*
PEX_RX1
PEX_RX1*
PEX_TX2
PEX_TX2*
PEX_RX2
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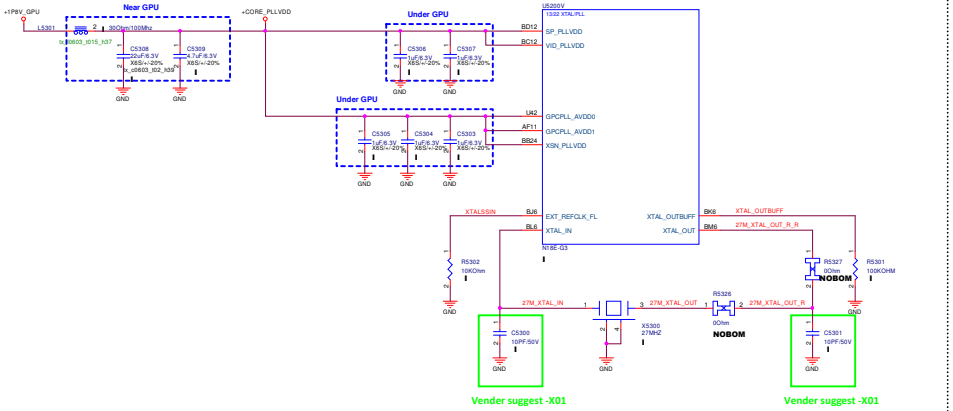
PEX_TX13*
PEX_RX13
PEX_RX13*
PEX_TX14
PEX_TX14*
PEX_RX14
PEX_RX14*
PEX_TX15
PEX_TX15*
PEX_RX15
PEX_RX15*
PEX_DVDD_1
PEX_DVDD_2
PEX_DVDD_3
PEX_DVDD_4
PEX_DVDD_5
PEX_DVDD_6
PEX_CVDD_1
PEX_CVDD_2
PEX_HVDD_1
PEX_HVDD_2
PEX_HVDD_3
PEX_HVDD_4
PEX_HVDD_5
PEX_HVDD_6
PEX_HVDD_7
PEX_HVDD_8
PEX_HVDD_9
PEX_HVDD_10
PEX_HVDD_11
PEX_PLL_HVDD
PEX_TERMP
R5204
2.49KOhm
1%
Under GPU
Near GPU
1V
+1P0V_GPU
+1P8V_GPU
C5202 1uF/6.3V X6S/+/-20%
C5204 1uF/6.3V X6S/+/-20%
C5206 1uF/6.3V X6S/+/-20%
C5209 1uF/6.3V X6S/+/-20%
C5246 4.7uF/6.3V X6S/+/-20%
C5247 4.7uF/6.3V X6S/+/-20%
C5248 10uF/6.3V X6S/+/-10%
C5249 10uF/6.3V X6S/+/-10%
C5250 22uF/6.3V X6S/+/-20%
C5210 1uF/6.3V X6S/+/-20%
C5212 1uF/6.3V X6S/+/-20%
C5214 1uF/6.3V X6S/+/-20%
C5217 1uF/6.3V X6S/+/-20%
C5251 4.7uF/6.3V X6S/+/-20%
C5252 10uF/6.3V X6S/+/-10%
C5253 22uF/6.3V X6S/+/-20%
C5224 1uF/6.3V X6S/+/-20%
C5227 1uF/6.3V X6S/+/-20%
C5223 1uF/6.3V X6S/+/-20%
C5257 4.7uF/6.3V X6S/+/-20%
C5258 4.7uF/6.3V X6S/+/-20%
C5259 10uF/6.3V X6S/+/-10%
C5260 10uF/6.3V X6S/+/-10%
C5261 22uF/6.3V X6S/+/-20%
C5219 1uF/6.3V X6S/+/-20%
C5220 1uF/6.3V X6S/+/-20%
C5228 1uF/6.3V X6S/+/-20%
C5254 4.7uF/6.3V X6S/+/-20%
C5255 10uF/6.3V X6S/+/-10%
C5256 22uF/6.3V X6S/+/-20%
GND
<Core Design>
PEGATRON
Title : GPU_PCIE
Pegatron Corp.
Engineer: James_Liao
Size A2
Project Name HELA/N18E
Rev X02
Date: Thursday, April 09, 2020
Sheet 52 of 110



Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED
all other configurations			(Reserved; do not configure) (Invalid; do not configure)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

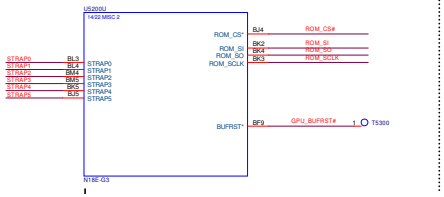
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

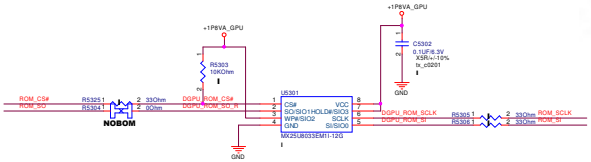
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

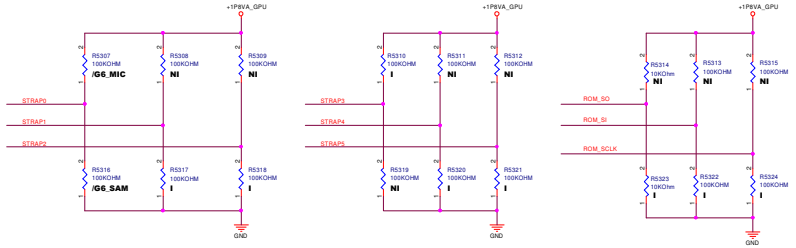
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Straps





GPU VRAM STRAP



Strap2,1,0, please check memory RVL

NON-GSYNC --> DEVID_SEL is 0
GSYNC --> DEVID_SEL is 1

Table 7. N18E-G0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production ready
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production ready

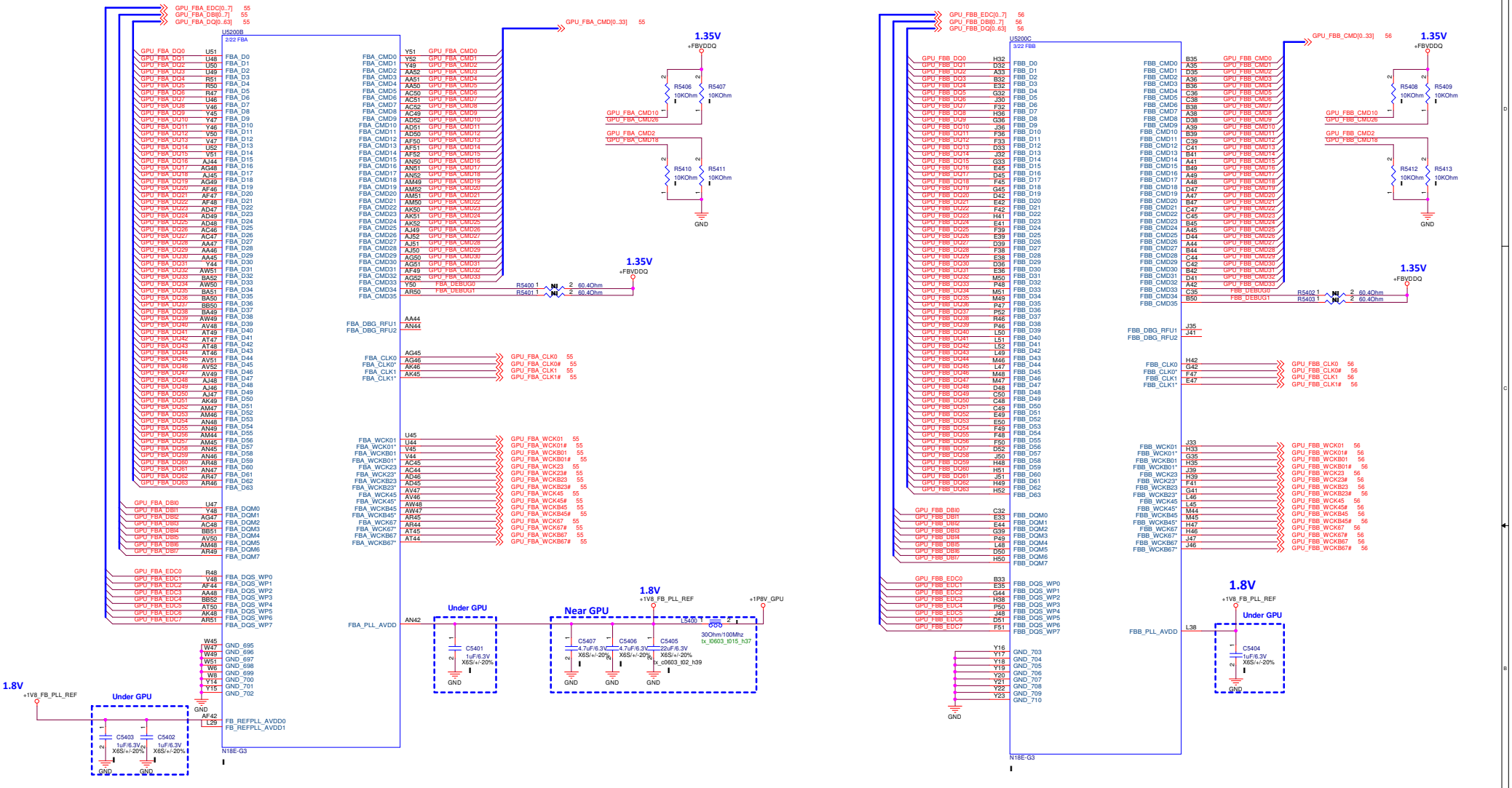
Table 6. N18E-G1R GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[4]	Full	Production candidate

Table 4. N18E-G2R GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[4]	Full	Production candidate

PEGATRON Title : GPU-Xtal & Straps
Pegatron Corp. Engineer: James_Liao
Size: Custom | Project Name: HELA/N18E | Rev: X02
Date: Thursday, April 09, 2020 Sheet 53 of 110



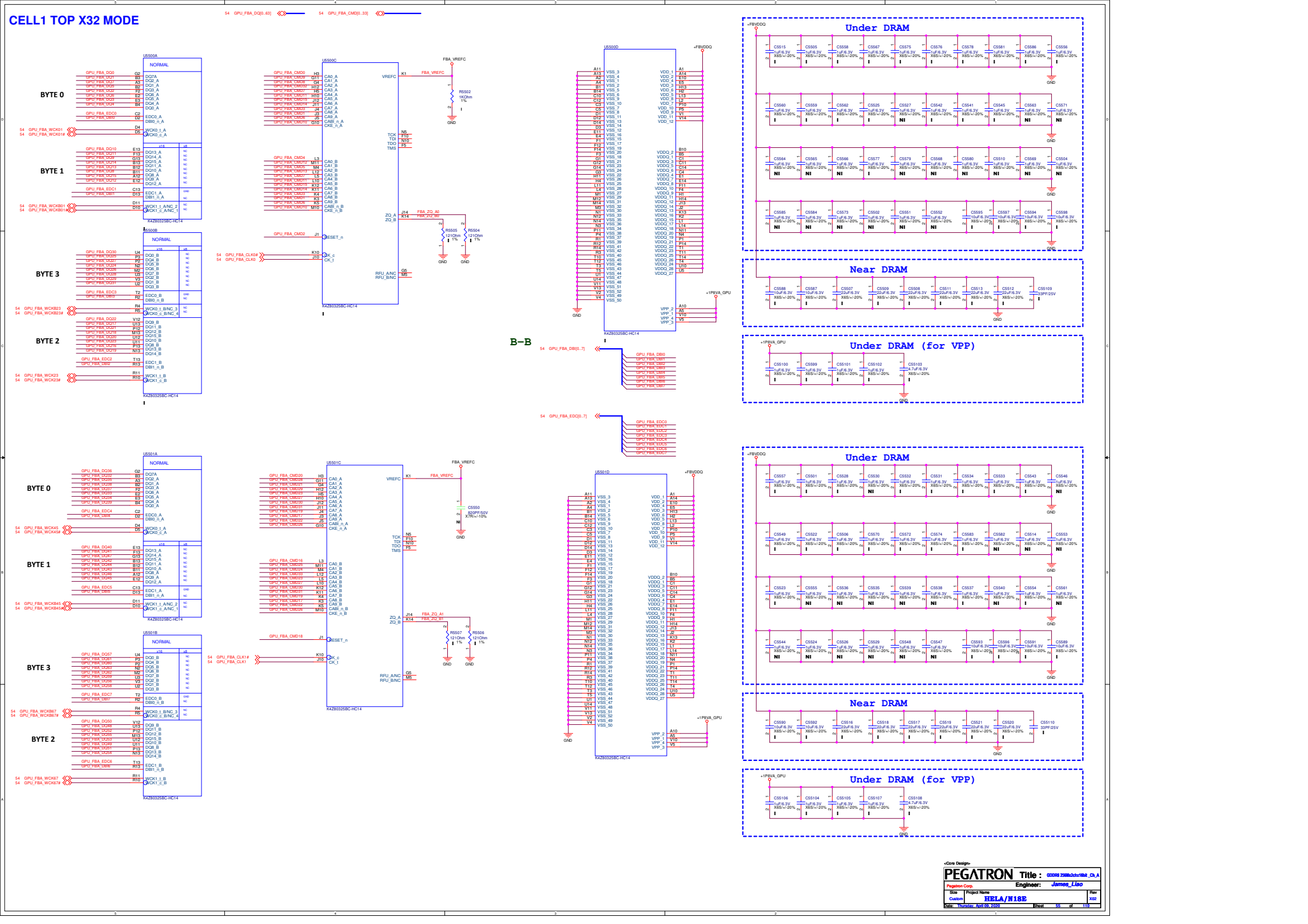
PEGATRON Title : GPU-BUFFER PARTITION A/B

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A2	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 54 of 110

CELL1 TOP X32 MODE



<Core Design>

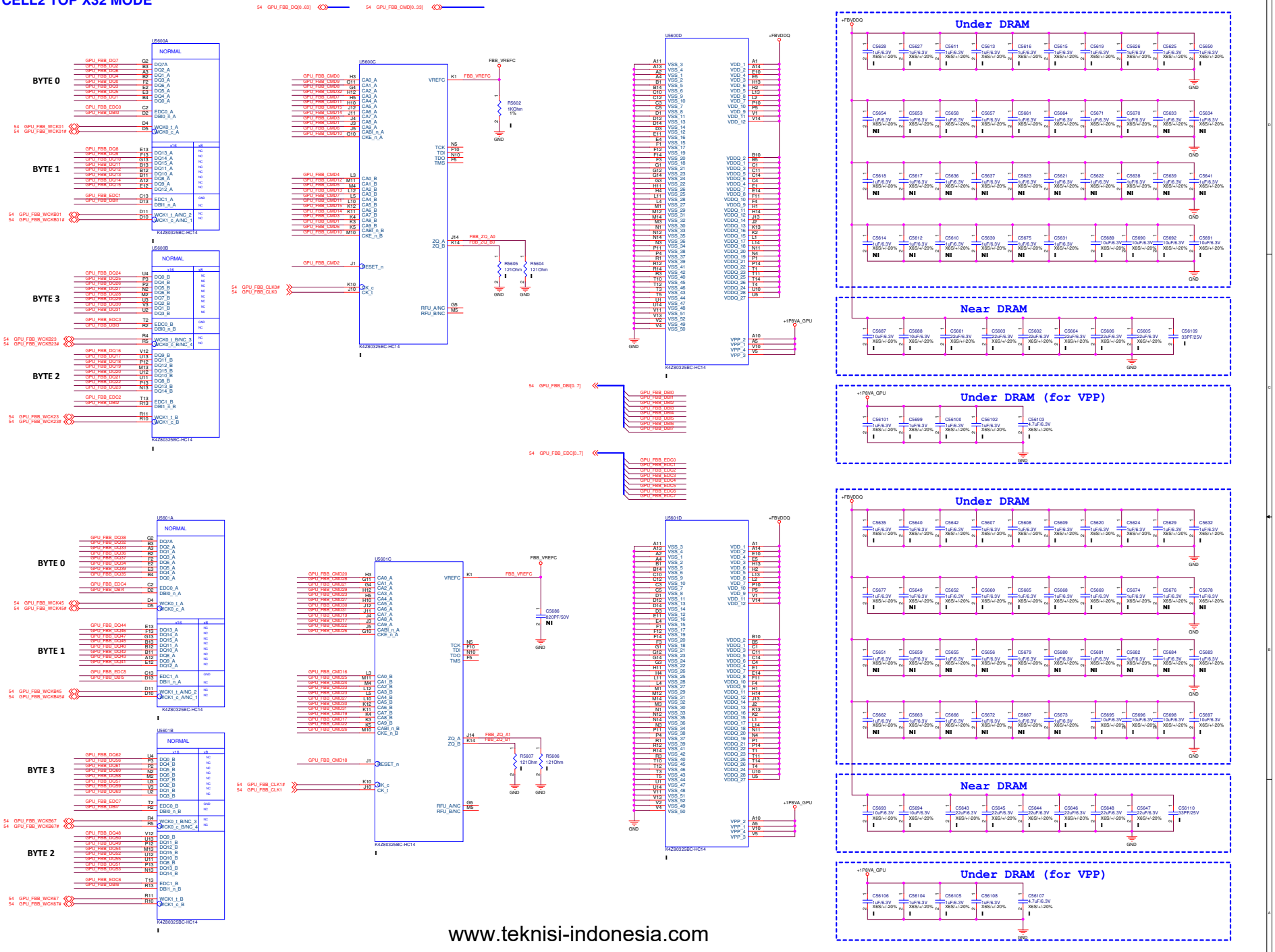
PEGATRON Title : GDDR6 256Mx2chx16bit_Ch_A

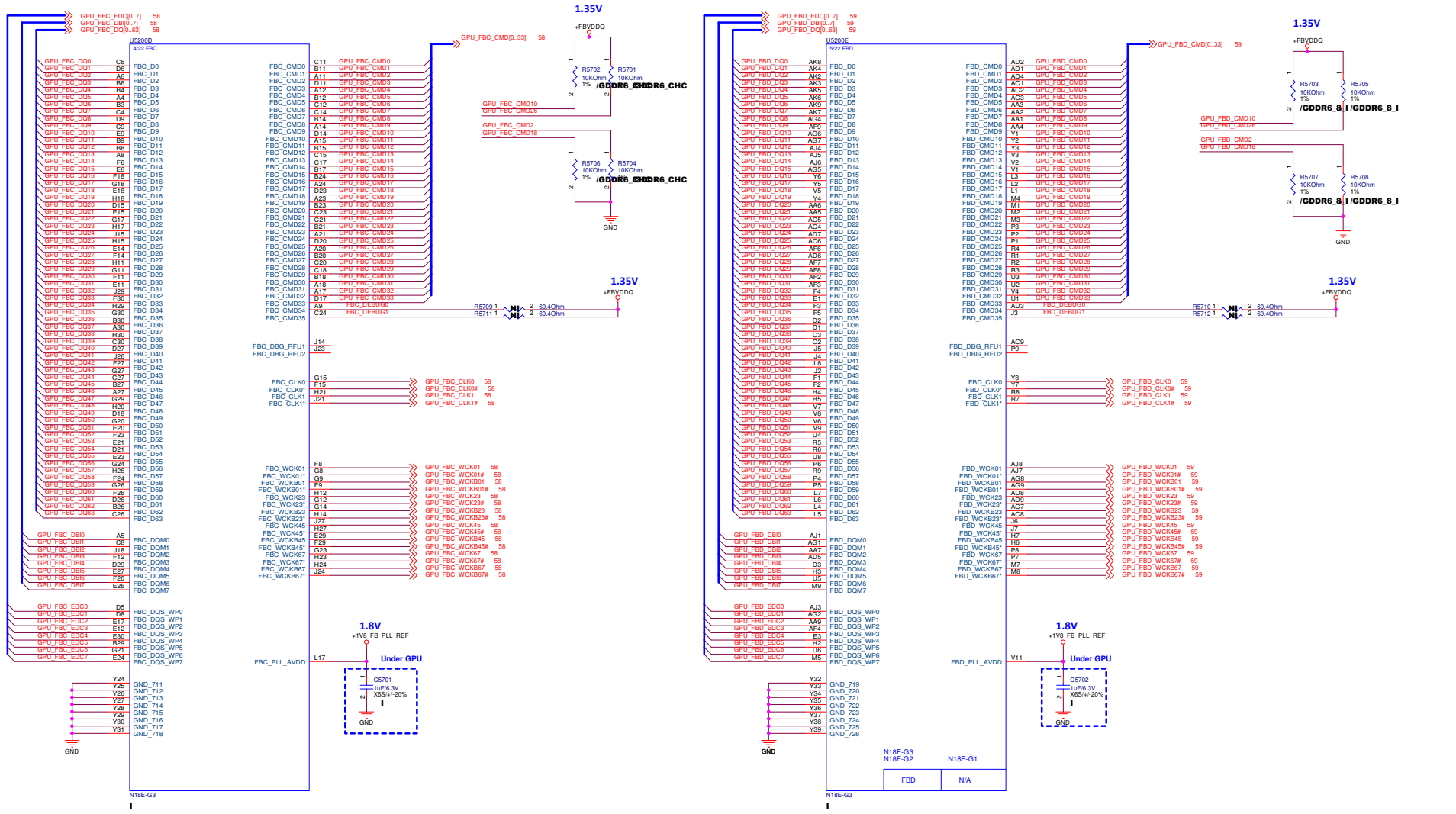
Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 55 of 110

CELL2 TOP X32 MODE





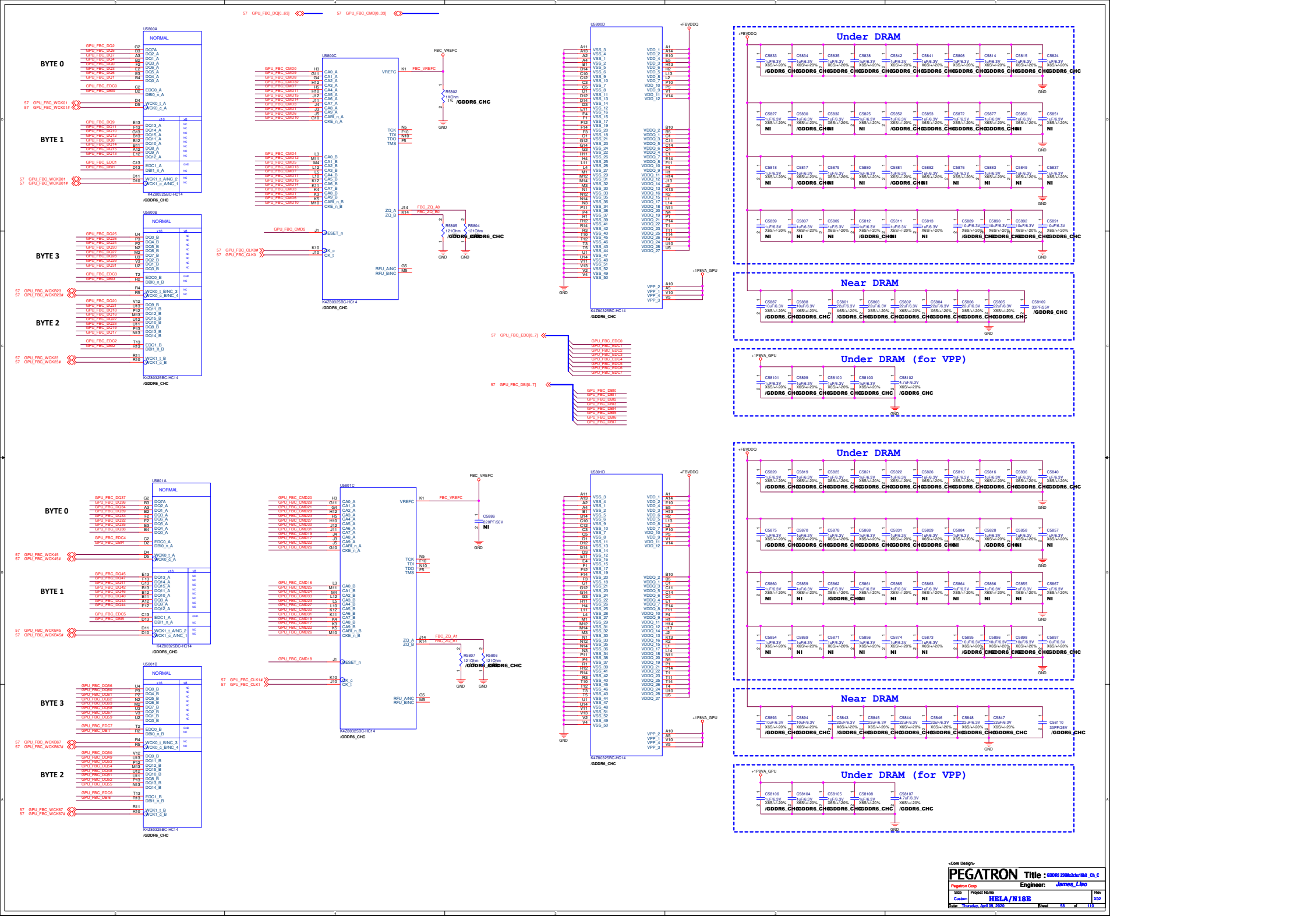
<Core Design>

PEGATRON Title : GPU-BUFFER PARTITION C/D

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A2	HELA/N18E	X02

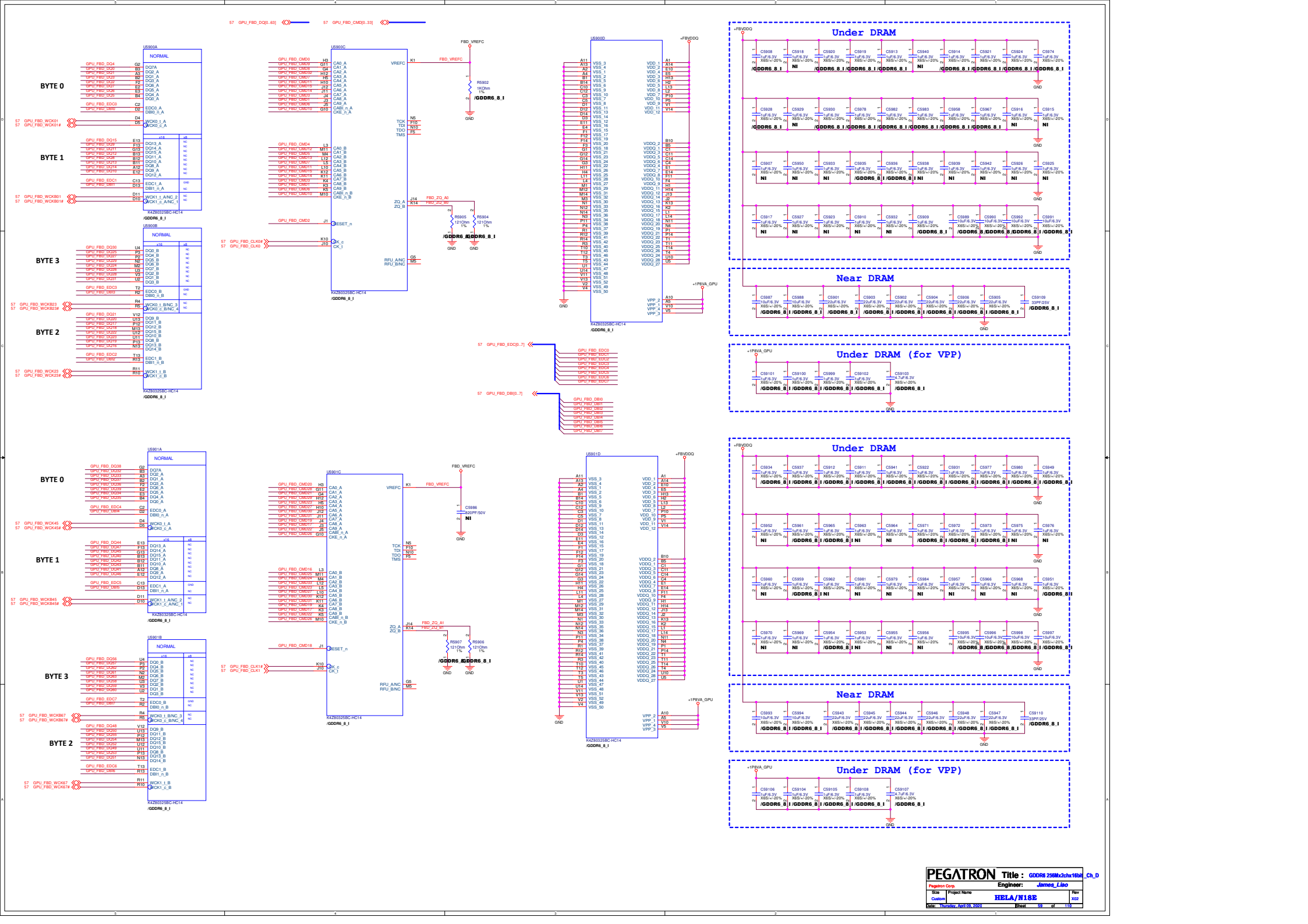
Date: Thursday, April 09, 2020 Sheet 57 of 110



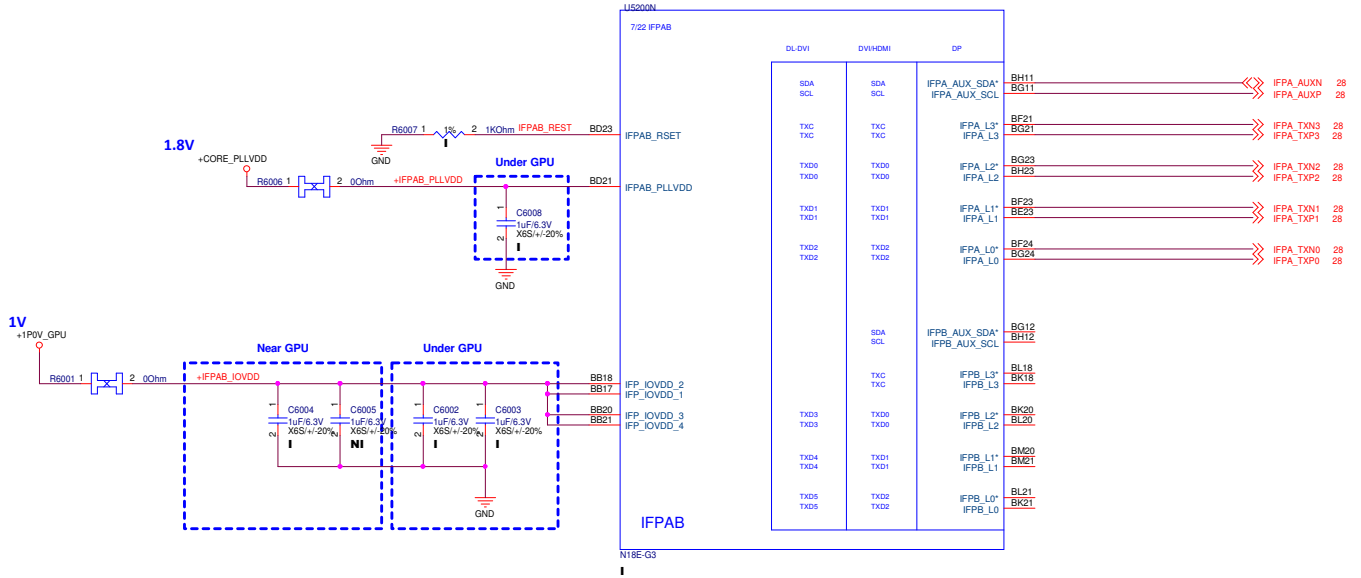
Pegatron Corp.
Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

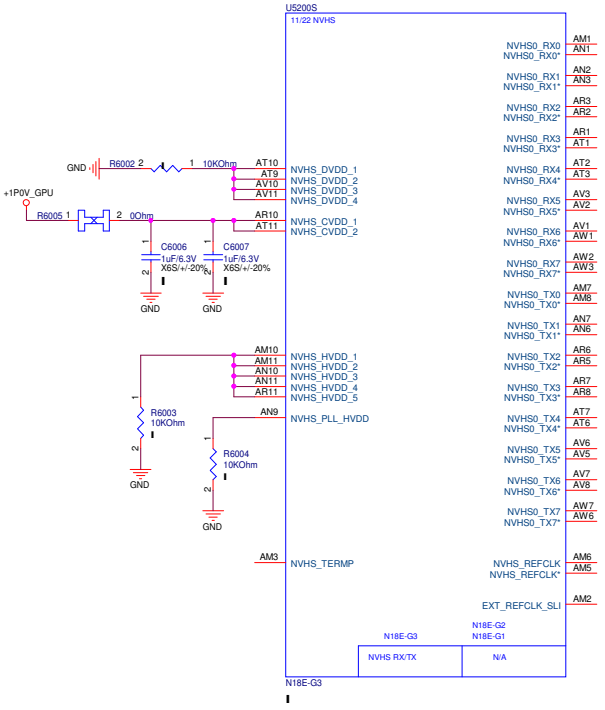
Date: Thursday, April 09, 2020 Sheet 58 of 110



PEGATRON	Title :	GDDR6 256Mx2chx16bit_Ch_D	
Pegatron Corp.	Engineer:	James_Liao	
Size: Custom	Project Name: HELA/N18E		Rev: X02
Date: Thursday, April 09, 2020	Sheet: 59 of 116		



TO TYPEC DP1



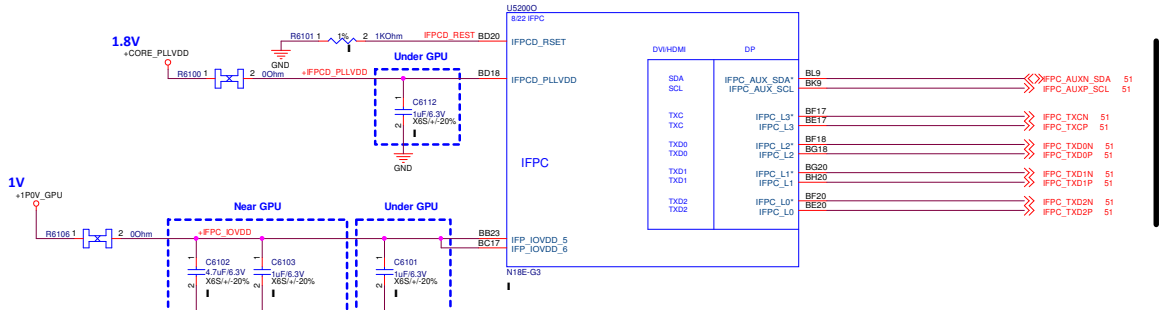
<Core Design>

PEGATRON Title : GPU_MIO

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
C	HELA/N18E	X02

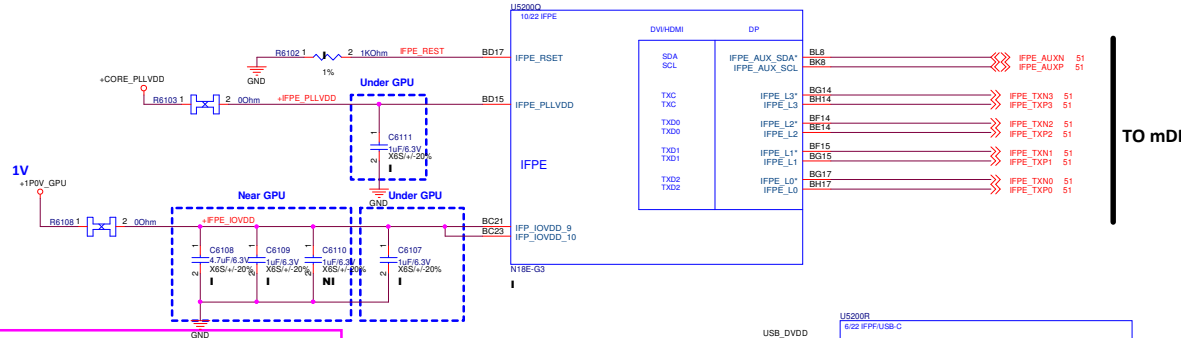
Date: Thursday, April 09, 2020 Sheet 60 of 110



TO HDMI

Table 9.6 HDMI Power Rails

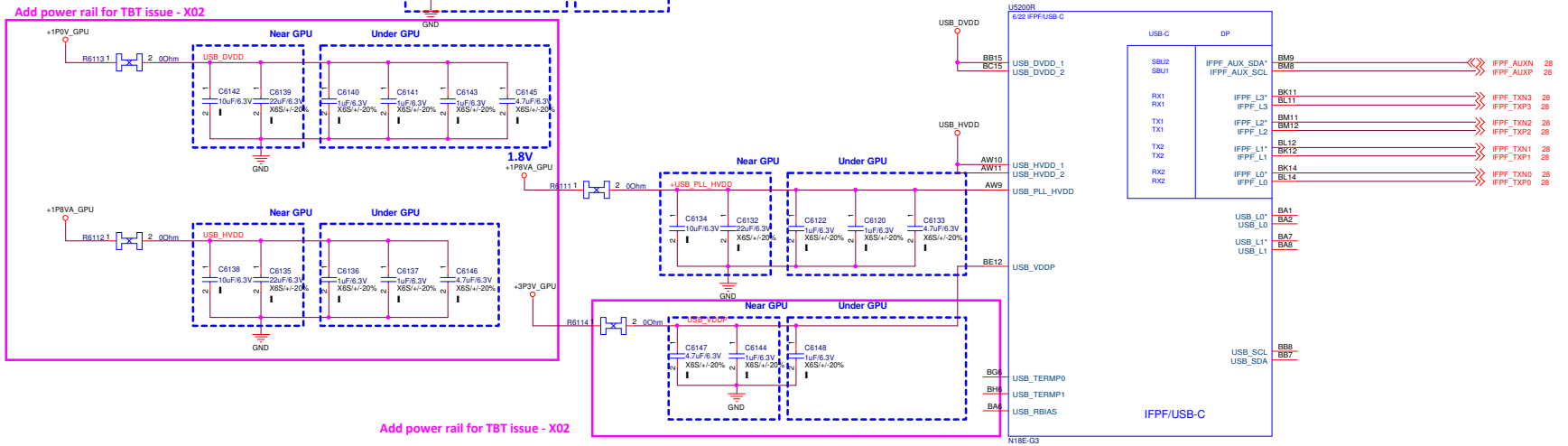
Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 10%	~98 mA
IFPCD_PLLVDD	1.8 V ± 10%	~98 mA
IFPEF_PLLVDD	1.8 V ± 10%	~98 mA



TO mDP

Table 9.11 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA



TO TYPEC DP2

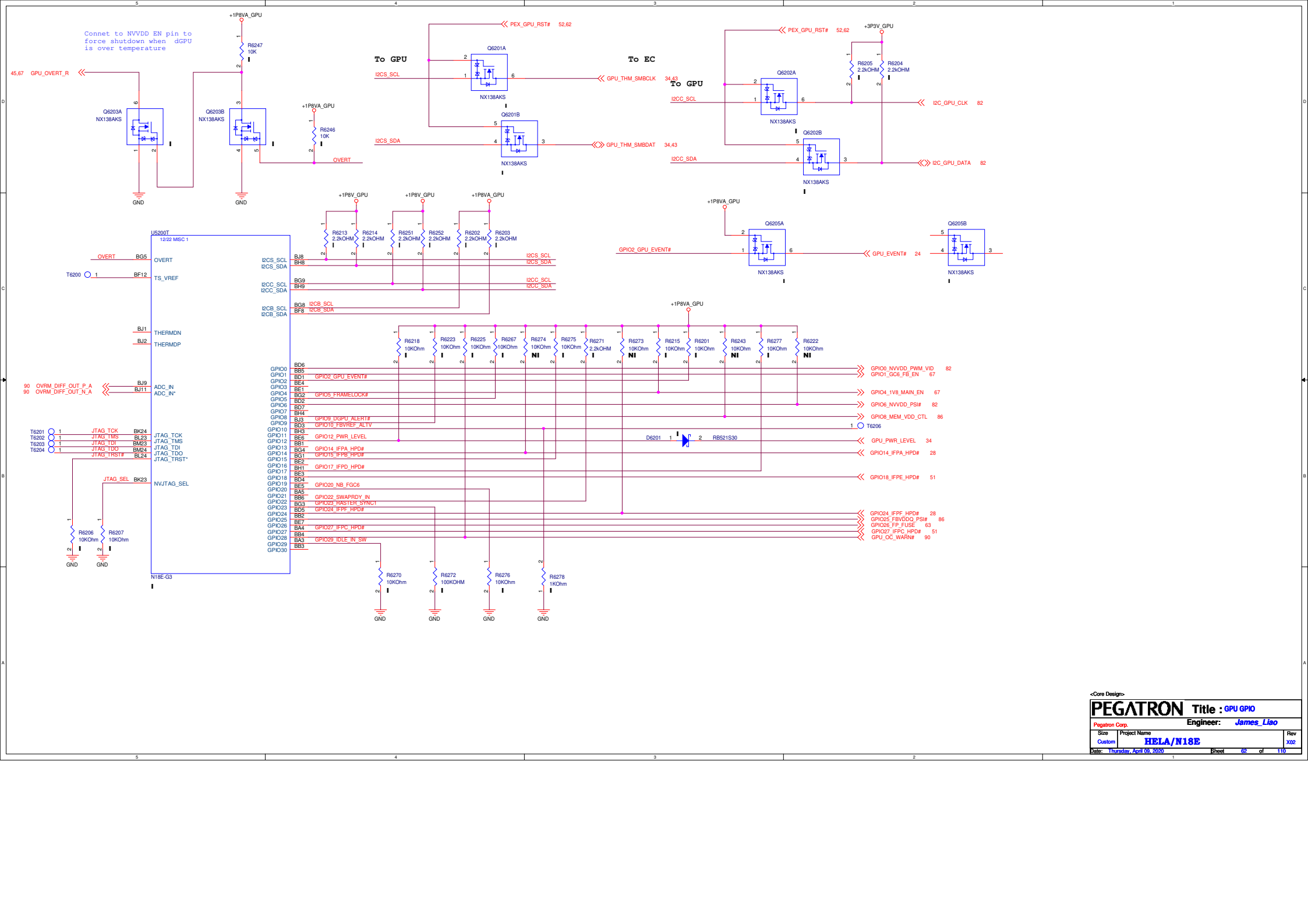
<Core Design>

PEGATRON Title : GPU mini DP/HDMI/MUX

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A2	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 61 of 110



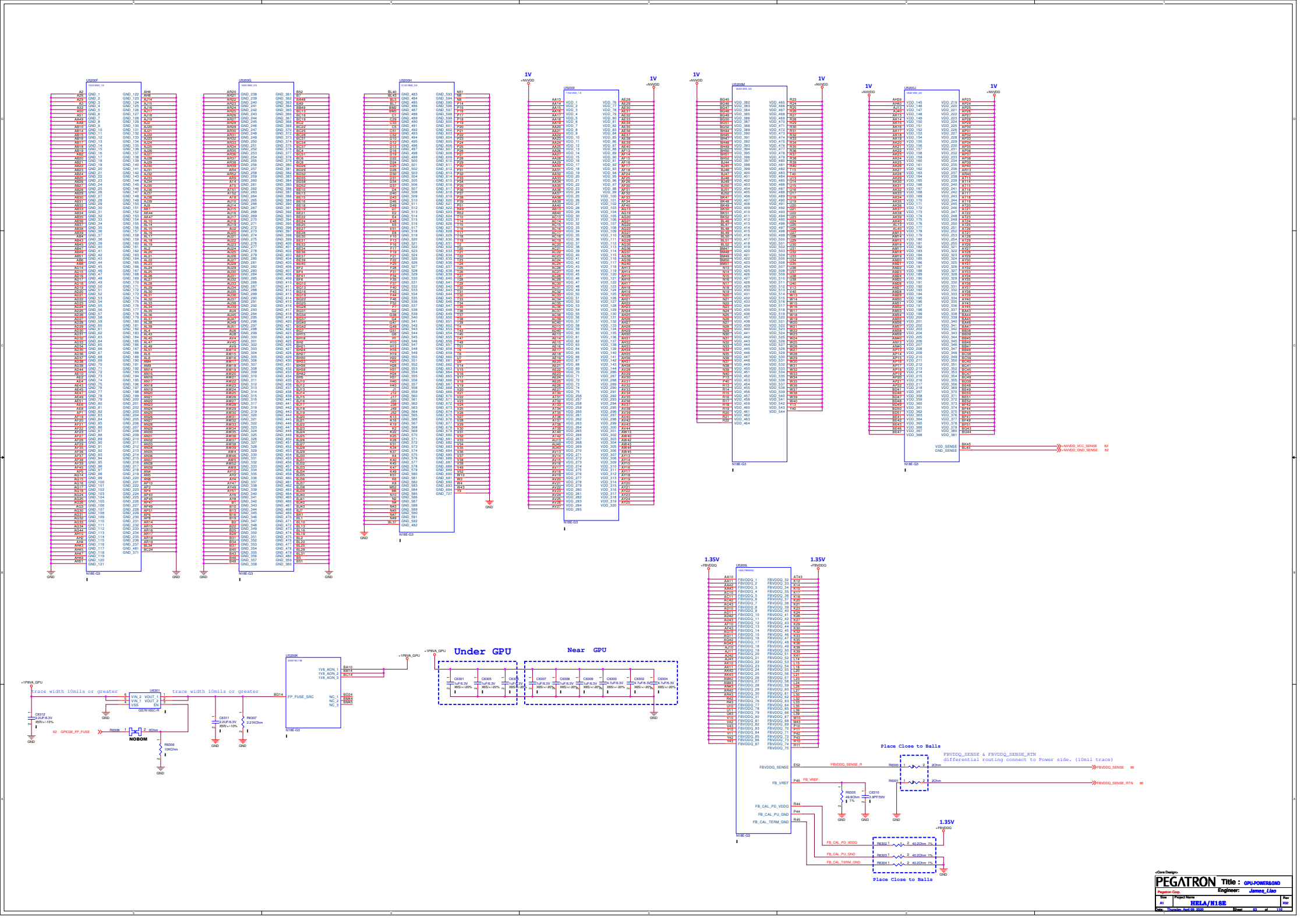
<Core Design>

PEGATRON Title : GPU GPIO

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
Custom	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 62 of 110


Under GPU
Near GPU
Place Close to Balls
Place Close to Balls
FBVDDQ_SENSE & FBVDDQ_SENSE_RTN
differential routing connect to Power side. (10mil trace)
trace width 10mils or greater
trace width 10mils or greater
N18E-G3
GND
1V
1.35V
+NVVDD
+FBVDDQ
+1PWA_GPU
PEGATRON
Title : GPU-POWER&GND
Engineer: James_Liao
Pegatron Corp.
HELA/N18E
Thursday, April 09, 2020

+FBVDDQ

+FBVDDQ

Under GPU

Partition A

C6413 1uF/6.3V X6S/+/-20% NI
C6414 1uF/6.3V X6S/+/-20%
C6415 1uF/6.3V X6S/+/-20%
C6416 1uF/6.3V X6S/+/-20%
C6417 1uF/6.3V X6S/+/-20%
C6418 1uF/6.3V X6S/+/-20% NI
C64237 10uF/6.3V X6S/+/-20%
C64238 10uF/6.3V X6S/+/-20%
GND

C6421 1uF/6.3V X6S/+/-20%
C6422 1uF/6.3V X6S/+/-20%
C6423 1uF/6.3V X6S/+/-20% NI
C6424 1uF/6.3V X6S/+/-20%
C6419 1uF/6.3V X6S/+/-20%
C6420 1uF/6.3V X6S/+/-20%
GND

Partition B

C6433 1uF/6.3V X6S/+/-20%
C6434 1uF/6.3V X6S/+/-20%
C6435 1uF/6.3V X6S/+/-20%
C6436 1uF/6.3V X6S/+/-20%
C6425 1uF/6.3V X6S/+/-20%
C6426 1uF/6.3V X6S/+/-20% NI
C64267 10uF/6.3V X6S/+/-20%
C64268 10uF/6.3V X6S/+/-20%
GND

C6429 1uF/6.3V X6S/+/-20% NI
C6430 1uF/6.3V X6S/+/-20% NI
C6432 1uF/6.3V X6S/+/-20% NI
C6431 1uF/6.3V X6S/+/-20% NI
C6427 1uF/6.3V X6S/+/-20% NI
C6428 1uF/6.3V X6S/+/-20%
GND

Partition C

C6445 1uF/6.3V X6S/+/-20% NI
C6446 1uF/6.3V X6S/+/-20% NI
C6447 1uF/6.3V X6S/+/-20% NI
C6448 1uF/6.3V X6S/+/-20% NI
C6437 1uF/6.3V X6S/+/-20% NI
C6438 1uF/6.3V X6S/+/-20% NI
C64269 10uF/6.3V X6S/+/-20%
C64270 10uF/6.3V X6S/+/-20%
GND

C6441 1uF/6.3V X6S/+/-20% NI
C6442 1uF/6.3V X6S/+/-20%
C6444 1uF/6.3V X6S/+/-20%
C6443 1uF/6.3V X6S/+/-20%
C6439 1uF/6.3V X6S/+/-20% NI
C6440 1uF/6.3V X6S/+/-20% NI
GND

Partition D

C6458 1uF/6.3V X6S/+/-20% NI
C6457 1uF/6.3V X6S/+/-20% NI
C6459 1uF/6.3V X6S/+/-20% NI
C6460 1uF/6.3V X6S/+/-20% NI
C6449 1uF/6.3V X6S/+/-20% NI
C6451 1uF/6.3V X6S/+/-20% NI
C64271 10uF/6.3V X6S/+/-20%
C64272 10uF/6.3V X6S/+/-20%
GND

C6453 1uF/6.3V X6S/+/-20% NI
C6455 1uF/6.3V X6S/+/-20% NI
C6456 1uF/6.3V X6S/+/-20% NI
C6454 1uF/6.3V X6S/+/-20% NI
C6450 1uF/6.3V X6S/+/-20% NI
C6452 1uF/6.3V X6S/+/-20% NI
GND

Near GPU

C64243 10uF/6.3V X6S/+/-20%
C64244 10uF/6.3V X6S/+/-20%
C64245 10uF/6.3V X6S/+/-20%
C64246 10uF/6.3V X6S/+/-20%
GND

C64247 22uF/6.3V X6S/+/-20%
C64248 22uF/6.3V X6S/+/-20%
C64249 22uF/6.3V X6S/+/-20%
C64250 22uF/6.3V X6S/+/-20%
C64251 22uF/6.3V X6S/+/-20%
C64252 22uF/6.3V X6S/+/-20%
C64253 22uF/6.3V X6S/+/-20%
C64254 22uF/6.3V X6S/+/-20%
C64255 22uF/6.3V X6S/+/-20%
GND

+NVVDD

+NVVDD

Near GPU

CE6403 330UF/2V tx_c7343d_t02_h59
CE6404 330UF/2V tx_c7343d_t02_h59
CE6405 330UF/2V tx_c7343d_t02_h59
GND

Under GPU

C6401 47UF/4V X6S/+/-20% tx_c0805_t02_h57
C6402 47UF/4V X6S/+/-20% tx_c0805_t02_h57
C6461 47UF/4V X6S/+/-20% tx_c0805_t02_h57
C64239 22uF/6.3V X6S/+/-20%
C64240 22uF/6.3V X6S/+/-20%
C64241 22uF/6.3V X6S/+/-20%
C64242 22UF/4V X6S/+/-20% tx_c0805_t02_h55
GND

+FBVDDQ — C64285 1 2 0.1UF/25V X5R/+/-10% NI — +NVVDD
+FBVDDQ — C64286 1 2 0.1UF/25V X5R/+/-10% NI — +NVVDD

+FBVDDQ_VIN — C64287 0.1UF/25V X5R/+/-10% — GND

Under GPU

C64256 10uF/6.3V X6S/+/-20%
C64257 10uF/6.3V X6S/+/-20%
C64258 10uF/6.3V X6S/+/-20%
C64259 10uF/6.3V X6S/+/-20%
C64260 10uF/6.3V X6S/+/-20%
C64261 10uF/6.3V X6S/+/-20%
C64262 10uF/6.3V X6S/+/-20%
C64263 10uF/6.3V X6S/+/-20%
C64264 10uF/6.3V X6S/+/-20%
C64265 10uF/6.3V X6S/+/-20%
C64266 10uF/6.3V X6S/+/-20%
C64280 10uF/6.3V X6S/+/-20%
C64281 10uF/6.3V X6S/+/-20%
C64282 10uF/6.3V X6S/+/-20%
C64283 10uF/6.3V X6S/+/-20%
C64273 10uF/6.3V X6S/+/-20%
C64274 10uF/6.3V X6S/+/-20%
C64275 10uF/6.3V X6S/+/-20%
C64276 10uF/6.3V X6S/+/-20%
C64277 10uF/6.3V X6S/+/-20%
C64278 10uF/6.3V X6S/+/-20%
C64279 10uF/6.3V X6S/+/-20%
C64284 10uF/6.3V X6S/+/-20%
GND

C6475 1uF/6.3V X6S/+/-20%
C6474 1uF/6.3V X6S/+/-20%
C6491 1uF/6.3V X6S/+/-20%
C6488 1uF/6.3V X6S/+/-20%
C6494 1uF/6.3V X6S/+/-20%
C6493 1uF/6.3V X6S/+/-20%
C6465 1uF/6.3V X6S/+/-20%
C64101 1uF/6.3V X6S/+/-20%
C64102 1uF/6.3V X6S/+/-20%
C6497 1uF/6.3V X6S/+/-20%
C64205 1uF/6.3V X6S/+/-20%
C64206 1uF/6.3V X6S/+/-20%
C64197 1uF/6.3V X6S/+/-20%
C64179 1uF/6.3V X6S/+/-20%
C64219 1uF/6.3V X6S/+/-20%
C64216 1uF/6.3V X6S/+/-20%
C64221 1uF/6.3V X6S/+/-20%
C64155 1uF/6.3V X6S/+/-20%
C64220 1uF/6.3V X6S/+/-20%
C64228 1uF/6.3V X6S/+/-20%
GND

C64131 1uF/6.3V X6S/+/-20%
C64128 1uF/6.3V X6S/+/-20%
C64113 1uF/6.3V X6S/+/-20%
C6476 1uF/6.3V X6S/+/-20%
C6485 1uF/6.3V X6S/+/-20%
C6498 1uF/6.3V X6S/+/-20%
C6482 1uF/6.3V X6S/+/-20%
C6477 1uF/6.3V X6S/+/-20%
C64193 1uF/6.3V X6S/+/-20%
C64207 1uF/6.3V X6S/+/-20%
C64195 1uF/6.3V X6S/+/-20%
C64194 1uF/6.3V X6S/+/-20%
C64227 1uF/6.3V X6S/+/-20%
C6495 1uF/6.3V X6S/+/-20%
C64236 1uF/6.3V X6S/+/-20%
C64202 1uF/6.3V X6S/+/-20%
C64217 1uF/6.3V X6S/+/-20%
C64203 1uF/6.3V X6S/+/-20%
C64204 1uF/6.3V X6S/+/-20%
C64192 1uF/6.3V X6S/+/-20%
GND

C6489 1uF/6.3V X6S/+/-20%
C6467 1uF/6.3V X6S/+/-20%
C64211 1uF/6.3V X6S/+/-20%
C64198 1uF/6.3V X6S/+/-20%
C64156 1uF/6.3V X6S/+/-20%
C64225 1uF/6.3V X6S/+/-20%
C64212 1uF/6.3V X6S/+/-20%
C64232 1uF/6.3V X6S/+/-20%
C64229 1uF/6.3V X6S/+/-20%
C6405 1uF/6.3V X6S/+/-20%
C6406 1uF/6.3V X6S/+/-20%
C6407 1uF/6.3V X6S/+/-20%
C6472 1uF/6.3V X6S/+/-20%
C6480 1uF/6.3V X6S/+/-20%
C6473 1uF/6.3V X6S/+/-20%
C6464 1uF/6.3V X6S/+/-20%
C6478 1uF/6.3V X6S/+/-20%
C64107 1uF/6.3V X6S/+/-20%
C64109 1uF/6.3V X6S/+/-20%
C64117 1uF/6.3V X6S/+/-20%
GND

C6470 1uF/6.3V X6S/+/-20%
C6463 1uF/6.3V X6S/+/-20%
C6481 1uF/6.3V X6S/+/-20%
C64124 1uF/6.3V X6S/+/-20%
C64123 1uF/6.3V X6S/+/-20%
C64119 1uF/6.3V X6S/+/-20%
C64118 1uF/6.3V X6S/+/-20%
C64116 1uF/6.3V X6S/+/-20%
C64121 1uF/6.3V X6S/+/-20%
C64147 1uF/6.3V X6S/+/-20%
C64135 1uF/6.3V X6S/+/-20%
C64134 1uF/6.3V X6S/+/-20%
C64151 1uF/6.3V X6S/+/-20%
C64150 1uF/6.3V X6S/+/-20%
C64148 1uF/6.3V X6S/+/-20%
C64169 1uF/6.3V X6S/+/-20%
C64170 1uF/6.3V X6S/+/-20%
C64167 1uF/6.3V X6S/+/-20%
C64143 1uF/6.3V X6S/+/-20%
C64165 1uF/6.3V X6S/+/-20%
GND

C64158 1uF/6.3V X6S/+/-20%
C64141 1uF/6.3V X6S/+/-20%
C64161 1uF/6.3V X6S/+/-20%
C64182 1uF/6.3V X6S/+/-20%
C64183 1uF/6.3V X6S/+/-20%
C64185 1uF/6.3V X6S/+/-20%
C64172 1uF/6.3V X6S/+/-20%
C64174 1uF/6.3V X6S/+/-20%
C64175 1uF/6.3V X6S/+/-20%
C64214 1uF/6.3V X6S/+/-20%
C64230 1uF/6.3V X6S/+/-20%
C64188 1uF/6.3V X6S/+/-20%
C64137 1uF/6.3V X6S/+/-20%
C64209 1uF/6.3V X6S/+/-20% NI
C64122 1uF/6.3V X6S/+/-20% NI
C6499 1uF/6.3V X6S/+/-20% NI
C64108 1uF/6.3V X6S/+/-20% NI
C6490 1uF/6.3V X6S/+/-20% NI
C6469 1uF/6.3V X6S/+/-20% NI
C6403 1uF/6.3V X6S/+/-20% NI
GND

C64149 1uF/6.3V X6S/+/-20% NI
C64210 1uF/6.3V X6S/+/-20% NI
C64200 1uF/6.3V X6S/+/-20% NI
C64208 1uF/6.3V X6S/+/-20% NI
C64132 1uF/6.3V X6S/+/-20% NI
C64130 1uF/6.3V X6S/+/-20% NI
C64120 1uF/6.3V X6S/+/-20% NI
C64140 1uF/6.3V X6S/+/-20% NI
C6409 1uF/6.3V X6S/+/-20% NI
C64133 1uF/6.3V X6S/+/-20% NI
C64145 1uF/6.3V X6S/+/-20% NI
C6404 1uF/6.3V X6S/+/-20% NI
C64139 1uF/6.3V X6S/+/-20% NI
C64138 1uF/6.3V X6S/+/-20% NI
C64136 1uF/6.3V X6S/+/-20% NI
C64144 1uF/6.3V X6S/+/-20% NI
C64146 1uF/6.3V X6S/+/-20% NI
C64201 1uF/6.3V X6S/+/-20% NI
C64142 1uF/6.3V X6S/+/-20% NI
C6487 1uF/6.3V X6S/+/-20% NI
GND

Under GPU

C64235 1uF/6.3V X6S/+/-20% NI
C6410 1uF/6.3V X6S/+/-20% NI
C64234 1uF/6.3V X6S/+/-20% NI
C64233 1uF/6.3V X6S/+/-20% NI
C6411 1uF/6.3V X6S/+/-20% NI
GND

<Core Design>

PEGATRON Title : GPU-Decoupling

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
A2	HELA/N18E	X02

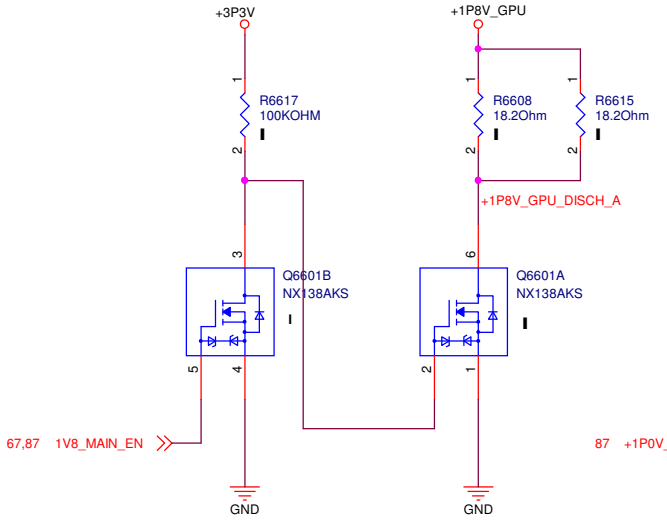
Date: Thursday, April 09, 2020 Sheet 64 of 110

h

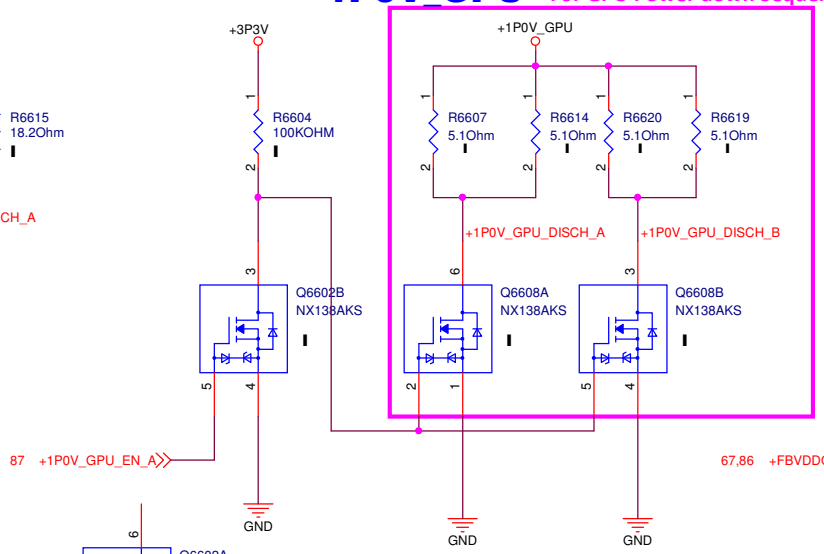
PEGATRON	Title : <Title>	
Pegatron Corp.	Engineer: James_Liao	
Size: C	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 65 of 110	

GPU POWER DISCHARGE

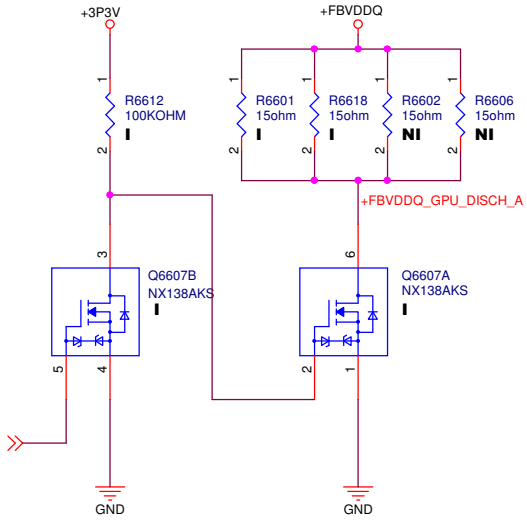
+1P8V_GPU

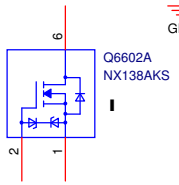


+1P0V_GPU For GPU Power down Sequence- X02

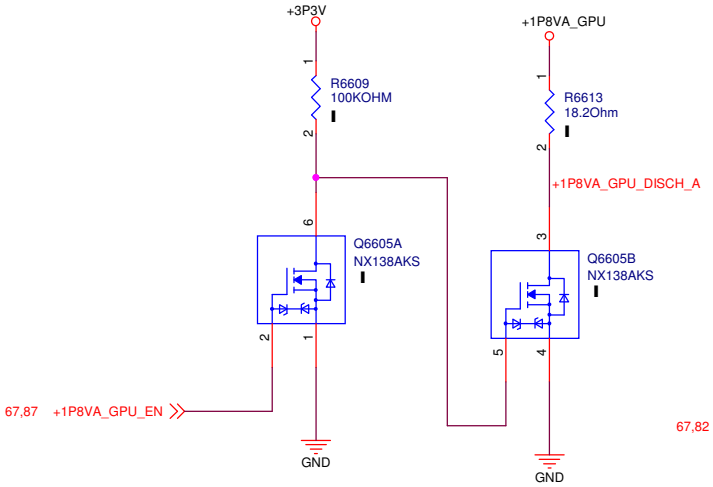


+FBVDDQ

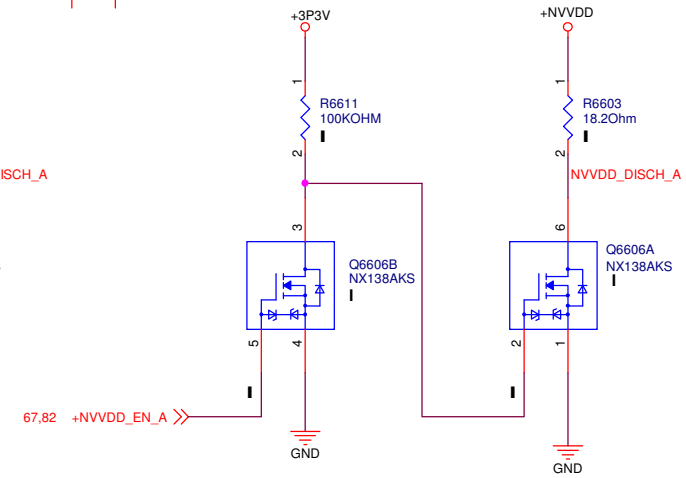




+1P8VA_GPU



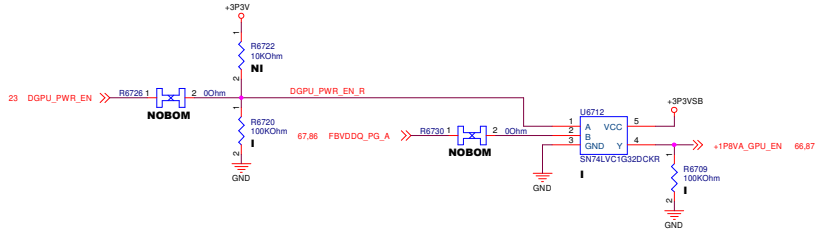
+NVVDD



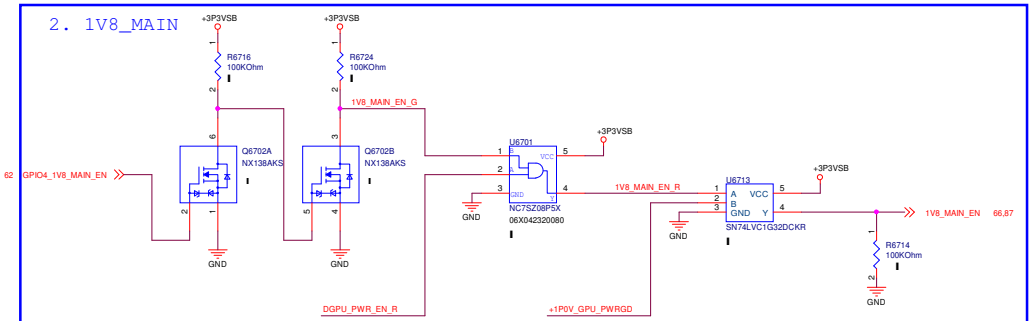
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : GPU POWER DISCHARG	
Pegatron Corp.	Engineer: James_Liao	
Size: B	Project Name: HELA/N18E	Rev: X02
Date: Thursday, April 09, 2020	Sheet 66 of 110	

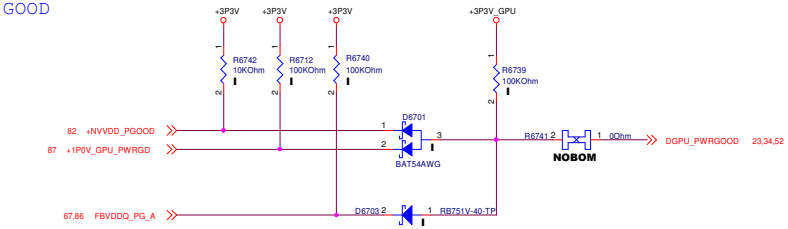
1.1V8_AON



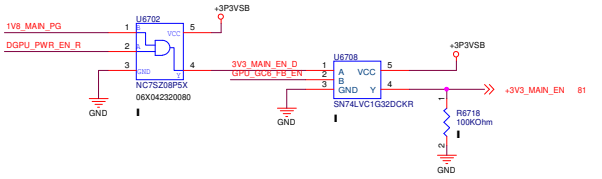
2. 1V8_MAIN



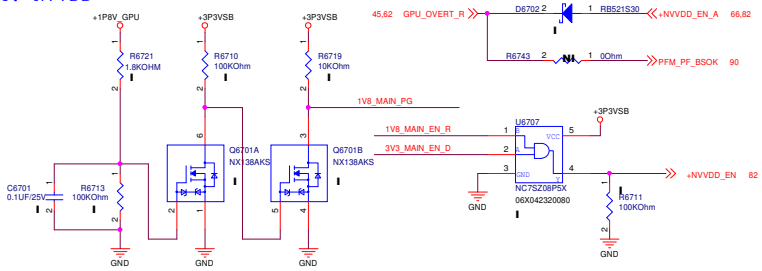
POWER GOOD



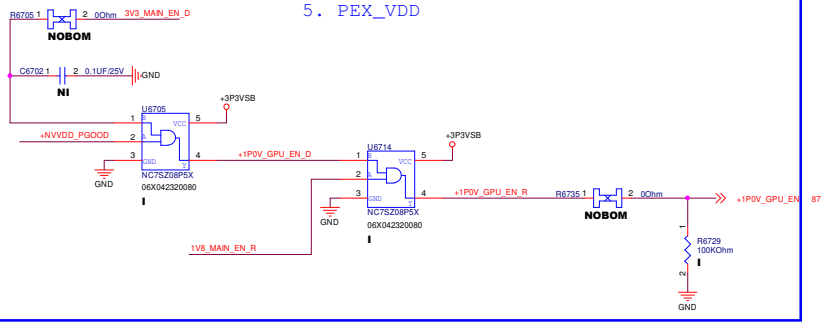
3. 3V3_MAIN



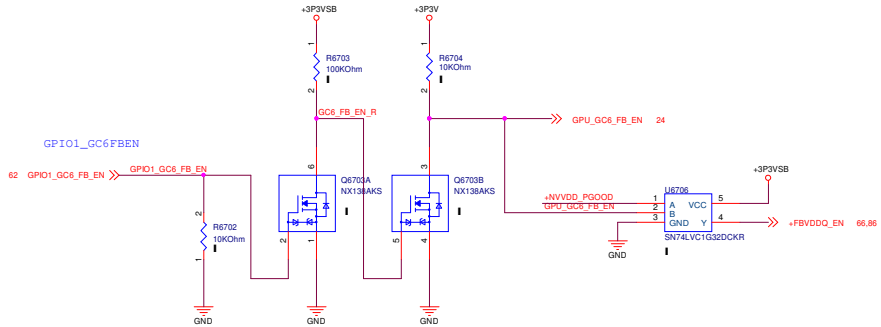
4. NVVDD



5. PEX_VDD



6. FBVDDQ



<Core Design>

PEGATRON Title : GPU_POWER Sequence

Pegatron Corp. Engineer: James_Liao

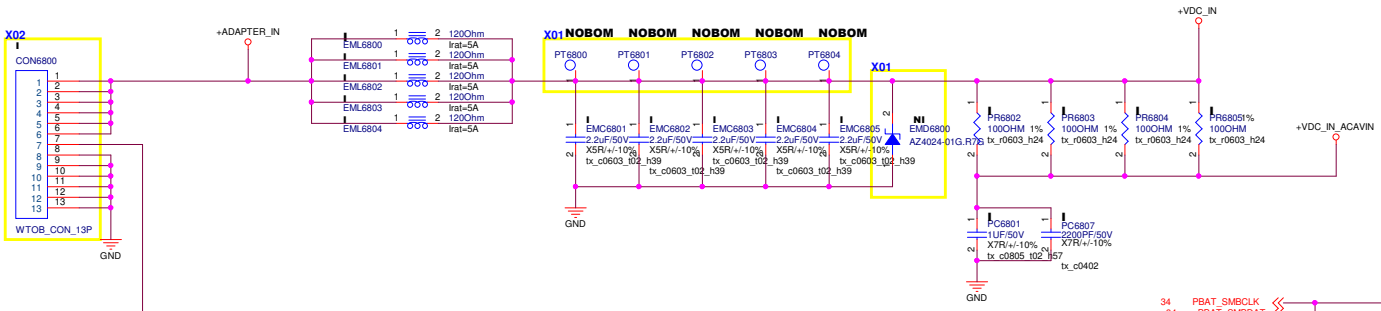
Size	Project Name	Rev
A2	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 67 of 110

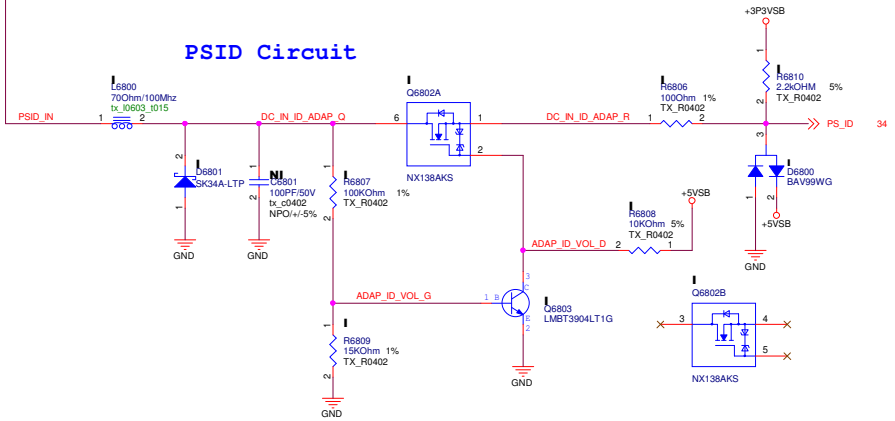
DC-IN connector

lin = 240W / 19.5V = 12.308A

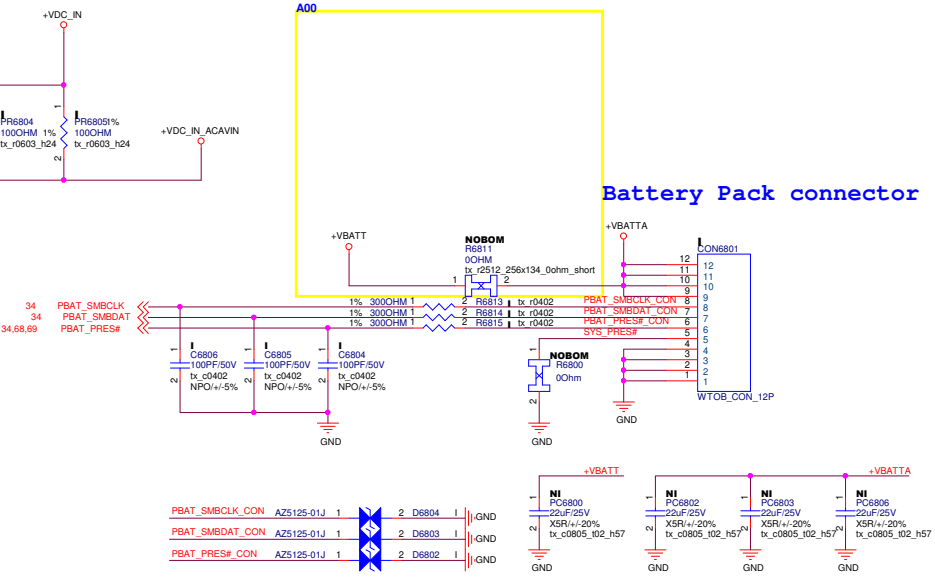
12.308 / (5*0.5) = 4.93 pcs => 5 pcs



PSID Circuit



Battery Pack connector



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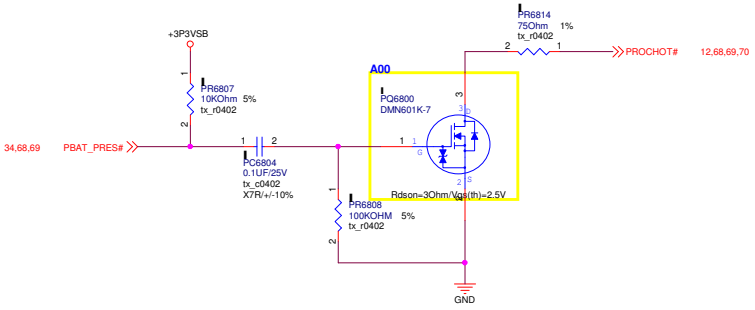
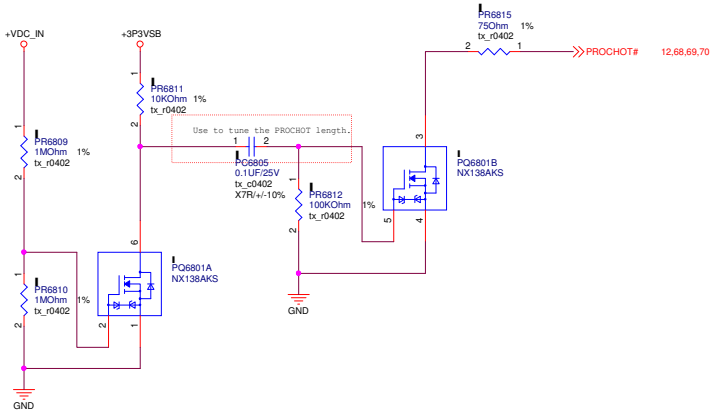
Adapter Protection Circuit



Battery Protection Circuit



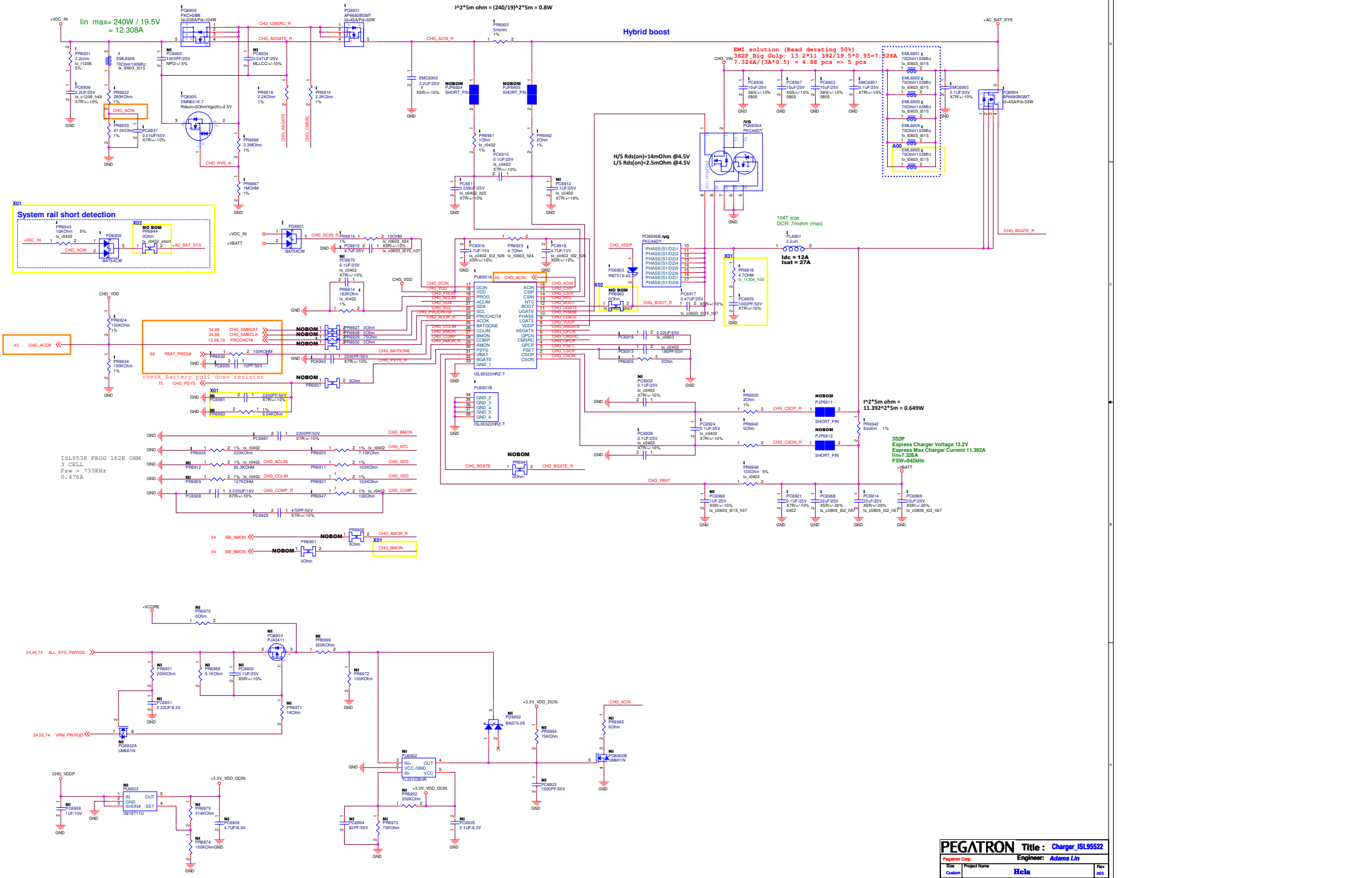
<Core Design>

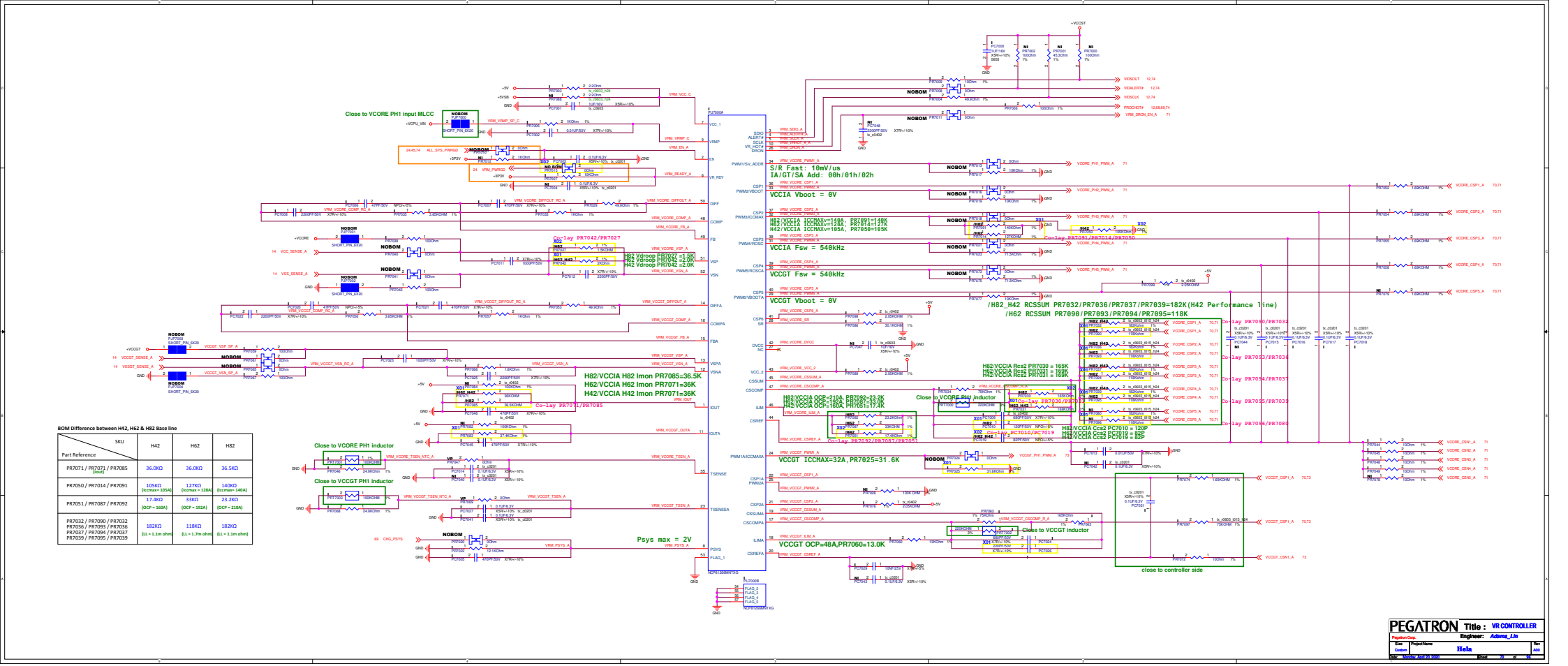
PEGATRON Title : DC_IN

Pegatron Corp. Engineer: Adams Lin

Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 68 of 94


Iin max= 240W / 19.5V
= 12.308A
I^2*5m ohm = (240/19)^2*5m = 0.8W
Hybrid boost
EMI solution (Bead derating 50%)
3822P_Big Gulp: 13.2*11.392/19.5*0.95=7.326A/(3A*0.5) = 4.88 pcs => 5 pcs
7.326A
H/S Rds(on)=14mOhm @4.5V
L/S Rds(on)=2.5mOhm @4.5V
104T size
DCR: 7mohm (max)
Idc = 12A
Isat = 27A
I^2*5m ohm =
11.392^2*5m = 0.649W
3S2P
Express Charger Voltage 13.2V
Express Max Charger Current 11.392A
Iin=7.326A
FSW=942kHz
System rail short detection
check Battery pull down resister
ISL9538 PROG 162K OHM
3 CELL
Fsw = 733KHz
0.476A
PEGATRON
Title : Charger_ISL95522
Engineer: Adams Lin
Pegatron Corp.
Project Name
Hela
Rev
A00
Date: Monday, April 20, 2020
Sheet 68 of 96


Close to VCORE PH1 input MLCC
S/R Fast: 10mV/us
1A/GT/SA Add: 00h/01h/02h
VCCIA Vboot = 0V
H82/VCCIA ICCMAXv=140A, PR7091=140K
H82/VCCIA ICCMAXv=128A: PR7014=127K
H42/VCCIA ICCMAXv=105A: PR7050=105K
VCCIA Fsw = 540kHz
VCCGT Fsw = 540kHz
VCCGT Vboot = 0V
/H82_H42 RCSSUM PR7032/PR7036/PR7037/PR7039=182K(H42 Performance line)
/H62 RCSSUM PR7090/PR7093/PR7094/PR7095=118K
Co-lay PR7042/PR7027
H82 Vdroop PR7027 =1.5K
H62 Vdroop PR7042 =2.0K
H42 Vdroop PR7042 =2.0K
Co-lay PR7071/PR7085
H82/VCCIA H82 Imon PR7085=36.5K
H62/VCCIA H62 Imon PR7071=36K
H42/VCCIA H42 Imon PR7071=36K
Close to VCORE PH1 inductor
Close to VCCGT PH1 inductor
H82/VCCIA OCP=210A, PR7092=23.2K
H62/VCCIA OCP=160A, PR7087=17.4K
H42/VCCIA OCP=160A, PR7051=17.4K
Co-lay PR7092/PR7087/PR7051
H82/VCCIA Rcs2 PR7030 = 165K
H62/VCCIA Rcs2 PR7031 = 169K
H42/VCCIA Rcs2 PR7031 = 169K
Co-lay PR7030/PR7032
Co-lay PR7033/PR7036
Co-lay PR7034/PR7037
Co-lay PR7035/PR7039
Co-lay PR7056/PR7080
H82/VCCIA Cs2 PC7010 = 120P
H62/VCCIA Cs2 PC7019 = 82P
H42/VCCIA Cs2 PC7015 = 82P
Co-lay PR7030/PR7032/PR7033/PR7034/PR7035/PR7036
Co-lay PR7031/PR7014/PR7050
Co-lay PC7010/PC7019
VCCGT ICCMAX=32A,PR7625=31.6K
VCCGT OCP=48A,PR7060=13.0K
Psys max = 2V
Close to VCCGT PH1 inductor
close to controller side
BOM Difference between H42, H62 & H82 Base line
SKU / Part Reference
H42
H62
H82
PR7071 / PR7071 / PR7085 (final)
36.0KΩ
36.0KΩ
36.5KΩ
PR7050 / PR7014 / PR7091
105KΩ (Iccmax= 105A)
127KΩ (Iccmax = 128A)
140KΩ (Iccmax= 140A)
PR7051 / PR7087 / PR7092
17.4KΩ (OCP = 160A)
33KΩ (OCP = 192A)
23.2KΩ (OCP = 210A)
PR7032 / PR7090 / PR7032
PR7036 / PR7093 / PR7036
PR7037 / PR7094 / PR7037
PR7039 / PR7095 / PR7039
182KΩ (LL = 1.1m ohm)
118KΩ (LL = 1.7m ohm)
182KΩ (LL = 1.1m ohm)
PEGATRON
Title : VR CONTROLLER
Engineer: Adams_Lin
Pegatron Corp.
Size: Custom
Project Name: Hela
Rev: A00
Date: Monday, April 29, 2019
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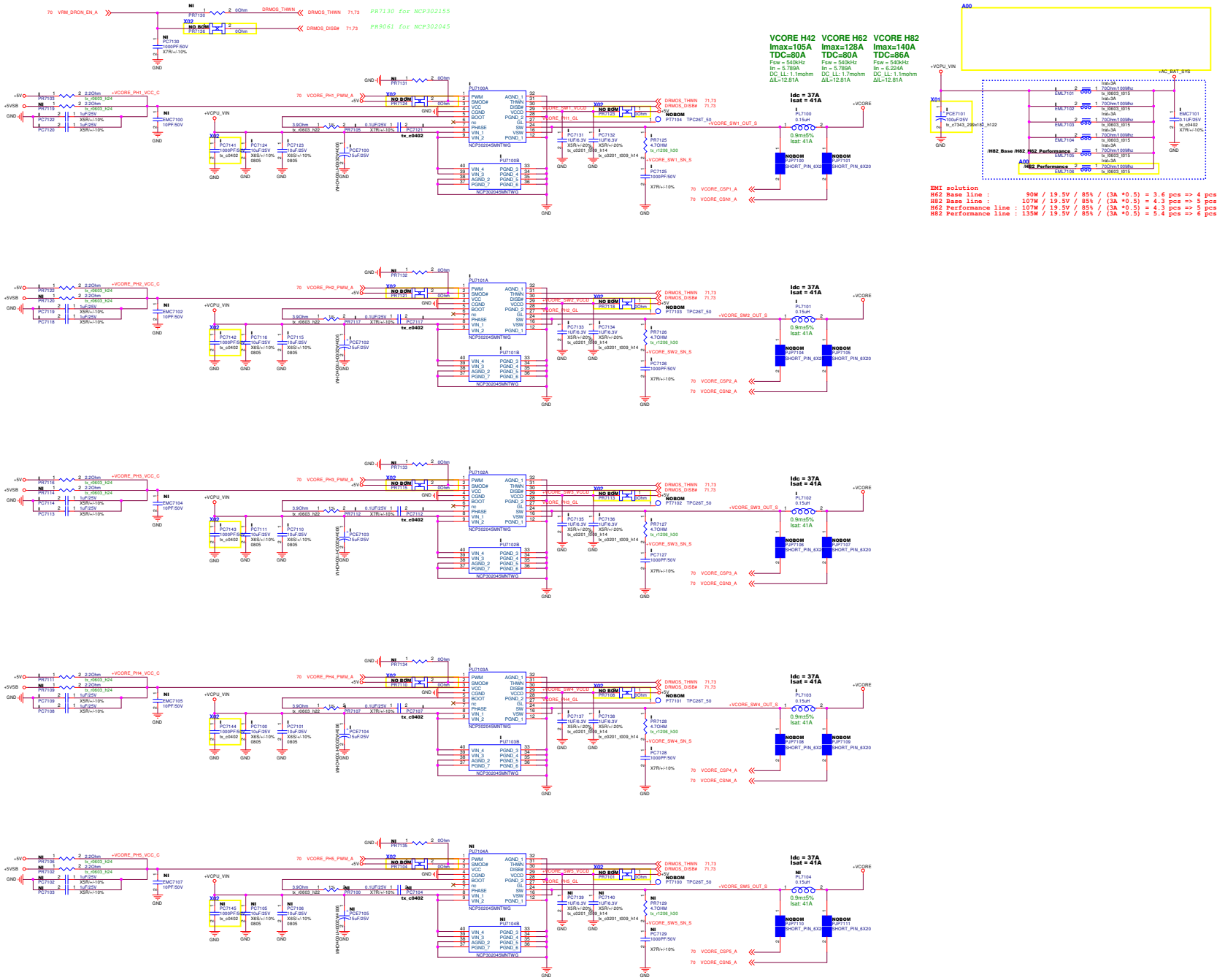


PEGATRON Title : Vcore Driver-1

Pegatron Corp. Engineer: Adams_Lin

Size: Custom | Project Name: Hela | Rev: A00

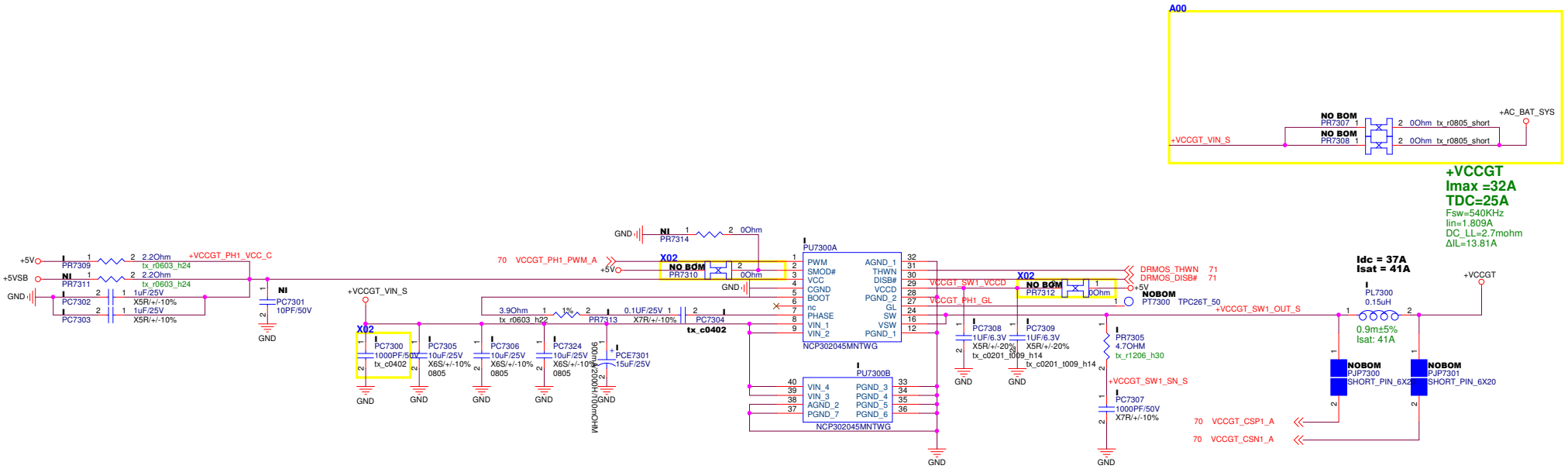
Date: Monday, April 20, 2020 Sheet 71 of 94

PEGATRON Title : Vcore Driver-2

Pegatron Corp. Engineer: Adams_Lin

Size: Custom | Project Name: Hela | Rev: A00

Date: Monday, April 28, 2008 Sheet 28 of 36

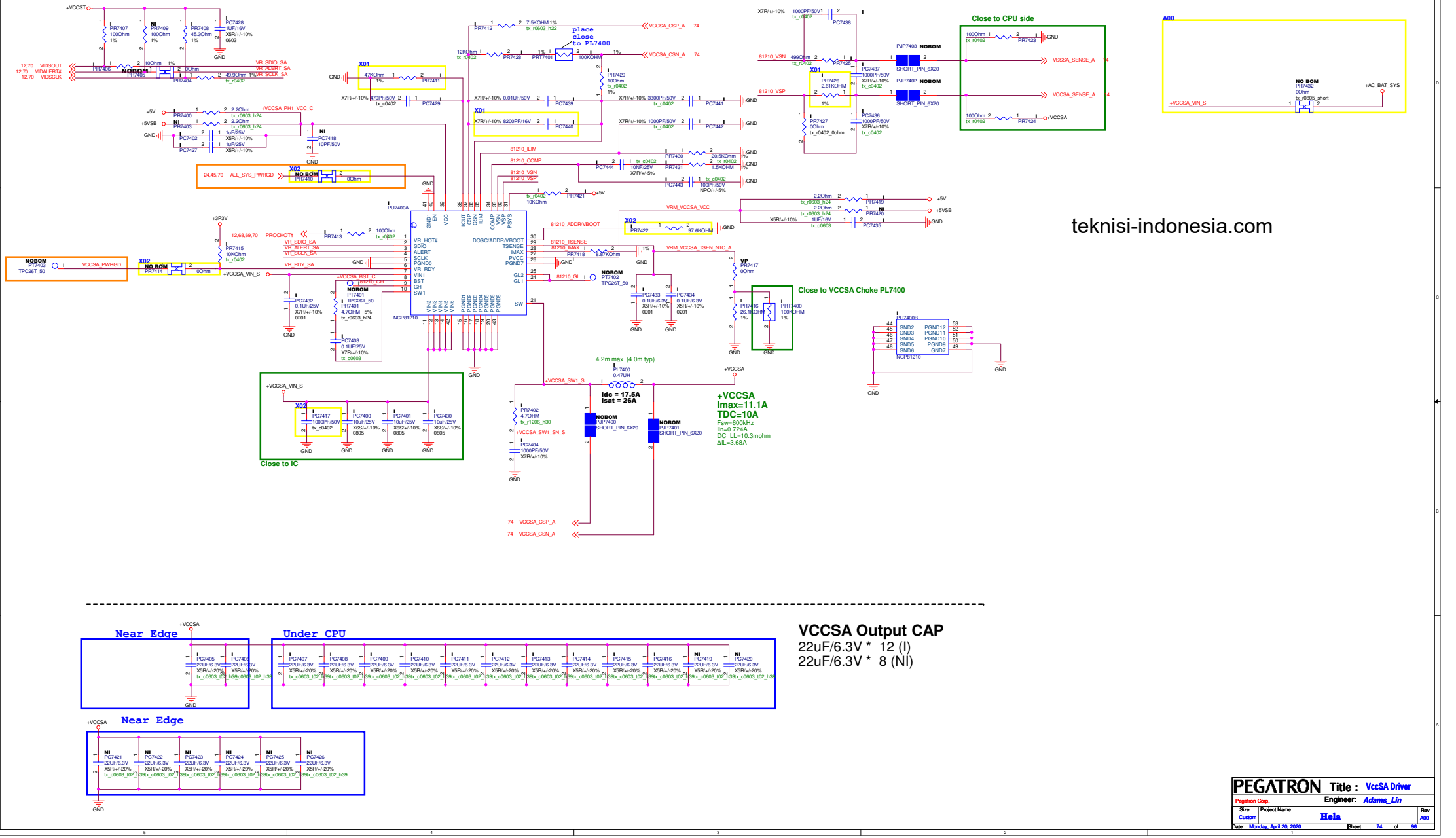


PEGATRON Title : VccGT Driver

Pegatron Corp. Engineer: Adams_Lin

Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 73 of 96

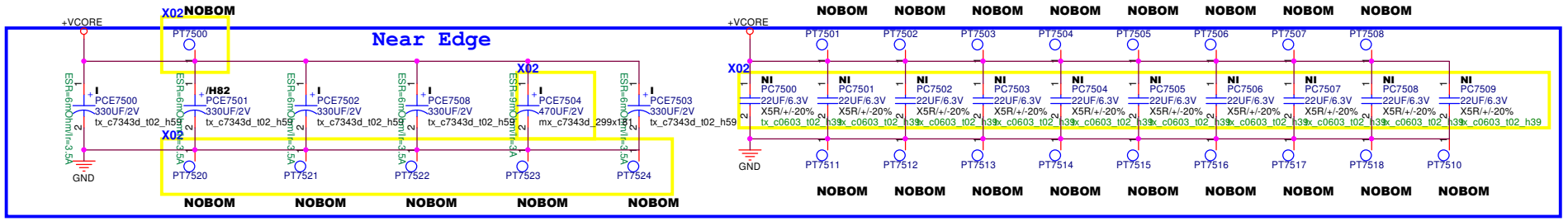


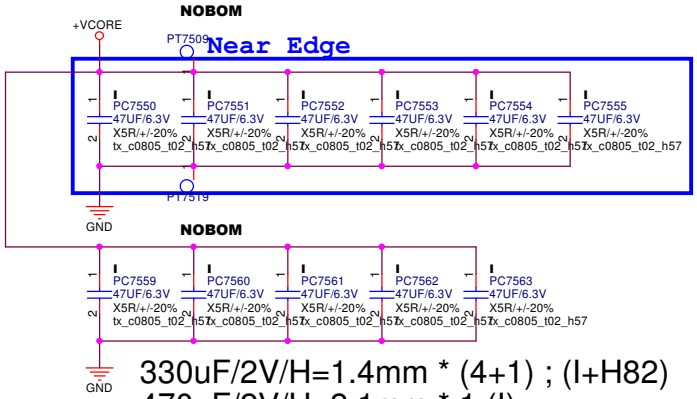
VCCSA Output CAP

22uF/6.3V * 12 (I)
22uF/6.3V * 8 (NI)

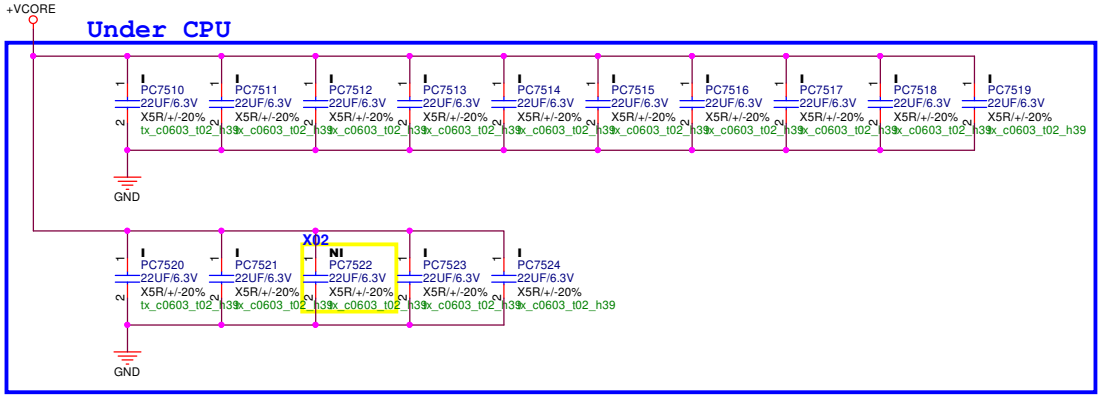
PEGATRON	Title : VccSA Driver		
Pegatron Corp.	Engineer: Adams_Lin		
Size: Custom	Project Name: Hela		Rev: A00
Date: Monday, April 20, 2020	Sheet 74 of 96		

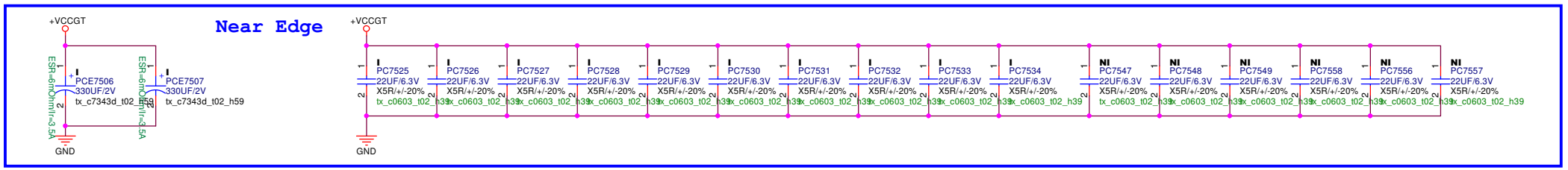
Vcore Output CAP

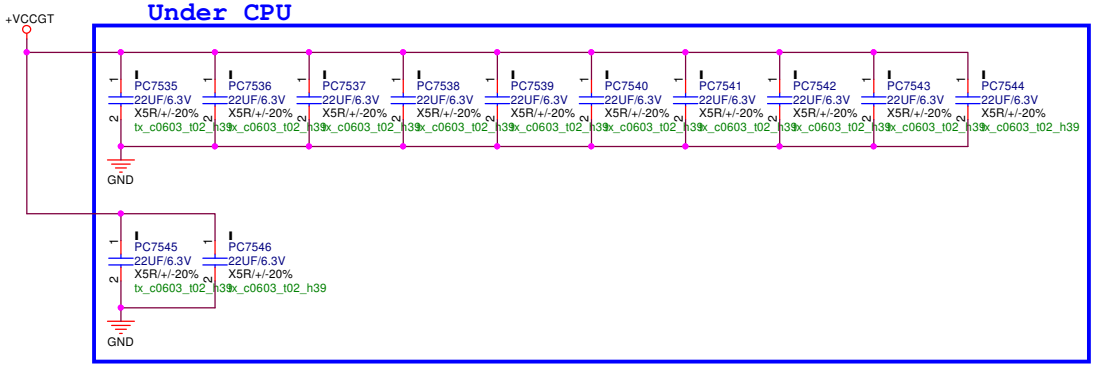




330uF/2V/H=1.4mm * (4+1) ; (I+H82)
470uF/2V/H=2.1mm * 1 (I)
22uF * 14 (I)
47uF * 11 (I)



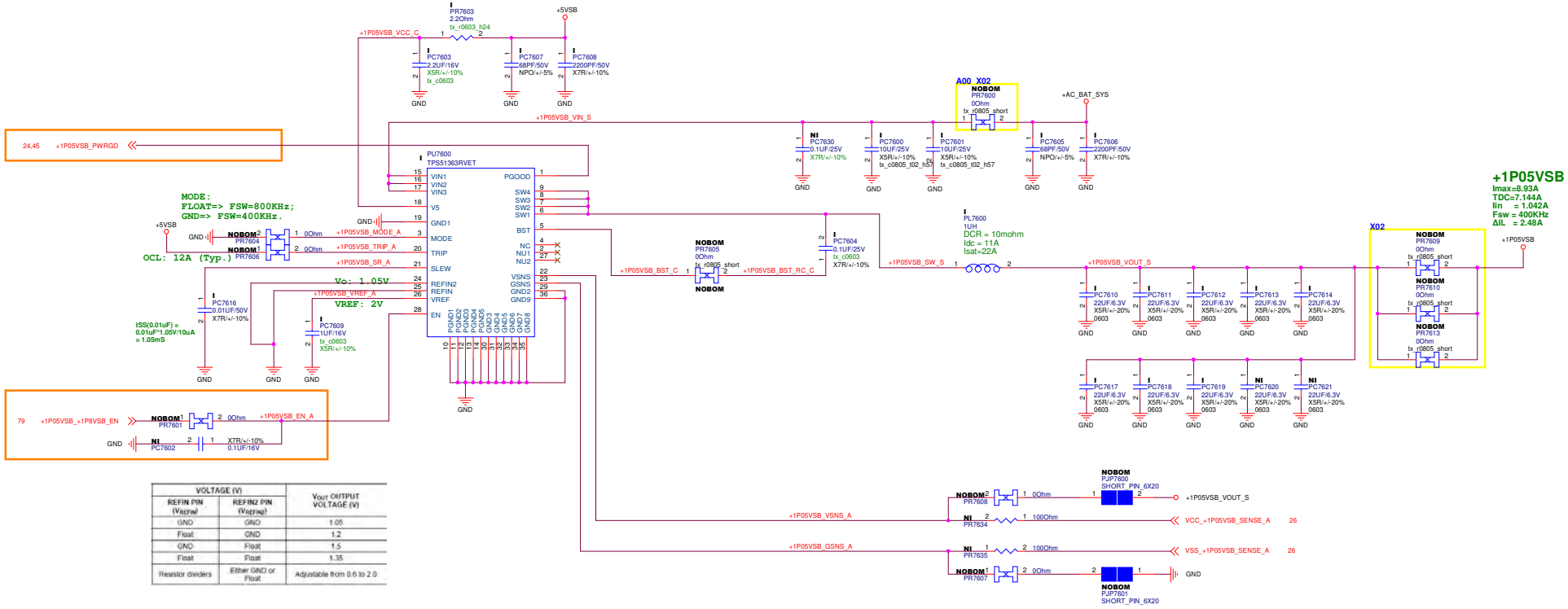




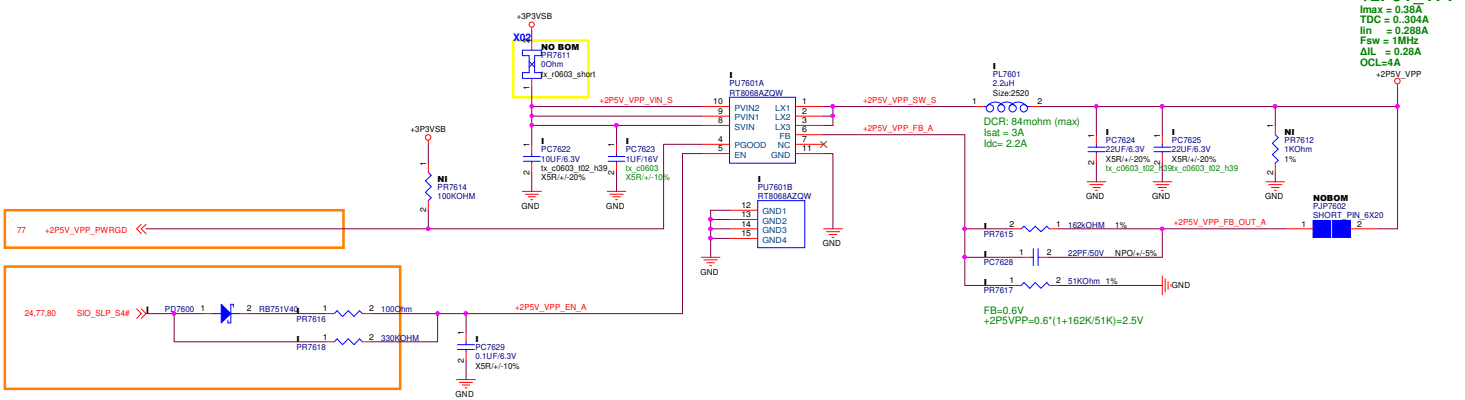
VCCGT Output CAP

330uF/2V/H=1.4mm * 2 (I)
22uF * 22 (I)
22uF * 6 (NI)

PEGATRON	Title : Vcore & VccGT CAP	
Pegatron Corp.	Engineer: Adams_Lin	
Size: Custom	Project Name: Hela	Rev: A00
Date: Monday, April 20, 2020	Sheet 75 of 96	



VOLTAGE (V)		
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	V_{OUT} OUTPUT VOLTAGE (V)
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

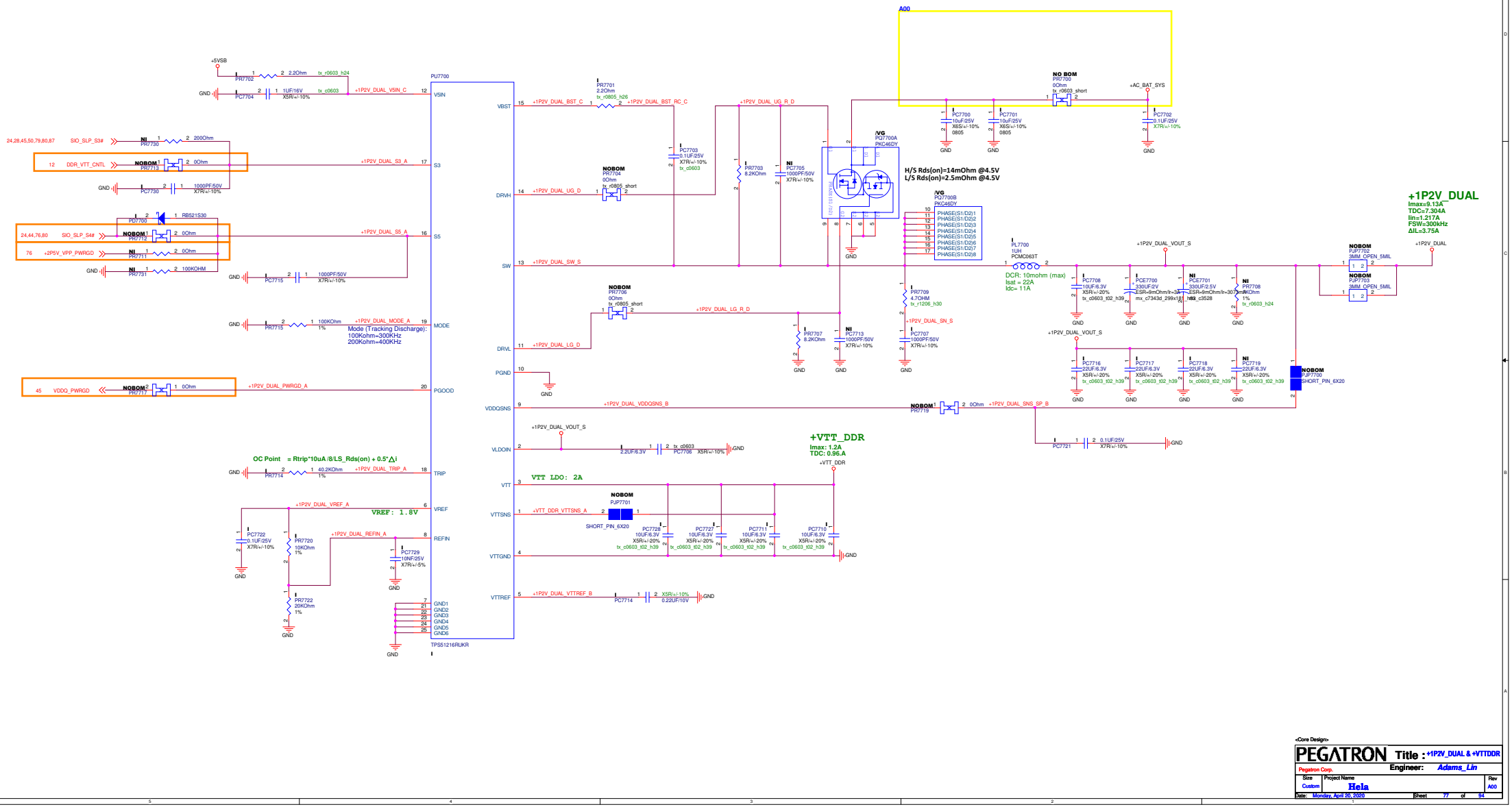


PEGATRON Title : +1P05VSB/+2P5VPP

Pegatron Corp. Engineer: Adams_Lin

Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 78 of 95



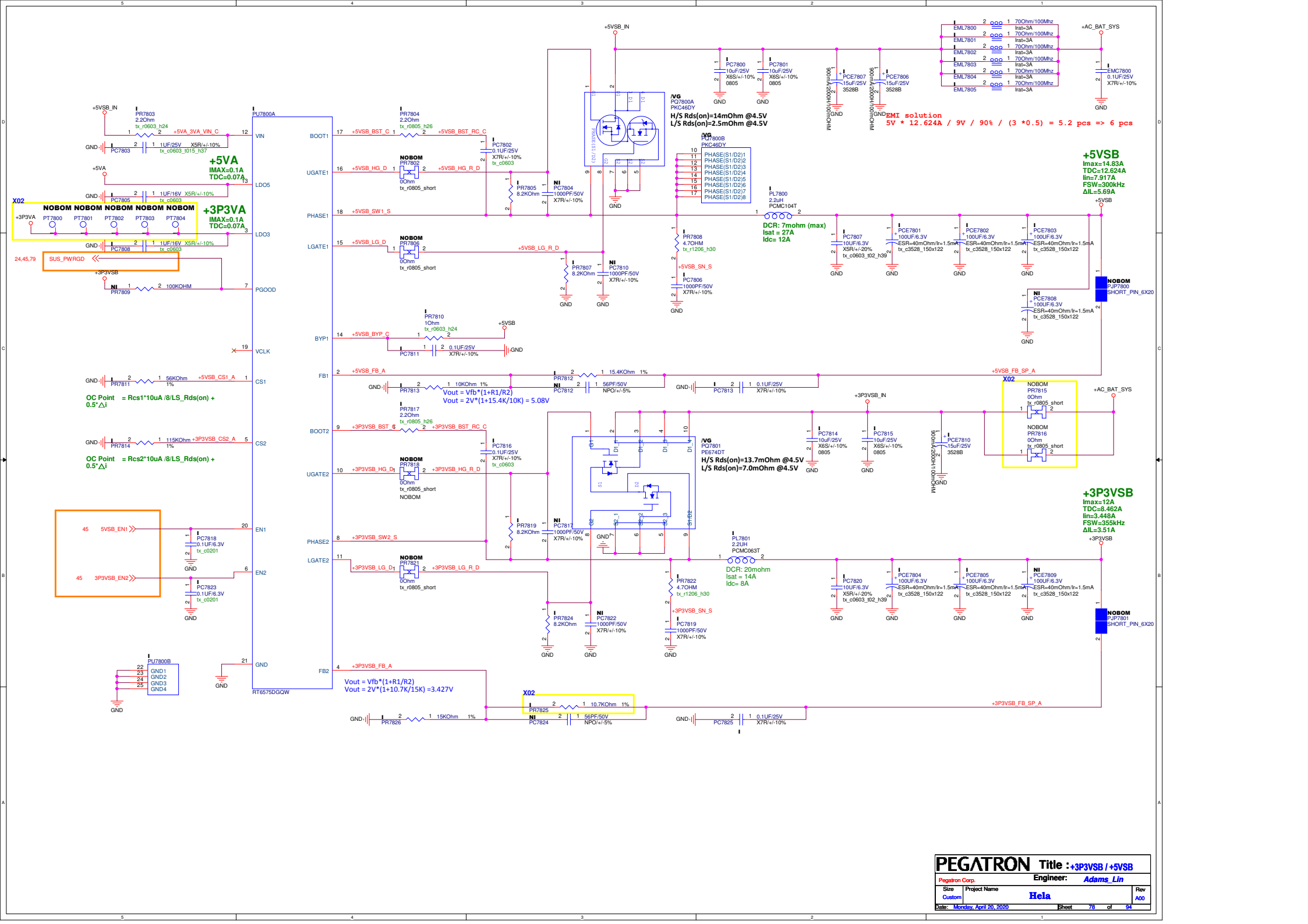
<Core Design>

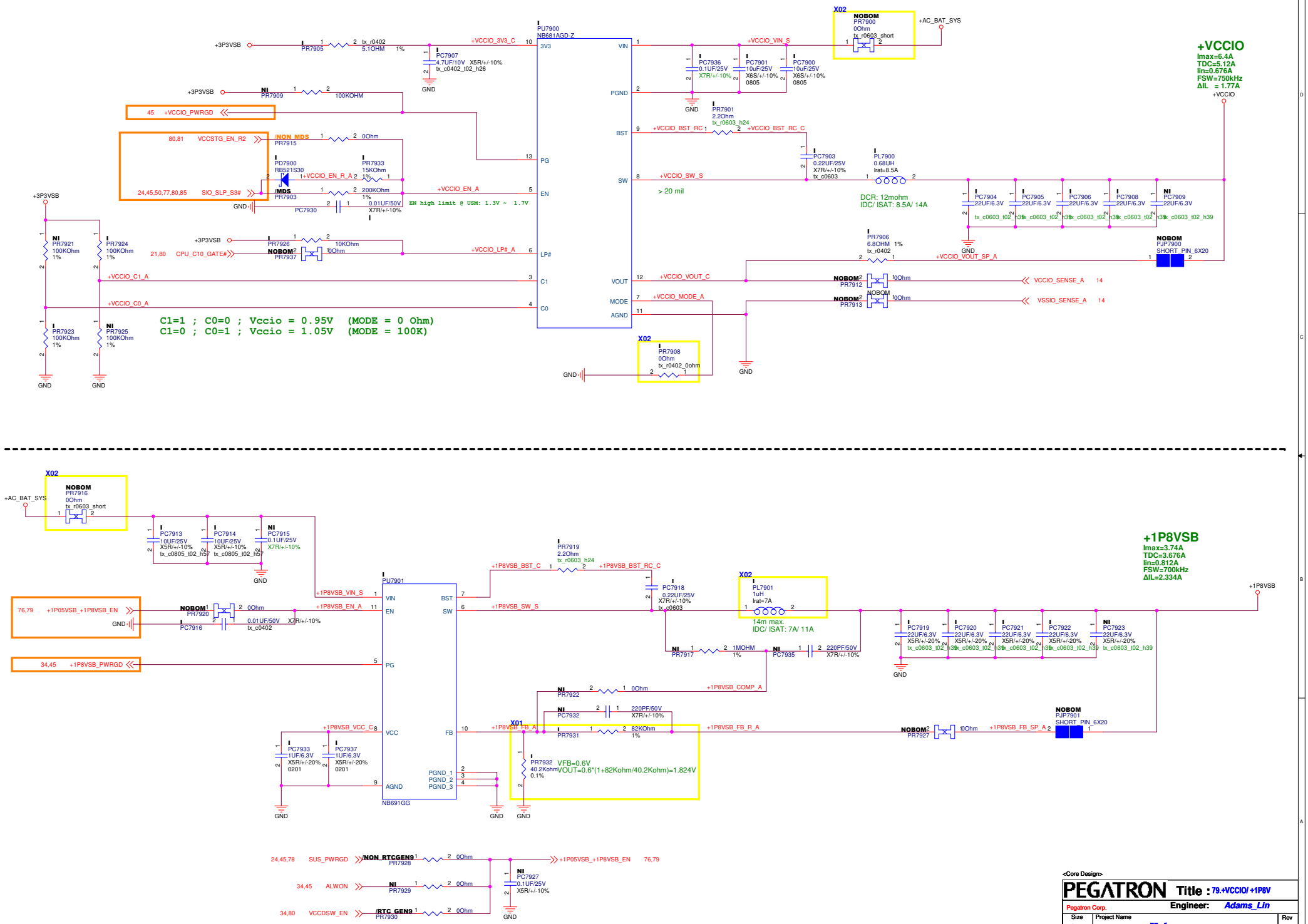
PEGATRON Title : +1P2V_DUAL & +VTTDDR

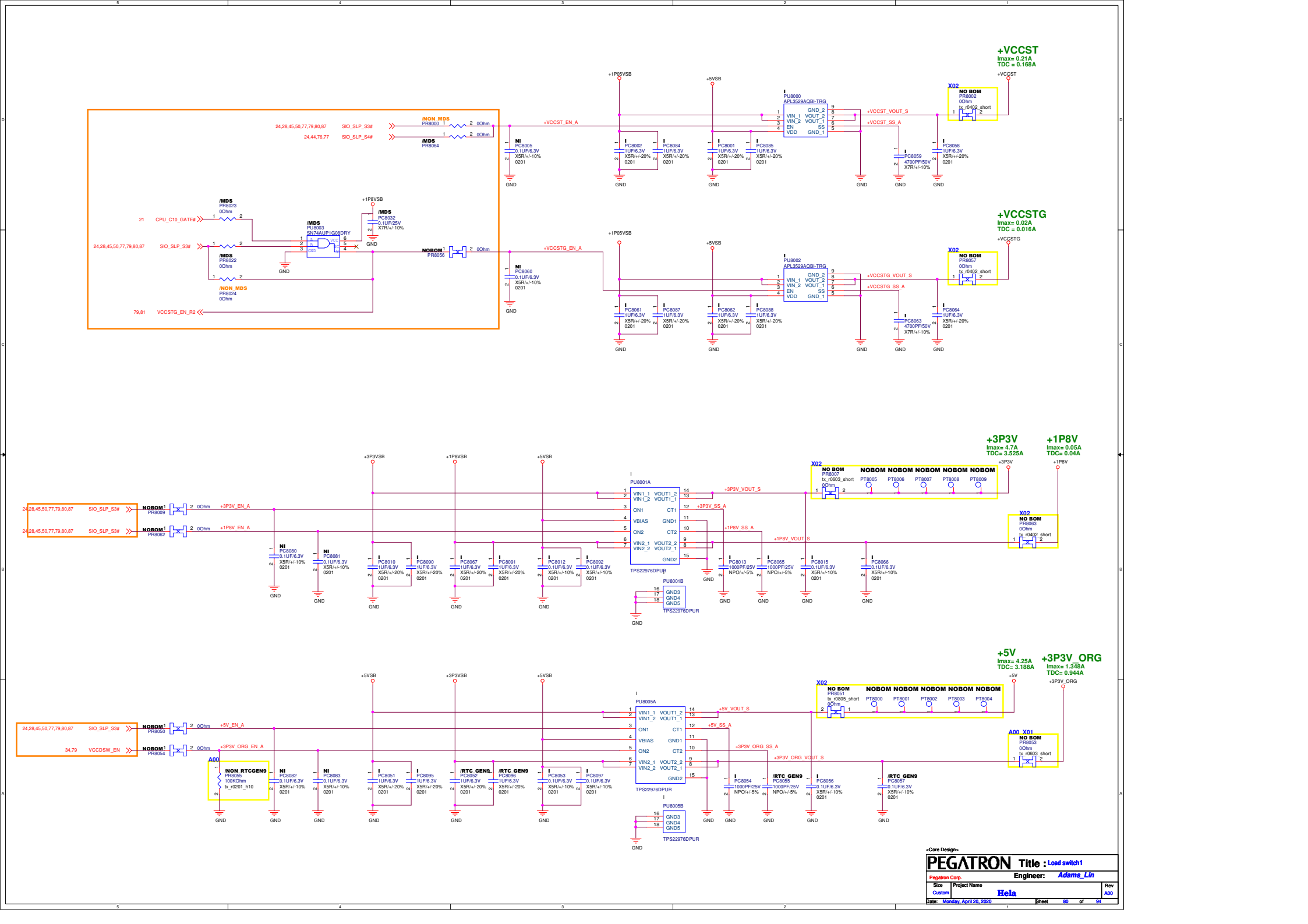
Pegatron Corp. Engineer: Adams_Lin

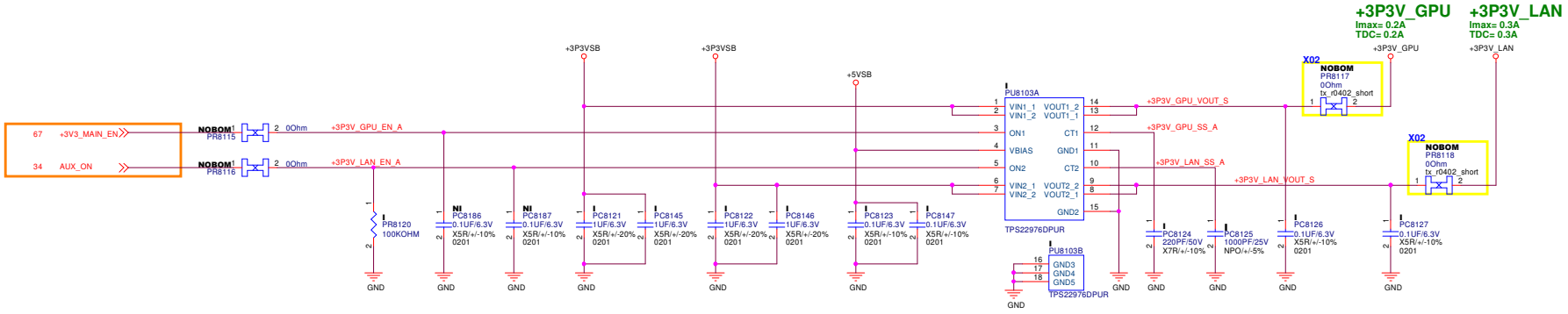
Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 77 of 94


+5VA
IMAX=0.1A
TDC=0.07A
+3P3VA
IMAX=0.1A
TDC=0.07A
NOBOM NOBOM NOBOM NOBOM NOBOM
SUS_PWRGD
PU7800A
RT6575DGQW
VIN
LDO5
LDO3
PGOOD
VCLK
CS1
CS2
EN1
EN2
GND
BOOT1
UGATE1
PHASE1
LGATE1
BYP1
FB1
BOOT2
UGATE2
PHASE2
LGATE2
FB2
+5VSB_IN
/VG
PQ7800A
PKC46DY
H/S Rds(on)=14mOhm @4.5V
L/S Rds(on)=2.5mOhm @4.5V
/VG
PQ7800B
PKC46DY
PL7800
2.2uH
PCMC104T
DCR: 7mohm (max)
Isat = 27A
Idc= 12A
+5VSB
Imax=14.83A
TDC=12.624A
Iin=7.917A
FSW=300kHz
ΔIL=5.69A
EMI solution
5V * 12.624A / 9V / 90% / (3 *0.5) = 5.2 pcs => 6 pcs
Vout = Vfb*(1+R1/R2)
Vout = 2V*(1+15.4K/10K) = 5.08V
OC Point = Rcs1*10uA /8/LS_Rds(on) + 0.5*△i
OC Point = Rcs2*10uA /8/LS_Rds(on) + 0.5*△i
+3P3VSB_IN
/VG
PQ7801
PE674DT
H/S Rds(on)=13.7mOhm @4.5V
L/S Rds(on)=7.0mOhm @4.5V
PL7801
2.2UH
PCMC063T
DCR: 20mohm
Isat = 14A
Idc= 8A
+3P3VSB
Imax=12A
TDC=8.462A
Iin=3.448A
FSW=355kHz
ΔIL=3.51A
Vout = Vfb*(1+R1/R2)
Vout = 2V*(1+10.7K/15K) =3.427V
+AC_BAT_SYS
EML7800
EML7801
EML7802
EML7803
EML7804
EML7805
70Ohm/100Mhz
Irat=3A
PCE7807
15uF/25V
3528B
PCE7806
15uF/25V
3528B
PCE7810
15uF/25V
3528B
PCE7801
100UF/6.3V
ESR=40mOhm/Ir=1.5mA
tx_c3528_150x122
PCE7802
PCE7803
PCE7804
PCE7805
PCE7808
PCE7809
NOBOM
PJP7800
SHORT_PIN_6X20
NOBOM
PJP7801
SHORT_PIN_6X20
PEGATRON
Title : +3P3VSB / +5VSB
Pegatron Corp.
Engineer: Adams_Lin
Size: Custom
Project Name: Hela
Rev: A00
Date: Monday, April 20, 2020
Sheet 78 of 94


+VCCIO
Imax=6.4A
TDC=5.12A
Iin=0.676A
FSW=750kHz
ΔIL = 1.77A
PU7900
NB681AGD-Z
+3P3VSB
PR7905
5.1OHM
+VCCIO_3V3_C
PC7907
4.7UF/10V X5R/+/-10%
tx_c0402_t02_h26
+AC_BAT_SYS
X02
NOBOM
PR7900
0Ohm
tx_r0603_short
PC7936
0.1UF/25V
X7R/+/-10%
PC7901
10uF/25V
X6S/+/-10%
0805
PC7900
10uF/25V
X6S/+/-10%
0805
PR7909
100KOHM
45 +VCCIO_PWRGD
80,81 VCCSTG_EN_R2
/NON_MDS
PR7915
0Ohm
PD7900
RB521S30
+VCCIO_EN_R_A
PR7933
15KOhm
1%
24,45,50,77,80,85 SIO_SLP_S3#
/MDS
PR7903
200KOhm
1%
+VCCIO_EN_A
PC7930
0.01UF/50V
X7R/+/-10%
EN high limit @ USM: 1.3V ~ 1.7V
PR7901
2.2Ohm
tx_r0603_h24
+VCCIO_BST_RC
+VCCIO_BST_RC_C
PC7903
0.22UF/25V
X7R/+/-10%
tx_c0603
PL7900
0.68UH
Irat=8.5A
> 20 mil
DCR: 12mohm
IDC/ ISAT: 8.5A/ 14A
PC7904
PC7905
PC7906
PC7908
PC7909
22UF/6.3V
tx_c0603_t02_h39
NOBOM
PJP7900
SHORT_PIN_6X20
PR7906
6.8OHM 1%
tx_r0402
+VCCIO_VOUT_SP_A
+VCCIO_VOUT_C
NOBOM
PR7912
PR7913
10Ohm
VCCIO_SENSE_A 14
VSSIO_SENSE_A 14
+VCCIO_MODE_A
+VCCIO_LP#_A
+VCCIO_C1_A
+VCCIO_C0_A
21,80 CPU_C10_GATE#
PR7926
10KOhm
PR7937
10Ohm
PR7921
PR7924
PR7923
PR7925
100KOhm
1%
C1=1 ; C0=0 ; Vccio = 0.95V (MODE = 0 Ohm)
C1=1 ; C0=1 ; Vccio = 1.05V (MODE = 100K)
PR7908
0Ohm
tx_r0402_0ohm
+1P8VSB
Imax=3.74A
TDC=3.676A
Iin=0.812A
FSW=700kHz
ΔIL=2.334A
+AC_BAT_SYS
PR7916
PC7913
PC7914
PC7915
10UF/25V
X5R/+/-10%
tx_c0805_t02_h57
0.1UF/25V
X7R/+/-10%
PR7919
2.2Ohm
tx_r0603_h24
+1P8VSB_BST_C
+1P8VSB_BST_RC_C
PC7918
0.22UF/25V
X7R/+/-10%
tx_c0603
PL7901
1uH
Irat=7A
14m max.
IDC/ ISAT: 7A/ 11A
PC7919
PC7920
PC7921
PC7922
PC7923
22UF/6.3V
X5R/+/-20%
tx_c0603_t02_h39
76,79 +1P05VSB_+1P8VSB_EN
PR7920
0Ohm
PC7916
0.01UF/50V
X7R/+/-10%
tx_c0402
+1P8VSB_VIN_S
+1P8VSB_EN_A
+1P8VSB_SW_S
PR7917
1MOHM
PC7935
220PF/50V
X7R/+/-10%
34,45 +1P8VSB_PWRGD
PR7922
0Ohm
+1P8VSB_COMP_A
PC7932
220PF/50V
X7R/+/-10%
PR7931
82KOhm
1%
+1P8VSB_FB_A
+1P8VSB_FB_R_A
PR7927
10Ohm
+1P8VSB_FB_SP_A
NOBOM
PJP7901
SHORT_PIN_6X20
+1P8VSB_VCC_C
PC7933
PC7937
1UF/6.3V
X5R/+/-20%
0201
PR7932 VFB=0.6V
40.2KohmVOUT=0.6*(1+82Kohm/40.2Kohm)=1.824V
0.1%
PU7901
VIN
EN
PG
VCC
AGND
BST
SW
FB
PGND_1
PGND_2
PGND_3
NB691GG
X01
24,45,78 SUS_PWRGD
/NON_RTCGEN9
PR7928
+1P05VSB_+1P8VSB_EN 76,79
34,45 ALWON
PR7929
PC7927
0.1UF/25V
X5R/+/-10%
34,80 VCCDSW_EN
/RTC_GEN9
PR7930
<Core Design>
PEGATRON
Title : 79.+VCCIO/ +1P8V
Pegatron Corp.
Engineer: Adams_Lin
Size Custom
Project Name Hela
Rev A00
Date: Monday, April 20, 2020
Sheet 79 of 94


+VCCST
Imax= 0.21A
TDC = 0.168A
+VCCSTG
Imax= 0.02A
TDC = 0.016A
+3P3V
Imax= 4.7A
TDC= 3.525A
+1P8V
Imax= 0.05A
TDC= 0.04A
+5V
Imax= 4.25A
TDC= 3.188A
+3P3V_ORG
Imax= 1.348A
TDC= 0.944A
PU8000 APL3529AQBI-TRG
PU8002 APL3529AQBI-TRG
PU8003 SN74AUP1G08DRY
PU8001A TPS22976DPUR
PU8001B TPS22976DPUR
PU8005A TPS22976DPUR
PU8005B TPS22976DPUR
NO BOM
NOBOM NOBOM NOBOM NOBOM NOBOM
PEGATRON
Title : Load switch1
Engineer: Adams_Lin
Pegatron Corp.
Size Custom
Project Name Hela
Rev A00
Date: Monday, April 20, 2020
Sheet 80 of 94



PEGATRON	Title :	Load switch2	
Pegatron Corp.	Engineer:	Adams_Lin	
Size: Custom	Project Name: Hela		Rev: A00
Date: Monday, April 20, 2020	Sheet 81 of 94		

/N18E-G1R_G2R => PU8200 BOM:
06T95M026N00 / 0695-018L000 (NCP81610MNTXG)

/N18E-G0 => PU8201 BOM:
06T95M030N00 / 0695-019U000 (NCP81611MNTXG)

Co-lay PU8200A/PU8201A

N18E-G1R/N18E-G2R PR8261=21.0K, PR8263=16.2K, PR8265=10.5K, PR8267=2.61K
N18E-G0 PR8282=34.8K, PR8283=26.1K, PR8284=17.4K, PR8286=4.32K

Co-lay PR8261/ PR8282
Co-lay PR8263/ PR8283
Co-lay PR8265/ PR8284
Co-lay PR8267/ PR8286

PHTH4 = 40A (4-Phase)
PHTH3 = 30A (2-Phase)
PHTH2 = 20A (1-Phase CCM)
PHTH1 = 5A (1-Phase DCM)
LPC2 : Full-phase @ boot up
LPC1 : Full-phase @ PSI low
I2C Address setting & Load-line disabled
tSS = 0.15mS

Close to NVVDD PH1 input MLCC

HIGH: 1.45V < VPS
MID: 0.8V < VPSI < 1.0V
LOW: 0.575V > VPSI

※Pull-up CSPx to VCC to disable PWMx output

※PU8200.13~16 could be left floating directly (only NCP81611)

0.3V ≤ Vout ≤ 1.3V
Vboot: 0.8V

N18E-G1R/N18E-G2R OCP=500A, PR8209=19.1K
N18E-G0/N18E-G1-B OCP=300A, PR8209=31.6K

Co-lay PR8209/PR8205

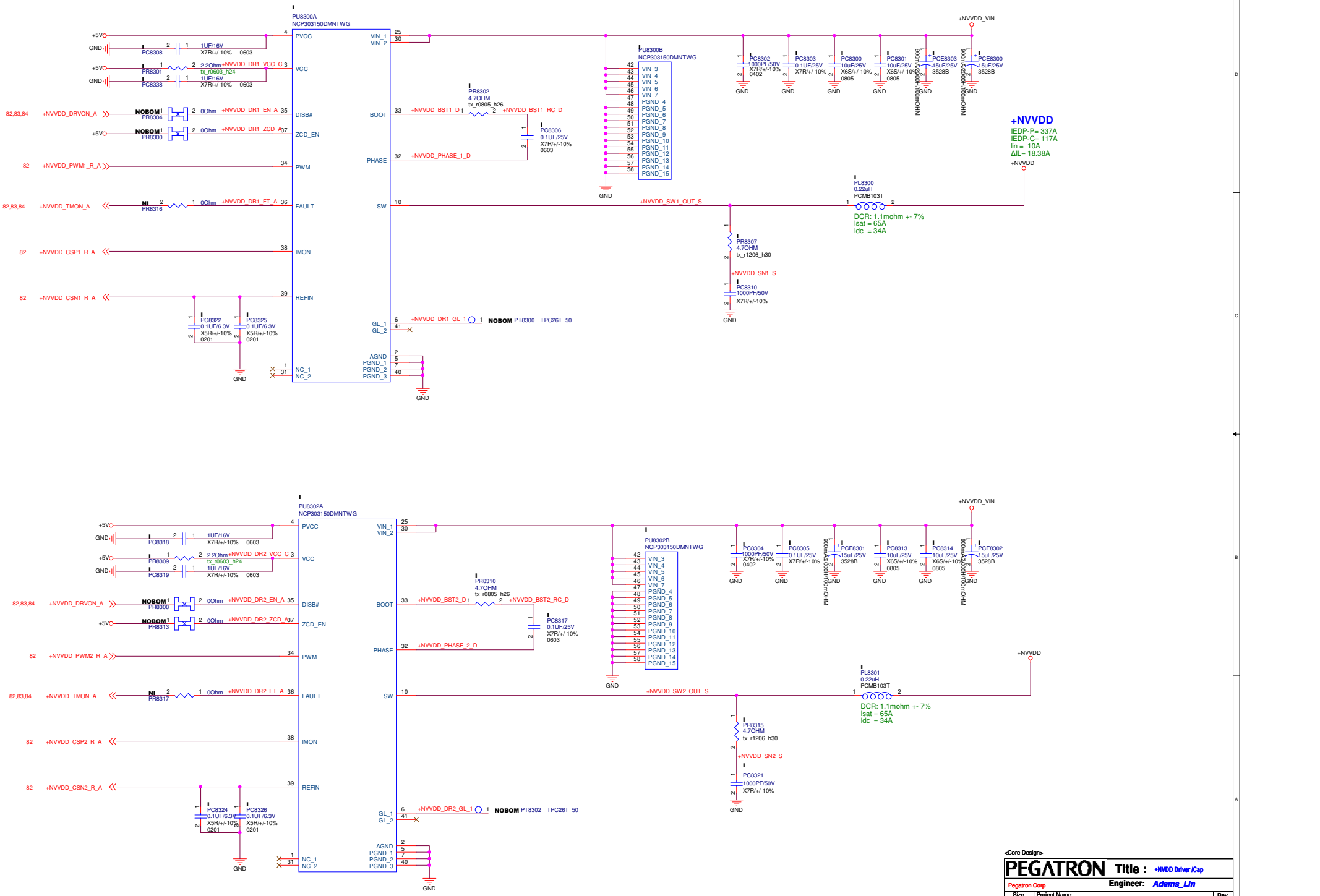
Co-lay PR8226/PR8225

Co-lay PU8200B/PU8201B

[N18E][NVVDD]
Phase = 3, EDPp = 225A, PR8225 = 10k-ohm (FSW = 293-kHz) (N18E-G0)
Phase = 3, EDPp = 225A, PR8226 = 10k-ohm (FSW = 293-kHz) (N18E-G1-B)
Phase = 5, EDPp = 375A, PR8225 = 10k-ohm (FSW = 355-kHz) (N18E-G1R,N18E-G2R)

<core Design>

PEGATRON Title : +NVVDD Controller
Pegatron Corp. Engineer: Adams_Lin
Size: Custom | Project Name: Hela | Rev: A00
Date: Monday, April 20, 2020 | Sheet 82 of 94



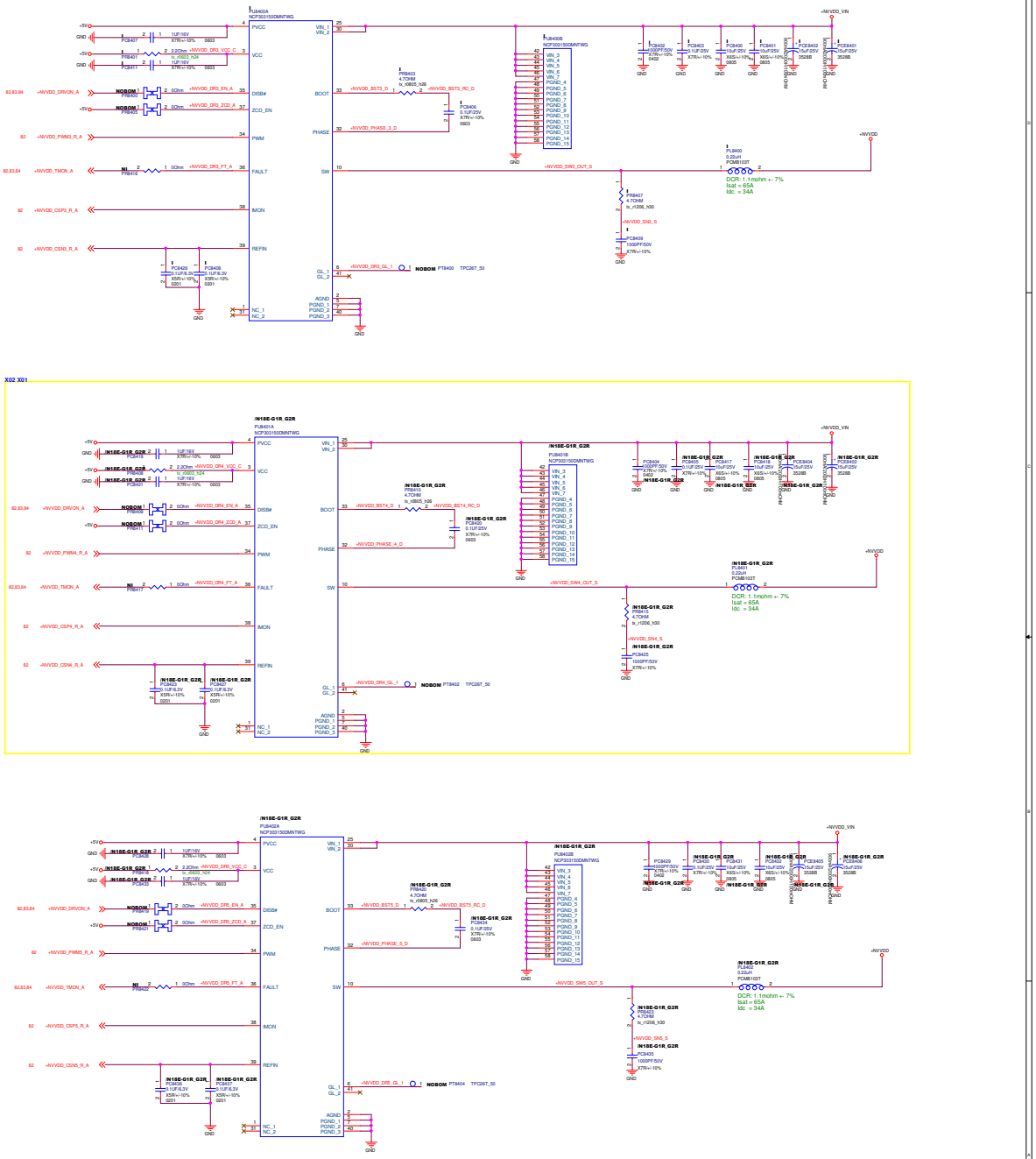
<Core Design>

PEGATRON Title : +NVDD Driver /Cap

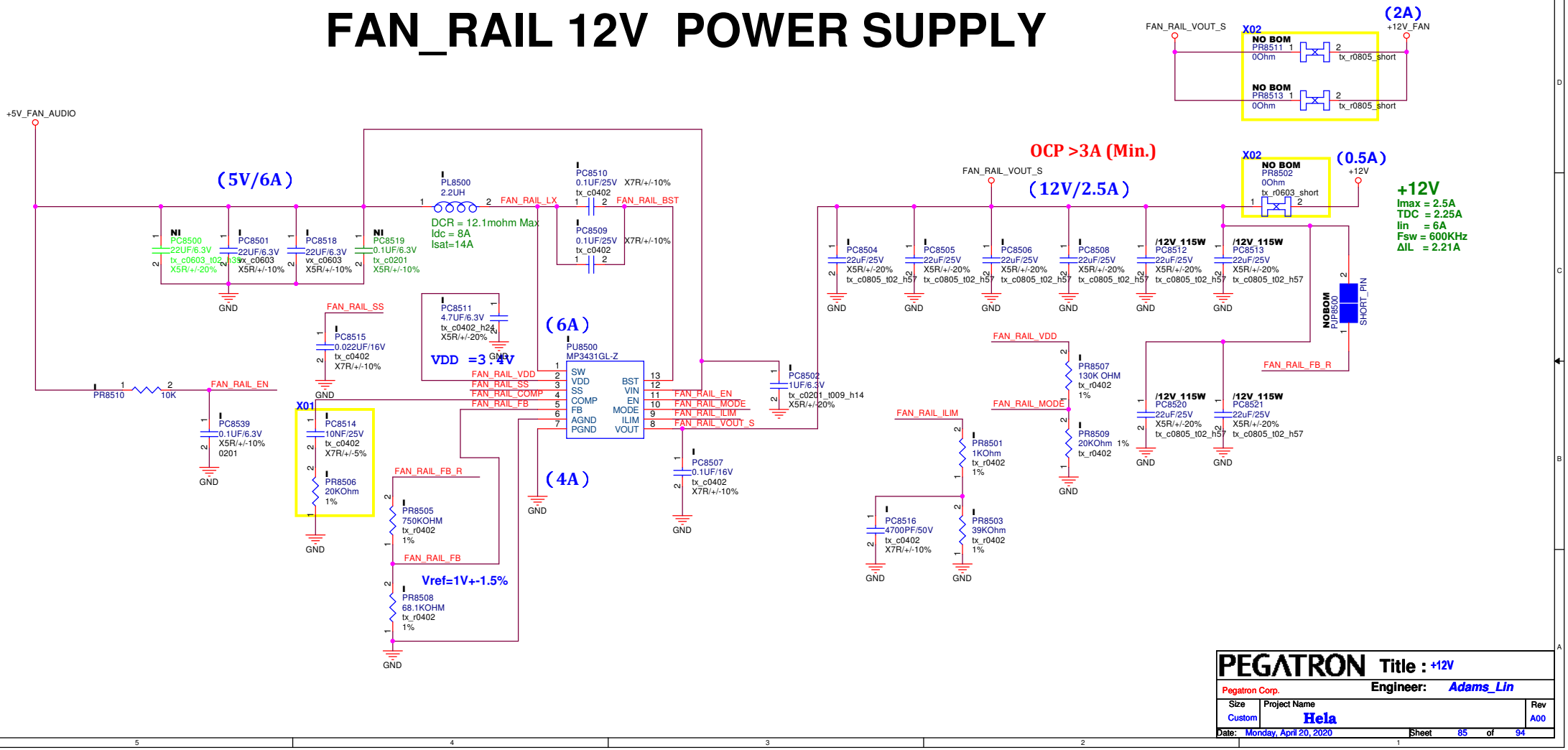
Pegatron Corp. Engineer: Adams_Lin

Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 83 of 94


X02 X01
/N18E-G1R_G2R
PU8401A
NCP303150DMNTWG
PU8401B
NCP303150DMNTWG
+NVVDD_VIN
+NVVDD
PU8400
0.22uH
PCMB103T
DCR: 1.1mohm +- 7%
Isat = 65A
Idc = 34A
PT8400 TPC28T_50
PT8402 TPC28T_50
PT8404 TPC28T_50

FAN_RAIL 12V POWER SUPPLY

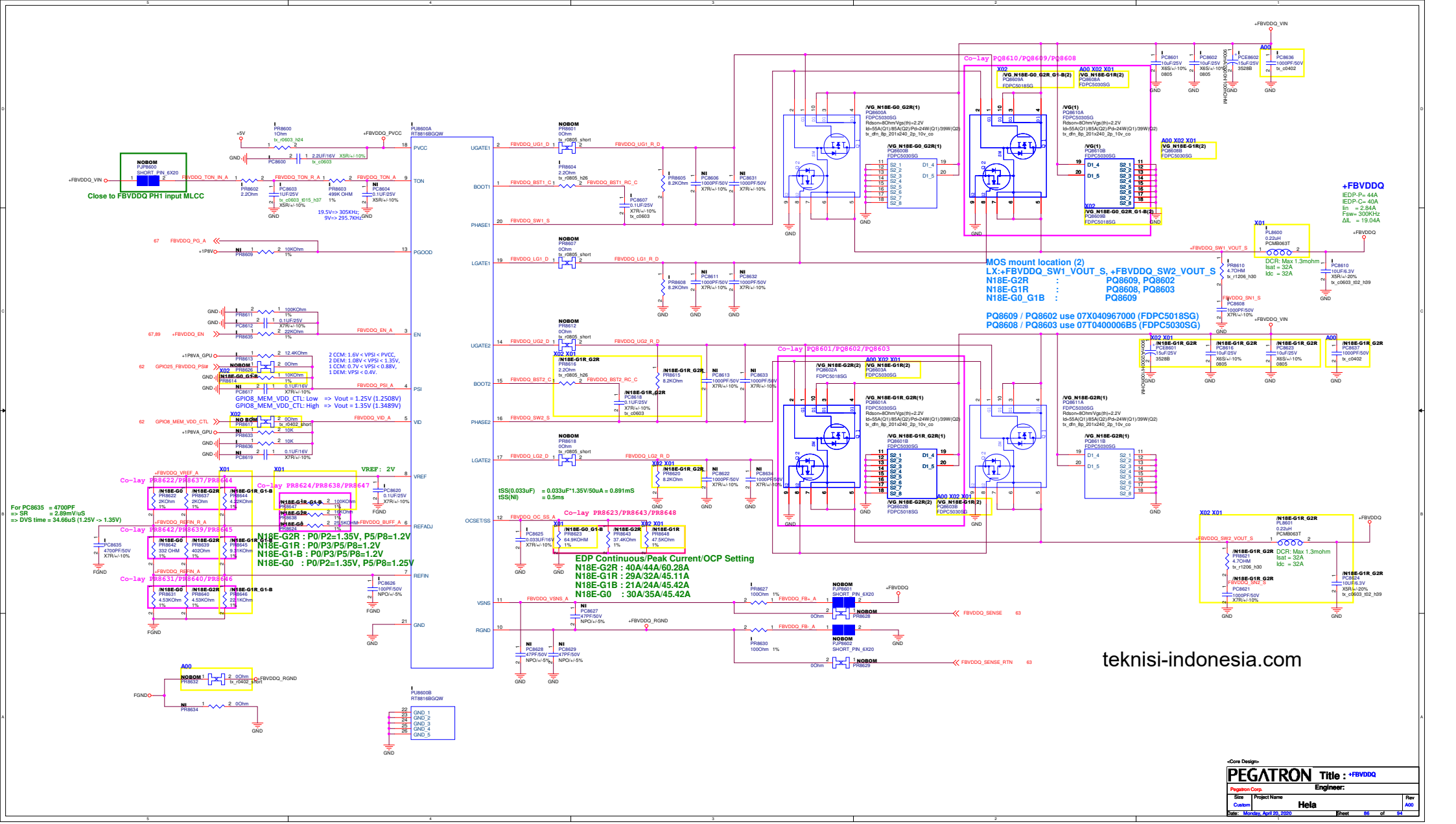


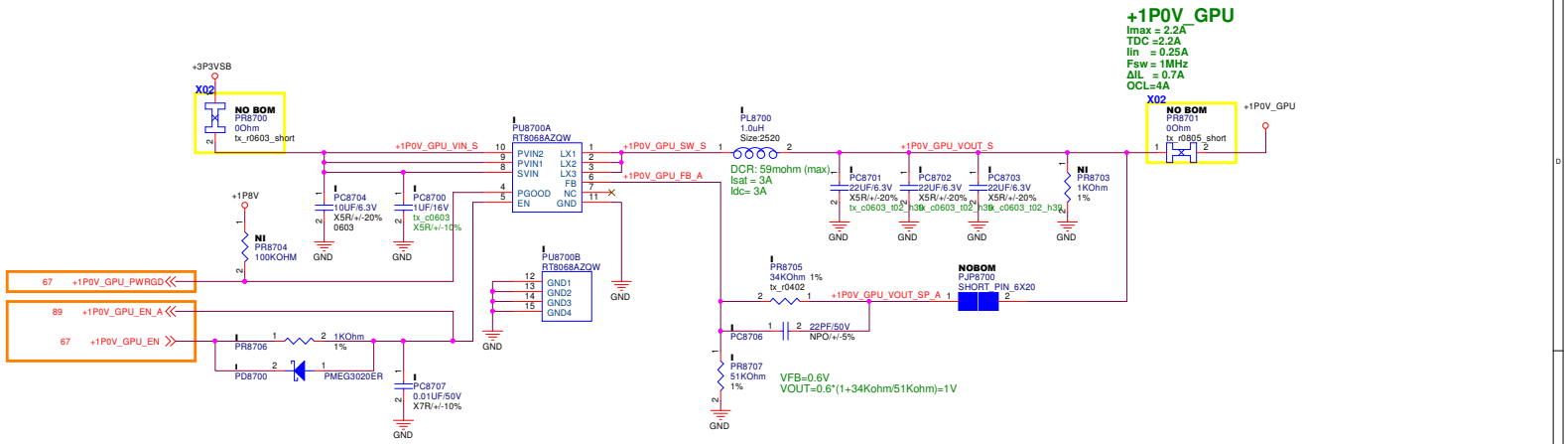
PEGATRON Title : +12V

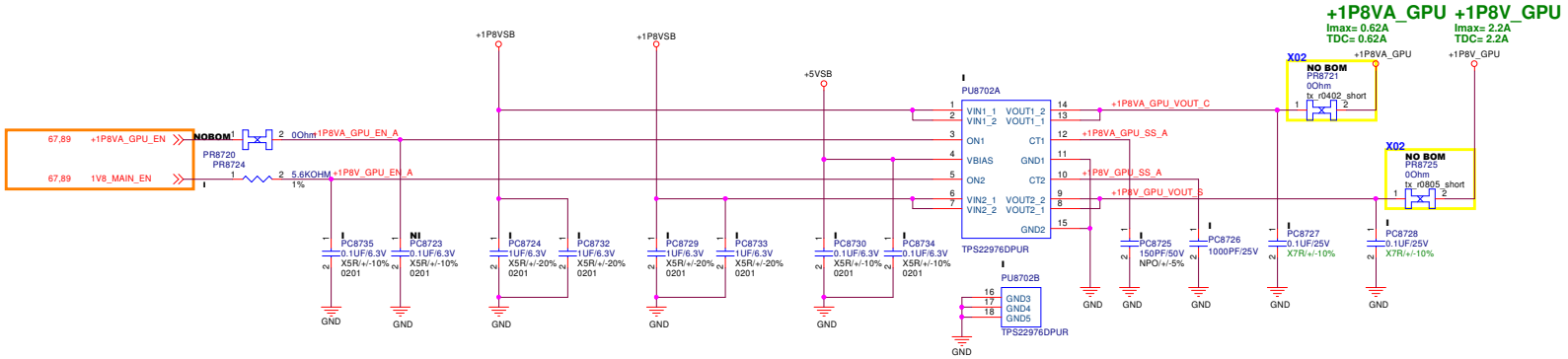
Pegatron Corp. Engineer: Adams_Lin

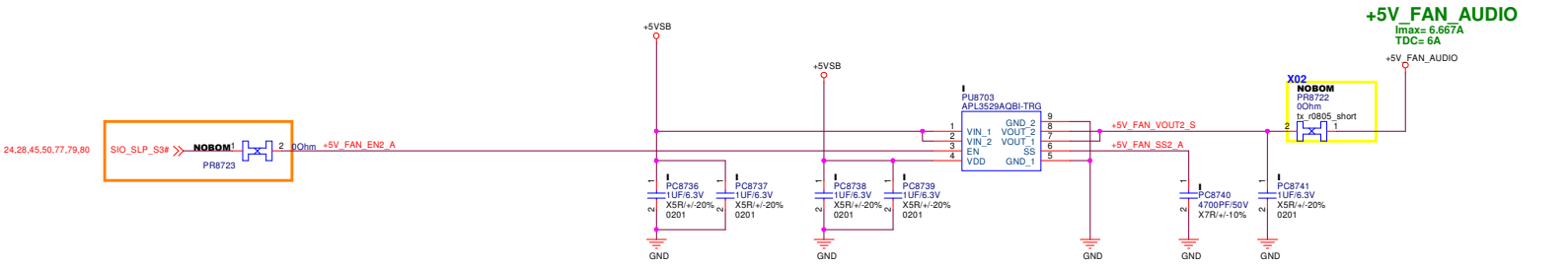
Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 85 of 94


Close to FBVDDQ PH1 input MLCC
19.5V=> 305KHz;
9V=> 295.7KHz
2 CCM: 1.6V < VPSI < PVCC.
2 DEM: 1.08V < VPSI < 1.35V.
1 CCM: 0.7V < VPSI < 0.88V,
1 DEM: VPSI < 0.4V.
GPIO8_MEM_VDD_CTL: Low => Vout = 1.25V (1.2508V)
GPIO8_MEM_VDD_CTL: High => Vout = 1.35V (1.3489V)
For PC8635 = 4700PF
=> SR = 2.89mV/uS
=> DVS time = 34.66uS (1.25V -> 1.35V)
N18E-G2R : P0/P2=1.35V, P5/P8=1.2V
N18E-G1R : P0/P3/P5/P8=1.2V
N18E-G1-B : P0/P3/P5/P8=1.2V
N18E-G0 : P0/P2=1.35V, P5/P8=1.25V
tSS(0.033uF) = 0.033uF*1.35V/50uA = 0.891mS
tSS(Nil) = 0.5ms
EDP Continuous/Peak Current/OCP Setting
N18E-G2R : 40A/44A/60.28A
N18E-G1R : 29A/32A/45.11A
N18E-G1B : 21A/24A/45.42A
N18E-G0 : 30A/35A/45.42A
MOS mount location (2)
LX:+FBVDDQ_SW1_VOUT_S, +FBVDDQ_SW2_VOUT_S
N18E-G2R : PQ8609, PQ8602
N18E-G1R : PQ8608, PQ8603
N18E-G0_G1B : PQ8609
PQ8609 / PQ8602 use 07X040967000 (FDPC5018SG)
PQ8608 / PQ8603 use 07T0400006B5 (FDPC5030SG)
+FBVDDQ
IEDP-P= 44A
IEDP-C= 40A
Iin = 2.84A
Fsw= 300KHz
ΔIL = 19.04A
DCR: Max 1.3mohm
Isat = 32A
Idc = 32A
teknisi-indonesia.com
PEGATRON
Title : +FBVDDQ
Engineer:
Pegatron Corp.
Size: Custom
Project Name: Hela
Rev: A00
Date: Monday, April 20, 2020
Sheet 86 of 94







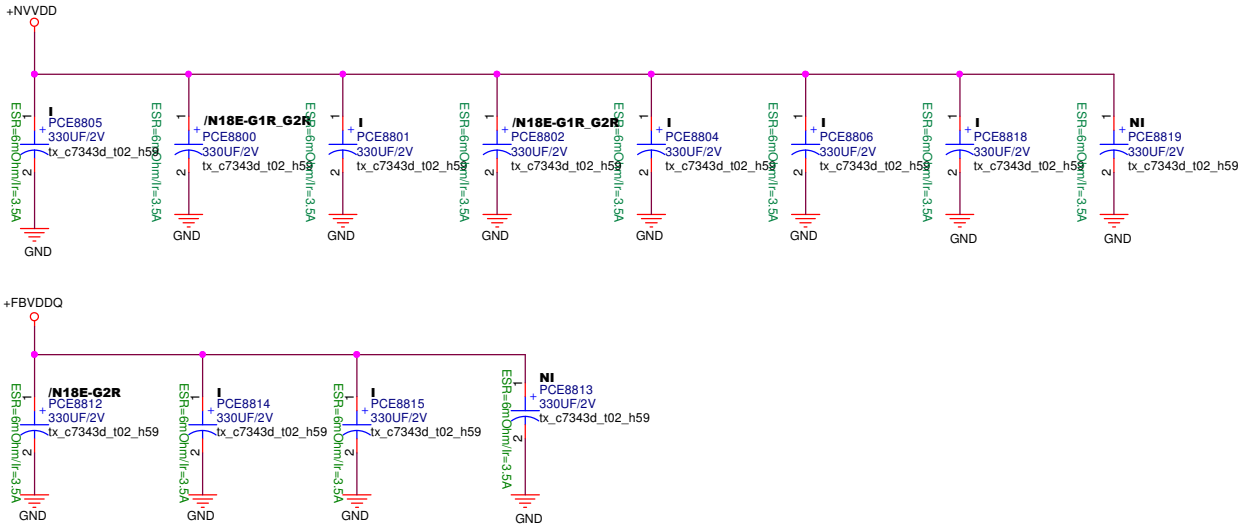
<Core Design>

PEGATRON Title : +1P0V_GPU/+1P8V_GPU & LDO

Pegatron Corp. Engineer: Adams_Lin

Size	Project Name	Rev
Custom	Hela	A00

Date: Monday, April 20, 2020 Sheet 87 of 94



+NVVDD Output CAP(w/ +NVVDDS)

330uF/2V/H=1.5mm * (5+2) ; (I+/N18E-G1R_G2R)
330uF/2V/H=1.5mm * 1(NI)

+FBVDDQ Output CAP

330uF/2V/H=1.5mm * (2+1) ; (I+/N18E-G2R)
330uF/2V/H=1.5mm * 1(NI)

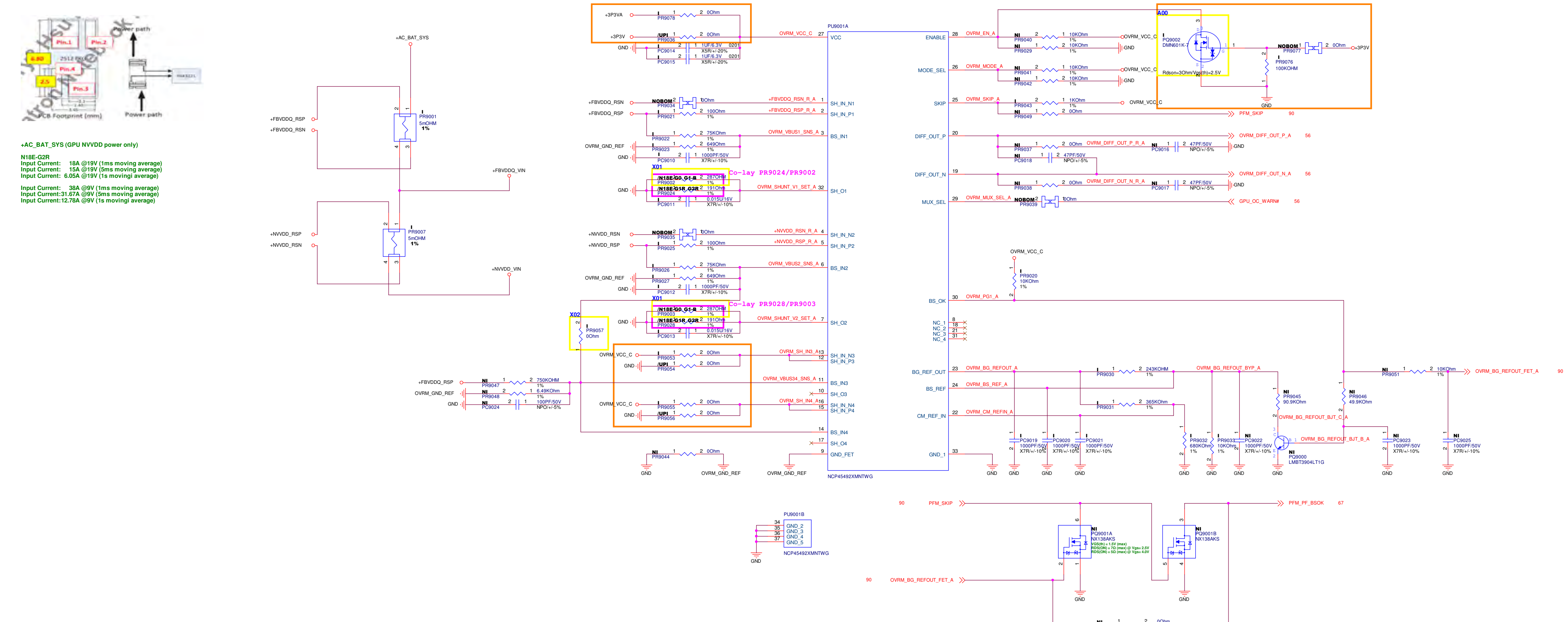
<Core Design>

PEGATRON	Title : GPU_POWER_CAP	
Pegatron Corp.	Engineer: Adams_Lin	
Size: Custom	Project Name: HELA	Rev: A00
Date: Monday, April 20, 2020	Sheet 88 of 94	

+AC_BAT_SYS (GPU NVVDD power only)

N18E-G2R
Input Current: 18A @19V (1ms moving average)
Input Current: 15A @19V (5ms moving average)
Input Current: 6.05A @19V (1s movingi average)

Input Current: 38A @9V (1ms moving average)
Input Current:31.67A @9V (5ms moving average)
Input Current:12.78A @9V (1s movingi average)



PEGATRON	Title : Power_sense		
Pegatron Corp.	Engineer: Adams_Lin		
Size: Custom	Project Name: Hela		Rev: A00
Date: Monday, April 20, 2020	Sheet 90 of 95		

<Core Design>

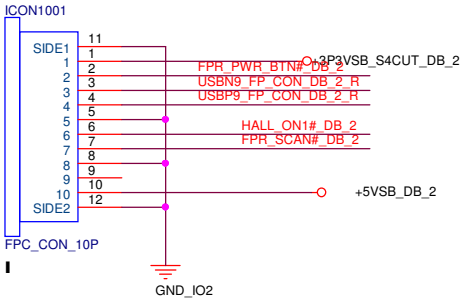
PEGATRON Title : POWER SENSE MAX34417

Pegatron Corp. Engineer: James_Liao

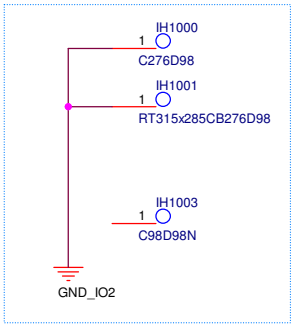
Size	Project Name	Rev
A2	HELA/N18E	X02

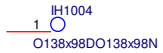
Date: Thursday, April 09, 2020 Sheet 92 of 110

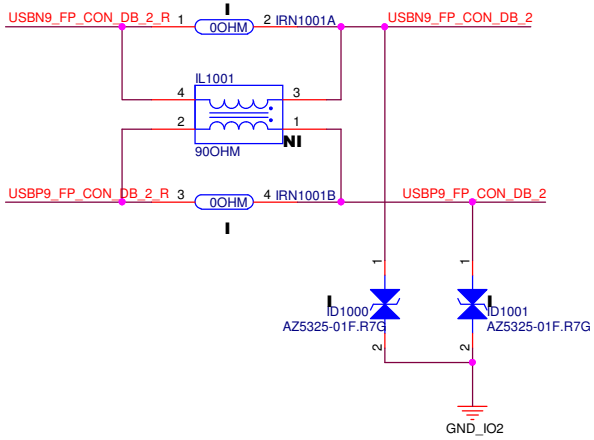
B01.17_IO CONN

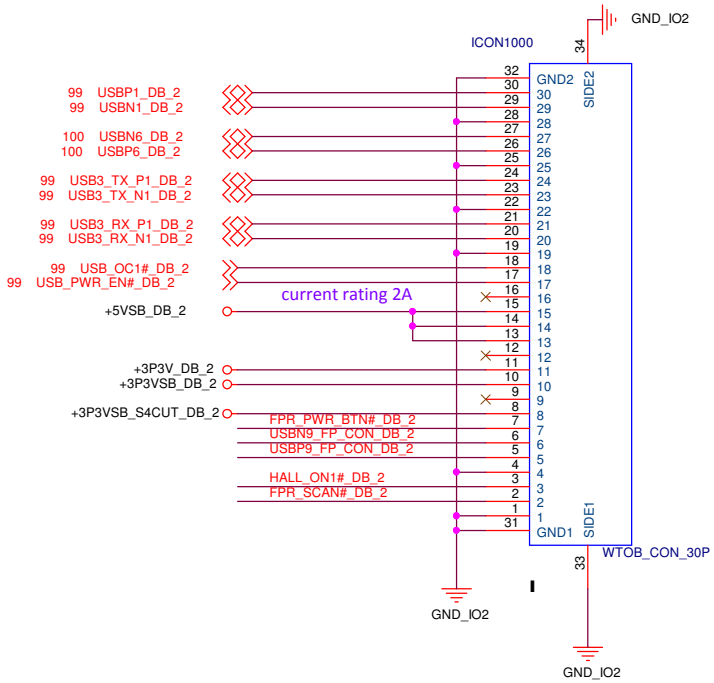


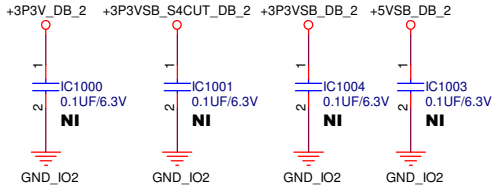
Screw Hole











<Core Design>

PEGATRON Title : IO CONN

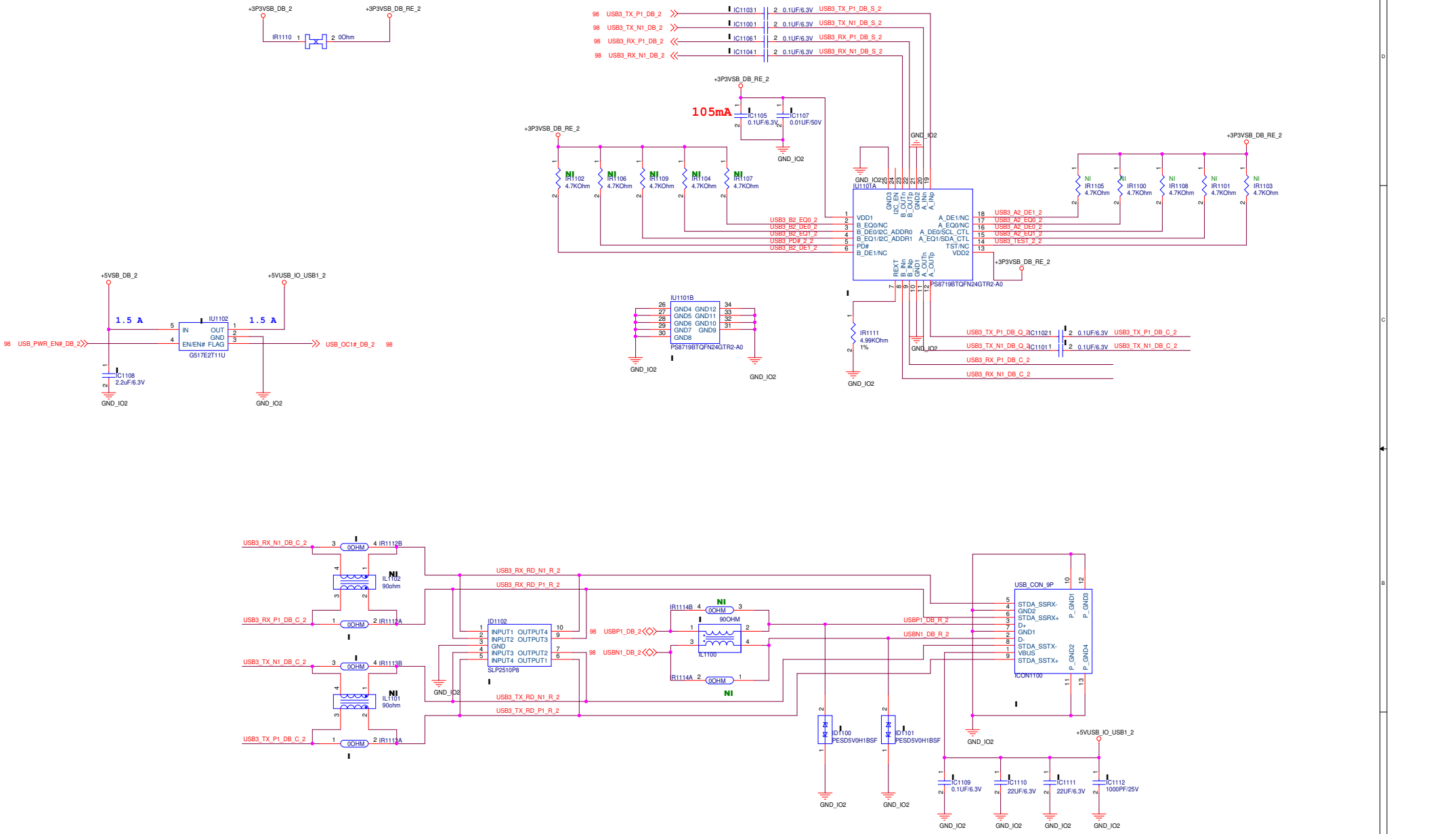
Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
B	HELA/N18P	X02

Date: Thursday, April 09, 2020 Sheet 98 of 110

B02.17_USB 3.0 PORT

Imax: 105mA



<Core Design>

PEGATRON Title : USB 3.0 PORT

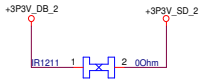
Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
C	HELA/N18E	X02

Date: Thursday, April 09, 2020 Sheet 99 of 110

B03.17_Card_reader_RTS5144-GR

POWER



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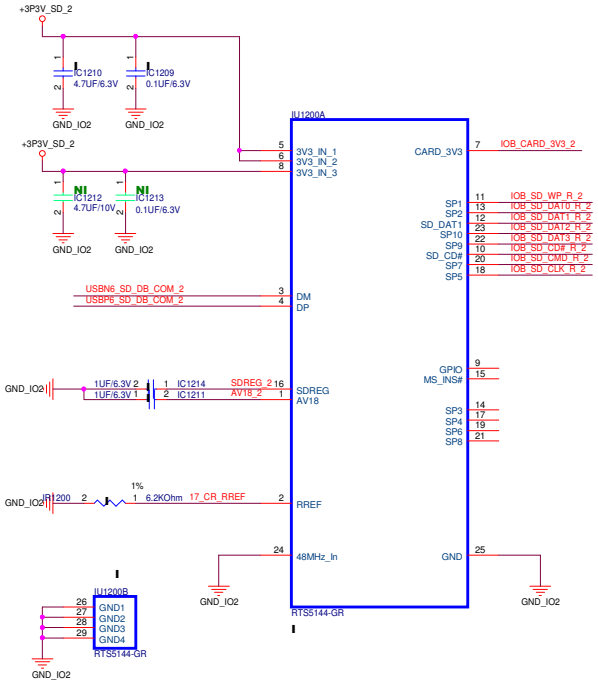
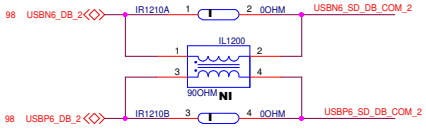
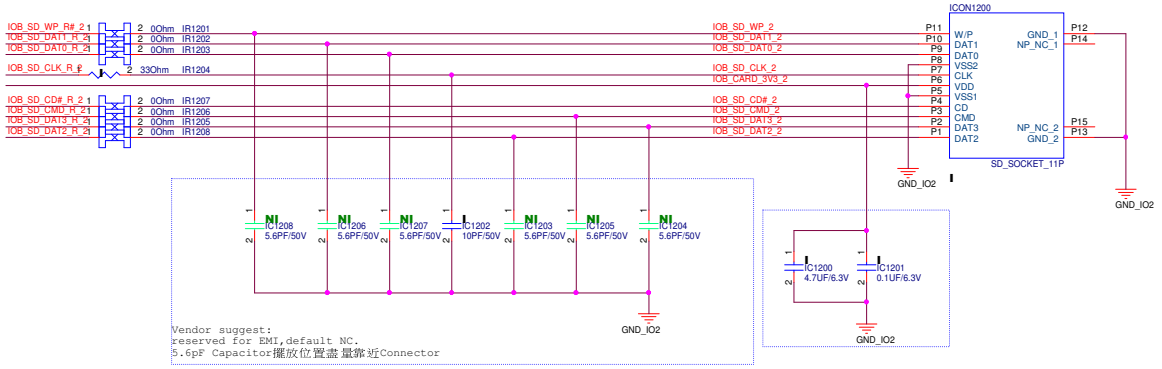
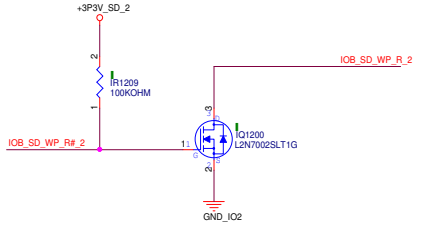




WITHOUT CARD		CARD INSERTED:LOCK		CARD INSERTED:UNLOCK	
W/P	GND	W/P	GND	W/P	GND
C/D	VSS1 P3	C/D	VSS1 P3	C/D	VSS1 P3





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PEGATRON Title : Card_reader_RTS5144GR

Pegatron Corp. Engineer: James_Liao

Size	Project Name	Rev
C	HELA/N18E	X02

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