AMD TR4(X399)

Promontry 300-Series

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Title: COVER SHEET		
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MS-7B09 Ver:1.1

CPU:
AMD TR4

System Chipset:
Promontory X399
(X399 GAMING PRO CARBON AC)

Main Memory:
DDR IV * 8 MAX:256 GB

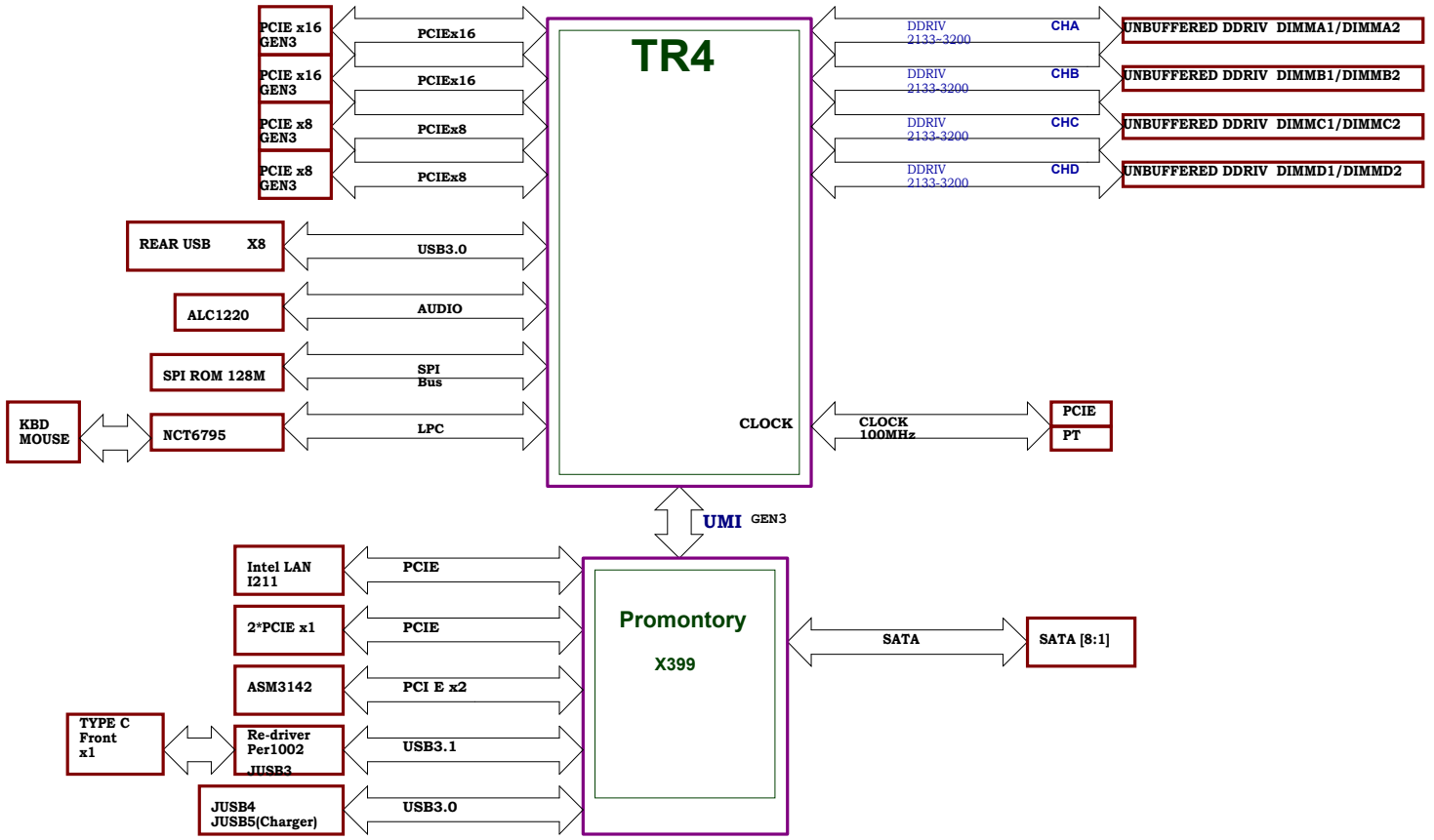
VRM
IR35201-10Phase
IR35201-3Phase

On Board Chipset:
LPC Super I/O --NCT6975
LAN Intel I211
Azalia CODEC - Realtek ALC1220

Expansion Slots:
From CPU
PCI Express X16 Slot * 2
PCI Express X8 Slot * 2

From FCH
PCI Express X1 Slot * 2

X399 BLOCK DIAGRAM



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Title: Block Diagram		
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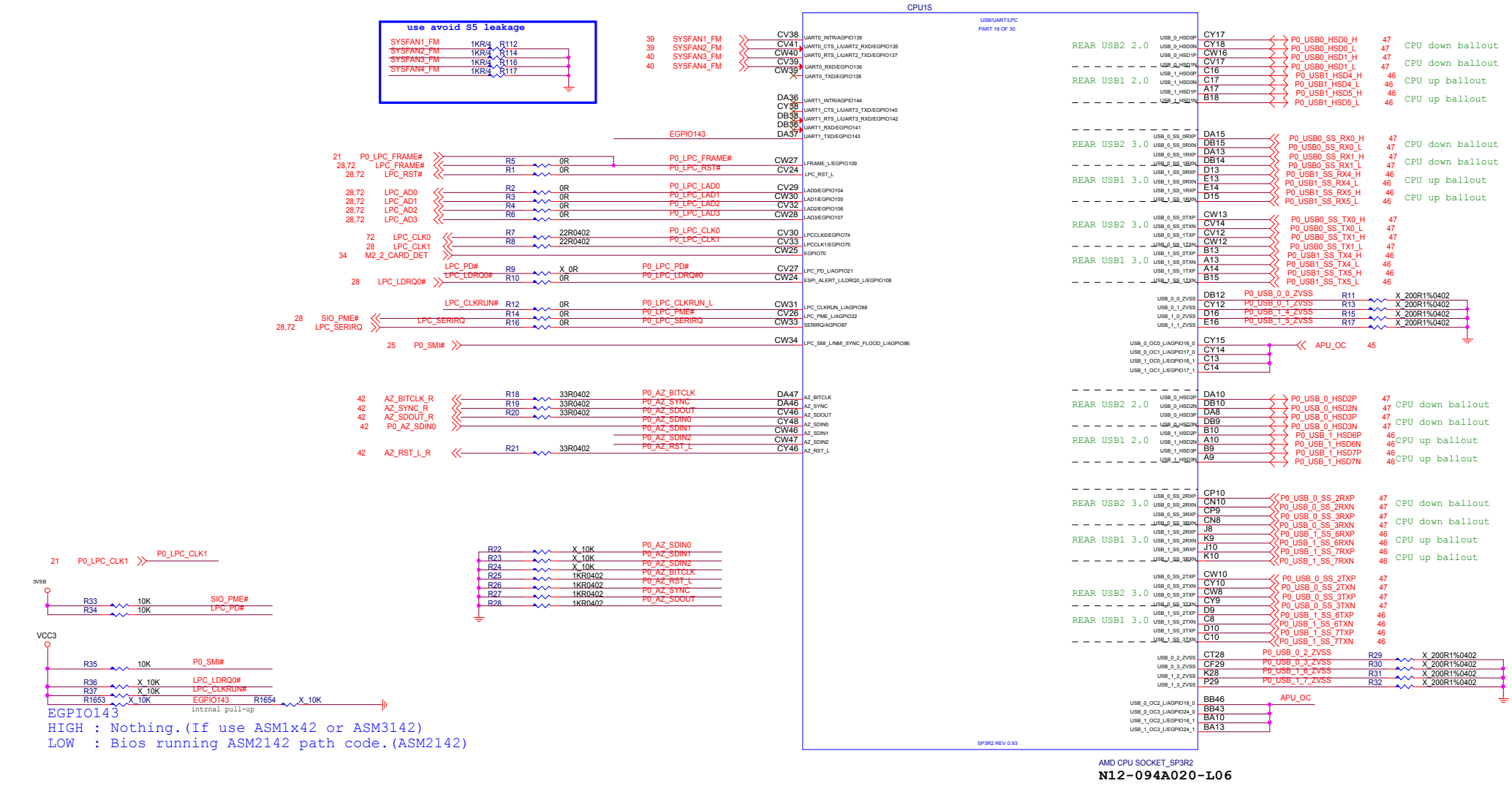
USB/LPC/UART/HDA



Title	TR USB/LPC/UART/HDA		
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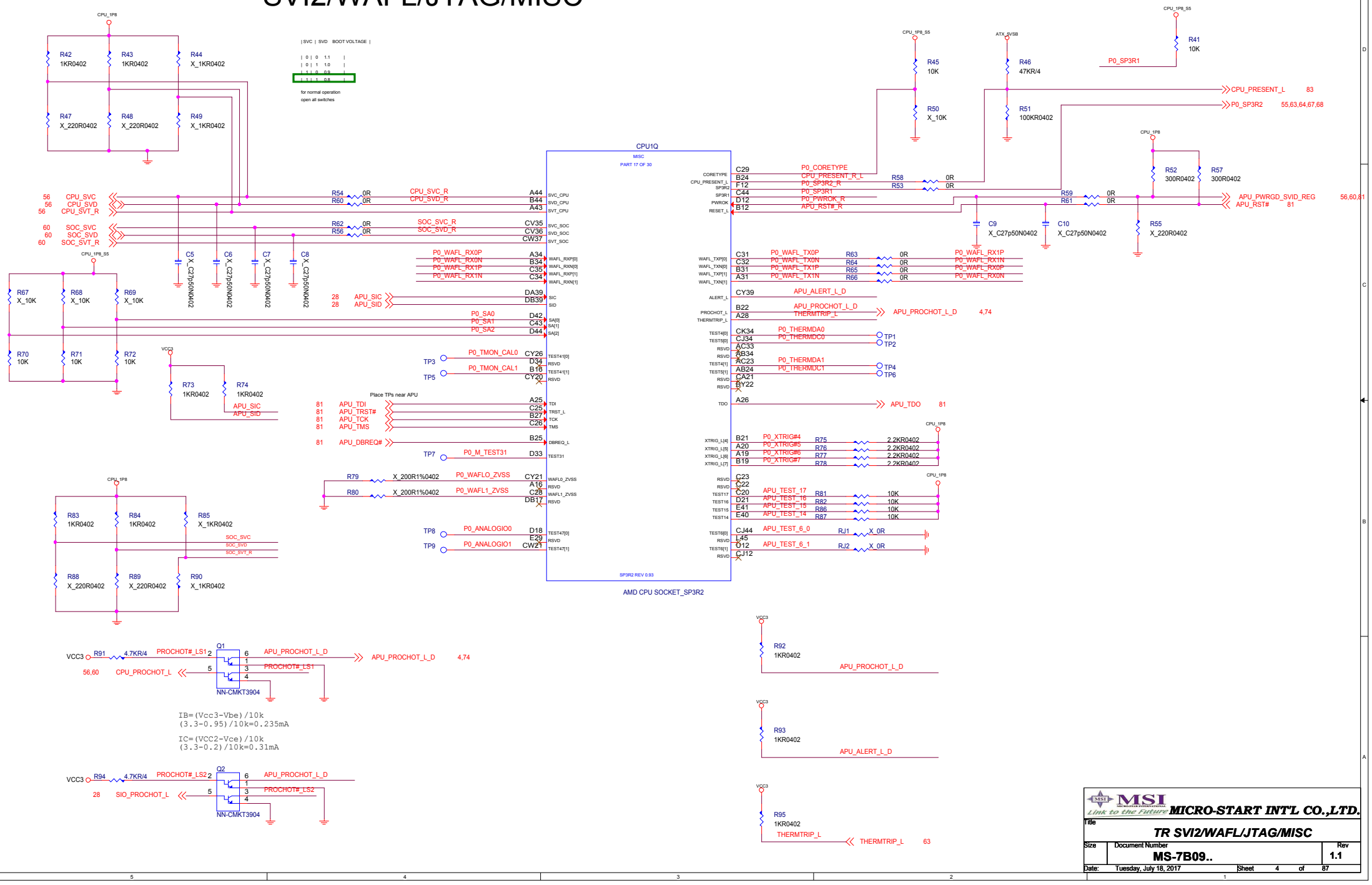
SVI2/WAFL/JTAG/MISC



MSI MICRO-STAR INT'L CO.,LTD.			
Title: TR SVI2/WAFL/JTAG/MISC			
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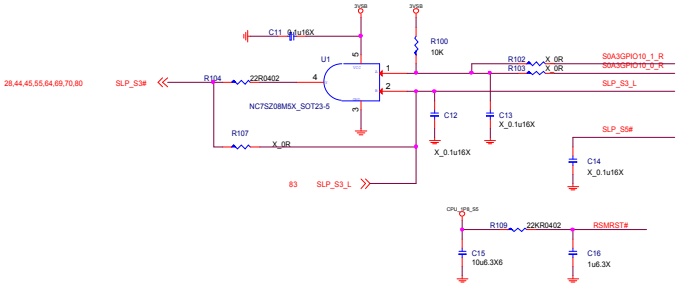
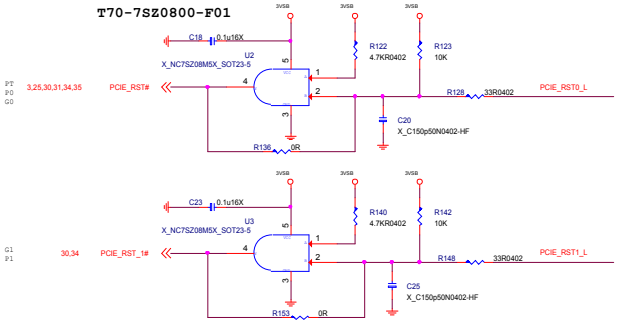
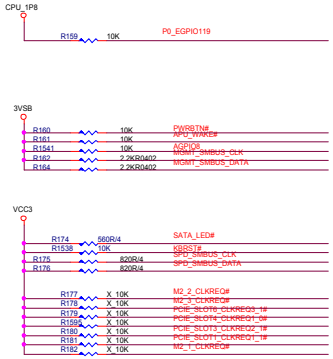
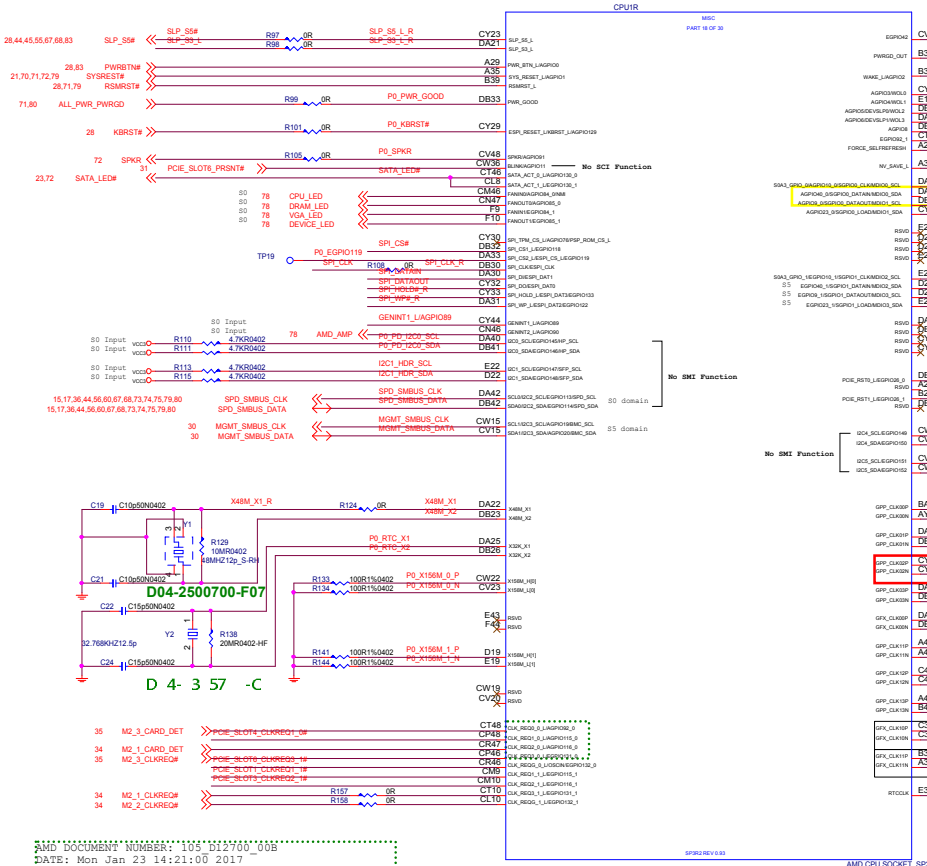
ACPI/SPI/I2C/CLK/GPIO



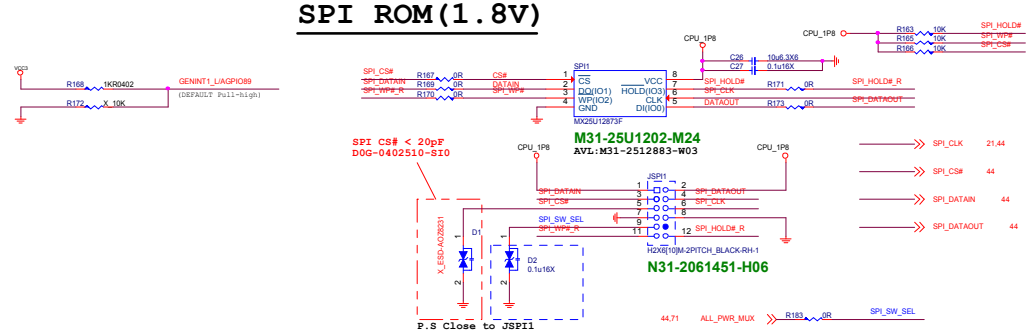


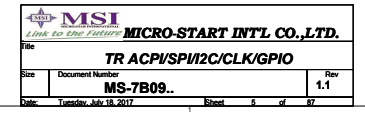




AMD DOCUMENT NUMBER: 105_D12700_00B
DATE: Mon Jan 23 14:21:00 2017
NOTE:
CLK_REQ[3:0]_0_L ARE NOT SUPPORTED ON THREADRIPPER.
PIN CT48,CP48,CR47 AND CP46 CAN ONLY BE USED AS GPIO.

SPI ROM(1.8V)





P0

CPU1M

PCIE

PART 13 OF 30

To PT4

To M2_3

X8,slot6

To PT4

To M2_3

X8,slot6

SP3R2 REV 0.93

AMD CPU SOCKET_SP3R2

G0

CPU1I

GoP

PART 9 OF 30

X16,slot4

X16,slot4

SP3R2 REV 0.93

AMD CPU SOCKET_SP3R2

G1

Change to M2 net

CPU1K

GoP

PART 11 OF 30

To M2_1 SSD-1

To M2_2 SSD-2

X8,slot3

To M2_1 SSD-1

To M2_2 SSD-2

X8,slot3

SP3R2 REV 0.93

AMD CPU SOCKET_SP3R2

P1

CPU1O

PCIE

PART 15 OF 30

X16,slot1

X16,slot1

SP3R2 REV 0.93

AMD CPU SOCKET_SP3R2

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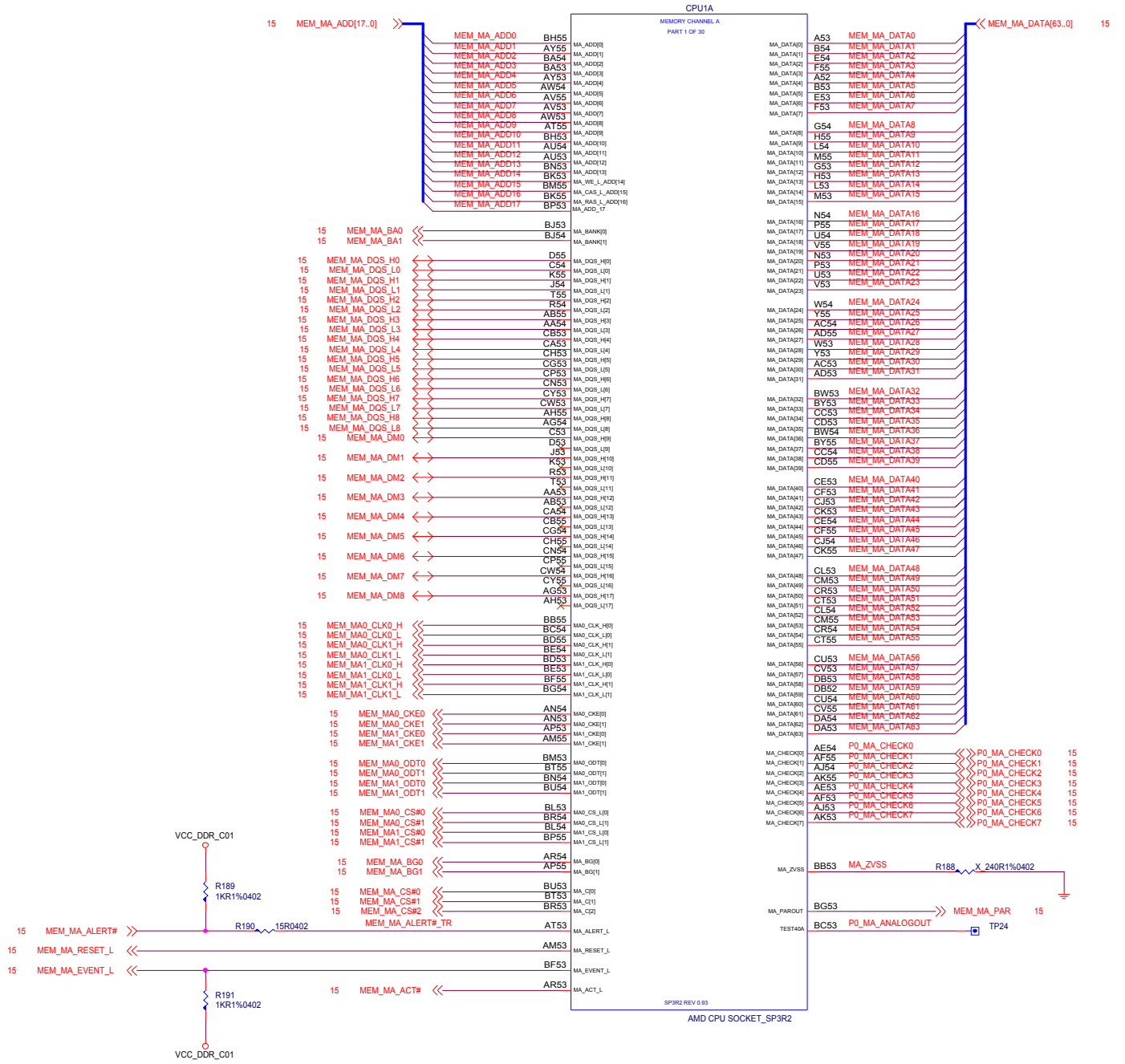

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Title: TR MEMORY A			
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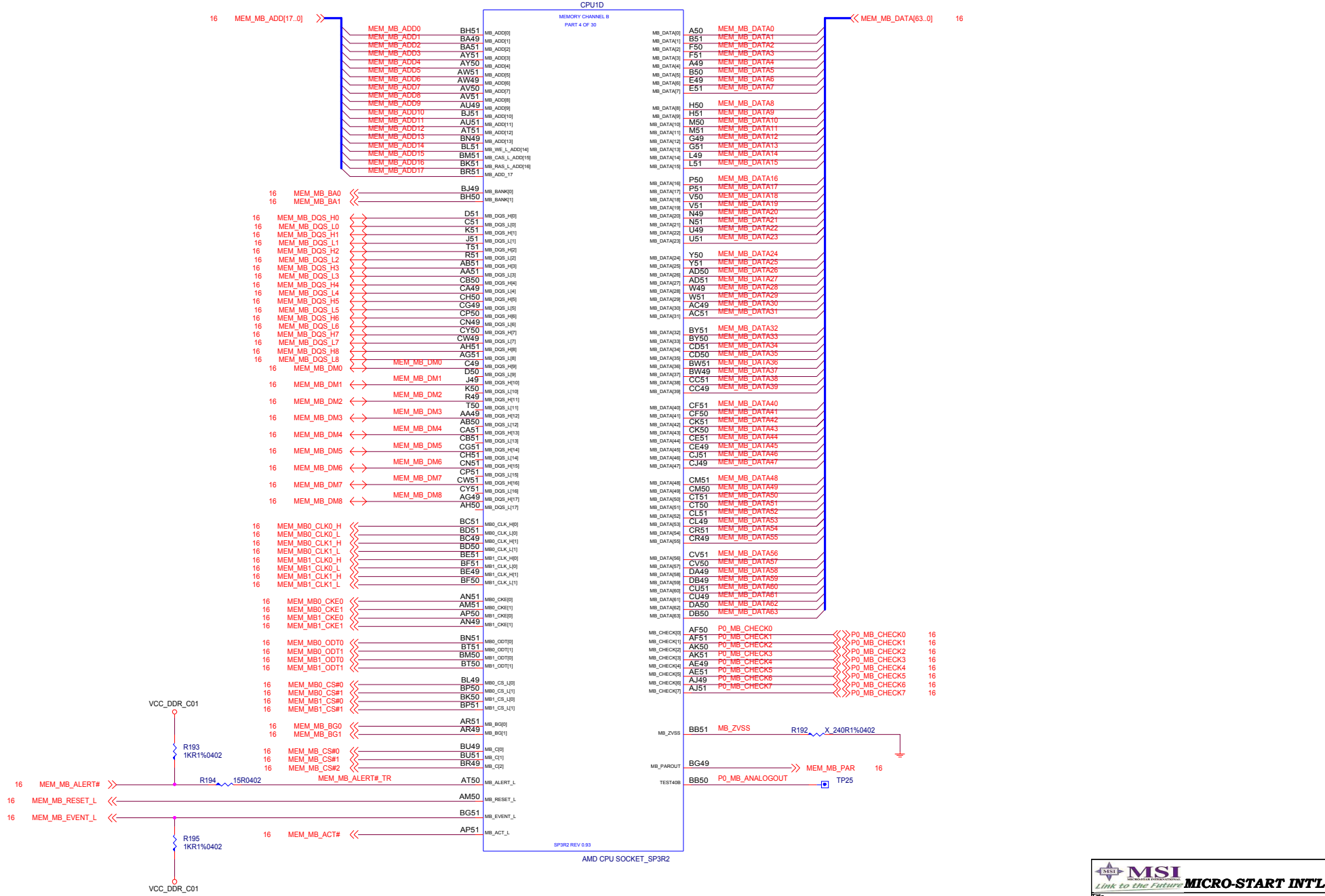

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Title	TR MEMORY B	
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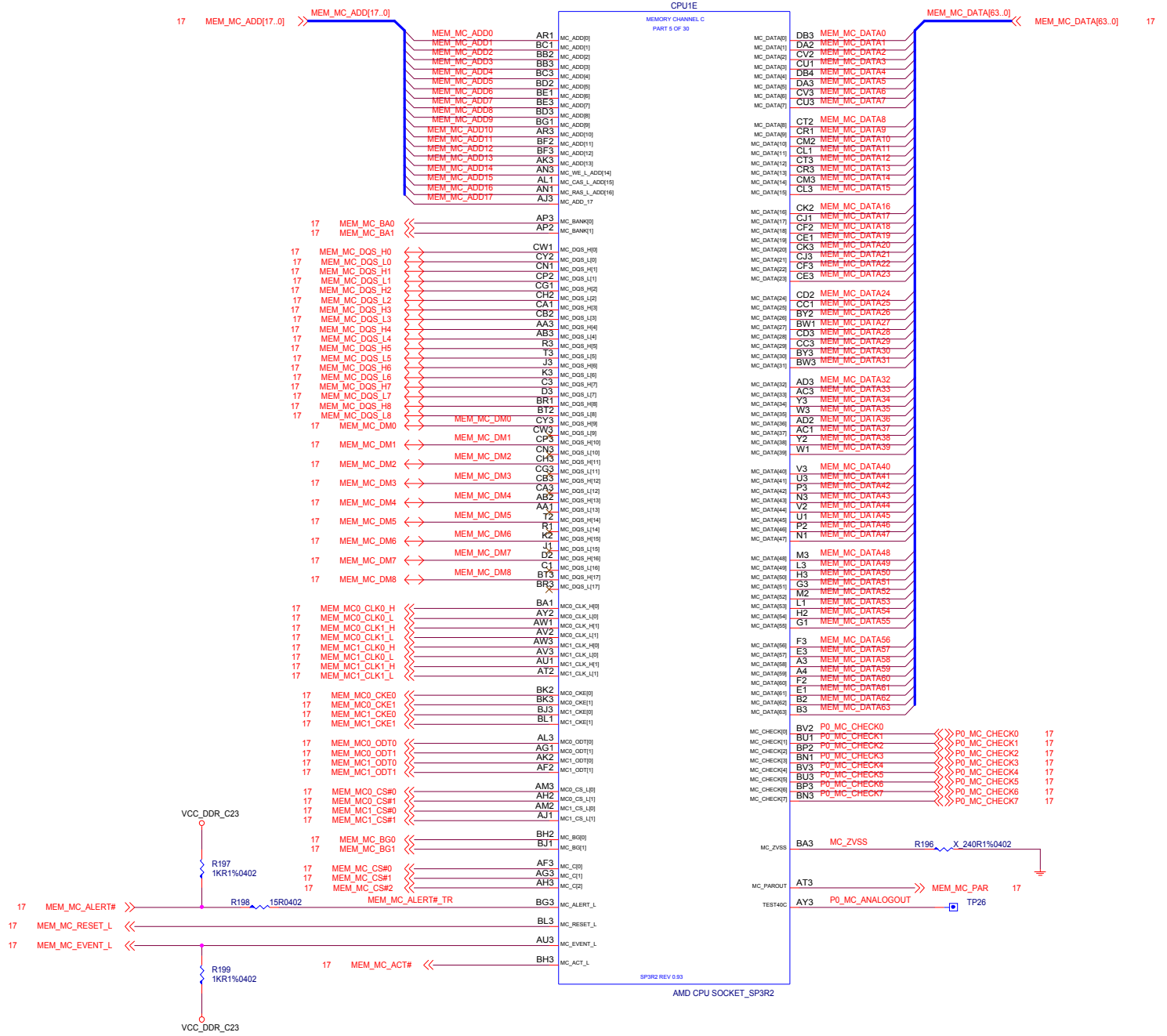

MICRO-START INT'L CO.,LTD.			
Title: TR MEMORY C			
Size	Document Number: MS-7B09..		Rev: 1.1
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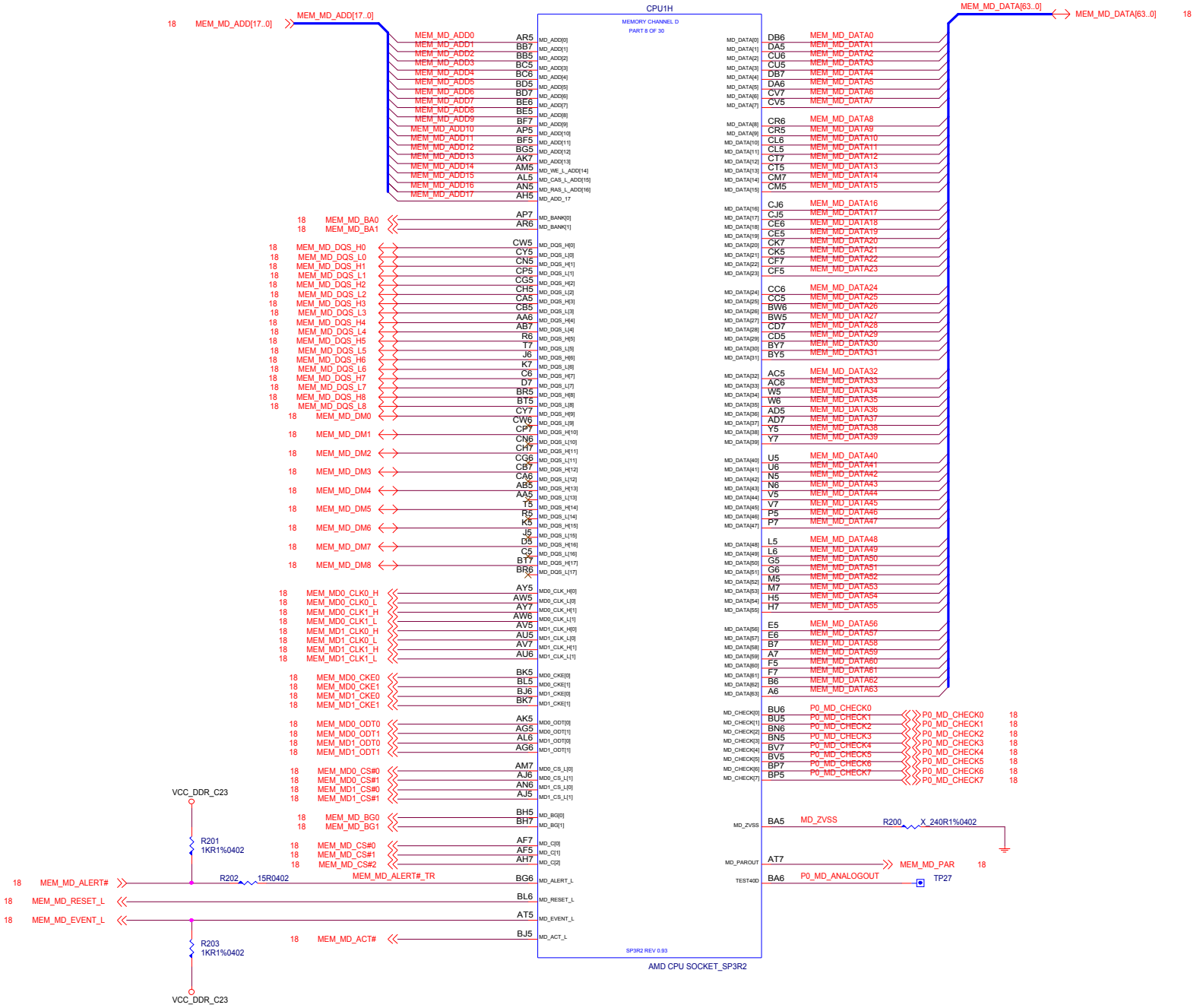

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Title: TR MEMORY D

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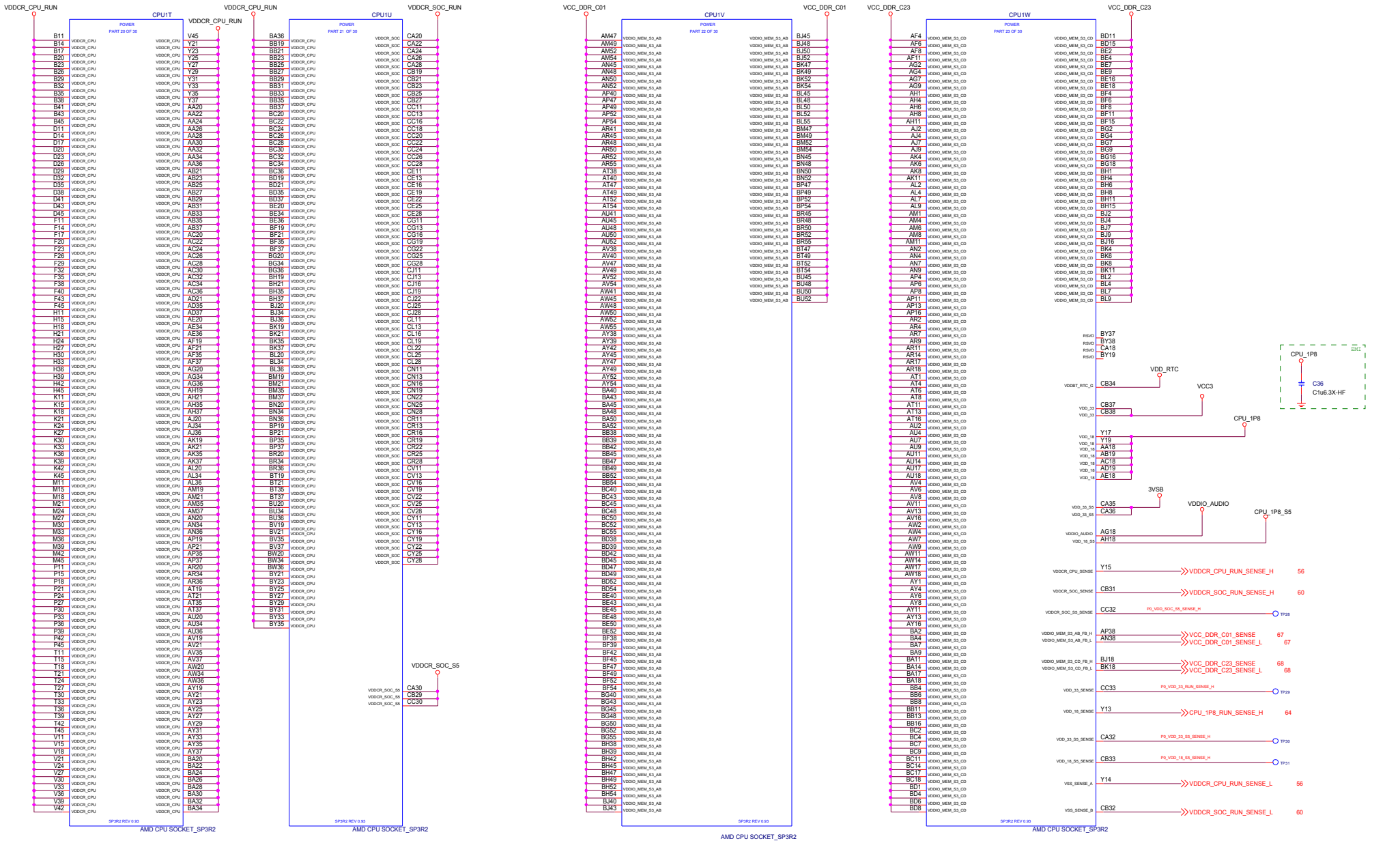
POWER



VDD: 180A(TDC)/240A(EDC);OC:200A(TDC)/264A(EDC)
VDDSOC: 60A(TDC)/80A(EDC)
VDDCR_SOC_S5: 2A(TDC/EDC)
VDDIO_MEM_AB: 15A(TDC/EDC)(CPU)+45A(TDC/EDC)(MEMORY)--EXCEPTED THIS INCLUDES OC
VDDIO_MEM_CD: 15A(TDC/EDC)(CPU)+45A(TDC/EDC)(MEMORY)--EXCEPTED THIS INCLUDES OC
VDD_1.8V: 3A(TDC)/3A(EDC)
VDD_1.8V_S5: 1A(TDC)/1A(EDC)

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Title	TR POWER	
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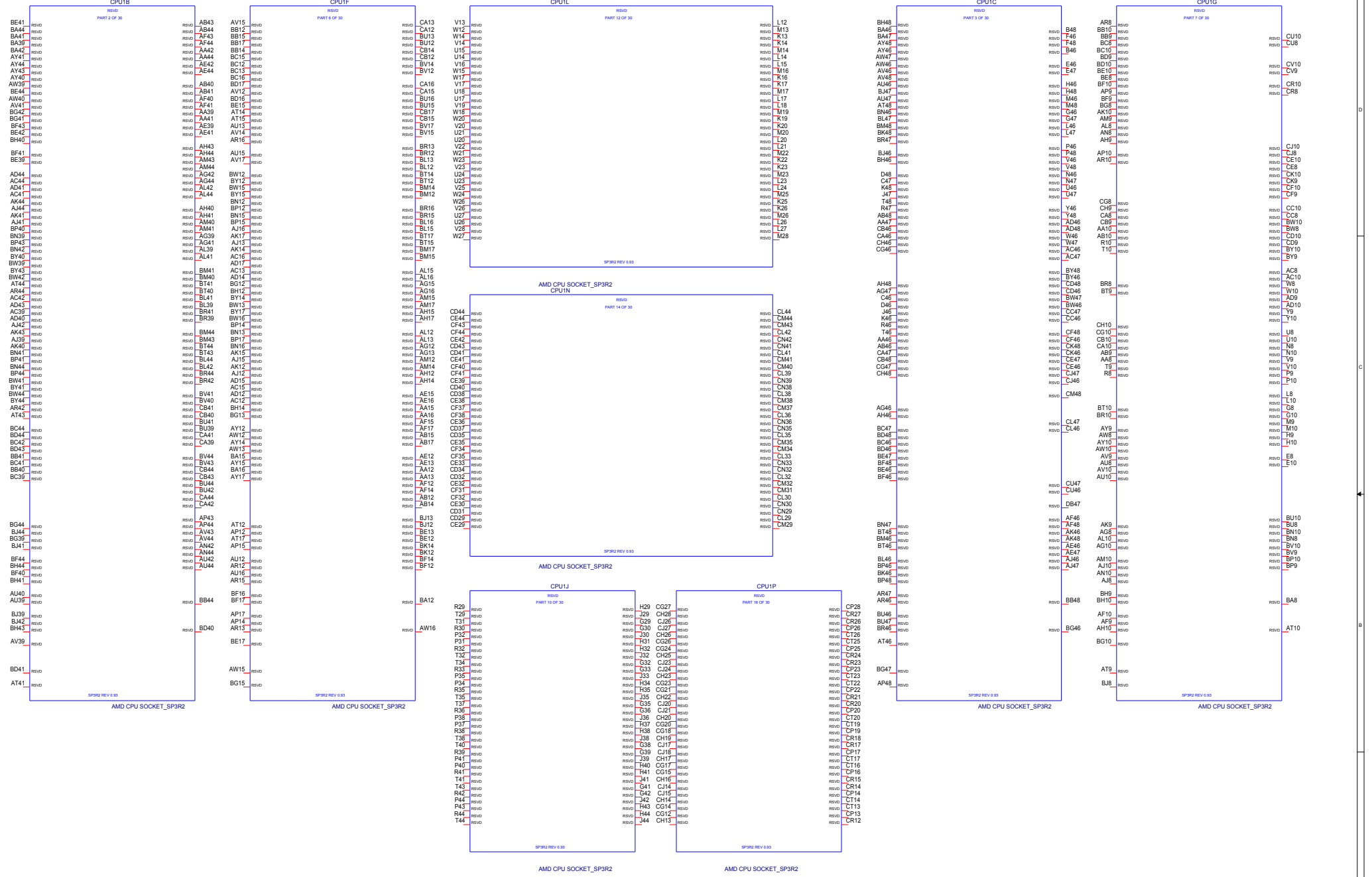

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Title

TR Reserved

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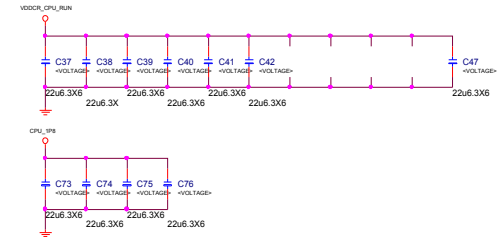
Decoupling Grouped by Placement Location

VDDCR_CPU Bottom Side Decoupling:

Top Side Decoupling:

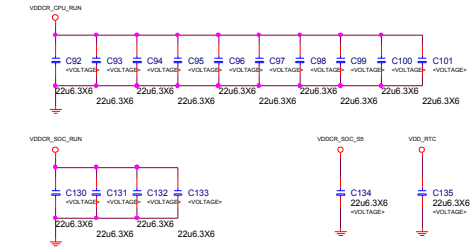
Bottom Side - Mirrored with Top Cavity - North

OEM Skt: 15; SLT Skt: 13



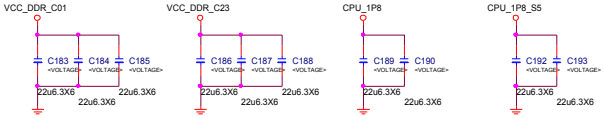
Bottom Side - Mirrored with Top Cavity - South

OEM Skt: 15; SLT Skt: 13



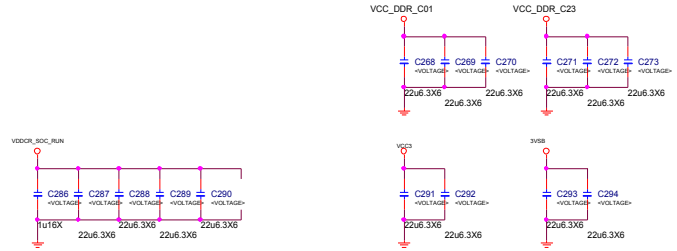
Bottom Side - North

OEM Skt: 24; SLT Skt: 24



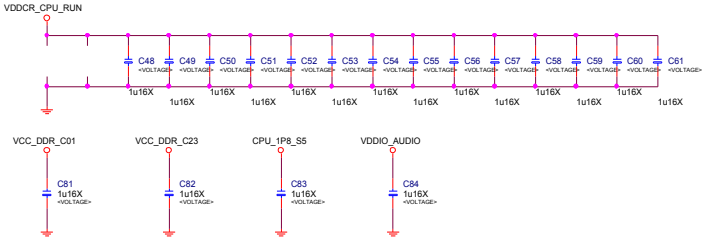
Bottom Side - South

OEM Skt: 24; SLT Skt: 24



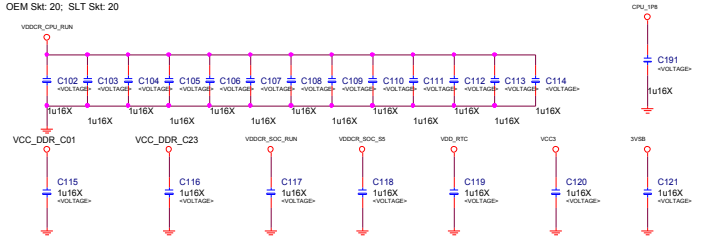
Bottom Side - North

OEM Skt: 20; SLT Skt: 20



Bottom Side - South

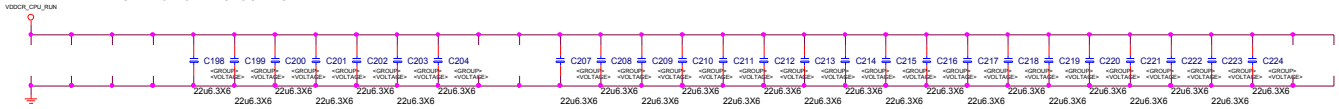
OEM Skt: 20; SLT Skt: 20



Bottom Side - In the socket split regions

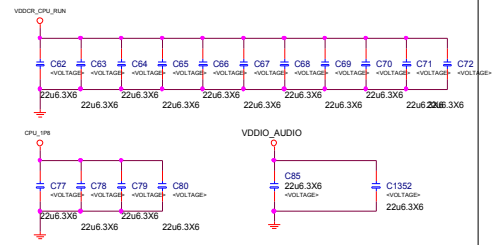
OEM SKT ONLY; NOT AVAILABLE IN SLT; CAN BE USED FOR RESISTORS

RSVD FOR OVER CLOCKING



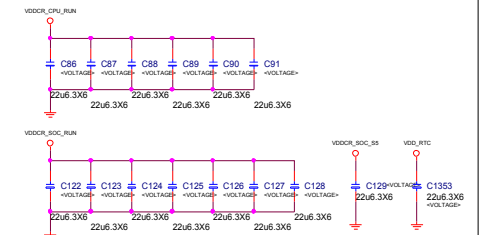
Top Cavity - North Decoupling

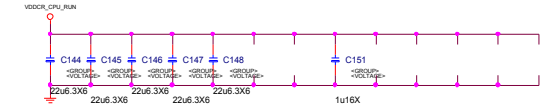
OEM Skt: 15; SLT Skt: 13



Top Cavity South Decoupling

OEM Skt: 15; SLT Skt: 13





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Title: TR GND			
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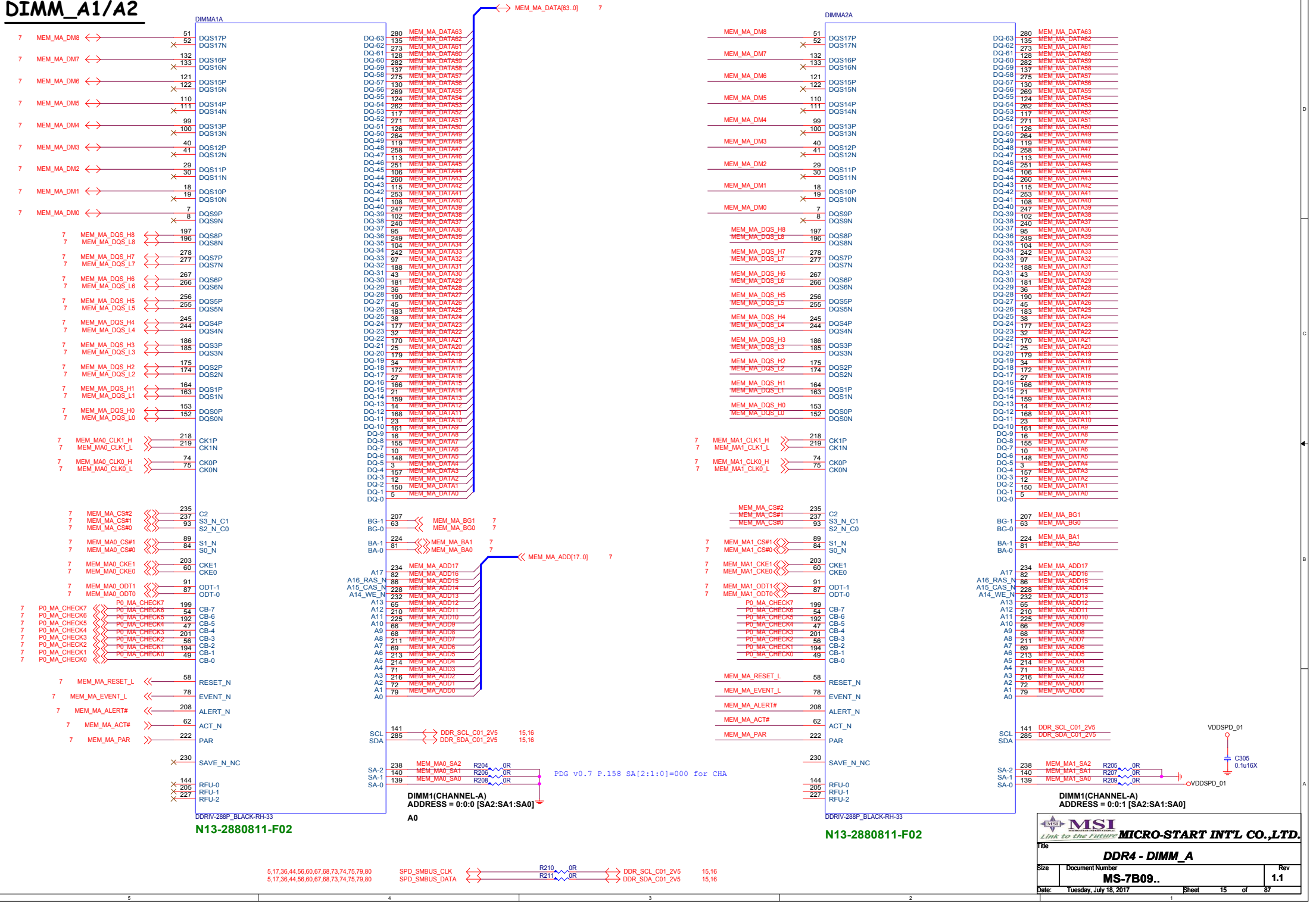
DIMM_A1/A2



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Title	DDR4 - DIMM_A	
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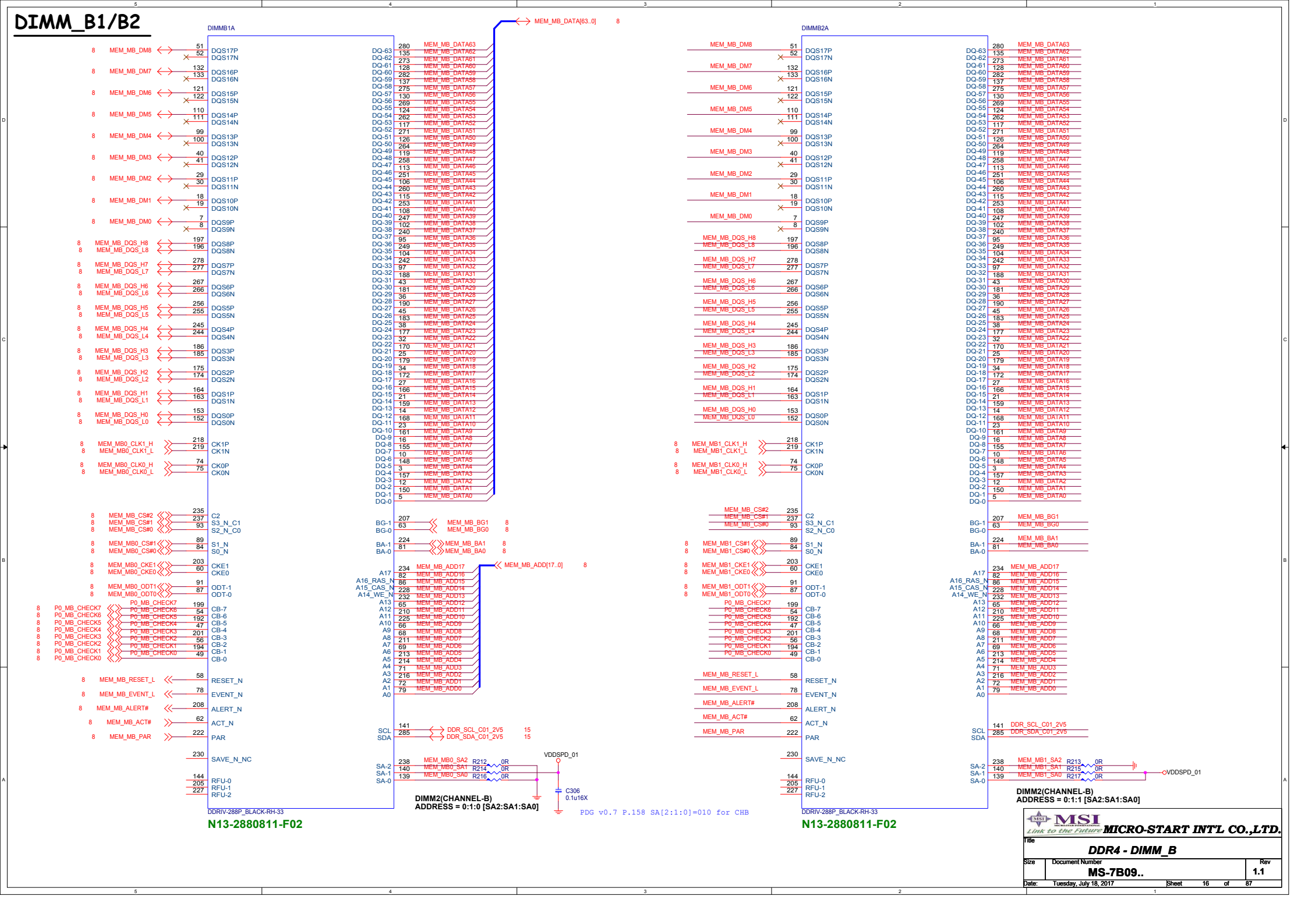
DIMM_B1/B2



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Title	DDR4 - DIMM_B	
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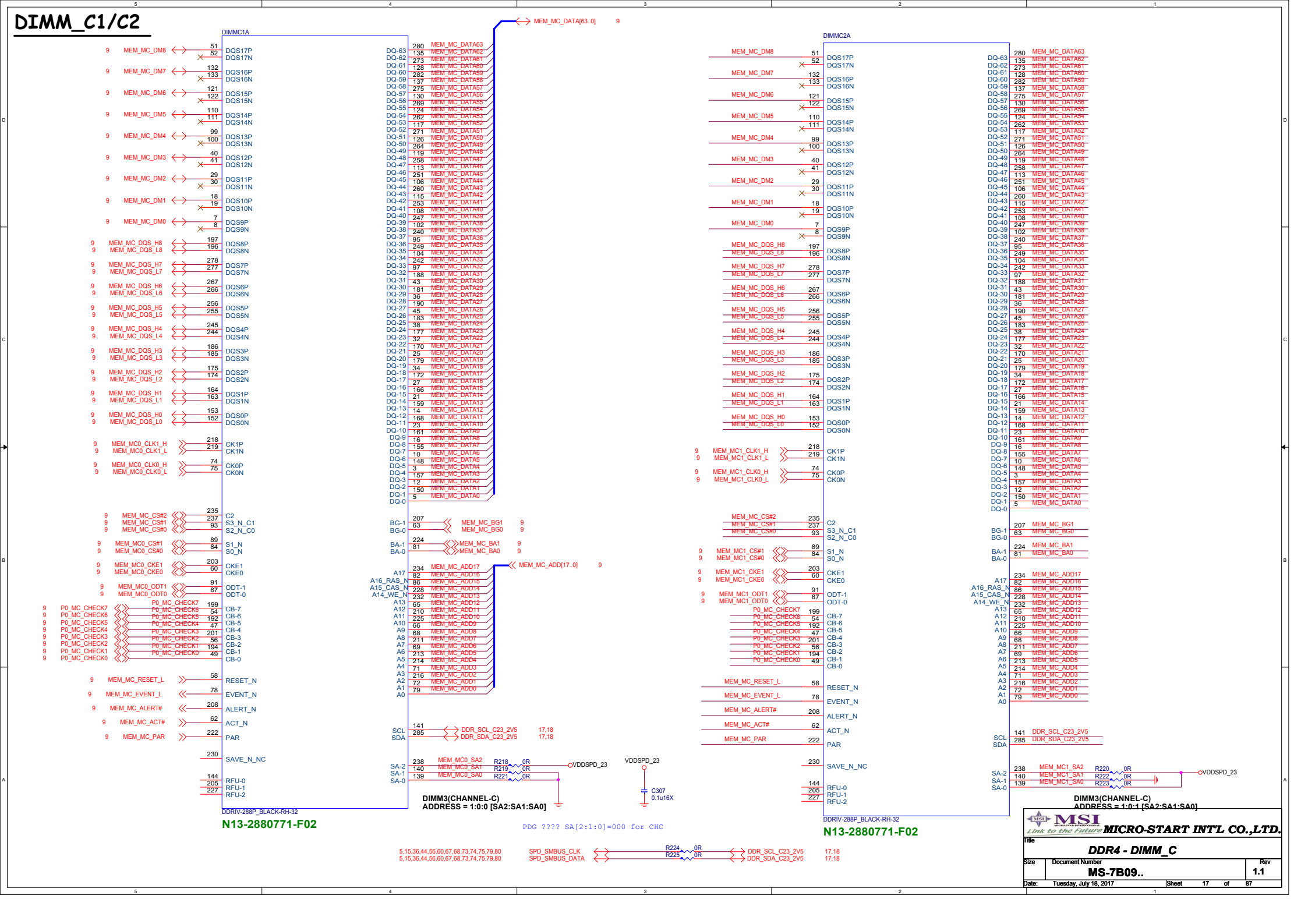
DIMM_C1/C2



Title	DDR4 - DIMM_C
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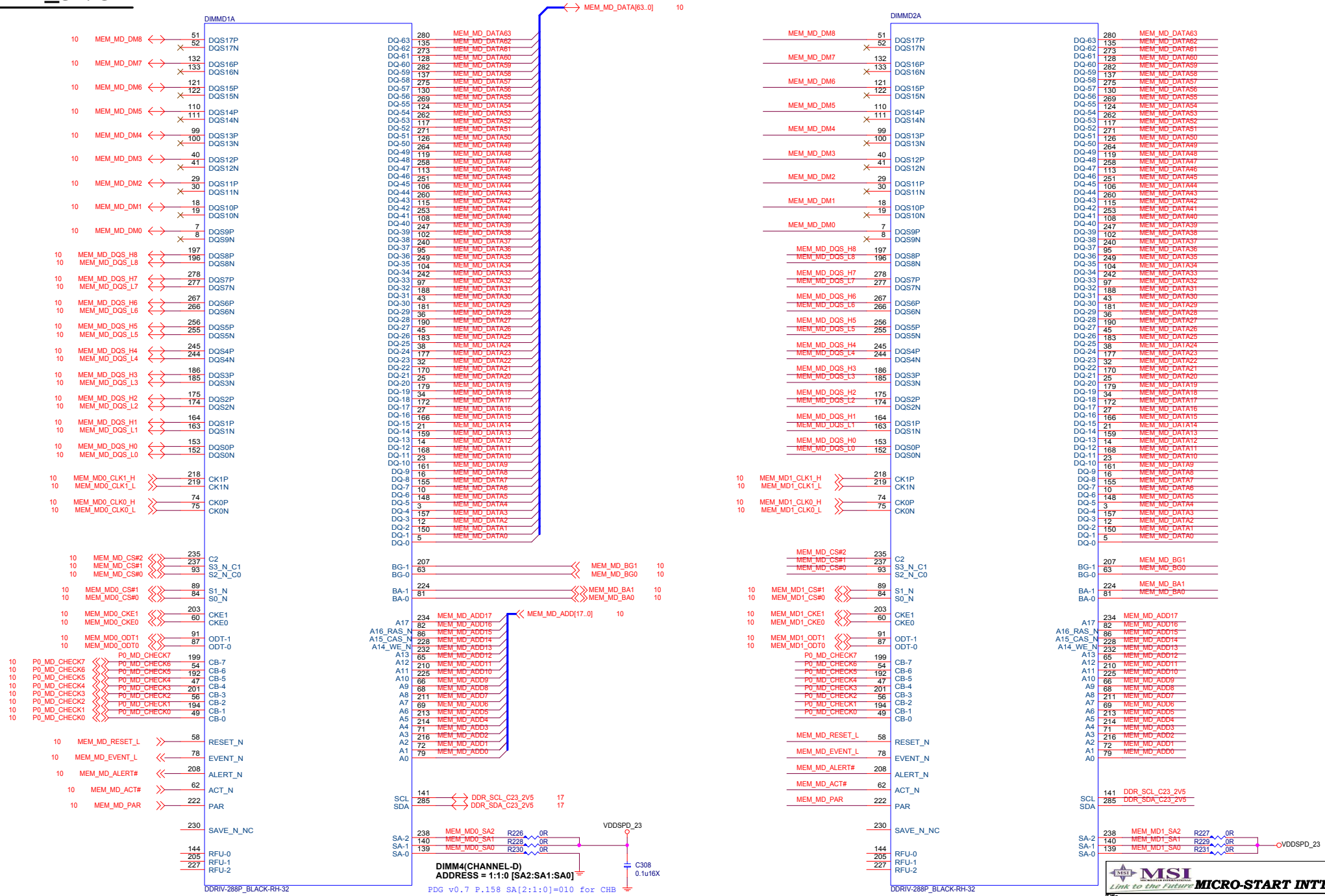
DIMM_D1/D2



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Title	DDR4 - DIMM_D	
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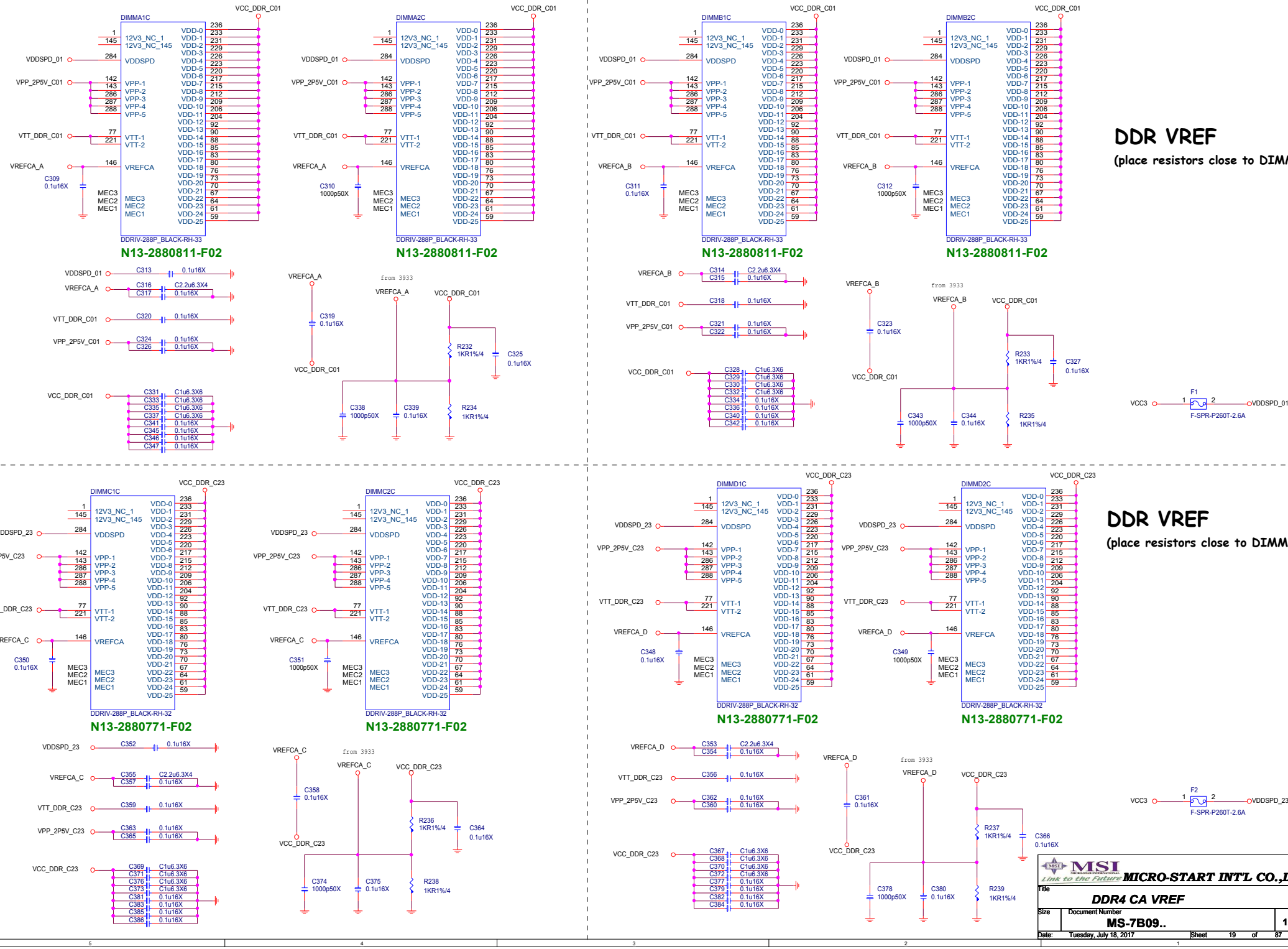
DIMMA1C
DIMMA2C
DIMMB1C
DIMMB2C
DDRIV-288P_BLACK-RH-33
N13-2880811-F02
VCC_DDR_C01
VDDSPD_01
VPP_2P5V_C01
VTT_DDR_C01
VREFCA_A
VREFCA_B
DDR VREF
(place resistors close to DIMMs)
DIMMC1C
DIMMC2C
DIMMD1C
DIMMD2C
DDRIV-288P_BLACK-RH-32
N13-2880771-F02
VCC_DDR_C23
VDDSPD_23
VPP_2P5V_C23
VTT_DDR_C23
VREFCA_C
VREFCA_D
DDR VREF
(place resistors close to DIMMs)
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DDR4 CA VREF
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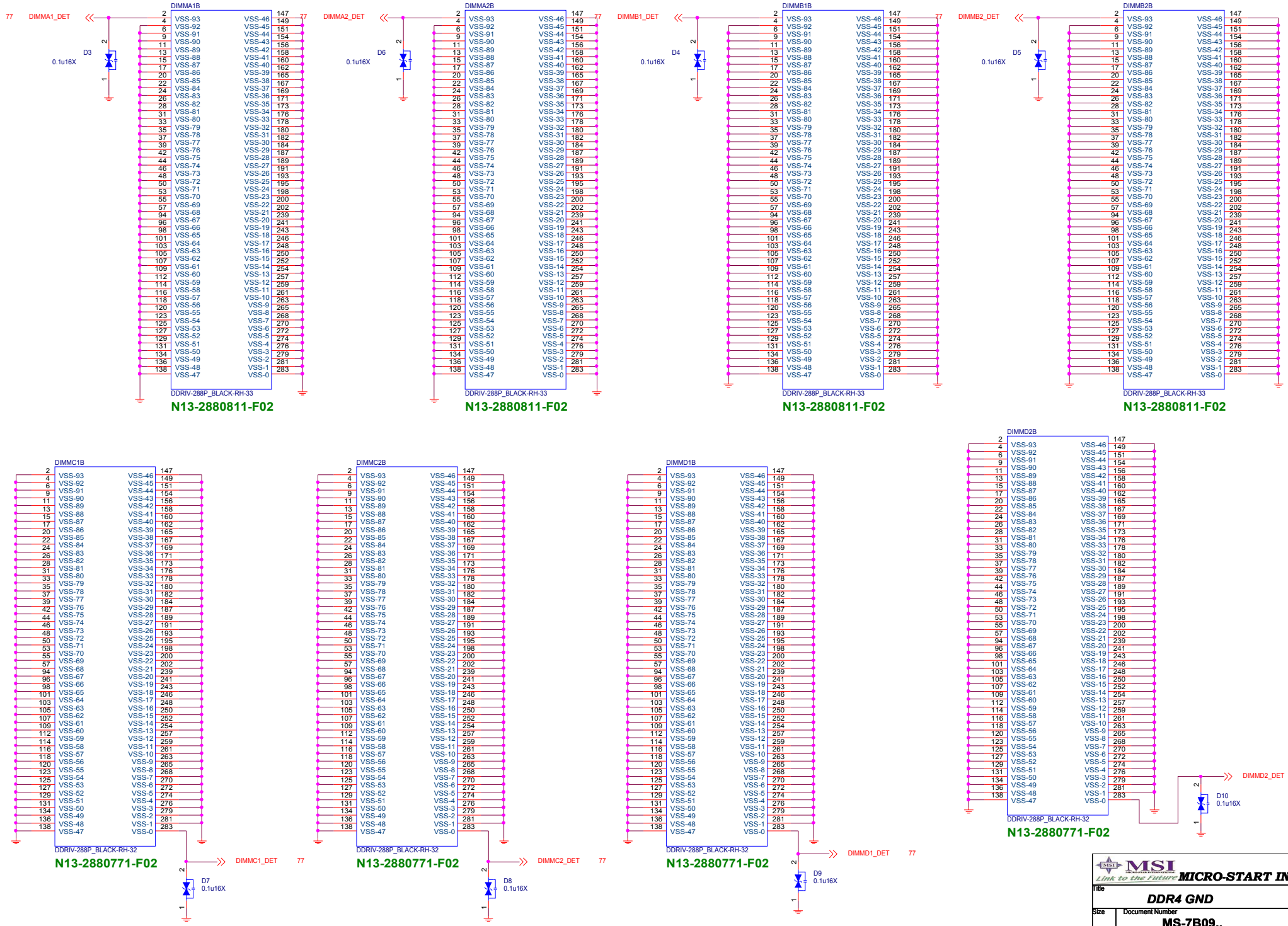

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Title	DDR4 GND	
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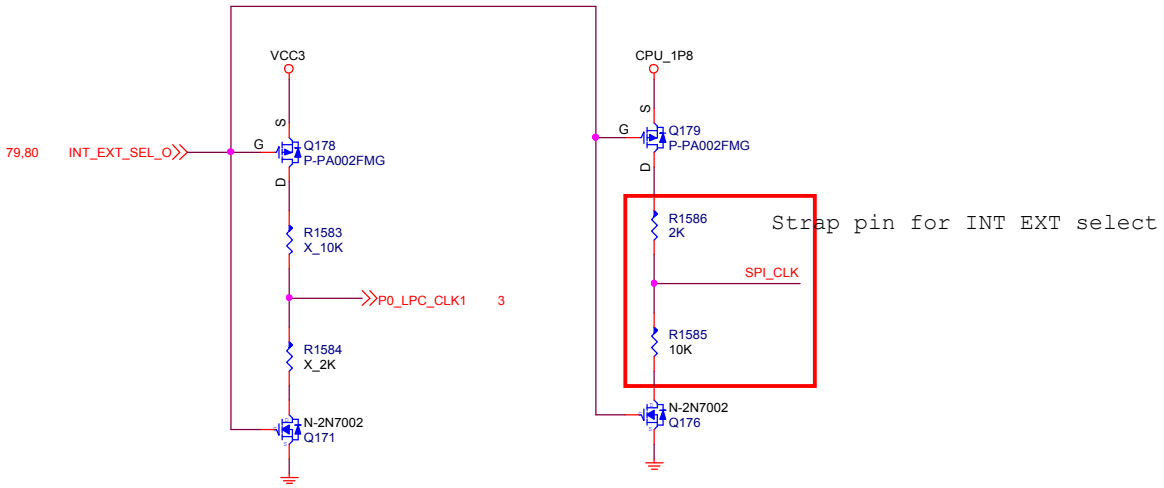
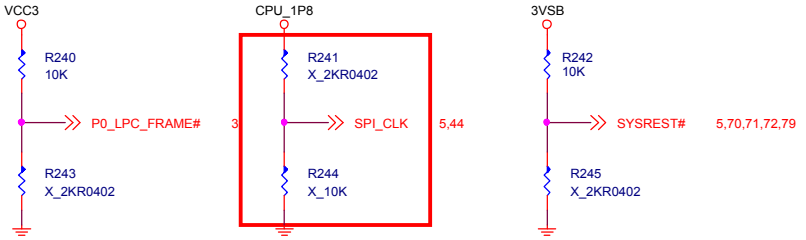


CPU STRAPS

STRAP	DEFINITION
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE
LPC_FRAME_L	ROM TYPE SELECT 1:BOOT FROM SPI ROM(DEFAULT) 0:BOOT FROM LPC ROM



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Title: CPU STRAPS		
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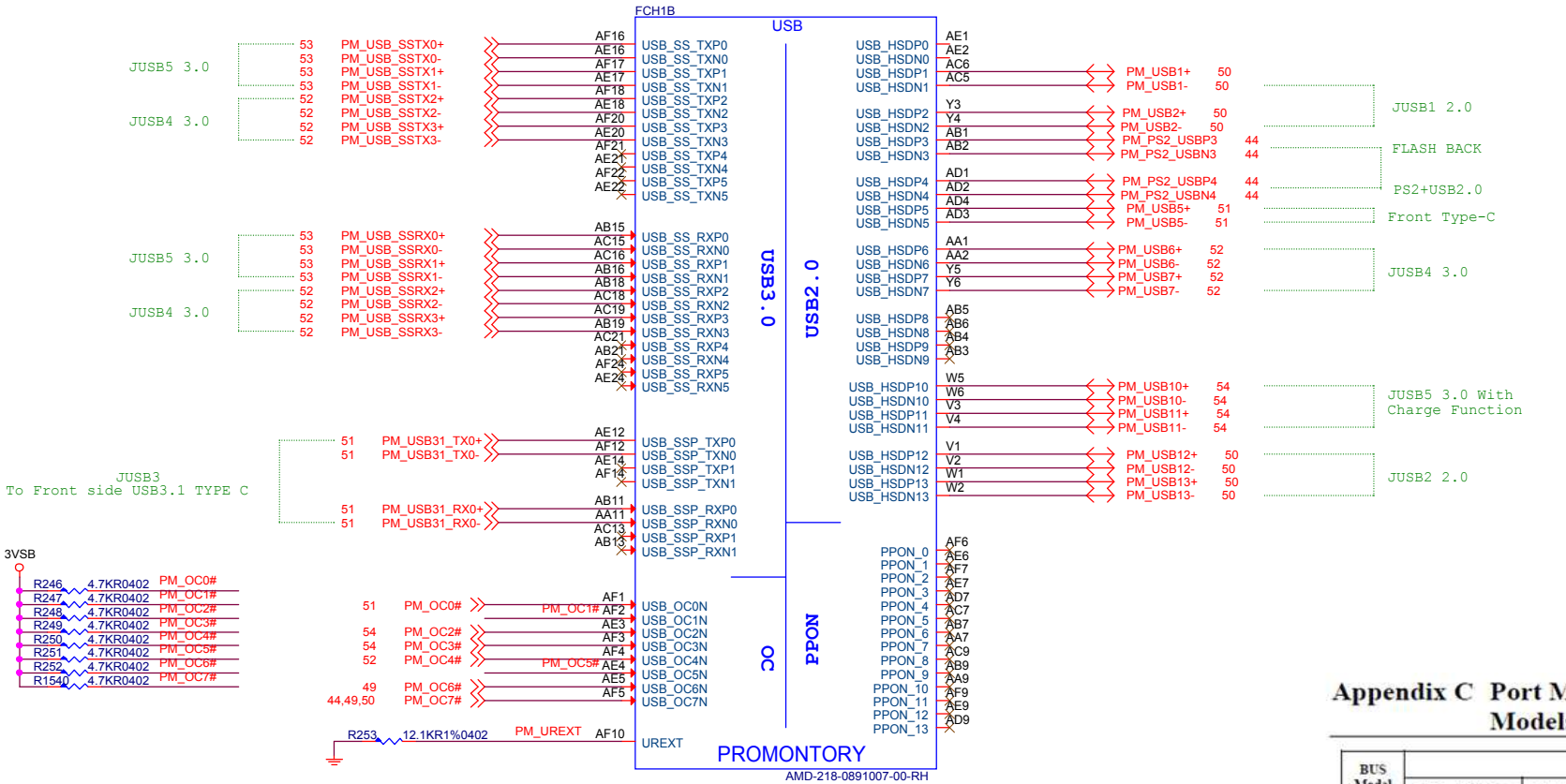

Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

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Title: **Promontory USB**

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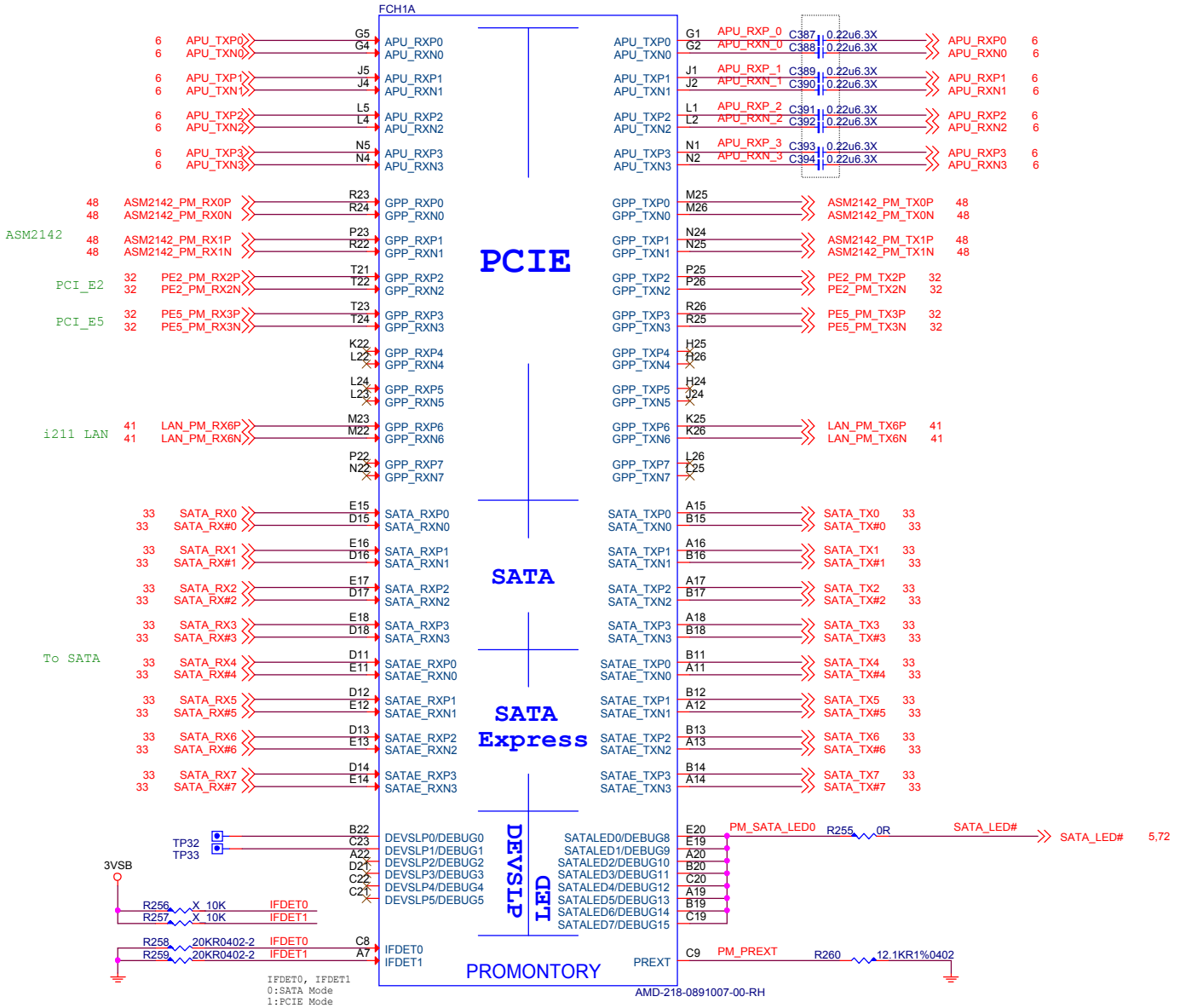

SATA port	DEVSLP signal
SATA_TX/RXP/N[0]	DEVSLP0
SATA_TX/RXP/N[1]	DEVSLP1
SATA_TX/RXP/N[2]	DEVSLP2
SATA_TX/RXP/N[3]	DEVSLP3
SATAE_TX/RXP/N[0]	SATAE_CLKREQ0N
SATAE_TX/RXP/N[1]	DEVSLP4
SATAE_TX/RXP/N[2]	SATAE_CLKREQ1N
SATAE_TX/RXP/N[3]	DEVSLP5

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Title	Promontory PCIE/SATA	
Size	Document Number MS-7B09..	Rev 1.1
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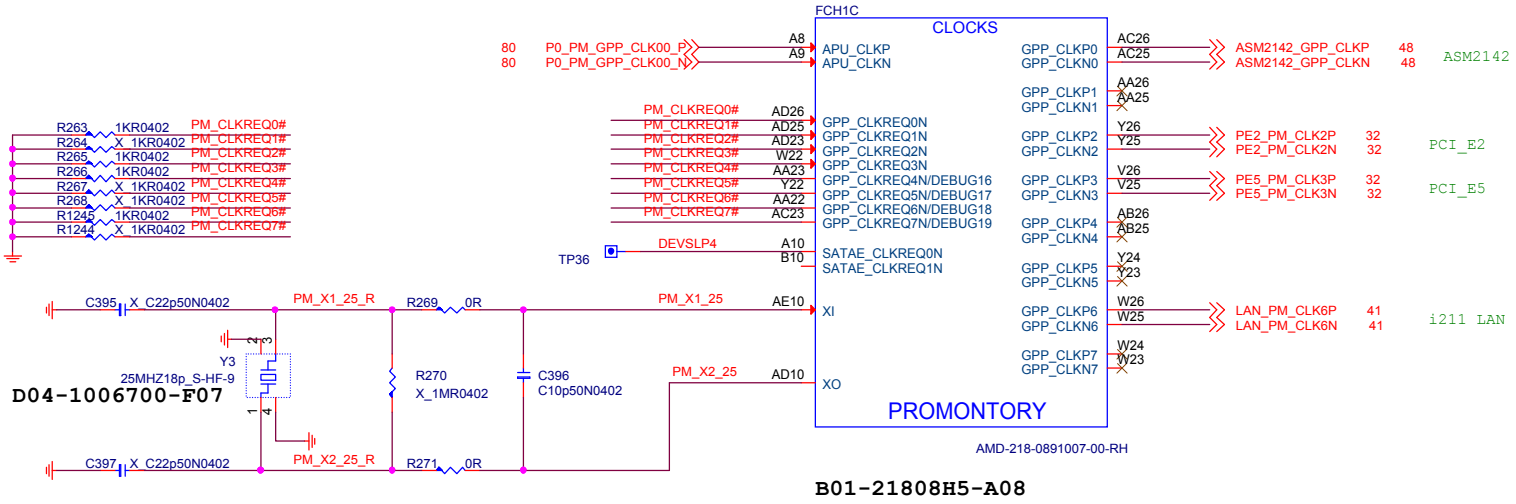

Title	Promontory CLOCK
Size	
Document Number	MS-7B09..
Rev	1.1
Date:	Tuesday, July 18, 2017
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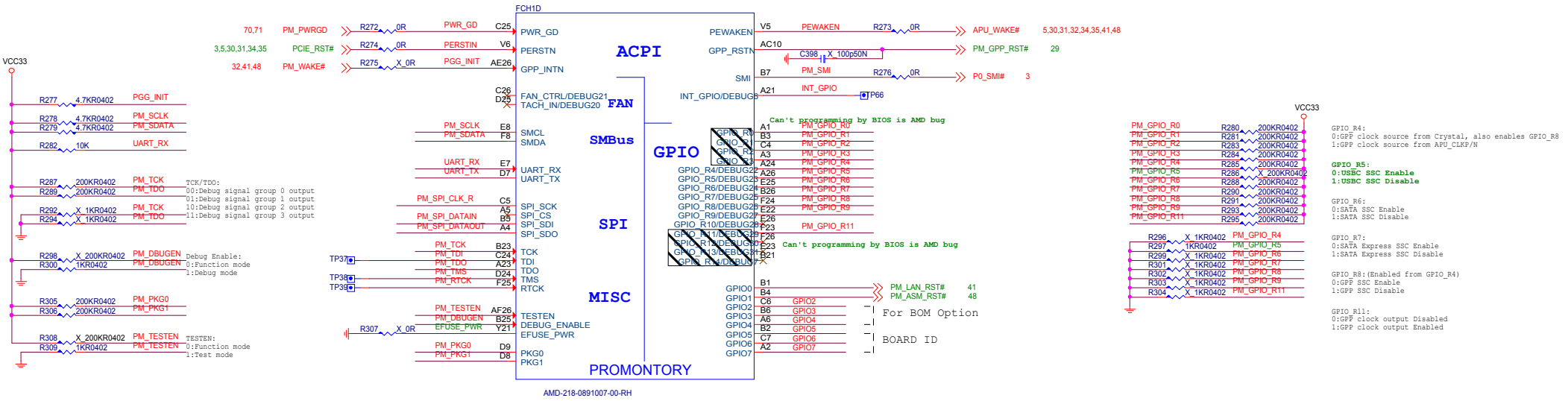
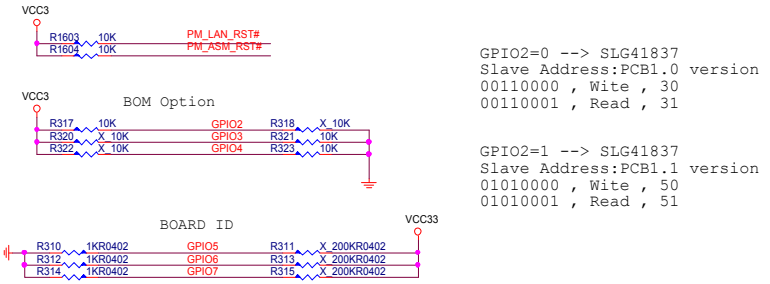
MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future





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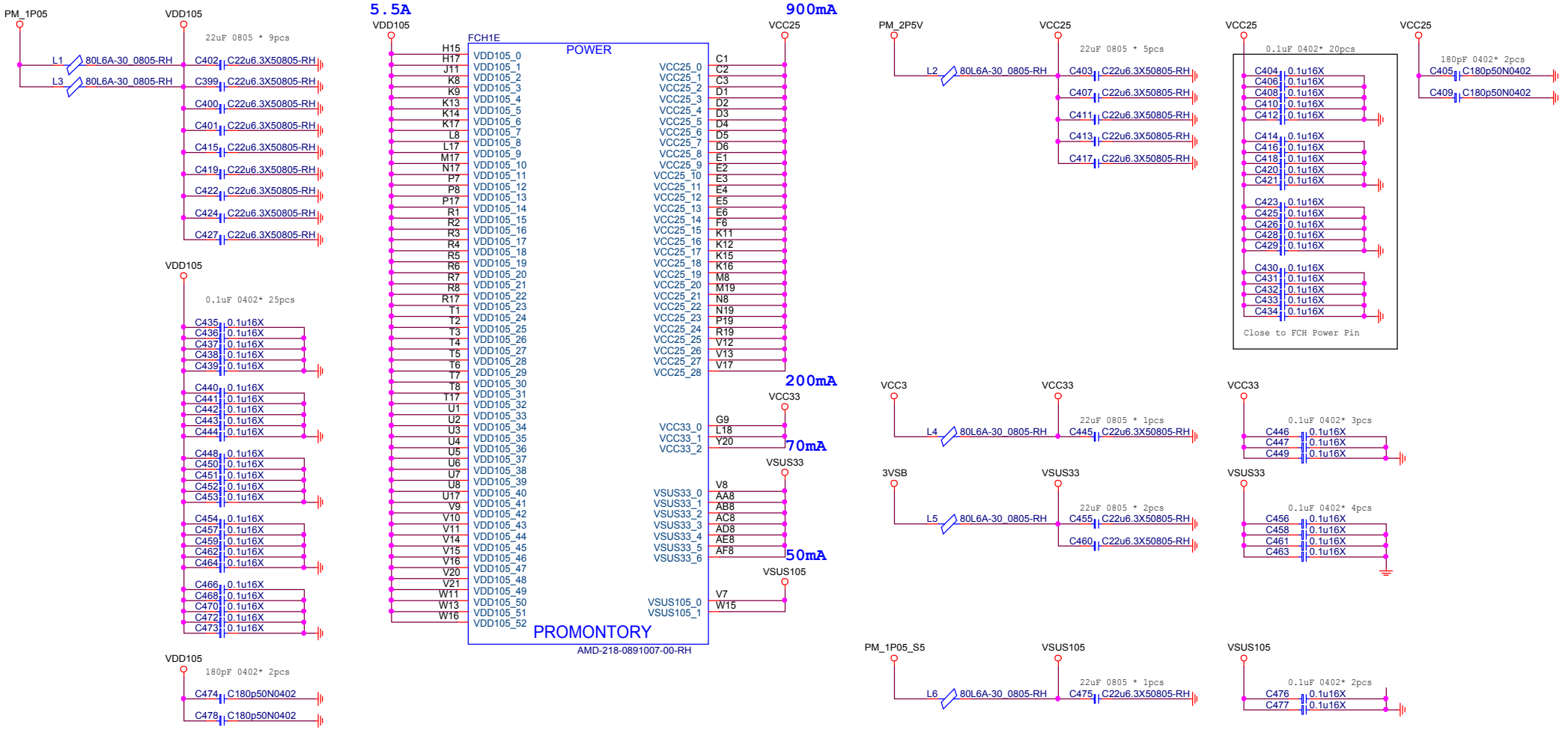
Link to the Future

Title	Promontory GPIO/SMB/SPI	
Size	Document Number: MS-7B09..	Rev: 1.1
Date: Tuesday, July 18, 2017	Sheet 25 of 87	

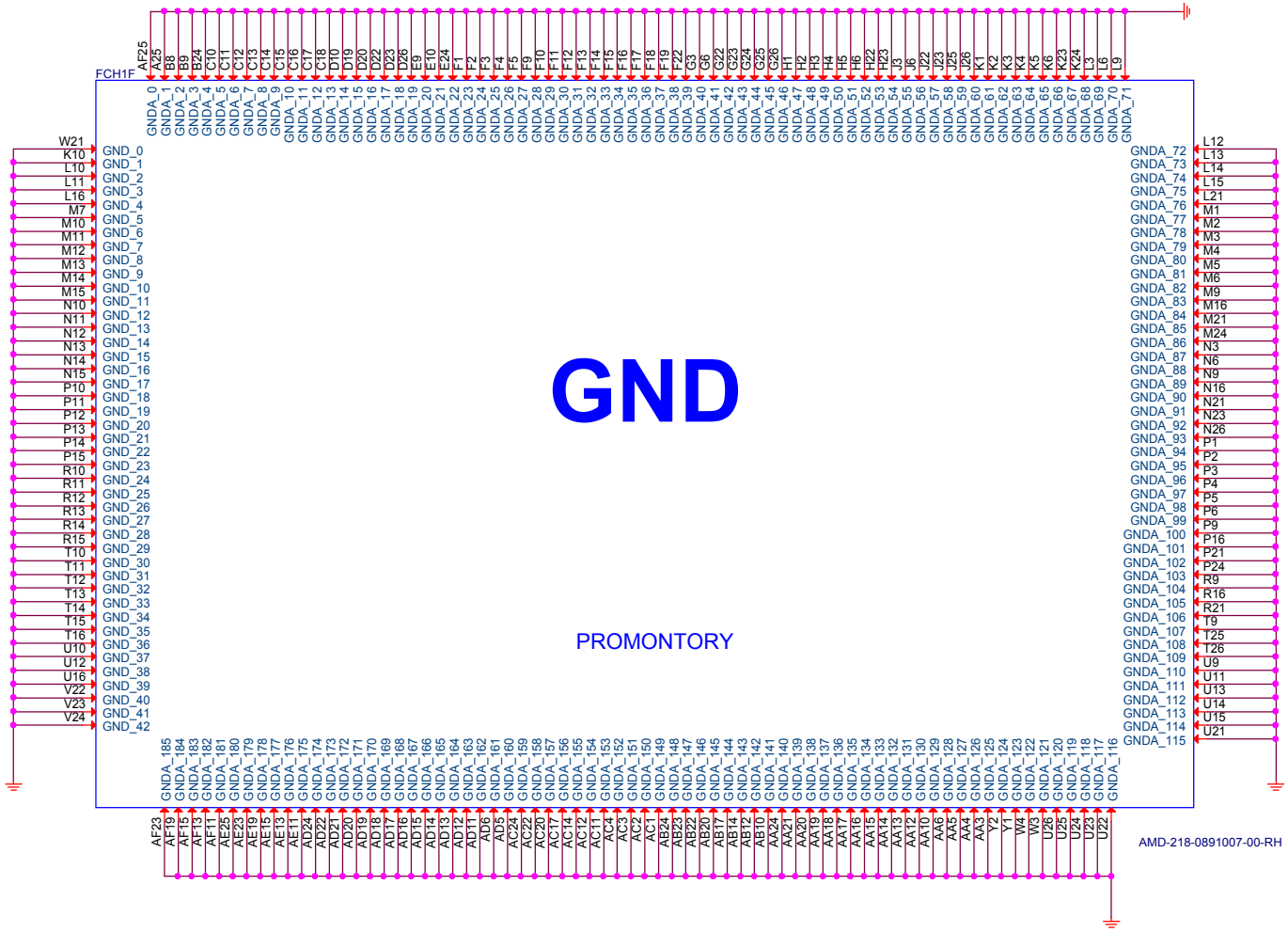


MICRO-START INT'L CO.,LTD.

Title: Promontory POWER

Size	Document Number	Rev
	MS-7B09..	1.1

Date: Tuesday, July 18, 2017 Sheet 26 of 87



MSI MICRO-STAR INTERNATIONAL Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Promontory GND		
Size	Document Number MS-7B09..		Rev 1.1
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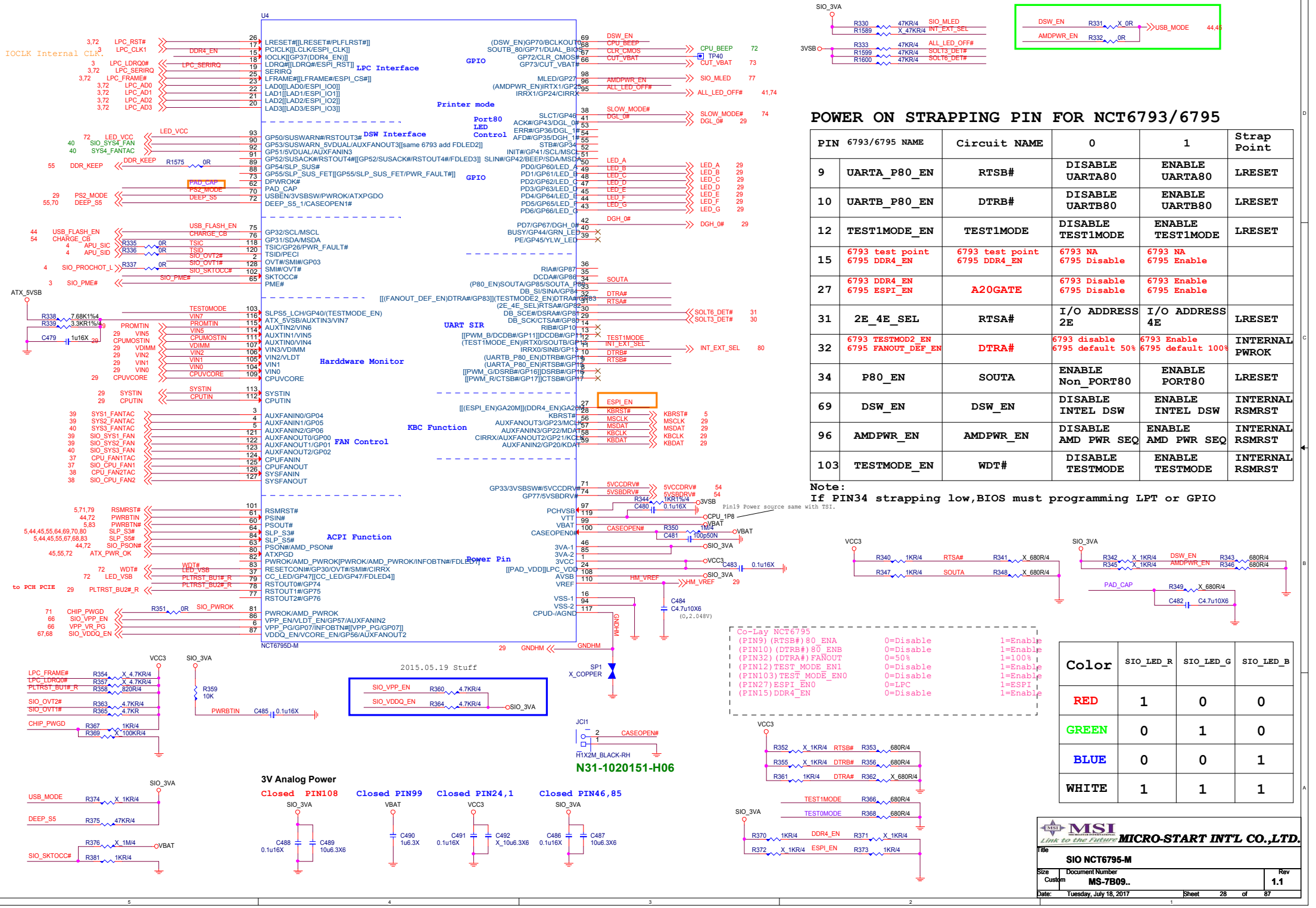

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Co-Lay NCT6795

(PIN9)(RTSB#)80_ENA	0=Disable	1=Enable
(PIN10)(DTRB#)80_ENB	0=Disable	1=Enable
(PIN32)(DTRA#)FANOUT	0=50%	1=100%
(PIN12)TEST_MODE_EN1	0=Disable	1=Enable
(PIN103)TEST_MODE_EN0	0=Disable	1=Enable
(PIN27)ESPI_EN0	0=LPC	1=ESPI
(PIN15)DDR4_EN	0=Disable	1=Enable

Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

MICRO-START INT'L CO.,LTD.

Title	SIO NCT6795-M	
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HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

VDDCR_CPU_RUN — R386 10K/1% — CPUVCORE 28

VCORE: R388 X_10KR1%/4, C494 10u6.3X6

+12V — R384 220K/1%/4 — VIN0 — VIN0 28

R389 20KR1%/4, C495 0.1u16X

VCC5 — R387 12K/1%/4 — VIN1 — VIN1 28

R390 3K/1%/4, C496 0.1u16X

Power Fault detect through VIN0,VIN1

VDDCR_SOC_RUN — R395 10K/1% — VIN2 — VIN2 28

VDDCR_SOC: R398 X_10KR1%/4, C501 10u6.3X6

VCC_DDR_C01 — R396 10K/1% — VDIMM — VDIMM 28

R399 10K/1%, C503 10u6.3X6

VCC_DDR_C23 — R397 10K/1% — VIN5 — VIN5 28

R1241 10K/1%, C502 10u6.3X6

TEMP SENSOR

For CPU — HM_VREF — HM_VREF 28,29

R402 10K/1%

CPUTIN — CPUTIN 28

RT1 10KRT1%0402, C510 C2200p50X

GNDHM — GNDHM 28

For System

Q3 P-3906 (E, B, C)

SYSTIN — SYSTIN 28

C509 C2200p50X

GNDHM

For CPU — HM_VREF — HM_VREF 28,29

R403 10K/1% — 2016/05/24 Add

CPUMOSTIN — CPUMOSTIN 28

RT2 10KRT1%0402, C511 C2200p50X

GNDHM

Close to CPU MOS

For PROM — HM_VREF — HM_VREF 28,29

R404 10K/1% — 2016/11/03 Add

PROMTIN — PROMTIN 28

RT3 10KRT1%0402, C512 C2200p50X

GNDHM

Place to under Promontory

DEBUG LED

Placement (Placement): POST4 POST3 POST2 POST1

28 LED_A … LED_G

Placement 要

(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

Debug LED OFF BIOS control

RN2 8P4R-220R0402

LED_C — H0_LED_C

LED_A — H0_LED_A

LED_B — H0_LED_B

LED_G — H0_LED_G

LED_D — H0_LED_D

LED_E — H0_LED_E

LED_F — H0_LED_F

RN3 8P4R-220R0402

POST1 (a b c d e f g) DIGH# DIGL#

LED06-R-7SEGX2-RH-2

H0_LED_A … H0_LED_G

L_DGH_0# L_DGL_0#

D0C-0603001-L05

SIO_3VA — R415 X_10K — DGH_0# — R417 0R — L_DGH_0#

28 DGH_0#

SIO_3VA — R414 X_10K — DGL_0# — R416 0R — L_DGL_0#

28 DGL_0#

COM PORT

PS2_VCC

PS2 Connect

RN1 8P4R-4.7K

C493 0.1u16X

R385 X_1KR/4

28 KBDAT

28 MSDAT

28 KBCLK

28 MSCLK

R391 33R/4 KBD

R392 33R/4 MSD

R393 33R/4 KBC

R394 33R/4 MSC

PS2_USB1A

C497 C180P50N

C498 C180P50N

C499 C180P50N

C500 C180P50N

MINIDIN_USBX2-RH-1

N58-14M0241-H06

Main:D0G-05A0529-A68

AVL:D0G-45B0510-I14

28

D11

MSC 6 — 4 KBC

MSD 1 — 3 KBD

ESD-AOZ8906C

VCC5 — ATX_5VSB

1u6.3X C504, C505 1u6.3X

44 5VDRV2_EN

45 5VDRV2 — R400 200KR1%/4 — 5VDRV2_EN

R401 56KR1%0402

28 PS2_MODE

R405 10K/1%

U5 UP7550PMA8_SOT23-8

S3# OC# EN GND 5VCC 5VSB VOUT1 VOUT2

C506 22u6.3X6, C507 X_0.1u16X, C508 0.1u16X

PS2_VCC

RESET

28 PLTRST_BU2#_R — PLTRST_BU2#_R — R408 X_22R1%/4 — PLTRST_BU2#

R406 100R1%4 PLTRST_BU2#_PCIE2 32

R407 100R1%4 PLTRST_BU2#_PCIE5 32

R409 100R1%4 PLTRST_BU2#_LAN 41

R410 100R1%4 PLTRST_BU2#_ASM1142 48

25 PM_GPP_RST# — PM_GPP_RST# — R411 0R — PLTRST_BU2#

Co-lay FCH Reset for meet FCH sequence. See 55553.

SIO_3VA

ATX_5VSB

C513 1u6.3X

U6 GS7116S5 VDD VOUT EN GND ADJ

EN:VIH1.6V

C514 0.1u16X

R412 10K/1%

C515 10u6.3X6

3VA_FB

R413 3.16K/1%

SIO_3VA

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Title	HWM/PS2/Debug LED	
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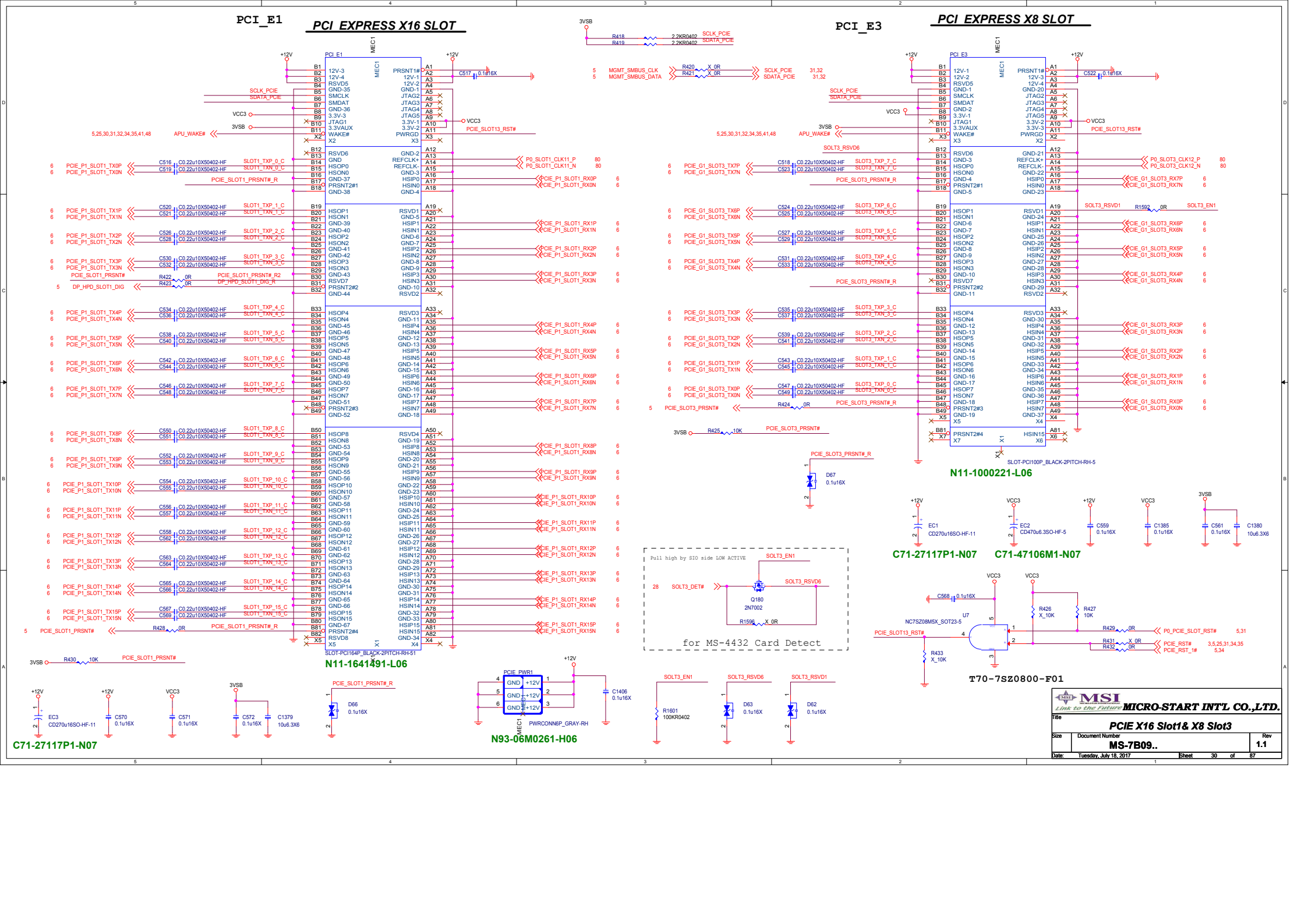
PCI_E1

PCI EXPRESS X16 SLOT

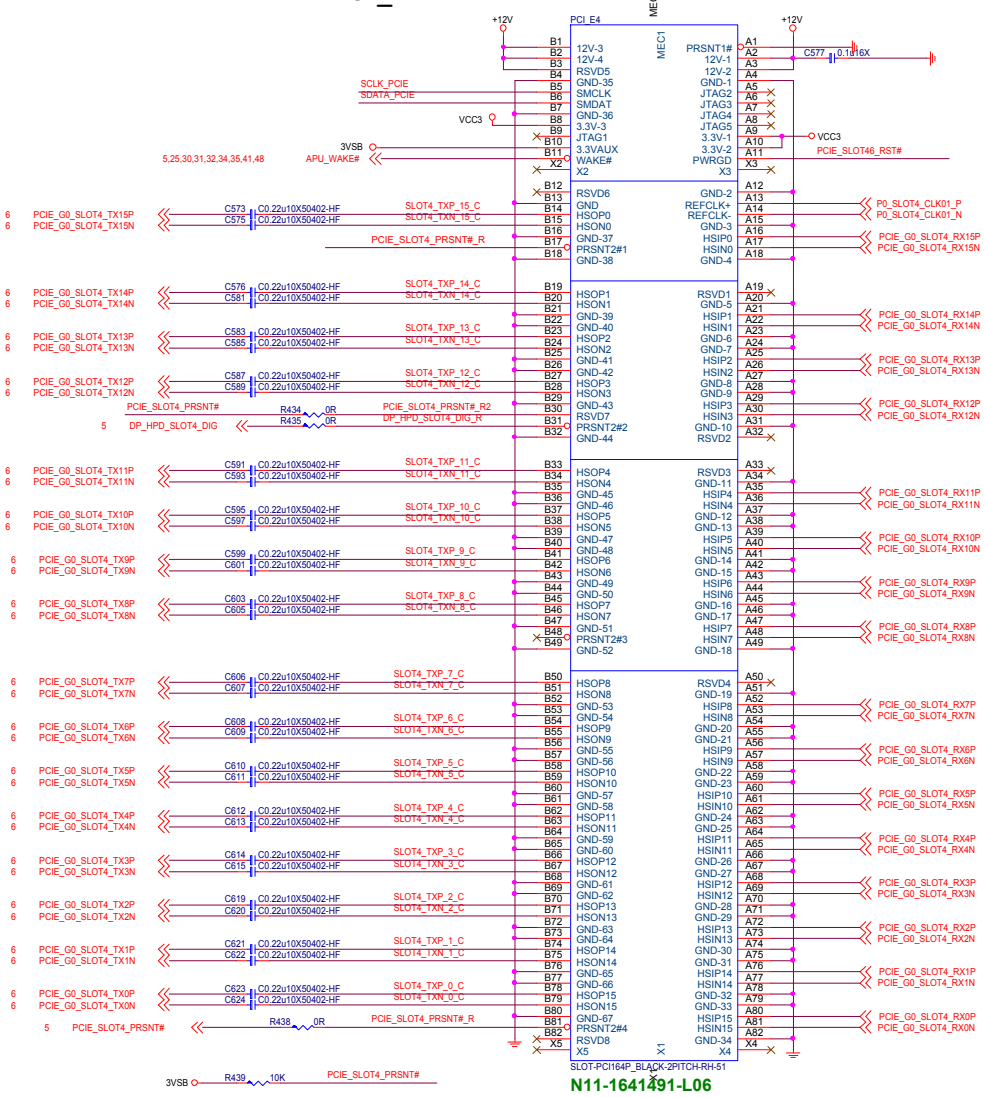
PCI_E3

PCI EXPRESS X8 SLOT



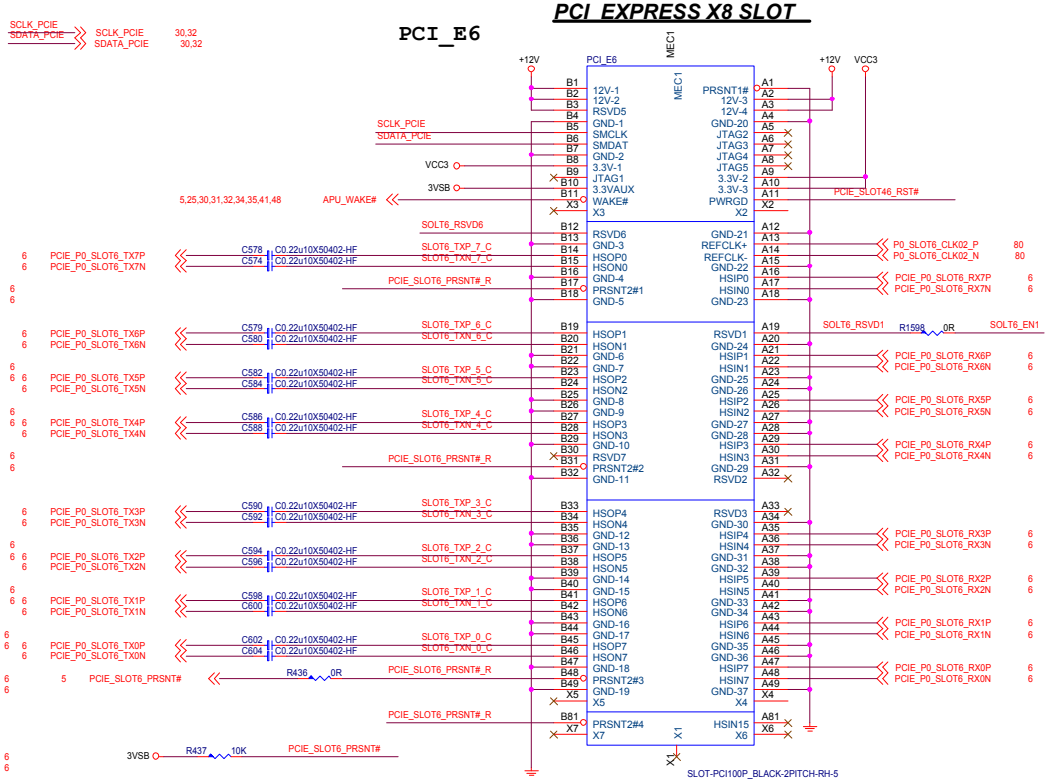
PCI EXPRESS X16 SLOT

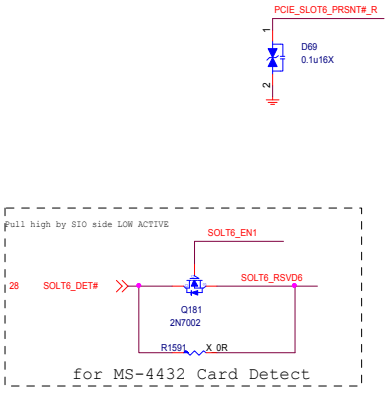
PCI_E4

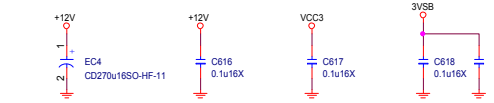


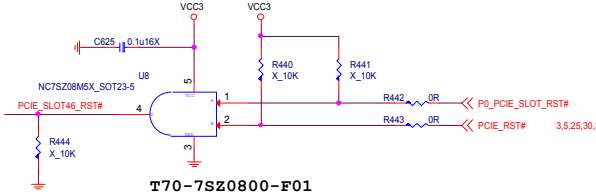
PCI EXPRESS X8 SLOT

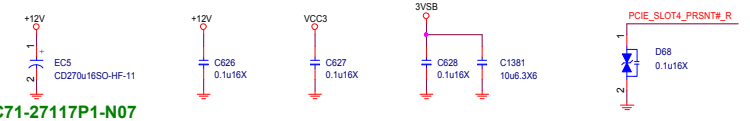
PCI_E6

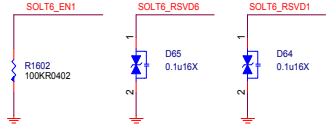












MSI	MICRO-START INT'L CO.,LTD.		
Title	PCIE X16 Slot4 & X8 Slot6		
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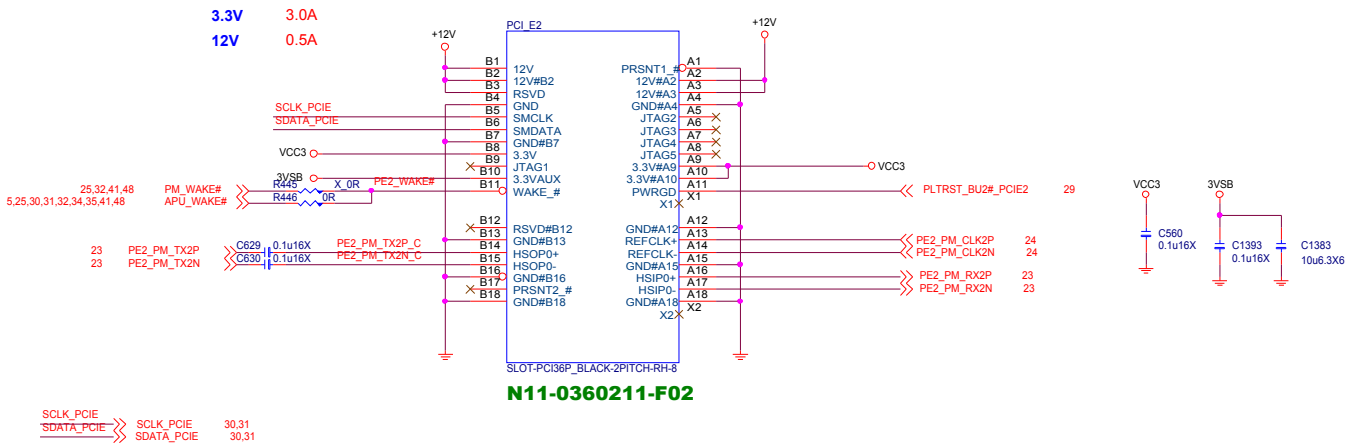
PCIEX1 12V 0.5A
3.3V weak 375mA

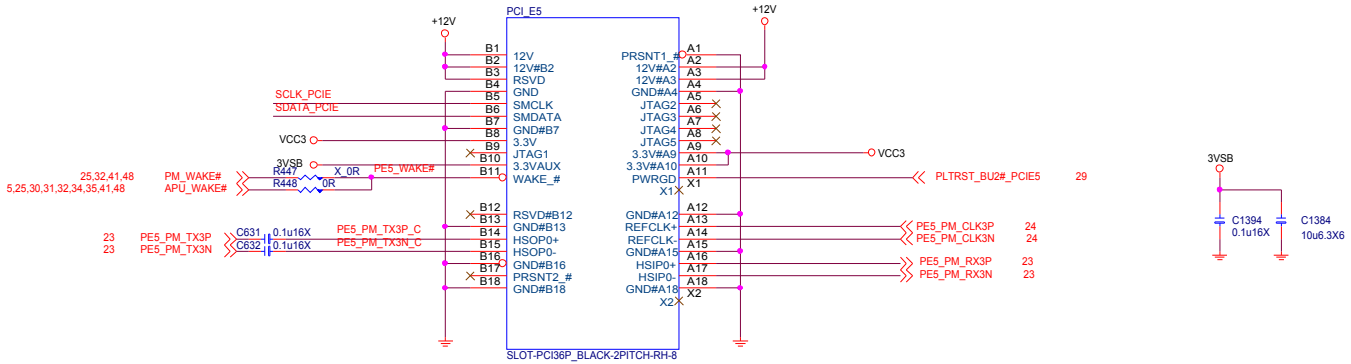
PCI_E2



N11-0360211-F02

SCLK_PCIE
SDATA_PCIE
SCLK_PCIE 30,31
SDATA_PCIE 30,31

PCI_E5



N11-0360211-F02

PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

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Title	PCIE X1 & SLOT2&5		
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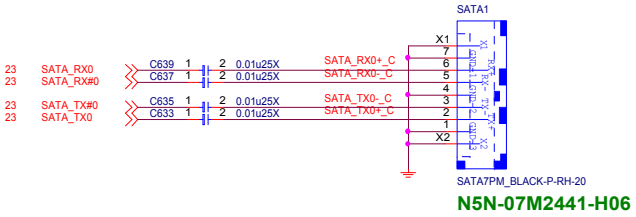
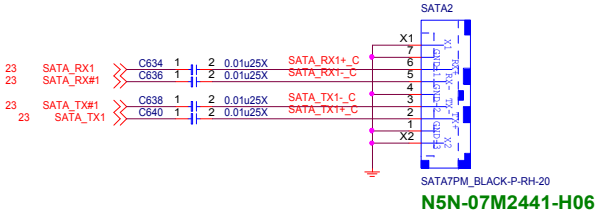
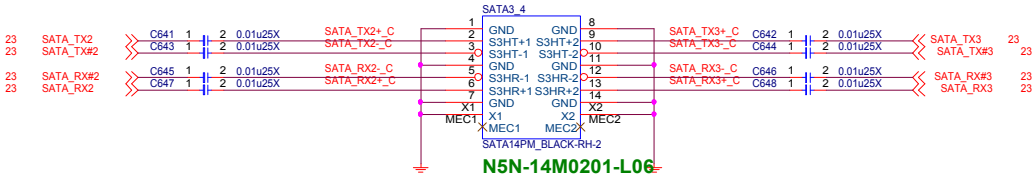
SATA Connector



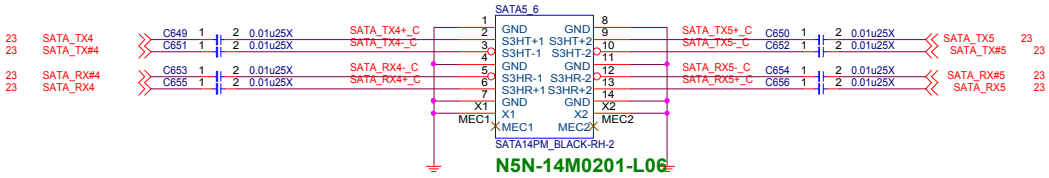
N5N-07M2441-H06



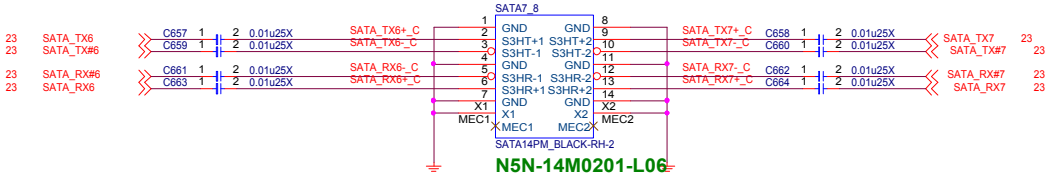
N5N-07M2441-H06



N5N-14M0201-L06



N5N-14M0201-L06



N5N-14M0201-L06

MICRO-STAR INT'L CO.,LTD.

Title: SATA Connector

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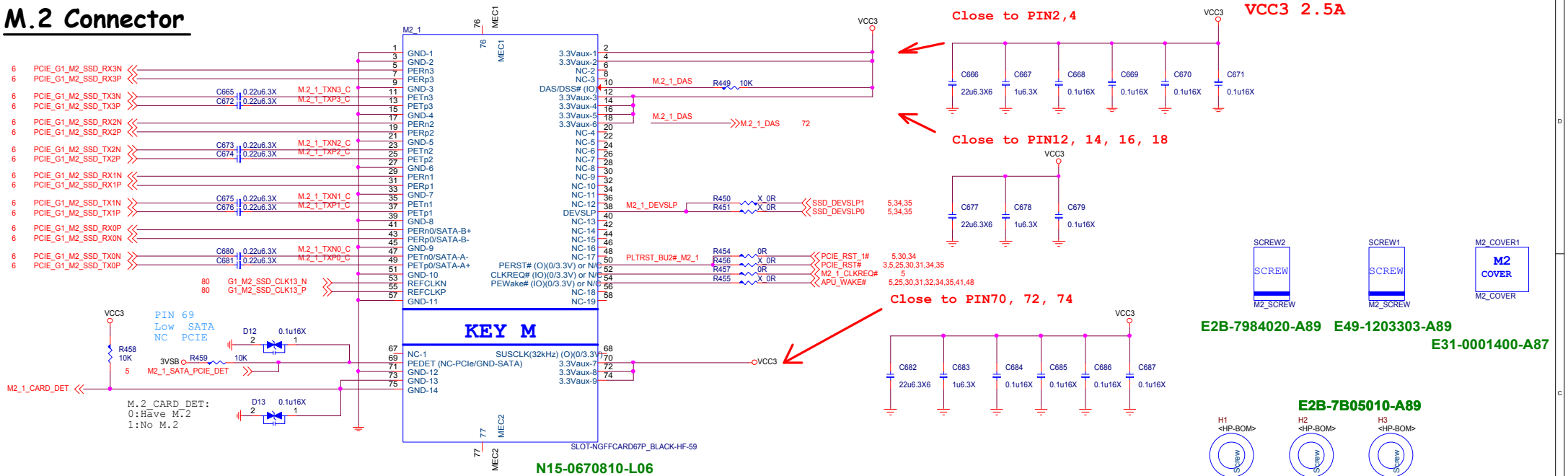
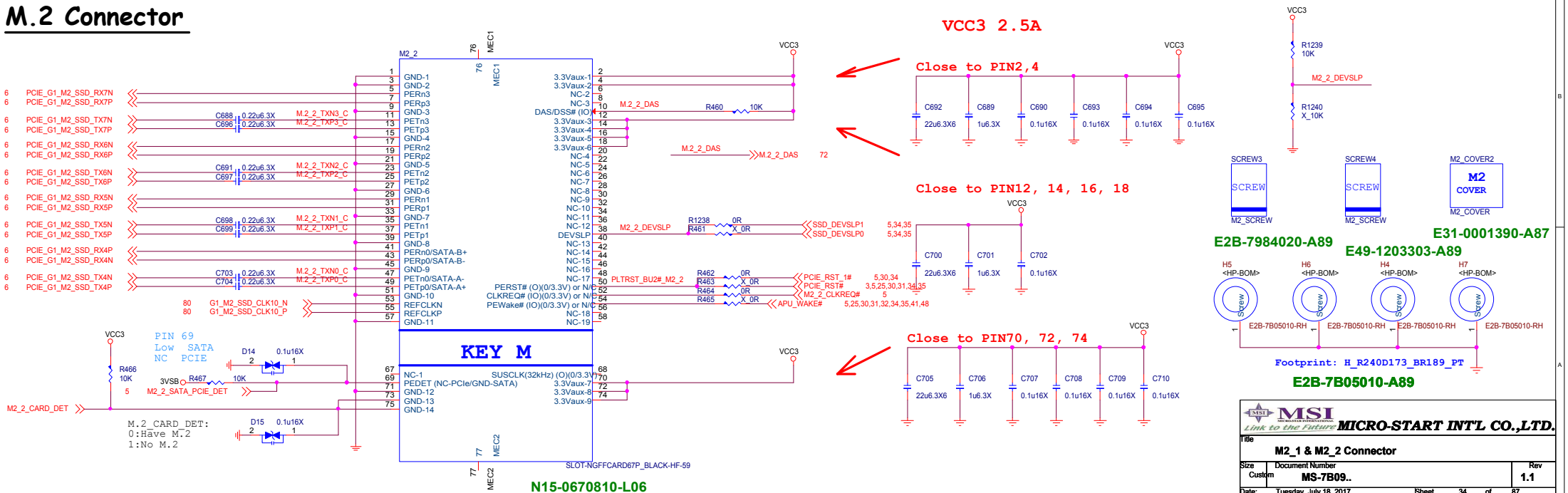
M.2 Connector



N15-0670810-L06

M.2 Connector



N15-0670810-L06

MICRO-START INT'L CO.,LTD.			
Title: M2_1 & M2_2 Connector			
Size: Custom	Document Number: MS-7B09..		Rev: 1.1
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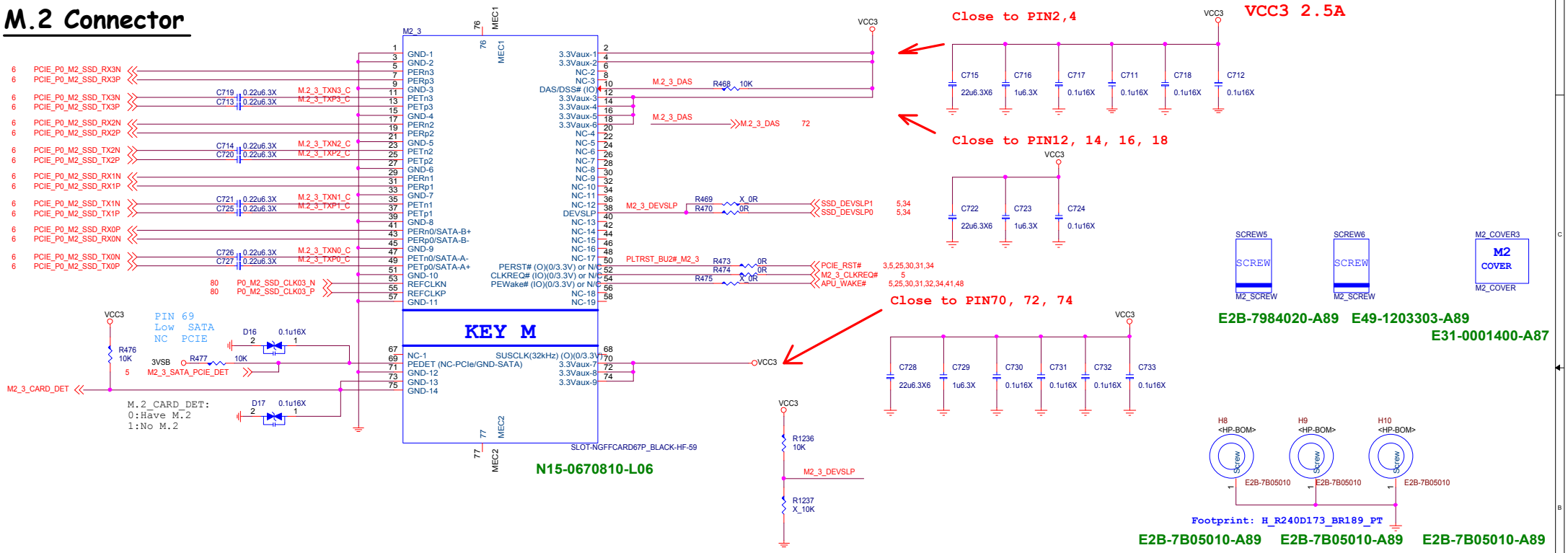
M.2 Connector



Title	M2_3 Connector
Size	Custom
Document Number	MS-7B09..
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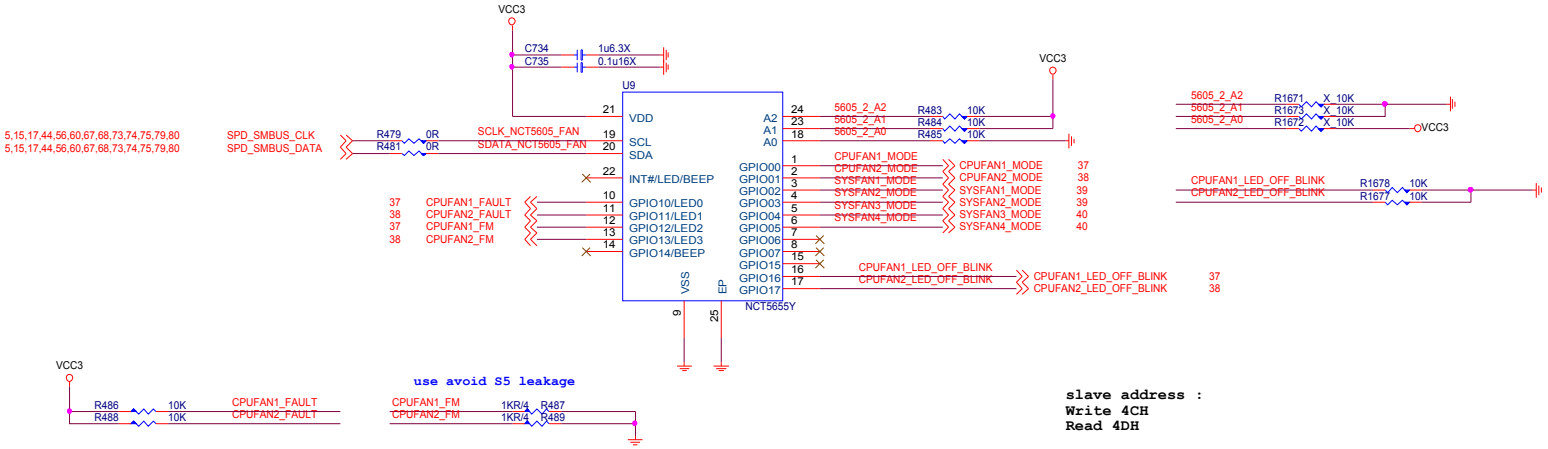
MICRO-START INT'L CO.,LTD.



use avoid S5 leakage

slave address :
Write 4CH
Read 4DH

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: CPU FAN Control		
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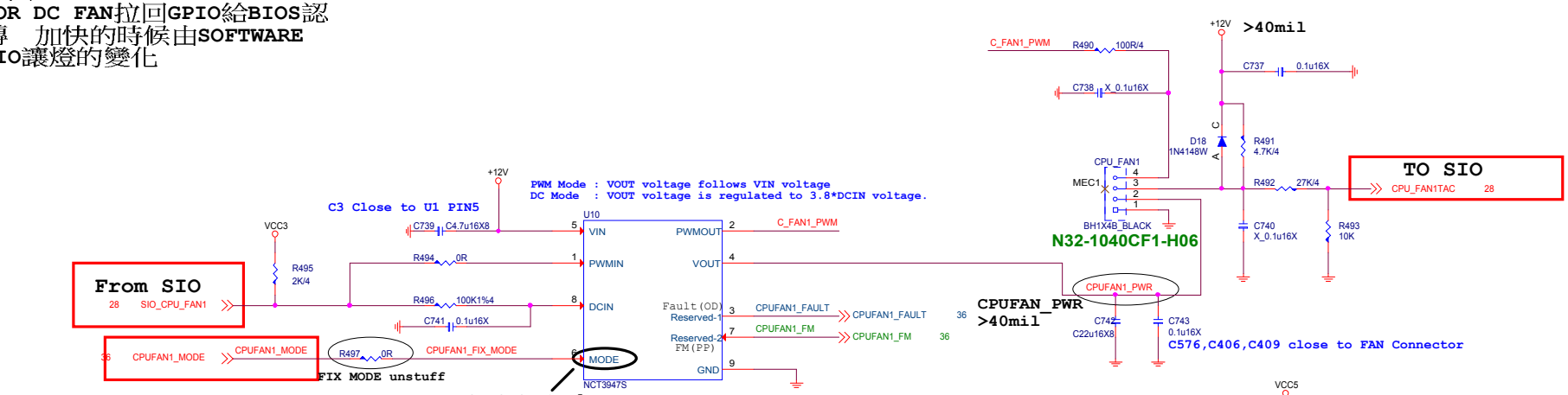
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCP LED(現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCP拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉　加快的時候由SOFTWARE
控制GPIO讓燈的變化



GPIO Control I22-3947S12-N62

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

NCT3947S Internall pull up 1.65V

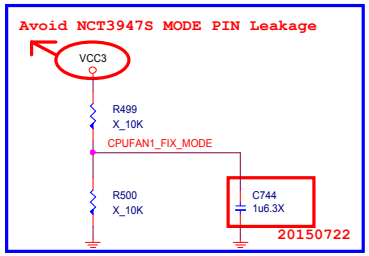
colay NCT3961

OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K

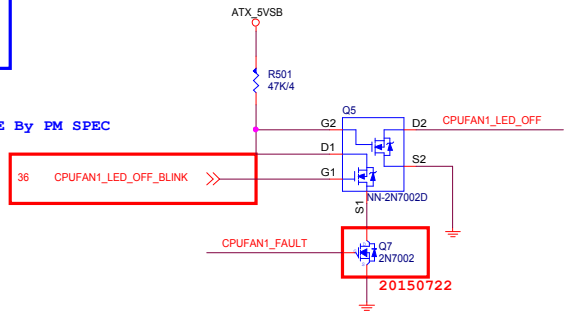
default

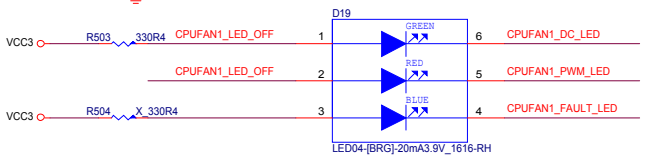
OC SET By PM SPEC

CPUFANX_FAULT



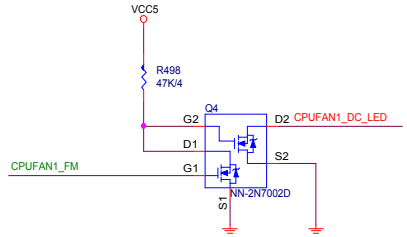
Resever For FIX DC or PWM MODE USE By PM SPEC



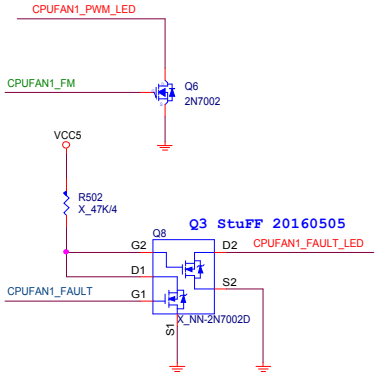


RGB
D0C-040S400-H91

20161024 Update
DC_FAN_LED( )
PWM_FAN_LED(藍)
FAN_OCP_LED(紅)



CHECK NCT3947S Sink Current



Q3 StuFF 20160505

CHECK NCT3947S Sink Current

1. MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2. FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title	CPU FAN1-TYPE J	
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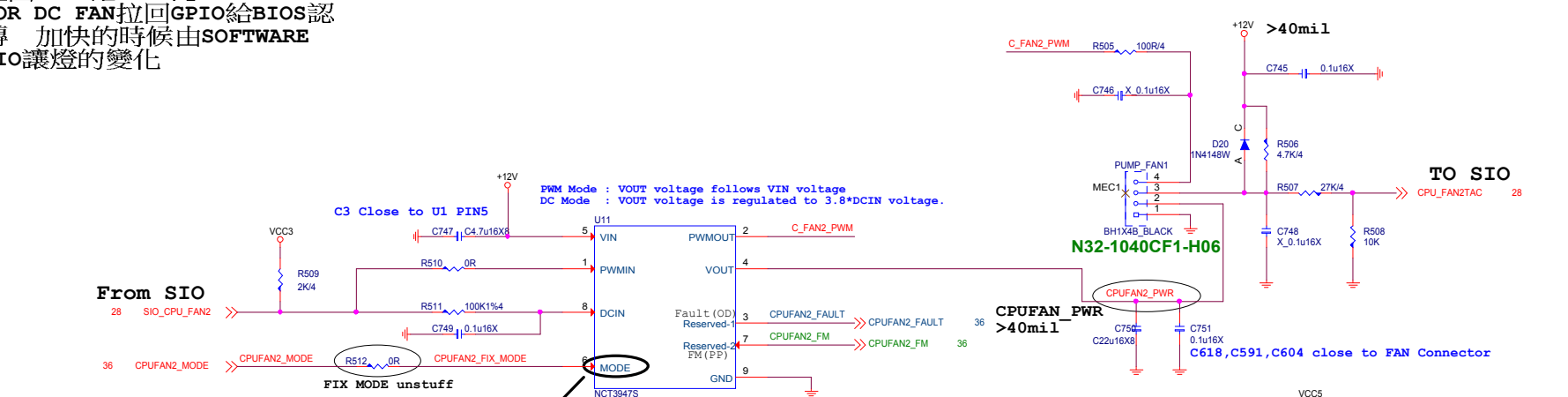
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCP LED(現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCP拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉　加快的時候由SOFTWARE
控制GPIO讓燈的變化



1. MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2. FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

MSI MICRO-STAR INT'L CO.,LTD.

Title	CPU FAN2-TYPE J(PUMP)	
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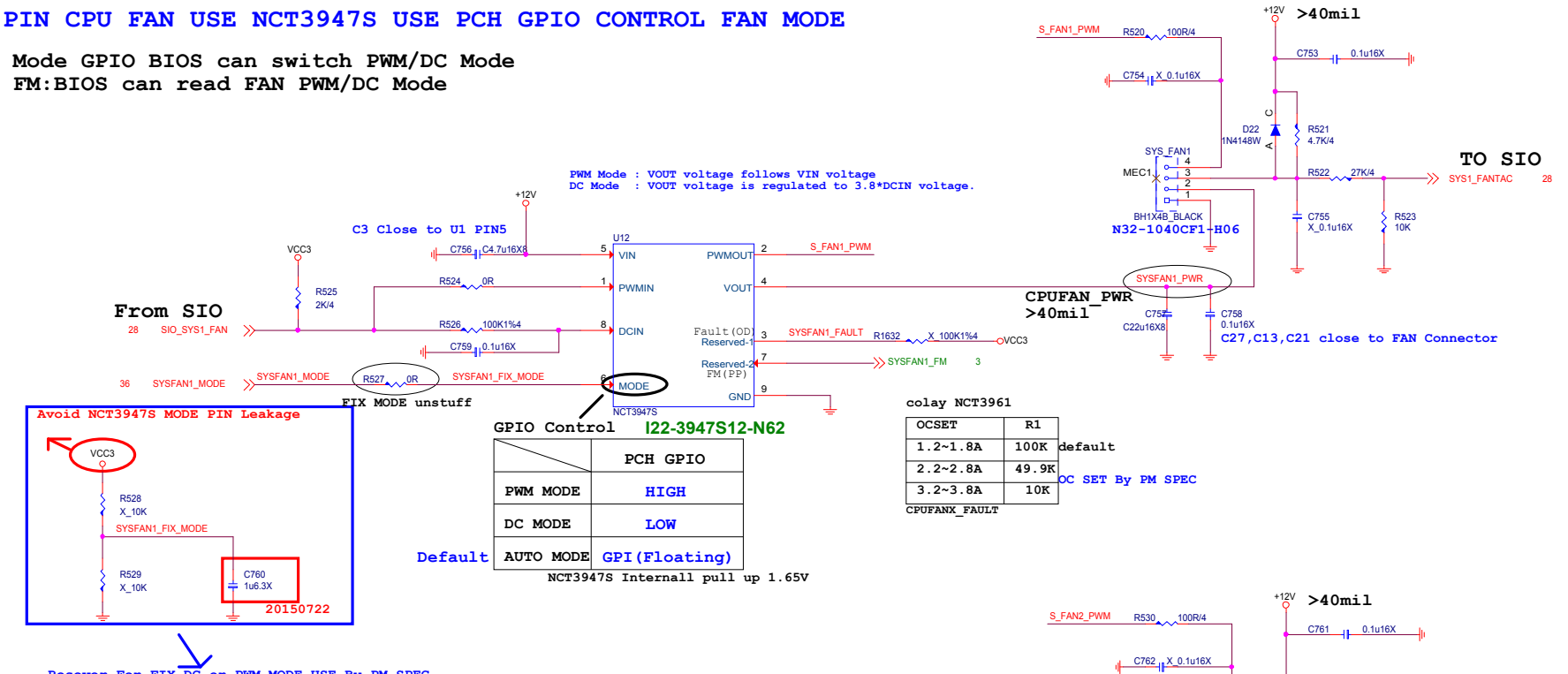
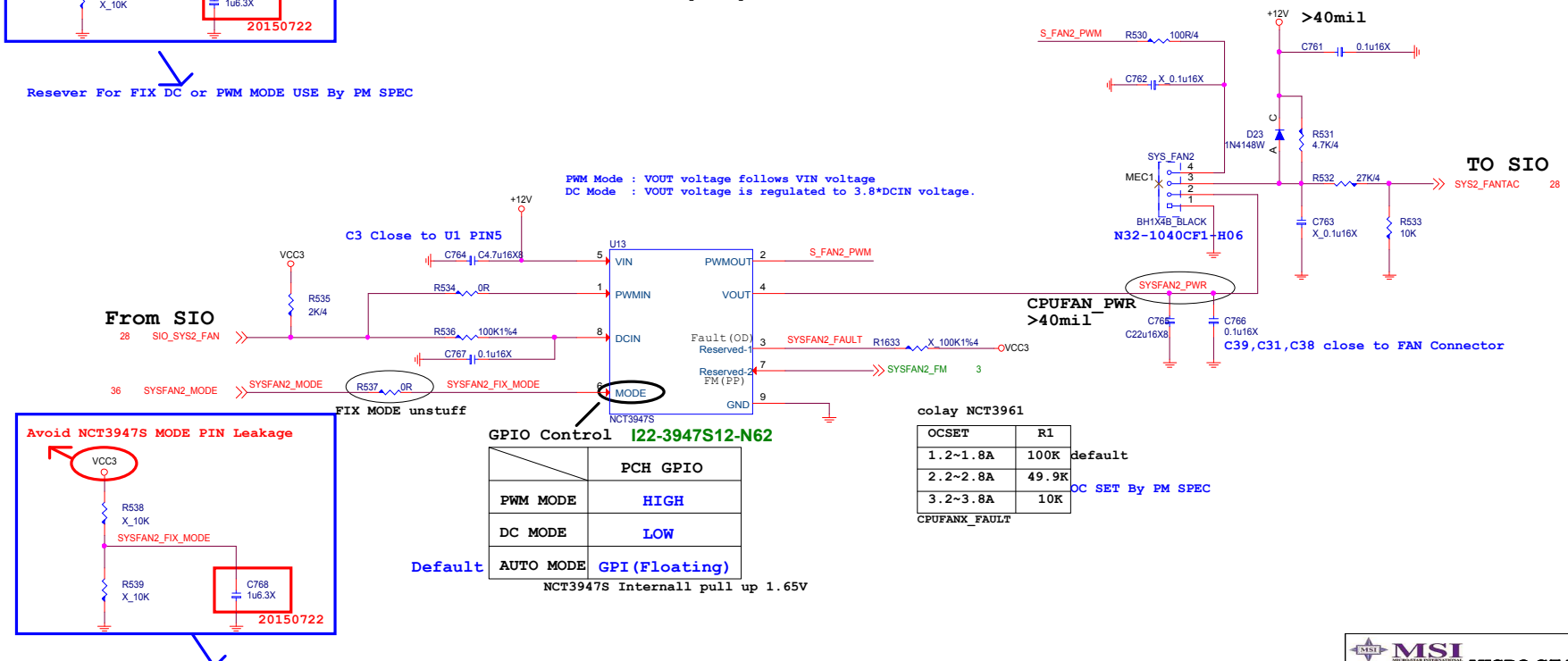
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode
2. FM:BIOS can read FAN PWM/DC Mode



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	
3.2~3.8A	10K	



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	
3.2~3.8A	10K	

Resever For FIX DC or PWM MODE USE By PM SPEC

MICRO-START INT'L CO.,LTD.

Title: SYSTEM FAN1/2-TYPE L

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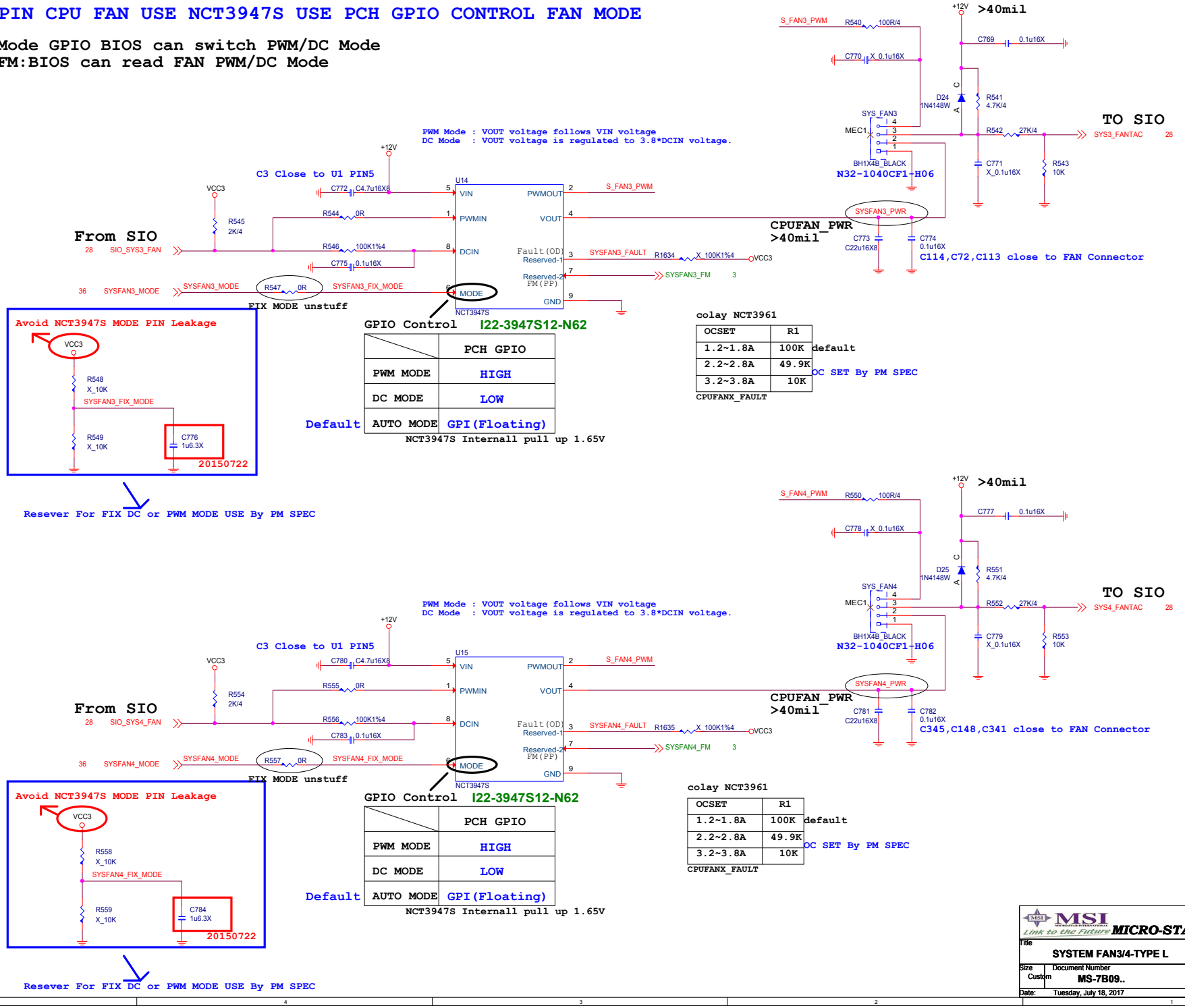
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode
2. FM:BIOS can read FAN PWM/DC Mode



MICRO-START INT'L CO.,LTD.

Title: SYSTEM FAN3/4-TYPE L

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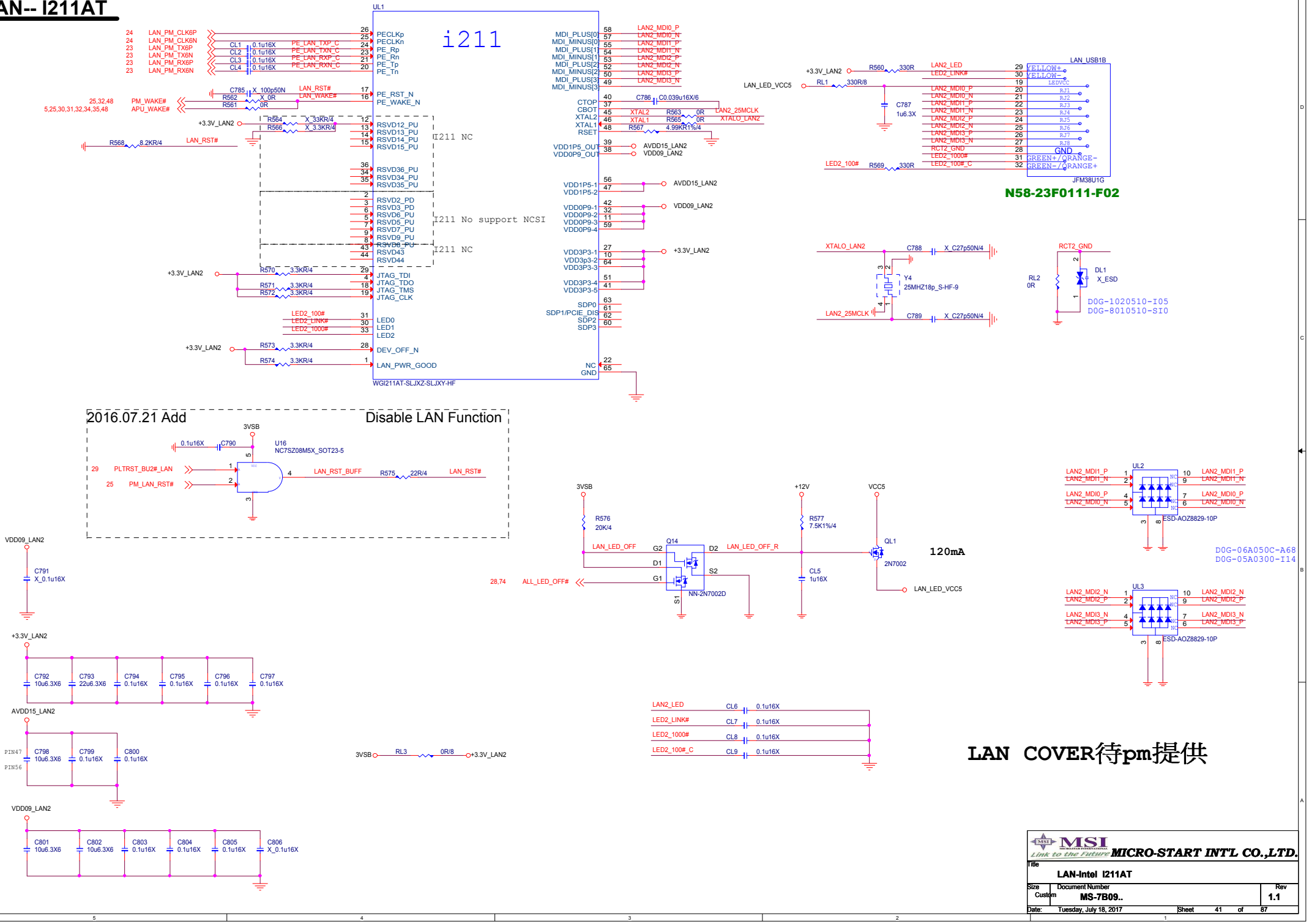
LAN-- I211AT



MICRO-START INT'L CO.,LTD.	
Title	LAN-Intel I211AT
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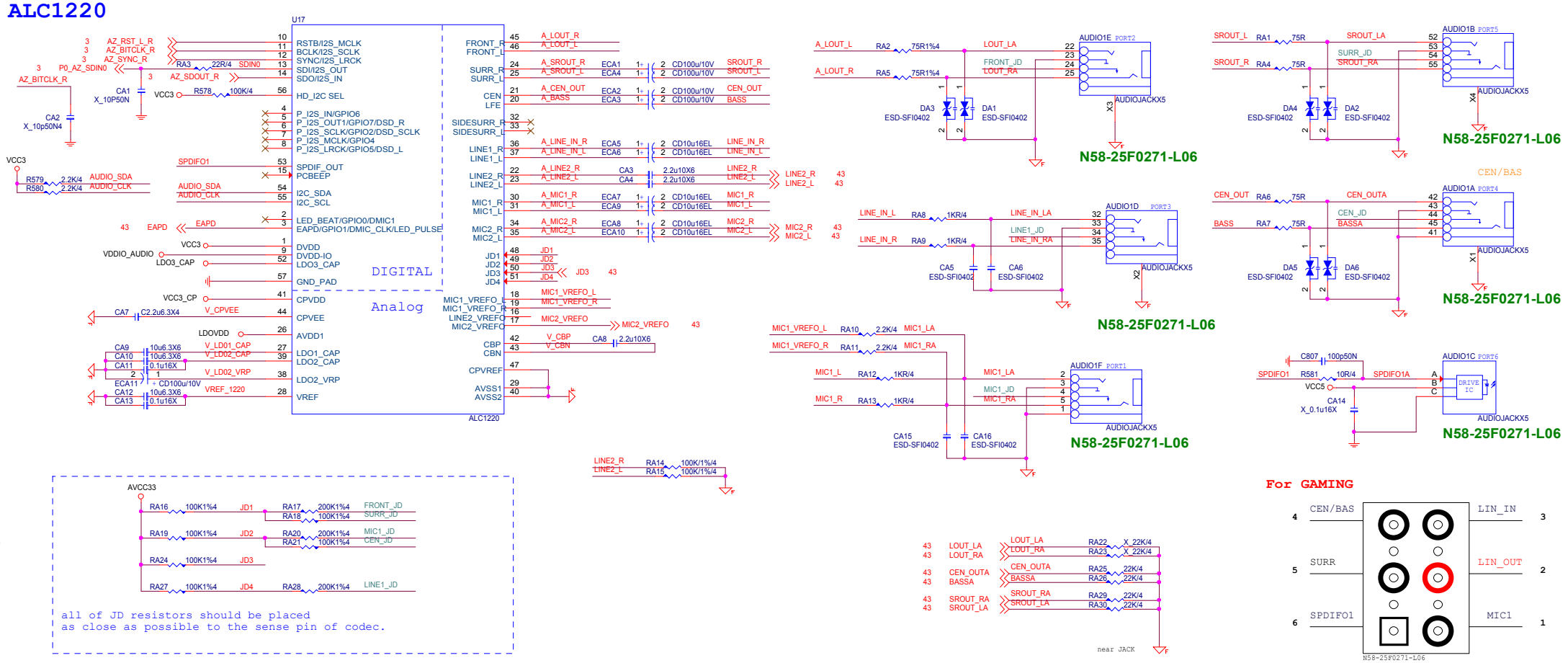
ALC1220



N58-25F0271-L06

N58-25F0271-L06

CEN/BAS

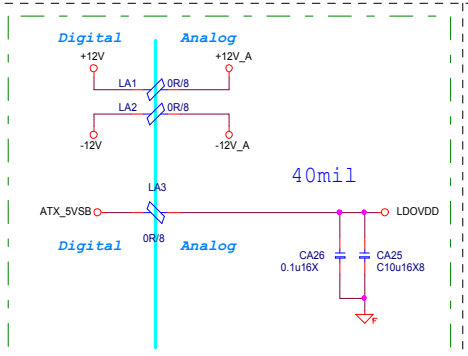
N58-25F0271-L06

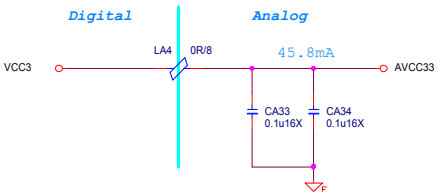
N58-25F0271-L06

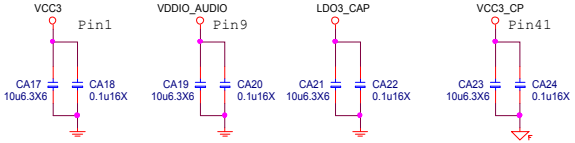
N58-25F0271-L06

N58-25F0271-L06

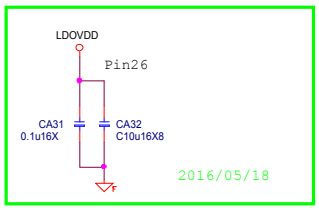
For GAMING





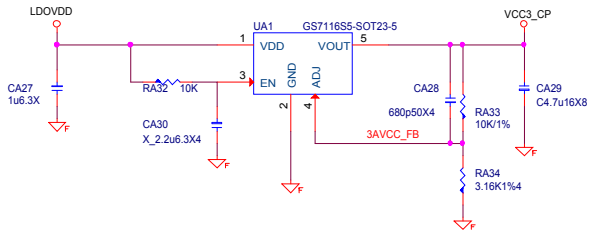


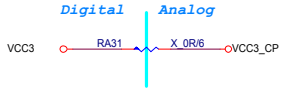
Closed Codec



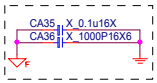
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

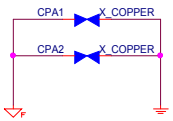
CPVDD:150mA





EMI





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Link to the Future

Title	Audio ALC1220-1		
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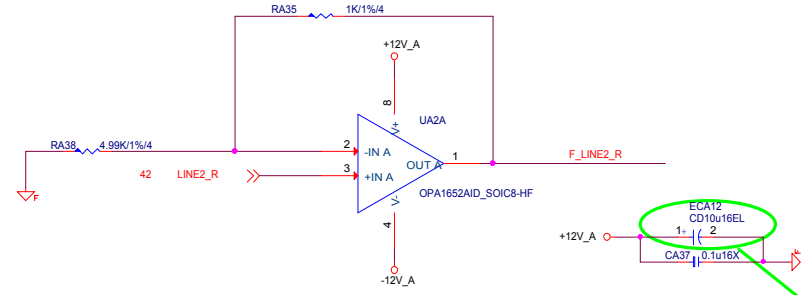
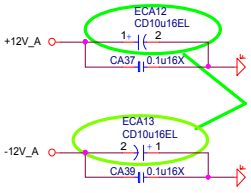
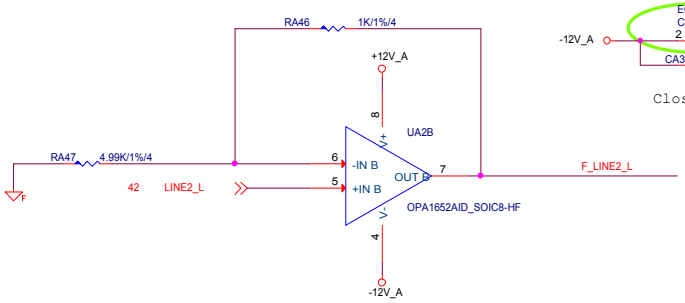
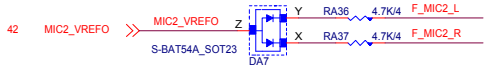


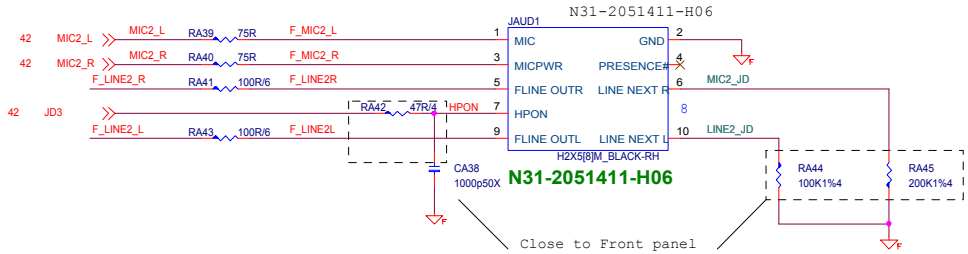


OC : C11-1067514-T04
GAMING: C91-1001611-N10

Close to U3





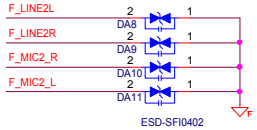


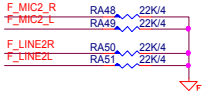
Close to Front panel
For HDA/AC97 front cable.

Close to Jack

ESD protect

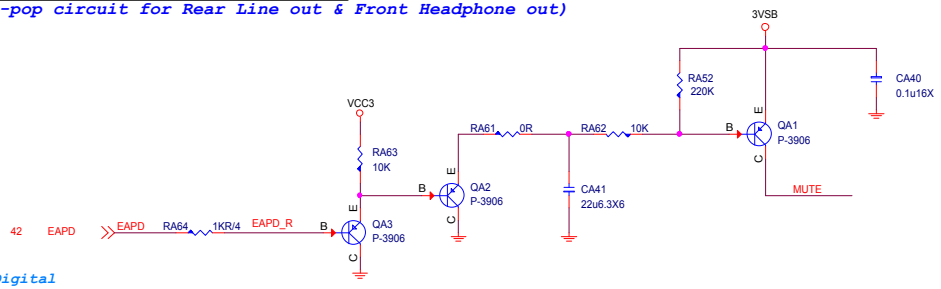
D0G-2950500-SI0
D0G-3010510-I05





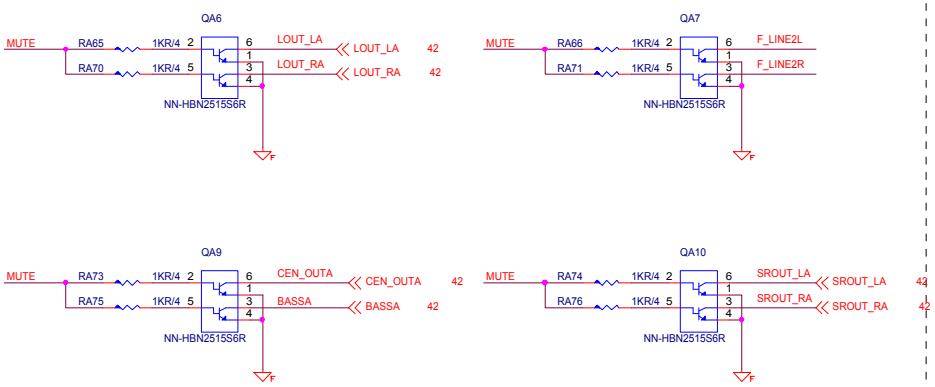
Rear Line OUT De-POP circuit

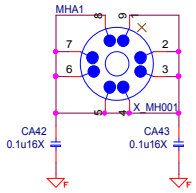
(De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog





MSI MICRO-STAR INTERNATIONAL
Link to the Future
MICRO-START INT'L CO.,LTD.

Title	**Audio ALC1220-2**	
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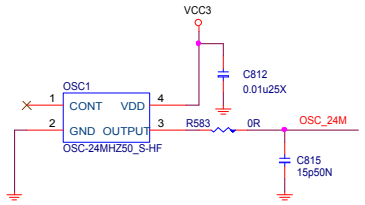
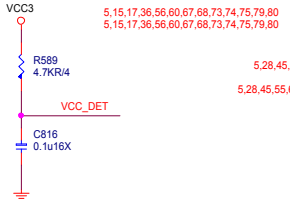
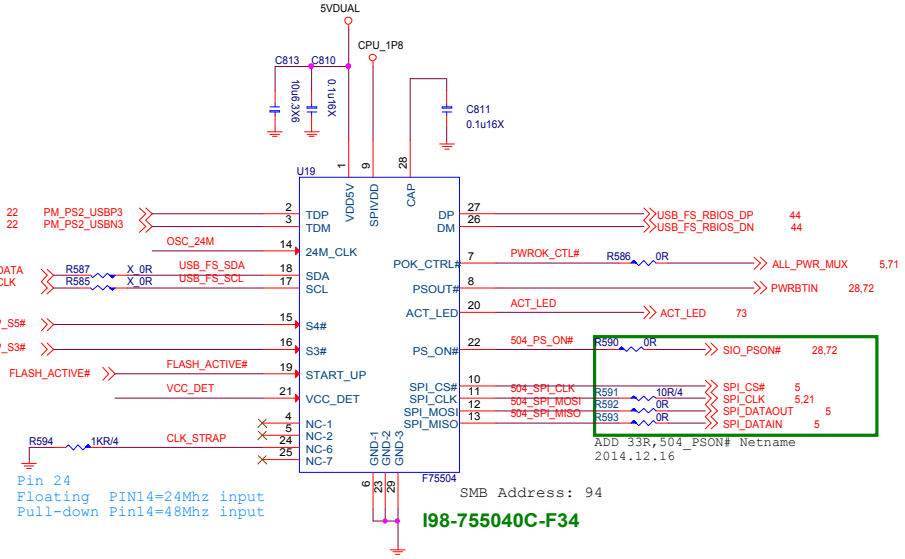
USB Flash BIOS

Host USB connector





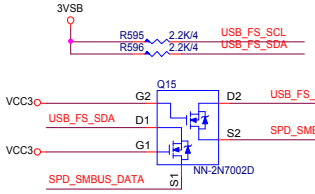


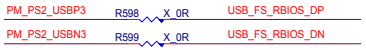
ADD 33R,504_PSON# Netname
2014.12.16

Pin 24
Floating PIN14=24Mhz input
Pull-down Pin14=48Mhz input

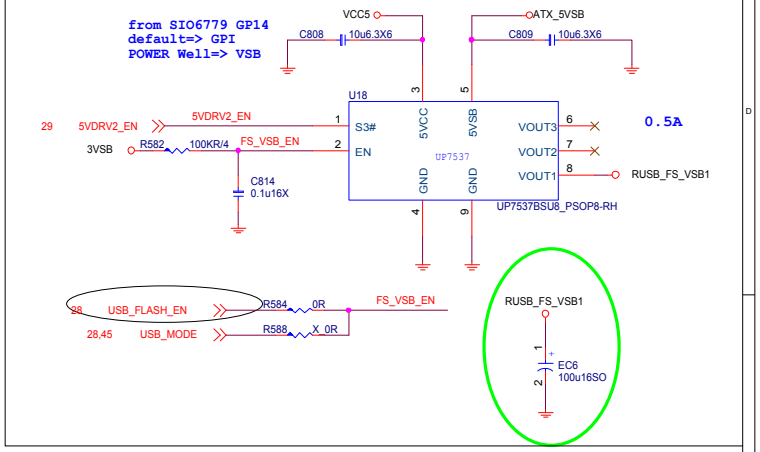
SMB Address: 94

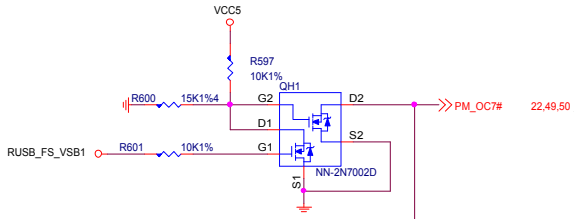
I98-755040C-F34





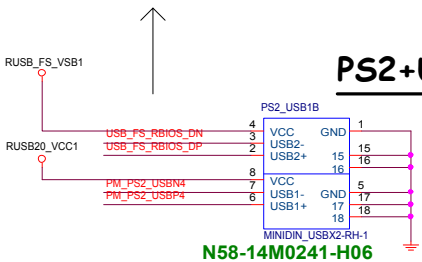
REAR Flash BIOS USB PORT 9





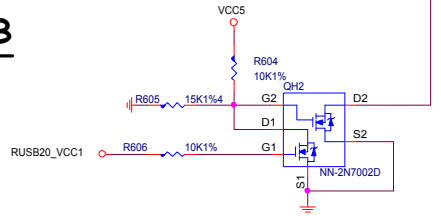
OC# signal connect to
SB OC pin.

USB Connector power come from UP7537
provide(USB Hotkey Connector same)

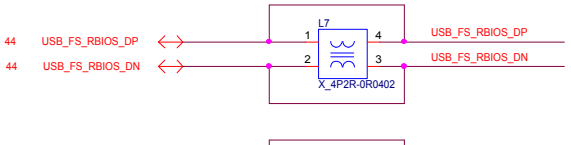


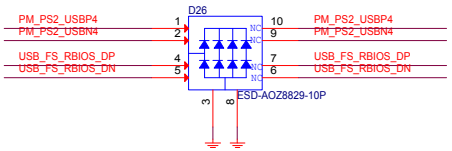
PS2+USB

N58-14M0241-H06

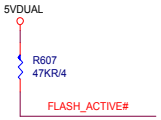


OC# signal connect to
SB OC pin.



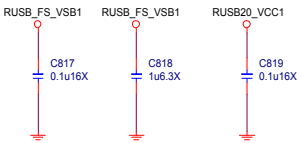


ESD close to connector.
(use usb3.0 ESD for eye diagram)



Reserved for when F75501 Hotkey device fail use

* All close to Front IO side



MICRO-START INT'L CO.,LTD.

Title: USB Flash BIOS

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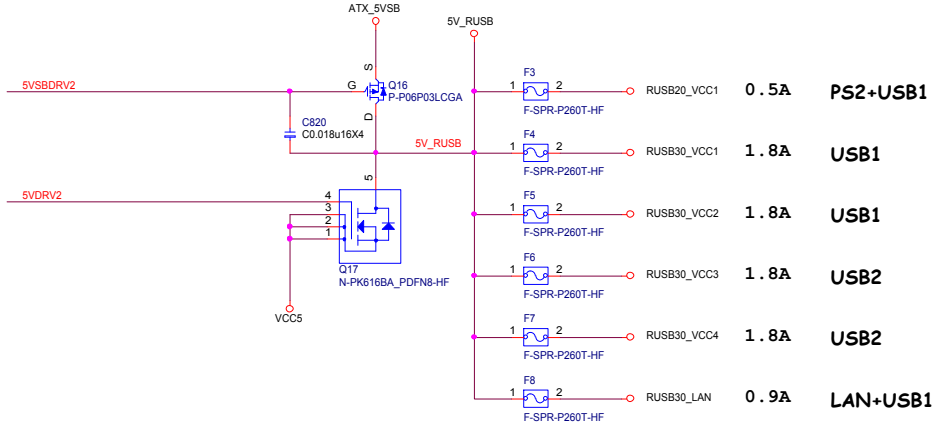
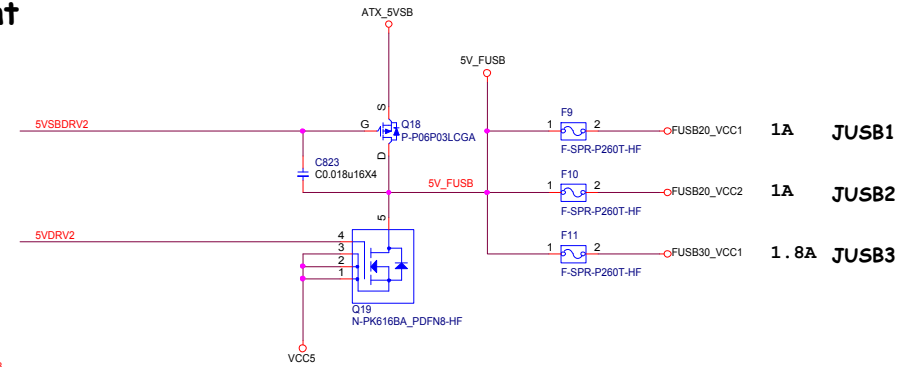
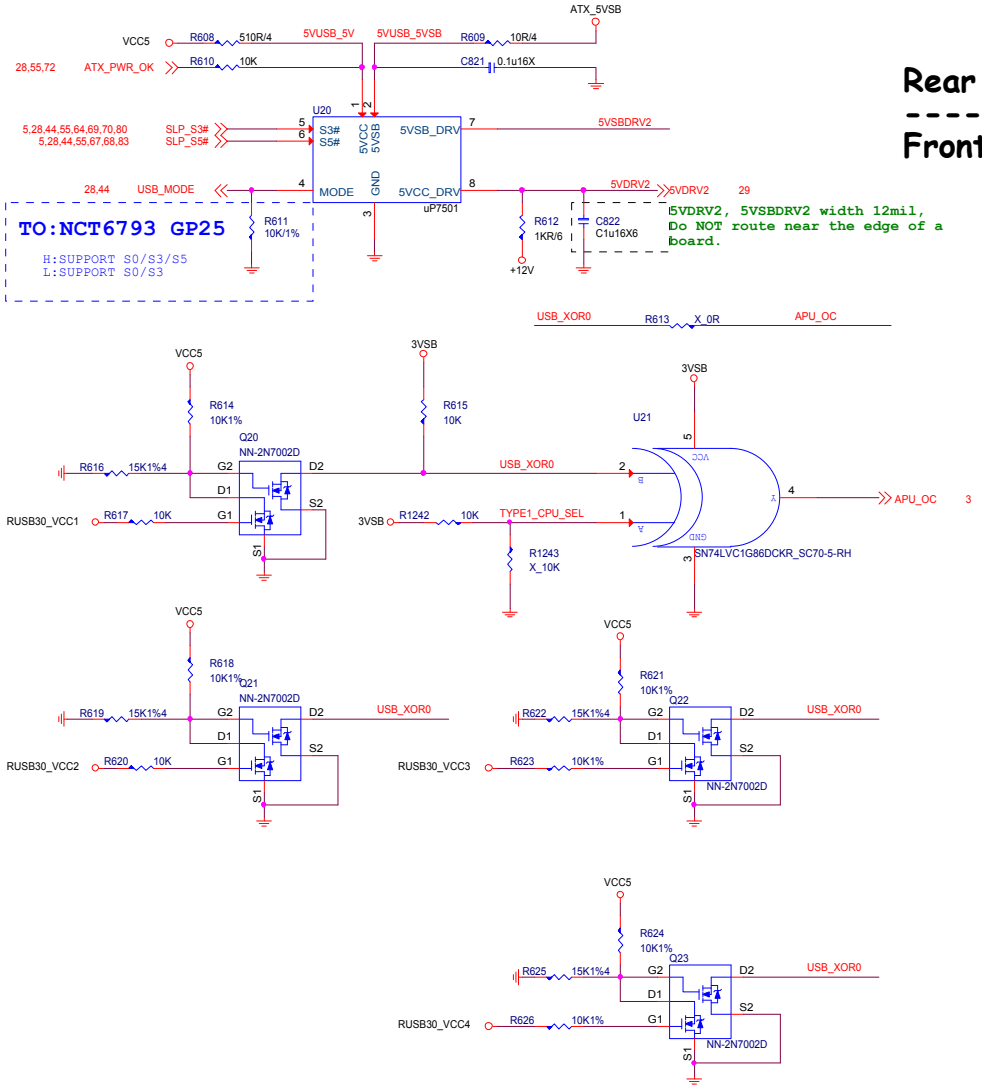
USB Power



Rear

Front





	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-START INT'L CO.,LTD.

Link to the Future

Title: USB Power		
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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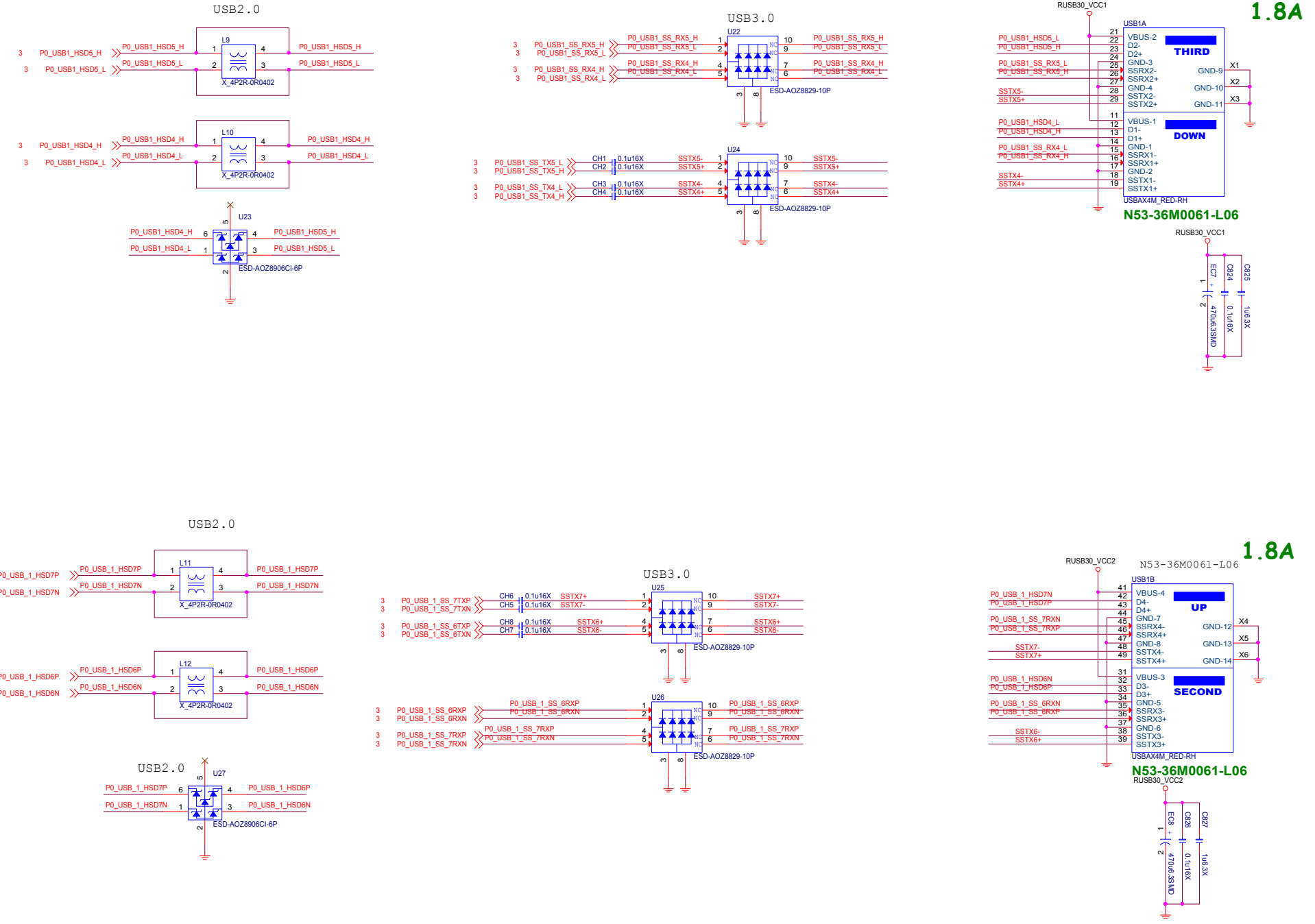
USB1



MICRO-START INT'L CO.,LTD.

Link to the Future

Title	USB1 Rear Side-TYPEA	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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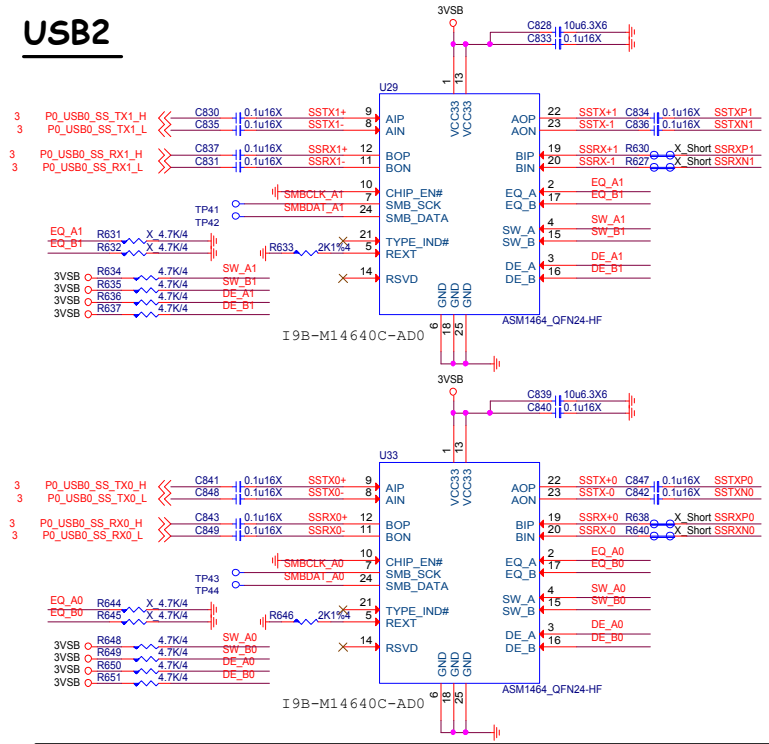
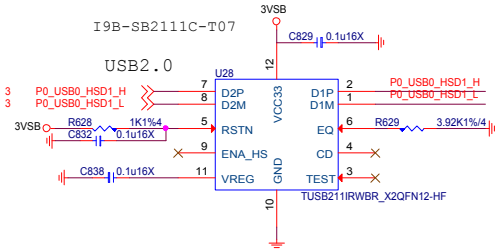
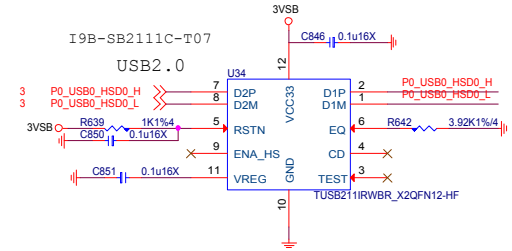
USB2



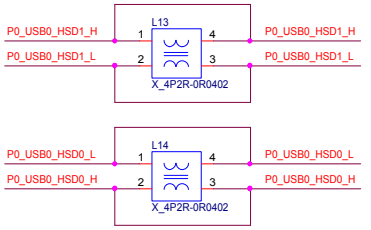


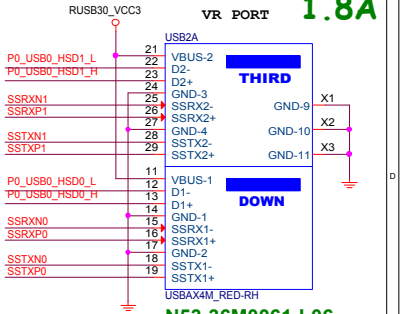
I9B-SB2111C-T07



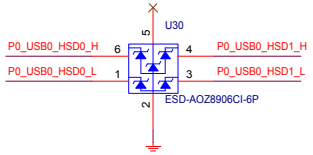
I9B-SB2111C-T07

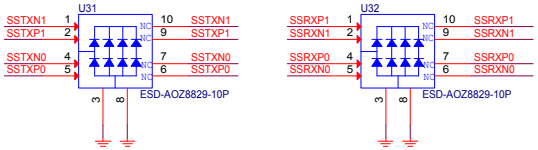
USB2.0

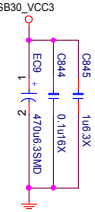


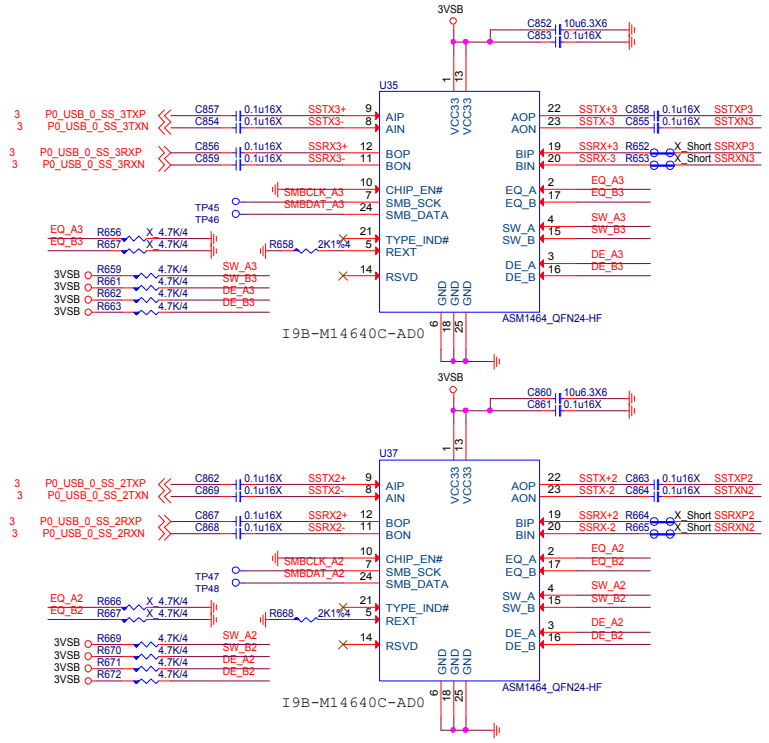


N53-36M0061-L06

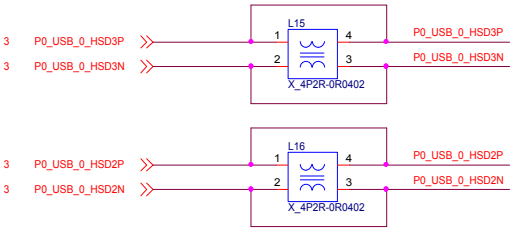




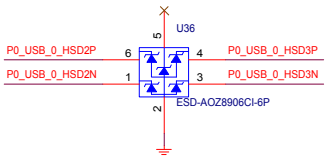


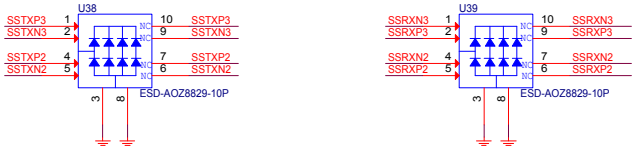


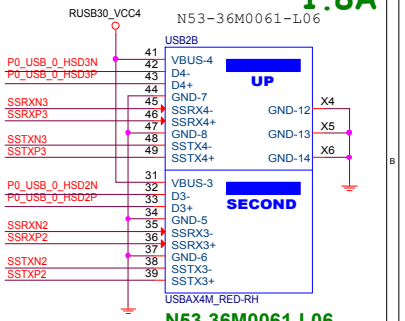
USB2.0



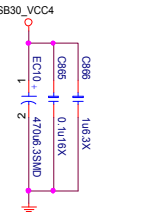
USB2.0







N53-36M0061-L06



MSI MICRO-STAR INT'L CO.,LTD.

Link to the Future

Title	USB3.0 Rear Side-VR	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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Use pure PCIE must provide CLK

Minimun gap should be greater of >15mil with other signal.

USB HS (90Ohm-Diff)

Chip to Connector ~1.5 inch.

PCIE Rule (Follow PM PDG)

USB SS (80Ohm-Diff)

ASM3142

B02-031420C-AD0

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

For SRIS mode

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

Power Consumption

	3.3V	3.3VSUS	2.5V	1.1V	1.1VSUS	Unit
ASM3142	TBD	TBD	TBD	TBD	TBD	mA
ASM2142	4	9	220	470	10	mA

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S): 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

SMD Crystal use 3225 size
M:D04-0900900-SC6
S:D04-0901100-T16
S:D04-0901200-F07

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

atx5vsb change to vcc5

2016.07.21 Add — Disable ASM1142 Function

ASM3142 1.1v Core Power

SN:L01-0107108-C08

MP2143DJ_TSOT23-8-RH

ASM3142 1.1v Suspend Power

ASM3142 2.5v Analog Power

EEPROM

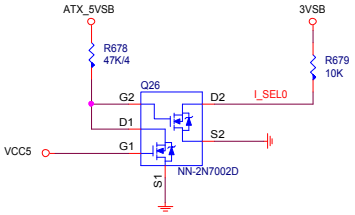
M31-25L1022-M24

M:M31-25L1022-M24 (1M)
S:M31-25X2023-W03 (2M)

MICRO-START INT'L CO.,LTD.

Title	USB3.1 ASM1142-1		
Size: Custom	Document Number: MS-7B09..		Rev: 1.1
Date: Tuesday, July 18, 2017	Sheet 48 of 87		

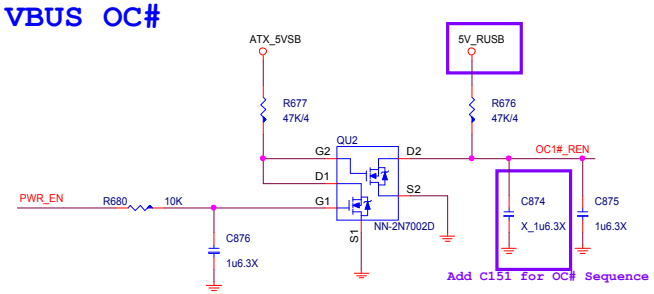
Current Mode

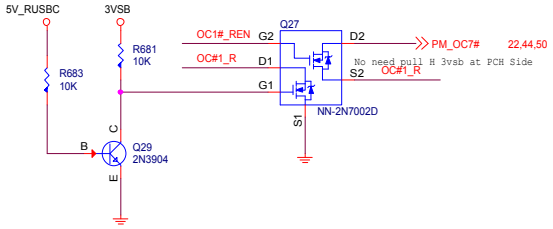


I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

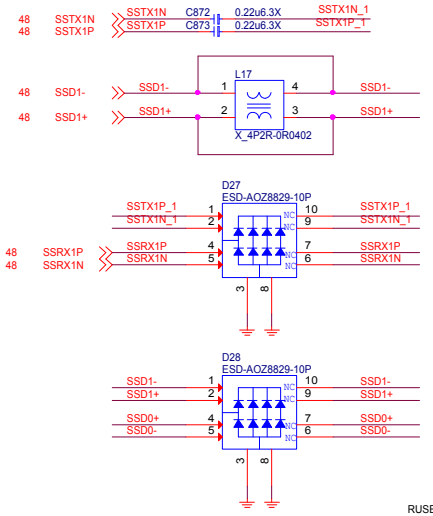
1.5A under S3 mode
3A under S0 mode

VBUS OC#

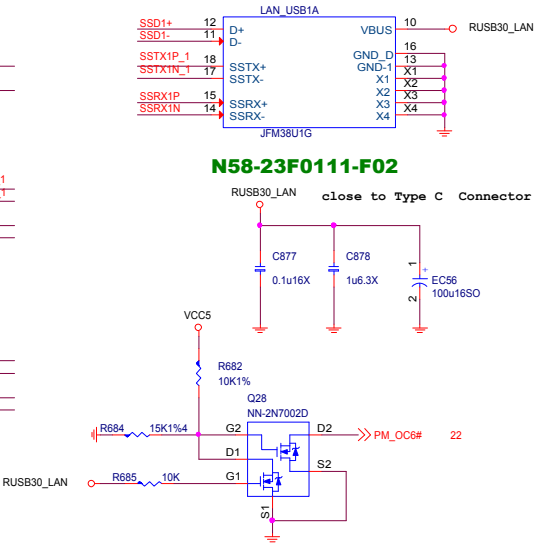




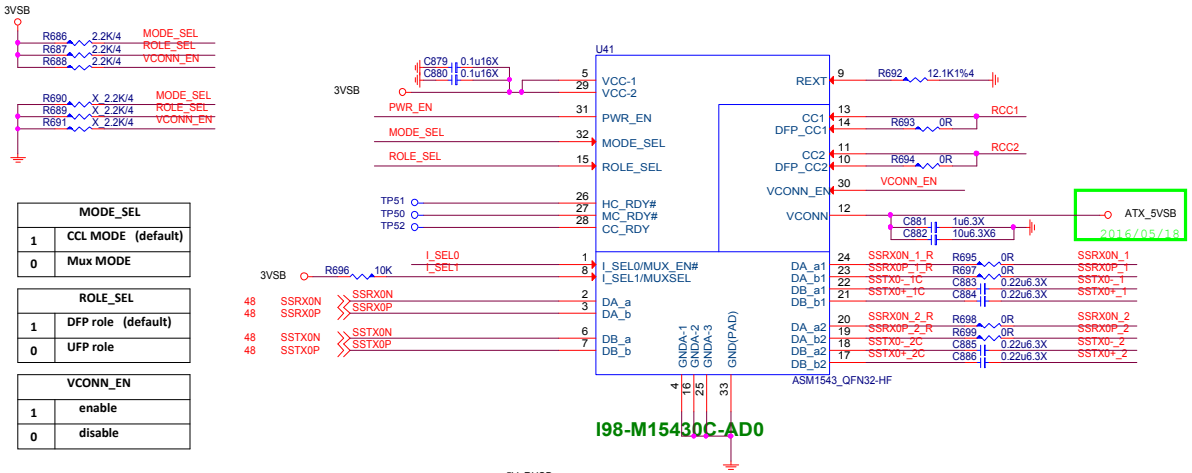
TYPE-A



LAN+USB TYPEA



USB Type-C MUX with Configuration Channel (CC)

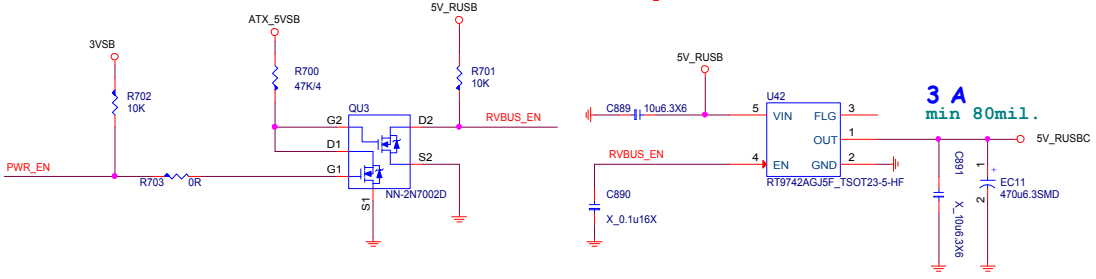


I98-M15430C-AD0

MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

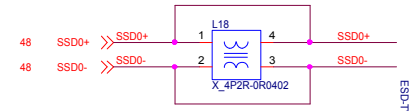
ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

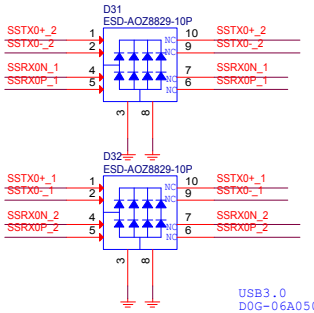


3 A
min 80mil.

TYPE-C



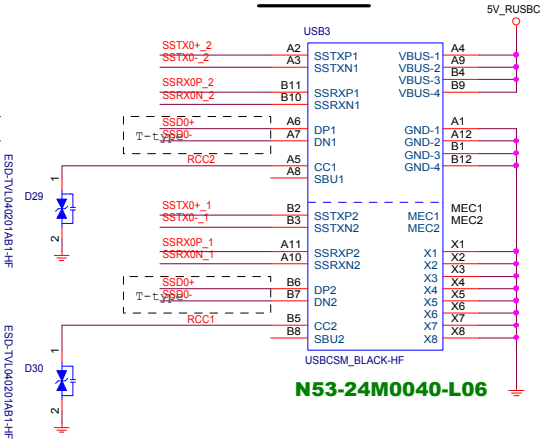
ESD Protection
NEAR CONNECTOR



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL

TYPEC

OC#4



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	USB3.1 ASM1142-2	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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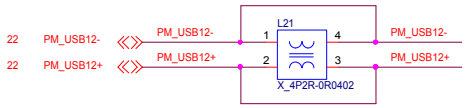
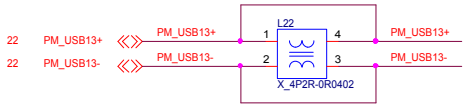
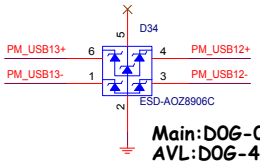
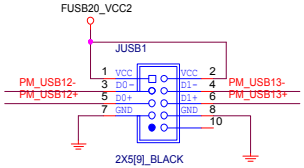
JUSB1+JUAB2



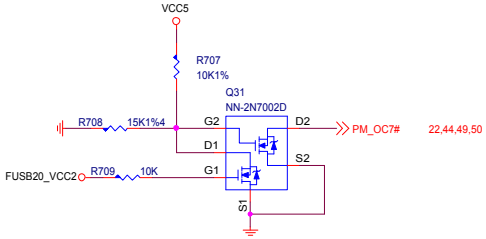


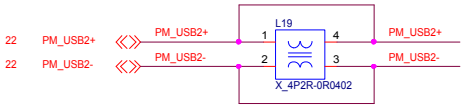


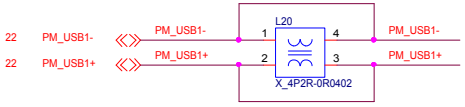
Main:DOG-05A0529-A68
AVL:DOG-45B0510-I14

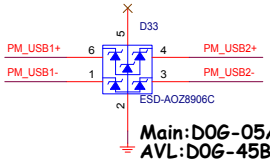


N31-2051BG1-H06

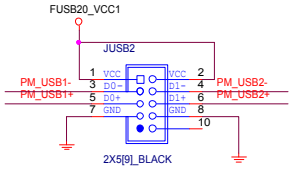




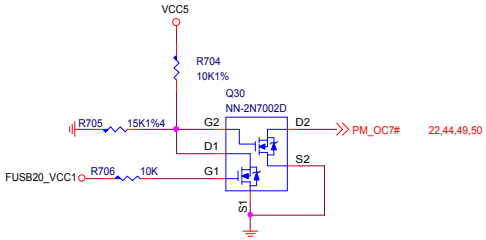




Main:DOG-05A0529-A68
AVL:DOG-45B0510-I14



N31-2051BG1-H06

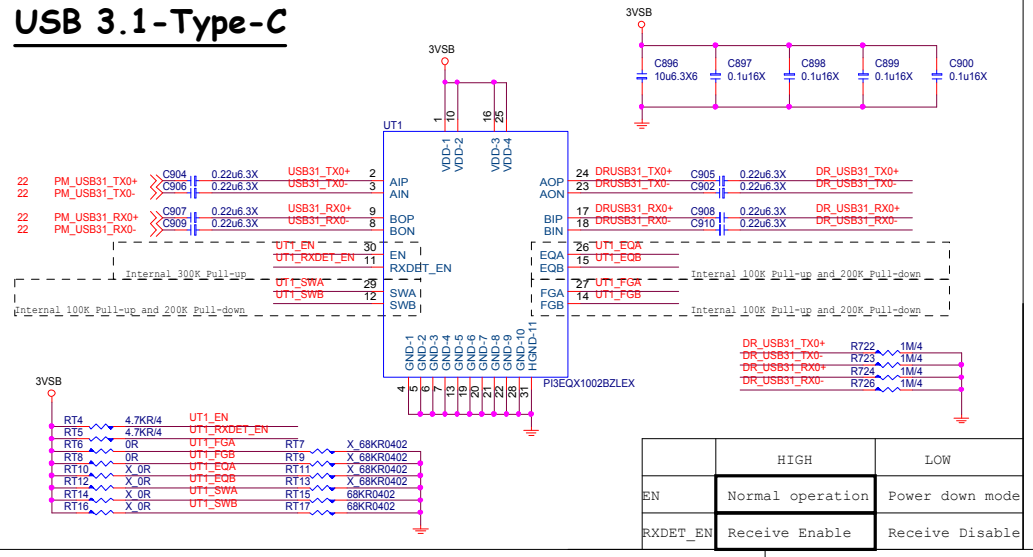


MSI MICRO-STAR INT'L CO.,LTD.

Link to the Future

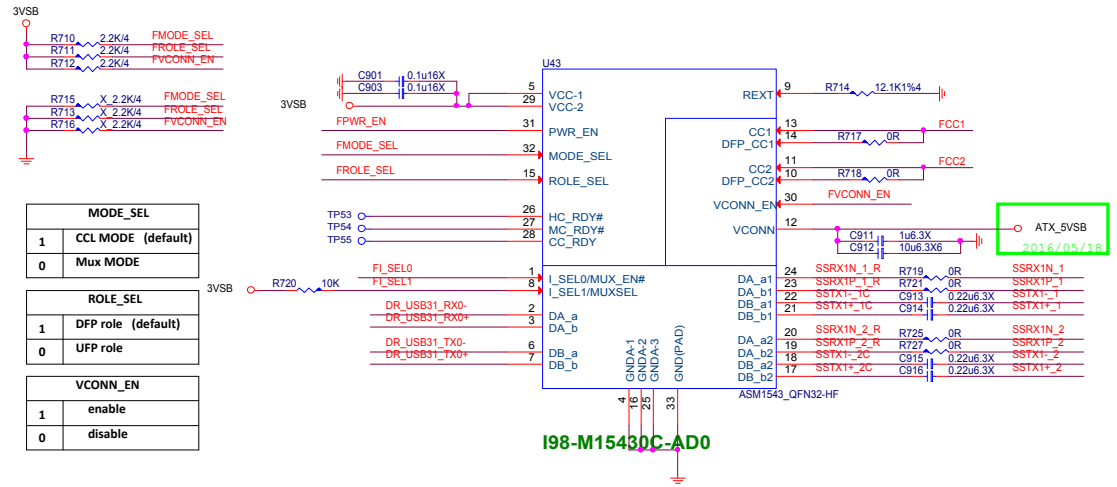
Title: USB Front Side-USB2.0		
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
Date: Tuesday, July 18, 2017	Sheet 50 of 87	

USB 3.1-Type-C



	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

USB Type-C MUX with Configuration Channel (CC)



I98-M15430C-AD0

MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

EQA/B are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B	*@2.5GHz*	*@5GHz*
0	5.1	10.9
R	1.9	6.7
F	3.5	8.9 (Default)
1	6.8	13.1

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

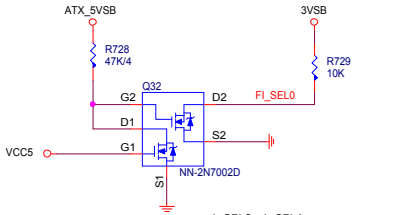
	Flat Gain Settings
FGA/B	*dB*
0	-3
R	-1.5
F	0 (Default)
1	+2

-1dB compression point linear Swing Setting:

SWA/B are the selection bits for the output linear swing setting

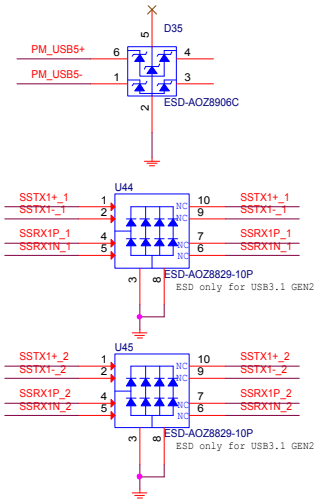
	Output Linear Swing Settings
SWA/B	*mVppd*
0	800
R	1200
F	1000 (Default)
1	1100

Current Mode

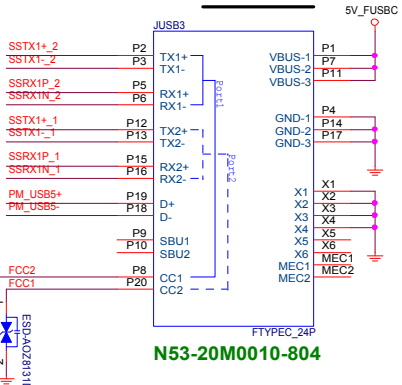


I_SEL0	I_SEL1	
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

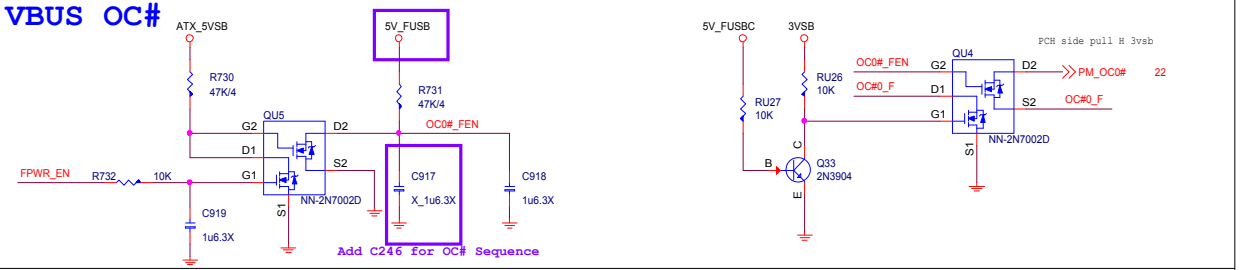


JUSB3

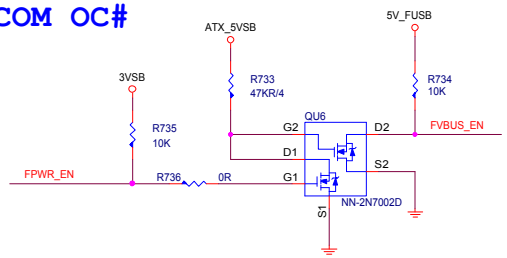


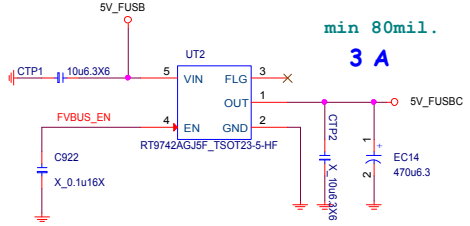
N53-20M0010-804

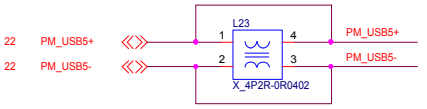
VBUS OC#

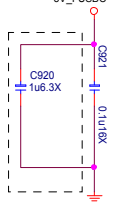


VCOM OC#









MICRO-START INT'L CO.,LTD.

Title	USB3.1 TYPE C-Front	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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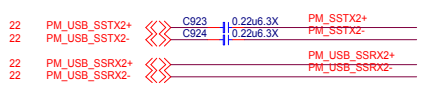
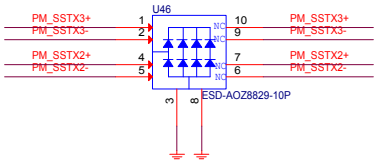
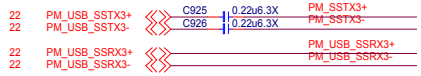
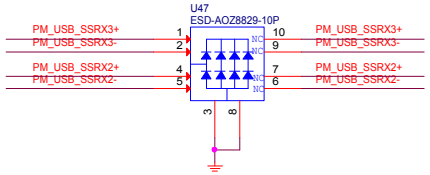
USB 3.0-JUSB4

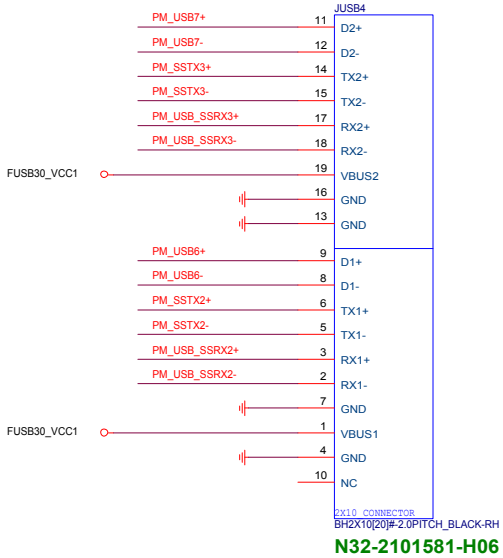




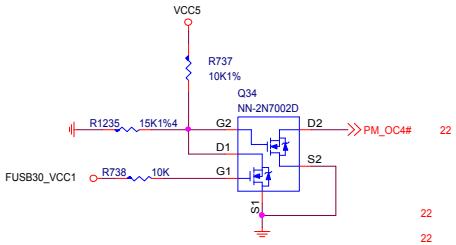


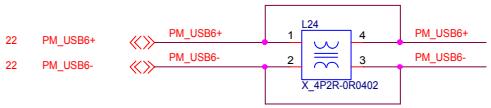


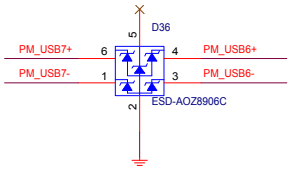
1.8A

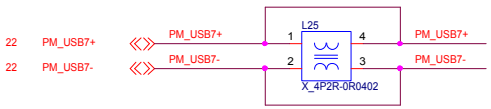


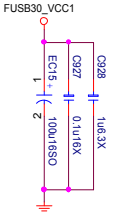
N32-2101581-H06











MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: USB Front Side-JUSB4		
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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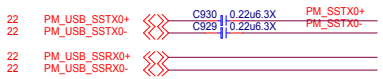
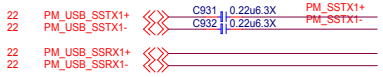
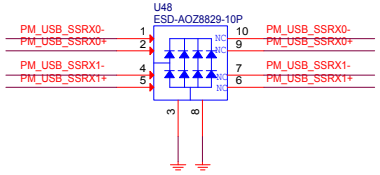
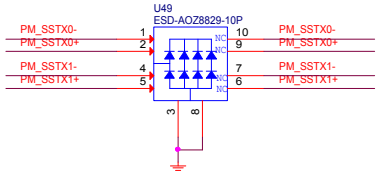
USB 3.0-JUSB5 With Charge(BC1.2)

1.7A+1.7A



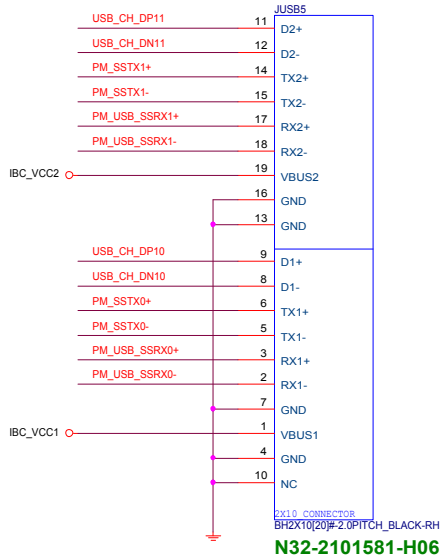




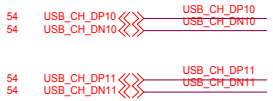


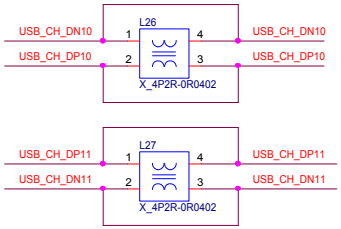
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

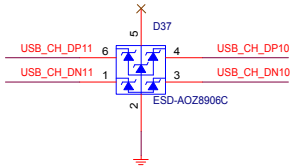
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

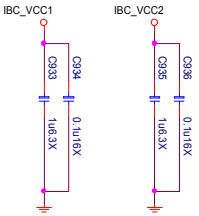


N32-2101581-H06









MICRO-START INT'L CO.,LTD.

Link to the Future

Title: USB Front Side-JUSB5		
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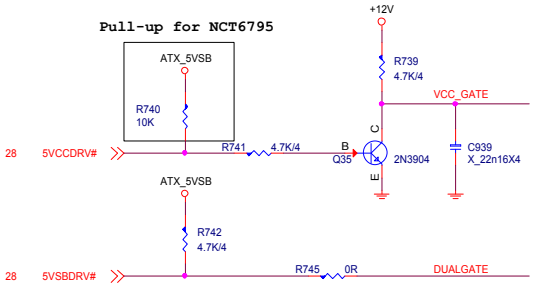
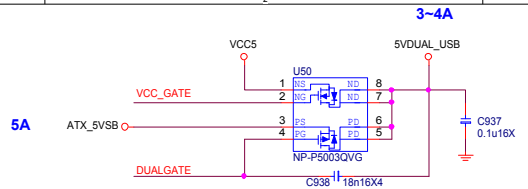
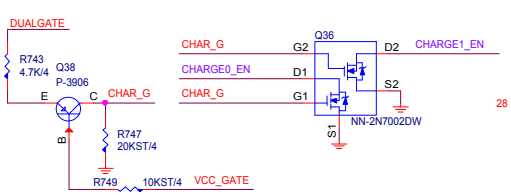
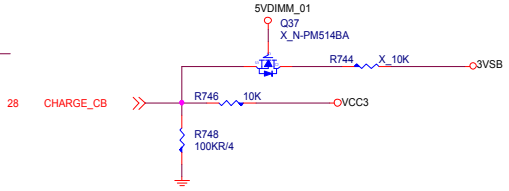
5VDUAL_USB



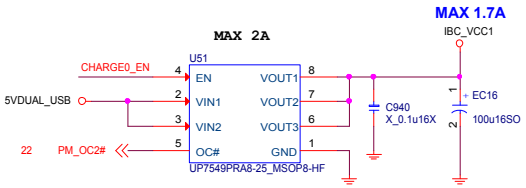


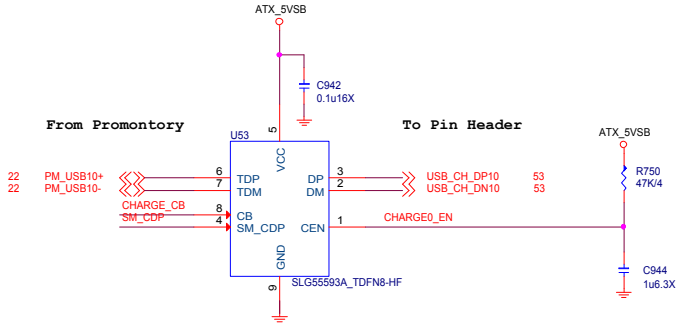
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



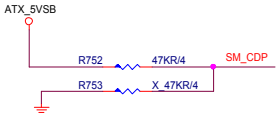


USB POWER PORT 0 For USB Charging

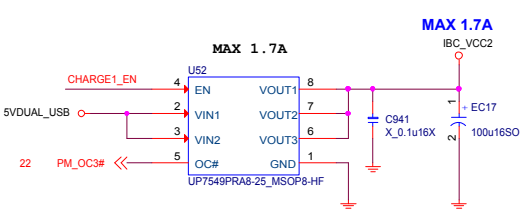


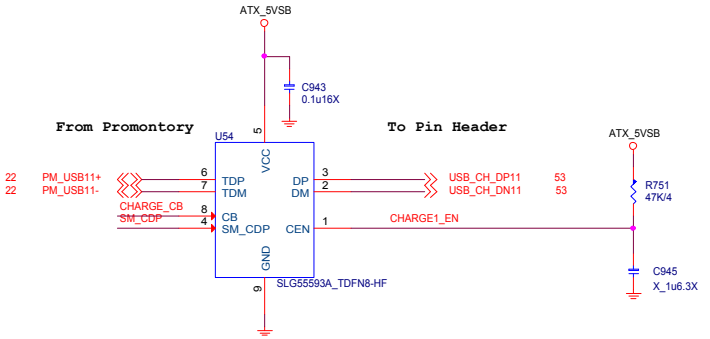


I98-555930C-SF9



USB POWER PORT 1 For USB Charging





I98-555930C-SF9

MICRO-STAR INT'L CO.,LTD.

Title: USB Charger

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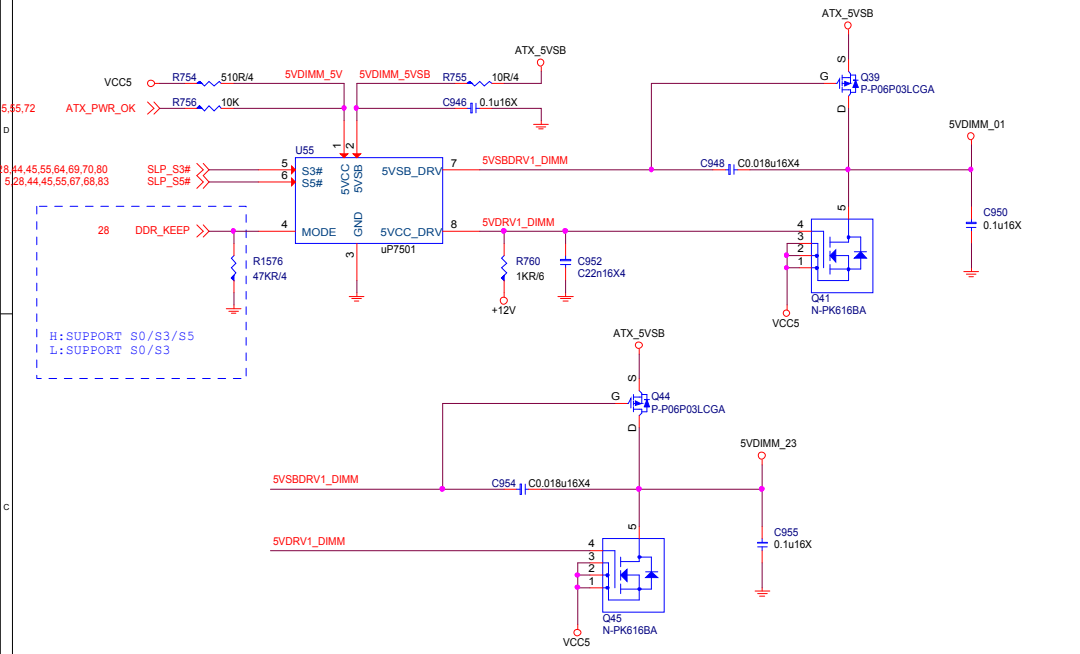
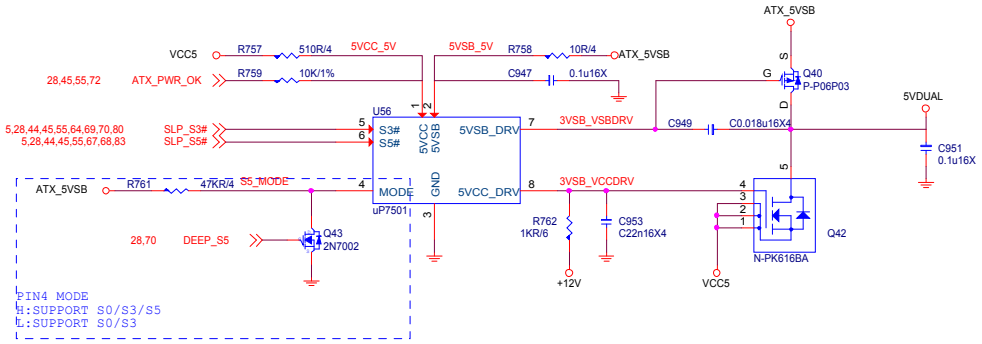
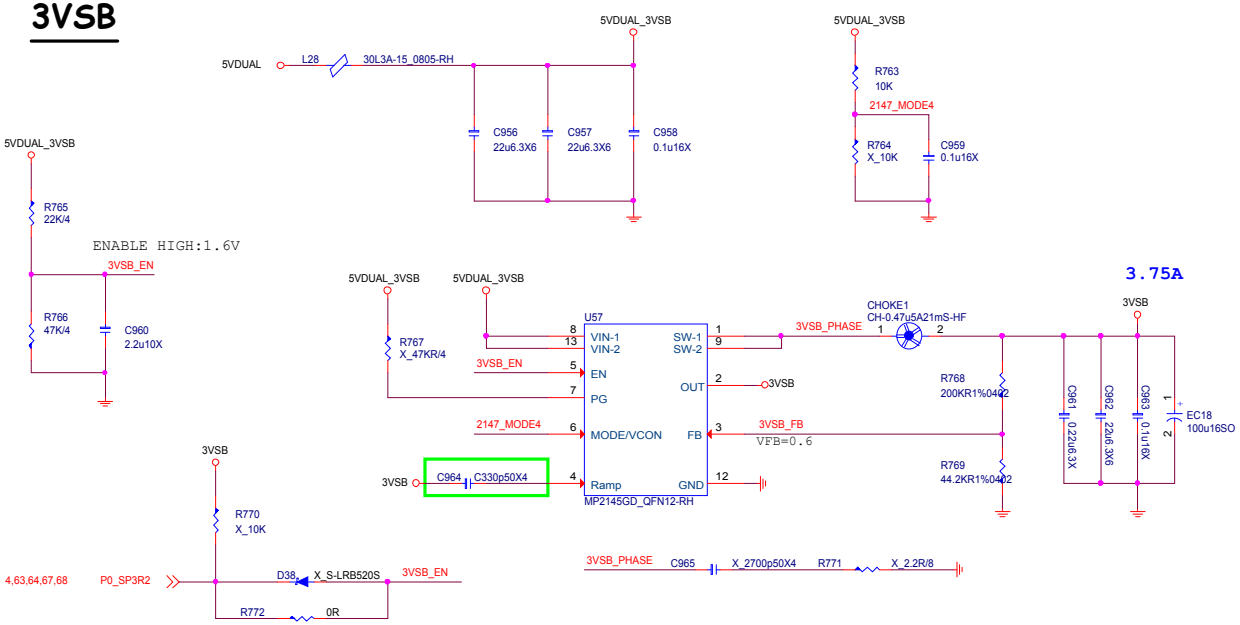
5VDIMM FOR DDR



5VDUAL For 3VSB、CPU 1.8V 、VDDP



3VSB



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Title	ACPI uPI-5VDIMM&3VSB	
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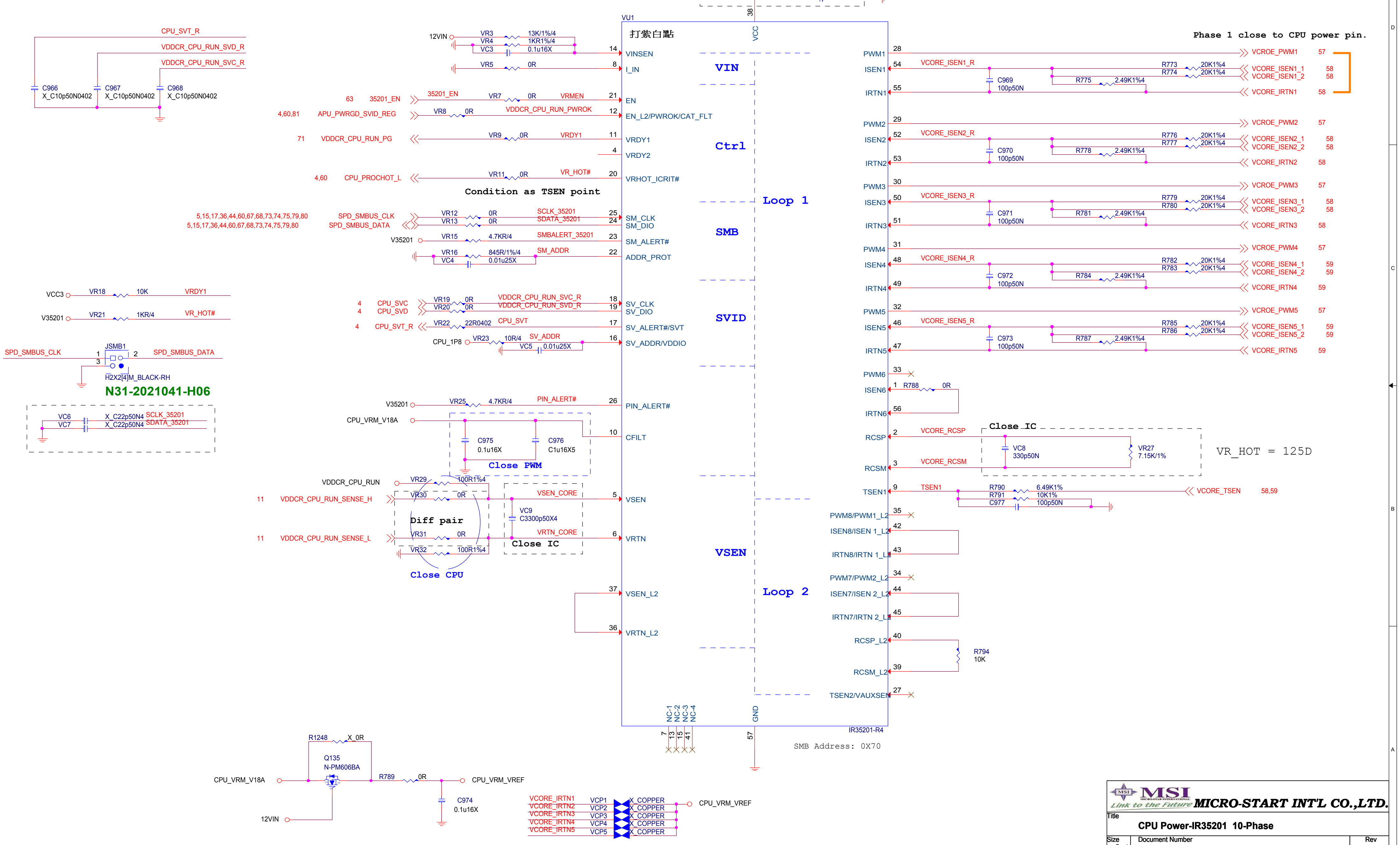
Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore: ICC Max 240A
LL: 0.3 mohm
OCP: 400A



Close IC
Phase 1 close to CPU power pin.
VU1
打紫白點
VIN
Ctrl
Loop 1
SMB
SVID
VSEN
Loop 2
Condition as TSEN point
Close PWM
Diff pair
Close CPU
VR_HOT = 125D
N31-2021041-H06
JSMB1
H2X2[4]M_BLACK-RH
VINSEN
I_IN
EN
EN_L2/PWROK/CAT_FLT
VRDY1
VRDY2
VRHOT_ICRIT#
SM_CLK
SM_DIO
SM_ALERT#
ADDR_PROT
SV_CLK
SV_DIO
SV_ALERT#/SVT
SV_ADDR/VDDIO
PIN_ALERT#
CFILT
VSEN
VRTN
VSEN_L2
VRTN_L2
PWM1
ISEN1
IRTN1
PWM2
ISEN2
IRTN2
PWM3
ISEN3
IRTN3
PWM4
ISEN4
IRTN4
PWM5
ISEN5
IRTN5
PWM6
ISEN6
IRTN6
RCSP
RCSM
TSEN1
PWM8/PWM1_L2
ISEN8/ISEN 1_L2
IRTN8/IRTN 1_L2
PWM7/PWM2_L2
ISEN7/ISEN 2_L2
IRTN7/IRTN 2_L2
RCSP_L2
RCSM_L2
TSEN2/VAUXSEN
IR35201-R4
SMB Address: 0X70
Q135
N-PM606BA
CPU_VRM_V18A
CPU_VRM_VREF
12VIN

MSI Link to the Future
MICRO-START INT'L CO.,LTD.
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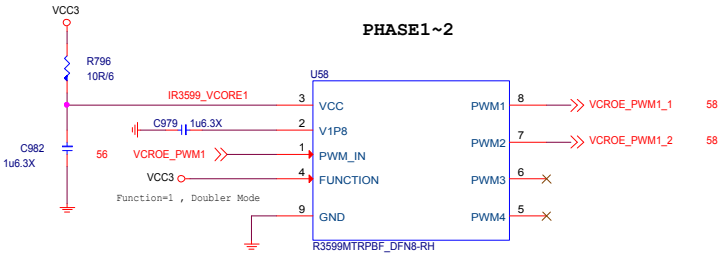
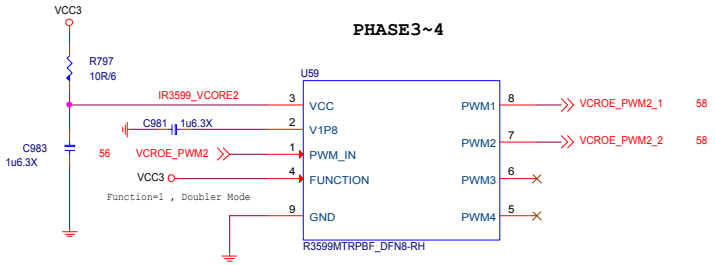
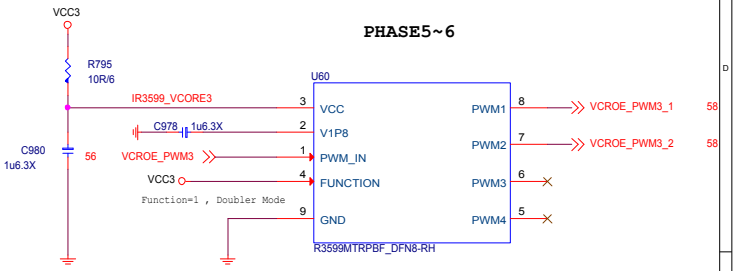
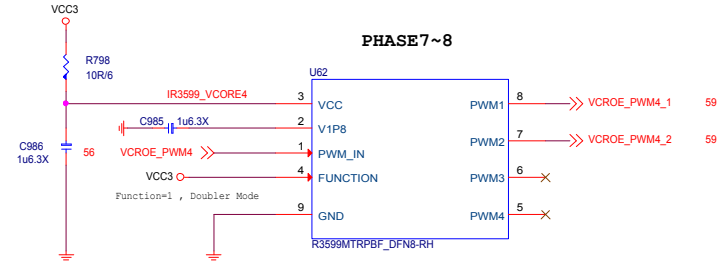
CPU_CORE Driver IC

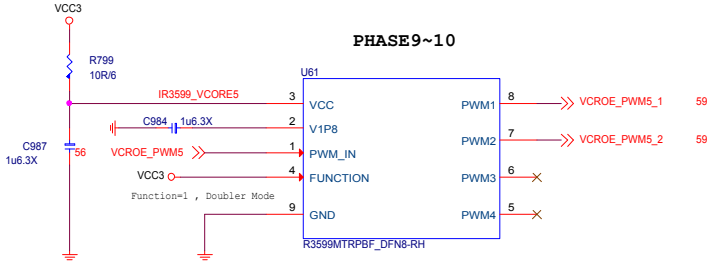
VCORE Double 10-PHASE











MSI MICRO-STAR INT'L CO.,LTD.

Link to the Future

Title: CPU Power IR3599		
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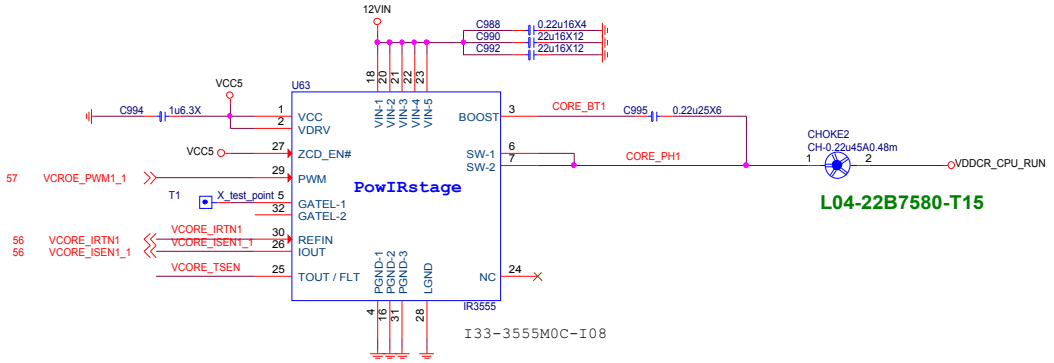

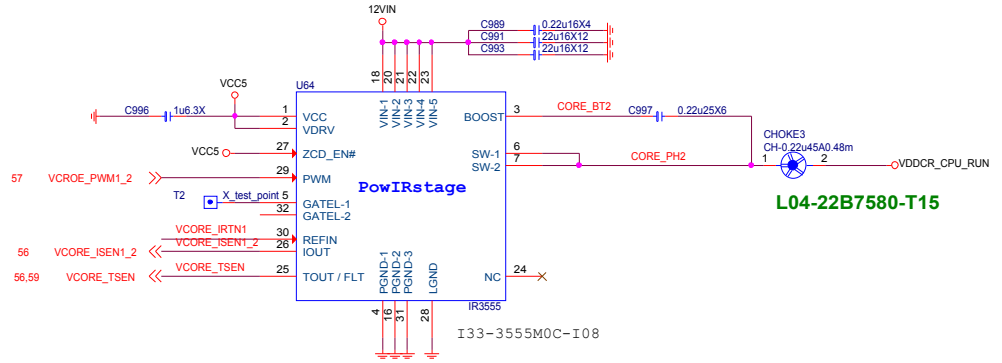

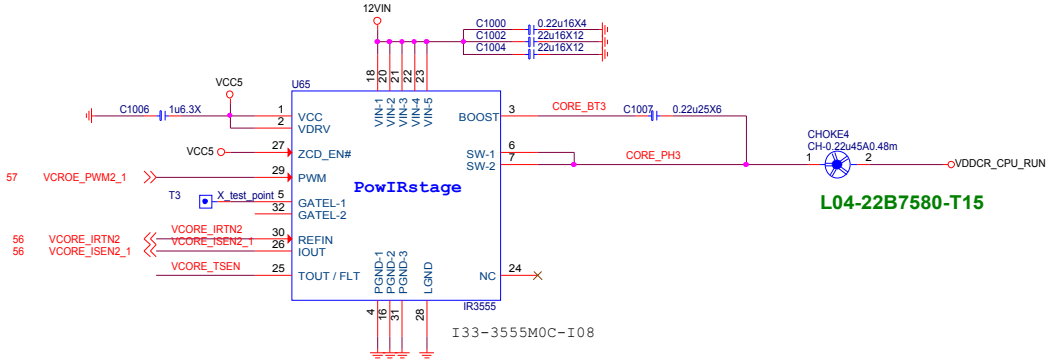

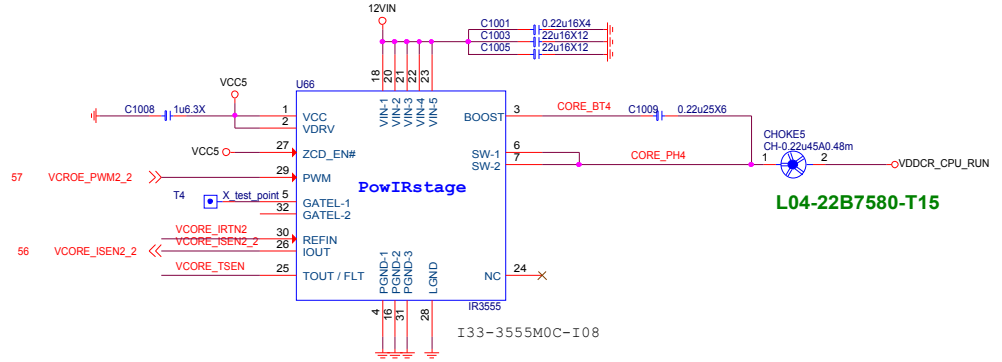

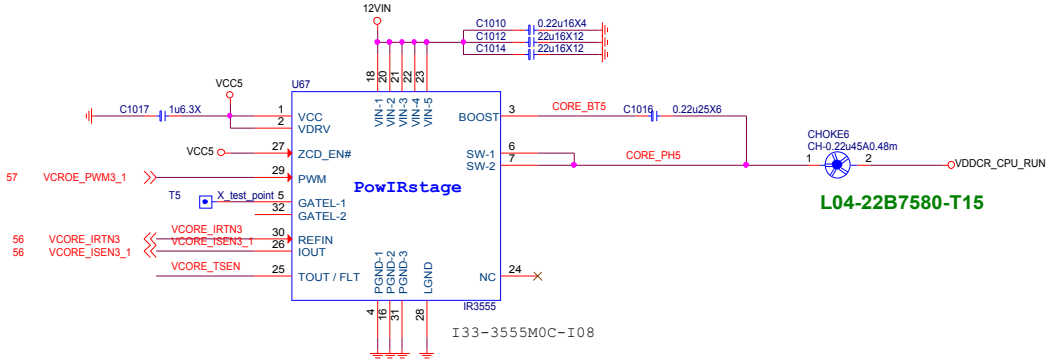

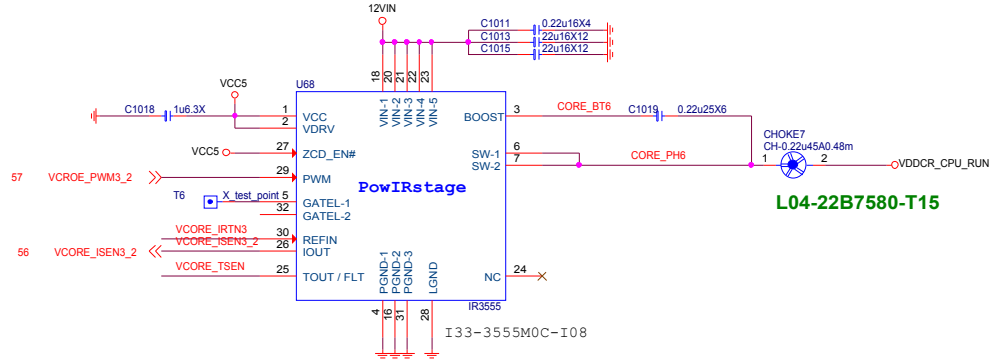

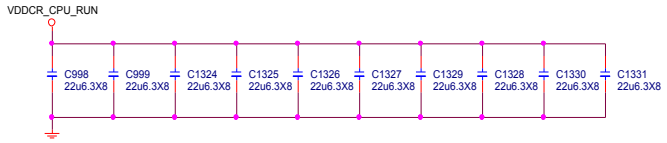

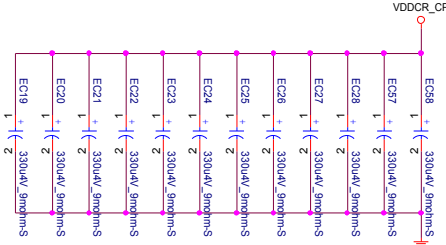

MICRO-START INT'L CO.,LTD.

Title: CPU Power Phase 1-6

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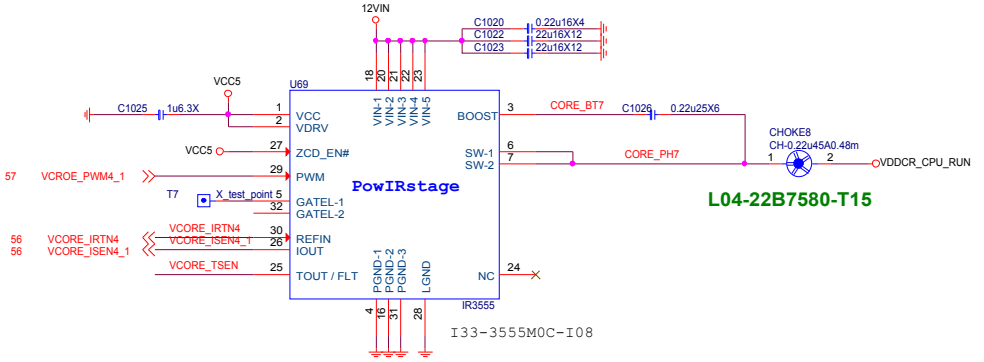

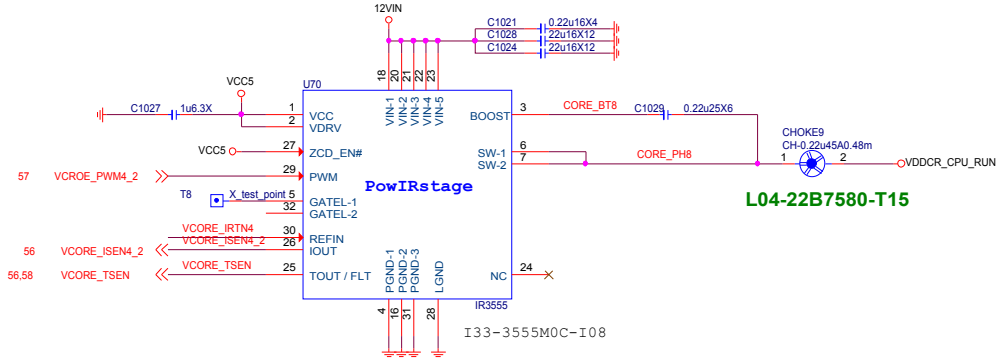

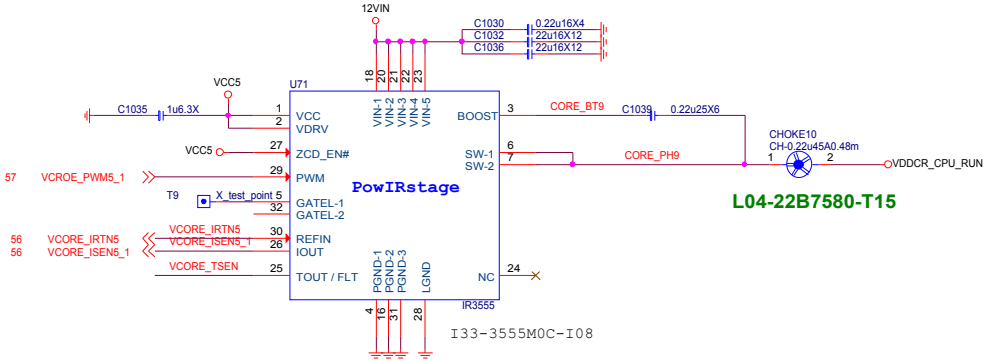

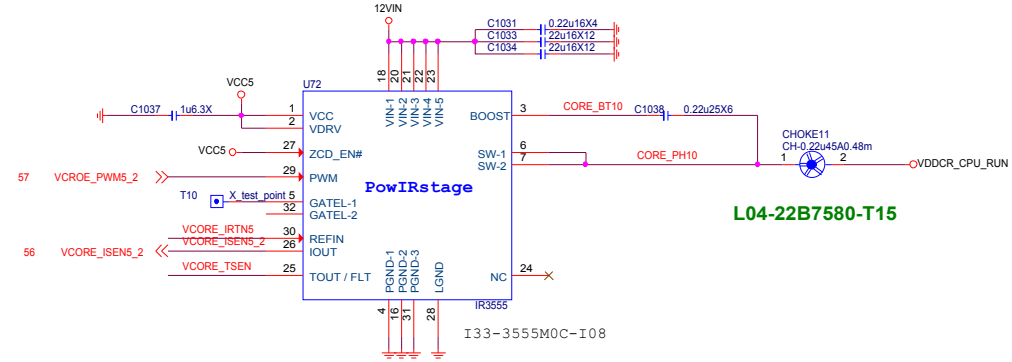

MICRO-START INT'L CO.,LTD.

Link to the Future

Title: CPU Power Phase 7-10		
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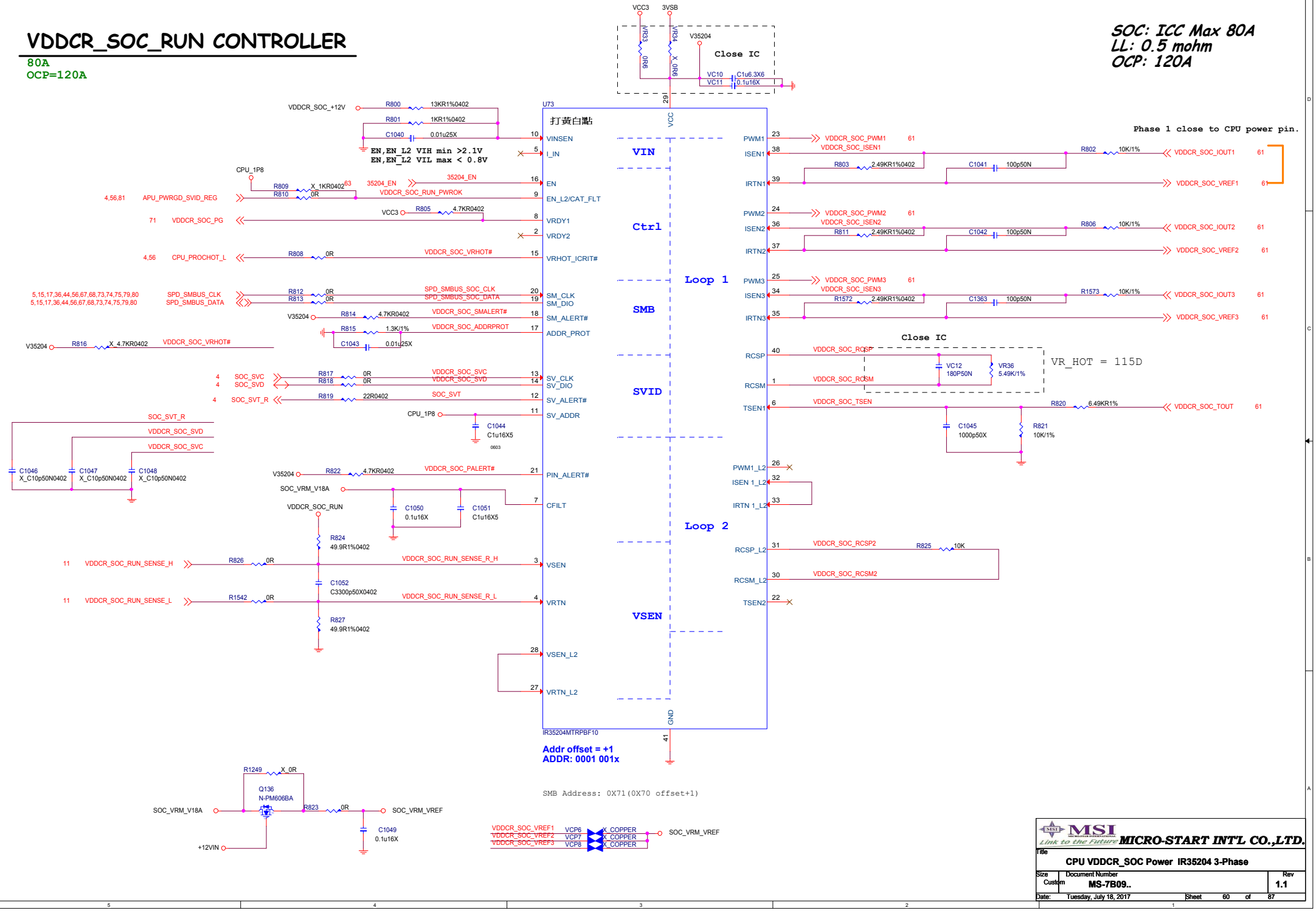
VDDCR_SOC_RUN CONTROLLER

80A
OCP=120A

SOC: ICC Max 80A
LL: 0.5 mohm
OCP: 120A



MICRO-START INT'L CO.,LTD.

Title	CPU VDDCR_SOC Power IR35204 3-Phase	
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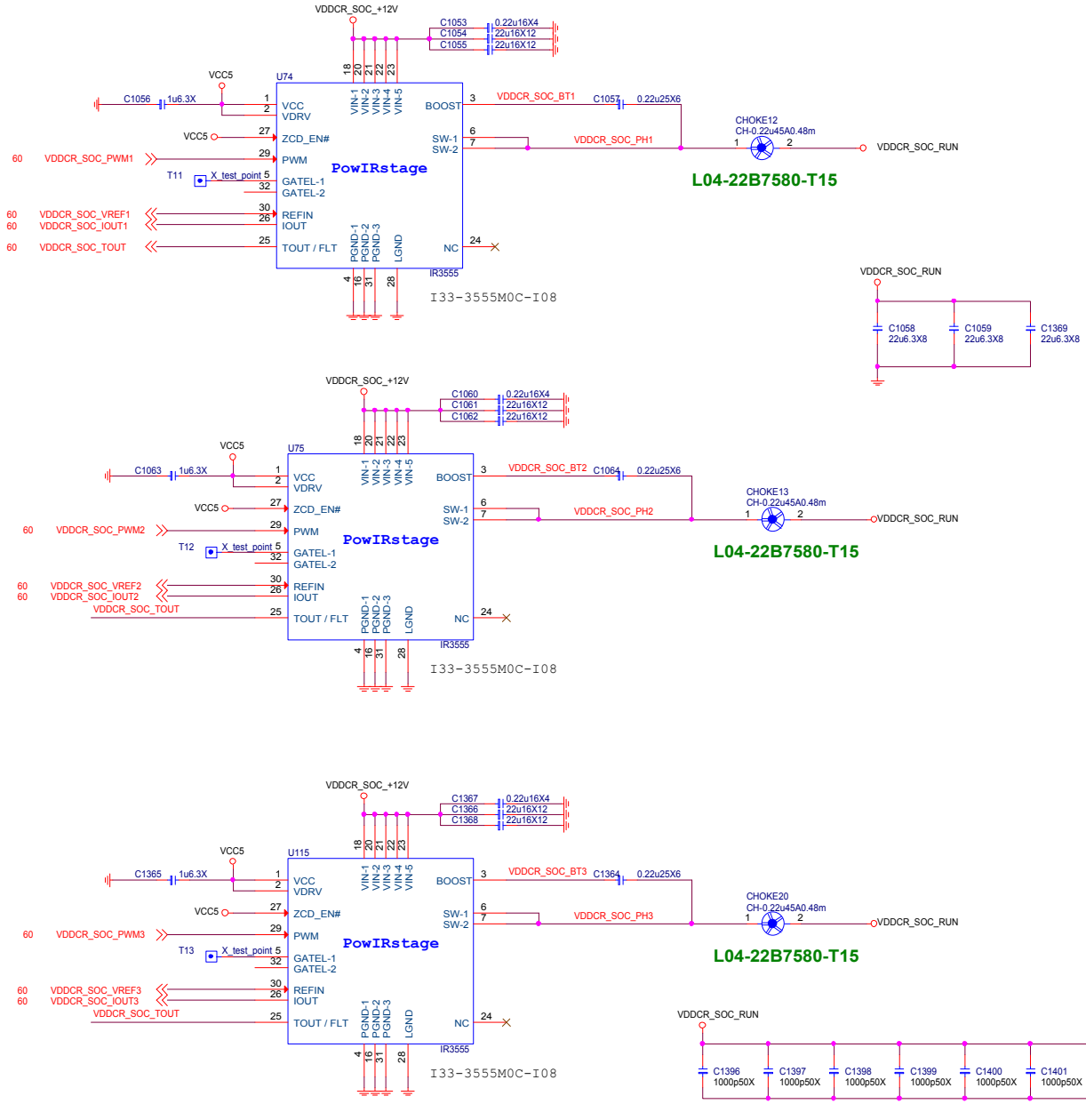
CPU_SOC Driver+MOS IC

3-PHASE



MICRO-START INT'L CO.,LTD.

Title	CPU VDDCR_SOC Power IR3555 1-3	
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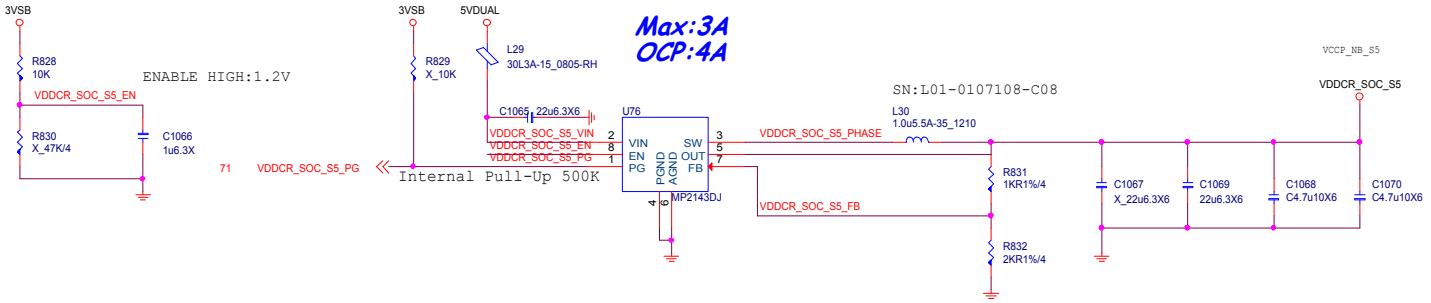
VDDCR_SOC_S5 0.9V

2A



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Link to the Future

Title: CPU Power VDDCR_SOC_S5		
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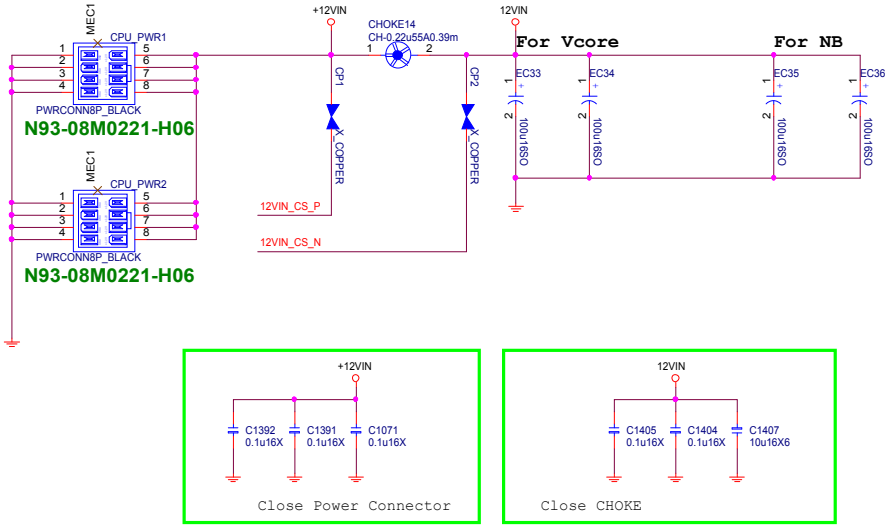
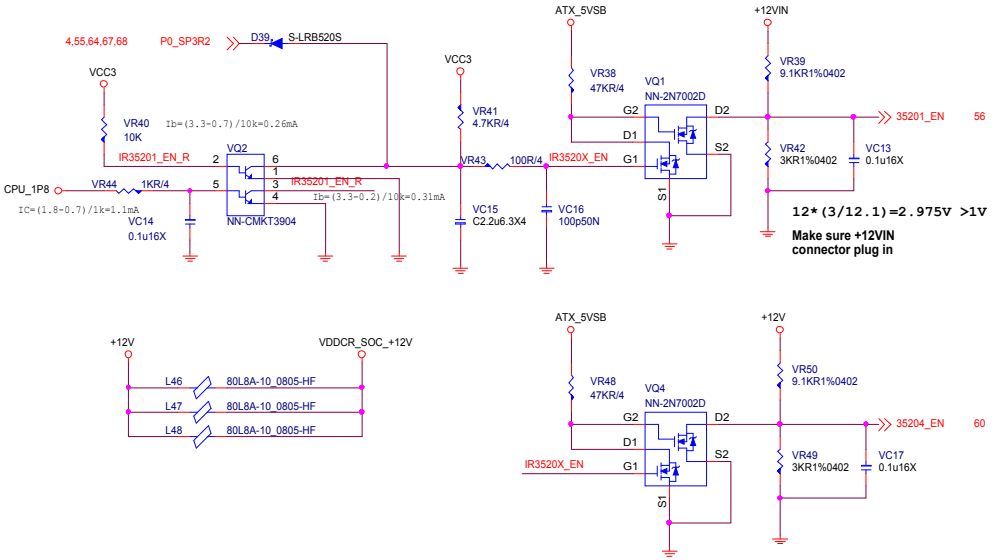
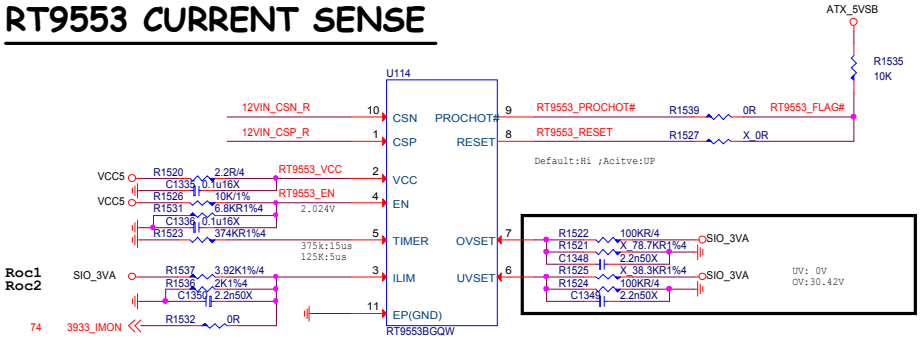
CPU POWER CONNECTOR

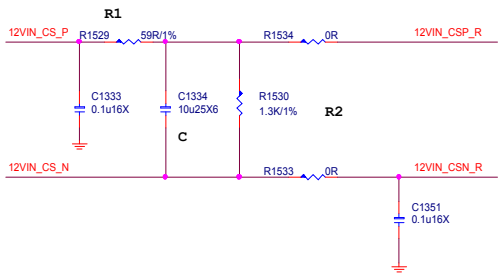


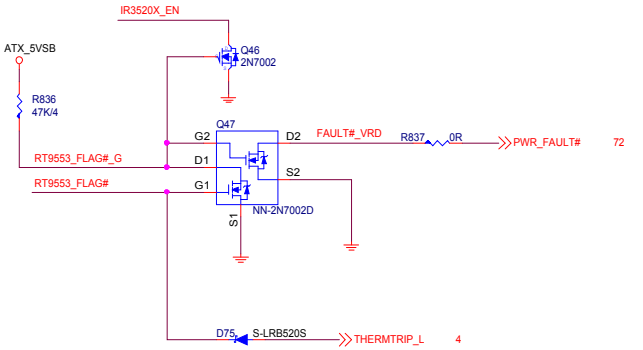
VRM_Enable circuit



RT9553 CURRENT SENSE







OCP:36A (Without CPU_SOC PWR)
Real OCP:45~59A

I3933_imon*[R17*R18/(R17+R18)]= Istep* Rdcr*100
I3933_imon= 10uA/step
Istep=4.785A

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Title: CPU Power Connector/RT9553B		
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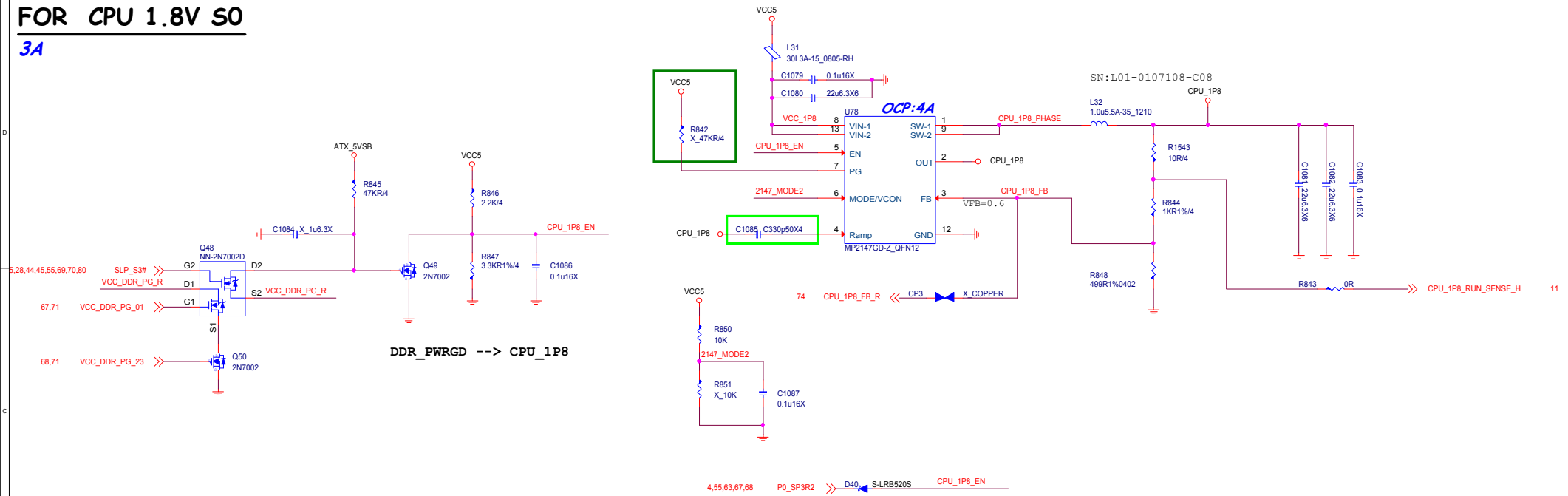
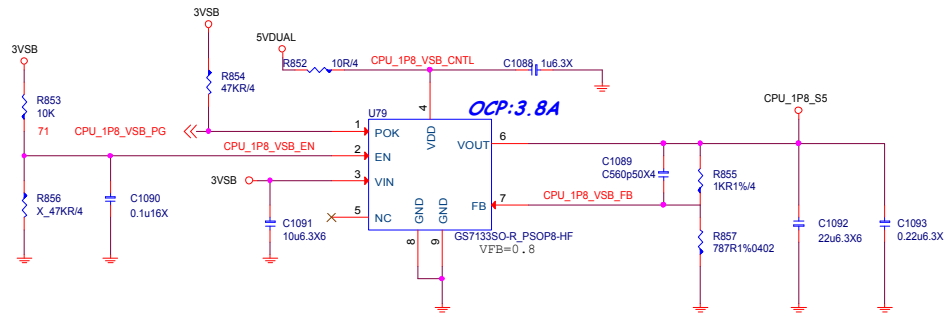
FOR CPU 1.8V S0

3A



FOR CPU 1.8V S5

1A



AVL: I31-3730S02-N62

MSI MICRO-STAR INTERNATIONAL
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MICRO-START INT'L CO.,LTD.

Title	CPU Power 1P8V-MP2147	
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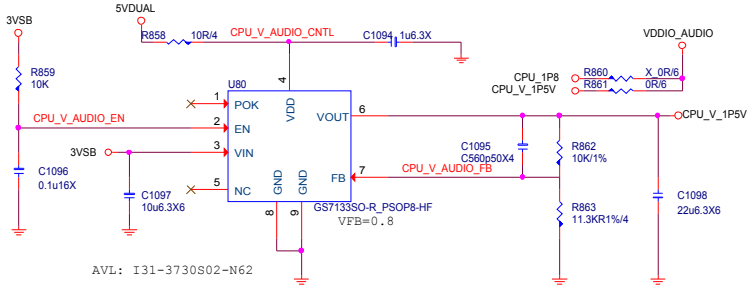
VDDIO_AUDIO Circuit

1.5V
0.25A



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: CPU Power Audio-GS7133		
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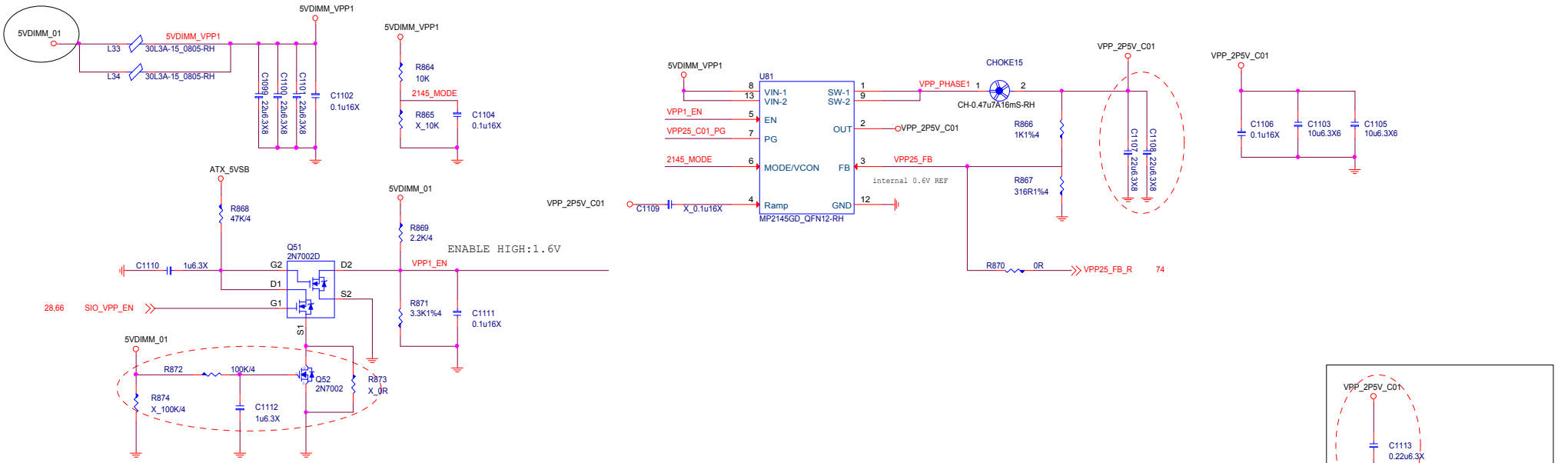
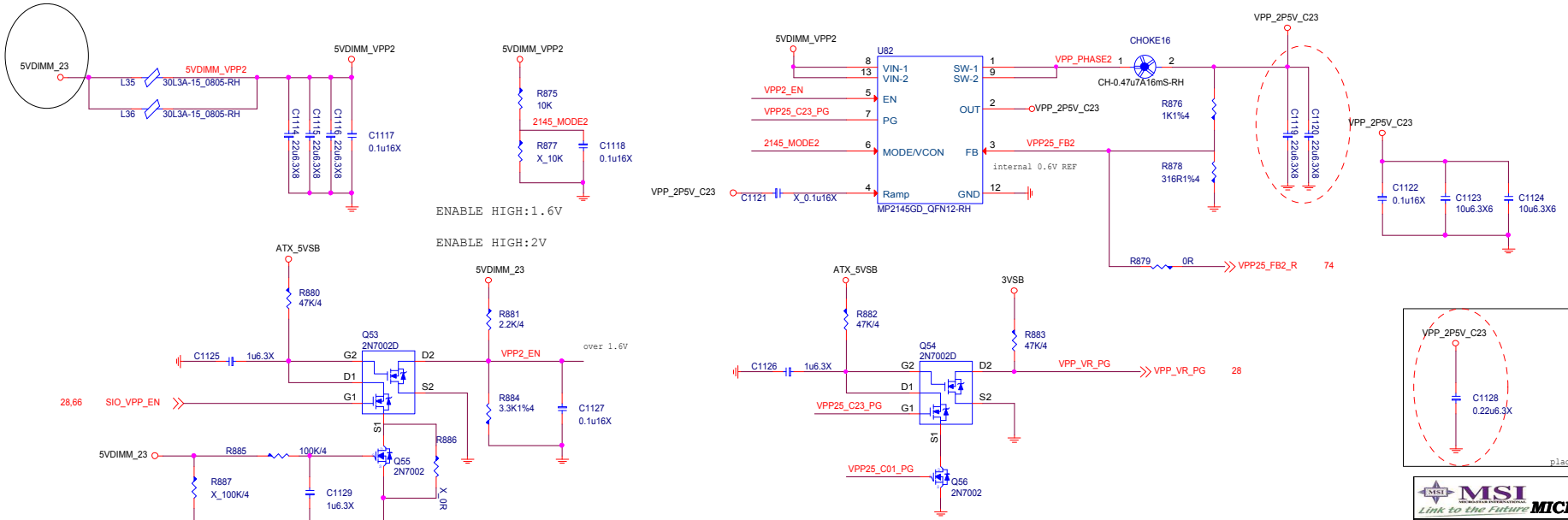
4DIMM :2.24A FOR DDR VPP2.5V

2.5+0.25/-0.125V
JESD79 DDR4 max 3V





MICRO-START INT'L CO.,LTD.

Title	DDR PWR VPP25/VTT-MP2145	
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DDR Power1-PV4210-2-Phase

DDR4_1.2V 15A+9.5A+1.2A=26A

15A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCP: 50A

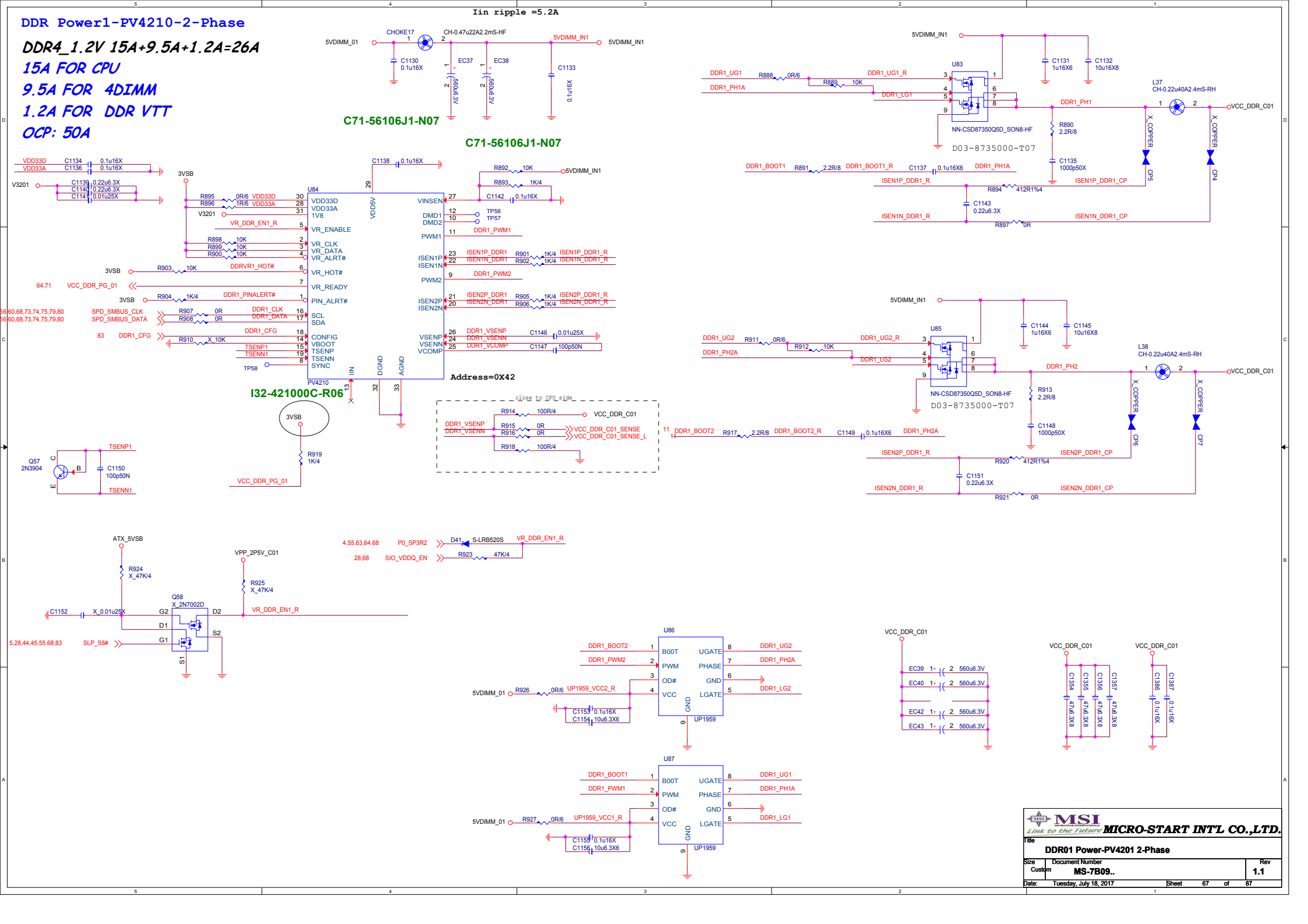
Iin ripple =5.2A

C71-56106J1-N07

C71-56106J1-N07

I32-421000C-R06

Address=0X42



Title	DDR01 Power-PV4201 2-Phase
Size	Custom
Document Number	MS-7B09..
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Date:	Tuesday, July 18, 2017
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MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

DDR Power1-PV4210-2-Phase

DDR4_1.2V 15A+9.5A+1.2A=26A

15A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCP: 50A

Iin ripple =5.2A

Table6#=1.21V

I32-421000C-R06

Address=0X44

PROC_ID1	Config	CPU TYPE
1	133K	SKX-X (VR13) (SVID)
0	110K	KBL-X(IMVP8) (non SVID)

Title	DDR23 Power-PV4201 2-Phase
Size	Custom
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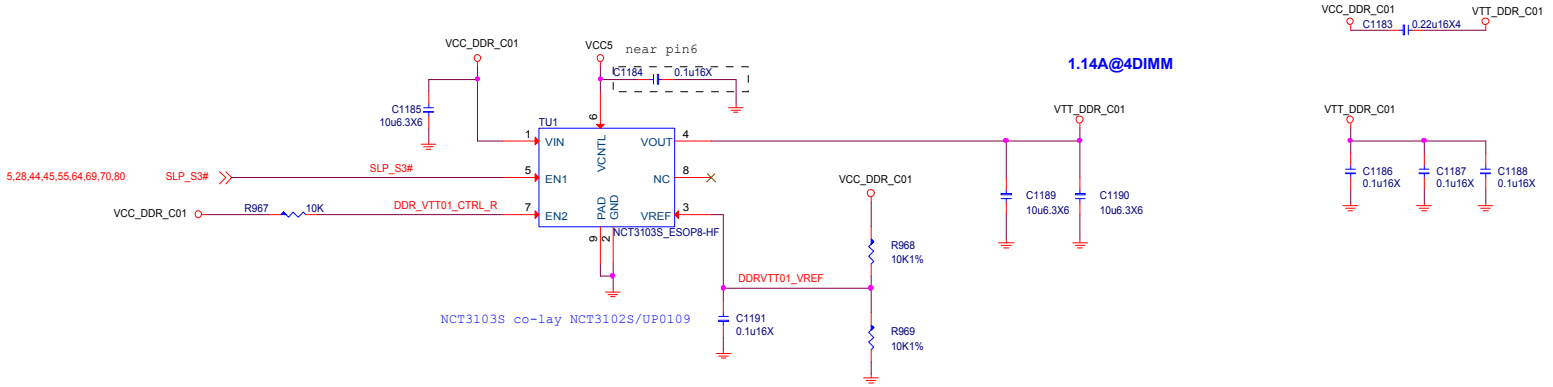
MICRO-START INT'L CO.,LTD.

DDR VTT Power

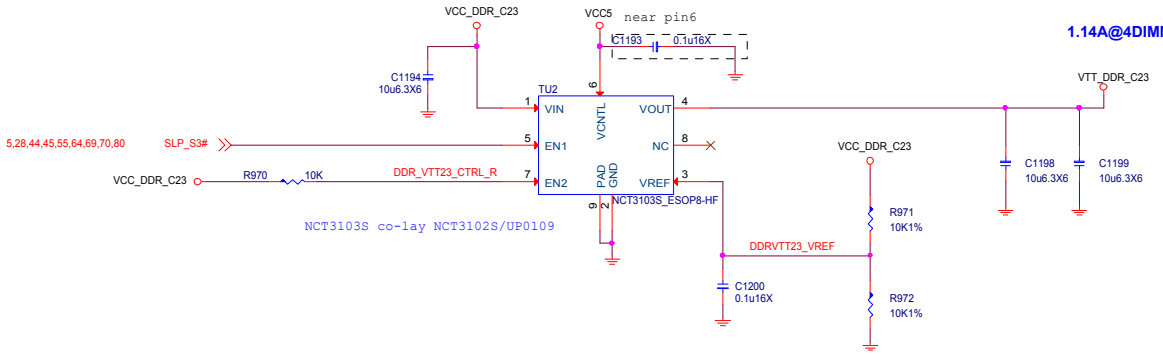
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



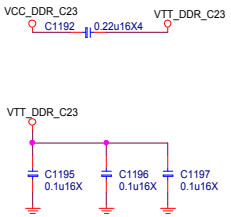
1.14A@4DIMM

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



1.14A@4DIMM



MSI MICRO-STAR INTERNATIONAL
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: VTTDDR		
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FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

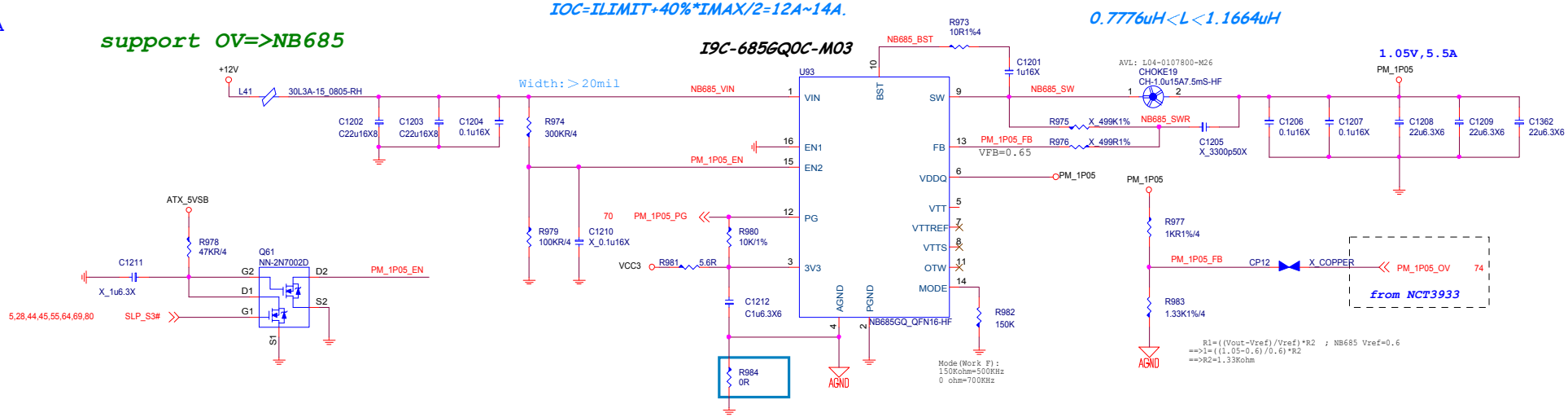
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH

support OV=>NB685

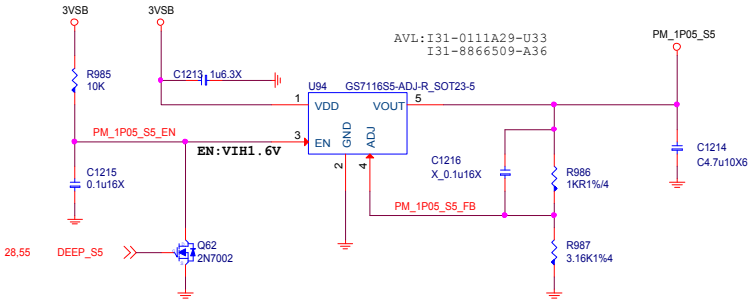
I9C-685GQ0C-M03

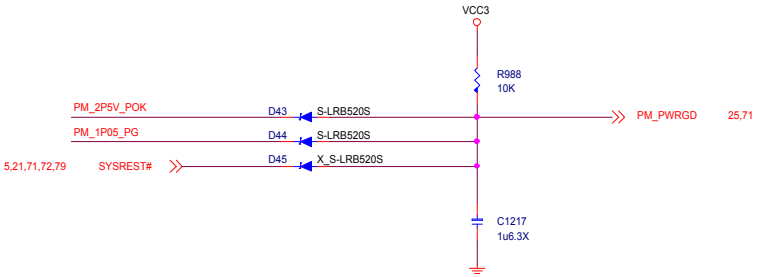
1.05V,5.5A



FOR Promontory 1.05V_S5

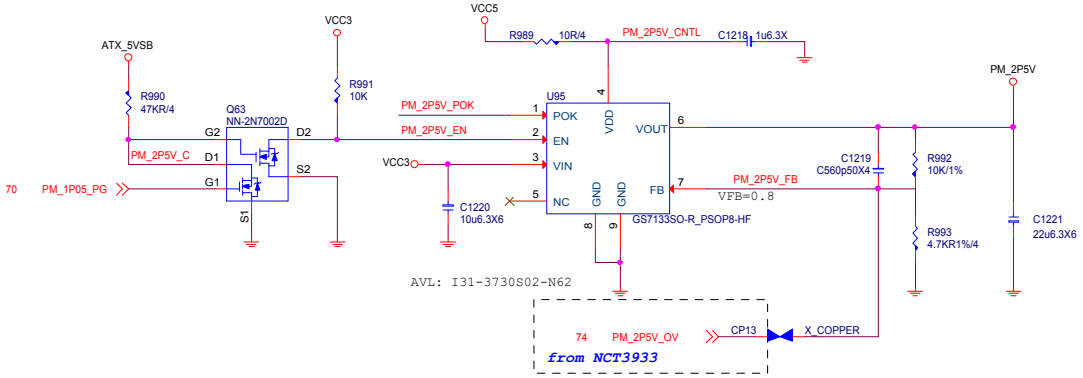
0.05A





Promontory-2.5V

2.5V; 900mA



MICRO-START INT'L CO.,LTD.
Link to the Future

Title	Promontory-NB685GQ-1.05V / GS7133-2.5V	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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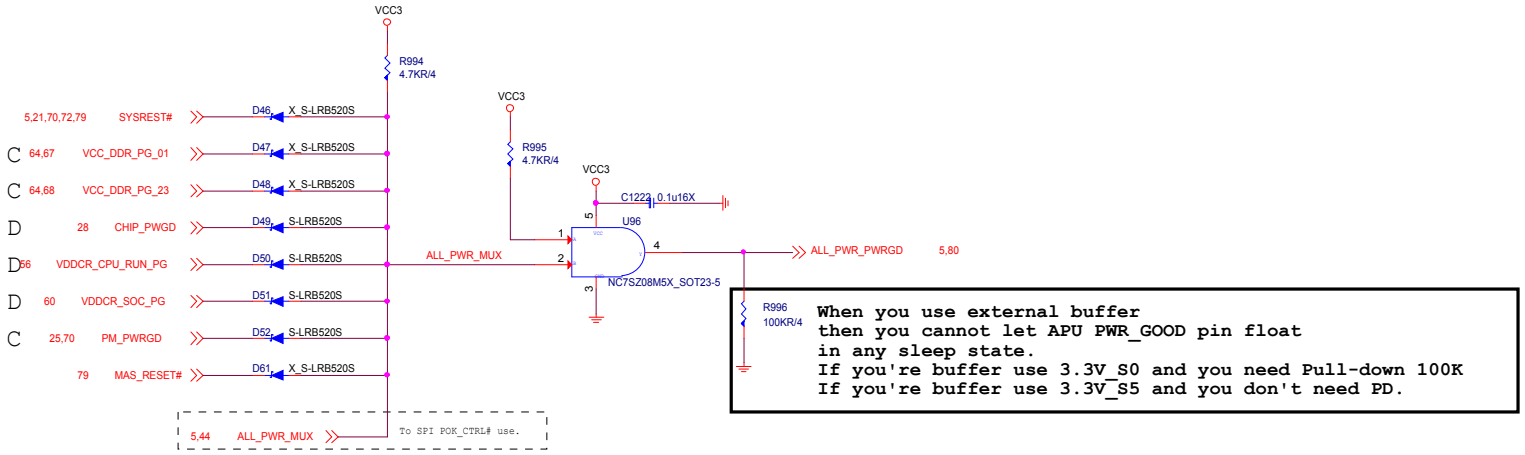
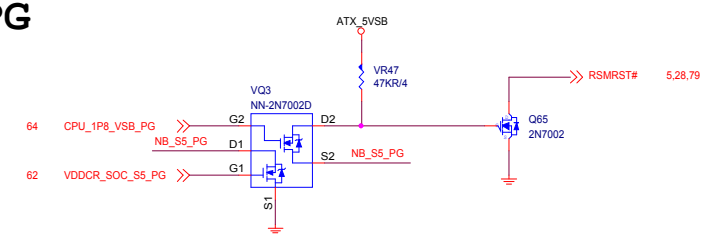
ALL POWER GOOD MUX



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: CPU Power Good		
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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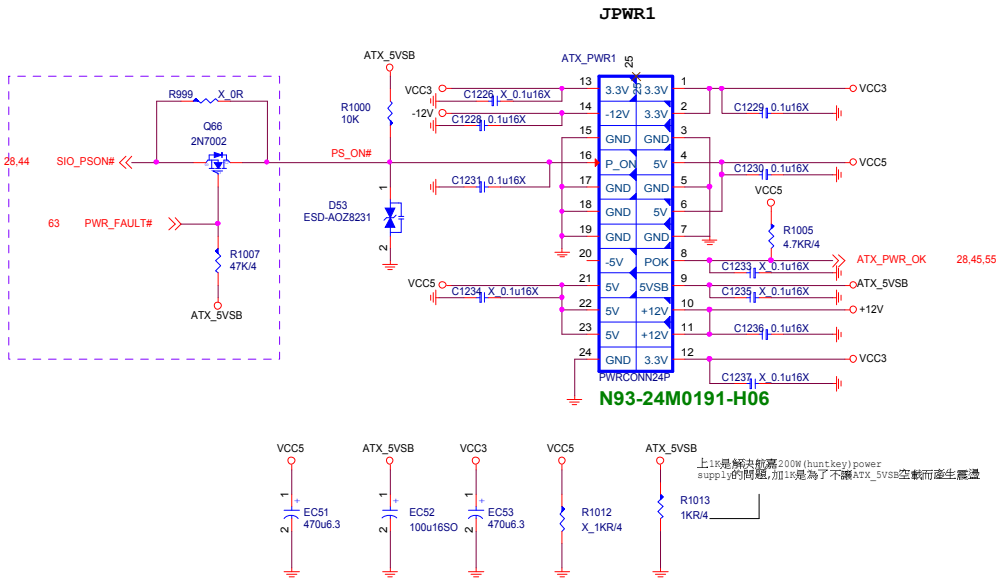
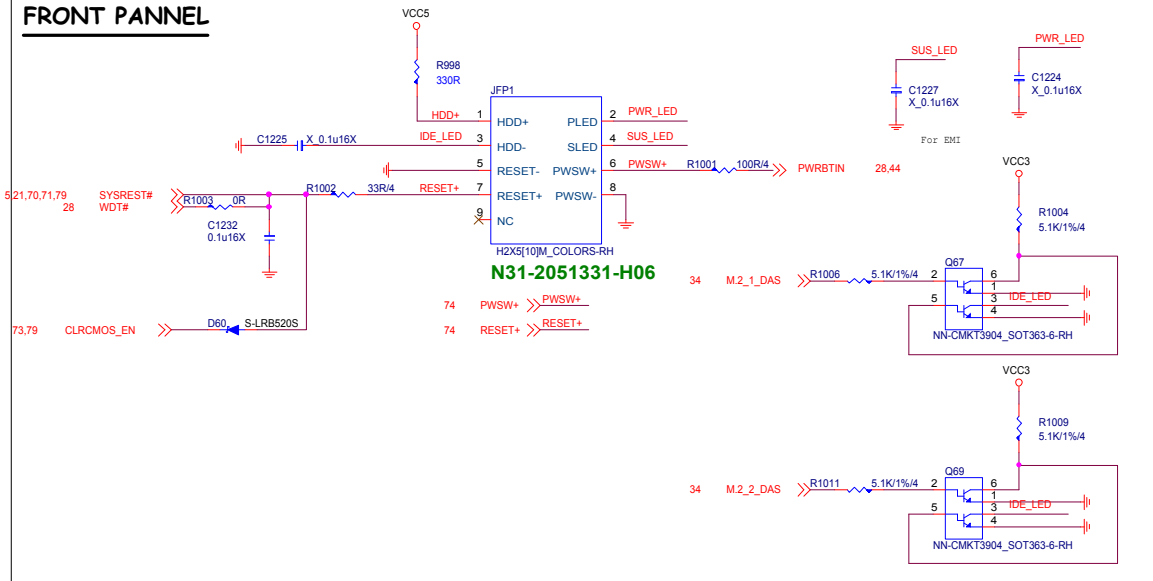
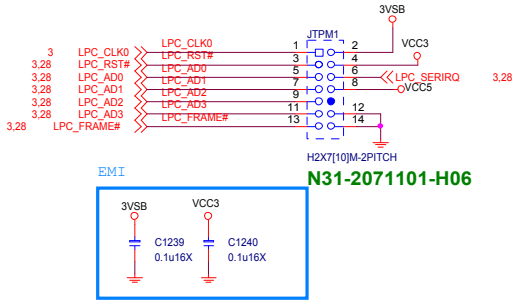
ATX POWER CONNECTOR



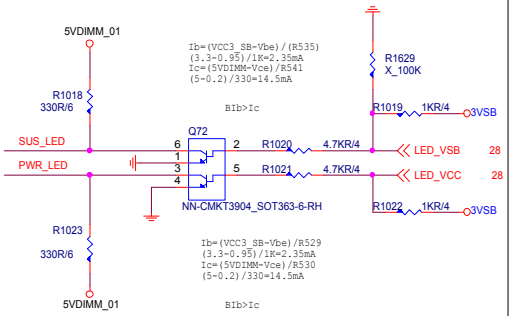
FRONT PANNEL

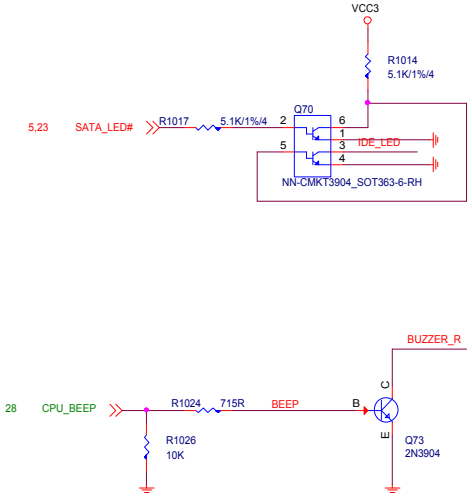


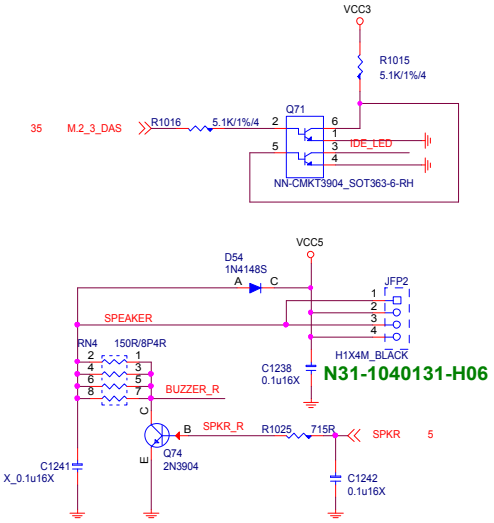
TPM



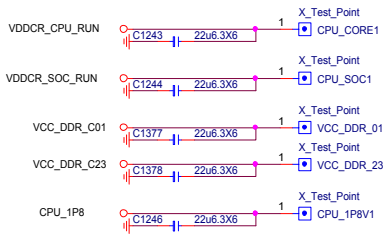
LED (for NCT6795D)



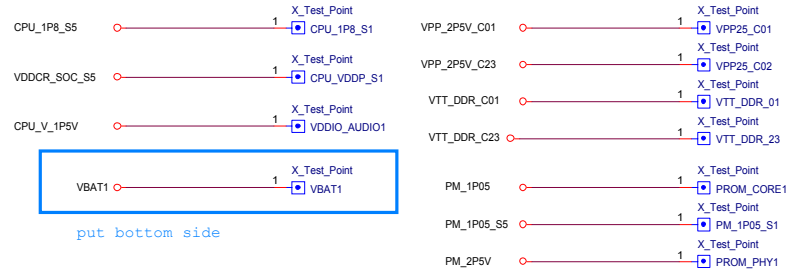




Voltage Mearsure Point



Close to output of IC



MICRO-START INT'L CO.,LTD.

Title	ATX/Front Panel	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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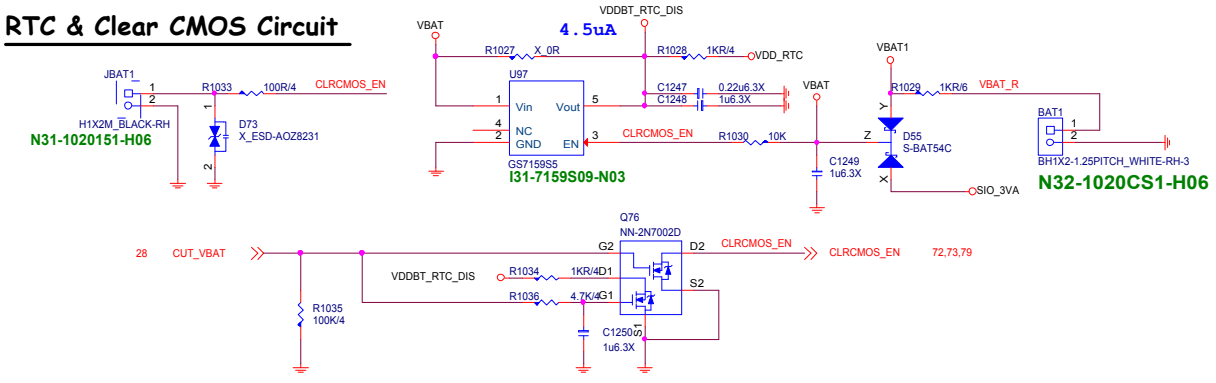
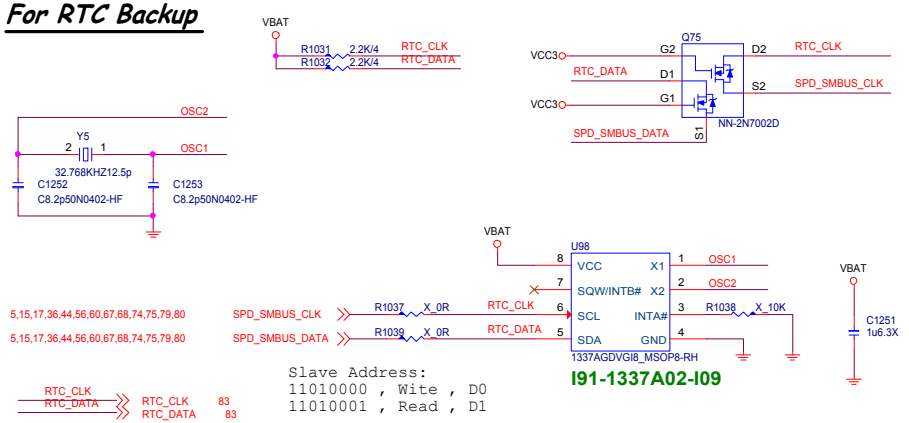
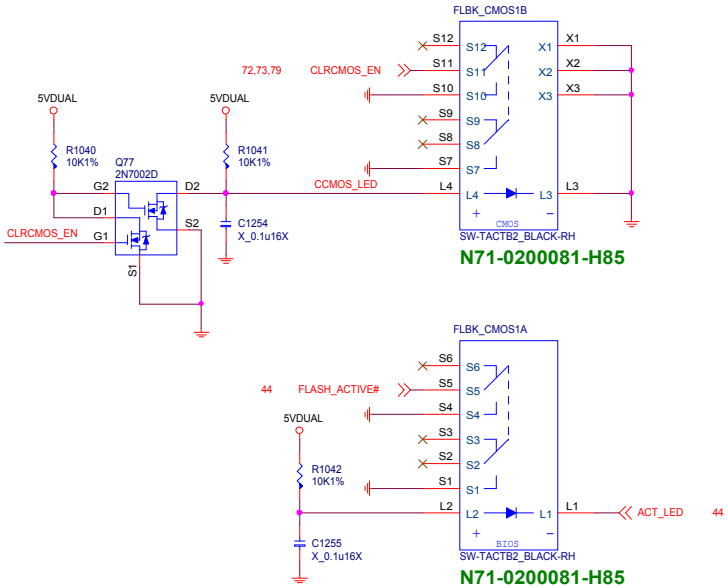
RTC & Clear CMOS Circuit



For RTC Backup



Clear CMOS&Flash Back button



MSI MICRO-STAR INT'L CO.,LTD.			
Title: RTC/Clear CMOS Circuit			
Size: Custom	Document Number: MS-7B09..		Rev: 1.1
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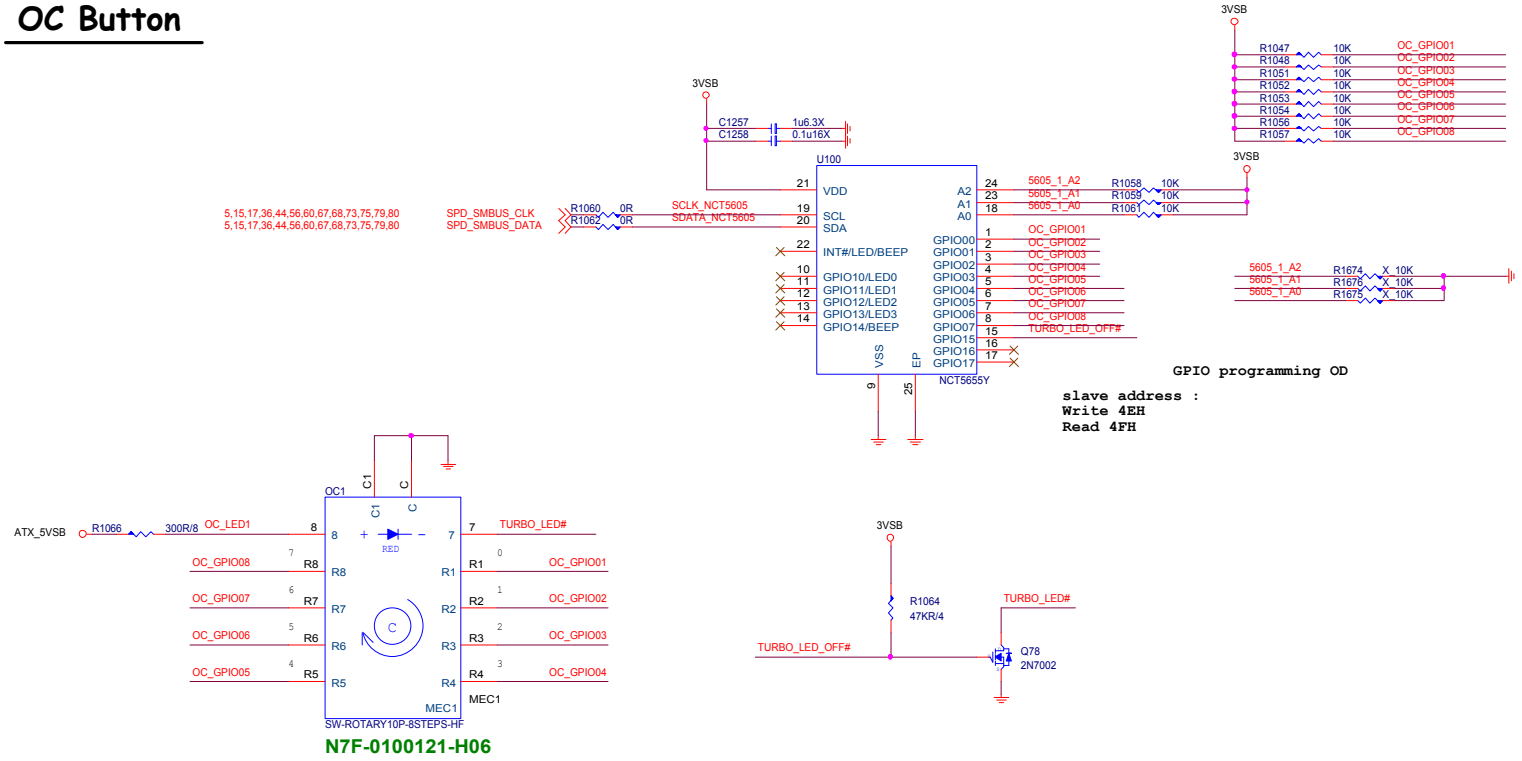
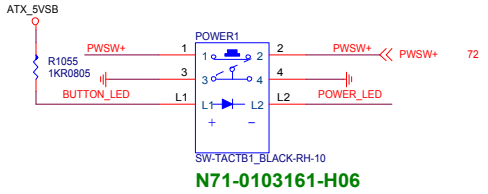
OC Button



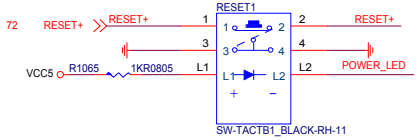
N7F-0100121-H06

Power ON Button

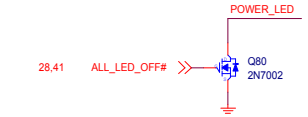


N71-0103161-H06

Reset Button



N71-0103151-H06

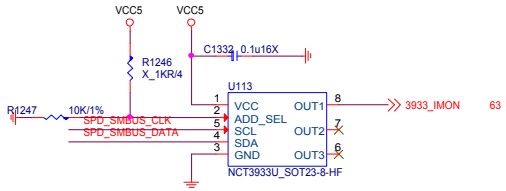


Over Voltage Control IC

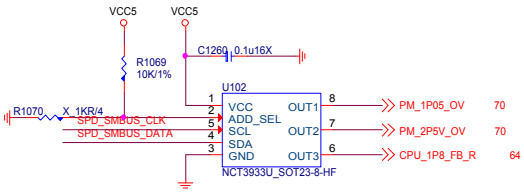
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

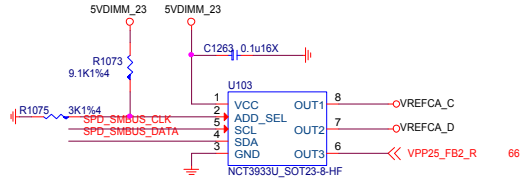
0x2A:RH=OPEN,RL=10K



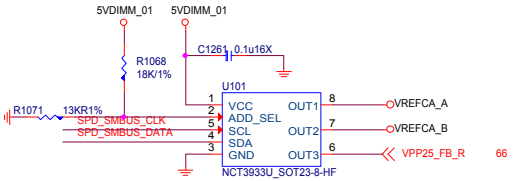
0x20:RH=10K,RL=OPEN



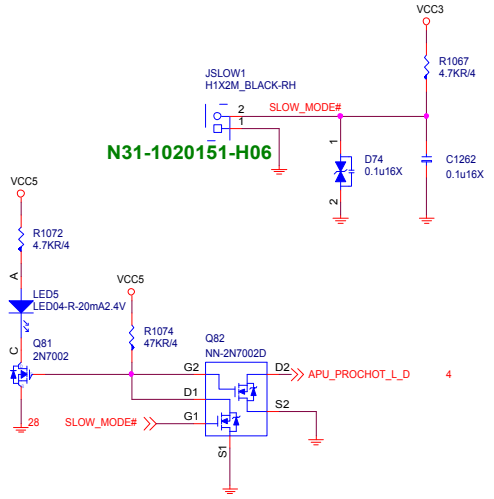
0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K



Slow Mode



N31-1020151-H06

MICRO-START INT'L CO.,LTD.

Link to the Future

Title	Button/OV Control/NCT3933	
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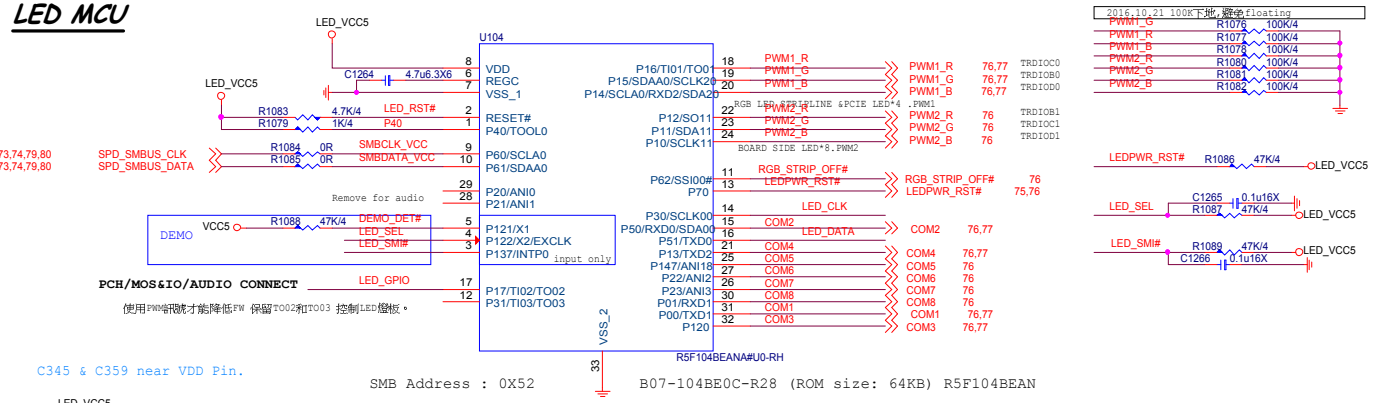
LED MCU

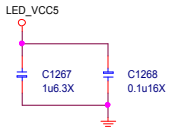


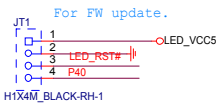
Control	Net Name	PWM USE	Connector
PCH	LED_GPIO	No Use	JPIPE_LED1
AUDIO Cover	LED_GPIO_01	No Use	JPIPE_LED2
MOS/IO cover	LED_GPIO_02	No Use	JPIPE_LED3
LED STRIPLINE	RGB_STRIP_OFF#	PWM1	JLED1
Board Side LED	COM1~8	PWM2	RGB LED
PCIE Side LED	COM1~4	PWM1	RGB LED

C345 & C359 near VDD Pin.

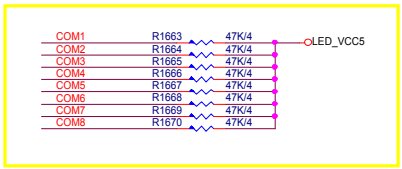
SMB Address : 0X52

B07-104BE0C-R28 (ROM size: 64KB) R5F104BEAN





1027 Remove JT1

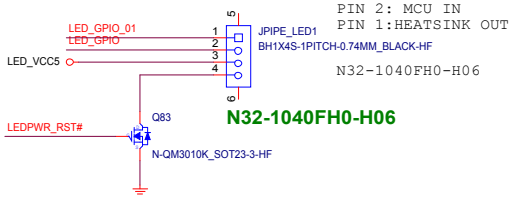


JPIPE:PIN1:output ,PIN2:input

1 PCH HEATSINK LED

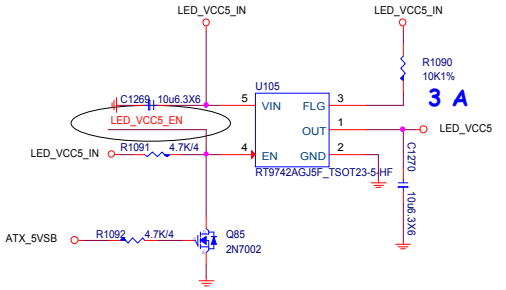
PCS LED*0.16W=W

PIN 2: MCU IN
PIN 1:HEATSINK OUT



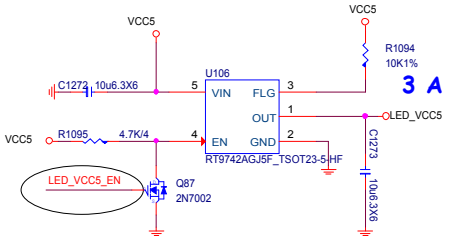
N32-1040FH0-H06

EXTERNAL POWER INPUT

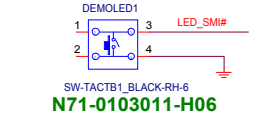


min 80mil.

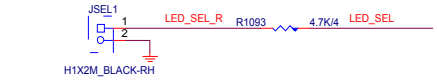
I36-9742A09-R11



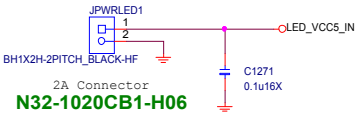
LED Demo Button



N71-0103011-H06



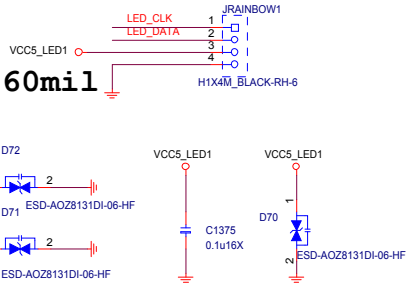
N31-1020151-H06



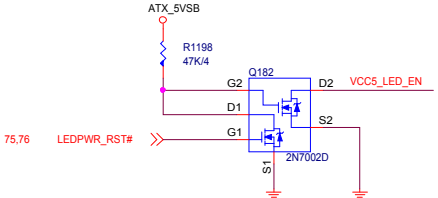
2A Connector

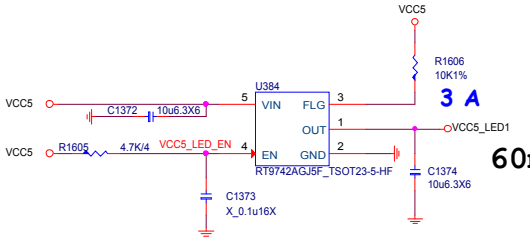
N32-1020CB1-H06

N32-1020CB1-H06



60mil

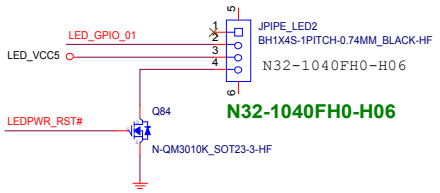




60mil

2 AUDIO/IO Cover LED

PCS LED*0.16W=W



N32-1040FH0-H06

JPIPE_LED3 no SPEC

MICRO-START INT'L CO.,LTD.

Title: LED MCU Control

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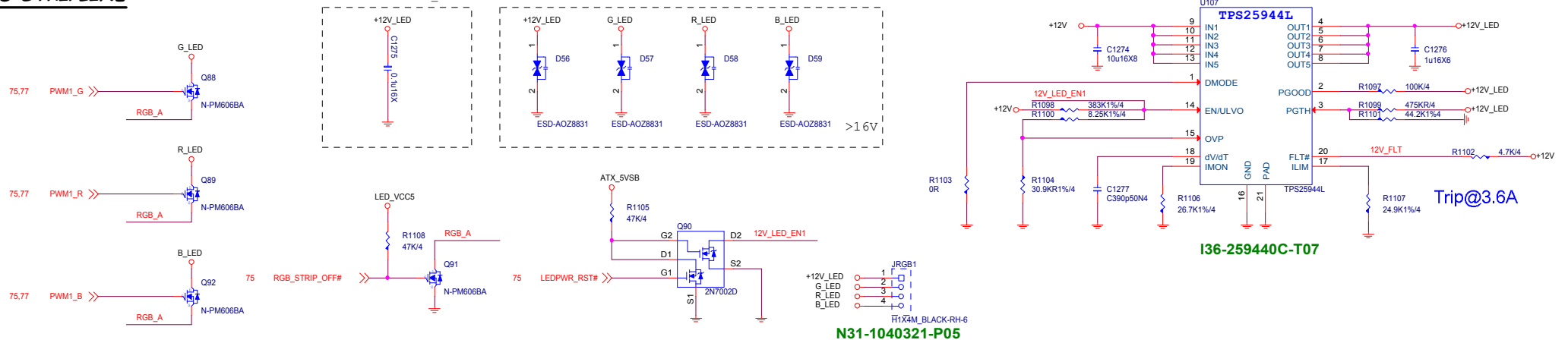
LED STRIPLINE

2016.07.06 only reserve now
2016.08.02 Add +12V_LED 0.1uF 2016.08.02 stuff ESD



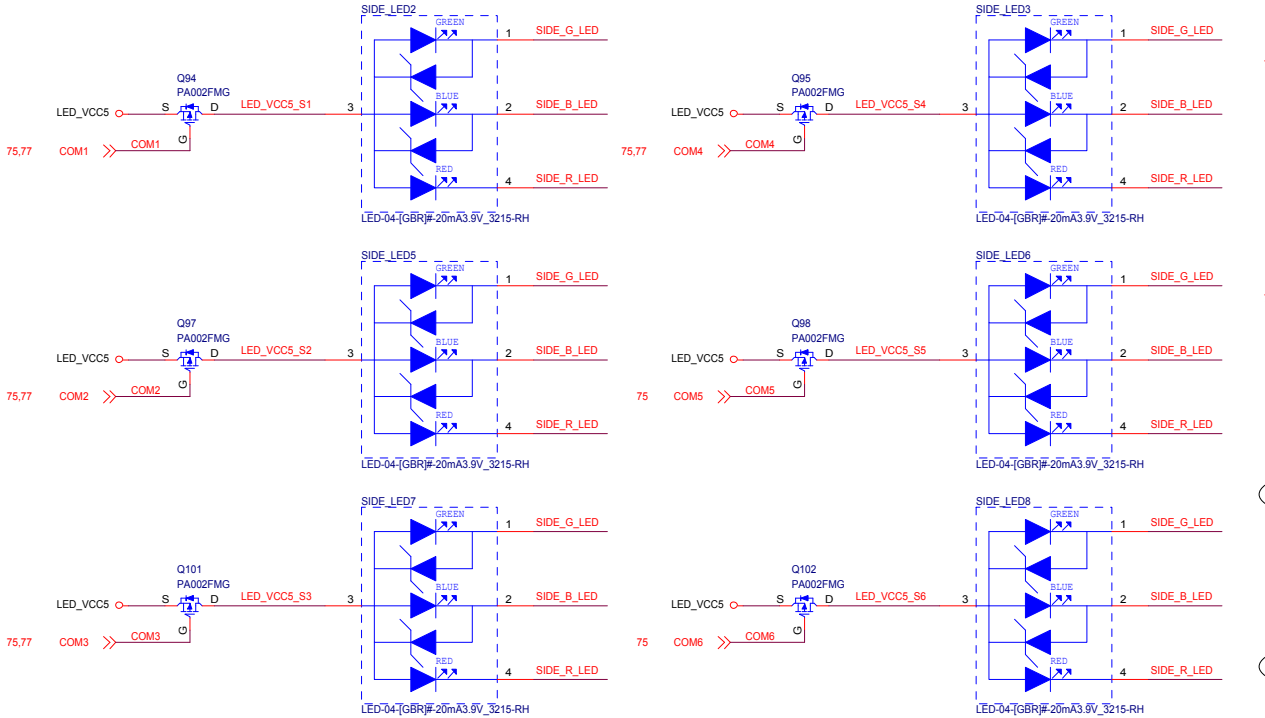
I36-259440C-T07

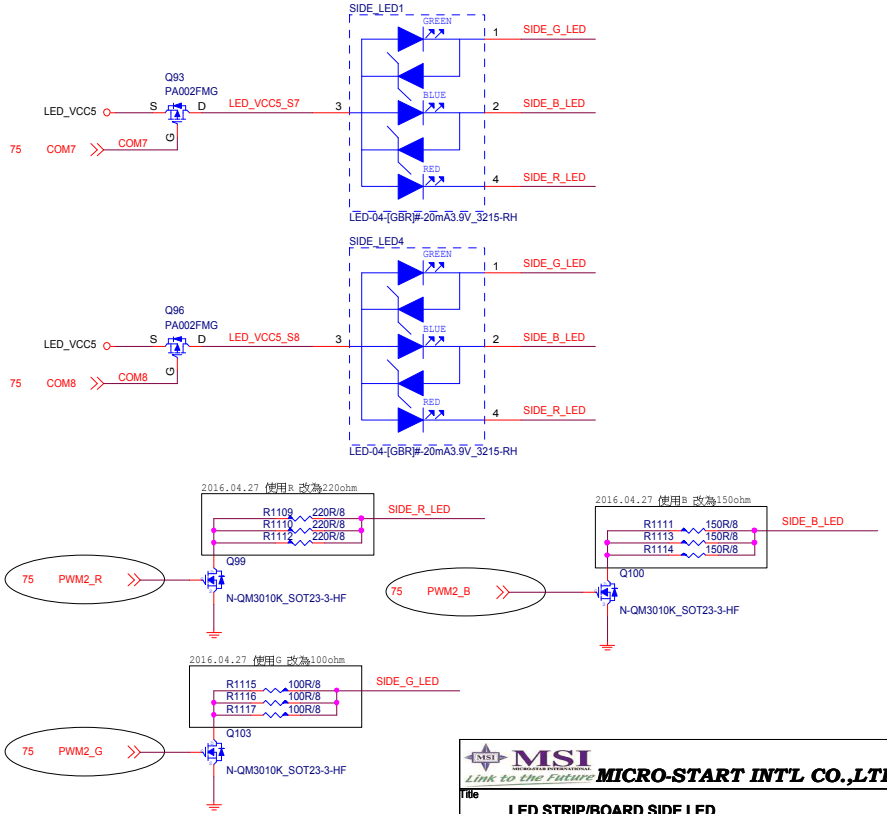
N31-1040321-P05

外接LED 燈條 (RGB)
---- PCB 文字面 (JLED1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) ,
長度限制為2公尺 (待7A20驗證)

BOARD SIDE LED *8

D0C-040R700-H91
Forward Current 20mA
Pulse Forward Current 30-60mA





MICRO-START INT'L CO.,LTD.

Title	LED STRIP/BOARD SIDE LED	
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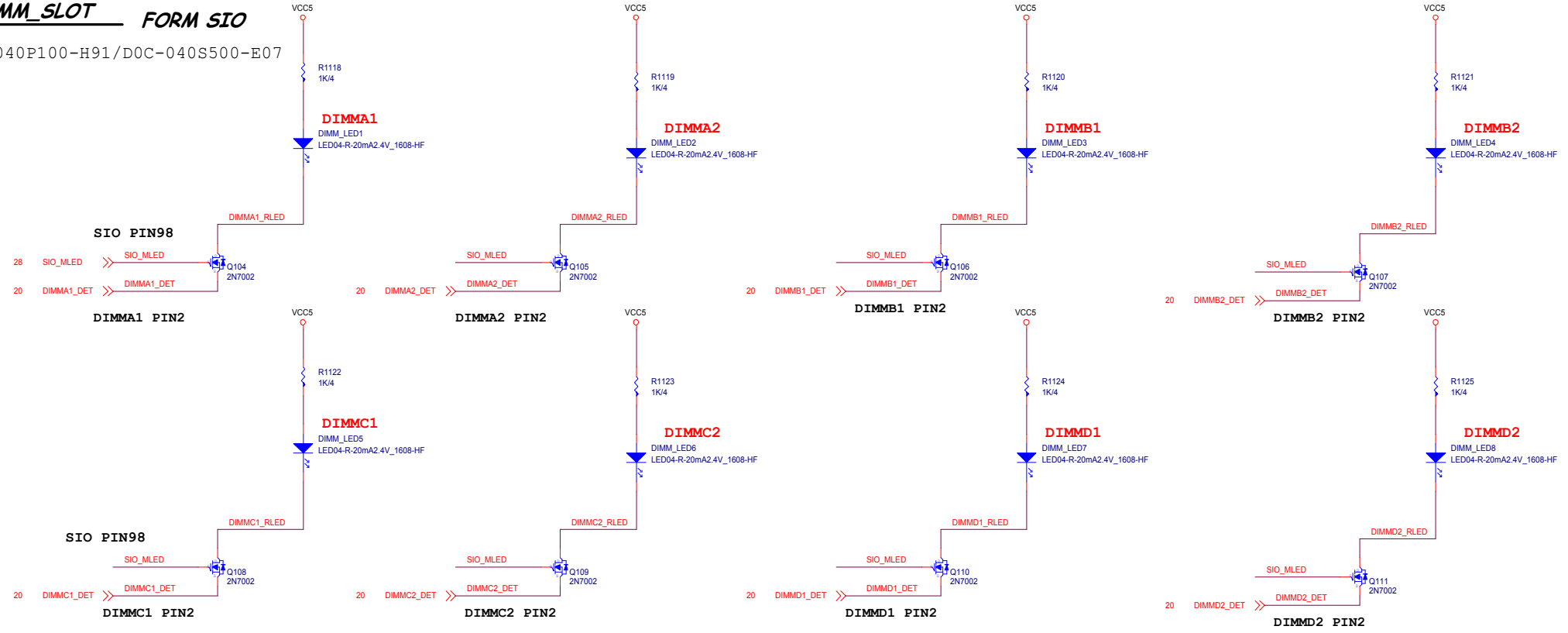
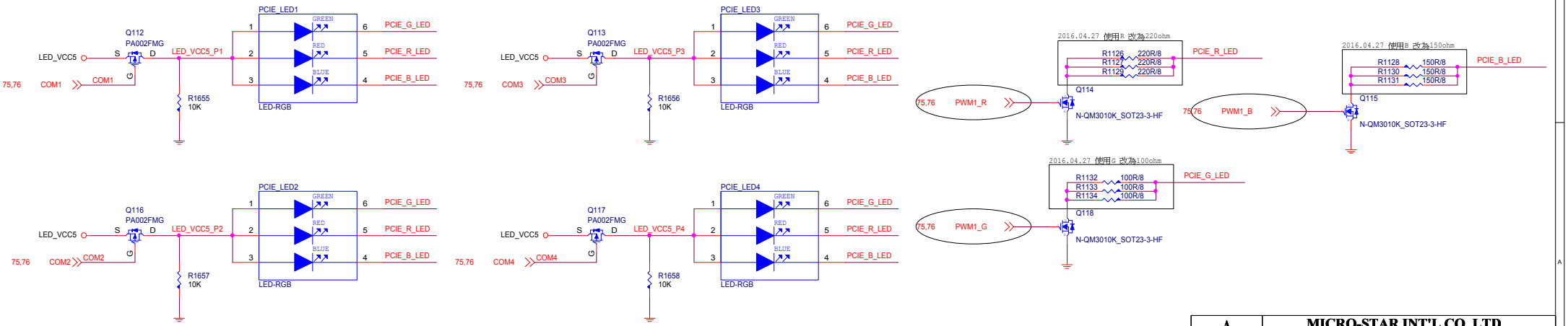
DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07



PCIE_SLOT LED*4 FORM MCU

D0C-040S400-H91



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MS-7B09..		
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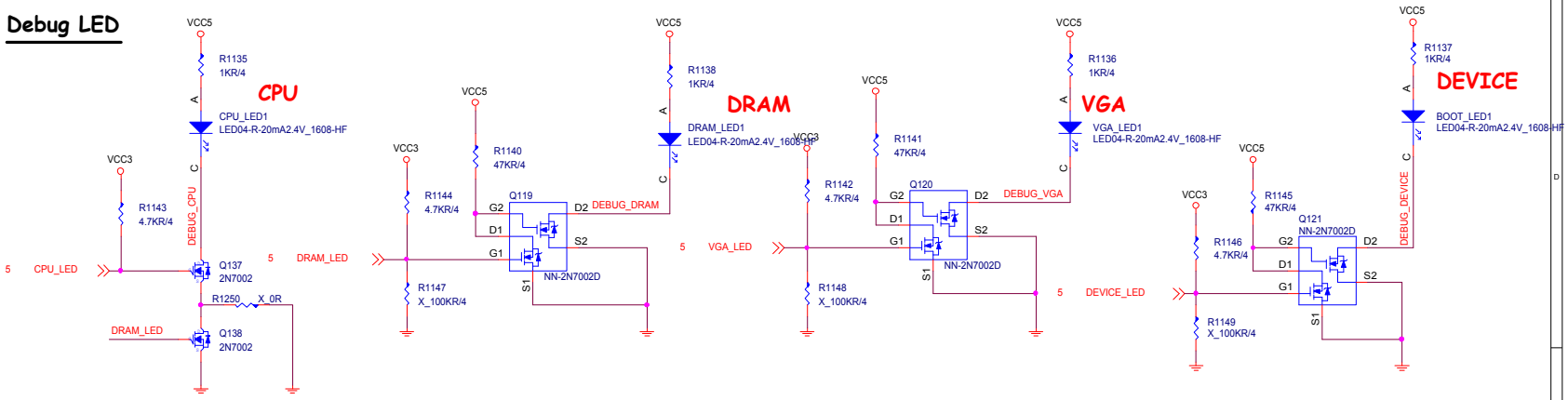
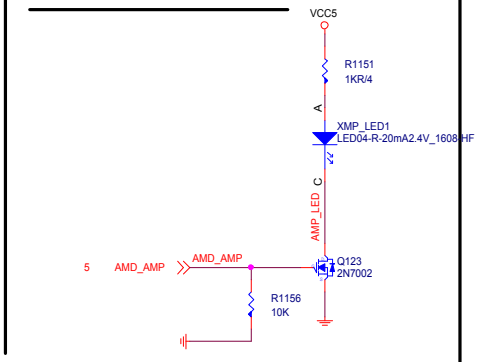
Debug LED



LED \ GPIO	AGPIO84_0	AGPIO85_0	EGPIO84_1	EGPIO85_1
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED



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Title: DEBUG LED

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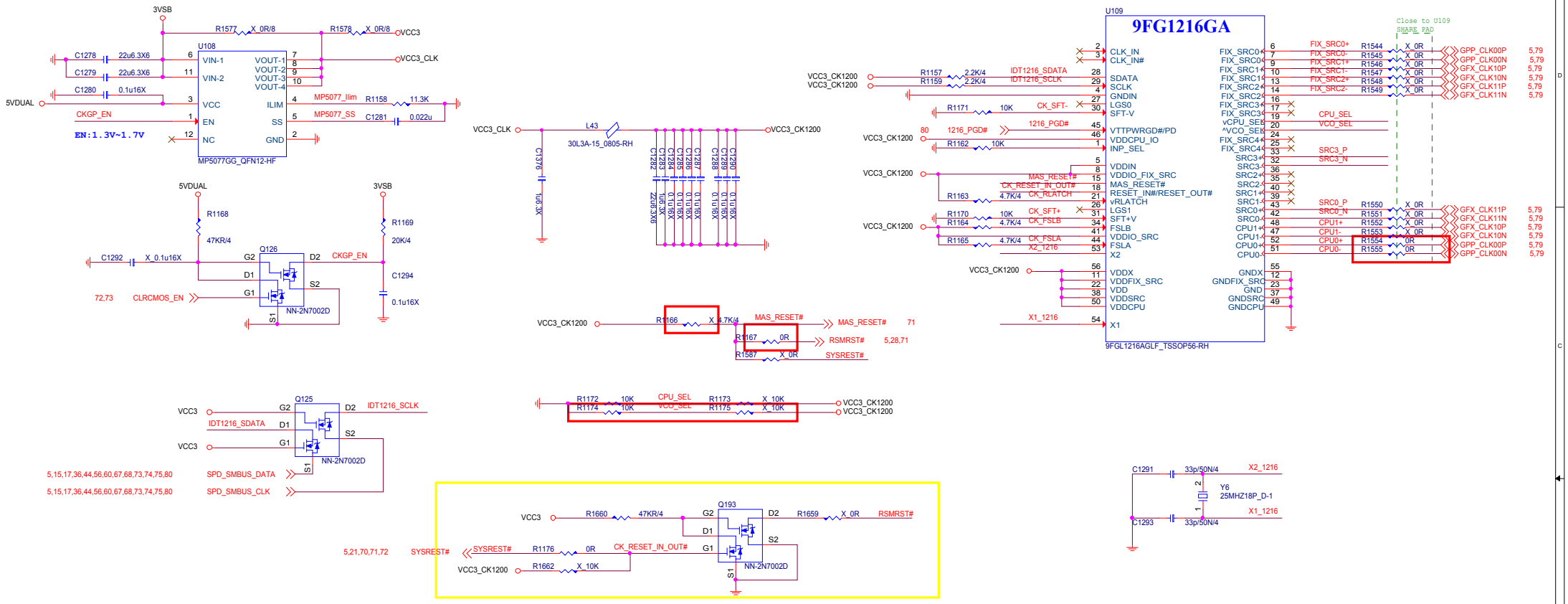
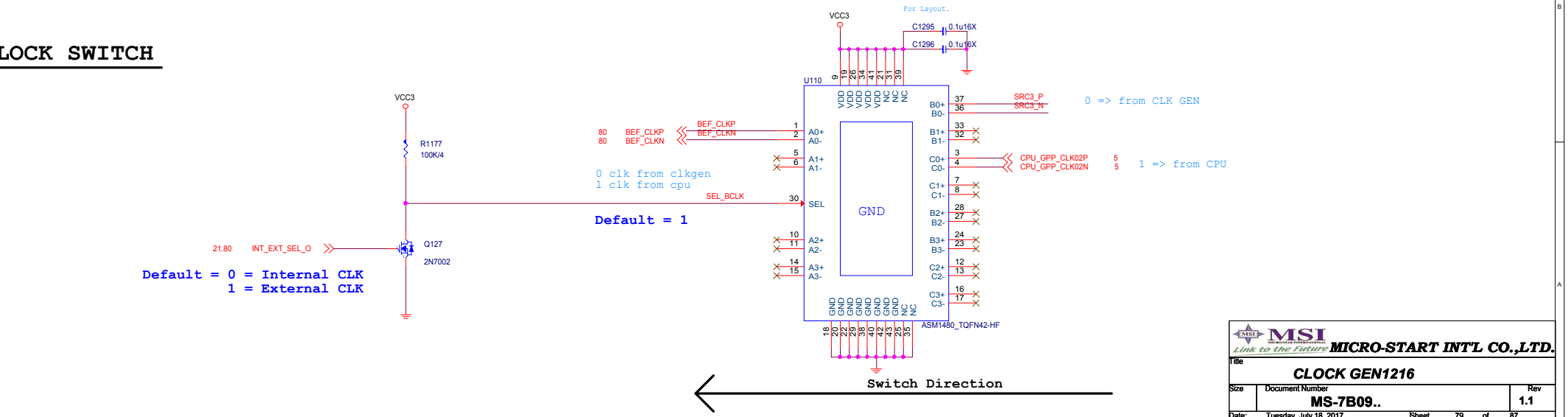
CLOCK GEN



CLOCK SWITCH



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Title: CLOCK GEN1216

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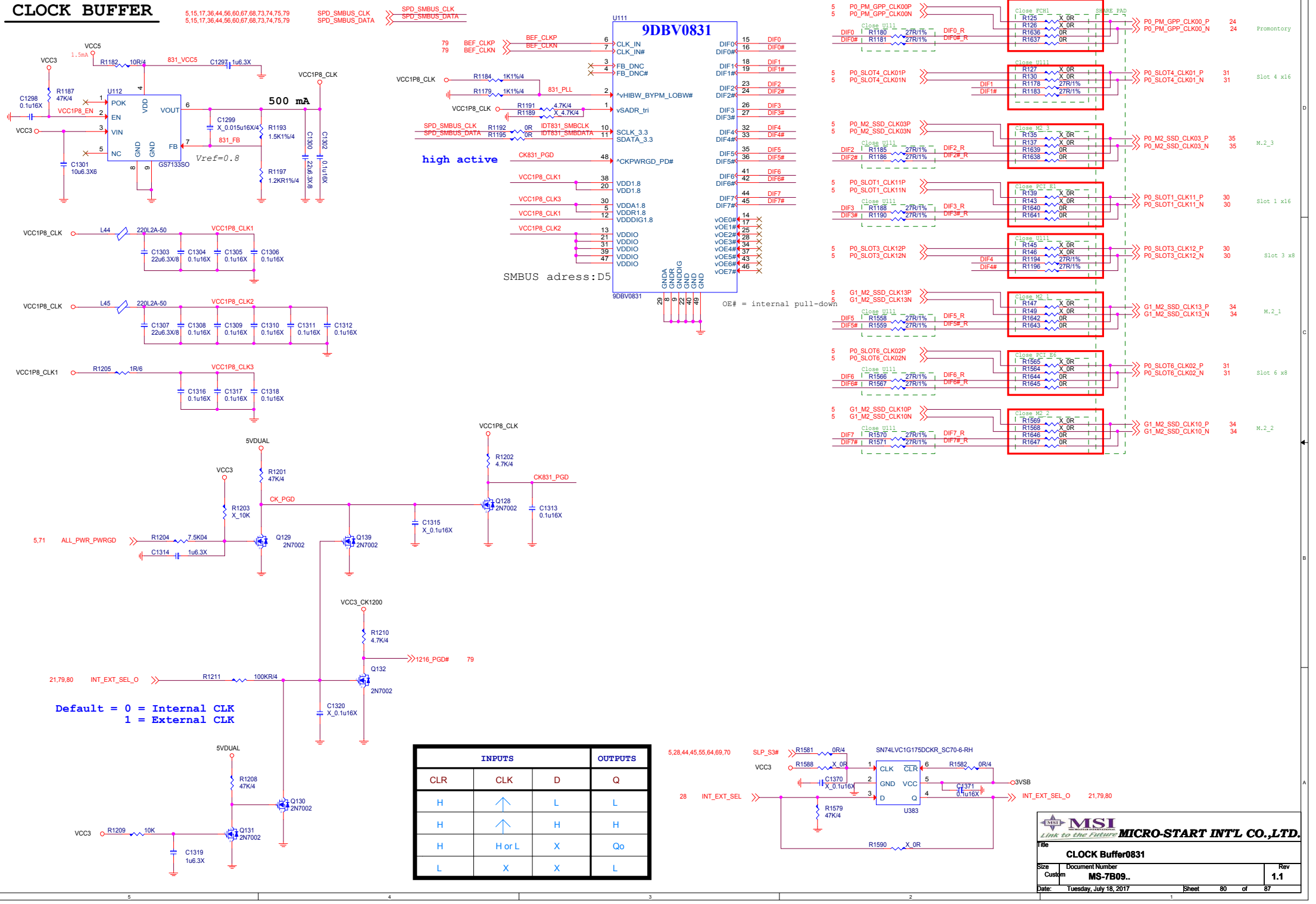
CLOCK BUFFER



INPUTS			OUTPUTS
CLR	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	Qo
L	X	X	L

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Title	CLOCK Buffer0831	
Size: Custom	Document Number: MS-7B09..	Rev: 1.1
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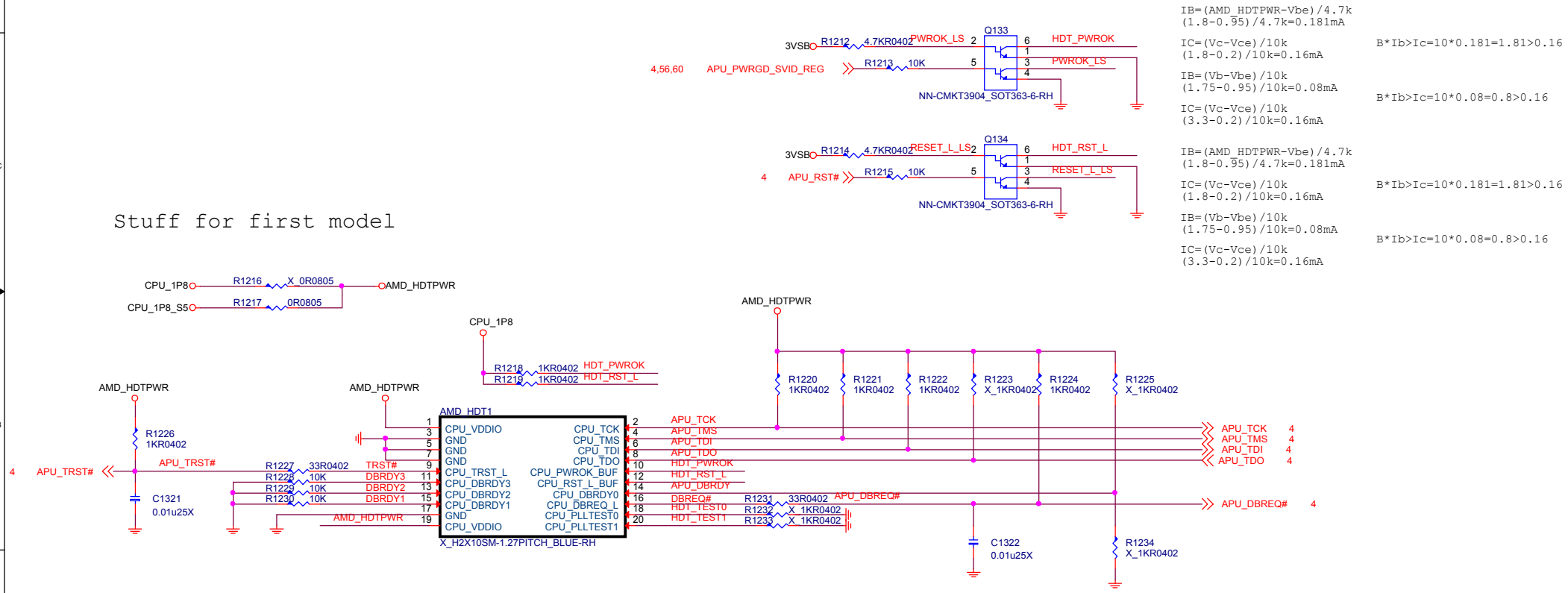

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Title: APU HDT DEBUG

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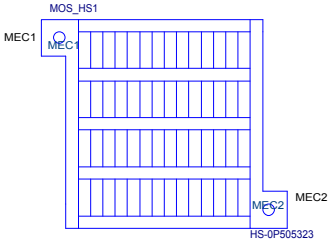
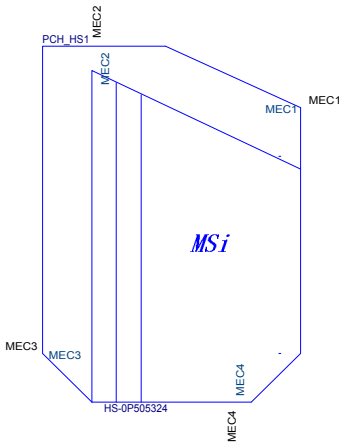
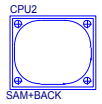
HEAT SINK

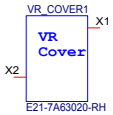




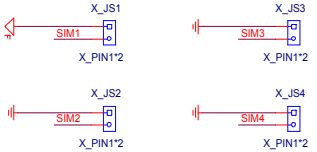
CPU Socket



VR COVER



Simulation



MANUAL PART

AMI1
AMI LABEL
G51-M1SPXXA-A09

CFOS1
Label
VIRTUAL
CFOS
Y02-MU00170-CFO

NAHIMIC1
Label
BUNDLE
NAHIMIC
Y02-MU00100-NAH

MKT1
Label
BUNDLE
MKT
G51-M1SPL82-Q13

XSPLIT1
Label
BUNDLE
XSPLIT
Y02-MA00401-XSP

SSE1
Label
VIRTUAL
SSE
Y02-MA00101-SSE

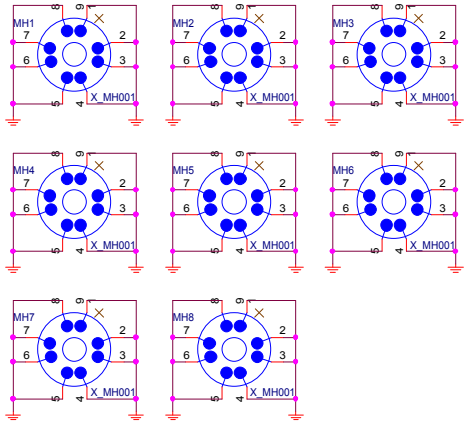
SLI1
Label
VIRTUAL
SLI
Y01-RNVIDIN-000

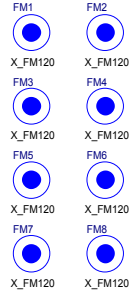
BAT1_X1
BAT-CR2032
D06-0105101-K26

PCB1
7B09-1.1
測試 only

VER: 1.0 --> 601-7B09-01S
VER: 1.1 --> 601-7B09-02S

Optics Orientation Holes





MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: BOM OPTION		
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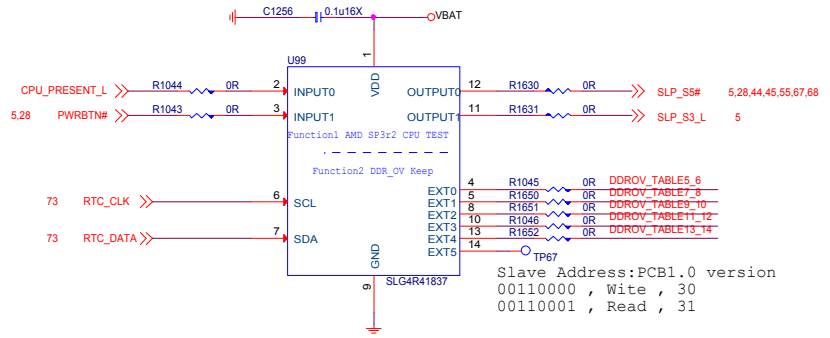
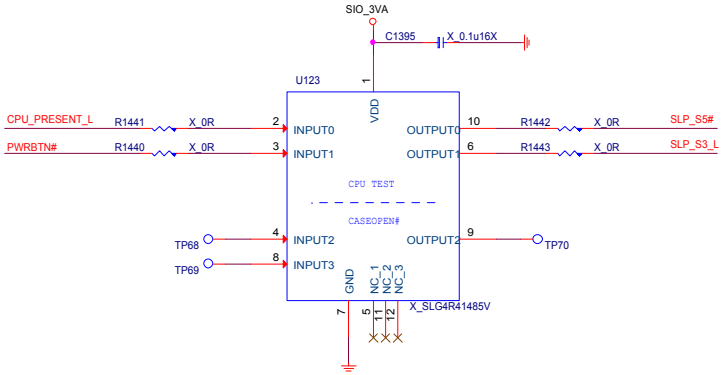
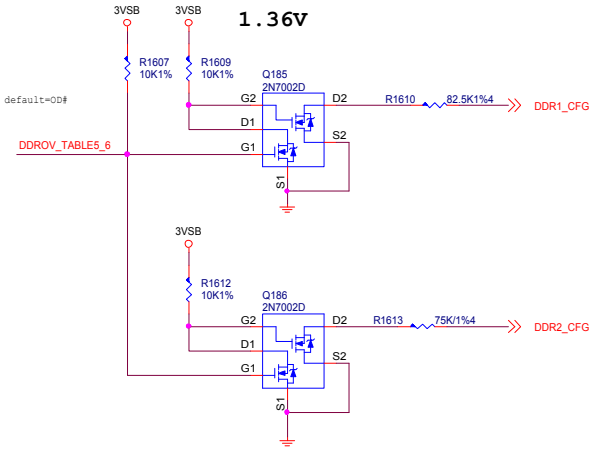
Add for EMI

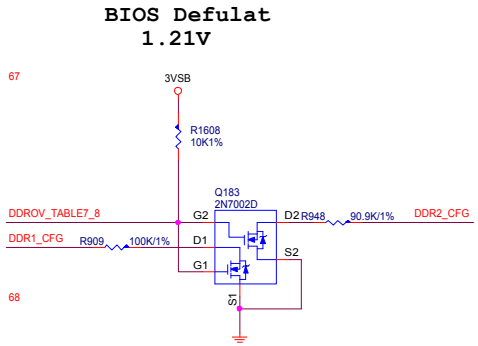


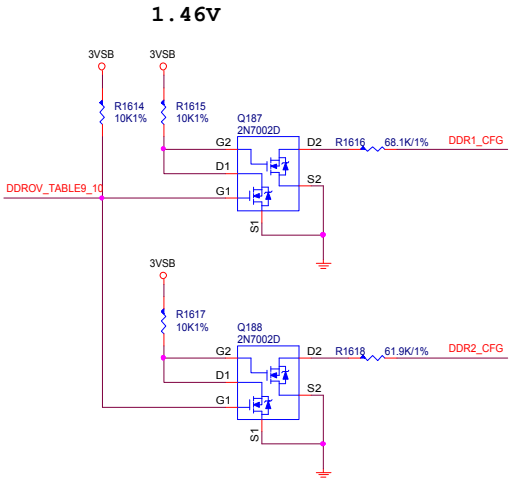
Slave Address:PCB1.0 version
00110000 , Wite , 30
00110001 , Read , 31

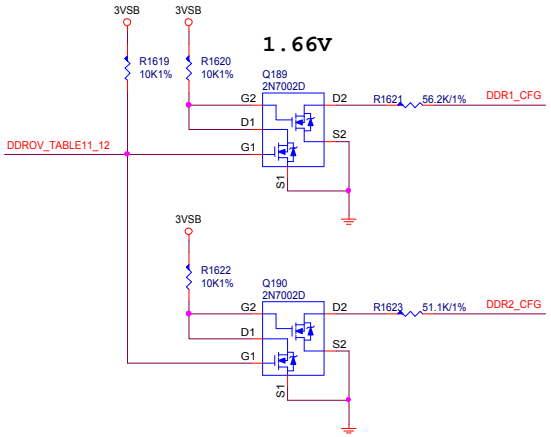
Slave Address:PCB1.1 version
01010000 , Wite , 50
01010001 , Read , 51

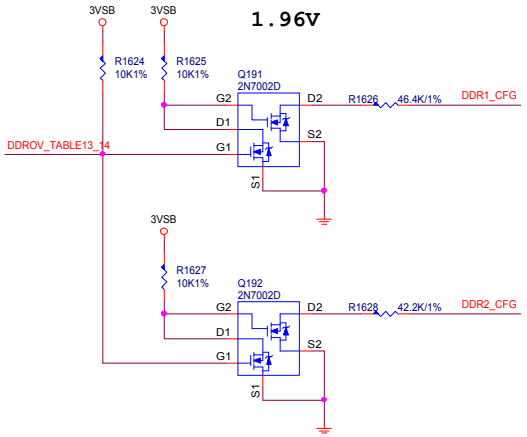












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