MS-7393

Version: 1.1

CPU: **Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe / Kentsfield family processors in LGA775 Package.**

System Chipset:

NVIDIA MCP73

On Board Device:

BIOS -- SPI Flash 4M
Azalia Codec -- ALC888
LPC Super I/O -- FINTEK F71882FG
LAN -- Realtek RTL8211BL-GR
CLOCK Gen -- Integated in MCP73

Main Memory:

Dual-channel DDR-II * 2 (Max 4GB)

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

Intersil PWM:

Controller: Intersil ISL6312 (3 Phases)

PCB = 245mm X 220mm 4L

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Size: Custom | Document Description: Cover Sheet | Rev: 0A
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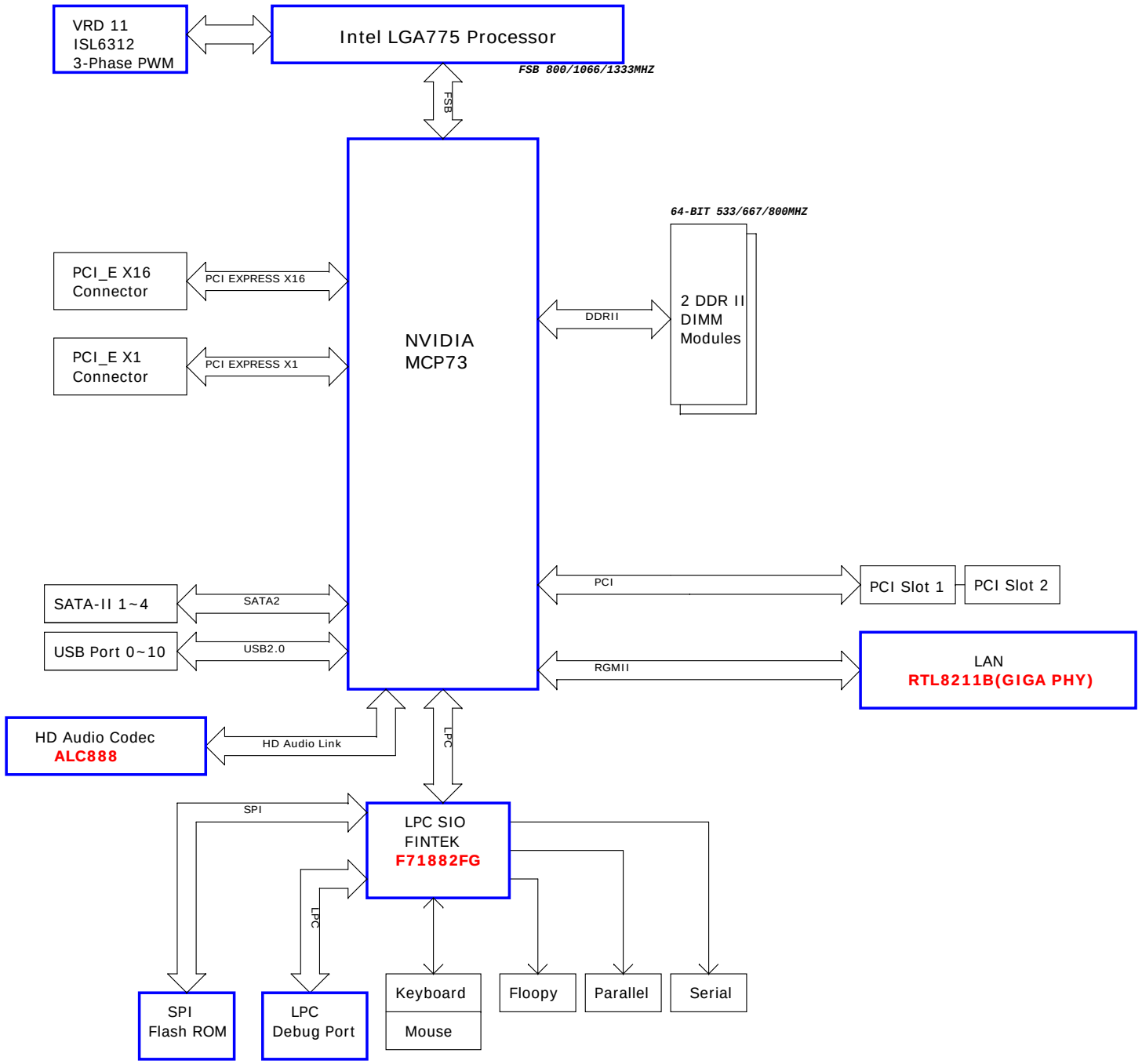
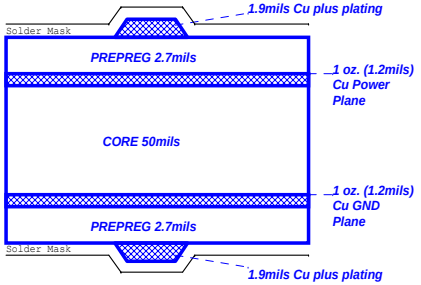
Block Diagram



Board Stack-up

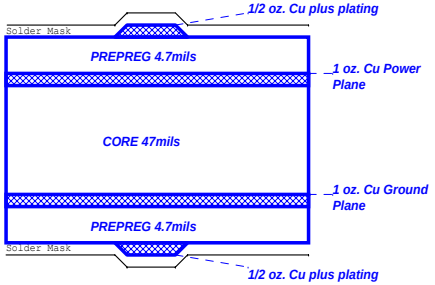
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils
IEEE1394 - 110ohm Top : 5/7/5
PCIE, LAN, SATA - 100ohm Top : 5/6/5
USB2.0 - 90ohm Top : 7.5/7.5/7.5

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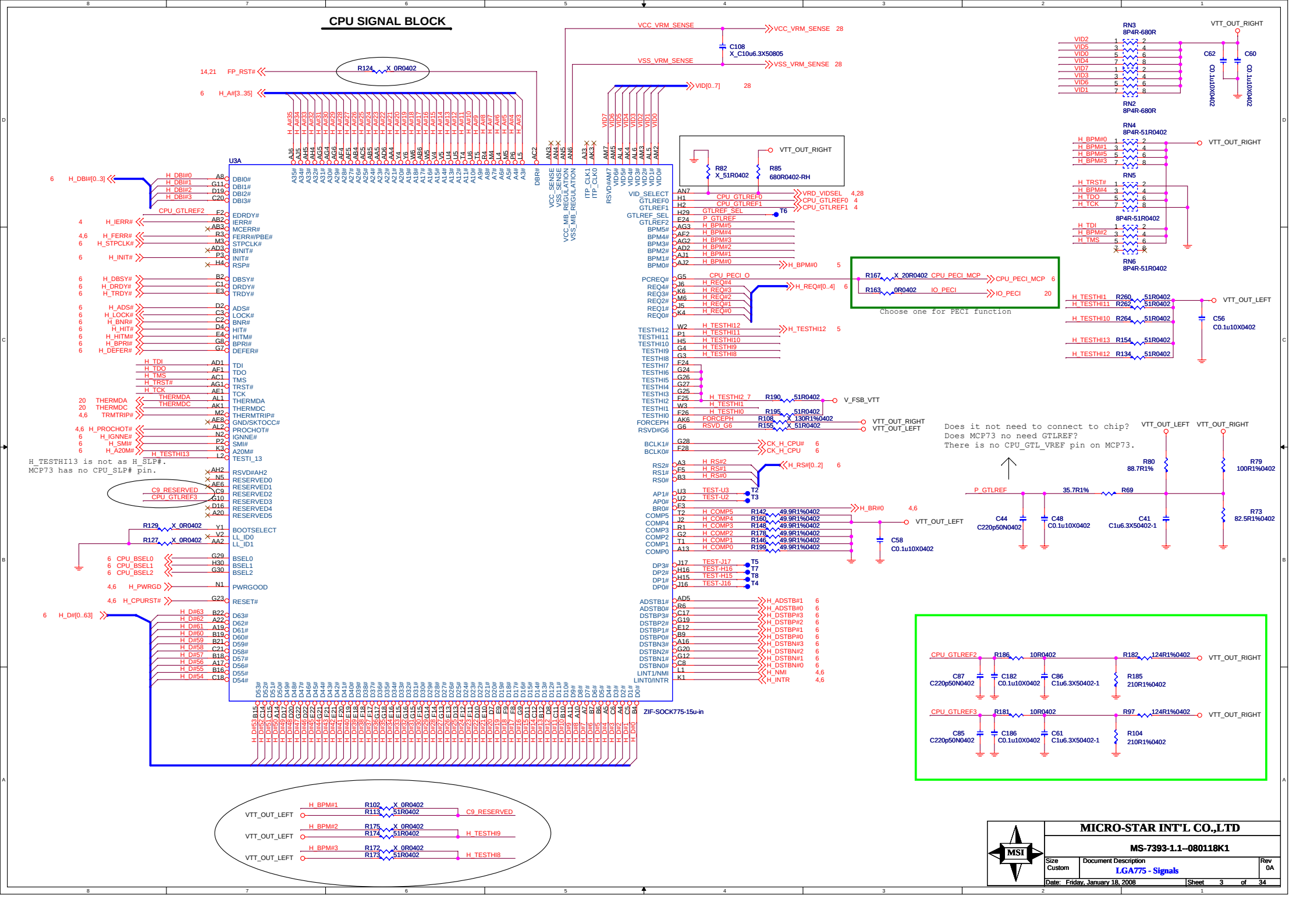
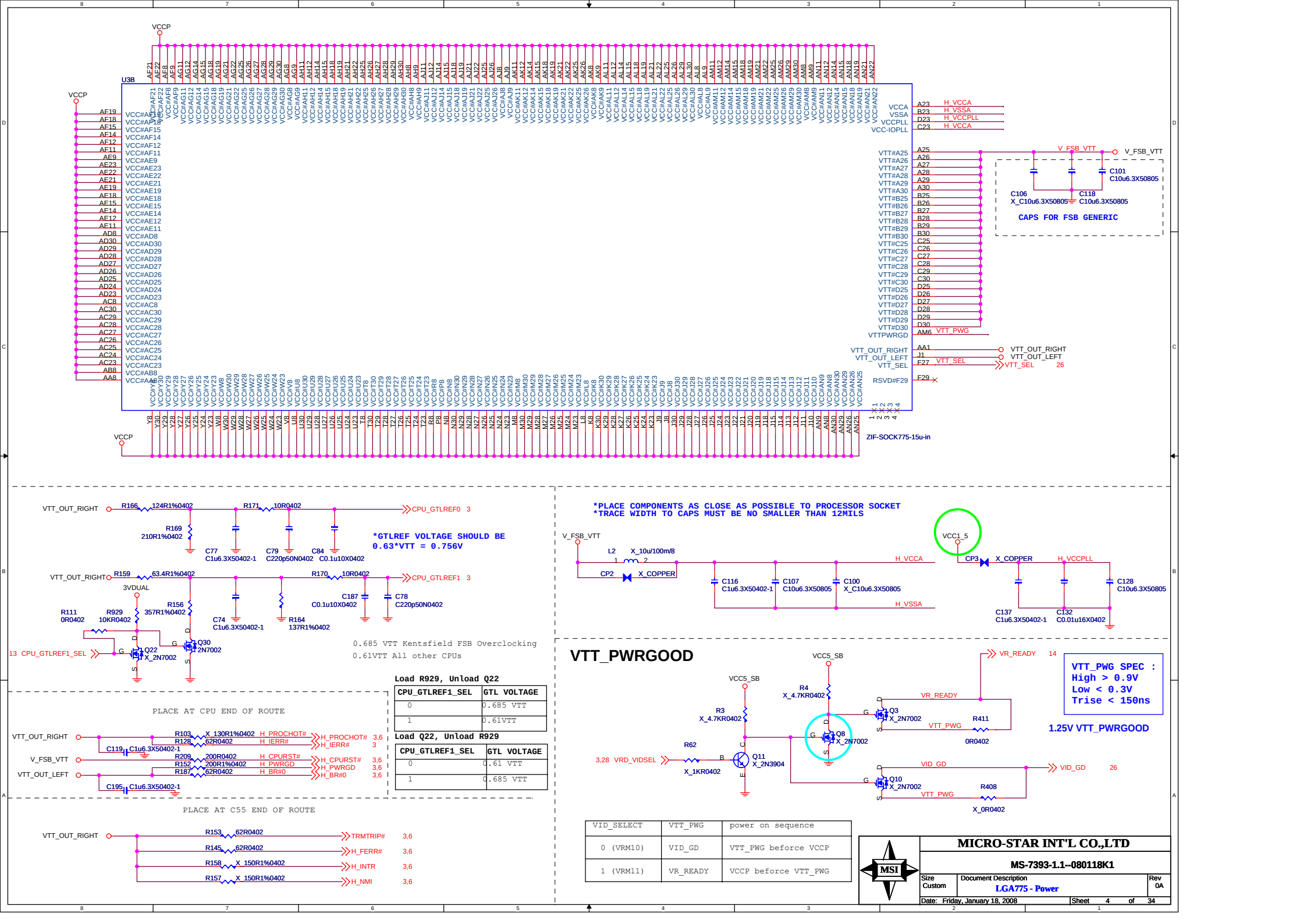
CPU SIGNAL BLOCK





Load R929, Unload Q22

CPU_GTLREF1_SEL	GTL VOLTAGE
0	0.685 VTT
1	0.61VTT

Load Q22, Unload R929

CPU_GTLREF1_SEL	GTL VOLTAGE
0	0.61 VTT
1	0.685 VTT

VID_SELECT	VTT_PWG	power on sequence
0 (VRM10)	VID_GD	VTT_PWG beforce VCCP
1 (VRM11)	VR_READY	VCCP beforce VTT_PWG

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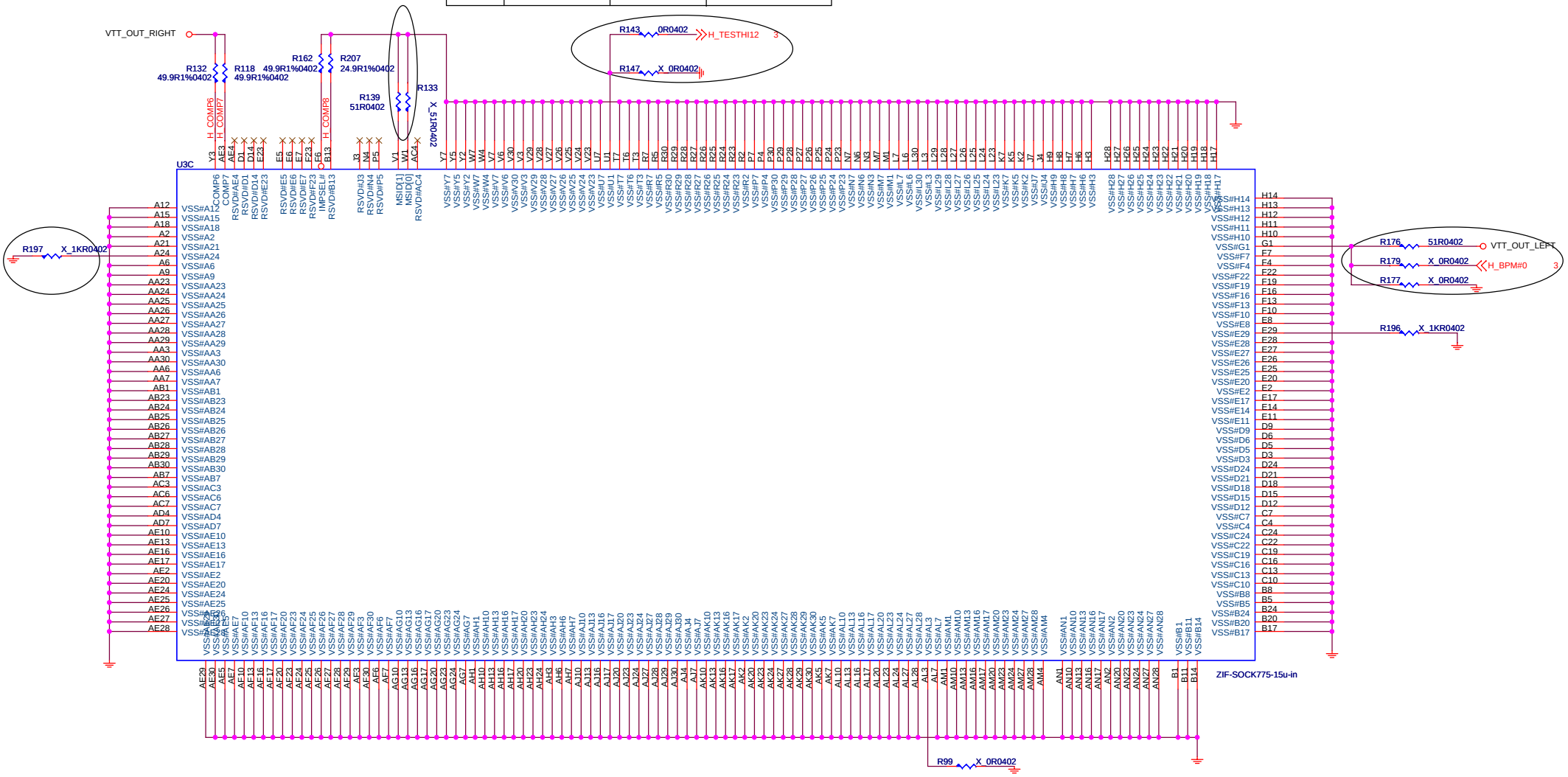
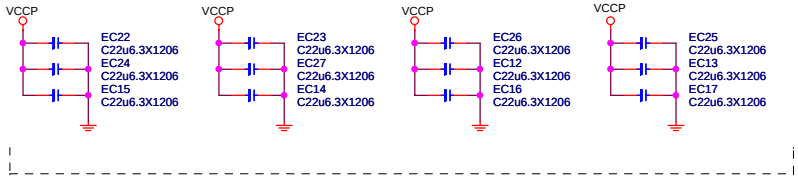
	05B (130W)	05A (95W)	2006 65W FSB
MSID1	pull-down	pull-down	NC
MSID0	pull-down	NC	NC



CPU DECOUPLING CAPACITORS



Place these caps within socket cavity

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Size	Document Description	Rev
Custom	LGA775 - GND	0A

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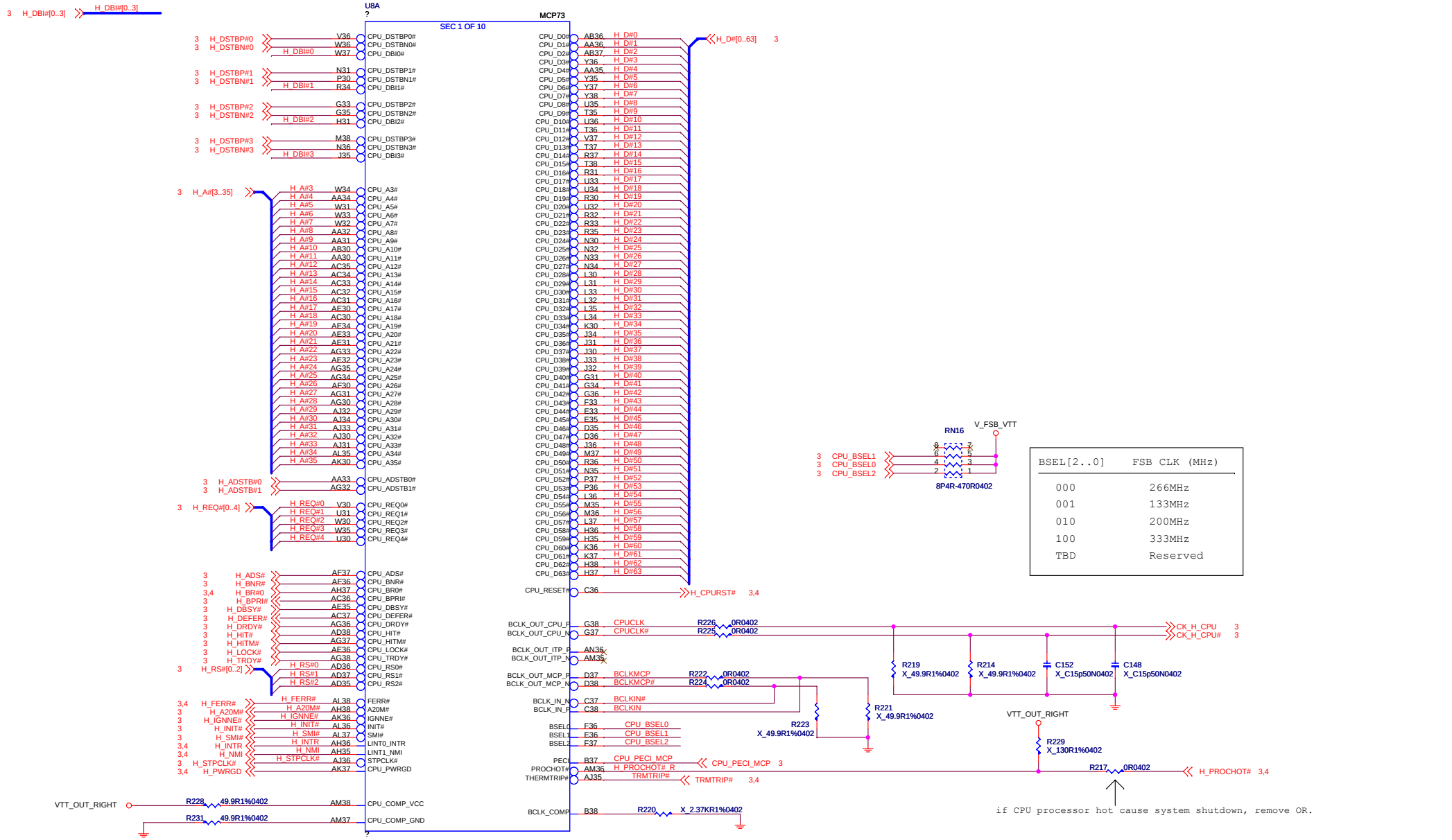

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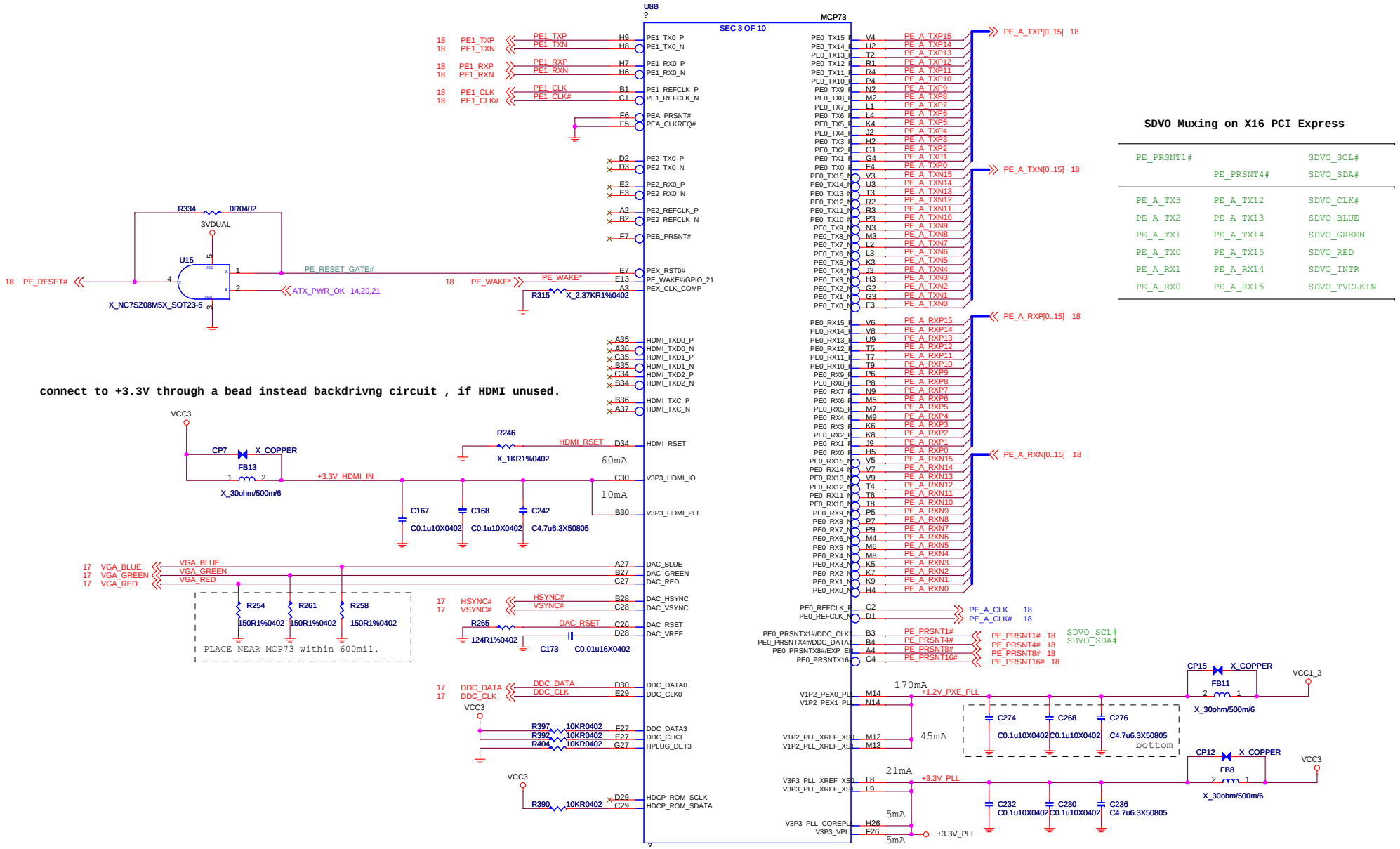

SDVO Muxing on X16 PCI Express

PE_PRSNT1#		SDVO_SCL#
	PE_PRSNT4#	SDVO_SDA#
PE_A_TX3	PE_A_TX12	SDVO_CLK#
PE_A_TX2	PE_A_TX13	SDVO_BLUE
PE_A_TX1	PE_A_TX14	SDVO_GREEN
PE_A_TX0	PE_A_TX15	SDVO_RED
PE_A_RX1	PE_A_RX14	SDVO_INTR
PE_A_RX0	PE_A_RX15	SDVO_TVCLKIN

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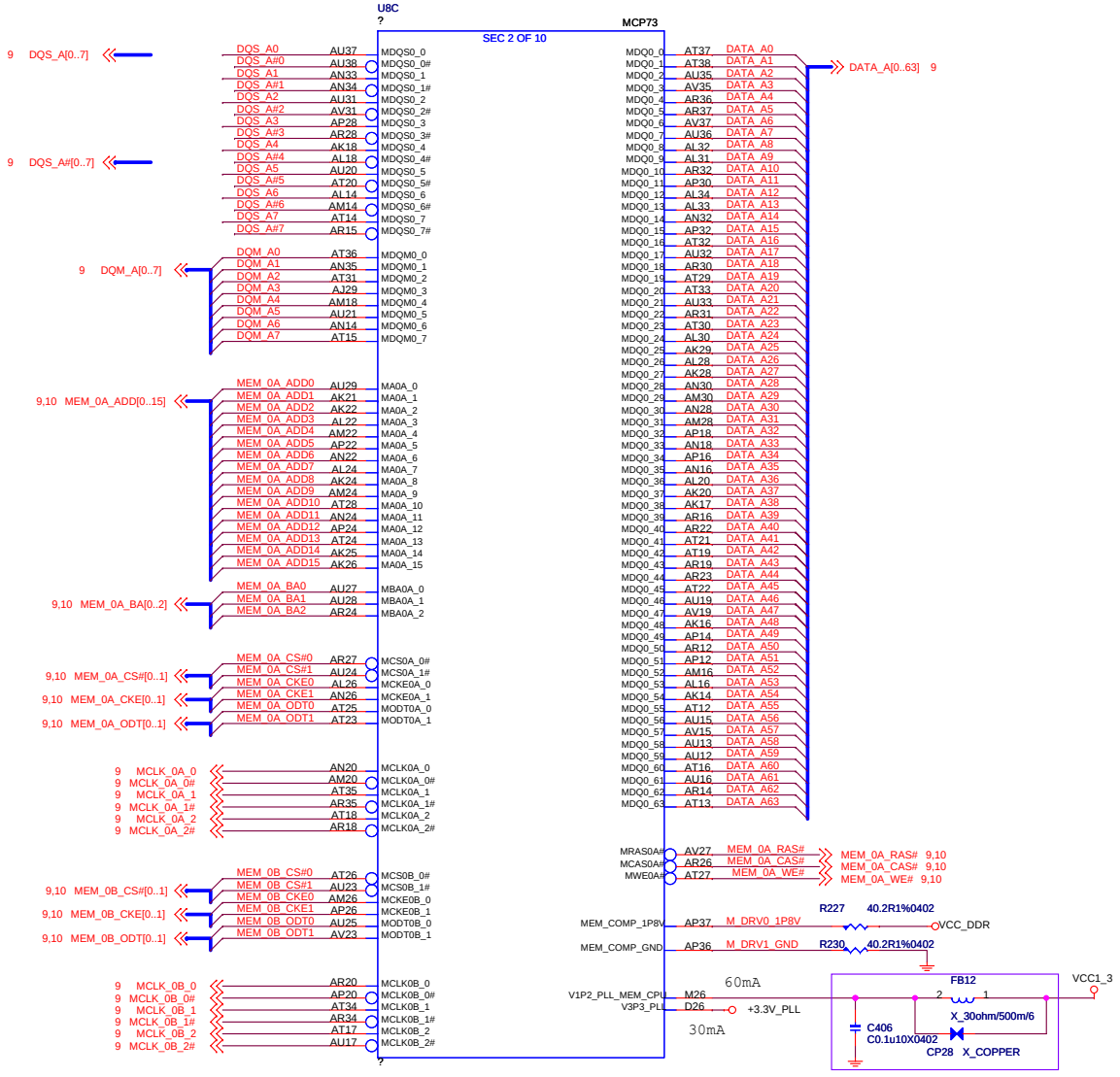
DATA 0

DIMM 1 ADDR 0A / CNTL 0A

DIMM 2 ADDR 0B / CNTL 0B

DIMM 0A



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Size: Custom	Document Description: MCP73-MEM
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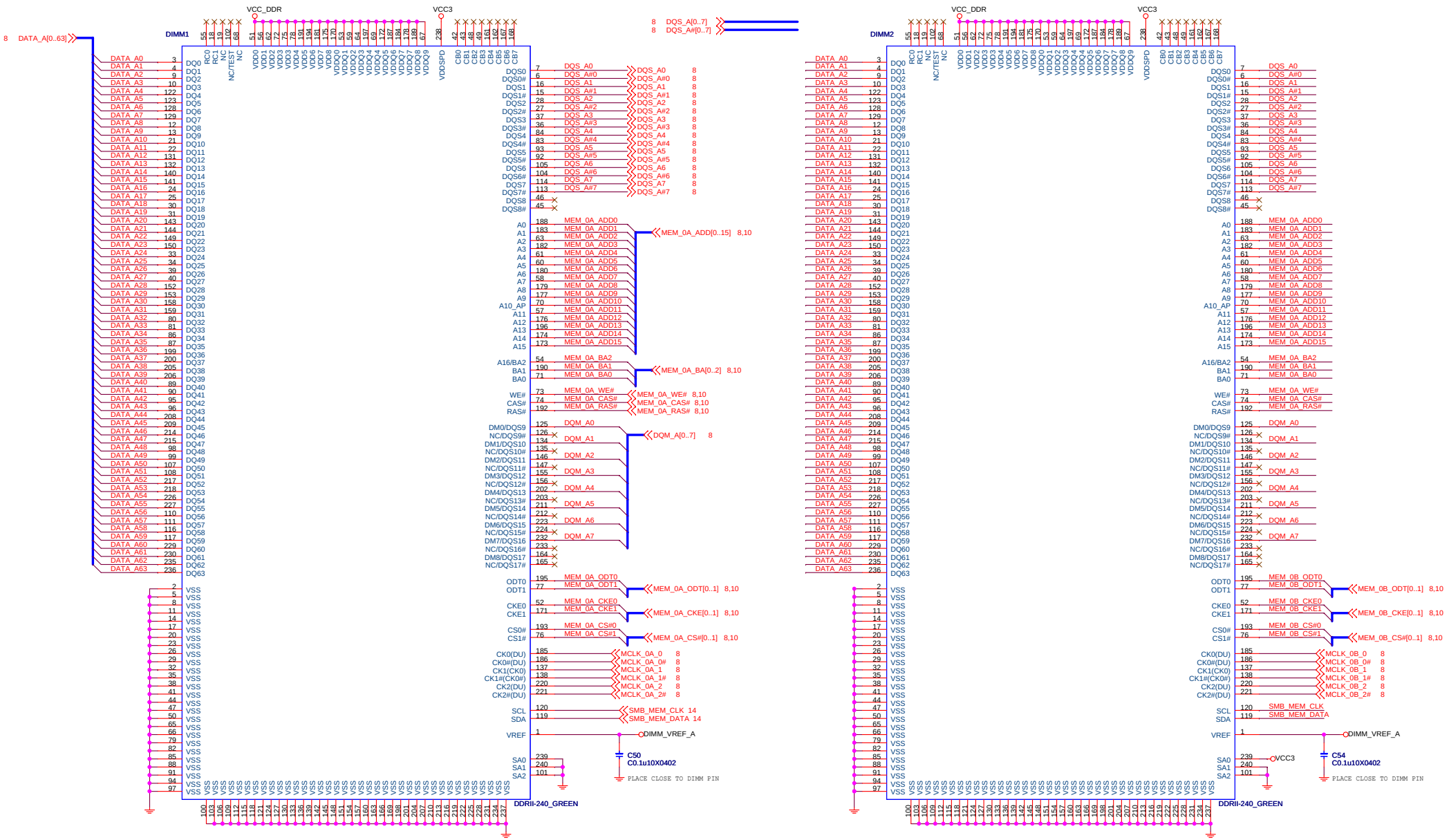

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR II - DIMM 1 & 2 Sockets
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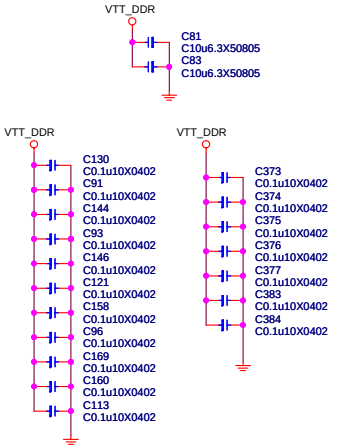
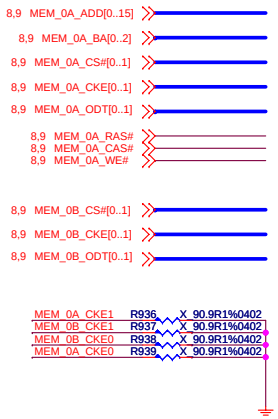
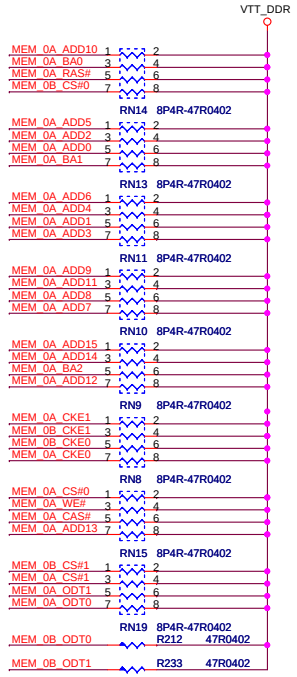
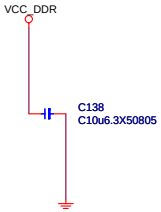
CHANNEL A VTT_DDR DECOULPING CAPS

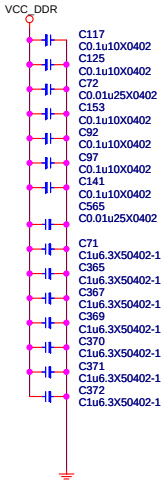


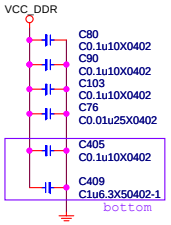
CHANNEL A ----- 0A , 0B







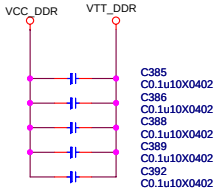




公板上0.1u X5, 1uX3, 10uX3
兩根再X2

C76,C72,C565
103P
EMI Ver1.1

C104P_10
C



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Size: Custom	Document Description: DDR II VTT Termination & Decoupling	Rev: 0A
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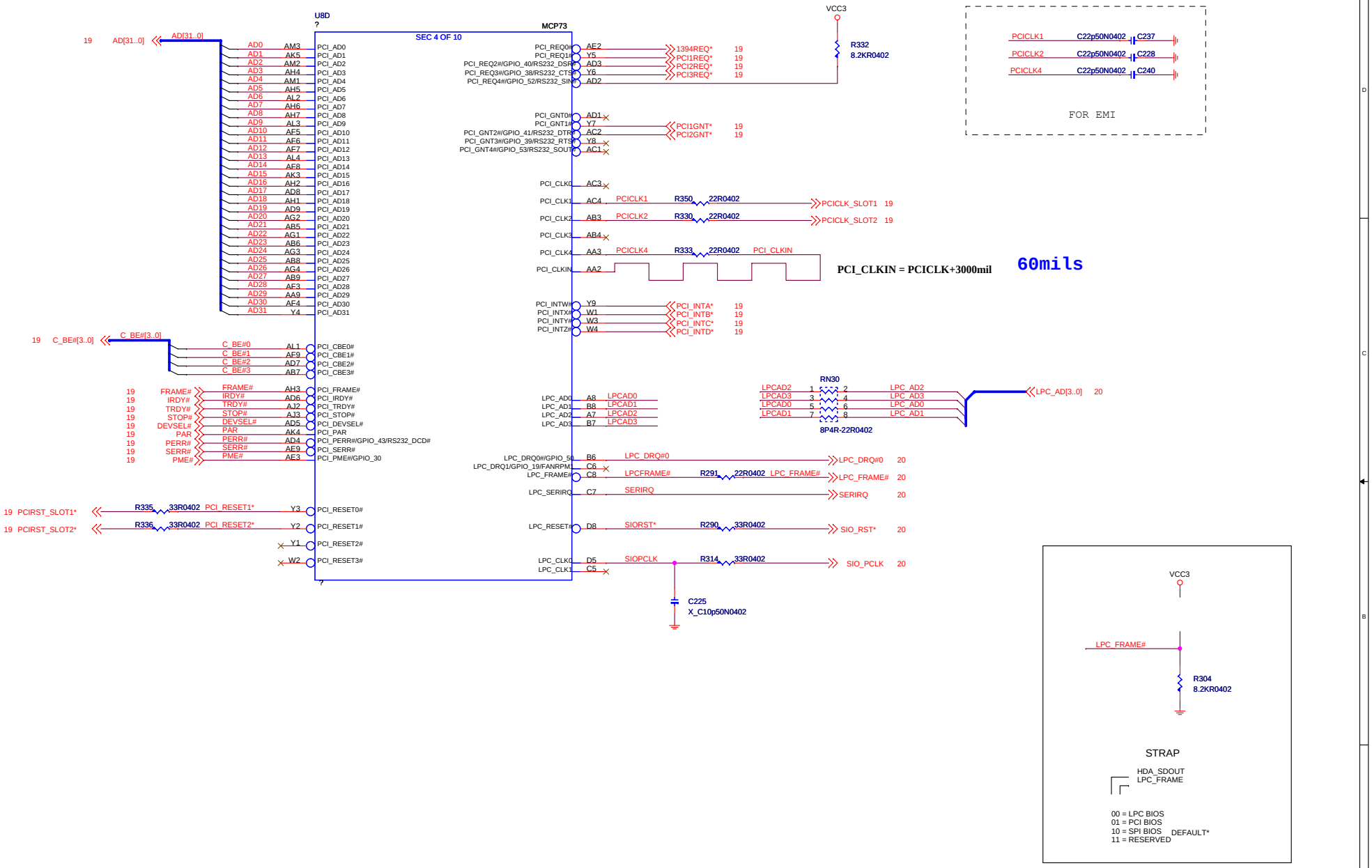

MICRO-STAR INT'L CO.,LTD		
MS-7393-1.1--080118K1		
Size: Custom	Document Description: MCP73-PCI/LPC	Rev: 0A
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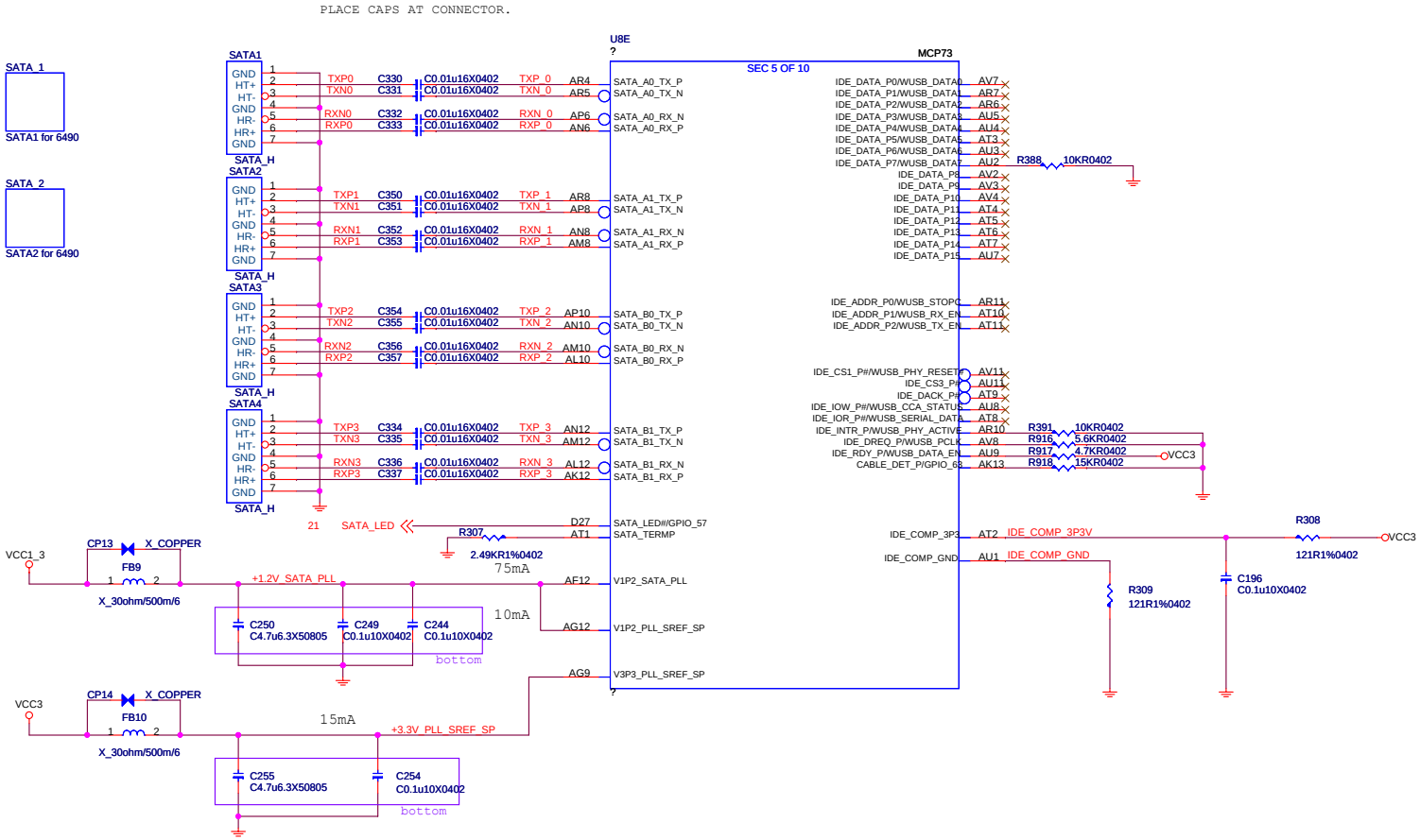

MICRO-STAR INT'L CO.,LTD		
MS-7393-1.1--080118K1		
Size: Custom	Document Description: MCP73-SATA/IDE	Rev: 0A
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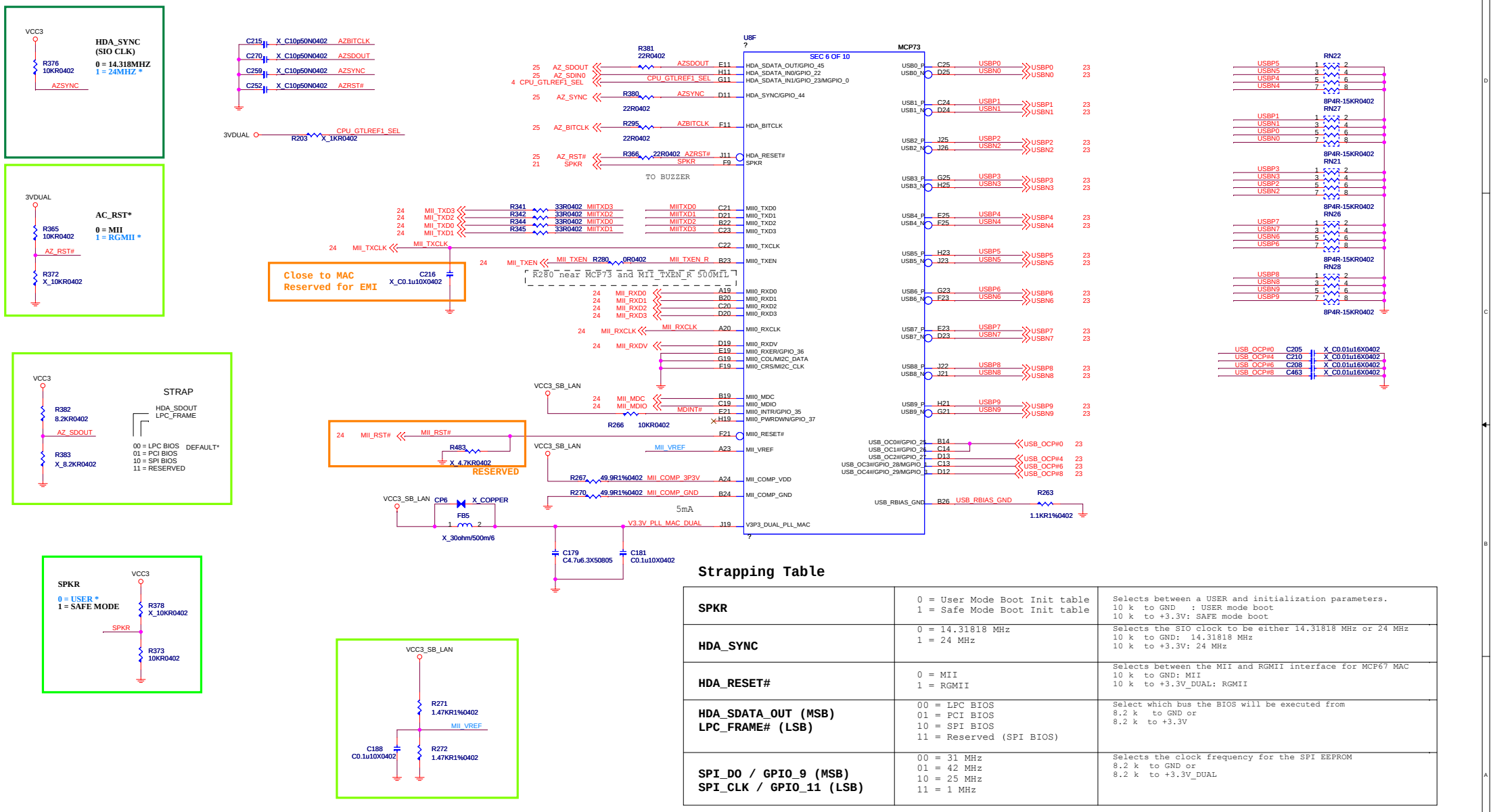

Strapping Table

SPKR	0 = User Mode Boot Init table 1 = Safe Mode Boot Init table	Selects between a USER and initialization parameters. 10 k to GND : USER mode boot 10 k to +3.3V: SAFE mode boot
HDA_SYNC	0 = 14.31818 MHz 1 = 24 MHz	Selects the SIO clock to be either 14.31818 MHz or 24 MHz 10 k to GND: 14.31818 MHz 10 k to +3.3V: 24 MHz
HDA_RESET#	0 = MII 1 = RGMII	Selects between the MII and RGMII interface for MCP67 MAC 10 k to GND: MII 10 k to +3.3V_DUAL: RGMII
HDA_SDATA_OUT (MSB) **LPC_FRAME# (LSB)**	00 = LPC BIOS 01 = PCI BIOS 10 = SPI BIOS 11 = Reserved (SPI BIOS)	Select which bus the BIOS will be executed from 8.2 k to GND or 8.2 k to +3.3V
SPI_DO / GPIO_9 (MSB) **SPI_CLK / GPIO_11 (LSB)**	00 = 31 MHz 01 = 42 MHz 10 = 25 MHz 11 = 1 MHz	Selects the clock frequency for the SPI EEPROM 8.2 k to GND or 8.2 k to +3.3V_DUAL

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Size: Custom | Document Description: MCP73-AUDIO/USB/GPIO | Rev: 0A

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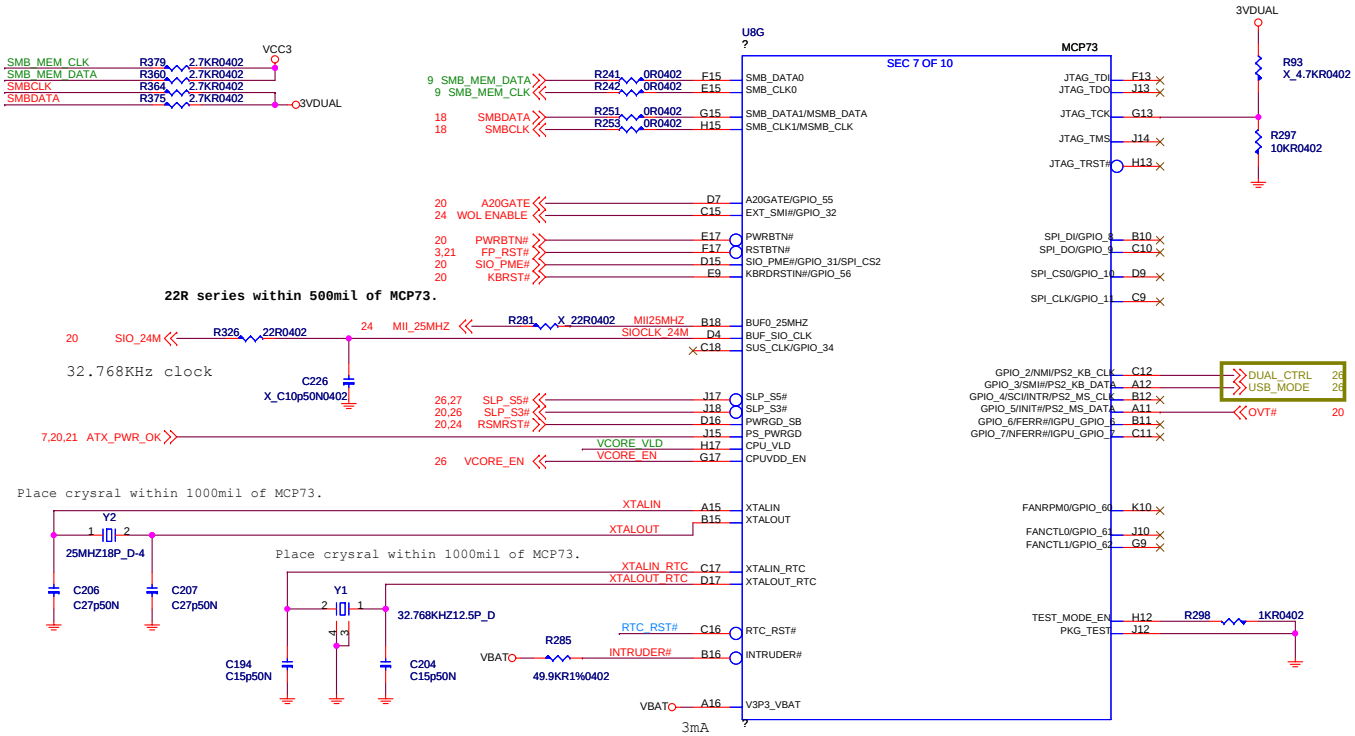

MICRO-STAR INT'L CO.,LTD	
MS-7393-1.1--080118K1	
Size: Custom	Document Description: MCP73-SPI/SMB
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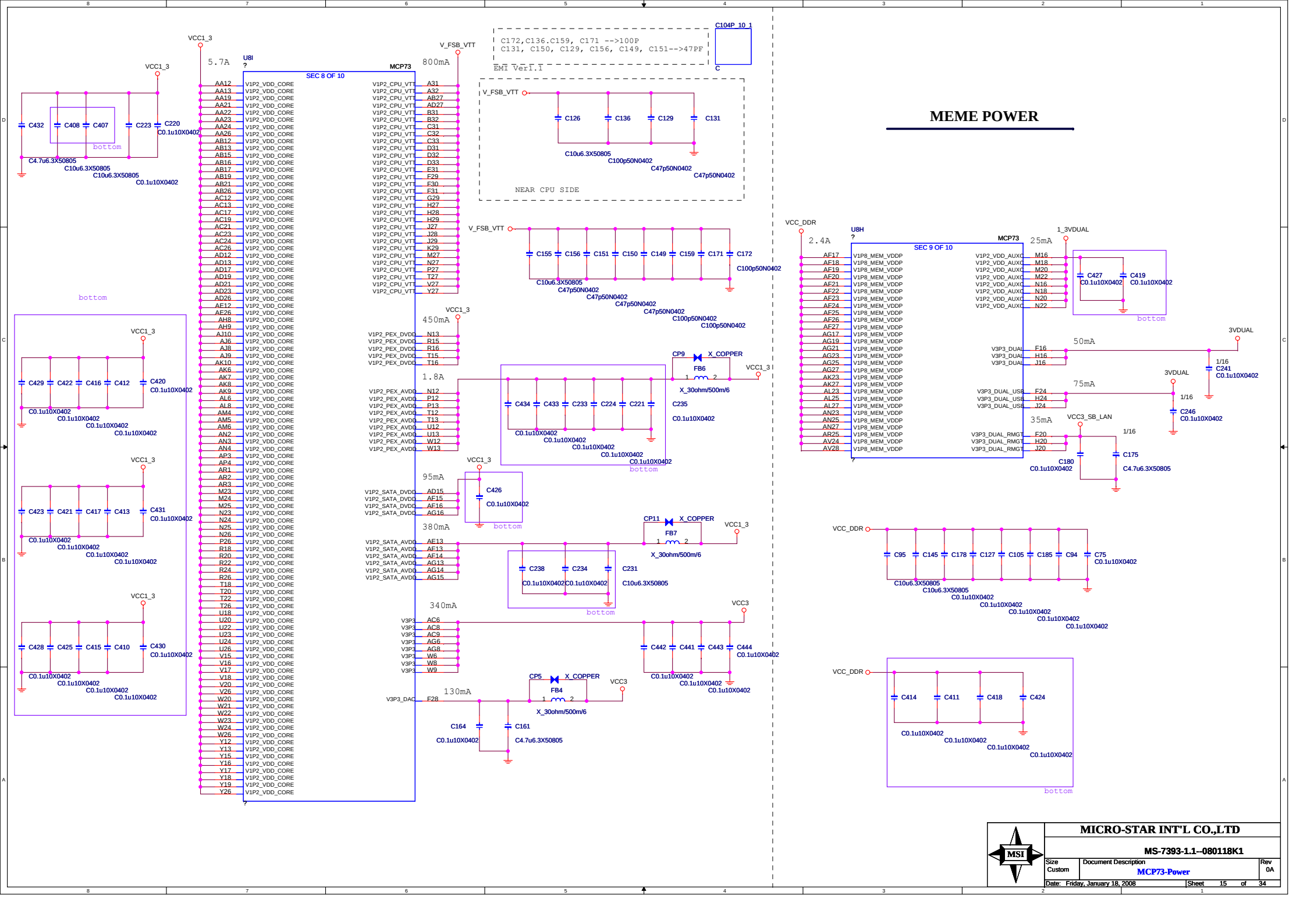
MEME POWER
U8I
SEC 8 OF 10
MCP73
U8H
SEC 9 OF 10
C104P_10_1
C172,C136.C159, C171 -->100P
C131, C150, C129, C156, C149, C151-->47PF
EMI Ver1.1
NEAR CPU SIDE
bottom
MICRO-STAR INT'L CO.,LTD
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MCP73-Power
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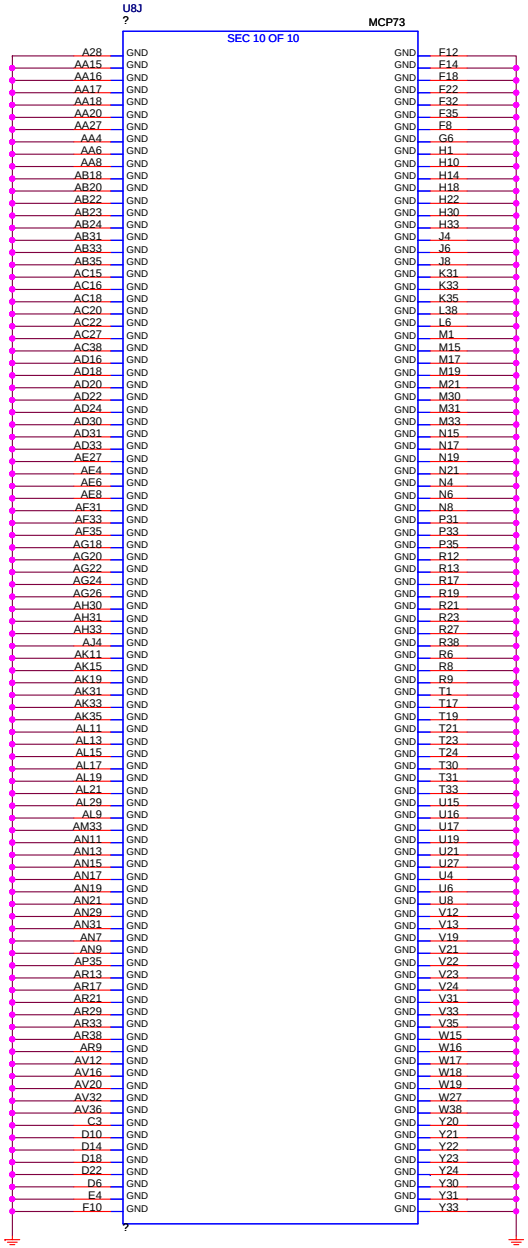

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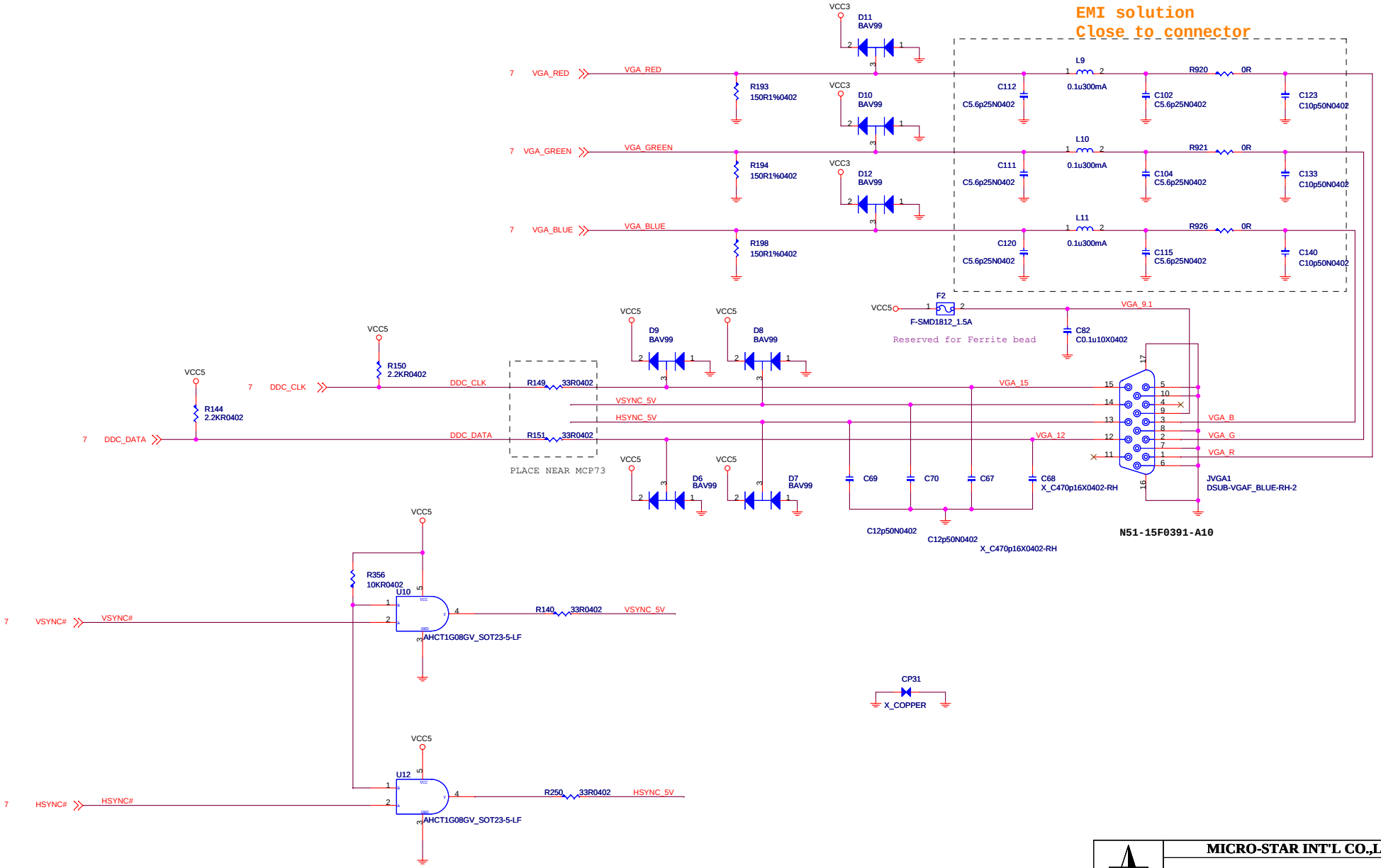
PLACE NEAR VGA CONNECTOR

EMI solution
Close to connector



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MS-7393-1.1--080118K1		
Size: Custom	Document Description: VGA Connector	Rev: 0A
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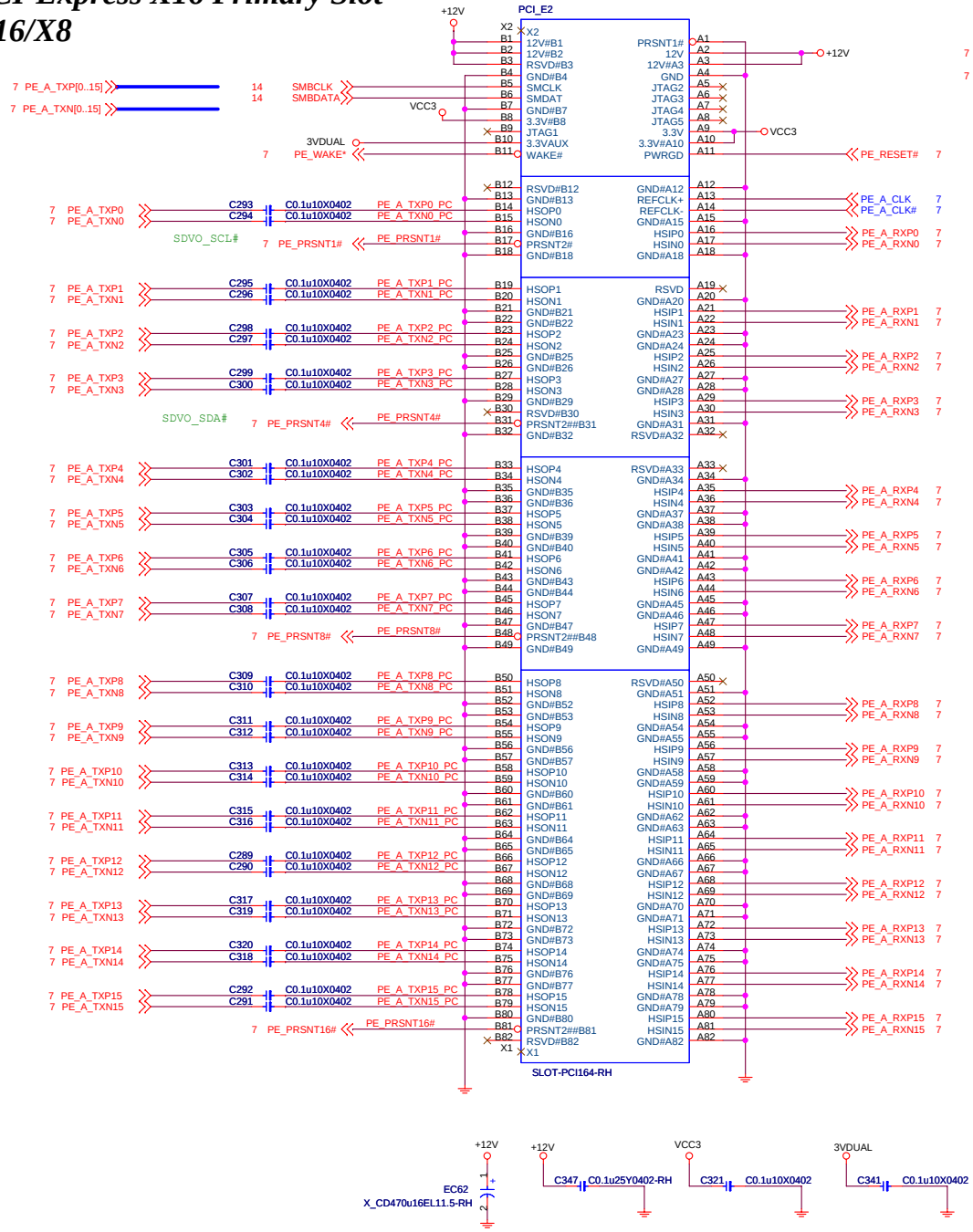
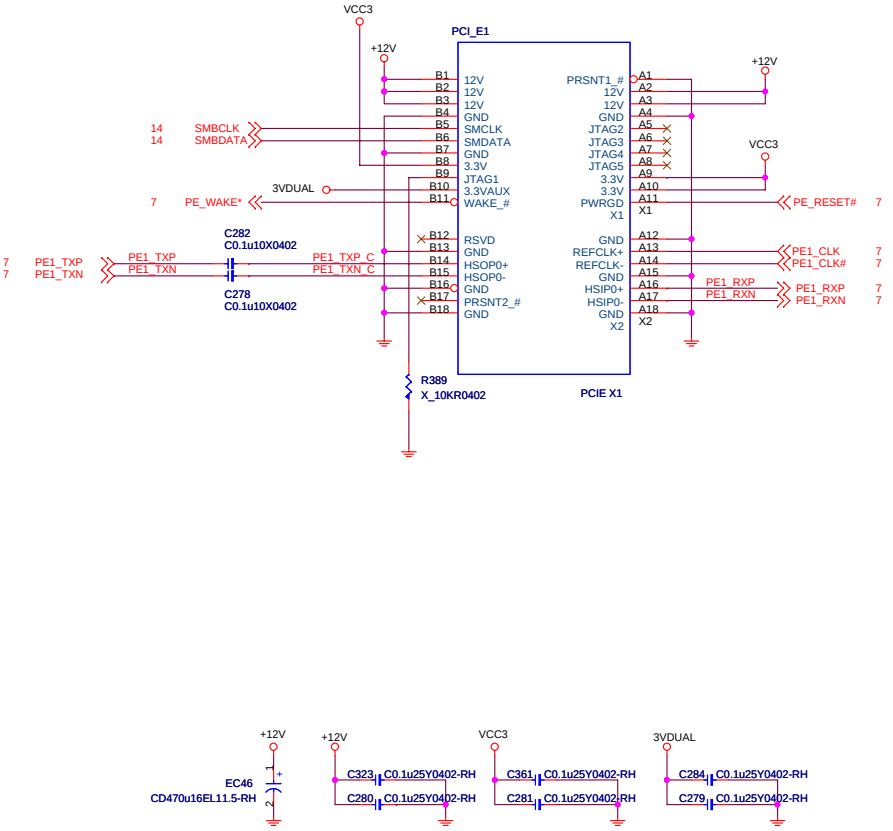
PCI-Express X16 Primary Slot
X16/X8



PCI-Express x1 SLOT 1



MICRO-STAR INT'L CO.,LTD		
MS-7393-1.1--080118K1		
Size: Custom	Document Description: PCI-E X16/X1 Slot	Rev: 0A
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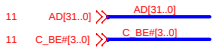
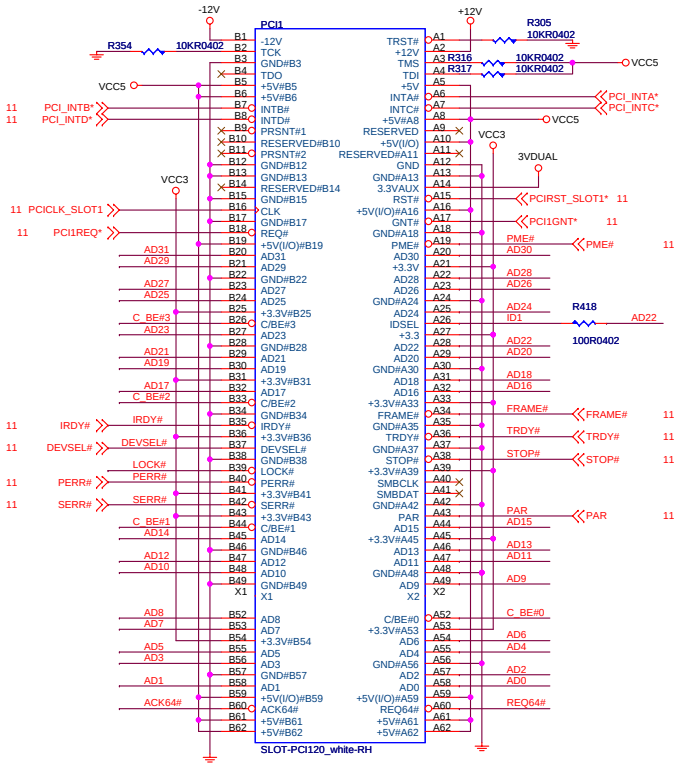
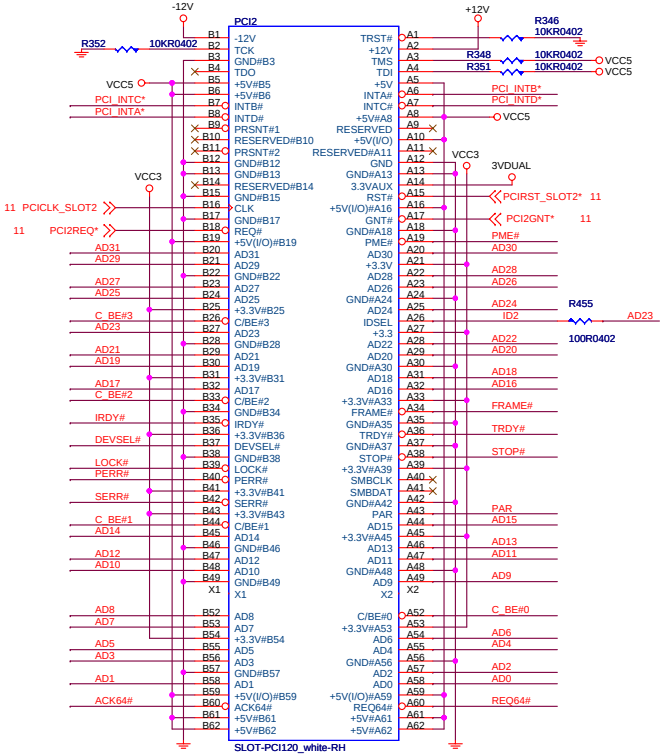


PCI SLOT 1 (PCI VER: 2.2 COMPLY)



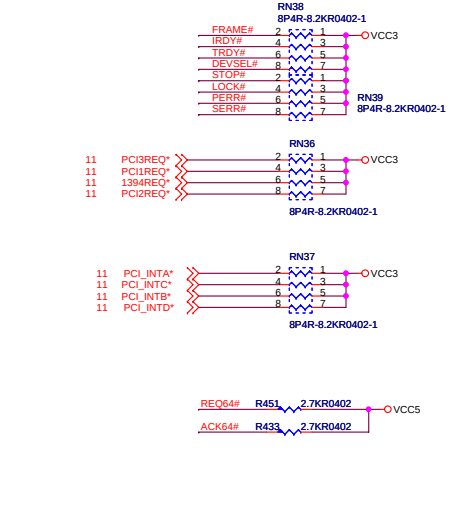
IDSEL = AD22
MASTER = PCI1REQ*
PCI1GNT*

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD23
MASTER = PCI2REQ*
PCI2GNT*

PCI PULL-UP / DOWN RESISTORS



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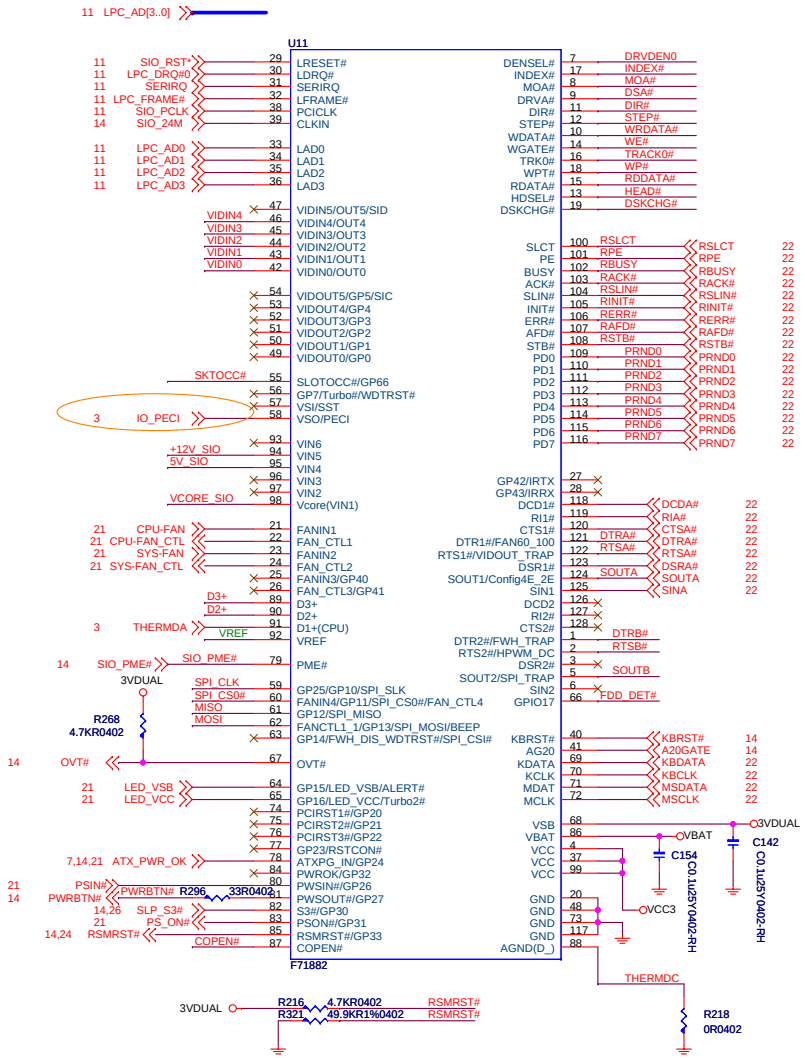
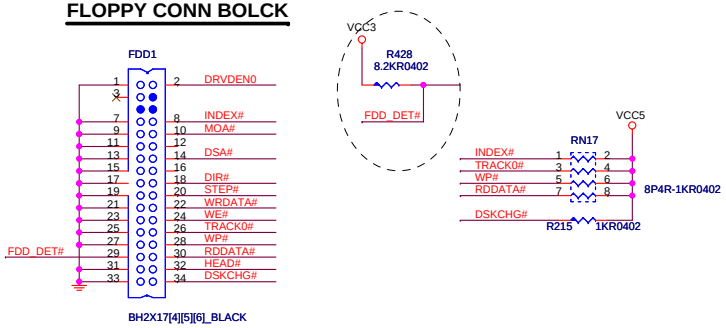
Super I/O

LPC SUPER I/O F71882

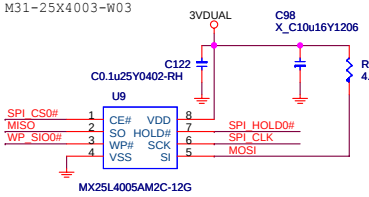


FLOPPY CONN BOLCK

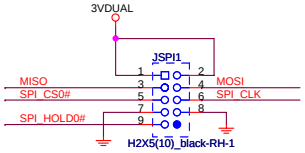


SPI 4M FLASH ROM

M31-25L4002-M24
M31-25X4003-W03

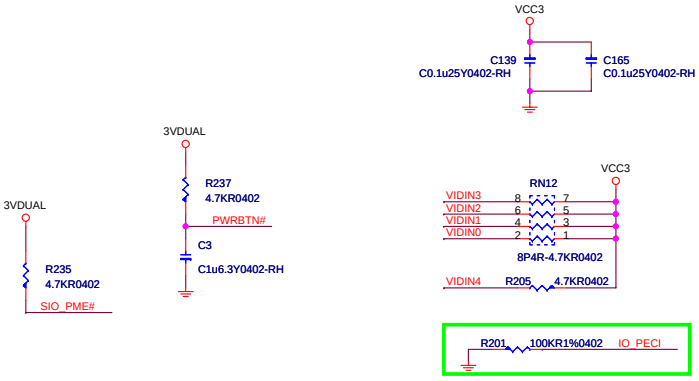


SPI DEBUG PORT

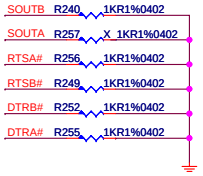


Part Number : N31-2051451-H06

Place close to SPI ROM



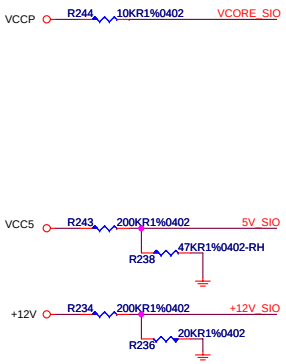
Strapping



	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRB#,SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

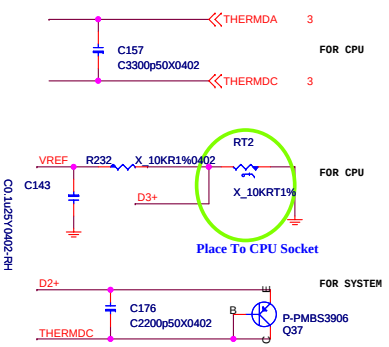
VOLTAGE SENSING(H/W Monitor).

The best voltage input level is about 1V.

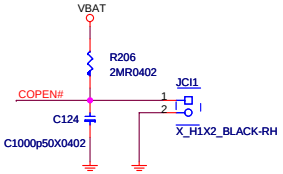


Temperature Sensing

DIODE SENSING CIRCUIT



CASE OPEN CIRCUIT



CPU VID reset

SLOT_OCC#

MICRO-STAR INT'L CO.,LTD

MS-7393-1.1--080118K1

Size	Document Description	Rev
Custom	LPC-Super I/O F71882FG	0A
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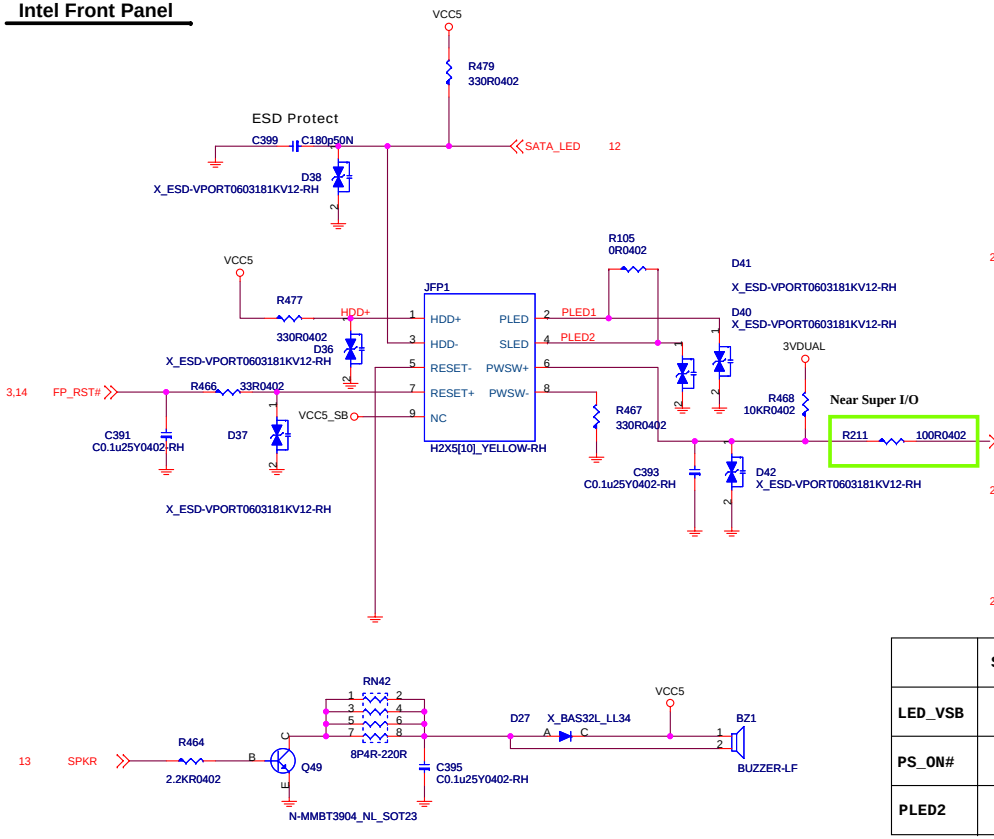
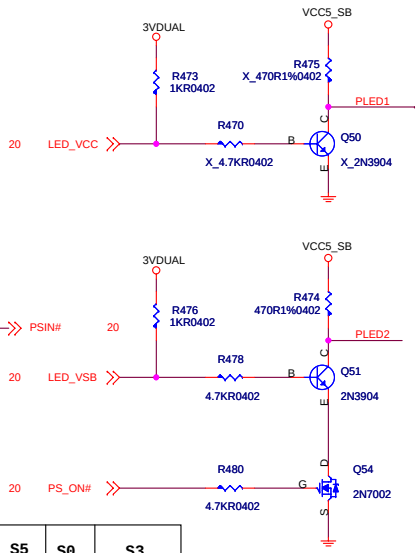
ATX connector / Front Panel

Intel Front Panel

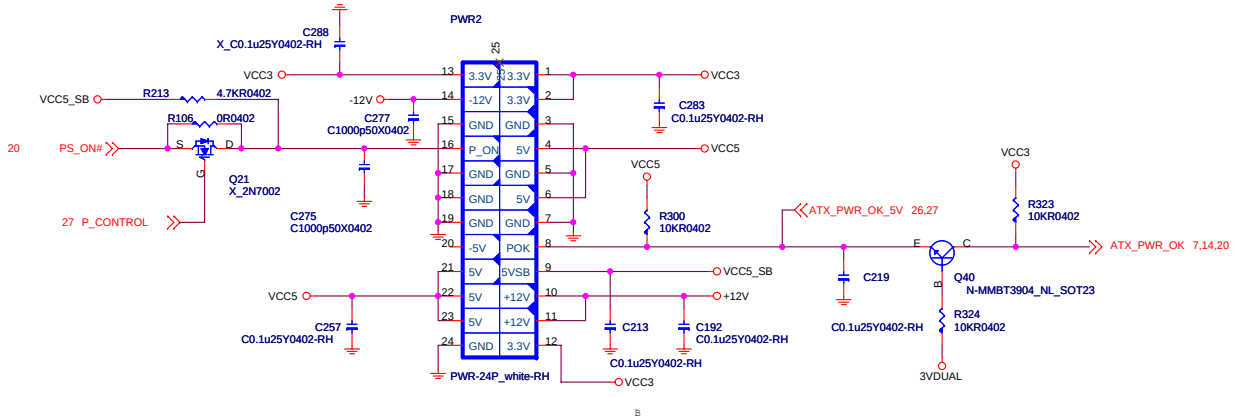


LED (for Fintek 71882)

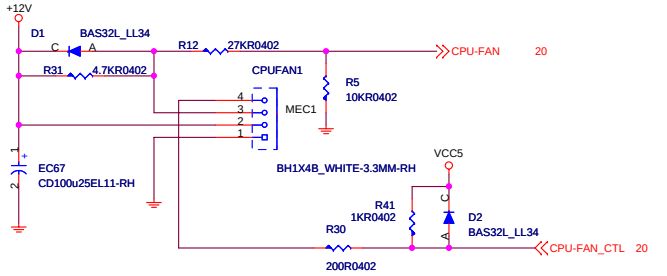


	S5	S0	S3
LED_VSB	H	H	BLINK
PS_ON#	H	L	H
PLED2	L	H	BLINK

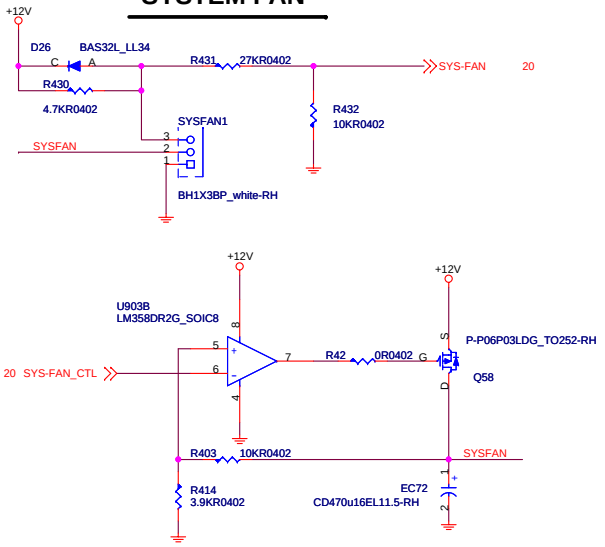
ATX Connector



CPU FAN



SYSTEM FAN



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: ATX/Front Panel/FAN
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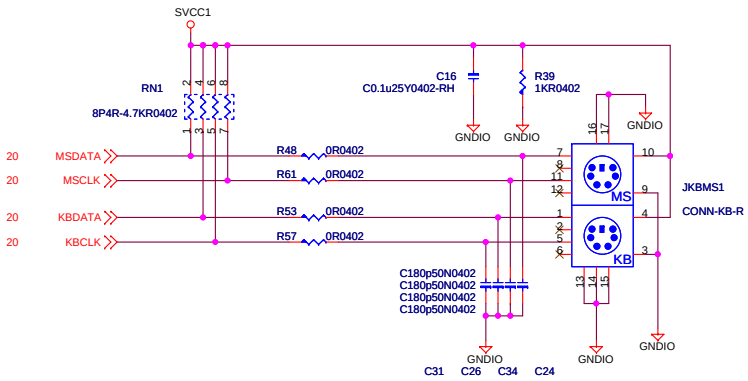
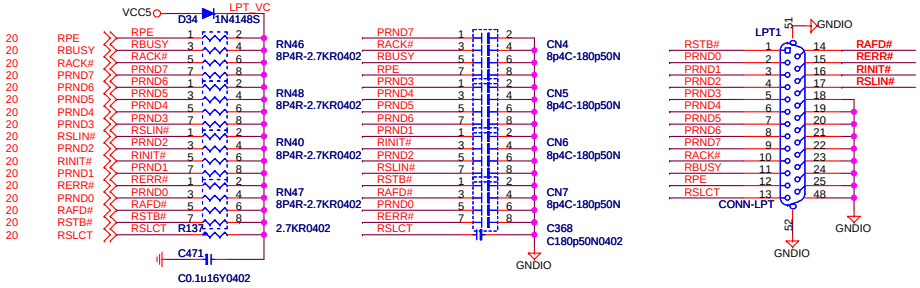
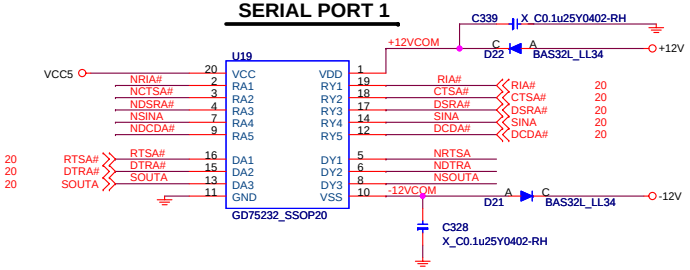
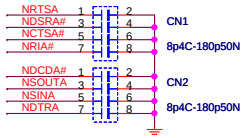
PS2 KEYBOARD & MOUSE CONNECTOR

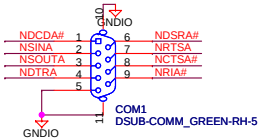




SERIAL PORT 1







MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7393-1.1--080118K1	
Size: Custom	Document Description: KB/COM1/IDE/FAN	Rev: 0A
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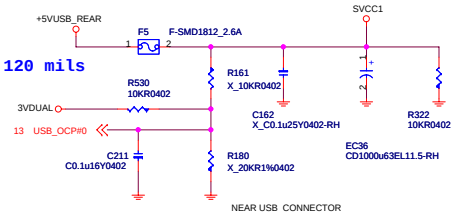
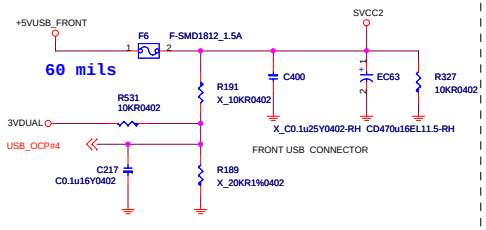
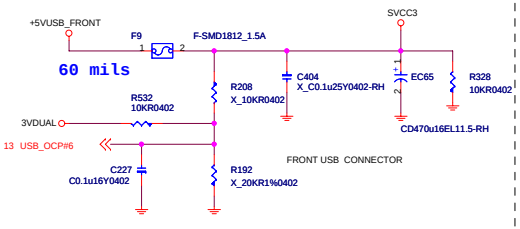
POWER CIRCUIT FOR USB PORT 0,1,2,3



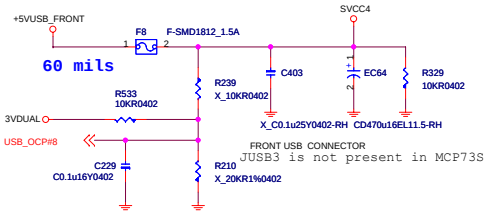
POWER CIRCUIT FOR USB PORT 4,5



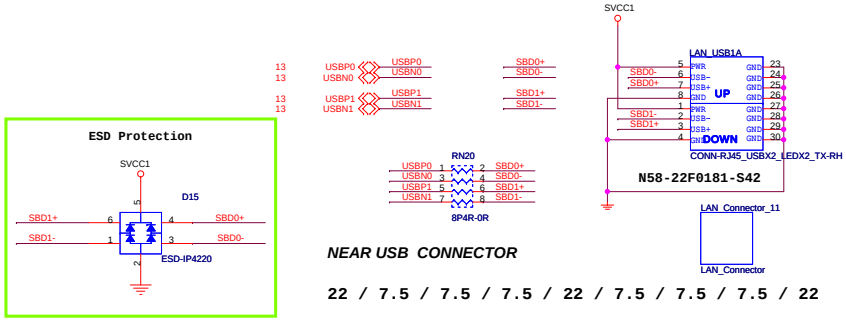
POWER CIRCUIT FOR USB PORT 6,7



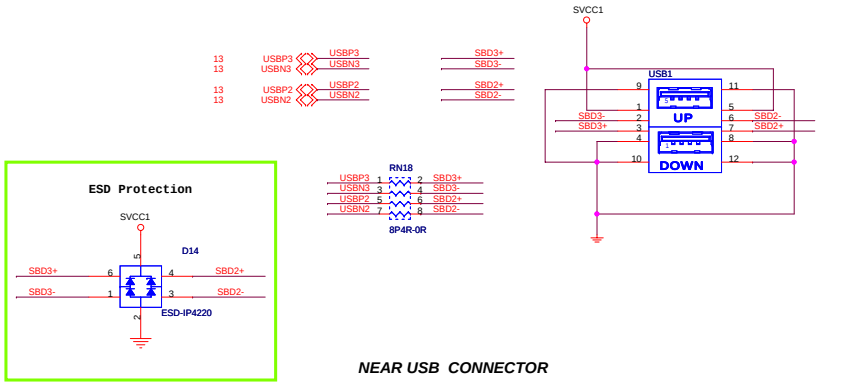
POWER CIRCUIT FOR USB PORT 8,9



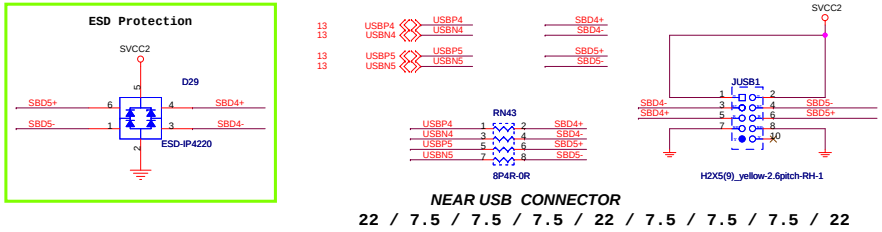
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



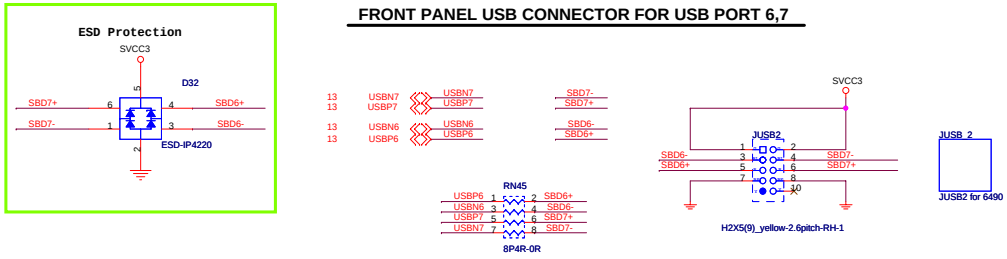
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



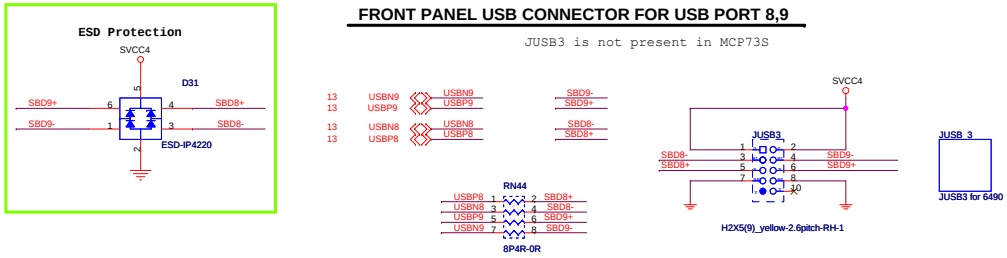
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



JUSB3 is not present in MCP73S

MSI	MICRO-STAR INT'L CO.,LTD	
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Size C	Document Description: USB Connectors	Rev 0A
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RTL8211BL-GR

R series within 500mil of PHY.

For EMI near Pin34

FOR RTL8211 can use LL4148: D01-4148S10-F01

Reserve L8 for EMI

RTL8211BL: (2.49K)
R11-2491T12-W08

Layout close to PIN1

Reserved for EMI
Bypass the clock to GND

N58-22F0181-S42

Giga-Lan
N58-22F0181-S42

Link Yellow
Active Blinking
1000 Orange
100 Green
10 None

Reserved for EMI
C184,C193,C174

For EMI
C435,C440,C438,C439,C436 must Load

For EMI close to Q31

For EMI close to Q44

Reserved for EMI
AVDD18,AVDD15 more than three cap(.1u)

Add for EMI
R282,R283

Normal -> to GND.
Delay TX/RX -> to 3VDUAL.

WOL LEVEL	DESCRIBE
S4/S5 H/L	WOL ENABLE/DISABLE DEFINE IN BIOS SETUP(DEFAUL :LOW)
S0/S3 HIGH	LAN ENABLE
S3 HIGH	LAN ENABLE

MICRO-STAR INT'L CO.,LTD

MS-7393-1.1--080118K1

Size: Custom | Document Description: LAN-RTL8211B | Rev: 0A

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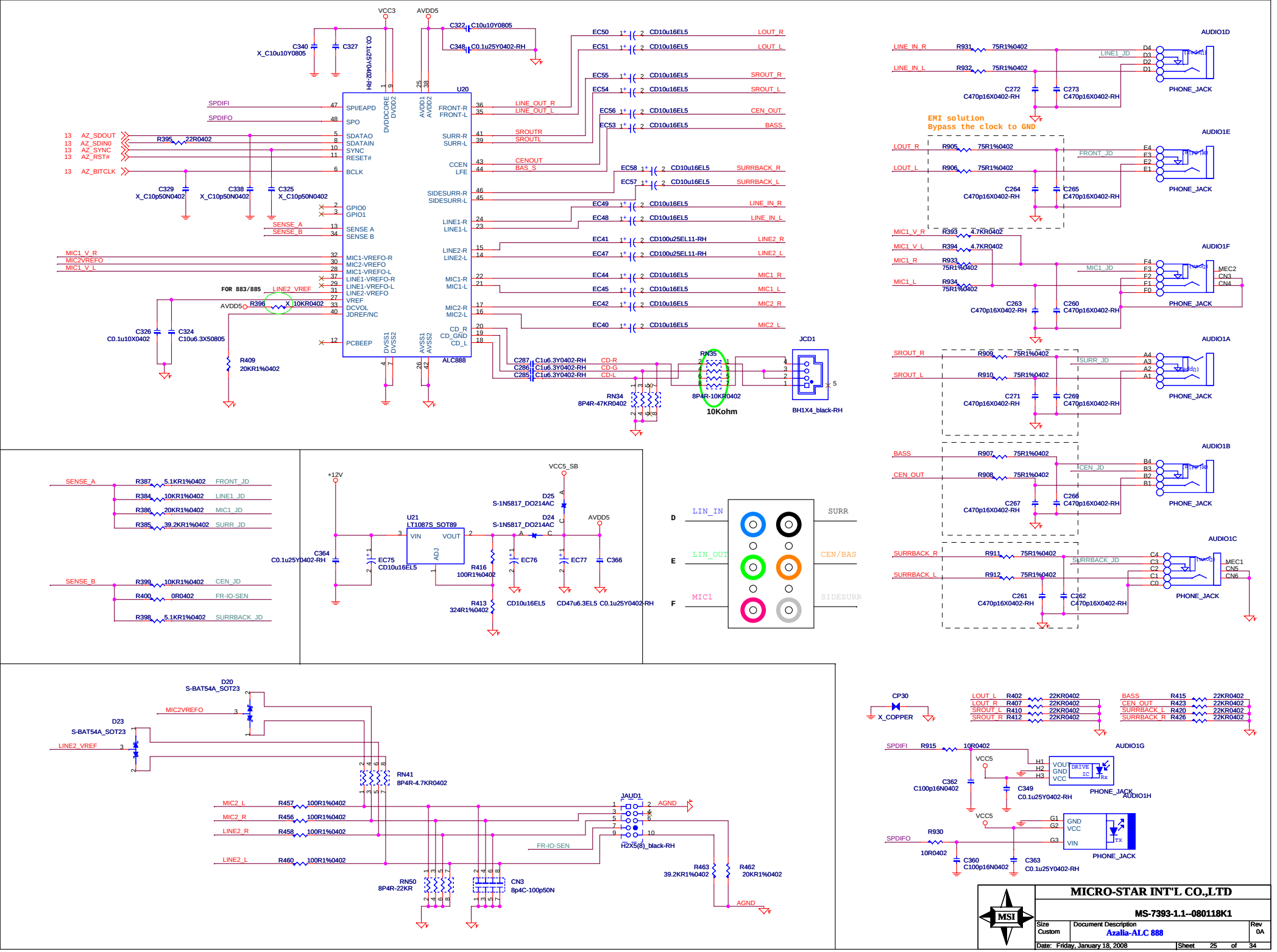
VCC3
AVDD5
C340 X_C10u10Y0805
C327
C322 C10u10Y0805
C348 C0.1u25Y0402-RH
U20
ALC888
SPDIFI
SPDIFO
AZ_SDOUT
AZ_SDIN0
AZ_SYNC
AZ_RST#
AZ_BITCLK
R395 22R0402
C329 X_C10p50N0402
C338 X_C10p50N0402
C325 X_C10p50N0402
SENSE_A
SENSE_B
MIC1_V_R
MIC2VREFO
MIC1_V_L
FOR 883/885
LINE2_VREF
R396 X 10KR0402
C326 C0.1u10X0402
C324 C10u6.3X50805
R409 20KR1%0402
PCBEEP
LINE_OUT_R
LINE_OUT_L
SROUTR
SROUTL
CENOUT
BAS_S
LINE1_R
LINE1_L
LINE2_R
LINE2_L
MIC1_R
MIC1_L
MIC2_R
MIC2_L
CD_R
CD_GND
CD_L
EC50 CD10u16EL5 LOUT_R
EC51 CD10u16EL5 LOUT_L
EC55 CD10u16EL5 SROUT_R
EC54 CD10u16EL5 SROUT_L
EC56 CD10u16EL5 CEN_OUT
EC53 CD10u16EL5 BASS
EC58 CD10u16EL5 SURRBACK_R
EC57 CD10u16EL5 SURRBACK_L
EC49 CD10u16EL5 LINE_IN_R
EC48 CD10u16EL5 LINE_IN_L
EC41 CD100u25EL11-RH LINE2_R
EC47 CD100u25EL11-RH LINE2_L
EC44 CD10u16EL5 MIC1_R
EC45 CD10u16EL5 MIC1_L
EC42 CD10u16EL5 MIC2_R
EC40 CD10u16EL5 MIC2_L
C287 C1u6.3Y0402-RH CD-R
C286 C1u6.3Y0402-RH CD-G
C285 C1u6.3Y0402-RH CD-L
RN34 8P4R-47KR0402
RN35 8P4R-10KR0402
10Kohm
JCD1
BH1X4_black-RH
AUDIO1D
AUDIO1E
AUDIO1F
AUDIO1A
AUDIO1B
AUDIO1C
LINE_IN_R R931 75R1%0402
LINE_IN_L R932 75R1%0402
LINE1_JD
PHONE_JACK
C272 C470p16X0402-RH
C273 C470p16X0402-RH
EMI solution
Bypass the clock to GND
LOUT_R R905 75R1%0402
LOUT_L R906 75R1%0402
FRONT_JD
C264 C470p16X0402-RH
C265 C470p16X0402-RH
MIC1_V_R R393 4.7KR0402
MIC1_V_L R394 4.7KR0402
MIC1_R R933 75R1%0402
MIC1_L R934 75R1%0402
MIC1_JD
MEC2
CN3
CN4
C263 C470p16X0402-RH
C260 C470p16X0402-RH
SROUT_R R909 75R1%0402
SROUT_L R910 75R1%0402
SURR_JD
C271 C470p16X0402-RH
C269 C470p16X0402-RH
BASS R907 75R1%0402
CEN_OUT R908 75R1%0402
CEN_JD
C267 C470p16X0402-RH
C266 C470p16X0402-RH
SURRBACK_R R911 75R1%0402
SURRBACK_L R912 75R1%0402
SURRBACK_JD
MEC1
CN5
CN6
C261 C470p16X0402-RH
C262 C470p16X0402-RH
SENSE_A R387 5.1KR1%0402 FRONT_JD
R384 10KR1%0402 LINE1_JD
R386 20KR1%0402 MIC1_JD
R385 39.2KR1%0402 SURR_JD
SENSE_B R399 10KR1%0402 CEN_JD
R400 0R0402 FR-IO-SEN
R398 5.1KR1%0402 SURRBACK_JD
+12V
VCC5_SB
U21 LT1087S_SOT89
VIN
VOUT
ADJ
D25 S-1N5817_DO214AC
D24 S-1N5817_DO214AC
C364 C0.1u25Y0402-RH
EC75 CD10u16EL5
R416 100R1%0402
EC76
EC77
C366
R413 324R1%0402
CD10u16EL5
CD47u6.3EL5
C0.1u25Y0402-RH
D
E
F
LIN_IN
LIN_OUT
MIC1
SURR
CEN/BAS
SIDESURR
D20 S-BAT54A_SOT23
D23 S-BAT54A_SOT23
MIC2VREFO
LINE2_VREF
RN41 8P4R-4.7KR0402
MIC2_L R457 100R1%0402
MIC2_R R456 100R1%0402
LINE2_R R458 100R1%0402
LINE2_L R460 100R1%0402
JAUD1
AGND
FR-IO-SEN
HI2X5(8)_black-RH
R463 39.2KR1%0402
R462 20KR1%0402
RN50 8P4R-22KR
CN3 8p4C-100p50N
CP30
X_COPPER
LOUT_L R402 22KR0402
LOUT_R R407 22KR0402
SROUT_L R410 22KR0402
SROUT_R R412 22KR0402
BASS R415 22KR0402
CEN_OUT R423 22KR0402
SURRBACK_L R420 22KR0402
SURRBACK_R R426 22KR0402
SPDIFI R915 10R0402
SPDIFO R930 10R0402
AUDIO1G
AUDIO1H
VCC5
C362 C100p16N0402
C349 C0.1u25Y0402-RH
C360 C100p16N0402
C363 C0.1u25Y0402-RH
PHONE_JACK
MICRO-STAR INT'L CO.,LTD
MS-7393-1.1--080118K1
Size Custom
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Azalia-ALC 888
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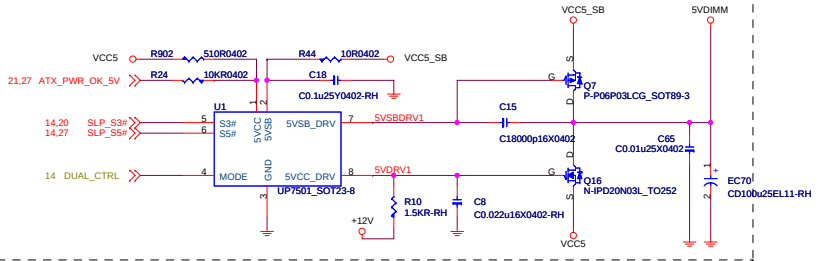
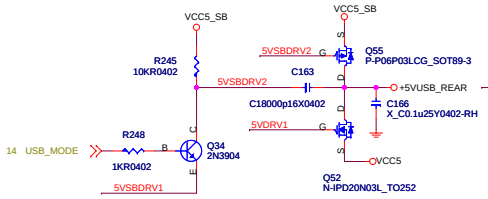
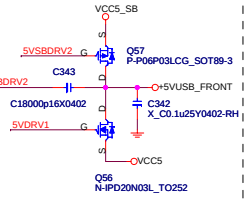
5VDIMM FOR DDR



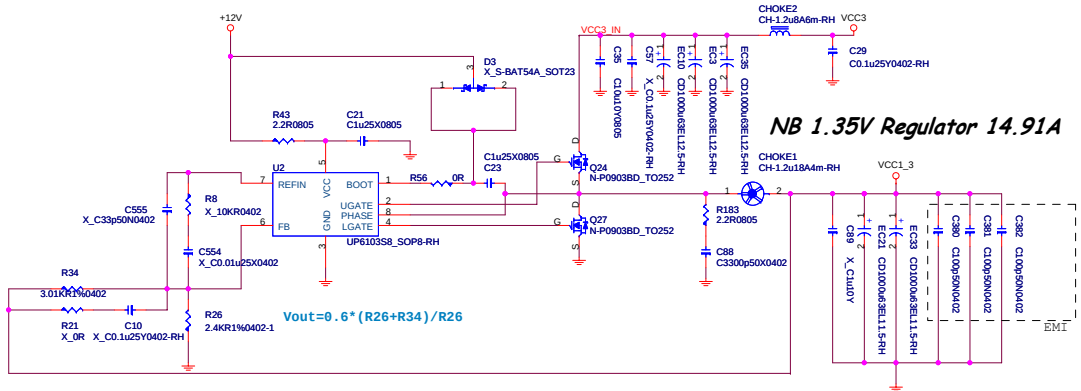
5VSB FOR Rear USB



5VSB FOR Front USB



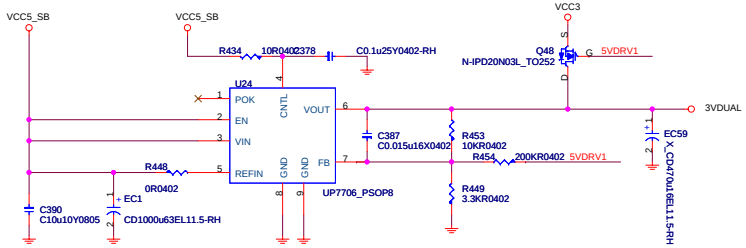
NB 1.35V Regulator 14.91A



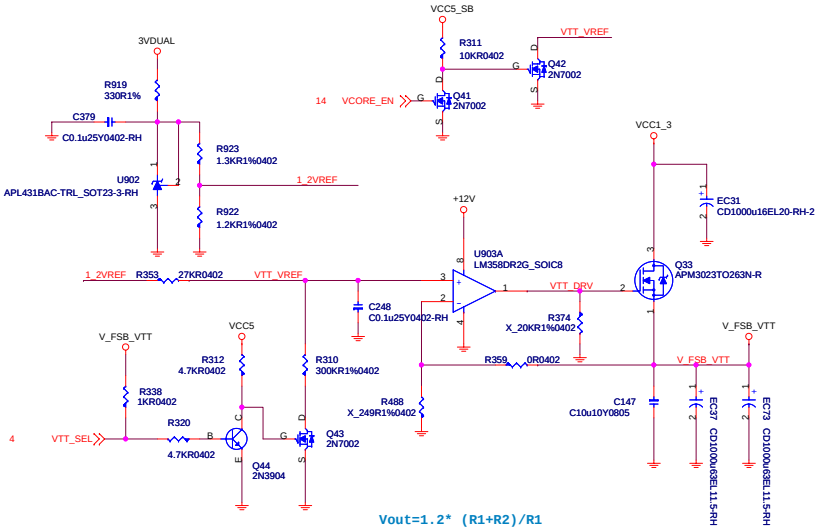
R34 3.01K(R11-3011T12-W08)-->1.35V
2.4K(R11-0242T22-W08)-->1.2V

5VSB

3VDUAL, ?A

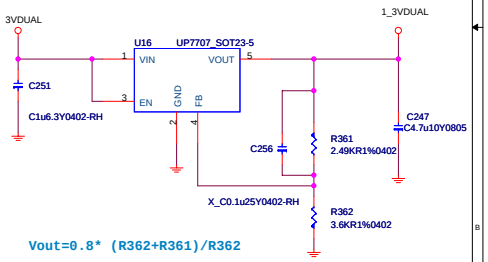


V_FSB_VTT



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

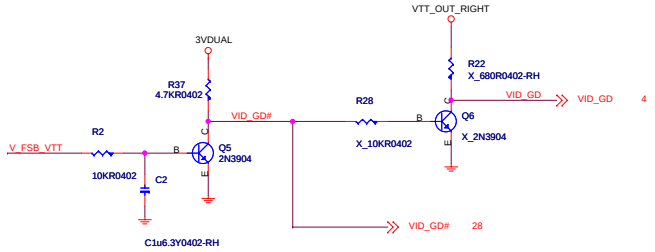
1_3VDUAL, 25mA



R362 3.6K(R11-0362T12-W08)-->1.35V
4.99K(R11-4991T12-R01)-->1.2V

	S0	S3	S4			S5		
DUAL_CTRL	X	X	0	1	1	0	1	1
5VSBDRV1	1	0	1	0	0	1	0	0
5VDRV1	1	0	0	0	0	0	0	0
5VSBDRV2	X	0	1	0	0	1	0	0
USB_MODE	X	1	X	1	0	X	1	0
5VDIMM	Y	Y	N	Y	N	N	Y	N
USB power	Y	Y	N	Y	N	N	Y	N

VID_GD# to PWM and VID_GD to CPU
for VRM10 power sequence.



MICRO-STAR INT'L CO.,LTD

MS-7393-1.1--080118K1

Size: Custom | Document Description: ACPI Controller | Rev: 0A

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DDR II 1.8V POWER

Tripple=7.7*0.6*0.8/1=3.70A
2.35*2*1.7=7.99>3.70A

CHOKE4
CH-1.2u8A6m-RH

5VDIMM_IN → 5VDIMM

C52 C10u10Y0805
EC18 CD1000u16EL20-RH-2
EC8 1000u/16V8*20
C561 C0.01u25X0402
C562 C0.01u25X0402
C59 C0.01u25X0402
C559 C0.01u25X0402
C560 C0.01u25X0402
C51 C0.1u25Y0402-RH

EMI Ver1.1

D4 S-BAT54C_SOT23
D5 X_S-BAT54A_SOT23
+12V
R89 0R → 5VDIMM
R94 X_0R → VCC5_SB
R72 X_0R
R91 2.2R0805
C63 C1u25X0805
C53 C1u25X0805

U5 UP6103S8_SOP8-RH
REFIN, VCC, BOOT, UGATE, PHASE, LGATE, GND, FB
R90 0R
phase
C5 X_C1u6.3Y0402-RH
R35 2KR1%0402
R25 X_0R
C12
R27 1KR1%0402
X_C0.1u25Y0402-RH

Q25 N-P0903BD_TO252
Q28 N-P0903BD_TO252

CHOKE5
CH-1.2u18A4m-RH
R184 2.2R0805
C114 C3300p50X0402

VCC_DDR
C59 X_C1u10V
EC39 CD1000u63EL11.5-RH
EC68 CD1000u63EL11.5-RH
C170 C10u6.3X50805
C191 C10u6.3X50805

NEAR DIMM1
EC43 CD1000u63EL11.5-RH
VCC5
EC71 X_CD470u16EL11.5-RH

VCC5_SB
R1 1KR0402
Q1 2N7002
Q2 2N3904
14,26 SLP_S5#
R19 1KR0402

VTT_DDR

To CPU Copper trace width > 200mils

0.6A

3VDUAL
U6 W83310DG_SOP8-RH
VREF2, ENABLE, VCNTL, BOOT_SEL, VIN, GND, VREF1, VOUT, GND
VCC_DDR
C73 C0.1u10X0402
C66
C359 C0.1u10X0402
VTT_DDR
R125 1KR1%0402
R138 1KR1%0402
0.9V/1.2A
EC66 CD1000u63EL11.5-RH
X_C0.1u25Y0402-RH

VCC1_5

VCC3
U22 UP7707_SOT23-5
VIN, VOUT, EN, GND, FB
C346 C1u6.3Y0402-RH
C345
R405 2.49KR1%0402
R100 1KR0402
C344 C4.7u6.3X50805
X_C0.1u25Y0402-RH
R903 2.8KR1%0402
VCC1_5
H_VCCPLL => 100m A
Vout=0.8* (R1+R2)/R1

3VDUAL
R469 330R0402
LED1 GREEN
POWER LED

The power OFF-ON solution

VCC5_SB
R98 X_4.7KR0402
R92 X_0R0402
R935 X_100R0402
U908A
U908B
CLR, D, CLK, PRE, Q, VCC, GND
21,26 ATX_PWR_OK_5V
X_F74_SOIC14
P_CONTROL 21
R95 X_4.7KR0402
R96 X_4.7KR0402
Q62 X_2N3904
Q63 X_2N3904
R357 X_10KR0402
+12V

MICRO-STAR INT'L CO.,LTD
MS-7393-1.1--080118K1
Size: Custom
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Voltage Regular Module

N-P0903BDG_TO252	mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5mΩ(10V/25A),Vgs(on) =1~3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs=±20V,RoHS compliance
P75N02LDG/TO252	mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7mΩ(@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs=±20V,RoHS compliance
C100U2SP	ESR<13mΩ,Ripple cur.<2.7A,LC<12uA,105C
CD560U4OS-2	CAP,OS-CON,560u/4V,Dip-2/8*9/3.5mm,ESR<7mohm, Ripplecur.=6100mA ,Lc. <500uA,SPEC series,RoHS compliance
1800UF/6.3V	ESR<12mΩ, Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.25uH/40A	,IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
CH-1.1U25A-LF	IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CD1000U16EL20-2	CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE

0.8375~1.6V / 125A

CP25,CP26,CP27,CP28 PLACE ON THE SOLDER SIDE, CLOSE TO INDUCTOR

Place close to inductor

BOTTOM PAD CONNECT TO GND

Pin9 of A0 = 0 ; I2C = 1000110X = 8C
Pin9 of A0 = 1 ; I2C = 1000111X = 8E

OS-CON Capactiors

SP Capacitors

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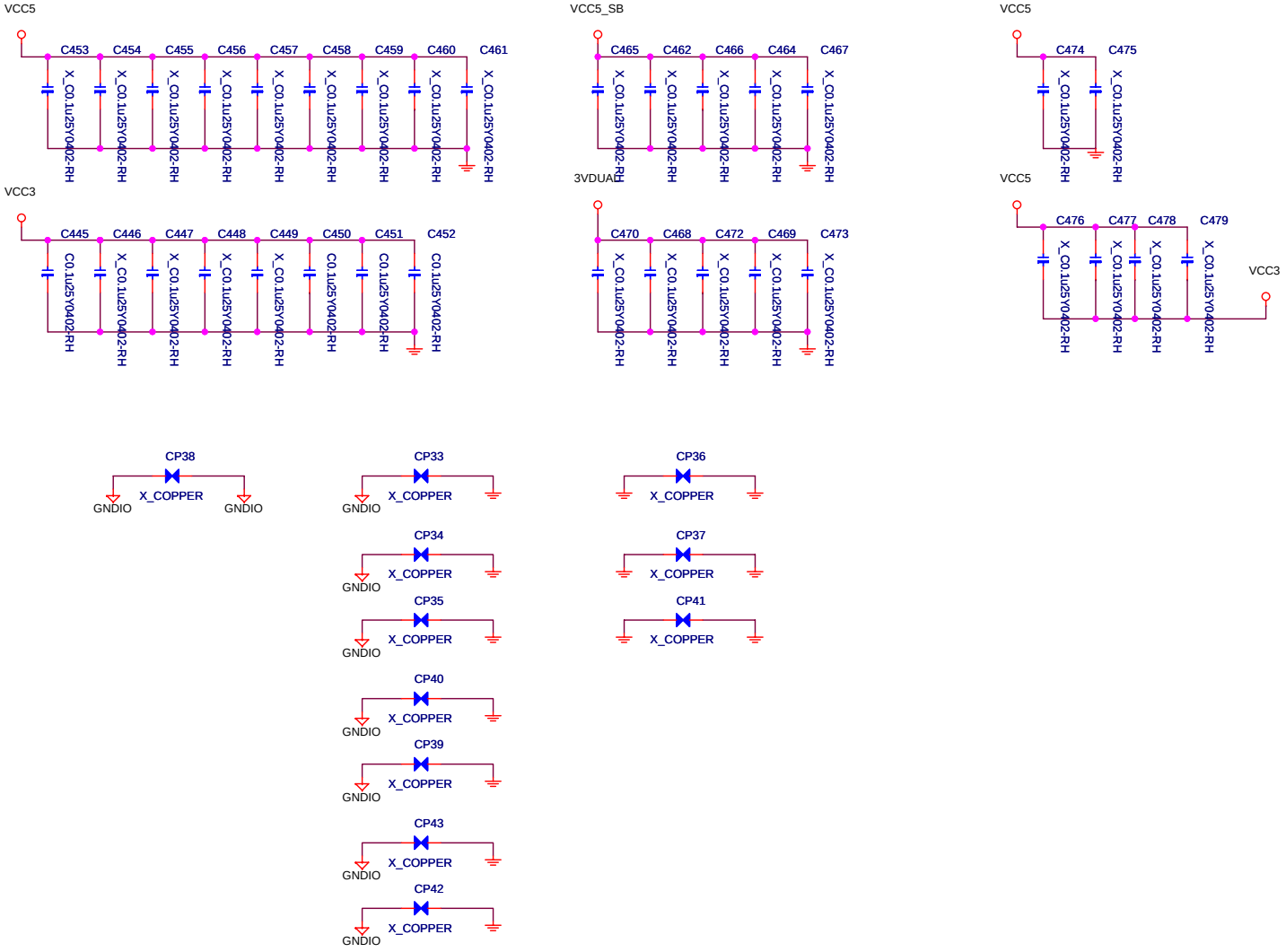
EMI



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U8_X1

MSI DDR

MCP_HEATSINK

暫用E31-0401580-K08

VBAT-S1

BAT-BCR2032P-RH

PCB1

PCB

P30-0739311-G37

AVL P30-0739311-E48

PCB1.0

PCB

AVL P30-0739310-E48

JP1

JUMPER-1X2A_GREEN-RH

Label-1

Pb-Free

Label-2

TA No

Label-3

LG Logo

Label-4

bios

Simulation

VCC5

X_JS1

SIM1

X_PIN1*2

X_JS2

SIM2

X_PIN1*2

Optics Orientation Holes

FM1 X_FM

FM2 X_FM

FM5 X_FM

FM6 X_FM

FM8 X_FM

FM9 X_FM

FM10 X_FM

FM11 X_FM

FM12 X_FM

FM3 X_FM

FM13 X_FM

FM4 X_FM

FM7 X_FM

Mounting Holes

MH1

MH2

MH3

MH4

MH5

MH6

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MCP73 GPIO Config.

Contol Register	Primary Signal	Secondary Function	Tertiary Funtion	Default State
C1	GPIO_2	NMI	PS2_CLK0	GPIO Input
C2	GPIO_3	SMI#	PS2_DATA0	GPIO Input
C3	GPIO_4	SCI/INTR	PS2_CLK1	GPIO Input
C4	GPIO_5	INT#	PS2_DATA1	GPIO Input
C5	GPIO_6	FERR#/SYS_SERR#	IGPU_GPIO_6	GPIO Input
C6	GPIO_7	NFERR#/SYS_PERR#	IGPU_GPIO_7	GPIO Input
C7	GPIO_8		SPI_DI	Tertiary Function
C8	GPIO_9		SPI_DO	Tertiary Function
C9	GPIO_10		SPI_CS0	Tertiary Function
CA	GPIO_11		SPI_CLK	Tertiary Function
D2	LPC_DRQ1#	GPIO_19	FANRPM1	GPIO Input
D3	PROCHOT#	GPIO_20		Primary Function
D4	PE_WAKE#	GPIO_21		Primary Function
D5	HDA_SDATA_IN0	GPIO_22		Primary Function
D6	HDA_SDATA_IN1	GPIO_23	MGPIO_0	Primary Function
D7	HDA_SDATA_IN2	GPIO_24	MGPIO_2	Primary Function
D8	USB_OC0#	GPIO_25		Primary Function
D9	USB_OC1#	GPIO_26		Primary Function
DA	USB_OC2#	GPIO_27		Primary Function
DB	USB_OC3#	GPIO_28	MGPIO_1	Primary Function
DC	USB_OC4#	GPIO_29	MGPIO_3	Primary Function
DD	PCI_PME#	GPIO_30		Primary Function
DE	SIO_PME#	GPIO_31	SPI_CS2	Primary Function
DF	EXT_SMI#	GPIO_32		Primary Function
E1	SUS_CLK	GPIO_34		Primary Function
E2	MII0_INTR	GPIO_35	PWR_LED#	Primary Function
E3	MII0_RXER	GPIO_36		Primary Function
E4	MII0_PWRDWN	GPIO_37		Primary Function
E5	PCI_REQ3#	GPIO_38	RS232_CTS#	GPIO Input
E6	PCI_GNT3#	GPIO_39	RS232_RTS#	GPIO Output High
E7	PCI_REQ2#	GPIO_40	RS232_DSR#	GPIO Input
E8	PCI_GNT2#	GPIO_41	RS232_DTR#	GPIO Output High
E9	PCI_CLKRUN#	GPIO_42		Primary Function
EA	PCI_PERR#	GPIO_43	RS232_DCD#	GPIO Input
EB	HDA_SYNC	GPIO_44		Primary Function
EC	HDA_SDATA_OUT	GPIO_45		Primary Function
F1	LPC_DRQ0#	GPIO_50		Primary Function
F3	PCI_REQ4#	GPIO_52	RS232_SIN#	GPIO Input
F4	PCI_GNT4#	GPIO_53	RS232_SOUT#	GPIO Output High
F6	A20GATE	GPIO_55		Primary Function
F7	KBRDSTIN#	GPIO_56		Primary Function
F8	SATA_LED#	GPIO_57		Primary Function
F9	THERMTRIP	GPIO_58		Primary Function
FA	THERM#	GPIO_59		Primary Function
FB	FANRPM0	GPIO_60		Primary Function
FC	FANCTL0	GPIO_61		Primary Function
FD	FANCTL1	GPIO_62		Primary Function
FE	CABLE_DET_P	GPIO_63		Primary Function

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA* PCI_INTB* PCI_INTC* PCI_INTA*	PCI1REQ* PCI1GNT*	AD22	PCICLK_SLOT1
PCI Slot 2	PCI_INTB* PCI_INTC* PCI_INTD* PCI_INTA*	PCI2REQ* PCI2GNT*	AD23	PCICLK_SLOT2

DDRII DIMM Config.

DIMM1	DIMM2
A0 1010000B	A2 1010001B
0A	1A

SIO GPIO FUNCTION

NAME	Function Description
FANIN1	CPU-FAN
FAN_CTL1	CPU-FAN_CTL
FANIN2	SYS-FAN
FAN_CTL2	SYS-FAN_CTL
FANIN3	NB-FAN

MCP73 GPIO FUNCTION

NAME	Function Description
GPIO_2	DUAL_CTRL
GPIO_3	USB_MODE
GPIO_23	CPU_GTLREF1_SEL

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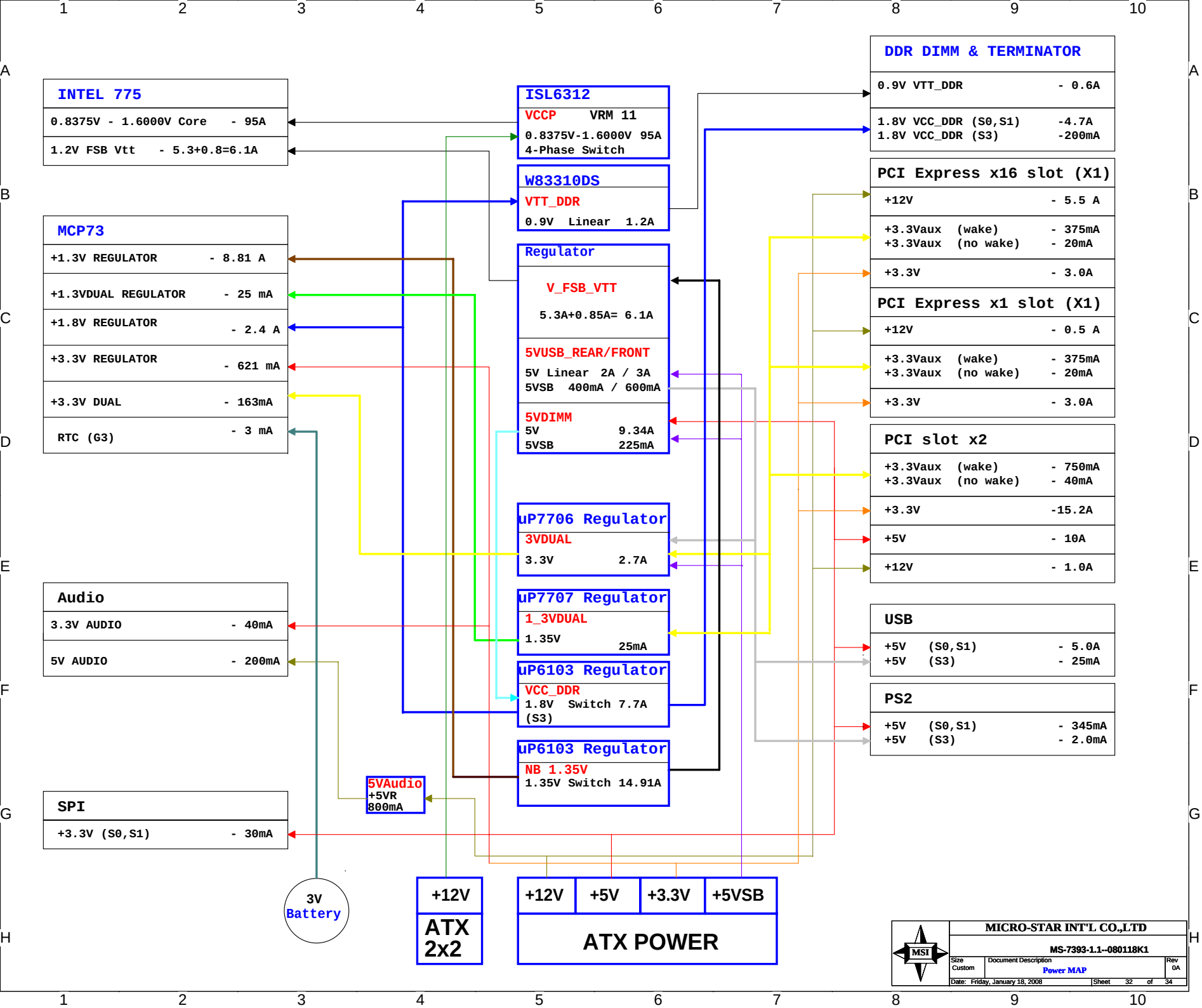
INTEL 775
0.8375V - 1.6000V Core - 95A
1.2V FSB Vtt - 5.3+0.8=6.1A
MCP73
+1.3V REGULATOR - 8.81 A
+1.3VDUAL REGULATOR - 25 mA
+1.8V REGULATOR - 2.4 A
+3.3V REGULATOR - 621 mA
+3.3V DUAL - 163mA
RTC (G3) - 3 mA
Audio
3.3V AUDIO - 40mA
5V AUDIO - 200mA
SPI
+3.3V (S0,S1) - 30mA
3V Battery
ISL6312
VCCP VRM 11
0.8375V-1.6000V 95A
4-Phase Switch
W83310DS
VTT_DDR
0.9V Linear 1.2A
Regulator
V_FSB_VTT
5.3A+0.85A= 6.1A
5VUSB_REAR/FRONT
5V Linear 2A / 3A
5VSB 400mA / 600mA
5VDIMM
5V 9.34A
5VSB 225mA
uP7706 Regulator
3VDUAL
3.3V 2.7A
uP7707 Regulator
1_3VDUAL
1.35V 25mA
uP6103 Regulator
VCC_DDR
1.8V Switch 7.7A
(S3)
uP6103 Regulator
NB 1.35V
1.35V Switch 14.91A
5VAudio
+5VR
800mA
+12V
ATX 2x2
+12V
+5V
+3.3V
+5VSB
ATX POWER
DDR DIMM & TERMINATOR
0.9V VTT_DDR - 0.6A
1.8V VCC_DDR (S0,S1) -4.7A
1.8V VCC_DDR (S3) -200mA
PCI Express x16 slot (X1)
+12V - 5.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Express x1 slot (X1)
+12V - 0.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI slot x2
+3.3Vaux (wake) - 750mA
+3.3Vaux (no wake) - 40mA
+3.3V -15.2A
+5V - 10A
+12V - 1.0A
USB
+5V (S0,S1) - 5.0A
+5V (S3) - 25mA
PS2
+5V (S0,S1) - 345mA
+5V (S3) - 2.0mA
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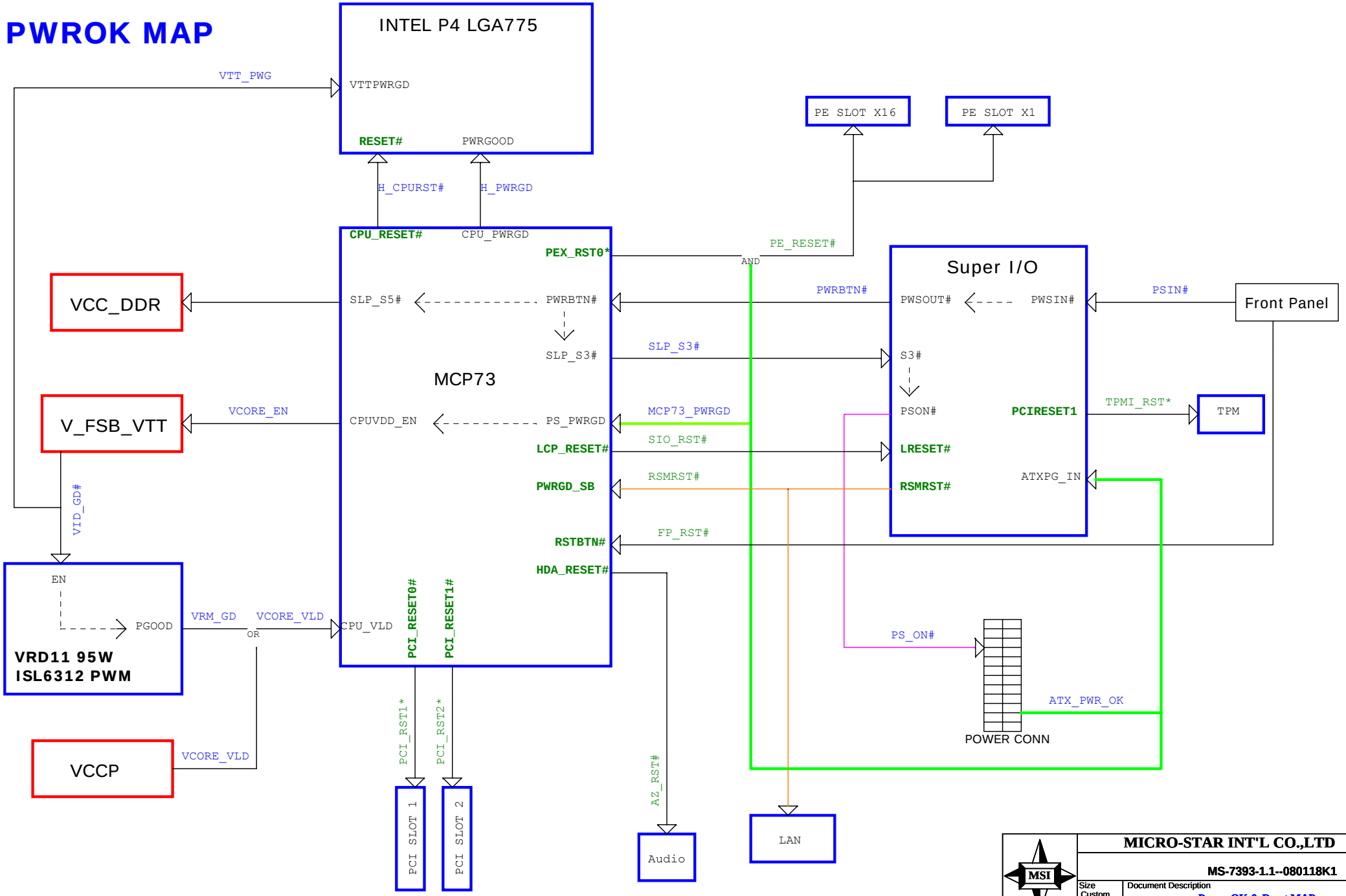
PWROK MAP



MSI	MICRO-STAR INT'L CO.,LTD	
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Ver.	Date	Change List	Page
0A	2007.0604	1.Add MCP73 strap option table in schematic	13
		2.Add standby LED	27
		3.Add GPIO table in schematic	31
		4.Add FDD detect function on pin29 of FDD connector	20
		5.Add SPDIF in/out	25
		6.Critical de-caps should be X7R type	
		7.GTLREF1 value in schematic it has been changed.	04
		8.LGE want to adopt 1W under in standby mode.	24
		9.Need pull up resistor when not used.	23
		10.TDI and TMS pull up to VCC,TRST pull down to GND	19
		11.Add 22ohm resistor near PHY of MII_TXCLK, RXCLK	24
		12.SMB_DATA0,1, CLOCK0,1 reserve 0 ohm resistor near MCP73	14
		13.AZ_RST reserve 10pF cap for AZ_RST	13
		14.V1P8_MEM_VDDP need 2 X 10uF (not 1uF)	27
		15.PS_PWRGD (RSMRST#) pull down to GND	20
		16.Connect PECI to Super I/O	03
		17. it can be leakage path of VCC5_SB to VCC5.	21
		18.Add ESD protection as MS-7372	21
		19.LG want to unify reau audio color as MS-7372 and MS-7342	25
		20.Add VSYNC, HSYNC signals need 3.3V to 5V buffer.	17
0B	2007.0801	1.VCC3_SB_LAN change to 3vdual (change to item 27)	13
		2.Nvidia release R226,225,222,224 from 33Ohm to 0 Ohm ; R219,214,152,148,223,221 unload	06
		3.Nvidia release Modify R209 from 62 Ohm to 200 Ohm	04
		4.Some SMPS do not work when quick AC ON/OFF solution	27
		5.The SIO pin LED_VCC can't work in S3 state, so we use the pin LED_VSB and PS_ON# to control the Power LED	21
		6.Load R249 for linier FAN	20
		7.Nvidia release JTAG_TCLK pull high to 3.3dual(R93) chip A02 cover it, so pull low(R297).	14
		8.VRM Modify ChangeR33 => 1.05k,R40 => 649R,R38 => 20k, R16 => 100R,R6 、R66、 R88 => 6.2k,C11 => 470pF, C19 => 1nF,C20 => 33pF Remove EC4、 EC5、 EC6 => N/C	28
		9.For VTT_PWG rise time keep <150ns solution (DA-03414-001_v01.pdf) P4. VTT_PWRGOOD area P14. Vcore power-on sequence control circuit	04.14
		10.Nvidia release(DA-02879-001_v02.pdf) CPU_GTLREF1 modify	04
		11.R324 pull-high from 5VSB to 3VDUAL	21
		12.C22 modify from 10u to EC67 100u; R30 from 0Ohm to 200Ohm; Load D41,D2	21
		13.Modify D16,D18 pull-high from 3VDUAL to VCC3	09
		14.RGB solution load C112,C111,C120 22p	17
		15.Unuse HDMI pull-high 10K(R390) to VCC3	07
		16.Nvidia release IDE_COMP_3P3V add .1u(C190) to GND	12
		17.Nvidia release MEM_0A_CKE0,MEM_0A_CKE1,MEM_0B_CKE0,MEM_0B_CKE1 pull 90.9Ohm to GND(R936,R937,R938,R939)	10
0B	2007.0801	18.Modify R404 from 22k to 10Kohm, Nvidia confirm	07
		19.RGMII MAC interface Page.13 pin E19,G19,F19 to GND Page.24 Modify R293 from 22 to 0 ohm	13,24
		20.Realtek Lan Current update Reserve R358,C203,C222,C216 Modfy C183,C253 from 10 u to 22u Add R282,R283	24
		21.Unload R936, R937, R938, R939	10
		22.Uunload R145,R158,R157 for Nvidia release VIL	04
		23.Add 0 ohm(R280) within MCP73	13
		24.Remove NB FAN	21
		25.Unload R152 for Nvidia release	04
		26.Add C379	26
		27.For Power Conconsumption Co-lay design 3VDUAL and VCC3_SB_LAN	13,15,24
		28.For Nvidia release for VGA solution C112,C111,C120 change from 22P to 5.6P C102,C104,C115 change from 10P to 5.6P L9,L10,L11 change from 68n to 100n C69,C70 from unload 47P to load 12P	17
		29.Unload R292,R281 Load C214,C212,Y3	24
1.0	2007.0920	1.OVT# solution The OVT# from SIO to MCP73	20,14
		2.power off-on issue solution update U908 BOM from F to HC; R92 from 4,7k to 0 ohm; R300,323,324 from 10k to 1k; ATX_PWR_OK change to ATX_PWR_OK_5V	27
		3.Add EC70 for 5VDIMM drop when S0 to S3 solution	26
		4.EMI Solution Remove CP10, load L8 Modify C228, C240, C237 from 10P to 22P Modify C184, C189, C193 ,C174 to 104P	24
		5.Nvidia release DDC_DATA3 and DDC_CLK3 must pull-high 10K to VCC3 when unuse.	07
		6. Load EC1 for 5VSB shake when G3 to S5	26
		7. Nvidia release Load R145 for H_FERR#	04
1.1	2007.1210	1. EMI Solution Add C380,C381,C382 from 1.3V to GND (Reduce 500MHz noise) Add 2 via (Reduce 800MHz~900MHz noise) Add C559,C560(103P) 5VDIMM to GND；C65 modify to 103P (Reduce 833~900Mhz noise) Add C561,C562(103P) 5VDIMM_IN to GND；C59 modify to 103P (Reduce 833~900Mhz noise) Add C565(103P) VCC_DDR to GND；C76,C72 modify to 103P (Reduce 633MHz~666MHz noise) C172,C136.C159, C171 modify to 100PF C131, C150, C129, C156, C149, C 151 modify to 47PF (Reduce 830MHz~890MHz noise)	10,15,26,27
1.1	2007.1210	2. Nvidia release about Vccddr and Vttddr Add and load C373,C374,C375,C376,C377,C383,C384 C71,C365,C367,C369,C370,C371,C372 C385,C386,C388,C389,C392	10
		3. Remove C551 For system fan OP control issue The C551 let the OP control noise on SMPS. System current on 12V rise up to 35A when system fan control runs, and system fan voltage varied 3 to 7V in idle status.	21
		4. Load C358 4.7u For 5VSB rise current to 3.6A when G3 TO S5 The C358 can let the rise current under 2.7A, it can keep power supply pk current spec.	24

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